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Application Number: 16126947

Document Date: 09/10/2018

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Form Revision Date: August 26, 2013

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UTILITY PATENT APPLICATION TRANSMITTAL <i>(Only for new nonprovisional applications under 37 CFR 1.53(b))</i>		Attorney Docket No. 4123.0480002	
		First Named Inventor Jifeng ZHU	
		Title See 1 in Addendum	
		Priority Mail Express® Label No.	

APPLICATION ELEMENTS <i>See MPEP chapter 600 concerning utility patent application contents.</i>	Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450
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1. ☐ Fee Transmittal Form (PTO/SB/17 or equivalent) 2. ☐ Applicant asserts small entity status. See 37 CFR 1.27 3. ☐ Applicant certifies micro entity status. See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent. 4. ☒ Specification [Total Pages <u>25</u>] Both the claims and abstract must start on a new page. (See MPEP § 608.01(a) for information on the preferred arrangement) 5. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets <u>13</u>] 6. Inventor's Oath or Declaration [Total Pages _____] (including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e)) a. ☐ Newly executed (original or copy) b. ☐ A copy from a prior application (37 CFR 1.63(d)) 7. ☒ Application Data Sheet * See note below. See 37 CFR 1.76 (PTO/AIA/14 or equivalent) 8. CD-ROM or CD-R in duplicate, large table, or Computer Program (Appendix) ☐ Landscape Table on CD 9. Nucleotide and/or Amino Acid Sequence Submission (if applicable, items a. – c. are required) a. ☐ Computer Readable Form (CRF) b. ☐ Specification Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statements verifying identity of above copies	ACCOMPANYING APPLICATION PAPERS 10. ☐ Assignment Papers (cover sheet & document(s)) Name of Assignee <u>Yangtze Memory Technologies Co., Ltd.</u> 11. ☐ 37 CFR 3.73(c) Statement ☒ Power of Attorney (when there is an assignee) 12. ☐ English Translation Document (if applicable) 13. ☐ Information Disclosure Statement (PTO/SB/08 or PTO-1449) ☐ Copies of citations attached 14. ☐ Preliminary Amendment 15. ☐ Return Receipt Postcard (MPEP § 503) (Should be specifically itemized) 16. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed) 17. ☐ Nonpublication Request Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent. 18. ☒ Other: <u>Authorization under 37 CFR 1.136(a)(3)</u>
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***Note:** (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
 (2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS			
☒ The address associated with Customer Number: <u>26111</u> OR ☐ Correspondence address below			
Name _____			
Address _____			
City _____	State _____	Zip Code _____	
Country _____	Telephone _____	Email _____	
Signature <u>/Donald J. Featherstone/</u>		Date <u>9/10/18</u>	
Name (Print/Type) <u>Donald J. Featherstone</u>		Registration No. (Attorney/Agent) <u>33,876</u>	

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

9960940

Addendum

1. WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: ZHU *et al.*

Applicant: Yangtze Memory Technologies
Co., Ltd.

Application No.: *To Be Assigned*

(Continuation of Appl. No.
PCT/CN2018/101308; Filed: August 20,
2018)

Filed: *Herewith*

Confirmation No.: *To Be Assigned*

Art Unit: *To Be Assigned*

Examiner: *To Be Assigned*

Atty. Docket: 4123.0480002

Title: **WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY
DEVICES AND FABRICATION METHODS THEREOF**

**Authorization to Treat a Reply as Incorporating an
Extension of Time Under 37 C.F.R. § 1.136(a)(3)**

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

The U.S. Patent and Trademark Office is hereby authorized to treat any concurrent or future reply that requires a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. The U.S. Patent and Trademark Office is hereby authorized to charge all required extension of time fees to our Deposit Account No. 19-0036, if such fees are not otherwise provided for in such reply.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 9/10/18

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600
9960941_1.docx

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480002
		Application Number	
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Jifeng		ZHU		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Wuhan, Hubei	Country of Residence ⁱ	CN		
Mailing Address of Inventor:					
Address 1	Yangtze Memory Technologies Co., Ltd.				
Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone				
City	Wuhan, Hubei	State/Province			
Postal Code		Country ⁱ	CN		
Inventor 2					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Zhenyu		LU		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Wuhan, Hubei	Country of Residence ⁱ	CN		
Mailing Address of Inventor:					
Address 1	Yangtze Memory Technologies Co., Ltd.				
Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone				
City	Wuhan, Hubei	State/Province			
Postal Code		Country ⁱ	CN		
Inventor 3					Remove
Legal Name					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480002
		Application Number	
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jun		CHEN	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				

City	Wuhan, Hubei	Country of Residence ⁱ	CN
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Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.		
Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone		
City	Wuhan, Hubei	State/Province	
Postal Code		Country ⁱ	CN

Inventor 4	Remove
Legal Name	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Si Ping		HU	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				

City	Wuhan, Hubei	Country of Residence ⁱ	CN
------	--------------	-----------------------------------	----

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.		
Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone		
City	Wuhan, Hubei	State/Province	
Postal Code		Country ⁱ	

Inventor 5	Remove
Legal Name	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Xiaowang		DAI	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				

City	Wuhan, Hubei	Country of Residence ⁱ	CN
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Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.		
Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone		
City	Wuhan, Hubei	State/Province	
Postal Code		Country ⁱ	CN

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480002
		Application Number	
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		

Inventor 6 Remove				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Lan		YAO	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Wuhan, Hubei	Country of Residence ⁱ	CN	

Mailing Address of Inventor:				
Address 1		Yangtze Memory Technologies Co., Ltd.		
Address 2		18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone		
City	Wuhan, Hubei	State/Province		
Postal Code		Country ⁱ	CN	

Inventor 7 Remove				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Li Hong		XIAO	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Wuhan, Hubei	Country of Residence ⁱ	CN	

Mailing Address of Inventor:				
Address 1		Yangtze Memory Technologies Co., Ltd.		
Address 2		18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone		
City	Wuhan, Hubei	State/Province		
Postal Code		Country ⁱ	CN	

Inventor 8 Remove				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	A Man		ZHENG	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Wuhan, Hubei	Country of Residence ⁱ	CN	

Mailing Address of Inventor:				
Address 1		Yangtze Memory Technologies Co., Ltd.		
Address 2		18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone		

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		4123.0480002	
		Application Number			
Title of Invention		WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF			

City	Wuhan, Hubei		State/Province		
Postal Code			Country ⁱ	CN	
Inventor 9					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Kun		BAO		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Wuhan, Hubei		Country of Residence ⁱ	CN	
Mailing Address of Inventor:					
Address 1		Yangtze Memory Technologies Co., Ltd.			
Address 2		18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone			
City	Wuhan, Hubei		State/Province		
Postal Code			Country ⁱ	CN	
Inventor 10					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Haohao		YANG		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Wuhan, Hubei		Country of Residence ⁱ	CN	
Mailing Address of Inventor:					
Address 1		Yangtze Memory Technologies Co., Ltd.			
Address 2		18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone			
City	Wuhan, Hubei		State/Province		
Postal Code			Country ⁱ	CN	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.					

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).	
☐ An Address is being provided for the correspondence information of this application.	
Customer Number	26111
Email Address	Add Email Remove Email

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480002
		Application Number	
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		

Application Information:

Title of the Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		
Attorney Docket Number	4123.0480002	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	13	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	26111		

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480002
		Application Number	
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	PCT/CN2018/101308	2018-08-20

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)ⁱ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	
201710774754.6	CN	2017-08-31	Access Code ⁱ (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480002
		Application Number	
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480002
		Application Number	
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.			
Applicant 1			
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.			
Clear			
☐ Assignee	☐ Legal Representative under 35 U.S.C. 117		☐ Joint Inventor
☒ Person to whom the inventor is obligated to assign.		☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor:			
If the Applicant is an Organization check here. ☒			
Organization Name	Yangtze Memory Technologies Co., Ltd.		
Mailing Address Information For Applicant:			
Address 1	18 Gaoxin 4th Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan, Hubei	State/Province	
Country	CN	Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480002
		Application Number	
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		

Assignee 1			
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.			
If the Assignee or Non-Applicant Assignee is an Organization check here. ☒			
Organization Name	Yangtze Memory Technologies Co., Ltd.		
Mailing Address Information For Assignee including Non-Applicant Assignee:			
Address 1	18 Gaoxin 4th Road		
Address 2	East Lake High-Tech Development Zone		
City	Wuhan, Hubei	State/Province	
Country ⁱ	CN	Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.			

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Donald J. Featherstone/		Date (YYYY-MM-DD)	2018-09-10
First Name	Donald	Last Name	Featherstone	Registration Number
33,876				
Additional Signature may be generated within this form by selecting the Add button.				

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480002
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Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

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WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF

CROSS-REFERENCE TO RELATED APPLICATIONS AND INCORPORATION BY REFERENCE

[0001] This application claims priority to Chinese Patent Application No. 201710774754.6, filed on August 31, 2017 and PCT Patent Application No. PCT/CN2018/101308, filed on August 20, 2018, which are incorporated herein by reference in their entirety.

TECHNICAL FIELD

[0002] The present disclosure generally relates to the field of semiconductor technology, and more particularly, to a method for forming a three-dimensional (3D) memory device.

BACKGROUND

[0003] Planar memory cells are scaled to smaller sizes by improving process technology, circuit design, programming algorithm, and fabrication process. However, as feature sizes of the memory cells approach a lower limit, planar process and fabrication techniques become challenging and costly. As such, memory density for planar memory cells approaches an upper limit. A three-dimensional (3D) memory architecture can address the density limitation in planar memory cells.

BRIEF SUMMARY

[0004] Embodiments of a word line contact structure for three-dimensional (3D) memory array and methods for forming the same are described in the present disclosure.

[0005] In some embodiments, a method for forming a 3D memory structure is described. The method includes forming a stack of films on a substrate. The stack of films includes a plurality of alternately-arranged oxide and nitride layers. The method also includes etching the stack of films to form a staircase structure. The method further includes forming a second oxide layer on the stack of films. The method includes forming an etch-stop layer on the top surface of the second oxide layer of the staircase structure.

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- [0006] The method further includes disposing a filling material on the etch-stop layer of the staircase structure. The filling material can be a third oxide layer. Using chemical-mechanical-polishing (CMP) processes, for example, the top surface of the third oxide layer over each level of staircase structure is made coplanar with the top surface of the uppermost portion of the etch-stop layer.
- [0007] The method also includes etching through the stack of films, from the top surface of the uppermost etch-stop layer down to the substrate surface, to form openings that expose the substrate. Through these openings, nitride layers of the staircase structure can be removed and replaced by high-k dielectric materials and metal films.
- [0008] The method also includes etching the third oxide layer with highly selective etching and exposing the etch-stop layer of each level of the staircase structure for vertical interconnect access (VIA). The method also includes removing exposed etch-stop layer in the openings of contact VIAs by reverse selective etching and further exposing the second oxide layer on each level of the staircase structure. The method includes removing the exposed second oxide layer and high-k dielectric material in the openings of contact VIAs and exposing the metal film of each level of the staircase structure. The method also includes forming metallic connections to the metal film of each level of the staircase structure through subsequent metal filling and polishing.
- [0009] In some embodiments, the etch-stop layer can include silicon nitride.
- [0010] In some embodiments, the metal film surrounded by high-k dielectric material can include tungsten.
- [0011] In some embodiments, the high-k dielectric material can include hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide films, or a combination thereof.
- [0012] In some embodiments, the 3D memory structure can be formed with any one of the processes stated above.
- [0013] In some embodiments, a 3D memory structure includes a substrate and a film stack having a plurality of alternately-arranged first oxide and metal films surrounded by high-k dielectric layers. The film stack has a staircase shape and is formed on the surface of the substrate. The 3D memory structure further includes a second oxide layer, also in the shape of staircase, over the film stack of the staircase structure. The 3D memory structure also

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includes an etch-stop film, in the shape of staircase, over the second oxide layer of the staircase structure. The 3D memory structure further includes a third oxide film formed on the etch-stop layer. A top surface of the third oxide film is formed coplanar with a top surface of the uppermost portion of etch-stop layer over the staircase structure. The 3D memory structure further includes openings for vertical interconnect access (VIA) that extend through the third oxide layer, the etch-stop film, the second oxide layer, and the high-k dielectric layers to expose the metal film. The 3D memory structure further includes contact openings that extend through the staircase structure that expose the substrate to facilitate the formation of contacts.

[0014] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the pertinent art to make and use the present disclosure.

[0016] Fig. 1 illustrates a cross-sectional view of a staircase structure with a stack of films including a plurality of alternately insulating layers and sacrificial layers, in accordance with some embodiments of the present disclosure.

[0017] Fig. 2 illustrates a cross-sectional view of a staircase structure and an insulating layer formed on the staircase structure, in accordance with some embodiments of the present disclosure.

[0018] Fig. 3 illustrates a cross-sectional view of a staircase structure and an etch-stop layer formed on the staircase structure, in accordance with some embodiments of the present disclosure.

[0019] Fig. 4 illustrates a cross-sectional view of a staircase structure filled with an insulating material, in accordance with some embodiments of the present disclosure.

[0020] Fig. 5A and 5B illustrate cross-sectional views of a staircase structure having alternately-arranged insulating and gate materials, in accordance with some embodiments of the present disclosure.

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- [0021] Fig. 6 illustrates a cross-sectional view of a staircase structure after the etching of the insulating films, in accordance with some embodiments of the present disclosure.
- [0022] Fig. 7 illustrates a cross-sectional view of a staircase structure after the etching of an etch-stop layer and exposing of an insulating layer, in accordance with some embodiments of the present disclosure.
- [0023] Fig. 8A and 8B illustrate cross-sectional views of a staircase structure after the etching of an insulating layer and a high-k dielectric layer, in accordance with some embodiments of the present disclosure.
- [0024] Fig. 9A and 9B illustrate cross-sectional views of a staircase structure after the filling of openings with a conductive film, in accordance with some embodiments of the present disclosure.
- [0025] Fig. 10 illustrates a process flow for forming multi-level contacts in a 3D memory structure, in accordance with some embodiments of the present disclosure.
- [0026] The features and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings, in which like reference characters identify corresponding elements throughout. In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the corresponding reference number.
- [0027] Embodiments of the present disclosure will be described with reference to the accompanying drawings.

DETAILED DESCRIPTION

- [0028] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the pertinent art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the pertinent art that the present disclosure can also be employed in a variety of other applications.
- [0029] It is noted that references in the specification to “one embodiment,” “an embodiment,” “an example embodiment,” “some embodiments,” etc., indicate that the

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embodiment described can include a particular feature, structure, or characteristic, but every embodiment can not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to affect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

[0030] In general, terminology can be understood at least in part from usage in context. For example, the term “one or more” as used herein, depending at least in part upon context, can be used to describe any feature, structure, or characteristic in a singular sense or can be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as “a,” “an,” or “the,” again, can be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term “based on” can be understood as not necessarily intended to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0031] It should be readily understood that the meaning of “on,” “above,” and “over” in the present disclosure should be interpreted in the broadest manner such that “on” not only means “directly on” something, but also includes the meaning of “on” something with an intermediate feature or a layer therebetween. Moreover, “above” or “over” not only means “above” or “over” something, but can also include the meaning it is “above” or “over” something with no intermediate feature or layer therebetween (i.e., directly on something).

[0032] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” and the like, can be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or process step in addition to the orientation depicted in the figures. The apparatus can be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein can likewise be interpreted accordingly.

[0033] As used herein, the term “substrate” refers to a material onto which subsequent material layers are added. The substrate includes a top surface and a bottom surface. The top

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surface of the substrate is where a semiconductor device is formed, and therefore the semiconductor device is formed at a top side of the substrate. The bottom surface is opposite to the top surface and therefore a bottom side of the substrate is opposite to the top side of the substrate. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0034] As used herein, the term “layer” refers to a material portion including a region with a thickness. A layer has a top side and a bottom side where the bottom side of the layer is relatively close to the substrate and the top side is relatively away from the substrate. A layer can extend over the entirety of an underlying or overlying structure, or can have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any set of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductor and contact layers (in which contacts, interconnect lines, and/or vias are formed) and one or more dielectric layers.

[0035] As used herein, the term “nominal/nominally” refers to a desired, or target, value of a characteristic or parameter for a component or a process step, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term “about” indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term “about” can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., $\pm 10\%$, $\pm 20\%$, or $\pm 30\%$ of the value).

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[0036] In the present disclosure, the term “horizontal/horizontally/lateral/laterally” means nominally parallel to a lateral surface of a substrate. In the present disclosure, the term “each” may not only necessarily mean “each of all,” but can also mean “each of a subset.”

[0037] As used herein, the term “3D memory device” refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as “memory strings,” such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term “vertical/vertically” means nominally perpendicular to the lateral surface of a substrate.

[0038] In some embodiments, a NAND string or a 3D memory device includes a semiconductor pillar (e.g., silicon pillar) that extends vertically through a plurality conductor/dielectric layer pairs. The plurality of conductor/dielectric layer pairs are also referred to herein as an “alternating conductor/dielectric stack.” The conductor layer of the alternating conductor/dielectric stack can be used as a word line (electrically connecting one or more control gates). An intersection of a word line and the semiconductor pillar forms a memory cell. Vertically-oriented memory strings require an electrical connection between the conductors materials (e.g., word line plates or control gates) and access lines (e.g., back end of line interconnection) so that each of the memory cells along the memory strings or in the 3D memory device can be uniquely selected for writing or reading functions. One method of forming electrical connections includes forming a staircase structure on an alternating conductor/dielectric stack.

[0039] As the demand for higher storage capacity continues to increase, the number of vertical levels of the memory cells and staircase structures also increases. Accordingly, it is challenging to balance the manufacturing throughput and the process complexity/cost.

[0040] Lithography and etching processes can be used to open contact areas for forming electrical connection to the conductive layer on each level of the staircase structure. Due to topology of staircase structures, depth of the contact hole from the top surface to each level of the staircase depends on the location of each level. For example, contact holes for lower levels may be deeper than contact holes for upper levels. Typically, all of the contact holes are formed with a single lithography mask and etching process. Often, before contact holes to the bottom levels are entirely formed, the materials exposed in contact holes at the upper

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levels are over-etched and lost. To resolve this issue, two or more lithography masks are used to separate etching processes, which adds cost and complexity to the fabrication process.

[0041] Various embodiments in the present disclosure provide methods and structures for improving word line contacts for 3D memory devices. In the present disclosure, a single lithography mask can be used to form contact areas for word lines of 3D memory array. By adding an etch-stop film over the staircase structure, openings of the vertical interconnect access (VIA) contacts for each level of the staircase structure can be formed simultaneously. The etch-stop film protects underlying layers during etching processes that form contact VIAs. The etch-stop film is exposed on each level of the staircase structure by a selective etching process, and then removed by reverse selective etching. Accordingly, the disclosed methods and structures can improve fabrication yield and reduce cost. The methods and structures described herein can be used to form semiconductor interconnect structures for inter-connecting components at different layers with an uneven topology.

[0042] Fig. 1 illustrates a staircase structure 100 having an alternating layer stack on a top surface of a substrate 101. Each staircase step includes a staircase layer (SC layer) 102, wherein the SC layer 102 includes an exposed top surface 102T and a side surface 102S. Each SC layer 102 includes a first insulating layer 104 and a sacrificial layer 106. The bottommost and the uppermost material of the staircase structure 100 can include the first insulating layer 104.

[0043] In some embodiments, the substrate 101 includes any suitable material for supporting the 3D memory structure. For example, the substrate 101 can include silicon, silicon germanium, silicon carbide, silicon on insulator (SOI), germanium on insulator (GOI), glass, gallium nitride, gallium arsenide, any suitable III-V compounds, any other suitable material, and/or combinations thereof.

[0044] In some embodiments, the first insulating layer 104 can include any suitable insulating materials, for example, silicon oxide, silicon oxynitride, silicon nitride, TEOS, aluminum oxide, or silicon oxide with F-, C-, N-, and/or H- incorporation.

[0045] In some embodiments, the sacrificial layer 106 includes any suitable material that is different from the first insulating layer 104 and can be removed selectively. For example, the sacrificial layer 106 can include silicon oxide, silicon oxynitride, silicon nitride, TEOS, polycrystalline silicon, polycrystalline germanium, polycrystalline germanium-silicon, and/or

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combinations thereof. In some embodiments, the sacrificial layer 106 also includes amorphous semiconductor materials, such as amorphous silicon or amorphous germanium.

[0046] In some embodiments, the first insulating layer 104 can be silicon oxide and the sacrificial layer 106 can be silicon nitride.

[0047] In some embodiments, a thickness of the first insulating layer 104 or the sacrificial layer 106 can be between about 10 nm and about 200 nm. In some embodiments, a thickness of the SC layer 102 can be different for each staircase level.

[0048] The formation of the first insulating layer 104 and the sacrificial layer 106 can include any suitable deposition methods such as, chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma-enhanced CVD (PECVD), low pressure chemical vapor deposition (LPCVD), sputtering, metal-organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), any other suitable deposition method, and/or combinations thereof. In some embodiments, poly-crystalline semiconductor material can be deposited in an amorphous state and converted to poly-crystalline through subsequent thermal treatments.

[0049] The plural steps of the staircase structure 100 is formed by applying a repetitive etch-trim process on the disposed film stacks using a mask stack (not shown). In some embodiments, the mask stack can include a photoresist or carbon-based polymer material. In some embodiments, the mask stack is removed after forming the staircase structure 100.

[0050] The etch-trim process includes an etching process and a trimming process. During the etching process, the portion of SC layer 102 with exposed top surface 102T are removed. The etch depth is a thickness of the SC layer 102. The etching process for the first insulating layer 104 can have a high selectivity over the sacrificial layer 106, and/or vice versa. Accordingly, an underlying SC layer 102 can function as an etch-stop layer. As a result, one staircase step is formed during each etch-trim cycle.

[0051] In some embodiments, the SC layer 102 can be etched using an anisotropic etching such as a reactive ion etch (RIE) or other dry etch processes. In some embodiments, the etchant can include fluorine based gases such as, for example, carbon-fluorine (CF₄) based gases, hexafluoroethane (C₂F₆) based gases, and/or any other suitable gases. In some embodiments, the SC layer 102 can be removed by wet chemistry, such as hydrofluoric acid or a mixture of hydrofluoric acid and ethylene glycol. In some embodiments, a timed etching

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approach can be used. The methods and etchants to remove a single layer stack should not be limited by the embodiments of the present disclosure.

[0052] The trimming process includes applying a suitable etching process (e.g., an isotropic dry etch or a wet etch) on the mask stack such that the mask stack can be pulled back laterally. The lateral pull-back dimension determines the lateral dimension “a” of each step of the staircase structure 100, as illustrated in Fig. 1. After mask stack trimming, one portion of the topmost SC layer 102 is exposed and the other portion of the topmost SC layer 102 remains covered by the mask stack. The next cycle of etch-trim process resumes with the etching process.

[0053] In some embodiments, the mask stack trimming process can include dry etching, such as RIE using O₂, Ar, N₂, etc.

[0054] In some embodiments, the topmost SC layer 102 can be covered by the first insulating layer 104. A process step of removing the first insulating layer 104 can be added to the etching process of each etch-trim cycle to form the staircase structure 100.

[0055] Referring to Fig. 2, a staircase structure 200 is formed by disposing a second insulating layer 208 on the staircase structure 100. The second insulating layer 208 covers the staircase structure 100, including a top surface 102T and a side surface 102S of each SC layer 102 (shown in Fig. 1). In some embodiments, the second insulating layer 208 can be an optional barrier layer. For example, the second insulating layer 208 can be used as a barrier layer for protecting the underlying structure during subsequent etching processes. In some embodiments, thicknesses of the second insulating layer 208 can be about the same on a side surface 102S and a top surface 102T. In some embodiments, thickness of the second insulating layer 208 on the side surface 102S can be thicker or thinner than that on the top surface 102T. In some embodiments, a thickness of the second insulating layer 208 can be in a range between 1 nm to 200 nm (e.g., 1 nm, 2 nm, 3 nm, 4 nm, 5 nm, 6 nm, 7 nm, 8 nm, 9 nm, 10 nm, 20 nm, 40 nm, 50 nm, 60 nm, 80 nm, 90 nm, 100 nm, 140 nm, 160 nm, 170 nm, 200 nm, any range bounded by the lower end by any of these values, or in any range defined by any two of these values). In some embodiments, the second insulating layer 208 can be made of similar material as the first insulating layer 104. In some embodiments, the second insulating layer 208 can be formed using similar techniques as the processes used to form the first insulating layer 104.

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[0056] Referring to Fig. 3, a staircase structure 300 is formed by disposing an etch-stop layer 310 on the staircase structure 200. A thickness of the etch-stop layer 310 can be in a range between 10 nm to 1000 nm (e.g., 10 nm, 20 nm, 30 nm, 40 nm, 50 nm, 60 nm, 70 nm, 80 nm, 90 nm, 100 nm, 200 nm, 300 nm, 400 nm, 500 nm, 600 nm, 700 nm, 800 nm, 900 nm, 1000 nm, any range bounded by the lower end by any of these values, or in any range defined by any two of these values). The etch-stop layer 310 can be made of any suitable insulating material that is different from the second insulating layer 208. In some embodiments, the etch-stop layer 310 can be disposed on the second insulating layer 208. In some embodiments, the second insulating layer 208 is optional and the etch-stop layer 310 can be directly disposed on the staircase structure 100. In some embodiments, the etch-stop layer 310 can cover the staircase structure 200, including the top surface 102T and the side surface 102S of each SC layer 102. In some embodiments, the thickness of the etch-stop layer 310 on a side surface 102S can be the same as that on a top surface 102T. In some embodiments, the thickness of the etch-stop layer 310 on the side surface 102S can be thicker or thinner than that on the top surface 102T. In some embodiments, etch-stop layer 310 can be made of silicon nitride, silicon oxynitride, spin-on-dielectric, and/or high-k dielectric films such as hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, or lanthanum oxide films. In some embodiments, etch-stop layer 310 can be disposed by any suitable methods such as CVD, PVD, PECVD, LPCVD, sputtering, MOCVD, ALD, spin-coating, or any other suitable deposition method, and/or combinations thereof.

[0057] Referring to Fig. 4, a staircase structure 400 is formed by disposing a third insulating layer 420 over the staircase structure 300, with a top surface 420S being coplanar with the top surface 310S of the uppermost portion of the etch-stop layer 310. The third insulating layer 420 can be made of any a suitable insulator that is different from the etch-stop layer 310. In some embodiments, the third insulating layer 420 is made of a similar material as the first insulating layer 104. In some embodiments, the forming of the third insulating layer 420 can use similar techniques as forming the first insulating layer 104. In some embodiments, the forming of the third insulating layer 420 can use any suitable processes such as, for example, a spin-coating process, CVD or high density plasma (HDP) deposition. In some embodiments, the forming of the third insulating layer 420 further includes a planarization

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process such as chemical-mechanical planarization (CMP). In some embodiments, the third insulating layer 420 can cover each step of the staircase structure 300.

[0058] Referring to Fig. 5A, a substrate opening 522 is formed in a staircase structure 500 by etching through the entire film stack of the staircase structure 400, exposing the surface of the substrate 101. (Although Figs. 5A and 5B illustrate one substrate opening 522, it is noted that, the location, shape, total number, and arrangement of the substrate opening 522, relative to the staircase structure 400, is only used for illustration purpose in the present disclosure, which does not limit the scope of the present disclosure.)

[0059] In some embodiments, through the substrate opening 522, the sacrificial layer 106 of each SC layer 102 in the staircase structure 400 is removed and replaced by a gate stack 525. The staircase structure 500 includes a plurality of replacement SC layers 526, wherein the replacement SC layer 526 includes the first insulating layer 104 and the gate stack 525. The first insulating layer 104 and the gate stack 525 are alternatingly arranged in the staircase structure 500.

[0060] In some embodiments, removing the sacrificial layer 106 includes wet etching or isotropic dry etching that is selective to the first insulating layer 104. For example, the etching rate of the first insulating layer 104 is slower than the etching rate of the sacrificial layer 106. In some embodiments, removing the sacrificial layer 106 is also selective to the second insulating layer 208. In some embodiments, the second insulating layer 208 is optional, and removing the sacrificial layer 106 is selective to the etch-stop layer 310.

[0061] Fig. 5B illustrates the details of a region 527 in Fig. 5A, in accordance with some embodiments of the present disclosure. The gate stack 525 can include a high-k dielectric layer 525H and a gate conductive layer 525M. The gate conductive layer 525M is surrounded by the high-k dielectric layer 525H, with one side next to the substrate opening 522.

[0062] In some embodiments, the high-k dielectric layer 525H can include hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, or lanthanum oxide films, and/or any combination thereof. The high-k dielectric layer 525H can be disposed by any suitable methods such as CVD, PVD, PECVD, LPCVD, MOCVD, ALD, and/or combinations thereof.

[0063] In some embodiments, the gate conductive layer 525M can be made from a metal, such as tungsten, cobalt, nickel, copper, or aluminum, and/or combinations thereof. The

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metal can be formed by any suitable deposition methods, for example, sputtering, thermal evaporation, e-beam evaporation, ALD, PVD, and/or combinations thereof.

[0064] In some embodiments, the gate conductive layer 525M can also be poly-crystalline semiconductors, such as poly-crystalline silicon, poly-crystalline germanium, poly-crystalline germanium-silicon and any other suitable material, and/or combinations thereof. In some embodiments, the poly-crystalline material can be incorporated with any suitable types of dopant, such as boron, phosphorous, or arsenic, and in the form of elements or a compound. In some embodiments, the gate conductive layer 525M can also be amorphous semiconductors.

[0065] In some embodiments, the gate conductive layer 525M can be made from a metal silicide, including WSi_x , $CoSi_x$, $NiSi_x$, or $AlSi_x$, etc. The forming of the metal silicide material can include forming a metal layer and a poly-crystalline semiconductor using similar techniques described above. The forming of metal silicide can further include applying a thermal annealing process on the deposited metal layer and the poly-crystalline semiconductor layer, followed by removal of unreacted metal.

[0066] In some embodiments, the gate stack 525 includes an interface material between the high-k dielectric layer 525H and the gate conductive layer 525M. The interface material can include silicon oxide or silicon oxynitride, etc.

[0067] The portion of the gate conductive layer 525M located on the sidewalls of the substrate opening 522 (not illustrated in Fig. 5A or 5B for simplicity), can be removed and replaced by a fifth insulating layer 530. Removal of sidewall portions of gate conductive layer 525M can be achieved by wet-etching or dry-etching. In some embodiments, the fifth insulating layer 530 can be made of the same material as the first insulating layer 104 or the etch-stop layer 310, and formed by similar techniques. In some embodiments, a portion of the fifth insulating layer 530 can be removed from the top surface of substrate 101 and the substrate surface can be exposed for electrical contacts in the subsequent processes. Removing the fifth insulating layer 530 from the substrate surface can be achieved by, for example, anisotropic dry-etching.

[0068] Referring now to Fig. 6, a staircase structure 600 includes vertical interconnect access (VIA) openings 640 for each replacement SC layer 526. In some embodiments, photoresist or polymer material can be used as a mask layer (not shown in the figure). A selective etching

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process can be used such that the etching rate of the third insulating layer 420 is higher than the etching rate of the etch-stop layer 310. During the one or more etching processes that form the VIA openings 640, the etch-stop layer 310 protects the underlying structure until all the VIA openings 640 are formed throughout the staircase structure 600. For example, a VIA opening 640L for a lower replacement SC layer 526L requires longer etch time than a VIA opening 640U for an upper replacement SC layer 526U. An additional thickness H of the third insulating layer 420 needs to be removed. The etch-stop layer 310 can protect underlying materials of the replacement SC layers 526 on upper levels, before the VIA openings 640 are formed for the replacement SC layers 526 on lower levels. For example, during the removal process of the extra thickness H of third insulating layer 420, the etch-stop layer 310 on top of the upper replacement SC layer 526U is not etched through, with a remaining etch stop layer 310R. The remaining etch-stop layer 310R provides protection for the replacement SC layers 526U, where the VIA openings 640U are already formed. The staircase structure 600 is formed after the portion of the third insulating layer 420 inside all the VIA openings 640 are removed for each replacement SC layer 526. The VIA openings 640 extend through the third insulating layer 420 and expose the underlying etch-stop layer 310. In some embodiments, the etch-stop layer 310 can be partially etched in some VIA openings 640, as shown in Fig. 6. In some embodiments, the thickness of the etch-stop layer 310 remains substantially the same during the one or more etching processes that form the VIA openings 640, because etch-stop layer 310 can be inert to the etchant used in the etching processes. In some embodiments, the selective etching includes anisotropic dry etching using chemical etchant such as, for example, CF_4 , CHF_3 , C_2F_6 , or C_3F_8 , and/or other suitable etchants.

[0069] In some embodiments, prior to forming VIA openings 640, a second conductive material can be disposed inside the substrate opening 522 of the staircase structure 500 (see FIG. 5) to form a substrate conductive structure 643 (see FIG. 6). Accordingly, an electrical connection is provided to the substrate 101 from the surface of the staircase structure 600. In some embodiments, the substrate conductive structure 643 can be formed with any suitable conductive material that can be the same as or can be different from the gate conductive layer 525M, and can be disposed using similar techniques. Additional planarization process can be included to form a top surface coplanar with the top surface of the third insulating layer 420.

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[0070] Referring to Fig. 7, portions of the etch-stop layer 310 inside VIA openings 740 are removed by reverse selective etching. During reverse selective etching, the etch-stop layer 310 can be etched faster than the second insulating layer 208. In some embodiments, the reverse selective etching process includes anisotropic or isotropic dry etching using chemistry, for example, O₂, N₂, CF₄, NF₃, Cl₂, HBr, BCl₃, and/or combinations thereof. In some embodiments, the reverse selective etching process includes wet chemical etching, for example, phosphorus acid. A staircase structure 700 is formed after the portion of etch-stop layer 310 inside the VIA openings 740 is removed for each replacement SC layer 526.

[0071] Referring to Fig. 8A and 8B, a portion of the second insulating layer 208 and a portion of the high-k dielectric layer 525H in gate stack 525 are removed inside the VIA openings 840, forming VIA openings 840 that extend through the third insulating layer 420, the etch-stop layer 310, the second insulating layer 208, and the high-k dielectric layer 525H and exposing the gate conductive layer 525M. In some embodiments, the etching process for etching the second insulating layer 208 and the high-k dielectric layer 525H can be similar to that used for etching the third insulating layer 420 or the etch-stop layer 310. A staircase structure 800 includes a portion of gate conductive layer 525M, which is exposed inside the VIA openings 840 for each replacement SC layer 526, enabling gate contacts for every 3D memory cell.

[0072] In some embodiments, the second insulating layer 208 is optional and the etching of the etch stop layer 310 exposes the high-k dielectric layer 525H inside the VIA openings 740/840. The high-k dielectric layer 525H can be removed in the subsequent etching process to further expose the gate conductive layer 525M inside the VIA openings 740/840. The VIA openings 840 extend through the third insulating layer 420, etch-stop layer 310 and the high-k dielectric layer 525H, exposing the gate conductive layer 525M.

[0073] Referring to Fig. 9A and 9B, a staircase structure 900 includes disposing a third conductive material to form VIA conductive structures 945 in the VIA openings 840. The VIA conductive structures 945 can be formed by disposing a third conductive material in the formed openings 840 and directly on the exposed portions of gate conductive layer 525M. In some embodiments, the VIA conductive structures 945 are directly disposed on the exposed gate conductive layer 525M. In some embodiments, the VIA conductive structures 945 can be made from a similar material as the gate conductive layer 525M. In some embodiments,

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the VIA conductive structures 945 can be disposed using a similar technique as the gate conductive layer 525M. In some embodiments, the VIA conductive structures 945 can be coplanar with the third insulating layer 420 using a planarization process such as, for example, a CMP process. In the staircase structure 900, the VIA conductive structures 945 can extend through the third insulating layer 420, the etch-stop layer 310, the second insulating layer 208 and the gate dielectric layer 525H, directly contacting and electrically connecting to the gate conductive layer 525M for each corresponding replacement SC layer 526. As discussed above, the second insulating layer 208 can be optional and in such scenarios the VIA conductive structures 945 can extend through the third insulating layer 420, the etch-stop layer 310 and the gate dielectric layer 525H, directly contacting and connected to the gate conductive layer 525M for each corresponding replacement SC layer 526. Therefore, the electrical conductive path for gate stack 525 of each memory cell can be wired up to the surface of the wafer, enabling various configurations of word lines for the 3D memory in the back-of-line process.

[0074] Fig. 10 illustrates an exemplary method 1000 for forming the word line contacts for a three-dimensional memory array, according to some embodiments. The processing steps of the method 1000 can be used to form memory device structures illustrated in Figs. 1-9. The processing steps shown in method 1000 are not exhaustive and other processing steps can be performed as well before, after, or between any of the illustrated process steps. In some embodiments, some processing steps of exemplary method 1000 can be omitted or include other processing steps that are not described here for simplicity. In some embodiments, processing steps of method 1000 can be performed in a different order and/or vary.

[0075] At process step 1010, an alternating layer stack is disposed over a substrate, followed by a repetitive etch-trim process to form a staircase structure. An example of the substrate can be the substrate 101 described in Fig. 1. A layer stack within the alternating layer stack can include a dielectric layer pair with a first insulating layer over a sacrificial layer. The first insulating layer can be the first insulating layer 104 in Fig. 1 and the sacrificial layer can be the sacrificial layer 106 in Fig. 1, and the dielectric layer pair can be formed using similar techniques as the first insulating layer 104 and the sacrificial layer 106.

[0076] One cycle of the repetitive etch-trim process includes an etching process that etches a height of a staircase step and a trimming process that determines a width of a staircase step.

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The etch-trim process is repeated for a number of cycles, corresponding to the number of steps or the number of dielectric layer pairs on the staircase structure. A mask stack can be used for patterning and can be removed after the etch-trim process.

[0077] At process step 1020, a second insulating layer is disposed on the staircase structure with alternating film stacks. The second insulating layer can be the second insulating layer 208 in Fig. 2 and can be formed using a similar technique.

[0078] At process step 1030, an etch-stop layer is disposed on the top surface of the second insulating layer on the staircase structure. The etch-stop layer can be the etch stop layer 310 in Fig. 3, and can be formed using a similar technique.

[0079] At process step 1040, a third insulating layer is disposed on the top surface of the etch-stop layer over the staircase structure, followed by an optional planarization process, to form a surface coplanar with the uppermost portion of the etch-stop layer. The third insulating layer can be the third insulating layer 420 in Fig. 4, and can be formed using a similar technique.

[0080] At process step 1050, an opening to the substrate is formed by etching through the entire film stack. Through the opening, the sacrificial layer of each dielectric layer pair in the staircase structure is removed and replaced by a gate stack. A similar structure is shown in Fig. 5A and 5B. The gate stack can be the gate stack 525 in Fig. 5A and 5B. The opening to the substrate can be the substrate opening 522 in Fig. 5A. Removing the sacrificial layer includes wet etching or isotropic dry etching that is selective to the surrounding first and second insulating layer. Disposing the gate stack includes first disposing a high-k dielectric layer and then a gate conductive layer. The high-k dielectric layer can be the high-k dielectric layer 525H in Fig. 5B, and can be formed using a similar technique. The gate conductive layer can be the gate conductive layer 525M, and can also be formed using a similar technique.

[0081] Process step 1050 also includes removing the gate conductive layer (or the conductive portion) from the sidewalls of the substrate opening and forming an isolation barrier layer. Removing the gate conductive layer from the sidewall can be achieved by wet-etching or dry-etching. The sidewall isolation layer can be fifth insulating layer 530 in Fig. 5A and 5B, and can be formed using a similar technique. The sidewall isolation material deposited on the substrate surface at the bottom of the opening can be removed by anisotropic dry-etching.

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- [0082] At process step 1060, a second conductive material can be disposed over the staircase structure, forming a substrate conductive structure inside the substrate opening. The substrate conductive structure can be the substrate conductive structure 643 in Fig. 6. A planarization process, for example, chemical mechanical polishing, can be used to form coplanar top surfaces between the substrate conductive structure and the third insulating layer.
- [0083] At process step 1060, contact VIA openings are also formed for each staircase level with selective etching. The contact VIA openings can be the same VIA openings 640 in Fig. 6. The etching rate of the third insulating layer can be higher than the etching rate of the etch-stop layer. Therefore, deep openings can be made for the bottom staircase level, while the etch-stop layer is not punched through on the uppermost staircase level.
- [0084] At process step 1070, the etch-stop materials inside the VIA openings are removed by reverse selective etching. During reverse selective etching, the etch-stop layer can be etched faster than the second insulating layer. At this step, the VIA openings can be the VIA openings 740 in Fig. 7.
- [0085] At process step 1080, the second insulating layer and the high-k dielectric layer of the gate stack is removed inside the VIA openings, by using a similar etching process as that for the third insulating layer or the etch-stop layer. The conductive material of the gate stack is exposed inside the VIA openings, enabling electrical connections to the gate of every 3D memory cell. At this step, the VIA openings can be the VIA openings 840 in Fig. 8A and 8B.
- [0086] At process step 1090, VIA conductive structures are formed by disposing and filling a third conductive material in all the VIA openings in the structure. The VIA conductive structure can be the VIA conductive structures 945 in Fig. 9A and 9B. The third conductive material can be planarized subsequently to form a coplanar surface with the top surface of the third insulating layer. The planarization process includes chemical mechanical polishing (CMP). Residual conductive materials outside the VIA openings can be removed by touch-up dry etching or wet etching. As a result, the conductive material in the VIA openings is connected with the conductive material of the gate stack for each level of the staircase structure. Therefore, the embedded gates of the vertically stacked 3D memory cells can be electrically connected from a planar surface on the top of the structure in the subsequent back-of-line processes, enabling various configurations of word lines for the 3D memory array.

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[0087] Process steps 1010-1050 illustrate the formation of the staircase structure 500 in Fig. 5, in accordance with some embodiments of the present disclosure, using a replacement gate technique. In this example, the sacrificial layer 106 is formed first on the staircase structure 100 in Figs. 1 at process steps 1010. The sacrificial layer 106 can be replaced by the gate stack 525 at process step 1050 to form staircase structure 500. Detailed structure and method of 3D memory with replacement gate is described in co-pending U.S. patent application, titled "Method for Forming Gate Structure of Three-Dimensional Memory Device," (Application No. 16/047,158 and filed on July 27, 2018), which is incorporated herein by reference in its entirety.

[0088] In some embodiments, the staircase structure 500 can also be formed with a so called "gate-first" approach, where a gate conductive layer can be disposed in Fig. 1 and at process steps 1010, in place of the sacrificial layer 106. The gate conductive layer can be a similar material as the gate conductive layer 525M in Fig. 5B and can be formed using similar techniques. The etch-trim process to form the staircase structure 100 can be modified accordingly so that the gate conductive layer 525M can be etched instead of the sacrificial layer 106. As such, the sacrificial layer 106 in Figs. 2-4 can also be replaced by the gate conductive layer 525M. At process step 1050, the step of removing the sacrificial layer 106 can be skipped in this embodiment. The substrate opening 522, the VIA openings 640/740/840, and the conductive structures 643/945 can be formed similarly as the ones in Figs. 5-9 and using similar methods in process steps 1050-1090.

[0089] In some embodiments, a semiconductor structure includes a staircase structure having a plurality of steps, and each step includes a conductive layer disposed over a dielectric layer. The semiconductor structure further includes a barrier layer disposed over a portion of the conductive layer of the each step. The semiconductor structure also includes an etch-stop layer disposed on the barrier layer and an insulating layer disposed on the etch-stop layer. The semiconductor structure also includes a plurality of conductive structures formed in the insulating layer and extending through the etch-stop layer and the barrier layer. Each conductive structure directly contacts the conductive layer of the each step.

[0090] In some embodiments, a semiconductor structure includes a staircase structure having a plurality of steps, and each step includes a conductive layer disposed over a dielectric layer. The semiconductor structure further includes an etch-stop layer disposed over a portion of

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the conductive layer of the each step and an insulating layer disposed on the etch-stop layer. The semiconductor structure further includes a plurality of conductive structures formed in the insulating layer and extending through the etch-stop layer. Each of the conductive structure directly contacts the corresponding conductive layer of the each step.

[0091] In some embodiments, a method for forming a semiconductor structure includes forming a plurality of steps of a staircase structure. Forming each step of the plurality of steps includes disposing a sacrificial layer over a dielectric layer and disposing an etch-stop layer on each step of the plurality of steps. The method further includes disposing an insulating layer on the etch-stop layer and replacing the sacrificial layer with a conductive layer for each step of the staircase structure. The method also includes forming a plurality of openings in the insulating layer and exposing portions of the etch-stop layer. The method also includes etching the exposed portions of the etch-stop layer in the plurality of openings and exposing the conductive layer of each step. The method also includes forming a plurality of conductive structures and each conductive structure is respectively formed in each opening of the plurality of openings.

[0092] The foregoing description of the specific embodiments will so fully reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt, for various applications, such specific embodiments, without undue experimentation, and without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the disclosure and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the disclosure and guidance.

[0093] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

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[0094] The Summary and Abstract sections can set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0095] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A semiconductor structure, comprising:
 - a staircase structure comprising a plurality of steps, wherein each step comprises a conductive layer disposed over a dielectric layer;
 - a barrier layer disposed over a portion of the conductive layer of the each step;
 - an etch-stop layer disposed on the barrier layer;
 - an insulating layer disposed on the etch-stop layer; and
 - a plurality of conductive structures formed in the insulating layer, wherein each conductive structure is formed on the conductive layer of the each step.
2. The semiconductor structure of claim 1, wherein the plurality of conductive structures extend through the barrier layer.
3. The semiconductor structure of claim 1, wherein the plurality of conductive structures extend through the etch-stop layer.
4. The semiconductor structure of claim 1, wherein the barrier layer comprises silicon oxide.
5. The semiconductor structure of claim 1, wherein the etch-stop layer comprises one or more of silicon nitride, a spin-on-dielectric, and a high-k dielectric.
6. The semiconductor structure of claim 1, wherein the each conductive structure directly contacts a corresponding one of the conductive layer of the each step.
7. The semiconductor structure of claim 1, wherein top surfaces of the plurality of conductive structures, the insulating layer, and a portion of the etch-stop layer are coplanar.
8. The semiconductor structure of claim 1, wherein the plurality of conductive structures comprise one or more of tungsten, cobalt, nickel, copper, and aluminum.

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9. The semiconductor structure of claim 1, wherein the barrier layer is formed on side and top surfaces of the plurality of steps.
10. The semiconductor structure of claim 1, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.
11. A semiconductor structure, comprising:
 - a staircase structure comprising a plurality of steps, wherein each step comprises a conductive layer disposed over a dielectric layer;
 - an etch-stop layer disposed over a portion of the conductive layer of the each step;
 - an insulating layer disposed on the etch-stop layer; and
 - a plurality of conductive structures formed in the insulating layer and extending through the etch-stop layer, wherein each conductive structure directly contacts the corresponding conductive layer of each step.
12. The semiconductor structure of claim 11, wherein the etch-stop layer is formed on a side surface and a top surface of each step.
13. The semiconductor structure of claim 12, wherein thicknesses of the etch-stop layer is the same on the side and top surfaces of each step.
14. The semiconductor structure of claim 11, wherein the etch-stop layer comprises one or more of silicon nitride, a spin-on-dielectric, and a high-k dielectric.
15. The semiconductor structure of claim 11, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.
16. A method for forming a semiconductor structure, comprising:
 - forming a staircase structure having a plurality of steps, wherein the forming of each step of the plurality of steps comprises disposing a sacrificial layer over a dielectric layer;
 - disposing an etch-stop layer on each step of the plurality of steps;

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disposing an insulating layer on the etch-stop layer;
replacing the sacrificial layer of each step with a conductive layer;
forming a plurality of openings in the insulating layer exposing portions of the etch-stop layer;
etching the exposed portions of the etch-stop layer in the plurality of openings and exposing at least a portion of the conductive layer of each step; and
forming a plurality of conductive structures in each of the plurality of openings.

17. The method of claim 16, wherein the forming the plurality of openings comprises performing an etching process on the insulating layer, wherein an etching rate of the insulating layer is higher than an etching rate of the etch-stop layer.
18. The method of claim 16, wherein the etching the exposed portions of the etch-stop layer comprises etching the exposed etch-stop layer at a higher etching rate than an etching rate of the conductive layer.
19. The method of claim 16, wherein disposing an etch-stop layer comprises disposing one or more of silicon nitride, a spin-on-dielectric, and a high-k dielectric.
20. The method of claim 16, wherein forming the plurality of conductive structures comprises disposing conductive materials directly on the exposed conductive layer of the each step.

ABSTRACT

Embodiments of semiconductor structures including word line contact structures for three-dimensional memory devices and fabrication methods for forming word line contact structures are disclosed. The semiconductor structures include a staircase structure having a plurality of steps, and each step includes a conductive layer disposed over a dielectric layer. The semiconductor structures further include a barrier layer disposed over a portion of the conductive layer of each step. The semiconductor structures also include an etch-stop layer disposed on the barrier layer and an insulating layer disposed on the etch-stop layer. The semiconductor structures also include a plurality of conductive structures formed in the insulating layer and each conductive structure is formed on the conductive layer of each step.

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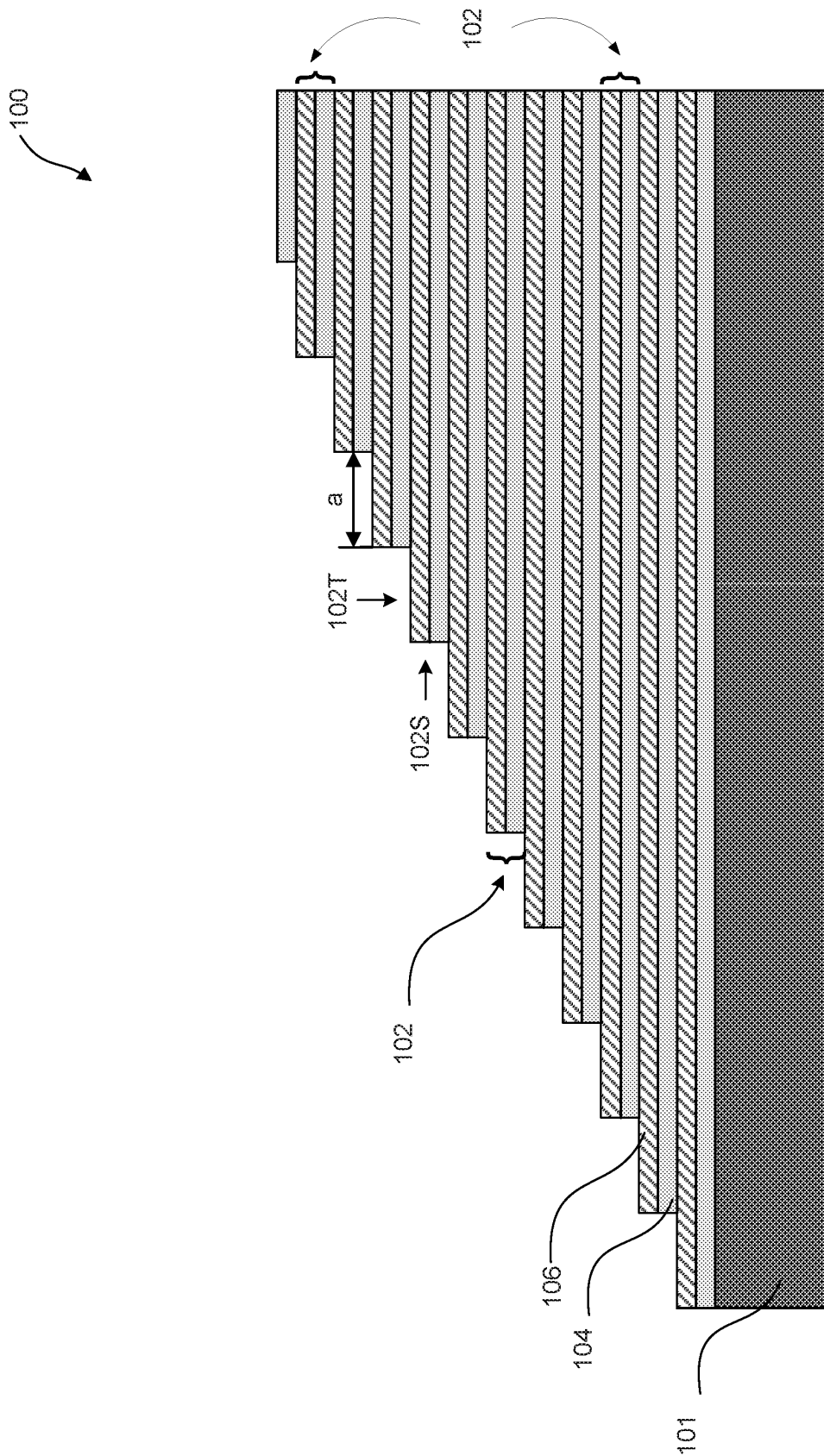


FIG. 1

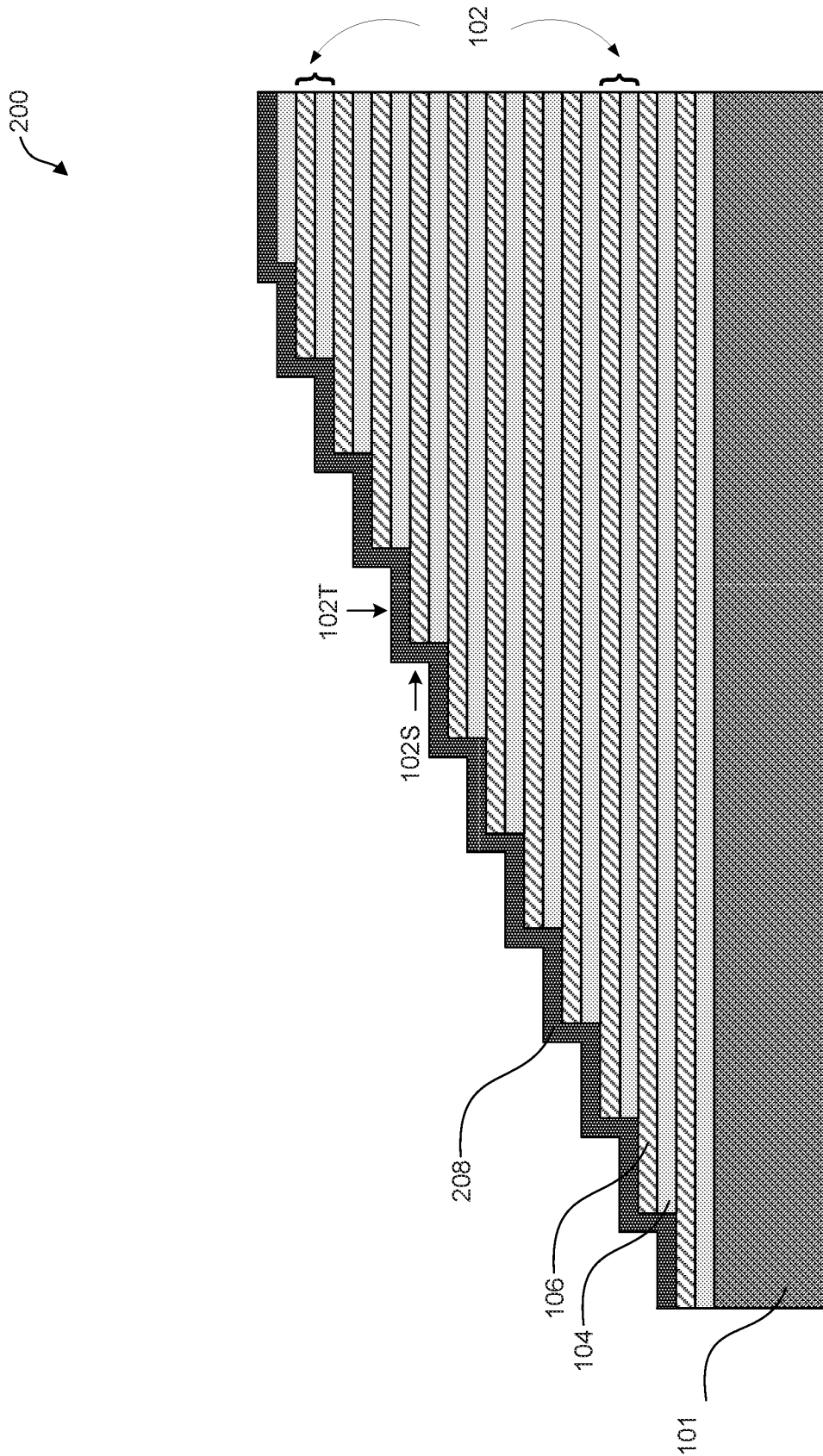


FIG. 2

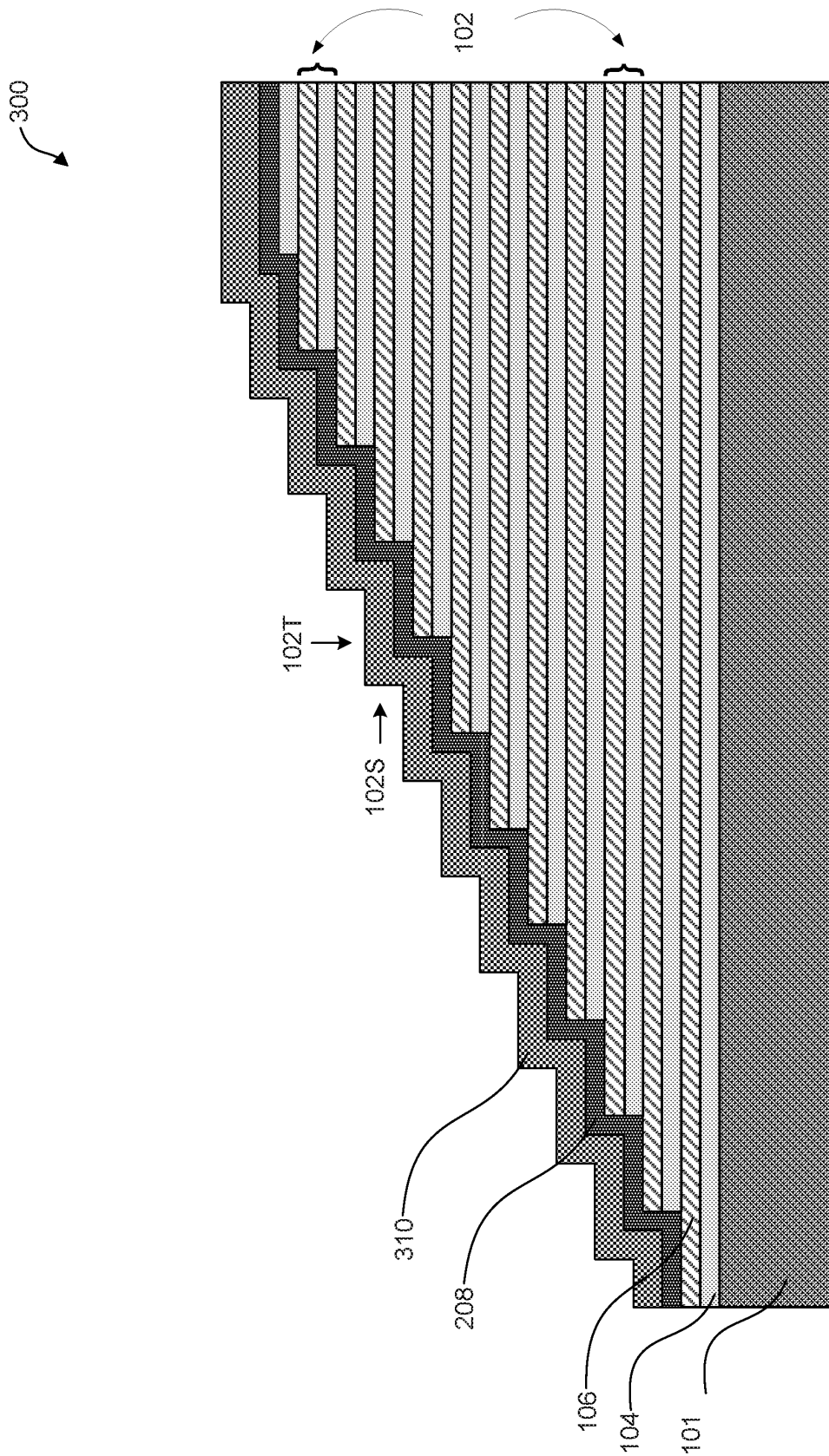


FIG. 3

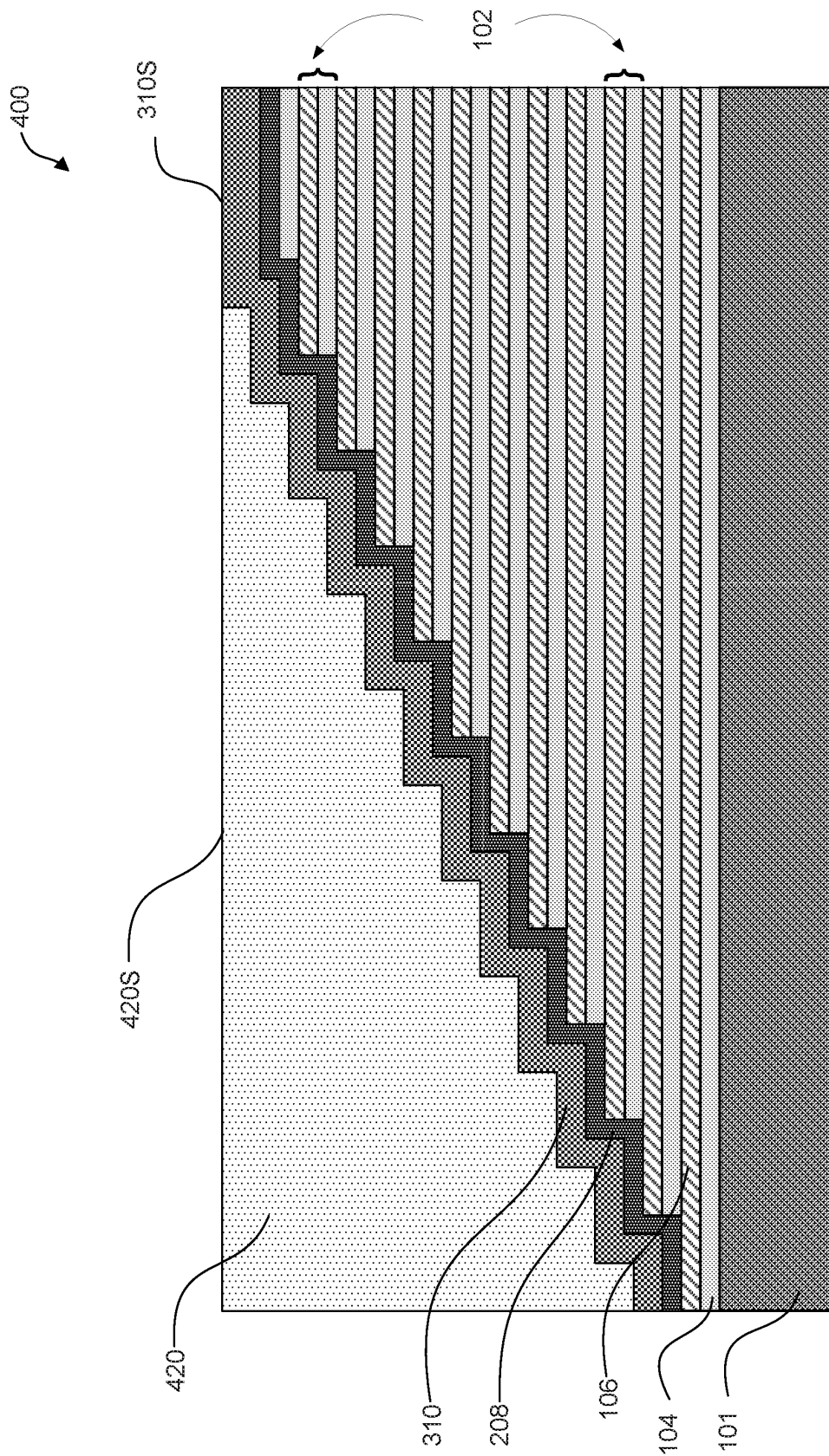
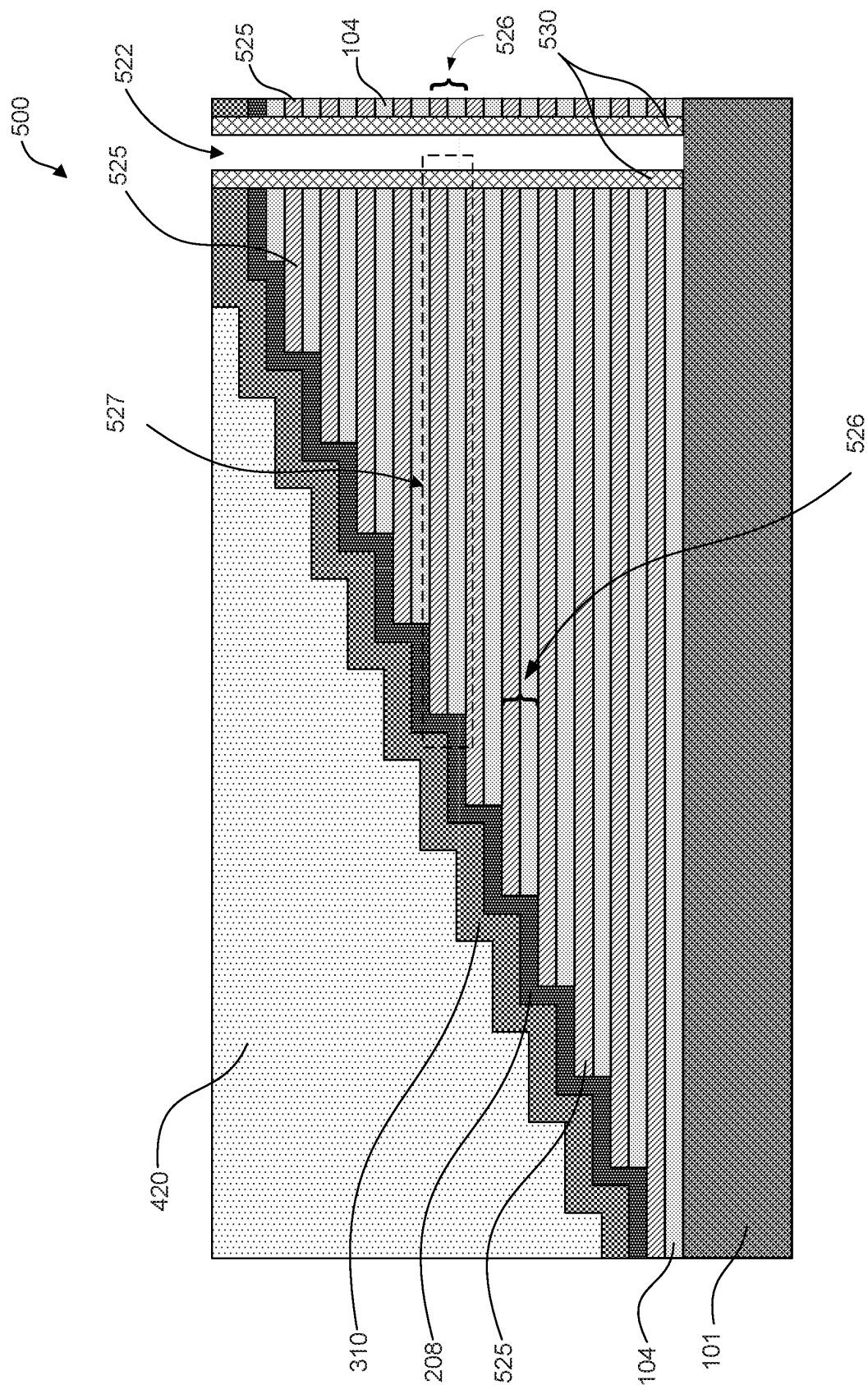


FIG. 4



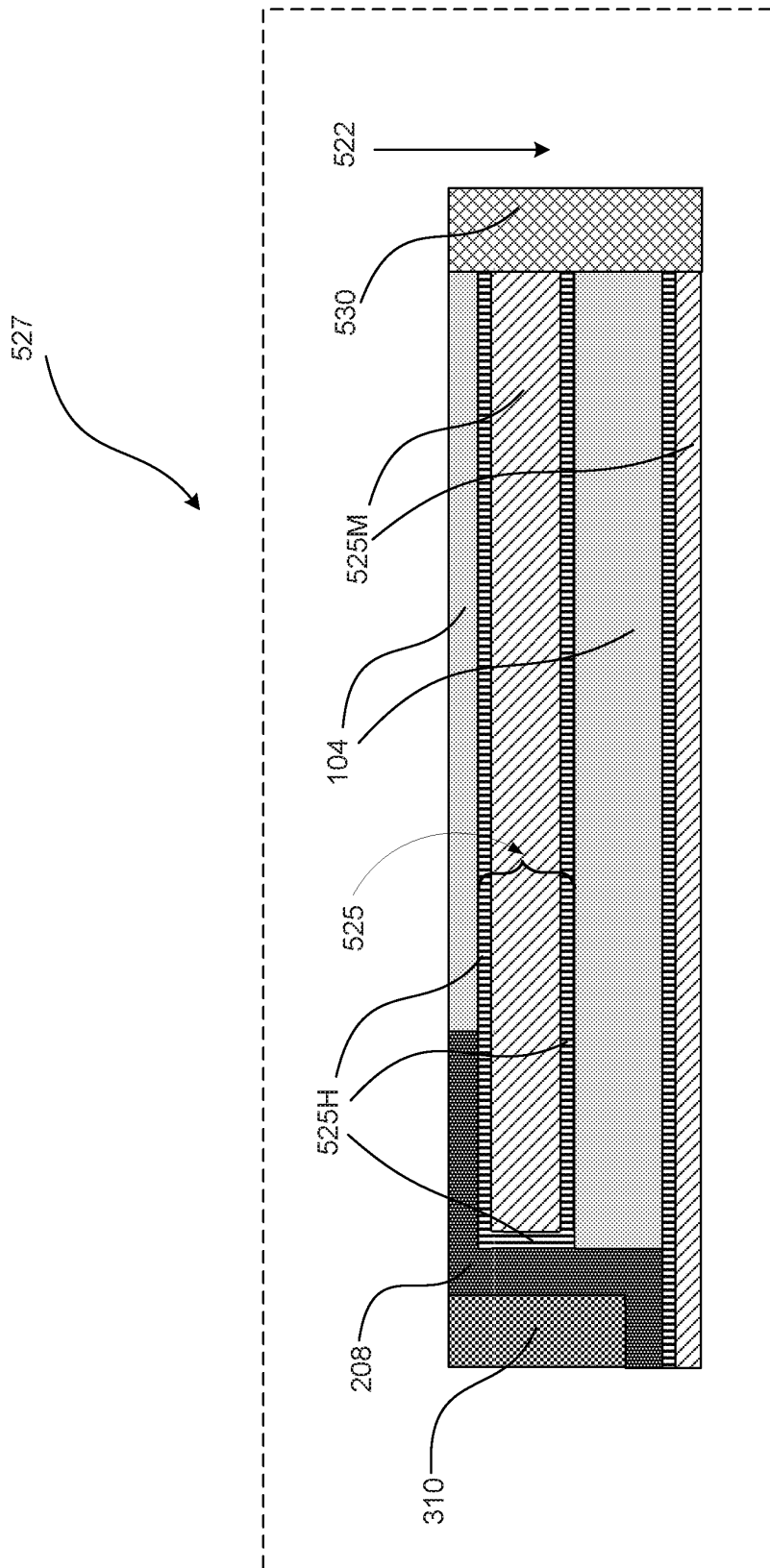


FIG. 5B

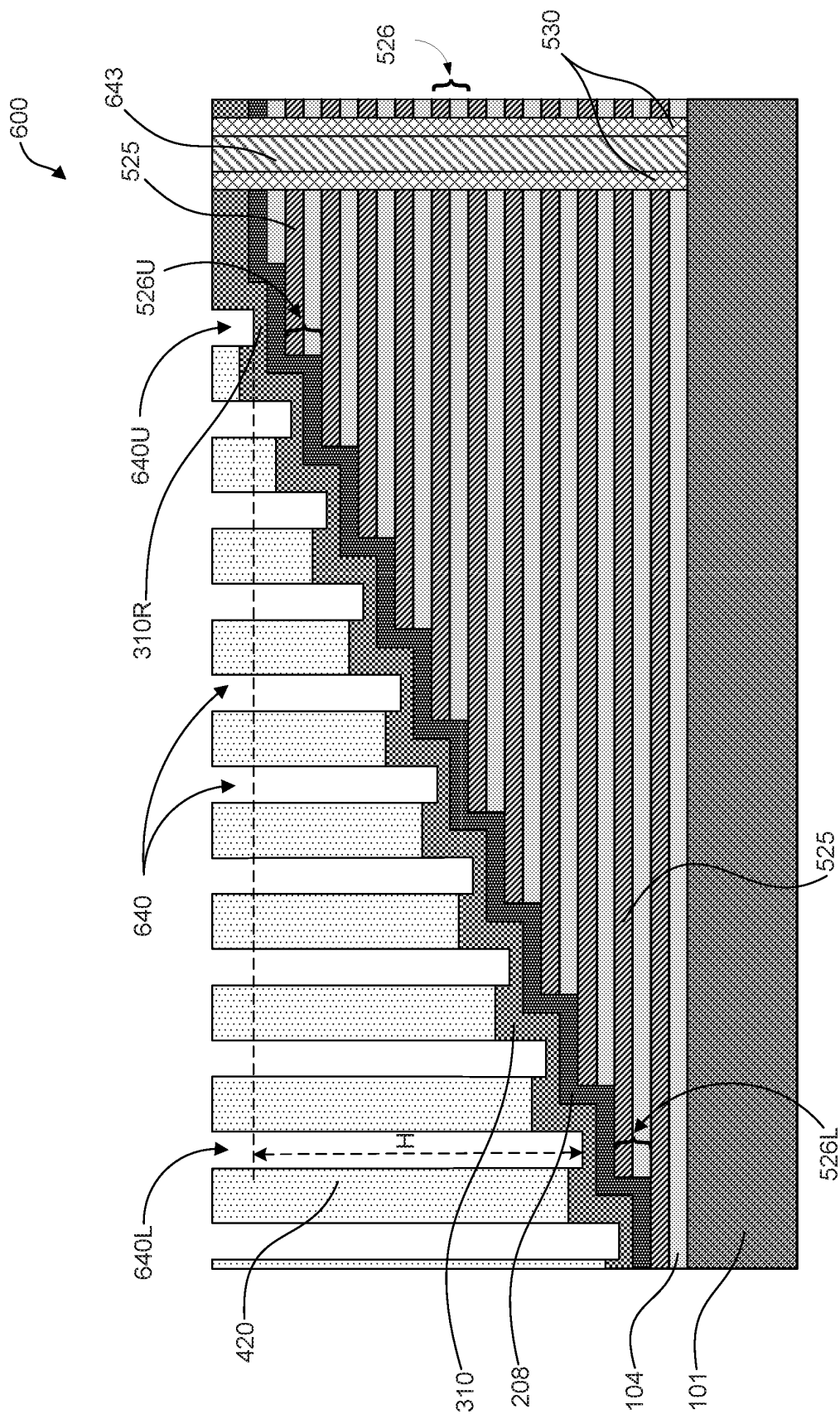


FIG. 6

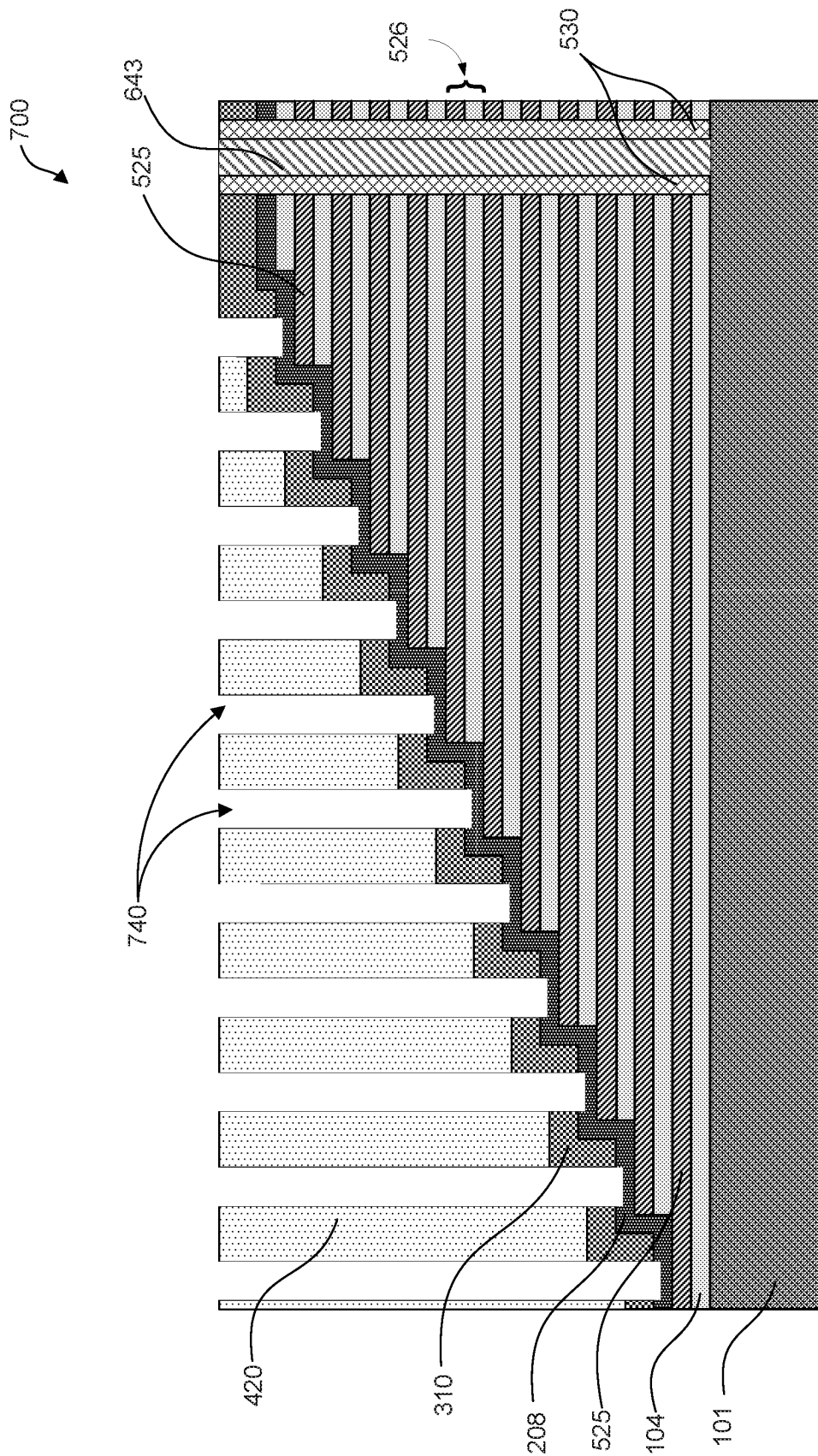


FIG. 7

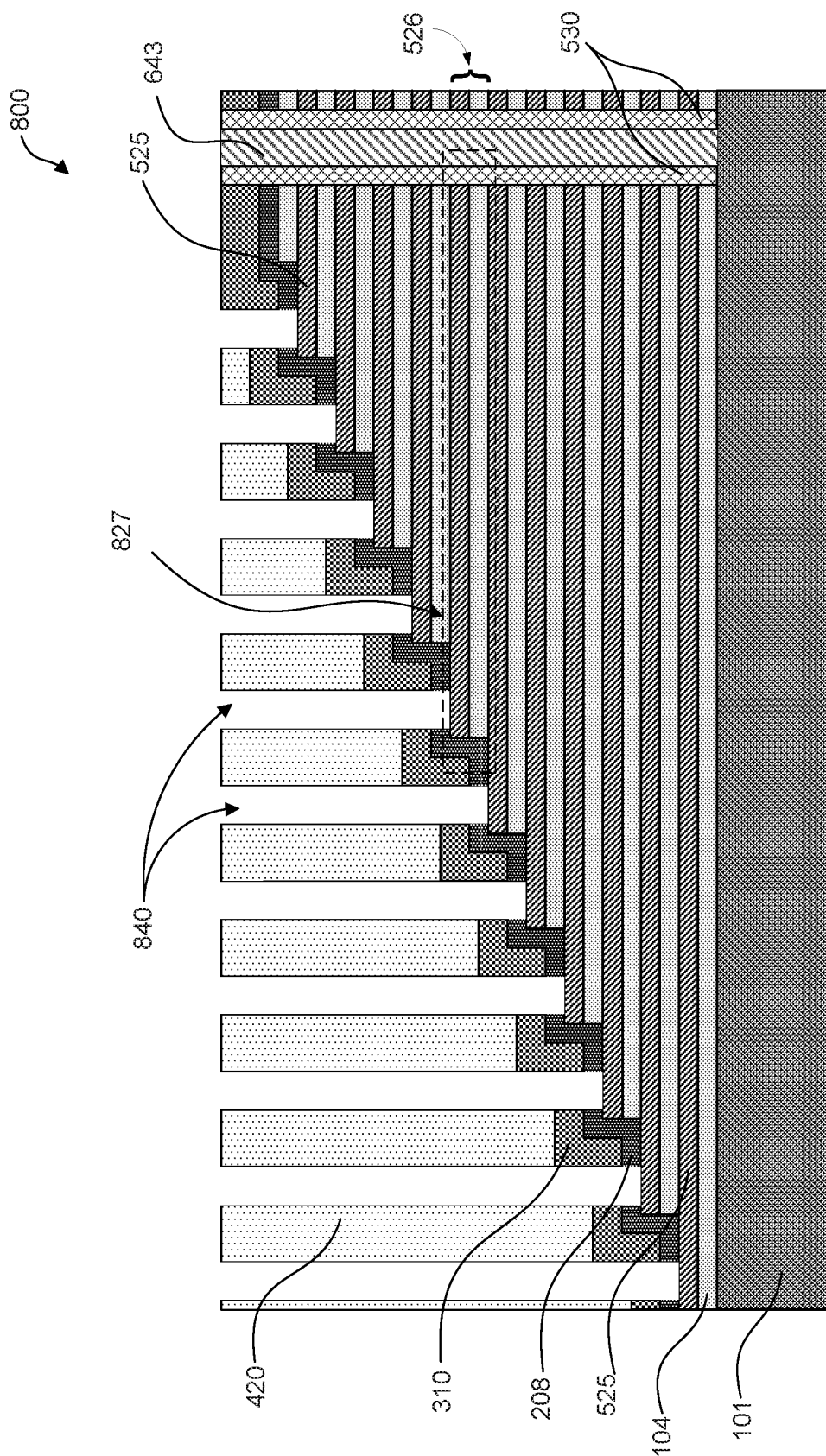


FIG. 8A

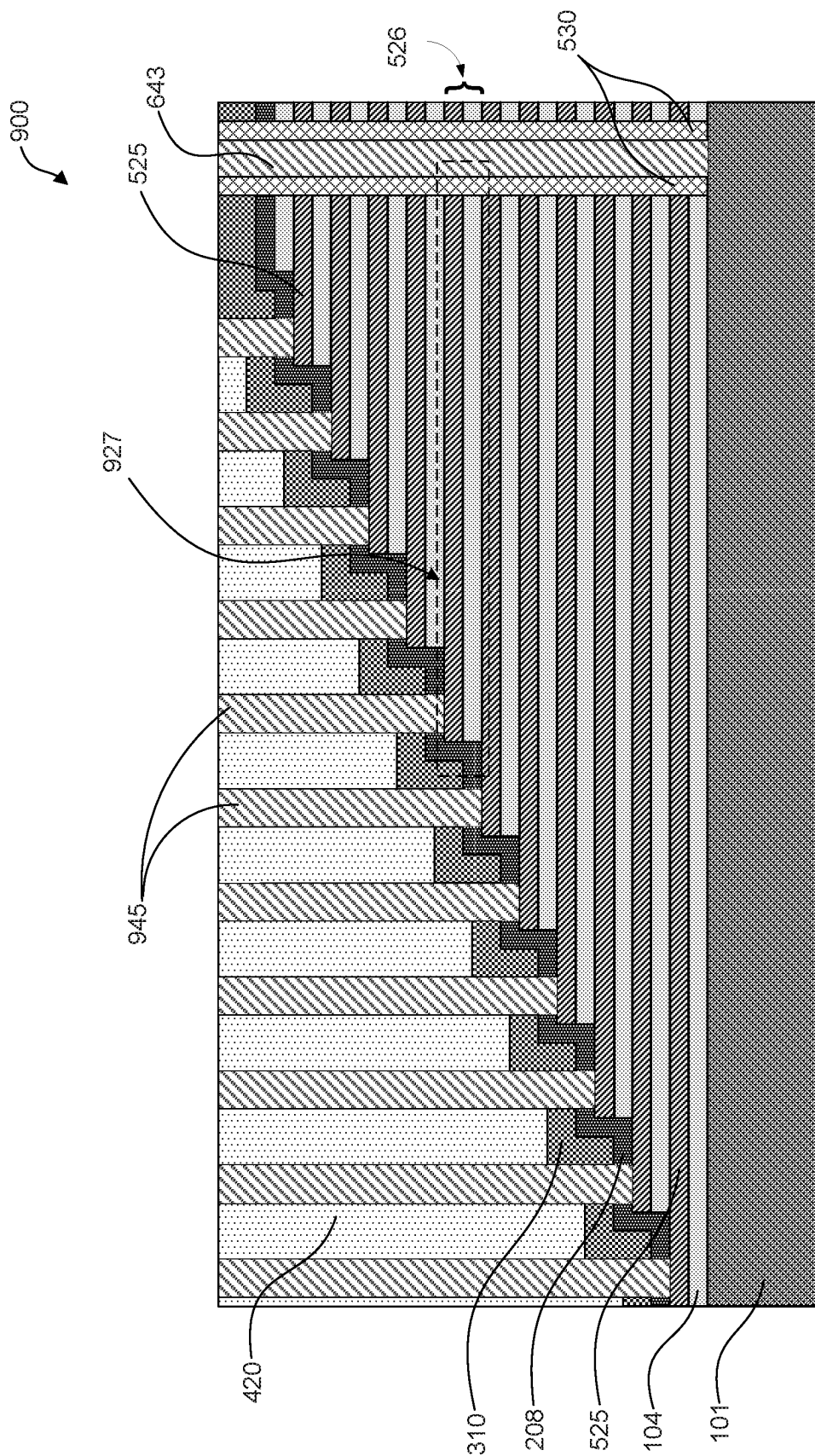


FIG. 9A

927

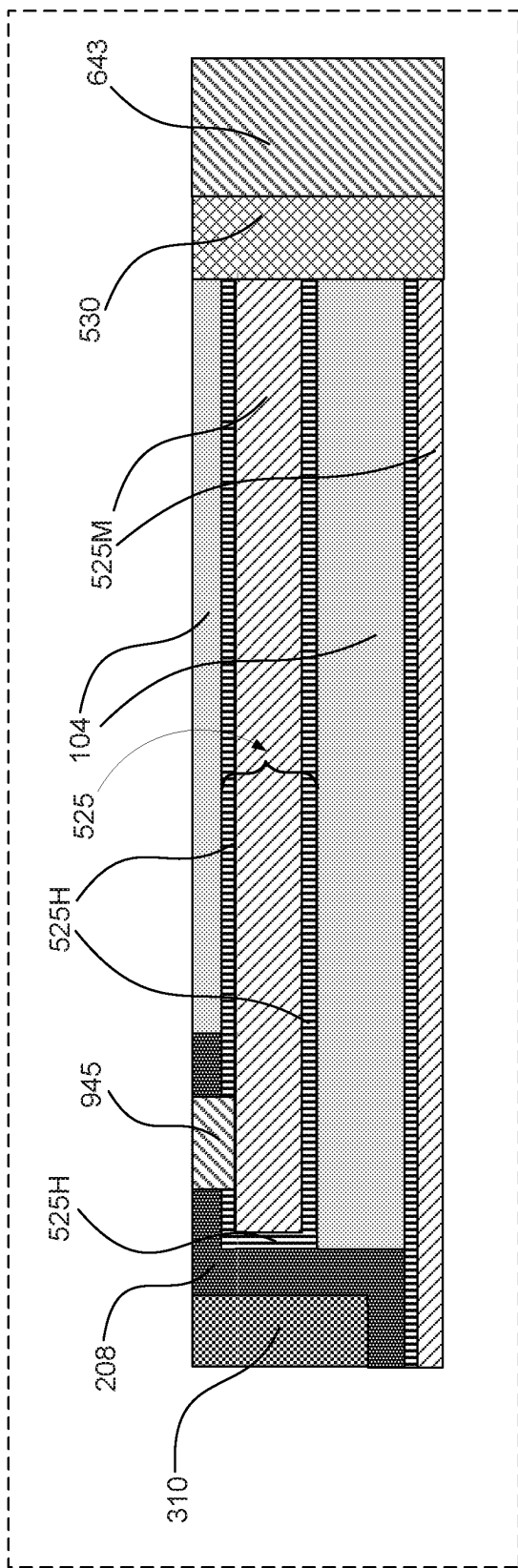


FIG. 9B

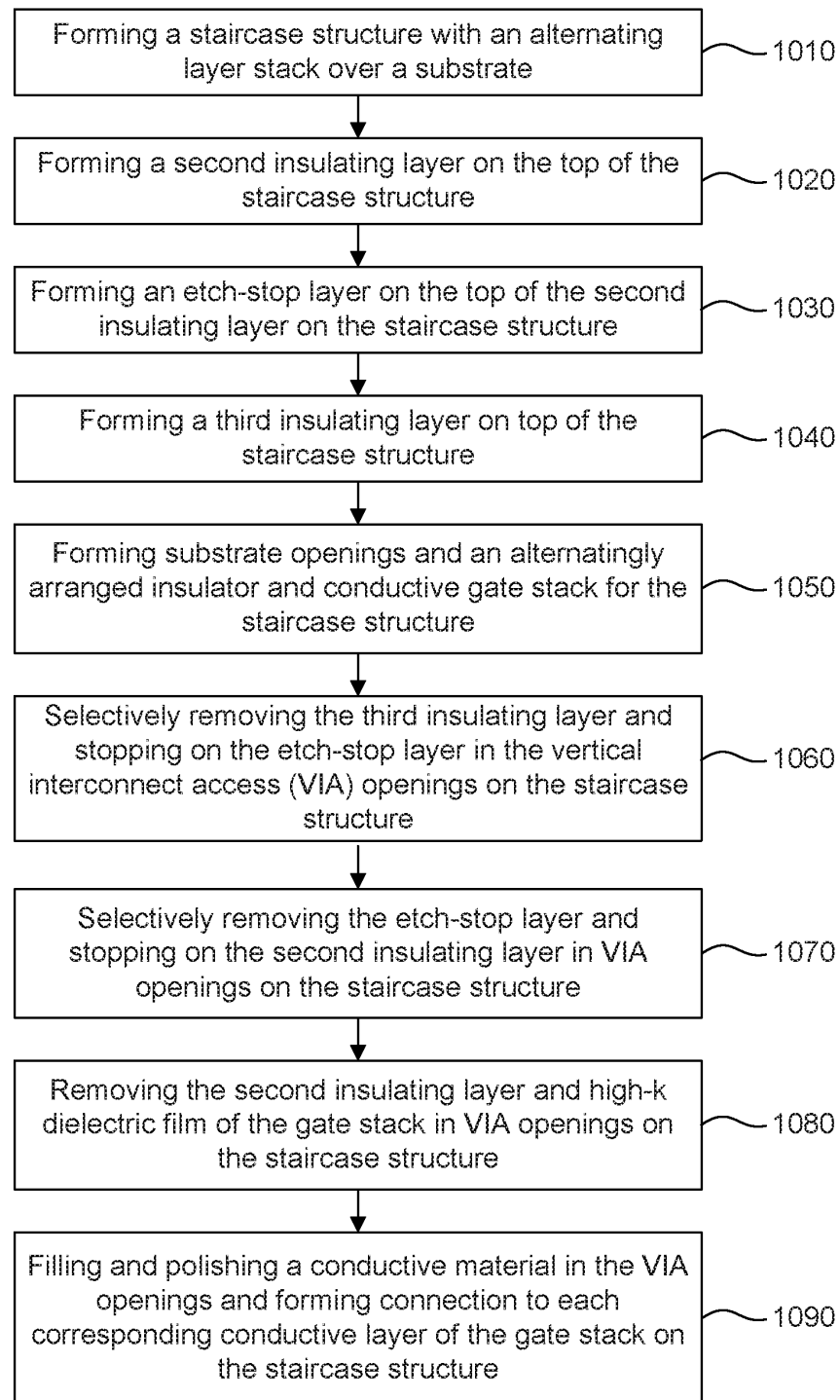


FIG. 10

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Application Number	To Be Assigned
Filing Date	Herewith
First Named Inventor	Jifeng ZHU
Title	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	4123.0480002

SIGNATURE of Applicant or Patent Practitioner

Signature	/Donald J. Featherstone/	Date (Optional)	9/10/18
Name	Donald J. Featherstone	Registration Number	33,876
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)		Yangtze Memory Technologies Co., Ltd.	

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I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.

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The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

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Name

Simon Shi-Ning Yang

Title

CEO

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Electronic Acknowledgement Receipt	
EFS ID:	33675919
Application Number:	16126947
International Application Number:	
Confirmation Number:	1077
Title of Invention:	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF
First Named Inventor/Applicant Name:	Jifeng ZHU
Customer Number:	26111
Filer:	Donald J. Featherstone/Tonyia Skinner
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Attorney Docket Number:	4123.0480002
Receipt Date:	10-SEP-2018
Filing Date:	
Time Stamp:	18:31:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		41230480002ContinuationApplication.pdf	2016624	yes	56
			26633f90da33dc38c11f63983602a3d06ed3765b		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Transmittal Letter	1	2
	Transmittal of New Application	3	4
	Authorization for Extension of Time all replies	5	5
	Application Data Sheet	6	16
	Specification	17	37
	Claims	38	40
	Abstract	41	41
	Drawings-only black and white line drawings	42	54
	Power of Attorney	55	56
Warnings:			
Information:			
Total Files Size (in bytes):		2016624	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

September 10, 2018

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: U.S. Non-Provisional Patent Application under 37 C.F.R. § 1.53(b)
(*Continuation of Appl. No. PCT/CN2018/101308; Filed: August 20, 2018*)
Appl. No. *To Be Assigned*; Filed: *Herewith*
For: **WORD LINE CONTACT STRUCTURE FOR THREE-
DIMENSIONAL MEMORY DEVICES AND FABRICATION
METHODS THEREOF**
Inventors: ZHU *et al.*
Our Ref: 4123.0480002

Commissioner:

The following documents are transmitted herewith for appropriate action by the U.S.
Patent and Trademark Office:

1. Utility Patent Application Transmittal Form (PTO/AIA/15);
2. Authorization to Treat a Reply As Incorporating An Extension of Time
Under 37 C.F.R. § 1.136(a)(3);
3. U.S. Utility Patent Application entitled:

**WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL
MEMORY DEVICES AND FABRICATION METHODS THEREOF**

and naming as inventors:

**Jifeng ZHU
Zhenyu LU
Jun CHEN
Si Ping HU
Xiaowang DAI
Lan YAO
Li Hong XIAO
A Man ZHENG
Kun BAO
Haohao YANG**

Sterne, Kessler, Goldstein & Fox P.L.L.C. | 1100 New York Avenue, NW | Washington, D.C. 20005
P 202.371.2600 | F 202.371.2540 | sternekessler.com

the application consisting of:

- a. An Application Data Sheet (37 C.F.R. § 1.76) (PTO/AIA/14);
 - b. A specification containing:
 - i. 21 pages of description prior to the claims;
 - ii. 3 pages of claims (20 claims);
 - iii. a one (1) page abstract; and
 - c. 13 sheets of drawings: (Figures 1-4, 5A-5B, 6-7, 8A-8B, 9A-9B and 10).
4. An executed Power of Attorney by Applicant form (PTO/AIA/82B) and the Transmittal for Power of Attorney form (PTO/AIA/82A).

The above-listed documents are filed electronically.

Correspondence should be sent to Customer Number 26111.

This patent application is being submitted under 37 C.F.R. § 1.53(b) without Declaration and without the required fees.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/Y-G/tas
Enclosures

9960939_1.docx

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 16/126,947	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 = *				x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/126,947	09/10/2018	Jifeng ZHU	4123.0480002

CONFIRMATION NO. 1077

FORMALITIES LETTER



OC000000103013976

26111

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Date Mailed: 10/15/2018

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.

The surcharge is due for any one of:

- late submission of the basic filing fee, search fee, or examination fee,
- late submission of inventor's oath or declaration,
- filing an application that does not contain at least one claim on filing, or
- submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- \$ **300** basic filing fee.
- \$ **160** surcharge.
- \$ **660** search fee.
- \$ **760** examination fee.
- \$ **(0)** previous unapplied payment amount.
- \$ **1880** TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):

Jifeng ZHU
Zhenyu LU
Jun CHEN
Si Ping HU
Xiaowang DAI
Lan YAO
Li Hong XIAO
A Man ZHENG
Kun BAO
Haohao YANG

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice".
<https://portal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/kgebremichael/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
16/126,947	09/10/2018	2812	0.00	4123.0480002	20	3

CONFIRMATION NO. 1077

FILING RECEIPT

26111

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005



CC000000103013975

Date Mailed: 10/15/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jifeng ZHU, Wuhan, CHINA;
Zhenyu LU, Wuhan, CHINA;
Jun CHEN, Wuhan, CHINA;
Si Ping HU, Wuhan, CHINA;
Xiaowang DAI, Wuhan, CHINA;
Lan YAO, Wuhan, CHINA;
Li Hong XIAO, Wuhan, CHINA;
A Man ZHENG, Wuhan, CHINA;
Kun BAO, Wuhan, CHINA;
Haohao YANG, Wuhan, CHINA;

Applicant(s)

Yangtze Technologies Co., Ltd., Wuhan, CHINA

Assignment For Published Patent Application

Yangtze Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2018/101308 08/20/2018

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

CHINA 201710774754.6 08/31/2017 No Access Code Provided

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 10/11/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/126,947**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND
FABRICATION METHODS THEREOF

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative,

page 2 of 4

this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/126,947	09/10/2018	Jifeng ZHU	4123.0480002

CONFIRMATION NO. 1077

FORMALITIES LETTER

26111

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005



OC000000103013976

Date Mailed: 10/15/2018

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.

The surcharge is due for any one of:

- late submission of the basic filing fee, search fee, or examination fee,
- late submission of inventor's oath or declaration,
- filing an application that does not contain at least one claim on filing, or
- submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- \$ 300 basic filing fee.
- \$ 160 surcharge.
- \$ 660 search fee.
- \$ 760 examination fee.
- \$(0) previous unapplied payment amount.
- \$ 1880 TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):

Jifeng ZHU
Zhenyu LU
Jun CHEN
Si Ping HU
Xiaowang DAI
Lan YAO
Li Hong XIAO
A Man ZHENG
Kun BAO
Haohao YANG

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice".
<https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/kgebrebmichael/

Donald J. Featherstone
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM



December 13, 2018

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 1077
Mail Stop Missing Parts

Re: U.S. Patent Application
Appl. No. 16/126,947; Filed: September 10, 2018
For: **WORD LINE CONTACT STRUCTURE FOR THREE-
DIMENSIONAL MEMORY DEVICES AND FABRICATION
METHODS THEREOF**
Inventors: ZHU *et al.*
Our Ref: 4123.0480002

Commissioner:

In reply to the "Notice to File Missing Parts of Non-Provisional Application," dated October 15, 2018, Applicant transmit the following documents for appropriate action by the U.S. Patent and Trademark Office:

1. Online Credit Card Payment Authorization for **\$1,880.00** to cover:
\$1,720.00 - Patent Application fee (including basic filing, search and examination fees)
\$160.00 - Surcharge for late filing fee or late Oath or Declaration
2. Original Declaration, executed by the inventors;

The above-listed documents are filed electronically.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036. If extensions of time under 37 C.F.R. § 1.136 other than those otherwise provided for herewith are required to prevent abandonment of the present patent application, then such extensions of time are hereby petitioned, and any fees therefor are hereby authorized to be charged to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/M-Y/d-o
Enclosures

10434079_1.docx

Sterne, Kessler, Goldstein & Fox P.L.L.C. | 1100 New York Avenue, NW | Washington, D.C. 20005
P 202.371.2500 | F 202.371.2540 | sternekessler.com

Micron Ex. 1002, p. 69
Micron v. YMTC
IPR2025-00117

Electronic Patent Application Fee Transmittal				
Application Number:		16126947		
Filing Date:		10-Sep-2018		
Title of Invention:		WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		
First Named Inventor/Applicant Name:		Jifeng ZHU		
Filer:		Donald J. Featherstone/David Ofori		
Attorney Docket Number:		4123.0480002		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1880

Electronic Acknowledgement Receipt	
EFS ID:	34579951
Application Number:	16126947
International Application Number:	
Confirmation Number:	1077
Title of Invention:	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF
First Named Inventor/Applicant Name:	Jifeng ZHU
Customer Number:	26111
Filer:	Donald J. Featherstone/David Ofori
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0480002
Receipt Date:	13-DEC-2018
Filing Date:	10-SEP-2018
Time Stamp:	16:55:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1880
RAM confirmation Number	121418INTEFSW16560200
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2018-12-13-Reply-Missing-Parts-Declaration-4123-0480002.pdf	5425498	yes	7
			512ac8697578429bbac715719c28f3027c0e8947		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Oath or Declaration filed		4	7	
	Applicant Response to Pre-Exam Formalities Notice		2	3	
	Miscellaneous Incoming Letter		1	1	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	37334	no	2
			530e23cdab5155c16dc011d74397f6d5fa1f825		
Warnings:					
Information:					
Total Files Size (in bytes):			5462832		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☒ United States application or PCT international application number 16/126,947
filed on September 10, 2018

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar (\$1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 26111** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: Jifeng ZHU Date: 2018.10.22

Signature of Inventor: Jifeng ZHU

LEGAL NAME OF INVENTOR

Inventor: Zhenyu LU Date: 2018.10.23

Signature of Inventor: Zhenyu Lu

LEGAL NAME OF INVENTOR

Inventor: Jun CHEN Date: 2018.10.23

Signature of Inventor: Jun CHEN

LEGAL NAME OF INVENTOR

Inventor: Si Ping HU Date: 2018.11.05

Signature of Inventor: Si Ping HU

LEGAL NAME OF INVENTOR

Inventor: Xiaowang DAI Date: 2018.11.2

Signature of Inventor: Xiaowang DAI

LEGAL NAME OF INVENTOR

Inventor: Lan YAO Date: 2018. 10. 22

Signature of Inventor: Lan Yao

LEGAL NAME OF INVENTOR

Inventor: Li Hong XIAO Date: 2018. 10. 22.

Signature of Inventor: Li Hong Xiao

LEGAL NAME OF INVENTOR

Inventor: A Man ZHENG Date: 2018. 10. 22

Signature of Inventor: A Man ZHENG

LEGAL NAME OF INVENTOR

Inventor: Kun BAO Date: 2018. 10. 22

Signature of Inventor: Kun BAO

LEGAL NAME OF INVENTOR

Inventor: Haohao YANG Date: 2018 / 10 / 22

Signature of Inventor: Haohao YANG

10202996_1.docx



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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
16/126,947	09/10/2018	2812	1880	4123.0480002	20	3

CONFIRMATION NO. 1077

UPDATED FILING RECEIPT

26111

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005



0000000104510448

Date Mailed: 12/18/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jifeng ZHU, Wuhan, CHINA;
Zhenyu LU, Wuhan, CHINA;
Jun CHEN, Wuhan, CHINA;
Si Ping HU, Wuhan, CHINA;
Xiaowang DAI, Wuhan, CHINA;
Lan YAO, Wuhan, CHINA;
Li Hong XIAO, Wuhan, CHINA;
A Man ZHENG, Wuhan, CHINA;
Kun BAO, Wuhan, CHINA;
Haohao YANG, Wuhan, CHINA;

Applicant(s)

Yangtze Technologies Co., Ltd., Wuhan, CHINA

Assignment For Published Patent Application

Yangtze Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2018/101308 08/20/2018

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

CHINA 201710774754.6 08/31/2017 No Access Code Provided

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 10/11/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/126,947**

Projected Publication Date: 03/28/2019

Non-Publication Request: No

Early Publication Request: No

Title

WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND
FABRICATION METHODS THEREOF

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative,

page 2 of 4

this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 16/126,947	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 = *				x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/126,947	09/10/2018	Jifeng ZHU	4123.0480002

CONFIRMATION NO. 1077

26111

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

PUBLICATION NOTICE



OC000000106951273

Title:WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF

Publication No.US-2019-0096810-A1

Publication Date:03/28/2019

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

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Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet

1

of

2

Complete if Known

Application Number	16/126,947
Filing Date	September 10, 2018
First Named Inventor	Zhu et al.
Art Unit	2811
Examiner Name	GURLEY, LYNNE ANN
Attorney Docket Number	4123.0480002

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	1	US- 2013/0313627 A1	11-28-2013	Lee et al.	
	2	US- 2016/0118398 A1	04-28-2016	Yon et al.	
	3	US- 8,828,884 B2	09-09-2014	Lee et al.	
	4	US- 9,515,086 B2	12-06-2016	Yon et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
	FP1	CN-104396004-A	03-04-2015	SANDISK TECHNOLOGIES INC.		
	FP2					
	FP3					
	FP4					
	FP5					
	FP6					

Examiner
SignatureDate
Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known	
		Application Number	16/126,947
		Filing Date	September 10, 2018
		First Named Inventor	Zhu et al.
		Art Unit	2811
		Examiner Name	GURLEY, LYNNE ANN
Sheet 1	of 1	Attorney Docket Number	4123.0480002

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	NPL 1	International Search Report and Written Opinion of the International Searching Authority directed to related International Patent Application No. PCT/CN2018/101308, mailed November 21, 2018; 6 pages.	

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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(10) 申请公布号 CN 104396004 A

(43) 申请公布日 2015.03.04

代理人 邱军

(51) Int. Cl.

H01L 21/768(2006.01)

H01L 27/115(2006.01)

2014. 12. 23

PCT/US2013/041410 2013.05.16

W02013/176960 EN 2013. 11. 28

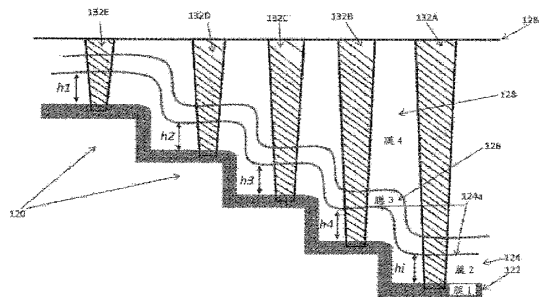
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三维存储器阵列的多级接触及其制造方法

一种制造多级接触的方法。该方法包括提供工艺过程多级装置,该多级装置包括至少一个装置区域和至少一个接触区域。该接触区域包括构造为台阶图案的多个导电层。该方法还包括在该多个导电层上方形成共形的蚀刻终止层(122),在该蚀刻终止层(122)的上方形成第一电绝缘层(124),在该第一电绝缘层的上方形成共形的牺牲层(126)和在该牺牲层上方形成第二电绝缘层(128)。该方法还包括蚀刻多个接触开口(130A-E),穿过在该接触区域中的该蚀刻终止层、该第一电绝缘层、该牺牲层和该第二电绝缘层,到达该多个导电层。



1. 一种制造多级接触的方法,包括:

提供工艺过程中多级装置,包括至少一个装置区域和至少一个接触区域,该接触区域包括构造为台阶图案的多个导电层;

在该多个导电层的上方形成共形的蚀刻终止层;

在该蚀刻终止层的上方形成第一电绝缘层;

在该第一电绝缘层的上方形成共形的牺牲层;

在该牺牲层的上方形成第二电绝缘层;以及

蚀刻多个接触开口,穿过在该接触区域中的该蚀刻终止层、该第一电绝缘层、该牺牲层和该第二电绝缘层,到达该多个导电层。

2. 如权利要求 1 所述的方法,其中:

该多个导电层包括至少一个第一导电层和第二导电层,该至少一个第一导电层位于衬底上方的第一装置级中,该第二导电层位于该衬底上方比第一装置级更高的第二装置级中;

该第一导电层包括第一部分,该第一部分横向延伸通过该第二导电层,以形成该台阶图案的至少一部分;以及

该多个接触开口包括第一接触开口和第二接触开口,该第一接触开口延伸至该第一导电层的该第一部分,该第二接触开口延伸至该第二导电层的上表面。

3. 如权利要求 2 所述的方法,还包括在该第一接触开口中形成第一导电接触和在该第二接触开口中形成第二导电接触,其中该第一导电接触比该第二导电接触延伸得更深。

4. 如权利要求 3 所述的方法,其中该蚀刻的步骤包括:

使用第一蚀刻化学物,使用该牺牲层作为蚀刻终止,选择性地蚀刻该多个接触开口的第一部分,穿过该第二电绝缘层;

使用第二蚀刻化学物,使用该第一电绝缘层作为蚀刻终止,选择性地蚀刻该多个接触开口的第二部分,穿过该牺牲层;

使用第三蚀刻化学物,使用该共形的蚀刻终止层作为蚀刻终止,选择性地蚀刻该多个接触开口的第三部分,穿过该第一电绝缘层;

使用第四蚀刻化学物,选择性地蚀刻该多个接触开口的第四部分,穿过该共形的蚀刻终止层,到达该多个导电层。

5. 如权利要求 4 所述的方法,其中:

该第一蚀刻化学物和该第三蚀刻化学物是相同的;

该第二蚀刻化学物和该第四蚀刻化学物是相同的;

该第一蚀刻化学物和该第二蚀刻化学物是不同的;

该共形的蚀刻终止层和该共形的牺牲层包括相同的材料;

该第一绝缘层和该第二电绝缘层包括相同的材料;以及

该共形的牺牲层包括与该第一电绝缘层不同的材料。

6. 如权利要求 5 所述的方法,其中:

该共形的蚀刻终止层和该共形的牺牲层包括相同的氮化物材料;以及

该第一电绝缘层和该第二电绝缘层包括相同的氧化物材料。

7. 如权利要求 6 所述的方法,其中该蚀刻终止层包括氮化硅,该第一电绝缘层包括氧

化硅,该牺牲层包括氮化硅,并且该第二电绝缘层包括氧化硅。

8. 如权利要求 4 所述的方法,其中:

该共形的蚀刻终止层、该第一电绝缘层和该牺牲层的每一个具有基本均匀的厚度,并且每一个布置为在该接触区域中的该多个导电层的上方的台阶图案;

该第二电绝缘层具有可变的厚度和基本平面的上表面;

该第二电绝缘层在该第一导电层的第一部分上方比在该第二导电层的上方更厚;

最浅的台阶位于在蚀刻方向中距离该第二电绝缘层的顶表面最短的距离处;

最深的台阶位于在蚀刻方向中距离该电绝缘层的顶表面最大的距离处;以及

当在该最深的台阶上方的蚀刻终止层的蚀刻完成时,在该最浅的台阶上的蚀刻终止层没有穿过。

9. 如权利要求 2 所述的方法,其中:

该装置包括垂直的 NAND 装置;

该装置区域包括:

多个半导体沟道,其中该多个半导体沟道的每一个的至少一个端部分基本垂直于该衬底的主表面延伸;

多个电荷储存区域,每个电荷储存区域与该多个半导体沟道的相应一个相邻设置;以及

多个控制栅电极,具有带状,基本平行于该衬底的该主表面延伸,其中该多个控制栅电极包括至少一个在该第一装置级中的第一控制栅电极和在该第二装置级中的第二控制栅电极;

该第一导电层包括该第一控制栅极的一部分,从该装置区域延伸至该接触区域;以及

该第二导电层包括该第二控制栅电极的一部分,从该装置区域延伸至该接触区域。

10. 一种制造多级接触的方法,包括:

提供工艺过程中的多级装置,该多级装置包括至少一个装置区域和至少一个接触区域,该接触区域包括:构造为台阶图案的多个导电层、位于该导电层上方的电绝缘层、位于该绝缘层上方的具有多个开口的掩模,和位于该掩模上方的减薄层;

蚀刻该减薄层以减小其厚度和宽度,从而暴露在该掩模中的第一开口;

蚀刻暴露在该第一开口中的电绝缘材料的一部分,以在该电绝缘材料中形成第一接触开口的一部分;

进一步蚀刻该减薄层以减小其厚度和宽度,从而暴露在该掩模中的第二开口。

11. 如权利要求 10 所述的方法,其中蚀刻该电绝缘材料的一部分的步骤与进一步蚀刻该减薄层的步骤同时发生。

12. 如权利要求 11 所述的方法,还包括继续蚀刻减薄层以减小其厚度和宽度,从而暴露在该掩模中的第三开口和蚀刻暴露在该第一开口和该第二开口中的电绝缘材料的一部分,以在该电绝缘材料中形成该第二接触开口的第一部分和该第一接触开口的第二部分,其中该第一接触开口比该第二接触开口更深。

13. 如权利要求 12 所述的方法,还包括继续蚀刻该减薄层直到暴露在该掩模中的所有该多个开口,并且蚀刻该多个接触开口的对应的一个,穿过在该掩模中的每一个开口,到达该多个导电层。

14. 如权利要求 13 所述的方法, 其中:

该多个导电层包括至少一个第一导电层和第二导电层, 该至少一个第一导电层位于衬底上方的第一装置级中, 该第二导电层位于该衬底上方比第一装置级更高的第二装置级中;

该第一导电层包括第一部分, 横向延伸通过该第二导电层, 以形成该台阶图案的至少一部分; 以及

该多个接触开口包括第一接触开口和第二接触开口, 该第一接触开口延伸至该第一导电层的该第一部分, 该第二接触开口延伸至该第二导电层的上表面。

15. 如权利要求 14 所述的方法, 还包括在该第一接触开口中形成第一导电接触和在该第二接触开口中形成第二导电接触, 其中该第一导电接触比该第二导电接触延伸得更深。

16. 如权利要求 15 所述的方法, 其中:

该装置包括垂直 NAND 装置;

该装置区域包括:

多个半导体沟道, 其中多个半导体沟道的每一个的至少一个端部分基本垂直于该衬底的主表面延伸;

多个电荷储存区域, 每个电荷储存区域与该多个半导体沟道的相应的一个相邻设置; 以及

多个控制栅电极, 具有带状, 基本平行于该衬底的该主表面延伸, 其中该多个控制栅电极包括在该第一装置级中的至少一个第一控制栅电极和在该第二装置级中的第二控制栅电极;

该第一导电层包括该第一控制栅电极的一部分, 从该装置区域延伸至该接触区域; 以及

该第二导电层包括该第二控制栅电极的一部分, 从该装置区域延伸至该接触区域。

17. 如权利要求 10 所述的方法, 其中该减薄层包括光致抗蚀剂层并且该掩模包括硬掩模。

18. 一种多级装置, 包括:

至少一个装置区域和至少一个接触区域, 该至少一个接触区域具有多个堆叠的导电层, 其中该导电层形成在该接触区域中的台阶图案;

位于该导电层的上方的共形的蚀刻终止层;

位于该蚀刻终止层的上方的第一电绝缘层;

位于该第一电绝缘层的上方的共形的牺牲层;

位于该牺牲层的上方的第二电绝缘层;

多个接触开口, 延伸穿过在该接触区域中的该蚀刻终止层、该第一电绝缘层、该牺牲层和该第二电绝缘层, 到达该多个导电层; 以及

多个导电接触, 其中该多个导电接触的相应的每一个位于该多个接触开口的相应的一个中, 以及每个导电接触与该多个导电层的相应的一层电接触。

19. 如权利要求 18 所述的方法, 其中:

该多个导电层包括至少一个第一导电层和第二导电层, 该至少一个第一导电层在位于衬底上方的第一装置级中, 该第二导电层位于该衬底上方比第一装置级更高的第二装置级

中；

该第一导电层包括第一部分，横向延伸通过该第二导电层，以形成该台阶图案的至少一部分；

该多个接触开口包括第一接触开口和第二接触开口，该第一接触开口延伸至该第一导电层的该第一部分，该第二接触开口延伸至该第二导电层的上表面；

该多个导电接触的第一导电接触位于该第一接触开口中；

该多个导电接触的第二导电接触位于该第二接触开口中；以及

该第一导电接触比该第二导电接触延伸得更深。

20. 如权利要求 19 所述的方法，其中：

该共形的蚀刻终止层和该共形的牺牲层包括相同的材料；

该第一电绝缘层和该第二电绝缘层包括相同的材料；以及

该共形的牺牲层包括不同于该第一电绝缘层的材料。

21. 如权利要求 20 所述的方法，其中：

该共形的蚀刻终止层和该共形的牺牲层包括相同的氮化物材料；以及

该第一绝缘层和该第二电绝缘层包括相同的氧化物材料。

22. 如权利要求 21 所述的方法，其中该蚀刻终止层包括氮化硅，该第一电绝缘层包括氧化硅，该牺牲层包括氮化硅，以及该第二电绝缘层包括氧化硅。

23. 如权利要求 19 所述的方法，其中：

该装置包括垂直的 NAND 装置；

该装置区域包括：

多个半导体沟道，其中多个半导体沟道的每一个的至少一个端部分基本垂直于该衬底的主表面延伸；

多个电荷储存区域，每个电荷储存区域与该多个半导体沟道的相应的一个相邻设置；以及

多个控制栅电极，具有带状，基本平行于该衬底的该主表面延伸，其中该多个控制栅电极包括在该第一装置级中的至少一个第一控制栅电极和在该第二装置级中的第二控制栅电极；

该第一导电层包括该第一控制栅电极的一部分，从该装置区域延伸至该接触区域；以及

该第二导电层包括该第二控制栅电极的一部分，从该装置区域延伸至该接触区域。

24. 如权利要求 19 所述的方法，其中：

该共形的蚀刻终止层、该第一电绝缘层和该牺牲层的每一个具有基本均匀的厚度，并且每一个布置为在该接触区域中的该多个导电层的上方的台阶图案；

该第二电绝缘层具有可变的厚度和基本平面的上表面；

该第二电绝缘层在该第一导电层的第一部分上方比在该第二导电层的上方更厚。

三维存储器阵列的多级接触及其制造方法

技术领域

[0001] 本发明大体涉及半导体装置领域,特别涉及三维(3D)垂直 NAND 串和其它三维装置及其制造方法。

背景技术

[0002] T.Endoh 等人的标题为“Novel Ultra High Density Memory With A Stacked-Surrounding Gate Transistor(S-SGT)Structured Cell”,IEDM Proc.(2001)33-36 的文章公开了三维垂直 NAND 串。然而,该 NAND 串只提供了每单元一位元。进一步地,NAND 串的有源区域由相对困难和耗时的工艺形成,该工艺包括侧壁间隔件的重复形成和蚀刻衬底的一部分,这导致了大致圆锥形的有源区域形状。

发明内容

[0003] 一个实施例涉及一种制造多级接触的方法。该方法包括提供工艺过程中的多级装置,包括至少一个装置区域和至少一个接触区域。该接触区域包括构造为台阶图案的多个导电层。该方法还包括在该多个导电层的上方形成共形的蚀刻终止层,在该蚀刻终止层的上方形成第一电绝缘层,在该第一电绝缘层的上方形成共形的牺牲层和在该牺牲层的上方形成第二电绝缘层。该方法还包括蚀刻多个接触开口,该多个接触开口穿过该接触区域的蚀刻终止层、第一电绝缘层、牺牲层和第二电绝缘层,到达该多个导电层。

[0004] 另一个实施例涉及一种制造多级接触的方法。该方法包括提供工艺过程中的多级装置,包括至少一个装置区域和至少一个接触区域。该接触区域包括构造为台阶图案的多个导电层,位于该导电层上方的电绝缘层,位于该绝缘层的上方的具有多个开口的掩模,以及位于该掩模上方的减薄层。该方法还包括蚀刻该减薄层以减小其厚度和宽度,从而暴露在该掩模中的第一开口,蚀刻该电绝缘材料的暴露于该第一开口中的一部分以形成在电绝缘材料中的第一接触开口的一部分;进一步蚀刻该减薄层以减小其厚度和宽度,从而暴露在该掩模中的第二开口。

[0005] 另一个实施例涉及包括至少一个装置区域和至少一个接触区域的多级装置。该接触区域具有多个堆叠导电层。该导电层形成在该接触区域中的台阶图案。该装置还包括在该导电层上方的共形的蚀刻终止层、在该蚀刻终止层上方的第一电绝缘层、在该第一电绝缘层上方的牺牲层和在该牺牲层上方的第二电绝缘层。该装置还包括多个接触开口,延伸穿过该接触区域的蚀刻终止层、第一电绝缘层、牺牲层和第二电绝缘层,到达该多个导电层。该装置还包括多个导电接触。多个电接触的相应的一个位于该多个接触开口的对应的一个中,并且每一个导电接触与该多个导电层的对应的一个电接触。

附图说明

[0006] 图 1A-1B 分别是一个实施例中的 NAND 串的侧视横截面图和俯视横截面图。图 1A 是该装置沿着图 1B 中线 Y-Y' 的侧视横截面图,而图 1B 是该装置沿着图 1A 中线 X-X' 的侧

视横截面图。

[0007] 图 2A 和 2B 分别是另一个实施例中的 NAND 串的侧视横截面图和俯视横截面图。图 2A 是该装置沿着图 2B 中线 Y-Y' 的侧视横截面图,而图 2B 是该装置沿着图 2A 中线 X-X' 的侧视横截面图。

[0008] 图 3 是常规的 NAND 串存储器装置的示意说明。

[0009] 图 4 是示出了栅电极的接触的常规的 NAND 串存储器装置的横截面的扫描电子显微镜 (SEM) 图像。

[0010] 图 5 是制造多级接触的常规方法的示意说明。

[0011] 图 6 是根据一个实施例制造多级接触的方法的示意说明。

[0012] 图 7 是提供图 6 的方法的附加细节的示意说明。

[0013] 图 8 是示出了根据一个实施例的第一(下)介电层的损耗作为第二共形介电层的厚度的函数的图。

[0014] 图 9a 是示出了在第二共形介电层的厚度为 600nm 时第一(下)介电层的损耗作为第三共形介电层的厚度的函数的图。

[0015] 图 9b 是示出了在第二共形介电层的厚度为 400nm 时第一(下)介电层的损耗作为第三共形介电层的厚度的函数的图。

[0016] 图 10a-10b 分别是根据一个实施例的在制造多级接触的方法中的一个步骤的侧视横截面图和俯视横截面图。

[0017] 图 10c-10d 分别是图 10a-10b 的在制造多级接触的方法中的一个后续步骤的侧视横截面图和俯视横截面图。

[0018] 图 10e-10f 分别是图 10a-10b 的在制造多级接触的方法中的一个后续步骤的侧视横截面图和俯视横截面图。

[0019] 图 10g-10h 分别是图 10a-10b 的在制造多级接触的方法中的一个后续步骤的侧视横截面图和俯视横截面图。

具体实施方式

[0020] 将参照附图如下描述本发明的实施例。应理解,以下实施例的意图为描述本发明示例的实施例,而不是限制本发明。

[0021] 单片三维存储器阵列是多个存储器级形成在一个例如半导体晶片的单衬底之上,而没有插入衬底。术语“单片”指阵列的每一级的层直接沉积在该阵列的每一个下层的级的层上。相反地,二维阵列可以被分别形成然后被封装在一起以形成非单片存储器装置。例如,如在 Leedy 的题为“Three Dimensional Structure Memory”的美国专利号 5915167 中,已通过在分立的衬底上形成存储器级并将该存储器级相互粘附来构造非单片堆叠存储器。在键合前可以减薄衬底或者将其从存储器级中移除。但是由于该存储器级一开始形成在分立的衬底上,因此这样的存储器不是真正的单片三维存储器阵列。

[0022] 本发明的实施例涉及制造例如单片 3D 阵列的多级存储器阵列的接触的方法。在一个实施例中,多级存储器装置包括至少一个装置区域和至少一个接触区域,存储器单元(例如垂直 NAND 串 180)位于该至少一个装置区域,多级接触位于该至少一个接触区域。如图 3 和 4 所示以及以下更详细的讨论,多级垂直 NAND 存储器阵列的控制栅的远端以台阶式

构造布置。以此方式,通过从存储器阵列的上表面向下至台阶 120 蚀刻在四周的介电层中的开口 130 的阵列以及在该开口 130 中沉积接触金属以接触该台阶 120,可以实现到单独控制栅极的电接触。在制作多级存储器阵列的控制栅级的接触的常规方法中,在暴露最深的台阶之前,会严重地过蚀浅的台阶。

[0023] 本发明的其它实施例提供了单片三维存储器装置阵列,例如垂直 NAND 串的阵列。该 NAND 串垂直取向,从而至少一个存储器单元位于另一个存储器单元的上方。该阵列允许 NAND 装置的垂直定标,以提供每单位面积的硅或者其它半导体材料的更高密度存储器单元。

[0024] 在一些实施例中,如图 1A、2A 和 3 所示,单片三维 NAND 串 180 包括半导体沟道 1,该半导体沟道 1 具有至少一个端部分,该端部分基本垂直于衬底 100 的主平面 100a 延伸。例如,如图 1A 和 2A 所示,该半导体沟道 1 可以具有柱形形状,并且整个柱形的半导体沟道基本垂直于衬底 100 的主平面 100a 延伸。在这些实施例中,如图 1A 和 2A 所示,该装置的源/漏电极可以包括提供在该半导体沟道 1 的下方的下电极 102 和形成在该半导体沟道 1 的上方的上电极 202。或者,如图 3 所示,该半导体沟道 1 可以具有 U 型管道的形状。该 U 形管道形状的半导体沟道 1 的两个翼部分 1a 和 1b 可以基本垂直于该衬底 100 的主平面 100a,并且该 U 形管道形状半导体沟道 1 的连接该两个翼部分 1a 和 1b 的连接部分 1c 基本平行于衬底 100 的主平面 100a 延伸。在这些实施例中,源极或者漏极区域之一区域 202₁ 从上方接触该半导体沟道 1 的第一翼部分,而源极或者漏极区域的另一个区域 202₂ 从上方接触该半导体沟道 1 的第二翼部分。可选的体接触电极(未示出)可以设置在衬底 100 中,以提供从下方接触该半导体沟道 1 的连接部分的体接触。该 NAND 串的选择栅极(SG)或者存取晶体管如图 3 所示。在如图 3 示出的实施例中,可以通过源线(SL)连接相邻 NAND 串的源区域 202₂,而可以通过位线(BL)连接相邻 NAND 串的漏区域 202₁。在该 U 型的实施例中,狭缝 210 分开该 U 形管道形状的两个翼部分 1a 和 1b。可以用介电材料填充该狭缝 210。

[0025] 在一些实施例中,如图 2A-2B 所示,半导体沟道 1 可以是被填充的结构。在一些另外的实施例中,如图 1A-1B 所示,半导体沟道 1 可以是中空,例如是填充有绝缘填充材料 2 的中空圆柱体。在这些实施例中,可以形成绝缘填充材料 2 以填充由该半导体沟道 1 围绕的中空部分。

[0026] 衬底 100 可以是任何现有技术已知的半导体衬底,例如单晶硅、例如硅-锗或者硅-锗-碳的 IV-IV 族化合物、III-V 族化合物、II-VI 族化合物、在这类衬底上的外延层或者例如氧化硅、玻璃、塑料、金属或者陶瓷衬底的任何其它半导体材料或者非半导体材料。该衬底 100 可以包括制备在其上的集成电路,例如用于存储器装置的驱动电路。

[0027] 任何合适的半导体材料可以用于半导体沟道 1,例如硅、锗、锗化硅,或者例如 III-V 族, II-VI 族的其它化合物半导体材料,或者导电或者半导电的氧化物等材料。半导体材料可以是非晶的、多晶的或者单晶的。该半导体沟道材料可以由任何合适的沉积方法形成。例如,在一个实施例中,该半导体沟道材料由低压化学气相沉积(LPCVD)形成。在一些其它的实施例中,该半导体沟道材料可以由通过再结晶初始沉积的非晶半导体材料形成的再结晶的多晶半导体材料形成。

[0028] 绝缘填充材料 2 可以包括任何电绝缘材料,例如氧化硅、氮化硅、氮氧化硅或者其它高 k 绝缘材料。

[0029] 如图 1A 至 1B、2A 至 2B 和 3 所示,该单片三维 NAND 串还包括多个控制栅极 (CG) 3。该控制栅电极 3 可以包括具有带状的部分,该部分基本平行于衬底 100 的主平面 100a 延伸。该多个控制栅电极 3 包括位于第一装置级 (例如,装置级 A) 中的至少一个第一控制栅电极 3a 和位于第二装置级 (例如装置级 B) 中的第二控制栅电极 3b,该第二装置级位于该衬底 100 的主平面 100a 的上方和该装置级 A 的下方。该控制栅极的材料可以包括现有技术已知的任何一种或者多种合适的导电或者半导体控制栅极材料,例如掺杂多晶硅、钨、铜、铝、钽、钛、钴、氮化钛或者它们的合金。例如,在一些实施例中,优选多晶硅以便容易处理。

[0030] 阻挡介电体 7 位于与控制栅极 3 相邻或者被其围绕。该阻挡介电体 7 可以包括位于与该多个控制栅电极 3 的相应的一个接触的多个阻挡介电部分,例如如图 1A-1B 和图 2A-2B 所示,位于装置级 A 中的第一介电体部分 7a 和位于装置级 B 中的第二介电体部分 7b 分别与控制电极 3a 和 3b 接触。或者,如图 3 所示,阻挡介电体 7 可以是连续的。

[0031] 单片三维 NAND 串也可以包括多个分离的电荷储存部分 9,每一个电荷储存部分 9 位于该阻挡介电体 7 和该沟道 1 之间。类似地,该多个分离电荷储存部分 9 包括位于装置级 A 中的至少一个第一分离电荷储存部分 9a 和位于装置级 B 中的第二分离电荷储存部分 9b。或者,如图 3 所示,该电荷储存部分可以是连续的。也就是说,该电荷储存部分可以包括在连续电荷储存层的局部区域。

[0032] 单片三维 NAND 串的隧道介电体 11 位于该多个分离电荷储存部分 9 的每一个和该半导体沟道 1 之间。该隧道介电体 11 可以包括多个阻挡介电部分 11 或者介电材料的连续层。

[0033] 该阻挡介电体 7 和隧道介电体 11 可以独立地选自任何一个或者更相同或者不同的绝缘材料,例如氧化硅、氮化硅、氮氧化硅或者其它高 k 介电材料。

[0034] 该电荷储存部分 9 可以包括分离或者连续的导体 (例如,金属或者金属合金,例如钛、铂、钌、氮化钛、氮化钨、氮化钽、氮化锆或者金属硅化物,例如硅化钛、硅化镍、硅化钴,或者它们的组合) 或者半导体 (例如,多晶硅) 浮置栅、导电纳米颗粒或者分离或者连续的电荷储存介电体 (例如,氮化硅或者其它介电材料) 结构。例如,在一些实施例中,分离电荷储存部分 9 是分离电荷储存介电结构,其每一个包括位于相应的蛤形阻挡介电部分 7 中的氮化物结构,其中氧化硅阻挡介电部分 7、氮化物结构 9 和氧化硅隧道介电体 11 形成该 NAND 串的氧化物-氮化物-氧化物的分离电荷储存结构。或者,可以使用多晶硅浮置栅极。

[0035] 图 4 是示出常规垂直 NAND 存储器装置的横截面的扫描电子显微镜 (SEM) 的图像。如图 4 所示,接触 132 从接触区域 134 的顶表面延伸至控制栅极 3 的栅电极台阶 120。如以下更详细的讨论,通过用例如铜或者铝或者它们的硅化物的导电材料填充形成在电绝缘 (介电) 材料 124 中的过孔,来制造接触 132。为形成如图 4 所示的台阶图案,构造该控制栅电极 3,从而第一导电层 (例如在层的堆叠中的下层) 包括横向延伸超过第二导电层 (例如,在该堆叠中更高的层) 的一部分。接触开口包括延伸至该第一导电层 (例如,120a) 的第一部分的第一接触开口 (例如,图 7 中的 130A) 和延伸至该第二导电层 (例如,120b) 的上表面的第二接触开口 (例如,图 7 中的 130B)。例如,该第一导电层 (例如,120a) 可以是第一控制栅电极 3 的一部分,从装置区域延伸至接触区域 134;并且该第二导电层 (例如,

120b) 可以是第二控制栅电极 3 的一部分, 从装置区域延伸至接触区域 134。

[0036] 图 5 示出了在使用制造上述图 4 讨论的多级接触的常规方法中的浅侧的问题。在常规方法中, 控制栅台阶 120 覆盖有堆叠的介电 (电绝缘) 材料层。第一介电层是共形的蚀刻终止层 122。该共形的蚀刻终止层 122 可以由例如氮化硅的任何合适的材料制成。该共形的蚀刻终止层 122 覆盖有由不同于层 122 的材料制成的第二介电层 124。该第二介电材料可以由包括例如氧化硅 (例如, SiO_2) 的氧化物的任何合适的材料制成。该第二介电层 124 不是共形的。也就是说, 介电层 124 的厚度 ($h_1, h_2, h_3, h_4 \dots h_i$) 随着每一个台阶 120 而变化, 从而该第二介电层 124 的上表面 124a 与衬底 100 的距离在所有台阶 120 中是相同的。第三介电层, 即牺牲阻挡层 126, 沉积在该第二介电层 124 的上方。该牺牲阻挡层 126 可以由任何合适的材料制成, 例如氮化硅 (例如, 优选与共形的蚀刻终止层 122 相同但与第二介电层 124 不相同的材料)。之后, 第四介电层 128 沉积在该牺牲阻挡层 126 上。第四介电层 128 可以由包括例如氧化硅 (例如, SiO_2) 的氧化物的任何合适的材料制成。

[0037] 为制造控制栅极台阶 120 的接触, 从该第四介电层 128 的顶表面 128a, 穿过该第四介电层 128、该牺牲阻挡层 126 和该第二介电层 124, 蚀刻开口 130A-130E。一般地, 在第一蚀刻步骤中非选择性地蚀刻 (即, 用以基本相同的速率蚀刻所有材料的蚀刻剂蚀刻) 该第四介电层 128 和该牺牲阻挡层 126。然后选择性地蚀刻 (即, 用蚀刻一种材料 (例如, 第二介电材料 124) 基本比下层的材料 (例如, 蚀刻终止层 122) 更快 (例如, 2-10 倍或者更快) 的蚀刻剂蚀刻), 从而开口在该蚀刻终止层 122 上停止。

[0038] 然而, 当蚀刻开口 130A-130E 时, 常见的是较浅的开口 (例如, 130E、130D、130C) 先于较深的开口 (例如, 130A) 穿过蚀刻终止层 122, 到达该蚀刻终止层 122。随着级 (台阶) 数目的增加, 这尤其成为问题。不限制在例如多级 NAND 装置的多级存储器装置中的级的数目, 其可以包括, 例如 2 至 256 级, 例如 4 至 128 级, 例如 8 至 64 级, 例如 16 至 32 级。通过将例如 Cu、Al、它们的合金、或者硅化物 (例如, Ti、Ni 或者 Co 硅化物) 的导电材料沉积在开口 130A-130E 中, 完成接触。

[0039] 图 6 和 7 是制造多级接触的第一实施例方法的示例说明。在该实施例中, 控制栅台阶 120 覆盖有介电材料堆叠, 包括: 如上描述的蚀刻终止层 122、第二介电层 124、牺牲阻挡层 126 和第四介电层 128。然而, 与图 5 的常规的堆叠相反, 该第二介电层 124 是共形的层。也就是说, 该第二介电层 124 的厚度 ($h_1, h_2, h_3, h_4 \dots h_i$) 对于所有的台阶 120 基本相同 (例如, $h_1 \approx h_2 \approx h_3 \approx h_4 \approx h_i$), 并且该第二介电层 124 的顶表面 124a 的形状跟随台阶 120。此外, 在该实施例中, 牺牲阻挡层 126 也优选是共形的 (例如, 对于所有的台阶 120, 厚度相同)。优先地, 层 122 和 126 由相同的第一材料制成, 而层 124 和 128 由不同于该第一材料的相同的第二材料制成。在一个实施例中, 该蚀刻终止层 122 和该牺牲阻挡层 126 由例如氮化硅的氮化物制成。也可以使用其它材料。该第二介电层 124 和该第四介电层 128 由例如氧化硅的氧化物制成。也可以使用其它介电材料。

[0040] 在该实施例的第一步骤中, 在第一蚀刻步骤 701 中, 选择性地蚀刻 (即, 用蚀刻该第四介电层 128 的材料比蚀刻该牺牲阻挡层 126 的材料更快的蚀刻剂 (具有第一蚀刻化学物质)) 蚀刻该第四介电层 128, 穿过图 7 示出的在光致抗蚀剂或者其它掩模 300, 302 中的孔。较深的开口 (例如, 130A, 130B) 停止在该牺牲阻挡层 126 上。较浅的开口 (例如, 130E, 130D, 130C) 可以完全穿过该牺牲阻挡层 126。然而, 由于在该步骤中使用了选择性的蚀刻,

当选择性的蚀刻剂到达该阻挡层 126 时,较浅的开口 130E,130D,130C 的蚀刻速率减慢,导致在该第一蚀刻步骤 701 中相对小的过蚀进第二介电层 124。这样,第一蚀刻化学物可以用于使用该牺牲阻挡层 126 作为蚀刻终止,选择性地蚀刻多个接触开口 130A 至 130E 的第一部分,通过该第四介电层 128。

[0041] 在第二蚀刻步骤 702 中,选择性地蚀刻(即,用蚀刻该牺牲阻挡层 126 的材料比该第二介电层 124 的材料更快的蚀刻剂蚀刻)在较深开口 130A,130B 中的阻挡层 126。当较深开口 130A,130B 到达该第二介电层 124 时,停止蚀刻。由于该第二蚀刻步骤 702 也使用了选择性的蚀刻,相对于将牺牲阻挡层 126 从较深的开口 130A,130B 的去除,在该第二介电层 124 中的浅开口 130E,130D,130C 的继续的蚀刻相对慢。优选地,所有的开口 130A-130E 停止在该第二介电层 124 中。这样,第二蚀刻化学物可以用于使用该第二介电层 124 作为蚀刻终止,选择性地蚀刻多个接触开口 130A-130E 的第二部分,穿过该牺牲阻挡层 126。

[0042] 在第三蚀刻步骤 703 中,选择性地蚀刻(例如,用蚀刻该第二介电层 124 的材料比该蚀刻终止层 122 的材料更快的蚀刻剂蚀刻)该第二介电层 124。当该第二介电层 124 从较深开口 130A,130B 去除时(即,当到达该蚀刻终止层 122 时),停止蚀刻。作为使用共形的第二介电层 124 和共形的牺牲阻挡层 126 连同多个选择性蚀刻步骤的结果,最小化了最后蚀刻的深度的差别。可以形成较深的开口 130A,130B,而不用穿过该蚀刻终止层 122 到达在浅开口 130E,130D,130C 中的控制栅极台阶 120。这样,第三蚀刻化学物可以用于使用该共形的蚀刻终止层 122 为蚀刻终止,选择性地蚀刻接触开口 130A-130E 的第三部分,穿过该第二介电层 124。当蚀刻完成到最深的台阶 120e 上方的蚀刻终止层时,在最浅的台阶 120a 上的蚀刻终止层 122 没有被穿透。

[0043] 可以执行第四蚀刻步骤以去除在开口 130A-130E 中的该蚀刻终止层 122,从而从第四介电层 128 的顶表面 128a 到控制栅极台阶 120 提供过孔。这样,第四蚀刻化学物可以用于选择性地蚀刻接触开口 130A-130E 的第四部分,穿过该共形的蚀刻终止层 122,到达导电层 120。

[0044] 在一个实施例中,该第一蚀刻化学物和第三蚀刻化学物是相同的,该第二蚀刻化学物和第四蚀刻化学物是相同的,并且第一蚀刻化学物和第二蚀刻化学物不相同。用于氧化硅(例如,层 124 和 128)的选择性蚀刻的选择率可以是用于氮化硅(例如,层 122,126)的选择性蚀刻的选择率的 13-15 倍,而用于氮化硅的选择性蚀刻的选择率可以是用于氧化硅的选择性蚀刻的选择率的 4-6 倍。

[0045] 在一个实施例中,该共形的蚀刻终止层 122、该第二介电层 124 和该牺牲阻挡层 126 的每一个具有基本均匀的厚度,并且布置为在接触区域 134 中的该多个导电层 120 的上方台阶图案。该第四介电层 128 具有可变的厚度和基本平面的上表面 128a。该第四介电层 128 在该第一导电层的第一部分(例如,台阶 128e)的上方比在该第二导电层(例如,台阶 120d)的上方更厚。最浅的台阶 120a 位于在蚀刻方向中距离该第四介电层 128 的顶表面 128a 最短的距离。最深的台阶 120e 位于在该蚀刻方向中距离该第四介电层 128 的顶表面 128a 最长的距离。

[0046] 如上讨论的,可以通过将例如 Cu、Al、它们的合金或者硅化物(例如,Ti、Ni 或者 Co 硅化物)的导电材料沉积在开口 130A-130E 中来形成接触 132A-132E。例如,形成在第一接触开口 130A 中的第一导电接触 132A 和在第二接触开口 130B 中的第二导电接触 132B(其中

该第一导电接触 132A 比该第二导电接触 132B 延伸得更深)。可以形成多个导电接触 132, 其中该多个导电接触 132 的每一个位于该多个接触开口 130 的相应的一个中, 并且每一个导电接触 132 与该多个导电层 120 的对应的一个电接触。

[0047] 图 8 示出了根据一个实施例, 该蚀刻终止层 122 的厚度损耗作为该共形的第二介电层 124 的厚度的函数。在这些模拟中, 牺牲阻挡层 126 的厚度固定在 150nm, 并且孔 130A 和 130E 的深度分别为 2480nm 和 780nm。图 8 示出了对于共形的第二介电层 124 的厚度范围约为 275-630nm, 在浅的开口中的蚀刻终止层 122 的损耗保持不变 (小于 30nm, 例如 25-29nm)。更厚的共形的第二介电层 124 的使用导致来自较深的开口的蚀刻终止层 122 的材料损耗的增加。然而, 来自较深的开口的损耗总是小于来自浅开口的材料损耗 (例如, 损耗的差值小于 20nm, 例如小于 12-19nm)。这样, 牺牲阻挡层 126 可以至少为 150nm 厚, 例如 15-250nm 厚。第二介电层 124 可以为 275-630nm 厚。

[0048] 图 9a 和 9b 示出了对于 (a) 第二共形层的厚度为 600nm 以及对于 (b) 第二共形层的厚度为 400nm, 该蚀刻终止层 122 的厚度损耗作为该牺牲阻挡层 126 的厚度的函数。如图中所示, 对于浅开口, 蚀刻终止层 122 的厚度损耗随着牺牲阻挡层 126 的厚度增加而减小。此外, 在深开口中的蚀刻终止层 122 的厚度损耗对牺牲阻挡层 126 的厚度不敏感。

[0049] 图 10a-10h 示出了根据另一个实施例制造多级接触的方法。图 10a、10c、10e 和 10g 是示出该方法中步骤的侧视横截面图, 而图 10b、10d、10f 和 10h 分别是与图 10a、10c、10e 和 10g 相对应的俯视横截面图。依次执行图 10a-10h 示出的步骤以制造图 1 和 2 示出的装置结构。也就是说, 在工艺过程中装置上制造多极接触。

[0050] 多级接触区域包括构造为台阶图案 120 的多个导电层。在该实施例中的多级接触区域还包括位于该导电层 120 上方的电绝缘层 (例如, 第二介电层 124)。该多级接触区域还可以选择性地包括位于该导电层 120 和该电绝缘层 124 之间的蚀刻终止层 122。在此实施例中, 可以省略牺牲阻挡层 126 和第四介电层 128。具有多个开口 304A-304E 的掩模 300 (例如, 硬掩模, 例如氧化硅、氮化硅、多晶硅等的一层或者多层) 位于该电绝缘层 124 的上方。减薄层 302 (例如, 光致抗蚀剂或者宽度和厚度可以由蚀刻或者灰化减薄的其它材料) 位于该掩模 300 的上方。

[0051] 在图 10a 和 10b 中示出的非限制性的实施例中, 随着位于最深台阶 120 上方的最大直径的开口 304A 到位于最浅开口 304E 上方的最小直径的开口 304e, 开口 304A-304E 的直径逐渐减小。这是有利的, 因为蚀刻在较大直径的开口中比在较小直径的开口中进行得更快。这样, 可以通过使用不同直径的开口, 实施对于该蚀刻工艺的附加控制。如示出的, 多级接触区域包括五个级 120。然而, 如上所讨论的, 没有限制在例如多级 NAND 装置的多级存储器装置中的级数目, 并且其可以包括, 例如 2 至 256 级, 例如 4 至 128 级, 例如 8 至 64 级, 例如 16 至 32 级。

[0052] 如图 10a 和 10b 所示, 该方法包括蚀刻或者部分灰化减薄层 302 以降低其厚度和宽度, 从而暴露在该掩模 300 中的第一开口 304A。其它的开口 304B 至 304E 保持由厚度/宽度降低的减薄层 302 覆盖。如图 10c-10d 所示, 可以蚀刻暴露在该第一开口 304A 中的电绝缘材料 124, 以形成在该电绝缘材料 124 中的第一接触开口 130A 的一部分。然后, 如图 10e 和 10f 所示, 可以蚀刻或者部分灰化减薄层 302 以降低其厚度和宽度, 从而暴露在该掩模 300 中的第二开口 304B。如图 10g 至 10h 所示, 可以蚀刻暴露在该第一和第二开口 304A,

304B 中的电绝缘材料 124, 以形成在该电绝缘材料 124 中的第二接触开口 130B 的一部分和进一步延伸接触开口 130A。然后可以重复该蚀刻和减薄步骤直到形成对于每一个台阶 120 的在该电绝缘材料 124 (如果示出, 还有层 122) 中的接触开口 130A-130E。例如, 还可以蚀刻或者灰化该减薄层 302 以减小其厚度和宽度, 从而暴露在该掩模 300 中的第三开口并且蚀刻暴露在该第一和第二开口 130A, 130B 中的电绝缘材料 124 的一部分, 以形成在该电绝缘材料中的第二接触开口 130A 的第一部分和第一接触开口 130A 的第二部分。该第一接触开口 130A 比该第二接触开口 130B 更深。在形成所有的开口 130A-130E 之后, 可以在该开口 130A-130E 中沉积例如 Cu、Al、它们的合金或者硅化物的导电材料, 以形成每个台阶的接触 132。该方法可以包括连续蚀刻减薄层 302 直到暴露在该掩模中的所有的多个开口 130A 至 130E, 并且蚀刻多个接触开口的相应一个穿过在掩模 300 中的每一个开口, 到达该多个导电层 120a-120e。

[0053] 在一个实施例中, 在相同的蚀刻步骤中, 可以使用相同的蚀刻化学物, 同时蚀刻该电绝缘材料 124 和该减薄层 302。在另一个实施例中, 在不同的蚀刻步骤中, 使用不同的蚀刻化学物, 蚀刻该电绝缘材料 124 和该减薄层 302。

[0054] 尽管前述参考特定的优选的实施例进行了描述, 但是应理解, 本发明并不受限于此。本领域普通技术人员可以对公开的实施例进行各种修改, 并且这些修改意图落在本发明的范围内。本文引用的所有的出版物、专利申请和专利的全部内容通过引用并入本文。

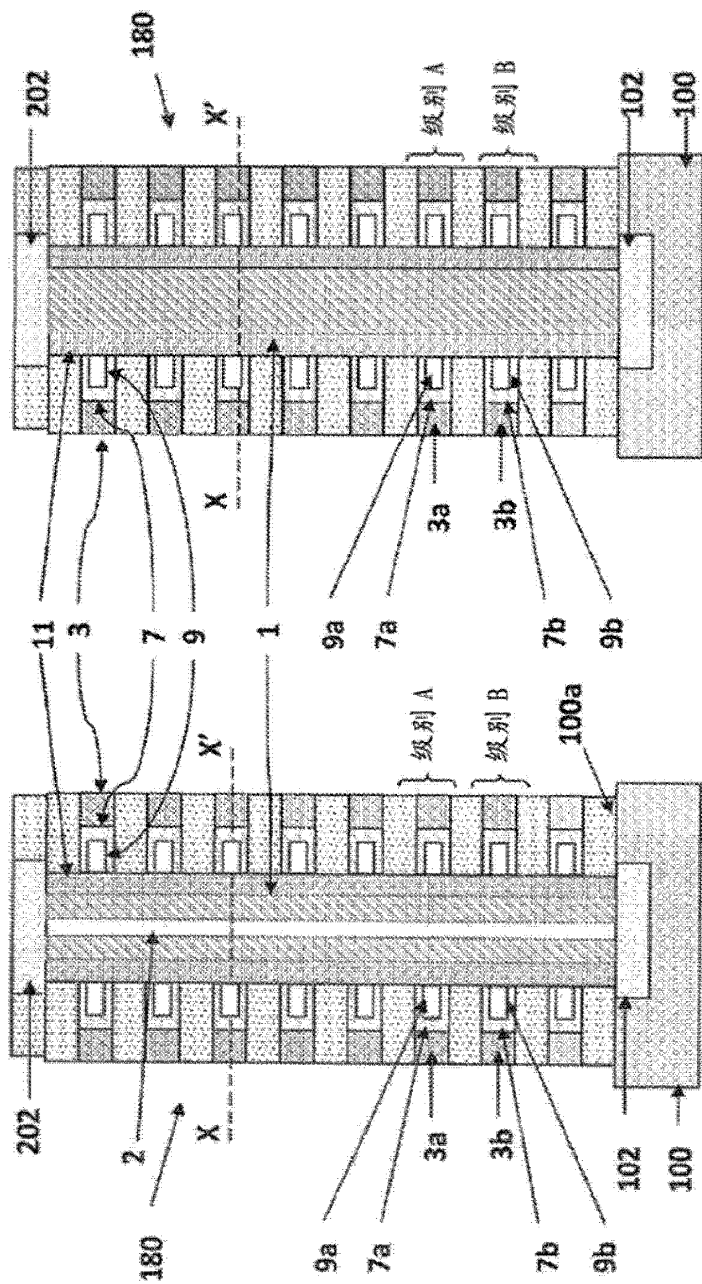


图 1A

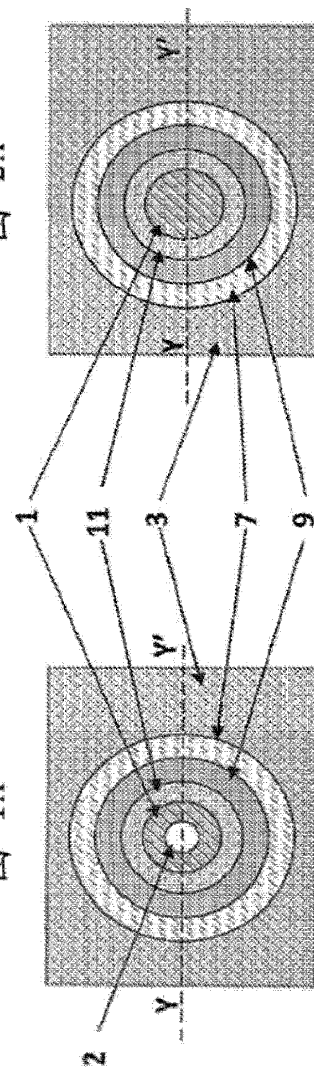


图 1B

图 2A

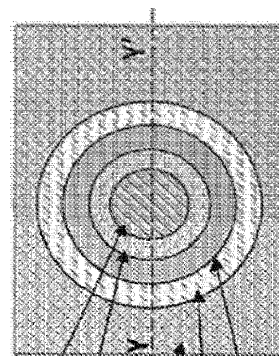


图 2B

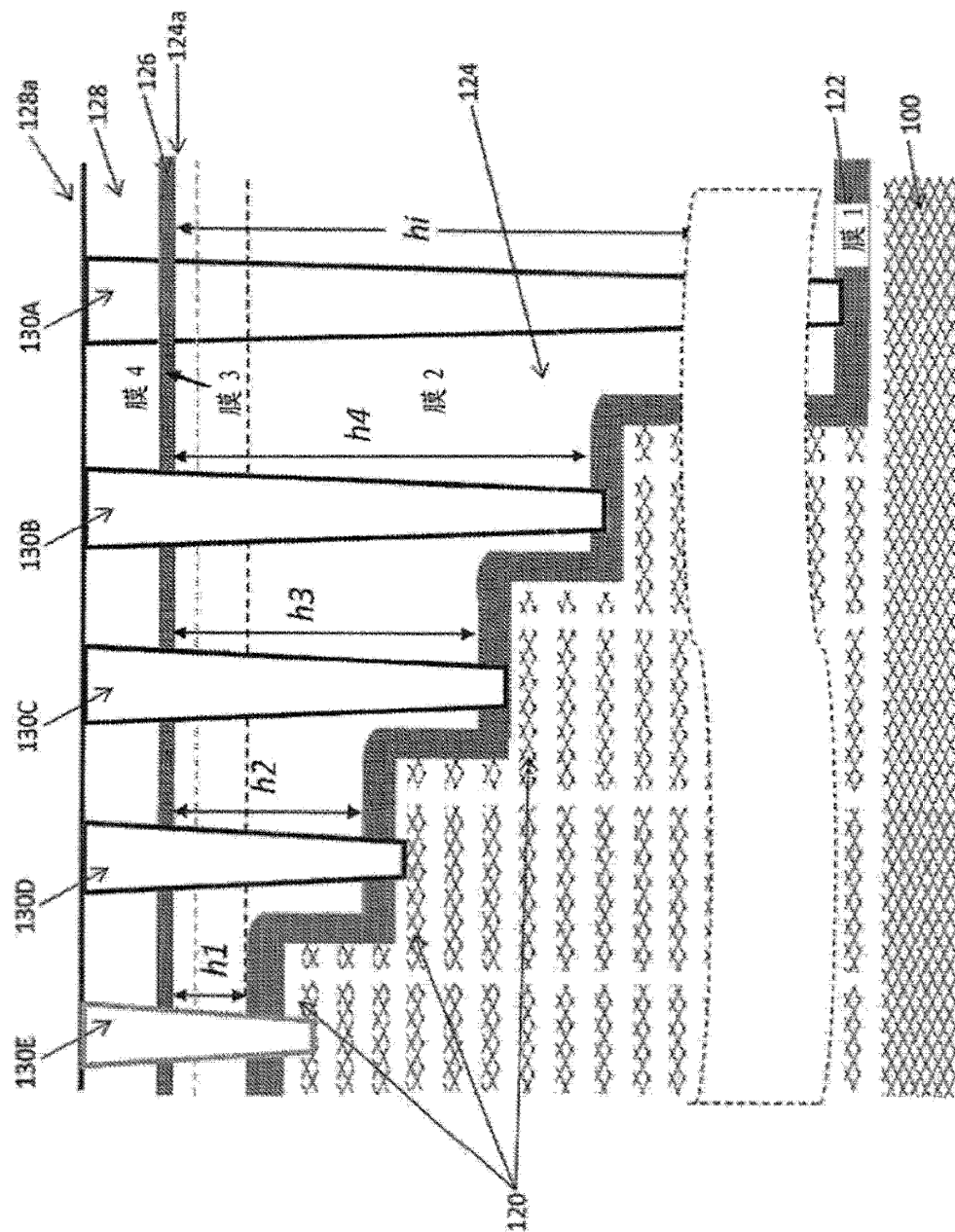


图 5 现有技术

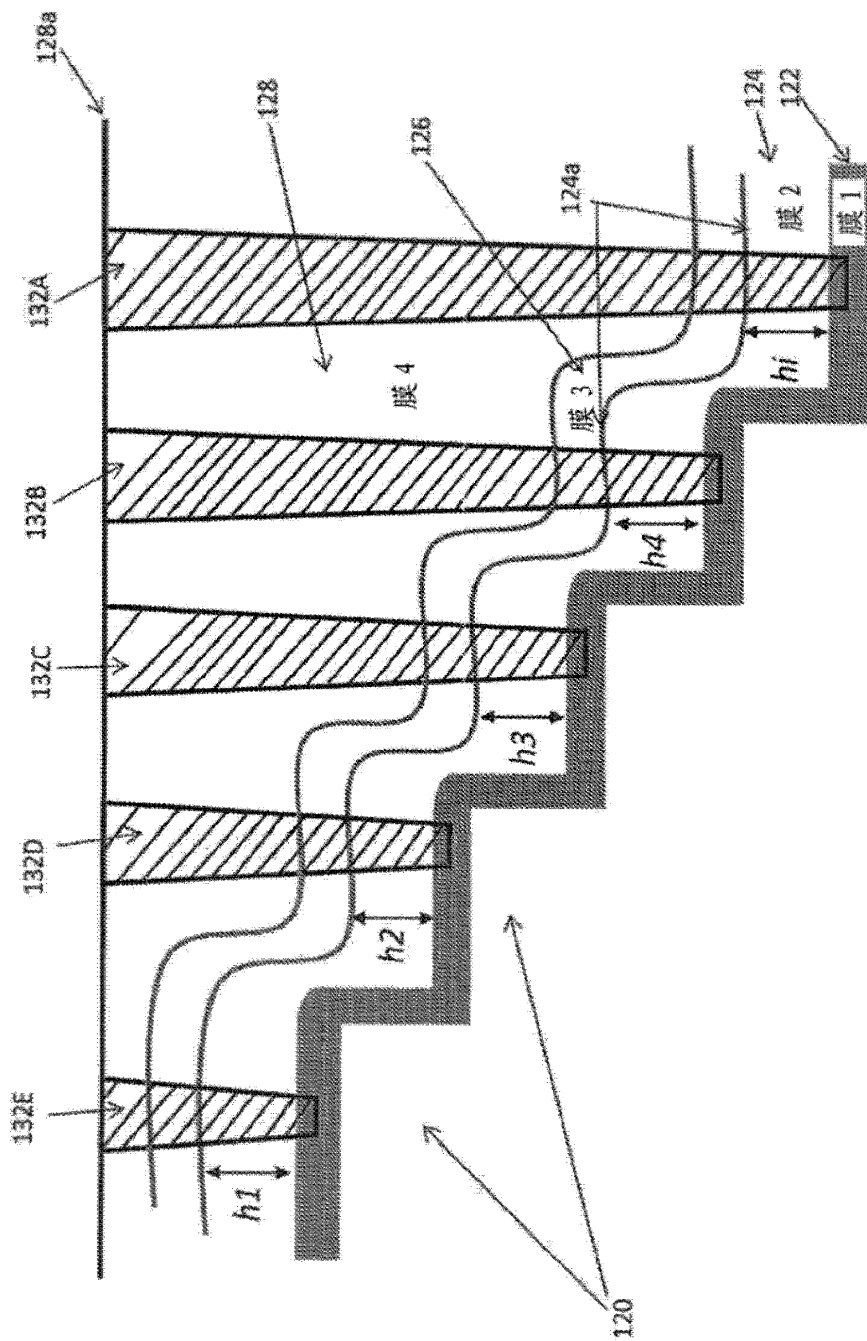


图 6

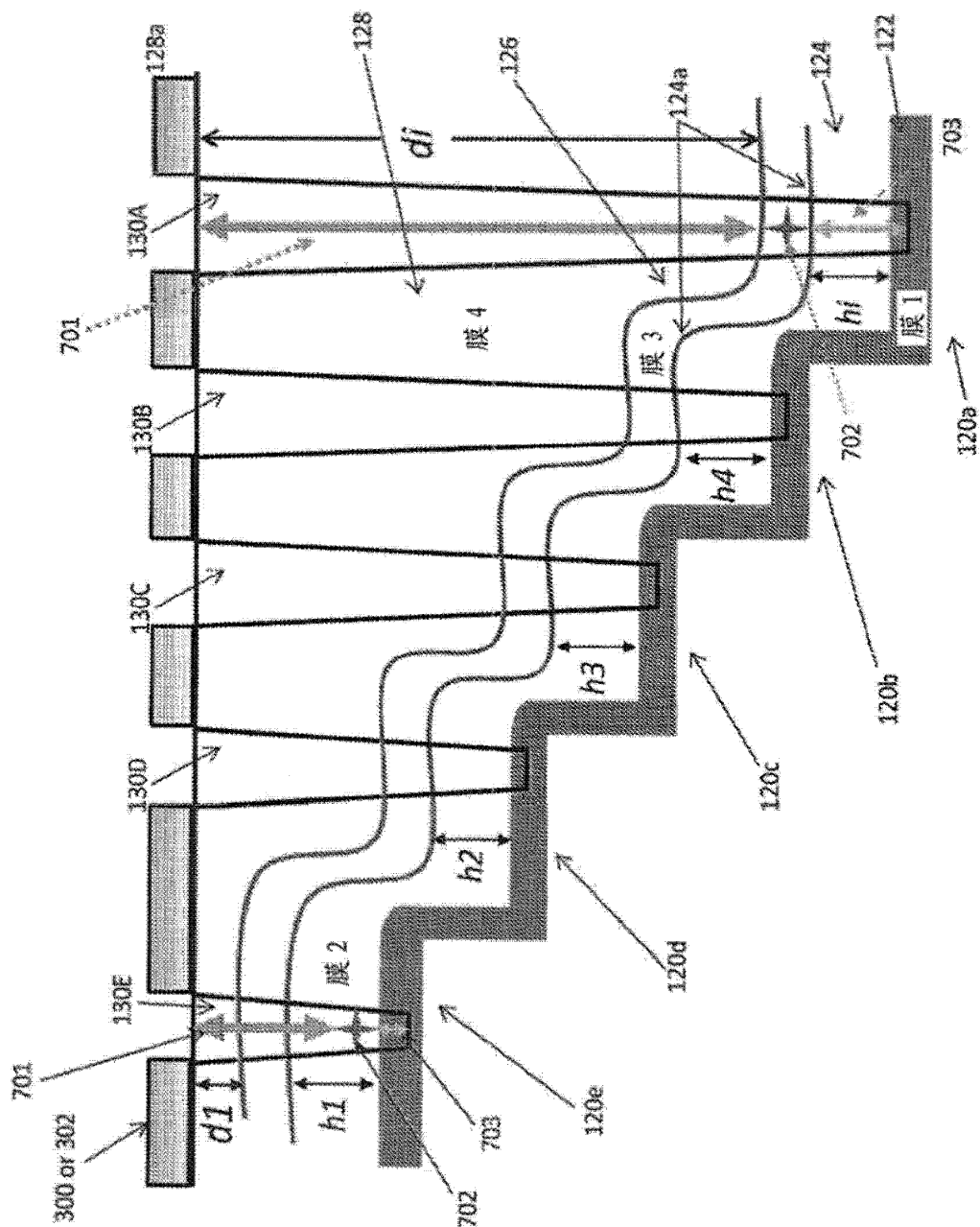


图 7

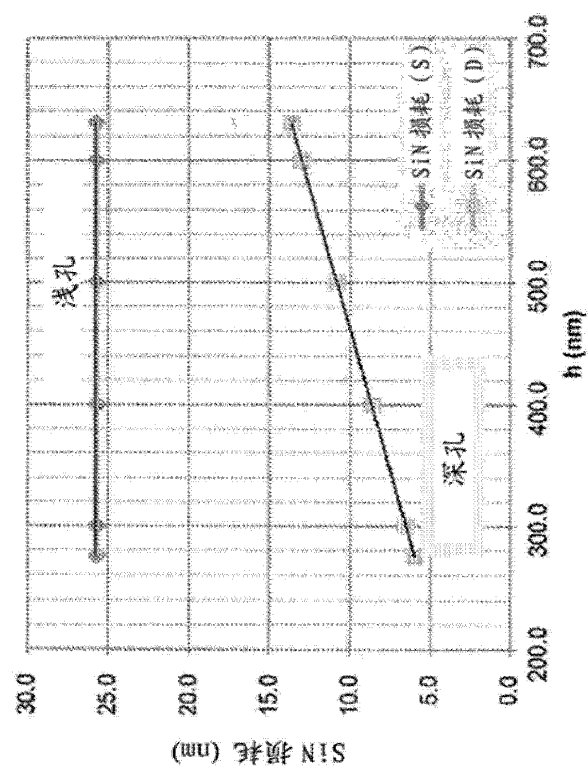


图 8

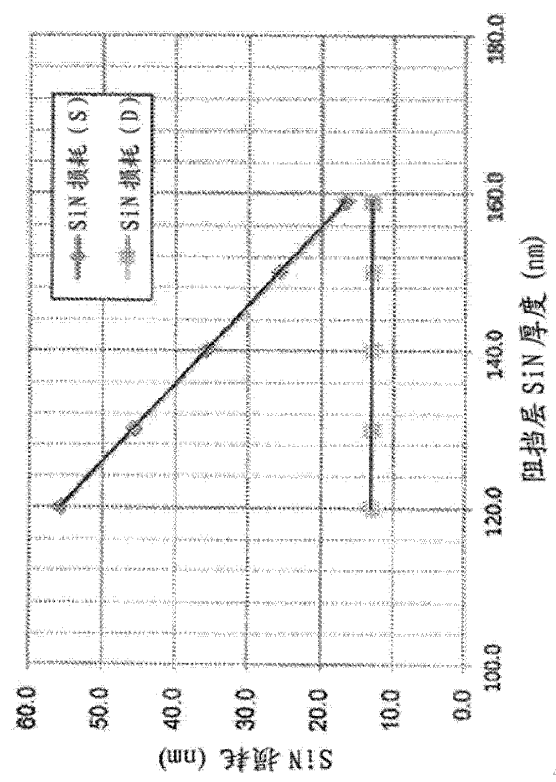


图 9a

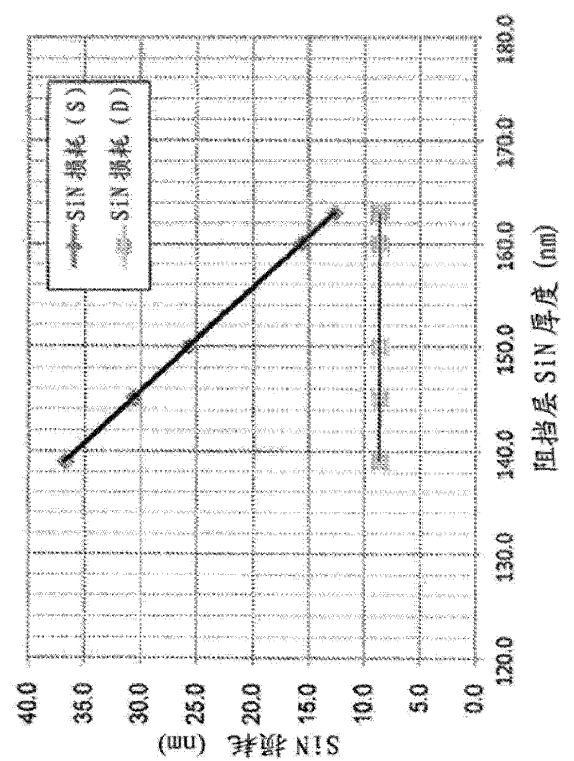


图 9b

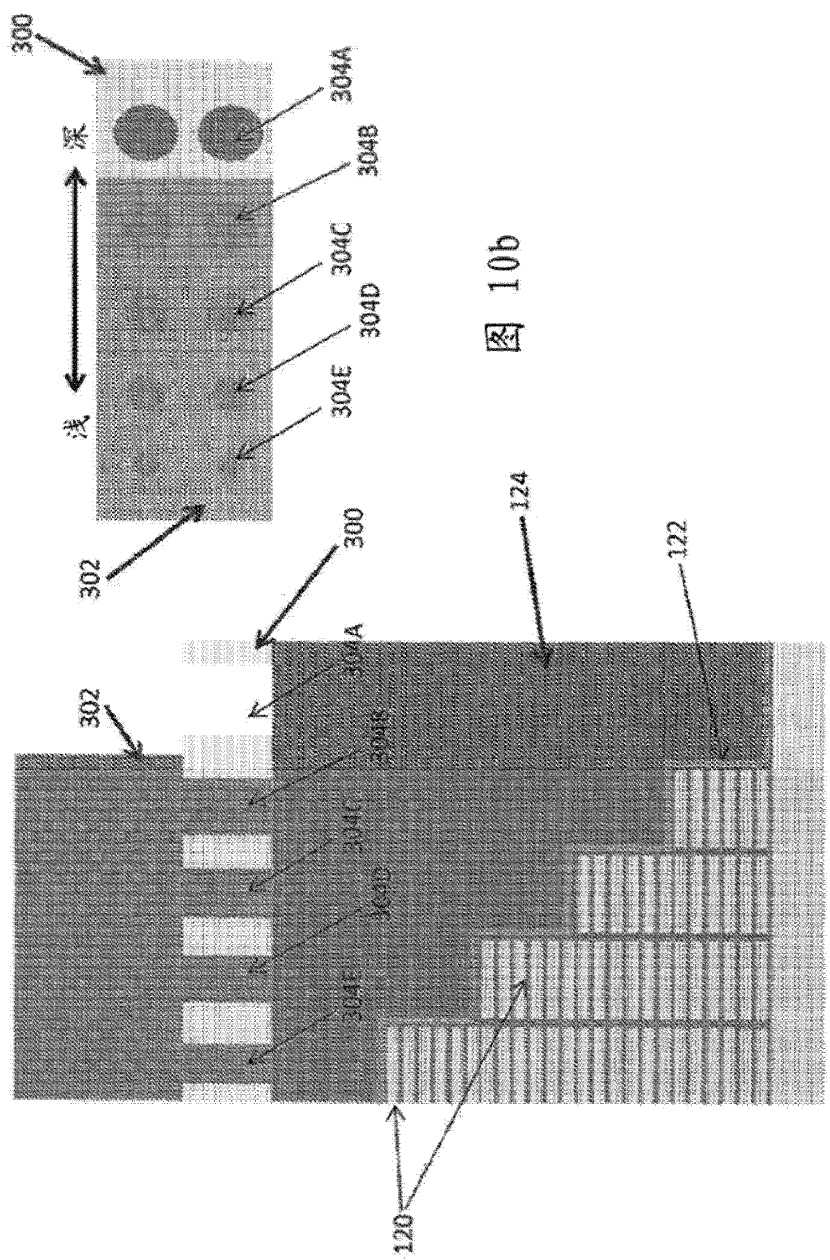
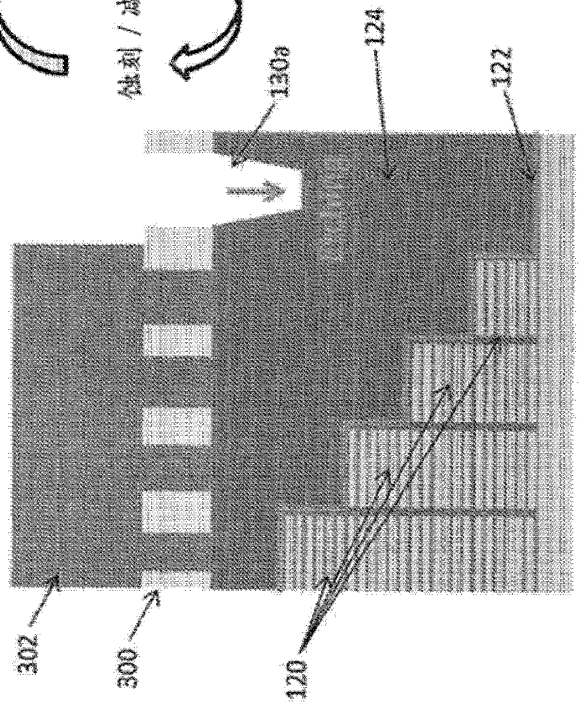
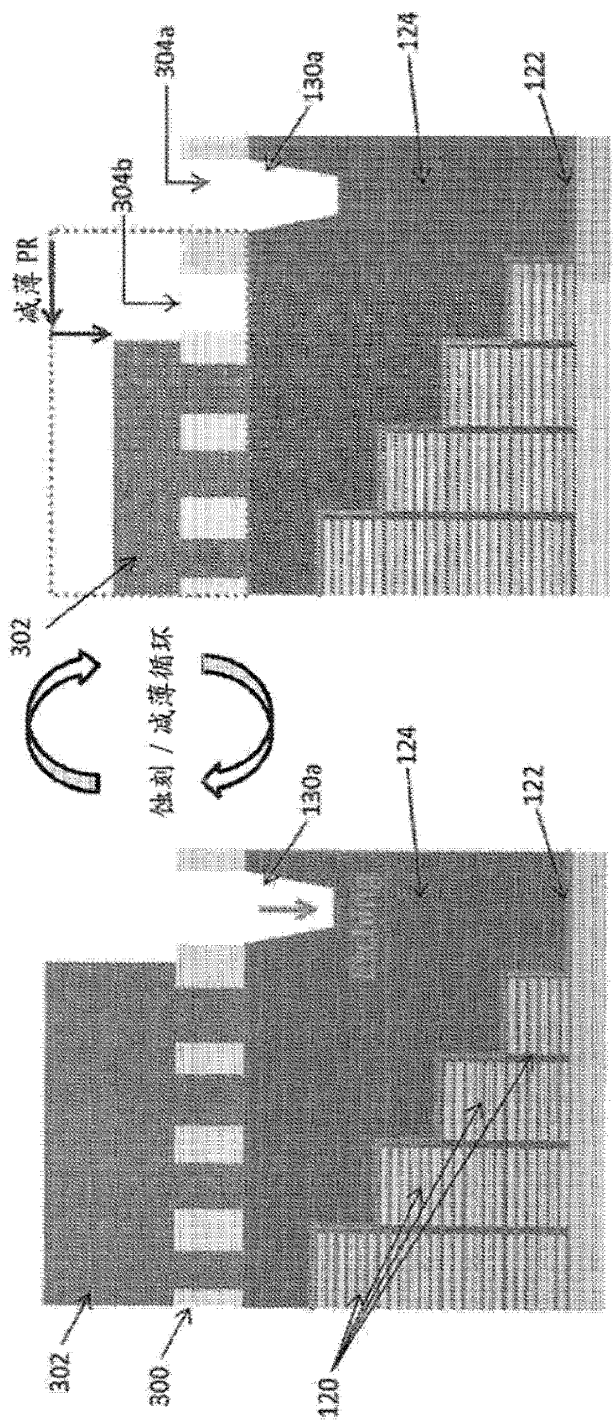
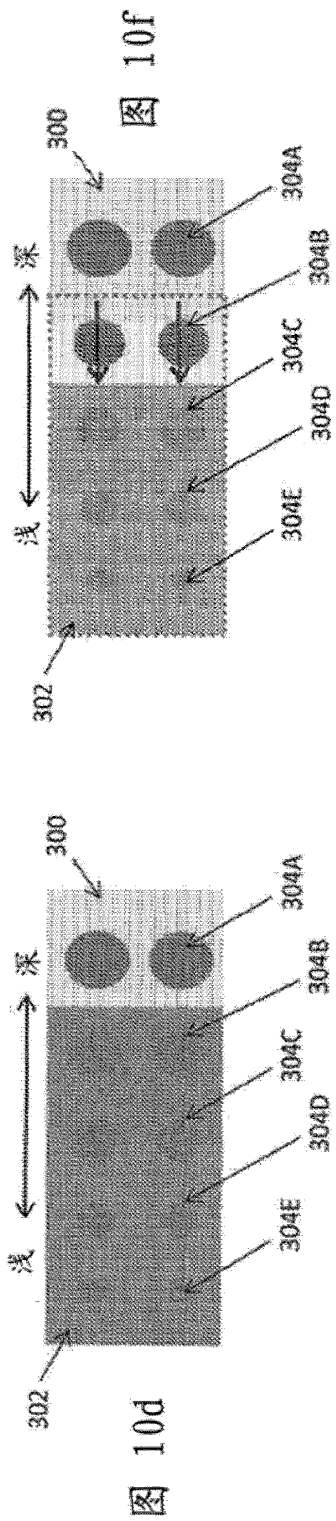


图 10a

图 10b



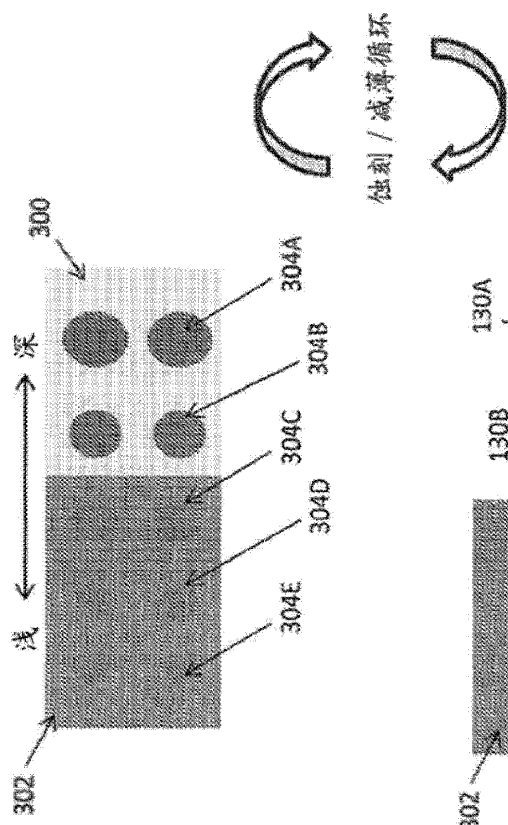


图 10h

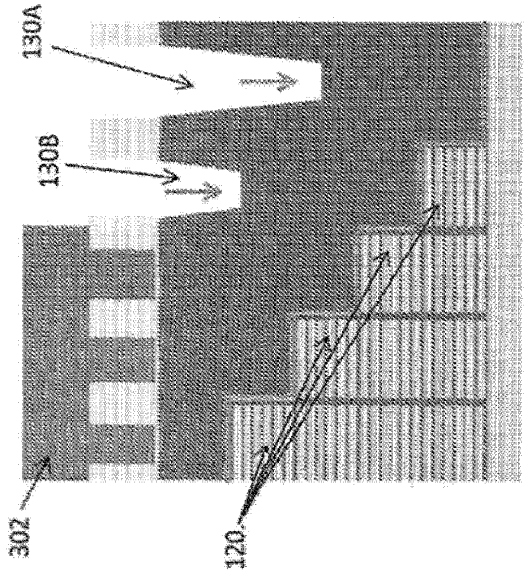


图 10g

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference P2018TC570	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/CN2018/101308	International filing date (<i>day/month/year</i>) 20 August 2018	(Earliest) Priority Date (<i>day/month/year</i>) 31 August 2017
Applicant Yangtze Memory Technologies Co., Ltd.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. Basis of the report

a. With regard to the **language**, the international search was carried out on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6bis(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 9A

☒ as suggested by the applicant.

☐ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2018/101308

A. CLASSIFICATION OF SUBJECT MATTER		
H01L 27/11529(2017.01)i; H01L 27/11551(2017.01)i		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
H01L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
CNPAT, WPI, EPODOC, CNKI, IEEE:step,conductive,layer,dielectric,etch-stop,barrier,insulating,nitride,opening		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013313627 A1 (LEE YAO-SHENG ET AL.) 28 November 2013 (2013-11-28) paragraphs[0024],[0029],[0039]-[0046]	1-20
A	US 9515086 B2 (YON GUKHYON ET AL.) 06 December 2016 (2016-12-06) the whole document	1-20
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "I" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search		Date of mailing of the international search report
06 November 2018		21 November 2018
Name and mailing address of the ISA/CN		Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA 6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088 China		LI,Wenhao
Facsimile No. (86-10)62019451		Telephone No. 86-(10)-53961341

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2018/101308

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2013313627	A1	28 November 2013	CN	104396004	B	30 January 2018
				WO	2013176960	A3	20 February 2014
				KR	20150079495	A	08 July 2015
US	9515086	B2	06 December 2016	KR	20160049159	A	09 May 2016

Form PCT/ISA/210 (patent family annex) (January 2015)

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To: 100013 China 10th Floor, Tower C, Beijing Global Trade Center, 36 North Third Ring Road East, Dongcheng District, Beijing NTD UNIVATION INTELLECTUAL PROPERTY AGENCY LTD.	PCT WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY (PCT Rule 43 <i>bis</i> .1)		
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%; padding: 2px;">Date of mailing (<i>day/month/year</i>)</td> <td style="width: 50%; text-align: center; padding: 2px;">21 November 2018</td> </tr> </table>		Date of mailing (<i>day/month/year</i>)	21 November 2018
Date of mailing (<i>day/month/year</i>)	21 November 2018		
Applicant's or agent's file reference P2018TC570	FOR FURTHER ACTION See paragraph 2 below		
International application No. PCT/CN2018/101308	International filing date (<i>day/month/year</i>) 20 August 2018		
Priority date (<i>day/month/year</i>) 31 August 2017			
International Patent Classification (IPC) or both national classification and IPC H01L 27/11529(2017.01)i; H01L 27/11551(2017.01)i			
Applicant Yangtze Memory Technologies Co., Ltd.			

1. This opinion contains indications relating to the following items: ☒ Box No. I Basis of the opinion ☐ Box No. II Priority ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability ☐ Box No. IV Lack of unity of invention ☒ Box No. V Reasoned statement under Rule 43<i>bis</i>.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement ☐ Box No. VI Certain documents cited ☐ Box No. VII Certain defects in the international application ☐ Box No. VIII Certain observations on the international application 2. FURTHER ACTION If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1<i>bis</i>(b) that written opinions of this International Searching Authority will not be so considered. If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later. For further options, see Form PCT/ISA/220.
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Name and mailing address of the ISA/ STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA China 6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088	Date of completion of this opinion 16 November 2018	Authorized officer LI, Wenhao
Facsimile No. (86—10) 62019451	Telephone No. 86-(10)-53961341	

Form PCT/ISA/237 (Cover sheet) (January 2015)

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/CN2018/101308

Box No. I	Basis of the opinion
1.	With regard to the language , this opinion has been established on the basis of: ☒ the international application in the language in which it was filed. ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).
2.	☐ This opinion has been established taking into account the rectification of an obvious mistake authorized by or notified to this Authority under Rule 91 (Rule 43 <i>bis</i> .1(a)).
3.	☐ With regard to any nucleotide and/or amino acid sequence disclosed in the international application, this opinion has been established on the basis of a sequence listing: a. ☐ forming part of the international application as filed: ☐ in the form of an Annex C/ST.25 text file. ☐ on paper or in the form of an image file. b. ☐ furnished together with the international application under PCT Rule 13<i>ter</i>.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file. c. ☐ furnished subsequent to the international filing date for the purposes of international search only: ☐ in the form of an Annex C/ST.25 text file (Rule 13<i>ter</i>.1(a)). ☐ on paper or in the form of an image file (Rule 13<i>ter</i>.1(b) and Administrative Instructions, Section 713).
4.	☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.
5.	Additional comments:

Form PCT/ISA/237 (Box No. I) (January 2015)

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/CN2018/101308

Box No. V	Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement																								
1. Statement	<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 35%; vertical-align: top;">Novelty (N)</td> <td style="width: 35%; vertical-align: top;">Claims</td> <td style="width: 20%; border-bottom: 1px solid black; text-align: center;">1-20</td> <td style="width: 10%; vertical-align: bottom; text-align: center;">YES</td> </tr> <tr> <td></td> <td style="vertical-align: top;">Claims</td> <td style="border-bottom: 1px solid black; text-align: center;">none</td> <td style="vertical-align: bottom; text-align: center;">NO</td> </tr> <tr> <td style="vertical-align: top;">Inventive step (IS)</td> <td style="vertical-align: top;">Claims</td> <td style="border-bottom: 1px solid black; text-align: center;">none</td> <td style="vertical-align: bottom; text-align: center;">YES</td> </tr> <tr> <td></td> <td style="vertical-align: top;">Claims</td> <td style="border-bottom: 1px solid black; text-align: center;">1-20</td> <td style="vertical-align: bottom; text-align: center;">NO</td> </tr> <tr> <td style="vertical-align: top;">Industrial applicability (IA)</td> <td style="vertical-align: top;">Claims</td> <td style="border-bottom: 1px solid black; text-align: center;">1-20</td> <td style="vertical-align: bottom; text-align: center;">YES</td> </tr> <tr> <td></td> <td style="vertical-align: top;">Claims</td> <td style="border-bottom: 1px solid black; text-align: center;">none</td> <td style="vertical-align: bottom; text-align: center;">NO</td> </tr> </table>	Novelty (N)	Claims	1-20	YES		Claims	none	NO	Inventive step (IS)	Claims	none	YES		Claims	1-20	NO	Industrial applicability (IA)	Claims	1-20	YES		Claims	none	NO
Novelty (N)	Claims	1-20	YES																						
	Claims	none	NO																						
Inventive step (IS)	Claims	none	YES																						
	Claims	1-20	NO																						
Industrial applicability (IA)	Claims	1-20	YES																						
	Claims	none	NO																						
2. Citations and explanations :	[1] D1: US2013/0313627 A1,(28.11.2013) [2] I. Novelty and Inventive Step [3] D1 discloses a method of making multi-level contact used in multilevel NAND device and a structure of the multilevel NAND device (see paragraphs[0024],[0029],[0039]-[0046]), the control gate steps 120(corresponding to a staircase structure comprising a plurality of steps, wherein each step comprises a conductive layer disposed over a dielectric layer) are covered with a stack of dielectric materials including: an etch stop layer 122(corresponding to an etch-stop layer disposed on the conductive layer of the each step), the second dielectric layer 124, the sacrificial barrier layer126, and the fourth dielectric layer 128 described above(corresponding to an insulating layer disposed on the etch-stop layer). The etch stop layer 122, and the sacrificial barrier layer 126 are made of a nitride, such as silicon nitride(corresponding to the etch-stop layer comprises one or more of silicon nitride). Etched with an etchant that etches the material of the second dielectric layer 124 faster than the material of the etch stop layer 122(corresponding to performing an etching process on the insulating layer, wherein an etching rate of the insulating layer is higher than an etching rate of the etch-stop layer).Openings 130A-130E are etched from the top surface 128a of the fourth dielectric layer 128 through the fourth dielectric layer 128, the contacts 132A-132E may be formed by depositing an electrically conducting material into the openings130A-130E(corresponding to a plurality of conductive structures formed in the insulating layer, wherein each conductive structure is formed on the conductive layer of the each step).From Fig1-Fig2, there must be an opening filled with contact which got through every layer, until the substrate 100(corresponding to the plurality of conductive structures extending through the etch-stop layer, the each conductive structure directly contacting a corresponding one of the conductive layer of the each step). [4] The difference between claims 1, 11 and D1 is: a barrier layer disposed between the conductive layer and the etch-stop layer. The technical problem to be solved is considered to be: how to protect conductive layer. But setting a dielectric layer to protect another layer is common knowledge in the art. The difference between claim 16 and D1 is: disposing a sacrificial layer over a dielectric layer and replacing the sacrificial layer of each step with a conductive layer. The technical problem to be solved is considered to be: how to forming the CG. But replacing the sacrificial layer of each step with a conductive layer is common knowledge in the art. [6] The additional features of claims 3,5-6,8 and 14,17,19 are disclosed by D1. [7] The additional features of claims 2,4,7,9-10 and 12-13,15,18,20 are common knowledge in the art. [9] Therefore claims 1-20 meet the criteria set out in PCT Article 33(2) but do not meet the criteria set out in PCT Article 33(3). [10] II. Industrial Applicability [11] The technical solution of claims 1-20 can be used in industry, and thus these claims are industrially applicable under PCT Article 33(4).																								

Form PCT/ISA/237 (Box No. V) (January 2015)

Electronic Acknowledgement Receipt	
EFS ID:	36426120
Application Number:	16126947
International Application Number:	
Confirmation Number:	1077
Title of Invention:	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF
First Named Inventor/Applicant Name:	Jifeng ZHU
Customer Number:	26111
Filer:	Donald J. Featherstone/Jon Baitlon
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0480002
Receipt Date:	27-JUN-2019
Filing Date:	10-SEP-2018
Time Stamp:	12:12:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	4123-0480002IDSCoverLetter.pdf	236242 255099c8f956d82ecd845cb89634c5da014f ce97	no	1
Warnings:					

Information:					
2	Transmittal Letter	4123-0480002IDSpleading.pdf	116823	no	6
			faebad68b478643eba394f6e620710fff18a6556		
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	4123-0480002-FormSB08a.pdf	141556	no	1
			ce6af59f4728158e12a214d8a50d1af08d4c3702		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
4	Information Disclosure Statement (IDS) Form (SB08)	4123-0480002-FormSB08b.pdf	183122	no	1
			ce0fe0df57bb77559de6cdb968ca650247ee1824		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
5	Foreign Reference	FP1_CN104396004A.pdf	4627605	no	23
			478c12a00efb8415b9eacb9b4ea49dbb3211c082		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
6	Non Patent Literature	NPL1_ISRWO.pdf	266652	no	6
			36ebeb64d0b2424bdd1a7e6d8ce28b4ac83f73b6		
Warnings:					
Information:					
Total Files Size (in bytes):			5572000		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

June 27, 2019

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 1077
Art Unit 2811
Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Application No. 16/126,947; Filing Date: September 10, 2018
For: **WORD LINE CONTACT STRUCTURE FOR THREE-
DIMENSIONAL MEMORY DEVICES AND FABRICATION
METHODS THEREOF**
Inventors: ZHU *et al.*
Our Ref: 4123.0480002

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Information Disclosure Statement;
2. Form PTO/SB/08a (1 sheet) listing 5 documents (**US1-US4** and **FP1**);
3. Form PTO/SB/08b (1 sheet) listing 1 document (**NPL1**); and
4. Copies of cited documents (**FP1** and **NPL1**).

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/MY/jcb
Enclosures

13288637_1.docx

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: ZHU *et al.*

Applicant: Yangtze Memory Technologies
Co., Ltd.

Application No.: 16/126,947

Filing Date: September 10, 2018

Confirmation No.: 1077

Art Unit: 2811

Examiner: GURLEY, LYNNE ANN

Atty. Docket: 4123.0480002

Title: **WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY
DEVICES AND FABRICATION METHODS THEREOF**

Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

Listed on accompanying IDS Forms PTO/SB/08a equivalent and PTO/SB/08b equivalent are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicant has checked the appropriate boxes below.

- ☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement: (i) was first cited in any communication from a patent office in a counterpart¹ foreign or international application or from the Office; and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of this information disclosure statement; OR (ii) is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of the information disclosure statement.
- ☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action

¹ The term counterpart foreign patent application means that a claim for priority has been made in either the U.S. application or a foreign application based on the other, or that the disclosures of the U.S. and foreign patent applications are substantively identical (e.g., an application filed in the European Patent Office claiming the same U.K. priority as claimed in the U.S. application).

after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

- ☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.
- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- ☐ c. The required fee is provided through online credit card payment authorization in the amount of \$240.00 in payment of the fee under 37 C.F.R. § 1.17(p).
- ☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or

Atty. Dkt. No. 4123.0480002

Notice of Allowance, but on or before payment of the Issue Fee. The required fee is provided through online credit card payment authorization in the amount of \$240.00 in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- ☒ 5. The patent family for one or more foreign language documents submitted herewith includes a United States patent, and other patent, in the English language. Copies of both the particular foreign patent(s) or published foreign patent applications cited in the foreign patent office communication, and that are not already of record in this application, are enclosed. Copies of the related United States or other English language patent or published application from the family list, if not already of record, are listed on the accompanying SB/08A form. For the purposes of a statement under 37 CFR 1.97(e)(1), the United States or

Atty. Dkt. No. 4123.0480002

other English language patent or published application are to be construed as being cited by the foreign patent office. MPEP 609.04(b)(V).

- ☐ 6. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. MPEP 609.04(a)(III).

- ☒ 7. A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3).

Document **US3** (8,828,884 B2) is submitted herewith as the English-language counterpart of document **FP1** (CN 104396004 A).

- ☒ 8. Copies of documents **FP1** and **NPL1** are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of the U.S. patents and patent application publications cited as documents **US1-US4** on the attached IDS Form are submitted.

- ☐ 9. Copies of the _____ documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. _____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

- ☐ 10. It is expected that the examiner will review the prosecution and cited art in the parent Application No(s). _____ in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

Atty. Dkt. No. 4123.0480002

- ☐ 11. In accordance with the Federal Circuit decision in *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003), Applicants submit herewith Office Actions from the co-pending U.S. Patent Application No. _____, filed _____, as documents _____ to _____. The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: June 27, 2019

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

Atty. Dkt. No. 4123.0480002

[illegible][illegible]

Examiner Signature		Date Considered	
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Micron Ex. 1002, p. 126
Micron v. YMTC
IPR2025-00117

Electronic Acknowledgement Receipt	
EFS ID:	36503025
Application Number:	16126947
International Application Number:	
Confirmation Number:	1077
Title of Invention:	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF
First Named Inventor/Applicant Name:	Jifeng ZHU
Customer Number:	26111
Filer:	Donald J. Featherstone/Nina Angileri
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0480002
Receipt Date:	05-JUL-2019
Filing Date:	10-SEP-2018
Time Stamp:	09:57:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	Cover_Letter.pdf	20674	no	1
			84213e11657e24c135f68266b5f291c832f88920		
Warnings:					

Information:					
2	Transmittal Letter	Pleading.pdf	28405	no	6
			7cd969568b5f0600611246ccfb2a4855b470026		
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	SB08a.pdf	14495	no	1
			00c7a9abe59a16ce14a33324320af9d4063cf4ee		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
Total Files Size (in bytes):			63574		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

July 5, 2019

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 1077
Art Unit 2811
Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Application No. 16/126,947; Filing Date: September 10, 2018
For: **WORD LINE CONTACT STRUCTURE FOR THREE-
DIMENSIONAL MEMORY DEVICES AND FABRICATION
METHODS THEREOF**
Inventors: ZHU *et al.*
Our Ref: 4123.0480002

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. First Supplemental Information Disclosure Statement; and
2. Form PTO/SB/08a (1 sheet) listing 4 documents (**US1-US4**).

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/M-Y/naa
Enclosures

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Sterne, Kessler, Goldstein & Fox P.L.L.C. | 1100 New York Avenue, NW | Washington, D.C. 20005
P 202.371.2800 | F 202.371.2540 | sternekessler.com

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: ZHU *et al.*

Confirmation No.: 1077

Applicant: Yangtze Memory Technologies
Co., Ltd.

Art Unit: 2811

Application No.: 16/126,947

Examiner: GURLEY, LYNNE ANN

Filing Date: September 10, 2018

Atty. Docket: 4123.0480002

Title: **WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY
DEVICES AND FABRICATION METHODS THEREOF**

First Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

Listed on accompanying IDS Form PTO/SB/08a equivalent are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Form based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicant has checked the appropriate boxes below.

- ☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement: (i) was first cited in any communication from a patent office in a counterpart¹ foreign or international application or from the Office; and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of this information disclosure statement; OR (ii) is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of the information disclosure statement.
- ☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.
- ☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office

¹ The term counterpart foreign patent application means that a claim for priority has been made in either the U.S. application or a foreign application based on the other, or that the disclosures of the U.S. and foreign patent applications are substantively identical (e.g., an application filed in the European Patent Office claiming the same U.K. priority as claimed in the U.S. application).

Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.
37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement.
37 C.F.R. § 1.97(e)(2).
- ☐ c. The required fee is provided through online credit card payment authorization in the amount of \$0.00 in payment of the fee under 37 C.F.R. § 1.17(p).
- ☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but on or before payment of the Issue Fee. The required fee is provided through online credit card payment authorization in the amount of \$0.00 in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

Atty. Dkt. No. 4123.0480002

- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- ☐ 5. The patent family for one or more foreign language documents submitted herewith includes a United States patent, and other patent, in the English language. Copies of both the particular foreign patent(s) or published foreign patent applications cited in the foreign patent office communication, and that are not already of record in this application, are enclosed. Copies of the related United States or other English language patent or published application from the family list, if not already of record, are listed on the accompanying SB/08A form. For the purposes of a statement under 37 CFR 1.97(e)(1), the United States or other English language patent or published application are to be construed as being cited by the foreign patent office. MPEP 609.04(b)(V).

Atty. Dkt. No. 4123.0480002

- ☐ 6. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. MPEP 609.04(a)(III).
- ☐ 7. A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3).
- ☒ 8. In accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of the U.S. patent application publications cited as documents **US1-US4** on the attached IDS Form are submitted.
- ☐ 9. Copies of the _____ documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. _____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).
- ☐ 10. It is expected that the examiner will review the prosecution and cited art in the parent Application No(s). _____ in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.
- ☐ 11. In accordance with the Federal Circuit decision in *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003), Applicants submit herewith Office Actions from the co-pending U.S. Patent Application No. _____, filed _____, as documents _____ to _____. The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the

Atty. Dkt. No. 4123.0480002

present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Form, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: July 5, 2019

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

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Atty. Dkt. No. 4123.0480002

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0480002
		Application Number	<u>16/126,947</u>
Title of Invention	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201710774754.6	CN	2017-08-31	<u>38C7</u>

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet must be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, all joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of all joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Donald J. Featherstone/			Date (YYYY-MM-DD)	2019-08-07
First Name	Donald	Last Name	Featherstone	Registration Number	33,876

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Electronic Acknowledgement Receipt	
EFS ID:	36806994
Application Number:	16126947
International Application Number:	
Confirmation Number:	1077
Title of Invention:	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF
First Named Inventor/Applicant Name:	Jifeng ZHU
Customer Number:	26111
Filer:	Donald J. Featherstone/Kim Perry
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0480002
Receipt Date:	07-AUG-2019
Filing Date:	10-SEP-2018
Time Stamp:	18:01:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	2019-08-07-Corrected-ADS-4123-0480002.pdf	105831	no	1
			b7dbfe456d22b59372d7b165d8e32ef3669a16f7		
Warnings:					

Information:	
This is not an USPTO supplied ADS fillable form	
Total Files Size (in bytes):	105831
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/126,947	09/10/2018	Jifeng ZHU	4123.0480002	1077
26111	7590	09/17/2019	EXAMINER	
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.			GEYER, SCOTT B	
1100 NEW YORK AVENUE, N.W.			ART UNIT	
WASHINGTON, DC 20005			PAPER NUMBER	
			2812	
			NOTIFICATION DATE	
			DELIVERY MODE	
			09/17/2019	
			ELECTRONIC	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

e-office@sternekessler.com

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-15, drawn to a device, classified in H01L 27/105+.
- II. Claims 16-20, drawn to a method, classified in H01L 21/768+.

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process, since the product requires a barrier layer whereas the process claims do not.

Restriction for examination purposes as indicated is proper because all the inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because one or more of the following reasons apply: the inventions require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search strategies or search queries).

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement

may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention.**

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other invention.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer (telephone: 571-272-1958). The examiner can normally be reached on Monday to Friday, 10AM - 4PM. Examiner interviews are available via telephone, in-person, and video conferencing using a

USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at:

<http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles D Garber (telephone: 571-272-2194). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (in U.S.A. or Canada) or 571-272-1000.

/SCOTT B GEYER/
Primary Examiner, Art Unit 2812

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: ZHU <i>et al.</i>	Confirmation No.: 1077
Applicant: Yangtze Memory Technologies Co., Ltd.	Art Unit: 2812
Application No.: 16/126,947	Examiner: GEYER, SCOTT B
Filing Date: September 10, 2018	Atty. Docket: 4123.0480002
Title: WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF	

Reply to Restriction Requirement

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In reply to the office action dated September 17, 2019, requesting an election of one group of claims to prosecute in the above-referenced patent application, Applicant hereby elects to prosecute **Group I**, represented by **claims 1-15, drawn to a device, classified in H01 L27/105+**. This election is made without prejudice to or disclaimer of the other claims or embodiments disclosed. This election is made without traverse.

Reconsideration and withdrawal of the Restriction Requirement, and consideration and allowance of all pending claims, are respectfully requested.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time

are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: September 24, 2019

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

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Atty. Dkt. No. 4123.0480002

Electronic Acknowledgement Receipt	
EFS ID:	37251040
Application Number:	16126947
International Application Number:	
Confirmation Number:	1077
Title of Invention:	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF
First Named Inventor/Applicant Name:	Jifeng ZHU
Customer Number:	26111
Filer:	Donald J. Featherstone/David Ofori Amanfo
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0480002
Receipt Date:	24-SEP-2019
Filing Date:	10-SEP-2018
Time Stamp:	17:02:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2019-09-24-Miscellaneous-Letter-4123-0480002.pdf	218817	no	1
			826e77b4a468c0bc1faeccc0efce82eefb38d21f		
Warnings:					

Information:					
2	Response to Election / Restriction Filed	2019-09-24-Reply-Restriction-Requirement-4123-0480002.pdf	85041	no	2
			102a8f6321e23e26a0bfd0b7b2d6057a887a5d13		
Warnings:					
Information:					
Total Files Size (in bytes):			303858		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

September 24, 2019

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 1077
Art Unit 2812

Re: U.S. Utility Patent Application
Appl. No. 16/126,947; Filing Date: September 10, 2018
For: WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL
MEMORY DEVICES AND FABRICATION METHODS THEREOF
Inventors: ZHU *et al.*
Our Ref: 4123.0480002

Commissioner:

Transmitted herewith for appropriate action is a document entitled ***Reply to Restriction Requirement***, which is submitted electronically.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) or credit any overpayment to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/M-Y/d-o
Enclosure

13871459_1.docx



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/126,947	09/10/2018	Jifeng ZHU	4123.0480002	1077
26111	7590	10/24/2019		
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C. 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			EXAMINER GEYER, SCOTT B	
			ART UNIT	PAPER NUMBER
			2812	
			NOTIFICATION DATE	DELIVERY MODE
			10/24/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

e-office@sternekessler.com

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I (claims 1-15) in the reply filed on September 24, 2019 is acknowledged.

Priority

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in China on August 31, 2017. It is noted, however, that applicant has not filed a certified copy of the foreign priority application as required by 37 CFR 1.55.

Information Disclosure Statement

The references cited within the IDS documents submitted on June 27, 2019 (two separate documents) and July 5, 2019 have been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

Claims 1-6, 9, and 11-14 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Oh (US 2016/0358855 A1).

As to **claim 1**, Oh teaches a semiconductor structure in figure 2A. The structure of Oh has:

a staircase structure comprising a plurality of steps, wherein each step comprises a conductive layer (20) disposed over a dielectric layer (12);

a barrier layer (14) disposed over a portion of the conductive layer of the each step;

an etch-stop layer (15) disposed on the barrier layer;

an insulating layer (16) disposed on the etch-stop layer; and

a plurality of conductive structures (23) formed in the insulating layer, wherein each conductive structure is formed on the conductive layer of the each step.

As to **claims 2 and 3**, Oh teaches the plurality of conductive structures extend through the barrier layer and the etch-stop layer (see figure 2A).

As to **claim 4**, Oh teaches the barrier layer (14) comprises silicon oxide (see paragraph 0024).

As to **claim 5**, Oh teaches the etch-stop layer (15) comprises silicon nitride (see paragraph 0025).

As to **claim 6**, Oh teaches each conductive structure (23) directly contacts a corresponding one of the conductive layer of the each step (see figure 2A).

As to **claim 9**, Oh teaches the barrier layer (14) is formed on side and top surfaces of the plurality of steps (see figure 2A).

As to **claim 11**, Oh teaches a semiconductor structure in figure 2A. The structure of Oh has:

- a staircase structure comprising a plurality of steps, wherein each step comprises a conductive layer (20) disposed over a dielectric layer (12);

- an etch-stop layer (15) disposed over a portion of the conductive layer (20) of the each step;

- an insulating layer (16) disposed on the etch-stop layer; and

- a plurality of conductive structures (23) formed in the insulating layer and extending through the etch-stop layer, wherein each conductive structure directly contacts the corresponding conductive layer of each step.

As to **claim 12**, Oh teaches the etch-stop layer is formed on a side surface and a top surface of each step (see figure 2A).

As to **claim 13**, Oh teaches thicknesses of the etch-stop layer is the same on the side and top surfaces of each step (see figure 2A).

As to **claim 14**, Oh teaches the etch-stop layer (15) comprises silicon nitride (see paragraph 0025).

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Claims 1-9 and 11-14 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Matsuda (US 2016/0020169 A1).

As to **claim 1**, Matsuda teaches a semiconductor structure in figure 2B. The structure of Matsuda has:

- a staircase structure comprising a plurality of steps, wherein each step comprises a conductive layer (16, e.g. 161) disposed over a dielectric layer (20, e.g. 200);

- a barrier layer (40) disposed over a portion of the conductive layer of the each step (see also figure 4B);

- an etch-stop layer (42) disposed on the barrier layer (see also figure 4B);

- an insulating layer (44) disposed on the etch-stop layer (see also figure 5B); and

- a plurality of conductive structures (68, e.g. 681) formed in the insulating layer, wherein each conductive structure is formed on the conductive layer of the each step.

As to **claims 2 and 3**, Matsuda teaches the plurality of conductive structures extend through the barrier layer and the etch-stop layer (see figure 2B).

As to **claim 4**, Matsuda teaches the barrier layer (40) comprises silicon oxide (see paragraph 0054).

As to **claim 5**, Matsuda teaches the etch-stop layer (42) comprises silicon nitride (see paragraph 0054).

As to **claim 6**, Matsuda teaches each conductive structure (68) directly contacts a corresponding one of the conductive layer of the each step (see figure 2B).

As to **claim 7**, Matsuda teaches top surfaces of the plurality of conductive structures (68), the insulating layer (44), and a portion of the etch-stop layer (42) are coplanar (see figure 2B).

As to **claim 8**, Matsuda teaches the plurality of conductive structures (68) comprise tungsten (see paragraph 0070).

As to **claim 9**, Matsuda teaches the barrier layer (40) is formed on side and top surfaces of the plurality of steps (see figure 2B).

As to **claim 11**, Matsuda teaches a semiconductor structure in figure 2B. The structure of Matsuda has:

- a staircase structure comprising a plurality of steps, wherein each step comprises a conductive layer (16, e.g. 161) disposed over a dielectric layer (20, e.g. 200);

- an etch-stop layer (42) disposed over a portion of the conductive layer of the each step;

- an insulating layer (44) disposed on the etch-stop layer; and

- a plurality of conductive structures (68, e.g. 681) formed in the insulating layer and extending through the etch-stop layer, wherein each conductive structure directly contacts the corresponding conductive layer of each step.

As to **claim 12**, Matsuda teaches the etch-stop layer is formed on a side surface and a top surface of each step (see figure 2B).

As to **claim 13**, Matsuda teaches thicknesses of the etch-stop layer is the same on the side and top surfaces of each step (see figure 2B).

As to **claim 14**, Matsuda teaches the etch-stop layer (42) comprises silicon nitride (see paragraph 0054).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 10 and 15 rejected under 35 U.S.C. 103 as being unpatentable over Matsuda as applied to claims 1 and 11 above (respectively), and further in view of Examiner's Official Notice.

As to **claims 10 and 15**, Matsuda teaches an etch-stop layer comprising silicon nitride and deposited by CVD (see paragraph 0054). Matsuda does not specifically teach the thickness of the etch-stop layer being in a range between 10nm to 1000nm.

However, the examiner takes official notice that a silicon nitride etch-stop layer having a thickness in the range of 10-1000 nm is notoriously well known in the art of semiconductor technology. Furthermore, the range recited in claims 10 and 15 lacks criticality, as evidenced by the range being two orders of magnitude, and as also supported by applicant's own lengthy disclosure within paragraph (0056).

Therefore, it would have been obvious to a person of ordinary skill in the art, before the filing date of the invention, to modify the structure of Matsuda with an etch-stop layer having a thickness concordant with practices recognized and notoriously well known in the art of semiconductor manufacturing.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer (telephone: 571-272-1958). The examiner can normally be reached on Monday to Friday, 10AM - 4PM. Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at: <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles D Garber (telephone: 571-272-2194). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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/SCOTT B GEYER/
Primary Examiner, Art Unit 2812

Notice of References Cited	Application/Control No. 16/126,947		Applicant(s)/Patent Under Reexamination ZHU et al.	
	Examiner Scott B Geyer		Art Unit 2812	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20160358855-A1	12-2016	OH; Kwang-Seok	H01L23/5226	1/1
*	B	US-9419013-B1	08-2016	Lee; Dong Sik	H01L27/11582	1/1
*	C	US-20110031546-A1	02-2011	UENAKA; Tsuneo	H01L27/11573	257/316
*	D	US-20110169071-A1	07-2011	Uenaka; Tsuneo	H01L27/105	257/326
*	E	US-20100207195-A1	08-2010	Fukuzumi; Yoshiaki	G11C16/0483	257/326
*	F	US-20160020169-A1	01-2016	MATSUDA; Yuya	H01L23/528	257/758
*	G	US-7539056-B2	05-2009	Katsumata; Ryota	G11C16/0483	365/185.18
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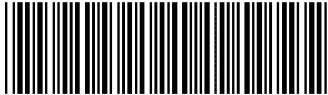
FOREIGN PATENT DOCUMENTS

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	N					
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	P					
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NON-PATENT DOCUMENTS

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<i>Search Notes</i> 	Application/Control No. 16/126,947	Applicant(s)/Patent Under Reexamination ZHU et al.
	Examiner Scott B Geyer	Art Unit 2812

CPC - Searched*		
Symbol	Date	Examiner
H01L27/115-11597	10/18/2019	SBG

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST search notes attached	10/18/2019	SBG

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

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Receipt date: 06/27/2019

PTO/SB/08b (07-09)
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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known	
		Application Number	16/126,947
		Filing Date	September 10, 2018
		First Named Inventor	Zhu et al.
		Art Unit	~~2814~~ 2812
		Examiner Name	~~GURLEY, LYNNE ANN~~
Sheet 1	of 1	Attorney Docket Number	4123.0480002

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/SG/	NPL1	International Search Report and Written Opinion of the International Searching Authority directed to related International Patent Application No. PCT/CN2018/101308, mailed November 21, 2018; 6 pages.	

Examiner Signature	/SCOTT B GEYER/	Date Considered	10/16/2019
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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.
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FIRST SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Application Number	16/126,947
				Filing Date	September 10, 2018
				First Named Inventor	Jifeng ZHU
				Art Unit	~~2811~~ 2812
				Examiner Name	~~GURLEY, LYNNE ANN~~
Sheet	1	of	1	Attorney Docket Number	4123.0480002

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Micron Ex. 1002, p. 162
Micron v. YMTC
IPR2025-00117

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	1122	(H01L27/115-11597).CPC. and (staircase stair-case (stair adj case))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/18 12:16
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CONFIRMATION NO. 1077

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
16/126,947	09/10/2018	257	2812	4123.0480002		
RULE						
APPLICANTS Yangtze Technologies Co., Ltd., Wuhan, CHINA INVENTORS Jifeng ZHU, Wuhan, CHINA; Zhenyu LU, Wuhan, CHINA; Jun CHEN, Wuhan, CHINA; Si Ping HU, Wuhan, CHINA; Xiaowang DAI, Wuhan, CHINA; Lan YAO, Wuhan, CHINA; Li Hong XIAO, Wuhan, CHINA; A Man ZHENG, Wuhan, CHINA; Kun BAO, Wuhan, CHINA; Haohao YANG, Wuhan, CHINA; /SBG/						
** CONTINUING DATA ***** This application is a CON of PCT/CN2018/101308 08/20/2018 ** FOREIGN APPLICATIONS ***** CHINA 201710774754.6 08/31/2017 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 10/11/2018						
Foreign Priority claimed ☒ Yes ☐ No	35 USC 119(a-d) conditions met ☐ Yes ☒ No	☐ Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
Verified and Acknowledged	/SCOTT B GEYER/ Examiner's Signature	Initials	CHINA	13	20	3
ADDRESS STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C. 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005 UNITED STATES						
TITLE WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF						
FILING FEE RECEIVED 1880	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

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				Application Number	16/126,947
				Filing Date	September 10, 2018
				First Named Inventor	Zhu et al.
				Art Unit	2811
				Examiner Name	GURLEY, LYNNE ANN
				Attorney Docket Number	4123.0480002
Sheet	1	of	2		

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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
/SG/	FP1	CN-104396004-A	03-04-2015	SANDISK TECHNOLOGIES INC.		
	FP2					
	FP3					
	FP4					
	FP5					
	FP6					

Examiner Signature	/SCOTT B GEYER/	Date Considered	10/16/2019
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(21) 申请号 201410404550. X

(22) 申请日 2014. 08. 15

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事务所(普通合伙) 11345
代理人 陈红

(51) Int. Cl.

H01L 27/115(2006. 01)

H01L 21/8247(2006. 01)

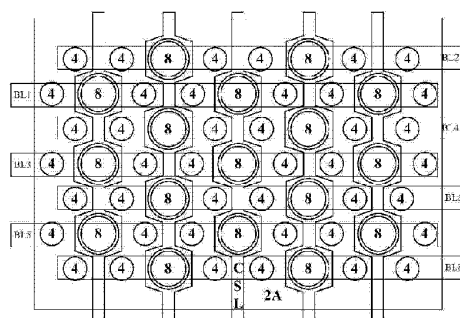
权利要求书2页 说明书7页 附图6页

(54) 发明名称

二维存储器及其制造方法

(57) 摘要

一种三维存储器制造方法,包括步骤:在衬底上形成第一材料层与第二材料层的堆叠结构;刻蚀堆叠结构露出衬底,形成垂直的多个第一开孔;在每个第一开孔中形成填充层;在每个第一开孔周围,刻蚀堆叠结构露出衬底,形成垂直的多个第二开孔;在每个第二开孔中形成垂直的沟道层和漏极;选择性刻蚀去除填充层,重新露出第一开孔;侧向刻蚀部分或者完全去除第二材料层,留下凹槽;在凹槽中形成栅极堆叠结构;在每个第一开孔底部的衬底上和/或中形成共源极。依照本发明的三维存储器制造方法,将 TCAT 三维器件的字线深槽替换为深孔刻蚀来完成相同的功能,提高集成密度,简化堆叠结构的刻蚀工艺,保留了金属栅控制性能。



1. 一种三维存储器制造方法,包括步骤:
在衬底上形成第一材料层与第二材料层的堆叠结构;
刻蚀堆叠结构露出衬底,形成垂直的多个第一开孔;
在每个第一开孔中形成填充层;
在每个第一开孔周围,刻蚀堆叠结构露出衬底,形成垂直的多个第二开孔;
在每个第二开孔中形成垂直的沟道层和漏极;
选择性刻蚀去除填充层,重新露出第一开孔;
侧向刻蚀部分或者完全去除第二材料层,留下凹槽;
在凹槽中形成栅极堆叠结构;
在每个第一开孔底部的衬底上和/或中形成共源极。
2. 如权利要求1所述的三维存储器制造方法,其中,第一材料层、第二材料层、填充层三者之间具有各自不同的刻蚀选择性。
3. 如权利要求2所述的三维存储器制造方法,其中,第一材料层、第二材料层、填充层材料选自氧化硅、氮化硅、氮氧化硅、非晶硅、非晶锗、DLC、非晶碳的任意一种及其组合。
4. 如权利要求1所述的三维存储器制造方法,其中,第一开孔的尺寸大于或等于第二开孔的尺寸。
5. 如权利要求1所述的三维存储器制造方法,其中,沟道层为中心包括绝缘体的中空结构。
6. 如权利要求1所述的三维存储器制造方法,其中,形成共源极之后进一步包括,在每个第一开孔侧壁形成绝缘层,在绝缘层侧壁以及每个第一开孔底部形成接触共源区的接触层。
7. 如权利要求6所述的三维存储器制造方法,其中,形成接触层之时或者之后进一步包括,控制沉积工艺参数或者回刻使得接触层的顶面低于栅极堆叠结构最顶层的底面,并且采用绝缘层回填。
8. 如权利要求6所述的三维存储器制造方法,其中,形成接触层之后进一步包括,刻蚀去除部分第一材料层、栅极堆叠结构形成第三开孔,在第三开孔中沉积绝缘材料形成与栅极堆叠结构最顶层之间的隔离绝缘区。
9. 如权利要求8所述的三维存储器制造方法,其中,形成隔离绝缘区之后进一步包括,在器件上形成层间介质层,刻蚀层间介质层形成第四开孔直至露出接触层,填充金属形成共源线引线。
10. 如权利要求9所述的三维存储器制造方法,其中,形成共源线接触塞之后进一步包括,在器件上形成第二层间介质层,刻蚀第二层间介质层形成第五开孔直至暴露沟道区,填充金属形成位线接触。
11. 如权利要求1所述的三维存储器制造方法,其中,刻蚀形成第一开孔之前进一步包括,在阵列区域周围的字线接触区域刻蚀堆叠结构形成台阶,依次暴露每个第一材料层和第二材料层的端部。
12. 一种三维存储器制造方法,包括步骤:
在衬底上形成第一材料层与第二材料层的堆叠结构;
刻蚀堆叠结构露出衬底,同时形成垂直的多个第一开孔以及在每个第一开孔周围的多

个第二开孔；

在每个第一开孔中形成填充层；

在每个第二开孔中形成垂直的沟道层和漏极；

选择性刻蚀去除填充层，重新露出第一开孔；

侧向刻蚀部分或者完全去除第二材料层，留下凹槽；

在凹槽中形成栅极堆叠结构；

在每个第一开孔底部的衬底上和 / 或中形成共源极。

13. 一种三维存储器，包括：

在衬底上垂直分布的多个共源极引线，与衬底中和 / 或上的共源极接触；

在每个共源极引线周围垂直于衬底分布的多个沟道层，每个沟道层顶部具有漏极；

在每个沟道层侧壁上的多个绝缘隔离层以及在每个绝缘隔离层之间的多个栅极堆叠结构。

三维存储器及其制造方法

技术领域

[0001] 本发明涉及一种半导体器件及其制造方法,特别是涉及一种高密度三维存储器及其制造方法。

背景技术

[0002] 为了改善存储器件的密度,业界已经广泛致力于研发减小二维布置的存储器单元的尺寸的方法。随着二维(2D)存储器件的存储器单元尺寸持续缩减,信号冲突和干扰会显著增大,以至于难以执行多电平单元(MLC)操作。为了克服2D存储器件的限制,业界已经研发了具有三维(3D)结构的存储器件,通过将存储器单元三维地布置在衬底之上来提高集成密度。

[0003] 业界目前一种常用的3D存储器件结构是太比特单元阵列晶体管(TCAT)。具体地,可以首先在衬底上沉积多层叠层结构(例如氧化物和氮化物交替的多个ONO结构);通过各向异性的刻蚀工艺对衬底上多层叠层结构刻蚀而形成沿着存储器单元字线(WL)延伸方向分布、垂直于衬底表面的多个沟道通孔(可直达衬底表面或者具有一定过刻蚀);在沟道通孔中沉积多晶硅等材料形成柱状沟道;沿着WL方向刻蚀多层叠层结构形成直达衬底的沟槽,露出包围在柱状沟道周围的多层叠层;针对叠层中相邻层之间的刻蚀选择性,选择刻蚀选择比较高的腐蚀液湿法去除叠层中的第二类型材料,在柱状沟道周围留下横向分布的第一类型材料构成的突起结构;在沟槽中突起结构的侧壁沉积高k介质材料的栅极介质层以及金属材质的栅极导电层构成的栅极堆叠;刻蚀叠层结构形成源漏接触并完成后端制造工艺。此时,叠层结构在柱状沟道侧壁留下的一部分突起形成了栅电极之间的隔离层,而留下的栅极堆叠夹设在多个隔离层之间作为控制电极。当向栅极施加电压时,栅极的边缘电场会使得例如多晶硅材料的柱状沟道侧壁上感应形成源漏区,由此构成多个串并联的闪存单元构成的门阵列而记录所存储的逻辑状态。其中,为了将单元区多个串并联MOSFET信号引出,在柱状沟道顶部沉积填充多晶硅材料形成漏区,并形成与漏区电连接的金属接触塞以进一步电连接至上方的位线(bit-line, BL)。此外,在多个垂直柱状沟道之间衬底中形成带有金属硅化物接触的共用源区。在单元导通状态下,电流从共用源区流向周围的垂直沟道区,并在控制栅极(与字线WL相连)施加的控制电压作用下向上穿过垂直沟道中感应生成的多个源漏区,通过沟道顶部的漏区而进一步流向上方的位线。

[0004] 该TCAT器件结构具有体擦除(改变控制栅极可以引起感应源漏区以及浮栅极中电势变化,能整体擦除)、金属栅极(能较方便通过控制金属材料控制功函数从而调节晶体管阈值)等诸多优点。但是另一方面,由于除了顶部的选择晶体管(USG,位于存储晶体管单元串上方)之外,其余栅极与字线(WL)连接都是通过刻蚀孔进行共享链接,并且采用后栅工艺刻蚀去除伪栅极形成栅极开口并沉积金属栅极,这种极高深宽比(AR例如通常大于40:1乃至100:1)的深接触孔以及栅极开口将由于沉积多层薄膜而使得宽度增大,进而使得TCAT的存储单元密度无法有效进一步减小。同时,深槽的刻蚀和深孔沟道的刻蚀都是对多层堆栈的刻蚀,工艺复杂度很高,深孔和深槽的形状差异使得刻蚀的工艺也要有所变化。

[0005] 与 TCAT 技术对应的,另一种常用的器件结构例如是采用位成本可缩减 (BiCS) 的 NAND 结构,通过将存储器单元三维地布置在衬底之上来提高集成密度、其中沟道层垂直竖立在衬底上,栅极分为下层的选择栅极、中层的控制栅极以及上层的选择栅极三部分,通过将栅极信号分布在三组栅电极中以减小信号之间的串扰。具体地,上层和下层的器件用作选择晶体管——栅极高度/厚度较大的垂直 MOSFET,栅极介质层为常规的单层高 k 材料;中层的器件用作存储单元串,栅极高度/厚度较小,栅极介质层为隧穿层、存储层、阻挡层的堆叠结构。基于 BiCS 的 NAND 结构器件的具体制造工艺一般包括,在硅衬底上沉积下层选择栅电极层,刻蚀下层选择栅电极层形成直达衬底的孔槽以沉积沟道层的下部分以及下层栅电极的引出接触,在上方沉积控制栅极层,刻蚀控制栅极层形成作为存储器单元区域的中间沟道区以及中层控制栅电极的引出接触,刻蚀形成控制栅极,按照字线、位线划分需要将整个器件分割为多个区域,在之上沉积上层选择栅极并刻蚀、沉积形成上部沟道以及上层引出接触,之后采用后续工艺完成器件的制造。在 BiCS 结构中,除了最上方的选择晶体管 USG 之外,下方的所有栅电极都可以是平板状,相对于 TCAT 而言可以避免深沟槽、深孔接触工艺,有利于提高存储器密度。在这种工艺过程中,最为关键的刻蚀步骤仅在于对于中间层存储器沟道区和引出接触的光刻,这直接决定了整个器件的集成度以及信号抗干扰能力。然而,BiCS 结构虽然通过存储阵列与选择晶体管堆叠放置而分别利用控制栅极阈值,并且通过分层连接栅极避免了过大深宽比的接触孔或栅极开口的复杂工艺,但是只能通过多晶硅材质的栅极诱导漏极泄漏电流 (GIDL) 进行擦除,无法进行体擦除,读写效率较低。

发明内容

[0006] 由上所述,本发明的目的在于克服上述技术困难,一种能以较低成本实现接触互连并且保持金属栅控制性能的新型三维存储器结构的制造方法。

[0007] 为此,本发明一方面提供了一种三维存储器制造方法,包括步骤:在衬底上形成第一材料层与第二材料层的堆叠结构;刻蚀堆叠结构露出衬底,形成垂直的多个第一开孔;在每个第一开孔中形成填充层;在每个第一开孔周围,刻蚀堆叠结构露出衬底,形成垂直的多个第二开孔;在每个第二开孔中形成垂直的沟道层和漏极;选择性刻蚀去除填充层,重新露出第一开孔;侧向刻蚀部分或者完全去除第二材料层,留下凹槽;在凹槽中形成栅极堆叠结构;在每个第一开孔底部的衬底上和/或中形成共源极。

[0008] 其中,第一材料层、第二材料层、填充层三者之间具有各自不同的刻蚀选择性。

[0009] 其中,第一材料层、第二材料层、填充层材料选自氧化硅、氮化硅、氮氧化硅、非晶硅、非晶锗、DLC、非晶碳的任意一种及其组合。

[0010] 其中,第一开孔的尺寸大于或等于第二开孔的尺寸。

[0011] 其中,沟道层为中心包括绝缘体的中空结构。

[0012] 其中,形成共源极之后进一步包括,在每个第一开孔侧壁形成绝缘层,在绝缘层侧壁以及每个第一开孔底部形成接触共源区的接触层。

[0013] 其中,形成接触层之时或者之后进一步包括,控制沉积工艺参数或者回刻使得接触层的顶面低于栅极堆叠结构最顶层的底面,并且采用绝缘层回填。

[0014] 其中,形成接触层之后进一步包括,刻蚀去除部分第一材料层、栅极堆叠结构形成第三开孔,在第三开孔中沉积绝缘材料形成与栅极堆叠结构最顶层之间的隔离绝缘区。

[0015] 其中,形成隔离绝缘区之后进一步包括,在器件上形成层间介质层,刻蚀层间介质层形成第四开孔直至露出接触层,填充金属形成共源线引线。

[0016] 其中,形成共源线接触塞之后进一步包括,在器件上形成第二层间介质层,刻蚀第二层间介质层形成第五开孔直至暴露沟道区,填充金属形成位线接触。

[0017] 其中,刻蚀形成第一开孔之前进一步包括,在阵列区域周围的字线接触区域刻蚀堆叠结构形成台阶,依次暴露每个第一材料层和第二材料层的端部。

[0018] 本发明另一方面提供了一种三维存储器制造方法,包括步骤:在衬底上形成第一材料层与第二材料层的堆叠结构;刻蚀堆叠结构露出衬底,同时形成垂直的多个第一开孔以及在每个第一开孔周围的多个第二开孔;在每个第一开孔中形成填充层;在每个第二开孔中形成垂直的沟道层和漏极;选择性刻蚀去除填充层,重新露出第一开孔;侧向刻蚀部分或者完全去除第二材料层,留下凹槽;在凹槽中形成栅极堆叠结构;在每个第一开孔底部的衬底上和/或中形成共源极。

[0019] 本发明又一方面提供了一种三维存储器,包括:在衬底上垂直分布的多个共源极引线,与衬底中和/或上的共源极接触;在每个共源极引线周围垂直于衬底分布的多个沟道层,每个沟道层顶部具有漏极;在每个沟道层侧壁上的多个绝缘隔离层以及在每个绝缘隔离层之间的多个栅极堆叠结构。

[0020] 依照本发明的三维存储器制造方法,将 TCAT 三维器件的字线深槽替换为深孔刻蚀来完成相同的功能,提高集成密度,简化堆叠结构的刻蚀工艺,保留了金属栅控制性能。

附图说明

[0021] 以下参照附图来详细说明本发明的技术方案,其中:

[0022] 图 1 至图 10 为依照本发明的三维半导体存储器件制造方法的各个步骤的剖视图和/或顶视图。

具体实施方式

[0023] 以下参照附图并结合示意性的实施例来详细说明本发明技术方案的特征及其技术效果,公开了能以较低成本实现接触互连并且保持金属栅控制性能的新型三维存储器结构的制造方法。需要指出的是,类似的附图标记表示类似的结构,本申请中所用的术语“第一”、“第二”、“上”、“下”等等可用于修饰各种器件结构或制造工序。这些修饰除非特别说明并非暗示所修饰器件结构或制造工序的空间、次序或层级关系。

[0024] 如图 1 所示,在衬底 1 上交替形成第一材料层 2A 与第二材料层 2B 的堆叠结构 2。衬底 1 材质可以包括体硅 (bulk Si)、体锗 (bulkGe)、绝缘体上硅 (SOI)、绝缘体上锗 (GeOI) 或者是其他化合物半导体衬底,例如 SiGe、SiC、GaN、GaAs、InP 等等,以及这些物质的组合。为了与现有的 IC 制造工艺兼容,衬底 1 优选地为含硅材质的衬底,例如 Si、SOI、SiGe、Si:C 等。堆叠结构 2 的选自以下材料的组合并且至少包括一种绝缘介质:如氧化硅、氮化硅、非晶碳、类金刚石无定形碳 (DLC)、氧化锗、氧化铝、等及其组合。第一材料层 2A 具有第一刻蚀选择性,第二材料层 2B 具有第二刻蚀选择性并且不同于第一刻蚀选择性(例如两种材料之间的刻蚀选择比大于 5:1 并优选大于 10:1)。在本发明一个优选实施例中,叠层结构 2A/2B 均为非导电材料,层 2A/层 2B 的组合例如氧化硅与氮化硅的组合、氧化硅与(未掺杂)多晶

硅或非晶硅的组合、氧化硅或氮化硅与非晶碳的组合等等。在本发明另一优选实施例中,层 2A 与层 2B 在湿法腐蚀条件或者在氧等离子干法刻蚀条件下具有较大的刻蚀选择比(例如大于 5:1)。层 2A、层 2B 的沉积方法包括 PECVD、LPCVD、HDPCVD、MOCVD、MBE、ALD、热氧化、蒸发、溅射等各种工艺。在本发明一个最优实施例中,层 2A 为二氧化硅,层 2B 为氮化硅。如图 1 所示,最低部的层 2B 将用于未来最底层选择栅电极形成,因此标注为 LSG,最顶部的层 2B 将用于未来最顶层选择栅电极形成,因此标注为 USG,中部具有从 WL0 ~ WLn 的多个层 2B 以用于 n+1 条位线。图 1 中仅示出了 n = 2 的情形,但是实际上 n 可以依照需要为大于等于 1 的任何正整数。

[0025] 任选的,如图 2 所包括的剖视图 2A 和顶视图 2B 所示,刻蚀堆叠结构 2A/2B,依次露出一部分层 2A/2B 的侧面端部以形成台阶状的字线焊垫区域(WL-Pad Region, WLPR),中心区域为阵列区域(Array Region, AR)。其中,在 WLPR 区域,依次暴露了顶层 USG 上方的层 2A:USG、用于 WL2 的层 2B 上方的层 2A:WL2、用于 WL1 的层 2B 上方的层 2A:WL1、用于 WL0 的层 2B 上方的层 2A:WL0、用于 LSG 的层 2B 上方的层 2A:LSG、以及保护衬底 1 的层 2A。以下图 3 至图 10 的步骤将针对图 2 中的中心的阵列区域进行,换言之也即各个顶视图仅示出了区域 2A:AR 中的一部分。

[0026] 在现有技术的 TCAT 结构制造方法中,一般是刻蚀深孔并沉积多晶硅等沟道材料形成沟道后,通过执行深槽刻蚀暴露出作为层 2B 的伪栅(SiN),之后移去层 2B 的伪栅并完成栅堆栈介质层和金属电极沉积等步骤完成存储单元的制备;随后通过侧墙、注入和硅化来完成共源区形成;接着通过深槽的氧化物填充、CMP,共源区 CSL 接触孔刻蚀和填充,金属线连线来完成 CSL 的连线。如背景技术部分所述,这种后形成的深槽往往难以兼顾深宽比以及金属填充率,容易导致器件失效。

[0027] 与之对照的,本发明的一个实例不用深槽而用如图 3 所示的深孔刻蚀,这样工艺和沟道形成工艺相同,在完成存储单元的制备之后,直接通过侧墙、硅化和金属的深孔填充完成共源区的接触,然后引线完成 CSL 连线。相对而言,多层介质刻蚀工艺简单,存储阵列的密度提高,共源区的接触孔引出工艺更加简单,原有的二氧化硅填充深槽并平坦化、刻蚀接触孔、填充接触孔的方式直接被深孔的侧墙绝缘层和金属接触孔填充所替代。

[0028] 如包括剖视图 3A、顶视图 3B 的图 3 所示,在阵列区域刻蚀堆叠结构 2 直至暴露衬底 1(该区域将形成未来的共源区),形成作为伪栅极开孔的第一开孔(未示出)并在伪栅极开孔中形成填充层 3。在稍后图 5 所示的步骤中,第一开孔将作为形成共源区 1S 以及侧向刻蚀去除部分层 2B 所用的入口区域。优选地,采用 RTE 或等离子干法刻蚀各向异性刻蚀层 2A/层 2B 的堆叠结构 2,形成露出衬底 1 以及衬底 1 上交替堆叠的层 2A/层 2B 的侧壁的第一开孔(未示出)。刻蚀气体例如针对二氧化硅和氮化硅等材质的碳氟基刻蚀气体,并且通过增加碳氟比而在侧壁形成由含 C 聚合物形成的临时保护侧壁,最终获得较好的垂直侧壁。在本发明一个优选实施例中刻蚀气体优选 C_3F_6 、 C_4F_8 等含 C 量比较高的气体并进一步优选通过增加氧化性气体如 O_2 、CO 等控制侧壁形貌。平行于衬底 1 表面切得的孔槽的截面形状可以为矩形、方形、菱形、圆形、半圆形、椭圆形、三角形、五边形、五角形、六边形、八边形等等各种几何形状。填充层 3 沉积方法包括 PECVD、HDPCVD、MOCVD、MBE、ALD、蒸发、溅射等,材质优选为与堆叠结构 2 的层 2A、层 2B 均具有高选择性的材料,例如层 3、层 2A、层 2B 三者之间每两个之间的刻蚀选择比均大于等于 5:1。在本发明一个优选实施例中,层 2A 为

氧化硅,层 2B 为氮化硅,填充层为非晶硅、非晶锗、非晶碳、DLC 等,反之亦然。

[0029] 接着,如包括剖视图 4A、顶视图 4B 的图 4 所示,在每个第一开孔周围刻蚀形成多个第二开孔并形成垂直的沟道区 4。与刻蚀形成第一开孔的工艺类似,RIE 或等离子干法刻蚀各向异性刻蚀层 2A/层 2B 的堆叠结构 2,在第一开孔的周围形成多个露出衬底 1 以及衬底 1 上交替堆叠的层 2A/层 2B 的侧壁的第二开孔(未示出)。刻蚀气体例如针对二氧化硅和氮化硅等材质的碳氟基刻蚀气体,并且通过增加碳氟比而在侧壁形成由含 C 聚合物形成的临时保护侧壁,最终获得较好的垂直侧壁。在本发明一个优选实施例中刻蚀气体优选 C_3F_8 、 C_4F_8 等含 C 量比较高的气体并进一步优选通过增加氧化性气体如 O_2 、CO 等控制侧壁形貌。如图 4A、4B 所示,用于暴露共源区的第一开孔的尺寸(例如直径)要大于或等于用于形成沟道区的第二开孔尺寸,例如两者尺寸(直径或者多边形的最大跨距的比值)比大于 1.5 并优选大于等于 2。在本发明一个实施例中,每一个第一开孔周围具有六个第二开孔,以便于提高稍后侧向刻蚀层 2B 的效率以及均匀性。在本发明其他实施例中,每一个第一开孔周围可以具有的第二开孔的数目为 2、3、4、5、6、7、8、9 乃至更多。

[0030] 此后,在第二开孔中形成多个垂直的沟道层 4。沟道层 4 的材质可以包括单晶硅、单晶锗、SiGe、Si:C、SiGe:C、SiGe:H 等半导体材料,沉积工艺包括 LPCVD、PECVD、HDPCVD、MOCVD、MBE、ALD 等。在本发明一个实施例中,沟道层 4 的沉积方式为局部填充第二开孔的侧壁而形成具有空气隙的中空柱形。在本发明其他实施例中,选择沟道层 4 的沉积方式以完全或者局部填充第二开孔,形成实心柱、空心环、或者空心环内填充绝缘层(未示出)的核心-外壳结构。沟道层 4 的水平截面的形状与第二开孔类似并且优选地共形,可以为实心的矩形、方形、菱形、圆形、半圆形、椭圆形、三角形、五边形、五角形、六边形、八边形等等各种几何形状,或者为上述几何形状演化得到的空心的环状、桶状结构(并且其内部可以填充绝缘层)。优选地,对于空心的柱状沟道层 4 结构,可以进一步在沟道层 4A 内侧填充绝缘隔离层 4B,例如通过 LPCVD、PECVD、HDPCVD 等工艺形成例如氧化硅材质的层 4B,用于支撑、绝缘并隔离沟道层 4A。此后,在沟道层 4 顶部沉积漏区接触 4D。优选地,采用与沟道层 4 材质相同或者相近(例如与 Si 相近的材质 SiGe、SiC 等,以便微调晶格常数而提高载流子迁移率,从而控制元器件的驱动性能)的材质沉积在第二开口的顶部而形成存储器件单元晶体管的漏区 4D,并且可以进一步形成硅化物(未示出)以降低接触电阻。

[0031] 如剖视图 5A 和顶视图 5B 所示,选择性刻蚀去除填充层 3,重新露出第一开孔 2T,利用第一开孔 2T 侧向刻蚀去除堆叠结构中的第二材料层(伪栅极层)2B。首先,采用垂直的各向异性刻蚀工艺,例如采用 RIE 或等离子干法刻蚀工艺(进一步提高碳氟比以刻蚀非晶硅、非晶锗,或者采用氧等离子干法刻蚀去除非晶碳、DLC 材质的填充层 3),或者针对填充层 3 的材质而选用基本或者完全不腐蚀层 2A、层 2B 的腐蚀液来湿法腐蚀去除层 3(例如针对非晶硅材质的层 3,采用 TMAH 腐蚀液)。垂直的各向异性刻蚀工艺完全去除了填充层 3,重新露出了较宽的垂直的第一开孔 2T。随后,采用各向同性干法刻蚀工艺,横向刻蚀去除层 2B,在层 2A 之间留下了侧向凹槽 2R。例如减小碳氟比以横向刻蚀氮化硅的层 2B、或者采用热磷酸腐蚀氮化硅的层 2B。备选地,当层 2A 为氮化硅、层 2B 为氧化硅时,可以采用 HF 基腐蚀液腐蚀层 2B。

[0032] 如附图 6 所示,在第一开孔 2T 底部形成共源区 1S,在凹槽 2R 中形成栅极堆叠结构 5A/5B。可以通过离子注入掺杂、以及优选地进一步在表面形成金属硅化物(未示出)而形

成源区 1S。金属硅化物例如 NiSi_{2-y} 、 $\text{Ni}_{1-x}\text{Pt}_x\text{Si}_{2-y}$ 、 CoSi_{2-y} 或 $\text{Ni}_{1-x}\text{Co}_x\text{Si}_{2-y}$ ，其中 x 均大于 0 小于 1， y 均大于等于 0 小于 1。栅极堆叠结构 5 包括栅极绝缘层 5A 和栅极导电层 5B。层 5A 的沉积方法包括 PECVD、HDPCVD、MOCVD、MBE、ALD、蒸发、溅射等。图中未示出的是，层 5A 优选地进一步包括多个子层，例如隧穿层、存储层、阻挡层。其中隧穿层包括 SiO_2 或高 k 材料，其中高 k 材料包括但不限于氮化物（例如 SiN 、 SiON 、 AlN 、 TiN ）、金属氧化物（主要为副族和铜系金属元素氧化物，例如 MgO 、 Al_2O_3 、 Ta_2O_5 、 TiO_2 、 ZnO 、 ZrO_2 、 HfO_2 、 CeO_2 、 Y_2O_3 、 La_2O_3 ）、氮氧化物（如 HfSiON ）、钙钛矿相氧化物（例如 $\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$ (PZT)、 $\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$ (BST)) 等，隧穿层可以是上述材料的单层结构或多层堆叠结构。存储层是具有电荷俘获能力的介质材料，例如 SiN 、 HfO 、 ZrO 等及其组合，同样可以是上述材料的单层结构或多层堆叠结构。阻挡层可以是氧化硅、氧化铝、氧化铪等介质材料的单层结构或多层堆叠结构。在本发明一个实施例中，层 5A 例如是氧化硅、氮化硅、氧化硅组成的 ONO 结构。

[0033] 栅极导电层 5B 可以是多晶硅、多晶锗硅、或金属，其中金属可包括 Co、Ni、Cu、Al、Pd、Pt、Ru、Re、Mo、Ta、Ti、Hf、Zr、W、Ir、Eu、Nd、Er、La 等金属单质、或这些金属的合金以及这些金属的氮化物，栅极导电层 5B 中还可掺杂有 C、F、N、O、B、P、As 等元素以调节功函数。栅极绝缘层 5A 与栅极导电层 5B 之间还优选通过 PVD、CVD、ALD 等常规方法形成氮化物的阻挡层（未示出），阻挡层材质为 M_xN_y 、 $\text{M}_x\text{Si}_y\text{N}_z$ 、 $\text{M}_x\text{Al}_y\text{N}_z$ 、 $\text{M}_x\text{Al}_y\text{Si}_z\text{N}_z$ ，其中 M 为 Ta、Ti、Hf、Zr、Mo、W 或其它元素。同样地，层 5B 可以是单层结构也可以是多层堆叠结构。

[0034] 进一步地，如图 6 所示，在第一开孔 2T 侧壁形成较薄的绝缘层 6A 并在绝缘层 6A 中填充金属形成源极接触 6B。绝缘层 6A 可以采用热氧化、化学氧化、PECVD、HDPCVD 等工艺形成，材质可以为氧化硅、氮化硅或高 K 材料。层 6A 优选仅覆盖第一开孔 2T 侧壁，底部堆积的较薄部分可以采用湿法腐蚀工艺或者各向同性干法刻蚀工艺去除，类似于侧墙技术。随后，采用 MOCVD、MBE、ALD、蒸发、溅射等工艺形成低电阻的共源极接触线 6B，也称作 CSL。优选地，采用 CMP 或者回刻方法，或者调整沉积金属工艺参数，降低层 6B 的高度使其顶部低于最顶部的栅极堆叠结构 5A/5B 的底面（顶部的该金属栅极结构即用于顶部选择晶体管的顶部选择栅线 USG），接着再回填绝缘层 6A 直至与最顶层的层 2A 齐平。

[0035] 此后，优选地，如图 7A 剖视图和图 7B 顶视图所示，刻蚀去除 CSL 层 6B 顶部的绝缘层 6A，露出下方的层 6B。在该刻蚀步骤中，刻蚀形成的第三开孔 6T 尺寸要大于第一开孔 2T 的尺寸（例如圆形的直径或多边形的最大跨距），去除了一部分 USG 层级的栅极堆叠结构 5A/5B。如图 7B 所示，共源极接触线 CSL 图形连接了多个第三开孔 6T，并且可以进一步延伸出存储单元区而连接至外部电路形成互连线。

[0036] 如图 8 所示，在第三开孔 6T 中填充同样的绝缘层 6A，形成了顶层选择栅极线的隔离绝缘区。

[0037] 如图 9 所示，在整个器件之上形成层间介质层 (ILD) 7。例如采用喷涂、旋涂、CVD 沉积等工艺形成低 k 材料的 ILD 7，低 k 材料包括但不限于有机低 k 材料（例如含芳基或者多元环的有机聚合物）、无机低 k 材料（例如无定形碳氮薄膜、多晶硼氮薄膜、氟硅玻璃、BSG、PSG、BPSG）、多孔低 k 材料（例如二硅三氧烷 (SSQ) 基多孔低 k 材料、多孔二氧化硅、多孔 SiOCH 、掺 C 二氧化硅、掺 F 多孔无定形碳、多孔金刚石、多孔有机聚合物）。随后刻蚀 ILD 7 直至暴露 CSL 层 6B，形成第四开孔（未示出）并沉积金属材料形成接触塞 8，连接了阵列的共源区 1S。

[0038] 如图 10A 和图 10B 所示,完整位线连接。在第一 ILD 7 之上采用类似工艺和材质沉积第二 ILD 9 并刻蚀形成暴露沟道区 4D 的接触孔,沉积金属形成位线连接 10。

[0039] 值得注意的是,图 1 至图 10 仅示出了根据本发明一个实施例的工艺方法,本发明还可以采用其他工序完成三维存储器件的制造。例如,在本发明一个优选的备选实施例中,图 3B 和图 4B 所示的用于共源区的第一开孔与用于沟道区的第二开孔可以通过一次光刻/刻蚀构图实现,也即图 3 和图 4 所示工艺可以合并,只要在每个第一开孔周边存在多个第二开孔即可。在本发明另一备选实施例中,在执行完成图 6 所示的栅极堆叠结构填充之后,在图 7A、图 7B 以及之后所示的连线阶段按照图 7B、图 10B 所示的版图进行刻蚀,完成各层栅电极隔离(中心包围了金属层 6A 的隔离层 6B 图形)并形成共源极连线 CSL 图形。具体地,在刻蚀孔完成栅堆栈沉积以后,然后介质填充平坦化整个平面,然后按照图 10B 所示 CSL 标注的区域进行物理刻蚀,类似于 TCAT 工艺中 WL-Cut 的步骤,沉积薄的介质层侧墙,然后沉积金属等导电层形成一个共源区的导电面。好处在于,前一个实例中除了 USG 隔离其他的 WL 没有隔离,这个方法可以完全像 TCAT 一样完成各层 WL 的隔离。

[0040] 在本发明另一备选实施例中,可以在图 5 移除作为伪栅极的层 2B 工序之中,与图 5 所示相邻两个第一开孔 2T 直线连线之间仅有一个沟道层 4 不同,如图 10C 所示,可以在两列(沿图 5B 中上下方向排列)第一开孔 2T 之间具有多个沟道层 4,由此增大了第一开孔 2T 之间的距离,并且在刻蚀去除层 2B 时仅部分去除而在凹槽 2R 中保留部分伪栅极层 2B,利用伪栅极层 2B 的自对准完成了控制栅的自动隔离。换言之,相邻的两列沟道层 4 之间的栅极堆叠结构 5A/5B 的侧面通过残留的第二材料层 2B 而绝缘隔离,增强了器件的绝缘性能。

[0041] 依照本发明的三维存储器制造方法,将 TCAT 三维器件的字线深槽替换为深孔刻蚀来完成相同的功能,提高集成密度,简化堆叠结构的刻蚀工艺,保留了金属栅控制性能。

[0042] 尽管已参照一个或多个示例性实施例说明本发明,本领域技术人员可以知晓无需脱离本发明范围而对器件结构或方法流程做出各种合适的改变和等价方式。此外,由所公开的教导可做出许多可能适于特定情形或材料的修改而不脱离本发明范围。因此,本发明的目的不在于限定在作为用于实现本发明的最佳实施方式而公开的特定实施例,而所公开的器件结构及其制造方法将包括落入本发明范围内的所有实施例。

2A
2B: USG
2A
2B: WL2
2A
2B: WL1
2A
2B: WL0
2A
2B: LSG
2A
1

图 1

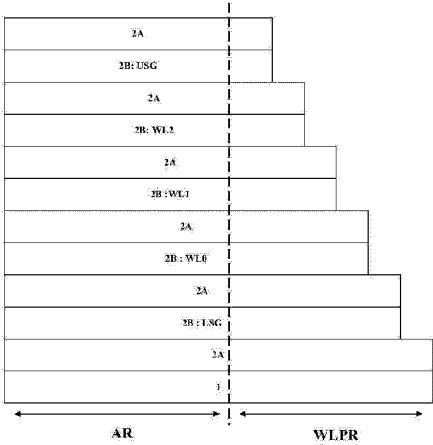


图 2A

2A: AR
2A: USG
2A: WL2
2A: WL1
2A: WL0
2A: LSG
2A

图 2B

2A	3	2A
2B: USG		2B: USG
2A		2A
2B: WL2		2B: WL2
2A		2A
2B: WL1		2B: WL1
2A		2A
2B: WL0		2B: WL0
2A		2A
2B: LSG		2B: LSG
2A	2A	
1		

图 3A

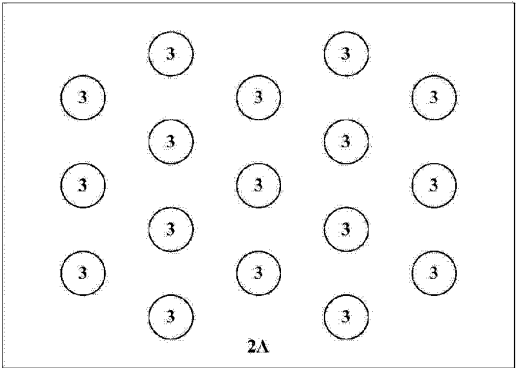


图 3B

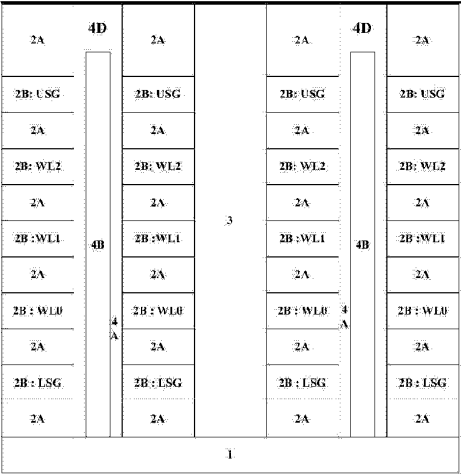


图 4A

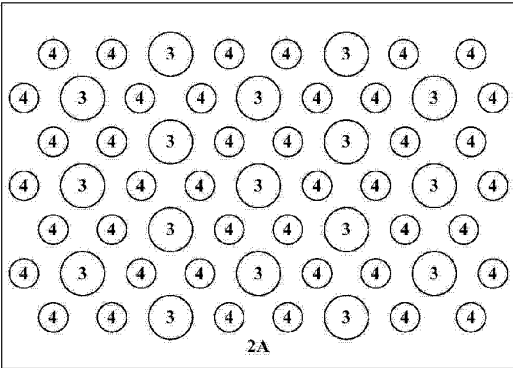


图 4B

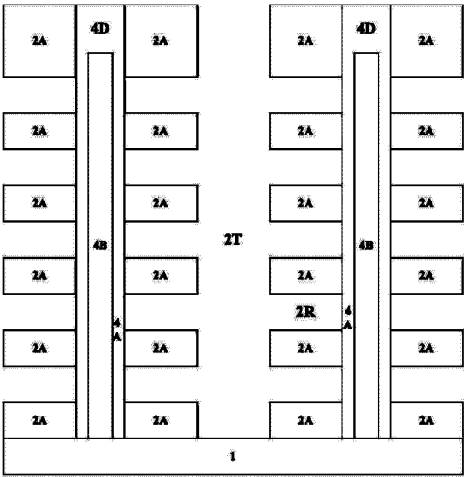


图 5A

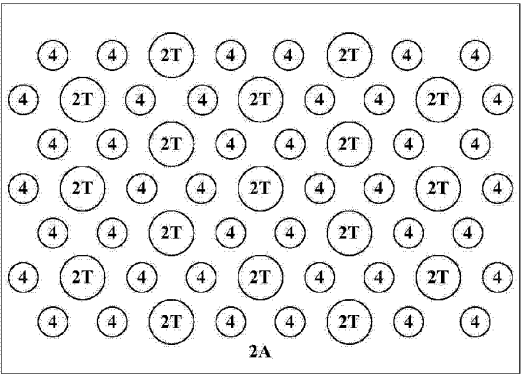


图 5B

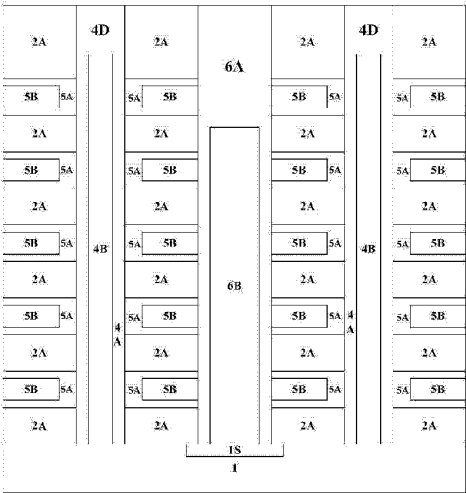


图 6

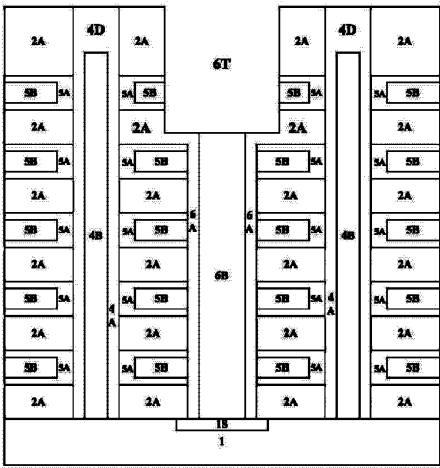


图 7A

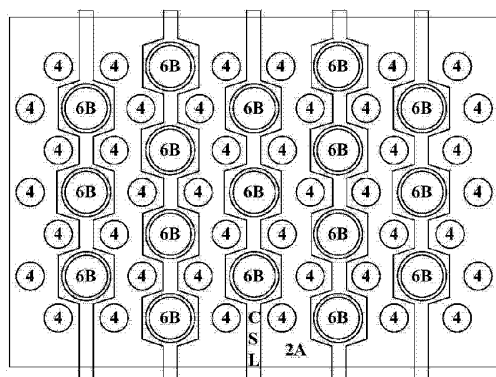


图 7B

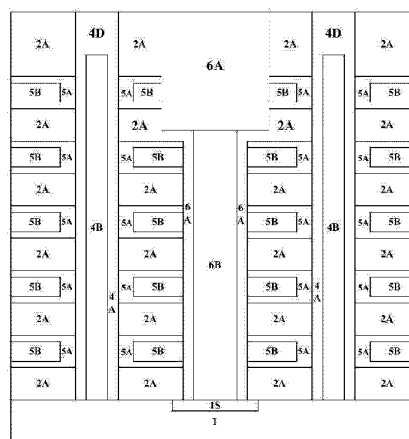


图 8

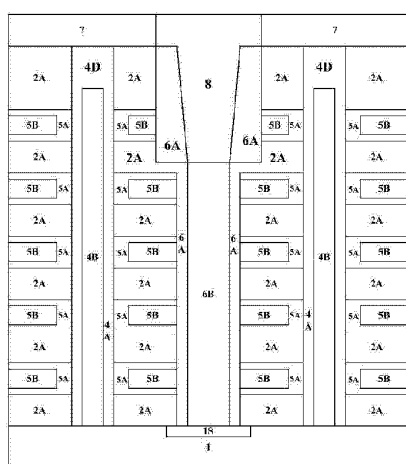


图 9

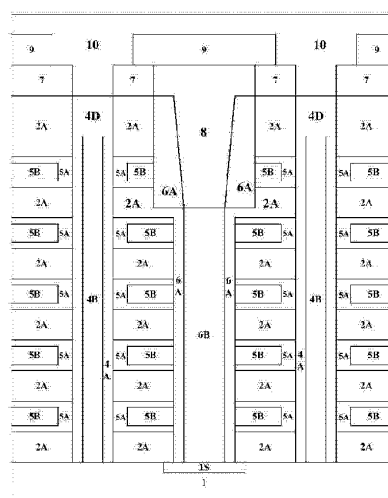


图 10A

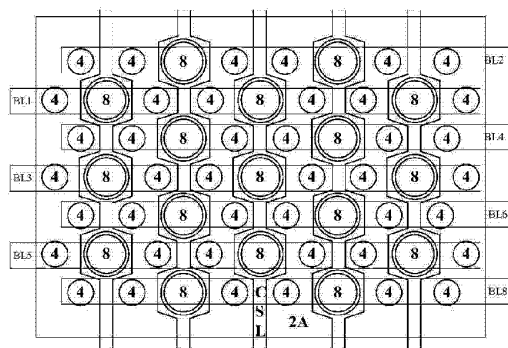


图 10B

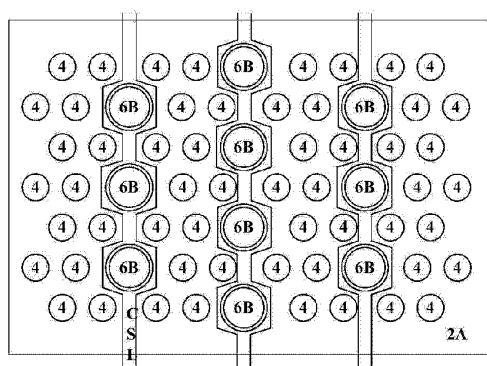


图 10C

Electronic Patent Application Fee Transmittal				
Application Number:		16126947		
Filing Date:		10-Sep-2018		
Title of Invention:		WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		
First Named Inventor/Applicant Name:		Jifeng ZHU		
Filer:		Min Yang/Laney Flanagan		
Attorney Docket Number:		4123.0480002		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
Total in USD (\$)				240

Electronic Acknowledgement Receipt	
EFS ID:	37719775
Application Number:	16126947
International Application Number:	
Confirmation Number:	1077
Title of Invention:	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF
First Named Inventor/Applicant Name:	Jifeng ZHU
Customer Number:	26111
Filer:	Min Yang/Laney Flanagan
Filer Authorized By:	Min Yang
Attorney Docket Number:	4123.0480002
Receipt Date:	12-NOV-2019
Filing Date:	10-SEP-2018
Time Stamp:	10:24:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 240
RAM confirmation Number	E2019ABA25323668
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		4123048_Bundle.pdf	74778	yes	9
			086f273b000c67816aba14e9206284a7add1f230		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Miscellaneous Incoming Letter		1	2	
	Transmittal Letter		3	8	
	Information Disclosure Statement (IDS) Form (SB08)		9	9	
Warnings:					
Information:					
2	Foreign Reference	FP1_CN104157654A.pdf	225294	no	16
			a5e0d8fa0a7de10fb500ce84d5754ffc7db48d4		
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30363	no	2
			80a08305d7e515d584d0432016bb80b010831447		
Warnings:					
Information:					
Total Files Size (in bytes):			330435		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

MIN YANG
PATENT AGENT
(202) 772-8702
MYANG@STERNEKESSLER.COM



November 12, 2019

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 1077
Art Unit 2812
Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Application No. 16/126,947; Filing Date: September 10, 2018
For: **WORD LINE CONTACT STRUCTURE FOR THREE-
DIMENSIONAL MEMORY DEVICES AND FABRICATION
METHODS THEREOF**
Inventors: ZHU *et al.*
Our Ref: 4123.0480002

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Online Credit Card Payment Authorization in the amount of \$240.00 in payment of the fee under 37 C.F.R. § 1.17(p);
2. Second Supplemental Information Disclosure Statement;
3. Form PTO/SB/08a (1 sheet) listing 3 documents (**US1-US2** and **FP1**); and
4. A copy of the cited document (**FP1**).

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Sterne, Kessler, Goldstein & Fox P.L.L.C. | 1100 New York Avenue, NW | Washington, D.C. 20005
P 202.371.2800 | F 202.371.2540 | sternekessler.com

Commissioner for Patents
November 12, 2019
Page 2

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Min Yang/

Min Yang
Agent for Applicant
Registration No. 78,149

M-Y/lef
Enclosures

14130995_1

Sterne, Kessler, Goldstein & Fox P.L.L.C. | 1100 New York Avenue, NW | Washington, D.C. 20005
P 202.371.2800 | F 202.371.2540 | sternekessler.com

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: ZHU *et al.*

Confirmation No.: 1077

Applicant: Yangtze Memory Technologies
Co., Ltd.

Art Unit: 2812

Application No.: 16/126,947

Examiner: GEYER, SCOTT B

Filing Date: September 10, 2018

Atty. Docket: 4123.0480002

Title: **WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY
DEVICES AND FABRICATION METHODS THEREOF**

Second Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

Listed on accompanying IDS Form PTO/SB/08a equivalent are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Form based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist.

The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicant has checked the appropriate boxes below.

- ☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement: (i) was first cited in any communication from a patent office in a counterpart¹ foreign or international application or from the Office; and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of this information disclosure statement; OR (ii) is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of the information disclosure statement.
- ☐ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.
- ☒ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office

¹ The term counterpart foreign patent application means that a claim for priority has been made in either the U.S. application or a foreign application based on the other, or that the disclosures of the U.S. and foreign patent applications are substantively identical (e.g., an application filed in the European Patent Office claiming the same U.K. priority as claimed in the U.S. application).

Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.
37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement.
37 C.F.R. § 1.97(e)(2).
- ☒ c. The required fee is provided through online credit card payment authorization in the amount of \$240.00 in payment of the fee under 37 C.F.R. § 1.17(p).
- ☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but on or before payment of the Issue Fee. The required fee is provided through online credit card payment authorization in the amount of \$240.00 in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

Atty. Dkt. No. 4123.0480002

- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- ☒ 5. The patent family for one or more foreign language documents submitted herewith includes a United States patent, and other patent, in the English language. Copies of both the particular foreign patent(s) or published foreign patent applications cited in the foreign patent office communication, and that are not already of record in this application, are enclosed. Copies of the related United States or other English language patent or published application from the family list, if not already of record, are listed on the accompanying SB/08A form. For the purposes of a statement under 37 CFR 1.97(e)(1), the United States or other English language patent or published application are to be construed as being cited by the foreign patent office. MPEP 609.04(b)(V).

Atty. Dkt. No. 4123.0480002

- ☐ 6. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. MPEP 609.04(a)(III).
- ☒ 7. A concise explanation of the relevance of the non-English language document appears below in accordance with 37 C.F.R. § 1.98(a)(3).
- Document **US2** (2017/0236836 A1) is submitted herewith as the English-language counterpart of document **FP1** (CN 104157654 A).
- ☒ 8. A copy of document **FP1** is submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of the U.S. patent application publications cited as documents **US1-US2** on the attached IDS Form are submitted.
- ☐ 9. Copies of the _____ documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. _____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).
- ☐ 10. It is expected that the examiner will review the prosecution and cited art in the parent Application No(s). _____ in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.
- ☐ 11. In accordance with the Federal Circuit decision in *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003), Applicants submit herewith Office Actions from the co-

Atty. Dkt. No. 4123.0480002

pending U.S. Patent Application No. _____, filed _____, as documents _____ to _____. The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Form, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Min Yang/

Min Yang
Agent for Applicant
Registration No. 78,149

Date: November 12, 2019

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

14130993_1

Atty. Dkt. No. 4123.0480002

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 16/126,947		Filing Date 09/10/2018		☐ To be Mailed	
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO									
APPLICATION AS FILED - PART I									
FOR		(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA			RATE (\$)		FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A			N/A			
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A			N/A			
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A			N/A			
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*			x \$100 =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*			x \$460 =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL			
APPLICATION AS AMENDED - PART II									
AMENDMENT	01/21/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	x \$100 =		0	
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	x \$460 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		0	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =			
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						LIE			
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/NICOLE LOVE HENSLEY/			
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".									
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: ZHU *et al.*

Applicant: Yangtze Memory Technologies
Co., Ltd.

Application No.: 16/126,947

Filing Date: September 10, 2018

Confirmation No.: 1077

Art Unit: 2812

Examiner: GEYER, SCOTT B

Atty. Docket: 4123.0480002

Title: **WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY
DEVICES AND FABRICATION METHODS THEREOF**

Amendment and Reply Under 37 C.F.R. § 1.111

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In reply to the Non-Final Office Action dated **October 24, 2019** ("Office Action"),

Applicant submits the following Amendment and Remarks.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A semiconductor structure, comprising:
 - a staircase structure comprising a plurality of steps, wherein each step comprises a ~~conductive layer~~ gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;
 - a barrier layer disposed over a portion of the ~~conductive layer~~ gate stack of the each step;
 - an etch-stop layer disposed on the barrier layer;
 - an insulating layer disposed on the etch-stop layer; and
 - a plurality of conductive structures formed in the insulating layer, wherein each conductive structure is formed on the conductive layer of the each step.
2. (Currently Amended) The semiconductor structure of claim 1, wherein the plurality of conductive structures extend through the barrier layer and the high-k dielectric layer.
3. (Original) The semiconductor structure of claim 1, wherein the plurality of conductive structures extend through the etch-stop layer.
4. (Original) The semiconductor structure of claim 1, wherein the barrier layer comprises silicon oxide.
5. (Original) The semiconductor structure of claim 1, wherein the etch-stop layer comprises one or more of silicon nitride, a spin-on-dielectric, and a high-k dielectric.

Atty. Dkt. No. 4123.0480002

6. (Original) The semiconductor structure of claim 1, wherein the each conductive structure directly contacts a corresponding one of the conductive layer of the each step.
7. (Original) The semiconductor structure of claim 1, wherein top surfaces of the plurality of conductive structures, the insulating layer, and a portion of the etch-stop layer are coplanar.
8. (Original) The semiconductor structure of claim 1, wherein the plurality of conductive structures comprise one or more of tungsten, cobalt, nickel, copper, and aluminum.
9. (Original) The semiconductor structure of claim 1, wherein the barrier layer is formed on side and top surfaces of the plurality of steps.
10. (Original) The semiconductor structure of claim 1, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.
11. (Currently Amended) A semiconductor structure, comprising:
 - a staircase structure comprising a plurality of steps, wherein each step comprises a ~~conductive layer~~ gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;
 - an etch-stop layer disposed ~~on~~ on a portion of the ~~conductive layer~~ gate stack of the each step;
 - an insulating layer disposed on the etch-stop layer; and
 - a plurality of conductive structures formed in the insulating layer and extending through the etch-stop layer and the high-k dielectric layer, wherein each conductive structure directly contacts the corresponding conductive layer of each step.

12. (Original) The semiconductor structure of claim 11, wherein the etch-stop layer is formed on a side surface and a top surface of each step.

13. (Original) The semiconductor structure of claim 12, wherein thicknesses of the etch-stop layer is the same on the side and top surfaces of each step.

14. (Original) The semiconductor structure of claim 11, wherein the etch-stop layer comprises one or more of silicon nitride, a spin-on-dielectric, and a high-k dielectric.

15. (Original) The semiconductor structure of claim 11, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.

16-20. (Cancelled)

21. (New) The semiconductor structure of claim 1, wherein the high-k dielectric layer comprises hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, or a combination thereof.

22. (New) The semiconductor structure of claim 1, wherein top and bottom surfaces and a sidewall of the conductive layer are covered by the high-k dielectric layer, except at an interface between the conductive layer and the conductive structure.

23. (New) The semiconductor structure of claim 11, wherein the high-k dielectric layer comprises hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, or a combination thereof.

24. (New) The semiconductor structure of claim 11, wherein top and bottom surfaces and a sidewall of the conductive layer are covered by the high-k dielectric layer, except at an interface between the conductive layer and the conductive structure.

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-15 and 21-24 are pending in the application, with claims 1 and 11 being the independent claims. Claims 16-20 are sought to be cancelled without prejudice to or disclaimer of the subject matter therein. Claims 1, 2 and 11 are sought to be amended. New claims 21-24 are sought to be added. The changes are not believed to introduce any new matter, and their entry is respectfully requested.

Based on the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn. Throughout the arguments, Applicant reminds the Examiner that the claims are given their broadest reasonable meaning in view of the specification, and any paraphrasing of the claim features is not to be interpreted as reading any features into, or characterizing of, the claims.

Rejections under 35 U.S.C. § 102 and § 103

Claims 1-6, 9 and 11-14 were rejected under 35 U.S.C. §102(a)(1) as being allegedly anticipated by U.S. Patent Application Publication No. 2016/0358855 A1 to Oh. (“Oh”). **Claims 1-9 and 11-14** were rejected under 35 U.S.C. §102(a)(1) as being allegedly anticipated by U.S. Patent Application Publication No. 2016/0020169 A1 to Matsuda. (“Matsuda”). **Claims 10 and 15** were rejected under U.S.C. §103 as being allegedly unpatentable over Matsuda. Applicant respectfully traverses these rejections.

Without acquiescing to the propriety of the rejections and reserving the right to argue additional or different distinguishing features in the future, independent claims 1 and 11 are sought to be amended. Support for the amended features can be found throughout the originally filed

Atty. Dkt. No. 4123.0480002

specification, for example, in paragraphs [0059], [0061], [0062], [0071], [0072] and [0073], as well as Figures 9A and 9B.

Independent claim 1, as amended, recites, *inter alia*:

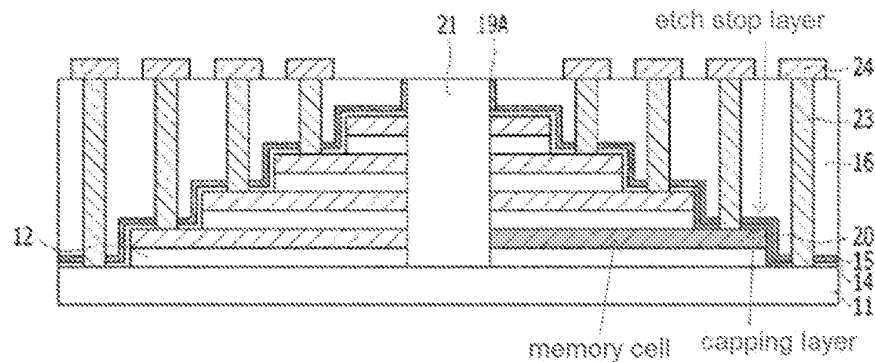
a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a **high-k dielectric layer** and a conductive layer;

a barrier layer disposed over a portion of the **gate stack** of the each step;

(Emphasis added.) Claim 11 recites similar distinguishing features, using its respective language.

Oh does not disclose or suggest the aforementioned distinguishing features. For example, Oh's capping layer 14 and etch-stop layer 15 are formed on the memory cells 20 directly. (Oh, ¶¶ [0016], [0036], FIGS. 1 and 2I-2K.) Oh's capping layer 14 and etch-stop layer 15 are respective oxide and nitride, while the memory cell 20 is a conductive material. (Oh, ¶¶ [0024]-[0025], [0036].)

FIG. 1



Annotated FIG. 2B of Matsuda

Additionally, dependent claims 2-10, 12 -15 are allowable at least based on their respective dependency to independent claims 1 and 11, and further in view of their distinguishing features. For example, Oh or Matsuda does not disclose that the conductive structures “extend through the barrier layer **and the high-k dielectric layer,**” as recited in claim 2. For at least these reasons, Applicant respectfully requests that the rejection of claims 1-15 under 35 U.S.C. § 102 or § 103, be reconsidered and withdrawn.

New Claims 21-24

New dependent claims 21-24 are sought to be added. Support for the new claims can be found throughout the originally filed specification, for example in paragraphs [0061]-[0062], [0071]-[0073], as well as originally filed drawings. Claims 21-24 are allowable at least because they recite all of the features of independent claims 1 and 11 from which they respectively depend, as well as for their additional distinguishing features.

Priority under 35 U.S.C. § 119

The Request to Retrieve Electronic Priority Application (PTO/SB/38) is submitted herein for the foreign priority application required by 37 CFR 1.55.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Atty. Dkt. No. 4123.0480002

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 1/21/20

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14372438_2.docx

Atty. Dkt. No. 4123.0480002

Request to Retrieve Electronic Priority Application(s)

Send completed form to: Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

COMPLETE IF KNOWN

Application Number	16/126,947
Filing Date	09/10/2018
First Named Inventor	ZHU et. al
Art Unit	2812
Examiner Name	GEYER, Scott B
Attorney Docket Number	4123.0480002

Pursuant to 37 CFR 1.55(i), the undersigned hereby requests that the USPTO retrieve an electronic copy of each of the following foreign applications for which priority has been claimed under 35 U.S.C. 119(a)-(d) from a foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement. This Request must be submitted:

- within the later of sixteen months from the filing date of the prior foreign application or four months from the actual filing date of an application under 35 U.S.C. 111(a),
- within four months from the later of the date of commencement (37 CFR 1.491(a)) or the date of the initial submission under 35 U.S.C. 371 of an application entering the national stage under 35 U.S.C. 371, or
- with a petition under 37 CFR 1.55(e) or (f).



OPTION A

Please retrieve the priority application identified in Column C, a certified copy of which is contained in the EP or JP application identified in Columns A and B:

A		B			C	
Code for Participating Office (EP or JP only)		Application containing the non-participating priority application			Non-participating priority application to be retrieved	
		App. No.	Filing Date	Access Code (for JP only)	Country Code	App. No.
1						



OPTION B

This Request may be used for the infrequent circumstance when a claim for priority to an application filed in a participating foreign intellectual property office was made prior to that foreign intellectual property office becoming a participating foreign intellectual property office.

Please retrieve the priority application identified in Columns A and B:

A		B		
Code for Participating Office (e.g., EP) or WIPO DAS Depositing Office (e.g., AU, BR, CN, DK, EA, EE, ES, FI, GB, IB, IN, JP, KR, MA, NL, NZ, SE)		Application to be retrieved		
		App. No.	Filing Date	Access Code (for WIPO DAS Depositing Office)
1				
2				

The USPTO will not attempt to retrieve the identified priority application(s) unless an identical claim for foreign priority to the application identified above is made pursuant to 37 CFR 1.55(d) or a petition is granted under 37 CFR 1.55(e) or (f). Applicants are advised to consult Private PAIR (accessed through www.uspto.gov) to assure that the retrieval has been successful. The applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period set forth in 37 CFR 1.55(g)(1).

I hereby declare that I have the authority to grant access to the above-identified foreign application(s).

/Donald J. Featherstone/

1/21/20

Signature

Donald J. Featherstone

Printed or Typed Name

Attorney for Applicant

Title

Date

202-371-2600

Telephone Number

33,876

Registration Number, if applicable

This collection of information is required by 37 CFR 1.55(d). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	38351792
Application Number:	16126947
International Application Number:	
Confirmation Number:	1077
Title of Invention:	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF
First Named Inventor/Applicant Name:	Jifeng ZHU
Customer Number:	26111
Filer:	Donald J. Featherstone/David Ofori Amanfo
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0480002
Receipt Date:	21-JAN-2020
Filing Date:	10-SEP-2018
Time Stamp:	15:54:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2020-01-21-Miscellaneous-Letter-4123-0480002.pdf	227032	no	1
			74fe97d86b1f5525955a80576fd756d5b0e02437		

Warnings:

Information:					
2		2020-01-21-Amendment-111-Reply-4123-0480002.pdf	408935 299abaad144237c2d7fc8d0c15a60e0b43f4333d	yes	10
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	5	
	Applicant Arguments/Remarks Made in an Amendment		6	10	
Warnings:					
Information:					
3	Request for USPTO to retrieve priority docs	2020-01-21-Request-Retrieve-Electronic-Priority-Application-4123-0480002.pdf	251283 a7f9a0a941a81f4162bc5763aa68aca038e9eac2	no	1
Warnings:					
Information:					
Total Files Size (in bytes):			887250		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

DONALD J. FEATHERSTONE
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January 21, 2020

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 1077
Art Unit 2812
Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Appl. No. 16/126,947; Filing Date: September 10, 2018
For: **WORD LINE CONTACT STRUCTURE OF THREE-
DIMENSIONAL MEMORY DEVICES AND FABRICATION
METHODS THEREOF**
Inventors: ZHU *et al.*
Our Ref: 4123.0480002

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Amendment and Reply Under 37 C.F.R. § 1.111; and
2. Request to Retrieve Electronic Priority Application.

The above-listed documents are filed electronically.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) or credit any overpayment to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
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DJF/M-Y/hsb
Enclosures

14448695_1



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
16/126,947	09/10/2018	2812	1880	4123.0480002	20	3

CONFIRMATION NO. 1077

REPLACEMENT FILING RECEIPT

26111

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005



0000000114132759

Date Mailed: 01/23/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

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Assignment For Published Patent Application

Yangtze Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2018/101308 08/20/2018

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

CHINA 201710774754.6 08/31/2017 Access Code Provided

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 01/22/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/126,947**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND
FABRICATION METHODS THEREOF

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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CERTIFICATE OF AVAILABILITY OF A CERTIFIED PATENT DOCUMENT IN A DIGITAL LIBRARY

The International Bureau certifies that a copy of the patent application indicated below has been available to the WIPO Digital Access Service since the date of availability indicated, and that the patent application has been available to the indicated Office(s) as of the date specified following the relevant Office code:

Document details: Country/Office: CN

Filing date: 31 Aug 2017 (31.08.2017)

Application number: 2017107747546

Date of availability of document: 26 Jun 2019 (26.06.2019)

The following Offices can retrieve this document by using the access code:

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Date of issue of this certificate: 23 Jan 2020 (23.01.2020)

34, chemin des Colombettes
1211 Geneva 20, Switzerland
www.wipo.int



证 明

本证明之附件是向本局提交的下列专利申请文件副本。

申 请 号：201710774754.6

申 请 类 型：发明专利

发 明 创 造 名 称：一种三维存储器阵列的多级接触及其制造方法

申 请 日：2017 年 08 月 31 日

申 请 人：长江存储科技有限责任公司

发明人或设计人：朱继锋、吕震宇、陈俊、胡思平、戴晓望、姚兰、
肖莉红、郑阿曼、鲍琨、杨号号

局长

申长雨

2019 年 06 月 26 日

权利要求书

1、一种三维存储器结构制备方法，包括：

第一步，阶梯式结构刻蚀：

提供基底；

在所述基底表面形成堆叠层，所述堆叠层包括多个交错叠加的氧化物层和氮化物层；

然后对堆叠层进行刻蚀，形成阶梯式结构的堆叠层；

第二步，在阶梯式结构的堆叠层上形成阶梯式结构的第二氧化物层：

第三步，在阶梯式结构的第二氧化物层上形成阶梯式结构的终止层；

第四步，在阶梯式结构的终止层上进行填充，形成与阶梯式结构的终止层的最高层等高的第三氧化物层，第三氧化物层形成后，采用化学机械抛光（CMP）工艺使得各台阶层的第三氧化物层的高度与阶梯式结构的终止层的最高层齐平；

第五步，蚀刻阶梯式结构的终止层的最高终止层，形成穿透各层直至接触基底的接触开口，然后将氮化硅层取代为包含绝缘膜 HK 的金属层；

第六步，刻蚀第三氧化物层，进行高选择比的刻蚀，形成达到各阶梯式结构的终止层的接触通道；

第七步，利用反向选择比的刻蚀，进一步刻蚀接触通道，透过各阶梯式结构终止层，得到达到第二氧化物层接触通道；

第八步，进一步刻蚀接触通道，透过第二氧化物层、绝缘膜 HK，得到达到绝缘膜 HK 的金属层的接触通道；

第九步，在前述的步骤中通过刻蚀实现了通孔之后，通过金属填充和研磨实现金属连接结构。

2、权利要求 1 所述的三维存储器结构制备方法，所述终止层是氮化硅。

3、权利要求 1 所述的三维存储器结构制备方法，所述绝缘膜 HK 的金属层包括钨。

4、权利要求 1 或 3 所述的三维存储器结构制备方法，所述绝缘膜 HK 为氧化钪膜、氧化锆膜、氧化铝膜、氧化钽膜或者氧化镧膜。

5、一种三维存储器结构，其由权利要求 1-3 任一所述方法制备得到。

6、一种三维存储器结构，包括：



权利要求书

基底 01;

堆叠层, 呈阶梯式结构, 形成在所述基底 01 表面, 所述堆叠层包括多个交错叠加的第一氧化物层 02 和包含绝缘膜 HK 的金属层;

第二氧化物层 04, 呈阶梯式结构, 位于阶梯式结构的堆叠层上;

终止层 05, 呈阶梯式结构, 位于阶梯式结构的第二氧化物层 04 上;

第三氧化物层 06, 形成在终止层 05 上; 第三氧化物层 06 与阶梯式结构的终止层的最高层 08 齐平;

接触通道, 形成在相邻的第三氧化物层 06 之间, 透过第二氧化物层 04、绝缘膜 HK, 达到绝缘膜 HK 的金属层的接触通道 11;

接触开口 07, 位于阶梯式结构的终止层的最高终止层 08 上, 并穿透各层直至接触基底。

7、权利要求 6 所述的三维存储器结构, 所述终止层是氮化物。

8、权利要求 6 或 7 所述的三维存储器结构, 所述绝缘膜 HK 的金属层包括钨。

9、权利要求 6 或 8 所述的三维存储器结构, 所述绝缘膜 HK 为氧化钪膜、氧化锆膜、氧化铝膜、氧化钽膜或者氧化镧膜。

权利要求书

1、一种三维存储器结构制备方法，包括：

第一步，阶梯式结构刻蚀：

提供基底；

在所述基底表面形成堆叠层，所述堆叠层包括多个交错叠加的氧化物层和氮化物层；

然后对堆叠层进行刻蚀，形成阶梯式结构的堆叠层；

第二步，在阶梯式结构的堆叠层上形成阶梯式结构的第二氧化物层：

第三步，在阶梯式结构的第二氧化物层上形成阶梯式结构的终止层；

第四步，在阶梯式结构的终止层上进行填充，形成与阶梯式结构的终止层的最高层等高的第三氧化物层，第三氧化物层形成后，采用化学机械抛光（CMP）工艺使得各台阶层的第三氧化物层的高度与阶梯式结构的终止层的最高层齐平；

第五步，蚀刻阶梯式结构的终止层的最高终止层，形成穿透各层直至接触基底的接触开口，然后将氮化硅层取代为包含绝缘膜 HK 的金属层；

第六步，刻蚀第三氧化物层，进行高选择比的刻蚀，形成达到各阶梯式结构的终止层的接触通道；

第七步，利用反向选择比的刻蚀，进一步刻蚀接触通道，透过各阶梯式结构终止层，得到达到第二氧化物层接触通道；

第八步，进一步刻蚀接触通道，透过第二氧化物层、绝缘膜 HK，得到达到绝缘膜 HK 的金属层的接触通道；

第九步，在前述的步骤中通过刻蚀实现了通孔之后，通过金属填充和研磨实现金属连接结构。

2、权利要求 1 所述的三维存储器结构制备方法，所述终止层是氮化硅。

3、权利要求 1 所述的三维存储器结构制备方法，所述绝缘膜 HK 的金属层包括钨。

4、权利要求 1 或 3 所述的三维存储器结构制备方法，所述绝缘膜 HK 为氧化钪膜、氧化锆膜、氧化铝膜、氧化钽膜或者氧化镧膜。

5、一种三维存储器结构，其由权利要求 1-3 任一所述方法制备得到。

6、一种三维存储器结构，其由权利要求 1-3 任一所述方法制备得到，该结



权利要求书

构包括：

基底（01）；

堆叠层，呈阶梯式结构，形成在所述基底（01）表面，所述堆叠层包括多个交错叠加的第一氧化物层（02）和包含绝缘膜 HK 的金属层；

第二氧化物层（04），呈阶梯式结构，位于阶梯式结构的堆叠层上；

终止层（05），呈阶梯式结构，位于阶梯式结构的第二氧化物层（04）上；

第三氧化物层（06），形成在终止层（05）上；第三氧化物层（06）与阶梯式结构的终止层的最高层（08）齐平；

接触通道，形成在相邻的第三氧化物层（06）之间，透过第二氧化物层（04）、绝缘膜 HK，达到绝缘膜 HK 的金属层的接触通道（11）；

接触开口（07），位于阶梯式结构的终止层的最高终止层（08）上，并穿透各层直至接触基底。

7、权利要求 6 所述的三维存储器结构，所述终止层是氮化物。

8、权利要求 6 或 7 所述的三维存储器结构，所述绝缘膜 HK 的金属层包括钨。

9、权利要求 6 所述的三维存储器结构，所述绝缘膜 HK 为氧化铅膜、氧化锆膜、氧化铝膜、氧化钽膜或者氧化镧膜。

说明书

一种三维存储器阵列的多级接触及其制造方法

技术领域

本发明涉及半导体装置领域，特别涉及三维存储阵列的多接触及其制造方法。

背景技术

现有技术制造例如单片 3D 阵列的多级存储器阵列的接触的方法。多级存储器装置包括至少一个装置区域和至少一个接触区域，存储器单元(例如垂直 NAND 串)位于该至少一个装置区域，多级接触位于该至少一个接触区域。多级垂直 NAND 存储器阵列的控制栅的远端以台阶式构造布置。以此方式，通过从存储器阵列的上表面向下至台阶蚀刻在四周的介电层中的开口的阵列以及在该开口中沉积接触金属以接触该台阶，可以实现到单独控制栅极的电接触。在制作多级存储器阵列的控制栅级的接触的常规方法中，当采用一层光罩工艺时，由于采用通过一种类型的刻蚀剂一刻到底的方式，实际刻蚀过程中由于台阶高低不同引起的不同位置刻蚀深度难于控制造成刻蚀不足或过刻蚀的问题出现。通常需要两层或三层光罩才能完成工艺目标。因此，现有三维存储器 NAND 工艺通过多层光罩实现接触结构的制作，使得工艺复杂，成本高。

发明内容

本发明的目的就是要提供一种三维存储器阵列的多级接触及其制造方法，可以通过结构的调整，只需要一层光罩就可以在 3D NAND 技术中实现接触结构的制备。通过在阶梯型硅/衬底结构上方放置用于选择比过渡的终止层，在刻蚀的过程中首先利用具有高选择比的刻蚀工艺，使接触通道停止在终止层上，再利用反向选择比的刻蚀工艺去掉终止层，最终实现均匀的打开台阶型硅/衬底上方的接触通道的目的。

本发明采用了一个刻蚀终止层，由于该终止层与其相邻的层在刻蚀工艺中对刻蚀剂的刻蚀效果有截然不同的结果，因此，可以通过不同刻蚀选择比的刻蚀剂的选择，实现第一次刻蚀精准的停留在刻蚀停止层，然后再利用第二次刻

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蚀实现接触通孔准确的停留在金属层上，相比于原来的只是通过一种类型的刻蚀剂一刻到底的方式，由于台阶高低不同引起的不同位置刻蚀深度难于控制产生刻蚀不足或过刻蚀的问题，提高了刻蚀精度。

本发明的目的是通过以下技术方案实现的。

通过在阶梯型硅/衬底结构上方放置用于选择比过渡的终止层，在刻蚀的过程中首先利用具有高选择比的刻蚀工艺，使接触通道停止在终止层上，再利用反向选择比的刻蚀工艺去掉终止层，最终实现均匀的打开台阶型硅/衬底上方的接触通道的目的。

一种三维存储器结构制备方法，包括：

第一步，阶梯式结构刻蚀：

提供基底；

在所述基底表面形成堆叠层，所述堆叠层包括多个交错叠加的氧化物层和氮化物层；

然后对堆叠层进行刻蚀，形成阶梯式结构的堆叠层；

第二步，在阶梯式结构的堆叠层上形成阶梯式结构的第二氧化物层；

第三步，在阶梯式结构的第二氧化物层上形成阶梯式结构的终止层；

第四步，在阶梯式结构的终止层上进行填充，形成与阶梯式结构的终止层的最高层等高的第三氧化物层，第三氧化物层形成后，采用化学机械抛光（CMP）工艺使得各台阶层的第三氧化物层的高度与阶梯式结构的终止层的最高层齐平；

第五步，蚀刻阶梯式结构的终止层的最高终止层，形成穿透各层直至接触基底的接触开口，然后将氮化硅层取代为包含绝缘膜 HK 的金属层；

第六步，刻蚀第三氧化物层，进行高选择比的刻蚀，形成达到各阶梯式结构的终止层的接触通道；

第七步，利用反向选择比的刻蚀，进一步刻蚀接触通道，透过各阶梯式结构终止层，得到达到第二氧化物层接触通道；

第八步，进一步刻蚀接触通道，透过第二氧化物层、绝缘膜 HK，得到达到绝缘膜 HK 的金属层的接触通道；

第九步，在前述的步骤中通过刻蚀实现了通孔之后，通过金属填充和研磨实

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现金属连接结构。

优选地，所述终止层是氮化硅。

优选地，所述绝缘膜 HK 的金属层包括钨。

优选地，所述绝缘膜 HK 为氧化钪膜、氧化锆膜、氧化铝膜、氧化钽膜或者氧化镧膜。

一种三维存储器结构，其由上述任一所述方法制备得到。

一种三维存储器结构，包括：

基底 01；

堆叠层，呈阶梯式结构，形成在所述基底 01 表面，所述堆叠层包括多个交错叠加的第一氧化物层 02 和包含绝缘膜 HK 的金属层；

第二氧化物层 04，呈阶梯式结构，位于阶梯式结构的堆叠层上；

终止层 05，呈阶梯式结构，位于阶梯式结构的第二氧化物层 04 上；

第三氧化物层 06，形成在终止层 05 上；第三氧化物层 06 与阶梯式结构的终止层的最高层 08 齐平；

接触通道，形成在相邻的第三氧化物层 06 之间，透过第二氧化物层 04、绝缘膜 HK，达到绝缘膜 HK 的金属层的接触通道 11；

接触开口 07，位于阶梯式结构的终止层的最高终止层 08 上，并穿透各层直至接触基底。

优选地，所述终止层是氮化物。

优选地，所述绝缘膜 HK 的金属层包括钨。

优选地，所述绝缘膜 HK 为氧化钪膜、氧化锆膜、氧化铝膜、氧化钽膜或者氧化镧膜。

本发明的优点或有益效果在于：通过本发明提供的上述工艺，将原来的一步刻蚀变为两步刻蚀，利用的是刻蚀停止层的设置，原理是利用的停止层对于不同的刻蚀剂有不同的刻蚀效果来实现，避免了现有技术中采用一层光罩进行刻蚀的过程中产生的刻蚀不足或过刻蚀的情况，采用这种新的工艺可以节省成本，降低工艺复杂度，扩大工艺窗口。

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附图说明

通过阅读下文优选实施方式的详细描述，各种其他的优点和益处对于本领域普通技术人员将变得清楚明了。附图仅用于示出优选实施方式的目的，而并不认为是对本发明的限制。而且在整个附图中，用相同的参考符号表示相同的部件。在附图中：

图 1 示出了本发明背景技术中采用三层光罩工艺获得的三维半岛器存储器结构；

图 2 示出了本发明背景技术中采用一层光罩工艺获得的具有缺陷的三维半岛器存储器结构；

图 3-10 示出了本发明实施例的用于三维存储器的结构制备工艺流程结构示意图。

具体实施方式

下面将参照附图更详细地描述本公开的示例性实施方式。虽然附图中显示了本公开的示例性实施方式，然而应当理解，可以以各种形式实现本公开而不应被这里阐述的实施方式所限制。相反，提供这些实施方式是为了能够更透彻地理解本公开，并且能够将本公开的范围完整的传达给本领域的技术人员。

参考图 3-10 所示，本发明实施例提供一种三维存储器的结构制备工艺，包括以下步骤：

一种三维存储器结构制备方法，包括：

第一步，阶梯式结构刻蚀：

提供基底 01；

在所述基底 01 表面形成堆叠层，所述堆叠层包括多个交错叠加的第一氧化物层 02 和氮化硅层 03；

然后对堆叠层进行刻蚀，形成阶梯式结构的堆叠层；

第二步，在阶梯式结构的堆叠层上形成阶梯式结构的第二氧化物层 04；

第三步，在阶梯式结构的第二氧化物层 04 上形成阶梯式结构的终止层 05；

第四步，在阶梯式结构的终止层上进行填充，形成与阶梯式结构的终止层的最高层等高的第三氧化物层 06，第三氧化物层 06 形成后，采用化学机械抛

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光 (CMP) 工艺使得各台阶层的第三氧化物层 06 的高度与阶梯式结构的终止层的最高层齐平;

第五步, 蚀刻阶梯式结构的终止层的最高终止层 08, 形成穿透各层直至接触基底的接触开口 07, 然后将氮化硅层 03 取代为包含绝缘膜 HK 的金属层;

绝缘膜 HK 是具有比氧化物和氮化硅中的每一个更高的介电常数(电容率)的绝缘材料的膜、即所谓高 k 膜(高介电常数膜)。在本申请中, 高 k 膜或者高介电常数膜是指具有高于氮化硅的介电常数(电容率)的膜。

可以使用金属氧化物膜作为绝缘膜 HK, 金属氧化物膜比如氧化铪膜、氧化锆膜、氧化铝膜、氧化钽膜或者氧化镧膜。这样的金属氧化物膜还可以包含氮(N)和硅(Si)中的一个或者二者。可以例如通过原子层沉积(ALD)工艺形成绝缘膜 HK。绝缘膜 HK 具有例如 3nm 的厚度。在高介电常数膜(这里为绝缘膜 HK)用作栅极绝缘膜时, 与使用氧化物膜的情况比较可以增加栅极绝缘膜的物理厚度; 因此, 可以减少漏电流。

第六步, 刻蚀第三氧化物层 06, 进行高选择比的刻蚀, 形成达到各阶梯式结构的终止层的接触通道 09;

第七步, 利用反向选择比的刻蚀, 进一步刻蚀接触通道, 透过各阶梯式结构终止层 05, 得到达到第二氧化物层 04 接触通道;

第八步, 进一步刻蚀接触通道, 透过第二氧化物层 04、绝缘膜 HK, 得到达到绝缘膜 HK 的金属层的接触通道 11;

第九步, 金属填充和研磨的步骤, 即在前述的步骤中通过刻蚀实现了通孔之后, 通过金属填充和研磨等方式实现金属连接结构。

本发明提供一种三维存储器结构, 其由前述制备方法制备得到。

优选, 所述终止层是氮化硅。

优选, 所述绝缘膜 HK 为氧化铪膜、氧化锆膜、氧化铝膜、氧化钽膜或者氧化镧膜。

一种三维存储器结构, 包括:

基底 01;

堆叠层, 呈阶梯式结构, 形成在所述基底 01 表面, 所述堆叠层包括多个交错叠加的第一氧化物层 02 和包含绝缘膜 HK 的金属层;



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第二氧化物层 04，呈阶梯式结构，位于阶梯式结构的堆叠层上；

终止层 05，呈阶梯式结构，位于阶梯式结构的第二氧化物层 04 上；

第三氧化物层 06，形成在终止层 05 上；第三氧化物层 06 与阶梯式结构的终止层的最高层 08 齐平；

接触通道，形成在相邻的第三氧化物层 06 之间，透过第二氧化物层 04、绝缘膜 HK，达到绝缘膜 HK 的金属层的接触通道 11；

接触开口 07，位于阶梯式结构的终止层的最高终止层 08 上，并穿透各层直至接触基底。

优选，所述终止层是氮化硅。

优选，所述绝缘膜 HK 为氧化铅膜、氧化锆膜、氧化铝膜、氧化钽膜或者氧化镧膜。

以上所述，仅为本发明较佳的具体实施方式，但本发明的保护范围并不局限于此，任何熟悉本技术领域的技术人员在本发明揭露的技术范围内，可轻易想到的变化或替换，都应涵盖在本发明的保护范围之内。因此，本发明的保护范围应以所述权利要求的保护范围为准。



说明书附图

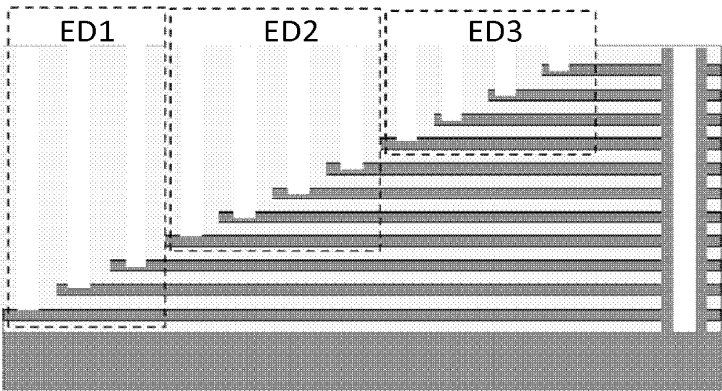


图 1

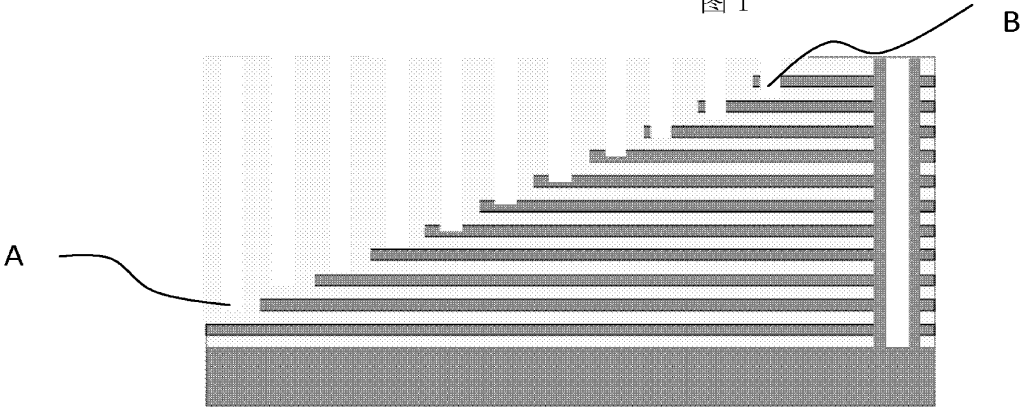


图 2

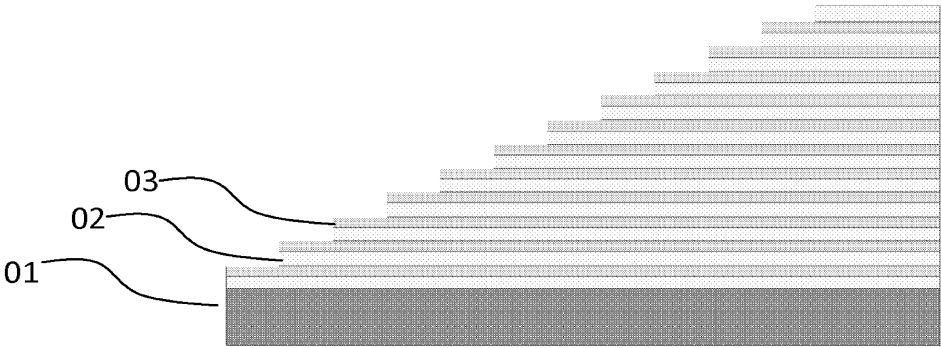


图 3



说明书附图

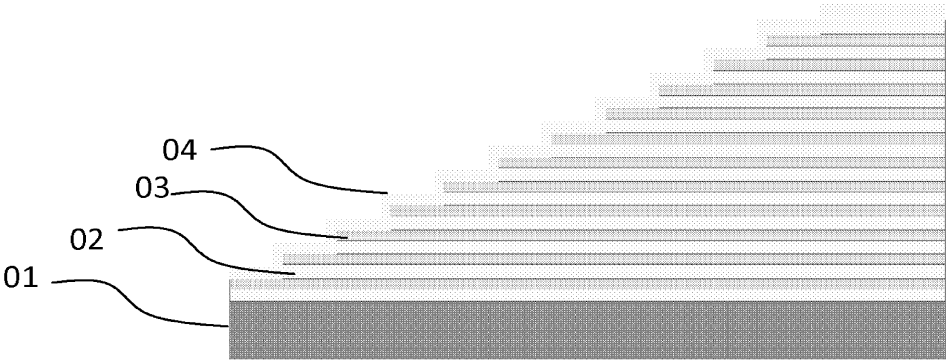


图 4

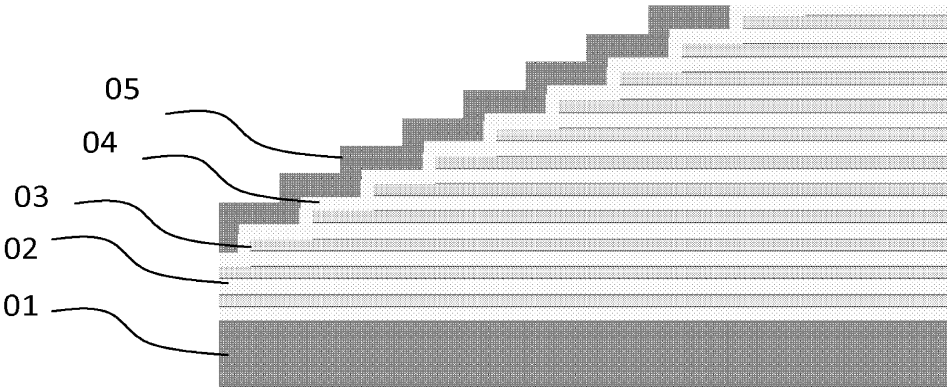


图 5



说明书附图

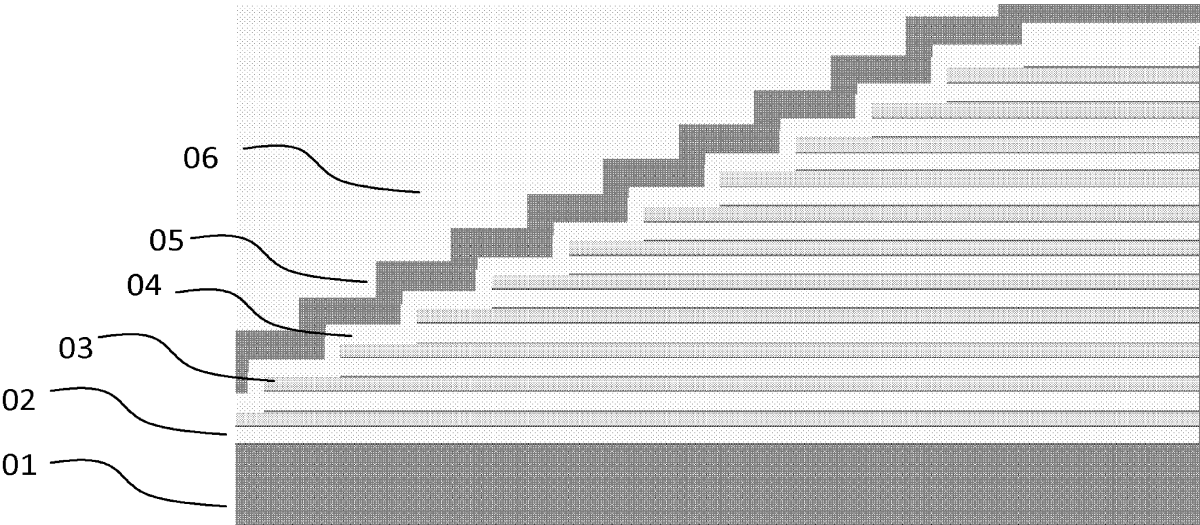


图 6

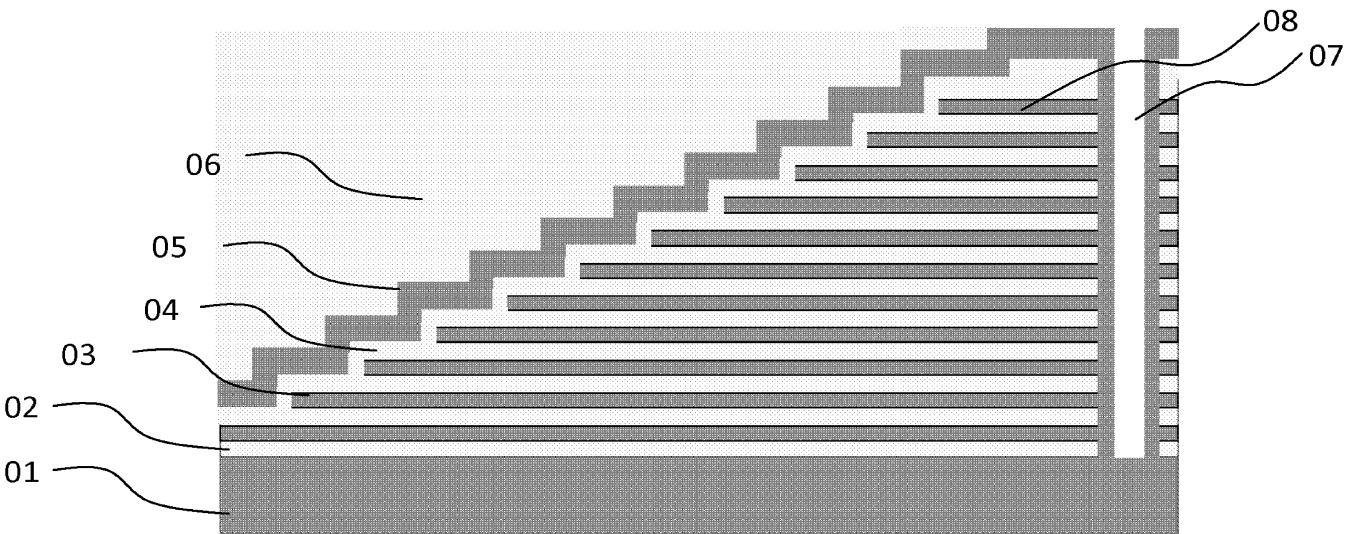


图 7



说明书附图

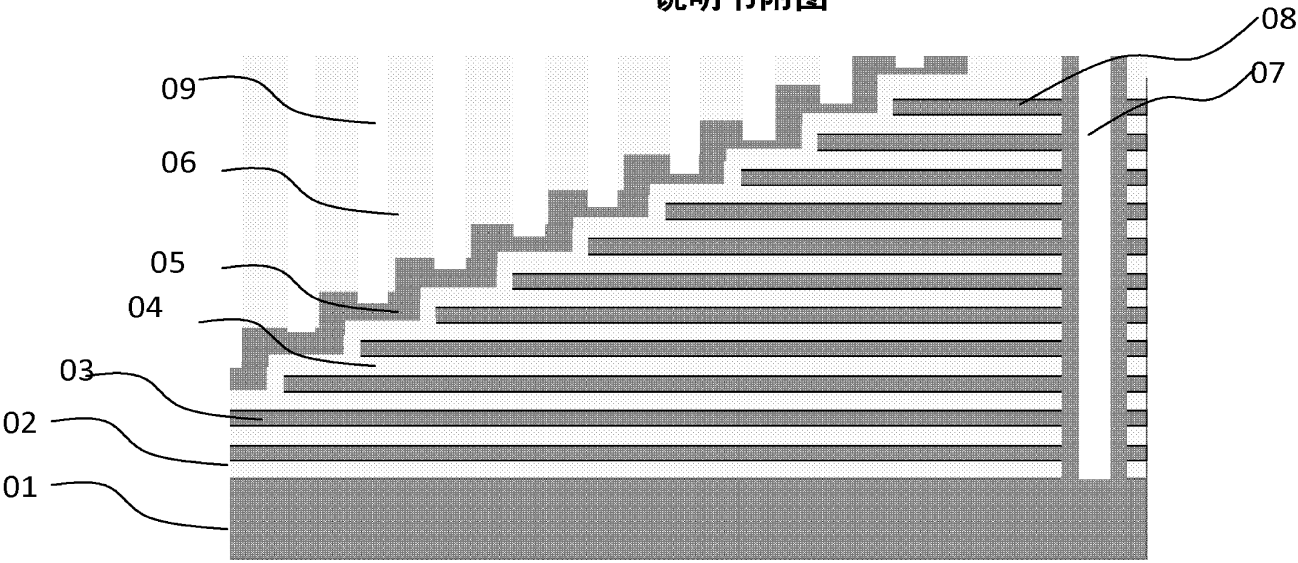


图 8

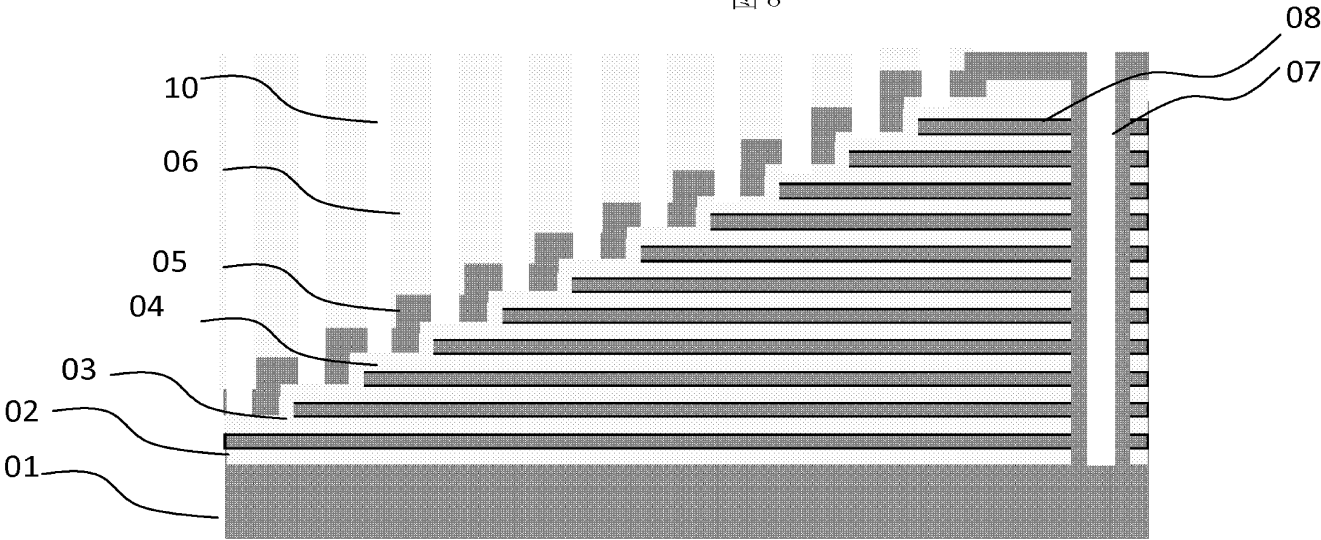


图 9



说明书附图

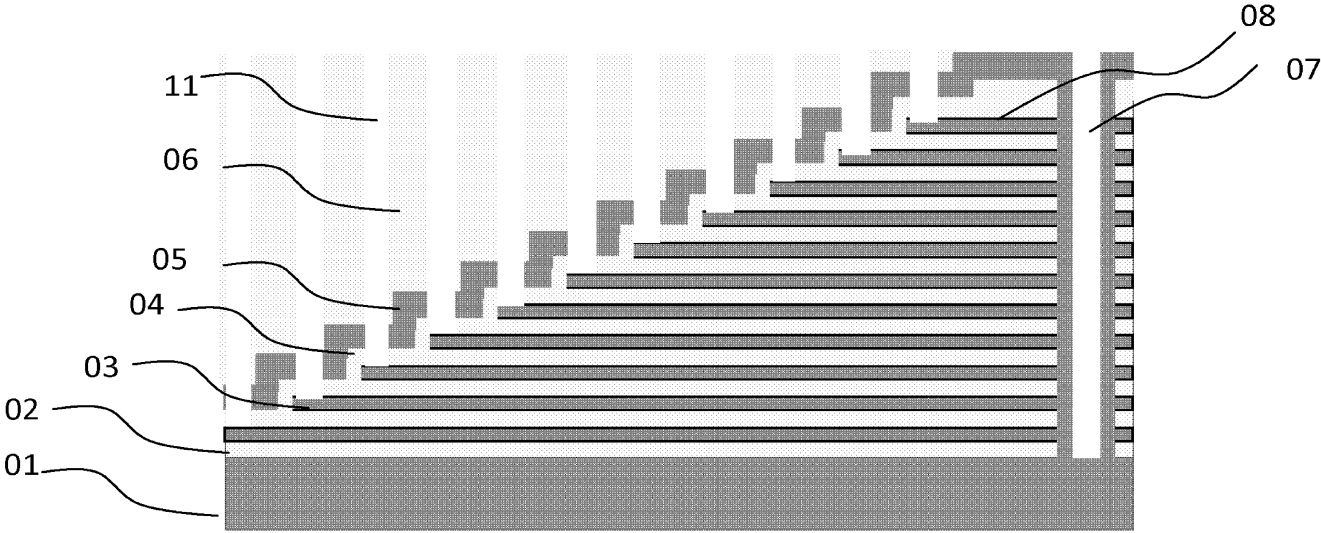


图 10



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

26111 7590 02/03/2020
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER

GEYER, SCOTT B

ART UNIT

PAPER NUMBER

2812

DATE MAILED: 02/03/2020

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/126,947	09/10/2018	Jifeng ZHU	4123.0480002	1077

TITLE OF INVENTION: WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	05/04/2020

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980.

It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26111 7590 02/03/2020
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/126,947	09/10/2018	Jifeng ZHU	4123.0480002	1077

TITLE OF INVENTION: WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	05/04/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
GEYER, SCOTT B	2812	257-751000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/126,947	09/10/2018	Jifeng ZHU	4123.0480002	1077
26111	7590	02/03/2020	EXAMINER	
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.			GEYER, SCOTT B	
1100 NEW YORK AVENUE, N.W.			ART UNIT	
WASHINGTON, DC 20005			PAPER NUMBER	

2812

DATE MAILED: 02/03/2020

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b) (2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/126,947	Applicant(s) ZHU et al.	
	Examiner Scott B Geyer	Art Unit 2812	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to papers filed on January 23, 2020.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-15 and 21-24. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:
a) ☒ All b) ☐ Some *c) ☐ None of the:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 20191112. 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	5. ☐ Examiner's Amendment/Comment 6. ☐ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
---	---

<i>Search Notes</i> 	Application/Control No. 16/126,947	Applicant(s)/Patent Under Reexamination ZHU et al.
	Examiner Scott B Geyer	Art Unit 2812

CPC - Searched*		
Symbol	Date	Examiner
H01L27/115-11597	10/18/2019	SBG

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST search notes attached	10/18/2019	SBG
EAST search updated	01/29/2020	SBG

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	Interference Search	01/29/2020	SBG

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Issue Classification 	Application/Control No. 16/126,947	Applicant(s)/Patent Under Reexamination ZHU et al.
	Examiner Scott B Geyer	Art Unit 2812

CPC						
Symbol					Type	Version
H01L	/	23	/	535	F	2013-01-01
H01L	/	27	/	11551	I	2013-01-01
H01L	/	21	/	76895	I	2013-01-01
H01L	/	27	/	11529	I	2013-01-01
H01L	/	27	/	11573	I	2013-01-01
H01L	/	27	/	11578	I	2013-01-01
H01L	/	27	/	11582	I	2013-01-01
H01L	/	27	/	1157	I	2013-01-01
H01L	/	27	/	11575	I	2013-01-01

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version
/		/		

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	19	
/SCOTT B GEYER/ Primary Examiner, Art Unit 2812	29 January 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5B, 9A

U.S. Patent and Trademark Office

Part of Paper No.: 20200129

Issue Classification 	Application/Control No. 16/126,947	Applicant(s)/Patent Under Reexamination ZHU et al.
	Examiner Scott B Geyer	Art Unit 2812

INTERNATIONAL CLASSIFICATION			
CLAIMED			
H01L		23	535
NON-CLAIMED			

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	19	
/SCOTT B GEYER/ Primary Examiner, Art Unit 2812	29 January 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5B, 9A

U.S. Patent and Trademark Office

Part of Paper No.: 20200129

Issue Classification 	Application/Control No. 16/126,947	Applicant(s)/Patent Under Reexamination ZHU et al.
	Examiner Scott B Geyer	Art Unit 2812

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	10	10		19										
2	2	13	11		20										
3	3	14	12	11	21										
4	4	15	13	12	22										
5	5	16	14	18	23										
6	6	17	15	19	24										
7	7		16												
8	8		17												
9	9		18												

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	19	
/SCOTT B GEYER/ Primary Examiner, Art Unit 2812	29 January 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5B, 9A

U.S. Patent and Trademark Office

Part of Paper No.: 20200129

Receipt date: 11/12/2019

PTO/SB/08a (07-09)

Approved for use through 11/30/2020, OMB 0651-0031

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO				Complete if Known <table border="1"> <tr> <td>Application Number</td> <td>16/126,947</td> </tr> <tr> <td>Filing Date</td> <td>09-10-2018</td> </tr> <tr> <td>First Named Inventor</td> <td>Jifeng ZHU</td> </tr> <tr> <td>Art Unit</td> <td>2812</td> </tr> <tr> <td>Examiner Name</td> <td>Geyer, Scott B</td> </tr> <tr> <td>Attorney Docket Number</td> <td>4123.0480002</td> </tr> </table>		Application Number	16/126,947	Filing Date	09-10-2018	First Named Inventor	Jifeng ZHU	Art Unit	2812	Examiner Name	Geyer, Scott B	Attorney Docket Number	4123.0480002
Application Number	16/126,947																
Filing Date	09-10-2018																
First Named Inventor	Jifeng ZHU																
Art Unit	2812																
Examiner Name	Geyer, Scott B																
Attorney Docket Number	4123.0480002																
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)																	
Sheet	1	of	1														

[illegible][illegible]

Examiner Signature	/SCOTT B GEYER/	Date Considered	01/29/2020
-----------------------	-----------------	--------------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kind Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	2268	(H01L27/115-11597).CPC. and (staircase stair-case stairstep stair-step stair)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/01/29 15:36
L3	465	2 and (etchstop etch-stop (etch adj stop))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/01/29 15:36
L4	128	2 and (barrier same (etchstop etch-stop (etch adj stop)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/01/29 15:38
L5	117	4 not ("2020" "2019").ay.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/01/29 15:38
L6	2	((("20140106569") or ("20170236836")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/01/29 15:41
L7	2	((("20130313627") or ("9515086")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/01/29 16:19
S1	49	((Yangtze adj Technologies).as. (Jifeng with ZHU).in. (Zhenyu with LU).in. (Jun with CHEN).in. (Si with HU).in. (Xiaowang with DAI).in. (Lan with YAO).in. (Li with XIAO).in. (Man with ZHENG).in. (Kun with BAO).in. (Haohao with YANG).in.) and (staircase stair-case (stair adj case))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/16 16:46
S2	4	((("20100013049") or ("20110169071") or ("20130337646") or ("20140284675")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/16 16:48
S3	4	((("20130313627") or ("20160118398") or ("8828884") or ("9515086")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/16 16:49
S4	38937	(H01L23/535 H01L21/76895 H01L27/11529 H01L27/11551 H01L27/1157 H01L27/11573	US-PGPUB; USPAT; USOCR;	OR	OFF	2019/10/16 16:51

		H01L27/11575 H01L27/11578 H01L27/11582).CPC.	FPRS; EPO; JPO; DERWENT; IBM_TDB			
S5	29035	(H01L27/115).CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/18 09:47
S6	83	(H01L27/115).CPC. and (staircase stair- case (stair adj case))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/18 09:48
S7	1105	(H01L27/115-11597).CPC. and (staircase stair-case (stair adj case))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/18 09:48
S8	600	(H01L27/115-11597).CPC. and (stairstep stair-step (stair adj step))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/18 09:49
S9	1609	S7 or S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/18 09:49
S10	302	S9 and (etchstop etch-stop (etch adj stop))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/18 09:49
S11	1	("20130313627").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/18 09:50
S12	1	(13/478483).APP.	USPAT; USOCR	OR	OFF	2019/10/18 09:50
S13	50	("20030011017" "20070210338" "20070252201" "20100013049" "20100044778" "20100112769" "20100120214" "20100155810" "20100155818" "20100181610" "20100207195" "20100320528" "20110031546" "20110076819" "20110133606" "20110169071" "20110266606" "20110284943" "20120001247" "20120001249"	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/18 09:50

		"20120001250" "7005350" "7023739" "7177191" "7221588" "7233522" "7514321" "7575973" "7745265" "7808038" "7848145" "7851851" "8008710" "8053829").PN. OR ("8828884").URPN.				
S15	1122	(H01L27/115-11597).CPC. and (staircase stair-case (stair adj case))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/18 12:16
S16	35	(H01L27/115-11597).CPC. and (stairway stair-way (stair adj way))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/18 12:16
S17	647	(H01L27/115-11597).CPC. and (stairstep stair-step (stair adj step))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/18 12:16
S18	451	(H01L27/115-11597).CPC. and (stair with stack\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/18 12:16
S19	1894	S15 or S16 or S17 or S18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/18 12:17
S21	358	S19 and (etchstop etch-stop (etch adj stop))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/18 12:17
S22	1	(12/727708).APP.	USPAT; USOCR	OR	OFF	2019/10/18 12:23
S23	22	("20070252201" "20090140234" "7381640" "7539056" "8278695" "8314455").PN. OR ("8581323").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/18 12:23
S24	1	(14/989144).APP.	USPAT; USOCR	OR	OFF	2019/10/18 14:08
S25	0	("9570393").URPN.	USPAT	OR	OFF	2019/10/18 14:08
S26	3392	(H01L27/115-11597).CPC. and (H01L23/528 H01L23/5283).CPC.	US-PGPUB; USPAT; USOCR;	OR	OFF	2019/10/18 14:10

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S27	398	S26 and (etchstop etch-stop (etch adj stop))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/18 14:11
S28	69	S27 and (staircase stair-case (stair adj case))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/18 14:14
S29	2	S27 and (stairway stair-way (stair adj way))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/18 14:14
S30	8	S27 and (stairstep stair-step (stair adj step))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/18 14:14
S31	74	S28 or S29 or S30	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/18 14:14
S32	2	((("20160358855") or ("20160020169")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/18 14:20
S35	1	("20160020169").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/18 15:40
S37	1	S35 and plug	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/18 15:40
S38	1957	(etchstop etch-stop (etch adj stop)) with (nitride SiN) with thickness	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/18 16:13
S39	318	(H01L27/115-11597).CPC. and ((stopper	US-PGPUB;	OR	ON	2019/10/18

		etchstop etch-stop (etch adj stop)) with (nitride SiN) with thickness)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			16:13
S40	221	S39 and (thickness with nm)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/18 16:13
S41	172	(H01L27/115-11597).CPC. and ((stopper etchstop etch-stop (etch adj stop)) with (nitride SiN) with thickness with nm)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/18 16:14
S43	7	((("20160358855") or ("20160020169") or ("20110169071") or ("20110031546") or ("20100207195") or ("9419013") or ("7539056")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/18 16:30

EAST Search History (I nterference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L8		(staircase stair-case stairstep stair-step stair).clm. and (barrier with (etchstop etch-stop (etch adj stop))).clm.	US-PGPUB; USPAT	OR	ON	2020/01/29 16:20
L9		(staircase stair-case stairstep stair-step stair).clm. and barrier.clm. and (etchstop etch-stop (etch adj stop)).clm.	US-PGPUB; USPAT	OR	ON	2020/01/29 16:21
L10		9 and ((high adj k).clm. or (high-k).clm.)	US-PGPUB; USPAT	OR	ON	2020/01/29 16:21

1/ 29/ 2020 4:23:09 PM

C:\Users\sgeyer\Documents\EAST\Workspaces\16 126947.wsp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: ZHU *et al.*

Confirmation No.: 1077

Applicant: Yangtze Memory Technologies
CO., LTD.

Art Unit: 2812

Application No.: 16/126,947

Examiner: Geyer, Scott B.

Filing Date: September 10, 2018

Atty. Docket: 4123.0480002

Title: **WORD LINE CONTACT STRUCTURE OF THREE-DIMENSIONAL MEMORY
DEVICES AND FABRICATION METHODS THEREOF**

Request for Corrected Official Filing Receipt

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

Applicant hereby requests that a corrected Official Filing Receipt be issued and sent to the undersigned representative. Specifically, the following corrections to the Official Filing Receipt are requested:

In the Applicant(s):

Please correct "Yangtze Technologies Co., Ltd." to --Yangtze Memory Technologies
Co., Ltd.--.

Assignment For Published Patent Application:

Please correct "Yangtze Technologies Co., Ltd." to --Yangtze Memory Technologies
Co., Ltd.--.

In support of the above request, a marked-up copy of the instant Official Filing Receipt is enclosed to show the corrections. It is requested that a corrected Official Filing Receipt be issued, and sent to the undersigned at the earliest possible time.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 2/12/2020

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14556694_1.docx



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
16/126,947	09/10/2018	2812	1880	4123.0480002	20	3

CONFIRMATION NO. 1077

REPLACEMENT FILING RECEIPT

26111

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005



0000000114132759

Date Mailed: 01/23/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

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Inventor(s)

Jifeng ZHU, Wuhan, CHINA;
Zhenyu LU, Wuhan, CHINA;
Jun CHEN, Wuhan, CHINA;
Si Ping HU, Wuhan, CHINA;
Xiaowang DAI, Wuhan, CHINA;
Lan YAO, Wuhan, CHINA;
Li Hong XIAO, Wuhan, CHINA;
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Kun BAO, Wuhan, CHINA;
Haohao YANG, Wuhan, CHINA;

Applicant(s)

Yangtze Memory Technologies Co., Ltd.
~~Yangtze Technologies Co., Ltd.~~, Wuhan, CHINA

Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd.
~~Yangtze Technologies Co., Ltd.~~, Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2018/101308 08/20/2018

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

CHINA 201710774754.6 08/31/2017 Access Code Provided

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

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Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 01/22/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/126,947**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND
FABRICATION METHODS THEREOF

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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Electronic Acknowledgement Receipt	
EFS ID:	38575570
Application Number:	16126947
International Application Number:	
Confirmation Number:	1077
Title of Invention:	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF
First Named Inventor/Applicant Name:	Jifeng ZHU
Customer Number:	26111
Filer:	Donald J. Featherstone/Julia Vang
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0480002
Receipt Date:	13-FEB-2020
Filing Date:	10-SEP-2018
Time Stamp:	15:32:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2020-02-12-Filing-Bundle-4123-0480002.pdf	4574965	yes	7
			7d1c19e3125dc3ae706af2954bf427564fc33f06		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Miscellaneous Incoming Letter	1	1
	Request for Corrected Filing Receipt	2	7
Warnings:			
Information:			
Total Files Size (in bytes):		4574965	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

DONALD J. FEATHERSTONE
DIRECTOR
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DONF@STERNEKESSLER.COM

February 12, 2020

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 1077
Art Unit 2812

Re: U.S. Utility Patent Application
Appl. No. 16/126,947; Filing Date: September 10, 2018
For: **WORD LINE CONTACT STRUCTURE OF THREE-
DIMENSIONAL MEMORY DEVICES AND FABRICATION
METHODS THEREOF**
Inventors: ZHU *et al.*
Our Ref: 4123.0480002

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Request for Corrected Official Filing Receipt

The above-listed documents are filed electronically.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) or credit any overpayment to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/M-Y/jcv
Enclosure

Sterne, Kessler, Goldstein & Fox P.L.L.C. | 1100 New York Avenue, NW | Washington, D.C. 20005
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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
16/126,947	09/10/2018	2812	1880	4123.0480002	20	3

CONFIRMATION NO. 1077

CORRECTED FILING RECEIPT

26111

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005



0000000114790389

Date Mailed: 02/19/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

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Inventor(s)

Jifeng ZHU, Wuhan, CHINA;
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Jun CHEN, Wuhan, CHINA;
Si Ping HU, Wuhan, CHINA;
Xiaowang DAI, Wuhan, CHINA;
Lan YAO, Wuhan, CHINA;
Li Hong XIAO, Wuhan, CHINA;
A Man ZHENG, Wuhan, CHINA;
Kun BAO, Wuhan, CHINA;
Haohao YANG, Wuhan, CHINA;

Applicant(s)

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2018/101308 08/20/2018

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

CHINA 201710774754.6 08/31/2017 Access Code Provided

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Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 01/22/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/126,947**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND
FABRICATION METHODS THEREOF

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

April 28, 2020

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 1077
Art Unit 2812
Attn: Mail Stop Issue Fee

Re: U.S. Utility Patent Application
Appl. No. 16/126,947; Filing Date: September 10, 2018
For: **WORD LINE CONTACT STRUCTURE OF THREE-
DIMENSIONAL MEMORY DEVICES AND FABRICATION
METHODS THEREOF**
Inventors: ZHU *et al.*
Our Ref: 4123.0480002

Commissioner:

In response to the **Notice of Allowance and Fee(s) Due** dated February 3, 2020, the following documents are transmitted for appropriate action by the U.S. Patent and Trademark Office:

1. Online Credit Card Payment Authorization in the amount of \$1,000.00 to cover:
\$1,000.00 – Issue Fee;

2. Issue Fee Transmittal

The above-listed documents are filed electronically.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) or credit any overpayment to our Deposit Account No. 19-0036.

Commissioner for Patents
April 28, 2020
Page 2

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/M-Y/jcv
Enclosures

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26111 7590 02/03/2020
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/126,947	09/10/2018	Jifeng ZHU	4123.0480002	1077

TITLE OF INVENTION: WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	05/04/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
GEYER, SCOTT B	2812	257-751000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Sterne, Kessler,
2 Goldstein & Fox P.L.L.C.
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Yangtze Memory Technologies Co., Ltd.

Wuhan, Hubei, CHINA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 19-0036

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Donald J. Featherstone/

Date 4/28/2020

Typed or printed name Donald J. Featherstone

Registration No. 33,876

Electronic Patent Application Fee Transmittal				
Application Number:		16126947		
Filing Date:		10-Sep-2018		
Title of Invention:		WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF		
First Named Inventor/Applicant Name:		Jifeng ZHU		
Filer:		Donald J. Featherstone/Julia Vang		
Attorney Docket Number:		4123.0480002		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1000

Electronic Acknowledgement Receipt	
EFS ID:	39291119
Application Number:	16126947
International Application Number:	
Confirmation Number:	1077
Title of Invention:	WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF
First Named Inventor/Applicant Name:	Jifeng ZHU
Customer Number:	26111
Filer:	Donald J. Featherstone/Julia Vang
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0480002
Receipt Date:	28-APR-2020
Filing Date:	10-SEP-2018
Time Stamp:	16:59:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1000
RAM confirmation Number	E20204RG59238754
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2020-04-28-Cover-Letter-4123-0480002.pdf	280975	no	2
			52ef319da3e03ad29581dae92cd20ff885ee84dc		
Warnings:					
Information:					
2	Issue Fee Payment (PTO-85B)	Issue-Fee-4123-0480002.PDF	108435	no	1
			a6bc4502efe57e41308a4f1a8ec2c154df30f09c		
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30591	no	2
			c5b314844982909a5f5e98de274de47a1433df09		
Warnings:					
Information:					
Total Files Size (in bytes):			420001		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/126,947	06/02/2020	10672711	4123.0480002	1077

26111 7590 05/13/2020
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Jifeng ZHU, Wuhan, CHINA;
Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA
Zhenyu LU, Wuhan, CHINA;
Jun CHEN, Wuhan, CHINA;
Si Ping HU, Wuhan, CHINA;
Xiaowang DAI, Wuhan, CHINA;
Lan YAO, Wuhan, CHINA;
Li Hong XIAO, Wuhan, CHINA;
A Man ZHENG, Wuhan, CHINA;
Kun BAO, Wuhan, CHINA;
Haohao YANG, Wuhan, CHINA;

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IR103 (Rev. 10/09)

Micron Ex. 1002, p. 270
Micron v. YMTC
IPR2025-00117



ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
16/126,947

RECEIPT DATE / TIME
07/03/2024 02:56:17 PM Z ET

ATTORNEY DOCKET #
4123.0480002

Title of Invention

WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND
FABRICATION METHODS THEREOF

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # 10672711

CONFIRMATION # 1077

FILED BY Hillary White

PATENT CENTER # 66231484

FILING DATE 09/10/2018

CUSTOMER # 26111

FIRST NAMED
INVENTOR Jifeng ZHU

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Mark Zimmerman

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
2017-00285-YMTC-PCT- US_POA.pdf	3	Power of Attorney	402 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
2017-00285-YMTC-PCT- US_POA.pdf	19AE7C8EA070B957110945EAD60D7327E5F89A226D6918B984 73D81068462632EB33D1D346B089FD9BAFD7A1B900F938A65 E9030A0D2B81B33044268120B9C24

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	16126947
Filing Date	September 10, 2018
First Named Inventor	Jifeng ZHU
Title	Word line contact structure for three-dimensional memory devices and fabrication methods thereof
Art Unit	2812
Examiner Name	SCOTT GEYER
Attorney Docket Number	2017-00285-YMTC-PCT-US

SIGNATURE of Applicant or Patent Practitioner

Signature	/Mark C. Zimmerman /	Date (Optional)	July 3, 2024
Name	Mark C. Zimmerman	Registration Number	44006
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	Yangtze Memory Technologies Co., Ltd.		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☐

*Total of _____ forms are submitted.

A Federal agency may not conduct or sponsor, and a person is not required to respond to, nor shall a person be subject to a penalty for failure to comply with an information collection subject to the requirements of the Paperwork Reduction Act of 1995, unless the information collection has a currently valid OMB Control Number. The OMB Control Number for this information collection is 0651-0035. Public burden for this form is estimated to average 3 minutes per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the information collection. Send comments regarding this burden estimate or any other aspect of this information collection, including suggestions for reducing this burden to the Chief Administrative Officer, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or email InformationCollection@uspto.gov. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.** If filing this completed form by mail, send to: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number

Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)



I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

34431

OR



I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:



The address associated with the above-mentioned Customer Number

OR



The address associated with Customer Number:

OR



Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.



Inventor or Joint Inventor (title not required below)



Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)



Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)



Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

Name

Tuenlap Daniel Chan

Title

Deputy General Counsel, Head of Intellectual Property Department

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of

forms are submitted.

A Federal agency may not conduct or sponsor, and a person is not required to respond to, nor shall a person be subject to a penalty for failure to comply with an information collection subject to the requirements of the Paperwork Reduction Act of 1995, unless the information collection has a currently valid OMB Control Number. The OMB Control Number for this information collection is 0651-0035. Public burden for this form is estimated to average 3 minutes per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the information collection. Send comments regarding this burden estimate or any other aspect of this information collection, including suggestions for reducing this burden to the Chief Administrative Officer, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or email InformationCollection@uspto.gov. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.** If filing this completed form by mail, send to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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