

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00117
U.S. Patent No. 10,672,711
Issue Date: June 2, 2020

Title: WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL
MEMORY DEVICES AND FABRICATION METHODS THEREOF

**DECLARATION OF SANJAY BANERJEE, Ph.D., IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 10,672,711**

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I, Sanjay Banerjee, hereby declare as follows:

I. INTRODUCTION

1. My name is Sanjay Banerjee. I have been retained on behalf of Petitioner Micron Technology, Inc. (“Micron”) to provide this Declaration concerning technical subject matter relevant to the *inter partes* review petition (“Petition”) concerning U.S. Patent No. 10,672,711 (Ex. 1001, the “’711 Patent”).

2. In the preparation of this Declaration, I have confined my analysis to the materials and opinions that were available at the time of the preparation of this Declaration. I reserve the right to supplement this Declaration in response to additional evidence that may come to light.

3. If requested, I am prepared to explain (in a deposition or at a trial before the Patent Trial and Appeal Board (the “Board”)) the technology disclosed in the ’711 Patent—including the state of the art in the relevant timeframe. Similarly, I am prepared to explain the technology disclosed in the Kim (Ex. 1005, U.S. Patent Publication No. 2012/0070944A1) and Park (Ex. 1006, Korean Patent No. 10-2015-0051841) references, and in any other prior art references cited herein. This may include, among other things, background information on 3D NAND technology.

4. I am over 18 years of age and competent to testify to the matters addressed in this Declaration.

II. QUALIFICATIONS

5. I currently serve as the Cockrell Family Regents Chair Professor of Electrical and Computer Engineering and Director of the Microelectronics Research Center at the University of Texas at Austin (“UT”). Prior to this position, I was first an Assistant Professor (September 1987-August 1990) and later an Associate Professor (September 1990-August 1993) at UT, before being named a Professor in September 1993. Prior to starting my academic work at UT, I was a member of the technical staff at Texas Instruments (Corporate R&D) from the time I completed my doctoral studies in 1983 until August 1987. I worked on vertical 3D Dynamic Random Access Memory (DRAM) cells (see S. Banerjee and M. Bordelon, “A Model for the Trench Transistor,” IEEE Trans. Elec. Dev., 34 (12), 2485-2493, December 1987).

6. In addition to my academic work at UT, I was also the Director of the South West Academy of Nanoelectronics, one of three centers created by the Semiconductor Research Corporation Nanoelectronics Research Initiative in 2006 to research and develop a replacement for conventional metal oxide semiconductor field effect transistors (“MOSFETs”) during the entire program.

7. I received my Ph.D. in Electrical Engineering from the University of Illinois in 1983. I also received an M.S. in Electrical Engineering from the University of Illinois in 1981. I received a B. Tech. in Electronics from the Indian

Institute of Technology at Kharagpur in 1979.

8. As described in my CV (Ex. 1004), I have more than 40 years of experience in the field of electrical engineering, including extensive experience in semiconductor development and fabrication including that of 3-Dimensional Dynamic Random Access Memory (“DRAM”) cells, MOSFETs, flash memory, and beyond-complementary metal-oxide-semiconductor (“CMOS”) transistors. My work in these fields has resulted in thirty-five United States patents related to methods of forming polysilicon and novel transistors, flash memory, and vertical DRAM cells. I have been elected a Fellow of the National Academy of Inventors.

9. Much of my research and experience has related to methods for MOSFET fabrication and design, including deposition of thin films by chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), patterning using photolithography and etching using plasma-based Reactive Ion Etching (RIE) which are some of the processing techniques used to make 3D NAND flash. I have worked extensively on polysilicon thin film transistors similar to the ones used in the channel of NAND flash memory cells, high-k and other dielectrics used for charge storage, and for tunneling. A number of the sponsored research grants on which I have been a principal or coinvestigator have related to chemical deposition methods and/or ultra-shallow source/drain junction technology, including “Transport in MOSFETs” (Motorola, August 1993-August 1994), “Ultra

Shallow Junction Technology” (SEMATECH January 1994-December 1996), and “Vertical Si-Ge-C MOSFETS” (Semiconductor Research Corporation September 2000-August 2003). In addition, I am an author on over forty publications relating to flash memory cells, including vertical 3D memory that can be used in NAND flash (e.g., Sarkar J, Dey S, Shahrjerdi D, Banerjee SK, “Vertical Flash memory cell with nanocrystal floating gate for ultradense integration and good retention,” IEEE Electron Device Letters 28 (5): 449-451 May 2007.) One of my papers on flash memory was given a Best Paper Award by the SRC.

10. I am a Fellow of the Institute of Electrical and Electronics Engineers (“IEEE”), the American Physical Society (“APS”), and the American Association for the Advancement of Science (“AAAS”). I have served on numerous professional and government committees in the electrical engineering field, including chairing multiple IEEE committees, meetings, and programs, serving on Morgan & Claypool’s editorial board, and serving as a member on the International Technology Roadmap for Semiconductors (“ITRS”).

11. I have taught courses in Semiconductor Physics, Solid State Electronic Devices, and Microelectronic and VLSI Device Fabrication at UT. In addition, I have delivered many courses to industry on Semiconductor Devices and Memory and Semiconductor Processing. I have taught courses that cover 3D memories, such as 3D NAND (Ultra Large Scale Integration Techniques and Solid State Electronic

Devices). As a principal investigator, I have been the advisor to over 80 Doctoral and Masters students.

12. I am the co-author of several books and invited book chapters covering the area of electronic and semiconductor devices, including: Dopant Diffusion, Solid State Electronic Devices (three editions), Silicon-germanium Devices, and Novel 3D CMOS. I have authored or co-authored more than 1,000 papers and presentations in the areas of semiconductor devices and electronics development over the course of my career.

13. I have been the recipient of fifty grants to fund my research from a variety of funding agencies including the National Science Foundation (“NSF”), DARPA, the Department of Energy, Semiconductor Research Corporation, the Department of Defense-Multidisciplinary University Research Initiative, and the Office of Naval Research.

14. I have received numerous awards for my work, including the NSF Presidential Young Investigator Award. The NSF Presidential Young Investigator Award was ¹ a highly competitive honor and grant bestowed annually upon

¹ The NSF Presidential Young Investigator Award was an award given out by the NSF until 1991, at which time it was replaced with the NSF Young Investigator Awards and Presidential Faculty Fellows Program.

recognized young academic leaders in science and engineering. I have received numerous other awards, including some the highest honors for semiconductor devices such as the Andrew Grove Award from the IEEE, and the Semiconductor Industry Association/Semiconductor Research Corporation University Researcher Award, for my work in semiconductor memory and transistors, which are described in more detail in my CV (Ex. 1004).

III. COMPENSATION

15. I am being compensated for my work in this matter at an hourly rate of \$650.00 for consulting services. My compensation is not based on the outcome of this matter or on the substance of my opinions.

IV. MATERIALS CONSIDERED

16. In preparing this declaration, I reviewed and considered the following materials, along with any other materials referenced in the body of my declaration:

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 10,672,711 to Zhu et al. (“the ’711 Patent”)
1002	File History of U.S. Patent No. 10,672,711 (“the ’711 FH”)
1003	Declaration of Dr. Sanjay Banerjee (“Banerjee”)
1004	<i>Curriculum Vitae</i> of Dr. Sanjay Banerjee
1005	U.S. Patent Publication No. 2012/0070944A1 to Kim et al. (“Kim”)

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Declaration of Sanjay Banerjee

EXHIBIT NO.	DESCRIPTION
1006	Korean Patent No. 10-2015-0051841 to Park et al. (“Park”) including certified translation
1007	U.S. Patent Publication No. 2019/0067306A1 to Fang et al. (“Fang”)
1008	U.S. Patent Publication No. 2017/0294384A1 to Chen (“Chen”)
1009	Aritome, “NAND Flash Memory Technologies” (2016)
1010	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1011	Michelsoni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1012	U.S. Patent Publication No. 2017/0117222A1 to Kim et al.
1013	Chang and Sze, “ULSI Technology” (1996)
1014	Orlowski et al., <i>Si, SiGe, Ge, and III-V Semiconductor Nanomembranes and Nanowires Enabled by SiGe Epitaxy</i> , ECS Transactions Vo. 33, No. 6 (2010), 777-89
1015	U.S. Patent No. 9,728,547 to Ohsaki et al.
1016	U.S. Patent Publication No. 2017/0148677A1 to Shin
1017	U.S. Patent Publication No. 2013/0313627A1 to Lee et al.

V. UNDERSTANDING OF THE GOVERNING LAW

17. I am not an attorney but have been instructed in and applied the law as described in this section.

A. Claim Construction

18. I understand that the first step in determining whether a patent claim would have been anticipated or obvious is to ascertain how a person of ordinary skill in the art (“POSITA”) would have understood the claim terms.

19. I have been instructed by counsel on the law regarding claim construction and patent claims, and I understand that a patent may include two types of claims: independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim, or it can further depend from another dependent claim. I understand that a dependent claim includes all the limitations that it recites, in addition to all the limitations recited in the claim(s) from which it depends.

20. It is my understanding that in proceedings before the USPTO, the claims of a patent are to be construed under what is referred to as the “Phillips standard.” I understand that this means that claim terms of a patent are given the ordinary and customary meaning they would have to a POSITA in view of the description provided in the patent itself and the patent’s file history.

21. I understand that to determine how a person of ordinary skill would understand a claim term, one should look to those sources available that show what a person of skill in the art would have understood the disputed claim language to mean. I understand that, in construing a claim term, one looks primarily to the

intrinsic patent evidence, including the words of the claims themselves, the patent specification, and the patent's prosecution history. I understand that extrinsic evidence, which is evidence external to the patent and the prosecution history, may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient.

22. I understand that words or terms should be given their ordinary and accepted meaning unless it clearly appears that the inventors were using them to mean something else. In making this determination, the claims, the remainder of the patent, and the prosecution history are of paramount importance. Additionally, the patent and its prosecution history must be consulted to confirm whether the patentee has acted as its own lexicographer (i.e., provided its own special meaning to any disputed terms) or intentionally disclaimed, disavowed, or surrendered any claim scope.

23. I further understand that in proceedings before the Board, claim terms need only be construed to the extent necessary to resolve any controversy that may arise.

24. In comparing the claims of the '711 Patent to the prior art, I have considered the '711 Patent and its file history in light of the understanding of a POSITA at the time of the alleged invention. I address further how a POSITA would have understood the claims of the alleged invention in §X.

B. Obviousness

25. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious under 35 U.S.C. §103(a) to a person of ordinary skill in the art of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed. I also understand that the Board considers certain objective factors if they are present, generally referred to as “secondary considerations” or “objective indicia” of nonobviousness, as further discussed below in this section.

26. I have been informed that there are two ways to determine whether prior art is analogous and thus can be considered prior art: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the patentee’s endeavor, whether the reference still is reasonably pertinent to the particular problem with which the patentee is involved. I have also been informed that the field of endeavor of a patent is not limited to the specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field. I have also been informed that a reference is

reasonably pertinent if, even though it may be in a different field from that of the patentee's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to a patentee's attention in considering his or her problem.

27. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there generally must have been some reason or motivation for one of ordinary skill in the art to combine the teachings of the prior art references to arrive at the claimed subject matter.

28. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a person of ordinary skill in the art at the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

29. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine, but that other times the motivation linking two or more prior art references is common sense to a POSITA at the time of the invention.

30. I understand that a particular combination may be proven obvious merely by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. I have further been informed and understand that a POSITA combines the teachings of the prior art references and does not necessarily combine the embodiments of those teachings physically.

31. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

32. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all of the elements of a claim are used in substantially the same manner in devices in the same field of endeavor, the claim is

likely obvious.

33. Additionally, I understand that a patent is likely to be invalid for obviousness if a person of ordinary skill can implement a predictable variation or if there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

34. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

35. I also understand that one of ordinary skill in the art must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

36. I have been informed and I understand that factors referred to as "objective indicia of non-obviousness" or "secondary considerations" are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

37. I also understand that evidence of objective indicia of nonobviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a “nexus,” between any such secondary indicia and the claimed invention. I also have been informed that even when they are present, secondary considerations may be unable to overcome primary evidence of obviousness (e.g., motivation to combine with predictable results) that is sufficiently strong.

38. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

39. I provide my opinions in this Declaration based on the guidelines set forth above.

VI. LEVEL OF SKILL IN THE ART

40. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

41. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication

of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a POSITA is also a person of ordinary creativity.

42. In my opinion, a POSITA in the field of the '711 Patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about the structure of 3D NAND, how it is manufactured, and its component parts.

43. In view of my educational background and work experience, I am a person of more than the ordinary level of skill in the art of the '711 Patent and was so by August 31, 2017. In forming my opinions, I have drawn on my academic background and professional experiences. In forming my opinions herein, however, I took into account the perspective of a POSITA.

VII. THE '711 PATENT'S EFFECTIVE FILING DATE

44. I understand that the application leading to the '711 Patent was filed on September 10, 2018. I further understand that the patent claims priority to an earlier-filed PCT publication No. PCT/CN2018/101308, filed on August 20, 2018,

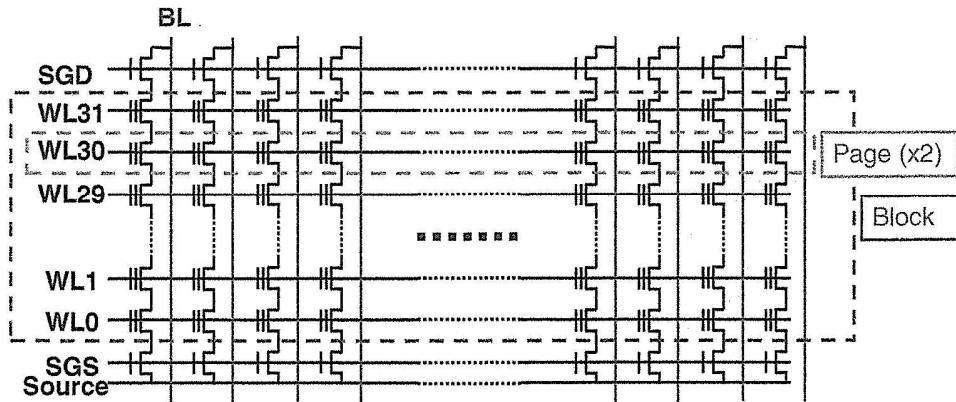
and further to a Chinese patent application 201710774754, filed on August 31, 2017.

45. For purposes of this declaration, I have been instructed to use August 31, 2017 as the priority date of the '711 Patent. My opinions in this declaration were formed from the perspective of a POSITA as of August 31, 2017, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the prior art.

VIII. TECHNOLOGY BACKGROUND

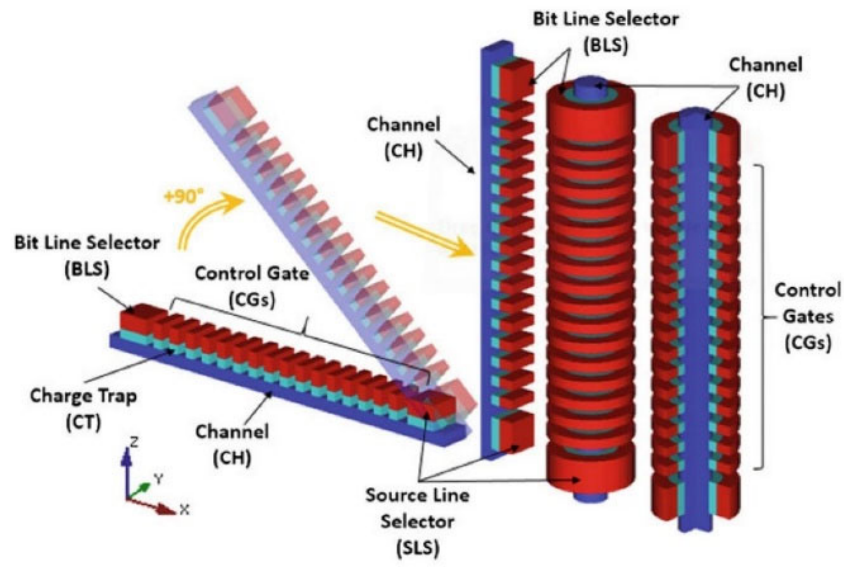
46. The '711 Patent and the prior art references discussed in this Declaration relate to three-dimensional (3D) memory devices, such as 3D NAND memory devices.

47. Central to NAND memory devices is a “memory cell,” which stores information as electrical charge. In these devices, NAND memory cells are arranged in “strings” having multiple cells “connected in series.” Ex. 1009, 38. Early NAND memory devices were formed as two-dimensional arrays of cells on a substrate surface. *Id.*, 58.

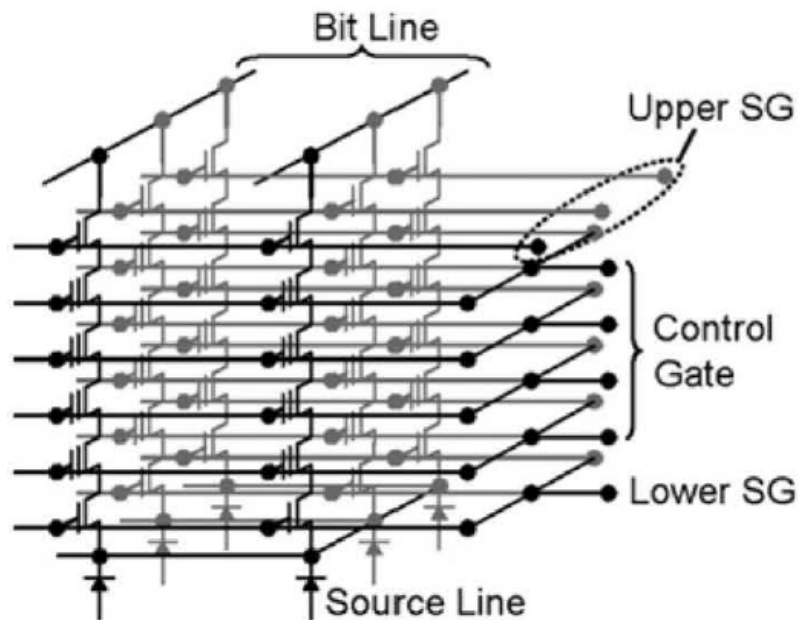


Id., 40.

48. “[T]o further scale down the memory cell size,” “three-dimensional (3D) NAND flash cells” were developed. Ex. 1009, 292. “Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside,” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1010, 3.



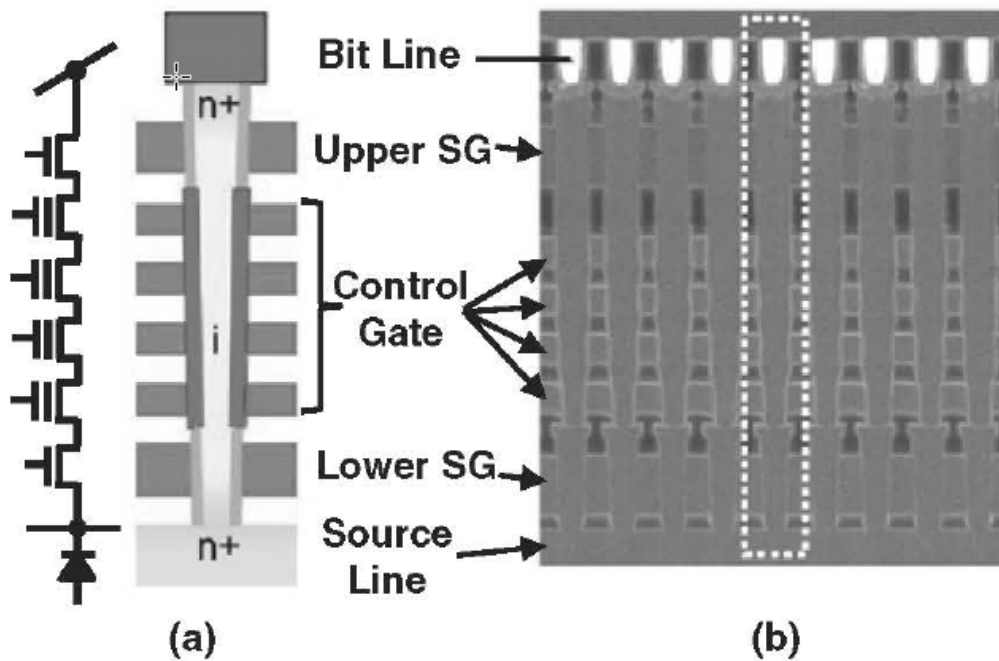
Ex. 1011, 122 (colors in the original). Multiple such vertical channels are repeated in a three-dimensional array:



Ex. 1009, 296. A voltage applied on the control gate (which is also known as the word line) of each cell and the information stored in the cell (e.g., binary 0 or 1 for a one-bit memory cell) determine whether the cell turns on or off. Specifically, the

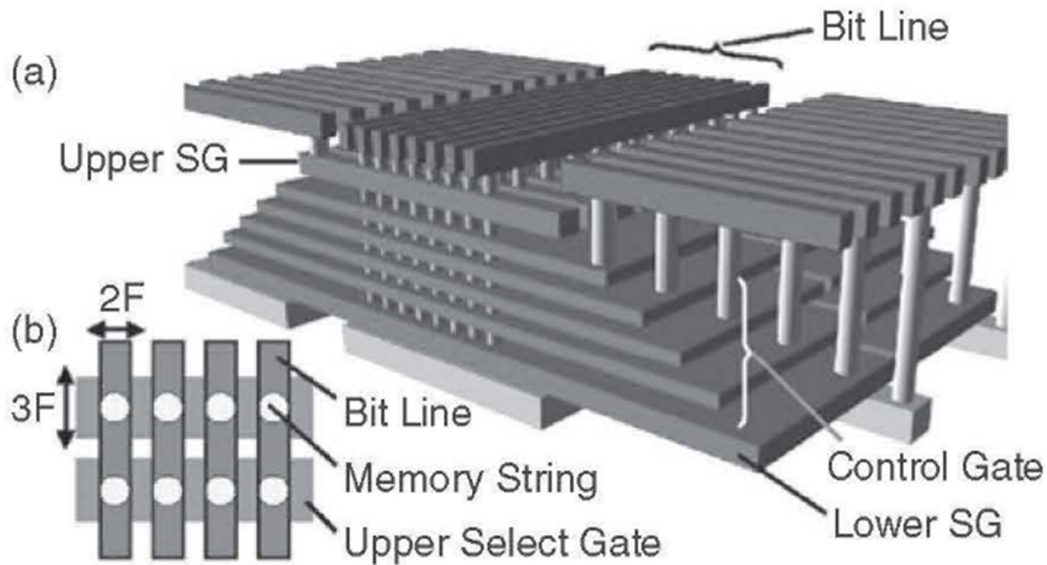
electrical charge (representing information) stored in the cell determines a threshold voltage of the cell, and the cell turns on when the control gate voltage is greater than the threshold voltage. Electrical current can only flow through a string when all cells in the string are turned on. Therefore, by applying a control gate voltage sufficient to turn on all but one cell (the selected cell) in a string and applying a suitable voltage to the control gate of the selected cell, the information stored in the selected cell may be determined using the amount of current flow through the string. *Id.* This process is repeated by selecting a different cell to read (as an example operation) in the next cycle, eventually retrieving the requested information from the cells that store it.

49. A particular vertical memory cell “string is selected by a bit line and an upper select gate (upper SG).” Ex. 1009, 295-296. A memory cell “is located in the intersection of a control gate plate” and the channel of the string. *Id.* The lowest layer is a “select gate (lower SG),” which allows the strings to connect to a lower “common source.” *Id.*, 295, 297. An example 3D NAND vertical memory cell string is shown below:



Id., 296.

50. 3D NAND memory devices include “multi-stacked layers of [control] gate (plate)” material alternated with “dielectric” (insulator of direct current) in a “[s]tack.” Ex. 1009, 294. A “through-hole[.]” channel (which is also known as a channel structure) “filled by memory film ... and channel poly-Si” passes through the layers to form a string of vertically arranged memory cells. *Id.*, 295. “Each” layer of “electrode plate acts as a control gate.” *Id.* “[T]he control gates ... are connected ... [in a] stair-like gate structure.” *Id.*, 295-97.



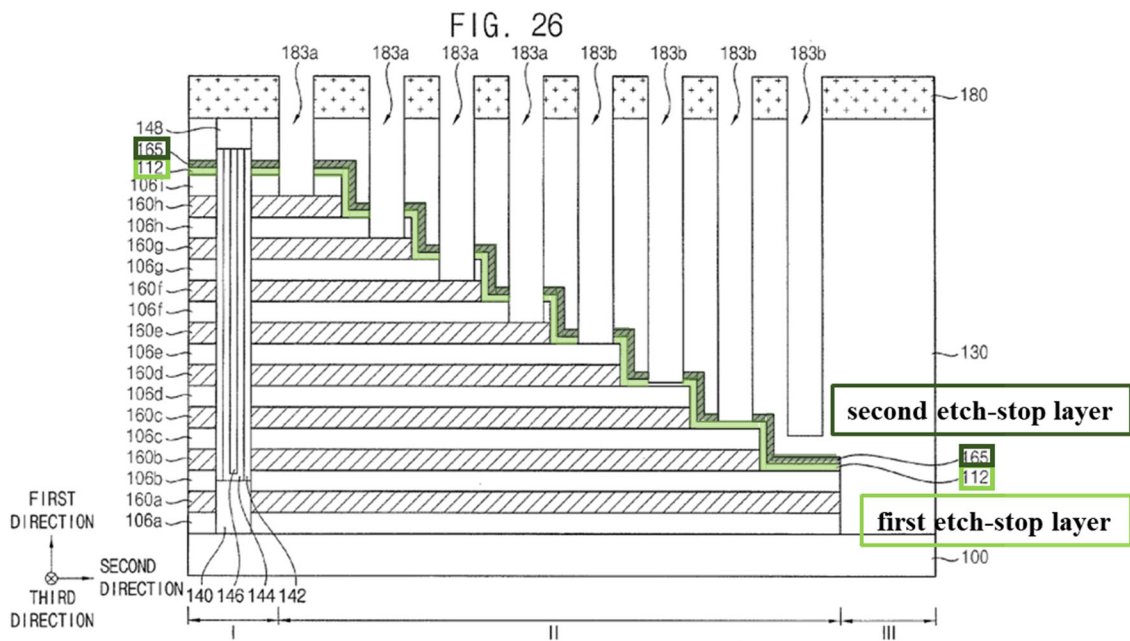
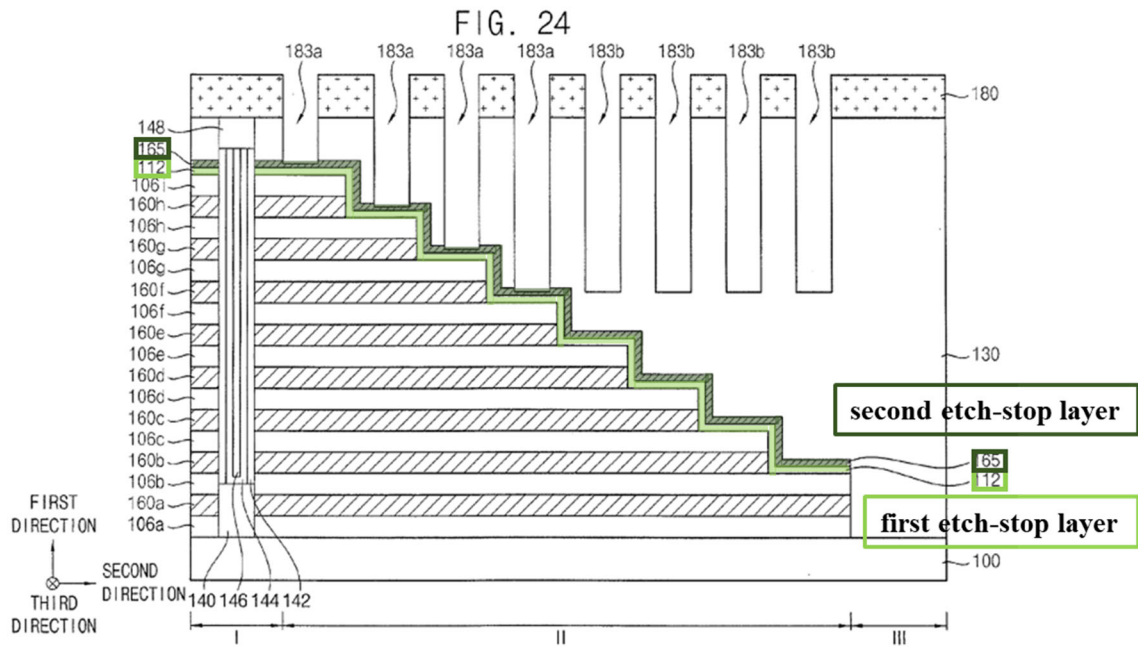
Id., 296 (Fig. 7.6). Vertical conductive structures to couple the control gates to control voltages. The steps of the staircase structure provide landing areas for the vertical conductive structures to contact the control gates. *Id.*, 298.

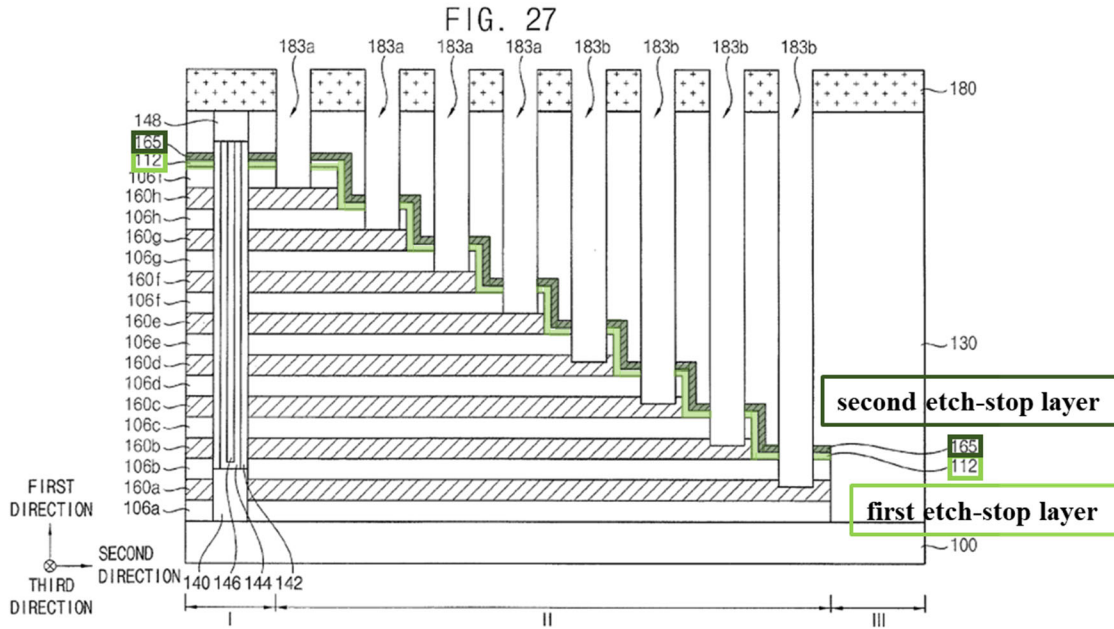
51. As can be seen in the figure above, the vertical conductive structures contacting the different control gate plates have different lengths because the landing areas of the plates are located at different heights. The '711 Patent and the prior art references relate to the technology of fabricating these vertical conductive structures in a reliable and cost-effective manner.

52. The vertical conductive structures are formed by etching holes through an insulating layer above the staircase structure and depositing a conductive material inside the holes. Etching can be done using various techniques and involves an etchant. Different materials react to an etchant differently and an etching rate is used

to characterize how fast or slow an etchant etches through a particular material. On the flip side, a material also can react differently to different etchants. For example, a material may have a high etching rate for one etchant and a low etching rate for a different etchant.

53. Because the conductive structures need to have different lengths and so the holes need to be etched to different depths, techniques were developed to etch holes to their respective lengths. The '711 Patent mentions one such prior art technique. Ex. 1001, 5:51-53. Another prior art technique is to place one or more etch-stop layers above the staircase structure. The etch-stop layers have a lower etching rate than the insulating layer for the etchant used to penetrate the insulating layer. Therefore, when etching reaches the etch-stop layers, etching slows down. This protects the underlying layers and prevents over-etching shallower holes while etching deeper holes. Ex. 1006, [0045]-[0046]. One prior art reference illustrates this through the following sequence of figures:





Ex. 1012, Figs. 24, 26-27.² As shown in Figure 24, etching slows down when it reaches an etch-stop layer such that the four contact holes 183a on the left, each having a different depth from the others, do not penetrate the second etch-stop layer 165. *Id.*, [0113]-[0116]. Then a second etching process is used to etch the second etch-stop layer 165. *Id.*, [0117]. This can also increase the depths of the contact holes 183b (on the right). *Id.*, [0118]. Then a third etching process can be used to further increase the lengths of the contact holes, as shown in Figure 26. *Id.*, [0119]-[0121]. Finally, a fourth etching process can further increase the depths of contact holes 183b. *Id.*, [0122]. Using the etch-stop layers allows the contact

² From this point forward, all color annotations in this Declaration are added except where noted otherwise.

holes of different depths be formed “without defects such as a punching or a not-open failure of the gate lines.” *Id.*, [0124]. Of course, this sequence is merely an example. Other etching sequences can be used as was within the ability of a POSITA.

54. More generally speaking, a layer (“layer 2”) functions as an etch-stop layer when its etching rate is lower than the etching rate of the layer immediately above (“layer 1”). This is known as selective etching and is based on the relative etching rates of materials in the layers. Ex. 1013, 220, 390, 593. Etch selectivity implies that layers 1 and 2 cannot be made from the same material if layer 2 is to function as an etch stop because the same material will have the same etching rate. As explained above, etch selectivity is determined by the etchant used. Accordingly, layer 1 may have a higher etching rate than layer 2 when one type of etchant is used, but a lower etching rate than layer 2 when a different type of etchant is used. These conventional processes were known as “selective etching” and “reverse selective etching.” Ex. 1014, 4, 6 (internal quotation marks omitted). Using different etchants allows greater flexibility in the choices of materials to use as an etch stop. For example, the materials of two layers may be swapped and using a different etchant can still allow the upper layer to function as an etch stop to the lower layer. Other factors in determining the required selectivity of the etch rates are the thickness variability of various layers and the random variability of etching rates of a particular

material due to etchant concentration variability in the etching tool, etc. It is necessary to account for the worst-case scenario where in some locations the thinner layers etch faster, while in other locations the thicker layers etch slower. This can lead to unintentional over-etching in certain locations and punching through the word lines, potentially resulting in short circuits, or under-etching in some other locations, potentially resulting in open circuits. The “barrier layer” in the ’711 Patent is effectively a second etch-stop layer. The use of two etch-stop layers provides additional flexibility in the process and guards against such problems because each layer can be specifically configured to slow down etching when etching penetrates the respective layer above and reaches each etch-stop layer, thereby protecting the underlying layers.

55. An etch stop may be somewhat of a misnomer because etching slows down (perhaps significantly) but does not truly stop. In other words, etching rate of a material can be very small but is not zero.

IX. THE ’711 PATENT AND ITS PROSECUTION HISTORY

56. The ’711 Patent describes 3D memory structures. More specifically, it relates to forming “word line contact structures” on a staircase structure. Ex. 1001, Abstract. As shown below, the word line contact structure is the landing area in which a vertical conductive structure 945 makes contact with a particular step. The landing area is also commonly referred to as the step, because it is the step in the

staircase. And the conductive structure is also commonly referred to as a staircase contact, because it is the contact to the step of the staircase. The '711 Patent discloses a conventional staircase structure 900 with alternating gate stacks 525 and dielectric layers 104:

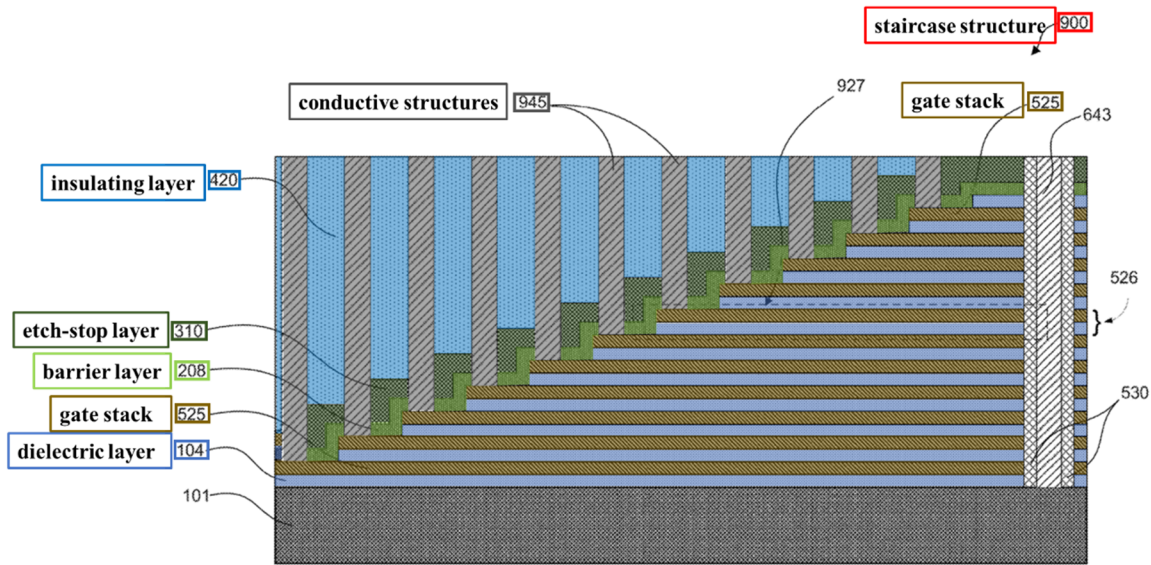


FIG. 9A

Id., Fig. 9A; 8:54-55. As also shown, an optional barrier layer 208 and an etch-stop layer 310 cover the side surface and a portion of the top surface of each step. *Id.*, 5:54-65, 7:30-39, 7:56-58, 7:66-8:3. These coverages are more apparent in Figures 2 and 3, which show the formation of these two layers before the vertical conductive structures are formed. An insulating layer 420 is disposed on the etch-stop layer 310. *Id.*, Fig. 4. Conductive structures 945 (commonly known as staircase contacts) penetrate the insulating layer 420, the etch-stop layer 310, and the barrier layer 208, and contact the gate stacks 525. *Id.*, 10:56-63, 11:14-19. The function of

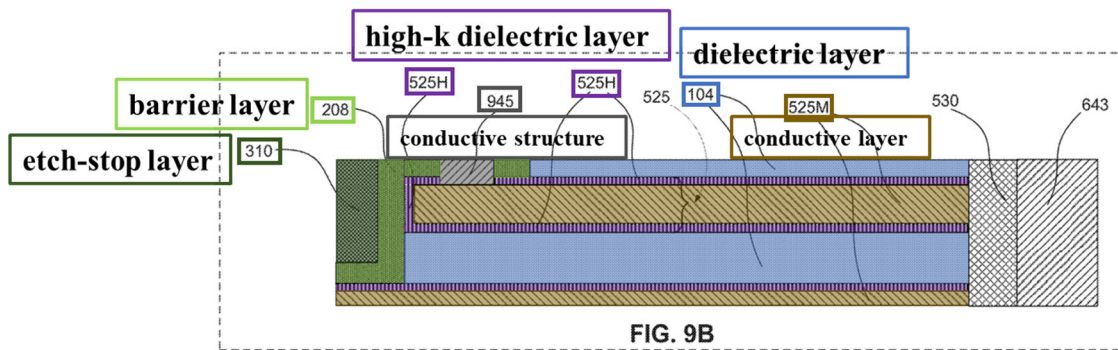
the staircase contacts is to electrically couple the control gate stacks to a word line control voltage. The penetration of the various layers is necessary for this function.

57. In the context of the '711 Patent, a barrier layer is simply an etch-stop layer called by another name. Consistent with the well-known principle I explained above in Technology Background (§ VIII), the '711 Patent states that relative etch selectivity is what enables a layer to “function as an etch-stop layer,” that is, to slow down etching to protect the underlying layers. Ex. 1001, 6:62-67. The only statement in the '711 Patent regarding the function of the barrier layer is that it serves as an etch stop: “protecting the underlying structure during subsequent *etching* processes.” *Id.*, 7:36-39 (emphasis added). The '711 Patent further discloses that “the second insulating layer 208 can be used as a barrier layer.” *Id.*, 7:35-39. This statement implies that the second insulating layer 208 is not necessarily (but merely can be) a barrier layer. Setting aside that implication and assuming the descriptions of insulating layer 208 in the '711 Patent apply to the barrier layer, what the patent discloses regarding the insulating layer 208 confirms the understanding that, for the '711 Patent, a barrier layer is just another etch-stop layer. To begin, the second insulating layer 208 and the etch-stop layer 310 are formed in sequence to the same step shape. *Id.*, 7:30-34, 7:56-58, 8:3-6, Figs. 3-4. They share the same thickness characteristics. *Id.*, 7:39-44, 8:6-10. Moreover, the barrier layer is optional, and, when it is absent, the etch-stop layer would take its place in the structure. *Compare*

id., 7:67-8:6 *with id.*, 7:30-34. When the barrier layer is present, it simply does what an etch-stop layer would do in its absence with respect to protecting the structure during etching. *Id.*, 8:56-64 (“In some embodiments, removing the sacrificial layer 106 is also selective to the second insulating layer 208. In some embodiments, the second insulating layer 208 is optional, and removing the sacrificial layer 106 is selective to the etch-stop layer 310.”). Both layers comprise an insulating material. *Id.*, 7:51-52 (“the second insulating layer 208 can be made of similar material as the first insulating layer 104.”), 7:64-66 (“The etch-stop layer 310 can be made of any suitable insulating material that is different from the second insulating layer 208.”). This last statement regarding the two layers having different materials is understandable from my explanation above, that two adjacent layers must have different materials for the lower layer to function as an etch-stop layer with respect to the upper layer. §VIII. Both layers have an etching rate needed to slow down etching, *i.e.*, an etching rate lower than that of the layer immediately above. Ex. 1001, 9:60-62 (“the etching rate of the third insulating layer 420 is higher than the etching rate of the etch-stop layer 310”), 10:45-47 (“the etch-stop layer 310 can be etched faster than the second insulating layer 208.”); §VIII. Thus, both etch-stop and barrier layers serve the same purpose, *i.e.*, to slow down the etching process to protect the underlying layers from over-etching. Ex. 1001, 5:61-63 (“The etch-stop film protects underlying layers during etching processes that form contact VIAs.”),

7:36-39 (“the second insulating layer 208 can be used as a barrier layer for protecting the underlying structure during subsequent etching processes.”), 10:3-14.

58. In certain embodiments of the '711 Patent, each gate stack 525 comprises a conductive layer 525M at the center, surrounded on three sides by a high-k dielectric layer 525H:



Ex. 1001, Fig. 9B, 8:65-9:4. The conductive structure 945 penetrates the high-k dielectric layer 525H in addition to (as shown above in Figure 9A) the insulating layer 420, the etch-stop layer 310, and the barrier layer 208 and contacts the conductive layer 525M, thereby forming a contact to the control gate. *Id.*, 10:56-63, 11:14-22. This contact, again, is necessary to control the respective gate layers, that is, word lines of the 3D memory device.

59. The '711 Patent asserts that by using an etch-stop layer, the staircase contacts 945 of different lengths may be simultaneously formed using one lithography mask without reducing manufacturing yields due to over-etching the shallower contact holes. Ex. 1001, 5:40-65. In other words, the '711 Patent alleges

that inadvertent punch-through (etching too far and into underlying layers) of shallower holes will not occur. The '711 Patent asserts that its etch-stop layer provides a lower-cost solution than the conventional method using multiple lithography masks. *Id.*, 5:51-53, 5:65-67.

60. During prosecution, the Examiner rejected various pending claims under §102(a)(1) as being anticipated by Oh (U.S. Patent Pub. No. 2016/0358855A1) and anticipated by Matsuda (U.S. Patent Pub. No. 2016/0020169A1). Ex. 1002, 152-56. The Examiner further rejected the remaining claims under §103 over Matsuda in view of Examiner's Official Notice regarding the thickness of an etch-stop layer. *Id.*, 156-57. The Applicant amended the independent claims to add a high-k dielectric layer to the gate stack. *Id.*, 201-08. The Examiner then allowed the amended claims. *Id.*, 239.

61. Every aspect of its alleged invention, however, including the high-k dielectric layer that led to allowance, was conventional by the time of the application was filed, as I will demonstrate below. In particular, a high-K material surrounding the gate layers was a well-known feature well before the priority date of the '771 Patent.

X. CLAIM CONSTRUCTION

62. I stated my understanding of the law on claim construction above. §V.A. It is my opinion that all terms of the '711 Patent's claims may be understood

based on their plain and ordinary meaning.

XI. SUMMARY OF OPINIONS

63. I have reviewed and analyzed the prior art references and materials listed in §XII below.

64. For the reasons I explain in greater detail below, it is my opinion that before the earliest possible filing date of the '711 Patent on August 31, 2017, a POSITA would have considered claims 1-19 of the '711 Patent to be unpatentable as obvious over the prior art discussed in this declaration. Below is the summary of the grounds detailed in this declaration:

Ground	Claim(s)	Prior Art Asserted
1	1-9, 11-16, and 18-19	Obvious under §103 based on Kim (Ex. 1005) in view of a POSITA's knowledge
2	10 and 17	Obvious under §103 based on Kim in view of Fang (Ex. 1007)
3	1-6, 8-9, 11-16, and 18-19	Obvious under §103 based on Park (Ex. 1006) in view of a POSITA's knowledge
4	7, 10, 15, and 17	Obvious under §103 based on Park in view of Fang

XII. THE PRIOR ART

65. The prior art references are analogous art to the '711 Patent. They are in the same field of endeavor of improving 3D memory devices, and more specifically relating to the word-line contact structures of such devices.

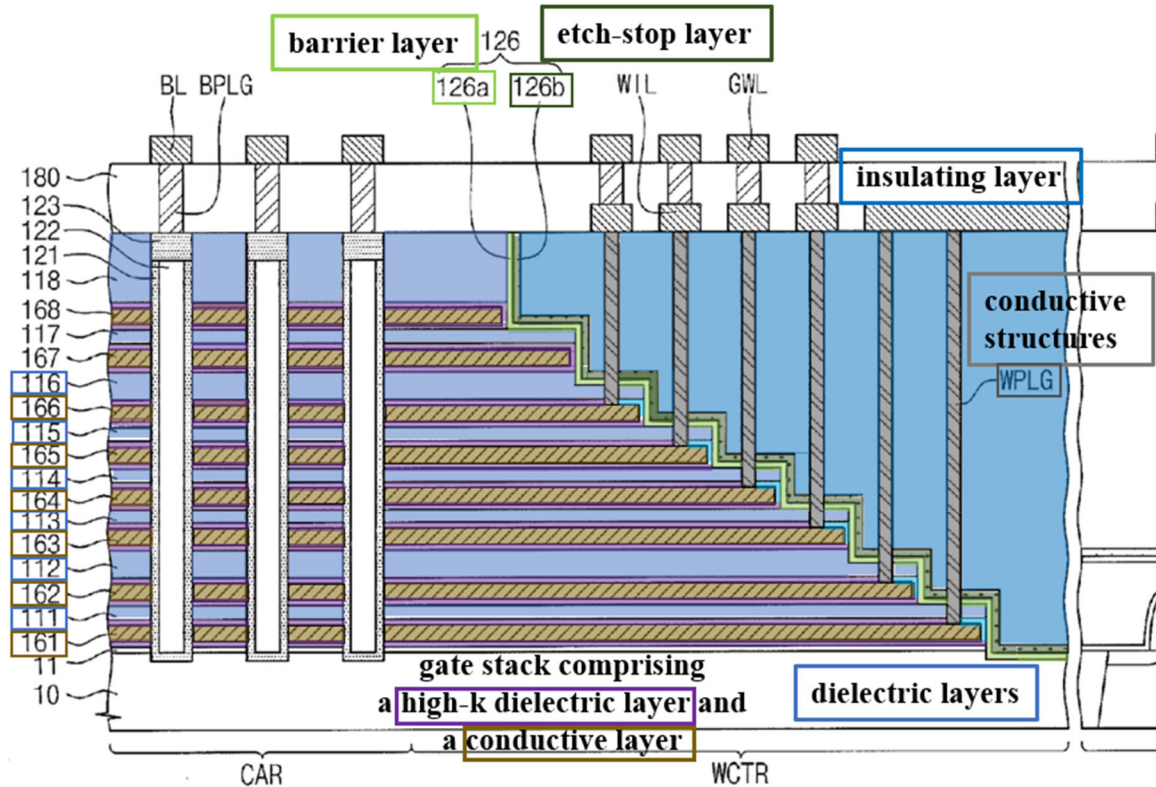
A. Kim

66. U.S. Patent Publication No. 2012/0070944 (Ex. 1005 or “Kim”). Kim was filed on September 13, 2011 and was published on March 22, 2012. Ex. 1005, Cover. I understand Kim is prior art to the ’711 Patent.

67. Kim discloses a 3D semiconductor memory device having a cell-array region, a peripheral-circuit region, and a word-line contact region WCTR disposed between the cell-array region and the peripheral-circuit region. Ex. 1005, Abstract, [0037]. Kim focuses on the issue of planarizing the interlayer dielectric (which is analogous to the insulating layer of the ’711 Patent) between the regions. *Id.*, [0024]-[0025].

68. It is my opinion that Kim’s descriptions of the word-line contact region WCTR render obvious the alleged invention of the ’711 Patent. In advance of the detailed analysis below, this is readily apparent by comparing Kim’s Figure 22A with Figures 9A-9B of the ’711 Patent in §IX above.

Fig. 22A



Ex. 1005, Fig. 22A.³

69. Like Figure 22A above, Kim's figures show embodiments in which a dielectric layer is disposed over a gate stack at each step. But Kim also discloses the reverse order, that is, embodiments in which a gate stack is disposed over a dielectric layer at each step. For example, after describing the layer ordering in its figures, Kim discloses that "[i]n other embodiments, each of top surfaces of the sacrificial

³ All cross-sectional images from Kim shown in this Declaration omit the peripheral-circuit region that is irrelevant to this Declaration.

layers SC1 to SC8, not the top surfaces of the insulating layers 111 to 118, may be partially exposed in the word line contact region WCTR.” Ex. 1005, [0090]. Sacrificial layers SC1-SC8 are replaced with, and thus positionally correspond to, gate stacks in the fully formed device comprising gate-electrode layers and blocking layers. *Id.*, [0104]-[0105], [0198]-[0200]. This can be seen by comparing Figures 17A and 22A, for example. More specifically, Kim discloses that the edge portions of the sacrificial layers SC1-SC8 (or of the insulating layers 111 to 118) may be exposed as the top surfaces of the steps. *Id.*, [0091] (“the insulating layers 111 to 118 and/or the sacrificial layers SC1 to SC8 thereof may have the edge portions sequentially exposed on the word line contact region WCTR.”), [0240] (“the insulating layers 111 to 118 and/or the sacrificial layers SC1 to SC8 thereof may have the edge portions sequentially exposed on the word line contact region WCTR.”). In other words, the edge portions of the gate stacks can be positioned directly below the first stop layer 126a. Therefore, Kim discloses disposing a gate stack over a dielectric layer at each step.

70. This Declaration relies on Kim’s Figure 17A-22B embodiment comprising an etch-stop layer and a barrier layer. Kim discloses other embodiments, such as Figures 5A-14B.

71. Even though Kim discloses different embodiments, a POSITA would have understood that descriptions of one of Kim’s embodiments apply to other

embodiments except where the embodiments differ. Kim discloses closely related embodiments having many of the same elements denoted by the same reference numerals. Ex. 1005, [0184]. For example, the embodiments shown in Figures 5A-14B and in Figures 17A-22B are closely related. Accordingly, Kim states that overlapping descriptions of the same elements are omitted in the descriptions of Figures 17A-22B. *Id.* Moreover, the descriptions of Figures 17A-22B extensively reference Figures 9A-14B. *Id.*, [0183]-[0212]. Similarly, as another example, descriptions of Figures 26-27 refer to the two embodiments in Figures 17A-22A and 8A-11A. *Id.*, [0221], [0223]-[0224]. A POSITA would have understood Kim's various embodiments to be variants of each other that share many common elements and characteristics.

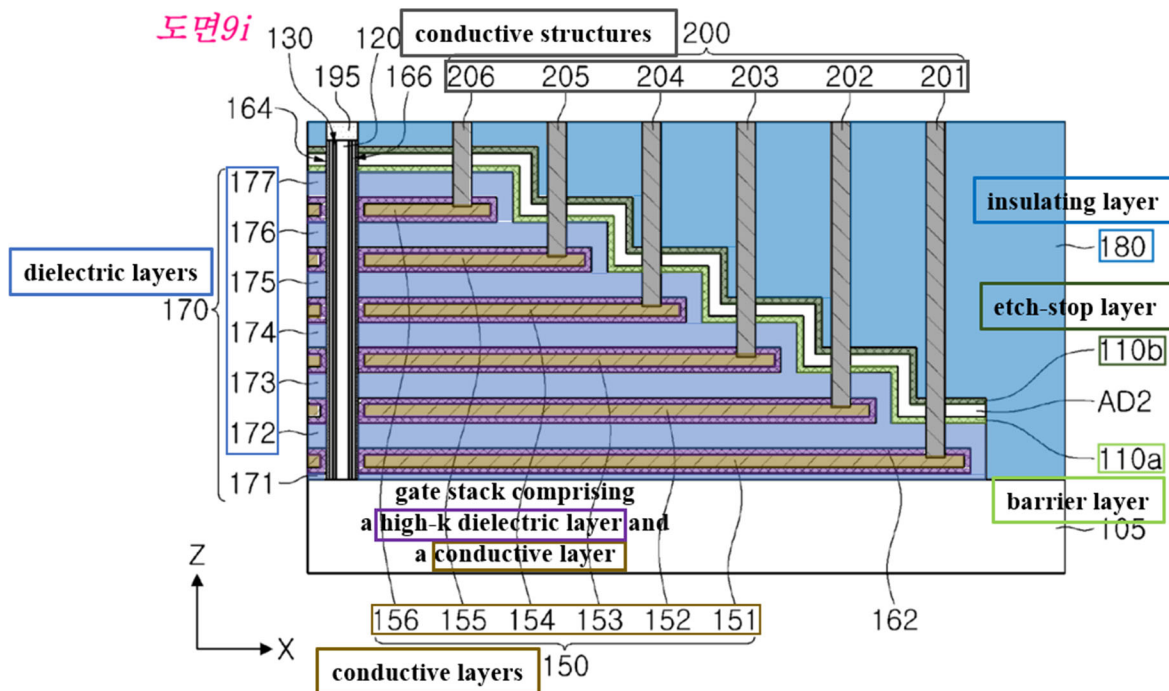
B. Park

72. Korean Patent Publication No. 20150051841A1 (Ex. 1006 or "Park"). Park was filed on November 5, 2013 and was published on May 13, 2015. Ex. 1006, Cover. I understand Park is prior art to the '711 Patent.

73. Park focuses on solving the same problem the '711 Patent alleges to solve, *i.e.*, preventing what is known as "bridge defects" caused by over-etching the shallow contact holes when forming word-line contacts. Ex. 1006, [0014], [0045]-[0046], [0050]-[0051]. Park's earlier solution is the same as that of the '711 Patent: using a barrier and etch-stop layer (which Park identifies as two etch-stop layers)

and including a high-k dielectric layer around the gate layers. *Id.*, [0049]-[0051]; §IX (explaining that the barrier layer of the '711 Patent is just another etch-stop layer).

74. In advance of the detailed analysis below, the fact that Park's descriptions of the word-line connection region disclose what the '711 Patent alleges to invent is also readily apparent by comparing Park's Figure 9i with Figures 9A-9B of the '711 Patent in §IX above.



Ex. 1006, Fig. 9i.

75. Like Kim, Park's figures show embodiments in which a dielectric layer is disposed over a gate stack at each step, as exemplified by Figure 9i above. But Park also discloses embodiments in which a gate stack is disposed over a dielectric

layer at each step. For example, with respect to the Figure 9 embodiment, Park discloses that “a portion of the top surface of each insulating layer (170) may be exposed by the plurality of pad regions (P1-P6).” Ex. 1006, [0102]. This describes Figure 9a. But Park further discloses that “unlike what is shown in FIG. 9a, a portion of the top surface of each sacrificial layer (140) may be exposed in a plurality of pad regions (P1-P6).” *Id.* Moreover, Park teaches the same about a closely related Figure 4/8 embodiment. *Id.*, [0042]. Like Kim and as was conventional, Park’s sacrificial layers 140 are replaced with gate stacks. *Id.*, [0104]-[0105]. This can be seen by comparing Figures 9a and 9i, for example. Therefore, Park discloses disposing a gate stack over a dielectric layer at each step.

76. This Declaration relies on the embodiment shown in Figures 5 (perspective view) and 9a-9j (cross-sectional views), comprising an etch-stop layer and a barrier layer (again, called two etch-stop layers in Kim). Ex. 1006, [0100]. Park discloses other embodiments, such as one illustrated in Figures 4 (perspective view) and 8a-8m (cross-sectional views). *Id.*, [0073].

77. Even though Park discloses different embodiments, a POSITA would have understood that descriptions of one of Park’s embodiments apply to other embodiments except where the embodiments differ. Park discloses closely related embodiments and teaches that “various embodiments may be combined,” and “elements indicated by the same symbols in the drawings are the same elements.”

Ex. 1006, [0017]. Further, most aspects of the Figure 5 embodiment “are the same as” the Figure 4 embodiment. *Id.*, [0049]. Thus, disclosures of Figures 4 and 8a-8m apply to Figures 5 and 9a-9j except where they differ. A POSITA would have understood Park’s various embodiments to be variants of each other that share many common elements and characteristics.

C. Fang

78. U.S. Patent Publication No. 2019/0067306A1 (Ex. 1007 or “Fang”) was filed on August 24, 2017 and was published on February 28, 2019. Ex. 1007, Cover. I understand Fang is prior art to the ’711 Patent.

79. Like the ’711 Patent, Kim, and Park, Fang discloses a 3D semiconductor memory device having a staircase structure. Ex. 1007, [0002]. The structure comprises alternating dielectric layers and conductive layers. *Id.*, Abstract. Fang’s structure further comprises a silicon nitride etch-stop layer and an oxide insulating layer. *Id.* Conductive word-line structures contacting the conductive layers are formed in openings through the insulating layer, the etch-stop layer, and the dielectric layers:

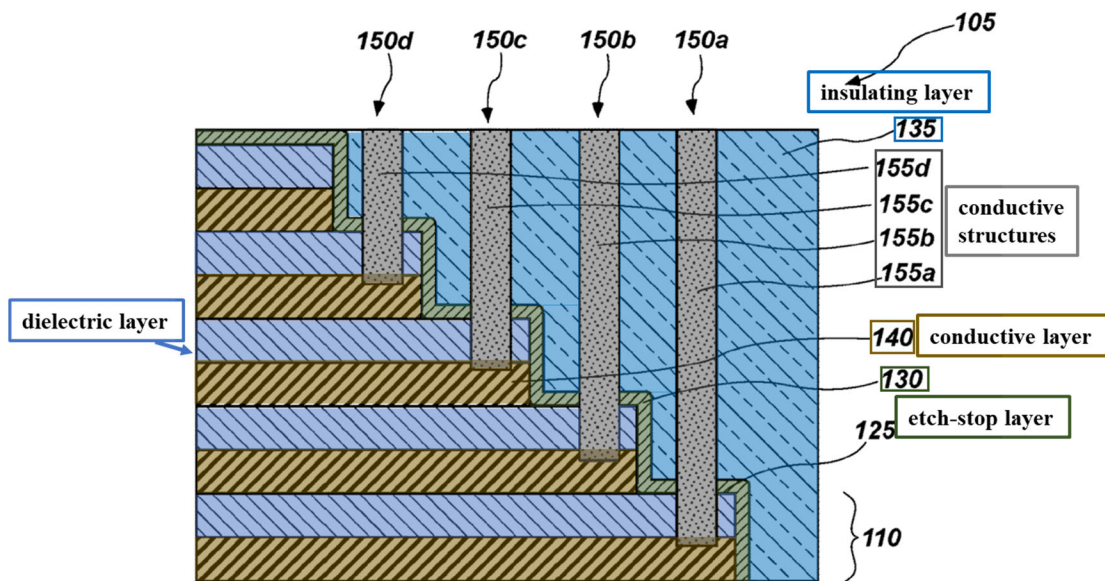


FIG. 6

Id., Fig. 6.

XIII. GROUND 1: KIM IN VIEW OF A POSITA'S KNOWLEDGE

A. Kim Discloses “a Gate Stack Disposed over a Dielectric Layer”

80. Kim discloses the gate-stack-on-top layer ordering even though its figures show the opposite order. §XII.A. A POSITA would have understood that this teaching of the gate-stack-on-top layer ordering applies to the Figure 17A-22B embodiment. As explained above, Kim's descriptions apply to common aspects across embodiments. *Id.* A POSITA would have understood that the reverse layer ordering is compatible with the variations between Kim's embodiments. Kim's teaching at least renders the limitation obvious. In fact, visualizing the reverse layer ordering would have been well within the grasp of a POSITA.

Chen discloses both orders side-by-side:

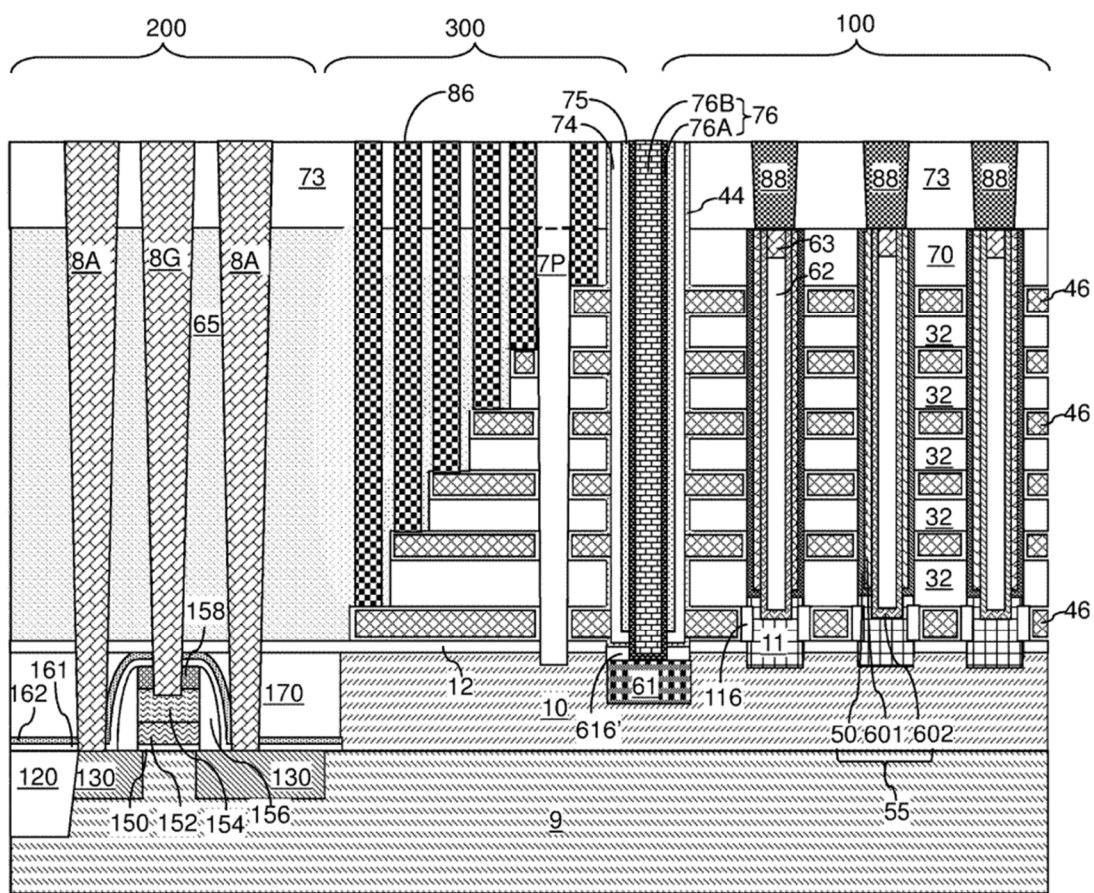


oxide on top, or nitride on top in the staircase. The nitride layers (which is

commonly the sacrificial layer) are then selectively etched off and the cavities refilled with a high-k gate dielectric such as hafnium dioxide and a word line metal such as tungsten (*i.e.*, the gate stack).

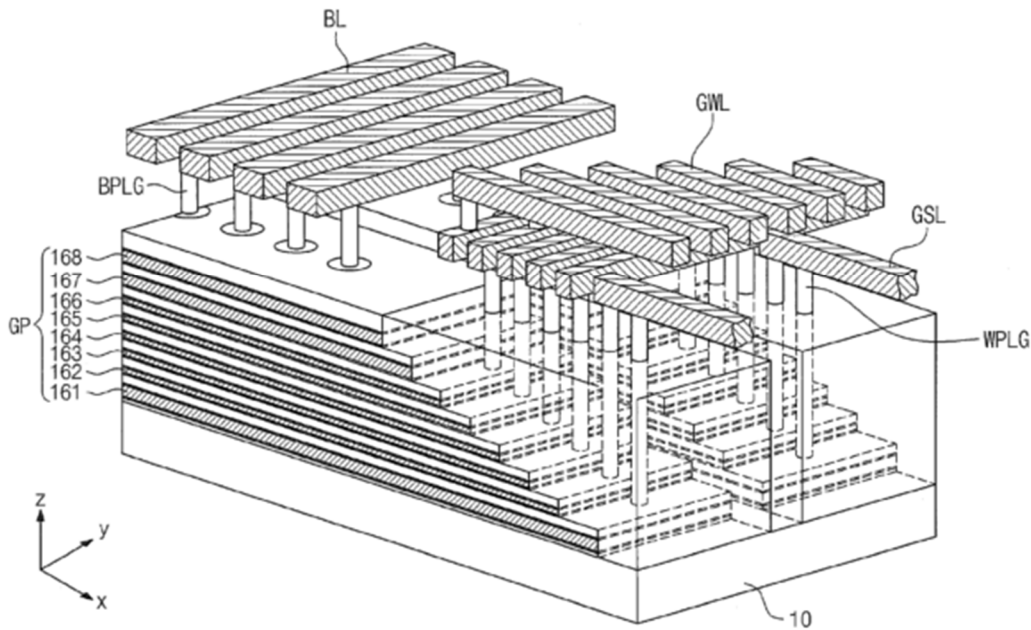
82. At the very least, as Chen confirms, Kim's teaching on reversing the order represents a known technique that is at least a suitable option for the Figure 17A-22B embodiment. Chen demonstrates that either order was viable and known to a POSITA.

83. Below, Kim's figures are modified to show this gate-stack-on-top ordering. Based on Kim's express teaching and a POSITA's knowledge, a POSITA could have easily visualized how the reversed order would be arranged. Doing so was well within the knowledge and skill of a POSITA. Furthermore, prior art references with gate-stack-on-top configurations would have helped a POSITA visualize a Kim embodiment with gate stacks on top. Two additional examples are shown below:



Ex. 1015, Fig. 13.

Fig. 4



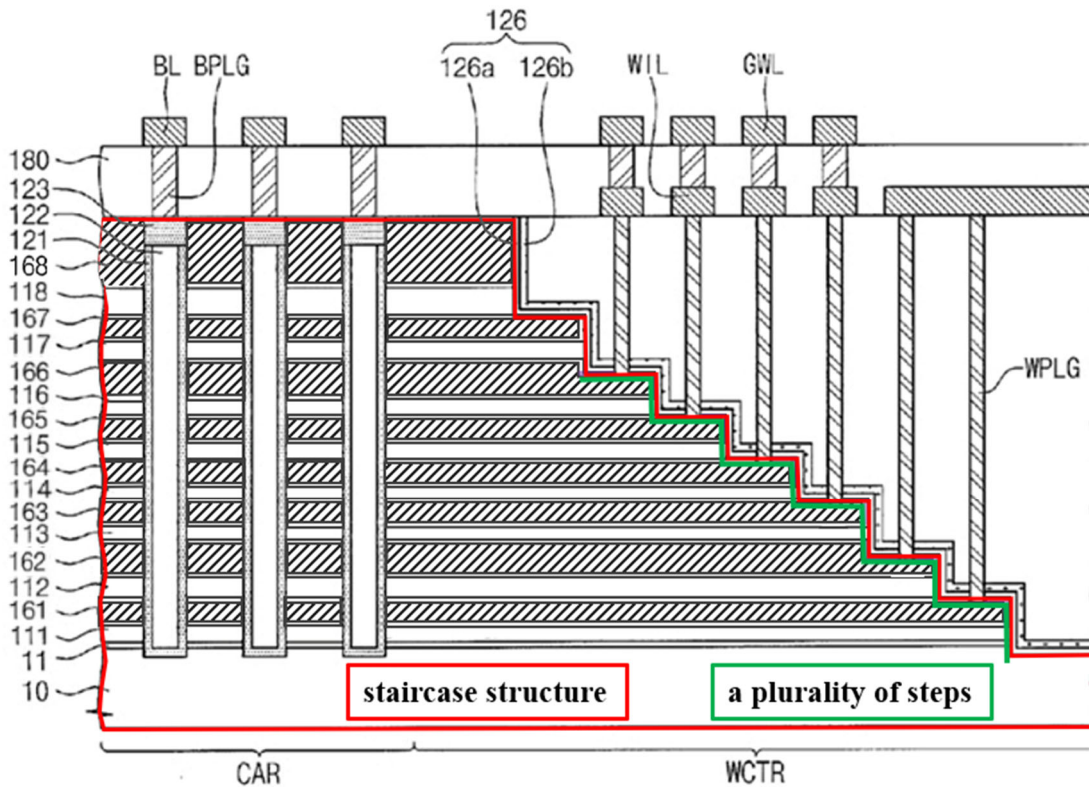
Id., Fig. 4. The word line contact staircase structure that is the focus of the '711 Patent is a prominent feature of this semiconductor structure.

2. [1.A] “a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;”

86. Kim at least renders this limitation obvious.

87. Kim’s 3D semiconductor device comprises *a staircase structure comprising a plurality of steps*:

Gate-Stack-on-Top Fig. 22A



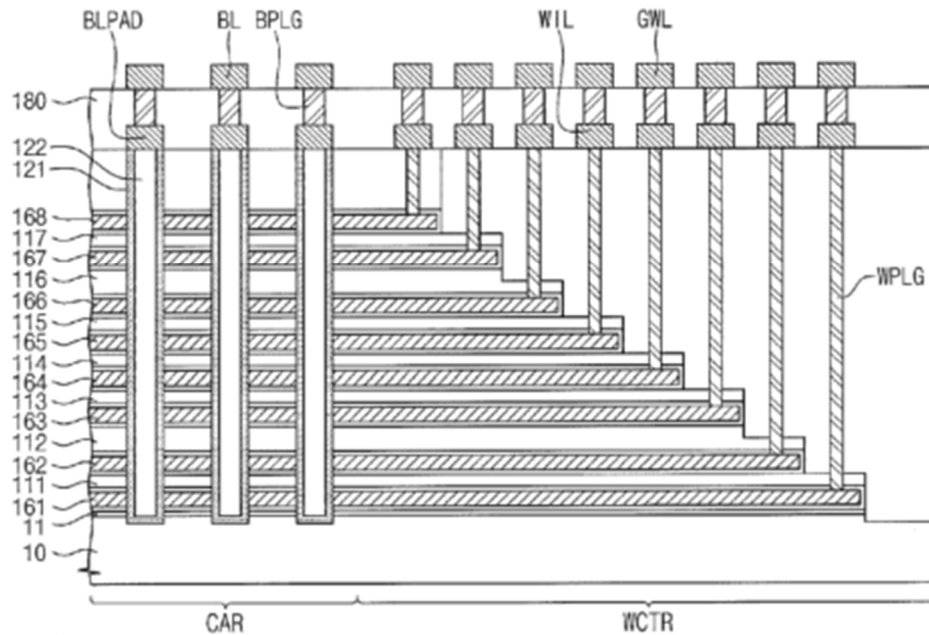
Ex. 1005, Fig. 22A, [0008] (“the stacked layer structure ... comprising a stepwise shaped portion disposed on the contact region”), [0185] (“[a] stacked layer structure ST having the stepwise structure”), [0211] (“the gate structure GP has a stepwise structure in the word line contact region WCTR”). The steps provide landing areas for staircase contacts.

88. As an initial matter and as shown above, the *plurality of steps* may be the bottom six steps, that is, the *plurality of steps* may not include all of the steps of the *staircase structure*. This is relevant to limitation [1.E], because [1.E] requires “wherein each conductive structure is formed on the conductive layer of the each

step.” The *plurality of steps* does not need to include all steps of the *staircase structure*, because I understand the term *a staircase structure comprising a plurality of steps* permits additional steps given the use of *comprising* in patent usage.

89. Moreover, a POSITA would have understood, and certainly found obvious, that there is a conductive structure that is not shown on the top steps, and the *plurality of steps* would then include all steps. This is because the channel structures are effectively a string of memory cells at the interface of the channel and the word lines (which are the conductive layers coupled to the vertical conductive structures), and for various memory cell operations (such as a read operation) targeting a memory cell in the middle of the memory string, it is necessary to turn on all memory cells above and below the target cell by applying a voltage (commonly known as a pass voltage) to the memory cells through the word lines (*i.e.*, gates). §VIII. The memory would not be able properly function without a contact to each gate layer because the pass voltage (for example) is applied through that contact to the memory cell at the intersection of the gate layer and the channel. Indeed, usually the top gate layer is a select (to turn on the memory string) layer, typically a drain-select layer. Therefore, it was conventional for a staircase structure to have a conductive structure on every step. Examples abound just within a few references cited in this Declaration. Ex. 1006, Fig. 9i; Ex. 1007, Fig. 17; Ex. 1008, Figs. 7A-7B. Indeed, Kim also discloses such an embodiment:

Fig. 30

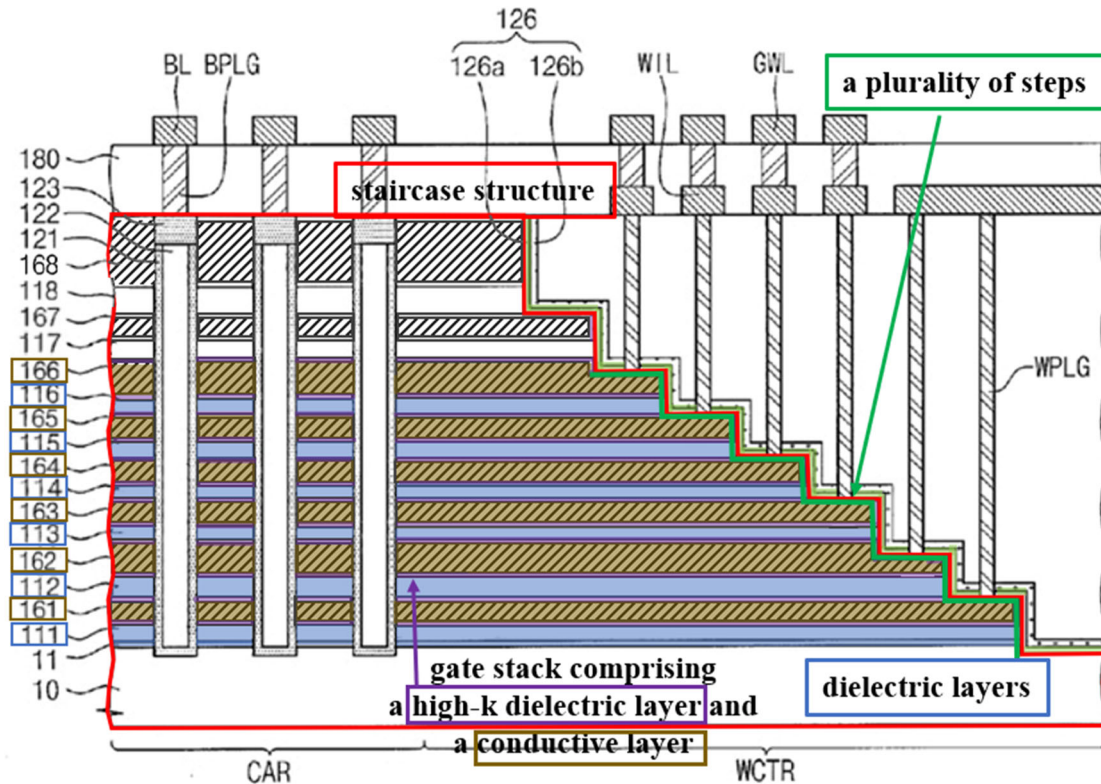


Ex. 1005, Fig. 30. This further demonstrates that a POSITA would have understood, and found obvious, to include a contact on the top steps. While the figures do not annotate the top step, this Ground equally applies to including contacts on each step of the staircase.

90. Getting back to the claim limitation, in the gate-stack-on-top embodiment, *each step comprises a gate stack disposed over a dielectric layer* (one of “insulating layers” 111-116), *the gate stack comprising a high-k dielectric layer* (“blocking insulating layer 150c,” shown in purple, included in “data storing

layer” 150⁵) *and a conductive layer* (one of “gate electrodes” 161-166):

Gate-Stack-on-Top Fig. 22A



Ex. 1005, Fig. 22A, [0229] (“the stacked layer structure ST may include gate conductive layers 101 to 108 and the insulating layers 111 to 118 alternately stacked on the substrate 10.”); [0185]-[0186] (“stepwise structure ... [comprising] insulating layers 111 to 118....”), [0211] (“the gate electrodes 161 to 168 located at different levels from each other”), [0064], [0086]-[0087], [0202] (“the gate electrodes 161 to 168 may be formed ... provided with the data storing layer 150”).

⁵ Layer 150 is shown in, *e.g.*, Figures 13A, 15A-D.

“The formation of the gate electrodes 161 to 168 may include forming a gate conductive layer....” *Id.*, [0202]; *id.*, [0157]. The high-k dielectric layer typically results from depositing the data-storing layer around the channel. That deposition occurs at a time when the sacrificial layers have been etched away and a recess region that connects to the channel has been formed in their place. *Id.*, [0200]. Therefore, when the channel is coated with a data-storing layer, the same material would form around the recess region, including the interface surfaces between the sacrificial layers (which are now removed) and dielectric layers.

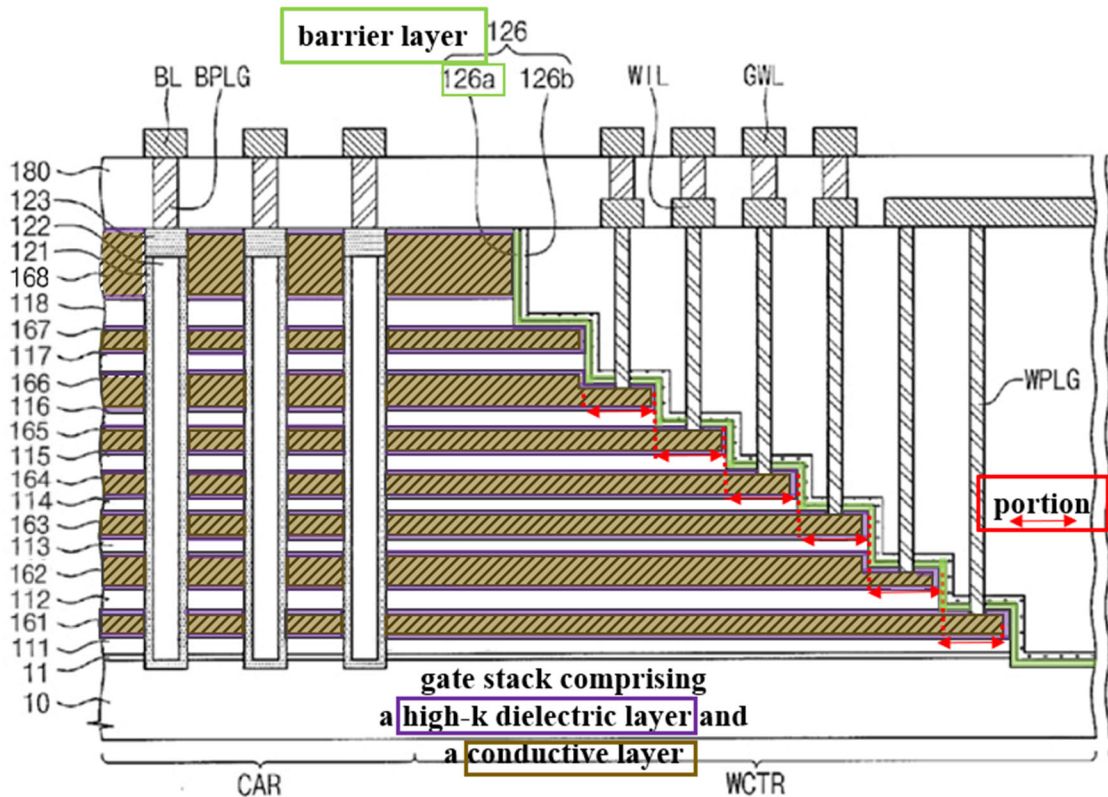
91. Kim discloses “forming a data storing layer 150 and gate electrodes 161 to [166]” between insulating layers. Ex. 1005, [0200]. The data-storing layer 150 forms a conformal covering of the gate electrodes. *Id.*, [0202], Figs. 13A-13B. Consistent with a POSITA’s understanding, Kim explains that “conformality is a layer property describing how well the topography of the underlying surface is replicated. For example, a conformal layer has substantially the same shape as the surface it covers and/or has substantially the same thickness throughout.” *Id.*, [0144]. The data-storing layer may include a blocking insulating layer 150c, which may comprise *a high-k dielectric*. *Id.*, [0148] (“the data storing layer 150 may include ... a blocking insulating layer 150c....”), [0151] (“The blocking insulating layer 150c may include ... high-k dielectric”), Figs. 15B-15D.

3. [1.B] “a barrier layer disposed over a portion of the gate stack of the each step;”

92. As a preliminary matter, Kim’s disclosures of the first stop layer 125a and the second stop layer 125b apply to the layers labeled 126a and 126b in Figure 22A, respectively, for purposes of these claims. The “stepwise etch stop pattern [comprising layers] 126[a and 126b]” simply results from removing the portions of the first stop layer 125a and the second stop layer 125b at the top surface of Kim’s staircase structure. Ex. 1005, [0201]; *compare id.*, Fig. 19A (showing 125a-125b) *with id.*, Fig. 20A (showing 126a-126b after the removal). Therefore, the layers 125a and 125b have the same respective materials and characteristics (such as etching rate and thickness) as the pattern 126a and 126b.

93. Kim discloses *a barrier layer* (“first stop layer” 126a) *disposed over a portion of the gate stack of the each step*:

Gate-Stack-on-Top Fig. 22A



Ex. 1005, Fig. 22A. Although Kim does not expressly state that the first stop layer 126a serves as an etch stop, a POSITA would have understood the etch selectivity of the first stop layer to serve the purpose of preventing punch-through and protecting underlying structures. *Id.*, [0186]-[0187]. Kim teaches that the two etch-stop layers, 126a and 126b, deposited after the WCTR stack has been formed, have different material compositions and therefore different (slower) etch rates for the anisotropic etch chemistry used to etch the deep VIAs in the thick interlayer insulator 134. In addition, the two etch-stop layers are selective with respect to the insulators (111-118) and the sacrificial layers (SC1-SC8) in the stack, respectively. If the

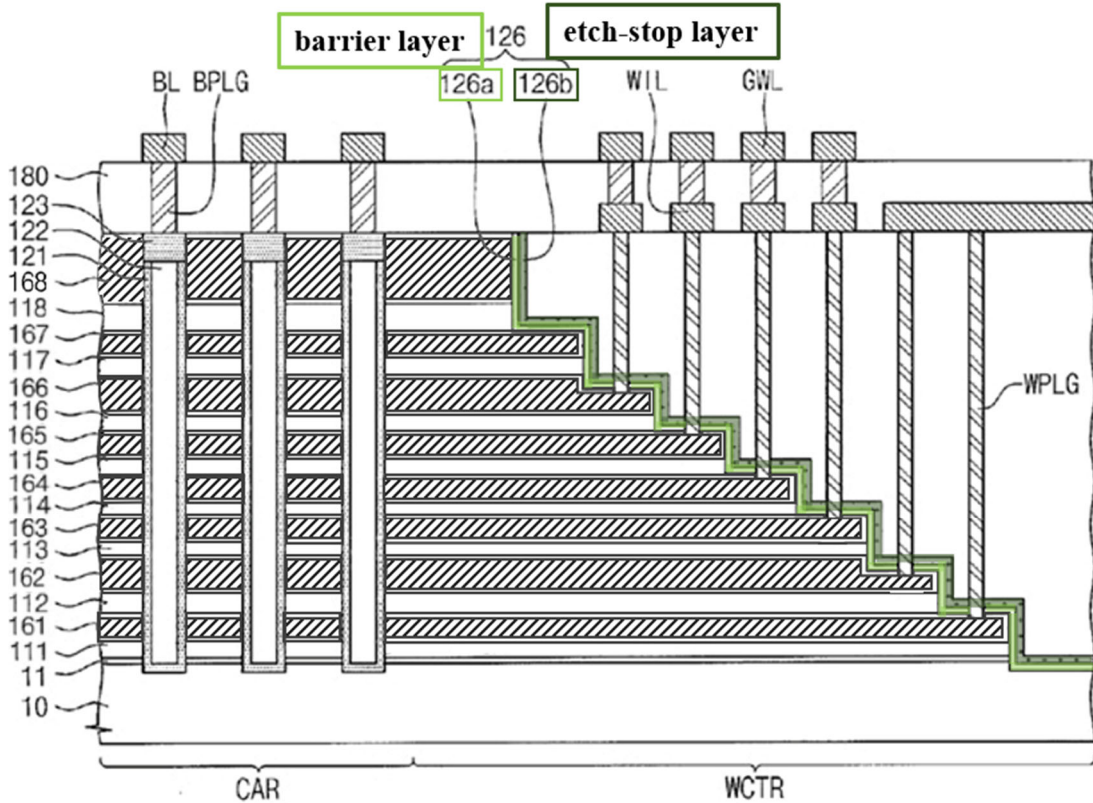
interlayer insulators 111-118 have the same composition as the thick insulator 134 (a viable option as a POSITA would have known), layer 126b can prevent punching through the insulators 111-118. On the other hand, layer 126a could be selective with respect to the sacrificial layers SC1-SC8, as well as the gate stack that is subsequently used to fill the cavities formed by etching SC1-SC8. Both layers 126a and 126b protect the sidewalls of the stack because the etch used to form the deep VIAs is anisotropic, that is, the etching rate can be different in different directions. If the order of the layers in the stack is reversed (*i.e.*, gate stack on top versus gate stack on bottom), it would be simple to modify the VIA etch process to handle either option. This serves the purpose and function of a barrier layer as explained above.

§IX (explaining that a barrier layer is just another etch-stop layer). An etch stop is what “stop” in “first stop layer” refers to. Again, an etch stop slows (not stops) the etch, thereby protecting the underlying layer from potential punch-through. This is consistent with my understanding that patent law does not require prior art to call a claim limitation by the same term in order to invalidate it. The first stop layer 125a in Kim is “formed to conformally cover an exposed surface,” including a top surface of a step or, equivalently, *a portion of the gate stack*, of the staircase structure. Ex. 1005, [0187]; *see also id.*, [0185], [0213].

4. [1.C] “an etch-stop layer disposed on the barrier layer;”

on the barrier layer (“first stop layer” 126a):

Gate-Stack-on-Top Fig. 22A



Ex. 1005, Fig. 22A, [0201]. Similar to the barrier layer limitation, although Kim does not expressly state that the second stop layer 126b serves as an etch stop, a POSITA would have understood the etch selectivity of the second stop layer to serve the purpose of preventing punch-through and protecting underlying structures. *Id.*, [0186]-[0187]. An etch stop is what “stop” in “second stop layer” refers to. Also,

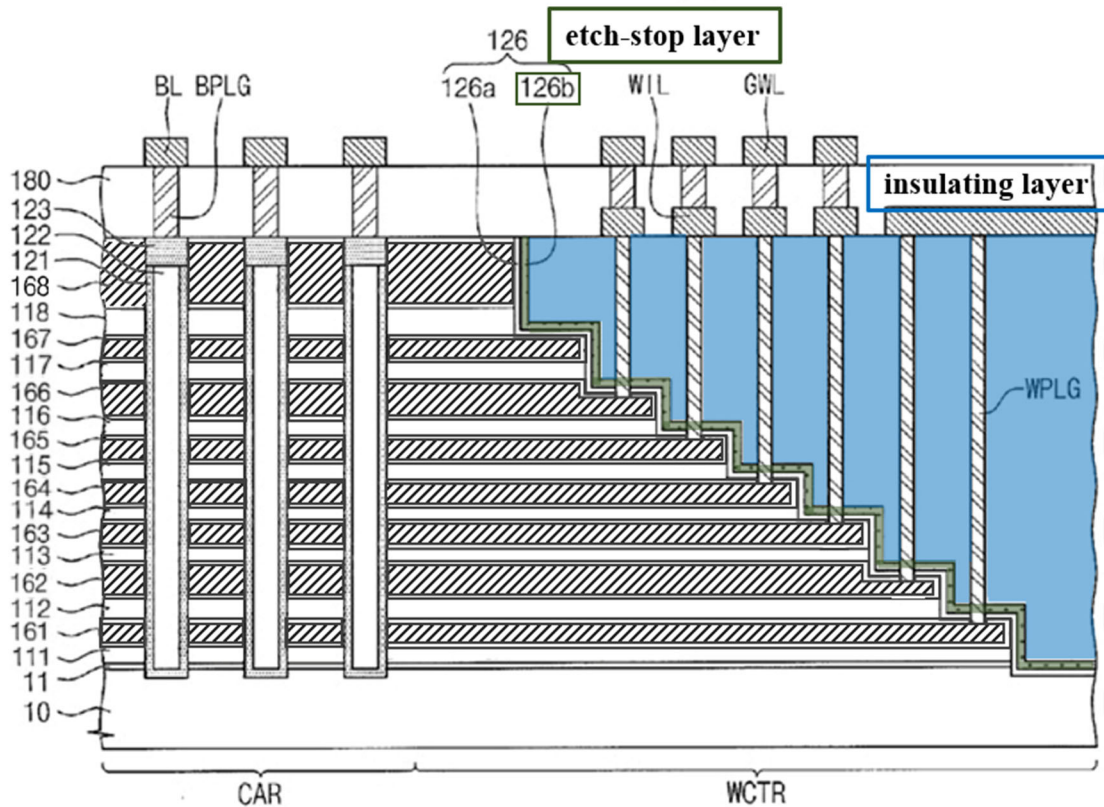
as explained, as long as the two layers comprise different materials and thus have different etching rates, both can serve the intended purpose of an etch stop.

**5. [1.D] “an insulating layer disposed on the etch-stop layer;
and”**

95. As a preliminary matter, similar to the interchangeability of reference numerals 125 and 126 for purposes of these claims, Kim’s descriptions of the interlayer dielectric 130 apply to the interlayer insulating pattern 134 in Figure 22A. The interlayer insulating pattern 134 results from the interlayer dielectric 130 after a planarization process. Ex. 1005, [0193]; *compare id.*, Fig. 18A (showing the interlayer dielectric 130) *with id.*, Fig. 19A (showing pattern 134 after planarization). A planarization process planarizes a material after deposition (planar layers are important for various reasons, for example, for reliable formation of metal layers above the stack, and depth of focus issues during lithography). Therefore, the dielectric 130 has the same material and characteristics (such as etching rate) as the pattern 134.

96. Kim discloses *an insulating layer* (“interlayer insulating pattern” 134) *disposed on the etch-stop layer* (“second stop layer” 126b):

Gate-Stack-on-Top Fig. 22A



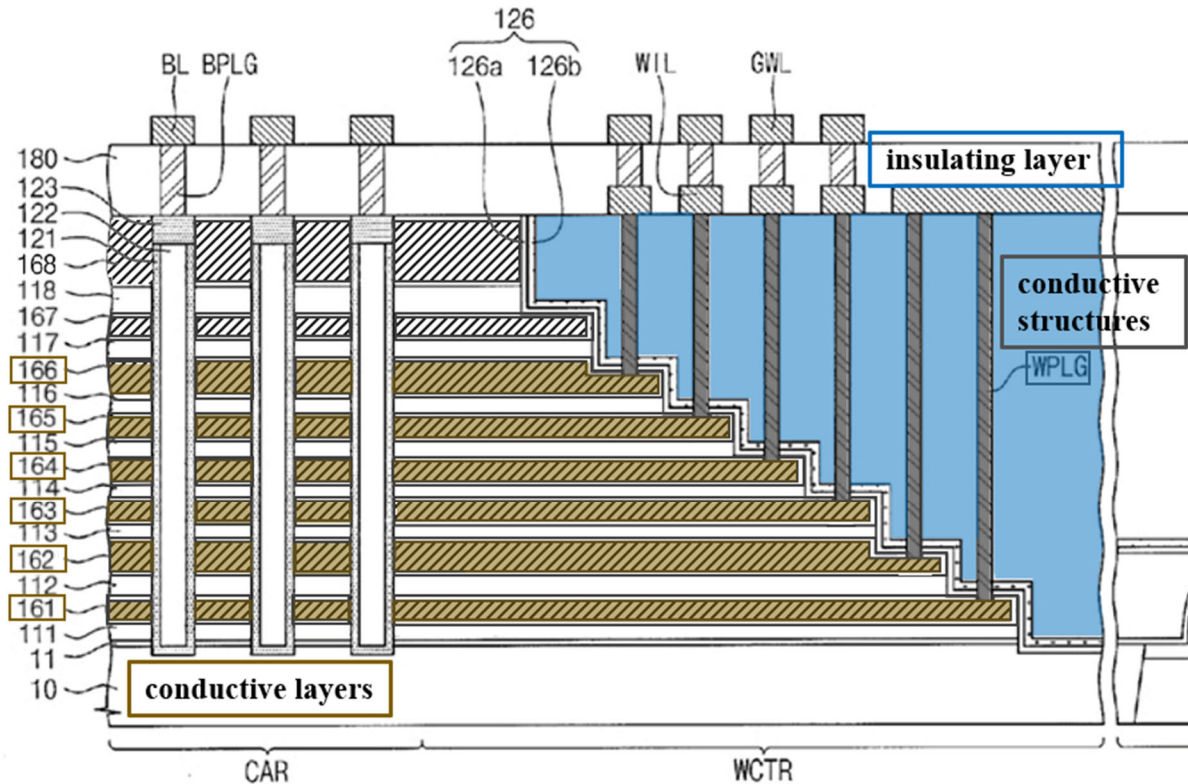
Ex. 1005, Fig. 22A, [0094], [0213] (“the interlayer dielectric 130 may be formed on the etch stop layer 125”), [0188] (same). Forming such an insulating layer was conventional and provides a planar surface for the local interconnects above that insulating layer.

6. [1.E] “a plurality of conductive structures formed in the insulating layer, wherein each conductive structure is formed on the conductive layer of the each step.”

97. Kim discloses *a plurality of conductive structures* (“word line contact plugs WPLG[s]”) *formed in the insulating layer* (“interlayer insulating pattern” 134), *wherein each conductive structure* (“WPLG”) *is formed on the conductive*

layer (corresponding one of the “gate electrodes” 161-166) *of the each step*:

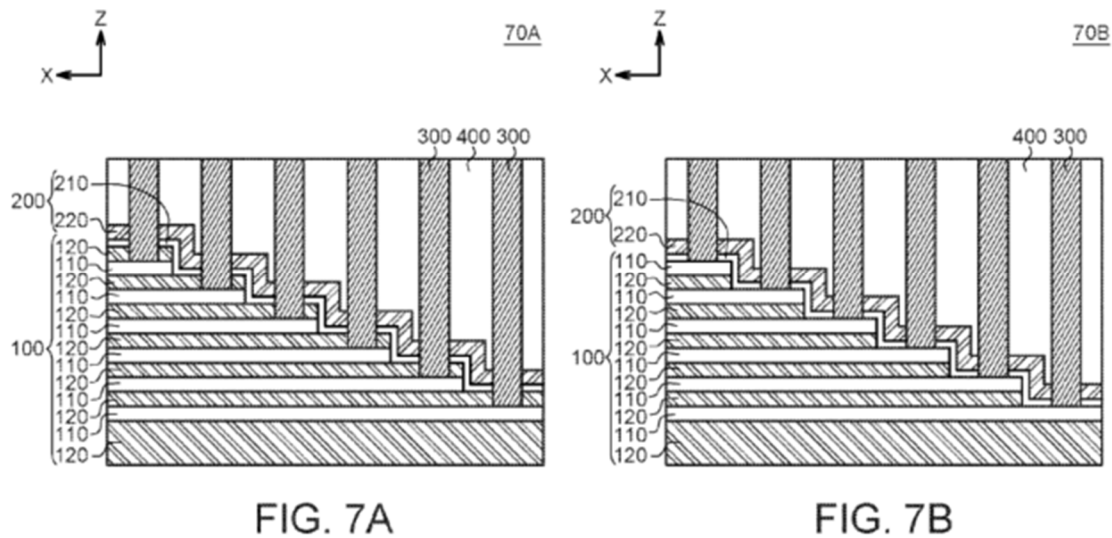
Gate-Stack-on-Top Fig. 22A



Ex. 1005, Fig. 22A, [0173]-[0174] (“the formation of word line contact plugs WPLG ... may include forming contact holes to penetrate the interlayer insulating pattern 134 ..., and filling the contact holes with a conductive material.”), [0210]-[0211] (“WPLG may be formed to connect the global word lines GWL and the gate electrodes 161 to 168”). Again, these word line contact plugs are commonly known as staircase contacts. And these staircase contacts were very well known. They were a prototypical component of 3D NAND memory devices.

98. With reversed layer ordering, that is, when the gate stack is disposed over the dielectric layer at each step, the conductive structures WPLGs are still formed on the respective gate electrodes. This is necessary because the function of the WPLGs is to electrically connect the gate electrodes with global word lines GWL, as a POSITA would have known. Ex. 1005, [0175], [0210], [0251]-[0252]. On the other hand, it is unnecessary for the WPLGs to reach the lower layer (the dielectric layer) in the reversed order. In other words, *each conductive structure* (“WPLG”) *is formed on the conductive layer* (corresponding one of the “gate electrodes” 161-166). Again, these word line contact plugs (*i.e.*, staircase contacts) physically contact, and thereby electrically couple to, the gate portion of the step, providing the electrical connection to the word line.

99. A POSITA would have known that the contact between the conductive word-line structures (such as Kim’s WPLGs) and the conductive layers stays the same regardless of the dielectric layer/gate stack ordering. For example, Chen discloses both orders:



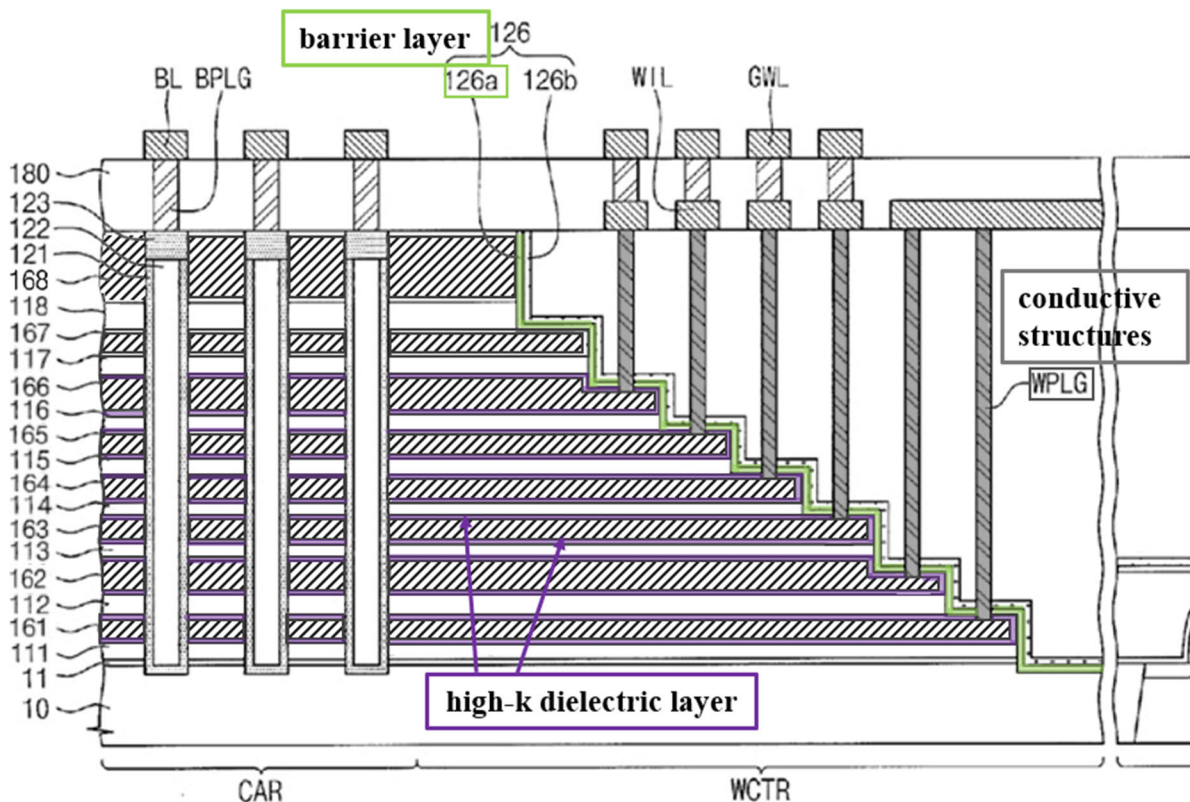
Ex. 1008, Figs. 7A (insulating layers 120 on top), 7B (conductive layers 110 on top). In both embodiments, each conductive structure 300 is formed on, and contacts, a respective conductive layer 110. *Id.*, [0045]-[0046]. As discussed, this contact is needed for the functioning of the control gate. On the other hand, as shown in Figure 7B, when the conductive layers are on the top of each step, the conductive structures 300 do not penetrate the conductive layers to reach the lower dielectric layers. In fact, were the conductive structures to penetrate the lower dielectric layers, the conductive structure may also pierce through to the underlying conductive gate, which is a well-known punch-through problem that a POSITA would have taken measures (such as etch stops) to protect from occurring.

C. Claim 2:

1. [2] “The semiconductor structure of claim 1, wherein the plurality of conductive structures extend through the barrier layer and the high-k dielectric layer.”

100. Kim discloses that *the plurality of conductive structures* (“WPLG[s]”) *extend[s] through the barrier layer* (“first stop layer” 126a) *and the high-k dielectric layer* (“blocking insulating layer” 150c):

Gate-Stack-on-Top Fig. 22A



Ex. 1005, Fig. 22A, [0174] (“the word line contact plugs WPLG ... may be formed to penetrate ... the data storing layer 150...”), [0187] (addressing etch characteristic of the first stop layer). This extension through the barrier layers and the high-k

dielectric layer would be achieved through a single- or dual-stage etching process, depending on the materials in the layers and the selected etchant(s).

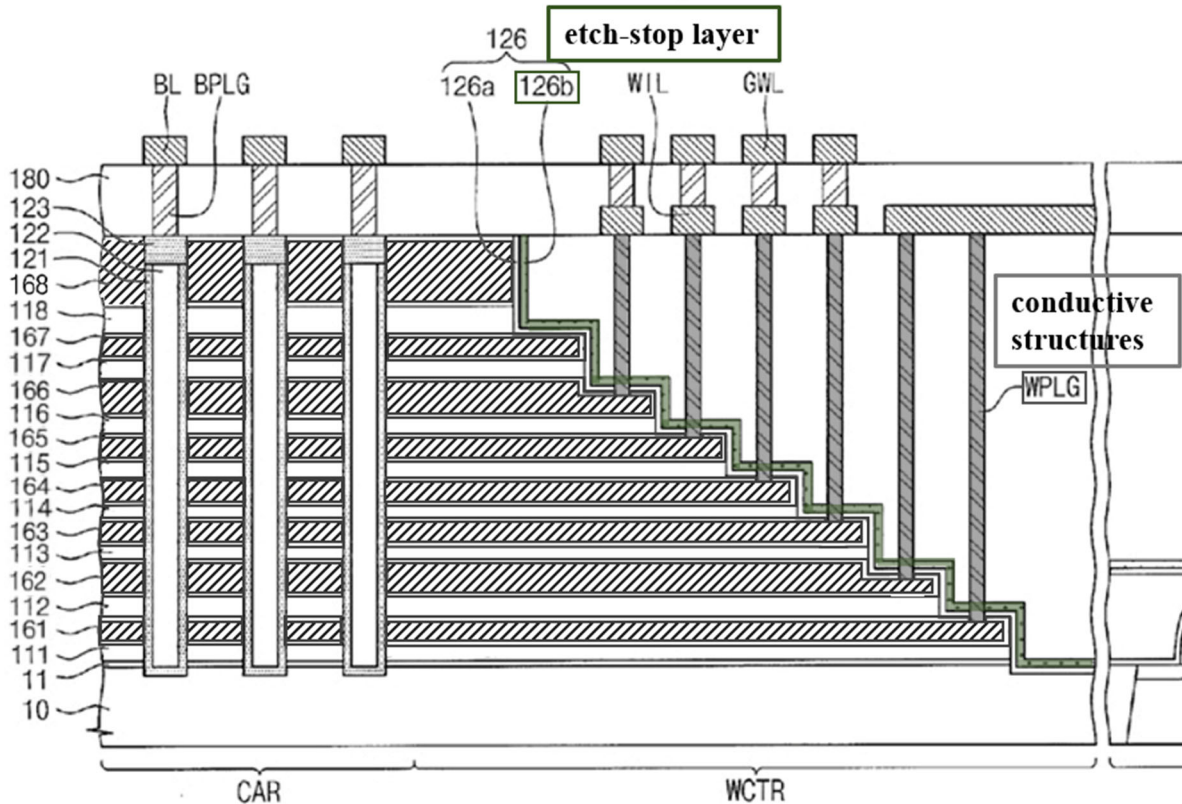
101. The WPLG “connect[s] the global word lines GWL and the gate electrodes.” Ex. 1005, [0210]-[0211]. Therefore, it is necessary for the WPLG to extend through the first stop layer and the blocking insulating layer to reach the gate electrodes regardless of the layer ordering. §§XIII.A, XIII.B.6 (a POSITA’s knowledge). Put simply, if the conductive structure did not extend through these layers, it would not contact the conductive gate layer, and the device would not be functional for the same reasons that I explain with respect to including staircase contacts for each gate layer.

D. Claim 3:

1. [3] “The semiconductor structure of claim 1, wherein the plurality of conductive structures extend through the etch-stop layer.”

102. Kim discloses that *the plurality of conductive structures* (“WPLG[s]”) *extend[s] through etch-stop layer* (“second stop layer” 126b):

Gate-Stack-on-Top Fig. 22A



Ex. 1005, Fig. 22A, [0187] (addressing etch characteristic of the second stop layer). Again, a POSITA would have understood that, to perform their function, the conductive structures must penetrate the etch-stop layer to reach the conductive layers. §XIII.C.1 (electrical-connection requirement). Again, if the conductive structure did not extend through the layers above the conductive gate portion, it would not contact the conductive gate layer, and the device would not be functional for the same reasons that I explained with respect to including staircase contacts for each gate layer.

E. Claim 4:

1. [4] **“The semiconductor structure of claim 1, wherein the barrier layer comprises silicon oxide.”**

103. Kim discloses that *the barrier layer* (“first stop layer” 125a/126a) *comprises silicon oxide*. Ex. 1005, [0187] (“the first stop layer 125a may be formed of silicon oxide....”). As explained, etching processes have great flexibility. For example, either a selective process or a reverse selective process may be used. §VIII. Therefore, as long as neither the etch-stop layer above nor the gate stack below the barrier layer comprise silicon oxide, a silicon oxide barrier layer can serve its intended function of an etch stop. I explained above that layer 125a and pattern 126a are equivalent for purpose of these claims. §XIII.B.3. Relevant here, the material in the layer does not change in the process of planarizing layer 125a to become layer 126a.

F. Claim 5:

1. [5] **“The semiconductor structure of claim 1, wherein the etch-stop layer comprises one or more of silicon nitride, a spin-on-dielectric, and a high-k dielectric.”**

104. Kim discloses that *the etch-stop layer* (“second stop layer” 125b/126b) *comprises ... silicon nitride*. Ex. 1005, [0187] (“the second stop layer 125b may be formed of silicon nitride.”). As explained, etching processes have much flexibility. For example, either a selective process or a reverse selective process may be used. §VIII. Therefore, as long as neither the insulating layer above nor the barrier layer

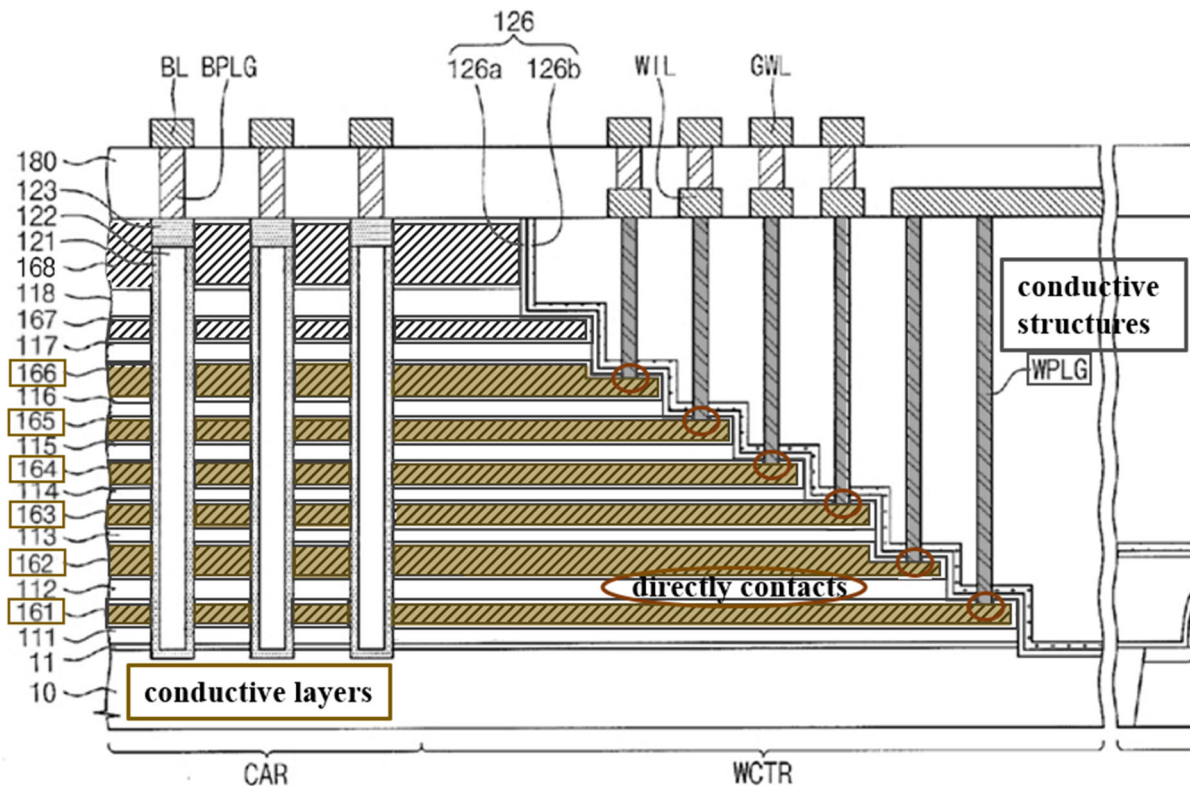
below the etch-stop layer comprise silicon nitride, a silicon nitride etch-stop layer can serve its intended function. And as just explained, the material in the layer does not change in the process of planarizing layer 125b to become layer 126b. §XIII.B.3 (equivalence of 125b and 126b).

G. Claim 6:

1. [6] “The semiconductor structure of claim 1, wherein the each conductive structure directly contacts a corresponding one of the conductive layer of the each step.”

105. Kim discloses that *the each conductive structure* (“WPLG”) *directly contacts a corresponding one of the conductive layer* (corresponding one of “gate electrodes” 161-166) *of the each step*:

Gate-Stack-on-Top Fig. 22A

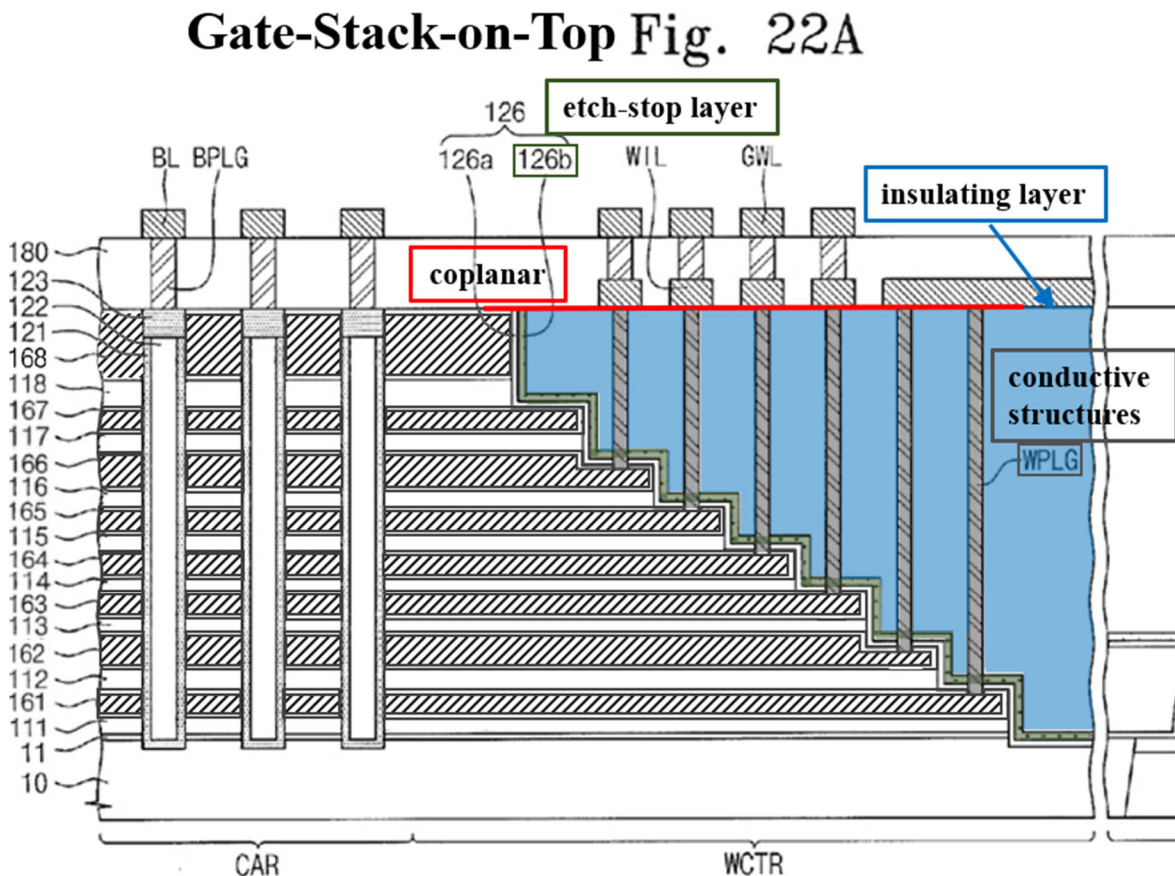


Ex. 1005, Fig. 22A. The WPLG “connect[s] the global word lines GWL and the gate electrodes.” *Id.*, [0210]-[0211]. The direct contacts between WPLGs and gate electrodes establish those connections. Again, a POSITA would have known this to be necessary for the functioning of the word lines. §§XIII.A, XIII.B.6 (a POSITA’s knowledge). And again, it would risk punch-through to extend through the gate layer into the underlying dielectric.

H. Claim 7:

1. [7] “The semiconductor structure of claim 1, wherein top surfaces of the plurality of conductive structures, the insulating layer, and a portion of the etch-stop layer are coplanar.”

106. Kim discloses that *top surfaces of the plurality of conductive structures* (“WPLG[s]”), *the insulating layer* (“interlayer insulating pattern” 134), and *a portion of the etch-stop layer* (“second stop layer” 126b) *are coplanar*:



Ex. 1005, Fig. 22A. A planar surface at the top of the structure is beneficial to further manufacturing stages because, for example, materials tend to be deposited, patterned and etched more easily on a planar surface, resulting in greater reliability.

107. Kim discloses planarizing the interlayer dielectric 130, which can “expose the top surface of the [staircase structure]” and result in “the interlayer insulating pattern 134 having a flat top surface.” Ex. 1005, [0103], [0193]. The flat top surface is the coplanar surface as shown above.

108. The top surfaces of WPLG, the interlayer insulating pattern 134, and the second stop layer 126b, as shown in the figure above, meet the plain and ordinary meaning of “top surface” as a POSITA would understand from the ’711 Patent. For example, the coplanar surface observably includes the upper boundaries *of conductive structures* (“WPLG[s]”), *the insulating layer* (“interlayer insulating pattern” 134), *and a portion of the etch-stop layer* (“second stop layer” 126b).

I. Claim 8:

1. [8] “The semiconductor structure of claim 1, wherein the plurality of conductive structures comprise one or more of tungsten, cobalt, nickel, copper, and aluminum.”

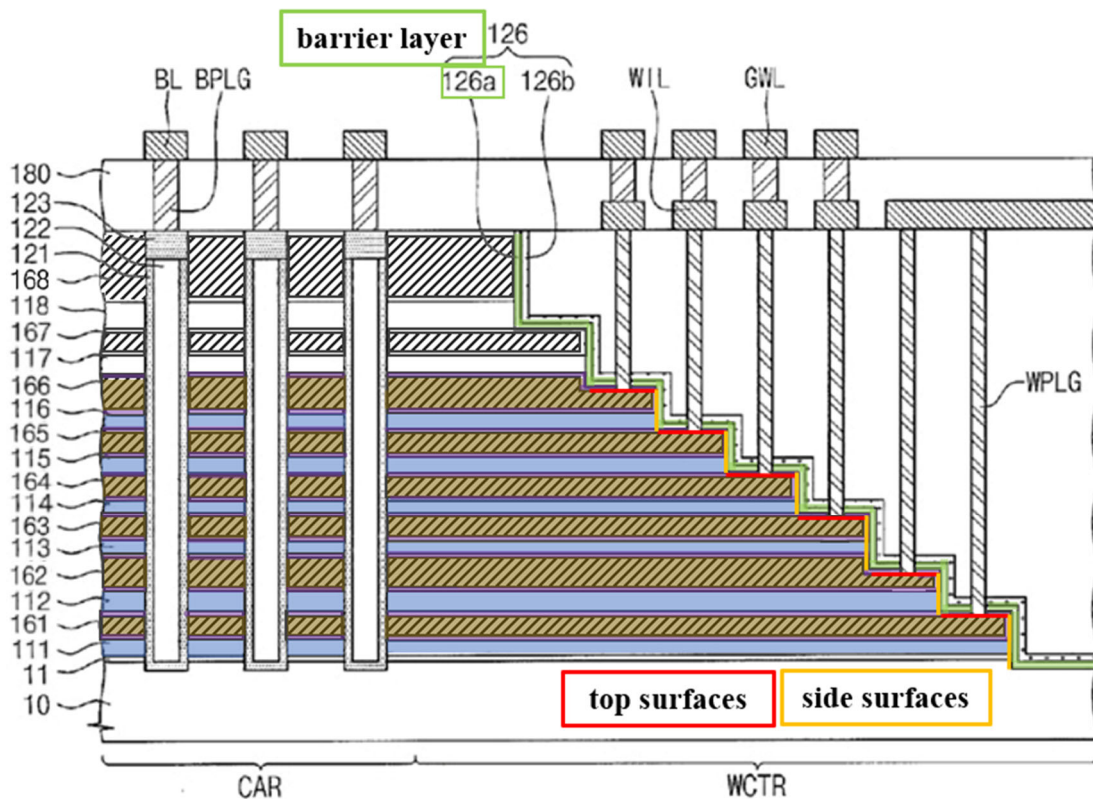
109. Kim discloses that *the plurality of conductive structures* (“WPLG[s]”) *comprise[s] ... tungsten*. Ex. 1005, [0173] (“the word line contact plugs WPLG ... may be formed of a metallic material (*e.g.*, tungsten).”). Tungsten is widely used in 3D memory devices because it is a harmless metal, that is, it does not diffuse like gold or copper. Metal diffusion can damage surrounding elements. As explained above, descriptions of Figures 5A-14B apply to Figure 22A. §XII.A.

J. Claim 9:

1. [9] “The semiconductor structure of claim 1, wherein the barrier layer is formed on side and top surfaces of the plurality of steps.”

110. Kim discloses that *the barrier layer* (“first stop layer” 126a) *is formed on side and top surfaces of the plurality of steps:*

Gate-Stack-on-Top Fig. 22A



Ex. 1005, Fig. 22A. Kim discloses that “[t]he first stop layer 125a may be formed to conformally cover an exposed surface of the stacked layer structure ST.” *Id.*, [0187]. Kim also teaches that “a conformal layer has substantially the same shape as the surface it covers....” *Id.*, [0144]. Together, these statements disclose that the

first stop layer 125a/126a covers the risers (side surfaces) and treads (top surfaces) of the plurality of steps. *Id.*, [0185], [0213] (“the interlayer dielectric 130 may be formed on the etch stop layer 125....”). Conformal coating had been known in the art for decades and was commonly used in semiconductor manufacturing.

K. Claim 11:

1. [11] “The semiconductor structure of claim 1, wherein the high-k dielectric layer comprises hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, or a combination thereof.”

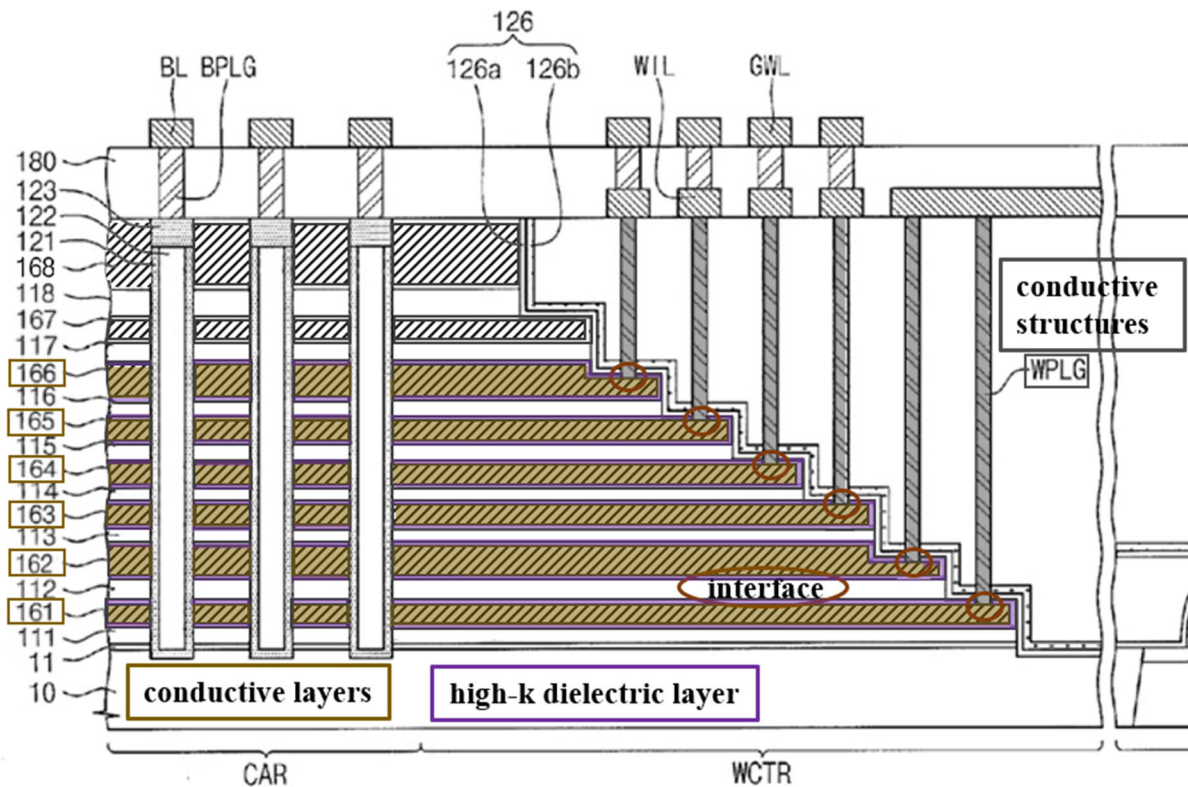
111. Kim discloses that *the high-k dielectric layer* (“blocking insulating layer” 150c) *comprises hafnium oxide, zirconium oxide, aluminum oxide, [or] tantalum oxide....* Ex. 1005, [0151] (“The blocking insulating layer 150c may include ... [a] high-k dielectric, ... e.g., tantalum oxide, ... , hafnium oxide, zirconium oxide, [or] aluminum oxide....”). As explained, the high-k dielectric layer is deposited when the channel is coated. §XIII.B.2. Therefore, the selection of material for this layer is determined by considerations related to channel formation.

L. Claim 12:

1. [12] “The semiconductor structure of claim 1, wherein top and bottom surfaces and a sidewall of the conductive layer are covered by the high-k dielectric layer, except at an interface between the conductive layer and the conductive structure.”

112. Kim discloses that *top and bottom surfaces and a sidewall of the conductive layer* (“gate electrodes” 161-166) *are covered by the high-k dielectric layer* (“blocking insulating layer” 150c), *except at an interface between the conductive layer and the conductive structure* (corresponding “WPLG”):

Gate-Stack-on-Top Fig. 22A



Ex. 1005, Fig. 22A.

113. The high-k dielectric layer is deposited during channel formation. §XIII.B.2. Kim describes this process of forming blocking insulating layer around the gate electrode. During the formation of the gate stack, “the data storing layer 150 [comprising blocking insulating layer 150c] may be formed to conformally cover ... the recess regions 142” between the insulating (dielectric) layers 111-116. Ex. 1005, [0200], [0202]. Recess regions 142 are created by etching away sacrificial layers SC1-SC8 as a first step of replacing the sacrificial layers with gate stacks. *Id.*, [0200]. “Thereafter, the gate electrodes 161 to 16[6] may be formed in ... the [respective] data storing layer 150.” *Id.*, [0202]. Then an opening is etched through the insulating layer, the etch-stop layer, the barrier layer, and an interface in the blocking insulating layer 150c to form a vertical opening. The opening is filled and becomes a WPLG. Penetrating these layers including through the interface in the blocking insulating layer is necessary so that WPLGs “may be formed to connect the global word lines GWL and the gate electrodes.” *Id.*, [0210]-[0211]. Again, this would have been within the knowledge of a POSITA.

114. A POSITA would have found it obvious that the layer ordering would not change the spatial relationship of gate electrodes and blocking insulating layer. For example, because the WPLG “connect[s] the global word lines GWL and the gate electrodes,” (Ex. 1005, [0210]-[0211]) the blocking insulating layer would not cover *an interface between the conductive layer* (“gate electrodes” 161-166) *and the*

conductive structure (corresponding “WPLG”). A POSITA would have known this to be true, for example, through the prior art references cited above. §§XIII.A, XIII.B.6 (a POSITA’s knowledge).

M. Claim 13:

1. [13.PRE] “A semiconductor structure, comprising:”

115. This preamble is identical to that of claim 1. Kim discloses it for the same reason as explained above. §XIII.B.1.

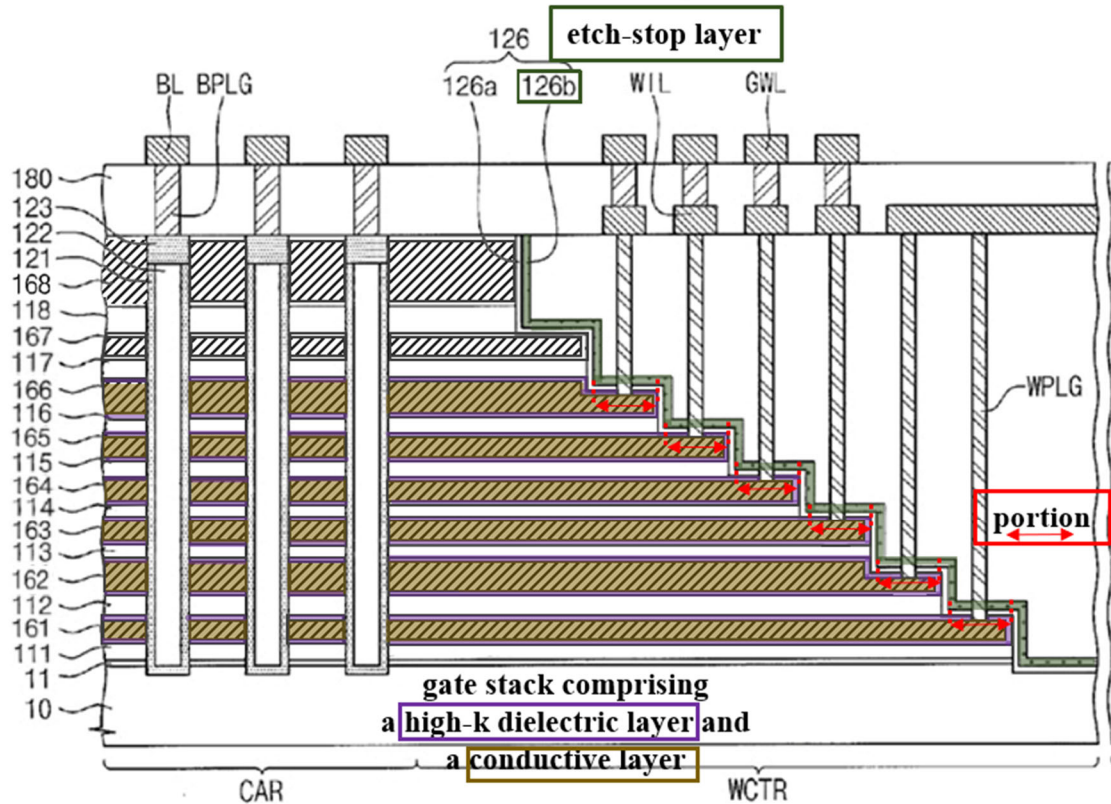
2. [13.A] “a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;”

116. This limitation is identical to [1.A]. Kim at least renders it obvious for the same reason as explained above. §XIII.B.2.

3. [13.B] “an etch-stop layer disposed on a portion of the gate stack of the each step;”

117. Kim discloses *an etch-stop layer* (“second stop layer” 126b) *disposed on a portion of the gate stack* (one of “gate electrodes” 161-166 and “blocking insulating layer” 150c) *of the each step*:

Gate-Stack-on-Top Fig. 22A



Ex. 1005, Fig. 22A. The *portion* is the exposed top surface or the tread of each step.

118. The '711 Patent defines “on” to include both directly on something and indirectly on that something. Ex. 1001, 4:1-6. Accordingly, Kim discloses limitation [13.B] even though the first stop layer 126a is positioned between the second stop layer 126b and the gate stack. Indeed, the '711 Patent has the same configuration. *Id.*, Figs. 9A-9B.

4. [13.C] “an insulating layer disposed on the etch-stop layer; and”

119. This limitation is identical to [1.D]. Kim discloses it for the same reason as explained above. §XIII.B.5.

5. [13.D] “a plurality of conductive structures formed in the insulating layer and extending through the etch-stop layer and the high-k dielectric layer, wherein each conductive structure directly contacts the corresponding conductive layer of each step.”

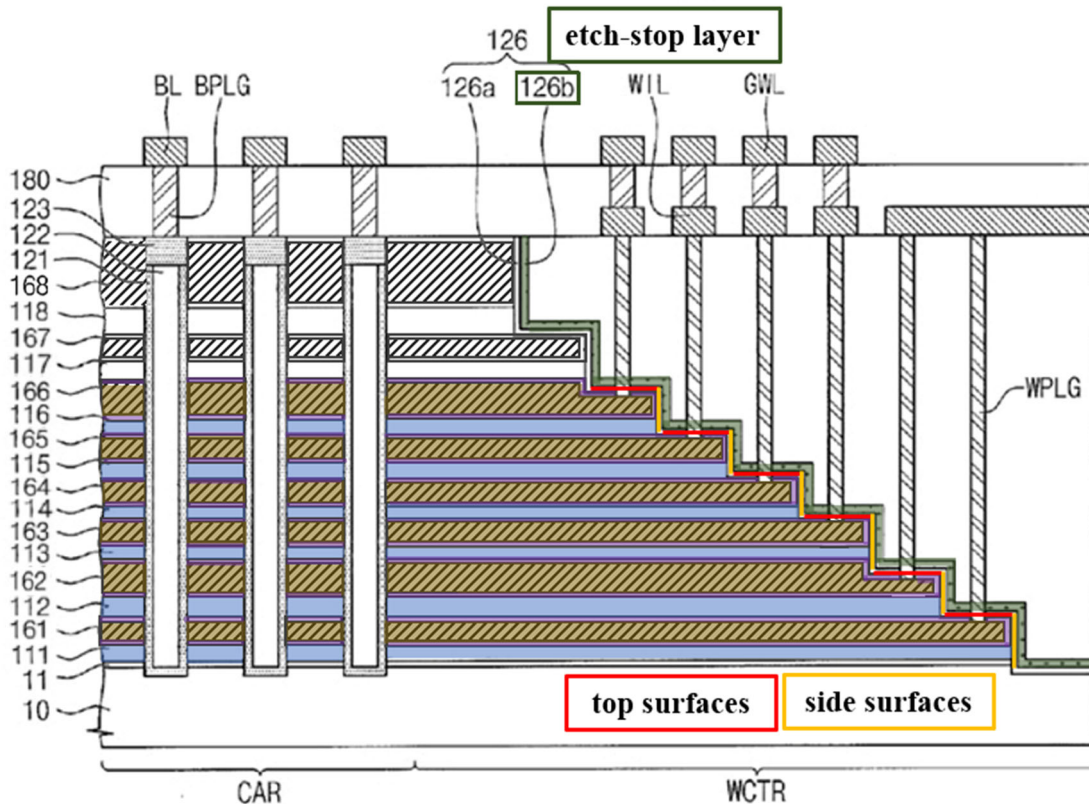
120. This limitation combines the requirements of limitation [1.E] and claims 2, 3, and 6. Kim at least renders it obvious for the same reason as explained above. §§XIII.B.6, XIII.C.1, XIII.D.1, XIII.G.1.

N. Claim 14:

1. [14] “The semiconductor structure of claim 13, wherein the etch-stop layer is formed on a side surface and a top surface of each step.”

121. Kim discloses that *the etch-stop layer* (“second stop layer” 126b) *is formed on a side surface and a top surface of each step*:

Gate-Stack-on-Top Fig. 22A



Ex. 1005, Fig. 22A.

122. As explained with respect to claim 9, Kim discloses that the first stop layer 125a (the barrier layer) is formed on side and top surfaces of the plurality of steps. §XIII.J.1. Kim further discloses that “the second stop layer 125b may be conformally formed on the first stop layer 125a.” Ex. 1005, [0187]. And “a conformal layer has substantially the same shape as the surface it covers....” *Id.*, [0144]. Thus, *the etch-stop layer* (second stop layer 126b) *is formed on a side surface and a top surface of each step.* *Id.*, [0256]. Conformal coating had been known in the art for decades and was commonly used in semiconductor

manufacturing. Again, “*on something*” in the ’711 Patent includes both directly and indirectly on that something. Ex. 1001, 4:1-6.

O. Claim 15:

1. [15] “The semiconductor structure of claim 14, wherein thicknesses of the etch-stop layer is the same on the side and top surfaces of each step.”

123. Kim discloses the additional limitation of claim 15.

124. Kim discloses that “the second stop layer 125b may be conformally formed on the first stop layer 125a.” Ex. 1005, [0187]. Further, “a conformal layer ... has substantially the same thickness throughout.” *Id.*, [0144]. Thus, *thicknesses of the etch-stop layer* (second stop layer 125b/126b) *is the same on the side and top surfaces of each step*. Again, conformal coating had been known in the art for decades and was commonly used in semiconductor manufacturing.

P. Claim 16:

1. [16] “The semiconductor structure of claim 13, wherein the etch-stop layer comprises one or more of silicon nitride, a spin-on-dielectric, and a high-k dielectric.”

125. The additional limitation of claim 16 is identical to that of claim 5. Kim discloses it for the same reason as explained above. §XIII.F.1.

Q. Claim 18:

1. [18] **“The semiconductor structure of claim 13, wherein the high-k dielectric layer comprises hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, or a combination thereof.”**

126. The additional limitation of claim 18 is identical to that of claim 11.

Kim discloses it for the same reason as explained above. §XIII.K.1.

R. Claim 19:

1. [19] **“The semiconductor structure of claim 13, wherein top and bottom surfaces and a sidewall of the conductive layer are covered by the high-k dielectric layer, except at an interface between the conductive layer and the conductive structure.”**

127. The additional limitation of claim 19 is identical to that of claim 12.

Kim discloses it for the same reason as explained above. §XIII.L.1.

XIV. GROUND 2: KIM IN VIEW OF FANG

A. Claim 10:

1. [10] **“The semiconductor structure of claim 1, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.”**

128. Kim at least renders obvious claim 1. §XIII.B. Kim in view of Fang renders obvious dependent claim 10.

129. To begin, as the Examiner took official notice, the claimed etch-stop layer thickness “[wa]s notoriously well known in the art.” Ex. 1002, 156. Moreover, the cited range—spanning three orders of magnitude—“lacks criticality.” *Id.* (citing

the equivalent of Ex. 1001, 7:56-8:19). The Examiner was right. Nothing in the '711 Patent disclosure teaches or even suggests why this wide range was chosen, what performance advantage it offered, or how a sub-range within might be suitable for one configuration or application. Furthermore, the '711 Patent claims the same wide thickness range whether or not the claimed structure includes a barrier layer. *Compare* Ex. 1001 claim 10 *with* claim 17. As discussed, the barrier layer of the '711 Patent is simply another etch-stop layer. Thus, the fact that the patent claims the same etch-stop thickness range with and without a barrier layer indicates that the range is not critical.

130. If more is required, Kim in view of Fang's etch-stop layer teaching renders claim 10 obvious. Fang discloses an analogous semiconductor structure with an etch-stop layer. Ex. 1007, Fig. 6, [0020]. To start, Kim's and Fang's etch-stop layers are similar. For example, both of their etch-stop layers may comprise the same material, silicon nitride. Ex. 1005, [0187], Ex. 1007, [0022]. Fang's etch-stop layer "may be formed by conventional techniques...." Ex. 1007, [0020]. It would have been obvious to a POSITA that such conventional techniques could be applied to form Kim's etch-stop layer. Additionally, Fang's disclosed thickness range may be adjusted based on Kim's staircase structure. Fang's layer "may be formed over the stairs 125 at a thickness ranging from about 50 Å to about 1000 Å." *Id.*, [0021]. That is equivalent to about 5 nm to 100 nm. This etch stop layer thickness

withstands etching of contact holes with depths “from about 1 μm to about 15 μm .” *Id.*, [0030]. The height of Kim’s staircase structure, and therefore the approximate depth of its deepest contact hole, ranges from “about 10,000 Å to about 40,000 Å,” which is about 1 μm to about 4 μm . Ex. 1005, [0068]. Etch processes often can be designed to have selectivities of 10 to 100 or higher. The required selectivity depends on the thickness of the layer being etched and the thickness of the etch barrier. In addition, as described earlier, a POSITA would have known how to account for variabilities of layer thicknesses and etch rates in determining the minimum required selectivity. Thus, a POSITA would have found it obvious that Fang’s disclosed maximum thickness may be scaled proportionally to 26.7 nm ($100\text{ nm} / 15\text{ }\mu\text{m} * 4\text{ }\mu\text{m}$) to account for the shallower holes required for Kim’s staircase structure when applying those teachings to specify Kim’s etch-stop thickness. This linear scaling based on etching rate would have been well within the skill of a POSITA. Additional techniques such as adjusting etchant type could have provided more flexibility in working with a specified range of etch stop thickness. A POSITA would have understood this is why the ’711 Patent does not explain the wide claimed range of thickness. Additionally, as explained below with respect to Park, the ’711 Patent does not even have a range for the height of its staircase structure and thus the depths of its contact holes. §XVI.B.1. This further confirms that the claimed range is not critical but is flexible. In any event, the thickness range

of 5 to 26.7 nm overlaps with the claimed *range between 10 nm and 1000 nm*. Thus, Kim in view of Fang renders claim 10 obvious.

131. Fang has two etch-stop layers while Kim has one. To the extent the thickness of Fang's etch-stop layer might be reduced to account for Kim's extra etch-stop layer when adapting Fang's etch-stop thickness to Kim's structure, a POSITA would have found it obvious that the thickness would still overlap with the claimed *range between 10 nm and 1000 nm*. This reduction may be done, for instance, to maintain a total etch resistance between two etch-stop layers or one, however many is present in the structure. For example, a POSITA would have found it unnecessary to reduce the maximum range of 26.7 nm to below 10 nm, which is the reduction required to avoid any overlap with the claimed thickness range, to account for one extra etch-stop layer. And again, there is flexibility in the thickness because other process parameters can be adjusted for the etch-stop layer to work within a thickness range.

B. Claim 17:

1. [17] **"The semiconductor structure of claim 13, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm."**

132. The additional limitation of claim 17 is identical to that of claim 10. Kim in view of Fang renders it obvious for the same reason as explained above.

§XIV.A.1.

C. Motivation to Combine

133. It is my opinion that a POSITA would have been motivated to apply Fang's disclosure of the etch-stop-layer thickness on Kim's staircase structure.

134. Kim focuses on the issue of planarizing the interlayer dielectric to reduce the height difference between the cell array region and the peripheral circuit region. Ex. 1005, [0024]-[0025]. Therefore, Kim does not state in detail certain aspects of the word line contact region WCTR that were well-known in the art. On the other hand, Fang focuses on preventing over-etching shallower openings when etching openings for the word line conductive structures. Ex. 1007, [0004], [0008]. A POSITA would have known that Fang's focus is an important consideration for manufacturing 3D memory devices and dovetails with Kim's focus to "reduce or prevent damage[s]" to the device during manufacturing. Ex. 1005, [0027]. In a sense, Fang can be considered to disclose a building block of Kim's device. Therefore, a POSITA would have considered Fang's teaching in implementing Kim's device. Moreover, a POSITA would have known that the thickness of an etch-stop layer is a necessary (but routine) design parameter and may be important to its purpose of preventing punch-through to underlying layers. Therefore, a POSITA would have been motivated to adapt Kim's etch-stop layer based on Fang's thickness range, especially since Kim does not specify a thickness.

135. A POSITA would have had a reasonable expectation of success in applying Fang's etch-stop-layer thickness to Kim because Fang's range (5-100 nm, or 5-26.7 nm adjusted) was reasonable, especially in light of the additional flexibility provided by other process parameters as explained above. Such additional flexibility also makes the required thickness more flexible, increasing the likelihood that some thickness within the wide range claimed by the '711 Patent would work well with Kim's device. Further, a POSITA would have had a reasonable expectation of success because of similarities between Kim's and Fang's disclosures regarding the etch-stop layer. For example, Kim discloses that its "etch stop layer 125 may be formed of a material having an etch selectivity with respect to the interlayer dielectric 130." Ex. 1005, [0213]. Fang discloses the same. Ex. 1007, [0020] ("The etch stop material 130 may also be substantially resistant to dry etch chemistries used to form openings 145 [through the insulating layer] (see FIG. 5)."). Kim discloses that its "second stop layer 125b may be formed of silicon nitride." Ex. 1005, [0187]. So does Fang. Ex. 1007, [0020]. A POSITA would have expected such similarities since Kim's and Fang's devices are analogous.

136. More generally, a POSITA would have had a reasonable expectation of success because both Kim and Fang are directed to similar 3D memory devices with staircase word line structures, for example, both comprising alternating conductive and dielectric layers at each step, an etch-stop layer and an insulating layer on the

steps, and conductive structures penetrating various layers to form contacts with the conductive layers. Again, a POSITA would have expected such similarities since Kim's and Park's devices are analogous. These components and the structure itself were routine and conventional, well within the knowledge of a POSITA.

137. Indeed, all of these similarities would have confirmed a POSITA's understanding that Kim and Fang disclose analogous devices and manufacturing processes. This would have bolstered a POSITA's expectation of success.

138. If Patent Owner were to argue against the combination by alleging Kim's additional barrier layer somehow makes a difference to claims 10 and 17, Patent Owner would be contradicting the '711 Patent. The patent requires the same etch-stop-layer material and thickness for devices with or without the barrier layer. *Compare* Ex. 1001 claims 5, 10 *with* claims 16-17. This requirement is an acknowledgement of a POSITA's understanding that the barrier layer need not matter to the etch-stop thickness. For example, as explained, etching depends on multiple parameters including thickness and etchant. Therefore, by adjusting other factors, the presence or absence of the barrier need not matter to the etch-stop thickness.

XV. GROUND 3: PARK IN VIEW OF A POSITA’S KNOWLEDGE

A. Park Discloses “a Gate Stack Disposed over a Dielectric Layer”

139. Park discloses a gate stack disposed over a dielectric layer even though its figures show the opposite order. §XII.B. In addition to Park’s express teaching, a POSITA would have known that either order was a common alternative. For example, Chen discloses both orders side-by-side. §XIII.A (citing Ex. 1008).

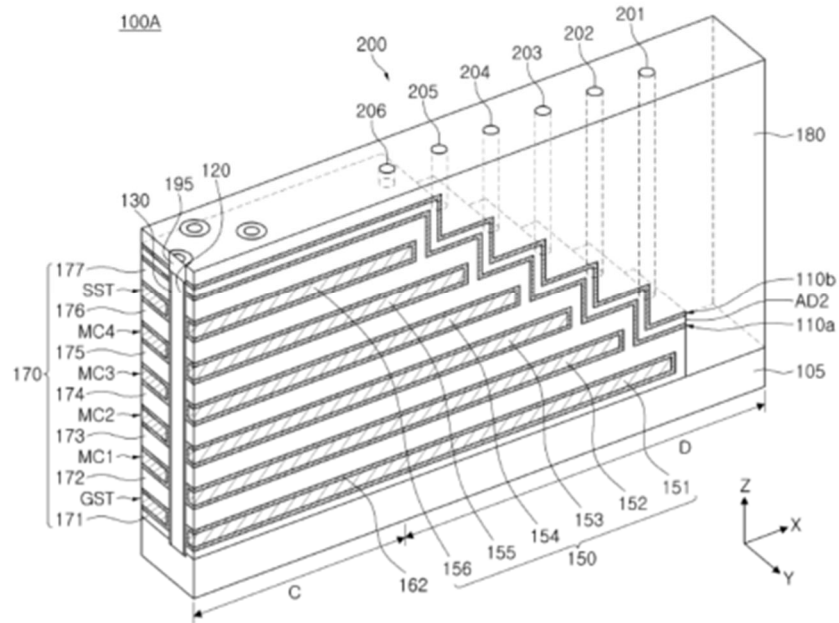
140. Below, Park’s figures are modified to show this gate-stack-on-top ordering. Based on Park’s express teaching and a POSITA’s knowledge, a POSITA could have easily visualized how the reversed order would be arranged. Doing so was well within the knowledge and skill of a POSITA. Furthermore, prior art references with gate-stack-on-top configurations would have helped a POSITA visualize a Park embodiment with gate stacks on top. §XIII.A (citing Exs. 1015-16). For clarity, the modified Park figures are annotated with “Gate-Stack-on-Top.”

B. Claim 1:

1. [1.PRE] “A semiconductor structure, comprising:”

141. Park discloses *a semiconductor structure*, such as “a nonvolatile memory device.” Ex. 1006, Summary.

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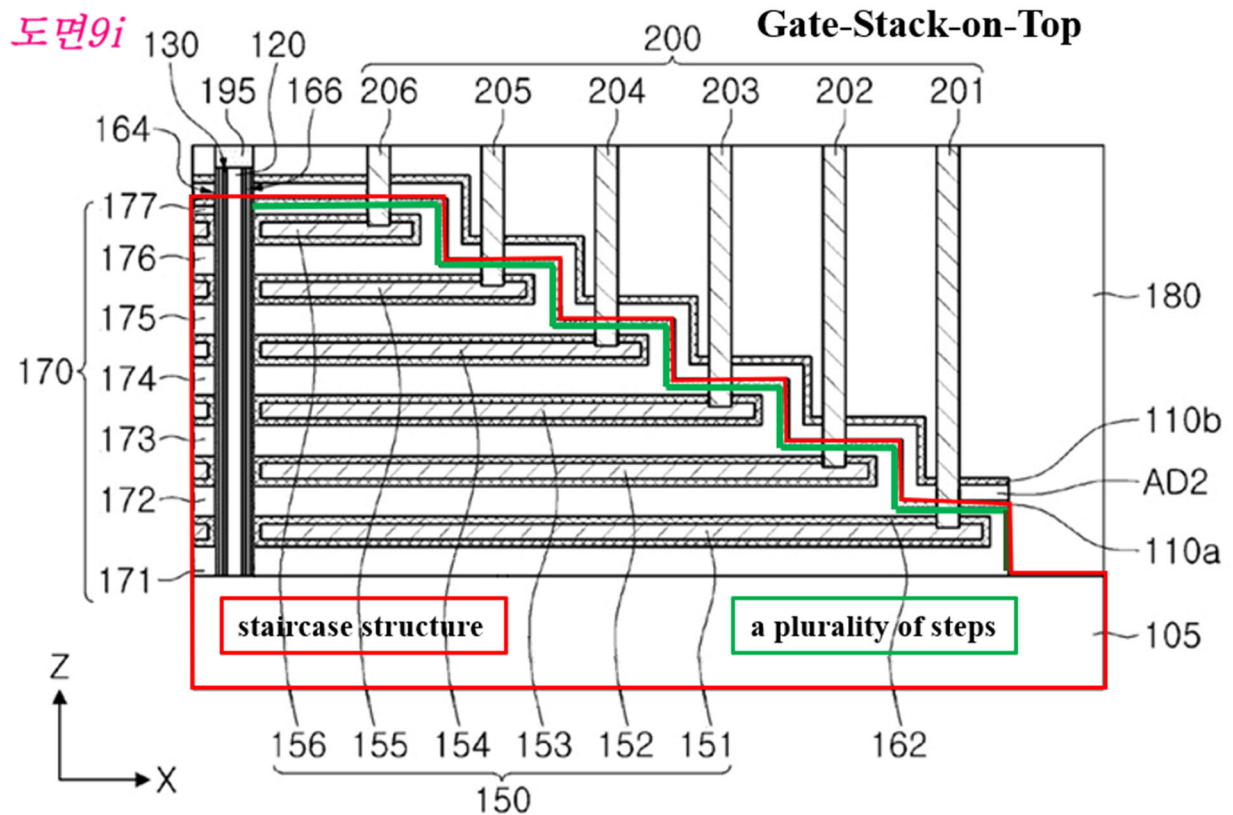


Id., Fig. 5. The word line contact staircase structure that is the focus of the '711 Patent is a prominent feature of this semiconductor structure in what Park calls the connection region (designated D in the figure).

2. [1.A] “a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;”

142. Park at least renders limitation [1.A] obvious.

143. Park’s nonvolatile memory comprises *a staircase structure comprising a plurality of steps*:

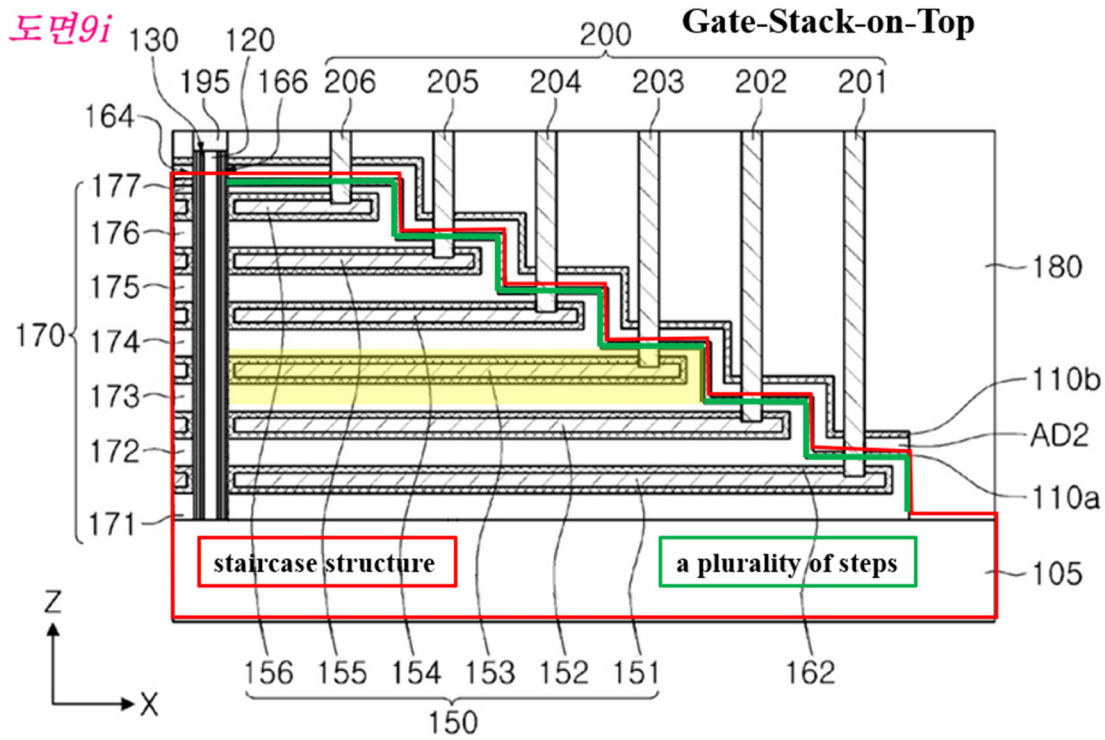


Ex. 1006, Fig. 9i, [0102] (“Each of the plurality of insulating layers (170) and sacrificial layers (140) ... forms a step with respect to another insulating layers (170) and sacrificial layers (140).”); *id.*, Summary (“a plurality of pad regions provided such that the plurality of gate electrode layers extends with different lengths along one direction”), [0004], [0036], [0042], [0081]. The steps provide landing areas for staircase contacts.

144. Park discloses that *each step comprises a gate stack disposed over a dielectric layer* (one of “insulating layers” 172-177). Further, *the gate stack compris[es] a high-k dielectric layer* (“blocking layer” 162) *and a conductive layer*

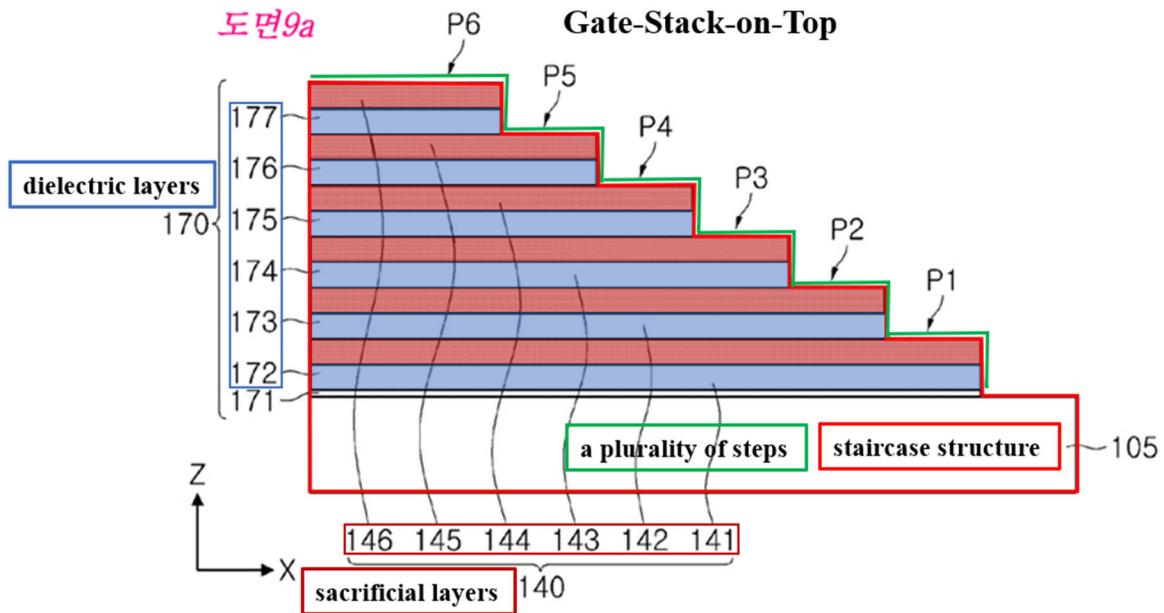
k dielectric layer typically results from depositing the data-storing layer around the channel. §XIII.B.2.

145. If Patent Owner were to argue that Park does not meet the “plurality of steps” limitation because its steps do not comprise a gate stack and a dielectric layer of the same width, Patent Owner would be wrong for several reasons. First, nothing in the claim limitation requires that the gate stack and dielectric layer be the same width. Second, even assuming Park shows gate stack and dielectric layers of different widths, it still forms a staircase. It is obvious which gate stack and dielectric layer are paired to form a step, namely, the gate stack and the immediately below dielectric layer, both of which are within the height range of the side surface or riser of one step. One such pair is shaded below:



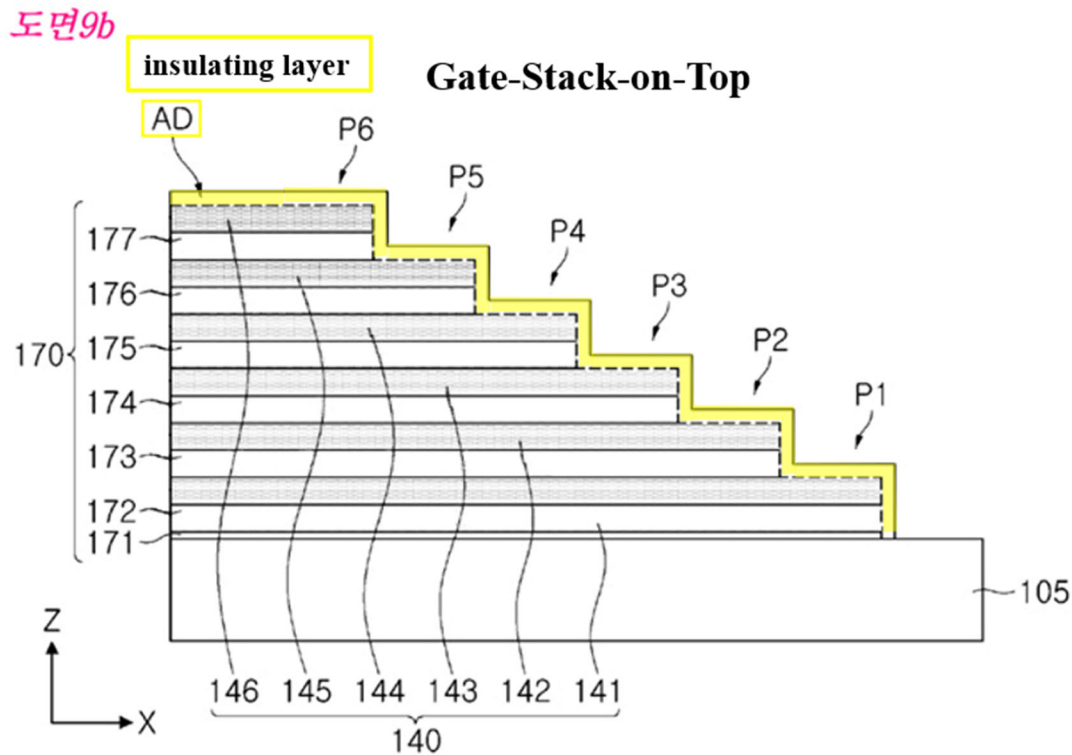
Ex. 1006, Fig. 9i. This ordinary understanding of “step” is consistent with the ’711 Patent, which does not define a “step” to require two layers of the same length. *See generally* Ex. 1001.

146. Third, and regardless, Park plainly describes gate stacks and dielectric layers of the same width. The '711 Patent explains that each step, including its lateral dimension, is configured by one cycle of an etch-and-trim process. Ex. 1001, 6:53-67, 7:13-22, 12:3-10. That refers to the process of forming the steps using a mask that is trimmed to expose more staircase area to be trimmed after each cycle of forming an additional step and lowering existing steps. The description of the '711 Patent matches exactly Park's process of forming the staircase structure:



Ex. 1006, Fig. 9a, [0102]. As shown, each respective pair of dielectric layers 172-177 and sacrificial layers 141-146 has the same width after the etch-and-trim process, consistent with “step” of the ’711 Patent. Each sacrificial layer is subsequently replaced with a gate stack. *Id.*, Figs. 9f-9g, [0104]-[0105].

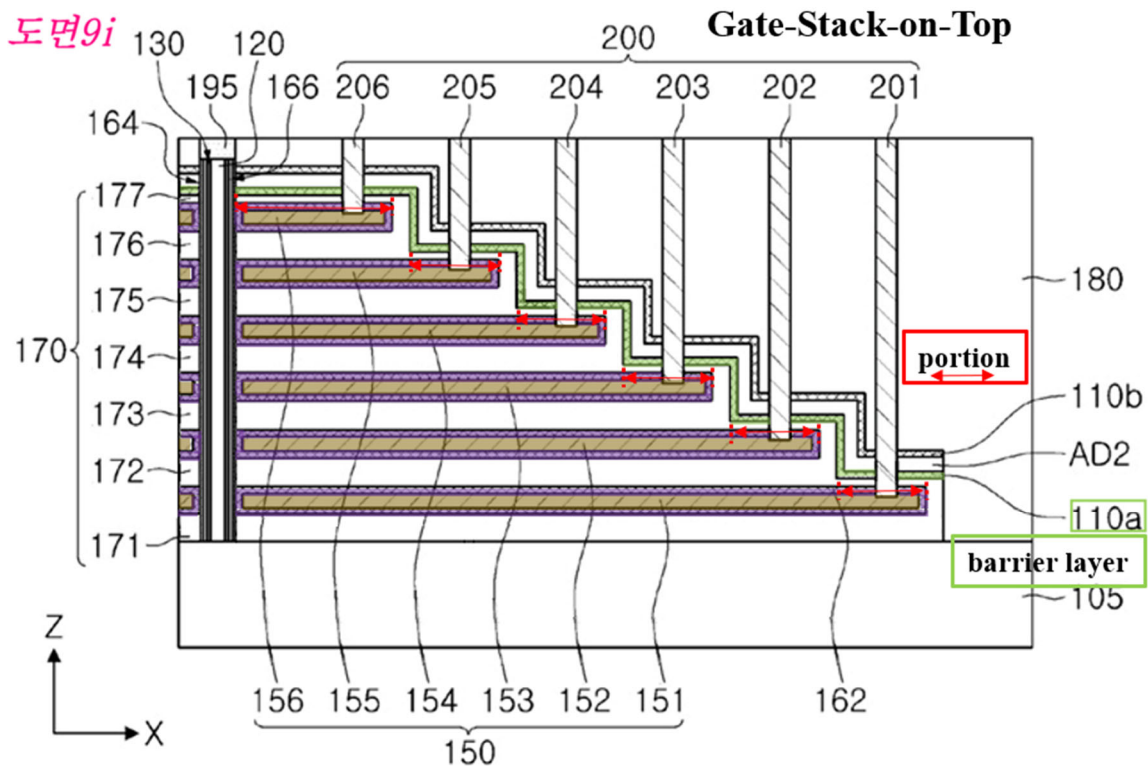
147. Park discloses optionally depositing additional insulation (layer AD) onto the staircase, which laterally extends the dielectric material. But that disclosure is irrelevant, because this limitation is a *comprising* limitation, which I understand to be open-ended and permits additional components or elements. An option to add dielectric material to the steps doesn’t change the fact that the gate stacks and dielectric layers had the same width before layer AD was deposited.



Ex. 1006, Fig. 9b, [0103]. Furthermore, Park does not say layer AD must be deposited. To the contrary, Park explains that layer AD is optional. *Id.*, [0103] (“When multiple pad regions (P1-P6) are in place, an insulating layer (AD) *can* be further formed on the pad region (P1-P6).”) (emphasis added). A POSITA would have known that layer AD can be omitted without affecting the functioning of the device. A POSITA would have known this through, for example, many prior art reference that do not teach such an additional layer. By omitting this optional insulating layer, each step would comprise a gate stack and a dielectric layer of the same width (which, again, is not a requirement of the claim).

3. [1.B] “a barrier layer disposed over a portion of the gate stack of the each step;”

148. Park at least renders obvious *a barrier layer* (“etch-stop layer” 110a) *disposed over a portion of the gate stack of the each step*:



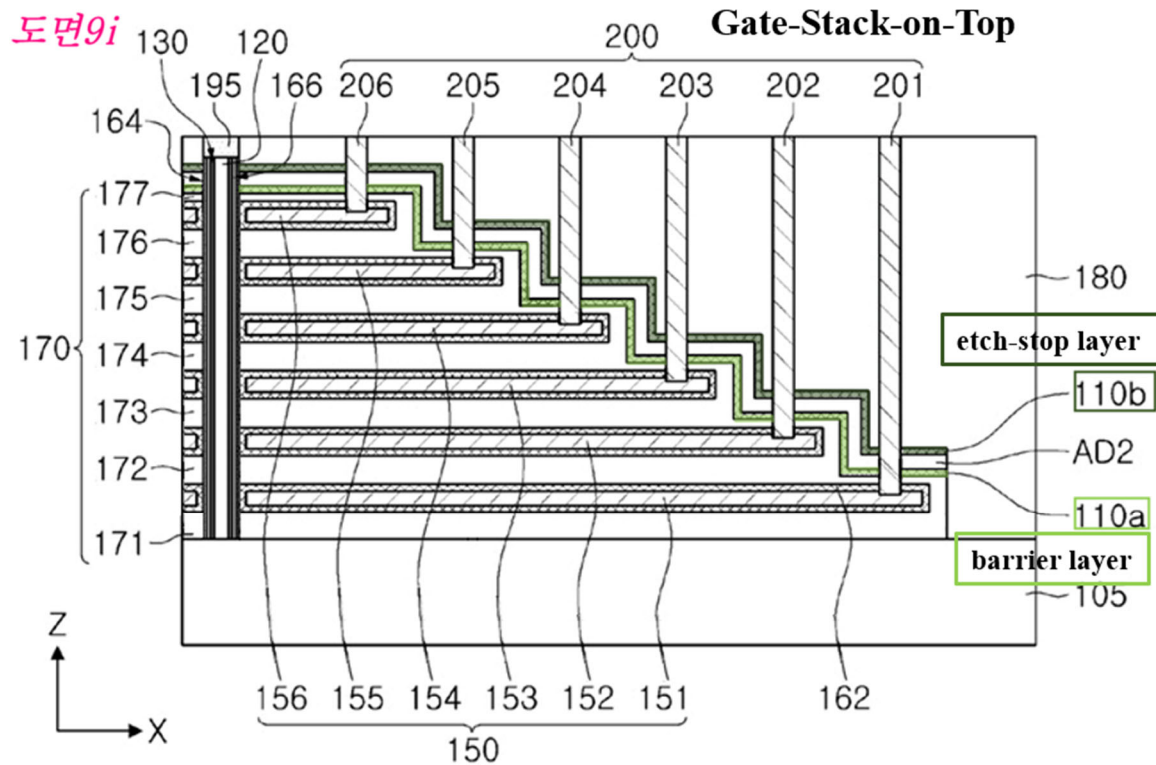
Ex. 1006, Fig. 9i, [0049]. Specifically, “one or more etch-stop layers (110) may be formed on the gate electrode (150) in a plurality of pad regions.” *Id.*, [0046]. As explained above, a barrier layer is another etch-stop layer. §IX. Park’s etch-stop layer 110a and the barrier layer of the ’711 Patent may comprise the same material: silicon oxide, silicon oxynitride, silicon nitride, or aluminum oxide. Ex. 1001, 7:50-52, 6:20-24 (disclosing that barrier layer may comprise the same material as the dielectric layer, which in turn may comprise one of the materials above); Ex. 1006,

[0124], [0041], [0063] (disclosing that etch-stop layer 110a may comprise the same material as the blocking layer, which in turn may comprise silicon oxide, silicon nitride, silicon oxynitride, or a high-k dielectric material, including aluminum oxide). Moreover, the etch-stop layer 110a “temporarily stop[s] or slow[s] down” the etching of vertical openings, “thereby preventing defects caused by penetration of the top gate electrode layer....” *Id.*, [0051]. That is the function of the barrier layer. Ex. 1001, 7:36-39 (“a barrier layer for protecting the underlying structure during subsequent etching processes”). Thus, etch-stop layer 110a functions as a barrier layer. The *portion[s]* over which the barrier layer are disposed are pad regions P1-P6. Ex. 1006, Figs. 9b-9c, [0046] (“one or more etch-stop layers (110) may be formed on the gate electrode (150) in a plurality of pad regions”).

149. The '711 Patent discloses that “‘over’ something” includes directly on that something. Ex. 1001, 4:6-10. Thus, this limitation is met when the gate stack is above the dielectric layer for the reason explained above with respect to Kim. §XIII.B.3.

4. [1.C] “an etch-stop layer disposed on the barrier layer;”

150. Park discloses *an etch-stop layer* (“etch-stop layer” 110b) *disposed on the barrier layer* (etch-stop layer 110a):



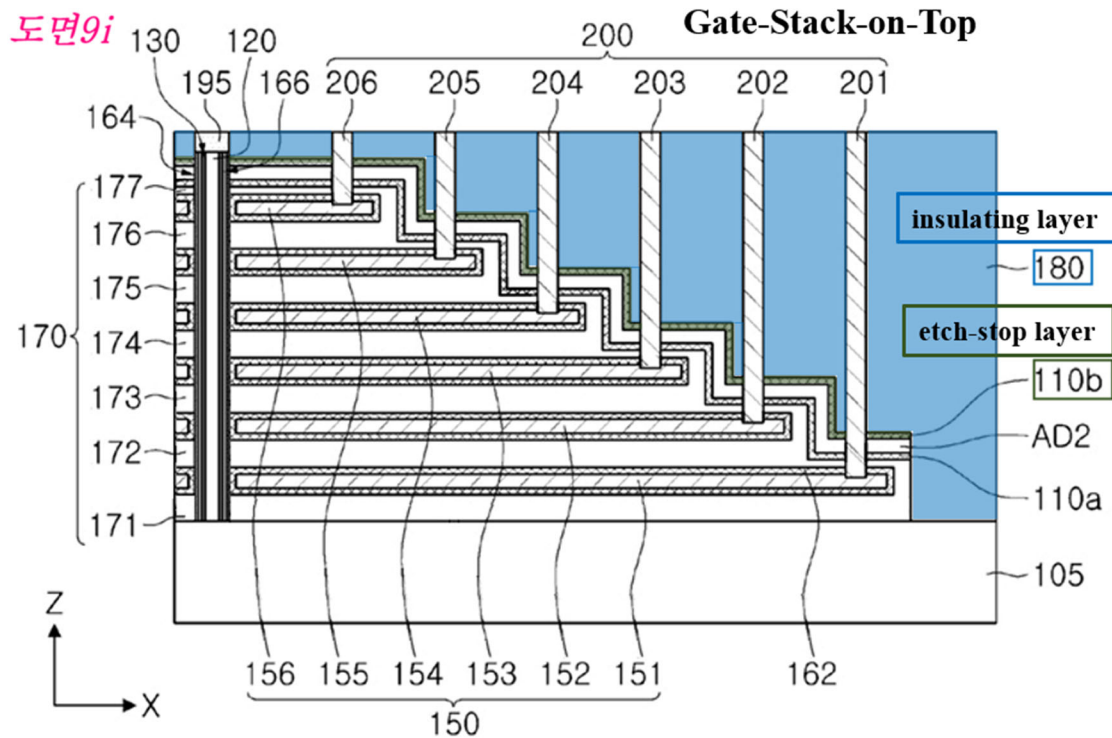
Ex. 1006, Fig. 9i, [0049]. Like layer 110a, the etch-stop layer 110b “temporarily stop[s] or slow[s] down” the etching of vertical openings, “thereby preventing defects caused by penetration of the top gate electrode layer...” *Id.*, [0051]. That performs the function of an etch-stop layer of the ’711 Patent. Ex. 1001, 5:61-63 (“The etch-stop film protects underlying layers during etching processes that form contact VIAs.”). As explained, as long as the two layers comprise different materials and thus have different etching rates, both can serve the intended purpose of an etch stop. That a layer AD2 may exist between the etch-stop layer and the barrier layer does not matter. First, the layer AD2 is optional. *Id.*, [0103] (“an insulating layer (AD2) *may be* further arranged between the first etch-stop sacrificial layer (115a)

and the second etch-stop sacrificial layer (115b)....”) (emphasis added). Second, when layer AD2 exists, the etching process still penetrates both etch-stop and barrier layers, and they still need to serve the function of an etch stop.

151. The ’711 Patent discloses that X “on” Y means X is directly or indirectly on Y, that is, “an intermediate ... layer” may exist between X and Y. Ex. 1001, 4:1-6. Therefore, this limitation is met even though an intermediate layer AD2 exists between etch-stop layers 110a and 110b.

**5. [1.D] “an insulating layer disposed on the etch-stop layer;
and”**

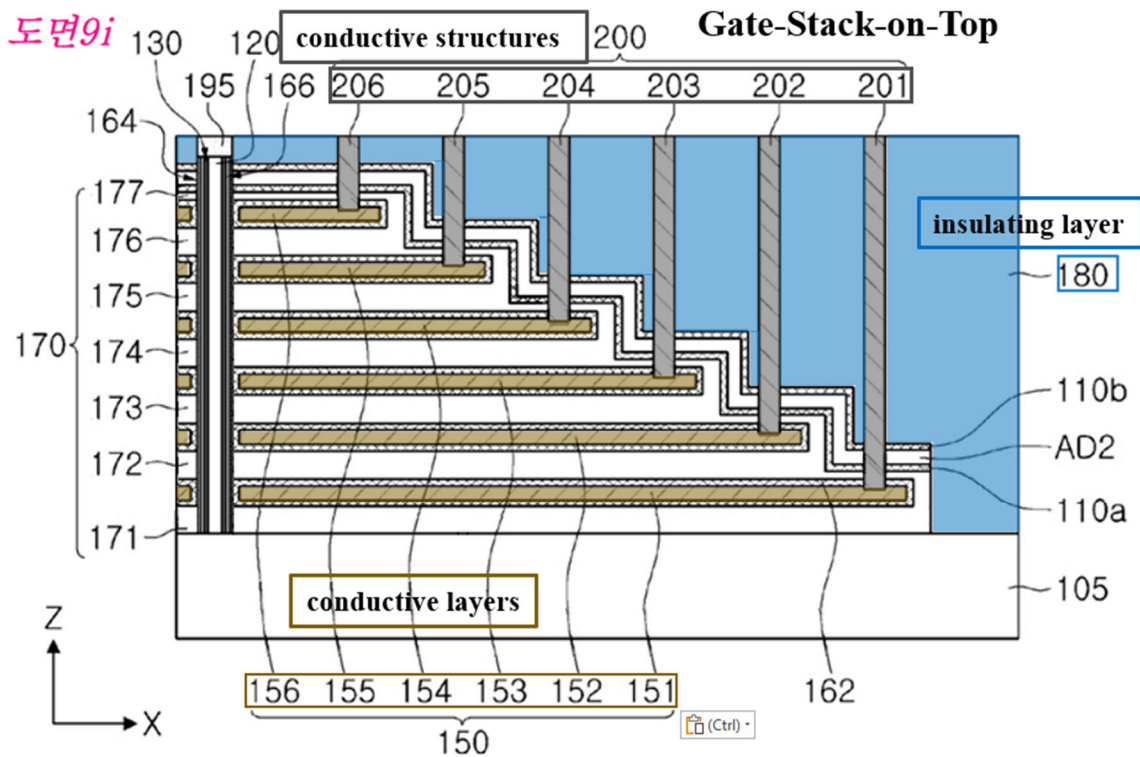
152. Park discloses *an insulating layer* (“connection region insulating layer” 180) *disposed on the etch-stop layer* (“etch-stop layer” 110b):



Ex. 1006, Fig. 9i, [0103] (“a connection region insulation layer (180) can be applied onto the second etch-stop sacrificial layer (115b)....”). Forming such an insulating layer was conventional and provides a planar surface for the local interconnects above that insulating layer.

6. [1.E] “a plurality of conductive structures formed in the insulating layer, wherein each conductive structure is formed on the conductive layer of the each step.”

153. Park discloses *a plurality of conductive structures* (“contact plugs” 201-206) *formed in the insulating layer* (“connection region insulating layer” 180), *wherein each conductive structure* (one of “contact plugs” 201-206) *is formed on the conductive layer* (corresponding one of “gate electrode layers” 151-156) *of the each step*:



Ex. 1006, Fig. 9i, [0050] (“a vertical opening in which a contact plug (206) is formed in connection with a gate electrode layer (156)”), [0108]-[0110] (describing an etching process “to prepare a plurality of vertical openings,” which are then “filled with an electrically conductive material” to form contact plugs “electrically connect[ed] [to] ... gate electrode layers....”); *id.*, [0043], [0045], [0049]. Again, these staircase contacts were very well known. They were a prototypical component of 3D NAND memory devices.

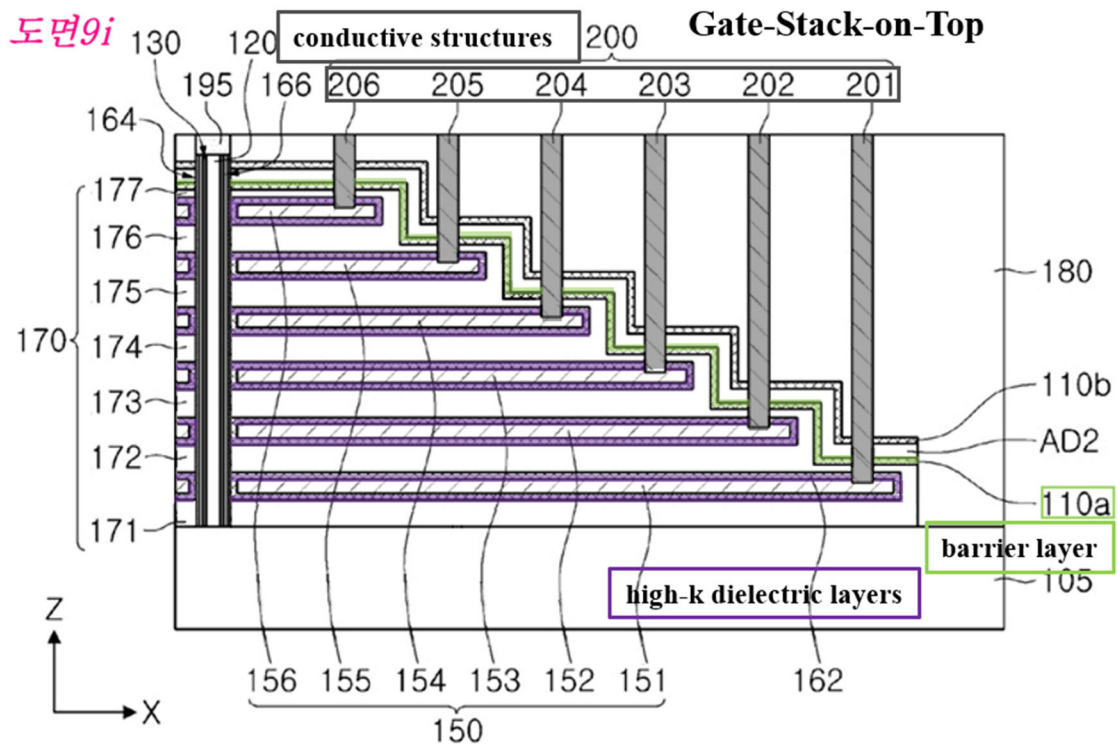
154. For the same reason explained in Ground 1, when the gate stack is disposed over the dielectric layer at each step, *each conductive structure* (“contact plugs” 201-206) is still *formed on the conductive layer* (corresponding one of “gate

electrode layers” 151-156). §§XIII.A, XIII.B.6 (a POSITA’s knowledge). This is consistent with Park, which discloses electrically connecting gate electrodes and connecting lines through contact plugs. Ex. 1006, [0110] (“the plurality of connecting lines (220) must be electrically connected with the plurality of gate electrode layers (150) through the plurality of contact plugs (200).”). Again, this was well within the knowledge of a POSITA.

C. Claim 2:

- 1. [2] “The semiconductor structure of claim 1, wherein the plurality of conductive structures extend through the barrier layer and the high-k dielectric layer.”**

155. Park at least renders obvious that *the plurality of conductive structures* (“contact plugs” 201-206) *extend[s] through the barrier layer* (“etch-stop layer” 110a) *and the high-k dielectric layer* (“blocking layer” 162):



Ex. 1006, Fig. 9i, [0049]-[0050] (“a vertical opening in which a contact plug (206) is formed in connection with a gate electrode layer (156). . . .”), [0110]; *id.*, [0056], [0125]. This extension through the barrier layers and the high-k dielectric layer would be achieved through a single- or dual-stage etching process, depending on the materials in the layers and the selected etchant(s).

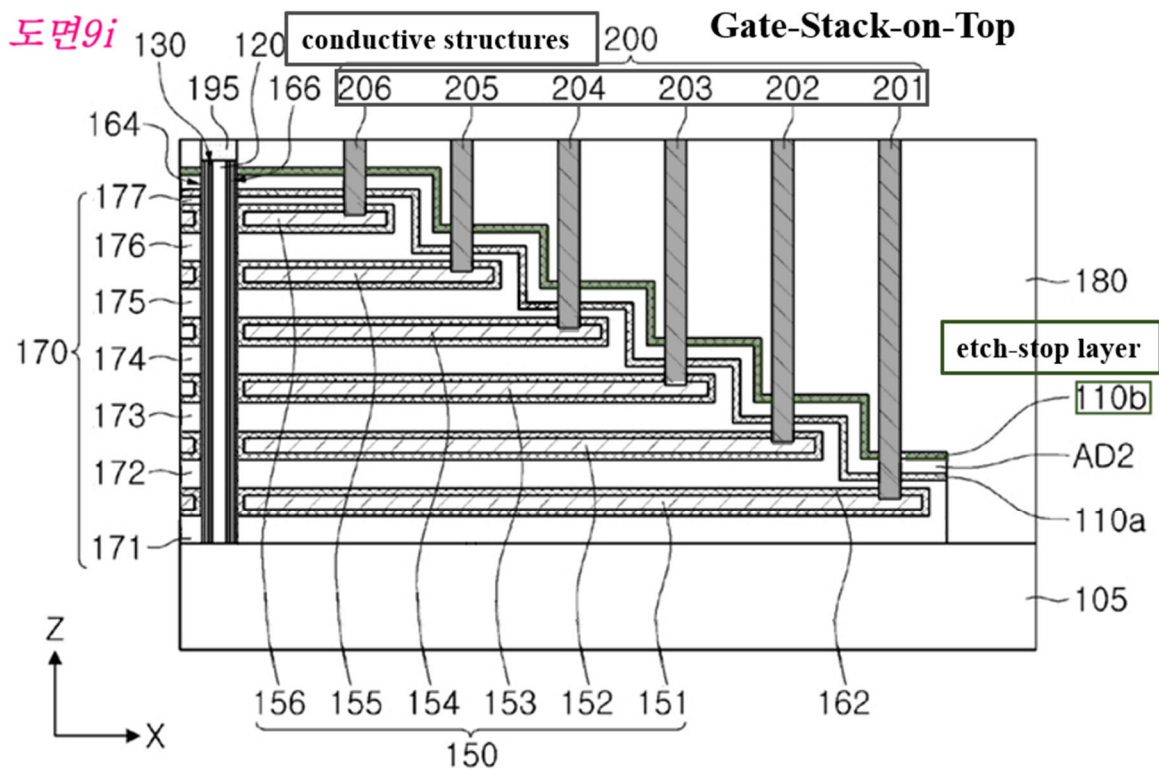
156. “[T]he plurality of connecting lines (220) must be electrically connected with the plurality of gate electrode layers (150) through the plurality of contact plugs (200).” Ex. 1006, [0110]. Thus, the contact plug must extend through the etch-stop layer 110a and the blocking layer to reach the gate electrode in the gate-stack-on-top configuration. Again, this was well within the knowledge of a

POSITA.

D. Claim 3:

1. [3] “The semiconductor structure of claim 1, wherein the plurality of conductive structures extend through the etch-stop layer.”

157. Park discloses that *the plurality of conductive structures* (“contact plugs” 201-206) *extend[s] through etch-stop layer* (“etch-stop layer” 110b):



Ex. 1006, Fig. 9i, [0049]-[0050] (“a contact plug (201) is formed is etched in connection with the gate electrode layer (151) ..., an etching process can be carried out to form two or more etch-stop layers (110a, 110b)”), [0110]; *id.*, [0056], [0125]. For the same reason explained above with respect to claim 2 that the conductive

structures must penetrate through the barrier layer and the high-k dielectric layer, they must also penetrate through the etch-stop layer. §XV.C.1. Again, if the conductive structure did not extend through the layers above the conductive gate portion, it would not contact the conductive gate layer, and the device would not be functional for the same reasons that I explained with respect to including staircase contacts for each gate layer.

E. Claim 4:

1. [4] “The semiconductor structure of claim 1, wherein the barrier layer comprises silicon oxide.”

158. Park discloses that *the barrier layer* (“etch-stop layer” 110a) *comprises silicon oxide*. Specifically, Park discloses that the blocking layer 162 may comprise silicon oxide. Ex. 1006, [0063]. Park further discloses that etch-stop layer 110a may comprise an identical material. *Id.*, [0105]. As explained, etching processes have great flexibility. For example, either a selective process or a reverse selective process may be used. §VIII. Therefore, as long as neither the etch-stop layer above nor the gate stack below the barrier layer comprise silicon oxide, a silicon oxide barrier layer can serve its intended function of an etch stop.

F. Claim 5:

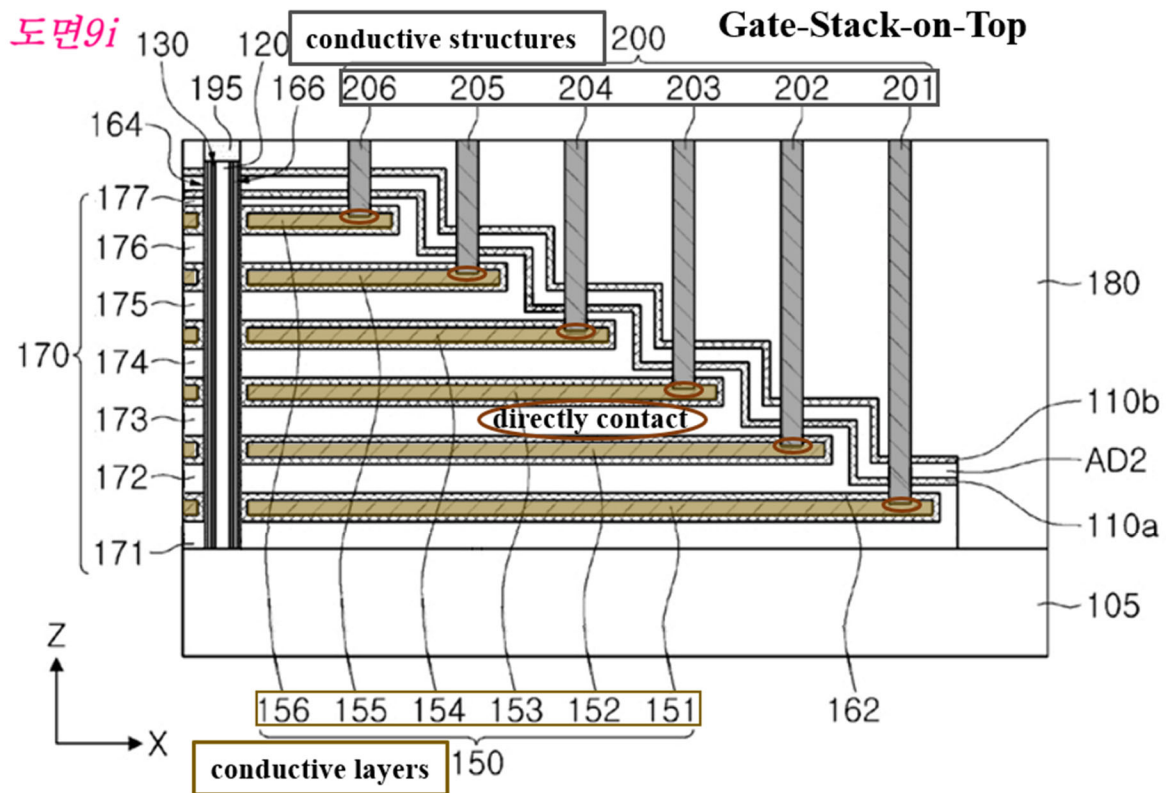
1. [5] “The semiconductor structure of claim 1, wherein the etch-stop layer comprises one or more of silicon nitride, a spin-on-dielectric, and a high-k dielectric.”

159. Park discloses that *the etch-stop layer* (“etch-stop layer” 110b) *comprises one or more of silicon nitride ... and a high-k dielectric*. Specifically, Park discloses that the blocking layer 162 may comprise silicon nitride (Si₃N₄) or a high-k dielectric. Ex. 1006, [0063]. Park further discloses that etch-stop layer 110b may comprise an identical material. *Id.*, [0105]. As explained, etching processes have much flexibility. For example, either a selective process or a reverse selective process may be used. §VIII. Therefore, as long as neither the insulating layer above nor the barrier layer below the etch-stop layer comprise silicon nitride, a silicon nitride etch-stop layer can serve its intended function.

G. Claim 6:

1. [6] “The semiconductor structure of claim 1, wherein the each conductive structure directly contacts a corresponding one of the conductive layer of the each step.”

160. Park at least renders obvious that *the each conductive structure* (one of “contact plugs” 201-206) *directly contacts a corresponding one of the conductive layer* (corresponding one of “gate electrode layers” 151-156) *of the each step*:



Ex. 1006, Fig. 9i, [0049]-[0050], [0110] (“the plurality of connecting lines (220) must be electrically connected with the plurality of gate electrode layers (150) through the plurality of contact plugs (200).”).

161. The direct contacts between contact plugs and gate electrode layers establish the required electrical connections. Ex. 1006, [0110]. Once again, this would have been well known to a POSITA. §§XV.B.6, XV.C.1 (electrical-connection requirement). And again, it would risk punch-through to extend through the gate layer into the underlying dielectric.

H. Claim 8:

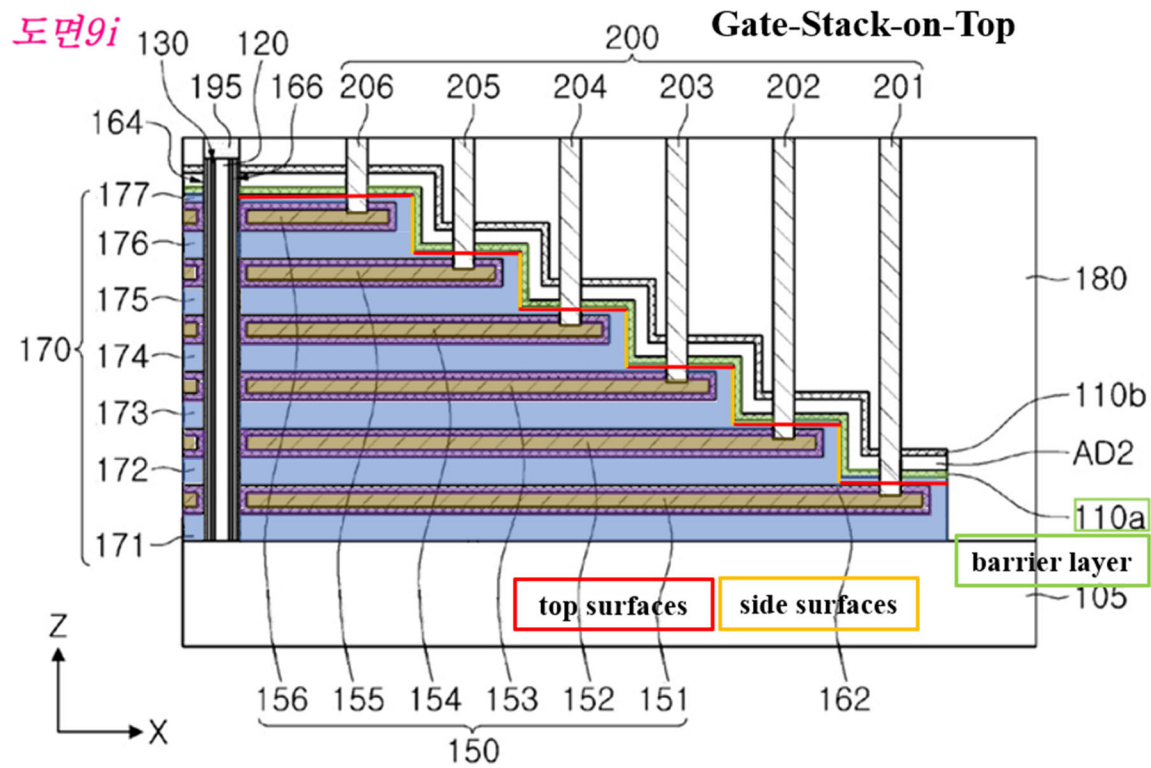
1. [8] “The semiconductor structure of claim 1, wherein the plurality of conductive structures comprise one or more of tungsten, cobalt, nickel, copper, and aluminum.”

162. Park discloses that *the plurality of conductive structures* (“contact plugs” 201-206) *comprise[s] ... tungsten*. Ex. 1006, [0110] (“the plurality of vertical openings (210) may be filled with an electrically conductive material - for example tungsten (W) - to form a contact plug (201-206: 200).”); *id.*, [0099] (“The electrically conductive material filling the vertical opening (210) may be the same as the electrically conductive material included in the gate electrode layer (150), in an example it may be tungsten (W).”). Tungsten is widely used in 3D memory devices because it is a harmless metal, that is, it does not diffuse like gold or copper. Metal diffusion can damage surrounding elements.

I. Claim 9:

1. [9] “The semiconductor structure of claim 1, wherein the barrier layer is formed on side and top surfaces of the plurality of steps.”

163. Park discloses that *the barrier layer* (“etch-stop layer” 110a) *is formed on side and top surfaces of the plurality of steps*:



Ex. 1006, Fig. 9i, [0049] (“a plurality of etch-stop layers (110a, 110b) is provided having a shape corresponding to a step arranged in the connection region (D).”). As can be seen in Figure 9i, this step shape *is formed on side and top surfaces of the plurality of steps*. Such a step shape may be formed using conformal coating, which had been known in the art for decades and was commonly used in semiconductor manufacturing.

J. Claim 11:

1. [11] “The semiconductor structure of claim 1, wherein the high-k dielectric layer comprises hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, or a combination thereof.”

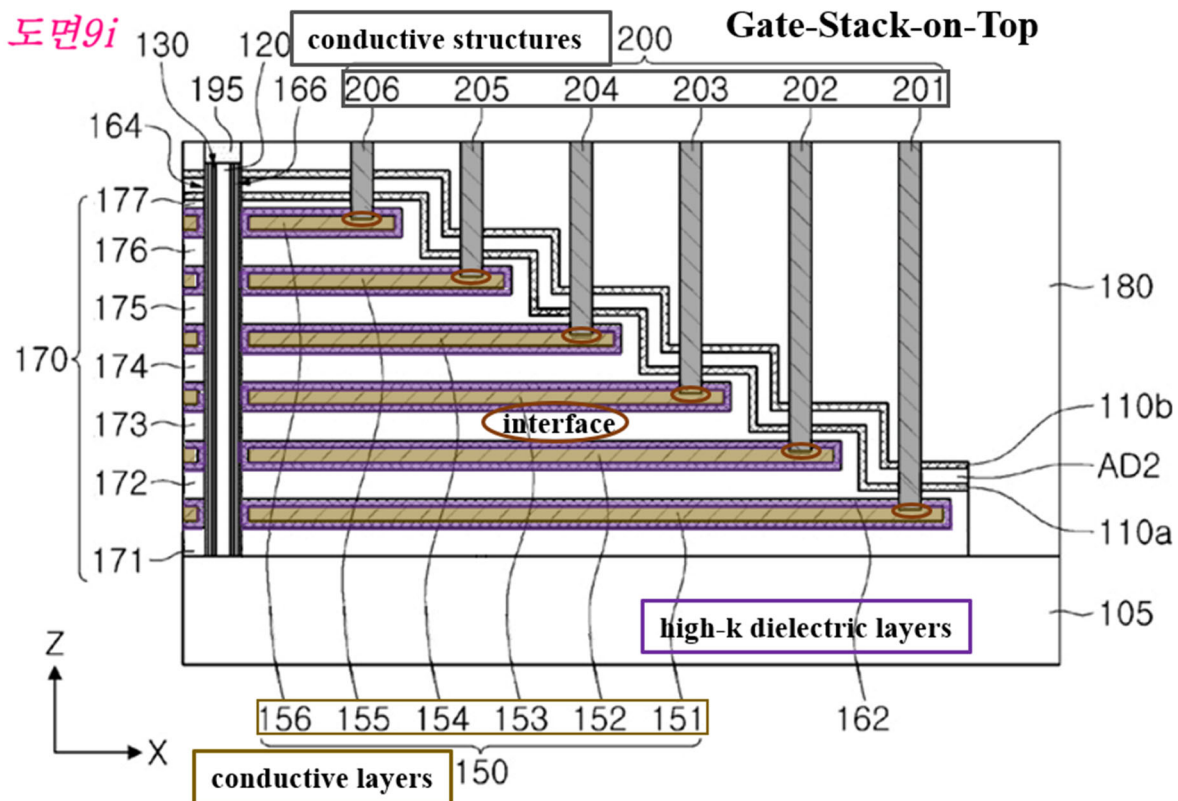
164. Park discloses that *the high-k dielectric layer* (“blocking layer” 162)

comprises hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, [or] lanthanum oxide.... Specifically, Park discloses that the blocking layer 162 may comprise a high-k dielectric, and that “[t]he high-k dielectric material may be any one of aluminum oxide (Al_2O_3), tantalum oxide (Ta_2O_3), ... zirconium oxide (ZrO_2), ... hafnium oxide (HfO_2), ... lanthanum oxide (La_2O_3)....” Ex. 1006, [0063]. As explained, the high-k dielectric layer is deposited when the channel is coated. §XIII.B.2; *see also, e.g.*, Ex. 1006, [0013] (“depositing an insulating material on a region from which the plurality of sacrificial layers ... [is] removed to form a gate insulating film....”). Therefore, the selection of material for this layer is determined by considerations related to channel formation.

K. Claim 12:

1. [12] **“The semiconductor structure of claim 1, wherein top and bottom surfaces and a sidewall of the conductive layer are covered by the high-k dielectric layer, except at an interface between the conductive layer and the conductive structure.”**

165. Park at least renders obvious that *top and bottom surfaces and a sidewall of the conductive layer* (one of “gate electrode layers” 151-156) *are covered by the high-k dielectric layer* (“blocking layer” 162), *except at an interface between the conductive layer and the conductive structure* (corresponding one of “contact plugs” 201-206):



Ex. 1006, Fig. 9i, [0060] (“The gate electrode layer (154) is surrounded by a blocking layer (162).”); [0105] (“a gate electrode layer (150) may be formed ... within the block layer (162).”); *id.*, [0041]. The high-k block layer is deposited during channel formation. §XV.J.1. Then a conductive material is deposited into the remaining recess region to form the word line layers. Finally, an interface between the conductive layer and the conductive structure is etched away during the formation of the conductive structures to establish contact between the two. Again, a POSITA would have known that the conductive structure must form an electrical contact with the corresponding conductive layer. §XV.C.1 (electrical-connection requirement). This, in turn, requires the conductive structure to penetrate the high-

k dielectric layer. Otherwise, the device would have an open circuit and would be non-functional.

166. For the reason explained in Ground 1, a POSITA would have found it obvious that the layer ordering would not change the spatial relationship of gate electrodes and blocking insulating layer. §XIII.L.1; Ex. 1006, [0110].

167. If Patent Owner were to argue that Park does not meet claim 12 because its high-k dielectric layer covers both sidewalls of the conductive layer, Patent Owner would be wrong. First, claim 12 is an open-ended comprising claim and is silent on the configuration at the second sidewall. The claim contains no requirement or suggestion regarding the configuration at the second sidewall. Second, the '711 Patent discloses a sidewall isolation barrier layer, insulating layer 530, that covers the conductive layer at the second sidewall. Ex. 1001, 9:41-44, 12:42-48. Park's high-k dielectric layer at the second sidewall is basically equivalent to such an isolation barrier layer. For example, the insulating layer 530 of the '711 Patent may comprise the same material as the etch-stop layer 310, which can be made of high-k dielectric films. *Id.*, 9:46-48, 8:10-14. That is the same material from which Park's block layer 162 may be made. Ex. 1006, [0063]. The '711 Patent provides no reason or hint that a structure of claim 12 cannot have this isolation barrier layer. Therefore, Park's high-k dielectric layer at the second sidewall does not render Park's disclosure outside the scope of claim 12.

L. Claim 13:

1. [13.PRE] “A semiconductor structure, comprising:”

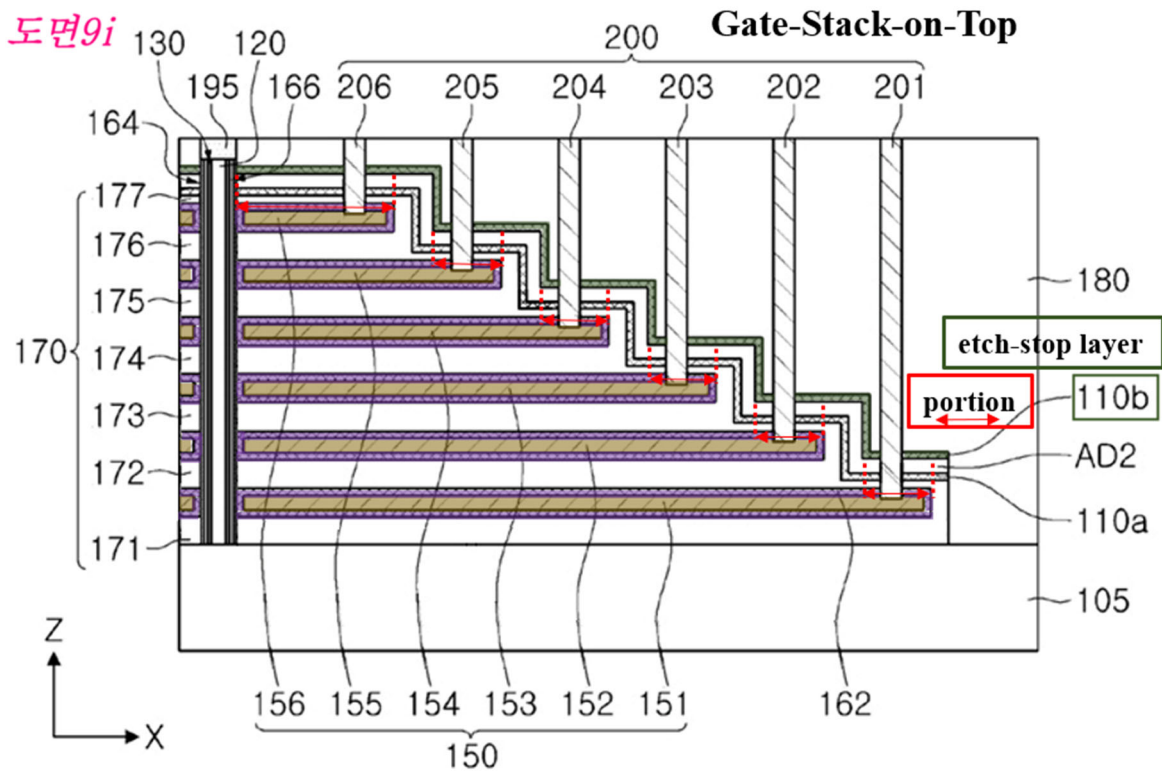
168. This preamble is identical to that of claim 1. Park discloses it for the same reason as explained above. §XV.B.1.

2. [13.A] “a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;”

169. This limitation is identical to [1.A]. Park at least renders it obvious for the same reason as explained above. §XV.B.2.

3. [13.B] “an etch-stop layer disposed on a portion of the gate stack of the each step;”

170. Park discloses *an etch-stop layer* (“etch-stop layer” 110b) *disposed on a portion of the gate stack* (one of “gate electrode layers” 151-156 and “blocking layer” 162) *of the each step*:



Ex. 1006, Fig. 9i, [0049] (“a plurality of etch-stop layers (110a, 110b) is provided having a shape corresponding to a step”). The *portion* is the exposed top surface or the tread of each step. Claim limitation [1.B] contains the same requirement but for the barrier layer. §XV.B.3.

171. As explained a few times above, the '711 Patent discloses that “on” something includes both direct and indirectly on that something. Ex. 1001, 4:1-6. Therefore, Park satisfies limitation [13.B] even though intermediate layers exist between the etch-stop layer 110b and the gate stack.

4. **[13.C] “an insulating layer disposed on the etch-stop layer; and”**

172. This limitation is identical to [1.D]. Park discloses it for the same reason as explained above. §XV.B.5.

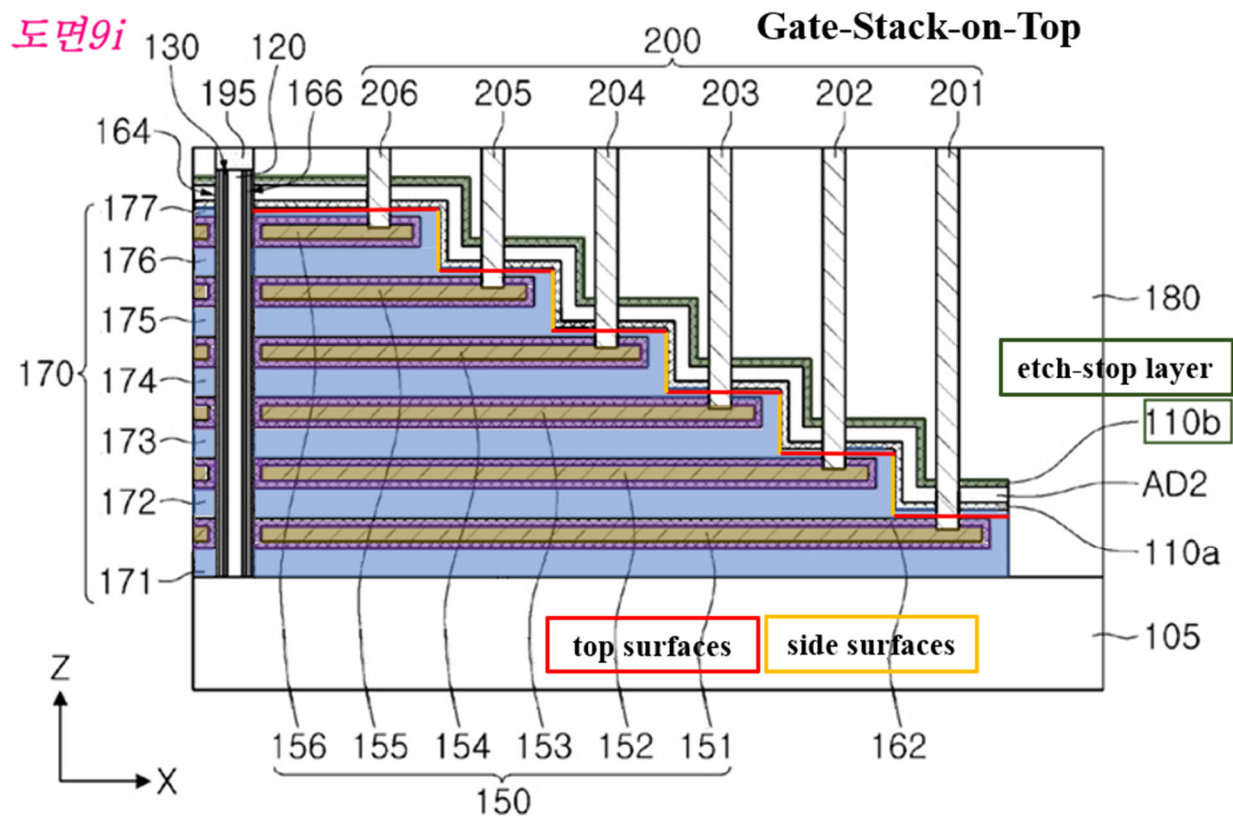
5. **[13.D] “a plurality of conductive structures formed in the insulating layer and extending through the etch-stop layer and the high-k dielectric layer, wherein each conductive structure directly contacts the corresponding conductive layer of each step.”**

173. This limitation combines the requirements of limitation [1.E] and claims 2, 3, and 6. Park at least renders it obvious for the same reason as explained above. §§XV.B.6, XV.C.1, XV.D.1, XV.G.1.

M. Claim 14:

1. **[14] “The semiconductor structure of claim 13, wherein the etch-stop layer is formed on a side surface and a top surface of each step.”**

174. Park discloses that *the etch-stop layer* (“etch-stop layer” 110b) *is formed on a side surface and a top surface of each step:*



Ex. 1006, Fig. 9i, [0049] (“a plurality of etch-stop layers (110a, 110b) is provided having a shape corresponding to a step”), [0008] (“The etch-stop layer may have a shape corresponding to a step between the plurality of pad regions.”); *id.*, [0124]. Again, the ’711 Patent discloses that “on” something includes both directly and indirectly on that something. Ex. 1001, 4:1-6. Thus, the fact that there are intermediate layers between the etch-stop layer and the steps in Park’s structure does not matter. Claim 9 contains virtually the same requirement but for the barrier layer. §XV.I.1.

N. Claim 15:

- 1. [15] “The semiconductor structure of claim 14, wherein thicknesses of the etch-stop layer is the same on the side and top surfaces of each step.”**

175. Park at least renders obvious the additional limitation of claim 15.

176. Park repeatedly refers to “*the* thickness of the etch-stop layer.”

Ex. 1006, [0006], [0060], [0067], [0070]-[0071]. A POSITA would have understood these references to mean that the etch-stop layer has a single thickness.

Thus, *thicknesses of the etch-stop layer* (“etch-stop layer” 110b) *is the same on the side and top surfaces of each step.*

177. A POSITA’s knowledge would have supported this understanding of Park. For example, it was known that an etch-stop layer of uniform thickness on all steps was desirable to achieve a uniform contact-hole depth below the etch-stop layer. Ex. 1017, [0042]. This prevents or reduces over-etching or under-etching. Furthermore, a layer of uniform thickness was common and easily achieved through techniques used to deposit a conformal etch-stop layer such as chemical vapor deposition (CVD) or atomic layer deposition (ALD).

O. Claim 16:

1. [16] **“The semiconductor structure of claim 13, wherein the etch-stop layer comprises one or more of silicon nitride, a spin-on-dielectric, and a high-k dielectric.”**

178. The additional limitation of claim 16 is identical to that of claim 5. Park discloses it for the same reason as explained above. §XV.F.1.

P. Claim 18:

1. [18] **“The semiconductor structure of claim 13, wherein the high-k dielectric layer comprises hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, lanthanum oxide, or a combination thereof.”**

179. The additional limitation of claim 18 is identical to that of claim 11. Park discloses it for the same reason as explained above. §XV.J.1.

Q. Claim 19:

1. [19] **“The semiconductor structure of claim 13, wherein top and bottom surfaces and a sidewall of the conductive layer are covered by the high-k dielectric layer, except at an interface between the conductive layer and the conductive structure.”**

180. The additional limitation of claim 19 is identical to that of claim 12. Park discloses it for the same reason as explained above. §XV.K.1.

XVI. GROUND 4: PARK IN VIEW OF FANG

A. Claim 7:

1. [7] “The semiconductor structure of claim 1, wherein top surfaces of the plurality of conductive structures, the insulating layer, and a portion of the etch-stop layer are coplanar.”

181. As explained above, Park at least renders obvious claim 1. §XV.B.

Park in view of Fang renders obvious claim 7.

182. Fang discloses that *top surfaces of the plurality of conductive structures* (“contacts” 155a-155d), *the insulating layer* (“another oxide material” 135), *and a portion of the etch-stop layer* (“etch stop material” 130) *are coplanar*:

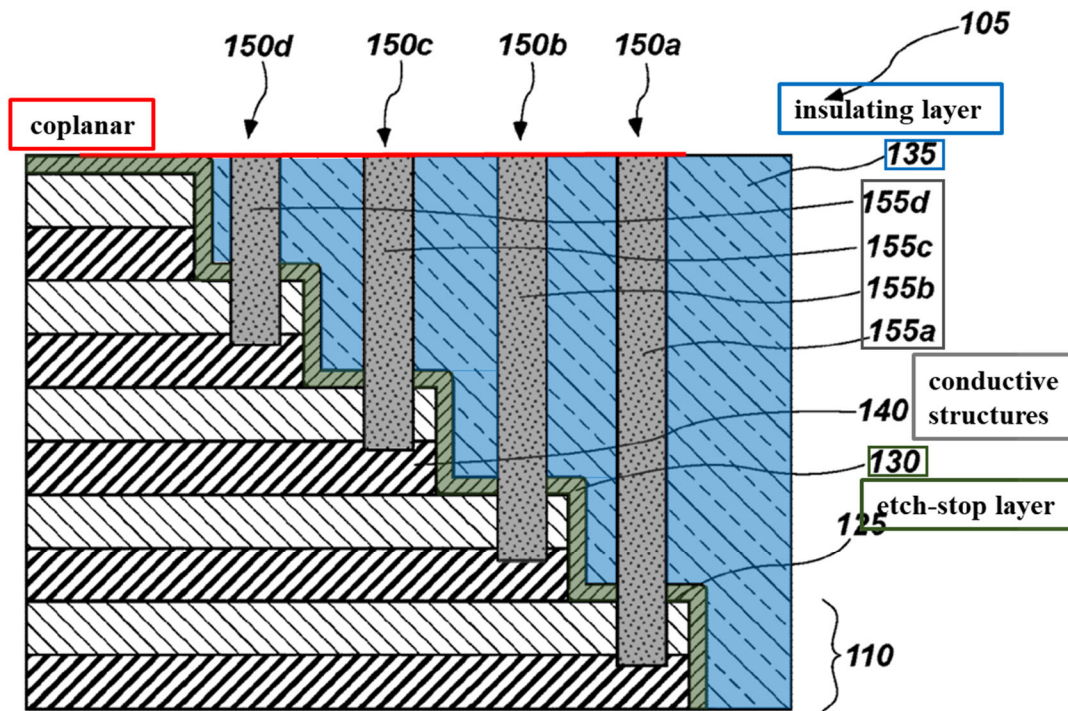
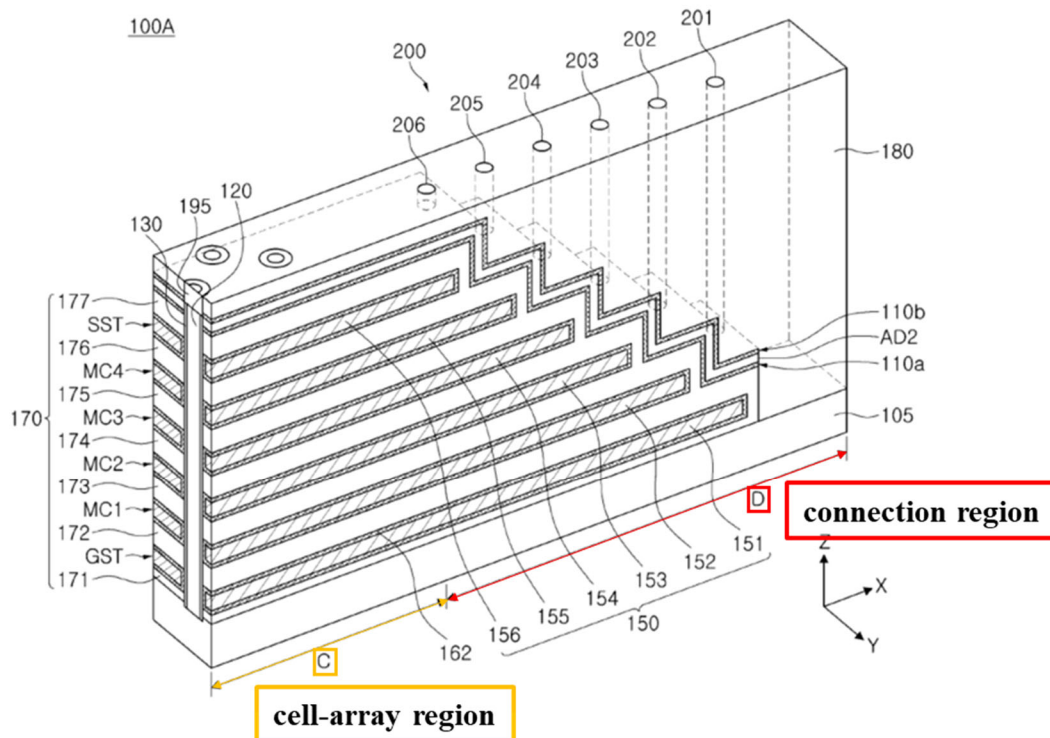


FIG. 6

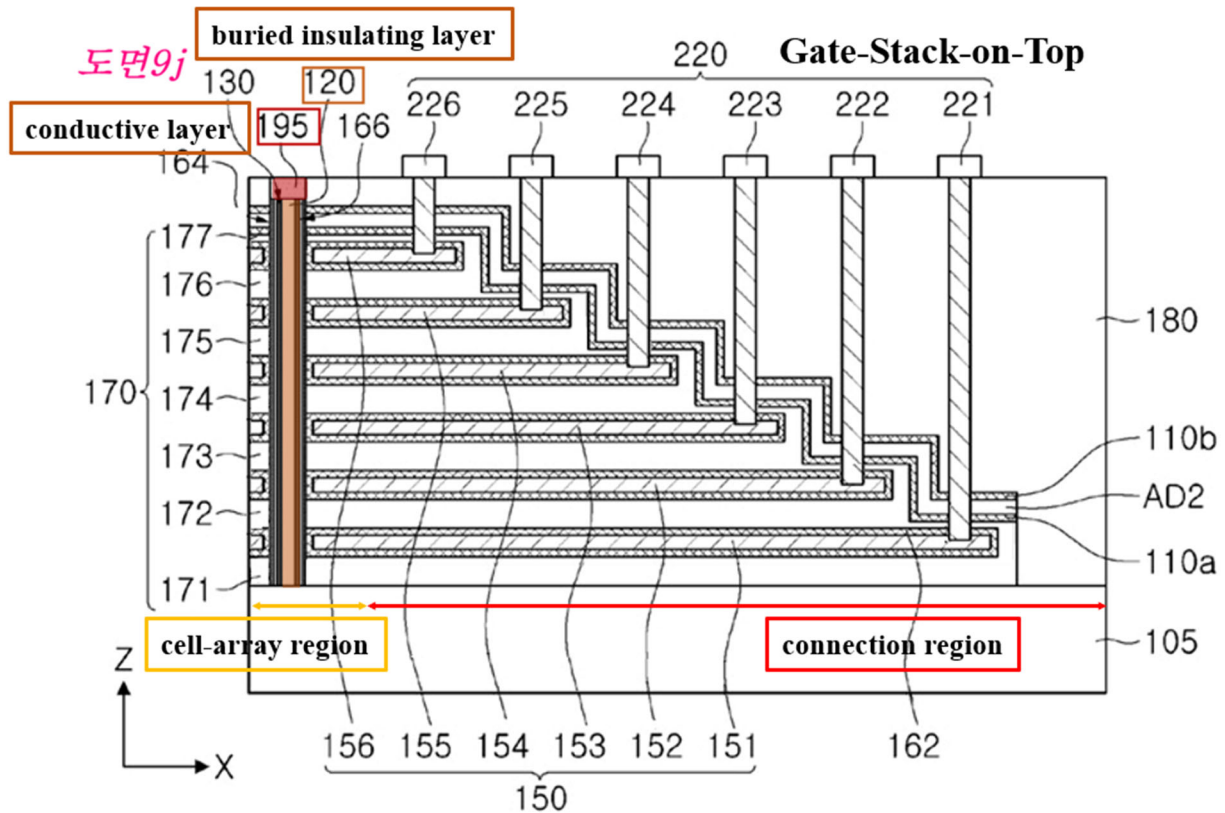
Ex. 1007, Fig. 6, [0024]. Fang achieves this coplanar surface through a planarization process. *Id.*, [0024]. A planar surface at the top of the structure is beneficial to further manufacturing stages because, for example, materials tend to be deposited, patterned and etched more easily on a planar surface, resulting in greater reliability.

183. Park also discloses planarizing the connection region insulating layer 180 to equalize the heights of the cell array region C, where the channel is located, and the connection region D, where the staircase structure is located. Ex. 1006, [0084] (“the heights of the cell array region (C), the connection region (D), and the peripheral circuit region may be equal by the formation and planarization process of the connection region insulating layer (180).”).

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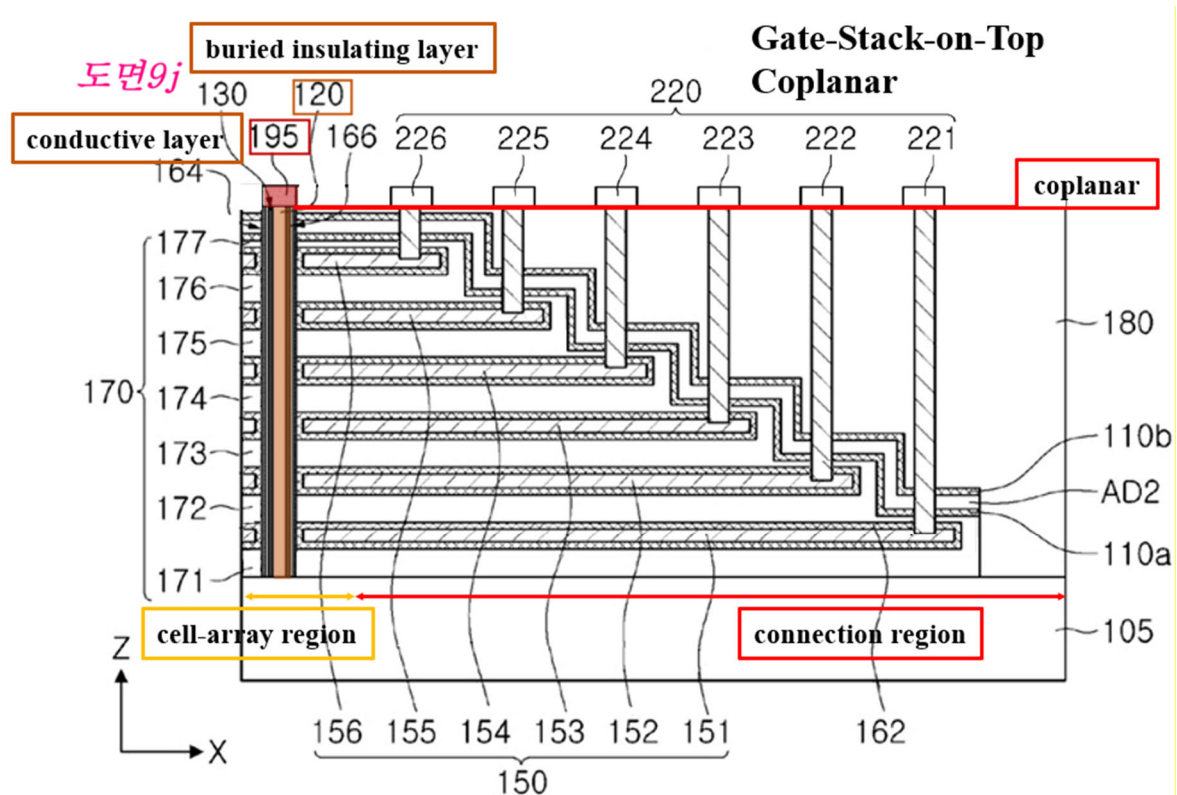
Id., Fig. 5. During this process, the top of the buried insulating layer (120) (within the channel region 130) may be removed together with the top of the connection region insulating layer 180. *Id.*, [0089] (“The top of the buried insulating layer (120) can then be partially removed using an etching process....”), [0103] (“a planarization process can be performed....”). Then conductive layer 195 is formed above the buried insulating layer 120:



Ex. 1006, Fig. 9j, [0089] (“a material that constitutes a conductive layer (195) can be deposited at the removed location. Again, a planarization process may be performed, such that a conductive layer (195) may be formed.”). As shown above, the top surfaces of Park’s insulation layer and conductive structures are coplanar with the top surface of the conductive layer 195, but not the etch-stop layer 110b.

184. In view of Fang, a POSITA would have found it obvious to modify Park’s planarization process such that *top surfaces of the plurality of conductive structures* (“contact plugs” 201-206), *the insulating layer* (“connection region insulating layer” 180), *and a portion of the etch-stop layer* (“etch-stop layer” 110b) *are coplanar*.

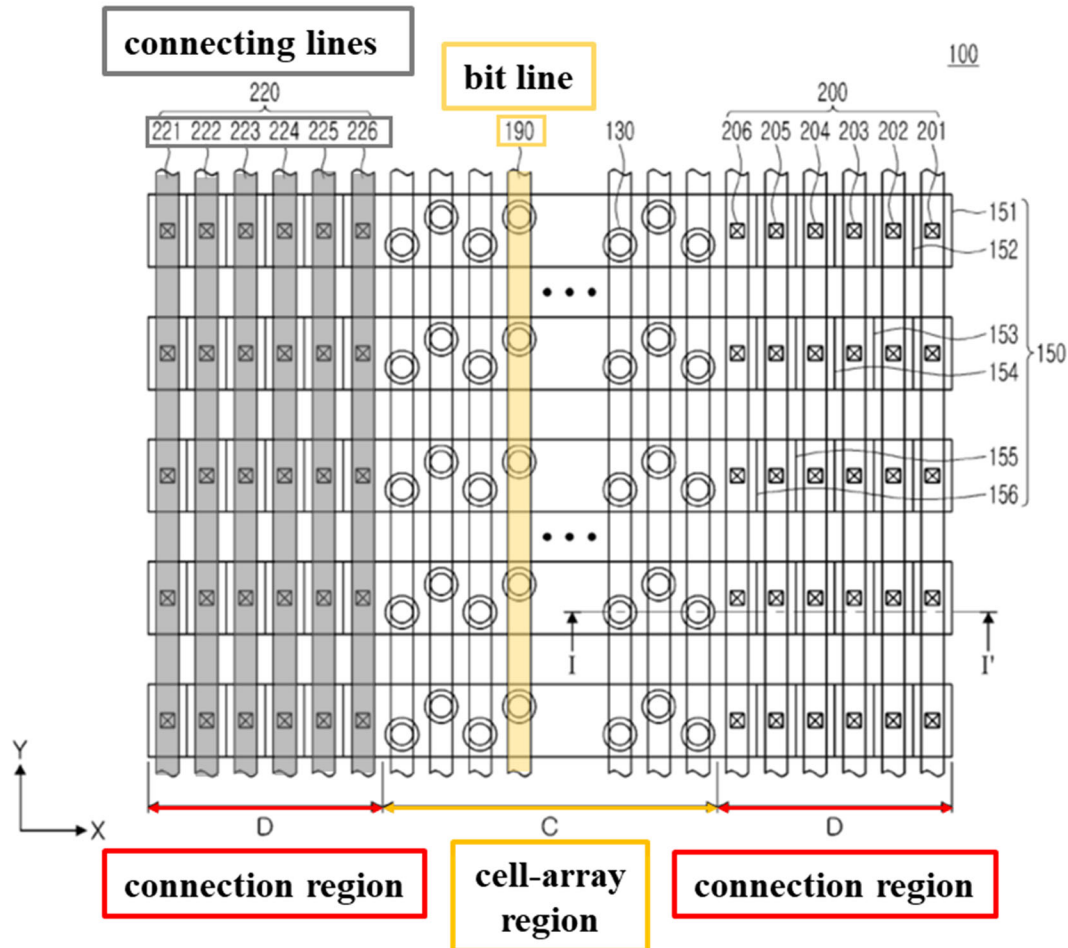
185. Park discloses planarizing the staircase structure serves the purpose “to remove unnecessary semiconductor material and insulating material covering the top connection region insulating layer (180).” Ex. 1006, [0089]. This planarization process occurs after forming the channel and before depositing the conductive layer 195, which is the conductive drain of the channel. *Id.*, [0088]-[0089]. In view of Fang, it would have been obvious that the materials above the top-surface plane of the etch-stop layer 110b is “unnecessary” and may be removed. *Id.*, [0089]. This would result in a device as shown below:



Id., Fig. 9j (top modified in addition to gate stack on top). This configuration is compatible with Park’s disclosure. This compatibility demonstrates that the

materials above the top surface plane of the etch-stop layer is indeed unnecessary and may be removed. For example, as shown above, when Fang's coplanar configuration is applied on Park's device, the connecting lines 221-226 would be lowered to roughly the same height as the conductive layer 195. This would not interfere with the device's function. This can be seen as follows. Park's conductive layer 195 connects the channel region 130 with a bit line 190. *Id.*, [0040]. The connecting lines 221-226 and bit lines 190 are parallel in the plan view in the x-and-y-axis direction:

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Id., Fig. 3. Therefore, lowering the connecting lines to the same height as the bit lines in the z-axis direction has no functional impact because parallel lines do not intersect whether they are at the same height in the z-axis direction. This allows the device to function as intended.

186. Furthermore, though not shown, Fang also discloses select lines and access lines that electrically connect to gate electrodes through contacts 155a-155d. Ex. 1008, [0026], [0040]. A POSITA would have understood these select lines and

access lines to be equivalent to Park's connecting lines, in that these lines in the respective devices serve the same function. As such, Fang's select lines/access lines are at the same vertical height as its contacts 155a-155d since as shown above it discloses a coplanar surface. This is the same as Park's modified configuration. Fang's configuration further renders it obvious that the extra thickness in Park's connection region insulating layer above the plane of the etch-stop layer is unnecessary. Thus, applying Fang's coplanar configuration on Park's device is simply applying a known technique (planarization disclosed in Park) and a suitable option (height of top surface as disclosed in Fang) on a similar device to remove additional, unnecessary material consistent with Park's disclosure.

B. Claim 10:

1. **[10] "The semiconductor structure of claim 1, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm."**

187. Park at least renders obvious claim 1. §XV.B. Park in view of Fang renders obvious claim 10.

188. For the reason explained above with respect to Kim, claim 10 is obvious over Park because the difference due to the additional thickness limitation, if any, is only dimensional. §XIV.A.1. Relative to claim 1, claim 10 does not produce any difference in performance. As explained, the etch-stop thickness has great flexibility because of flexibility in materials and etchants used to form and etch the various

layers.

189. If more is required, Fang discloses an analogous semiconductor structure having an etch-stop layer. Ex. 1007, Fig. 6, [0020]. Their etch-stop layers are analogous as well. The etch-stop layer of both Park's and Fang's devices may comprise silicon nitride. Ex. 1005, [0187], §XV.F.1. Fang's etch-stop layer "may be formed by conventional techniques...." Ex. 1007, [0020]. It would have been obvious that such conventional techniques, some of which Park already uses, may be used to form Park's etch-stop layer. Ex. 1006, [0086] (disclosing the use of ALD and CVD). Fang's etch-stop layer "may be formed over the stairs 125 at a thickness ranging from about 50 Å to about 1000 Å." Ex. 1007, [0021]. That is equivalent to about 5 nm to 100 nm. This range overlaps with the claimed *range between 10 nm and 1000 nm*. Therefore, Park in view of Fang renders claim 10 obvious.

190. Fang has two etch-stop layers while Park has one. To the extent the thickness of Fang's etch-stop layer might be reduced to account for Park's extra etch-stop layer when adapting Fang's etch-stop thickness to Park's structure, a POSITA would have found it obvious that the thickness would still overlap with the claimed *range between 10 nm and 1000 nm*. This reduction may be done, for instance, to maintain a total etch resistance between two etch-stop layers or one, however many is present in the structure. For example, a POSITA would not have reduced Fang's etch-stop layer to below 10 nm, which is the reduction required to

avoid any overlap with the claimed thickness range, to account for Park's extra etch-stop layer. Moreover, there is flexibility in the thickness because other process parameters can be adjusted for the etch-stop layer to work within a thickness range.

191. If Patent Owner were to argue that this combination would not have been obvious because Park does not disclose the height of its staircase structure and thus the depths of contact holes, Patent Owner would be wrong. A POSITA would have understood that both Fang and the '711 Patent include a broad range (20x and 100x, respectively) around what the Examiner took official notice and characterized as "notoriously well[-]known" thicknesses for etch-stop layers. Ex. 1002, 156. A POSITA would have found it obvious that some subset of values within the range would work with an appropriate choice of etchant and relative etch selectivities. The '711 Patent is consistent with this understanding. The patent only discloses a range of the thickness of each dielectric layer or sacrificial/conductor layer. Ex. 1001, 6:38-40. That range is wide from 10 to 200 nm, a factor of 20x. *Id.* Relatedly, the patent places no upper or lower limits on the number of steps in the staircase. Furthermore, it discloses that "a thickness of the SC layer 102 [which is a step] can be different for each staircase level." *Id.*, 6:40-41. These disclosures together do not provide enough information for a POSITA to determine the height of the '711 Patent staircase and thus the depths of its contact holes. The height may vary by orders of magnitude. Yet presumably the claimed range is adequate for an etch-stop

layer for the staircase, regardless of the contact-hole depths. This is consistent with a conclusion that a POSITA could have easily configured Park in view of Fang's teachings to have an etch-stop layer within the broad claimed thickness range of 10 to 1000 nm.

C. Claim 15:

1. **[15] “The semiconductor structure of claim 14, wherein thicknesses of the etch-stop layer is the same on the side and top surfaces of each step.”**

192. In addition to Park in view of a POSITA's knowledge (§XV.N.1), Park in view of Fang renders obvious claim 15.

193. Fang discloses that “[t]he thickness of the etch stop material 130 on the stairs 125 may be substantially uniform.” Ex. 1007, [0021]. In light of that, *thicknesses of the etch-stop layer* (“etch-stop layer” 110b) *is the same on the side and top surfaces of each step.*

194. A POSITA would have been motivated to apply Fang's teaching with the knowledge that an etch-stop layer of uniform thickness on all steps was desirable, as explained above. §XV.N.1 (citing Ex. 1017). Further, a POSITA would have had a reasonable expectation of success because a uniform thickness is consistent with Park's repeated references to “*the* thickness of the etch-stop layer.” Ex. 1006, [0006], [0060], [0067], [0070]-[0071]. Furthermore, a layer of uniform thickness was common and easily achieved through techniques used to deposit a conformal

etch-stop layer such as chemical vapor deposition (CVD) or atomic layer deposition (ALD). This would have bolstered a POSITA's reasonable expectation of success.

D. Claim 17:

1. [17] **“The semiconductor structure of claim 13, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.”**

195. The additional limitation of claim 17 is identical to that of claim 10. Park in view of Fang renders it obvious for the same reason as explained above. §XVI.B.1.

E. Motivation to Combine

196. In addition to the reasons already stated (§§XVI.A.1, XVI.C.1), a POSITA would have been motivated to apply Fang's disclosures of the coplanar configuration and the etch-stop-layer thickness on Park's staircase structure and would have had a reasonable expectation of success in doing so.

197. To begin, the two references focus on solving the same problem using similar techniques. Both Park and Fang are directed to reducing defects in 3D memory devices due to over-etching shallow openings when forming openings for the word line conductive structures. Ex. 1006, [0014], Ex. 1007, [0004]. A POSITA would have understood that Park and Fang have the same goal, for example, “improv[ing] reliability” of a “high[ly] integrat[ed]” 3D memory device by reducing “processing ... , complexity, and cost” of the manufacturing process. Ex. 1006,

[0003]; Ex. 1007, [0004]. A POSITA would have known that such manufacturing processes involve many parameters and would have found Fang's "specific details" useful to supply information, such as thickness of the etch-stop layer, that Park does not specify. Ex. 1007, [0009]. Therefore, a POSITA would have been motivated to consult Fang in addition to Park for a more complete combined teaching on addressing the same issue. Fang discloses a single etch-stop layer, while Park discloses two, but a POSITA would be able to choose either option to satisfy the need to etch conductive structures to the word lines without over- or under-etching with a suitable choice of the etch stop thicknesses.

198. A POSITA would have known that Fang's range of etch stop thickness was reasonable, especially in light of the additional flexibility provided by other process parameters as explained above. Such additional flexibility also makes the required thickness more flexible, increasing the likelihood that some thickness within the wide range claimed by the '711 Patent would work well with Park's device. A POSITA thus would have had a reasonable expectation of success in adapting Park's etch-stop layer to Fang's disclosure, as explained above. §§XVI.B.1-XVI.C.1.

199. Further, a POSITA would have had a reasonable expectation of success because of similarities between Park's and Fang's disclosures regarding the etch-stop layer. For example, Park discloses that its etch-stop layer may be formed of a

material having an etch selectivity with respect to the connection region insulating layer through which vertical openings are formed. Ex. 1006, [0050], [0108] (“the etching process for forming the plurality of vertical openings (210) may have a predetermined etching selectivity with respect to the etch-stop layers (110a, 110b)”). Fang discloses the same. Ex. 1007, [0020] (“The etch stop material 130 may be any material that is not substantially removed (e.g., etched) during removal and replacement of the nitride materials 120 of the staircase structure 105.”). Park discloses that its etch-stop layer may be formed of silicon nitride. §XV.F.1. So does Fang. Ex. 1007, [0020]. A POSITA would have expected such similarities since Park’s and Fang’s devices are analogous.

200. Moreover, a POSITA would have had a reasonable expectation of success because Park’s and Fang’s disclosures are directed to similar 3D memory devices with staircase word-line structures. For example, both comprise alternating conductive and dielectric layers at each step, one or more etch-stop layer and an insulating layer on the steps, and conductive structures penetrating the various layers to form contacts with the conductive layers. Again, a POSITA would have expected such similarities since Kim’s and Park’s devices are analogous. These components and the structure itself were routine and conventional, well within the knowledge of a POSITA.

201. As explained, a POSITA would have found it obvious that Fang's thickness range could be applied to Park's device and would have been motivated to do so to fill in a parameter that Park does not disclose. Although Park's embodiment relied on in this Declaration discloses an additional barrier layer, Park also discloses an embodiment with a single etch-stop layer 110 like Fang. Ex. 1006, Fig. 4, claim 1 (claiming one or more etch-stop layers). And Park makes no distinction regarding the thickness of its etch-stop layer based on the number of etch-stop layers in the embodiment. *See generally id.* This is consistent with a POSITA's understanding that the etch-stop thickness was flexible based on other parameters, such as the choice of etchant and layer thickness. By adjusting other factors, the presence or absence of the barrier need not matter to the etch-stop thickness. Therefore, a POSITA would have found it obvious that Park's etch-stop layer could be adapted to Fang's thickness range.

202. Additionally, a POSITA would have been motivated to apply Fang to make the top surface of the etch-stop layer coplanar with those of the insulating layer and conductive structure. First, Park itself teaches planarization as a way to remove unnecessary materials at the top of the staircase structure. Ex. 1006, [0089]. Based on Fang's disclosure, it would have been obvious that the materials above the top surface plane of the etch-stop layer is unnecessary. §XVI.A.1. Indeed, as explained above, a POSITA would have understood that making the top surfaces of the

insulating layer and conductive structure coplanar with the top surface of the etch-stop layer would have been compatible with Park's device. §XVI.A.1. Therefore, the extent to which the materials above the top surface plane of the etch-stop layer are removed is simply a matter of design choice. A height either as disclosed by Park or by Fang would have been a suitable choice. Further, Fang's configuration reduces the overall height of the structure, reducing device size, which is desirable for memory devices.

203. A POSITA would have had a reasonable expectation of success to apply Fang's coplanar disclosure to Park's device. The modification simply extends Park's existing planarization process to remove a greater thickness of the same materials that Fang makes clear to be unnecessary. And Park already teaches that its planarization process serves to remove unnecessary materials. Additionally, this modification is compatible with Park's device. §XIII.A.1.

XVII. SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS

204. During my review of the materials discussed herein, I did not become aware of any evidence suggesting the existence of any secondary indicia or considerations of non-obviousness. In the event that Patent Owner proffers any such evidence, I shall provide my opinions on such evidence in a reply declaration.

XVIII. DECLARATION

205. In signing this declaration, I realize that this declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the USPTO.

206. I am aware that willfully false statements and the like made by me in connection with this declaration are punishable by fine or imprisonment, or both (18 U.S.C. § 1001) and may jeopardize the validity of the Petition. All statements herein made by me of my own knowledge are true and all statements made on information and belief are believed to be true. I declare under penalty of perjury that the foregoing is true and correct.

Executed this 12th day of November 2024 at Austin, Texas.



Sanjay Banerjee, Ph.D.