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Si, SiGe, Ge, and III-V Semiconductor Nanomembranes and Nanowires Enabled by SiGe Epitaxy

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SiGe epitaxy in conjunction with selective etching lends itself as an excellent method for manufacturing of nanomembranes and nanowires as well as for "universal" semiconductor substrates capable of accommodating various advanced CMOS including optoelectronics applications. Early device application of this technique has been demonstrated for the device architecture of SON and GeON MOSFETs allowing accommodation of a SOI-type and GeOI devices on a bulk Si wafer. This approach has been successfully extended to multi-channel and multi-nanowire devices. Together with the availability of thin Ge layers (e.g. by virtue of Ge condensation), SiGe epitaxy opens up the possibility of a heterogeneous co-integration of high efficiency III-V multijunction solar cells, III-V complementary logic, thermophotovoltaic device structures, lasers, modulators and detectors. Furthermore, the nanomembranes and nanowires lend themselves for exploration of differences between material 3D (bulk) properties and 2D (nanomembrane and nanoribbon) and 1D (nanowire) structures.

Introduction

Selective SiGe epitaxy on Si layers coupled with the ability to remove one type of the layer while leaving intact the other by highly selective isotropic etches, offers a wide range of enabling semiconductor substrates as well as the ability to manufacture monocrystalline semiconductor membranes and nanowires in a cost-effective and in a well-controlled way. It is well known that epitaxy allows one to control the thickness of the thin epitaxial layers and by extension membranes as well as cross-section of semiconductor wires with the help of spacer technology to a few nanometers. Silicon-On-Nothing technology (SON) [1] has demonstrated that local SOI areas can be defined on a Si bulk wafer and similarly the Germanium-On-Nothing (GeON) [2] approach has achieved the same objective in establishing local GeOI-like areas on Si bulk wafers.

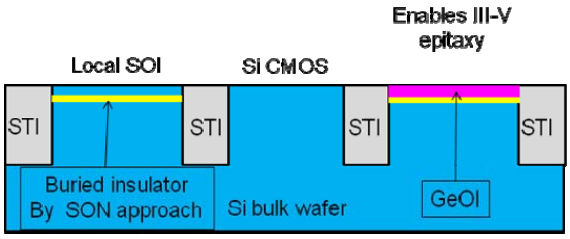

Fig.1 Universal wafer allowing bulk Si CMOS, SOI, GeOI, and solar cells and optoelectronics enabled by the Ge seed layer.

With these techniques a universal semiconductor substrate can be realized (see Fig.1) unifying CMOS, SOI, GeOI as well as applications enabled by compound semiconductors grown on Ge seed layers (see also Fig. 19 below). The basic mechanism of epitaxial growth of multi-stack layers composed for example of SiGe/Si or Ge/GaAs or

Micron Ex. 1014, p. 1
Micron v. YMTC
IPR2025-00117

GaAs/AlAs, followed by subsequent selective etches of targeted sacrificial layers enables manufacturing of multichannel devices in a nanometer regime as well as of semiconductor nanomembranes and nanowires in a well-controlled top-down approach on ubiquitous Si wafer substrates. In Fig. 2, a collection of GaAs membranes is shown, reported recently by Yoon et al [3]. Such compound semiconductor membranes can also be manufactured by virtue of substrates shown in Fig. 1 on Si bulk wafers using SiGe epitaxy.

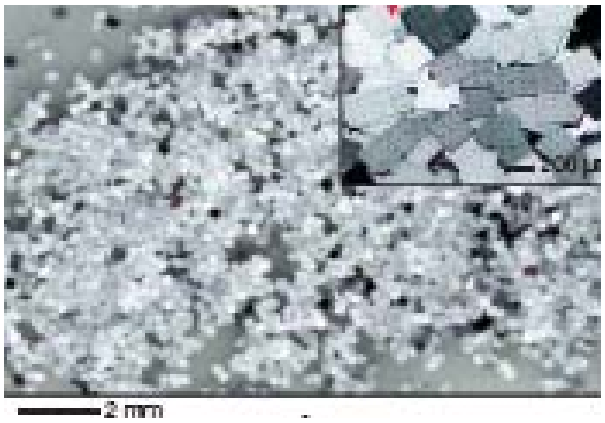

Fig. 2 A pile of GaAs 200 μm x 200 μm membranes [3].

Thus it is apparent that by utilizing SiGe epitaxy on Si substrates in concert with the selective etches between Si and Ge, the entire CMOS legacy together with its infrastructure can be leveraged for diverse breakthrough technologies including most of the compound semiconductor applications. Here, the ability to provide monocrystalline local Ge seed layers on bulk Si wafers is the crucial element for the integration of heterogeneous of compound semiconductors on Si bulk wafers (see also Fig.19). The close lattice constant match between Ge and GaAs makes it relatively easy to grow high quality buffer layers enabling high-speed device, optoelectronics, laser, and thermophotovoltaic applications.

The paper is organized as follows: in section 2, the SON [1] and the related localized SOI (LSOI) processes are reviewed. Here, we do not focus on the properties of the transistor, for which the process integration was originally conceived, but on the method's ability to generate local SOI areas on bulk Si wafers. In section 5, the SON method is extended to incorporate Ge active layers with the crucial addition of Ge condensation process step which is called Germanium-On-Nothing (GeON) [2] leading to formation of local GeOI areas on a Si bulk substrate. In cases of SON and GeON, the transistor applications are only mentioned for historical and illustrative reasons. It will be seen that the transistor aspect matters only as far as some simple substitute for the gate module of the MOSFETs is needed to prevent the collapse of the Si/SiGe structure after the removal of the sacrificial layer. However, the integrity of the tunnel left after selective etch can be preserved by far simpler means than the deployment of an entire gate stack of a leading edge MOSFET. The gate stack of the specific architecture of a MOSFET motivated the development of SON and GeON techniques, but now these techniques stand on their own, and can be used to provide various semiconductor seed layers on Si bulk wafers and to enable an efficient manufacturing of low dimensional nanostructures. In section 3, the SiGe and Si epitaxy facet-free processes are briefly characterized. In section 4, the highly selective etches between Si and SiGe and some of its limitations are described. In section 5, as already mentioned, the composite process of SON followed by Ge condensation is described leading to the desired utility of local GeOI. In section 6, a variety of multichannel devices is reviewed and it is shown that the underlying method lends itself also to a production of nanomembranes and nanowires. In section 7, the discussion of the Si/SiGe system is extended to GaAs/AlAs systems grown on Ge seed layer embedded in a Si bulk wafer.

Silicon-On Nothing process enabled by sacrificial SiGe epitaxial layer

SiGe alloy can be deposited defect-free on Si with the same lattice constant (in the growth plane) provided that it does not exceed the critical thickness for plastic relaxation. SiGe can be buried between mono-Si layers and be

Micron Ex. 1014, p. 2
Micron v. YMTC
IPR2025-00117

used as a sacrificial layer for lateral etching. In this approach, high selectivity between SiGe and Si is crucial. The selective etching between SiGe and Si is described in more detail in section 4. Very thin films of monocrystalline semiconductors have been recognized for their scaling potential of CMOS transistors [4-10]. Various fabrication technologies (SIMOS, BESOI, Smart Cut, ELTRAN, ELO etc) have been developed to provide thin Si films on buried oxide, but they are all bedeviled – to various degrees - by uniformity, defect, and cost issues. In this context, SON offers a very convenient way to manufucture of extremely thin films and very thin dielectric layers. The SON process is CMOS-compatible to produce thin-film SOI-like devices [1, 11-17]. For this purpose, two selective epitaxial growth (SEG) steps need to be performed after the formation of shallow trench isolation (STI). The first SEG eiptaxy grows selectively a SiGe layer on Si, and the second SEG grows selectively a Si layer on SiGe in predefined active Si areas of the substrate. After the conventional gate stack formation, the STI trenches (or the outer portions of the active region) are recessed to provide access to the SiGe layer, which is subsequently etched out. After the etch step, the gate stack together with spacers is hanging over the void (or tunnel) created by the SiGe etch. It should be noted that the top Si layer and the gate module stay suspended over the tunnel since the gate is anchored on the isolation surrounding the active area of the transistor. Subsequently, the tunnel is oxidized and filled with Si_3N_4. To complete the transistor the SiO_2 and Si_3N_4 are removed from source/drain regions and selective Si epitaxy is employed to reconstruct the source/drain electrodes. The SON process in its LSOI version [18] for a MOSFET is shown in Fig. 3.

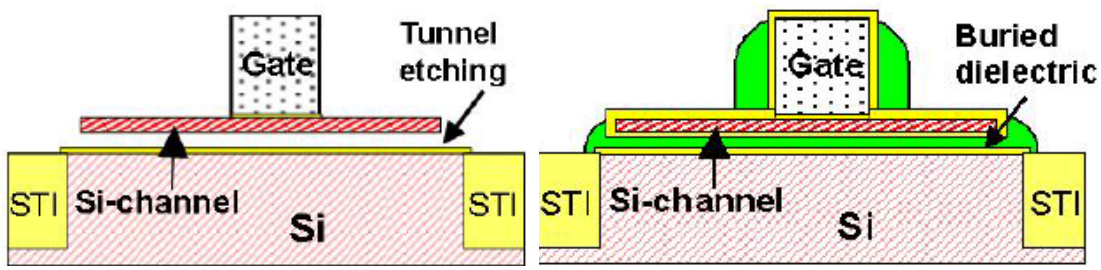

Fig. 3 The principle of the SON proces in the version of the so-called localized SOI [18].

The SON process can be extended to localized SOI (LSOI) approach [18] in which the tunnel underneath the active Si extends over the entire active region from one STI trench to another. The original SON process provided a SOI channel only underneath the gate with source/drain regions still being embedded in bulk silicon. The LSOI process removes the necessity of breaking the unity between source/drain and channel regions. The indispensable access to the buried SiGe layer is obtained by time-controlled underetch of STI just deep enough to expose a vertical sidewall with the SiGe layer. Then the crucial selective etch of SiGe relative to Si allows entire removal of the sacrificial SiGe layer. The remaining Si-cap layer then remains suspended over the tunnel and is supported by the gate stack that bridges the active area and is anchored on the STI isolation. The resulting tunnel (dark) and the Si-cap layer are shown in Fig. 4. Typically, the resulting SOI-like transistors have a silicon channel thickness of 10 nm and are disposed on about a 30 nm thick composite dielectric layer (SiO_2/Si_3N_4) that isolates the channel from the bulk. It should be also mentioned that the SON/LSOI process can be readily adapted to fabricate double gate or gate-all-around (GAA) MOSFETs [19]. The GAA SON based process starts with selective epitaxial growth of SiGe followed by that of Si on active areas isolated by STI. The SiGe/Si stack is then patterned by Reactive Ion Etching (RIE) into strips encroaching on the STI isolation. Subsequently, the underlying SiGe is selectively etched out and a dielectric is deposited by oxidation or by Atomic Layer Deposition (ALD) to fill the gap between Si channel and the substrate. The subsequent RIE provides the desired gate electrode geometry.

SiGe and Si selective epitaxy

SiGe alloy can be deposited on Si while keeping the same lattice constant as long as the SiGe layer thickness is lower than the critical thickness to prevent plastic relaxation and defect formation. This critical thickness decreases with the Ge content of the SiGe layer. The Si and SiGe layers are grown on (100) Si substrates by reduced pressure chemical vapor deposition (CVD).

Micron Ex. 1014, p. 3
Micron v. YMTC
IPR2025-00117

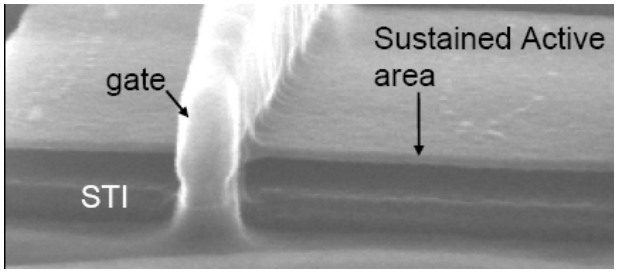

Fig. 4 A thin Si layer is suspended over the tunnel region created by the removal of sacrificial SiGe layer [19].

The Ge content has been varied between 10% and 50%. For a typical Ge content of 30% the critical SiGe thickness is about 40 nm. Layers of SiGe of 20 nm have been grown - i.e. markedly below the critical thickness of 40 nm. As a consequence, the SiGe layer was fully pseudomorphic, which induces a biaxial compressive strain within the SiGe layer. The subsequent Si layer of about 13 nm is fully relaxed. One of the key processes of the local SOI (LSOI) approach was the control of the facet-free epitaxy process. This technique is crucial to the ability to grow the SiGe/Si layers without the formation of facets at the shalow trench isolation STI edges. In this way, direct access to the buried SiGe layer becomes possible for the subsequent selective removal of the SiGe layer. In-situ HCl etching was used to create a short recess (~30nm) of the active area after the STI integration. This recess was directly followed by the $Si_{0.7}Ge_{0.3}$ epitaxy (sacrificial layer), and the process was followed by the mono-Si growth on the SiGe-cap layer. The Fig.5 shows the morphology of those layers, without facets formation along the STI.

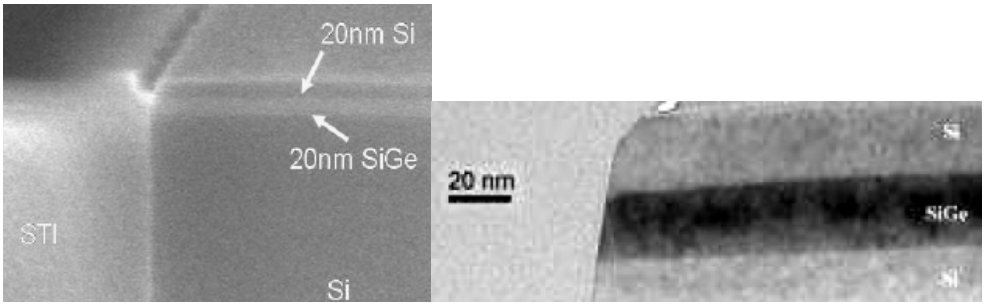

Fig. 5 Facet-free epitaxy process of $Si_{0.7}Ge_{0.3}$/Si growth [19].

Selective etching of sacrificial layers of the SiGe-Si layer system

Multiple epitaxial layer system of alternating SiGe and Si layers can be used either to etch sacrificial SiGe layers relative to Si or to etch sacrificial Si layers relative to SiGe layers as shown in Fig 6. In both cases highly efficient selective etches have been developed. The case of selective SiGe etch is described first. Three different etches have been developed [20] for selective SiGe etch relative to Si: 1) chemical plasma etching using pure CF_4 as the etching gas in a downstream plasma reactor; 2) HCl etching; and 3) wet etching using the chemistry $HF/HNO_3/CH_3COOH$. The first method, although plasma-based, does not require any ion bombardment and consequently no bias voltage is applied to the electrostatic chuck. The same isotropic chemical reactivity is expected as compared with wet etching solutions. The plasma is generated in a quartz tube by a microwave generator at 2.45 GHz. The plasma species then diffuse through a teflon tube before reaching the etching chamber. Due to numerous recombination processes no ion species reaches the etching chamber. Only neutral atoms, molecules, and very long-lived species such as fluorine radicals, which are the main etching species, remain in the etching gas. The fluorine radicals react with Si to form SiF_4 volatile molecules. The selectivity of SiGe relative Si is achieved through the role of Ge in SiGe layer. It turns

Micron Ex. 1014, p. 4
Micron v. YMTC
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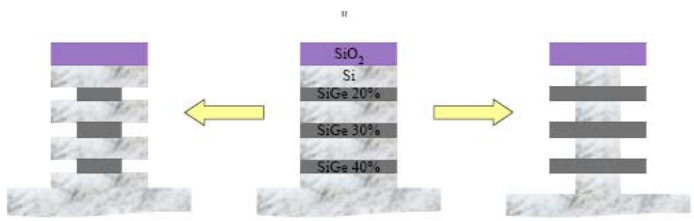

Fig. 6 Selective etching of SiGe:Si (left arrow) and of Si:SiGe (right arrow).

out that the Si-Ge bond (3.12 eV) is sufficiently weaker than the Si-Si bond (3.25 eV) [21]. (The ultimate mechanism for the selectivity is still not very well-known.) This suggests that the formation of SiF_4 volatile species is easier for SiGe than it is for pure Si. Of course, the preference of formation of SiF_4 in SiGe increases with the Ge content. The process parameters have been optimized to achieve a complete removal of the SiGe layer with a minimal overetch of the Si layers. A typical etching time is 25-60 sec. The result of an incomplete (partial) etch is shown in Fig.7.

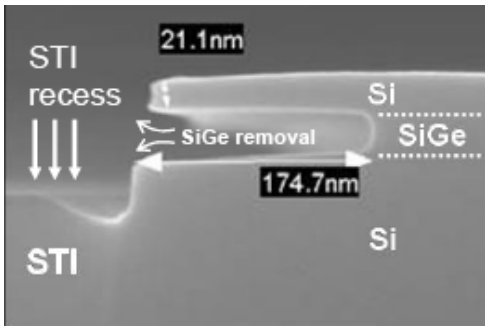

Fig 7. SEM cross-section of partially etched SiGe layer.

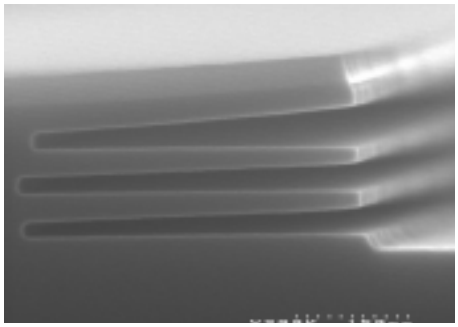

Fig.8 Selective etch of multilayer system

A test structure, shown in Fig. 8, demonstrates the action of the selective etch on a multilayer Si/SiGe system. As can be observed, there is a slight bevel at the entrance for chosen parametes. In Fig. 9 a SEM cross-section of 120 nm long tunnel (etched SiGe) with a 12 nm monocrystralline Si layer is shown. It can also be seen that the thickness uniformity of the Si layer is excellent. Compared with the original Si epi layer of 13 nm only 1 nm has been lost. Longer etch times might result in thinning of Si layers or in non-uniform channel thickness with a bevel at both ends.

The etch rate of SiGe with 30% Ge content is about 120Å/min and the SiGe-to-Si selectivity is about 80-100. Doping of silicon seems also to affect the SiGe etch selectivity; for As-doped Si the selectivity decreases, whereas the selectivity increases for B-doped Si. However, by adding a small amount of oxydgen to the CF_4, the etch selectivity can be increased [22]. In the latter case, no Si etching could be detected. Similar etch selectivities can be achieved using the hot HCl etch. In this case, the etch rate of SiGe at the same Ge content is however much lower about 10Å/min but the SiGe-to-Si selectivity is slightly higher 100-120. The disadvantage of the HCl etch method is that it has a very slow etch rate for Ge contents lower than 30%. Finally, the wet etching approach using $HF/HNO_3/CH_3COOH$ chemistry can be used. An etch rate of 115Å/min of SiGe at [Ge]=30% has been achieved with an excellent selectivity of about 200. However, the etch rate depends strongly on the Ge content as shown in Fig. 10. The bottom SiGe layer with Ge content of 15% etches much slower than the top SiGe layer with [Ge]=30%.

Micron Ex. 1014, p. 5
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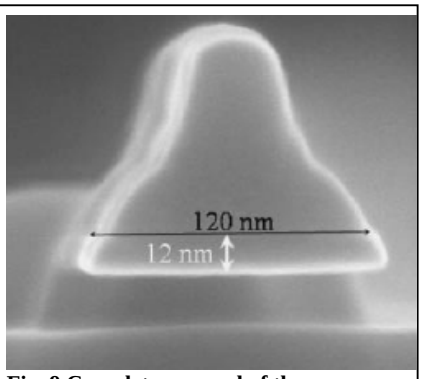

Fig. 9 Complete removal of the sacrificial SiGe layer [20].

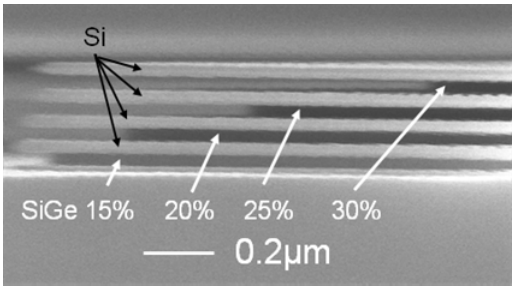

Fig. 10 Selective etch of SiGe with varying Ge content.

Finally, the "reverse" selective etching can be used to remove Si selectively to the SiGe material. Here also a combination of both dry and wet approach is feasible. The dry etch method uses a combination of $CF_4/O_2/N_2$ gases. It has been found that the Si etch rate is considerably fast (about 130 nm/min) and the selectivity for Ge contents above 20% is infinite. An SEM image of the Si etch selective to SiGe is shown in Fig. 11.

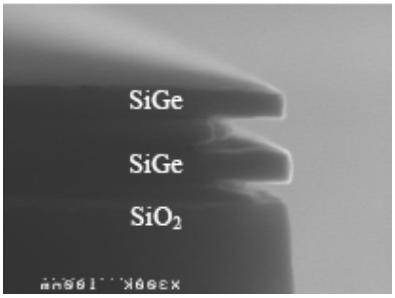

Fig. 11 Selective etching of Si relative to SiGe.

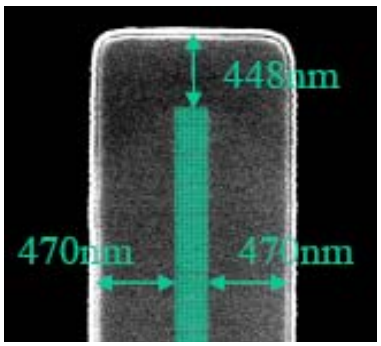

Fig. 12 Isotropic etching of SiGe seen underneath the semi-transparent Si layer.

The wet selective etching operates on the principle of silicon oxidation using an oxidation agent such as HNO_3 or H_2O_2 with an etching agent (HF). For the wet SiGe etch the selectivity to Si is 63, 83, and 115 and for SiO_2 is 25, 50, and 74 for [Ge]=20%, 30%, and 40% respectively. The etch rate and selectivity increase with Germanium content. Moreover, the selective SiGe etch is isotropic as shown in Fig. 12. The SiGe removal could be monitored with SEM and the remaining SiGe could be detected by the contrast in electron transparency. In this way, the depth of the etch tunnel can be measured on each sample by a non-destructive metrology as shown in Fig. 13.

There are some limitations, though, to the selective etching and the tunnel lengths attainable. One limitation is associated with residues observed inside the tunnel. In order to prevent residue formation one has to break up the etch time into smaller segments and after each etch rinse the structure. Another limitation observed for long tunnels is the structure tilting, membrane sticking and structure collapse as illustrated in Fig. 14.

Ge-On-Nothing (GeON) by sacrificial SiGe layers and Ge condensation

GeON [2] is using two SiGe epitaxial layers. The first epitaxial SiGe and the Si-cap layers are the same as in the SON approach. However, after completing the SON module 2nd SiGe layer is grown on the Si-cap layer. The process flow for GeON is shown in Fig. 15. The first steps of the procedure are the same as in the case of SON. The process starts with SiGe/Si facet-free epitaxy. After STI recess, SiGe is selectively etched in a remote plasma tool. In one case of a silicon film with no gate module on it, the film can be supported either by SiGe pillars or by dummy gate substitute that can be patterned to hold the silicon film suspended over the void left by SiGe etch.

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Micron v. YMTC
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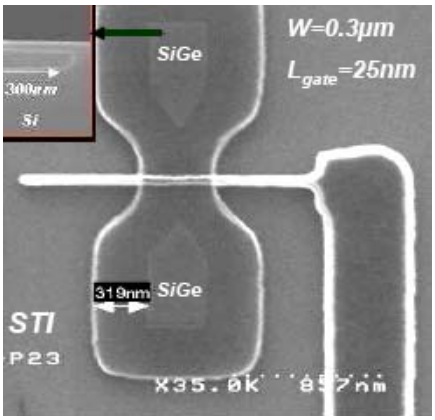


Fig. 13 Rate of SiGe can be monitored by transparency of SEM.

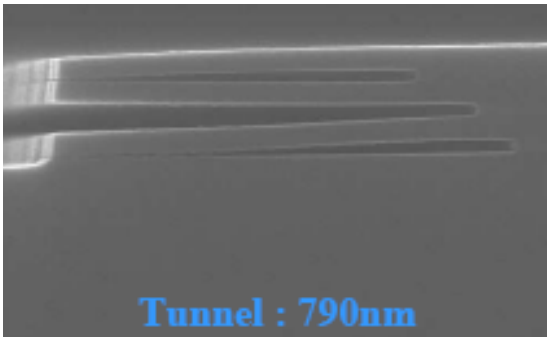
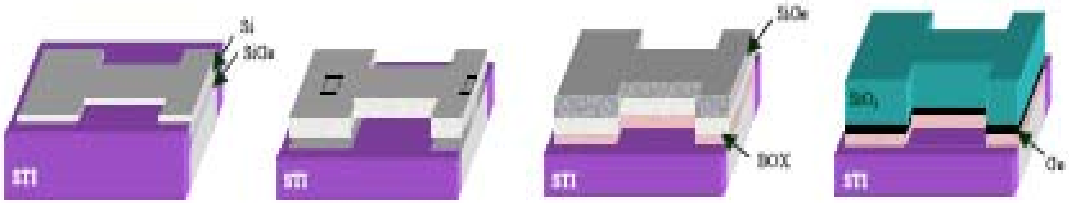


Fig. 14 Sticking of membranes for long tunnels perhaps due to capillary forces.



a) b) c) d)

Fig. 15 GeON process flow: a) SiGe/Si epi, b) STI recess and selective SiGe etch, c) tunnel filling and SiGe epi on the Si-cap layer, d) Ge condensation [2].

The tunnel is then filled with a dielectric to obtain a thin Si film on insulator. After that a second selective SiGe epitaxy is performed. The Ge content and the epi thickness of the 2nd SiGe layer define the thickness and the Ge content of the resulting enriched Ge layer. To obtain a high quality SiGe layer epitaxy is performed at rather high temperature of 750C. The double layer SiGe/Si is then subjected to high temperature wet oxidation to transform the SiGe/Si layer into highly enriched Ge layer. The 2nd SiGe layer on the Si-cap layer is shown in Fig. 16 and the resulting Ge condensed layer in Fig. 17. Fig. 18 shows the morphology of the Ge film. Ge contents of 70%-95% can be obtained depending on the oxidation conditions and the starting material.

An alternative approach to GeOn can be pursued by growing a SiGe/Si/SiGe stack of layers where the first layer is relatively thick and of lower Ge content between 10% and 20%. Then the sandwiched Si layer is etched out selectively relative to SiGe. Subsequently, the tunnel left behind is filled with dielectric material. The result is a SiGe layer directly on top of the buried dielectric layer. The SiGe top layer is then subjected to oxidation resulting in an enriched Ge layer. This process flow integration has the advantage that the condensation process does not have to contend with the enrichment of the intervening Si layer. Consequently, higher degrees of Ge enrichment in the Ge condensation process are achievable.

Micron Ex. 1014, p. 7
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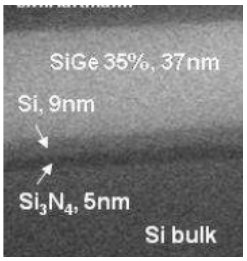

Fig. 16 SEM picture after 2nd SiGe epi, [Ge]=35% [2].

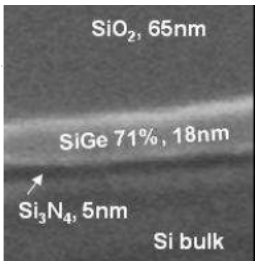

Fig. 17 SEM picture after Ge condensation[Ge]=71% [2].

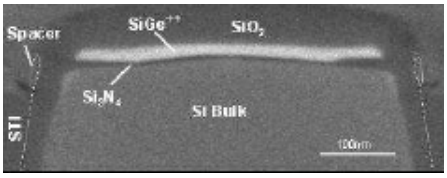

Fig. 18 SEM picture og 500nm long Ge layer [Ge]=88% [2].

In both cases, the buried dielectric layer is a stopping layer against Ge outdiffusion during the oxidation/condensation process step. After condensation, an 18 nm thick Ge-enriched ($SiGe^{++}$) film is obtained. It should be noted that during the condensation the Ge content is largely conserved. For the process conditions mentioned above Ge contents between 71% and 95% can be obtained. Because of the lateral condensation, the Ge enrichment depends on the pattern dimensions. Therefore, smaller active areas lead to faster or higher level of Ge enrichment. The next step is the removal of SiO_2 where precautions have to be taken not to overetch the STI isolation.

The implementation of SON and GeON on bulk Si substrate has already been summarized in Fig. 1. It shows a bulk silicon substrate with local areas of thin SOI with very thin insulator layer and with local areas of Ge layer on thin insultor layer. Thus combined SON and GeON approaches allow a fabrication of a universal wafer substrate that can accommodate traditional CMOS enhanced by SOI-enabled applications including FinFET transistors and III-V epitaxial semiconductor layers that can be grown easily on Ge seed layers. Ge can also be used to accommodate high-performance PMOSFET and NMOSFET transistors and photodetectors. A thin GaAs buffer layer will be grown either by molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD) on the Ge-exposed regions of the patterned GOI/SOI substrate, after which only one MOCVD growth will be necessary to form the optoelectronic devices. Owing to close lattice matching between GaAs and Ge, the threading dislocation density in these regions should be much lower than when grown directly on Si. Since it will not be necessary to restrict carrier motion within the plane of the active region to minimize the impact of non-radiative recombination on laser performance, the gain medium can be built using multiple quantum wells (QWs) instead of a multi-layer, self-assembled quantum dot (QD) structure. In fact, high-performance metamorphic high electron mobility transistors and heterojunction bipolar transistors were demonstrated on Ge and Ge-OI/Si substrates using MBE growth techniques (see Fig. 19) [23,24].

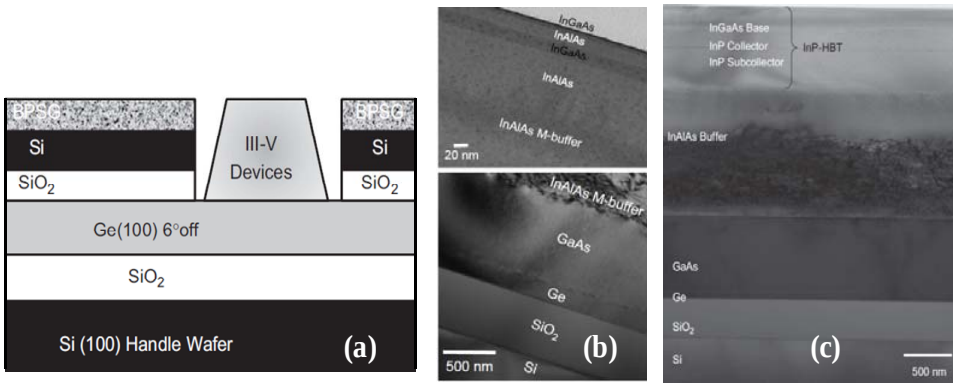

Fig. 19: (a) Schematic showing the placement of III–V epilayers in the growth window of a GeOI/Si substrate; (b) cross-sectional TEM image of an metamorphic HEMT and (c) metamorphic HBT structures grown on an GeOI/Si substrates [23, 24].

Micron Ex. 1014, p. 8
Micron v. YMTC
IPR2025-00117

Multichannel Devices, Nanomembranes and Nanowires

In this section it is shown that alternating stack of Si/SiGe layers lends itself to novel multichannel devices utilizing as a channel body either semiconductor nano-membranes or nanowires. A schematic of a multilayer Si/SiGe structure is shown in Fig. 20 a) and in Fig. 20 b) a SEM picture is shown of partially etched SiGe sacrificial layers. The multilayer structure can be patterned in such a way as to accommodate FinFET [25] architecture. The basic FinFET architecture can be then extended to Multiple-Channel FinFET array [26, 27] (MC-FinFET) allowing n-fold increase of I_{dsat} while providing even tighter gate control of the subthreshold leakage. In this case the fin section of the FinFET is exposed to the selective etch while the larger source/drain sections are masked and are therefore not subject to the SiGe etch. After the fin patterning but before the gate definition, SiGe is etched selectively to Si in the fin area leaving suspended nano-ribbons or nano-rods (depending on the fin dimensions) of silicon (or SiGe) connecting the source and drain regions. On the suspended silicon membranes or nanowires a gate dielectric is formed by oxidation or by the atomic layer deposition. It is noteworthy that this structure allows naturally for the gate-all-around (GAA) configuration which offers the tightest possible short channel control. The channel nanowires can be achieved when the width of the fin and the height of the Si body are of similar dimensions resulting in roughly circular cross-section of the silicon nanowires. In a realization of such a device, the burden for the device processing would lie on the nanowire width definition, since the height of the active region are not overly problematic as they can be controlled precisely by the epitaxy process. The other extreme case of a wide fin and small thickness of Si epitaxial layers would lead to a stack of GAA fully depleted transistors in parallel sharing the same source/drain electrode.

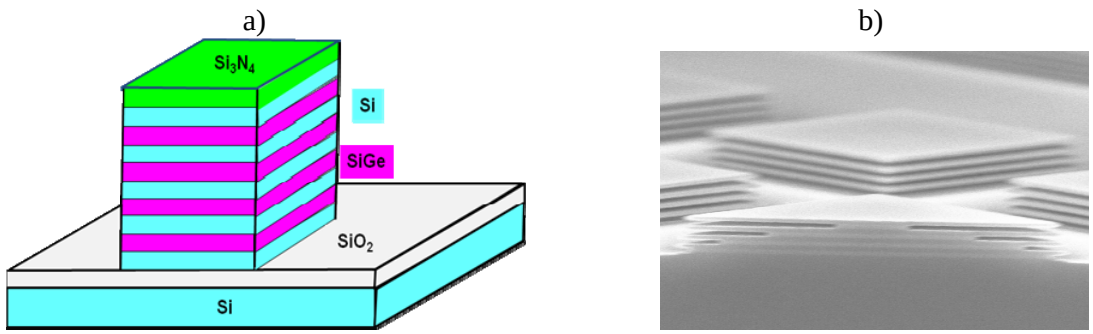

Fig. 20 a) A schematic of a multilayer stack of alternating SiGe and Si layers; b) A SEM of Si nanomembranes with partially etched SiGe sacrificial layers.

The multi-channel structure can be implemented both on bulk and on SOI wafers. This stacked channel architecture, however, does not lend itself to multiple independent gate applications. The final structure of MC-FinFET is shown in Fig. 21 a). Fig. 21 b) shows the cross-section of the fin after the gate electrode module has been completed [28].

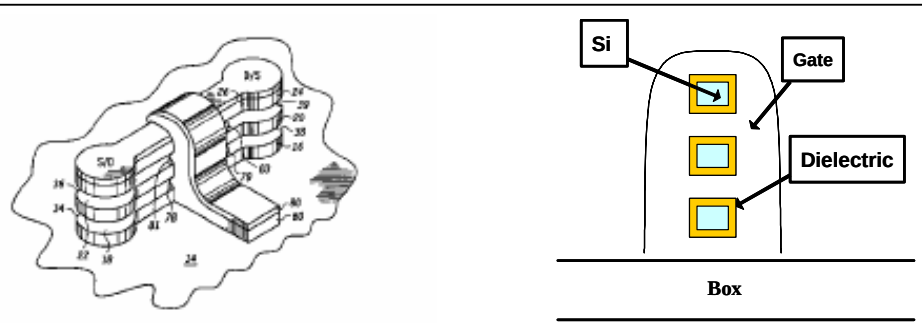

Fig. 21 a) A bird's eye view of the multichannel FinFET architecture with gate wraping around the middle section representing the transistor channel, b) a schematic of the gate and channel cross-section [28].

The discussed multichannel approach can be extended to well-defined multi-nanowire FinFET device by combining spacer technology [29, 30] with the above approach. The combined approach leads to multiple pairs of

Micron Ex. 1014, p. 9
Micron v. YMTC
IPR2025-00117

nanowires suspended between the source/drains of a FinFET-like GAA transistor [31]. In this case the height of the nanowire is determined by the thickness of the Si or SiGe layer and the width dimension of the cross-section is determined by the spacer technology. Both technologies allow a dimension control within 1-2 nm. The resulting structure is shown in the gate-channel cross-section shown in Fig. 22. The Multi-Bridge-Channel MOSFET (MBCFET) [32,33] is another transistor architecture extending the capabilities of a FinFET transistor. It employs also a stack of multiple SiGe and Si epitaxial layers to form a conventional planar MOSFET structure in the first stage of the process. Along with patterned blocking oxide segments placed on the outer portions of source/drain regions, a dummy gate is formed to serve as a mask for the patterning of the Si/SiGe layer stack in the channel region. At this step, the Si/SiGe-stack in the source/drain regions is being anisotropically removed. Thus, the created source/drain cavities allow selective etching of the SiGe in the channel regions. The selective etching proceeds by and large from the source/drain direction. This is in contrast to MC-FinFET where the selective etching proceeds for the most part from the gate direction. In a subsequent process step, the source/drain cavities are filled using selective Si epitaxy. The schematics of an MBCFET with two channel bridges and its silicon implementation are shown in Fig. 23. MBCFET achieves the same objective of n-fold current increase as the MC-FinFET albeit using a different process flow.

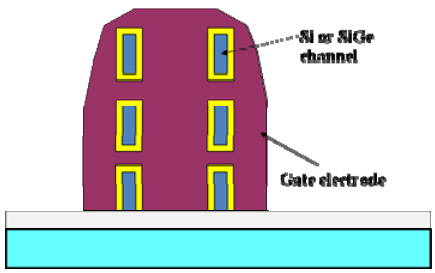

Fig. 22 Cross-section through the gate-channel section of multi-twin nanowire FinFET [31].

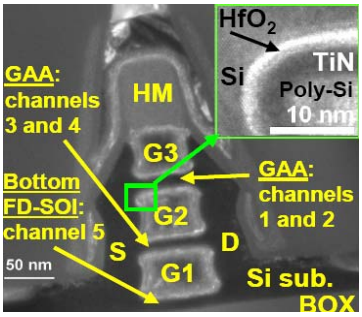

Fig. 23 Cross-section TEM of a 60 nm gate length MC-FET [27].

Besides the mentioned advanced device applications discussed above, the combined method of Si/SiGe epi, the selective etches, and of spacer technology has the ability to create nanostructures such as nano-membranes, nano-ribbons, and nano-wires in a well-defined top-down approach. This opens a possibility to explore the physics of the nanostructures. One inquiry is concerned with the diffusion of dopants in 2D (nano-membranes and nano-ribbons) and 1D (nano-wire) systems as opposed to the bulk material (3D system) properties. Because of the large surface-to-volume ratio, one can speculate that the diffusion is determined mainly by the interface effects. Two papers address the diffusion in Si [33] and Ge [34] nanostructures presented at this conference.

Selective etching of epitaxial compound semiconductor layers

The techniques described above for manufacturing of Si, Ge, and SiGe membranes and nanowires can be readily extended to compound semiconductors. It is known that Ge is very closely lattice matched with GaAs and that is therefore relative easy to grow high quality GaAs epitaxial layers on Ge. What prevents a wider use of this approach is the scarcity of Ge and a high cost of Ge wafers. However, with the GeON method described above, Ge can be made available on any size of Si wafers, either in a blanket manner (GeOI) or localized (GeON) needed for specific applications. (GeOI wafer are available in small quantities from companies such as SOITEC specializing in engineered wafer substrates.) It is well known that compound semiconductors such as gallium arsenide (GaAs) provide significant advantages over silicon for many applications, owing to their direct bandgap and high carrier mobilities. However, growing large, high quality wafers of these materials, and integrating them preferably on Si or on amorphous substrates is very cost-ineffective. There is therefore a keen interest in availibility of methods that yield large quantities of high quality semiconductor material that can serve for various device applications. Recently, Yoon et al [3] described a releasable multilayer epitaxial assembly which fits perfectly well the paradigm discussed in this paper. The basic strategy is shown in Fig. 24 and Fig. 25. Fig. 24 shows a schematic of a multilayer stack of GaAs/AlAs epitaxial layers and the subsequent release of GaAs membranes through selective etching of AlAs layers. It should be noted that GaAs and AlGaAs are lattice matched, resulting in high quality epitaxial layers. The layer stack has to be first patterned into mesa islands through vertical etching using citric acid and hydrogen peroxide at a 10:1 volume ratio [3]. Once the mesa islands are patterned a brief immersion in HF is sufficient to etch the AlAs layers. The etching rate for $Al_xGa_{1-x}As$ over GaAs depends on the Al content [35].

Micron Ex. 1014, p. 10
Micron v. YMTC
IPR2025-00117

Increase of the aluminum content over 70% results in highly enhanced rates of etching in HF. In general, selectivity between GaAs and AlGaAs is very good with aluminum content being above 30%. In the limiting case of x=1, the etching of GaAs is six orders of magnitude lower than that of AlAs [36]. Moreover, the fast etching non-AlAs component may include materials other than GaAs provided that the other materials have sufficiently low etching rate in HF. Fig. 25 shows the layer stack shown on the left side in Fig. 24 after partial etching of the AsAl layers. The GaAs layers are left intact.

Other examples, include InP and InGaAs (with gallium composition of 47%) that are lattice matched and can be etched selectively with respect to one another, and GaAs and GaInP (with indium composition of 50%) that are also lattice matched and can be etched selectively with respect to one another. Similar opportunities exist in GaN, AlN, and SiC systems that can be wet etched selectively [37, 38]. This general approach allows manufacturing of membranes and nanowires of mono-crystalline materials, either freestanding or at predetermined locations and geometries. In Fig. 2 a collection of GaAs membranes (square platelets ~ 200 μm on a side and 4.5 μm thick) is shown formed by release from a three-layer stack.

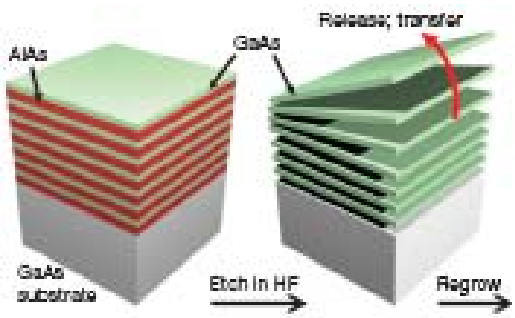

Fig. 24 Schematic illustration of a multilayer stack of GaAs/AlAs and release of GaAs membranes [3].

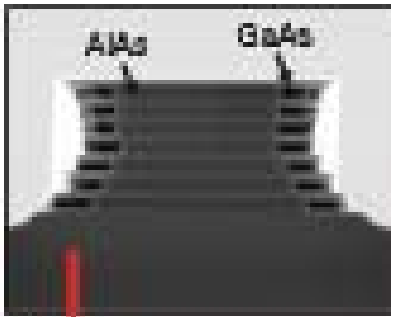

Fig. 25 SEM cross-section of partially etched AlAs layers [3].

Conclusion

SiGe epitaxy in tandem with selective etch capability is a powerful enabler for a wide range of technologies. First, this technique appears to be a natural agent and a boon to bridge the gap between Si and Ge and between Si and compound semiconductors by the intermediate step of Ge collocation on Si bulk wafers. One immediate result is an enablement of a universal substrate which can accommodate the traditional CMOS on bulk Si substrates with local SOI and GeOI as well as the possibility of a heterogeneous co-integration of high efficiency III-V multijunction solar cells, III-V complementary logic, thermovoltaic device structures, lasers, and modulators. Second, the other invaluable benefit of this technique is the ability to manufacture with great precision a variety of nanostructures (nano-membranes, nano-ribbons and nanowires) ranging from micrometer to nanometer dimensions and large range of aspect ratios and made of different semiconductor materials in a time-tested, top-down approach on ubiquitous, inexpensive Si wafers. This encompasses fabrication of multichannel transistors (with multi-membranes or multi-nanowire channels) with the highest drive current per foot print. Insofar this technique allows leveraging of the legacy technological base that led to successful exploitation of the silicon technology and access the wealth of opportunities offered by compound semiconductors. Third, the technique opens a new field of exploration of physics of lower dimensional systems by making available nanostructures of predetermined geometry and of various monocrystalline semiconductor materials.

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References

[1] M. Jurczak, T. Skotnicki, M. Paoli, B. Tormen, J. Martins, J. Regolini, D. Dutartre, P. Ribot, D. Lenoble, R. Pantel, S. Monfray, Electron Devices, IEEE Transactions, vol **47**(11), pp. 2179 – 2187 (2000)

Micron Ex. 1014, p. 11
Micron v. YMTC
IPR2025-00117

[2] E. Batail, S. Monfray, D. Rideau, M. Szczap, N. Loubet, T. Skotnicki, C. Tabone, J. Hartmann, S. Borel, G. Rabille, J. Damlencourt, B. Vincent, B. Previtali, L. Clavelier, Solid State Device Research Conference, ESSDERC 2007. pp. 450 - 453 (2007)

[3] J. Yoon, S. Jo, I-S Chun, I. Jung, H-S, Kim, M. Meitl, E. Menard, X. Li, J. Coleman, U. Pail, J. A. Rogers, Nature **465**, pp. 329-334 (2010)

[4] H. Wong, D. Frank, P. Solomon, IEDM Tech. Dig., pp. 407-410 (1998)

[5] T. Schulz, W. Rosner, L. Risch, U. Langmann, IEDM Tech. Dig. pp. 61-64 (2000)

[6] M. Ieong, E.C. Jones, T. Kanrasky, Z. Ren, O. Dokumaci, R. Roy, L. Shi, T. Furukawa, Y. Taur, R.J. Miller, H. Wong, IEDM Tech. Dig. pp. 441-444 (2001)

[7] R. Chau, J. Kavalieros, B. Doyle, A. Murphy, N. Paulsen, D. Lionnerger, D. Barlage, R. Arghavani, B. Roberts, M. Doczy, IEDM Tech. Dig., pp. 621-624 (2001)

[8] D. Esseni, M. Mastrapasqua, C. Fiegna, G.K. Celler, L. Selmi, E. Sangiorgi, IEDM Tech. Dig., pp. 445-448 (2001)

[9] H. Majima, Y. Saito, T. Hiramoto, IEDM Tech. Dig., pp. 733-736 (2001)

[10] F. Balestra, M. Benachir, J. Brini, G. Ghibaudo, IEEE Trans. Electron Devixces, **37**(11), pp. 2302-2311 (1990)

[11] M. Jurczak, T. Skotnicki, M. Paoli, B. Tormen, J.-L. Regolini, C. Morin, A. Schiltz, J. Pantel, J. Galvier, VLSI Tech. Dig. pp. 29-30 (1999)

[12] S. Monfray, T. Skotnicki, Y. Morand, S. Descombes, A. Talbot, D. Dutartre, F. Leverd, Y. Le Friec, R. Pantel, M. Haond, M.-E. Nier, C. Vizioz, D. Louis, IEEE SOI Conference Proc. pp. 22-25 (2002)

[13] S. Monfray, T. Skotnicki, B. Tavel, Y. Morand, S. Descombes, A. Talbot, D. Dutartre, C. Jenny, P. Mazoyer, R. Palla, F. Leverd, Y. Le Friec, R. Pantel, M. Haond, C. Charbuillet, C. Vizioz, D. Louis, N. Buffet, IEDM Tech. Dig., pp. 263-266 (2002)

[14] T. Skotnicki, M. Jurczak, R. Gwoziecki, D. Lenoble, P. Ribot, M. Paoli, J. Martins, B. Tormen, A. Grouillet, R. Pantel, J. Galvier, IEDM Tech. Dig., pp. 513-516 (1999)

[15] S. Monfray, T. Skotnicki, Y. Morand, S. Descombes, M. Paoli, P. Ribot,A. Talbot, D. Dutratre, F. Leverd, Y. Lefriec, R. Pantel, M. Haond, D. Renaud, M.-E. Nier, C. Vizioz, D. Louis, IEDM Tech. Dig., pp.645-648, 2001

[16] M. Jurczak, T. Skotnicki, M. Paoli, B. Tormen, J. Martins, J.L. Regolioni, D. Dutartre, P. Ribot,D. Lenoble, R. Pantel, S. Monfray, IEEE Trans. Electron Devices. **47**(11), pp. 2179 -2187 (2000)

[17] T. Skotnicki, ECS Proc., p. 391 (2001)

[18] S. Monfray, M.P. Samson, D. Dutartre, T. Ernst, E. Rouchouze, D. Renaud, B. Guillaumot, D. Chanemougame, G. Rabille, S. Borel, J.P. Colonna, C. Arvet, N. Loubet, Y. Campidelli, J.M. Hartmann, L. Vandroux, D. Bensahel, A. Toffoli, F. Allain, A. Margin, L. Clement, A. Quiroga, S. Deleonibus, T. Skotnicki, IEDM Tech. Dig. pp. 693-696 (2007)

[19] S. Monfray, T. Skotnicki, Y. Morand, S. Descombes, P. Coronel, P. Mazoyer, S. Harrison, P. Ribot, A. Talbot, D. Dutartre, M. Haond, R. Palla, Y. Le Friec, F. Leverd, M.-E. Nier, C. Vizioz, D. Louis, VLSI Technology, 2002. Tech. Dig., pp.108-109 (2002)

[20] V. Caubet, S. Borel, C. Arvet, J. Bilde, D. Chanemougame, S. Monfray, R. Ranica, P. Mazoyer, T. Skotnicki, Jap. Journal of Applied Physics, **44** (7B) pp. 5795-5798 (2005)

Micron Ex. 1014, p. 12
Micron v. YMTC
IPR2025-00117

[21] R.C. Weast, CRC Handbook of Chemistry and Physics, 53rd edition (1973)

[22] S. Monfray, T. Skotnicki, S. Borel, "Techniques for SiGe/Si", in Silicon Heterostructures Handbook, editor: J.D. Gressler, CRC Press, pp. 187-209 (2006)

[23] W.K.Liu , D.Lubyshev, J.M.Fastenau, Y.Wu, M.T.Bulsara, E.A.Fitzgerald, M.Urteaga, W. Ha, J.Bergman, B.Brar, W.E.Hoke, J.R.LaRoche, K.J.Herrick, T.E.Kazior, D.Clark, D. Smith, R.F.Thompson, C.Drazek, N.Daval, "Monolithic integration of InP-based transistors on Si substrates using MBE" J. Crystal Growth, **311**, pp. 1979-1983 (2009).

[24] D. Lubyshev, J. M. Fastenau, Y. Wu, W. K. Liu, M. T. Bulsara, E. A. Fitzgerald, and W. E. Hoke, "MBE Growth of M-HEMTs and M-HBTs on Ge and Ge-on-Insulator/Si Substrates" 25th North American Conference on Molecular Beam Epitaxy, Albuquerque, NM, September, pp. 23–26 (2007)

[25] D. Hisamoto, Wen-Chin Lee, J. Kedzierski, E. Anderson, H. Takeuchi, H.; K. Asano, Tsu-Jae King; J. Bokor, Chenming Hu, IEDM Tech. Dig., p.1032 (1998)

[26] Eun-Jung Yoon; Sung-Young Lee; Sung-Min Kim; Min-Sang Kim; Sung Hwan Kim; Li Ming; Sungdae Suk; Kyounghawn Yeo; Chang Woo Oh; Jung-dong Choe; Donguk Choi; Dong-Won Kim; Donggun Park; Kinam Kim;Byung-Il Ryu, IEDM Tech. Dig., p. 627 (2004)

[27] E. Bernard, T. Ernst, B. Guillaumot, N. Vulliet, P. Coronel, T. Skotnicki, S. Deleonibus, O. Faynot, IEEE Trans. on Electron Devices, IEEE Transactions, **56**(6), pp. 1243-1251 and pp. 1252-1261 (2009)

[28] M. Orlowski and L. Mathew, "Method of forming a transistor having multiple channels" US Patent 6,921,700 (2005)

[29] Sung Min Kim; Eun Jung Yoon; Hye Jin Jo; Ming Li; Chang Woo Oh; Sung Young Lee; Kyoung Hwan Yeo; Min Sang Kim; Sung Hwan Kim; Dong Uk Choe; Jeong Dong Choe; Sung Dae Suk; Dong-Won Kim; Donggun Park; Kinam Kim; Byung-Il Ryu;, IEDM Tech. Dig., p. 639 (2004)

[30] C. Ndoye, T. Liu, K. Meehan, H. Baumgart, M. Orlowski "Si Nanowire MOSFET with Gate-All-Around Electrode", paper # 79 at ISDRS 2009, December 9-11, (2009)

[31] M. Orlowski, „Multi-channel transistor structure and method of making thereof " US Patent 7,608,893 (2009)

[32] J.L. Huguenin, S. Monfray, S Denorme, G. Bidal, P. Perreau, S. Barnola, M.-P. Samson, M. K. Benotmane, N. Loubet, Y Campidelli, F. Leverd, F. Abbate, L. Clement, C. Borowiak, D. Golanski, C. Fenouillet-Beranger, F. Boeuf, G. Ghibaudo, T. Skotnicki, International Symposium on VLSI Technology Systems and Applications, pp. 118-119 (2010)

[33] C. Ndoye, T. Liu, M.Orlowski, ECS Conference Las Vegas, October 2010, Proceedings (2010)

[34] T. Liu, C. Ndoye, M. Orlowski, ECS Conference Las Vegas October 2010, Proceedings (2010)

[35] E. Yablonovitch, T. Gmitter, J.P. Harbison, J.P. Bhat, Appl. Phys.Lett. **51**, pp. 2222-2224 (1987)

[36] M. M. A. Voncken, J.J. Schermer, G. J. Bauhuis, P. Mulder, P.K. Larsen, Appl. Phys. A **79**, pp. 1801-1807 (2004

[37] D. Zhuang, J.H. Edgar, Materials Science and Engineering, **R 48**, pp. 1-46 (2005)

[38] G. C. DeSalvo, W. F. Tseng, J. Comas, J. Elctrochem. Soc..**139**(3), p. 831-835 (1992)

Micron Ex. 1014, p. 13
Micron v. YMTC
IPR2025-00117