Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: March 12, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00117
Patent 10,672,711

PATENT OWNER'S PRELIMINARY RESPONSE

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2002	Plaintiff/Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s and Counterclaim Defendant Yangtze Memory Technologies, Inc.'s Opposition to Micron's Motion to Stay Case Pending Inter Partes Review and Post-Grant Proceedings, *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.*, No. 3:23-cv-05792-RFL (N.D. Cal. Feb. 3, 2025), ECF No. 221
2003	Docket Entry Order (issuing temporary stay), *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.*, No. 3:23-cv-05792-RFL (N.D. Cal. Mar. 3, 2025), ECF No. 242
2004	U.S. District Courts–Time Intervals from Filing Date to Beginning Date for Completed Civil Trials, by District, During the 12-Month Period Ending September 30, 2024 (https://www.uscourts.gov/sites/default/files/2025-01/jb_t3_0930.2024.pdf)
2005	RESERVED
2006	Curriculum Vitae of Stephen Campbell, Ph.D.
2007	Declaration of Dr. Campbell ("Campbell")

I. Introduction

Patent Owner Yangtze Memory Technologies Company, Ltd. ("YMTC" or "Patent Owner") respectfully submits this Preliminary Response to the Petition for *inter partes* review of U.S. Patent 10,672,711 ("'711 patent"). As explained below, Petitioner fails to carry its burden to show a reasonable likelihood that at least one of the challenged claims is unpatentable. Thus, the Board should deny the Petition, and no IPR proceeding should be instituted.

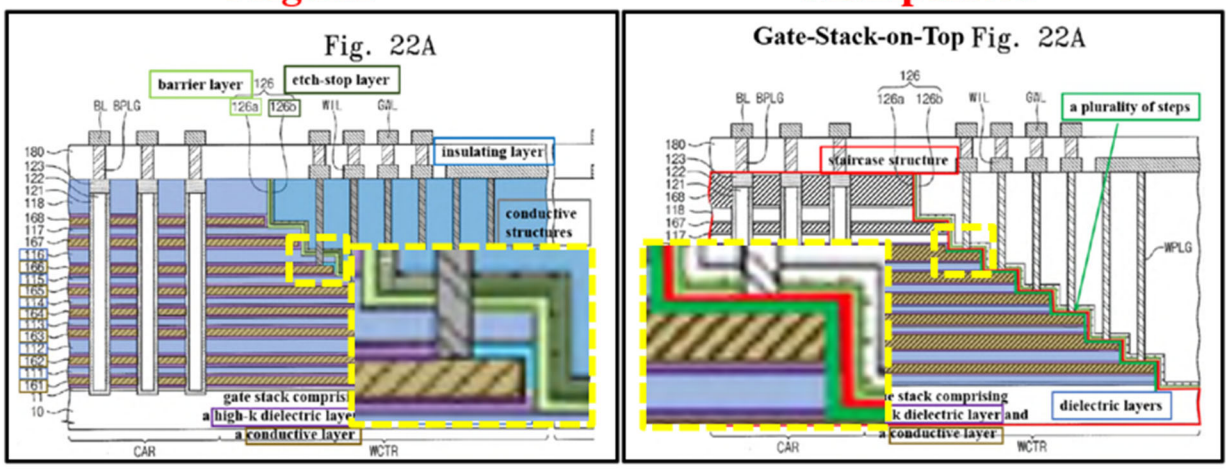
The '711 Patent describes and claims an innovative "staircase structure" for a 3D NAND memory. Specifically, the '711 Patent claims staircase structures with an etch-stop layer, where the gate stack is "disposed over" a dielectric layer. This specific arrangement allows for a single etching process to allow for holes of different depths that connect the gate stack with external devices.

The Petition relies on embodiments from two primary references, Kim (Ex.1005) (Grounds 1-2) and Park (Ex.1006) (Grounds 3-4). The Petition acknowledges that those embodiments all disclose a gate stack ***under*** a dielectric layer. Pet. 29-31. But the Challenged Claims all require "a gate stack ***disposed over*** a dielectric layer"—the opposite configuration. Petitioner resorts to redrawing the figures of Kim and Park to support its arguments.

For Kim, Petitioner changes the "insulating layers" of Kim's original Figure 22 (as annotated by Petitioner in purple) into "gate electrodes" by adding diagonal

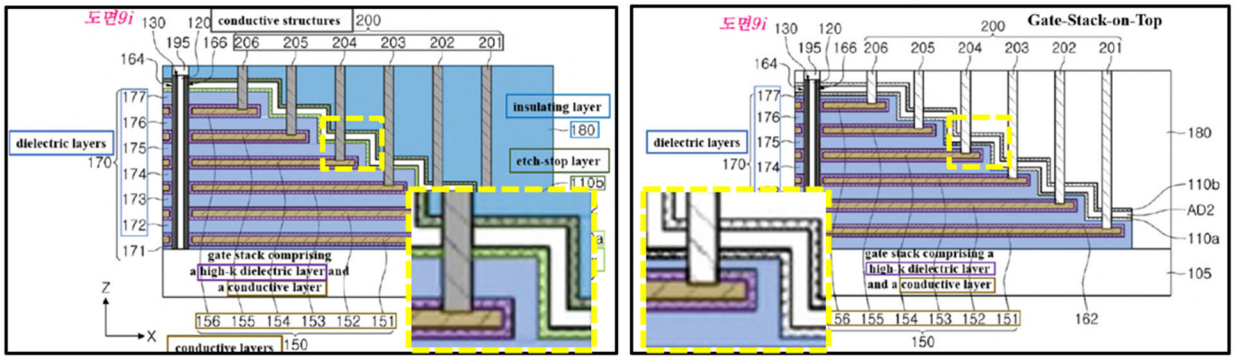
hatches. Petitioner then changes the "gate electrodes" of Kim's original Figure 22 (as annotated by Petitioner in brown) into "insulating layers" by removing the diagonal hatches. This manipulation is shown below.

Original **Manipulated**



For Park, Petitioner similarly exchanges the gate stacks in Park's original Figure 9i (as annotated by Petitioner in brown) and insulating layers so that the gate stacks appear "over" the insulating layers (as annotated by Petitioner in purple), instead of under as Park actually teaches.

Original **Manipulated**



As discussed in greater detail below, Petitioner has failed to provide any reason a POSITA would have been motivated to make such modifications by combining disparate embodiments in Kim and Park. *In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017) ("combining multiple embodiments from a single reference" requires "a motivation to make the combination"). Petitioner identifies no flaw or problem these modifications would address. Nor does Petitioner identify any benefit that would result from the proposed modifications. And Petitioner does not provide any explanation as to why a POSITA would have had a reasonable expectation of success in making these extensive changes, whereby conductive gate electrodes become non-conductive insulators and vice versa.

The Board should deny the Petition.

II. Background

A. 3D NAND Memories

3D NAND memory devices are "memory arrays" with memory cells stacked one on top of the other. Memory cells can be written or read by applying a voltage to corresponding conductors that run horizontally across the memory array, called "wordlines."

An exemplary 3D NAND memory is shown in Figure 5.20 of Petitioner's Exhibit 1011, which depicts a series of vertically stacked memory cells, each controlled by a "Control Gate" (the wordline) shown in red as "CG0" through

"CG3." Ex.1011, 134. In other words, the wordlines serve as the gates of the transistors comprising the memory stack.

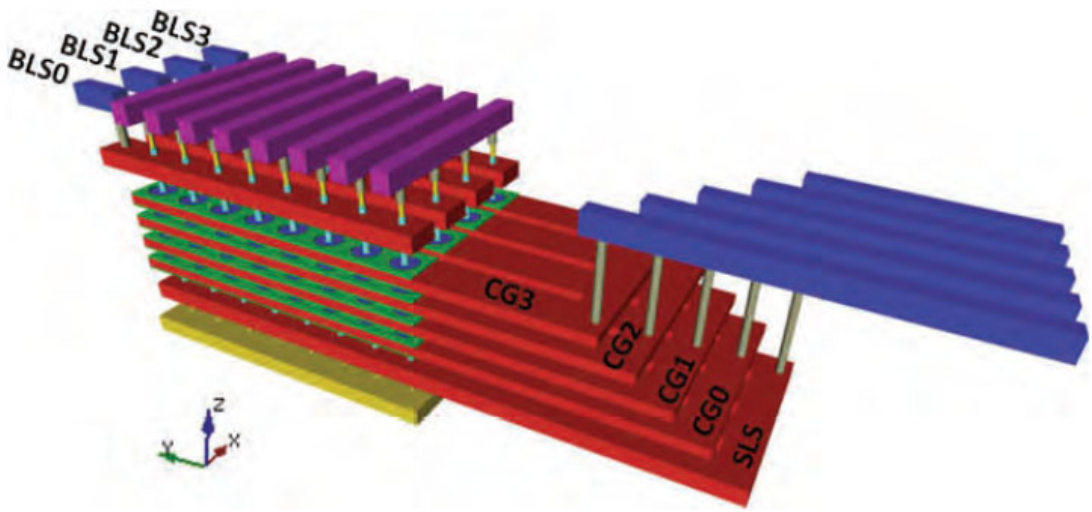


Fig. 5.20 C-FG NAND Flash array with fan-out

The word lines (CG0, CG1, CG2, and CG3) need to be accessed externally to the memory device in order to control the memory. The word lines extend out of one memory array in a staggered manner as shown above, which is sometimes referred to as a "staircase structure." With such a "staircase," the word lines can then be separately accessed through the vertical vias (shown in tan) connected to external conductive lines (shown in blue). Ex.1011, 134.

B. The '711 Patent (Ex.1001)

The '711 Patent discloses "a word line contact structure for three-dimensional (3D) memory array and methods for forming the same." Ex.1001 ("'711 Patent") 1:34-36; Ex.2007 ("Campbell") ¶¶23-27.

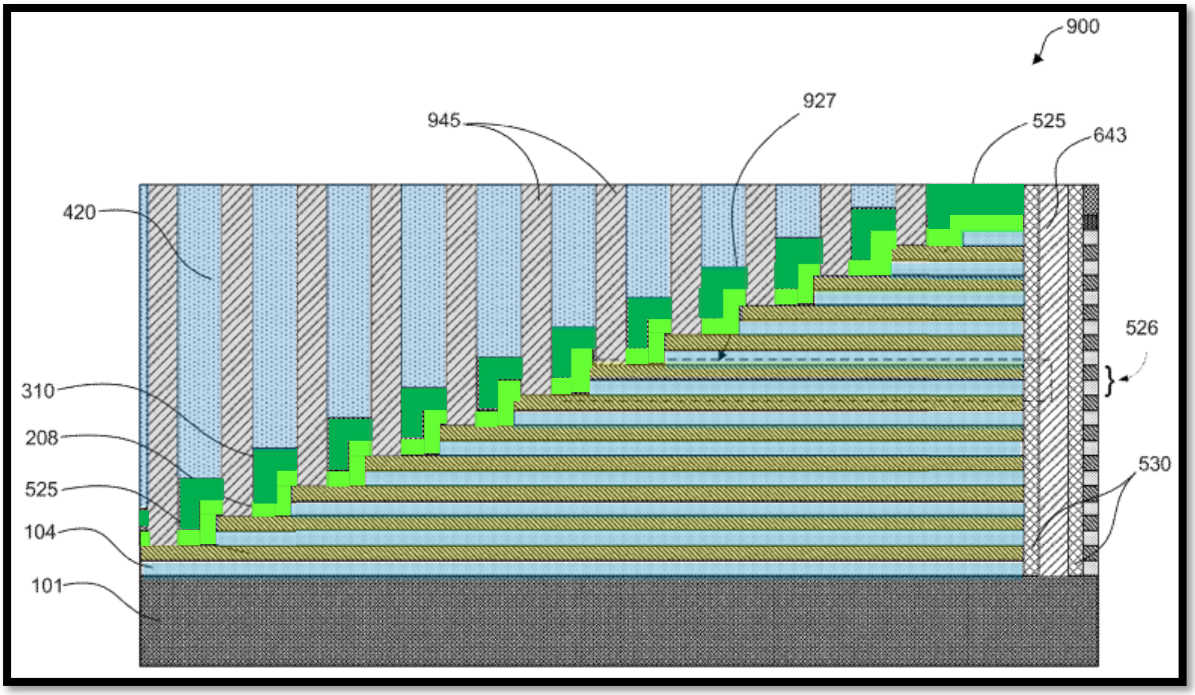
To meet the demand for higher storage capacity in 3D NAND memories, manufacturers have tried to increase the number of conductor/dielectric layer pairs in 3D memory devices. '711 Patent at 5:35-39. The added layers, however, create challenges in etching holes of differing depths above the staircase structure to create the vertical word line contacts. *Id.* 5:40-47. As the '711 patent recognizes, "contact holes for lower levels may be deeper than contact holes for upper levels." *Id.* According to the '711 patent, "[t]ypically, all of the contact holes are formed with a single lithography mask and etching process." *Id.* 5:47-48. But "[o]ften, before contact holes to the bottom levels are entirely formed, the materials exposed in contact holes at the upper levels are over-etched and lost." *Id.* 5:48-51.

The '711 Patent solves the problems of the prior art by disclosing an "etch stop layer" over the staircase structure, which protects underlying staircase structure layers during the etching process and permits the simultaneous etching of all word line holes. '711 Patent 5:54-65. This improves fabrication yield and reduces cost. *Id.* 5:65-67.[1] A barrier layer can also be introduced over the staircase structure "for protecting the underlying structure during subsequent etching

[1] The patented solution also allows the formation of semiconductor interconnect structures for inter-connecting components at different layers with an uneven topology. *Id.* 5:67-6:3; Campbell ¶27.

processes." *Id.* 7:35-39; Campbell ¶26. To implement these structures, the steps of the staircase arrange the gate stacks of the wordlines over corresponding dielectric layers. '711 Patent 6:4-5, 8:54-55, 10:29-34.

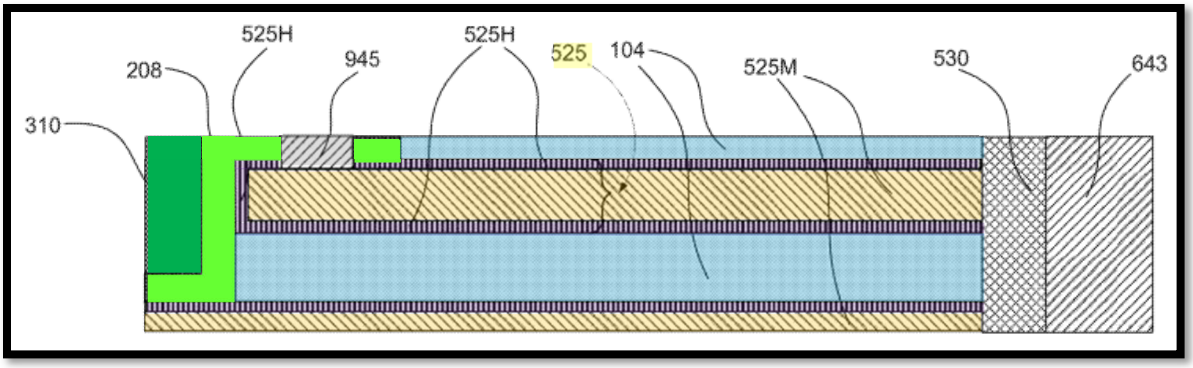
Below is an annotated version of Figure 9A, showing an exemplary '711 Patent 3D memory device staircase structure. The staircase structure 900 includes alternating layers of gate stacks 525 (yellow) over insulating layers 104 (lighter blue). '711 Patent 6:4-5, 8:54-55, 10:29-34. A second insulating layer 208 (bright green) is formed on the top and side surfaces of each step and an etch-stop layer 310 (green) is formed on the second insulating layer. *Id.* 7:30-39, 7:56-58, 7:66-67. A third insulating layer 420 (dark blue) is on the staircase structure 900. *Id.* 8:20-24. Vertical interconnect access ("VIA") structures 945 (grey) are formed in VIA openings 840 in the third insulating layer 420. *Id.* 11:14-19; Campbell ¶28.



No.	Structure
525	Gate Stack
104	First Insulating Layer
208	Second Insulating Layer
310	Etch-Stop Layer
420	Third Insulating Layer
945	Vertical Interconnect Access Conductive Structures

'711 Patent Fig. 9A (annotated) and color key; Campbell ¶28.

Figure 9B shows details of the gate stack 525 of Figure 9A above. The gate stack includes a high-k dielectric layer 525H (purple), which surrounds a gate conductive layer 525M (orange) with one side next to fifth insulating layer 530. '711 Patent 8:65-9:4, 9:40-44. The VIA conductive structures 945 (grey) may be directly disposed on an exposed portion of gate conductive layer 525M. *Id.* 11:16-22; Campbell ¶33.



No.	Structure
104	First Insulating Layer
525H	High-k Dielectric Layer
525M	Gate Conductive Layer
208	Second Insulating Layer
310	Etch-Stop Layer
945	Vertical Interconnect Access Conductive Structures

'711 Patent Fig. 9B (annotated) and color key; Campbell ¶33.

C. Person of Ordinary Skill in the Art

For purposes of this Preliminary Response, YMTC does not dispute Petitioner's proposed level of a person of ordinary skill in the art ("POSITA").[2] Pet. 27. Regardless of the precise definition of a POSITA, Petitioner's grounds do not render any challenged claims unpatentable. Campbell ¶22.

[2] YMTC reserves the right to argue an alternative level of a POSITA in other proceedings or if the Board institutes review.

D. Claim Construction

Petitioner asserts that the terms of the '711 patent's claims have their plain and ordinary meaning. Pet. 26. For purposes of this Preliminary Response, YMTC agrees because Petitioner fails to show that any Ground has a reasonable likelihood of prevailing under any reasonable construction, including their plain meaning.[3]

III. Ground 1: Petitioner Fails to Meet Its Burden to Establish Kim in View of a POSITA's Knowledge Renders Obvious Claims 1-9, 11-16, and 18-19

All Challenged Claims require "a plurality of steps" where "each step comprises a gate stack disposed over a dielectric layer." As discussed below, Kim fails to disclose or render obvious this limitation.

A. Kim Does Not Disclose "each step comprises a gate stack disposed over a dielectric layer"

According to Petitioner, "[t]his Petition relies on Kim's Figs. 17A-22B embodiment." Pet. 29. The Petition alleges that "Kim discloses the gate-stack-on-top layer ordering ***even though its figures show the opposite order***"—i.e., a dielectric layer disposed over a gate stack. Pet. 32-33.[4] That is a non-sequitur. As Petitioner acknowledges, Fig. 22A of the embodiment Petitioner "relies on" shows

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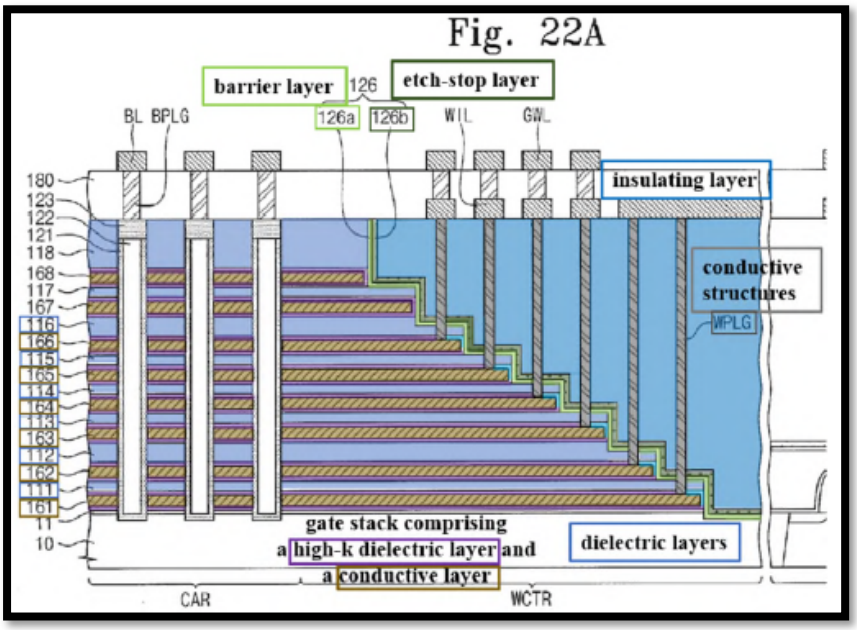
[3] YMTC reserves the right to argue alternative constructions in other proceedings or if the Board institutes review.

[4] All emphasis added unless noted otherwise.

that each step comprises a gate stack 161 to 168 (tan) disposed ***below*** a dielectric layer 111-118 (purple)—not a "gate stack disposed ***over*** a dielectric layer" as required by the claims. Campbell ¶35. Petitioner does not cite anything in Kim's description of the Figs. 17A-22B embodiment that teaches a "gate stack disclosed over a dielectric layer."

Original



Pet. 28 (Kim Fig. 22A); Campbell ¶35. Thus, Kim does not disclose a "gate stack disposed over a dielectric layer" in the embodiment the Petition "relies on."

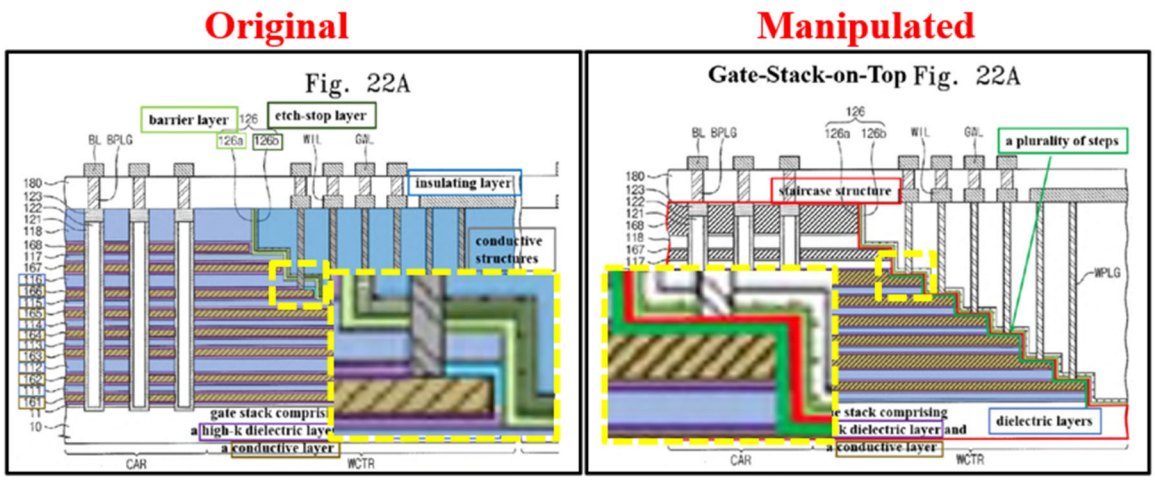
B. Kim in View of a POSITA's Knowledge Does Not Render Obvious "each step comprises a gate stack disposed over a dielectric layer"

Petitioner asserts that Kim "at least renders the [each step comprises a gate stack disposed over a dielectric layer] limitation obvious" in the Figs. 17A-22B embodiment. Pet. 29, 32-33. According to Petitioner, although "[t]his Petition

relies on Kim's Figs. 17A-22B embodiment," Kim "discloses other embodiments, e.g., Figures 5A-14B." Pet. at 29. Thus, as Petitioner recognizes, Figures 5A-14B is a separate embodiment from the embodiment of Figs. 17A-22B. Kim, [014], [017]. Petitioner then cites to various paragraphs about the Figures 5A-14B embodiment to support a wholesale recreation of Figure 22A of the Figs. 17A-22B embodiment that reverses the order of the gate stack and dielectric layer. Pet. 28-29.[5]

In the manipulated version of Fig. 22A Petitioner relies on, Petitioner changes the "insulating layers" of Figure 22A to be "gate stacks" and the "gate stacks" of Figure 22A to be "insulating layers." To do this, Petitioner adds hatching to the insulating layers of the original figure (as annotated by Petitioner) to turn them into gate stacks and removes hatching from the gate stacks of the original figure to turn them into insulating layers as shown below.

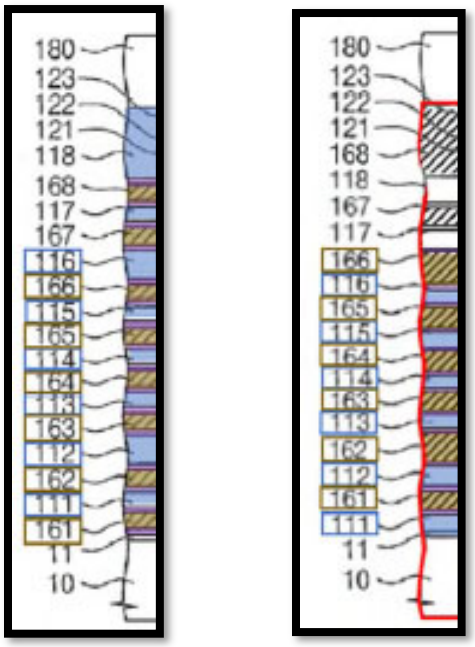
[5] According to Kim, "FIG. 5A through 14A and 5B and 14B are sectional views illustrating a method of fabricating three-dimensional semiconductor memory device of FIG. 4." Kim [0013]-[0014].



Pet. 28 (Kim Fig. 22A), 40 (Kim "Gate-Stack-on-Top Fig. 22A"); Campbell ¶38.

Petitioner then renumbers the labels of Fig. 22A so that Kim's insulating layers are relabeled as gate electrodes and vice versa. For example, Petitioner changes the label "116" (corresponding to an insulating layer) to "166" (corresponding to a gate electrode) and "115" (corresponding to an insulating layer) to "165" (corresponding to a gate electrode), and so on. Campbell ¶¶38-39; Kim [0140] ("gate electrodes 161 to 168"); [0232] ("insulating layers … 111, 113 to 116, and 118"). Based on this manipulation of Kim's Fig. 22A, Petitioner argues that Kim renders obvious the "each step comprises a gate stack disposed over a dielectric layer" limitation. Pet. 36-41.

Original **Manipulated**



Pet. 28 (Kim Fig. 22A), 40 (Kim "Gate-Stack-on-Top Fig. 22A"); Campbell ¶39.

But Petitioner fails to establish that a POSITA would have been motivated to combine Kim's disparate embodiments to arrive at the manipulated figure. Nor has Petitioner shown that a POSITA would have had a reasonable expectation of success in doing so.

1. Petitioner Has Failed To Establish A POSITA Would Have Been Motivated To Combine Disparate Embodiments Of Kim To Arrive At The Claimed "each step comprises a gate stack disposed over a dielectric layer"

Petitioner's proposed modification of Kim suffers a fundamental flaw: Petitioner fails to establish that a POSITA would have been motivated to combine Kim's Fig. 17A-22B embodiment with Kim's Fig. 5A-14B embodiment as Petitioner proposes. Pet. 29.

This Board has consistently held that Petitioners must establish a motivation to combine "disparate embodiments" within a single prior art reference. *Apple, Inc. v. Uniloc Luxembourg, S.A.*, IPR2018-00294, 2018 Pat. App. LEXIS 9221, at *23 (Aug. 8, 2018); *Stepan*, 868 F.3d at 1346 n.1 ("combining multiple embodiments from a single reference" requires "a motivation to make the combination"); *In re Kotzab*, 217 F.3d 1365, 1370 (Fed. Cir. 2000) ("[e]ven when obviousness is based on a single prior art reference, there ***must be*** a showing of a suggestion or motivation to modify the teachings of that reference") (citations omitted). As the Federal Circuit has found, the use of "generic statements" to describe features "[i]n other embodiments" "do not establish" the requisite motivation to combine. *BlephEx, LLC v. Myco Indus., Inc.*, 24 F.4th 1391, 1401 (Fed. Cir. 2022) (finding no motivation to combine features based on prior art's teachings of features "[i]n other embodiments").

Here, Petitioner acknowledges that it is combining features from Kim's Figs. 17A-22B embodiment with features from the Figures 5A-14B embodiment. Pet. 29. But Petitioner fails to provide any reason why a POSITA would have been motivated to replace the "gate electrodes" in the memory stack of the Figs. 17A-22B embodiment with "insulating layers," and "insulating layers" with "gate electrodes." Petitioner identifies no flaw or problem this modification would address. Nor does Petitioner identify any benefit that would result from the

proposed modification. Petitioner provides only conclusory reasons that purport to support its modification of Figs. 17A-22B. All fail.

First, Petitioner asserts that "[a] POSITA would have understood that descriptions of one of Kim's embodiments apply to other embodiments except where the embodiments differ." Pet. 29. As support, Petitioner cites only its expert, Dr. Banerjee. But Dr. Banerjee only parrots the language of the Petition. Ex.1003 ¶¶ 70-71. The Board should not give Dr. Banerjee's declaration any weight. *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15-16 (Aug. 24, 2022) (precedential) (expert testimony that is "conclusory and unsupported, [and] adds little to the conclusory assertion for which it is offered to support" is "entitled to little weight") (citations omitted).

Regardless, Petitioner's conclusory assertion that Kim's disparate embodiments can be combined "except where the embodiments differ" falls well short of articulating a proper motivation to combine as required. *In re Nuvasive, Inc.*, 842 F.3d 1376, 1381-85 (Fed. Cir. 2016) (holding that a proper motivation to combine includes "identif[ying] a reason why a PHOSITA would have combined the prior art references—i.e., 'minimiz[ing] waste' and 'allow[ing] for a greater degree of movement'—that had a foundation in the prior art") (citation omitted); *Personal Web. Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993-94 (Fed. Cir. 2017) (rejecting reasoning "that a skilled artisan, once presented with the two references,

would have understood that they could be combined" because "that is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention") (citations omitted). Petitioner provides no reason ***why*** a POSITA would have been motivated to combine the Figs. 17A-22B embodiment with the Figs. 5A-14B embodiment to reverse the order of gate electrodes and insulating layers. Pet. 29. The Petition identifies no problems solved and no benefits achieved by this modification.

Second, Petitioner asserts that "Kim discloses closely related embodiments." Pet. at 29. Courts have found that generic assertions of relatedness (like Petitioner's) are insufficient to establish a motivation to combine as required. *Securus Techs., Inc. v. Glob. Tel*Link Corp.*, 701 F. App'x 971, 977 (Fed. Cir. 2017) ("a broad characterization of [prior art references] as both falling within the same alleged field . . . without more, is not enough for [Petitioner] to meet its burden of presenting a sufficient rationale to support an obviousness conclusion"); *see also Microsoft Corp. v. Enfish, LLC*, 662 F. App'x. 981, 990 (Fed. Cir. 2016) ("[The] Board correctly concluded that [the petitioner] did not articulate a sufficient motivation to combine. With respect to [certain challenged claims], [the petitioner] gave no reason for the motivation of a person of ordinary skill to combine [the two references] except that the references were directed to the same art or same techniques . . . ."). If anything, Petitioner's acknowledgment that the

embodiments are reportedly "closely related" recognizes that the embodiments are disparate. As such, Petitioner's conclusory allegation that Kim's embodiments are "closely related" fails to establish a proper motivation to combine.

Regardless, Micron's reasons for alleging the embodiments are "closely related" do not provide a motivation to combine the disparate embodiments. For example, Petitioner alleges that "many of the same elements [are] denoted by the same reference numerals." Pet. 29. Petitioner cites no authority holding that denoting elements with the "same reference numerals" is sufficient to establish a motivation to combine. None exist. To the contrary, Kim makes clear that the use of the same reference numbers and "previously described" element descriptions is to allow "for ***concise description***"—not because Kim contemplates mixing and matching features from disparate embodiments. Kim [0184]. Petitioner also cites paragraph 184 of Kim to allege that the Figs. 5A-14B and 17A-22B embodiments are "closely related." Pet. 29. But paragraph 184 of Kim simply acknowledges that, in describing the Figs. 17A to 22B embodiment, "overlapping description[s] of elements previously described with reference to Figs. 5A through 14A and Figs. 5B through 14B may be omitted." Kim [0184]. It does not provide a motivation to combine the two disparate embodiments, let alone in the particular manner that Petitioner proposes in its manipulated figures described above.

Third, Petitioner asserts that "the descriptions of Figures 17A-22B extensively reference Figures 9A-14B." Pet. 29. Again, Petitioner fails to establish how or why this would motivate a POSITA to make the proposed modifications to the Figs. 17A-22B embodiment. In the cited paragraphs, Kim only states that certain features of the Figs. 17-22B embodiment may be "described with reference to" Figures 9A to 14B—for example, the steps of forming "the interlayer dielectric 130 and the polishing stop layer" (Kim [0188]); various "planarization" processes (*id.* [0190], [0193]); forming "trenches" and "replacing the sacrificial layers" (*id.* [0198]) and others. The cited paragraphs do not say anything about combining the disclosures about the insulating layers and gate electrodes of the Figs. 17A-22B embodiment with disclosures about those structures from the Figs. 5A-14B embodiment—let alone disclose that the insulating layers and gate electrodes of the Fig. 17A-22B embodiment may swapped.[6]

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[6] Petitioner also asserts that "descriptions of Figures 26-27 refer to the two embodiments in Figures 17A-22A and 8A-11A." Pet. 29. But Petitioner does not propose combining the Figs. 17A-22A embodiment with anything from Figures 26-27.

Finally, Petitioner cites the Chen reference in passing and asserts that "POSITA would have known that either order was a common alternative." Pet. 33. But just because Chen discloses semiconductors with a "dielectric on top" and a "conductor on top" does not mean a POSITA "would have been motivated to make the combinations or modifications" to Kim's Figs. 17A-22B embodiment. *See Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) ("[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.") (citations omitted); *Personal Web Techs.*, 848 F.3d at 993-94 (conclusion that a combination "would have allowed for" a claimed limitation "is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention") (citations omitted).

In short, Petitioner has failed to establish that a POSITA would have been motivated to combine disparate embodiments of Kim as Petitioner proposes to arrive at the claimed invention.

2. Petitioner Has Failed To Establish A POSITA Would Have Had A Reasonable Expectation Of Success With Modifying Kim To Arrive At The Claimed "each step comprises a gate stack disposed over a dielectric layer"

Even if Petitioner has established a motivation to combine (it has not), Petitioner has failed to establish that a POSITA would have had a reasonable

expectation of success in implementing the proposed combination. The Federal Circuit has "emphasize[d]" the "clear distinction in our case law between a patent challenger's burden to prove that a skilled artisan would have been motivated to combine prior art references and the additional requirement that the patent challenger also prove that the skilled artisan would have had a reasonable expectation of successfully achieving the claimed invention from the combination." *Eli Lilly and Co. v. Teva Pharms. Int'l GmbH*, 8 F.4th 1331, 1344 (Fed. Cir. 2021) (citations omitted). "A finding by the Board that a patent challenger has demonstrated a motivation to combine references does not necessarily imply that the challenger has also met its burden of showing a reasonable expectation of success in achieving a claimed method of treatment." *Id.*

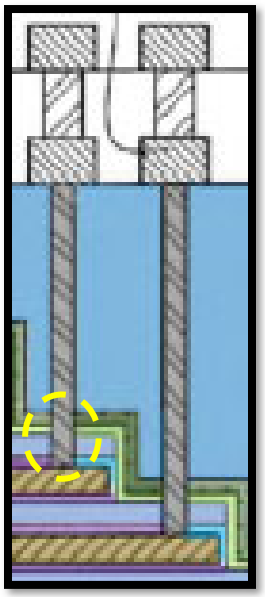
Here, Petitioner asserts that "[a] POSITA would have known that" changing the order of Kim's insulating layer and gate electrode "was routine, highly predictable, and would have had a reasonable expectation of success for implementing a gate-stack-on-top embodiment." Pet. 33. As support, Petitioner cites Dr. Banerjee, who parrots the language of the Petition and adds that "common deposition techniques such as CVD or ALD" could be used with the proposed modification. Ex.1003 ¶ 81.

Petitioner misses the point. Merely because "common deposition techniques" can be used with the proposed modification does not provide a "clear,

evidence-supported account" of "how the combination" would work as required. *Personal Web Techs.*, 848 F.3d at 994. This is especially true where, as here, the proposed combination involves fundamentally changing the memory stack of Kim by replacing insulating materials with conductive gate electrodes and conductive gate electrodes with insulating materials. *See supra* § III.B.1.

While Petitioner attempts to trivialize its wholesale modification to Kim, a POSITA would understand that replacing a functional, gate stack with insulating material and vice versa would require extensive modifications to the manufacturing process and device—all of which Petitioner ignores. Campbell ¶¶41-42. As just one example (and as Petitioner recognized in its modified figure), for Petitioner's "Gate-Stack-on-Top" modification to work, the process for forming word line contacts (shown in gray below) would also need to be modified to use an entirely different etching process because the contact opening in the modified device penetrates through different materials with different depths. Campbell ¶¶41-42. While Petitioner draws this necessary modification in its manipulated figure, Petitioner provides no explanation of how or why a POSITA could actually etch such vertical contacts without undue experimentation and with a reasonable expectation of success. Pet. 28 (Kim Fig. 22A), 40 (Kim "Gate-Stack-on-Top" Fig. 22A).

Original



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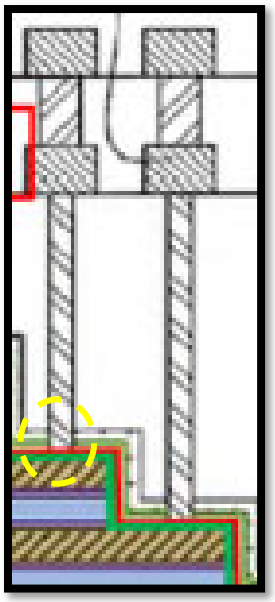


Changing how a vertical contact penetrates the layers of a semiconductor device is not a trivial change, but requires fundamental changes to the manufacturing process and device structure. Campbell ¶¶41-42. Petitioner does not address this (and other) modifications that would be required at all. *Id.*

Petitioner purports to quote *Retractable Technologies, Inc. v. Becton, Dickinson & Co.* to suggest that it need only show that using conductors over dielectrics represents a "known technique" or "a suitable option." Pet. 33-34 (quoting *Retractable Techs., Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296, 1303 (Fed. Cir. 2011)). But the quoted language does not appear in *Retractable Techs.* To the contrary, in *Retractable Techs.*, the Federal Circuit affirmed a jury's finding of nonobviousness there because the defendant failed to establish that a POSITA would have been motivated to replace a "'locking' mechanism" with a "'lodging'

mechanism," even though both were known in the art. *Id.* Thus, *Retractable Techs.* supports Patent Owner, not Petitioner.

In short, Petitioner has failed to identify any motivation to combine disparate embodiments of Kim or that a POSITA would have had a reasonable expectation of success in doing so. The Petition should be denied.

C. Kim in View of a POSITA's Knowledge Does Not Render Obvious the Dependent Claims (Claims 2-9, 11-12, 14-16, 18-19)

Because they depend from the independent claims, Petitioner fails to establish claims 2-9, 11-12, 14-16, and 18-19 are obvious for the reasons described above. *See In re Fine*, 837 F.2d 1071, 1076 (Fed. Cir. 1988) ("Dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious.") (citations omitted); *Tris Pharma, Inc. v. Teva Pharms. USA, Inc.*, No. 05-cv-00212, 2022 WL 4082190, at *18 (D.N.J. Sept. 6, 2022) ("Because I have found that claim 1 of the '545 patent nonobvious and claim 24 of the '545 patent is dependent on claim 1, claim 24 must therefore also be nonobvious and valid.") (citation omitted).

IV. Ground 2: Petitioner Fails to Meet Its Burden to Establish Kim in View of Fang Renders Obvious Claims 10 and 17

Kim in view of a POSITA's knowledge does not render obvious all claim limitations of claims 1 and 13. *See supra* §III.

Petitioner does not rely on Fang to teach any claim limitation in claims 1 and 13. Pet. 62-64. Instead, Petitioner purports to rely on Fang to disclose a thickness of a etch-stop layer of 5-26.7 nm. *Id.* 63. Because they depend from the independent claims, Petitioner fails to establish claims 10 and 17 are obvious for reasons described above. *See In re Fine*, 837 F.2d at 1076; *Tris Pharma*, 2022 WL 4082190, at *18. Accordingly, Petitioner has not established a reasonable likelihood that it would prevail in its challenge of claims 10 and 17.

V. Ground 3: Petitioner Fails to Meet Its Burden to Establish Park in View of a POSITA's Knowledge Renders Obvious Claims 1-6, 8-9, 11-16, and 18-19

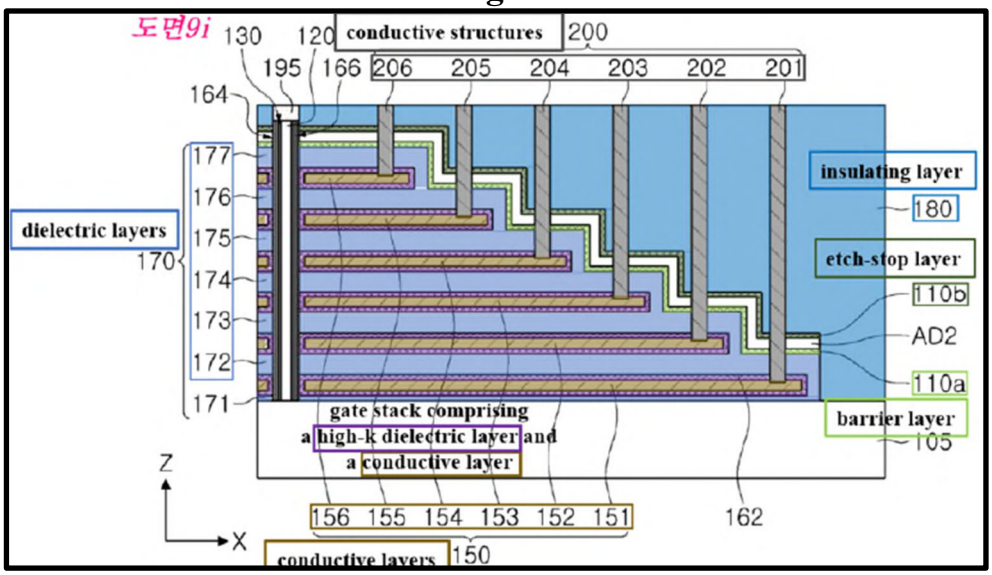
All Challenged Claims require "a plurality of steps" where "each step comprises a gate stack disposed over a dielectric layer." As discussed below, Park fails to disclose or render obvious this limitation.

A. Park Does Not Disclose "each step comprises a gate stack disposed over a dielectric layer"

According to Petitioner, "[t]his Petition relies on the embodiment shown in Figures 5 (perspective view) and 9a-9j (cross-sectional views)." Pet. 31. The Petition alleges that in the relied-upon embodiment, "Park discloses a gate stack disposed over a dielectric layer ***even though its figures show the opposite order***"—i.e., a dielectric layer disposed over a gate stack. Pet. 66-67. As Petitioner acknowledges, Fig. 9i of the embodiment Petitioner "relies on" shows that each step of the Figs. 5, 9a-9j staircase comprises a gate electrode layer 151-

156 (tan) ***below*** an insulating layer 171-177 (purple)—not a "gate stack disclosed ***over*** a dielectric layer" as required by the claims. Campbell ¶44.

Original



Pet. 30 (Park Fig. 9i); Campbell ¶44.

Petitioner cites only paragraph 102 of Park, with no further explanation, to assert that Figure 9 discloses "a gate stack is disposed over a dielectric layer at each step." Pet. 30-31. But that paragraph only states that "a portion of the top surface of each insulating layer (170) may be exposed by the plurality of pad regions (P1-P6), and, unlike what is shown in FIG. 9a, a portion of the top surface of each sacrificial layer (140) may be exposed in a plurality of pad regions (P1-P6)." Park [0102]. Petitioner fails to explain how a POSITA would understand that disclosure to necessarily mean that the gate stack is disposed over the insulating layer, in contrast to what Fig. 9i actually shows. Campbell ¶45. At most, paragraph 102 recognizes that both insulating layers 170 and sacrificial

layers 140 may be "exposed" in the pad regions P1-P6 (as shown in Fig. 9b), rather than just "insulating layer" 170 as shown. *Id.* Fig. 9a, 9b. Petitioner provides no explanation for its assertion.

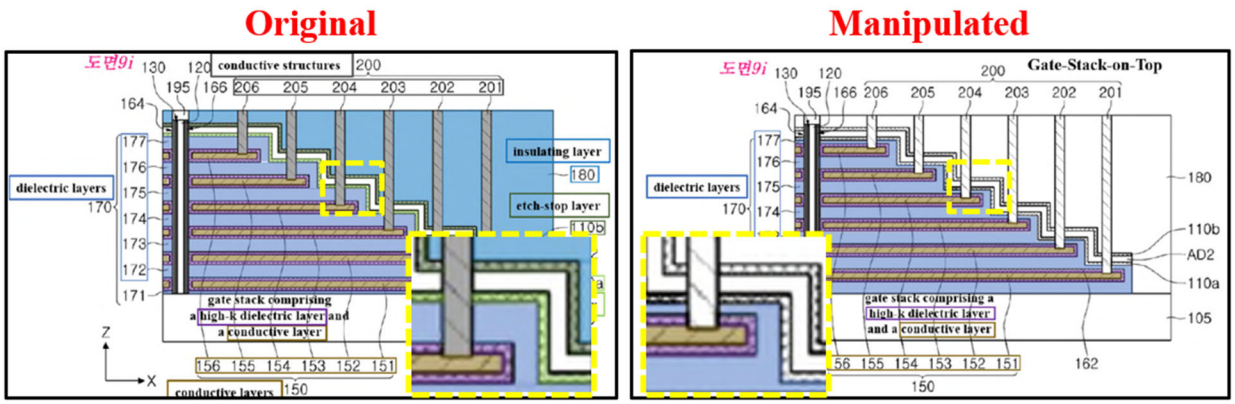
In short, Park does not disclose that the relied-upon Figs. 5/9 embodiment includes a "gate stack disposed over a dielectric layer."

B. Park in View of a POSITA's Knowledge Does Not Render Obvious "each step comprises a gate stack disposed over a dielectric layer"

Petitioner asserts that Park "at least renders the [each step comprises a gate stack disposed over a dielectric layer] limitation obvious" in the Figs. 5, 9a-9j embodiment that the Petition "relies on." Pet. 31, 66-68. Petitioner argues that although "[t]his Petition relies on the embodiment shown in Figures 5 (perspective view) and 9a-9j (cross-sectional views)," Park discloses "other embodiments, *e.g.*, one illustrated in Figures 4 (perspective view) and 8a-8m (cross-sectional views)." Pet. at 31. Thus, as Petitioner recognizes, Park discloses separate embodiments from the one relied on in the Petition. Petitioner then concludes that "[a] POSITA would have understood that descriptions of one of Park's embodiments apply to other embodiments except where the embodiments differ" (*id.*) to support a wholesale recreation of Figure 9i of Park.

In the manipulated version of Figure 9i Petitioner relies on, Petitioner switches the gate electrodes so that they appear "disposed over" the insulating

layers as claimed. Petitioner fails to establish that a POSITA would have been motivated to combine Park's disparate embodiments to arrive at Petitioner's manipulated figure, or that a POSITA would have had a reasonable expectation of success in doing so.



Pet. 69 (Park "Gate-Stack-on-Top Fig. 9i"); Campbell ¶¶46-47.

1. Petitioner Has Failed To Establish A POSITA Would Have Been Motivated To Combine Disparate Embodiments Of Park To Arrive At The Claimed "each step comprises a gate stack disposed over a dielectric layer"

Petitioner fails to establish that a POSITA would have been motivated to combine Park's Figs. 5, 9a-9j embodiment with Park's Figs. 4, 8a-9m embodiment as Petitioner proposes. Pet. 31.

As discussed, this Board has consistently held that Petitioners must establish a motivation to combine "disparate embodiments" within a single prior art reference. *See supra* §III.B. Petitioner acknowledges that it is combining features from Park's Figs. 5/9 embodiment with features from Park's Figs. 4/8

embodiment. Pet. 30-31. But Petitioner fails to provide any reason why a POSITA would have been motivated to move the Figs. 5/9 gate stacks as proposed to purportedly be "disposed over" the dielectric layers. Petitioner identifies no flaw or problem this modification would address. Nor does Petitioner identify any benefit that would result from the proposed modification. Petitioner provides only conclusory reasons that purport to support its modification of the Figs. 5/9 embodiment. All fail.

First, Petitioner asserts that "would have understood that descriptions of one of Park's embodiments apply to other embodiments except where the embodiments differ." Pet. 31. As support, Petitioner cites only its expert, Dr. Banerjee. But, as he did with the Kim ground, Dr. Banerjee again only parrots the language of the Petition. Ex.1003 ¶¶ 76-77. The Board should not give Dr. Banerjee's declaration any weight. *Xerox Corp.*, IPR2022-00624, Paper 9 at 15-16. Further, when Park contemplated disclosures that apply to multiple embodiments, it said so explicitly. *See, e.g.*, Park [0104] ("Referring to FIG. 9e next, a channel region (130) may be formed. The method of forming a channel region (130) may be ***the same as described with reference to FIG. 8h above***."). Petitioner does not cite anything in Park that discloses reversing the gate electrodes and insulating layers of the Figs. 5/9 embodiment as Petitioner suggests. Nor does Petitioner identify any reason

why a POSITA would be motivated to do so, as it was required to do. *E.g.*, *Nuvasive*, 842 F.3d at 1381-85.

Second, Petitioner asserts that "Park discloses closely related embodiments and teaches that 'various embodiments may be combined,' and 'elements indicated by the same symbols in the drawings are the same elements.'" Pet. 31. Petitioner cites no authority that holds that such generic statements are sufficient to establish a motivation to combine different embodiments. They are not. *See Securus Techs.*, 701 F. App'x at 977; *Enfish*, 662 F. App'x. at 990; *BlephEx, LLC*, 24 F.4th at 1401 (holding generic statement referring to "other embodiments" insufficient to establish motivation to combine). And, as discussed, Petitioner fails to provide any reason ***why*** a POSITA would have moved the gate electrodes and insulating layers of Park's Fig. 5/9 embodiment as Petitioner proposes. *Belden Inc.*, 805 F.3d at 1073 ("[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.") (citations omitted). If anything, Petitioner's acknowledgment that the embodiments are reportedly "closely related" recognizes that the embodiments are disparate. As such, Petitioner's conclusory assertion that the embodiments are "closely related" fails for the same reasons discussed above with respect to Kim. *See supra* § III.B.1.

Third, Petitioner asserts that "most aspects of the Figure 5 embodiment 'are the same as' the Figure 4 embodiment." Pet. 31. As support, Petitioner cites paragraph 49 of Park. But paragraph 49 does not say that "most aspects" of the two embodiments are the same. To the contrary, paragraph 49 only states that certain "transistors" and other specific components Fig. 5 embodiment "are the same as Fig. 4." Park [0049].

Notably, Park notes that the "steps" of the two embodiments—which comprise the gate stack and insulating layers at issue—are different. As Park notes, the Figs. 5/9 embodiment includes, for example, "a plurality of etch-stop layers" and "insulating layer (AD2)" on each step that the Figs. 4/8 embodiment does not include. *Id.* Petitioner ignores these differences and does not explain why a POSITA would be motivated to combine features from the steps of the Figs. 4/8 embodiment with the Figs. 5/9 embodiment despite such differences. Campbell ¶49.

In short, Petitioner has not identified any reason a POSITA would have been motivated to combine Park's Figs. 5/9 embodiment with its Figs. 4/8 embodiment so that the gate stacks are over the insulating layer, rather than the other way around as disclosed.

2. Petitioner Has Failed To Establish A POSITA Would Have Had A Reasonable Expectation Of Success Of Modifying Kim To Arrive At The Claimed "each step comprises a gate stack disposed over a dielectric layer"

Even if Petitioner has established a motivation to combine (it has not), Petitioner has failed to establish a reasonable expectation of success as required. *See supra*; *Eli Lilly and Co. v. Teva Pharms. Int'l GmbH*, 8 F.4th at 1344. Petitioner makes no attempt to establish that a POSITA would have had a reasonable expectation of success in implementing its proposed modification of moving the gate electrodes of Park's Fig. 5/9 embodiment to be over the dielectric layers.

To the contrary, a POSITA would understand that moving a functional, gate stack to be ***over*** a dielectric layer, when Park teaches the opposite, would require extensive modifications to the manufacturing process and device—all of which Petitioner ignores. For example, the word line contacts would need to also be modified so that they do not penetrate the insulating layer as Park actually discloses. Petitioner provides no explanation of how or why a POSITA could actually do so without undue experimentation and with a reasonable expectation of success. Pet. 30 (Park Fig. 9i), 69 (Park "Gate-Stack-on-Top Fig. 9i"). Changing how a vertical contact penetrates the layers of a semiconductor device is not a trivial change, but requires fundamental changes to the manufacturing process and

device structure. Campbell ¶¶51-52. Petitioner does not address this additional modification at all. *Id.*

In short, Petitioner has failed to identify any motivation to combine disparate embodiments of Kim or that a POSITA would have had a reasonable expectation of success in doing so. The Petition should be denied.

C. Park in View of a POSITA's Knowledge Does Not Render Obvious the Dependent Claims (Claims 2-6, 8-9, 11-12, 14-16, 18-19)

Because they depend from independent claim 1 or 13, Micron fails to establish claims 2-6, 8-9, 11-12, 14-16, and 18-19 are obvious for the reasons described for the independent claims. *See In re Fine*, 837 F.2d at 1076; *Tris Pharma*, 2022 WL 4082190, at *18.

VI. Ground 4: Petitioner Fails to Meet Its Burden to Establish Park in View of Fang Does Not Render Obvious Claims 7, 10, 15, and 17

Park in view of a POSITA's knowledge does not render obvious all claim limitations of claims 1 and 13. *See* §V.

Petitioner does not rely on Fang to teach any claim limitation in claims 1 and 13. Pet. 91-103. Instead, Petitioner purports to rely on Fang to disclose the top surfaces of the plurality of conductive structures, the insulating layer, and some of etch-stop layer are coplanar, a thickness of a etch-stop layer of 5-26.7 nm, and thickness of an etch-stop layer being the same on the side and top surfaces of each step. *Id.* 94, 97-100.

Because they depend from independent claim 1 or 13, Petitioner fails to establish claims 7, 10, 15, and 17 are obvious for reasons described for the independent claims described above. *See In re Fine*, 837 F.2d at 1076; *Tris Pharma*, 2022 WL 4082190, at *18. Accordingly, Petitioner has not established a reasonable likelihood that it would prevail in its challenge of claims 7, 10, 15, and 17.

VII. The Board should exercise its discretion and deny institution under 35 U.S.C. § 314.

Institution of an IPR is always discretionary. 35 U.S.C. § 314(a). Here, the Board should exercise its discretion to deny institution because the Petition will not serve as an effective and efficient alternative to litigation. Rather, the overall balance of the *Fintiv* factors shows that "efficiency, fairness, and the merits support the exercise of authority to deny institution." *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (Mar. 20, 2020) (precedential).

A. Factor 1 favors denial if the district court denies Petitioner's motion to stay and lifts the temporary stay before institution.

The Court has temporarily stayed the Parallel Proceeding[7] while it considers Petitioner's motion for a stay pending IPRs. Ex. 2001; Ex. 2003. The Parallel

[7] *Yangtze Memory Technologies Company, Ltd. V. Micron Technology, Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.).

Proceeding involves 70 asserted claims from 19 patents. Ex. 2002 at 006. Of those, the Board has only instituted IPRs against 23 claims from 8 patents. Ex. 2002 at 006. And 11 claims from one patent have had IPR institution denied across the board. *Id.*; *see, e.g.*, *Entangled Media, LLC v. Dropbox Inc.,* 732 F. Supp. 3d 1120, 1124 (N.D. Cal. 2024) (characterizing arguments about simplification as "premature" "[b]ecause the PTO has not yet instituted proceedings," and denying motion to stay); *Skillz Platform Inc. v. Aviagames Inc.*, No. 21-cv-02436-BLF, 2022 WL 1189882, at *3–4, *5 (N.D. Cal. Apr. 21, 2022) (denying motion to stay, stating that any simplification from IPRs "is purely *speculative at this stage*," and "*the cost of non-institution would be delay without benefit*").

It is not clear how long the temporary stay will remain in effect.[8] However, if the district court denies Petitioner's stay motion and lifts the temporary stay, Factor 1 would favor denial. *Inergy Tech., Inc. v. Force MOS Tech. Co.*, IPR2024-00094, Paper 9 at 32 (May 21, 2024) (denial of stay motion favors discretionary denial of IPR petition); *see also Fintiv*, Paper 11 at 7-8 (similar).

For these reasons, this factor favors discretionary denial of institution.

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[8] YMTC reserves its rights to address changes in the district court proceeding as they relate to discretionary denial in future briefs.

B. Factor 2 is neutral because the trial date is three days after Final Written Decision.

Trial is set to begin in the Parallel Proceeding on June 15, 2026.[9] Ex. 1018 at 002. That is three days after the statutory deadline for a Final Written Decision in this case (June 12, 2026). And it is *well before* the expected Final Written Decisions that would issue in *eight* other proceedings filed by Micron against patents at issue in the Parallel Proceeding. *See* IPR2025-00190, -00191, -00228, -00229, -00244, -00245, -00294, and PGR2025-00021. This factor therefore favors denial of institution, or is at worst neutral. *Fintiv,* IPR2020-00019, Paper 11 at 9 ("If the court's trial date is at or around the same time as the projected statutory deadline, … the decision whether to institute will likely implicate other factors …."); *Catalyst Orthoscience Inc. v. Shoulder Innovations, Inc.*, PGR2024-00042, Paper 17 at 12-14 (Dec. 19, 2024) (finding Factor 2 neutral where scheduled trial was "just weeks" after the scheduled conclusion of the PGR). A Final Written Decision here would issue after expert discovery, after dispositive motions, and after the pretrial conference. Ex. 1018 at 002.

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[9] Petitioner's assertion of a 48.9-month median time to trial (Pet. 13 (citing Ex. 1019) misleadingly includes non-jury trials, which have a significantly longer time-to-trial. *See* Ex. 2004 at 003. The corresponding number for jury trials is 32.8 months. Ex. 2004 at 003.

C. Factor 3 favors denial because substantial effort will have been expended by the deadline for institution.

The parties have expended, and continue to expend, substantial resources into the Parallel Proceeding. In that case, the parties have collectively propounded, responded to, and supplemented responses to 38 interrogatories and 117 requests for production. The parties have already produced over 113,000 pages of documents and are continuing to produce thousands more pages of documents. Ex. 2002 at 012. They have also engaged in extensive source code discovery, which has involved 14 days of YMTC expert and/or attorney review of code in this District and, more recently, three weeks and counting of code review at Micron's headquarters in Boise, ID. Ex. 2002 at 012. And upon order of the Court, YMTC has narrowed its claims of infringement to 70 asserted claims, which has required extensive analysis of infringement, validity, and damages issues. Ex.2002 at 012.

The parties have also devoted, and continue to devote, substantial effort to claim construction, including exchanging claim terms and proposed constructions and filing a Joint Claim Construction and Prehearing Statement. The parties have also exchanged expert declarations in connection with claim construction and conducted two claim construction expert depositions.

Petitioner's assertion that the parties and district court have invested "very little" in the Parallel Proceeding is both wrong and, at the time of this filing and the institution decision, outdated. Pet. 13. Petitioner does not even address the

substantial effort invested in the Parallel Proceeding in the more than 7 months between filing and the Board's institution decision. Because the parties and the Court will expend significant effort in the parallel litigation *before institution*, this factor favors discretionary denial of institution. *See, e.g.*, *Comcast Cable Commc'ns, LLC v. Touchstream Techs., Inc.,* IPR2024-00323, Paper 13 at 9-10, 2024 WL 3530021, at *4 ("Factor 3 favor[ed] denial" where "substantial work on claim construction [had] happened," and "the related district court litigation ha[d] progressed in other aspects as well," including with respect to contentions); *10x Genomics, Inc. v. President & Fellows of Harvard Coll.*, IPR2023-01299, Paper 15 at 18, 2024 WL 993828, at *8 (similar, noting that the parties had exchanged contentions, "completed claim construction briefing," and that the "district court ha[d] also considered two motions to dismiss and presided over several discovery disputes"); *Boe Tech. Grp. Co. v. Element Cap. Com. Co. Pte. Ltd*, IPR2023-00808, Paper 9 at 23, 2023 WL 7715885, at *8 (finding "the parties and the District Court ha[d] invested substantial resources in th[e] litigation" because, among other things, "[s]ignificant discovery ha[d] been completed, including the exchange of infringement and invalidity contentions, document requests and interrogatories, and proposed claim terms for construction").

D. Factor 4 favors denial because there is significant overlap between the issues raised in the Petition and the district court proceeding.

Petitioner Micron has served invalidity contentions identifying the same art from its Petition, and explicitly incorporating its IPR petition by reference. Petitioner has also not filed a *Sotera*-type stipulation in this proceeding. *Cf. Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (Dec. 1, 2020) (precedential). Although Petitioner stipulates in its Petition that "[s]hould the Board institute, it will not advance in District Court on any ground asserted in this Petition," no such stipulation has been made in the district court. Pet. 14. Such a narrow stipulation runs the risk of significant overlap both in consideration of the same evidence and arguments framed as "different grounds" than the Petition. Because such a narrow stipulation risks having the district court address substantially the same evidence and arguments that the Board will have to address should it institute an IPR, and on a similar timeline, an IPR of the '711 patent would be an inefficient use of the Board's resources and would risk conflicting decisions. *See 10x Genomics*, IPR2023-01299, Paper 15 at 20, 2024 WL 993828, at *9 ("[W]e agree with Patent Owner that the overlapping art and arguments presented in the parallel proceeding weigh in favor of exercising our discretion to deny institution.") (footnote omitted); *see also Comcast*, IPR2024-00323, Paper 13 at 12, 2024 WL 3530021, at *5 (questioning whether a narrower stipulation "not to pursue in the District Court any ground that utilizes the same combination of prior

art references relied upon in the instituted petition" adequately addressed "concerns of inefficiency and the possibility of conflicting decisions").

E. Factor 5 favors denial because Micron is the defendant in the district court proceeding.

Petitioner is the defendant and counterclaimant in the parallel district court case and, as such, will have a full and fair opportunity to litigate its (overlapping) invalidity contentions in that forum. Thus, this factor favors discretionary denial. *Comcast*, IPR2024-00323, Paper 13 at 13, 2024 WL 3530021, at *5 ("Petitioner is the defendant in the related district court case…. We find that this factor favors denial.") (citations omitted); *Boe Tech.*, IPR2023-00808, Paper 9 at 24-27, 2023 WL 7715885, at *9.

F. Factor 6: The limited resources of the Board favors denial.

"The sixth *Fintiv* factor takes into account other circumstances that may bear on the decision to exercise discretion to deny, such as the merits of the patentability challenges." *Comcast*, IPR2024-00323, Paper 13 at 13, 2024 WL 3530021, at *5 (citation omitted). For the reasons explained in Sections III-VI, the Petition fails on the merits for numerous reasons, including because the Petition fails motivate its proposed modifications to Kim and Park, and thus does not present a "particularly strong" showing that can tip the scales in favor of institution. *Fintiv*, IPR2020-00019, Paper 11 at 14-15 ("[I]f the merits of a ground raised in the petition seem particularly strong on the preliminary record, this fact

has favored institution…. [I]f the merits of the grounds raised in the petition are a closer call, then that fact has favored denying institution when other factors favoring denial are present.") (citations omitted); *see also USPTO Rescinds Memorandum Addressing Discretionary Denial Procedures* (Feb. 28, 2025), available at https://www.uspto.gov/about-us/news-updates/uspto-rescinds-memorandum-addressing-discretionary-denial-procedures (compelling merits analysis no longer applicable).

As five of the six *Fintiv* factors favor discretionary denial of institution, and the remaining factor is, at worst, neutral, Patent Owner respectfully requests that the Board exercise its discretion to deny institution.

VIII. Conclusion

For the reasons set forth above, the Board should deny the Petition for *Inter Partes* Review.

Respectfully submitted,

Dated: March 12, 2025

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CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Patent Owner's Preliminary Response complies with the word count limitation of 37 C.F.R. § 42.24(b)(1) because the Patent Owner's Preliminary Response contains 7,701 words using Microsoft Word's counting feature, excluding the cover page, signature block, and the parts of the Patent Owner's Preliminary Response exempted by 37 C.F.R. § 42.24(b)(1).

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 12th day of March, 2025, a true and correct copy of the foregoing **Patent Owner's Preliminary Response and all Exhibits** were served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

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