

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: August 26, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MICRON TECHNOLOGY, INC.,  
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,  
Patent Owner.

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IPR2025-00117  
Patent 10,672,711

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**PATENT OWNER'S RESPONSE**

**TABLE OF CONTENTS**

|                                                                                                                                                                            | <b><u>Page</u></b> |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| I. Introduction.....                                                                                                                                                       | 1                  |
| II. Background.....                                                                                                                                                        | 2                  |
| A. The '711 Patent (Ex.1001) .....                                                                                                                                         | 2                  |
| B. Person of Ordinary Skill in the Art .....                                                                                                                               | 7                  |
| C. Claim Construction .....                                                                                                                                                | 8                  |
| III. Ground I: Petitioner Failed to Demonstrate Kim in View of a<br>POSITA's Knowledge Renders Obvious Claims 1-9, 11-16, and 18-<br>19. ....                              | 15                 |
| A. Kim does not disclose "each step compris[ing] a gate stack<br>disposed over a dielectric layer." .....                                                                  | 15                 |
| 1. Petitioner improperly relies on multiple embodiments<br>from Kim to justify manipulating the figures Kim<br>discloses. ....                                             | 17                 |
| 2. Petitioner improperly relies on additional prior art<br>references and a POSITA's knowledge to justify<br>inverting the layers.....                                     | 21                 |
| 3. Petitioner's unjustified manipulation of the figures<br>misled the Board. ....                                                                                          | 27                 |
| B. Kim does not render claims 14 or 15 obvious because Kim does<br>not disclose "the etch-stop layer is formed on a side surface and<br>a top surface of each step." ..... | 28                 |
| IV. Ground II: Petitioner Failed to Demonstrate Kim in View of Fang<br>Renders Obvious Claims 10 and 17. ....                                                              | 30                 |
| A. Fang is directed toward carbon-doped silicon nitride etch-stop<br>material, which Kim does not use. ....                                                                | 31                 |

|     |                                                                                                                                                                    |    |
|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| B.  | Structural differences between Fang and Kim counsel a POSITA against applying Fang's etch-stop layer thicknesses to Kim. ....                                      | 38 |
| C.  | Petitioner fails to establish a reasonable expectation of success in combining Fang's etch-stop layer thicknesses to Kim. ....                                     | 41 |
| V.  | Ground III: Petitioner Failed to Demonstrate Park in View of a POSITA's Knowledge Renders Obvious Claims 1-6, 8-9, 11-16, and 18-19. ....                          | 43 |
| A.  | Park does not disclose "each step compris[ing] a gate stack disposed over a dielectric layer." ....                                                                | 43 |
| 1.  | Petitioner improperly relies on multiple embodiments from Park to justify manipulating the figures Park discloses. ....                                            | 44 |
| 2.  | Petitioner improperly relies on a POSITA's knowledge to justify inverting the layers. ....                                                                         | 47 |
| B.  | Park does not render claims 14 or 15 obvious because Park does not disclose "the etch-stop layer is formed on a side surface and a top surface of each step." .... | 48 |
| C.  | Park does not render claim 15 obvious because Petitioner improperly relies on a POSITA's background knowledge to satisfy a missing limitation. ....                | 52 |
| VI. | Ground IV: Petitioner Failed to Demonstrate Park in View of Fang Renders Obvious Claims 7, 10, 15, and 17. ....                                                    | 55 |
| A.  | Petitioner fails to establish adequate motivation to combine Park in view of Fang. ....                                                                            | 55 |
| 1.  | Petitioner fails to establish a motivation to combine the Park and Fang references to render dependent claim 7 obvious. ....                                       | 56 |
| 2.  | Petitioner fails to establish a motivation to combine the Park and Fang references to render dependent claims 10 and 17 obvious. ....                              | 65 |

|      |                                                                                                                                                                                    |    |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| 3.   | Petitioner fails to establish a motivation to combine the Park and Fang references, or a reasonable expectation of success in doing so, to render dependent claim 15 obvious. .... | 69 |
| VII. | Conclusion .....                                                                                                                                                                   | 72 |

**TABLE OF AUTHORITIES****Page(s)****CASES**

|                                                                                                                                                                                                        |        |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|
| <i>Abbott Diabetes Care Inc. v. Dexcom, Inc.</i> ,<br>No. IPR2022-00913, 2023 WL 7225556 (P.T.A.B. Nov. 2, 2023).....                                                                                  | 23     |
| <i>Adidas AG v. Nike, Inc.</i> ,<br>963 F.3d 1355 (Fed. Cir. 2020) .....                                                                                                                               | 30, 56 |
| <i>Bicon, Inc. v. Straumann Co.</i> ,<br>441 F.3d 945 (Fed. Cir. 2006) .....                                                                                                                           | 14     |
| <i>BlephEx, LLC v. Myco Indus., Inc.</i> ,<br>24 F.4th 1391 (Fed. Cir. 2022) .....                                                                                                                     | 19     |
| <i>Bradium Techs. LLC v. Iancu</i> ,<br>923 F.3d 1032 (Fed. Cir. 2019) .....                                                                                                                           | 34     |
| <i>Chamberlain Grp., Inc. v. Techtronic Indus. Co.</i> ,<br>935 F.3d 1341 (Fed. Cir. 2019) .....                                                                                                       | 17     |
| <i>Eli Lilly &amp; Co. v. Teva Pharms. Int'l GmbH</i> ,<br>8 F.4th 1331 (Fed. Cir. 2021) .....                                                                                                         | 20     |
| <i>FullView, Inc. v. Polycom, Inc.</i> ,<br>No. 2023-1201, 2024 WL 1843686 (Fed. Cir. Apr. 29, 2024).....                                                                                              | 23     |
| <i>In re Fulton</i> ,<br>391 F.3d 1195 (Fed. Cir. 2004) .....                                                                                                                                          | 34     |
| <i>InTouch Techs., Inc. v. VGO Commc'ns, Inc.</i> ,<br>751 F.3d 1327 (Fed. Cir. 2014) .....                                                                                                            | 18     |
| <i>Janssen Pharms., Inc. v. Mylan Laboratories Ltd.</i> ,<br>No. 2:20-cv-13103, 2023 WL 3605733 (D.N.J. May 23, 2023), <i>aff'd</i> ,<br>No. 2023-2042, 2025 WL 946390 (Fed. Cir. Mar. 28, 2025) ..... | 23     |
| <i>Koninklijke Philips N.V. v. Google LLC</i> ,<br>948 F.3d 1330 (Fed. Cir. 2020) .....                                                                                                                | 22     |

|                                                                                                                                  |        |
|----------------------------------------------------------------------------------------------------------------------------------|--------|
| <i>In re Kotzab</i> ,<br>217 F.3d 1365 (Fed. Cir. 2000) .....                                                                    | 18, 45 |
| <i>Motorola Mobility LLC v. Largan Precision Co.</i> ,<br>IPR2024-00688, Paper 7 (P.T.A.B. Oct. 28, 2024) .....                  | 22     |
| <i>NetMoneyIN, Inc. v. Verisign, Inc.</i> ,<br>545 F.3d 1359 (Fed. Cir. 2008) .....                                              | 17     |
| <i>Square One Choices Inc. v. Ditec Sols., LLC</i> ,<br>No. 2:23-CV-555-HCN-DBP, 2025 WL 918966<br>(D. Utah Mar. 21, 2025) ..... | 23     |
| <i>In re Stepan Co.</i> ,<br>868 F.3d 1342 (Fed. Cir. 2017) .....                                                                | 18, 45 |
| <i>Tesla, Inc. v. Autonomous Devices, LLC</i> ,<br>No. IPR2023-01169, 2025 WL 33587 (P.T.A.B. Jan. 6, 2025) .....                | 23     |
| <i>Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.</i> ,<br>853 F.3d 1272 (Fed. Cir. 2017) .....                                     | 14     |

## REGULATIONS

|                                |    |
|--------------------------------|----|
| 37 C.F.R. § 42.104(b)(4) ..... | 22 |
|--------------------------------|----|

## OTHER AUTHORITIES

|                                                                                                                                                                        |    |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| USPTO Memorandum, Enforcement and Non-Waiver of 37 C.F.R. §<br>42.104(b)(4) and Permissible Uses of General Knowledge in Inter<br>Partes Reviews (July 31, 2025) ..... | 22 |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|

**Exhibit List**

| <b>Ex.</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                       |
|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2001       | Micron's Motion to Stay the Case Pending Inter Partes Review and Post Grant Review Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Jan. 16, 2025), ECF No. 200                                                                                                                                               |
| 2002       | Plaintiff/Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s and Counterclaim Defendant Yangtze Memory Technologies, Inc.'s Opposition to Micron's Motion to Stay Case Pending Inter Partes Review and Post-Grant Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Feb. 3, 2025), ECF No. 221 |
| 2003       | Docket Entry Order (issuing temporary stay), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Mar. 3, 2025), ECF No. 242                                                                                                                                                                                                   |
| 2004       | U.S. District Courts—Time Intervals from Filing Date to Beginning Date for Completed Civil Trials, by District, During the 12-Month Period Ending September 30, 2024 ( <a href="https://www.uscourts.gov/sites/default/files/2025-01/jb_t3_0930.2024.pdf">https://www.uscourts.gov/sites/default/files/2025-01/jb_t3_0930.2024.pdf</a> )                                                 |
| 2005       | RESERVED                                                                                                                                                                                                                                                                                                                                                                                 |
| 2006       | Curriculum Vitae of Stephen Campbell, Ph.D.                                                                                                                                                                                                                                                                                                                                              |
| 2007       | Declaration of Dr. Campbell ("Campbell")                                                                                                                                                                                                                                                                                                                                                 |
| 2008       | Transcript of the deposition Sanjay Banerjee, Ph.D., taken August 13, 2025                                                                                                                                                                                                                                                                                                               |
| 2009       | Declaration of Dr. Campbell, Ph.D. in Support of Patent Owner's Response ("Campbell2")                                                                                                                                                                                                                                                                                                   |

## **I. Introduction**

Patent Owner Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Patent Owner”) respectfully submits this Patent Owner Response to the Petition for *inter partes* review of U.S. Patent No. 10,672,711 (“’711 patent”). As explained below, Petitioner has failed to carry its burden to show that any of the challenged claims are unpatentable.

The ’711 patent is directed to an innovative “staircase structure” for a 3D NAND memory, which addresses the challenges of forming vertical word line contacts in memory devices with increased storage capacity. Each independent claim of the ’711 patent requires the staircase structure to have steps where the gate stack is “disposed over” a dielectric layer within each step, a configuration that enhances fabrication yield and reduces costs.

The Petition relies on embodiments from two primary references, Kim (Ex.1005) for Grounds 1-2 and Park (Ex.1006) for Grounds 3-4. However, neither Kim nor Park disclose steps where the gate stack is “disposed over” a dielectric layer, as required by the independent claims of the ’711 patent. Furthermore, both Kim and Park fail to disclose the limitations of certain dependent claims, which specify additional structural and functional features of the patented staircase structure.

In an attempt to fill these gaps, the Petition improperly relies on a Person of Ordinary Skill in the Art's ("POSITA") knowledge and other prior art references. However, the Petition fails to provide any motivation to combine these references with Kim and Park or a reasoned analysis or evidentiary support for such combinations. Consequently, the Petition does not meet the necessary burden to demonstrate the unpatentability of the challenged claims.

## **II. Background**

### **A. The '711 Patent (Ex.1001)**

The '711 patent issued from U.S. Application No. 16/126,947, which was filed on September 10, 2018. Ex.1001 ("'711 patent") Cover. The '711 patent claims priority to a PCT application (PCT/CN2018/101308), filed on August 20, 2018, which claims priority to a Chinese application (CN 2017/10774754), filed on August 31, 2017. *Id.* Cover, 1:7-11.

The '711 patent discloses "a word line contact structure for three-dimensional (3D) memory array and methods for forming the same." '711 patent 1:34-36; Ex.2009 ("Campbell2") ¶¶23-33.

To meet the demand for higher storage capacity in 3D NAND memories, manufacturers have tried to increase the number of conductor/dielectric layer pairs in 3D memory devices. '711 patent 5:35-39. The added layers, however, create challenges in etching holes of differing depths above the staircase structure to create

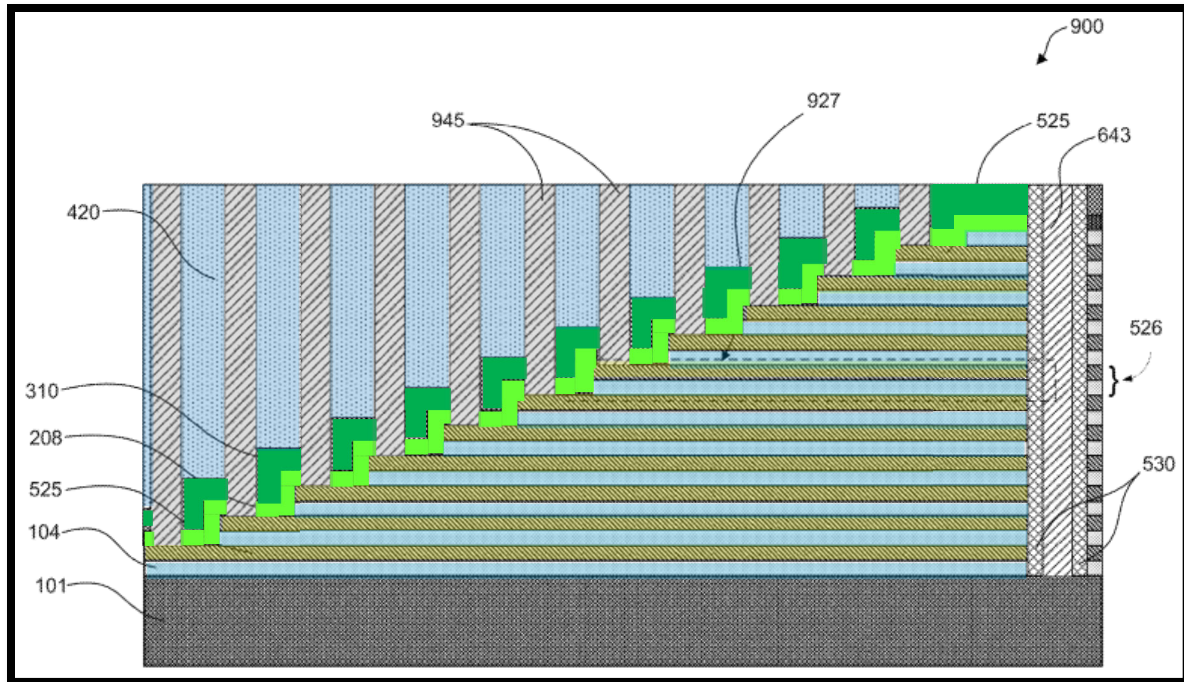
the vertical word line contacts. *Id.* 5:40-47. As the '711 patent recognizes, “contact holes for lower levels may be deeper than contact holes for upper levels.” *Id.* According to the '711 patent, “[t]ypically, all of the contact holes are formed with a single lithography mask and etching process.” *Id.* 5:47-48. But “[o]ften, before contact holes to the bottom levels are entirely formed, the materials exposed in contact holes at the upper levels are over-etched and lost.” *Id.* 5:48-51.

The '711 patent solves the problems of the prior art by disclosing an “etch stop film” over the staircase structure, which protects underlying staircase structure layers during the etching process of the staircase contact holes, such that contact holes with various depths can be etched simultaneously. *Id.* 5:54-65; Campbell2 ¶¶23-33. This improves fabrication yield and reduces cost. '711 patent 5:65-67; Campbell2 ¶26.<sup>1</sup> A barrier layer can also be introduced over the staircase structure “for protecting the underlying structure during subsequent etching processes.” *Id.* 7:35-39; Campbell2 ¶26. To implement these structures, the steps of the staircase arrange the gate stacks of the word lines over corresponding dielectric layers. '711 patent 6:4-5, 8:54-55, 10:29-34; Campbell2 ¶¶23-33.

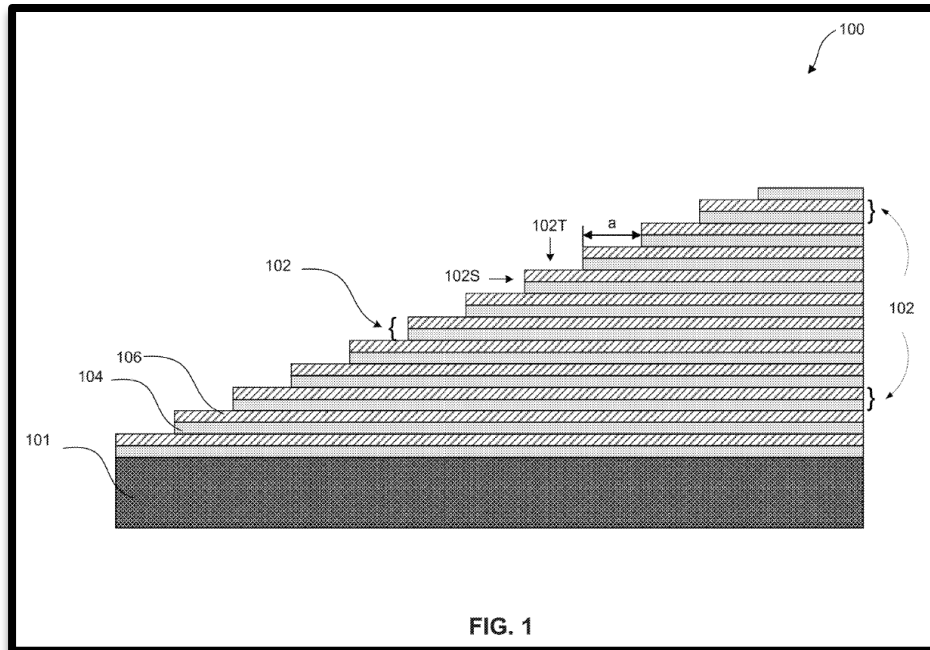
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<sup>1</sup> The patented solution also allows the formation of semiconductor interconnect structures for inter-connecting components at different layers with an uneven topology. '711 patent 5:67-6:3; Campbell2 ¶27.

Below is an annotated version of Figure 9A, showing an exemplary '711 patent 3D memory device staircase structure. The staircase structure 900 includes alternating layers of gate stacks 525 (yellow) over insulating layers 104 (lighter blue). '711 patent 6:4-5, 8:54-55, 10:29-34; Campbell2 ¶28. Each step of the staircase structure includes the first insulating layer 104 and a sacrificial layer 106, with a top surface 102T and a side surface 102S, as seen in Figure 1. '711 patent 6:4-5; Campbell2 ¶28. As seen in Figure 9A, the sacrificial layer 106 is removed and becomes the gate stack 525 during the manufacturing process. '711 patent 8:48-55; Campbell2 ¶28. A second insulating layer 208 (bright green) is formed on and directly contacting the top and side surfaces of each step and an etch-stop layer 310 (green) is formed on and directly contacting the second insulating layer 208. '711 patent 7:30-39, 7:56-58, 7:66-67; Campbell2 ¶28. A third insulating layer 420 (dark blue) is formed on and directly contacting the etch-stop layer 310. '711 patent 8:20-24; Campbell2 ¶28. Vertical interconnect access ("VIA") structures 945 (grey) are formed in VIA openings 840 in the third insulating layer 420. '711 patent 11:14-19; Campbell2 ¶28.

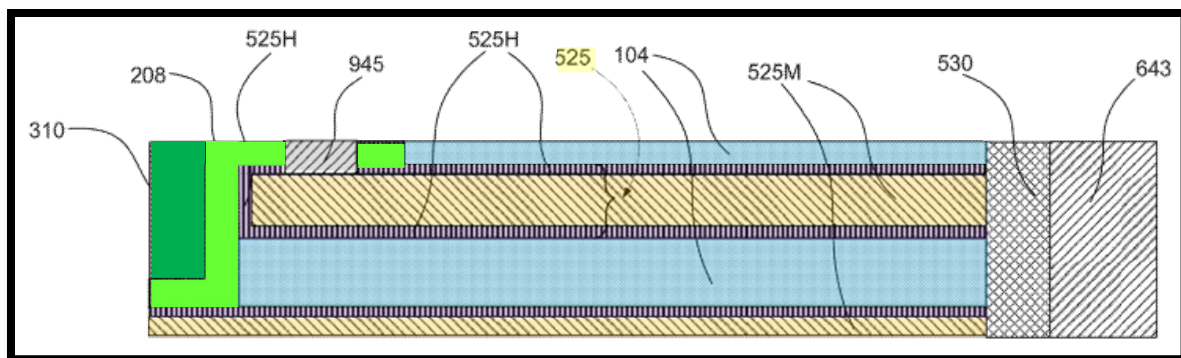


| No. | Structure                                          |
|-----|----------------------------------------------------|
| 525 | Gate Stack                                         |
| 104 | First Insulating Layer                             |
| 208 | Second Insulating Layer                            |
| 310 | Etch-Stop Layer                                    |
| 420 | Third Insulating Layer                             |
| 945 | Vertical Interconnect Access Conductive Structures |



'711 patent Fig. 9A (annotated) and color key; Campbell2 ¶28.

Figure 9B shows details of the gate stack 525 of Figure 9A above. The gate stack includes a high-k dielectric layer 525H (purple), which surrounds a gate conductive layer 525M (orange) with one side next to fifth insulating layer 530. '711 patent 8:65-9:4, 9:40-44; Campbell2 ¶33. The VIA conductive structures 945 (grey) may be directly disposed on an exposed portion of gate conductive layer 525M. '711 patent 11:16-22; Campbell2 ¶33.



| No.  | Structure                                          |
|------|----------------------------------------------------|
| 104  | First Insulating Layer                             |
| 525H | High-k Dielectric Layer                            |
| 525M | Gate Conductive Layer                              |
| 208  | Second Insulating Layer                            |
| 310  | Etch-Stop Layer                                    |
| 945  | Vertical Interconnect Access Conductive Structures |

'711 patent Fig. 9B (annotated) and color key; Campbell2 ¶33.

### **B. Person of Ordinary Skill in the Art**

Petitioner has proposed that a “POSITA in the field of the ’711 patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience).” Pet. 27. Petitioner has further proposed that the “POSITA would have been aware of and generally knowledgeable about 3D NAND’s structure, how it is manufactured, and its component parts.” *Id.* YMTC does not dispute this definition of a POSITA for purposes of these proceedings.

**C. Claim Construction**

The prior art Petitioner cites fails to disclose the subject matter of the challenged claims under any reasonable construction. Petitioner does not raise any claim construction disputes and alleges all terms have their plain and ordinary meaning. Pet. 26. While Patent Owner agrees that all claims should be construed according to their plain and ordinary meaning, there appears to be a dispute with respect to the meaning of the terms “on a side surface and a top surface of each step,” as it appears in claim 14 and its dependent claim 15, and the related term “on the side and top surfaces of each step,” as it appears in claim 15.

“On a side surface and a top surface of each step” should be construed as “directly contacting a side surface and a top surface of each step.” This construction is supported by intrinsic evidence. As claim 15 depends from claim 14, Patent Owner does not believe claim 15 needs to be independently construed. However, to the extent there is a dispute regarding the similar language of claim 15, namely “on the side and top surfaces of each step,” it should be construed as “directly contacting the side and top surfaces of each step.”

Petitioner contends the '711 patent specifies that “on” means “‘directly on’ something, but also includes the meaning of ‘on’ something with an intermediate feature or layer therebetween.” '711 patent 4:1-6. Based on this, Petitioner argues

that the term “on” in claim 14 includes components “both directly and indirectly on [the side surface and top surface of each step].” Pet. 59-60. But this argument fails.

Petitioner's argument is inconsistent with the intrinsic record. The '711 patent uses the term “on [a/the] surface” more narrowly than the term “on.” “[O]n [a/the] surface” means “directly contacting” that surface. For example, Figure 1 “illustrates a staircase structure 100 having an alternating layer stack *on a top surface* of a substrate 101.” '711 patent 6:4-5; Campbell2 ¶28.<sup>2</sup> The alternating layer stack directly contacts the surface of substrate 101 in Figure 1, reproduced below. Figure 2 shows the second insulating layer, or barrier layer, 208 is disposed “*on a side surface 102S and a top surface 102T*” of the staircase structure 100 seen in Figure 1. '711 patent 7:32-41; Campbell2 ¶28. Figure 3 shows etch-stop layer 310 is disposed “*on the top surface* of the second insulating layer on the staircase structure.” '711 patent 1:44-45, 12:15-18; Campbell2 ¶28. And Figure 4 shows insulating layer 420 is disposed “*on the top surface* of the etch-stop layer.” '711 patent 12:19-24; Campbell2 ¶28. Figure 4 is also reproduced below as showing the culmination of the layering described with respect to Figures 1-3. As described in each case above, the specified layer can be seen directly contacting the surface of the layer beneath it.

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<sup>2</sup> All emphases added unless otherwise indicated.

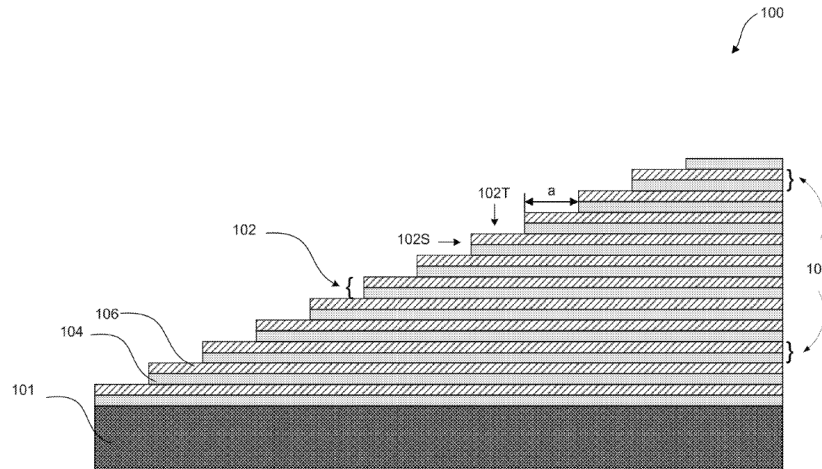


FIG. 1

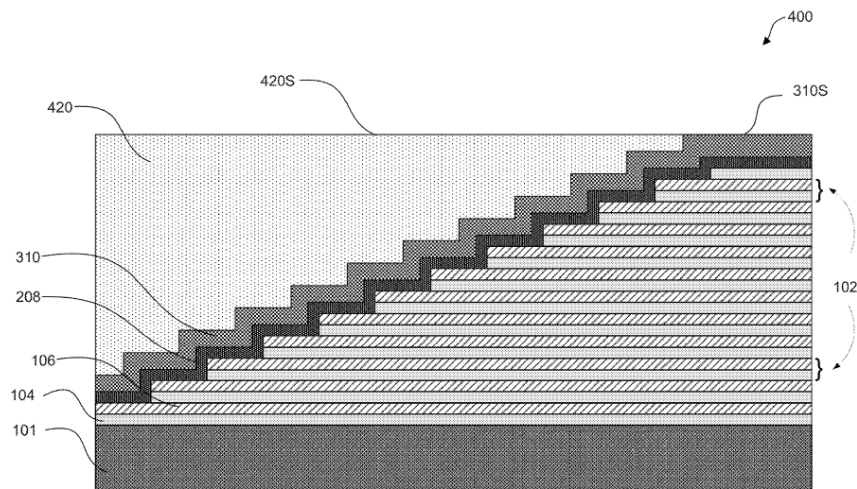


FIG. 4

Further, Petitioner's position that the etch-stop layer could be "on a *side* surface" while still having intervening layers is inconsistent with the specification equating "on" with "above" and "over." '711 patent 4:1-10.

If Petitioner argues that the surface of “each step” in claims 14 and 15 refers to the surface of additional layers placed on top of the staircase steps, such as the barrier layer or etch stop layer, that contradicts the specification.

Each step includes “a conductive layer disposed over a dielectric layer.” ’711 patent 14:7-8; *see also id.* 6:8-9. Figure 1 shows “a staircase structure 100 having an alternating layer stack.” *Id.* 6:4-5. The specification describes forming the “plural steps of staircase structure 100” using a repetitive etch-trim process and a mask, where “one staircase step is formed during each etch-trim cycle.” *Id.* 6:53-67. Each etch-trim cycle includes an etching process “that etches a height of a staircase step,” and a trimming process that “determines a width of a staircase step.” *Id.* 12:3-5. For example, Figure 1 shows a lateral dimension “a” of each step. *Id.* 7:16-18. This process is repeated for “a number of cycles corresponding to the number of steps or the number of dielectric layer pairs on the staircase structure.” *Id.* 12:6-8.

As Figures 9A and 9B show, each conductive structure penetrates the insulating layer 420, the etch-stop layer 310, the barrier layer 208, and the high-k dielectric 525H and “directly contacts the corresponding conductive layer of the each step.” *Id.* 14:15-17; *see also id.* 10:56-63, 11:14-19.

A reading of “step” that includes the layers covering each gate stack and insulating layer pair is also inconsistent with Petitioner’s and its expert’s own statements, which use “step” to refer to the underlying staircase structure made up

of a gate stack and dielectric layer, not the additional layers placed on top of that structure. Petitioner explains the '711 patent relates to a “staircase structure on an alternating conductor/dielectric stack” (i.e., alternative stack of gate and dielectric layers),” and that the staircase structure “*provides landing areas, i.e., steps, for the contacts* (which the '711 patent refers to as ‘conductive structures’) that physically connect to the gate layers.” Pet. 1. Similarly, Dr. Banerjee explains that in the '711 patent, “the word line contact structure is the *landing area* in which a vertical conductive structure 945 *makes contact with a particular step*” and “[t]he *landing area is also commonly referred to as the step*, because it is the step in the staircase.” Ex.1003 ¶56; *see also id.* ¶87 (“The steps provide landing areas for staircase contacts.”).

Dr. Banerjee is also clear that additional layers formed on top of the step are not part of the step itself. Referring to Figure 9A of the '711 patent, Dr. Banerjee explains that “an optional barrier layer 208 and an etch-stop layer 310 *cover* the side surface and a portion of the top surface *of each step*.” Ex.1003 ¶56; Pet. 23; *see also* Ex.1003 ¶145 (“It is obvious which gate stack and dielectric layer are paired to form a step, namely, the gate stack and the immediately below dielectric layer.”); Pet. 46.

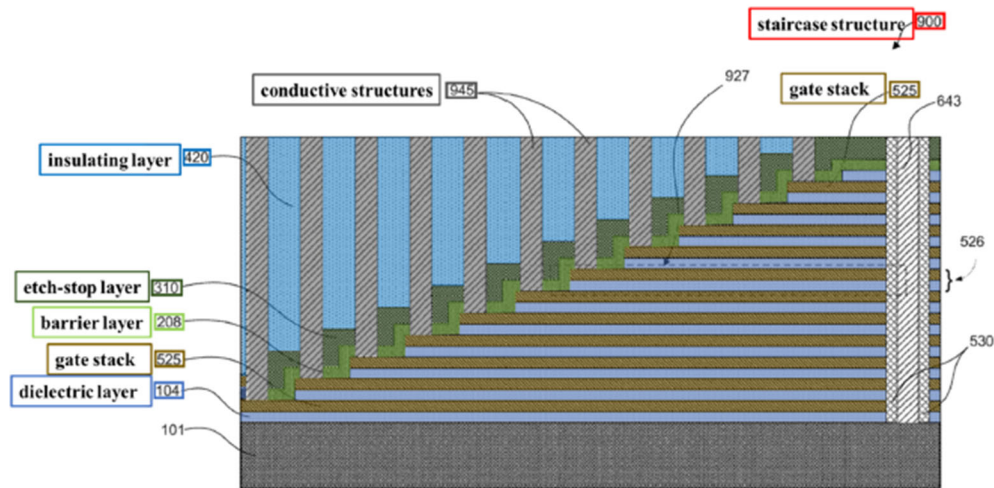
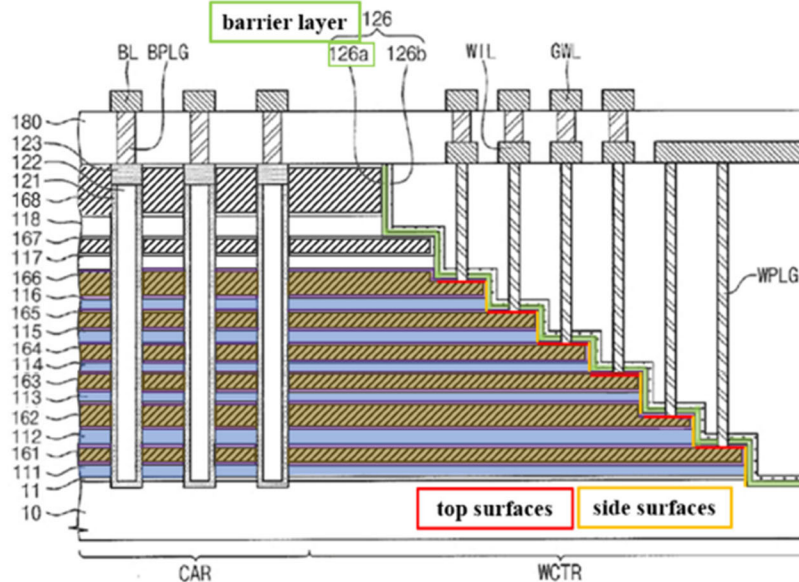


FIG. 9A

Ex.1003 ¶56.

Further, Dr. Banerjee provides an annotated version of his modified version of Kim's Figure 22A where he identifies the "side surfaces" and "top surfaces" of each step. As seen below, Dr. Banerjee places the "side surfaces" and "top surfaces" of each step on the underlying staircase structure, beneath additional layers such as the barrier or etch-stop layers.

**Gate-Stack-on-Top Fig. 22A**

Ex.1003 ¶110 (annotating Petitioner's modified "Gate-Stack-on-Top" version of Kim Fig. 22A); *see also id.* ¶121 (same).

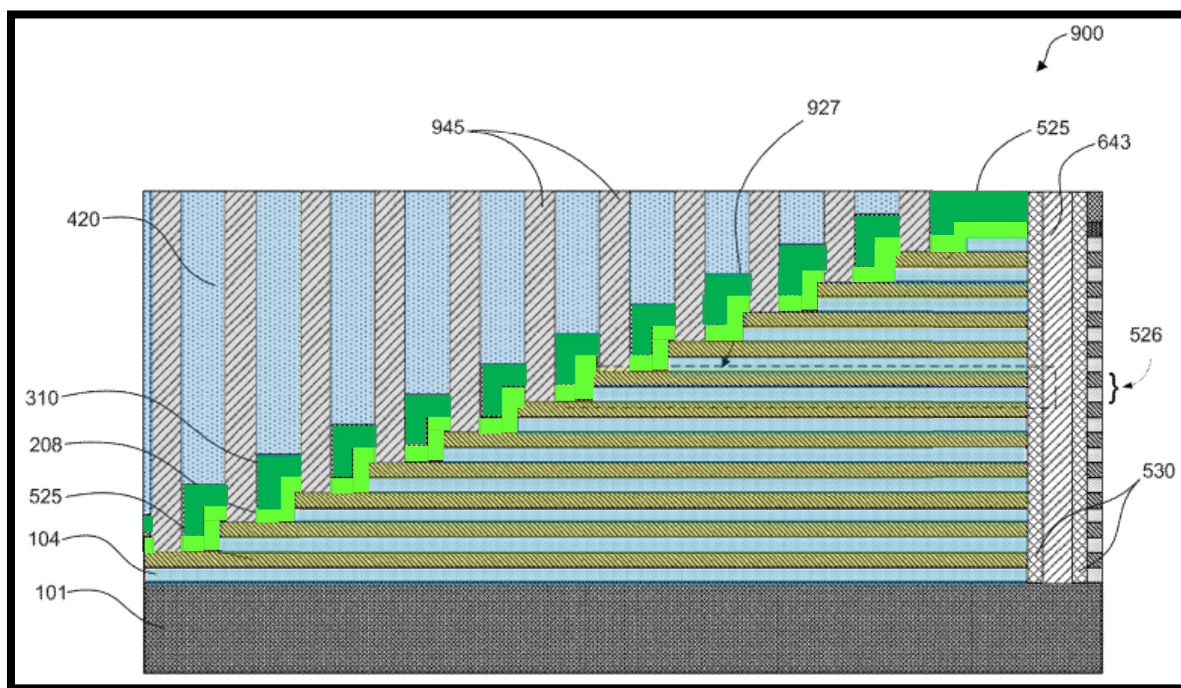
Moreover, Petitioner's argument renders the term "surface" superfluous in claims 14 and 15. Under Petitioner's view, there is no difference between being "on a side surface and a top surface of each step" and simply being "on a side and top of each step." Constructions that create such surplusage are disfavored. *Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.*, 853 F.3d 1272, 1288 n.10 (Fed. Cir. 2017) ("It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous."); *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006) ("[C]laims are interpreted with an eye toward giving effect to all terms in the claim.").

For these reasons, the term “on a side surface and a top surface of each step” as it appears in claim 14 should be construed to mean “directly contacting a side surface and a top surface of each step.”

### III. Ground I: Petitioner Failed to Demonstrate Kim in View of a POSITA's Knowledge Renders Obvious Claims 1-9, 11-16, and 18-19.

#### A. Kim does not disclose “each step compris[ing] a gate stack disposed over a dielectric layer.”

Each independent claim of the '711 patent requires “a plurality of steps” where “each step comprises a gate stack disposed over a dielectric layer.” '711 patent cl. 1. In other words, the '711 patent claims a staircase structure, where each step of that staircase includes a bottom dielectric layer and a top gate stack layer. This can be seen in annotated Figure 9A below, which shows alternating layers on each step with the yellow gate stacks disposed over the blue dielectric layers.

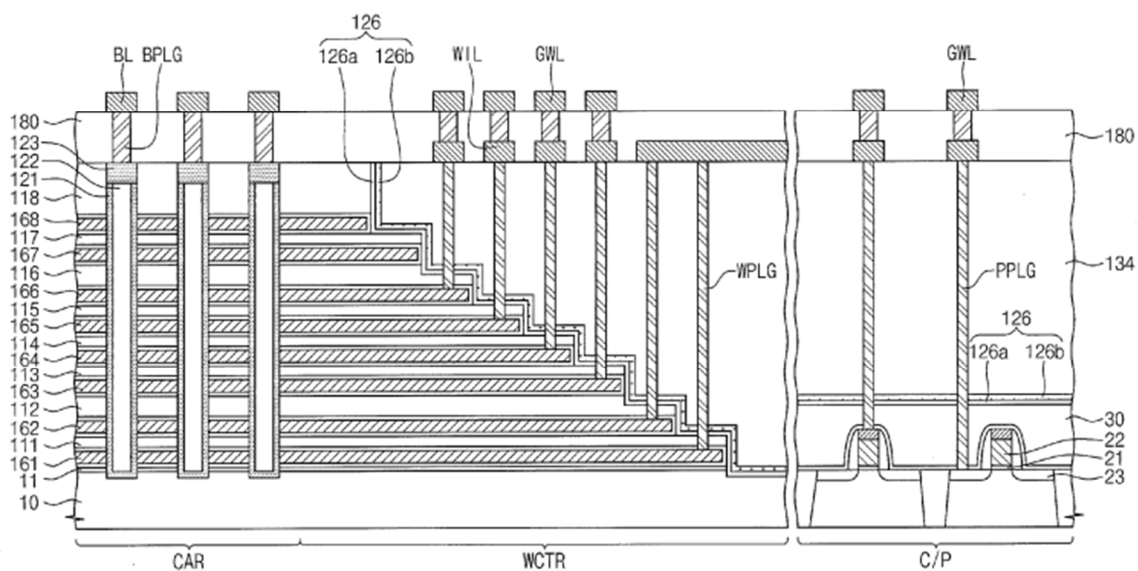


| No. | Structure                                          |
|-----|----------------------------------------------------|
| 525 | Gate Stack                                         |
| 104 | First Insulating Layer                             |
| 208 | Second Insulating Layer                            |
| 310 | Etch-Stop Layer                                    |
| 420 | Third Insulating Layer                             |
| 945 | Vertical Interconnect Access Conductive Structures |

'711 patent Fig. 9A (annotated) and color key; Campbell2 ¶¶28-32.

Petitioner admits its argument that Kim discloses this limitation “relies on Kim’s Figures 17A-22B.” Pet. 29. Yet as can be seen from the below figure, not only does Kim not disclose such an arrangement, the cited figures disclose the *opposite*, a white dielectric layer 111 disposed over a cross-hatched gate stack 161.

Fig. 22A



Ex.1005 (“Kim”) Fig. 22A; Campbell2 ¶¶35-37; Ex.2008 34:22-35:4.

**1. Petitioner improperly relies on multiple embodiments from Kim to justify manipulating the figures Kim discloses.**

Petitioner openly admits that Kim’s “figures show the opposite order” of the claims of the ’711 patent. *See* Pet. 32; Ex.1003 ¶¶69, 80; Campbell2 ¶36. In an effort to overcome this lack of disclosure, Petitioner inverts the order of the dielectric and gate stack layers and argues that other embodiments from Kim support that inversion. Pet. 29 (citing Kim Figs. 5A-14B); *see, e.g.*, Campbell2 ¶¶37-40. Yet even single-reference obviousness<sup>3</sup> requires a motivation to combine disparate

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<sup>3</sup> It is unclear whether Petitioner bases this argument on anticipation or obviousness. While styled as obviousness, Petitioner contends that “a reference invalidates if it enables a POSITA to ‘at once envisage’ ‘the claimed arrangement.’” Pet. 33 (citing *Chamberlain Grp., Inc. v. Techtronic Indus. Co.*, 935 F.3d 1341, 1350 (Fed. Cir. 2019)). That is the anticipation standard. *Id.* To the extent Petitioner contends the basis for this ground is anticipation, that argument was never properly disclosed in the petition. Regardless, such an argument would fail for the same reasons expressed in this section. Anticipation requires that “that the four corners of a single, prior art document describe every element of the claimed invention” and disclose those elements “arranged as in the claim[s].” *NetMoneyIN, Inc. v. Verisign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (internal quotations marks and citations omitted). It is

embodiments in one reference, along with a reasonable expectation of success. *In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017) (“[C]ombining multiple embodiments from a single reference” requires “a motivation to make the combination.”); *In re Kotzab*, 217 F.3d 1365, 1370 (Fed. Cir. 2000) (“Even when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference.”) (citations omitted). Petitioner makes no effort to provide either. Petitioner has not identified any benefit to inverting Kim’s layers, any problem that would be solved by doing so, or more broadly, any reason beyond hindsight. *See* Ex.2008 35:12-36:1 (“Q. [I]n your declaration you don’t list any benefits to reversing the order of the layers; right? A. I don’t think so.... Q. It’s a matter of simply choice, but there’s no reason you give to go one way or the other; right? A. No, I did not.”); Campbell<sup>2</sup> ¶43; *InTouch Techs., Inc. v. VGO Commc’ns, Inc.*, 751 F.3d 1327, 1351-52 (Fed. Cir. 2014) (describing “conclusory” testimony that a POSITA “*could* combine” prior art

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not enough that a prior art reference discloses only part of the claimed invention, which an “ordinary artisan might supplement to make the whole, or that it includes multiple, distinct teachings that the artisan might somehow combine to achieve the claimed invention.” *Id.* at 1371. Here, Petitioner has made no such showing for the same reasons expressed with respect to single reference obviousness.

references, “not that they *would* have been motivated to do so” as “fraught with hindsight bias”) (original emphasis).

Petitioner's manipulation of Kim's Figure 22A is unjustified. Petitioner reversed the order of the “insulating layers” and “gate stacks” of Figure 22A, changing the shading and labels of the original figure to match. Campbell<sup>2</sup> ¶¶37-40. For example, Petitioner changes the label “116” (corresponding to an insulating layer) to “166” (corresponding to a gate electrode) and “115” (corresponding to an insulating layer) to “165” (corresponding to a gate electrode), and so on. *Id.* ¶¶38-39; *see, e.g.*, Pet. 37. Petitioner has not established any motivation to combine the different embodiments of Kim to arrive at the manipulated version of Figure 22A. At most, Petitioner asserts that “[a] POSITA would have understood that descriptions of one of Kim's embodiments apply to other embodiments except where the embodiments differ.” Pet. 29. But that statement is unsupported by anything but Dr. Banerjee's conclusory recitation of the same language. Ex.1003 ¶¶70-71. That is insufficient to show a motivation to combine. *BlephEx, LLC v. Myco Indus., Inc.*, 24 F.4th 1391, 1401 (Fed. Cir. 2022) (finding no motivation to combine features based on prior art's teachings of features “[i]n other embodiments”).

Further, the embodiments Petitioner seeks to combine *do* differ in material ways such that their descriptions would not apply to one another, and a POSITA would not combine them or have a reasonable expectation of success doing so.

Petitioner admits it “relies on Kim’s Figures 17A-22B” for this Petition, but Petitioner *only* cites to language from *other* embodiments to argue Kim discloses a gate-stack-on-top arrangement. Pet. 28-29 (citing Kim [0090]-[0091] with reference to Figs. 4, 8A and 8B, and [0240] with reference to Fig. 31 that explicitly refers back to Figs. 8A and 8B). And the language Petitioner cites and that appears in Kim’s other embodiments is conspicuously *absent* from the description of Figures 17A-22B. Campbell2 ¶36. Moreover, the embodiments in Figures 4, 8A-8B and 31 are missing key elements disclosed only in Figures 17A-22B, including an etch-stop layer and a barrier layer. *Id.* Petitioner fails to provide any motivation to combine these embodiments, much less cherry pick the purported layer-switching aspect and apply it to Figures 17A-22B from which the specification specifically leaves it out. For each of these same reasons, a POSITA would not be motivated to combine the embodiment of Figures 17A-22B with the embodiments of Figures 4, 8A and 8B or 31. *Id.*

Even if a POSITA would have been motivated to combine the disparate embodiments of Kim that Petitioner relies on, there would not have been a reasonable expectation of successfully doing so because of key differences between the embodiments and the impact on the design and manufacturing process, as discussed further below. *Eli Lilly & Co. v. Teva Pharms. Int’l GmbH*, 8 F.4th 1331, 1344 (Fed. Cir. 2021) (citations omitted) (“A finding by the Board that a patent

challenger has demonstrated a motivation to combine references does not necessarily imply that the challenger has also met its burden of showing a reasonable expectation of success in achieving a claimed method of treatment.”); *see infra* Section III.A.2.

**2. Petitioner improperly relies on additional prior art references and a POSITA's knowledge to justify inverting the layers.**

To cure Kim's deficient disclosures, Petitioner improperly relies on prior art references not included in its obviousness combination and a POSITA's knowledge to gap-fill a justification for inverting the layers.<sup>4</sup>

Petitioner attempts to rely on prior art references not at issue in this Petition, such as Chen, Ohsaki, and Shin, to provide support for certain limitations being obvious to a POSITA. *See, e.g.*, Pet. 38. But Petitioner is not entitled to make an end-run around establishing a motivation to combine and reasonable expectation of success for these references. If Petitioner intended to rely on Chen, Ohsaki, or Shin to supply a missing limitation, it was required to make them part of an obviousness combination and conduct the proper analysis to support their use. It failed to do so here.

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<sup>4</sup> Petitioner improperly relies on the same prior art references not at issue in this Petition to cure similarly deficient disclosures in Park. *See* Pet. 66. This section applies with equal force to Petitioner's corresponding arguments regarding Park.

To the extent Petitioner relies on these references as an indication of general knowledge, that argument fails too. A Petitioner “must specify where each element of the claim is found in the prior art patents or printed publications *relied upon*.” 37 C.F.R. § 42.104(b)(4). The Petition does not include these references as references in this ground and is not entitled to rely on them to supply a limitation that Kim does not disclose. The Acting Director of the USPTO recently issued a memorandum that goes into effect September 2025 clarifying as much, explaining that “enforcement of Rule 104(b)(4) means that applicant admitted prior art (AAPA), expert testimony, common sense, and other evidence that is not ‘prior art consisting of patents or printed publications’ (collectively ‘general knowledge’) may not be used to supply a missing claim limitation.” *See* USPTO Memorandum, Enforcement and Non-Waiver of 37 C.F.R. § 42.104(b)(4) and Permissible Uses of General Knowledge in Inter Partes Reviews at 1 (July 31, 2025).

Even in the context of invalidity more generally, the Court of Appeals for the Federal Circuit has held that general knowledge may only supply a missing claim limitation when “the missing limitation in question [is] *unusually simple* and the technology *particularly straightforward*.” *Motorola Mobility LLC v. Largan Precision Co.*, IPR2024-00688, Paper 7 at 29 (P.T.A.B. Oct. 28, 2024) (quoting *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337-38 (Fed. Cir. 2020)) (original emphasis). But even then, it “cannot be used as a wholesale substitute for

reasoned analysis and evidentiary support.” *Google*, 948 F.3d at 1337-38. Thus, relying on the knowledge of a POSITA to supply missing limitations is an exception that is only available in limited circumstances for “unusually simple” limitations within “particularly straightforward” technologies. *See, e.g., Square One Choices Inc. v. Ditec Sols., LLC*, No. 2:23-CV-555-HCN-DBP, 2025 WL 918966, at \*9 (D. Utah Mar. 21, 2025) (“flexible mat” limitation for a silicone mat mold); *FullView, Inc. v. Polycom, Inc.*, No. 2023-1201, 2024 WL 1843686, at \*5 (Fed. Cir. Apr. 29, 2024) (“contiguous support structure” limitation for mechanically supporting camera and providing conduit for camera cables); *Tesla, Inc. v. Autonomous Devices, LLC*, No. IPR2023-01169, 2025 WL 33587, at \*24 (P.T.A.B. Jan. 6, 2025) (limitation to record input by different users by recording input from a pressed button or move of a joystick controller).

But here, the missing limitations of “a gate stack disposed over a dielectric layer” is not “unusually simple,” nor is 3D NAND memory array design a “particularly straightforward” technology. *See, e.g., Janssen Pharms., Inc. v. Mylan Laboratories Ltd.*, No. 2:20-cv-13103, 2023 WL 3605733, at \*21 (D.N.J. May 23, 2023) (limitation related to pharmacokinetics not “unusually simple” or technology at issue “particularly straightforward”), *aff’d*, No. 2023-2042, 2025 WL 946390 (Fed. Cir. Mar. 28, 2025); *Abbott Diabetes Care Inc. v. Dexcom, Inc.*, No. IPR2022-00913, 2023 WL 7225556, at \*16 (P.T.A.B. Nov. 2, 2023); *see Campbell* 2 ¶¶41-43.

This technology does not meet that standard. As described herein, 3D semiconductor design and manufacturing, which employs concepts of chemical, mechanical, and electrical engineering on a microscopic scale, is not “particularly straightforward” technology. Campbell2 ¶¶41-42. This is especially true for etch processes involved in device manufacturing, where each detail is important and can have significant effects. *Id.* ¶41. Nor are the missing limitations “unusually simple” such that Petitioner may rely on a POSITA’s knowledge to make up for them. *Id.* Dr. Banerjee correctly stated multiple times in deposition that “details matter” and “specifics matter.” *See* Ex.2008 40:20-22, 41:5-8, 45:12, 46:18, 57:2-3, 61:18-19; Campbell2 ¶41. Rearranging the layers of a semiconductor device requires changes in both device design and manufacturing processes, including changes to etching processes. *Id.* Etch processes depend on multiple parameters that are optimized to achieve desired etch characteristics for a specific device design. *Id.* When the device design changes, various etching parameters must be re-optimized to design a new etching process for the new design, such as etch chemistries, or the combination of gases used as the etchant, plasma power, bias voltage, chamber pressure, temperature, and etch time. *Id.*; Ex.2008 37:9-41:8 (identifying these various etch parameters); *see, e.g., id.* 61:21-64:10 (confirming that any one of these parameters can effect etch-depth). As Dr. Banerjee admitted, such changes can also affect the

number and sequence of steps in the etching processes. Ex.2008 37:9-41:8, 47:8-48:1, 61:21-64:10.

As further evidence of the complexity of this technology, Petitioner appears to have made a mistake in altering Kim's Figure 22A. As Dr. Banerjee acknowledged, Figure 22A required other modifications once the order of the layers was changed. For instance, Petitioner also altered the depth of the word line contacts in Figure 22A, which would have required changes to the etch-parameters as described above. *See id.* 36:9-41:8; Campbell2 ¶42. However, Kim's Figure 22A also includes a lower gate insulating layer labeled as element 11. *See, e.g.,* Kim [0061], [0064], [0071], [0142]. The purpose of that layer is to prevent "electrical crosstalk" between the lowermost gate and the substrate. Ex.2008 30:21-31:22; *see* Campbell2 ¶42. Yet when Petitioner altered the layer order, it placed an insulating layer in contact with the substrate, rather than a gate stack. *See* Ex.1003 ¶90, Modified Fig. 22A. This made the lower gate insulating layer unnecessary. Campbell2 ¶42. Despite that, Petitioner did not account for this change or modify the placement of the lower gate insulating layer, even though it was no longer needed. *Id.*

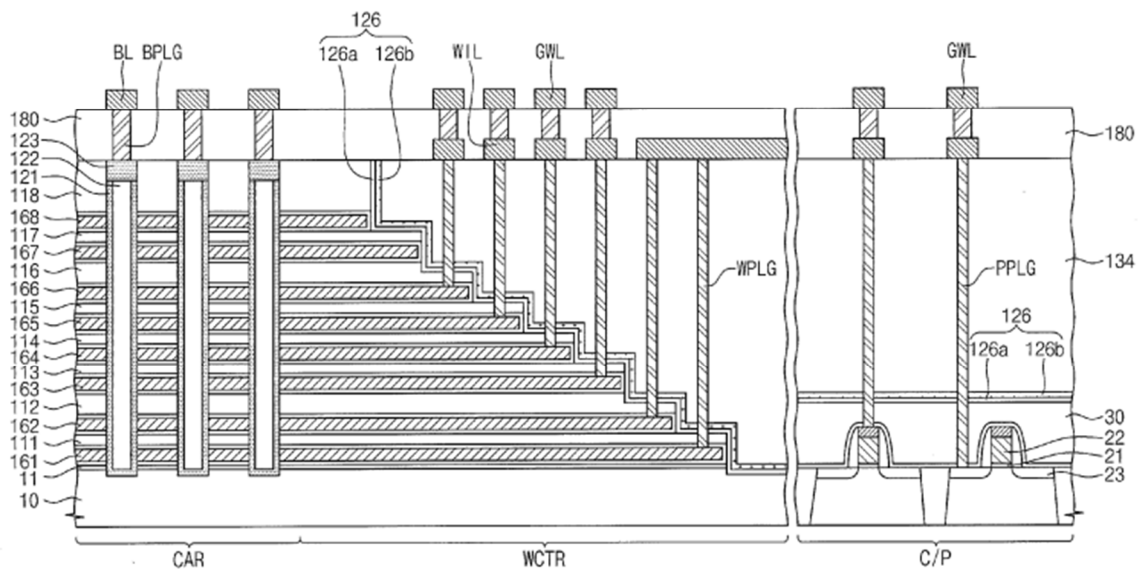
Further, Petitioner argues a POSITA would have a reasonable expectation of success in combining a POSITA's knowledge of a gate-stack-on-top layering because, according to Petitioner's expert, "either order was compatible with

common deposition techniques such as CVD or ALD used to deposit these layers” and deals only with two layers. Pet. 33; Ex.1003 ¶81. But regardless of deposition techniques or number of layers, and as described above, etch processes are highly dependent on, among other things, the materials used and the order of layers. Campbell2 ¶41. Even Dr. Banerjee confirmed that “whenever you have different materials combinations, you have to tweak the etch chemistries a little bit” and that “once again, details matter.” Ex.2008 45:9-12; *see also id.* 44:18-21 (“Q. So once those gases get you through 126b, do you have to change the etch chemistry again when you get to 126a? A: Generally speaking.”). Further, reducing the number of protective layers over the gate stack, which Petitioner’s modification does by putting the gate stack on top of the insulating layer of each step, increases the risk of short-circuits from over-etching. *See* Campbell2 ¶54; Ex.2008 48:20-49:8 (“Q. [I]f you have the—the dielectric layer there between—between the high-k dielectric and the stop layer 126a, that’s going to increase the safety margin; right? ... A. I mean, in general, the more different materials that you have that the etch has to go through, in general, that provides additional safety margins.”). Thus, even if a gate-stack-on-top ordering was known, a POSITA would not have a reasonable expectation of success applying it on that basis alone.

### **3. Petitioner's unjustified manipulation of the figures misled the Board.**

To be clear, Petitioner’s manipulation of Kim’s Figure 22A appears to have had real consequences in misleading the Board concerning what Kim actually discloses. In particular, the Institution Decision states that “the bottom-most step has a lower dielectric layer 111 on which the gate stack 161 is disposed,” and cites not to Petitioner’s annotated Figure 22A, but to the Figure 22A actually disclosed in Kim. ID at 9. As can be seen from the unmodified Figure below, that is simply not true. Rather, Figure 22A shows the opposite, a lower gate stack 161, on which the dielectric layer 111 is disposed.

Fig. 22A



To be sure, gate stack 162 is also disposed over insulating layer 111, but as the Board acknowledged, “that pair is shown to involve two steps, not as a corresponding single step.” ID at 9. Given that the claim requires “each step” to comprise a gate stack disposed over an insulating layer, any combination requiring two different steps would not meet that limitation.

**B. Kim does not render claims 14 or 15 obvious because Kim does not disclose “the etch-stop layer is formed on a side surface and a top surface of each step.”**

Petitioner fails to show claim 14 is obvious over Kim.<sup>5</sup> Dependent claim 14 claims “[t]he semiconductor structure of claim 13, wherein the etch-stop layer is formed on a side surface and a top surface of each step.” ’711 patent cl. 14. However, the etch-stop layer of Kim is formed on a side surface and a top surface of the *barrier layer* and not on a side surface and a top surface of *each step* of the plurality of steps.

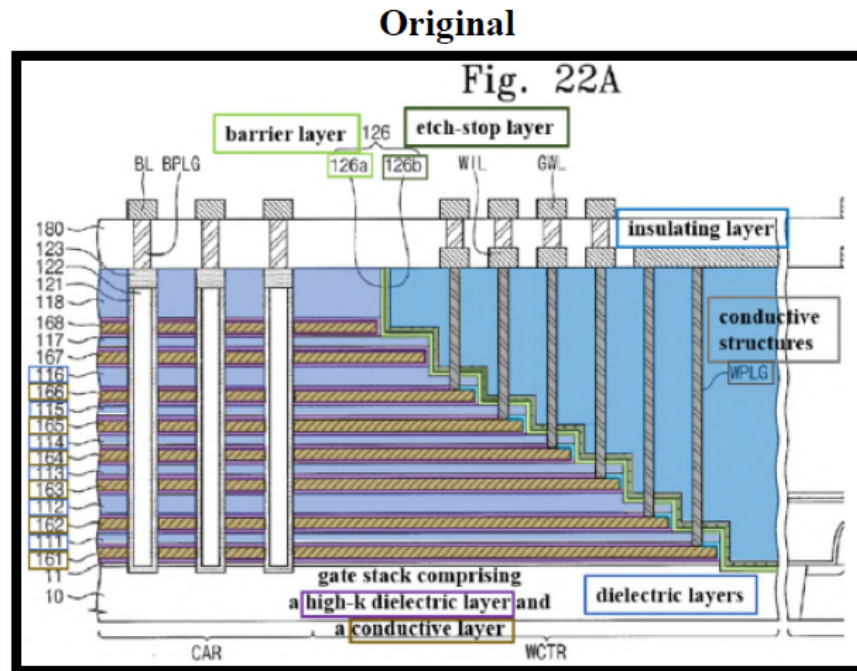
Petitioner maps Kim’s “second stop layer 126b” to the ’711 patent’s “etch-stop layer,” and Kim’s “first stop layer 126a” to the ’711 patent’s “barrier layer.” *See, e.g.*, Pet. 35-43; Campbell2 ¶45. And as seen in Figure 22A, the “second stop layer 126b” (i.e., etch-stop layer) is “conformally formed *on the first stop layer 125a*,” (i.e., barrier layer), and not on the side and top surfaces of the plurality of steps. Kim [0187]; Campbell2 ¶46; *see also* Pet. 60. Instead, the “first stop layer

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<sup>5</sup> These arguments apply with equal force to claim 15, which depends from 14.

125a [i.e., barrier layer] is formed *on side and top surfaces of the plurality of steps.*”

Pet. 60; Campbell2 ¶46. Thus, Petitioner fails to show Kim discloses “the etch-stop layer is formed on a side surface and a top surface of each step.”



Kim Fig. 22A (annotated); Campbell2 ¶45.

Petitioner argues this limitation is met because the '711 patent “disclos[es] that ‘on’ something includes both directly and indirectly on that something.” Pet. 60. But as explained previously, the '711 patent uses the term “on [a/the] surface” of something more narrowly than the term “on,” to mean “directly contacting” the surface of something. *Supra* Section II.C.

Thus, as seen in at least Figure 22A, Kim does not disclose “the etch-stop layer is formed on a side surface and a top surface of each step,” as required by dependent claim 14.

To the extent Petitioner argues Kim discloses claim 14 in Figure 34, Petitioner has waived this argument. Petitioner makes no mention of Figure 34 in its Petition, nor does Petitioner meet its burden to show how Figure 34 meets the other limitations of the '711 patent or would be combined with other embodiments to do so.

**IV. Ground II: Petitioner Failed to Demonstrate Kim in View of Fang Renders Obvious Claims 10 and 17.**

Claims 10 and 17 of the '711 patent claim “a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.” Kim does not disclose the thickness of any alleged etch-stop layer. Campbell<sup>2</sup> ¶48 (citing Ex.2008 42:8-16). Thus, Petitioner relies on Fang for that element. However, Petitioner fails to establish a motivation to combine Kim and Fang to render dependent claims 10 and 17 obvious. *See id.* ¶¶48-55.

Petitioner argues that a POSITA would be motivated to apply Fang's disclosure of etch-stop-layer thickness on Kim's staircase structure primarily because Kim does not itself disclose an etch-stop-layer thickness and Fang does. Pet. 64-65. But this is an inadequate motivation to combine analysis. *Adidas AG v. Nike, Inc.*, 963 F.3d 1355, 1359 (Fed. Cir. 2020) (“Fundamental differences between the references are central to th[e] motivation to combine inquiry.”). Petitioner ignores meaningful differences between Kim and Fang both with respect to the materials they use and the design elements they call for. These differences would not motivate

a POSITA to combine Fang's etch-stop layer thicknesses to Kim. Further, a POSITA would not have a reasonable expectation of successfully achieving such a combination.

**A. Fang is directed toward carbon-doped silicon nitride etch-stop material, which Kim does not use.**

Petitioner attempts to combine Fang's etch-stop layer thicknesses with Kim because Kim fails to disclose any etch-stop layer thicknesses. Pet. 64-65; Ex.2008 42:8-16. But Petitioner ignores significant differences between Fang and Kim's etch-stop materials that counsel against their combination. Fang is directed towards carbon-doped silicon nitride, which Kim does not use. *See* Ex.1007 ("Fang") Title, Abstract, [0020], [0022] (identifying carbon-doped silicon nitride as the primary example of "etch stop material 130"); *see also e.g.*, Fang cls. 1-27 (*all claims* explicitly using carbon-doped silicon nitride); Kim [0186], [0187]; Campbell2 ¶49; *see* Ex.2008 51:8-15 ("Q: Fair to say that all of the claims require a carbon-doped silicon nitride etch-stop? ... A: Okay. The ones that I'm seeing all have carbon-doped silicon nitride ...."). This difference is important for multiple reasons.

First, a POSITA would know that different materials have different etch chemistries and would not be motivated to use Fang's carbon-doped silicon nitride etch-stop layer thicknesses in Kim where Kim never uses that material. *See* Kim [0186], [0187] (disclosing only silicon oxide, silicon carbide, silicon nitride (without carbon doping), silicon oxynitride, and silicon oxycarbide and possible etch-stop

materials). Campbell2 ¶49; Ex.2008 41:5-8 (“Q: The impact of all of these parameters on the etch depth is going to depend on the specific materials that you’re etching through correctly; correct? A: Yes.”). Petitioner’s expert, Dr. Banerjee, explains that “[d]ifferent materials react to an etchant differently and an etching rate is used to characterize how fast or slow an etchant etches through a particular material” and that “a material also can react differently to different etchants. For example, a material may have a high etching rate for one etchant and a low etching rate for a different etchant.” Ex.1003 ¶52; *see* Ex.2008 55:19-56:9; Campbell2 ¶49. A POSITA would know that etch-stop-layer thicknesses are not fungible across different materials. Here, Fang’s etch-stop-layer thicknesses are specific to carbon-doped silicon nitride. *See* Fang [0020], [0022], cls. 1-27; Campbell2 ¶49. Kim never uses carbon-doped silicon nitride. Campbell2 ¶49. Thus, Fang’s etch-stop thicknesses are not applicable, and thus irrelevant, to the necessary thickness for the materials Kim discloses, and a POSITA would not be motivated to combine Fang’s carbon-doped silicon nitride etch-stop-layer thicknesses with Kim simply because “Kim does not specify a thickness.”

Relatedly, a POSITA would know that Fang’s etch-stop-layer thicknesses are specific to a combination of carbon-doped silicon nitride etch-stop material and a silicon nitride sacrificial layer—a combination Kim also does not use. *See* Fang [0019]-[0022] (identifying *only* silicon nitride as the “nitride material 120” and

carbon-doped silicon nitride as the primary “etch stop material 130”); *see also e.g., id.* [0015], [0019], [0025], cls. 21-22; Campbell2 ¶50. For example, Fang states that “[s]ince the etch stop material 130 [i.e., carbon-doped silicon nitride] is not substantially removed by the etch chemistry used to remove the nitride materials 120 [i.e., silicon nitride] ..., *the thickness of the etch stop material 130 may be minimal and yet still provide desired etch stop properties.*” Fang [0021]. Kim, however, never contemplates a carbon-doped etch stop material, much less the combination of carbon-doped silicon nitride etch stop material with a silicon nitride sacrificial layer. Campbell2 ¶50. And as discussed below, Kim also uses a high-k dielectric surrounding the conductive layer of each step. *Id.* Thus, Petitioner is incorrect that a POSITA would look to Fang for exemplary etch stop thicknesses for use in Kim where Kim uses a different etch-stop material and sacrificial layer combination, and adds a high-k dielectric layer surrounding the gate stack.

Further, Petitioner argues that Kim's and Fang's etch-stop-layer disclosures are similar in that both disclose an etch-stop layer formed of silicon nitride. This is flatly wrong.<sup>6</sup> Fang teaches away from the combination by explicitly *prohibiting* an etch-stop layer material of silicon nitride, which Kim permits. *Bradium Techs. LLC*

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<sup>6</sup> Petitioner makes the same incorrect statements about the Park and Fang combination as well.

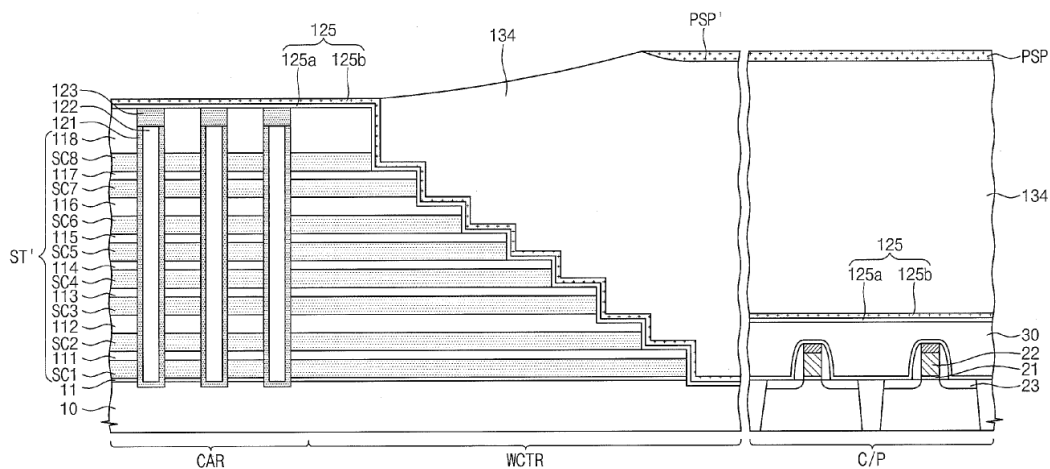
*v. Iancu*, 923 F.3d 1032, 1047 (Fed. Cir. 2019) (“A prior art reference teaches away if it ‘criticizes, discredits, or otherwise discourages the solution claimed.’”) (citing *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004)); *see* Kim [0187]; Fang [0020]; Campbell2 ¶51. Fang states that the etch stop material may be “***any material that is not substantially removed (e.g., etched) during removal and replacement of the nitride materials 120*** of the staircase structure,” where “the nitride material 120 is silicon nitride (SiN).” Fang [0019]-[0020]. In other words, Fang *does not allow* for silicon nitride as an etch stop material and specifies an etch-stop material of carbon-doped silicon nitride precisely because of its specific etch selectivity with (i.e., a different etch chemistry than) silicon nitride. *Id.*; *see* Ex.2008 55:4-9 (“Q. Is it fair to say that carbon doping has an impact on the etch rate of the silicon nitride? A: It could. If you left everything else the same in the etch process, changing the composition in general will change the etch rate.”); Campbell2 ¶51. Thus, Petitioner is wrong that both Kim and Fang disclose silicon nitride etch-stop material, and a POSITA would not be motivated to adapt Fang’s etch-stop layer thicknesses to Kim for that reason. Nor would a POSITA have a reasonable expectation of success adapting Fang’s etch-stop layer thicknesses to Kim where Kim does not use carbon-doped silicon nitride.

Petitioner’s other arguments for why a POSITA would be motivated to combine Fang and Kim are wholly inadequate. Petitioner suggests a POSITA would

have been motivated to combine Fang with Kim because, according to Petitioner, Fang's focus on "preventing over-etching shallower openings when etching openings for the word-line conductive structures" is an important consideration for manufacturing 3D memory devices and "dovetails" with Kim's focus "to reduce or prevent damages to the device during manufacturing." Pet. 64-65. But Fang and Kim are focused on solving *different* problems, and their disparate focuses do not provide a motivation to combine the references. *See* Campbell2 ¶¶52-53. As demonstrated below, Petitioner attempts to establish motivation to combine by shoehorning Fang's focus on preventing certain over etching of the conductive structure openings into an over-generalized characterization of Kim.

Kim's device is separated into three distinct regions: a cell array region (CAR), a word line contact region (WCTR), and a peripheral circuit region (C/P). Kim [0036]; Campbell2 ¶52. These regions are marked for identification in Kim's figures, including in Figures 17-22. For example, these regions are identified in Figure 19A below:

Fig. 19A



Kim is focused on reducing or preventing “dishing”<sup>7</sup> that can occur over the peripheral circuit region (C/P) and contact region (WCTR) when planarizing, or mechanically polishing down, the interlayer dielectric.<sup>8</sup> Kim [0025]-[0026], [0104],

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<sup>7</sup> “Dishing” is an unintentional recess in the interlayer dielectric over the WCTR and C/P regions that occurs because the contact pads 123 of the cell array region (CAR) may have a different removal rate from the interlayer dielectric, meaning the interlayer dielectric on the WCTR and C/P regions “may be etched faster than the contact pads 123 of the cell array region.” Kim [0105], [0190]-[0197].

<sup>8</sup> Figure 19A shows interlayer insulating pattern 134 instead of interlayer dielectric 130 because Figure 19A is post-planarization, but they refer to the same component. For example, Figure 18A shows the interlayer dielectric 130 before any planarization

[0190]-[0197]; Campbell2 ¶52. In addition to dishing over the WCTR and C/P regions, the planarizing process can cause damage to the contact pads 123 in the adjacent CAR region. Kim [0027], [0105], [0190]-[0197]; Campbell2 ¶52. Kim discloses forming a “polishing stop layer PSL” over the interlayer dielectric and “etch stop layer 125” over the contact pads 123 that, due to their etch selectivity, can reduce or prevent dishing and damage to the contact pads 123 in the CAR region. Kim [0027], [0105], [0190]-[0197]; Campbell2 ¶52. Thus, to the extent Kim is focused on reducing or preventing damage “to the device during manufacturing,” it is targeted toward preventing damage resulting from a specific process (polishing), to specific components (contact pads 123), in a specific region of the device (cell array region CAR). Campbell2 ¶52.

Fang is directed toward an entirely different problem, resulting from a different process, in a different region of the device. Specifically, Fang is directed toward preventing over-etching, or “punch through,” of shallow openings for word-line conductive structures in the region Kim refers to as the word-line contact region,

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process occurs. In later Figures, such as Figure 19A, the post-planarized interlayer dielectric is referred to as interlayer insulating pattern 134. *See* Kim [0193]. The same is true of the polishing stop layer PSL before planarization and the polishing stop pattern PSP' after planarization. *See id* [0196]-[0197].

or WCTR. Fang [0004], [0008]; Campbell2 ¶53. Fang discloses using a single etch-stop layer formed directly on the insulating and conductive layers of the staircase structure to prevent “punch through” into the conductive material of the step during the chemical etching processes used to create openings for the word-line conductive structures. Fang [0004], [0008]; Campbell2 ¶53. Given these disparate issues, a POSITA would not be motivated to combine Fang and Kim in the manner or for the reason Petitioner suggests. Campbell2 ¶53.

Moreover, Petitioner's only specific reason a POSITA would be motivated to adapt Fang's etch-stop layer thicknesses to Kim is that Kim does not itself specify a thickness. *See* Pet. 64-65. But as discussed above, not only is Kim concerned with an entirely different problem, but a POSITA would know that different materials have different etch chemistries, and a POSITA would not be motivated to use etch-stop layer thickness ranges for carbon-doped silicon nitride in Kim where Kim never uses that material.

**B. Structural differences between Fang and Kim counsel a POSITA against applying Fang's etch-stop layer thicknesses to Kim.**

In addition to the important differences between Fang and Kim's materials, Petitioner also ignores significant structural differences that would counsel a POSITA against adapting the etch-stop layer thicknesses of Fang to Kim. *See* Campbell2 ¶¶54-55.

A POSITA would understand that the purpose of the etch-stop layer is to protect underlying structures during the etching process, making certain structural differences, such as the number and type of protective layers used, important to determining the processes and necessary thickness of an etch-stop layer. *See, e.g.*, Fang [0026] (“[U]sing the etch stop material 130 according to embodiments of the disclosure prevents or reduces punch through into the conductive materials 140.”); Ex.1003 ¶94 (“[A]lthough Kim does not expressly state that the second stop layer 126b serves as an etch stop, a POSITA would have understood the etch selectivity of the second stop layer to serve the purpose of preventing punch-through and protecting underlying structures.”) (citing Kim [0186]-[0187]); Campbell2 ¶¶54-55. Further, a POSITA would also understand that each additional layer may change the necessary etch process to form vias for the conductive structures of each step. Campbell2 ¶¶54-55.

Kim discloses using a high-k dielectric layer around the conductive layer of each step while Fang does not. *See, e.g.*, Kim [0148], [0151], Fig. 22A. A POSITA would know that use of a high-k dielectric layer surrounding the conductive layer provides added protection to the gate stack layer and affects the necessary etch processes, which can affect the thickness of the etch-stop layer. Campbell2 ¶¶50, 55; *see* Ex.2008 49:5-8 (“[T]he more different materials that you have that the etch has to go through, in general, that provides additional safety margins.”). Thus, a POSITA

would not be motivated to apply Fang's etch-stop layer thicknesses to Kim's design using a high-k dielectric layer surrounding the conductive layer of each step.

Kim also discloses using two etch-stop layers while Fang discloses only a single etch-stop layer. Petitioner claims that arguing against combination of Fang and Kim on these grounds "contradict[s]" the '711 patent, because, according to Petitioner, the '711 patent requires the same etch-stop-layer material and thickness for devices with or without the barrier layer. Pet. 66. But Petitioner ignores that the '711 patent specifies a *range* of thickness in its etch-stop layer, and this range can accommodate varying thicknesses based on materials used or structural differences, such as including or excluding the barrier layer.

Kim's *two* etch-stop layers would provide further protection to underlying structures compared to Fang's design, and would also require different etch processes than Fang. *See* Kim Fig. 22A; Campbell2 ¶55. Unlike Kim's multi-layered scheme, Fang discloses a *single* etch-stop layer. *See, e.g.,* Fang Fig. 4. Thus, a POSITA would not be motivated to apply Fang's etch-stop layer thicknesses for a single-etch-stop-layer design to Kim's etch-stop layer in a multi-layered design, much less when Kim does not use the same etch-stop material as Fang.

Finally, Petitioner does not account for differences in etch-stop layer thicknesses based on a gate-stack-on-top design compared to a gate-stack-on-bottom design, instead assuming a POSITA would adapt Fang to Kim in applying the same

etch-stop-layer thicknesses to both. *See* Pet. 32-35, 64-66. But reordering layers requires changes in manufacturing and etch processes, which Petitioner fails to account for. Campbell<sup>2</sup> ¶55. A POSITA would know that etch-stop-layer thicknesses in Fang correspond to a gate-stack-on-bottom structure and would not apply the same to the gate-stack-on-top structure Petitioner argues is present in Kim.

**C. Petitioner fails to establish a reasonable expectation of success in combining Fang's etch-stop layer thicknesses to Kim.**

Petitioner fails to show a POSITA would have a reasonable expectation of success in combining Fang's etch-stop layer thicknesses to Kim.

While Petitioner asserts that there was a reasonable expectation of success because Fang's range of thicknesses "was reasonable, Pet. 65, that argument is a tautology.<sup>9</sup> Petitioner cannot justify a reasonable expectation of success with an expert's conclusory and unsupported opinion that the combination was reasonable.

Similarly, Petitioner's argument supporting a reasonable expectation of success because "both disclosures are directed to similar 3D memory devices with staircase word-line structures" is equally conclusory and unsupported. Pet. 66. Petitioner states both devices use alternating conductive and dielectric layers at each step, an etch-stop layer and insulating layer on the steps, and conductive structures penetrating layers to make contact with the conductive layers of the steps. *Id.* But

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<sup>9</sup> Petitioner makes the same argument for combining Fang with Park. Pet. 101.

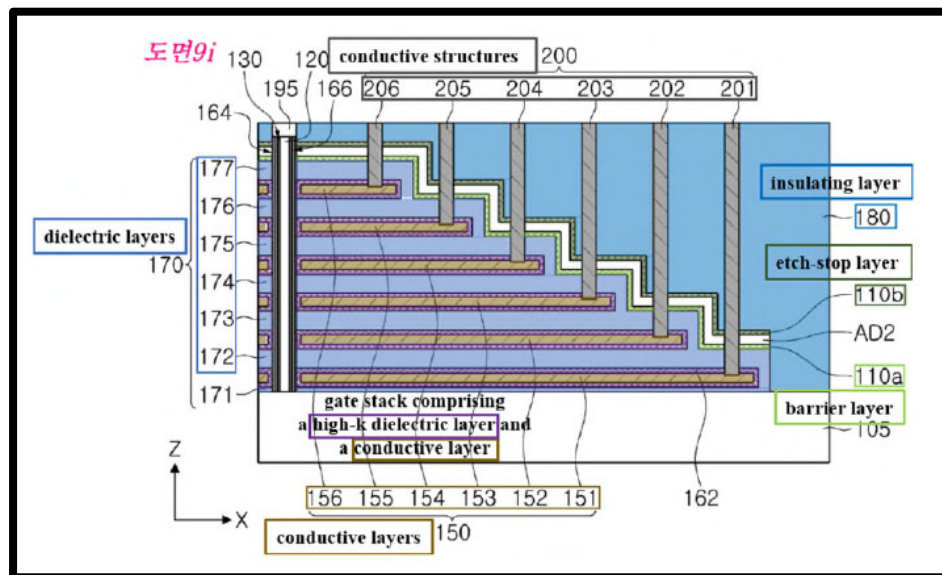
these general characteristics of 3D memory devices are insufficient to provide a motivation to combine or a reasonable expectation of success in doing so. Indeed, Dr. Banerjee's statement that these are "similar 3D memory devices" ignores the many differences discussed previously, including related to materials used and structure of the devices. *See* Ex.1003 ¶¶136-137.

Lastly, Petitioner's argument that "similarities between Kim's and Fang's disclosure regarding the etch-stop layer" would support a reasonable expectation of success is misguided. *See* Pet. 65. Specifically, Petitioner argues that both disclose an etch-stop layer formed of silicon nitride and that both disclose an etch-stop layer having selectivity with respect to the connection region insulating layer through which vertical openings are formed. *Id.* 65-66. But as previously described, Petitioner is flatly wrong that Fang discloses an etch-stop layer formed of silicon nitride—Fang prohibits it. Fang [0020]; Campbell2 ¶51. Relatedly, etch selectivity between the etch-stop layer and the connection region insulating layer above it is dependent on, among other things, the materials used. Campbell2 ¶41. Thus, the mere fact that both references disclose such selectivity provides a POSITA with no expectation of success in their combination, especially where Kim allows for an etch-stop layer material specifically prohibited by Fang (i.e., silicon nitride) and does *not* use the etch-stop material specifically called for in Fang (i.e., carbon-doped silicon nitride).

**V. Ground III: Petitioner Failed to Demonstrate Park in View of a POSITA's Knowledge Renders Obvious Claims 1-6, 8-9, 11-16, and 18-19.**

**A. Park does not disclose “each step compris[ing] a gate stack disposed over a dielectric layer.”**

As discussed above with respect to Kim, each independent claim requires “a plurality of steps” where “each step comprises a gate stack disposed over a dielectric layer.” ’711 patent cl. 1. Park neither discloses this limitation nor renders it obvious. The Petition is clear that it “relies on the embodiment shown in “Figures 5 (perspective view) and 9a-9j (cross-sectional views).” Pet. 31. As can be seen in the figures themselves, these figures show the opposite, gate electrode layers 151-156 disposed below dielectric layers 171-177 in each of the respective steps.



Ex.1006 (“Park”) Fig. 9i (annotated); Campbell2 ¶57.

Petitioner acknowledges the same, admitting that Park’s “figures show the opposite order” required by the claims. Pet. 30; Campbell2 ¶58. Petitioner cites only

paragraph 102 of Park, with no further explanation, to assert that Figure 9 discloses “a gate stack is disposed over a dielectric layer at each step.” Pet. 30-31. But that paragraph only states that “a portion of the top surface of each insulating layer (170) may be exposed by the plurality of pad regions (P1-P6), and, unlike what is shown in FIG. 9a, a portion of the top surface of each sacrificial layer (140) may be exposed in a plurality of pad regions (P1-P6).” Park [0102]. Petitioner fails to explain how a POSITA would understand that disclosure to mean that in each step, the gate stack is disposed over the insulating layer, in contrast to what Figure 9i actually shows. Campbell2 ¶58. At most, paragraph 102 recognizes that both insulating layers 170 and sacrificial layers 140 may be “exposed” in the pad regions P1-P6 (as shown in Figure 9b), rather than just “insulating layer” 170 as shown. *Id.*; Park Figs. 9a, 9b. Petitioner provides no explanation for its assertion.

Thus, as with Kim's Figure 22A, Petitioner's manipulation of Park's Figure 9i is unjustified. Petitioner reversed the order of the insulating layers and gate electrodes of Figure 9i, changing the shading and labels of the original figure to match. Campbell2 ¶¶59-61; *see, e.g.*, Pet. 40; *see supra* Section III.A.

**1. Petitioner improperly relies on multiple embodiments from Park to justify manipulating the figures Park discloses.**

Petitioner again attempts to overcome this lack of disclosure in its only reference by arguing that “other embodiments” disclose the claimed order of layers and that “[a] POSITA would have understood that descriptions of one of Park's

embodiments apply to other embodiments except where the embodiments differ.”

Pet. 31. But applying different embodiments to each other for single reference obviousness requires a motivation to combine. *Stepan*, 868 F.3d at 1346 n.1; *Kotzab*, 217 F.3d at 1370. And similar to Kim, Petitioner has not established any motivation to combine the disparate embodiments of Park to arrive at the manipulated version of Figure 9i, nor a reasonable expectation of successfully doing so. *See supra* Section III.A.

Specifically, a POSITA would not have been motivated to combine Park's Figures 5, 9a-9j embodiment with Park's Figures 4, 8a-8m embodiment as Petitioner suggests. *See* Pet. 31. Petitioner provides no actual reason why a POSITA would have inverted the layers to be the opposite of Figures 5, 9a-9j. Campbell2 ¶¶62-65 (citing Ex.2008 35:12-36:1). At most, Petitioner identifies generic statements that “Park discloses closely related embodiments and teaches that ‘various embodiments may be combined,’ and ‘elements indicated by the same symbols in the drawings are the same elements.’” Pet. 31. Yet these boilerplate statements cannot be used to substitute for a motivation to combine. *See supra* Section III.A. Thus, Petitioner's argument fails for the same reasons addressed above with respect to Kim. *Id.*

While Petitioner asserts that a POSITA “would have understood that descriptions of one of Park's embodiments apply to other embodiments except where the embodiments differ, Pet. 31, that is not consistent with Park's own

specification. Park makes clear that when disclosures apply to different embodiments, it discloses that explicitly. *See, e.g.*, Park [0104] (“Referring to FIG. 9e next, a channel region (130) may be formed. The method of forming a channel region (130) may be ***the same as described with reference to FIG. 8h above.***”) Notably, Park states that the “steps” of the two embodiments—which comprise the gate stack and insulating layers at issue—are different. As Park explains, the Figures 5/9 embodiment includes, for example, “a plurality of etch-stop layers” and “insulating layer (AD2)” on each step that the Figures 4/8 embodiment does not include. *Id.* [0049]. The Figures 4/8 embodiment includes only a single etch-stop layer with no AD2 insulating layer. Petitioner ignores these differences and does not explain why a POSITA would be motivated to combine features from the steps of the Figures 4/8 embodiment with the Figures 5/9 embodiment despite such differences. Campbell2 ¶62.

Beyond failing to provide any motivation to combine Park's distinct embodiments, Petitioner fails to establish that a POSITA would have a reasonable expectation of successfully doing so. *See* Campbell2 ¶¶63-65. To the contrary, a POSITA would understand that moving a functional, gate stack to be over a dielectric layer, when Park teaches the opposite, would require extensive modifications to the manufacturing process and device—all of which Petitioner ignores. *See id.* For example, moving these layers necessitates changes to etch steps

and sequences. *Id.* ¶¶64-65; *see also supra* Section III.A. In addition, the word line contacts would need to also be modified so that they do not penetrate the insulating layer as Park actually discloses. Campbell2 ¶65. Petitioner provides no explanation of how or why a POSITA could actually do so without undue experimentation and with a reasonable expectation of success. Pet. 30 (Park Fig. 9i), 69 (Park “Gate-Stack-on-Top Fig. 9i”). Changing how a vertical contact penetrates the layers of a semiconductor device is not a trivial change, but requires fundamental changes to the manufacturing process and device structure. Campbell2 ¶¶64-65. Petitioner does not address this additional modification or why a POSITA would have a reasonable expectation of successfully achieving it. *Id.* ¶¶63-65. Further, reducing the number of protective layers over the gate stack, which Petitioner’s modification does by putting the gate stack on top of the insulating layer of each step, increases the risk of short-circuits from over-etching. *See id.* ¶83; Ex.2008 48:20-49:8.

**2. Petitioner improperly relies on a POSITA’s knowledge to justify inverting the layers.**

To cure Park’s deficient disclosures, Petitioner also improperly relies on prior art not included in its obviousness combination and a POSITA’s knowledge to gap-fill for missing limitations. Petitioner’s reliance on such prior art is improper. *See supra* Section III.A.2. As discussed above, the rules governing IPRs require Petitioners to identify claim limitations in the prior art relied upon. *Id.* Moreover, general knowledge may only supply a missing claim limitation only when “the

missing limitation in question [is] *unusually simple* and the technology *particularly straightforward*.” *Id.* Not so here. Petitioner relies on the knowledge of a POSITA to satisfy the limitation of claim 1 requiring the gate stack to be disposed over a dielectric layer in view of Park. Petitioner relies on other prior art references not at issue in this proceeding to argue a POSITA would have known about a gate-stack-on-top ordering. Pet. 33-34. But Petitioner fails to show why this ordering is “unusually simple,” and this argument fails for the same reasons discussed above with respect to Kim. *Supra* Section III.A. For example, as discussed above, rearranging the layers of a semiconductor device requires changes in both device design and manufacturing processes, including changes to etching processes and steps. *Supra* Sections III.A, V.A.

**B. Park does not render claims 14 or 15 obvious because Park does not disclose “the etch-stop layer is formed on a side surface and a top surface of each step.”**

Petitioner fails to show claim 14 is obvious over Park.<sup>10</sup> Dependent claim 14 claims “[t]he semiconductor structure of claim 13, wherein the etch-stop layer is formed on a side surface and a top surface of each step.” ’711 patent cl. 14. The Park

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<sup>10</sup> These arguments apply with equal force to claim 15, which depends from 14. Campbell<sup>2</sup> ¶71. Dependent claim 15 claims “thicknesses of the etch-stop layer is the same on the side and top surfaces of each step.”

reference in combination with a POSITA's knowledge fails to render dependent claim 14 obvious for at least the same reasons described above with respect to Ground I, *see supra* Section III.B, but also for two additional reasons, *see* Campbell2 ¶¶66-70. First, Park does not disclose etch-stop layer on the side surface of *each step* of the staircase structure. Second, the etch-stop layer of Park is formed on a side surface and a top surface of either the *insulating layer* "AD2" or the *barrier layer* and not on a side surface and a top surface of each step.

Claim 14 requires an etch-stop layer on the side and top surfaces of "each step," but Park's staircase structure has at least one step with no etch-stop layer on its side, which prevents it from satisfying claim 14. Campbell2 ¶67. Not one of Park's many embodiments, including those relied on by Petitioner, have etch-stop layer on the side surfaces of "*each step*." *Id.* For example, the bottom step of the staircase structures disclosed in the Figures 4/7 and 5/8 embodiments have no etch-stop layer formed on the side or side surface of the step. *Id.* And the Figures 6/10 embodiment has no etch-stop layer on the sides or side surfaces of *any* of the steps of the staircase structure. *Id.* This is plainly observed in the annotated exemplary Figures 4-6 below. Parks remaining embodiments are likewise deficient. *See* Park Figs. 11-13.

## Steps without etch-stop layer on the side

FIG. 4

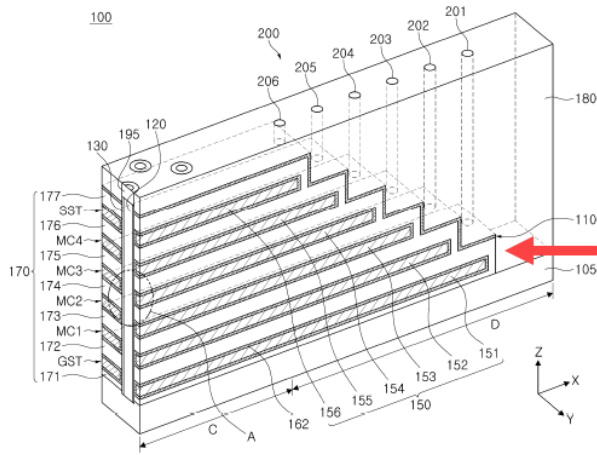


FIG. 5

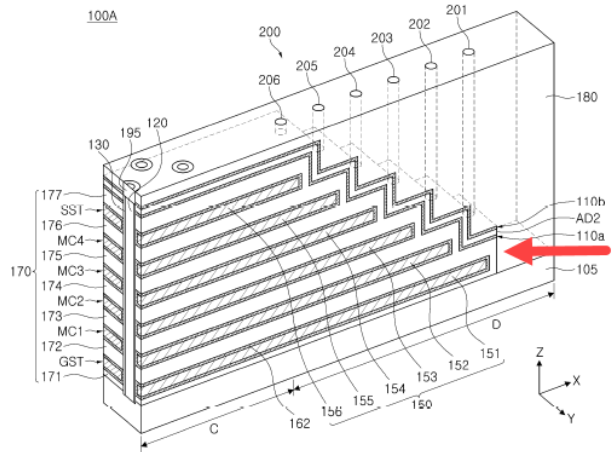
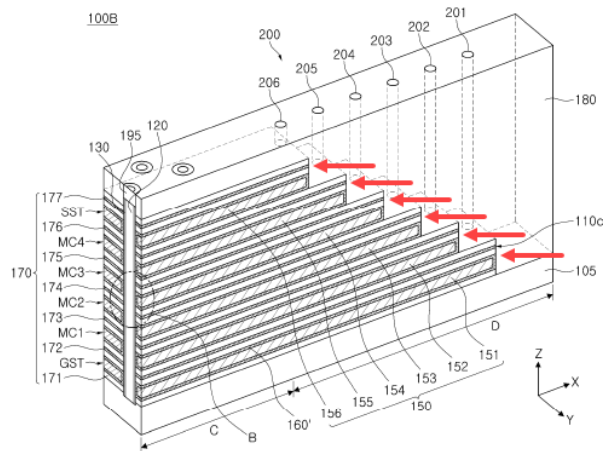
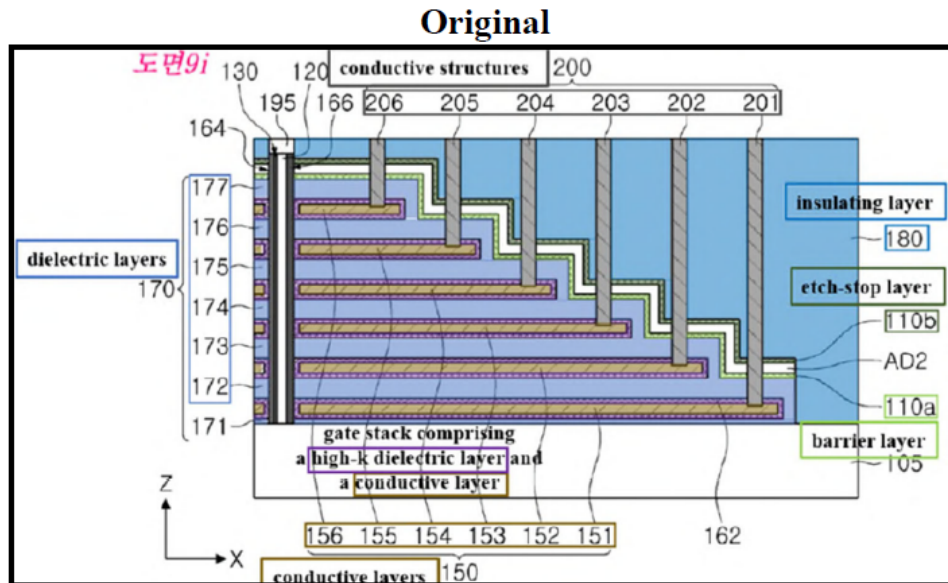


FIG. 6



Moreover, the etch-stop layer of Park is not formed on a side *surface* and a top *surface* of each step, but is instead formed either the *insulating layer* “AD2” or the *barrier layer*. Campbell2 ¶¶68-70. Petitioner maps Park’s “etch-stop layer 110b” to the ’711 patent’s “etch-stop layer,” and Park’s “etch-stop layer 110a” to the ’711 patent’s “barrier layer.” Pet. 74-75; Campbell2 ¶¶68. Further, Park discloses additional insulating layers “AD” and “AD2” physically separating the underlying staircase steps from etch-stop layers 110a, and physically separating etch-stop layer

110a from etch-stop layer 110b, respectively. *See, e.g.*, Park [0049], [0082], [0103]. So, as seen in Figure 9i, the “etch-stop layer (110b)” (i.e., etch-stop layer) is formed on “insulating layer (AD2)” instead of a side surface and top surface of a step of the underlying staircase structure of Park. Park Fig. 9i; *see* Pet. 89; Campbell2 ¶69. To the extent Petitioner argues the AD2 insulation layer of Park is optional, the “etch-stop layer (110b)” of Figure 9i would still be formed on “etch-stop layer (110a)” (i.e., barrier layer) instead of on a side surface and top surface of a step of the underlying staircase structure. *See, e.g.*, Pet. 72 (arguing that Park considers the AD layer optional, although saying nothing of the AD2 layer); Park [0049], [0082], [0103]; Ex.2008 65:22-66:10 (“Q. You’ve labeled layer 110b as the etch-stop layer; is that right? A. Yes. Q. All right. So the etch-stop layer is formed on layer AD2; right? A. In this figure, yes, but if you look at the specifications, Park says that AD2 is this additional dielectric, which is optional. Q. So it would either be formed on AD2 or on the surface of the barrier layer? A. That’s correct.”); Campbell2 ¶69. Thus, Petitioner fails to show Park discloses “the etch-stop layer is formed on a side surface and a top surface of each step.”



Park Fig. 9i (annotated); Campbell2 ¶68.

Petitioner argues this limitation is met because the '711 patent “disclos[es] that ‘on’ something includes both directly and indirectly on that something.” See Pet. 89. But as described above, the '711 patent uses the term “on the surface” or “on a surface” differently to mean “directly on” something. Campbell2 ¶70; see also *supra* Section III.B.

Thus, as seen in at least Figure 9i, Park does not disclose “the etch-stop layer is formed on a side surface and a top surface of each step,” as required by dependent claim 14.

**C. Park does not render claim 15 obvious because Petitioner improperly relies on a POSITA's background knowledge to satisfy a missing limitation.**

Petitioner relies on knowledge of a POSITA to satisfy the limitation of claim 15 requiring the “thicknesses of the etch-stop layer is the same on the side and top

surfaces of each step” in view of Park. Pet. 89-90. Such gap filling is inappropriate for the reasons already discussed above, as is Petitioner's reliance on the Lee reference—a prior art reference not included in its obviousness combination. *Supra* Sections III.A.2, V.A.2. Petitioner argues that a POSITA would understand Park's references to “the thickness of the etch-stop layer” to mean the etch-stop layer has a single thickness and that this understanding is supported by a POSITA's knowledge, because “it was known that an etch-stop layer of uniform thickness on all steps was desirable to achieve a uniform contact-hole depth below the etch-stop layer [and to] prevent[] or reduce[] over-etching or under-etching.” Pet. 89-90. But Petitioner's argument fails for multiple reasons.

First, Petitioner's reliance on references to “the thickness of the etch-stop layer” is a red herring because, as discussed previously, Park does not include any embodiments where there is etch-stop layer on “the side ... surfaces of *each* step,” *See, e.g.*, Park Figs. 4-6, 8-13; Campbell2 ¶¶66-71. Second, Petitioner fails to show why a POSITA would find the limitation of claim 15 “unusually simple” or simply assume a uniform thickness where Park discloses an entirely different method of forming etch-stop layers compared to the '711 patent and other references. Campbell2 ¶71. Specifically, Park uses a sacrificial etch-stop layer that is later removed and replaced with the etch-stop material, in contrast to method disclosed in the '711 patent, as well as Kim and Fang, which forms the etch-stop layer directly

onto the underlying structure and sequentially forms the insulating layer on top of it.

*Id.* This is especially true where Park's method involves forming its etch-stop layer in opening T2—a long, serpentine shape, making it more difficult and costly to achieve uniformity during the deposition process. *Id.* Third, Petitioner's argument that it was known that an etch-stop layer of uniform thickness on all steps was “desirable to achieve a uniform contact-hold depth below the etch-stop layer,” Pet. 89-90, 99-100, is unsupported and explains only why a POSITA may desire a uniform thickness on the *top* surfaces of all steps—it says nothing about why it is desirable to have uniform thickness between the *top and side* surfaces of each step, as required by claim 15. A POSITA's primary concern would be uniform etch-stop layer of sufficient thicknesses across the top of each step, and sufficient thickness on the side of each step to prevent punch through, and not uniform thickness between the etch-stop layer on the top and sides of each step. Campbell2 ¶71. Further, the etch-stop layers on the top and side of the step may not share the same etch-rate, as the horizontal etch-stop layer would be subject to direct ion bombardment where the vertical etch-stop layer would only be subject to indirect ion bombardment. *Id.*

As described herein, 3D semiconductor design and manufacturing, which the employs concepts of chemical, mechanical, and electrical engineering on a microscopic scale, is not “particularly straightforward” technology. *See, e.g.,* Campbell2 ¶¶41, 64, 71. Nor are the missing claim limitations identified by

Petitioner “unusually simple” such that Petitioner may rely on a POSITA’s knowledge to make up for them. *Id.*

**VI. Ground IV: Petitioner Failed to Demonstrate Park in View of Fang Renders Obvious Claims 7, 10, 15, and 17.**

**A. Petitioner fails to establish adequate motivation to combine Park in view of Fang.**

Petitioner fails to establish a motivation to combine the Park and Fang references to render dependent claims 7, 10, 15, and 17 obvious.

Petitioner argues that both Park and Fang are directed to “reducing defects in 3D memory devices resulting from over-etching shallow openings when forming openings for the word-line conductive structures,” and that a POSITA would understand both Park and Fang have the same goal of “improving reliability of a highly integrated 3D memory device by reducing processing complexity, and cost of the manufacturing process.” Pet. 100-01 (cleaned up). For these reasons, Petitioner contends a POSITA would have known that such manufacturing processes “involve many parameters” and would have found Fang’s details useful in places where Park does not specify them. *Id.* But Petitioner ignores important differences in Park and Fang’s materials and designs that would counsel a POSITA against their combination and, contrary to their goal, frustrate the manufacturing process, as discussed further below. *See Campbell* 2 ¶¶71-89; *see Adidas AG*, 963 F.3d at 1359

(Fed. Cir. 2020) (“Fundamental differences between the references are central to [the] motivation to combine inquiry.”).

**1. Petitioner fails to establish a motivation to combine the Park and Fang references to render dependent claim 7 obvious.**

Petitioner fails to establish a motivation to combine the Park and Fang references to render dependent claim 7 obvious. Claim 7 of the '711 patent claims the “top surfaces of the plurality of conductive structures, the insulating layer, and a portion of the etch-stop layer are coplanar.”

Petitioner argues that a POSITA would be motivated to apply Fang's coplanar design of “mak[ing] the top surface of the etch-stop layer coplanar with those of the insulating layer and conductive structure” with Park. Pet. 100-01. Specifically, Petitioner argues that because Park teaches planarizing “to remove unnecessary semiconductor material and insulating material covering the top connection region insulating layer (180),” it would have been obvious that “the materials above the top-surface plane of the etch-stop layer [were] unnecessary.” *Id.* 94-95; *see* Park Fig. 9. Petitioner argues such modification would “simply [be] a matter of design choice,” as “partial or complete removal of the materials ... are both suitable options for design.” Pet. 102-03. However, Petitioner overlooks significant differences in Park's manufacturing sequence and processes that would counsel a POSITA against combining Fang's coplanar design with Park. Campbell2 ¶¶72-82.

- a. **Park's etch-stop-layer formation method, which is meaningfully different than Fang's, would prevent a POSITA from applying Fang's coplanar design in the manner suggested by Petitioner.**

- (1) **Unlike Fang, Park uses etch-stop sacrificial layers to form its etch-stop layer.**

As seen in Figures 9b-9j, Park forms its etch-stop layers using a multi-step process that includes (1) forming insulating layer AD on top of the staircase structure, (2) forming etch-stop sacrificial layers 115a and 115b, separated by insulating layer AD2, on top of insulating layer AD, and (3) forming the connection region insulating layer 180 on top of etch-stop sacrificial layer 115b. Park [0049], [0082]-[0089], [0103]-[0105]; Campbell2 ¶73.

**FIG. 9b**

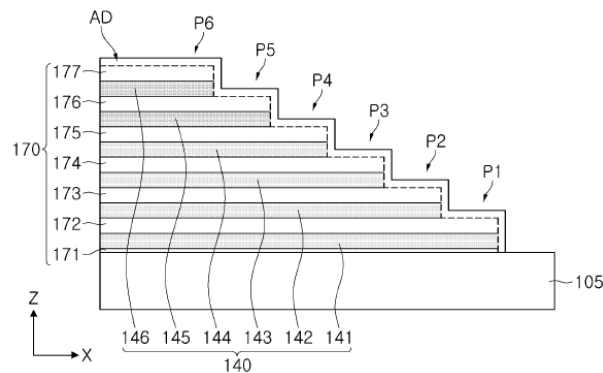
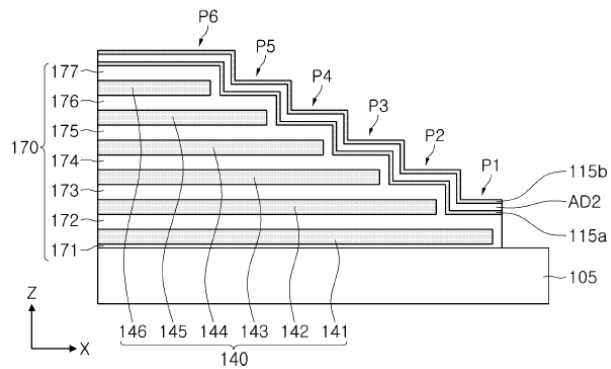
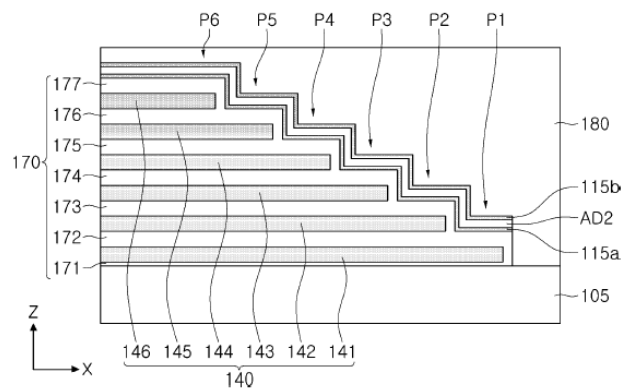
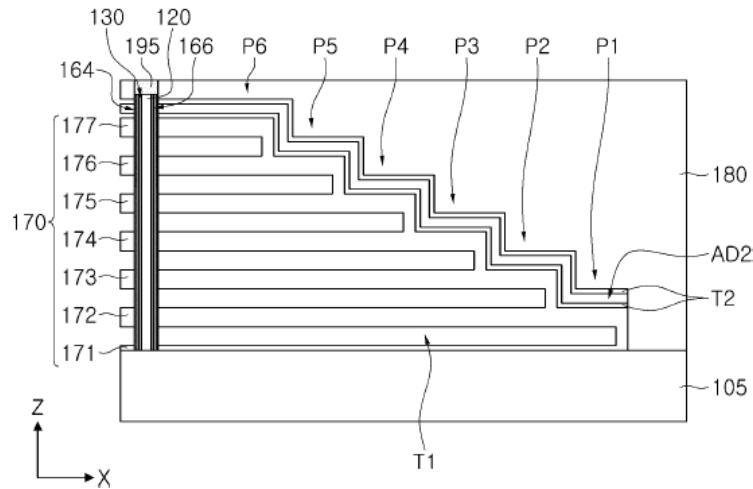
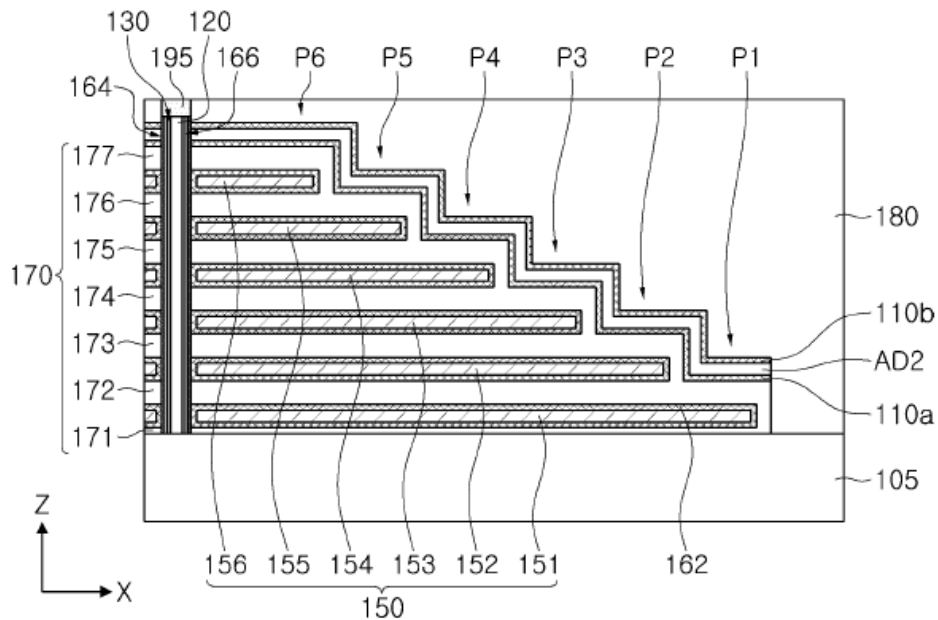


*FIG. 9c**FIG. 9d*

Later in the process, after forming a channel structure 130 and conducting layer 195, Park then (4) removes the etch-stop sacrificial layers to form side openings T2, as seen in Figure 9f. Park [0090], [0104]; Campbell2 ¶74.

**FIG. 9f**

Finally, (5) side openings T2 are then back-filled with the etch-stop material to form etch-stop layers 110a and 110b, as seen in Figure 9g. Park [0091]-[0092], [0105]-[0106]; Campbell2 ¶75.

**FIG. 9g**

By contrast, Fang does not use a sacrificial etch-stop layer and simply forms its etch-stop layer directly on the staircase structure, and then forms the connection region insulating layer on top of it. *See, e.g.*, Fang [0020], Fig. 2; *see also* Campbell2 ¶76.

While Petitioner argues that a POSITA would have a reasonable expectation of successfully combining Park and Fang's etch-stop disclosures based on Dr. Banerjee's declaration, Pet. 100-03 (citing Ex.1003 ¶¶196-203), Dr. Banerjee appears to fundamentally misunderstand Park's design and method of manufacture related to its etch-stop layers, Ex.2008 66:15-71:10, 74:10-76:7. *See* Campbell2 ¶77. For example, Dr. Campbell identifies multiple statements from Dr. Banerjee's deposition testimony demonstrating he incorrectly believes that (1) sacrificial layers 115a and 115b are the same as etch-stop layers 110a and 100b, *see id.* ¶78 (citing Ex.2008 70:20-22, 71:6-10), and (2) only portions of sacrificial layers 115a and 115b are removed during manufacturing, and that they are removed due to etching of the vias for the conductive structures, *see id.* (citing Ex.2008 69:1-11, 70:3-71:4). Both of these opinions are patently incorrect. *Id.* ¶78; Park Figs. 9b-9j, [0100]-[0110]. Further, Dr. Banerjee testified that sacrificial layers 115a and 115b mapped to the '711 patent's barrier layer and etch-stop layer, respectively, in direct contradiction

to the opinion advanced in his declaration.<sup>11</sup> *Compare* Ex.2008 69:8-10, with Ex.1003 ¶150.

(2) **Adapting Fang's coplanar design to Park removes material necessary to Park's manufacturing process.**

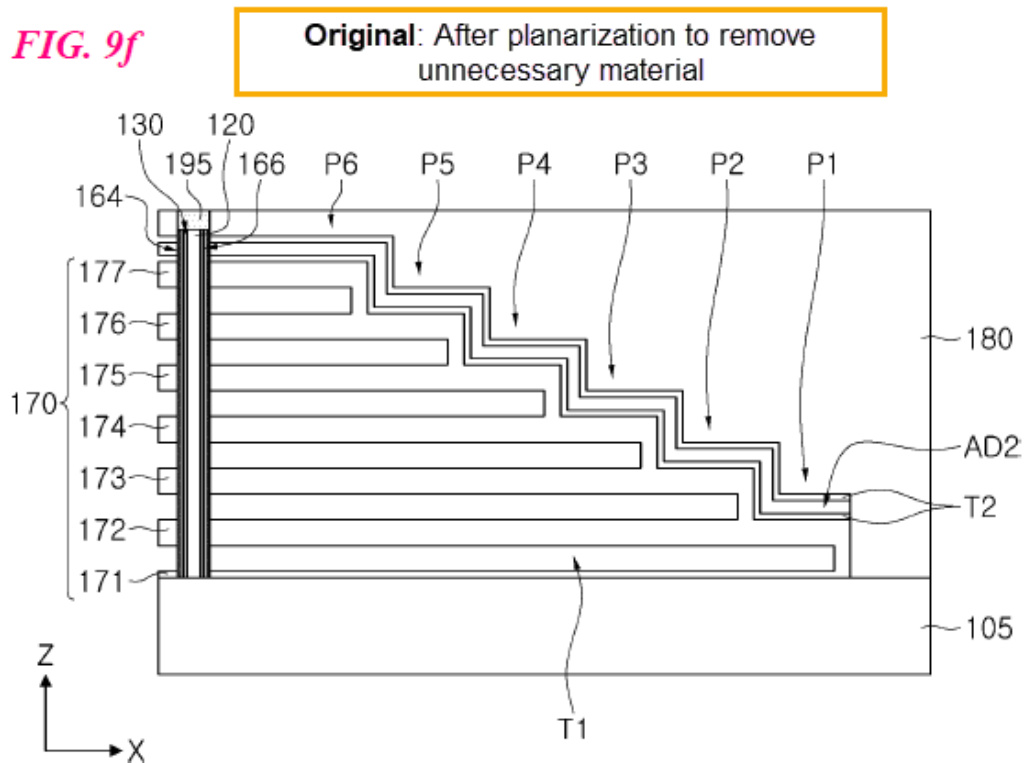
The distinction between Park's and Fang's etch-stop layer design and method of manufacture is significant because adapting Fang's design to Park would remove material necessary to Park's manufacturing process. *See* Campbell2 ¶¶79-82.

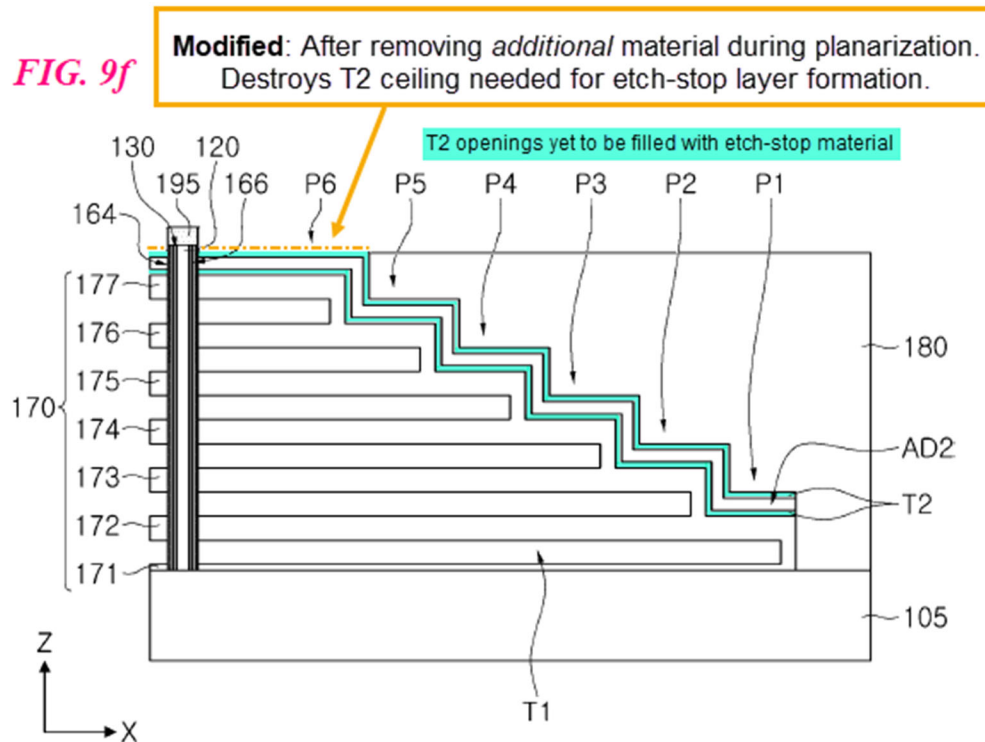
After depositing the connection region insulating layer 180, Park's manufacturing process discloses planarizing "to remove unnecessary semiconductor material and insulating material covering the top connection region insulating layer (180)." Park [0089], [0103]. As Petitioner points out, this occurs "after forming the channel and before depositing the conductive layer 195." Pet. 94-95; *see* Park [0085]-[0089], [0102]-[0106]. Petitioner argues it would have been obvious that the materials above the top-surface plane of the etch-stop layer 110b were "unnecessary," and so these materials could be removed during this planarization process. Pet. 94-95. But Park's planarization to remove unnecessary material occurs *before* the etch-stop sacrificial layer 115b has been removed (i.e., step 4 above) and

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<sup>11</sup> Even after Dr. Banerjee's counsel gave him an opportunity to review relevant portions of Park and correct his testimony, Dr. Banerjee only confirmed his incorrect understanding. *See* Ex.2008 75:13-76:7.

the etch-stop layer 110b has been formed by filling side opening T2 with etch-stop material (i.e., step 5 above). *See* Park [0089]-[0092], [0105]-[0106]; Campbell2 ¶80. Planarizing to remove this additional material, as Petitioner suggests, would actually destroy the top ceiling of side opening T2 required to form the etch-stop layer 110b. *See, e.g.*, Park Figs. 9e-9f; Campbell2 ¶80. For example, compare Figure 9e (pre-planarization) to Modified Figure 9f below (post-planarization and removal of sacrificial etch-stop layer 115b). Campbell2 ¶80.





Indeed, Park shows this material being present and intact *even after* teaching the step of removing unnecessary material via planarizing, further demonstrating that this material is necessary. *See, e.g.,* Park [0089]-[0090], [0104], Figs. 9e-9g. Thus, a POSITA would understand that the additional material above the surface of the etch-stop layer is *not* unnecessary and Fang's coplanar design could not be adapted to Park merely by removing additional material during planarization. Campbell2 ¶¶79-80.

Even if a POSITA were to attempt to avoid this problem by removing the top material via planarization *after* Park's etch-stop layer was formed, it would risk damaging the already-formed channel structure 130 and conductive layer 195. *See, e.g.,* Park Fig. 9g; Campbell2 ¶81. Planarization occurs via chemical mechanical

polishing (CMP), which involves pressing a wafer against a physical, spinning, polishing pad in the presence of a polishing slurry. Campbell2 ¶81. While CMP can be selectively targeted towards specific materials, performing CMP after the formation of the channel structure 130 and conductive layer 195 would necessarily require a less controlled and precise process than removing material via etching processes in order to remove the additional material and planarize the channel structure 130 and conductive layer 195. *Id.* Conducting a CMP process after the channel structure and conductive layer have been formed on the surface of the device could cause damage to those structures. *Id.*; *see, e.g.*, Kim [0105] (“[S]ome of the contact pads 123 may be damaged by chemical and/or physical attacks during the planarization process using the CMP technique.”). Thus, a POSITA would not be motivated to adapt Fang’s coplanar design by adding an additional planarization step to Park’s manufacturing process in this manner.

**b. Petitioner fails to establish a reasonable expectation of success in combining Fang’s coplanar design to Park.**

Petitioner fails to show a POSITA would have a reasonable expectation of success in combining Fang’s coplanar design to Park.

Petitioner’s argument that a POSITA would have a reasonable expectation of success because “the modification simply extends Park’s existing planarization process to remove a greater thickness of the same, unnecessary, materials” overlooks critical differences in Park’s manufacturing process. *See* Pet. 103. As discussed

above, Park forms the etch-stop layer using a sacrificial etch-stop layer that, after planarization, is removed and replaced with the etch-stop material. *Supra* Section VI.A.1. Simply “removing a greater thickness” of the connection region insulating material during Park’s planarizing process, as Petitioner and its expert suggest, would destroy the ceiling of the T2 opening necessary for forming Park’s etch-stop layer. Campbell<sup>2</sup> ¶80. And adding an additional planarization step after the etch-stop layer is formed would risk damaging the structure. *Id.* ¶81. Thus, a POSITA would not have a reasonable expectation of success in applying Fang’s coplanar design to Park. *Id.* ¶82.

**2. Petitioner fails to establish a motivation to combine the Park and Fang references to render dependent claims 10 and 17 obvious.**

Petitioner fails to establish a motivation to combine the Park and Fang references to render dependent claims 10 and 17 obvious. Claims 10 and 17 of the ’711 patent claim “a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.”

Petitioner fails to establish a motivation to combine the Park and Fang references for at least the same reasons it fails as to the Kim and Fang combination. *See supra* Section IV. Petitioner argues that a POSITA would be motivated to apply Fang’s disclosure of etch-stop-layer thickness on Park’s staircase structure primarily because Park does not itself disclose an etch-stop-layer thickness and Fang does.

Pet. 100-02. But again, this is an inadequate motivation to combine and ignores material differences in Park's materials and design that would counsel a POSITA against adapting Fang's etch-stop layer thicknesses to Park.

For example, like Kim, Park never uses a carbon-doped silicon nitride etch-stop material and Park does not use a combination of carbon-doped silicon nitride etch-stop material and a silicon nitride sacrificial layer. *See supra* Section IV.A. Also like Kim, Park includes structural differences that counsel against combination, as described below.

**a. Structural differences between Fang and Park counsel a POSITA against applying Fang's etch-stop layer thicknesses to Park.**

Park has many structural differences from Fang that would counsel a POSITA against using Fang's etch-stop-layer thicknesses with Park.

A POSITA would understand that the purpose of the etch-stop layer is to protect underlying structures during the etching process, making certain structural differences, such as the number of protective layers used, material to determining the necessary thickness of an etch-stop layer. *See, e.g.*, Fang [0026] (“[U]sing the etch stop material 130 according to embodiments of the disclosure prevents or reduces punch through into the conductive materials 140.”); Park [0051] (The “process of forming a vertical opening ... may be temporarily stopped or slowed down by a plurality of etch-stop layers (110a, 110b), thereby preventing defects

caused by penetration of the top gate electrode layer (156).”); Campbell2 ¶83. Further, a POSITA would also understand that each additional layer requires an additional etch process to form vias for the conductive structures of each step. *See* Campbell2 ¶83; Ex.2008 43:5-48:1.

Similar to Kim, Park discloses using a high-k dielectric layer around the conductive layer of each step while Fang does not. *See, e.g.*, Park [0063], Figs. 7a, 9j. A POSITA would know that use of a high-k dielectric layer surrounding the conductive layer provides added protection to the gate stack layer and affects the necessary etch processes, which can affect the necessary thickness of the etch-stop layer. Campbell2 ¶84. Thus, a POSITA would not be motivated to apply Fang's etch-stop layer thicknesses, which are for designs without high-k dielectrics, to Park's design using a high-k dielectric layer surrounding the conductive layer of each step.

Park also discloses using multiple etch-stop and protective layers above the staircase structure while Fang discloses only a single etch-stop layer. *See, e.g.*, Park Figs. 9b-9g; Fang Fig. 4. Petitioner concedes it relies on an embodiment from Park that “discloses an additional barrier layer,” but Petitioner argues this is irrelevant because “Park makes no distinction regarding thickness of its etch-stop layer based on the number of such layers in the embodiment.” Pet. 102. But a POSITA would not expect Park to provide such information where Park does not specify *any* etch-

stop layer thicknesses. Campbell2 ¶85. Park includes *two* etch-stop layers, and *two* additional insulating layers that would provide further protection to underlying structures, and also require different etch processes compared to Fang's design. *See* Park [0103] (identifying insulating layer (AD) and insulating layer (AD2)), [0103]-[0105], Fig. 9g; Campbell2 ¶85. Unlike Park's multi-layered design, Fang discloses a *single* etch-stop layer formed directly on the insulating and sacrificial layers of the underlying staircase step. *See, e.g.,* Fang Fig. 4; *see also* Campbell2 ¶85. Thus, a POSITA would not be motivated to apply Fang's etch-stop-layer thicknesses for a single-etch-stop-layer design to Park's etch-stop layer in a multi-layered-etch-stop and multi-protective-layer design, much less when Park does not use the same etch-stop material as Fang.

Finally, Petitioner does not account for differences in etch-stop layer thicknesses based on a gate-stack-on-top design compared to a gate-stack-on-bottom design, instead assuming a POSITA would adapt Fang to Park in applying the same etch-stop-layer thicknesses to both. *See* Pet. 66-67, 100-03; Campbell2 ¶85. But, as discussed previously, reordering layers requires changes in both device design and manufacturing processes, including etch processes and steps, which Petitioner fails to account for. *See supra* Section III.A.2. A POSITA would know that etch-stop-layer thicknesses in Fang correspond to a gate-stack-on-bottom structure and would

not apply the same to the gate-stack-on-top structure Petitioner argues is present in Park.

**b. Petitioner fails to establish a reasonable expectation of success in combining Fang's etch-stop layer thicknesses with Park.**

Petitioner fails to show a POSITA would have a reasonable expectation of success in combining Fang's etch-stop layer thicknesses with Park. *See* Campbell2 ¶¶83-86

Petitioner argues a reasonable expectation of success in applying Fang's etch-stop layer thicknesses to Park for the same reasons as to Kim—namely, because Fang's etch-stop layer thickness is purportedly “reasonable,” because of purported similarities between Park and Fang's etch-stop layer disclosures, and because of general characteristics of 3D memory devices shared by both Park and Fang. Pet. 101-02. However, the same reasons why a POSITA would not have a reasonable expectation of success in applying Fang's etch-stop layer thicknesses to Kim apply to Park as well. *See supra* Section IV.

**3. Petitioner fails to establish a motivation to combine the Park and Fang references, or a reasonable expectation of success in doing so, to render dependent claim 15 obvious.**

Petitioner fails to establish a motivation to combine the Park and Fang references to render dependent claim 15 obvious. Claim 15 of the '711 patent claims

“wherein thicknesses of the etch-stop layer is the same on the side and top surfaces of each step.”

Petitioner argues that a POSITA would be motivated to apply Fang's teaching that “[t]he thicknesses of the etch stop material 130 on the stairs 125 may be substantially uniform” to Park because a POSITA would know that “an etch-stop layer of uniform thickness on all steps was desirable.” Pet. 99-100. And that a POSITA would have a reasonable expectation of success because a uniform thickness “is consistent” with Park's references to “the thickness of the etch-stop layer.” *Id.* However, a POSITA would not be motivated to combine Fang's teachings regarding etch-stop layer thickness to Park, nor do so with a reasonable expectation of success, for at least the reasons described above for dependent claims 10 and 17. *See supra* Section VI.A.2; Campbell2 ¶¶88-89.

A POSITA would also not be motivated to combine Fang's teachings regarding uniform etch-stop layer thickness to Park, nor do so with a reasonable expectation of success, for the reasons described above in Section V.C discussing Park's deficient disclosures on this point. First, Fang's teaching is inconsistent with Park's disclosures because Park does not disclose etch-stop layer on the side surface of *each step* of the staircase structure. *See supra* Section V.C; Campbell2 ¶87. Second, Park discloses an entirely different method of forming etch-stop layers compared to Fang. Fang forms its etch-stop layer directly on the staircase structure,

but Park first forms an etch-stop sacrificial layer that must later be removed to form a cavity where the etch-stop material can be filled in. *See supra* Section V.C; Campbell2 ¶87. Thus, Park's method makes achieving the claimed uniformity especially difficult and costly because of the long, narrow, serpentine-shaped cavity that must be filled with etch-stop material. *See supra* Section V.C; Campbell2 ¶87. Third, Petitioner's claims that a POSITA would find it "desirable" to achieve uniformity in the etch-stop layer thickness between the top and side surfaces of each step is unsupported. At most, Petitioner explains why uniform thickness between each top surface is desirable, namely "to achieve a uniform contact-hole depth below the etch-stop layer." *See* Pet. 89-90, 99-100; Ex.1003 ¶177; *see supra* Section V.C; Campbell2 ¶87. But this says nothing about why uniformity in etch-top layer thickness between top and side surfaces is desirable. *See* Campbell2 ¶¶71, 87. A POSITA's primary concern would be uniformity in etch-stop layer thicknesses across the top of each step and sufficient thickness on the side of each step to prevent punch through, and not uniformity between the thickness on the top and sides of each step. *Id.* Especially where their etch rates may differ. *See id.*

Thus, a POSITA would not be motivated to combine Fang's teachings regarding uniform etch-stop layer thicknesses to Park, nor have a reasonable expectation of success in doing so.

## VII. Conclusion

For the reasons set forth above, the Board should deny the Petition for *Inter Partes* Review.

Respectfully submitted,

Dated: August 26, 2025

By: / Alex Grabowski /

Alex Grabowski (Reg. No. 74,009)  
alex.grabowski@lw.com  
Latham & Watkins LLP  
330 North Wabash Avenue, Ste. 2800  
Chicago, IL 60611  
Telephone: 312.876.7700  
Fax: 312.993.9767

*Counsel for Patent Owner  
Yangtze Memory Technologies  
Company, Ltd.*

**CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24**

I hereby certify that this Patent Owner's Response complies with the word count limitation of 37 C.F.R. § 42.24(b)(2) because the Patent Owner's Response contains a total of 13,978 words, which is the sum of 13,769 words calculated by Microsoft Word's word-count feature and 209 words hand counted in the figures. This total excludes the cover page, signature block, and the parts of the Patent Owner's Response exempted by 37 C.F.R. § 42.24(b)(2).

By: / Alex Grabowski /

Alex Grabowski (Reg. No. 74,009)  
alex.grabowski@lw.com  
Latham & Watkins LLP  
330 North Wabash Avenue, Ste. 2800  
Chicago, IL 60611  
Telephone: 312.876.7700  
Fax: 312.993.9767

*Counsel for Patent Owner  
Yangtze Memory Technologies  
Company, Ltd.*

**CERTIFICATE OF SERVICE**

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 26th day of August, 2025, a true and correct copy of the foregoing **Patent Owner's Response and all Exhibits** were served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

Jeremy Jason Lang (Reg. No. 73,604)  
Travis Jensen (Reg. No. 60,087)  
Jared Bobrow (*Pro Hac Vice* to be submitted)  
Orrick, Herrington & Sutcliffe LLP  
1000 Marsh Road  
Menlo Park, CA 94025-1015  
T: 650-614-7400  
F: 650-614-7401  
jlang@orrick.com  
tjensen@orrick.com  
jbobrow@orrick.com  
PTABDocketJJL2@orrick.com  
P52PTABDocket@orrick.com  
PTABDocketJ3B3@orrick.com  
PTABDocketJ1H1@orrick.com  
MICRON-YMTC\_ohs@orrick.com

Johannes Hsu (Reg. No. 74,689)  
Orrick, Herrington & Sutcliffe LLP  
2050 Main Street, Suite 1100  
Irvine, CA 92614-8255  
T: 949-567-6700  
F: 949-567-6710  
johanneshsu@orrick.com

By: / Alex Grabowski /

Alex Grabowski (Reg. No. 74,009)  
alex.grabowski@lw.com  
Latham & Watkins LLP  
330 North Wabash Avenue, Ste. 2800  
Chicago, IL 60611  
Telephone: 312.876.7700  
Fax: 312.993.9767

*Counsel for Patent Owner  
Yangtze Memory Technologies  
Company, Ltd.*