UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v. : Case IPR2025-00117

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner. : U.S. Patent No. 10,672,711

Deposition of SANJAY BANERJEE, Ph. D.

Conducted Virtually

Wednesday, August 13, 2025

6:58 a.m. PST

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Pages: 1 - 79

Reported by: Dwayne W. Lewis, Jr., CA-CSR 14636

YMTC
Exhibit 2008
Micron v. YMTC
IPR2025-00117
Ex. 2008-001

Deposition of SANJAY BANERJEE, Ph. D., conducted virtually.

Pursuant to notice, before Dwayne W. Lewis, Jr. CA-CSR 14636.

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C O N T E N T S

WITNESSES PAGE
CALLED BY THE PATENT OWNER:
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THEREUPON, the following proceedings were had and taken, commencing at 06:58 AM:

THE TECHNICIAN: Thank you to everyone for attending this proceeding remotely which we anticipate will run smoothly. Please remember to speak slowly and do your best not to talk over one another. Please be aware that we are recording this proceeding for backup purposes. Any off-the-record discussions should be had away from the computer. Please remember to mute your mic for those conversations.

Please have your video enabled to help the reporter identify who is speaking. If you are unable to connect with video and are connecting via phone, please identify yourself each time before speaking. We will provide a complementary unedited recording of this deposition with the purchase of a transcript. I apologize in advance for any technical related interruptions. Thank you.

SANJAY BANERJEE, PH. D. , called as a witness by the Patent Owner, having been first duly sworn testified as follows:

DIRECT EXAMINATION

BY MR. GRABOWSKI:

Q. All right. Good morning, Dr. Banerjee. Am I saying that correctly?

A. Banerjee, yes.

Q. Banerjee, perfect. My name is Alex Grabowski. So thank you first off for your time today. If you wouldn't mind just stating your name and business address for the record.

A. Sanjay Banerjee, University of Texas at Austin.

Q. All right. And have you ever been deposed before?

A. Yes.

Q. About how many times?

A. Like 20 to 30 times.

Q. All right. Well, then I'm sure you've heard the ground rules speech before, but I'm going to go over them again quickly just to act as a refresher. So I'm going to give you questions and you'll give me answers, is that all right?

A. Yes.

Q. I'd appreciate it if you give me verbal answers only, not nodding or shaking your head so that we can get it down for the court reporter, is that all right?

A. Yes.

Q. All right. As the court reporter [sic] mentioned, since Zoom in particular doesn't allow multiple people to talk, let's try not to talk over each other. I will try to do the same for you. If you don't understand anything, please ask for clarification, otherwise I'll assume you understood my question, is that all right?

A. Yes.

Q. All right. You understand your lawyer may make objections from time to time, but unless he instructs you not to answer, you're still going to answer the question; right?

A. Yes.

Q. Perfect. We'll have an opportunity to take breaks. We can take a break whenever you like, the only thing I ask is that if there's a question pending, will you answer that before we take the break; is that okay?

A. Yes.

Q. All right. And then a couple questions I have to ask everyone, are you taking any medication that might interfere with your ability to give complete and accurate testimony today?

A. No.

Q. Is there any other reason you can't give complete and accurate testimony today?

A. No.

Q. All right. Because this is a remote deposition I have just a few other questions about your setup. Is there anybody else in the room with you?

A. No.

Q. Okay. Do you have any notes or documents in front of you?

A. I have a clean copy of my declaration and the 711 patent on my desk, and on my computer I have open electronic versions of my declaration, the Kim patent and the Park patent.

Q. Perfect. And are there any annotations or notes on the electronic copies?

A. No.

Q. Other than the documents you mentioned, are there any other applications open on your computer?
A. I guess Zoom.
Q. Fair enough.
A. E-mail -- e-mail. I can close Outlook if you want me to.
Q. If you don't mind, yeah, I'd appreciate it.
A. Okay.
Q. Perfect. Any other applications open?
A. No.
Q. All right.
A. I guess adobe Acrobat is open because I have those files open.
Q. Yeah, fair enough. That will be useful, I think you can keep that one. You mentioned about 20 or 30 prior depositions. Were you acting as an expert witness in all of those?
A. Yes.
Q. Were they all patent cases?
A. Yes.
Q. All right. What did you to to prepare for your deposition today?

A. I reviewed my declaration, the 711 patent and some of the cited prior art such as Kim, Park, Fang and others.

Q. Did you review any materials that weren't cited in your declaration?

A. I don't think so, not in the past few days at least.

Q. Did you review any materials that weren't cited in your declaration to prepare for this deposition prior to the past few days?

A. No.

Q. Okay.

A. No.

Q. Did you speak to anyone to prepare for your deposition today?

A. I spoke briefly with my counsel yesterday and on Friday, which would be August 8th.

Q. And who exactly did you meet with?

A. Mr. Hsu, Johannes Hsu.

Q. Anyone else?

A. No.

Q. About how long was the meeting yesterday?

A. About an hour.

Q. And how long was the meeting on the 8th?

A. I think half an hour, or maybe an hour at most.

Q. Did you speak to any non-attorneys to prepare for this deposition?

A. No.

Q. Do you recall when you were first contacted about this case?

A. By this case, are you referring only to the 711 patent? Because there's a lot of -- lots of --

Q. Fair enough. We'll start with the 711 patent and then maybe go back from there.

A. I don't recall. I've been handling so many patents that it's all in a haze, but probably around a year. I could be wrong.

Q. All right. And then I guess more generally do you recall when you were first contacted about this dispute between Micron and YMTC?

A. Once again, I don't recall exactly, but I think over a year back.

(Patent Owner's Exhibit 1003 was marked for

identification.)

Q. Now, speaking, again, specifically about this -- this patent and this declaration that we're here today to deal with, you have in front of you -- you mentioned the declaration. I just want to make sure we're talking about the same thing. That's Exhibit 1003 for U.S. patent number 10,672,711; is that right?

A. Yes.

Q. All right. About how long did you spend preparing this declaration, Exhibit No. 1003?

A. So this is my declaration and the opinions are mine, but I worked collaboratively with Counsel preparing it as I think is good in most cases, and I provided technical feedback, counsel gave me legal guidelines. So once again, speaking from memory, probably, I don't know, 20, 30 hours perhaps, or maybe more. I don't know.

Q. And who provided the references you cite in your declaration?

A. I don't recall exactly, because typically what happens is in various cases the Counsels provide some and they ask me to do some prior art search in some

cases, so I provide some. I think in this case the references are provided by Counsel. I may have done some searches for some of the prior art, but the key ones I think Counsel provided.

(Patent Owner's Exhibit 1005 was marked for identification.)

Q. All right. And when you say Counsel provided the key ones, you mentioned the Kim reference earlier, that's Exhibit 1005; correct?

A. Yes.

Q. All right. And did Counsel provide Exhibit 1005 to you?

A. Yes.

(Patent Owner's Exhibit 1006 was marked for identification.)

Q. All right. And you mentioned the Park reference, that's Exhibit 1006; correct?

A. Yes.

Q. Did Counsel provide the Park reference to you?

A. Yes.

(Patent Owner's Exhibit 1007 was marked for identification.)

Q. And the other reference used in some of your grounds is the Fang reference, Exhibit 1007; is that right?

A. Yes.

Q. Did Counsel provide the Fang reference to you?

A. Yes.

Q. And I appreciate there are other references cited in your declaration, but am I correct that those are the only three references that form parts of the actual obviousness combination for any of your grounds?

A. Those are the primary ones, though we do cite a few others like the Chen patent for example -- in passing, you know, Chen and Exhibit 1015 I think we refer to in passing, but 1005, 6 and 7 are the primary 103 combinations.

Q. And when you say they are the primary 103 combinations, like I said, I appreciate you cite other references. Do you have an understanding of what it means to be part of an obvious combination for purposes of patent law?

A. Well, I'm not a lawyer, so my opinions about what is an obviousness argument, I've given my

declaration, but on a very high level. Based on layman's terms, I think if all the claim elements are found in a single reference that's anticipation if you had to combine various pieces of prior art I think that's obviousness, but that's a nonlawyer understanding.

Q. Understood, and I --

A. And a --

Q. Excuse me. I didn't mean to cut you off.

A. The precise understanding that I applied is described in my declaration.

Q. And I just want to make sure we're on the same page, that you cite other references like Chen for instance, but that isn't part of the actual obviousness combination in any of the grounds; correct?

A. No, I guess not.

Q. Okay. And then the only three references that make up any of the obviousness combinations in any of the grounds are Park, Fang and Kim; correct?

A. And knowledge of the procedure.

Q. Understood. All right. Did you speak to any non-lawyers about your declaration?

A. No.

MR. GRABOWSKI: All right. Could we pull up Exhibit 1003, Dr. Banerjee's declaration, please.

THE TECHNICIAN: Stand by. Okay. I've placed it in the chat. I'm about to pull it up on screen.

BY MR. GRABOWSKI:

Q. All right. Thank you very much. And just for the record, Dr. Banerjee, this is Exhibit 1003, the declaration we've been talking about so far, yes?

A. Yes.

Q. All right. And this declaration contains your complete opinions on the 711 patent?

A. Yes.

Q. Are there any mistakes you're aware of in this declaration as you sit here today?

A. Yes. I noticed a few typos.

Q. Typos. All right. Are there any you need to correct or they just --

A. A couple of the typos involved when we're comparing Kim with Fang and Park with Fang, Fang has one etch-top layer, while both Kim and Park have two. I accidentally flipped those two in a couple of places,

and then in another location where we're talking with the range of thicknesses, 10 through 1000 nanometers, I accidentally said that's three orders of magnitude. It should be two orders of magnitude.

Q. All right. Let's go through it and find those spots just so we are all talking about the same thing. Would you mind walking me through the declaration and pointing out exactly what you're talking about?

A. Sure. Is it okay if I pull up my version on my computer?

Q. Yeah, that -- that's fine. Whatever's convenient for you.

A. So the error about three orders of magnitude is in paragraph 129 where we say the cited range spanning three orders of magnitude lacks criticality. It should read two orders of magnitude.

Q. Understood.

A. Okay. And then -- okay. So in paragraph 131 I state Fang has two etch-stop layers and Kim has one. Should be the other way around, Kim has two etch-stop layers while Fang has one. And then in paragraph 190 I state Fang has 2 etch-stop layers while Park has one.

Once again, they are flipped. It should be Park has two etch-stop layers but Fang has one. I think those are the typos that I...

Q. All right. Thank you for that. Are there any other mistakes you're aware of in your declaration?

A. Not that I can think of.

Q. Okay. All right. We touched on this briefly already, but you have a layman's understanding of what obviousness means in the context of patent law; right?

A. Yes.

Q. And what is that understanding?

A. Let me refer to my declaration and be precise. I'm instructed by Counsel to consider the following factors: The scope and content of the prior art, the difference or differences between each claim of the patent and the prior art and the level of ordinary skill in the art at the time the patent was filed. And then one should also consider secondary considerations, art objective indicia of non-obviousness.

And then to make these evaluations, one has to determine whether the art is from the same field of endeavor regardless of the problem addressed. If the

reference is not within the field of the patentee's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the patentee is involved. The field of endeavor is not limited to the specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field.

I can keep reading, but my understanding is described in paragraphs 27, 28, 29, 30, 31, 32, 33, 34, 36, 37, 38.

Q. Just for completeness I think you skipped 35 there. Was that intentional?

A. Yes. I meant 35 also. Thank you.

Q. And then your opinion relates to four grounds of invalidity; is that correct?

A. Yes.

Q. Is it your understanding that all four of those grounds are based on obviousness?

A. Yes.

Q. Okay. And you've heard of anticipation in the context of patent law; right?

A. Yes.

Q. You don't offer any opinion in your declaration that any claims of the 711 patent are anticipated; right?

A. That's correct.

MR. GRABOWSKI: All right. Could we go to paragraph five of your declaration? I'd like to talk a little bit about your background. You received a PhD in electrical engineering from the University of Illinois; correct?

A. Yes.

Q. Excellent school, most of my family went there.

A. Really?

Q. And then you went to work at Texas Instruments; correct?

A. Yes.

Q. While you were at Texas Instruments, you worked on 3D (DRAM) cells; do I have that right?

A. Yes.

Q. And (DRAM) stands for Dynamic Random Access Memory?

A. Yes.

Q. And (DRAM) is different from (NAND) memory; correct?

A. They are both semiconductor memories, and there's a certain degree of commonality between different types of memory as in these memory cells are organized in rows and columns that are addressed by row decoders, column decoders. So the peripheral circuitry has a lot of commonality but the memory cells themselves are different. A (DRAM) is a volatile memory involving a storage capacitor and a pass transistor, while a flash memory is a non-volatile memory.

Q. And you mentioned flash memory. NAND is a type of flash memory; right?

A. Yes.

Q. There are other type of flash memory as well; correct?

A. Yes.

Q. All right. And then, looking now at paragraph six, it mentioned you worked on developing a replacement for MOSFETs; correct?

A. Yes.

Q. All right. And MOSFETs are also different

from NAND memory; correct?

A. MOSFETs are the switches that are used in most of the circuitry, so NAND memory also involves the use of MOSFETs.

Q. So a MOSFET is one element of NAND memory; is that fair to say?

A. MOSFETs are used in the peripheral circuits, that is the row decoders and the column decoders and sense amplifiers, and then the memory cells themselves, while they are not exactly a MOSFET, there's commonalities in the sense that they have a source and a drain and a channel and the flow of carriers to the channel is controlled by a control gate.

But in a flash memory you have an additional floating gate or a storage medium. I'm not claiming that flash memory is exactly like a MOSFET, but there's a fair degree of overlap.

Q. All right. Looking at paragraph eight now, you mention 40 years of experience in the field and then you go on to talk about a few projects, 3D (DRAM) cells, MOSFETs, flash memory and CMOS transistors. Do you see that?

A. Yes.

Q. Did any of those projects specifically involve 3D NAND memory cells?

A. I work on 3D flash type devices, but I've worked on individual memory cells. In academia we don't have the luxury of making complete chips, but the physics that we study is directly applicable to products.

So if you are asking if I made a string of these memory cells as in a NAND flash, I did not, but I did make memory cells themselves which are applicable to NAND flash, and furthermore in the course -- during the research you have to be aware of the current state of the art, so I've extensively studied what's been published in NAND flash by industry, talked to industry experts, I've been funded by industry in this area.

MR. GRABOWSKI: All right. You'll probably want to keep the physical one up, but we can take Exhibit 1003 off the screen. Can we put Kim Exhibit 1005 up, please.

THE TECHNICIAN: Stand by.

BY MR. GRABOWSKI:

Q. All right. And Doctor, this is Exhibit 1005, the Kim reference that you relied on in forming your opinions in this case; correct?

A. That's one of -- that's the main Kim reference. There's also a secondary Kim reference.

Q. Fair enough. This is -- this is Exhibit 1005, the Kim reference that forms part of your obviousness combinations for grounds one and two; is that right?

A. Yes.

MR. GRABOWSKI: Okay. I'd like to go to paragraph 27 if we could, please.

THE TECHNICIAN: Counsel, do you have a PDF page that I could go to?

MR. GRABOWSKI: Yeah. It's PDF page 57.

THE TECHNICIAN: Thank you.

BY MR. GRABOWSKI:

Q. Can you see that all right, Doctor?

A. Yes.

Q. Paragraph 27 of Kim is discussing the purported benefits of its alleged invention; is that right?

A. It's talking about some of the benefits, yes.

Q. And it explains specifically that its inventive concept may reduce or prevent damage from occurring on contact paths on the semiconductor patterns in the cell array region as a result of planarizing the interlayer dielectric; right?

A. I see that.

Q. And paragraph 27 of Kim doesn't discuss any damage to the device other than damage to the contact paths in the cell array region; right?

A. Could you repeat that question, please?

Q. Sure. Paragraph 27 of Kim doesn't discuss any damage to the device other than damage to the contact paths in the cell array region; right?

A. I think I would respectfully disagree a little bit, because if we read the last sentence, it says in the process of forming contact plugs and interconnection lines, can thereby be performed with a sufficient process margin. I've read the whole patent, evaluated this precisely, but when one is talking about the interconnection lines, that could also refer to another word lines which extend into the staircase region for example, the bit lines, which go into the periphery.

And when you're talking about making these with a sufficient process margin, I think there's an element of disclosure of preventing defects and those things also, so that the chip functions properly. Having said that, under the primary discussion in this particular paragraph, it is in the cell array region.

Q. All right. Can I just try to understand your answer a little more? I think you said you'd have to read the whole patent a little more to understand what contact plugs and interconnection lines mean, did I understand that correctly?

A. No. I said I did not -- I didn't -- I don't think I expressed any opinion specifically about this paragraph in my declaration. If I did, kindly point to that, but I think your question was whether paragraph 27 only talks about damage in the cell array region.

And my answer is yeah, it does, but there's a caveat in the sense that the last sentence also mentions interconnection lines, and those very often go from the cell array region into the peripheral region, so I think there's an implication of preventing damage in those regions also, but I've not opined on these aspects

specifically in my report.

Q. All right. Do you have an understanding of what Kim means by the cell array region?

A. Yes.

Q. What is your understanding of the cell array region as Kim uses that term?

A. So as I was telling you a few minutes earlier, there's a lot of commonality between different types of memory. So we have a central section typically where we have these two dimensional arrays of memory cells. This could be in this case vertical NAND memory strings. It could be a DRAM cell, it could be an SRAM cell, but that surrounding this cell array with the memory cells themselves are located, we have peripheral circuitry and some of the main ones are what are called row decoders and column decoders which then feed into sense amplifiers.

And what these refer to -- the rows refer to word lines, where the columns refer to bit lines, and you typically have a memory cell at an intersection of a bit line and a word line so the cell array is where the memory cells themselves are located, and they are

generally surrounded by various types of peripheral circuitry such as the ones that I mentioned.

You also have other circuitry, such as, you know, input and output buffers for the data, timing circuitries, charge pumps.

Q. Does the cell array region itself contain any word line conductor structures?

A. Yes.

Q. All right. Now, it's your opinion that Kim discloses a structure with a plurality of stacks; right?

A. Yes.

Q. And it's your opinion that Kim discloses having each step comprise a gate stack disposed over a dielectric layer; right?

A. I believe that's true, but if you could point me to my declaration, to a specific paragraph?

Q. Yeah. That would be paragraph 90.

A. Yes.

MR. GRABOWSKI: Okay. Could we look at Kim's figure 22A, PDF page 39. Thank you. All right. Figure 22A is one of the figures showing the embodiment from Kim that you relied on for your

opinions in grounds one and two; correct?

A. Well, I interpreted figure 22A where the gate stack is below the insulating layer in light of the written description. That's why I call the gate stack on top, figure 22A in my declaration in paragraph 90.

So while 22A, as shown, might show the gate stack below the insulator, I proceeded to be able to interpret figure 22A in light of the specs where the order would be flipped as shown in the figure in my declaration.

Q. All right. So I appreciate you have the modified figure, and we are going to get there. For the moment I just want to talk about the figure 22A as it actually appears in the Kim reference, all right?

A. Okay.

Q. So figure 22A as it appears in the Kim reference shows a staircase structure for a 3D semiconductor memory device; right?

A. Yes.

Q. All right. And the staircase shown in Kim's figure 22A has a series of alternating insulating layers and gate stack layers; right?

A. Yes.

Q. All right. And each of those pairs of insulating layers and gate stack layers makes up a step of the staircase; right?

A. Yes.

Q. And do you see that there are numbers in figure 22A with lines pointing to different parts of the figure?

A. Yes.

Q. Do you have an understanding of the purpose of those numbers?

MR. HSU: Objection, vague.

THE WITNESS: Those numbers refer to specific elements of the figure, so that when you read the specifications, you can correlate the two and make sense of the description.

BY MR. GRABOWSKI:

Q. All right. Could we look -- if you look at number 11, do you see that?

A. Yes.

Q. Do you know what number 11 in figure 22A designates?

A. I'm pretty sure, but let me look at my soft copy of Kim. It says in paragraph 230 of Kim that layer 11 is a lower gate insulating layer formed between the lowermost gate conductive layer 101 and the substrate -- that's a silicon substrate -- 10.

Q. Do you know what the purpose of the lower gate insulating layer is?

A. Well, as a term, insulating gate, it's an electrical non-conductor, so it prevents electrical crosstalk with the substrate. Let me see if Kim has further description of that. Yeah, I don't believe Kim has any additional description, but, you know, as a POSITA or hopefully as an expert -- people do this all the time where the starting silicone substrate, you want to protect the top surface by growing a thermal oxide such as layer 11 to create a passivating film if you will and then it can make the structures on top of that.

It's sort of an additional insulating buffer, if you will, between the structures that I'm putting down in the 3D NAND flash and the starting substrate. I believe that's what they're doing over here, but I did not opine on those aspects in my report.

Q. All right. All right. And these numbers that label these different elements, is it your understanding that they are consistent across the patent?

A. Depends on what you mean across the patent, but as I describe in my report, certain figures do have a consistent set of numbering. For example, figure 22A and I believe figure 8 have similar numbering schemes, and to me that shows that Kim intends discussions for one figure being applicable to discussions with another figure, unless he explicitly points out differences.

MR. GRABOWSKI: So could we actually go to figure 8A, it's on PDF page 12.

Q. So number 11 there would also refer to a lower insulating gate layer; correct? Did I say that correctly?

A. I believe so.

Q. All right. And if I saw a number 11 in one of the other figures or referenced elsewhere in the specification, it would consistently refer to that same component?

A. I haven't done a detailed comparison. You know, sometimes people mess up patents, they have

misnumbered figures and all of that, but in general, in particular using similar notations in numbering schemes in different figures generally implies that they are comparable structures.

Q. All right. Comparable structures or the same structure?

A. I think that would depend on the specifications. I mean, if you point me to something specific, I can comment on that.

MR. GRABOWSKI: That's fine. Can we go back to figure 22, please. I lost of the page for you. Perfect. Thank you.

Q. Okay. So again, we're talking about figure 22A as it is in the actual Kim reference. The insulating layers are numbered 111 through 118; correct?

A. Yes.

Q. The gate stack layers are numbered 161 through 168; right?

A. Yes.

Q. So the combination of for instance insulating layer 111 and gate stack layer 168 make up one step of the staircase; right?

MR. HSU: Objection.

BY MR. GRABOWSKI:

Q. I'm sorry, I misspoke. I apologize. The combination -- strike that. Let's start this over.

The combination of insulating layer 111 and gate stack layer 161 make up one step of the staircase; correct?

A. Yes.

Q. And so for instance, looking at layers 111 and 162 in Kim's figure 22A, those are part of two different steps; correct?

A. Yes.

Q. All right. And you don't dispute that the actual figure 22A in Kim shows the gate stack layers on the bottom of each step; right?

A. I don't dispute that figure 22A, as shown, as already mentioned, but I would like to respectfully add this caveat that if you interpret figure 22A in light of the written description, it could be the other way around also, that the gate stack is on top and the insulator is below that.

Q. Understood. I'm just asking about the actual

picture in Kim itself. It has the gate stack on the bottom; correct?

A. Yes, figure 22, as shown, has the gate stack below the insulator.

Q. All right. Now, you've prepared a modified version of figure 22A at page 56 of your declaration showing a reversed order; right?

A. Yes, among other pages.

Q. And in that modified version, the gate stacks are shown on top; right?

A. Yes.

Q. All right. Now, in your declaration you don't list any benefits to reversing the order of the layers; right?

A. I don't think so. I mean, I cited to other prior arts such as Chen showing that it could go either way it's. A binary choice. Either the gate stack is going to be on top or below and Chen shows two figure side-by-side so it's a matter of simple choice, you can see that.

Q. It's a matter of simple choice, but there's no reason you give to go one way or the other; right?

A. No, I did not.

Q. All right. And reversing the order of the layers isn't the only modification you made to the figures; right?

MR. HSU: Objection, vague.

THE WITNESS: Could you point me to what other modifications I made?

BY MR. GRABOWSKI:

Q. Yeah. You also changed the depth of the word line contacts; right?

A. I did, but that's a trivial change in my opinion. If you put the gate stack on the top of each step the distance from the top surface to that would go down a little bit so the word line plug is a little bit shorter.

Q. And that would require a change to the etching process; right?

MR. HSU: Objection, vague.

THE WITNESS: I -- I respectfully disagree. You're etching through this insulator that covers the side of the staircase, and it's very, very hard to perform these vertical anisotropic etches

through things like reactive ion etching. A lot of these chemistries are very well-established, so to me, that is what the etching process involved and that doesn't have to be changed. Whether you have to maybe increase the etch time a tiny percentage, I don't feel like it's a new etching process per se.

BY MR. GRABOWSKI:

Q. Okay. You agree you would have to change the etch time because you're going to a different depth; right?

A. If you kept all the other etch parameters exactly the same, you would have to marginally increase etch time, but if etch time was important, there's plenty of other parameters that a POSITA can tweak. For example, maybe, you know, changing the plasma power a little bit or tweaking the chemistry of the gases a little bit.

I mean, there's many knobs that one can twiddle in the etch processes. See, in my opinion, the etch process per se refers to whether I'm using things like reactive ion etching, which is generally used to

perform these anisotropic etches and then you choose appropriate gases, you choose a certain etch chamber, and those are the essential elements of the etch process. Whether the time has to be increased by a couple of percent or so, it's not rocket science.

Q. Okay. It sounds like we might be just using different terms here. So you're talking about etch process versus etch parameters; is that fair?

A. Well, I was talking about the etch process broadly, and of course the different parameters that enter into etch process include things like plasma power and the etch time, so if you left all the other parameters in a particular etch process the same going from gate stack below to gate stack above would involve increase in the etch times a small percentage, and that's a very simple modification in my opinion.

Q. All right. And if you wanted to leave the etch time the same but change the depth of the etch to account for the reverse order, what other parameters might you change instead?

A. There's many process -- many parameters that can be changed. So in general if you increase the

plasma power that is used in a reactive ion etcher, etch rates tend to go up. In reactive ion etching you typically place the wafers on what is called the powered electrode on which a bias is applied, which allows the ions in the plasma to perform this anisotropic bombardment.

You can increase that bias in voltage a little bit. You can change -- these etch gases are typically a mixture of different gases. You have -- I mean, you'd have to show me the exact process because I mean, I've been doing plasma etching for 40 years. I mean, you can change the percentages of some of the components to tweak the etch rates. This is all very standard tweaks that a process engineer would know how to do.

Q. When you say change the percentages of the components, do you mean the components of the gas or of the structure itself?

A. Components of the gas. That's what I meant.

Q. Are there any other parameters you could tweak to achieve a different etch depth?

A. I think I mentioned plasma power, etch gas chemistry and the biasing voltage. The chamber pressure

would be another parameter. If you reduce the pressure, generally speaking, the mean free path of the ions will go up and that can sometimes increase the etch rate. So that would be another parameter.

Q. Any other parameters you can think of?

A. Temperature could be a parameter also. In general, higher the temperature, etch rates can go up. I'm speaking in very broad terms, okay? I mean, these reactive ion etches have a physical component to the etch, where ions bombard the surface essentially in the vertical direction.

That's what makes the etch anisotropic, but they tend to be somewhat non-selective, so you also have a chemical component to the etch, which is selective. And that's very important in this context in that selective component the chemical component of the etch is generally going to be temperature dependent, and as you increase the temperature of the substrate in general that etch rate will go up, but once again, you know, specifics matter, so you have to show me a specific processes, and there's always technological counterexamples.

Q. Understood. And the impact of all of these parameters -- strike that.

Because I think this is what I think you're getting at with specifics matters, but I just want to make sure. The impact of all of these parameters on the etch depth is going to depend on the specific materials that you're etching through correctly; correct?

A. Yes.

Q. Perfect. All right. Okay. All right. Now, we -- and depending on whether the gate stack is on the top or on the bottom, there would be an additional dielectric layer you would either have to etch through or not; correct?

MR. HSU: Objection, vague.

THE WITNESS: At each step, if the gate stack was below the insulating layer -- there's layers 111 to 118 -- you'd have to etch through those layers to reach the gate electrode itself, but once again, these are trivial changes in my opinion.

BY MR. GRABOWSKI:

Q. Okay. And we touched on this briefly when going through the typos, but let me just get a clean

record: Kim discloses two stop layers; right?

A. Yes.

Q. And those are 126A and 126B; correct?

A. Yes.

Q. And it's your opinion that 126B is the etch-stop layer required by the claims; right?

A. Yes.

Q. All right. You don't offer an opinion in your declaration that Kim discloses any specific thickness of that second stop layer; right?

A. For the second stop, are you referring to 126B?

Q. Yes.

A. Yeah. No, Kim does not have any disclosure of thicknesses, which is why we use the combination with Fang.

Q. All right. We've been going about an hour, doctor, and this is a pretty good place to stop, so if you want to take a break, this might be a good time.

A. Yeah, I would like that. Yeah. How long?

Q. How long would you like?

A. Five to 10 minutes, maybe?

Q. Ten minutes sounds perfect.

A. Thank you.

(Off the Record from 7:57 AM to 8:10 AM)

BY MR. GRABOWSKI:

Q. All right. Could we bring back up that figure 22A from Kim, please. All right. So we've been talking about the etching process and etching parameters before we broke off and I just wanted to understand the process a little more. Looking at figure 22A here as it is in Kim with the gate stack on the bottom, do you see that?

A. Yes.

Q. And so to etch one of these word line contacts or I guess the hole for it, you're going to have to drill through -- or etch through, excuse me -- the insulator that is labeled 134; right?

A. Yes.

Q. And then you're going to have to etch through stop layer 126B; right?

A. Yes.

Q. And then you're going to have to etch through stop layer 126A; right?

A. Yes.

Q. And then you're going to have to etch through the insulating layer that's disposed over that particular gate stack; correct?

A. Yes.

Q. All right. The purpose of stop layers 126A and 126B is to be resistant to etching; correct?

A. It's to be resistant to over etching. You want to etch holes in 134 and then slow down the etching dramatically once you hit 126B in this case.

Q. So proactively speaking, once you're through 134 and you hit 126B you have to change the etch parameters; right?

A. Yes, typically the etch chemistry.

Q. Okay. And when you say change the etch chemistry what do you mean by that?

A. The gases that are used for the reactive ion etch process

Q. Okay. So once those gases get you through 126B, do you have to change the etch chemistry again when you get to 126A?

A. Generally speaking. So the reason for having two different etch top layers. 126A and 126B is to give

you additional margins of safety, if you will. I mean, you can make do with just one etch top layer as Fang has for example. This merely gives you additional flexibility in preventing over etching to the staircase stack.

Q. And so once you're through 126A and you get to the dielectric layer that's disposed over the top of the gate stack do you have to change etch chemistries again?

A. Typically. So typically whenever you have different materials combinations, you have to tweak the etch chemistries a little bit. Now, when I say tweak, they are very often -- once again, details matter. I'm speaking again in generalities, so very often these -- the class of gases called CFCs, chlorofluorocarbons, and then you have additive gases.

So it's not as if -- in most cases you're not talking about drastic changes, but the way etch top layers work is based on the fact that you're looking at different materials, which are different etch rates in a particular gas, and the ratio of the etch rates is what's called etch selectivity, so by having etch-stop layers it gives you additional margins of safety.

You also then -- after you etch through the insulator you also have to etch high-k gate dielectrics that are surrounding the electrode, okay? So that's -- I don't think that's labeled in this figure specifically, whereas that cap layer covering the crosshatch regions 161 and 162.

Q. Okay. So once you get through the two stop layers you change etch chemistry to etch through the insulator if the insulator is on top and then you change etch chemistry again to etch through the high-k dielectric?

A. Generally speaking, yes.

Q. And then if the gate stack is on top, you still have to change etch chemistry to go through the high-k dielectric, but you don't have to change etch chemistry to go through the insulator because that's not there; right?

A. So once again, it depends on the specifics, but in many cases this insulating layer 134 is generally going to be made up of silicon dioxide as well as these layers 111, okay? Not in all cases, but in many cases. So the etch chemistry that you use for 134 will very

often work through layers 111 through 118, okay? In general, but I mean, of course, they can be counterexamples.

So in broad terms, when you have two different materials that I'm trying to etch, you generally have to have a tweak of the etch gas chemistry so that you preferentially etch one but not the other.

Q. And in instances where the insulating layer is disposed over the top of the gate stack, there's going to be one more instance of changing the etch chemistry to get through that layer even if it is going back to the original -- strike that.

That was a terrible question. In cases where there's a dielectric disposed over the top of the gate stack layer, you're going to have to change etch chemistries to go through that layer; correct?

A. If the dialectic layer was on top of the gate stack, you typically have to change etch chemistries between -- in this case layer -- etch top layer 126A and the dialectic layer, okay? But as we propose, if you put the gate stack on top of the insulating layers, you don't have to do that change, okay? So that's a benefit

of the modification that we are showing.

Q. And the insulating layer on top, however, provides extra margin to prevent over etching; correct?

A. Not necessarily -- necessarily because you have actually quite a few margins of safety, right? In addition to these two etch stop layers, 126A and B as I said. You also have the high-k dielectric surrounding the metallic gate electrode or the polysilicon top gate electrode and the etch to that high-k dielectric also if you are using a high-k dielectric, which is generally done these days. That will have a different composition typically than the etch-stop layers, so that gives yet another margin of safety.

Not a huge margin, however, because these high-k dielectrics tend to be very thin, so even if you slow down the etch rate, you don't buy a lot of extra time. These are all very well known teachings that a POSITA would know. I mean, I teach this to my undergrads. Even they can do it.

Q. Okay. So the high-k dielectric provides a safety margin. I appreciate there are other safety margins, but if you have the -- the dielectric layer

there between -- between the high-k dielectric and the stop layer 126A, that's going to increase the safety margin; right?

MR. HSU: Objection, asked and answered.

THE WITNESS: I mean, in general, the more different materials that you have that the etch has to go through, in general, that provides additional safety margins.

BY MR. GRABOWSKI:

Q. All right. We can take Kim down for the moment. Before we go on to the next document I just want to double-check, did you speak to your counsel during the break?

A. No.

MR. GRABOWSKI: Okay. Could we put up Exhibit 1007 Fang, please.

THE TECHNICIAN: Stand by.

BY MR. GRABOWSKI:

Q. All right. And do you recognize this as Exhibit 1007, the Fang reference you relied on for your declaration?

A. Yes.

Q. And in your opinion Fang discloses the use of an etch-stop material; right?

A. Yes.

Q. And specifically as we have discussed, Fang discloses a single layer of etch-stop material; right?

A. Yes.

Q. Fang doesn't disclose the use of a barrier layer; right?

A. Not that I remember.

Q. The only specific material Fang identifies as an etch-stop is carbon-doped silicon nitride; right?

A. I don't recall if (inaudible). Can you blow up the page a little bit maybe? At my age I can't read with glasses or without glasses. Within the extract talking about using a carbon-doped silicon nitride as the etch-stop layer. I don't know if in the specs he has other descriptions, but this is just exemplary in my opinion.

Q. Fair to say you are not aware of anywhere else in Fang where he discloses an alternative etch-stop material?

A. I have not searched for that. I can pull up

my soft copy and do a quick search, but often I'm not.

Q. You're welcome to take a look if you like, otherwise I'm happy to take it as you're not aware.

A. Yeah, sitting here and not doing a search right now, I am not aware.

MR. GRABOWSKI: All right. And could we go to the claims of Fang which start on PDF 16.

Q. Fair to say that all of the claims require a carbon-doped silicon nitride etch-stop?

A. Can you scroll down? Is 11 the last claim?

Q. No. It goes on to the next page.

A. Okay. The ones that I'm seeing all have carbon-doped silicon nitride, but I may add that it's in this case mostly silicon nitride with tiny percentages of carbon added to it.

MR. GRABOWSKI: All right. Could we go to the next page just so Dr. Banerjee can confirm it's all the claims?

THE WITNESS: Yeah. I believe the claims specifically mention carbon-doped silicon nitride, but the main teaching we took from Fang was teachings about the thicknesses of the etch-stop

layer, and I think that basic teaching would carry over to some other etch-stop compositions also.

BY MR. GRABOWSKI:

Q. Do you have an understanding of whether there is a difference between silicon nitride and carbon-doped silicon nitride?

A. Yes.

Q. What is your understanding of that difference?

A. So silicon nitride is a chemical composition of (Si3N4), but very often that also has a certain amount of hydrogen in it depending on the way you deposit it, specifically very often silica nitrite is deposited through what is called plasma enhanced chemical vapor deposition using precursor gases such as silane and ammonia and you end up getting different percentages of hydrogen in it, but the basic formula of silicon nitride is (Si3N4).

Q. And what's the difference between (Si3N4) and carbon-doped silicon nitride?

A. Well, as the claims and I guess the specs describe they are incorporating different percentages -- small percentages of carbon, I guess one to 10 percent,

can't remember exactly, I guess one to 15 percent I guess. So in this case if you're depositing these etch-stop layers through PECVD, plasma enhanced chemical vapor deposition, you have to throw in a carbon precursor also. There's many of these, you know, maybe methane or ethane or whatever. I haven't reviewed those lately, but one might be able to use those.

So depending on the exact percentage of carbon, the etch -- unintentional etch rates of this etch-stop layer may vary somewhat, but I think the main teaching that once you take away from Fang is the etch-stop layer thicknesses discloses I believe five nanometers to a hundred nanometers and then these etch-stop layers can have slightly different carbon content.

So to me, the fact that it's not disclosing different thicknesses for the different carbon compositions tells me that the exact composition may not matter that much. I mean, the POSITA will know how to choose a particular etch process depending on the precise etch layer composition and thickness, and the main overarching goal is whatever material I'm trying to

etch above the etch-stop layer should -- it doesn't really stop.

So the term etch-stop layer is a bit of a misnomer. I should call it an etch slowdown layer or etch drastically slow down layer. You're never going to get infinite selectivity between the material that I'm mentioning and the etch-stop layer, so it would be well within the capabilities of the POSITA to choose layer thicknesses and etch processes so that when I'm etching the layer I drastically slow down on the etch-stop layer.

And once again. The teaching that we took from Fang is the disclosure about the range of etch-stop layer thicknesses and the fact that, you know, it's a pretty wide range from five nanometers to 100 nanometers is a factor of 20. So I think it tells you as I discuss in my report these things are, in general, not going to be that critical.

Similarly, in the 711 patent it's an even larger range, 10 to a thousand nanometers in the factor of a hundred; right? So if those exact layer thicknesses of the etch-stop layer are critical in my

opinion the patentee should have narrowed down the range.

Q. I just want to break that down a little bit so I make sure I understand it. Is it fair to say that the carbon doping has an impact on the etch rate of the silicon nitride?

A. It could. If you left everything else the same in the etch process, changing the composition in general will change the etch rate.

Q. And carbon-doped silica -- strike that.

You've used the term etch selectivity. Can you just explain what you meant by that?

A. Sure. So when I'm etching through a multilayer stack for a particular etch process -- and by process I mean the whole thing, etch gas composition, plasma power, temperature, the whole thing -- so for a particular process you have a certain etch rate or etch velocity of a certain material, okay?

So suppose I have two materials, material one above material two is going to have an etch velocity V1 which would be the thickness of material one removed in a certain time T1, okay? Then once that etch reaches

material two you generally have -- you'll have a different etch velocity the thickness of material two removed in a certain time T2, okay? So the term etch selectivity is a ratio of the two etch rates, okay? So in the case of etch-stop layers or etch drastically slow down layers, you'd want the etch velocity of material one to be much, much higher than the incidental etch velocity of the material two, in this case the etch-stop layer.

Q. And so you've described the etch selectivity as a ratio. So fair to say that if the etch selectivity were a ratio of 1-to-1, there would be no etch selectivity?

A. That's correct.

Q. And if the etch-stop layer were made of the same material as the layer beneath it, then it would have the same etch velocity; right?

A. Do you mean the material above it because I'm etching a material and stopping on the etch-stop layer.

Q. Fair. I guess either way, but if the etch-stop layer were made as the -- of the same material as the layer above it, it would have no etch

selectivity; right?

A. In general, but in a -- once again, details matter. So you could deposit quote unquote the same material by different techniques, which might have an impact on the microstructure, and by different techniques I mean you could use plasma-enhanced CVD as I mentioned, but you could also use a technique called sputtering so we might deposit silicon nitride with the two techniques where nominally they both are (Si3N4) but one may be more porous than the other and in general more porous materials etch faster, but in broad terms it's the material chemistry that could impact the etch rate and therefore etch selectivity the most.

Q. All right. Have you ever, in your experience, used a material with the same chemistry as an etch-stop layer for an adjacent material?

MR. HSU: Objection, vague.

THE WITNESS: Could you repeat the question, please?

BY MR. GRABOWSKI:

Q. In your experience, have you ever used an etch-stop layer that has the same chemistry as the

material above it?

A. No, I have not.

Q. Okay. Have you ever heard of anyone doing that?

A. Off-hand I can't think of anyone.

MR. GRABOWSKI: All right. We can take Fang down. Can we put up Exhibit 1006 Park, please.

THE TECHNICIAN: Stand by.

BY MR. GRABOWSKI:

Q. All right. Doctor, this is Exhibit 1006 the Park reference you relied on in forming your opinions in this case; right?

A. Yes.

Q. And again, it's your opinion that Park discloses a staircase structure comprising a plurality of steps?

A. Yes.

Q. All right. And it's your opinion that Park discloses having each step comprise a gate stack disposed over a dielectric layer; right?

A. Yes.

MR. GRABOWSKI: All right. Could we go to

Park figure 9I, which is on PDF 30.

Q. All right. And Doctor, figure 9I is one of the figures showing the embodiment from Park that you relied on for your opinions in grounds three and four; right?

A. Well, I took figure nine, but as I describe in my report, it would be trivial to flip the order of the gate stack layer in the insulator.

Q. So I appreciate that, and we'll get to the modified figure, again, but for the moment I want to talk about Park figure 9I as it is in the reference itself; is that all right?

A. Okay.

Q. So figure 9I in Park shows a staircase structure for a 3D semiconductor memory device; is that right?

A. Yes.

Q. And again, it shows a serious alternating insulating layers and gate stack layers; right?

A. Yes.

Q. I realize by the way I've been using insulating and dielectric somewhat interchangeably. Do

you understand those to mean the same thing for the purpose of these staircase layers?

A. Yes. In this context, yes.

Q. All right. So the dielectric layers in figure 9I are numbered 171 through 177; correct?

A. Yes.

Q. And the conducting layers or gate stack layers are numbered 151 through 156; correct?

A. Yes.

Q. All right. And again, there's no dispute that the actual figure 9I in Park shows the gate stack layers on the bottom of each step; right?

A. Yeah, figure 9I specifically shows the gate stacks on the bottom, but once, reading Park in light of the specs, it would be trivial to flip the order.

Q. All right. And as we discussed, you prepared a modified version of figure 9I that shows that reversed order; right?

A. Yes.

Q. And as we discussed with Kim, you also changed the depth of the word line context; am I right.

A. By a trivial percentage, and I say trivial

because if you look at these figures, the etch time would be governed by 201; right? That's the deepest contact plug and that corresponds to a step height of the order of microns, each insulating layer -- 171, 172-177, it's much, much thinner than the depth of 180.

So when you flip the order, the change in the thickness that you have to etch changes by a tiny percentage, basically that with a ratio of thickness of, say, 172 divided by the thickness of 180, and that's a small percentage.

Q. And when we were looking at the Kim reference earlier we discussed a number of parameters of the etch-stop process that could be changed to achieve that change in etch depth; right?

A. Yes.

Q. Do all those same parameters apply here?

MR. HSU: Objection, vague.

THE WITNESS: In general, yes, but specifics matter, of course.

BY MR. GRABOWSKI:

Q. All right. Fair to say you could achieve the change in etch-depth by holding all the parameters

constant except etch time and changing the etch time?

MR. HSU: Objection, incomplete hypothetical.

THE WITNESS: I mean, if you kept everything else about the structure the same except flipping the order of the insulator and the gate electrode and you kept everything about the etch process itself the same, you'd have to change the etch time by a tiny amount as I just mentioned.

BY MR. GRABOWSKI:

Q. All right. And I believe you mentioned you could also achieve the change in etch depth by holding the parameters constant except for the etch chemistry and changing that slightly; is that correct?

A. You'll have to give me specifics, but in general that's true, because when you change the composition of the etch gases, etch rates tend to change.

Q. And you could also achieve it by holding all of the parameters constant and changing the etch temperature; is that right?

A. So these reactive ion etches, these anisotropic etches, which etch predominantly in the

vertical direction but not laterally, have two components to the etch: A physical component due to the ion bombardment, which is not that selective, but then a chemical component, which is generally much more selective, and chemical component generally depends strongly on temperature -- well, depends on temperature very often in Arrhenius dependence.

Q. Okay. So is that a yes, you could achieve a different etch depth by holding all the other parameters constant and changing temperature?

A. Yes. In general that's true, in broad terms.

Q. And you also mentioned I believe plasma power as a possible parameter you could alter to achieve a different etch depth; is that right?

A. Yes, plasma power also impacts etch rate, therefore you could use that as a parameter to tweak etch depth or etch times.

Q. Okay. And you could also adjust the bias voltage to achieve a different etch depth; is that right?

A. Yes. If you kept all the other parameters the same, the bias that you apply to the substrate will

impact the ion bombardment energy and that could have an impact on the etch rate.

Q. Are there any other parameters you could adjust that would alter the etch depth in light of the change in order layer?

A. I mentioned pressure -- chamber pressure -- so in general, the lower the pressure the longer the mean free path of the gas molecules and the ions, and that generally makes ion bombardment easier, so that's another parameter.

Q. Are there any other parameters I've left out?

A. There may be, but I can't think of anything off-hand.

Q. All right. All right. I'd like to look now at page 104 of your declaration. Just let me know when you're there.

A. Okay.

MR. GRABOWSKI: And if we could have it on the screen as well, that would be helpful.

THE TECHNICIAN: Counsel, you said 104?

MR. GRABOWSKI: Yes, of Banerjee 1.

THE TECHNICIAN: Stand by.

BY MR. GRABOWSKI:

Q. Thank you. Looking at page 104 of your declaration, this is a modified version of figure 9I from Park; is that right?

A. Yes. Here we have the gate stack on top.

Q. And this shows what, in your opinion, are the barrier layer and etch-stop layer that Park discloses; right?

A. Yes.

Q. All right. You've labeled element 110A as the barrier layer; right?

A. Yes.

Q. And that element 110A is formed on the surface of the steps; right?

A. Yes.

Q. All right. And then over the barrier layer is another layer labeled AD2; right?

A. Yes.

Q. All right. And then on layer AD2 is layer 110B; correct?

A. Yes.

Q. All right. You've labeled layer 110B as the

etch-stop layer; is that right?

A. Yes.

Q. All right. So the etch-stop layer is formed on layer AD2; right?

A. In this figure, yes, but if you look at the specifications, Park says that AD2 is this additional dielectric, which is optional.

Q. So it would either be formed on AD2 or on the surface of the barrier layer?

A. That's correct.

Q. All right. And then it's the barrier layer that's formed on the surface of the steps, not the etch-stop; right?

A. Yes.

MR. GRABOWSKI: All right. I'd like to talk about the manufacturing process that Park uses. Could we go to Park page 103? That's Exhibit 1006 -- I apologize, not page 103, page 27. All right.

Q. Do you see here figures 9B through 9D? And we can scroll to show you the top label on that figure if we need to.

A. Sure, I see it.

Q. All right. Looking at figure 9B this shows the formation of insulating layer AD on top of the staircase structure; right?

A. Yes, and if you look at the specs, once again, Park says that's an optional layer.

Q. And then in 9C below it, it shows the formation of etch-stop sacrificial layers 115A and 115B; right?

A. Yes.

Q. All right. And those are formed on top of layer AD in the figure; right?

A. Yes, but once again, that layer AD is an optional layer according to the specs.

Q. All right. And then looking at figure 9D, it shows the formation of the connection region insulating layer No. 180 on top of etch-stop sacrificial layer 115B; right?

A. Could you scroll down a little bit maybe? Could you repeat the question, please.

Q. Yes. Looking at figure 9D, it shows the formation of the connecting region insulating layer 180

on top of etch-stop sacrificial layer 115B?

A. I still didn't get your question, my apologies. 115B on top of...

Q. Sorry, I'll start over. Figure 9D shows the formation of the connection region insulating layer 180; is that right?

A. That's actually showing 9E, not D, but anyway.

Q. It's kind of an artifact of how these are done. 9E is actually the figure on the next page I believe.

A. Oh, okay. Oh, okay. All right. I was reading it the other way around. Okay. Yeah. So 180 is an insulator on top of the connection region. Yes.

Q. Okay. And 180 is formed on top of sacrificial layer 115B?

A. Yes.

Q. Okay. Do you have an understanding of what a sacrificial layer is?

A. Well, here it's the etch-stop layer 115B, but in general the term sacrificial would mean you don't have it in the final structure. You sacrifice it; right, at some point?

Q. Okay. So I -- I'm sorry, I just want to make sure I understand. Is it your understanding that 115B is the etch-stop layer or that it's the sacrificial layer to form the etch-stop layer?

A. In my opinion, 115A and 115B would have different compositions, and therefore in a particular etch chemistry they could have different etch rates. So those could be the -- so if I make a correspondence with 711, 115B would be the etch-stop layer and 115A would be a barrier layer, but the barrier layer is also another type of etch-stop layer when I read 711.

MR. GRABOWSKI: Okay. Let's -- let's keep going. Could we -- could we scroll down to figure 9F please?

Q. All right. Do you see what's labeled T2 there?

A. Yes.

Q. Do you have an understanding of what element T2 is?

A. I don't recall. Let me search my soft copy.

Q. Paragraph 103 may be helpful I believe.

A. Okay. It says it's the side opening

corresponding to etch the space in which the etch-stop sacrificial layers are provided.

Q. So is it your understanding that T2 corresponds to a space left after the removal of layers 115A and 115B?

A. I don't think 115A and B would be completely removed. You're only going to be etching those in the word line plug regions, okay? And that doesn't cover the entire thread of the step. If you go back to, say, figure 9A, it shows these vertical word line contacts, right? And that doesn't cover the entire width of the staircase step.

So if I can scroll down -- see, if you look at figure -- I guess nine -- it's confusing. You said that the figures -- the figure captions refer to the figure --

Q. And --

A. Okay. So if we look at I guess figure 9H as an example. You're etching these vertical cavities, but you're not getting rid of -- I think here they are called two etch-stop layers 110A and 110B, but it's clearly the same as 115A and 115B. So we can see that

when I'm etching the vertical cavity, I'm not getting rid of all of 110A or 110B or correspondingly 115A and B, so the sides T2 will still have the remaining portions of 115A and B in my opinion.

Q. All right. So I just want to make sure I understand. It's your understanding that elements 115A and 115B are the same as elements 110A and 110B; is that right?

A. I'd have to review the patent to be a hundred percent sure, but I think that's right.

Q. All right. If it's okay with you, this may be another good spot for a break.

A. Yes, I'd love that. Thank you. Five, ten minutes again maybe?

MR. GRABOWSKI: Yeah. Let's do 10 minutes again.

(Off the Record from 8:57 AM to 9:03 AM)

MR. GRABOWSKI: Thank you very much, Dr. Banerjee. I have no further questions. I'll pass it to your counsel.

THE WITNESS: Thank you.

CROSS-EXAMINATION

BY MR. HSU:

Q. Yes. I have just a few questions for you, Dr. Banerjee, to make sure I understood your testimony. Recall [sic] earlier you had quite a bit of discussion with Counsel about etch parameters; is that right?

A. Yes.

Q. And you mentioned etch parameters such as plasma power, gas chemistry, voltage, chamber pressure, temperature and pressure; is that right?

A. Yes.

Q. Okay. And I think you characterized them as knobs; is that right?

A. Yes.

Q. And you also recall that you mentioned that these etch parameters would be depending on the specific materials that's involved?

A. Yes.

Q. Now, turning to your opinion that Kim discloses swapping of the order of each step in the stair -- staircase, okay?

A. Yes.

Q. How many of these parameters or how many of

these knobs does a POSITA have to turn to accomplish that order swapping?

A. A trivial change of the etch time, and I say trivial because, as I mentioned, when you look at the entire stack, each insulating layer is very, very thin compared to the entire staircase stack height, so very approximately the change of the -- keeping everything else the same, the etch time would have to be changed by the ratio of the insulating layer thickness or the entire stack thickness, which is a very, very small percentage.

Q. And is that all -- all that a POSITA would have to do to accomplish that order swapping?

MR. GRABOWSKI: Object to form.

THE WITNESS: I believe so, but if -- because it's important for the POSITA to keep the times exactly the same. You could twiddle some of those other knobs that I mentioned, so there's many ways of skinning this cat.

BY MR. HSU:

Q. And are those many ways within the knowledge and skill set of a POSITA?

MR. GRABOWSKI: Object to form.

THE WITNESS: Yes, they are, and I've been teaching an undergrad class on this topic of fabrication for 40 years. Even my undergrads could do it.

BY MR. HSU:

Q. Okay. And would your answer be the same with regard to swapping the order in the Park reference?

A. Yes.

Q. Okay. Turning now to your testimony toward the very end. Do you recall Counsel had discussion with you about the -- the layer T2 in the Park reference?

A. Yes.

Q. And I think you testified in response to Counsel's question on -- related to that and particularly the layers 115A and B, T2 and then 110A and B. You say that you'd have to review the patent to be sure. Do you recall that exchange?

A. Yes, yes.

Q. Okay. I would like to turn your attention if we can put the Park reference back on, or if it's more convenient for you --

A. Yeah.
Q. -- feel free to use your own copy.
A. Yes.
Q. But I'd like to turn your attention to paragraphs 104 through 107. I would like you to just take a little time to review those paragraphs, 104 through 107?
THE TECHNICIAN: Counsel, do you have a PDF page number you can send me?
MR. HSU: Oh, of course. Page 14. Thank you.
THE WITNESS: Yes, I see that.
BY MR. HSU:
Q. Okay. And to the extent that you recall what you testified regarding T2 and the layers 115A and B versus 110A and B, now that you have a chance to review these paragraphs, is there anything that you recall that -- that you -- strike that.
Okay. So is it your opinion -- strike that.
Is it your understanding that elements 115A and 115B are the same as elements 110A and 110B?
MR. GRABOWSKI: Object to form.
THE WITNESS: You're reading paragraphs 104

and 105. Yeah, I think there's a 1-to-1 correspondence between 115A and 110A and 115B and one oh -- 110B. Both of them are referred to as etch-stop layers.

BY MR. HSU:

Q. And that's what you meant by correspondence?

A. Yes.

MR. HSU: No further questions.

MR. GRABOWSKI: Nothing further for me. Thank you.

THEREUPON, the deposition of SANJAY BANERJEE, PH. D., taken at the instance of the Patent Owner, concluded at 9:09 a.m.

ACKNOWLEDGMENT OF DEPONENT

I, SANJAY BANERJEE, PH. D., do hereby acknowledge that I have read and examined the foregoing testimony, and the same is a true correct and complete transcription of the testimony given by me, and any corrections appear On the attached Errata sheet signed by me.

_____ _____

(DATE) (SIGNATURE)

C E R T I F I C A T E

I, Dwayne W. Lewis, Jr., CA-CSR 14636, do hereby certify:

That SANJAY BANERJEE, PH. D., the witness whose Deposition is hereinbefore set forth, was duly sworn by me before the commencement of such deposition and that such deposition was taken virtually and is a true record of the testimony given by such witness.

I further certify that the adverse party, MICRON TECHNOLOGY, INC., was represented by counsel at the deposition.

I further certify that the deposition of SANJAY BANERJEE, PH. D., occurred virtually, on Wednesday, August 13th, 2025, from 6:58 a.m. to 9:09 a.m. PST.

I further certify that I am not related to any of the parties to this action by blood or marriage, I am not employed by or an attorney to any of the parties to this action, and that I am in no way interested, financially or otherwise, in the outcome of this matter.

IN WITNESS WHEREOF, I have hereunto set my hand this 13th day of August, 2025.

_____

Dwayne W. Lewis, Jr., CA-CSR 14636

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