

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No. IPR2025-00117
U.S. Patent No. 10,672,711

**DECLARATION OF SANJAY BANERJEE, PH.D.,
IN SUPPORT OF PETITIONER'S REPLY BRIEF**

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I, Sanjay Banerjee, hereby declare as follows:

I. INTRODUCTION

1. My name is Sanjay Banerjee. I have been retained on behalf of Petitioner Micron Technology, Inc. (“Petitioner” or “Micron”) as an independent consultant in this proceeding before the United States Patent and Trademark Office (“USPTO”).

2. I have already submitted a declaration in this proceeding concerning technical subject matter relevant to the above-captioned *inter partes* review petition (“Petition”) of U.S. Patent No. 10,672,711 (Ex. 1001, the “’711 Patent”). My “Initial Declaration” is Ex. 1003.

3. A summary of my education, professional experience, and other qualifications is included within Paragraphs 5 to 14 in Ex. 1003 and in my CV (Ex. 1004).

4. I have been asked to review the Patent Trial and Appeal Board’s (the “Board’s”) Institution Decision, issued on June 4, 2025. I have also been asked to review Yangtze Memory Technologies Co., Ltd.’s (“Patent Owner” or “YMTC”) Patent Owner Response (“POR”), the accompanying exhibits—including the supporting Declaration of Stephen Campbell (Ex. 2009)—and the transcript from Dr. Campbell’s deposition, taken on November 7, 2025 (Ex. 1027), and to provide my opinions on certain statements and arguments presented in YMTC’s materials.

5. In this “Reply Declaration,” I do not address every argument or opinion that appears in YMTC’s Patent Owner Response or Dr. Campbell’s declaration with which I disagree. Instead, I focus on arguments and opinions that seem likely to be relevant to the determination of obviousness. For this reason, the opinions that I express in this Reply Declaration are not exhaustive of my opinions regarding the unpatentability of claims 1-19 of the ’711 Patent. Importantly, the fact that I do not address a particular point or argument should not be understood to indicate an agreement or concession on my part. And, unless I state otherwise, the opinions I provide below apply equally to both YMTC’s Patent Owner Response and Dr. Campbell’s declaration, such that any opinions concerning the Patent Owner Response apply to the corresponding section of Dr. Campbell’s declaration (and vice versa).

6. I have confined my analysis to the materials that were available when I prepared this Reply Declaration. I reserve the right to supplement my Initial Declaration and this Reply Declaration in response to additional evidence that may come to light.

II. COMPENSATION

7. I am being compensated for my work in this matter at an hourly rate of \$650.00 for consulting services. My compensation is not based on the outcome of this matter or on the substance of my opinions.

III. MATERIALS CONSIDERED

8. In preparing this Reply Declaration, I considered the following materials, along with any other materials referenced in the body of my Initial Declaration and this Reply Declaration:

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 10,672,711 to Zhu et al. (“the ’711 Patent”)
1002	File History of U.S. Patent No. 10,672,711 (“the ’711 FH”)
1003	Declaration of Dr. Sanjay Banerjee (“Banerjee”)
1005	U.S. Patent Publication No. 2012/0070944A1 to Kim et al. (“Kim”)
1006	Korean Patent No. 10-2015-0051841 to Park et al. (“Park”) including certified translation
1007	U.S. Patent Publication No. 2019/0067306A1 to Fang et al. (“Fang”)
1008	U.S. Patent Publication No. 2017/0294384A1 to Chen (“Chen”)
1009	Aritome, “NAND Flash Memory Technologies” (2016)
1010	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1011	Michelsoni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1012	U.S. Patent Publication No. 2017/0117222A1 to Kim et al.
1013	Chang and Sze, “ULSI Technology” (1996)

EXHIBIT NO.	DESCRIPTION
1014	Orlowski et al., <i>Si, SiGe, Ge, and III-V Semiconductor Nanomembranes and Nanowires Enabled by SiGe Epitaxy</i> , ECS Transactions Vo. 33, No. 6 (2010), 777-89
1015	U.S. Patent No. 9,728,547 to Ohsaki et al.
1016	U.S. Patent Publication No. 2017/0148677A1 to Shin
1017	U.S. Patent Publication No. 2013/0313627A1 to Lee et al.
1027	Transcript of November 7, 2025 deposition of Stephen Campbell, Ph.D.
1029	U.S. Patent Publication No. 2013/0228837A1 to Sukekawa et al. (“Sukekawa”)
1030	U.S. Patent Publication No. 2007/0075428A1 to Wang et al. (“Wang”)
1032	Dhungana et al., <i>Combinatorial Survey of Fluorinated Plasma Etching in the Silicon-Oxygen-Carbon-Nitrogen-Hydrogen System</i> , Journal of Vacuum Science and Technology A (2016), 061302-1–18

9. As stated above, I also reviewed and considered the Board’s Institution Decision (Paper 19), issued on June 4, 2025; YMTC’s Patent Owner Response (Paper 27), filed on August 26, 2025; and the exhibits that YMTC submitted with its Patent Owner Response, including Dr. Campbell’s declaration (Ex. 2009).

IV. UNDERSTANDING OF THE GOVERNING LAW

10. I am not an attorney but have been instructed on and applied the law as described in my Initial Declaration.

V. CLAIM CONSTRUCTION

11. In my Initial Declaration, I opined that “all terms of the ’711 Patent’s claims may be understood based on their plain and ordinary meaning.” Ex. 1003 ¶ 62. I further explained that “[t]he ’711 Patent defines ‘on’ to include both directly on something and indirectly on that something.” *Id.* ¶¶ 118, 122, 151, 171, 174 (citing Ex. 1001, 4:1-6.).

12. Dr. Campbell opined that, as an exception to the definition of “on” in the ’711 Patent, the phrase “on the surface” means “directly on [the surface].” Ex. 2009 ¶¶ 47, 70. Dr. Campbell testified that this construction is solely based on the embodiments of the ’711 Patent. Ex. 1027, 122:6-123:4, 124:6-23. His explanation of the embodiments appears in Paragraph 28 of his Declaration Ex. 2009.

13. Patent Owner’s construction has a different wording from Dr. Campbell’s. Patent Owner construes “[o]n a side surface and a top surface...” as “*directly contacting* a side surface and a top surface.”¹ POR, 8.

14. I disagree with Dr. Campbell and Patent Owner for several reasons.

15. First, it is plain to a POSITA that the ’711 Patent defines the word “on.” I am not aware of the patent also disclosing an exception to this definition. Nor did Dr. Campbell identify any such exception. Thus, Dr. Campbell’s construction is

¹ All emphases are added unless noted otherwise.

contradicted by the '711 Patent's express definition.

16. Second, Dr. Campbell's redefinition of "on the surface" as "directly on [the surface]" inserts a word into the phrase. Ex. 2009 ¶¶ 47, 70. This is inconsistent with the understanding of a POSITA. The '711 Patent repeatedly uses phrases such as "directly disposed on" and "directly on." Ex. 1001, 7:67-8:3, 11:16-19, 11:29-22. Although these phrases do not involve a "surface," they indicate to a POSITA that the inventors used the word "directly" with "on" when they intended that narrower (than the express definition) meaning. The absence of "directly" in the claim language makes clear that direct contact is not required.

17. Patent Owner's redefinition of "[o]n a surface" as "*directly contacting* a surface" suffers from a similar problem. The '711 Patent uses the phrase "directly contacting" or "directly contacts" several times. Ex. 1001, 11:29-35, 11:35-41, 14:4-5, 14:15-17. Once again, this indicates to a POSITA that the inventors used the phrase "directly contacting" when they intended that specific meaning. In fact, in each of these four times the '711 Patent uses "directly contact[s]/[ing]," it refers to the direct contact between the conductive structures and the gate conductive layers. This at least suggests that the inventors used "directly contact[s]/[ing]" where an electrical connection between the two contacting components is needed. But the etch-stop layer of claims 14 and 15 does not establish electrical contact with another component. The etch-stop layer is an insulator.

18. Furthermore, claims 6 and 13 recite “directly contacts.” I understand that different patent terms are typically understood to have different meanings. Here, claims 14 and 15, by virtue of their dependency from claim 13, recite both “directly contacts” and “on.” Those recitations of different terms strongly suggest different meanings. As explained in the previous paragraph, a POSITA would understand that “each conductive structure *directly contacts* the corresponding conductive layer of each step” of claim 13 involves an electrical connection, and “the etch-stop layer is formed *on* a side surface and a top surface of each step” of claim 14 does not. Thus, a POSITA would understand these two different terms to mean different things.

19. Third, Dr. Campbell testified that his construction is solely based on the embodiments of the '711 Patent. Ex. 1027, 122:6-123:4, 124:6-23. I understand that the presence of a structure or configuration in an embodiment is not an adequate basis to limit the scope of a term. Furthermore, his construction directly contradicts the '711 Patent's statement that the embodiments are merely exemplary and do not limit the claims. Ex. 1001, 14:64-67. Thus, in view of the '711 Patent's express statement that the embodiments are not limiting, a POSITA would not have understood exemplary embodiments to override the express definition of “on.”

20. Patent Owner further argues that Petitioner's position is inconsistent with the '711 Patent's “equating ‘on’ with ‘above’ and ‘over.’” POR, 10 (citing Ex.

1001, 4:1-10). I note that Patent Owner does not cite Dr. Campbell, and this allegation is simply attorney argument. Nonetheless, I disagree with this argument. The '711 Patent defines all three terms such that “the[ir] meaning[s] ... in the present disclosure should be interpreted in the broadest manner...” Ex. 1001, 4:1-3. Toward that objective, the patent defines “on” to include “‘on’ something with an intermediate feature or a layer therebetween,” and “above” and “over” to include “‘above’ or ‘over’ something with no intermediate feature or layer therebetween (i.e., directly on something).” *Id.*, 4:1-10. In other words, all three terms may refer to a situation where a thing is “on,” “above,” or “over” another thing with or without an intermediate feature or layer. While Patent Owner is right that the patent thereby equates the meaning of the three words, there is no inconsistency between the Petitioner’s position and the three words having the same meaning.

21. Patent Owner’s argument against a hypothetical position appears to be just that — a hypothetical. POR, 11-13 (“If Petitioner argues....”). I did not opine in my Initial Declaration that “the surface of ‘each step’ in claims 14 and 15 refers to the surface of additional layers placed on top of the staircase steps....” *Id.*, 11. Patent Owner’s cites to statements from the Petition and my Initial Declaration confirm as much. *Id.*, 11-13.

22. Patent Owner further argues that if “on a side/top surface” can include “indirectly on a side/top surface,” that would render “side/top surface” meaningless.

POR, 14. Initially, I note this is again an attorney argument without any citation to Dr. Campbell. Regardless, I disagree with this argument. “Surface” can identify a plane or a two-dimensional set of points that is the reference for “on a side/top surface.” For example, if claim 14 had recited “wherein the etch-stop layer is formed on a side [] and a top [] of each step” and omitted the word “surface,” a POSITA would understand the claim to possibly permit the etch-stop layer to be part of the step, that is, part of the etch-stop layer may be in the interior of each step (yet still on, e.g., the “side” of the step). On the other hand, the actual claim 14, reciting “wherein the etch-stop layer is formed on a side surface and a top surface of each step,” requires the etch-stop layer to be a structure that is on the exterior of the step.

VI. GROUND 1

A. Kim Renders Obvious “Each Step Comprises a Gate Stack Disposed Over a Dielectric Layer”

1. Kim’s embodiments are properly combined

23. In my Initial Declaration, I explained that while Kim illustrates a staircase structure with dielectric layers at the top of each step, Kim also expressly discloses the opposite order, i.e., a staircase structure with gate stack at the top of each step. Ex. 1003 ¶ 69. I also explained that, although the express disclosure of the opposite order is made in the context of other embodiments, a POSITA would have understood that it is also applicable to the Figure 17A-22B embodiment. *Id.* ¶ 71. I further cited additional references to explain that both configurations were

well known in the art. *Id.* ¶¶ 80-83. In particular, prior art reference Chen discloses both configurations side-by-side with only short descriptions. *Id.* ¶ 81 (citing Ex. 1008, Figs. 7A-7B, [0044]-[0046]). Kim's disclosure, along with these references, demonstrates that both layer orders were well known and routine to implement.²

24. The gate-layer-on-top and the dielectric-layer-on-top configuration were common, well understood, and predictable variations of a staircase structure. In both, the alternating layers perform their typical functions: the gate layers serve as word lines connecting the vertical conductive structures to the gate terminals of memory cells, and the dielectric layers provide insulation and structural support between the gate layers. The order of the alternating layers in each step of the staircase does not change or impact their function in a meaningful way. Selecting one of the two orders was a simple design choice, as I testified in my deposition.

² Similarly, I explained that Park also expressly discloses a staircase structure with gate stack at the top of each step even though its figures *for the same embodiment* illustrate the opposite order. Ex. 1003 ¶ 75. And the references supporting both layer orders for Kim also support the same for Park. *Id.* ¶ 139. Patent Owner does not dispute this cross applicability. POR, 21 n.4. Indeed, Kim and Park's analogous disclosures further reinforce the conclusion that both layer orderings were well known and routine.

Ex. 2008, 35:12-36:1. The two orders are functionally equivalent, predictable variations of each other. Both make good staircase designs. Each provides alternating dielectric and conductive layers, and in both orderings, the staircase contacts extend into or on respective conductive layers, thereby providing contacts to the word lines in a 3D NAND design. Either one may substitute for the other. Because both configurations were routinely used and well understood, Kim (and Park) simply mentions the opposite gate-stack-on-top configuration in passing.

25. Chen illustrates this conclusion well. Chen's Figures 9A-11B illustrate a manufacturing process for a 3D memory staircase comprising an etch-stop layer and conductive structures. Chen, Figs. 9A-11B, [0018]. The two side-by-side figures in each pair (e.g., 9A and 9B, 10A and 10B) respectively show a dielectric-layer-on-top configuration and a gate-layer-on-top configuration. Figures 9A and 9B show the formation of the steps of the staircase. The two opposite orders are simply described together in one short paragraph. *Id.*, [0055]. Figures 10A and 10B show the formation of the etch-stop layer on top of the staircase. Again, the two figures are described together in one short paragraph. *Id.*, [0056]. Figures 11A and 11B show the formation of the dielectric layer and the conductive structures above the staircase. Again, the two figures are described together in one short paragraph. *Id.*, [0057]. Chen simply does not distinguish these two opposite orders in its descriptions. Chen shows that these two opposite orders are simply a design choice,

a suitable substitute for each other, and do not make a difference for purposes of constructing a 3D memory staircase. Importantly, Chen does not discuss differentiating implementation details between the two orders, because these implementation details are well known to a POSITA.

26. The '711 Patent similarly omits many details of its implementation, an observation with which Dr. Campbell agrees. When asked about the numerous etch-stop thickness ranges disclosed by the '711 Patent, and how any particular thickness or thickness range is appropriate for the numerous combinations of materials for the sacrificial layer and the etch-stop layer, he first acknowledged that the '711 Patent does not identify any particular thickness range as suitable for a particular material combination, and that a POSITA would have to experiment to make it work. Ex. 1027, 105:23-107:6. But he further testified that “*every time* you do *any* deposition and etching, you have to” “experiment to make [it] work.” *Id.*, 106:23–107:10. “[A] POSITA would certainly know that’s what you have to do. This is not unique to this process.” *Id.* In other words, given the disclosure of the '711 Patent (or Chen, for example), a POSITA would have to run routine experimentation to implement any disclosed embodiment, using implementation details known to a POSITA and therefore not disclosed in the patent. *Id.*, 110:14-111:5. Such experimentation includes details of etching, for example, such as the “kind of machine” or the type of plasma to use, which is for the engineers to “figure out.” *Id.*, 58:20-59:11.

27. Implementing either layer ordering was well within the knowledge and skill of a POSITA. As I testified, even my undergraduate students would know how to implement either order. Ex. 2008, 72:4-74:9. One straightforward method of forming a staircase structure with the opposite layer order is simply to reverse the order of depositing a sacrificial layer (which will be replaced by a gate stack) and a dielectric layer. For example, depositing a dielectric layer first on the substrate, followed by a sacrificial layer on top, and repeating in the same order for the desired number of times, can form a gate-stack-on-top staircase when the steps are completed. To form a dielectric-layer-on-top staircase, one can deposit a sacrificial layer first on the substrate, followed by a dielectric layer on top, and repeat in the same order for the desired number of times. Dr. Campbell agrees that this simple change in the order of deposition will change the layer order of the staircase structure. Ex. 1027, 93:12-18, 95:13-25.

28. While the high-level changes that I briefly describe would involve changes in implementation details, such as deposition or etch parameters, such changes, in the words of Dr. Campbell, “[are] not unique to this process.” Ex. 1027, 106:23–107:10. “[A] POSITA would certainly know that’s what you have to do.” *Id.*

29. Dr. Campbell does not dispute that Kim discloses the gate-stack-on-top configuration. Ex. 2009 ¶ 36. He merely argues that the express disclosure of the

opposite layer order is made in the context of the Figures 4 embodiment and does not apply to the Figure 17A-22B embodiment. He further made a conclusory statement that the Figure 4 embodiment does not include an etch-stop layer or a barrier layer, and thus a POSITA would not have been motivated to apply the express disclosure regarding Figure 4 to the Figure 17A-22B embodiment. I disagree with Dr. Campbell.

30. Preliminarily, I note that Figures 5A through 14B “illustrat[e] a method of fabricating the three-dimensional semiconductor memory device of FIG. 4.” Kim, [0014]. Thus, Figures 4 and 5A-14B, like Figures 17A-22B, constitute one embodiment. Next, the differences between the Figure 4-14B embodiment and Figure 17A-22B embodiment are not in the staircase. Dr. Campbell identifies the absence or presence of the etch-stop layers 126a/126b. Ex. 2009 ¶ 36. But as a POSITA would have understood, the formation of the etch-stop layers does not affect the formation of the staircase itself. These different structures are formed in sequential steps, and the steps of forming the etch-stop layers do not impact the steps of forming a staircase. That is why, for example, Kim uses the same reference numbers to refer to common elements, including all elements in the staircase, between the two embodiments. Kim, [0184]. That is also why Kim’s description of the Figure 17A-22B embodiment begins directly with the etch-stop layers, skipping descriptions of the staircase. *Id.*, [0185]-[0188]. This is in direct contrast to the

description of the Figure 5A-14B embodiment, which begins with a discussion of staircase formation. *Id.*, Figs. 5A-7B, [0058]-[0085]. References to the layers SC1-SC8 and 111-118 within the staircase of the Figure 17A-22B embodiment are related to the etch selectivity of the etch-stop layer relative to the staircase layers, which are descriptions of the etch-stop layer relative to the base staircase layers. *Id.*, [0186]-[0187]. A POSITA would have understood, and certainly found obvious, that the starting point for the description of the Figure 17A-22B embodiment would be the opposite ordering of the gate and dielectric layers when a gate-stack-on-top embodiment is desired. Kim's disclosure discredits Dr. Campbell's conclusory argument that "a POSITA would not be motivated to combine [the Figure 4 and 5A-14B embodiment] with the embodiments of Figs. 17A-22B" because the former "do[es] not teach an etch-stop layer or a barrier layer." Ex. 2009 ¶ 36. As I testified, selecting between the two layer orderings is a matter of simple design choice. Ex. 2008, 35:12-36:1.

2. Kim has no missing limitation and Ground 1 does not rely on another source to supply a limitation

31. As a preliminary matter, I note that Patent Owner alleges the claim limitation "a gate stack disposed over a dielectric layer" to be "missing" from Kim, and that Petitioner appeared to "rely on Chen, Ohsaki, or Shin to supply [that]"

missing limitation.” POR, 21, 23.³ By referring to Chen, Ohsaki, and Shin, Patent Owner indicates that it uses “missing limitation” to refer to a feature that is missing from the reference the Ground expressly includes, e.g., Kim. I disagree that the gate-stack-on-top limitation is missing from Kim, as explained in my Initial Declaration and in the section above. Further, Dr. Campbell’s opinion does not appear to support Patent Owner’s argument that the gate-stack-on-top limitation is missing from Kim. Referring to Kim’s Figure 17A-22B embodiment, Dr. Campbell stated that “[t]his *embodiment* of Kim does not disclose that each step comprises a gate stack disposed over a dielectric layer as recited in claims 1 and 13.” Ex. 2009 ¶ 35. And he admits that the gate-stack-on-top configuration is disclosed in relation to “Figures 4, 8A, and 8B,” that is, the Figure 4 and 5A-14B embodiment. *Id.* ¶ 36. Thus, Patent Owner’s argument that the gate-stack-on-top limitation is missing from Kim appears to be an erroneous attorney argument.⁴

³ This is not the case. As my Initial Declaration shows, Chen, Ohsaki, and Shin show that a gate-layer-on-top configuration was common. Ex. 1003 ¶¶ 81-83.

⁴ Patent Owner makes another attorney argument by alleging that page 38 of the Petition relies on prior art such as Chen, Ohsaki, and Shin to provide support for certain limitations. POR, 21. That argument seems to refer to a POSITA’s knowledge as reflected in Park, Fang, and Chen that it was “conventional for a

32. Referring to implementing Kim’s gate-stack-on-top disclosure (“each of top surfaces of the sacrificial layers SC1 to SC8, not the top surfaces of the insulating layers 111 to 118, may be partially exposed in the word line contact region WCTR,” Kim, [0090]), Dr. Campbell asserts that “[t]he proposed modification is neither simple nor straightforward.” Ex. 2009 ¶ 41. I disagree. At the outset, it may be helpful to clarify that the so-called “modification” refers to fabricating a gate-stack-on-top staircase instead of a dielectric-layer-on-top staircase starting from the bottom, not “modifying” a dielectric-layer-on-top staircase that is already fabricated. As I discussed above, for example, Chen demonstrates each option by *starting* with a staircase with each ordering. As explained in the previous section, these two

staircase structure to have a conductive structure on every step.” Pet., 38. The conclusory attorney argument does not contradict the clear teachings of these references. But even if they did not contain such clear teachings, claim limitation 1[e] (“each conductive structure is formed on the conductive layer of the *each* step”) does not require a conductive structure on *all* steps for two reasons. First, the ’711 Patent defines “each” to include the meaning of “each of a subset.” Ex. 1001, 5:6-8. Second, as explained in my Initial Declaration, a POSITA would read “comprising” to be open ended. Thus, a plurality of steps may correspond to some but not all of the steps of the staircase. Ex. 1003 ¶ 88.

configurations are simply predictable variations of a staircase structure. The “extensive modifications” that Dr. Campbell referred to are merely obvious adjustments to the structure or process that logically follow from putting the gate stack instead of the dielectric layer on the top of each step. These adjustments represent differences between the structure in the two configurations or the process used to fabricate them. Both layer-ordering configurations and their design and manufacturing were well known. In other words, Chen for example shows that a POSITA would have known how to build a staircase using either layer ordering from the substrate up. Thus, the reference to “modifications” is misleading.⁵ But in any case, because a POSITA would have known what is involved in building a staircase in either layer ordering from the substrate up, in the scenario where a POSITA starts with a dielectric-layer-on-top design and seeks to “modify” it to a gate-stack-on-top

⁵ Dr. Campbell also describes implementing the alternative order as “*replacing* a functional gate stack with insulating material and vice versa.” Ex. 2009 ¶ 41. That is similarly a misleading description for the same reason. There is no replacement of one layer with the other layer. It is simply structuring the staircase in the opposite order starting from the substrate. Indeed, Dr. Campbell testified that forming a gate-stack-on-top staircase simply means “start[ing] with the insulator rather than the sacrificial layer” and proceeding through the steps. Ex. 1027, 92:5-93:18.

design (an artificial scenario that Patent Owner and Dr. Campbell seem to construct), a POSITA would also know how to adjust the structure and the process to achieve this “modification.”

33. For example, one of the “modifications” Dr. Campbell refers to is the different depths of word line contacts. Ex. 2009 ¶ 41. The word line contacts have different depths (or heights) between the two layer orderings because the word line contacts need to reach their corresponding gate conductive layers, which occupy a different layer of the step in the two orderings. But the differences in depths can be easily accomplished by adjusting the etching and deposition time as required, resulting in holes and conductive structures of the appropriate depths. The adjustment to the etch time, for example, may simply be achieved by knowing the etch rate and the depth to which the holes are to be etched. Dr. Campbell’s testimony supports this understanding. Ex. 1027, 56:15-21 (“Q. How does one determine when to end an etching process -- a particular etching step? A. Well, the simplest scenario of sequences of this, the simple one is just to know your etch rate and time it, know the thickness.”).

34. Patent Owner alleges that the gate-stack-on-top configuration has an increased risk of over-etching. POR, 26. Preliminarily, I note that this is an attorney argument because the cites that follow it do not support this assertion. Dr. Campbell’s declaration at paragraph 54 merely discusses how structural differences

may affect the process and thickness of an etch-stop layer. It says nothing about over etching. My deposition testimony that Patent Owner cites addresses counsel's question on additional safety margin provided by additional layers and is unrelated to the risk of over etching of a gate-stack-on-top embodiment. *Id.*, 26 (citing Ex. 2008, 48:20-49:8).

35. In any event, this attorney argument is incorrect. The number of layers above the gate-stack layer is irrelevant to the risk of over etching the gate stack to cause short circuit. Regardless of the number of layers above the gate stack, the layer immediately above the gate stack must be *intentionally* etched to form a direct contact between the gate conductor layer and the word line contacts. Whether the layer immediately above the gate stack is an alternating dielectric layer (in the dielectric-layer-on-top embodiment) or an etch-stop or barrier layer (in the gate-stack-on-top embodiment), that layer has a uniform thickness and is etched via a well-controlled process. Furthermore, the risk of over etching due to, e.g., process variations may be mitigated using a technique called end-pointing, which Dr. Campbell testified about. Ex. 1027, 56:22-57:25. In end-pointing, the plasma produced by etching may be monitored for its chemical composition. Thus, over etching may be prevented by monitoring the plasma for the presence of the metal (e.g., tungsten) used to form the gate conductive layer. When tungsten is detected in the plasma, etching has reached the gate conductive layer and can be stopped.

This “most common” technique has “been around for 20 years, 30 years,” as Dr. Campbell testified. *Id.*, 57:12-25. Because techniques for preventing over etching were routine regardless of the layer ordering, Chen, as an example, only briefly discusses the formation of the conductive structures and does not differentiate between the two embodiments. Chen, [0057] (describing Figures 11A and 11B).

36. Dr. Campbell also includes “etch processes” such as “reoptimiz[ation]” of etch parameters in the alleged “extensive modifications.” Ex. 2009 ¶ 41. But as discussed in the last paragraph, etching contact holes in the gate-layer-on-top configuration is actually simpler because it does not require one more etch step to etch through the dielectric layer at the top of each step in the dielectric-layer-on-top configuration. Further, as Dr. Campbell himself testified, making adjustments to etch processes was routine to a POSITA. Ex. 1027, 106:23–107:10 (“*every time you do any deposition and etching, you have to*” “experiment to make [it] work.”). I testified that “specifics matter” and “details matter,” as Dr. Campbell cites. Ex. 2008, 40:20, 45:12 (cited in Ex. 2009 ¶ 41). But these are specifics and details that a POSITA would have well understood. They may involve many interacting or interrelated parameters that need to be adjusted to fabricate a staircase of the opposite layer order. But these are knobs that a POSITA would have known how to adjust. As an analogy, assembling a piece of IKEA furniture involves many details. There may be variations to the assembly and the parts needed (e.g., assembling a table that

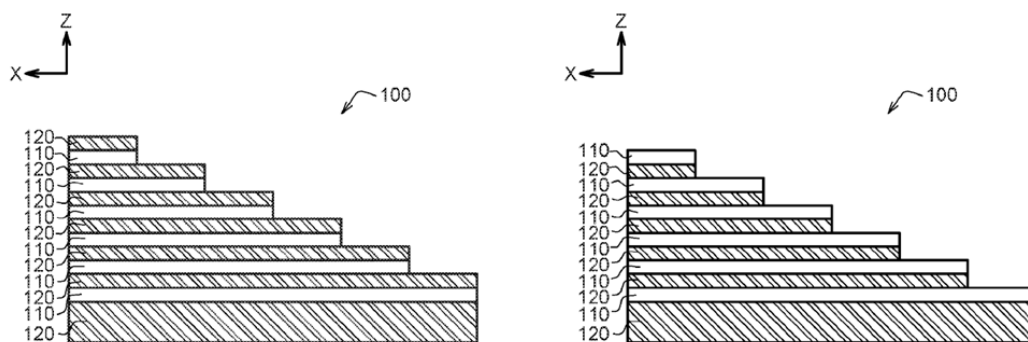
may be configured in one of several configurations such as different lengths or different shapes (rectangular or L-shaped, for instance)). But the assembly is not a “complicated” process because the steps are well known. Ex. 2009 ¶ 41.

37. Dr. Campbell alleges that changing the layer ordering “may also change the etch selectivity between the insulating layer above the sacrificial layers SC1-8 and sacrificial layers themselves such that the first stop layer 126a or the second stop layer 126b is not *needed*.” *Id.* I disagree for two reasons. First, two etch-stop layers provide additional protection that may be desirable in a cost-benefit analysis, trade-offs that are routinely evaluated in engineering. Second, a second etch-stop layer is not *needed* in either layer ordering. Chen plainly shows this by disclosing devices in both orders with one etch-stop layer (Figures 4A-4B) as well as devices in both orders with two etch-stop layers (Figures 7A-7B). Park also supports this conclusion. As I explained in my Initial Declaration, Park discloses the gate-stack-on-top variation for both the Figure 5/9 embodiment and the Figure 4/8 embodiment. Ex. 1003 ¶ 75 (citing Park, [0102], [0042]). Park’s Figure 5/9 embodiment has two etch-stop layers. The Figure 4/8 embodiment has one etch-stop layer. Thus, Park also demonstrates that both two etch-stop layers and one etch-stop layer are simply alternatives in both layer orderings. In fact, like Chen and Park, the ’711 Patent itself makes plain that the barrier layer is optional in the gate-stack-on-top configuration. Ex. 1001, cl. 1 (barrier layer), cl. 13 (no barrier layer). All of these references show

that Dr. Campbell is wrong to assert that “[a] POSITA would not use the stop pattern 126 if its function is not *needed* because a POSITA would not want to add the time or material to include a non-functional component” because they all show that a second etch-stop layer is not ever *needed*.

38. Dr. Campbell asserts that I made a mistake by including the lower gate insulating layer 11 in the modified Figure 22A because he asserts that the layer is “unnecessary” in the gate-stack-on-top embodiment. Ex. 2009 ¶ 42. I disagree. Dr. Campbell’s premise seems to be that a POSITA would not want to include an unnecessary layer due to the extra process and materials involved. But as explained in the last paragraph, that is a wrong premise. On this specific issue of the lower gate insulating layer, as a technical matter, including the lower gate insulating layer 11 in the gate-stack-on-top embodiment is a suitable choice. Dr. Campbell asserts that lower gate insulating layer 11 “prevent[s] ‘electrical crosstalk’ between the lowermost gate and the substrate.” *Id.* The level of reduction in electrical crosstalk is determined by, among other things, the distance and the material between the two components involved in the crosstalk, here, based on Dr. Campbell’s description, the distance and the material between the lowermost gate and the substrate. Adding a thin insulating layer between the two increases the distance and the amount of insulating material between them and improves the attenuation of crosstalk. Chen confirms this by showing an extra thick insulating layer 120 below the bottommost

gate conductive layer 110:



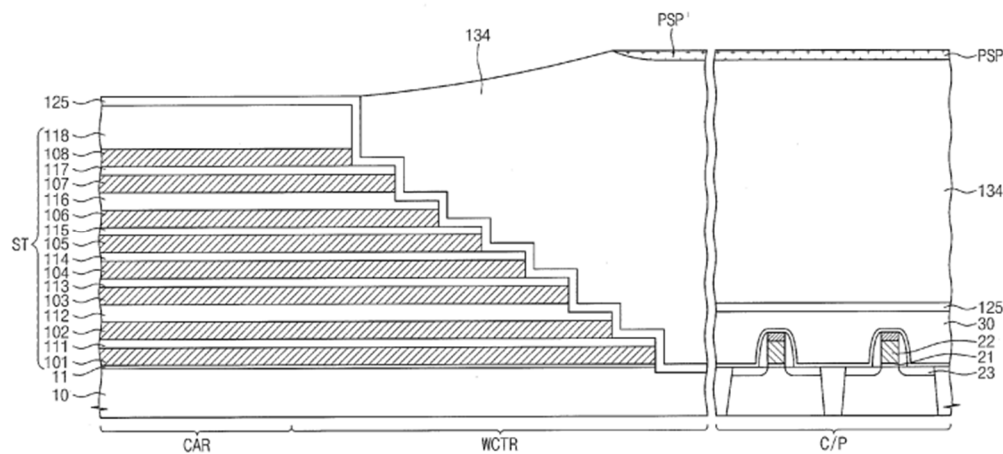
Chen, Figs. 9A-9B.⁶ This extra thick insulating layer reduces crosstalk to a greater extent than a thin insulating layer. Similarly, it is suitable to include that optional layer in the gate-stack-on-top embodiment to reduce electrical crosstalk to a greater extent. And whether this layer is present in a gate-stack-on-top embodiment, the staircase functions in a predictable manner.

B. Kim Renders Obvious Claims 14–15 Under Both the Correct Claim Construction and PO’s Incorrect Construction

39. Dr. Campbell asserts that Kim does not disclose the additional limitation of claims 14 and 15 because Kim’s etch-stop layer 126b directly contacts its barrier layer 126a, and thus the etch-stop layer 126b is not “directly on” a side surface and a top surface of each step as required by claim 14. I explain above why Dr. Campbell’s claim construction is incorrect. *Supra* § V.

⁶ This bottommost layer is an insulating layer 120. Chen, [0055]. It is not a substrate, which Chen omits from its disclosure. *See generally* Chen.

40. But even if Patent Owner’s claim construction were correct, Kim still renders obvious claims 14 and 15. Kim discloses, with respect to the Figure 17A-22B embodiment, a one etch-stop alternative and a two etch-stop alternative. Kim, [0185], [0187]. The etch-stop layer in the one etch-stop alternative “is formed on [i.e., directly contacting under Patent Owner’s construction] a side surface and a top surface of each step.” This can be observed through Kim’s Figure 34 embodiment, which shows a single etch-stop layer:



Id., Fig. 34. As shown, the etch-stop layer 125 directly contacts the side and top surfaces of the staircase. The one etch-stop alternative of the Figure 17A-22B embodiment has the same characteristic in this regard. This is consistent with my above explanation that two etch stops (or a “barrier layer” and an additional etch stop) or not necessary, but merely optional.

VII. GROUND 2

41. In my Initial Declaration, I noted that the Examiner took official notice during prosecution that the claimed etch-stop thickness “[wa]s notoriously well known in the art.” Ex. 1003 ¶ 129 (citing Ex. 1002, 156). Dr. Campbell did not respond to this.

42. Instead, Dr. Campbell’s testimony confirms the Examiner’s remark that the claimed 10 to 1000 nm thickness range lacks criticality. Ex. 1002, 156. Dr. Campbell testified that the typical staircase around the time of the patent is “about” or “a little more” than a micron. Ex. 1027, 31:19-25. A micron is 1000 nm, the upper limit of the claimed etch-stop thickness range. In other words, the claims allow an etch-stop layer about as thick as the staircase structure itself. Thus understood, the claims permit an etch-stop layer that is much, much thicker than the thickness suggested by the figures of the ’711 Patent (which figures do not limit the claims but are supposed to inform the reader of the invention).

43. The ’711 Patent itself makes plain to a POSITA that the 10 to 1000 nm range contains numerous subranges and accommodates a large variation of materials and device structures. To begin, it discloses that “[a] thickness of the etch-stop layer 310 can be in a range between 10 nm to 1000 nm (e.g., 10 nm, 20 nm, 30 nm, 40 nm, 50 nm, 60 nm, 70 nm, 80 nm, 90 nm, 100 nm, 200 nm, 300 nm, 400 nm, 500 nm, 600 nm, 700 nm, 800 nm, 900 nm, 1000 nm, any range bounded by the lower

end by any of these values, or in any range defined by any two of these values).”

Ex. 1001, 7:58-64. The nineteen exemplary values clearly indicate the indiscriminate nature of the range. They further permit hundreds of subranges “bounded by the lower end by any of these values, or in any range defined by any two of these values.” *Id.* A POSITA would understand the 10 to 1000 nm range merely represents a starting point within which a thickness is to be determined through routine design decisions and/or routine experimentation, as Dr. Campbell testified. Ex. 1027, 105:23-106:10.

44. Further, the large range can accommodate an etch-stop layer “made of any suitable insulating material that is different from the second insulating layer 208.” Ex. 1001, 7:64-66. Some exemplary materials include “silicon nitride, silicon oxynitride, spin-on-dielectric, and/or high-k dielectric films such as hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, or lanthanum oxide films.” *Id.*, 8:10-14.

45. More specifically, as to the claims themselves, claims 10 and 17 are not even limited to the exemplary materials because exemplary materials are recited in claims 5 and 16. And claims 5 and 10 both depend from claim 1; claims 16 and 17 both depend from claim 13. Thus, a POSITA would understand the claimed 10 to 1000 nm range applies to “any suitable insulating material that is different from the second insulating layer 208” beyond the list of exemplary materials. Ex. 1001, 7:64-

66.

46. Additionally, as I explained in my Initial Declaration, the '711 Patent claims the same 10 to 1000 nm thickness range whether or not a barrier is present in the device. Ex. 1003 ¶ 138. This “is an acknowledgement of a POSITA’s understanding that the barrier layer need not matter to the etch-stop thickness.” *Id.* By adjusting etching parameters, a wide range of thickness is suitable for the etch-stop functionality. Such adjustment is routine and well within the knowledge and skill of a POSITA, as Dr. Campbell testified. Ex. 1027, 105:23-106:10 (“The range that’s given [in the '711 Patent] is a place to start doing experiments to determine the actual thickness that you would need.”); 106:23-107:10 (“*every time* you do *any* deposition and etching, you have to” “experiment to make [it] work.”).

47. Moreover, the claimed thickness range is presumably sufficient to protect against any suitable variation of contact hole depths. But, as explained in my Initial Declaration, the '711 Patent does not limit or even disclose the height of the staircase or the number of steps. Ex. 1003 ¶ 191. This again indicates that the inventors considered the claimed range to be adequate for any suitable staircase structures and heights, such that it is unnecessary to specify the height of the staircase (which is roughly the same as the maximum depth of contact holes) that the etch-stop thickness is good for, even though, as Dr. Campbell testified, the height is an important consideration for the etch resistance and thus thickness of the etch-stop

layer. Ex. 1027, 87:20-25.

48. Next, as I testified in deposition, Fang's disclosed 5-100 nm thickness range similarly lacks criticality. Ex. 2008, 54:12-18. Fang's range is suitable for "any material that is not substantially removed (e.g., etched) during removal and replacement of the nitride materials of the staircase structure." Fang, [0020] (numerals omitted). For example, the same range applies regardless of the carbon-doping composition. Ex. 2008, 53:8–54:2. Such a range lacking criticality swallows up any minor differences between Kim and Fang that Dr. Campbell alleges are inconsistent with a motivation to apply Fang's etch-stop thickness to Kim.

49. It is worth noting that Kim's etch-stop has an inherent thickness. Fang simply specifies a suitable range that a POSITA would have desired to know, as Dr. Campbell acknowledged. Ex. 1027, 56:15-21. Fang's large range is a suitable range independent of the minor differences between Kim and Fang. But as I further explain in the sections below, those alleged differences are not actual differences or are irrelevant to applying Fang's etch-stop thickness range to Kim (or Park).

A. Fang's Carbon Doping Is Optional and Immaterial to the Obviousness Analysis

50. Dr. Campbell opines that the difference in the etch-stop materials between Kim and Fang would not have motivated a POSITA to apply Fang's thickness range to Kim. Ex. 2009 ¶ 48. The first two differences he alleges are based on his assertion that Fang uses carbon-doped silicon nitride, and Kim does

not. *Id.* ¶¶ 49-50. But that is not a necessary or material difference, as I explain below. The third difference is the alleged difference between Kim and Fang’s focuses. *Id.* ¶¶ 52-53. This difference is based on a mischaracterization of Kim’s etch-stop layer, which I also explain below.

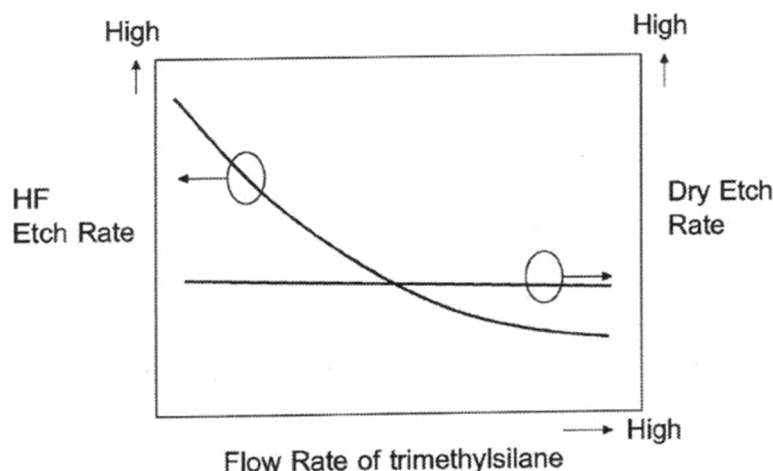
51. Kim and Fang can use the same or similar material for the etch-stop layer. Kim teaches “a second stop layer 125 b having an etch selectivity with respect to the insulating layers 111 to 118.” Kim, [0187]. Fang similarly permits “any material that is not substantially removed (e.g., etched) during removal and replacement of the nitride materials of the staircase structure.” Fang, [0020] (numerals omitted). Fang discloses carbon-doped silicon nitride “[b]y way of example only.” *Id.* It discloses a thickness range for the etch-stop layer in the paragraph immediately after that statement. *Id.*, [0020]-[0021]. The specified thickness range makes no reference to carbon doping. *Id.*, [0021]. Accordingly, a POSITA would have understood that the range applies to the “any [suitable] material,” not just carbon-doped silicon nitride. *Id.*, [0020]. Fang’s wide thickness range, spanning a factor of 20, confirms it is not specific to “carbon-doped silicon nitride” and makes it appropriate for any suitable materials that can be used for the etch-stop layer in light of the flexibility of etch chemistry and methodology.

52. Dr. Campbell’s assertion about the combination of materials is based on his mistaken understanding that Fang’s thickness is only for carbon-doped silicon

nitride. Ex. 2009 ¶ 50. Additionally, the sacrificial layer material is irrelevant to the etch-stop layer thickness because of the intervening barrier layer. As Dr. Campbell testified, an etch stop protects the immediately adjacent layer from the etchant (in the forward direction of etchant flow). Ex. 1027, 23:4-8. Thus, when a barrier layer is present between the sacrificial layer and the etch-stop layer, it is the combination of materials of the barrier layer and the sacrificial layer that matters. *See id.*, 97:2-10. That is why, for the configuration having only one etch-stop layer, Kim discloses etch selectivity between the sacrificial layer and the etch-stop layer. Kim, [0187] (“In other embodiments, the etch stop layer 125 may be a single layer, which is formed of a material having an etch selectivity with respect to the sacrificial layers SC1 to SC8 and the insulating layers 111 to 118.”). But for the configuration with two etch-stop layers, Kim discloses etch selectivity between the sacrificial layer and the first (lower) etch-stop layer 125a, i.e., the barrier layer. *Id.* (“the etch stop layer 125 may include a first stop layer 125a having an etch selectivity with respect to the sacrificial layers SC1 to SC8 and a second stop layer 125b having an etch selectivity with respect to the insulating layers 111 to 118.”).

53. Even if Fang required carbon-doped silicon nitride as Dr. Campbell incorrectly opines, the carbon doping does not affect the etch-stop thickness. As he testified, it is the relative etch rates or etch selectivity between the etch-stop layer and the insulator layer above it that matters. Ex. 1027, 23:9-17, 97:2-10. As Fang

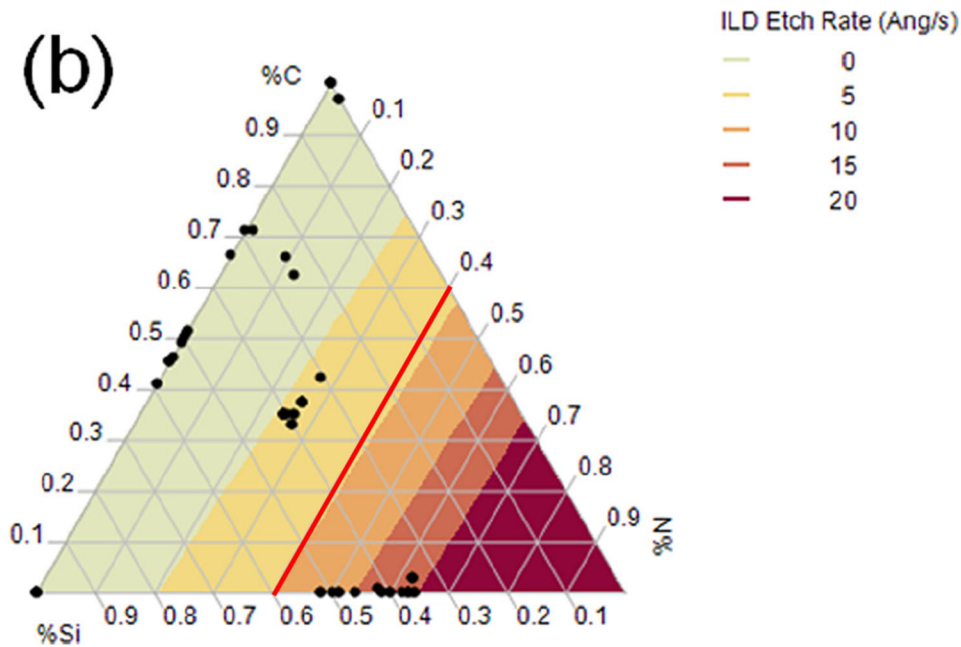
discloses, the contact holes through the insulator layer are formed using dry etch chemistries. Fang, [0020]. This is because dry etch can be highly directional (known as “an anisotropic etch process”), which is needed for etching holes with high aspect ratios. *Id.*, [0028]; Kim, [0070], Ex. 1027, 24:2-25:18. Thus, the dry etch rate of the etch-stop layer affects the thickness that is appropriate to protect the staircase from over-etching. But as this figure below shows, the dry etch rate is constant for varying amounts of carbon doping. This figure “is a chart showing the relationships between a carbon-doped amount in a silicon nitride film (the flow rate of trimethylsilane) and etch rates (wet and dry).” Ex. 1029, [0035]. The changing level of carbon doping indicates a nonstoichiometric silicon carbon nitride. *Id.*, [0064]; Fang, [0017] (“The carbon-doped silicon nitride differs from silicon carbon nitride (SiCN), which includes a stoichiometric amount of carbon, such as $\text{Si}_{1.5}\text{C}_{1.5}\text{N}_4$.”).



Ex. 1029, Fig. 19. The figure shows level of carbon doping on the horizontal axis. The dry etch rate is represented by the right vertical axis. The horizontal line across

the plot, indicating a constant, shows the dry etch rate of silicon nitride at different levels of carbon doping (the oval with an arrow to the right confirms that the horizontal line represents the dry etch rate). *Id.*, [0074] (“The silicon nitride films have substantially the same dry etch rates, regardless of their ratios of the flow rate of trimethylsilane.”). Thus, even assuming the addition of carbon doping to Fang’s etch-stop layer, the thickness of Fang’s etch stop and the corresponding over-etch protection it provides is directly applicable to Kim’s silicon nitride etch-stop because the carbon doping has no impact on the dry etch rate.

54. This phenomenon was well known in the art for silicon-nitride-based materials. For example, Dhungana shows a constant etch rate for ILD (interlayer dielectric above an etch-stop layer) for nonstoichiometric silicon carbon nitride ($\text{a-SiC}_x\text{N}_y\text{:H}$) across different levels of carbon doping, as shown via diagonal lines connecting constant Si and N levels. The red diagonal line represents 40% nitrogen and 60% silicon, the approximate weight composition of silicon nitride Si_3N_4 :



Ex. 1032, Fig. 12(b). As shown, the ILD etch rate is yellow (5 angstrom per second) along the Si_3N_4 tie line, showing that the etch rate remains constant across different carbon doping levels (represented by the axis on the left side of the triangle).⁷ This etch rate is based on a CHF_3 plasma, i.e., a dry etch. *Id.* at 2, 4; *see also* Ex. 1001, 10:26-28 (“the selective etching includes anisotropic dry etching using chemical etchant such as, for example, ... CHF_3 ... and/or other suitable etchants.”).

55. Dr. Campbell asserts that my statement that Fang’s etch-stop layer “may comprise ... silicon nitride” is incorrect. Ex. 1003 ¶ 130 (cited in Ex. 2009

⁷ The weight composition of silicon and nitrogen in the composite material decreases with increasing amount of carbon doping. But the dry etch rate remains constant across the level of carbon doping as the color-coded areas indicate.

¶ 51). To the contrary, my statement is correct in context. Fang itself refers to the etch-stop layer as silicon nitride: “the etch stop material is a silicon nitride material, such as a carbon-doped silicon nitride material.” Fang, [0008]; *id.*, [0025] (“both the nitride materials 120 of the staircase structure 105 and the etch stop material 130 are silicon nitride-based”). My Initial Declaration simply made the point that “Kim’s and Fang’s etch-stop layers are similar.” Ex. 1003 ¶ 130. In that context, “small percentages” of carbon doping do not make a meaningful difference. Ex. 2008, 52:18–54:2. The above discussion on the dry etch rate, for example, demonstrates this.

56. Next, Dr. Campbell alleges that Kim and Fang’s different focuses would not have provided motivation for a POSITA to apply Fang’s thickness range to Kim. Ex. 2009 ¶¶ 52-53. I disagree. Dr. Campbell incorrectly characterizes the use of Kim’s etch-stop layer 125 as merely protecting the contact pads. *Id.* ¶ 52. If that were the case, the etch-stop layer simply needs to be formed over the top-level surface of the staircase because chemical mechanical polishing (“CMP”) only polishes the top surface and cannot damage materials below the surface, as Dr. Campbell acknowledges. Ex. 1027, 61:23-62:2. Since CMP and the related dishing phenomenon cannot damage underlying layers, a POSITA would have understood Kim’s etch-stop covering the entire staircase to provide over-etching protection when contact holes are etched. Without that function, a POSITA would not design

Kim's etch-stop layer to cover the entire staircase because, according to Dr. Campbell, "a POSITA would not want to add the time or material to include a non-functional component." Ex. 2009 ¶ 41. For example, Park's Figure 11 shows an etch-stop layer covering only part of the staircase. Regardless, the etch-stop layer is present on the steps, it functions as an etch stop on the step, just like Fang. Therefore, Kim's etch-stop layer has the function of Fang's etch-stop layer.

B. The Wide Etch-Stop Thickness Range and Etch-Chemistry Flexibility Render Kim and Fang's Structural Differences Immaterial

57. Dr. Campbell alleges that structural differences between Kim and Fang would not have motivated a POSITA to apply Fang's etch-stop thickness to Kim. Ex. 2009 ¶ 54. Specifically, he identifies Kim's inclusion of a high-k dielectric layer, Kim's inclusion of an underlying etch-stop layer, and Kim and Fang's opposite layer orderings as the relevant structural differences. *Id.* ¶ 55. I disagree.

58. As Dr. Campbell testified, an etch-stop layer "provides its protective function relative to the etching of the layer that's immediately above it." Ex. 1027, 23:4-8; *see also id.*, 41:2-6 (similar). Therefore, when either the high-k dielectric layer or the lower of two etch-stop layers is functioning as an etch stop, it is to protect its underlying layer against over etching during the etching of the layer above it, i.e., the barrier layer (when present) immediately above the high-k dielectric layer, or the etch-stop layer immediately above the high-k dielectric layer (when the barrier layer

is absent) or the barrier layer (when present). In other words, these additional barrier and high-k dielectric layers in Kim that are not in Fang do not function as an etch stop when the insulating layer above the etch-stop layer is etched. Therefore, these additional layers have little bearing on the etch-stop thickness, which protects against over etching when the insulating layer above the etch-stop layer is etched.

59. Although these additional layers can serve as an etch stop during the etching of the insulating layer above the etch-stop layer if over etching occurs and the etch-stop layer is etched away, they merely provide a backup safety margin that a POSITA would not rely on to reduce the etch-stop thickness, as Dr. Campbell alleges. For example, the high-k layer “tend[s] to be very thin” and merely provides a little bit of extra margin against punch-through. Ex. 2008, 48:2-19. Again, Fang’s range spanning a factor of 20 represents a loose range that accommodates various conditions. *See Id.*, 54:19-55:2. Thus, the small additional safety margin provides additional insurance against punch-through rather than making Fang’s disclosed thickness range unsuitable for Kim.

60. The extra etch-stop layer has no impact on the etch-stop thickness range for an additional reason, as shown by the ’711 patent itself. The patent specifies the same thickness range whether or not a barrier layer (i.e., an additional etch-stop layer) is present. Ex. 1001, cls. 10, 17. This thickness range is not something novel that was taught by the ’711 Patent, as the Examiner observed. Instead, it is simply

a range lacking criticality. Relatedly, Patent Owner argues that the '711 Patent disclosure is irrelevant because “the '711 Patent specifies a *range* of thickness....” POR, 40 (emphasis in original). Patent Owner, however, overlooks that Fang also discloses a range, 5-100 nm. Ex. 1003 ¶ 130. Thus, Patent Owner’s argument relies on a non-distinction.⁸

61. Dr. Campbell argues that “the use of multiple etch-stop layers would require a different etch process than Fang’s single layer design.” Ex. 2009 ¶ 55. But that “different etch process” is irrelevant to the etch-stop thickness. Again, the etch-stop layer functions as an etch stop during the etching of the insulating layer above it. Ex. 1027, 23:4-8. The thickness of the etch-stop layer is based on the etching of that insulating layer above, to slow down etching when the layer above has been completely etched and the etchant reaches the etch-stop layer. It needs to be thick enough to protect its underlying layer. But the barrier layer (or Kim’s first stop layer 126a) functions as an etch stop when the *etch-stop layer* is *intentionally* etched. *Id.*, 44:19-23 (“Q. And would you agree that the barrier layer also has an etch-stop property with respect to the etch-stop layer? A. Yes, that’s exactly what it does.”);

⁸ I note again that this appears to be another attorney argument as Patent Owner does not cite Dr. Campbell for support. POR, 40. I do not find this argument in Dr. Campbell’s declaration.

54:5-17. Thus, the presence or absence of the barrier layer has no impact on the etch-stop thickness, because that is determined by the need to prevent over-etching during the etching of the upper insulating layer. Kim's etch-stop layer 126a does not reduce the required thickness of the etch-stop layer 126b because that thickness protects against the etching of the insulating layer 134.

62. Lastly, Dr. Campbell alleges that reversing the layer ordering “impact[s] manufacturing and etch-processes.” Ex. 2009 ¶ 55. He does not explain how such changes impact the etch-stop thickness. Nor can I think of a cause-and-effect relationship between the two. Chen supports this conclusion. Chen discloses both gate-layer-on-top and dielectric-layer-on-top embodiments. Chen, Figs. 7A-7B. But in its discussion on etch-stop thickness, Chen makes no distinction between the two embodiments. *Id.*, [0047]-[0053]. Further, the shorter contact holes in the gate-layer-on-top embodiment reduce the risk of over-etching when the etch-stop thickness is kept constant because etching shorter contact holes requires less time, leaving more etch-stop margin. A POSITA would have understood this to provide an additional safety margin and would not change the thickness. Further, this additional safety margin (or, alternatively, the extra thickness) is insignificant. For example, the difference in the depths of the deepest contact hole for a 32-step staircase between the two layer orderings is less than 2% (31 steps versus 31.5 steps, assuming the alternating layers and the steps have uniform thickness). Ex. 1027,

85:13-25 (identifying 32-step staircase structures in 2017). A POSITA would find desirable an extra 2% safety margin rather than to reduce the etch-stop thickness by 2% in a cost-benefit analysis because the consequence of not having enough safety margin outweighs any benefits provided by a 2% reduction in etch-stop thickness.

C. PO's Recycled Expectation-of-Success Argument Fails

63. Patent Owner argues against a reasonable expectation of success in applying Fang's etch-stop thickness to Kim. POR, 41-42. I note that Dr. Campbell's declaration does not offer an opinion on this issue. Instead, Patent Owner cites Dr. Campbell's opinion alleging different etch-stop materials between Kim and Fang. *Id.*, 42 (citing Ex. 2009 ¶¶ 41, 51). I have refuted those allegations above.

64. In any event, Fang's 20x thickness range is designed to accommodate a wide range of conditions. Such a wide range ensures its successful application to Kim. The similarities in Kim and Fang's devices create a reasonable expectation of success considering the lack of criticality of the 20x range. Ex. 1003 ¶¶ 135-137.

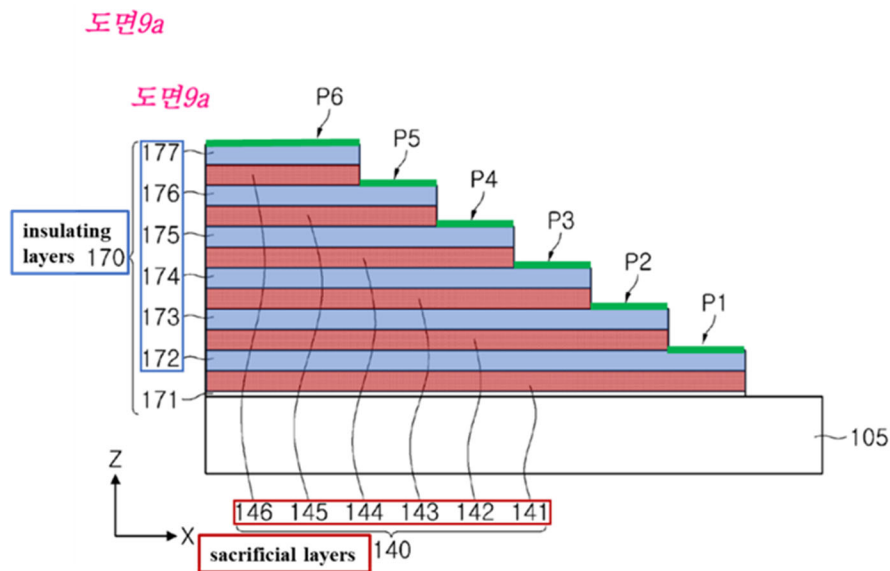
VIII. GROUND 3

A. Park Renders Obvious "Each Step Comprises a Gate Stack Disposed Over a Dielectric Layer"

65. As I described in my Initial Declaration, Park discloses placing the sacrificial layer (which is replaced by the gate stack during the fabrication process) as the top layer of each step. Ex. 1003 ¶ 75. Park discloses:

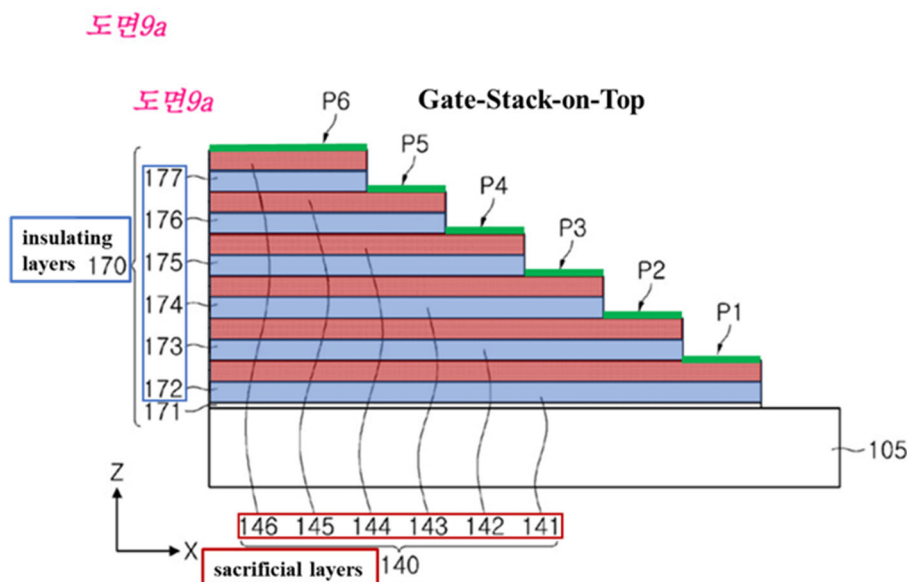
In addition, a portion of the top surface of each insulating layer (170) may be exposed by the plurality of pad regions (P1-P6), and, unlike what is shown in FIG. 9a, a portion of the top surface of each sacrificial layer (140) may be exposed in a plurality of pad regions (P1-P6).

Park, [0102]. The first part of this quote (“a portion of the top surface of each insulating layer (170) may be exposed by the plurality of pad regions (P1-P6)”) describes what is shown in Figure 9a, where a portion of the top surface of each insulating layer (170) (indicated by a green line) is exposed by the plurality of pad regions (P1-P6):



Id., Fig. 9a. The second part of this quote (“a portion of the top surface of each sacrificial layer (140) may be exposed in a plurality of pad regions (P1-P6)”) describes the figure below, in which the sacrificial layer is the top layer of each step,

where a portion of the top surface of each sacrificial layer (140) is indicated by a green line:



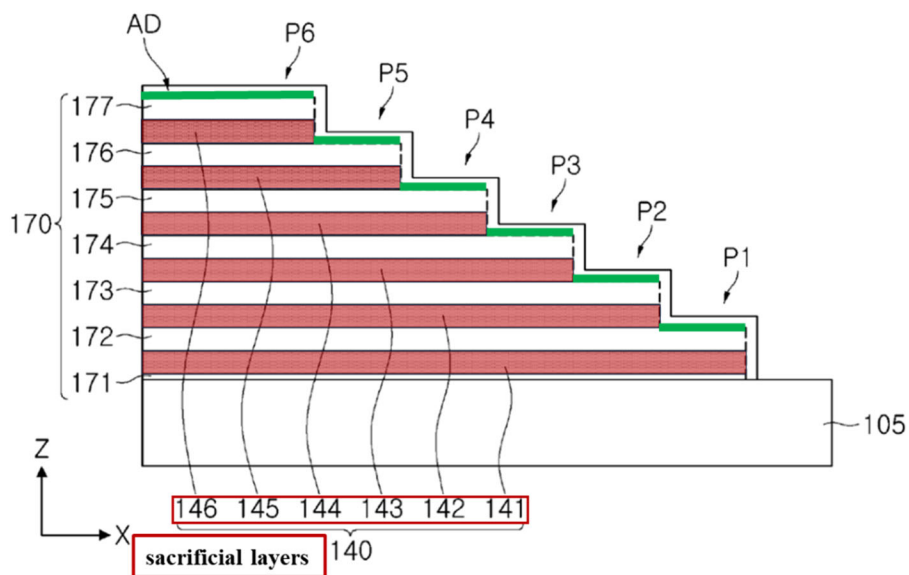
Id., Fig. 9a (modified). The phrase “unlike what is shown in FIG. 9a” between the two portions of the quote supports this understanding that the two parts of the quote describe opposite layer orderings.

66. Dr. Campbell asserts that the quoted passage “explicitly teaches that a portion of the top surface of each insulating layer *and* sacrificial layer may be exposed in a plurality of pad regions.” Ex. 2009 ¶ 58 (emphasis in original). He asserts that “[t]his could occur, for example, if the etch process is alternated between sacrificial and oxide layers.” *Id.* This explanation is nonsensical because the etch process is already alternated between the two layers in Figure 9a. He simply hasn’t shown what a staircase that has “a portion of the top surface of each insulating layer *and* sacrificial layer ... exposed in a plurality of pad regions” looks like. *Id.*

(emphasis in original). I cannot visualize such a staircase in a practical implementation. In any event, that is not what Park teaches.

67. Relatedly, Patent Owner's speculation⁹ that Park's disclosure means "both insulating layers 170 and sacrificial layers 140 may be 'exposed' in the pad regions P1-P6 (as shown in Figure 9b)" has no merit. POR, 44. Figure 9b does not show exposed sacrificial layers:

도면9b



Park, Fig. 9b.

⁹ This is yet another attorney argument as Dr. Campbell's declaration does not address it.

1. Park's embodiments are properly combined

68. Dr. Campbell argues that a gate-stack-on-top configuration of Park would not have been obvious in light of a POSITA's knowledge. But, first of all, as explained above, Park expressly discloses this configuration for the Figure 9 embodiment. But even if the Ground were to involve the combination of the Figures 4/8 embodiment and the Figures 5/9 embodiment, Dr. Campbell's arguments are still incorrect.

69. I note that many of Dr. Campbell's arguments are the same as those asserted against Kim. For example, paragraphs 41 and 43 (Kim) and 64 to 65 (Park) basically make the same arguments. Therefore, they are incorrect for the same reasons. *See supra* § III.A. I address those arguments that may be specific to Park in this section.

70. Dr. Campbell asserts that because Figures 5/9 include etch-stop layers while Figures 4/8 do not, "the steps are precisely where those embodiments differ." Ex. 2009 ¶ 62. I disagree. Contrary to Dr. Campbell's assertion, the etch-stop layers are not part of the steps. As Patent Owner extensively cites to support its claim construction argument, Patent Owner agreed with my Initial Declaration that "'step' ... refer[s] to the underlying staircase structure made up of a gate stack and dielectric layer, **not** the additional layers placed on top of that structure," such as the etch-stop layers. POR, 11-12. Thus, Dr. Campbell's and Patent Owner's assertions contradict

each other on whether the etch-stop layer is part of the steps.

71. Patent Owner argues that “Park makes clear that when disclosures apply to different embodiments, it discloses that explicitly.” POR, 45-46 (citing Park, [0104]).¹⁰ I disagree. First, I identified in my Initial Declaration Park’s disclosure that a POSITA would have understood as indicating that “descriptions of one of Park’s embodiments apply to other embodiments except where the embodiments differ.” Ex. 1003 ¶ 77. Second, Park paragraph 104 refers the discussion of channel formation back to the Figures 4/8 embodiment. Park, [0104]. A POSITA would have understood this cross-reference to serve the purpose of avoiding duplicative descriptions. This single express cross-reference would not have changed a POSITA’s understanding that other descriptions of the staircase of

¹⁰ This appears to be yet another attorney argument. Although the argument appears in a paragraph that cites paragraph 62 of Dr. Campbell’s declaration, that citation supports Patent Owner’s argument in the second half of the paragraph regarding the alleged differences between the embodiments. That citation to paragraph 62 of Dr. Campbell’s declaration does not support this argument that cross applicability between embodiments requires an explicit disclosure because, for example, Dr. Campbell does not cite Park paragraph [0104] that Patent Owner uses to support its argument.

Figures 4/8 apply to Figure 5/9 because of their similarities, including the use of common reference numerals, as I explain above. In any event, the teaching of layer-ordering reversal for the Figure 4/8 embodiment merely *adds to* the obviousness of the layer-order reversal because the description of the Figure 5/9 embodiment contains the same disclosure. *Id.*, [0102].

B. Park Renders Obvious Claims 14–15 Under the Correct Claim Construction and PO’s Incorrect Construction

72. Dr. Campbell first argues that Park does not satisfy claims 14 and 15 for the same reasons that Kim does not. Ex. 2009 ¶¶ 66, 68-70. I address above why Dr. Campbell is incorrect. *See supra* § III.B.

73. Even if Patent Owner’s claim construction were correct, Park still renders obvious claims 14 and 15. Park’s Figures 4/8 embodiment shows that its first stop layer 110a is optional. As shown in the figures below, the Figures 4/8 embodiment and the Figures 5/9 embodiment simply differ in the number of etch-stop layers. All other components are the same and are designated using the same reference numerals:

FIG. 4

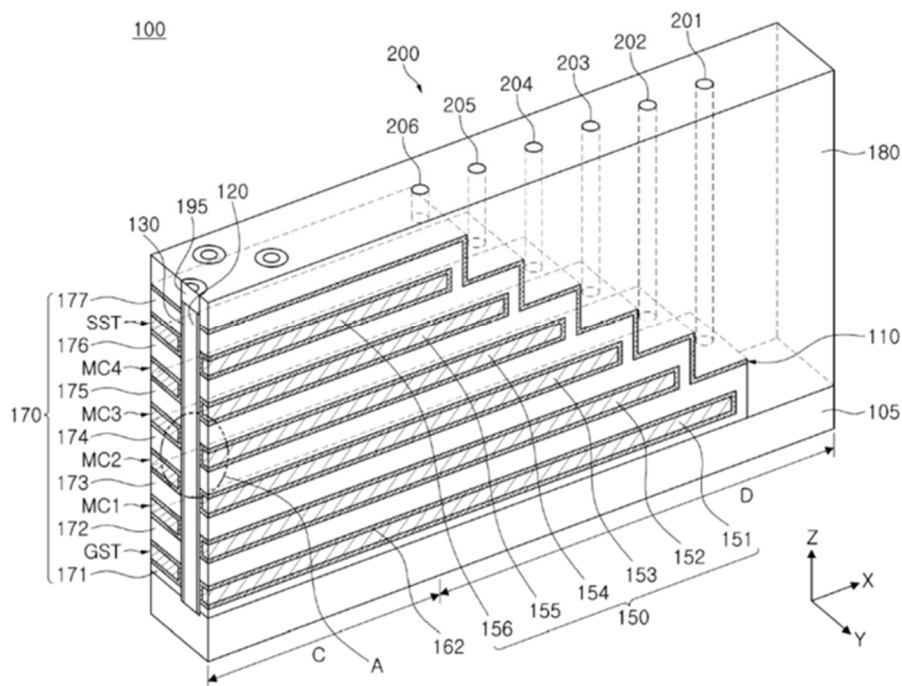
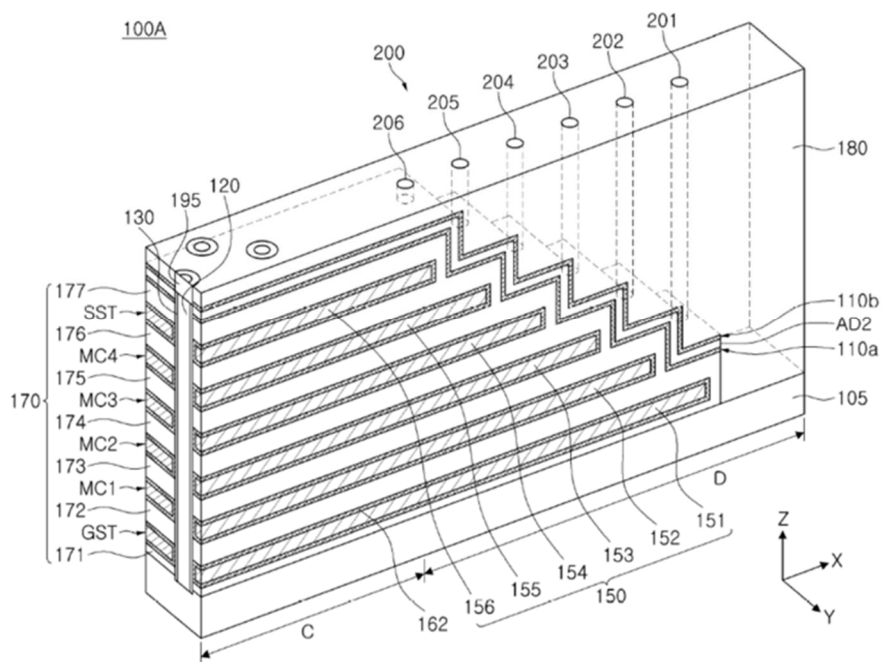


FIG. 5



Park, Figs. 4, 5; *see also id.*, [0049] (“FIG. 5 is a perspective view illustrating a nonvolatile memory device (100A) according to *another embodiment of FIG. 4.* ...

[Numerous listed components] are the same as FIG. 4. However, in the embodiment shown in FIG. 5, a plurality of etch-stop layers (110a, 110b) is provided....”); Ex. 2009 ¶ 64 (identifying only the number of etch-stop layers as the difference between the two embodiments). In the Figure 5/9 embodiment without an optional second etch-stop layer, the etch-stop layer directly contacts the side and top surfaces of each step as required under Patent Owner’s claim construction.

74. Next, Dr. Campbell argues that “Park does not disclose etch-stop layer on the side surface of *each* of its steps” because the etch-stop layer does not cover the side of the bottommost step. Ex. 2009 ¶ 67. This argument ignores what the ’711 Patent itself discloses. The ’711 Patent defines “each”: “In the present disclosure, the term ‘each’ may not only necessarily mean ‘each of all,’ but can also mean ‘each of a subset.’” Ex. 1001, 5:6-8. Accordingly, *each* step of claim 14 need not include *all* steps of the staircase.

C. Park Renders Obvious Claim 15

75. Dr. Campbell alleges that Park does not disclose a uniform etch-stop thickness on the side and top surfaces as required by claim 15. Ex. 2009 ¶ 71. I disagree. Park repeatedly refers to “*the* thickness of the etch-stop layer.” Ex. 1003 ¶ 176. Furthermore, Figures 4, 5, 8, and 9 all show uniform etch-stop thickness. Thus, a POSITA would have understood to Park to disclose a uniform etch-stop thickness (which, as I discuss below, is consistent with Park’s discussion of forming

these layers).

76. Ignoring Park's disclosures, Dr. Campbell argues that Park's method of forming a sacrificial etch-stop layer and then replacing it with the final etch-stop layer, in contrast to Kim's method of directly forming the final etch-stop layer, makes it not obvious that the etch-stop thickness is uniform. Ex. 2009 ¶ 71. I disagree. The final etch-stop layer has the same shape as the sacrificial etch-stop layer it replaces. And the sacrificial etch-stop layer is formed using the same method as the etch-stop layer in Kim, by depositing the layers from above the staircase structure. *Compare* Park, Figs. 9b-9c *with* Kim, Fig. 17A; *see also* Park, [0103]-[0104]. Therefore, Park's final etch-stop layer would have the same shape as if it were deposited from above the staircase structure, which would have uniform thickness on the side surface and the top surface as Kim does, a point Dr. Campbell does not dispute.

77. Moreover, a uniform thickness on both the side and the top would have been obvious by using the conventional atomic layer deposition ("ALD") technique, which Park uses. Park, [0086], [0092]. As the name suggests, this method deposits materials one atomic layer at a time. As Dr. Campbell agrees, there is "extraordinary control over the thickness [using ALD], and [one is] able to deposit into areas that are very difficult to get uniform films otherwise." Ex. 1027, 66:17-24. ALD conforms to the shape of a structure: the dielectrics will fill the opening left by removing the sacrificial etch-stop layer to a uniform thickness. In other words, not

only is ALD a suitable method to form Park's final etch-stop layer during replacement, but it is also the desirable method to deposit into the serpentine shape opening "to get uniform films" on both the side and top surfaces. *Id.* In fact, Dr. Campbell concedes that "side openings T2 are back-filled with etch-stop material using an ALD or CVD process to form etch-stop layer 110a and 110b." Ex. 2009 ¶ 75.

IX. GROUND 4

A. The Petition Shows Motivation to Combine Park and Fang

1. Dependent claim 7

78. In my Initial Declaration, I explained that the materials above the topmost horizontal surface of the etch-stop layer may be removed, forming a coplanar surface between the conductive structures, the insulating layer, and a portion of the etch-stop layer. Ex. 1003 ¶ 182-86. Dr. Campbell asserts that the insulating layer above the topmost horizontal surface of the etch-stop layer (the "extra material") is needed during Park's fabrication steps of replacing sacrificial etch-stop with the final etch-stop layer. Ex. 2009 ¶¶ 80-81. Because, under Dr. Campbell's argument, the extra material is needed during the replacement of the sacrificial etch-stop layer, removing the extra material after that replacement would moot his argument because the extra material would then still be present during the replacement, at the time Dr. Campbell asserts that it is needed.

79. Park suggests a second planarization step to remove the extra material. *See* Park, [0089] (“Next, a planarization process can be performed ... and a material that constitutes a conductive layer (195) can be deposited ... *Again*, a planarization process may be performed....”). This second planarization process further ensures a planar top surface before the connecting lines 220 are formed thereon in the last step of the process. *Id.*, [0110], Fig. 9j. It also results in a coplanar surface. *Pet.*, 94–97. These benefits and removing the extra material to achieve a smaller size would have motivated a POSITA to perform this second planarization process.

80. Dr. Campbell argues that performing this second planarization process “would risk damaging the channel structure 130 and conductive layer 195.” *Ex.* 2009 ¶ 81. I first note that he states “risk,” i.e., Dr. Campbell does not appear to suggest that the second planarization process would certainly damage these structures. To the extent he suggests there is a substantial “risk” of damage, however, I disagree. It was conventional by the time of the ’711 Patent to complete a CMP step with intentionally formed protruding structures. For example, Wang teaches performing a first CMP step to create a planar surface:

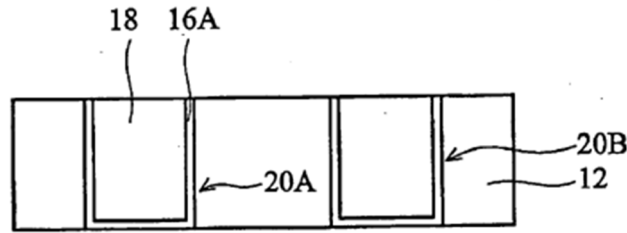


FIG. 1D

Ex. 1030, Fig. 1D, [0018]. Then, Wang further teaches “a second CMP process” “to selectively remove a thickness portion of the dielectric layer 12 upper surface to leave an upper portion of the damascene structures e.g., 20A, 20B, including barrier layer 16A sidewall portions, protruding (extending) above the surface of the dielectric layer 12.” *Id.*, [0019]. This results in the structure below:

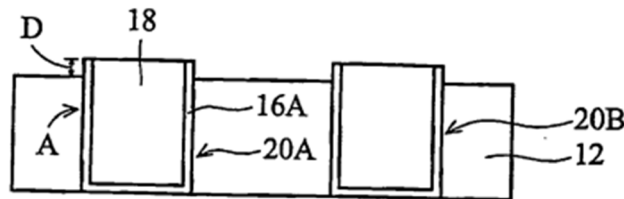


FIG. 1E

Id., Fig. 1E. As Figure 1E shows, the second CMP step intentionally creates a protruding structure.

81. As Wang illustrates, forming a planar top surface is a standard, selectivity-controlled operation in the process of fabricating a 3D memory device. Risk management was routine. A POSITA would have known how to planarize a top surface without damaging adjacent structures. To the extent that Dr. Campbell’s is asserting that damage would occur, Wang shows that a POSITA would have

known to mitigate any damage to the channel structure 130 and conductive layer 195 while performing the second planarization process, which Park evidently assumes to be true in suggesting the second planarization process.

82. Dr. Campbell asserts that my deposition testimony shows a fundamental misunderstanding of Park's design and method of manufacturing the etch-stop layers. Ex. 2009 ¶ 78. Dr. Campbell is mistaken. The key concept of my testimony is that Park's sacrificial etch-stop layers *correspond* to the barrier layer and the etch-stop layer of the '711 Patent. Ex. 2008, 69:1-11. Dr. Campbell asserts that I testified that "sacrificial layers 115a and 115b of Park *map* to the '711 Patent's barrier layer and etch-stop layer, respectively." I did not. *See generally* Ex. 2008.

2. Dependent claims 10 and 17

83. Dr. Campbell largely repeats his argument against applying Fang's etch-stop thickness to Kim in this section. For example, his arguments in paragraphs 54-55 (Kim) and 83-85 (Park) are basically the same. Therefore, his arguments are incorrect for the same reasons I explain with respect to Kim. *Supra* § VII.

84. My Initial Declaration explained that Park discloses both one- and two-etch-stop-layer embodiments but "makes no distinction regarding the thickness of its etch-stop layer based on the number of etch-stop layers in the embodiment." Ex. 1003 ¶ 201. Dr. Campbell asserts that is expected since "Park does not specify *any* etch-stop layer thickness." Ex. 2009 ¶ 85 (emphasis in original). That is factually

incorrect. Park specifies etch-stop thickness in numerous places. *See, e.g.*, Park, [0006] (“The thickness of the etch-stop layer may be less than or equal to two times the thickness of the gate insulating film.”); [0060], [0067], cl. 3 (similar). Claim 3 of Park specifies that “the thickness of the etch-stop layer is less than or equal to two times the thickness of the gate insulating films.” And claim 3 depends from claim 1, which requires “at least one etch-stop layer,” i.e., one or more etch-stop layers, each having the same thickness relative to the thickness of the gate insulating films. Park also discloses embodiments that have different numbers of etch-stop layers on different steps. *Id.*, Fig. 11 (etch-stop layer 110b covering only the four bottommost steps), Fig. 13 (two etch-stop layers in the middle four steps and one layer in the other steps); [0051] (describing the same). But Park does not teach or suggest changing the thickness of the etch-stop layer based on that difference. In other words, Park’s etch-stop thickness, like Fang’s, is insensitive to factors such as the number of etch-stop layers.

85. Moreover, Fang’s 20x thickness range is designed to accommodate a wide range of conditions and can accommodate differences in the layer structures and both orders of the alternative layers in the staircase. A POSITA would have known that Fang’s thickness range is suitable for Park.

3. Dependent claim 15

86. Dr. Campbell's argument against the obviousness of claim 15 based on Park in view of Fang simply repeats his prior arguments. He references his earlier sections or paragraphs throughout. *See, e.g.*, Ex. 2009 ¶ 87 (citing § VIII.C and ¶ 71), ¶ 88 (citing § IX.B), ¶ 89 ("As discussed previously...."). These arguments are incorrect for the same reasons I explain above. *See, e.g., supra* §§ VIII.C, IX.A.2.

X. DECLARATION

87. In signing this declaration, I realize that this declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the USPTO.

88. I am aware that willfully false statements and the like made by me in connection with this declaration are punishable by fine or imprisonment, or both (18 U.S.C. § 1001) and may jeopardize the validity of the Petition. All statements herein made by me of my own knowledge are true and all statements made on information and belief are believed to be true. I declare under penalty of perjury that the foregoing is true and correct.

Executed this 25 day of November 2025 at Austin, Texas.



Sanjay Banerjee, Ph.D