

Micron Technology, Inc.
Petitioner
v.
Yangtze Memory Technologies Company, Ltd.
Patent Owner

Case No. IPR2025-00117
U.S. Patent No. 10,672,711

Micron's Hearing Demonstratives

March 13, 2026

Claim 1

1. A semiconductor structure, comprising:

a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;

a barrier layer disposed over a portion of the gate stack of the each step;

an etch-stop layer disposed on the barrier layer;

an insulating layer disposed on the etch-stop layer; and

a plurality of conductive structures formed in the insulating layer, wherein each conductive structure is formed on the conductive layer of the each step.

Claims 7 and 10

7. The semiconductor structure of claim 1, wherein top surfaces of the plurality of conductive structures, the insulating layer, and a portion of the etch-stop layer are coplanar.

10. The semiconductor structure of claim 1, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.

Claim 13

13. A semiconductor structure, comprising
- a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;
 - an etch-stop layer disposed on a portion of the gate stack of the each step;
 - an insulating layer disposed on the etch-stop layer; and
 - a plurality of conductive structures formed in the insulating layer and extending through the etch-stop layer and the high-k dielectric layer, wherein each conductive structure directly contacts the corresponding conductive layer of each step.

Claims 14, 15, and 17

14. The semiconductor structure of claim 13, wherein the etch-stop layer is formed on a side surface and a top surface of each step.

15. The semiconductor structure of claim 14, wherein thicknesses of the etch-stop layer is the same on the side and top surfaces of each step.

17. The semiconductor structure of claim 13, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.

Road Map

- I. The IPR Grounds
- II. The '711 Patent
- III. Claim Construction
- IV. Ground 1: Kim in View of a POSITA's Knowledge
- V. Ground 2: Kim in View of Fang
- VI. Ground 3: Park in View of a POSITA's Knowledge
- VII. Ground 4: Park in View of Fang
- VIII. Dr. Campbell Is Not a POSITA

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Instituted Grounds

Ground	Prior Art	Claims
1	Kim	1-9, 11-16, and 18-19 obvious
2	Kim + Fang	10 and 17 obvious
3	Park	1-6, 8-9, 11-16, and 18-19 obvious
4	Park + Fang	7, 10, 15, and 17 obvious

Pet. (Paper 1), 11.

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The Technical Field: 3D Memory Staircase Structure

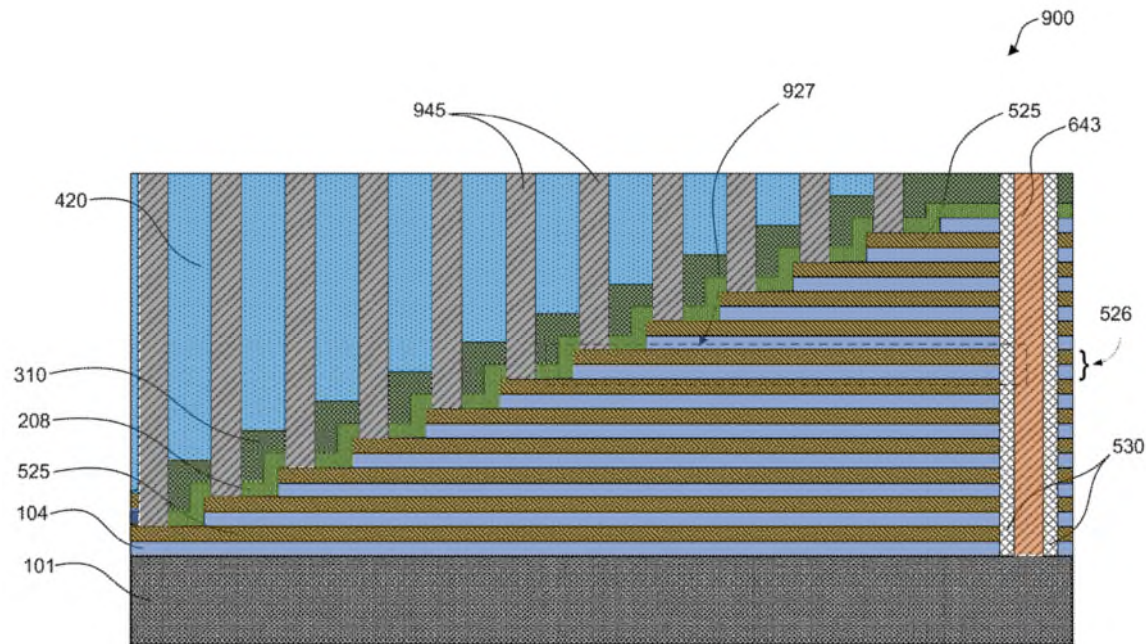


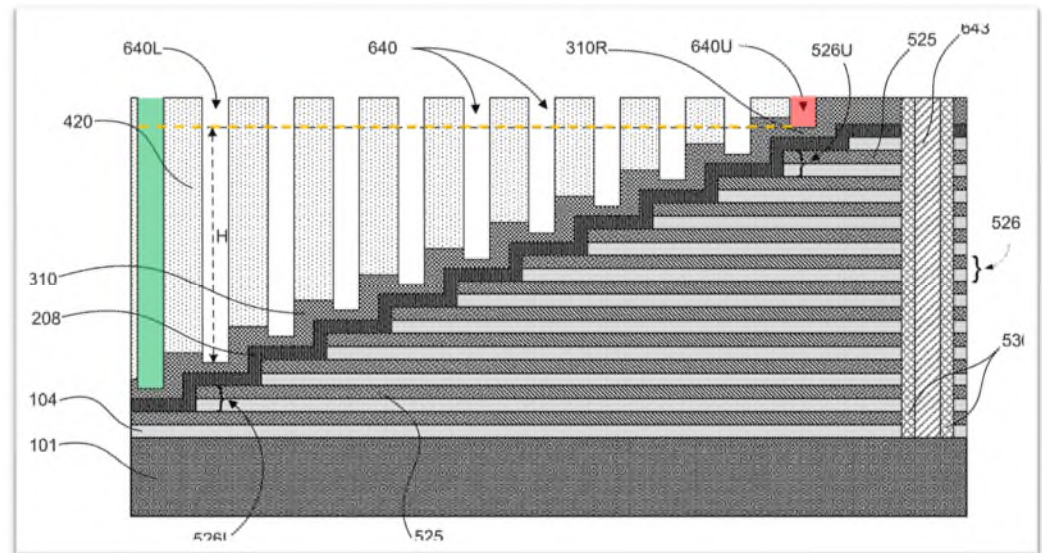
FIG. 9A

'711 Patent, Fig. 9A (Pet. (Paper 1), 23);
see also *id.*, 1:34-36 (POR (Paper 27), 2).

The Perceived Problem: Over-Etching Shallow Contact Holes While Etching Deeper Contact Holes

Lithography and etching processes can be used to open contact areas for forming electrical connection to the conductive layer on each level of the staircase structure. Due to topology of staircase structures, depth of the contact hole from the top surface to each level of the staircase depends on the location of each level. For example, contact holes for lower levels may be deeper than contact holes for upper levels. Typically, all of the contact holes are formed with a single lithography mask and etching process. Often, before contact holes to the bottom levels are entirely formed, the materials exposed in contact holes at the upper levels are over-etched and lost. To resolve this issue, two or more lithography masks are used to separate etching processes, which adds cost and complexity to the fabrication process.

'711 Patent, 5:40-53
(Pet. (Paper 1), 25; POR (Paper 27), 2-3).

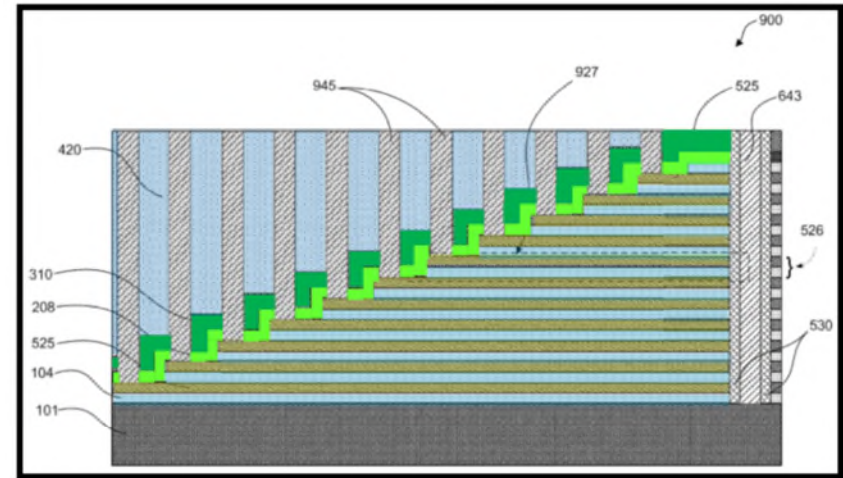


'711 Patent, Fig. 6
(Campbell POR Decl. ¶ 30; POR (Paper 27), 3).

The Alleged Invention: an Etch-Stop Layer to Protect Underlying Layers When Etching Contact Holes

Various embodiments in the present disclosure provide methods and structures for improving word line contacts for 3D memory devices. In the present disclosure, a single lithography mask can be used to form contact areas for word lines of 3D memory array. By adding an etch-stop film over the staircase structure, openings of the vertical interconnect access (VIA) contacts for each level of the staircase structure can be formed simultaneously. The etch-stop film protects underlying layers during etching processes that form contact VIAs. The etch-stop film is exposed on each level of the staircase structure by a selective etching process, and then removed by reverse selective etching. Accordingly, the disclosed methods and structures can improve fabrication yield and reduce cost. The methods and structures described

'711 Patent, 5:54-67
(Pet. (Paper 1), 26; POR (Paper 27), 3).



No.	Structure
525	Gate Stack
104	First Insulating Layer
208	Second Insulating Layer
310	Etch-Stop Layer
420	Third Insulating Layer
945	Vertical Interconnect Access Conductive Structures

'711 Patent, Fig. 9A; POR (Paper 27), 5.

The Gate-Stack-on-Top Configuration Is a Peripheral Limitation

- Dr. Campbell describes the alleged "solution" as the etch-stop film

26. The '711 patent solves the punch through problem without the drawbacks of separate etching steps for different hole depths. '711 patent 5:54-65. The solution includes an "etch-stop film" over the staircase structure, which protects underlying staircase structure layers during the etching process and permits the simultaneous etching of all word line holes. *Id.* This improves fabrication yield and reduces cost. *Id.* 5:65-67. A barrier layer can also be introduced over the staircase structure "for protecting the underlying structure during subsequent etching processes." *Id.* 7:35-39. The '711 patent specifies a

*Campbell POR Decl. ¶ 26
(POR (Paper 27),3).*

The '711 Patent Specifies a Two-Order-of-Magnitude Etch-Stop Thickness Range That Can Accommodate Material and Structural Differences

during subsequent etching processes.” *Id.* 7:35-39. The '711 patent specifies a range of thicknesses of etch-stop and barrier layers which can accommodate varying thicknesses based on materials used or structural differences, such as including or excluding the barrier layer. *See id.* 7:36-8:19, claims 10, 17.

Campbell POR Decl. ¶ 26 (citing '711 Patent, 7:36-8:19) (POR (Paper 27), 3).

'711 Patent, 7:56-8:14
(*Pet. (Paper 1)*, 62; *POR (Paper 27)*, 3).

Referring to FIG. 3, a staircase structure 300 is formed by disposing an etch-stop layer 310 on the staircase structure 200. A thickness of the etch-stop layer 310 can be in a range between 10 nm to 1000 nm (e.g., 10 nm, 20 nm, 30 nm, 40 nm, 50 nm, 60 nm, 70 nm, 80 nm, 90 nm, 100 nm, 200 nm, 300 nm, 400 nm, 500 nm, 600 nm, 700 nm, 800 nm, 900 nm, 1000 nm, any range bounded by the lower end by any of these values, or in any range defined by any two of these values). The etch-stop layer 310 can be made of any suitable insulating material that is different from the second insulating layer 208. In some embodiments, the etch-stop layer 310 can be disposed on the second insulating layer 208. In some embodiments, the second insulating layer 208 is optional and the etch-stop layer 310 can be directly disposed on the staircase structure 100. In some embodiments, the etch-stop layer 310 can cover the staircase structure 200, including the top surface 102T and the side surface 102S of each SC layer 102. In some embodiments, the thickness of the etch-stop layer 310 on a side surface 102S can be the same as that on a top surface 102T. In some embodiments, the thickness of the etch-stop layer 310 on the side surface 102S can be thicker or thinner than that on the top surface 102T. In some embodiments, etch-stop layer 310 can be made of silicon nitride, silicon oxynitride, spin-on-dielectric, and/or high-k dielectric films such as hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, or lanthanum oxide films.

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The '711 Patent Defines "On" as Broader than Requiring "Direct[] Contact[]"—The Definition Is Binding

It should be readily understood that the meaning of "on," "above," and "over" in the present disclosure should be interpreted in the broadest manner such that "on" not only means "directly on" something, but also includes the meaning of "on" something with an intermediate feature or a layer therebetween. Moreover, "above" or "over" not only means "above" or "over" something, but can also include the meaning it is "above" or "over" something with no intermediate feature or layer therebetween (i.e., directly on something).

'711 Patent, 4:1-6
(Pet. (Paper 1), 60, 89).

conductive structures 945 in the VIA openings 840. The VIA conductive structures 945 can be formed by disposing a third conductive material in the formed openings 840 and directly on the exposed portions of gate conductive layer 525M. In

ing layer 208. In some embodiments, the etch-stop layer 310 can be disposed on the second insulating layer 208. In some embodiments, the second insulating layer 208 is optional and the etch-stop layer 310 can be directly disposed on the staircase structure 100. In some embodiments, the etch-stop

711 Patent, 11:16-19, 7:66-8:3
(Banerjee Reply Decl. ¶ 16; Reply (Paper 36), 2).

1) The '711 patent defines "on" to include indirectly on: an element need not "directly contact" another to be "on" it, as PO proposes.

a. *Thorner v. Sony Comput. Ent. Am. LLC*, 669 F.3d 1362, 1366 (Fed. Cir. 2012) (holding that the word "means" indicates lexicography).

Reply (Paper 36), 2.

2) The definition is binding

a. "the patentee's lexicography **must** govern the claim construction analysis." *Braintree Labs., Inc. v. Novel Labs., Inc.*, 749 F.3d 1349, 1356 (Fed. Cir. 2014)

Reply (Paper 36), 3-4.

In the POR, PO Tries to Redefine "On a/the [Side or Top] Surface" as "Directly Contacting a/the [Side or Top] Surface"

14. The semiconductor structure of claim 13, wherein the etch-stop layer is formed on a side surface and a top surface of each step.

15. The semiconductor structure of claim 14, wherein thicknesses of the etch-stop layer is the same on the side and top surfaces of each step.

'711 Patent, cls. 14-15.

“On a side surface and a top surface of each step” should be construed as “directly contacting a side surface and a top surface of each step.” This construction

POR (Paper 27), 8.

PO's Proposed Construction Cannot Be Correct, Because the '711 Patent Uses "Directly Contacting" in Claims 13-15 to Indicate Electrical Contact

13. A semiconductor structure, comprising:
a staircase structure comprising a plurality of steps,
wherein each step comprises a gate stack disposed over
a dielectric layer, the gate stack comprising a high-k
dielectric layer and a conductive layer;
an etch-stop layer disposed on a portion of the gate stack
of the each step;
an insulating layer disposed on the etch-stop layer; and
a plurality of conductive structures formed in the insulat-
ing layer and extending through the etch-stop layer and
the high-k dielectric layer, wherein each conductive
structure directly contacts the corresponding conduc-
tive layer of each step.

*'711 Patent, cl. 13
(Reply (Paper 36), 2).*

18. Furthermore, claims 6 and 13 recite “directly contacts.” I understand that different patent terms are typically understood to have different meanings. Here, claims 14 and 15, by virtue of their dependency from claim 13, recite both “directly contacts” and “on.” Those recitations of different terms strongly suggest different meanings. As explained in the previous paragraph, a POSITA would understand that “each conductive structure *directly contacts* the corresponding conductive layer of each step” of claim 13 involves an electrical connection, and “the etch-stop layer is formed *on* a side surface and a top surface of each step” of claim 14 does not. Thus, a POSITA would understand these two different terms to mean different things.

*Banerjee Reply Decl. ¶ 18;
see also id. ¶ 17 (Reply (Paper 36), 2).*

SIPCO, LLC v. Emerson Elec. Co., 794 F. App'x 946, 949 (Fed. Cir. 2019)
(different terms are presumed to have different meanings)

Reply (Paper 36), 2.

The '711 Patent Specification Does Not Support Redefining "On a/the [Side or Top] Surface" as "Directly Contacting a/the [Side or Top] Surface"

PO alleges the '711 patent consistently uses "on a/the surface" to refer to "directly contacting a/the surface." *POR (Paper 27)*, 9. But:

- a. "It is not enough for a patentee to simply disclose a single embodiment or use a word in the same manner in all embodiments, the patentee must 'clearly express an intent' to redefine the term." *Thorner v. Sony Comput. Ent. Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012) (*Reply (Paper 36)*, 2-3).
- b. The embodiments are merely 'exemplary' and do not limit the claim scope. *Aventis Pharma S.A. v. Hospira, Inc.*, 675 F.3d 1324, 1331 (Fed. Cir. 2012) (*Reply (Paper 36)*, 3).

The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

'711 Patent, 14:64-67
(*Reply (Paper 36)*, 3).

Defining "On the Surface" to Permit an Intermediate Layer Does Not Render "Surface" Superfluous

- "Surface" requires the etch-stop layer to be completely external to the steps

*Banerjee Reply Decl. ¶ 22
(Reply (Paper 36), 3-4).*

Dr. Campbell. Regardless, I disagree with this argument. "Surface" can identify a plane or a two-dimensional set of points that is the reference for "on a side/top surface." For example, if claim 14 had recited "wherein the etch-stop layer is formed on a side [] and a top [] of each step" and omitted the word "surface," a POSITA would understand the claim to possibly permit the etch-stop layer to be part of the step, that is, part of the etch-stop layer may be in the interior of each step (yet still on, e.g., the "side" of the step). On the other hand, the actual claim 14, reciting "wherein the etch-stop layer is formed on a side surface and a top surface of each step," requires the etch-stop layer to be a structure that is on the exterior of the step.

- Undermining PO, Dr. Campbell himself considered "surface" to be superfluous

*Ex. 1027 (Campbell Dep.), 122:15-20
(Banerjee Reply Decl. ¶ 12; Reply (Paper 36), 2).*

Q Do you mean on the side surface or just simply on the side?

A Certainly on the side surface would be direct contact, and I think we would use on the side as well as direct contact.

Even If Defining "on a/the Surface" to Permit an Intermediate Layer Renders "Surface" Superfluous, the Express Definition Governs

"the patentee's lexicography must govern the claim construction analysis."

Braintree Labs., Inc. v. Novel Labs., Inc., 749 F.3d 1349, 1356 (Fed. Cir. 2014). (*Reply (Paper 36)*, 3-4).

"Here, as discussed above, the Board's construction is consistent with, and indeed tracks a verbatim definition set forth in, the [patent]."

Chevron U.S.A. Inc. v. Univ. of Wyoming Rsch. Corp., 978 F.3d 1361, 1367 (Fed. Cir. 2020).

The superfluous-language rule does not "supersede[] all other principles of claim construction."

SimpleAir, Inc. v. Sony Ericsson Mobile Commc'ns AB, 820 F.3d 419, 429 (Fed. Cir. 2016). (*Reply (Paper 36)*, 3).

• PO's case law fails

- In *Bicon Inc. v. Straumann Co.*, the construction that would render a claim term meaningless is contrary to the specification (as recognized in *Chevron U.S.A.*)

(*Sur-Reply (Paper 44)*, 2).

- The PO in *Ralph Lauren Corp. v. Lexos Media IP, LLC* did not construe any term in the POR. The petitioner's new construction in Reply was not in response to the POR. Here, Petitioner's construction is in the Petition and is thus timely

(*Sur-Reply (Paper 44)*, 3-4).

Road Map

- I. The IPR Grounds
- II. The '711 Patent
- III. Claim Construction
- IV. Ground 1: Kim in View of a POSITA's Knowledge
 - A. Claim 1: "each step comprises a gate stack disposed over a dielectric layer"
 - B. Claims 14-15: "on a/the ... surface"
- V. Ground 2: Kim in View of Fang
- VI. Ground 3: Park in View of a POSITA's Knowledge
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(A) Petition's Showing—Kim Discloses "Each Step Comprises a Gate Stack Disposed over a Dielectric Layer"

- Kim discloses (1) embodiments with a gate-stack-on-top ordering even though the figures show the opposite and (2) that it will not repeat overlapping descriptions for the same reference numerals.
- Thus, Kim discloses reversing the gate stack ordering shown in Figures 17-22.

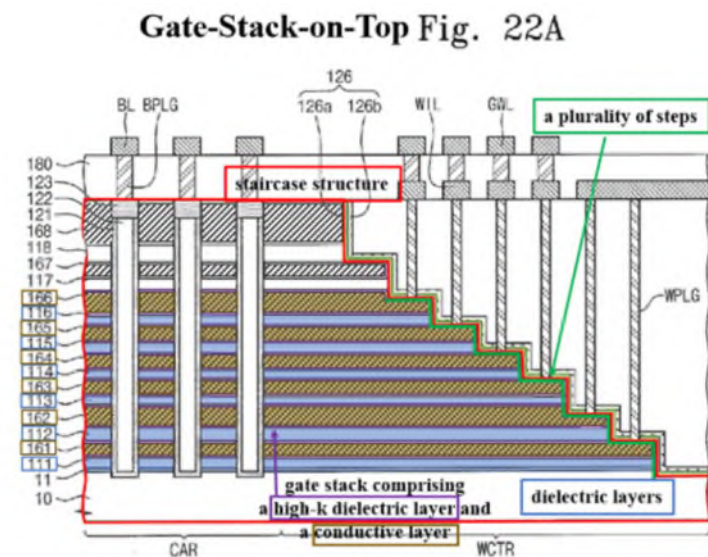
Pet. (Paper 1), 28-29, 32-34.

WCTR. In other embodiments, each of top surfaces of the sacrificial layers SC1 to SC8, not the top surfaces of the insulating layers 111 to 118, may be partially exposed in the word line contact region WCTR.

Kim ¶ [0090] (Pet. (Paper 1), 28).

[0184] In these embodiments, the same elements as in the embodiments previously described with reference to FIGS. 5A through 14A and FIGS. 5B through 14B will be denoted by the same reference numbers therein, and for concise description, overlapping description of elements previously described with reference to FIGS. 5A through 14A and FIGS. 5B through 14B may be omitted.

Kim ¶ [0184] (Pet. (Paper 1), 29).

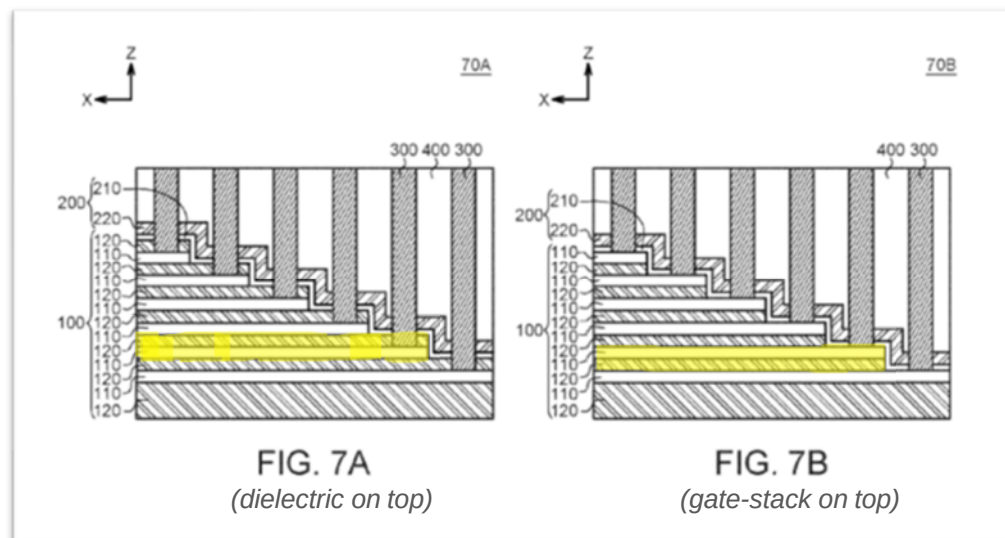


Kim, Fig. 22A (Pet. (Paper 1), 40).

(A) Petition's Showing—Kim Renders Obvious "Each Step Comprises a Gate Stack Disposed over a Dielectric Layer"

- Other prior art **additionally** demonstrates that each layer ordering was a well-known, routine, and suitable option.

Pet. (Paper 1), 33-34.



*Chen Figs. 7A-7B
(Pet. (Paper 1), 33).*

respect to another insulating layers (170) and sacrificial layers (140). In addition, a portion of the top surface of each insulating layer (170) may be exposed by the plurality of pad regions (P1-P6), and, unlike what is shown in FIG. 9a, a portion of the top surface of each sacrificial layer (140) may be exposed in a plurality of pad regions (P1-P6).

Park, [0102] (Pet. (Paper 1), 30-31).

(A) PO's Arguments Fail—Claim 1 Summary

- 1) PO's argument that there must be a "benefit" to reversing the gate ordering fails, because the gate-stack-on-top ordering is a "suitable option" that addresses the same problem (put another way, a predictable variation).
- 2) PO's "missing limitation" argument fails, because Kim itself discloses layer reversal: there is no "missing limitation."
- 3) Even if there were a missing limitation, reversing Kim's gate ordering was obvious, because the prior art demonstrates that layer reversal was "unusually simple" to a POSITA.

Reply (Paper 36), 4-11.

(1) The Gate-Stack-on-Top Configuration Is a Suitable Option for the Problem of Constructing a Staircase

- A gate-stack-on-top was a suitable option and predictable variation for addressing the problem of constructing a staircase structure.

Reply (Paper 36), 1, 5.

Id., 296 (Fig. 7.6). The staircase structure provides landing areas on the control gates for contacts with vertical conductive structures to couple the control gates to control voltages. *Id.*, 298; Banerjee ¶ 50.

Pet. (Paper 1), 19.

24. The gate-layer-on-top and the dielectric-layer-on-top configuration were common, well understood, and predictable variations of a staircase structure. In both, the alternating layers perform their typical functions: the gate layers serve as word lines connecting the vertical conductive structures to the gate terminals of memory cells, and the dielectric layers provide insulation and structural support between the gate layers. The order of the alternating layers in each step of the staircase does not change or impact their function in a meaningful way. Selecting one of the two orders was a simple design choice, as I testified in my deposition.

Banerjee Reply Decl. ¶ 24 (Reply (Paper 36), 5-6).

- **Kim, Chen, and Park** all demonstrate that each gate ordering was a suitable and predictable option.

Reply (Paper 36), 5.

(1) This "Suitable Option" for the Staircase Provides the Motivation

Reversing the Board in finding no motivation due to the substitution resulting in no "obvious improvement," the Federal Circuit held that a "known way to address [the same] problem is precisely the reason that there's a motivation to combine under KSR." Put another way, it was only necessary to show "suitable option."

Intel Corp. v. PACT XPP Schweiz AG, 61 F.4th 1373, 1380 (Fed. Cir. 2023) (citation modified). (*Reply (Paper 36)*, 5, 9).

A combination that simply arranges old elements to perform the conventional function and yields expected results is obvious.

KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 417 (2007). (*Reply (Paper 36)*, 5, 7).

"Combining two embodiments disclosed adjacent to each other ... does not require a leap of inventiveness."

Boston Sci. Scimed, Inc. v. Cordis Corp., 554 F.3d 982, 990–92 (Fed. Cir. 2009). (*Reply (Paper 36)*, 6).

(1) PO's Case Law Fails

- PO's case law fails

- The *CommScope* petition asserted “‘improvement’ and ‘predictable, beneficial results’ without further explanation,” and did not demonstrate how the alleged option addresses the alleged problem.

Sur-Reply (Paper 44), 5.

- *In re Stepan* does not involve two well-known, predictable variations set forth in the primary reference itself and in other references

Reply (Paper 36), 6.

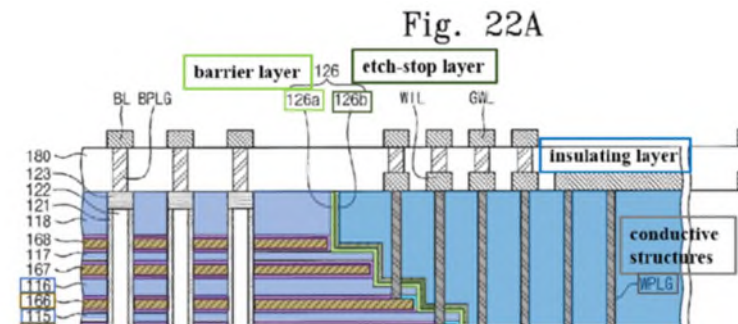
- *Intel Corp. v. Tela Innovations, Inc.* does not overcome *Boston Scientific* because there, as PO acknowledged (*Sur-Reply*, 6), the adjacent placement was the *only* rationale for combining the two embodiments

Sur-Reply (Paper 44), 6.

(2) Kim Has No Missing Limitation—It Discloses Layer-Order Reversal

- Kim expressly discloses reversing the ordering:

horizontal area of the mask pattern MP. As the stacked layer structure ST is repeatedly etched, the insulating layers 111 to 118 may have edge portions having exposed top surfaces. In other words, each of top surfaces of the insulating layers 111 to 118 constituting the stepwise stacked layer structure ST may be partially exposed in the word line contact region WCTR. In other embodiments, each of top surfaces of the sacrificial layers SC1 to SC8, not the top surfaces of the insulating layers 111 to 118, may be partially exposed in the word line contact region WCTR.



Kim ¶ [0090], Fig. 22A (partial) (Pet. (Paper 1), 28).

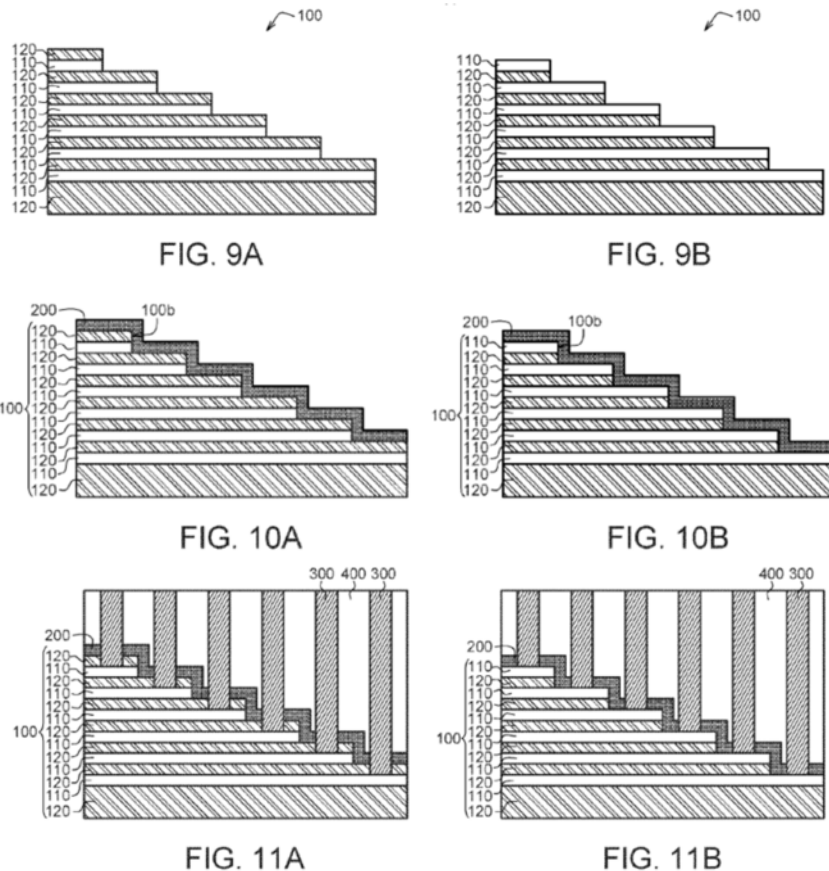
- Dr. Campbell admits that Kim discloses gate-stack on top (i.e., layer-order reversal)

specific passage of Kim for support. I note that in a previous section, Dr. Banerjee cites to paragraphs 90-91 of Kim, asserting that they describe “embodiments in which a gate stack is disposed over a dielectric layer at each step.” Ex. 1003 ¶69 (citing Kim (Ex. 1005) [0090]-[0091]). However, those passages of Kim specifically relate to Figures 4, 8A, and 8B and not the Figure 17A-22B embodiment the Petition and Dr. Banerjee relies on. See Kim [0086]. Dr. Banerjee

Campbell POR Decl. ¶ 36 (Banerjee Reply Decl. ¶ 31; Reply (Paper 36), 9).

(3) Prior Art Shows That Implementing Either Layer Ordering Was Unusually Simple to a POSITA

- Chen describes the process step-by-step without distinguishing details based on the layer ordering



[0054] FIGS. 9A-11B illustrate a process for manufacturing a semiconductor structure according to an embodiment of the present disclosure. FIGS. 9A, 10A, and 11A and FIGS. 9B, 10B, and 11B respectively illustrate the processes for manufacturing the semiconductor structures as shown in FIG. 4A and FIG. 4B. The elements in the present embodiment sharing similar or the same labels with those in the previous embodiment are similar or the same elements, and the description of which is omitted.

[0055] As shown in FIGS. 9A and 9B, the stack structure 100 is formed. The present step includes forming a plurality of conductive layers 110 and forming a plurality of insulating layers 120, and the conductive layers 110 and the insulating layers 120 are stacked interlacedly. As shown in FIGS. 9A and 9B, the stack structure 100 has a staircase structure with the insulating layers 120 and the conductive layers 110 as the surfaces of the staircase.

[0056] As shown in FIGS. 10A and 10B, the etching stop layer 200 is formed on the stack structure 100. For example, as shown in FIGS. 1A-1B, the etching stop layer 200 is formed on a sidewall 100a of the stack structure 100, and the etching stop layer 200 is made of a material having an energy gap of larger than 6 eV. As shown in FIGS. 10A and 10B, the etching stop layer 200 is formed on the surfaces of the insulating layers 120 and the surfaces of the conductive layers 110, and the etching stop layer 200 is formed on a side surface 100b of the staircase of the stack structure 100.

[0057] Next, as shown in FIGS. 11A and 11B, the conductive structure 300 is formed, and the dielectric layer 400 is formed on the etching stop layer 200. One conductive structure 300 is electrically connected to at least one of the conductive layers 110. As shown in FIGS. 11A and 11B, each of the conductive structures 300 is respectively electrically connected to each of the corresponding conductive layers 110. As such, the semiconductor structures 40A and 40B as shown in FIGS. 4A and 4B are formed.

Chen, Figs. 9A-11B, [0054]-[0057] (Banerjee Reply Decl. ¶ 25; Reply (Paper 36), 7, 10).

(3) Prior Art Shows That Implementing Either Layer Ordering Was Unusually Simple to a POSITA

- Kim and Park disclose inverting the ordering without needing to provide any details

horizontal area of the mask pattern MP. As the stacked layer structure ST is repeatedly etched, the insulating layers 111 to 118 may have edge portions having exposed top surfaces. In other words, each of top surfaces of the insulating layers 111 to 118 constituting the stepwise stacked layer structure ST may be partially exposed in the word line contact region WCTR. In other embodiments, each of top surfaces of the sacrificial layers SC1 to SC8, not the top surfaces of the insulating layers 111 to 118, may be partially exposed in the word line contact region WCTR.

Kim ¶ [0090] (Reply (Paper 36), 7).

Referring to FIG. 9a, a plurality of insulating layers (170) and sacrificial layers (140) alternately stacked on the top surface of the substrate (105) are etched to provide a plurality of pad regions (P1-P6). Each of the plurality of insulating layers (170) and sacrificial layers (140), by a plurality of pad regions (P1-P6), forms a step with respect to another insulating layers (170) and sacrificial layers (140). In addition, a portion of the top surface of each insulating layer (170) may be exposed by the plurality of pad regions (P1-P6), and, unlike what is shown in FIG. 9a, a portion of the top surface of each sacrificial layer (140) may be exposed in a plurality of pad regions (P1-P6).

Park, [0102] (Reply (Paper 36), 7).

(B) Petition's Showing—Kim Renders Obvious Claims 14-15 Under the Correct Claim Construction of "on a/the [Side or Top] Surface"

- PO's argument relies on its construction of "on a side/top surface" that erroneously requires "direct contact" and thus ignores the '711 express definition.

Reply (Paper 36), 2, 12.

It should be readily understood that the meaning of “on,” “above,” and “over” in the present disclosure should be interpreted in the broadest manner such that “on” not only means “directly on” something, but also includes the meaning of “on” something with an intermediate feature or a layer therebetween. Moreover, “above” or “over” not only means “above” or “over” something, but can also include the meaning it is “above” or “over” something with no intermediate feature or layer therebetween (i.e., directly on something).

'711 Patent, 4:1-6 (Pet. (Paper 1), 60).

(B) Kim Renders Obvious Claims 14-15 Under PO's Incorrect Claim Construction of "on a Surface"

- Should the Board adopt PO's construction, Kim's single-etch-stop variant renders the claims obvious.

125a. In some embodiments, the first stop layer 125a may be formed of silicon oxide and the second stop layer 125b may be formed of silicon nitride. In other embodiments, the etch stop layer 125 may be a single layer, which is formed of a material having an etch selectivity with respect to the sacrificial layers SC1 to SC8 and the insulating layers 111 to 118.

Kim [0187] (Banerjee Reply Decl. ¶¶39–40; Reply (Paper 36), 12).

- Petitioner is permitted to respond to PO's construction:

"[P]etitioner must be afforded a reasonable opportunity in reply to present argument and evidence under [PO's] new construction."

Axonics, Inc. v. Medtronic, Inc., 75 F.4th 1374, 1383 (Fed. Cir. 2023), dismissed, 2025 WL 471226 (Fed. Cir. Feb. 12, 2025). (*Reply (Paper 36), 12*).

Road Map

- I. The IPR Grounds
- II. The '711 Patent
- III. Ground 1: Kim in View of a POSITA's Knowledge
- IV. Ground 2: Kim in View of Fang
 - A. Claims 10 and 17: "a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm"
- V. Ground 3: Park in View of a POSITA's Knowledge
- VI. Ground 4: Park in View of Fang
- VII. Dr. Campbell Is Not a POSITA

(A) Petition's Showing—the Claimed Etch Stop Thickness Range Was Notoriously Well Known and Lacks Criticality

- Examiner's "office notice":

However, the examiner takes official notice that a silicon nitride etch-stop layer having a thickness in the range of 10-1000 nm is notoriously well known in the art of semiconductor technology. Furthermore, the range recited in claims 10 and 15 lacks criticality, as evidenced by the range being two orders of magnitude, and as also supported by applicant's own lengthy disclosure within paragraph (0056).

*'711 Patent FH, 156
(Pet. (Paper 1), 62).*

Referring to FIG. 3, a staircase structure 300 is formed by disposing an etch-stop layer 310 on the staircase structure 200. A thickness of the etch-stop layer 310 can be in a range between 10 nm to 1000 nm (e.g., 10 nm, 20 nm, 30 nm, 40 nm, 50 nm, 60 nm, 70 nm, 80 nm, 90 nm, 100 nm, 200 nm, 300 nm, 400 nm, 500 nm, 600 nm, 700 nm, 800 nm, 900 nm, 1000 nm, any range bounded by the lower end by any of these values, or in any range defined by any two of these values). The etch-stop layer 310 can be made of any suitable insulating material that is different from the second insulating layer 208. In some embodiments, the etch-stop layer 310 can be disposed on the second insulating layer 208. In some embodiments, the second insulating layer 208 is optional and the etch-stop layer 310 can be directly disposed on the staircase structure 100. In some embodiments, the etch-stop

'711 Patent, 7:56-8:3 (Pet. (Paper 1), 62).

- The upper end of the range is about **as thick as the staircase itself**.

Reply (Paper 36), 13 (citing Ex. 1027 (Campbell Dep.), 31:19–25).

- Where, as here, the “[d]ifferences between the prior art and the claimed invention[, if any, is merely] dimensional,” not resulting in “differences in performance,” the claim is not valid.

Gardner v. TEC Sys., Inc., 725 F.2d 1338, 1345-46 (Fed. Cir. 1984) (Reply (Paper 36), 62).

(A) Petition's Showing—Kim and Fang Render Obvious the Claimed "Range Between 10 nm and 1000 nm"

- If more is required (it is not), Fang discloses a range that overlaps with claimed range:

[0021] The etch stop material 130 may be formed over the stairs 125 at a thickness ranging from about 50 Å to about 1000 Å, such as from about 50 Å to about 600 Å, or from about 100 Å to about 500 Å. The thickness of the etch stop

Fang, [0021] (Pet. (Paper 1), 63).

- Fang discloses an analogous structure with an etch-stop: (1) both etch stops may comprise silicon nitride, (2) both etch stops may be formed of conventional techniques, and (3) Fang's range may be adjusted to Kim's staircase.

Pet. (Paper 1), 63.

- A POSITA would have been motivated to consider Fang's punch-through teachings because they dovetail with Kim's focus on reducing damage and Kim does not detail contact region concerns.

Pet. (Paper 1), 65.

(A) PO's Arguments Fail—Claims 10 and 17 Summary

- 1) PO is incorrect; criticality is relevant to obviousness.
- 2) PO is incorrect that Fang's etch-stop material is limited to carbon-doped silicon nitride ("CDSN") and thus irrelevant to Kim. Even if it were, CDSN's dry etch rate is the same as silicon nitride (Kim's etch stop), and thus the alleged difference is irrelevant.
- 3) PO "different focus" argument does not defeat motivation, because Fang and Kim both disclose etch stops on steps.
- 4) PO is incorrect that structural differences below Kim's etch stop layer impact Fang's range applicability.
- 5) PO's recycled arguments against a reasonable expectation of success fail.

Pet. (Paper 1), 62; Reply (Paper 36), 13-19.

(1) PO Is Incorrect on the Law

- "A presumption of obviousness applies '[w]here a claimed range overlaps with a range disclosed in the prior art.'"

UCB, Inc. v. Actavis Lab'ys UT, Inc., 65 F.4th 679, 687, 689-90 (Fed. Cir. 2023)
(*Sur-Reply (Paper 44)*, 12-13).

- Criticality is relevant to whether PO meets its burden of production to overcome this presumption.

Pet. (Paper 1), 62.

(1) The Lack of Criticality Demonstrates that the Limitation Is a Non-Inventive, Workable Range

- Dr. Campbell testified that the ***upper bound of the range is as tall as the staircase itself.***

Ex. 1027 (Campbell Dep.), 31:19-25 (Reply (Paper 36), 13).

- Dr. Campbell testified the range is a place to start doing experiments.

Q And a POSITA reading the '711 Patent, supposed the POSITA picks out a particular combination of materials for the sacrificial layer and the etch-stop layer, the POSITA would know what's the appropriate thickness or thickness range for that particular combination of materials, is that correct?

A No, not completely, no.
The range that's given there is a place to start doing experiments to determine the actual thickness that you would need.

Ex. 1027 (Campbell Dep.), 105:23-106:10 (Reply (Paper 36), 13).

"[I]t is not inventive to discover the optimum or workable ranges by routine experimentation," much less a broad range within which a workable range is to be found.

In re Aller, 220 F.2d 454, 456 (C.C.P.A. 1955) (Reply (Paper 36), 13-14).

(1) Like the '711 Patent's Range, Fang's Range Lacks Criticality

- Fang specifies a wide thickness range, 5-100 nm, which is a factor of 20.

Reply (Paper 36), 14 (citing Pet. (Paper 1), 63).

- Fang's range is suitable “for any material” “not substantially removed (e.g., etched)” with “the nitride materials of the staircase structure.”

Reply (Paper 36), 14 (citing Fang, [0020]) (numerals omitted).

- Fang's range applies regardless of the carbon-doping composition.

Reply (Paper 36), 14 (citing Ex. 2008, 53:8-54:2).

- Because Fang's “range” limitation also lacks criticality, any minor differences between Kim and Fang are irrelevant to a POSITA's motivation and expectation of success in applying Fang's range to Kim.

Reply (Paper 36), 14 (citing Banerjee Reply Decl. ¶¶48-49).

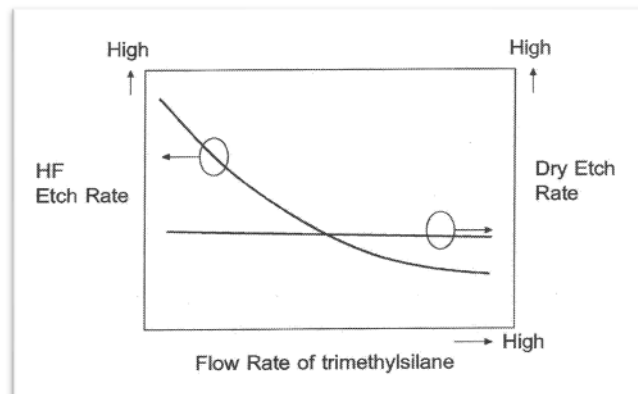
(2) Fang's CDSN Etch Stop Layer Is Exemplary and, Even If It Were Not, the Alleged Difference Is Irrelevant

- Fang's range is not specific to CDSN:

or a diffusion process. The etch stop material 130 may be any material that is not substantially removed (e.g., etched) during removal and replacement of the nitride materials 120 of the staircase structure 105. By way of example only, the etch stop material 130 may be formed from the carbon-doped silicon nitride, which is not substantially removed during removal of the nitride materials 120 of the staircase structure 105. The etch stop material 130 may exhibit a

Fang [0020] (Banerjee Reply Decl. ¶ 51; Reply (Paper 36), 15).

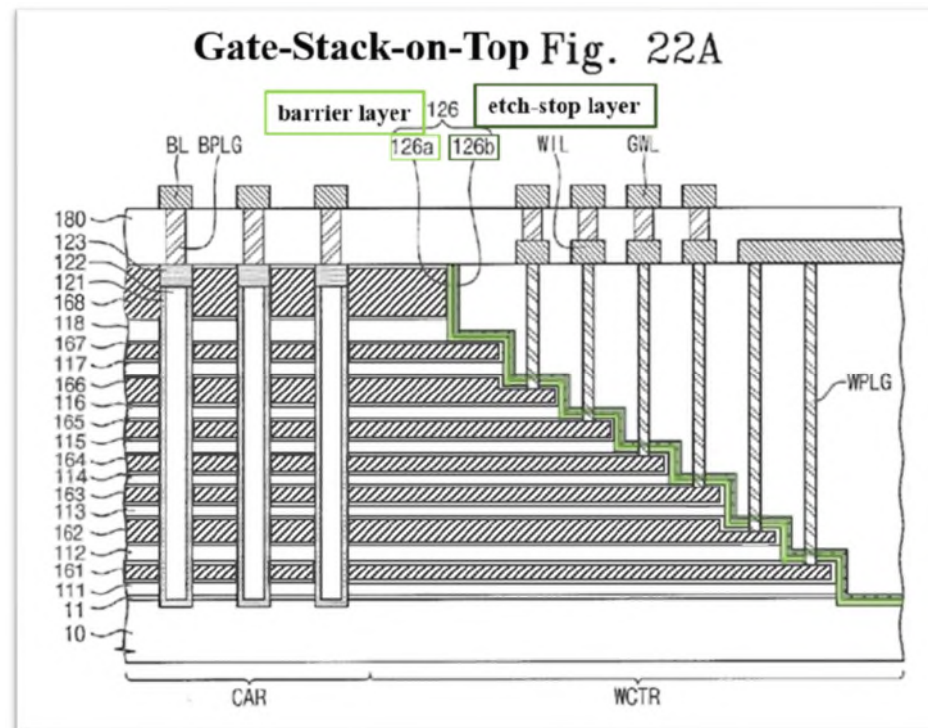
- Even if it were specific to CDSN, that is irrelevant, because the dry etch rate of CDSN and Kim's SN is the same:



Ex. 1029, Fig. 19 (Reply (Paper 36), 16; Banerjee Reply Decl. ¶ 53).

(3) PO's "Different Focus" Argument Ignores the Record: Kim Plainly Has an Etch Stop Covering Its Steps

- PO's characterization of Kim's etch-stop layer 125 as only protecting the contact pads is incorrect.



Kim, Fig. 22A
(Pet. (Paper 1), 43; Reply (Paper 36), 16).

(4) Underlying Structural Differences Below an Etch-Stop Layer Do Not Affect the Etch Stop's Thickness: an Etch Stop Protects the Underlying Films

- An etch stop **protects** its **underlying layers**:
- Likewise, an underlying barrier layer **protects** its **underlying layers**:
- Likewise, an underlying high-K layer **protects** its **underlying layers**:

can be formed simultaneously. The etch-stop film protects underlying layers during etching processes that form contact VIAs. The etch-stop film is exposed on each level of the

'711 Patent (Ex. 1001), 5:61-63 (Pet. (Paper 1), 24-25).

be an optional barrier layer. For example, the second insulating layer 208 can be used as a barrier layer for protecting the underlying structure during subsequent etching processes. In some embodiments, thicknesses of the second

'711 Patent (Ex. 1001), 7:36-39 (Pet. (Paper 1), 24-25).

Q Is it fair to say that the etch-stop layer provides its protective function relative to the etching of the layer that's immediately above it?

A Yes.

Ex. 1027 (Campbell Dep.), 23:4-8
(Reply (Paper 36), 18).

(4) Underlying Structural Differences Below an Etch-Stop Layer Do Not Affect the Etch Stop's Thickness: Chen Rejects PO's Position

- Chen contradicts PO's arguments: it discloses the same "etch stop" thickness for both gate orderings, which have different underlying structures.

Reply (Paper 36), 18.

[0048] FIG. 8A shows a curve of applied voltages vs. the thickness of a single-layer silicon nitride etching stop layer 200, wherein the silicon nitride layer has a tunneling length L1, and FIG. 8B shows a curve of applied voltages vs. the thickness of a single-layer aluminum oxide etching stop layer 200, wherein the aluminum oxide layer has a tunneling length L2. It is apparent that the tunneling length L2 is larger than the tunneling length L1.

Chen, [0048] (Reply (Paper 36), 18).

(4) Underlying Structural Differences Below an Etch-Stop Layer Do Not Affect the Etch Stop's Thickness: the Overlying Layer Effects Thickness

- The etch stop's thickness is based on the layers above it:

that “different etch process” is irrelevant to the etch-stop thickness. Again, the etch-stop layer functions as an etch stop during the etching of the insulating layer above it. Ex. 1027, 23:4-8. The thickness of the etch-stop layer is based on the etching of that insulating layer above, to slow down etching when the layer above has been completely etched and the etchant reaches the etch-stop layer. It needs to be thick enough to protect its underlying layer. But the barrier layer (or Kim’s first stop layer 126a) functions as an etch stop when the *etch-stop layer* is *intentionally* etched. *Id.*, 44:19-23 (“Q. And would you agree that the barrier layer also has an etch-stop property with respect to the etch-stop layer? A. Yes, that’s exactly what it does.”);

Banerjee Reply Decl. ¶ 61 (Reply (Paper 36), 18).

(4) Underlying Structural Differences Below an Etch-Stop Layer Do Not Affect the Etch Stop's Thickness: PO's Concession that the Range Applies to Structural Differences

- PO admits that a “range of thickness” (like the '711 patent's range) applies to a device regardless of whether the device includes an extra lower etch-stop layer.

for devices with or without the barrier layer. Pet. 66. But Petitioner ignores that the '711 patent specifies a *range* of thickness in its etch-stop layer, and this range can accommodate varying thicknesses based on materials used or structural differences, such as including or excluding the barrier layer.

POR (Paper 27), 40 (Reply (Paper 36), 17).

(5) PO's Recycled Arguments Against a Reasonable Expectation of Success Fail

- PO's arguments against a reasonable expectation of success are the same as those against motivation to combine and fail for the same reasons: the impact of alleged material and structural differences, even if taken as true, are immaterial to ranges that lack criticality.

POR (Paper 27), 41-42; Reply (Paper 36), 18–19.

Road Map

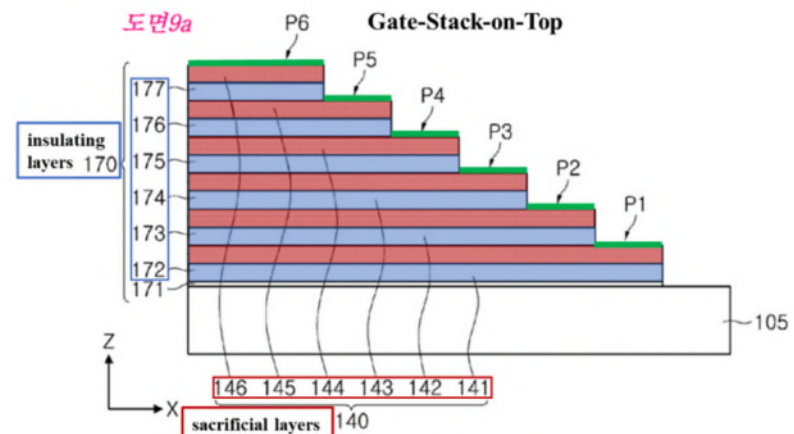
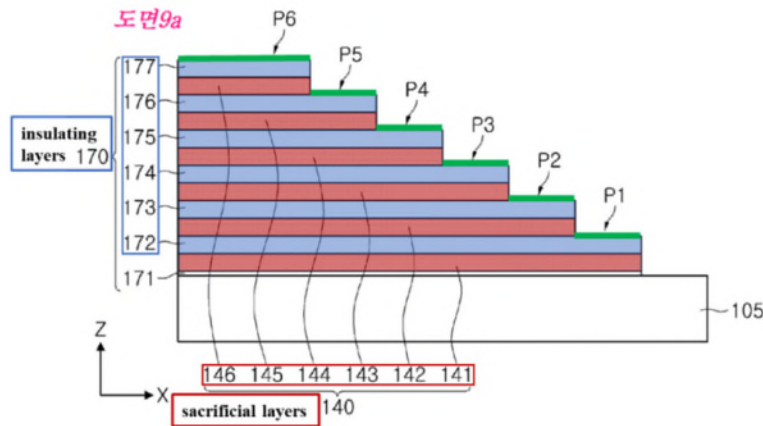
- I. The IPR Grounds
- II. The '711 Patent
- III. Claim Construction
- IV. Ground 1: Kim in View of a POSITA's Knowledge
- V. Ground 2: Kim in View of Fang
- VI. Ground 3: Park in View of a POSITA's Knowledge
 - A. Claim 1: "each step comprises a gate stack disposed over a dielectric layer"
 - B. Claims 14-15: "on a/the ... surface" "of each step"
 - C. Claim 15: " thicknesses ... is the same on the side and top surfaces"
- VII. Ground 4: Park in View of Fang
- VIII. Dr. Campbell Is Not a POSITA

(A) Petition's Showing—Park Discloses and at Least Renders Obvious the "Each Step Comprises a Gate Stack Disposed over a Dielectric Layer"

- Park discloses both gate layer orderings for Figure 9:

respect to another insulating layers (170) and sacrificial layers (140). In addition, a portion of the top surface of each insulating layer (170) may be exposed by the plurality of pad regions (P1-P6), and, unlike what is shown in FIG. 9a, a portion of the top surface of each sacrificial layer (140) may be exposed in a plurality of pad regions (P1-P6).

Park, [0102] (Pet. (Paper 1), 30-31).



Park, Fig. 9a (Reply (Paper 36), 20).

(A) PO's Arguments Fail—Claim 1 Summary

- 1) PO is incorrect: Park plainly discloses layer-order reversal in Figure 9.
- 2) PO's missing-limitation argument fails for the same reason as with Kim (*supra*).

Reply (Paper 36), 19-22.

(1) Park Discloses Layer-Order Reversal for the Figure 9 Embodiment

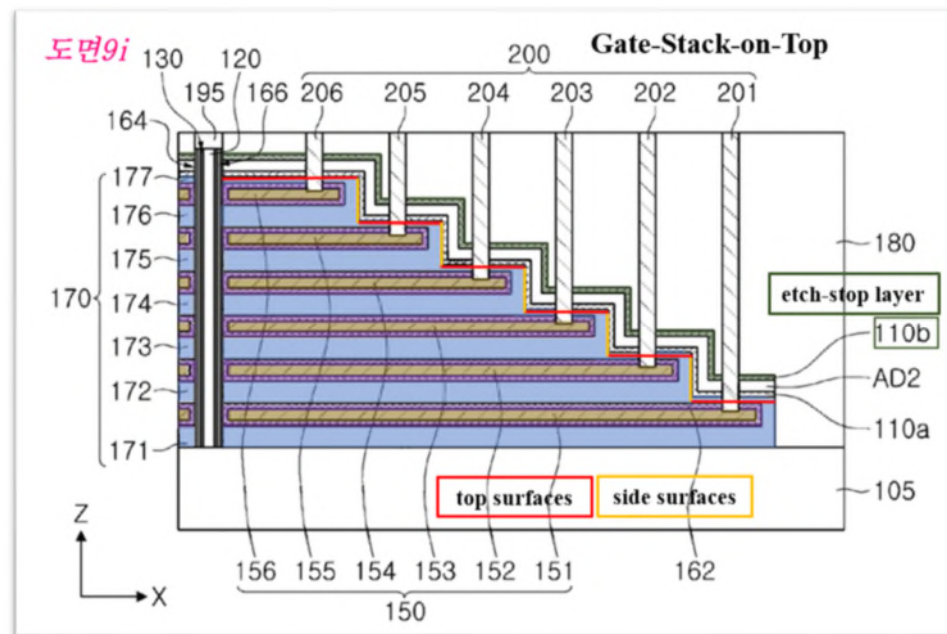
- Park discloses layer-order reversal for its Figure 9:

Referring to FIG. 9a, a plurality of insulating layers (170) and sacrificial layers (140) alternately stacked on the top surface of the substrate (105) are etched to provide a plurality of pad regions (P1-P6). Each of the plurality of insulating layers (170) and sacrificial layers (140), by a plurality of pad regions (P1-P6), forms a step with respect to another insulating layers (170) and sacrificial layers (140). In addition, a portion of the top surface of each insulating layer (170) may be exposed by the plurality of pad regions (P1-P6), and, unlike what is shown in FIG. 9a, a portion of the top surface of each sacrificial layer (140) may be exposed in a plurality of pad regions (P1-P6).

Park, [0102]; Reply (Paper 36), 19.

(B) Petition's Showing—Park Renders Obvious "the Etch-Stop Layer Is Formed on a Side Surface and a Top Surface of Each Step"

- Park includes an etch-stop layer "on" the top and sides of steps, as shown below:



*Park, Fig. 9i
(Pet. (Paper 1), 89).*

(B) PO's Arguments Fail—Claims 14 & 15 Summary

- 1) The correct construction of "on a surface" includes "on" an intervening layer above the surface.
- 2) Under PO's incorrect construction, Park discloses a single-etch-stop embodiment, rendering claims 14 and 15 obvious.
- 3) PO is incorrect to argue that the etch-stop layer must cover all steps of the staircase. The correct construction of "comprising," "a plurality of steps," and "each step" does not require "all" steps of the entire staircase.

Reply (Paper 36), 22-23.

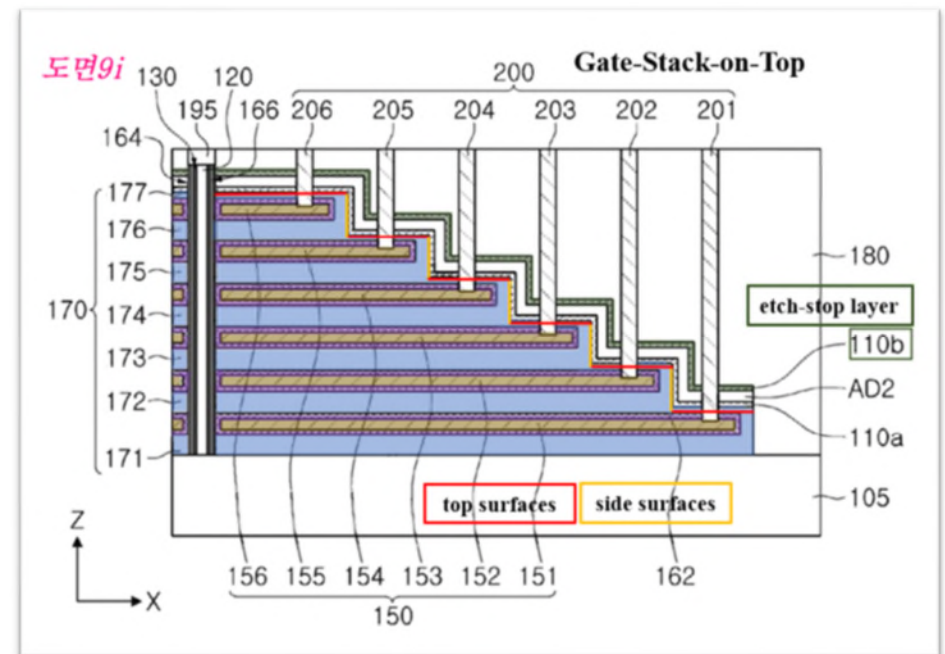
(1) Park Renders Obvious Claims 14-15 Under the Correct Claim Construction of "on a Surface"

- PO's construction that excludes an intervening layer is legally erroneous.

Reply (Paper 36), 23.

It should be readily understood that the meaning of “on,” “above,” and “over” in the present disclosure should be interpreted in the broadest manner such that “on” not only means “directly on” something, but also includes the meaning of “on” something with an intermediate feature or a layer therebetween. Moreover, “above” or “over” not only means “above” or “over” something, but can also include the meaning it is “above” or “over” something with no intermediate feature or layer therebetween (i.e., directly on something).

'711 Patent, 4:1-6 (Pet. (Paper 1), 89).



Park, Fig. 9i
(Pet. (Paper 1), 89).

(2) Park Renders Obvious Claims 14-15 Under PO's Incorrect Claim Construction of "on a Surface"

- Park discloses a single-etch-stop embodiment without a barrier layer, such that the etch-stop directly contacts the top and side surface of each step

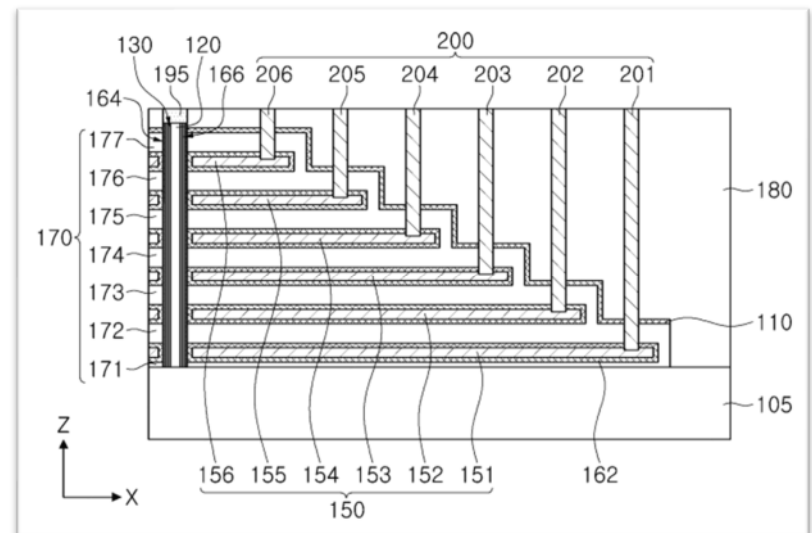
"[P]etitioner must be afforded a reasonable opportunity in reply to present argument and evidence under [PO's] new construction."

Axonics, Inc. v. Medtronic, Inc., 75 F.4th 1374, 1383 (Fed. Cir. 2023), dismissed, 2025 WL 471226 (Fed. Cir. Feb. 12, 2025)

Reply (Paper 36), 12, n. 6.

- The AD layer in Figure 9 is optional.

Pet. (Paper 1), 72.



Park, Fig. 8m, [0049] (Reply (Paper 36), 23; Pet. (Paper 1), 102).

(3) Park Renders Obvious Claims 14-15 Under the Correct Claim Construction of "Each" and "Comprising"

- "Each step" does not require "all" steps of the staircase.

13. A semiconductor structure, comprising:
a staircase structure comprising a plurality of steps,
wherein each step comprises a gate stack disposed over
a dielectric layer, the gate stack comprising a high-k
dielectric layer and a conductive layer;
an etch-stop layer disposed on a portion of the gate stack
of the each step;
an insulating layer disposed on the etch-stop layer; and
a plurality of conductive structures formed in the insulating
layer and extending through the etch-stop layer and
the high-k dielectric layer, wherein each conductive
structure directly contacts the corresponding conductive
layer of each step.

14. The semiconductor structure of claim 13, wherein the
etch-stop layer is formed on a side surface and a top surface
of each step.

'711 Patent, cls. 13-14.

"comprising" permits additional steps.
Genentech, Inc. v. Chiron Corp., 112
F.3d 495, 501 (Fed. Cir. 1997)

Reply (Paper 36), 23.

surface of a substrate. In the present disclosure, the term
"each" may not only necessarily mean "each of all," but can
also mean "each of a subset."

*'711 Patent, 5:6-8;
(Reply (Paper 36), 22-23).*

(C) Petition's Showing—Park at Least Renders Obvious Uniform Thickness

- Park expressly discloses "the thickness":

Pet. (Paper 1), 89-90.

The thickness of the etch-stop layer may be less than or equal to two times the thickness of the gate insulating film.

(160) is not limited to that shown in FIG. 7a and may vary. On the other hand, in this example, the thickness of the etch-stop layer (110) may be no more than twice the thickness of the blocking layer (162) to prevent the material included in the gate electrode layer (154) from flowing into the etch-stop layer (110).

each insulating layer (173, 174). In order to prevent the conductive material included in the gate electrode layer (154) from being included in the etch-stop layer (110), the thickness of the etch-stop layer (110) may be less than twice the thickness of the blocking layer (162).

Park, [0006], [0060], [0067]; Pet. (Paper 1), 89.

- Park's disclosures are consistent with a POSITA's knowledge that uniform thickness was beneficial to contact-hole etching.

Pet. (Paper 1), 90 (citing Ex. 1017, [0042]).

(C) PO's Arguments Fail—Claim 15 Summary

- 1) PO is incorrect that Park does not disclose a uniform etch-stop thickness. This moots PO's missing limitation argument.
- 2) Even if the limitation were missing (it's not), it would have been obvious to form Park's etch stop layers with atomic layer deposition (ALD), which produce a uniform thickness.
- 3) PO is incorrect that contact-hole etching renders obvious uniform thickness only of the top surface, not the side surface, because ALD deposits the etch stop on both the top and side surfaces.

Reply (Paper 36), 23-25.

(1) Park Discloses a Uniform Thickness

- Park's "the thickness" is consistent with its figures:

Reply (Paper 36), 23.

"Patent drawings may be useful in shedding light about the general shapes and relative sizes of elements of the claimed invention...."

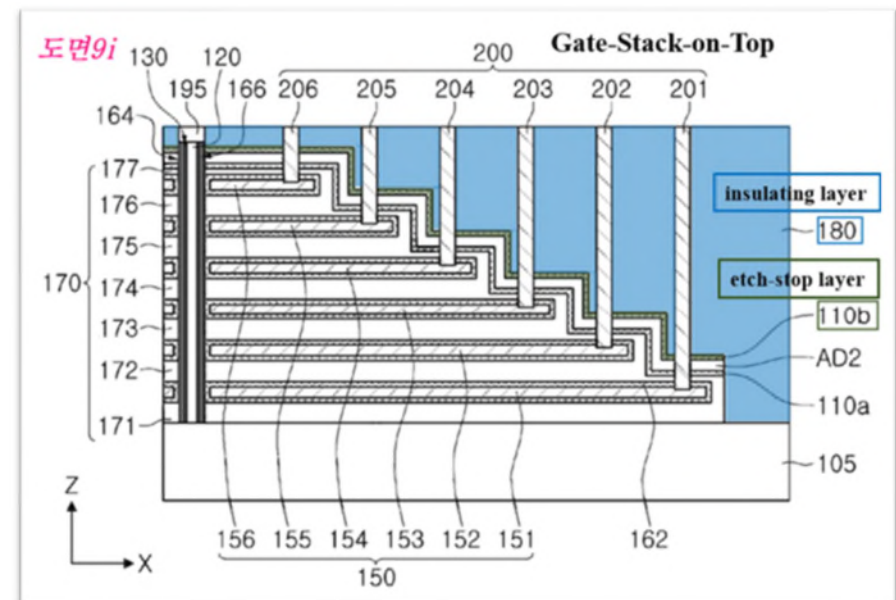
Regents of Univ. of Cal. v. Satco Prods., Inc., 2024 WL 4972639, at *3 (Fed. Cir. Dec. 4, 2024)

Reply (Paper 36), 23-24.

- PO's case law is inapposite:

- *Nystrom v. TREX Co.* applies "if the specification is **completely silent** on the issue."

Sur-Reply (Paper 44), 21.



*Park, Fig. 9i;
Pet. (Paper 1), 75.*

(2) The Petition's Evidence Is Consistent with Dr. Campbell's Concession During Trial: Park's ALD Produces the Beneficial Uniform Thickness

- The Petition's evidence confirms Park's uniform thickness disclosure: an etch-stop layer of uniform thickness on all steps was desirable to achieve a uniform contact-hole depth below the etch-stop layer.

Pet. (Paper 1), 90 (citing Ex. 1017, [0042]).
- Dr. Campbell testimony is consistent with the Petition's obviousness showing, because ALD creates "uniform films."

Q Why is it called atomic layer deposition?

A Because you're depositing a film basically one atom at a time. So you have extraordinary control over the thickness, and you're able to deposit into areas that are very difficult to get uniform films otherwise.

*Ex. 1027 (Campbell Dep.), 66:17-24
(Reply (Paper 36), 24).*

75. Then, as shown in Figure 9g, side openings T2 are back-filled with etch-stop material using an ALD or CVD process to form etch-stop layer 110a and 110b, as seen in Figure 9g. Park [0091]-[0092], [0105]-[0106].

*Campbell POR Decl. ¶ 75
(Reply (Paper 36), 24).*

(3) ALD Produces a Uniform Thickness Along the Staircase

- An ALD deposition on the top will also form a uniform thickness on the staircase.

Q And so, for example, at least using ALD, as we previously discussed, these layers can have -- can be conformal layers, uniform thickness, correct?

A Yes, as long as there's an ALD chemistry. Not every material is suitable for ALD.

*Ex. 1027 (Campbell Dep.), 117:9–22
(Reply (Paper 36), 24-25).*

Road Map

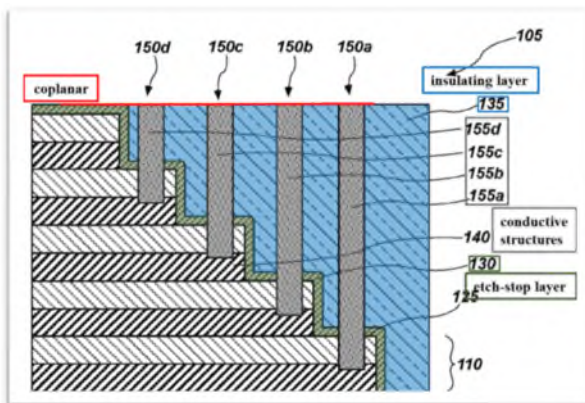
- I. The IPR Grounds
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- VII. Ground 4: Park in View of Fang**
 - A. Claim 7: Coplanar top surface
 - B. Claims 10 and 17: thickness range
 - C. Claim 15: uniform thickness
- VIII. Dr. Campbell Is Not a POSITA

(A) Petition's Showing—Park and Fang Combination Renders Obvious a "Coplanar" Top Surface

- Fang discloses the "coplanar" requirement (conductive structures, insulating layer, and portion of etch stop). Because Park already discloses removing unnecessary material, it would have been obvious to further remove the unnecessary material above the etch stop layer:

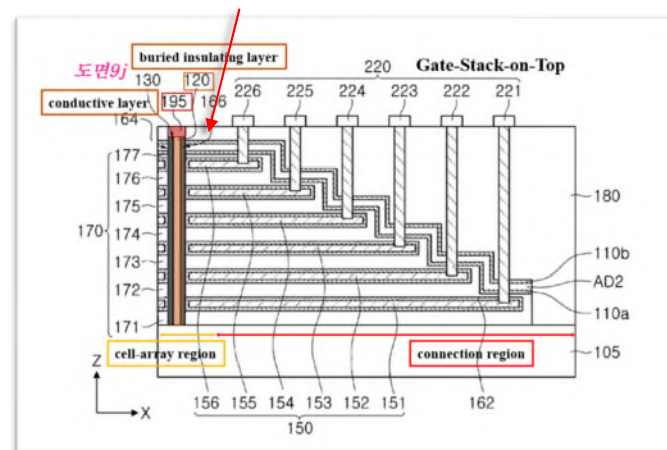
Pet. (Paper 1), 92-94

Fang



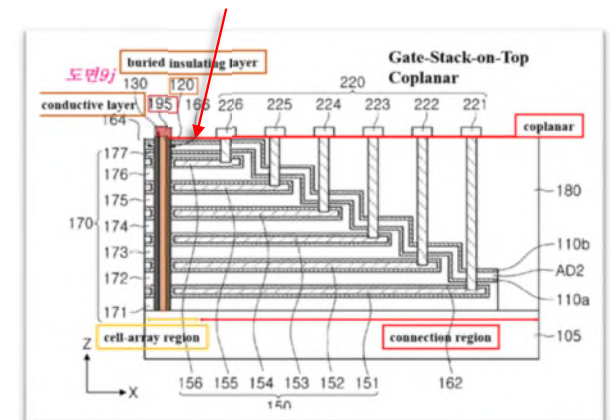
*Fang, Fig. 6
(Pet. (Paper 1), 92).*

Original of Park



*Park, Fig. 9j
(Pet. (Paper 1), 94).*

Modification of Park



*Park, Fig. 9j
(Pet. (Paper 1), 95).*

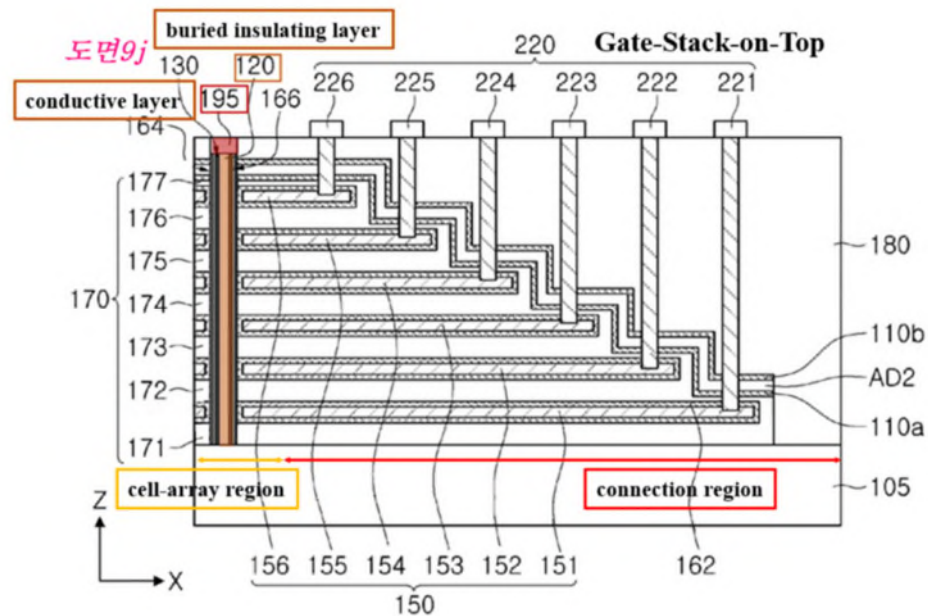
(A) PO's Arguments Fail—Claim 7 Summary

- 1) PO's arguments against motivation to combine and reasonable expectation of success incorrectly assume chemical mechanical polishing ("CMP") cannot occur without damaging protrusions above the top surface

Reply (Paper 36), 25-26.

(1) PO's Argument Incorrectly Assumes CMP Cannot Occur Without Damaging Protrusions Above the Top Surface

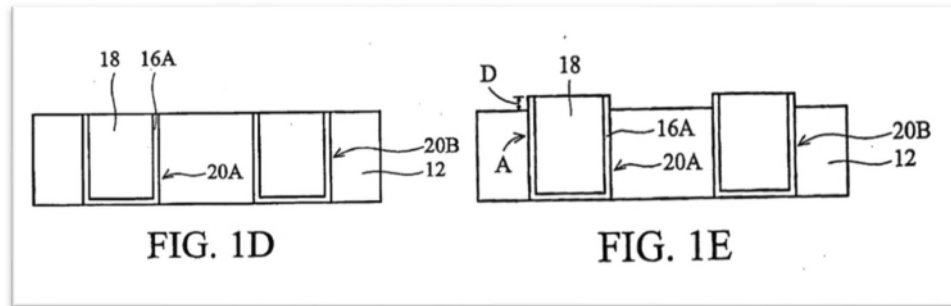
- PO's arguments hinge on the assumption that **CMP cannot occur after forming the etch-stop layer** due to risk of damaging the protruding conductive layer 195 that already exists at this step in Park's fabrication:



Reply (Paper 36), 25-26.

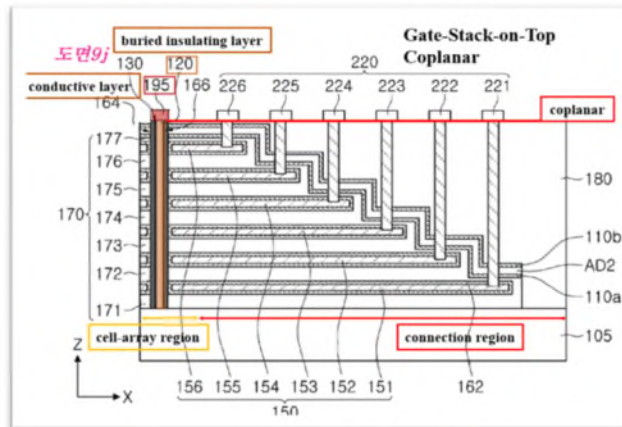
(1) PO's Argument Incorrectly Assumes CMP Cannot Occur Without Damaging Protrusions Above the Top Surface

- CMP was known to planarize a surface that includes protruding surfaces:



Ex. 1030, Figs. 1D-1E
(Reply (Paper 36), 26).

- Thus, it would have been obvious to CMP the unnecessary material:



Park, Fig. 9j
(Pet. (Paper 1), 95).

(B) PO's Arguments Fail—Claim 10 and 17 Summary

1. PO relies on the same, incorrect arguments against Kim in view of Fang.

Reply (Paper 36), 26.

2. Further supporting motivation and reasonable expectation of success, (1) Park's etch-stop thickness is in Fang's range and (2) Park discloses single-layer and multi-layer etch stops, and Park does not distinguish between the thickness of the etch-stop in these variations.

Reply (Paper 36), 27; Pet. (Paper 1), 101-102.

(1) Park in View of Fang Renders Obvious the 10-1000 nm Etch-Stop Thickness Range

- Park's claim 3 together with Dr. Campbell's testimony on the thickness of high-k dielectric layers puts Park's etch-stop thickness in Fang's range (5-100nm).

Reply (Paper 36), 26-27.

Claim 3

The nonvolatile memory device of Claim 2, further comprising:

wherein the thickness of the etch-stop layer is less than or equal to two times the thickness of the gate insulating films.

Park, 2 (Reply (Paper 36), 27).

Q So would you put the high-K layer around the gate layer within that extremely thin layer or outside that scope?

A Those layers are certainly not layers. They are an additional, maybe 2 to 10 nanometers. Even 2 is kind of small. Let's say 5 to 10, maybe 15 nanometers.

*Ex. 1027 (Campbell Dep.), 100:21-101:2
(Reply (Paper 36), 27).*

(2) Park in View of Fang Renders Obvious the 10-1000 nm Etch-Stop Thickness Range

- Park does not distinguish between the thickness of its single-layer and multi-layer etch stops.

Reply (Paper 36), 27.

The gate electrode layer (154) is surrounded by a blocking layer (162), and consequently between the channel region (130) and the gate electrode layer (154) is sequentially disposed, from the channel region (130), the tunneling layer (166), the charge storage layer (164), and the blocking layer (162). The thickness of the blocking layer (162), the charge storage layer (164), and the tunneling layer (166) included in the gate insulating film (160) is not limited to that shown in FIG. 7a and may vary. On the other hand, in this example, the thickness of the etch-stop layer (110) may be no more than twice the thickness of the blocking layer (162) to prevent the material included in the gate electrode layer (154) from flowing into the etch-stop layer (110).

Claim 1

A nonvolatile memory device comprising: a channel region extending in a direction perpendicular to an upper surface of a substrate;
a plurality of gate electrode layers disposed on the substrate so as to be adjacent to the channel region;
a plurality of pad regions wherein the plurality of gate electrode layers extends to different lengths along one direction;
at least one etch-stop layer disposed on the plurality of gate electrode layers and spaced apart from the plurality of gate electrode layers in the plurality of pad regions; and
a plurality of contact plugs connected with the plurality of gate electrode layers.

Park, [0060], Claim 1 (Reply (Paper 36), 27).

(C) Petition's Showing: Park in View of Fang Renders Obvious a Uniform Etch-Stop Thickness—Claim 15

- Fang expressly discloses an etch stop that is "substantially uniform."

[0021] The etch stop material 130 may be formed over the stairs 125 at a thickness ranging from about 50 Å to about 1000 Å, such as from about 50 Å to about 600 Å, or from about 100 Å to about 500 Å. The thickness of the etch stop material 130 on the stairs 125 may be substantially uniform. Since the etch stop material 130 is not substantially removed by the etch chemistry used to remove the nitride materials 120 of the tiers 110, the thickness of the etch stop material 130 may be minimal and yet still provide desired etch stop properties.

Fang, [0021] (Pet. (Paper 1), 99-100).

- Uniform thickness on all steps was desirable to achieve a uniform contact-hole depth below the etch-stop layer. This prevents or reduces over-etching or under-etching.

Pet. (Paper 1), 89-90, 99-100 (citing Ex. 1017, [0042]).

- Fang's teaching is consistent with Park's "the thickness" disclosures.

Pet. (Paper 1), 89-90, 99-100.

(C) Park in View of Fang Renders Obvious a Uniform Etch-Stop Thickness—Claim 15

- PO's recycled arguments fail for the same reasons as its arguments against Park (Ground 3) for claim 15.

Reply (Paper 36), 27; POR (Paper 27) 69–71; Sur-Reply (Paper 44), 22 n.7.

Road Map

- I. The IPR Grounds
- II. The '711 Patent
- III. Claim Construction
- IV. Ground 1: Kim in View of a POSITA's Knowledge
- V. Ground 2: Kim in View of Fang
- VI. Ground 3: Park in View of a POSITA's Knowledge
- VII. Ground 4: Park in View of Fang
- VIII. Dr. Campbell Is Not a POSITA

PO Did Not Dispute the POSITA Qualifications in its POR

B. Person of Ordinary Skill in the Art

Petitioner has proposed that a “POSITA in the field of the ’711 patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).” Pet. 27. Petitioner has further proposed that the “POSITA would have been aware of and generally knowledgeable about 3D NAND’s structure, how it is manufactured, and its component parts.” *Id.* YMTC does not dispute this definition of a POSITA for purposes of these proceedings.

POR (Paper 27), 7.

Dr. Campbell Admitted that He Does Not Have Design Experience

Sitting here today, you do not know the typical height or the typical range of heights of a step in a staircase structure as of 2017, is that correct?

A I could make an estimate of it because we know roughly how many transistors are in the string.

But I'm being deposed as an expert in this area, and I'm not an expert in the design of the device.

*Ex. 1027 (Campbell Dep.), 32:16-25
(Reply (Paper 36), 28).*

A The '711 Patent is primarily a process in -- a process description.

The design, if you will, where the transistors go and so forth is really modest by comparison. I don't know if the processing people are saying which layers go where and how thick they are and how you're going to etch things. Those are all process parameters.

*Ex. 1027 (Campbell Dep.), 134:17-135:3, 150:20-151:5;
Sur-Reply (Paper 44), 25.*



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DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

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