Micron Technology, Inc. (Petitioner)
v.
Yangtze Memory Technologies Company, Ltd. (Patent Owner)

IPR2025-00117 (US Patent 10,672,711)

Patent Owner YMTC's Demonstratives

March 13, 2026

YMTC
Exhibit 2012
Micron v. YMTC
IPR2025-00117

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Four Asserted Grounds Fail

Petition

Petitioner challenges the claims on the following grounds:

Ground 1: Claims 1-9, 11-16, and 18-19 are obvious over Kim in view of a POSITA's knowledge;

Ground 2: Claims 10 and 17 are obvious over Kim in view of Fang;

Ground 3: Claims 1-6, 8-9, 11-16, and 18-19 are obvious over Park in view of a POSITA's knowledge; and

Ground 4: Claims 7, 10, 15, and 17 are obvious over Park in view of Fang.

Pet. 11

Agenda

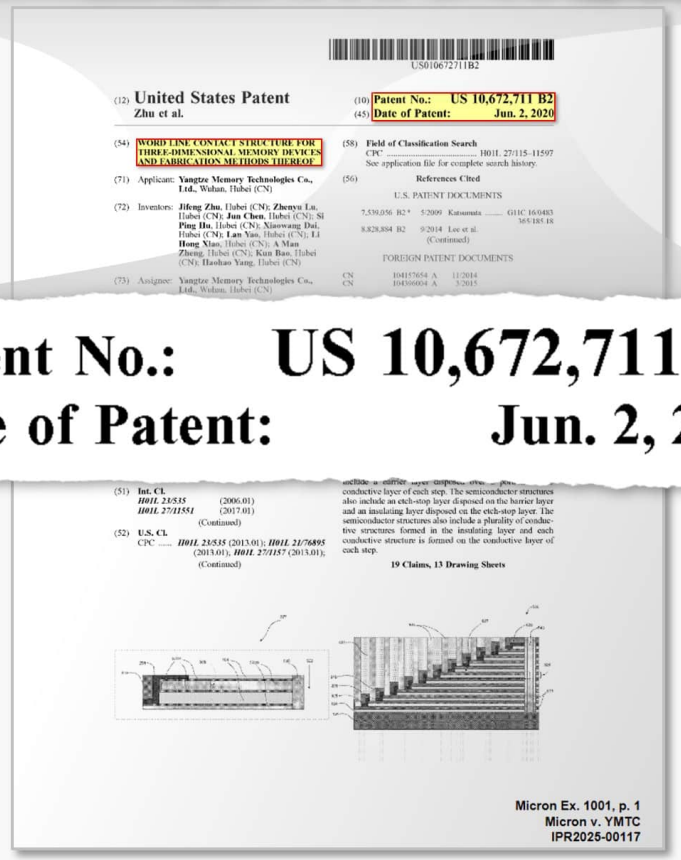
- '711 Patent
- Petitioner's Flawed Obviousness Theories
  - Ground 1 (Kim) Fails
  - Ground 2 (Kim + Fang) Fails
  - Ground 3 (Park) Fails
  - Ground 4 (Park + Fang) Fails

Agenda

- '711 Patent
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  - Ground 2 (Kim + Fang) Fails
  - Ground 3 (Park) Fails
  - Ground 4 (Park + Fang) Fails

The '711 Patent

WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF



US010672711B2

(12) **United States Patent**
Zhu et al.

(10) **Patent No.: US 10,672,711 B2**
(45) **Date of Patent: Jun. 2, 2020**

(54) WORD LINE CONTACT STRUCTURE FOR THREE-DIMENSIONAL MEMORY DEVICES AND FABRICATION METHODS THEREOF

(71) Applicant: **Yangtze Memory Technologies Co., Ltd.**, Wuhan, Hubei (CN)

(72) Inventors: **Jifeng Zhu**, Hubei (CN); **Zhenyu Lu**, Hubei (CN); **Jun Chen**, Hubei (CN); **Si Ping Hu**, Hubei (CN); **Xiaowang Dai**, Hubei (CN); **Lan Yao**, Hubei (CN); **Li Hong Xiao**, Hubei (CN); **A Man Zheng**, Hubei (CN); **Kun Bao**, Hubei (CN); **Haohao Yang**, Hubei (CN)

(73) Assignee: **Yangtze Memory Technologies Co., Ltd.**, Wuhan, Hubei (CN)

(58) **Field of Classification Search**
CPC H01L 27/115–11597
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

7,539,056 B2 * 5/2009 Katsumata G11C 16/0483 365/185.18
8,828,884 B2 9/2014 Lee et al.
(Continued)

FOREIGN PATENT DOCUMENTS

CN 104157654 A 11/2014
CN 104396004 A 3/2015

Patent No.: US 10,672,711 B2
Date of Patent: Jun. 2, 2020

(51) **Int. Cl.**
H01L 23/535 (2006.01)
H01L 27/11551 (2017.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 23/535*** (2013.01); ***H01L 21/76895*** (2013.01); ***H01L 27/1157*** (2013.01);
(Continued)

conductive layer of each step. The semiconductor structures also include an etch-stop layer disposed on the barrier layer and an insulating layer disposed on the etch-stop layer. The semiconductor structures also include a plurality of conductive structures formed in the insulating layer and each conductive structure is formed on the conductive layer of each step.

19 Claims, 13 Drawing Sheets

Micron Ex. 1001, p. 1
Micron v. YMTC
IPR2025-00117

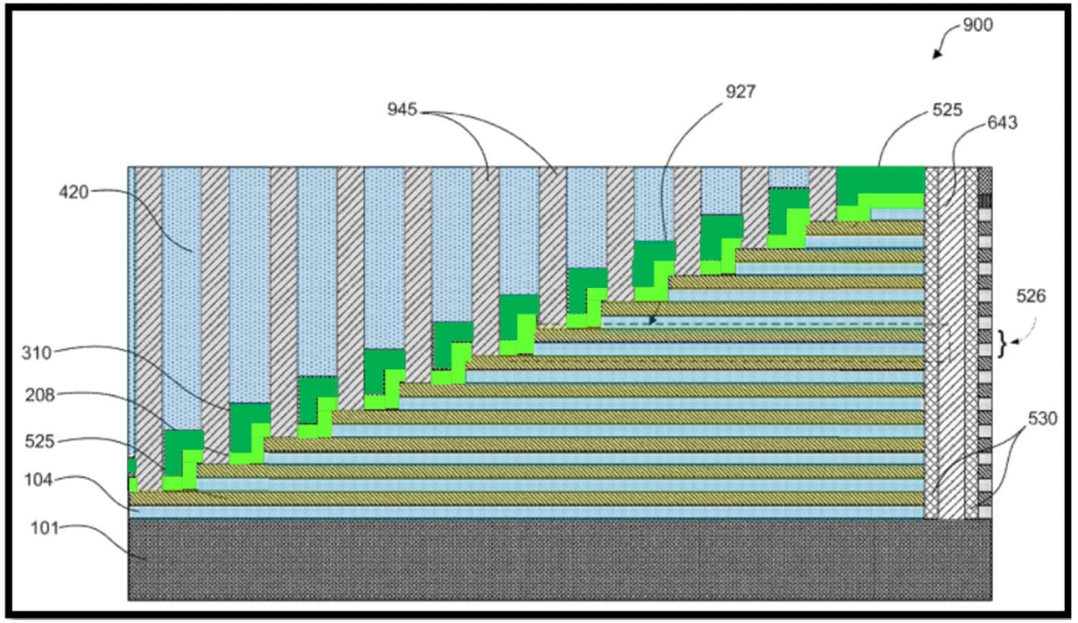
Ex. 1001 ('711 Patent)

'711 Patent - 3D NAND Difficulties

Various embodiments in the present disclosure provide methods and structures for improving word line contacts for 3D memory devices. In the present disclosure, a single lithography mask can be used to form contact areas for word lines of 3D memory array. By adding an etch-stop film over the staircase structure, openings of the vertical interconnect access (VIA) contacts for each level of the staircase structure can be formed simultaneously. The etch-stop film protects underlying layers during etching processes that form contact VIAs. The etch-stop film is exposed on each level of the staircase structure by a selective etching process, and then removed by reverse selective etching. Accordingly, the disclosed methods and structures can improve fabrication yield and reduce cost. The methods and structures described herein can be used to form semiconductor interconnect structures for inter-connecting components at different layers with an uneven topology.

Ex. 1001 ('711 Patent), 5:54-6:3

'711 Patent at Fig. 9A



No.	Structure
525	Gate Stack
104	First Insulating Layer
208	Second Insulating Layer
310	Etch-Stop Layer
420	Third Insulating Layer
945	Vertical Interconnect Access Conductive Structures

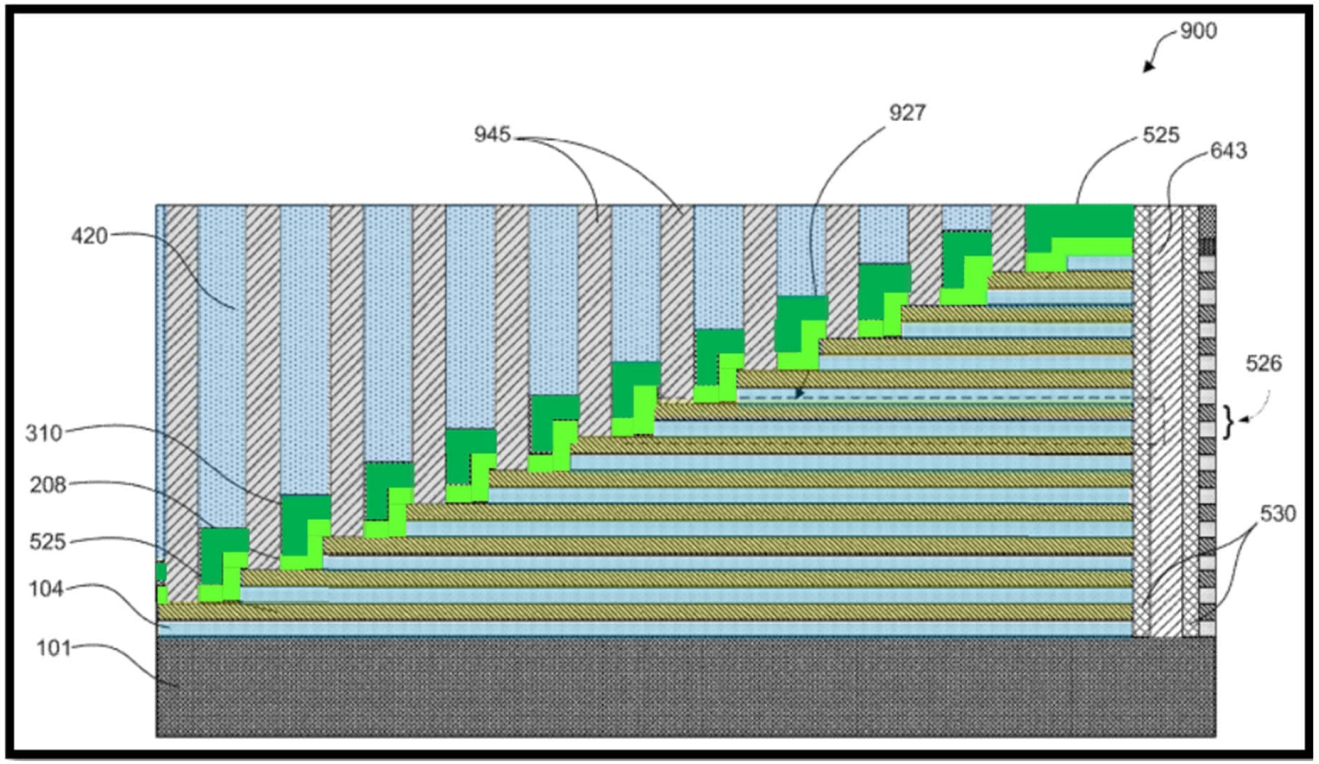
POR 5; Ex. 1001 ('711 Patent), Fig. 9A

'711 Patent's Solution

1. A semiconductor structure, comprising:
a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;
a barrier layer disposed over a portion of the gate stack of the each step;
an etch-stop layer disposed on the barrier layer;
an insulating layer disposed on the etch-stop layer; and
a plurality of conductive structures formed in the insulating layer, wherein each conductive structure is formed on the conductive layer of the each step.

Ex. 1001 ('711 Patent), Claim 1

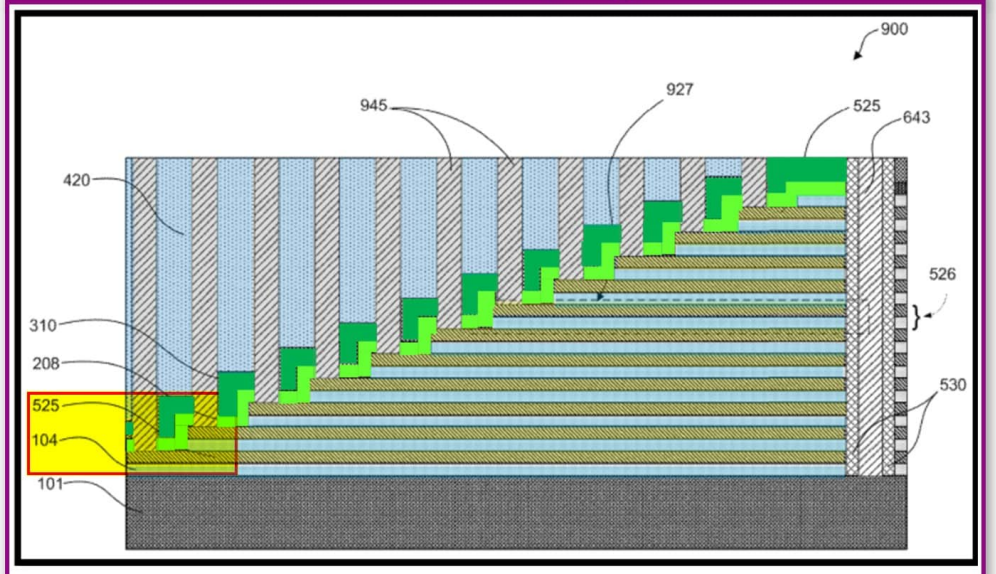
'711 Patent at Fig. 9A



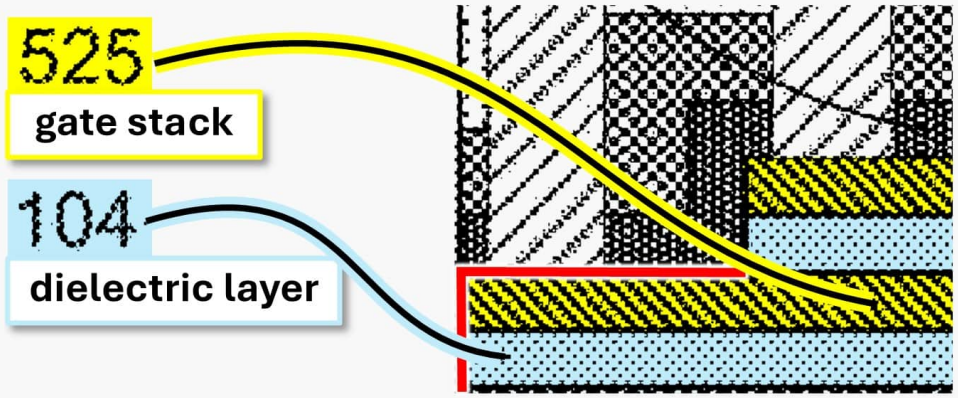
POR 5; Ex. 1001 ('711 Patent), Fig. 9A

Claims 1 And 13: "each step comprises a gate stack disposed over a dielectric layer"

'711 Patent, Fig. 9A



POR 15; Ex. 1001 ('711 Patent), Fig. 9A



1. A semiconductor structure, comprising:
a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;
a barrier layer disposed over a portion of the gate stack of the each step;
an etch-stop layer disposed on the barrier layer;
an insulating layer disposed on the etch-stop layer; and
a plurality of conductive structures formed in the insulating layer, wherein each conductive structure is formed on the conductive layer of the each step.

Ex. 1001 ('711 Patent), Claim 1

13. A semiconductor structure, comprising:
a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;
an etch-stop layer disposed on a portion of the gate stack of the each step;
an insulating layer disposed on the etch-stop layer; and
a plurality of conductive structures formed in the insulating layer and extending through the etch-stop layer and the high-k dielectric layer, wherein each conductive structure directly contacts the corresponding conductive layer of each step.

Ex. 1001 ('711 Patent), Claim 13

Agenda

- '711 Patent
- **Petitioner's Flawed Obviousness Theories**
  - **Ground 1 (Kim) Fails**
  - Ground 2 (Kim + Fang) Fails
  - Ground 3 (Park) Fails
  - Ground 4 (Park + Fang) Fails

Ground 1: Petition Relies Only On Kim's Fig. 17A-22B Embodiment

1. A semiconductor structure, comprising:
a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;
* * *

Ex. 1001 ('711 Patent), Claims 1, 13

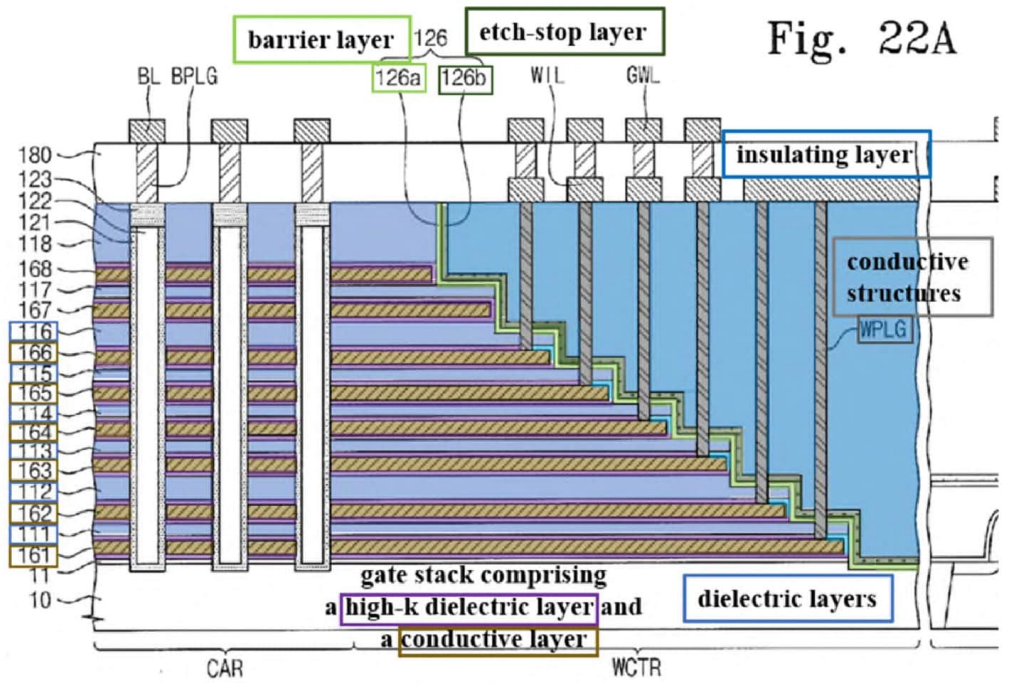
13. A semiconductor structure, comprising:
a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;
* * *

Petition

This Petition relies on Kim's Figures 17A-22B embodiment comprising an etch-stop layer and a barrier layer. Kim discloses other embodiments, *e.g.*, Figures 5A-14B.

Pet. 29

Petition



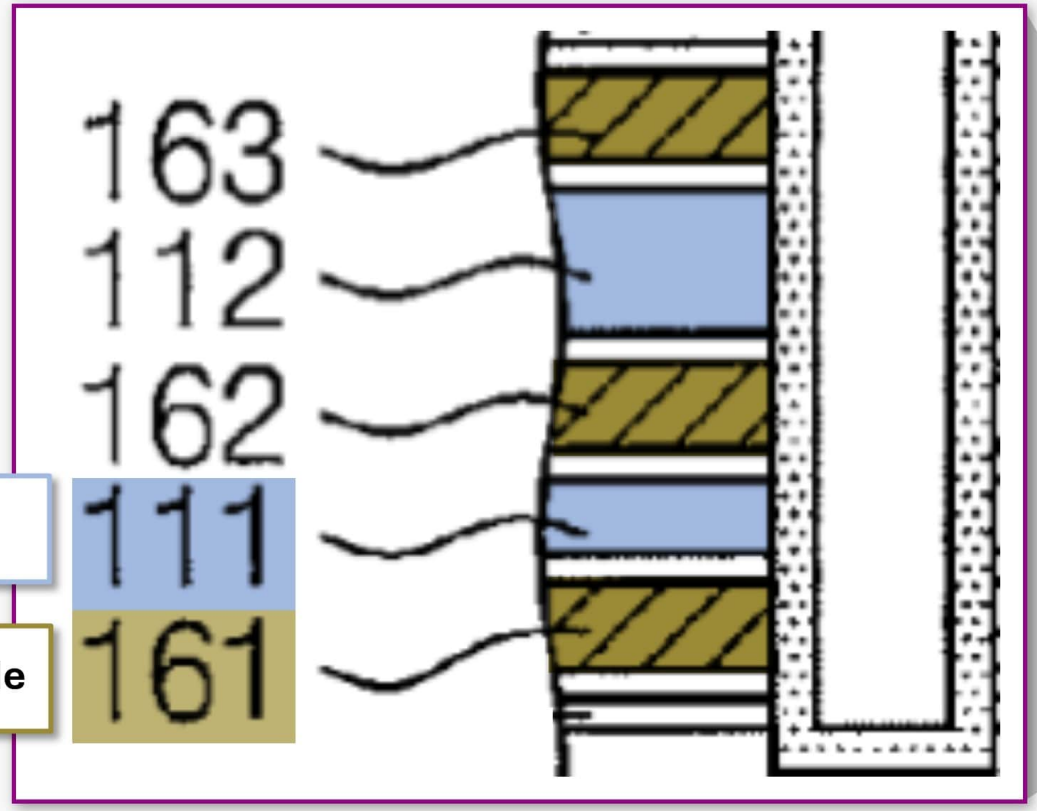
Pet. 28; Ex. 1005 (Kim), Figs. 17A-22B

Ground 1: Kim's Fig. 17A-22B Embodiment Is Gate-Stack-On-*Bottom*

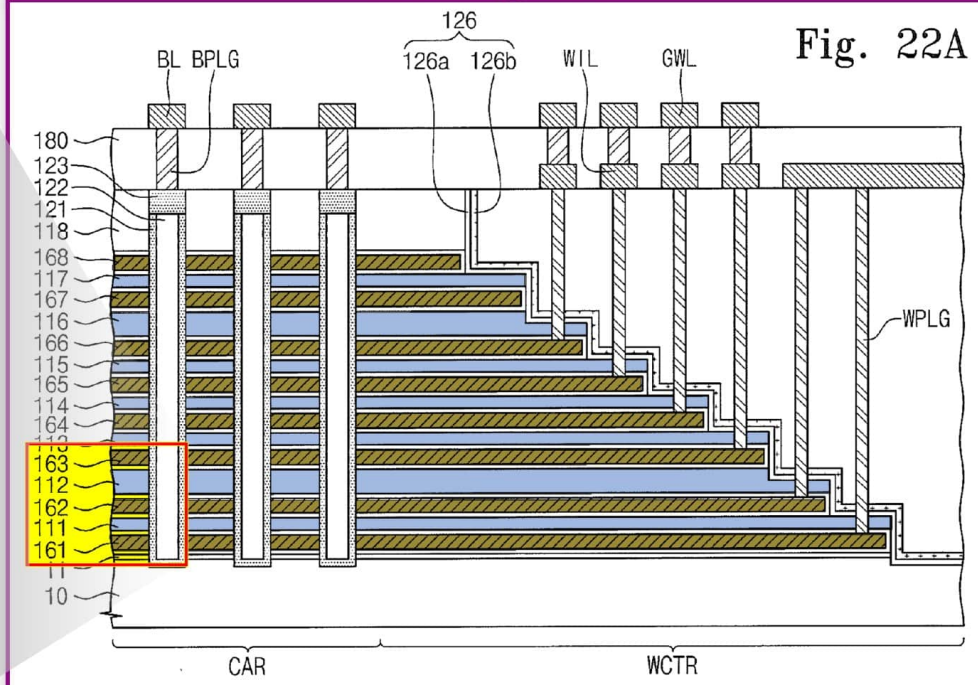
1. A semiconductor structure, comprising:
a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;
* * *

Ex. 1001 ('711 Patent), Claims 1, 13

13. A semiconductor structure, comprising:
a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;
* * *



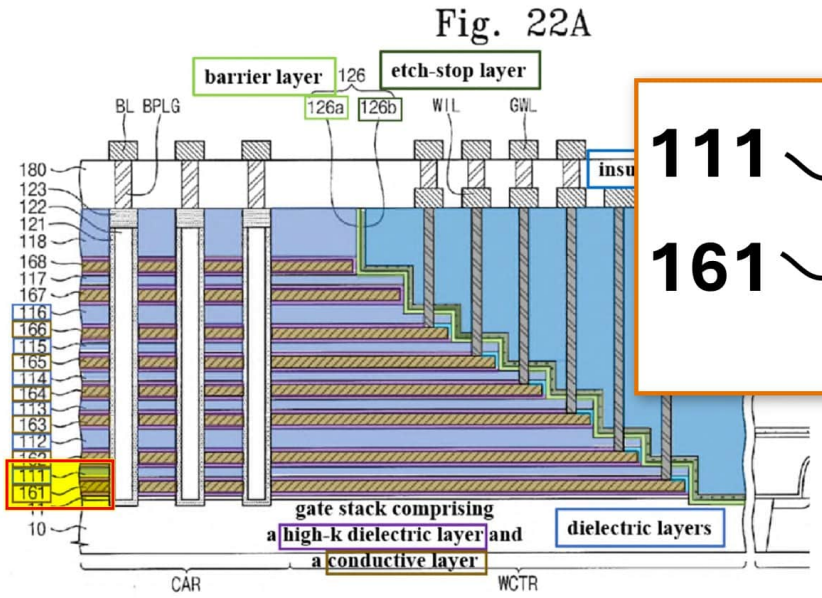
Kim Fig. 22A



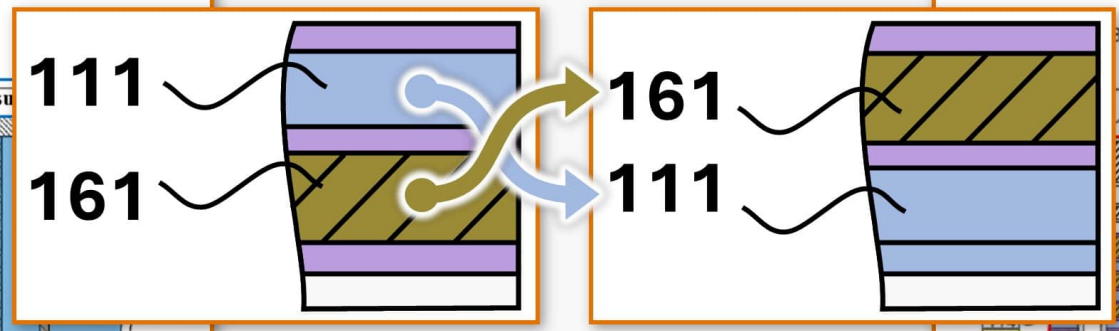
POR 16; Ex. 1005 (Kim), Fig. 22A

Ground 1: Petitioner's Hindsight Modification Of Kim's Fig. 22A Embodiment

Petition

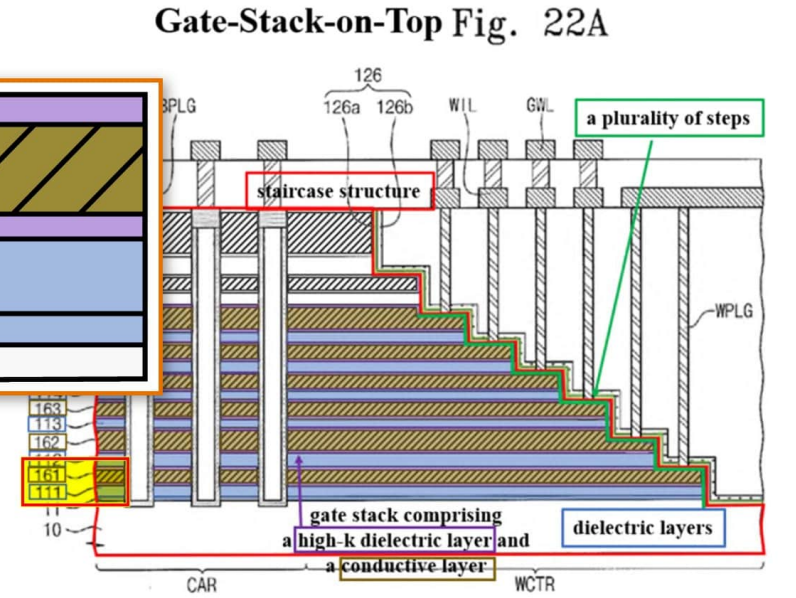


Pet. 28; POR 29; Ex. 1005 (Kim), Figs. 17A-22B



demonstrative graphics

Petition



Pet. 40 (modified by Petitioner)

Petition

Kim discloses the gate-stack-on-top layer ordering even though its figures show the opposite order. §IX.A. This teaching of the gate-stack-on-top layer

Pet. 32; Ex. 1003 (Petitioner's Expert Banerjee Decl.) ¶ 80

A Motivation Is Required To Combine Embodiments From A Single Reference

In Re Stepan

"Whether a rejection is based on combining disclosures from multiple references, combining multiple embodiments from a single reference, or selecting from large lists of elements in a single reference, there must be a motivation to make the combination and a reasonable expectation that such a combination would be successful, otherwise a skilled artisan would not arrive at the claimed combination."

***In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017) (quoted at POR 45; POSR 6)**

Ground 1: Insufficient Motivation To Modify Kim's Fig. 22A

Petition

Additionally, a POSITA would have known that either order was a common alternative. For example, Chen discloses both orders side-by-side:

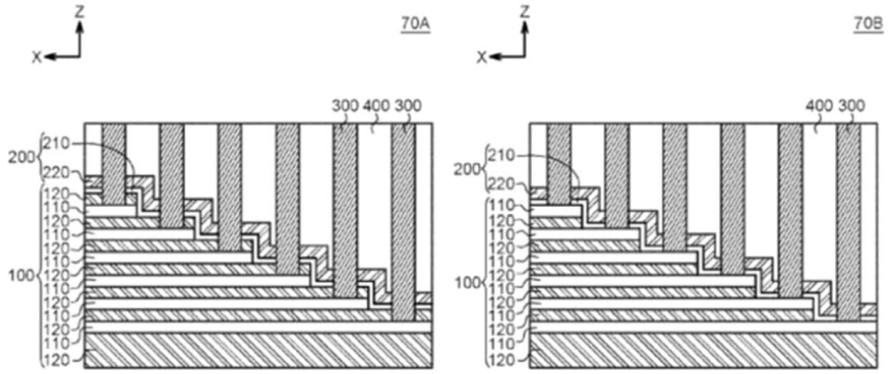


FIG. 7A FIG. 7B

Chen, Figs. 7A (dielectric on top), 7B (conductor on top), [0044]-[0046]. A POSITA would have known that either order was routine, highly predictable, and would have had a reasonable expectation of success for implementing a gate-stack-on-top embodiment. Banerjee ¶ 81.

At a minimum, Kim's teaching on reversing the order represents a "known technique" that is at least "a *suitable* option" for the Figures 17A-22B embodiment.

Pet. 33-34

Petitioner Identified No Benefit To Reversing Layers

Petitioner's Expert Dr. Banerjee

Q. All right. Now, in your declaration you don't list any benefits to reversing the order of the layers; right?

A. I don't think so. I mean, I cited to other prior arts such as Chen showing that it could go either way it's. A binary choice. Either the gate stack is going to be on top or below and Chen shows two figure side-by-side so it's a matter of simple choice, you can see that.

Q. It's a matter of simple choice, but there's no reason you give to go one way or the other; right?

A. No, I did not.

Ex. 2008 (Petitioner's Expert Dr. Banerjee Dep.), 35:12-36:1

Intel Is Distinguishable

Petitioner

Intel

"That Kabemoto and Bauman address the same problem and that Bauman's cache was a known way to address that problem is precisely the reason that there's a motivation to combine under *KSR* and our precedent."

***Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023)**

Patent Owner

CommScope

"Petitioner *has not* identified a need or problem known in the field of endeavor at the time of invention or explained how Fukushima helped address that problem."

***CommScope, Inc. v. TQ Delta, LLC*, IPR2022-01012, 2023 WL 7491179, at *11 (P.T.A.B. Nov. 13, 2023) (Paper 31) (italics original)**

Petitioner's "problem" Is Mere Attorney Argument

Petitioner's Reply

to combine under *KSR*…." *Id.* The petitioner "never had to show that replacing" one known mechanism for addressing the same problem (here, constructing a staircase structure using one gate-stack-dielectric order) with another known mechanism (the alternative order) "was an 'improvement' in a categorical sense"; petitioner needed only to show that it was a "suitable option." *Id.* at 1381.

Reply 5 (citing *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1381 (Fed. Cir. 2023))

Kim's Fig. 22A Materially Differs From Other Embodiments

Fig. 22A shows the gate-stack-on-*bottom*

Pet. 32; POR 16-17

Fig. 22A has two etch-stop layers

POR 20; POSR 10-11

Fig. 22A has high-k dielectric layer surrounding conductive layer of each step

POR 39-40; POSR 10

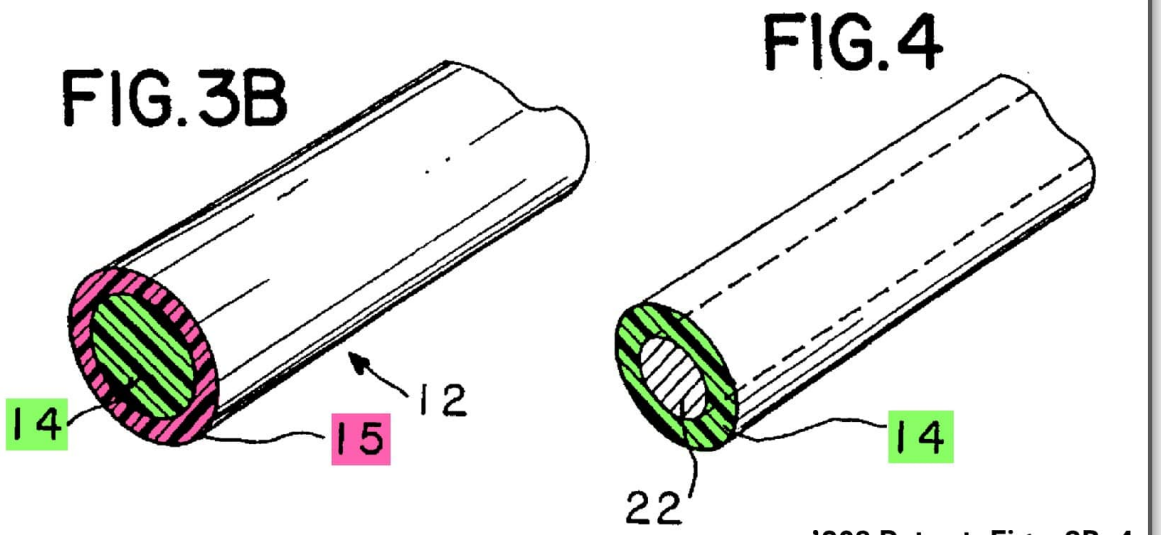
Distinct materials result in different etch chemistries and safety margins

POR 20, 26

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Boston Scientific Is Distinguishable

U.S. Patent No. 5,545,208 From *Boston Scientific*



'208 Patent, Figs. 3B, 4

Boston Scientific

"One of ordinary skill would have been motivated to coat the metal stent of figure 4, including its layer 14 of drug-containing polymer, with a second layer of polymer, like layer 15 depicted in figure 3B, that is substantially free of an elutable material.

Just as the stent in figure 3B benefits from the two layers, one containing a drug and the other limiting diffusion of the drug, so would the stent in figure 4 benefit from the same two coating layers."

***Bos. Sci. Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 (Fed. Cir. 2009**

Boston Scientific Is Distinguishable

Intel

"The [*Boston Scientific*] court found that the motivation to add the second coating layer from the first embodiment to the stent in the second embodiment was the expectation of achieving the same benefit … The court's analysis in *Boston Scientific* indicates that adjacent placement alone is not sufficient.

Accordingly, the fact that Yano describes the fifth embodiment shown in Figure 5 immediately after discussing the fourth embodiment shown in Figure 4 is not by itself sufficient to show a reason or motivation to combine the features of those embodiments in the manner set forth by Petitioner."

***Intel Corp. v. Tela Innovations, Inc.*, IPR2019-01521, 2021 WL 912764, at *9 (P.T.A.B. Mar. 9, 2021) (Paper 65)**

A POSITA Would Not Have Had A Reasonable Expectation Of Success In Reversing Layers Of Kim

Different etch depths

POR 25

Change to etch parameters

POR 25; Ex. 2009 (Dr. Campbell Sec. Decl.) ¶ 41

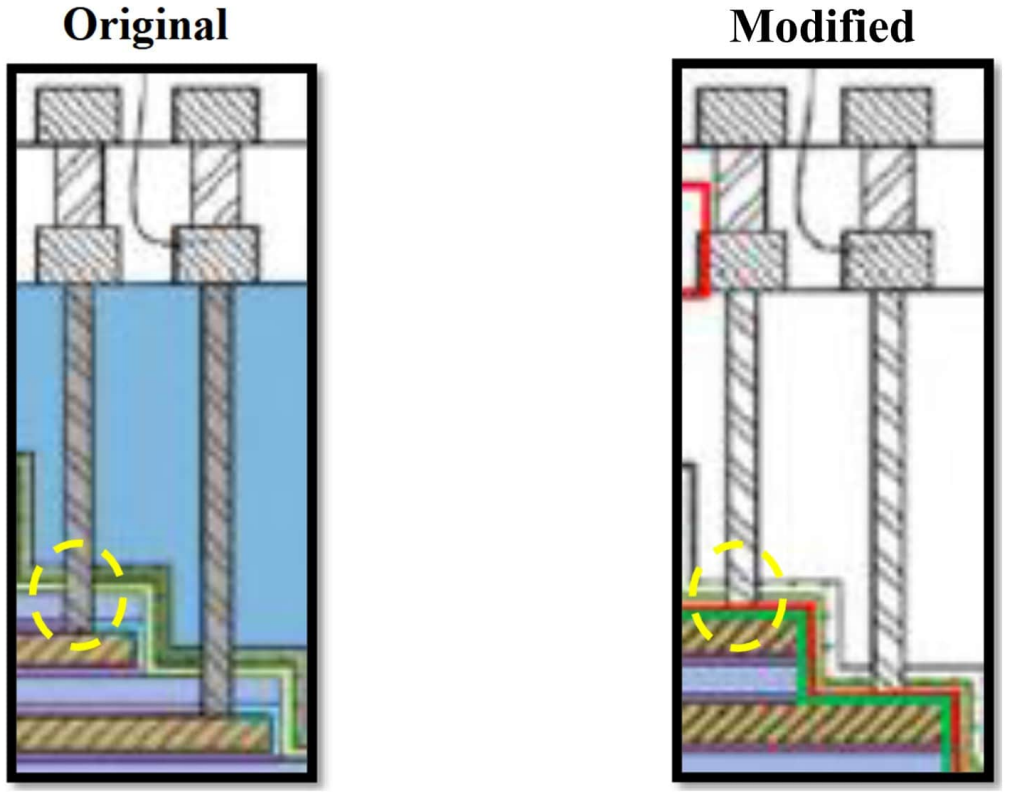
Increased risk of short circuiting

POR 25-26

Petitioner's expert said "details matter"

Ex. 2008 (Petitioner's Expert Dr. Banerjee Dep.), 45:9-12

Dr. Campbell Second Declaration



Ex. 2009 (Dr. Campbell Sec. Decl.) ¶ 41

POSR 25-26; Ex. 2009 (Petitioner's Expert Dr. Campbell Sec. Decl.) ¶ 41

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 1:
Claims 14 And 15 Would Not Have Been Obvious

14. The semiconductor structure of claim **13**, wherein the etch-stop layer is formed on a side surface and a top surface of each step.

Ex. 1001 ('711 Patent), Claim 14

15. The semiconductor structure of claim **14**, wherein thicknesses of the etch-stop layer is the same on the side and top surfaces of each step.

Ex. 1001 ('711 Patent), Claim 15

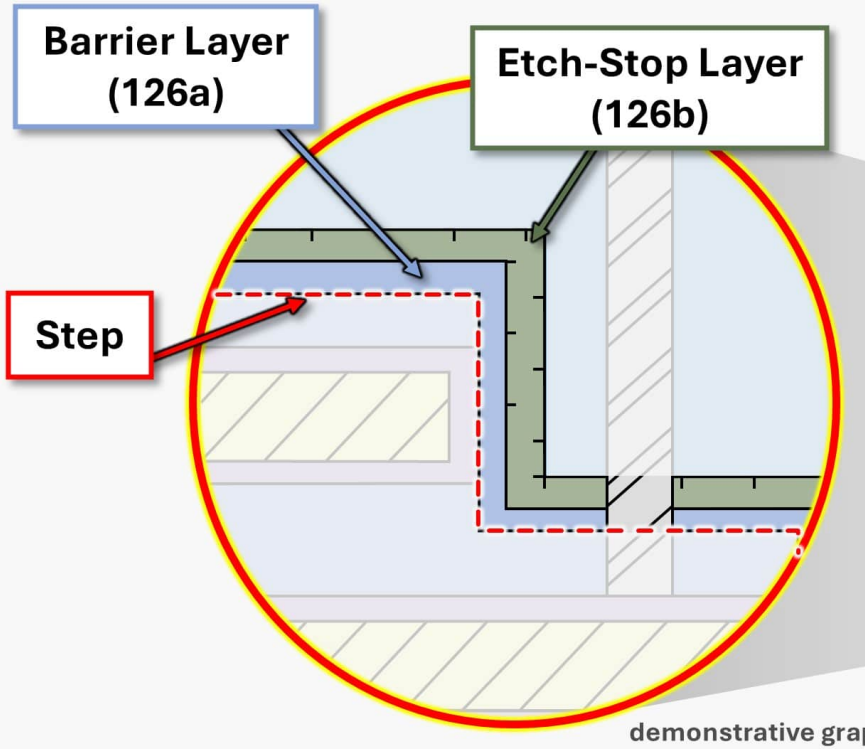
Petitioner's Construction Renders "surface" Superfluous

14. The semiconductor structure of claim 13, wherein the etch-stop layer is formed on a side surface and a top surface of each step.

Ex. 1001 ('711 Patent), Claim 14

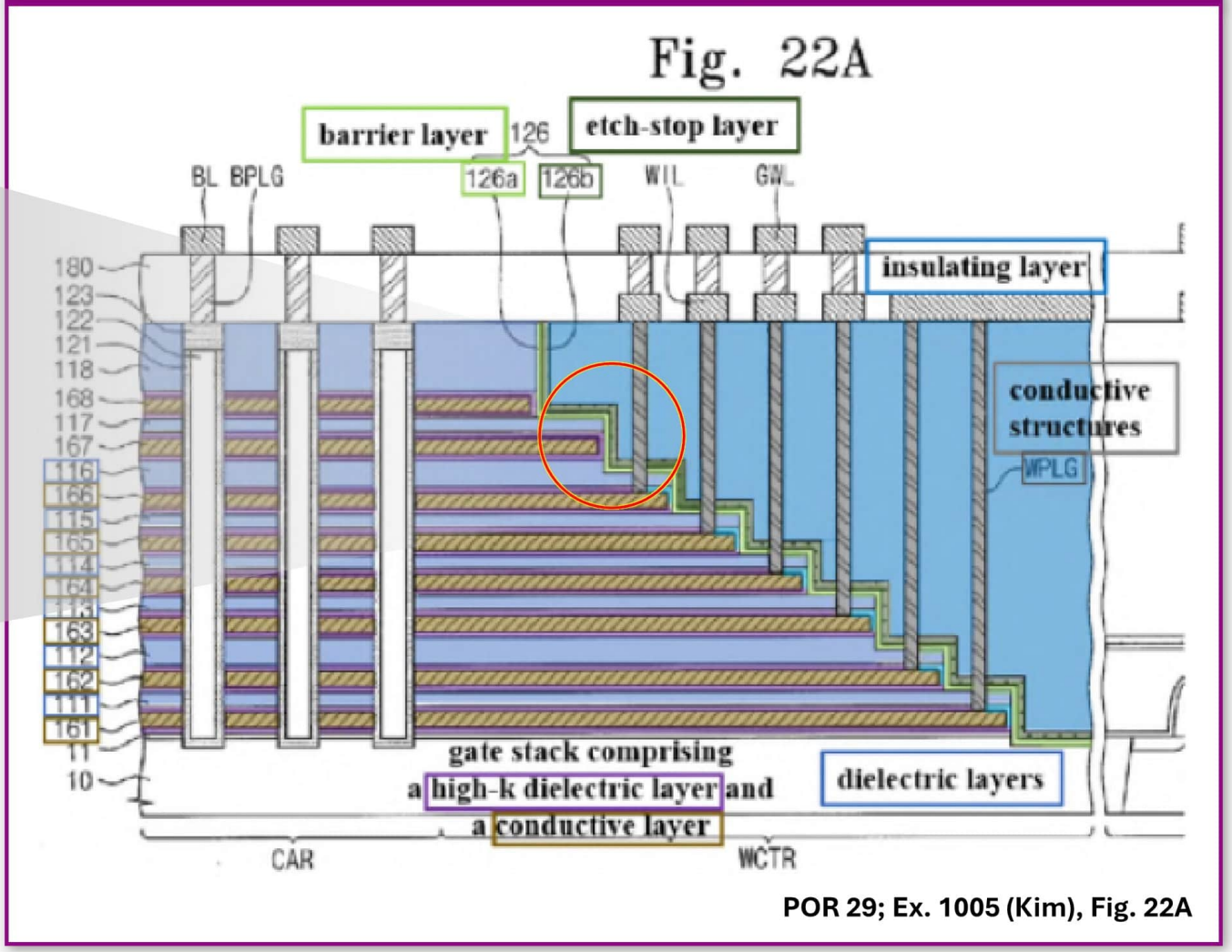
***Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.*, 853 F.3d 1272, 1288 n.10 (Fed. Cir. 2017);**
***Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006)**

Kim Does Not Disclose The Etch-Stop Layer "on a side surface and a top surface of each step"



demonstrative graphic

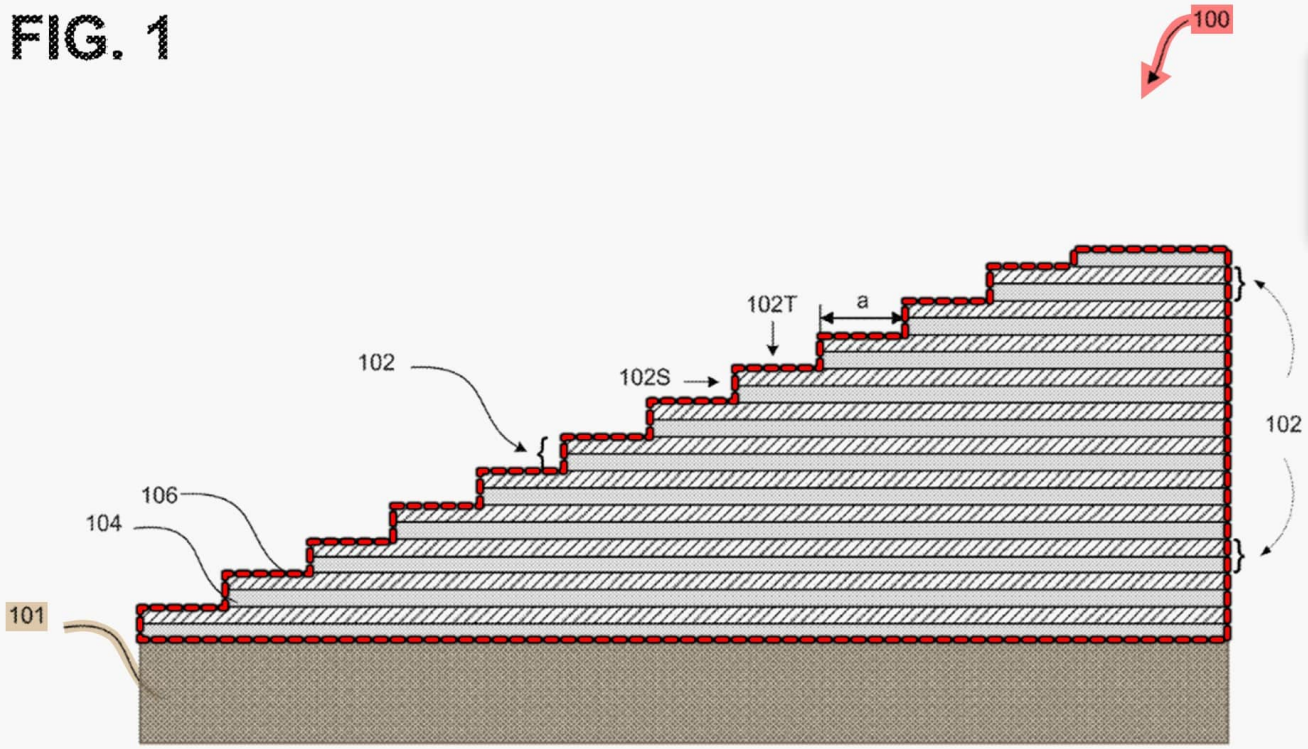
Patent Owner Response



POR 29; Ex. 1005 (Kim), Fig. 22A

When '711 Patent Refers To "on a top surface," It Describes Direct Contact

FIG. 1



Ex. 1001 ('711 Patent), Fig. 1

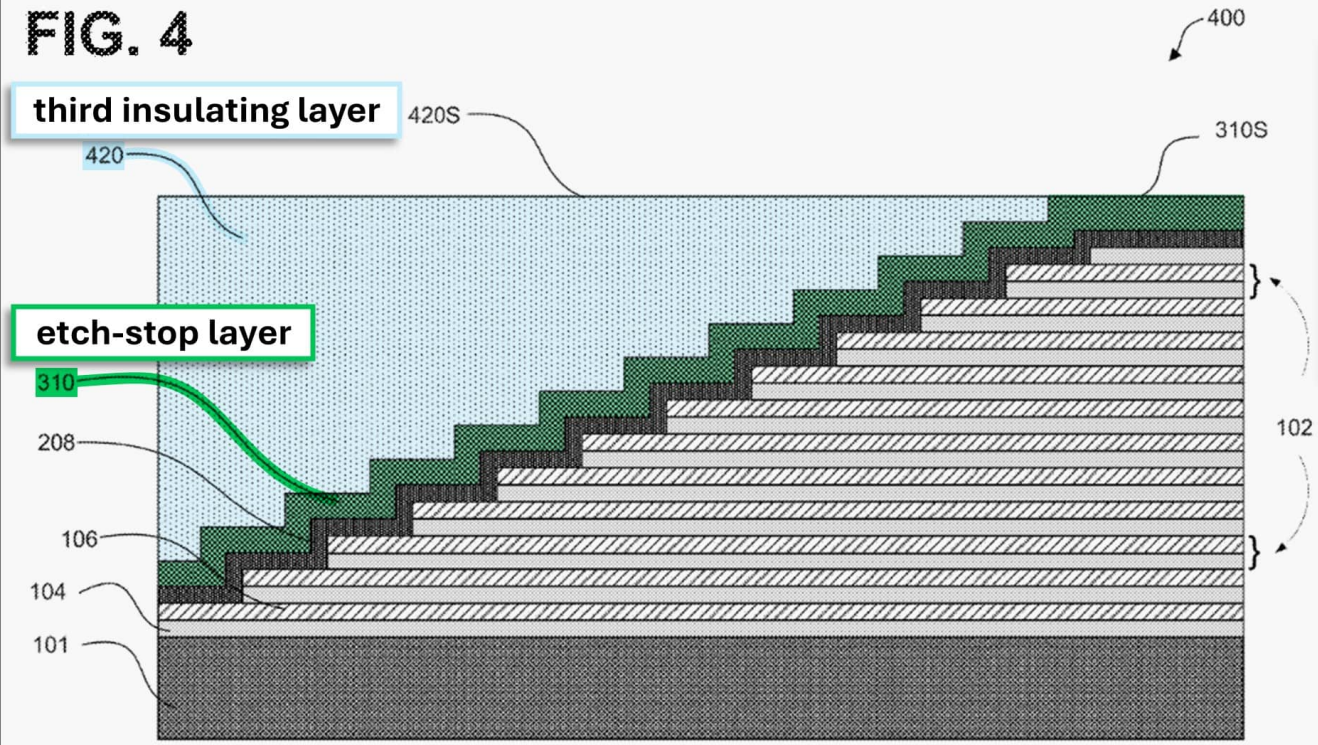
FIG. **1** illustrates a staircase structure **100** having an alternating layer stack on a top surface of a substrate **101**.

Ex. 1001 ('711 Patent), 6:4-5

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

When '711 Patent Refers To "on a top surface," It Describes Direct Contact

FIG. 4



Ex. 1001 ('711 Patent), Fig. 4

At process step **1040**, a third insulating layer is disposed on the top surface of the etch-stop layer over the staircase structure, followed by an optional planarization process, to form a surface coplanar with the uppermost portion of the etch-stop layer. The third insulating layer can be the third

Ex. 1001 ('711 Patent), 12:19-23

Petitioner Changes Constructions For "on a side surface and a top surface of each step"

Petitioner's Construction

"plain and ordinary meaning"

Pet. 26

Petitioner's Reply Construction

Lexicography

"directly on" and "'on' [as] something with an intermediate feature or a layer therebetween"

Reply 2-3 (original alteration)

See Ralph Lauren Corp. v. Lexos Media IP, LLC, IPR2018-01755, 2020 WL 1488393, at *5 (P.T.A.B. Mar. 25, 2020) (Paper 22) (declining to address new construction first raised by Petitioner in reply), *aff'd sub nom. Ralph Lauren Corp. v. Hirshfeld*, 852 F. App'x 540 (Fed. Cir. 2021).
POSR 3, 10-12; POR 8.

Petitioner's Argument That "surface" Must Mean "exterior" Is Nonsensical

Petitioner's Reply

superfluous…." POR, 14. It does not. The terms "side/top surface" provide a reference point to the ***exterior*** of the step. Were the claims to just recite "top" or "side" of the step, the claim scope would be ambiguous as to whether, for example, the etch-stop layer may be in contact with the step's interior. Regardless, the

Reply 3

Patent Owner's Sur-Reply

Petitioner now argues that "surface" specifies only that the layer is on the step's exterior rather than interior. Reply 3. This new argument is unsupported and non-sensical. Petitioner does not identify what constitutes the "step's interior" or how the claimed etch-stop layer would be on it. Nor does Petitioner explain why the meaning of "surface" would not also include an *interior* surface. Petitioner cannot

POSR 3

Petitioner Waived Reliance On Kim's Embodiments With Single Etch-Stop

Petition

it covers…." *Id.*, [0144]. Thus, *the etch-stop layer* (second stop layer 126b) *is formed on a side surface and a top surface of each step*. *Id.*, [0256]; Ex. 1001, 4:1-

Pet. 60

Petitioner's Reply

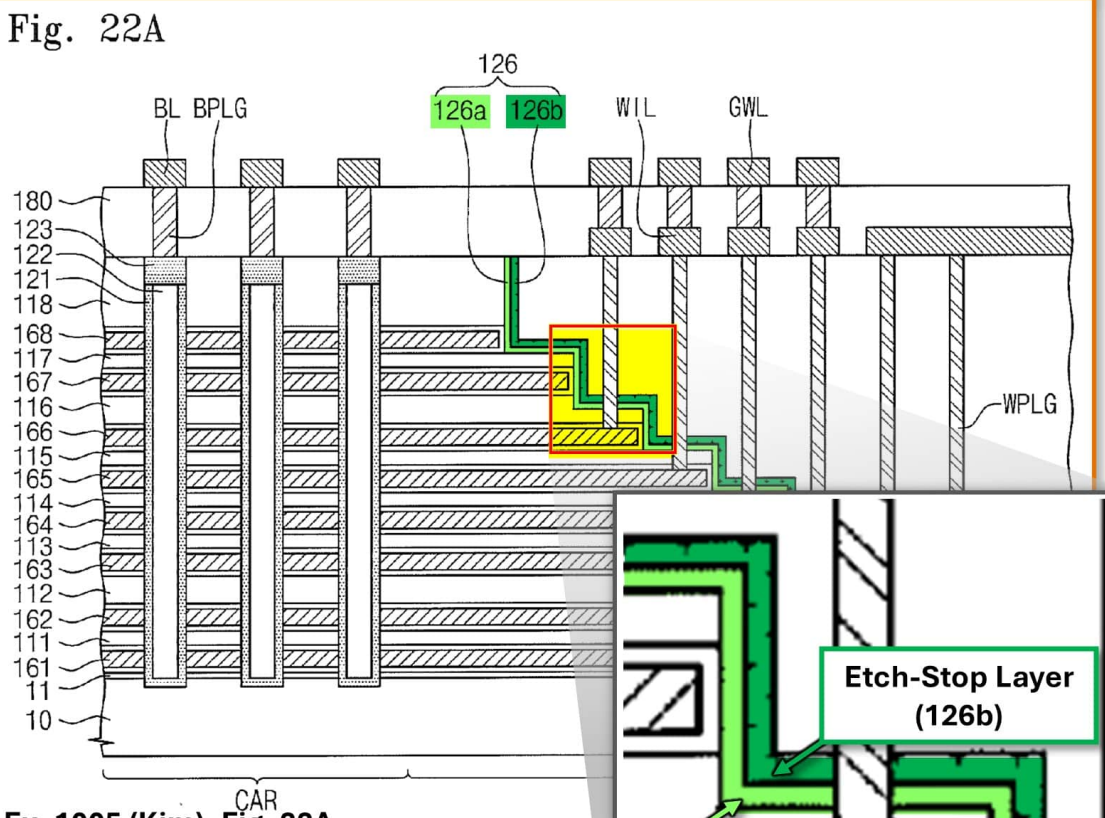
Should the Board adopt PO's construction, Kim still renders the claims obvious.[6] Kim discloses a single-etch-stop variant of the Figure 17A–22B embodiment, which illustrates that the barrier layer is optional. This satisfies claims 14–15 under PO's construction because the etch-stop layer would ***directly contact*** each step's side and top surfaces. Kim, [0185]–[0186]; Banerjee2 ¶¶39–40.

Reply 12; POSR 10-11; Ex. 1028 (Petitioner's Expert Banerjee Reply Decl.) ¶¶ 39-40

***Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1367 (Fed. Cir. 2015)**
(finding "no error in the Board's rejection of Ariosa's reliance, in its Reply submissions, on previously unidentified portions of a prior-art reference to make a meaningfully distinct contention.")

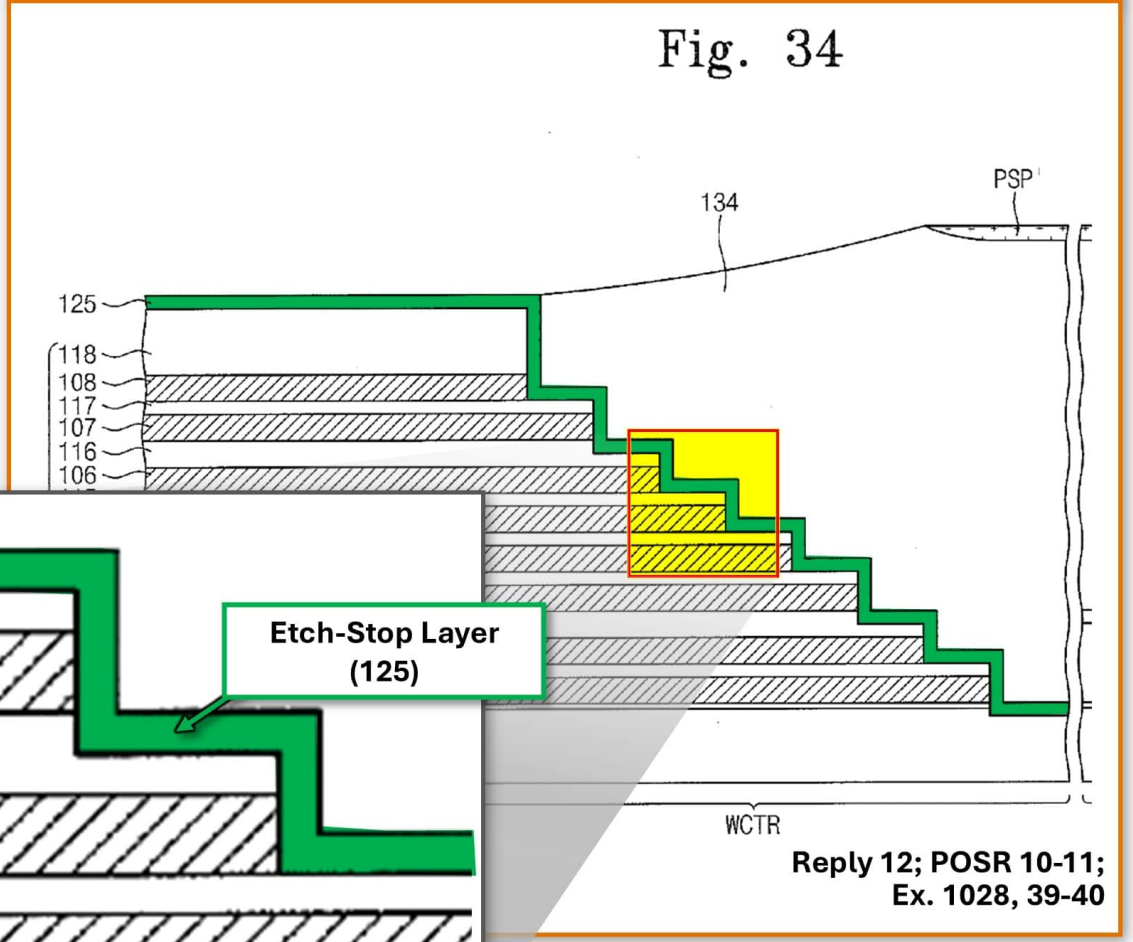
Petitioner Waived Reliance On Kim's Embodiments With Single Etch-Stop

Petition



Ex. 1005 (Kim), Fig. 22A

Reply



Reply 12; POSR 10-11; Ex. 1028, 39-40

Axonics Does Not Support Petitioner's Reliance On New Embodiment

Axonics

We have held that a petitioner may not in reply rely on new prior art to teach a claim limitation. *See Intelligent Bio-Sys.*, 821 F.3d at 1369 (holding a reply brief and declaration exceeded the proper scope for a reply because they cited "a number of non-patent literature references which were not relied upon to support unpatentability in the Petition").

But that is not the situation here: Axonics did not rely on new prior art in its reply. We leave for another day the question of whether, when presented with a new claim construction, a petitioner can rely in its reply on new embodiments from the prior art references that were relied on in the petition. … Here, Axonics, in the reply, relied on the same embodiments as it relied on in the petition.

Axonics, Inc. v. Medtronic, Inc., 75 F.4th 1374, 1383-84 (Fed. Cir. 2023), *dismissed*, 2025 WL 471226 (Fed. Cir. Feb. 12, 2025)

Agenda

- '711 Patent
- **Petitioner's Flawed Obviousness Theories**
  - Ground 1 (Kim) Fails
  - **Ground 2 (Kim + Fang) Fails**
  - Ground 3 (Park) Fails
  - Ground 4 (Park + Fang) Fails

Ground 2:
Kim And Fang Do Not Render Obvious Claims 10 And 17

10. The semiconductor structure of claim **1**, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.

Ex. 1001 ('711 Patent), Claim 10

17. The semiconductor structure of claim **13**, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.

Ex. 1001 ('711 Patent), Claim 17

Petitioner Relies On Fang To Modify Kim's Etch-Stop Layer

Petitioner's Expert Dr. Banerjee

Q. All right. You don't offer an opinion in your declaration that Kim discloses any specific thickness of that second stop layer; right?

A. For the second stop, are you referring to 126B?

Q. Yes.

A. Yeah. No, Kim does not have any disclosure of thicknesses, which is why we use the combination with Fang.

Ex. 2008 (Petitioner's Expert Dr. Banerjee), 42:8-16

Petitioner Relied On Fang's CDSN Layer, Which Is Not In Kim

Petition

If more is required (it is not), Kim in view of Fang's etch-stop layer teaching renders claim 10 obvious. Fang discloses an analogous semiconductor structure with an etch-stop layer. Fang, Fig. 6, [0020]. To start, Kim's and Fang's etch-stop layers are similar. For example, both of their etch-stop layers may comprise silicon nitride. Kim, [0187]; Fang, [0022]. Fang's etch-stop layer "may be formed by conventional

Pet. 63; Ex. 1003 (Petitioner's Expert Banerjee Decl.) ¶ 130

Kim

125*a*. In some embodiments, the first stop layer **125***a* may be formed of silicon oxide and the second stop layer **125***b* may be formed of silicon nitride. In other embodiments, the etch stop layer **125** may be a single layer, which is formed of a material having an etch selectivity with respect to the sacrificial layers SC**1** to SC**8** and the insulating layers **111** to **118**.

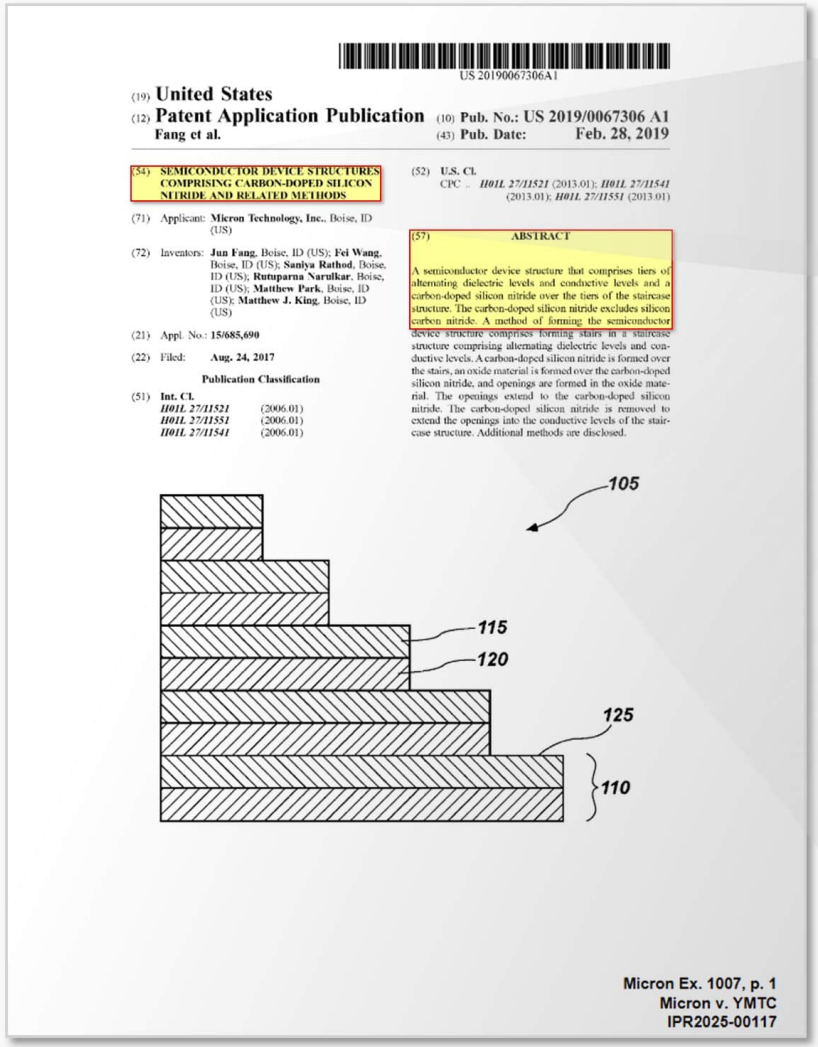
Ex. 1005 (Kim), [0187]

Fang

[0022] The etch stop material **130** may be a carbon-doped silicon nitride including from about 1 wt % of carbon to about 30 wt % of carbon, such as from about 1 wt % of

Ex. 1007 (Fang), [0022]

Fang Discloses CDSN Etch-Layer



US 20190067306A1

(19) United States

(12) Patent Application Publication

Fang et al.

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(43) Pub. Date: Feb. 28, 2019

(54) SEMICONDUCTOR DEVICE STRUCTURES COMPRISING CARBON-DOPED SILICON NITRIDE AND RELATED METHODS

(71) Applicant: Micron Technology, Inc., Boise, ID (US)

(72) Inventors: Jun Fang, Boise, ID (US); Fei Wang, Boise, ID (US); Saniya Rathod, Boise, ID (US); Rutuparna Narulkar, Boise, ID (US); Matthew Park, Boise, ID (US); Matthew J. King, Boise, ID (US)

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H01L 27/11541 (2006.01)

(52) U.S. Cl.
CPC ... H01L 27/11521 (2013.01); H01L 27/11541 (2013.01); H01L 27/11551 (2013.01)

(57) ABSTRACT

A semiconductor device structure that comprises tiers of alternating dielectric levels and conductive levels and a carbon-doped silicon nitride over the tiers of the staircase structure. The carbon-doped silicon nitride excludes silicon carbon nitride. A method of forming the semiconductor device structure comprises forming stairs in a staircase structure comprising alternating dielectric levels and conductive levels. A carbon-doped silicon nitride is formed over the stairs, an oxide material is formed over the carbon-doped silicon nitride, and openings are formed in the oxide material. The openings extend to the carbon-doped silicon nitride. The carbon-doped silicon nitride is removed to extend the openings into the conductive levels of the staircase structure. Additional methods are disclosed.

Micron Ex. 1007, p. 1
Micron v. YMTC
IPR2025-00117

Ex. 1007 (Fang)

SEMICONDUCTOR DEVICE STRUCTURES COMPRISING CARBON-DOPED SILICON NITRIDE AND RELATED METHODS

(57) **ABSTRACT**

A semiconductor device structure that comprises tiers of alternating dielectric levels and conductive levels and a carbon-doped silicon nitride over the tiers of the staircase structure. The carbon-doped silicon nitride excludes silicon carbon nitride. A method of forming the semiconductor

Kim Does Not Disclose CDSN Etch-Layer

Kim

[0186]

to the stacked layer structure ST. For instance, the etch stop layer **125** may be formed of a material having an etch selectivity with respect to the sacrificial layers SC**1** to SC**8** and the insulating layers **111** to **118** of the stacked layer structure ST. In some embodiments, the etch stop layer **125** may include at least one of silicon carbide (SiC), silicon nitride (SiN), silicon oxynitride (SiON) and/or silicon oxycarbide (SiOC).

Ex. 1005 (Kim), [0186]

Kim

[0187]

125*a*. In some embodiments, the first stop layer **125***a* may be formed of silicon oxide and the second stop layer **125***b* may be formed of silicon nitride. In other embodiments, the etch

Ex. 1005 (Kim), [0187]

Undisputed That Etch Rate Depends On Material Composition

Petitioner's Expert Dr. Banerjee

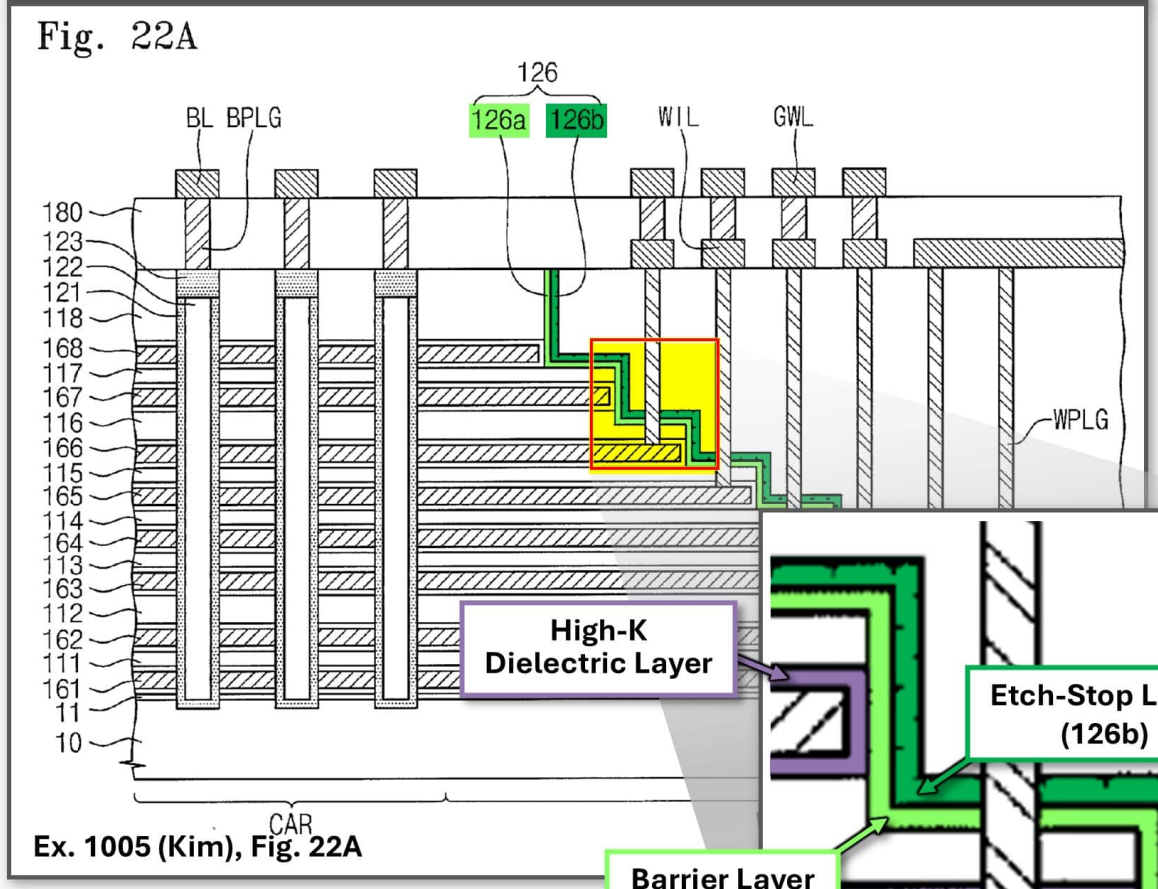
Q. Is it fair to say that the carbon doping has an impact on the etch rate of the silicon nitride?

A. It could. If you left everything else the same in the etch process, changing the composition in general will change the etch rate.

Ex. 2008 (Petitioner's Expert Dr. Banerjee), 55:4-9

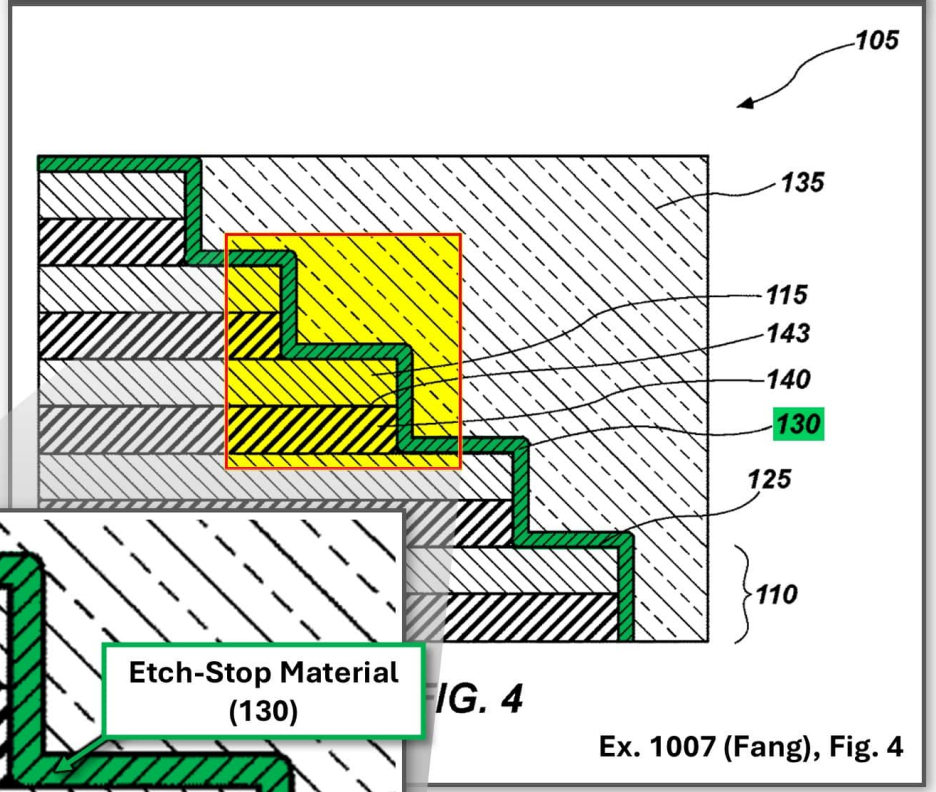
Petitioner Relies On Fang To Modify Kim's Etch-Stop Layer

Kim



Ex. 1005 (Kim), Fig. 22A

Fang



Ex. 1007 (Fang), Fig. 4

Other Structural Differences Undermine Combination

Kim's high-k dielectric layer

POSR 16-17; POR 39-40.

Different structures have different thicknesses

POSR 17-18

Chen's thickness applies to tunneling problem not present in Kim

POSR 18

Agenda

- '711 Patent
- **Petitioner's Flawed Obviousness Theories**
  - Ground 1 (Kim) Fails
  - Ground 2 (Kim + Fang) Fails
  - **Ground 3 (Park) Fails**
  - Ground 4 (Park + Fang) Fails

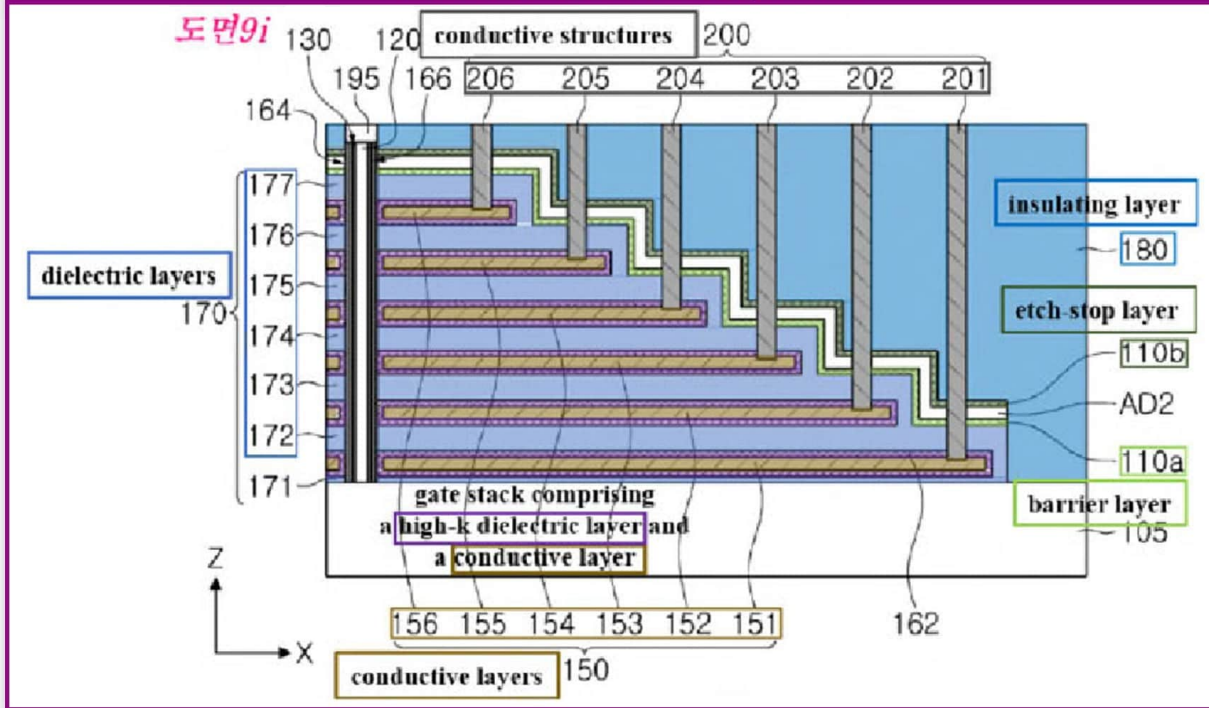
Ground 3: Petition Relies On Park's Figs. 5, 9a-9j Embodiment Alone

1. A semiconductor structure, comprising:
a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;
* * *

13. A semiconductor structure, comprising:
a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;
* * *

Ex. 1001 ('711 Patent), Claims 1, 13

Patent Owner's Response



POR 43; Ex. 1006 (Park), Fig. 9i

Petition

This Petition relies on the embodiment shown in Figures 5 (perspective view) and 9a-9j (cross-sectional views), comprising an etch-stop layer and a barrier layer. Park, [0100]. Park discloses other embodiments, *e.g.*, one illustrated in Figures 4 (perspective view) and 8a-8m (cross-sectional views). *Id.*, [0073].

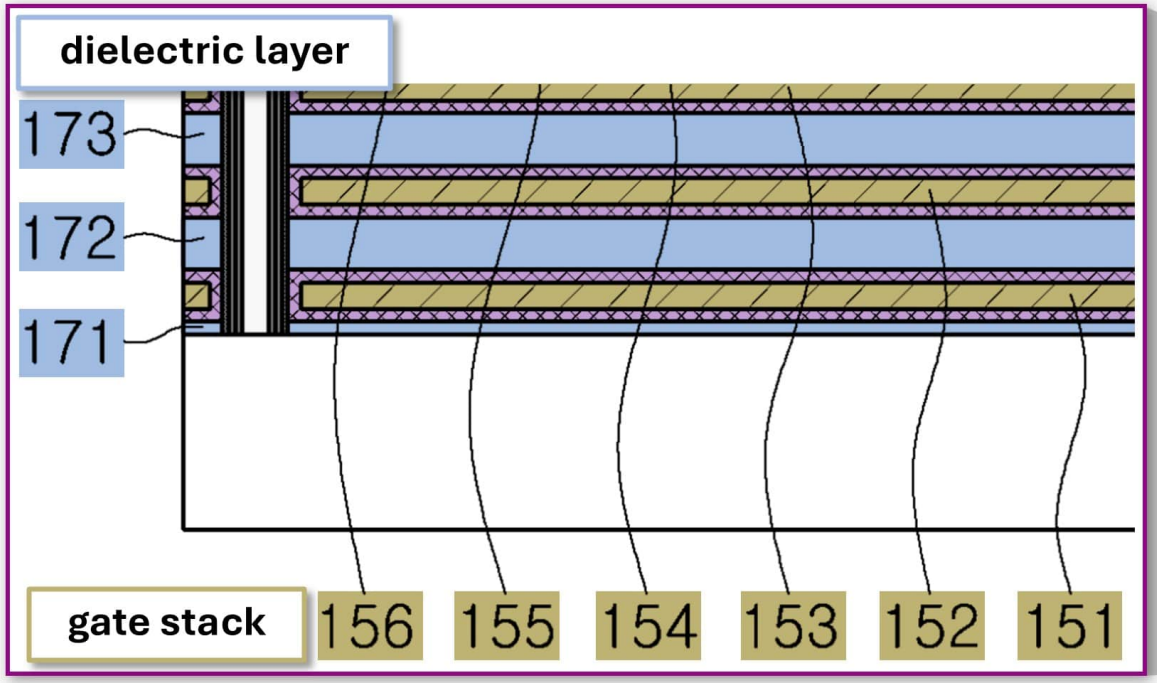
Pet. 31

Ground 3: Park's Figs. 5, 9a-9j Embodiment Is Gate-Stack-on-*Bottom*

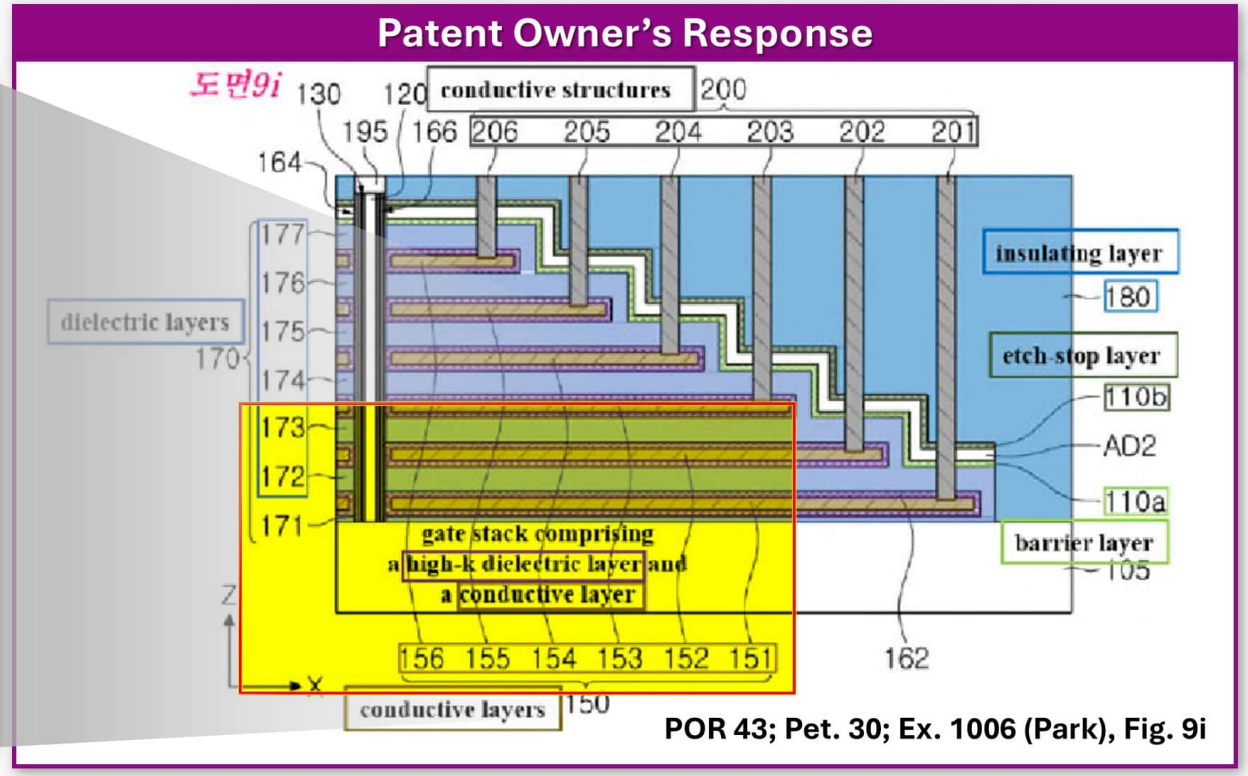
1. A semiconductor structure, comprising:
a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;
* * *

13. A semiconductor structure, comprising:
a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;
* * *

Ex. 1001 ('711 Patent), Claims 1, 13



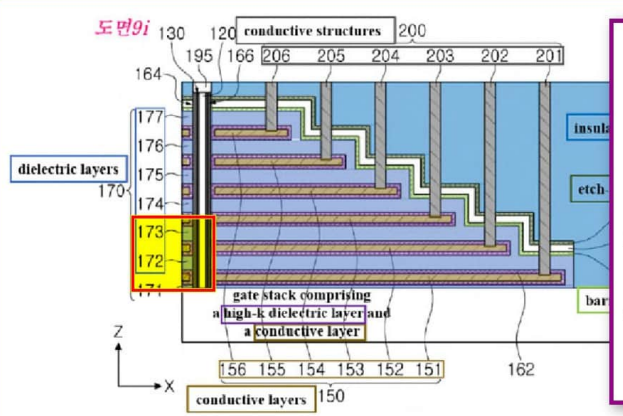
Patent Owner's Response



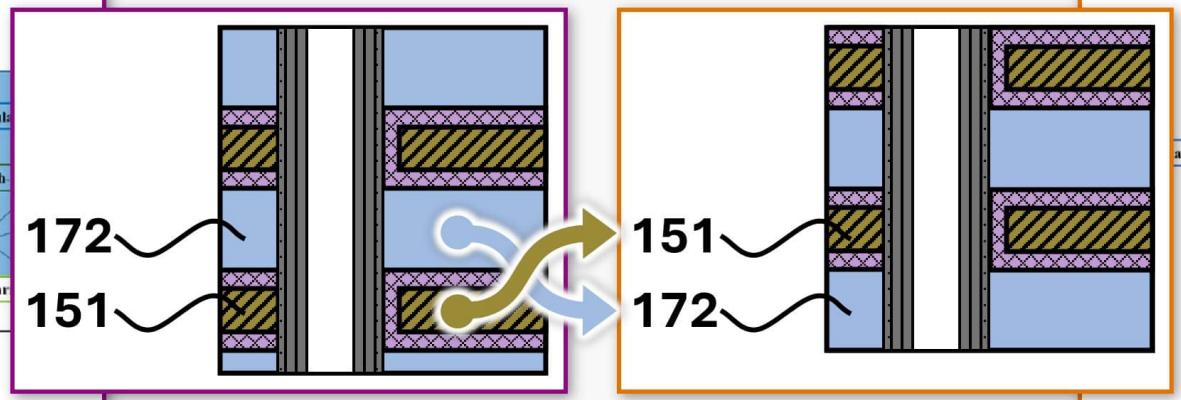
POR 43; Pet. 30; Ex. 1006 (Park), Fig. 9i

Like Kim, Petitioner Modified Park Fig. 9i

Park

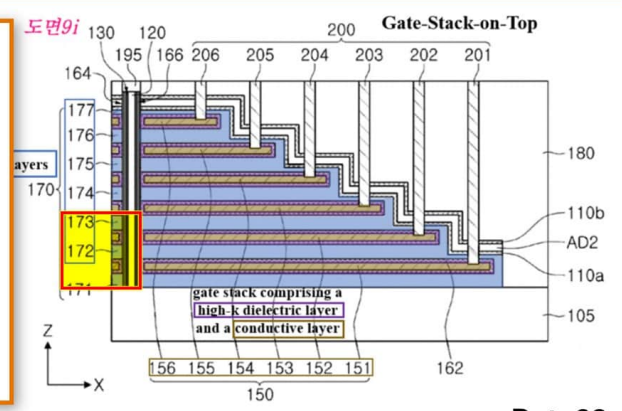


POR 43; Ex. 1006 (Park), Fig. 9i



demonstrative graphics

Petition



Pet. 69;
Ex. 1006 (Park), Fig. 9i (modified by Petitioner)

Petition

Like Kim, Park discloses embodiments in which a gate stack is disposed over a dielectric layer at each step, even though its figures show the opposite order. For

Pet. 30

Petitioner's Inadequate Motivation To Reverse Layers Of Park's Fig. 9A

Petition

A POSITA would have understood that descriptions of one of Park's embodiments apply to other embodiments except where the embodiments differ. Banerjee ¶¶ 76-77. Park discloses closely related embodiments and teaches that "various embodiments may be combined," and "elements indicated by the same symbols in the drawings are the same elements." Park, [0017]. Further, most aspects of the Figure 5 embodiment "are the same as" the Figure 4 embodiment. *Id.*, [0049]. Thus, disclosures of Figures 4 and 8a-8m apply to Figures 5 and 9a-9j except where they differ.

Pet. 31

Petitioner Identified No Benefit To Reversing Layers

Petitioner's Expert Dr. Banerjee

Q. All right. Now, in your declaration you don't list any benefits to reversing the order of the layers; right?

A. I don't think so. I mean, I cited to other prior arts such as Chen showing that it could go either way it's. A binary choice. Either the gate stack is going to be on top or below and Chen shows two figure side-by-side so it's a matter of simple choice, you can see that.

Q. It's a matter of simple choice, but there's no reason you give to go one way or the other; right?

A. No, I did not.

Ex. 2008 (Petitioner's Expert Dr. Banerjee Dep.), 35:12-36:1

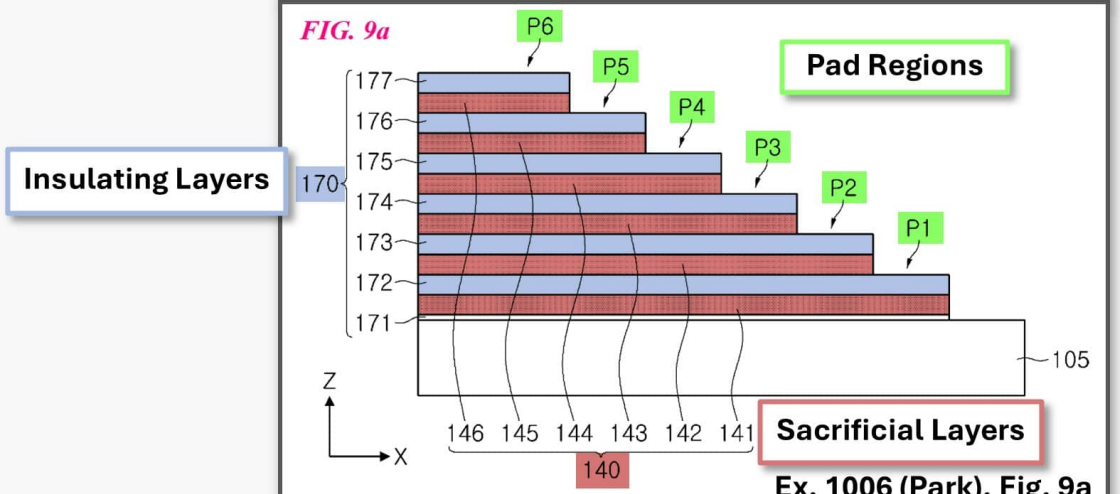
Park Describes The Etch Process, Not Reversing Layers

Park

[0102] Referring to FIG. 9a, a plurality of insulating layers (170) and sacrificial layers (140) alternately stacked on the top surface of the substrate (105) are etched to provide a plurality of pad regions (P1-P6). Each of the plurality of insulating layers (170) and sacrificial layers (140), by a plurality of pad regions (P1-P6), forms a step with respect to another insulating layers (170) and sacrificial layers (140). In addition, a portion of the top surface of each insulating layer (170) may be exposed by the plurality of pad regions (P1-P6), and, unlike what is shown in FIG. 9a, a portion of the top surface of each sacrificial layer (140) may be exposed in a plurality of pad regions (P1-P6).

Ex. 1006 (Park), [0102]

Park



Ex. 1006 (Park), Fig. 9a

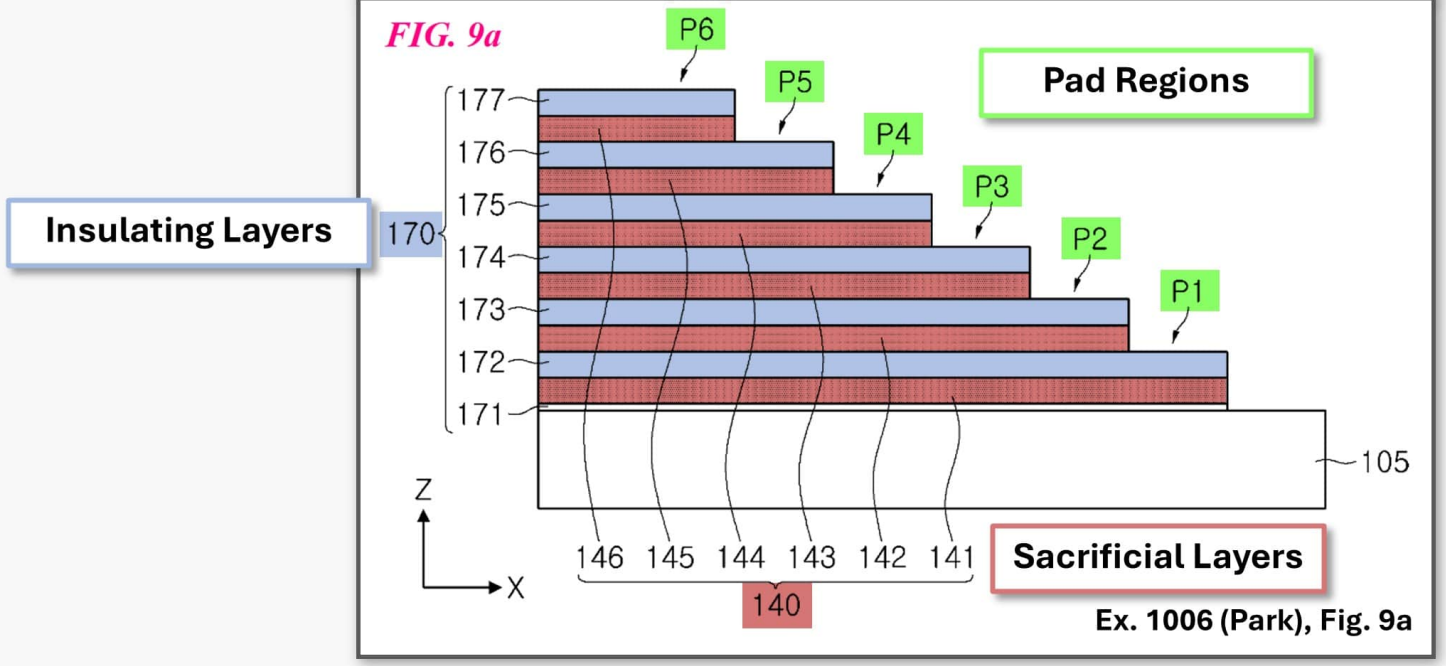
Park Describes Extending Sacrificial Layer, Not Reversing Layers

Park

respect to another insulating layers (170) and sacrificial layers (140). In addition, a portion of the top surface of each insulating layer (170) may be exposed by the plurality of pad regions (P1-P6), and, unlike what is shown in FIG. 9a, a portion of the top surface of each sacrificial layer (140) may be exposed in a plurality of pad regions (P1-P6).

Ex. 1006 (Park), [0102]

Park



Ex. 1006 (Park), Fig. 9a

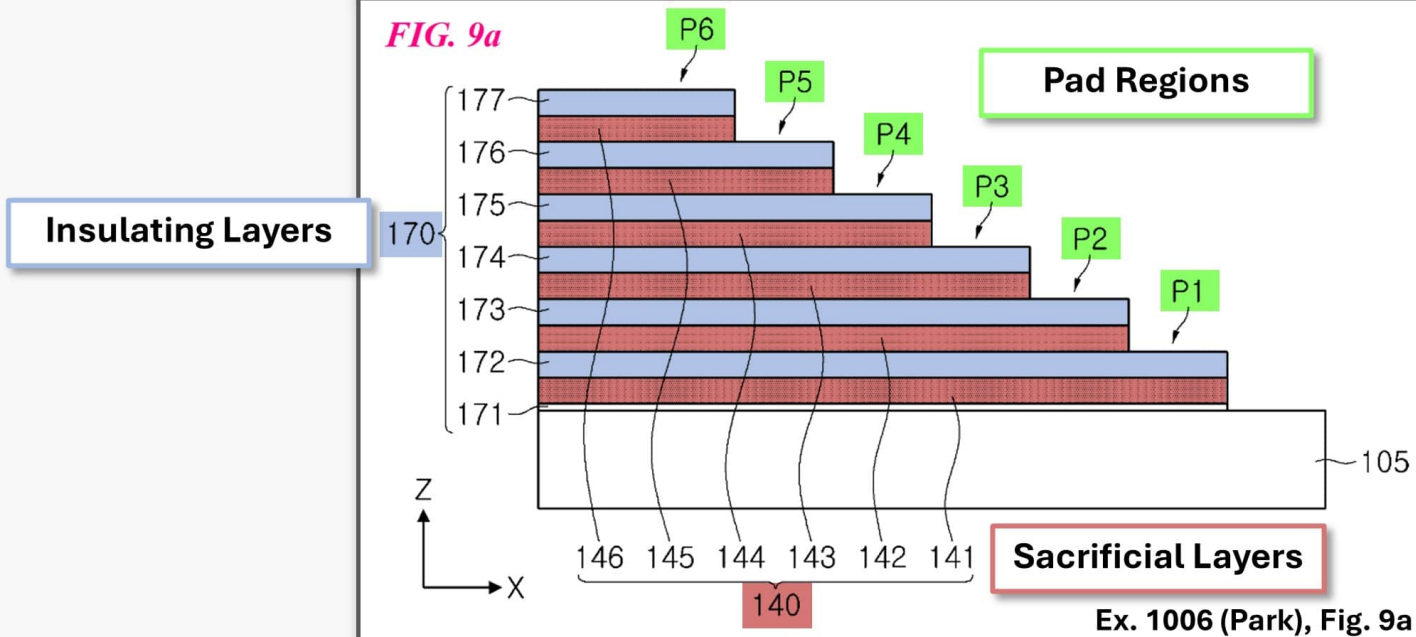
Park Describes Extending Sacrificial Layer, Not Reversing Layers

Park

respect to another insulating layers (170) and sacrificial layers (140). In addition, a portion of the top surface of each insulating layer (170) may be exposed by the plurality of pad regions (P1-P6), and, unlike what is shown in FIG. 9a, a portion of the top surface of each sacrificial layer (140) may be exposed in a plurality of pad regions (P1-P6).

Ex. 1006 (Park), [0102]

Park



Ex. 1006 (Park), Fig. 9a

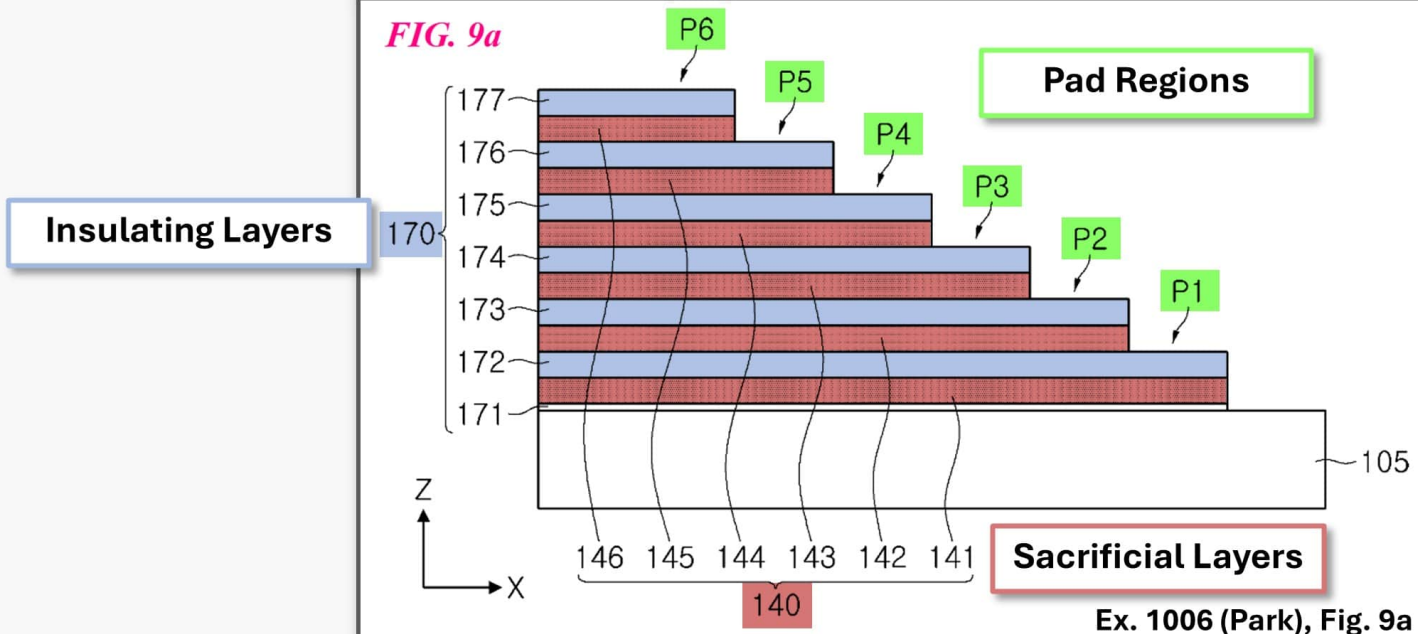
Park Describes Extending Sacrificial Layer, Not Reversing Layers

Park

respect to another insulating layers (170) and sacrificial layers (140). In addition, a portion of the top surface of each insulating layer (170) may be exposed by the plurality of pad regions (P1-P6), and, unlike what is shown in FIG. 9a, a portion of the top surface of each sacrificial layer (140) may be exposed in a plurality of pad regions (P1-P6).

Ex. 1006 (Park), [0102]

Park



Ex. 1006 (Park), Fig. 9a

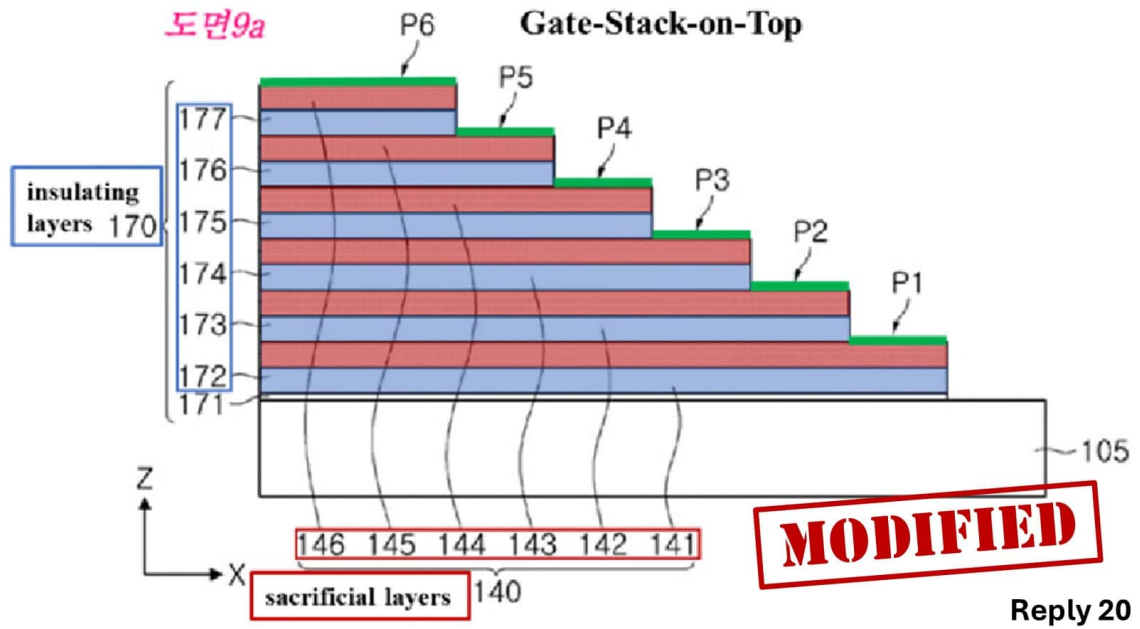
Park Describes Extending Sacrificial Layer, Not Reversing Layers

Park

respect to another insulating layers (170) and sacrificial layers (140). In addition, a portion of the top surface of each insulating layer (170) may be exposed by the plurality of pad regions (P1-P6), and, unlike what is shown in FIG. 9a, a portion of the top surface of each sacrificial layer (140) may be exposed in a plurality of pad regions (P1-P6).

Ex. 1006 (Park), [0102]

Petitioner's Reply



Reply 20

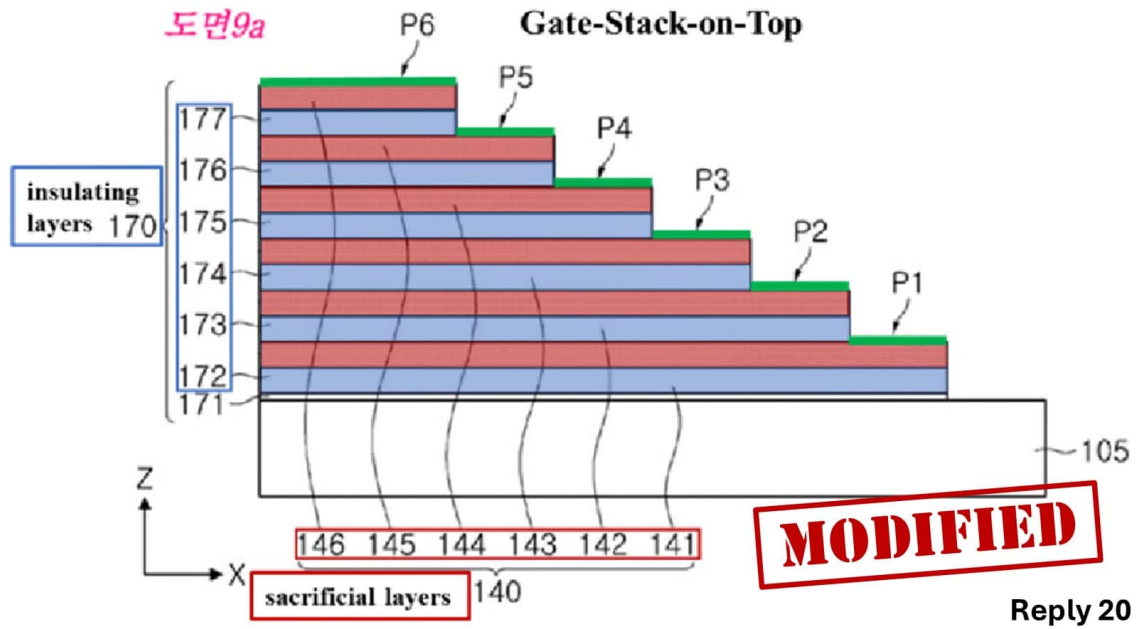
Park Describes Extending Sacrificial Layer, Not Reversing Layers

Park

respect to another insulating layers (170) and sacrificial layers (140). In addition, a portion of the top surface of each insulating layer (170) may be exposed by the plurality of pad regions (P1-P6), and, unlike what is shown in FIG. 9a, a portion of the top surface of each sacrificial layer (140) may be exposed in a plurality of pad regions (P1-P6).

Ex. 1006 (Park), [0102]

Petitioner's Reply



Reply 20

When Park Disclosed Reversing Layers Or Referenced Another Embodiment, It Did So Expressly

Park

pad regions. In FIG. 4, the insulating layer (170) is depicted as being positioned above the gate electrode layer (150) along the z-axis direction in each pad region, but conversely, the gate electrode layer (150) may be positioned above the insulating layer (170).

Ex. 1006 (Park), [0042]

Park

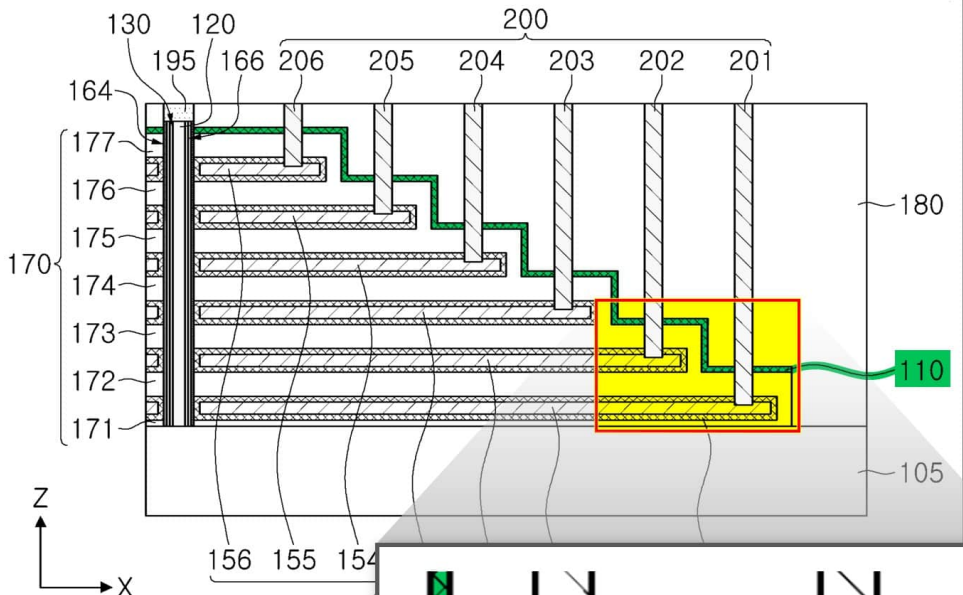
Referring to FIG. 9e next, a channel region (130) may be formed. The method of forming a channel region (130) may be the same as described with reference to FIG. 8h above. Once the channel region (130) is formed, the etch-stop sacrificial layer (115a, 115b) and the plurality of sacrificial layers (140) can be removed to provide side openings (T1, T2), as shown in FIG. 9f. The first side opening (T1) corresponds to the space in which the

Ex. 1006 (Park), [0104]

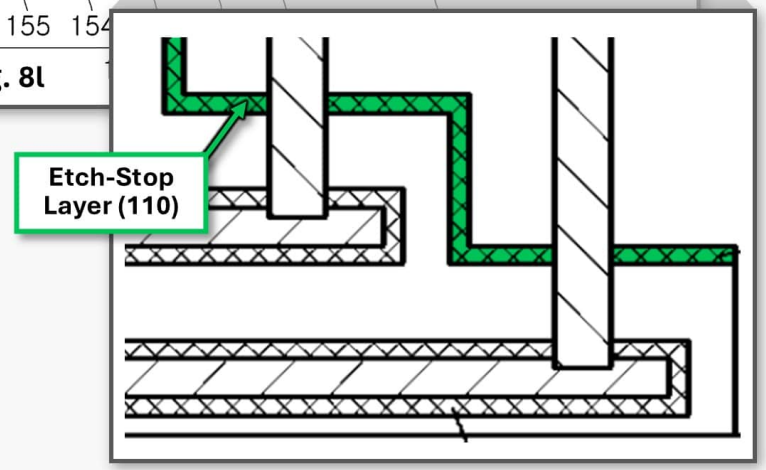
Park's Figs. 4/8 And Figs. 5/9 Are Materially Different Designs

Park

FIG. 8l

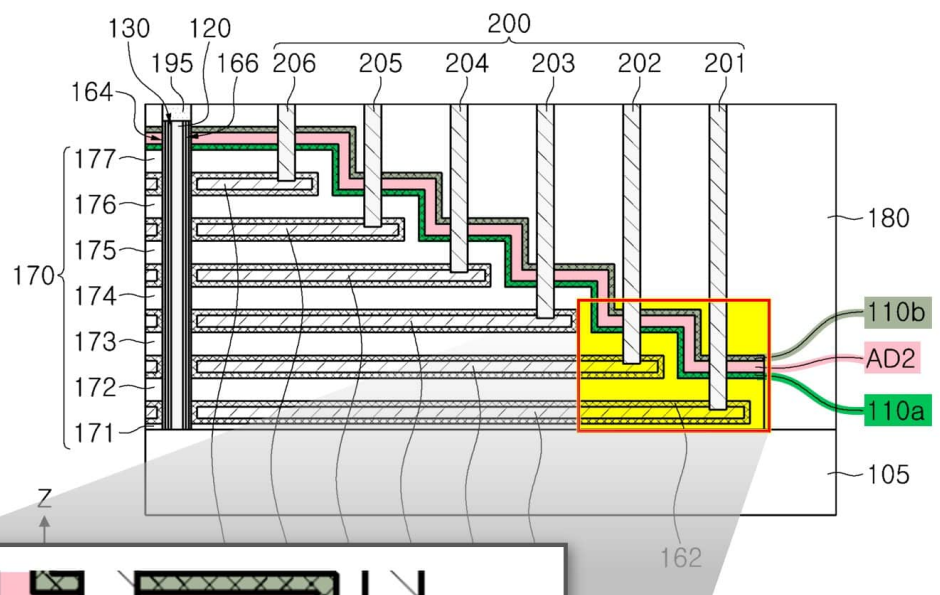


Ex. 1006 (Park), Fig. 8l

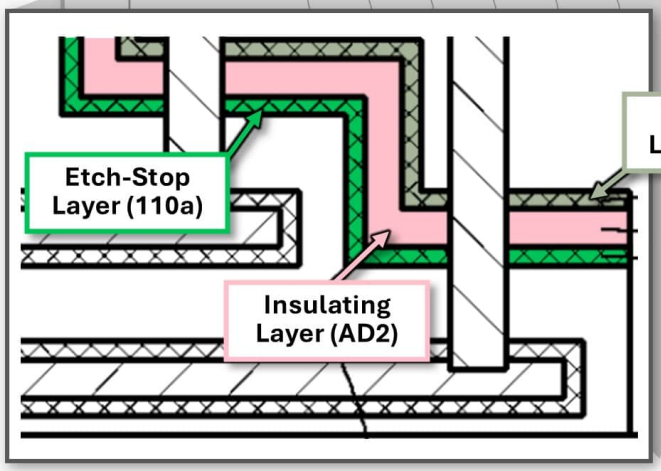


Park

FIG. 9i



Ex. 1006 (Park), Fig. 9i



DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 3: Claims 14 And 15 Are Not Obvious

14. The semiconductor structure of claim **13**, wherein the etch-stop layer is formed on a side surface and a top surface of each step.

Ex. 1001 ('711 Patent), Claim 14

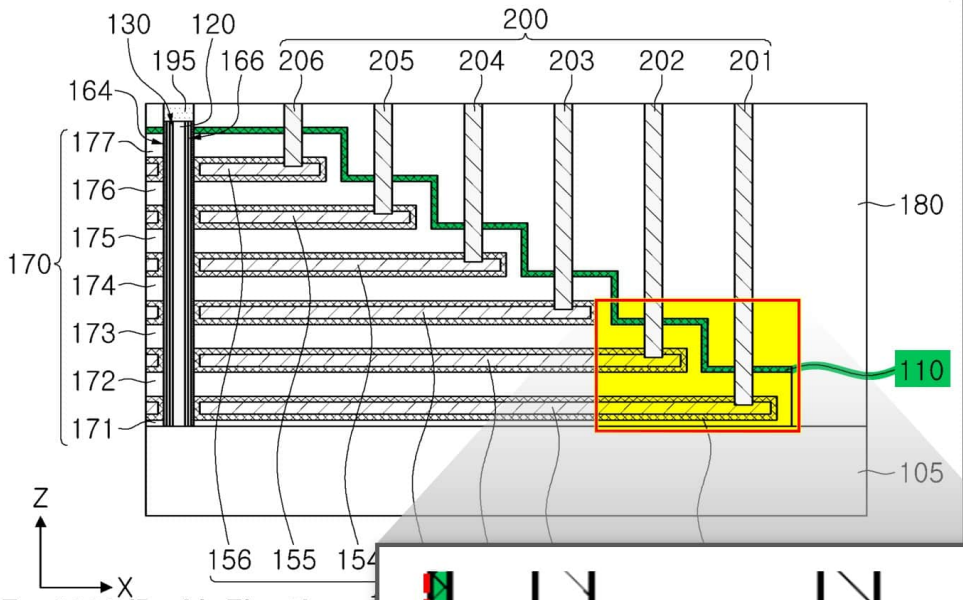
15. The semiconductor structure of claim **14**, wherein thicknesses of the etch-stop layer is the same on the side and top surfaces of each step.

Ex. 1001 ('711 Patent), Claim 15

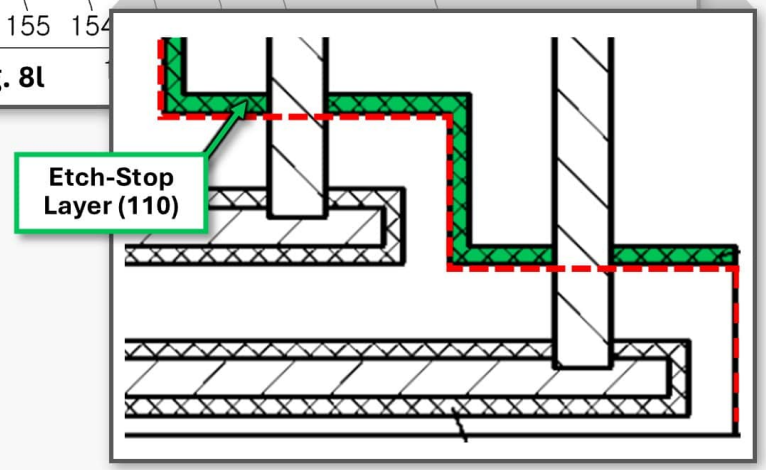
Park's Etch-Stop Layer Is Not "formed on a side surface and a top surface of each step"

Park

FIG. 8l

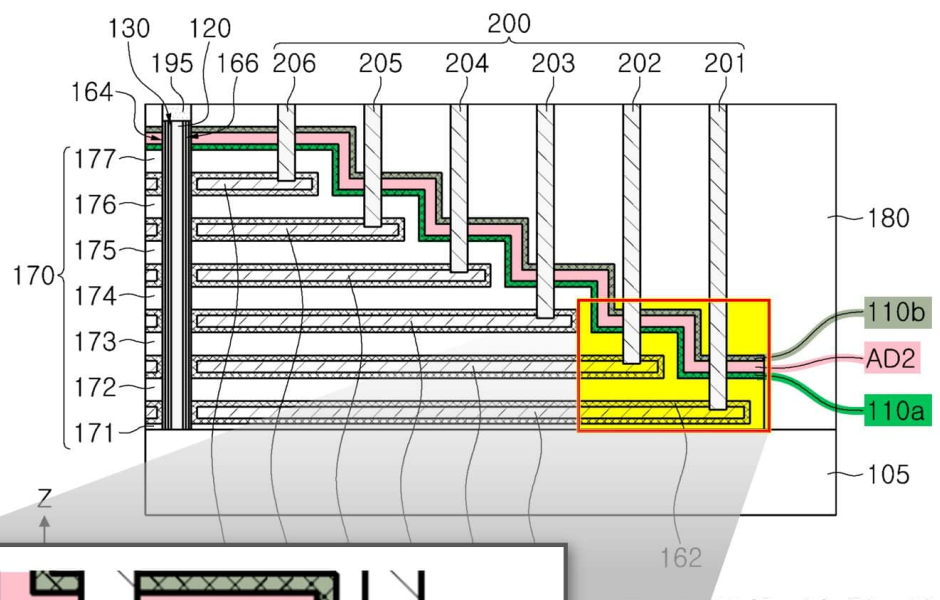


Ex. 1006 (Park), Fig. 8l

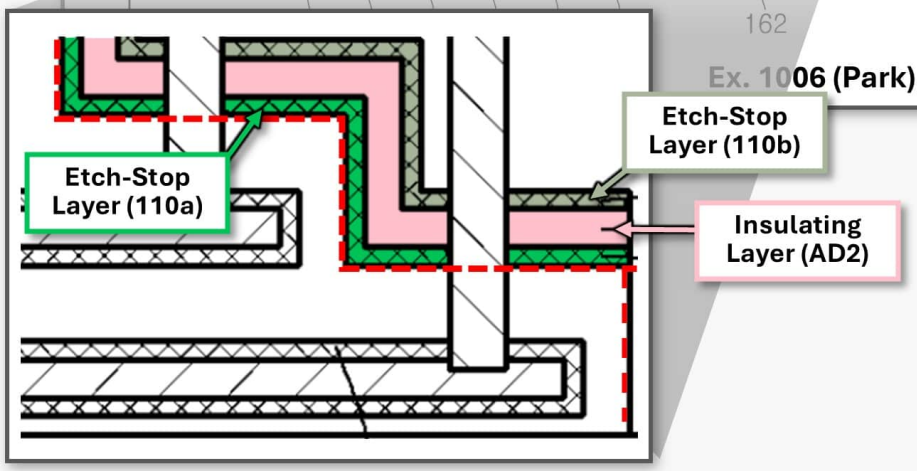


Park

FIG. 9i

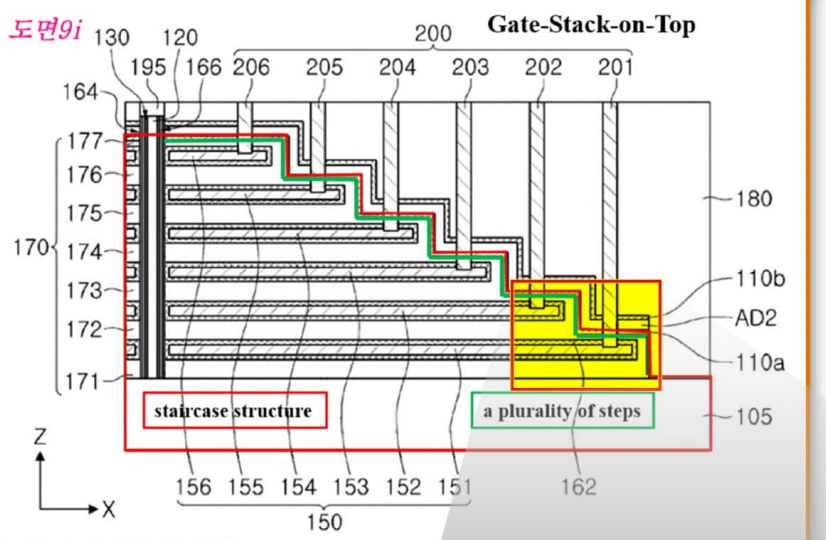


Ex. 1006 (Park), Fig. 9i

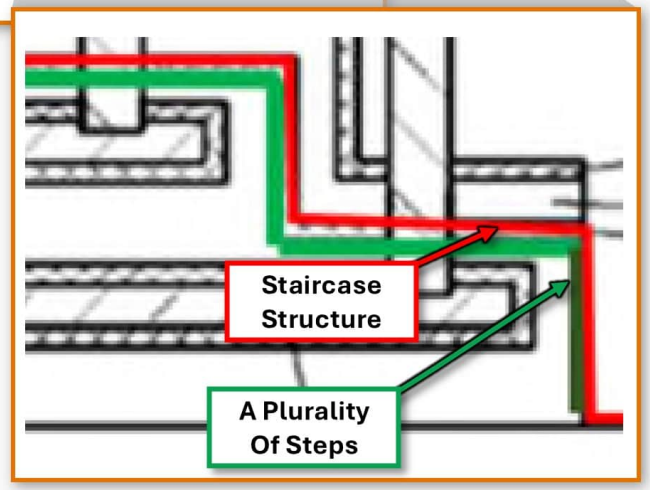


Park's Etch-Stop Layer Is Not "formed on a side surface ... of each step"

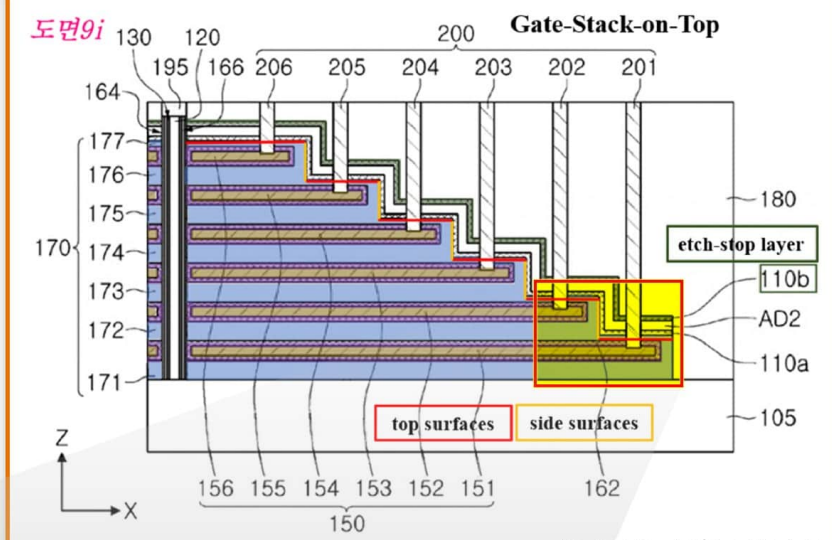
Petition



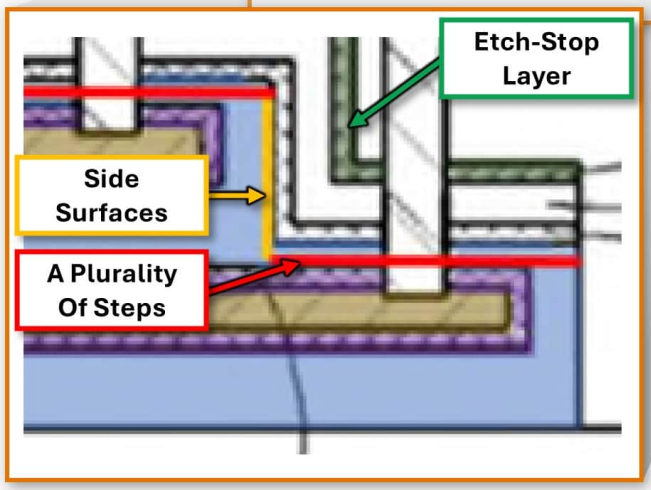
Pet. 68; POSR 21



Petition

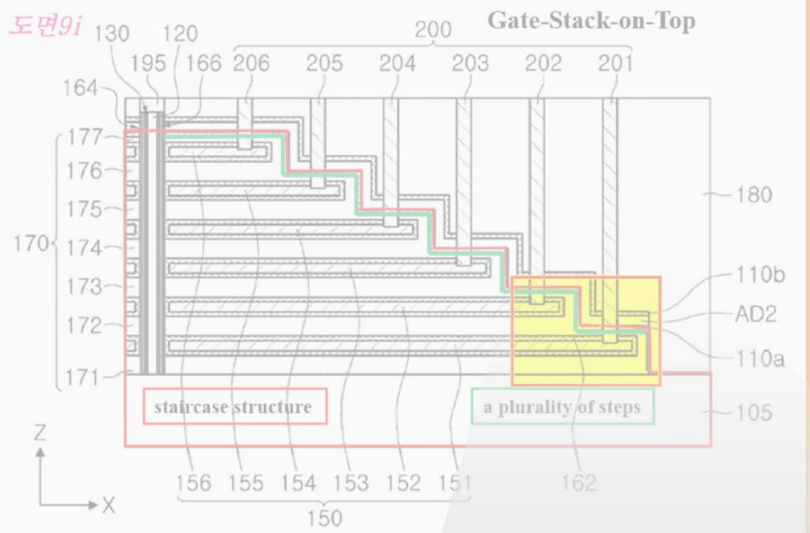


Pet. 89; POR 48-50

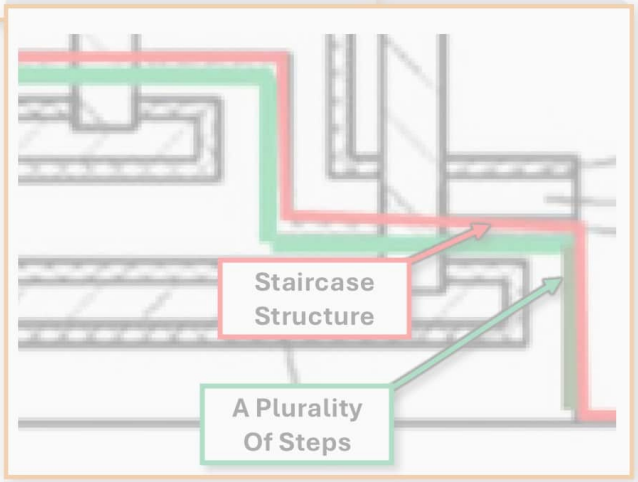


Park's Etch-Stop Layer Is Not "formed on a side surface ... of each step"

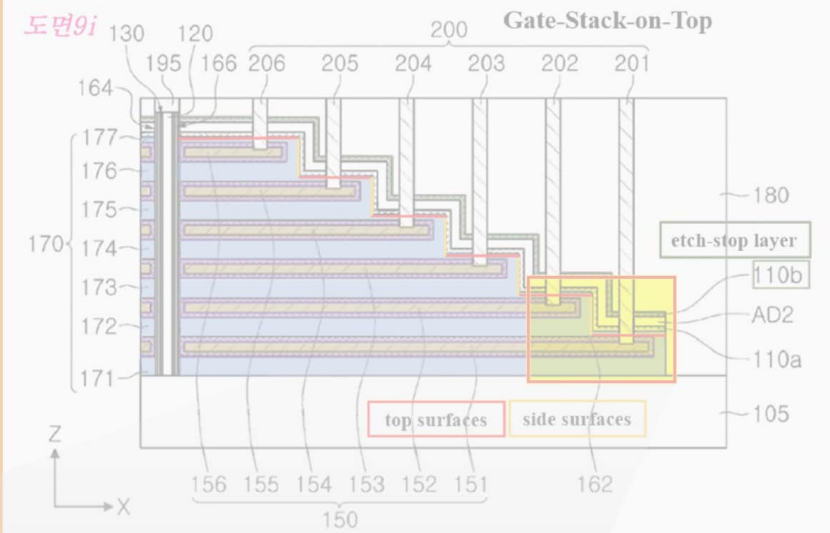
Petition



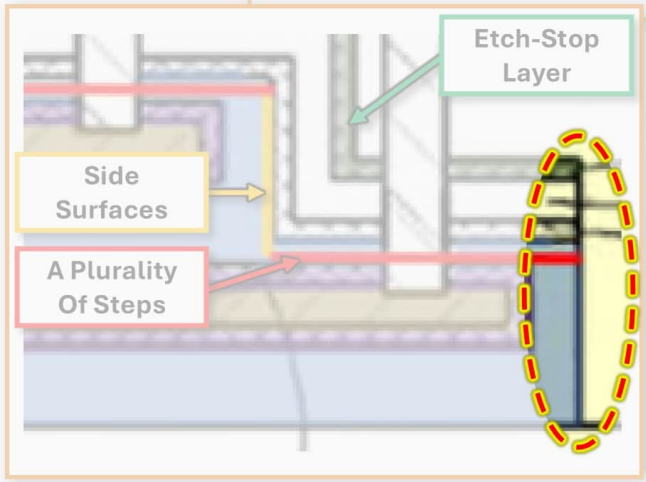
Pet. 68; POSR 21



Petition



Pet. 89; POR 48-50

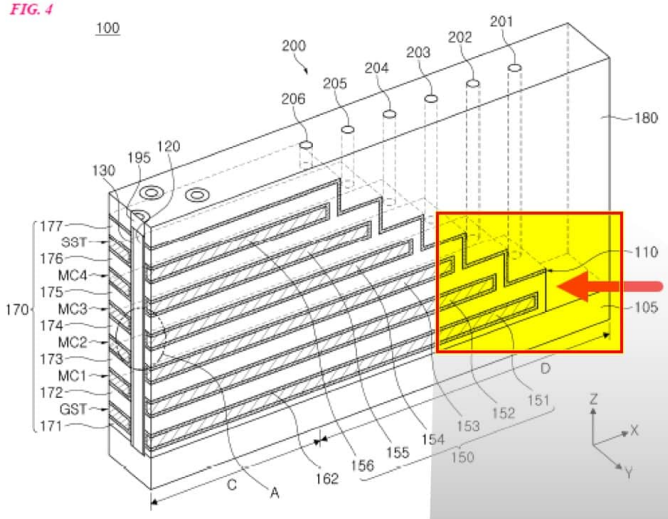


No Etch-stop Layer

None Of Park's Embodiments Show Etch-Stop Layer "formed on a side surface ... of each step"

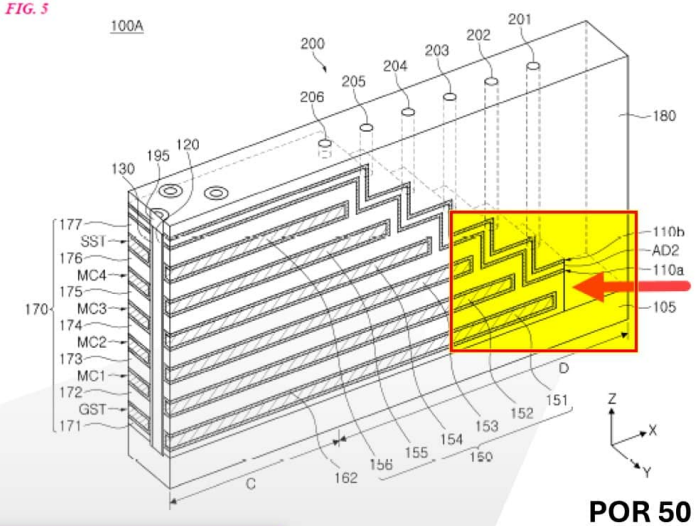
POR

FIG. 4

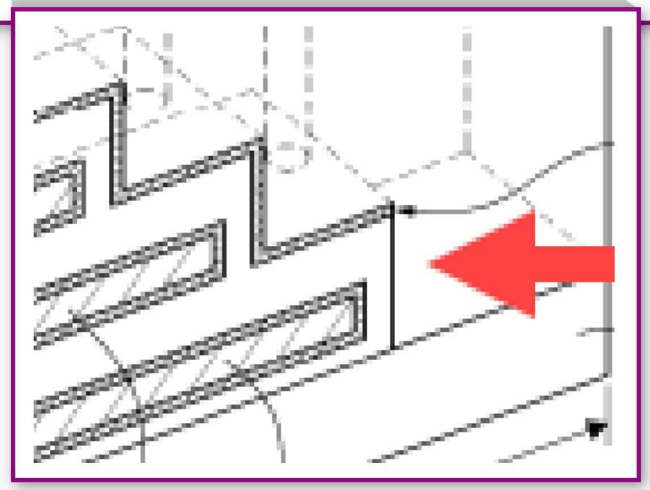


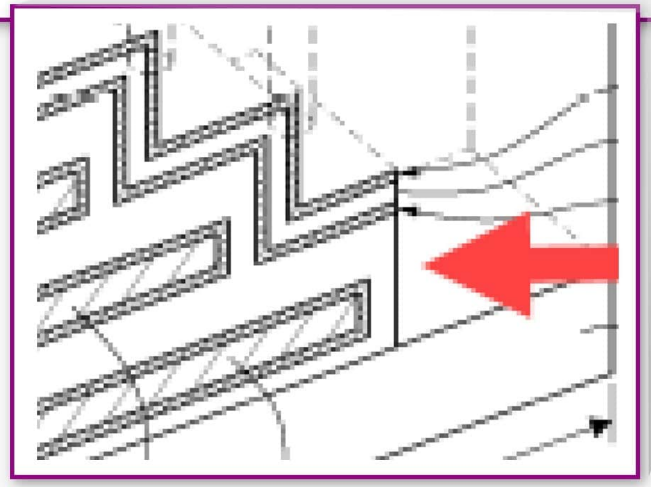
Steps without etch-stop layer on the side

FIG. 5



POR 50

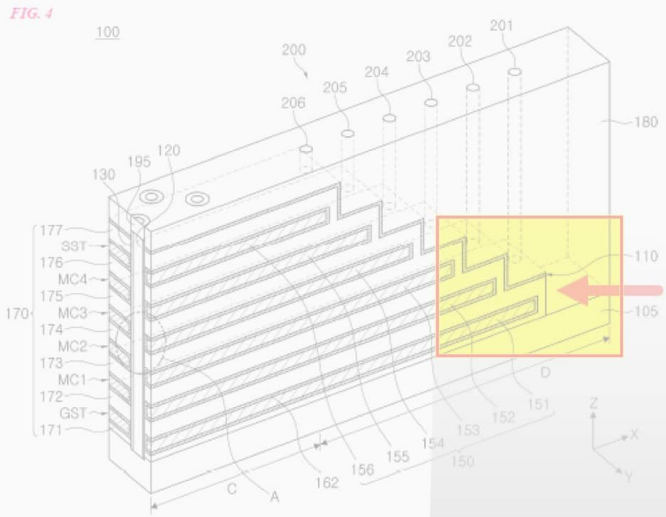


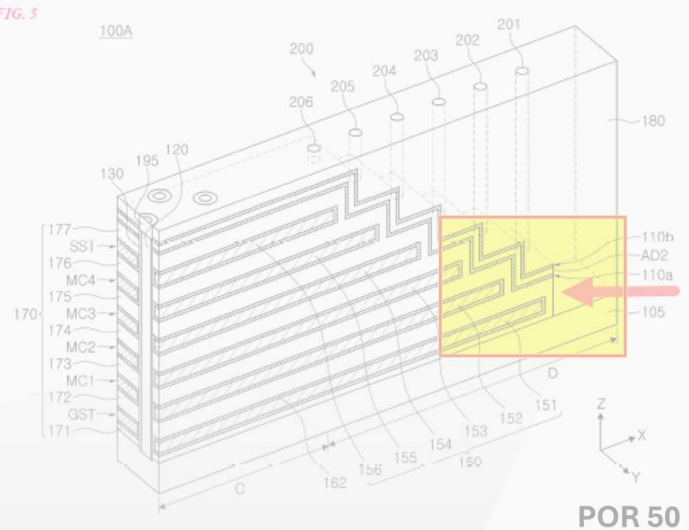


None Of Park's Embodiments Show Etch-Stop Layer "formed on a side surface ... of each step"

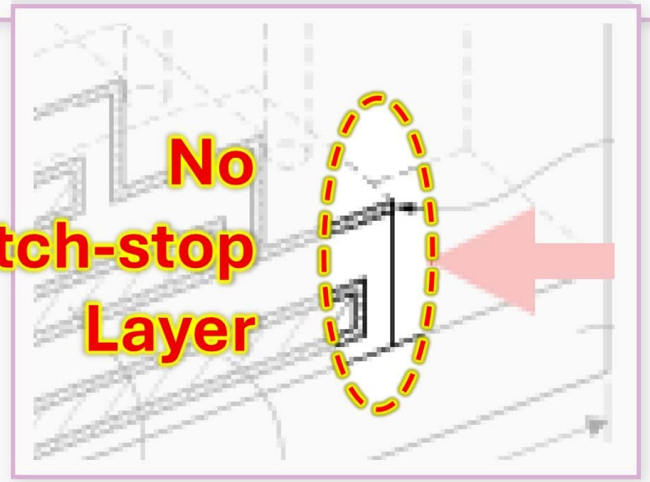
POR

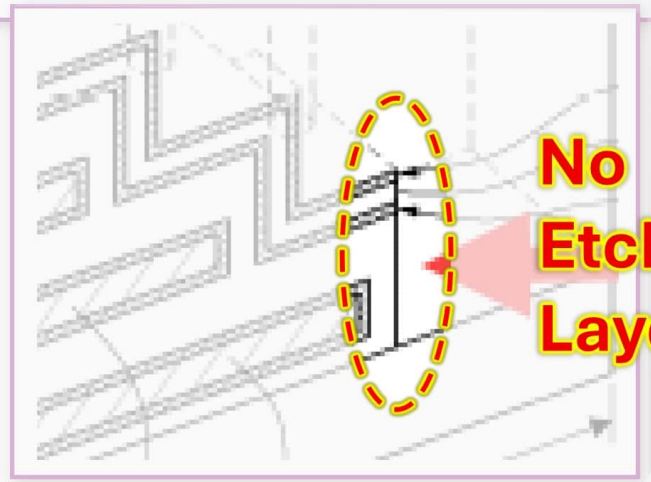
Steps without etch-stop layer on the side





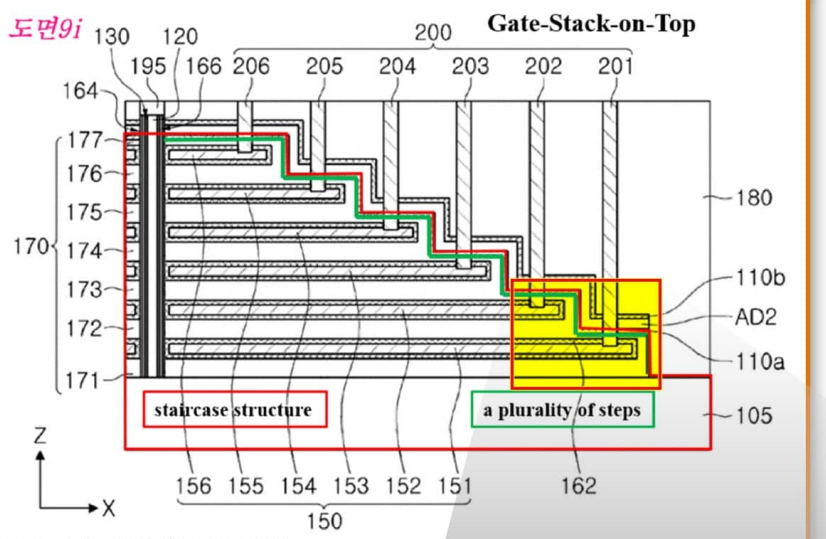
POR 50





Petitioner's "subset" Of "each step" Argument Is Unsupported And Contradicts Petition

Petition

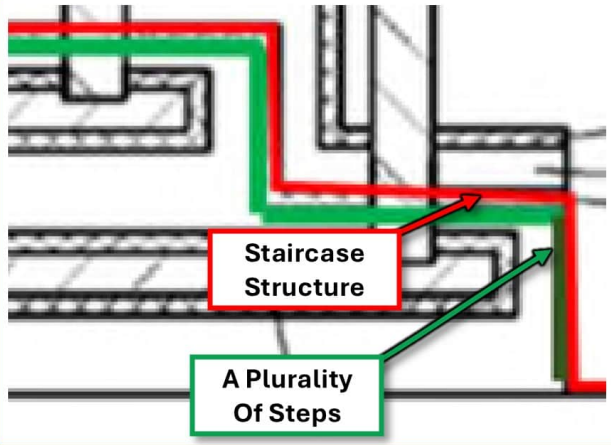


Pet. 68; POSR 20-23

Petitioner's Reply

PO's first argument is based on Park's figure showing that the etch-stop layer does not cover the side of the bottom step. But the claimed "each" step is not the same as "all" steps of the staircase structure. First, ***each*** "can also mean 'each of a subset.'" Ex.1001, 5:6–8.[8] Second, "a staircase structure comprising a plurality of steps" need not include all steps of the staircase because "comprising" is open-ended. *Genentech, Inc. v. Chiron Corp.*, 112 F.3d 495, 501 (Fed. Cir. 1997).

Reply 22



Petitioner's Waived "optional" Barrier Layer Argument Fails

Petitioner's Expert Dr. Banerjee

Q. All right. You've labeled layer 110B as the etch-stop layer; is that right?

A. Yes.

Q. All right. So the etch-stop layer is formed on layer AD2; right?

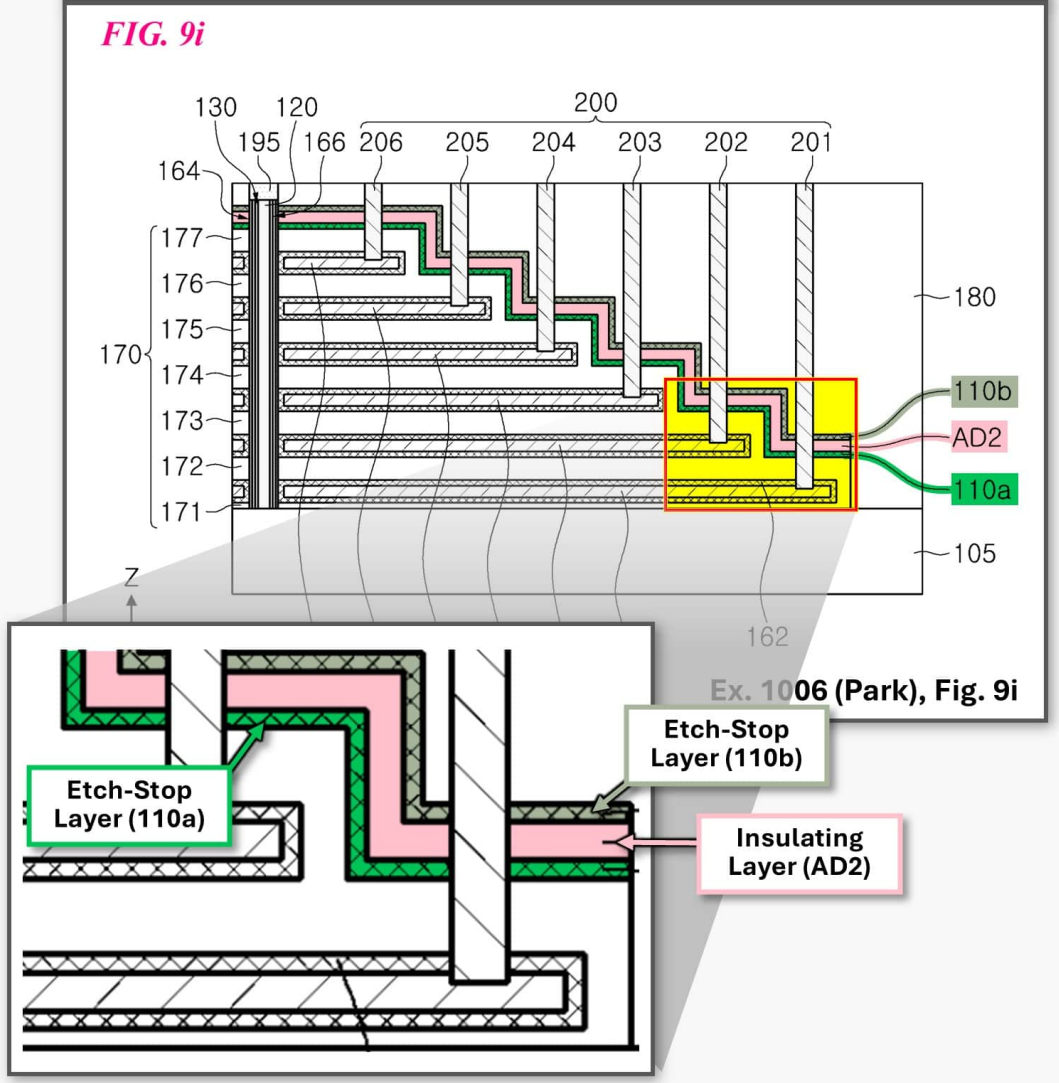
A. In this figure, yes, but if you look at the specifications, Park says that AD2 is this additional dielectric, which is optional.

Q. So it would either be formed on AD2 or on the surface of the barrier layer?

A. That's correct.

Ex. 2008 (Petitioner's Expert Dr. Banerjee Dep.), 65:22-66:10

Park



Ex. 1006 (Park), Fig. 9i

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Claim 15: Petitioner Gap-fills Same Thickness On Side And Top Surfaces Of Park's Etch-Stop Layer

15. The semiconductor structure of claim 14, wherein thicknesses of the etch-stop layer is the same on the side and top surfaces of each step.

Ex. 1001 ('711 Patent), Claim 15

Park

The thickness of the etch-stop layer may be less than or equal to two times the thickness of the gate insulating film.

* * *

invention to a person having average knowledge in the relevant technical field. Therefore, the shapes and sizes of elements in the drawings may be exaggerated for clearer explanation, and elements indicated by the same symbols in the drawings are the same elements.

Ex. 1006 (Park), [0006], [0017]

Park Does Not Disclose Uniform Etch-Stop Thickness "on the side and top surfaces of each step"

Park

[0058] FIG. 7a is an enlarged view of part A in a nonvolatile memory device according to the embodiment shown in FIG. 4.

Ex. 1006 (Park), [0058]

[0060] The gate electrode layer (154) is surrounded by a blocking layer (162), and consequently between the channel region (130) and the gate electrode layer (154) is sequentially disposed, from the channel region (130), the tunneling layer (166), the charge storage layer (164), and the blocking layer (162). The thickness of the blocking layer (162), the charge storage layer (164), and the tunneling layer (166) included in the gate insulating film (160) is not limited to that shown in FIG. 7a and may vary. On the other hand, in this example, the thickness of the etch-stop layer (110) may be no more than twice the thickness of the blocking layer (162) to prevent the material included in the gate electrode layer (154) from flowing into the etch-stop layer (110).

Ex. 1006 (Park), [0060]

[0067] On the other hand, an etch-stop layer (110) may be provided within each insulating layer (173, 174). The etch-stop layer (110) may comprise the same material as the blocking layer (162) surrounding the gate electrode layer (154), and may comprise, for example, aluminum oxide (Al_2O_3). FIG. 7B illustrates that one etch-stop layer (110) is included in each insulating layer (173, 174), but two or more etch-stop layers (110) may be included in each insulating layer (173, 174). In order to prevent the conductive material included in the gate electrode layer (154) from being included in the etch-stop layer (110), the thickness of the etch-stop layer (110) may be less than twice the thickness of the blocking layer (162).

Ex. 1006 (Park), [0067]

Claim 15: A POSITA Would Not Have Been Motivated To Have Uniform Thickness On Top *AND* Side

Dr. Campbell Second Declaration

more information. Further, a POSITA would be most concerned with the horizontal etch-stop layers on the top of each step being adequate and of uniform thickness to avoid punch through while forming vias for the conductive structures of each step. A POSITA would also find it desirable to have etch-stop layers on the side of a step be thick enough to prevent punch through by the etching used to form vias on the adjacent step, in the event the mask alignment is not adequately aligned. A POSITA would not be as concerned that etch-stop layers on the top and side of each step are of equal thickness relative to each other, especially because they may not share the same etch rate where the horizontal etch-stop layer receives direct bombardment of ions and the vertical layer does not. Further, uniformity between

Ex. 2009 (Patent Owner's Expert Dr. Campbell Sec. Decl.) ¶ 71

Agenda

- '711 Patent
- **Petitioner's Flawed Obviousness Theories**
  - Ground 1 (Kim) Fails
  - Ground 2 (Kim + Fang) Fails
  - Ground 3 (Park) Fails
  - **Ground 4 (Park + Fang) Fails**

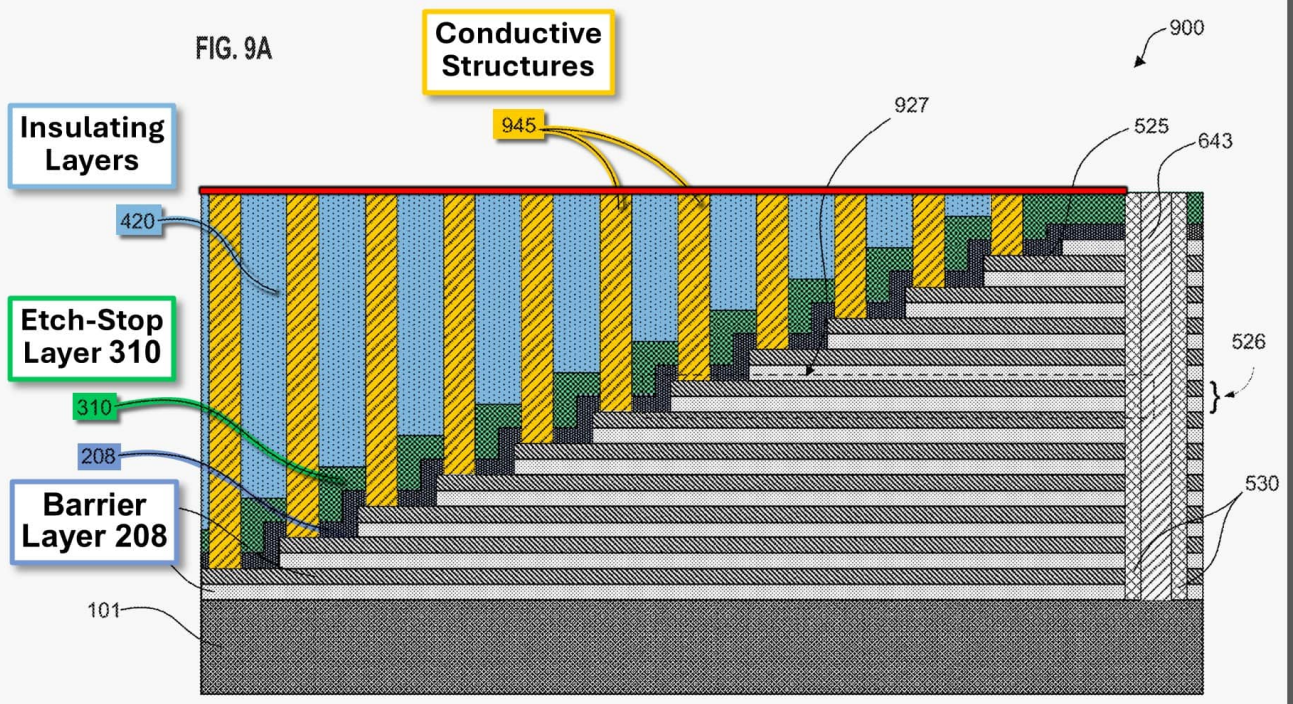
Claim 7 Would Not Have Been Obvious Over Park And Fang

1. A semiconductor structure, comprising:
a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;
a barrier layer disposed over a portion of the gate stack of the each step;
an etch-stop layer disposed on the barrier layer;
an insulating layer disposed on the etch-stop layer; and
a plurality of conductive structures formed in the insulating layer, wherein each conductive structure is formed on the conductive layer of the each step.

Ex. 1001 ('711 Patent), Claim 1

7. The semiconductor structure of claim 1, wherein top surfaces of the plurality of conductive structures, the insulating layer, and a portion of the etch-stop layer are coplanar.

Ex. 1001 ('711 Patent), Claim 7



Ex. 1001 ('711 Patent), Fig. 9A

Petitioner Modifies Park's Planarization Process According To Fang

Petition

In view of Fang, a POSITA would have found it obvious to modify Park's planarization process such that *top surfaces of the plurality of conductive structures* ("contact plugs" 201-206), *the insulating layer* ("connection region insulating layer" 180), *and a portion of the etch-stop layer* ("etch-stop layer" 110b) *are coplanar*.

Pet. 94

Fang's coplanar disclosure to Park's device. The modification simply extends Park's existing planarization process to remove a greater thickness of the same, unnecessary, materials in view of Fang. Banerjee ¶ 203. Additionally, this

Pet. 103

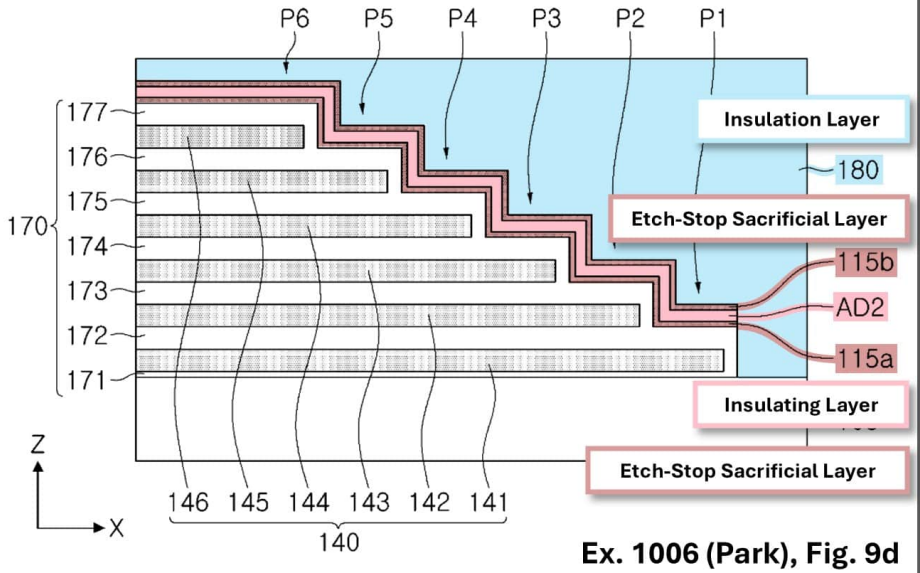
Park's Manufacturing Process – Sacrificial Layers 115a, 115b

Park

region (P1-P6) and an etch-stop sacrificial layer (115a, 115b) can be provided as shown in FIGS. 9b and 9c. At this time, an insulating layer (AD2) may be further arranged between the first etch-stop sacrificial layer (115a) and the second etch-stop sacrificial layer (115b) to physically separate the first etch-stop sacrificial layer (115a) and the second etch-stop sacrificial layer (115b). Once an etch-stop sacrificial layer (115a, 115b) is in place, a connection region insulation layer (180) can be applied onto the second etch-stop sacrificial layer (115b) and a planarization process can be performed, forming a structure as shown in FIG. 9d.

Ex. 1006 (Park), [0103]

FIG. 9d



Ex. 1006 (Park), Fig. 9d

Park's Manufacturing Process – Conductive Layer 195 And Openings T2

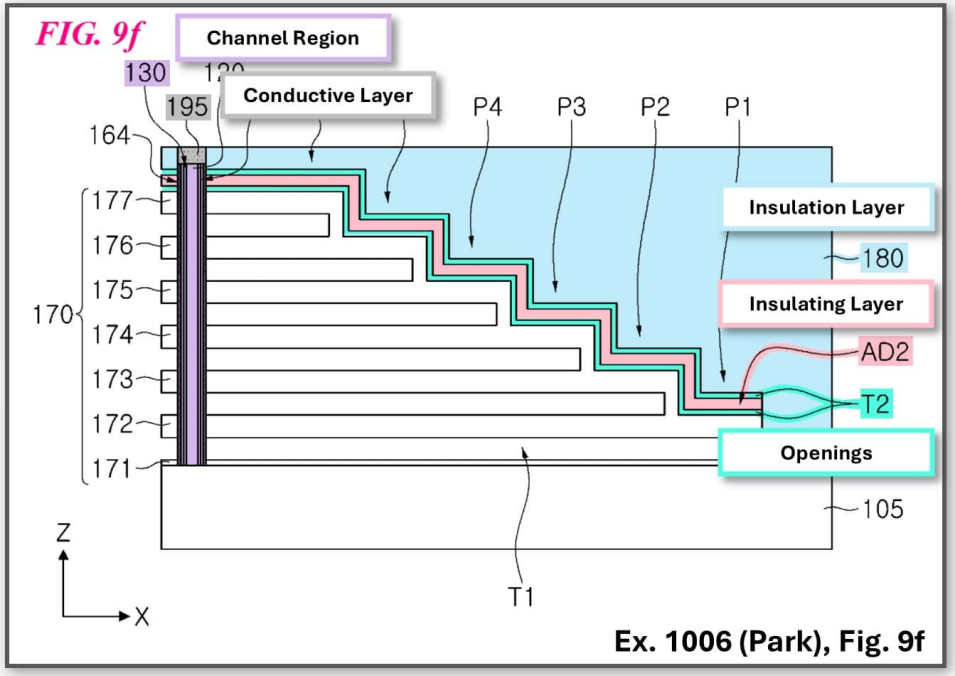
Park

Referring to FIG. 9e next, a channel region (130) may be formed. The method of forming a channel region (130) may be the same as described with reference to FIG. 8h above. Once the channel region (130) is formed, the etch-stop sacrificial layer (115a, 115b) and the plurality of sacrificial layers (140) can be removed to provide side openings (T1, T2), as shown in FIG. 9f. The first side opening (T1) corresponds to the space in which the plurality of sacrificial layers (140) was provided, and the second side opening (T2) can correspond to the space in which the etch-stop sacrificial layers (115a, 115b) were provided.

Ex. 1006 (Park), [0104]

Next, a planarization process can be performed to remove unnecessary semiconductor material and insulating material covering the top connection region insulating layer (180). The top of the buried insulating layer (120) can then be partially removed using an etching process or the like, and a material that constitutes a conductive layer (195) can be deposited at the removed location. Again, a planarization process may be performed, such that a conductive layer (195) may be formed.

Ex. 1006 (Park), [0089]



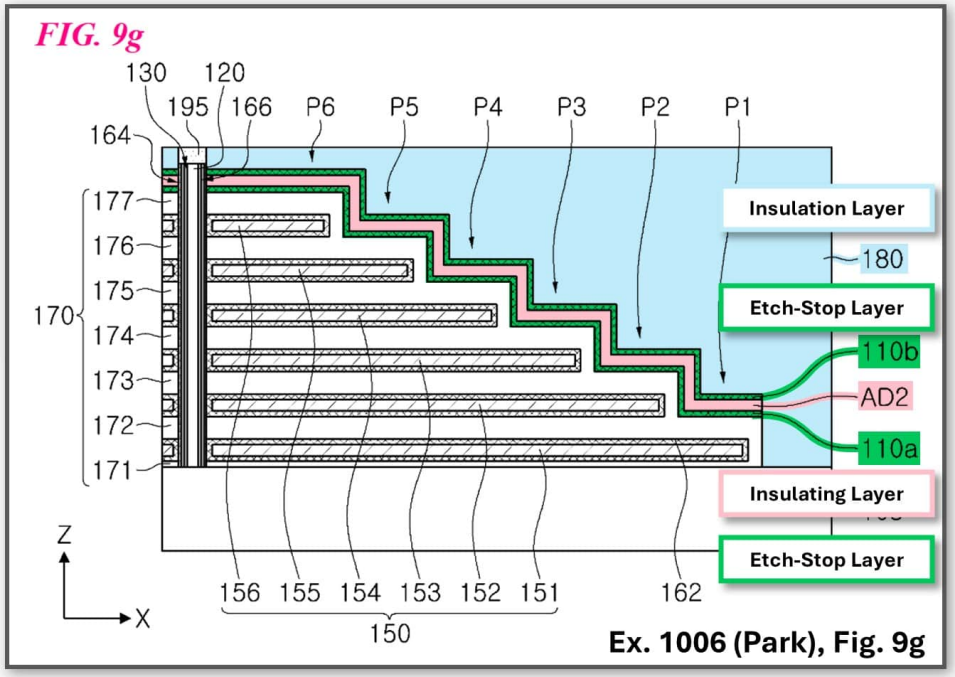
Ex. 1006 (Park), Fig. 9f

Park's Manufacturing Process – Etch-Stop Layers 110a, 110b

Park

The side openings (T1, T2) may be introduced with certain materials, such as shown in Figure 9g. At this time, the first side opening (T1) may be first deposited with a blocking layer (162) to form a gate insulating film (160) with the charge storage layer (164) and tunneling layer (166) provided outside of the channel region (130), and a gate electrode layer (150) may be formed with an electrically conductive material such as tungsten (W) within the block layer (162). The second side opening (T2) may be deposited with the same material as the blocking layer (162) such that an etch-stop layer (110a, 110b) is formed.

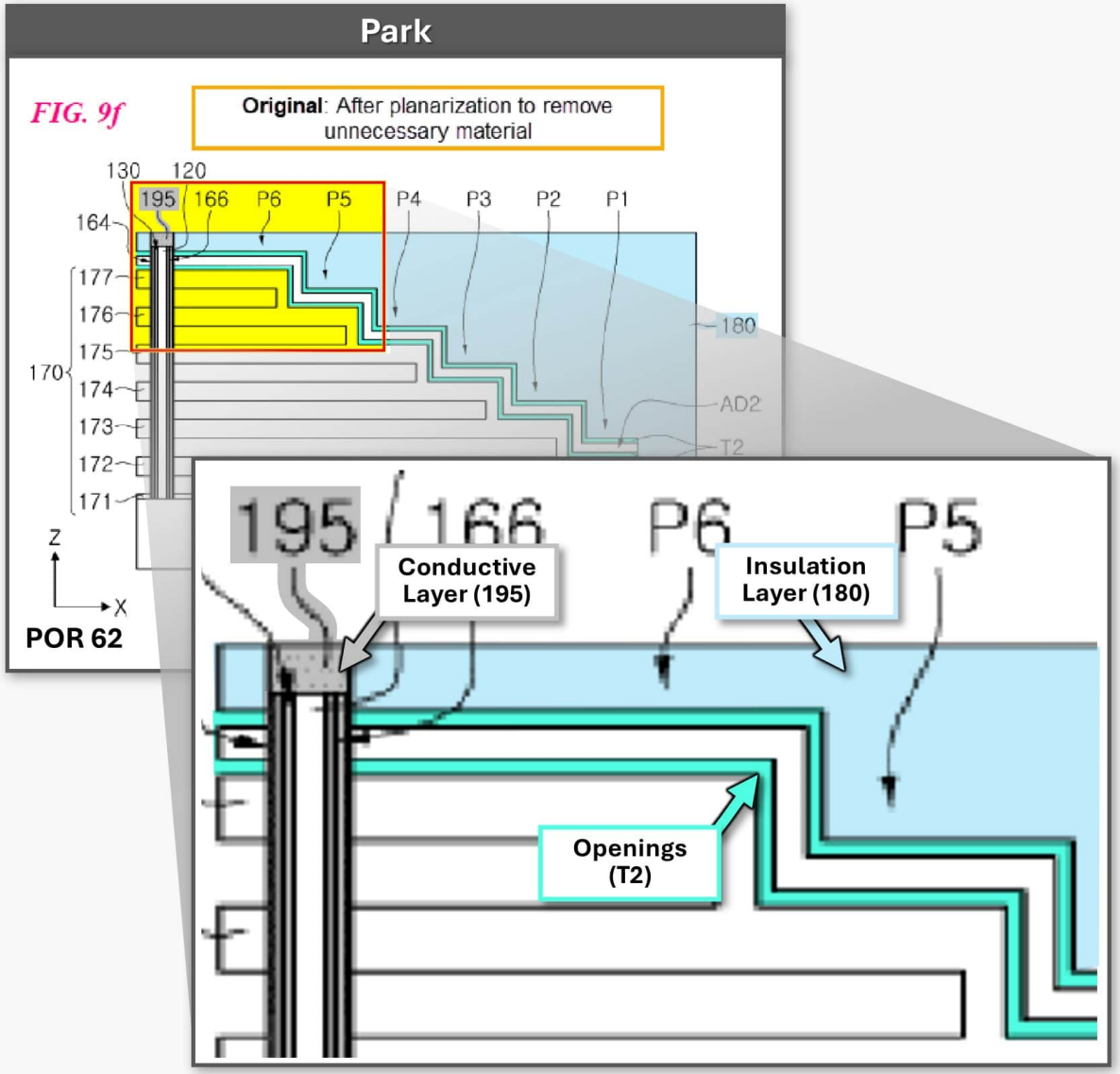
Ex. 1006 (Park), [0105]



Ex. 1006 (Park), Fig. 9g

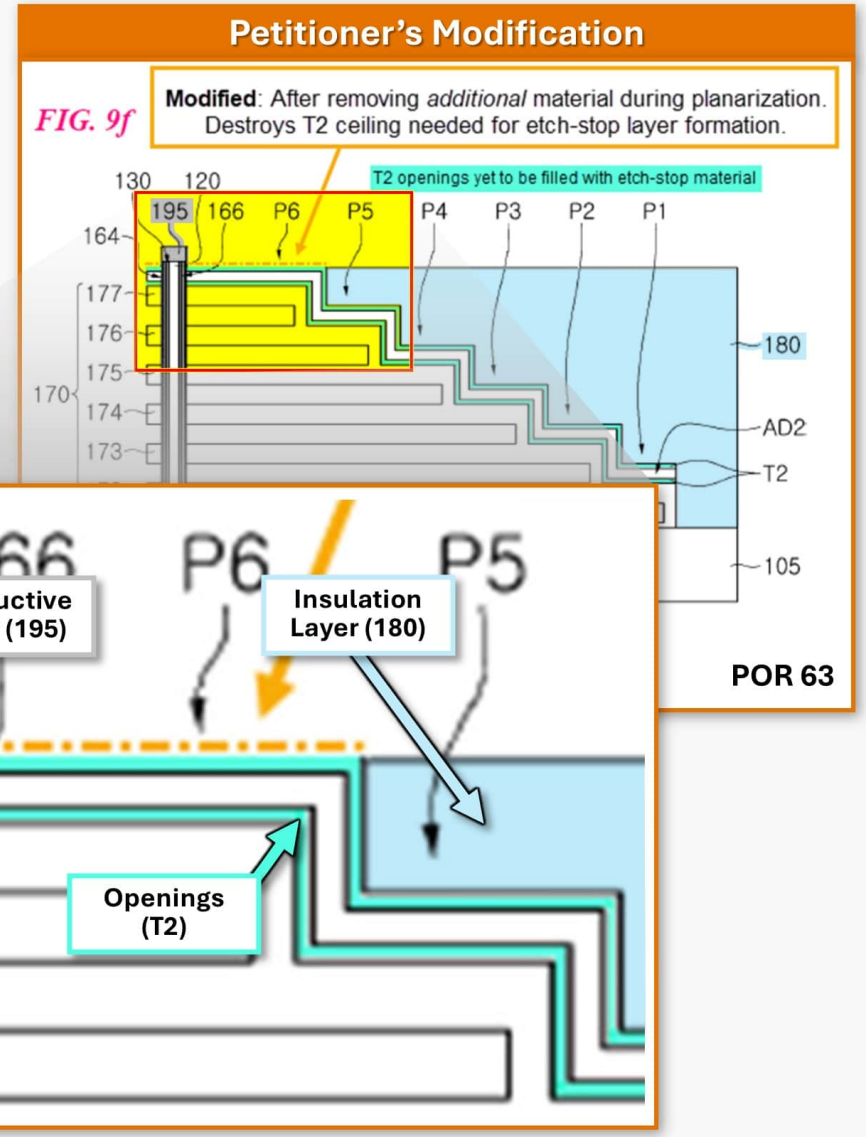
Petitioner's Modification Destroys Park's Manufacturing Process

Park



POR 62

Petitioner's Modification

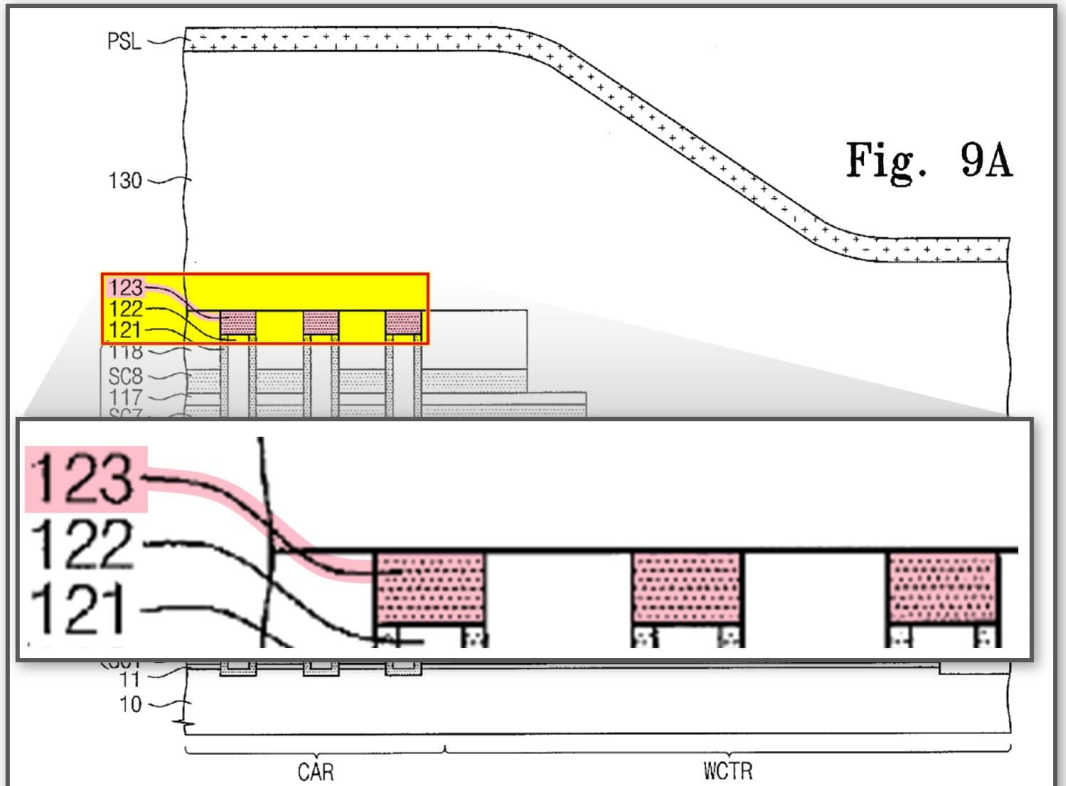


POR 63

Petitioner's Modification Destroys Park's Manufacturing Process

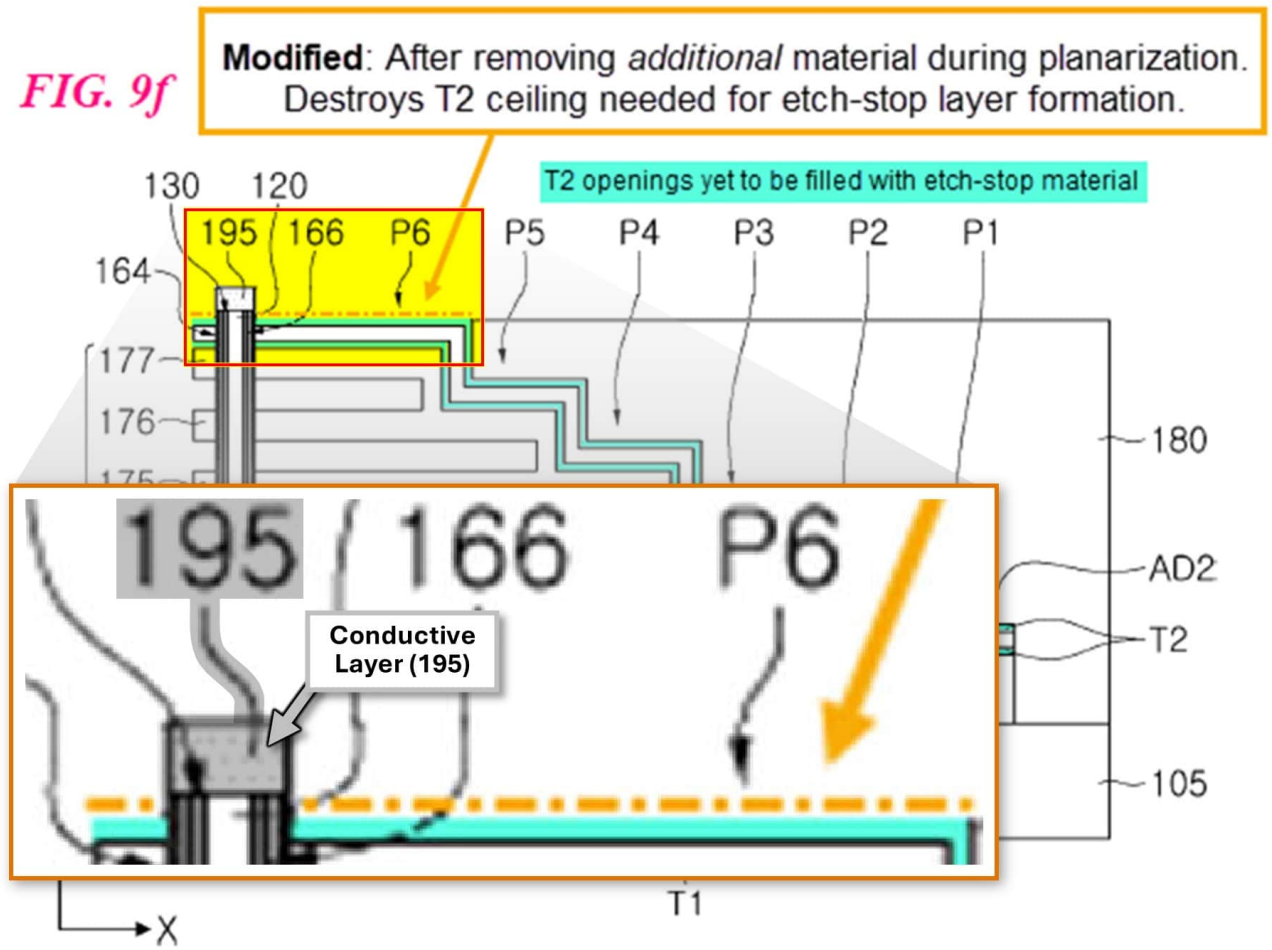
Kim

region C/P. In addition, some of the contact pads **123** may be damaged by chemical and/or physical attacks during the planarization process using the CMP technique.



POR 64; Ex. 1005 (Kim), [0105], Fig. 9A

Petitioner's Modification



POR 63; Ex. 2009 (PO's Expert Dr. Campbell Sec. Decl.) ¶ 81

Petitioner's New Reply Theories Are Forfeited And Defective

Petitioner's Reply

64. PO is incorrect. Prior art shows repetitive CMP applications that result in protruding elements above a planarized surface:

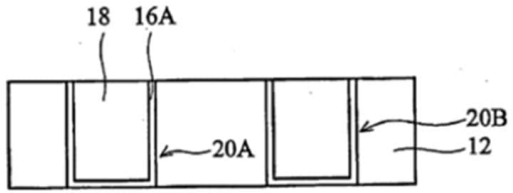


FIG. 1D

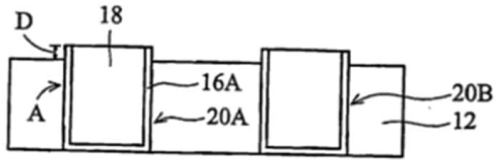


FIG. 1E

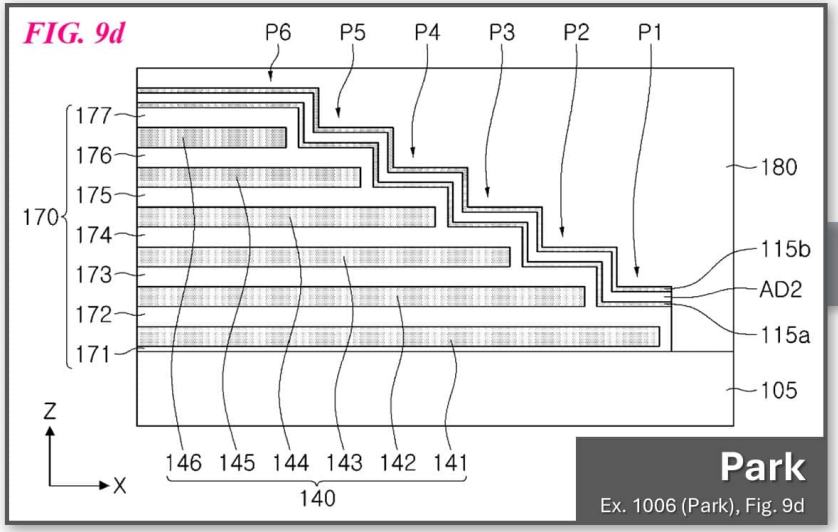
Ex. 1030, Figs. 1D–1E, [0018]–[0019]. This illustrates that a POSITA would have known how to planarize a top surface without damaging adjacent protruding structures.

Further, Park itself suggests two CMP steps, before and after forming the conductive layer.[10] Park, [0089]; [0110], Fig. 9j; Banerjee2 ¶79. Indeed, it was routine to protect vulnerable elements during CMP processes. Banerjee2 ¶¶78–81.

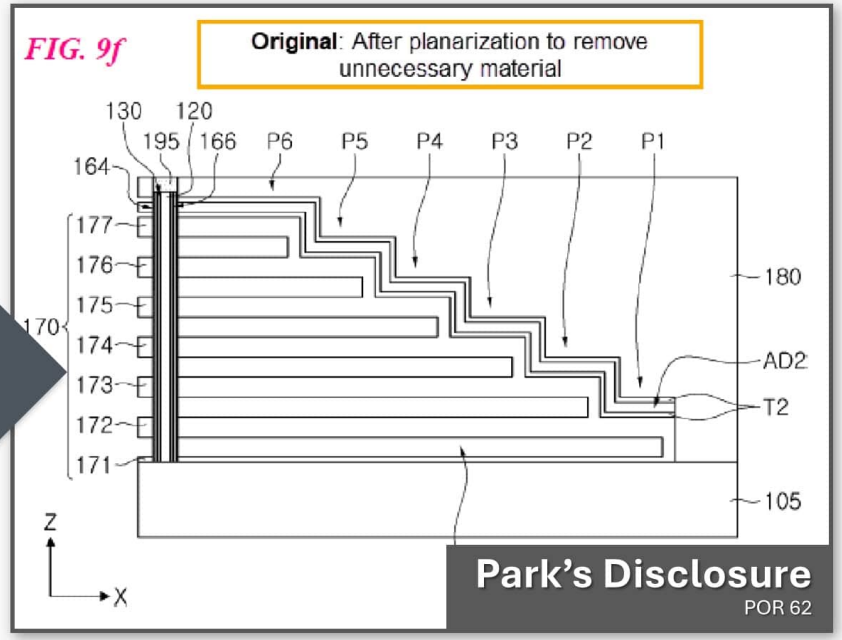
Reply 25-26

Manufacturing Differences Between Park And Fang Defeat Motivation To Combine

Planarization *Before* Etch-Stop Layer

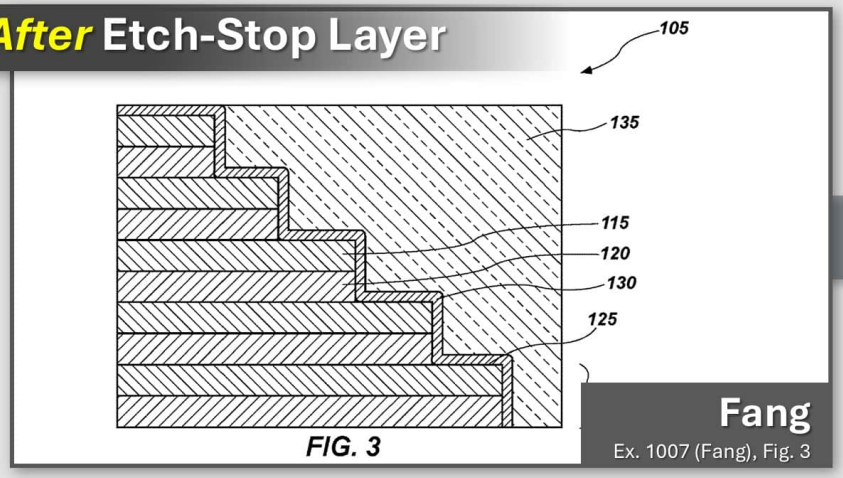


Park
Ex. 1006 (Park), Fig. 9d

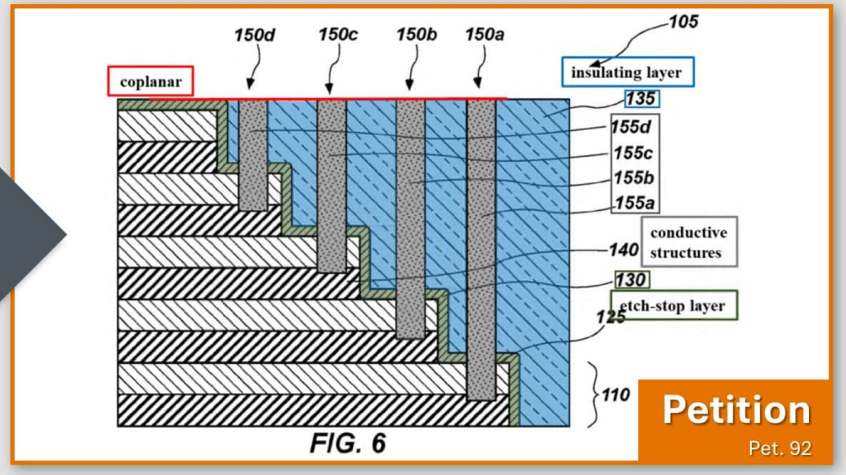


Park's Disclosure
POR 62

Planarization *After* Etch-Stop Layer



Fang
Ex. 1007 (Fang), Fig. 3



Petition
Pet. 92

Petitioner's Expert Misunderstood Park's Design

Petitioner's Expert Dr. Banerjee

Q. Okay. And to the extent that you recall what you testified regarding T2 and the layers 115A and B versus 110A and B, now that you have a chance to review these paragraphs, is there anything that you recall that -- that you -- strike that. Okay. So is it your opinion -- strike that. Is it your understanding that elements 115A and 115B are the same as elements 110A and 110B?

A. You're reading paragraphs 104 and 105. Yeah, I think there's a 1-to-1 correspondence between 115A and 110A and 115B and one oh -- 110B. Both of them are referred to as etch-stop layers.

Q. And that's what you meant by correspondence?

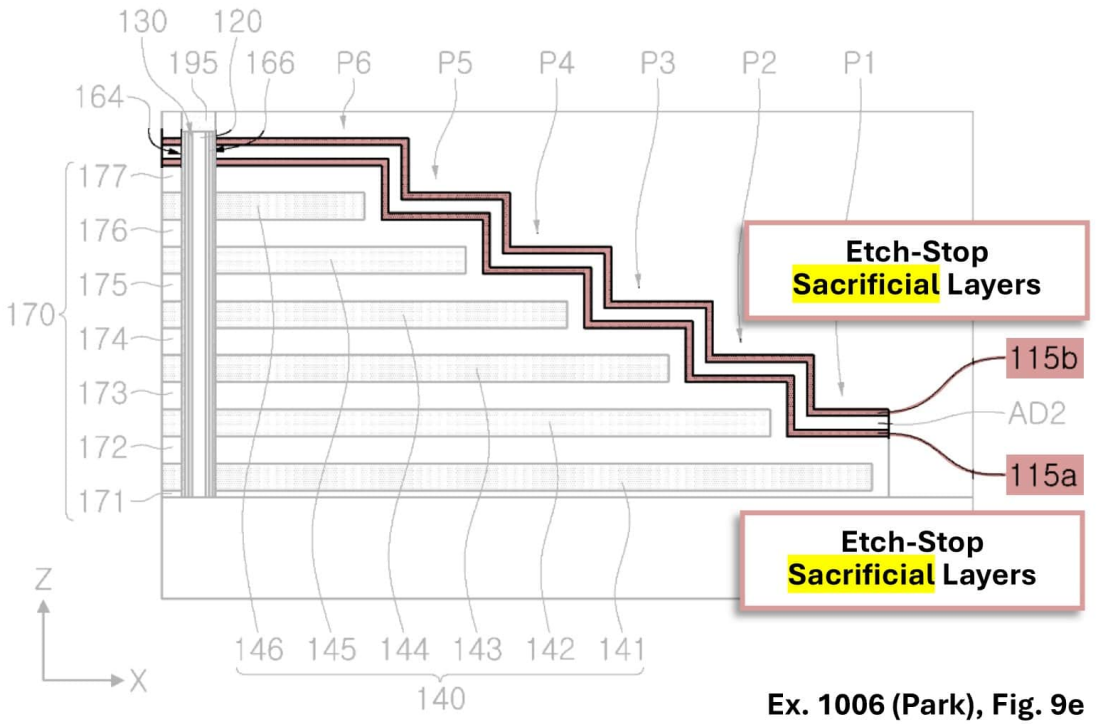
A. Yes.

Ex. 2008 (Petitioner's Expert, Dr. Banerjee Dep.), 75:13-76:7 (objection omitted)

Petitioner's Expert Misunderstood Park's Design

Park

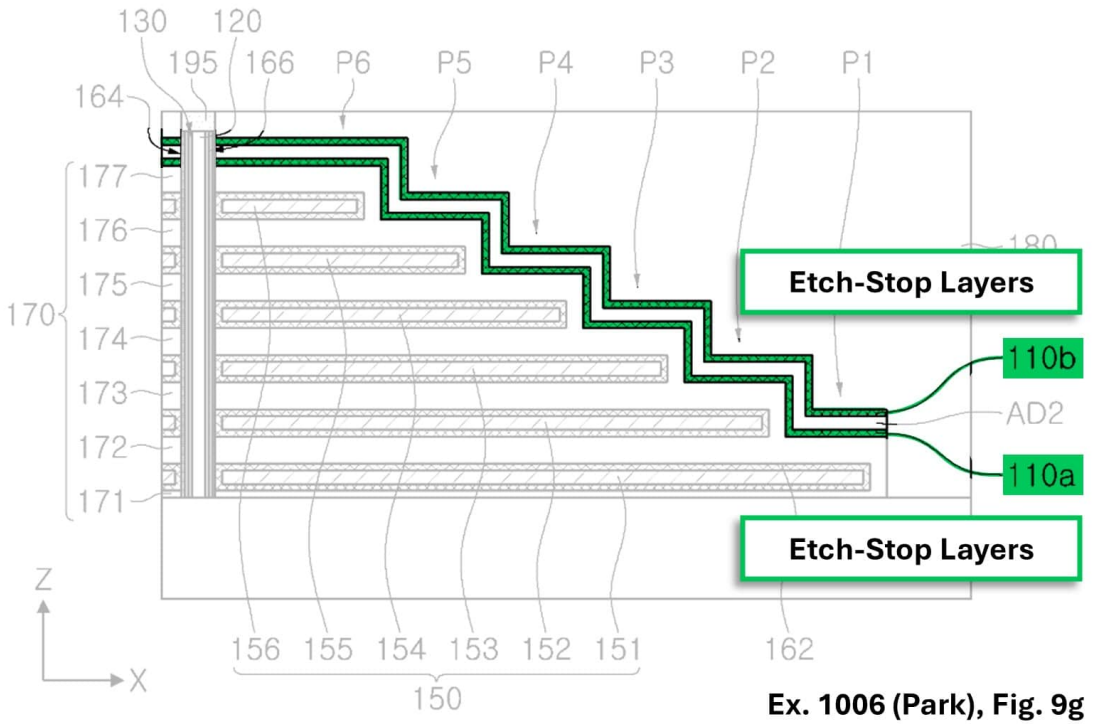
FIG. 9e



Ex. 1006 (Park), Fig. 9e

Park

FIG. 9g



Ex. 1006 (Park), Fig. 9g

Ground 4: Park And Fang Do Not Render Obvious Claims 10 And 17

10. The semiconductor structure of claim **1**, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.

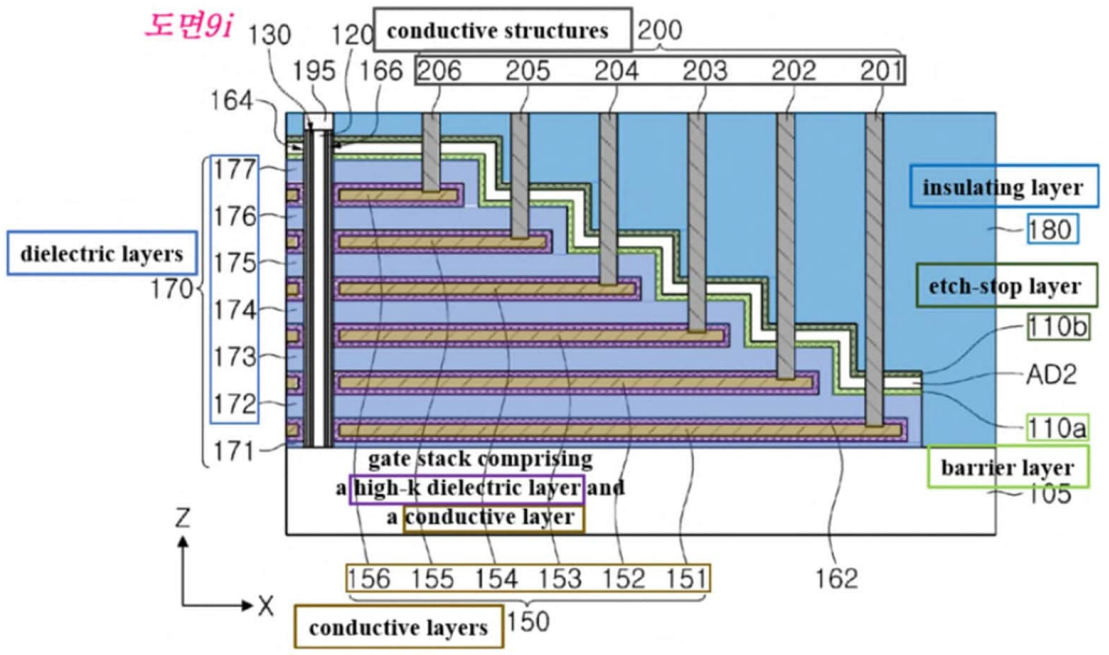
Ex. 1001 ('711 Patent), Claim 10

17. The semiconductor structure of claim **13**, wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.

Ex. 1001 ('711 Patent), Claim 17

A POSITA Would Not Have Applied Fang's Thicknesses To Park

Petition



Pet. 30; Ex. 1006 (Park), Fig. 9i

Petition

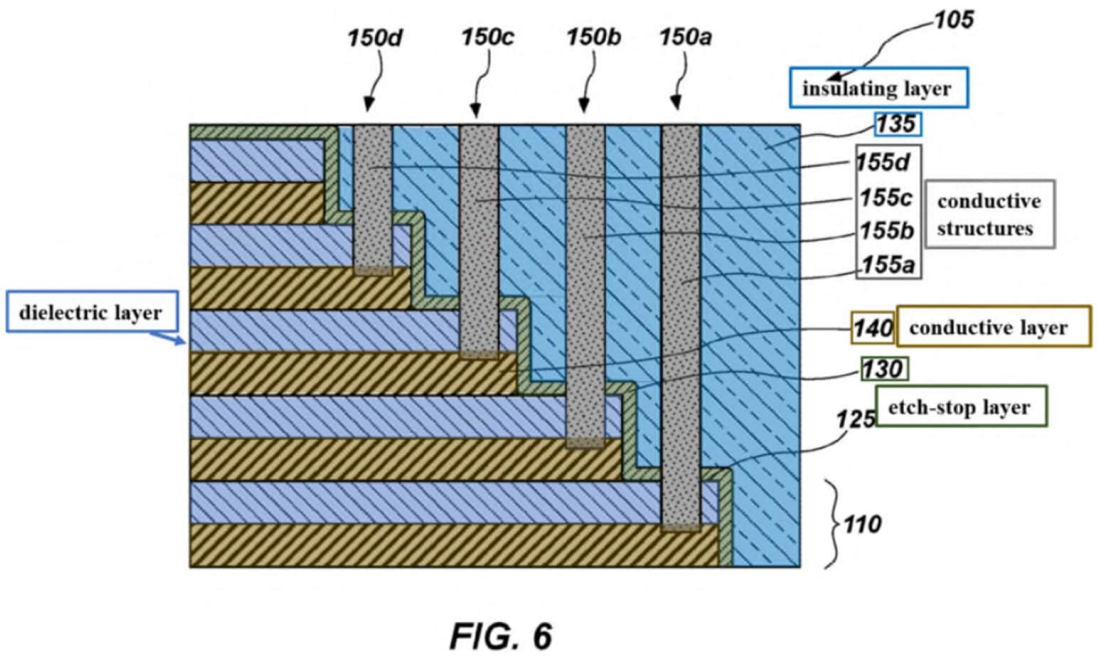


FIG. 6

Pet. 32; Ex. 1007 (Fang), Fig. 6

A POSITA Would Not Have Applied Fang's Thicknesses To Park

Patent Owner's Expert Dr. Campbell

Q. Well, sorry, then let me set up the scenario a little better. So you have -- let's go from the bottom to the top. You add a first layer, a second layer and a third layer.

A. Yeah.

Q. Is it also a good engineering practice to have the etch rates between the first and the third layer be selective, meaning etching have a higher etch rate for the first layer -- for the third layer than the first layer?

A. I'm trying to envision in what way that would be helpful. The only way that you -- that I can conceive of is if layer two is extremely thin so that ions penetrate not just etch but go all the way through layer two to layer three.

Q. So would you put the high-K layer around the gate layer within that extremely thin layer or outside that scope?

A. Those layers are certainly not layers. They are an additional, maybe 2 to 10 nanometers. Even 2 is kind of small. 2 Let's say 5 to 10, maybe 15 nanometers.

Ex. 1027 (PO's Expert Dr. Campbell Dep.), 98:24-99:6; 99:13-100:8; 100:21-101:2 (objections omitted)

Dr. Campbell Is A POSITA

Petition

VIII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the field of the '711 patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, how it is manufactured, and its component parts. Banerjee, ¶ 42.

Pet. 27

Dr. Campbell Is A POSITA

Patent Owner's Expert, Dr. Campbell's CV

Curriculum Vitae
Stephen A. Campbell

Educational History

PhD	Physics	Northwestern University	1981
MS	Physics	Northwestern University	1978
BA	Physics	College of St. Thomas	1975

* * *

Professor Campbell is the author of *Fabrication Engineering at the Micro and Nanoscale*, one of the most widely used textbook on microfabrication. This text has been used in more than 60 US schools as well as many schools in Europe and Asia.

* * *

Professor Campbell's teaching experience includes Microfabrication, Semiconductor Devices, Electromagnetic Fields, Analog Electronics, Linear Circuits, Circuits Lab, Senior Design, and Materials and Devices. In research, Professor Campbell is most well-known for pioneering efforts in high permittivity (aka high-k) materials for the gate insulator in deeply scaled MOSFETs. This revolution in transistor design has now been adopted by most of the leading-edge integrated circuit manufacturers. His other current interests include ultra-high-speed MEMS and efficient thin film

Ex. 2006 (PO's Expert Dr. Campbell's CV), 1

Dr. Campbell's Knowledge Shows He Is A POSITA

Etch Material

Patent Owner's Expert, Dr. Campbell

A. ... Further, etch processes are highly dependent on the material used, the depth and aspect ratio of the desired etch, the material to be deposited on the sidewalls, the material on which the etch is stopped ...

Q. And how do these excerpts we read relate to your area of expertise?

A. These align very well with the areas that I am an expert in.

Ex. 1027 (PO's Expert Dr. Campbell Dep.), 133:8-24

Etch Process Design Aspects

Patent Owner's Expert, Dr. Campbell

Q. ...[D]o you consider yourself qualified to offer an opinion on those types of design aspects that relate to etch processes?

A. Absolutely ... that's the point to the process people ... telling the designers you can't do this ....

Ex. 1027 (PO's Expert Dr. Campbell Dep.), 134:17-135:3

Petitioner's "design" Attack Is A Strawman

Patent Owner's Expert, Dr. Campbell

Q. Is it your opinion that a POSITA in the area of semiconductor designs can build a device using the disclosure of the '711 Patent assuming there's no limit on time and resources?

A. The '711 Patent is primarily a process in -- a process description. The design, if you will, where the transistors go and so forth is really modest by comparison. I don't know if the processing people are saying which layers go where and how thick they are and how you're going to etch things. Those are all process parameters.

So a POSITA in design, probably not because he's not in the right area.

Ex. 1027 (PO's Expert Dr. Campbell Dep.), 150:14-151:5