

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: June 16, 2026

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2025-00117
Patent 10,672,711

PATENT OWNER'S NOTICE OF APPEAL

Notice is hereby given, pursuant to 37 C.F.R. § 90.2(a), that Patent Owner Yangtze Memory Technologies Company, Ltd. ("Patent Owner") appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision entered by the Patent Trial and Appeal Board (the "Board") on June 1, 2026 (Paper 56) (the "Final Written Decision," a copy of which is attached hereto as Exhibit A).

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Patent Owner further indicates that the issues on appeal may include, without limitation:

- Whether the Board erred in determining that Petitioner has shown by a preponderance of the evidence that any or all of the challenged claims (claims 1-19) of U.S. Patent No. 10,672,711 are unpatentable as obvious, along with all reasons, findings, opinions, and orders leading thereto or underlying that decision.

Pursuant to 35 U.S.C. § 142 and 37 C.F.R. § 90.2(a), this Notice is being filed with the Director of the USPTO, and a copy of this Notice is being concurrently filed with the Board. In addition, a copy of the Notice of Appeal, along with the required docketing fee, is being filed with the Clerk of Court for the United States Court of Appeals for the Federal Circuit.

Respectfully submitted,

Dated: June 16, 2026

By: / Inge A. Osman /

Inge A. Osman (Reg. No. 74,480)
inge.osman@lw.com
Latham & Watkins LLP
555 Eleventh Street, NW, Ste. 1000
Washington, DC 20004-1304
Tel.: 202.637.2200
Fax: 202.637.2201

*Counsel for Patent Owner
Yangtze Memory Technologies
Company, Ltd.*

CERTIFICATE OF SERVICE

I hereby certify that, pursuant to 37 C.F.R. § 90.2(a)(1)(ii), on this 16th day of June, 2026, I electronically filed the foregoing **PATENT OWNER'S NOTICE OF APPEAL** with the Patent Trial and Appeal Board via P-TACTS, in accordance with 37 C.F.R. § 42.6(b)(1).

I also hereby certify that, pursuant to 37 CFR 90.2(a)(1)(i), on this 16th day of June, 2026, a true and correct copy of the foregoing **PATENT OWNER'S NOTICE OF APPEAL** is being filed with the Director of the United States Patent and Trademark Office by electronic mail to efileSO@uspto.gov.

I also hereby certify that, pursuant to Federal Circuit Rule 52(a)(2), on the 16th day of June, 2026, a true and correct copy of the foregoing **PATENT OWNER'S NOTICE OF APPEAL** and the filing fee, were filed with the Clerk's Office of the U.S. Court of Appeals for the Federal Circuit via CM/ECF.

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 16th day of June, 2026, a true and correct copy of the foregoing **PATENT OWNER'S NOTICE OF APPEAL** was served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

Jeremy Jason Lang (Reg. No. 73,604)
Travis Jensen (Reg. No. 60,087)
Jared Bobrow (admitted *pro hac vice*)
Orrick, Herrington & Sutcliffe LLP
1000 Marsh Road
Menlo Park, CA 94025-1015
T: 650-614-7400
F: 650-614-7401
jlang@orrick.com
tjensen@orrick.com
jbobrow@orrick.com
PTABDocketJL2@orrick.com
P52PTABDocket@orrick.com
PTABDocketJ3B3@orrick.com
PTABDocketJ1H1@orrick.com
MICRON-YMTC_ohs@orrick.com

Johannes Hsu (Reg. No. 74,689)
Orrick, Herrington & Sutcliffe LLP
2050 Main Street, Suite 1100
Irvine, CA 92614-8255
T: 949-567-6700
F: 949-567-6710
johanneshsu@orrick.com

By: / Inge A. Osman /

Inge A. Osman (Reg. No. 74,480)
inge.osman@lw.com
Latham & Watkins LLP
555 Eleventh Street, NW, Ste. 1000
Washington, DC 20004-1304
Tel.: 202.637.2200
Fax: 202.637.2201

*Counsel for Patent Owner
Yangtze Memory Technologies
Company, Ltd.*

EXHIBIT A

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2025-00117
Patent 10,672,711 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

CYGAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. *Background and Summary*

Micron Technology, Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–19 of U.S. Patent No. 10,672,711 B2 (Ex. 1001, “the ’711 patent”). Paper 1 (“Pet.”). The Petition is supported by a Declaration from Dr. Sanjay Banerjee. Ex. 1003 (“Banerjee Declaration”). Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) filed a Preliminary Response to the Petition, supported by a Declaration from Dr. Stephen Campbell. Paper 9 (“Prelim. Resp.”); Ex. 2007 (“Campbell Dec.”). On that record, we instituted an *inter partes* review of claims 1–19 of the ’711 patent. Paper 19 (“Inst. Dec.”).

Patent Owner filed a Response accompanied by a second declaration from Dr. Campbell. Paper 27 (“PO Resp.”); Ex. 2009 (“Campbell 2nd Dec.”). Patent Owner also filed a deposition of Dr. Banerjee. Ex. 2008 (“Banerjee Dep.”). Petitioner filed a Reply accompanied by a second declaration from Dr. Banerjee. Paper 36 (“Pet. Reply”); Ex. 1028 (“Banerjee 2nd Dec.”). Petitioner also filed a deposition of Dr. Campbell. Ex. 1027 (“Campbell Dep.”). Patent Owner filed a Sur-reply. Paper 44 (“PO Sur-reply”). We held an oral hearing on March 13, 2026, and a transcript of that hearing is included in the record. Paper 55 (“Tr.”).

B. *Real Parties-in-Interest*

Petitioner identifies itself and its subsidiaries, including Micron Consumer Products Group LLC, as real parties-in-interest. Pet. 6. Patent Owner identifies itself as the real party-in-interest. Paper 4, 1.

C. *Related Matters*

The parties represent that the ’711 patent is involved in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and*

Micron Consumer Products Group, LLC, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023). Paper 4, 1; Pet. 6–7. Petitioner also filed IPRs challenging other patents asserted in the district court case. Pet. 7–8.

D. The '711 Patent

The '711 patent is titled “Word Line Contact Structure for Three-Dimensional Memory Devices and Fabrication Methods Thereof.” Ex. 1001, code (54). The '711 patent issued on June 2, 2020, from Application No. 16/126,947, filed on September 10, 2018, and is a continuation of PCT/CN/2018/101308, filed on August 20, 2018. *Id.* at codes (21), (22), (63). The '711 patent relates to a word line contact structure including a staircase structure having a conductor layer disposed over a dielectric layer, with a barrier layer disposed over a portion of the conductive layer on each step of the staircase. *Id.* at code (57).

E. Illustrative Claim

Claim 1 is illustrative, and recites as follows:¹

[1.PRE] A semiconductor structure, comprising:

[1.A] a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer;

[1.B] a barrier layer disposed over a portion of the gate stack of the each step;

[1.C] an etch-stop layer disposed on the barrier layer;

[1.D] an insulating layer disposed on the etch-stop layer;
and

¹ Bracketed organization added as per the Petition.

[1.E] a plurality of conductive structures formed in the insulating layer, wherein each conductive structure is formed on the conductive layer of the each step.

Ex. 1001, 15:2–12.

F. Evidence

Petitioner relies on the following patent and non-patent document evidence:

Name	Document	Exhibit
Kim et al. “Kim”	US 2012/0070944 A1	1005
Park et al. “Park”	KR 10-2015-0051841	1006
Fang	US 2019/0067306 A1	1007

G. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–19 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–9, 11–16, 18, 19	103 ²	Kim ³
10, 17	103	Kim, Fang
1–6, 8, 9, 11–16, 18, 19	103	Park
7, 10, 15, 17	103	Park, Fang

² We apply AIA 35 U.S.C. § 103 to the ’711 patent because it was filed after, and never claimed the benefit of an effective filing date before, March 16, 2013. Ex. 1001, codes (22), (63); Pet. 6.

³ Petitioner styles this ground and the Park ground as also being based on “a POSITA’s [Person of Ordinary Skill In The Art] knowledge.” Pet. 11. However, an *inter partes* review may be requested “only on the basis of prior art consisting of patents or printed publications,” although it may “rely on evidence beyond prior art documents.” 35 U.S.C. § 311(b); *Qualcomm Inc. v. Apple, Inc.*, 24 F.4th 1367, 1374–75 (Fed. Cir. 2022). Patent Owner did not raise a § 311(b) challenge.

II. ANALYSIS

A. *Legal Standards*

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, “would have been obvious at the time the invention was made to a person having ordinary skill in the art [to which said subject matter pertains].” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness.⁴ *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. *Level of Ordinary Skill in the Art*

Petitioner asserts that a person of ordinary skill in the art (“POSITA”) at the critical time “would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience).” Pet. 27 (citing Ex. 1003 ¶ 42). Petitioner further asserts that a POSITA “would have been aware of and generally knowledgeable about 3D NAND’s structure, its component parts, how it operates, and how it is controlled.” *Id.* Patent Owner does not dispute Petitioner’s definition. PO Resp. 7. We adopt Petitioner’s proposed

⁴ Neither party presents evidence or arguments regarding objective evidence of non-obviousness. Pet. 103; PO Resp.

level of ordinary skill, as it appears to be consistent with the specification of the '711 patent and the prior art of record.

C. Claim Construction

In an *inter partes* review, we construe a patent claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). Under this standard, the words of a claim generally are given their “ordinary and customary meaning,” which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

Petitioner did not propose any express claim construction in its Petition. Pet. 26. In its Response, Patent Owner states that it agrees that all terms have their plain and ordinary meaning. PO Resp. 8.

However, for claims 13–15, the Petition relies on a definition from the '711 patent. Pet. 58–60, 86–89. In these claims, Petitioner addresses the limitation, “the etch-stop layer is formed on a side surface and a top surface of each step.” Ex. 1001, Claim 14. Petitioner asserts that “the '711 patent defines ‘on’ to include both directly on something and indirectly on that something.” Pet. 58 (citing Ex. 1001, 4:1–6; Ex. 1003 ¶¶ 117–118). Petitioner requires this definition for its obviousness assertions because it relies on a teaching of a layer that is indirectly “on”; i.e., via another intermediate layer. Pet. 58–60, 86–89.

Patent Owner argues that this limitation of claims 14 and 15 should be construed as “directly contacting a side surface and a top surface of each step.” PO Resp. 8. Patent Owner acknowledges that the '711 patent specifies a broader definition of “on,” permitting an intermediate feature or

layer therebetween. *Id.* (citing Ex. 1001, 4:1–6). However, Patent Owner argues that a more specific definition is provided for “on [a/the] surface.” *Id.* at 9 (alteration in original). Patent Owner points to multiple places in the ’711 patent of “on [a/the] surface” being used to describe directly touching the surface. *Id.* (citing Ex. 2009 ¶ 28) (alteration in original); PO Sur-reply 3–4. Patent Owner further points to Dr. Banerjee’s annotation of Kim’s Fig. 22A, showing red “top surfaces” and yellow “side surfaces” directly contacting the alternating gate stack and insulating layers. PO Resp. 13–14 (citing Ex. 1003 ¶ 110). Patent Owner further argues that Dr. Campbell’s statement that an “expert in semiconductor fabrication” would understand “on the surface” to mean “there has to be contact between one layer and the other” supports its characterization of the plain meaning of that phrase. PO Sur-reply 3 (citing Ex. 1027, 146:25–147:6).

Based on the record before us, we agree with Petitioner that “on a surface” should be interpreted in line with the definition of “on” set forth in the ’711 patent. Ex. 1001, 4:1–6. We particularly note that the ’711 patent states that “‘on’ . . . should be interpreted in the broadest manner” and that “on” is not limited to “directly on.” *Id.* Instead, the ’711 patent states that “‘on’ also includes the meaning of ‘on’ something with an intermediate feature or layer therebetween.” *Id.* Patent Owner agrees that this definition controls the “standalone ‘on’” term such that A may be on B even if there is an intervening layer between them. Tr. 55:8–11 (“The standalone ‘on,’ we agree in the context of the patent, you can have intervening layers. I think the patent is clear about that.”). Claim 14 recites that the etch-stop layer is “on” something; i.e., “on a side surface and a top surface of each step.” Ex. 1001, 16:20–22. Patent Owner agrees that a surface is a “something.” Tr. 56:5–8 (“surface obviously is a something”). Substituting the “a

surface” of claim 14 for the “something” of the ’711 patent’s definition of “‘on’ *something* with an intermediate feature or layer therebetween” results in claim 14 reading as, “on *a surface* with an intermediate feature or layer therebetween.” Unlike “directly on,” which specifies the relation between two things, “a surface” may merely indicate the thing that something is “on,” particularly when “on” is “interpreted in the broadest manner” as expressly required by the ’711 patent.

Although Patent Owner argues that the ’711 patent provides examples such as Figures 1 and 9A in which “on a surface” is illustrated or described as directly touching that surface, these examples are not described as limiting. *See, e.g.*, Ex. 2009 ¶ 28; Ex. 1001, Figs. 1, 3–4, 9A. Moreover, the ’711 patent uses “directly” as an additional descriptor, indicating that certain layers are “directly on,” “directly disposed on,” or “directly contacting” other layers. *See, e.g.*, Ex. 1001, 11:16–19 (“a third conductive material . . . directly on the exposed portions of the exposed gate conductive layer”), 11:20–22 (“VIA conductive structures 945 are directly disposed on the exposed gate conductive layer”), 11:39–40 (“directly contacting and connected to”). Similarly, Patent Owner’s argument that Figures 9A and 9B are described by language such as “directly contacts” does not transform the construction of the separate term “on” into “directly on.” PO Resp. 9–11. Indeed, figures are not required to describe the full extent of the claims (particularly, dependent claims), but may describe certain embodiments. As noted by Petitioner, the embodiments are described as merely “exemplary.” Pet. Reply 2–3 (citing Ex. 1001, 14:64–67). Rather, the use of “directly on” appearing in certain descriptions in the ’711 patent indicates it is used for particular embodiments for which the features are in direct contact, and that features should not be assumed to be in direct contact in the absence of the

“directly” (or similar) qualifier. As further noted by Petitioner, claim 13, from which claim 14 depends, uses the narrower term “directly contacts” to describe the relation between its conductive structures and its conductive layers, but only requires that the etch-stop layer is “disposed on” its gate stack layer. *Id.* at 2 (citing Ex. 1001, 16:12–13). Considering “on” to permit intervening layers unless further qualified by “directly” or a similar term is consistent with the description of “on” as including, but not limited to, “directly on.” Ex. 1001, 4:1–6.

Although Dr. Campbell testified in his deposition in response to Petitioner’s counsel that “on the surface” requires direct contact with the surface, his interpretation was based on “embodiments of” the patent rather than a general understanding of a person skilled in the art confronted with that term. Ex. 1027, 122:6–25, 124:6–23 (“I’m not sure if there are other sources for that, but it was on the ’711, so I’ve taken it there.”). Dr. Campbell, upon questioning from Patent Owner’s counsel, later stated that “an expert in semiconductor fabrication” would understand “on the surface” to mean “contact between one layer and another . . . with nothing in between.” *Id.* at 146:25–147:6. However, Dr. Campbell did not explain why such an interpretation is particular to the semiconductor fabrication art, or provide other explanation or support for this statement, which is in tension with the definition of “on” in the ’711 patent. Accordingly, we significantly discount the weight accorded to that statement. *Phillips*, 415 F.3d at 1318 (stating, “conclusory, unsupported assertions by experts as to the definition of a claim term are not useful to a court. Similarly, a court should discount any expert testimony ‘that is clearly at odds with the claim construction mandated by the claims themselves, the written description, and

the prosecution history, in other words, with the written record of the patent.”).

On balance, Dr. Campbell’s testimony is best understood as a description of certain Figures of the ’711 patent rather than a representation of an ordinarily skilled person’s understanding of the term “on the surface.” *See* Ex. 2009 ¶ 47 (describing Figs. 1, 3, and 4 as depicting layers in contact with the underlying layer or substrate). For example, Dr. Campbell describes Figure 9A as having a barrier layer “on *and* directly contacting the top and side surfaces of each step.” *Id.* ¶ 28 (emphasis added) (citing *inter alia* Ex. 1001, 7:6–67). Dr. Campbell does not explain why, beyond the fact that many Figures show layers as adjacent and in contact, a person of ordinary skill in the relevant art would understand those Figures to limit the claim language rather than illustrating particular embodiments that fall within a broader scope of claims 14 and 15. *See Hill-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014) (“While we read claims in view of the specification, of which they are a part, we do not read limitations from the embodiments in the specifications into the claims.”).

We do not agree with Patent Owner that “on the surface” in claim 14 needs to be “directly on the surface” in order to give some meaning to the term “surface.” PO Resp. 14; PO Sur-reply 4. Claim 14 further limits claim 13, which requires the etch-stop layer only “on a portion” of each step, by additionally requiring the etch-stop layer to be on particular parts of each step; i.e., the side surface and the top surface of each step. *See* Pet. Reply 3 (“terms ‘side/top surface’ provide a reference point”). Claim 13 does not require an etch-stop layer on a side of each step, but Claim 14 does.

With respect to Patent Owner’s argument that the ’711 patent equates “on” with “above” and “over, we agree with Petitioner that both “above” and

“over” are also used in the ’711 patent to permit, but not require, direct contact. PO Resp. 10 (citing Ex. 1001, 4:1–10); Pet. Reply 3; Ex. 1001, 4:6–10 (“‘above’ or ‘over’ means ‘above’ or ‘over’ something, but can also include the meaning it is ‘above’ or ‘over’ something with no intermediate feature or layer therebetween (i.e., directly on something)”). Moreover, the language at issue in claims 14 and 15 is “on,” which has an express meaning in the ’711 patent, and not “above” or “over,” which may have additional or divergent meanings in that document. *See* Ex. 1001, 4:11–12 (discussing “above” as a “spatially relative term), 4:40–41 (indicating that a layer can be “over” either an “overlying” or an “underlying” structure). Thus, the explicit definition of “on” provided in the ’711 patent is much more probative in determining the meaning of the language “on [a/the] side surface” in claims 14 and 15.

Patent Owner also asserts that the ’711 patent does not permit the surface of each step to include the surface of additional layers placed on the staircase steps, because the staircase steps are the result of an etch-trim cycle having a lateral dimension “a.” PO Resp. 11 (citing Ex. 1001, 6:53–67, 7:16–18, 12:3–5). Patent Owner further points to Petitioner’s statement that the staircase structure “provides landing areas, i.e., steps, for the contacts,” and Dr. Banerjee’s statements that the steps “provide landing areas for staircase contacts” and “a step, namely, the gate stack and the immediately below dielectric layer.” *Id.* at 12 (citing Ex 1003 ¶¶ 57, 87, 145; Pet. 1, 46) (emphasis omitted). However, the ’711 patent does not limit “step” to the result of the etch-trim cycle, but more generally refers to each stair as a step even where covered with further layers. *See, e.g.*, Ex. 1001, 7:56–58, 8:20–24, 8:36–38 (stating, “In some embodiments, the third insulating layer 420 can cover each step of the staircase structure 300,” where “staircase structure

300 is formed by disposing an etch-stop layer on the staircase structure 200” and staircase structure 300 has a “top surface 310S”).

Patent Owner argues that the Petitioner exceeds the scope of its Reply “in abandoning plain meaning (Pet. 26) for lexicography (Reply 2).” PO Sur-reply 4. We do not agree, because Petitioner asserts in the Petition that the ’711 patent contains a definition of “on” that controlled its meaning in claims 13–15. Pet. 58–60, 86–89. Regardless of whether Petitioner characterizes its assertions as “lexicography,” Patent Owner was apprised of Petitioner’s “on” assertions and responded to them in its Patent Owner Response. PO Resp. 8 (“there appears to be a dispute with respect to the meaning of the terms ‘on a side surface and a top surface of each step’” . . . “Petitioner contends that the ’711 patent specifies that ‘on’ means “‘directly on’ something, but also includes the meaning of ‘on’ something with an intermediate feature or layer therebetween.” (citing Ex. 1001, 4:1–6)). We must consider the Petition’s lexicography-based arguments to which Patent Owner has responded. *See Axonics, Inc. v. Medtronic, Inc.*, 75 F.4th 1374, 1381 (Fed. Cir. 2023) (“in an IPR proceeding, ‘the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond.’”). Consequently, Petitioner’s Reply properly addressed this issue.

Based upon the entirety of the disclosure of the ’711 patent and the evidence of record, we determine that “on the surface” and “on a surface” as set forth in claims 14 and 15 include something that is on the/a surface with an intermediate layer therebetween.

D. Obviousness over Kim

Petitioner asserts that claims 1–9, 11–16, 18, and 19 are unpatentable under 35 U.S.C. § 103 as obvious over Kim in view of the knowledge of a

person of ordinary skill in the art. Pet. 32–62. Patent Owner argues against this assertion. PO Resp. 9–26.

1. *Kim*

Kim is titled “Methods of Manufacturing Three Dimensional Semiconductor Devices.” Ex. 1005, code (54). Kim relates to providing a semiconductor substrate including a peripheral region, having a peripheral structure, and a cell array region, having a cell structure thicker than the peripheral structure. *Id.* at code (57). Both structures are covered by an interlayer dielectric, on which is formed a polishing stop layer. *Id.* The interlayer dielectric is planarized using the polishing stop layer as a planarization stop. *Id.*

2. *Analysis of Claim 1*

We begin our analysis of Petitioner’s obviousness contentions with Petitioner’s assertions as to claim 1. Patent Owner contests Petitioner’s assertion that Kim in view of the knowledge of the prior art teaches “wherein each step comprises a gate stack disposed over a dielectric layer,” as set forth in limitation [1.A]. PO Resp. 15–28.

[1.PRE] A semiconductor structure, comprising: [1.A] a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer

To the extent the preamble [1.PRE] is limiting, Petitioner asserts that it is taught by Kim’s description of a 3D semiconductor device. Pet. 35 (citing Ex. 1005, code (57)). Petitioner asserts that Kim’s “stacked layer structure ST having the stepwise structure” teaches a staircase structure comprising a plurality of steps. *Id.* at 36–37 (citing Ex. 1005, Fig. 22A, ¶¶ 8, 185, 211; Ex. 1003 ¶ 87). Petitioner further asserts that each of Kim’s

steps comprises a gate stack comprising a high-k dielectric layer (Kim's "blocking insulating layer 150c") and a conductive layer (Kim's "gate electrodes 161–166"). *Id.* at 39–40 (citing Ex. 1005 ¶ 202 ("The formation of the gate electrodes 161 to 168 may include forming a gate conductive layer"), ¶ 200 ("forming a data storing layer 150 and gate electrodes 161 to [166]")); Ex. 1003 ¶ 90. Petitioner relies upon Figure 22A of Kim, reproduced below:

Fig. 22A

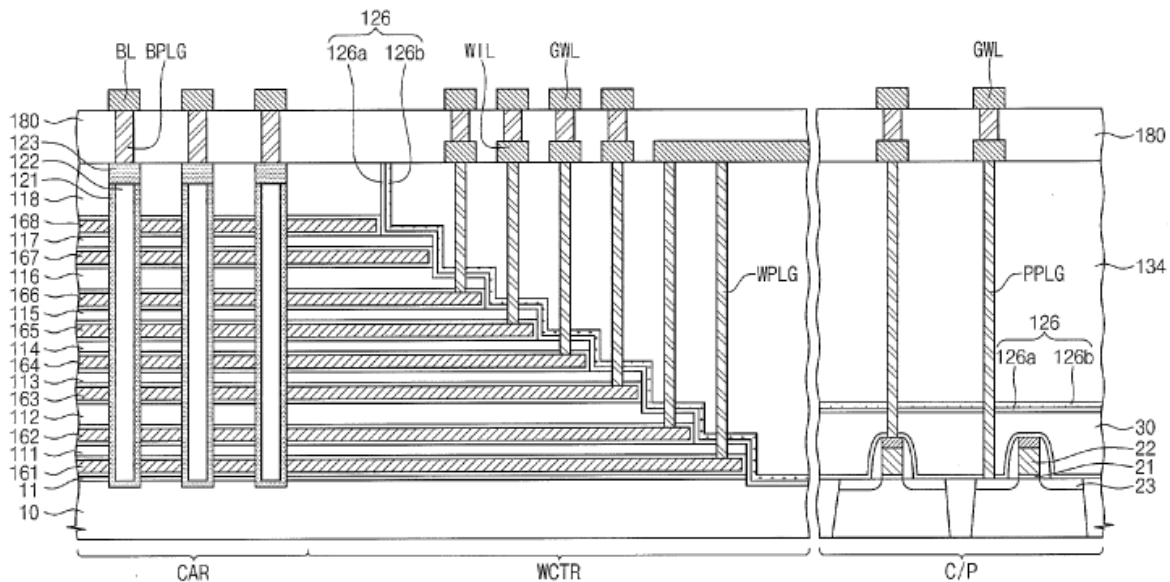


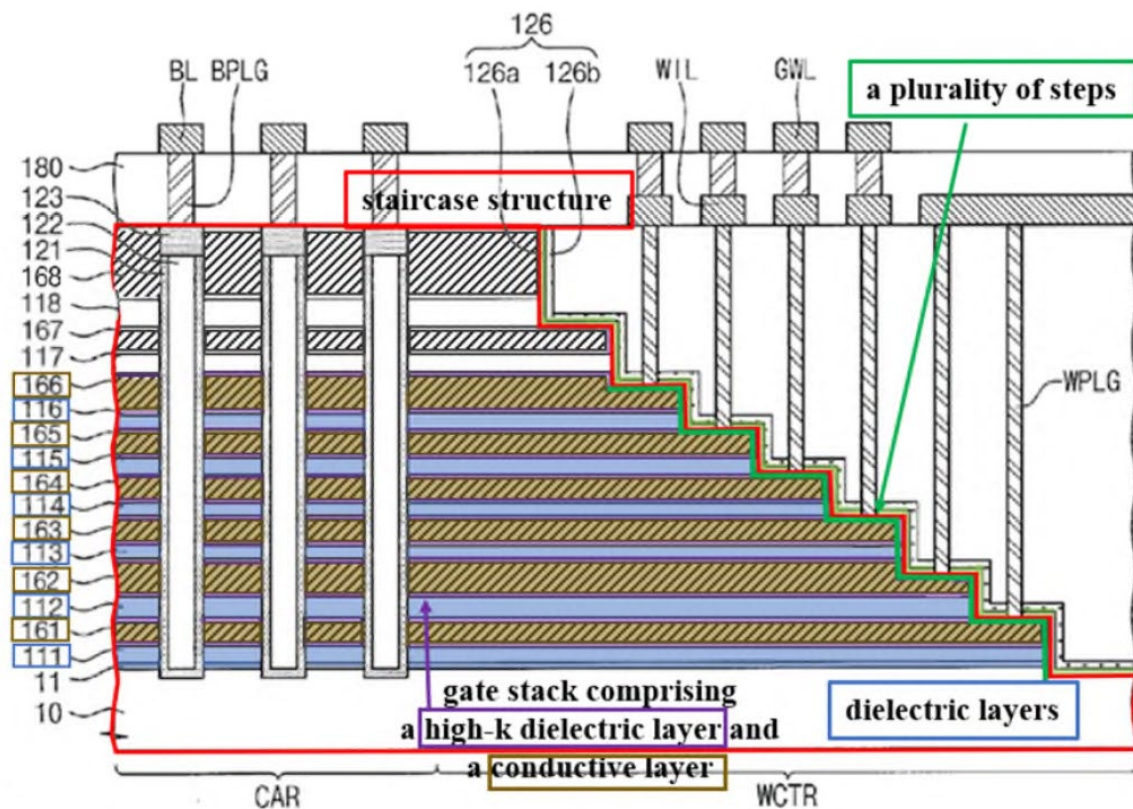
Figure 22A depicts, in pertinent part, gate electrodes 161–168 formed between insulating layers 111 to 118, supported by lower gate insulating layer 11 atop substrate 10. Ex. 1005 ¶¶ 141–142, 201–202, 209–210.

Petitioner further asserts that, in some of Kim's embodiments, the top surfaces of sacrificial layers SC1 to SC8, rather than the top surfaces of insulating layers 111 to 118, may be partially exposed and replaced with gate stacks. Pet. 28–29 (citing Ex. 1005 ¶¶ 90, 104–105, 198–200).

Petitioner asserts that Kim's embodiments having an etch-stop layer 126b and a barrier layer 126a (Figures 17A–22B) include the structure of other

elements that are only described in other embodiments (e.g., Figures 5A–14B). *Id.* at 29 (citing Ex. 1005 ¶¶ 183–212; Ex. 1003 ¶¶ 70–71), 41–43 (citing Ex. 1005 ¶ 201). Petitioner asserts that these combined descriptions describe that each gate stack may be disposed over a dielectric layer (one of Kim’s “insulating layers” 111–116). Pet. 39. Petitioner’s assertions are illustrated by an annotated Figure 22A, reproduced below:

Gate-Stack-on-Top Fig. 22A



Id. at 40. Annotated Figure 22A shows a staircase structure (red), a plurality of steps (green), dielectric layers (blue), a gate stack comprising a high-k dielectric layer (violet), and a conductive layer (tan).

a) Motivation to combine Kim’s descriptions

Patent Owner argues that Petitioner presents an obviousness argument that requires a motivation for combining distinct teachings from different

embodiments of a single reference. PO Resp. 17–18 (citing *In re Kotzab*, 217 F.3d 1365, 1370 (Fed. Cir. 2000) (“Even when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference.”)). Patent Owner argues that Petitioner relies on combining one embodiment in either Figure 4 or Figure 5A–14B with a separate embodiment in Figures 17A–22B. PO Sur-reply 5–6 (“Petitioner recreated Kim’s Figure 22A using an alternative description of yet another embodiment of Kim’s Figure 4”). Patent Owner argues that Petitioner only asserts that such teachings could be combined, not that there would be any benefit to doing so, or how both embodiments address the same problem. PO Resp. 18–19 (citing Ex. 2008, 35:12–36:1 (Banerjee Dep.)); PO Sur-reply 5–6. Patent Owner argues that there would instead be a detriment to switching the gate-stack order because it would require structural changes and changes to etching processes. PO Sur-reply 7–8. Patent Owner contends that although Petitioner argues that Kim’s embodiments have features that may be combined except where they differ, the embodiments sought to be combined do differ in material aspects such that their combination would have been unobvious and lack a reasonable expectation of success. PO Resp. 19, 25–26.

We determine that Petitioner has sufficiently shown that a person having ordinary skill in the art conversant with Kim would have found it obvious to combine Kim’s gate-stack-on-top configuration and its etch-stop and barrier layer structure. Kim partitions its disclosure into two main sections pertinent to this issue. First, Kim describes its “methods of fabricating,” including numerous embodiments, with reference to Figures 4 through 15. Ex. 1005 ¶¶ 13–14, 56–57. Kim’s statement that the top surfaces of the steps may be either the gate stack (e.g., the replaced

sacrificial layers) or the insulating layer are part of this first section. *Id.*

¶¶ 90, 140. Patent Owner does not dispute that Kim teaches that the order of layers may be reversed so as to form the gate stack on top. Tr. 44:1–2.

Second, Kim describes “other example embodiments” with reference to Figures 17 through 22. Ex. 1005 ¶¶ 179–184. Kim’s description of its etch-stop and barrier layer structure are part of this second section. *Id.* ¶ 187.

We agree with Petitioner that Kim’s first and second section are described as compatible, not mutually exclusive, embodiments. Kim’s second section builds further layers upon the structure of its first section, and states:

In these embodiments, the same elements as in the embodiments previously described with reference to FIGS. 5A through 14A and FIGS. 5B through 14B will be denoted by the same reference numbers therein, and *for concise description, overlapping description of elements* previously described with reference to FIGS. 5A through 14A and FIGS. 5B through 14B *may be omitted*.

Ex. 1005 ¶ 184 (emphasis added). Patent Owner argues that only the embodiments in Figures 17A–22B describe an etch-stop layer and a barrier layer (as claimed), and that the language cited for a gate-stack-on-top configuration (e.g., Ex. 1005 ¶¶ 90, 91, and 240) is “conspicuously absent from the description of Figures 17A–22B.” PO Resp. 20 (citing Ex. 2009 ¶ 36). However, Figures 17A–22B do not further address the underlying staircase structure that was detailed in the descriptions of the Figures 4 through 15 embodiments. While Figures 17A–22B show a gate-stack-on-bottom configuration, this merely continues the gate-stack-on-bottom illustrations that were used in all of the previous Figures, even for those in which it is undisputed that a gate-stack-on-top configuration is a described alternative. The Figures exemplify rather than limit the description of the

embodiments of Figure 17A–22B in the same manner that they present the gate-stack-on-bottom view in Figures 4–15 and do not exclude the gate-stack on bottom description of the embodiments exemplified by those figures.

Patent Owner argues that Petitioner has not met its burden to show that the description of the stack structure in Figure 22A would include the particular description of the gate-stack-on-top configuration. Tr. 52:4–9. In Patent Owner’s view, even the description of possible materials for the underlying gate stack would not be carried into the embodiments of Figures 17A–22B unless the later embodiments specifically refer back to that particular material. Tr. 74:23–75:14 (“If [the description in the Figure 4 to Figure 15 embodiments] says this certain layer can be tungsten . . . does [the Figure 17A to 22B embodiment description] refer back and say . . . for this layer . . . you can use any of the materials[?]”).⁵ A requirement that each embodiment explicitly refer back to elements described in earlier embodiments is not consistent with Kim’s statement that previously described elements are “omitted” in the Figures 17A to 22B section “for concise description.” Kim’s statement is instead more consistent with Petitioner’s assertion that aspects of the stack structure would be understood to apply to modifications above the stack in the embodiments of Figures 17A–22B, which rely upon, in unaltered form, the earlier-described elements of the stack.

⁵ However, Patent Owner does not contest Petitioner’s assertion for claim 8 that Kim’s description of word line conductive plugs comprising tungsten in Figures 4 and 14 applies to Petitioner’s word line conductive plugs of Figure 22A, despite the fact that Kim does not mention what materials those plugs may comprise in its description of Figure 22A. Pet. 53 (citing Ex. 1005 ¶ 173 and stating that descriptions of Figures 5A–14B apply); PO Resp.

Patent Owner points to *In re Fritch* for the proposition that one “cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art.” *In re Fritch*, 972 F.2d 1260, 1266 (Fed. Cir. 1992). However, the situation in *Fritch* was quite different from the one presented here. In *Fritch*, the Examiner went beyond the teachings of the reference to create new structural features; for example, finding an entire device to be flexible despite only a single portion of that device having been described to be flexible. *Id.* at 1265–66. In *Kim*, however, the stair structure being altered in Petitioner’s combination is expressly described as being able to be altered in that manner; i.e., to reverse the order of gate stack and insulator in each stair step. Ex. 1005 ¶ 90. Petitioner’s combination is similar to that in *Boston Scientific* in which a reference’s teaching of two coatings on a polymer stent made obvious the use of two coatings on a metal stent, despite the metal stent being described with only a single coating. *Boston Scientific Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 (Fed. Cir. 2009). *Boston Scientific* determined that this would have been a “predictable variation” such that obviousness “bars its patentability.” *Id.* (quoting *KSR*, 550 U.S. at 417); see *Chiron Corp. v. Genentech, Inc.*, 363 F.3d 1247, 1253 (Fed. Cir. 2004) (a specification need not disclose “itself . . . how to make and use every possible variant of the claimed invention, for the artisan's knowledge of the prior art and routine experimentation can often fill gaps, [and] **interpolate between embodiments**”) (emphasis per Pet. Reply 8). The Federal Circuit further explained that a single reference may describe “two existing approaches to a single problem as sufficiently interchangeable to motivate replacing one with the other.” *Apple, Inc. v. Smart Mobile Techs., LLC*, 2026 WL 55104 at *6 (Fed. Cir. Feb. 27, 2026) (nonprecedential) (describing the holding in *Intel Corp. v. PACT XPP*

Schweiz AG, 61 F. 4th 1373 (Fed. Cir. 2023)). Petitioner’s combination is not based solely on reconstructing the claims of the ’711 patent; instead, it is grounded in Kim’s explicit teaching of alternate possible orderings of gate stack and insulator in each step of the stair structure.

Petitioner’s reason to combine the disclosures in Kim is sufficient under *KSR*. Petitioner first argues that Kim’s description of either ordering of layers in the stair step would apply to the Figure 17A–22B embodiment because they are closely related and the later embodiment extensively references the earlier. Pet. 29. Contrary to Patent Owner’s argument that Petitioner relies solely on Figure 22A, which is limited to the insulator-on-top structure shown therein, Petitioner relies more generally on Kim’s teachings of a barrier layer that is “formed to conformally cover an exposed surface,” including a portion of the gate stack of the staircase structure, and an etch-stop layer disposed on the barrier layer. Pet. 42–43 (citing Kim ¶¶ 185–187, 213). Although the “Petition relies on Kim’s Figures 17A–22B embodiment comprising an etch-stop layer and a barrier layer,” the Petition also explicitly relies on Kim’s descriptions of other embodiments “with many of the same elements denoted by the same reference numerals” that are “extensively reference[d].” Pet. 29 (citing Ex. 1005 ¶¶ 183–212).

Moreover, Petitioner asserts that Kim’s teaching that the layer order may be reversed represents that either would be a suitable option for the Figures 17A–22B embodiment. Pet. 33–34. Petitioner identifies the problem sought to be addressed by both layer stack orders as “constructing a staircase structure,” and we agree that Kim’s staircase structure is integral to its methods of manufacturing three dimensional semiconductor devices to address limitations in the art, and as such, both represent alternative means for solving the same problem. *See* Ex. 1005 ¶¶ 3–8. Petitioner further

points to recognition in the art that either order was routine and highly predictable for semiconductor devices. Pet. 33 (citing Ex. 1008, Figs. 7A–7B as showing alternate layer orders), 34–35 (citing Exs. 1015, 1016 as illustrating a gate-stack-on-top ordering). Dr. Banerjee attests that “it would be trivial to alter the sequence of the precursor gas flows . . . to achieve either” material on top in the staircase because “either order was compatible with common deposition techniques such as CVD or ALD used to deposit these layers.” Ex. 1003 ¶ 81. Dr. Campbell and Patent Owner contest this characterization, attesting that the etching is “a very difficult process” as “it’s going to work in the actual fab[rication],” and attempting to swap the layers will cause “a lot of heartache.” Ex. 1027, 109:15–110:7; PO Resp. 20–21 (arguing that changes to the design and manufacturing processes would be required). However, Dr. Campbell also attests that “[i]t may be made to work eventually,” and that “generally speaking,” the prior art cited by Petitioner “provide[s] additional details in helping a [person of ordinary skill in the art] to implement these two embodiments”; i.e., the different layer ordering. Ex. 1027, 110:3–25 (referring to Ex. 1008, Figs. 7A, 7B). Dr. Campbell states that changing the layer order as shown in the prior art is “a lot of work,” but is not the “insane amount of work” that would be required in making a stack where “you are starting from ground zero.” *Id.* at 111:1–12. Based on the entirety of this evidence, we determine that despite some “heartache” in the process, a person of ordinary skill would be guided by knowledge in the prior art such that implementing Kim’s gate-stack-on-top ordering would be a predictable variation of Kim’s Figure 17A–22B embodiment for which a reasonable expectation of success exists.

Based on Dr. Campbell’s characterization of the knowledge in the art, the prior art presented by Petitioner, and Kim’s broad and unrestricted

statement that either ordering can be achieved in its formation processes, we determine that a person having ordinary skill in the art would have a reasonable expectation of success in applying Kim’s teaching to use either layer ordering.

b) Reliance on additional art and knowledge beyond Kim

Patent Owner argues that Petitioner improperly relies on prior art references such as Chen, Ohsaki, and Shin to provide support for certain limitations being obvious. PO Resp. 21 (citing “e.g., Pet. 38”). Patent Owner argues that Petitioner may not rely on those references to supply a limitation that Kim does not disclose. *Id.* at 22 (citing USPTO Memorandum, Enforcement and Non-Waiver of 37 C.F.R. § 42.104(b)(4) and Permissible Uses of General Knowledge in Inter Partes Reviews at 1 (July 31, 2025) (available at https://www.uspto.gov/sites/default/files/documents/aapa_memo_final__signed.pdf));⁶ *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337-38 (Fed. Cir. 2020) (general knowledge may only supply a missing claim limitation when “the missing limitation in question [is] *unusually simple* and the technology *particularly straightforward*.” (alterations in original, emphasis added)). Patent Owner argues that the technology claimed here is not unusually simple or particularly straightforward, because etch processes on a microscopic scale in device manufacturing are such that “each detail is important and can have significant effects.” PO Resp. 24, 26 (citing Ex. 2009 ¶¶ 41–42; Ex. 2008 (“details matter”)). Patent Owner further argues that the complexity of the

⁶ This Memorandum states, “[t]his Memorandum will apply to any petition for IPR filed on or after September 1, 2025.” Memorandum at 3. The Memorandum does not apply to this Petition, which was filed on November 12, 2024. *See* Pet. Reply 10.

technology is further evidenced by an alleged mistake in Petitioner's alteration of Kim that would render the lower gate insulating layer unnecessary by placing the insulating layer (rather than the gate stack) in the lowest step adjacent to it. *Id.* at 25. Patent Owner further argues that even if gate-stack-on-top ordering was known, a person of ordinary skill in the art would not have a reasonable expectation of success because of these complexities and the reduction of the number of protective layers over the gate stack that increases the risk of short-circuits from over-etching. *Id.* at 26 (citing Ex. 2008, 48:20–49:8; Ex. 2009 ¶ 41).

However, we agree with Petitioner that “there is no ‘missing limitation’ [because] Kim expressly discloses both orderings.” Pet. Reply 9 (citing Pet. 28, 32–33). Petitioner relies upon additional prior art documents to support its contention to “that either layer ordering was a well-known, suitable option.” *Id.* Here, such reliance on the knowledge in the prior art as a whole to support a reason to combine relevant prior art teachings to achieve the claimed invention is appropriate. *Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1362 (Fed. Cir. 2007).

Consequently, we determine that Petitioner has sufficiently shown each element of limitation [1.A] with sufficient reason to combine the teachings of Kim with a reasonable expectation of success.

[1.B] a barrier layer disposed over a portion of the gate stack of the each step; [1.C] an etch-stop layer disposed on the barrier layer; [1.D] an insulating layer disposed on the etch-stop layer; and [1.E] a plurality of conductive structures formed in the insulating layer, wherein each conductive structure is formed on the conductive layer of the each step.

We further determine that Petitioner has sufficiently shown Kim to teach a first stop layer 126a (barrier layer) disposed over a portion of the

gate stack of the each step, a second stop layer 126b (etch-stop layer) disposed on the barrier layer, and an interlayer insulating pattern 134 (insulating layer) disposed on the etch-stop layer. Pet. 41–44 (citing Ex. 1005, Fig. 22A, ¶¶ 94, 185–187, 193, 201, 213; Ex. 1003 ¶¶ 92–96). We also determine that Petitioner has shown Kim to teach a plurality of word line contact plugs (conductive structures) formed on the gate electrodes 161–166 (conductive layer) of the each step. *Id.* at 45–47 (citing Ex. 1005, Fig. 22, ¶¶ 173–74, 210–11, Ex. 1003 ¶ 97–99).

For the above-described reasons, we determine that Petitioner has met its burden to show, by a preponderance of the evidence, that claim 1 would have been obvious over Kim.

3. *Claims 13–15*

Claim 13 is similar to claim 1, but lacks the limitation of a barrier layer between gate stack and etch-stop layer, and instead states that the “etch-stop layer [is] disposed on a portion of the gate stack of the each step” of the staircase structure. Ex. 1001, 16:6–13. Petitioner asserts that although Kim describes a barrier layer between the etch-stop layer and the gate stack, the etch-stop layer is still “on” the gate stack because the term “on” as used in the ’711 patent permits intervening layers. Pet. 58 (citing Ex. 1001, 4:1–6). Patent Owner does not contest this interpretation for claim 13, or provide any separate argument for independent claim 13. PO Resp. 8–9. For the reasons described above with respect to claim 1, we determine that Petitioner has met its burden to show, by a preponderance of the evidence, that claim 13 would have been obvious over Kim.

The ’711 patent states, “‘on’ not only means ‘directly on’ something, but also includes the meaning of ‘on’ something with an intermediate feature or a layer therebetween.” Ex. 1001, 4:1–6. Based upon that definition, we

determine that Petitioner has sufficiently shown Kim to teach an etch-stop layer disposed on a portion of the gate stack. For reasons expressed in our discussion of the similar limitations of claim 1, we further determine that Petitioner has sufficiently shown Kim to teach the remaining limitations of claim 13.

Patent Owner separately argues against Petitioner's asserted unpatentability of claims 14 and 15. PO Resp. 28–30. Patent Owner argues that “on a surface” has a narrower meaning than “on”; i.e., “directly contacting” the surface of something. *Id.* at 29.

However, we have determined that such a construction of “on a surface” is unduly narrow because the '711 patent's express definition of “on” as permitting intervening layers is not limited by exemplary figures that show layers directly contacting a feature. *Supra* § II.C. The proper construction of “on a surface” permits an intervening barrier layer to be between an etch-stop layer and a surface of a step where the etch-stop layer is “formed on a side surface and a top surface of each step,” as recited in claim 14. *Id.* Consequently, we determine that Petitioner has sufficiently shown the additional limitations of claim 14. Because Petitioner also sufficiently shows the additional limitation of claim 15 that the thicknesses of the etch-stop layer is the same on the side and the top surfaces of each step, through Kim's description of its conformal layer as having “substantially the same thickness throughout,” we determine that Petitioner has sufficiently shown the additional limitations of claim 15. Pet. 61 (citing Ex. 1005 ¶ 144).

For the above-described reasons, we determine that Petitioner has met its burden to show, by a preponderance of the evidence, that claims 14 and 15 would have been obvious over Kim.

4. *Claims 2–9, 11–12, 16, 18, and 19*

Patent Owner does not specifically contest Petitioner’s showing for claims 2–9, 11–12, 16, 18, and 19. PO Resp. We have reviewed Petitioner’s showing for each of these claims and determine that it is supported by the cited evidence for the reasons expressed in the Petition. Pet. 47–57, 61–62.

With respect to claim 2, we determine that Petitioner’s assertion that in a gate-stack-on-top configuration, Kim teaches “that *the plurality of conductive structures* (‘WPLG[s]’) *extend[s] through the barrier layer* (‘first stop layer’” 126a) *and the high-k dielectric layer* (‘blocking insulating layer’ 150c)” is, for the reasons expressed in the Petition, supported by the evidence and teaches the limitations of claim 2 italicized therein. Pet. 47–48 (color omitted, alterations in original); Ex. 1005, Fig. 22A, ¶¶ 174, 187, 210–211.

With respect to claim 3, we determine that Petitioner’s assertion that in a gate-stack-on-top configuration, Kim teaches “that *the plurality of conductive structures* (‘WPLG[s]’) *extend[s] through etch-stop layer* (‘second stop layer’ 126b)” is, for the reasons expressed in the Petition, supported by the evidence and teaches the limitations of claim 3 italicized therein. Pet. 49 (color omitted); Ex. 1005, Fig. 22A, ¶ 187.

With respect to claim 4, we determine that Petitioner’s assertion that Kim teaches “that *the barrier layer* (‘first stop layer’ 125a/126a) *comprises silicon oxide*” is supported by the evidence and teaches the limitations of claim 4 italicized therein. Pet. 41 (descriptions of stop layers 125 apply to layers 126 (citing Ex. 1003 ¶ 92)), 50 (color omitted); Ex. 1005 ¶ 187.

With respect to claims 5 and 16, we determine that Petitioner’s assertion that Kim teaches “that *the etch-stop layer* (‘second stop layer’

125b/126b) *comprises . . . silicon nitride*” is supported by the evidence and teaches the limitations of claims 5 and 16 italicized therein. Pet. 41 (descriptions of stop layers 125 apply to layers 126 (citing Ex. 1003 ¶ 92)), 50 (color omitted), 61; Ex. 1005 ¶ 187.

With respect to claim 6, we determine that Petitioner’s assertion that in a gate-stack-on-top configuration, Kim teaches “that *the each conductive structure* (‘WPLG’) *directly contacts a corresponding one of the conductive layer* (corresponding one of ‘gate electrodes’ 161-166) *of the each step*” is supported by the evidence and teaches the limitations of claim 6 italicized therein. Pet. 50–51 (color omitted); Ex. 1005, Fig. 22A, ¶¶ 210–211.

With respect to claim 7, we determine that Petitioner’s assertion that in a gate-stack-on-top configuration, Kim teaches that “*top surfaces of the plurality of conductive structures* (‘WPLG[s]’), *the insulating layer* (‘interlayer insulating pattern’ 134), *and a portion of the etch-stop layer* (‘second stop layer’ 126b) *are coplanar*” is, for the reasons expressed in the Petition, supported by the evidence and teaches the limitations of claim 7 italicized therein. Pet. 52–53 (color omitted, alteration in original); Ex. 1005, Fig. 22A, ¶¶ 103, 193; Ex. 1003 ¶¶ 106–107.

With respect to claim 8, we determine that Petitioner’s assertion that in a gate-stack-on-top configuration, Kim teaches “that *the plurality of conductive structures* (‘WPLG[s]’) *comprise[s] . . . tungsten*” is supported by the evidence and teaches the limitations of claim 8 italicized therein. Pet. 53 (color omitted, alterations in original); Ex. 1005 ¶ 173. For reasons expressed in our determination that Kim’s gate-stack-on-top configuration would have been obvious to use in Kim’s Figure 22A embodiment (*supra* § II.D.2), we determine that Kim’s use of tungsten for its WPLG structures in

Figures 4 and 14 embodiment would have been obvious for its WPLG structures in its Figure 22A embodiment.

With respect to claim 9, we determine that Petitioner’s assertion that in a gate-stack-on-top configuration, Kim teaches “that *the barrier layer* (first stop layer’ 126a) *is formed on side and top surfaces of the plurality of steps*” is supported by the evidence and teaches the limitations of claim 9 italicized therein. Pet. 53–54 (color omitted); Ex. 1005, Fig. 22A, ¶¶ 144, 185, 187, 213.

With respect to claims 11 and 18, we determine that Petitioner’s assertion that in a gate-stack-on-top configuration, Kim teaches “that *the high-k dielectric layer* (‘blocking insulating layer’ 150c) *comprises hafnium oxide, zirconium oxide, aluminum oxide, [or] tantalum oxide*” is supported by the evidence and teaches the limitations of claims 11 and 18 italicized therein. Pet. 55 (color omitted, alteration in original), 61; Ex. 1005 ¶ 151.

With respect to claims 12 and 19, we determine that Petitioner’s assertion that in a gate-stack-on-top configuration, Kim teaches “that *top and bottom surfaces and a sidewall of the conductive layer* (‘gate electrodes’ 161-166) *are covered by the high-k dielectric layer* (blocking insulating layer’ 150c), *except at an interface between the conductive layer and the conductive structure* (corresponding ‘WPLG’)” is supported, for the reasons set forth in the Petition, by the evidence and teaches the limitations of claims 12 and 19 italicized therein. Pet. 55–57 (color omitted), 62; Ex. 1005, Fig. 22A, ¶¶ 200, 202, 210–211; Ex. 1003 ¶ 114.

For the above-described reasons, we determine that Petitioner has met its burden to show, by a preponderance of the evidence, that claims 2–9, 11–12, 16, 18, and 19 would have been obvious over Kim.

E. Obviousness over Kim and Fang

1. Fang

Fang is a U.S. patent application publication titled “Semiconductor Device Structures Comprising Carbon-Doped Silicon Nitride and Related Methods,” filed on August 24, 2017 and published on February 28, 2019. Ex. 1007, codes (22), (43), (54). Fang describes a nonvolatile memory device including a carbon-doped silicon nitride, excluding silicon carbon nitride, disposed over the tiers of a semiconductor device structure having alternating dielectric and conductive levels. *Id.* at code (57).

2. Analysis

Claims 10 and 17 depend from claims 1 and 13, and further recite that the thickness of the etch-stop layer is in a range between 10 nm and 1000 nm. Petitioner asserts that this range would have been obvious over Kim because the cited range is merely dimensional and does not result in differences of performance. Pet. 62 (citing *Gardner v. TEC Sys., Inc.*, 725 F.2d 1338, 1345–46 (Fed. Cir. 1984)). Petitioner points to the teaching of Fang of an etch-stop layer in an analogous semiconductor structure having a thickness of about 5 nm to 100 nm. Pet. 63. Petitioner asserts that it would have been obvious to have used a thickness in the claimed range as taught by Fang in the device of Kim, even accounting for Kim’s extra etch-stop layer and the height of Kim’s staircase structure. *Id.* at 63–64.

Patent Owner contests Petitioner’s asserted unpatentability of claims 10 and 17 based on the combined teachings of Kim and Fang, arguing that Petitioner provides insufficient reason to combine the teachings of Kim and Fang. PO Resp. 30–42. We have reviewed Petitioner’s assertions for these claims and determine that they are supported by the

record evidence for the reasons expressed in the Petition, including Petitioner's reasons to combine Kim and Fang. *See* Pet. 62–66.

Patent Owner first argues that Fang's thickness teachings are not applicable to Kim because Fang is directed towards carbon-doped silicon nitride, and Kim is directed only to undoped silicon nitride. PO Resp. 30–34; PO Sur-reply 14–15. Dr. Campbell attests that Fang's etch-stop is described as being made of any material that is not etched during removal of the nitride materials, which would exclude silicon nitride from use as the etch-stop material. Ex. 2009 ¶ 51 (citing Ex. 1008 ¶¶ 19–20). However, although Fang frequently discusses carbon-doped silicon nitride, Fang clearly states that the use of undoped silicon nitride as an etch-stop is also part of its invention. Ex. 1007 ¶ 8 (“In some embodiments, the etch-stop material is a silicon nitride material, *such as* a carbon-doped silicon nitride material.”) (emphasis added). Moreover, Fang's nitride materials are not limited to silicon nitride, but are more generally described as “nitride materials.” *Id.* ¶¶ 15, 19–20. Thus, Fang's description of its materials is not limited to silicon nitride on its stairs and carbon-doped silicon nitride on its etch layer. Similarly, Fang's description of its thicknesses is not limited to its carbon-doped silicon nitride embodiments. *Compare* Fang ¶ 21 (thicknesses of etch-stop materials), *with id.* ¶ 22 (“may be a carbon-doped silicon nitride”). Because Fang, like Kim, contemplates non-carbon-doped silicon nitride, Patent Owner's arguments based upon the differences between carbon-doped silicon nitride and undoped silicon nitride are unavailing.

Patent Owner next argues that the asserted combination of Kim and Fang is inappropriate because Fang is directed towards the problem of preventing punch-through in the word line contact region, whereas Kim is

directed towards the problem of preventing or reducing damage to the cell array region of the device from the polishing of contact pads during manufacturing. PO Resp. 37–38. However, obviousness does not require both references to address the same problem. *KSR*, 550 U.S. at 420 (“The . . . error of the Court of Appeals lay in its assumption that a person of ordinary skill attempting to solve a problem will be led only to those elements of prior art designed to solve the same problem.”). Instead, we agree with Petitioner that a person having ordinary skill in the art conversant with Kim, which lacks “certain aspects of the word line contact region,” would have looked to teachings such as Fang, which not only provide detail missing in Kim, but also provide processes to prevent problems that may arise in that region. Pet. 64–65 (citing Ex. 1005 ¶¶ 24–25, 27; Ex. 1007 ¶¶ 4, 8). Petitioner further points out that Fang’s focus “dovetails with Kim’s focus to reduce or prevent damages to the device during manufacturing.” *Id.* at 65 (citing Ex. 1005 ¶ 27).

Patent Owner next argues that Kim’s structural features would discourage such a combination with Fang. PO Resp. 38–41; PO Sur-reply 16–18. Patent Owner points to features such as Kim’s additional etch-stop layer and Kim’s additional high-k dielectric layer and its effect on the necessary etch processes. PO Resp. 33, 38–40 (citing Ex. 2009 ¶¶ 50, 55; Ex. 2008, 49:5–8). Patent Owner also points to differences in etch-stop thickness based on a gate-stack-on-top configuration, which would require changes in manufacturing and etch processes that have not been accounted for by Petitioner. *Id.* at 40–41 (citing Ex. 2009 ¶ 55).

The Petition explains how Fang’s range would be adjusted to the particular dimensions of Kim. Pet. 63 (“Fang’s disclosed thickness range may be adjusted based on Kim’s staircase structure.”). Despite Patent

Owner's emphasis on differences in etching based upon Kim's additional high-k layer, Dr. Campbell testified that the high-k dielectric layer does not serve as an etch-stop due to the intervening barrier layer. Ex. 1027, 56:2–14; Pet. Reply 17 (citing Ex. 2008, 48:2–19). Similarly, Dr. Banerjee attests that a second, lower etch-stop layer designed to stop the purposeful etching of an above etch-stop layer would not cause the thickness of the above etch-stop layer to be meaningfully altered, because the above etch-stop layer still performs the function of stopping the etching of the layer above it. Ex. 1028 ¶¶ 57–61.

Based upon the entirety of the record evidence, we determine that Petitioner has shown sufficient reason to combine the teachings of Kim and Fang. Consequently, we determine that Petitioner has met its burden to show, by a preponderance of the evidence, that claims 10 and 17 would have been obvious over Kim and Fang.

F. Obviousness over Park

Petitioner asserts that claims 1–6, 8, 9, 11–16, 18, and 19 would have been obvious over Park.

1. Park

Park is a published Korean patent titled “Nonvolatile memory device and manufacturing method thereof,” filed on November 5, 2013 and published on May 13, 2015. Ex. 1006, codes (22), (43), (54). Park describes a nonvolatile memory device including:

a channel region extending in a direction perpendicular to an upper surface of a substrate, a plurality of gate electrode layers disposed on the substrate so as to be adjacent to the channel region, a plurality of pad regions provided such that the plurality of gate electrode layers extends with different lengths along one direction, at least one etch-stop layer spaced apart from the plurality of gate electrode layers in the plurality of pad regions

and arranged on the plurality of gate electrode layers, and a plurality of contact plugs connected to the plurality of gate electrode layers.

Id. at code (57).

2. *Analysis of Claim 1*

We begin our analysis of Petitioner’s obviousness contentions with Petitioner’s assertions as to claim 1. Patent Owner contests Petitioner’s assertion that Park in view of the knowledge of the prior art teaches “wherein each step comprises a gate stack disposed over a dielectric layer,” PO Resp. 43–48. We first focus on this disputed limitation.

[1.PRE] A semiconductor structure, comprising: [1.A] a staircase structure comprising a plurality of steps, wherein each step comprises a gate stack disposed over a dielectric layer, the gate stack comprising a high-k dielectric layer and a conductive layer

To the extent the preamble [1.PRE] is limiting, Petitioner asserts that it is taught by Kim’s description of a 3D semiconductor device. Pet. 67 (citing Ex. 1006, code (57)). With respect to limitation [1.A], Petitioner asserts that Park Figure 9i illustrates a staircase structure having a plurality of steps. Pet. 30 (citing Ex. 1006 ¶ 102 (stating, “a portion of the top surface of each insulating layer (170) may be exposed by the plurality of pad regions (P1–P6)”), 66. Park Figure 9i is reproduced below:

FIG. 9i

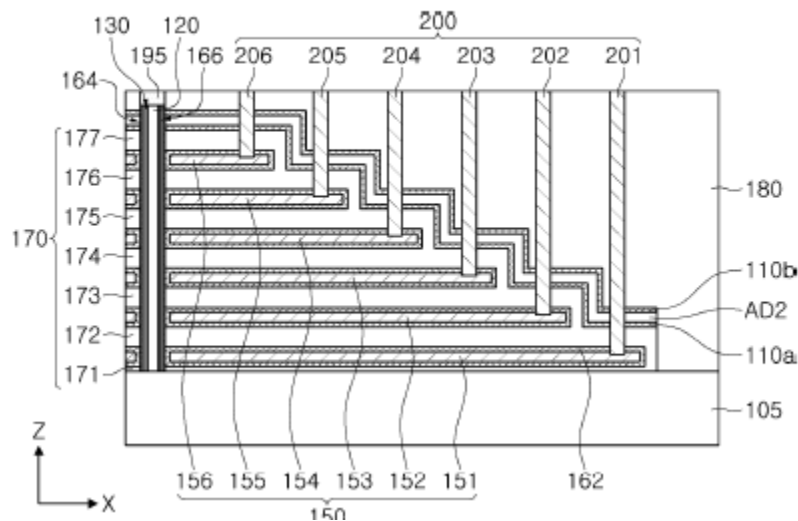
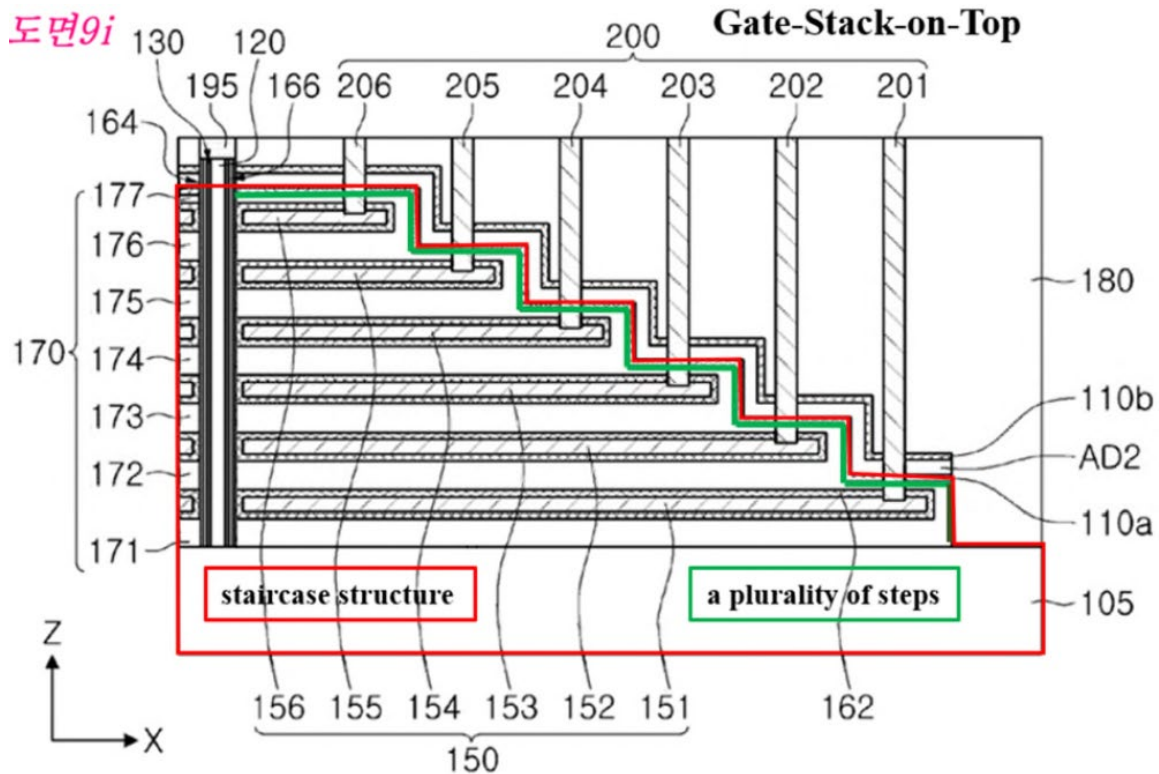


Figure 9i illustrates alternating gate electrode layers (150) and insulating layers (170) on a substrate (105), with etch-stop layers (110a, b) formed on the insulating layers. Ex. 1006 ¶ 103.

Petitioner asserts that Park teaches an alternate layer ordering in which sacrificial layers 140 lie atop insulating layers 170 at each step. Pet. 30–31 (citing Ex. 1006 ¶ 102 (stating, “unlike what is shown in FIG. 9a, a portion of the top surface of each sacrificial layer (140) may be exposed in a plurality of pad regions (P1–P6)”). Petitioner further asserts that Park’s sacrificial layers are replaced by a gate stack comprising a high-k dielectric layer (162) and a conductive layer (150). *Id.* at 30. Based on these descriptions, Petitioner provides an annotated version of Park’s Figure 9i that illustrates Petitioner’s characterization of Park’s gate-stack-on-top configuration:



Pet. 68.

Patent Owner argues that Petitioner provides no reason to combine different embodiments of Park to result in its proposed gate-stack-on-top configuration of altered Figure 9i. PO Resp. 44–47; PO Sur-reply 19–20. Patent Owner argues that Petitioner is relying on Park’s embodiment of Figures 4 and 8 to combine with the separate embodiment of Figures 5 and 9 for its gate-stack-on-top teachings. PO Resp. 45–47. Patent Owner argues that Park does not suggest combining those embodiments, despite Park’s explicit description that other features are common to different embodiments, and that extensive modification risking short-circuits from over-etching would be required to make such a change. *Id.*

However, Petitioner is not relying on a separate embodiment of Park, but the same Figure 9 embodiment. Pet. 30–31 (“unlike what is shown in FIG. 9a, a portion of the top surface of each sacrificial layer (140) may be

exposed in a plurality of pad regions (P1-P6).” (quoting Ex. 1006 ¶ 102)); Pet. Reply 19–20. We agree with Petitioner that Park’s description that the sacrificial layers 140 may be exposed in the pad region relates to its Figure 9 embodiment, not the Figure 8 embodiment. Ex. 1006 ¶ 102. Moreover, in Park’s Figure 5 embodiment, “the plurality of pad regions are the same as FIG. 4.” *Id.* ¶ 49. Dr. Banerjee testifies that the only difference between the Figures 4/8 embodiment and the Figures 5/9 embodiment is the number of etch-stop layers. Ex. 1028 ¶ 73. Thus, even if Petitioner relied upon Park’s Figure 4 pad regions, those would be the same as in Figure 5, and consequently in Figure 9, because it is the method of making the device of Figure 5. Ex. 1006 ¶ 100.

Patent Owner further disputes the structure that would result from Park’s statement regarding Figure 9. PO Resp. 44. Patent Owner argues that Park’s alternative is not a structure having only the gate stack over the insulating layer, but instead, a structure having both the insulating and gate layers exposed. *Id.* (citing Ex. 2009 ¶ 58; Ex. 1005, Fig. 9b). Dr. Campbell states that “[t]his could occur, for example, if the etch process is alternated between sacrificial and oxide layers.” Ex. 2009 ¶ 58. Patent Owner states that this describes “the process of ‘etch[ing] to provide a plurality of pad regions (P1-P6)’ and what occurs during the processing of the staircase structure.” PO Sur-reply 19 (alteration in original).

However, Patent Owner’s proposed structure is not consistent with that described by Park. There is no description in Park of a resulting structure having both insulating and gate layers being exposed in the manner proposed by Patent Owner. Instead, Park’s Figure 9a embodiment describes exposure of “a portion” of the insulating layer, and “unlike” Figure 9a, an alternate arrangement exposes “a portion” of the sacrificial layer. Ex. 1006

¶ 102. Further, Park describes that the ordering of insulating and gate electrode layers may be reversed. Park describes that in the pad regions of Figure 4, “the insulating layer (170) is depicted as being positioned above the gate electrode layer (150) along the z-axis direction in each pad region, but conversely, the gate electrode layer (150) may be positioned above the insulating layer (170).” *Id.* ¶ 42. Although Petitioner relies on the method of Figure 9, which results in the structure of Figure 5, the pad structure of Figure 5 is “the same as” the pad structure of Figure 4. *Id.* ¶ 49. Thus, Petitioner’s interpretation of Park’s description in paragraph 102 as reflecting a reversed layer order has significant support within Park, whereas Patent Owner’s interpretation as reflecting an exposure of both layers has little, if any.

We further credit Dr. Banerjee’s testimony that he could not “visualize such a staircase [having both insulating and gate layer exposed] in a practical implementation.” Ex. 1028 ¶ 66. Dr. Banerjee also attests that Figure 9b does not show exposed sacrificial layers. *Id.* ¶ 67. As to Dr. Campbell’s explanation that Park’s paragraph 102 refers to alternating the etch process between sacrificial and oxide layers, Dr. Banerjee characterized this as “nonsensical because the etch process is already alternated between the two layers in Figure 9a.” *Id.* ¶ 66.

In view of the totality of the record, we determine that Petitioner has sufficiently shown that a person having ordinary skill in the art would have understood Park to teach a variant of its Figure 9i in which the gate stack layer lies atop the insulating layer.

Patent Owner also argues that Petitioner has not shown how or why a person having ordinary skill in the art could have performed a gate-stack-on-top modification with a reasonable expectation of success. PO Resp. 47.

Dr. Campbell testifies that such a change necessitates modifying the word contacts, which requires fundamental changes to the manufacturing process. Ex. 2009 ¶¶ 64–65. Dr. Campbell further testifies that such a change reduces the number of protective layers over the gate stack, increasing the risk of short-circuits from over-etching. *Id.* ¶ 83.

However, as discussed above, the question is whether a person having ordinary skill would have a reasonable expectation of success, not whether such an undertaking would require changes to the design and manufacturing processes. *Supra* § II.D.2.a. Based on Dr. Campbell’s characterization of the knowledge in the art, the prior art presented by Petitioner, and Park’s statements that either ordering can be used, we determine that a person having ordinary skill in the art would have had a reasonable expectation of success in applying Park’s teaching to use either layer ordering. *Id.*

Patent Owner also argues that Petitioner relies improperly on art not included in its obviousness combination and the knowledge of a person of ordinary skill in the art to fill for the missing limitation of a gate stack on top. PO Resp. 47 (citing Patent Owner’s Kim-based assertions). For the same reasons we did not agree with such arguments pertaining to Kim, we do not agree with such arguments pertaining to Park. *Supra* § II.D.2.b. As discussed, like Kim, Park does not have a missing limitation of the gate stack over a dielectric layer because that teaching is found in Park itself.

[1.B] a barrier layer disposed over a portion of the gate stack of the each step; [1.C] an etch-stop layer disposed on the barrier layer; [1.D] an insulating layer disposed on the etch-stop layer; and [1.E] a plurality of conductive structures formed in the insulating layer,

wherein each conductive structure is formed on the conductive layer of the each step.

We further determine that Petitioner has sufficiently shown Park to teach a first etch-stop layer 110a (barrier layer) disposed over a portion of the gate stack of the each step, a second stop layer 110b (etch-stop layer) disposed on the barrier layer, and an insulating layer 180 (insulating layer) disposed on the etch-stop layer. Pet. 73–76 (citing Ex. 1006, Fig. 9i, ¶¶ 46, 49, 51, 63, 124; Ex. 1003 ¶¶ 148–152). We also determine that Petitioner has shown Park to teach a plurality of contact plugs (conductive structures) formed in the insulating layer 180 and on the on the gate electrodes 151–156 (conductive layer) of the each step. *Id.* at 76–78 (citing Ex. 1006, Fig. 9i, ¶¶ 43, 45, 49, 50, 108–110; Ex. 1003 ¶ 153–154).

For the above-described reasons, we determine that Petitioner has met its burden to show, by a preponderance of the evidence, that claim 1 would have been obvious over Park.

3. Claims 13–15

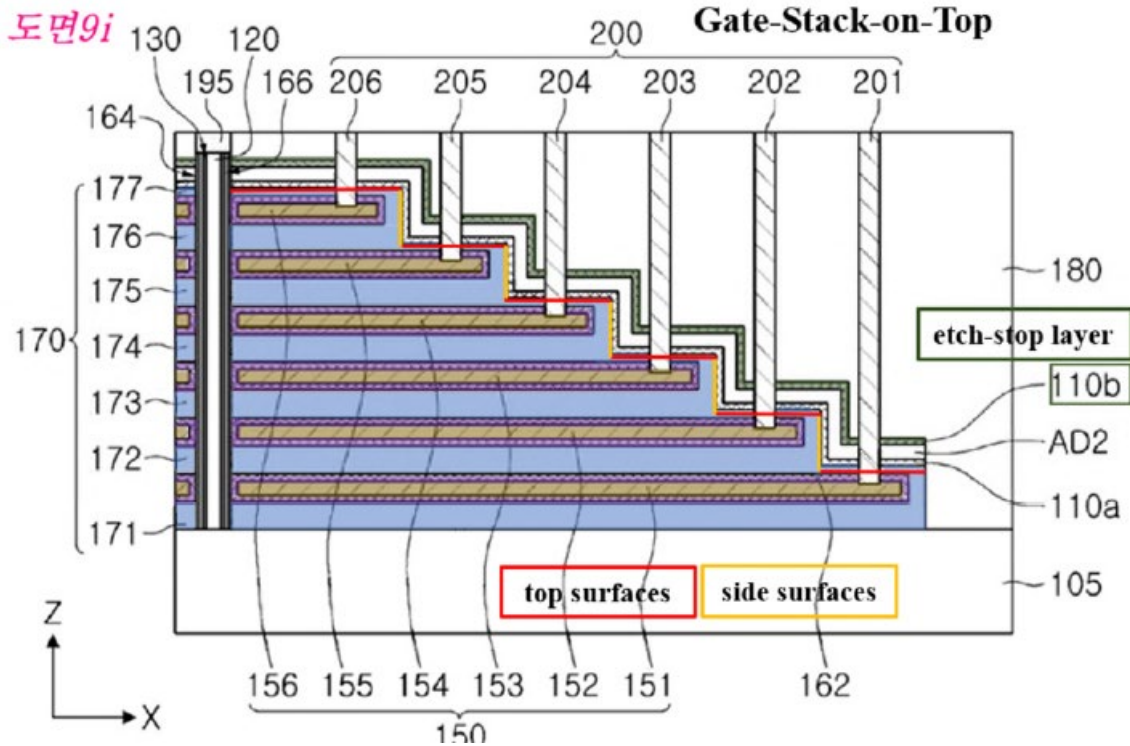
Claim 13 is similar to claim 1, but lacks the limitation of a barrier layer between gate stack and etch-stop layer, and instead states that the “etch-stop layer [is] disposed on a portion of the gate stack of the each step” of the staircase structure. Ex. 1001, 16:6–13. Petitioner asserts that Park teaches claim 13 in the same manner as claim 1; i.e., through etch-stop layer 110b above the gate stack (relying on Park for teaching that the insulating and gate stack layers may be reversed). Pet. 87. As in its Kim-based assertions, Petitioner asserts that the presence of intermediate layers (such as layer 110a) does not affect Park’s teaching that the etch-stop layer is “on” the gate stack. *Id.* (citing Ex. 1001, 4:1–6).

Patent Owner does not provide reasons to contest Petitioner's assertions for claim 13 separate from those argued against claim 1. *See* PO Resp. 28. Because we determined those reasons to be unavailing, we determine that Petitioner has met its burden to show, by a preponderance of the evidence, that claim 13 would have been obvious over Park.

Claim 14 depends from claim 13, and further recites that the etch-stop layer is formed on a side surface and a top surface of each step. Patent Owner argues that Park does not teach this because Park has an intervening layer between etch-stop layer and the top surface of the step. PO Resp. 50–51. However, we determined that such a construction is incorrect, and that claim 14 permits an intervening layer. *Supra* § II.C.

Patent Owner also argues that Petitioner does not show that Park's etch-stop layer is on "each" step. PO Resp. 49–50 (citing Ex. 1006, Figs. 4–6). Specifically, Patent Owner points to the bottom step (171, 151, 172) that has no etch-stop layer 110a or 110b on its right periphery. *Id.* Petitioner cites the '711 patent's statement that "[i]n the present disclosure, the term 'each' may not only necessarily mean 'each of all,' but can also mean 'each of a subset,'" and that the term "comprising" in claim 14 is open-ended. Pet. Reply 22–23 (quoting Ex. 1001, 5:6–8). Patent Owner responds by arguing that Petitioner has not provided any reason why the claim includes all stairs except the bottom stair. PO Sur-reply 21.

In the Petition, Park's bottom step is included as a claimed "each step" of independent claim 13. Pet. 87 (annotated Park Fig. 9i). Although Petitioner labels Park's bottom step as having a top surface, Petitioner does not label Park's bottom step as having a side surface in its discussion of claim 14:



Annotated Park Figure 9i, labeled “Gate-Stack-on-Top,” illustrates a staircase of insulating layers 170 and gate layers 150 having top surfaces highlighted in red for each step and side surfaces highlighted in yellow for each step except the bottom step. Pet. 89.

Because the Petition includes Park’s bottom step as a claimed “each step,” but does not show how Park teaches a side surface of the bottom step having an etch-stop layer thereon, the Petition does not show that it would have been obvious to have formed an etch-stop layer on a side surface of each step as required by claim 14 and, through dependency, claim 15. We do not consider Petitioner’s newly provided explanation that the ’711 patent defines “each” step as a “subset of each” step, or that the “comprising” preamble permits claim 14 to be met by a teaching of by less than all steps of the staircase. Pet. Reply 22–23 (citing Ex. 1001, 5:6–8); *see* PTAB Consolidated Trial Practice Guide § II.I (Dec. 2025) (“Petitioner may not submit new evidence or argument in reply that it could have presented

earlier, e.g., to make out a prima facie case of unpatentability.”). Although Petitioner at oral argument pointed to use of “comprising” at page 71 of its Petition, that instance was in reference to whether Park teaches a “plurality of steps” regardless of its steps potentially having a gate stack and dielectric layer of different widths. Tr. 71:1–13; Pet. 70–71. The Petition did not argue that the presence of “comprising” altered the “each step” requirement, but instead illustrated its point with an annotated version of Park’s Figure 9i highlighting each step, including the lowest step that lacked an etch-stop layer on its side surface, with a green outer border labeled “a plurality of steps.” Pet. 70. The Petition expressly indicated that all steps of Figure 9i were considered part of the “each step” and Petitioner’s later explanations conflict with that reasoning set forth in the Petition. Thus, either explanation amounts to a new theory of obviousness that was not present in the Petition.

Consequently, Petitioner has not shown, by a preponderance of the evidence, that claims 14 and 15 would have been obvious over Park.

4. *Claims 2–6, 8, 9, 11, 12, 16, 18, and 19*

Patent Owner does not specifically contest Petitioner’s showing for claims 2–6, 8, 9, 11–12, 16, 18, and 19. *See* PO Resp. 43–55. We have reviewed Petitioner’s showing for each of these claims and determine that it is supported by the cited evidence for the reasons expressed in the Petition. Pet. 78–86, 90–91.

With respect to claim 2, we determine that Petitioner’s assertion that in a gate-stack-on-top configuration, Park teaches “that *the plurality of conductive structures* (‘contact plugs’ 201-206) *extend[s] through the barrier layer* (‘etch-stop layer’ 110a) *and the high-k dielectric layer* (‘blocking layer’ 162)” is, for the reasons expressed in the Petition, supported by the evidence and teaches the limitations of claim 2 italicized

therein. Pet. 78 (color omitted, alteration in original); Ex. 1006, Fig. 9i, ¶¶ 49–50, 56, 110, 125; Ex. 1003 ¶¶ 155–56.

With respect to claim 3, we determine that Petitioner’s assertion that in a gate-stack-on-top configuration, Park teaches “*the plurality of conductive structures* (‘contact plugs’ 201-206) *extend[s] through etch-stop layer* (‘etch-stop layer’ 110b)” is, for the reasons expressed in the Petition, supported by the evidence and teaches the limitations of claim 3 italicized therein. Pet. 79–80 (color omitted, alteration in original); Ex. 1006, Fig. 9i, ¶¶ 49–50, 56, 110, 125; Ex. 1003 ¶ 157.

With respect to claim 4, we determine that Petitioner’s assertion that Park teaches “that *the barrier layer* (‘etch stop layer’ 110a) *comprises silicon oxide*” is, for the reasons expressed in the Petition, supported by the evidence and teaches the limitations of claim 4 italicized therein. Pet. 80 (color omitted, alteration in original); Ex. 1006 ¶¶ 63, 105.

With respect to claims 5 and 16, we determine that Petitioner’s assertion that Park teaches “that *the etch-stop layer* (‘etch stop layer’ 110b) *comprises one or more of silicon nitride . . . and a high-k dielectric*” is, for the reasons expressed in the Petition, supported by the evidence and teaches the limitations of claims 5 and 16 italicized therein. Pet. 80 (color omitted, alteration in original), 90; Ex. 1006 ¶¶ 63, 105.

With respect to claim 6, we determine that Petitioner’s assertion that in a gate-stack-on-top configuration, Park teaches “that *the each conductive structure* (one of ‘contact plugs’ 201-206) *directly contacts a corresponding one of the conductive layer* (corresponding one of ‘gate electrode layers’ 151-156) *of the each step*” is supported by the evidence and teaches the limitations of claim 6 italicized therein. Pet. 81 (color omitted); Ex. 1006, Fig. 9i, ¶¶ 49–50, 110.

With respect to claim 8, we determine that Petitioner’s assertion that in a gate-stack-on-top configuration, Park teaches “that *the plurality of conductive structures* (“contact plugs” 201-206) *comprise[s] . . . tungsten*” is supported by the evidence and teaches the limitations of claim 8 italicized therein. Pet. 82 (color omitted, alterations in original); Ex. 1006 ¶¶ 99, 110.

With respect to claim 9, we determine that Petitioner’s assertion that in a gate-stack-on-top configuration, Park teaches “that *the barrier layer* (‘etch stop layer’ 126a) *is formed on side and top surfaces of the plurality of steps*” is supported by the evidence and teaches the limitations of claim 9 italicized therein. Pet. 82–83 (color omitted); Ex. 1006, Fig. 9i, ¶ 49.

With respect to claims 11 and 18, we determine that Petitioner’s assertion that in a gate-stack-on-top configuration, Park teaches “that *the high-k dielectric layer* (‘blocking layer’ 162) *comprises hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, [or] lanthanum oxide*” is supported by the evidence and teaches the limitations of claims 11 and 18 italicized therein. Pet. 83–84 (color omitted, alteration in original), 90; Ex. 1006 ¶ 63.

With respect to claims 12 and 19, we determine that Petitioner’s assertion that in a gate-stack-on-top configuration, Park teaches “*top and bottom surfaces and a sidewall of the conductive layer* (one of ‘gate electrode layers’ 151-156) *are covered by the high-k dielectric layer* (‘blocking layer’ 162), *except at an interface between the conductive layer and the conductive structure* (corresponding one of ‘contact plugs’ 201–206)” is supported, for the reasons set forth in the Petition, by the evidence and teaches the limitations of claims 12 and 19 italicized therein. Pet. 84–86 (color omitted), 90–91; Ex. 1006, Fig. 9i, ¶¶ 60, 105; Ex. 1003 ¶ 165.

For the above-described reasons, we determine that Petitioner has met its burden to show, by a preponderance of the evidence, that claims 2–6, 8, 9, 11–12, 16, 18, and 19 would have been obvious over Park.

G. Obviousness over Park and Fang

Petitioner asserts that claims 7, 10, 15, and 17 would have been obvious over Park in view of Fang. Pet. 91–103. Patent Owner argues that Petitioner has not shown that a person having ordinary skill in the art would have combined the teachings of Park and Fang, and that such a person would not have had a reasonable expectation of success in doing so. PO Resp. 55–71.

1. Analysis of Claim 7

We begin our analysis of Petitioner’s obviousness contentions with Petitioner’s assertions as to claim 7. Claim 7 depends from claim 1, and further recites, “wherein top surfaces of the plurality of conductive structures, the insulating layer, and a portion of the etch-stop layer are coplanar.” Ex. 1001, 15:27–29. Petitioner relies upon Fang for teaching a planarization process to equalize the heights of the top surfaces of its contacts 155a–d, its insulating layer 135, and a portion of its etch-stop material 130. Pet. 91–92 (citing Ex. 1007, Fig. 6, ¶ 24; Ex. 1003 ¶ 182). Petitioner points to Park’s use of a planarization process to equalize the heights of its channel-containing cell-array region and its staircase-containing connection region, although not its etch-stop layer. *Id.* at 92–94 (citing Ex. 1006, Fig. 5, ¶¶ 84, 89, 103). Petitioner asserts that it would have been obvious to have a portion of Park’s etch-stop layer being coplanar with its conductive layer and its insulating layer because the materials above the top surface of the etch–stop layer 110 “are ‘unnecessary’ and may be removed.” *Id.* at 94–95 (citing Ex. 1006 ¶ 89). If so modified, Petitioner

asserts that both Park and Fang would have select lines/access lines at the same vertical height as its contacts. *Id.* at 96–97 (citing Ex. 1007 ¶¶ 26, 40; Ex. 1003 ¶ 186). Petitioner asserts that “applying Fang’s coplanar configuration on Park’s device represents nothing more than applying a known technique and a suitable option on a similar device.” *Id.* at 98. Petitioner also describes the removal of materials above the top-surface plane as a choice between available options of partial or complete removal. *Id.* at 102–103 (citing Ex. 1003 ¶ 202). Petitioner further asserts that Fang’s configuration desirably reduces the device size by merely extending Park’s existing planarization process to remove a greater thickness as guided by Fang. *Id.* at 103 (citing Ex. 1003 ¶¶ 202-03).

Petitioner also provides a broader statement of the reasons to combine the teachings of Park and Fang that is applicable to claims 7, 10, 15, and 17. Pet. 100. Petitioner asserts that both Park and Fang seek the same goal of improving reliability of a highly integrated 3D memory device by reducing processing, complexity, and cost of the manufacturing process, and to reducing defects resulting from over-etching openings for wordline conductive structures. *Id.* at 100–101 (citing Ex. 1006 ¶¶ 3, 14; Ex. 1007 ¶ 4). Petitioner points to other similarities between Park and Fang, including selectivity of a silicon nitride etch-stop layer, and asserts that Fang provides specific details for manufacturing process parameters not otherwise specified in Park, which would be useful for a more complete combined teaching. *Id.* at 101 (citing Ex. 1003 ¶ 197; Ex. 1007 ¶ 9).

Patent Owner argues that Park and Fang have important differences in materials and designs that would frustrate the manufacturing process. PO Resp. 55 (citing Ex. 2009 ¶¶ 71–89). Patent Owner argues that Park’s

planarization occurs on a sacrificial etch-stop layer 115b and not on its replacement, etch-stop layer 110. PO Resp. 61–62 (citing Ex. 1006 ¶¶ 89–92, 105–106; Ex. 2009 ¶ 80). Patent Owner argues that Fang deposits its etch-stop layer directly on the staircase structure whereas Park uses a multi-step process that interposes an insulating layer between the etch-stop and staircase, with the etch-stop material originally being a sacrificial etch-stop material 115 replaced by a final etch-stop material 110. *Id.* at 55–61 (citing Ex. 2009 ¶¶ 73–76; Ex. 1006 ¶¶ 49, 82–92, 103–106; Ex. 1007 ¶ 20, Fig. 2). Patent Owner argues that merely extending Park’s existing planarization step would remove material needed for etch-stop layer formation; i.e., the “T2 ceiling” for T2 openings yet to be filled with etch-stop material. *Id.* at 62–63 (citing Ex. 1006 ¶¶ 89–90, 104, Figs. 9e–9g; Ex. 2009 ¶¶ 79–80).

However, the Petition asserts that the combination would be to “modify Park’s planarization process such that” a portion of “‘etch-stop layer’ 110b” is coplanar with the other top surfaces. Pet. 94. The Petition modifies the planarization “[i]n view of Fang” to act on the etch-stop layer 110, not the sacrificial etch-stop layer 115. Pet. 93 (reproducing Park’s Figure 5 containing layers 110a and 110b), 94–95 (reproducing Park’s Figure 9j containing layers 110a and 110b). Although the Petition also mentions that Park is to be modified by “removing a greater thickness” during its planarization process, the Petitioner’s focus on etch-stop layer 110 rather than sacrificial etch-stop layer 115 indicates that the modification includes the point at which the planarization is to be performed; i.e., at a point when etch-stop layer 110 exists. Although Patent Owner argues that the Petition did not assert that planarization should be performed after the formation of etch-stop layer 110, the above portions of the Petition clearly

present this assertion, and therefore Petitioner's later assertions and evidence regarding planarization of etch-stop layer 110 were not newly introduced.

Finally, Patent Owner argues that even if planarization were performed after Park's etch-stop layer 110 is formed, the necessary chemical polishing to do so would risk damaging Park's channel structure 130 and conductive layer 195. *Id.* at 63–64 (citing Ex. 2009 ¶ 81; Ex. 1005 ¶ 105). Patent Owner further argues that such risk of damage indicates a lack of a reasonable expectation of success in the combination. *Id.* at 64–65.

The weight of the evidence supports Petitioner. Petitioner presents evidence in the prior art of successive chemical mechanical polishing actions that result in protruding elements above a planarized surface. Pet. Reply 25–26 (citing Ex. 1030, Figs. 1D–1E, ¶¶ 18–19). Petitioner and Dr. Banerjee point to Park as suggesting two such polishing steps, before and after forming the conductive layer. *Id.* at 26 (citing Ex. 1006 ¶¶ 89, 110, Fig. 9j); Ex. 1028 ¶ 79 (quoting Ex. 1006 ¶ 89 “Next, a planarization process can be performed . . . and a material that constitutes a conductive layer (195) can be deposited . . . **Again**, a planarization process may be performed . . .”). Although Patent Owner characterizes the word “Again” as “more of a summary of this paragraph rather than a second step,” the text of Park describes the second-mentioned process as following a deposition of the conductive layer after the first planarization process. Tr. 73:22–74:3; Ex. 1006 ¶ 89. Park's description of planarization following conductive layer deposition directly contradicts Patent Owner's main argument that such polishing would not have been obvious because it would damage a conductive layer. PO Resp. 63–64. Dr. Banerjee further testifies that it is routine to protect vulnerable elements during such polishing processes. Ex. 1028 ¶¶ 78–81. Based on the evidence, we determine that Petitioner has

shown sufficient reason to combine the teachings of Park and Fang as asserted with respect to claim 7.

Consequently, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 7 would have been obvious over the combination of Park and Fang.

2. *Analysis of Claims 10 and 17*

Claim 10 depends from claim 1, and further recites, “wherein a thickness of the etch-stop layer is in a range between 10 nm and 1000 nm.” Ex. 1001, 15:35–37. Claim 17 depends from claim 13 and recites an identical limitation. *Id.* at 16:29–31. Petitioner’s Park and Fang assertions mirror its assertions for Kim and Fang; i.e., that the thickness does not result in performance differences and that Fang’s range overlaps with the claimed range, even accounting for the extra etch-stop layer of the primary reference (here, Park). Pet. 97–98.

Patent Owner argues that “Petitioner fails to establish a motivation to combine the Park and Fang references for at least the same reasons it fails as to the Kim and Fang combination.” PO Resp. 65–69 (citing to its Kim and Fang discussion of, *inter alia*, Fang’s use of carbon-doped silicon nitride rather than Park’s silicon nitride, Park’s additional etch-stop layer, Park’s additional high-k dielectric layer and its effect on the necessary etch processes, and differences in etch-stop thickness based on Park’s gate-stack-on-top configuration rather than Fang’s gate-stack-on-bottom configuration). Patent Owner also argues that there would be no reasonable expectation of success in such a combination for the same reasons as advanced against Petitioner’s combination of Kim and Fang. *Id.* at 69.

Patent Owner’s arguments are unavailing for the reasons expressed above with respect to Petitioner’s Kim and Fang combination. *Supra* § II.E.

Additionally, Petitioner points to Park’s description that the etch-stop layer thickness is “less than or equal to two times the thickness of the gate insulating films,” and Dr. Campbell’s testimony that the gate insulating films are 5–15 nm thick. Pet. Reply 27 (citing Ex. 1027, 100:21–101:2). Petitioner argues that combining these statements yields a thickness of 10–30 nm, within Fang’s described range, which further illustrates that Fang’s range is applicable to Park. *Id.*

Consequently, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 10 and 17 would have been obvious over the combination of Park and Fang.

3. *Analysis of Claim 15*

Claim 15 depends from claim 14, and further recites, “wherein thicknesses of the etch-stop layer is the same on the side and top surfaces of each step.” Ex. 1001, 16:23–25. Petitioner relies on Fang’s teaching that “[t]he thickness of the etch stop material 130 on the stairs 125 may be substantially uniform.” Pet. 99 (citing Ex. 1007 ¶ 21). Petitioner asserts that such a uniform thickness of an etch-stop layer would have been recognized by a person having ordinary skill in the art as being desirable, and “consistent with Park’s repeated references to “*the* thickness of the etch-stop layer.” *Id.* at 100 (citing Ex. 1006 ¶¶ 6, 60, 67, 70, 71; Ex. 1003 ¶ 194), 90 (citing Ex. 1017 ¶ 42).

Patent Owner cites to its arguments for Petitioner’s assertions for claims 10 and 17 as a reason why a person having ordinary skill in the art would not find motivation to combine Fang’s teachings with those of Park with a reasonable expectation of success. PO Resp. 70. However, we find those assertions unavailing for the same reasons discussed above with respect to claims 10 and 17.

Patent Owner argues that Petitioner only explains why uniform thickness between each top surface is desirable; i.e., to achieve a uniform contact-hole depth, but that this does not explain why uniformity between top and side surfaces is desirable. PO Resp. 71. Patent Owner argues that etch rates between top and sides may differ, and that Park's method would be costly to achieve uniformity due to its a long, serpentine cavity that must be filled with etch-stop material. *Id.* (citing Ex. 2009 ¶ 87).

Based on the record, we find that Petitioner has sufficiently shown that it would have been obvious to have a uniform etch-stop thickness on the side and top surfaces. Because Park describes "the" thickness of its etch-stop material, Fang specifies that its etch-stop thickness may be substantially uniform, and Petitioner explains that such uniform thickness is desirable at least at the top surfaces, the use of a uniform thickness over the entire layer would have been obvious to a person having ordinary skill in the art.

Patent Owner further argues that that claim 15 suffers the same deficiency as claim 14 in that Petitioner has not shown "each step," including the lower step, to have a side surface with an etch-stop layer thereon. PO Resp. 70. The Petition asserts that the teachings of Park and Fang make desirable "an etch-stop layer of uniform thickness on all steps." Pet. 100. As discussed *supra*, the Petition included all steps in its "each step" teachings of Park. *Supra* § II.F.3. Although Petitioner did not show how Park teaches an etch-stop layer on the side surface, Petitioner is clearly asserting that the combination with Fang teaches this. In its description of Fang, Petitioner relies on an illustration of Fang in which the etch-stop layer covers the top and side surfaces of all shown steps:

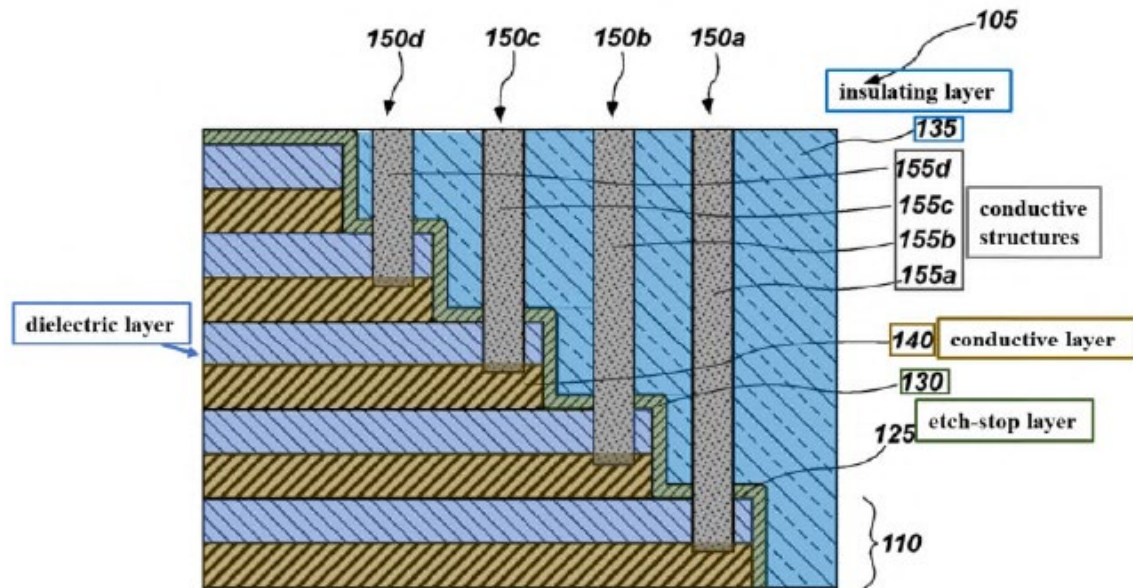


FIG. 6

Pet. 32 (annotated Fig. 6 of Fang). Annotated Figure 6 of Fang shows alternating steps of dielectric and conductive layers having etch-stop layer 130 on the top and sides of each step. Petitioner explains, with sufficient evidentiary support, how the combination of Park and Fang makes obvious an etch-stop layer on each step. Although we have determined that Park alone does not teach the limitations of claim 14, from which claim 15 depends, Fang provides the sole limitation that we found lacking. Because Petitioner relies on Fang for its uniform thickness of its etch-stop layer on side and top surface of each step, Petitioner has shown the combination of Park and Fang to also teach claim 14's "etch-stop layer is formed on a side surface and a top surface of each step" that is incorporated into claim 15.

Consequently, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 15 would have been obvious over the combination of Park and Fang.⁷

III. CONCLUSION⁸

After reviewing the record and weighing the evidence offered by both parties, we determine that Petitioner shows by a preponderance of the evidence that claims 1–19 are unpatentable.

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–9, 11– 16, 18, 19	103	Kim	1–9, 11–16, 18, 19	
10, 17	103	Kim, Fang	10, 17	
1–6, 8, 9, 11–16, 18, 19	103	Park	1–6, 8, 9, 11– 13, 16, 18, 19	14–15
7, 10, 15, 17	103	Park, Fang	7, 10, 15, 17	
Overall Outcome			1–19	

⁷ Because Petitioner has not asserted that claim 14 is obvious over the combination of Park and Fang, we do not make any determination specific to claim 14 on such a combination.

⁸ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

IV. ORDER

For the foregoing reasons, it is:

ORDERED that Petitioner has established by a preponderance of the evidence that claims 1–19 are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2025-00117
Patent 10,672,711 B2

For PETITIONER:

Jeremy Lang
Travis Jensen
Johannes Hsu
ORRICK, HERRINGTON & SUTCLIFFE LLP
ptabdocketjjl2@orrick.com
t61ptabdocket@orrick.com
ptabdocketjh1@orrick.com

For PATENT OWNER:

Inge Osman
Brenda Danek
Steven Peters
Amit Makker
Charles Sanders
Brent Watson
Alex Grabowski
Richard Lowry
Adam Greenfield
LATHAM & WATKINS LLP
inge.osman@lw.com
brenda.danek@lw.com
speters@cgsh.com
amit.makker@lw.com
charles.sanders@lw.com
thomas.watson@lw.com
alex.grabowski@lw.com
richard.lowry@lw.com
adam.greenfield@lw.com