Doc Code: ECOMM.AUTH/ECOMM.WTDW
Doc Description: Internet Communications Authorized/Internet Communications Authorization Withdrawn

PTO/SB/439 (11-15)

AUTHORIZATION FOR INTERNET COMMUNICATIONS IN A PATENT APPLICATION OR REQUEST TO WITHDRAW AUTHORIZATION FOR INTERNET COMMUNICATIONS		
	Application No.	N/A
	Filing Date	N/A
	First Named Inventor	Zhiguo Li
	Art Unit	N/A
	Examiner Name	N/A
	Practitioner Docket No.	YMTP0079USA3

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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II. To withdraw authorization for Internet Communications.

☐ The authorization given on _____, to the USPTO to communicate with the undersigned and any practitioner in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via Internet communications such as video conferencing, instant messaging, or electronic mail is hereby withdrawn. I understand that the withdrawal is effective when approved rather than when received.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 67314.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Roger Chen/	11/28/2018
Signature	Date
Roger Chen	3027291562
Typed or printed name	Telephone Number

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Atty. Docket No. YMTP0079USA3

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DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

☒ The attached application, or

☐ United States application or PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is Room 7018, No.18, Huaguang Boulevard, Guandong Tech. Industrial Park, Donghu Development Area, Hongshan District, Wuhan City, Hubei Province, P.R.C. (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **Integrated Circuit Electrostatic Discharge Bus Structure and Related Method** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial

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property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 27765** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

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IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: Zhiguo Li Date: 2018.9.6

Signature of Inventor: Zhiguo Li

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Doc Code: PA..
Document Description: Power of Attorney

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Application Number	N/A
Filing Date	N/A
First Named Inventor	Zhiguo Li
Title	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	YMTP0079USA3

SIGNATURE of Applicant or Patent Practitioner

Signature	/Roger Chen/	Date (Optional)	11/28/2018
Name	Roger Chen	Registration Number	67314
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

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hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or he boxes below.

Application Number	Filing Date

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☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 27765

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. [Note: Complete form PTO/AIA/82C.)

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OR

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Telephone		Email			

am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Simon	Date (Optional)	AUG 21 2018
Name	SIMON SHI-NING YANG		
Title	CEO		

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Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method
First Named Inventor/Applicant Name:	Zhiguo Li
Filer:	Winston Hsu/Vickie Lee
Attorney Docket Number:	YMTP0079USA3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
INDEPENDENT CLAIMS IN EXCESS OF 3	1201	1	460	460
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	2180

Electronic Acknowledgement Receipt	
EFS ID:	34428724
Application Number:	16207183
International Application Number:	
Confirmation Number:	2734
Title of Invention:	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method
First Named Inventor/Applicant Name:	Zhiguo Li
Customer Number:	27765
Filer:	Winston Hsu/Sibyl Yu
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	YMTP0079USA3
Receipt Date:	02-DEC-2018
Filing Date:	
Time Stamp:	22:27:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$2180
RAM confirmation Number	120318INTEFSW00009611503105
Deposit Account	503105
Authorized User	Sibyl Yu
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

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37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Drawings-only black and white line drawings	3325825.PDF	95478 7a3ea90825304c793a5ca38eb8e881363efe66d6	no	3
Warnings:					
Information:					
2	Abstract	3325824.PDF	29852 18f97a241421a62255aa0f48a745c91b98e3c2d5	no	1
Warnings:					
Information:					
3	Claims	3325823.PDF	34138 e2e3335d17260f2c0c30613c776fdb667cc7248b	no	3
Warnings:					
Information:					
4	Specification	3325822.PDF	59903 671bd112f5ba318e05c85d4c473d9f9f14f365aa	no	8
Warnings:					
Information:					
5	Application Data Sheet	3325364.PDF	1782191 c78837cde93d908c4a40290fa1e37428d969415c	no	8
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Information:					
6	Internet Communications Authorized	3325361.PDF	415082 b1bbd8a2af460e89397b51e109d387244eb503dc	no	2
Warnings:					
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7	Oath or Declaration filed	3325360.PDF	120711 4da041fc20d78f4152e19a38a6dac3083991fcba	no	3
Warnings:					
Information:					
8	Power of Attorney	3325359.PDF	502348 bc5dc96fafa16cf5118432e17bcecc848812a016	no	2
Warnings:					
Information:					
9	Fee Worksheet (SB06)	fee-info.pdf	36799 3df1d5c48e10b519bf5e5b44520d4567d8c99a3f	no	2
Warnings:					
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<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

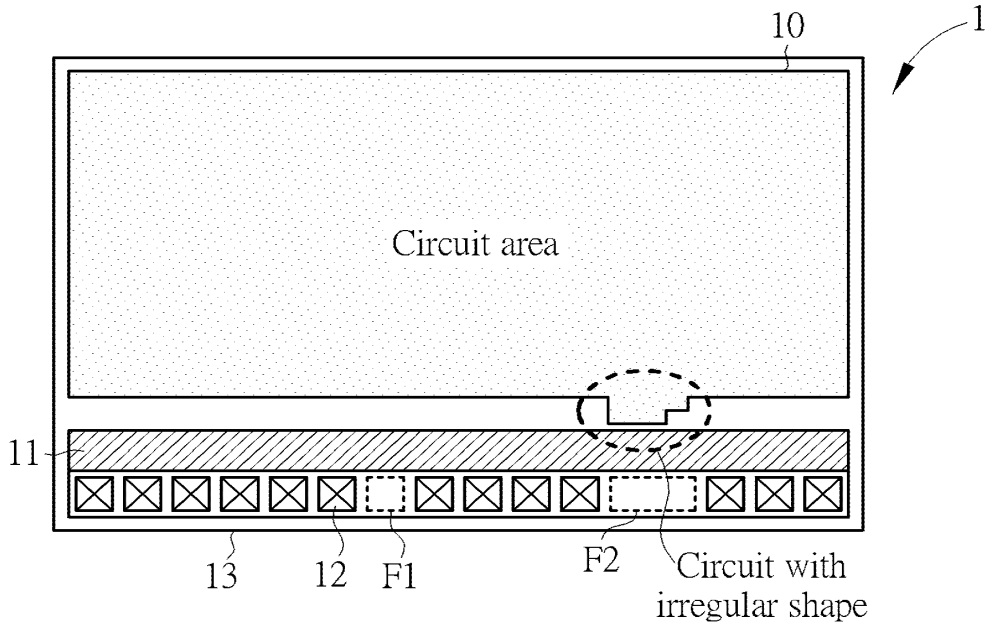


FIG. 1 PRIOR ART

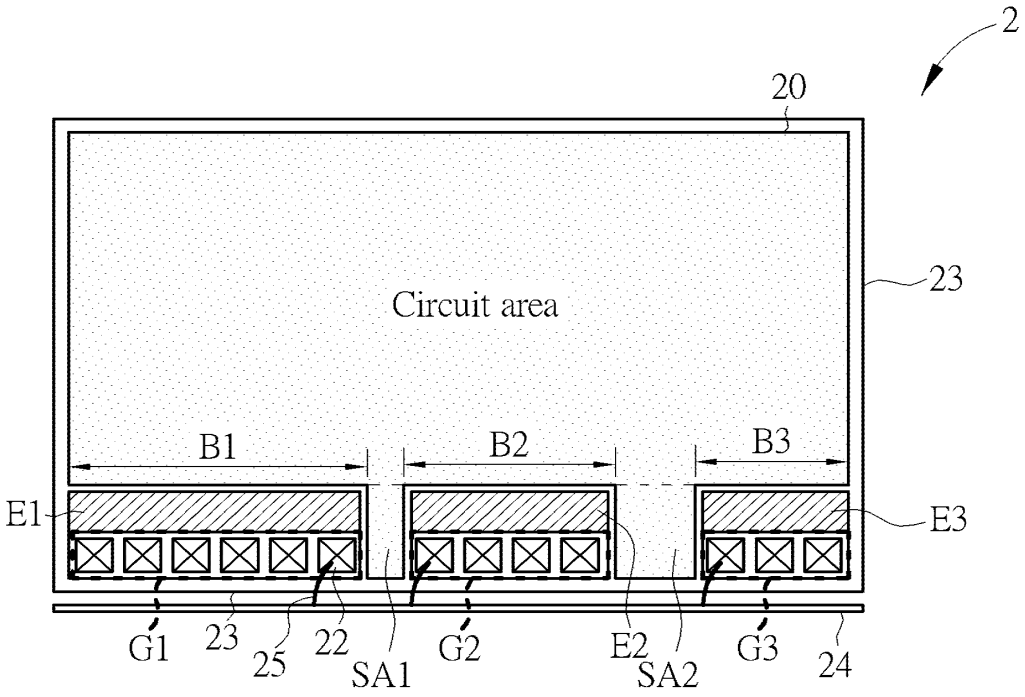


FIG. 2

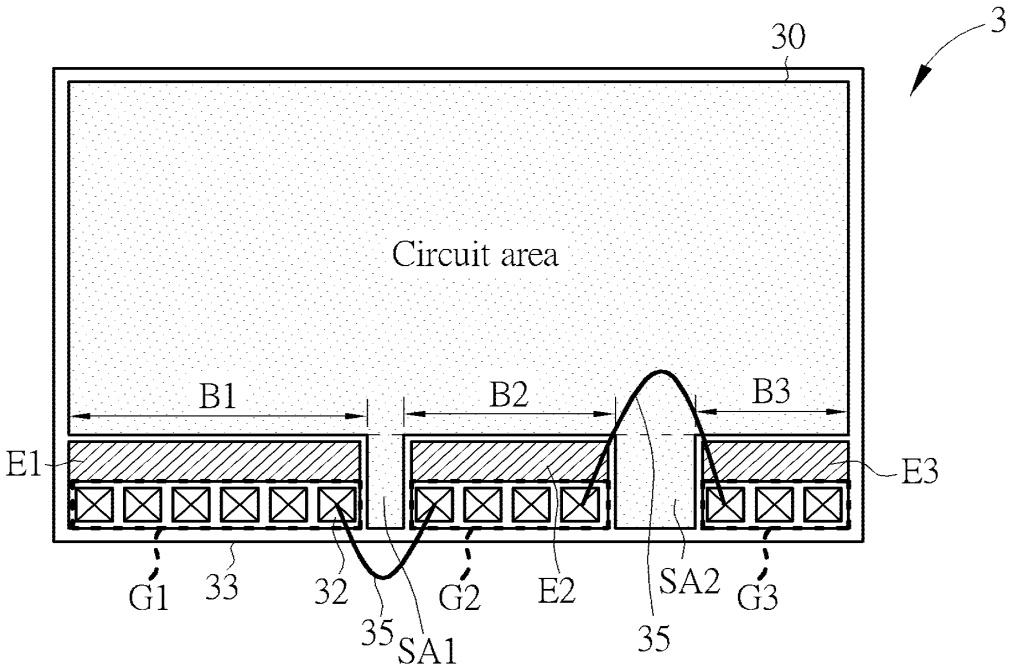

3
30
Circuit area
B1
B2
B3
E1
E3
G1
33
32
35
SA1
G2
E2
35
SA2
G3

FIG. 3

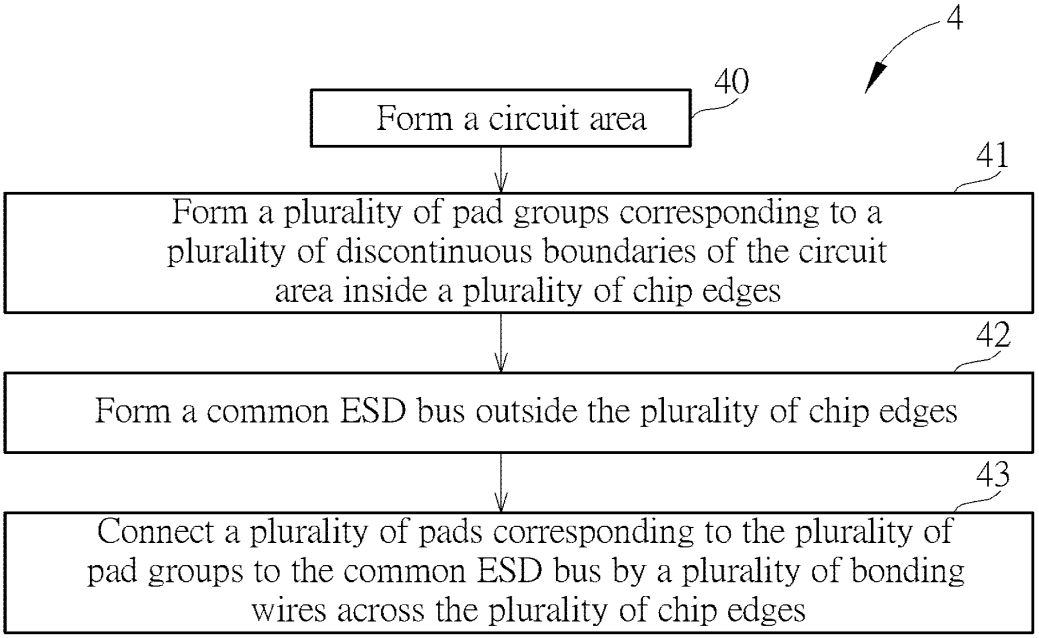

4
40
Form a circuit area
41
Form a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area inside a plurality of chip edges
42
Form a common ESD bus outside the plurality of chip edges
43
Connect a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires across the plurality of chip edges

FIG. 4

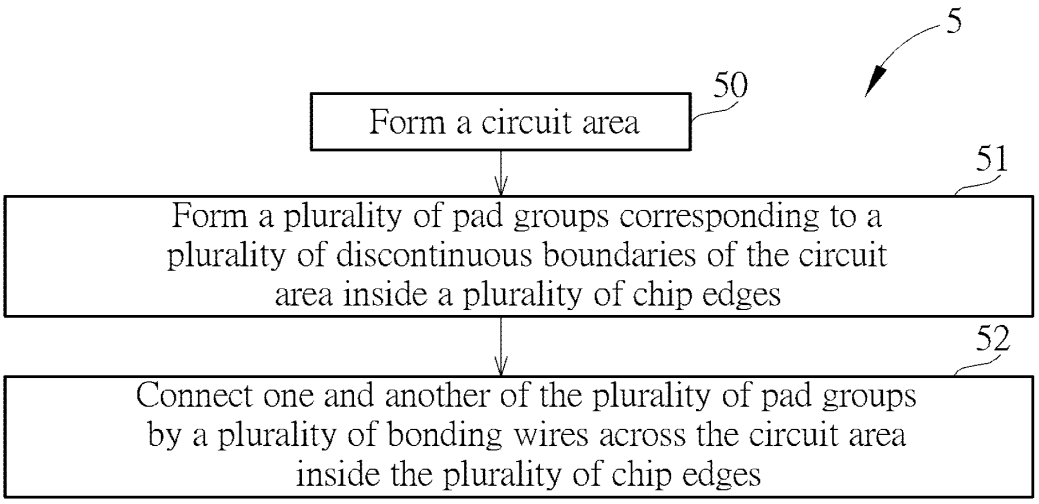

5
50
Form a circuit area
51
Form a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area inside a plurality of chip edges
52
Connect one and another of the plurality of pad groups by a plurality of bonding wires across the circuit area inside the plurality of chip edges

FIG. 5

Abstract of Disclosure

An integrated circuit ESD bus structure includes a circuit area; a plurality of electrostatic discharge (ESD) buses; a plurality of pad groups adjacent and connected to the plurality of ESD buses; a common ESD bus; and a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus.

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Claims

What is claimed is:

1. An integrated circuit structure, comprising:
   a circuit area;
   a plurality of ESD buses;
   a plurality of pad groups, adjacent and connected to the plurality of ESD buses;
   a common ESD bus, adjacent to the plurality of pad groups; and
   a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus.

2. The integrated circuit structure of claim 1, wherein each of the plurality of pad groups comprises at least one pad, and the plurality of bonding wires is configured to connect the at least one pad to the common ESD bus.

3. The integrated circuit structure of claim 1, wherein common ESD bus comprises a plurality discontinuous ESD bus groups.

4. The integrated circuit structure of claim 1, wherein the common ESD bus is formed outside the plurality of chip edges or inside the plurality of chip edges.

5. The integrated circuit structure of claim 1, wherein the circuit area comprises at least one saved area adjacent to the ESD buses, the plurality of pad groups.

6. The integrated circuit structure of claim 1, wherein the common ESD bus is parallel to the plurality of ESD buses.

7. An integrated circuit structure, comprising:
   a circuit area;
   a plurality of ESD buses;
   a plurality of pad groups, adjacent and connected to the plurality of ESD buses; and

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a plurality of bonding wires configured to connect one to another of the plurality of pad groups.

8. The integrated circuit structure of claim 7, wherein the circuit area comprises at least one saved area adjacent to the plurality of ESD buses and the plurality of pad groups.

9. The integrated circuit structure of claim 7, wherein each of the plurality of pad groups comprises a connecting pad, and the plurality of bonding wires are configured to connect the connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups.

10. A method of integrated circuit structure, comprising:
forming a circuit area;
forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area;
forming a common ESD bus adjacent to the plurality of pad groups; and
connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires.

11. The method of integrated circuit structure of claim 10, wherein each of the plurality of pad groups comprises at least one pad, and the plurality of bonding wires is configured to connect the at least one pad to the common ESD bus.

12. The method of integrated circuit structure of claim 10, further comprising:
forming the common ESD bus outside the plurality of chip edges or inside the plurality of chip edges.

13. The method of integrated circuit structure of claim 10, wherein the common ESD bus is parallel to the plurality of ESD buses.

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14. A method of integrated circuit structure, comprising:
forming a circuit area;
forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area; and
connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires across the circuit area.

15. The method of integrated circuit structure of claim 14, wherein the circuit area comprises at least one saved area adjacent to the plurality of ESD buses and the plurality of pad groups.

16. The method of integrated circuit structure of claim 14, wherein the common ESD bus is parallel to the plurality of ESD buses and the plurality of pad groups.

17. The method of integrated circuit structure of claim 14, wherein each of the plurality of pad groups comprises a connecting pad, and the plurality of bonding wires are configured to connect the connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups.

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Title

Integrated Circuit Electrostatic Discharge Bus Structure and Related Method

Cross Reference To Related Applications

[0001] This present application is a continuation application of International Application No. PCT/CN2018/113271 filed on November 1, 2018, which is incorporated herein by reference in its entirety.

Background of the Invention

1. Field of the Invention

[0002] The present invention relates to an integrated circuit structure and related method, and more particularly, to an integrated circuit electrostatic discharge bus structure and related method.

2. Description of the Prior Art

[0003] For an integrated circuit electrostatic discharge (hereinafter abbreviated ESD) structure 1 as shown in FIG. 1, I/O (input/output) pads 12 are placed around a circuit area 10 inside a plurality of chip edges 13 based on particular sequence and position, wherein the placement of the I/O pads 12 is adjustable within a specific range.

[0004] In general, it is commonly to place filler cells F1 and F2 at empty spaces between the I/O pads 12, and connect the filler cells F1 and F2 to an electrostatic discharge (ESD) bus 11 (e.g., a layout trace connected to a ground or a system voltage), which makes each portion of the circuit area 10 and the filler cells F1 and F2 are connected to the continuous ESD bus to provide ESD protection to the integrated circuit ESD bus structure 1.

[0005] However, the filler cells F1 and F2 take a portion of the circuit area 10 to be wasteful to the integrated circuit ESD bus structure 1. Further, under the strict requirement of the integrated circuit ESD bus structure 1 having a rectangular shape, it causes the lack

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of flexibility for internal circuit layout design.

[0006] Further, when there are circuits with irregular shapes and different areas, the circuit area 10 must be increased in order to contain the circuits with irregular shapes and different areas, which increases production cost.

[0007] Accordingly, it is desirable to provide an integrated circuit ESD bus structure and related method to make full use of the circuit area.

Summary of the Invention

[0008] It is therefore an objective of the present invention to provide an integrated circuit electrostatic discharge bus structure and related method.

[0009] To achieve the above technical object, according to the present invention, an integrated circuit electrostatic discharge (ESD) structure is provided, and includes a circuit area; a plurality of electrostatic discharge buses ; a plurality of pad groups adjacent and connected to the plurality of ESD buses; a common ESD bus; and a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus.

[0010] To achieve the above technical object, according to the present invention, an integrated circuit electrostatic discharge (ESD) structure is provided, and includes a circuit area; a plurality of electrostatic discharge (ESD) buses; a plurality of pad groups; and a plurality of bonding wires configured to connect one to another of the plurality of pad groups.

[0011] To achieve the above technical object, according to the present invention, a method of integrated circuit ESD bus structure is provided, and includes forming a circuit area; forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area; forming a common ESD bus; and connecting a

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plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires across one of the plurality of chip edges.

[0012] To achieve the above technical object, according to the present invention, a method of integrated circuit ESD bus structure is provided, and includes forming a circuit area, forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area; and connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires across the circuit area.

[0013] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

[0014] FIG. 1 is a schematic diagram of an integrated circuit ESD bus structure according to the prior art.

[0015] FIG. 2 is a schematic diagram of an integrated circuit ESD bus structure according to an embodiment of the present invention.

[0016] FIG. 3 is a schematic diagram of an integrated circuit ESD bus structure according to an embodiment of the present invention.

[0017] FIG. 4 is a flowchart of an integrated circuit packaging process according to an embodiment of the present invention.

[0018] FIG. 5 is a flowchart of an integrated circuit packaging process according to an embodiment of the present invention.

Detailed Description

[0019] FIG. 2 is a schematic diagram of an integrated circuit electrostatic discharge (ESD) structure 2 according to an embodiment of the present invention. The integrated circuit ESD bus structure 2 includes a circuit area 20, a plurality of ESD buses E1, E2 and E3, a plurality of pad groups G1, G2 and G3, a common ESD bus 24,

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and a plurality of bonding wires 25.

[0020] The circuit area 20 is formed by a plurality of chip edges 23; for example, the four chip edges 23 forms a rectangular area configured to contain the circuit area 20. The circuit area 20 includes a plurality of discontinuous boundaries B1, B2 and B3. The plurality of ESD buses E1, E2 and E3 is formed inside the chip edges 23, corresponding and adjacent to the plurality of discontinuous boundaries B1, B2, and B3.

[0021] The plurality of pad groups G1, G2 and G3 is formed inside the chip edges 23, adjacent and connected to the plurality of ESD buses E1, E2 and E3. The common ESD bus 24 is formed outside the chip edges 23, which is not limited. The common ESD bus 24 may not be formed in one piece, and include a plurality of discontinuous ESD bus groups. The plurality of bonding wires 25 is formed across the chip edges 23, and configured to connect the plurality of pad groups B1, B2 and B3 to the common ESD bus 24. In one embodiment, the common ESD bus 24 is parallel to the plurality of ESD buses E1, E2 and E3 and the plurality of pad groups G1, G2 and G3.

[0022] Each of the plurality of pad groups G1, G2 and G3 includes at least one pad 22, wherein the pad 22 is an input/output pad connected to a ground or a system low voltage. At least one of the plurality of bonding wires 25 is configured to connect the at least one pad 22 to the common ESD bus 24. In one embodiment, multiple bonding wires 25 may be configured to connect multiple pads 22 of the pad group G1 to the common ESD bus 24, which provides multiple connections to enhance conductivity between the pad group G1 and the common ESD bus 24 to improve ESD protection.

[0023] In such a structure, the discontinuous ESD buses E1, E2 and E3 may be connected together by connecting the pads 22 of the pad groups G1, G2 and G3 to the common ESD bus 24 through the bonding wires 25, which equivalently forms a continuous ESD bus for the

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integrated circuit ESD bus structure 2. As a result, the present invention may get rid of the filler cells of the prior art. In addition, spaces between the discontinuous ESD buses E1 and E2 (or, E2 and E3) may be configured with circuit elements to make full use of the integrated circuit ESD bus structure 2.

[0024] For example, the ESD bus 11 and the filler cells F1 and F2 shown in FIG. 1 are replaced by saved areas SA1 and SA2 in FIG. 2. The saved area SA1 is adjacent to the ESD buses E1 and E2 and the pads 22 of the pad groups G1 and G2. The saved area SA2 is adjacent to the ESD buses E2 and E3 and the pads 22 of the pad groups G2 and G3. In one embodiment, the common ESD bus 24 is formed inside the chip edges 23, and adjacent to the plurality of pad groups G1, G2 and G3 and the saved areas SA1 and SA2.

[0025] FIG. 3 is a schematic diagram of an integrated circuit ESD bus structure 3 according to an embodiment of the present invention. The integrated circuit ESD bus structure 3 includes a circuit area 30, a plurality of ESD buses E1, E2 and E3, a plurality of pad groups G1, G2 and G3, and a plurality of bonding wires 35.

[0026] The circuit area 30 is formed by a plurality of chip edges 33; for example, the four chip edges 33 form a rectangular area to contain the circuit area 30. The circuit area 30 includes a plurality of discontinuous boundaries B1, B2 and B3. The plurality of ESD buses E1, E2 and E3 is formed inside the chip edges 33, corresponding and adjacent to the plurality of discontinuous boundaries B1, B2, and B3.

[0027] The plurality of discontinuous ESD buses E1, E2 and E3 is formed inside the chip edges 33, and adjacent to the plurality of discontinuous boundaries B1, B2, and B3. The plurality of pad groups G1, G2, and G3 is formed inside the chip edges 33, adjacent and connected to the plurality of ESD buses E1, E2 and E3. The plurality of bonding wires 35 is formed across the circuit area 30, and

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configured to connect the plurality of pad groups G1, G2, and G3 from one group to another group, e.g., one bonding wire 35 may connect the pad group G1 to the pad group G2, and another bonding wire 35 may connect the pad group G2 to the pad group G3.

[0028] Each of the plurality of pad groups G1, G2 and G3 includes a plurality of pads 32, wherein the pad 32 is an input/output pad connected to a ground or a system low voltage. The plurality of bonding wires 35 is configured to connect the pads 32 of one group to another group. Each of the plurality of pad groups G1, G2 and G3 comprises a connecting pad (e.g., a right most pad of the pad group G1, left and right most pads of the pad group G2, and a left most pad of the pad group G3), and the plurality of bonding wires 35 are configured to connect the connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups. For example, one of the bonding wires 35 is configured to connect the right most pad 32 of the pad group G1 to the left most pad 32 of the pad group G2, and one of the bonding wires 35 is configured to connect the right most pad 32 of the pad group G2 to the left most pad 32 of the pad group G3, which is not limited.

[0029] In such a structure, the discontinuous ESD buses E1, E2 and E3 may be connected together by connecting the pads 32 of the pad groups G1, G2 and G3 from one group to another group, which equivalently forms a continuous ESD bus for the integrated circuit ESD bus structure 3. As a result, the present invention may get rid of the filler cells of the prior art. In addition, spaces between the discontinuous ESD buses E1 and E2 (or, E2 and E3) may be configured with circuit elements to make full use of the integrated circuit ESD bus structure 3. For example, the ESD bus 11 and the filler cells F1 and F2 shown in FIG. 1 are replaced by saved areas SA1 and SA2 in FIG. 2, and thus the circuit area 20 may contain the circuits with irregular shapes and different areas without increasing its area, which saves production cost.

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[0030] FIG. 4 is a flowchart of an integrated circuit ESD bus structure process 4 according to an embodiment of the present invention.

[0031] Step 40: Form a circuit area.

[0032] Step 41: Form a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area inside a plurality of chip edges.

[0033] Step 42: Form a common ESD bus outside the plurality of chip edges.

[0034] Step 43: Connect a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires across the plurality of chip edges.

[0035] In Step 40, a circuit area is formed; in step 41, a plurality of pad groups corresponding to a plurality of discontinuous boundaries of a circuit area inside a plurality of chip edges is formed; in step 42, a common ESD bus outside the plurality of chip edges is formed; and in step 43, a plurality of pads corresponding to the plurality of pad groups is connected to the common ESD bus by a plurality of bonding wires across the plurality of chip edges. By the integrated circuit ESD bus structure process 4, a continuous ESD bus may be equivalently formed and the filler cells of the prior art may be omitted.

[0036] FIG. 5 is a flowchart of an integrated circuit ESD bus structure process 5 according to an embodiment of the present invention.

[0037] Step 50: Form a circuit area.

[0038] Step 51: Form a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area inside a plurality of chip edges.

[0039] Step 52: Connect one and another of the plurality of pad groups by a plurality of bonding wires across the circuit area inside the plurality of chip edges.

[0040] In Step 50, a circuit area is formed; in step 51, a plurality

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of pad groups corresponding to a plurality of discontinuous boundaries of a circuit area inside a plurality of chip edges is formed; and in step 52, one and another of the plurality of pad groups are connected together by a plurality of bonding wires across the circuit area inside the plurality of chip edges. By the integrated circuit ESD bus structure process 5, a continuous ESD bus may be equivalently formed and the filler cells of the prior art may be omitted.

[0041] To sum up, the present invention utilizes bonding wires to connect a plurality of pads of a plurality of pad groups, so as to equivalently form a continuous ESD bus. As a result, the present invention may get rid of the filler cells of the prior art. In addition, spaces between the discontinuous ESD buses may be configured with circuit elements to make full use of the integrated circuit ESD bus structure.

[0042] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	YMTP0079USA3
	Application Number	
Title of Invention	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

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Residence Information (Select One) US Residency ● Non US Residency Active US Military Service

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Postal Code	**Country** [i] CN

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

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Application Information:

Title of the Invention	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method		
Attorney Docket Number	YMTP0079USA3	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	3	**Suggested Figure for Publication (if any)**	

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Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
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This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	PCT/CN2018/113271	2018-11-01

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	YMTP0079USA3
	Application Number	
Title of Invention	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method	

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This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Title of Invention	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method	

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When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

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The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	YMTP0079USA3
	Application Number	
Title of Invention	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method	

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Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

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● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

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Country	CN	Postal Code	
Phone Number		Fax Number	
Email Address			

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Assignee 1

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This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Roger Chen/			Date (YYYY-MM-DD)	2018-11-28
First Name	Roger	Last Name	Chen	Registration Number	67314

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	YMTP0079USA3
	Application Number	
Title of Invention	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method	

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/207,183	12/02/2018	2811	2180	YMTP0079USA3	17	4

CONFIRMATION NO. 2734

FILING RECEIPT

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., No.389, Fuhe Rd., Yonghe Dist.
New Taipei City,
TAIWAN

OC000000104643475

Date Mailed: 12/27/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Zhiguo Li, Wuhan City, CHINA;

Applicant(s)

Yangtze Memory Technologies Co., Ltd., Wuhan City, CHINA;

Power of Attorney: The patent practitioners associated with Customer Number 27765

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2018/113271 11/01/2018

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 12/20/2018
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/207,183**
Projected Publication Date: 05/07/2020

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Non-Publication Request: No

Early Publication Request: No

Title

Integrated Circuit Electrostatic Discharge Bus Structure and Related Method

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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IPR2025-00118

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/207,183

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	17 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4 minus 3 =	* 1				x 460 =	460
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2180

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16207183
	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	YMTP0079USA3

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20140061881	A1	2014-03-06	Yeh	

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1	201737459	TW	A	2017-10-16			Abstract

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16207183
	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	YMTP0079USA3

	1		

EXAMINER SIGNATURE			
Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16207183
	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	YMTP0079USA3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Roger Chen/	Date (YYYY-MM-DD)	2019-07-05
Name/Print	Roger Chen	Registration Number	67314

201737459

(19)中華民國智慧財產局

(12)發明說明書公開本 (11)公開編號：TW 201737459 A

(43)公開日： 中華民國 106 (2017) 年 10 月 16 日

(21)申請案號：105111171 (22)申請日： 中華民國 105 (2016) 年 04 月 11 日

(51)Int. Cl.： *H01L23/60 (2006.01)*

(71)申請人：力祥半導體股份有限公司 (中華民國) UBIQ SEMICONDUCTOR CORP. (TW)
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(72)發明人：陳志豪 CHEN, CHIH-HAO (TW)

(74)代理人：葉璟宗

申請實體審查：無 申請專利範圍項數：10 項 圖式數：5 共 28 頁

(54)名稱

暫態電壓抑制積體電路

TRANSIENT VOLTAGE SUPPRESSING INTEGRATED CIRCUIT

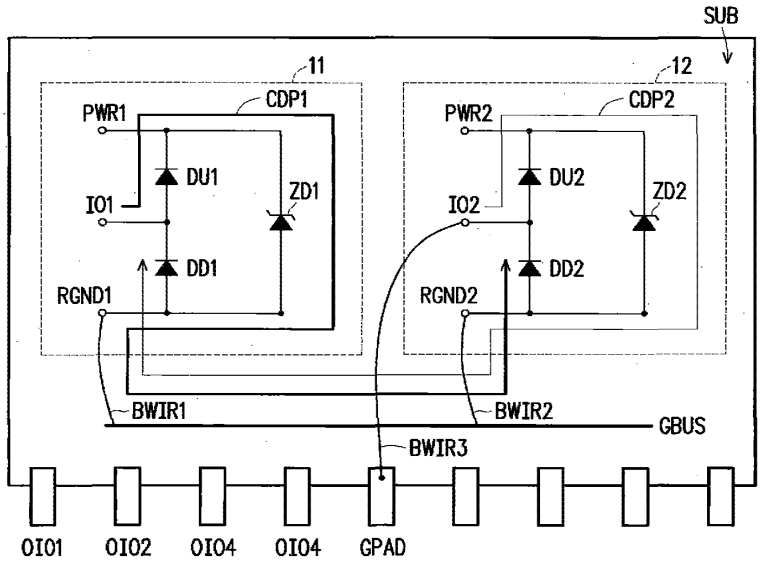
(57)摘要

暫態電壓抑制積體電路包括輸入輸出接腳、接地接腳、基板、第一暫態電壓抑制晶粒以及第二暫態電壓抑制晶粒。基板提供共同匯流排。第一暫態電壓抑制晶粒配置在基板上，且包括第一輸入輸出端與第一參考接地端。第二暫態電壓抑制晶粒配置在基板上，且包括第二輸入輸出端與第二參考接地端。第二參考接地端透過共同匯流排電性耦接至第一參考接地端，第一輸入輸出端耦接輸入輸出接腳，第二輸入輸出端耦接接地接腳。

A transient voltage suppressing (TVS) integrated circuit includes an input output pin, a ground pin, a substrate, a first TV die and a second TVS die. The substrate provides a common bus. The first TVS die is disposed on the substrate, and includes a first input output end and a first reference ground end. The second TVS die is disposed on the substrate and includes a second input output end and a second reference ground end. The second reference ground end is electrical coupled to the first reference ground end through the common bus, and the first input output end is coupled to the first input out pin, and the second input output end is coupled to a ground pin.

指定代表圖：

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【圖1】

符號簡單說明：

100・・・暫態電壓抑制積體電路

SUB・・・基板

11・・・第一暫態電壓抑制晶粒

12・・・第二暫態電壓抑制晶粒

RGND1~RGND2・・・參考接地端

IO1~IO2・・・輸入輸出端

BWIR1~BWIR3・・・封裝導線

GPAD・・・接地接腳

GBUS・・・共同匯流排

OIO1~OIO4・・・輸入輸出接腳

CDP1、CDP2・・・電流路徑

PWR1~PWR2・・・電源端

DU1、DD1、DU2、DD2・・・通道二極體

ZD1~ZD2・・・基納二極體

201737459
專利案號：105111171
201737459
申請日：105.4.11
IPC分類：H01L 23/60 (2006.1)

【發明摘要】

【中文發明名稱】

暫態電壓抑制積體電路

【英文發明名稱】

TRANSIENT VOLTAGE SUPPRESSING INTEGRATED CIRCUIT

【中文】暫態電壓抑制積體電路包括輸入輸出接腳、接地接腳、基板、第一暫態電壓抑制晶粒以及第二暫態電壓抑制晶粒。基板提供共同匯流排。第一暫態電壓抑制晶粒配置在基板上，且包括第一輸入輸出端與第一參考接地端。第二暫態電壓抑制晶粒配置在基板上，且包括第二輸入輸出端與第二參考接地端。第二參考接地端透過共同匯流排電性耦接至第一參考接地端，第一輸入輸出端耦接輸入輸出接腳，第二輸入輸出端耦接接地接腳。

【英文】A transient voltage suppressing (TVS) integrated circuit includes an input output pin, a ground pin, a substrate, a first TV die and a second TVS die. The substrate provides a common bus. The first TVS die is disposed on the substrate, and includes a first input output end and a first reference ground end. The second TVS die is disposed on the substrate and includes a second input output end and a second reference ground end. The second reference ground end is electrical coupled to the first reference ground end through the common bus, and the first input output end is coupled to

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the first input out pin, and the second input output end is coupled to a ground pin.

【指定代表圖】圖1。

【代表圖之符號簡單說明】

100：暫態電壓抑制積體電路

SUB：基板

11：第一暫態電壓抑制晶粒

12：第二暫態電壓抑制晶粒

RGND1~RGND2：參考接地端

IO1~IO2：輸入輸出端

BWIR1~BWIR3：封裝導線

GPAD：接地接腳

GBUS：共同匯流排

OIO1~OIO4：輸入輸出接腳

CDP1、CDP2：電流路徑

PWR1~PWR2：電源端

DU1、DD1、DU2、DD2：通道二極體

ZD1~ZD2：基納二極體

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【發明說明書】

【中文發明名稱】

暫態電壓抑制積體電路

【英文發明名稱】

TRANSIENT VOLTAGE SUPPRESSING INTEGRATED CIRCUIT

【技術領域】

【0001】 本發明是有關於一種暫態電壓抑制積體電路，且特別是有關於一種可分散靜電放電能量的暫態電壓抑制積體電路。

【先前技術】

【0002】 在現有的積體電路技術中，利用暫態電壓抑制器（transient voltage suppressor, TVS）來提供靜電放電電流的路徑，並藉以保護積體電路不因靜電放電現象而損毀是常見的作法。在習知技術領域中，暫態電壓抑制器會提供串接在電源端以及接地端間的二極體串與基納二極體來配合，並藉此產生電流路徑以執行靜電放電保護的動作。然而，當暫態電壓抑制器上的輸入輸出端上存在靜電放電電壓時，所有的靜電放電能量全由單一暫態電壓抑制器來承受。如此一來，暫態電壓抑制器能提供的靜電放電保護能力將會受到限制。

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【發明內容】

【0003】 本發明提供一種暫態電壓抑制積體電路，可有效增加靜電放電保護的能力。

【0004】 本發明的暫態電壓抑制積體電路包括輸入輸出接腳、接地接腳、基板、第一暫態電壓抑制晶粒以及第二暫態電壓抑制晶粒。基板提供共同匯流排。第一暫態電壓抑制晶粒配置在基板上，且包括第一輸入輸出端與第一參考接地端。第二暫態電壓抑制晶粒配置在基板上，且包括第二輸入輸出端與第二參考接地端。第二參考接地端透過共同匯流排電性耦接至第一參考接地端，第一輸入輸出端耦接輸入輸出接腳，第二輸入輸出端耦接接地接腳。

【0005】 在本發明的一實施例中，上述的第一暫態電壓抑制晶粒包括二極體串以及基納二極體，耦接於電源端以及第一參考接地端間。二極體串包括第一輸入輸出端。基納二極體的陽極耦接至第一參考接地端，陰極耦接至電源端。

【0006】 在本發明的一實施例中，上述的二極體串包括第一通道二極體以及第二通道二極體。第一通道二極體的陰極耦接至電源端，其陽極耦接至第一輸入輸出端。第二通道二極體的陰極耦接至第一通道二極體的陽極，其陽極耦接至第一參考接地端。

【0007】 在本發明的一實施例中，上述的第二暫態電壓抑制晶粒包括二極體串以及基納二極體。二極體串耦接於電源端以及第二參考接地端間，二極體串包括第二輸入輸出端。基納二極體的陽極耦接至第二參考接地端，其陰極耦接至電源端。

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【0008】 在本發明的一實施例中，上述的二極體串包括第一通道二極體以及第二通道二極體。第一通道二極體的陰極耦接至電源端，其陽極耦接至第二輸入輸出端。第二通道二極體的陰極耦接至第一通道二極體的陽極，其陰極耦接至第二參考接地端。

【0009】 在本發明的一實施例中，上述的第二暫態電壓抑制晶粒與第一暫態電壓抑制晶粒為相同構造。

【0010】 在本發明的一實施例中，上述的暫態電壓抑制晶粒的基底與基板電性隔離。

【0011】 在本發明的一實施例中，上述的第二暫態電壓抑制晶粒更具有一電源端，其中電源端與共同匯流排電性耦接。

【0012】 在本發明的一實施例中，當上述的第一暫態電壓抑制晶粒的數量為多個時，第二暫態電壓抑制晶粒配置於暫態電壓抑制晶粒的幾何中心。

【0013】 一種暫態電壓抑制積體電路，包括至少一輸入輸出接腳、接地接腳、基板、至少一第一暫態電壓抑制晶粒以及第二暫態電壓抑制晶粒。基板提供共同匯流排。第一暫態電壓抑制晶粒配置在基板上，包括第一輸入輸出端與第一參考接地端。第二暫態電壓抑制晶粒配置在基板上，包括第二輸入輸出端與第二參考接地端。第二參考接地端透過共同匯流排電性耦接至第一參考接地端，第一輸入輸出端耦接輸入輸出接腳其中之一，第二輸入輸出端耦接接地接腳。當靜電放電電壓存在於輸入輸出接腳的其中一個時，電流路徑經由與輸入輸出接腳耦接的第一輸入輸出端、

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第一參考接地端、共同匯流排、第二參考接地端、第二輸入輸出端至接地接腳。

【0014】 基於上述，本發明提供暫態電壓抑制積體電路，以在靜電放電現象發生時，透過第一暫態電壓抑制晶粒以及第二暫態電壓抑制晶粒提供的電流路徑來執行靜電放電的電流宣洩動作。如此一來，靜電放電的能量可由多個晶粒來共同分擔，可有效提升暫態電壓抑制積體電路的靜電放電保護的能力。

【0015】 本發明的基板可為半導體基板、陶瓷基板、印刷電路板、導線架或其他任何習知基板，並於其上佈置共同匯流排。此外，本發明實施例利用基板做為共同匯流排(例如：導線架)，可使暫態電壓抑制積體電路具有較佳散熱效果。

【0016】 為讓本發明的上述特徵和優點能更明顯易懂，下文特舉實施例，並配合所附圖式作詳細說明如下。

【圖式簡單說明】

【0017】

圖 1 繪示本發明的暫態電壓抑制積體電路的等效電路及靜電放電動作示意圖。

圖 2A 繪示本發明一實施例的多通道暫態電壓抑制積體電路的示意圖。

圖 2B 及圖 2C 繪示本發明一實施例的多通道暫態電壓抑制積體電路的等效電路及靜電放電動作示意圖。

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圖 3A 及圖 3B 繪示本發明另一實施例的多通道暫態電壓抑制積體電路的等效電路及靜電放電動作示意圖。

圖 4 及圖 5 分別繪示本發明不同實施例的多通道暫態電壓抑制積體電路的晶粒配置方式的示意圖。

【實施方式】

【0018】 請參照圖 1，圖 1 繪示本發明的暫態電壓抑制積體電路的等效電路及靜電放電動作示意圖。暫態電壓抑制積體電路 100 包括基板 SUB、輸入輸出接腳 OIO1~OIO4、接地接腳 GPAD 以及暫態電壓抑制晶粒 11、12。基板 SUB 提供共同匯流排 GBUS，暫態電壓抑制晶粒 11、12 配置在基板 SUB 上，且第一暫態電壓抑制晶粒 11 包括由通道二極體 DU1 以及 DD1 串接形成的二極體串，第二暫態電壓抑制晶粒 12 則包括由通道二極體 DU2 以及 DD2 串接形成的二極體串。在本實施例中，通道二極體 DU1 的陰極耦接至電源端 PWR1，通道二極體 DU1 的陽極耦接至通道二極體 DD1 的陰極並形成輸入輸出端 IO1。通道二極體 DD1 的陽極則耦接至參考接地端 RGND1。此外，通道二極體 DU2 的陰極耦接至電源端 PWR2，通道二極體 DU1 的陽極耦接至通道二極體 DD2 的陰極並形成輸入輸出端 IO2。通道二極體 DD2 的陽極則耦接至參考接地端 RGND2。

【0019】 暫態電壓抑制晶粒 11、12 並分別包括基納二極體 ZD1 及 ZD2。基納二極體 ZD1 的陰極耦接至電源端 PWR1，其陽極耦

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接至參考接地端 RGND1，基納二極體 ZD2 的陰極耦接至電源端 PWR2，其陽極耦接至參考接地端 RGND2。

【0020】 此外，輸入輸出端 IO1 可透過封裝導線電性耦接至輸入輸出接腳 OIO1~OIO4 的其中之一。

【0021】 上述第一暫態電壓抑制晶粒 11 的參考接地端 RGND1 透過封裝導線 BWIR1 電性耦接至共同匯流排 GBUS，其中共同匯流排 GBUS 可以為具導電性的基板 SUB(例如：導線架)或配置在基板 SUB 上的導線（或導電層）。當共同匯流排 GBUS 為具導電性的基板 SUB 時，參考接地端 RGND1 透過封裝導線 BWIR1 直接電性耦接至基板 SUB。第二暫態電壓抑制晶粒 12 的參考接地端 RGND2 也透過封裝導線 BWIR2 電性耦接至共同匯流排 GBUS1，並與參考接地端 RGND1 電性耦接。第二暫態電壓抑制晶粒 12 的輸入輸出端 IO2 則透過封裝導線 BWIR3 電性耦接至暫態電壓抑制積體電路 100 的接地接腳 GPAD，並可透過接地接腳 GPAD 耦接至接地電壓。

【0022】 當靜電放電現象發生時，例如在輸入輸出端 IO1 發生正向（大於 0 伏特）的靜電放電電壓時，通道二極體 DU1、基納二極體 ZD1 以及通道二極體 DD2 對應靜電放電電壓被導通，電流路徑 CDP1 對應被形成並使靜電放電電流可以由輸入輸出端 IO1 依序通過通道二極體 DU1、基納二極體 ZD1、共同匯流排 GBUS、通道二極體 DD2 以及輸入輸出端 IO2 順利地被宣洩至接地接腳 GPAD。

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【0023】 在另一方面，當靜電放電現象發生時，且在輸入輸出端IO1發生負向(小於0伏特)的靜電放電電壓時，通道二極體DU2、基納二極體ZD2以及通道二極體DD1對應靜電放電電壓被導通，電流路徑 CDP2 對應被形成並使靜電放電電流可以由輸入輸出端IO2依序經由通道二極體DU2、基納二極體ZD2、共同匯流排GBUS以及通道二極體DD1順利地被宣洩至輸入輸出端IO1。

【0024】 由上述說明可知，當靜電放電現象發生時，本發明實施例的暫態電壓抑制積體電路100利用暫態電壓抑制晶粒11、12共同承擔靜電放電能量。也就是說，本發明實施例透過共同匯流排來使得多個暫態電壓抑制晶粒承擔靜電放電能量，並可有效提昇所能提供的靜電放電保護的能力。

【0025】 上述實施例中，暫態電壓抑制晶粒11、12可以是具有完全相同電路結構的晶粒，如此一來，本發明實施例可透過一種基本的暫態電壓抑制元件，藉由封裝手段來產生不同的通道，如此，可以不需製作額外的新光罩、也不需生產新的晶圓的條件下，就可有效達到以多晶粒承受靜電放電能量的功效。

【0026】 特別值得一提的，本發明實施例中可直接由具導電性的基板 SUB（例如：導線架）來提供共同匯流排 GBUS，可使暫態電壓抑制積體電路 100 在靜電放電電流宣洩的過程中，還可具有較佳散熱效果。

【0027】 請參照圖 2A，圖 2A 繪示本發明一實施例的多通道暫態電壓抑制積體電路的示意圖。與圖 1 實施例不同的是，圖 2A 實施

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例的暫態電壓抑制晶粒為多通道暫態電壓抑制晶粒，並且具有額外的第一暫態電壓抑制晶粒 120，用以提供更多的輸入輸出端。

【0028】 多通道暫態電壓抑制積體電路 200 包括基板 101、暫態電壓抑制晶粒 110、120、130。暫態電壓抑制晶粒 110、120 以及 130 分別配置於基板 101 不同位置上，且暫態電壓抑制晶粒 110、120、130 與基板 101 的接觸面間可具有介電層（未繪示），以使暫態電壓抑制晶粒 110、120、130 的基底與基板 101 電性隔離。

【0029】 第一暫態電壓抑制晶粒 110、120 分別具有多個輸入輸出端 IO1~IO4、IO5~IO8 以及參考接地端 RGND1、RGND3。在本實施例中，參考接地端 RGND1 以及 RGND3 可分別透過封裝導線 BWIR1 以及 BWIR3 電性耦接至基板 101，而基板 101 可提供一匯流排使參考接地端 RGND1 以及 RGND3 相互耦接。

【0030】 此外，多個輸入輸出端 IO1~IO8 可透過多個封裝導線分別電性耦接至多通道暫態電壓抑制積體電路 200 的多個輸入輸出接腳 OIO1~OIO8。

【0031】 第二暫態電壓抑制晶粒 130 具有一個（或一個以上）的輸入輸出端 AIO1 以及參考接地端 RGND2。第二暫態電壓抑制晶粒 130 的參考接地端 RGND2 可透過基板 101 電性耦接至參考接地端 RGND1。在本實施例中，第二暫態電壓抑制晶粒 130 的參考接地端 RGND2 可透過封裝導線 BWIR2 電性耦接至基板 101 所提供的匯流排，並透過這個匯流排與參考接地端 RGND1 與 RGND3 電性耦接。並且，第二暫態電壓抑制晶粒 130 的輸入輸出端 AIO1

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可透過封裝導線 BWIR4 連接至接地接腳 GPAD，並透過接地接腳 GPAD 接收接地電壓。

【0032】 當靜電放電現象發生時，靜電放電電流可以自輸入輸出接腳 OIO1~OIO8 進入第一暫態電壓抑制晶粒 110（或 120）。經由基板 101 所提供的匯流排，靜電放電電流可進一步的透過第二暫態電壓抑制晶粒 130 宣洩至接地接腳 GPAD（接地電壓），以達到靜電放電保護的效果。

【0033】 為更仔細得知本發明實施例的動作細節，以下請參照圖 2B 以及圖 2C 繪示的暫態電壓抑制積體電路的等效電路及靜電放電動作示意圖。

【0034】 在圖 2B 中，第一暫態電壓抑制晶粒 110 包括多個二極體串以及基納二極體 ZD1，並具有電源端 PWR1、參考接地端 RGND1 以及多個輸入輸出端 IO1~IO4。二極體串相互並聯耦接，並耦接在電源端 PWR1 以及參考接地端 RGND1 間，基納二極體 ZD1 同樣耦接在電源端 PWR1 以及參考接地端 RGND1 間，並且，基納二極體 ZD1 的陽極耦接至參考接地端 RGND1 而基納二極體 ZD1 的陰極耦接至電源端 PWR1。以由通道二極體 DU11 以及 DD11 所形成的二極體串為範例，通道二極體 DU11 的陰極耦接至電源端 PWR1 而其陽極形成輸入輸出端 IO2 並耦接至通道二極體 DD11 的陰極。另外，通道二極體 DD11 的陽極則耦接至參考接地端 RGND1。

【0035】 第一暫態電壓抑制晶粒 120 包括多個二極體串以及基納

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二極體 ZD2，並具有電源端 PWR3、參考接地端 RGND3 以及多個輸入輸出端 IO5~IO8。第一暫態電壓抑制晶粒 120 與第一暫態電壓抑制晶粒 110 可具有相同的電路架構，在此處不多贅述。

【0036】 在另一方面，第二暫態電壓抑制晶粒 130 包括多個並聯耦接於電源端 PWR2 以及參考接地端 RGND2 的二極體串以及基納二極體 ZD3。此外，由通道二極體 DUR1 以及 DDR1 所形成的二極體串中，通道二極體 DUR1 的陰極耦接至電源端 PWR2，其陽極形成輸入輸出端 AIO1 並耦接至通道二極體 DDR1 的陰極。另外，通道二極體 DDR1 的陽極則耦接至參考接地端 RGND2。

【0037】 第一暫態電壓抑制晶粒 110、120 以及第二暫態電壓抑制晶粒 130 分別具有參考接地端 RGND1-RGND3，分別透過封裝導線 BWIR2、BWIR2 及 BWIR3 電性耦接至基板所提供的共同匯流排 GBUS。另外，第二暫態電壓抑制晶粒 130 上的輸入輸出端 AIO1 則透過封裝導線 BWIR4 電性耦接至接地接腳 GPAD。

【0038】 圖 2B 為正向的靜電放電動作示意圖，當大於接地電壓（例如 0 伏特）的靜電放電電壓存在於一耦接輸入輸出端 IO2 上的輸入輸出接腳（未繪示）時，由於第一暫態電壓抑制晶粒 110 透過共同匯流排 GBUS 連接第二暫態電壓抑制晶粒 130。形成電流路徑 CDP3 經由輸入輸出端 IO2、參考接地端 RGND1、共同匯流排 GBUS、參考接地端 RGND2 至輸入輸出端 AIO1，並延伸至接地接腳 GPAD，以將靜電放電電流至接地電壓。

【0039】 圖 2C 為負向的靜電放電動作示意圖，在當小於接地電壓

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（例如 0 伏特）的靜電放電電壓存在於例如與輸入輸出端 IO7 耦接的輸入輸出接腳（未繪示）時，形成電流路徑 CDP4 通過第二暫態電壓抑制晶粒 130、共同匯流排 GBUS 及第一暫態電壓抑制晶粒 120，以進行靜電放電電流的宣洩動作，達到以多晶粒承載靜電放電能量的功效。

【0040】 在本實施例中，第一暫態電壓抑制晶粒 110、120 以及第二暫態電壓抑制晶粒 130 都可以利用相同電路架構的晶粒來實施。而關於第二暫態電壓抑制晶粒 130 的實施方式中，僅需選擇第二暫態電壓抑制晶粒 130 中的一個或多個輸入輸出端為輸入輸出端，並將被選中的輸入輸出端透過封裝導線電性耦接至基板所提供的共同匯流排 GBUS 上即可。

【0041】 圖 3A 及圖 3B 繪示本發明另一實施例的多通道暫態電壓抑制積體電路的等效電路及靜電放電動作示意圖。與前述實施例不同的是，第二暫態電壓抑制晶粒 330 的電源端 PWR2 透過封裝導線 BWIR5 電性耦接至基板所提供的共同匯流排 GBUS 上。此結構除了具有前述實施例的功效外，更可降低負向靜電放電時，電流路徑的導通電壓，進而提升靜電放電保護的效果。

【0042】 圖 3A 為正向的靜電放電動作示意圖，當大於接地電壓（例如 0 伏特）的靜電放電電壓存在於與輸入輸出端 IO2 耦接的輸入輸出接腳上（未繪示）時，其電流路徑 CDP5 與圖 2B 的實施例相同，在此不多贅述。

【0043】 圖 3B 為負向的靜電放電動作示意圖，當小於接地電壓

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（例如 0 伏特）的靜電放電電壓存在於與輸入輸出端 IO7 耦接的輸入輸出接腳（未繪示）時，產生電流路徑 CDP6 通過兩個晶粒，達到以多晶粒承載靜電放電能量的功效。由於第二暫態電壓抑制晶粒 330 的電源端 PWR2 電性耦接至共同匯流排 GBUS 上，電流路徑 CDP6 僅通過通道二極體 DUR1 與 DD21，並避過基納二極體 ZD3，降低了電流路徑 CDP6 上電流路徑的導通電壓，進而提升靜電放電保護的效果。

【0044】 以下請參照圖 4 及圖 5，圖 4 及圖 5 分別繪示本發明不同實施例的暫態電壓抑制積體電路的晶粒配置方式的示意圖。本發明實施例中，第一暫態電壓抑制晶粒與第二暫態電壓抑制晶粒的配置方式，可依據圖 2 實施例的方式，將第二暫態電壓抑制晶粒 130 配置在第一暫態電壓抑制晶粒 110 及 120 的中間。透過這樣的配置方式，可以使發生在輸入輸出端上的靜電放電電壓所產生的電流路徑長度均勻化，而不會因為一個或部分的輸入輸出端所產生的電流路徑的長度過長而降低靜電放電保護的等級。除圖 2 的配置方式外，本發明實施例的暫態電壓抑制積體電路上的晶粒還有多種不同的配置方式。

【0045】 請先參照圖 4，圖 4 中的暫態電壓抑制積體電路 400 具有第一暫態電壓抑制晶粒 401-404 以及第二暫態電壓抑制晶粒 410。第一暫態電壓抑制晶粒 401-404 分別具有參考接地端 RGND1、RGND3、RGND4 以及 RGND5，第二暫態電壓抑制晶粒 410 則具有參考接地端 RGND2。參考接地端 RGND1、RGND3 分別透過不

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同的封裝導線電性耦接至基板所提供的共同匯流排 GBUS1，而參考接地端 RGND4、RGND5 分別透過不同的封裝導線電性耦接至基板所提供的共同匯流排 GBUS2，而參考接地端 RGND2 則可透過多個封裝導線電性耦接至共同匯流排 GBUS1 及 GBUS2。共同匯流排 GBUS1 及 GBUS2 是電性相連的。在圖 4 中，第二暫態電壓抑制晶粒 410 可配置在鄰近於第一暫態電壓抑制晶粒 401-404 的幾何中心的位置或直接配置在第一暫態電壓抑制晶粒 401-404 的幾何中心的位置上。並藉此均勻化發生在第一暫態電壓抑制晶粒 401-404 上的輸入輸出端上的靜電放電電壓產生的電流路徑長度。

【0046】 接著請參照圖 5，在圖 5 中，暫態電壓抑制積體電路 500 具有第一暫態電壓抑制晶粒 501-503 以及第二暫態電壓抑制晶粒 510。第一暫態電壓抑制晶粒 501-503 以三角形的方式進行配置，而第二暫態電壓抑制晶粒 510 則鄰近於第一暫態電壓抑制晶粒 501-503 的幾何中心來進行配置，並使靜電放電電壓在第一暫態電壓抑制晶粒 501-503 上的多個輸入輸出端所產生的電流路徑的長度可以均勻化。

【0047】 附帶一提的，本發明實施例中的第一暫態電壓抑制晶粒以及第二暫態電壓抑制晶粒的數量並沒有固定的限制，設計者可以依據實際的需求來設置不同數量的第一暫態電壓抑制晶粒以及第二暫態電壓抑制晶粒，並依據基板的形狀、基板所提供的外引腳的位置來針對第一暫態電壓抑制晶粒以及第二暫態電壓抑制晶

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粒進行不同位置配置。

【0048】 綜上所述，本發明在暫態電壓抑制積體電路中提供一個或多個的第二暫態電壓抑制晶粒，以分擔第一暫態電壓抑制晶粒所承載靜電放電現象產生的能量，有效提升暫態電壓抑制積體電路所能提供的靜電放電保護的等級。

【0049】 雖然本發明已以實施例揭露如上，然其並非用以限定本發明，任何所屬技術領域中具有通常知識者，在不脫離本發明的精神和範圍內，當可作些許的更動與潤飾，故本發明的保護範圍當視後附的申請專利範圍所界定者為準。

【符號說明】

【0050】

100、200、300、400、500：暫態電壓抑制積體電路

101、SUB：基板

11、12、110、120、130、310、320、330、401~404、501~503、410、510：暫態電壓抑制晶粒

RGND1~RGND3：參考接地端

IO1~IO8：輸入輸出端

OIO1~OIO8：輸入輸出接腳

BWIR1~BWIR5：封裝導線

AIO1：輸入輸出端

GPAD：接地接腳

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ZD1~ZD3：基納二極體

PWR1~PWR3：電源端

DU1、DD1、DU2、DD2、DU11、DD11、DUR1、DDR1：通道二極體

GBUS、GBUS1、GBUS2：匯流排

CDP1~CDP6：電流路徑

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【發明申請專利範圍】

【第1項】　一種暫態電壓抑制積體電路，包括：

一輸入輸出接腳；

一接地接腳；

一基板，提供一共同匯流排；

一第一暫態電壓抑制晶粒，配置在該基板上，且包括一第一輸入輸出端與一第一參考接地端；以及

一第二暫態電壓抑制晶粒，配置在該基板上，且包括一第二輸入輸出端與一第二參考接地端；

其中，該第二參考接地端透過該共同匯流排電性耦接至該第一參考接地端，該第一輸入輸出端耦接該輸入輸出接腳，該第二輸入輸出端耦接該接地接腳。

【第2項】　如申請專利範圍第1項所述的暫態電壓抑制積體電路，其中該第一暫態電壓抑制晶粒包括：

一個二極體串，耦接於一電源端以及該第一參考接地端間，該二極體串包括該第一輸入輸出端；以及

一基納二極體，其陽極耦接至該第一參考接地端，其陰極耦接至該電源端。

【第3項】　如申請專利範圍第2項所述的暫態電壓抑制積體電路，其中該二極體串包括：

一第一通道二極體，其陰極耦接至該電源端，其陽極耦接至該第一輸入輸出端；以及

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一第二通道二極體，其陰極耦接至該第一通道二極體的陽極，其陽極耦接至該第一參考接地端。

【第4項】　如申請專利範圍第1項所述的暫態電壓抑制積體電路，其中該第二暫態電壓抑制晶粒包括：

一個二極體串，耦接於一電源端以及該第二參考接地端間，該二極體串包括該第二輸入輸出端；以及

一基納二極體，其陽極耦接至該第二參考接地端，其陰極耦接至該電源端。

【第5項】　如申請專利範圍第4項所述的暫態電壓抑制積體電路，其中該二極體串包括：

一第一通道二極體，其陰極耦接至該電源端，其陽極耦接至該第二輸入輸出端；以及

一第二通道二極體，其陰極耦接至該第一通道二極體的陽極，其陰極耦接至該第二參考接地端。

【第6項】　如申請專利範圍第1項所述的暫態電壓抑制積體電路，其中該第二暫態電壓抑制晶粒與該第一暫態電壓抑制晶粒為相同構造。

【第7項】　如申請專利範圍第1項所述的暫態電壓抑制積體電路，其中該些暫態電壓抑制晶粒的基底與該基板電性隔離。

【第8項】　如申請專利範圍第1項所述的暫態電壓抑制積體電路，其中該第二暫態電壓抑制晶粒更具有一電源端，其中該電源端與該共同匯流排電性耦接。

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【第9項】　如申請專利範圍第1項所述的暫態電壓抑制積體電路，其中當該第一暫態電壓抑制晶粒的數量為多個時，該第二暫態電壓抑制晶粒配置於該些暫態電壓抑制晶粒的幾何中心。

【第10項】　一種暫態電壓抑制積體電路，包括：

至少一輸入輸出接腳；

一接地接腳；

一基板，以提供一共同匯流排；

至少一第一暫態電壓抑制晶粒，配置在該基板上，包括一第一輸入輸出端與一第一參考接地端；以及

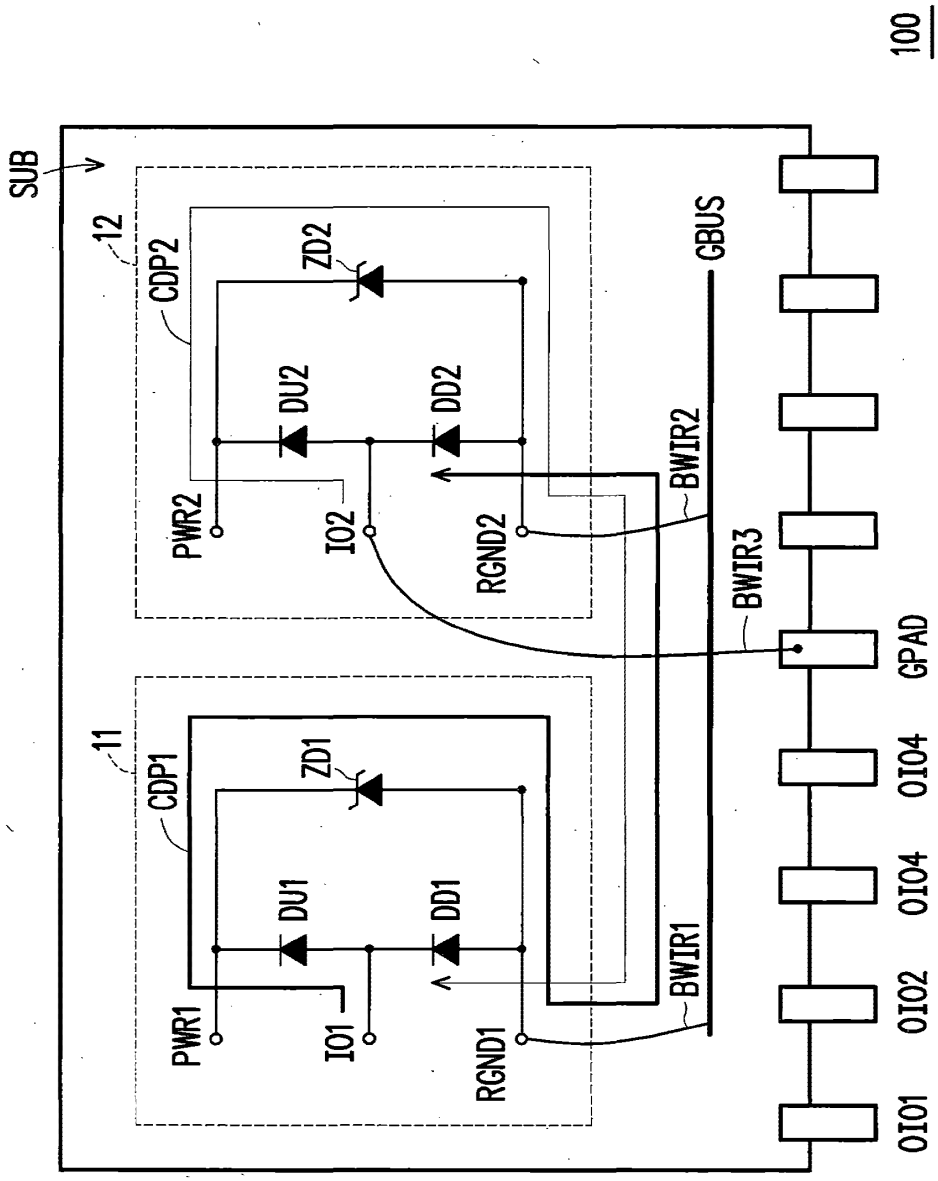
一第二暫態電壓抑制晶粒，配置在該基板上，包括一第二輸入輸出端與一第二參考接地端；

其中，該第二參考接地端透過該共同匯流排電性耦接至該第一參考接地端，該第一輸入輸出端耦接該些輸入輸出接腳其中之一，該第二輸入輸出端耦接該接地接腳，

其中，當一靜電放電電壓存在於其中一個該輸入輸出接腳時，一電流路徑經由與該輸入輸出接腳耦接的該第一輸入輸出端、該第一參考接地端、該共同匯流排、該第二參考接地端、該第二輸入輸出端至該接地接腳。

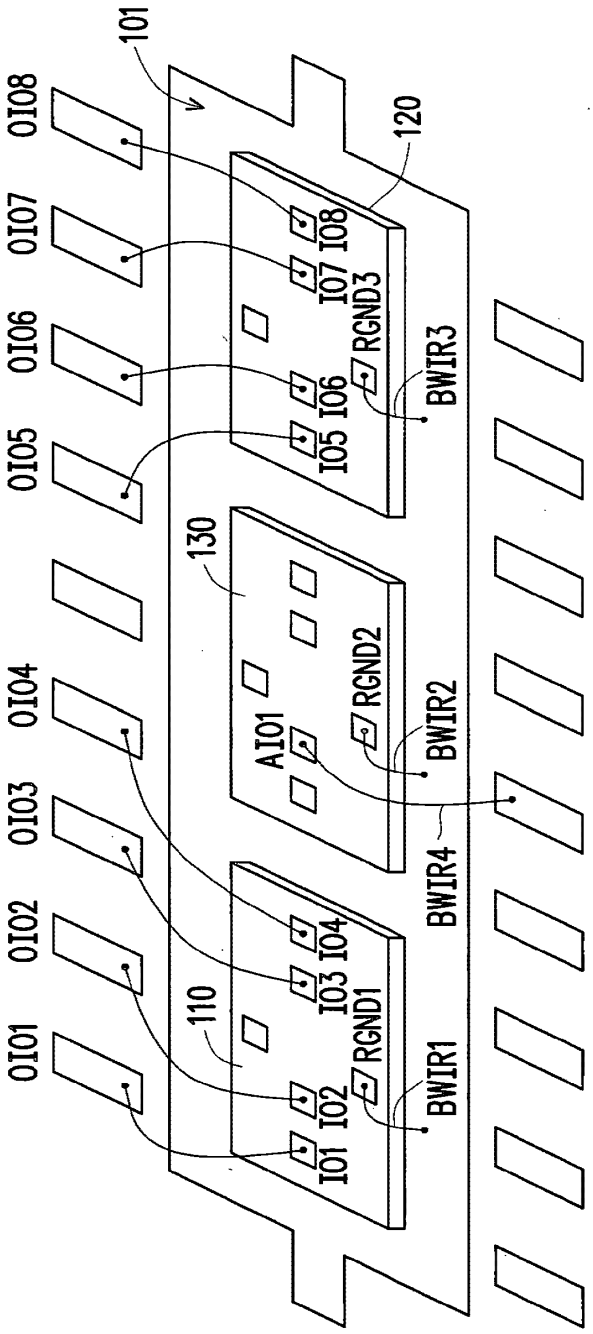
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【發明圖式】



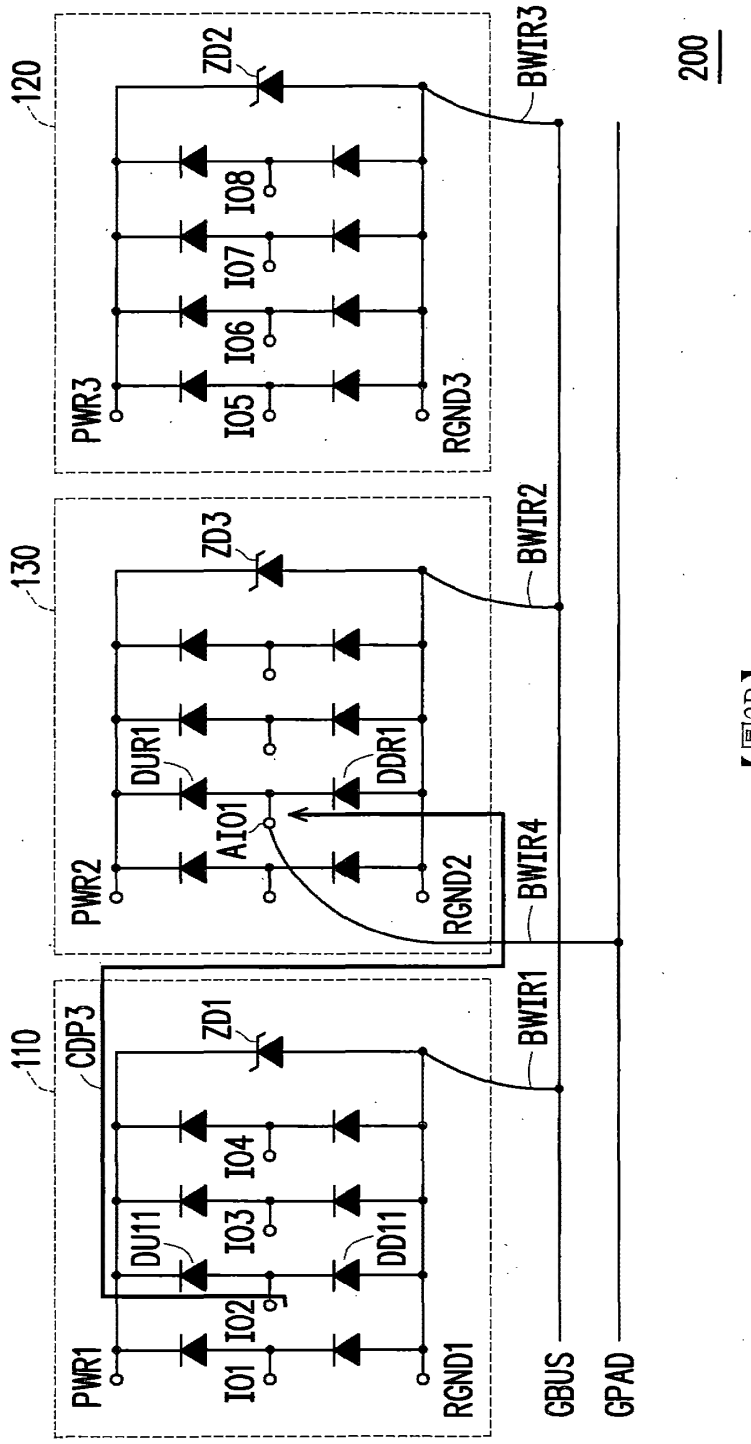
【圖1】

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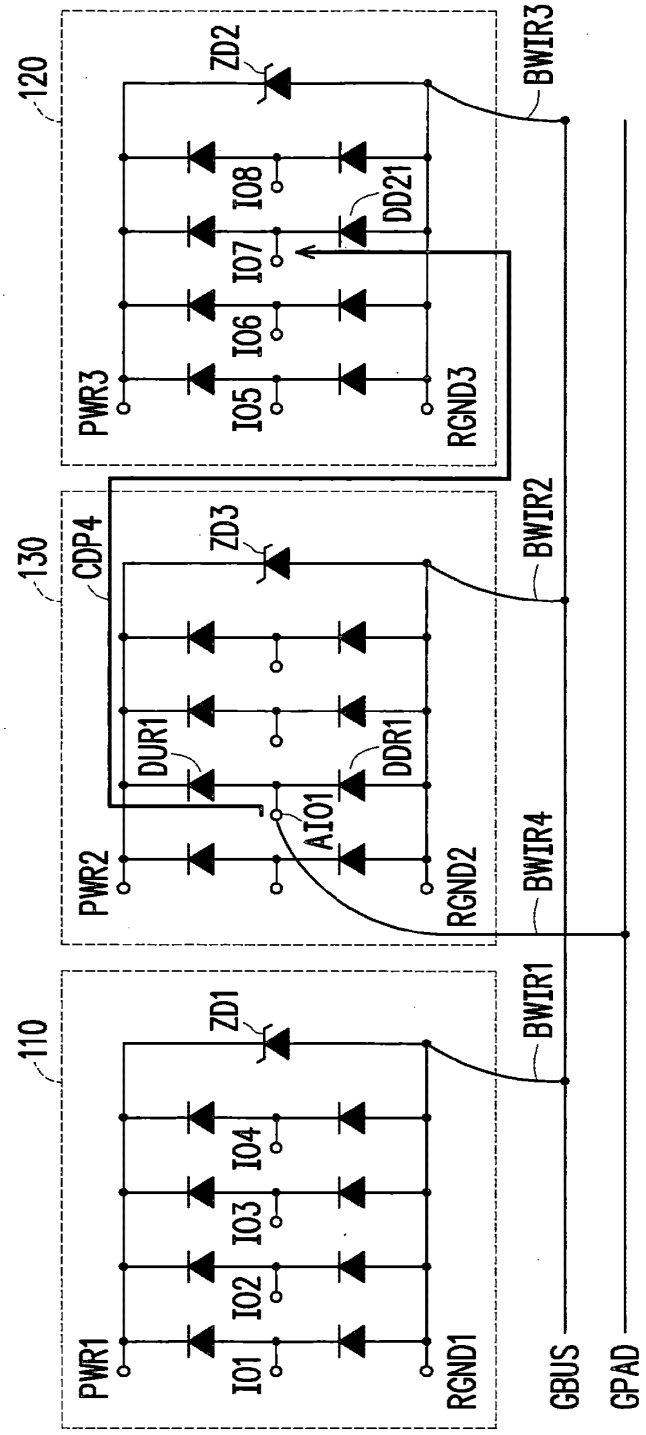
【圖2A】

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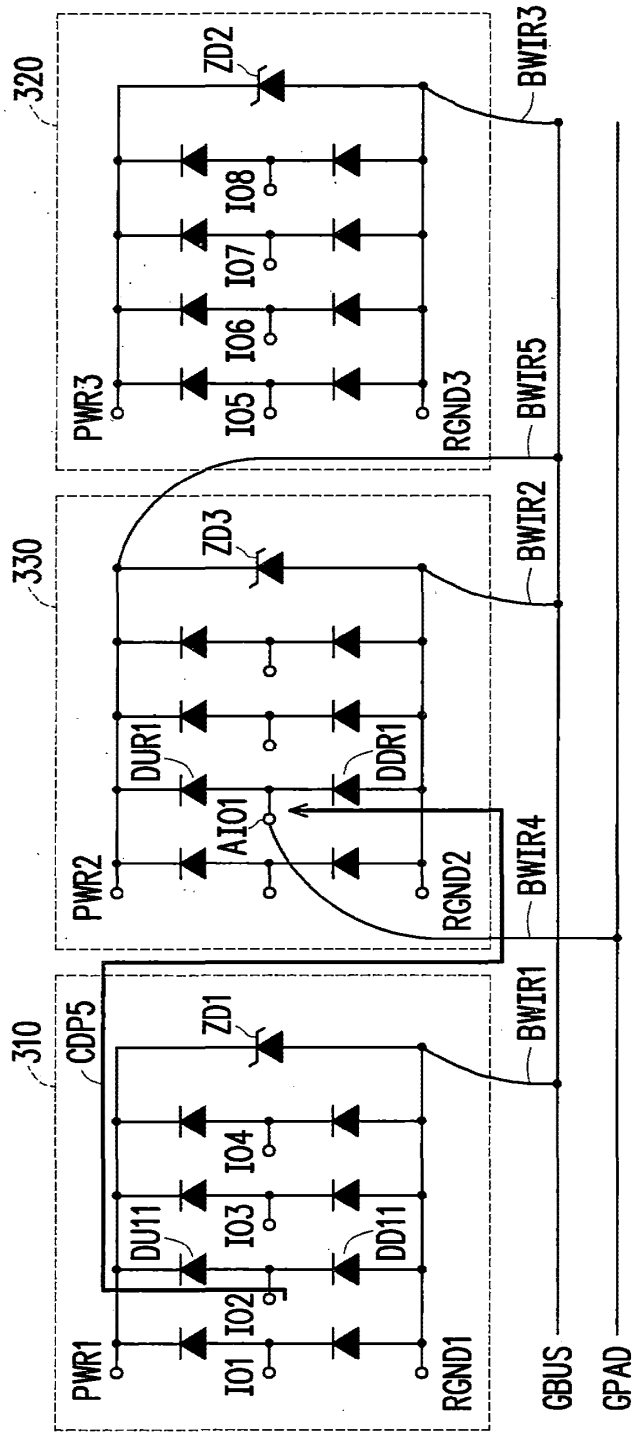
【圖2B】

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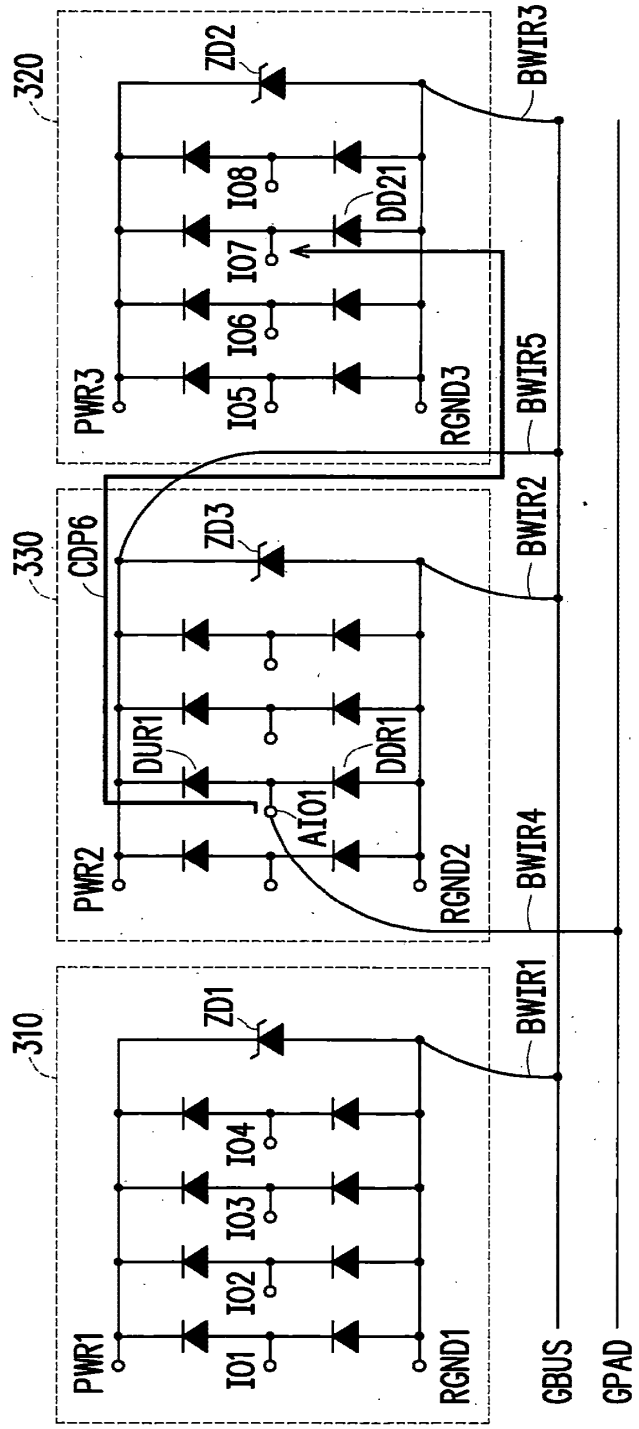
【圖2C】

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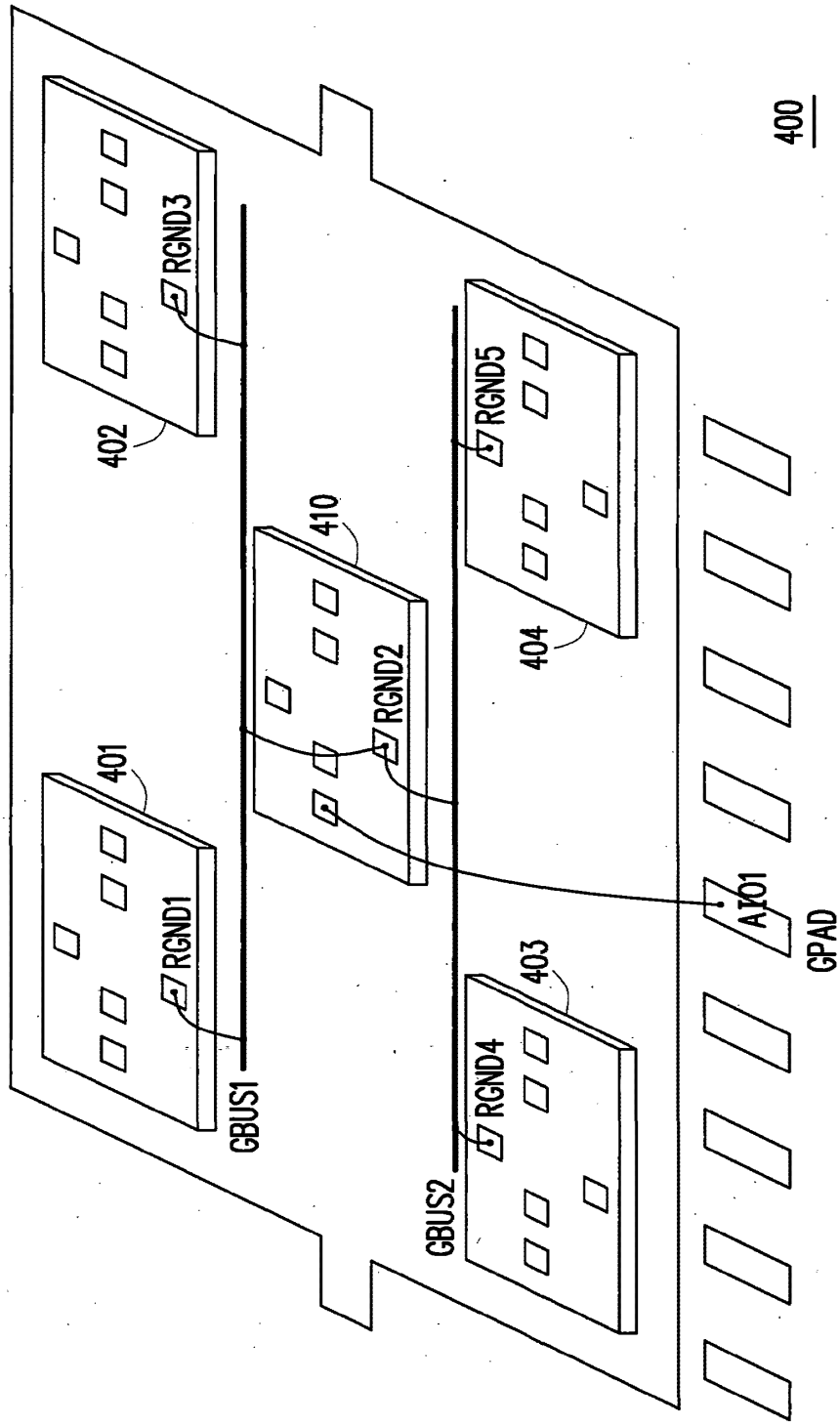
【圖3A】

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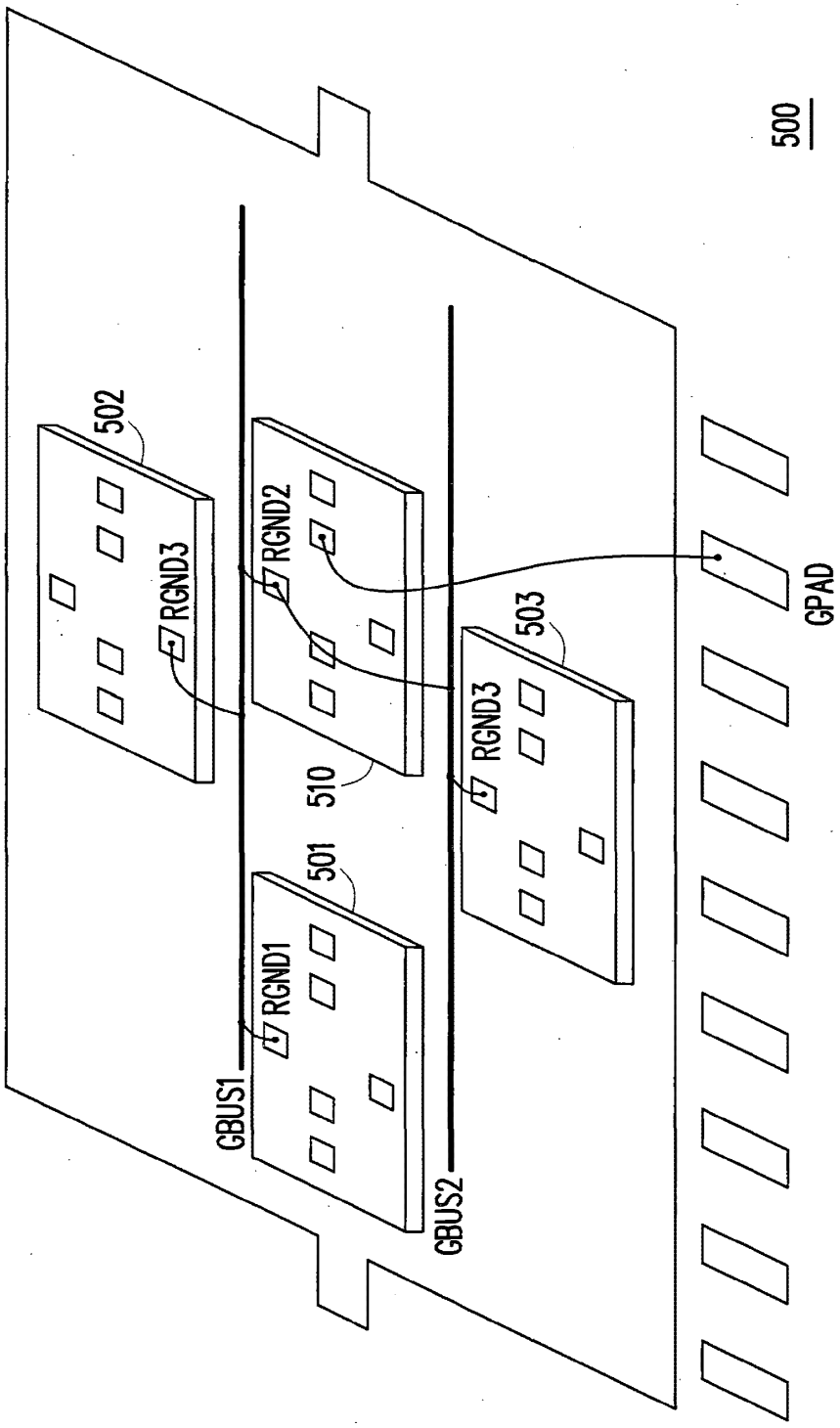
【圖3B】

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【圖4】

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【圖5】

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Electronic Acknowledgement Receipt

EFS ID:	36502408
Application Number:	16207183
International Application Number:	
Confirmation Number:	2734
Title of Invention:	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method
First Named Inventor/Applicant Name:	Zhiguo Li
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Edie Hung
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	YMTP0079USA3
Receipt Date:	08-JUL-2019
Filing Date:	02-DEC-2018
Time Stamp:	03:59:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	3518760.PDF	26032 276b8efed3d5416fed2d31a5a3089f38726c93b1	no	3

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16207183
	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	YMTP0079USA3

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1	101221629	CN	A	2008-07-16			Abstract
	2	102054523	CN	A	2011-05-11			Abstract
	3	103681654	CN	A	2014-03-26			Abstract

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
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	First Named Inventor	Zhiguo Li
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	YMTP0079USA3

NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1		

EXAMINER SIGNATURE			
Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16207183
	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	YMTP0079USA3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Roger Chen/	Date (YYYY-MM-DD)	2019-07-12
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Abstract of CN101221629

A chip for a smart card including a plurality of electrical contacts for communication of data with a smart card reader is disclosed. In one embodiment, a chip for a smart card includes a core circuit and a plurality of input/output pads corresponding to said set of electrical contacts, wherein said input/output pads are divided into at least a first column and a second column placed immediately adjacent to the first column, such that the first and second columns form a cluster. In another embodiment, eight input/output pads are divided into two columns, placed immediately adjacent to each other. The cluster may be partially surrounded by the core circuit. The chip may further comprise an ESD network, comprising VDD and GND buses for improved ESD protection while reducing the size of the chip.

[19] 中华人民共和国国家知识产权局

[12] 发明专利申请公布说明书

[21] 申请号 200810002239.7

[51] Int. Cl.
G06K 19/077 (2006.01)
H01L 27/02 (2006.01)
H01L 23/482 (2006.01)
H01L 23/60 (2006.01)
H05K 9/00 (2006.01)

[43] 公开日 2008 年 7 月 16 日

[11] 公开号 CN 101221629A

[22] 申请日 2008.1.2
[21] 申请号 200810002239.7
[30] 优先权
[32] 2007. 1.10 [33] US [31] 11/651,870
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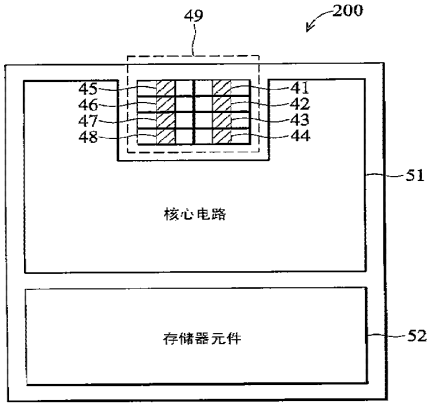
权利要求书 2 页 说明书 7 页 附图 5 页

[54] 发明名称

智能卡芯片以及放置输入/输出焊盘的方法

[57] 摘要

一种智能卡芯片以及放置输入/输出焊盘的方法，该智能卡芯片包括用于向智能卡读取器传送数据的多个电性接点。 在一个实施例中，智能卡芯片包括核心电路以及对应于电性接点的多个输入/输出焊盘，其中输入/输出焊盘划分成至少一个第一列以及放置成与第一列直接相邻的第二列，使得第一列以及第二列形成丛聚。 在另一个实施例中，八个输入/输出焊盘被划分成彼此直接相邻的两列。 丛聚可被核心电路部分地包围。 芯片还可包括静电放电网络，包括 VDD 以及 GND 总线，以改善静电放电保护而减少芯片的尺寸。 本发明能够大幅减少芯片尺寸，而仍然提供极佳的静电放电功能，并且不限定芯片内丛聚的配置；此外，本发明能够容易地与芯片内电压稳压器整合。



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1.一种智能卡芯片，包括用于向智能卡读取器传送数据的多个电性接点，上述智能卡芯片包括：

核心电路；以及

多个输入/输出焊盘，对应于所述电性接点，其中所述输入/输出焊盘划分成至少一个第一列以及放置成与所述第一列直接相邻的第二列，使得所述第一列以及所述第二列形成丛聚。

2．如权利要求 1 所述的智能卡芯片，其中所述第一列或所述第二列具有至少四个输入/输出焊盘。

3．如权利要求 1 所述的智能卡芯片，其中所述丛聚被所述核心电路的三个邻近侧部分地包围。

4．如权利要求 1 所述的智能卡芯片，其中所述多个输入/输出焊盘包括电源焊盘、接地焊盘、串行数据传送焊盘、时钟信号焊盘、复位焊盘、冗余电源焊盘以及冗余接地焊盘，并且所述输入/输出焊盘放置在所述丛聚内，以使得所述串行数据传送焊盘、所述时钟信号焊盘以及所述复位焊盘被所述电源焊盘、所述冗余电源焊盘、所述接地焊盘以及所述冗余接地焊盘部分地围住。

5．如权利要求 4 所述的智能卡芯片，还包括：静电放电网络，包括电性连接至所述电源焊盘的至少一个 VDD 总线，以及电性连接至所述接地焊盘的至少一个 GND 总线，使得所述 VDD 总线与所述 GND 总线放置成大体上平行于所述第一列与所述第二列，其中所述 VDD 总线放置在所述丛聚的各侧并且所述 GND 总线放置在所述第一列与所述第二列之间，其中各所述输入/输出焊盘经由静电放电单元而至少耦接至所述 GND 总线或耦接至至少一个 VDD 总线，以提供变短的静电放电的放电路径。

6．如权利要求 5 所述的智能卡芯片，还包括：VDD/GND 保护环结构，用于防止闩锁；以及至少一个或多个边缘单元，具有所述 VDD/GND 保护环结构。

7．一种放置输入/输出焊盘的方法，适用于包括核心电路以及用于向智能卡读取器传送数据的多个输入/输出焊盘的智能卡芯片，所述方法包括以下

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步骤：

将所述输入/输出焊盘划分成至少一个第一列以及第二列，所述第一列以及所述第二列具有相同数量的输入/输出焊盘；以及

将所述第一列以及所述第二列放置成彼此直接相邻，以在所述核心电路内形成丛聚。

8．如权利要求 7 所述的放置输入/输出焊盘的方法，其中所述丛聚被所述核心电路的至少三个邻近侧部分地包围。

9．如权利要求 7 所述的放置输入/输出焊盘的方法，其中所述第一列包括至少一个接地焊盘以及串行数据传送焊盘。

10．如权利要求 9 所述的放置输入/输出焊盘的方法，其中所述第二列包括至少一个电源焊盘、复位焊盘以及时钟信号焊盘。

11．如权利要求 10 所述的放置输入/输出焊盘的方法，其中所述接地焊盘以及所述电源焊盘被放置成彼此直接相邻，以减少电源或接地总线的绕线面积，并通过减少电源或接地总线的电阻来改善静电放电的功能。

12．如权利要求 10 所述的放置输入/输出焊盘的方法，其中所述丛聚还包括冗余接地焊盘以及冗余电源焊盘。

13．如权利要求 12 所述的放置输入/输出焊盘的方法，其中所述输入/输出焊盘放置在所述丛聚内，以使得所述串行数据传送焊盘、所述时钟信号焊盘以及所述复位焊盘被所述电源供应焊盘、所述冗余电源供应焊盘、所述接地焊盘以及所述冗余接地焊盘部分地围住。

14．如权利要求 7 所述的放置输入/输出焊盘的方法，其中所述丛聚还包括至少一个或多个测试焊盘，以及来自电压稳压器的输入的焊盘，以允许容易地与芯片内电压稳压器整合。

15．如权利要求 7 所述的放置输入/输出焊盘的方法，其中所述丛聚还包括至少一个或多个边缘单元，具有保护环结构以防止闩锁。

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智能卡芯片以及放置输入/输出焊盘的方法

技术领域

本发明涉及智能卡（smart card）芯片，特别涉及智能卡内所使用芯片的输入/输出焊盘（pad）的配置，用以改善静电放电（electrostatic discharge，ESD）功能并减少芯片的布局面积。

背景技术

智能卡是一种内嵌集成电路（integrated circuit）芯片的塑胶卡片型式的卡，集成电路芯片可包括非易失性（non-volatile）存储器存储元件以及一些其他特定的安全逻辑电路。智能卡增强系统广泛使用在保健、银行业务、娱乐以及运输等范围。

智能卡包括接触卡、无接触（contactless）卡以及混合（hybrid）卡。无接触卡使用射频（radio frequency，RF）来进行卡片与卡片读取器之间的传送。接触卡以及混合卡包括位于卡片外侧的一组电性接点，用以插入且耦接于卡片读取器。

智能卡传统上包括芯片，其中芯片包括微处理器以及可经由电性接点进行存取的存储器，例如：随机存取存储器（Random Access Memory，RAM）、只读存储器（Read Only Memory，ROM）以及电可擦可编程只读存储器(Electrically Erasable Programmable Read Only Memory，EEPROM)。接点提供电源、串行数据（serial data）传送的输入/输出、用以读取智能卡时钟（clock，CLK）信号的连接、用以复位（reset，RST）智能卡的连接以及智能卡的编程电压（programming voltage）的连接。这些接点的尺寸、功能以及位置由工业标准 ISO 7816-2 以及 7816-3 来规定（参考图 1A）。上述标准可允许不同的制造商生产可互相兼容的智能卡以及装置。

图 1B 示出智能卡的输入以及输出（I/O）焊盘的传统布局。然而，图 1B 布局中的主要缺点是需要越过芯片（cross-chip）的 VDD/GND（或是图 1B 中 VCC/GND）总线金属连接来提供足够的静电放电保护网络。越过芯片的

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VDD/GND 总线金属连接会增加芯片的尺寸，所以不是令人满意的解决方案。

嵌入在智能卡内的芯片传统上是由互补金属氧化物半导体（complementary metal oxide semiconductor，CMOS）技术制造的，并需要免于受到静电放电的损害。当智能卡被到处携带、从皮夹内放入和取出并插入至卡片读取器时，静电电荷会累积在智能卡上。当足够的电荷累积在智能卡的特定尖端时，电荷将被传导至最低电位的电压（传统为接地端）。在累积电荷的尖端到较低电位的路径上，当电荷足够高时会损害芯片。与芯片所能承受的最大电压或电流相比，例如：金属氧化物半导体的栅极氧化物可能被仅略高于一般供应电压（5 伏特、3.3 伏特或甚至更低）的电压所破坏，由累积电荷所感应的电压和电流可能相当大，例如：2000 伏特甚至更大的电压，或是越过 1.5k 欧姆的电阻的 1.3 安培以上甚至更大的电流。

传统上将静电放电保护电路加入到芯片的结合焊盘（bond pad）上，其中结合焊盘为提供芯片耦接至外部电路、电力供应、接地端以及电信号的连接。静电放电保护电路必须能够允许芯片正常操作，使得静电放电保护电路在芯片正常操作期间能有效地与芯片的核心电路隔离。

具有四种 P 型以及 N 型半导体材料可选择层的半导体元件或被称为可控硅整流器（silicon controlled rectifier，SCR）的 PNPN 元件可以是静电放电保护电路中能防止静电放电产生损害的最有效的元件之一。可控硅整流器操作在两种模式：阻隔（blocking）模式以及闩锁（latch up）模式。在阻隔模式中，可控硅整流器会阻挡电流通过，使得静电放电保护电路不会对要被保护的核心电路造成影响。当可控硅整流器内有足够的电流再生时，闩锁情况被触发。闩锁出现在互补寄生双极性晶体管结构中，其传统上存在于互补金属氧化物半导体结构内。既然互补寄生双极性晶体管非常靠近，互补双极性结构即能互相电性作用，从而形成动作表现如 PNPN 二极管的元件结构。静电放电事件中，大电流能流经可控硅整流器从而越过核心电路。

然而，无论使用何种结构作为静电放电保护电路，智能卡上的传统芯片还是必须包括会增加芯片尺寸的越过芯片的 VDD/GND 总线金属连接（参考图 1B）。

因此，在智能卡设计的技术中，需要能够对智能卡内所使用的芯片的输入/输出焊盘提供有效空间布局的新设计。

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发明内容

本发明涉及智能卡芯片，特别涉及智能卡内所使用芯片的输入/输出焊盘的配置，用以改善静电放电功能并减少芯片的布局面积。仅作为示例来说，本发明可用于智能卡内所使用的芯片上。然而，本领域技术人员可认识到，本发明还具有更大范围的实用性。

在一个特定实施例中，本发明提供一种具有新输入/输出焊盘配置的智能卡芯片。在一个实施例中，智能卡芯片包括核心电路。芯片还包括对应于上述电性接点的多个输入/输出焊盘，其中上述输入/输出焊盘划分成至少一个第一列以及放置成与上述第一列直接相邻的第二列，使得上述第一列以及上述第二列形成丛聚。

上述智能卡芯片中，第一列或第二列可具有至少四个输入/输出焊盘。

上述智能卡芯片中，丛聚可被核心电路的三个邻近侧部分地包围。

上述智能卡芯片中，多个输入/输出焊盘可包括电源焊盘、接地焊盘、串行数据传送焊盘、时钟信号焊盘、复位焊盘、冗余电源焊盘以及冗余接地焊盘，并且所述输入/输出焊盘放置在所述丛聚内，以使得串行数据传送焊盘、时钟信号焊盘以及复位焊盘被电源焊盘、冗余电源焊盘、接地焊盘以及冗余接地焊盘部分地围住。

上述智能卡芯片还可包括：VDD/GND 保护环结构，用于防止闩锁；以及至少一个或多边缘单元，具有 VDD/GND 保护环结构。

在另一个实施例中，公开一种放置输入/输出焊盘的方法，适用于包括核心电路以及与智能卡读取器传送数据的多个输入/输出焊盘的智能卡芯片。上述方法包括将上述输入/输出焊盘划分成至少一个第一列以及第二列，上述第一列以及上述第二列具有相同数量的输入/输出焊盘。上述方法还包括将上述第一列以及上述第二列放置成彼此直接相邻，以在上述核心电路内形成丛聚。

上述放置输入/输出焊盘的方法中，丛聚可被核心电路的至少三个邻近侧部分地包围。

上述放置输入/输出焊盘的方法中，第一列可包括至少一个接地焊盘以及串行数据传送焊盘。

上述放置输入/输出焊盘的方法中，第二列可包括至少一个电源焊盘、复位焊盘以及时钟信号焊盘。

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上述放置输入/输出焊盘的方法中，接地焊盘以及电源焊盘可放置成彼此直接相邻，以减少电源或接地总线的绕线面积，并通过减少电源或接地总线的电阻来改善静电放电的功能。

上述放置输入/输出焊盘的方法中，从聚还可包括冗余接地焊盘以及冗余电源焊盘。

上述放置输入/输出焊盘的方法中，输入/输出焊盘可放置在从聚内，以使得串行数据传送焊盘、时钟信号焊盘以及复位焊盘被电源供应焊盘、冗余电源供应焊盘、接地焊盘以及冗余接地焊盘部分地围住。

上述放置输入/输出焊盘的方法中，从聚还可包括至少一个或多个测试焊盘，以及来自电压稳压器的输入的焊盘，以允许容易地与芯片内电压稳压器整合。

上述放置输入/输出焊盘的方法中，从聚还可包括至少一个或多个边缘单元，具有保护环结构以防止闩锁。

在又一个实施例中，芯片包括静电放电网络，其包括电性连接至上述电源焊盘的至少一个 VDD 总线，以及电性连接至上述接地焊盘的至少一个 GND 总线，上述 VDD 总线与上述 GND 总线被放置成大体上平行于上述输入/输出焊盘的上述列。上述 VDD 总线可被放置在上述 cluster 的各侧且上述 GND 总线被放置在上述列之间，其中各上述输入/输出焊盘经由静电放电单元而至少耦接至上述 GND 总线或 VDD 总线，因此提供从上述输入/输出焊盘至上述 GND 总线或 VDD 总线直至接地端的短路径。

对客户芯片而言，既然不需要越过芯片的 VDD/GND 总线连接，所以优于传统相关技术的新配置的优点之一是芯片尺寸至少可减少 3%至 5%。另一个优点包括本发明可改善静电放电功能。既然从聚可被放置在芯片内的任何地方，因此可容易地与芯片内电压稳压器整合。

附图说明

图 1A 示出根据 ISO 标准的智能卡接点的简单布局图；

图 1B 示出智能卡芯片中输入/输出焊盘的传统配置的简单布局图；

图 2 示出根据本发明一个实施例所述智能卡芯片中输入/输出焊盘的配置的简单布局图；

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图 3 示出根据本发明另一个实施例所述智能卡芯片中输入/输出焊盘的配置的放大布局图；以及

图 4 示出根据本发明又一个实施例所述智能卡芯片中输入/输出焊盘的配置以及静电放电网络的简单布局图。

其中，附图标记说明如下：

1-8~电性接点

10-11~距离

100~图示

102、200~芯片

21-28、41-48~输入/输出焊盘

29、30~列

31、51~核心电路

32、52~存储器元件

33、34~越过芯片的 VDD/GND 总线连接

400~布局视图

49、300~丛聚

61-65、70~焊盘

68~冗余接地焊盘

69~冗余电源焊盘

71、72~测试焊盘

73~丛聚边缘单元

80~静电放电网络

81、82~VDD 总线

83~GND 总线

86-97~静电放电保护元件

9~智能卡边缘

具体实施方式

为让本发明的上述和其他目的、特征、和优点能更明显易懂，下文特举出较佳实施例，并配合所附图式，作详细说明如下：

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实施例：

图 1A 示出根据 ISO 标准的智能卡接点的简单布局图。如图 1A 所示，图示 100 示出 ISO 标准中与智能卡边缘 9 的电性接点 1-8 相关的配置。接点 1 与接点 5 被设计成耦接至供应电源以及接地端。接点 7 作为串行数据的输入/输出焊盘。接点 3 作为用以读出智能卡时钟信号的连接。接点 2 作为用以复位智能卡的连接，而接点 6 用于智能卡的编程电压的连接。接点的配置分别由从智能卡上边以及左边的一组距离 10 与距离 11 来决定。接点 4 以及接点 8 保留给将来使用。

图 1B 示出智能卡芯片中输入/输出焊盘的传统配置的简单布局图。图 1A 所示出的 ISO 标准接点 1-8 的配置会导致如图 1B 所示的智能卡芯片的输入/输出焊盘的传统配置。传统上，芯片 102 具有位于芯片 102 边缘、划分成列（column）29 与列 30、并由核心电路 31 分隔的输入/输出焊盘 21-28。

芯片 102 还包括存储器元件 32。核心电路 31 与存储器元件 32 均对静电放电非常敏感，因此芯片 102 也必须包括由越过芯片的 VDD/GND 总线连接 33、34 构成的足够的静电放电保护电路。上述越过芯片的 VDD/GND 总线连接会显著增加芯片的总面积以及总线电阻。

图 2 示出根据本发明一个实施例的智能卡芯片中输入/输出焊盘的配置的简单布局图。参考图 2，其示出智能卡的输入/输出焊盘 41-48 的布局。与传统配置相比，列 29 与列 30（参考图 1B）被放置成彼此直接紧邻，并组成丛聚（cluster）49。通过修改核心电路 51 的形状，就能部分地包围丛聚 49（以及输入/输出焊盘 41-48）。芯片 200 还包括存储器元件 52。全部的输入/输出焊盘 41-48 还聚集在丛聚 49 的相连区域内。

图 3 示出根据本发明另一个实施例的智能卡芯片中输入/输出焊盘的配置的放大布局图。丛聚 300 包括作为电源（VDD）的焊盘 61、用以复位芯片的焊盘 62（RST）、用以读取芯片的脉冲信号的焊盘 63（CLK）、作为接地端的焊盘 64，以及与芯片传送串行数据的焊盘 65（IO）。然而，与图 2 中的丛聚 49 相比，丛聚 300 额外地包括冗余接地焊盘（Dummy GND）68、冗余电源焊盘（Dummy VDD）69、作为来自电压稳压器的输入的焊盘 70（VDDC）以及测试焊盘 71（TEST PAD_1）与测试焊盘 72（TEST PAD_2）。丛聚边缘单元 73 包括 VDD/GND 保护环（guard ring）结构以防止闩锁现象。

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如图 3 所示，分别作为电源以及接地的焊盘 61 与焊盘 64 被放置成背对背。增加冗余接地焊盘 68 以及冗余电源焊盘 69 以改善静电放电保护功能，使得焊盘 62、焊盘 63 与焊盘 65 被 VDD/GND 焊盘（焊盘 61、64）以及冗余 VDD/GND 焊盘（焊盘 68、69）所包围。

图 4 示出根据本发明另一个实施例的智能卡芯片中输入/输出焊盘的配置以及静电放电网络的简单布局图。图 4 示出图 3 中智能卡芯片内输入/输出焊盘的配置以及静电放电网络 80 的布局视图 400。静电放电网络 80 包括作为主要静电放电总线的 VDD 总线 81、82 以及 GND 总线 83。静电放电网络 80 还包括多个静电放电保护元件 86-97（例如可控硅整流器），静电放电保护元件 86-97 分别耦接于焊盘 61-68 以及 VDD 总线 81、82 与 GND 总线 83 之间，用以例如当使用者意外地接触到智能卡的接触点时，保护各输入/输出端免于任何意外的静电放电。

可以了解到，包括焊盘 64、65 的第一组结合焊盘以及包括焊盘 61-63 的第二组结合焊盘被静电放电金属总线（GND）包围在两侧。耦接于第一组结合焊盘以及第二组结合焊盘之间的静电放电金属总线（VDD）经由背对背的 VDD/GND 与冗余 VDD/GND 与边缘单元相邻。与现有技术相比，上述设计提供变短的全面静电放电路径以将电荷传导至接地端。本领域技术人员可认识到，VDD 总线以及 GND 总线越短，则电阻越低且放电速度越快。

本发明排除了对于越过芯片的 VDD/GND 总线连接的需要，因此大幅地减少了芯片尺寸（在客户芯片上大约减少 3％至 5％），而仍然提供极佳的静电放电功能。由于 VDD 总线以及 GND 总线的电阻减少，本发明还提供较佳的静电放电保护功能，且没有限定芯片内丛聚的配置。另外，本发明能够容易地与芯片内电压稳压器（voltage regulator，VR）整合，以提供额外的冗余接地焊盘以及其他电源焊盘，如图 3 所示。

上述说明提供许多不同的实施例或是用以实施本发明不同特征的实施例。描述构成以及步骤的特定实施例可帮助理解本发明。当然，上述说明只是实施例，并没有打算在权利要求意义上限定本发明。

本发明虽以优选实施例公开如上，然而所公开内容并非用以限定本发明的范围，任何本领域技术人员，在不脱离本发明的精神和范围内，当可做一定的更动与修改，因此本发明的保护范围应以所附权利要求为准。

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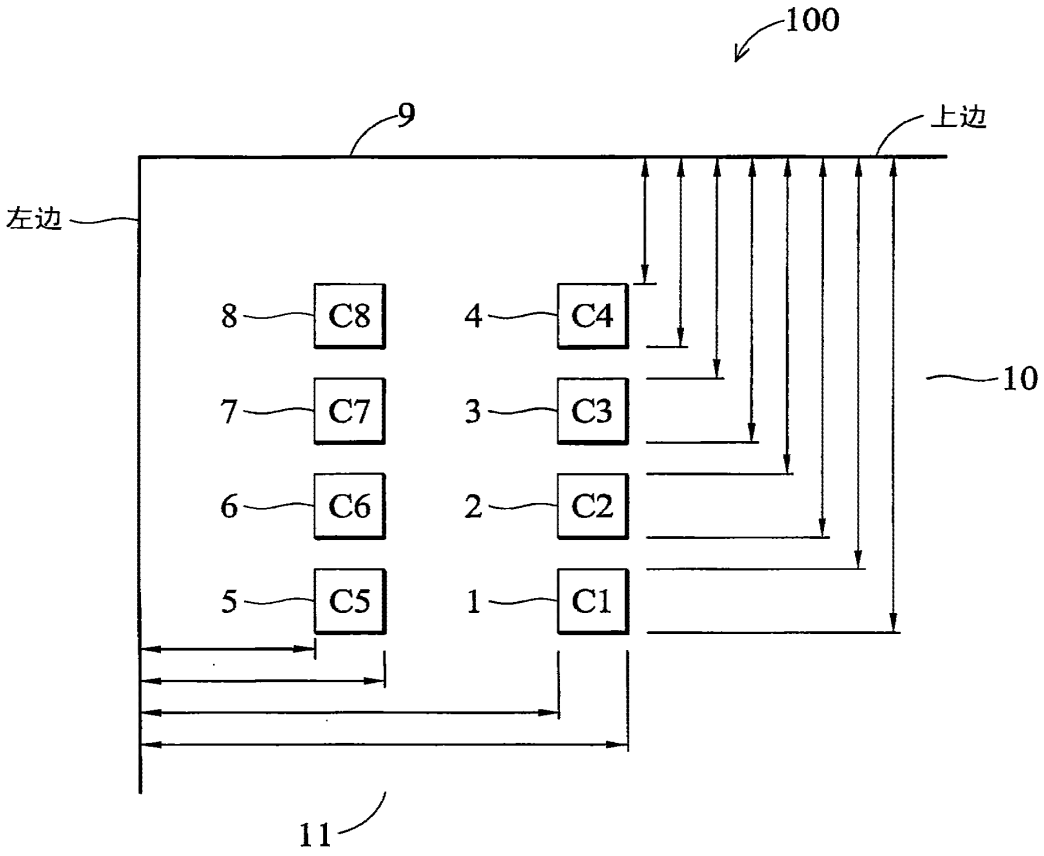


图1A

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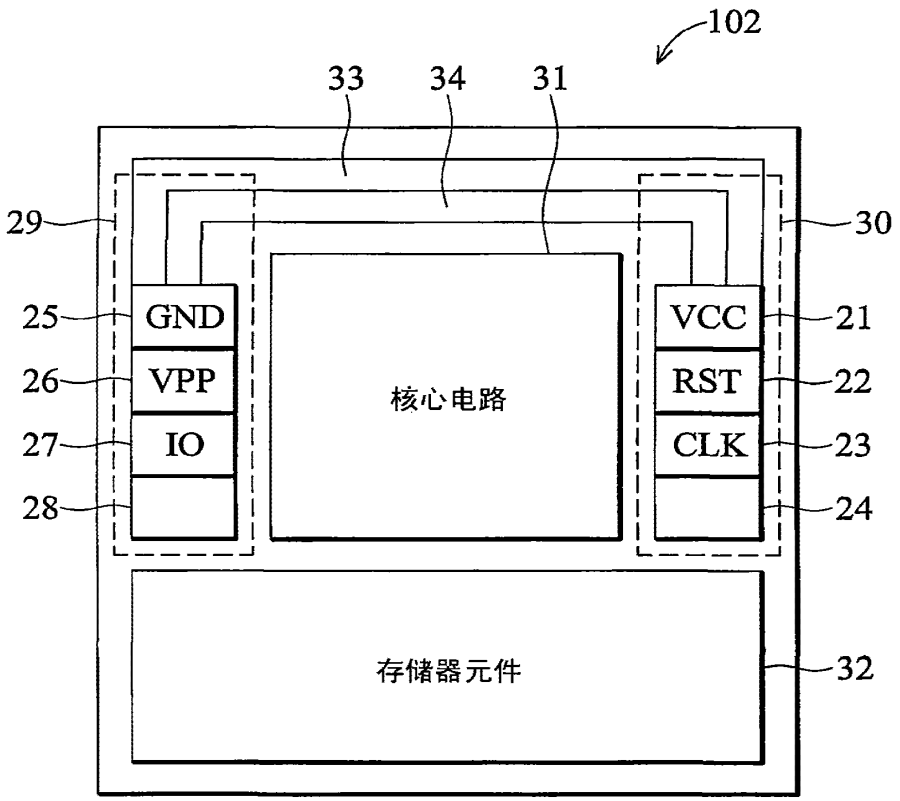


图1B

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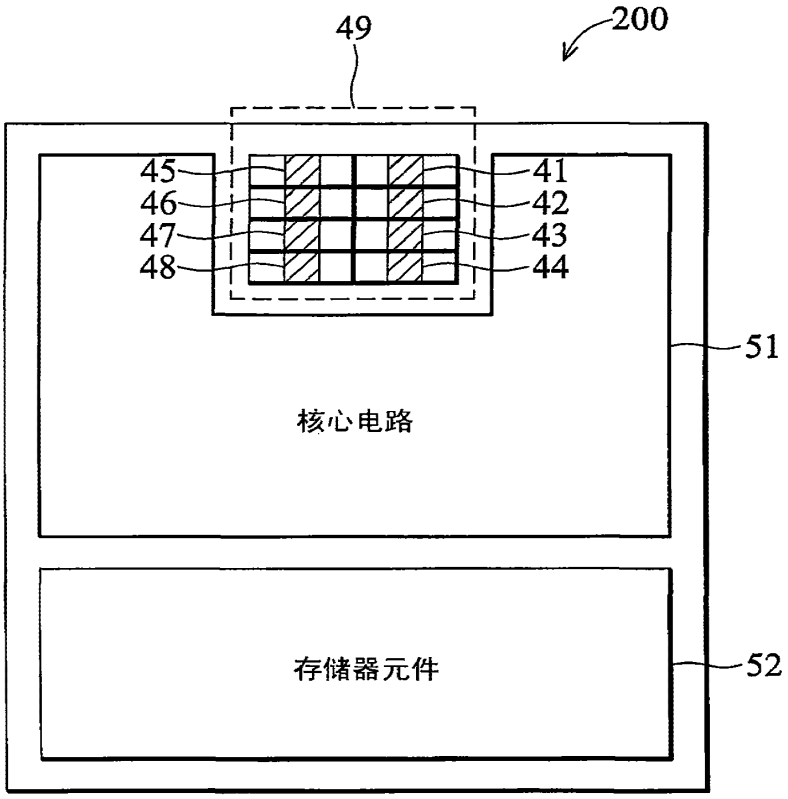


图2

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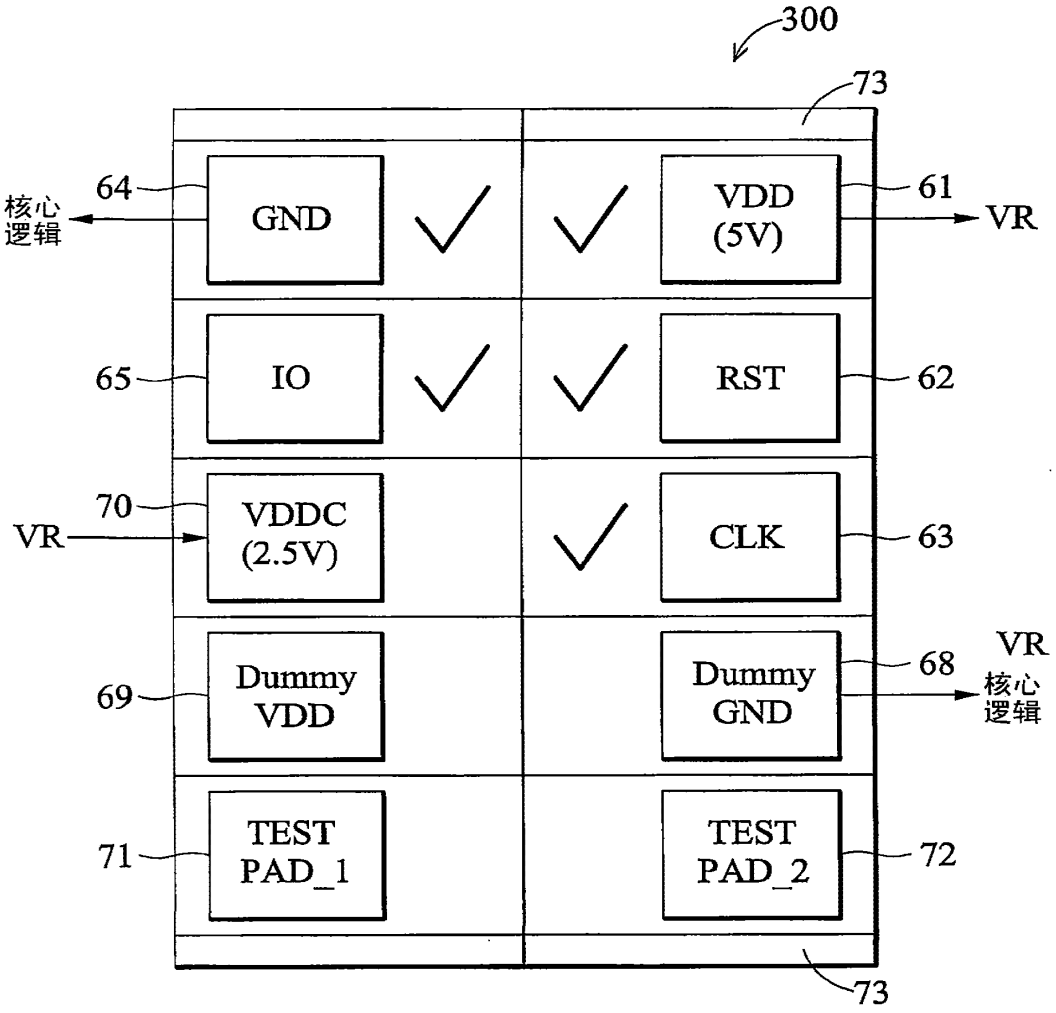


图3

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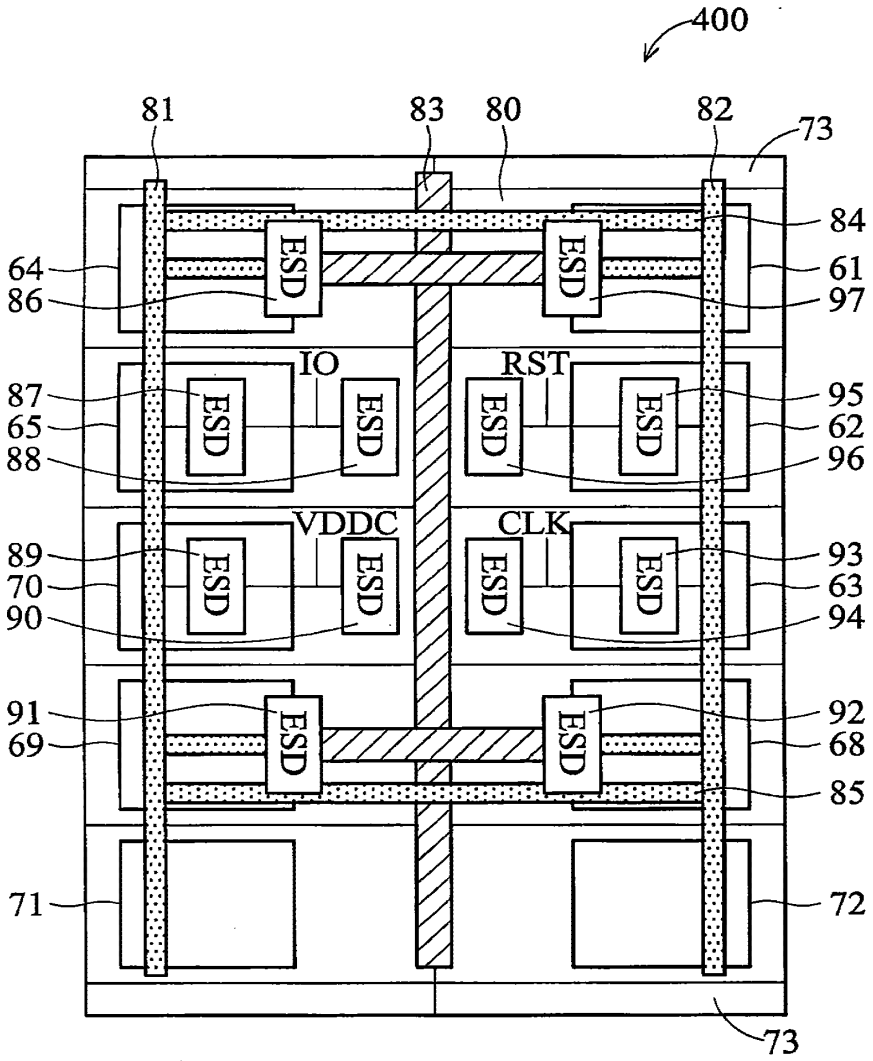


图4

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Abstract of CN102054523

The invention discloses an input/output (I/O) unit and an integrated circuit chip. The I/O unit comprises an N type electrostatic discharge protection circuit, a P type electrostatic discharge protection circuit, a bonding pad and an I/O logic circuit which are distributed transversely, wherein the N type electrostatic discharge protection circuit is isolated from the P type electrostatic discharge protection circuit by the bonding pad; the N type electrostatic discharge protection circuit is connected with a ground wire; and the P type electrostatic discharge protection circuit is connected with a power wire. The area of the I/O unit is small and a larger layout wiring area is correspondingly provided for a core circuit region of the integrated circuit chip, so that the layout wiring difficulty of the core circuit region is lowered. Under the condition of certain core circuit area, the integrated circuit chip which comprises the I/O unit has a smaller area.

(19)中华人民共和国国家知识产权局

(12)发明专利申请

(10)申请公布号 CN 102054523 A
(43)申请公布日 2011.05.11

(21)申请号 200910198462.8

(22)申请日 2009.11.04

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(51)Int.Cl.
G11C 7/24(2006.01)

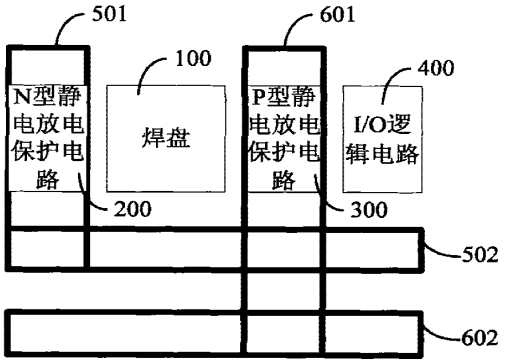
权利要求书 1 页 说明书 3 页 附图 4 页

(54)发明名称

I/O 单元及集成电路芯片

(57)摘要

一种 I/O 单元及集成电路芯片。所述 I/O 单元包括：横向分布的 N 型静电放电保护电路、P 型静电放电保护电路、焊盘以及 I/O 逻辑电路，其中 N 型静电放电保护电路和 P 型静电放电保护电路由焊盘隔离，N 型静电放电保护电路与接地线相连，P 型静电放电保护电路与电源线相连。所述 I/O 单元的面积较小，相应提供给集成电路芯片的核心电路区域的可布局布线面积更大，减小了核心电路区域布局布线的难度。在核心电路面积一定的情况下，包括所述 I/O 单元的集成电路芯片具有更小的面积。



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1. 一种 I/O 单元，其特征在于，包括 ：横向分布的 N 型静电放电保护电路、P 型静电放电保护电路、焊盘以及 I/O 逻辑电路，其中 N 型静电放电保护电路和 P 型静电放电保护电路由焊盘隔离，N 型静电放电保护电路与接地线相连，P 型静电放电保护电路与电源线相连。

2. 如权利要求 1 所述的 I/O 单元，其特征在于，所述接地线包括第一接地线和第二接地线，所述第一接地线和第二接地线垂直相连，所述第一接地线和 N 型静电放电保护电路相连。

3. 如权利要求 2 所述的 I/O 单元，其特征在于，所述第一接地线覆盖 N 型静电放电保护电路。

4. 如权利要求 2 所述的 I/O 单元，其特征在于，所述电源线包括第一电源线和第二电源线，所述第一电源线和第二电源线垂直相连，所述第一电源线和 P 型静电放电保护电路相连。

5. 如权利要求 4 所述的 I/O 单元，其特征在于，所述第一电源线覆盖 P 型静电放电保护电路。

6. 一种包括权利要求 1 至 5 任一项所述的 I/O 单元的集成电路芯片，其中，各相邻 I/O 单元中相邻部分为同类型电路。

7. 一种包括权利要求 4 所述的 I/O 单元的集成电路芯片，其中，各相邻 I/O 单元中的第二接地线、第二电源线各自相连。

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I/O 单元及集成电路芯片

技术领域

[0001] 本发明涉及半导体集成电路设计领域，特别涉及 I/O 单元及集成电路芯片。

背景技术

[0002] 随着半导体器件功能的日趋复杂及尺寸的日趋减小，其所能承受的静电放电 (ESD，Electro Static Discharge) 电压的上限值也不断减小。因而，在半导体集成电路设计时，经常采用各种静电放电保护设计对于集成电路芯片内部的半导体器件进行保护。

[0003] 目前，比较常用的一种静电放电保护设计是在集成电路芯片的输入 / 输出 (I/O) 单元中集成静电放电保护电路，并将所述静电放电保护电路与 I/O 单元中的相应焊盘 (PAD) 相连。图 1 为现有技术的一种 I/O 单元的结构示意图。参照图 1 所示，所述 I/O 单元包括 ：纵向相邻分布的焊盘 10、N 型静电放电保护电路 20、P 型静电放电保护电路 30 及 I/O 逻辑电路 40。其中，N 型静电放电保护电路 20 指由 NMOS 管构成的静电放电保护电路，P 型静电放电保护电路 30 指由 PMOS 管构成的静电放电保护电路，I/O 逻辑电路 40 通常包括一些输入 / 输出的接口电路，例如电压泵等。所述 N 型静电放电保护电路 20 处布局有接地线 50，所述 P 型静电放电保护电路 30 处布局有电源线 60。所述 N 型静电放电保护电路 20 和所述 P 型静电放电保护电路 30 可根据实际的静电放电保护需求而择一与焊盘相连，或共同与焊盘相连。

[0004] 所述 I/O 单元由于其纵向相邻分布而具有较好的布局对称性，非常适合于采用这种 I/O 单元的集成电路芯片进行自动布局布线。图 2 所示为具有上述 I/O 单元的一种集成电路芯片结构示意图。参照图 2 所示，通过将所述 I/O 单元添加至自动布局布线软件的单元库中，则自动布局布线软件就可根据集成电路芯片 1 中核心电路的位置及剩余的可布局布线面积，对所述 I/O 单元的位置进行自动分配，并根据设计进行自动布线。

[0005] 然而，从图 2 中也可看到，虽然所述 I/O 单元的纵向相邻分布结构具有较好的布局对称性，但基于避免产生闩锁效应的设计规则，P 型静电放电保护电路和 N 型静电放电保护电路之间必需保留很大间距。如此，I/O 单元所占面积很大，使得集成电路芯片 1 的核心电路区域 (图 2 中虚线框范围) 的可布局布线面积很小，大大增加了所述核心电路区域的布局布线难度，因此在布局布线时会产生大量的空间浪费。同时，由于 I/O 单元所占面积很大造成了集成电路芯片 1 转角浪费的面积也很大，因此整个集成电路芯片 1 的面积会大大增加。

发明内容

[0006] 本发明解决现有技术包含静电放电保护电路的 I/O 单元面积较大，使得集成电路芯片中核心电路区域的可布局布线面积很小且集成电路芯片面积很大的问题。

[0007] 为解决上述问题，本发明提供一种 I/O 单元，包括 ：横向分布的 N 型静电放电保护电路、P 型静电放电保护电路、焊盘以及 I/O 逻辑电路，其中 N 型静电放电保护电路和 P 型静电放电保护电路由焊盘隔离，N 型静电放电保护电路与接地线相连，P 型静电放电保护电

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路与电源线相连。

[0008] 相应地，本发明还提供一种包括上述 I/O 单元的集成电路芯片，其中，各相邻 I/O 单元中相邻部分为同类型电路。

[0009] 与现有技术相比，上述 I/O 单元及集成电路芯片具有以下优点：灵活运用焊盘隔离了 N 型静电放电电路和 P 型静电放电电路，满足了避免产生闩锁效应的设计规则，则 I/O 单元的面积就可减小很多。相应地，也能够提供集成电路芯片中核心电路区域较大的可布局布线面积，减小了所述核心电路区域的布局布线的难度。

[0010] 并且，由于 I/O 单元面积的减小，在核心电路区域面积一定的情况下，所述集成电路芯片具有更小的面积。

附图说明

[0011] 图 1 是现有技术的一种 I/O 单元的结构示意图；

[0012] 图 2 是具有图 1 所示 I/O 单元的一种集成电路芯片的结构示意图；

[0013] 图 3 是本发明 I/O 单元的一种实施例的结构示意图；

[0014] 图 4 是图 3 所示 I/O 单元应用于集成电路芯片的一种实施例示意图。

具体实施方式

[0015] 参照图 3 所示，本发明 I/O 单元的一种实施例包括：横向相邻分布的 N 型静电放电保护电路 200、焊盘 100、P 型静电放电保护电路 300 以及 I/O 逻辑电路 400。其中，N 型静电放电保护电路 200 指由 NMOS 管构成的静电放电保护电路，P 型静电放电保护电路 300 指由 PMOS 管构成的静电放电保护电路，I/O 逻辑电路 400 通常包括一些输入 / 输出的接口电路，例如电压泵等。所述 N 型静电放电保护电路 200 与接地线连接。具体地说，所述接地线包括第一接地线 501 和第二接地线 502，所述第一接地线 501 和第二接地线 502 垂直相连，所述 N 型静电放电保护电路 200 与所述第一接地线 501 相连。所述 P 型静电放电保护电路 300 与电源线连接。具体地说，所述电源线包括第一电源线 601 和第二电源线 602，所述第一电源线 601 和第二电源线 602 垂直相连，所述 P 型静电放电保护电路 300 与所述第一电源线 601 相连。所述第一接地线 501 与 N 型静电放电保护电路 200 的连接方式以及第一电源线 601 与 P 型静电放电保护电路 300 的连接方式，可以是图 3 所示的第一接地线 501 覆盖所述 N 型静电放电保护电路 200、第一电源线 601 覆盖所述 P 型静电放电保护电路 300 的方式，也可以是通过导线连接的非覆盖的连接方式（图 3 未示）。此外，第二接地线 502 及第二电源线 602 的上下位置可根据实际设计需求而调整。

[0016] 上述实施例中，N 型静电放电保护电路 200 和 P 型静电放电保护电路 300 由焊盘 100 隔离，因此能够借用焊盘尺寸满足避免产生闩锁效应的设计规则。由此，所述 I/O 单元中的 N 型静电放电保护电路 200、焊盘 100、P 型静电放电保护电路 300 以及 I/O 逻辑电路 400 都可保持较小的间距。例如，可在集成电路芯片的设计要求允许的前提下，使得各部分都保持工艺上的最小间距。从而，所述 I/O 单元的面积就可较大程度地减小。

[0017] 以下通过图 3 所示 I/O 单元应用于集成电路芯片的实例进行进一步说明。

[0018] 参照图 4 所示，集成电路芯片 2 具有 6 个引脚，所述 6 个引脚各自通过集成电路芯片 2 中的 6 个 I/O 单元中的焊盘引出。所示 6 个 I/O 单元分布于所述集成电路芯片 2 的周

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边，其中一个 I/O 单元还分布于集成电路芯片 2 的转角处，各 I/O 单元中的第二接地线 502 和第二电源线 602 各自相连。并且，相邻的 I/O 单元中相邻部分均为同类型电路。例如，核心电路区域（虚线框范围）上方的两个相邻的 I/O 单元中，相邻部分都为 I/O 逻辑电路。而核心电路区域下方的三个相邻的 I/O 单元中，两个相邻部分分别都为 I/O 逻辑电路和 N 型静电放电保护电路。

[0019] 对比图 2 和图 4 可以发现，对于同样是 6 个引脚的集成电路芯片，本发明实施例的 I/O 单元相对于现有技术的 I/O 单元，不仅在集成电路芯片 2 的周边，而且在集成电路芯片 2 的转角处，其面积都有了较大的减小。

[0020] 具体地说，不同于现有技术的 I/O 单元结构，本实施例的 I/O 单元可以横向放置在集成电路芯片 2 中，大大减小了 I/O 单元所占的面积，I/O 单元所占面积的减小使得可用于核心电路布局布线的区域更趋于正方形，在降低布局布线难度的同时，可以使得这些布线区域的利用率最大化，也就减少了核心电路的面积。同时 I/O 单元所占面积的减小使得在集成电路芯片 2 转角处所用掉的转角面积也比以前大大减小。

[0021] 并且，图 4 中第二接地线 502 和第二电源线 602 都有各自独立的布线空间，其间并不包含任何电路，相应可选择更多的金属层来构成第二接地线 502 和第二电源线 602。从而，对于布线资源的调配也更有利。

[0022] 从另一方面来说，对于同样的核心电路面积，由于本发明实施例的 I/O 单元的面积远小于现有技术的 I/O 单元的面积，因此采用本发明实施例的 I/O 单元的集成电路芯片的面积也要远小于采用现有技术的 I/O 单元的集成电路芯片的面积。

[0023] 虽然本发明已以较佳实施例披露如上，但本发明并非限定于此。任何本领域技术人员，在不脱离本发明的精神和范围内，均可作各种更动与修改，因此本发明的保护范围应当以权利要求所限定的范围为准。

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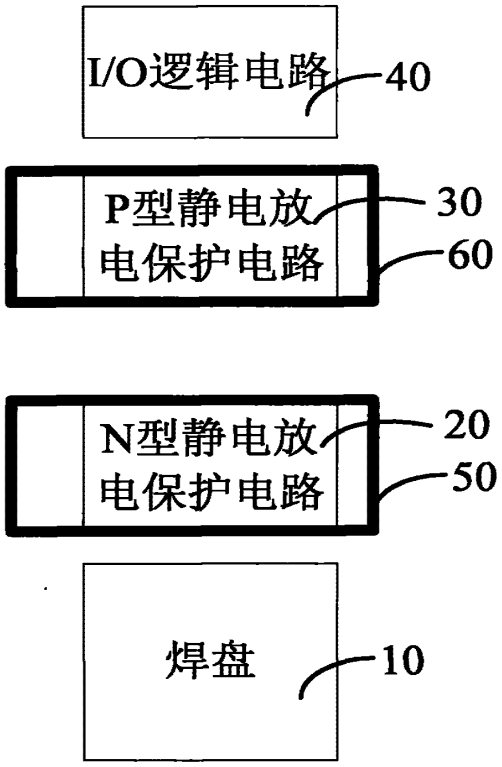


图 1

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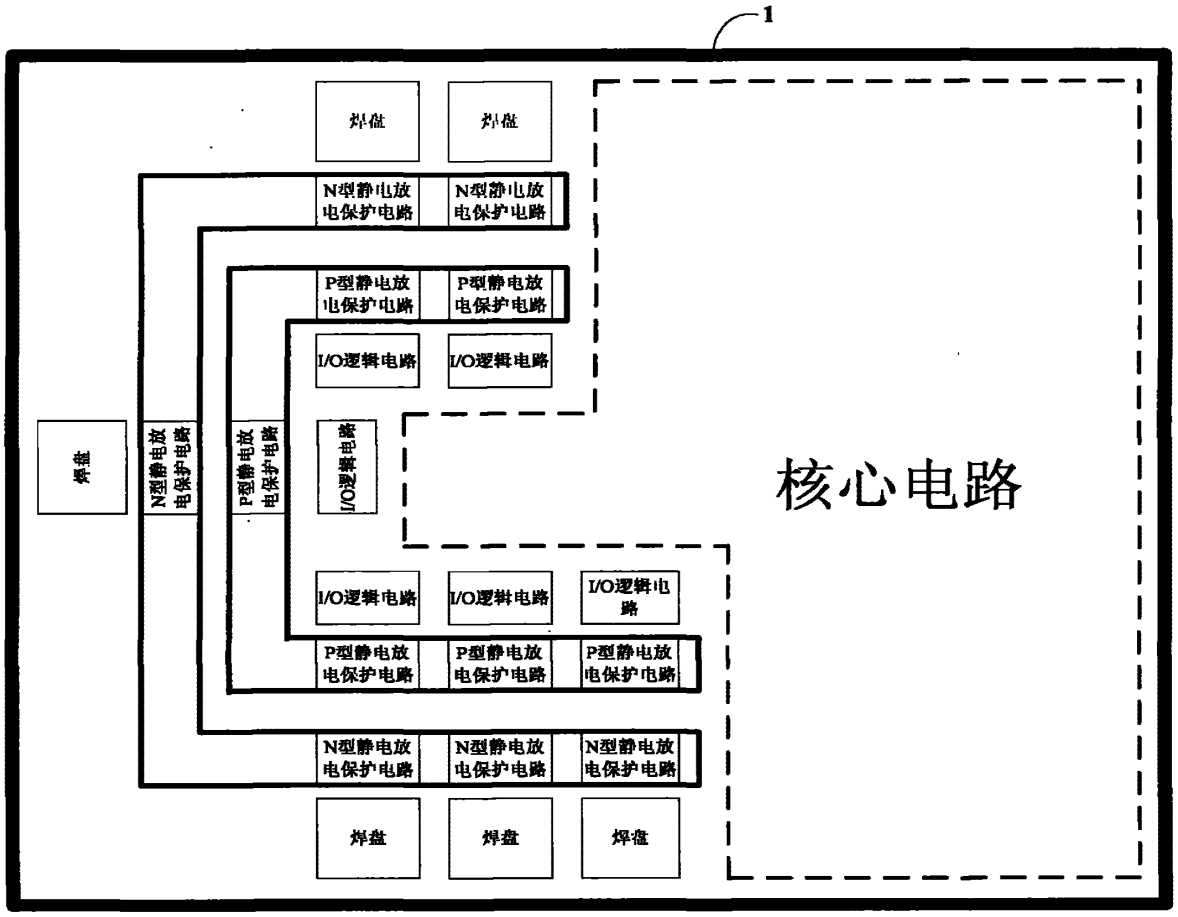


图 2

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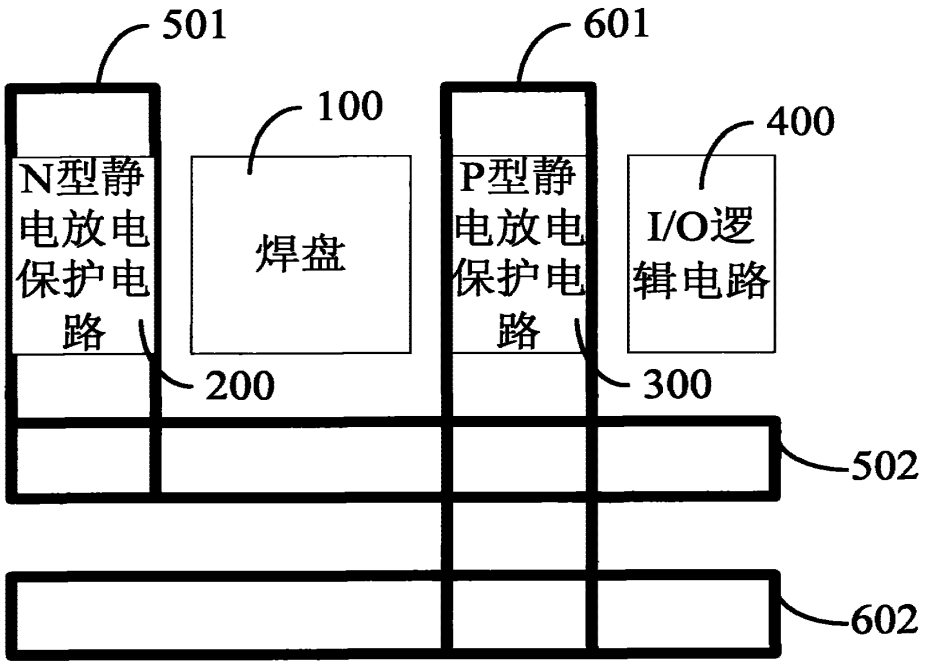


图 3

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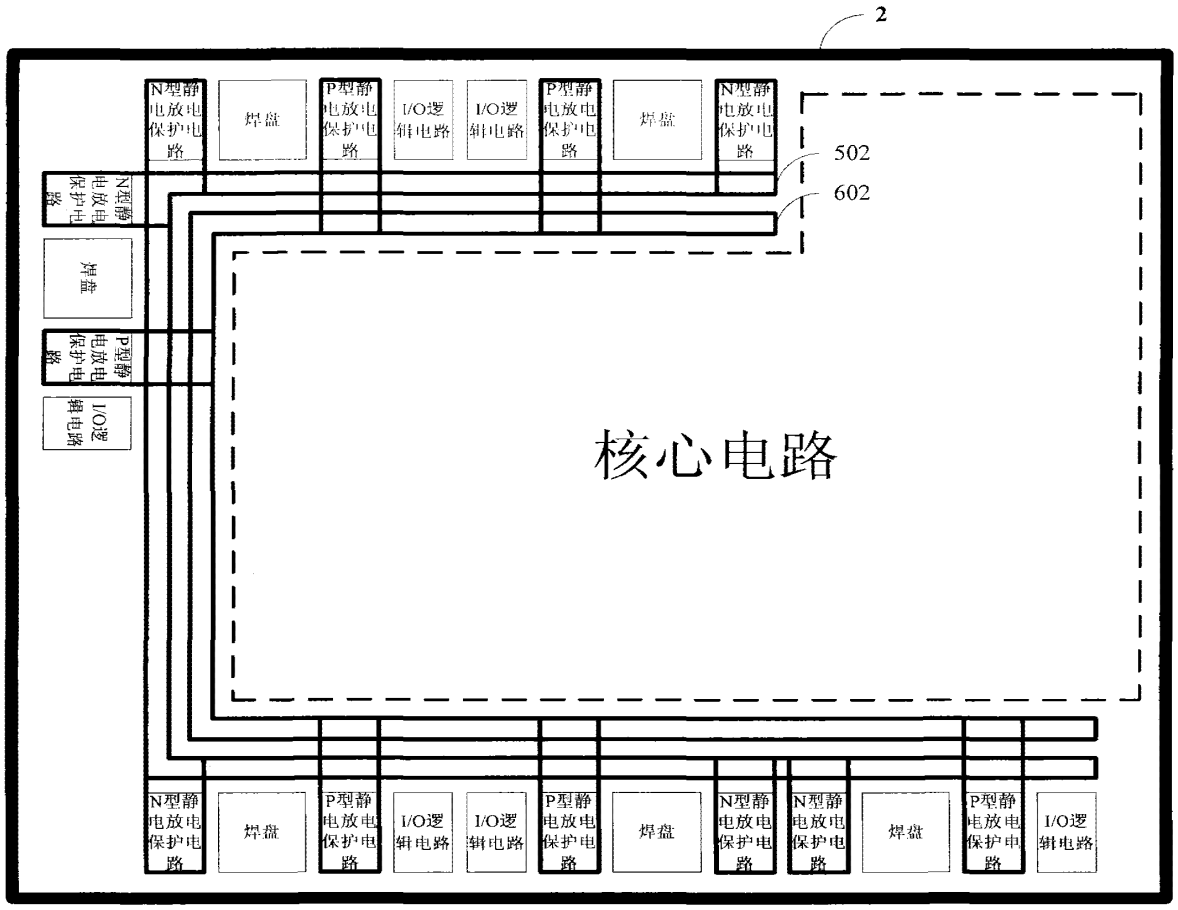


图 4

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Abstract of CN103681654

The invention provides a semiconductor device of ESD resistance while the width of the wiring pattern is not increased and the pin level of a chip of the semiconductor device is improved. A semiconductor device according to an embodiment includes a plurality of pads, a plurality of ESD protection circuits, each one of the ESD protection circuits being connected to a corresponding one of the plurality of pads, and an I/O circuit which is connected to a connection portion connecting output terminals of the plurality of ESD protection circuits to each other and which receives at least one input signal inputted into the plurality of pads..

(19)中华人民共和国国家知识产权局

(12)发明专利申请

(10)申请公布号 CN 103681654 A
(43)申请公布日 2014.03.26

(21)申请号 201310318354.6

(22)申请日 2013.07.26

(30)优先权数据
2012-198792 2012.09.10 JP

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(51)Int.Cl.
H01L 27/02(2006.01)
H01L 23/488(2006.01)

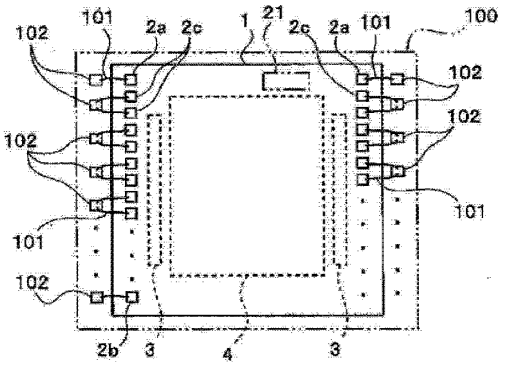
权利要求书2页 说明书7页 附图5页

(54)发明名称

半导体装置

(57)摘要

本发明提供一种能够不增加布线图案宽度而提高半导体装置的芯片的管脚级的ESD耐性的半导体装置。根据实施方式，半导体装置具有：多个焊盘；多个ESD保护电路，以使一个ESD保护电路对应于一个焊盘的方式，连接于多个焊盘；以及I/O电路，连接于将多个ESD保护电路的输出端彼此连接的连接部，输入向多个焊盘输入的至少一个输入信号。



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1. 一种半导体装置，具有：

多个第一焊盘；

多个 ESD 保护电路，以使一个 ESD 保护电路对应一个上述第一焊盘的方式连接于上述多个第一焊盘；以及

I / O 电路，连接于上述多个 ESD 保护电路的输出。

2. 根据权利要求 1 记载的半导体装置，

还具备与上述多个第一焊盘连接的外部电极，

上述多个第一焊盘通过键合引线分别与上述外部电极连接。

3. 根据权利要求 1 记载的半导体装置，还具有：

设置在上述多个第一焊盘间的开关部；以及

对上述开关部的开闭进行控制的开关控制部。

4. 根据权利要求 1 记载的半导体装置，

上述多个第一焊盘沿上述半导体芯片的至少一边配置为直线状。

5. 根据权利要求 1 记载的半导体装置，

上述多个第一焊盘配置在上述半导体装置的内部。

6. 根据权利要求 1 记载的半导体装置，

上述多个第一焊盘的一部分沿上述半导体芯片的至少一边配置为直线状，上述多个第一焊盘的剩余的一部分配置在上述半导体装置的内部。

7. 根据权利要求 5 记载的半导体装置，

配置在上述半导体装置的内部的上述多个第一焊盘层叠在配置有上述 ESD 保护电路的层之上。

8. 根据权利要求 6 记载的半导体装置，

配置在上述半导体装置的内部的上述多个第一焊盘层叠在配置有上述 ESD 保护电路的层之上。

9. 根据权利要求 2 记载的半导体装置，

上述外部电极包括球电极。

10. 根据权利要求 9 记载的半导体装置，

上述外部电极形成在与上述多个 ESD 保护电路不同的层上。

11. 根据权利要求 10 记载的半导体装置，

上述半导体装置以晶片级芯片尺寸封装 WLCSP 构成。

12. 根据权利要求 10 记载的半导体装置，

上述外部电极包括输入信号的电极。

13. 根据权利要求 5 记载的半导体装置，

上述半导体装置的半导体芯片具有矩形状，

上述多个第一焊盘沿与矩形的上述半导体芯片的至少一边正交的方向配置。

14. 根据权利要求 6 记载的半导体装置，

上述半导体装置的半导体芯片具有矩形状，

上述多个第一焊盘沿与矩形的上述半导体芯片的至少一边正交的方向配置。

15. 一种半导体装置，具备：

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至少一个焊盘；

多个 ESD 保护电路；

开关部，插入上述多个 ESD 保护电路的输入部之间；以及

I / O 电路，连接有上述多个 ESD 保护电路的输出端，

上述一个焊盘，与直接连接的第一 ESD 保护电路、和通过将上述开关部闭合而电连接的至少一个第二 ESD 保护电路连接。

16. 根据权利要求 15 记载的半导体装置，

还具备与上述多个第一焊盘连接的外部电极，

上述多个第一焊盘通过键合引线分别与上述外部电极连接。

17. 根据权利要求 16 记载的半导体装置，

上述外部电极包括球电极。

18. 根据权利要求 17 记载的半导体装置，

上述外部电极形成在与上述多个 ESD 保护电路不同的层上。

19. 根据权利要求 18 记载的半导体装置，

上述半导体装置以晶片级芯片尺寸封装 WLCSP 构成。

20. 根据权利要求 16 记载的半导体装置，

上述外部电极包括输入信号的电极。

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半导体装置

[0001] 本申请享受 2012 年 9 月 10 日申请的日本专利申请第 2012 — 198792 的优先权，并在本申请中引用该日本专利申请的全部内容。

技术领域

[0002] 本发明的实施方式涉及半导体装置。

背景技术

[0003] 在电子设备中，由于静电放电（Electro-Static Discharge：以下称为 ESD）引起的静电破坏而采取用来保护电路的 ESD 对策。

[0004] 为了评价 ESD 对策，以往按照设备或模块的级别（level），基于 HBM（人体模式，human body mode）、MM（机器模式，machine mode）来进行 ESD 耐性评价。例如，对于评价对象的设备或模块，在 HBM 下施加 2KV ～ 3KV 的电压，在 MM 下施加 200V 的电压，来进行 ESD 耐性评价。

[0005] 此外，以往，对于搭载了半导体装置的电子设备或模块的级别，例如还依照 IEC — 61000 — 4. 2 的 ESD 规格，在接触放电下施加 8KV 的电压，在气体放电下施加 15KV 的电压，来进行 ESD 耐性评价，然而最近，有时即使是半导体装置的芯片的管脚级也需要依照上述规格的同样的 ESD 耐性评价。

[0006] 通常，在芯片的管脚级，为了满足规定规格的 ESD 耐性条件，在 I / O 设计中，需要电源箝位（power clamp）电路的功能提高、或增加布线图案的宽度来降低布线电阻这样的对策。

[0007] 但是，布线图案宽度的增加这一方法，不仅给芯片的布局设计带来大的制约，而且作为结果，存在导致芯片面积的增加、以及芯片的成本增加的问题。

发明内容

[0008] 本发明要解决的课题在于，提供一种能够不增加布线图案宽度而提高半导体装置的芯片的管脚级的 ESD 耐性的半导体装置。

[0009] 实施方式的半导体装置，具有：多个第一焊盘；多个 ESD 保护电路，以使一个 ESD 保护电路对应一个上述第一焊盘的方式连接于上述多个第一焊盘；以及 I / O 电路，连接于上述多个 ESD 保护电路的输出。

[0010] 此外，另一实施方式的半导体装置，具备：至少一个焊盘；多个 ESD 保护电路；开关部，插入上述多个 ESD 保护电路的输入部间；以及 I / O 电路，连接有上述多个 ESD 保护电路的输出端；

[0011] 上述一个焊盘，与直接连接的第一 ESD 保护电路、和通过将上述开关部闭合而电连接的至少一个第二 ESD 保护电路连接。

[0012] 根据上述结构的半导体装置，能够不增加布线图案宽度而提高半导体装置的芯片的管脚级的 ESD 耐性。

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附图说明

[0013] 图 1 是表示实施方式的半导体装置的芯片布局概念的图。

[0014] 图 2 是用来说明实施方式的半导体装置被搭载在半导体封装中的状态的图。

[0015] 图 3 是用来说明实施方式的芯片 1 的包含 ESD 保护电路 12 的 I/O 部的结构的电路图。

[0016] 图 4 是用来说明实施方式的半导体装置的变形例 1 的结构的电路图。

[0017] 图 5 是用来说明在实施方式的半导体装置的变形例 1 中、对一个焊盘 2c1 设有多个 ESD 保护电路 12 的结构的电路图。

[0018] 图 6 是用来说明实施方式的半导体装置的变形例 2 的结构的、芯片 1A 上的焊盘 2c 的布局的图。

[0019] 图 7 是用来说明实施方式的半导体装置的变形例 3 的结构的、芯片 1B 上的焊盘 2c 的布局的图。

[0020] 图 8 是用来说明实施方式的半导体装置的变形例 4 的结构的、芯片 1C 的包含 ESD 保护电路 12 的 I / O 部的结构的电路图。

具体实施方式

[0021] 以下，参照附图说明实施方式。

[0022] (结构)

[0023] 图 1 是表示本实施方式的半导体装置的芯片布局概念的图。图 2 是用来说明本实施方式的半导体装置被搭载在半导体封装上的状态的图。

[0024] 本实施方式的半导体芯片(以下简称为芯片)1 中，如图 1 所示，在矩形的芯片的两个周边部，例如连接键合引线(bonding wire)的多个焊盘 2 沿芯片 1 的两边配置为直线状。

[0025] 另外，这里，在具有矩形形状的芯片 1 的两边的周边部，多个焊盘 2 被配置为直线状，但多个焊盘 2 也可以配置在四边的周边部，也可以不仅配置在周边部。

[0026] 芯片 1 的多个焊盘 2 的一部分焊盘 2a、2b 是电源用的焊盘，一部分的多个焊盘 2c 是应被相互电连接的输入输出信号用的焊盘。如后述那样，输入输出信号用的多个焊盘 2c 连接于 I / O 部 3，该 I / O 部 3 包含使用了二极管的多个 ESD 保护电路。在芯片 1 的中央部配置有逻辑电路 4，该逻辑电路 4 是实现各种功能的处理部。芯片 1 的处理部也可以是存储器部等。因而，处理部包含输入来自 I / O 部 3 的输出信号的逻辑电路以及存储器电路中的至少一个。

[0027] 另外，在以下的说明中，关于包含多个 ESD 保护电路的 I / O 部 3，对有关输入输出信号用焊盘的 I / O 部 3 进行说明，对于输入信号用焊盘也可以同样地设置包含多个 ESD 保护电路的 I / O 部 3。

[0028] 如图 2 所示，芯片 1 被封入搭载到用双点划线表示的半导体封装 100 中。芯片 1 的多个焊盘 2 通过作为连接布线单元的键合引线 101，连接到与管脚或焊球等多个外部连接端子连接的多个电极端子(以下称作外部电极) 102。半导体封装 100 的多个外部连接端子(未图示) 连接到搭载半导体封装 100 的印刷布线基板等的多个焊接区(land)。

[0029] 如图 2 所示，以使一组焊盘 2c 与一个外部电极 102 连接的方式，将输入信号用的

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多个焊盘 2c 连接到多个外部电极 102。多个焊盘 2c 通过各个外部电极 102 相互电连接。对芯片 1 输入多个输入信号，各输入信号在逻辑电路 4 中被进行规定的处理。被进行了该规定的处理的各种信号作为多个输出信号从芯片 1 输出。

[0030] 图 3 是用来说明芯片 1 的包含 ESD 保护电路 12 的 I / O 部的结构的电路图。多个焊盘 2 中的焊盘 2a 及 2b 是电源用的焊盘。焊盘 2a 是被施加电源电压 VDD 的电极，焊盘 2b 是连接地电位 VSS 的电极。电源箝位电路 11 设置在焊盘 2a 与 2b 之间。另外，图 3 中，作为电源用的焊盘 2，将焊盘 2a 和焊盘 2b 各示出了一个，但芯片 1 上也可以分别设置多个焊盘 2a 和 2b。

[0031] 并且，在图 3 中，焊盘 2c1 和 2c2 是多个焊盘 2 中的输入信号用的电极。焊盘 2c1 和 2c2 连接到与焊盘 2c1 和 2c2 连接的一个外部电极 102，是用来输入一个输入信号的一组焊盘。焊盘 2c1 和 2c2 通过两条键合引线 101，与半导体封装 100 内的一个外部电极 102 连接。

[0032] 图 3 中，仅示出了向一个外部电极 102 输入的一个输入信号用的焊盘 2c1 和 2c2，但是在芯片 1 上设有多组输入信号用的焊盘 2c，各组的焊盘 2c 通过两条键合引线 101，与对应的一个外部电极 102 连接。

[0033] 另外，这里，对于向外部电极 102 输入的一个输入信号，设有两个焊盘 2c1 和 2c2，但如图 3 中双点划线所示，对于一个输入信号，也可以设置三个焊盘 2c1、2c2、2c3，进而，虽未图示，对于一个输入信号，也可以设置大于等于四个的焊盘。即，对于输入各输入信号的外部电极，可以设置大于等于 3 个的焊盘 2c。

[0034] 并且，这里，对于全部输入信号中的各个输入信号，设有包含多个 ESD 保护电路 12 的 I / O 部 3，但也可以是，设置芯片 1 的多个输入信号中的至少一个输入信号用的、包含多个 ESD 保护电路 12 的 I / O 部 3。

[0035] 如以上那样，芯片 1 对多个输入信号分别设有一组焊盘 2c1 和 2c2。

[0036] 焊盘 2c1 和 2c2 分别连接到包含两个二极管 Dp、Dn 和电阻 R 的 ESD 保护电路 12。如图 3 所示，焊盘 2c1 和 2c2 分别连接到连接有电阻 R 的一端的两个二极管 Dp 和 Dn 的连接点 P1 和 P2。

[0037] 具体而言，焊盘 2c1 连接到 ESD 保护电路 12。ESD 保护电路 12 的二极管 Dp 的阴极与电源电压 VDD 连接，二极管 Dp 的阳极与二极管 Dn 的阴极连接。二极管 Dn 的阳极与作为基准电位的地电位 VSS 连接。焊盘 2c1 连接到二极管 Dp 和 Dn 的连接点 P1。

[0038] 焊盘 2c2 也与同样的 ESD 保护电路 12 连接，并连接到 ESD 保护电路 12 的两个二极管 Dp 和 Dn 的连接点 P2。

[0039] 即，多个(这里是两个)ESD 保护电路 12 与两个焊盘 2c1、2c2 连接，使得一个 ESD 保护电路 12 与一个焊盘 2c 对应。

[0040] 并且，连接点 P1 和 P2 分别连接电阻 R 的一端，两个电阻 R 的另一端彼此用连接点 Pc 连接，该连接点 Pc 的电位被输入 I / O 电路 13。

[0041] 即，I / O 电路 13 连接到连接点 Pc，该连接点 Pc 是两个 ESD 保护电路 12 的输出端彼此连接的连接部，向两个焊盘 2c1、2c2 输入的输入信号被输入 I / O 电路 13。

[0042] I / O 电路 13 是包含晶体管和电阻的缓冲电路、或者输入输出转换电路等。I / O 电路 13 的输出被输入逻辑电路 4。

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[0043] 如以上那样，如图 2 所示，芯片 1 的半导体封装 100 上设有通过键合引线 101 连接了多个焊盘例如焊盘 2c1、2c2 的多个外部电极 102。

[0044] 芯片 1 按每个输入信号设有两个焊盘 2c1 和 2c2。多个(这里是两个)焊盘 2c (这里是 2c1、2c2) 沿矩形的芯片 1 的至少一边(这里是二边) 配置为直线状。

[0045] 各焊盘 2c1 和 2c2 与 ESD 保护电路 12 连接。两个 ESD 保护电路 12 的输出端彼此连接，其连接点的电位被输入 I / O 电路 13。I / O 电路 13 的输出被输入逻辑电路 4。

[0046] 另外，在对一个输入信号设有大于等于三个的焊盘 2c 的情况下，各焊盘 2c 连接到两个二极管 Dp 和 Dn 的连接点，大于等于三个的 ESD 保护电路 12 的输出端彼此连接，其连接点 Pc 的电位被输入 I / O 电路 13。

[0047] (动作)

[0048] 接着，说明图 1 ～图 3 所示的芯片 1 的动作。

[0049] 向各外部电极 102 输入的一个输入信号，经作为两条信号线的键合引线 101，输入两个焊盘 2c1、2c2。

[0050] 输入信号的电流分支而流过两个焊盘 2c1、2c2，分支后的两个电流 I1、I2 分别经布线 L1、L2，输入 ESD 保护电路 12。由于两个 ESD 保护电路 12 的输出端在连接点 Pc 连接，所以从两个 ESD 保护电路 12 输出的电流在连接点 Pc 合流，并输入 I / O 电路 13。经过了 I / O 电路 13 的输入信号被输入逻辑电路 4，被进行规定的处理。

[0051] 例如，在对某外部电极 102 施加了高电压的静电的情况下，其电压还经两条键合引线 101 施加于焊盘 2c1、2c2。

[0052] 但是，由对外部电极 102 施加的电压产生的电流 I 向两个焊盘 2c1、2c2 分支，流过两个焊盘 2c1、2c2 的电流 I1、I2 分别经布线 L1、L2，流向对应的 ESD 保护电路 12。

[0053] 由于两条布线 L1、L2 相互并联地连接到 ESD 保护电路 12，所以流向布线 L1、L2 的电流 I1、I2 减小，因此能够实现布线 L1、L2 的电阻值的余量(margin)。进而，例如，若布线 L1 和 L2 是相同布线图案宽度且为相同长度，则由于流过各布线 L1、L2 的电流 I1、I2 成为整体电流 I 的一半，所以各电流 I1、I2 经 ESD 保护电路 12 的二极管 Dp 或 Dn 而电荷容易向 VDD 侧或 VSS 侧逃脱。其结果，I / O 电路 13 以及逻辑电路 4 变得难以被破坏。

[0054] 在不利用上述的本实施方式那样的结构的现有半导体装置中，采取提高电源箝位电路的功能以及增加布线图案宽度等对策。例如，在增加布线图案宽度的情况下，包括焊盘、ESD 保护电路 12 以及 I / O 电路 13 在内的电路部整体的面积增大。

[0055] 但是，在上述的本实施方式那样的结构的情况下，虽然对一个输入信号设置两个焊盘和两个 ESD 保护电路 12，但不需要增加布线图案宽度，且能够使两个焊盘的大小与以往的焊盘相比减小，所以能够抑制芯片面积的增加。

[0056] 此外，即使对一个输入信号设置多个焊盘和 ESD 保护电路 12，I / O 电路 13 也是一个即可。

[0057] 因而，对于一个输入信号，即使焊盘 2c 以及 ESD 保护电路 12 各自的数量为两个、三个、四个，关于焊盘、ESD 保护电路 12 以及 I / O 电路 13 的电路整体的面积，由于 I / O 电路 13 是一个即可，所以电路整体的面积不会成为 2 倍、3 倍、4 倍。例如，在焊盘、ESD 保护电路 12 以及 I / O 电路 13 的面积比例如为 4 :1 :5 的情况下，即使焊盘及 ESD 保护电路各自的数量增加为两个、三个、四个，在本实施方式中焊盘、ESD 保护电路 12 以及 I / O 电

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路 13 的电路整体的面积也不会成为 2 倍、3 倍、4 倍，而是成为 1．5 倍、2 倍、2．5 倍。

[0058] 因而，根据本实施方式，能够实现一种不增加布线图案宽度而能够提高芯片的管脚级的 ESD 耐性的半导体装置，结果，在半导体装置中，不会导致大的芯片面积的增加以及芯片的成本增加。

[0059] 接着说明几个变形例。

[0060] 图 4 是用来说明本实施方式的半导体装置的变形例 1 的结构的电路图。图 4 中，仅示出了被输入一个输入信号的两个焊盘 2c1、2c2。如图 4 所示，在焊盘 2c1、2c2 间设有开关 SW。开关 SW 的两端与焊盘 2c1 和 2c2 连接。开关 SW 的开闭通过开关控制信号 CS 控制。若开关 SW 通过开关控制信号 CS 而闭合，则两个焊盘 2c1、2c2 间导通。

[0061] 输出对开关 SW 的开闭进行控制的开关控制信号 CS 的开关控制电路 21，如图 1 及图 2 中双点划线所示那样，设置在芯片 1 上。开关控制电路 21 构成对控制开关 SW 的开闭的开关控制信号 CS 的输出进行控制的开关控制部。

[0062] 在芯片 1 被搭载于半导体封装 100 中之前的状态下，在同时向两个焊盘 2c1、2c2 施加了静电的状态下进行 ESD 评价时，使用开关 SW。

[0063] 即，不仅在芯片 1 的状态下对两个焊盘 2c1、2c2 分别施加 ESD 评价用的规定的电压，还能够通过将这样的开关 SW 设置在两个焊盘 2c1、2c2 间，从而以等同于向两个焊盘 2c1、2c2 所对应的外部电极 102 施加了规定的电压的状态，进行 ESD 评价。

[0064] 具体而言，不仅能够通过对两个焊盘 2c1、2c2 分别施加规定的电压，从而在芯片 1 的状态下按每个焊盘进行 ESD 评价，还能够通过将开关 SW 闭合，从而成为与如同使两个焊盘 2c1、2c2 与外部电极 102 连接、同时对两个焊盘 2c1、2c2 施加了规定的电压相同的状态。

[0065] 因而，在搭载于半导体封装 100 之前的芯片 1 的状态下，通过利用开关控制电路 21 进行控制使得开关 SW 闭合，从而能够在等同于宛如将两个焊盘 2c1、2c2 与外部电极 102 连接、并对外部电极 102 施加了规定的电压的状态下，进行 ESD 评价。

[0066] 另外，在相对于一个输入信号而焊盘 2c 为大于等于三个的情况下，多个开关 SW 设置在大于等于三个的焊盘 2c 的相邻的各一对焊盘 2c 间。并且，将多个开关 SW 设置为，使得当多个开关 SW 全部闭合时能够同时对多个焊盘 2c 施加规定的电压。

[0067] 另外，图 4 所示的变形例 1 中，通过经开关 SW 将两个焊盘 2c1、2c2 导通，来向两个 ESD 保护电路 12 输入共通信号，但焊盘的数量和 ESD 保护电路的数量不必相同。

[0068] 图 5 是用来说明在本实施方式的半导体装置的变形例 1 中、对一个焊盘 2c1 设有多个 ESD 保护电路 12 的结构的电路图。即，如图 5 所示，即使没有焊盘 2c2，也由于通过将开关 SW 闭合而向 ESD 保护电路 12 并行地输入一个输入信号，从而 ESD 耐性提高。

[0069] 图 5 那样的结构对于通过 I / O 部占用芯片的大量面积的情况是有效的。

[0070] 因而，对于一个输入，通过经由一个焊盘且多个 ESD 保护电路、或者多个焊盘且多个 ESD 保护电路，从而 ESD 耐性提高。

[0071] 图 6 是用来说明本实施方式的半导体装置的变形例 2 的结构的芯片 1A 上的焊盘 2c 的布局的图。

[0072] 上述的图 1 及图 2 的情况下，设于芯片 1A 的多个焊盘沿芯片 1A 的二边排列一列地配置，本变形例 2 中，两个焊盘 2c1、2c2 中的一方配置在与芯片 1A 的一边正交的方向上。

[0073] 即，多个(这里是两个)焊盘 2c（2c1、2c2)沿与矩形的芯片 1 的至少一边正交的方

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向配置。

[0074] 如图6所示，两个焊盘2c1、2c2中的一方的焊盘2c1设置在芯片1A的两边的附近，另一方的焊盘2c2配置在逻辑电路4的正上方。另一方的焊盘2c2设置为，层叠在芯片1A的形成了ESD保护电路12或I / O电路13的层之上。

[0075] 另外，若对于一个输入信号的焊盘2为三个，则如图6中虚线所示，第三个焊盘2c3在比焊盘2c2更靠近芯片1A的内侧设置在与焊盘1的一边正交的方向上。在对于一个输入输出信号的焊盘2为大于等于四个的情况下，也与第三个同样地，进一步在芯片1A的内侧，设置在与芯片1A的一边正交的方向上。

[0076] 根据这样的结构，由于两个焊盘2c不仅配置在芯片1A的一边，所以即使焊盘数量变为2倍(或大于等于3倍)，也不需要根据焊盘数量的增加而增大芯片1A的边方向的尺寸，从而芯片1A紧凑。

[0077] 图7是用来说明本实施方式的半导体装置的变形例3的结构的芯片1B上的焊盘2c的布局的图。

[0078] 本变形例3中，当对于一个输入信号的焊盘2c为四个时，如图7中虚线所示，对于一个输入信号的四个焊盘2c配置为，沿芯片1B的边缘设置两个，并且沿与芯片1B的边缘正交的方向设置两个。

[0079] 具体而言，如图7所示，在对于一个输入信号设有四个焊盘2c1、2c2、2c3、2c4的情况下，四个中的两个焊盘2c1、2c2沿芯片1B的各边配置，剩余的两个焊盘2c3、2c4沿与芯片1B的各边正交的方向配置。

[0080] 即，多个焊盘2c的一部分沿矩形的芯片1B的至少一边配置为直线状，多个焊盘2c的剩余的一部分沿与矩形的芯片1B的至少一边正交的方向配置。

[0081] 根据这样的结构，也产生可以不根据焊盘数量的增加而增大芯片1B的边方向的尺寸的效果。

[0082] 另外，这里，说明了对一个输入信号设置四个焊盘2c的情况，但也可以是，在设置更多的焊盘2c的情况下，使n个焊盘2c沿芯片1B的各边缘配置，并且，使各剩余的焊盘2c沿与芯片1B的各边缘正交的方向配置n个，来将多个焊盘2c配置为n×n的矩阵状。

[0083] 并且，在对一个输入信号设置多个焊盘的情况下，沿芯片1B的一边配置的焊盘2c的数量与沿与芯片1B的该边正交的方向配置的焊盘2c的数量也可以不同。

[0084] 图8是用来说明实施方式的半导体装置的变形例4的结构的芯片1C的包含ESD保护电路12的I / O部的结构的电路图。图8是将实施方式适用于WLCSP (Wafer Level Chip Size Package，晶片级芯片尺寸封装)的变形例。对于图8，对与图3相同的结构附加同一符号而省略说明。

[0085] 焊盘2c1、2c2、2c3是输入信号用的电极。焊盘2c1、2c2、2c3与外部电极110共通连接。焊盘2c1、2c2、2c3经外部电极110及布线L10而连接。

[0086] 外部电极110形成在焊盘2c1、2c2、2c3、ESD保护电路12、I / O电路13、逻辑电路4的上层。图8中为了简略，外部电极110仅图示了一个，但不限于一个，多个外部电极110在逻辑电路4等的上层形成为阵列状。此外，外部电极110形成球电极，进行来自芯片外部的信号的输入输出。

[0087] 通过将外部电极110形成在焊盘2c1、2c2、2c3及逻辑电路4等的上层，能够实现

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一种能够减小芯片面积并且能够不增加布线图案宽度而提高 ESD 耐压的半导体装置。

[0088] 如以上那样，根据上述的本实施方式以及各变形例，能够实现一种能够不增加布线图案宽度而提高芯片的管脚级的 ESD 耐性的半导体装置，结果，在半导体装置中，不会导致大的芯片面积的增加以及芯片的成本增加。

[0089] 说明了本发明的几个实施方式，但这些实施方式是作为例子而例示的，并不意欲限定发明的范围。这些新的实施方式能够以其他各种形态实施，在不脱离发明主旨的范围内，能够进行各种省略、替换、变更。这些实施方式及其变形包含在发明的范围及主旨中，并包含在权利要求的范围所记载的发明及其等同范围内。

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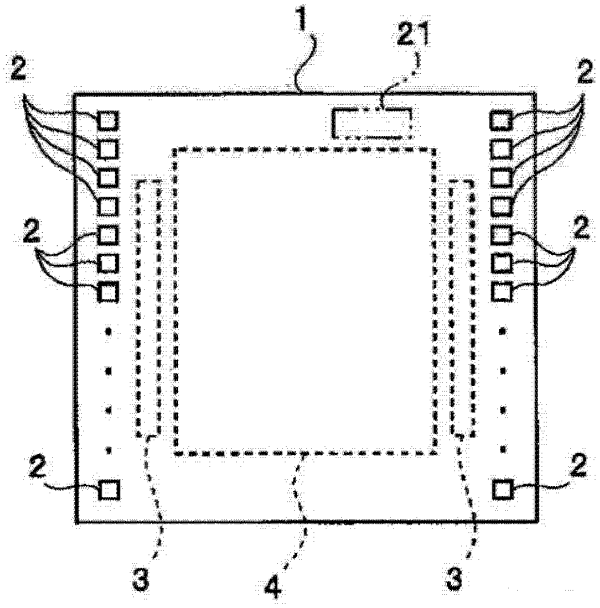


图 1

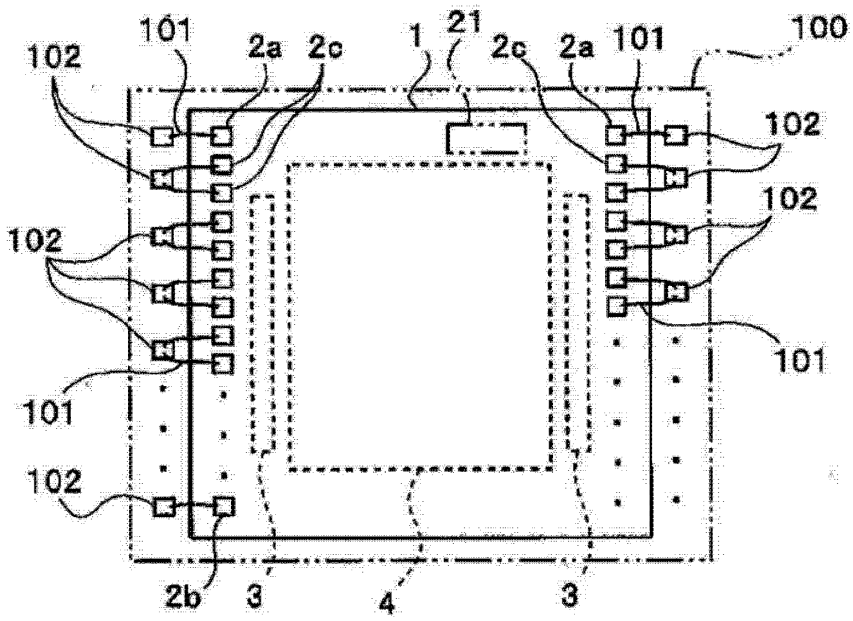


图 2

Micron Ex. 1002, p. 115
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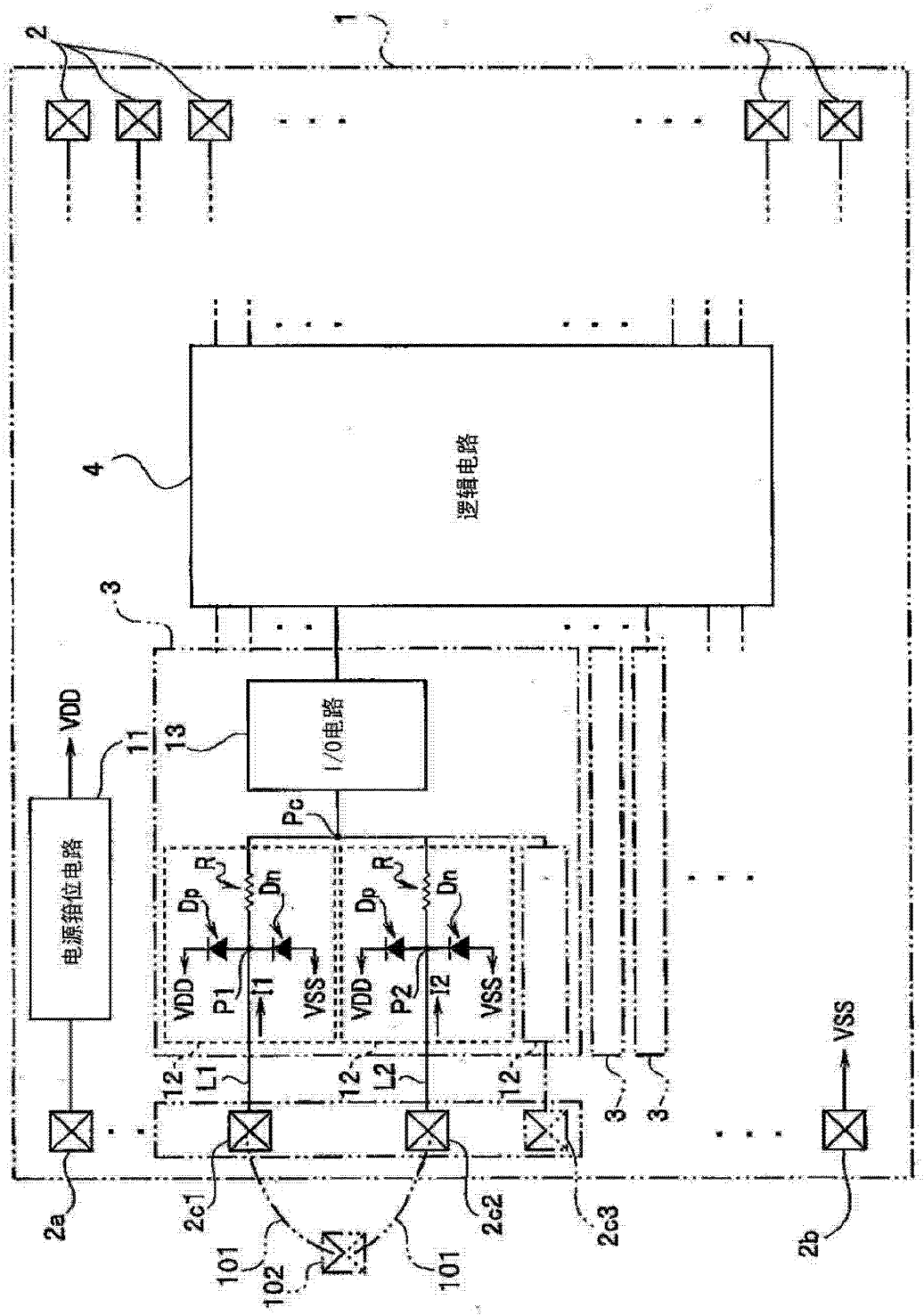


图 3

Micron Ex. 1002, p. 116
Micron v. YMTC
IPR2025-00118

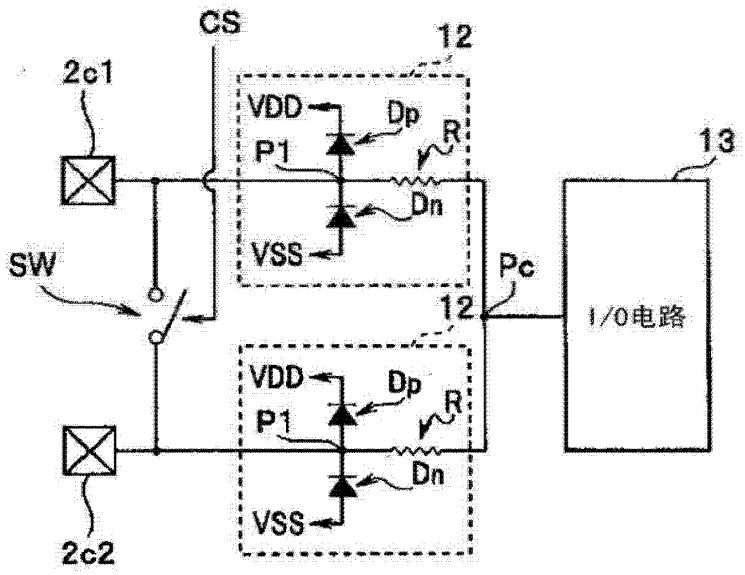


图 4

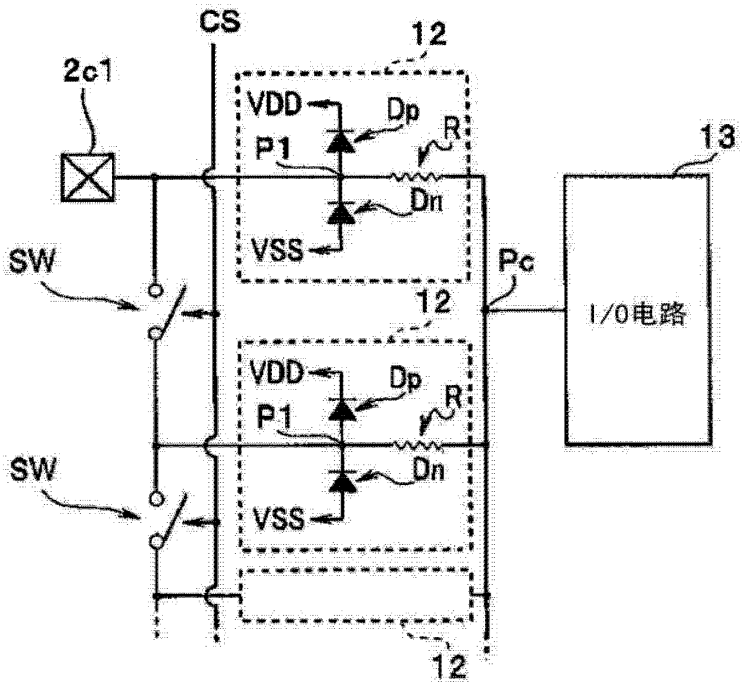


图 5

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Micron v. YMTC
IPR2025-00118

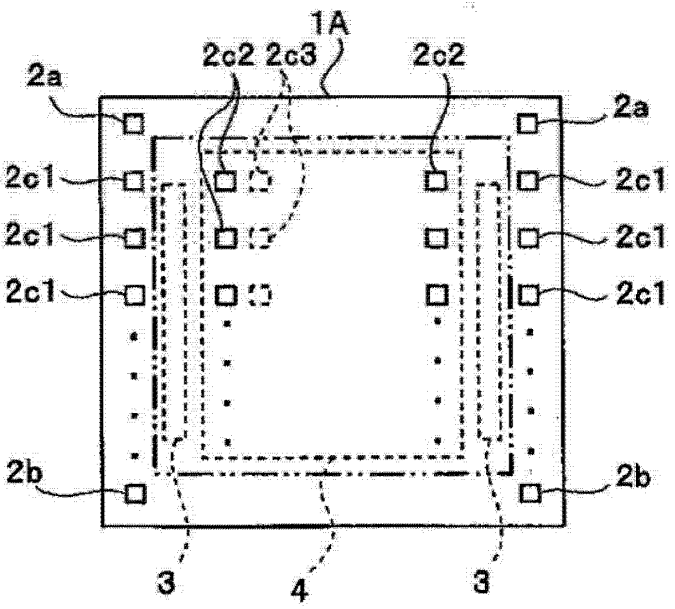


图 6

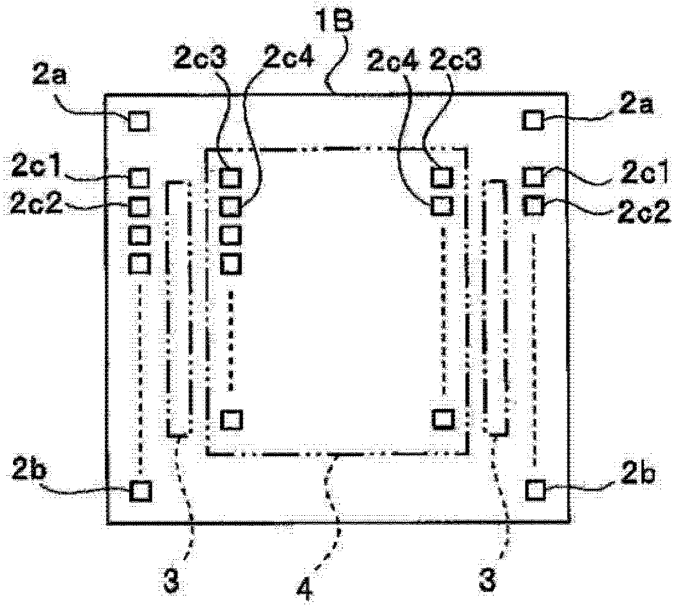


图 7

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Micron Ex. 1002, p. 119
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IPR2025-00118

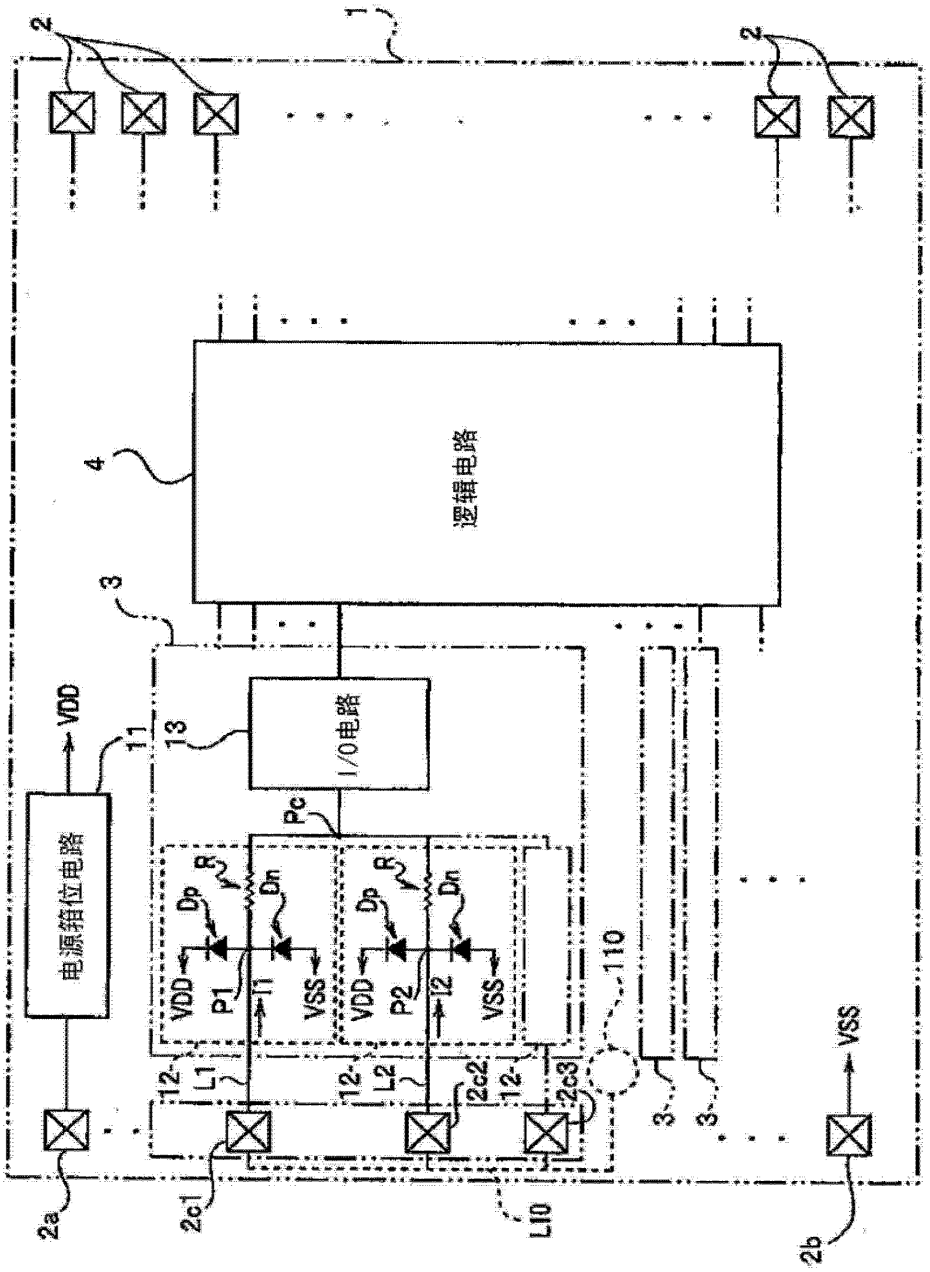


图 8

Electronic Acknowledgement Receipt

EFS ID:	36563728
Application Number:	16207183
International Application Number:	
Confirmation Number:	2734
Title of Invention:	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method
First Named Inventor/Applicant Name:	Zhiguo Li
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Anna Lu
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	YMTP0079USA3
Receipt Date:	16-JUL-2019
Filing Date:	02-DEC-2018
Time Stamp:	05:01:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	3527426.PDF	26097 8a2c9234ce29e1f9d5de6b344aec710d9203da19	no	3

Warnings:

Information:					
This is not an USPTO supplied IDS fillable form					
2	Foreign Reference	CN_101221629.PDF	688388 04f62688c0e45677964093aca7f37c080ab72601	no	16
Warnings:					
Information:					
3	Foreign Reference	CN_102054523.PDF	348764 8709b3fa43cb4f00378a76d3312b92a63e122e84	no	10
Warnings:					
Information:					
4	Foreign Reference	CN_103681654.PDF	1131810 7f4b93fa8264c0298c7b4bef92a2e731ed6bad79	no	16
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16207183
	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	YMTP0079USA3

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1	101097304	CN	B	2011-07-13			Abstract
	2	103000625	CN	A	2013-03-27			Abstract
	3	20020034470	KR	A	2002-05-09			Abstract

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16207183
	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	YMTP0079USA3

NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1		

EXAMINER SIGNATURE			
Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16207183
	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	YMTP0079USA3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Roger Chen/	Date (YYYY-MM-DD)	2019-08-13
Name/Print	Roger Chen	Registration Number	67314

Abstract of CN101097304

An active element array mother base board fits for cutting several active element array base boards, the active element mother base board includes a base board, a plurality of active element arrays and a plurality of outer circuit pads. Thereinto, the base board is provided with a plurality of preset areas, each preset area respectively defines a position for an active element array base board. Besides, the active element arrays and outer circuit pads are distributed in the preset areas, and within the preset area, the outer circuit pad and signal wire of the active element array are electrically connected. Especially, at least outer circuit pad in one preset area is electrically connected with outer circuit pad in the other preset area.

(19)中华人民共和国国家知识产权局

(12)发明专利

(10)授权公告号 CN 101097304 B
(45)授权公告日 2011.07.13

(21)申请号 200610099789.6
(22)申请日 2006.06.27
(73)专利权人 中华映管股份有限公司
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代理人 陈亮
(51)Int.Cl.
G02F 1/133(2006.01)
G02F 1/136(2006.01)
(56)对比文件
CN 1077295 C,2002.01.02, 全文.
CN 1527104 A,2004.09.08, 说明书第3页第5行 第5页第8行,第8页第5 26行、附图1,3,7.
US 6043971 A,2000.03.28, 全文.
审查员 佟晓惠

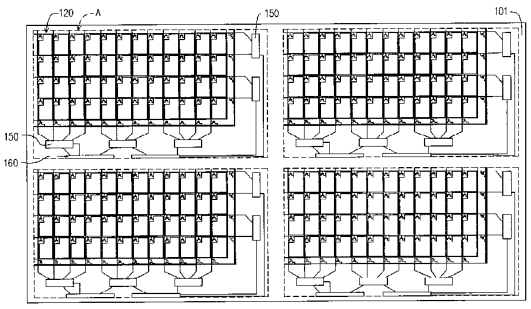
权利要求书 1 页 说明书 6 页 附图 6 页

(54)发明名称

主动元件阵列母基板

(57)摘要

一种主动元件阵列母基板,其适于分割出多片主动元件阵列基板,主动元件阵列母基板包括一基板、多组主动元件阵列与多个外部电路焊盘(pad)。其中,基板具有多个预定区,此预定区分别定义出主动元件阵列基板的所在位置。此外,上述主动元件阵列与外部电路焊盘均分别配置于预定区内,且在各预定区内,外部电路焊盘与主动元件阵列的信号线电性连接。特别地是,至少一个预定区内的所述外部电路焊盘与另外一个预定区内的外部电路焊盘彼此电性相连。



CN 101097304 B

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1. 一种主动元件阵列母基板，适于分割出多片主动元件阵列基板，其特征在于，所述主动元件阵列母基板包括：

一基板，具有多个预定区，其中所述预定区分别定义出所述主动元件阵列基板的所在位置；

多组主动元件阵列，分别配置于所述预定区内，其中各组主动元件阵列具有多条信号线；

多个外部电路焊盘，配置于所述预定区内，且在各所述预定区内，所述信号线是电性连接至所述外部电路焊盘；以及

一引线，配置于所述基板上的所述预定区外，其中各所述预定区内的所述外部电路焊盘均电性连接至所述引线，而使所述主动元件阵列通过所述引线而彼此电性相连，

其中，所述基板之各所述预定区内还包括：

多个驱动芯片焊盘，分别与所述主动元件阵列的所述信号线电性连接；以及

一内部静电放电保护环，电性连接于所述驱动芯片焊盘与所述信号线之间，且所述内部静电放电保护环电性连接至所述外部电路焊盘其中之一。

2. 如权利要求 1 所述的主动元件阵列母基板，其特征在于，所述内部静电放电保护环包括：

多个保护元件，分别电性连接于所述信号线与所述驱动芯片焊盘之间；以及

一连接导线，串接所述保护元件，并电性连接至所述外部电路焊盘其中之一。

3. 如权利要求 1 所述的主动元件阵列母基板，其特征在于，还包括多个开关元件，电性连接于所述外部电路焊盘与所述引线之间。

4. 如权利要求 3 所述的主动元件阵列母基板，其特征在于，所述开关元件包括薄膜晶体管或二极管至少其中之一。

5. 如权利要求 1 所述的主动元件阵列母基板，其特征在于，所述外部电路焊盘包括多个第一焊盘与多个第二焊盘，且在各所述预定区内的所述信号线包括：

多条数据线，分别电性连接至所述预定区内的所述第一焊盘，且所述第一焊盘与所述数据线为同一膜层；以及

多条扫描线，分别电性连接至所述预定区内的所述第二焊盘，且所述第二焊盘与所述扫描线为同一膜层。

6. 如权利要求 5 所述的主动元件阵列母基板，其特征在于，所述引线包括一第一导电层与一第二导电层，所述第二导电层位于所述第一导电层上方，且所述第一焊盘电性连接至所述第一导电层，而所述第二焊盘电性连接至所述第二导电层。

7. 如权利要求 5 所述的主动元件阵列母基板，其特征在于，所述引线为一透明导电层，且所述第一焊盘与所述第二焊盘均电性连接至所述透明导电层。

8. 如权利要求 7 所述的主动元件阵列母基板，其特征在于，所述透明导电层的材料包括铟锡氧化物或铟锌氧化物。

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主动元件阵列母基板

技术领域

[0001] 本发明有关于一种主动元件阵列母基板，且特别有关于一种具有静电放电(electro static discharge，ESD)防护功效的主动元件阵列母基板。

背景技术

[0002] 在液晶显示器的制造过程中，操作人员、机台或检测仪器都可能带有静电，而上述的带电体（操作人员、机台或检测仪器）接触到液晶显示面板时，可能导致液晶显示面板内的元件以及电路遭受静电放电(electro static discharge)破坏。因此，一般都会在液晶显示面板的非显示区中设计静电放电保护电路。以主动矩阵液晶显示面板来说，其通常是在制造主动元件阵列的过程中一并将静电放电保护电路形成于基板上，并且令主动元件阵列与这些静电放电保护电路电性连接。如此一来，当液晶显示面板遭受到静电放电的冲击时，会触发静电放电保护电路的保护机制，因而通过静电放电保护电路将静电分散、减弱，以避免静电直接导入显示区内部的元件及电路而造成损毁。

[0003] 图1为现有的主动元件阵列基板示意图。图1中所示的主动元件阵列基板100包括形成于基板110上的主动元件阵列120、多个驱动芯片焊盘(pad)150以及静电放电保护电路160。其中，基板110具有一显示区112与一周边电路区114，主动元件阵列120配置于显示区112内，并包括多个主动元件122、多个象素电极124、多条扫描线130与多条数据线140。详细地说，扫描线130与数据线140适于驱动其所对应的主动元件122，以通过主动元件122来驱动象素电极124。而且，主动元件阵列120通过扫描配线130与数据配线140而电性连接至驱动芯片焊盘150，并通过驱动芯片焊盘150而与外部的驱动电路（未示出）电性连接。

[0004] 在目前的平面显示器中，常见的静电放电保护电路160包括内部静电放电保护环162与外部静电放电保护环164。其中，内部静电放电保护环162电性连接于驱动芯片焊盘150与主动元件阵列120之间。当静电放电现象发生于主动元件阵列120中时，静电会开启内部静电放电保护环162，并通过内部静电放电保护环162而将静电分散。此外，为避免在驱动芯片焊盘150与外部驱动电路（未示出）之间发生静电破坏，外部静电放电保护环164是配置于基板110外围，并电性连接于驱动芯片焊盘150。同理，当静电放电现象发生于任一驱动芯片焊盘150时，静电会开启外部静电放电保护环164，并藉此而将静电分散。

[0005] 图2为现有的一种主动元件阵列母基板的示意图。请参照图2，一般来说，上述主动元件阵列基板100的制造方式是先在大片的玻璃基板101上定义出多个预定区A，之后在这些预定区A内形成上述的主动元件阵列120以及相关电路，最后再对大片的玻璃基板101进行切割，以切出多片主动元件阵列基板。在经济效益的考虑下，各个预定区A之间的距离会尽可能的缩小，以增加玻璃基板101的利用率。因此，近年来便发展出一种COG(Chip On Glass)技术，其是直接将驱动电路芯片（未示出）贴附在玻璃基板101上的驱动芯片焊盘150，并通过驱动芯片焊盘150而与可挠性电路板（未示出）电性连接，以节省空间。

[0006] 然而，若在COG的技术中置入外部静电放电保护环164，则会对玻璃基板101上的

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走线造成线路干涉的问题。而且，当各个预定区 A 之间的距离变小后，玻璃基板 101 上无足够的面积配置外部静电放电保护环 164。也就是说，传统的 COG 技术中，在玻璃基板 101 上的主动元件阵列 120 仅能靠内部静电放电保护环来分散静电。如此一来，将使各主动元件阵列 120 的抗静电放电破坏的能力大幅降低，进而导致主动元件阵列 120 中的元件与电路面临极高的静电放电破坏的风险。

发明内容

[0007] 有鉴于此，本发明的目的在于提供一种主动元件阵列母基板，以避免主动元件阵列母基板上各主动元件阵列遭受到静电放电的破坏。

[0008] 为达上述或其他目的，本发明提出一种主动元件阵列母基板，其适于分割出多片主动元件阵列基板，主动元件阵列母基板包括一基板、多组主动元件阵列与多个外部电路焊盘以及一引线。其中，基板具有多个预定区，此预定区分别定义出主动元件阵列基板所在位置。此预定区内还包括多个驱动芯片焊盘和一内部静电放电保护环。其中多个驱动芯片焊盘分别与主动元件阵列的信号线电性连接。内部静电放电保护环电性连接于驱动芯片焊盘与信号线之间，且内部静电放电保护环电性连接至外部电路焊盘其中之一。此外，上述多组主动元件阵列分别配置于预定区内，且各组主动元件阵列均具有多条信号线。外部电路焊盘也配置于预定区内，且在各预定区内，上述信号线分别与外部电路焊盘电性连接。引线配置于基板的预定区外，其中各预定区内的外部电路焊盘均电性连接至引线，而使主动元件阵列通过引线而彼此电性相连。

[0009] 在本发明的一实施例中，上述内部静电放电保护环包括多个保护元件与一连接导线。其中，这些保护元件分别电性连接于信号线与驱动芯片焊盘之间，且这些保护元件是通过此连接导线而彼此电性连接。此外，此连接导线还电性连接至此预定区内的一外部电路焊盘。

[0010] 在本发明的一实施例中，上述主动元件阵列母基板还包括多个开关元件，分别电性连接于这些外部电路焊盘与上述引线之间。其中，这些开关元件可以是薄膜晶体管、二极管或其组合。

[0011] 在本发明的一实施例中，上述外部电路焊盘包括多个第一焊盘与多个第二焊盘，且在各预定区内的信号线包括多条数据线与多条扫描线。其中，扫描线分别电性连接至其所在的预定区内的这些第一焊盘，且这些第一焊盘与这些扫描线为同一膜层。这些数据线则是分别电性连接至第二焊盘，且这些第二焊盘与这些数据线为同一膜层。

[0012] 在本发明的一实施例中，上述引线可以由第一导电层与第二导电层所构成，且第二导电层位于第一导电层上方。此外，上述第一焊盘可以电性连接至第一导电层，第二焊盘则可以电性连接至第二导电层。

[0013] 在本发明的一实施例中，上述引线可以是一透明导电层，且上述第一焊盘与第二焊盘均电性连接至此透明导电层。

[0014] 在本发明的一实施例中，上述透明导电层的材料包括铟锡氧化物或铟锌氧化物。

[0015] 本发明还提出了一种主动元件阵列母基板，适于分割出多片主动元件阵列基板，主动元件阵列母基板包括：一基板，具有多个预定区，其中预定区分别定义出主动元件阵列基板的所在位置，各预定区内还包括一总线；多组主动元件阵列，分别配置于预定区内，其

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中各组主动元件阵列具有多条信号线，且在各预定区内，主动元件阵列的信号线包括多条共用配线；以及多个外部电路焊盘，配置于预定区内，且在各预定区内，信号线是电性连接至外部电路焊盘，共用配线通过总线而与外部电路焊盘电性连接，而位于不同预定区内的总线通过外部电路焊盘至少其中之一而彼此电性连接。

[0016] 本发明的主动元件阵列母基板是令至少两预定区内的焊盘彼此电性连接，而使得不同预定区内的线路彼此电性连接。因此，当静电放电现象发生于某一主动元件阵列中时，静电会被进一步分散至整个母基板上，以减弱静电对单一主动元件阵列所造成的冲击。

[0017] 为让本发明的上述和其他目的、特征和优点能更明显易懂，下文特举较佳实施例，并配合附图，作详细说明如下。

附图说明

[0018] 图 1 是现有的主动元件阵列基板示意图。

[0019] 图 2 是现有的一种主动元件阵列母基板示意图。

[0020] 图 3 是本发明第一实施例中主动元件阵列母基板示意图。

[0021] 图 4 是本发明第二实施例中主动元件阵列母基板示意图。

[0022] 图 5A 是本发明一实施例中图 3 的主动元件阵列母基板沿 1-1’线的剖面示意图。

[0023] 图 5B 是本发明另一实施例中图 3 的主动元件阵列母基板沿 I-I’线的剖面示意图。

[0024] 图 6 是本发明第三实施例中主动元件阵列母基板示意图。

具体实施方式

[0025] 图 3 是本发明第一实施例中主动元件阵列母基板示意图。请参考图 3，主动元件阵列母基板 300 适于被分割为多片主动元件阵列基板。具体来说，此主动元件阵列母基板 300 包括一基板 310、多组主动元件阵列 320 与多个外部电路焊盘 350。其中，基板 310 可以具有预定区 A、B、C 与 D，而各组主动元件阵列 320 即是分别配置于预定区 A、B、C 与 D 内。也就是说，本实施例的主动元件阵列母基板 300 在后续制程中可以被切割成四片主动元件阵列基板。当然，本发明并无意局限基板 310 上的预定区数目，这可以视欲制作出的主动元件阵列基板的尺寸与片数而作适当调整。

[0026] 请继续参照图 3，各组主动元件阵列 320 均具有多条信号线 322，且熟习此技艺者应该知道，这些信号线 322 包括扫描线 321 与数据线 323。此外，预定区 A、B、C 与 D 内均配置有多个外部电路焊盘 350，且在各预定区 A、B、C 与 D 内，外部电路焊盘 350 与其所对应的主动元件阵列 320 互相电性连接。由图 3 可清楚得知，主动元件阵列 320 是通过扫描线 321 或数据配线 323 而电性连接至外部电路焊盘 350。在此，外部电路焊盘 350 可以用来与可挠性电路板（flexible printed circuit，FPC）（未示出）电性连接。

[0027] 特别的是，主动元件阵列母基板 300 上至少两预定区内的外部电路焊盘 350 彼此电性连接。如此一来，当任一预定区内的主动元件阵列 320 中发生静电放电的现象时，此静电会被导散至整个基板 310 上，进而避免基板 310 上的任何电子元件遭受到静电放电的破坏。

[0028] 详细来说，主动元件阵列母基板 300 在各预定区 A、B、C 与 D 中还包括多个内部静电放电保护环 360 与多个驱动芯片焊盘 370。其中，驱动芯片焊盘 370 是电性连接于信号

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线 322 与外部电路焊盘 350 之间。换言之，主动元件阵列 320 的信号线 322 是先电性连接至驱动芯片焊盘 370，再经由驱动芯片焊盘 370 而与外部电路焊盘 350 电性连接。其中，后续欲贴附于基板 310 上的驱动芯片（未示出）即是贴在这些驱动芯片焊盘 370 上。

[0029] 另外，在各预定区内，内部静电放电保护环 360 是电性连接于信号线 322 与驱动芯片焊盘 370 之间。而且，内部静电放电保护环 360 可以由多个保护元件 362 与连接导线 364 所构成，其中保护元件 362 可以是薄膜晶体管、二极管或是这些元件的组合。连接导线 364 则是将这些保护元件 362 串接起来，而且连接导线 364 更进一步与至少一外部电路焊盘 350 电性连接。如此一来，当主动元件阵列 320 中发生静电放电现象时，静电荷可以经由信号线 322 往内部静电放电保护环 360 移动，并开启保护元件 362，进而通过连接导线 364 而分散至外部电路焊盘 350。此时，由于本发明的主动元件阵列母基板 300 上不同预定区内的外部电路焊盘 350 彼此电性连接，因此静电荷会再从外部电路焊盘 350 散逸至其他预定区内，以避免静电荷过于集中而损坏主动元件阵列 320。

[0030] 在本实施例中，主动元件阵列母基板 300 可以利用一引线 380 来电性连接不同预定区内的外部电路焊盘 350，进而使位于不同预定区 A、B、C 与 D 内的主动元件阵列 320 通过引线 380 而彼此电性相连。其中，引线 380 配置于基板 210 上，且位于预定区 A、B、C 与 D 之外。值得一提的是，引线 380 可以与外部电路焊盘 350、扫描线 321 或数据线 323 一并形成。当然，引线 380 也可以是在主动元件阵列母基板 200 的其他制程中所遗留下来的金属线。换言之，本发明可以在不额外增加制程的情况下形成引线 380。

[0031] 此外，本发明当然也可以在各外部电路焊盘 350 与引线 380 之间配置有开关元件 390，如图 4 所示，其中开关元件 390 可以是薄膜晶体管、二极管或这些元件的组合。

[0032] 请再次参照图 3，当主动元件阵列母基板 300 上发生静电放电现象时，静电所带的高电压会启动内部静电放电保护环 360 的保护机制，因此静电荷会通过连接导线 364 分散并传递至外部电路焊盘 350，并通过引线 380 而分散至基板 310 上的其他预定区内。换言之，静电在开启保护元件 362 之后，会消耗静电的部分能量，且静电会再通过引线 380 而散逸至整个基板 310，因而减低静电放电破坏的能力。

[0033] 一般而言，在较大尺寸的主动元件阵列母基板 300 中，上述效果会更加显著，这是因为较大尺寸的主动元件阵列母基板 300 会具有较长且范围较大的静电散逸路径，静电的能量会在传导的过程中被消耗，且静电会被分散至较大的范围中，而造成静电放电破坏的能力大幅衰减。因此，本发明可使不适合制作现有外部静电放电保护环 164（如图 1 所示）的主动元件阵列母基板 300，仍然具有良好的静电放电防护功效。而且在实务上，由于本实施例的主动元件阵列母基板 300 上并没有图 1 的外部静电放电保护环 164，所以无须进行额外的切割制程来分离外部静电放电保护环，因此不必担心磨边导角的限制。

[0034] 另一方面，由于本实施例的主动元件阵列母基板 300 并非以外部静电放电保护环来提供静电散逸路径，因此可以避免外部静电放电保护环与基板 310 上的线路相互干涉的问题。

[0035] 在本实施例中，外部电路焊盘 350 包括多个第一焊盘 352 与多个第二焊盘 354，其中第一焊盘 352 可以用以承载欲与扫描线 321 电性连接的可挠性电路板（未示出），第二焊盘 354 可以用以承载欲与数据线 323 电性连接的可挠性电路板（未示出）。换言之，扫描线 321 是电性连接至第一焊盘 352，数据线 323 则是电性连接至第二焊盘 354。而且，扫描

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线 321 可以与第一焊盘 352 同层，数据线 323 则可以与第二焊盘 354 同层。

[0036] 承上所述，熟习此技艺者应该知道，扫描线 321 与数据线 323 分属不同膜层，也就是说，第一焊盘 352 与第二焊盘 354 也分属不同膜层。以下将举例说明在此种情况下，如何令第一焊盘 352 与第二焊盘 354 均与引线 380 电性连接。

[0037] 图 5A 为本发明一实施例中图 3 的主动元件阵列母基板沿 I-I' 线的剖面示意图。请参照图 5A，在此实施例中，引线 380 是由第一导电层 382 与第二导电层 384 所构成，其中第二导电层 384 位于第一导电层 382 上方，且第一焊盘 352 是通过导线 352a 电性连接至第一导电层 382，第二焊盘 354 则是通过导线 354a 电性连接至第二导电层 384。

[0038] 图 5B 为本发明另一实施例中图 3 的主动元件阵列母基板沿 I-I' 线的剖面示意图。请参照图 5B，在此实施例中，引线 380 为单一膜层，且其足同时与分属不同层的第一焊盘 352 与第二焊盘 354 电性连接。详细来说，引线 380 可以位于第一焊盘 352 与第二焊盘 354 上方的膜层，且其可以直接覆盖于由第二焊盘 354 所延伸出的导线 354a 上，并通过位于第一焊盘 352 与第二焊盘 354 间的介电层 327 中的接触窗开口 329 而与第一焊盘 352 所延伸出的导线 352a 电性连接。举例来说，引线 380 可以是一透明导电层，且其可以是与主动元件阵列 320 中的象素电极 324（如图 3 所示）在同一道光罩制程下一并形成。换言之，引线 380 的材质可以为铟锡氧化物 (ITO) 或铟锌氧化物 (IZO)。

[0039] 请同时参照图 3 及图 5B，若静电放电现象发生于主动元件阵列 320 的扫描线 321 上，静电荷可经由第一焊盘 352 传递至引线 380，并通过引线 380 而分散至第二焊盘 354，进而使数据线 323 与扫描线 321 具有相同电位。同样地，若静电放电现象发生于主动元件阵列 320 的数据线 323 上，静电荷可经由第二焊盘 354 传递至引线 380，并通过引线 380 而分散至第一焊盘 352，进而使扫描线 321 与数据线 323 具有相同电位。如此一来，可以有效降低静电放电对主动元件阵列母基板 300 所造成的冲击，进而达到保护主动元件阵列母基板 300 的目的。

[0040] 值得注意的是，当基板 310 上的各组主动元件阵列 320 的排列过于紧密，而未有足够的空间配置图 3 的引线 380 时，本发明仍可以其他方法来使不同预定区内的外部电路焊盘 350 彼此电性连接，以下将举例说明之。

[0041] 图 6 是本发明第二实施例的主动元件阵列母基板示意图。为了凸显本实施例的特征，在图 6 中省略了部分元件的绘制，并将重点放在不同预定区内线路彼此之间的连接方式。请参考图 6，主动元件阵列母基板 600 在各预定区内还包括一总线 610，且各组主动元件阵列 320 的信号线除了包括图 3 的扫描线 321 与数据线 323 之外，也包括多条共用配线 620，而各预定区内的总线 610 即是与这些共用配线 620 电性连接，用以将外部所提供的信号传输至这些共用配线 620。由图 6 可清楚得知，总线 610 是环绕在主动元件阵列 320 的周围，并且与外部电路焊盘 350 电性连接。更特别的是，本实施例的外部电路焊盘 350 是电性连接于两预定区的总线 620 之间，因此当静电放电现象发生于主动元件阵列母基板 600 的某预定区内的主动元件阵列 320 时，静电会从共用配线 620 经总线 610 而传导至外部电路焊盘 350，并进一步通过外部电路焊盘 350 而散逸至其他预定区。这样一来，便可以有效降低并分散静电放电对主动元件阵列母基板 600 所造成的冲击，进而达到保护主动元件阵列母基板 600 的目的。

[0042] 需要一提的是，虽然图 6 仅将位于预定区 A 与预定区 C 中的总线 610 通过外部电

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路焊盘 350 而彼此电性连接，但熟习此技艺者应该知道，当然实际上还可以将其他预定区 B 或 D 的总线 610 一并连接在一起，在此并不作特别限定。

[0043] 综上所述，本发明的主动元件阵列母基板至少具有下列优点：

[0044] 一、本发明将主动元件阵列母基板上位于不同预定区内的主动元件阵列电性连接，以大幅增加静电的散逸路径以及范围。这样一来，当静电放电现象发生时，静电会被充分地分散，进而使静电的破坏能力大幅降低，进而达到保护各主动元件阵列的效果。而且，外部电路焊盘在与可挠性电路板接合的制程中也可免于遭受静电放电破坏。

[0045] 二、本发明的主动元件阵列母基板可以在不制作外部静电放电保护环的情况下，仍然具有良好的静电放电防护的功效。因此，本发明适用于以 COG 技术来制作主动元件阵列基板的制程中。

[0046] 三、本发明的主动元件阵列母基板上的引线可以在原有的制程中形成，且主动元件阵列母基板上毋须制作外部静电放电保护环即可具有静电放电防护功效。因此，本发明的主动元件阵列母基板具有较低的制造成本。

[0047] 虽然本发明已以较佳实施例揭示如上，然其并非用以限定本发明，任何熟习此技艺者，在不脱离本发明的精神和范围内，当可作些许更动与润饰，因此本发明的保护范围当视权利要求所界定者为准。

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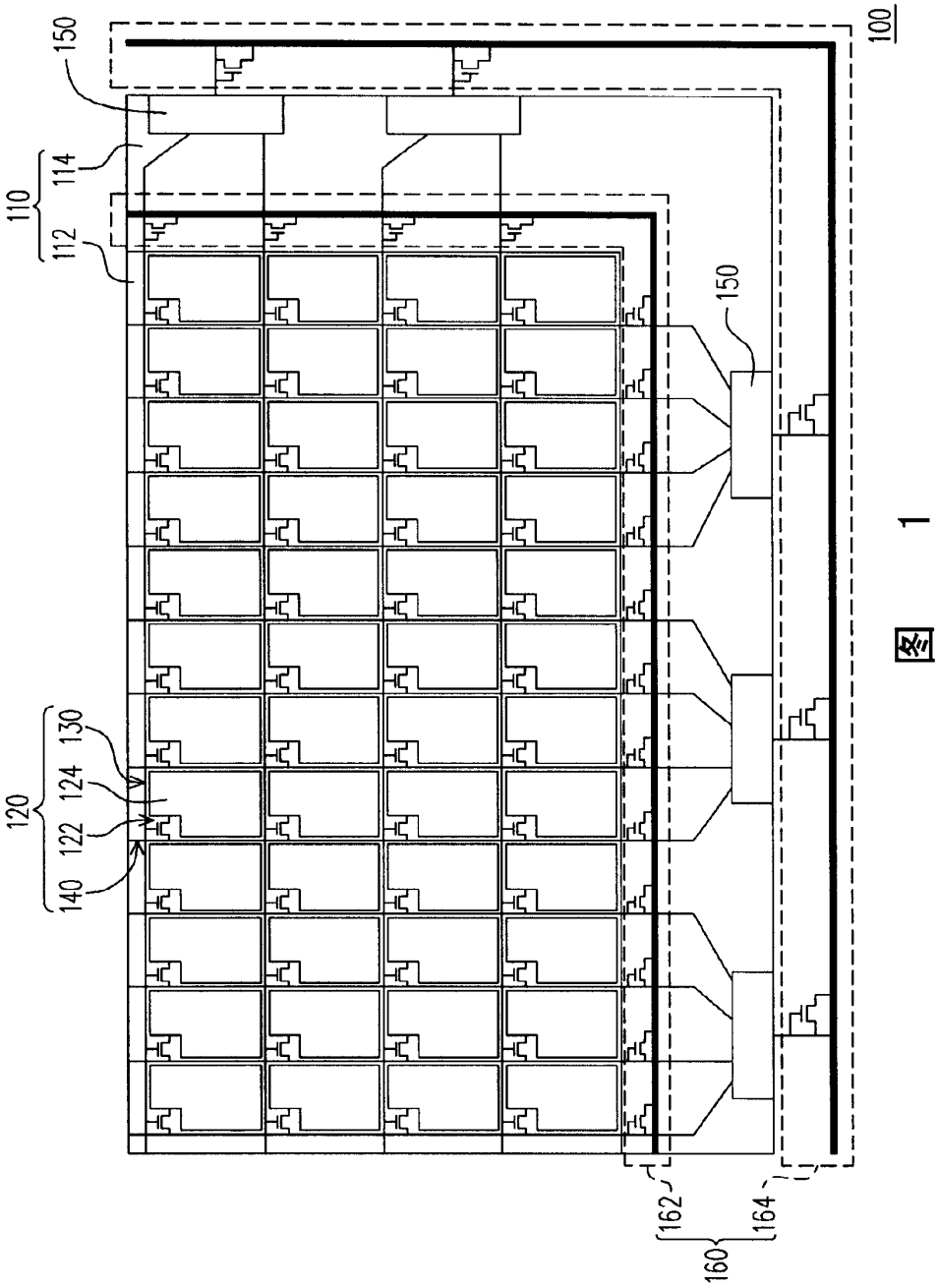


图 1

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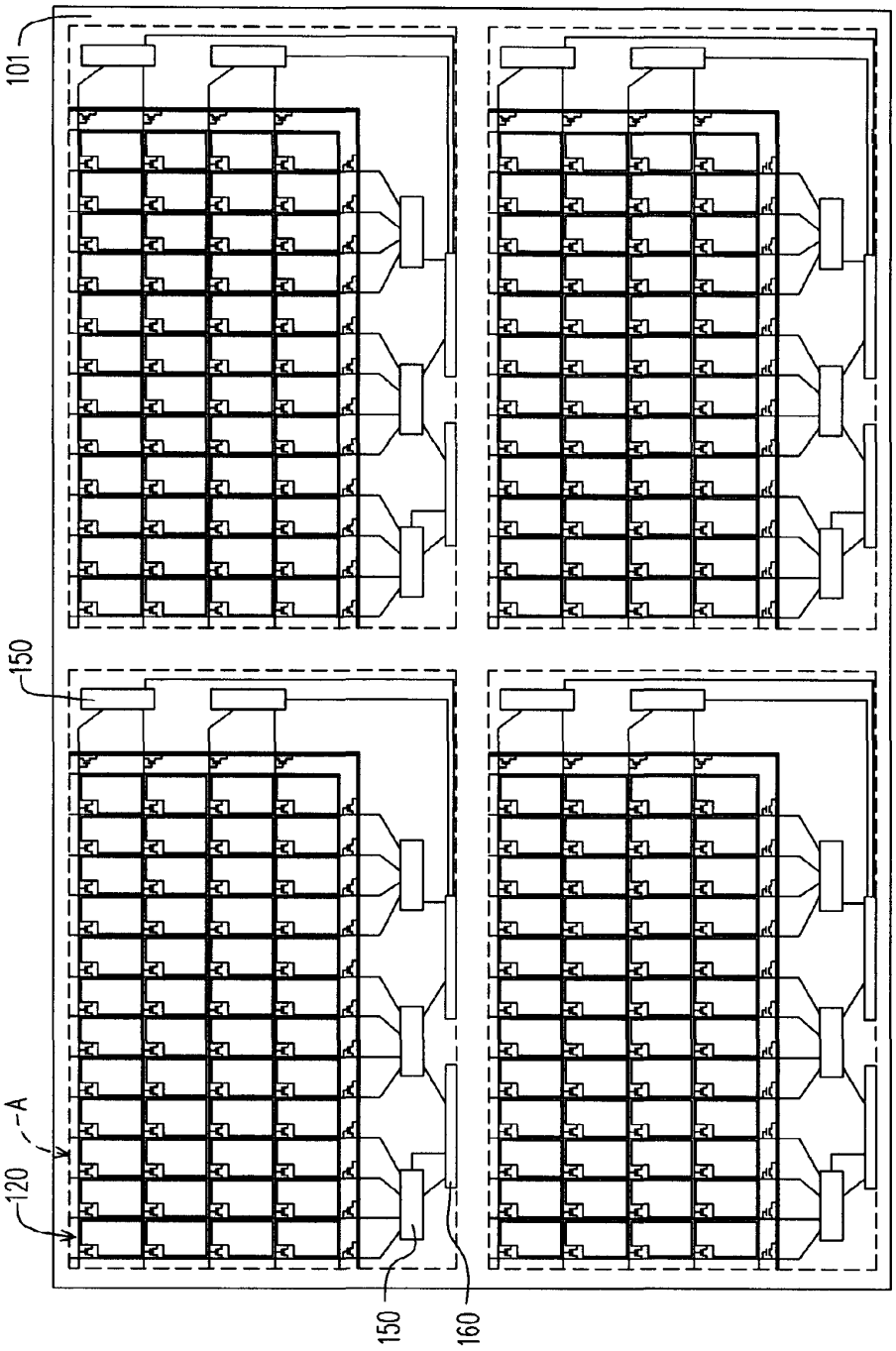


图 2

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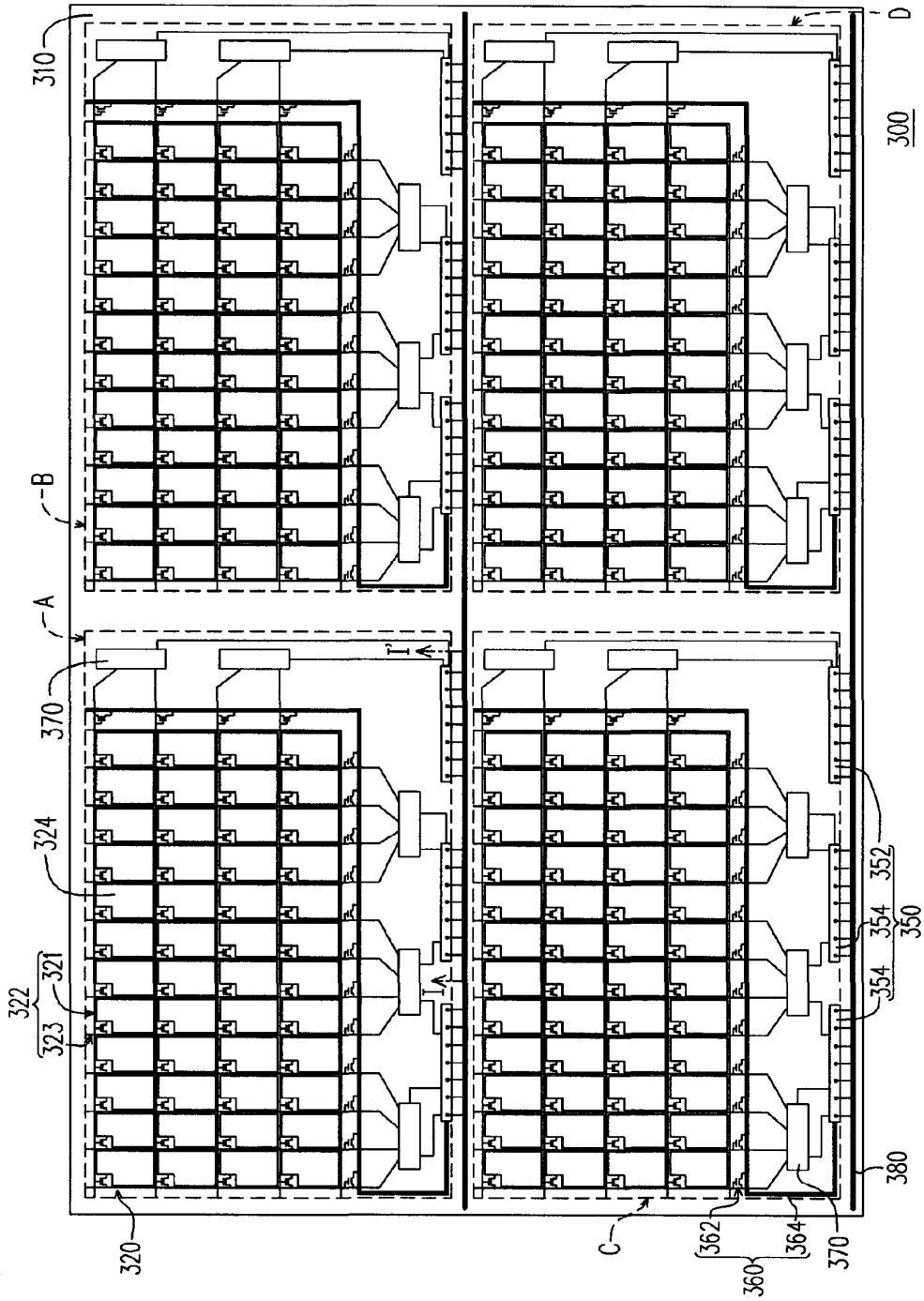


图 3

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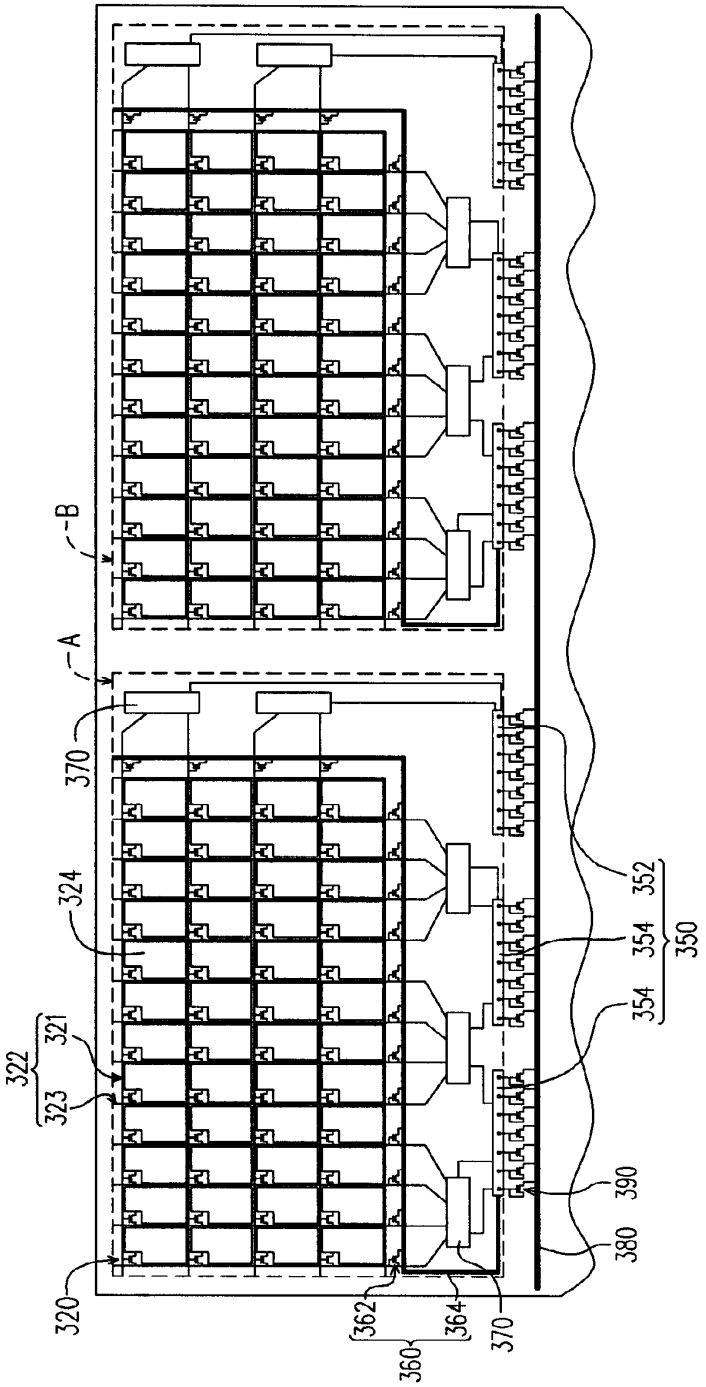


图 4

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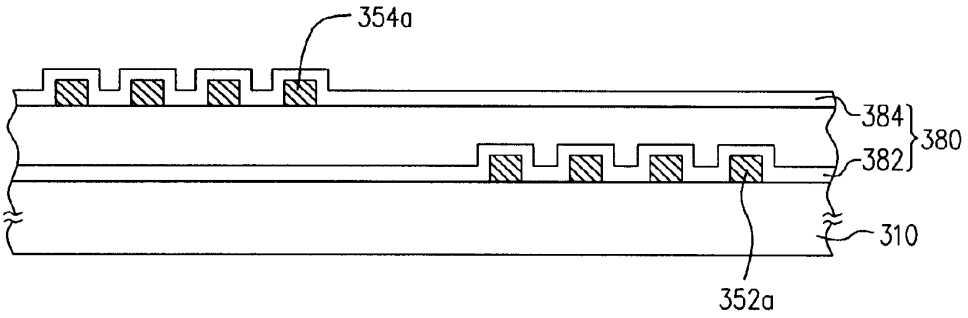


图 5A

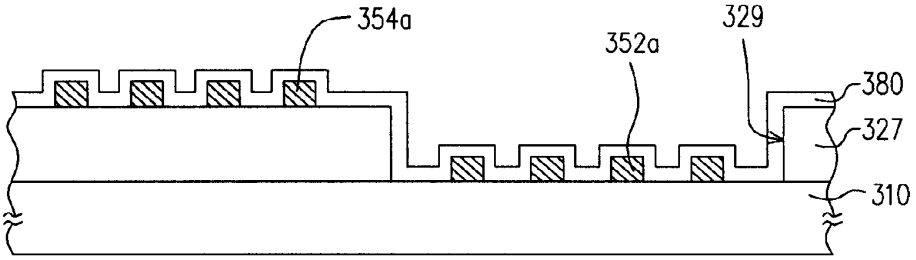


图 5B

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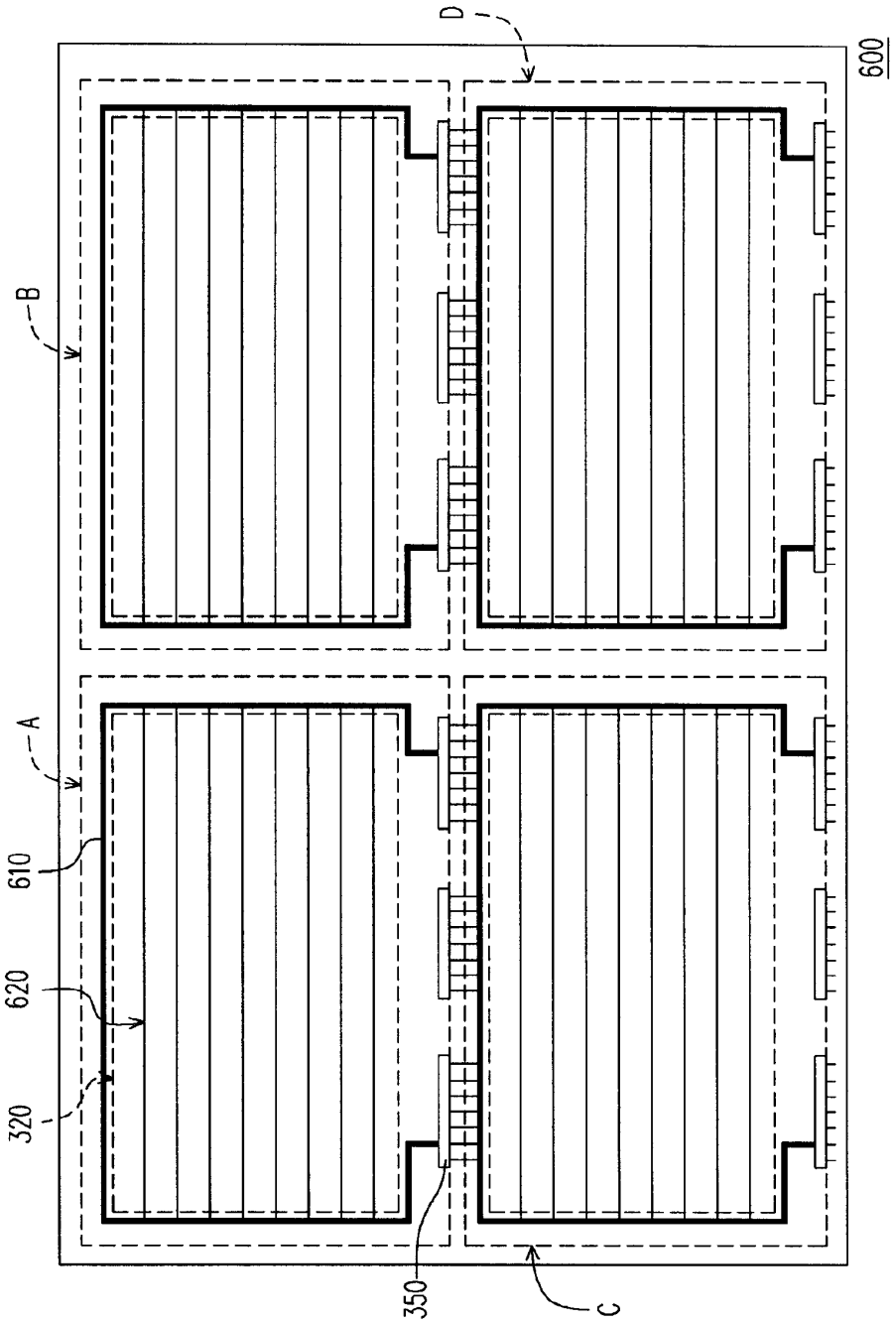


图 6

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Abstract of CN 103000625

An integrated circuit structure includes first and second integrated circuit devices disposed on an interposer. Each integrated circuit device has electrostatic discharge (ESD) protection circuitry therein connected to an internal ESD bus. The first and second integrated circuit devices communicate with one another through the interposer. The interposer includes an ESD bus electrically connected to the ESD busses of the first and second integrated circuit devices for providing cross-device ESD protection for the integrated circuit devices.

(19)中华人民共和国国家知识产权局

(12)发明专利申请

(10)申请公布号 CN 103000625 A
(43)申请公布日 2013.03.27

(21)申请号 201210019492.X

(22)申请日 2012.03.09

(30)优先权数据
13/227,502 2011.09.08 US

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(51)Int.Cl.
H01L 27/02(2006.01)
H02H 9/04(2006.01)

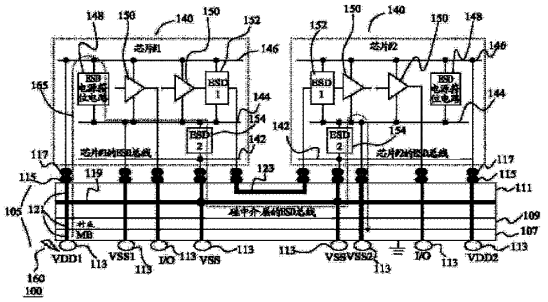
权利要求书 2 页 说明书 8 页 附图 8 页

(54)发明名称

2．5D/3D集成电路系统的ESD保护

(57)摘要

本发明涉及一种集成电路结构，包括设置在中介层上的第一集成电路器件和第二集成电路器件。每个集成电路器件中都具有与内部ESD总线连接的静电放电(ESD)保护电路。第一和第二集成电路器件通过中介层相互通信。为了向集成电路器件提供交叉器件的ESD保护，该中介层包括与第一和第二集成电路器件的ESD总线电连接的ESD总线。本发明还提供了一种2.5D/3D集成电路系统的ESD保护。



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1. 一种集成电路结构，包括：

第一集成电路器件和第二集成电路器件，设置在中介层上，每个集成电路器件中都具有与内部 ESD 总线相连接的静电放电 (ESD) 保护电路，所述中介层包括与所述第一集成电路器件和所述第二集成电路器件的所述 ESD 总线电连接的 ESD 总线，用于向所述集成电路器件提供交叉器件 ESD 保护。

2. 根据权利要求 1 所述的集成电路，其中，所述第一集成电路器件和所述第二集成电路器件通过所述中介层与位于所述中介层的底面的相应接地连接器相连接，并且所述中介层的 ESD 总线与位于所述中介层的底面的相应接地连接器电连接。

3. 根据权利要求 1 所述的集成电路，其中，所述中介层包括金属互连层，并且所述中介层的所述 ESD 总线形成在所述金属互连层内的金属线级层内。

4. 根据权利要求 3 所述的集成电路结构，其中，所述中介层的所述 ESD 总线以网状结构被布置在所述第一集成电路器件和所述第二集成电路器件下面。

5. 根据权利要求 4 所述的集成电路结构，并且其中，所述第一集成电路器件和所述第二集成电路器件的 ESD 总线直接与所述中介层的 ESD 总线电连接，而在其间没有连接任何有源器件。

6. 根据权利要求 4 所述的结成电路结构，其中，所述第一集成电路和所述第二集成电路至少包括：第一 ESD 保护电路和第二 ESD 保护电路，所述第一 ESD 保护电路和所述第二 ESD 保护电路分别电连接在所述第一集成电路器件的 ESD 总线和所述第二集成电路器件的 ESD 总线与所述中介层的 ESD 总线之间。

7. 根据权利要求 3 所述的集成电路结构，其中，所述中介层的所述 ESD 总线包括：

第一环形结构，设置在所述第一集成电路器件下面；以及

第二环形结构，设置在所述第二集成电路器件下面，并且与所述中介层中的所述第一环形结构相连接。

8. 根据权利要求 7 所述的集成电路结构，其中，所述第一集成电路器件的 ESD 总线和所述第二集成电路器件的 ESD 总线分别直接与所述第一环形结构和所述第二环形结构电连接，而在其间没有连接任何有源器件。

9. 根据权利要求 7 所述的集成电路，其中，所述第一集成电路和所述第二集成电路至少包括第一 ESD 保护电路和第二 ESD 保护电路，所述第一 ESD 保护电路和所述第二 ESD 保护电路分别电连接在所述第一集成电路器件和所述第一环形结构之间以及所述第二集成电路器件和所述第二环形结构之间。

10. 根据权利要求 1 所述的集成电路结构，至少包括：第一 ESD 保护电路和第二 ESD 保护电路，所述第一 ESD 保护电路和所述第二 ESD 保护电路分别电连接在所述第一集成电路器件的低电源节点和所述第二集成电路器件的低电源节点与所述中介层的所述 ESD 总线之间。

11. 根据权利要求 10 所述的集成电路结构，其中，所述第一 ESD 保护电路和所述第二 ESD 保护电路分别包括在所述第一集成电路器件和所述第二集成电路器件内，并且电连接在每个集成电路器件的所述低电源节点和 ESD 总线之间。

12. 根据权利要求 10 所述的集成电路结构，其中，所述第一 ESD 保护电路和所述第二 ESD 保护电路形成在所述中介层中。

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13. 根据权利要求 10 所述的集成电路结构，其中，所述第一 ESD 保护电路和所述第二 ESD 保护电路均包括交叉相连的二极管对。

14. 一种集成电路结构，包括：

中介层，包括金属互连层和所述金属互连层之间的衬底层；以及

第一集成电路芯片和第二集成电路芯片，设置在所述中介层上，每个集成电路器件具有芯片上静电放电 (ESD) 保护电路，每个集成电路芯片的所述芯片上 ESD 保护电路都包括用于电源到接地保护的 ESD 电源箝位电路以及输入 / 输出 (I/O) 信号 ESD 保护电路；以及

第一噪声隔离 ESD 保护电路和第二噪声隔离 ESD 保护电路，分别用于隔离与所述第一集成电路芯片和所述第二集成电路芯片相关的不同的接地之间的噪声；以及

其中，为了向所述集成电路芯片提供交叉器件 ESD 保护，所述中介层包括与所述第一噪声隔离 ESD 保护电路和所述第二噪声隔离 ESD 保护电路电连接的 ESD 总线。

15. 根据权利要求 14 所述的集成电路，其中，所述第一集成电路芯片和所述第二集成电路芯片分别通过所述中介层在所述中介层的所述金属互连层之一处与第一接地连接器和第二接地连接器连接，并且所述中介层的所述 ESD 总线在所述金属互连层之一处与中介层接地连接器电连接。

16. 根据权利要求 15 所述的集成电路结构，其中，所述第一接地连接器和所述第二接地连接器分别与所述第一集成电路芯片和所述第二集成电路芯片的所述 ESD 电源箝位电路以及 I/O 信号 ESD 保护电路相连接。

17. 根据权利要求 16 所述的集成电路结构，其中，所述中介层的 ESD 总线包括：位于所述第一集成电路芯片和所述第二集成电路芯片下面的金属线网，所述第一集成电路芯片和所述第二集成电路芯片形成在另一个所述金属互连层内。

18. 根据权利要求 17 所述的集成电路结构，其中，所述第一噪声隔离 ESD 保护电路和所述第二噪声隔离 ESD 保护电路形成在所述中介层中，并且分别电连接在所述第一接地连接器和所述第二接地连接器与所述中介层的 ESD 总线之间。

19. 根据权利要求 16 所述的集成电路结构，其中，所述顶面金属互连层内的 ESD 总线包括：第一环形结构；位于所述第一集成电路芯片下面；以及第二环形结构；位于所述第二集成电路芯片下面并且与所述第一环形结构相连接。

20. 根据权利要求 19 所述的集成电路结构，其中，所述第一噪声隔离 ESD 保护电路和所述第二噪声隔离 ESD 保护电路形成在所述中介层中并且分别电连接在所述第一接地连接器和所述第二接地连接器与所述中介层的 ESD 总线之间。

21. 一种集成电路结构，包括：

第一集成电路器件和第二集成电路器件，设置在有源中介层上，为了传送交叉芯片 ESD 电流，所述有源中介层包括与所述第一集成电路器件和所述第二集成电路器件电连接的 ESD 总线，所述有源中介层包括形成在每个集成电路器件中的所述每个集成电路器件的 ESD 保护电路，所述每个集成电路器件都与所述有源中介层的 ESD 总线电连接。

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2.5D/3D 集成电路系统的 ESD 保护

技术领域

[0001] 本发明涉及的是集成电路结构的 ESD 保护方案，并且更具体地涉及的是 2.5D/3D 集成电路结构的 ESD 保护方案。

背景技术

[0002] 集成电路（“IC”）被集成到许多电子器件中。IC 封装的发展使得可以将多个 IC 垂直地叠加在所谓的三维（“3D”）封装件中，从而节省了印刷电路板（“PCB”）上的水平面积。为将一个或多个管芯与 PCB 相连接，被称为 2.5D 封装件的可选的封装技术可以使用中介层，该中介层可以由半导体材料（诸如，硅）形成。中介层是一种经常被用来为互连布线或被用作为不同 IC 芯片的接地面 / 电源面的中间层。在中介层上装配了可以属于同类技术或不同类技术的多个 IC 芯片。在中介层中通过导电图案为多个 IC 之间的连接布线。在现今的 2.5D/3D 应用中的 ESD 保护仍局限于没有任何芯片对芯片 ESD 放电路径的内部芯片 ESD 保护。

发明内容

[0003] 根据本发明的一个方面，提供了一种集成电路结构，包括：第一集成电路器件和第二集成电路器件，设置在中介层上，每个集成电路器件中都具有与内部 ESD 总线相连接的静电放电 (ESD) 保护电路，所述中介层包括与所述第一集成电路器件和所述第二集成电路器件的所述 ESD 总线电连接的 ESD 总线，用于向所述集成电路器件提供交叉器件 ESD 保护。

[0004] 在该集成电路中，所述第一集成电路器件和所述第二集成电路器件通过所述中介层与位于所述中介层的底面的相应接地连接器相连接，并且所述中介层的 ESD 总线与位于所述中介层的底面的相应接地连接器电连接。

[0005] 在该集成电路中，所述中介层包括金属互连层，并且所述中介层的所述 ESD 总线形成在所述金属互连层内的金属线级层内。

[0006] 在该集成电路中，所述中介层的所述 ESD 总线以网状结构被布置在所述第一集成电路器件和所述第二集成电路器件下面。

[0007] 在该集成电路中，所述第一集成电路器件和所述第二集成电路器件的 ESD 总线直接与所述中介层的 ESD 总线电连接，而在其间没有连接任何有源器件。

[0008] 在该集成电路中，所述第一集成电路和所述第二集成电路至少包括：第一 ESD 保护电路和第二 ESD 保护电路，所述第一 ESD 保护电路和所述第二 ESD 保护电路分别电连接在所述第一集成电路器件的 ESD 总线和所述第二集成电路器件的 ESD 总线与所述中介层的 ESD 总线之间。

[0009] 在该集成电路中，所述中介层的所述 ESD 总线包括：第一环形结构，设置在所述第一集成电路器件下面；以及第二环形结构，设置在所述第二集成电路器件下面，并且与所述中介层中的所述第一环形结构相连接。

[0010] 在该集成电路中，所述第一集成电路器件的 ESD 总线和所述第二集成电路器件的

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ESD 总线分别直接与所述第一环形结构和所述第二环形结构电连接，而在其间没有连接任何有源器件。

[0011] 在该集成电路中，所述第一集成电路和所述第二集成电路至少包括第一 ESD 保护电路和第二 ESD 保护电路，所述第一 ESD 保护电路和所述第二 ESD 保护电路分别电连接在所述第一集成电路器件和所述第一环形结构之间以及所述第二集成电路器件和所述第二环形结构之间。

[0012] 在该集成电路中，至少包括：第一 ESD 保护电路和第二 ESD 保护电路，所述第一 ESD 保护电路和所述第二 ESD 保护电路分别电连接在所述第一集成电路器件的低电源节点和所述第二集成电路器件的低电源节点与所述中介层的所述 ESD 总线之间。

[0013] 在该集成电路中，所述第一 ESD 保护电路和所述第二 ESD 保护电路分别包括在所述第一集成电路器件和所述第二集成电路器件内，并且电连接在每个集成电路器件的所述低电源节点和 ESD 总线之间。

[0014] 在该集成电路中，所述第一 ESD 保护电路和所述第二 ESD 保护电路形成在所述中介层中。

[0015] 在该集成电路中，所述第一 ESD 保护电路和所述第二 ESD 保护电路均包括交叉相连的二极管对。

[0016] 根据本发明的另一方面，提供了一种集成电路结构，包括：中介层，包括金属互连层和所述金属互连层之间的衬底层；以及第一集成电路芯片和第二集成电路芯片，设置在所述中介层上，每个集成电路器件具有芯片上静电放电 (ESD) 保护电路，每个集成电路芯片的所述芯片上 ESD 保护电路都包括用于电源到接地保护的 ESD 电源箝位电路以及输入 / 输出 (I/O) 信号 ESD 保护电路；以及第一噪声隔离 ESD 保护电路和第二噪声隔离 ESD 保护电路，分别用于隔离与所述第一集成电路芯片和所述第二集成电路芯片相关的不同的接地之间的噪声；以及其中，为了向所述集成电路芯片提供交叉器件 ESD 保护，所述中介层包括与所述第一噪声隔离 ESD 保护电路和所述第二噪声隔离 ESD 保护电路电连接的 ESD 总线。

[0017] 在该集成电路中，所述第一集成电路芯片和所述第二集成电路芯片分别通过所述中介层在所述中介层的所述金属互连层之一处与第一接地连接器和第二接地连接器连接，并且所述中介层的所述 ESD 总线在所述金属互连层之一处与中介层接地连接器电连接。

[0018] 在该集成电路中，所述第一接地连接器和所述第二接地连接器分别与所述第一集成电路芯片和所述第二集成电路芯片的所述 ESD 电源箝位电路以及 I/O 信号 ESD 保护电路相连接。

[0019] 在该集成电路中，所述中介层的 ESD 总线包括：位于所述第一集成电路芯片和所述第二集成电路芯片下面的金属线网，所述第一集成电路芯片和所述第二集成电路芯片形成在另一个所述金属互连层内。

[0020] 在该集成电路中，所述第一噪声隔离 ESD 保护电路和所述第二噪声隔离 ESD 保护电路形成在所述中介层中，并且分别电连接在所述第一接地连接器和所述第二接地连接器与所述中介层的 ESD 总线之间。

[0021] 在该集成电路中，所述顶面金属互连层内的 ESD 总线包括：第一环形结构；位于所述第一集成电路芯片下面；以及第二环形结构；位于所述第二集成电路芯片下面并且与所述第一环形结构相连接。

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[0022] 在该集成电路中，所述第一噪声隔离 ESD 保护电路和所述第二噪声隔离 ESD 保护电路形成在所述中介层中并且分别电连接在所述第一接地连接器和所述第二接地连接器与所述中介层的 ESD 总线之间。

[0023] 根据本发明的又一方面，提供了一种集成电路结构，包括：第一集成电路器件和第二集成电路器件，设置在有源中介层上，为了传送交叉芯片 ESD 电流，所述有源中介层包括与所述第一集成电路器件和所述第二集成电路器件电连接的 ESD 总线，所述有源中介层包括形成在每个集成电路器件中的所述每个集成电路器件的 ESD 保护电路，所述每个集成电路器件都与所述有源中介层的 ESD 总线电连接。

附图说明

[0024] 所附的视图示出的是本发明的优选实施例以及根据本公开的其他信息，其中：

[0025] 图 1 是 2.5D/3D 集成电路封装件的实施例的示意图；

[0026] 图 2 示出的是 2.5D/3D 集成电路封装件的 ESD 保护方案的实施例；

[0027] 图 3 示出的是在图 2 的 2.5D/3D 集成电路封装件的中介层内的 ESD 总线的一个实施例；

[0028] 图 4 示出的是在图 2 的 2.5D/3D 集成电路封装件的中介层内的 ESD 总线的另一个实施例；

[0029] 图 5 示出的是 2.5D/3D 集成电路封装件的 ESD 保护方案的实施例；

[0030] 图 6 示出的是在图 5 的 2.5D/3D 集成电路封装件的中介层内的 ESD 总线的一个实施例；

[0031] 图 7 示出的是在图 5 的 2.5D/3D 集成电路封装件的中介层内的 ESD 总线的另一个实施例；以及

[0032] 图 8A- 图 8C 示出的是使用在图 1 的 2.5D/3D 集成电路封装件中的 ESD 保护电路的实施例。

具体实施方式

[0033] 对于示例性实施例的描述旨在接合附图进行阅读，附图被认为是整个书面描述的一部分。应该理解，在该说明中的相对关系术语，诸如，“下面的”、“上面的”、、“水平的”、“垂直的”、“在 ... 上面”、“在 ... 下面”、“向上的”、“向下的”、“顶部”和“底部”以及其派生词（例如，“水平地”、“向下地”、“向上地”等）与随后所描述的或在论述过程中视图所示出的方向相关。这些相对关系术语旨在更容易地描述，并不要求部件按此特定的方向装配或操作。除非另有明确说明，否则这些涉及了连接，耦合等的术语（诸如“连接的”和“互连的”）涉及的是彼此直接固定或连接或通过中间结构间接地固定或附接的结构之间的关系，以及两者可移动或不可移动的连接或关系。另外，除非另有说明，否则关于电连接等的术语（诸如，“接合的”、“连接的”以及“互连的”）涉及的都是相互直接通信或通过中间结构间接通信的结构之间的关系。

[0034] 在本文中公开的改进的 2.5D/3D 集成电路 (IC) 设计提供了用于提供交叉芯片 (cross-chip)ESD 保护的整体 ESD 总线。在该改进的技术中，在 2.5D/3D IC 的整个 I/O 范围内连续地设置 ESD 总线提供了可靠的 ESD 保护。在实施例中，为了获得可靠的“交叉芯

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片”ESD 保护，整体的 ESD 总线被结合到与每个芯片的 ESD 总线相连接的中介层中。

[0035] 图 1 是 2.5D/3D 集成电路封装件 10 的实例的高示意性视图。由于通常的 ESD 保护结构既应用于 2.5D 设计又应用于 3D 设计，所以该封装件在此被称为“2.5D/3D”设计。如图 1 所示，2.5D/3D IC 封装件 10 包括设置在中介层 20 上的芯片 30 的三芯片堆叠。该芯片堆叠 30 的芯片被标记为“芯片 #1-1”、“芯片 #1-2”以及“芯片 #1-3”。芯片堆叠 30 中的每个芯片都具有其自身的用于导通 ESD 电流的 ESD 总线 32。第二、第三和第四芯片 40、50 和 60 也分别设置在中介层 20 上并且具有其自身的相应的 ESD 总线 42、52 和 62。要特别注意的是，该中介层具有其自身的整体 ESD 总线 22，如下面更详细地描述的该总线 22 与芯片 30、40、50、60 的 ESD 总线相连接。芯片 30、40、50、60 彼此互连并且通过小的导电凸块 70 与中介层 20 互连，该导电凸块 70 可以被称为“微凸块”或“μ 凸块”。为了将 IC 封装件 10 与在其上设置了该 IC 封装件的印刷电路板（“PCB”）（未示出）相连接，将导电凸块或导电球 62 设置在中介层 20 的底面上。通常，PCB 可以具有形成在其底面上的更大的导电“球”。将 IC 芯片与中介层 20 相连接的微凸块 70 可以具有与将中介层 20 与 PCB 相连接的凸块 62 所不同的尺寸和电性能。

[0036] 应该理解，设置在中介层上的芯片可以属于同类设计或不同类设计并且可以（仅作为实例）是逻辑芯片、存储芯片、存储器堆叠件、现场可编程门阵列 (FPGA)、集成的无源器件 (IPD) 或微处理器。

[0037] 本领域的技术人员将熟知，中介层 20 包括了半导体衬底（例如，硅衬底），该半导体衬底具有分别形成在其正面和背面的主要面上的正面互连层和背面互连层。在一些应用中，衬底是不接地的，并且由此是电浮动的。正面互连层和背面互连层中的每个都可以包括多个金属间介电 (IMD) 层，这些金属间介电层包括通孔级层 (via level layer)(V1、V2 等) 以及金属线级层 (metal line level layer)（例如，M1、M2 等）。当然，该中介层也可以包括并且使用其他连接层，诸如，PO、OD 或 RDL 层。正面互连层中的导体可以通过从半导体衬底的正面延伸到半导体衬底的背面的硅通孔（“TSV”）与背面互连层中的金属导体电连接。根据对中介层结构的这种大概了解，根据图 2- 图 7 对 2.5D/3D IC 系统的 ESD 保护方案的实施例进行说明。

[0038] 图 2 示出的是 2.5D/3D IC 封装件 100 的实现方式，该封装件具有在无源中介层内的整体 ESD 总线，该无源中介层与每个芯片的 ESD 整体总线相连接，从而提供了完整的交叉芯片 ESD 保护网络。尽管所示的 2.5D/3D IC 封装件 100 仅具有两个芯片（被标记为芯片 #1 和芯片 #2），但应该理解，该设计同样适用于具有两个以上芯片的封装件，诸如，图 1 中所示的封装件。

[0039] 就其 ESD 保护方面而言，每个芯片 140 都具有通常的内部 ESD 保护方案。每个芯片都具有连接在高电源轨 146 和低电源轨 144 之间并且与 I/O 输入端（在图 2 的底部被标记为“I/O”）相连接的 I/O 缓冲器 150。每个芯片 140 还都包括：连接在供电轨道 144、146 之间的用于 I/O ESD 保护的 ESD 电源箝位电路 148 和第一 ESD 保护模块 152（被标记为“ESD1”）以及连接在供电轨道 144 和芯片 ESD 总线 142 之间的用于噪声 ESD 保护的第二 ESD 模块 154。应该理解，根据设计要求，每个芯片 140 都可以包括多个 ESD 模块 148，152 和模块 154。每个芯片的低电源轨都与相应的接地凸块连接器 113(VSS1 或 VSS2) 相连接，该接地凸块连接器具有相应的接地分配器。中介层 105（下面进行描述）的 ESD 总线 119 与

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接地连接器 (VSS) 相连接，该接地连接器具有与集成电路器件相连接的接地连接器 VSS1、VSS2 不同的接地分配器 (ground assignment)。地电位 VSS1、VSS2 和 VSS 可以通过 PCB 的与相同的接地分配器相连接，但对于噪声隔离而言，接地 VSS1、VSS2、VSS 在 IC 芯片级上是断开的。当然，对于不考虑噪声隔离的 IC 系统而言，VSS1、VSS2 和 VSS 可以与集成电路器件的相同的接地分配器连接，并且在此情况下可以省略 ESD2 保护。

[0040] 图 8A- 图 8C 示出了 ESD 电源箝位电路 148 以及第一和第二 ESD 模块 152、154 的常规实施例。图 8A 具体地示出了包括 RC 电路（由电阻器 R 和电容器 C 形成）、反相器 I 以及晶体管 T 的电源箝位电路 148。图 8B 示出的是 ESD 模块 152，并且该模块包括一对堆叠的二极管 D1 和 D2，这对二极管连接在电源线和地线 146、144 之间，在其间连接有 I/O 节点。该 ESD 模块 152 被配置成提供输入 / 输出 (I/O) 信号 ESD 保护电路。最后，图 8C 中示出了 ESD 模块 154 并且该 ESD 模块 154 包括一对交叉连接（背对背）的二极管 D3 和 D4，这对二极管连接在低电源轨 144 和芯片的 ESD 总线 142 之间。该模块提供了噪声隔离 ESD 保护电路并且通过中介层的 ESD 总线完成了 ESD 保护网络。

[0041] 回到图 2，以参考标号 105 表示多层中介层。该多层中介层 105 包括（从底部到顶部）背面金属互连层 107、衬底层 109 以及顶面或正面金属互连层 111。背面金属互连层 107 及正面金属互连层 111 皆可能包含多层金属层及介电层供多层金属绕线使用。导电凸块 113 被设置在底面互连层 107 处并且被标记为 VDD1 和 VDD2（分别用于芯片 #1 和芯片 #2 高电源）、VSS1 和 VSS2（分别用于芯片 #1 和芯片 #2 低电源（即，接地））、I/O（用于芯片 I/O) 以及 VSS（共用于芯片 #1、芯片 #2 以及中介层 ESD 接地）。为了与芯片 140 的相匹配的微凸块 117 相连接，中介层 105 具有微凸块 115。每组微凸块 115、117 都通过穿过中介层 105 形成的导电通孔 121（以及任选的一个或多个横向的金属互连件）与对应的导电凸块 113 相连接。在一个实施例中，ESD 总线 119 形成在顶面金属互连层 111 内并且通过其各自的导电通孔 121 与 VSS 导电凸块相连接。当然，ESD 总线 119 也可以整体地或部分地在中介层内的其他互连层（仅作为实例，背面金属层、RPL 层、OD 层或 PO 层）中形成。芯片 140 的 I/O 通过位于顶面金属互连件 111 中的一个或多个导线 123 连接在一起，从而允许芯片间相通信。中介层 105 的 ESD 总线 119 用于消除位于任意两个不同的芯片引脚之间的交叉芯片的 ESD 事件。例如，图 2 中所示的虚线路径 165 示出的是用于芯片 #1 的 VDD1 终端上的 ESD 事件 160 的放电路径。该放电路径 165 以如下方式进行 ：从 VDD1 终端 / 凸块经过中介层 105 的对应的导电通孔 121 ；到达芯片 #1 的高电源轨 146 ；经过芯片 #1 的 ESD 电源箝位电路 148 ；经过芯片 #1 的低电源轨 144 ；经过芯片 #1 的 ESD2 模块 154 ；进入并且经过中介层 105 的 ESD 总线 119 ；到达芯片 #2 的低电源轨 144 ；并且向下通过中介层 105 内的对应的导电通孔到达芯片 #2 的 VSS2 终端。在不连接中介层 105 内的 ESD 总线 119 的情况下，释放交叉芯片 ESD 电流的唯一路径将会穿过位于两个芯片之间（例如，从轨道 146 到 I/O150、ESD 模块 152 并且经过界面导线 123 到达第二芯片）的界面信号，从而增大了界面电路处的 ESD 故障几率。

[0042] 图 3 示出的是中介层 200 的实施例的示意性俯视图。图 3 具体地示出了中介层内部的 ESD 总线（例如，图 1 中的 ESD 总线 22 或图 2 中的 ESD 总线 119) 的布局实施例。在该实施例中，ESD 总线 210 被布置在导电的网状布局 (mesh layout) 中，优选地是金属网状布局。如上面根据图 1 和图 2 所论述的那样，芯片（诸如，芯片 220a、220b、220c 和 220d（通

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过虚线轮廓示出））被设置在中介层 200 和 ESD 总线 210 上方。芯片 220 到导电网 210（例如，到网交叉点 212 或偶数的网脚 214）的连接是通过从上面的芯片 220 穿过中介层 111 中的导电通孔 121 而构成的（见图 2）。同样地，从网 210 到导电凸块 113（尤其是 VSS 凸块 113）的连接是由穿过互连层 111、衬底 109 以及底部金属互连层 107 而形成的导电通孔 121 所构成的（再次见图 2）。该网布局提供了两个有益之处。首先，该网状布局提供了多个合适的位置来连接上面的芯片以及下面的导电凸块 113。因此该设计非常灵活，同时该设计还在网内留出了大量开口区域 216，通过这些开口区域可以形成与芯片 220（例如，VDD、VSS 和 I/O）的其他连接。其次，由于该网状总线简化了为 ESD 电流的通过提供短路径的选择性连接，所以该网状总线 210 允许了 ESD 放电的低电阻路径设计。这种能力改进了 ESD 性能。

[0043] 图 4 示出的是中介层 200A 的可选的实施例的示意性俯视图。图 4 具体地示出了中介层内的 ESD 总线（例如，图 1 中的 ESD 总线 22 或图 2 中的 ESD 总线 119）的布局的实施例。在该实施例中，ESD 总线 210A 被布置在多个连接的环 230a、230b、230c、230d 中，每个连接的环都与相应的上面的芯片 220a、220b、220c、220d 相结合。这些环分别限定出了较大的（与图 3 中的设计相比较的时候）开口区域 240a、240b、240c、240d，这些开口区域通过金属连接件 250 相连接。金属连接件 250 可以被配置成网，从而提供可以允许导电通孔穿过其延伸的开口区域 252。当中介层 200A 中的资源是有限的或非常昂贵的时候可以使用该实施例，这是因为，ESD 总线 210 在中介层中占用的金属区域更少（即，所占用的空间更小）并且留下了更多可以允许其他连接件（垂直的和水平的）穿过的开口区域。在该实施例中，优选地在环 230 的角上形成芯片到 ESD 总线的连接件，这些角中的一些被标记为角 235。也可以将 ESD 总线到导电凸块 113 连接件形成至角 235 或环状连接区域 250。

[0044] 图 5 示出的是 2.5D/3D IC 封装件 100A 的另一个实例。除了中介层 105 是有源的而不是无源的以外，IC 封装件 100A 与图 2 中所示的以及上面描述的 IC 封装件相同，并且类似的参考标号同样被用于表示类似的部件。图 5 中可以看出，IC 封装件 100A 包括经过修改的中介层 105A，该中介层被用于相关的经过修改的芯片 140A。芯片 140A 不包括噪声保护 ESD2 模块 154 或 ESD 总线 142（见图 2）。然而，经过修改的中介层 105A 中构造有与 ESD 总线 119A 相连接的 ESD2 模块 154A。芯片 140A 的低电源轨 144 被标记为芯片 140A 的 ESD 总线。

[0045] 图 2A 中所示的虚线路径 165A 示出的是放电路径，该放电路径用于分配到芯片 #1 的 VDD1 终端上的 ESD 事件。该放电路径以如下方式进行：从 VDD1 终端经过中介层 105A 的相应的导电通孔 121；到达芯片 #1 的高电源轨 146；经过芯片 #1 的 ESD 电源箝位电路 148；经过芯片 #1 的充当第一芯片 ESD 总线的低电源轨 144；进入中介层 105A 内部的第一 ESD2 模块 154A；经过中介层 105A 的 ESD 总线 119A；经过与芯片 #2 连接的第二 ESD2 模块 154A；并且向下通过中介层 105 内部的相应的导电通孔到达芯片 #2 的 VSS2 终端。在不连接中介层 105 内的 ESD 总线 119A 的情况下，两个芯片之间的界面电路将遭遇到交叉芯片的 ESD 事件并且处于该 ESD 事件所造成的危险下。

[0046] 尽管图 5 示出的是噪声隔离 ESD2 电路形成在有源的中介层 105A 中，但是应该理解，系统的其他 ESD 保护部件也可以形成在该有源中介层中，该其他 ESD 保护部件包括，例如，用于增强 IC 系统性能的 ESD 电源箝位电路和 / 或 I/O 信号 ESD 保护电路。

[0047] 图 6 示出的是中介层 300 的实施例的示例性俯视图。与图 3 类似，图 6 具体地示出

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了中介层内部的ESD总线（例如，图1的ESD总线22或图5中的ESD总线119A）的布局。在该实施例中，ESD总线210被布置在导电的网状布局中，优选地是金属网状布局。芯片320a、320b、320c和320d（通过虚线轮廓示出）被设置在中介层300上以及ESD总线119A上方。ESD2模块350形成在中介层105A（见图5）的衬底层109中并且在一个端部处通过中介层111内部的导电通孔和/或互连365与ESD总线310相连接，并且在另一个端部处通过导电互连和通孔360向上直到相应的芯片320的ESD总线。这些连接件的垂直方面可以出现在网开口316内。在该实施例中，芯片320不需要与ESD总线310直接连接，而是通过有源器件（即，通过ESD2模块350）进行连接。根据图3的实施例，从网310到导电凸块113（尤其是VSS凸块113）的连接件由穿过互连层111、衬底以及底部金属互连层107形成的导电通孔121构成（再次见图2）。

[0048] 应该理解，中介层中的整体ESD总线不必须形成在单个的导电层中。而是可以使用不同的导电层形成ESD总线，从而形成网连接。在实施例中，即使是背面金属层也能够用于形成部分的整体ESD总线。

[0049] 如上面根据图3所述的那样，网状的ESD总线布局提供了多个用于制造连接件的便利位置并且由此在设计上非常灵活，同时还能够在网内留下大量开口区域316，穿过这些开口区域可以形成与芯片320的其他连接件。中介层105A可以包括一个以上的用于每个芯片320的ESD2模块350。网状总线310为ESD放电提供了低电阻，这是因为，该网状总线减小了发生ESD事件的ESD路径的长度。这种能力改善了ESD性能。

[0050] 图7示出的是中介层300A的可选实施例的示意性俯视图。与图4类似，图7具体地示出了中介层内部的ESD总线（例如，图1的ESD总线22或图5中的ESD总线119A）的布局。在该实施例中，ESD总线310被布置在多个连接的环330a、330b、330c、330d中，每个连接的环都与相应的上面的芯片320a、320b、320c、320d相结合。这些环分别限定出了大的开口区域340a、340b、340c、340d，这些开口区域通过金属连接件350相连接，该金属连接件350可以被配置成网，从而提供了开口区域352，导电通孔连接穿过该开口区域352延伸。当中介层中的资源有限的时候，可以使用该实施例，这是因为ESD总线310在中介层中占用的金属区域更少（即，所占用的空间更小）并且提供了更多用于其他连接件（垂直的以及水平的）的开口区域。根据图6的实施例，芯片到ESD模块的连接件通过垂直的和水平的互连件360构成，而ESD模块到ESD总线的连接件通过垂直的和水平的互连件365构成。从ESD总线310A至导电凸块113的连接件可以在环形连接区域350的角335或边337中形成。

[0051] 尽管图2、图3、图6和图7所示出的ESD总线119、119A具有网状构造或环形构造，但应该理解，根据设计需要也可以使用其他形状和构造。通常，通过最小化ESD总线中的ESD路径的长度来增强ESD性能。以此原则作为指导，可以基于相应的芯片导电凸块70和中介层导线凸块62的位置以及中介层的互连层107、111内部的金属互连的布局来设计ESD总线布局。从上述公开中应该理解，中介层内部的ESD路径可以只包括无源部件（例如，导线和/或电容器）或可以包括有源部件（例如，二极管）。

[0052] 应该意识到，即使在本文中根据2.5D封装件的设计或混合的2.5D/3D设计对各个实施例进行了描述，其中，单个芯片和芯片堆叠件都被设置在中介层上，但应该理解，在此所述的ESD保护结构仍适用于带有芯片堆叠件和中介层的纯3D设计，该芯片堆叠件设置在

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中介层上并且该中介层部分用于在堆叠件的芯片之间通信。而且，甚至可以将该 ESD 保护结构使用在芯片不共享 I/O 的设计中，这是因为，ESD 事件可能发生在不同芯片的电源 / 接地引脚之间。该中介层为交叉芯片提供了 ESD 保护，从而提供了可靠并且全面的 ESD 保护。

[0053] 在本文中公开的 2.5D/3D 集成电路结构的一个实施例中，该集成电路结构包括设置在中介层上的第一集成电路器件和第二集成电路器件。每个集成电路器件在其中都具有与内部 ESD 总线连接的静电放电 (ESD) 保护电路。为了向集成电路器件提供交叉器件 ESD 保护，该中介层包括与第一和第二集成电路器件的 ESD 总线电连接的 ESD 总线。

[0054] 在 2.5D/3D 集成电路结构的其他实施例中，该结构包括中介层，该中介层具有金属互连层以及其间的衬底层，并且第一集成电路芯片和第二集成电路芯片被设置在该中介层上。每个集成电路器件都具有芯片上静电放电 (ESD) 保护电路。每个集成电路芯片的芯片上 ESD 保护电路都包括用于保护电源到接地的 ESD 电源箝位电路以及输入 / 输出 (I/O) 信号 ESD 保护电路。为了不同接地之间的噪声隔离，该 2.5D/3D 集成电路结构还包括分别与第一集成电路芯片和第二集成电路芯片相结合的第一噪声隔离 ESD 保护电路和第二噪声隔离 ESD 保护电路。为了向集成电路芯片提供交叉器件 ESD 保护，该中介层包括与第一噪声隔离 ESD 保护电路和第二噪声隔离 ESD 保护电路电连接的 ESD 总线。

[0055] 在另一个实施例中，集成电路结构包括设置在有源中介层上的第一集成电路器件和第二集成电路器件，为了传送交叉芯片的 ESD 电流，该有源中介层包括与第一集成电路器件和第二集成电路器件电连接的 ESD 总线。该有源中介层包括形成在每个集成电路器件中的与有源中介层的 ESD 总线电连接的每个集成电路器件的 ESD 保护电路。

[0056] 虽然已经通过示例性的实施例对本发明进行了描述，但本发明并不局限于此。相反地，所附的权利要求应该包括本发明的其他变型和实施例。本领域的技术人员可以在不背离本发明的范围和等效设置的范围的条件下实现这些变型和实施例。

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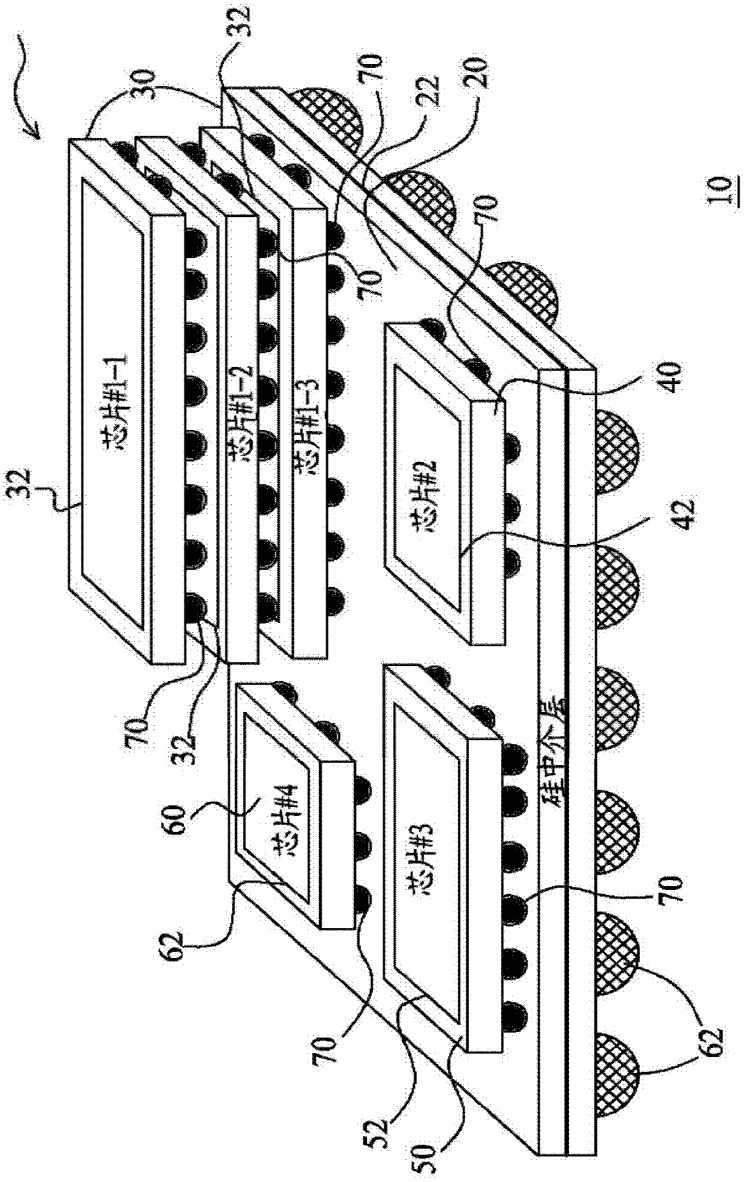


图 1

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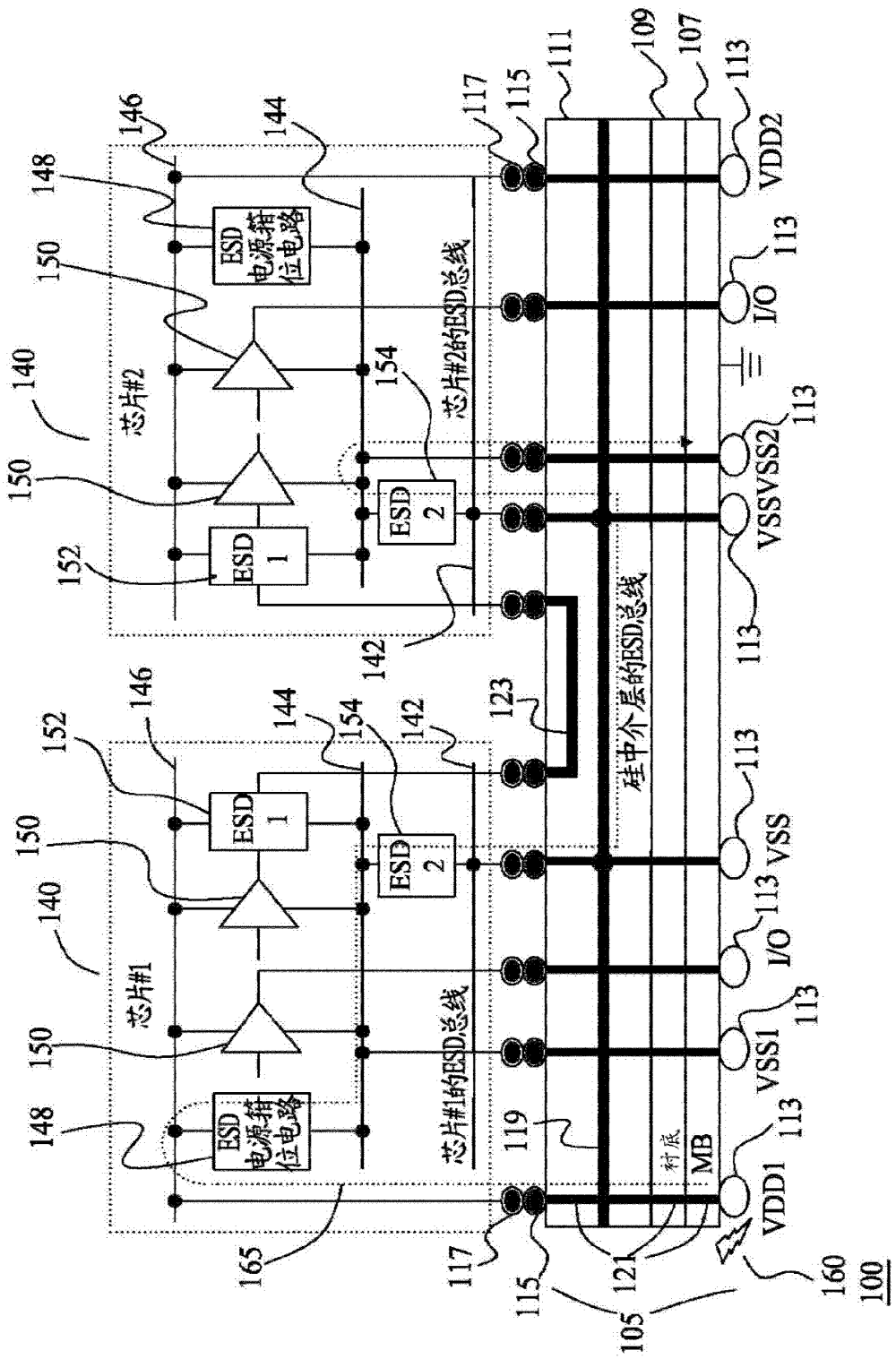


图 2

Micron Ex. 1002, p. 153
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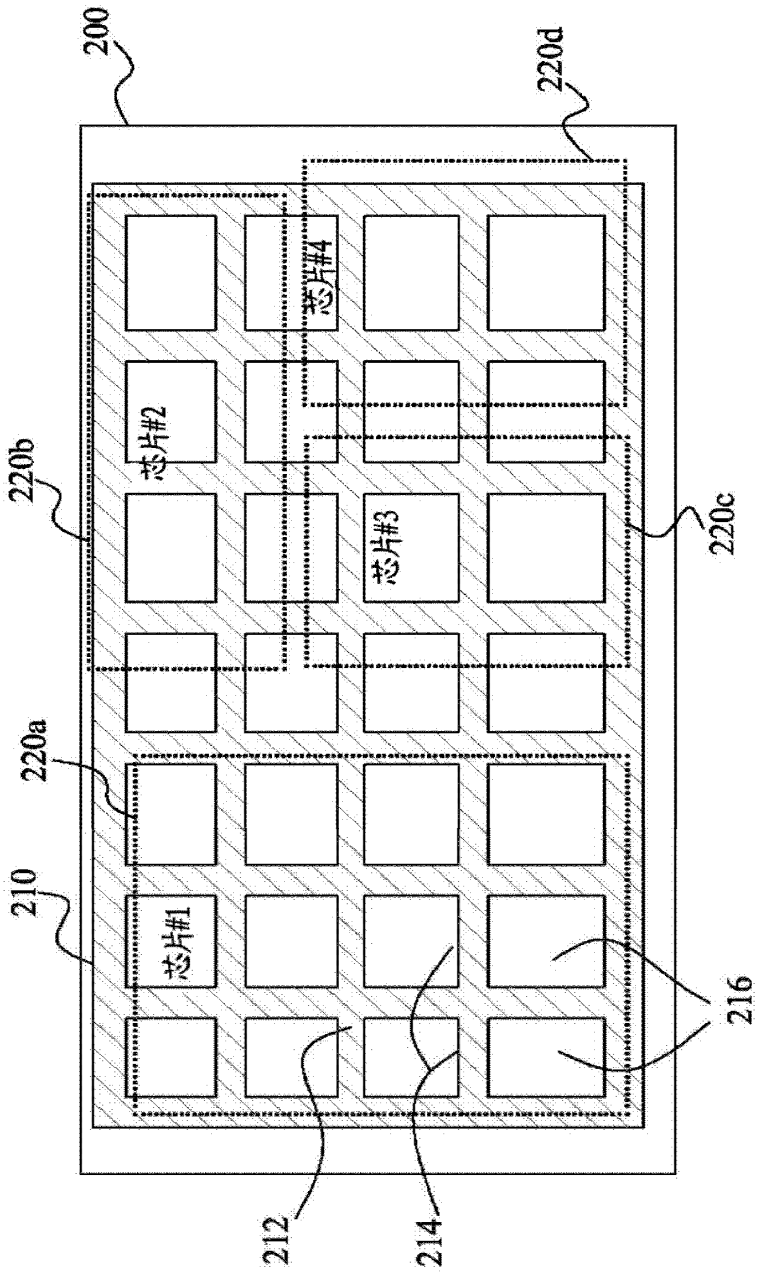


图 3

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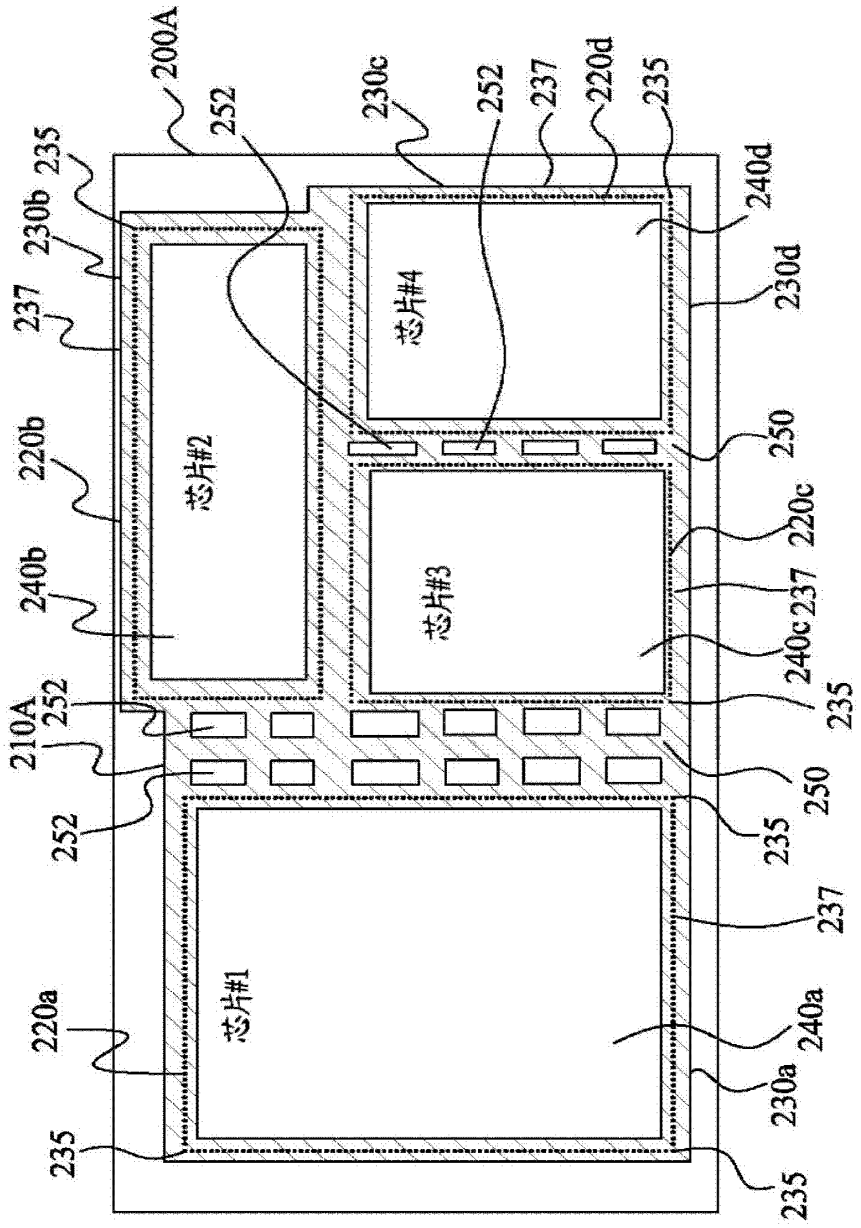


图 4

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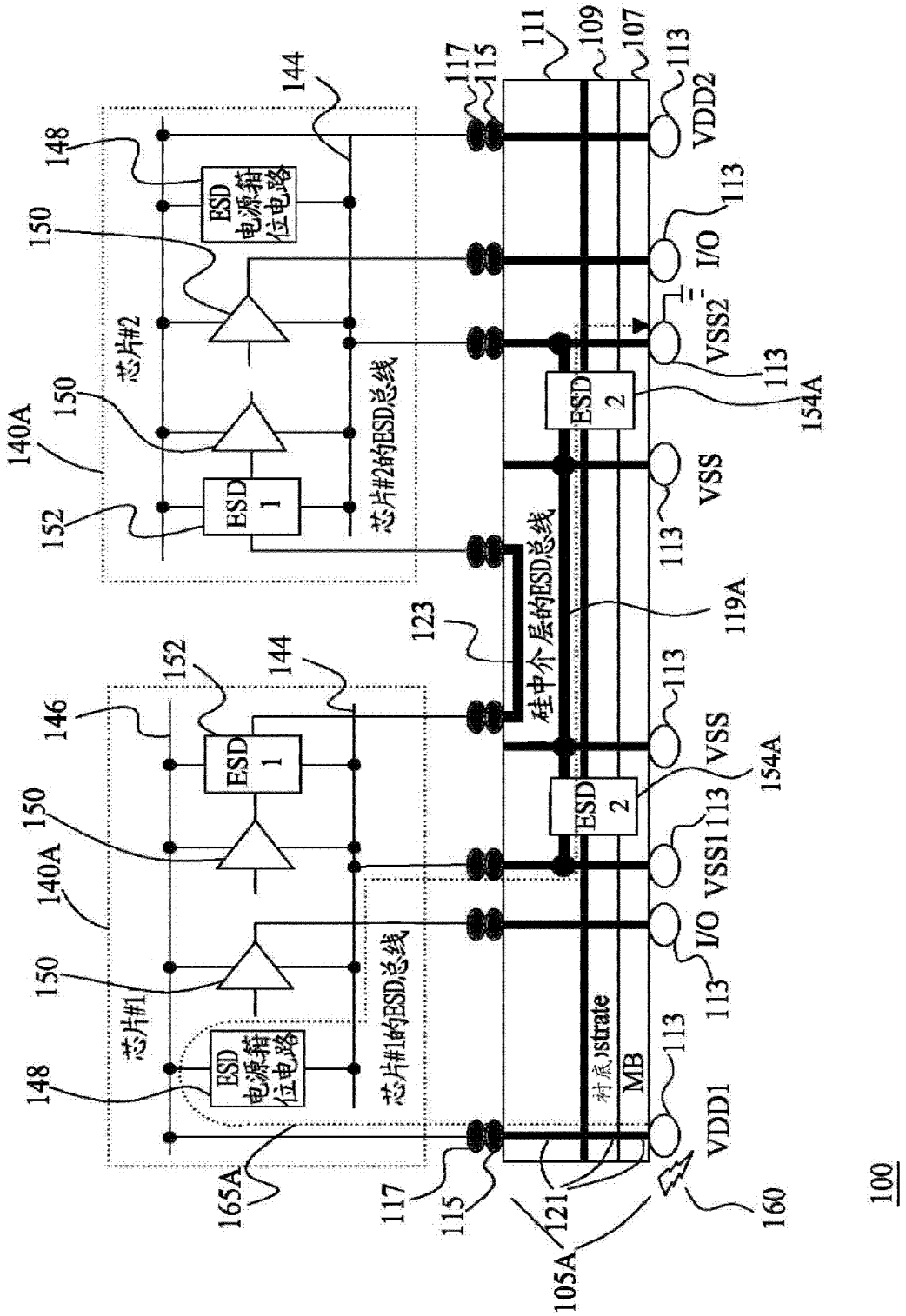


图 5

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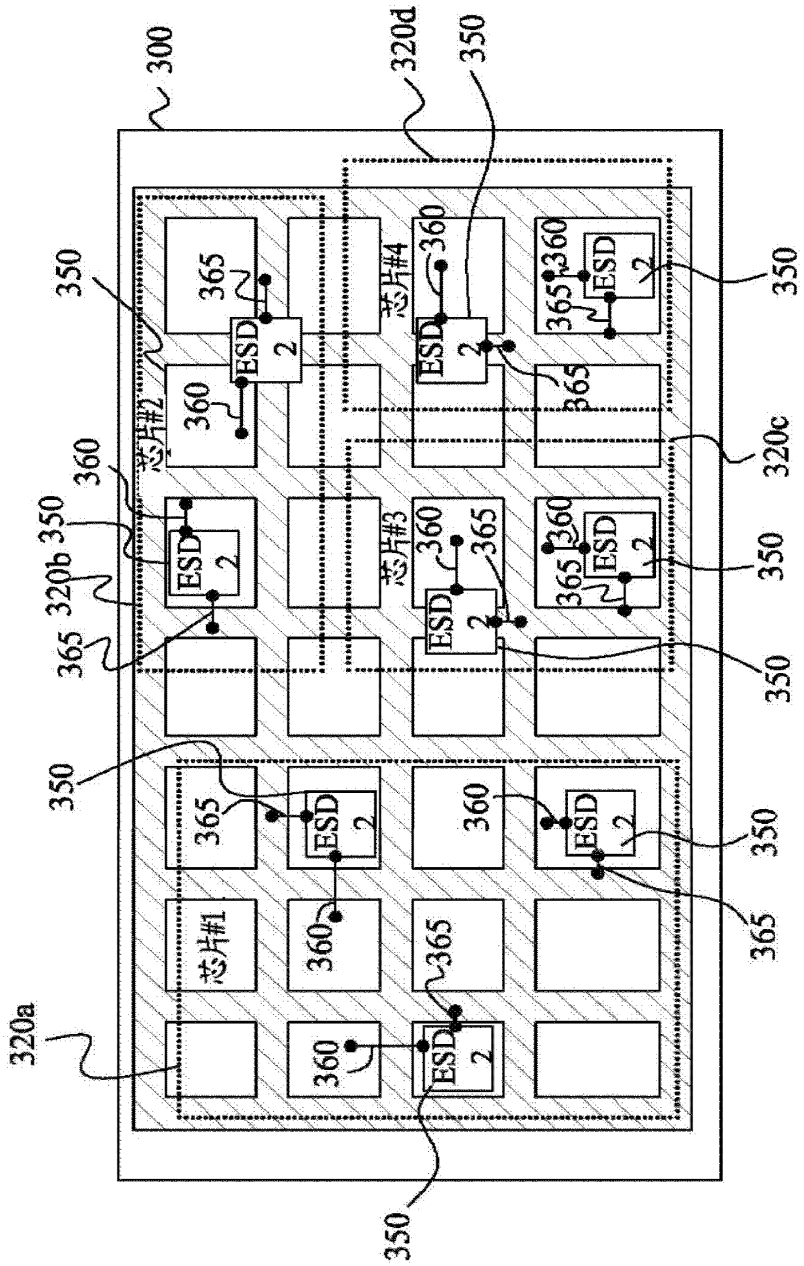


图 6

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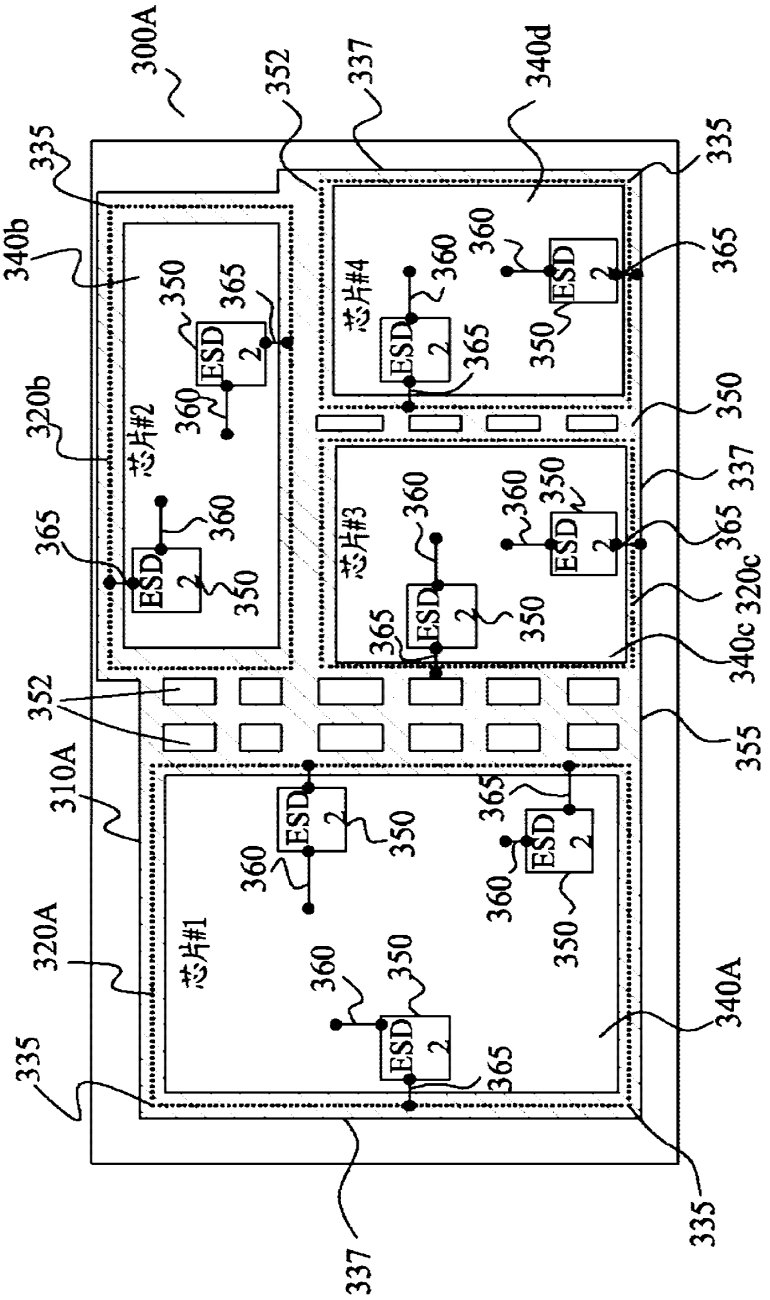


图 7

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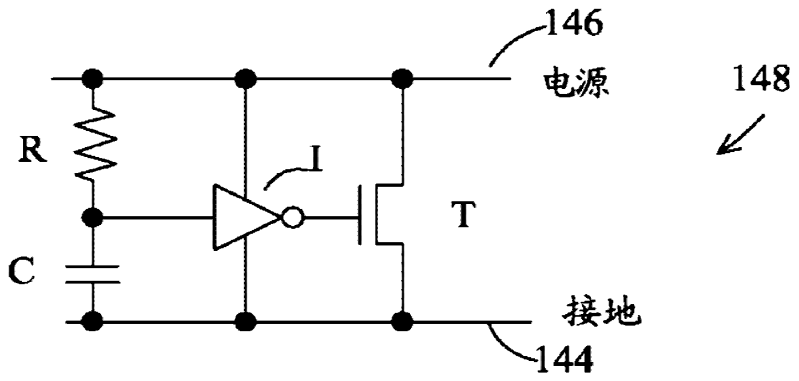


图 8A

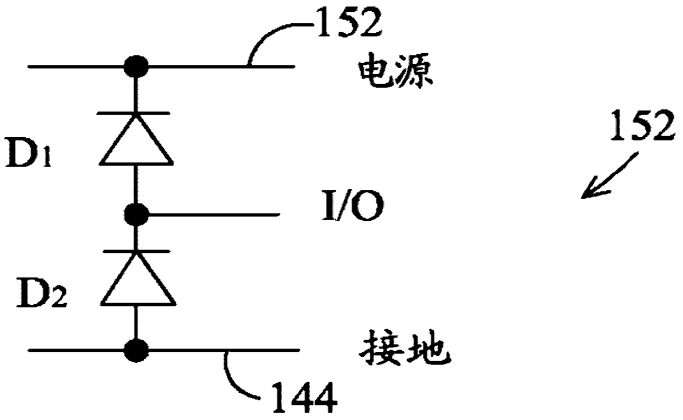


图 8B

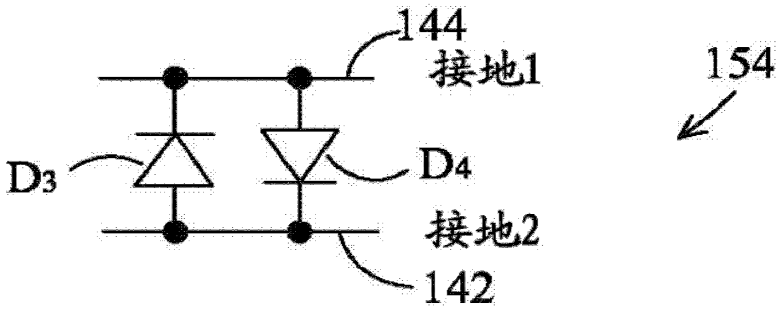


图 8C

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Abstract of KR 20020034470

PURPOSE: An electrostatic discharge (ESD) protection device is provided to realize an electrostatic discharge characteristic of high performance, by making each resistance of a drain path between ladders connected to a pad have the same value so that each unit ladder uniformly discharges charges.

CONSTITUTION: A plurality of ladders (61,62,63,64,65,66,67,68) are disposed. A pair of adjacent two ladders are connected to the first metal layer. The first metal layer (69a) is connected to the second metal layer (69b). The second metal layer is connected to the third metal layer (69c) connected to a pad(60). The metal layer is formed of a single or multi layer structure.

(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(11) 공개번호 특2002-0034470
(43) 공개일자 2002년05월09일

(51) 국제분류코드
H01L 27/04 (2006.01)

(21) 출원번호 10-2000-0064792

(22) 출원일자 2000년11월02일

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전체 청구항 수 : 총 3 항

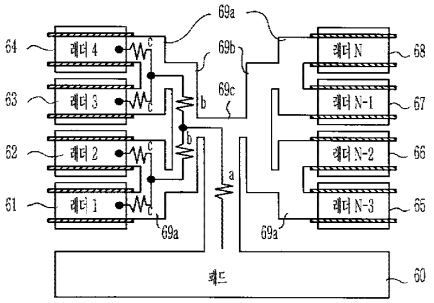
(54)정전기 방전 보호 소자

(57)요 약

본 발명은 정전기 방전 보호 소자(Electro Static Discharge protection device)에 관한 것으로, 특히 패드(PAD)에 연결되어 있는 각 래더(ladder) 간 드레인 경로(drain path)의 저항을 서로 동일하게 하므로써, 정전기 방전 보호 소자의 동작시 각 단위 래더들이 전체적으로 전하를 균일하게 방전하여 고성능(high performance)의 정전기 방전(ESD) 특성을 갖게하고, 패드 인풋 캡 스펙(PAD input cap spec)이 낮아(Ci < 2.4pF) 정전기 방전 보호 소자의 면적이 작아야만 하는 램버스 디램(Rambus DRAM)과 같은 고속 제품에 적합한 정전기 방전 보호 소자에 관하여 기술된다.

키워드 : 정전기 방전 보호 소자, ESD, 래더, 드레인 인풋 저항

대 표 도 - 도 6



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청구의 범위

청구항 1

다수의 래더가 배열되고, 상기 래더 중 이웃하는 2개의 래드를 한 쌍으로 하여 제 1 메탈 레이어에 의해 연결하고, 상기 제 1 메탈 레이어를 제 2 메탈 레이어로 연결하고, 상기 제 2 메탈 레이어를 패더에 연결된 제 3 메탈 레이어에 연결되도록 구성하는 것을 특징으로 하는 정전기 방전 보호 소자.

청구항 2

제 1 항에 있어서,

상기 각 래더는 드레인 경로의 저항이 동일한 것을 특징으로 하는 정전기 방전 보호 소자.

청구항 3

제 1 항에 있어서,

상기 메탈 레이어는 싱글 레이어나 멀티 레이어 구조로 형성하는 것을 특징으로 하는 정전기 방전 보호 소자.

명세서

발명의 명칭

정전기 방전 보호 소자{Electro static discharge protection device}

도면의 간단한 설명

[0001] 도 1은 일반적인 정전기 방전 보호 소자의 회로 구성도.

[0002] 도 2는 일반적인 정전기 방전 보호 소자의 전류 특성 곡선.

[0003] 도 3은 종래 정전기 방전 보호 소자의 레이아웃.

[0004] 도 4는 도 3의 단위 래더의 전류 특성 곡선.

[0005] 도 5는 도 3의 래더간 저항차에 의한 전류 특성 곡선.

[0006] 도 6은 본 발명의 실시 예에 따른 정전기 방전 보호 소자의 레이아웃.

[0007] <도면의 주요 부분에 대한 부호의 설명>

[0008] 30, 60: 패드 31 내지 38 및 61 내지 68: 단위 래더

[0009] 39, 69a, 69b, 69c: 메탈 레이어

발명의 상세한 설명

[0010] 본 발명은 정전기 방전 보호 소자(Electro Static Discharge protection device)에 관한 것으로, 특히 패드(PAD)에 연결되어 있는 각 래더(ladder) 간 드레인 경로(drain path)의 저항을 서로 동일하게 하므로써, 정전기 방전 보호 소자의 동작시 각 단위 래더들이 전체적으로 전하를 균일하게 방전하여 고성능(high performance)의 정전기 방전(ESD) 특성을 갖게하는 정전기 방전 보호 소자에 관한 것이다.

[0011] 일반적으로, 정전기 방전 보호 소자의 구조는, 도 1에 도시된 바와 같이, 단위 래더(unit ladder)들의 병렬 연결로 구성되어 있다. 정전기 방전 회로 소자의 전류 특성 곡선을 도시한 도 2에서 알수 있듯이, 정전기 방전 보호 소자의 동작은 어느 한 래더로 부터 트리거(trigger)되어 여러 단계에 걸쳐 래더들이 트리거되어 동작하게 된다.

[0012] 도 3은 종래 정전기 방전 보호 소자의 래이아웃도로서, 제 1, 2, 3, 4, ..., N-3, N-2, N-1 및 N 래더(31, 32, 33, 34, 35, 36, 37 및 38)가 배열되어 있고, 각각의 단위 래더(31, 32, 33, 34, 35, 36, 37 및 38)는 메탈 레이어(metal layer; 39)와 개별적으로 연결되므로 모든 래더는 패드(30)와는 병렬로 연결되어 있어, 각 래더(31, 32, 33, 34, 35, 36, 37 및 38) 간 드레인 경로의 저항(a, b, c 및 d)이 서로 동일하지 않게 설계되어 있다. 즉, 제 1 래더(31)와 제 4 래더(34)간의 저항 차이는 "a" + "b" + "c" 만큼 발생하게 된다. 이 저항은 도 2의 정전기 방전 보호 소자의 전류 특성 곡선에서 구간 "p" 에서의 특성을 좌우하여 2차 항복전압(BV) 레벨(level)에 영향을 준다.

[0013] 이와 같이, 종래 구조에서는 정전기 방전 보호 소자 동작시 비대칭(asymmetry)적인 저항에 의해 단위 래더들간의 2차 항복 전압(Bvanap)이 변

화(variation)가 크게되면, 그 중 2차 항복 전압이 낮은 래더의 2차 항복 전압을 1차 항복 전압(Trigger Voltage)보다 크게 설계해야 하는데 - 이와 같이 설계해야 하는 것은 1차 항복 전압보다 2차 항복 전압이 낮은 래더가 존재하게 되면 다른 래더를 트리거 시키기 전에 그 래더가 감당할 수 없는 전류가 흐르게 되어 그 래더가 파괴되기 때문이며 - 이렇게 되면 전체 래더가 방전할 수 있는 전하(charge)량이 줄어 정전기 방전 보호 소자의 특성이 저하되게 된다. 이러한 원리는 단위 래더의 전류 특성 곡선을 도시한 도 4 및 래더간 저항차에 의한 전류 특성 곡선을 도시한 도 5에 나타나 있다.

[0014] 따라서, 본 발명은 패드에 연결되어 있는 각 래더간 드레인 경로의 저항을 서로 동일하게 하므로써, 정전기 방전 보호 소자의 동작시 각 단위 래더들이 전체적으로 전하를 균일하게 방전하여 고성능의 정전기 방전 특성을 갖게하는 정전기 방전 보호 소자를 제공함에 그 목적이 있다.

[0015] 이러한 목적을 달성하기 위한 본 발명의 실시 예에 따른 정전기 방전 보호 소자는 다수의 래더가 배열되고, 상기 래더 중 이웃하는 2개의 래드를 한 쌍으로 하여 제 1 메탈 레이어에 의해 연결하고, 상기 제 1 메탈 레이어를 제 2 메탈 레이어로 연결하고, 상기 제 2 메탈 레이어를 패더에 연결된 제 3 메탈 레이어에 연결되도록 구성하는 것을 특징으로 한다.

[0016] 상기에서, 각 래더는 드레인 경로의 저항이 동일하며, 메탈 레이어는 싱글 레이어나 멀티 레이어 구조로 형성한다.

[0017] 이하, 본 발명을 첨부된 도면을 참조하여 상세히 설명하기로 한다.

[0018] 도 6은 본 발명의 실시 예에 따른 정전기 방전 보호 소자의 래이아웃도로서, 제 1, 2, 3, 4, ..., N-3, N-2, N-1 및 N 래더(61, 62, 63, 64, 65, 66, 67 및 68)가 배열되어 있고, 이웃하는 한 쌍의 래더간 예를 들어, 제 1 래더(61)와 제 2 래더(62), 제 3 래더(63) 와 제 4 래더(64), 제 N-3 래더(65)와 제 N-2 래더(66), 제 N-1 래더(67)와 제 N 래더(68) 간을 제 1 메탈 레이어(69a)로 연결하고, 제 1 메탈 레이어(69a)는 제 2 메탈 레이어(69b)에 연결하고, 제 2 메탈 레이어(69b)는 패더(60)에 연결된 제 3 메탈 레이어(69c)에 연결되도록 구성한다.

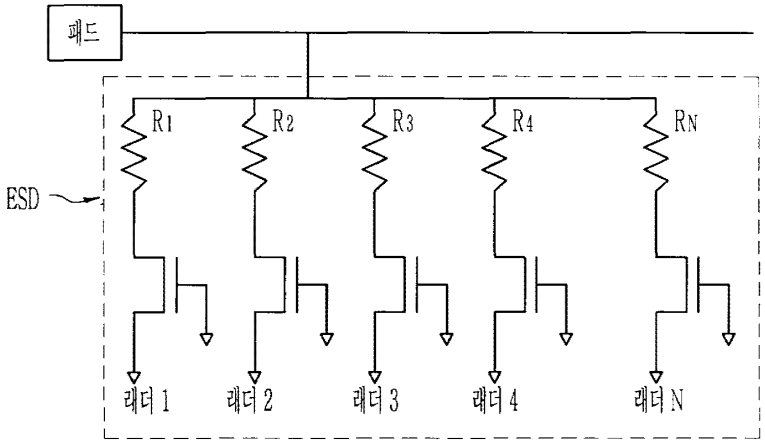
[0019] 본 발명의 정전기 방전 보호 소자는 각 래더간 드레인 경로의 저항을 메탈 레이어를 이용하여 대칭(symmetry)되게 구성하므로, 각각의 단위 래더에 걸리는 저항은 제 1 메탈 레이어(69a)의 저항 "c"와 제 2 메탈 레이어(69b)의 저항 "b"와 제 3 메탈 레이어(69c)의 저항 "a"의 합이된다. 즉, 각각의 단위 래더간 드레인 경로의 저항은 저항 "a" + "b" + "c"로 서로 동일하게 된다.

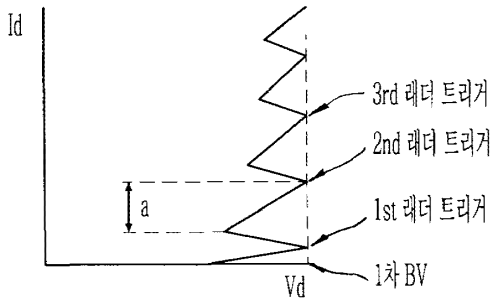
[0020] 각 래더간 드레인 경로의 메탈 레이어는 싱글 레이어(single layer) 구조로 형성하거나 멀티 레이어(multi layer) 구조로 형성할 수 있다.

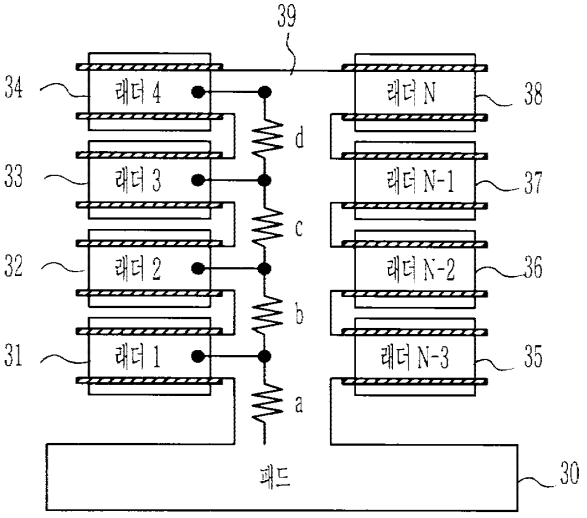
[0021] 본 발명의 구조에서는 정전기 방전 보호 소자 동작시 대칭(symmetry)적인 저항에 의해 단위 래더들간의 2차 항복 전압이 변화가 작게되므로, 기존 처럼 2차 항복 전압이 낮은 래더의 2차 항복 전압을 1차 항복 전압(Trigger Voltage)보다 크게 설계할 필요가 없을 뿐만 아니라, 항복 전압의 차이에 의한 특정 래더의 파괴가 없어 전체 래더가 방전할 수 있는 전하량이 줄어들지 않아 정전기 방전 보호 소자의 특성이 저하되지 않는다.

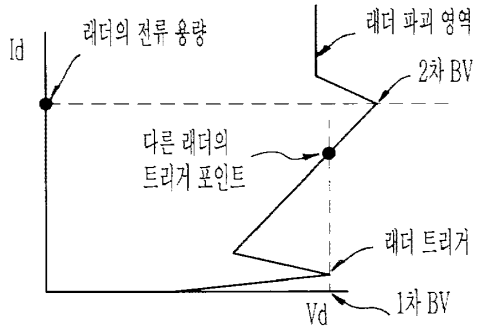
[0022] 상술한 바와 같이, 본 발명은 패드에 연결되어 있는 각 래더간 드레인 경로의 저항을 서로 동일하게 하므로써, 정전기 방전 보호 소자의 동작시 각 단위 래더들이 전체적으로 전하를 균일하게 방전하여 고성능의 정전기 방전 특성을 갖게하고, 종래 기술에 비해 적은 면적을 가지고 정전기 방전 보호 소자를 설계할 수 있어 인풋 캡이 작아야 하는 램버스 디램(Input Cap: Rambus DRAM = 2.0pF ~ 2.4pF, Sync. DRAM ≒ 5pF) 정전기 방전 보호 소자에 적합하다.

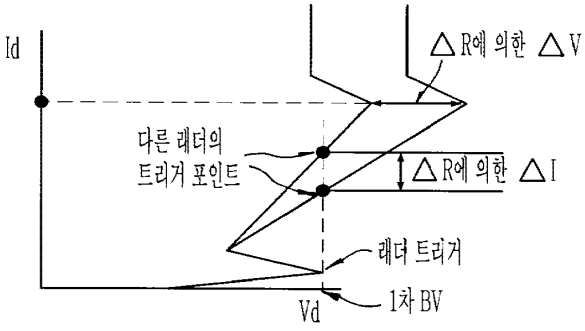
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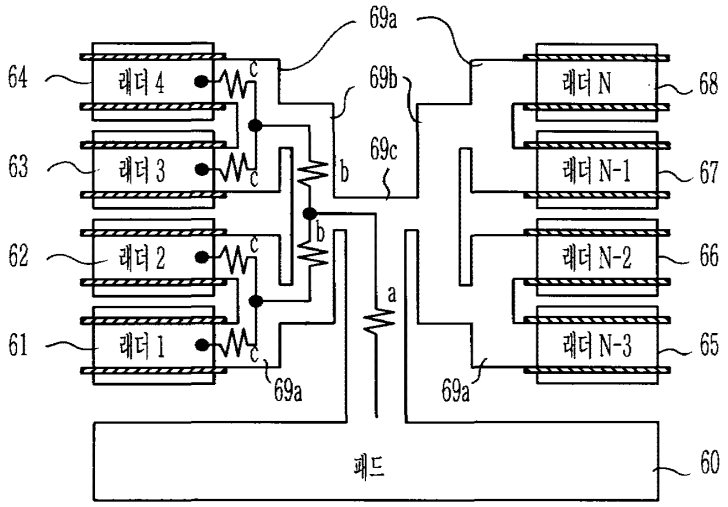

패드
R1
R2
R3
R4
RN
ESD
래더 1
래더 2
래더 3
래더 4
래더 N


Id
3rd 래더 트리거
2nd 래더 트리거
a
1st 래더 트리거
1차 BV
Vd


39
34
래더 4
래더 N
38
d
33
래더 3
래더 N-1
37
c
32
래더 2
래더 N-2
36
b
31
래더 1
래더 N-3
35
a
패드
30


래더의 전류 용량
Id
래더 파괴 영역
2차 BV
다른 래더의
트리거 포인트
래더 트리거
1차 BV
Vd


Id
△R에 의한 △V
다른 래더의
트리거 포인트
△R에 의한 △I
래더 트리거
1차 BV
Vd


69a
64
래더 4
c
69b
래더 N
68
63
래더 3
c
b
69c
래더 N-1
67
62
래더 2
c
b
래더 N-2
66
a
61
래더 1
c
래더 N-3
65
69a
69a
패드
60

Electronic Acknowledgement Receipt

EFS ID:	36853977
Application Number:	16207183
International Application Number:	
Confirmation Number:	2734
Title of Invention:	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method
First Named Inventor/Applicant Name:	Zhiguo Li
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Anna Lu
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	YMTP0079USA3
Receipt Date:	14-AUG-2019
Filing Date:	02-DEC-2018
Time Stamp:	01:44:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	3553256.PDF	26252 bdfbb1d01ba5a69d723a88dace725987b04b05d2	no	3

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Warnings:					
Information:					
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/207,183	12/02/2018	Zhiguo Li	YMTP0079USA3	2734

27765 7590 04/02/2020

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

EXAMINER
CLARK, SHEILA V

ART UNIT	PAPER NUMBER
2891	

NOTIFICATION DATE	DELIVERY MODE
04/02/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

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Office Action Summary	Application No. 16/207,183	Applicant(s) Li, Zhiguo	
	Examiner S. V CLARK	Art Unit 2891	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-17 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-17 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

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Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5, 8, 13, 15. 16 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

In claims 5, 8 and 15 are unclear what is meant by a “saved area”.

In claims 13 and 15, “the plurality of ESD buses” is not recited in claim 10 nor 14.

In claim 16, “no common ESD bus” is recited in claim 14.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-6 are rejected under 35 U.S.C. 103 as being unpatentable over Tamura in view of Wu.

Tamura teaches in for example figure 4 an integrated circuit structure, comprising: a circuit area a (core logic circuitry area), a plurality of ESD buses (see obvious statement below), a plurality of pad groups 208, adjacent and connected to the plurality of ESD buses; a common ESD bus 220, adjacent to the plurality of pad groups; and a plurality of bonding wires (not labelled but shown connected to 210) configured to connect the plurality of pad groups to the common ESD bus.

Though figure 4 does not show the integrated structure having a plurality of EDS buses, figure 1A and Wu teaches an integrated structure of the prior art formed with a plurality of buses. It would have been therefore obvious to one having ordinary skill in this art that the integrated structure of Tamura may be modified to include a plurality (at least two) buses if desired in view of the teachings of figure 1A and Wu.

2. The integrated circuit structure of claim 1, wherein each of the plurality of pad groups comprises at least one pad, and the plurality of bonding wires is configured to connect the at least one pad to the common ESD bus. (see figure 4)

3. The integrated circuit structure of claim 1, wherein common ESD bus comprises a plurality discontinuous ESD bus groups. (see obvious plurality discontinuous bus 304 and 306 in Wu figure 3)

4. The integrated circuit structure of claim 1, wherein the common ESD bus is formed outside the plurality of chip edges or inside the plurality of chip edges. (see figure 4)

5. The integrated circuit structure of claim 1, wherein the circuit area comprises at least one saved area (Vss or I/O area) adjacent to the ESD buses, the plurality of pad groups. (see figure 4)

6. The integrated circuit structure of claim 1, wherein the common ESD bus is parallel to the plurality of ESD buses. (see figure 4 and obvious statement above)

Claims 7-9 are rejected under 35 U.S.C. 103 as being unpatentable over Tamura in view Wu.

Tamura teaches in for example figure 4 (and figure 1A) an integrated circuit structure, comprising: a circuit area (core logic circuitry area); an ESD bus (see obvious statement below for the teaching of 220 a plurality of ESD buses in figure 1A); a plurality of pad groups 208 adjacent and connected to the plurality of ESD buses; and a plurality of bonding wires (not labelled but shown connected to 210) configured to connect one to another of the plurality of pad groups.

Though figure 4 does not show the integrated structure having a plurality of EDS buses, figure 1A and Wu teaches an integrated structure of the prior art formed with a plurality of buses. It would have been therefore obvious to one having ordinary skill in this art that the integrated structure of Tamura may be modified to include a plurality (at least two) buses if desired in view of the teachings of figure 1A and Wu.

8. The integrated circuit structure of claim 7, wherein the circuit area comprises at least one saved area (Vss or I/O area) adjacent to the plurality of ESD buses and the plurality of pad groups. (see figure 4)

9. The integrated circuit structure of claim 7, wherein each of the plurality of pad groups comprises a connecting pad, and the plurality of bonding wires are configured to connect the connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups. (see figure 4 and Wi figure 2)

Claims 10-12 are rejected under 35 U.S.C. 103 as being unpatentable over Tamura.

Tamura teaches in for example figure 4 (and figure 1A) a method of integrated circuit structure, comprising: forming a circuit area (core logic circuitry area) 208; forming a plurality of pad groups 208 corresponding to a plurality of discontinuous boundaries of the circuit area (pads shown on lateral sides are on discontinuous boundaries); forming a common ESD bus 220 is shown adjacent to the plurality of pad groups; and connecting a plurality of pads 208 corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires (not labelled but shown connected to 210).

It would have been obvious to one having ordinary skill in this art that the invention of Tamura would obviously possess the steps of forming and connecting.

11. The method of integrated circuit structure of claim 10, wherein each of the plurality of pad groups comprises at least one pad, and the plurality of bonding wires is configured to connect the at least one pad to the common ESD bus. (see figure 4)

12. The method of integrated circuit structure of claim 10, further comprising: forming the common ESD bus outside the plurality of chip edges or inside the plurality of chip edges. (see figure 4)

Claim 13 is rejected under 35 U.S.C. 103 as being unpatentable over Tamura in view of Wu.

13. The method of integrated circuit structure of claim 10, wherein the common ESD bus is parallel to the plurality of ESD buses.

Though figure 4 does not show the integrated structure having a plurality of EDS buses, figure 1A and Wu (figure 2) teach an integrated structure of the prior art formed with a plurality of buses. It would have been therefore obvious to one having ordinary skill in this art that the integrated structure of Tamura may be modified to include a plurality (at least two) buses if desired in view of the teachings of figure 1A and Wu

Claims 14-17 are rejected under 35 U.S.C. 103 as being unpatentable over Wu.

Wu teaches in for example figures 2 and 3 a method of integrated circuit structure, comprising: forming a circuit area on the active surface of chip 202 including power circuits 204-208 forming a plurality of pad groups (left side 232, 243 and right side 244, 245-though other groups are shown) corresponding to a plurality of

discontinuous boundaries (left and right) of the circuit area; and electrically connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires across the circuit area (see pads electrically connected by wires through power net 204).

It would have been obvious to one having ordinary skill in this art that the invention of Wu would obviously possess the steps of forming and connecting.

15. The method of integrated circuit structure of claim 14, wherein the circuit area comprises at least one saved area (power nets 202-206) adjacent to the plurality of ESD buses and the plurality of pad groups.

Figure 2 of Wu shows power buses 116 and 114 and col. 2, line 40 teach that invention is applicable to improving problems with signal cross coupling which would obviously include electrostatic discharge (ESD) issues, therefore one having ordinary skill in this are would deem this to suggest that said power buses may obviously be ESD buses)

16. The method of integrated circuit structure of claim 14, wherein the common ESD bus is parallel to the plurality of ESD buses and the plurality of pad groups. (see figure 2 and obvious statement in 15)

17. The method of integrated circuit structure of claim 14, wherein each of the plurality of pad groups comprises a connecting pad, and the plurality of bonding wires are

configured to electrically connect the connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups. (see figure 2)

Claims 1-17 are rejected

Any inquiry concerning this communication or earlier communications from the examiner should be directed to S. V. CLARK whose telephone number is (571)272-1725.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Matthew Landau. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. V. CLARK/
Primary Examiner, Art Unit 2891
March 28, 2020

Notice of References Cited	Application/Control No. 16/207,183	Applicant(s)/Patent Under Reexamination Li, Zhiguo	
	Examiner S. V CLARK	Art Unit 2891	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-6078068-A	06-2000	Tamura; Ronald Kazuo	H01L23/62	257/203
*	B	US-7129574-B2	10-2006	Wu; Ping	H01L23/50	257/691
*	C	US-5365091-A	11-1994	Yamagishi; Mikio	H01L27/11898	257/203
*	D	US-5347150-A	09-1994	Sakai; Izumi	H01L27/0218	257/203
*	E	US-7692247-B2	04-2010	Woo; Agnes N.	H01F17/0006	257/355
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Micron v. YMTC
IPR2025-00118

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/207,183	Li, Zhiguo
	Examiner	Art Unit
	S. V CLARK	2891

CPC - Searched*		
Symbol	Date	Examiner
H01L 23/50, H01L 23/60, H01L 2924/14, H01L 24/06, H01L 27/0292, H01L 23/62	02/24/2020	SVC

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
257	691, 784	02/24/2020	SVC
438	106	02/24/2020	SVC

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST	02/24/2020	SVC

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

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Micron v. YMTC
IPR2025-00118

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	50	257/$.ccls. and (ESD adj bus)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/02/24 06:34
L3	15	("4559579" | "4893168" | "4945395" | "5019889" | "5063429" | "5087955" | "5347150" | "5365091" | "5581202" | "5593927" | "5602406" | "5672895" | "5773854" | "5940258" | "5955764").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/02/24 06:52
L4	31	257/$.ccls. and (ESD adj2 bus) and wire	US-PGPUB; USPAT; USOCR	OR	OFF	2020/02/24 07:00
L5	28	257/$.ccls. and (ESD adj2 bus) and (bond$3 adj wire) and pads	US-PGPUB; USPAT; USOCR	OR	OFF	2020/02/24 07:03
L6	2	438/$.ccls. and (ESD adj2 bus) and (bond$3 adj wire) and pads	US-PGPUB; USPAT; USOCR	OR	OFF	2020/02/24 07:04
L7	64	(semiconductor or chip or die) and (ESD adj2 bus) and (bond$3 adj wire) and pads	US-PGPUB; USPAT; USOCR	OR	OFF	2020/02/24 07:18
L8	16	7 AND ((H01L23/50 OR H01L23/60 OR H01L2924/14 OR H01L24/06 OR H01L27/0292 OR H01L23/62).CPC.)	US-PGPUB; USPAT; USOCR	OR	OFF	2020/02/24 07:20

2/24/2020 7:24:56 AM
C:\Users\sclark\Documents\EAST\Workspaces\November 6, 2019.wsp

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Micron v. YMTC
IPR2025-00118

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16207183
	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	YMTP0079USA3

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20140061881	A1	2014-03-06	Yeh	

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1	201737459	TW	A	2017-10-16			Abstract

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.V.C/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	YMTP0079USA3

	1		
EXAMINER SIGNATURE			
Examiner Signature	/S. V. CLARK/	Date Considered	03/28/2020
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

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	First Named Inventor	Zhiguo Li
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	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	YMTP0079USA3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Roger Chen/	Date (YYYY-MM-DD)	2019-07-05
Name/Print	Roger Chen	Registration Number	67314

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	First Named Inventor	Zhiguo Li
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	YMTP0079USA3

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	1					

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1	101221629	CN	A	2008-07-16			Abstract
	2	102054523	CN	A	2011-05-11			Abstract
	3	103681654	CN	A	2014-03-26			Abstract

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	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	YMTP0079USA3

NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
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Examiner Signature	/S. V. CLARK/	Date Considered	03/28/2020

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	Attorney Docket Number	YMTP0079USA3

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☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

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Signature	/Roger Chen/	Date (YYYY-MM-DD)	2019-07-12
Name/Print	Roger Chen	Registration Number	67314

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	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	YMTP0079USA3

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	1					

U.S.PATENT APPLICATION PUBLICATIONS

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	1					

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1	101097304	CN	B	2011-07-13			Abstract
	2	103000625	CN	A	2013-03-27			Abstract
	3	20020034470	KR	A	2002-05-09			Abstract

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16207183
	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	YMTP0079USA3

NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1		

EXAMINER SIGNATURE			
Examiner Signature	/S. V. CLARK/	Date Considered	03/28/2020

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	Application Number	16207183
	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	YMTP0079USA3

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☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Roger Chen/	Date (YYYY-MM-DD)	2019-08-13
Name/Print	Roger Chen	Registration Number	67314

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.V.C/

Integrated Circuit Electrostatic Discharge Bus Structure and Related Method

Appl. No.	: 16/207,183	Confirmation No. 2734
First Named Inventor	: Zhiguo Li	
Filed	: December 2, 2018	
TC/A.U.	: 2891	
Examiner	: CLARK, SHEILA V	
Docket No.	: YMTP0079USA3	
Customer No.	: 27765	

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

In response to the Office action of April 02, 2020, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

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Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (original) An integrated circuit structure, comprising:
a circuit area;
a plurality of ESD buses;
a plurality of pad groups, adjacent and connected to the plurality of ESD buses;
a common ESD bus, adjacent to the plurality of pad groups; and
a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus.

2. (original) The integrated circuit structure of claim 1, wherein each of the plurality of pad groups comprises at least one pad, and the plurality of bonding wires is configured to connect the at least one pad to the common ESD bus.

3. (original) The integrated circuit structure of claim 1, wherein common ESD bus comprises a plurality discontinuous ESD bus groups.

4. (original) The integrated circuit structure of claim 1, wherein the common ESD bus is formed outside the plurality of chip edges or inside the plurality of chip edges.

5. (currently amended) The integrated circuit structure of claim 1, wherein the circuit area comprises at least one saved area between ~~adjacent to~~ the plurality of ESD buses[[,]] and between the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

6. (original) The integrated circuit structure of claim 1, wherein the common ESD bus is parallel to the plurality of ESD buses.

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7. (original) An integrated circuit structure, comprising:
a circuit area;
a plurality of ESD buses;
a plurality of pad groups, adjacent and connected to the plurality of ESD buses; and
a plurality of bonding wires configured to connect one to another of the plurality of pad groups.

8. (currently amended) The integrated circuit structure of claim 7, wherein the circuit area comprises at least one saved area between ~~adjacent to~~ the plurality of ESD buses[[,]] and between the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

9. (original) The integrated circuit structure of claim 7, wherein each of the plurality of pad groups comprises a connecting pad, and the plurality of bonding wires are configured to connect the connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups.

10. (currently amended) A method of integrated circuit structure, comprising:
forming a circuit area;
forming a plurality of ESD buses;
forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses;
forming a common ESD bus adjacent to the plurality of pad groups; and
connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires.

11. (original) The method of integrated circuit structure of claim 10, wherein each of

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the plurality of pad groups comprises at least one pad, and the plurality of bonding wires is configured to connect the at least one pad to the common ESD bus.

12. (original) The method of integrated circuit structure of claim 10, further comprising:

forming the common ESD bus outside the plurality of chip edges or inside the plurality of chip edges.

13. (original) The method of integrated circuit structure of claim 10, wherein the common ESD bus is parallel to the plurality of ESD buses.

14. (currently amended) A method of integrated circuit structure, comprising:

forming a circuit area;

forming a plurality of ESD buses;

forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses; and

connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires across the circuit area.

15. (currently amended) The method of integrated circuit structure of claim 14, wherein the circuit area comprises at least one saved area between ~~adjacent to~~ the plurality of ESD buses[[,]] and between the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

16. (currently amended) The method of integrated circuit structure of claim 14, wherein a ~~the~~ common ESD bus is parallel to the plurality of ESD buses and the plurality of pad groups.

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17. (original) The method of integrated circuit structure of claim 14, wherein each of the plurality of pad groups comprises a connecting pad, and the plurality of bonding wires are configured to connect the connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups

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Micron v. YMTC
IPR2025-00118

Electronic Acknowledgement Receipt

EFS ID:	39308033
Application Number:	16207183
International Application Number:	
Confirmation Number:	2734
Title of Invention:	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method
First Named Inventor/Applicant Name:	Zhiguo Li
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Edie Hung
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	YMTP0079USA3
Receipt Date:	04-MAY-2020
Filing Date:	02-DEC-2018
Time Stamp:	02:14:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	3814306.PDF	1584284 b847e0e38a291bb74b337f74004687b5bf7cb92b	no	9

Warnings:

Information:					
2	Amendment/Req. Reconsideration-After Non-Final Reject	3814305.PDF	99320 4b108c40b6c364d9928276ab87f10ee3fc60ff84	no	1
Warnings:					
Information:					
3	Claims	3814304.PDF	108494 ee23ad5b4dd44d2206da1ab4055b90341f91659a	no	4
Warnings:					
Information:					
		Total Files Size (in bytes):	1792098		

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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file.

Claim Amendments

Claims 5, 8 and 15 have been amended to clarify that the circuit area comprises at least one saved area between the plurality of ESD buses and between the plurality of pad groups, and there is **no ESD bus and no pad** in the at least one saved area, which is at least supported by Para [0024] and FIG. 2. No new matter is entered.

Claims 10, 14 have been amended to clarify that the instant application forming a plurality of ESD buses and the plurality of pad groups are adjacent and connected to the plurality of ESD buses, which is at least supported by Para [0021]. No new matter is entered.

Claim 16 has been amended to clarify that a common ESD bus is parallel to the plurality of ESD buses and the plurality of pad groups. No new matter is entered.

Claim Rejections under 35 U.S.C 112

Claims 5, 8, 13, 15, 16 are rejected under 35 U.S.C 112 (b), as being indefinite or failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Response:

Claims 5, 8 and 15 have been amended to clarify that the circuit area comprises **at least one saved area between** the plurality of ESD buses and **between** the plurality of pad groups, and there is **no ESD bus and no pad in the at least one saved area**. Therefore, those skilled in the art know what is meant by "saved area".

Claims 10, 14 have been amended to recite a plurality of ESD buses.

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Claim 16 has been amended to recite **a** common ESD bus.

As shown in the above, claims 5, 8, 10, 14-16 have been amended to particularly point out and distinctly claim the subject matter which applicant regards as the invention, to overcome claim rejections under 35 U.S.C 112 (b).

Claims in view of 35 U.S.C. 102 & 103

Claims 1-6, 7-9, 13 are rejected under 35 U.S.C 103(a) as being unpatentable over Tamura (US 6,078,068) in view of Wu (US 7,129,574);

Claims 10-12 are rejected under 35 U.S.C 103(a) as being unpatentable over Tamura (US 6,078,068); and

Claims 14-17 are rejected under 35 U.S.C 103(a) as being unpatentable over Wu (US 7,129,574).

Response:

The Examiner considers that *"though figure 4 of Tamura does not show a plurality of EDS buses, figure 1A of Tamura and Wu teaches a plurality of EDS buses. It would have been therefore obvious to one having ordinary skill in this art that the integrated* ***structure of Tamura may be modified to include a plurality (at least two) buses*** *if desired in view of the teachings of figure 1A and Wu."*

However, Tamura teaches *"****In order to meet the need for semiconductor devices that have high levels of ESD protection, the use of an ESD bus 120*** *has recently gained popularity. For example, when the conduction lead connection 114 provides a ground source (Vss) to a bond pad 108,* ***the bond pad 108 is also connected to the ESD bus 120 through a ground isolation and conduction circuit 110.*** *As will be described with reference to FIG. 1B below, the ESD bus 120 is needed in order to dissipate electrostatic charge when Vss bus cuts are implemented in order to separate different types of internal Vss buses.*

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Typically, ***a die edge seal 122 is also patterned along the periphery of a chip edge 104 of the semiconductor die.*** *Normally, the die edge seal 122 is a metallization pattern that is formed at each metallization layer of an integrated circuit device. Accordingly, the die edge seal 122 will form a stacked plurality of metallization rings, one stacked over another, near the chip edge 104. The lowermost metallization ring of the die edge seal 122 is typically connected to the chip substrate via a suitable substrate connection. Therefore,* ***the die edge seal 122 serves as a mechanical and electrical barrier to contaminants that may disrupt the operation of the semiconductor die 100.*** *(col. 1 line 55- col. 2 line 9)"*

"Although shown as ***only one metallization line here for simplicity, the ESD bus die edge seal 220 is actually repeated at each metallization layer in an integrated circuit device to provide a sufficient amount of mechanical support as well as a good electrical barrier to contaminants.*** *One advantage of combining the ESD bus and the die edge seal of the prior art into a single ESD bus die edge seal 220 is that* ***chip surface area can be saved and an integrated circuit device can be fabricated on a smaller physical chip****. (col 5. Lines 1-9)"*

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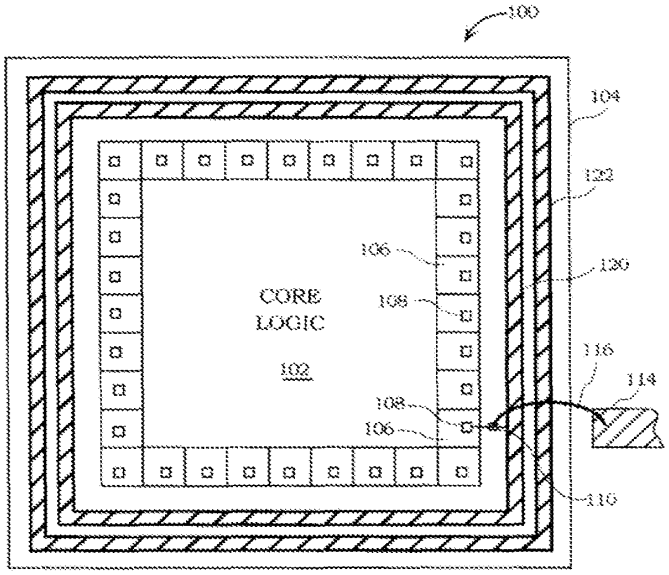


FIG. 1A
(Prior art)

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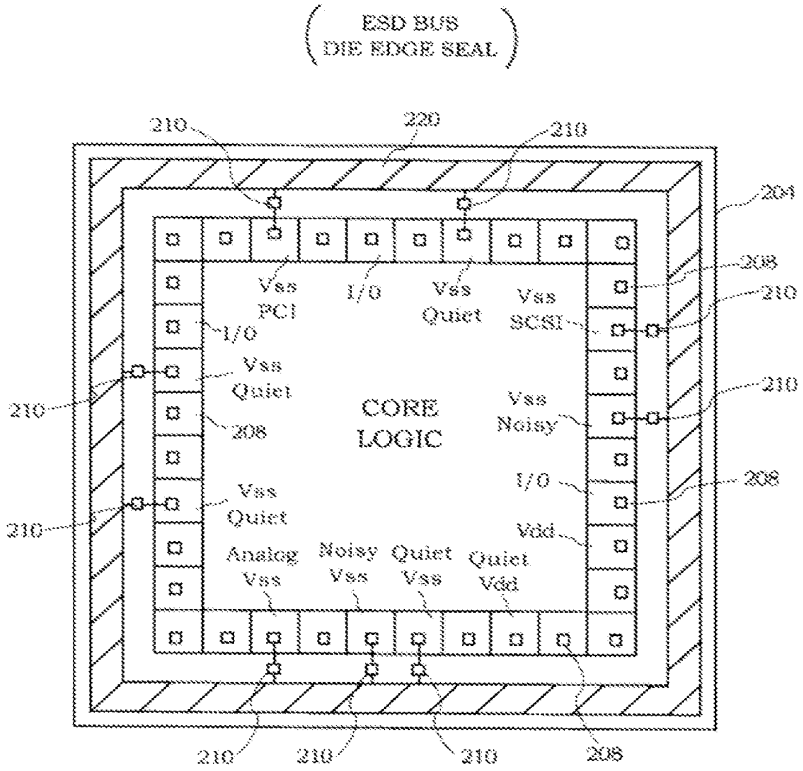


FIG. 4

In other words, Tamura in FIG. 1 teaches that the ESD bus 120 is utilized for ESD protection and the die edge seal 122 is utilized for mechanical and electrical barrier to prevent contaminants from disrupting operations of the semiconductor die, wherein the die edge seal 122 is **NOT utilized for ESD protection, and are not adjacent and connected to the bond pads 108.**

Besides, Tamura in FIG. 4 teaches that the ESD bus 120 and the die edge seal 122 **are combined as a single ESD bus die edge seal 220 with both functions to save area.**

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On the other hand, Wu teaches *"First power-ring 114 and second power-ring 116 are dedicated to* ***provide a respective maximum number of potential receiving bonding sites for two independent chip power supply nets*** *(not shown) disposed on a multi-power IC chip having dual independent power supply nets to be mounted in the multi-power package 100. (col. 7, lines 33-38)"*

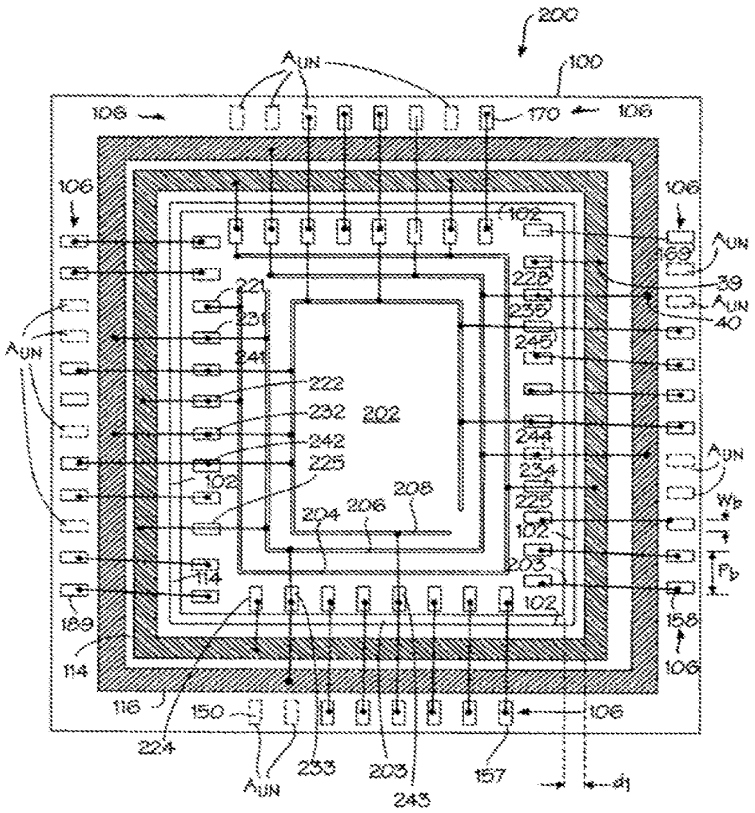


Fig. 2

In other words, together with FIG. 2, Wu teaches that the power-ring 114 and the power-ring 116 provide a respective maximum number of potential receiving bonding sites for two independent chip power supply nets, i.e. **the power-ring 114 and the power-ring 116 are not utilized for ESD and the power-ring 116 is not adjacent to pads 232, 243-245 in Wu's teaching**.

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In comparison, claim 1 and amended 14 recite:

"a plurality of pad groups, **adjacent and connected to the plurality of ESD buses**; (claim 1)"

"forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein **the plurality of pad groups are adjacent and connected to the plurality of ESD buses**; and (amended claim 14)"

In other words, in the instant application, the pad groups are **adjacent and connected to the plurality of ESD buses**, which is different from Tamura's teaching that the die edge seal 122 is **NOT utilized for ESD protection, and are not adjacent and connected to the bond pads 108 (ONLY the inner die edge seal 122 is adjacent to the bond pads 108)**, and also different from **Wu's teaching that the power-ring 114 and the power-ring 116 are not utilized for ESD and the power-ring 116 is not adjacent to pads 232, 243-245 (only the power-ring 114 is adjacent to the pads 232, 243-245).**

Besides, Tamura teaches that the ESD bus 120 and the die edge seal 122 **are combined as a single ESD bus die edge seal 220 in FIG. 4 with both functions to save area**. Under such a situation, without improper hindsight, those skilled in the art would have no motivation to "**modify structure FIG. 4 of Tamura to include a plurality buses** in view of the teachings of figure 1 A and Wu" as pointed out by the Examiner.

In addition, the instant application specifies:

" The integrated circuit structure of claim 1, wherein the circuit area comprises at least one saved area **between** the plurality of ESD buses **and between** the plurality of pad groups, and there is **no ESD bus and no pad in the at least one saved area**. (amended claim 5)"

"Each of the plurality of pad groups G1, G2 and G3 includes at least one pad 22, wherein the pad 22 is an input/output pad connected to a ground or a system low

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voltage. At least one of the plurality of bonding wires 25 is configured to connect the at least one pad 22 to the common ESD bus 24. In one embodiment, multiple bonding wires 25 may be configured to connect multiple pads 22 of the pad group G1 to the common ESD bus 24, which provides multiple connections to enhance conductivity between the pad group G1 and the common ESD bus 24 to improve ESD protection. (Para [0022])"

"For example, ***the ESD bus 11 and the filler cells F1 and F2 shown in FIG. 1 are replaced by saved areas SA1 and SA2 in FIG. 2.*** *The saved area SA1 is adjacent to the ESD buses E1 and E2 and the pads 22 of the pad groups G1 and G2. The saved area SA2 is adjacent to the ESD buses E2 and E3 and the pads 22 of the pad groups G2 and G3. In one embodiment, the common ESD bus 24 is formed inside the chip edges 23, and adjacent to the plurality of pad groups G1, G2 and G3 and the saved areas SA1 and SA2. (Para [0024])"*

In other words, in the instant application, at least one saved area is **between** the plurality of ESD buses **and between** the plurality of pad groups, and there is **no ESD bus and no pad in the at least one saved area**, which is different from Tamura's teaching that all bond pads 108/208 are adjacent (the Vss or I/O area analogized by the Examiner are known by those skilled in the art as bond pads 208 connected to Vss or I/O).

Since claim 1 and amended claim 14 have been recite the above limitations which are not taught by Tamura, Wu or their combination, claims 1, 14 should be patentable over Tamura, Wu.

Claims 7, 10 recite limitations similar to claim 1. Thus, claims 7, 10 should be allowable. Dependent claims of claims 1, 7, 10 and 14 should be allowable if their respective base claims are allowed. Reconsideration of claims 1-17 is therefore respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this

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case.

Sincerely yours,

/Roger Chen/ Date: 04/30/2020

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/207,183	12/02/2018	Zhiguo Li	YMTP0079USA3

CONFIRMATION NO. 2734

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

PUBLICATION NOTICE

OC000000116831737

Title: Integrated Circuit Electrostatic Discharge Bus Structure and Related Method

Publication No.US-2020-0144174-A1
Publication Date:05/07/2020

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/207,183	12/02/2018	Zhiguo Li	YMTP0079USA3	2734

27765 7590 08/05/2020

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
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EXAMINER
CLARK, SHEILA V

ART UNIT	PAPER NUMBER
2891	

NOTIFICATION DATE	DELIVERY MODE
08/05/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

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Office Action Summary	Application No. 16/207,183	Applicant(s) Li, Zhiguo	
	Examiner S. V CLARK	Art Unit 2891	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 5/4/2020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-17 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-4,6-7,9-14 and 16-17 is/are rejected.

8) ☑ Claim(s) 5,8 and 15 is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

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Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5, 8, 15 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

In claims 5, 8 and 15 continue to be unclear by what is meant by a “saved area”.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4, 6 are rejected under 35 U.S.C. 103 as being unpatentable over Tamura in view of Wu.

Tamura teaches in for example figure 4 an integrated circuit structure, comprising: a circuit area a (core logic circuitry area), a plurality of ESD buses (see obvious statement below), a plurality of pad groups 208, adjacent and connected to the

plurality of ESD buses; a common ESD bus 220, adjacent to the plurality of pad groups; and a plurality of bonding wires (not labelled but shown connected to 210) configured to connect the plurality of pad groups to the common ESD bus.

Though figure 4 does not show the integrated structure having a plurality of EDS buses, figure 1A and Wu teaches an integrated structure of the prior art formed with a plurality of buses. It would have been therefore obvious to one having ordinary skill in this art that the integrated structure of Tamura may be modified to include a plurality (at least two) buses if desired in view of the teachings of figure 1A and Wu.

2. The integrated circuit structure of claim 1, wherein each of the plurality of pad groups comprises at least one pad, and the plurality of bonding wires is configured to connect the at least one pad to the common ESD bus. (see figure 4)

3. The integrated circuit structure of claim 1, wherein common ESD bus comprises a plurality discontinuous ESD bus groups. (see obvious plurality discontinuous bus 304 and 306 in Wu figure 3)

4. The integrated circuit structure of claim 1, wherein the common ESD bus is formed outside the plurality of chip edges or inside the plurality of chip edges. (see figure 4)

6. The integrated circuit structure of claim 1, wherein the common ESD bus is parallel to the plurality of ESD buses. (see figure 4 and obvious statement above)

Claims 7, 9 are rejected under 35 U.S.C. 103 as being unpatentable over Tamura in view Wu.

Tamura teaches in for example figure 4 (and figure 1A) an integrated circuit structure, comprising: a circuit area (core logic circuitry area); an ESD bus (see obvious statement below for the teaching of 220 a plurality of ESD buses in figure 1A); a plurality of pad groups 208 adjacent and connected to the plurality of ESD buses; and a plurality of bonding wires (not labelled but shown connected to 210) configured to connect one to another of the plurality of pad groups.

Though figure 4 does not show the integrated structure having a plurality of EDS buses, figure 1A and Wu teaches an integrated structure of the prior art formed with a plurality of buses. It would have been therefore obvious to one having ordinary skill in this art that the integrated structure of Tamura may be modified to include a plurality (at least two) buses if desired in view of the teachings of figure 1A and Wu.

9. The integrated circuit structure of claim 7, wherein each of the plurality of pad groups comprises a connecting pad, and the plurality of bonding wires are configured to connect the connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups. (see figure 4 and Wi figure 2)

Claims 10-12 are rejected under 35 U.S.C. 103 as being unpatentable over Tamura.

Tamura teaches in for example figure 4 (and figure 1A) a method of integrated circuit structure, comprising: forming a circuit area (core logic circuitry area) 208; forming a plurality of EDS buses (see obvious statement below), forming a plurality of pad groups 208 corresponding to a plurality of discontinuous boundaries of the circuit area (pads shown on lateral sides are on discontinuous boundaries); wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses: forming a common ESD bus 220 is shown adjacent to the plurality of pad groups; and connecting a plurality of pads 208 corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires (not labelled but shown connected to 210).

Though figure 4 does not show the integrated structure having a plurality of EDS buses, figure 1A and Wu teaches an integrated structure of the prior art formed with a plurality of buses. It would have been therefore obvious to one having ordinary skill in this art that the integrated structure of Tamura may be modified to include a plurality (at least two) buses if desired in view of the teachings of figure 1A and Wu.

It would have been obvious to one having ordinary skill in this art that the invention of Tamura would obviously possess the steps of forming and connecting.

11. The method of integrated circuit structure of claim 10, wherein each of the plurality of pad groups comprises at least one pad, and the plurality of bonding wires is configured to connect the at least one pad to the common ESD bus. (see figure 4)

12. The method of integrated circuit structure of claim 10, further comprising: forming the common ESD bus outside the plurality of chip edges or inside the plurality of chip edges. (see figure 4)

Claim 13 is rejected under 35 U.S.C. 103 as being unpatentable over Tamura in view of Wu.

13. The method of integrated circuit structure of claim 10, wherein the common ESD bus is parallel to the plurality of ESD buses.

Though figure 4 does not show the integrated structure having a plurality of EDS buses, figure 1A and Wu (figure 2) teach an integrated structure of the prior art formed with a plurality of buses. It would have been therefore obvious to one having ordinary skill in this art that the integrated structure of Tamura may be modified to include a plurality (at least two) buses if desired in view of the teachings of figure 1A and Wu

Claims 14, 16, 17 are rejected under 35 U.S.C. 103 as being unpatentable over Wu.

Wu teaches in for example figures 2 and 3 a method of integrated circuit structure, comprising: forming a circuit area; forming a plurality of EDS buses (see obvious statement below) on the active surface of chip 202 including power circuits 204-208 forming a plurality of pad groups (left side 232, 243 and right side 244, 245-though other groups are shown) corresponding to a plurality of discontinuous boundaries (left and right) of the circuit area; wherein the plurality of pad groups are shown adjacent and

connected to the plurality of ESD buses and electrically connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires across the circuit area (see pads electrically connected by wires through power net 204).

Though figures 2 and 3 do not show the integrated structure having a plurality of EDS buses, figure 1A and Wu teaches an integrated structure of the prior art formed with a plurality of buses. It would have been therefore obvious to one having ordinary skill in this art that the integrated structure of Tamura may be modified to include a plurality (at least two) buses if desired in view of the teachings of figure 1A and Wu.

It would have been obvious to one having ordinary skill in this art that the invention of Wu would obviously possess the steps of forming and connecting.

16. The method of integrated circuit structure of claim 14, wherein the common ESD bus is parallel to the plurality of ESD buses and the plurality of pad groups. (see figure 2 and obvious statement in 15)

17. The method of integrated circuit structure of claim 14, wherein each of the plurality of pad groups comprises a connecting pad, and the plurality of bonding wires are configured to electrically connect the connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups. (see figure 2)

Claims 1-4, 6, 7, 9-14, 16-17 are rejected.

Claims 5, 8, 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of

the base claim and any intervening claims once issues relative to 35 U.S.C. 112 are success fully resolved.

Applicant's arguments filed 5/4/2020 have been fully considered but they are not persuasive. The claimed features continue to possess primarily the same features recited in the original claims. The prior art rejections are deemed to continue to be applicable and have therefore been repeated.

Applicant argues details relative to the instant claims and expresses that they allegedly fail to teach the features of the prior art used in the rejection. Since the instant claims are recited broadly, the references provided are deemed to be applicable as detailed above. Applicant is encouraged to provide more distinguishing details to the instant claims so they can be further considered for allowance.

Page 5 of the specification paragraph (0024) provide specific discussion and feature representation of what is meant by a “saved area” and said area is presented to have a specific structural representation and therefore would appear to have a specific definition. Applicant states that one having ordinary skill in this art would know what is meant by “saved area” but said area expressed in paragraph (0024) is presented as being inventive and unique to applicant’s invention so therefore would not be a feature that is well known in this invention. A “saved area” can have many definitions and structural representations depending on the application, invention, and how said saved area is used. Each device or invention may have a unique definition of what is meant by a “saved area” and said “saved area” would have to be provided with additional

descriptive language to understand the meaning for a specific invention as is the case with the "saved area" recited in these claims. More descriptive details are necessary to determine what is meant by "saved area" for this invention. Once clarity is successfully realized the features in claims 5, 8 and 15 which have this features would be considered allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to S. V. CLARK whose telephone number is (571)272-1725.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an

interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Matthew Landau. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. V. CLARK/
Primary Examiner, Art Unit 2891
August 1, 2020

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/207,183	Li, Zhiguo
	Examiner	Art Unit
	S. V CLARK	2891

CPC - Searched*		
Symbol	Date	Examiner
H01L 23/50, H01L 23/60, H01L 2924/14, H01L 24/06, H01L 27/0292, H01L 23/62	02/24/2020	SVC
updated	08/01/2020	SVC

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
257	691, 784	02/24/2020	SVC
438	106	02/24/2020	SVC
updated		08/01/2020	SVC

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST	02/24/2020	SVC

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/207,183	Filing Date 12/02/2018	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)			
FOR	NUMBER FILED	NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	09/10/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 14	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 4	Minus	*** 4	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/JACKIE A WHITE/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/30EFS (09-08)
Approved for use through 10/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	16/207,183	Filing Date	2018-12-02	Docket Number (if applicable)	YMTP0079USA3	Art Unit	2891
First Named Inventor	Zhiguo Li			Examiner Name	CLARK, SHEILA V		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 503105

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (09-08)
Approved for use through 10/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Roger Chen/	Date (YYYY-MM-DD)	2020-09-10
Name	Roger Chen	Registration Number	67314

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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IPR2025-00118

Electronic Patent Application Fee Transmittal

Application Number:	16207183
Filing Date:	02-Dec-2018
Title of Invention:	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method
First Named Inventor/Applicant Name:	Zhiguo Li
Filer:	Roger Gwan-Jye Chen/Edie Hung
Attorney Docket Number:	YMTP0079USA3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
RCE- 1ST REQUEST	1801	1	1300	1300
		Total in USD ($)		**1300**

Electronic Acknowledgement Receipt

EFS ID:	40513782
Application Number:	16207183
International Application Number:	
Confirmation Number:	2734
Title of Invention:	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method
First Named Inventor/Applicant Name:	Zhiguo Li
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Edie Hung
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	YMTP0079USA3
Receipt Date:	10-SEP-2020
Filing Date:	02-DEC-2018
Time Stamp:	22:17:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1300
RAM confirmation Number	E202090M18258715
Deposit Account	503105
Authorized User	Edie Hung
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	3953729.PDF	669963 fddee4e422c91725f6d32fd7e50f460e6c9f4cbe	no	4
Warnings:					
Information:					
2	Amendment Submitted/Entered with Filing of CPA/RCE	3953728.PDF	96413 a0f0a80831b608f782c0d58c8aea435dc6de17eb	no	1
Warnings:					
Information:					
3	Claims	3953727.PDF	102334 f282dfccaa17ba3f64a8c1f842752945159d67ac	no	4
Warnings:					
Information:					
4	Request for Continued Examination (RCE)	3953629.pdf	323265 27059fd0063c4fd042d0a35c6c4878ae083762aa	no	3
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	30242 bdc6712fca4ec1280ad12c3ef542e45e46f0cd25	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1222217		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

Request for Continued Examination:

The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file.

Claim Amendments

Claims 1, 7, 14 have been amended to include all the limitations of claims 5, 8, 15, respectively, and claim 10 has been correspondingly amended, to clarify that the circuit area comprises at least one saved area, **each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups**, and there is no ESD bus and no pad in the at least one saved area, and claims 5, 8, 15 are correspondingly cancelled, which is at least supported by Para [0024] and FIG. 2. No new matter is entered.

Claim Rejections under 35 U.S.C 112

Claims 5, 8, 15 are rejected under 35 U.S.C. 112 (b), as being indefinite or failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Response:

Claims 1, 7, 14 have been amended to include all the limitations of claims 5, 8, 15, respectively, and claim 10 has been correspondingly amended, to clarify that the circuit area comprises at least one saved area, **each of at least one saved area is**

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adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area, which is at least supported by FIG. 2 and Para [0024] *"For example, the ESD bus 11 and the filler cells F1 and F2 shown in FIG. 1 are replaced by saved areas SA1 and SA2 in FIG. 2.* ***The saved area SA1 is adjacent to the ESD buses E1 and E2 and the pads 22 of the pad groups G1 and G2. The saved area SA2 is adjacent to the ESD buses E2 and E3 and the pads 22 of the pad groups G2 and G3.*** *In one embodiment, the common ESD bus 24 is formed inside the chip edges 23, and adjacent to the plurality of pad groups G1, G2 and G3 and the saved areas SA1 and SA2. (Para [0024]"*

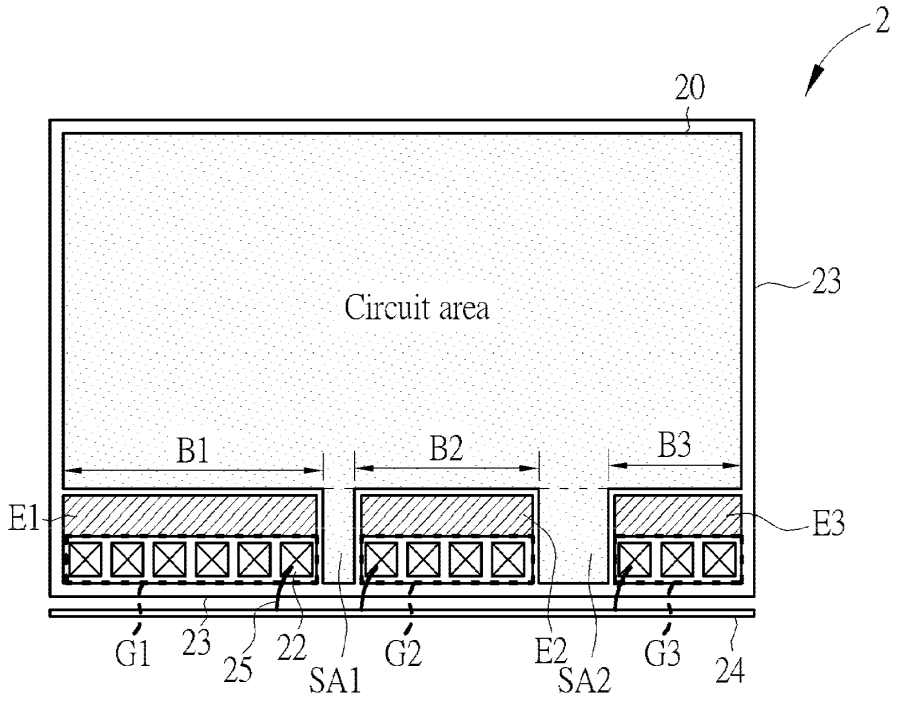


FIG. 2

Therefore, "saved area" has been specifically defined according to Para [0024] to particularly point out and distinctly claim the subject matter which applicant regards as

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the invention, to overcome claim rejections under 35 U.S.C. 112 (b).

Claims in view of 35 U.S.C. 103

Claims 1-4, 6, 7, 9, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura (US 6,078,068) in view of Wu (US 7,129,574);

Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura (US 6,078,068); and

Claims 14, 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (US 7,129,574).

Response:

As Examiner stated, claims 5, 8, 15 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims once issues relative to 35 U.S.C. 112 are success fully resolved..

As set forth in the above amendments and arguments, "saved area" has been specifically defined according to Para [0024] to overcome claim rejections under 35 U.S.C. 112 (b).

Claim 1 has been amended to include the limitations of claim 5 in response to allowable subject matter of the Office Action. This amendment recites the limitations of claim 5 and overcomes claim rejections under 35 U.S.C. 112 (b). Therefore, claim 1 should be allowable.

Claim 7 has been amended to include the limitations of claim 8 in response to allowable subject matter of the Office Action. This amendment recites the limitations of claim 8 and overcomes claim rejections under 35 U.S.C. 112 (b). Therefore, claim 7 should be allowable.

Claim 14 has been amended to include the limitations of claim 15 in response to

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allowable subject matter of the Office Action. This amendment recites the limitations of claim 15 and overcomes claim rejections under 35 U.S.C. 112 (b). Therefore, claim 15 should be allowable.

Claim 10 has been correspondingly amended to recite similar limitation of any of amended claims 1, 7, 14 in response to allowable subject matter of the Office Action. Therefore, claim 10 should be allowable.

Dependent claims of claims 1, 7, 10 and 14 should be allowable if their respective base claims are allowed. Reconsideration of claims 1-4, 6-7, 9-14, 16-17 is therefore respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/Roger Chen/ Date: 09/10/2020

Roger Chen, Patent Agent No. 67,314
5F., No.389, Fuhe Rd., Yonghe Dist., New Taipei City, Taiwan
Voice Mail: 302-729-1562
e-mail : RogerChen@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

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IPR2025-00118

Integrated Circuit Electrostatic Discharge Bus Structure and Related Method

Appl. No.	: 16/207,183	Confirmation No. : 2734
First Named Inventor	: Zhiguo Li	
Filed	: December 2, 2018	
TC/A.U.	: 2891	
Examiner	: CLARK, SHEILA V	
Docket No.	: YMTP0079USA3	
Customer No.	: 27765	

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT AND REQUEST FOR CONTINUED EXAMINATION

In response to the Office action of August 5, 2020, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

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Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended): An integrated circuit structure, comprising:
a circuit area;
a plurality of ESD buses;
a plurality of pad groups, adjacent and connected to the plurality of ESD buses;
a common ESD bus, adjacent to the plurality of pad groups; and
a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus;
wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

2. (original): The integrated circuit structure of claim 1, wherein each of the plurality of pad groups comprises at least one pad, and the plurality of bonding wires is configured to connect the at least one pad to the common ESD bus.

3. (original): The integrated circuit structure of claim 1, wherein common ESD bus comprises a plurality discontinuous ESD bus groups.

4. (original): The integrated circuit structure of claim 1, wherein the common ESD bus is formed outside the plurality of chip edges or inside the plurality of chip edges.

5. (canceled)

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6. (original): The integrated circuit structure of claim 1, wherein the common ESD bus is parallel to the plurality of ESD buses.

7. (currently amended): An integrated circuit structure, comprising:
a circuit area;
a plurality of ESD buses;
a plurality of pad groups, adjacent and connected to the plurality of ESD buses; and
a plurality of bonding wires configured to connect one to another of the plurality of pad groups;
wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

8. (canceled)

9. (original): The integrated circuit structure of claim 7, wherein each of the plurality of pad groups comprises a connecting pad, and the plurality of bonding wires are configured to connect the connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups.

10. (currently amended): A method of integrated circuit structure, comprising:
forming a circuit area;
forming a plurality of ESD buses;
forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses;

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forming a common ESD bus adjacent to the plurality of pad groups; and

connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires;

wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

11. (original): The method of integrated circuit structure of claim 10, wherein each of the plurality of pad groups comprises at least one pad, and the plurality of bonding wires is configured to connect the at least one pad to the common ESD bus.

12. (original): The method of integrated circuit structure of claim 10, further comprising:

forming the common ESD bus outside the plurality of chip edges or inside the plurality of chip edges.

13. (original): The method of integrated circuit structure of claim 10, wherein the common ESD bus is parallel to the plurality of ESD buses.

14. (currently amended): A method of integrated circuit structure, comprising:

forming a circuit area;

forming a plurality of ESD buses;

forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses; and

connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires across the circuit area;

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wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

15. (canceled)

16. (previously presented): The method of integrated circuit structure of claim 14, wherein a common ESD bus is parallel to the plurality of ESD buses and the plurality of pad groups.

17. (original): The method of integrated circuit structure of claim 14, wherein each of the plurality of pad groups comprises a connecting pad, and the plurality of bonding wires are configured to connect the connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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NOTICE OF ALLOWANCE AND FEE(S) DUE

27765 7590 09/22/2020

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

EXAMINER
CLARK, SHEILA V

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 09/22/2020

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/207,183	12/02/2018	Zhiguo Li	YMTP0079USA3	2734

TITLE OF INVENTION: Integrated Circuit Electrostatic Discharge Bus Structure and Related Method

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	12/22/2020

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27765 7590 09/22/2020

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/207,183	12/02/2018	Zhiguo Li	YMTP0079USA3	2734

TITLE OF INVENTION: Integrated Circuit Electrostatic Discharge Bus Structure and Related Method

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	12/22/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
CLARK, SHEILA V	2891	257-691000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/207,183	12/02/2018	Zhiguo Li	YMTP0079USA3	2734

27765 7590 09/22/2020

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

EXAMINER	
CLARK, SHEILA V	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 09/22/2020

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	**Application No.** 16/207,183	**Applicant(s)** Li, Zhiguo	
	Examiner S. V CLARK	**Art Unit** 2891	**AIA (FITF) Status** Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 9/10/2020.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-4,6-7,9-14 and 16-17 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/S. V. CLARK/
Primary Examiner, Art Unit 2891

Micron Ex. 1002, p. 243
Micron v. YMTC
IPR2025-00118

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/207,183	Li, Zhiguo
	Examiner	**Art Unit**
	S. V CLARK	2891

CPC						
Symbol					**Type**	**Version**
H01L	/	23	/	50	F	2013-01-01
H01L	/	23	/	49	I	2013-01-01
H01L	/	27	/	0248	I	2013-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	14	
/S. V. CLARK/ Primary Examiner, Art Unit 2891	16 September 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office — Part of Paper No.: 20200916

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Micron v. YMTC
IPR2025-00118

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/207,183	Li, Zhiguo
	Examiner	**Art Unit**
	S. V CLARK	2891

INTERNATIONAL CLASSIFICATION					
CLAIMED					
H01L	/	23	/	52	

NON-CLAIMED					
	/		/		

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
257	691

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					
257	784					
438	106					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	14	
/S. V. CLARK/ Primary Examiner, Art Unit 2891	16 September 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office — Part of Paper No.: 20200916

Micron Ex. 1002, p. 245
Micron v. YMTC
IPR2025-00118

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/207,183	Li, Zhiguo
	Examiner	**Art Unit**
	S. V CLARK	2891

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	8	10												
2	2	9	11												
3	3	10	12												
4	4	11	13												
	5	12	14												
5	6		15												
6	7	13	16												
	8	14	17												
7	9														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	14	
/S. V. CLARK/ Primary Examiner, Art Unit 2891	16 September 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office — Part of Paper No.: 20200916

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Micron v. YMTC
IPR2025-00118

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/207,183	Li, Zhiguo
	Examiner	Art Unit
	S. V CLARK	2891

CPC - Searched*		
Symbol	**Date**	**Examiner**
H01L 23/50, H01L 23/60, H01L 2924/14, H01L 24/06, H01L 27/0292, H01L 23/62	02/24/2020	SVC
updated	08/01/2020	SVC
updated	09/16/2020	SVC

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
257	691, 784	02/24/2020	SVC
438	106	02/24/2020	SVC
updated		08/01/2020	SVC
updated		09/16/2020	SVC

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
EAST	02/24/2020	SVC

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Micron v. YMTC
IPR2025-00118

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/207,183	Li, Zhiguo
	Examiner	Art Unit
	S. V CLARK	2891

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
257	691, 784, PG PUBS	09/16/2020	SVC
438	106, PG PUBS	09/16/2020	SVC

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Micron v. YMTC
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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BIB DATA SHEET

CONFIRMATION NO. 2734

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
16/207,183	12/02/2018	257	2891	YMTP0079USA3

APPLICANTS
Yangtze Memory Technologies Co., Ltd., Wuhan City, CHINA;

INVENTORS
Zhiguo Li, Wuhan City, CHINA;

**** CONTINUING DATA ***************************
This application is a CON of PCT/CN2018/113271 11/01/2018

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
12/20/2018

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
❑ Yes ☑ No	❑ Yes ☑ No	/S V CLARK/ Examiner's Signature	❑ Initials	CHINA	3	17	4

ADDRESS

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

TITLE

Integrated Circuit Electrostatic Discharge Bus Structure and Related Method

FILING FEE RECEIVED		
2180	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other _____ ❑ Credit

Micron Ex. 1002, p. 249
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EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	0	(integrated adj circuit) and (ESD adj2 buses) and (pad adj groups) and (bonding adj wires) and (no adj pad)	US-PGPUB; USPAT	OR	OFF	2020/09/16 14:03
L4	0	(integrated adj circuit) and (ESD adj2 bus) and (pad adj groups) and (bonding adj wires) and (no adj pad)	US-PGPUB; USPAT	OR	OFF	2020/09/16 14:04

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16207183
	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2891
	Examiner Name	CLARK, SHEILA V
	Attorney Docket Number	YMTP0079USA3

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6078068	A	2000-06-20	Tamura	
	2	6770963	B1	2004-08-03	Wu	
	3	5365091	A	1994-11-15	Yamagishi	
	4	5347150	A	1994-09-13	Sakai	

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	

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	1	0028664	WO	A3	2001-07-26			
	2	101097304	CN	A	2008-01-02			Abstract
	3	101221629	CN	A	2008-07-16			Abstract

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1		

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Roger Chen/	Date (YYYY-MM-DD)	2020-10-14
Name/Print	Roger Chen	Registration Number	67314

Abstract of CN101221629

A chip for a smart card including a plurality of electrical contacts for communication of data with a smart card reader is disclosed. In one embodiment, a chip for a smart card includes a core circuit and a plurality of input/output pads corresponding to said set of electrical contacts, wherein said input/output pads are divided into at least a first column and a second column placed immediately adjacent to the first column, such that the first and second columns form a cluster. In another embodiment, eight input/output pads are divided into two columns, placed immediately adjacent to each other. The cluster may be partially surrounded by the core circuit. The chip may further comprise an ESD network, comprising VDD and GND buses for improved ESD protection while reducing the size of the chip.

[19] 中华人民共和国国家知识产权局

[12] 发明专利申请公布说明书

[21] 申请号 200810002239.7

[51] Int. Cl.
G06K 19/077 (2006.01)
H01L 27/02 (2006.01)
H01L 23/482 (2006.01)
H01L 23/60 (2006.01)
H05K 9/00 (2006.01)

[43] 公开日 2008 年 7 月 16 日

[11] 公开号 CN 101221629A

[22] 申请日 2008.1.2
[21] 申请号 200810002239.7
[30] 优先权
[32] 2007. 1.10 [33] US [31] 11/651,870
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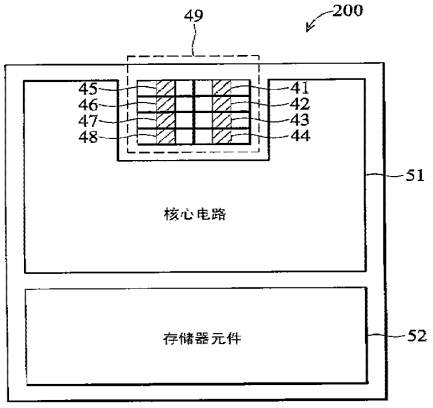
权利要求书 2 页 说明书 7 页 附图 5 页

[54] 发明名称

智能卡芯片以及放置输入/输出焊盘的方法

[57] 摘要

一种智能卡芯片以及放置输入/输出焊盘的方法，该智能卡芯片包括用于向智能卡读取器传送数据的多个电性接点。 在一个实施例中，智能卡芯片包括核心电路以及对应于电性接点的多个输入/输出焊盘，其中输入/输出焊盘划分成至少一个第一列以及放置成与第一列直接相邻的第二列，使得第一列以及第二列形成丛聚。 在另一个实施例中，八个输入/输出焊盘被划分成彼此直接相邻的两列。 丛聚可被核心电路部分地包围。 芯片还可包括静电放电网络，包括 VDD 以及 GND 总线，以改善静电放电保护而减少芯片的尺寸。 本发明能够大幅减少芯片尺寸，而仍然提供极佳的静电放电功能，并且不限定芯片内丛聚的配置；此外，本发明能够容易地与芯片内电压稳压器整合。



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1.一种智能卡芯片，包括用于向智能卡读取器传送数据的多个电性接点，上述智能卡芯片包括：

核心电路；以及

多个输入/输出焊盘，对应于所述电性接点，其中所述输入/输出焊盘划分成至少一个第一列以及放置成与所述第一列直接相邻的第二列，使得所述第一列以及所述第二列形成丛聚。

2．如权利要求 1 所述的智能卡芯片，其中所述第一列或所述第二列具有至少四个输入/输出焊盘。

3．如权利要求 1 所述的智能卡芯片，其中所述丛聚被所述核心电路的三个邻近侧部分地包围。

4．如权利要求 1 所述的智能卡芯片，其中所述多个输入/输出焊盘包括电源焊盘、接地焊盘、串行数据传送焊盘、时钟信号焊盘、复位焊盘、冗余电源焊盘以及冗余接地焊盘，并且所述输入/输出焊盘放置在所述丛聚内，以使得所述串行数据传送焊盘、所述时钟信号焊盘以及所述复位焊盘被所述电源焊盘、所述冗余电源焊盘、所述接地焊盘以及所述冗余接地焊盘部分地围住。

5．如权利要求 4 所述的智能卡芯片，还包括：静电放电网络，包括电性连接至所述电源焊盘的至少一个 VDD 总线，以及电性连接至所述接地焊盘的至少一个 GND 总线，使得所述 VDD 总线与所述 GND 总线放置成大体上平行于所述第一列与所述第二列，其中所述 VDD 总线放置在所述丛聚的各侧并且所述 GND 总线放置在所述第一列与所述第二列之间，其中各所述输入/输出焊盘经由静电放电单元而至少耦接至所述 GND 总线或耦接至至少一个 VDD 总线，以提供变短的静电放电的放电路径。

6．如权利要求 5 所述的智能卡芯片，还包括：VDD/GND 保护环结构，用于防止闩锁；以及至少一个或多个边缘单元，具有所述 VDD/GND 保护环结构。

7．一种放置输入/输出焊盘的方法，适用于包括核心电路以及用于向智能卡读取器传送数据的多个输入/输出焊盘的智能卡芯片，所述方法包括以下

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步骤：

将所述输入/输出焊盘划分成至少一个第一列以及第二列，所述第一列以及所述第二列具有相同数量的输入/输出焊盘；以及

将所述第一列以及所述第二列放置成彼此直接相邻，以在所述核心电路内形成丛聚。

8．如权利要求 7 所述的放置输入/输出焊盘的方法，其中所述丛聚被所述核心电路的至少三个邻近侧部分地包围。

9．如权利要求 7 所述的放置输入/输出焊盘的方法，其中所述第一列包括至少一个接地焊盘以及串行数据传送焊盘。

10．如权利要求 9 所述的放置输入/输出焊盘的方法，其中所述第二列包括至少一个电源焊盘、复位焊盘以及时钟信号焊盘。

11．如权利要求 10 所述的放置输入/输出焊盘的方法，其中所述接地焊盘以及所述电源焊盘被放置成彼此直接相邻，以减少电源或接地总线的绕线面积，并通过减少电源或接地总线的电阻来改善静电放电的功能。

12．如权利要求 10 所述的放置输入/输出焊盘的方法，其中所述丛聚还包括冗余接地焊盘以及冗余电源焊盘。

13．如权利要求 12 所述的放置输入/输出焊盘的方法，其中所述输入/输出焊盘放置在所述丛聚内，以使得所述串行数据传送焊盘、所述时钟信号焊盘以及所述复位焊盘被所述电源供应焊盘、所述冗余电源供应焊盘、所述接地焊盘以及所述冗余接地焊盘部分地围住。

14．如权利要求 7 所述的放置输入/输出焊盘的方法，其中所述丛聚还包括至少一个或多个测试焊盘，以及来自电压稳压器的输入的焊盘，以允许容易地与芯片内电压稳压器整合。

15．如权利要求 7 所述的放置输入/输出焊盘的方法，其中所述丛聚还包括至少一个或多个边缘单元，具有保护环结构以防止闩锁。

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智能卡芯片以及放置输入/输出焊盘的方法

技术领域

本发明涉及智能卡（smart card）芯片，特别涉及智能卡内所使用芯片的输入/输出焊盘（pad）的配置，用以改善静电放电（electrostatic discharge，ESD）功能并减少芯片的布局面积。

背景技术

智能卡是一种内嵌集成电路（integrated circuit）芯片的塑胶卡片型式的卡，集成电路芯片可包括非易失性（non-volatile）存储器存储元件以及一些其他特定的安全逻辑电路。智能卡增强系统广泛使用在保健、银行业务、娱乐以及运输等范围。

智能卡包括接触卡、无接触（contactless）卡以及混合（hybrid）卡。无接触卡使用射频（radio frequency，RF）来进行卡片与卡片读取器之间的传送。接触卡以及混合卡包括位于卡片外侧的一组电性接点，用以插入且耦接于卡片读取器。

智能卡传统上包括芯片，其中芯片包括微处理器以及可经由电性接点进行存取的存储器，例如：随机存取存储器（Random Access Memory，RAM）、只读存储器（Read Only Memory，ROM）以及电可擦可编程只读存储器(Electrically Erasable Programmable Read Only Memory，EEPROM)。接点提供电源、串行数据（serial data）传送的输入/输出、用以读取智能卡时钟（clock，CLK）信号的连接、用以复位（reset，RST）智能卡的连接以及智能卡的编程电压（programming voltage）的连接。这些接点的尺寸、功能以及位置由工业标准 ISO 7816-2 以及 7816-3 来规定（参考图 1A）。上述标准可允许不同的制造商生产可互相兼容的智能卡以及装置。

图 1B 示出智能卡的输入以及输出（I/O）焊盘的传统布局。然而，图 1B 布局中的主要缺点是需要越过芯片（cross-chip）的 VDD/GND（或是图 1B 中 VCC/GND）总线金属连接来提供足够的静电放电保护网络。越过芯片的

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VDD/GND 总线金属连接会增加芯片的尺寸，所以不是令人满意的解决方案。

嵌入在智能卡内的芯片传统上是由互补金属氧化物半导体（complementary metal oxide semiconductor，CMOS）技术制造的，并需要免于受到静电放电的损害。当智能卡被到处携带、从皮夹内放入和取出并插入至卡片读取器时，静电电荷会累积在智能卡上。当足够的电荷累积在智能卡的特定尖端时，电荷将被传导至最低电位的电压（传统为接地端）。在累积电荷的尖端到较低电位的路径上，当电荷足够高时会损害芯片。与芯片所能承受的最大电压或电流相比，例如：金属氧化物半导体的栅极氧化物可能被仅略高于一般供应电压（5 伏特、3.3 伏特或甚至更低）的电压所破坏，由累积电荷所感应的电压和电流可能相当大，例如：2000 伏特甚至更大的电压，或是越过 1.5k 欧姆的电阻的 1.3 安培以上甚至更大的电流。

传统上将静电放电保护电路加入到芯片的结合焊盘（bond pad）上，其中结合焊盘为提供芯片耦接至外部电路、电力供应、接地端以及电信号的连接。静电放电保护电路必须能够允许芯片正常操作，使得静电放电保护电路在芯片正常操作期间能有效地与芯片的核心电路隔离。

具有四种 P 型以及 N 型半导体材料可选择层的半导体元件或被称为可控硅整流器（silicon controlled rectifier，SCR）的 PNPN 元件可以是静电放电保护电路中能防止静电放电产生损害的最有效的元件之一。可控硅整流器操作在两种模式：阻隔（blocking）模式以及闩锁（latch up）模式。在阻隔模式中，可控硅整流器会阻挡电流通过，使得静电放电保护电路不会对要被保护的核心电路造成影响。当可控硅整流器内有足够的电流再生时，闩锁情况被触发。闩锁出现在互补寄生双极性晶体管结构中，其传统上存在于互补金属氧化物半导体结构内。既然互补寄生双极性晶体管非常靠近，互补双极性结构即能互相电性作用，从而形成动作表现如 PNPN 二极管的元件结构。静电放电事件中，大电流能流经可控硅整流器从而越过核心电路。

然而，无论使用何种结构作为静电放电保护电路，智能卡上的传统芯片还是必须包括会增加芯片尺寸的越过芯片的 VDD/GND 总线金属连接（参考图 1B）。

因此，在智能卡设计的技术中，需要能够对智能卡内所使用的芯片的输入/输出焊盘提供有效空间布局的新设计。

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发明内容

本发明涉及智能卡芯片，特别涉及智能卡内所使用芯片的输入/输出焊盘的配置，用以改善静电放电功能并减少芯片的布局面积。仅作为示例来说，本发明可用于智能卡内所使用的芯片上。然而，本领域技术人员可认识到，本发明还具有更大范围的实用性。

在一个特定实施例中，本发明提供一种具有新输入/输出焊盘配置的智能卡芯片。在一个实施例中，智能卡芯片包括核心电路。芯片还包括对应于上述电性接点的多个输入/输出焊盘，其中上述输入/输出焊盘划分成至少一个第一列以及放置成与上述第一列直接相邻的第二列，使得上述第一列以及上述第二列形成丛聚。

上述智能卡芯片中，第一列或第二列可具有至少四个输入/输出焊盘。

上述智能卡芯片中，丛聚可被核心电路的三个邻近侧部分地包围。

上述智能卡芯片中，多个输入/输出焊盘可包括电源焊盘、接地焊盘、串行数据传送焊盘、时钟信号焊盘、复位焊盘、冗余电源焊盘以及冗余接地焊盘，并且所述输入/输出焊盘放置在所述丛聚内，以使得串行数据传送焊盘、时钟信号焊盘以及复位焊盘被电源焊盘、冗余电源焊盘、接地焊盘以及冗余接地焊盘部分地围住。

上述智能卡芯片还可包括：VDD/GND 保护环结构，用于防止闩锁；以及至少一个或多边缘单元，具有 VDD/GND 保护环结构。

在另一个实施例中，公开一种放置输入/输出焊盘的方法，适用于包括核心电路以及与智能卡读取器传送数据的多个输入/输出焊盘的智能卡芯片。上述方法包括将上述输入/输出焊盘划分成至少一个第一列以及第二列，上述第一列以及上述第二列具有相同数量的输入/输出焊盘。上述方法还包括将上述第一列以及上述第二列放置成彼此直接相邻，以在上述核心电路内形成丛聚。

上述放置输入/输出焊盘的方法中，丛聚可被核心电路的至少三个邻近侧部分地包围。

上述放置输入/输出焊盘的方法中，第一列可包括至少一个接地焊盘以及串行数据传送焊盘。

上述放置输入/输出焊盘的方法中，第二列可包括至少一个电源焊盘、复位焊盘以及时钟信号焊盘。

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上述放置输入/输出焊盘的方法中，接地焊盘以及电源焊盘可放置成彼此直接相邻，以减少电源或接地总线的绕线面积，并通过减少电源或接地总线的电阻来改善静电放电的功能。

上述放置输入/输出焊盘的方法中，从聚还可包括冗余接地焊盘以及冗余电源焊盘。

上述放置输入/输出焊盘的方法中，输入/输出焊盘可放置在从聚内，以使得串行数据传送焊盘、时钟信号焊盘以及复位焊盘被电源供应焊盘、冗余电源供应焊盘、接地焊盘以及冗余接地焊盘部分地围住。

上述放置输入/输出焊盘的方法中，从聚还可包括至少一个或多个测试焊盘，以及来自电压稳压器的输入的焊盘，以允许容易地与芯片内电压稳压器整合。

上述放置输入/输出焊盘的方法中，从聚还可包括至少一个或多个边缘单元，具有保护环结构以防止闩锁。

在又一个实施例中，芯片包括静电放电网络，其包括电性连接至上述电源焊盘的至少一个 VDD 总线，以及电性连接至上述接地焊盘的至少一个 GND 总线，上述 VDD 总线与上述 GND 总线被放置成大体上平行于上述输入/输出焊盘的上述列。上述 VDD 总线可被放置在上述 cluster 的各侧且上述 GND 总线被放置在上述列之间，其中各上述输入/输出焊盘经由静电放电单元而至少耦接至上述 GND 总线或 VDD 总线，因此提供从上述输入/输出焊盘至上述 GND 总线或 VDD 总线直至接地端的短路径。

对客户芯片而言，既然不需要越过芯片的 VDD/GND 总线连接，所以优于传统相关技术的新配置的优点之一是芯片尺寸至少可减少 3%至 5%。另一个优点包括本发明可改善静电放电功能。既然从聚可被放置在芯片内的任何地方，因此可容易地与芯片内电压稳压器整合。

附图说明

图 1A 示出根据 ISO 标准的智能卡接点的简单布局图；

图 1B 示出智能卡芯片中输入/输出焊盘的传统配置的简单布局图；

图 2 示出根据本发明一个实施例所述智能卡芯片中输入/输出焊盘的配置的简单布局图；

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图 3 示出根据本发明另一个实施例所述智能卡芯片中输入/输出焊盘的配置的放大布局图；以及

图 4 示出根据本发明又一个实施例所述智能卡芯片中输入/输出焊盘的配置以及静电放电网络的简单布局图。

其中，附图标记说明如下：

1-8~电性接点

10-11~距离

100~图示

102、200~芯片

21-28、41-48~输入/输出焊盘

29、30~列

31、51~核心电路

32、52~存储器元件

33、34~越过芯片的 VDD/GND 总线连接

400~布局视图

49、300~丛聚

61-65、70~焊盘

68~冗余接地焊盘

69~冗余电源焊盘

71、72~测试焊盘

73~丛聚边缘单元

80~静电放电网络

81、82~VDD 总线

83~GND 总线

86-97~静电放电保护元件

9~智能卡边缘

具体实施方式

为让本发明的上述和其他目的、特征、和优点能更明显易懂，下文特举出较佳实施例，并配合所附图式，作详细说明如下：

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实施例：

图 1A 示出根据 ISO 标准的智能卡接点的简单布局图。如图 1A 所示，图示 100 示出 ISO 标准中与智能卡边缘 9 的电性接点 1-8 相关的配置。接点 1 与接点 5 被设计成耦接至供应电源以及接地端。接点 7 作为串行数据的输入/输出焊盘。接点 3 作为用以读出智能卡时钟信号的连接。接点 2 作为用以复位智能卡的连接，而接点 6 用于智能卡的编程电压的连接。接点的配置分别由从智能卡上边以及左边的一组距离 10 与距离 11 来决定。接点 4 以及接点 8 保留给将来使用。

图 1B 示出智能卡芯片中输入/输出焊盘的传统配置的简单布局图。图 1A 所示出的 ISO 标准接点 1-8 的配置会导致如图 1B 所示的智能卡芯片的输入/输出焊盘的传统配置。传统上，芯片 102 具有位于芯片 102 边缘、划分成列（column）29 与列 30、并由核心电路 31 分隔的输入/输出焊盘 21-28。

芯片 102 还包括存储器元件 32。核心电路 31 与存储器元件 32 均对静电放电非常敏感，因此芯片 102 也必须包括由越过芯片的 VDD/GND 总线连接 33、34 构成的足够的静电放电保护电路。上述越过芯片的 VDD/GND 总线连接会显著增加芯片的总面积以及总线电阻。

图 2 示出根据本发明一个实施例的智能卡芯片中输入/输出焊盘的配置的简单布局图。参考图 2，其示出智能卡的输入/输出焊盘 41-48 的布局。与传统配置相比，列 29 与列 30（参考图 1B）被放置成彼此直接紧邻，并组成丛聚（cluster）49。通过修改核心电路 51 的形状，就能部分地包围丛聚 49（以及输入/输出焊盘 41-48）。芯片 200 还包括存储器元件 52。全部的输入/输出焊盘 41-48 还聚集在丛聚 49 的相连区域内。

图 3 示出根据本发明另一个实施例的智能卡芯片中输入/输出焊盘的配置的放大布局图。丛聚 300 包括作为电源（VDD）的焊盘 61、用以复位芯片的焊盘 62（RST）、用以读取芯片的脉冲信号的焊盘 63（CLK）、作为接地端的焊盘 64，以及与芯片传送串行数据的焊盘 65（IO）。然而，与图 2 中的丛聚 49 相比，丛聚 300 额外地包括冗余接地焊盘（Dummy GND）68、冗余电源焊盘（Dummy VDD）69、作为来自电压稳压器的输入的焊盘 70（VDDC）以及测试焊盘 71（TEST PAD_1）与测试焊盘 72（TEST PAD_2）。丛聚边缘单元 73 包括 VDD/GND 保护环（guard ring）结构以防止闩锁现象。

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如图 3 所示，分别作为电源以及接地的焊盘 61 与焊盘 64 被放置成背对背。增加冗余接地焊盘 68 以及冗余电源焊盘 69 以改善静电放电保护功能，使得焊盘 62、焊盘 63 与焊盘 65 被 VDD/GND 焊盘（焊盘 61、64）以及冗余 VDD/GND 焊盘（焊盘 68、69）所包围。

图 4 示出根据本发明另一个实施例的智能卡芯片中输入/输出焊盘的配置以及静电放电网络的简单布局图。图 4 示出图 3 中智能卡芯片内输入/输出焊盘的配置以及静电放电网络 80 的布局视图 400。静电放电网络 80 包括作为主要静电放电总线的 VDD 总线 81、82 以及 GND 总线 83。静电放电网络 80 还包括多个静电放电保护元件 86-97（例如可控硅整流器），静电放电保护元件 86-97 分别耦接于焊盘 61-68 以及 VDD 总线 81、82 与 GND 总线 83 之间，用以例如当使用者意外地接触到智能卡的接触点时，保护各输入/输出端免于任何意外的静电放电。

可以了解到，包括焊盘 64、65 的第一组结合焊盘以及包括焊盘 61-63 的第二组结合焊盘被静电放电金属总线（GND）包围在两侧。耦接于第一组结合焊盘以及第二组结合焊盘之间的静电放电金属总线（VDD）经由背对背的 VDD/GND 与冗余 VDD/GND 与边缘单元相邻。与现有技术相比，上述设计提供变短的全面静电放电路径以将电荷传导至接地端。本领域技术人员可认识到，VDD 总线以及 GND 总线越短，则电阻越低且放电速度越快。

本发明排除了对于越过芯片的 VDD/GND 总线连接的需要，因此大幅地减少了芯片尺寸（在客户芯片上大约减少 3％至 5％），而仍然提供极佳的静电放电功能。由于 VDD 总线以及 GND 总线的电阻减少，本发明还提供较佳的静电放电保护功能，且没有限定芯片内丛聚的配置。另外，本发明能够容易地与芯片内电压稳压器（voltage regulator，VR）整合，以提供额外的冗余接地焊盘以及其他电源焊盘，如图 3 所示。

上述说明提供许多不同的实施例或是用以实施本发明不同特征的实施例。描述构成以及步骤的特定实施例可帮助理解本发明。当然，上述说明只是实施例，并没有打算在权利要求意义上限定本发明。

本发明虽以优选实施例公开如上，然而所公开内容并非用以限定本发明的范围，任何本领域技术人员，在不脱离本发明的精神和范围内，当可做一定的更动与修改，因此本发明的保护范围应以所附权利要求为准。

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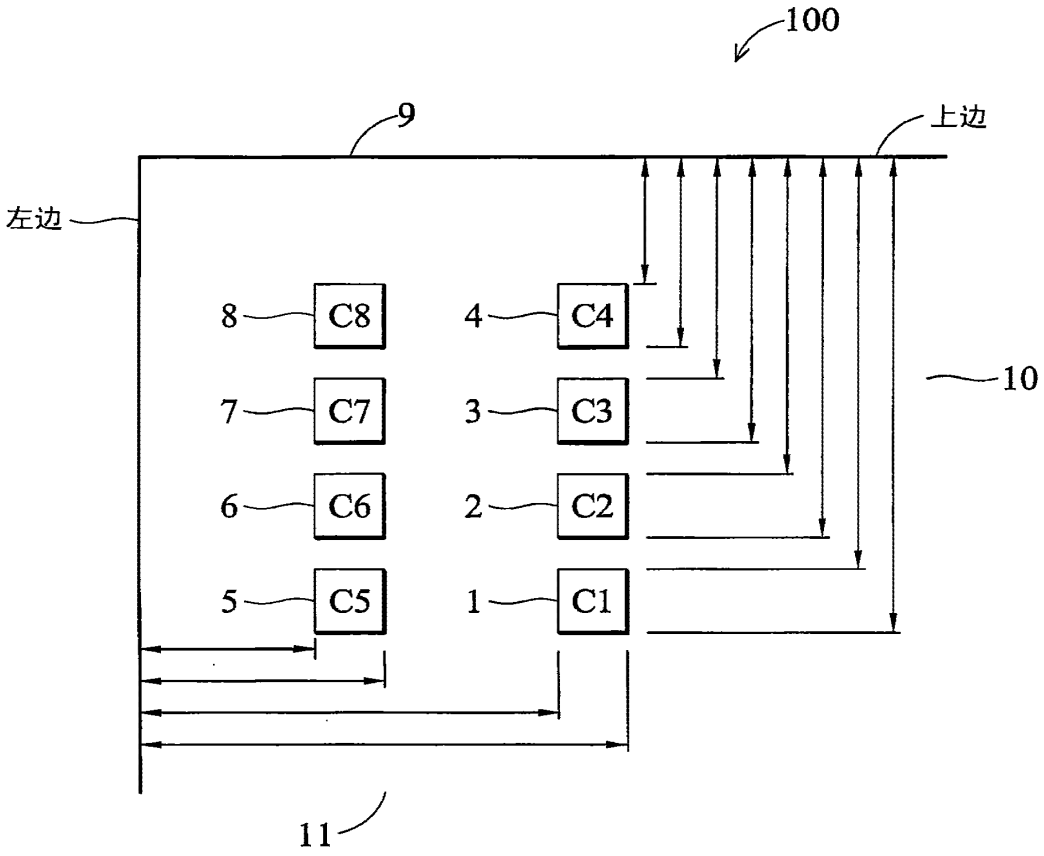


图1A

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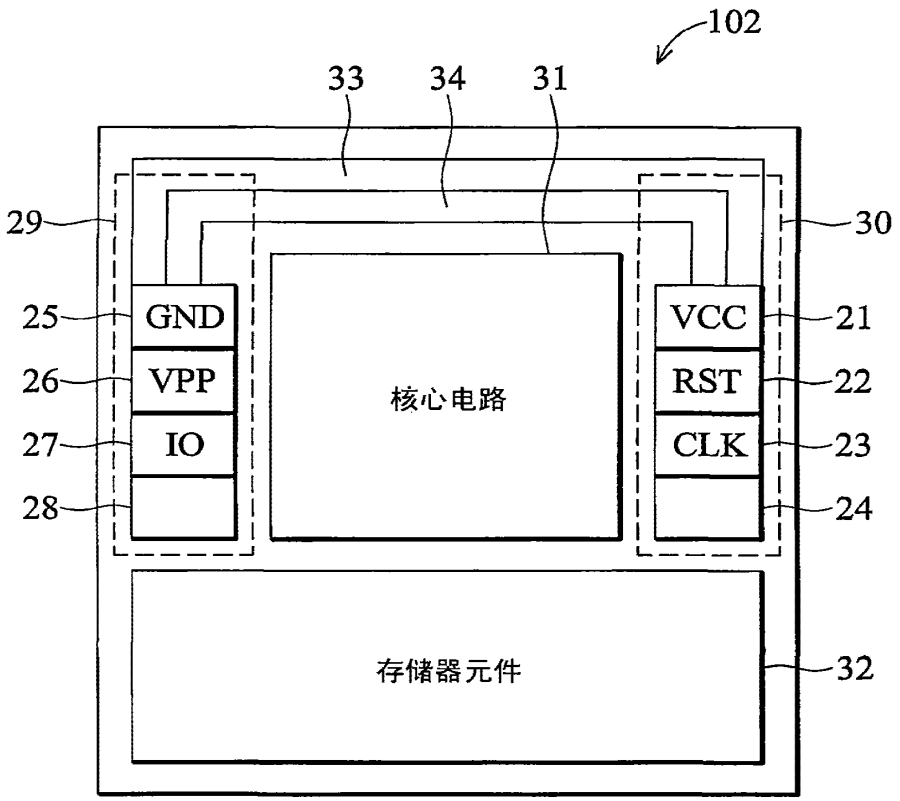


图1B

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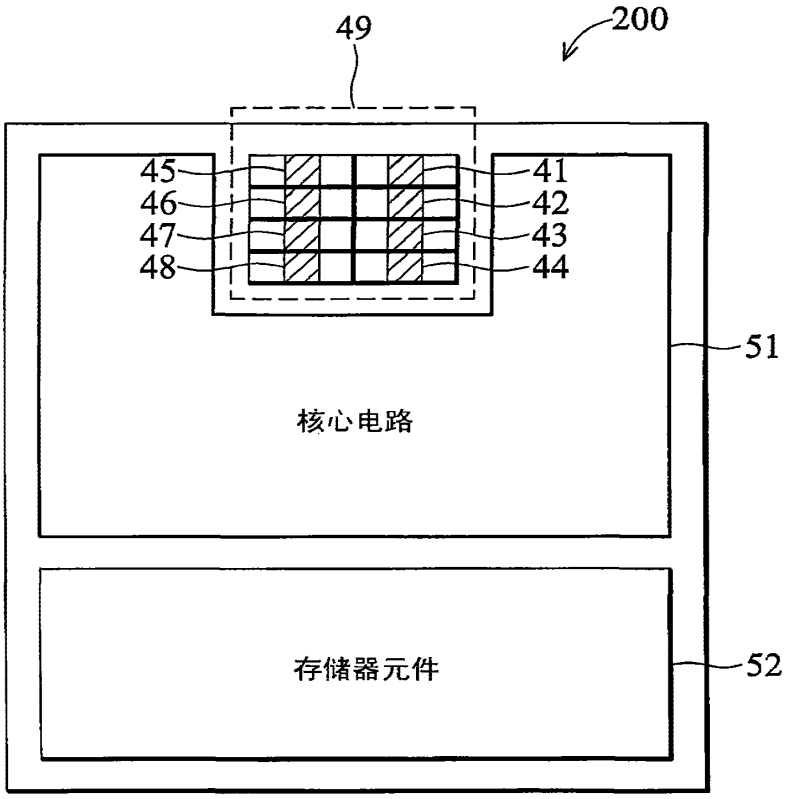


图2

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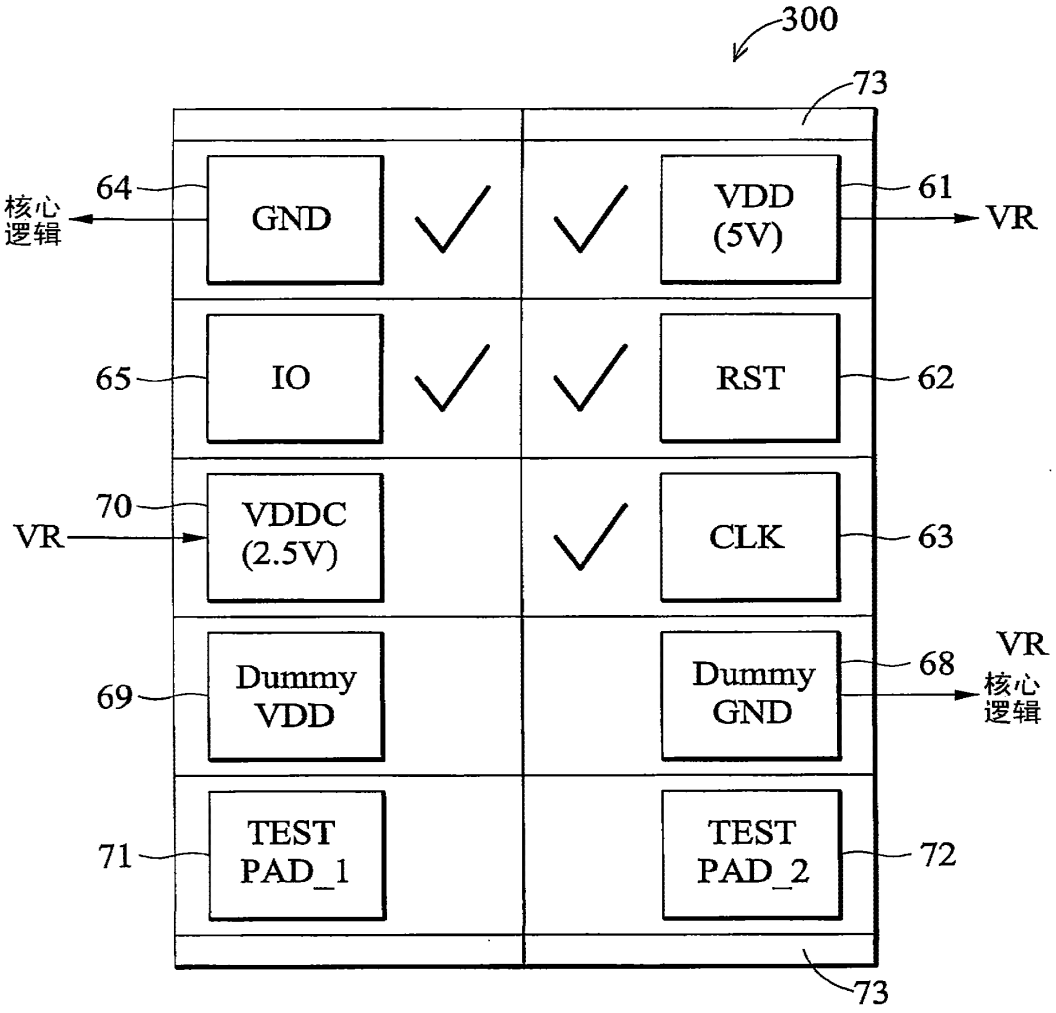


图3

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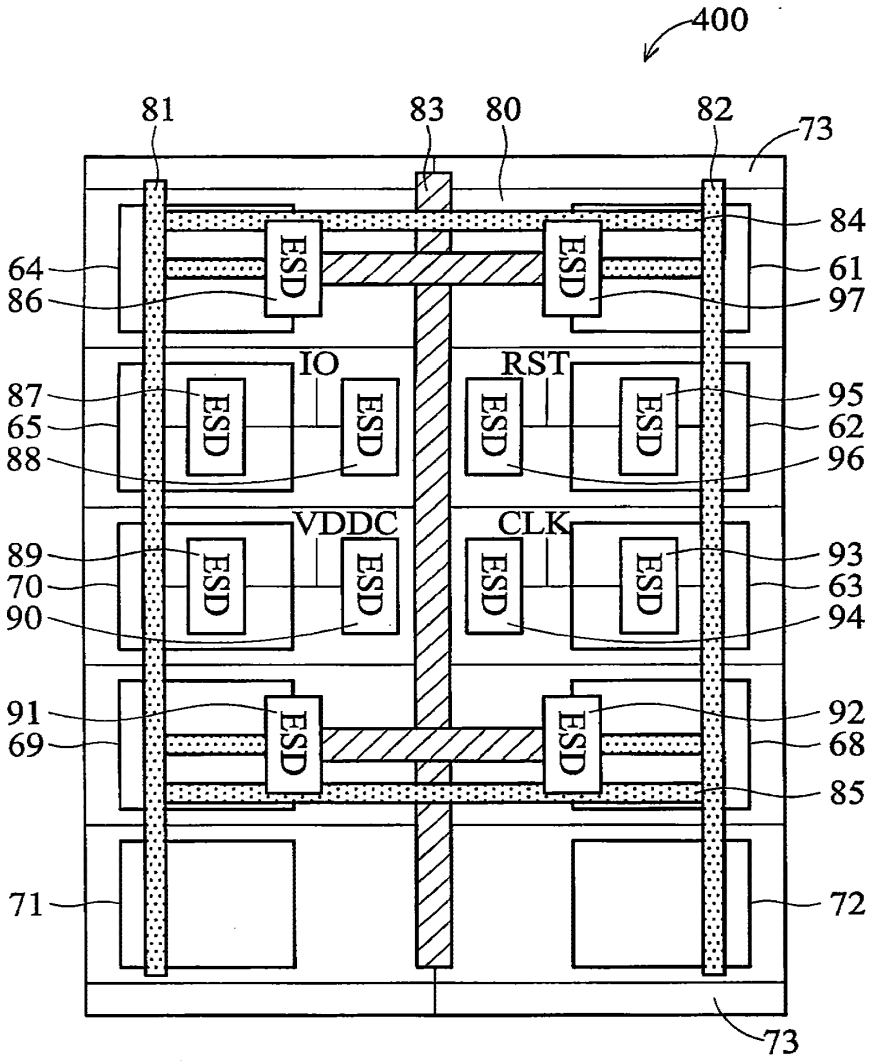


图4

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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 May 2000 (18.05.2000)

PCT

(10) International Publication Number
WO 00/28664 A3

(51) International Patent Classification[7]: H03J 3/08, 3/18, H03D 7/16, H03K 3/283, H03G 1/00, H03J 1/00, H03B 5/36

(21) International Application Number: PCT/US99/26700

(22) International Filing Date:
12 November 1999 (12.11.1999)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

60/108,209	12 November 1998 (12.11.1998)	US
60/108,210	12 November 1998 (12.11.1998)	US
60/108,459	12 November 1998 (12.11.1998)	US
60/117,609	28 January 1999 (28.01.1999)	US
60/136,115	26 May 1999 (26.05.1999)	US
60/136,116	26 May 1999 (26.05.1999)	US
60/136,654	27 May 1999 (27.05.1999)	US
60/159,726	15 October 1999 (15.10.1999)	US

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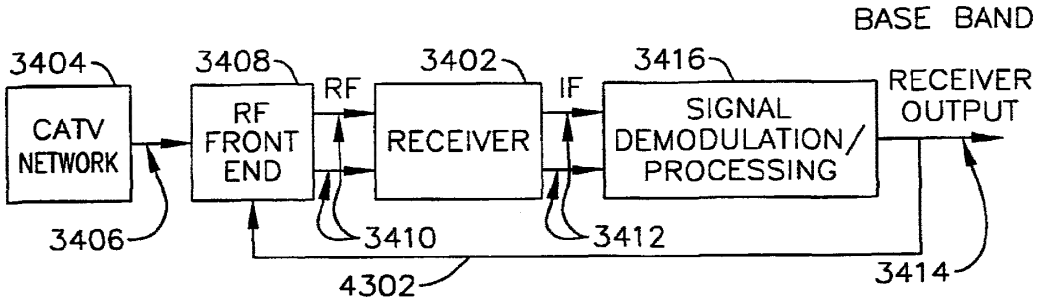
(74) Agent: **RAHN, LeRoy, T.**; Christie, Parker & Hale, LLP, Post Office Box 7068, Pasadena, CA 91109-7068 (US).

(81) Designated States *(national)*: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent

[Continued on next page]

(54) Title: FULLY INTEGRATED TUNER ARCHITECTURE



(57) Abstract: An integrated receiver with channel selection and image rejection substantially implemented on a single CMOS integrated circuit is described. A receiver front end provides programable attenuation and a programable gain low noise amplifier. Frequency conversion circuitry advantageously uses LC filters integrated onto the substrate in conjonction with image reject mixers to provide sufficient image frequency rejection. Filter tuning and inductor Q compensation over temperature are performed on chip. The filters utilize multi track spiral inductors. The filters are tuned usingt local oscillators to tune a substitute filter, and frequency scaling during filter component values to those of the filter being tuned. In conjunction with filtering, frequency planning provides additional image rejection. The advantageous choice of local oscillator signal generation methods on chip is by PLL out of band local oscillation and by direct synthesis for in band local oscillator. The VCOs in the PLLs are centered using a control circuit to center the tuning capacitance range. A differential crystal oscillator is advantageously used as a frequency reference. Differential signal transmission is advantageously used throughout the receiver.

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(AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(88) Date of publication of the international search report:
26 July 2001

(15) Information about Correction:
Previous Correction:
see PCT Gazette No. 07/2001 of 15 February 2001, Section II

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/26700

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03J3/08 H03J3/18 H03D7/16 H03K3/283 H03G1/00
H03J1/00 H03B5/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03J H03H H03D H03K H03G H03B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	POOLE S J ET AL: "A CMOS SUBCRIBER LINE AUDIO PROCESSING CIRCUIT INCLUDING ADAPTIVE BALANCE" PROCEEDINGS OF THE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS,US,NEW YORK, IEEE, vol. CONF. 21, 1988, pages 1931-1934, XP000124806 ISBN: 951-721-240-2 Paragraph titled: "DIGITAL ARCHITECTURE" page 1933 -page 1934; figure 4 ---	1,2
X	US 4 789 976 A (FUJISHIMA MASAKAZU) 6 December 1988 (1988-12-06) column 6, line 40 -column 7, line 3; figure 1 --- -/--	1,2

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
20 December 2000	10. 01. 2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Peeters, M

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 393 717 A (SANYO ELECTRIC CO) 24 October 1990 (1990-10-24) page 2, line 13 - line 325; figure 1	1,2
X	DE 37 23 778 A (TOSHIBA KAWASAKI KK) 28 January 1988 (1988-01-28) page 5, line 8 - line 39; figure 5	1
A	US 5 031 233 A (RAGAN LAWRENCE H) 9 July 1991 (1991-07-09)	
A	DE 195 06 324 C (SIEMENS AG) 12 October 1995 (1995-10-12)	
X	GB 2 058 505 A (TEXAS INSTRUMENTS INC) 8 April 1981 (1981-04-08) page 3, line 126 -page 4, line 44	23,24,39
A	page 5, line 101 - line 105	26
X	US 5 715 012 A (LIMBERG ALLEN LEROY ET AL) 3 February 1998 (1998-02-03)	101-103
A	column 6, line 37 -column 7, line 20; figure 1 column 13, line 43 - line 55	23,24, 28,42, 49,53
X	US 5 737 035 A (ROTZOLL ROBERT RUDOLF) 7 April 1998 (1998-04-07)	101-103
A	figure 4	24,29,39
A	EP 0 629 040 A (THOMSON CONSUMER ELECTRONICS) 14 December 1994 (1994-12-14) figure 2	42,99, 100
A	US 4 211 975 A (KURODA MASAHIRO) 8 July 1980 (1980-07-08) column 3, line 26 - line 53; figure 4	25,28,54
A	US 5 200 826 A (SEONG CHANG-YEOL) 6 April 1993 (1993-04-06) abstract; figure 2	40,96
X	US 4 353 039 A (HUNTLEY CHRISTOPHER R) 5 October 1982 (1982-10-05) figure 1	30,31,34
X	US 4 141 209 A (BARNETT JAMES V ET AL) 27 February 1979 (1979-02-27) claim 1; figure 1	30,32
X	EP 0 767 532 A (SONY CORP) 9 April 1997 (1997-04-09) figure 2	30

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 133 618 A (ITT IND GMBH DEUTSCHE ;ITT (US)) 6 March 1985 (1985-03-06) figure 1 ---	106
X	US 5 757 220 A (MURDEN FRANKLIN M ET AL) 26 May 1998 (1998-05-26) column 2, line 41 - line 60; figure 1 ---	35,108
X	LEUNG L H Y ET AL: "10-MHZ 60-DB DYNAMIC-RANGE 6-DB VARIABLE GAIN AMPLIFIER" IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS,US,NEW-YORK, NY: IEEE, 9 June 1997 (1997-06-09), pages 173-176, XP000805369 ISBN: 0-7803-3584-8 page 174, right-hand column, paragraph 2 -page 175, left-hand column, paragraph 1; figures 4-6 ---	35,108
X	GILBERT B: "A LOW-NOISE WIDEBAND VARIABLE-GAIN AMPLIFIER USING AN INTERPOLATED LADDER ATTENUATOR" IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE,US,IEEE INC. NEW YORK, vol. 34, 1 February 1991 (1991-02-01), pages 280-281,330, XP000238340 ISSN: 0193-6530 figure 4 ---	35,108
X	WO 98 47237 A (PHILIP A RUBIN AND ASSOCIATES) 22 October 1998 (1998-10-22) the whole document ---	104
X	US 5 251 324 A (MCMULLAN JR JAY C) 5 October 1993 (1993-10-05) the whole document ---	105
Y	US 5 077 541 A (GILBERT BARRIE) 31 December 1991 (1991-12-31) figure 7 ---	107
Y	US 5 581 213 A (LINDER LLOYD F ET AL) 3 December 1996 (1996-12-03) column 7, line 48 - line 55; figure 7 ---	107
A	US 5 630 214 A (NODA MASAKI ET AL) 13 May 1997 (1997-05-13) figure 1 ---	107
X	US 5 423 076 A (WESTERGREN LARRY L ET AL) 6 June 1995 (1995-06-06) column 4, line 67 -column 7, line 44; figure 1 --- -/--	109,110

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INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 311 318 A (DOBROVOLNY PIERRE) 10 May 1994 (1994-05-10) column 3, line 11 - line 27 -----	109

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

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Ir. ational application No.
PCT/US 99/26700

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

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FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-22, 70-72, 74, 76, 86

An integrated circuit chip including a circuit to be adjusted, an on-chip dummy circuit replicating the circuit to be adjusted, means for adjusting the dummy circuit and means for transferring the state of the dummy circuit to the circuit to be adjusted.

XP124806, Poole et al: "A CMOS SUBCRIBER LINE AUDIO PROCESSING CIRCUIT INCLUDING ADAPTIVE BALANCE" discloses all the features of claims 1 and 2. It thus deprives claim 1 of novelty and already solves the problem underlying the present invention.

2. Claims: 23-29, 39-69, 73, 75, 77-85, 87-103

XP124806, Poole et al: "A CMOS SUBCRIBER LINE AUDIOPROCESSING CIRCUIT INCLUDING ADAPTIVE BALANCE" does not disclose a receiver that is partially implemented on an IC, a TV-receiver, an integrated receiver and method comprising image rejection measures, a CATV tuner or a VCR, and therefore all the features of claims 23-29, 39-69, 75, 77-85 and 87-103, are considered to be the potential special technical features of the second invention.
These features are obviously not the same as those of the first invention.

3. Claims: 30-34 , 106

XP124806, Poole et al: "A CMOS SUBCRIBER LINE AUDIOPROCESSING CIRCUIT INCLUDING ADAPTIVE BALANCE" does not disclose a differential oscillator or a crystal oscillator, and therefore all the features of claims 30-34 and 106 are considered to be the potential special technical features of the third invention.
These features are obviously not the same as those of the first invention.

4. Claims: 35-38, 108

XP124806, Poole et al: "A CMOS SUBCRIBER LINE AUDIOPROCESSING CIRCUIT INCLUDING ADAPTIVE BALANCE" does not disclose an AGC-circuit or a method for processing a received radio frequency signal and therefore all the features of claims 35-38 and 108 are considered to be the potential special technical features of the fourth invention.
These features are obviously not the same as those of the first invention.

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FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

5. Claim : 104

XP124806, Poole et al: "A CMOS SUBCRIBER LINE AUDIOPROCESSING CIRCUIT INCLUDING ADAPTIVE BALANCE" does not disclose a television set top box and therefore all the features of claim 104 are considered to be the potential special technical features of the fifth invention.
These features are obviously not the same as those of the first invention.

6. Claim : 105

XP124806, Poole et al: "A CMOS SUBCRIBER LINE AUDIOPROCESSING CIRCUIT INCLUDING ADAPTIVE BALANCE" does not disclose a cable modem and therefore all the features of claim 105 are considered to be the potential special technical features of the sixth invention.
These features are obviously not the same as those of the first invention.

7. Claim : 107

XP124806, Poole et al: "A CMOS SUBCRIBER LINE AUDIOPROCESSING CIRCUIT INCLUDING ADAPTIVE BALANCE" does not disclose an integrated receiver front end and therefore all the features of claim 107 are considered to be the potential special technical features of the seventh invention.
These features are obviously not the same as those of the first invention.

8. Claims: 109-110

XP124806, Poole et al: "A CMOS SUBCRIBER LINE AUDIOPROCESSING CIRCUIT INCLUDING ADAPTIVE BALANCE" does not disclose a method of tuning a receiver and therefore all the features of claims 109 and 110 are considered to be the potential special technical features of the eighth invention.
These features are obviously not the same as those of the first invention.

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INTERNATIONAL SEARCH REPORT

rmation on patent family members

International Application No
PCT/US 99/26700

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4789976 A	06-12-1988	NONE	
EP 0393717 A	24-10-1990	JP 2021309 C	19-02-1996
		JP 2279004 A	15-11-1990
		JP 7044383 B	15-05-1995
		CA 2014968 A	20-10-1990
		DE 69028869 D	21-11-1996
		DE 69028869 T	28-05-1997
		ES 2095220 T	16-02-1997
		KR 177149 B	01-04-1999
		US 5317216 A	31-05-1994
		JP 3187511 A	15-08-1991
DE 3723778 A	28-01-1988	JP 7087332 B	20-09-1995
		JP 63026111 A	03-02-1988
		GB 2194402 A,B	02-03-1988
		KR 9002955 B	03-05-1990
		US 4818903 A	04-04-1989
US 5031233 A	09-07-1991	AU 6143390 A	22-02-1991
		WO 9101599 A	07-02-1991
DE 19506324 C	12-10-1995	CA 2170221 A	24-08-1996
		EP 0729229 A	28-08-1996
		JP 8265225 A	11-10-1996
		US 5828589 A	27-10-1998
GB 2058505 A	08-04-1981	US 4162452 A	24-07-1979
		US 4408347 A	04-10-1983
		US 4162451 A	24-07-1979
		BR 7804326 A	03-04-1979
		CA 1110356 A	06-10-1981
		CA 1136222 A	23-11-1982
		DE 2829538 A	25-01-1979
		FR 2408944 A	08-06-1979
		GB 2000926 A,B	17-01-1979
		GB 2058500 A,B	08-04-1981
		JP 1021648 B	21-04-1989
		JP 1547509 C	28-02-1990
		JP 54018208 A	10-02-1979
		NL 7807307 A	09-01-1979
US 5715012 A	03-02-1998	US 5999223 A	07-12-1999
		US 5959699 A	28-09-1999
		US 6137545 A	24-10-2000
US 5737035 A	07-04-1998	NONE	
EP 0629040 A	14-12-1994	NONE	
US 4211975 A	08-07-1980	NONE	
US 5200826 A	06-04-1993	JP 6078227 A	18-03-1994
US 4353039 A	05-10-1982	CA 1162256 A	14-02-1984
US 4141209 A	27-02-1979	NONE	

Micron Ex. 1002, p. 279
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INTERNATIONAL SEARCH REPORT

rmation on patent family members

International Application No
PCT, US 99/26700

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0767532 A	09-04-1997	JP 9102712 A	15-04-1997
		CN 1151631 A	11-06-1997
		SG 48472 A	17-04-1998
		US 5717363 A	10-02-1998
EP 0133618 A	06-03-1985	AU 3126084 A	31-01-1985
		DE 3372432 D	13-08-1987
		JP 60047503 A	14-03-1985
		US 4560955 A	24-12-1985
US 5757220 A	26-05-1998	WO 9828842 A	02-07-1998
WO 9847237 A	22-10-1998	US 6009116 A	28-12-1999
		AU 6967398 A	11-11-1998
		EP 0985276 A	15-03-2000
		US 6108365 A	22-08-2000
US 5251324 A	05-10-1993	US 5235619 A	10-08-1993
		US 5155590 A	13-10-1992
		US 5142690 A	25-08-1992
		US 5255086 A	19-10-1993
		AU 669659 B	20-06-1996
		AU 1680492 A	21-10-1992
		BR 9205792 A	28-06-1994
		CA 2106597 A	20-09-1992
		CN 1066359 A	18-11-1992
		CS 9200834 A	14-10-1992
		EP 0576597 A	05-01-1994
		JP 6506334 T	14-07-1994
		MX 9201232 A	01-10-1992
		PL 169709 B	30-08-1996
		WO 9217027 A	01-10-1992
		AT 174738 T	15-01-1999
		AU 651967 B	11-08-1994
		AU 7562291 A	21-10-1991
		AU 659372 B	11-05-1995
		AU 7564291 A	21-10-1991
		AU 641755 B	30-09-1993
		AU 7583991 A	21-10-1991
		BR 9106266 A	01-12-1992
		BR 9106267 A	01-12-1992
		BR 9106268 A	13-04-1993
		CA 2078561 A	21-09-1991
		CA 2078562 A	21-09-1991
		CA 2078563 A	21-09-1991
		CN 1058876 A	19-02-1992
		CN 1059250 A	04-03-1992
		CN 1056788 A	04-12-1991
		DE 69126432 D	10-07-1997
		DE 69126432 T	08-01-1998
		DE 69130642 D	28-01-1999
		DE 69130642 T	02-09-1999
		EP 0532504 A	24-03-1993
		EP 0532507 A	24-03-1993
		EP 0531302 A	17-03-1993
		ES 2108711 T	01-01-1998
		ES 2127195 T	16-04-1999
		MX 174056 B	06-04-1994

Form PCT/ISA/210 (patent family annex) (July 1992)

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INTERNATIONAL SEARCH REPORT

rmation on patent family members

International Application No
PCT/US 99/26700

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5251324 A		MX 174456 B	17-05-1994
		WO 9115062 A	03-10-1991
		WO 9115065 A	03-10-1991
		WO 9115064 A	03-10-1991
		US 5505901 A	09-04-1996
		US 5045816 A	03-09-1991
		US 5225902 A	06-07-1993
		AU 642367 B	14-10-1993
		AU 7568591 A	21-10-1991
US 5077541 A	31-12-1991	DE 69130801 D	04-03-1999
		DE 69130801 T	08-07-1999
		EP 0543927 A	02-06-1993
		JP 6500440 T	13-01-1994
		WO 9203874 A	05-03-1992
US 5581213 A	03-12-1996	NONE	
US 5630214 A	13-05-1997	NONE	
US 5423076 A	06-06-1995	NONE	
US 5311318 A	10-05-1994	CA 2104182 A,C	18-02-1994

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Abstract of CN101097304

An active element array mother base board fits for cutting several active element array base boards, the active element mother base board includes a base board, a plurality of active element arrays and a plurality of outer circuit pads. Thereinto, the base board is provided with a plurality of preset areas, each preset area respectively defines a position for an active element array base board. Besides, the active element arrays and outer circuit pads are distributed in the preset areas, and within the preset area, the outer circuit pad and signal wire of the active element array are electrically connected. Especially, at least outer circuit pad in one preset area is electrically connected with outer circuit pad in the other preset area.

[19] 中华人民共和国国家知识产权局

[51] Int. Cl.
G02F 1/133 (2006.01)
G02F 1/136 (2006.01)

[12] 发明专利申请公布说明书

[21] 申请号 200610099789.6

[43] 公开日 2008 年 1 月 2 日

[11] 公开号 CN 101097304A

[22] 申请日 2006.6.27
[21] 申请号 200610099789.6
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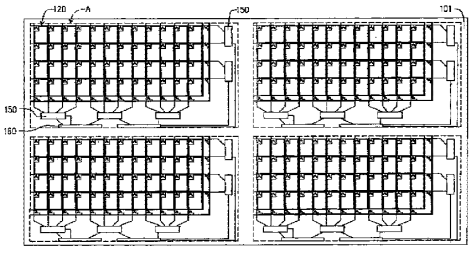
权利要求书 2 页 说明书 8 页 附图 6 页

[54] 发明名称

主动元件阵列母基板

[57] 摘要

一种主动元件阵列母基板，其适于分割出多片主动元件阵列基板，主动元件阵列母基板包括一基板、多组主动元件阵列与多个外部电路焊盘(pad)。其中，基板具有多个预定区，此预定区分别定义出主动元件阵列基板的所在位置。 此外，上述主动元件阵列与外部电路焊盘均分别配置于预定区内，且在各预定区内，外部电路焊盘与主动元件阵列的信号线电性连接。 特别地是，至少两预定区内的外部电路焊盘彼此电性相连。



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1.一种主动元件阵列母基板，适于分割出多片主动元件阵列基板，其特征在于，所述主动元件阵列母基板包括：

一基板，具有多个预定区，其中所述预定区分别定义出所述主动元件阵列基板的所在位置；

多组主动元件阵列，分别配置于所述预定区内，其中各组主动元件阵列具有多条信号线；以及

多个外部电路焊盘，配置于所述预定区内，且在各所述预定区内，所述信号线是电性连接至所述外部电路焊盘，

其中至少两预定区内的所述外部电路焊盘彼此电性相连。

2.如权利要求 1 所述的主动元件阵列母基板，其特征在于，在各所述预定区内还包括：

多个驱动芯片焊盘，分别与所述主动元件阵列之所述信号线电性连接；以及

一内部静电放电保护环，电性连接于所述驱动芯片焊盘与所述信号线之间，且所述内部静电放电保护环电性连接至所述外部电路焊盘其中之一。

3.如权利要求 2 所述的主动元件阵列母基板，其特征在于，所述内部静电放电保护环包括：

多个保护元件，分别电性连接于所述信号线与所述驱动芯片焊盘之间；以及

一连接导线，串接所述保护元件，并电性连接至所述外部电路焊盘其中之一。

4.如权利要求 2 所述的主动元件阵列母基板，其特征在于，还包括一引线，配置于所述基板上的所述预定区外，其中各所述预定区内的所述外部电路焊盘均电性连接至所述引线，而使所述主动元件阵列通过所述引线而彼此电性相连。

5.如权利要求 4 所述的主动元件阵列母基板，其特征在于，还包括多个开关元件，电性连接于所述外部电路焊盘与所述引线之间。

6.如权利要求 5 所述的主动元件阵列母基板，其特征在于，所述开关元件包括薄膜晶体管或二极管至少其中之一。

7.如权利要求 4 所述的主动元件阵列母基板，其特征在于，所述外部电路焊盘包括多个第一焊盘与多个第二焊盘，且在各所述预定区内的所述信号线包括：

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多条数据线，分别电性连接至所述预定区内的所述第一焊盘，且所述第一焊盘与所述数据线为同一膜层；以及

多条扫描线，分别电性连接至所述预定区内的所述第二焊盘，且所述第二焊盘与所述扫描线为同一膜层。

8.如权利要求 7 所述的主动元件阵列母基板，其特征在于，所述引线包括一第一导电层与一第二导电层，所述第二导电层位于所述第一导电层上方，且所述第一焊盘电性连接至所述第一导电层，而所述第二焊盘电性连接至所述第二导电层。

9 如权利要求 7 所述的主动元件阵列母基板，其特征在于，所述引线为一透明导电层，且所述第一焊盘与所述第二焊盘均电性连接至所述透明导电层。

10.如权利要求 9 所述的主动元件阵列母基板，其特征在于，所述透明导电层的材料包括铟锡氧化物或铟锌氧化物。

11.如权利要求 1 所述的主动元件阵列母基板，其特征在于，其在各所述预定区内还包括一总线，且在各所述预定区内，所述主动元件阵列的所述信号线包括多条共用配线， 所述共用配线通过所述总线而与所述外部电路焊盘电性连接，而位于不同预定区内的总线通过所述外部电路焊盘至少其中之一而彼此电性连接。

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主动元件阵列母基板

技术领域

本发明有关于一种主动元件阵列母基板，且特别有关于一种具有静电放电（electro static discharge，ESD）防护功效的主动元件阵列母基板。

背景技术

在液晶显示器的制造过程中，操作人员、机台或检测仪器都可能带有静电，而上述的带电体（操作人员、机台或检测仪器）接触到液晶显示面板时，可能导致液晶显示面板内的元件以及电路遭受静电放电（electro static discharge）破坏。因此，一般都会在液晶显示面板的非显示区中设计静电放电保护电路。以主动矩阵液晶显示面板来说，其通常是在制造主动元件阵列的过程中一并将静电放电保护电路形成于基板上，并且令主动元件阵列与这些静电放电保护电路电性连接。如此一来，当液晶显示面板遭受到静电放电的冲击时，会触发静电放电保护电路的保护机制，因而通过静电放电保护电路将静电分散、减弱，以避免静电直接导入显示区内部的元件及电路而造成损毁。

图 1 为现有的主动元件阵列基板示意图。图 1 中所示的主动元件阵列基板 100 包括形成于基板 110 上的主动元件阵列 120、多个驱动芯片焊盘（pad）150 以及静电放电保护电路 160。其中，基板 110 具有一显示区 112 与一周边电路区 114，主动元件阵列 120 配置于显示区 112 内，并包括多个主动元件 122、多个象素电极 124、多条扫描线 130 与多条数据线 140。详细地说，扫描线 130 与数据线 140 适于驱动其所对应的主动元件 122，以通过主动元件 122 来驱动象素电极 124。而且，主动元件阵列 120 通过扫描配线 130 与数据配线 140 而电性连接至驱动芯片焊盘 150，并通过驱动芯片焊盘 150 而与外部的驱动电路（未示出）电性连接。

在目前的平面显示器中，常见的静电放电保护电路 160 包括内部静电放电保护环 162 与外部静电放电保护环 164。其中，内部静电放电保护环 162 电性连接于驱动芯片焊盘 150 与主动元件阵列 120 之间。当静电放电现象发生于主动元件阵列 120 中时，静电会开启内部静电放电保护环 162，并通过内部静电放电保护环 162

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而将静电分散。此外，为避免在驱动芯片焊盘 150 与外部驱动电路（未示出）之间发生静电破坏，外部静电放电保护环 164 是配置于基板 110 外围，并电性连接于驱动芯片焊盘 150。同理，当静电放电现象发生于任一驱动芯片焊盘 150 时，静电会开启外部静电放电保护环 164，并藉此而将静电分散。

图 2 为现有的一种主动元件阵列母基板的示意图。请参照图 2，一般来说，上述主动元件阵列基板 100 的制造方式是先在大片的玻璃基板 101 上定义出多个预定区 A，之后在这些预定区 A 内形成上述的主动元件阵列 120 以及相关电路，最后再对大片的玻璃基板 101 进行切割，以切出多片主动元件阵列基板。在经济效益的考虑下，各个预定区 A 之间的距离会尽可能的缩小，以增加玻璃基板 101 的利用率。因此，近年来便发展出一种 COG（Chip On Glass）技术，其是直接将驱动电路芯片（未示出）贴附在玻璃基板 101 上的驱动芯片焊盘 150，并通过驱动芯片焊盘 150 而与可挠性电路板（未示出）电性连接，以节省空间。

然而，若在 COG 的技术中置入外部静电放电保护环 164，则会对玻璃基板 101 上的走线造成线路干涉的问题。而且，当各个预定区 A 之间的距离变小后，玻璃基板 101 上无足够的面积配置外部静电放电保护环 164。也就是说，传统的 COG 技术中，在玻璃基板 101 上的主动元件阵列 120 仅能靠内部静电放电保护环来分散静电。如此一来，将使各主动元件阵列 120 的抗静电放电破坏的能力大幅降低，进而导致主动元件阵列 120 中的元件与电路面临极高的静电放电破坏的风险。

发明内容

有鉴于此，本发明的目的在于提供一种主动元件阵列母基板，以避免主动元件阵列母基板上各主动元件阵列遭受到静电放电的破坏。

为达上述或其他目的，本发明提出一种主动元件阵列母基板，其适于分割出多片主动元件阵列基板，主动元件阵列母基板包括一基板、多组主动元件阵列与多个外部电路焊盘。其中，基板具有多个预定区，此预定区分别定义出主动元件阵列基板所在位置。此外，上述多组主动元件阵列分别配置于预定区内，且各组主动元件阵列均具有多条信号线。外部电路焊盘也配置于预定区内，且在各预定区内，上述信号线分别与外部电路焊盘电性连接。特别地，至少两预定区内的外部电路焊盘彼此电性相连。

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在本发明的一实施例中，上述主动元件阵列母基板在各预定区内还包括多个驱动芯片焊盘与一内部静电放电保护环。其中，这些驱动芯片焊盘是与主动元件阵列的信号线电性连接，而内部静电放电保护环电性连接于这些驱动芯片焊盘与信号线之间，且内部静电放电保护环还与此预定区内的至少一外部电路焊盘电性连接。

在本发明的一实施例中，上述内部静电放电保护环包括多个保护元件与一连接导线。其中，这些保护元件分别电性连接于信号线与驱动芯片焊盘之间，且这些保护元件是通过此连接导线而彼此电性连接。此外，此连接导线还电性连接至此预定区内的一外部电路焊盘。

在本发明的一实施例中，上述主动元件阵列母基板还包括一引线，其配置于基板上，且位于预定区外。而且，上述外部电路焊盘均电性连接至此引线，使各主动元件阵列通过此引线而彼此电性相连。

在本发明的一实施例中，上述主动元件阵列母基板还包括多个开关元件，分别电性连接于这些外部电路焊盘与上述引线之间。其中，这些开关元件可以是薄膜晶体管、二极管或其组合。

在本发明的一实施例中，上述外部电路焊盘包括多个第一焊盘与多个第二焊盘，且在各预定区内的信号线包括多条数据线与多条扫描线。其中，扫描线分别电性连接至其所在的预定区内的这些第一焊盘，且这些第一焊盘与这些扫描线为同一膜层。这些数据线则是分别电性连接至第二焊盘，且这些第二焊盘与这些数据线为同一膜层。

在本发明的一实施例中，上述引线可以由第一导电层与第二导电层所构成，且第二导电层位于第一导电层上方。此外，上述第一焊盘可以电性连接至第一导电层，第二焊盘则可以电性连接至第二导电层。

在本发明的一实施例中，上述引线可以是一透明导电层，且上述第一焊盘与第二焊盘均电性连接至此透明导电层。

在本发明的一实施例中，上述透明导电层的材料包括铟锡氧化物或铟锌氧化物。

在本发明的一实施例中，上述主动元件阵列母基板在各预定区内还包括一总线，且所述主动元件阵列基板的信号线包括多条共用配线。其中这些共用配线通过此总线而与上述外部电路焊盘电性连接，且位于不同预定区内的总线通过这些外部

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电路焊盘至少其中之一而彼此电性连接。

本发明的主动元件阵列母基板是令至少两预定区内的焊盘彼此电性连接，而使得不同预定区内的线路彼此电性连接。因此，当静电放电现象发生于某一主动元件阵列中时，静电会被进一步分散至整个母基板上，以减弱静电对单一主动元件阵列所造成的冲击。

为让本发明的上述和其他目的、特征和优点能更明显易懂，下文特举较佳实施例，并配合附图，作详细说明如下。

附图说明

图 1 是现有的主动元件阵列基板示意图。

图 2 是现有的一种主动元件阵列母基板示意图。

图 3 是本发明第一实施例中主动元件阵列母基板示意图。

图 4 是本发明第二实施例中主动元件阵列母基板示意图。

图 5A 是本发明一实施例中图 3 的主动元件阵列母基板沿 I-I’ 线的剖面示意图。

图 5B 是本发明另一实施例中图 3 的主动元件阵列母基板沿 I-I’ 线的剖面示意图。

图 6 是本发明第三实施例中主动元件阵列母基板示意图。

具体实施方式

图 3 是本发明第一实施例中主动元件阵列母基板示意图。请参考图 3，主动元件阵列母基板 300 适于被分割为多片主动元件阵列基板。具体来说，此主动元件阵列母基板 300 包括一基板 310、多组主动元件阵列 320 与多个外部电路焊盘 350。其中，基板 310 可以具有预定区 A、B、C 与 D，而各组主动元件阵列 320 即是分别配置于预定区 A、B、C 与 D 内。也就是说，本实施例的主动元件阵列母基板 300 在后续制程中可以被切割成四片主动元件阵列基板。当然，本发明并无意局限基板 310 上的预定区数目，这可以视欲制作出的主动元件阵列基板的尺寸与片数而作适当调整。

请继续参照图 3，各组主动元件阵列 320 均具有多条信号线 322，且熟习此技

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艺者应该知道，这些信号线 322 包括扫描线 321 与数据线 323。此外，预定区 A、B、C 与 D 内均配置有多个外部电路焊盘 350，且在各预定区 A、B、C 与 D 内，外部电路焊盘 350 与其所对应的主动元件阵列 320 互相电性连接。由图 3 可清楚得知，主动元件阵列 320 是通过扫描线 321 或数据配线 323 而电性连接至外部电路焊盘 350。在此，外部电路焊盘 350 可以用来与可挠性电路板(flexible printed circuit, FPC)（未示出）电性连接。

特别的是，主动元件阵列母基板 300 上至少两预定区内的外部电路焊盘 350 彼此电性连接。如此一来，当任一预定区内的主动元件阵列 320 中发生静电放电的现象时，此静电会被导散至整个基板 310 上，进而避免基板 310 上的任何电子元件遭受到静电放电的破坏。

详细来说，主动元件阵列母基板 300 在各预定区 A、B、C 与 D 中还包括多个内部静电放电保护环 360 与多个驱动芯片焊盘 370。其中，驱动芯片焊盘 370 是电性连接于信号线 322 与外部电路焊盘 350 之间。换言之，主动元件阵列 320 的信号线 322 是先电性连接至驱动芯片焊盘 370，再经由驱动芯片焊盘 370 而与外部电路焊盘 350 电性连接。其中，后续欲贴附于基板 310 上的驱动芯片（未示出）即是贴在这些驱动芯片焊盘 370 上。

另外，在各预定区内，内部静电放电保护环 360 是电性连接于信号线 322 与驱动芯片焊盘 370 之间。而且，内部静电放电保护环 360 可以由多个保护元件 362 与连接导线 364 所构成，其中保护元件 362 可以是薄膜晶体管、二极管或是这些元件的组合。连接导线 364 则是将这些保护元件 362 串接起来，而且连接导线 364 更进一步与至少一外部电路焊盘 350 电性连接。如此一来，当主动元件阵列 320 中发生静电放电现象时，静电荷可以经由信号线 322 往内部静电放电保护环 360 移动，并开启保护元件 362，进而通过连接导线 364 而分散至外部电路焊盘 350。此时，由于本发明的主动元件阵列母基板 300 上不同预定区内的外部电路焊盘 350 彼此电性连接，因此静电荷会再从外部电路焊盘 350 散逸至其他预定区内，以避免静电荷过于集中而损坏主动元件阵列 320。

在本实施例中，主动元件阵列母基板 300 可以利用一引线 380 来电性连接不同预定区内的外部电路焊盘 350，进而使位于不同预定区 A、B、C 与 D 内的主动元件阵列 320 通过引线 380 而彼此电性相连。其中，引线 380 配置于基板 210 上，且

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位于预定区 A、B、C 与 D 之外。值得一提的是，引线 380 可以与外部电路焊盘 350、扫描线 321 或数据线 323 一并形成。当然，引线 380 也可以是在主动元件阵列母基板 200 的其他制程中所遗留下来的金属线。换言之，本发明可以在不额外增加制程的情况下形成引线 380。

此外，本发明当然也可以在各外部电路焊盘 350 与引线 380 之间配置有开关元件 390，如图 4 所示，其中开关元件 390 可以是薄膜晶体管、二极管或这些元件的组合。

请再次参照图 3，当主动元件阵列母基板 300 上发生静电放电现象时，静电所带的高电压会启动内部静电放电保护环 360 的保护机制，因此静电荷会通过连接导线 364 分散并传递至外部电路焊盘 350，并通过引线 380 而分散至基板 310 上的其他预定区内。换言之，静电在开启保护元件 362 之后，会消耗静电的部分能量，且静电会再通过引线 380 而散逸至整个基板 310，因而减低静电放电破坏的能力。

一般而言，在较大尺寸的主动元件阵列母基板 300 中，上述效果会更加显著，这是因为较大尺寸的主动元件阵列母基板 300 会具有较长且范围较大的静电散逸路径，静电的能量会在传导的过程中被消耗，且静电会被分散至较大的范围中，而造成静电放电破坏的能力大幅衰减。因此，本发明可使不适合制作现有外部静电放电保护环 164（如图 1 所示）的主动元件阵列母基板 300，仍然具有良好的静电放电防护功效。而且在实务上，由于本实施例的主动元件阵列母基板 300 上并没有图 1 的外部静电放电保护环 164，所以无须进行额外的切割制程来分离外部静电放电保护环，因此不必担心磨边导角的限制。

另一方面，由于本实施例的主动元件阵列母基板 300 并非以外部静电放电保护环来提供静电散逸路径，因此可以避免外部静电放电保护环与基板 310 上的线路相互干涉的问题。

在本实施例中，外部电路焊盘 350 包括多个第一焊盘 352 与多个第二焊盘 354，其中第一焊盘 352 可以用以承载欲与扫描线 321 电性连接的可挠性电路板（未示出），第二焊盘 354 可以用以承载欲与数据线 323 电性连接的可挠性电路板（未示出）。换言之，扫描线 321 是电性连接至第一焊盘 352，数据线 323 则是电性连接至第二焊盘 354。而且，扫描线 321 可以与第一焊盘 352 同层，数据线 323 则可以与第二焊盘 354 同层。

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承上所述，熟习此技艺者应该知道，扫描线 321 与数据线 323 分属不同膜层，也就是说，第一焊盘 352 与第二焊盘 354 也分属不同膜层。以下将举例说明在此种情况下，如何令第一焊盘 352 与第二焊盘 354 均与引线 380 电性连接。

图 5A 为本发明一实施例中图 3 的主动元件阵列母基板沿 I-I' 线的剖面示意图。请参照图 5A，在此实施例中，引线 380 是由第一导电层 382 与第二导电层 384 所构成，其中第二导电层 384 位于第一导电层 382 上方，且第一焊盘 352 是通过导线 352a 电性连接至第一导电层 382，第二焊盘 354 则是通过导线 354a 电性连接至第二导电层 384。

图 5B 为本发明另一实施例中图 3 的主动元件阵列母基板沿 I-I' 线的剖面示意图。请参照图 5B，在此实施例中，引线 380 为单一膜层，且其是同时与分属不同层的第一焊盘 352 与第二焊盘 354 电性连接。详细来说，引线 380 可以位于第一焊盘 352 与第二焊盘 354 上方的膜层，且其可以直接覆盖于由第二焊盘 354 所延伸出的导线 354a 上，并通过位于第一焊盘 352 与第二焊盘 354 间的介电层 327 中的接触窗开口 329 而与第一焊盘 352 所延伸出的导线 352a 电性连接。举例来说，引线 380 可以是一透明导电层，且其可以是与主动元件阵列 320 中的象素电极 324（如图 3 所示）在同一道光罩制程下一并形成。换言之，引线 380 的材质可以为铟锡氧化物（ITO）或铟锌氧化物（IZO）。

请同时参照图 3 及图 5B，若静电放电现象发生于主动元件阵列 320 的扫描线 321 上，静电荷可经由第一焊盘 352 传递至引线 380，并通过引线 380 而分散至第二焊盘 354，进而使数据线 323 与扫描线 321 具有相同电位。同样地，若静电放电现象发生于主动元件阵列 320 的数据线 323 上，静电荷可经由第二焊盘 354 传递至引线 380，并通过引线 380 而分散至第一焊盘 352，进而使扫描线 321 与数据线 323 具有相同电位。如此一来，可以有效降低静电放电对主动元件阵列母基板 300 所造成的冲击，进而达到保护主动元件阵列母基板 300 的目的。

值得注意的是，当基板 310 上的各组主动元件阵列 320 的排列过于紧密，而未有足够的空间配置图 3 的引线 380 时，本发明仍可以其他方法来使不同预定区内的外部电路焊盘 350 彼此电性连接，以下将举例说明之。

图 6 是本发明第三实施例的主动元件阵列母基板示意图。为了凸显本实施例的特征，在图 6 中省略了部分元件的绘制，并将重点放在不同预定区内线路彼此之

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间的连接方式。请参考图 6，主动元件阵列母基板 600 在各预定区内还包括一总线 610，且各组主动元件阵列 320 的信号线除了包括图 3 的扫描线 321 与数据线 323 之外，也包括多条共用配线 620，而各预定区内的总线 610 即是与这些共用配线 620 电性连接，用以将外部所提供的信号传输至这些共用配线 620。由图 6 可清楚得知，总线 610 是环绕在主动元件阵列 320 的周围，并且与外部电路焊盘 350 电性连接。更特别的是，本实施例的外部电路焊盘 350 是电性连接于两预定区的总线 620 之间，因此当静电放电现象发生于主动元件阵列母基板 600 的某预定区内的主动元件阵列 320 时，静电会从共用配线 620 经总线 610 而传导至外部电路焊盘 350，并进一步通过外部电路焊盘 350 而散逸至其他预定区。这样一来，便可以有效降低并分散静电放电对主动元件阵列母基板 600 所造成的冲击，进而达到保护主动元件阵列母基板 600 的目的。

需要一提的是，虽然图 6 仅将位于预定区 A 与预定区 C 中的总线 610 通过外部电路焊盘 350 而彼此电性连接，但熟习此技艺者应该知道，当然实际上还可以将其他预定区 B 或 D 的总线 610 一并连接在一起，在此并不作特别限定。

综上所述，本发明的主动元件阵列母基板至少具有下列优点：

一、本发明将主动元件阵列母基板上位于不同预定区内的主动元件阵列电性连接，以大幅增加静电的散逸路径以及范围。这样一来，当静电放电现象发生时，静电会被充分地分散，进而使静电的破坏能力大幅降低，进而达到保护各主动元件阵列的效果。而且，外部电路焊盘在与可挠性电路板接合的制程中也可免于遭受静电放电破坏。

二、本发明的主动元件阵列母基板可以在不制作外部静电放电保护环的情况下，仍然具有良好的静电放电防护的功效。因此，本发明适用于以 COG 技术来制作主动元件阵列基板的制程中。

三、本发明的主动元件阵列母基板上的引线可以在原有的制程中形成，且主动元件阵列母基板上毋须制作外部静电放电保护环即可具有静电放电防护功效。因此，本发明的主动元件阵列母基板具有较低的制造成本。

虽然本发明已以较佳实施例揭示如上，然其并非用以限定本发明，任何熟习此技艺者，在不脱离本发明的精神和范围内，当可作些许更动与润饰，因此本发明的保护范围当视权利要求所界定者为准。

Micron Ex. 1002, p. 293
Micron v. YMTC
IPR2025-00118

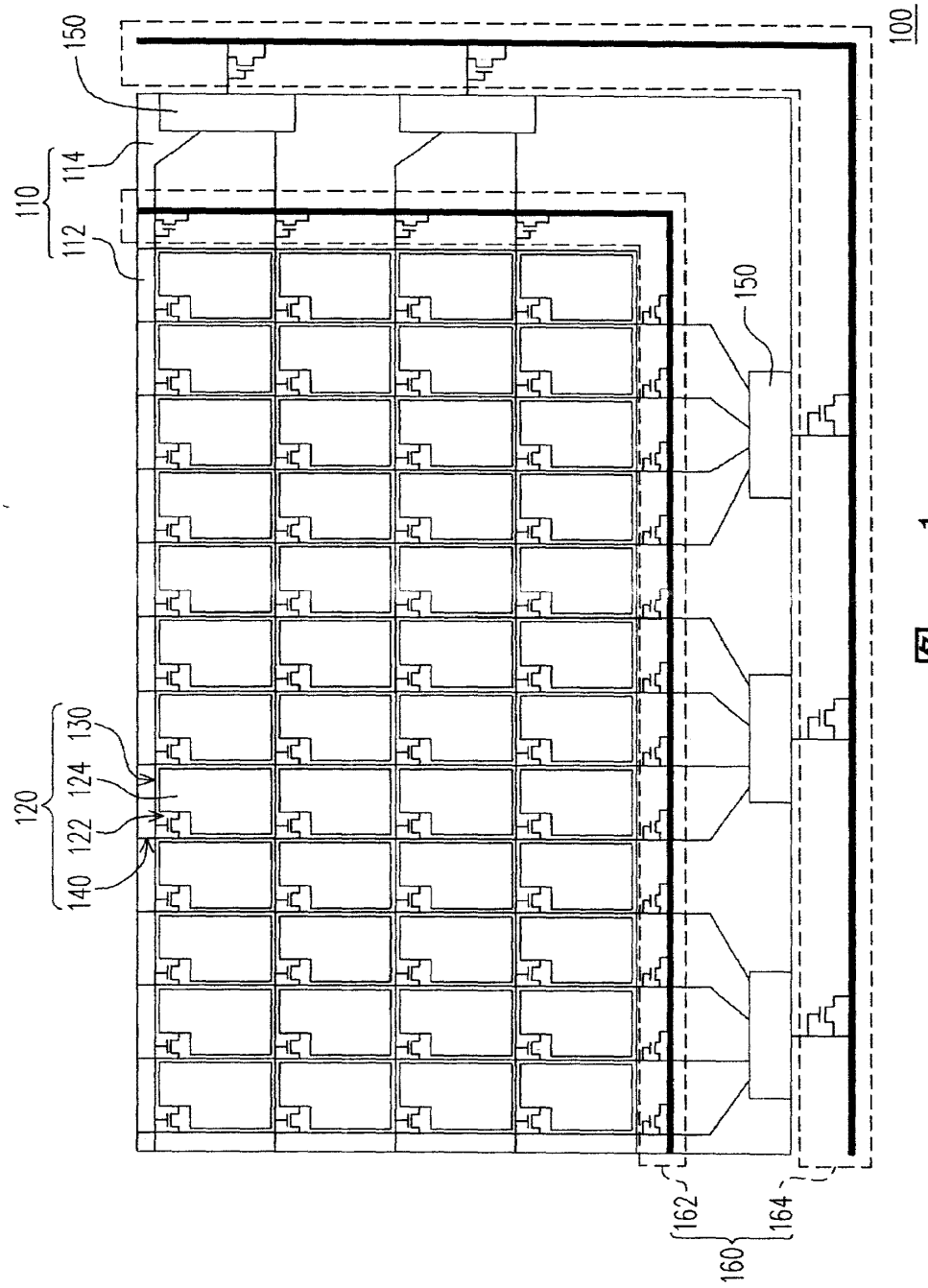


图 1

Micron Ex. 1002, p. 294
Micron v. YMTC
IPR2025-00118

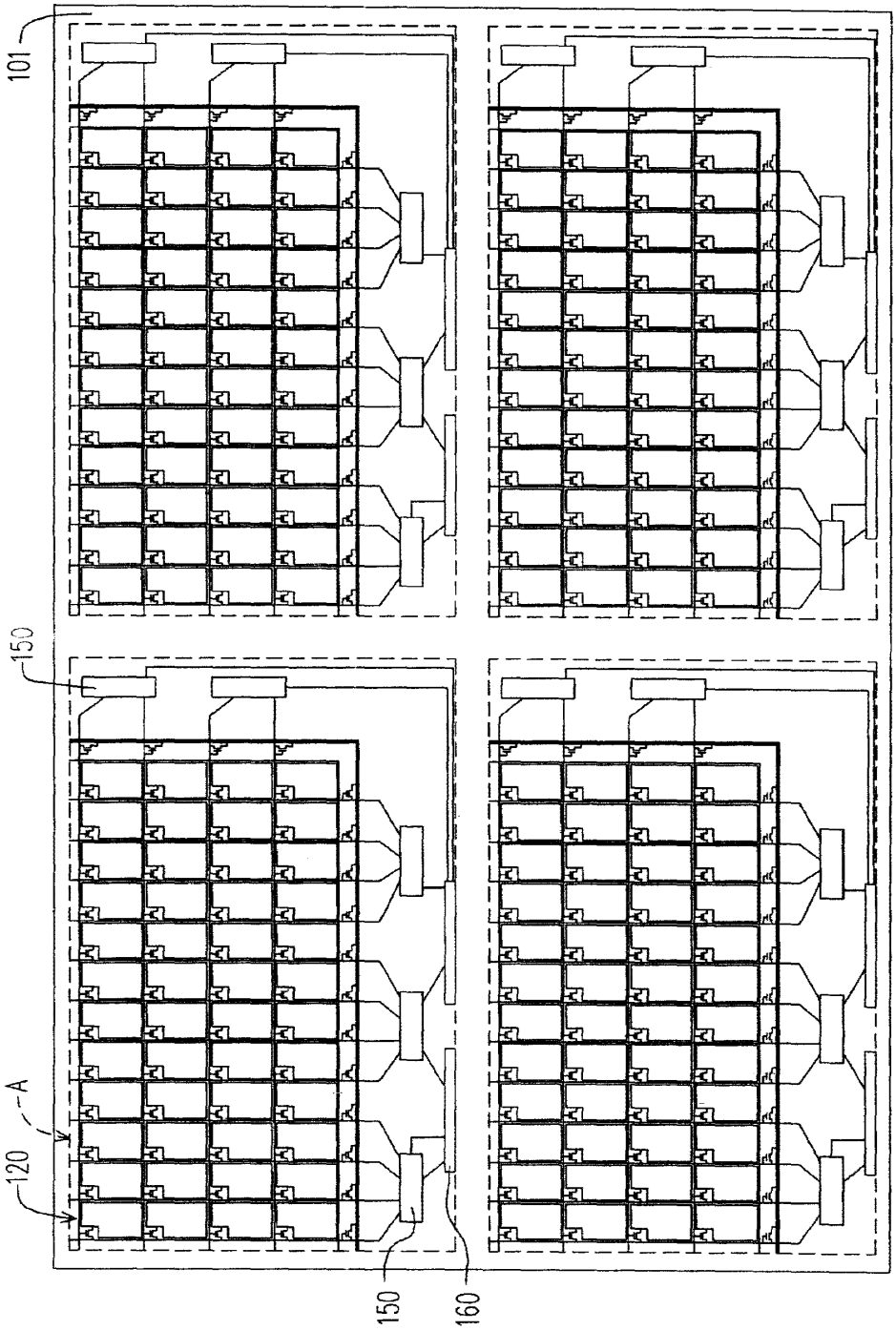


图 2

Micron Ex. 1002, p. 295
Micron v. YMTC
IPR2025-00118

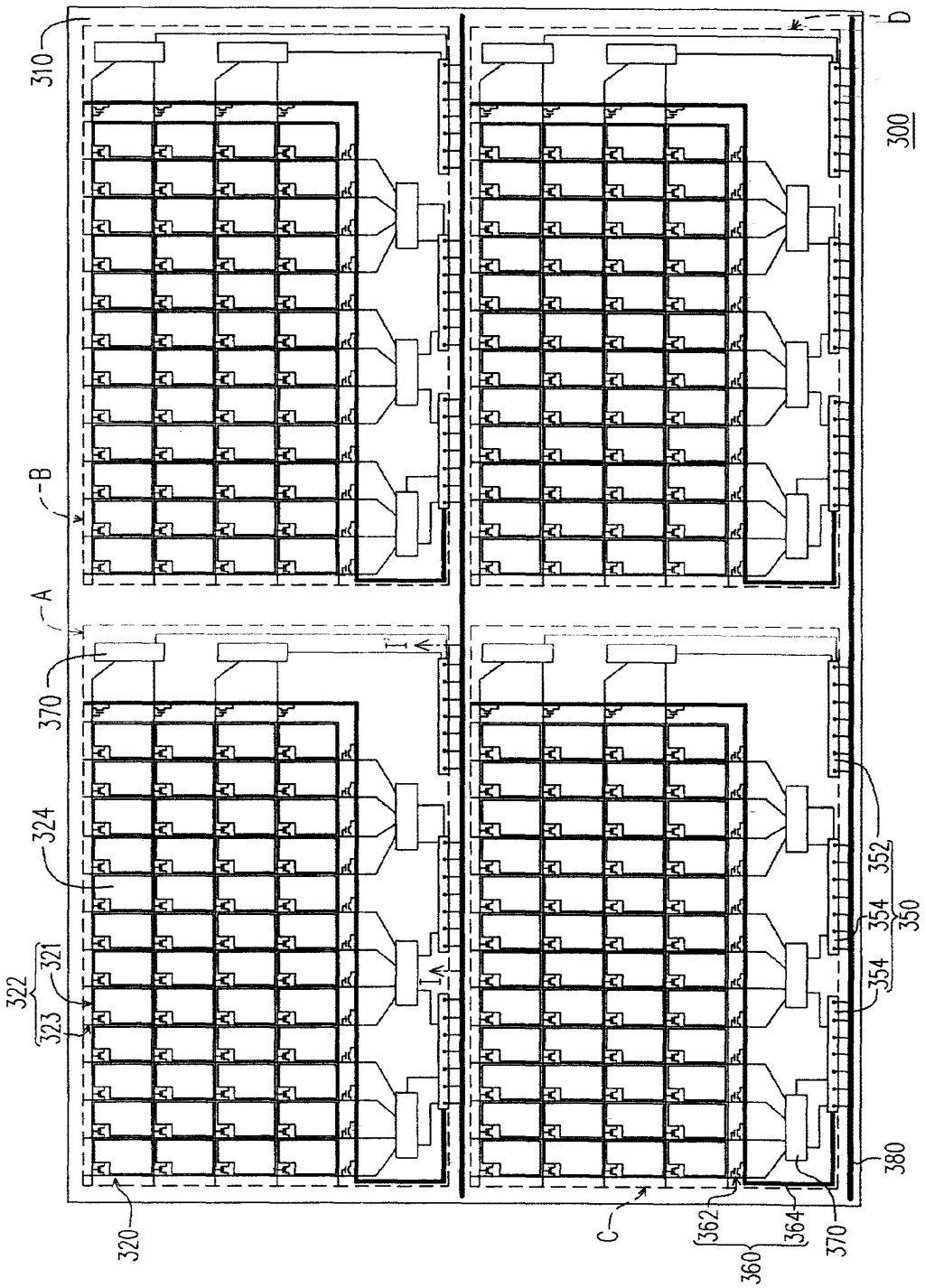


图 3

Micron Ex. 1002, p. 296
Micron v. YMTC
IPR2025-00118

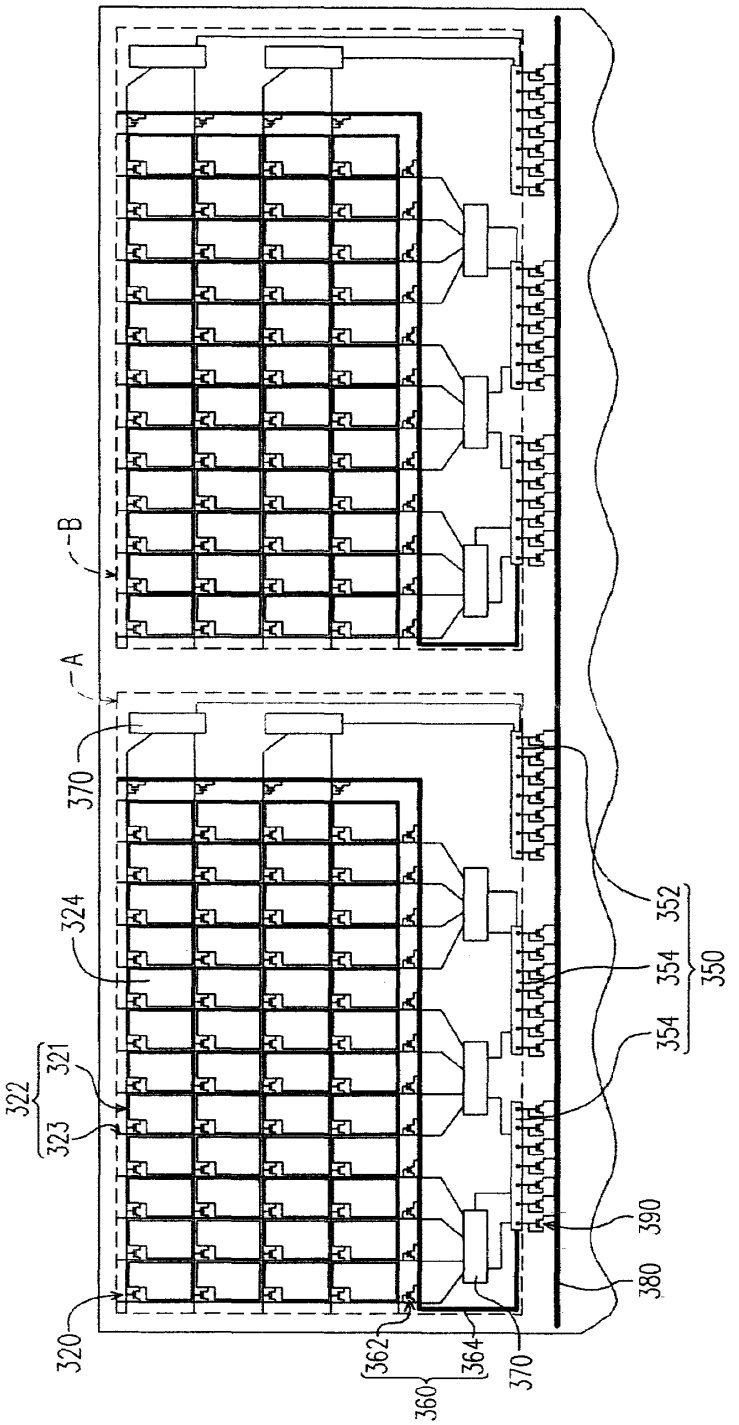


图 4

Micron Ex. 1002, p. 297
Micron v. YMTC
IPR2025-00118

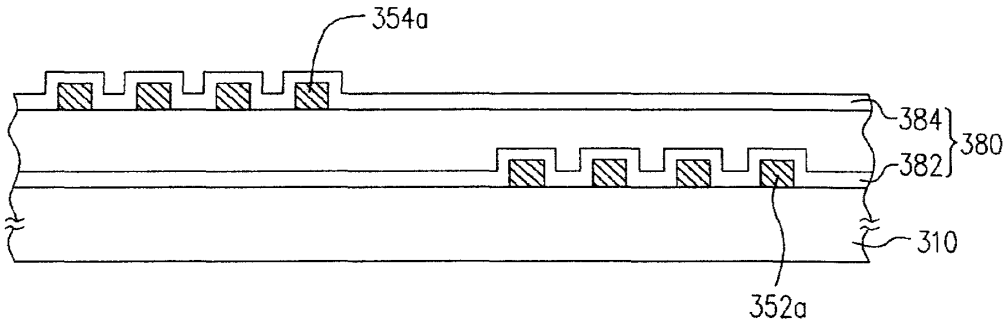


图 5A

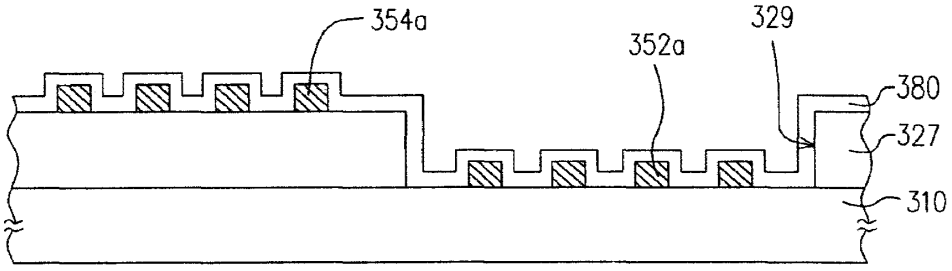


图 5B

Micron Ex. 1002, p. 298
Micron v. YMTC
IPR2025-00118

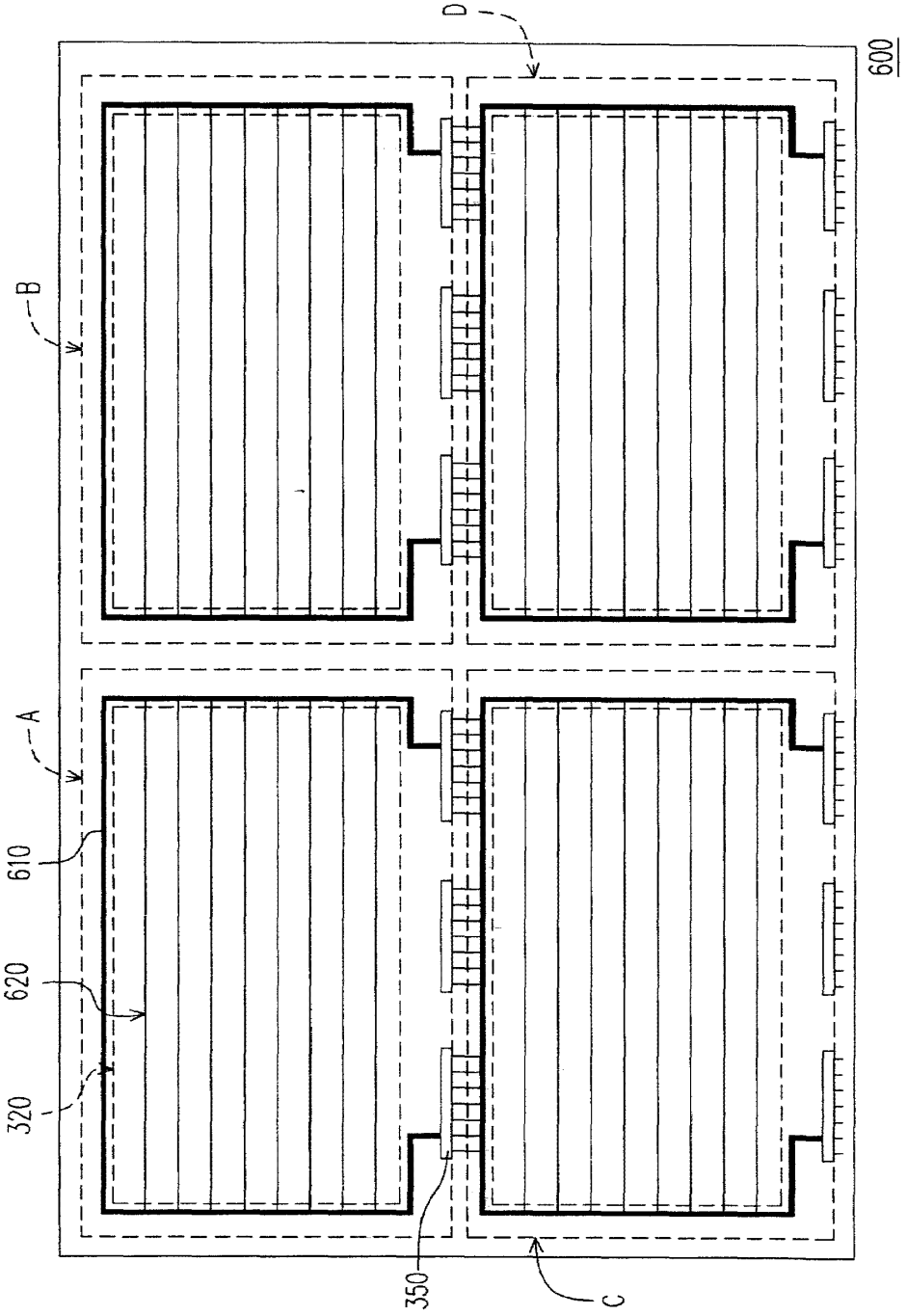


图 6

Micron Ex. 1002, p. 299
Micron v. YMTC
IPR2025-00118

Electronic Patent Application Fee Transmittal

Application Number:	16207183
Filing Date:	02-Dec-2018
Title of Invention:	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method
First Named Inventor/Applicant Name:	Zhiguo Li
Filer:	Roger Gwan-Jye Chen/Anna Lu
Attorney Docket Number:	YMTP0079USA3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
		Total in USD ($)		**260**

Electronic Acknowledgement Receipt

EFS ID:	40848269
Application Number:	16207183
International Application Number:	
Confirmation Number:	2734
Title of Invention:	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method
First Named Inventor/Applicant Name:	Zhiguo Li
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Anna Lu
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	YMTP0079USA3
Receipt Date:	15-OCT-2020
Filing Date:	02-DEC-2018
Time Stamp:	03:10:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$260
RAM confirmation Number	E20200E411060434
Deposit Account	503105
Authorized User	Anna Lu
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	3987680.PDF	26836 9abdef8ba2b0bc9c3b053454ae7810f38a16d779	no	3
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
2	Foreign Reference	CN_101221629.PDF	688386 8462957dbb3b14e51bb73c392ce5613304be7323	no	16
Warnings:					
Information:					
3	Foreign Reference	WO_0028664.PDF	477046 df524c91d6eb7a633240c02320562c64d1f0cc10	no	12
Warnings:					
Information:					
4	Foreign Reference	CN_101097304.PDF	1045894 06f87d7cc8d824453bc3caf780d3a7700006deb8	no	18
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	30472 2a539733f167df472744bab8c5cb9ccfc912eb97	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2268634		

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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/207,183	12/02/2018	Zhiguo Li	YMTP0079USA3	2734

27765 7590 11/13/2020

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

EXAMINER	
CLARK, SHEILA V	

ART UNIT	PAPER NUMBER
2891	

NOTIFICATION DATE	DELIVERY MODE
11/13/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

Micron Ex. 1002, p. 305
Micron v. YMTC
IPR2025-00118

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Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR/ PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
16/207,183	12/02/2018	Li, Zhiguo	YMTP0079USA3

	EXAMINER	
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION 5F., NO.389, FUHE RD., YONGHE DIST. NEW TAIPEI CITY,	S. V CLARK	
	ART UNIT	PAPER
	2891	20201107

DATE MAILED: _____

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The IDS filed 10/15/2020 has been initialed and is attached.

/S. V. CLARK/
Primary Examiner, Art Unit 2891

PTO-90C (Rev.04-03)

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16207183
	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2891
	Examiner Name	CLARK, SHEILA V
	Attorney Docket Number	YMTP0079USA3

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6078068	A	2000-06-20	Tamura	
	2	6770963	B1	2004-08-03	Wu	
	3	5365091	A	1994-11-15	Yamagishi	
	4	5347150	A	1994-09-13	Sakai	

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

.

FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.V.C/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16207183
	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2891
	Examiner Name	CLARK, SHEILA V
	Attorney Docket Number	YMTP0079USA3

	1	0028664	WO	A3	2001-07-26			
	2	101097304	CN	A	2008-01-02			Abstract
	3	101221629	CN	A	2008-07-16			Abstract

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1		

EXAMINER SIGNATURE

Examiner Signature	/S. V. CLARK/	Date Considered	11/07/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.V.C/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16207183
	Filing Date	2018-12-02
	First Named Inventor	Zhiguo Li
	Art Unit	2891
	Examiner Name	CLARK, SHEILA V
	Attorney Docket Number	YMTP0079USA3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Roger Chen/	Date (YYYY-MM-DD)	2020-10-14
Name/Print	Roger Chen	Registration Number	67314

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.V.C/

PART B – FEE(S) TRANSMITTAL

Complete and send this form, together with the applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

By fax, send to: (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27765 7590 09/22/2020

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., No.389, Fuhe Rd., Yonghe Dist.,
New Taipei City,
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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Connie Chen	(Typed or printed name)
/Connie Chen/	(Signature)
11/17/2020	(Date)

APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
16/207,183	12/02/2018	Zhiguo Li	YMTP0079USA3	2734

TITLE OF INVENTION: Integrated Circuit Electrostatic Discharge Bus Structure and Related Method

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	12/22/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
CLARK, SHEILA V	2891	257-691000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363)

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Winston Hsu
2.
3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Yangtze Memory Technologies Co., Ltd.

(B) RESIDENCE: (CITY and STATE or COUNTRY): Wuhan City, Hubei Province, P.R.C.

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. Fees Submitted: ☑ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment (*Please first reapply any previously paid fee shown above*):

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☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 50-3105

5. Change of Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29. NOTE: Absent a valid Certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27. NOTE: If the application was previously under micro entity status, checking this box will be taken as a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status. NOTE: Checking this box will be taken as a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Winston Hsu/ Date 11/16/2020

Typed or printed name Winston Hsu Registration No. 41526

Micron Ex. 1002, p. 310
Micron v. YMTC
IPR2025-00118

Electronic Patent Application Fee Transmittal

Application Number:	16207183
Filing Date:	02-Dec-2018
Title of Invention:	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method
First Named Inventor/Applicant Name:	Zhiguo Li
Filer:	Winston Hsu/Connie Chen
Attorney Docket Number:	YMTP0079USA3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1000**

Electronic Acknowledgement Receipt

EFS ID:	41138711
Application Number:	16207183
International Application Number:	
Confirmation Number:	2734
Title of Invention:	Integrated Circuit Electrostatic Discharge Bus Structure and Related Method
First Named Inventor/Applicant Name:	Zhiguo Li
Customer Number:	27765
Filer:	Winston Hsu/connie chen
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	YMTP0079USA3
Receipt Date:	17-NOV-2020
Filing Date:	02-DEC-2018
Time Stamp:	01:35:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1000
RAM confirmation Number	E2020AG236053091
Deposit Account	503105
Authorized User	connie chen
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	4023588.PDF	762558 aa59cfb1495e649d4b1a43f778ab5994c96814c6	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30082 cf65f84a30515b448127ccdd7e280f91ce53c391	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	792640		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/207,183	12/29/2020	10879164	YMTP0079USA3	2734

27765 7590 12/09/2020

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 30 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Yangtze Memory Technologies Co., Ltd., Wuhan City, CHINA;
Zhiguo Li, Wuhan City, CHINA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

Micron Ex. 1002, p. 315
Micron v. YMTC
IPR2025-00118