

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00118
U.S. Patent No. 10,879,164

**DECLARATION OF DR. DANIEL FOTY IN SUPPORT OF PETITION
FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,879,164**

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I. INTRODUCTION

1. I have been retained by counsel for Micron Technology, Inc. (“Micron” or “Petitioner”) in the above-captioned matter as an independent consultant to offer opinions regarding the patentability claims 1-14 (the “Challenged Claims”) of U.S. Patent No. 10,879,164 (the “’164 patent” or the “Challenged Patent”).

2. In the preparation of this Declaration, I have confined my analysis to the materials and opinions that were available at the time of the preparation of this Declaration - supplemented with my own knowledge and experience in the field. Should new materials, analyses, or opinions be introduced subsequent to the filing of this Declaration, I reserve the right to provide supplementary Declarations to the extent necessary to address any such newly-introduced items.

3. If requested, I am prepared to explain (in a deposition or at a trial before the Patent Trial and Appeal Board (the “Board”)) the technology disclosed in the challenged patent - including the state of the art in the relevant timeframe. Similarly, I am prepared to explain the technology disclosed in the prior art references cited herein; this may include (among other things) background information on electrostatic discharge (“ESD”) technology, circuit design, layout, manufacturing, and packaging.

II. QUALIFICATIONS

4. My qualifications to testify as an expert in electronics technology are set forth in my *curriculum vitae* – Ex. 1004 – which includes a listing of cases in which I have provided expert testimony. I have more than thirty years of experience as an engineer, scientist, and consultant in the electronics industry, including in the areas of integrated circuit (IC) design, layout, structure, and operation, in the design and analysis of transistor-based digital and analog circuits, in RF technology for wireless communications, in technology development, and in technical and business development.

5. My *curriculum vitae* contains further details regarding my experience, education, and other qualifications which allow me to render expert opinions in connection with this proceeding.

III. COMPENSATION

6. I am being compensated for my work in this matter at an hourly rate of \$600 for consulting services. My compensation does not depend on the content of my opinions or the outcome of this investigation.

IV. MATERIALS CONSIDERED

7. In preparing this declaration, I reviewed and considered the following materials, along with any other materials referenced in the body of my declaration:

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 10,879,164 to Li (“the ’164 patent”)
1002	File History of U.S. Patent No. 10,879,164
1005	Japanese Unexamined Patent Application Publication No. JP2006-93598 to Yoshinaga (“Yoshinaga”)
1006	Certified Translation of Japanese Unexamined Patent Application Publication No. JP2006-93598 to Yoshinaga (“Yoshinaga”)
1007	U.S. Patent No. 9,070,700 to Haralabidis (“Haralabidis”)
1008	IC Mask Design: Essential Layout Techniques, Christopher Saint and Judy Saint, McGraw-Hill (2002) (“Saint”)
1011	U.S. Patent No. 6,078,068 to Tamura (“Tamura”)
1012	U.S. Patent No. 7,129,574 to Wu (“Wu”)
1013	U.S. Patent No. 6,144,542 to Ker et al.
1014	U.S. Patent Publ. No. 2004/0140860 to Miller (“Miller”)
1015	U.S. Patent No. 7,880,310 to Mathew (“Mathew”)
1016	U.S. Patent Publ. No. 2007/0215994 to Beauchamp et al. (“Beauchamp”)
1017	Comprehensive Dictionary of Electrical Engineering, 2nd Ed. (2005)
1018	Wiley Electrical and Electronics Engineering Dictionary (2004)
1019	The Authoritative Dictionary of IEEE Standards Terms, 7th Ed. (2000)
1020	U.S. Patent No. 6,097,098 to Ball (“Ball”)

EXHIBIT NO.	DESCRIPTION
1023	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, LTD.'s Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1025	YMTC's October 2, 2024 Infringement Contentions for the '164 Patent [FILED UNDER SEAL]
1026	C. Ito, K. Banerjee, and R. Dutton, "Analysis and Design of ESD Protection Circuits for High-Frequency/RF Applications," Proceedings of the International Symposium on Quality of Electronic Design, pp. 117-122 (2001).
1027	Uyemura, "Chip Design for Submicron VLSI," Thomson, 2006.

8. I may use these documents and information, or other information obtained during the course of this proceeding, as well as representative charts, graphs, demonstratives, schematics and diagrams, animations, and models based on those documents and information, to support and to explain my testimony. I note here that citations in this declaration are to the "endorsed" page numbers placed by counsel in the lower right corner of each exhibit.

9. My opinions are based in part on a review and analysis of the above-mentioned documents and materials. I have also drawn on my education, experience, and knowledge of basic engineering and circuit design principles in forming my opinions.

V. UNDERSTANDING OF THE LAW

A. Legal Standards

10. I am not an attorney, but I have been informed of several legal principles, which I have employed in forming my opinions in this declaration. I have been informed that each patent claim is considered separately for purposes of patentability and that a dependent claim that depends from another claim includes all of the limitations of the claim it depends from.

1. Claim Construction

11. I have been informed that the claims of the challenged patents in this proceeding are to be construed using the same claim construction standard applied in district court. I have been informed the claim construction analysis begins with the ordinary meaning of a claim term, and there is a presumption that the term carries its plain and ordinary meaning to persons of ordinary skill in the art as of the effective filing date of the patent. I have also been informed that the most important sources for determining the meaning of a claim term are the claims, the specification, and the prosecution history of the patent at issue, which collectively is called “intrinsic evidence.” I have been further informed that the meaning of a claim term may also be guided by “extrinsic evidence,” such as contemporaneous dictionaries and treatises, as well as the testimony of technically-skilled witnesses such as myself.

2. Burden of Proof

12. I have been informed that the petitioner in an *inter partes* review bears the burden of establishing unpatentability by “a preponderance of the evidence.” I have been further informed and understand that, to prove an assertion by “a preponderance of the evidence,” the party with the burden of proof must demonstrate that it is more likely than not that the assertion is true.

3. Anticipation

13. I have been informed that a patent claim is unpatentable if it is “anticipated” by prior art. I have been informed that a reference anticipates a claim if the reference discloses each limitation of the claim at issue, either expressly or inherently. I have been informed that a prior art reference may anticipate a claim without disclosing a feature of the claimed invention if that missing characteristic is necessarily present, or inherent, in the single anticipating reference as would have been understood by one of ordinary skill in the art.

14. I have been informed that material not explicitly contained in a single prior art document may still be considered for purposes of anticipation if that material is incorporated by reference into the document.

4. Obviousness

15. I have been informed that a patent claim is unpatentable if it would have been obvious to a person of ordinary skill in the art (“POSITA”) at the time of the claimed invention. I have been further informed that a claimed invention is not

patentable if differences between it and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. I have been informed that factors relevant to the determination of obviousness include the scope and content of the prior art, the level of ordinary skill in the art at the time of the invention, differences between the claimed invention and the prior art, and “secondary considerations” or objective indicia of non-obviousness.

16. I have been informed that a single reference alone can render a patent claim obvious, if any differences between the reference and the claim would have been known or obvious to a POSITA at the time of the invention. That is, if the POSITA could have adapted the reference to meet the claims of the patent by applying known concepts to achieve expected results, then the patent claims are rendered obvious by that reference.

17. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I have been further informed and understand that when a patent claim simply arranges old elements with each performing the same function it had been known to perform, and yields no more than one of ordinary skill would expect from such an arrangement, the combination is obvious.

18. I have been informed that a patent claim composed of several limitations is not obvious merely because each limitation was independently known in the prior art. Hindsight reasoning is not an appropriate basis for combining references to form an obviousness combination. I have been further informed that it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine multiple prior art references, or multiple teachings of the same prior art reference. I also understand that one of ordinary skill in the art must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

19. I have been informed that various “secondary considerations” (sometimes referred to as objective indicia of non-obviousness) may support a determination of non-obviousness and that such secondary considerations must be considered as part of an obviousness analysis. I have been informed that even strong evidence of secondary considerations may not be sufficient to rebut a strong showing of obviousness. I have been informed that the patentee bears the burden of showing the existence and effect of secondary considerations of non-obviousness, after which the burden of coming forward with rebuttal evidence shifts to the party arguing obviousness. I have been informed that the following secondary considerations may indicate non-obviousness:

20. ***Copying***: evidence that others, including the accused infringer, copied the patented invention.

21. ***Long-standing problem or need***: evidence of a persistent problem or need in the art that was resolved by the patented invention.

22. ***Prior failure***: evidence that others have tried and failed to solve the problem or failed to provide the need resolved by the claimed invention.

23. ***Commercial acquiescence of competitors***: the willingness of industry to license the patent at issue.

24. ***Skepticism***: evidence that those of ordinary skill in the art were skeptical as to the merits of the invention.

25. ***Praise***: evidence of praise directed to an invention by others in the field.

26. ***Unexpected results***: evidence that those of ordinary skill in the art were surprised by the capabilities of the claimed invention.

27. I have also been informed that the near-simultaneous invention by others can be evidence that a claimed invention is obvious. I have further been informed that the patentee bears the burden of showing a “nexus” between the claimed invention and the evidence proffered on secondary considerations (*e.g.*, proof of commercial success of a product that practices the claimed invention is not enough; there must be evidence that the commercial success resulted, at least in part, from the claimed invention).

B. Priority Date

28. I have been informed that a U.S. patent may claim “priority” to the filing date of one or more earlier filed applications. I have been informed that the priority date, also called the “effective filing date,” is the earliest filing date to which a claim is entitled – and that such date is relevant for determining what qualifies as prior art. I understand that a claim must have written description support in the application(s) to which it claims priority to be entitled to an earlier effective filing date. I have been informed that the priority date determination is done on a claim-by-claim basis, and that claims in the same patent may have different priority dates. I have been instructed by counsel for Petitioner to use November 1, 2018 (the “Priority Date”) as the priority date for all claims of the ’164 patent.

C. Level of Skill in the Art

29. I have been informed that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons one of ordinary skill in the art may have for combining references.

30. I have been informed that factors that may be considered in determining the level of ordinary skill include: (1) the type of problems encountered in the art; (2) prior art solutions to those problems; (3) rapidity with which innovations are made; (4) sophistication of the technology; and (5) education level of active workers

in the relevant field. I have been further informed that a POSITA is also a person of ordinary creativity.

31. The '164 patent generally pertains to the field of circuit design and layout - and more particularly to the design and layout of circuitry and buses that protect the (naturally-sensitive) circuitry of integrated circuits against electrostatic discharge ("ESD") – and thus protect that circuitry from being damaged or otherwise harmed by ESD events.

32. Thus, a person of ordinary skill in the art ("POSITA") in the technology field of the '164 patent at the Priority Date would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience with the design, layout, and manufacture of integrated circuits containing ESD circuitry and buses. A Master's or Ph.D. degree in a relevant field may substitute for some work experience and vice versa.

33. I was at the time of the alleged invention at least a POSITA in the art relevant to the challenged patent. Further, based on my experience, I understand and know of the capabilities of a POSITA in 2018 – and I am familiar with how a POSITA would have understood and used the terminology found in the '164 patent when filed, and with the state of the art at that time.

VI. SUMMARY OF OPINIONS

34. I have been asked to evaluate the patentability of the claims of the '164 patent in view of the prior art references listed above in Section IV. Based on my evaluation and analysis, it is my conclusion and opinion that, as of the '164 patent's Priority Date, the Challenged Claims are unpatentable as obvious. The table below summarizes the prior art combinations which I have concluded render the Challenged Claims unpatentable as obvious:

Ground	Claim(s) ¹
1	Claims 6-7, 12, and 14 are obvious based on Yoshinaga in combination with Saint and the knowledge of a POSITA
2	Claims 1-6, 8-11, and 13 are obvious based on Yoshinaga in combination with Saint, Haralabidis, and the knowledge of a POSITA
3	Claims 1-14 are obvious based on Saint in combination with Haralabidis and the knowledge of a POSITA

35. My substantive analysis in Section XI will explain in detail why I have concluded that the three Grounds listed above render the Challenged Claims unpatentable.

¹ I have been informed by counsel for Petitioner that the Yoshinaga, Haralabidis, and Saint references all qualify as prior art to the '164 patent.

36. Further, I reserve the right to cite and rely on additional portions of the cited prior art in any future declarations or depositions.

VII. TECHNOLOGY BACKGROUND

37. Before considering the '164 patent in detail, some background on the technology of the '164 patent should be considered. This involves some basic concepts of IC design, manufacturing, layout, and packaging - as well as some basic concepts of ESD events and their mitigation.

A. Integrated Circuits

38. What today we call “electronics technology” emerged quietly from a collection of remarkable laboratory experiments in the early part of the 19th century; this technology grew in scope rapidly – since electronics technology is versatile and flexible, can be used over a wide range of scale (in terms of both size *and* the amount of energy being used).

39. One key feature of electronics technology is that the circuitry involved can be built up from various components – and if the components are well-understood and robust, then implementations (such as circuits) can be created that are robust, reliable, and repeatable.

40. While a large (and still-growing) roster of electronic circuit components has been created, a major departure (from earlier mechanically-driven technologies such as mechanical relays) appeared during the 20th century – when

robust three-terminal all-electronic devices, called transistors, were developed. A transistor can be used as a simple on/off switch.

41. It soon became clear that as a single transistor became quite small, it was possible to create more than one transistor on a single piece of substrate material. This idea was developed separately by Jack Kilby at Texas Instruments (1958) and Bob Noyce at Fairchild Semiconductor (1959) (and later at Intel, where Noyce was a founder of the new company).

42. Unique properties of silicon allowed for the development of the metal-oxide-semiconductor (MOS) transistor, and for its use in a circuit technology known as CMOS (complementary MOS) technology. It was CMOS technology that proved to be a natural for predictable and successive rounds of size reductions – eventually allowing thousands, millions, and eventually *billions* of transistors to be placed on the same relatively-small-sized pieces of silicon. In fact, it was CMOS technology that allowed Gordon Moore’s simple 1965 projection (of the number of transistors that could be put into the same-sized silicon area) to continue – for decades. This has led to silicon slivers that feature the integration of large numbers of transistors and circuits – products which are thus commonly-known nowadays as *integrated circuits* (ICs).

43. The ability to put thousands/millions/billions of transistors into a small sliver of silicon brings a related curse – organizing a billion transistors (or a billion

anything) is an obvious challenge. Fortunately, CMOS proved adept at this task – as CMOS is (fortunately) amenable to being organized in a hierarchical manner; silicon circuitry can be organized so that higher-level functions, lower-level functions, and transistor-level circuits can be evaluated separately – so that a large, billion-transistor integrated circuit can be built up in hierarchical blocks.

44. This has led to a rather-standard design flow in the development of any large-scale silicon integrated circuit.

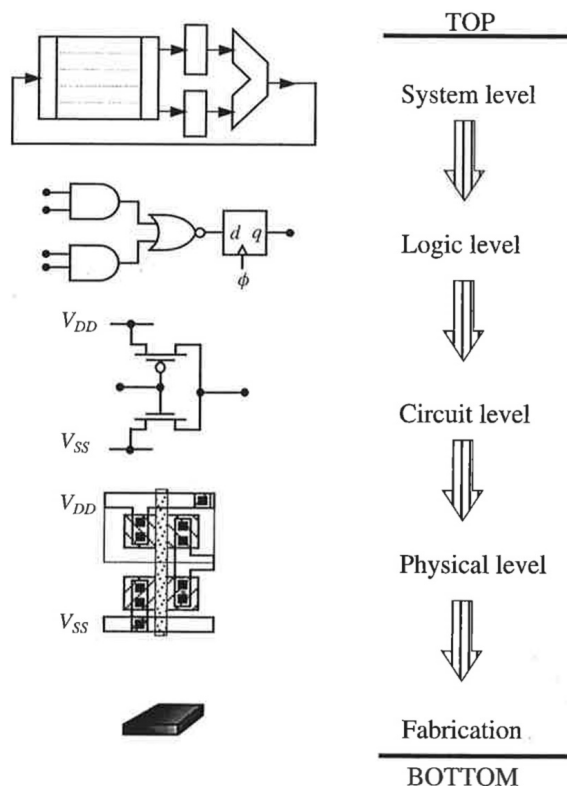
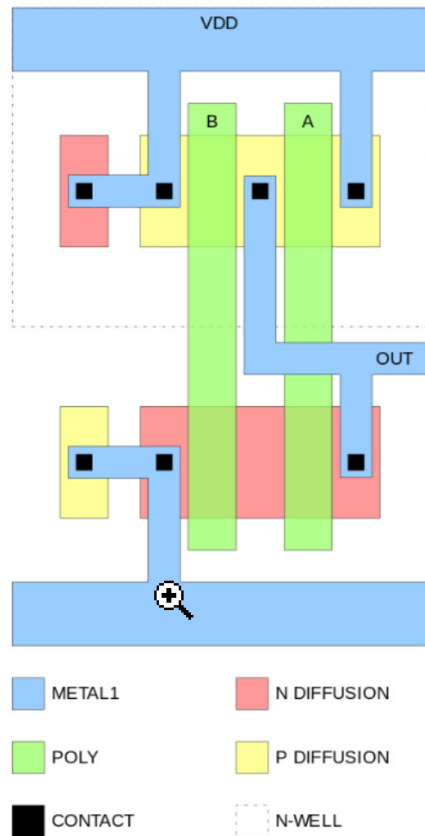


Exhibit 1027, p. 6 (Figure 2.2). First, the operational functionalities to be instantiated into the IC are developed. Next, those system functions are rendered in the logic gates that will provide the desired Boolean logic functionality. Then, these

logic functions are rendered in the form of the topological description of the circuitry that will be needed to produce this functionality – with the circuitry being “topological” since it describes the components and how they will be connected together, but does not actually describe the actual “blueprints” that are used for manufacturing. The “blueprints” are provided by the physical design phase – where the topological description of the circuitry is converted into the actual shapes and photolithographic mask renderings of the desired circuits, which are sent to the fabrication facility as the instructions for the manufacture of a particular IC.

45. It is the physical design phase where this topological description is converted into the actual on-silicon configuration (called a “layout”) that will be used for manufacturing of this circuit. An example layout is shown below.²

² <https://siliconvlsi.com/wp-content/uploads/2023/08/NAND-Gate-Layout.png>.



It is the layout form of a circuit that is actually manufactured – with the different colors of the shapes representing the various lithographic steps and processing steps that are used to make the different layers. By building a sequence of such layers (including multiple layers of metal wiring), a full-fledged IC product is manufactured. The nomenclature used to describe ground and power rails (like the blue “VDD” power rail in the figure above) included the term “bus” – and, in addition (and more generally), the term “bus” was also commonly used to describe metal wires/traces used to interconnect multiple elements. That this was well-known in the art can be seen via, e.g., various technical dictionary definitions (such as those in Exhibits 1017-1019); for example, Exhibit 1018 (at pp. 3-4) defines “bus” as

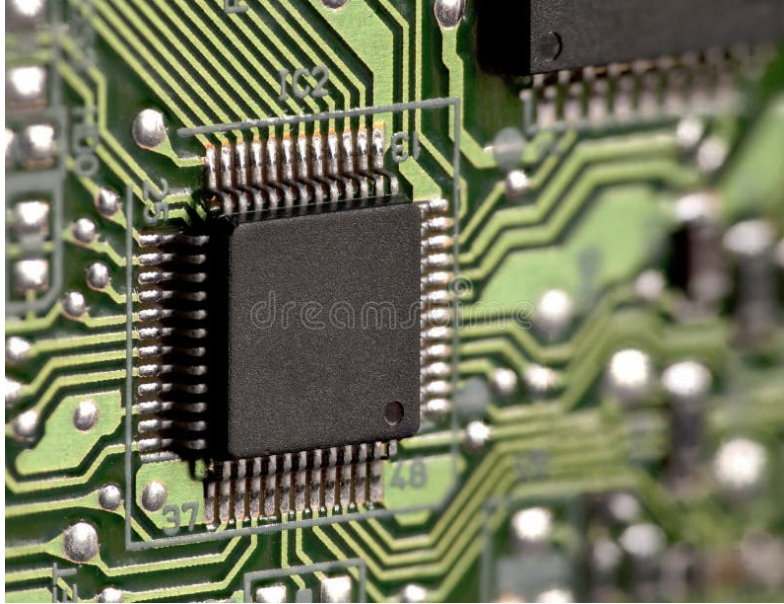
“[o]ne or more conductors which serve as a common connection for multiple circuits.” As a further example, Exhibit 1019 (at p. 3) defines bus as “[o]ne or more conductors used for transmitting signals or power from one or more sources to one or more destinations.”

B. Bond Wires and Pads

46. While an IC is a useful marvel, to be truly useful the IC must be connected to the outside world – so that it can function in some larger-scale electronic system.

47. One requirement for this implementation is that the IC must be packaged – so that it can both be protected *and* integrated into a host system. Often, this involves connecting a packaged IC onto a circuit board, with the circuit board being part of the host system.³

³ <https://thumbs.dreamstime.com/b/integrated-circuit-circuit-board-macro-shot-92131206.jpg>.



Obviously, the wiring on the circuit board connects to the IC in some way. There are a variety of methods used in the industry, but one of the most-commonly-used methods is what is known simply as “wire-bonding,” in which a “bond wire” is connected between a pin on the package and a large (by IC standards) metal pad on the IC. The white squares around the periphery of the IC in the image below are the “bond pads.”

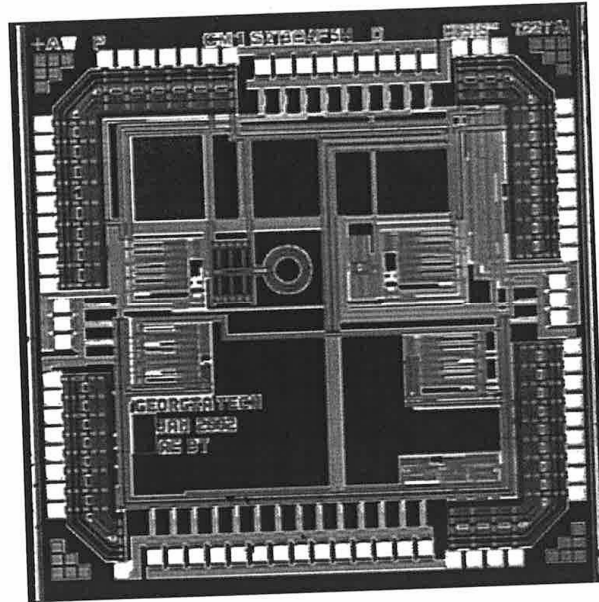
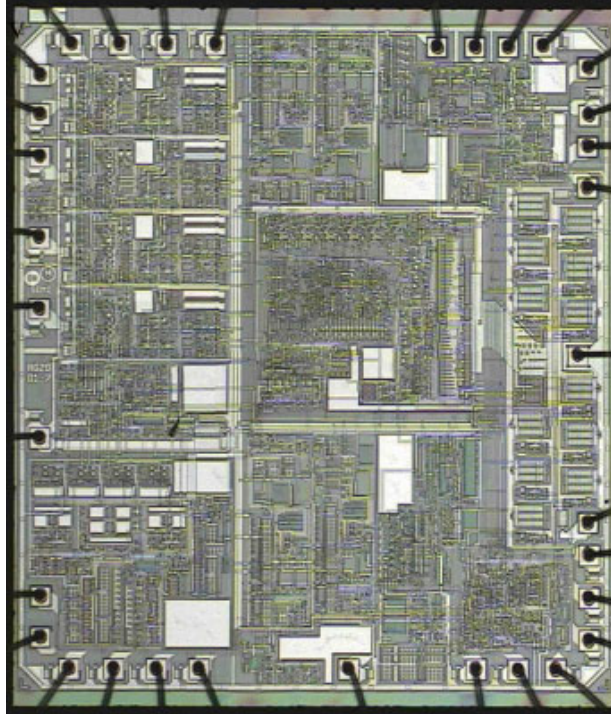


Exhibit 1027, p. 5.

48. An image of an IC with bond wires is shown in the image⁴ below. As can readily be seen, the wires connect the pads of the IC (which are shown) to particular pins of the package (which are not shown) – which allows the packaged (and thus protected) IC to be connected into a circuit board, and thus used in an electronic system. As can be seen (once again), the bond pads are arranged around the periphery of the integrated circuit.

⁴ <https://cdn.sparkfun.com/r/4000->

[400/assets/e/f/1/b/8/51c0d009ce395ff933000000.jpg](https://cdn.sparkfun.com/r/4000-400/assets/e/f/1/b/8/51c0d009ce395ff933000000.jpg).



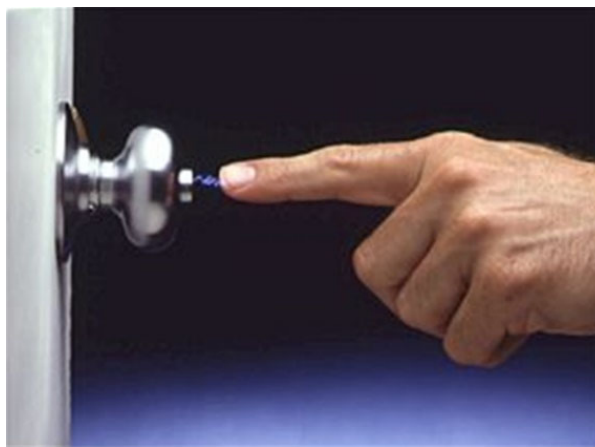
49. The design above is a good example of what is known in the art as a “core-limited” IC – which means that the (minimum) size of the IC is limited by the large amount of circuitry in the IC; in this case, even more wire bond pads could be included, but as those are unnecessary there is no reason to add them in.

50. The opposite of a “core-limited” IC is what is known in the art as a “pad-limited” IC – which is a situation wherein the number of bonding pads required is so large that the size of the IC must be large enough to accommodate all these pads. In this situation, there is thus (as a result of that need) more space for circuitry than the required circuitry uses. “Core-limited” ICs are common (such as in large-scale digital ICs), while “pad-limited” ICs more-typically occur in analog, mixed-signal, and RF designs.

51. Note also how the bond wires exit the area of the IC as directly as possible; this is considered to be good practice – as wires that run above silicon circuit areas (particularly if the wires are relatively long – which they will more likely be if they exit the IC area less directly) can droop down onto the silicon and cause short-circuiting. *See Saint*, pp. 209-210 – and especially Figures 9-15, 9-16, and 9-17. Due to the nature of how bonding machines work – i.e., “pulling” a wire from one point to another – the resulting bond wires are typically straight (when viewed from above).

C. Electrostatic Discharge (ESD)

52. Electrostatic Discharge (ESD) is a well-known and commonly-observed phenomenon in nature – covering a huge range of scale, such as lightning and the spark which occurs when one reaches for a metal doorknob.



In both cases, separate charge regions build up until the dielectric material (air) between them can no longer sustain the induced voltage – at which point the dielectric material breaks down, charge flows through the breakdown path, and the

charge-separation-induced voltage difference between the two sides disappears. In the case of the “doorknob shock,” breakdown is induced by the decreasing distance between the hand and the doorknob – as the incoming hand decreases the distance between itself and the doorknob; as the distance decreases for the same amount of separated charge, the voltage difference between the hand and the doorknob will correspondingly increase. At some point, this voltage difference becomes large enough to induce dielectric breakdown – and a lightning-like spark will occur between the hand and the doorknob as the separated charge flows and the voltage difference is neutralized.

53. There are several notable phenomena associated with electrostatic discharge events of any size or scale, including the rapidity and intensity with which they occur. Anyone who has observed a lightning strike knows that it is intense but very short-lived - while the more-prosaic doorknob shock lasts for a few tens of nanoseconds. In addition, the doorknob-shock event is further characterized by a very high transient voltage (i.e., thousands or even tens of thousands of volts), as well as a very high transient current (i.e., several amperes). Though short-lived, these events clearly pack a lot of energy punch into a small amount of time - making them potentially destructive to any sensitive electronics that might be on the receiving end of one of these events. Various solutions exist relating to shunting the energy of lightning strikes to ground - so that this energy is directed away from

electrical equipment (such as a water pump) that might be damaged by a lightning strike.

54. Not surprisingly, ESD events can be very damaging to integrated circuits - which operate in the real world and are exposed to human touch and similar phenomena. In the particular case of silicon-based CMOS technology, the vulnerabilities can be particularly severe. Like the doorknob example (where the dielectric (air) between the finger and doorknob breaks down due to an ESD event), the gate dielectric in a MOS transistor can also break down if subject to an ESD event. However, unlike the case of an air dielectric, dielectric breakdown of the MOS transistor gate dielectric will be catastrophic and irreparable; thus, an ESD event in a MOS transistor can destroy the transistor itself and render it permanently non-functional (or at least severely damaged).

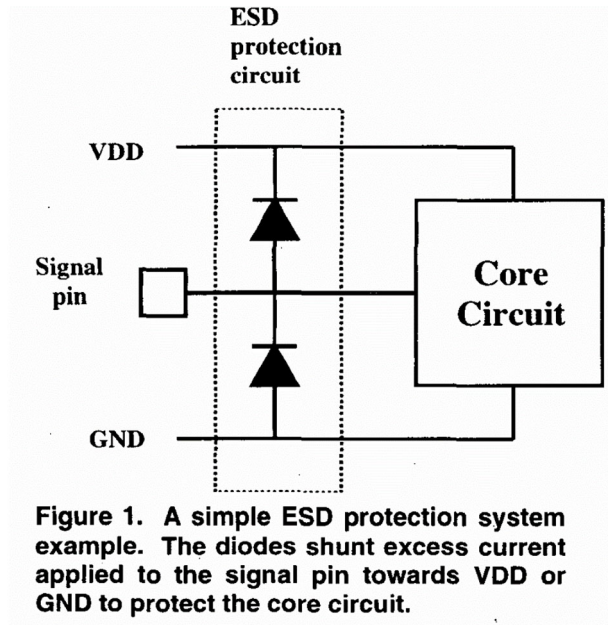
55. Not surprisingly, various approaches have been devised in the semiconductor industry over the years to try and ameliorate ESD events - so that when an event occurs, the sensitive circuitry will be protected and remain undamaged. However, any ESD protection circuitry should also have little-or-no effect on the circuitry that it is protecting - so that the performance of the CMOS circuitry will not be reduced (e.g., slowed down) by the presence and active operation of ESD protection circuitry.

56. The most-commonly-used generalized method of protection is for the ESD circuitry to shunt the transient ESD energy (e.g., current) away from the protected circuitry - and, more specifically, to shunt that ESD event to one of the power supply rails:

The protection circuit may be composed of various devices, such as diodes, transistors, or silicon controlled rectifiers (SCRs), but in all cases, these devices shunt ESD current coming from the signal pin to the power supply rails and away from the core circuit.

Ex. 1026, p. 1. The power supply rails (e.g., V_{DD} , V_{SS} , etc.) provide a readily-available destination for the energy of an ESD event - as to first-order a power supply rail can be treated as being an infinite source or (more importantly here) infinite sink of charge.

57. A simple and commonly-known ESD protection addition to a circuit involves the use of two diodes, configured to cause the shunting described above to occur.



Ex. 1026, p. 1. In the case of a positive-voltage ESD event striking the signal pin, the upper diode will turn on – and provide a shunt path diverting the energy of that event to the VDD power supply rail. Conversely, in the case of a negative-voltage ESD event striking the signal pin, the lower diode will turn on – and provide a shunt path between the pad and the GND (or VSS) power supply rail. In this manner, the core circuit is protected from being damaged by an ESD event – and the ESD protection circuitry meets the requirement of having little-or-no effect on the operation of that core circuitry.

58. Thus, the general nature of the ESD art is clear. ESD protection is added to the circuitry connected to a particular signal pin, the added ESD protection circuitry protects the circuitry directly associated with that particular signal pin, and

the method-of-protection is to shunt the energy (e.g., current) to a ground or a power supply rail.

59. Adding ESD protection onto the voltage supply and ground lines is a common way to address ESD concerns. Some people may refer to this as an ESD bus but it's nothing special, it's just some power or ground line that has ESD protection associated with / attached to it.

VIII. THE '164 PATENT

A. Overview

60. U.S. Patent No. 10,879,164 (“the '164 patent”) is entitled “Integrated Circuit Electrostatic Discharge Bus Structure and Related Method.” The sole inventor is Zhiguo Li, and the listed assignee is Yangtze Memory Technologies Co., Ltd; the application which led to the issuance of the '164 patent was filed on December 2, 2018, and is a continuation of an application filed on November 1, 2018.

61. The problem that the '164 patent is attempting to address is depicted in the Prior Art figure of Figure 1:

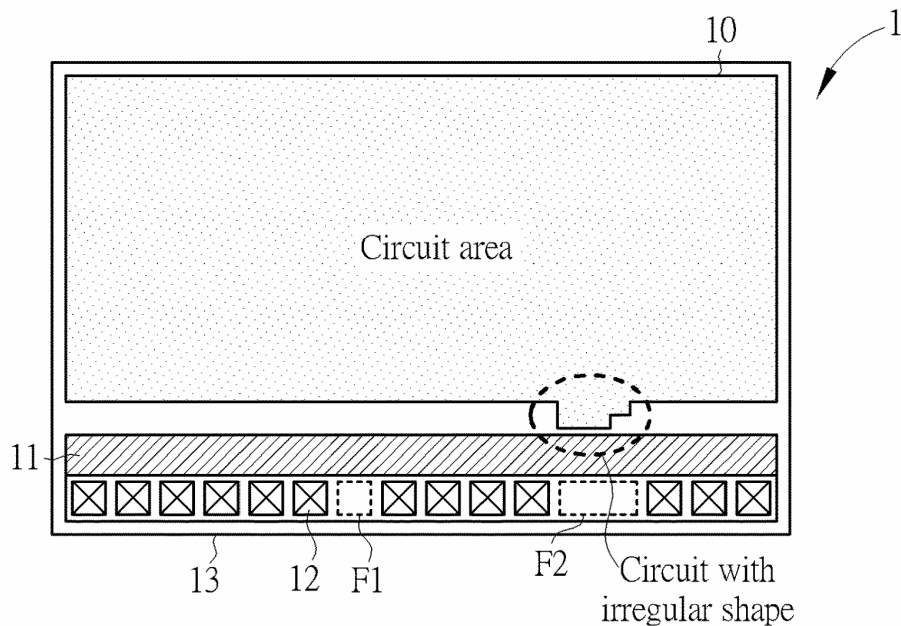


FIG. 1 PRIOR ART

The IC structure (1) includes a circuit area (10), an ESD bus (11), and bond pads (12); as the '164 patent specification describes, this ESD bus (11) is connected to a system ground or a system voltage (“... a layout trace connected to a ground or a system voltage...” – '164 patent at 1:33-34) in the conventional ESD protection formulation (as detailed in Section VII.C). In particular, as this is clearly a “core-limited” IC design (a term explained in Section VII.A), there is empty space between some of the bond pads – space which is blocked off from the circuit area of the IC by the ESD bus; this space is therefore filled up with “filler cells” (a term well-known in the art) – and as the filler cells provide no circuit functionality, this can be regarded as wasted space in the IC floorplan.

62. The '164 patent proposes a modification of this basic structure to make better use of the space available in the IC – as depicted in the embodiment presented in Figure 2:

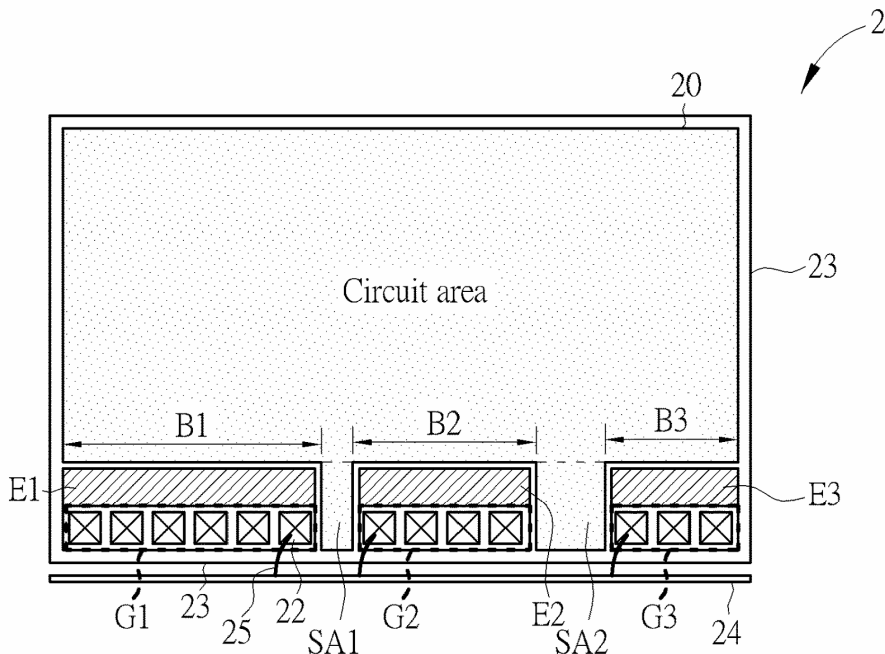


FIG. 2

Here, the ESD bus has been divided up into multiple subsections, so that it does not block the area between the circuit area and the bottom edge of the integrated circuit (i.e., the area that, in Figure 1, was required to be occupied by the filler cells). By breaking up the ESD bus and allowing the filler cells to be removed, the available circuit area is expanded to include the “saved areas” (SA1 and SA2) shown in Figure 2.

63. However, as just noted, the formerly continuous ESD bus (11) has been broken up into several bus structures. To remedy this introduced shortcoming, the

'164 patent adds what it calls a “common ESD bus” (24) external to the IC; the various ESD buses must be connected to this common ESD bus for the shunting functionality of IC ESD protection (*see* Section VII.C) to be most effective.

64. One way that the '164 patent addresses this problem as depicted in

Figure 3:

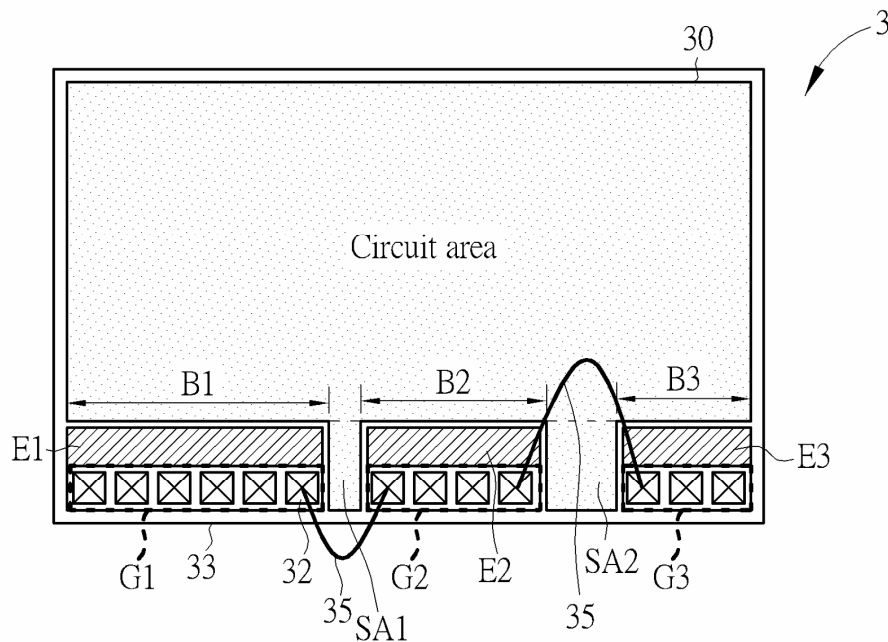


FIG. 3

Here, each ESD bus segment is connected to one or more bond pads (32 and its multiple instances) – and the connection between these ESD bus segments is provided by pad-to-pad bonding wire segments (35). To complete the connectivity that is used to provide ESD protection, one of these wire-bond-interconnected pads must be “connected to a ground or a system low voltage” ('164 patent at 3:63-64).

B. Prosecution History

65. The application which led to the issuance of the '164 patent was filed on December 2, 2018 – and claimed a priority date of November 1, 2018 based on a foreign patent application of that date.

66. On April 2, 2020, the applicant received a final rejection of all 17 claims of the application. Ex. 1002, pp. 170-179. Claims 5, 8, 13, 15, and 16 were rejected as being indefinite – while Claims 1 – 13 were rejected as being rendered obvious by Tamara (U.S. Patent No. 6,078,068) in view of Wu (U.S. Patent No. 7,129,574), and Claims 14 – 17 were rejected as being rendered obvious by Wu. *Id.*

67. On May 4, 2020, the applicant filed a response to this rejection – by amending several of the claims, and by disputing particular aspects of the rejection. Ex. 1002, pp. 192-207.

68. On August 5, 2020, the applicant received a second final rejection of all 17 claims of the application – on largely the same grounds; Claims 5, 8, and 15 were rejected as being indefinite, Claims 1 – 4, 6, 7, 9, and 13 were rejected as being rendered obvious by Tamara in view of Wu, and Claims 14, 16, and 17 were rejected as being rendered obvious by Wu. Ex. 1002, pp. 209-219.

69. On September 10, 2020, the applicant filed a response to this rejection – by further amending several of the claims so as to address the concerns of the Examiner. Ex. 1002, pp. 230-238.

70. On September 22, 2020, the applicant received a Notice of Allowance – and U.S. Patent No. 10,879,164 issued on December 29, 2020. Ex. 1002, pp. 239-241.

IX. CLAIM TERMS

71. I have given the terms in the challenged claims their plain and ordinary meanings, as would have been understood by a person of ordinary skill in the art at the time of the alleged invention, taking into consideration the language of the claims, the specification, and the prosecution history of the '164 patent. I have applied these understandings of the claim terms in my analysis and in forming my opinions where appropriate in this Declaration.

X. OVERVIEW OF THE PRIOR ART REFERENCES

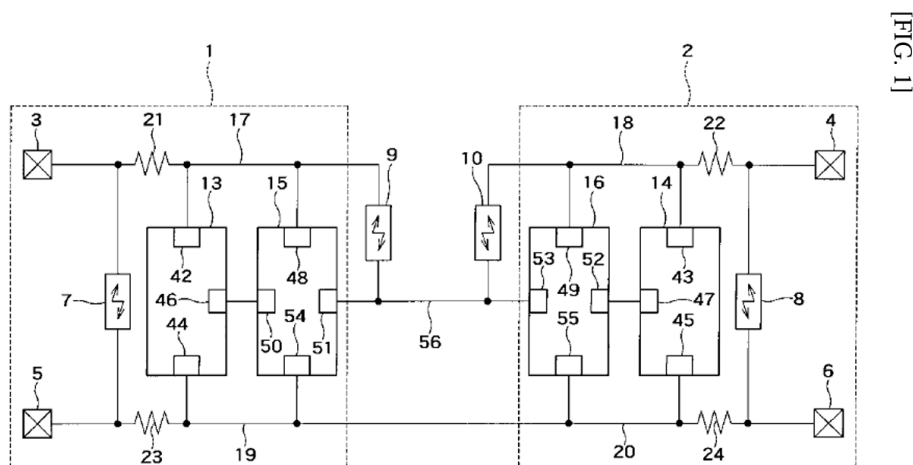
72. This section provides brief overviews of the main prior art references that I used in my analysis (which will be detailed in Section XI).

A. The Yoshinaga Reference

73. The Yoshinaga reference (“Yoshinaga”) is Japanese Patent Application JP2006-93598; as this application is only available in the original Japanese and as I do not speak Japanese (other than a few pleasantries and random words), I reviewed a certified translation of this patent application – which is Exhibit 1006. This reference is entitled “Semiconductor Integrated Circuit,” and the sole inventor is

Hiroyuki Yoshinaga; this patent application was published on April 6, 2006 – and thus is demonstrably prior art to the '164 patent.

74. Yoshinaga describes several embodiments of circuitry that involve the shunting of ESD over-voltage events from the affected signal line to a power supply voltage line or reference voltage line. Yoshinaga provides a base-level example embodiment in Figure 1:



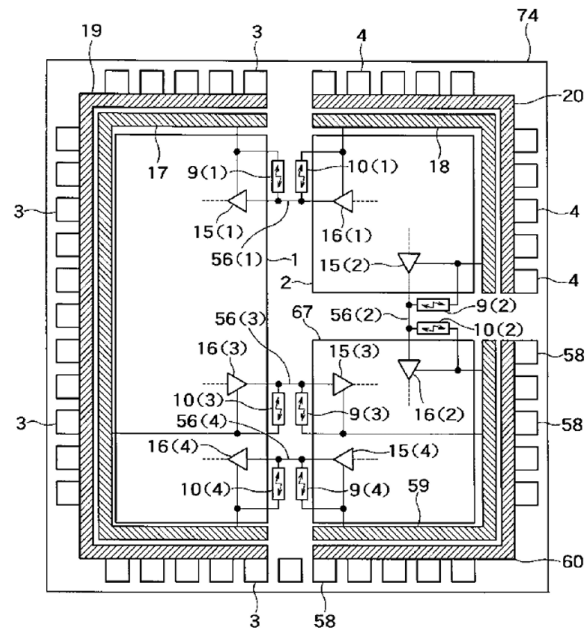
Yoshinaga identifies the entire embodiment of the figure as being a “semiconductor integrated circuit” (Yoshinaga at [0013]), with 1 and 2 being exemplary constituent circuits of that larger “integrated circuit.” Elements 13, 14, 15, and 16 are identified as being circuit elements of the larger (prior-identified) circuits 1 and 2, and elements 7, 8, 9, and 10 are identified as being ESD protective elements; pads 3 and 4 are identified as being power supply voltage pads, while pads 5 and 6 are identified as being reference voltage pads. ESD protection is provided by shunting the energy of an ESD event to one of the power supply pads (using ESD element 9 or 10), or to

any of the four pads using (respectively) ESD protective elements 7 or 8; note, however, that the reference voltage pads 5 and 6 are connected together by a common line (*i.e.*, an ESD bus) – so that when the energy of an ESD event is shunted in this direction, it is shunted onto this common line (and can thus be removed from the circuitry at either pad 5 or pad 6, or both together).

75. Note also that the embodiment of Figure 2 includes additional ESD protective elements 11 and 12 – which provide a complement to the ESD protective elements 9 and 10 (which first appear in Figure 1), allowing a path from this area of the integrated circuit to the common reference voltage line (connecting pad 5 and pad 6) that was described above. Note further that in the embodiment of Figure 3, the notion of a common connection line between reference voltage pads (here, pad 39 and pad 40) is further developed – with the “reference potential line 41” (Yoshinaga at [0061]) providing the path for the removal (from the circuitry) of the energy of an ESD event.

76. Yoshinaga combines these disclosures together into an IC embodiment in Figure 6:

[FIG. 6]



Elements 1, 2, and 67 are circuit blocks, multiple incarnations of elements 9 and 10 provide ESD protective elements (as described above), pads 3, 4, and 58 are the power supply pads, elements 17, 18, and 59 are (separate) power supply voltage lines, and elements 19, 20, and 60 are (separate) reference voltage lines. Note in particular that there are open “lanes” between the circuit blocks (1, 2, and 67) – where the ESD protective elements (the various incarnations of 9 and 10) are located; note also that these open “lanes” extend to the edge of the IC, and that in the top and right-hand cases, there is no bonding pad where the open “lane” reaches the edge of the IC (whereas there *is* a bonding pad in the case of the “lane” which reaches the bottom edge of the IC).

B. The Saint Reference

77. The Saint Reference (“Saint,” Exhibit 1008) is a book published in 2002 – with a full title of “IC Mask Design: Essential Layout Techniques.” The authors are Christopher Saint and Judy Saint, and the book was published by McGraw Hill.

78. This book is lengthy – running well over 400 pages in length; as such, it contains a great deal of material, and covers a wide range of ground in physical design (which includes layout) – including discussion of ESD-protection physical design and bond pad physical design. Rather than attempt to provide an overview of an entire book of this size, specific excerpts will be cited as necessary during the analysis provided in Section XI.

C. The Haralabidis Reference

79. The Haralabidis reference (“Haralabidis,” Exhibit 1007) is U.S. Patent No. 9,070,700, and is entitled “Apparatus for Electrostatic Discharge Protection and Noise Suppression in Circuits”; the two inventors are Nikolaos Haralabidis and Ioannis Kokolakis; the application which led to the issuance of this patent was filed on March 30, 2012, and claims priority to a provisional application filed on November 4, 2011 – and thus is demonstrably prior art to the ’164 patent.

80. Haralabidis addresses a known problem in “system-on-a-chip” (“SoC”) integrated circuit design – where various circuit blocks are gathered together into a

single IC. The ability to build up a large, complicated IC from blocks (either hierarchical or disparate – or both) is one of the natural-and-good features of silicon CMOS IC technology – as it allows high levels of integration, which reduces costs and improves circuit performance.

81. However, a known problem in SoC design occurs when the various blocks being assembled (and connected together – as the ability to connect these blocks together in close proximity is one of the reasons for using an SoC approach) are sufficiently-functionally-different to cause interaction problems. A salient problem (which is discussed in Haralabidis) is that digital circuit signals are binary (i.e., the digital “1”s and “0”s involve rapid rail-to-rail switching) and thus very noisy during switching events. In contrast, the circuitry which is included to perform analog, RF, and similar functions is designed to process signals that are in sinusoidal (rather than digital) form; as such, these types of circuits can suffer from unacceptable signal degradation when the switching noise from digital circuitry reaches them – usually over common (i.e., bus or bus-like) connection lines (such as a shared power supply line). The problems become even more complicated when the circuitry must also be designed to include ESD protection – protection which serves to mitigate the possible problems that ESD events can cause (as described in Section VII.C).

82. Haralabidis addresses these problems via the embodiment disclosed in Figure 5.

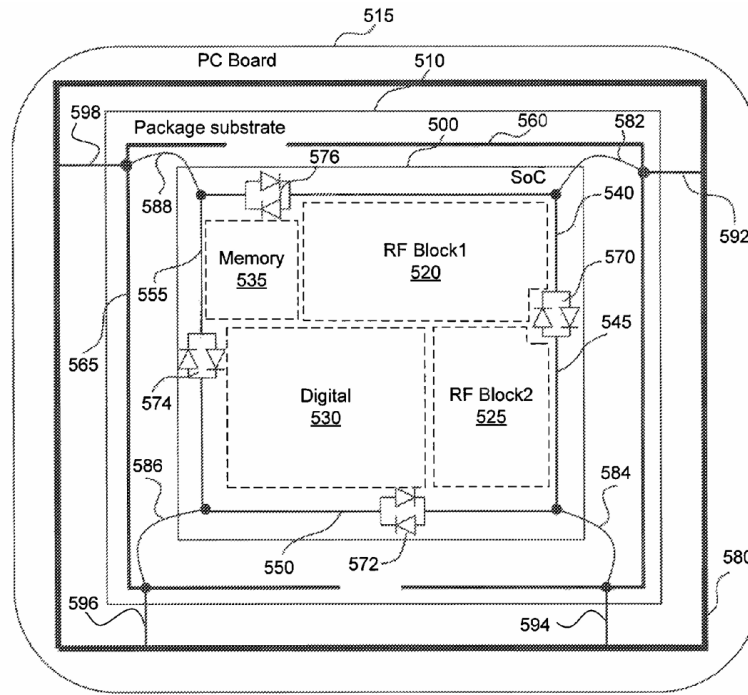


FIG. 5

Here, in the SoC 500, the “digital” block 530 and the memory block 535 are the digital circuit blocks, while 520 and 525 are RF blocks. Each block has its own segmented ground rail (540, 545, 550, and 555 respectively); there are two segmented package rails (560 and 565) – and the segmented ground rails of the digital circuit blocks both connect to the same segmented package ground rail (565) using the connections 586 and 588, while the segmented ground rails of the RF blocks both connect to the same segmented package ground rail (560) using the connections 582 and 584; as there are two package segmented ground rails, it is likely that each package segmented ground rail connects to a package pin of its own.

Finally, both package segmented ground rails connect to the PC board common ground rail 580, via the connections 592, 594, 596, and 598; as can be seen in the figure, there is a single PC board ground rail 515 – which is depicted in Figure 5 as extending completely around the package substrate 510.

83. However, for purposes of this Declaration and the associated analysis, in addition to the inventive Figure 5 of the patent, there is also a prior art embodiment Figure 3 that is relevant.

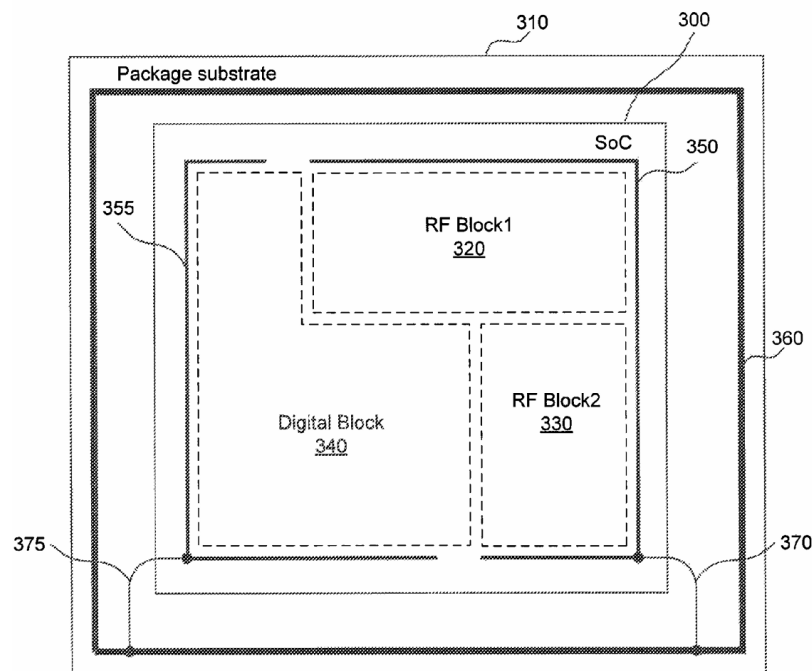


FIG. 3
Conventional Art

In this embodiment, the SoC IC (300) is connected into a package substrate (310). As in the Figure 5 embodiment, there are (two, rather than four) segmented ground rails in the SoC – but in contrast to the Figure 5 embodiment (which has four

segmented ground rails), the Figure 3 embodiment contains only two segmented ground rails; one of these provides the ground connection (375) to the digital block (340), while the other provides the ground connection (350) to the RF blocks (320 and 330); however, unlike the case of the Figure 5 embodiment, there is only a single package ground rail (360) – which is a common ground rail connected to the two segmented ground rails (in the SoC) using the connections 370 and 375. Haralabidis describes the single package ground rail (360) as providing the rail to which the energy of an ESD is shunted – to provide ESD protection for the IC circuitry.

84. As mentioned above, Figure 3 of Haralabidis is a prior art embodiment – and Haralabidis teaches the embodiment of Figure 5 as an inventive improvement over the prior art embodiment of Figure 3. However, the source and status of this prior art embodiment (Figure 3) is immaterial to its usage for analysis with respect to the '164 patent – as Haralabidis being demonstrably a prior art reference means that this prior art embodiment is also demonstrably prior art to the '164 patent.

XI. UNPATENTABILITY ANALYSIS

85. As will be explained in detail below, it is my conclusion and opinion that all the claims of the '164 patent are unpatentable – as they are rendered obvious (in various ways) by the three references cited above (in Section X) and the knowledge of a POSITA at the time of the filing of the application that led to the issuance of the '164 patent. It should be noted that while particular references are

used in this analysis, their content is not exclusive to those references – as supporting material (which will be cited during the description of the analysis) also demonstrates that this material was well-known in the art (and well-beyond the particular references chosen for use in the analysis) at the '164 patent Priority Date.

A. Ground 1—Yoshinaga, Saint, and the Knowledge Possessed by a POSITA

86. It is my conclusion and opinion that Claims 6, 7, 12, and 14 of the '164 patent are rendered obvious by Yoshinaga in combination with Saint and the knowledge of a POSITA.

1. Motivation to Combine Yoshinaga and Saint

87. In Section V.A.4, I provided my understanding of the legal standards related to requirements for showing obviousness of patent claims. In particular, with respect to the combining-together of more than one prior art reference,

I have been further informed that it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine multiple prior art references, or multiple teachings of the same prior art reference.

As also noted in Section V.A.4, I have also been informed that a POSITA should also have a reasonable expectation of success, without undue experimentation, when combining two-or-more prior art references.

88. It is my further understanding that there is not a rigid test that is used to assess the viability (or lack thereof) of an assertion of a motivation to combine two or more prior art references – but rather, as per the excerpt (from earlier in this Declaration) cited above, that the requirement is only that one must identify “a reason that would have prompted a person of ordinary skill in the relevant field to combine multiple prior art references.” I further understand from counsel for Petitioner that the following considerations may be taken into account when assessing modifications to a reference: (A) combining prior art elements according to known methods to yield predictable results; (B) simple substitution of one known element for another to obtain predictable results; (C) use of known technique to improve similar devices in the same way; (D) applying a known technique to a known device ready for improvement to yield predictable results; (E) “obvious to try” – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; (F) known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art.

89. It is my conclusion and opinion that a POSITA would have been motivated to combine the teachings of Yoshinaga and Saint – and would have been able to do so with a reasonable expectation of success, and without undue

experimentation. Based on my understandings as explained in the prior paragraph, there are at least five reasons that a POSITA would have been motivated to combine Yoshinaga and Saint – with some being general, while others relate to more specific aspects of the disclosures of Yoshinaga (which is a patent application) and the material provided in Saint (which is a book).

a. Yoshinaga and Saint Address Interrelated Issues.

90. Yoshinaga and Saint are in the same general field of art – and therefore address interrelated issues on multiple levels.

91. Yoshinaga and Saint both deal with the general form of an IC footprint (including bond pads). Further, Yoshinaga and Saint both discuss ICs at this footprint level – including bond pads, buses, ESD connection layout, and circuitry inside the inner area of the IC.

92. Yoshinaga specifically addresses ESD protection in integrated circuits; e.g., Yoshinaga begins by stating that the teachings of the patent application will involve “a semiconductor integrated circuit having an Electro Static Discharge (ESD) protection circuit.” Yoshinaga at [0001]. Yoshinaga notes the particular problem of the standard ESD protection architecture (which was described earlier, in Section VII.C) when both digital circuitry and analog circuitry are present in the same IC – that switching noise generated in the digital circuitry can propagate through the ESD protection circuitry and reach the analog circuitry, where this

digital switching noise can be detrimental to the operation of the more-sensitive (to input signals) analog circuitry (e.g., *see* Yoshinaga at [0004]); as digital circuit blocks and analog circuit blocks often have independent power supply lines to mitigate this kind of noise-transmission (by effectively isolating the power supply lines running to the different blocks), connecting the ESD protection circuitry to the same power supply line overrides this power-supply-isolation technique. Thus, Yoshinaga proposes to remedy this problem with a different circuit architecture (vs. the prior art); *see*, e.g., *id.* at [0007] – [0008].

93. Saint is a textbook – and thus covers a great deal of ground. Saint deals broadly with the actual design, development, and manufacturing of integrated circuits; in particular, Saint is focused on the “physical design” phase of integrated circuit design and development (with physical design (which includes what is commonly known in the art as “layout” of the circuitry) having been explained in Section VII.A). As part of the discussions of the physical design of ICs, Saint includes copious discussion of ESD protection circuitry and its implementation during physical design – *see*, e.g., “ESD Supply Strategies” at pp. 160-164, as well as the generalized discussion in pp. 316-350.

94. Therefore, a POSITA would be motivated to combine Yoshinaga and Saint because they address interrelated issues.

b. Yoshinaga and Saint are Analogous Art to Each Other and to the '164 Patent.

95. Yoshinaga and Saint are analogous art to each other, and are both analogous art to the '164 patent.

96. As noted above, Yoshinaga and Saint both address many of the same issues in the design of real integrated circuits at many different levels – including floorplanning, placement of circuit blocks, configuration of bond pad placement, ESD protection architecture, etc. With regard to Yoshinaga, relevant exemplary excerpts include [0001]-[0010], [0053]-[0055], [0074]-[0086], Figure 2, and Figure 6; Figure 6 is particularly-noteworthy – as it depicts (at a conceptual level) an IC floorplan, with the floorplan including circuit blocks, connections between the blocks, rail lines for power supply voltages, grounds, and reference voltages, and bond pads around the periphery of the IC. With regard to Saint, relevant exemplary excerpts include pp. 63-64, 160-172, 211-221, 344, and 347.

97. A POSITA would thus have been motivated to combine Yoshinaga and Saint – because they are analogous art to each other. A POSITA would also realize that while Yoshinaga is comparatively-terse (as Yoshinaga is a patent application) and Saint is rather wide-ranging (as Saint is a book – and a fairly large one at that), there is considerable overlap in the topics they discuss; this, as just mentioned, makes Yoshinaga and Saint analogous art to one another, and to the '164 patent (which shows layouts in Figure 2 and Figure 3 at a similar level of granularity).

c. Saint Provides Information That Allows for Better Use of Silicon Floorspace in Yoshinaga.

98. Saint provides particular information that can be used to improve the teachings of Yoshinaga – in particular, Saint provides information that shows a POSITA how to make better use of extra silicon floorplan space that is already disclosed in Yoshinaga; this is space that Yoshinaga shows as empty – rather than being occupied with items such as bond pads, rails/buses, or other structures.

99. Further, Yoshinaga demonstrates an awareness of one of the main reasons for making most-efficient use of silicon floorplan space – as it is desirable to design an IC so that “there is little increase in the chip size and the total number of wiring, and thus increase in the unit price of the chip can be prevented as much as possible.” Yoshinaga at [0086]. This is consistent with the well-known constraint facing IC designers – that silicon wafer surface space basically costs a particular amount per the extent of the area used for the IC; thus, reducing the size of the IC will also reduce the cost of manufacturing that IC.

100. Saint explicitly describes using empty space between bond pads as locations for the deployment of IC circuitry – which amounts to more-efficient use of silicon floorplan space, which (as mentioned above as being well-known in the art) allows for a smaller-sized IC and a lower cost of manufacturing that IC. Specifically, Saint (at p. 220) suggests that “[i]f you do have a core-limited circuit design, you will have some wasted space around the edges between the pads. Maybe

you can push some of your circuitry into this wasted space to try to use those gaps.”

Saint also states in a figure caption (Figure 9-28, on p. 221) that “We can use extra space surrounding our pads to shrink our chip size.”

101. Therefore, a POSITA would have been motivated to combine Yoshinaga and Saint – for the purpose of using Saint’s discussion of using “wasted space” between the bond pads to expand the circuit area available in the IC floorplan; this amounts to utilizing the empty inter-pad space in Yoshinaga to host circuitry (and to reduce the overall IC size, for the beneficial reasons mentioned above).

d. Saint Provides Detailed Material on the Use of Bond Wiring.

102. Saint provides further particular information that can be used to improve the teachings of Yoshinaga – in particular, Saint provides information that shows a POSITA how to make good and proper use of bond wires and bond wiring.

103. As was noted earlier, Figure 6 of Yoshinaga depicts a full design of a silicon integrated circuit – which includes the bond pads that provide the locations where the circuitry of the silicon integrated circuit is connected to the outside world. However, Yoshinaga is silent on the details of how the bond pads (in Figure 6) are used and connected.

104. A POSITA would have been well-aware that bond wires and bond wiring were already well-known in the art. However, as Saint provides considerable detail on this topic, a POSITA would clearly have been motivated to consult Saint

for the details of wire bonds and wire bonding that are (and long have been) commonly used in the integrated circuitry industry – for the express purpose (mentioned above) of connecting that silicon-based IC to the outside world (such as to a printed-circuit board (PCB) that would allow the leads of the silicon IC to be connected to a host system of some sort). As Saint states (at p. 207), “Wire bonding is the most common method of attaching a chip to a package” – and in the following discussion (on pp. 207-214), Saint provides extensive detailed discussion of the details of using wire bonding to “[attach] a chip to a package.”

105. Thus, a POSITA would have been motivated to combine Yoshinaga and Saint, so as to use Saint’s detailed information (along with extant POSITA knowledge) to provide bond wiring for Yoshinaga’s IC – as an IC has no use if its various connection points (which encompass power lines, ground lines, signal lines, etc.) cannot be connected to the outside world.

106. In addition, a POSITA would have understood that it was well-known in the art that in addition to providing connections between the IC bond pads and the package traces (which lead to the package pins), it was also well-known that wire bonding and the same wire bonding techniques could be used to connect one bonding pad directly to another, or one package trace directly to another.

107. This can be clearly seen in several prior art references – which are used in some of the analysis below with respect to Ground 1. For example, Miller (Ex.

1014) depicts pad-to-pad wire bond connections in (at least) Figure 7, Figure 10, and Figure 13, and discusses this usage in (at least) the Abstract of the patent application. In addition, Mathew (Ex. 1015) depicts wire bond connections between rail lines within the IC (Figure 2 and the discussion of Figure 2 at 6:67-7:7). As a final example, Beauchamp (Ex. 1016) depicts (in Figures 4-8) the use of bonding wires to directly make connections that are pad-to-pad and package-trace-to-package trace (often using a simple “daisy-chaining” technique to accomplish this); Beauchamp discusses these teachings in more detail in the specification in several places – such as a description of the reasoning behind the teachings at [0007], a description of wire bonding equipment (and various techniques for forming the bond between the wire and the bond pad) at [0027]-[0030], and a description of the aforementioned figures (Figures 4-8) at [0034]-[0038].

108. Thus, a POSITA would have been motivated to combine the well-known use of wiring bonding techniques to provide inter-pad (and inter-trace) connections) with Saint’s extensive detailed discussions of generalized techniques for using wire bonding to connect bond pads to package traces – and to combine those techniques with Yoshinaga.

e. A POSITA Would Have Had a Reasonable Expectation of Success in Making These Combinations.

109. The four reasons (of why a POSITA would have been motivated to combine Yoshinaga and Saint) above analyzed the content of those references and

the motivations to combine them in various ways. However, as noted above (and also in Section V.A.4), this motivation must also be shown to include a reasonable expectation of success, and without undue experimentation.

110. It is my conclusion and opinion that a POSITA would have had a reasonable expectation of success without undue experimentation when making these combinations. This conclusion was inherent in my analysis of the specific details of the reasons underlying a motivation to combine Yoshinaga and Saint (as is clear from what was said above); however, some additional (and/or reinforcing) discussion will be provided here.

111. A POSITA would have had a reasonable expectation of success when combining Yoshinaga's IC design teachings with Saint's description of using the "wasted space" (as Saint calls it) for some of the circuitry of the IC – as this more-efficient use of the silicon real estate (by essentially expanding the "circuit area" to include what was originally "wasted space") requires no special techniques.

112. As noted in Section XI.A.2.f, Yoshinaga discloses empty space between the pads / pad-groups, but does not discuss what to do with them; however, as a POSITA would have been aware that "wasted space" is undesirable and would have wanted to make use of it, Saint provides an explanation of why there is nothing that mitigates *against* using that "wasted space" (in, e.g., Yoshinaga Figure 6) for circuitry.

113. Further, Saint provides additional practical details regarding *how* to actually place circuitry in those spaces. Saint notes something that would have been well-known to a POSITA – that in order to place circuitry anywhere in the circuit area (including in the “wasted spaces”), the layout ground rules (associated with the particular manufacturing process to be used to fabricate the IC) must be followed (*see, e.g.*, Saint at pp. 224-225). As just mentioned, this (known) requirement would also apply to the situation where circuitry is being placed in the “wasted spaces” – which confirms (and would confirm to a POSITA) that the circuit layout rules apply to those “wasted spaces” in the same way that they apply to anywhere in the circuit area; for example, there are design rules that limit how close to a bond pad any circuitry can be placed – and these design rules apply to any circuitry, whether it is in a “wasted” space or not. With specific reference to Saint Figure 9-28, Saint expressly discloses using these “extra spaces” to host circuitry “in and around the[] pads.” Saint at p. 221.

114. Thus, a POSITA would have had a reasonable expectation of success, and without undue experimentation, when placing circuitry inside the “wasted spaces” – and would have been able to do this to the Figure 6 embodiment of Yoshinaga by combining in the guidance provided by Saint.

115. In addition, a POSITA would have had a reasonable expectation of success, and without undue experimentation, when combining Saint’s guidance

regarding bond wires with Yoshinaga's teachings (such as the Figure 6 embodiment) that depict bond pads but provide no further details regarding how those bond pads are to be connected to the outside world. As noted above (in Section XI.A.1.d), Saint (at p. 207) states that "[w]ire bonding is the most common method of attaching a chip to a package." Therefore, a POSITA would have been able to use Saint's guidance to connect Yoshinaga's bond pads to the outside world – using wire bonding techniques to connect the bond pads to package traces (and thus to package pins).

116. Further, a POSITA would have been able to further combine Yoshinaga and Saint as detailed just above – and add in the further combination of using wire-bonding techniques to provide direct pad-to-pad (and trace-to-trace) connections. The three references mentioned in Section XI.A.2.e (Ex. 1014, Ex. 1015, and Ex. 1016) all confirm that this was well-known in the art – and these references also show that typical wire-bonding equipment and typical wire-bonding techniques can readily be used to create these wire bonds. Indeed, the same (well-known) techniques that are used to connect one end of a wire to a bond pad can readily be used to connect the other end of a wire to another bond pad. Connecting two bond pads directly together (e.g., with a jumper wire) would have involved only the application of well-known wire bond techniques (which were discussed above). Note also that this is true regardless of whether or not the jumper spanned a “saved

area” – as the wire would serve its known purpose (as an ohmic electrical connection) in just the same way.

117. Therefore, a POSITA would have had a reasonable expectation of success, and without undue experimentation, in extending well-known wire-bonding techniques (well-described by Saint) to include pad-to-pad (and trace-to-trace) wire bonds.

118. Thus, in summary, a POSITA would have been motivated to combine Yoshinaga with Saint, and (for the reasons described) just above) would have been able to do so with a reasonable expectation of success and without undue experimentation.

2. Claim 6

119. Claim 6 is an independent claim, and is an apparatus claim.

a. [6-pre]: “An integrated circuit structure, comprising:”

120. As an initial matter, I will be offering no opinion regarding whether or not the preamble of claim 6 is limiting; I have been instructed by counsel for the Petitioner to assume that the preamble is limiting – and I have thus conducted my analysis using that assumption.

121. Yoshinaga discloses the preamble of Claim 6 – as can easily be seen via simple examination of Yoshinaga. First, the title of Yoshinaga is

“Semiconductor Integrated Circuit.”⁵ Second, the Abstract of Yoshinaga begins with “To improve ESD resistance in a semiconductor integrated circuit...” In total the phrase “integrated circuit” (or the plural form “integrated circuits”) appears 42 times in Yoshinaga. *See, e.g.*, Yoshinaga, [0001], [0009], [0074]-[0086], Figs. 1-4, 6. Thus, Yoshinaga renders obvious the preamble of Claim 6.

b. [6a]: “a circuit area;”

122. Yoshinaga discloses this claim element of Claim 6.

123. To begin, what the ’164 patent means by “a circuit area” is explained in the Abstract:

An integrated circuit ESD bus structure includes *a circuit area*; a plurality of electrostatic discharge (ESD) buses; a plurality of pad groups adjacent and connected to the plurality of ESD buses; a common ESD bus; and a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus. (’164 patent at Abstract; emphasis added.)

⁵ An “integrated circuit” is commonly-known in popular parlance as a “silicon chip”; however, an integrated circuit can be (and frequently is) constructed using materials other than silicon. Thus, the term “integrated circuit” – both in general and in Yoshinaga – is not restricted to just *silicon* integrated circuits; in fact, Yoshinaga itself makes no such limitation.

In this form, the “circuit area” – as used in the ’164 patent – is exclusive of the other items listed as being *not* part of the “circuit area.”

124. The ’164 patent further illustrates a “circuit area” in those same terms, via Figure 2 of the patent:

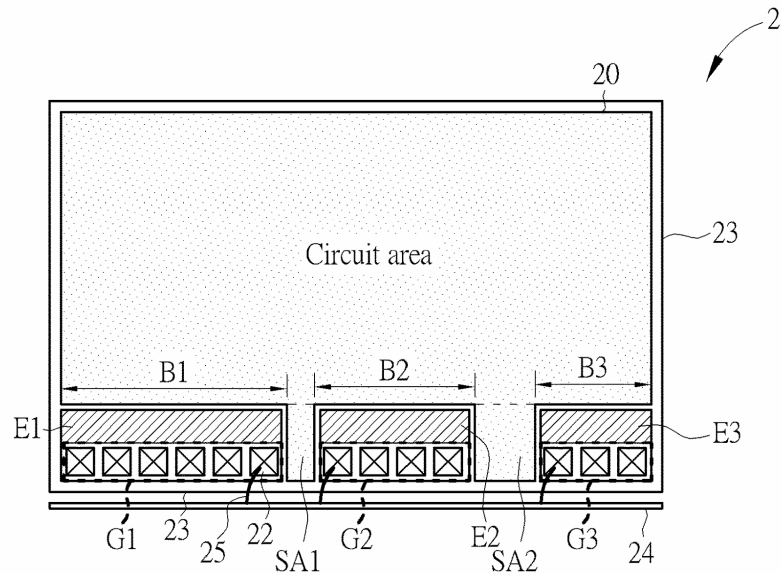
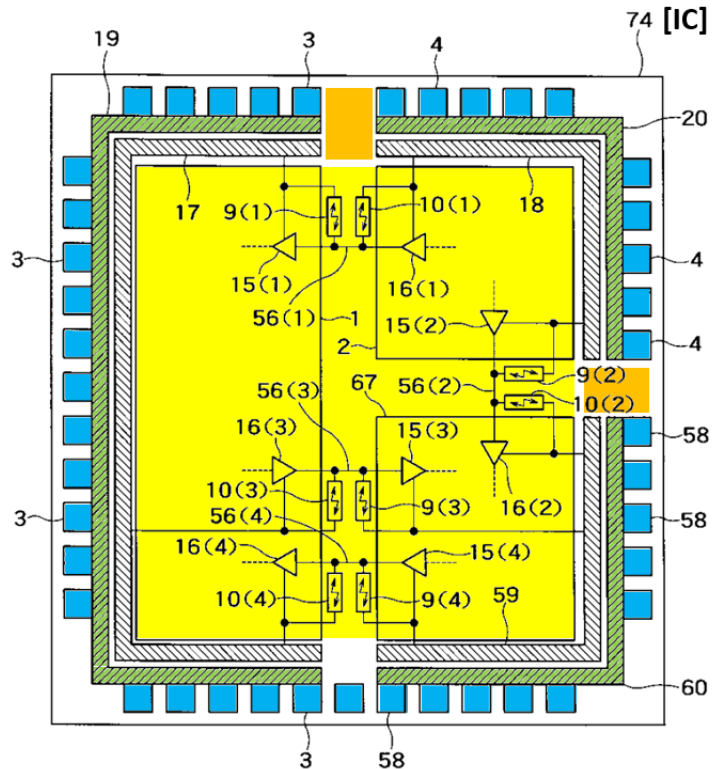


FIG. 2

This visual description is consistent with the explanation provided in the Abstract, as detailed above.

125. Viewed in this light, Yoshinaga discloses this claim element of Claim 6 of the ’164 patent. Yoshinaga discloses “a circuit area” which contains the circuitry – with the same list of items (as listed in the Abstract of the ’164 patent) being regarded as exclusive from the circuit area. This can readily be seen via an annotated version of Figure 6 of Yoshinaga:



As is done in the '164 patent, Yoshinaga illustrates a “circuit area” (highlighted in yellow) which contains circuitry and circuit blocks. *See* Yoshinaga, [0075]-[0076]. Separately, power supply lines (17, 18, and 59), reference potential lines (10, 20, and 60), and bond pads (3, 4, 58, and others⁶) are located outside of the circuit area. This is the same organization that is described in the '164 patent.

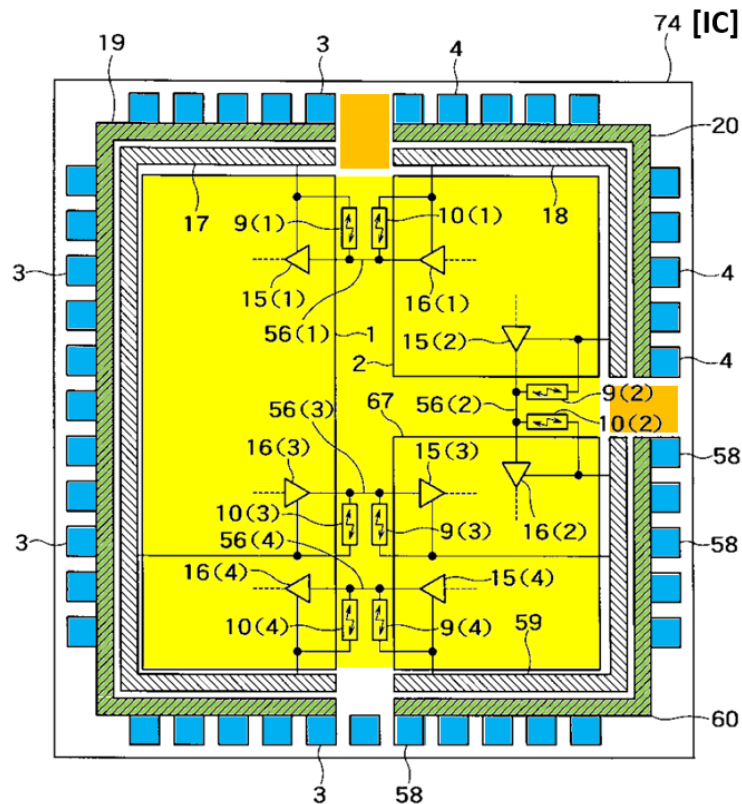
⁶ Yoshinaga specifically identifies the pads labeled 3, 4, and 58 as “power supply pads”; however, it is well-known in the art (and would be well-known to a POSITA) that an IC must have bond pads for connections other than just “power [supplies]” – things such as reference potential lines and signal lines. Thus, one can conclude that

126. Thus, claim element [6a] is satisfied by Yoshinaga.

c. [6b]: “a plurality of ESD buses;”

127. Yoshinaga discloses this claim element of Claim 6 of the '164 patent.

128. As a first step, the annotated Figure 6 of Yoshinaga (provided above) can be reprised here:

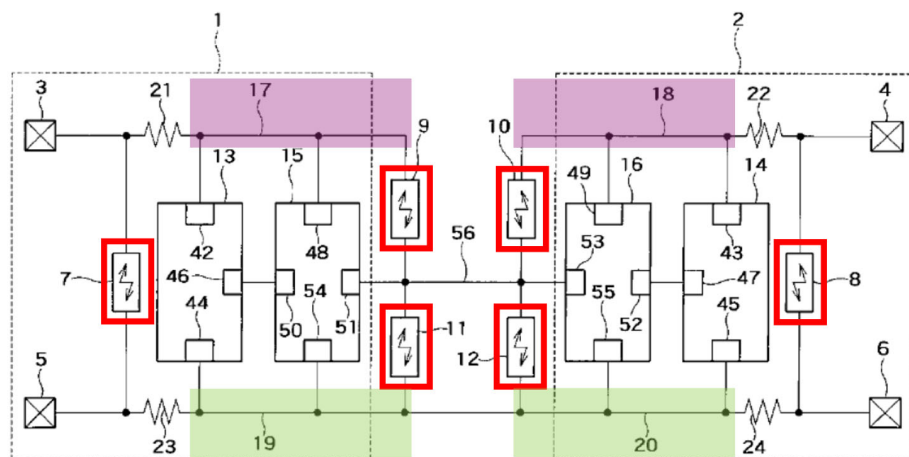


pads other than those that Yoshinaga has identified as “power supply pads” will be used to perform those sorts of functions. In fact, Yoshinaga explicitly points this out – e.g., “Reference potential pads are not shown to simplify the drawing.” Yoshinaga, [0078].

The “reference potential line 19, reference potential line 20, and reference potential line 60” in Yoshinaga are the claimed “plurality of ESD buses.” Yoshinaga, [0077].

129. Yoshinaga specifically identifies elements 7 – 12 as “ESD protective element[s].” Yoshinaga, [0013]-[0015], [0054]. As can be seen in Figure 2 below, these elements are connected to what Yoshinaga identifies as the “power supply lines” (in these connections as either 17, 18, or 59) and/or reference lines 19 and 20. This is consistent with the conventional implementation of ESD protection in an integrated circuit (as described in Section VII.C) – whereby the energy of an ESD event is shunted to a power supply rail or ground, making reference lines 19 and 20 (which take (and sink) the energy) ESD buses.

130. Yoshinaga provides a further depiction of this type of circuit architecture in Figure 2 – which is included here in annotated form:



Yoshinaga provides further textual descriptions of these functionalities at, e.g., [0036], [0046], [0052], [0054], [0061], and [0073]. Moreover, a POSITA would

have understood that the same configuration and connections of circuits 1 and 2 in Yoshinaga Figure 2 (e.g., respective ESD circuits connected to a local ground bus) apply to circuit 67 in Figure 6. One reason for this understanding is because Figure 6 shows the same ESD elements 9, 10, 15, 16, and 56 between circuits 1, 2, and 67; in addition, a POSITA would have further understood that the shared ground connection between ground rails 19 (in circuit 1) and 20 (in circuit 2) would extend to ground rail 60 in Figure 6.

131. Thus, Yoshinaga satisfies claim element of Claim 6 of the '164 patent.

d. [6c]: “a plurality of pad groups, adjacent and connected to the plurality of ESD buses; and”

132. Yoshinaga discloses and/or renders obvious this claim element of Claim 6 of the '164 patent.

133. To simplify the analysis, this claim element will be split into claim sub-elements.

i. [6c-1]: “a plurality of pad groups”

134. Yoshinaga discloses and/or renders obvious this claim sub-element of claim element [6c] of Claim 6 of the '164 patent.

135. As an initial matter, the '164 patent graphically describes what is meant by “pad groups” in Figure 2 of the patent:

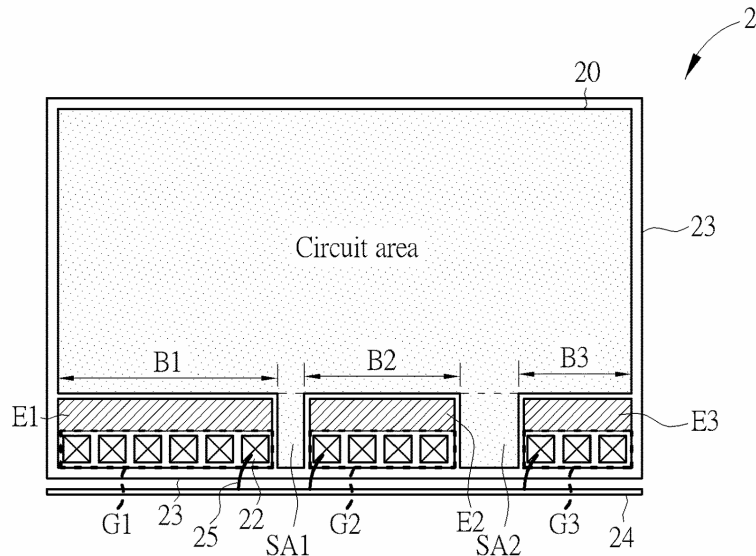


FIG. 2

The specification (at 2:51-52) identifies G1, G2, and G3 as “pad groups” – and G1, G2, and G3 as “a plurality of pad groups.”⁷

136. The highlighted version of Yoshinaga Fig. 6 (below) shows various “pads” in blue, with power supply pads 3, 4, and 58 being examples. Yoshinaga, Figure 6, [0076]-[0077]. As noted elsewhere, Yoshinaga explains that the “[r]eference potential pads are not shown [in Figure 6] to simplify the drawing” – however, the reference pads are shown in Yoshinaga Figures 1-4 with the numerals

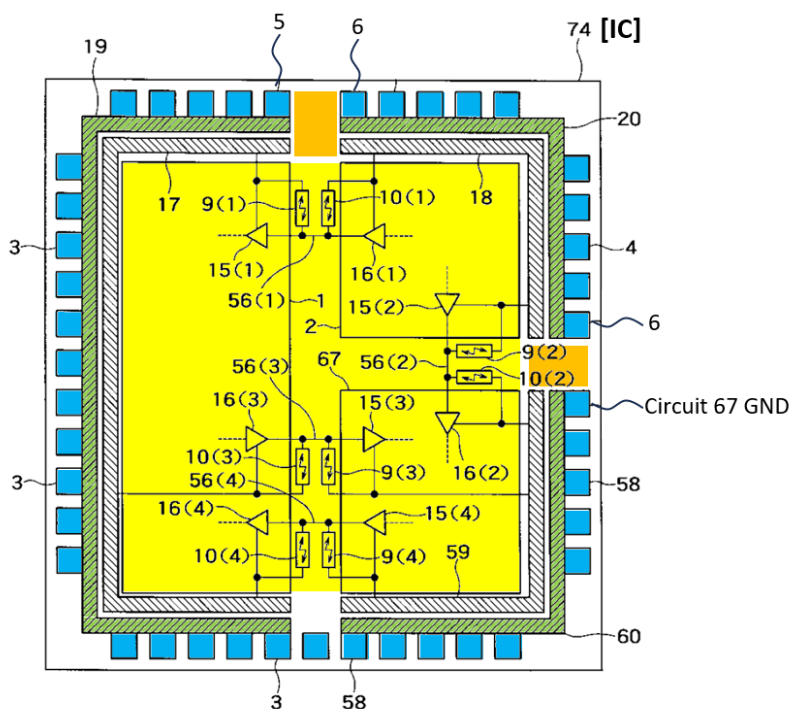
⁷ For completeness, it should be noted that the specification also states that a pad group contains “at least one pad” (at 3:6-7); therefore, a “pad group” could consist of only one pad – and thus a single pad in a prior art reference would also amount to a disclosure of a “pad group.”

5, 6, 39, 40. *Id.*, [0078], Figs. 1-4. As such, a POSITA would understand that Yoshinaga Fig. 6 is merely an illustrative rendering, and is not intended to reflect the exact number of pads which may be present – or to convey their specific electrical connections. This is apparent, for example, by looking at the “power supply pads” 3, 4, and 58 in Figure 6 which are shown next to the ground rail; a POSITA would understand that those pads are connected to the power rails 17, 18, and 59 (as is shown in the schematics of Figures 1-4) – and are not connected to the ground rails 19, 20, and 60 (because such a connection would create a short circuit).

137. As it relates to the reference pads (such as pads 5 and 6 in Figures 1-4), a POSITA would have understood that those pads are connected to ground rails 19, 20, and 60. Further, the pads in Yoshinaga Figure 6 are largely fungible when it comes to their specific assigned connections – and their assigned locations among the available pads; for example, a POSITA would have understood that the pads labeled 3, 4, and 58 could just as readily be used for reference pads. The choice of selecting which pads to assign for ground, power, signals, etc. is left to the discretion of the designer - and may depend on factors such as the size of the chip, whether the chip is pad-limited or core-limited, the number of I/O signals, and the number available pads; however, there is no inherent restriction on how pads may be assigned. Indeed, Saint shows exactly this in its discussion of Figure 7-6 and 7-7, where the grouping and pin assignments are rearranged to not be “[s]cattered” (i.e.,

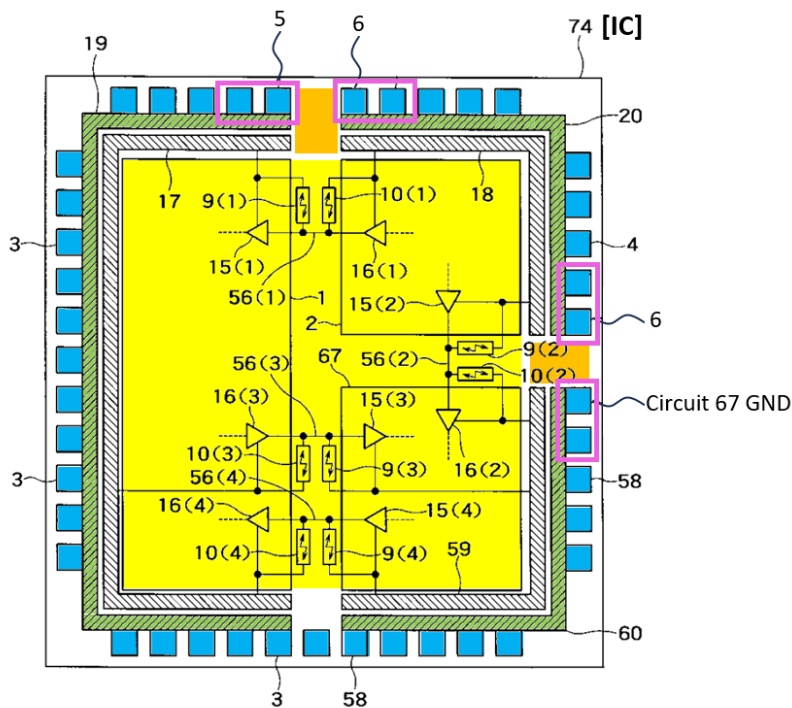
placed without regard to where their respective internal IC connections will be made). Thus, a POSITA would have understood (or at least found it obvious) to use the pads immediately next to the saved areas as reference pads (*e.g.*, pads 5 and 6). One reason for this selection (discussed further for element [6d]) is to preserve Yoshinaga's saved area for other circuitry – as taught by Saint.

138. For purposes of illustration, reference pads (*e.g.*, pads 5, 6, etc.) are located as shown below near the orange saved spaces. Although Yoshinaga does not assign a numeral for the reference/ground pad of circuit 67, that pad is also labelled below as “Circuit 67 GND” – to indicate that it is a reference line for circuit 67.



Yoshinaga, Fig. 6 (annotated).

139. Just as the '164 patent illustrates and describes pad groups of varying sizes (from a single pad up to six pads), Yoshinaga's pads may be grouped into pad groups as well. Again, for illustrative purposes, the pink boxes below show groupings of two pads - but the pad groups could just as easily have more or fewer pads, and groups of different sizes would be just as obvious as groups of two.



Yoshinaga, Fig. 6 (annotated).

ii. [6c-2]: “adjacent and connected to the plurality of ESD buses”

140. Yoshinaga discloses and/or renders obvious this claim sub-element of claim element [6c] of Claim 6 of the '164 patent.

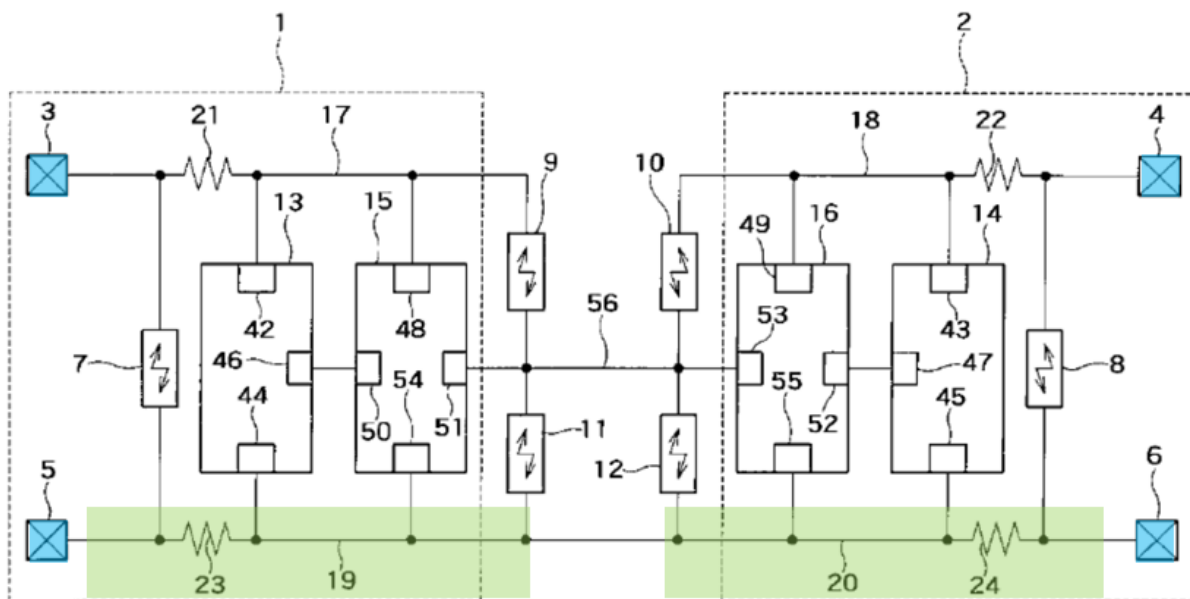
141. As an initial matter, the '164 patent offers no specific definition of the word “adjacent”; thus, plain-and-ordinary meaning should be assumed. A dictionary definition⁸ of “adjacent” that is germane to this situation includes either “not distant: nearby” or “having a common endpoint or border.”

142. The exemplary pad groups in Yoshinaga Figure 6 are located adjacent to the reference potential lines 19, 20, and 60 – and Yoshinaga Figure 6 shows the reference lines in close proximity (“adjacent”) to the pad groups. Even under a narrow and more restrictive interpretation of “adjacent” – one that required that the claimed “pad groups” and “plurality of ESD buses” actually share a border or endpoint – Yoshinaga Figure 6 satisfies (or least renders obvious) this as well.

143. With regard to the “connected to” requirement, my analysis for the previous sub-element explained that a POSITA would understand that the reference pads would be connected to their respective ground rails. As further confirmation of this, Yoshinaga Figures 1-4 show that pad groups (comprising reference voltage pads 5 and 6 (shown in Fig. 2 below) and/or pads 39 and 40 (from Fig. 3)) are “connected to” the reference potential lines 19, 20, and 60 (highlighted in green below). Accordingly, Yoshinaga discloses that the claimed “a plurality of pad groups” (e.g., the pads in Figure 6 corresponding to reference pads 5, 6, 39, and/or

⁸ <https://www.merriam-webster.com/dictionary/adjacent>.

40) are “connected to” the “plurality of ESD buses” (e.g., reference lines 19, 20, and 60).



Yoshinaga, Fig. 2 (annotated), [0035]-[0036], [0053]-[0062], [0088].

e. [6d]: “a plurality of bonding wires configured to connect one to another of the plurality of pad groups;”

144. This claim element of Claim 6 of the ’164 patent is rendered obvious by Yoshinaga and the knowledge of a POSITA.

145. As an initial matter, the use of bond wires – to connect the bond pads of the IC to the package leads (which connect to the pins of the package) – is very well-known in the art, having been used pretty much since the introduction of integrated circuits and their packaging.

146. For example, Saint describes (at p. 207) how “[w]ire bonding is the most common method of attaching a chip to a package,” while further noting (as

described just above) that “bond wires” are used to connect “bond pads on the chip” to the package leads (which connect to the pins of the package). This is depicted graphically in Figure 9-2 of Saint:

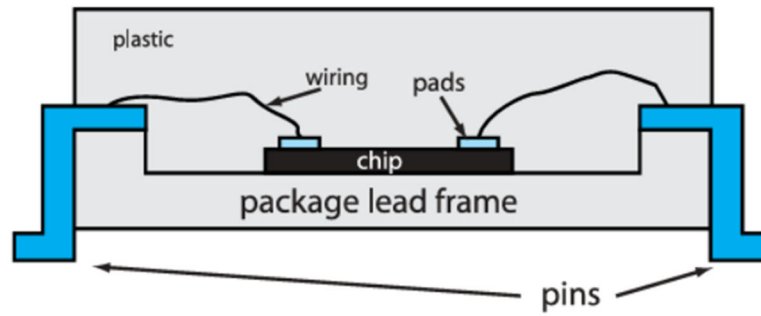
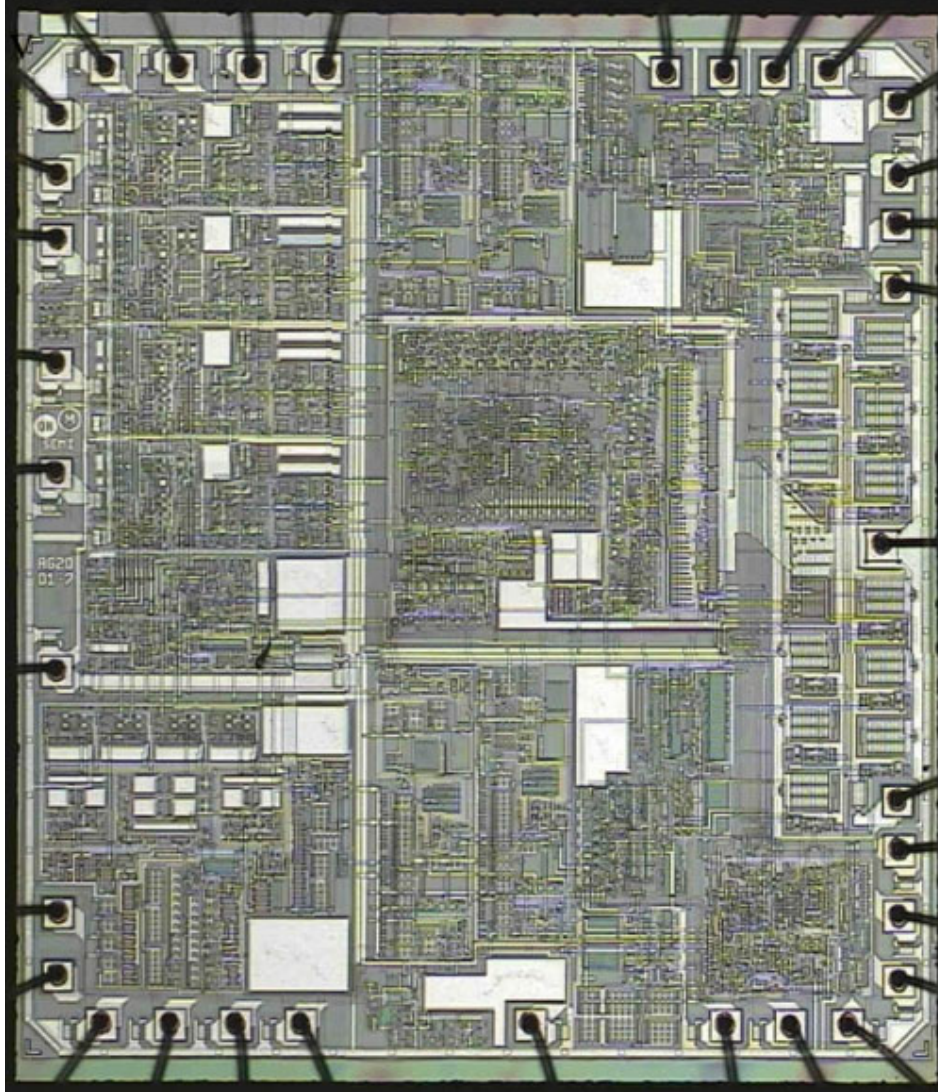


Figure 9–2. The top plastic is molten when deposited. The wires are surrounded before it hardens.

147. As another example, a microphotograph image in a 2010 article⁹ shows bond wires connecting to the bond pads of an integrated circuit:

⁹ <https://www.sparkfun.com/news/384>.



As can be seen, bond wires connect to the bond pads – and these wires (as per Figure 9-2 of Saint and the general knowledge of a POSITA) connect to the package leads and thus to the package pins.

148. This claim element of Claim 6 of the '164 patent, however, differs from this art – as the claim element describes using bond wires “... to connect one to another of the plurality of pad groups”; that is, this claim element involves the use

of bond wires to connect a bond pad in one pad group to a bond pad in another pad group. This is depicted, e.g., in Figure 3 of the '164 patent¹⁰:

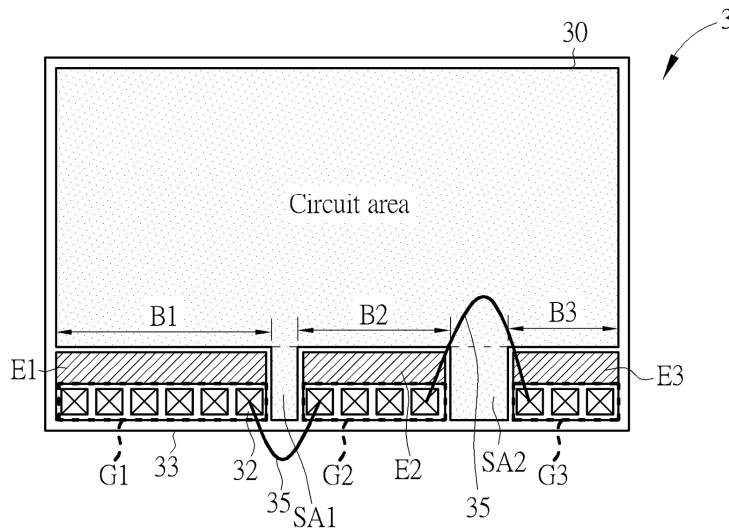


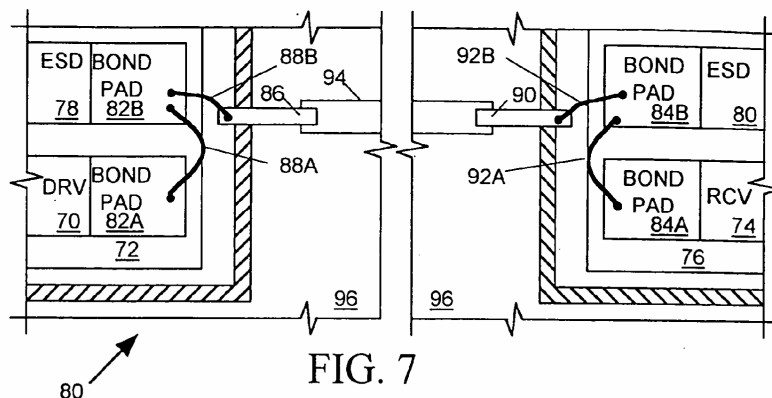
FIG. 3

The two depicted instances of bond wire 35 involve using a bond wire as a “jumper” to directly connect a bond pad in one pad group to a bond pad in another pad group.

149. The use of bond wires to connect one bond pad to another bond pad was disclosed, for example, by Miller (Exhibit 1014). As Miller explains in the

¹⁰ Note that in this depiction, while the “jumper” bond wires (the two instances of 32) appear to be “flat” with respect to the x-y plane of “structure” (3), in reality bond wires are routed up-and-over (i.e., in the z dimension, above) the underlying surface – as Figure 9-2 of Saint and the image from the 2010 article make clear; this is also well-known in the art, and would have been known to a POSITA at the time of the filing of the '164 patent.

Abstract, “The contact pads are linked to one another and to the IC I/O terminal though inductive conductors such as bond wires...” Miller at Abstract. This is shown in Figure 7 of Miller:



As can be seen, bond wires 88A and 92A are used to directly connect one bond pad to another bond pad – over a space that intervenes between the two bond pads (82A/82B and 84A/84B, respectively); as Miller explains “Bond pad 82A is connected to bond pad 82B through a bond wire 88A...” and “[s]imilarly, bond pad 84A is connected to bond pad 84B though a bond wire 92A...” *Id.* at [0051].

150. As another example, the use of bond wires to connect one bond pad to another bond pad is disclosed, for example, by Beauchamp (Exhibit 1016). Beauchamp depicts this pad-to-pad connection in, for example¹¹, Figure 4 (plan view) and Figure 6 (cross-sectional view):

¹¹ See also Figures 5, 7, and 8 – which are similar to Figure 4.

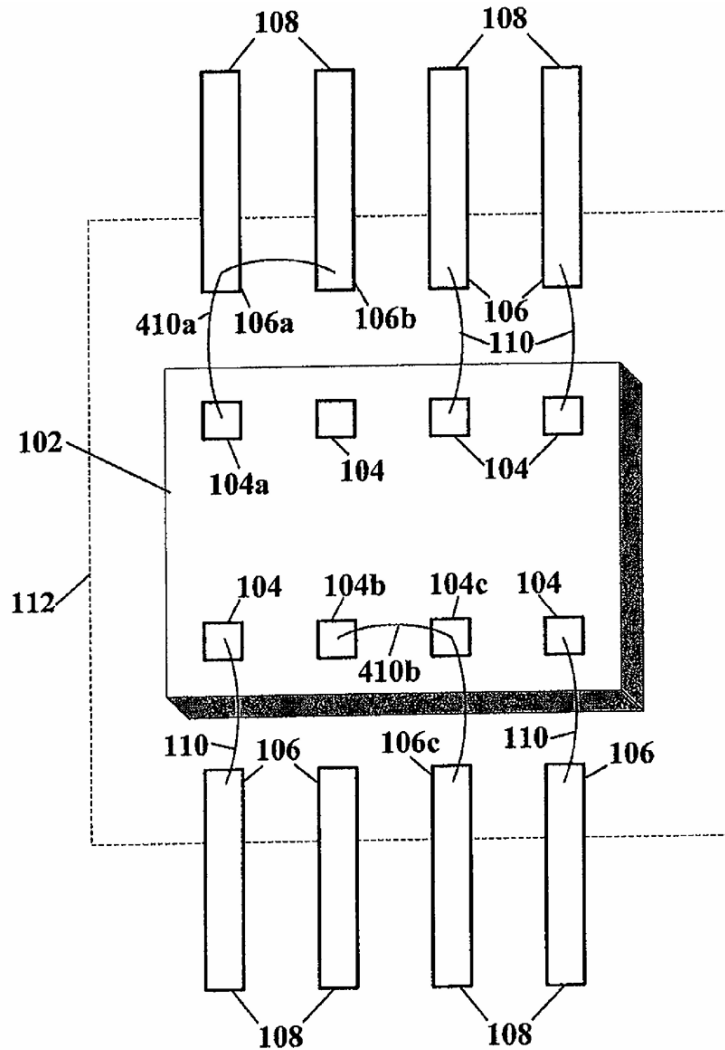


FIGURE 4

FIG. 4 is a schematic plan view of an integrated circuit device comprising an integrated circuit die having two bond pads thereon and an inner lead of a leadframe and connected together with a single bond wire, and two other inner leads of the leadframe *connected to another bond*

pad with another single bond wire, according to specific example embodiments of this disclosure.

Beauchamp at [0020] (emphasis added). Note that in Figure 4, Beauchamp depicts both the use of bond wires to connect bond pads directly together, and the use of bond wires to connect package traces (which essentially are the package pins) together.

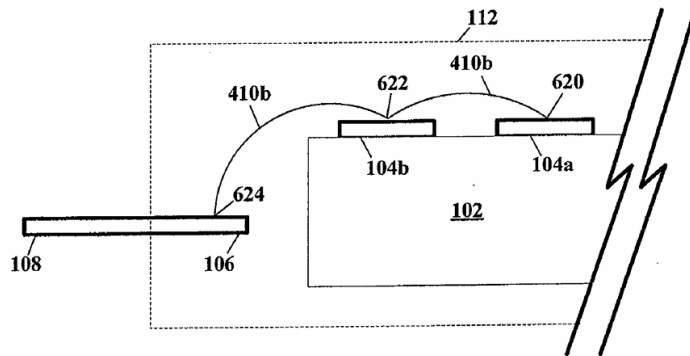


FIG. 6 is a schematic elevational view of an integrated circuit device having a single bond wire connecting bond pads of an integrated circuit die to an inner leadframe, according to specific example embodiments of this disclosure.

Id. at [0022]. This figure clearly shows that Beauchamp discloses that the pad-to-pad connections are created by daisy-chaining the wire from location to location (here, from bond pad 620 to bond pad 622, and then to package trace 106). On the pad labeled 104b, this allows the bond to the pad (622) to be connected to another

bond pad (and to the package trace) with only a single bond formed on that pad; as Beauchamp explains,

Preferably, the first connection will be at the bond pad 104a. A connection to bond pad 104b may be made by wedge bonding the bond wire 410b *which remains unbroken or continuous* until bonded to the inner lead 106.

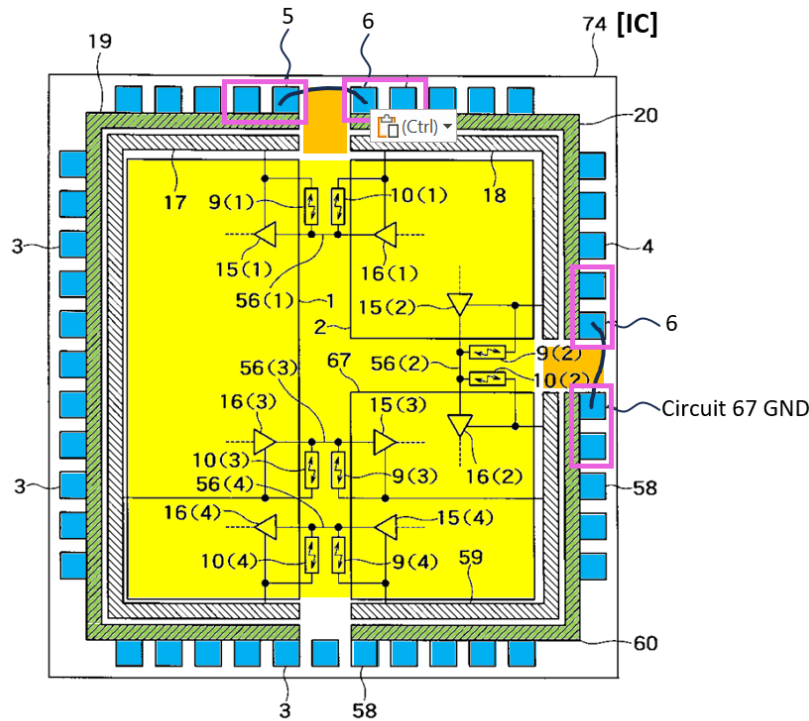
Id. at [0036] (emphasis added).

151. As can readily be seen, Beauchamp teaches both pad-to-pad connections using bond wires, and package-trace-to-package-trace connections using bond wires – in addition to the well-known (and widely-disclosed) use of bond wires to connect bond pads to package traces. Note that while Miller’s Figure 7 shows “jumper” bond wire 88A connecting ESD circuitry to driver circuitry and “jumper” bond wire 88B connecting ESD circuitry to receiver circuitry, there is nothing that prevents the connecting together of two separate instances ESD circuitry (i.e., two pad groups connected to separate ESD buses) – and a POSITA would clearly understand this. (Note also that U.S. Patent No. 7,880,310 to Mathew (Ex. 1015) discloses the use of bond wires to connect together things inside the basic IC structure – indicating that Miller and Beauchamp are not unique or unusual in disclosing the use of these basic techniques as described above.)

152. Thus, a POSITA would combine this knowledge of the art (as reflected in, for example, Miller and Beauchamp) with the layout embodiment (i.e., Figure 6

embodiment) of Yoshinaga – so as to connect together the separated ESD buses of Yoshinaga, which Yoshinaga teaches are electrically connected as shown in Figures 1-4. Moreover, a POSITA would have understood that the reference line for circuit 67 in Yoshinaga Figure 6 would likewise be connected as part of the common rail – so as to improve ESD performance in the same manner that Yoshinaga describes for circuits 1 and 2. In other words, a POSITA would understand that reference lines 19, 20, and 60 were electrically connected.

153. Thus, it would have been obvious to a POSITA to connect together the disparate ESD buses of Yoshinaga by using the POSITA's knowledge as reflected in Miller, Beauchamp, and others – that is, by using a “jumper” bond wire to connect a pad of one pad group to a pad of another pad group, across the space that intervenes between them.



154. Moreover, wire bonding was a commonplace and well-established technique (decades before the priority date of the '164 patent); therefore, a POSITA would have had a more than reasonable expectation of success in using wire bonds as described above to connect bond pads in Yoshinaga's IC. Therefore, Yoshinaga in combination the knowledge of a POSITA renders obvious this claim element of Claim 6 of the '164 patent.

f. [6e]: “wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.”

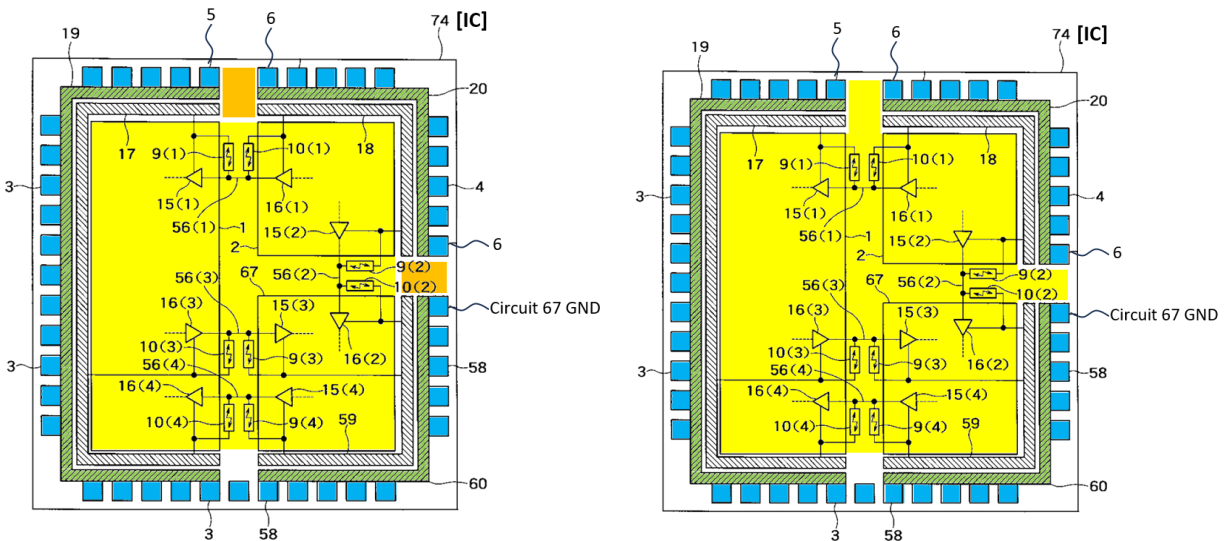
155. Yoshinaga discloses this claim element of Claim 6 of the '164 patent. Additionally, Yoshinaga combined with Saint renders this claim element obvious.

156. To simplify the analysis, this claim element will be split into claim sub-elements.

i. [6e-1]: “wherein the circuit area comprises at least one saved area”

157. This claim sub-element is disclosed by Yoshinaga, and is also rendered obvious by Yoshinaga in combination with Saint.

158. This is readily seen in an annotated version of Figure 6 of Yoshinaga (below). The orange areas depicted here (in Yoshinaga's Figure 6 embodiment, in the left-hand figure below) between the pads and power supply/reference lines disclose the “saved areas” of claim sub-element [6e-1] of Claim 6. Another way to conceptualize this is shown in a differently-annotated version of Figure 6 (on the right-hand side) – where the “saved areas” are also shown in yellow, so as to indicate that they are actually part of the available “circuit area.”



159. Therefore, Yoshinaga alone discloses this claim sub-element of claim element [6e] of the '164 patent.

160. Should YMTC argue that while Yoshinaga *depicts* instances of saved area(s) but does not *show* instances of circuitry being deployed there – and thus that Yoshinaga does not disclose this claim sub-element of claim element [6e] of the '164 patent – this argument fails for two reasons.

161. First, the claim element describes only that at least one “saved area” must be present – and does not stipulate that circuitry must actually be deployed there. The specification (e.g., at 1:40-47) suggests that the saved area could be used to provide more “flexibility for internal circuit layout design” ('164 patent at 1:42-43) – such as allowing total circuit area to be made smaller by using the available

silicon real estate more efficiently and effectively¹²; however, as noted above, the claim itself does not include any requirement that circuitry be placed in any “saved area.”

¹² It would be well-known and obvious to anyone of skill in the art (such as POSITA) that the availability of some additional “saved area(s)” could be put to different uses, depending on the needs of the particular IC being designed. Additional circuit area could be used for the inclusion of additional circuitry within the same IC footprint; alternatively, the same circuitry could be used – but some placed into the saved area(s), so that the IC footprint could be reduced. A POSITA would understand that doing so would reduce size of the die – and thus, by increasing the number of dies per wafer, reduce the cost per die. Also (as the ’164 patent describes in the specification excerpt just presented), the circuit area size (and thus the IC footprint) can be reduced by the addition of “flexibility” that would end up using the same circuitry while reducing the amount of dead space in the circuit area (due to various circuit blocks not being able to fit together with 100% circuit area coverage). All of these options are basically the same thing – amounting to how best to use the “circuit area budget” in a particular IC design. Note that here “IC footprint” means the entire IC, including the bond pads *see, e.g.*, the microphotograph from the 2010 article, above); note also that the “circuit area budget” can be used flexibly in a core-limited

162. Second, even if one accepts this argument, the use of “saved area(s)” between pad groups for circuitry was explicitly disclosed (in that form) by Saint.

163. Saint (at p. 220) describes the existence of “wasted space around the edges between the pads” – which (as will be confirmed by a figure from Saint, below) is the same thing as the orange-annotated extra space in the Figure 6 embodiment of Yoshinaga and the “saved space” of the ’164 patent. Consistent with what was said above (regarding the option of deploying some circuitry into those spaces, allowing e.g., the overall structure size to be reduced), Saint (also at p. 220) discloses that “... you can push some of your circuitry into this wasted space to try

situation – but effectively does not exist in a pad-limited situation (where there is already more circuit area available than is needed for the circuitry).

to use those gaps.” Saint shows this usage explicitly in annotated Figure 9-28^{13,14} below, where saved areas are highlighted in orange and pads are in blue.

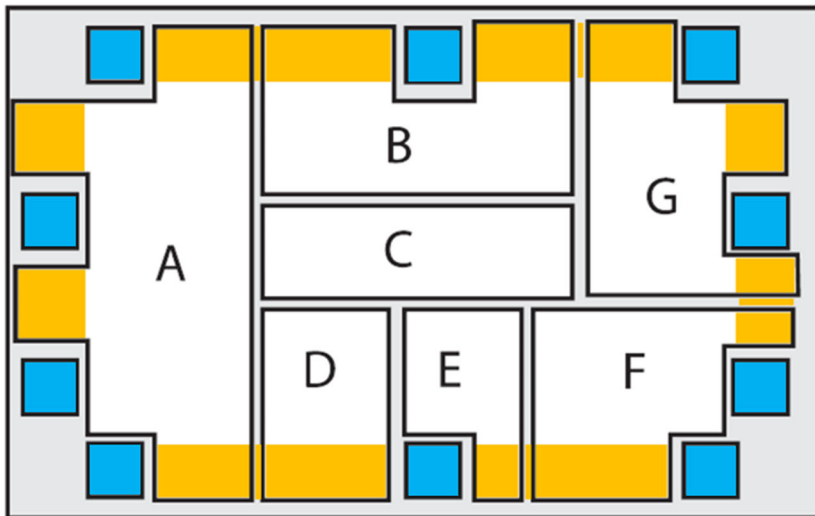


Figure 9–28. We can use extra space surrounding our pads to shrink our chip size.

As Saint explains (on p. 221), “you can re-lay parts of your circuit elements in and around these pads trying to get the chip as small as possible.”

¹³ Here, Saint shows space between individual pads; however, since (as described in Section XI.A.2.d) the ’164 patent states that a “pad group” can have just one pad, Saint’s depiction matches the ’164 patent’s description of saved space between pad groups. It would also be obvious to a POSITA that Saint’s teachings (as described here) would apply in the same way if any “pad group” had more than one pad in it.

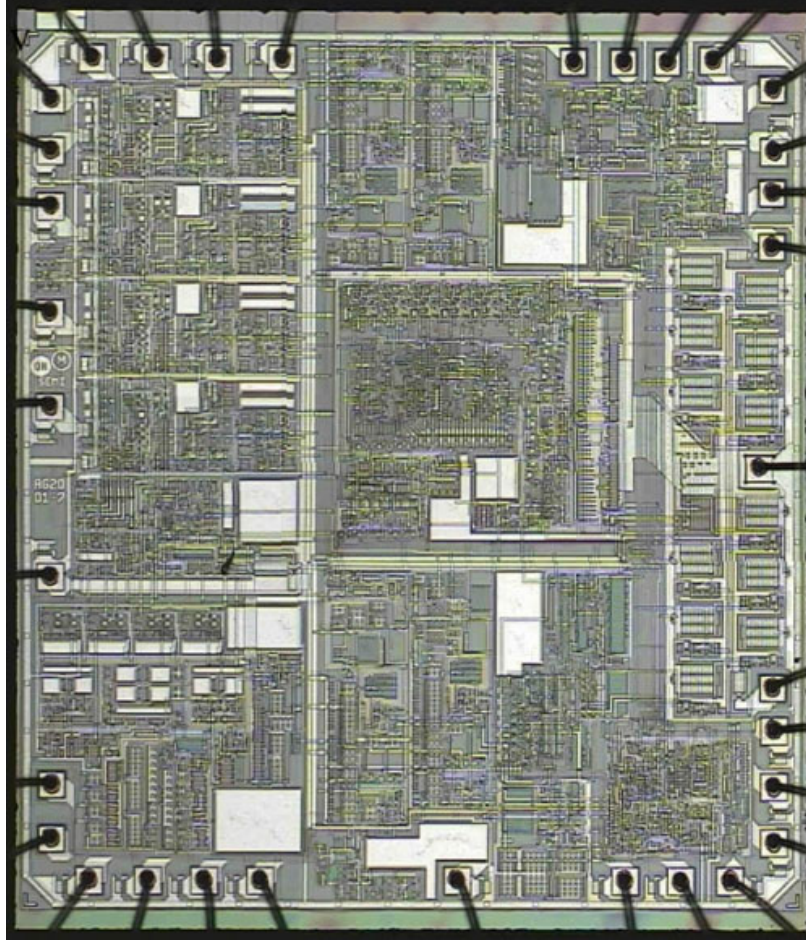
¹⁴ Note that this exemplary depiction represents an IC that is core-limited (rather than pad-limited).

164. This use of the “saved space” for circuitry is the same as what is described in the *specification* (but not the claims) of the ’164 patent. Therefore, this claim sub-element of claim element [6e] of Claim 6 of the ’164 patent is disclosed by Saint (and thus by Yoshinaga in combination with Saint).

165. For completeness, it should be noted that the use of the space between pad groups for circuitry was also broadly-known in the art. For example, the 2010 article¹⁵ mentioned earlier contains a figure (that was also shown earlier) that is a microphotograph of an IC¹⁶ that has been “torn down” so as to show its innards:

¹⁵ <https://www.sparkfun.com/news/384>.

¹⁶ Note that this actual product IC is (as is the IC in Saint’s exemplary description) core-limited.



As can be seen by simple inspection, there is circuitry deployed in the spaces between the pad groups.

166. Thus, this claim sub-element of claim element [6e] of Claim 6 of the '164 patent is disclosed and/or rendered obvious by Yoshinaga and Yoshinaga combined with Saint – along with the knowledge of a POSITA.

167. Finally, the analysis of this claim sub-element is particularly notable – since during prosecution, the Examiner allowed various claims of the application that led to the '164 patent on the grounds that “saved space” represented inventive material. In particular, the applicant amended what were at the time claims 5, 8, and

15 – so as to overcome the rejection based on Tamura (*see* Section VIII.B). In particular, the Applicant made these amendments to clarify that the “saved area” is between the non-continuous ESD buses and the non-continuous pad groups (e.g., “there is no ESD bus and no pad in the at least one saved area”). *See* Ex. 1002 at pp. 193-196 and p. 199. In particular, as mentioned above, the Applicant specifically stated that this amendment distinguished the application claims from the cited prior art: “In other words, in the instant application, at least one saved area is between the plurality of ESD buses and between the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area, which is different from Tamura’s teaching.” *See* Ex. 1002 at p. 206 (emphasis omitted). In response, the Examiner basically agreed with the Applicant’s clarifications and assertions – providing only a request for a procedural clean-up of the claims: “[m]ore descriptive details are necessary to determine what is meant by ‘saved area’ for this invention. Once clarity is successfully realized the features in [dependent] claims 5, 8 and 15 which have this (sic) features would be considered allowable if rewritten in independent form.” *See* Ex. 1002 at pp. 216-218.

168. However, as has been shown here, this is *not* inventive material – having been well-known (as shown above) in the prior art; thus, the Examiner (with all due respect) was incorrect in reaching this conclusion. For this additional reason,

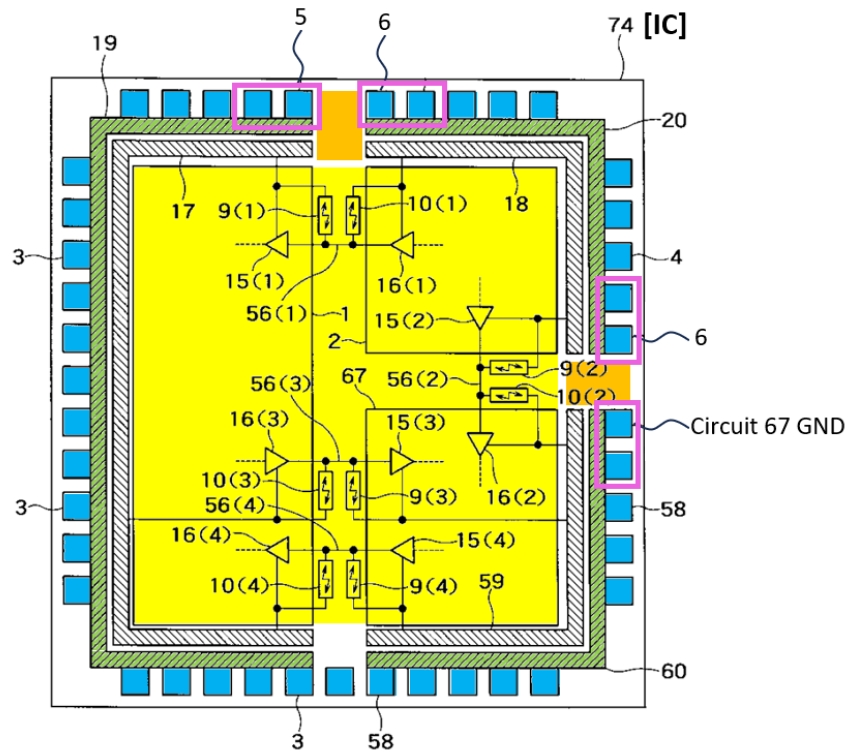
this claim sub-element of claim element [6e] of Claim 6 of the '164 patent is unpatentable.

ii. [6e-2]: “each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups”

169. This claim sub-element of claim element [6e] of Claim 6 of the '164 patent is satisfied by Yoshinaga.

170. As an initial matter, the various aspects of the phrase “saved area” were already considered above in the discussion of claim sub-element [6e-1] (in Section XI.A.2.f.i) – and will not be further-discussed here.

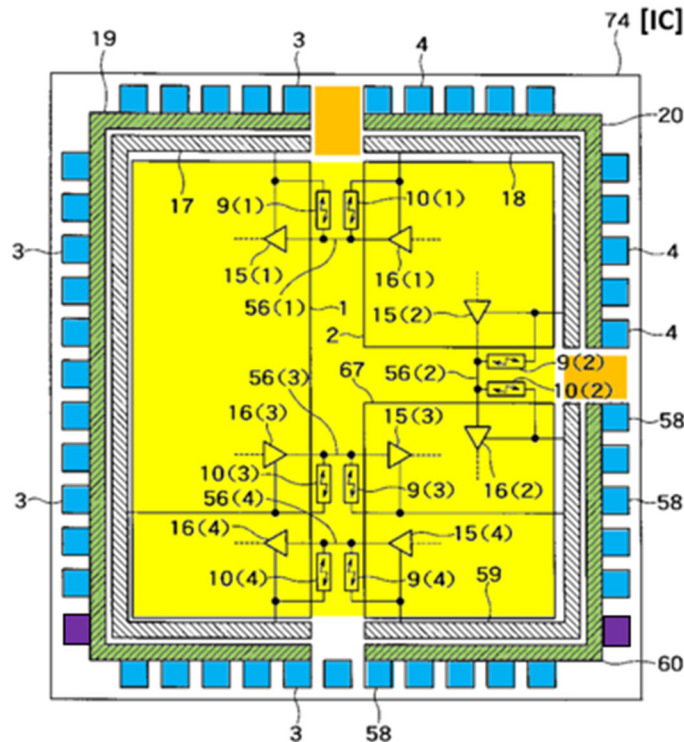
171. All remaining parts of this claim sub-element are disclosed by Yoshinaga – as can be seen by once again examining an annotated version of the Figure 6 embodiment of Yoshinaga:



The “two respective ESD buses of the plurality of ESD buses” and the “respective pads of two respective pad groups of the plurality of pad groups” – their compositions and locations – were already explained in the discussion of claim element [6c] (in Section XI.A.2.d); as can be seen, the saved areas (annotated in orange) are adjacent to these structures.

172. As noted elsewhere, although Yoshinaga Figure 6 does not identify the “[r]eference potential pads” (e.g., pads 5, 6 in Figure 2) “to simplify the drawing” (Yoshinaga,, [0078]), a POSITA would have understood that they are present in the areas shown by the blue-annotated pads “at the periphery of the chip” (*id.*, [0076])), and not located in the orange saved spaces. In Yoshinaga’s verbiage, the statement that “[r]eference potential pads are not shown [in Figure 6]” (Yoshinaga, [0078])

indicates that the reference pads are not labelled. There are many pads (highlighted in blue) that are available for use - but Yoshinaga does not label them to “simplify the drawing.” *Id.*, [0078]. In other words, the pads that are “shown” in Yoshinaga Figure 6 are simply those pads that are assigned a numeric label. When Yoshinaga intended to indicate the presence of a pad in what would otherwise be a saved space, he did so - as evidenced by the blue pad in the middle of the bottom row of Figure 6. By contrast, there are no pads depicted as being in the orange saved areas. Further, Yoshinaga’s Figure 6 floorplan is exemplary – and Yoshinaga does not describe any fixed limits on the floorplan that he presents in Figure 6. Thus, a POSITA would know that, if required, Yoshinaga’s floorplan could be expanded to include more silicon floorspace – and thus (among other things) space for additional pads. This can be roughly illustrated by adding two pads (annotated in purple) to the Figure 6 embodiment of Yoshinaga (in which the pads present in the original figure are still annotated in blue):



Yoshinaga is silent on possible design rule constraints (for a particular manufacturing process) that may apply to the amount of minimum separation allowed between a pad and, for example, the corner where the ground line 19 passes; however, a POSITA would be well-aware of the need to ensure that the pad placement complied with the design rules – and would know how to make modifications to this exemplary embodiment of Yoshinaga in the case of a real IC design (with real design rules). This demonstrates available space for more pads outside of the “saved areas,” where Yoshinaga chose not to include pad spaces.

173. Thus, this claim sub-element of claim element [6e] of Claim 6 of the ’164 patent is disclosed by Yoshinaga.

g. Claim 6 Summary

174. For all of the reasons described above, Claim 6 of the '164 patent is rendered obvious by Yoshinaga in combination with Saint and the knowledge of a POSITA.

- 3. Claim 7: “The integrated circuit structure of claim 6, wherein each of the plurality of pad groups comprises a connecting pad, and the plurality of bonding wires are configured to connect the connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups.”**

175. Claim 7 is a dependent claim, and depends from Claim 6; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.A.2) that Claim 6 of the '164 patent is rendered obvious by the references cited there and the analysis provided there.

176. With regard to Claim 7, this claim is essentially a repetition of claim element [6d] of Claim 6 of the '164 patent – with the only difference being the addition of the term “connecting pad” to identify the pads that are used to provide connections for the “jumper” bond wires that directly-connect together two bond pads (each of which is in a different pad group). As noted in the analysis of claim element [6d] (in Section XI.A.2.e), these “jumper” bond wires are depicted in Figure 3 of the '164 patent:

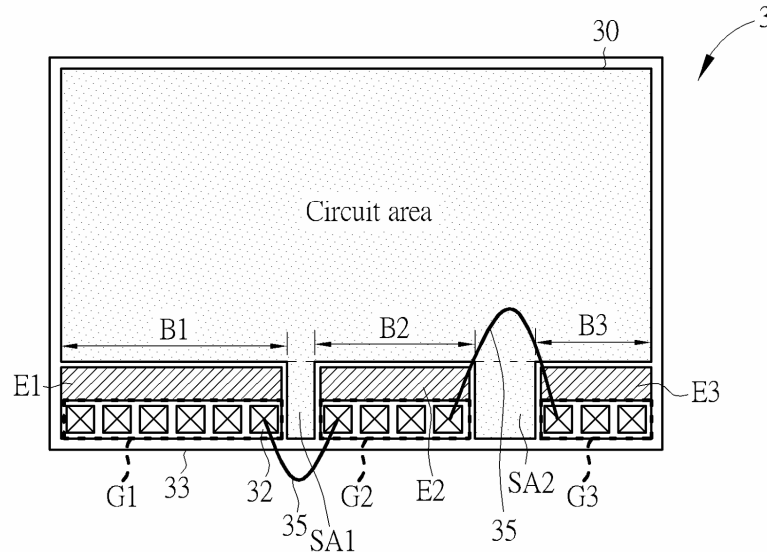


FIG. 3

As can be seen, the four depicted pads (that provide the pads for the “jumper” bond wires, two instances of 35) are used for these direct pad-to-pad connections.

177. As was described in the analysis of claim element [6d], the use of “jumper” bond wires to provide pad-to-pad connections was known in the art – disclosed, for example by both Miller and Beauchamp. In conventional practice a bond pad may have a “standard” size (to accommodate a single bond-wire connection and to meet process ground rules) – and that thus, any bond pad used for a “jumper” connection to another pad may not be available for connecting to a package trace (and thus to the package pin associated with that package trace); as explained in the analysis of claim element [6d], all of this was well-known to a POSITA at the time of the ’164 patent.

178. Thus, Claim 7 of the '164 patent is clearly about defining terminology to reflect the above reality – choosing to identify bond pads that are used solely for pad-to-pad “jumper” connections (and which are thus not available for connection to package traces) by a unique identifier. Since – as shown in the analysis of claim element [6d] – all of this was already known in the art, adding specific terminology for this is effectively meaningless.

179. Therefore, as claim element [6d] is rendered obvious by Yoshinaga in combination with the knowledge of a POSITA, Claim 7 is also rendered obvious by Yoshinaga in combination with the knowledge of a POSITA; the addition of terminology via Claim 7 provides no specific teachings – and no addition to the content of this dependent claim.

4. Claim 12

180. Claim 12 is an independent claim, and is a method claim. Further, Claim 12 is basically the method-claim version of the apparatus-claim Claim 6 – distinguished mostly by the addition of the word “forming” to the claim elements already stated in Claim 6; there are no specific or additional teachings involving particular methods used to construct the apparatus described in Claim 6. Therefore, most of the analysis of Claim 12 can simply refer to the analysis already provided above with respect to Claim 6 – with further discussion here of only the differences (between Claim 12 and Claim 6) that appear in the elements of Claim 12.

a. [Claim 12 preamble]: “A method of integrated circuit structure, comprising:”

181. As an initial matter, I will be offering no opinion regarding whether or not the preamble of claim 12 is limiting; I have been instructed by counsel for the Petitioner to assume that the preamble is limiting – and I have thus conducted my analysis using that assumption.

182. The preamble, as written, does not make grammatical sense. Counsel instructed me to assume that it reads: “A method of forming an integrated circuit structure, comprising.”

183. As per what was detailed above, Claim 12 is a method-claim version of Claim 6 – but contains no further teachings involving specific methods used to form the structure disclosed in Claim 6; therefore, for the reasons explained in Section XI.A.2.a, the preamble of Claim 12 is satisfied by Yoshinaga.

b. [12a]: “forming a circuit area;”

184. As per what was detailed above, claim element [12a] adds in the word “forming” – but is otherwise the same as claim element [6a]; as there are no further teachings involving specific methods used to form the structure disclosed in claim element [6a] (and the “circuit area” must be formed to exist), for the reasons explained in Section XI.A.2,b claim element [12a] is satisfied by Yoshinaga.

c. [12b]: “forming a plurality of ESD buses;”

185. As per what was detailed above, claim element [12b] adds in the word “forming” – but is otherwise the same as claim element [6b]; as there are no further teachings involving specific methods used to form the structure disclosed in claim element [6b] (and the “ESD buses” must be formed to exist), for the reasons explained in Section XI.A.2.c claim element [12b] is rendered satisfied by Yoshinaga.

d. [12c]: “forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are [sic] adjacent and connected to the plurality of ESD buses; and”

186. As per what was detailed above, claim element [12c] adds in the word “forming” – and the remainder of the beginning and the end of this claim element (“a plurality of pad groups ... adjacent and connected to the plurality of ESD buses”) is identical to claim element [6c]; as there are no further teachings involving specific methods used to form the structure disclosed in claim element [6c] (and the “pad groups” must be formed to exist), for the reasons explained in Section XI.A.2.d claim element [12c] is rendered obvious by Yoshinaga.

187. Besides the aforementioned inclusion of the word “forming,” claim element [12c] differs from claim element [6c] by the inclusion (which occurs in the lacuna of the quote above) of the phrase “... corresponding to a plurality of

discontinuous boundaries of the circuit area, wherein the plurality of pad groups are [sic] ...”

188. The second part of this insertion (“... wherein the plurality of pad groups are...”) can be handled first. This is actually a repetition of the earlier occurrence of the phrase “a plurality of pad groups” as “the plurality of pad groups” – but this latter phrase also stipulates that these pad groups are “adjacent and connected to the plurality of ESD buses”; this also amounts to being the same as claim sub-element [6c-1] – and thus, this part of claim element [12c] is also rendered obvious by Yoshinaga for the same reasons as discussed above respect to claim sub-element [6c-1].

189. As can thus be seen, the only extra stipulation included in claim element [12c] is that a plurality of pad groups “correspond[s] to a plurality of discontinuous boundaries of the circuit area.” Figure 2 of the ’164 patent illustrates “discontinuous” boundaries B1, B2, and B3.

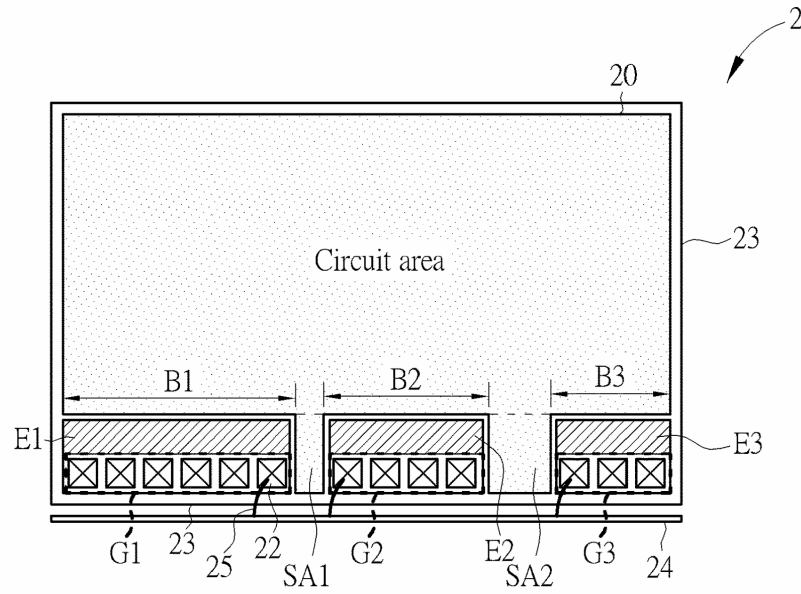
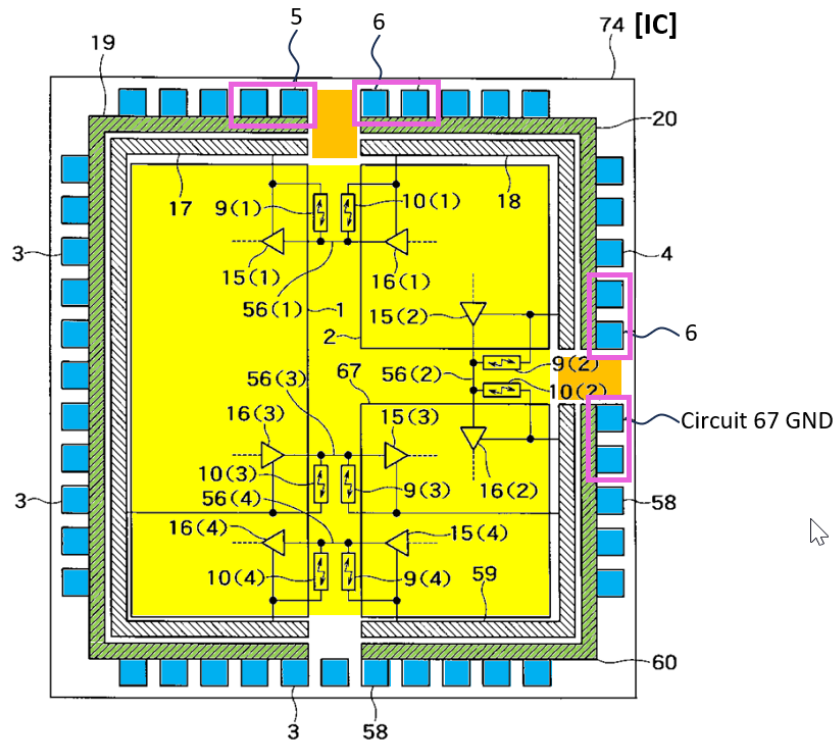


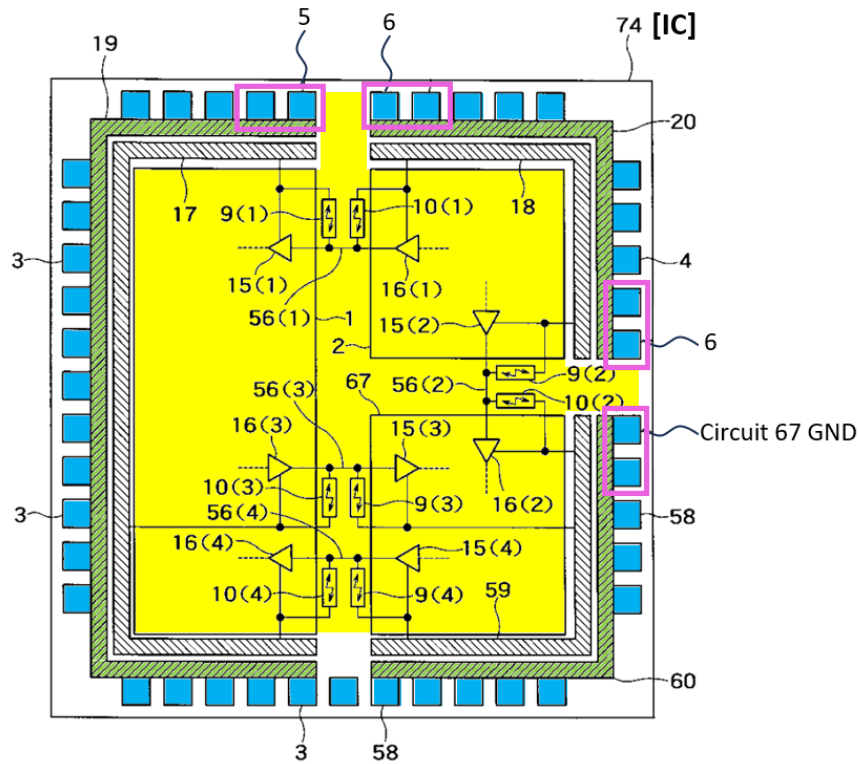
FIG. 2

190. Both Yoshinaga alone and Yoshinaga in combination with Saint disclose this aspect of claim element [12c] in the same way that it is illustrated in the '164 patent.

191. With respect to Yoshinaga alone, that Yoshinaga discloses this aspect of claim element [12c] is readily-apparent from examination of an annotated version of Figure 6 of Yoshinaga (which was presented as part of the discussion of claim element [6c-i]:



As can be seen in this annotated figure above where, the pad groups (annotated in pink) and the ESD buses (20 and 60) associated with them are all discontinuous – and there are saved areas (highlighted in orange) between the discontinuous boundaries of the pad groups and the ESD buses. As also explained in the discussion associated with claim sub-element [6e-1], the saved areas are also disclosed by Saint – and thus are also disclosed by Yoshinaga in combination with Saint. In the image below – where the circuit area in yellow is shown as including the saved areas (because circuitry can be placed there) – the claimed “discontinuous boundaries of the circuit area” are even more apparent.



192. For all of these reasons, claim element [12c], *in toto*, is rendered satisfied by either Yoshinaga alone or rendered obvious by Yoshinaga in combination with Saint.

e. [12d]: “connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires across the circuit area;”

193. It is helpful to split this claim element into two claim sub-elements.

i. [12d-1]: “connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires”

194. This claim sub-element is essentially identical to claim element [6d] (“a plurality of bonding wires configured to connect one to another of the plurality of

pad groups”) – with the language rearranged as part of here describing a method of connecting two bond pads together using a “jumper” bond wire; the language differences between claim sub-element [12d-1] and claim element [6d] do not matter – as in both instances, the same disclosure is being recited.

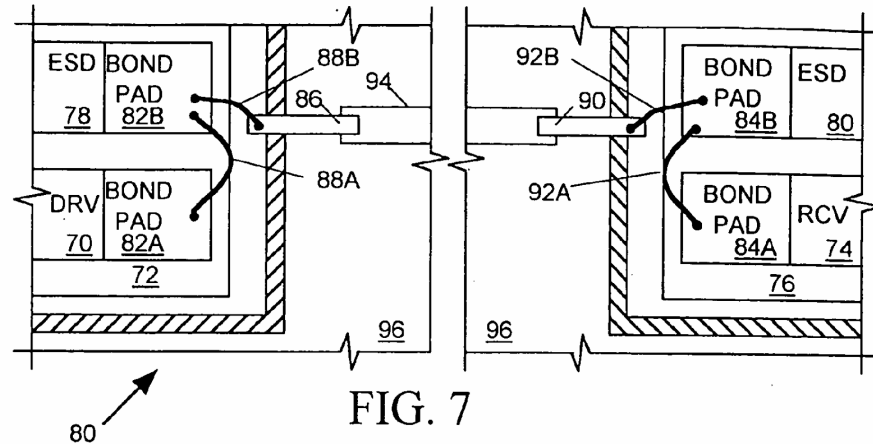
195. Thus, claim sub-element [12-d1] is disclosed by Yoshinaga in combination with Saint – for the same reasons as those provided in the analysis of claim element [6d] (in Section XI.A.2.e).

ii. [12d-2]: “across the circuit area”

196. This claim sub-element is an addition to claim element [12d-1] – which, as shown above, is essentially identical to claim element [6d]. This claim sub-element stipulates that the “jumper” bond wire that connects together two bond pads does so “across a circuit area” – which means that rather than connecting together two bond pads in the same pad group, the “jumper” bond wire connects together two bond pads where those two bond pads are each in a different pad group.

197. This claim sub-element is rendered obvious by a combination of Yoshinaga, Saint, and the knowledge of a POSITA.

198. As was discussed with respect to claim element [6d], Miller discloses connecting together two bond pads using a “jumper” bond wire:



As was explained in the discussion of claim element [6d], Miller shows how this is done – by using “jumper” bond wires (88A and 88B) to connect together, respectively, bond pads 82A-82B and bond pads 84A-84B.

199. Thus, using “jumper” wires to connect bond pads was well-known in art at the time of the priority date of the '164 patent. As was also discussed with respect to claim element [6d], Beauchamp also shows the same use of jumper wires – but with an additional disclosure that is germane here:

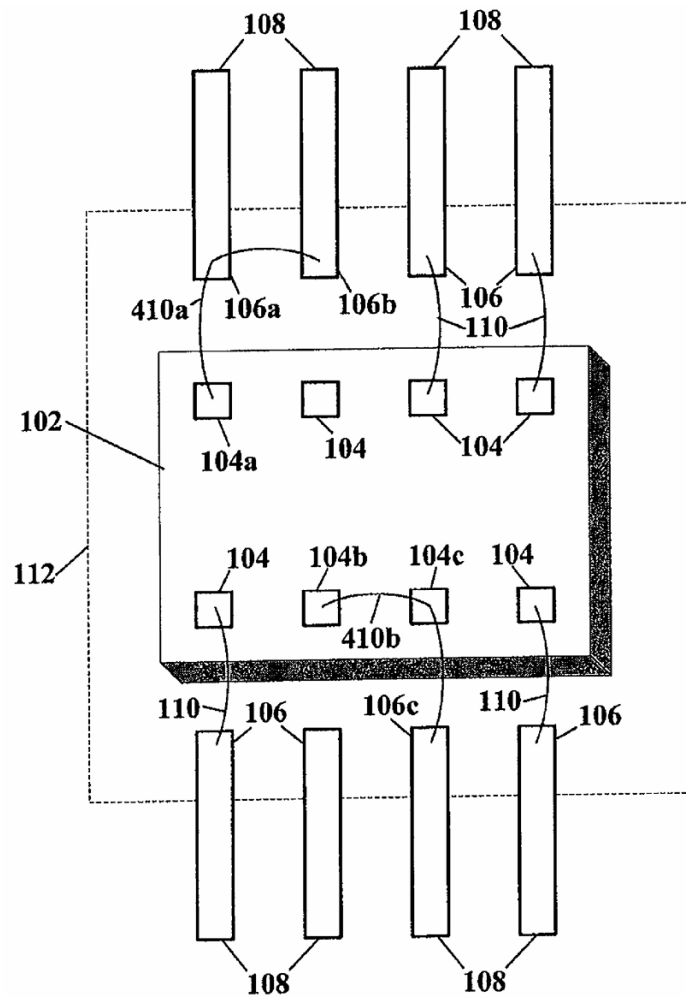
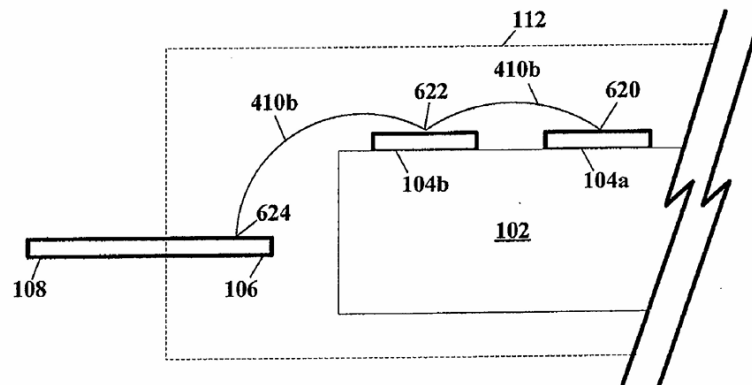


FIGURE 4



As explained in the discussion above regarding claim element [6d], Beauchamp discloses the use of bond wire to connect two bond pads together – such as the wire 410b connecting together bond pad 104b and bond pad 104c (Figure 4), and the wire 410b connecting together bond pad 620 and bond pad 622 (Figure 6). However, note also that the area between bond pad 104b and bond pad 104c (or between bond pad 620 and bond pad 622) can be treated as “saved space” (as per the teachings of Saint, such as in Figure 9-28 (p. 221)).

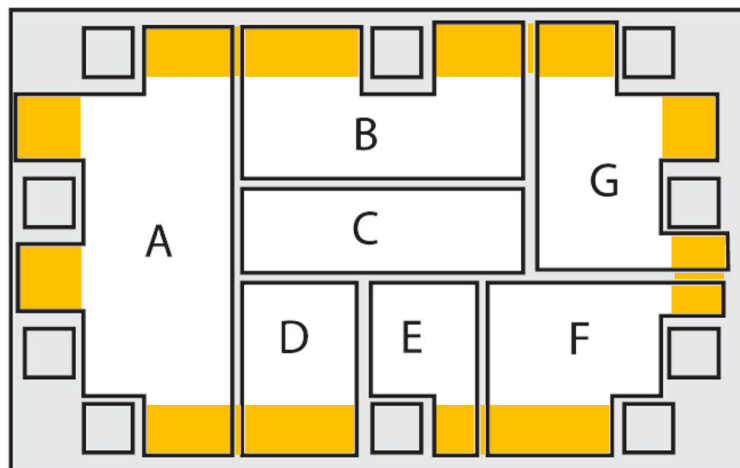
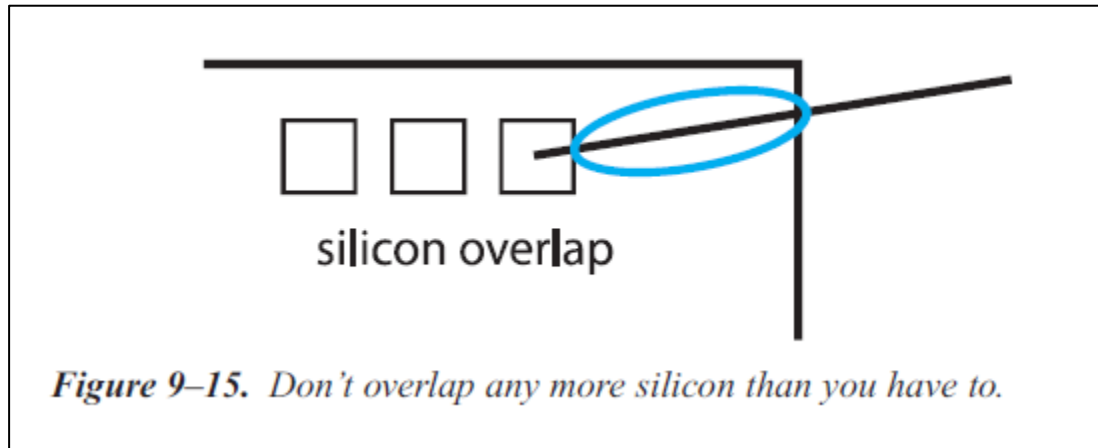


Figure 9–28. We can use extra space surrounding our pads to shrink our chip size.

(Annotations added to show the “saved areas” in orange.) In both Figure 4 (plan view) and Figure 6 (cross-sectional view) of Beauchamp, the bond wire 410b is clearly depicted as running above (i.e., across) the circuit area between two bond pads.

200. Saint also acknowledges that bond wires may “overlap[] ... the silicon” circuit area, as shown in Fig. 9-15:



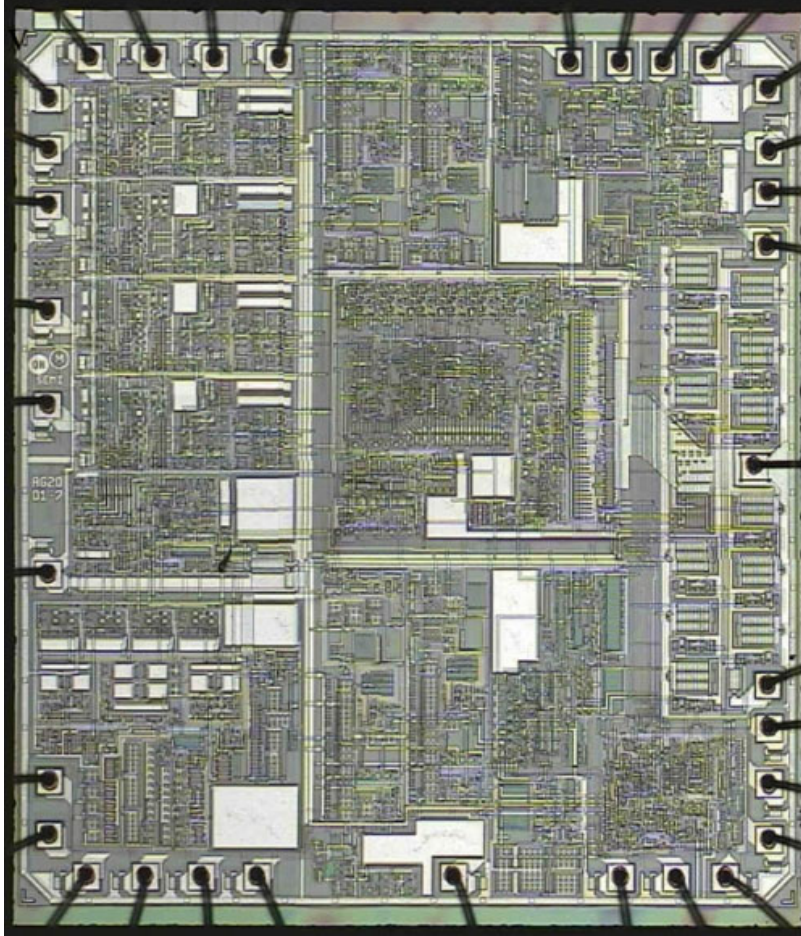
Saint, p. 209 (Fig. 9-15). Saint further teaches the desirability of “keep[ing] the overlap of the bond wire over unused silicon as short as possible.” *Id.*, p. 209; *see generally id.*, pp. 206-210. A POSITA would have understood that the shortest route between two bond pads in a segmented ground bus (like that in Yoshinaga) would be directly over the “extra space” between the bond pads. Saint further teaches that it is preferable to avoid overlapping bond wires over each other – so as to reduce the chance of overlapping wires coming into contact with each other (and creating short circuits). *Id.*, pp. 206-210. Thus, Saint’s teachings render obvious the “across the circuit area” requirement of [12d-2].

201. More generally, as noted above, using “jumper” wires to connect bond pads across a circuit area was also well-known in art at the time of the priority date of the ’164 patent – and thus would have been known and obvious to a POSITA; this

is especially the case considering that Yoshinaga teaches that his segmented reference rails share a common ground connection for improved ESD protection (while leaving the choice of a specific technique for connecting to the common ground to the discretion of the designer). Additionally, a POSITA would have found it obvious to place bond wires across the saved circuit area – because there are only two possible options for running the bond wires: over the circuit area, or not over the circuit area. Running the bond wires over the circuit area has the benefit of ensuring that they do not interfere with other bond wires which connect pads to the package traces.

202. Further, bond wires almost universally run in straight lines (as can be seen in any number of microphotographs – such one presented earlier, from a 2010 article) due to manufacturing considerations¹⁷:

¹⁷ <https://www.sparkfun.com/news/384>.



As can be seen, the bond wires run in straight lines – which is consistent with how wire bonding is carried out (using equipment specially developed for this purpose). This use of straight wiring runs is also disclosed in numerous other prior art sources – such as in Saint; for example, this can be seen via Figure 9-11 and Figure 9-19 of Saint:

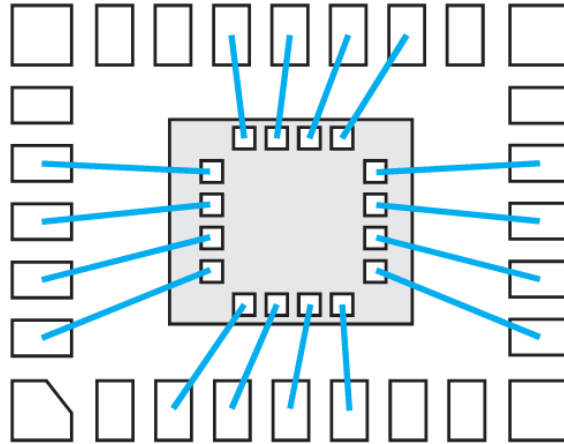


Figure 9-11. Example of a good bond-out. It looks nice, so it will work well.

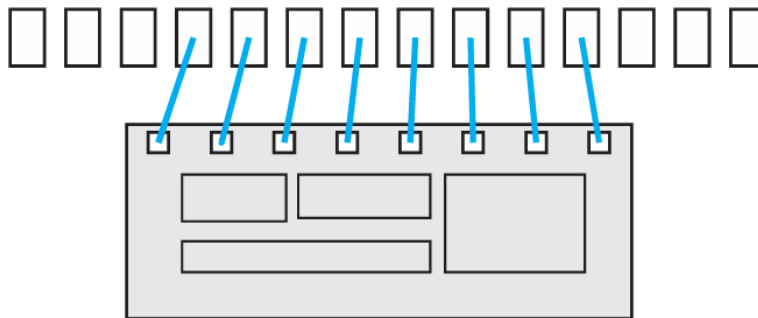
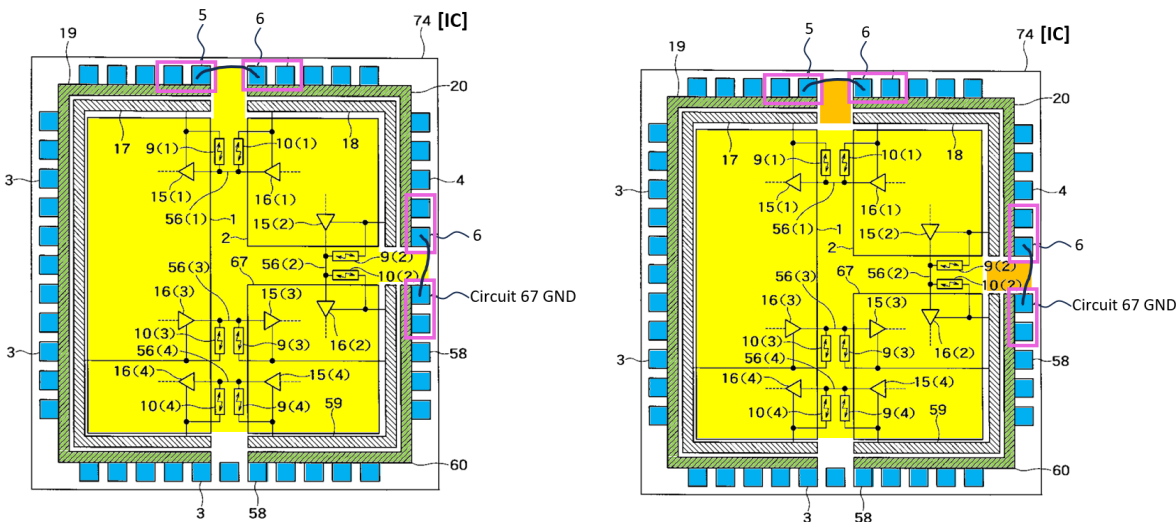


Figure 9-19. Improved pad spacing.

203. The fact that bond wires run in straight lines further supports my conclusion and opinion that when a “jumper” bond wire (as discussed in the Miller and Beauchamp references) connects two bond pads from different pad groups, the wire would run “across [i.e., above] the circuit area” – as the wire must be run in a straight line; as discussed with respect to claim sub-element [6e-1] the “saved area” portion of the “circuit area” provides the region where the “jumper” bond wire goes “across” (i.e., above) the circuit area.

204. This was already shown in the discussion of claim element [6d] – where it was shown that the Figure 6 embodiment of Yoshinaga in combination with the knowledge of a POSITA renders that claim element obvious:



The two “jumper” bond wires shown here cross above the “saved area” portion of the circuit area. As was explained with respect to claim sub-element [6e-1], the “saved area” of Yoshinaga is part of the “circuit area” of the ’164 patent – with there being no specific need (as per the claim language) for circuitry to be required to be present in the “saved area.” As was also explained in the discussion of claim sub-element [6e-1], Saint explicitly discloses the inclusion of circuitry in the “saved area(s)” between the pad groups – and this is also evident in a microphotograph of a product integrated circuit that was also provided in the discussion of claim sub-element [6e-1].

205. For all of these reasons, claim sub-element [12d-2] is rendered obvious for the reasons compiled in this discussion.

iii. [12d] Summary

206. For all of the reasons discussed above, claim element [12d] is rendered obvious by Yoshinaga, Saint, and the knowledge of a POSITA.

f. [12e]: “wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.”

207. Claim element [12e] is identical claim element [6e] – and is thus rendered obvious for the same reasons.

g. Claim 12 Summary

208. For all of the reasons described above, Claim 12 of the '164 patent is rendered obvious by Yoshinaga in combination with Saint and the knowledge of a POSITA.

5. Claim 14: “The method of integrated circuit structure of claim 12, wherein each of the plurality of pad groups comprises a connecting pad, and the plurality of bonding wires are configured to connect the connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups.”

209. Claim 14 is a dependent claim, and depends from Claim 12; thus, to the extent necessary to meet the dependence requirement, it has already been shown

above (in Section XI.A.4) that Claim 12 of the '164 patent is rendered obvious by the references cited there and the analysis provided there.

210. Further, Claim 14 is identical to claim 7 – and is thus rendered obvious for the same reasons provided for the obviousness of Claim 7 (in Section XI.A.3).

B. Ground 2—Yoshinaga, Saint, Miller, Haralabidis and the Knowledge of a POSITA

211. It is my conclusion and opinion that Claims 1-6, 8-11, and 13 of the '164 patent are rendered obvious by Yoshinaga – in combination with Saint, Haralabidis, and the knowledge of a POSITA.

1. Motivation to Combine Yoshinaga, Saint and Haralabidis

212. In Section XI.A.1, I provided an explanation of my understanding of the criteria for evaluating the conditions under which a POSITA would have been motivated to combine two or more prior art references together. Further, in that same section, I provided an explanation for why it is my conclusion and opinion that a POSITA would have been motivated to combine Yoshinaga and Saint.

213. Here, I provide a discussion of additionally combining Haralabidis with Yoshinaga and Saint – and will explain why it is my conclusion and opinion that a POSITA would have been motivated to combine Haralabidis with the two references already considered (with respect to Ground 1).

214. As in Section X.A.1, I will break this discussion up – here, into consideration of four reasons for reaching that conclusion and that opinion.

a. Haralabidis Addresses Similar Issues.

215. It can be seen by inspection that Haralabidis addresses issues and challenges that are similar to those already discussed earlier (in Section X.A.1) with respect to Yoshinaga and Saint. In particular, Haralabidis (as is clear from the title of the patent) involves ESD protection challenges; “The present application is directed to an electronic device with electrostatic discharge (ESD) ... suppression.” Haralabidis at 1:16-18.

216. Haralabidis also attempts to address the difficulties (also described by Yoshinaga) that occur when ESD buses can work against the separation of power and ground rails that is used to prevent the digital switching noise of digital circuits from propagating to the analog circuitry (and degrading the functionalities of that circuitry): “The present application is directed to an electronic device with electrostatic discharge (ESD) *and interference* suppression.” Haralabidis at 1:16-18 (emphasis added). As described (with respect to Yoshinaga) in Section X.A.1, if digital switching noise is able to propagate over to analog circuit blocks via the ESD-event-shunting paths, this defeats one of the purposes of having separate power and ground lines for digital and analog blocks.

217. In combination (of these two related challenges), Haralabidis describes the motivation of his disclosures as “[c]onventional techniques to provide electrostatic discharge (ESD) protection in electronic devices and conventional

techniques to mitigate electronic interference are insufficient. Therefore, there is a need to provide ESD techniques with improved ESD protection, and to reduce electronic interference from both internal and external sources.” Haralabidis at 1:24-29.

218. Therefore, a POSITA would have been motivated to combine Haralabidis with Yoshinaga and Saint – as Haralabidis involves issues similar to the issues addressed by Yoshinaga and Saint.

b. Haralabidis is Analogous Art to Yoshinaga, Saint, and the '164 patent.

219. Further, a POSITA would have been motivated to combine Haralabidis with Yoshinaga and Saint, because they all involve analogous art – to each other, and to the teachings of the '164 patent.

220. As all three of these references involve addressing the same challenges, many of the underlying concepts addressed in all three references are the same. For example, the teachings of Haralabidis involve the shunting of the energy of ESD events (using ESD protection circuitry) to common rails (such as power supply rails, ground rails, and reference voltage rails); *see, e.g.*, Haralabidis at the Abstract and at 1:16-2:4 – and also in Figures 3-5, which are explained in detail in the specification at 3:9-4:42. Note that this technique is also discussed in both Yoshinaga and Saint – and is also well-known in the general art, as was demonstrated in Section VII.C. As Yoshinaga, Saint, and Haralabidis each teach (or, in the case

of Saint, describe) variations on the basic underlying approach, a POSITA would understand that the differences are complementary to each other – and can readily be combined together when that is advantageous.

c. Haralabidis Teaches Architectures That Would Benefit from Combination with the Teachings of Yoshinaga and Saint.

221. As was noted in the overview of Haralabidis (in Section X.C), the teachings of Haralabidis mainly involve the effort to improve the prior art embodiment(s) of Figure 1 and Figure 3 (where the common ESD line is in the package substrate) by developing the inventive embodiment of Figure 5 (where the common ESD line is pushed further out – outside of the package substrate, and into the PCB onto which the packaged IC is mounted); the purpose of this invention is to shunt the energy of an ESD event further out from the package substrate – so as to prevent the (already-mentioned) propagation of digital switching noise to the analog blocks via the common ESD line. Haralabidis notes that while a common ground rail will be able to “ensure a solid return path for ESD protection” (Haralabidis at 2:55-56; *see, more generally, id.* at 2:55-61), if the common ground rail (used as a common ESD bus) is in the IC or in the package substrate, the problem of digital noise propagation (to the analog blocks) may still present a challenge (*see, e.g., id.* at 2:57-3:8).

222. However, a POSITA would have been motivated to use both architectures that appear in Haralabidis – both the prior art embodiment of Figure 3 and the inventive embodiment of Figure 5, depending on the circuitry architecture at hand.

223. Of particular note, Yoshinaga describes (at [0005]) how in the general prior art (that he is trying to overcome with his inventions), “one of multiple reference potential lines is used as a main ESD discharge path, and multiple reference potential lines are connected to each other” (Yoshinaga at [0005]; *see also id.* at [0009] and [0061]). The circuitry depicted in Figures 1-4 of Yoshinaga involves various incarnations of trying to address this challenge.

224. However, notably, Yoshinaga discloses no teachings that involve what happens beyond the bond pads; thus, a POSITA would clearly be motivated to combine Yoshinaga with a reference that provides details on connecting the IC (via its bond pads) to external lines that could be used as destinations for the shunted energy of any ESD events.

225. Haralabidis provides such a reference to combine with Yoshinaga – for several reasons, most of which were already discussed (to some degree) in Section X.C.

226. With regard to the (prior art) Figure 3 embodiment of Haralabidis, Haralabidis describes how such external connections (via the bond pads) can be

created for this purpose; the IC contains (internally) segmented ground rails 350 and 355 (a concept which is discussed in Saint – *see, e.g.*, Figure 7-7 of Saint), and these segmented ground rails are connected to the common ground rail (using bond pads which are connected to these rails, and wire bonding that connects those bond pads to the common ground rail) of the package substrate. (Haralabidis describes a prior art improvement to the embodiment of Figure 3 – in which a pair of “anti-parallel diodes” (480 and 485) are added (*see* Figure 4), so that the ESD performance of the circuitry can be improved; however, as Haralabidis also notes, this addition may not mitigate the problem of digital switching noise propagating to analog blocks via the ESD common bus.). However, the common line in the package substrate (of Figure 3) is still a viable option – as placing it there (rather than in the IC itself) provides the benefit of improving the robustness of the ESD protection architecture.

227. As mentioned above, the Figure 5 embodiment of Haralabidis provides inventive material – in which the location of the common ESD line is pushed out beyond the package substrate, and onto the printed circuit board (which hosts the packaged IC). Haralabidis teaches that this architecture serves to mitigate the aforementioned problem of digital switching noise propagating to the analog blocks via the common ESD line (when that common ESD line is in the package substrate).

228. As Yoshinaga requires at least one further reference to provide guidance on how to provide outside-the-IC connections for the ESD-energy shunt

paths, Haralabidis fills that gap nicely – in fact, by offering an extensive discussion of the problems that can occur when this is done, along with embodiments that depict actual circuitry for accomplishing this task.

229. Finally, it is noteworthy that while Haralabidis discusses the use of an encircling (in the shape of a rectangle) common ESD bus that is either on the PC board (Figure 5) or in the package substrate (Figure 3), Saint describes a similar encircling (in the shape of a rectangle) common ESD bus – but which is between the circuitry and the bond pads (*see* Figure CS1-99 at p. 344); this provides another option for the location of the common ESD bus – an option that could (and would) also be combined with Yoshinaga to achieve the benefits discussed above. Note also that this common ESD bus is essentially identical to the on-chip common ESD bus that appears in Figure 1 of Haralabidis; given that Haralabidis explains how its Figures 3 and 5 improve on Figure 1, a POSITA would have been further motivated to use Haralabidis' more-advantageous embodiments such as Figure 3 and Figure 5, by combining then with Figure CS1-99 of Saint.

230. Thus, a POSITA would have been motivated to combine Yoshinaga, Saint, and Haralabidis – because Haralabidis teaches architectures that can be combined with the teachings of Yoshinaga and Saint.

d. A POSITA Would Have Had a Reasonable Expectation of Success in Making These Combinations.

231. Finally, a POSITA would have had a reasonable expectation of success in combining these three references – and would have been able to do so without undue experimentation.

232. As noted above, Yoshinaga discusses the need to provide ESD shunt path connections (such as using a common reference line) to his circuit designs – but provides no specific teachings on how to do this. Haralabidis provides simple circuit instructions for providing the circuitry that can perform these functions – and this circuitry involves simple ohmic connections (using wires and similar); in fact, as noted earlier, the Figure 3 embodiment of Haralabidis is identified (by Haralabidis) as being “Conventional Art” (*see* the Figure 3 caption; *see also* the Figure 4 caption). Further, in the specification, Haralabidis describes the Figure 3 embodiment as being “conventional” (at 3:9), and the Figure 4 embodiment as also being “conventional” (at 3:34); (*see also, generally*, 3:9-64). Thus, the circuitry of these embodiments was already known in the art, used “convention[ally]” – and therefore was known to work properly; thus, a POSITA would have had a reasonable expectation of success in implementing these architectures, and would have been able to do so without undue experimentation.

2. Claim 13: “The method of integrated circuit structure of claim 12, wherein a common ESD bus is parallel to the plurality of ESD buses and the plurality of pad groups.”

233. The combination of Yoshinaga, Saint, and Haralabidis renders Claim 13 obvious. Claim 13 is a dependent claim, and depends from Claim 12; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.A.4) that Claim 12 of the ’164 patent is rendered obvious by the references cited there and the analysis provided there. I thus begin the analysis of Ground 2 with an analysis of Claim 13 – because I have already discussed independent Claim 12 on which Claim 13 depends (immediately above).

234. Further, Claim 13 is a method claim; however, as in multiple situations considered above (particularly in Ground 1), there are no further teachings involving specific methods used to form the structures disclosed in Claim 13. Thus, there is nothing about Claim 13 being a method claim that otherwise distinguishes it from the apparatus claims that will be cited below for the analysis.

235. Claim 13 requires “a common ESD bus ...” While not illustrated in Yoshinaga Figure 6, Yoshinaga explains that “multiple reference potential lines are connected to each other” to provide “a main ESD discharge path.” Yoshinaga, [0005]; *see also id.*, [0009], [0061], Figs. 1-4. In other words, a POSITA would recognize that Yoshinaga discloses a common ESD bus.

236. Yoshinaga explains that the reference voltage lines for each circuit block (*e.g.*, circuit 1, circuit 2, etc.) are connected so as to provide more robust ESD protection; however, Yoshinaga does not teach any specific technique or implementation for connecting the otherwise-separate ground rails. Yoshinaga, Figs. 1-4, [0005], [0009], [0061].

237. Haralabidis discloses that including a “package common ground rail 360” around an IC was “conventional” (with the implementation being shown in Figure 3, as presented below). *See* Haralabidis, 3:9-18. Haralabidis explains that one use of his common ground rail is to provide the rail to which the energy of an ESD event is shunted – so as to provide ESD protection for the IC circuitry.

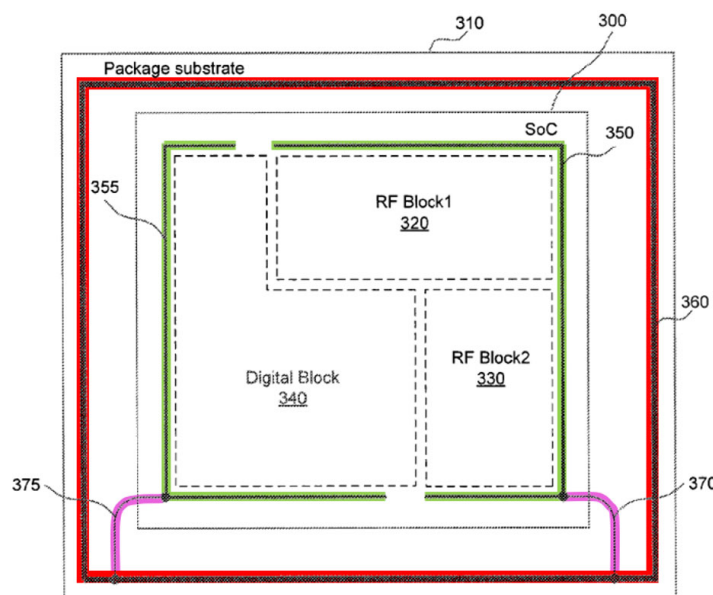
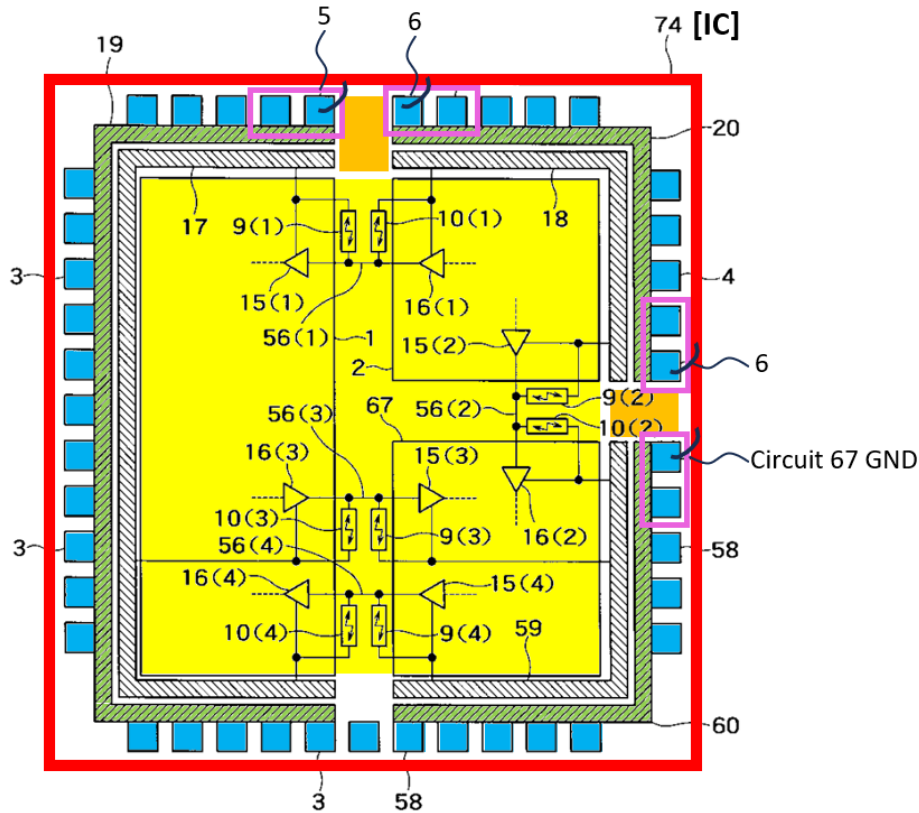


FIG. 3
Conventional Art

Id., Fig. 3 (annotated to show the “package common ground rail 360” in red and connections thereto in magenta). Haralabidis’ common ground rail connects

“segmented ... ground rails 350, 355” through the connections labeled 370 and 375. *Id.*, 3:9-18. As described in Haralabidis (and as detailed in Section X.C), the green-annotated rails (350 and 355) are the “segmented” ground rails (of the IC interior), while the red annotated rail (360) is the common ground rail that is part of the package substrate; as can also be seen by inspection (and as was described in Section X.C), the segmented ground rails (350 and 356) are connected to the common ground rail (360) via (respectively) the magenta-annotated wiring lines 370 and 375. Haralabidis further teaches that the connections 370 and 375 (shown in pink) can be bond wire connections. *Id.*, 1:65-2:4.

238. Combining Haralabidis’ teachings of a common ground teaching with Yoshinaga’s Figure 6 embodiment would result in the IC embodiment shown below. One reason that this combination would have been obvious to a POSITA is because Haralabidis’ common ground was “conventional” – and Yoshinaga already teaches that his reference rails connect to one another. One result of using a common rail is that doing so allows all circuits to source the reference voltage from the same line – and thus, the printed circuit board can provide a single common line that will be provided to all internal IC circuits.



Yoshinaga, Fig. 6 (annotated, common rail added in red). Of course, the common ground would serve no purpose to the IC if it were not connected to the individual ground rails. Given that Haralabidis discloses such connections (e.g., connections 370 and 375) using bond wires, a POSITA would have found it obvious to do the same in Yoshinaga – by making the same of connections to the existing bond pads. *See Haralabidis, 1:61-2:4, Fig. 3 (connections 370 and 375).*

239. The second part of Claim 13 requires that the common ESD bus be “parallel to the plurality of ESD buses and the plurality of pad groups.” The common ESD bus (annotated in red above) is parallel to both the segmented buses and the pad groups on any of the four sides of the structure of the combined embodiment of

Yoshinaga Figure 6 and Haralabidis. While Yoshinaga only shows two segmented buses (and their associated pad groups) on a single edge of a chip, it would have been obvious to have three (or more) such buses (and their associated pad groups) on the same chip edge - in which case they too would meet the “parallel” requirement.

240. For completeness, it can be noted that Saint provides a description (of a common ESD bus) that is similar to the Figure 3 disclosure of Haralabidis; this description in Saint would thus satisfy claim 13 for the same reasons. This description in Saint is contained in Figure CS1-99 (on p. 344):

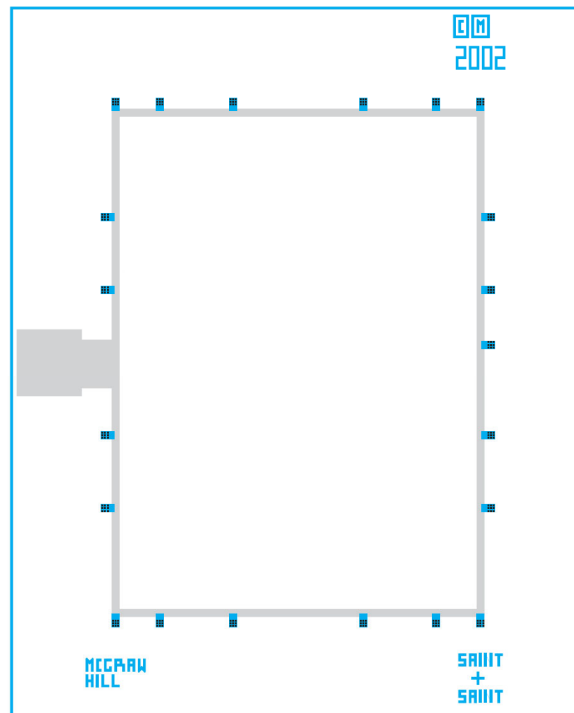


Figure CS1-99

The text associated with this figure describes the figure as depicting “ESD Ground Wiring,” and further explains that “This simplified plot shows the ground wires

associated with the ESD protection system. Notice that this wire creates a continuous ring around the active circuitry.” Saint at p. 344. This continuous ring of ground wires associated with the ESD protection system provides a description of a common ESD bus that is effectively identical to the one described (as detailed above) by Haralabidis – and would yield the same result.

241. Therefore, Claim 13 in *toto* is rendered obvious by Yoshinaga in combination with Saint and Haralabidis.

3. Claim 1

242. Claim 1 is an independent claim, and is an apparatus claim.

a. [1-pre]: “An integrated circuit structure, comprising:”

243. As an initial matter, I will be offering no opinion regarding whether or not the preamble of Claim 1 is limiting; I have been instructed by counsel for the Petitioner to assume that the preamble is limiting – and I have thus conducted my analysis using that assumption.

244. The preamble of Claim 1 is identical to the preamble of Claim 6; thus, for the reasons already discussed (in Section XI.A.2.a), Yoshinaga renders obvious the preamble of Claim 1 of the ’164 patent.

b. [1a]: “a circuit area;”

245. Claim element [1a] is identical to claim element [6a]; thus, for the reasons already discussed (in Section XI.A.2.b), Yoshinaga renders obvious this claim element of Claim 1 of the '164 patent.

c. [1b]: “a plurality of ESD buses;”

246. Claim element [1b] is identical to claim element [6b]; thus, for the reasons already discussed (in Section XI.A.2.c), Yoshinaga renders obvious this claim element of Claim 1 of the '164 patent.

d. [1c]: “a plurality of pad groups, adjacent and connected to the plurality of ESD buses;”

247. Claim element [1c] is identical to claim element [6c]; thus, for the reasons already discussed (in Section XI.A.2.d), Yoshinaga renders obvious this claim element of Claim 1 of the '164 patent.

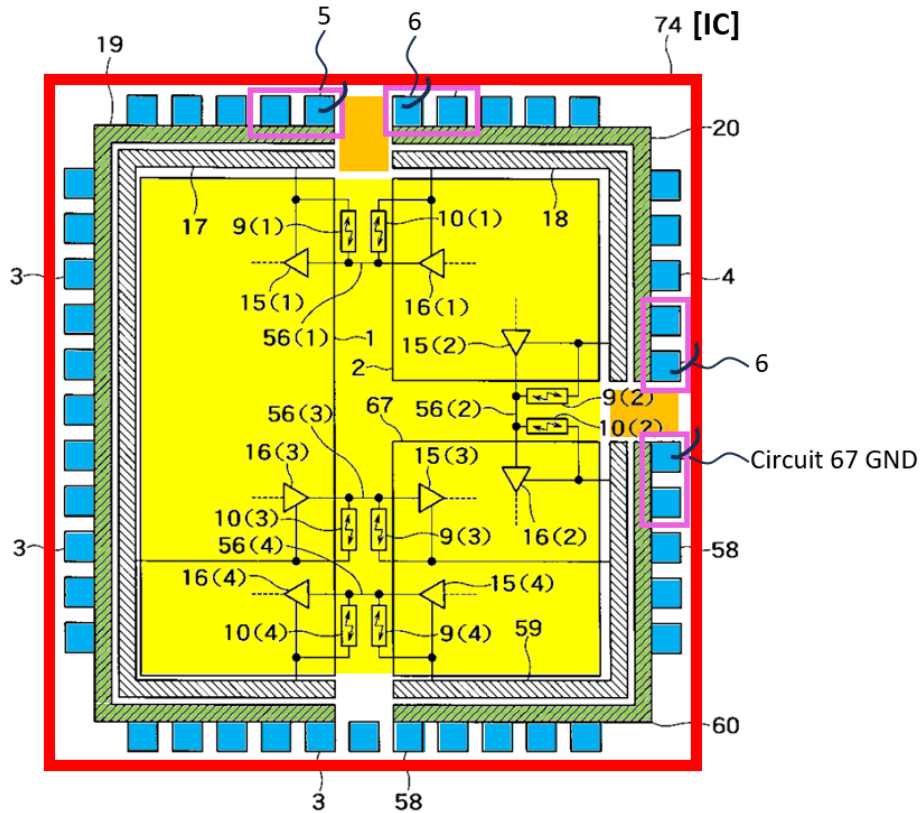
e. [1d]: “a common ESD bus, adjacent to the plurality of pad groups; and”

248. As an initial matter, this claim element uses the word “adjacent” – and, as noted in Section XI.A.2.d.ii, the specification provides no specific definition of this word; thus, once again, the plain-and-ordinary meaning of this term should be assumed. As also noted in Section XI.A.2.d.ii, the '164 patent offers no specific definition of the word “adjacent”; thus, plain-and-ordinary meaning should be

assumed. As in Section XI.A.2.d.ii, a dictionary definition¹⁸ of “adjacent” that is germane to this situation includes either “not distant: nearby” or “having a common endpoint or border.” This definition of “adjacent” will be used for the analysis to be described here.

249. As a further initial matter, claim element [1d] is actually nearly-identical to Claim 13 element, except that the claimed “common ESD bus” in [1d] is “adjacent to,” instead of “parallel to,” the pad groups. This “adjacent to” requirement is satisfied by Yoshinaga in combination with Haralabidis and Saint, as can be seen in the annotated version of Yoshinaga Fig. 6 below, which was used for the analysis of Claim 13.

¹⁸ <https://www.merriam-webster.com/dictionary/adjacent>.



250. Therefore, Yoshinaga in combination with Haralabidis renders obvious this claim element of Claim 1 of the '164 patent.¹⁹

¹⁹ Note that while the Figure 3 embodiment of Haralabidis was here combined with the Figure 6 embodiment of Yoshinaga, the claim element would also be disclosed by combining the Figure 5 embodiment of Haralabidis with the Figure 6 embodiment of Yoshinaga; as will be explained below (in the discussions of Claim 3 and Claim 4), only Claim 3 and Claim 4 include more-detailed stipulations in the claim language – specifying that the common ESD bus must be comprised of multiple discontinuous segments (rather than by a single line) in Claim 3, and that the

f. [1e]: “a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus;”

251. In the discussion presented earlier regarding claim element [6d] (in Section XI.A.2.e), it was noted that whatever provision is made for connecting together ESD shunting-destination lines (such as ground lines), these lines must be connected to a path that provides a sink for the energy of an ESD event – such as a to a package pin that serves as a “pickup pin” for all of the ESD shunt-destination lines. Thus, in-and-of itself, it would be obvious to a POSITA that such a provision would have to be made – for the evacuation of the energy an ESD event from the IC itself via some connection to a package pin (or similar – such as multiple package pins).

252. This functionality is described by Haralabidis in Figure 3 – as was actually already described in association with the discussion above of claim element [1d]:

common ESD must be either inside the plurality of chips edges or outside of the plurality of chip edges in Claim 4.

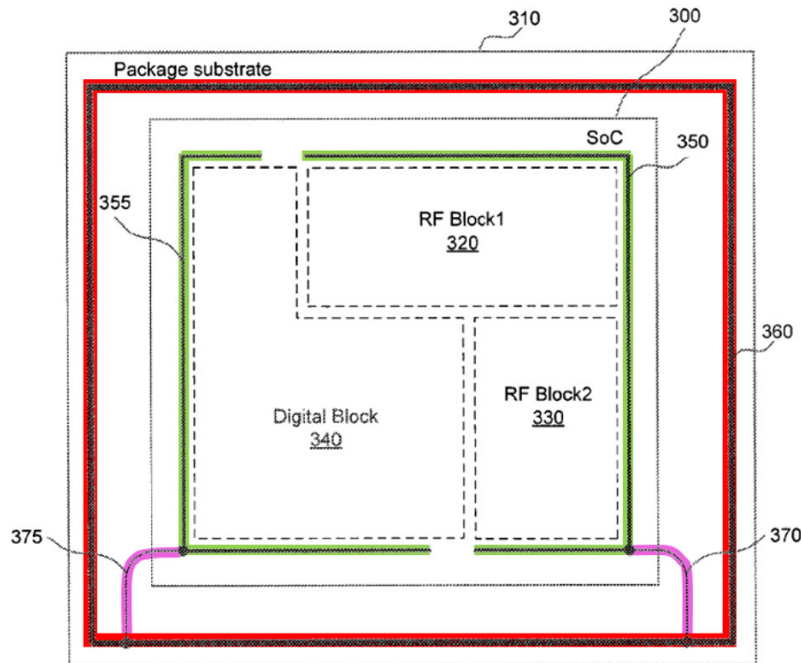


FIG. 3
Conventional Art

Haralabidis, Fig. 3 (annotated). As Haralabidis describes the segmented ground lines (350 and 355) as being inside the IC, while the common ground line (360) is part of the package substrate, it would be obvious to a POSITA that the most-commonly-used way to connect the segmented ground lines (350 and 355) to the common ground line of the package substrate would be via bond pads and bond wires – which is the standard technique used to connect the IC circuitry to the package pins.

253. That this is the standard technique that is used to connect IC circuitry to package pins is described by Saint; e.g.,

To get signals from the chip circuitry to the package pins, thin wires join the bond pads on the chip to the inside²⁰ portion of the metal pins.

Saint, p. 202. Further, Haralabidis describes the use of such connections:

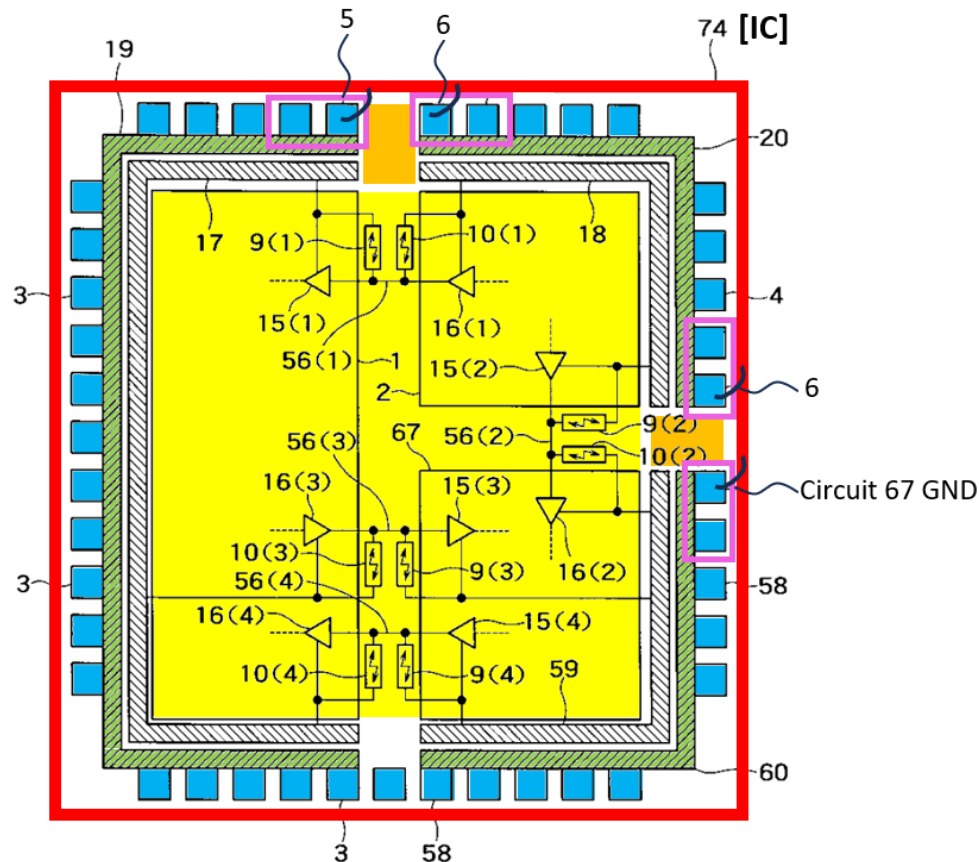
The plurality of circuit blocks have [sic] corresponding ground nodes electrically coupled to corresponding segments of the IC ground rail. Further, the segments of the IC ground rail are coupled to corresponding segments of the package ground rail by corresponding first electrical connections that could be, for example: *wirebonds*, solder bumps, solder balls, and the like.

Haralabidis, 1:59-65 (emphasis added). Thus, Haralabidis also describes the use of this specific technique for the purposes described above – with “solder bumps, solder balls, and the like” describing more- involved techniques²¹ of connecting IC circuitry to package pins (techniques which have been developed to address the need for more pins for connections to complex ICs).

²⁰ As the surrounding discussion in Saint makes clear, “inside” here refers to “inside the package.”

²¹ Note that the ’164 patent discusses only the use of bond wiring, and none of these more-involved methods.

254. It would thus be obvious to a POSITA to connect the pads/pad-groups of the Figure 6 embodiment of Yoshinaga to the common ESD bus (of Haralabidis, which was shown to be an obvious combination with Yoshinaga in the discussion above of claim element [1d]) using bond wires as described by Haralabidis and Saint:



Yoshinaga, Fig. 6 (annotated).

255. Thus, this claim element of Claim 1 of the '164 patent is rendered obvious by Yoshinaga in combination with Haralabidis, Saint, and the knowledge of a POSITA.²²

g. [1f]: “wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.”

256. Claim element [1f] is identical to claim element [6e]; thus, for the reasons already discussed (in Section XI.A.2.f), Yoshinaga renders obvious this claim element of Claim 1 of the '164 patent.

h. Claim 1 Summary

257. For all of the reasons described above, Claim 1 of the '164 patent is rendered obvious by Yoshinaga in combination with Saint, Haralabidis, and the knowledge of a POSITA.

²² Note again that as Saint is a textbook (and not a patent), it to a large degree provides a compilation of the knowledge of a POSITA at the time of its publication (2002).

- 4. Claim 2: “The integrated circuit structure of claim 1, wherein each of the plurality of pad groups comprises at least one pad, and the plurality of bonding wires is configured to connect the at least one pad to the common ESD bus.”**

258. Claim 2 is a dependent claim, and depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.B.3) that Claim 1 of the '164 patent is rendered obvious by the references cited there and the analysis provided there.

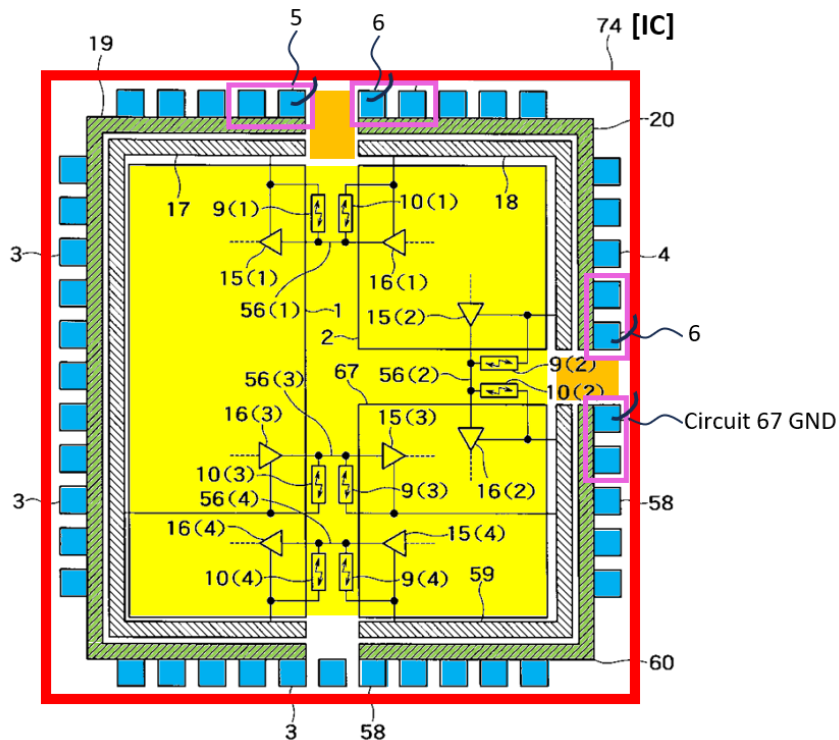
259. Further, Claim 2 provides material that was already provided in (and discussed above with respect to) claim elements [6c], [1d], and [1e] – and thus, Claim 2 (as will be confirmed below) is rendered obvious by Yoshinaga in combination with Haralabidis and Saint.

260. With detailed regard to Claim 2, it is helpful to break this claim into separate elements – for separate analysis.

a. [2a]: “wherein each of the plurality of pad groups comprises at least one pad”

261. It was shown in the discussion of claim sub-element [6c-1] (in Section XI.A.2.d.i) that this claim element is rendered obvious by Yoshinaga.

262. As shown in that discussion²³, Yoshinaga discloses pad groups – as can be seen in an annotated version of Figure 6 of Yoshinaga:



The pad groups of Yoshinaga are annotated in red.

263. Thus, Yoshinaga renders obvious this claim element of Claim 2 of the '164 patent.

²³ As also noted via a footnote included with that discussion, the specification also states that a pad group contains “at least one pad” (at 3:6-7); therefore, a “pad group” could consist of only one pad – and thus a single pad in a prior art reference would also amount to a disclosure of a “pad group.”

b. [2b]: “and the plurality of bonding wires is configured to connect the at least one pad to the common ESD bus”

264. This claim element was actually already considered (in separate pieces) with respect to claim element [1d] (Section XI.B.3.e) and claim element [1e] (Section XI.B.3.f) – where it was shown that claim element [1d] is rendered obvious by Yoshinaga in combination with either Haralabidis or Saint, while claim element [1e] is rendered obvious by Yoshinaga in combination with Haralabidis, Saint, and the knowledge of a POSITA.

265. That a “common bus” is rendered obvious was explained with respect to claim element [1d], while the use of bonding wires to connect at least one pad of a pad group to the common ESD bus was explained with respect to claim element [1e] (and its being rendered obvious). While Haralabidis depicts the connections to-and-from the segmented and common ESD buses as simple (undescribed) ohmic connections (which may or may not include bond pads – the specific technique used to create the aforementioned ohmic connections is not discussed by Haralabidis), a POSITA would have found it obvious to utilize Yoshinaga’s existing bond pads given their placement between the segmented ground rails and the common ground rail. More generally, it was very well-known in the art (and thus to a POSITA) that one common way to create a bond wire connection was to connect bond wires to bond pads as is shown in Miller Figs. 1, 4, 7, 10, 13, and 14, Beauchamp Figs. 1-8, and Saint, pp. 202-211 (showing and discussing bond wire connections to bond pads,

including “Ultrasonic Wedge Bonding” and “Ultrasonic Ball Bonding” techniques). Thus, the knowledge of a POSITA also renders obvious connecting a bond wire to a bond pad - especially where existing bond pads are already available.

266. Therefore, claim element [2b] of Claim 2 of the ’164 patent is rendered obvious by Yoshinaga in combination with Haralabidis, Saint, and the knowledge of a POSITA.

c. Claim 2 Summary

267. Therefore, Claim 2 of the ’164 patent is rendered obvious by Yoshinaga in combination with Haralabidis, Saint, and the knowledge of a POSITA.

5. Claim 3: “The integrated circuit structure of claim 1, wherein common ESD bus comprises a plurality [sic] discontinuous ESD bus groups.”

268. Claim 3 is a dependent claim, and depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.B.3) that Claim 1 of the ’164 patent is rendered obvious by the references cited there and the analysis provided there.

269. The specific teaching of this claim – that the common ESD comprises a plurality of discontinuous ESD bus groups – is disclosed by Haralabidis. Referring back to the discussion of the definition of “discontinuous” that was provided during analysis of claim element [12c] in (Section XI.A.4.d), a similar use of “discontinuous” applies here for Claim 3 - except that “discontinuous ESD bus

groups” refers to a bus that is physically discontinuous but electrically common (as illustrated in the ’164 patent).

270. As was explained in the overview of Haralabidis (in Section X.C) Haralabidis discloses an inventive embodiment (Figure 5) in which – in addition to the internal IC ground lines (which as used for receiving the energy of an ESD event) being segmented – the package substrate ground line (which is also used for receiving the energy of an ESD event) is also segmented (rather than being a single line, as was the case in Figure 3); the segments of the package substrate ground line are connected to a common ground line on the PC board (to which the packaged IC is mounted).

271. This can readily be seen in an annotated version of Figure 5 of Haralabidis:

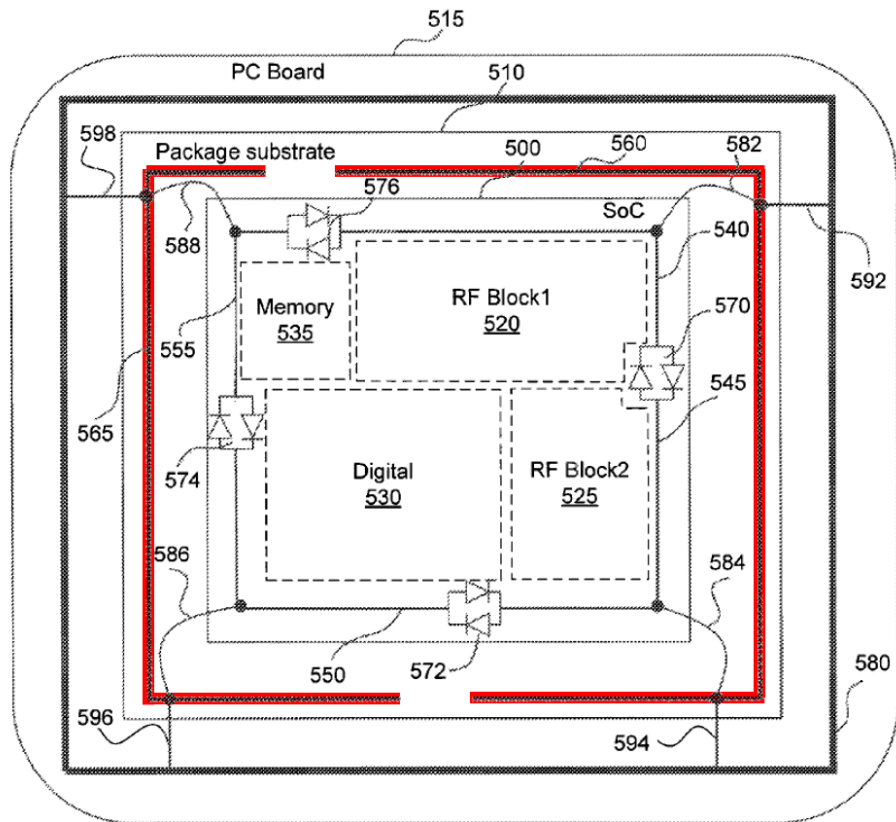


FIG. 5

The segmented lines of the ground lines (ESD bus segments) in the package substrate (560 and 565) provide a “common ESD bus” that “comprises a plurality” of “discontinuous ESD bus groups.”

272. Finally, as the simple single-line package-substrate bus was shown to be readily used in Yoshinaga’s Figure 6 embodiment (in claim element [1d], discussed in Section XI.B.3.e), in the same way it would be obvious to a POSITA to use this segmented package-substrate bus in Yoshinaga’s Figure 6 embodiment – and that, as in Haralabidis Figure 5, this segmented bus can be connected to the common single-line ESD bus on the PC board to which the IC is mounted.

273. Therefore, Yoshinaga in combination with Saint and Haralabidis renders obvious Claim 3 of the '164 patent.

6. Claim 4: “The integrated circuit structure of claim 1, wherein the common ESD bus is formed outside the plurality of chip edges or inside the plurality of chip edges.”

274. Claim 4 is a dependent claim, and depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.B.3) that Claim 1 of the '164 patent is rendered obvious by the references cited there and the analysis provided there.

275. The specific teaching of this claim actually involves two possible descriptions of the location of the common ESD bus – and separates them with an “or.” Therefore, if a prior art reference is able to disclose either description, then this claim is rendered obvious; however, *both* descriptions are disclosed in the prior art references being used for this analysis.

276. The first option “the common ESD bus is formed outside the plurality of chip edges” is disclosed by Haralabidis – in two separate instances, both of which were described above.

277. As was discussed with respect to claim element [1d] (in Section XI.B.3.e), the Figure 3 embodiment of Haralabidis discloses this first option of the claim:

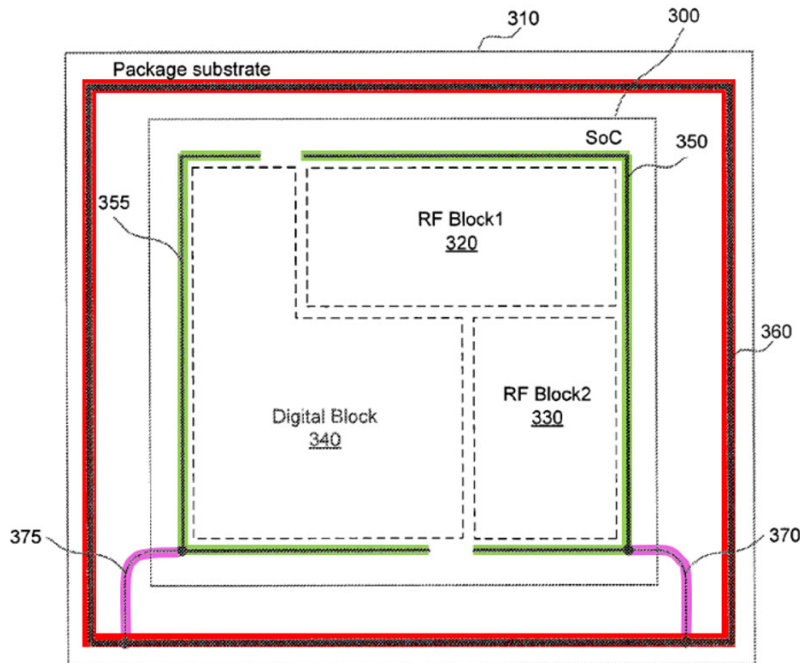


FIG. 3
Conventional Art

Haralabidis, Fig. 3 (annotated). As described in the discussion of claim element [1d], the common ESD bus (360 – which here is a single line) is part of the package substrate – and therefore is outside of the chip (and thus outside of the plurality of chip edges). For completeness, it should be noted that if the teachings of the '164 patent are interpreted in a manner in which the “chip” is considered to include the package substrate, then the common ground that Haralabidis places in the package substrate would be considered to be “inside the plurality of chip edges” – and would also satisfy the “second option” of Claim 4.

278. As was discussed with respect to Claim 3 (in Section XI.B.5), the Figure 5 embodiment of Haralabidis also discloses the first option of the claim:

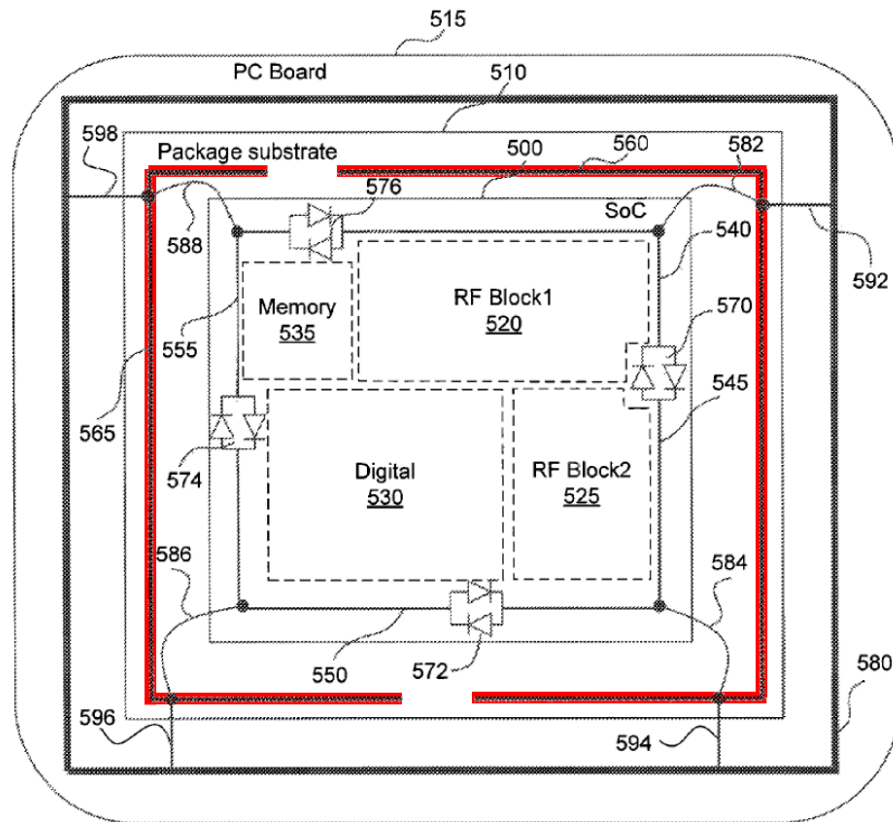


FIG. 5

Haralabidis, Fig. 5 (annotated). Here, as described in the discussion of Claim 3, the common ESD bus (which here is segmented into two lines – 560 and 565) is part of the package substrate – and therefore is also outside of the IC (and thus outside of the plurality of chip edges).

279. Note that this Claim simply refers to “the common bus” – and as no further details are provided, either the single-line ESD bus of Figure 3 or the segmented-line ESD bus of Figure 5 discloses the first option of the Claim.

280. Therefore, Haralabidis discloses Claim 4 of the ’164 patent – by disclosing the first of the two options listed.

281. With regard to the second option (“the common ESD bus is formed ... inside the plurality of chip edges”), this option is disclosed by Saint – as was also described above.

282. As was discussed with respect to claim element [1d] (in Section XI.B.3.e), Saint discloses this second option of the claim:

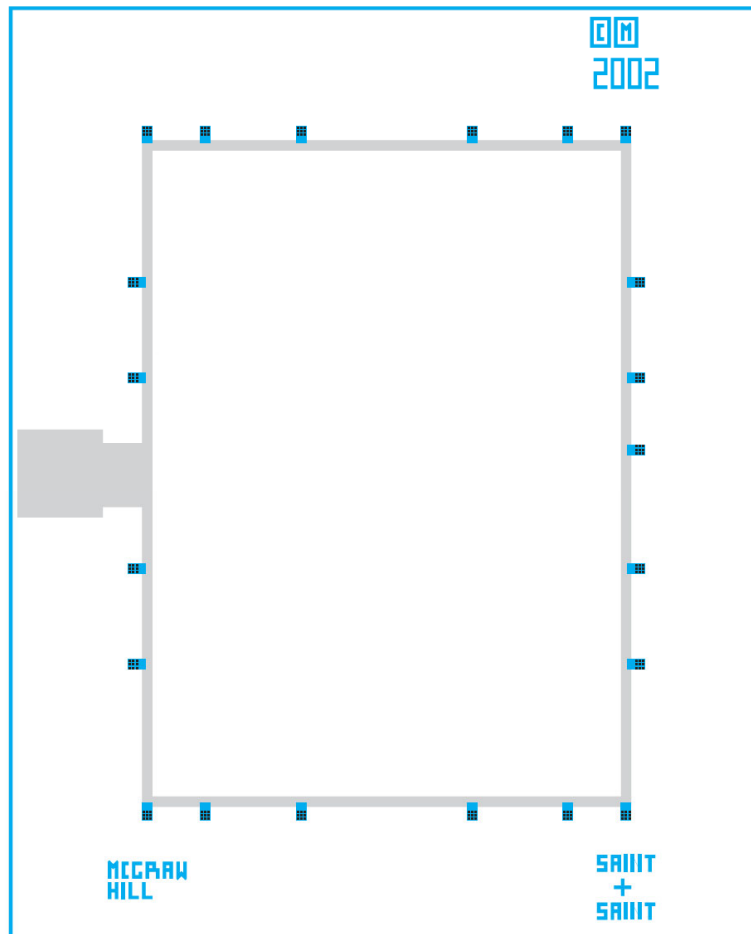


Figure CS1-99

Saint, p. 344 (Fig. CS1-99). As noted in Section XI.B.2, the text associated with this figure describes the figure as depicting “ESD Ground Wiring,” and further describes

that “This simplified plot shows the ground wires associated with the ESD protection system. Notice that this wire creates a continuous ring around the active circuitry.”

283. Therefore, Saint discloses Claim 4 of the '164 patent.

284. Thus, both Haralabidis and Saint (separately) render obvious Claim 4 of the '164 patent.

7. Claim 5: “The integrated circuit structure of claim 1, wherein the common ESD bus is parallel to the plurality of ESD buses.”

285. Claim 5 is a dependent claim, and depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.B.3) that Claim 1 of the '164 patent is rendered obvious by the references cited there and the analysis provided there.

286. Further, the additional requirements of claim 5 are all present in claim 13 – and claim 5 is thus rendered obvious for the same reasons as were described with respect to claim 13. That claim 5 is an apparatus claim and claim 13 is a method claim does not change the earlier (Claim 13) prior art analysis – and similarly, the difference of “a common” in Claim 13 and “the common” in Claim 5 is immaterial.

8. Claim 6

287. The combination of Yoshinaga, Saint, and Haralabidis renders claim 6 obvious. My conclusions and opinions for all the elements (except claim element [6d]) are the same as they were in Ground 1. To analyze claim element [1d] (and claim 13), I apply Haralabidis' common ESD bus to Yoshinaga's segmented

reference rails (*see* claim element [1d] and Claim 13). This identical configuration meets [6d] under the interpretation set forth in Patent Owner’s infringement contentions in Exhibit 1025 – in which Patent Owner reads claim element [6d] to cover a common bus that indirectly connects pad groups.

9. Claim 8

288. Claim 8 is an independent claim, and is a method claim.

289. Further, it was noted at the beginning of the discussion of Claim 12 (in Section XI.A.4) that Claim 12 is basically the method-claim version of the apparatus-claim Claim 6 – distinguished mostly by the addition of the word “forming” to the claim elements already stated in Claim 6; it was further noted that there are no specific or additional teachings involving particular methods used to construct the apparatus described in Claim 6 – and as a result, most of the analysis of Claim 12 involved simply referring to the analysis already provided earlier with respect to Claim 6 – with further discussion there (in Section XI.A.4) of only the differences (between Claim 12 and Claim 6) that appear in the elements of Claim 12.

290. The same can basically said of Claim 8 – that it is basically the method-claim version of the apparatus-claim Claim 1 – distinguished mostly by the addition of the word “forming” to the claim elements already stated in Claim 1; also, in same way that Claim 12 and Claim 6 relate to each other, there are in Claim 8 no specific

or additional teachings involving particular methods used to construct the apparatus described in Claim 1 – and as a result, once again in the same way that Claim 12 and Claim 6 relate to each other, most of the analysis of Claim 8 could involve simply referring to the analysis already provided earlier with respect to Claim 1 – with further discussion of only the differences (between Claim 8 and Claim 1) that appear in the elements of Claim 8.

291. However, as was noted just above (in Section XI.B.3), Claim 1 (an apparatus claim) is very similar to Claim 6 (also an apparatus claim); thus, it can be seen by inspection (and will be confirmed in the analysis below) that Claim 8 (a method claim) is also very similar to Claim 12 (also a method claim). As a result, I have chosen to analyze Claim 8 with respect to Claim 12 (which was discussed in Section XI.A.4); however, an analysis based on analyzing Claim 8 with respect to Claim 1 (which was discussed in Section XI.B.3) would lead to the same results and conclusions.

a. [8-pre]: “A method of integrated circuit structure, comprising:”

292. As an initial matter, I will be offering no opinion regarding whether or not the preamble of claim 8 is limiting; I have been instructed by counsel for the Petitioner to assume that the preamble is limiting – and I have thus conducted my analysis using that assumption.

293. The preamble of Claim 8 is identical to the preamble of Claim 12; thus, for the reasons already discussed with respect to Claim 12, the preamble of Claim 8 is rendered obvious by Yoshinaga.

b. [8a]: “forming a circuit area;”

294. Claim element [8a] is identical to claim element [12a]; thus, for the reasons already discussed (in Section XI.A.4.b), Yoshinaga renders obvious this claim element of Claim 8 of the '164 patent.

c. [8b]: “forming a plurality of ESD buses;”

295. Claim element [8b] is identical to claim element [12b]; thus, for the reasons already discussed (in Section XI.A.4.c), Yoshinaga renders obvious this claim element of Claim 8 of the '164 patent.

d. [8c]: “forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses;”

296. Claim element [8c] is identical to claim element [12c]; thus, for the reasons already discussed (in Section XI.A.4.d), Yoshinaga renders obvious this claim element of Claim 8 of the '164 patent.

e. [8d]: “forming a common ESD bus adjacent to the plurality of pad groups; and”

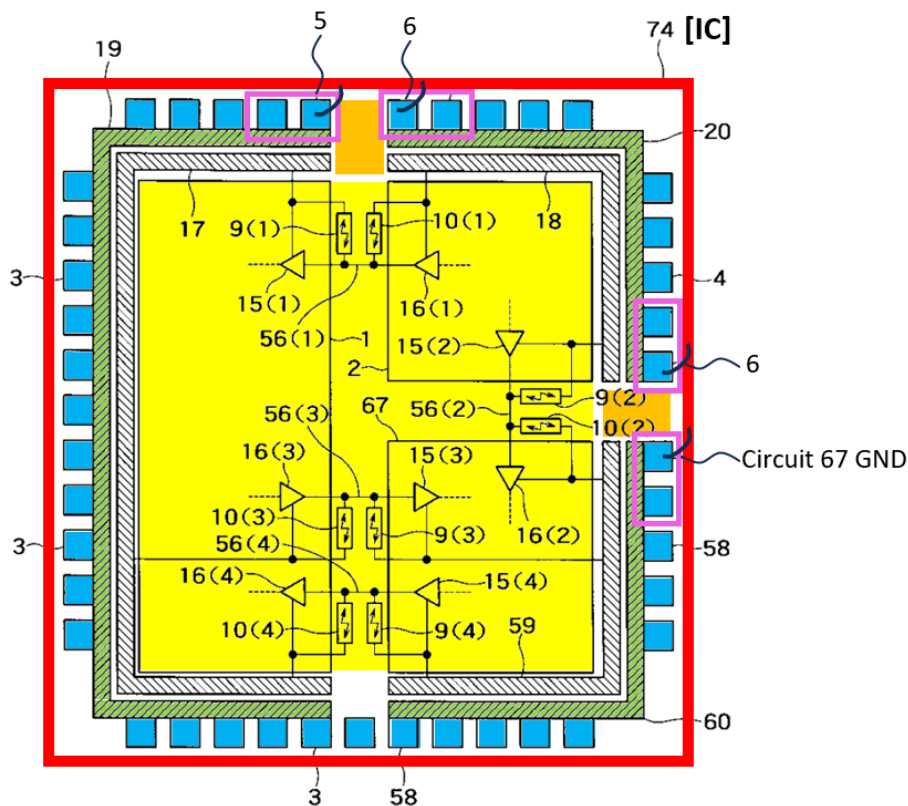
297. As per what was detailed above, claim element [8d] adds in the word “forming” – but is otherwise the same as claim element [1d]; as there are no further teachings involving specific methods used to form the structure disclosed in claim element [1d], for the reasons explained in Section XI.B.3.e claim element [8d] is rendered obvious by Saint in combination with Haralabidis.

f. [8e]: “connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires;”

298. This claim element is very similar to claim element [1e] (“a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus”). However, Claim 1 is an apparatus claim, while Claim 8 is a method claim; thus, the differences that can be seen between claim element [8e] and claim element [1e] are largely due this structural difference – and both describe connecting a plurality of pad groups to the common ESD bus by a plurality of bonding wires, in the same way. Thus, most of claim element [8e] is rendered obvious for the same reasons as those discussed with respect to claim element [1e] (in Section XI.B.3.f).

299. The only wrinkle that causes claim element [8e] to differ from claim element [1e] is the use of language stating that this claim involves “connecting a plurality of pads corresponding to a plurality of pad groups” (continuing with “to the common ESD bus by a plurality of bonding wires”). However, in the analysis

provided with respect to claim element [1e], it was shown that it would have been obvious to a POSITA to combine the Figure 3 embodiment of Haralabidis with the Figure 6 embodiment of Yoshinaga:



Yoshinaga Fig. 6 (annotated).

300. The additional teachings of claim element [8e] were not considered in the discussion of claim element [1e] – as the relevant claim language (discussed just above) of claim element [8e] was simply not present in claim element [1e]. However, inspection of this combined embodiment shows that it also discloses claim element [8e] – as (at the top of the depicted combined embodiment) there are structures that are “connecting a plurality of pads corresponding to the plurality of

pad groups to the common ESD bus by a plurality of bonding wires.” In other words, each pad in Yoshinaga pad groups (illustrated by the pink boxes) “corresponds” to that group – and, of course, where a pad group comprises a single pad, that pad would necessarily be part of the pad group.

301. Therefore, this claim element is rendered obvious by Yoshinaga in combination with Saint and Haralabidis – for the same reasons as those described for claim element [1e] (in Section XI.B.3.f).

g. [8f]: “wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.”

302. Claim element [8f] is identical to claim element [12e]; thus, for the reasons already discussed (in Section XI.A.4.f), Yoshinaga renders obvious this claim element of Claim 8 of the ’164 patent.

h. Claim 8 Summary

303. For all of the reasons described above, Claim 8 of the ’164 patent is rendered obvious by Yoshinaga in combination with Saint, Haralabidis, and the knowledge of a POSITA.

- 10. Claim 9: “The method of integrated circuit structure of claim 8, wherein each of the plurality of pad groups comprises at least one pad, and the plurality of bonding wires is configured to connect the at least one pad to the common ESD bus.”**

304. Claim 9 is a dependent claim, and depends from Claim 8; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.B.9) that Claim 8 of the '164 patent is rendered obvious by the references cited there and the analysis provided there.

305. Aside from the opening indication that it is dependent from Claim 8, Claim 9 is otherwise identical to Claim 2; thus, for the same reasons as those discussed for Claim 2 (in Section XI.B.4), Claim 9 is rendered obvious for the same reasons discussed there.

- 11. Claim 10: “The method of integrated circuit structure of claim 8, further comprising: forming the common ESD bus outside the plurality of chip edges or inside the plurality of chip edges.”**

306. Claim 10 is a dependent claim, and depends from Claim 8; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.B.9) that Claim 8 of the '164 patent is rendered obvious by the references cited there and the analysis provided there.

307. Aside from the opening indication that it is dependent from Claim 8, Claim 10 is otherwise very similar to Claim 4. Claim 10 reads as:

further comprising: forming the common ESD bus outside the plurality of chip edges or inside the plurality of chip edges.

Aside from the opening indication that it is dependent from Claim 1, Claim 4 reads as:

wherein the common ESD bus is formed outside the plurality of chip edges or inside the plurality of chip edges.

The only difference between these two excerpts is due to Claim 10 being a method claim (which thus contains the method-claim language of “forming”), while Claim 4 is an apparatus claim (which thus contains the post-formation apparatus claim language of “wherein ... is formed”). Otherwise, the claim language and what is being claimed are identical.

308. Thus, for the same reasons as those discussed for Claim 4 (in Section XI.B.6), Claim 10 is rendered obvious for the same reasons discussed there.

12. Claim 11: “The method of integrated circuit structure of claim 8, wherein the common ESD bus is parallel to the plurality of ESD buses.”

309. Claim 11 is a dependent claim, and depends from Claim 8; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.B.9) that Claim 8 of the ’164 patent is rendered obvious by the references cited there and the analysis provided there.

310. Aside from the opening indication that it is dependent from Claim 8, Claim 11 is otherwise identical to Claim 5; thus, for the same reasons as those discussed for Claim 5 (in Section XI.B.7), Claim 11 is rendered obvious for the same reasons discussed there.

C. Ground 3—Saint, Haralabidis and the Knowledge of a POSITA

311. It is my conclusion and opinion that Claims 1-14 of the ’164 patent are rendered obvious by Saint – in combination with Haralabidis and the knowledge of a POSITA.

1. Motivation to Combine Saint and Haralabidis

312. Ground 1 involved combining Yoshinaga with Saint – and the motivation to combine those two references was discussed in Section XI.A.1. Ground 2 involved combining Yoshinaga with Saint and Haralabidis – and the motivation to combine those three references was discussed in Section XI.B.1.

313. Ground 3 involves combining Saint with Haralabidis; therefore, the general idea of combining these two references has already been considered with respect to Ground 2. However, as here Saint (rather than Yoshinaga) is the primary reference, the motivation to combine these two references is considered from a slightly-different perspective.

314. It is my conclusion and opinion that a POSITA would have been motivated to combine Saint and Haralabidis – and would have been able to do so with a reasonable expectation of success, and without undue experimentation. Based on my understandings as explained in the prior paragraph, there are at least five reasons that a POSITA would have been motivated to combine Saint and Haralabidis – with some being general, while others relate to more-specific aspects of the disclosures of the material provided in Saint (which is a book) and those of Haralabidis (which is a patent).

a. Saint and Haralabidis Involve Similar Issues and Concepts.

315. Saint and Haralabidis are in the same general field of art – and therefore address similar issues and concepts on multiple levels.

316. As described in Section XI.A.1, Saint is a textbook – and thus covers a great deal of ground. Saint deals broadly with the actual design, development, and manufacturing of integrated circuits; in particular, Saint is focused on the “physical design” phase of integrated circuit design and development (with physical design

(which includes what is commonly known in the art as “layout” of the circuitry) having been explained in Section VII.A). Saint provides a generalized explanation of what the book is about (on pp. 13-17) – and, as part of the discussions of the physical design of ICs, Saint includes copious discussion of ESD protection circuitry and its implementation during physical design – *see, e.g.*, “ESD Supply Strategies” at pp. 160-164, as well as the generalized discussion in pp. 316-350.

317. While Saint covers a great deal of ground, there are some issues which are not covered in Saint – for example, Saint concentrates almost entirely on the IC alone, and rarely ventures outside of the IC bond pads (other than to describe, in Chapter 9 and the “case studies” at the end of the book, how package arrangements are handled in IC design and how bond pads are connected to package traces (and thus to package pins)).

318. Haralabidis (as his title indicates) provides these sorts of additional details – involving the various aspects of ESD protection circuitry (such as the problem of digital switching noise propagating to the analog circuit blocks via the ESD protection network) that extends outside of the IC (including its bond pads) – to involve the package and even the PC board onto which a packaged IC is mounted. Further, Haralabidis provides discussions of conventional prior-art techniques which have already been used – techniques that involve the use of a common ESD bus in the package substrate; these are described by Haralabidis in Figure 3 and Figure 4,

and further in the specification (at 3:9-64). To overcome shortcomings (such as the problem of digital switching noise propagating to analog circuit blocks via the common ESD line in the package substrate) in these conventional art approaches, Haralabidis offers (as inventive material) Figure 5 – in which the common ESD bus is placed out on the PC board (rather than in the package substrate). (See the discussion of Figure 5 at 3:65-5:41.)

319. While the prior paragraph shows that there are differences between Saint and Haralabidis, there are also similarities – similarities that would motivate a POSITA to apply the teachings of Haralabidis to Saint, so that the designs of Saint could be improved by including the teachings of Haralabidis.

320. For example, Saint depicts both segmented ground rails (Figure 7-7 on p. 162), as well as a continuous ESD ground rail that encircles (in the form of a rectangle) the entire circuit area of the IC (i.e., it is located at the periphery of the circuit area, but inward of the bond pads) (Figure CS1-99 on p. 344). A POSITA would have been motivated, for example, to use the common ESD bus concepts of Haralabidis – and to locate the continuous rectangular common ESD bus in the package substrate, or even on the PC board (for the reasons described by Haralabidis with regard to his Figure 5), because Saint provides few (if any) teachings about printed circuit boards.

b. Saint and Haralabidis Provide Methods of Reducing IC Size (and Thus IC Cost).

321. Saint and Haralabidis both provide related teachings that provide techniques for reducing IC size. Since the cost to manufacture a silicon IC is a direct function of the areal size of the IC (since the cost of a wafer is a fixed cost – and so a smaller IC means a lower cost per IC), a POSITA would be motivated to use various techniques to reduce IC size; thus, a POSITA would be motivated to use techniques from different references – and to, where possible, use them in tandem.

322. As noted elsewhere already, Saint describes how (in a core-limited design) there may be “wasted space” (i.e., space that is not part of the circuit area) between the bond pads – and directly suggests that by expanding the circuit area to include this “wasted space,” the more-efficient use of available silicon real estate allows for the IC to be made smaller; *see* Saint at pp. 211-213 for an explanation of “core-limited” IC designs and “pad-limited” IC designs; *see also id.* at p. 221 (particularly Figure 9-28) for a description of how one may use the “wasted space” between the bond pads to expand the size of the circuit area – and thus reduce the size of the IC.

323. Haralabidis describes techniques for a common ESD bus that are outside of the IC (rather than inside the IC, as depicted in Saint Figure CS1-99 on p. 344); specifically, Haralabidis describes prior art in Figure 3 (in which the common ESD bus is placed in the package substrate), and inventive material in Figure 5 (in

which the common ESD bus is placed on the PC board). As a POSITA would recognize, these techniques can also reduce the size of an IC – by placing the common ESD bus (such as shown in Saint Figure CS1-99) outside of the IC.

324. Note in particular that Haralabidis’ descriptions and teachings (as just described) are unrelated to Saint’s description of converting the “wasted space” between the bond pads into circuit area space. Thus, Saint and Haralabidis provide different (but complementary) techniques for reducing IC size – and a POSITA would be motivated to combine Saint and Haralabidis, so as to take advantage of these independent (but co-usable) techniques for reducing IC size.

c. Haralabidis is Analogous Art to Saint and the ’164 patent.

325. Further, a POSITA would have been motivated to combine Saint with Haralabidis, because they because involve analogous art – to each other, and to the teachings of the ’164 patent.

326. As a primary example, both Saint and Haralabidis involve extensive expositions on architectures and circuitry for ESD protection in integrated circuits. This topic (and further discussion of the analogous-art aspects of Saint and Haralabidis) were already described in Section XI.B.1 – and so those discussions can simply be incorporated here.

d. Haralabidis Provides Circuit Architectures That Can Be Used to Improve the ESD Protection Capabilities of the Circuitry of Saint.

327. As detailed already, Haralabidis provides teachings that improve both the robustness of ESD protection *and* the ability to prevent digital switching noise from propagating to the analog circuit blocks via the ESD protection network – with his overall gameplan being introduced at 1:33-35; note also that the block diagrams of Haralabidis (in Figure 1 and Figure 3, 4, and 5) depict the presence (in the IC) of both digital circuit blocks and analog (specifically, RF) circuit blocks.

328. As was also detailed already, Haralabidis cites a conventional architecture which places the ESD common bus in the package substrate (Figure 3 and Figure 4); Haralabidis provides details of the package-substrate common-bus architecture at 1:50-2:4 – and notes that the segmented rails (inside the IC) represent an architectural improvement over the continuous rail (inside the IC) that is used in the Figure 1 prior art embodiment. Further, Haralabidis teaches an architecture which actually meets the goals of his gameplan – in the Figure 5 embodiment (which is described in the specification at 3:65-5:41).

329. Saint also addresses these issues to a considerable degree. In Figure 7-7 (on p. 162), Saint shows an IC design that has (in pairs) three power supply rails and three ground rails – which are used (obviously) to provide separate power and ground lines to different circuit blocks. Further, Saint has an entire chapter (Chapter

6) that discusses “Noise Issues” – including the problems that can occur if digital switching noise is able to propagate (through a common power supply line or common ground line) to an analog circuit block (*see Saint*, p. 138).

330. Therefore, a POSITA would have been motivated to combine the circuit architecture improvements of Haralabidis (which use ESD circuitry outside of the IC) with the circuitry of Saint – to improve the ESD protection capabilities of an IC, while mitigating the problem of digital switching noise propagating through the ESD protection network to the analog circuit blocks.

e. A POSITA Would Have Had a Reasonable Expectation of Success in Making These Combinations.

331. Finally, a POSITA would have had a reasonable expectation of success in combining these two references – and would have been able to do so without undue experimentation.

332. As noted several times, Saint is a book; there is therefore a great deal of information in Saint, on a variety of topics. Saint is particularly notable for being a practical text, written by a practitioner in the field (as opposed to, e.g., an academic) who has extensive product-level work experience with the material that he is discussing. Saint covers very practical, product-IC topics in detail – such as floorplanning (Chapter 7) and packaging (Chapter 9). Thus, a POSITA would have had a reasonable expectation of success when using the material of Saint (since the material described in Saint has already been used extensively to design real IC

products) – and to be able to do so without undue experimentation (for the same reason just described in parentheses).

333. Haralabidis, on the other hand, is a patent – and therefore focuses on the inventive material to be presented, and background to that inventive material. Haralabidis provides details necessary for that purpose – but examination of Haralabidis clearly indicates that the basic teachings of Saint (that would be known to a POSITA) are implicitly included in Haralabidis; e.g., Haralabidis shows a circuit area with circuit blocks in the figures, and Haralabidis describes ESD protection architectures without discussing the well-known use of two diodes (as described in Section VII.C) that shunt the energy of an ESD event to a rail (as it is assumed that a POSITA would already be familiar with this circuit architecture). Finally, note that much of the architectural teachings of Haralabidis involve the use of simple ohmic connections (such as simple wire bond connections, package traces, and printed circuit board traces). Thus, a POSITA would have a reasonable expectation of success when using the teachings of Haralabidis (since they are straightforward and easy to understand) – and to be able to do so without undue experimentation (for the same reason just described in parentheses).

334. Due to these commonalities – and the clarity of the material of Saint and the teachings of Haralabidis – a POSITA would have had a reasonable expectation of success when combining Saint and Haralabidis; further, it would be

expected that this could be achieved without undue experimentation. The reasons for this final assertion are based on the characterizations provided separately for Saint and for Haralabidis in the preceding two paragraphs; as these characterizations are true for both references, they also apply to combining the two references together. Both references are easy to understand, and either can readily be used to provide material (for combination) that is missing from the other (as shown above).

2. Claim 1

335. Claim 1 is an independent claim, and is an apparatus claim.

a. [1-pre]: “An integrated circuit structure, comprising:”

336. As an initial matter, I will be offering no opinion regarding whether or not the preamble of Claim 1 is limiting; I have been instructed by counsel for the Petitioner to assume that the preamble is limiting – and I have thus conducted my analysis using that assumption.

337. Saint discloses the preamble of Claim 1 – as can easily be seen via simple examination of Saint. First, the title of the Saint book is “IC Mask Design” – where, as mentioned earlier, “IC” is the acronym for “integrated circuit.” Second, the sub-title of the Saint book is “Essential Layout Techniques;” as was explained in Section VII.A, “layout” refers to the physical-design phase of integrated circuit development and design – a process whose goal is the eventual fabrication of integrated circuit structures. Finally, as the Introduction of Saint states (at p. 13),

“A good mask designer is crucial to the development of superior integrated circuits.”

As this book runs to some 460 pages, a very lengthy list of further examples could be provided – but these alone are more than sufficient.

338. Saint discloses exemplary ICs in Figures 7-7 and 9-21, which are referred to further in my analysis. Saint, pp. 162, 213. While both of these Figures abstract various details, a POSITA would understand that each Figure represents an IC.

339. Therefore, Saint renders obvious the preamble of Claim 1 of the '164 patent.

b. [1a]: “a circuit area;”

340. Saint discloses this claim element of Claim 1 of the '164 patent. As with the preamble, a very large number of examples can be cited from Saint to demonstrate this disclosure; however, for brevity, two will be provided here to prove the point.

341. First, Saint has an entire chapter (Chapter 7) on floorplanning of an integrated circuit. A good example of a circuit area in an integrated circuit can be found in Figure 7-9:

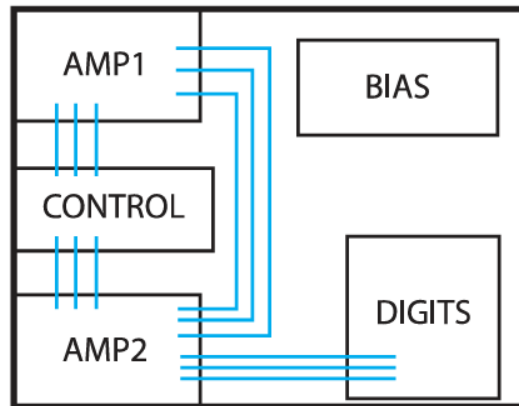


Figure 7-9. Better layout avoids cross wiring, keeps wires shorter.

This figure shows circuit blocks in a circuit area.

342. As a second example, Saint depicts an IC floorplan that includes circuit blocks in a circuit area and bond pads around the periphery of the IC – in Figure 9-21 (at p. 213).

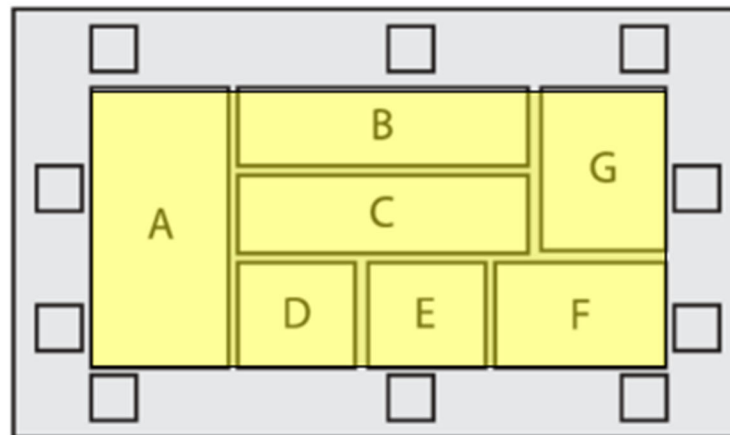


Figure 9-21. The minimum size of the chip limited by the anticipated sizes of the blocks.

The circuit blocks (A-F) illustrate a circuit area – as the area where the circuitry is placed/found. While the “circuit area” in many ICs may be rectangular or square,

the “circuit area” may in fact have other shapes - such as shown below by Saint

Figure 9-28:

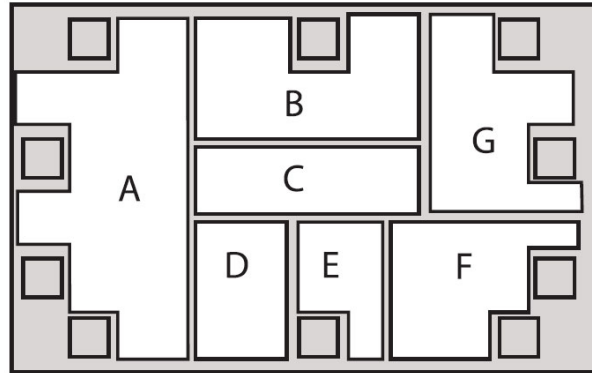


Figure 9–28. *We can use extra space surrounding our pads to shrink our chip size.*

Another example of the claimed “circuit area” (highlighted in yellow) is shown below in Saint Fig. 7-7.

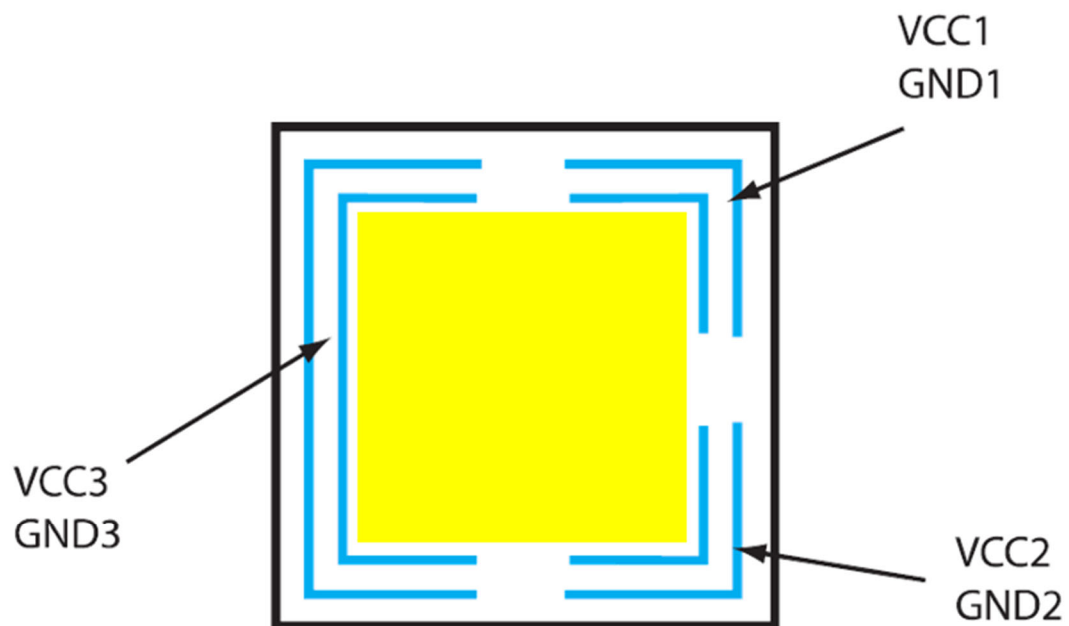


Figure 7–7. *Pin-out simplification showing like protects grouped together.*

343. Therefore, Saint renders satisfies this claim element of Claim 1 of the '164 patent.

c. [1b]: “a plurality of ESD buses;”

344. Saint discloses this claim element of Claim 1 of the '164 patent.

345. As was explained in Section VII.C, it has long been conventional practice to use supply rails (such as power supply rails and ground rails) as ESD rails/buses – via which the energy of an ESD event is safely evacuated from an integrated circuit (so that this shunting of the energy in this way prevents it from going into/through circuit structures and causing damage). The '164 patent describes this technique for ESD mitigation in the specification:

In general, it is commonly [sic] to place filler cells F1 and F2 at empty spaces between the I/O pads 12, and connect the filler cells F1 and F2 to an electrostatic discharge (ESD) bus 11 (e.g., a layout trace connected to a ground or a system voltage), which makes each portion of the circuit area 10 and the filler cells F1 and F2 are connected [sic] to the continuous ESD bus to provide ESD protection to the integrated circuit ESD bus structure 1.

'164 patent at 1:30-37; (instances of somewhat unusual English usage in the original).

346. While this basic technique is described above in the Background section of the '164 patent, that this is the technique that is used in the teachings of the '164 patent is demonstrated elsewhere in the specification; e.g.,

Each of the plurality of pad groups G1 , G2 and G3 includes a plurality of pads 32 , wherein the pad 32 is an input / output pad connected to a ground or a system low voltage.

'164 patent at 3:61-64. Saint discloses the same basic techniques, used in the same ways.

347. For example, in the aforementioned chapter (of Saint) on floorplanning, Saint shows (at Figure 7-7 on p. 162) an outline of such an IC floorplan, which includes power supply rails²⁴ and ground rails:

²⁴ Saint here uses the label “VCC” to represent the power supply lines; as is well-known in the art (and would have been known to a POSITA), this is the commonly-used labeling in integrated circuits that use bipolar transistors – as the power supply line is generally connected to the collector pin of a bipolar transistor. In contrast (but using the same nomenclature logic), integrated circuits that use MOS transistors (such as the commonly-used CMOS architecture) commonly use the label “VDD” to represent power supply lines – since, for MOS transistors, the power supply lines are generally connected to the drain pin of a MOS transistor.

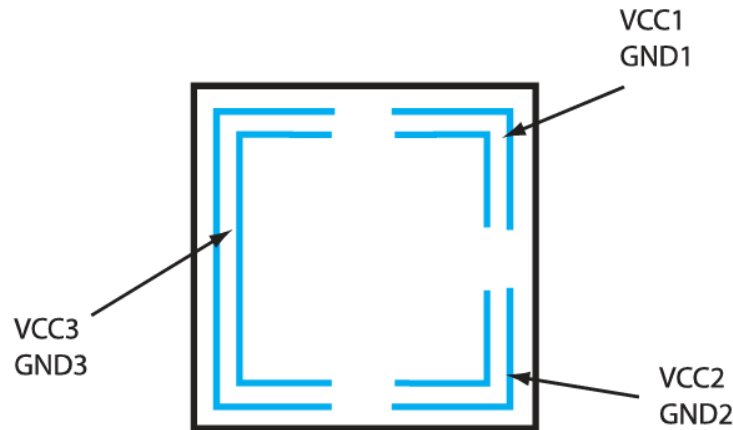


Figure 7-7. Pin-out simplification showing like protects grouped together.

That Saint depicts the usage of the power supply and ground rails for the shunting of the energy of an ESD event is confirmed via Figure 7-3 (on p. 160):

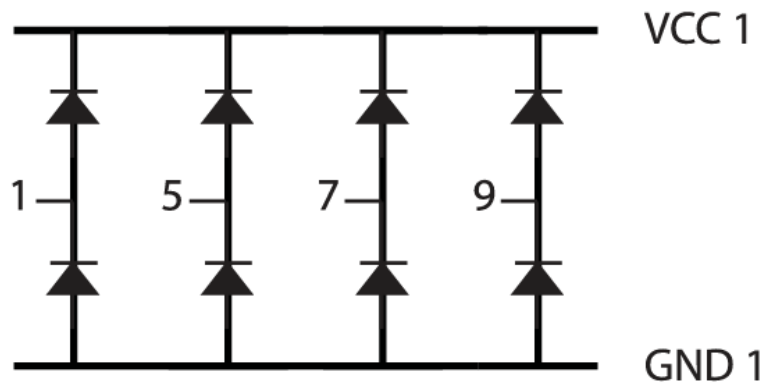


Figure 7-3. Pins 1, 5, 7, and 9 protected to VCC1 and GND1.

As described in Section VII.C, this type of dual-diode structure is the commonly-used circuit inclusion that serves to provide ESD protection (as described in detail in Section VII.C). See also Figure 7-4 and Figure 7-5 on p. 161 – which show the other pins of the IC being similarly-connected to other power supply and ground rails for the same purpose.

348. Therefore, Saint renders obvious this claim element of Claim 1 of the '164 patent.

d. [1c]: “a plurality of pad groups, adjacent and connected to the plurality of ESD buses;”

349. Saint discloses this claim element of Claim 1 of the '164 patent.

350. As discussed just above with respect to claim element [1b], Saint discloses a plurality of ESD buses – as described in detail there. Saint discloses the remainder of this claim element. Saint Figure 7-6 (on p. 161) shows ground/power supply pins (numbered 1 to 16) as being “[s]cattered” – which simply means that the pin assignments have been selected without consideration of where the power supply rails and ground rails are actually located in the IC. Saint, p. 161.

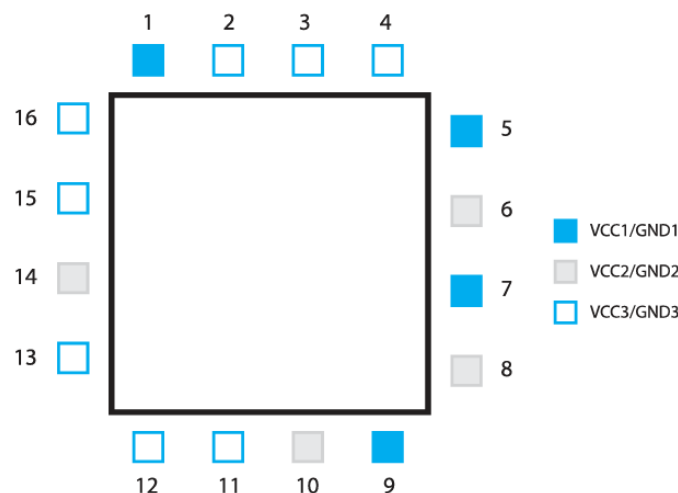


Figure 7-6. Scattered pins on the same protect circuit.

351. A POSITA would have understood that each pin labeled 1-16 corresponds to an IC pad - and that the various GND/VCC pads are (as Saint says)

“scattered”; as noted above, by “scattered,” Saint means that the package pins have been assigned locations without consideration for the locations of the power supply rails and the ground rails (to which the assigned pins are supposed to connect). Saint teaches a remedy for this “scattered” situation – as “[a] nicer way to prepare for this chip’s layout is to ... take the four signals that were on pins 1, 5, 7, and 9 and move them close to each other,” resulting in the VCC/GND groups shown in Fig. 7-7 below. Saint, pp. 161-162. A POSITA would have understood the groupings as follows: VCC1/GND1 include pads for pins 1, 5, 7, and 9; VCC2/GND2 includes pads for pins 6, 8, 10, and 14; and VCC3/GND3 includes pads for pins 2-4, 11-13, and 15-16. A POSITA would have understood (or at least found it obvious) that the “plurality of pad groups” (*e.g.*, pads for connecting the groups of GND1, GND2, and GND3 pins) are “adjacent and connected to the plurality of ESD buses” (GND1, GND2, and GND3 buses in Fig. 7-7).

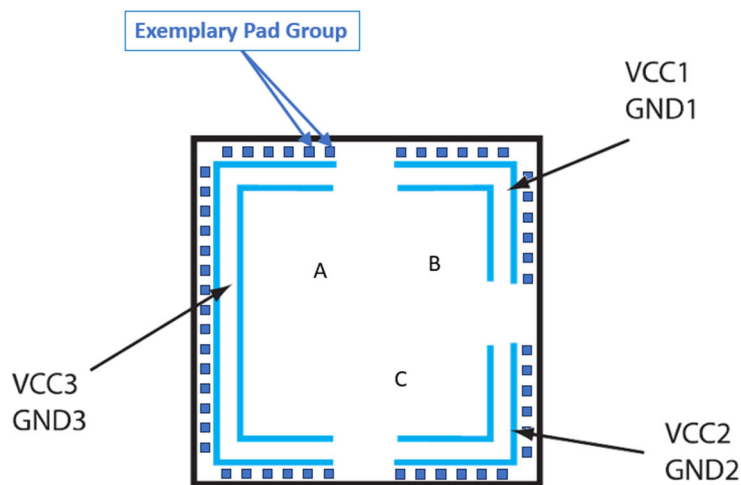


Figure 7-7. Pin-out simplification showing like protects grouped together.

Saint, Fig. 7-7 (p. 162). This is similar to Saint Figure 7-1 – which shows an arrangement where “[l]ike items [are] set side by side.” *Id.*, p. 159. Even if the term “adjacent” (more narrowly) meant “immediately beside,” a POSITA would have found such an arrangement obvious – as well as advantageous for the purpose of reducing the wire resistance (as well as to reduce the amount of wiring needed to connect each bus with its respective pads).

352. Furthermore, Figures 7-3 to 7-5 in Saint illustrate the pad groups as each being connected to respective GND and VCC lines. Saint, pp. 160-161. Looking at pins 1, 5, 7, and 9 (and by extension their corresponding pads) as an example, these pins are connected to VCC1 and GND1 through diodes, as shown in Figure 7-3.

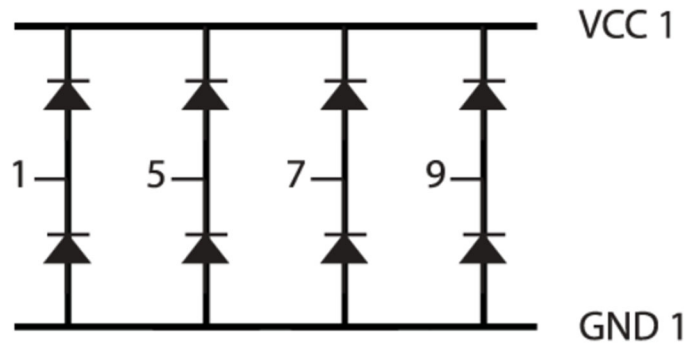


Figure 7-3. Pins 1, 5, 7, and 9 protected to VCC1 and GND1.

353. Therefore, Saint discloses this claim element of Claim 1 of the '164 patent.

e. [1d]: “a common ESD bus, adjacent to the plurality of pad groups; and”

354. Saint or Saint in combination with Haralabidis discloses this claim element of Claim 1 of the '164 patent.

355. As an initial matter, claim element [1d] makes use of parts of claim element [1c] – and therefore, reference back to the discussion of claim element [1c] will be made here as necessary.

356. As part of a “case study” (CS1) in Saint’s book, Saint provides a section (of the case study) entitled “ESD Ground Wiring” (at p. 344) – which consists of a figure and some explanatory text.

357. The figure describes the ESD ground wiring visually:

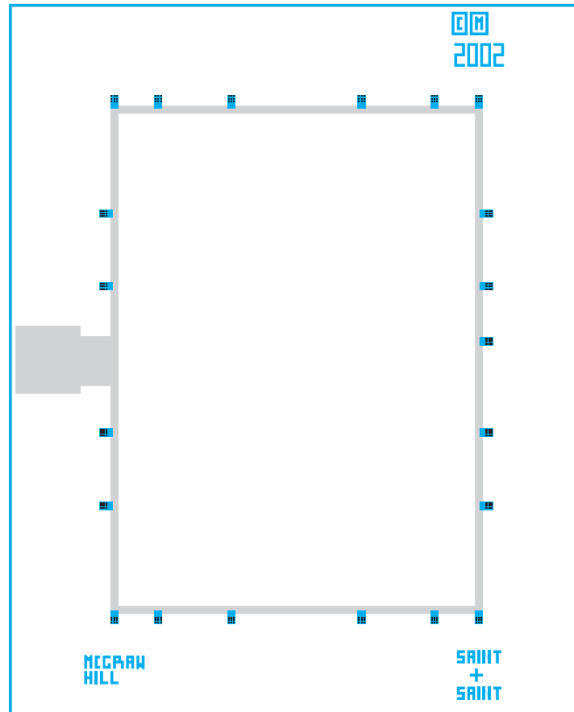


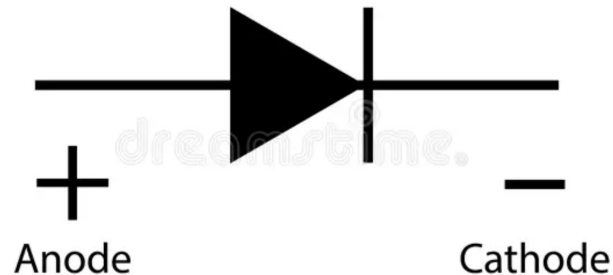
Figure CS1-99

As the associated text explains,

This simplified plot shows the ground wires associated with the ESD protection system. Notice that this wire creates a continuous ring around the active circuitry and that the ESD diode inner terminals (*anodes*) are connected. (Emphasis added.)

The term “anodes” (which is, of course, the plural of “anode”) is highlighted because its use here deserves an explanation. A POSITA (or even someone below the level of a POSITA, such as an electrical-engineering undergraduate) would be familiar with the use of the term “anode” (and its word-partner, “cathode”) to separately describe a particular terminal of the two terminals of a diode; for example,

Diode



This diagram identifies the names used for the two terminals of a simple diode; further, a POSITA (or, again, even someone below the level of a POSITA, such as an electrical-engineering undergraduate) would understand that these names are used to describe a diode *structurally* – that is, they provide a description of a diode as a circuit element, and the name will not be altered by operational considerations (such as which in which direction a voltage difference is applied, or in which direction a current flows, etc.)

358. As described in the discussion above involving claim element [1c], Saint (in Figure 7-3, Figure 7-4, and Figure 7-5) depicts the use of a ground rail that provides an ESD bus – along with a visual description of how the diodes of the ESD protection circuitry are connected to that ESD bus:

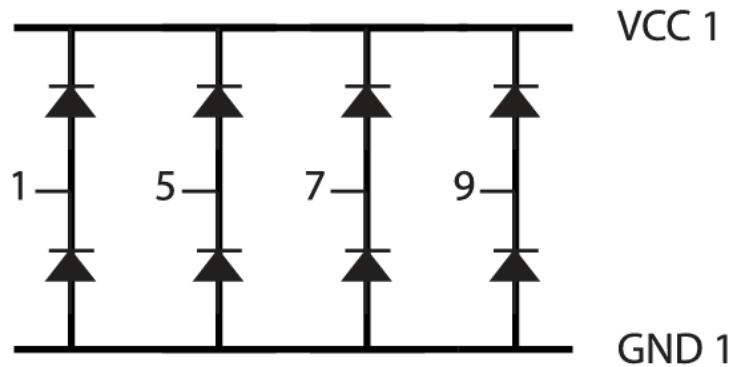


Figure 7-3. Pins 1, 5, 7, and 9 protected to VCC1 and GND1.

(Figure 7-3 is sufficient for the discussion to follow – but Figure 7-4 and Figure 7-5 depict essentially the same thing.) As per the quote from Saint p. 344, “the ESD diode inner terminals (anodes) are connected” to the ESD bus (here, GND 1).

359. As explained above (in the discussion associated with claim element [1c]), in the Chapter 7 discussion Saint has depicted a design where there are three separate power supply and three separate ground lines – with each ground buss (i.e., GND 1, GND 2, and GND 3) providing a ground bus which is connected to the “diode inner terminals (anodes)” of the ESD protection circuitry of the pins associated with the particular tandem (e.g., VCC 1 and GND 1) of power supply rail and ground rail.

360. However, in the different design of the case study depicted (in part) on p. 344, Saint is *not* using the three-ground-rails (which provide three ESD buses) configuration of the Chapter 7 design – rather, Saint is using a *single* ground rail which provides a single ESD bus; this single ground rail – by providing a single ESD

bus to which *all* of the anode-sides-connected-to-ground of the ESD protection circuit diodes are connected – provides the recited “common ESD bus” of claim element [1d].

361. Finally, that this “common ESD bus” is “adjacent to plurality of pad groups” was already demonstrated just above – in the discussion associated with claim element [1c].

362. There – as just mentioned – a design described by Saint involves three separate ground rails, which provide three corresponding ESD buses; as per Figure 7-7:

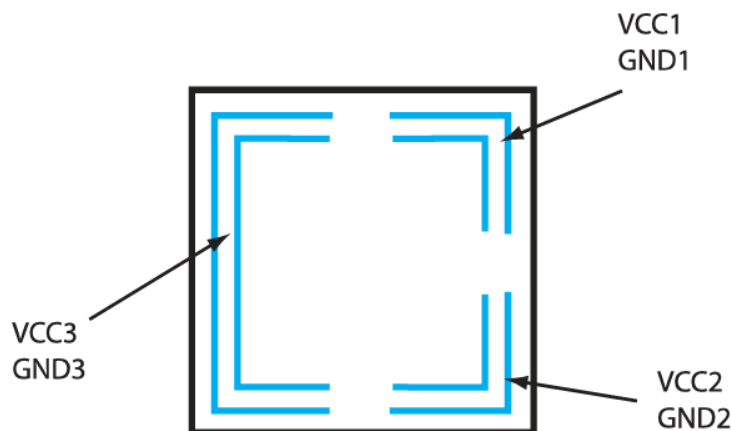


Figure 7-7. Pin-out simplification showing like protects grouped together.

As noted in that discussion (of claim element [1c]), GND1, GND2, and GND3 provide separate ESD buses for the IC being designed (in Chapter 7). Further, it was noted that Saint also provides a depiction (as part of that same IC design) of the bond pads to which the separate ESD buses will be connected (as per Figure 7-6):

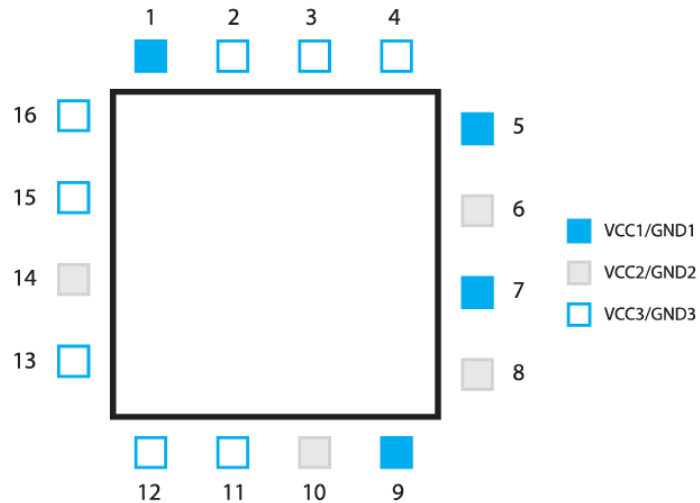


Figure 7-6. Scattered pins on the same protect circuit.

As explained there, Saint thus describes (for that particular IC design) that the ESD buses are adjacent to the plurality of pad groups.

363. However, in the case study chapter (and as described above), the IC design uses a single ground bus rather than three ground buses – and Saint describes this single ground bus as providing “ESD ground wiring.” It would have been obvious to combine Saint’s design of Chapter 7 with Saint’s case study 1, which satisfies this claim element. As further confirmation, Saint provides a pin-out diagram for the IC design of case study 1 (on p. 261):

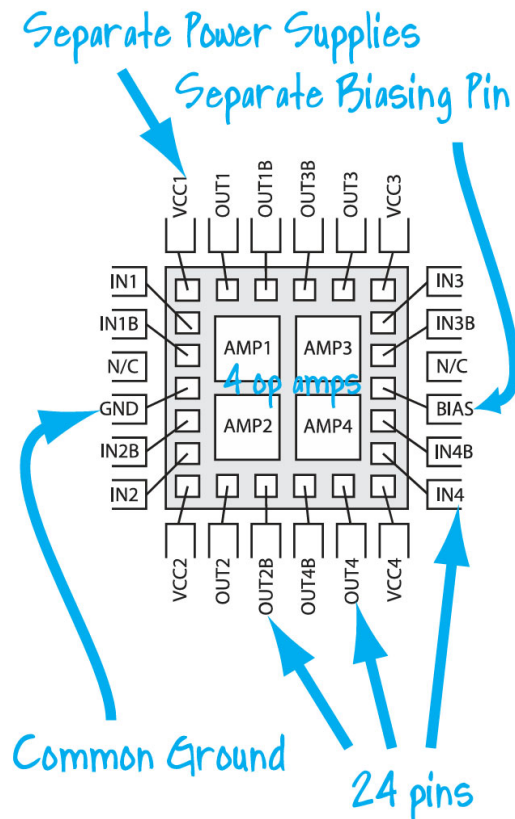


Figure CS1-1. Bond-out design using a 24-pin package.

As can be seen, there is a single (common) ground pin – but multiple (in fact, four) separate power supply pins; in fact, in a quick depiction of the layout of the power supply rails (on p. 346), Saint depicts the four power supply rails in that layout.

364. Therefore, Saint renders obvious claim element [1d] of Claim 1 of the '164 patent.

365. As also mentioned at the outset of this discussion of claim element [1d], this claim element is also rendered obvious by Saint in combination with Haralabidis.

366. As detailed in the overview of Haralabidis (in Section X.C), Haralabidis describes the use of a common ground rail, which also serves to provide the rail to

which the energy of an ESD event is shunted – to provide ESD protection for the IC circuitry.

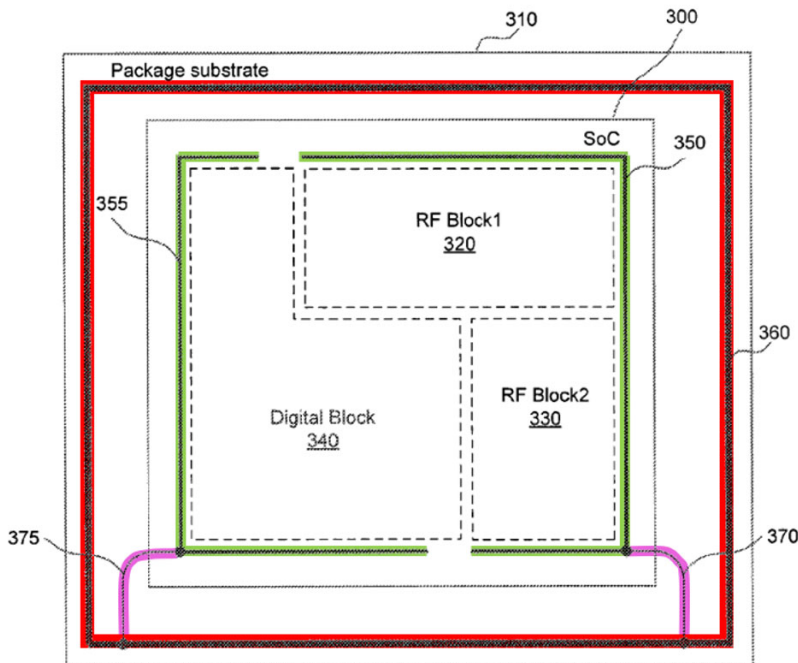


FIG. 3
Conventional Art

(Figure 3 of Haralabidis; annotations added). As described in Haralabidis (and as detailed in Section X.C), the green-annotated rails (350 and 355) are the “segmented” ground rails (of the IC interior), while the red annotated rail (360) is the common ground rail that is part of the package substrate; as can also be seen by inspection (and as was described in Section X.C), the segmented ground rails (350 and 356) are connected to the common ground rail (360) via (respectively) the magenta-annotated wiring lines 370 and 375.

367. As noted above (and in Section X.C), Haralabidis describes the common ground line (360) as being the line to which the energy of ESD events (that

are first shunted to the segmented ground lines (350 and 355)) is finally shunted; thus, Haralabidis describes (and thus renders obvious) a common ESD bus.

368. With this being known in the art and taught by Haralabidis, it is a fairly simple exercise (and would have been a simple exercise for a POSITA) to add the common ESD bus described by Haralabidis to the Figure 7-7 presentation of Saint – and (since they have to connect somewhere) to connect the segmented rails of Saint’s Figure 7-7 presentation to this common ESD bus:

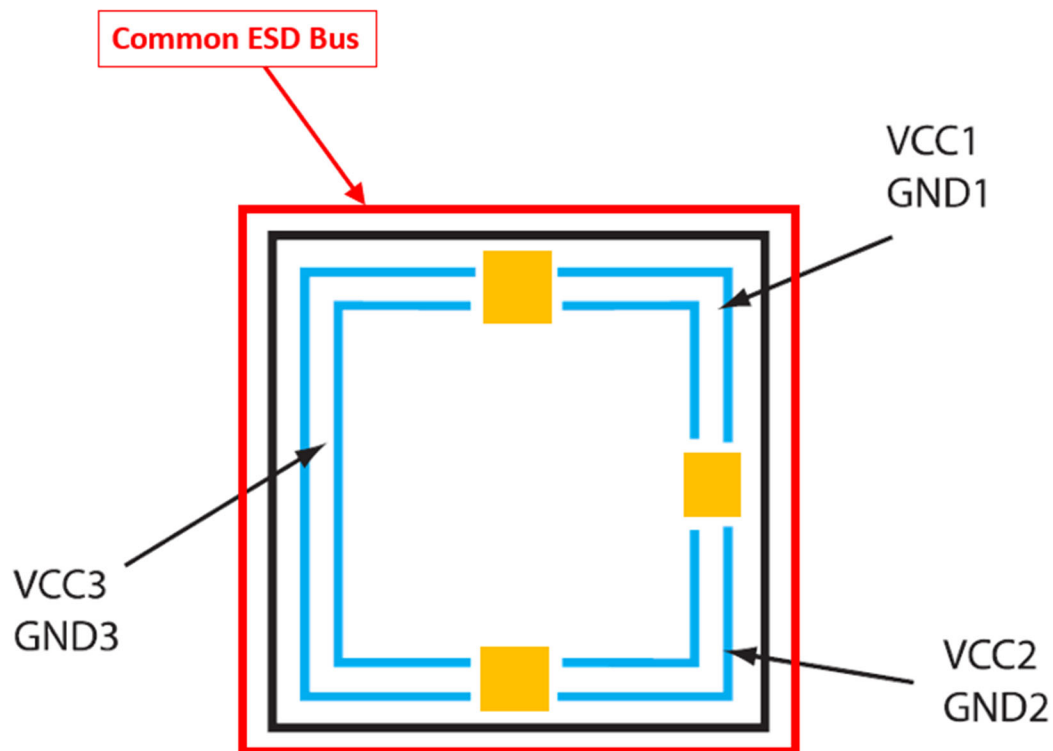


Figure 7–7. Pin-out simplification showing like protects grouped together.

Using a common rail allows circuits to source the reference voltage from the same line (as discussed above for Saint Figure CS1-1), so that the printed circuit board (or

other external circuitry) only needs to feed the common line – which then shares the reference voltage with all of the internal IC circuits. Therefore, Saint in combination with Haralabidis also renders obvious this claim element of Claim 1 of the '164 patent.

f. [1e]: “a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus;”

369. In the discussions involving Ground 1 (specifically, in Section XI.A.2.e) and Ground 2 (specifically, at Section XI.B.3.f), it was noted that whatever provision is made for connecting together ESD shunting-destination lines (such as ground lines), these lines must be connected to a path that provides a sink for the energy of an ESD event – such as a to a package pin that serves as a “pickup pin” for all of the ESD shunt-destination lines. Thus, in-and-of itself, it would be obvious to a POSITA that such a provision would have to be made – for the evacuation of the energy an ESD event from the IC itself via some connection to a package pin (or similar – such as multiple package pins).

370. This functionality is described by Haralabidis in Figure 3 – as was actually already described in association with the discussion above of claim element [1d]:

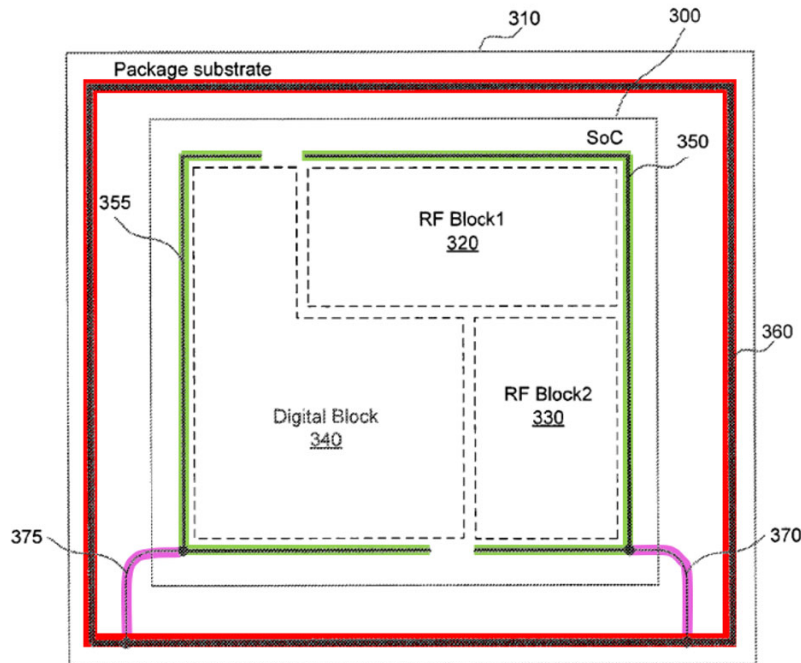


FIG. 3
Conventional Art

As Haralabidis describes the segmented ground lines (350 and 355) as being inside the IC, while the common ground line (360) is part of the package substrate, it would be obvious to a POSITA that the most-commonly-used (and perhaps only) way to connect the segmented ground lines (350 and 355) to the common ground line of the package substrate would be via bond pads and bond wires – which is the standard technique used to connect the IC circuitry to the package pins.

371. That this is the standard technique that is used to connect IC circuitry to package pins is described by Saint; e.g.,

To get the signals from the chip circuitry to the package pins, thin wires join the bond pads on the chip to the inside²⁵ portion of the metal pins.

Saint, p. 202. Further, Haralabidis describes the use of such connections:

The plurality of circuit blocks have [sic] corresponding ground nodes electrically coupled to corresponding segments of the IC ground rail. Further, the segments of the IC ground rail are coupled to corresponding segments of the package ground rail by corresponding first electrical connections that could be, for example: *wirebonds*, solder bumps, solder balls, and the like.

Haralabidis at 1:59-65; emphasis added. Thus, Haralabidis also describes the use of this specific technique for the purposes described above – with “solder bumps, solder balls, and the like” describing more-involved²⁶ techniques of connecting IC circuitry to package pins (techniques which have been developed to address the need for more pins for connections to complex ICs).

²⁵ As the surrounding discussion in Saint makes clear, “inside” here refers to “inside the package.”

²⁶ Note that the ’164 patent discusses only the use of bond wiring, and none of these more-involved methods.

372. It would thus be obvious to a POSITA to connect the pads/pad-groups of the Figure 7-6 / Figure 7-7 design of Saint to the common ESD bus (of Haralabidis, which was shown to be an obvious combination with Saint in the discussion above of claim element [1d]) using bond wires as described by both Haralabidis and Saint. Further, it was very well-known in the art (and thus to a POSITA) that one common way to create a bond wire connection was to connect bond wires to bond pads as is shown in Miller Figs. 1, 4, 7, 10, 13, and 14, Beauchamp Figs. 1-8, and Saint, pp. 202-211 (showing and discussing bond wire connection to bond pads, including “Ultrasonic Wedge Bonding” and “Ultrasonic Ball Bonding” techniques). Thus, the knowledge of a POSITA also renders obvious connecting a bond wire to a bond pad, especially where existing bond pads are already available.

373. Thus, this claim element of Claim 1 of the '164 patent is rendered obvious by Saint in combination with Haralabidis and the knowledge of a POSITA.

g. [1f]: “wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.”

374. Saint – and Saint in combination with the knowledge of a POSITA – discloses this claim element of Claim 6 of the '164 patent.

375. To simplify the analysis, this claim element will be split into claim sub-elements.

i. [1f-1]: “wherein the circuit area comprises at least one saved area”

376. Saint discloses this claim sub-element of claim element [1f] of the ’164 patent.

377. At page 220, Saint describes the existence of “wasted space around the edges between the pads” – which (as will be confirmed by a figure from Saint, below) is the same thing as the “saved space” of the ’164 patent. Further, Saint (also at p. 220) discloses that “... you can push some of your circuitry into this wasted space to try to use those gaps.” Saint shows this usage explicitly, in Figure 9-28^{27,28}:

²⁷ Here, Saint shows space between individual pads; however, since (as described in Section XI.A.2.d) the ’164 patent states that a “pad group” can have just one pad, Saint’s depiction matches the ’164 patent’s description of saved space between pad groups. It would also be obvious to a POSITA that Saint’s teachings (as described here) would apply in the same way if any “pad group” had more than one pad in it.

²⁸ Note that this exemplary depiction represents an IC that is core-limited (rather than pad-limited).

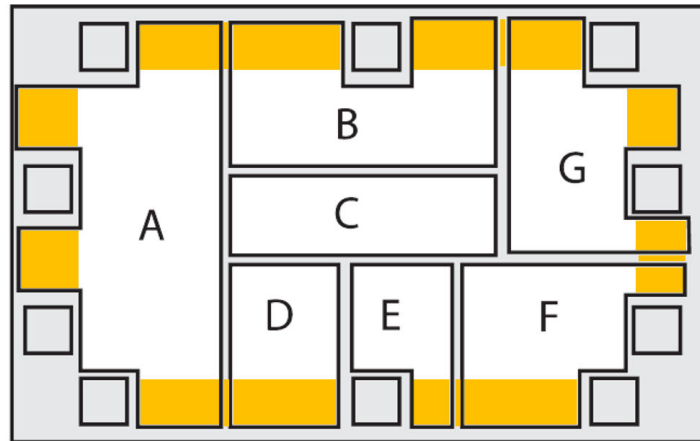


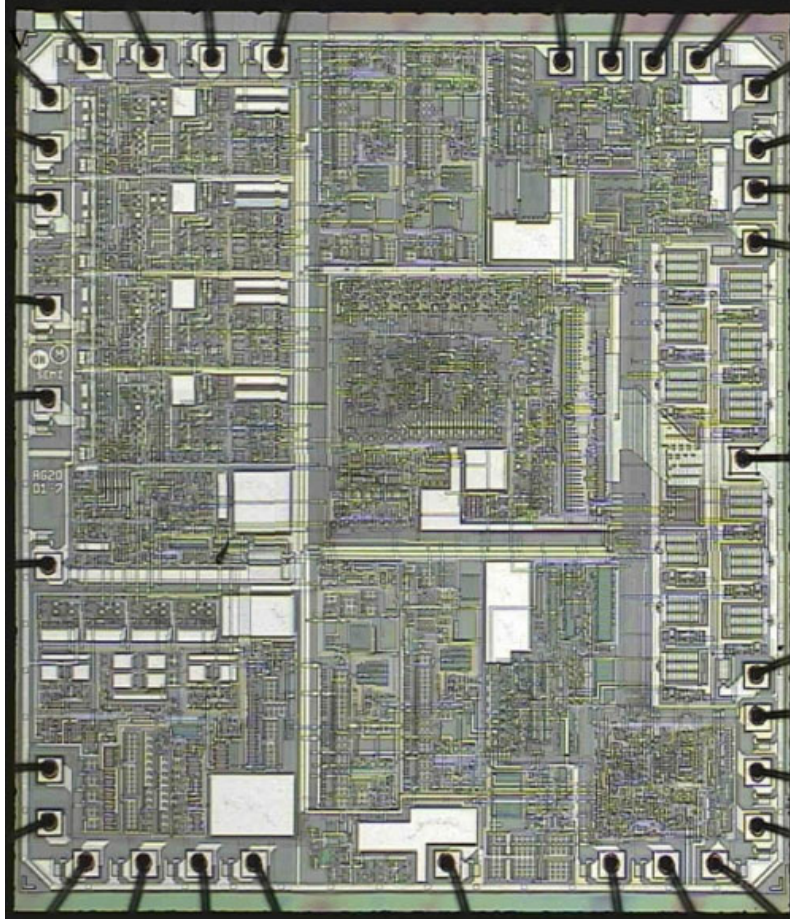
Figure 9–28. We can use extra space surrounding our pads to shrink our chip size.

(Annotations added to show the “saved space” identified by Saint.) As Saint explains (on p. 221), “you can re-lay parts of your circuit elements in and around these pads trying to get the chip as small as possible.”

378. This use of the “saved space” for circuitry is the same as what is described in the *specification* (but not the claims) of the ’164 patent. Therefore, this claim sub-element of claim element [1f] of Claim 1 of the ’164 patent is rendered obvious by Saint.

379. For completeness, it should be noted that the use of the space between pad groups for circuitry was also broadly-known in the art. For example, the 2010

article²⁹ mentioned earlier contains a figure (that was also shown earlier) that is a microphotograph of an IC³⁰ that has been “torn down” so as to show its innards:



As can be seen by simple inspection, there is circuitry deployed in the spaces between the pad groups.

²⁹ <https://www.sparkfun.com/news/384>.

³⁰ Note that this actual product IC is (as is the IC in Saint’s exemplary description) core-limited.

380. Thus, this claim sub-element of claim element [1f] of Claim 1 of the '164 patent is rendered obvious by Saint along with the knowledge of a POSITA.

381. Finally, the analysis of this claim sub-element is particularly notable – since during prosecution, the Examiner allowed various claims of the application that led to the '164 patent on the grounds that “saved space” represented inventive material. In particular, the applicant amended what were at the time claims 5, 8, and 15 – so as to overcome the rejection based on Tamura (*see* Section VIII.B). In particular, the Applicant made these amendments to clarify that the “saved area” is between the non-continuous ESD buses and the non-continuous pad groups (e.g., “there is no ESD bus and no pad in the at least one saved area”). *See* Ex. 1002 at pp. 193-196 and p. 199. In particular, as mentioned above, the Applicant specifically stated that this amendment distinguished the application claims from the cited prior art: “In other words, in the instant application, at least one saved area is between the plurality of ESD buses and between the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area, which is different from Tamura’s teaching.” *See* Ex. 1002 at p. 206. In response, the Examiner basically agreed with the Applicant’s clarifications and assertions – providing only a request for a procedural clean-up of the claims: “[m]ore descriptive details are necessary to determine what is meant by ‘saved area’ for this invention. Once clarity is successfully realized the features in [dependent] claims 5, 8 and 15 which have this

(sic) features would be considered allowable if rewritten in independent form.” *See* Ex. 1002 at pp. 216-218.

382. However, as has been shown here, this is *not* inventive material – having been well-known (as shown above) in the prior art; thus, the Examiner (with all due respect) was incorrect in reaching this conclusion. For this additional reason, this claim sub-element of claim element [6e] of Claim 6 of the ’164 patent is unpatentable.

ii. [1f-2]: “each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups”

383. This claim sub-element of claim element [1f] of Claim 1 of the ’164 patent is rendered obvious by Saint in combination with the knowledge of a POSITA.

384. As an initial matter, the various aspects of the phrase “saved area” were already considered above in the discussion of claim sub-element [1f-1] (in Section XI.C.2.g.i) – and will not be further-discussed here. A POSITA would have been motivated to apply Saint’s “extra space” (saved area) teachings from Fig. 9-28 with Saint’s segmented GND bus approach (Saint, p. 162 (Figure 7-7)) to achieve the benefits of smaller chip size; further, as explained by Saint, the use of segmented buses improves the ESD protection architecture (and improves the isolation between

digital circuit blocks and analog circuit blocks (*id.*, p. 162)). This combined teaching is shown below – with orange highlighting used to denote the “saved area(s)” that are extant in Figure 7-7 of Saint:

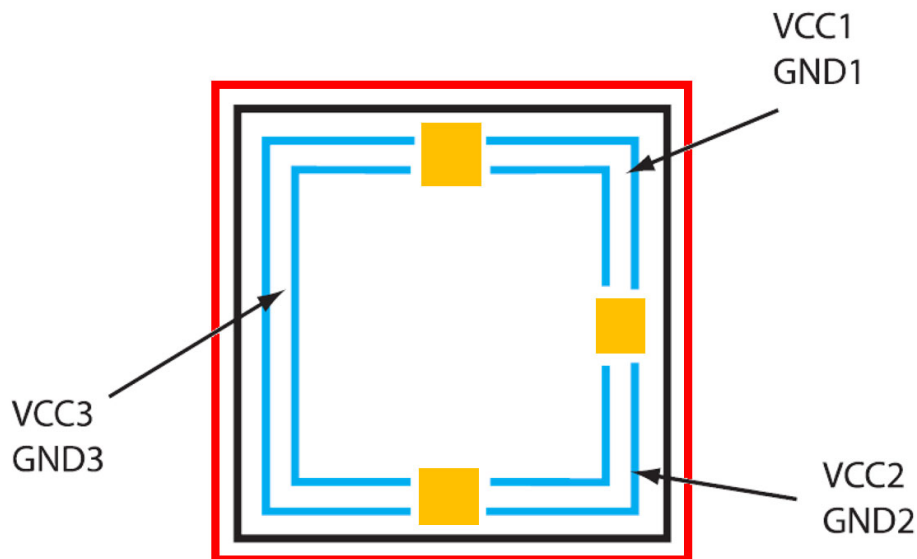


Figure 7-7. Pin-out simplification showing like protects grouped together.

(Annotations added, showing the “saved areas” annotated in orange.) Thus, Saint discloses the part of the claim element requiring that “each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses.” The only loose end is the last part of the claim sub-element – that at least one saved area be adjacent to “respective pads of two respective pad groups of the plurality of pad groups.” This part of the claim sub-element is disclosed by Saint in combination with the knowledge of a POSITA. At page 220, Saint describes the existence of “wasted space around the edges between the pads” – which (as will be confirmed by a figure from Saint, below) is the same thing as the “saved space” of the ’164 patent.

Further, Saint (also at p. 220) discloses that “... you can push some of your circuitry into this wasted space to try to use those gaps.” Saint shows this usage explicitly, in Figure 9-28:

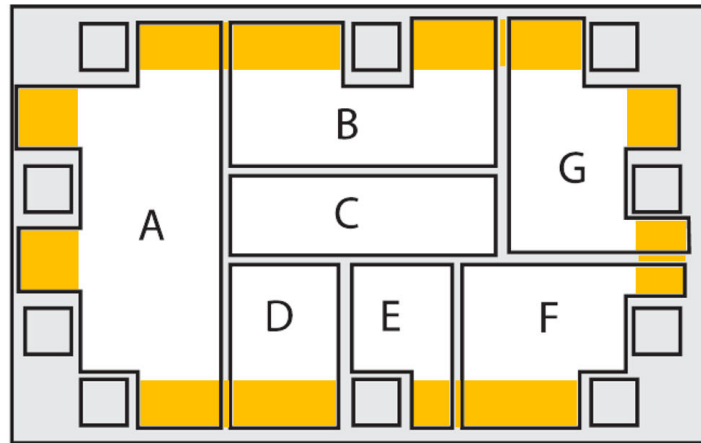


Figure 9–28. *We can use extra space surrounding our pads to shrink our chip size.*

Annotations are added to show the “saved space” identified by Saint. As Saint explains (on p. 221), “you can re-lay parts of your circuit elements in and around these pads trying to get the chip as small as possible.” Thus, Saint discloses, or at least renders obvious, that the circuit area comprises one or more saved areas that are each “adjacent to two ... respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.” A more complete depiction of an IC footprint combining Saint’s teachings from Figure 9-28 with Figure 7-7, which includes deployment of typical bond pad layouts around the periphery of the IC, is shown below.

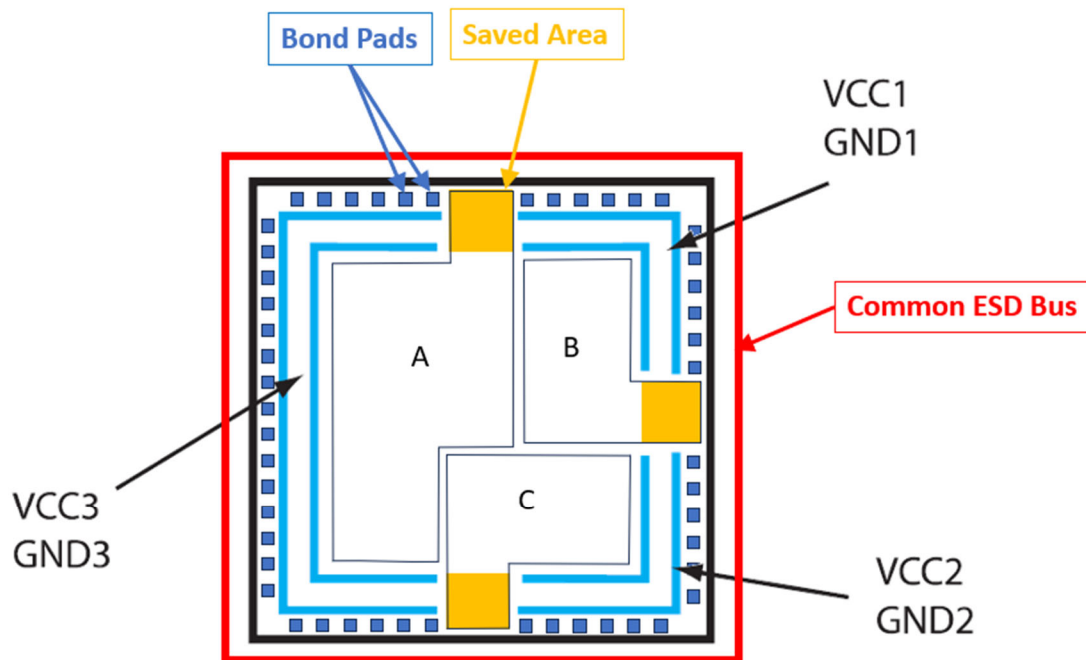


Figure 7–7. Pin-out simplification showing like protects grouped together.

Saint, 162 (Fig. 7-7) (annotated to show exemplary bond pads and circuit blocks). This image is only intended to be illustrative – and is not drawn to scale; however, it clearly shows that Saint’s separate teachings of pad placement and using “wasted space” (in a core-limited IC design situation) would have been (when combined with the knowledge of a POSITA) obvious to a POSITA. Further, this is supported by comparing this combined depiction with the exemplary 2010 microphotograph of a product IC that was presented above in Paragraph 379 (and elsewhere in this declaration) – as the same basic IC footprint structure appears in both depictions; that is, both are core-limited IC designs, both have wasted/saved spaces between the bond pads (i.e., pad groups), and both depict (verbally in Saint, by examination in the microphotograph) circuitry being deployed into those wasted/saved spaces.

385. Therefore, this claim sub-element of claim element [1f] is rendered obvious by Saint in combination with the knowledge of a POSITA.

iii. [1f] Summary

386. As just shown, Saint discloses claim sub-element [1f-1] of claim element [1f] of Claim 1 of the '164 patent, while Saint in combination with the knowledge of a POSITA discloses claim sub-element [1f-2] of claim element [1f] of Claim 1 of the '164 patent; therefore, this claim element of Claim 1 of the '164 patent is rendered obvious by Saint in combination with the knowledge of a POSITA.

h. Claim 1 Summary

387. For all of the reasons described above, Claim 1 of the '164 patent is rendered obvious Saint and the knowledge of a POSITA.

3. Claim 2: “The integrated circuit structure of claim 1, wherein each of the plurality of pad groups comprises at least one pad, and the plurality of bonding wires is configured to connect the at least one pad to the common ESD bus.”

388. Claim 2 is a dependent claim, and depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.C.2) that Claim 1 of the '164 patent is rendered obvious by the references cited there and the analysis provided there.

389. Further, Claim 2 provides material that was already provided in (and discussed above with respect to) claim elements [1c] and [1e] – and thus, Claim 2

(as will be confirmed below) is rendered obvious by Saint in combination with Haralabidis and the knowledge of a POSITA for the same reasons as described for claim elements [1c] and [1e].

4. Claim 3: “The integrated circuit structure of claim 1, wherein common ESD bus comprises a plurality [sic] discontinuous ESD bus groups.”

390. Claim 3 is a dependent claim, and depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.C.2) that Claim 1 of the '164 patent is rendered obvious by the references cited there and the analysis provided there.

391. Claim 3 is disclosed by Haralabidis. Here, I will not repeat the previous discussion of the '164 patent's meaning of “discontinuous” that was provided above.

392. As was explained in the overview of Haralabidis (in Section X.C) Haralabidis discloses an inventive embodiment (Figure 5) in which – in addition to the internal IC ground lines (which as used for receiving the energy of an ESD event) being segmented – the package substrate ground line (which is also used for receiving the energy of an ESD event) is also segmented (rather than being a single line, as is the case in Figure 3); the segments of the package substrate ground line are connected to a common ground line on the PC board (to which the packaged IC is mounted).

393. This can readily be seen in an annotated version of Figure 5 of Haralabidis:

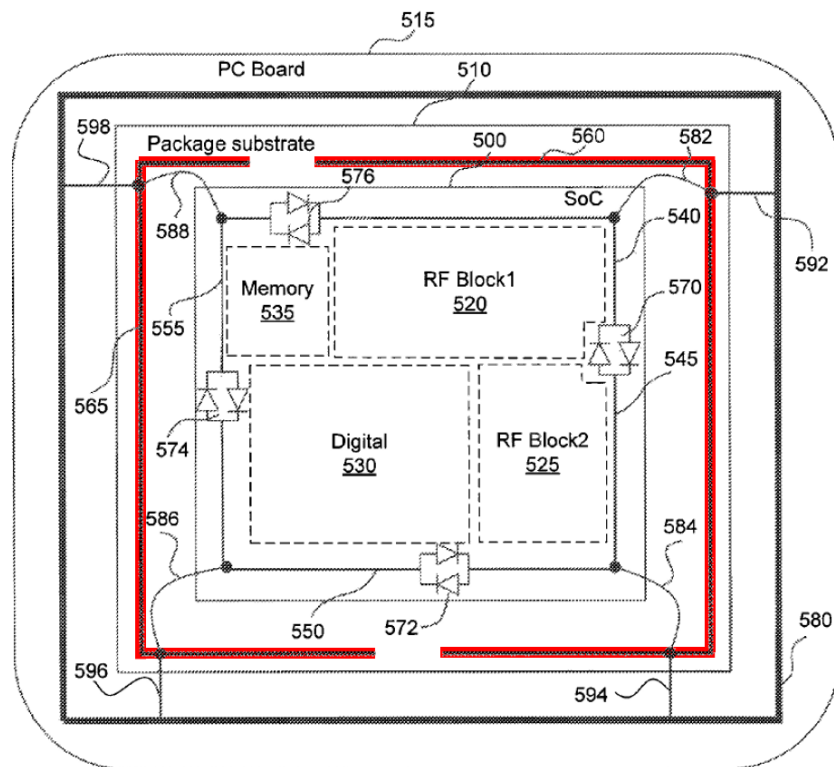


FIG. 5

The segmented lines of the ground lines (ESD bus segments) in the package substrate (560 and 565) provide a “common ESD bus” that “comprises a plurality” of “discontinuous ESD bus groups.” Further segmentation would have been a design choice – and thus an obvious variation of Haralabidis’ teaching regarding segmentation.

394. Finally, as the simple single-line package-substrate bus was shown to be readily used in Saint’s Figure 7-7 presentation (in claim element [1d], discussed in Section XI.C.2.e), in the same way it would be obvious to a POSITA to use this

segmented package-substrate bus in Saint's Figure 7-7 presentation – and that, as in Haralabidis Figure 5, this segmented bus can be connected to the common single-line ESD bus on the PC board to which the IC is mounted.

395. Therefore, Saint in combination with Haralabidis renders obvious Claim 3 of the '164 patent.

5. Claim 4: “The integrated circuit structure of claim 1, wherein the common ESD bus is formed outside the plurality of chip edges or inside the plurality of chip edges.”

396. Claim 4 is a dependent claim, and depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.C.2) that Claim 1 of the '164 patent is rendered obvious by the references cited there and the analysis provided there.

397. Although my analysis of Claim 4 in Ground 2 relied upon Figure 6 of Yoshinaga as the baseline integrated circuit, the same reasoning and analysis that I discussed there for applying Haralabidis' common ground rail teachings and placement (e.g., inside or outside the chip edges) applies here to Ground 3 in the same way – but with the baseline integrated circuit provided by Saint (e.g., Figures 9-28 and 7-7). Indeed, Haralabidis' teachings regarding common ground bus placement complement Saint's common ESD bus disclosure regarding “a continuous ring around the active circuitry.” Saint, p. 344. Thus, Saint combined with Haralabidis renders Claim 4 obvious.

6. Claim 5: “The integrated circuit structure of claim 1, wherein the common ESD bus is parallel to the plurality of ESD buses.”

398. Claim 5 is a dependent claim, and depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.C.2) that Claim 1 of the ’164 patent is rendered obvious by the references cited there and the analysis provided there.

399. Further, the additional requirements of claim 5 are all present in claim 13 (which I discuss further below, at Section XI.C.14) – and claim 5 is thus rendered obvious for the same reasons as is the case with claim 13. The fact that claim 5 is an apparatus claim and claim 13 is a method claim does not change the prior art analysis; similarly, the difference of “a common” in Claim 13 and “the common” in Claim 5 is immaterial.

400. Therefore, Claim 5 of the ’164 patent is rendered obvious by Saint in combination with Haralabidis.

7. Claim 6

401. Claim 6 is an independent claim, and is an apparatus claim. In addition, Claim 6 is almost identical to Claim 1 – with only one claim element being at all different.

a. [6-pre]: “An integrated circuit structure, comprising:”

402. As an initial matter, I will be offering no opinion regarding whether or not the preamble of Claim 6 is limiting; I have been instructed by counsel for the

Petitioner to assume that the preamble is limiting – and I have thus conducted my analysis using that assumption.

403. The preamble of Claim 6 is identical to the preamble of Claim 1; thus, the preamble of Claim 6 is rendered obvious for the same reasons discussed above (in Section XI.C.2.a) with respect to the preamble of Claim 1.

b. [6a]: “a circuit area;”

404. Claim element [6a] is identical to claim element [1a]; thus, claim element [6a] is rendered obvious for the same reasons discussed above (in Section XI.C.2.b) with respect to claim element [1a].

c. [6b]: “a plurality of ESD buses;”

405. Claim element [6b] is identical to claim element [1b]; thus, claim element [6b] is rendered obvious for the same reasons discussed above (in Section XI.C.2.c) with respect to claim element [1b].

d. [6c]: “a plurality of pad groups, adjacent and connected to the plurality of ESD buses; and”

406. Claim element [6c] is identical to claim element [1c]; thus, claim element [6c] is rendered obvious for the same reasons discussed above (in Section XI.C.2.d) with respect to claim element [1c].

e. [6d]: “a plurality of bonding wires configured to connect one to another of the plurality of pad groups;”

407. This claim element of Claim 6 of the '164 patent is rendered obvious by Saint in combination with Haralabidis and the knowledge of a POSITA.

408. In contrast to claim element [1d] (in which bond wires connect pad groups to a common ESD bus), the pad groups in claim element [6d] connect to each other. Compare claim elements [1d] and [1d] with claim element [6d].

409. Saint discloses using “ESD Ground Wiring” to “create[] a continuous ring around the active circuitry” to which ESD diodes are connected, as shown in Fig. CS1-99. Saint, p. 344. Saint also discloses that “[w]ire bonding is the most common method of attaching a chip to a package.” *Id.*, p. 207. Saint further discloses that “bond wires” connect to “bond pads on the chip.” *Id.*, pp. 202-204.

410. I have already discussed the state of the art and the knowledge of a POSITA as it relates to wire bonding generally - and connecting to bond pads on the same chip specifically - when analyzing claim element [6d] for Ground I (*see* Section XI.A.2.e, discussing Miller, Beauchamp, etc.). That discussion applies equally here – but is not repeated for brevity. Accordingly, one obvious way to connect Saint’s segmented reference potential lines—and perhaps the most obvious way—is by using “jumper” bond wires. Therefore, Saint in combination with the knowledge of a POSITA renders obvious this claim element of Claim 6 of the '164 patent.

411. Additionally, the combination of Saint and Haralabidis renders claim 6 obvious under the interpretation of claim element [6d] set forth in Patent Owner's infringement contentions in Exhibit 1025 – in which Patent Owner reads claim element [6d] so as to cover a common bus that indirectly connects pad groups. My analysis for claim element [6d] is the same as that described for claim element [1d] and Claim 13. More generally, under this interpretation, my opinions, and conclusions for all other elements of Claim 6 are the same as for Claim 1.

f. [6e]: “wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.”

412. Claim element [6e] is identical to claim element [1f]; thus, claim element [6e] is rendered obvious for the same reasons discussed above (in Section XI.C.2.g) with respect to claim element [1f].

g. Claim 6 Summary

413. For all of the reasons described above, Claim 6 of the '164 patent is rendered obvious by Saint in combination with Haralabidis and the knowledge of a POSITA.

- 8. Claim 7: “The integrated circuit structure of claim 6, wherein each of the plurality of pad groups comprises a connecting pad, and the plurality of bonding wires are configured to connect the connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups.”**

414. Claim 7 is a dependent claim, and depends from Claim 6; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.C.7) that Claim 6 of the ’164 patent is rendered obvious by the references cited there and the analysis provided there.

415. With regard to Claim 7, this claim is essentially a repetition of claim element [6d] of Claim 6 of the ’164 patent – with the only difference being the addition of the term “connecting pad” to identify the pads that are used to provide connections for the “jumper” bond wires that directly-connect together two bond pads (each of which is in a different pad group). As noted in the analysis of claim element [6d] (in Section XI.C.7.e), these “jumper” bond wires are depicted in Figure 3 of the ’164 patent:

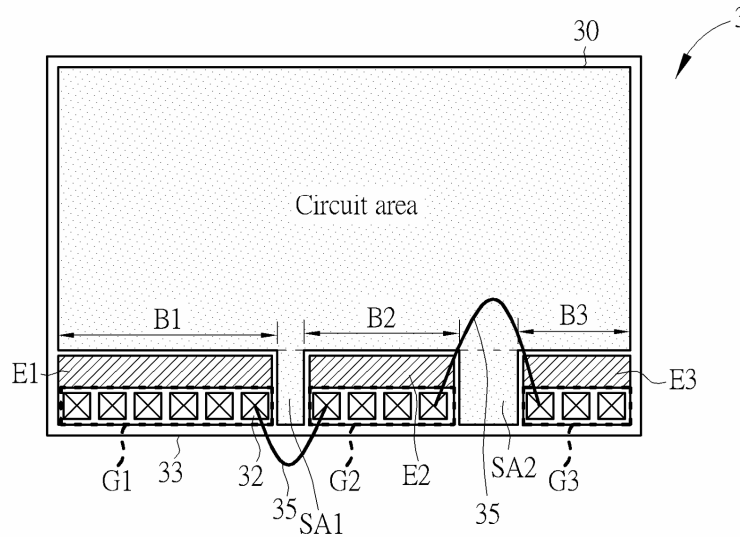


FIG. 3

As can be seen, the four depicted pads (that provide the pads for the “jumper” bond wires, two instances of 35) are used for these direct pad-to-pad connections.

416. Against this backdrop, a POSITA would have understood that Saint’s pads qualify as so-called “connecting pads” – because the purpose of a bond pad is to provide a connection point for a bond wire. As was described in the analysis of claim element [6d], the use of “jumper” bond wires to provide pad-to-pad connections was known in the art - disclosed, for example by both Miller and Beauchamp. In conventional practice a bond pad may have a “standard” size (to accommodate a single bond-wire connection and to meet process ground rules) - and that thus, any bond pad used for a “jumper” connection to another pad may not be available for connecting to a package trace (and thus to the package pin associated with that package trace); as explained in the analysis of claim element [6d], all of this was well-known to a POSITA at the time of the ’164 patent.

417. Thus, Claim 7 of the '164 patent is clearly about defining terminology to reflect the above reality – choosing to identify bond pads that are used solely for pad-to-pad “jumper” connections (and which are thus not available for connection to package traces) by a unique identifier. Since – as shown in the analysis of claim element [6d] – all of this was already known in the art, adding specific terminology for this is effectively meaningless.

418. Therefore, as claim element [6d] is rendered obvious by Saint in combination with the knowledge of a POSITA, Claim 7 is also rendered obvious by Saint in combination with the knowledge of a POSITA; the addition of terminology via Claim 7 provides no specific teachings – and no addition to the content of this dependent claim.

9. Claim 8

419. Claim 8 is an independent claim, and is a method claim.

420. Claim 8 is basically the method-claim version of the apparatus-claim Claim 1 – distinguished mostly by the addition of the word “forming” to the claim elements already stated in Claim 1; further, there are in Claim 8 no specific or additional teachings involving particular methods used to construct the apparatus described in Claim 1 – and as a result, , most of the analysis of Claim 8 can involve simply referring to the analysis already provided earlier with respect to Claim 1 –

with further discussion of only the differences (between Claim 8 and Claim 1) that appear in the elements of Claim 8.

a. [8-pre]: “A method of integrated circuit structure, comprising:”

421. As an initial matter, I will be offering no opinion regarding whether or not the preamble of claim 8 is limiting; I have been instructed by counsel for the Petitioner to assume that the preamble is limiting – and I have thus conducted my analysis using that assumption.

422. The preamble of Claim 8 is identical to the preamble of Claim 1 – other than that the preamble indicates that it is a method claim, while the preamble of Claim 1 indicates that it is an apparatus claim. As discussed just above, Claim 8 offers no specific or additional teachings involving particular methods used to construct the apparatus described in Claim 1; thus, for the reasons already discussed with respect to Claim 1, the preamble of Claim 8 is rendered obvious by Saint.

b. [8a]: “forming a circuit area;”

423. As per what was detailed above, claim element [8a] adds in the word “forming” – but is otherwise the same as claim element [1a]; as there are no further teachings involving specific methods used to form the structure disclosed in claim element [1a], for the reasons explained in Section XI.C.2.b claim element [8a] is rendered obvious by Saint.

c. [8b]: “forming a plurality of ESD buses;”

424. As per what was detailed above, claim element [8b] adds in the word “forming” – but is otherwise the same as claim element [1b]; as there are no further teachings involving specific methods used to form the structure disclosed in claim element [1b], for the reasons explained in Section XI.C.2.c claim element [8b] is rendered obvious by Saint.

d. [8c]: “forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses;”

425. The combination of Saint and Haralabidis renders this claim element obvious. The claim language “a plurality of pad groups ... wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses” is the same as the language in claim element [1c] – and is met here for the same reasons. The rest of the claim language is also disclosed by Saint.

426. To begin, claim element [8c] additionally recites “forming” pad groups, because claim 8 is a method claim; however, this difference has no impact on the prior art analysis. The analysis presented earlier (for claim element [1c]) explains how Saint discloses “pad groups,” which must have been “formed” or they would not exist.

427. Next, claim element [8c] further says that the “plurality of pad groups correspond[] to a plurality of discontinuous boundaries of the circuit area.” Saint

satisfies this aspect of claim element [8c] – as claim element [1f] discusses how Saint discloses using so-called “wasted space” between pads; Further, when Saint’s “extra space” teaching is applied to Saint Figure 7-7, the orange-annotated saved spaces are located as shown below.

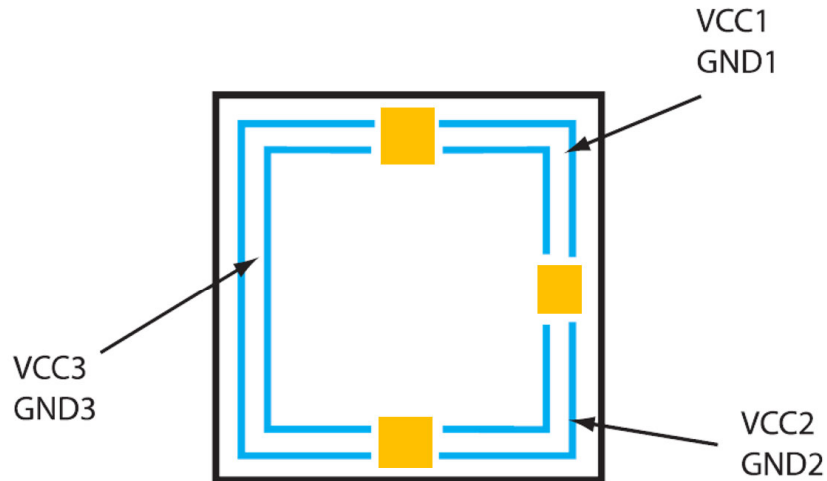


Figure 7-7. Pin-out simplification showing like protects grouped together.

Saint, p. 162 (Fig. 7-7) (annotated to show saved area(s) in orange). As discussed for claim element [8c], the ground pads (the claimed “pad groups”) for the respective ground segments thus correspond to the claimed “discontinuous boundaries of the circuit area,” akin to Saint Figure 9-28:

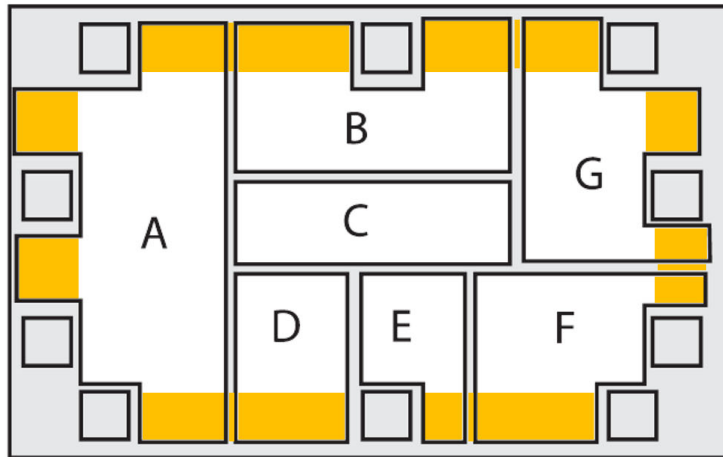


Figure 9–28. *We can use extra space surrounding our pads to shrink our chip size.*

Id., p. 221 (Fig. 9-28) (annotated). Thus, the combination of Saint and Haralabidis satisfies element [8.C].

e. [8d]: “forming a common ESD bus adjacent to the plurality of pad groups; and”

428. As per what was detailed above, claim element [8d] adds in the word “forming” – but is otherwise the same as claim element [1d]; as there are no further teachings involving specific methods used to form the structure disclosed in claim element [1d], for the reasons explained in Section XI.C.2.e claim element [8d] is rendered obvious by Saint.

f. [8e]: “connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires;”

429. This claim element is very similar to claim element [1e] (“a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD

bus”). However, Claim 1 is an apparatus claim, while Claim 8 is a method claim; thus, the differences that can be seen between claim element [8e] and claim element [1e] are largely due this structural difference – and both describe connecting a plurality of pad groups to the common ESD bus by a plurality of bonding wires, in the same way. Thus, most of claim element [8e] is rendered obvious for the same reasons as those discussed with respect to claim element [1e] (in Section XI.C.2.f).

430. The only wrinkle that causes claim element [8e] to differ from claim element [1e] is the use of language stating that this claim involves “connecting a plurality of pads corresponding to a plurality of pad groups” (continuing with “to the common ESD bus by a plurality of bonding wires”). However, in the analysis provided with respect to claim element [1e], it was shown that it would have been obvious to a POSITA to combine the Figure 3 embodiment of Haralabidis with the Figure 7-7 description of Saint:

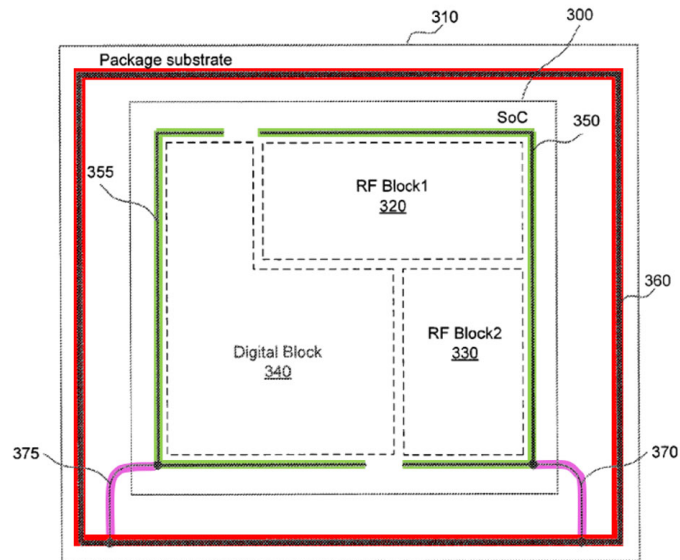


FIG. 3
Conventional Art

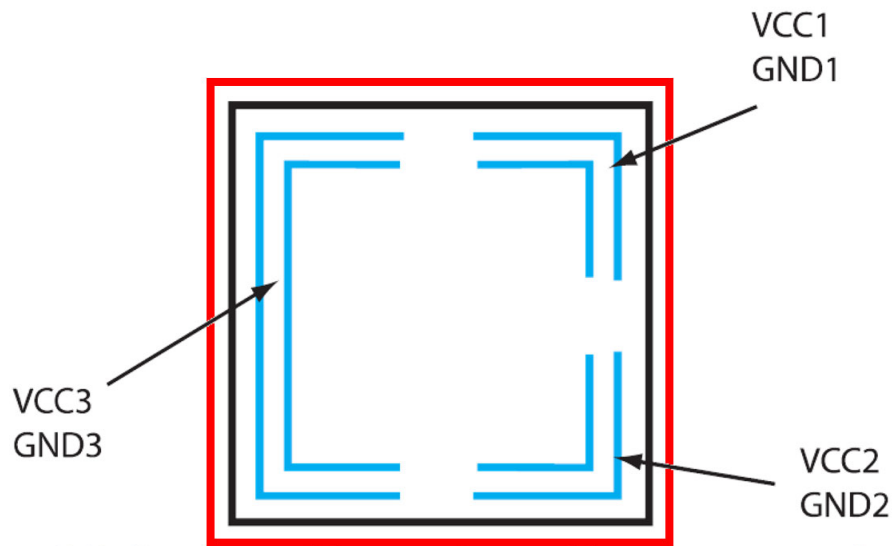


Figure 7-7. Pin-out simplification showing like protects grouped together.

431. The additional teachings of claim element [8e] were not considered in the discussion of claim element [1e] – as the relevant claim language (discussed just above) of claim element [8e] was simply not present in claim element [1e]. However, inspection of this combined embodiment shows that it also discloses claim

element [8e] – as the Figure 3 embodiment of Haralabidis includes structures that are “connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires,” and these are *de facto* included in the combined embodiment. In other words, each pad “corresponds” to the pad group to which it belongs. Of course, where a pad group comprises a single pad, that pad would necessarily be part of the pad group.

432. Therefore, this claim element is rendered obvious by Saint in combination with Haralabidis – for the same reasons as those described for claim element [1e] (in Section XI.C.2.f).

g. [8f]: “wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.”

433. Claim element [8f] is identical to claim element [1f]; thus, this claim element is rendered obvious for the reasons already discussed with respect to claim element [1f] (in Section XI.C.2.g).

h. Claim 8 Summary

434. For all of the reasons described above, Claim 8 of the ’164 patent is rendered obvious by Saint, in combination with Haralabidis and the knowledge of a POSITA.

- 10. Claim 9: “The method of integrated circuit structure of claim 8, wherein each of the plurality of pad groups comprises at least one pad, and the plurality of bonding wires is configured to connect the at least one pad to the common ESD bus.”**

435. Claim 9 is a dependent claim, and depends from Claim 8; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.C.9) that Claim 8 of the '164 patent is rendered obvious by the references cited there and the analysis provided there.

436. Aside from the opening indication that it is dependent from Claim 8, Claim 9 is otherwise identical to Claim 2; thus, for the same reasons as those discussed for Claim 2 (in Section XI.C.3), Claim 9 is rendered obvious for the same reasons discussed there.

- 11. Claim 10: “The method of integrated circuit structure of claim 8, further comprising: forming the common ESD bus outside the plurality of chip edges or inside the plurality of chip edges.”**

437. Claim 10 is a dependent claim, and depends from Claim 8; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.C.9) that Claim 8 of the '164 patent is rendered obvious by the references cited there and the analysis provided there.

438. Aside from the opening indication that it is dependent from Claim 8, Claim 10 is otherwise very similar to Claim 4. Claim 10 reads as:

further comprising: forming the common ESD bus outside the plurality of chip edges or inside the plurality of chip edges.

Aside from the opening indication that it is dependent from Claim 1, Claim 4 reads as:

wherein the common ESD bus is formed outside the plurality of chip edges or inside the plurality of chip edges.

The only difference between these two excerpts is due to Claim 10 being a method claim (which thus contains the method-claim language of “forming”), while Claim 4 is an apparatus claim (which thus contains the post-formation apparatus claim language of “wherein ... is formed”). Otherwise, the claim language and what is being claimed are identical.

439. Thus, for the same reasons as those discussed for Claim 4 (in Section XI.C.5), Claim 10 is rendered obvious for the same reasons discussed there.

12. Claim 11: “The method of integrated circuit structure of claim 8, wherein the common ESD bus is parallel to the plurality of ESD buses.”

440. Claim 11 is a dependent claim, and depends from Claim 8; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.C.9) that Claim 8 of the ’164 patent is rendered obvious by the references cited there and the analysis provided there.

441. Aside from the opening indication that it is dependent from Claim 8, Claim 11 is otherwise identical to Claim 5; thus, for the same reasons as those discussed for Claim 5 (in Section XI.C.6), Claim 11 is rendered obvious for the same reasons discussed there.

13. Claim 12

442. Claim 12 is an independent claim, and is a method claim. In addition, Claim 12 is almost identical to Claim 8 – with only one claim element being at all different.

a. [Claim 12 preamble]: “A method of integrated circuit structure, comprising:”

443. As an initial matter, I will be offering no opinion regarding whether or not the preamble of claim 12 is limiting; I have been instructed by counsel for the Petitioner to assume that the preamble is limiting – and I have thus conducted my analysis using that assumption.

444. The preamble of Claim 12 is identical to the preamble of Claim 8; thus, the preamble of Claim 8 is rendered obvious for the reasons already discussed (in Section XI.C.9.a) with respect to the preamble of Claim 8.

b. [12a]: “forming a circuit area;”

445. Claim element [12a] is identical to claim element [8a]; therefore, claim element [12a] is rendered obvious for the reasons already discussed (in Section XI.C.9.b) with respect to claim element [8a].

c. [12b]: “forming a plurality of ESD buses;”

446. Claim element [12b] is identical to claim element [8b]; therefore, claim element [12b] is rendered obvious for the reasons already discussed (in Section XI.C.9.c) with respect to claim element [8b].

d. [12c]: “forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are [sic] adjacent and connected to the plurality of ESD buses; and”

447. Claim element [12c] is identical to claim element [8c]; therefore, claim element [12c] is rendered obvious for the reasons already discussed (in Section XI.C.9.d) with respect to claim element [8c].

e. [12d]: “connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires across the circuit area;”

448. Claim element [12d] is rendered obvious by Saint and the knowledge of a POSITA.

449. This limitation is nearly identical to claim element [6d] – and Saint with a POSITA’s knowledge renders most of it obvious for the same reasons. There are

only two differences to note between claim element [6d] and claim element [12d]. The first arises because Claim 12 is a method claim, while Claim 6 is an apparatus claim. Claim element [12d] recites “connecting,” whereas claim element [6d] recites being “configured to connect”; however, this difference is immaterial, and makes no difference with respect to the earlier prior art analysis. The second difference is that in claim element [12d] the bond wires go “across the circuit area” – something which is not required by claim element [6d]. However, bond wire placement is a design choice – and a POSITA would have known that bond wires may be placed across (i.e., above) the circuit area. And for the same reasons already discussed for claim element [12d] of Ground 1 (in Section XI.A.2.e) doing so would have been obvious to a POSITA in view of Saint.

f. [12e]: “wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.”

450. Claim element [12e] is identical claim element [6e]; therefore, claim element [12e] is rendered obvious for the reasons already discussed (in Section XI.C.7.f) with respect to claim element [6e].

g. Claim 12 Summary

451. For all of the reasons described above, Claim 12 of the '164 patent is rendered obvious by Saint in combination with the knowledge of a POSITA.

14. Claim 13: “The method of integrated circuit structure of claim 12, wherein a common ESD bus is parallel to the plurality of ESD buses and the plurality of pad groups.”

452. Claim 13 is a dependent claim, and depends from Claim 12; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.C.13) that Claim 12 of the '164 patent is rendered obvious by the references cited there and the analysis provided there.

453. Further, Claim 13 is a method claim; however, as in multiple situations considered above, there are no further teachings involving specific methods used to form the structures disclosed in Claim 13. Thus, there is nothing about Claim 13 being a method claim that otherwise distinguishes it from the apparatus claims that will be cited below for the analysis.

454. In the discussion of claim element [1d], it was shown that it would be obvious to combine the common ESD bus of Haralabidis Figure 3 with the Figure 7-7 description of Saint – producing the following combined embodiment:

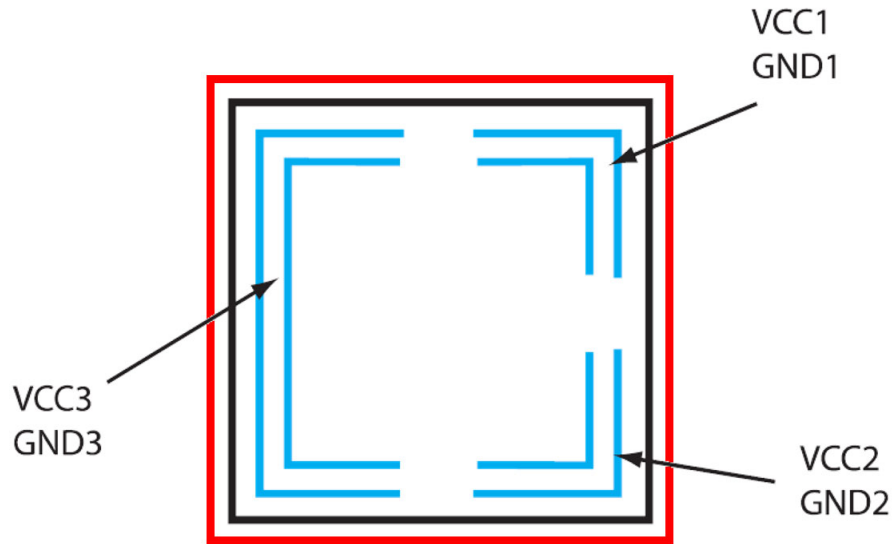


Figure 7-7. Pin-out simplification showing like protects grouped together.

As can readily be seen, in this combined embodiment, the common ESD bus of Haralabidis (annotated in red) is parallel to the plurality of ESD buses on any of the four sides of the structure of the Figure 7-7 description of Saint (in this combined embodiment).

455. While Saint only shows two more segmented buses (and their associated pad groups) on a single edge of a chip, it would have been obvious to have three (or more) such buses (and their associated pad groups) on the same chip edge – in which case they too would meet the “parallel” requirement, discussed below.

456. Claim 13 also requires that the “common ESD bus is parallel to ... the plurality of pad groups.” As can be seen, the pads of Saint Figure 9-28 (below) run parallel to the chip edges – which align with the segmented ground buses and the

common ground rail (as shown in the modified Figure 7-7, above). Thus, the combined teachings of these two figures (*viz.*, placing the pads around the periphery of Saint Figure 7-7) result in a plurality of pad groups on each of the four sides of the IC – and such that the common bus is “parallel” to the pad groups, which were commonly placed around the periphery of the integrated circuit and parallel to the edges of the die.

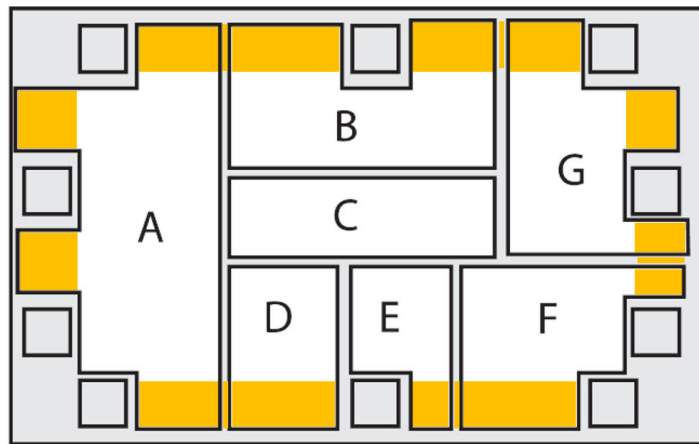


Figure 9–28. We can use extra space surrounding our pads to shrink our chip size.

457. Therefore, Claim 13 in *toto* is rendered obvious by Saint in combination with Haralabidis.

- 15. Claim 14: “The method of integrated circuit structure of claim 12, wherein each of the plurality of pad groups comprises a connecting pad, and the plurality of bonding wires are configured to connect the connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups.”**

458. Claim 14 is a dependent claim, and depends from Claim 12; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XII.C.13) that Claim 12 of the '164 patent is rendered obvious by the references cited there and the analysis provided there.

459. Further, Claim 14 is identical to claim 7 – and is thus rendered obvious for the same reasons provided for the obviousness of Claim 7 (in Section XI.C.8).

XII. SECONDARY CONSIDERATIONS

460. Based on my review of the '164 patent's file history, I note that no secondary considerations of non-obviousness were identified in connection with the patent's claims. Nor am I otherwise aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, or the like relating to the '164 patent. Instead, as discussed above, it is my opinion that the subject matter embraced by the challenged claims was known in and obvious over the prior art. If I later become aware of arguments of any secondary consideration, I may assess those arguments when they arise, in order to form opinions regarding their correctness; I reserve the right to file supplemental declarations should such circumstances occur.

XIII. CONCLUSION

461. I am aware that this declaration will be filed as evidence in an IPR proceeding before the PTAB. I am aware that making willfully false statements in my declaration are punishable by fine or imprisonment, or both (under 18 U.S.C. § 1001), and thus such actions may compromise the validity of the IPR Petition. All statements herein made by me of my own knowledge are true, and all statements made on information and belief are believed to be true.

462. I declare under penalty of perjury that the foregoing is true and correct.

Executed this 14th day of November, 2024 in Fletcher, Vermont.



Daniel Foty, Ph.D.