

(19) Japan Patent Office (JP)

**(12) Japanese Unexamined Patent
Application Publication (A)**(11) Japanese Unexamined
Patent Application
Publication Number
**JP2006-93598 (P2006-
93598A)**(43) Publication date **April 6, 2006 (4.6.2006)**

(51) Int. Cl.	F1	Theme codes (reference)
H01L 27/04 (01.2006)	H01L 27/04 H	5F038
H01L 21/822 (01.2006)		

Request for examination	Not yet requested	Number of claims 5OL	(Total of 16 pages)
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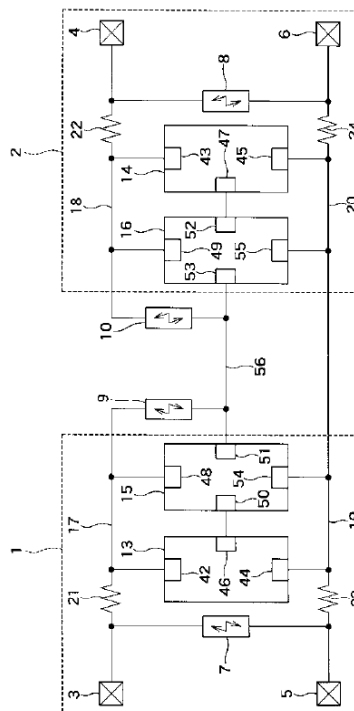
(54) [Title of the Invention] Semiconductor integrated circuit

(57) [Abstract]

[Problem] To improve ESD resistance in a semiconductor integrated circuit having a plurality of circuits each having an separated power supply line and signal propagation paths disposed between the circuits.

[Means for Solving] First and second power supply lines, first and second reference potential lines, first and second circuits connected to the first and second power supply lines and the first and second reference potential lines, a signal line connecting the first and second circuits, a protective element connected between the first power supply line and the signal line that, when over-voltage is applied between the first power supply line and the signal line, flows current between the first power supply line and the signal line in response to the direction of application of over-voltage, and a protective element connected between the second power supply line and the signal line that, when over-voltage is applied between the second power supply line and the signal line, flows current between the second power supply line and the signal line in response to the direction of application of over-voltage.

[Representative Drawing] FIG. 1



[Scope of Patent Claims]

[Claim 1]

Comprising a first and second power supply terminal for supplying first and second power supply voltages;
 a first and second power supply line connected to the first and second power supply terminals;
 a first and second reference potential terminal for providing a first and second reference potential;
 a first and second reference potential line connected to the first and second reference potential terminals;
 a first circuit having a first internal circuit power supply terminal connected to the first power supply line, a first internal circuit reference potential terminal connected to the first reference potential line, and a signal output terminal outputting a generated signal, the first circuit operating at the first power supply voltage during normal operation;

a second circuit having a second internal circuit power supply terminal connected to the second power supply line, a second internal circuit reference potential terminal connected to the second reference potential line, and a signal input terminal inputting a signal generated by the first circuit, the second circuit operating at the second power supply voltage during normal operation;

a signal line connecting the signal output terminal and the signal input terminal;

a reference potential line connection connecting the first and second reference potential lines;

a first protective element connected in parallel with the first circuit between the first power supply line and the first reference potential line and on when an over-voltage higher than the first power supply voltage is applied between the first internal circuit power supply terminal and the first internal circuit reference potential terminal in non-operation of the first circuit, which prevents electrostatic breakdown of the first circuit by flowing current from the first power supply line to the first reference potential line or vice versa in response to the direction of application of the over-voltage;

a second protective element connected in parallel with the second circuit between the second power supply line and the second reference potential line and on when an over-voltage higher than the second power supply voltage is applied between the second internal circuit power supply terminal and the second internal circuit reference potential terminal in non-operation of the second circuit, to prevent electrostatic breakdown of the second circuit by flowing current from the second power supply line to the second reference potential line or vice versa in response to the direction of application of the over-voltage;

a third protective element connected between the first power supply line and the signal line and on when an over-voltage is applied between the first internal circuit power supply terminal and the signal output terminal that is higher than the first power supply voltage during non-operation of the first circuit to prevent electrostatic breakdown of the first circuit by flowing current from the first power supply line to the signal line or vice versa in response to the direction of application of the over-voltage; and

a fourth protective element connected between the second power supply line and the signal line and on when an over-voltage is applied between the signal input terminal and the second internal circuit power supply terminal that is higher than the second power supply voltage during non-operation of the second circuit to prevent electrostatic breakdown of the second circuit by flowing current from the second power supply line to the signal line or vice versa in response to the direction of application of the over-voltage;

a semiconductor integrated circuit.

[Claim 2]

Wherein a fifth protective element connected between the signal line and the first reference potential line and on when an over-voltage higher than the first power supply voltage is applied between the signal output terminal and the first internal circuit reference potential terminal to prevent electrostatic breakdown of the first circuit by flowing current from the signal line to the first reference potential line or vice versa in response to the direction of application of the over-voltage; and

a sixth protective element connected between the signal line and the second reference potential line and on when an over-voltage higher than the second power supply voltage is applied between the signal input terminal and the second internal circuit reference potential terminal to prevent electrostatic breakdown of the second circuit by passing current from the signal line to the second reference potential line or vice versa in response to the direction in which the over-voltage is applied;

the semiconductor integrated circuit according to claim 1.

[Claim 3]

The semiconductor integrated circuit according to claim 1 or 2, characterized in that the third and fourth protective elements are each one or more diodes connected in anti-parallel, or diodes connected in anti-parallel in a plurality of

stages connected in series.

[Claim 4]

The semiconductor integrated circuit according to claim 1 or 2, characterized in that the third protective element and the fourth protective element each include a MOS transistor and have a first terminal connected to a gate, a source, and a body in common, and a second terminal connected to a drain.

[Claim 5]

Wherein the first circuit has, as its output, a first inverter with one end connected to the first power supply line and the other end connected to the first reference potential line and an output connected to the signal line; and

the second circuit has, as its input, a second inverter, one end connected to the second power supply line and the other end connected to the second reference potential line and an input connected to the signal line;

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the semiconductor integrated circuit according to any of claims 1 to 4.

[Detailed description of the invention]

[Technical field]

[0001]

The present invention relates to a semiconductor integrated circuit having an Electro Static Discharge (ESD) protection circuit.

[Background art]

[0002]

As integrated circuits become smaller each year, the electrostatic breakdown voltage of semiconductor elements such as transistors decreases, and electrostatic breakdown protection circuits (ESD protection circuits) become more important. In particular, in a CMOS (Complementary Metal Oxide Semiconductor) thin film element with a gate insulating film thickness of about 1 nm, the dielectric film breakdown voltage is only about 4 V.

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[0003]

Integrated circuits are also becoming large-scale integrated circuits (LSIs), and some have more than 1,000 terminals for power and signals supplied from outside the integrated circuit. To ensure the ESD (Electro Static Discharge) resistance of an integrated circuit, appropriate ESD protection must be provided between all terminals of the integrated circuit. However, the greater the number of terminals, the more difficult it is to ensure ESD resistance. For example, if an ESD voltage is applied between terminals placed on opposite sides of a rectangular LSI chip or between diagonally placed pads, problems are likely to arise. This is partly due to the longer wiring and greater wiring resistance due to the distant pad-to-pad spacing. In such cases, ESD resistance is lower than in the case of adjacent pad-to-pad spacing.

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[0004]

The internal circuitry of an LSI may have different supply voltages depending on its operating functions. In addition, even in circuits with the same operating voltage, analog circuits often have separate power supply lines and reference potential lines to prevent noise from being introduced from digital circuits through the power supply wiring. Circuits with separated power sources are extremely vulnerable in terms of ESD resistance, and there are many challenges with ESD protection network design.

[0005]

Circuits having separated power supply lines are not usually completely separated from each other, and one of multiple reference potential lines is used as a main ESD discharge path, and multiple reference potential lines are connected to each other. The reference potential lines may be connected by bidirectional diodes that are connected in parallel to one another in the opposite direction to avoid noise.

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[0006]

Even circuits that have separate power lines are often connected to each other by signal lines. The circuit portion that outputs a signal to this signal line, or the circuit portion from which the signal is input, is referred to here as the signal boundary. Signals is transferred between circuits through this signal boundary. The signal boundary portion corresponds to the signal input/output portion, and may be a variety of circuits, for example an inverter-based buffer circuit.

[0007]

However, in the past, there has been a problem in the LSI with regard to multiple circuits with separate power supply lines, where each circuit is connected with a signal line to each other, that the ESD resistance is significantly weaker than when each circuit is not connected with a signal line to each other.

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[Patent Literature 1] JP2000-269432

[Disclosure of the Invention]

[Problems to be Solved by the Invention]

[0008]

The present invention is intended to improve ESD resistance in a semiconductor integrated circuit having a plurality of circuits each having an separated power supply line and having a signal propagation path disposed between the circuits.

[Methods of solving the problems]

[0009]

A semiconductor integrated circuit according to one aspect of the present invention comprises: a first and second power supply terminal for supplying first and second power supply voltages; a first and second power supply line connected to the first and second power supply terminals; a first and second reference potential terminal for providing a first and second reference potential; a first and a second reference potential line connected to the first and second reference potential terminals; a first internal circuit power supply terminal connected to the first power supply line; a first internal circuit reference potential terminal connected to the first reference potential line; a signal output terminal outputting the generated signal; a first circuit operating under the first power supply voltage during normal operation; and a second internal circuit power supply terminal connected to the second power supply line; a second internal circuit reference potential terminal connected to the second reference potential line; a signal input terminal for inputting a signal generated by the first circuit; a second circuit operating under the second power supply voltage during normal operation; a signal line connecting the signal output terminal and the signal input terminal; a reference potential line connection connecting the first and second reference potential lines; connected in parallel with the first circuit between the first power supply line and the first reference potential line; turns on when an over-voltage is applied between the first internal circuit power supply terminal and the first internal circuit reference potential terminal that is higher than the first power supply voltage in non-operation of the first circuit; a first protective element which is turned on when an over-voltage higher than the first power supply voltage is applied between the first internal circuit power supply terminal and the first internal circuit reference potential terminal while the first circuit is not in operation, and which prevents electrostatic breakdown of the first circuit by causing a current to flow from the first power supply line to the first reference potential line or vice versa depending on the direction in which the over-voltage is applied; a second protective element that is connected in parallel with the second circuit between the second power supply line and the second reference potential line, and that turns on when an over-voltage higher than the second power supply voltage is applied between the second internal circuit power supply terminal and the second internal circuit reference potential terminal while the second circuit is not in operation, and prevents electrostatic breakdown of the second circuit by causing a current to flow from the second power supply line to the second reference potential line or vice versa depending on the direction in which the over-voltage is applied; a third protective element that is connected between the first power supply line and the signal line, and that is turned on when an over-voltage higher than the first power supply voltage is applied between the first internal circuit power supply terminal and the signal output terminal while the first circuit is not in operation, and that prevents electrostatic breakdown of the first circuit by causing a current to flow from the first power supply line to the signal line or vice versa depending on the direction in which the over-voltage is applied; and a fourth protective element that is connected between the second power supply line and the signal line, and that turns on when an over-voltage higher than the second power supply voltage is applied between the signal input terminal and the second internal circuit power supply terminal while the second circuit is not in operation, and prevents electrostatic breakdown of the second circuit by causing a current to flow from the second power supply line to the signal line or vice versa depending on the direction in which the over-voltage is applied.

[Effect of the Invention]

[0010]

According to the present invention, ESD resistance can be improved in a semiconductor integrated circuit having a plurality of circuits each having an separated power supply line and signal propagation paths disposed between the circuits.

[Best mode for carrying out the invention]

[0011]

Hereinafter, one embodiment of the present invention will be described with reference to the drawings.

[0012]

FIG. 1 is a block diagram illustrating an example configuration of a semiconductor integrated circuit according to an

embodiment of the present invention.

[0013]

The semiconductor integrated circuit of FIG. 1 broadly comprises a circuit 1 and a circuit 2, and one of the major features of the present invention, an ESD protective element 9 and an ESD protective element 10.

[0014]

The circuit 1 has, as a circuit element, an internal circuit 13, a signal boundary portion 15, an ESD protective element 7, a power supply pad 3, a reference potential pad 5, a power supply wiring resistance 21, a reference potential line wiring resistance 23, a power supply line 17 and a reference potential line 19.

[0015]

An ESD protective element 7 is connected between the power supply pad 3 and the reference potential pad 5. A power supply line wiring resistance 21 is connected between power supply pad 3 and both internal circuit 13 and signal boundary portion 15. In addition, a reference potential line wiring resistance 23 is connected between reference potential pad 5 and internal circuit 13 and between reference potential pad 5 and signal boundary portion 15 .

[0016]

In general, internal circuit 13 is composed of a circuit comprising a number of elements. The power supply line wiring resistance 21 and the reference potential line wiring resistance 23 are also composed of a number of resistive elements, each represented by one resistance to simplify the description.

[0017]

The internal circuit 13 has an internal circuit power supply terminal 42, an internal circuit reference potential terminal 44, and an internal circuit signal terminal 46 connected to a signal boundary portion signal terminal 50 at a subsequent signal boundary portion 15.

[0018]

Here, the internal circuit signal terminal 46 is not for input/output with the outside of the semiconductor integrated circuit (e.g., other chips), but for input/output of signals within the integrated circuit. The signal terminals that perform input/output with the exterior of the semiconductor integrated circuit do not appear in the description in FIG. 1, so the illustration is omitted.

[0019]

Although only one internal circuit power supply terminal 42, internal circuit reference potential terminal 44 and internal circuit signal terminal 46 in internal circuit 13 are depicted here, there are usually multiple respective terminals in actual integrated circuits, including this example. Each is represented by one terminal here for simplicity.

[0020]

The internal circuit power supply terminal 42 is connected to the power supply line 17 and the internal circuit reference potential terminal 44 is connected to the reference potential line 19.

[0021]

The signal boundary portion 15 includes a signal boundary portion signal terminal 50, a signal boundary portion signal terminal 51 connected to another power supply circuit, a signal boundary portion power supply terminal 48, and a signal boundary portion reference potential terminal 54. The signal boundary portion 15 includes, for example, an inverter. If the signal boundary portion 15 includes an inverter, the source of the pull-up PMOS transistor is connected to the signal boundary portion power supply terminal 48, the drain is connected to the drain of the pull-down NMOS transistor, and the source of the pull-down NMOS transistor is connected to the signal boundary portion reference potential terminal 54. The gates of both transistors are connected in common to the signal boundary portion signal terminal 50 and the output is connected to the signal boundary portion signal terminal 51.

[0022]

Although only one signal boundary portion power supply terminal 48, signal boundary portion reference potential terminal 54, signal boundary portion signal terminal 50 and signal boundary portion signal terminal 51 at signal boundary portion 15 are depicted here, there are usually multiple respective terminals in actual integrated circuits, and the present invention includes this. Each is represented by one terminal here for simplicity.

[0023]

The signal boundary portion power supply terminal 48 is connected to the power supply line 17 and the signal boundary portion reference potential terminal 54 is connected to the reference potential line 19.

[0024]

The configuration of circuit 2 is similar to that of circuit 1.

[0025]

That is, an ESD protective element 8 is connected between the power supply pad 4 and the reference potential pad 6. A power supply line wiring resistance 22 is connected between power supply pad 4 and both internal circuit 14 and signal boundary portion 16. Also, a reference potential line wiring resistance 24 is connected between the reference potential pad 6 and the internal circuit 14 and the signal boundary portion 16.

[0026]

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The internal circuit 14 has an internal circuit power supply terminal 43, an internal circuit reference potential terminal 45, and an internal circuit signal terminal 47 connected to a signal boundary portion signal terminal 52 at signal boundary portion 16.

[0027]

The internal circuit power supply terminal 43 is connected to the power supply line 18 and the internal circuit reference potential terminal 45 is connected to the reference potential line 20.

[0028]

The signal boundary portion 16 includes a signal boundary portion signal terminal 52, a signal boundary portion signal terminal 53, a signal boundary portion power supply terminal 49, and a signal boundary portion reference potential terminal 55. The signal boundary portion 16 includes, for example, an inverter. If the signal boundary portion 16 includes an inverter, the source of the pull-up PMOS transistor is connected to the signal boundary portion power supply terminal 49, the drain is connected to the drain of the pull-down NMOS transistor, and the source of the pull-down NMOS transistor is connected to the signal boundary portion reference potential terminal 55. The gates of both transistors are connected in common to the signal boundary portion signal terminal 53, and the output is connected to the signal boundary portion signal terminal 52.

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[0029]

The signal boundary portion power supply terminal 49 is connected to the power supply line 18 and the signal boundary portion reference potential terminal 55 is connected to the reference potential line 20.

[0030]

signal boundary portion signal terminal 51 of signal boundary portion 15 in circuit 1 and signal boundary portion signal terminal 53 of signal boundary portion 16 in circuit 2 are connected by signal line 56. In an actual integrated circuit, there are usually a plurality of signal lines 56, and the present invention includes this. Here, only one is illustrated for simplicity.

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[0031]

An ESD protective element 9 is connected between the signal line 56 and the power supply line 17 in the circuit 1, and an ESD protective element 10 is connected between the signal line 56 and the power supply line 18 in the circuit 2.

[0032]

Although only two ESD protective elements, ESD protective element 9 and ESD protective element 10, are depicted in FIG. 1, if there are multiple signal lines 56, ESD protective elements corresponding to ESD protective element 9 and ESD protective element 10 are added for each signal line, respectively. Here, it is necessary to use an ESD protective element 9 and an ESD protective element 10 that has the ability to perform ESD discharge in two directions.

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[0033]

As ESD protective element 9 and ESD protective element 10, for example, one or more diodes can each be connected in anti-parallel, or these anti-parallel connections further connected in series can be used. In addition, a MOS transistor having a first terminal connected to a common gate, source, and body, and a second terminal connected to a drain can also be used.

[0034]

Described below is the case where an ESD voltage is applied between the power supply pad 3 and the power supply pad 4 in such a semiconductor integrated circuit. In the case where a voltage is applied, for example, in the case of a

semiconductor integrated circuit device alone or mounted on a mounting board, an over-voltage due to static electricity generated during handling or transport may be applied between the power supply pad 3 and the power supply pad 4.

[0035]

When an ESD voltage is applied between the power supply pad 3 and the power supply pad 4 to apply an over-voltage higher than the normal operating voltage to the internal circuit 13, the ESD protective element 7 and the ESD protective element 8 are turned on. Then, ESD current flows through the power supply pad 3, the ESD protective element 7, the reference potential line wiring resistance 23, the reference potential line wiring resistance 24, and the ESD protective element 8 to the power supply pad 4. However, if the polarity of the ESD voltage applied between the power supply pad 3 and the power supply pad 4 is reversed, the current path is reversed.

[0036]

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On the other hand, there is also an ESD discharge path through signal line 56. This is the path from the power supply pad 3 to the power supply pad 4 through the power supply line wiring resistance 21, the ESD protective element 9, the signal line 56, the ESD protective element 10, and the power supply line wiring resistance 22. However, as described above, if the polarity of the voltage applied between the power supply pad 3 and the power supply pad 4 is reversed, the current path is reversed.

[0037]

Here, we consider the conditions under which signal boundary portion 15 and signal boundary portion 16 break down.

[0038]

As a prerequisite, the ESD current through signal line 56 is negligible (the on voltage and on resistance values of ESD protective elements 7, 8, 9, 10 and the values of each resistance 21-24 are designed so that reference potential line 19 is the main path of the ESD current), and thus the voltage drop at power supply line wiring resistance 21 and power supply line wiring resistance 22 is negligible.

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[0039]

It is assumed that the signal boundary portion signal terminal 51 of signal boundary portion 15 is in the high level output state and is at the same potential as signal boundary portion power supply terminal 48. More specifically, for example, the signal boundary portion 15 includes an inverter. The state of the inverter is considered to be a floating state, so any state is possible due to noise, but here it is assumed that the output is high level. This condition is the weakest against ESD. As a result, the potential of signal line 56 is the same as that of power supply pad 3.

[0040]

On the other hand, the potential of the signal boundary portion power supply terminal 49 of the signal boundary portion 16 is the same as the power supply pad 4.

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[0041]

Therefore, an ESD voltage is applied between the signal boundary portion signal terminal 53 and the signal boundary portion power supply terminal 49.

[0042]

An ESD protective element 10 is connected between the signal boundary portion signal terminal 53 and the signal boundary portion power supply terminal 49, and if the ESD protective element 10 is clamped at or below the insulation breaking voltage, the signal boundary portion 16 is protected. When clamping is performed for ESD at ESD protective element 10, ESD current flows to ESD protective element 10. In the range where the ESD current is small, the current path at the signal boundary portion 15 side is from the signal boundary portion power supply terminal 48 to the signal boundary portion signal terminal 51.

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[0043]

Here, when the ESD current becomes larger and the ESD current exceeds the permissible current of the element at the signal boundary portion 15, the signal boundary portion power supply terminal 48 and the signal boundary portion signal terminal 51 no longer have the same potential (the signal boundary portion 15 is often composed of transistors of small dimensions, and the current driving capacity is usually low), resulting in a potential difference. The higher the ESD voltage, the greater the potential difference.

[0044]

However, since the ESD protective element 9 and the ESD protective element 10 are turned on and clamped before the breaking voltage is reached, the signal boundary portion 15 and signal boundary portion 16 are protected. That is, the

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signal boundary portion 15 or signal boundary portion 16 breaks down if the clamp voltage of either the ESD protective element 9 and the ESD protective element 10 exceeds the insulation film breaking voltage (e.g., the insulation breaking voltage of the gate insulating film in the transistors that make up the signal boundary portion 15 and signal boundary portion 16 to be protected).

[0045]

If the ESD protective element 9 and the ESD protective element 10 are configured with the same element, the clamp voltages are equal. If circuit 1 and circuit 2 operate at the same power supply voltage and are configured with elements of the same insulation film breaking voltage, the breaking voltage (voltage applied between power supply pad 3 and power supply pad 4) via the signal boundary is twice the insulation film breaking voltage.

[0046]

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On the other hand, circuit 1 does not break unless the sum of the clamp voltage of ESD protective element 7 and the voltage drop due to reference potential line wiring resistance 23, i.e., the voltage difference between power supply line 17 and reference potential line 19, exceeds the insulation film breaking voltage of circuit 1 (the current flowing through reference potential line wiring resistance 23 is sufficiently greater than power line wiring resistance 21, so the voltage drop of power supply line wiring resistance 21 is ignored). Similarly, circuit 2 will not break down unless the sum of the clamp voltage of the ESD protective element 8 and the voltage drop due to the reference potential line wiring resistance 24, i.e., the potential difference between the power supply line 18 and the reference potential line 20, exceeds the insulation film breakdown voltage of circuit 2 (the current flowing through reference potential line wiring resistance 24 is sufficiently greater than power line wiring resistance 22, so the voltage drop of power supply line wiring resistance 22 is ignored). In other words, when focusing on the discharge path of the reference potential line, a maximum of twice the insulation breakdown voltage is allowed between the power supply pad 3 and the power supply pad 4.

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[0047]

In the circuits previously implemented by the present inventor, there were no ESD protective element 9 and ESD protective element 10 in the circuit of FIG. 1, and when the voltage between the power supply pad 3 and the power supply pad 4 reached the dielectric breakdown voltage, there was a problem that the signal boundary portion 15 or signal boundary portion 16 would break (e.g., if the signal boundary portion 15 is in the inverter and the pull-up PMOS transistor is on, the voltage between the power supply pad 3 and the signal boundary portion signal terminal 53 and the signal boundary portion 16). In contrast, in accordance with the present embodiment, the ESD protective element 9 and the ESD protective element 10 were provided between the power supply lines 17, 18 and the signal line 56, thereby increasing the ESD voltage tolerance by up to twice.

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[0048]

Here, the clamp voltage of the ESD protective element 7 and the ESD protective element 8 usually depends on the polarity of the applied voltage.

[0049]

For example, if a gate grounded NMOS (ggNMOS) transistor is used as an ESD protective element and a positive voltage is applied to the drain, the snapback characteristic is exhibited, and the clamp voltage is determined by the reverse breakdown voltage of the PN junction and the voltage drop due to the channel resistance. On the other hand, forward characteristics of the PN junction are exhibited when a negative voltage is applied to the drain.

[0050]

In this way, if the clamp voltage of the ESD protective element is different depending on the polarity of the applied voltage, and the ESD voltage is applied between the power supply pads, one ESD protective element will be clamped in the opposite direction and the other ESD protective element will be clamped in the forward direction, so it will not operate at the same time. Thus, in this case, the protective limit of the ESD protective element is not twice the insulation film breakdown voltage.

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[0051]

Here, the ESD protective element used for clamping the signal boundary can use a smaller size element than the ESD protective element used between the power supply pad and the reference potential pad. This will be explained in more detail below.

[0052]

If the protective element size is small, the current tolerance that can be discharged is small, and the inter-terminal

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resistance (on-resistance) when on is also large. Since the reference potential line is typically the primary discharge path for the ESD current, the reference potential line wiring resistance 23 and the reference potential line wiring resistance 24 are lower than the corresponding power supply line wiring resistance 21 and power supply line wiring resistance 22, respectively. Therefore, the resistance of the discharge path through the signal line 56 is greater than that of the discharge path through the reference potential line. The discharge path of the ESD is only these two paths and the current is diverted according to the combined resistance of each discharge path. By estimate, if the size of the ESD protective element 9 and the ESD protective element 10 were to be one-hundredth of the size of the ESD protective element 7 and the ESD protective element 8, the discharge resistance would be 100 times different. Thus, the discharge current via the signal line 56 is 100 times greater than the discharge current via the reference potential line. In this way, the reference potential line is usually the primary discharge path for the ESD current, so it is acceptable for the ESD protective element on the other discharge path to be small in size. This makes it possible to minimize the increase in circuit size.

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[0053]

FIG. 2 is a block diagram illustrating another example configuration of a semiconductor integrated circuit according to an embodiment of the present invention.

[0054]

In FIG. 2, for the circuit shown in FIG. 1, an ESD protective element 11 is connected between the signal line 56 and the reference potential line 19 on the circuit 1 side, and an ESD protective element 12 is connected between the signal line 56 and the reference potential line 20 on the circuit 2 side. It is necessary to use an ESD protective element 11 and an ESD protective element 12 that have the ability to discharge ESD bi-directionally.

[0055]

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The ESD protective element 11 and the ESD protective element 12 are effective in protecting the signal boundary portions 15 and 16 when an ESD voltage is applied between the reference potential pad 5 and the power supply pad 4 and when an ESD voltage is applied between the power supply pad 3 and the reference potential pad 6. This is also effective against Charged Device Model (CDM) surge voltages. This is because CDM surge voltages cause ESD current to flow through all the ESD protection elements of the chip being tested.

[0056]

FIG. 3 is a block diagram illustrating a specific example of the semiconductor integrated circuit of FIG. 1.

[0057]

Between the power supply pad 3 and the reference potential pad 5, a gate-grounded NMOS (ggNMOS) transistor 31 is connected as an ESD protective element. In addition, ggNMOS transistor 32 is connected between power supply pad 4 and reference potential pad 6 as an ESD protective element. The ggNMOS transistors are gates, sources, and bodies connected to one another in the NMOS transistors, which exhibit snapback characteristics when a positive voltage is applied to the drain, and forward characteristics of the PN junction diode when a negative voltage is applied to the drain.

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[0058]

Between the power supply line 17 and the signal line 56, a bi-directional diode chain 33 is connected as an ESD protective element, with a diode row connected in series of three diodes connected in anti-parallel to each other. Also, between the signal line 56 and the power supply line 18, a bi-directional diode chain 34 is connected as an ESD protective element, with a diode row connected in series of three diodes in anti-parallel to each other. Here, the number of steps of the bi-directional diode chain 33 and the bi-directional diode chain 34 (in the present example, three steps) is designed in consideration of the operating voltage and insulation membrane breakage voltage of the elements used in the circuit 1 and circuit 2 to be protected, and the trigger voltage and clamp voltage of the ESD protective elements connected between the power supply pad and the reference potential pad.

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[0059]

In addition, inverter 29 is connected as a signal boundary between power supply line 17 and reference potential line 19. Inverter 29 includes a pull-up PMOS transistor 25 and a pull-down NMOS transistor 27. The gates of the pull-up PMOS transistor 25 and the pull-down NMOS transistor 27 are connected to the internal circuit signal terminal 46, and the drains of both transistors are connected to the signal line 56. The source of the pull-up PMOS transistor 25 is connected to the power supply line 17 and the source of the pull-down NMOS transistor 27 is connected to the reference potential line 19.

[0060]

Inverter 30 is connected as a signal boundary portion between internal circuit power supply line 18 and reference potential line 20. The inverter 30 includes a pull-up PMOS transistor 26 and a pull-down NMOS transistor 28. The gate of the pull-up PMOS transistor 26 and the pull-down NMOS transistor 28 are connected to the signal line 56, and the drain of both transistors is connected to the internal circuit signal terminal 47. The source of the pull-up PMOS transistor 26 is connected to the power supply line 18 and the source of the pull-down NMOS transistor 28 is connected to the reference potential line 20.

[0061]

Also, unlike FIG. 1, in FIG. 3, the respective reference potential lines are separated between circuit 1 and circuit 2 to avoid noise between the reference potential lines and are connected to the third reference potential line 41 via a bidirectional diode pair 37 and a bidirectional diode pair 38. This third reference potential line 41 is used as a discharge path. A third reference potential line 41 is connected to the reference potential pad 39 and the reference potential pad 40. In this way, if reference potential line 41 is the discharge path for ESD, the ESD withstand capacity is lower due to the voltage drop due to forward characteristics of bidirectional diode pair 137 and bidirectional diode pair 38.

[0062]

Here, if circuit 1 and circuit 2 are both configured with thin film elements, and the like, when applying the predetermined ESD standard, the reference potential line wiring resistance 23 and reference potential line wiring resistance 24 are required to be as close as possible to 0 Ω in the above example circuit implemented before the present invention, and the reference potential line wiring resistance 23 and reference potential line wiring resistance 24 have a low design margin. However, according to the present embodiment, the clamp voltage value between the power supply pad 3 and the power supply pad 4 can be higher than before, thus easing the requirement for the reference potential line wiring resistance 23 and the reference potential line wiring resistance 24 and increasing the design margin.

[0063]

FIG. 4 is a circuit for performing a circuit simulation to confirm the effect of the present embodiment. This circuit is a specific example of the circuit shown in FIG. 2.

[0064]

In the circuit of FIG. 4, diode trigger thyristor (DTSCR) 57a and diode trigger thyristor 57b are used as the ESD protective element 7 and ESD protective element 8 in FIG. 2. In addition, as in FIG. 3, the inverter 29 and the inverter 30 are used as the signal boundary portion 15 and signal boundary portion 16 in FIG. 2. In addition, as ESD protective elements 9 to 12 in FIG. 2, bidirectional diode chains 33-36 are used in which diode rows connected in series with diodes are connected in opposite directions in parallel to each other. However, the type of ESD protective element is not important, and similar effects can be expected for other protective elements.

[0065]

Below, a case where a surge voltage is applied using the human body model (HBM) is simulated using the circuit of FIG. 4.

[0066]

ESD voltage was applied between the power supply pad 3 and the power supply pad 4 under the conditions where the ESD resistance is strictest as described above (PMOS transistor 25 in inverter 29 is turned on). Since the internal circuit 13 and the internal circuit 14 are not particularly important in the simulation, the power supply terminal 42 in the internal circuit 13 and the signal terminal 47, power supply terminal 43 and reference potential terminal 45 in the internal circuit 14 were all open. The internal circuit reference potential terminal 44 and the signal terminal 46 in the internal circuit 14 were shorted (not shown) to operate the inverter 29 at a high level. As discussed above, this state is the state in which the ESD resistance is lowest.

[0067]

FIG. 5 is a graph showing the results of circuit simulation using the circuit of FIG. 4, assuming a HBM surge of 5000 V as the ESD voltage.

[0068]

The horizontal axis is time and the vertical axis is voltage.

[0069]

The voltage between the power supply pad 3 and the power supply pad 4 when applying the ESD voltage is slightly above 6 V around 30 ns, whereas the voltage between the extremity voltage of the ESD protective element 33, i.e. the power supply line 17 and the signal line 56, and the extremity voltage between the ESD protective element 10, i.e. the signal line 56 and the power supply line 18, are 3.0 V or less, which is approximately half the voltage between power supply pad 3 and power supply pad 4. Note that in the graph of FIG. 5, the curve indicating the voltage between the power supply line 17 and the signal line 56 and the curve indicating the voltage between the signal line 56 and the power supply line 18 overlap.

[0070]

In addition, the voltage between the power supply terminal 42 and the reference potential terminal 44 in the internal circuit 13 is 3.6V, and the voltage between the power supply terminal 43 and the reference potential terminal 45 in the internal circuit 14 is about 2.4V.

[0071]

In the semiconductor integrated circuit configuration implemented by the present inventor prior to the present invention (for example, the configuration without bidirectional diode chains 33-36 in FIG. 4), if the internal circuit breakage voltage is set to 4 V, the voltage between the power supply pad 3 and the power supply pad 4 (near 6 V) will directly apply to the inverter 30 in the circuit 2, for example, and breakdown cannot be avoided. However, according to the present embodiment, the voltages at the internal circuit 13, the internal circuit 14, the signal boundary portion 29 and the signal boundary portion 30 can all be suppressed to 4 V or less, and breakdown can be avoided.

[0072]

The effect of the circuit in FIG. 4 has been described above using the example of an ESD voltage applied under the HBM. However, a similar effect can also be expected when an ESD voltage is applied based on the above-mentioned Charged Device Model (CDM).

[0073]

CDM surge voltages are shorter than other test standards, HBM and Machine Model (MM), with a pulse width of around 1 ns, but surge currents are higher and can reach from a few amps to as high as 20 A. Because of its short pulse characteristics, CDM has the characteristic that ESD protective elements require fast response characteristics. In addition, under HBM and MM, there is a charged body outside the device, and surge voltage is applied from there, but in contrast CDM has the feature that the device itself is charged and becomes the source of the surge voltage. ESD protective elements (e.g., ESD protective elements 7 and 8 in FIG. 1) provided in an integrated circuit previously operated connected to a power supply terminal, reference potential terminal, signal terminal, etc. connected to the exterior of the integrated circuit to block the application of ESD voltage from the exterior, but sufficient ESD protection could not necessarily be realized in CDM, where voltage is generated from the interior of the device. In contrast, according to the present embodiment, in addition to the path through the ESD protective element between the power supply terminal and the reference potential terminal within the integrated circuit, an additional discharge path has been provided, allowing effective protection against CDM.

[0074]

FIG. 6 is a schematic diagram of an integrated circuit chip 74 including the semiconductor integrated circuit of FIG. 1.

[0075]

The integrated circuit chip consists of three major circuits: circuit 1, circuit 2 and circuit 67.

[0076]

The power supplies of each circuit 1, 2, 67 are separated, and rectangular power supply pad 3, power supply pad 4, and power supply pad 58 are disposed near each circuit 1, 2, 67 at the periphery of the chip.

[0077]

Power supply lines and reference potential lines are usually called power supply rings because they are ring-shaped. The power supply ring is divided into three parts corresponding to the three power supplies. The power supply line is divided into power supply line 17, power supply line 18, and power supply line 59, respectively. The reference potential line is divided into reference potential line 19, reference potential line 20 and reference potential line 60 and is positioned outside the power supply line parallel to the power supply lines 17, 18, 59.

[0078]

Reference potential pads are not shown to simplify the drawing. In addition, ESD protective elements (e.g., ESD protective elements 7, 8 in FIG. 1) connected between the power supply pad and the reference potential pad are usually located on the underside of the power supply ring (in a direction perpendicular to the paper surface), but the illustration has been omitted to simplify the drawing.

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[0079]

In FIG. 6, the signal boundary portion 15 (1) in circuit 1 is connected at signal boundary portion 16 (1) and signal line 56 (1) in circuit 2. The signal line 56 (1) is connected to the power supply line 17 via the ESD protective element 9 (1) and to the power supply line 18 via the ESD protective element 10 (1), which provides protection from ESD at the signal boundary.

[0080]

The signal boundary portion 15 (2) in circuit 2 is connected at signal boundary portion 16 (2) and signal line 56 (2) in circuit 67. The signal line 56 (2) is connected to the power supply line 18 via the ESD protective element 9 (2) and to the power supply line 59 via the ESD protective element 10 (2), which provides protection from ESD at the signal boundary.

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[0081]

Circuit 67 is connected at two locations to circuit 1.

[0082]

On the other hand, the signal boundary portion 15 (3) in circuit 67 and the signal boundary portion 16 (3) in circuit 1 are connected by signal line 56 (3). The signal line 56 (3) is connected to the power supply line 59 via the ESD protective element 9 (3) and is connected to the power supply line 17 via the ESD protective element 10 (3).

[0083]

On the other hand, the signal boundary portion 15 (4) in circuit 67 and the signal boundary portion 16 (4) in circuit 1 are connected by signal line 56 (4). The signal line 56 (4) is connected to the power supply line 59 via the ESD protective element 9 (4) and to the power supply line 17 via the ESD protective element 10 (4).

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[0084]

Thus, in the chip shown in FIG. 6, ESD protective elements 9 (1) to 9 (4), 10 (1) to 10 (4), which are one of the major features of the present invention, are provided in the chip interior (previous ESD protective elements (not shown in FIG. 6) are provided in the underside of the power supply ring near the periphery of the chip as described above). Normally, it is difficult to use a large ESD protective element inside the chip, but in the present embodiment, the size of the ESD protective element may be small, as described above, so it is possible to greatly improve the ESD resistance while keeping the chip size as small as possible.

[0085]

As described above, in accordance with the present embodiment, a significant improvement in ESD resistance can be achieved by providing ESD protective elements that can be energized bi-directionally between one power supply line and the signal line and between the other power supply line and the signal line, respectively, between circuits in which the power supply lines are separated from each other and have signal propagation paths (signal lines).

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[0086]

In addition, according to the present embodiment, the size of the newly installed ESD protective element may be small, so there is little increase in the chip size and the total number of wiring, and thus increase in the unit price of the chip can be prevented as much as possible.

[Brief Description of the Drawings]

[0087]

[FIG. 1] A block diagram showing the configuration of a semiconductor integrated circuit according to an embodiment of the present invention.

[FIG. 2] A block diagram showing other configurations of semiconductor integrated circuits according to an embodiment of the invention.

[FIG. 3] A block diagram showing a specific example of the semiconductor integrated circuit of FIG. 1.

[FIG. 4] A block diagram showing the configuration of a circuit for performing a simulation to confirm the effect of the present embodiment.

[FIG. 5] A graph showing the results of simulation using the circuit in 4.

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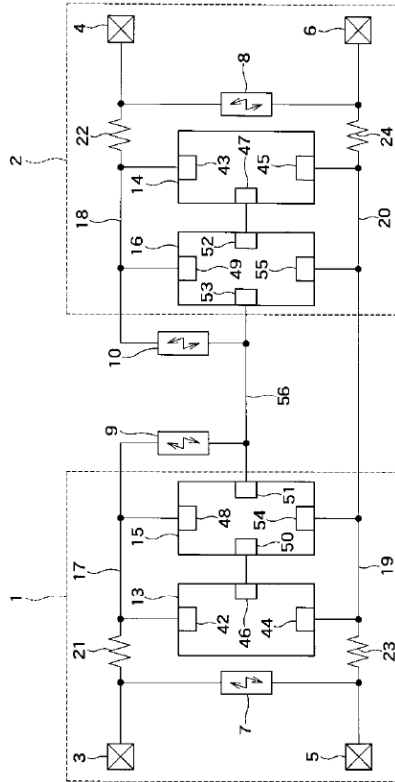
[FIG. 6] A schematic diagram of an integrated circuit chip including the semiconductor integrated circuit of FIG. 1.

[Explanation of References]

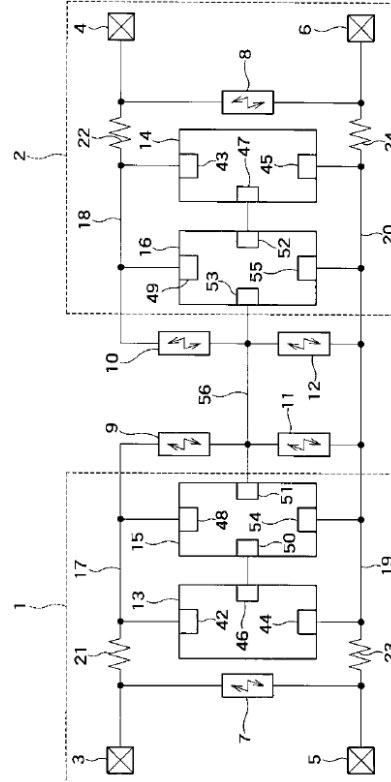
[0088]

1, 2, 67	Circuits	
3, 4, 58	Power supply pads	
5, 6, 39, 40	Reference potential pads	
7 to 12	ESD protective elements	
13, 14	Internal circuits	
15, 16	Signal boundaries	
17, 18, 59	Power supply lines	20
19, 20, 41, 60	Reference potential lines	
21, 22	Power line wiring resistance	
23, 24	Reference potential line wiring resistance	
25, 26	Pull-up PMOSFETs	
27, 28	Pull-down NMOSFETs	
29, 30	Inverters	
31, 32	ggNMOS transistors	
33 to 36	Bidirectional diode chains	
37, 38	Bidirectional diode pair	
42, 43	Internal circuit power supply terminals	30
44, 45	Internal circuit reference potential terminals	
46, 47	Internal circuit signal terminals	
48, 49	Signal boundary power supply terminals	
50 to 53	Signal boundary signal terminals	
54, 55	Signal boundary reference potential terminals	
56	Signal lines	
57	Diode triggered thyristor	
74	Integrated circuit chips	

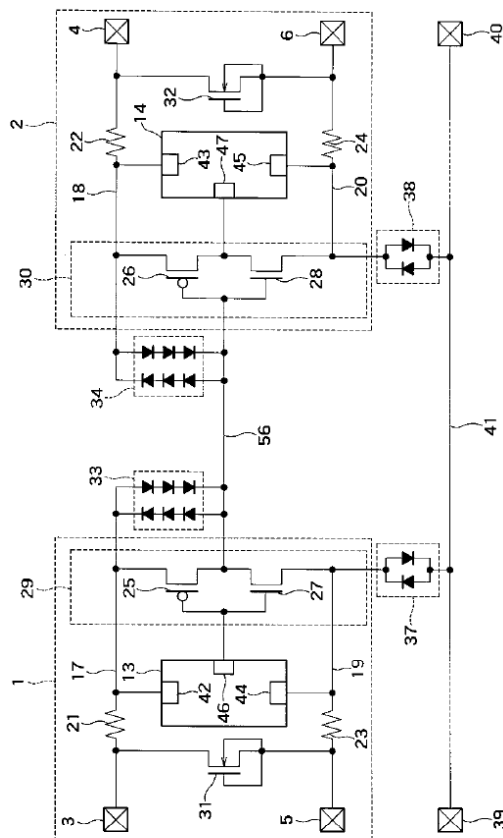
[FIG. 1]



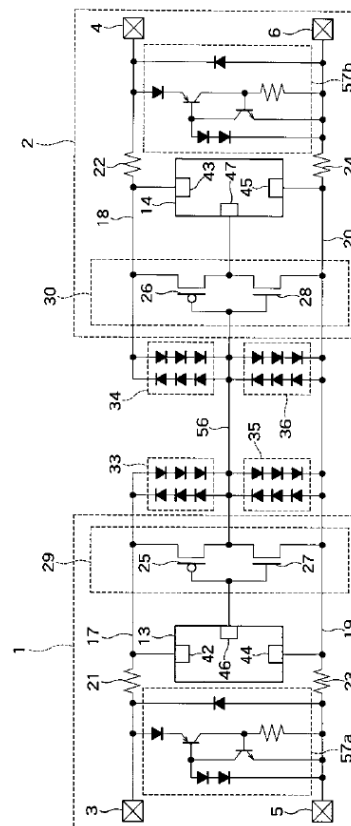
[FIG. 2]



[FIG. 3]



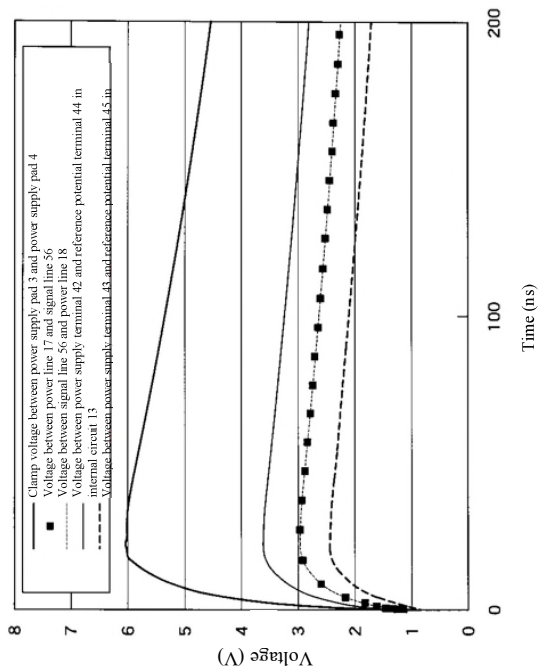
[FIG. 4]



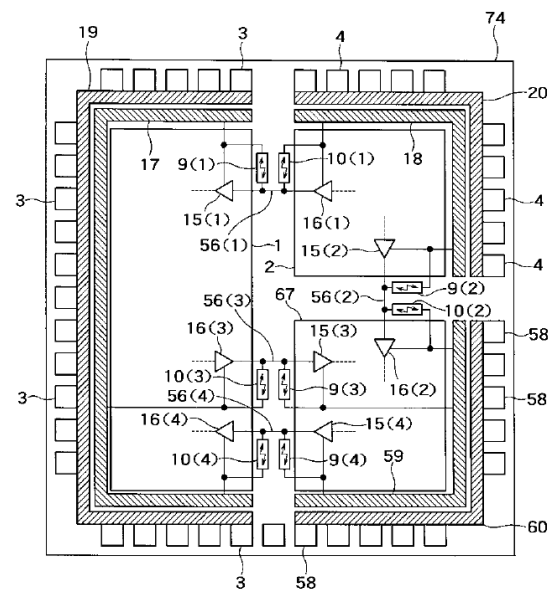
(15)

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[FIG. 5]



[FIG. 6]



Continued from Front Page

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F terms (for reference) 5F038 BH02 BH05 BH06 BH07 BH13 EZ20

October 17, 2024

Certification

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That I possess advanced knowledge of the Japanese and English languages.

My qualifications include the following:

- I am a native speaker of both Japanese and English (born in Japan).
- I have been a professional linguist since 1988 and a QM for TransPerfect since 2003 (internal and external).
- I have completed fellowship/cultural exchange studies at Disney College.
- I have a Linguistics-equivalent degree from a branch of the NHK Broadcasting Culture Research Institute, and by extension, bilingual broadcasting experience.

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