

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: March 12, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00118
Patent 10,879,164

DECLARATION OF DR. SUNIL KHATRI

1. I have been retained on behalf of YMTC (“YMTC”), and its counsel, Latham & Watkins, LLP, to provide expert opinions relating to U.S. Patent 10,879,164 (“Asserted Patent”) in connection with Micron’s Petition for *inter partes* review. I am personally knowledgeable about the matters stated herein and am competent to make this declaration.

2. I am being compensated for my time at my standard hourly rate of \$800 per hour.

3. This declaration, including the exhibits hereto and cited materials, identifies my opinions to date, although I may provide further testimony and opinions if asked to testify in court or at a deposition. I also reserve the right to supplement or amend my opinions, as well as the bases for those opinions, if I receive additional relevant information or to respond to opinions offered by other experts in this case. I may rely on demonstrative exhibits, including pictures, figures, and drawings that appear in this declaration and the referenced exhibits and materials.

I. BACKGROUND AND QUALIFICATIONS

4. I have over thirty-five years of experience with electronics, electrical engineering, and computer engineering. A copy of my latest curriculum vitae (CV) is attached hereto as Appendix A and provides further details regarding my background and qualifications.

5. During my career, I have acquired extensive knowledge and experience with VLSI circuits, computer architecture, testing, computer-aided design (CAD) algorithms and algorithm acceleration, logic synthesis, semiconductor memory, redundancy, synchronous and asynchronous circuits, and related software and hardware topics. Most relevant to the Asserted Patent my technical expertise includes extensive work with semiconductor integrated circuits (ICs), including the design and layout of input/output (IO) drivers and their electrostatic discharge (ESD) circuits. This work was performed for a commercial microprocessor IC, as well as 3 ICs whose fabrication I led at Texas A&M University. I have one US patent in the area of IO driver design. My work on semiconductor memory devices has included work on 3D integration and novel ring-based memory architectures, power and speed tradeoffs using selective body bias, architectures and circuit approaches for processing-in-memory, radiation hardening analysis for memories, the use of flash transistors for designing logic circuits (such as ternary Content-addressable Memories (CAMs), Field Programmable Gate Arrays (FPGAs), and traditional binary-valued as well as ternary-valued digital logic, secure logic circuits, analog circuits like Finite Impulse Response (FIR) filters, Discrete Fourier Transform (DFT) circuits, and in-memory mixed-signal computing architectures like Convolutional Neural Networks (CNNs)), large language models (LLMs) and

clocking and source-synchronous design. I recently was awarded a research grant by the Air Force Research Laboratory (AFRL) in Rome, NY, to conduct research in secure digital circuits using flash-based digital design approaches.

6. Another recent research grant from the National Science Foundation (NSF) will fund research on the use of flash transistors for general purpose mixed-signal arithmetic. Additionally, I have led-authored a book chapter on the use of flash transistors in novel Very Large Scale Integrated (VLSI) design applications. My MS thesis involved designing a memory interface for a multi-threaded Reduced Instruction Set Computing (RISC) microprocessor.

7. The following describes some of my relevant experience. I earned my Bachelor of Science in Electrical Engineering in 1987 from the Indian Institute of Technology, Kanpur, India. After graduating with my B.S. degree, I was a candidate for a Master of Science degree in Electrical and Computer Engineering at the University of Texas from 1987–89. At the University of Texas, I held the Microelectronics and Computer Development (MCD) Fellowship from 1987–89. I also conducted my M.S. research and wrote my thesis on the design of the METRIC memory interface and memory system. METRIC was one of the first super-scalar processors that was developed in the world. I earned an M.S. degree in 1989 from the University of Texas, Austin.

8. After leaving the University of Texas, I worked at Motorola Inc. from 1989–93 as a design engineer for the MC88110 and PowerPC 603 reduced instruction set computing (RISC) microprocessor teams. My duties included the design of digital and analog circuitry, test logic and circuits, JTAG boundary scan design, input/output driver design (including ESD circuits in these drivers), and clock phase-locked loop (PLL) logic. During my time at Motorola, I was independently responsible for the design of the factory test controller of the MC88110 microprocessor. I performed all attendant tasks in a “vertical” VLSI design methodology, which included high-level modeling, circuit and layout design and verification, as well as global and detailed routing. I also helped in the design of the Translation Lookaside Buffer (TLB) unit, which included a static random-access memory (SRAM) block.

9. In 1999, I earned a Doctor of Philosophy degree in Electrical Engineering and Computer Sciences from the University of California, Berkeley. While at Berkeley, I held the California Microelectronics (MICRO) Fellowship in 1993.

10. I joined the faculty at the University of Colorado, Boulder, in 2000 as an Assistant Professor of Electrical and Computer Engineering. At the University of Colorado my research focused on VLSI logic design automation, VLSI layout design automation, and VLSI design methodologies to address

Deep Submicron (DSM) issues such as crosstalk and power.

11. I joined the faculty at Texas A&M University in 2004 as an Assistant Professor in Electrical and Computer Engineering. In 2010 I was promoted to Associate Professor in Electrical and Computer Engineering. In 2015, I was promoted to full Professor in Electrical and Computer Engineering. My research focuses on three primary areas: the first is computer systems, including computer architecture from the circuits up, and algorithm acceleration using GPUs, FPGAs and custom ICs. The second is logic and its applications, while the third area consists of interdisciplinary extensions of the first two. Some specific recent research topics include circuit design using floating gate (flash) devices, wireless power delivery and battery-less electronic systems, machine learning architectures, secure computing approached from both a hardware and software perspective, a formal framework for designing and verifying cryptographic hash functions, and extreme high-speed serial interfaces for Artificial Intelligence / Machine Learning (AI/ML) systems such as those used in Large Language Models (LLMs) like ChatGPT. One of my new focus areas is intelligent and secure computing viewed from the hardware (circuit) as well as the software levels. I have conducted research on tamper-proof memory techniques, as well as multi-row read architectures for SRAM, DRAM and flash memory arrays.

12. At Texas A&M I teach classes that cover circuit design and memories extensively, featuring thorough discussion of sense amplifiers, row and column decoders, and different types of memory circuits. For example, in Electrical and Computer Engineering (ECEN) 752 “Advances in VLSI Circuit Design,” a graduate level course, I cover all aspects of VLSI design, including memory design for various types of memories as well as IO drivers and ESD. In this course, (and also in ECEN 449/749 “Microprocessor System Design,”), I cover memories, including flash memories, the design of flash memory cells, the organization of memories into multiple banks, and the division of data across multiple banks of memory, as well as other design techniques that can be used to optimize and manage memories. The ECEN 449/749 course is attended by both undergraduate (ECEN 449) and graduate (ECEN 749) students. In ECEN 454 “Digital Circuit Design,” a senior undergraduate course, I cover circuit design techniques for memory in detail. The Ph.D. thesis dissertation topic for 3 of my current Ph.D. students covers the use of flash memory transistors for analog and digital applications. The Ph.D. thesis of one of my recent doctoral students dealt with the use of flash transistors to design logic circuits. The research of a recent M.S. student entailed a new ring-based source synchronous architecture for 3D DRAM technologies, which has been published at a conference and in a journal and is being submitted for dissemination as a

research monograph. In the past, I have conducted research into new topologies for efficient memory redundancy as part of a course project for my graduate course.

13. Since 2000, I have earned at least 24 research contracts from funders including Intel, the National Science Foundation, the National Security Agency, Altera Corporation, the National Center for Atmospheric Research, National Semiconductor Corporation, and several private sources. The total amount for these research grants is at least \$17.53 million, of which my portion is at least \$2.85 million.

14. I have a total of over 289 peer-reviewed publications. Among these papers, five received a best paper award, while seven others received best paper nominations (including one journal best paper nomination). An additional six journal papers and three conference paper are currently undergoing peer review. I have co-authored nine research monographs, one edited research monograph, and four book chapters. Additionally, I have seven awarded U.S. Patents (two of which were filed during my tenure at Texas A&M), two filed provisional U.S. Patents, and another U.S. Patent which is currently under review and was also submitted during my tenure at Texas A&M. I have co-authored one invited journal paper and 13 invited conference or workshop papers (including one from Design Automation Conference (DAC) and one from Allerton). Moreover, I

was invited to serve as a panelist at a conference seven times and have presented four conference tutorials. I received the “Outstanding Professor Award” in the ECE Department at Texas A&M University in 2007 and also in 2020. In 2009 and in 2019, I received a university-level and a college-level teaching award respectively, at Texas A&M. My H-index is 36 (per Google Scholar).

15. Since 2003, I have published numerous research monographs, journal papers, and conference papers on flash transistors and memory systems, as well as IO drivers, as detailed in my CV attached in Appendix A. A few papers on relevant subject areas authored or co-authored by me include:

- *"Flash - A "Forgotten" Technology in VLSI Design"*. Khatri, Vrudhula, Abusultan, Bharathi, Chu, Lee, Scott, Singh, Wagle. Appears "Frontiers of Quality Electronic Design (QED)". Springer publishers, Sept 2022. Pages 67-136. Ali Iranmanesh, Ed. ISBN: 978-3-031-16344-9;
- *"Flash – An Overlooked Technology in VLSI Design"*, Khatri, Vrudhula. Monday Tutorial to be presented at the ACM/CEDA Design Automation Conference (DAC), San Francisco, CA, June 2024;
- *"A Mixed-Signal Quantized Neural Network Accelerator Using Flash Transistors"*, Scott, Lee, Khatri, Vrudhula. IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 71, no. 3, pp. 1025-1038,

March 2024;

- *"An ASIC Accelerator for QNN With Variable Precision and Tunable Energy-Efficiency"*, Wagle, Singh, Khatri Vrudhula. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Jan 2024;
- *"A Digital Low Dropout (LDO) Voltage Regulator Using Pseudoflash Transistors"*, Lee, Khatri. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 31, no. 12, pp. 1960-1969, Dec. 2023;
- *"A Novel ASIC Design Flow using Weight-tunable Binary Neurons as Standard Cells"*, Wagle, Singh, Khatri, Vrudhula. IEEE Transactions on Circuits and Systems I (Regular Papers), 69(7): 2968-2981 (Sept 2022);
- *"CIDAN-XE: Computing in DRAM with Artificial Neurons"*, Singh, Wagle, Khatri, Vrudhula. Frontiers in Electronics, section Integrated Circuits and VLSI. vol. 3, Feb 2022;
- *"An Extremely Low-Voltage Floating Gate Artificial Neuron"*, Scott, Khatri. 2023 IEEE International Conference on Circuits and Systems (ISCAS), May 21-25, 2023. Monterey, CA;
- *"A Novel Pseudo-Flash Based Digital Low Dropout (LDO) Voltage Regulator"*, Lee, Khatri, Vrudhula. 2023 International Symposium on

Quality Electronic Design (ISQED), April 5-7 2023. San Francisco, CA;

- *"A Flash-based Digital to Analog Converter for Low Power Applications"*, Scott, Khatri. IEEE 40th International Conference on Computer Design (ICCD), October 2022. Lake Tahoe, CA. pp 1-8;
- *"A Flash-based Current-mode IC to Realize Quantized Neural Networks"*, Scott, Lee, Khatri, Vrudhula. IEEE Design Automation and Test in Europe Conference, Mar 2022, Antwerp, Belgium. pp 1029-1034;
- *"CIDAN: Computing in DRAM with Artificial Neurons"*, Singh, Wagle, Vrudhula, Khatri. 39th IEEE International Conference on Computer Design (ICCD) 2021, pp 349-356, Oct 2021, virtual conference;
- *"A Statistical Methodology for Post-Fabrication Weight Tuning in a Binary Perceptron"*, Azari, Wagle, Khatri, Vrudhula. IEEE 21st International Symposium on Quality Electronic Design (ISQED) 2020. Mar 25-26, 2020, Santa Clara, CA. pp 141-148;
- *"Threshold Logic in a Flash"*, Wagle, Singh, Yang, Khatri, Vrudhula. 37th IEEE International Conference on Computer Design (ICCD), 2019. Abu Dhabi, UAE, pp 550-558. Nov 17-20, 2019;
- Fast, Ring-based Design of 3D Stacked DRAM, IEEE Transactions on

Very Large Scale Integrated Circuits (TVLSI), IEEE Transactions on Very Large Scale Integration (VLSI) Systems. Vol 27 number 8, Aug 2019. pp 1731-1741.;

- Fast, Ring-Based Design of 3D Stacked DRAM, IEEE International Conference on Computer Design 2017: pp 665-672;
- Selective Forward Body Bias for High Speed and Low Power SRAMs, Journal of Low Power Electronics, Vol. 5, No. 2, Aug. 2009, pp. 185-95;
- Low Power and High Performance SRAM Design using Bank-based Selective Forward Body Bias, IEEE/ACM Great Lakes Symposium on VLSI, May 10-12, 2009, Boston, MA, pp. 441-44;
- Modeling Dynamic Stability of SRAMs in the Presence of Single Event Upsets (SEUs), IEEE International Symposium on Circuits and Systems, May 18-21, 2008, Seattle, WA, pp. 1788-91;
- “Design of a Flash-based Circuit for Multi-valued Logic”, Proceedings of the Great Lakes Symposium on VLSI (GLSVLSI) 2017, pp 41-46, May 10-12, 2017. Banff, Canada.
- "SAT-Based Optimization for Flash-Based Digital Designs", IEEE/ACM Design Automation Conference (DAC), Jun 18-22 2017, Austin, TX.

- "A Flash-based Digital Circuit Design Flow", IEEE/ACM International Conference on Computer-Aided Design (ICCAD) 2016, Austin, TX, Nov 2016.
- "Implementing low power digital circuits using flash devices", 2016 IEEE 34th International Conference on Computer Design (ICCD), pp 109-116, Oct 3-5, 2016, Phoenix, AZ.
- "Exploring Flash Devices to Implement Digital Circuits", IEEE/ACM Design Automation Conference (DAC), June 2016, Austin, TX.
- FTCAM: An Area-efficient Flash-based Ternary CAM Design, IEEE Transactions on Computers, Vol. 65, No. 8, Aug. 2016, pp. 2652-58;
- An Area-efficient Ternary CAM Design Using Floating Gate Transistors, IEEE International Conference on Computer Design, Oct. 19-22, 2014, Seoul, S. Kor., pp. 55-60; and
- A Fast Ternary CAM Design for IP Networking Applications, International Conference on Computer Communications and Networks, October 22, 2003, Dallas, TX, pp. 434-39 (awarded best paper).
- U.S. Patent 05448182: "Driver Circuit with Self-adjusting Impedance Matching." Countryman, Khatri. Issued September 1995.

16. In addition to my work on the papers listed above, I have also served as an editor for IEEE Transactions on Computers, ACM Transactions on

Design Automation of Electronic Systems, and MDPI Journal of Electronics.

17. I have served as EDA Track Co-Chair for ICECS 2014, Panel Chair for TexasWISE 2014, Track Co-Chair (VLSI Systems, Applications and Computer Aided Design track) for ICECS 2013, Poster Session Chair for TexasWISE 2013, Advisory Committee for HotPI 2013, Panel Session Chair for SLiP 2013, Track Chair (Logic track) for ICCAD 2009-10, 2015-17, Track Chair (logic track) for DAC 2016-17, General Chair for IWLS 2009, Technical Program Chair for IWLS 2008, Track Co-Chair, Computer Aided Network Design (CANDE) Track, for ISCAS 2008-10, Track Co-Chair, Test and Methodologies Track, for ICCD 2007, Panel Chair for ITSW 2009, Publicity Co-Chair for GLS-VLSI 2009, and as a member of the TPC for several conferences.

II. SUMMARY OF MATERIALS REVIEWED AND CONSIDERED

18. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, while drawing on my experience in the field of semiconductor circuit design, I reviewed the Petition and all exhibits attached thereto, and all exhibits cited herein.

19. My opinions are additionally guided by my appreciation of how a person of ordinary skill in the art would have understood the claims of the '164

patent at the time of the invention, which I have been asked to assume is November 1, 2018.

III. UNDERSTANDING OF LEGAL STANDARDS

20. I am not an attorney, and in this Declaration, I do not opine on matters of law. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions. My understanding of these principles is set forth below.

21. I have been informed by Counsel that the validity analysis is a two-step process. First, the patent claims are construed to ascertain their proper scope. Second, the construed claims are compared to the identified prior art to determine if the claims are valid over the prior art.

22. I have been informed by Counsel that patent claims can be deemed invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. While such conclusions are often based on more than one piece of prior art, only one is required. It is not sufficient that a collection of prior art references merely recites the various elements of a challenged patent claim. Rather, as I have been informed by Counsel, the prior art must present the elements in a manner that is consistent with their arrangement or use in the challenged claims. I have been

informed by Counsel that obviousness cannot be based on the hindsight-driven combination of components selectively culled from the prior art.

23. I have been informed by Counsel that a person having ordinary skill in the art (i.e., a POSITA) is a hypothetical person who is presumed to have known the relevant art at the time the invention was made. I have been informed by Counsel that the condition “at the time the invention was made” is imposed to rule out impermissible hindsight. I also have been informed by Counsel that an expert is to analyze the prior art from the perspective of a person of ordinary skill in the art at the time the invention was made, and not simply to provide his/her own personal conclusions.

24. I also have been informed by Counsel that an obviousness determination includes several factual inquiries, including (1) determining the scope and content of the prior art; (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the pertinent art; and (4) taking into consideration any objective indicia of nonobviousness.

25. I have been informed by Counsel that obviousness must be determined as of the date of the invention (i.e., the effective filing date or priority date of the patent). In considering the reason or motivation to combine references, it is essential to avoid using hindsight. For example, the problem

examined when considering obviousness is the general problem that confronted the inventor before the invention was made, not the specific problem solved by the invention. Defining the problem in terms of its solution leads to improper hindsight in the selection of the prior art relevant to obviousness. Further, an overly narrow statement of the problem can represent a form of hindsight, because often the inventive contribution lies in defining the problem in a new revelatory way. Similarly, a conclusory assertion that a person of ordinary skill could combine the references, rather than a showing that they would have been motivated to do so, is an impermissible form of hindsight. Moreover, knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references to reach the particular claimed invention.

26. I have been informed by Counsel that a motivation to solve a problem (or issue) is not the same as a motivation to have combined references.

27. I have been informed by Counsel that the analysis of the motivation to combine should be explicit. Additionally, it must include articulated reasoning with rational underpinnings to support the conclusion of obviousness. Providing a full explanation of the motivation to combine the references and the reasonable expectation of success is a necessary component of the obviousness inquiry, as inventions in most, if not all, instances rely upon building blocks

long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. However, conclusory statements fail to adequately explain why a person of ordinary skill would have a motivation to combine the potential prior art references.

28. I have been informed by Counsel that common sense, common wisdom, and common knowledge may be used to support a motivation to combine, so long as the use of common sense in the analysis is explained with sufficient reasoning. But, common sense can only be used to supply a limitation missing from the prior art where the technology is unusually simple and straightforward.

29. I also have been informed by Counsel that evidence suggesting reasons to combine cannot be viewed apart from evidence suggesting reasons not to combine. In analyzing motivation, both advantages and disadvantages must be considered. Teaching away, for example, is a statement in the prior art that either (i) discourages one from following the path of the claimed invention, or (ii) encourages one to follow a path that diverges from the path of the claimed invention. The concept of teaching away bears directly on whether there was a reason to combine prior art.

IV. LEVEL OF ORDINARY SKILL IN THE ART

30. Dr. Foty defines a person of ordinary skill in the art (“POSITA”)

as a person having “a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience with the design, layout, and manufacture of integrated circuits containing ESD circuitry and buses. A Master’s or Ph.D. degree in a relevant field may substitute for some work experience and vice versa.” Ex. 1003 ¶ 32.

31. For the purposes of this declaration, I have not been asked to provide an opinion on the level of ordinary skill in the art, or to opine on Dr. Foty’s definition on this issue. In view of my educational background and work experience, I surpass Dr. Foty’s definition of a POSITA. Using Dr. Foty’s definition of a POSITA, the Petition does not show the challenged claims obvious. I reserve the right to opine as to an alternative level of a POSITA in other proceedings or if the Board institutes review in this proceeding.

V. THE ’164 PATENT

32. The ’164 Patent discloses “an integrated circuit electrostatic discharge bus structure and related method.” ’164 Patent 1:17-20. In the prior art, an integrated circuit electrostatic discharge or “ESD” structure comprises a “circuit area 10,” “I/O (input/output) pads 12,” and an “electrostatic discharge (ESD) bus 11” as shown in Figure 1. *Id.* 1:24-37. But it was “commonly [known] to place filler cells F1 and F2 at empty spaces between the I/O pads 12, and connect the filler cells F1 and F2 to an electrostatic discharge (ESD) bus

11.” *Id.* 1:30-37. The ESD bus is a “layout trace connected to a ground or a system voltage.” *Id.*

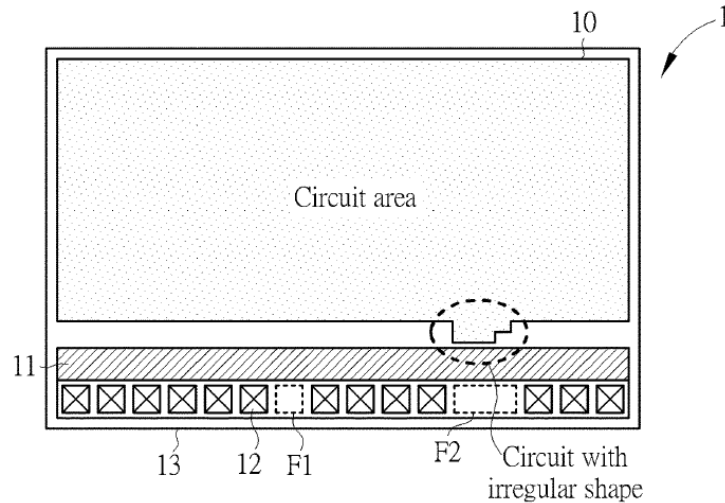


FIG. 1 PRIOR ART

33. A drawback of the prior art approach is that “filler cells F1 and F2 take a portion of the circuit area 10 to be wasteful to the integrated ESD bus structure 1.” *Id.* 1:38-43. Further, as shown in Figure 1, “when there are circuits with irregular shapes and different areas, the circuit area 10 must be increased in order to contain the circuits with irregular shapes and different areas, which increases production cost.” *Id.* 1:44-47. The ’164 Patent teaches two configurations for overcoming the drawbacks of the prior art.

34. As shown in Figure 2, the ’164 Patent teaches one configuration where a “plurality of pad groups G1, G2 and G3 is formed inside the chip edges 23, adjacent and connected to the plurality of ESD buses E1, E2, and E3.” ’164 Patent 2:61-63. A “common ESD bus 24 is formed outside the chip edges 23.”

Id. 2:63-65. Each of the “plurality of pad groups G1, G2 and G3 includes at least one pad 22” that is “connected to a ground or a system low voltage.” *Id.* 3:6-9. Bonding wires 25 connect “pads 22 of the pad groups G1, G2 and G3 to the common ESD bus.” *Id.* 3:17-22.

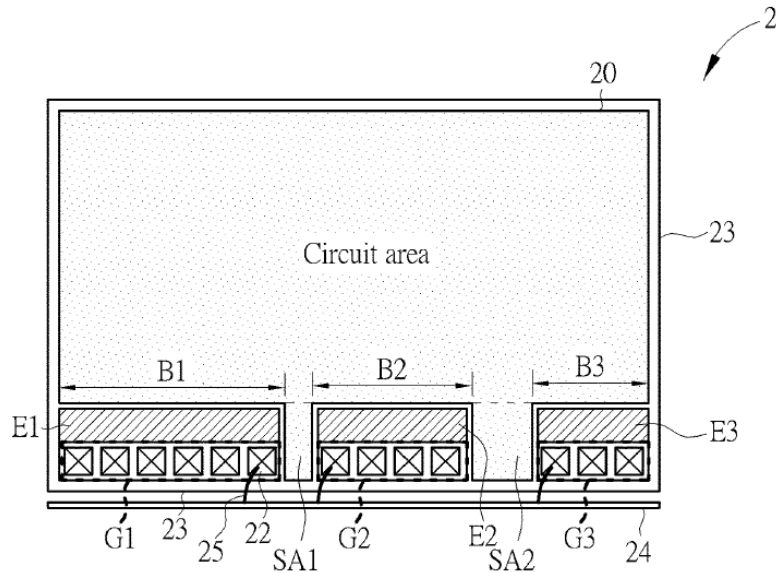


FIG. 2

35. As a result, “the discontinuous ESD buses E1, E2 and E3 may be connected together by connecting pads 22 of the pad groups G1, G2 and G3 to the common ESD bus 24 through bonding wires 25.” *Id.* 3:17-22. In this way, “spaces between the discontinuous ESD buses E1 and E2 (or, E2 and E3) may be configured with circuit elements to make full use of the integrated circuit ESD bus structure 2.” *Id.* 3:23-26. The ’164 Patent refers to those “spaces” as “saved areas SA1 and SA2.” *Id.* 3:29-32.

36. As shown in Fig. 3, an alternative embodiment also includes

“circuit area 30,” a “plurality of ESD buses E1, E2 and E3,” a “plurality of pad groups G1, G2 and G3,” and “a plurality of bonding wire 35.” *Id.* 3:36-41. Unlike the Fig. 2 embodiment where the “bonding wires 25” connect pads 22 to a “common ESD bus,” the “bonding wires 35” of the Fig. 3 embodiment connect “pads 32 of one group to another group.” *Id.* 3:64-65. This also results in the “saved areas” for adding additional circuitry.

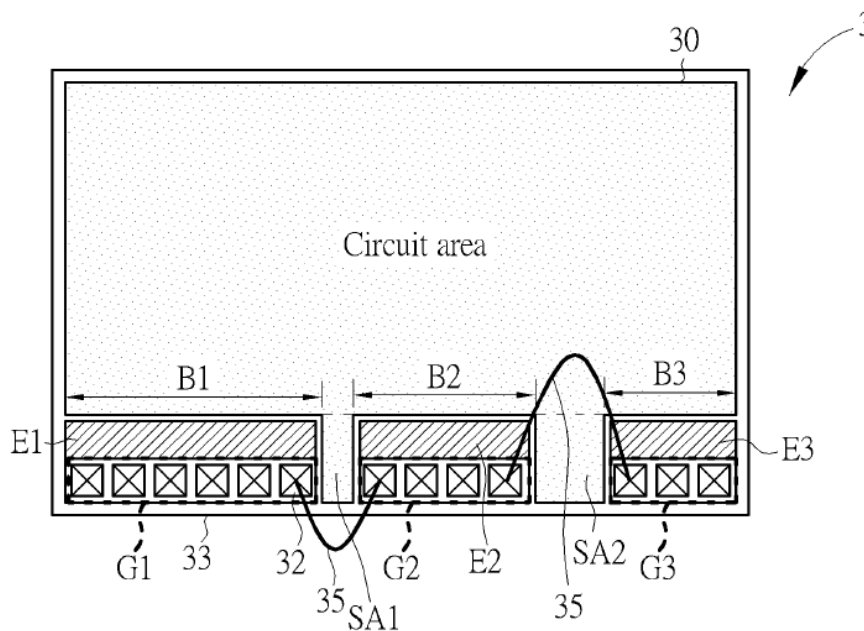


FIG. 3

I. CLAIM CONSTRUCTION

37. Dr. Foty asserts that the terms of the '164 patent's claims have their plain and ordinary meaning. Ex. 1003 ¶ 71. For purposes of this Preliminary Response, I agree because the Petition does not show any Ground has a reasonable likelihood of prevailing under any reasonable construction, including their plain meaning. I reserve the right to propose alternative constructions in

other proceedings or if the Board institutes review.

II. GROUND 1

- A. **Yoshinaga, Saint, and POSITA Knowledge Do Not Render Obvious “a plurality of bonding wires configured to connect one to another of the plurality of pad groups” (claims 6 and 7) or “connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires” (claims 12 and 14)**

38. Dr. Foty redraws Yoshinaga’s Figure 6 by changing Yoshinaga’s “power supply pad[s]” 3, 4, and 58 to become “reference potential pads” 5, 6, and “Circuit 67 GND” respectively, and drawing bonding wires between its newly added reference potential pads. Ex. 1003 ¶¶ 136-139, 144-153. I disagree that a POSITA would have been motivated to make these modifications.

39. Dr. Foty asserts that “the pads in Yoshinaga Figure 6 are largely fungible when it comes to their specific assigned connections – and their assigned locations among the available pads; for example, a POSITA would have understood that the pads labeled 3, 4, and 58 could just as readily be used for reference pads.” Ex. 1003 ¶ 137. Based on that, Dr. Foty asserts that “reference pads (e.g., pads 5, 6, etc.) are located as shown below near the orange saved spaces.” *Id.* ¶ 138. I disagree. Merely because Fig. 6 is “an illustrative rendering” as Dr. Foty asserts (Ex. 1003 ¶ 136) does not mean a POSITA would disregard that the pads deliberately labeled as “power supply pads” (3, 4, and 58) are not power supply pads as Dr. Foty suggests. Dr. Foty provides no reason why a POSITA would use pads 3, 4, and 58 specifically as “reference potential

pads” when Yoshinaga teaches that they are to be used as power supply pads. Power supply pads and reference potential pads are very different. Power supply pads supply power and reference potential pads serve as the “reference” or “ground” for the circuit. Dr. Foty does not provide any reason a POSITA would have been motivated to change Yoshinaga’s layout and replace its power supply pads with reference potential pads. In fact, Yoshinaga states that the “reference potential pads” are “not shown,” which a POSITA would understand means they are not located at any of the pads locations that *are* shown.

40. I also disagree that “pads ... are largely fungible.” The precise location of pads in an integrated circuit has a tremendous impact on inductive and capacitive parasitics, and several design performance metrics such as noise, power consumption and delay. Replacing the “power supply pad[s]” 3, 4, and 58 by “reference potential pads” 5, 6, and “Circuit 67 GND” is an exercise that could have a detrimental effect on design performance metrics. Furthermore, Dr. Foty does not discuss where the replaced power supply pads 3, 4 and 58 are moved to, a decision which would impact design metrics.

41. Dr. Foty suggests only that one reason for locating reference potential pads 5 and 6 “immediately next to the saved areas” as shown in his modified figure is to “preserve Yoshinaga’s saved area for other circuitry.” Ex. 1003 ¶ 137. I disagree. Preserving the saved area, however, does not require a

POSITA to place reference pads where the power supply pads of Yoshinaga are located. Specifically, it does not provide any motivation for a POSITA to take Yoshinaga's power supply pads 3, 4, and 58 and change them into reference potential pads as proposed, nor does it explain how such a significant change would impact the performance metrics of the design.

42. Based on my argument above, Dr. Foty's decision to replace the "power supply pad[s]" 3, 4, and 58 with "reference potential pads" 5, 6, and "Circuit 67 GND" appears to be guided by no more than hindsight, to meet the claim limitations of the '164 patent, rather than any actual reason a POSITA would have been motivated to make that modification, let alone with any reasonable expectation of success.

43. Dr. Foty also ignores that the Saint textbook he cites includes entire sections about how to properly place pads for "powers" and "grounds." Saint 143-147 ("Pin-Driven Planning"). Note, for purposes of this declaration, I cite the actual page numbers of Saint, on the upper right hand corner. Even for a simple change of placement of power and ground pins (shown in Figures 7-1 and 7-2, Saint states that both are "totally valid pin-out[s]", but each "directly affects how you floorplan your chip", since a "good choice of pin-out could reduce parasitics", and "pin-out drives the complexity of the .. blocks." Saint 144-145.

44. While Dr. Foty acknowledges that “[t]he choice of selecting which pads to assign for ground [and] power ... depend[s] on factors such as the size of the chip, whether the chip is pad-limited or core-limited, the number of I/O signals, and the number of available pads.” Ex. 1003 ¶ 137. This contradicts his statements just a few lines above, where he says that “the pads ... are largely fungible when it comes to their specific assigned connections”. Dr. Foty’s recognition that various considerations go into choosing appropriate pads for power and ground confirm that pads are not “fungible” and that a POSITA could simply change power supply pads into ground/reference pads. Dr. Foty does not address any of those considerations for pad selection while proposing to change Yoshinaga’s power supply pads into ground or reference pads. A POSITA would understand that you cannot just arbitrarily make this change, without other modifications to the layout and design, and extensive simulations to quantify the effect of this change on design performance metrics such as noise, power consumption and delay. As just one example, Dr. Foty does not explain where the power supply pads 3, 4 and 58 (which he replaces) would be relocated to after he replaces them with reference potential pads 5, 6 and “Circuit 67 GND”.

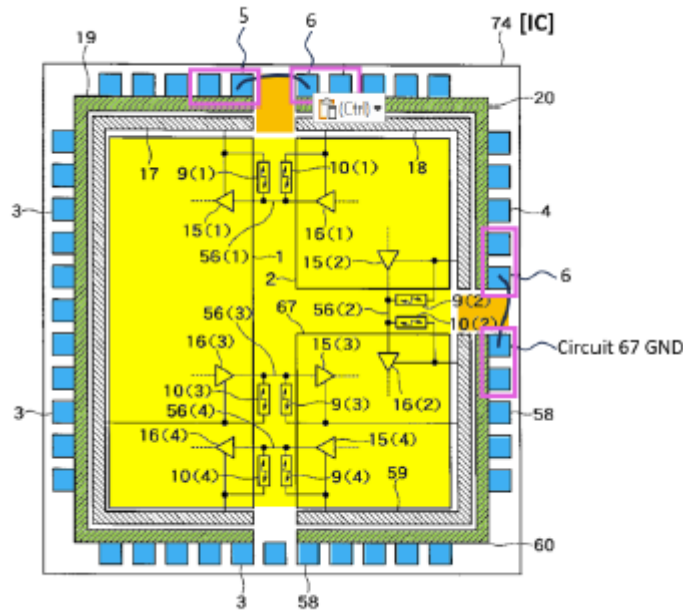
45. I also disagree with Dr. Foty’s proposed modification of using bonding wires to connect the reference potential pads as shown in his modified

figure (Ex. 1003, page 79) as well. According to Dr. Foty, “Yoshinaga is silent on the details of how the bond pads (in Figure 6) are used and connected.” Ex.1003 ¶ 103. Based on that, Dr. Foty asserts that “it would have been obvious to a POSITA to connect together the disparate ESD buses of Yoshinaga by using the POSITA’s knowledge as reflected in Miller, Beauchamp, and others – that is, by using a ‘jumper’ bond wire to connect a pad of one pad group to a pad of another pad group, across the space that intervenes between them.” Ex.1003 ¶ 153.

46. Dr. Foty overlooks that Yoshinaga expressly discloses that “[t]he reference potential lines *may be connected by bidirectional diodes* that are connected in parallel to one another in the opposite direction *to avoid noise*.” Yoshinaga [0005] (emphasis mine). A POSITA would know that using bidirectional diodes between reference potential pads would reduce the injection of noise from one circuit into the other, while providing ESD protection. A POSITA would also know that using “jumper” wires between the reference potential pads would negate the noise reduction feature of the bidirectional diodes, and also that “jumper” wires would cause the bidirectional diodes to never conduct and therefore never provide ESD protection. Moreover, because bond wires have inductance, using bond wires actually add noise, which is contrary to Yoshinaga’s teachings that bidirectional diodes should be used to

“avoid noise.” Dr. Foty does not explain why a POSITA would disregard Yoshinaga’s disclosure of connecting the reference potential lines “by directional diodes to avoid noise” and use bond wires to connect the reference potential pads instead. He does not identify any advantages with using bond wires over bidirectional diodes or any drawbacks with the use of bidirectional diodes that bond wires would solve. From an ESD protection viewpoint, connecting reference potential pads with bond wires would be redundant given Yoshinaga’s express disclosure of using of bidirectional diodes to connect reference potential lines.

47. While Dr. Foty cites references to show the use of bond wires was well-known, he ignores what they teach about the use of bond wires. For example, the Saint textbook he cites in this Ground would discourage POSITAs from using bond wires between pads 5 and 6 and 6 and circuit 67 GND as Petitioner proposes (shown below).



48. Saint teaches that bond wires should only be used where there is “minimal silicon overlap.” Saint 195. According to Saint, “the bond wire could sag or droop, causing a short in the circuit” and “[s]o, you have to keep the overlap of the bond wire over the unused silicon as short as possible.” *Id.* In view of Saint’s teachings, a POSITA would be discouraged from deliberately forming the bond wire to overlap entirely with “unused silicon” (the alleged “saved areas” shown in orange) as Dr. Foty proposes.

III. GROUND II

- A. **Ground 2: Yoshinaga, Saint, Haralabidis, and POSITA Knowledge Do Not Render Obvious “a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus” and “connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires”**

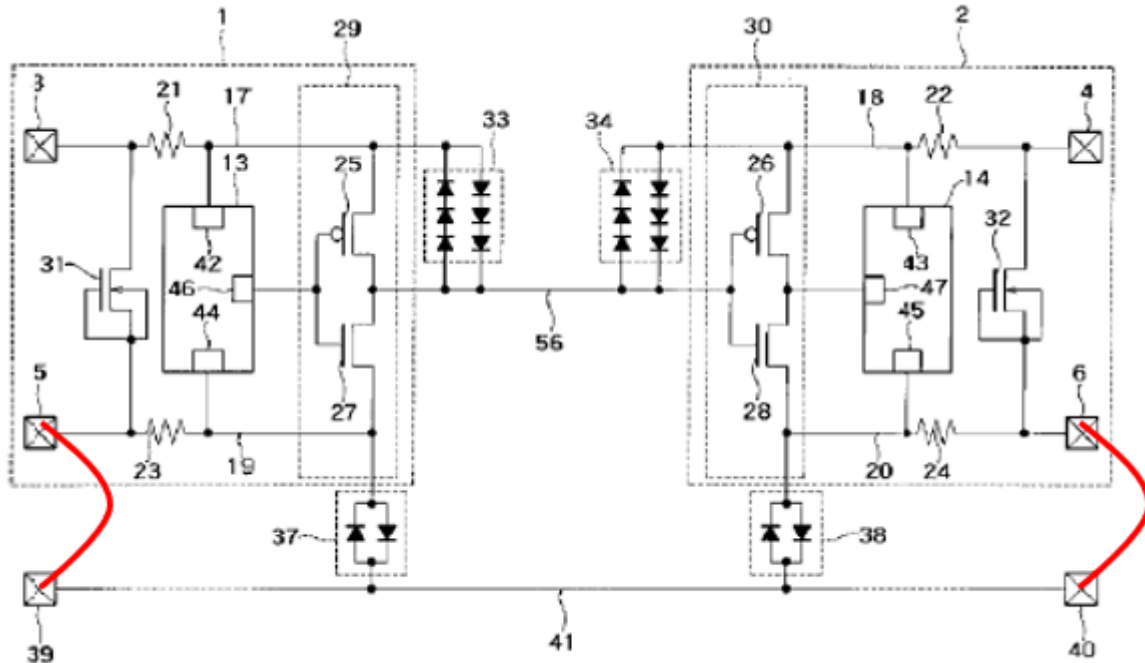
49. While admitting that “Yoshinaga discloses a common ESD bus” (Ex. 1003, ¶ 235), Dr. Foty asserts that a POSITA would have been motivated

to combine Haralabidis with Yoshinaga because, according to him, “notably, Yoshinaga discloses no teachings that involve what happens beyond the bond pads; thus, a POSITA would clearly be motivated to combine Yoshinaga with a reference that provides details on connecting the IC (via its bond pads) to external lines that could be used as destinations for the shunted energy of any ESD events” such as Haralabidis. Ex.1003 ¶ 224.

50. Dr. Foty again ignores that Yoshinaga states that “reference potential lines *may be connected by bidirectional diodes* that are connected in parallel to one another in the opposite direction *to avoid noise*.” Yoshinaga [0005] (emphasis mine). Yoshinaga further discloses how to connect reference potential lines 19 and 20 to a “third reference potential line 41” (such as the alleged “common ESD bus” of Haralabidis)—namely, “via a bidirectional diode pair 37 and a bidirectional diode pair 38” as shown in Figure 3. *Id.* [0061], Fig. 3. According to Yoshinaga, this “avoid[s] noise between the reference potential lines”. *Id.* I have discussed supra how the use of bond wires to connect reference potential pads would actually increase noise (due to the inductance of the bond wires as well as the direct injection of noise from one reference potential pad to the other) and also would cause the bidirectional diodes to never conduct and therefore never provide ESD protection. As a result, the inclusion of the teaching of Haralabidis contradicts and negates the teaching of Yoshinaga.

51. In my opinion, a POSITA would not have been motivated to look to other references like Haralabidis or Saint to connect reference potential lines 19 and 20 of Yoshinaga. Dr. Foty does not provide any reason that Yoshinaga's disclosures for connecting the reference potential lines 19 and 20 to a "third reference potential line 41" are inadequate or insufficient. Nor does Dr. Foty provide any reason why a POSITA would disregard Yoshinaga's disclosures of bidirectional diodes and use bond wires instead—a fundamentally different connection method with disadvantages that I have mentioned *supra*. Dr. Foty does not identify any advantages with using bond wires or any drawbacks such "bond wires" would solve. And, as discussed above, Dr. Foty ignores the drawbacks of using bond wires altogether.

52. Dr. Foty's proposed modification of adding "bond wires" (red) to connect reference potential pads 5 and 6 of Yoshinaga is redundant in view of Yoshinaga's teachings. Ex. 1003 ¶ 254. Dr. Foty's proposed modification is shown below in the modified version of Yoshinaga's Fig. 3, with the proposed bond wires shown in red:



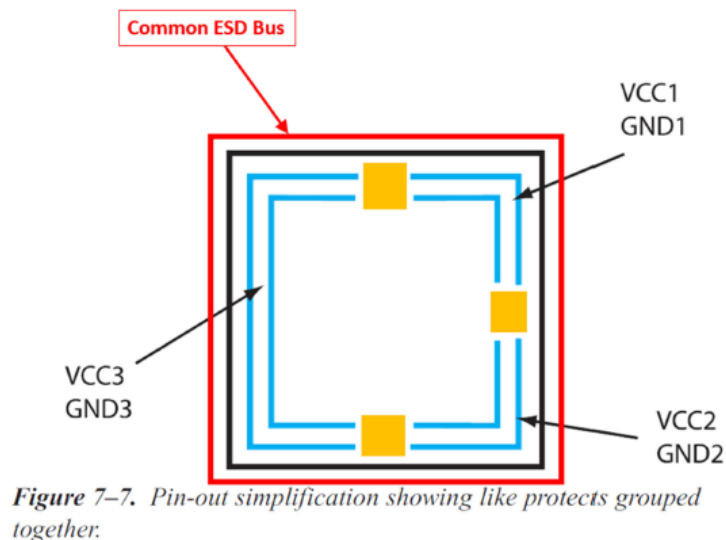
53. As shown, reference potential lines 19 and 20 are already connected by the bidirectional diodes (circuit elements 37 and 38). Yoshinaga Fig. 3, [0061]. Thus, the bond wires connecting reference potential pads 5 and 6 to the “third reference potential line 41” serve no beneficial purpose. In fact, they negatively impact both the ESD and noise performance of the design, as I have stated above. These red bond wires add additional (and unnecessary) components, parasitics (and associated noise), and complexity. Dr. Foty does not explain this at all, let alone why a POSITA would have been motivated to use bond wires as required by the patent claims.

IV. GROUND III

A. Saint, Haralabidis, and POSITA Knowledge Does Not Disclose Or Render Obvious “a common ESD bus”

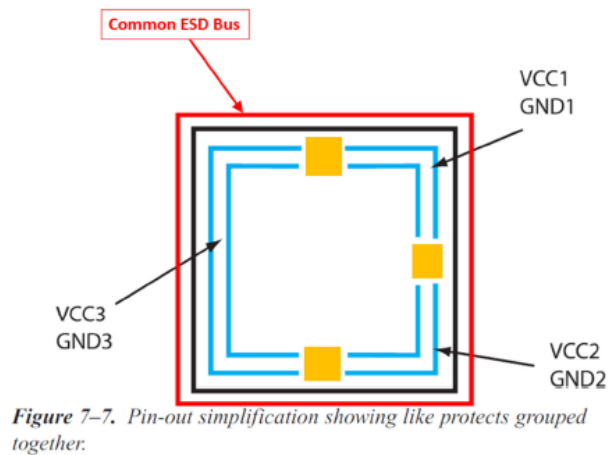
54. Dr. Foty argues that Saint and Haralabidis render obvious claims 1-14. I disagree. The independent claims of the '164 Patent require either (i) “a common ESD bus” (claims 1 and 8) or (ii) “a plurality of pad groups ... connected to the plurality of ESD buses,” wherein the “plurality of pad groups” are connected “to another” (claims 6 and 12).

55. Dr. Foty states that “it is a fairly simple exercise (and would have been a simple exercise for a POSITA) to add the common ESD bus described by Haralabidis to the Figure 7-7 presentation of Saint – and (*since they have to connect somewhere*) to connect the segmented rails of Saint’s Figure 7-7 presentation to this common ESD bus.” Ex. 1003 ¶ 368 (emphasis mine). Dr. Foty’s proposed modification is shown below.



56. As an initial matter, the segmented rails of Haralabidis are electrically the same terminal, since they are connected together either at the

package substrate or the printed circuit board (PC Board). In contrast, the reference rails of Saint are distinct and separate electrical terminals (GND1, GND2 and GND3) and are as such not segmented reference rails. Therefore it is incorrect to refer to these as “the segmented rails of Saint’s Figure 7-7”. Ex. 1003, ¶ 368.



57. Saint’s Figure 7-7 is derived from Figures 7-3, 7-4 and 7-5, which clearly show that the three reference rails GND1, GND2 and GND3 are separate and distinct electrical terminals, with separate and distinct voltages, and therefore it would be an error to connect them as Dr. Foty suggests. Saint 160-163. As these three figures from Saint show, the rails GND1, GND2 and GND3 are separate rails, that do not correspond to the same electrical terminal.

58. In the Saint reference, per Figure 7-3, pins 1, 5, 7 and 9 are protected against the VCC1 supply and the GND1 reference terminal. In Figure 7-4, pins 6, 8, 10 and 14 are protected against the VCC2 supply and the GND2

reference terminal, while in Figure 7-5, pins 2, 3, 4, 11, 12, 13, 15 and 16 are protected against the VCC3 supply and the GND3 reference terminal. If these pins are connected to the alleged “common ESD bus” in Dr. Foty’s modification, all these 16 pins would be protected against a common reference terminal (the common terminal in Dr. Foty’s modification) which would result in a different electrical design than contemplated by Saint. Dr. Foty provides no analysis as to why a POSITA would make such a drastic design change. In fact, a POSITA would not make such a change.

59. Dr. Foty overlooks that a POSITA would not have been motivated to add any “common ESD bus” to Figure 7-7 of Saint because the Figure 7-7 layout discloses three separate and distinct power supply voltages and reference potentials—namely VCC1/GND1, VCC2/GND2, and VCC3/GND3. Saint 160-163. Fig. 7-7 of Saint illustrates one way to arrange a circuit so that the pins 1 through 16, that are “protected to the same supply” are moved “close together” because the chip design has three *different* VCC and GNC signals. In other words, pins 1, 5, 7 and 9 are moved close together and protected against VCC1 and GND1, while pins 6, 8, 10 and 14 are moved close together and protected against VCC2 and GND2, and pins 2, 3, 4, 11, 12, 13, 15 and 16 are moved close together and protected against VCC3 and GND3. Saint never teaches connecting the different GND1, GND2, and GND3 signals together to

a “common ground” as Dr. Foty proposes. In fact, a POSITA would have understood from Figure 7-3, 7-4, 7-5 and 7-7 that GND1, GND2, and GND3 are separate reference potentials that should *not* be connected together as Dr. Foty proposes.

60. Dr. Foty tries to justify his proposal to use a common ground by pointing to “Case Study 1” at the end of Saint on page 344 and arguing that Saint also contemplates the use of a “single ground rail.” Ex. 1003 ¶ 359-360. As a preliminary matter, the case study Dr. Foty refers to starts on page 259 of Saint and walks through the design of a specific CMOS amplifier circuit. Saint does not say that the specific example of Case Study 1 can be generally applicable to all designs of Saint, let alone that it is applicable to Figure 7-7. In fact, this “single ground rail” is not applicable in general, and not applicable to Figure 7-7 in particular. Regardless, the exemplary CMOS amplifier design of Case Study 1 includes only one “GND” signal. Saint 261 and 273 (CS1-1, CS1-10). That is why CS1-99—the figure Dr. Foty relies on that is part of Case Study 1—shows the use of a single, “continuous ring” ESD ground wiring. Saint, 344. Dr. Foty himself recognizes that Figure 7-7 depicts “a design where there are three separate power supply and three separate ground lines” while the design of Case Study 1 is “*not* using the three-ground-rails (which provide three ESD buses) configuration of the Chapter 7 design” and instead “use[s] a *single* ground rail.”

Ex. 1003 ¶ 359-360.

61. Dr. Foty provides no reason that a POSITA would have been motivated by the disclosures of Saint's Case Study 1 that relate to a single ground signal design to modify the Figure 7-7 design to connect its three separate signals GND1, GND2, and GND3 together to a "common ESD bus," like the one Dr. Foty points to in Haralabidis. Connecting three separate signals together to a "common ESD ground" would drastically alter the electrical characteristics of the design and require other modifications as well. Such a modification would result in noise from one circuit being injected into another, which would result in a degradation of circuit performance. Further, the use of a "common ground rail (360)" in the package substrate as taught by Haralabidis, with wire bond connections to the chip, (see Ex. 1003, ¶ 367) would result in increased inductive and resistive parasitics, resulting in degraded reference impedances and increased noise. As a result, a POSITA would be discouraged to combine the teaching of Saint with Haralabidis, as Dr. Foty proposes.

62. Similarly, Haralabidis teaches the use of a "common ground rail" to connect "segmented ground rails." Ex. 1007 3:9-22, 3:34-40, 3:65-4:12. A POSITA would understand "segmented ground rails" to refer to a single ground signal that has been "segmented." That is fundamentally different from the design of Saint's Figure 7-7 that Dr. Foty relies on, which uses three *different*

ground signals, GND1, GND2, and GND3—not a single ground signal that has been “segmented.” Because of that, a POSITA would not have been motivated to change the Figure 7-7 design completely to connect three separate signals (GND1, GND2 and GND3) together as Dr. Foty proposes. Ex. 1003 ¶ 368.

63. As to the claims that require the “plurality of pad groups” connected “to another,” Dr. Foty references his discussion with respect to the “common ESD bus” claim elements and cites to Case Study 1 of Saint, without any additional analysis. Ex. 1003 ¶¶ 409, 448-49. Dr. Foty’s analysis fails for the same reason—namely, a POSITA would not have been motivated to connect the “plurality of pad groups” of Dr. Foty’s proposed modification of Figure 7-7 to each other because each of the pad groups correspond to an entirely distinct and separate reference signal (GND1, GND2, or GND3). Further, given that Case Study 1 has an on-chip “continuous ring around the active circuitry,” there would be no “plurality of pad groups”, and therefore no need to utilize a “plurality of bonding wires configured to connect one to another of the plurality of pad groups,” as taught by the ’164 patent.

64. As I have mentioned supra, Saint states that bond wires should only be used where there is “minimal silicon overlap.” Saint 195. According to Saint, “the bond wire could sag or droop, causing a short in the circuit” and “[s]o, you have to keep the overlap of the bond wire over the unused silicon as

short as possible.” *Id.* In view of Saint’s teachings, a POSITA would be discouraged from deliberately forming the bond wire to overlap entirely with “unused silicon” (the alleged “saved areas” shown in orange) as Dr. Foty proposes.

V. CONCLUSION

All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under penalty of perjury that the foregoing is true and correct.

Executed March 12, 2025 in College Station, Texas.



Dr. Sunil Khatri