

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: March 12, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00118
Patent 10,879,164

PATENT OWNER'S PRELIMINARY RESPONSE

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EXHIBIT LIST

Ex.	Description
2001	Micron's Motion to Stay the Case Pending Inter Partes Review and Post Grant Review Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Jan. 16, 2025), ECF No. 200
2002	Plaintiff/Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s and Counterclaim Defendant Yangtze Memory Technologies, Inc.'s Opposition to Micron's Motion to Stay Case Pending Inter Partes Review and Post-Grant Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Feb. 3, 2025), ECF No. 221
2003	Docket Entry Order (issuing temporary stay), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Mar. 3, 2025), ECF No. 242
2004	U.S. District Courts—Time Intervals from Filing Date to Beginning Date for Completed Civil Trials, by District, During the 12-Month Period Ending September 30, 2024 (https://www.uscourts.gov/sites/default/files/2025-01/jb_t3_0930.2024.pdf)
2005	RESERVED
2006	Curriculum Vitae of Dr. Sunil Khatri
2007	Declaration of Dr. Sunil Khatri ("Khatri")

I. Introduction

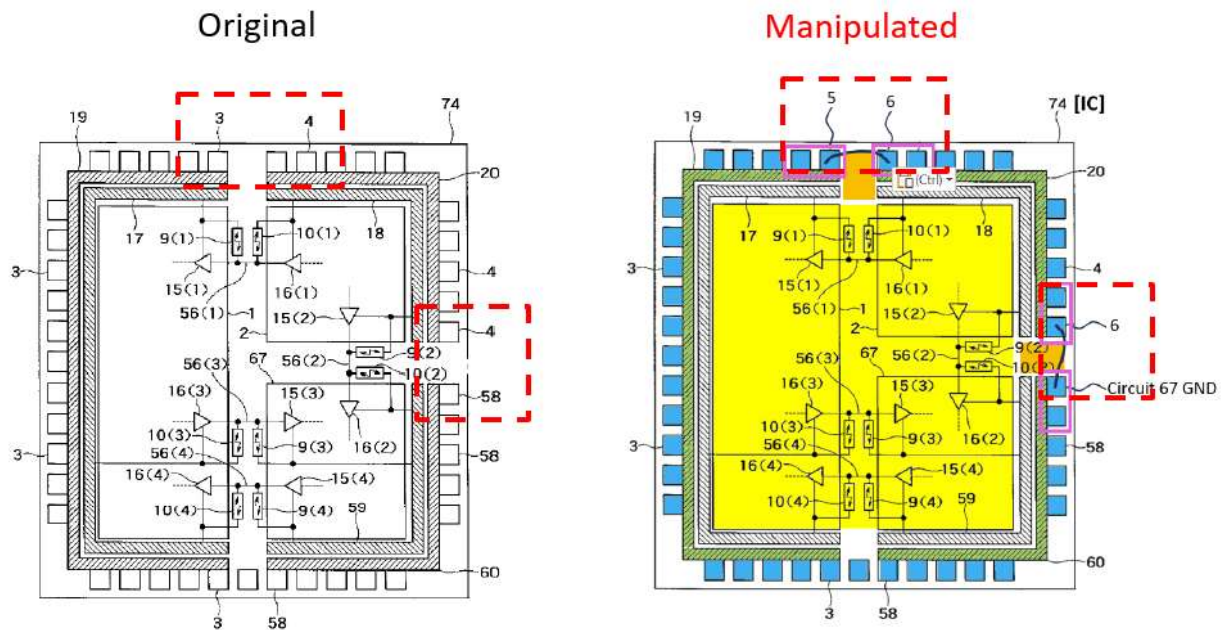
Patent Owner Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Patent Owner”) respectfully submits this Preliminary Response to the Petition for *inter partes* review of U.S. Patent 10,879,164 (“’164 patent” (Ex.1001)). As explained below, Petitioner fails to carry its burden to show a reasonable likelihood that at least one of the challenged claims is unpatentable. Thus, the Board should deny the Petition, and no IPR proceeding should be instituted.

The ’164 Patent discloses a novel “integrated circuit electrostatic discharge bus structure” that comprises a “plurality of pad groups” connected to a “plurality of ESD buses.” ’164 Patent Abst. The pad groups are connected either “one to another” or to a “common ESD bus” using “bond wires.” This results in “saved areas” between the “plurality of pad groups” and “plurality of ESD buses” where a designer can place additional circuitry.

Petitioner relies on two primary references for its obviousness grounds: Yoshinaga (Ex.1006) (Grounds 1-2) and Saint (Ex.1008) (Ground 3). Both fail.

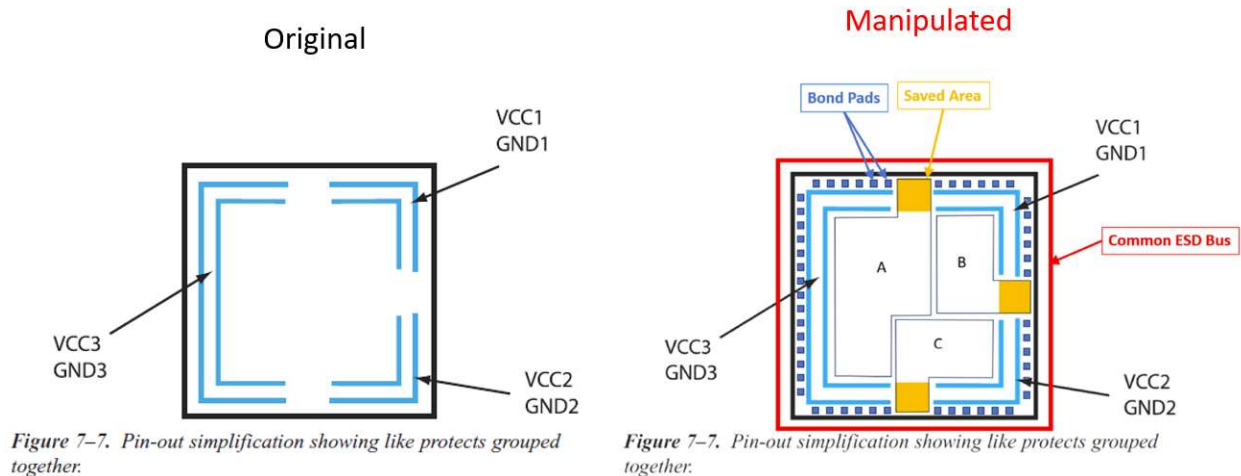
Petitioner acknowledges that Yoshinaga does not disclose “a plurality of pad groups” connected either “one to another” or to a “common ESD bus” with “bond wires.” Petitioner instead redraws Yoshinaga’s figures to (i) change “power supply pads” 3, 4, and 58 to “reference potential pads” 5, 6, and “Circuit 67 GND”

and (ii) add bond wires across the newly added reference potential pads, as shown below:



Petitioner provides no reason a POSITA would have been motivated to make these substantial changes or have a reasonable expectation of success in doing so.

As to Saint, Petitioner also relies on a heavily manipulated version of Saint's Figure 7-7 to support its obviousness arguments:



But Petitioner fundamentally misunderstands Figure 7-7. Petitioner's arguments hinge on its bald assertion that Figure 7-7's GND1, GND2 and GND3 are a "plurality of ESD *buses*." But Petitioner has failed to establish those lines are "buses" when Saint expressly refers to the figure as showing "pins" that are "located close to each other." Saint 160-161. Petitioner also ignores that each blue line represents *different* signals—VCC1/GND1, VCC2/GND2, and VCC3/GND3—that a POSITA would not be motivated to connect together as Petitioner proposes.

The Board should deny the Petition.

II. Background

A. The '164 Patent (Ex.1001)

The '164 Patent discloses "an integrated circuit electrostatic discharge bus structure and related method." '164 Patent 1:17-20; Khatri (Ex. 2007) ¶ 32.

In the prior art, an integrated circuit electrostatic discharge or “ESD” structure comprises a “circuit area 10,” “I/O pads 12,” and an “electrostatic discharge (ESD) bus 11” as shown in Figure 1. ’164 Patent 1:24-37. According to the ’164 Patent, it was “commonly [known] to place filler cells F1 and F2 at empty spaces between the I/O pads 12, and connect the filler cells F1 and F2 to an electrostatic discharge (ESD bus) 11.” *Id.* 1:30-37. The ESD bus is a “layout trace connected to a ground or a system voltage.” *Id.*

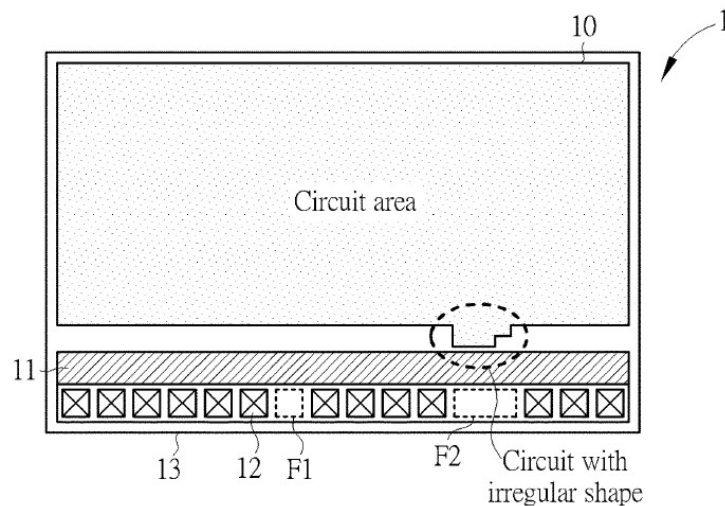


FIG. 1 PRIOR ART

A drawback of the prior art approach is that “filler cells F1 and F2 take a portion of the circuit area 10 to be wasteful to the integrated ESD bus structure 1.” *Id.* 1:38-43; Khatri ¶ 33. Further, as shown in Figure 1, “when there are circuits with irregular shapes and different areas, the circuit area 10 must be increased in order to contain the circuits with irregular shapes and different areas, which

increases production cost.” ’164 Patent 1:44-47. The ’164 Patent teaches two configurations for overcoming the drawbacks of the prior art.

Fig. 2 Embodiment. As shown in Figure 2, the ’164 Patent teaches one configuration where a “plurality of pad groups G1, G2 and G3 is formed inside the chip edges 23, adjacent and connected to the plurality of ESD buses E1, E2, and E3.” ’164 Patent 2:61-63. A “common ESD bus 24 is formed outside the chip edges 23.” *Id.* 2:63-65. Each of the “plurality of pad groups G1, G2 and G3 includes at least one pad 22” that is “connected to a ground or a system low voltage.” *Id.* 3:6-8. Bonding wires 25 connect “pads 22 of the pad groups G1, G2 and G3 to the common ESD bus.” *Id.* 3:17-22; Khatri ¶ 34.

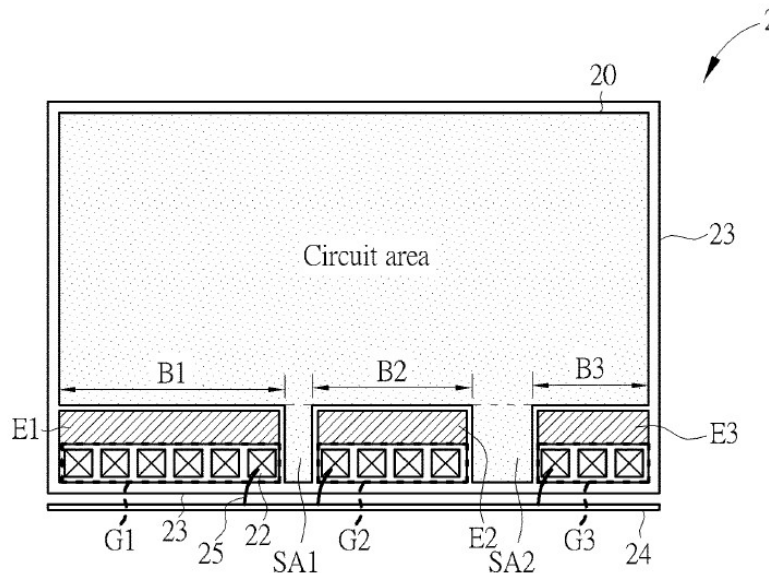


FIG. 2

As a result, “the discontinuous ESD buses E1, E2 and E3 may be connected together by connecting pads 22 of the pad groups G1, G2 and G3 to the common

ESD bus 24 through bonding wires 25.” ’164 Patent 3:17-22. This way, “spaces between the discontinuous ESD buses E1 and E2 (or, E2 and E3) may be configured with circuit elements to make full use of the integrated circuit ESD bus structure 2.” *Id.* 3:23-26. The ’164 Patent refers to those “spaces” as “saved areas SA1 and SA2.” *Id.* 3:29-32; Khatri ¶ 35.

Fig. 3 Embodiment. As shown in Fig. 3, an alternative embodiment also includes “circuit area 30,” a “plurality of ESD buses E1, E2 and E3,” a “plurality of pad groups G1, G2 and G3,” and “a plurality of bonding wire 35.” ’164 Patent 3:36-35. Unlike the Fig. 2 embodiment where the “bonding wires 25” connect pads 22 to a “common ESD bus,” the “bonding wires 35” of the Fig. 3 embodiment connect “pads 32 of one group to another group.” *Id.* 3:64-65. This also results in the “saved areas” for adding additional circuitry. Khatri ¶ 36.

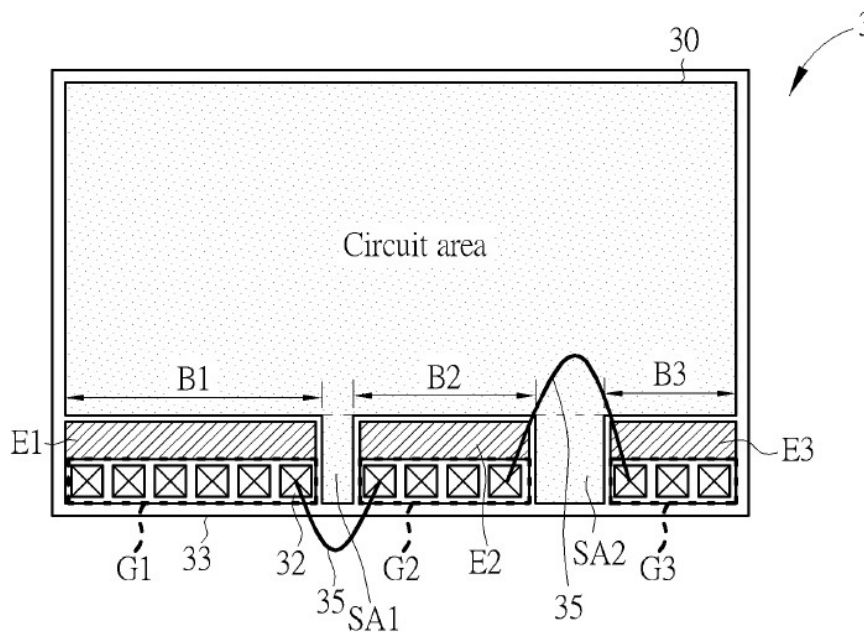


FIG. 3

B. Person of Ordinary Skill in the Art

For purposes of this Preliminary Response, YMTC does not dispute Petitioner's proposed level of a person of ordinary skill in the art ("POSITA").¹ Pet. 27. Regardless of the precise definition of a POSITA, Petitioner's grounds do not render any challenged claims unpatentable. Khatri ¶ 30.

C. Claim Construction

Petitioner asserts that the terms of the '164 patent's claims have their plain and ordinary meaning. Pet. 26. For purposes of this Preliminary Response, YMTC agrees because Petitioner fails to show that any Ground has a reasonable likelihood of prevailing under any reasonable construction, including their plain meaning.² Khatri ¶ 37.

¹ YMTC reserves the right to argue an alternative level of a POSITA in other proceedings or if the Board institutes review.

² YMTC reserves the right to argue alternative constructions in other proceedings or if the Board institutes review.

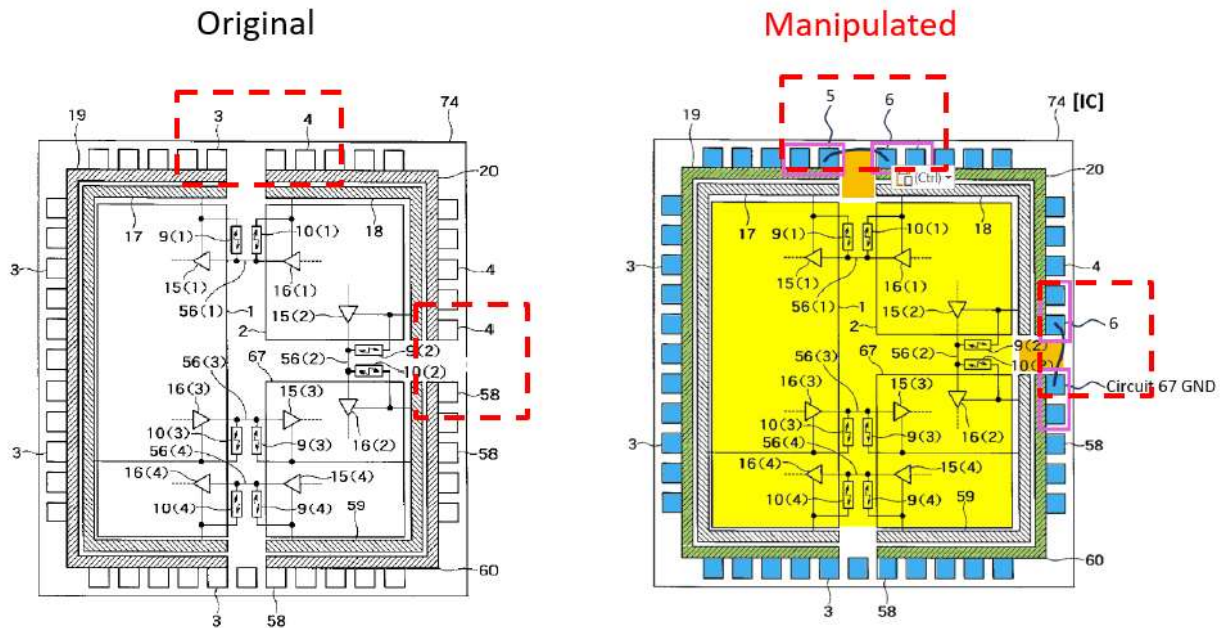
III. Ground 1: Petitioner Fails To Meet Its Burden to Establish Yoshinaga, Saint And POSITA Knowledge Renders Obvious Claims 6, 7, 12, and 14

A. Yoshinaga, Saint, and POSITA Knowledge Do Not Render Obvious “a plurality of bonding wires configured to connect one to another of the plurality of pad groups” (claims 6 and 7) or “connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires” (claims 12 and 14)

The Challenged Claims of Ground 1 (claims 6, 7, 12, and 14) require “a plurality of bonding wires configured to connect one to another of the plurality of pad groups” (claims 6 and 7) or “connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires” (claims 12 and 14). Petitioner identifies Yoshinaga’s “[r]eference potential pads” as the claimed “plurality of pad groups” (Pet. 30-31), because the claims require the “pad groups” to be connected to “ESD buses.”

Petitioner acknowledges that Yoshinaga does not disclose any “bonding wires”—let alone “bonding wires” that connect reference potential pads. Pet. 34-35. Petitioner nevertheless alleges that Yoshinaga, Saint, and the knowledge of a POSITA renders obvious “a plurality of bonding wires configured to connect one to another of the plurality of pad groups.” *Id.* To support its arguments, Petitioner redraws Yoshinaga’s Figure 6 with two improper modifications. Pet 36; Khatri ¶ 38. **First**, Petitioner changes Yoshinaga’s “power supply pad[s]” 3, 4, and 58 to become “reference potential pads” 5, 6, and “Circuit 67 GND.” Yoshinaga

(Ex.1006) [0076]-[0077]. **Second**, Petitioner draws bonding wires between its newly added reference potential pads.³ Pet. 36.



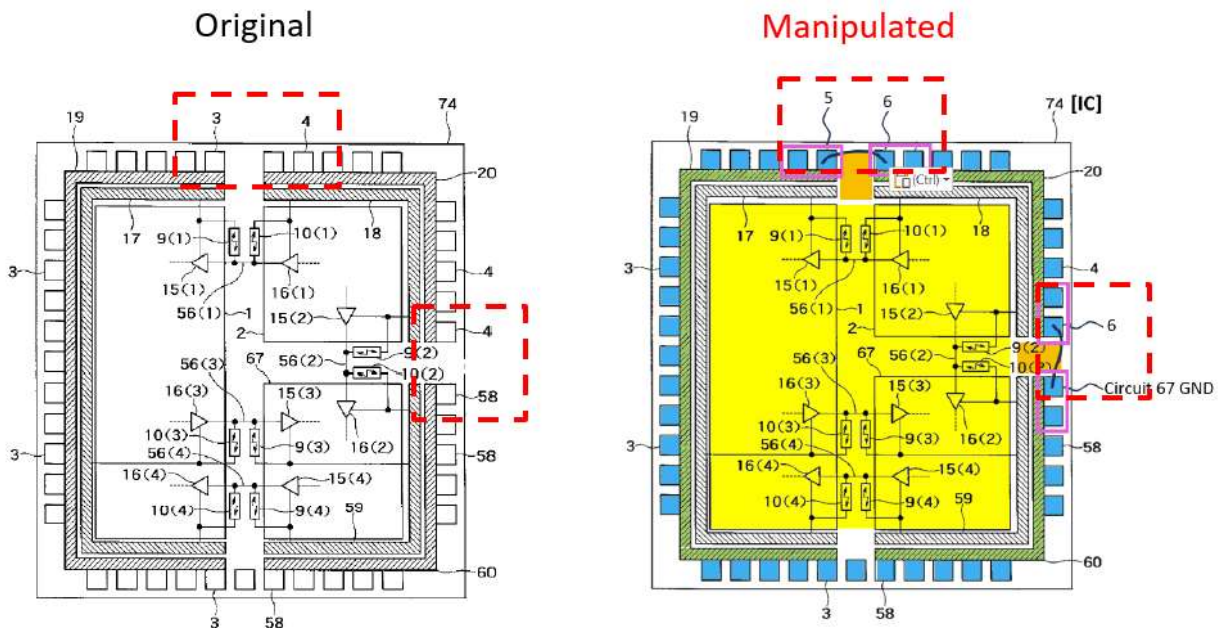
As discussed below, a POSITA would not have been motivated to make Petitioner's proposed modifications to Fig. 6 to render obvious "a plurality of bonding wires" that connect the "plurality of pad groups" or have had a reasonable

³ It is unclear whether Petitioner's manipulated Fig. 6 is even based on a version of Fig. 6 from Yoshinaga. For example, the manipulated figure includes an "[IC]" designation that is found nowhere in Yoshinaga. Compare Pet. 36 with Yoshinaga Fig. 6. Similarly, the term "Circuit 67 GND" is found nowhere in the version of Yoshinaga either. *Id.*

expectation of success in doing so. Khatri ¶¶ 38-48. As such, Petitioner failed to meet its burden to show that these limitations would have been obvious to a POSITA.

1. A POSITA Would Not Have Been Motivated To Replace Yoshinaga's Power Supply Pads With Reference Potential Pads Or Have Had A Reasonable Expectation Of Success In Doing So

Petitioner asserts that “POSITA would also have understood the pads labelled 3, 4, and 58 could just as readily be used as reference pads” to support Petitioner's relabeling of pads 3 and 4 to become the reference potential pads 5 and 6 as shown below. Pet. 31. Petitioner is incorrect.



First, Petitioner's assertion that power supply pads 3 and 4 “could” be used as “reference potential pads” is insufficient to establish that a POSITA “*would*

have” been motivated to change Yoshinaga’s power supply pads into reference potential pads. *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”) (citations omitted); *In re Nuvasive, Inc.*, 848 F.3d 1376, 1381-85 (Fed. Cir. 2016) (holding that a proper motivation to combine includes “identif[ying] a reason why a PHOSITA would have combined the prior art references—i.e., ‘minimiz[ing] waste’ and ‘allow[ing] for a greater degree of movement’—that had a foundation in the prior art”) (citations omitted). Petitioner identifies no advantages that would result from changing the power supply pads to reference potential pads. Nor does Petitioner identify any alleged problems changing power supply pads to reference potential pads would solve.

Petitioner makes the cursory assertion that “[o]ne reason” for changing power supply pads 3 and 4 into reference potential pads is “to preserve Yoshinaga’s saved area for other circuitry as taught by Saint.” Pet. 31-32. That misses the point. “[P]reserv[ing] Yoshinaga’s saved area” would, at most, motivate a POSITA not to place the reference potential pads in Yoshinaga’s alleged “saved area” (in orange). Khatri ¶¶ 41-42. It does not provide any motivation for a POSITA to take Yoshinaga’s power supply pads 3, 4, and 58 and change them into reference potential pads as proposed, or how such a significant

change would work. *Id. Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017) (“[A] clear, evidence-supported account of the contemplated workings of the combination is a prerequisite to adequately explaining and supporting a conclusion that a relevant skilled artisan would have been motivated to make the combination...”). Indeed, power supply pads and reference potential pads are fundamentally different: they are connected to different circuit elements and serve entirely different purposes. Khatri ¶ 39. Petitioner ignores this.

Second, Yoshinaga expressly states that “[r]eference potential pads are **not shown** to simplify the drawing” in Figure 6. Yoshinaga [0078]. Thus, the pads that **are** shown in Fig. 6—such as power supply pads 3, 4, and 58—are not reference potential pads. Khatri ¶ 39. Petitioner attempts to sidestep this flaw by asserting that “in Yoshinaga’s vernacular, the statement that ‘[r]eference potential pads are not shown’ ... simply means they are not labelled.” Pet. 20. Petitioner cites no support for its assertion that “not shown” actually means “not labeled.” As Petitioner recognizes, there are many other pads that are “not labelled” in Figure 6 (Pet. 20), yet Yoshinaga does not state that those other types of pads are all “not shown” merely because they are “not labelled.”

Indeed, Yoshinaga consistently uses the term “not shown” to refer to elements that do not appear in a figure. Yoshinaga [0084] (“previous ESD protective elements” are “not shown in Fig. 6” because they are “provided in the

underside” and not depicted); [0066] (“short[ing]” the “[t]he internal circuit reference potential terminal 44 and the signal terminal 46 in the internal circuit 14” is “not shown” in Fig. 4 and the internal circuitry of 14 is not depicted).

Third, a POSITA would not have had a reasonable expectation of success in changing power supply pads to reference potential pads as Petitioner proposes. *Eli Lilly and Co. v. Teva Pharms. Int’l GmbH*, 8 F.4th 1331, 1344 (Fed. Cir. 2021) (noting “the additional requirement that the patent challenger also prove that the skilled artisan would have had a reasonable expectation of successfully achieving the claimed invention from the combination.”) (citations omitted). As the Saint textbook recognizes “[y]ou cannot just blindly put your input/output pads wherever you feel like it” and there are “rules and guidelines” that must be followed. Saint (Ex.1008) 187. Saint includes entire sections about how to properly place pads for “powers” and “grounds.” *Id.* 143-147 (“Pin-Driven Planning”); Khatri ¶ 43. And Petitioner’s own expert acknowledges that “[t]he choice of selecting which pads to assign for ground [and] power ... depend[s] on factors such as the size of the chip, whether the chip is pad-limited or core-limited, the number of I/O signals, and the number of available pads.” Ex.1003 ¶ 137; Khatri ¶ 44. Consistent with Saint and Petitioner’s expert, a POSITA would understand that pads are not “largely fungible” as Petitioner alleges. Khatri ¶¶ 39-40.

In changing Yoshinaga's power supply pads to reference potential pads, Petitioner ignores all of the considerations for pad selection articulated in Saint and by its own expert. Khatri ¶¶ 43-44. Petitioner provides no evidence that a POSITA would have had a reasonable expectation of success in changing Yoshinaga's power supply pads to reference potential pads—especially where Saint further recognizes that the “choice of pin out” affects “parasitics” and “complexity” of the design. Saint 144-145; Khatri ¶¶ 43-44. Petitioner does not even explain where the power supply pads would be moved to if they are replaced with reference potential pads.

In short, Petitioner has failed to show that a POSITA would have had been motivated to change Yoshinaga's expressly disclosed “power supply pads” into “reference potential pads” or have had a reasonable expectation of success in doing so. Petitioner's proposed modifications to Yoshinaga fail for this reason alone.

2. A POSITA Would Not Have Been Motivated To Use Bond Wires To Combine Reference Pads As Shown In Petitioner's Manipulated Figure 6

Petitioner asserts that “[a]n obvious way to connect Yoshinaga's reference potential lines” is “by wire bonding the pads connected to the respective buses.” Pet. 35. Petitioner is incorrect.

First, Petitioner asserts that “Yoshinaga is silent regarding the mechanism used to connect the reference lines.” Pet. 35. Petitioner is incorrect. Yoshinaga

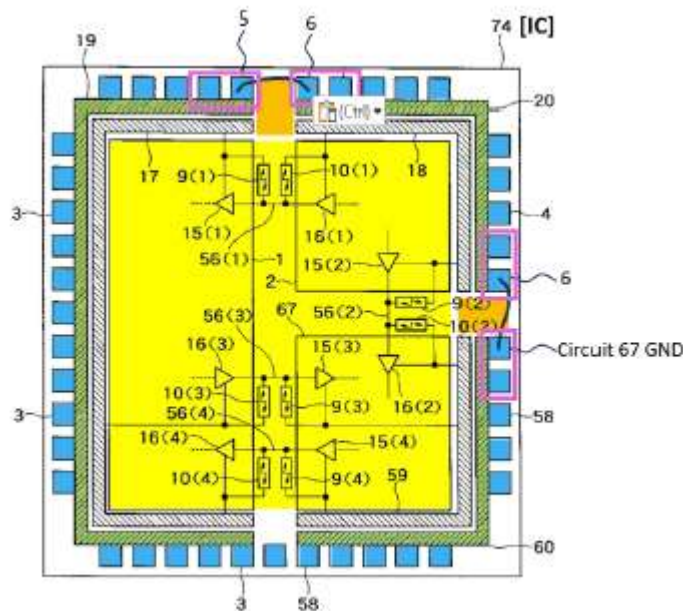
expressly discloses that “[t]he reference potential lines *may be connected by bidirectional diodes* that are connected in parallel to one another in the opposite direction to avoid noise.” Yoshinaga [0005]⁴; Khatri ¶¶ 45-46. Yoshinaga’s express disclosure renders Petitioner’s proposed modification of using “bond wires” to connect the reference potential lines entirely redundant. Khatri ¶¶ 45-46. Petitioner ignores Yoshinaga’s disclosure completely.

Second, even if not redundant, a POSITA would understand that connecting reference potential lines with “bidirectional diodes” as Yoshinaga teaches is different than connecting reference potential pads with bond wires. Khatri ¶ 46. Petitioner does not provide any reason why a POSITA would disregard Yoshinaga’s disclosure of connecting the reference potential lines “by directional diodes to avoid noise” and use bond wires to connect the reference potential pads instead. *Id.* Petitioner does not identify any advantages with using bond wires over bidirectional diodes or any drawbacks with the use of bidirectional diodes that bond wires would solve. *Id.* And Petitioner ignores that connecting reference potential pads with bond wires would be redundant given Yoshinaga’s express disclosure of using of bidirectional diodes to connect reference potential lines. *Id.*

⁴ All emphasis added unless noted otherwise.

Third, Petitioner cites references including the Saint textbook to show that the use of bond wires was “well-known to a POSITA at the Priority Date.” Pet. 36. Merely because “bond wires” were well-known does not mean a POSITA would have been motivated to use bond wires—especially in view of Yoshinaga’s teachings about connecting the reference potential lines 19 and 20 without bond wires to “reduce noise” as discussed above. *Belden Inc.*, 805 F.3d at 1073 (Fed. Cir. 2015); *In re Nuvasive, Inc.*, 848 F.3d at 1381-85.

Fourth, the Saint textbook Petitioner cites would discourage POSITAs from using bond wires between pads 5 and 6 and 6 and circuit 67 GND as Petitioner proposes (shown below). Khatri ¶¶ 47-48.



Saint teaches that bond wires should only be used where there is “minimal silicon overlap.” Saint 195. According to Saint, “the bond wire could sag or

droop, causing a short in the circuit” and “[s]o, you have to keep the overlap of the bond wire over the unused silicon as short as possible.” *Id.* In view of Saint’s teachings, a POSITA would be discouraged from deliberately forming the bond wire to overlap entirely with “unused silicon” (the alleged “saved areas” shown in orange) as Petitioner proposes. Khatri ¶¶ 47-48; *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994) (“A reference may be said to teach away when a person of ordinary skill, upon [examining] the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.”). Petitioner provides no explanation as to why a POSITA would be motivated to disregard Saint’s teachings and form the bond wires to be substantially over “unused silicon” as proposed.

IV. Ground 2: Petitioner Fails To Meet Its Burden to Establish Yoshinaga, Saint, Haralabidis, and POSITA Knowledge Renders Obvious Claims 1-6, 8-11, and 13

As an initial matter, claim 13 depends from claim 12. As explained above, Yoshinaga in view of Saint and POSITA knowledge do not render obvious claim 12. Petitioner only alleges that Haralabidis further discloses claim 13’s additional limitation of “a common ESD bus is parallel to the plurality of ESD buses and the plurality of pad groups” in claim 13. Thus, Petitioner has failed to meet its burden to establish that claim 13 is obvious for the same reasons discussed above with

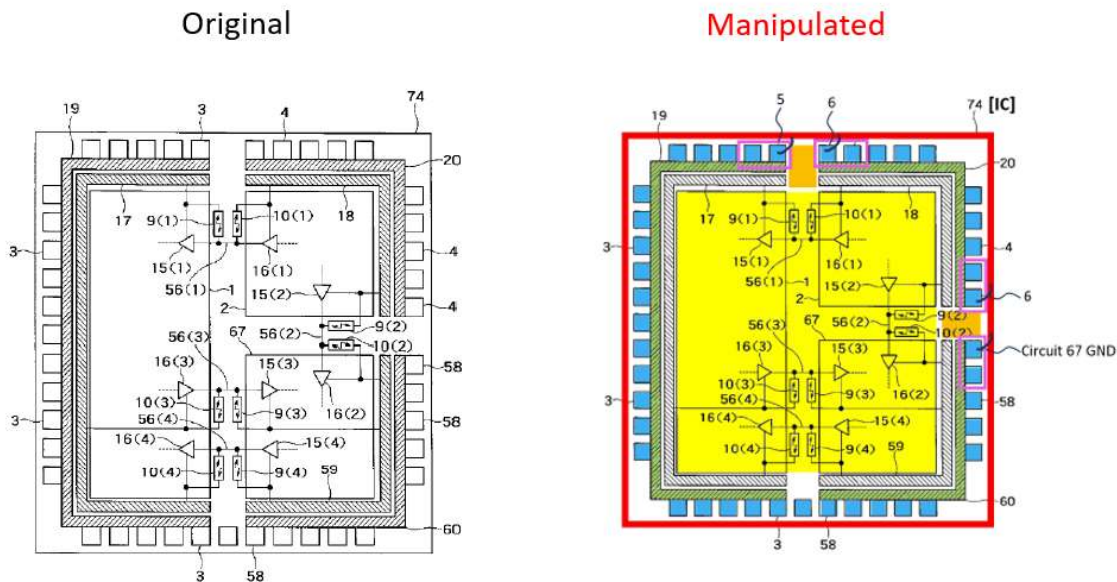
respect to Ground 1, i.e., Yoshinaga, Saint, Haralabidis, and POSITA knowledge fail to render obvious “connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires” as claim 12 requires.

A. Yoshinaga, Saint, Haralabidis, and POSITA Knowledge Do Not Render Obvious “a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus” and “connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires”

Claim 1-5, 8-11 of Ground 2 all require “a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus” (claims 1-5) and “connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires” (claims 8-11).⁵ Petitioner again identifies Yoshinaga’s “[r]eference potential pads” as the “plurality of pad groups.” Pet. 30-31.

⁵ Claim 6 does not recite using “bonding wires” to connect pad groups to a “common ESD bus.” Yet Petitioner asserts, with no explanation, that “Element [1.D] applies Haralabidis’ common ESD bus approach” and “[t]his same configuration meets [6.D] under PO’s overly broad interpretation.” Pet. 63. Petitioner appears to treat element [1.D] identically as [6.D], and therefore, Petitioner’s assertions as to claim 6 fail for the same reasons discussed for claim 1.

As discussed, Petitioner acknowledges that Yoshinaga does not disclose any “bonding wires.” Petitioner also acknowledges that Yoshinaga does not disclose a “common ESD bus.” Pet. 52-53. Petitioner nevertheless asserts that Yoshinaga combined with Saint and Haralabidis renders using “bonding wires” to connect a “plurality of pad groups” to a “common ESD bus” obvious. Pet. 56. To support its arguments, Petitioner again redraws Yoshinaga’s Figure 6. As discussed with Ground 1, Petitioner first changes Yoshinaga’s “power supply pad[s]” 3, 4, and 58 to become “reference potential pads” 5, 6, and “Circuit 67 GND.” Petitioner next adds a “common bus” (red) and “wire bonds” to “connect pad groups (via respective pads) to the common bus.” Pet. 57-58.



1. A POSITA Would Not Have Been Motivated To Replace Yoshinaga's Power Supply Pads With Reference Potential Pads Or Have Had A Reasonable Expectation Of Success In Doing So

As with Ground 1, Petitioner's combination requires changing Yoshinaga's power supply pads 3, 4, and 58 into reference potential pads 5, 6, and "Circuit 67 GND." Petitioner does not assert any additional reason to support this proposed modification with respect to Ground 2. Petitioner's proposed modification of Ground 2 therefore fails for the same reasons discussed with respect to Ground 1.

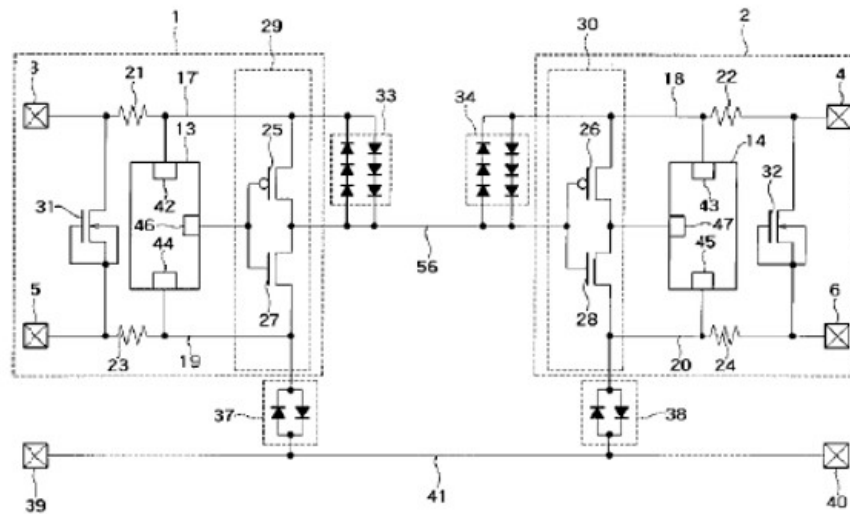
2. A POSITA Would Not Have Been Motivated To Connect a "plurality of pad groups" to a "common ESD bus" with "bond wires"

Petitioner asserts that Yoshinaga combined with Haralabidis' "common ground rail 360" and "bond wires" from Saint and the knowledge of a POSITA renders obvious connecting a "plurality of pad groups" to a "common ESD bus" Pet. 56-58. Petitioner is incorrect.

First, Petitioner asserts that "Yoshinaga teaches the reference voltage lines for each circuit (e.g., 1, 2, 67) are connected, but does not teach any specific connection technique/implementation." Pet. 52, 66-67. Petitioner again overlooks Yoshinaga's express disclosures.

As discussed above, Yoshinaga states that "reference potential lines *may be connected by bidirectional diodes* that are connected in parallel to one another in the opposite direction to avoid noise." Yoshinaga [0005]; Khatri ¶¶ 49-50.

Yoshinaga further discloses how to connect reference potential lines 19 and 20 to a “third reference potential line 41” (such as the alleged “common ESD bus” of Haralabidis in Petitioner’s proposed combination)—namely, “via a bidirectional diode pair 37 and a bidirectional diode pair 38” as shown in Figure 3. Yoshinaga [0061], Fig. 3. According to Yoshinaga, this “avoid[s] noise between the reference potential lines.” *Id.*; Khatri ¶ 50.

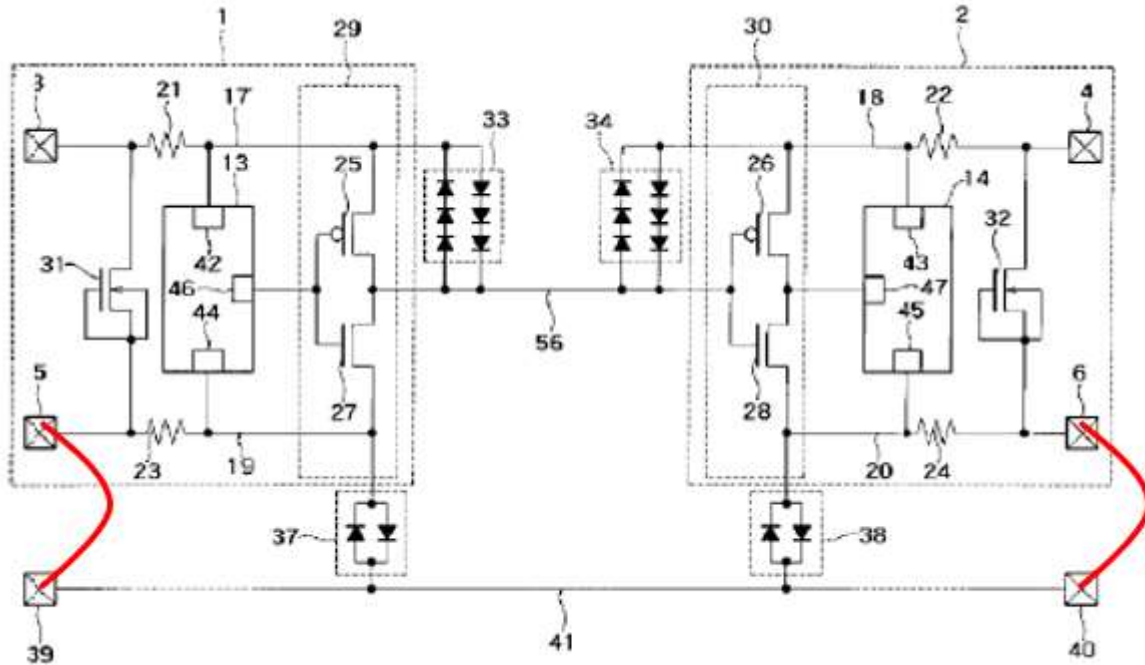


Thus, a POSITA would not have been motivated to look to other references like Haralabidis or Saint to connect reference potential lines 19 and 20; Yoshinaga already teaches how those lines are connected to “avoid noise.” Yoshinaga [0061]; Khatri ¶ 51. Petitioner does not provide any reason that Yoshinaga’s disclosures for connecting those lines to a “third reference potential line 41” are inadequate or insufficient. *Id.* Nor does Petitioner provide any reason why a POSITA would disregard Yoshinaga’s disclosures and use bond wires instead—a fundamentally

different connection method that has the effect of introducing noise. *Id.* Petitioner does not identify any advantages with using bond wires or any drawbacks such “bond wires” would solve. And, as discussed above, Petitioner ignores the drawbacks of using bond wires altogether.

Second, Petitioner's proposed modification of adding “bond wires” (red) to connect reference potential pads 5 and 6 (Pet. 58), of Yoshinaga is redundant in view of Yoshinaga's teachings. Khatri ¶ 52. Petitioner's proposed modification is shown below in the modified version of Yoshinaga's Fig. 3, with the proposed bond wires shown in red⁶:

⁶ Petitioner recognizes that the “ESD circuitry and connections” of Figure 3 apply to the layout shown in Figure 6. Pet. 22.

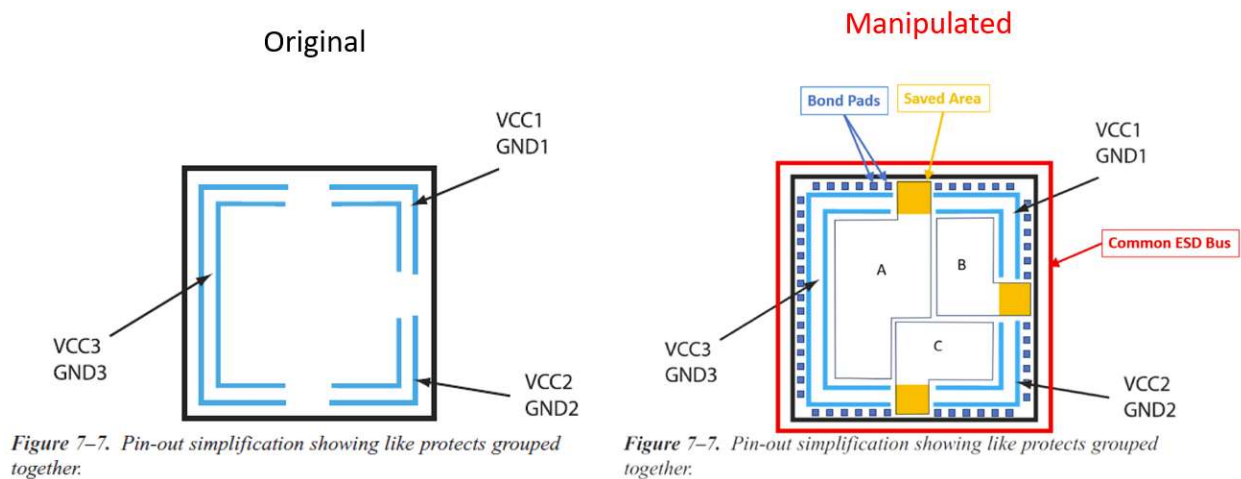


As shown, reference potential lines 19 and 20 are already connected by circuit elements 37 and 38 when a third reference potential line is used. *Khatri* ¶ 53; *Yoshinaga* Fig. 3, [0061]. In other words, the bond wires connecting reference potential pads 5 and 6 to the “third reference potential line 41” serve no beneficial purpose. *Khatri* ¶ 53. They only add additional (and unnecessary) components, parasitics (and associated noise), and complexity. *Id.* Petitioner does not propose removing elements 37 and 38, which would be unnecessary if bond wires were added—let alone explain why a POSITA would have had a reasonable expectation of success in doing so. In short, Petitioner’s proposal of adding bond wires to connect *Yoshinaga*’s reference potential pads to a common ESD bus ignores the actual disclosures of *Yoshinaga*.

Thus, a POSITA would not have been motivated to modify Yoshinaga to use bond wires to connect a “plurality of pad groups” to a “common ESD bus” as Petitioner proposes.

V. Ground 3: Petitioner Fails To Meet Its Burden To Establish Saint, Haralabidis, and POSTIA Knowledge Renders Obvious Claims 1-14

Petitioner's Ground 3 is based cobbling together discrete, cherry-picked disclosures from the Saint textbook and Haralabidis, and then creating a heavily manipulated version of Fig. 7-7 of Saint as shown below:



As discussed below, Petitioner's manipulations are based on a fundamental misunderstanding of Figure 7.

A. Saint, Haralabidis, and POSITA Knowledge Does Not Disclose Or Render Obvious “a plurality of ESD buses” (claims 1-14)

All Challenged Claims require “a plurality of ESD buses.” Petitioner asserts that “Saint discloses three GND (known as ground or reference voltage) buses shown in blue in Figure 7-7, which constitute a plurality of ESD buses.” Pet. 70.

Petitioner has failed to establish that the blue lines of Figure 7-7 are “buses.”

According to Saint, Figure 7-7 is a “simplification” to show discrete “pins” that are “located close to each other.” Saint 145-147. Discrete pins are not “buses.” Pet. 70-71 (acknowledging that a “bus” is a “layout trace.”).

Specifically, Figure 7-7 is titled “*Pin-out simplification*” showing like protects grouped together.” Saint 145-147. Figure 7-7 is intended to show an improvement to the immediately preceding figure, 7-6. According to Saint, it is not desirable to have pins corresponding to GND1 (blue), GND2 (gray), and GND3 (blue outline) “[s]cattered” around the chip, as shown in Fig. 7-6.

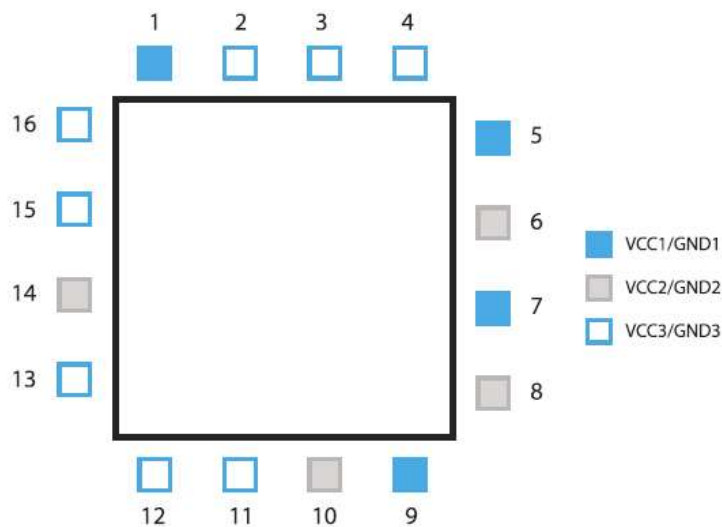


Figure 7-6. Scattered pins on the same protect circuit.

To remedy the deficiencies of Fig. 7-6, Saint teaches taking pins that correspond to the same ground, such as “pins 1, 5, 7, and 9” which are all GND1, and “mov[ing] them close to each other.” Saint 147. Saint teaching “do[ing] the same for the other supply pin sets” so that the pins corresponding to GND1,

GND2, and GND3 are all “located close to each other.” *Id.* The result is shown in Figure 7-7, which Saint describes as a “***Pin-out*** simplification showing like protects grouped together.”

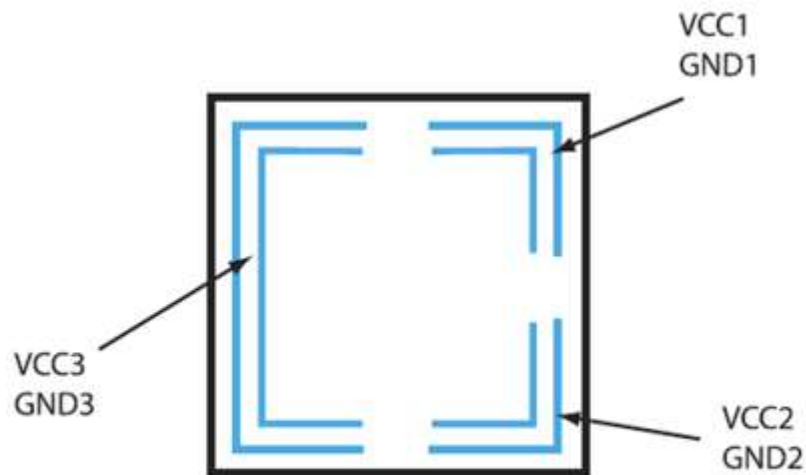


Figure 7-7. Pin-out simplification showing like protects grouped together.

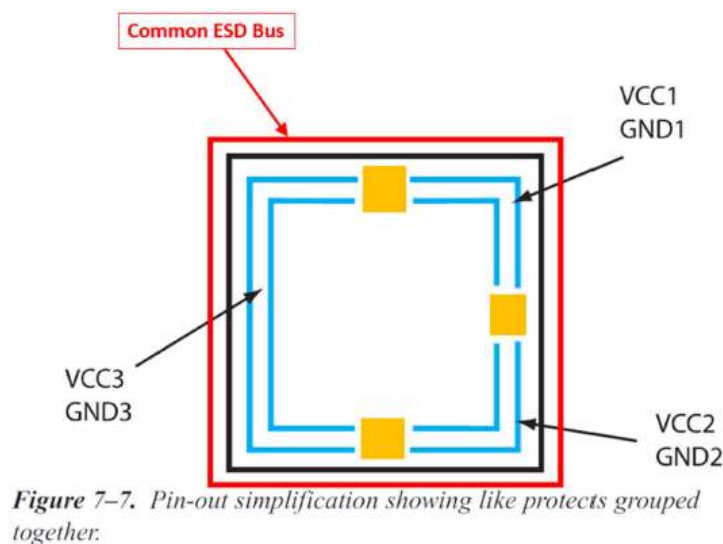
In other words, Petitioner has failed to show that the “blue lines” Petitioner identifies are “buses” or “traces,” rather than “pins” that are “grouped close to each other.”

Petitioner ignores Saint’s disclosures about Fig. 7-7 and concludes, without analysis or support, that the blue lines are “buses.” Pet 70-71. Petitioner provides no reason why a POSITA would understand that Saint’s disclosure of pins “grouped close to each other” to be “ESD buses” or “traces.” Pet. 70-71. Indeed, Saint discusses “[b]uses” in other sections, separate from its discussion of pin layouts. *See, e.g.,* Saint 165, 277, 298, 321, 368.

Ground 3 should be rejected because Petitioner has failed to identify a “plurality of ESD buses” as required by every Challenged Claim.

B. Saint, Haralabidis, and POSITA Knowledge Does Not Disclose Or Render Obvious “a common ESD bus” (claims 1-5, 8-11) or “connect[ing] one to another of the plurality of pad groups” (claims 6-7)/“connecting one of the plurality of pad groups to another” (claims 12-14)

Petitioner asserts “[a]pplying either Saint’s ‘ESD Ground Wiring’ or Haralabidis’ common ground rail teachings” renders obvious a “common ESD bus” as shown in Petitioner’s modified version of Figure 7-7 from Saint below. Pet. 76-77. Petitioner is incorrect.



Petitioner ignores that Saint’s Figure 7-7 teaches the use of three separate and distinct ground signals—GND1, GND2, and GND3—and that Saint does not contemplate, teach, or suggest shorting them together as Petitioner proposes with its “common ESD bus” shown above. Saint 160-163; Khatri ¶¶ 55-57. Petitioner

provides no reason a POSITA would do so. Indeed, Saint's Figure 7-7 is derived from Figures 7-3, 7-4 and 7-5, which all show three separate reference rails GND1, GND2, and GND3. Khatri ¶¶ 56-57. And according to Saint, the whole point of Figure 7-7 is to illustrate one way to arrange a circuit when a design has three *different* VCC and GNC signals. *Id.* Saint never teaches connecting the different GND1, GND2, and GND3 signals together in the layout of Figure 7-7—let alone contemplates using a “common ESD bus” to do so. Khatri ¶¶ 56-58. To the contrary, a POSITA would understand that three separate signals GND1, GND2, and GND3 should *not* be connected together as Petitioner proposes. *Id.* ¶¶ 58-59.

Petitioner's reliance on Fig. CS1-99 of Saint and Haralabidis' disclosures do not support its proposed modification.

First, Fig. CS1-99 is part of “Case Study 1” at the end of the Saint textbook that walks through an exemplary circuit layout process. Notably, the exemplary design of Case Study 1 includes only one “GND” signal. Saint 261 (CS1-1, CS1-10); Khatri ¶ 60. As a result, Saint teaches that a single “continuous ring” can be used as an “ESD Ground Wiring” for that case study design with a single GND. Saint 344; Khatri ¶ 60. The layout shown in Figure 7-7, however, includes three *separate* ground signals, GND1, GND2, and GND3. In fact, Petitioner's expert recognizes that Figure 7-7 depicts “a design where there are three separate power supply and *three separate ground lines*” while the design of Case Study 1 is “*not*

using the three-ground-rails (which provide three ESD buses) configuration of the Chapter 7 design” and instead “use[s] a *single* ground rail.” Ex. 1003 ¶ 359.

A POSITA would not have been motivated by Saint’s “Case Study 1” to connect the three separate ground signals of Figure 7-7 together to a “common ESD bus” as Petitioner proposes. Khatri ¶ 61. At a minimum, this would result in drastically changed electrical characteristics of the design and would require additional design changes that Petitioner ignores. Khatri ¶ 61. Petitioner’s cherry-picking from entirely separate disclosures of Saint is legal error. *In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017) (“combining embodiments in a single reference” requires “a motivation to make the combination”).

Second, as to Haralabidis, Petitioner alleges that “it was common practice to place ‘package common ground rail 360’ around an IC.” Pet. 75. Petitioner ignores that Haralabidis contemplates a single ground signal that is “segmented,” not three separate reference potentials. Haralabidis 3:9-22, 3:34-40, 3:65-4:12; Khatri ¶¶ 56, 62. Because of that, Haralabidis discloses a “common ground rail 360” to connect the segmented—but common—ground signal together. Haralabidis 3:9-22, 3:34-40, 3:65-4:12. Haralabidis does not disclose or suggest using a “common ground rail” to connect together three different and separate ground signals, such as those explicitly shown in Figure 7-7 of Saint as Petitioner proposes. Khatri ¶¶ 62. A POSITA would understand Haralabidis’ teachings of a

“common ground rail” are simply inapplicable to (and incompatible with) a design like Figure 7-7 with different ground signals/reference potentials, expressly labeled GND1, GND2, and GND3. *Id.* Petitioner does not address this at all.

In short, Petitioner does not explain why a POSITA would have been motivated add a “common ESD bus” to Figure 7-7, which is intended to illustrate a layout for a design that uses three separate reference signals, or why a POSITA would have had a reasonable expectation of success in shorting the three different signals of Figure 7-7 together. Khatri ¶¶ 56-62.

Third, rather than a “common ESD bus,” claims 6 and 7 require “a plurality of bonding wires configured to connect one to pad in the at least one saved area another of the plurality of pad groups” and claims 12-14 require “connecting one of the plurality of pad groups to another of the plurality of pad groups.” Petitioner and its expert rely on the same arguments as it does for the “common ESD bus” (Pet. 86, 93) and does not provide any actual analysis on how the prior art allegedly renders obvious these limitations. Khatri ¶ 63. Petitioner’s arguments should be rejected for this reason alone. *Id.* Regardless, Petitioner’s arguments fail for the same reasons discussed above with respect to a “common ESD bus”—namely, a POSITA would not have been motivated to connect any alleged “plurality of pad groups” to one another in Figure 7-7 of Saint because Figure 7-7 contemplates three separate ground signals, GND1, GND2, and GND3. Nor would

a POSITA have had a reasonable expectation of success in connecting those three different signals in Figure 7-7 together as Petitioner proposes. The Petition does not address this fact at all.

VI. The Board should exercise its discretion and deny institution under 35 U.S.C. § 314.

Institution of an IPR is always discretionary. 35 U.S.C. § 314(a). Here, the Board should exercise its discretion to deny institution because the Petition will not serve as an effective and efficient alternative to litigation. Rather, the overall balance of the *Fintiv* factors shows that “efficiency, fairness, and the merits support the exercise of authority to deny institution.” *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (Mar. 20, 2020) (precedential).

A. Factor 1 favors denial if the district court denies Petitioner's motion to stay and lifts the temporary stay before institution.

The Court has temporarily stayed the Parallel Proceeding⁷ while it considers Petitioner's motion for a stay pending IPRs. Ex. 2001; Ex. 2003. The Parallel Proceeding involves 70 asserted claims from 19 patents. Ex. 2002 at 006. Of those, the Board has only instituted IPRs against 23 claims from 8 patents. Ex. 2002 at 006. And 11 claims from one patent have had IPR institution denied

⁷ *Yangtze Memory Technologies Company, Ltd. V. Micron Technology, Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.).

across the board. *Id.*; *see, e.g., Entangled Media, LLC v. Dropbox Inc.*, 732 F. Supp. 3d 1120, 1124 (N.D. Cal. 2024) (characterizing arguments about simplification as “premature” “[b]ecause the PTO has not yet instituted proceedings,” and denying motion to stay); *Skillz Platform Inc. v. Aviagames Inc.*, No. 21-cv-02436-BLF, 2022 WL 1189882, at *3–4, *5 (N.D. Cal. Apr. 21, 2022) (denying motion to stay, stating that any simplification from IPRs “is purely *speculative at this stage*,” and “*the cost of non-institution would be delay without benefit*”).

It is not clear how long the temporary stay will remain in effect.⁸ However, if the district court denies Petitioner’s stay motion and lifts the temporary stay, Factor 1 would favor denial. *Inergy Tech., Inc. v. Force MOS Tech. Co.*, IPR2024-00094, Paper 9 at 32 (May 21, 2024) (denial of stay motion favors discretionary denial of IPR petition); *see also Fintiv*, Paper 11 at 7-8 (similar).

For these reasons, this factor favors discretionary denial of institution.

⁸ YMTC reserves its rights to address changes in the district court proceeding as they relate to discretionary denial in future briefs.

B. Factor 2 is neutral because the trial date is three days after Final Written Decision.

Trial is set to begin in the Parallel Proceeding on June 15, 2026.⁹ Ex. 1021 at 002. That is three days after the statutory deadline for a Final Written Decision in this case (June 12, 2026). And it is *well before* the expected Final Written Decisions that would issue in *eight* other proceedings filed by Micron against patents at issue in the Parallel Proceeding. *See* IPR2025-00190, -00191, -00228, -00229, -00244, -00245, -00294, and PGR2025-00021. This factor therefore favors denial of institution, or is at worst neutral. *Fintiv*, IPR2020-00019, Paper 11 at 9 (“If the court’s trial date is at or around the same time as the projected statutory deadline, ... the decision whether to institute will likely implicate other factors”); *Catalyst Orthoscience Inc. v. Shoulder Innovations, Inc.*, PGR2024-00042, Paper 17 at 12-14 (Dec. 19, 2024) (finding Factor 2 neutral where scheduled trial was “just weeks” after the scheduled conclusion of the PGR). A Final Written Decision here would issue after expert discovery, after dispositive motions, and after the pretrial conference. Ex. 1021 at 002.

⁹ Petitioner’s assertion of a 48.9-month median time to trial misleadingly includes non-jury trials, which have a significantly longer time-to-trial. *See* Ex. 2004 at 003. The corresponding number for jury trials is 32.8 months. Ex. 2004 at 003.

C. Factor 3 favors denial because substantial effort will have been expended by the deadline for institution.

The parties have expended, and continue to expend, substantial resources into the Parallel Proceeding. In that case, the parties have collectively propounded, responded to, and supplemented responses to 38 interrogatories and 117 requests for production. The parties have already produced over 113,000 pages of documents and are continuing to produce thousands more pages of documents. Ex. 2002 at 012. They have also engaged in extensive source code discovery, which has involved 14 days of YMTC expert and/or attorney review of code in this District and, more recently, three weeks and counting of code review at Micron's headquarters in Boise, ID. Ex. 2002 at 012. And upon order of the Court, YMTC has narrowed its claims of infringement to 70 asserted claims, which has required extensive analysis of infringement, validity, and damages issues. Ex. 2002 at 012.

The parties have also devoted, and continue to devote, substantial effort to claim construction, including exchanging claim terms and proposed constructions and filing a Joint Claim Construction and Prehearing Statement. The parties have also exchanged expert declarations in connection with claim construction and conducted two claim construction expert depositions.

Petitioner's assertion that the parties and district court have invested "very little" in the Parallel Proceeding is both wrong and, at the time of this filing and the institution decision, outdated. Petitioner does not even address the substantial

effort invested in the Parallel Proceeding in the more than 7 months between filing and the Board's institution decision. Because the parties and the Court will expend significant effort in the parallel litigation *before institution*, this factor favors discretionary denial of institution. *See, e.g., Comcast Cable Commc'ns, LLC v. Touchstream Techs., Inc.*, IPR2024-00323, Paper 13 at 9-10, 2024 WL 3530021, at *4 ("Factor 3 favor[ed] denial" where "substantial work on claim construction [had] happened," and "the related district court litigation ha[d] progressed in other aspects as well," including with respect to contentions); *10x Genomics, Inc. v. President & Fellows of Harvard Coll.*, IPR2023-01299, Paper 15 at 18, 2024 WL 993828, at *8 (similar, noting that the parties had exchanged contentions, "completed claim construction briefing," and that the "district court ha[d] also considered two motions to dismiss and presided over several discovery disputes"); *Boe Tech. Grp. Co. v. Element Cap. Com. Co. Pte. Ltd*, IPR2023-00808, Paper 9 at 23, 2023 WL 7715885, at *8 (finding "the parties and the District Court ha[d] invested substantial resources in th[e] litigation" because, among other things, "[s]ignificant discovery ha[d] been completed, including the exchange of infringement and invalidity contentions, document requests and interrogatories, and proposed claim terms for construction").

D. Factor 4 favors denial because there is significant overlap between the issues raised in the Petition and the district court proceeding.

Petitioner Micron has served invalidity contentions identifying the same art from its Petition, and explicitly incorporating its IPR petition by reference.

Petitioner has also not filed a *Sotera*-type stipulation in this proceeding. *Cf. Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (Dec. 1, 2020)

(precedential). Although Petitioner stipulates in its Petition that “[s]hould the Board institute, it will not advance in District Court on any ground asserted in this Petition,” no such stipulation has been made in the district court. Pet. 10. Such a narrow stipulation runs the risk of significant overlap both in consideration of the same evidence and arguments framed as “different grounds” than the Petition.

Because such a narrow stipulation risks having the district court address substantially the same evidence and arguments that the Board will have to address should it institute an IPR, and on a similar timeline, an IPR of the ’164 patent

would be an inefficient use of the Board’s resources and would risk conflicting decisions. *See 10x Genomics*, IPR2023-01299, Paper 15 at 20, 2024 WL 993828, at *9 (“[W]e agree with Patent Owner that the overlapping art and arguments presented in the parallel proceeding weigh in favor of exercising our discretion to deny institution.”) (footnote omitted); *see also Comcast*, IPR2024-00323, Paper 13 at 12, 2024 WL 3530021, at *5 (questioning whether a narrower stipulation “not to pursue in the District Court any ground that utilizes the same combination of prior

art references relied upon in the instituted petition” adequately addressed “concerns of inefficiency and the possibility of conflicting decisions”).

E. Factor 5 favors denial because Micron is the defendant in the district court proceeding.

Petitioner is the defendant and counterclaimant in the parallel district court case and, as such, will have a full and fair opportunity to litigate its (overlapping) invalidity contentions in that forum. Thus, this factor favors discretionary denial. *Comcast*, IPR2024-00323, Paper 13 at 13, 2024 WL 3530021, at *5 (“Petitioner is the defendant in the related district court case.... We find that this factor favors denial.”) (citations omitted); *Boe Tech.*, IPR2023-00808, Paper 9 at 24-27, 2023 WL 7715885, at *9.

F. Factor 6: The limited resources of the Board favors denial.

“The sixth *Fintiv* factor takes into account other circumstances that may bear on the decision to exercise discretion to deny, such as the merits of the patentability challenges.” *Comcast*, IPR2024-00323, Paper 13 at 13, 2024 WL 3530021, at *5 (citation omitted). For the reasons explained in Sections III-VI, the Petition fails on the merits for numerous reasons and thus does not present a “particularly strong” showing that can tip the scales in favor of institution. *Fintiv*, IPR2020-00019, Paper 11 at 14-15 (“[I]f the merits of a ground raised in the petition seem particularly strong on the preliminary record, this fact has favored institution.... [I]f the merits of the grounds raised in the petition are a closer call,

then that fact has favored denying institution when other factors favoring denial are present.”) (citations omitted); *see also USPTO Rescinds Memorandum Addressing Discretionary Denial Procedures* (Feb. 28, 2025), available at <https://www.uspto.gov/about-us/news-updates/uspto-rescinds-memorandum-addressing-discretionary-denial-procedures> (compelling merits analysis no longer applicable).

As five of the six *Fintiv* factors favor discretionary denial of institution, and the remaining factor is, at worst, neutral, Patent Owner respectfully requests that the Board exercise its discretion to deny institution.

VII. Conclusion

For the reasons set forth above, the Board should deny the Petition for *Inter Partes* Review.

Respectfully submitted,

Dated: March 12, 2025

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CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Patent Owner's Preliminary Response complies with the word count limitation of 37 C.F.R. § 42.24(b)(1) because the Patent Owner's Preliminary Response contains 7,069 words using Microsoft Word's counting feature, excluding the cover page, signature block, and the parts of the Patent Owner's Preliminary Response exempted by 37 C.F.R. § 42.24(b)(1).

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 12th day of March, 2025, a true and correct copy of the foregoing **Patent Owner's Preliminary Response and all Exhibits** were served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

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