

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2025-00118
Patent 10,879,164 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

KOKOSKI, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Micron Technology, Inc. (“Petitioner”) filed a Petition to institute an *inter partes* review of claims 1–14 of U.S. Patent No. 10,879,164 B2 (“the ’164 patent,” Ex. 1001). Paper 1 (“Pet.”). Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) filed a Preliminary Response. Paper 10 (“Prelim. Resp.”). With Board authorization, Petitioner filed a Preliminary Reply (“Prelim. Reply,” Paper 12), and Patent Owner filed a Preliminary Sur-reply (“Prelim. Sur-reply,” Paper 14).

Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314 (2018); *see also* 37 C.F.R. § 42.4 (2023). For the reasons discussed below, we determine that Petitioner establishes a reasonable likelihood of prevailing with respect to the unpatentability of at least one claim of the ’164 patent. We also determine that the arguments and evidence of record do not support discretionary denial of the Petition under 35 U.S.C. § 314(a). Accordingly, we institute an *inter partes* review of claims 1–14 of the ’164 patent.

A. *Real Parties in Interest*

Petitioner identifies “Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC” as the real parties in interest. Pet. 5. Patent Owner identifies itself as the real party in interest. Paper 5 (Mandatory Notice), 1.

B. *Related Matters*

The parties indicate that the ’164 patent is asserted in *Yangtze Memory Techs. Co., Ltd. v. Micron Tech. Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.). Pet. 5; Paper 5, 1.

C. The '164 Patent

The '164 patent, titled “Integrated Circuit Electrostatic Discharge Bus Structure and Related Method,” relates to an integrated circuit electrostatic discharge (“ESD”) structure and method that makes “full use of the circuit area.” Ex. 1001, code (54), 1:48–50. The '164 patent explains that filler cells are commonly placed at empty spaces between the input/output (“I/O”) pads and connected to an ESD bus to provide ESD protection to the integrated circuit ESD bus structure. *Id.* at 1:30–37. The filler cells, however, occupy a portion of the circuit area, which is “wasteful to the integrated circuit ESD bus structure,” and “causes the lack of flexibility for internal circuit layout design” under the “strict requirement” that the integrated circuit ESD bus structure have a rectangular shape. *Id.* at 1:38–43. To address these issues, the '164 patent provides an integrated circuit (“IC”) ESD structure that includes a circuit area, a plurality of ESD buses, a plurality of pad groups, and a plurality of bond wires configured to connect one another to another of the plurality of pad groups. *Id.* at 1:65–2:4.

Figure 3 is reproduced below.

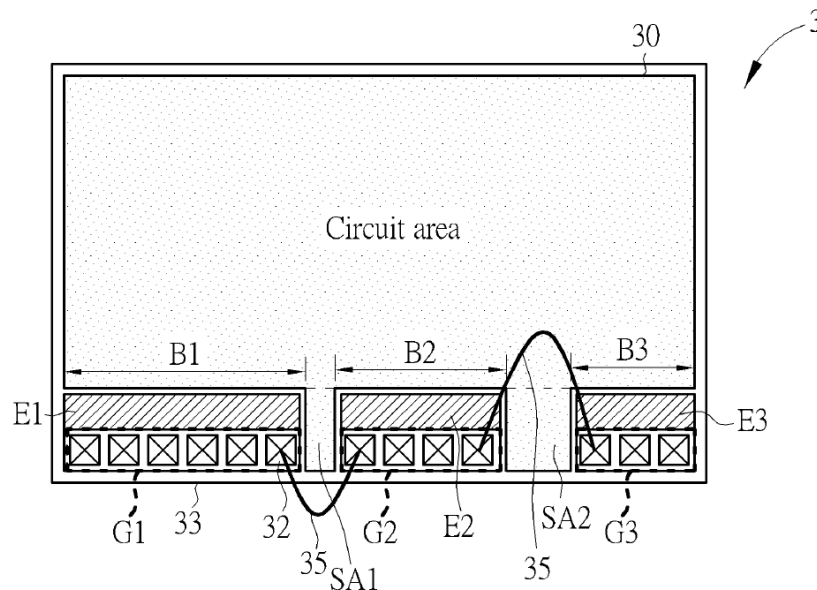


FIG. 3

Figure 3 is a schematic diagram of an integrated circuit ESD bus structure described in the '164 patent. Ex. 1001, 2:35–37. Integrated circuit ESD bus structure 3 includes circuit area 30, plurality of ESD buses E1, E2, and E3, plurality of pad groups G1, G2, and G3, and plurality of bond wires 35. *Id.* at 3:36–41. Circuit area 30 is contained within a rectangular area formed by four chip edges 33. *Id.* at 3:42–44. ESD buses E1, E2, and E3 are formed inside chip edges 33, corresponding to adjacent discontinuous boundaries B1, B2, and B3. *Id.* at 3:46–48. Saved areas SA1 (adjacent to ESD buses E1 and E2 and pads 32 of pad groups G1 and G2) and SA2 (adjacent to ESD buses E2 and E3 and pads 32 of pad groups G2 and G3) replace the filler cells commonly used in the prior art. *Id.* at 3:27–32; 4:20–22. Pad groups G1, G2, and G3 are also formed inside chip edges 33, adjacent and connected to ESD buses E1, E2, and E3. *Id.* at 3:51–54. Each of pad groups G1, G2, and G3 includes plurality of pads 32, wherein each pad 32 is an I/O pad connected to a ground or system low voltage. *Id.* at 3:61–64. One of

bonding wires 35 is configured to connect the rightmost pad 32 of pad group G1 to the leftmost pad 32 of pad group G2, and another one of bonding wires 35 is configured to connect the rightmost pad 32 of pad group G2 to the leftmost pad of pad group G3, thus “equivalently form[ing] a continuous ESD bus for the integrated circuit ESD bus structure 3.” *Id.* at 4:5–15.

According to the ’164 patent, saved areas SA1 and SA2 may be configured with circuit elements to make full use of integrated circuit ESD bus structure 3. Ex. 1001, 4:17–20. As a result, circuit area 30 “may contain the circuits with irregular shapes and different areas without increasing its area, which saves production cost.” *Id.* at 4:22–25.

D. Illustrative Claims

Claims 1, 6, 8, and 12 are the independent challenged claims. Claims 6 and 12 are illustrative of the claimed subject matter, and are reproduced below.

1. [6.PRE] An integrated circuit structure, comprising:
 - [6.A] a circuit area;
 - [6.B] a plurality of ESD buses;
 - [6.C] a plurality of pad groups, adjacent and connected to the plurality of ESD buses; and
 - [6.D] a plurality of bonding wires configured to connect one to another of the plurality of pad groups;
 - [6.E] wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

Ex. 1001, 5:42–54 (bracketed material added by Petitioner).

12. [12.PRE] A method of integrated circuit structure, comprising:

[12.A] forming a circuit area;

[12.B] forming a plurality of ESD buses;

[12.C] forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses; and

[12.D] connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires across the circuit area;

[12.E] wherein the circuit area comprises at least one save area, each of at least one save area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

Id. at 6:32–47 (bracketed material added by Petitioner).

E. Asserted Grounds

Petitioner asserts that claims 1–14 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
6, 7, 12, 14	103	Yoshinaga, ¹ Saint ²
1–6, 8–11, 13	103	Yoshinaga, Saint, Haralabidis ³
1–14	103	Saint, Haralabidis

Pet. 7–8. Petitioner relies on the Declaration of Dr. Daniel Foty (“Foty Declaration,” Ex. 1003) to support its contentions. Patent Owner submits

¹ Yoshinaga, JP2006-93598, published April 6, 2006 (Ex. 1006).

² Christopher Saint & Judy Saint, IC MASK DESIGN: ESSENTIAL LAYOUT TECHNIQUES (2002) (Ex. 1008).

³ Haralabidis, US 9,070,700 B2, issued June 30, 2015 (Ex. 1007).

the Declaration of Dr. Sunil Khatri (Ex. 2007) in support of its Preliminary Response.

II. ANALYSIS

A. *Level of Ordinary Skill in the Art*

Petitioner contends that a person of ordinary skill in the art (“POSITA”)

would have had a bachelor of science degree in electrical engineering or similar discipline, and 2–3 years of professional experience working with (*e.g.*, researching, analyzing, designing, or teaching) ICs, or equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience and vice versa). This POSITA would have been aware of and generally knowledgeable about IC design, layout, manufacturing, packaging, and ESD protection.

Pet. 18 (citing Ex. 1003 ¶¶ 29–33). Patent Owner states that, for purposes of its Preliminary Response, it “does not dispute Petitioner’s proposed level of” ordinary skill in the art. Prelim. Resp. 7.

For purposes of this Decision, we adopt Petitioner’s undisputed proposed definition because it appears to be consistent with the cited prior art and the disclosure of the ’164 patent. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required “where the prior art itself reflects an appropriate level and a need for testimony is not shown” (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985))).

B. *Claim Construction*

We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in

the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

Petitioner contends that “the ’164 Patent’s claims do not require further construction and should receive their plain and ordinary meaning.” Pet. 18. For purposes of its Preliminary Response, Patent Owner agrees with Petitioner. Prelim. Resp. 7.

Based on the record before us, we determine that no claim term requires express construction for purposes of this Decision. *See Realtime Data*, 912 F.3d at 1375.

C. Ground 1: Asserted Obviousness over Yoshinaga and Saint

Petitioner contends that claims 6, 7, 12, and 14 would have been obvious over the combined teachings of Yoshinaga and Saint. Pet. 27–52.

1. Yoshinaga

Yoshinaga relates to a semiconductor integrated circuit having an ESD protection circuit. Ex. 1006 ¶ 1.

Figure 6 is reproduced below.

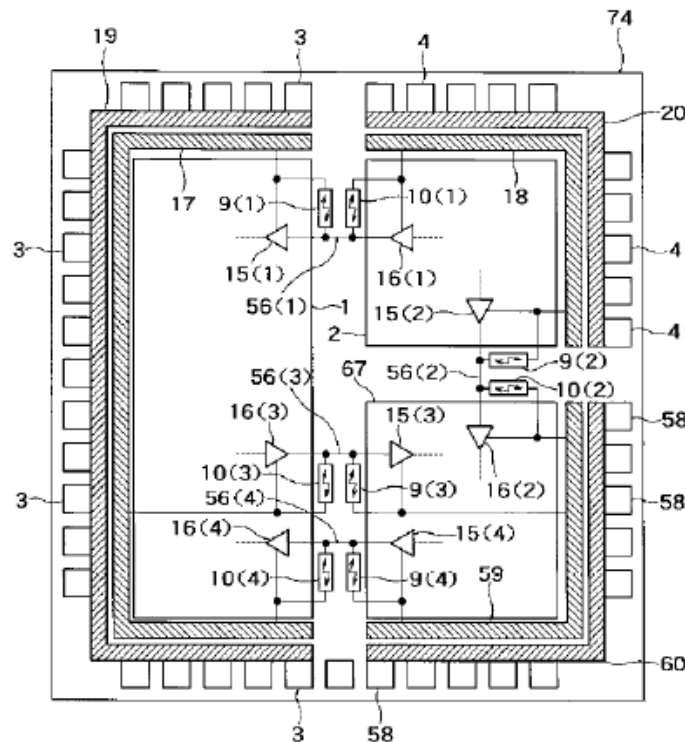


Figure 6 is a schematic diagram of an integrated circuit chip included in a semiconductor integrated circuit described in Yoshinaga. *Id.* ¶ 87.

Integrated circuit chip 74 consists of three major circuits: circuit 1, circuit 2, and circuit 67. *Id.* ¶¶ 74–75. Rectangular power supply pad 3, power supply pad 4, and power supply pad 58 are disposed near each circuit 1, 2, 67 at the periphery of the chip. *Id.* ¶ 76. The power supply line is divided into power supply line 17, power supply line 18, and power supply line 59. *Id.* ¶ 77. The reference potential line is divided into reference potential line 19, reference potential line 20, and reference potential line 60, and is positioned outside the power supply line parallel to power supply lines 17, 18, 59. *Id.*

Signal boundary portion 15 (1) in circuit 1 is connected at signal boundary portion 16(1) and signal line 56 (1) in circuit 2. Ex. 1006 ¶ 79. Signal line 56(1) is connected to power supply line 17 via ESD protective

element 9 (1) and to power supply line 18 via ESD protective element 10 (1), which provides protection from ESD at the signal boundary. *Id.* Signal boundary portion 15 (2) in circuit 2 is connected at signal boundary portion 16 (2) and signal line 56 (2) in circuit 67. *Id.* ¶ 80. Signal line 56 (2) is connected to power supply line 18 via ESD protective element 9 (2) and to power supply line 59 via ESD protective element 10 (2), which provides protection from ESD at the signal boundary. *Id.* Signal boundary portion 15 (3) in circuit 67 and signal boundary portion 16 (3) in circuit 1 are connected by signal line 56 (3). *Id.* ¶ 82. Signal line 56 (3) is connected to power supply line 59 via ESD protective element 9 (3) and is connected to power supply line 17 via ESD protective element 10 (3). *Id.* ¶ 82. Signal boundary portion 15 (4) in circuit 67 and signal boundary portion 16 (4) in circuit 1 are connected by signal line 56 (4). *Id.* ¶ 83. Signal line 56 (4) is connected to power supply line 59 via ESD protective element 9 (4) and to power supply line 17 via ESD protective element 10 (4). *Id.*

ESD protective elements 9 (1) to 9 (4) and 10 (1) to 10 (4) are provided in the chip interior as shown in Figure 6. Ex. 1006 ¶ 84. Yoshinaga explains that “[n]ormally, it is difficult to use a large ESD protective element inside the chip,” but in the chip shown in Figure 6, “the size of the ESD protective element may be small . . . so it is possible to greatly improve the ESD resistance while keeping the chip size as small as possible.” *Id.* Therefore, Yoshinaga teaches,

a significant improvement in ESD resistance can be achieved by providing ESD protective elements that can be energized bi-directionally between one power supply line and the signal line and between the other power supply line and the signal line, respectively, between circuits in which the power supply lines

are separated from each other and have signal propagation paths (signal lines).

Id. ¶ 85. Yoshinaga also explains that, because the size of the ESD protective element may be small, “there is little increase in the chip size and the total number of wiring” and “increase in the unit price of the chip can be prevented as much as possible.” *Id.* ¶ 86.

2. *Saint*

Saint, titled *IC Mask Design: Essential Layout Techniques*, is a textbook “that provides step-by-step detailed guidance on every aspect of the mask design process.” Ex. 1008, 13.⁴ For example, *Saint* teaches that “[w]ire bonding is the most common method of attaching a chip to a package.” *Id.* at 207. *Saint* also teaches that, in a core-limited circuit design, there will be “wasted space around the edges between pads,” but if circuits are being reused, parts of the circuit elements can be re-laid in around the pads to try “to get the chip as small as possible.” *Id.* at 220–221.

3. *Claim 6*

Petitioner contends that the combination of Yoshinaga and *Saint* discloses all of the limitations of claim 6. Pet. 27–41. Petitioner relies on an annotated version of Yoshinaga’s Figure 6, reproduced below, to illustrate some of its contentions.

⁴ We refer to the page numbers added by Petitioner to the bottom right corner of the page.

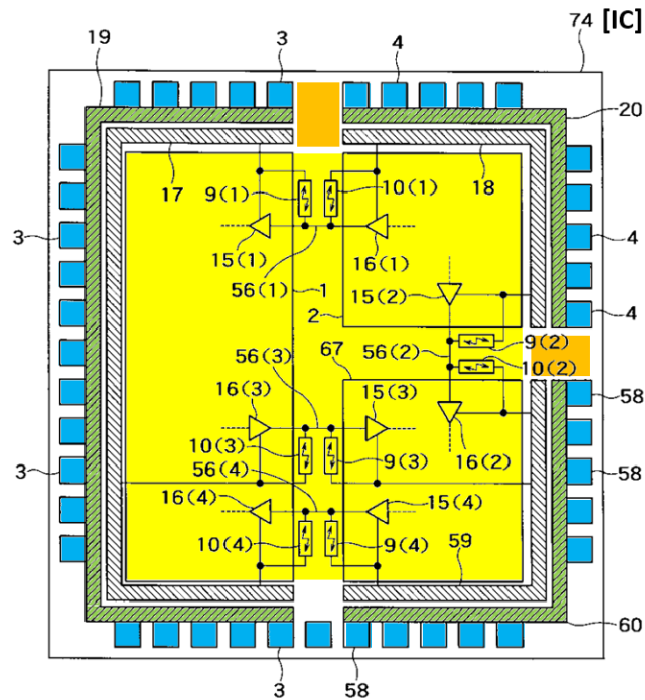


Figure 6 is a schematic diagram of an integrated circuit chip included in a semiconductor integrated circuit described in Yoshinaga with Petitioner's addition of blue shading to the rectangles surrounding the chip, green shading to the border area below the blue rectangles, orange shading at the top and right side of the chip in the open area between ends of the green shaded area, and yellow shading to the interior of the chip. Pet. 28; Ex. 1006 ¶ 87. Referring to annotated Figure 6, Petitioner contends that Yoshinaga teaches "a circuit area" (area containing circuits 1, 2, and 67 (yellow)), "a plurality of ESD buses" (reference potential lines 19, 20, and 60 (green)), and "the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of the two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area" (orange shaded area adjacent to reference potential lines 19, 20, 60 (ESD buses, green) and two respective pad groups (blue)). Pet. 27–30, 39–

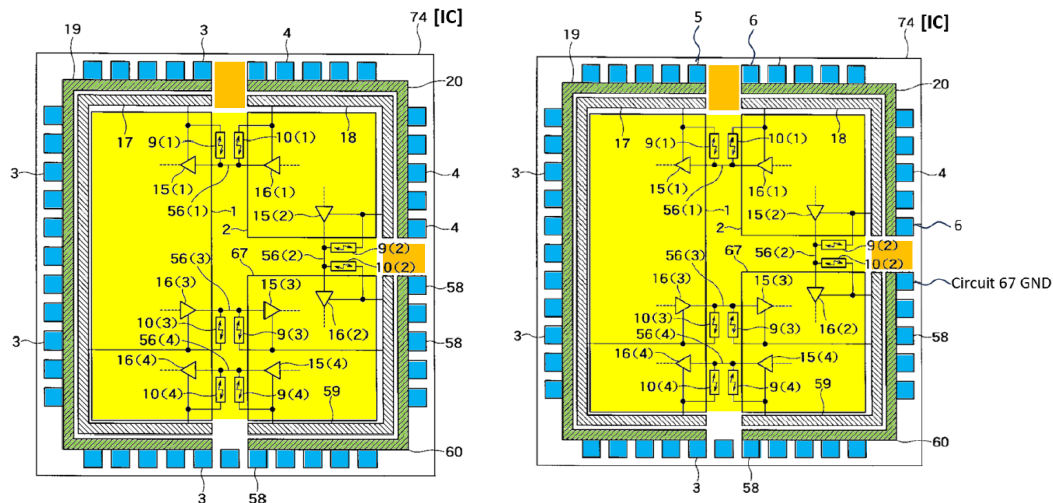
41 (and evidence cited therein). At this stage of the proceeding, Patent Owner’s arguments in response are directed to the “a plurality of pad groups, adjacent and connected to the plurality of ESD buses” and “a plurality of bonding wires configured to connect one to another of the plurality of pad groups” limitations of claim 6. *See* Prelim. Resp. 8–17. We address these limitations below.

a) “a plurality of pad groups, adjacent and connected to the plurality of ESD buses”

With respect to the “a plurality of pad groups, adjacent and connected to the plurality of ESD buses” limitation of claim 6, Petitioner asserts that Yoshinaga’s Figure 6 “shows various ‘pads’ (blue), such as power supply pads 3, 4, and 58.” Pet. 31 (citing Ex. 1006 ¶¶ 76–77, Fig. 6). Petitioner further asserts that “Yoshinaga explains that ‘[r]eference potential pads are not shown [in Fig. 6] to simplify the drawing,’ but they are shown in Figs. 1–4 (numerals 5, 6, 39, 40).” *Id.* (citing Ex. 1006 ¶ 78, Figs. 1–4) (alteration in original). Petitioner notes that “Yoshinaga Fig. 6 is an illustrative rendering, not intended to necessarily reflect the exact number of pads present or their electrical connections,” and, “even though ‘power supply pads’ 3, 4, and 58 are shown next to the ground rail, a POSITA would have understood they are connected to the power rails 17, 18, and 59 (shown in Figs. 1–4) and not ground rails 19, 20 and 60, as doing so would create a short circuit between power and ground.” *Id.* (citing Ex. 1003 ¶ 136). Accordingly, Petitioner contends, “a POSITA would have understood the reference pads (*e.g.*, pads 5 and 6) were connected to ground rails 19, 20, and 60” and “the pads labelled 3, 4, and 58 could just as readily be used as reference pads, and selecting which pads to use for ground, power, signals, etc. is a design choice that depends on factors like chip size,

the number of I/O signals, and the number of pads available.” *Id.* (citing Ex. 1003 ¶¶ 137–139).

Petitioner then contends that “a POSITA would have understood, or at least found it obvious, to use the pads immediately next to the saved areas as reference pads (*e.g.*, pads 5 and 6) as pad assignments were left to the designer’s discretion” in order “to preserve Yoshinaga’s saved area for other circuitry as taught by Saint.” Pet. 31–32 (citing Ex. 1003 ¶¶ 137–139; Pet. 19–23 (§ IX.A)). Petitioner alters the labels on its annotated version of Yoshinaga’s Figure 6 to illustrate its contentions; reproduced below is Petitioner’s annotated version of Figure 6 before Petitioner’s alteration (left) and after (right).



Annotated Figure 6, on the left, maintains the labels provided in Yoshinaga, and altered annotated Figure 6, on the right, (a) changes the label on the pad (blue) to the left of the saved area (orange) at the top of the chip from “3” to “5”, (b) removes the “4” label from the pad (blue) to the right of the saved area (orange) at the top of the chip, (c) labels the pad (blue) immediately to the right of the saved area (orange) at the top of the chip “6”, (d) changes the label on the pad (blue) above the saved area (orange) on the right side of the

chip from “4” to “6”, and (e) changes the label on the pad (blue) below the saved area (orange) on the right side of the chip from “58” to “Circuit 67 GND.” Pet. 29, 31–32; Ex. 1006, Fig. 6. Referring to altered annotated Figure 6 and Yoshinaga’s Figure 2, Petitioner concludes that “Yoshinaga discloses a plurality of pad groups (*e.g.*, pads in Fig. 6 corresponding to voltage reference pads 5, 6, 39, and/or 40) connected to the plurality of ESD buses (*e.g.*, reference lines 19, 20, and 60, each with wiring resistors 21, 22, 23, and 24).” Pet. 34 (citing Ex. 1006 ¶¶ 35, 36, 53–62, 88, Fig. 2; Ex. 1003 ¶ 143) (emphases omitted).

Patent Owner responds that “Petitioner’s assertion that power supply pads 3 and 4 ‘could’ be used as ‘reference potential pads’ is insufficient to establish that a POSITA ‘would have’ been motivated to change Yoshinaga’s power supply pads into reference potential pads.” Prelim. Resp. 10–11 (emphases omitted). Patent Owner argues that Petitioner does not identify any advantages resulting from changing the power supply pads to reference potential pads or any problems making such a change would solve. *Id.* at 11. Patent Owner argues that Petitioner also fails to explain how changing Yoshinaga’s power supply pads 3, 4, and 58 to reference potential pads would work, as power supply pads and reference potential pads “are connected to different circuit elements and serve entirely different purposes.” *Id.* at 11–12 (citing Ex. 2007 ¶¶ 39, 41–42). Patent Owner further asserts that “Petitioner provides no evidence that a POSITA would have had a reasonable expectation of success in changing Yoshinaga’s power supply pads to reference potential pads—especially where Saint further recognizes that the ‘choice of pin out’ affects ‘parasitics’ and ‘complexity’ of the design,” and “Petitioner does not even explain where the

power supply pads would be moved to if they are replaced with reference potential pads.” *Id.* at 14 (citing Ex. 1008, 144–145; Ex. 2007 ¶¶ 43–44).

On this record, we are persuaded that Petitioner sufficiently establishes that the combination of Yoshinaga and Saint teaches “a plurality of pad groups, adjacent and connected to the plurality of ESD buses” as recited in claim 6. Yoshinaga describes an integrated circuit that includes power supply pads and reference potential pads. Ex. 1006 ¶¶ 4, 78, Figs. 1–4, 6. Dr. Foty credibly testifies that a POSITA would have understood that reference pads 5 and 6 shown in Yoshinaga’s Figures 1–4 are connected to ground rails 19, 20, and 60, whereas power supply pads 3, 4, and 58 shown in Yoshinaga’s Figure 6 are connected to power rails 17, 18, and 59. Ex. 1003 ¶¶ 136–137, 152; *see* Ex. 1007, Fig. 1 (showing pads 5 and 6 connected to rails 19 and 20, respectively, and pads 3 and 4 connected to rails 17 and 18, respectively).

Dr. Foty further testifies that that

[t]he choice of selecting which pads to assign for ground, power, signals, etc. is left to the discretion of the designer—and may depend on factors such as the size of the chip, whether the chip is pad-limited or core-limited, the number of I/O signals, and the number of available pads; however, there is no inherent restriction on how pads may be assigned.

Id. ¶ 137. Dr. Foty’s testimony in this regard is consistent with Saint, which teaches that the quality of the pin-out (also called the pad-out) “directly affects how good [the] chip floorplan will be and how easy the chip will be to lay out,” and a “simple pin placement decision dictates” how to run the power wires. Ex. 1008, 158–160 (emphasis omitted); *see also id.* at 160–163 (discussing pin placement with respect to ESD protection). Saint further teaches that “[a] good choice of pin-out could reduce parasitics and help the

mask designer produce a clean layout.” *Id.* at 160; *see also id.* at 163 (explaining that the example shown in Figures 7-3 through 7-7 demonstrates “that the pin-out decisions directly affect not only the layout of the chip, but the size and quality of the end product as well”). There is no dispute, on this record, that a POSITA would know how to select and place the pads used for each function. *See* § II.A, *supra* (a POSITA would have been aware of and generally knowledgeable about integrated circuit design and layout).

We considered Patent Owner’s arguments and find them unavailing at this stage of the proceeding. For example, Patent Owner argues that “a POSITA would not have had a reasonable expectation of success in changing power supply pads to reference potential pads” because, “[a]s the Saint textbook recognizes ‘[y]ou cannot just blindly put your input/output pads wherever you feel like it’ and there are ‘rules and guidelines’ that must be followed.” Prelim. Resp. 13 (citing Ex. 1008, 201) (alteration in original). Patent Owner argues that “a POSITA would understand that pads are not ‘largely fungible’ as Petitioner alleges.” *Id.* (citing Ex. 2007 ¶¶ 39–40).

At this stage of the proceeding, Petitioner, with supporting testimony from Dr. Foty, provides adequate reasons why using the pads immediately next to the saved areas in Yoshinaga’s Figure 6 as reference pads would have been a “predictable use of prior art elements according to their established functions.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007); *see* Pet. 30–34 (and evidence cited therein). We acknowledge that Patent Owner disagrees, but find that Patent Owner’s disagreement raises issues of fact that are best resolved on a full trial record.

For these reasons, and based on the record before us, we are persuaded that Petitioner establishes a reasonable likelihood of showing that

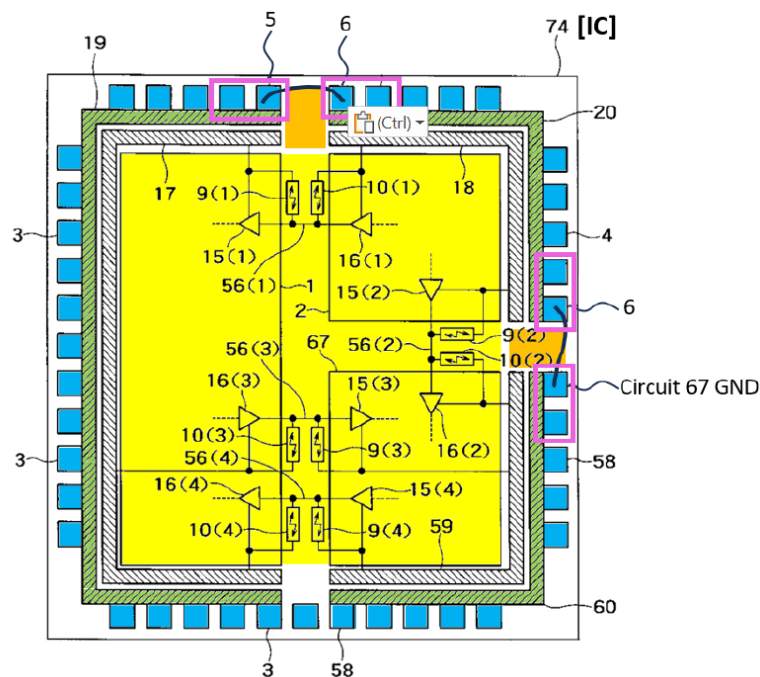
the combination of Yoshinaga and Saint discloses “a plurality of pad groups, adjacent and connected to the plurality of ESD buses.”

b) *“a plurality of bonding wires configured to connect one to another of the plurality of pad groups”*

With respect to “a plurality of bonding wires configured to connect one to another of the plurality of pad groups” limitation of claim 6, Petitioner contends that “Yoshinaga discloses that ‘[c]ircuits having separated power supply lines are not usually completely separated from each other, and one of multiple potential (ground) lines is used as a main ESD discharge path, and multiple reference potential lines are connected to each other.’” Pet. 34 (citing Ex. 1006 ¶ 5) (alteration in original). Petitioner asserts that Yoshinaga’s Figure 2 shows reference lines 19 and 20 are electrically connected, and contends that a POSITA would have understood that reference potential lines 19, 20, and 60 in Yoshinaga’s Figure 6 are connected. *Id.* at 35 (citing Ex. 1003 ¶¶ 130, 152). Petitioner further asserts that Yoshinaga does not describe the mechanism used to connect the reference potential lines, and contends that “[a]n obvious way” to do so “is by wire bonding the pads connected to the respective buses.” *Id.* (citing Pet. 12–14 (§ V), 48–52 (§ X.E); Ex. 1003 ¶¶ 149–154).

In that regard, Petitioner asserts that “Saint discloses ‘[w]ire bonding is the most common method of attaching a chip to a package’ and ‘bond wires’ connect to ‘bond pads on the chip.’” Pet. 38 (citing Ex. 1008, 202–204, 207) (internal citations omitted, alteration in original). Petitioner contends that “[a] POSITA would have turned to Saint and been motivated to use Saint’s bond wire teachings (and a POSITA’s knowledge) because bond wires were considered the ‘most common method of attaching a chip

to a package” and “a POSITA would have understood pad-to-pad bond wire connections were common.” *Id.* at 50 (citing Ex. 1008, 207; Ex. 1014,⁵ code (57), Figs. 7, 10, 13; Ex. 1015,⁶ 6:67–7:7; Ex. 1016⁷ ¶¶ 7, 27–30, 34–36, Figs. 4–6; Ex. 1003 ¶¶ 104–107). Petitioner contends that a POSITA would have had a reasonable expectation of success in using bond wires in Yoshinaga because “[t]he manufacturing techniques to connect pads with wire bonding were well-known and routine to implement.” *Id.* at 38 (citing Ex. 1015, code (57), Fig. 2, 6:67–7:7; Ex. 1016 ¶¶ 7, 27–30, 34–36, Figs. 4–6; Ex. 1003 ¶¶ 46–51, 154). Petitioner further annotates altered annotated Figure 6 of Yoshinaga, reproduced below, to illustrate its contentions.



To altered annotated Figure 6 Petitioner further adds purple boxes around the two pads (blue) to the right and left (and above and below) the saved areas (orange), a black line representing a bonding wire connecting pad 5 to

⁵ Miller, US 2004/0140860 A1, published July 22, 2004 (Ex. 1014).

⁶ Mathew, US 7,880,310 B2, issued Feb. 1, 2011 (Ex. 1015).

⁷ Beauchamp, US 2007/0215994 A1, published Sept. 20, 2007 (Ex. 1016).

pad 6 at the top of the chip, and a black line representing a bonding wire connecting pad 6 to pad Circuit 67 GND on the right side of the chip. *Id.* at 36; Ex. 1006, Fig. 6.

Patent Owner counters that “Yoshinaga expressly discloses that ‘[t]he reference potential lines *may be connected by bidirectional diodes* that are connected in parallel to one another in the opposite direction to avoid noise.” Prelim. Resp. 14–15 (citing Ex. 1006 ¶ 5; Ex. 2007 ¶¶ 45–46) (alteration in original). Patent Owner argues that “Petitioner does not identify any advantages with using bond wires over bidirectional diodes or any drawbacks with the use of bidirectional diodes that bond wires would solve.” *Id.* at 15 (citing Ex. 2007 ¶ 46). Patent Owner further argues that Saint “would discourage POSITAs from using bond wires between pads 5 and 6 and circuit 57 GND” because “Saint teaches that bond wires should only be used where there is ‘minimal silicon overlap.’” *Id.* at 16 (citing Ex. 1008, 209; Ex. 2007 ¶¶ 47–48). Therefore, according to Patent Owner, “a POSITA would be discouraged from deliberately forming the bond wire to overlap entirely with ‘unused silicon’ (the alleged ‘saved areas’ shown in orange) as Petitioner proposes.” *Id.* at 17 (citing Ex. 2007 ¶¶ 47–48).

On this record, we are persuaded that Petitioner sufficiently establishes that the combination of Yoshinaga and Saint teaches “a plurality of bonding wires configured to connect one to another of the plurality of pad groups” as recited in claim 6. At this stage of the proceeding, the record sufficiently establishes that using bond wires was well known in the art. *See* Pet. 36–38; Prelim. Resp. 16; *see also* Ex. 1008, 207 (“Wire bonding is the most common method of attaching a chip to a package.”); Ex. 1014, code (57) (“The contact pads are linked to one another and to the IC I/O terminal through inductive conductors such as bond wires”); Ex. 1015, 7:4–7

(wires “bonded to conductive elements 40 may carry power and ground signals,” and some wires “are used to directly connect two conductive elements 40”); Ex. 1016 ¶ 7 (“A single wire may be ball or wedge (stitch) bonded between one or more die bond pads and one or more inner leads of a leadframe, and/or between a plurality of bond pads to create a common connection therebetween.”).

We acknowledge that Yoshinaga states:

Circuits having separated power supply lines are not usually completely separated from each other, and one of multiple reference potential lines is used as a main ESD discharge path, and multiple reference potential lines are connected to each other. The reference potential lines may be connected by bidirectional diodes that are connected in parallel to one another in the opposite direction to avoid noise.

Ex. 1006 ¶ 5. This statement, which appears in the “Background art” section of Yoshinaga, identifies bidirectional diodes as one way to connect reference potential lines, but we are not directed to any teaching in Yoshinaga that requires using such bidirectional diodes in the integrated circuit chip shown in Yoshinaga’s Figure 6. Indeed, Yoshinaga teaches that Figure 6 includes the semiconductor integrated circuit shown in Figure 1, which does not show a bidirectional diode connecting reference lines 19 and 20. *Id.* ¶ 74; *compare id.* ¶¶ 58, 61, Fig. 3 (illustrating bidirectional diode chains 33 and 34, bidirectional diode pairs 37 and 38) *with id.* at Fig. 1 (absence of bidirectional diodes). This at least suggests that Yoshinaga does not teach using bidirectional diodes to connect the reference lines in the integrated circuit in Figure 6. *See* Pet. 50 (“But Yoshinaga does not teach *how* to connect the pads.”). Accordingly, we credit Dr. Foty’s testimony that “a POSITA would have been motivated to combine the well-known use of wiring bonding technique to provide inter-pad (and inter-trace)

connections[] with Saint’s extensive detailed discussions of generalized techniques for using wire bonding to connect bondpads to package traces—and to combine those techniques with Yoshinaga.” Ex. 1003 ¶ 108; *see id.* ¶¶ 102–107.

We considered Patent Owner’s arguments and find them unavailing at this stage of the proceeding. For example, we disagree with Patent Owner that Saint would have discouraged a POSITA from using bonding wires as Petitioner proposes. Prelim. Resp. 16–17. Saint teaches that, when the end pad is not in the corner of the chip, the bond wire overlaps “too much of the silicon,” and “the bond wire could sag or droop, causing a short in the circuit.” Ex. 1008, 209. Saint goes on to teach that the overlap of the bond wire over unused silicon should be kept “as short as possible” and bond wires length should also be as short as possible. *Id.* at 209–210. The bond wire that Petitioner proposes to connect the references pads on each side of the saved areas in Yoshinaga’s Figure 6 would span a very small amount of saved area and would be very short. *See* Pet. 35–36. Moreover, Petitioner notes that Saint teaches that parts of the circuit elements can be re-laid in and around the saved area in an attempt “to get the chip as small as possible,” which would also minimize the amount of unused silicon with which the bond wire would overlap. *Id.* at 40–41 (citing Ex. 1008, 220–221, Fig. 9-28).

c) Other Limitations

At this stage of the proceeding, Patent Owner does not address Petitioner’s specific contentions with respect to the other limitations of claim 6. We reviewed Petitioner’s contentions for all the elements of independent claim 6, as well as the supporting evidence. Pet. 27–41. Based on the record before us, we are persuaded that Petitioner’s discussion of the

particular structures and methods in Yoshinaga and Saint, and the explanations in the Foty Declaration, establishes a reasonable likelihood that the combined teachings of Yoshinaga and Saint disclose or suggest all of the limitations of independent claim 6. *Id.*

4. *Claims 7, 12, and 14*

Petitioner also contends that the combined teachings of Yoshinaga and Saint disclose or suggest all of the limitations of claim 7, which depends from claim 6, independent claim 12, and claim 14, which depends from claim 12. Pet. 43–48. At this stage of the proceeding, Patent Owner does not address Petitioner’s specific contentions with respect to the limitations of claims 6, 12, and 14. *See Prelim. Resp.* We reviewed Petitioner’s contentions for all the elements of claims 7, 12, and 14, as well as the supporting evidence. Pet. 43–48. Based on the record before us, we are persuaded that Petitioner’s discussion of the particular structures and methods in Yoshinaga and Saint, and the explanations in the Foty Declaration, establishes a reasonable likelihood that the combined teachings of Yoshinaga and Saint disclose or suggest all of the limitations of claims 7, 12, and 14. *Id.*

5. *Conclusion*

Based on the current record, and for the reasons set forth above, we determine that Petitioner establishes a reasonable likelihood of showing that claims 6, 7, 12, and 14 would have been obvious over the combined teachings of Yoshinaga and Saint.

D. Ground 2: Asserted Obviousness over Yoshinaga, Saint, and Haralabidis

Petitioner contends that claims 1–6, 8–11, and 13 would have been obvious over the combined teachings of Yoshinaga, Saint, and Haralabidis. Pet. 52–67.

1. Haralabidis

Haralabidis “is directed to an electronic device with electrostatic discharge (ESD) and interference suppression.” Ex. 1007, 1:16–18. Haralabidis teaches that “[t]he ESD configuration can be used in integrated circuits configured for system-on-chip (SoC) and system-in-package (SiP) implementations,” and that “electronic interference from both internal and external sources is reduced with respect to the integrated circuits included in the SoC and SiP implementations.” *Id.* at 1:35–41.

Figure 3 is reproduced below.

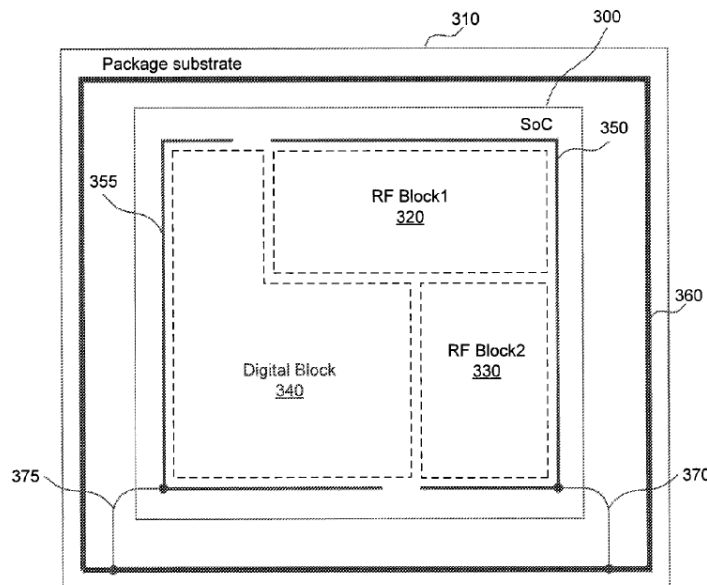


FIG. 3
Conventional Art

Figure 3 illustrates conventional SoC 300 encapsulated in package substrate 310. Ex. 1007, 2:13–14, 3:9–10. SoC 300 includes RF

block1 320, RF block2 330, digital block 340, segmented ground rails 350 and 355, and common groundrail 360. *Id.* at 3:11–15. Segmented ground rails 350 and 355 are independently connected to common ground rail 360 via separate connections 370 and 375, respectively. *Id.* at 3:15–18.

Haralabidis teaches that segmented ground rails 350 and 355 minimize interference from a noisy aggressor block to other blocks on the SoC. *Id.* at 3:19–21. For example, Haralabidis explains that known noisy aggressor blocks like digital block 340 are connected to segmented ground rail 355, and are thereby isolated from another block like RF block1 or RF block2, which are susceptible to noise/interference and are connected to segmented ground rail 350. *Id.* at 3:21–26.

Figure 5 is reproduced below.

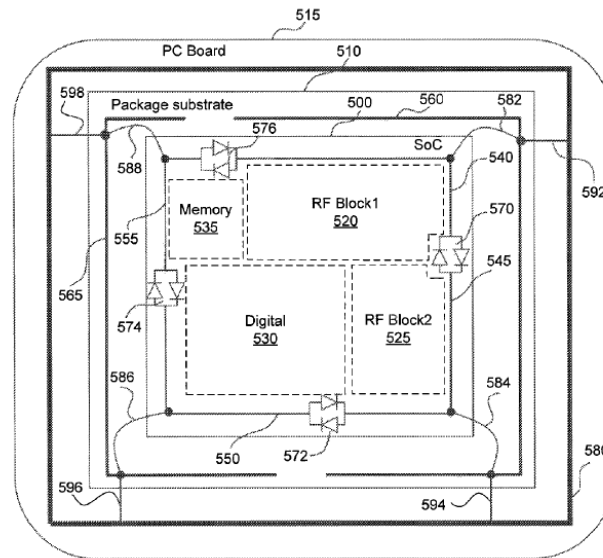


FIG. 5

Figure 5 illustrates an exemplary SoC according to an embodiment described in Haralabidis. Ex. 1007, 2:17–18. SoC 500 is encapsulated in package substrate 510, which is placed on and/or connected to printed circuit (PC) board 515. *Id.* at 3:65–4:2. Soc 500 includes RF block1 520, RF block2 525, digital block 530, memory block 535, and segmented ground

rails 540, 545, 550, and 555 that are connected to the respective ground node of RF block1 520, RF block2 525, digital block 530, and memory block 535. *Id.* at 4:2–6. Segmented ground rails 540, 545, 550, and 555 are connected to each other via anti-parallel diodes 570, 572, 574, and 576, and are also connected to segmented package ground rails 560 and 565 through connections 582, 584, 586, and 588, respectively. *Id.* at 4:13–17.

Segmented package ground rails 560 and 565 are connected to PC board common ground rail 580 through connections 592, 594, 596, and 598. *Id.* at 4:17–20. Haralabidis explains that “[t]he assembly, including the SoC 500 and package substrate, with or without the PC board may be referred to as an IC assembly, or electronic device, as will be understood by those skilled in the arts.” *Id.* at 4:23–26.

2. *Claim 1*

Petitioner contends that “most of the elements of claims 1 and 6 are identical and are satisfied for the same reasons.” Pet. 55 (citing Ex. 1003 ¶¶ 242–247, 256–257). Petitioner contends that the combination of Yoshinaga and Haralabidis teaches the “a common ESD bus, adjacent to the plurality of pad groups” limitation of claim 1, and that the combination of Yoshinaga, Saint, and Haralabidis teaches the “a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus” limitation of claim 1. *Id.* at 55–58. Patent Owner relies on the arguments it made with respect to Ground 1 to argue that a POSITA would not have been motivated to replace Yoshinaga’s power supply pads with reference potential pads with a reasonable expectation of success. Prelim. Resp. 20–21. As it also did in Ground 1, Patent Owner argues that a POSITA would not have been motivated to connect a plurality of pad groups to a common ESD bus with bond wires because Yoshinaga teaches using bidirectional

diodes to connect reference lines. *Id.* at 21–24. At this stage of the proceeding, Patent Owner does not address Petitioner’s specific contentions with respect to the other limitations of claim 1.

We reviewed Petitioner’s contentions for all the elements of independent claim 1, as well as the supporting evidence. Pet. 55–58. Based on the record before us, we are persuaded that Petitioner’s discussion of the particular structures and methods in Yoshinaga, Saint, and Haralabidis, and the explanations in the Foty Declaration, establishes a reasonable likelihood that the combined teachings of Yoshinaga, Saint and Haralabidis disclose or suggest all of the limitations of independent claim 1. *Id.* We considered Patent Owner’s arguments and find them unavailing at this stage of the proceeding for the reasons set forth above with respect to claim 6 in Ground 1. *See* § II.C.3, *supra*.

3. *Claims 2–6, 8–11, and 13*

Petitioner also contends that the combined teachings of Yoshinaga and Saint disclose or suggest all of the limitations of claim 2–5 that depend from claim 1, independent claim 6, independent claim 8, claims 9–11 that depend from claim 8, and claim 13 that depends from claim 12. Pet. 52–55, 59–65. At this stage of the proceeding, Patent Owner does not address Petitioner’s specific contentions with respect to the limitations of claims 2–6, 8–11, and 13. *See* Prelim. Resp. We reviewed Petitioner’s contentions for all the elements of claims 2–6, 8–11, and 13, as well as the supporting evidence. Pet. 52–55, 59–65. Based on the record before us, we are persuaded that Petitioner’s discussion of the particular structures and methods in Yoshinaga, Saint and Haralabidis, and the explanations in the Foty Declaration, establishes a reasonable likelihood that the combined

teachings of Yoshinaga, Saint, and Haralabidis discloses or suggests all of the limitations of claims 2–6, 8–11, and 13. *Id.*

E. Ground 3: Asserted Obviousness over Saint and Haralabidis

Petitioner contends that claims 1–14 would have been obvious over the combined teachings of Saint and Haralabidis. Pet. 68–99. Having already determined that Petitioner establishes a reasonable likelihood of establishing that claims 1–14 would have been obvious over Yoshinaga and Saint or Yoshinaga, Saint, and Haralabidis, we need not address this ground in full. We offer the following comments in response to the parties’ arguments and evidence to provide guidance to the parties.

1. Claim 1

Petitioner contends that Saint discloses the claimed “a plurality of ESD buses” because it “discloses three GND (known as ground or reference voltage) buses shown in blue in Figure 7-7,” which is reproduced below. Pet. 70 (citing Ex. 1008, 162).

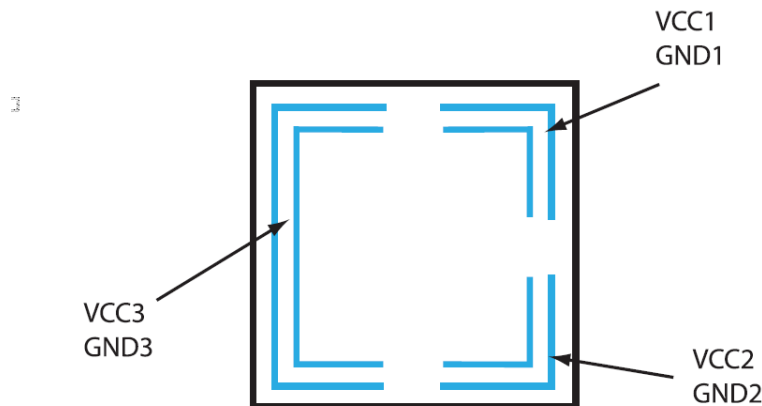


Figure 7-7. Pin-out simplification showing like protects grouped together.

Figure 7-7 is a simplified floorplan depicting power supply voltages VCC1, VCC2, and VCC3, and ground voltages GND1, GND2, and GND3.

Ex. 1008, 162. Petitioner contends that “a POSITA would have understood

that Saint's GND (and VCC) buses are 'ESD buses' because they serve as ground and power supply buses, respectively, and further because Saint explicitly discloses ESD protection connected to these buses." Pet. 71 (citing Ex. 1008, 160–164; Ex. 1003 ¶¶ 350, 59).

Patent Owner responds that Petitioner does not establish that Saint's Figure 7-7 illustrates ESD buses. Prelim. Resp. 25. Patent Owner asserts that Saint describes Figure 7-7 as "a 'simplification' to show discrete 'pins' that are 'located close to each other.'" *Id.* (citing Ex. 1008, 160–162). Referring to Saint's Figure 7-6, Patent Owner argues that "Saint teaches taking pins that correspond to the same ground, such as 'pins 1, 5, 7, and 9' which are all GND1, and 'mov[ing] them close to each other,'" and "do[ing] the same for the other supply pin sets' so that the pins corresponding to GND1, GND2, and GND3 are all 'located close to each other.'" *Id.* (citing Ex. 1008, 162) (alterations in original). Patent Owner argues that "Petitioner provides no reason why a POSITA would understand that Saint's disclosure of pins 'grouped close to each other' to be 'ESD buses' or 'traces,'" and asserts that "Saint discusses '[b]uses' in other sections, separate from its discussion of pin layouts." *Id.* at 26 (citing Ex. 1008, 180, 289, 322, 333, 379) (alteration in original).

On this record, we disagree with Patent Owner. Saint explains that pins 1, 5, 7, 9 are grouped together and protected to VCC1 and GND1, pins 6, 8, 10, and 14 are grouped together and protected to VCC2 and GND2, and pins 2–4, 11–13, 15, and 16 are grouped together and protected to VCC3 and GND3. Ex. 1008, 160–162. This is illustrated in Saint's Figures 7-3 through 7-5, reproduced below.

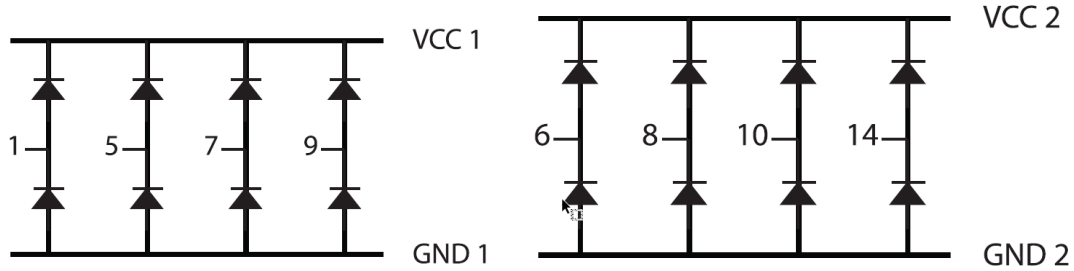


Figure 7-3. Pins 1, 5, 7, and 9 protected to VCC1 and GND1.

Figure 7-4. Pins 6, 8, 10, and 14 protected to VCC2 and GND2.

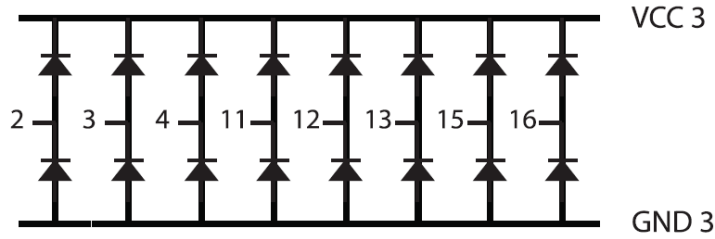


Figure 7-5. The remaining pins protected to VCC3 and GND3.

Id. at 160–161. Saint’s Figures 7-3, 7-4, and 7-5 show diodes providing ESD protection between each pin and the VCC and GND lines. *Id.*; *see also* Ex. 1003 ¶ 347 (Dr. Foty testifying “[t]hat Saint depicts the usage of the power supply and ground rails for the shunting of the energy of an ESD event is confirmed via Figure 7-3 (on p. 160).”).

Dr. Foty explains that “this type of dual-diode structure is the commonly-used circuit inclusion to provide ESD protection.” Ex. 1003 ¶ 347; *see also id.* ¶ 57 (Dr. Foty testifying that “[a] simple and commonly-known ESD protection addition to a circuit involves the use of two diodes, configured to cause the shunting described above to occur.”). Dr. Foty further explains:

ESD protection is added to the circuitry connected to a particular signal pin, the added ESD protection circuitry protects the circuitry directly associated with that particular signal pin, and the method-of-protection is to shunt the energy (e.g., current) to a ground or power supply rail.

Adding ESD protection onto the voltage supply and ground lines is a common way to address ESD concerns. Some

people may refer to this as an ESD bus but it's nothing special, it's just some power or ground line that has ESD protection associated with/attached to it.

Id. ¶¶ 58–59. Dr. Foty, therefore, provides an explanation as to why a POSITA would understand that Saint discloses the claimed “a plurality of ESD buses.”

Patent Owner also argues that Petitioner does not establish that Saint and Haralabidis teach “a common ESD bus, adjacent to the plurality of pad groups” as recited in claim 1 or “connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires” as recited in claim 8. Prelim. Resp. 27–31.

In that regard, Petitioner asserts that “Saint discloses ‘ESD Ground Wiring’ that ‘creates a continuous ring around the active circuitry’ to which ESD diodes are connected,” and “Haralabidis discloses that it was common practice to place ‘package common ground rail 360’ around an IC” to connect “‘segmented . . . ground rails 350, 355’ via connections 370 and 374.” Pet. 74–76 (citing Ex. 1008, 344, Fig. CS1-99; Ex. 1007, 3:9–18, Fig. 3). Petitioner provides an annotated version of Saint’s Figure 7-7, reproduced below, to illustrate its contentions.

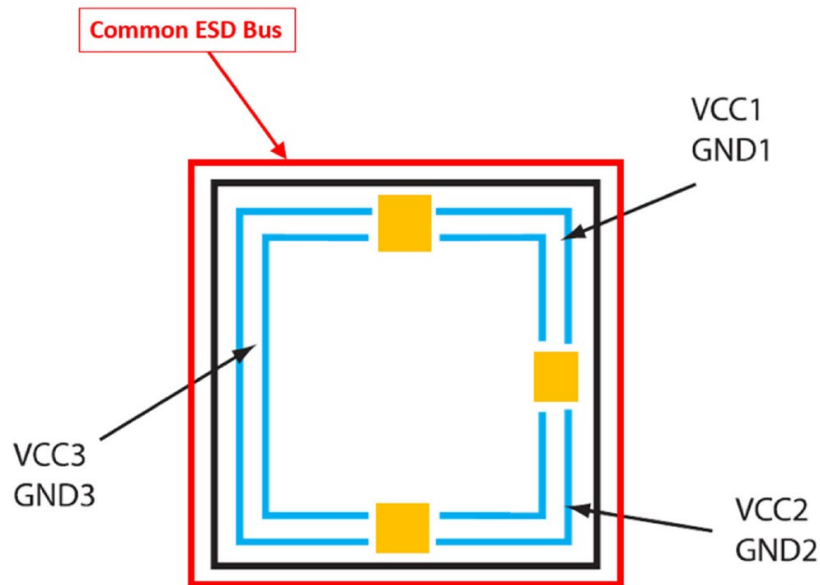


Figure 7-7. Pin-out simplification showing like protects grouped together.

Petitioner's annotations to Figure 7-7 include the addition of a red box labelled "Common ESD bus" around the entire package, and the addition of orange shading in the spaces between the ends of GND1 and GND2 (right side), GND2 and GND3 (bottom), and GND3 and GND 1 (top). Pet. 77 (citing Ex. 1008, 162, Fig. 7-7; Ex. 1003 ¶ 368). Petitioner contends that, as the "conceptual implementation" depicted in annotated Figure 7-7 shows, "[a]pplying either Saint's 'ESD Ground Wiring' or Haralabidis' common ground rail teachings results in a common ESD bus[] [red box] adjacent to the plurality of ESD buses [blue segments] and the plurality of pad groups [not shown but present as explained previously]." *Id.* at 76–77 (citing Ex. 1003 ¶¶ 356–367) (second to fourth alterations in original). According to Petitioner, "[t]he common rail allows circuits to source the reference voltage from the same line, so the PCB (or other external circuitry) need only feed the common line which propagates the reference voltage to all appropriate internal IC circuits." *Id.* at 77–78 (citing Ex. 1003 ¶ 368).

Patent Owner argues that “Petitioner ignores that Saint’s Figure 7-7 teaches the use of three separate and distinct ground signals—GND1, GND2, and GND3—and that Saint does not contemplate, teach, or suggest shorting them together as Petitioner proposes with its ‘common ESD bus’ shown above.” Prelim. Resp. 27 (citing Ex. 1008, 160–163; Ex. 2007 ¶¶ 55–57). Patent Owner argues that “a POSITA would understand that three separate signals GND1, GND2, and G[ND]3 should *not* be connected together as Petitioner proposes.” *Id.* at 28 (citing Ex. 2007 ¶¶ 58–59). Patent Owner further argues that Saint’s Case Study 1, upon which Petitioner relies to support its contentions, includes only one GND signal and, “[a]s a result, Saint teaches that a single ‘continuous ring’ can be used as an ‘ESD Ground Wiring’ for that case study design with a single GND.” *Id.* (citing Ex. 1008, 344; Ex. 2007 ¶ 60). Patent Owner argues that connecting Saint’s three separate ground signals to a common ESD bus “would result in drastically changed electrical characteristics of the design and would require additional design changes that Petitioner ignores.” *Id.* at 29 (citing Ex. 2007 ¶ 61). Patent Owner also argues that “Haralabidis does not disclose or suggest using a ‘common ground rail’ to connect together three different and separate ground signals, such as those explicitly shown in Figure 7–7 of Saint as Petitioner proposes.” *Id.* (citing Ex. 2007 ¶ 62). Patent Owner argues that “[a] POSITA would understand Haralabidis’ teachings of ‘common ground rail’ are simply inapplicable to (and incompatible with) a design like Figure 7-7 with different ground signals/reference potentials, expressly labeled GND1, GND2, and GND3.” *Id.* at 29–30 (citing Ex. 2007 ¶ 62).

We find Patent Owner’s arguments in this regard have merit on this record. As Patent Owner notes, Saint’s Case Study 1 is directed to a design

with a single GND signal, and Haralabidis is directed to a single GND signal that is segmented into three different reference potentials; neither includes multiple, separate GND signals as shown in Saint’s Figure 7-7. Ex. 1008, 160–163, 344; Ex. 1007, 3:9–22, 3:34–40, 3:65–4:12; Ex. 1003 ¶¶ 359–360; Ex. 2007 ¶¶ 60, 62. In light of these disclosures in Saint and Haralabidis, we question whether a POSITA would have been motivated to apply Saint’s “ESD Ground Wiring” or Haralabidis’ common ground rail teachings to Saint’s Figure 7-7 with a reasonable expectation of success.

The parties are invited to develop these arguments further at trial, to the extent permitted under our rules.

F. Discretionary Denial under 35 U.S.C. § 314(a)

Under 35 U.S.C. § 314(a) we have discretion to deny institution of an *inter partes* review. *Cuozzo Speed Techs., LLC v. Lee*, 579 U.S. 261, 273–74 (2016). Petitioner argues against discretionary denial under 35 U.S.C. § 314(a). Pet. 11–14. Patent Owner argues that we should exercise our discretion under 35 U.S.C. § 314(a) and not institute trial. Prelim. Resp. 31–38. For the reasons set forth below, we do not exercise our discretion to deny institution in view of the parallel district court proceeding.

Institution of an *inter partes* review is discretionary. *See* 35 U.S.C. § 314(a) (authorizing institution of an *inter partes* review under particular circumstances, but not requiring institution under any circumstances); *Cuozzo*, 136 S. Ct. at 2140 (“[T]he agency’s decision to deny a petition is a matter committed to the Patent Office’s discretion.”); *SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1356 (2018) (“[Section] 314(a) invests the Director with discretion on the question whether to institute review” (emphasis omitted)); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir.

2016) (“[T]he PTO is permitted, but never compelled, to institute an IPR proceeding.”).

We consider several factors when determining whether to deny institution under § 314(a) based on a parallel district court proceeding, specifically

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board’s exercise of discretion, including the merits.

Apple Inc. v. Fintiv, Inc., IPR2020-00019, Paper 11 at 5–6 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”).

1. *Factor 1 – Whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted*

Under the first *Fintiv* factor, we consider “whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted.” *Fintiv* at 6.

In the Preliminary Response, Patent Owner represents that the parallel proceeding was temporarily stayed pending consideration of Petitioner’s motion for a stay in light of the filed *inter partes* review proceedings. Prelim. Resp. 31 (citing Ex. 2001; Ex. 2003). Subsequently, Patent Owner notified the Board that the parallel proceeding “was stayed pending

resolution of related IPR proceedings.” Paper 11, 1; *see also* Ex. 1030 (district court order granting motion to stay case). Accordingly, we determine that *Fintiv* factor 1 weighs strongly against exercising our authority to deny institution. *See Snap, Inc. v. SRK Technology, Inc.*, IPR2020-00820, Paper 15 at 9 (PTAB Oct. 21, 2020) (precedential) (“The granting of a stay pending *inter partes* review has weighed strongly against exercising discretion to deny institution under *NHK*.”)

2. *Factor 2 – The proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision*

Under the second *Fintiv* factor, we consider the “proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision.” *Fintiv* at 6.

Patent Owner asserts that trial in the parallel proceeding is scheduled for June 15, 2026, which “is three days after the statutory deadline for a Final Written Decision in this case (June 12, 2026).” Prelim. Resp. 33. Patent Owner asserts “[a] Final Written Decision here would issue after expert discovery, after dispositive motions, and after the pretrial conference.” *Id.* (citing Ex. 1021, 2). Patent Owner contends that “[t]his factor therefore favors denial of institution, or is at worst neutral.” *Id.* (citing *Fintiv* at 9). Petitioner argues that, there is no set trial date because the parallel proceeding is stayed, and a trial date will not “be set until after the completion of the IPR proceedings.” Prelim. Reply 2.

Because the parallel proceeding is stayed pending the resolution of the related IPR proceedings, any trial that occurs will happen well after the projected statutory deadline for a final written decision in this case. *See* Ex. 3001, 3 (“The parties shall file a joint status report every six months, and

shall notify the Court within 30 days of the completion of *all* IPR proceedings.” (emphasis added)). Accordingly, factor 2 weighs against exercising our authority to deny institution.

3. *Factor 3 – Investment in the parallel proceeding by the court and the parties*

Under the third *Fintiv* factor, we consider the “investment in the parallel proceeding by the court and the parties.” *Fintiv* at 6.

Patent Owner argues that the parties have expended “substantial resources into the Parallel Proceeding,” including propounding and responding to numerous interrogatories and requests for production, and Patent Owner “has narrowed its claims of infringement to 70 asserted claims, which has required extensive analysis of infringement, validity, and damages issues.” Prelim. Resp. 34 (citing Ex. 2002, 12). Patent Owner argues that, “[b]ecause the parties and the Court will expend significant effort in the parallel litigation *before institution*, this factor favors discretionary denial of institution.” *Id.* at 35. Petitioner contends that “[v]irtually no progress has been made related to the ’164 Patent.” Pet. 9. Petitioner also asserts that, “[i]n its order staying the case, the district court recognized that ‘the litigation is in an early stage.’” Prelim. Reply 2 (citing Ex. 1030, 1).

Although we recognize that the parties have invested some resources, much work remains to be done in the parallel proceeding. The parallel proceeding appears to be in an early stage, there is no evidence that the district court has issued any substantive orders related to the ’164 patent or the prior art set forth in the Petition, and the parallel proceeding was stayed as of March 14, 2025. *See* Ex. 1030, 1 (staying the parallel proceeding and noting that “the litigation is in an early stage” and “[c]laim construction

briefs have not yet been filed”). Thus, we determine that *Fintiv* factor 3 weighs slightly against exercising our authority to deny institution.

4. *Factor 4 – Overlap between issues raised in the petition and in the parallel proceeding*

Under the fourth *Fintiv* factor, we consider the “overlap between issues raised in the petition and in the parallel proceeding.” *Fintiv* at 6.

Petitioner states that, “[s]hould the Board institute, [Petitioner] stipulates that it will not advance in District Court any ground asserted in this Petition,” which “eliminates any potential overlap in issues between the proceedings here and in District Court.” Pet. 10.

Patent Owner asserts that Petitioner served invalidity contentions in the parallel proceeding “identifying the same art from its Petition, and explicitly incorporating its IPR petition by reference.” Prelim. Resp. 36. Patent Owner also asserts that although Petitioner offers a stipulation in the Petition, “no such stipulation has been made in the district court.” *Id.* (citing Pet. 10). In any event, Patent Owner argues, “[s]uch a narrow stipulation runs the risk of significant overlap both in consideration of the same evidence and arguments framed as ‘different grounds’ than the Petition.” *Id.*

Here, any potential overlap in issues is mitigated by the district court’s stay of the parallel proceeding pending resolution of the related IPR proceedings. *See* Ex. 1030, 2 (“The overlapping subject matter of these claims means that staying the case pending IPR will likely simplify infringement, validity, and claim construction issues in this case.”). Accordingly, we determine that *Fintiv* factor 4 weighs slightly against exercising our authority to deny institution.

5. *Factor 5 – Whether the petitioner and the defendant in the parallel proceeding are the same party*

Under the fifth *Fintiv* factor, we consider “whether the petitioner and the defendant in the parallel proceeding are the same party.” *Fintiv* at 6. In consideration of the fact that the parallel District Court proceeding is stayed, and that Petitioner’s stipulation reduces potential overlap between the invalidity contentions and the Petition challenges, we regard the consideration of the fifth *Fintiv* factor as neutral or, at most, weighing slightly in favor of exercising discretion to deny institution.

6. *Factor 6 – Other circumstances that impact the Board’s exercise of discretion, including the merits*

Under the sixth *Fintiv* factor, we consider “other circumstances that impact the Board’s exercise of discretion, including the merits.” *Fintiv* at 6. Petitioner contends this factor weighs against discretionary denial because the Petition “has significant substantive merit.” Pet. 10.

The parties disagree on the strength of the merits of the Petition. Pet. 10; Prelim. Resp. 37–38. As detailed above, we determine that the Petitioner meets its burden for institution for all challenged claims. *See* §§ II.C, II.D, *supra*. As noted, Petitioner’s case for Grounds 1 and 2 is not undermined by any facts or arguments on the current record. *Id.* §§ II.C.3–4, II.D.2–3. As such, on this record, factor 6 weighs against exercising our authority to deny institution.

7. *Conclusion – Fintiv*

Absent a compelling reason to the contrary, we take “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review” when evaluating the *Fintiv* factors. *Fintiv* at 6. Having evaluated all of the factors on this record, we determine that the

circumstances presented do not support exercising our discretion under § 314(a) to deny institution of this *inter partes* review.

III. CONCLUSION

Based on the arguments in the Petition, the Preliminary Response, the Preliminary Reply, and the Preliminary Sur-reply, and the evidence of record, we determine that Petitioner establishes a reasonable likelihood that it will prevail on its challenge to at least one claim of the '164 patent. We also determine that the arguments and evidence of record do not support discretionary denial of the Petition under 35 U.S.C. § 314(a). Accordingly, we institute an *inter partes* review of all the challenged claims on all the challenged grounds.

The factual findings set forth in this Decision are preliminary and provided for the sole purpose of deciding whether to institute a review. Any final findings will be based on the full trial record, including any information presented in a timely filed response to the Petition. *See Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1068 (Fed. Cir. 2016) (noting that “there is a significant difference between a petitioner’s burden to establish a ‘reasonable likelihood of success’ at institution, and actually proving invalidity by a preponderance of the evidence at trial”) (quoting 35 U.S.C. § 314(a); comparing *id.*, with § 316(e)).

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that an *inter partes* review is instituted with respect to all of the grounds asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this Decision.

IPR2025-00118
Patent 10,879,164 B2

FOR PETITIONER:

Jeremy Jason Lang
Travis Jensen
ORRICK, HERRINGTON & SUTCLIFFE LLP
ptabdocketjjl2@orrick.com
t61ptabdocket@orrick.com

FOR PATENT OWNER:

Inge A. Osman
Brenda L. Danek
Steven Peters
Amit Makker
LATHAM & WATKINS LLP
inge.osman@lw.com
brenda.danek@lw.com
speters@cgsh.com
amit.makker@lw.com