UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

_____

Case IPR2025-00118

Patent 10,879,164

_____

REMOTELY CONDUCTED DEPOSITION OF

DANIEL FOTY, PHD

WEDNESDAY, AUGUST 6, 2025

9:03 A.M. EDT

JOB NO.: 592768

PAGES: 1 - 266

REPORTED BY: KARISA EKENSEAIR, CCR RPR RMR RDR

**YMTC**
**Exhibit 2011**
**Micron v. YMTC**
**IPR2025-00118**
Ex. 2011-001

DEPOSITION OF DANIEL FOTY, PHD, CONDUCTED VIA ZOOM VIDEOCONFERENCE.

Pursuant to notice, before Karisa J. Ekenseair, Certified Shorthand Reporter in and for the States of Arkansas, Oklahoma, Missouri, Illinois, Tennessee, Georgia, New Mexico, Washington, and California; National Registered Professional Reporter; National Registered Merit Reporter; National Registered Diplomate Reporter; Notary Public.

A P P E A R A N C E S

ON BEHALF OF THE PETITIONER (VIA ZOOM):

SHANE ANDERSON, ESQUIRE
TRAVIS JENSEN, ESQUIRE
ORRICK, HERRINGTON & SUTCLIFFE LLP
1000 MARSH ROAD
MENLO PARK, CALIFORNIA 94025
650-614-7400

ON BEHALF OF THE PATENT OWNER (VIA ZOOM):

B. THOMAS WATSON, ESQUIRE
LATHAM & WATKINS LLP
12670 HIGH BLUFF DRIVE
SAN DIEGO, CALIFORNIA 92130
858-523-3944

ALSO PRESENT:

DAVID MIELCAREK, REMOTE TECHNICIAN

T A B L E O F C O N T E N T S

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P R O C E E D I N G S

THE REPORTER: Will counsel please stipulate that in lieu of formally swearing in the witness, the reporter will instead ask the witness to acknowledge that their testimony will be true under penalties of perjury, that counsel will not object to the admissibility of the transcript based on proceeding in this way and that the witness has verified that they are, in fact, DANIEL FOTY, PHD, beginning with the noticing attorney, please?

MR. WATSON: Yes.

MR. ANDERSON: Yes.

DANIEL FOTY, PHD

of lawful age, being first duly sworn, deposes and says in reply to the questions propounded as follows:

EXAMINATION

BY MR. WATSON:

Q Good morning, Dr. Foty.

A Good morning, Counselor.

Q Could you please state your full name for

the record?

A Daniel Patrick Foty.

Q And can you please state your home address for the record?

A 452 Black Mountain Road. The mailing address is Cambridge, Vermont. The physical location is Fletcher, Vermont because Fletcher does not have a post office. It's a Vermont thing.

Q And that's your home address, correct?

A Affirmative. This is my residence where I am today.

Q Okay. So right now you're located at your home; is that correct?

A That is correct, yes.

Q Okay. Have you been deposed before, Dr. Foty?

A Many, many times.

Q And in this case today, you are being deposed because you gave a declaration in an IPR proceeding, correct?

A That's my understanding, yes.

Q So I am going to go over some ground rules with you about deposition basics, just to refresh your memory, if that's okay with you?

A That's fine.

Q Okay. Do you understand that your testimony today is under oath and under penalty of perjury?

A I understand that. Yes.

Q And you understand that you are under the same obligation to tell the truth as if you are testifying before a judge and jury?

A I understand that. Yes.

Q Now, we have a court reporter with us here and it's important that she is able to transcribe your answers.

Do you understand that?

A Yes. And I'll do my best and I request if there's something that -- about my speech or my accent that's troubling the court reporter, to please advise me and I'll try to correct it as best I can.

Q Perfect. And can you try to provide

verbal answers to my questions as we go?

A That as per past experience is what I'll try to do.

Q All right. Now, if you do not understand one of my questions, please let me know so I can try to rephrase it. Okay?

A I will do so, yes.

Q Okay. And if you answer, I will assume that you understood my question; is that okay?

A That's fair. Yes.

Q Okay. Now, your attorney may state an objection to the form of some of my questions. But unless your attorney instructs you not to answer, you still need to answer the question.

Do you understand that?

A That's my understanding, yes.

Q And during the deposition, you are not to communicate with your counsel while we are on the record.

Do you understand that?

A I understand that, yes.

Q Do you understand that that includes

verbal, nonverbal cues, as well as electronic means?

A I understand that. Yes.

Q And is there any reason you cannot provide full and truthful testimony today?

A Not that I'm aware of, no.

Q Okay. When I refer to this case or this IPR, I want you to understand that I'm referring to IPR2025-00118. Okay?

A Yes. And that's in this covey of matters, this is the only one I have been working on so that should be implicit.

Q And just so we're on the same page, when I refer to the '164 patent, I am referring to U.S. Patent No. 10,879,164 that's at issue in this IPR. Okay?

A That's the patent number I have on the cover page of my declaration, so I assume that is -- agrees with yours.

Q Yes. Yes. So when I refer to the '164 patent, I'm referring to that patent that you discussed in your declaration; is that -- is that

fair?

A Yes. And again, the -- there's only one patent here that we're discussing so there's hopefully less room for confusion.

Q I will try to take breaks every hour, but if any time you need to take a break, don't hesitate to ask.

But all I would ask is that if a question is pending, you answer the question before we go on the break.

A I am not -- I am asking for breaks. If I need them -- but unless there's an emergency, I will ask for -- I will answer your question before we go to a break.

Q Dr. Foty, do you have any materials in front of you right now?

A What I have with me to make this easier is I have clean copies of my declaration, the exhibits, and things of that sort. They are just for the purpose of this deposition so they are completely clean. They have no marks on them.

I also have a little pad of sticky notes

which sometimes those -- they're blank. They're for use as bookmarks because if we get flipping around, you know what can happen.

And I also have -- actually have my -- a copy -- my copy of Saints' book which is, again, it's completely clean. The reason I have this -- I'll put it over on the windowsill. I also have the produced copy in printed form. It might be easier to thumb through the book rather than the binder. So I just have that here as an option.

Q So to be clear, you do not have any notes before you; is that fair?

A That is correct. For the deposition, I just have clean copies of everything.

Q And you don't -- you don't have a phone in front of you; is that correct?

A No, I do not. My mobile phone is off and my VoI -- voiceover IP landline is disconnected so we shouldn't be interrupted by that hopefully.

Q Do you have any other applications open on your computer besides this deposition video conference?

A I've just got the usual background and e-mail handler and some folders to look at photos and things like that. But I have nothing -- I have no interest -- I will not be consulting anything other than what you provide and what I have in paper form around my desk today.

Q Are there any screen -- other screens in the room you're in right now that are on?

A There's no screens that are on, just the one on my laptop.

Q Is there anyone else in the room with you?

A No. Just cats. They may make appearance, as you know.

Q Can you agree with me today to not take your cell phone out and look at it during the deposition today; is that fair?

A It's over on the stand by the back door and it's turned off so I have no need to look at it or use it unless, again, there's a fire breaks out or some emergency which I doubt will happen.

Q And so just to be clear, you'll agree with me that you won't look at your cell phone during

the deposition; is that fair?

A No, I won't. I won't even turn it on so that should cover it.

Q Will you also agree with me that you won't access the internet during this deposition?

A Only if -- again, if there's an emergency of some sort.

Q Okay. Other than an emergency which you'll inform me of, you will not be accessing the internet during this deposition; is that fair?

A Unfortunately, I can't just turn my internet access off or I will lose this, so I have to be connected to the fiber line and the Wi-Fi and all that, but that's all I'll be using it for.

Q Just to be clear, the reason I'm asking all these questions, of course, is to make sure that you're answering based on the documents and the exhibits you have and not any outside information, fair?

A That's understood. Again, I've done this before. And in the past five years, we've done plenty of the remote depositions and I understand

all those rules.

Q Now, you mention you've been deposed before.

How many times have you been deposed?

A I've been doing this for a while. I stopped counting at some point when it was in the 20s or 30s. I would say it's probably north of 70 times. It's hard to believe but that seems to be true. I didn't go count, but it's been an awful lot.

Q Have you ever been deposed in a case regarding -- regarding 3D NAND technology before?

MR. ANDERSON: Objection to scope.

A I don't believe that I have. And of course, this patent is not a 3D NAND technology patent.

Q Have you ever been deposed about the bonding wire in integrated circuits prior to this matter?

A I believe that I have, yes.

Q What matter would that have been?

A I believe there have been matters I've

worked on involving ESD that involve bond wiring as well. I've been doing this for so long I didn't go back and make a record, but bond requires are extremely commonly used for connecting ICs to packages, so they come up inherently in a lot of these matters.

MR. WATSON: Let's pull up if we could Exhibit 1004.

(Exhibit 1004 marked for identification.)

REMOTE TECHNICIAN: Please stand by.

Q Dr. Foty, this is Exhibit 1004 here on the screen.

Do you have that in front of you?

A I see that. And I have a paper copy in my big binder to my right which I was thumbing to if you need to go to anything.

Q In this Exhibit 1004, you have listed your litigation-related experience; is that correct?

A I believe that I do. Yes.

Q Okay. Could you just scan through those real quick and just identify which of those cases, if any, involve the use of bonding wire and

integrated circuits.

REMOTE TECHNICIAN: Counsel, also just to let you know, I can give control of the screen to either you or Dr. Foty if that's needed at any point.

MR. WATSON: Okay.

A I believe that the entire set of Microchip matters had some degree of bond wiring going on there.

And I'm looking back now. If you get more than five years back, it's hard to remember exactly what went on in these various matters and what pieces came up.

It's possible that a decade ago the Xicore versus SST matter might have had bond wires in it.

So those are just a few samples. And again, when -- since I worked in industry for a number of years, bond wires -- bond wires were inherent in the work that we did because you have to bond an IC to the -- you have to connect an IC to the package pad using bonding wires.

Q And just for clarity, when you refer to

the Microchip matters, you're referring to the various cases listed on your CV between a company called Aptiv v Microchip?

A Yes. There were two IPRs and there was a -- there's a district court matter which is still dragging on, as far as I know. I'd have to check that. I just know those involved a lot of very different things and that might have been an issue in there as well.

Q Okay. Okay. You can put that to the side.

MR. WATSON: We can take that off the screen.

A Let me just put it back in the binder.

Q Sure.

A I'm back.

Q So Dr. Foty, what did you do to prepare for today's deposition?

A I reviewed my -- my declaration. I reviewed the exhibits involved in the declaration, and I had a couple of meetings with counsel.

Q Who did you meet with at Campbell?

MR. ANDERSON: Objection, to the extent it calls for privileged information. You may answer, Daniel.

A I met with Mr. Anderson and Mr. Jensen a few times.

Q How long were those meetings?

A We maybe had three meetings, couple hours, a couple hours, an hour, things like that.

Q Okay. And when were those meetings?

A There was one two weeks ago, one last week, and there was -- actually, there was a fourth. There was one on Monday, and a small one yesterday.

Q And were those meetings in person or by video or by phone?

A They were by video, like our deposition is today.

Q Were any in-house lawyers from Micron present?

A Not that I'm aware of, no.

Q And was anyone who isn't a lawyer present at the meeting?

A Other than myself and maybe a visiting cat, no.

Q Besides the attorneys in this case, have you discussed this case with anyone else?

A Not to my recollection, no.

Q And when preparing to testify today, did you review any documents?

A Well, as I said a moment ago, I reviewed my declaration. I reviewed the exhibits, things of that sort in preparation for both the deposition and for the preparation for the preparation sessions.

Q Besides the exhibits to your declaration and your declaration, did you review any other documents?

A Not that I recall, no.

Q Okay. And did your review of those documents refresh your recollection?

A Given that we put this declaration in in, I think, it was mid-November last year, yes, it was necessary to refresh my recollection.

Q Since you signed your declaration that you

submitted in this IPR, have you changed any of your opinions?

A I don't believe I have.

Q And in preparing -- in preparation for the deposition today, did you review your declaration again?

A Yes, I did.

Q And other than your attorneys, did you discuss the substance of your declaration with anyone else?

A Just with counsel at Orrick.

Q Have you formed any new opinions regarding this IPR that are not currently listed in your declaration?

A I don't believe so. I believe that everything is in the declaration and stands as I filed it last November.

Q Okay. How much time have you put into this IPR so far?

A I have the -- most of the work was done last fall so I didn't go back and review my -- you know, my invoices or anything like that. But it

was fairly substantial. It was something in the 100-hour or more range. It was a nontrivial amount of time that I put in.

Q So around or more than 100 hours you -- sorry, strike that.

You spent more than -- around or more than 100 hours working on your declaration on -- on this IPR; is that fair?

A That's a rough guess. Of course, if we need to get the exact numbers or something closer, I'd have to go look at my invoices since again, most of that was almost a year ago.

Q Now, how much of that time did you spend preparing your declaration?

A Well, it depends how you define "prepare." If you mean physically typing words or just, you know, the entire process of learning and figuring things out.

So basically the entire time I was doing that, I was either studying the materials in order to reach conclusions and form opinions or I was actually typing the words and working from there

and creating figures and things like that.

Q Okay. Well, about how much time do you spend overall in preparing the declaration, including reviewing materials and typing the declaration out?

A Basically, the same answer as before. Since I -- basically that's what my task was for the time I was putting in, it would be similar to the 100 or 100-plus hours roughly. Again, if we need to get specific numbers, I have to go consult my invoices from last fall.

Q Okay. So you spent -- in preparing your declaration, you spent 100 or more hours reviewing materials in preparing the declaration; is that fair?

A That's a rough guess. As I said, if we need to go find the exact numbers, I can -- I could do that but I didn't review my invoices from last fall.

Q Who initially drafted the text of your declaration?

A I did.

MR. WATSON: Let's pull up his declaration. That's Exhibit 1003.

(Exhibit X marked for identification.)

A And I have a paper copy open to my left here.

MR. WATSON: Can I have control of the screen, please, or of the document?

REMOTE TECHNICIAN: Sure. Just a second. If you click on it first, it should give you control now.

Q Dr. Foty, is Exhibit 1003 the declaration you submitted in this IPR?

A The paper copy I have is and from what I see on the screen, so far this electronic copy appears to be identical to my declaration in a paper copy. So I would say, yes, this appears to be my declaration. And the document says it has 219 pages which seems to be correct.

Q Now, I'm going to take you down to paragraph 7 of your declaration. Can you tell me when you're there?

A Yes. I have paragraph 7 which is the --

mainly the list of materials considered.

Q In paragraph 7, you list 27 exhibits, correct?

A Actually, that's not correct because you'll note that there's some numbers which aren't used. Like, you'll note between -- there's no 1009 and 1010.

Q Fair, fair. But -- but the exhibits listed here in paragraph 7 are the exhibits that you relied on and reviewed in preparing your declaration; is that fair?

A That is correct. That's the complete sum of the materials I reviewed to reach conclusions and form opinions.

Q And did you review any documents not listed in paragraph 7 in preparing for your deposition?

A The only other documents would be there are a few things mentioned inline in the declaration and URLs are provided. For example, there's a 2010 -- 2010, excuse me, article that I cite and a figure from it. And that's in there,

so that -- that is listed inline.

Q Besides the 2010 article you referred to, are there any other materials or exhibits that are not listed in paragraph 7 that you relied on or reviewed in preparing your declaration?

A Only if there's -- there's some things listed inline which is mainly, you know, referring to figures and things of that sort. And those would all be footnoted with the URL to the link.

Q And so just to be clear, the materials listed here in paragraph 7 and then any materials that are included in footnotes of this declaration are the only materials you reviewed and relied upon in preparing your declaration for this matter; is that fair?

A That's fair. I used those to reach conclusions and form the opinions as discussed in this declaration.

Q Your declaration involves a number of references that are called prior art, correct?

A Yes. I believe we use that phrase in discussing this matter and I believe I use that

phrase in the -- in the declaration.

Q Who provided you with the prior art for your analysis?

A Some was provided by counsel; some was provided myself.

Q Looking at the exhibits here in paragraph 7, which of those exhibits did you provide?

MR. ANDERSON: Objection to the extent it calls for privileged information.

A I'll try to work through this sequentially. I was going to do it nonsequentially but it's better since there's several. I'll try to go through this in the number order to make this easier for you.

Reference 1008, the Saint book, I provided that.

Although it wasn't used, it's listed here on the reference list though it's not cited in the material, 1013, the Ker patent. I provided that although ended up not using it in the discussion at all.

And the last two 1026, which is a paper from a conference -- it's a paper regarding the ESD protection, I provided that and that had been an earlier matter. I'd had that available and I provided it there so that was already in my toolkit.

And the same with 1027, this is an excerpt from Uyemura's book is listed there. I provided that excerpt from that book as well.

Q So to summarize, you provided Exhibits 1008, 1013, 1026, and 1027; is that fair?

A That's fair. It's possible some of the other ones I may just -- I don't know how you'd say they're provided because, for example, if they're mentioned in the file history, you know, file history exists -- I actually went and got the file history off the U.S. Patent Office website myself, things like that. And but those were going to be intrinsically in the matter anyway no matter who provided them.

Q Understood. Did counsel provide you with the other references listed here?

A Well, obviously counsel provided me with the '164 patent because that's how this all got started. And counsel provided the Yoshinaga reference and the Haralabidis reference. And I don't recall who provided Miller, Matthew, and Beauchamp. That could have been -- some of those could have been mine; some of those could have been counsel.

And obviously, for example, 1023 and 1025 were from another matter that's been going on, or a related matter to this.

Q Were you ever asked to perform a prior art search of your own for this matter?

A I don't know if I was asked -- formally asked to do it, but I tend to do it for completeness. I have a lot of experience a lot of years doing this and so I've actually built these things and so I'm familiar with a lot of the language and background of these things and so I do my own searches regardless. And for example, that's how I found 1008, the Saint book.

Q Do you review -- after your review of the

prior art, do you find that the prior art that you relied on is the best prior art?

MR. ANDERSON: Objection, calls for a legal conclusion.

A Well, I'm not sure what you mean by "best prior art," because, obviously, you know, who knows what other art might be out there. This is a -- you know, the integrated circuit business has been around for a very long time. I've been in it for a very long time. And so if there's other prior art out there which may be, quote/unquote, better, I'm not necessarily aware of it.

But on the other hand, the prior art that I was provided and that I also found on my own was sufficient for me to form the conclusions and the opinions that I did.

Q Now, sitting here today, is there anything in your declaration that you'd like to correct?

A Actually, there is. If I can get this visitor off my declaration.

In paragraphs 350 and 351, there -- it must have been fatigue mistake because I had

everything correct around it and somehow botched what I said in 350 and 351.

If you look on the prior page, such as in paragraph 347 I talk about how Saint discloses signal pins which are connected to three different power supply and ground buses in order for the ESD protection, the twin diode configuration, and EP groups pad. Some of the signals will go to VCC and ground one, some will go to VCC and ground 2, and some will go to VCC and ground 3. And that's pretty straightforward.

And then somehow in 350, I refer to those pins as being ground power supply pins and that -- that's -- they're signal pins. That's just that goof-up on my part. Again, I -- must have been fatigue. It was a lot of late nights back in the dark, cold fall working on this. And obviously, wouldn't have 16 power pins.

And so those really are -- those are signal pins and the signal pins are grouped so that those signal -- particular subset of the signal pins use a particular bus, VCC 1 bus or 2

or 3 and the corresponding ground for the -- the ESD path to shunt the ESD energy out of the -- away from the circuitry and off to the rails.

And I make a similar comment somewhere in 351. And then at the end of 351, I start talking about the pins 1 -- the groupings involve shunting them to ESD. And then in 352, I have -- I have this correct where I say that the pad groups are connected to the respective lines for ESD protection.

So that thing in 350 and 351 where I somehow said that -- referred to them -- went off-track and referred to them as ground and power supply pins, that's just a goof. I don't know how that happened. I plead fatigue. But around it, before and after it, it's done correctly, so...

Q So just to be clear for the record, in paragraph 350 where you say "Saint Figure 7-6 (on p. 161) shows ground/power supply pins,) that should say "shows signal pins"?

A It's signal pins that are connected to the identified ground and supply rails for providing

ESD protection, which before this part and after this part I had correct.

Q So paragraph 350 of your declaration should say "Saint Figure 7-6 (on p. 161) shows signal pins that are connected to the identified ground and supply rails for providing ESD protection"?

MR. ANDERSON: Objection to form.

A Something to that effect. Basically, even if it just said "shows signal pins," that would be -- that would cover what happened. Because later is where you have -- and again, it's correct before and after in my declaration.

You have the signal pins and then the signal pins are grouped because of the circuitry being different types of circuitry, you connect the different types of circuitry to different buses to keep them separate from each other for reasons I discuss elsewhere in the declaration.

Q Okay. So just to be clear, paragraph 350 should say, at minimum, "Saint Figure 7-6 on page 161 shows signal pins"; is that fair?

A The signal pins numbered 1 to 16. And, again, in the next paragraph why they're have that -- that little notation, the color -- Saint has the coloring to show the different VCC 1, 2, 3, why that's listed that way to the side there.

Q Okay. Besides that change from "ground/power supply pins" to "signal pins," are there any other changes you need to make to your declaration?

A Similarly the beginning of 351, the same thing happens at the line at the bottom of page 168. Again, this could be the simplest correction where it says "ground/VCC pads," those are signal pads.

Q So other than the changes to paragraphs 350 and 351, is there anything else in your declaration you'd like to correct?

A Not at this time, no. I'm sure that in something with 219 pages, there might be a few typos here and there but we're only human. But if anything else come up in the discussion that appears that way, I will certainly say something.

But that's the one I noticed when I was reviewing it. Slapped myself in the face when I wondered how that happened.

Q So other than the changes you just mentioned to paragraphs 350 and 351, there are no other changes you'd like to make at this time to your declaration?

A That is correct. I said, if we go through something and as we're going through it I find a problem, I will certainly let you know.

Q Perfect. Okay. Let's go to paragraph 6 of your declaration. Let me know when you're there.

A Oh, yes. I'm there on my paper copy and I see you have it in front of me as well on the screen.

Q In paragraph 6 of your declaration, you state you are being compensated at a rate of $600 per hour, correct?

A That is correct.

Q Do you have any stock in Micron?

A No, I do not. And I never have either. I

have never owned any of Micron's equities.
Q Do you have any bonus tied to how well Micron does as a company?
A No, I do not.
Q Have you ever received any compensation for your inventions from Micron?
A For what was that?
Q Let me repeat my question.
Have you ever received any compensation for any invention you may have made from Micron?
A No --
MR. ANDERSON: Objection to relevance.
A Okay.
THE WITNESS: Well, sorry, Shane. I stepped on you. Why don't you object and I'll --
MR. ANDERSON: Objection to relevance.
A No. I have not received any compensation for inventions. I did briefly have Micron as a client way back in, like, 2001 or so. I did pay them a visit in Boise. We were working on -- they were potentially interested in using some of my analog process design kits that I had developed

for -- at the time, they were thinking about doing a -- some type of CMOS image sensor and some of the things I was doing were an interest to them.

I paid them a visit. They paid my expenses for the visit. They paid some time for my hours, but the key -- my recollection is the key guy driving that left Micron and they dropped that.

Now, if they picked it up years later, I'm unaware of that. But that was my only formal interaction with Micron and that was almost 25 years ago.

Q So to be clear, your only interaction with Micron is a brief consulting visit you did back in 2001?

A 2001. And I may have done some -- you know, a few hours of work preparing some things about these low voltage, low current process design kits they were interested in having me develop and use.

If they pursued that CMOS image sensor, which they did not at the time, as I said, I was

told that the gent who was driving it left Micron, if they picked it up later and did that I'm unaware of it. If Micron later decided to make a CMOS image sensor, I wasn't involved in it in any way.

Q Other than your consulting visit with Micron in 2001 regarding the CMOS image sensor, have you done any other consulting for Micron?

A No, I have not, other than the litigation support, of course.

Q Okay. All right. Let's pull up Exhibit 1001.

(Exhibit 1001 marked for identification.)

REMOTE TECHNICIAN: Again, when it's on screen, would you like control, Counsel?

MR. WATSON: Yes.

Q Dr. Foty, do you have Exhibit 1001 in front of you?

A I have it on the screen and I have my paper copy to my left.

Q Okay. Exhibit 1001 is U.S. Patent No. 10,879,164, correct?

A That appears to be the case, yes. And I have it listed in my binder as Exhibit 1001.

Q So if I refer to the '164 patent, you understand I'm referring to this exhibit, fair?

A That's fair. Fortunately, we don't have any cross-numbers here that are a problem. I've run into that before, but we don't have that here.

Q All right. Let's go down to the claims, shall we.

You there, Dr. Foty?

A Yes. I'm there on my paper copy as well.

Q Okay. So the '164 patent has four independent claims, correct?

A Claim 1, claim 6, claim 8, and claim 12 appear to be four independent claims. Yes.

Q Okay. If you'll go to claim 1, it requires "a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus."

Do you see that?

A I see that, yes.

Q Okay. Go to claim 6 now. Claim 6

requires "a plurality of bonding wires configured to connect one to another of the plurality pad groups."

Do you see that?

A I see that. Yes.

Q Would you agree with me that one difference between claim 1 and claim 6 of the '164 patent is claim 1 requires using bonding wire to connect pad groups to a common ESD bus, while claim 6 requires using bonding wires to connect pad groups to each other?

MR. ANDERSON: Objection, calls for a legal conclusion.

A That's what they appear to say and 1 and 6 obviously have some differences or they couldn't be -- it couldn't be separate claims in the patent.

Q Would you agree with me that one of those differences is claim 1 involves using bonding wire to connect pad groups to the ESD bus while claim 6 requires using bonding wire to connect the pad groups to each other?

MR. ANDERSON: Same objection.

A Well, the claim 1 specifically refers to a common ESD bus which is a term used in this, not just ESD bus but common ESD bus; and claim 6 says what it says.

So I will agree to the extent what you said these -- these two claim elements are similar but they refer to slightly different things.

Q Now turn to claim 8, if you would.

A Okay.

Q Would you agree with me that claim 8 is basically a method claim version of claim 1?

MR. ANDERSON: Objection, calls for legal conclusion.

A I think you're correct in that count. And if that is correct, I should mention that when I do the analysis because I -- I know that in the declaration, I did mention that a particular claim was the method version of an apparatus claim that appeared earlier.

Q Well, let's go -- let's go to that. Let's pull up again Exhibit 1003, your declaration.

Let's go to paragraph 290 of your declaration.

A Yes. I'm there. 289 and 290 seem to be what I was referring to mentioning certain claims being method versions of earlier apparatus claims.

Q Okay. So you would agree that claim 8 is basically a method claim version of claim 1; is that fair?

A That's fair. And again, that's what I said right there in paragraph 290.

Q Okay. And similarly, if you look at paragraph 289, claim 12 is basically the method claim version of apparatus claim 6?

A That's what I said there, yes. And there are some -- the way they're organized, I believe I had some discussion it was easier to refer to certain aspects to cross to the other earlier apparatus claim. I may have said that in there. But as I said, 12 is basically the method claim version of the apparatus claim 6.

Q Now, if we go back to the '164 patent, I'll turn there, one of the terms found is the term "ESD bus."

Do you see that?

A Apologies, Counselor. I was coughing and missed part of your question. So could I have that again?

I think the smoke is acting up here again, so I'll do my best today.

Q Sure. Do you see that the claims of the '164 patent discuss an ESD bus or ESD buses?

A There is numerous references in the claims to "ESD bus" and "ESD buses" in many -- in a variety of forms, shall we say.

Q What was your understanding of what an ESD bus is when you analyze these claims?

A Well, the -- my understanding from experience is that the plain and ordinary meaning of a bus is something to which more -- a number of things can be connected in order to essentially all be connected to the same thing.

A power supply bus, for example, would be a place where you could connect circuits to the same power supply. So it -- it refers to something to which provides a sort of generalized

reference or generalized line -- it's a generalized line, a generalized metal line of some sort to which a number of things can be connected to have them be connected to the same thing.

Q So let's turn back to paragraph 59 of your declaration, I apologize for jumping back and forth but I want to make sure you have the original source.

A I have the space here to do it, so...

Q Are you there in paragraph 59 of your declaration?

A Yes. I'm there at that paragraph now.

Q So based on what you said in paragraph 59, would you agree that an ESD bus is a power or ground line that has ESD protection associated with or attached to it?

A That is the general use in the art and that's where that 1026 reference is handy. It shows that general use. There are a few -- I don't know if I want to call them niches or something where there's a separate ESD bus, but the general tone in the art and it's what appears

in the '164 patent and the references here, is compatible at least with the standard approach which in the -- what is 1026, the -- I want to refer to it as the Ito paper or Banerjee paper -- 1026, the Ito paper, I have a reference from that, there's a very nice figure showing the standard protection you have where the input pad is connected on the way to the circuitry.

There's a dual diode architecture and what that does is the two diodes allow positive events -- I believe it's positive events or positive polarity ESD events are shunned to the power supply rail and negative ESD power supply events are shunted to the ground rail or to the lower voltage rail.

Q So when you referred to an ESD bus in the '164 patent, you were referring to ground or power lines with ESD protection associated with it; is that fair to say generally?

A I believe that it is. If we're going through this and we stumble across one that's, you know, often a small application where there's

something different done, but I don't believe here there's any sort of other bus than -- than using power supply and ground lines in the standard fashion.

Q Now, let's turn back to the '164 patent real quick. I want to go to column 1, lines 48 through 50.

Let me know when you're there.

A I'm there, yes.

Q Okay. Would you agree with me that one of the purposes of the '164 patented invention is to provide an integrated circuit ESD bus structure that makes full use of the circuit area?

MR. ANDERSON: Objection to form.

A That's what it says. The -- the patent is teaching techniques for rearranging things so that the -- so that there's saved space created between the various things, increase the amount of circuit area.

Q Okay. All right. Let's go back to your declaration.

Let's go to paragraph 34 of your

declaration.

A Yes. I'm there on the paper copy as well.

Q In your declaration, you're arguing for three grounds of obviousness, correct?

A That is correct. That's what my analysis provides later in the declaration.

Q Okay. You did not offer an opinion that the claims in the '164 patent are anticipated by the prior art, correct?

A No, I do not. I don't offer any anticipation assertions for these claims.

Q And in paragraph 34, those are the only three grounds of obviousness you analyze in preparing your declaration for this IPR proceeding?

A That is correct.

MR. ANDERSON: Objection to form.

THE WITNESS: Sorry, Shane. Shane, do you want to get that on the record?

MR. ANDERSON: Objection to form. Thanks.

A These -- these are the only three grounds that came out of my analysis and the conclusions I

reached and the opinions I formed. And those are what are written up in this declaration.

Q Have you done any other analysis regarding the obviousness of these claims?

A Not that I'm aware of. I believe all my conclusions and opinions are embodied in the declaration.

MR. WATSON: Can we pull up Exhibit 1006?

REMOTE TECHNICIAN: Please stand by counsel.

(Exhibit 1006 marked for identification.)

BY MR. WATSON:

Q Dr. Foty, do you have Exhibit 1006 in front of you?

A It's on the screen and what's on the screen appears to be what's the same as my clean copy I have to my left here.

Q Is Exhibit 1006 the translation of the reference you've referred to as Yoshinaga?

A Yes. This is a certified translation of Yoshinaga. The original is in Japanese.

Q So you referred to Exhibit 1006 when you

were analyzing Yoshinaga?

A Yes. I refer to 1006 as Yoshinaga in the declaration. This is the Yoshinaga reference.

Q You put that one to the side. We'll come back to it.

MR. WATSON: Let's pull up 1007.

REMOTE TECHNICIAN: Stand by.

(Exhibit 1007 marked for identification.)

Q Dr. Foty, do you have Exhibit 1007 in front of you?

A I see it on the screen and this appears to be the same document as I have in my binder for Exhibit 1007.

Q Is Exhibit 1007 the reference you refer to as Haralabidis?

A Well, we can argue about the Greek pronunciation. This appears to be the Haralabidis reference. And if that's -- and I don't mind, Counselor, if you want to because I'm humane, if we want to refer to this as "H" or something so we don't end up with ten versions of the same reference in the transcript, it's up to you.

Q You called it Haralabidis? How did you say it again?

A Haralabidis. If it's -- judging by his first name and his co-author, I believe that they're Greek. And the letter "Iota" in Greek is pronounced like the "I" we have in "kit," so that's my best guess. But again, if you -- it's a tongue-twister. And if you think it will be better to refer to this as "H" in order so that the transcript doesn't have multiple versions of what are the same reference, I'm happy to do that to make our lives easier today.

Q You know what, let's just call it Exhibit 1007; is that okay? When I refer to Haralabidis or Exhibit 1007, you'll understand I'm referring to this reference; is that fair?

A That's fair. Again, it's a tongue-twister and I want to make sure that neither of us gets locked up and/or that the transcript -- the record gets messed up by that. So if we want to refer to it as 1007, I'll understand what that is.

Q Okay. All right.

MR. WATSON: Let's load up Exhibit 1008.

REMOTE TECHNICIAN: One second, please.

(Exhibit 1008 marked for identification.)

Q Dr. Foty, Exhibit 1008 is the reference you refer to as "Saint," correct?

A Yes. The authors are Saint and Saint, and so it's a book that I refer to as the Saint reference.

Q Okay. So when I refer to "Saint," you'll understand I'm referring to Exhibit 1008?

A Yes. Fortunately, "Saint" is easy to pronounce.

Q Much easier. I agree with that. Well, let's go back to your declaration. I just want to make sure we were on the same page as to what reference we're talking about when we discussed Saint, Exhibit 1007 or Haralabidis.

A Don't need to try.

Q The "H" reference, and then Exhibit 1006 is Yoshinaga.

A That's fine.

Q Let's go back to Exhibit 1003

paragraph 34. Let me know when you're there.

A Okay. I'm at paragraph 34, and you have it on the screen here.

Q For ground 1, you opine that claims 6 through 7, 12 and 14 are obvious based on Yoshinaga in combination with Saint and the knowledge of a POSITA, correct?

A That's my conclusion. Yes.

Q For ground 1, you only rely -- list the Saint and Yoshinaga reference in your obviousness combination, correct?

A Yes. That, and the knowledge of a POSITA.

Q You do not include any references other that Yoshinaga and Saint in ground 1, correct?

A None of the documentary references, no. Just Yoshinaga and Saint.

Q For ground 2, you opine that claims 1 through 6, 8 through 11, and 13 are obvious based on Yoshinaga in combination with Saint, Exhibit 1007, and the knowledge of a POSITA, correct?

A That is correct. That's what I state

there.

Q Okay. And for ground 2, you only rely on the Yoshinaga, Saint, and Haralabidis or Exhibit 1007 reference in your obviousness combination, correct?

A Was that referring to ground 2 or ground 3? Sorry.

Q Ground 2.

A Yes. Ground 2 is, yes, Yoshinaga in combination with Saint, 1007, and the knowledge of a POSITA.

Q For ground 2, you do not include any references other than Yoshinaga, Saint, and 1007?

A Those are the documentary references I use for ground 2. That is correct.

Q For ground 3, you opine that claims 1 through 14 are obvious based on Yoshinaga in combination with Saint -- sorry, excuse me, let me strike that and let's try that question again.

A Sure.

Q For ground 3, you opine that claims 1 through 14 are obvious based on Saint in

combination with Exhibit 1007 -- yeah. Sorry. Having a tongue-twister this morning. Let me try that one more time.

A If you're having trouble with "1007," I'm worried.

Q For ground 3, you opine that claims 1 through 14 are obvious based on Saint in combination with Exhibit 1007 and the knowledge of a POSITA, correct?

A That is correct. That's what I say there.

Q And for ground 3, you only rely on the two references you listed there in your obviousness combination?

A Yes. Those are the only two documentary references that appear in ground 3.

Q Now, for each ground you rely -- let me strike that. Let me try that question again.

For each ground, you relied on the knowledge of a POSITA to allege that the challenged claims are obvious, correct?

A Yes. I refer to those various items which were known in the art that a POSITA would have

known and had in their toolkit, shall we say, at the time.

Q Why did you not include a ground of obviousness based on only prior art patents or publications?

A Because there are certain things that are very common in the art that rather than the specific references or provided in the discussion, they're not used as documentary simply because they're showing how they're very common, they were known to do these things. So that's why it's grouped under the knowledge of a POSITA.

Q So do you need the knowledge of a POSITA in addition to these references you list here in order to arrive at your obviousness combinations?

A Well, I would say that the way I would answer that question is that rather than put multiple references for that and clutter things up, there's certain things that appear multiple times very easily found in the prior art multiple times without doing an exhaustive search. And that indicates they were very well known and so a

POSITA would have been aware of them, would have known of them at the time due to the large amount of instances it appear in the art.

Q Okay. I don't think that answered my question so let me try it again.

For grounds 1 through 3, do you need the knowledge of a POSITA to arrive at your obviousness conclusions or can you just rely on the references cited?

A Well, I would say the knowledge of a POSITA is necessary to show that these -- there are things that are so extremely well known, that's basically what it meant. So those are required to reach the conclusion.

Q Okay. So you need to use common general knowledge in addition to these references to arrive at your obviousness conclusions; is that fair?

A That's fair. And again, the -- there were examples in here that appear where something is just there and it's not even discussed because it's so obvious what's going on there.

Q Okay. Let's go to paragraph 28 of your declaration.

A I have that in front of me as well as on the screen.

Q Dr. Foty, you applied the date of November 1st, 2018, as the priority date, correct?

A Yes. I was instructed by counsel that that is the priority date that should be assumed for the '164 patent.

Q Do you agree that November 1st, 2018, is the priority date of the '164 patent?

MR. ANDERSON: Objection, calls for a legal conclusion.

A Well, again, with the caveat I'm not an attorney and the attorneys, knowing more about this, provided that.

When I examined the -- the first page of '164, the furthest back that references go are November 1st, 2018. So that was what counsel informed me I should use as the priority date and I see it on the face of the patent.

Q Did you do any analysis to determine

whether the '164 patent can claim priority back to the November 1st, 2018, date?

A Not particularly. I didn't see anything -- my recollection is I didn't see anything in the file history that contradicted that.

Q But you have no reason to doubt that the '164 patent is entitled to the November 1st, 2018, date, correct?

MR. ANDERSON: Objection, calls for a legal conclusion.

A I see no reason -- I see -- nothing I saw would cause me to question that.

Q Okay. Did you analyze obviousness under any other priority date?

A Not that I'm aware of, no. That was the priority date which defined what was -- could be said to be prior art to the '164 patent.

Q Let's go to paragraph 32 of your declaration: Let me know when you're there.

A I'm there.

Q Does paragraph 32 of your declaration lay

out your opinion of the qualifications of a person of ordinary skill in the art that you used when analyzing obviousness regarding the '164 patent?

A Yes. I believe that it does describe what a POSITA would be.

Q Did you -- do you apply any other qualifications of a person of ordinary skill in the art in your analysis?

A No, I did not. This was sufficient for the purpose.

Q Okay. Let's turn to paragraph 65 in your declaration.

A I have -- I have that in front of me and I see you're scrolling down to it and will be there soon.

Q Okay. Dr. Foty, you reviewed the prosecution history of the '164 patent, correct?

A Yes, I did.

Q Is there anything in the prosecution history that you reviewed that suggests the claim should be limited beyond their plain and ordinary meaning?

A I -- in reviewing it and I did my write-up here, I saw nothing to contradict that. I didn't see anything that needed to go beyond plain and ordinary meaning.

Q All right. Let's go to paragraph 71 of your declaration.

Are you there?

A Yes. And as you can tell, I've got a little company right now.

Q Just for the record, the company is your little cat?

A The company is Vidar, yes. He must like your voice, Counselor.

Q So Dr. Foty, in performing your analysis, you used the plain and ordinary meanings of the terms in the patent, correct?

A Yes. I used the plain and ordinary meanings of those terms.

Q You did not supply any special definitions to any claim terms, correct?

A No. I was -- one claim term I have made reference in the text to dictionary definitions

and that was -- that was all I did, plain and ordinary meaning.

Q And what was that claim term?

A The -- somewhere in here I have a couple places where I actually quote -- excuse me, dictionary definitions for the word "adjacent."

Q And those dictionary definitions you cited reflect what you understand to be the plain and ordinary meaning of the word "adjacent"?

A That is correct.

Q You did not identify any terms that require claim construction, correct?

A Not in this declaration, no.

Q Okay.

MR. WATSON: We've been going about an hour and ten minutes. Probably a good time to take a break before we move on to the next subject so want to take a five-minute break or so?

MR. ANDERSON: Sounds good to me.

(Whereupon a break was had.)

THE REPORTER: We are back on the record. Would counsel like to make their appearance for

the record.

MR. WATSON: Sure. I am Tom Watson from Latham & Watkins and I represent the Patent Owner, Yangtze Memory Technologies Company, LTD.

MR. ANDERSON: I am Shane D. Anderson of Orrick Herrington Sutcliffe representing Micron Technology, Incorporated. And with me on the line is my colleague, Travis Jensen also from Orrick.

THE REPORTER: Thank you, Counsel.

BY MR. WATSON:

Q Dr. Foty, have a nice break?

A Are we back on the record? Just wanted to make sure, yes. So I'm back, you're back, so we're good to go.

Q Dr. Foty, did you talk about the substance of your testimony with anyone during the break?

A No, I did not.

Q Okay. Let's turn to paragraph 50 of your declaration. Can we put up Exhibit 1003?

A And you said 50, 5-0?

Q 5-0.

A Thank you. I just wanted to make sure.

Q Takes a while to scroll these things.

Do you have paragraph 50 in front of you?

A I have it on the screen and I also have my paper copy to the left here.

Q In paragraph 50, you talk about core-limited integrated circuit and a pad-limited integrated circuit, correct?

A Yes. That is correct. Those are well known terms in the art and I've been familiar with them for a good 30-plus years.

Q What's the difference between a core-limited integrated circuit and a pad-limited integrated circuit?

A Well, I describe it here in paragraph 50 but the short take is a core-limited circuit means that the -- sorry, a core-limited integrated circuit simply means that -- it's an IC that has a great deal of circuitry and the circuitry takes up so much space that the size of the IC is limited by that circuitry. It's not limited by the number of pads you need. And in fact, and there's an example in the figure right above it from a 2010

article, shows an IC like that.

The circuitry is very large, and because of that, it doesn't need a complete set of pads around the outside. So it's the core circuitry that limits the minimum size you can make the IC. And that's very common in big, complicated, digital circuits, for example.

In a pad-limited IC, you basically have small circuitry but the need for a large number of pads so the size of the IC is limited by the number of pads you need since the pads have to be, by the ground rules, have to be a particular size and spaced a certain amount apart, that the amount of space inside the pad -- surrounding pads you need is so large that the circuitry doesn't fill up the inner space. You can have -- often, you'll have essentially empty space because you need to make the IC big enough to accommodate all the pads. And that's -- that's a more common event, as I said, in analog and mixed signal and RF types of designs.

Q So to summarize generally, a core-limited

IC is limited by the size of the circuitry itself, correct?

MR. ANDERSON: Objection to form.

A If you're trying to make -- obviously, you want to make the IC as small as possible. And the limit on making it small is the circuitry, not the pads.

Q And then pad-limited integrated circuits are limited by the size and number of the pads as opposed to the circuitry, is that fair?

MR. ANDERSON: Objection to form.

A They're limited by essentially the pads are -- you need to have the pads be around the edge of the IC. And the pads have to have, by ground rule for the process, have a certain minimum size and a certain minimum spacing between them. And so that's what limits the -- the ability to shrink the IC. You can only shrink it down to the extent you can shrink the pad way down. And oftentimes, you'll have more area inside that than the circuitry needs.

I had a project I worked on many moons ago

where the IC was -- you know, the circuitry was only four square millimeters or square microns -- square millimeters, I guess. And the having to include the pads made that footprint be six or something like that.

But what it says here are correct. These are well-known terms in the art where the pad-limited means you need to have enough pads as required and that makes the footprint of the IC bigger than you need for the amount of circuitry you're putting inside the pads.

Q Does Yoshinaga describe a core-limited circuit or a pad-limited integrated circuit?

A I would have to review Yoshinaga, but I don't think he uses the term. If he does, I'm willing to stand corrected because I know Saint mentions that term.

Q Do you want to pull up Yoshinaga real quick and just see if there's any discussion?

A I would have to review the entirety of Yoshinaga. I have to re-read -- how long is the text. The text is, like, 12 or 14 or 13 pages.

I don't recall Yoshinaga specifically using those terms and he may not go into those details. So it could be Yoshinaga -- what Yoshinaga talks about does not get involved in pad-limited and core-limited, I don't believe. But again, I would have to review 13 pages to confirm exactly what he says.

Q So sitting here today, you don't know whether Yoshinaga is core-limited or pad-limited integrated circuit; is that fair?

MR. ANDERSON: Objection to form.

A I don't think he specifies either one and so it would be -- there's nothing in there that indicates that his teachings apply to only one or the other.

Q Okay.

A Just again, these were well-known terms in the art by the way at the time of Yoshinaga.

Q Yeah. I guess my question is: Would you characterize Yoshinaga as describing a core-limited integrated circuit or a pad-limited integrated circuit, or is it just silent on the

matter?

A I would, again, have to review for details and it may come up in the inline text, but I don't -- I don't think Yoshinaga specifies one or the other. He does not make that a determinant in what he's teaching.

Q Okay. For Exhibit 1007, does that describe a core-limited integrated circuit a pad-limited integrated circuit or like Yoshinaga, is it silent on the matter?

MR. ANDERSON: Objection to form.

A Again, I would have to review 1007 in detail. But my understanding from just reading it is that, again, he doesn't take a limit to one or the other. 1007 describes an SOC approach which would involve assembling blocks. And so the blocks could be either digital or analog and he discusses the issues that occur with having both of those.

So it's probably one of those, the devil would be in the details. A certain SOC being assembled from blocks might be pad-limited or it

might be core-limited. There's no restriction either way that I'm aware of with 1007.

Q Let's go to paragraph 49 of your declaration.

A I have that -- I have that in front of me, sorry. If we're going to discuss this, it may involve the figure above, by the way. So I have it in front of me on paper, but it may involve that figure above there that's kind of peeking out on the screen.

Q So in paragraph 49, you mention that in a core-limited integrated circuit, even more wire bond pads could be included but as those are unnecessary there's no reason to add them; is that correct?

A Yes. Basically, the -- the footprint as you see in that figure above -- and by the way, that article is not about core-limited or pad-limited or even using saved space. That article is about something completely different, but it's a very nice picture that I found to illustrate this, that basically, you look at the

number of pads you need and you only use -- you'll notice every pad is bonded. There's no blank pads because that's a waste of space.

So the pads are removed to -- what you just need for a minimum. If someone wanted to redesign this, they would have to, you know, make some changes, but other pads could be added, say, if a new piece of circuitry was dropped in. But it's pretty clear when you look at this, it's a great example of a core-limited design because the pads are -- there's -- there's -- the pad spaces have no pads in places because you don't need more pads than you see here on this -- this figure above paragraph 49.

Q Would you agree that adding unnecessary components such as bond pads could complicate a design and increase costs?

MR. ANDERSON: Objection to form.

A Well, I would agree to the extent you wouldn't do that and this figure shows that. You have the minimum number of pads you need and the limit in the size here is not a pad-limited case

where you have pads occupying the whole walls and circuits based inside that doesn't cover the interior. So this is a good example of a core-limited case where you have that. You don't -- you take the pads to the minimum. There's no point in having pads doing nothing.

Q Okay. So you wouldn't agree that adding unnecessary components could complicate a design and increase costs?

MR. ANDERSON: Objection to form.

A Well, I'd have to know what is specifically meant by unnecessary component, but in this business, you only put on what you need. And then you have to cope if there are issues with -- like, in a pad-limited design if you have a bunch of empty space, then you have to do something to, you know, deal with manufacturing rules.

But in the business you don't generally put in more than you need, but I don't know if there are cases where people put in filler and things like that for various reasons.

Q So in your experience, is it standard practice to add components only when they are necessary for the design's function?

MR. ANDERSON: Objection to form.

A I think that's a fair statement. I will note that sometimes when there's space, people put little cartoons and things in. There's entire websites dedicated to the little cartoons that appear when chips are torn down. But I don't know if those are considered necessary by the designers. Maybe some do. Sarcasm alert.

Q In the pad-limited circuit, how are the power supply pads assigned?

A Basically it depends on the circuitry. And again, this is one of the reasons that analog and mixed signal designs tend to have pad-limited cases. Typically, the circuitry in an analog or mixed-signal design is a fairly small number of transistors so the actual circuitry is relatively small. But as is well known in the art I've dealt with it -- this is, again, we're talking 30-plus years and, actually, Exhibit 1007 discusses this,

you may need to have multiple power supply rails and multiple ground rails in order to keep crosstalk between various blocks of different -- different types of circuitry from interfering with each other. Such as digital circuitry is very noisy when it switches and that can -- that can get over to your sensitive signal processing analog circuitry. It can mess up its functionality.

Q How are ground pads assigned in a pad-limited integrated circuit?

A Well, in the same way. First, you need to determine how many you need. That's design-dependent. Sometimes you have one power and one ground. Other times, you may have multiple for the reasons that I described. And then it's up to the designer to position them in what the designer concludes is most efficient manner for, for example, for bond wiring so that wires aren't interfering with each other and so forth.

Q So in a pad-limited integrated circuit,

what fraction of the total chip pads are power supply pads?

MR. ANDERSON: Objection to form.

A There's no fixed case because it depends on the circuitry being put in. There could be one. There could be multiple. It depends on the circuitry and the different types of blocks and the type of signals that are being processed.

Q So would you agree with me in a -- integrated circuit the number of power supply pads and ground pads is dependent upon the power needs of the circuit?

MR. ANDERSON: Objection to form.

A I don't know exactly what --

THE WITNESS: Sorry, Shane, go ahead. I stepped on you.

MR. ANDERSON: Objection to form.

THE WITNESS: Sorry.

A I would characterize it as I don't know what you exactly mean by "power needs," but there's power needs in terms of the amount of power that needs to be supplied, but there's much

of the using, say, multiple power supply or ground pads has to do with signal integrity, keeping one block's signals from contaminating the other block. Typically, this is digital signals which are very noisy. Their -- their noise can propagate through, say, a common ground line and interfere with the operation of the nearby -- a nearby analog block.

Q So when you look at a design circuit, would you assume that the power supply pads are proportionate to the amount of power needed in the circuitry?

MR. ANDERSON: Objection to form.

A I suppose that could be a factor where you're going to distribute power. It's almost like distributing power in a local power grid. But the main reason you separate ground and power lines is for signal integrity purposes just to keep signals -- to keep noise from propagating through -- through -- through, say, a common ground back through another -- another block.

Oftentimes, things are moved further out

because you want to have a lower resistance, like if you get in the package the lines are wider. In the PC board, the lines are even wider. And the low resistance parts of that -- and this -- actually, 1007 discusses this. The low resistance parts help attenuate that noise.

So if you have a noisy digital block, there's techniques for having that go to a line with a resistivity which is much lower to attenuate it. But again, you have the separate power supplies and the separate grounds. The main reason is signal integrity, which is why you see that in analog circuits.

There may be big digital circuits because large digital circuits pull down a frightening amount of power where there may be power distribution issues in a big -- like a microprocessor or something like that.

Q Would you place all the power supply pads on one side of a chip and all the ground pads on the other side of a chip?

MR. ANDERSON: Objection to form.

A That's a design-specific choice depending on what blocks are put in and where they're placed. You would want to put -- if you have digital blocks and analog blocks, you would typically put the power supplies for them close to where they are. So there are a wide variety of reasons why you would do that and, typically, it's to keep pads close to the blocks to which they're going to be connecting.

Q So if you needed more power supply in an area -- a block of the circuit, you would want more power supply pads near that area, correct?

MR. ANDERSON: Objection to form.

A Well, again, that would be very design-specific because, again, as I said, the main reason you have multiple power supply pads is for signal integrity reasons. As I said, there may be some digital designs where you have issues with needing multiple wires to go in so that certain pads into the circuitry don't carry too much current, say for electro migration concerns. But that's one possible option in that realm.

The main reason, though, you see that done, as I said, is for signal integrity -- excuse me, signal integrity reasons.

Q Would you agree that ground and power supply pads are freely moveable among each other?

A I'm not --

MR. ANDERSON: Objection to form.

THE WITNESS: Sorry, Shane. Go ahead.

MR. ANDERSON: Objection to form. Sorry.

A Well, I'm not sure what you mean by "freely moveable." But in a design, you have -- the designer has great flexibility to place pads around the periphery of the IC as to optimize the design, particularly with regard to wire bonding where the wire bonds go to the traces in the package.

Q Let's go to paragraph 45 of your report.

A Technically, it's a declaration.

Q Declaration, you're correct. Sorry. Let's go to paragraph 45 of your declaration.

A The reason I mention that, I don't want someone reading that and looking for the report in

addition to the declaration. So there is no report, just one declaration.

Q Let me know when you're in paragraph 45 of your declaration.

A Yes. And I'll note that 45 actually spans three pages with a large figure in the middle of it.

Q Yeah. I want to direct your attention to that figure in paragraph 45, if that's okay.

A Okay. I'll pull it up here. I may have to pause to read the text around it.

Q No problem. So what does the figure in paragraph 45 of your declaration show?

A I believe this shows a particular physical design layout and these are the shapes that we put in mask. That's why Saint refers to -- the title of Saint is Mask IC Design, by the way. Saint is not involved in this figure or discussion, but these are the different layers that are used when you manufacture this circuit. And I think this circuit is a two-input CMOS NAND gate, a logic gate.

Q Does the figure in paragraph 45 represent a typical or well-known user case for circuit design?

A I believe that it does. This is a -- this is a typical layout, a very, you know, dense, densified layout of a two-input NAND gate which has four transistors.

Q In this figure in paragraph 45, what is metal 1?

A Metal 1 is the lowest in the stack of metal layers you form. It's the lowest metal wiring layer formed in the IC. You could actually -- I mean, there's six layers here and they would be done in a sequence, and I can recite the sequence if you wish, but you'll notice the six levels there in manufacturing. You would perform each of those separately as you built this up.

Q So what is metal 1 used for?

A Metal 1 is actually -- exists to provide the connections between the transistor terminals that would give you the logic functionality of a

CMOS NAND two-input NAND gate. This actually, one reason I included the Uyemura -- back in paragraph 44, you can see the -- Uyemura reference, there we go, reference that shows the design flow. And so you can see that there's a system level first; then that's reduced to logic gates in a digital design; and then that's reduced to an actual transistor-based circuit, how are you going to put the stick diagram of the circuit together.

Then the stick diagram, you see in the middle of the figure in paragraph 44, it's the same actually with everything above it, but that is essentially a topological description. It tells you what transistors and components are there and how their terminals are connected together. But it's just a purely topological description.

And then that has to be taken and converted into the physical design which is the layouts which are used for mask layers. You'll actually create photolithographic masks of -- there will be six of them represented in this

figure we see on the screen in paragraph 45. And so those are the various layers that are used in order to form this physical design.

And metal 1 serves to provide the connections between the transistor terminals. And one of skill in the art can look at this and sort of work backwards as to which transistor terminals are which, but it does come out to the two-input NAND gate. I did not provide a topological depiction of the two-input NAND gate, but that's extremely well-known in the art.

Q So is metal 1 used to connect the components within the circuit?

MR. ANDERSON: Objection to form.

A It's used to connect the terminals. The only exception to that is because the inputs -- like the A input of the NAND gate goes to both the -- a PMOSS transistor and an NMOSS transistor, so that's done with one shape here. And the same with B, you have -- it's convenient to have the -- when the same signal input goes to two transistors, you provide it with one shape and

that's what's done there.

And so the metal one connects together the sources and the drains of the transistors in order to connect to the power supply at the top, the ground or low voltage VSS at the bottom, and the output. So essentially, here you provide that functionality, in this case, by connecting together the -- the diffusions of the transistors. That's what metal 1 does here, but metal 1 could connect to other things.

Q Could metal 1 one be used to connect pads?

MR. ANDERSON: Objection to form.

A I suppose that's theoretically possible, but you wouldn't do that because the pads are at the very top. And so typically connections for the pads are made with higher level metal such as the -- whatever the top metal is in the particular process because those lines are wider and thicker and they can carry more current.

So again, it's -- you think of it as a -- in the city, how electricity is distributed in the city. You have the big -- big lines on the

outside and the lines are stepped down with transformers when they come into your house. The voltage is stepped down.

Q So is there a metal 2 layer here in this circuit shown in paragraph 45?

A It's not depicted, but unless it's a very simple process, there would be multiple metal layers like metal 2, metal 3. I think nowadays, we're up to, like, 15 or 16 metal layers in the most advanced processes that are being manufactured. Like the -- I think we're down to 3 nanometer processes now and there's like 16 or 17 metal layers.

Q So a typical integrated circuit could have up to 16 different metal layers; is that fair?

A It depends on the process generation. For example, 130 nanometer processes of, like, 20-plus years ago had five metal layers. And basically, every process generation, another metal layer is added. And so, that has held. And basically, I have to go check, but I think the more -- you know, the really small processes that are being

manufactured nowadays have, like, 15, 16, 17 metal layers stacked up on top of each other.

Q Do these other metal layers, are -- strike that.

Are these other metal layers used to connect pads in the integrated circuits?

A Typically, the pads are connected to the topmost metal layer where they connect in to the highest levels of power and ground and signal buses. And then those -- those basically fan out to the -- you have a billion transistors and you have 100 pads. Obviously, there's going to be quite a bit of fanning out going on.

So again, it's like a municipal electricity system where you have the stuff at the top and then it fans out. And at your house you get a small line with a transformer stepping it down to 120 volts AC for you. So typically, the top metal is what's connected to the pads, although there's not -- that may depend on the ground rules. There may be some other options other than just using the top metal.

Q So if you had a three metal -- strike that.

If you had a three-layer integrated circuit, metal 3 would be used to connect the pads typically?

MR. ANDERSON: Objection to form.

A When you say a three-layer process, that's not a term of the art.

Do you mean a three-metal layer process?

Q Sure. Let me -- let me rephrase it. Thanks. I appreciate the clarification.

When you say a three-layer metal process -- or strike that.

When you say a three-metal layer process, metal 3 would be the one used to connect the pads, correct?

A That would be --

MR. ANDERSON: Objection to form.

THE WITNESS: Sorry, Shane. Go ahead.

MR. ANDERSON: Objection to form.

A That would be the typical expectation. I would have to review ground rules for a specific

process if there were other things you could do. But, typically, if you wanted to even, like -- say you wanted to connect to metal 2, you would actually have -- the pad would connect to metal 3 and then it would connect down to metal 2. So eventually, though, the pads -- if the pads are ground-rule limited to being only connected to the top metal, then you work your way down with vias to metal 2 and metal 1 and you work your way down that way.

Q Okay. Now, in this figure in paragraph 45, what are the contacts in the figure?

A The contacts are the layer below metal 1 that connects, as we see here, to the diffusions of the transistors. The kind of reddish area and the kind of yellowish area are the diffusions of the transistors, the sources and drains.

Q Are those contacts considered pads?

A No, they're not. They're considered via contacts.

Q Are there any pads depicted in this figure in paragraph 45?

A Not in this particular figure. This is a low-level primitive of a very simple circuit, a two-input NAND gate. This would typically be -- in a design, this would either be a library of circuits. And usually these libraries would have -- they might have 10 or 12 or more two-input NAND gates that are different from each other in their -- like, their dimensions, their transistor dimensions. But this is a low-level primitive and a designer would put this block into a design to layout a two-input NAND gate.

Just to -- the one thing that makes this technology work so well is somewhat -- a designer would not have to sit down, the physical design engineer, and draw this circuit multiple times. This circuit would be drawn once, put in a library, and then reused. But basically, this circuit shows what a two-input NAND gate looks like and would be copied into the design as a block.

Q Are -- does the figure in paragraph 45 include any bonding wires?

A No, it does not. This figure is exemplary to show what physical design means and the shapes mean. That's why it's in the overview section.

A bond pad would somewhere connect to the metal lines we see here. Somewhere between this circuit and the outside world there would be a bunch of metals vias going upward and eventually obviously there would be a VDD pad and obviously there would be a VSS pad, the lower section.

The output of this might go to another circuit. It could go to a pin. So those are higher level for the moment here. This is simply illustrating the kind of design -- the physical design phase which is the layout phase of the circuitry.

Q So in -- in this figure in paragraph 45, there are no bonding wires depicted, correct?

A No. This is a -- this is a primitive, essentially a low-level circuit that would be included at the lower levels of the IC stack.

Q Now, I want to talk a little bit about the metal layers again, if that's okay.

A Sure.

Q So you mentioned that typically the pads are connected via these different metal layers; is that correct?

A The typical design would be the pads would be connected to the top metal layer and then, typically, that's required because if you think of it like a sandwich, you know, the bread on the bottom and the cheese on the top of the cheeseburger are separated from each other. So you stack the things up.

And so the -- as you build the IC up in layers, you would build metal 1, metal 2, metal 3 to the top metal, and then the pads go above that. And so you typically would connect the pad downward to the top metal in order to start the process of having the pad -- you know, you have a -- essentially you have a metal path down to a transistor in order to have the circuit have functionality.

Q And so if -- going back to our three-metal layer example, if you wanted to connect something

beneath the top layer, you would connect it using metal 2 or metal 1 as opposed to metal 3; is that fair to say?

MR. ANDERSON: Objection to form.

A Could you repeat that? I -- it was confusing and it may not be compatible with the design so I don't want to answer if it's a question that doesn't make sense in terms of physics of the --

Q Yeah. Let me repeat it and break it down a little bit, if that's okay.

A Thank you.

Q All right. So we -- for this example, I want to refer to a three-metal layer, okay?

A Three-metal layer process?

Q Yes. Three-metal layer process. Yes.

A Okay.

Q So we have a three-metal layer process with metal 1, 2, and 3. Okay?

A Correct.

Q Okay. Metal layer 1 is the bottom layer connection; is that fair?

A In the -- in the inner connect stack which is above the circuitry, it would be the bottom layer. And in this figure we're looking at, this metal 1 is actually the highest layer you see depicted here in this vertical stack, but then metal 2 and metal 3 would be above that.

Q Okay. And then metal 3 would be the topmost layer, correct?

A If it's a three-metal process, yes, it would be the topmost layer.

Q And metal 3 would be what connects the different pads; is that right?

A That would be --

MR. ANDERSON: Objection to form.

THE WITNESS: Go ahead, Shane.

MR. ANDERSON: Objection, form.

A That would be the typical implementation scenario.

Q If you wanted to connect pads underneath that top layer, you would use either metals 2 or metal 1 to make that connection; is that fair?

A Yes. The contacts you see here -- and

this is a good example to explain that, the black contacts you see are essentially below metal 1. That would be called via 1. So you have via 1 is formed. You put metal 1 down and you connect things together through metal 1 down to the silicon through the vias.

Then the second metal, you would make a via 2 which would be on various places in metal 1, and then you would put the metal 2 lines through to connect to those vias to connect metal 2 down through via 1 to metal 1. And then you put via 2 on top of metal 2 and then put metal 3 on top of via 2. And you would continue that process for as many metal layers as you have.

Q Let's switch topics up a little bit.

What is wire bonding?

A Well, I had a whole section starting on the -- paragraph 46.

Wire bonding is long been used and it's basically one of the most common methods of you connect an IC to the traces in a package because you have to take the IC and plug it into

something. It has to be the -- the pins have to be connected to it.

And so basically the IC, the edge of the IC is the pads. The pads are put there specifically to allow wire bonds to be done. And then so you have a tool. There's a piece of equipment that puts the wire bond to a pad on the edge of the IC and then connects that to a package trace. And then that package trace is actually in the package and connects to a pin on the package.

And then, typically, what's done is once the wire bonding is done, molten plastic is poured in to isolate and hold everything in place. And then you have a packaged IC, such as the one you see on page 24. There's a figure showing a plastic packaged IC with pins on a PC board. And that's the end goal.

And the -- on the page 25 and page 26, there are figures showing a typical IC showing the pads that are used for wire bonding. And the one at the top of page 26 shows that earlier figure we looked at, the core-limited IC, showing the wire

bonds going to all the pads and leaving the picture because they go to traces that are connected to the package pins.

And in order to make this figure, this is a what's known as a teardown. You actually have a, usually, a specialized lab has to be able to remove all that plastic that was poured in, the molten plastic, to seal everything in place so you can see what was inside there.

So wire bonding is well-known and it's illustrated here by these figures, particularly the figure on page 26.

Q Now, do you need to be able to access the metal pads in order to be able to wire bond them to these traces?

A Well, I don't know what you mean by "access" because the way you do this is when the IC is first made, it's made with what you see, for example, in the figure at the top of page 25. You have the whole integrated circuit and then you have the pads around the outside.

And, typically, what's done in

manufacturing is that you have a wafer full of these chips. And before the wafer is even cut up into individual dies, testing is done to identify which are good and which are bad. Then when it's cut up, the bad ones aren't sent off to be bonded and packaged. So then you would have to -- it's call singulation, is the term of the art, where you cut the wafer up into the various individual ICs.

And then those ICs are put in a package, mounted up in the package. Then the wire bonding is done to make it a real product that you can plug into a circuit board. And then once the wire bonding is done, the typical thing is to pour molten plastic in and seal the whole thing up.

And then that can be essentially -- you see on -- on the top of page 24, that's something that's been wire bonded and packaged. And now it can be soldered in to a PC board in some sort of system product.

Q Would you be able to connect bonding wire to the pad from its bottom side, from the bottom

side of a circuit?

MR. ANDERSON: Objection to form.

A Well, the -- I'll pick a caveat after I answer that.

The typical way this is done is what you see in pages 24, 25, and 26. You have the IC is a single type. It's a -- you know, it's a chip. It's just a two-dimensional piece with the pads and you bond them to the wire bond, like you see on the top of page 26.

Now, that's typical of that. I know that -- it's outside what we've talked about here, but I'm aware that nowadays there are also -- when you get into these 3D structures and multichip packages, there are things done to bond things from the top and the bottom. And -- I'm aware of them, but I didn't consider them here. But I'm aware they exist, just as I'm aware there's a lot of circuit boards can be multilayer and there's a lot of art in multilayer circuit boards and connecting things from the top and the bottom and so forth.

But that's -- that's not in play in the '164 patent or the prior art. This is a more conventional type of simple, flat integrated circuit.

Q So typically, bonding wire connects to the external traces at the top of the circuit on the external side of the circuit?

MR. ANDERSON: Objection to form.

A When you say "external side of the circuit," what do you mean by that?

Q I mean, the -- using our layers of metal, like at the topmost layer.

A Well, typically, the topmost metal layer is not where the pads are formed. Typically, the topmost layer -- nowadays, it's copper, but the pads are still typically aluminum so you have, like, this extra layer where the pads are formed in aluminum. And then the pads are what in the simple, you know, basic, flat two-dimensional IC, surface IC that we see here, then you would wire bond those off to the package to connect to the package traces and then connect to the -- which

the traces literally are metal pieces that on one side it's a trace you bond to; the other side it's a pin in the package and then you fill it all up with molten plastic.

But again, it's outside what we did here with the '164 patent. There are other -- when you get into, you know, stacking multiple chips into these multichip packages and things are tipped sideways and etched, there's a whole art that's just not at play here in the '164 package. So I can't speak to that type of art today.

Q Okay. So on the typical process, an integrated circuit is formed and then the wire bonds are placed on the top; is that correct?

MR. ANDERSON: Objection to form.

A When wire bonds are used, that's typical process. Again, there are other methods of doing that which are mentioned in the report.

Like, you know, these solder balls and things like that. They are other -- other various method. But the wire bond method is very common. And again, this is the -- this doesn't include any

of this other art that involves, you know, 3D packages and flip-chipping and doing things where things are turned on their sides and ground and etched. There's a whole art that I didn't consider here because it didn't need to be considered in this with regard to the '164 patent.

Q Now, when a wire bond is created, there's a resistance added at the point of contact to the pad, correct?

MR. ANDERSON: Objection to form.

A There --

THE WITNESS: Sorry, Shane. Go ahead.

MR. ANDERSON: Objection to form.

A There -- any time you have any metal, a metal has resistance, you know. We often can treat it as not having that, but there is always some material resistance, unless it's a superconductor which we don't use in the IC business, at least not yet.

So there will be some resistance in any of these things. And the technology is developed so that any resistance in the wiring and the metal

lines is hopefully essentially negligible. You don't have to consider it.

Q So it's your opinion then that the amount of resistance both in the wire itself and in the points of contact of the pad is negligible?

MR. ANDERSON: Objection to form.

A In the typical case, you would want it to be. There is always going to be some resistance. There are long arguments about how much is -- is suitable. That's why the switch was made in IC from aluminum wiring to copper to lower the resistance. But you want the resistance to be as low as possible. And if it becomes too large, that can be problematic to the circuit operation.

But again, if there are special cases where that becomes an issue, they weren't in play here.

Q But the very nature of wire bonding does require adding some resistance, though you try to minimize it?

A Unless you're using a superconductor, any -- any metal line has some resistance. And

one of the things that makes semiconductors so successful is because semiconductor materials and the transistors have some degree of resistance but it's moderate, I'll use that word, because it lets you essentially treat the insulators as being perfect insulators; the metals as being perfect metals; and for your -- most of your calculations, are at least your understanding.

But any time you have any metal, unless you found some way to put a superconductor in here, then it will have some resistance. That's just the nature of physics.

Q Now, how does wire bonding compare resistance-wise to printed surface wiring?

A Are you referring to the wire -- the traces on a printed circuit board?

Q Yes.

A My understanding, and this is also in -- this is actually discussed in reference 1007, is that, essentially, if you use the same metal, that's a good way to think of this, the wider and thicker -- and/or thicker that metal is, the

bigger the cross-section, the lower the resistance will be.

So in an IC, one of the reasons you keep the metals at the bottom, like metal 1 is very narrow, because you have to thread it into very small spaces. As you move upward in the metal stack, the metal lines because wider and thicker because they were -- things are converging there. There's more current going through them.

When you go up -- when you go up to the bonding wires and you go to the package traces, those are bigger still. And so those have lower resistance than does the lower-level interconnects. And then out in the printed circuit board those, by comparison to what's going on in -- like, a 4-nanometer manufacturing process, those are huge. And so they have very low resistance compared to the wiring.

So basically, it's simple metallic physics. And the thicker and/or wider, essentially the bigger the cross-section for the same metal, the lower the resistance will be.

Sorry that was convoluted, but there's -- there's so many different levels of operation here, I want to make sure I'm complete about what is going on.

Q I appreciate that. I appreciate that.

Let's turn to paragraph 146 of your declaration. Let me know when you're there.

A Sorry, I'm there. It's -- 146 spans two pages and there's Figure 9.2 from Saint.

Q Okay. In paragraph 146, you cite a passage in Saint that says, "Wire bonding is the most common method of attaching a chip to a package."

Do you see that?

A Yes. I see that. And certainly, at the time of Saint it was.

Q Okay. Has that changed since then?

A There's so many methods used now that -- that are used. For example, if you look at your -- if you look at a microprocessor that has, I don't know, 500 pins, there's a -- those methods may not work. Wire bonding is replaced by some

other methods for those packages. But wire bonding is still very commonly used. It's the most commonly used method over time, shall we say, in the business.

Q At the time of 2018, what other methods were used to make these connections?

MR. ANDERSON: Objection to form.

A Somewhere in here, I actually have somewhere I mention some of the methods because someone mentions them. But a variety of methods like ball grid array and flip-chip, and there's a whole bunch of them. But wire bonding is still a very common base use.

And I'll also note, by the way, this confirms what I was telling you earlier. You'll notice the figure caption refers to that molten plastic that I mentioned earlier. I just noticed that in the figure caption. I just wanted to mention that since I mentioned molten plastic earlier. There -- it's right there in Saint.

Q So as of 2018, there were other methods besides wire bonding that were used to connect

packages to traces?

A There have been numerous methods for some time going back, you know, as long as I've been in the business. Wire bonding is just still the simplest method and has long been commonly used.

Q So then let's turn back to your declaration paragraph 147.

And in this paragraph you cite a microphotograph image that shows bonding wires connecting to the bond pads of an integrated circuit, correct?

A Yes. And it shows that figure which I use multiple times, appears on the next page.

Q Then in paragraph 148, you note that claim 6 of the '164 patent differs from the teachings in Saint in the light of photograph -- microphotograph image in paragraph 147 but -- because it involves the use of bond wires to connect a bond pad in one pad group to a bond pad in another group, correct?

A Yes. I note here that the -- the -- what the '164 patent is doing with the bond wires, it

doesn't discuss -- well, I guess it does discuss it, but it shows in, for example, Figure 3 using these I call them jumper bond wires where you're essentially creating a jumper bond wire between two pads rather than a pad to a package trace as is shown over on the figure on page 72.

Q Okay. So would you agree with me that Saint and the microphotograph image in paragraph 147 do not teach connecting a bond pad in one group to a bond pad in another group using bond wire?

A There's no --

MR. ANDERSON: Form.

THE WITNESS: Go ahead, Shane. Sorry.

MR. ANDERSON: Objection to form.

A There is no depiction in Saint or in this figure we're looking at here, which is why that was demonstrated with other art such as Miller and Beauchamp in my declaration.

Q So in paragraph 148 you refer to -- or strike that.

In paragraph 149, you refer to a reference

known as Miller, correct?

A That is correct. This is -- again, Miller and Beauchamp are used to demonstrate the knowledge of a POSITA regarding this particular use of bond wires.

Q Okay. And you refer to Miller and -- strike that.

Exhibit 1014 is the Miller reference you refer to?

A It should be. And it's done correctly, yes, in the production.

Q Okay. You do not list Miller as a prior art reference in any of the grounds you rely on, correct?

A I don't use it as a primary reference. I use it -- Miller and Beauchamp were used to demonstrate the knowledge of a POSITA, that this was well known in the art at the time of the '164 patent.

Q Okay. But you don't list Miller in your grounds explicitly, correct?

A I don't. I didn't think it was necessary.

Q Okay. In paragraph 150, you refer to the Beauchamp article, correct?

A I guess, the yes -- well, if we want to say it in French properly or in English, but I think "Beauchamp" is sufficient. I believe the gentleman actually is Canadian, but regardless.

Q Okay. And Beauchamp is Exhibit 1016 in this proceeding?

A Yes, it is. And Mr. Beauchamp is actually listed as residing in Arizona, so he's -- he may have -- he has ancestry in -- in French Canada but he's not residing there now, so he probably goes by Beauchamp.

Q And you don't list Beauchamp as a prior art reference in any of the grounds you rely on, correct?

A No, I do not for the same reasons as Miller. It was included to demonstrate this was widely known in the art and would have been part of the knowledge of a POSITA in my view.

MR. WATSON: Let's pull up Exhibit 1014.

(Exhibit 1014 marked for identification.)

A I have that in front of me and I guess we're still waiting for it on the screen.

Q So Exhibit 1014 is the reference you discuss as Miller, correct?

A Yes. This appears to be the Miller reference discussed in my declaration.

Q Okay. So let's turn to paragraph 6 of Miller.

Let me know when you're there.

A I have it in front of me now.

Q Okay. So in paragraph 6 of Miller, it states, "In a typical packaged IC a bond wire connects the bond pad to a conductive leg or pin extending from the package surrounding the IC."

Do you see that?

A Where is that in the paragraph? Top, bottom? It's a long paragraph.

Q Second para- -- second sentence.

A Okay. Yes. I see that. And that is correct, that is the typical usage that we've seen in, for example, the ones we were just discussing, such as that 2010 microphotograph.

Q Okay. Then if we go to paragraph 7 of Miller, let me know when you're there.

A Okay. If you're going to quote something, let me know where in the paragraph it is.

Q Yeah. I'm going to read the first two sentences of paragraph 7 of Miller. Okay?

A Uh-huh. That's fair.

Q Okay. Miller states that, "In high frequency applications a combination of series inductances and shunt capacitances in the signal path provided by the interconnect system attenuate and distort signals. The bond wire and package leg typically contribute most of the series inductance."

Do you see that?

A Yes. And bond pads being wires, independent wires, actually will contribute inductance which is why using these kinds of integrated circuits for RF applications is so difficult.

Q So using bonding wire will contribute to the inductance of a circuit?

A It will contribute in a digital circuit that typically doesn't matter. And when you get into RF, having done RF design, you essentially have to completely redesign how you approach the entire IC from the bottom up, even have to lay the transistor out very differently.

So in high-frequency applications, that's -- that's something you would run into some of these problems he's describing.

Q So high levels of inductance is a potential problem with using bonding wire; is that fair?

A In --

MR. ANDERSON: Objection to form.

THE WITNESS: Sorry, Shane. Go ahead.

MR. ANDERSON: Objection to form.

A In the use in high-frequency RF applications and their -- you could cause them to happen in digital but it's -- it would be very difficult to cause to happen. But typically in certain RF situations you would have to worry about inductance, not only in -- in the bond wire

but in all the interconnect wiring. You'd have the inductance and you'd also have capacitance. When you go to very high frequencies particularly typically analog RF high frequencies, then you have -- you run into these kind of issues with reactances.

Q So will using bonding wire increase the inductance of a circuit?

MR. ANDERSON: Objection to form.

A Well, any wiring will -- there's inductances inherent in the entire structure of the IC at the metal levels and up into -- into the wire bonds and even further out into the package traces and things like that. So those are inherent in any of these things, just a question of when did they become enough to be something you have to worry about. And in the -- certainly the world of RF, particularly higher frequencies, these kind of reactances, capacitances, inductances throughout the entire -- the entire circuit, the entire IC, the entire package and so forth and so on becomes important.

Q So as Miller states here, the bonding wire will contribute most of the series inductance; is that fair to say?

MR. ANDERSON: Objection to form.

A Well, he says the bond wire in the package leg. And so that's -- that -- the bond wire is one part -- the package leg is the trace in the package which is a bigger piece of metal going to the pin. So those contribute to the inductance simply because of the frequency that's being used. If it was a digital -- a typical digital circuit, that would not be a factor. But when you go to the case of high-frequency RF and analog-type circuits -- sorry, signals that are being processed, then it becomes more of an issue which is why it's so challenging to do those things having --

Q I understand. I understand.

So just to be clear in Miller, where it says "the bond wire and package leg typically contribute most of series inductance," you don't disagree with that statement?

A I only will clarify that you can't understand that statement without understanding the sentence before, that he's speaking about high-frequency applications.

Q Okay. That's fair. All right. Let's pull up Exhibit 1016.

(Exhibit 1016 marked for identification.)

MR. ANDERSON: We've been going for another hour. If you want to find a good kind of breaking point to take a break, that would be awesome.

MR. WATSON: Yeah. Let me go through -- through this and then we'll --

THE WITNESS: I can last as long as it doesn't go more than 10 or 15 minutes. That's all.

MR. WATSON: Okay. All right.

Q Dr. Foty, do you see Exhibit 1016 in front of you?

A Yes. And I believe this is what we call the Beauchamp reference.

Q Okay. Let's turn to paragraph 27 of the

Beauchamp reference.

A I have that in front of me. And again, it's a lengthy paragraph so if you're going to quote something from it, could you just let me know where in the paragraph it is so I can follow along?

Q Okay. Let's go to the last sentence of paragraph 27.

Do you see that?

A I see that. Yes.

Q The last sentence of paragraph 27 states, "This creates a low resistance connection between the bond pad 104 and the ball at the end of the bond wire 110."

Do you see that?

A I see that. And it's concluding a description of the process of putting a bond wire on a bond pad that you see above.

Q What is the low-resistance connection that's being referred to here?

A If we go back, actually, I think that if we go back to the figure we were looking at a

minute ago, I think this is -- I think the figure from that 2010 article, I'll try to find that, but if you have a page I could go to, I could explain this much -- yes, I'll go to page 72 of my declaration to explain this because you can see it here.

When you do this type of bonding, you can see what happens, that there's a ball created essentially. And that's why the pad has some size to it, is to accommodate that ball. And essentially by putting that ball and spreading the metal out, you reduce the contact resistance between the ball at the end of the bond wire which the tool creates for you and the bond pad underneath.

That's why you can see, as you look at these, you can literally see what looks like a ball in that microphotograph, and that's why that's there.

Q So the connection between the ball and the bond pad has some level of resistance; is that fair?

A Unless someone's found a way to use a superconductor, there will be resistance of some sort. Hopefully, the idea is to make it small enough that it's negligible or can be neglected.

Q And so going back to Beauchamp paragraph 27, do you have that in front of you?

A I have that on the screen and I have that also in my paper copy.

Q So the low-resistance connection here is not referring to the connection between the two pads, correct?

A No. But I don't know if Beauchamp discusses this, but if you can create a low-resistance connection between the bod pad and the end of the bond wire, that will apply if you have another pad next to it. Because you have a low-resistance ball bond to the band pad, one. You have a low-resistance connection between the other end of the wire and the ball at the end of that piece of wire at opposite ends of the wire. So you have a low-resistance connection at both ends of what I call the jumper bond wire.

Q So -- so let me break that down a little bit.

So you have a resistance in the connection between the bond pad and the ball at the end of the bond wire, correct?

A There would be some, hopefully, very small resistance. And since bond wiring works so well at resistance, has to be small for ICs to use it and work properly.

Q Okay. And so you would have the ball at the end -- both ends of the bond wire, correct?

A If you're using what I called a bond wire jumper, then you would have a ball at each end of it. And I believe if you look at Miller's figures, Miller actually shows in -- because his artwork, he actually shows the little ball at each end of a jumper, a bond wire jumper.

Q So each of those balls and their connections has some level of resistance; is that fair?

A Some. But as Beauchamp says, it's a low-resistance connection at that contact.

Q Okay. And then there's some resistance that's just internal to the bonding wire; fair?

A Again, unless it's a superconductor there will be something there, hopefully negligible, and make things work and -- to make the ICs work properly it has to be considered to be -- be able to be considered to be negligible.

Q Okay. Okay.

MR. WATSON: All right. I think we've been going for a little while, so we could probably take a break here.

THE WITNESS: Okay. Ten minutes?

MR. WATSON: Sure. Let's go off the record.

(Whereupon a break was had.)

BY MR. WATSON:

Q Dr. Foty, did you talk to anyone about the substance of the testimony you've given in this deposition during the break?

A No. I just told the folks at my vet that I was tied up today but I would break away if we needed to deal with that issue.

Q Dr. Foty, for grounds one and two, you rely on Yoshinaga as the primary reference; is that fair?

A I think that's fair. I think that's the way I organized it.

Q Okay. And in particular, you rely on Figure 6 in Yoshinaga in making your obviousness arguments?

A I would say that's the key figure. I refer to other parts of Yoshinaga obviously.

Q Now, let's turn to paragraph -- let's turn to paragraph 153 of your declaration and put that on the screen.

Now, in this figure in paragraph 153, you made a number of changes to arrive at the '164 patent's claimed invention, correct?

MR. ANDERSON: Objection to form.

A Well, I don't know what you mean by a number of modifications, but I show some -- some things here that we'll discuss I'm sure.

Q You made some modifications from what is the actual figure in Figure 6 of Yoshinaga, fair?

A I did some things to it in my view based on, you know, knowledge from Saint and a POSITA of course. I didn't just pull it out of thin air.

Q So let me -- I just want to walk through those changes to understand what -- what changes you made, if that's okay.

A Well, I may dispute if you call something a change that I don't think it's a change. But regardless, we'll see what the questions are.

Q Yeah, sure. Let's go actually to page -- let's see, I guess we don't have a clean version next to the -- okay. We'll stay here on paragraph 153.

You with me?

A Yes. And okay. I have Yoshinaga, my paper copy of Yoshinaga available if I need it.

Q Okay. So in Figure 6, at the top of the figure, there's a number 3 in Yoshinaga, correct?

A In the raw Figure 6 that I'm looking at from Yoshinaga, there's a 3 in that left of the orange block pad, yes.

Q And you've -- you've changed figure -- let

me strike that.

In making your arguments, you've changed the power supply pad 3 into a reference pad labeled 5; is that correct?

A Yes. Yoshinaga actually says that he doesn't show the locations of the reference pad to simplify the drawing, is what he says.

Q Okay. So one of the changes you made was you changed the 3 into a 5; is that fair?

A Yes. This reflects the notion that the locations of the pads is what I called fungible. That the pads can be, you know, assigned differently. And so since he doesn't have specific teachings, I chose to assign a reference voltage pad 5 to that location.

Q Okay. So is it your opinion that the assignment pad listed 3 was not assigned specifically to be a power supply pad?

A No. I don't agree with that. 3 is a power supply pad but the pad could go somewhere else. It could be relocated elsewhere. And you'll see there are also a couple of other

instantiations of 3 along the left side of the figure.

Q Okay. Now, another one of the changes you made to Figure 6 is you removed the label 4 from the pad to the right of the orange area at the top of the chip.

Do you see that?

A Yes. Although the way it's drawn in Yoshinaga, that's not, you know -- that's not changing the pad, just removing the points here to focus instead on the reference pads.

Q Okay. And another one of the changes you made to Figure 6 is you labeled the pad immediately to the right of the orange area at the top of the chip with a 6, correct?

A That's correct. Again, the pad locations are fungible. Yoshinaga says he doesn't show where they can go and so there's no reason you couldn't put the pad 5 and the pad 6 as I've shown them in this figure.

Q Another one of the changes you made to Figure 6 is you changed the label on the pad above

the orange area on the right side of the chip from a 4 to a 6, correct?

A Yes. Again, and that comports with what I said a moment ago about the fungibility of the pads in Yoshinaga, saying he doesn't show where they -- the reference pads would go to simplify the drawing, is literally what he says.

Q Okay. And another one of the changes you made to Figure 6 is you changed the label on the pad below the orange on the right side of the chip from 58 to circuit 67 GND; is that correct?

A Yes. That's what that shows.

Q And each of those changes you made because, as you said, a person of ordinary skill would understand that pads are fungible; is that fair?

A Well, I use the word "fungible." I don't know if that -- if that would be recorded as appropriate. But basically, it just means that Yoshinaga says that the pads could be moved around or he says he doesn't show them. So a person of skill in the art would be trying to find places to

put those pads perhaps. And there's no restrictions on where the POSITA could put the reference -- voltage reference pads, the low-voltage, potentially, reference pads.

Q Can you -- if you have Yoshinaga in front of you, can you point to me where he says that the pads could be moved around?

A I don't know if he says that explicitly but this is why the combination with Saint because Saint does say that. Saint says the -- the pad assignment, shall I call them, what they're going to connect to, can be moved around to optimize the design as the designer sees fit.

Yoshinaga does say in paragraph 78 that the reference potential pads are not shown to simplify the drawing. That's what he says. So it's not in Yoshinaga the combination with Saint. Saint teaches explicitly that you can move the pads around in the design -- call them the pad assignments. You're not physically moving the pad, but you're changing the assignment of the pad, what it's being bonded to.

Q So Yoshinaga does not teach that you can assign pads differently?

MR. ANDERSON: Objection, mischaracterization.

A He doesn't explicitly say it. But Saint teaches it and a POSITA would know that from Saint, that it's common practice to change the assignments to optimize the design. And Saint has expensive discussions of that.

Q Okay. So the idea that you can change pad 3 to pad 5 comes from Saint, correct?

A Excuse me. It comes explicitly from Saint. But again, I regard that also as being something a POSITA would know because what Saint describes is well known, that you can change the assignments of the pads as you see fit to optimize the design such as which pads are closest to which blocks and the functionality needs we were talking about earlier.

Q The idea that you can change pad 3 to pad 5 is not explicitly stated in Yoshinaga, correct?

A It's not explicitly stated, but it

certainly is in Saint, and as I said in my experience, it's common knowledge you can do that.

Q I appreciate that. But I have asked you a yes-or-no question.

Is the idea that you can change pad 3 to pad 5 explicitly stated in Yoshinaga?

MR. ANDERSON: Objection to form.

A Yoshinaga is silent on that. He doesn't discuss it.

Q Okay. Let's turn back to the Figure 153, the figure that you have in paragraph 153.

Do you see that --

A I'm sorry, when you said Figure 153, that was confusing.

Q Yeah, sorry. Let's turn back to the figure that is in paragraph 153 of your declaration. Okay?

A Okay. I'm back there now. Sorry.

Q Okay. Another change you made to Figure 6 is you added a jumper bond wire to connect reference pad 5, 6, and 67, correct?

A There are two jumper bond wires shown, one

at the top connecting between what I have labeled as pads 5 and 6 at the top, and there's another one shown on the side between the pad labeled 6 and the pad labeled, circuit 67 ground. Yes. Those jumper bond wires are added.

Q So Yoshinaga does not disclose using jumper bond wires to connect reference pads, correct?

A Yoshinaga does not disclose that. Again, knowledge of a POSITA as reflected in Miller and Beauchamp is the argument.

Q Okay. Let's turn to paragraph 238 of your declaration.

A Okay. I have paragraph 238 in front of me. It's not on the screen yet.

Q Yeah. Let me turn that on the screen just so we're on the same page. Okay.

Dr. Foty, do you have paragraph 238 in front of you, in particular the figure there?

A I have the paragraph 238 and the figure is on the following page.

Q Okay. Another change you made to Figure 6

of Yoshinaga was you added a common rail which is in red in the figure in paragraph 238, correct?

A Yes. This is a common rail or a common bus running around the outside which I believe is a combination from Exhibit 1007 as we're calling it.

Q Okay. So Yoshinaga does not explicitly disclose a common rail around the circuit, correct?

A Yoshinaga has no discussion of what goes on beyond the pads, so it can't come from Yoshinaga but something has to go on beyond the pads obviously.

Q And another change you made to Figure 6 was you added a bond wire connection between reference pads 5, 6, and 67 to the common ground rail you added, correct?

A That's correct. Again, that comes from the combination of Yoshinaga and reference -- sorry, Exhibit 1007.

Q Okay. So Yoshinaga does not explicitly describe connecting bonding -- strike that.

Yoshinaga does not explicitly describe using bonding wire to connect reference pads to the common ground rail?

A As I said Yoshinaga, doesn't go beyond the pads, so this has to be combined with another reference to get this. Yoshinaga does not go to that level of design.

Q Okay. Okay. Other than the changes we just discussed, are you aware of any other changes to Yoshinaga Figure 6 that you made to show obviousness of the claims of the '164 patent?

A I don't -- well, there's labels on here that, for example, it shows some -- that there's magenta boxes at the top showing, you know -- showing a pad group. I arbitrarily -- semi-arbitrarily surrounding some pads, but I believe everything here is an annotation. It's not actually modification, just for what that's worth, the coloring and things like that.

Q Okay. So you -- another change is you added the pink box -- boxes shown in paragraph -- the figure in paragraph 238?

A Well, they're -- they're annotations. They don't affect the design. Everything else is like those and the coloring-in of the yellow and the green and the blue and the orange areas, those are annotations. It doesn't represent any change to Yoshinaga. It's just a highlighting of things in Yoshinaga.

Q Fair. So the coloring was added by you, correct?

A Yes. It was added by me, although one of the folks at Orrick might have done the actual coloring. But this is something under my direction because it's just -- again, this the annotation in Yoshinaga is typical for patents is black and white and it's a little easier to see what I'm talking about when you color it up like this.

Q All right. Let's turn to paragraph 144 of your declaration. I'm going to bounce around for a second here.

A No problem.

Q Do you have paragraph 144 in front of you?

A Sorry, yes, I do.

Q Okay. Paragraph 144 discusses limitation 6d of the '164 patent, correct?

A I believe that was 6d as in delta, not 60, so the record is clear.

Q Yes. 6d. Thank you for clarifying.

A There's no claim 60, but I wanted to make sure that the record didn't somehow show a claim 60 that none of us know about.

Q Thank you. Limitation 6d is a plurality of bonding wires configured to connect to another of the plurality of pad groups.

A I think you dropped a word in there, but it's "connect one to another of the plurality of pad groups" is the -- what the element actually says.

Q Thank you. Appreciate that.

A Whatever -- whatever is written on the screen here is what the claim element says I think is the bottom line, for the record.

Q Okay. Would you agree that limitation 6d of the '164 patent is not taught by Yoshinaga?

A It's not --

MR. ANDERSON: Objection to form.

THE WITNESS: Sorry. Go ahead, Shane.

MR. ANDERSON: Objection to form.

A I would agree it's not explicitly taught. But again, I regard that as being well known in the art.

Q And you don't say here that limitation 6d is obvious in view of Yoshinaga and Saint, correct?

A No. Saint is combined in just to show some general ideas about wire bonding, but it's mainly combining Yoshinaga and the knowledge of a POSITA as the argument for this claim element.

Q Let's turn to paragraph 249.

A Sorry, I'm there and you're there, too, I see.

Q So paragraph 249 relates to limitation 1d of the '164 patent, correct?

A Yes. That's what it says in the -- should the element is -- on the previous page, it says what the element is if we need to see that.

Q So limitation 1d of the '164 patent is "a common ESD bus adjacent to the plurality of pad groups; and," correct?

A That is correct.

Q Yoshinaga by itself does not disclose the limitation 1d of the '164 patent, correct?

A Not explicitly. Because as I said earlier, Yoshinaga doesn't discuss what's going on beyond the pads. And obviously, something has to be going on.

Q Okay. So Yoshinaga doesn't disclose the common ESD bus; is that fair?

A Not explicitly because it's outside the over of what Yoshinaga teaches.

Q Okay. Instead, you argue that Yoshinaga in combination with Exhibit 1007 renders obvious claim limitation 1d?

A Yes. Because as I said, Yoshinaga does not go out beyond the pins. And obviously, in a real design you would have to go beyond the pins to connect things together. And that includes having to connect the ESD discharge pads in

Yoshinaga to something outside the pads of Yoshinaga.

Q Let's turn to paragraph 254.

A I'm there and you're there, I see.

Q Paragraph 254 discusses limitation 1e of the '164 patent, correct?

A It appears to discuss 1e as, in echo, yes.

Q Limitation 1e of the '164 patent is not taught by Yoshinaga, correct?

A Yes. It is for the same --

MR. ANDERSON: Objection to form.

THE WITNESS: Sorry. Go ahead, Shane.

MR. ANDERSON: Objection to form.

A It's not taught in Yoshinaga because, again, Yoshinaga does not go outside the pads. And in a real situation, that would be to have addressed and so it's done by combination.

Q Yoshinaga also does not say anything about using bonding wire, correct?

A Yoshinaga, again, doesn't go beyond the pads. He doesn't discuss any issues of bonding which, obviously, in a real product would have to

be done.

Q Would you agree with me that the pads -- strike that. Strike that.

But Yoshinaga does not teach using bonding wire to connect pad groups, correct?

A Yoshinaga teaches nothing about bonding wires of any -- in any form, way, shape, or form so Yoshinaga would not, does not disclose that. He stops -- his discussion stops at the pad.

Q Let's turn to paragraph 269.

Are you there?

A Sorry, I'm there. I was just reading the claim and things like that.

Q Paragraph 269 discusses claim 3 of the '164 patent?

A Yes, it does.

Q Yoshinaga does not teach the limitation of claim 3, correct?

A Again, for the same reasons, Yoshinaga does not teach this for the reasons that he teaches only out to the pads. He doesn't teach anything beyond that, and that would include

common ESD bus. He doesn't discuss that at all in any form.

Q Go to -- let's go paragraph 284. We can go paragraph 274 first. Sorry.

A Okay. I see paragraph 274, which is the introductory paragraph for claim 4, if that's what you're pointing to.

Q Yes. So this paragraph discusses claim 4 of the '164 patent?

A Yes, it does.

Q Yoshinaga does not teach claim 4 of the '164 patent either, correct?

MR. ANDERSON: Objection to form.

A Well, again, it's by combination with the other references. So Yoshinaga does not teach this explicitly for the same reason. Yoshinaga does not teach out to the level of what's going on beyond the pads for the ESD bussing to get to the -- to get, for example, to the ground where the actual ESD energy of an event is sunk.

Q Okay. Let's turn to paragraph 134 of your declaration.

A I'm there, and I see you're getting there. There we go.

Q Okay. When you are a -- actually, let's go to paragraph 136.

When you are identifying the claim plurality of pad groups for limitation 6c-1, you are not identifying the power supply pads 3, 4, and 58, correct?

A Well, I believe this is constructed is I'm using the -- the modifications to Yoshinaga of identifying the pads differently. But regardless, of how the pads are identified, it seems pretty -- pretty straightforward that as the '164 patent, how it defines pad groups are in Yoshinaga no matter what assignments are made to the various pads.

Q But for purposes of disclosing a plurality of pad groups, you point to the reference potential pads as fulfilling that limitation?

A Well, I point to the -- the two pads as they appear in the figure on page 68. The pads themselves are disclosed by Yoshinaga in that

form. So regardless of what the label is, there are pads there and no matter what the pad assignment is, Yoshinaga discloses pad groups in -- in the way that the '164 patent defines what a pad group is.

Q If that's the case, why did you change the power supply group pad 3 to -- to the reference potential pad 5 in the figure in paragraph 13?

A Consistency with the embodiments I've been using, with the modified embodiment. I could have used the original Yoshinaga figure here and it would have produced the same conclusion. It's just this is a choice of the one we've been using already that's already annotated with all the colors and everything.

Q Okay. Now, you would you agree with me that Yoshinaga describes an integrated circuit chip and integrated circuits within that chip?

A I'd have to see what Yoshinaga calls it, but I would generically agree that Yoshinaga shows here is an integrated circuit with circuits inside it and it includes going all the way out to having

the pads around the edges of the IC, the bonding pads.

Q Is there any teaching in Yoshinaga about packaging?

A Yoshinaga is completely silent on packaging. But, of course, you would have to have packaging to do something with this IC. So you would have to combine Yoshinaga with a package to make a real product. And again, to sink for example -- you have to have a path somewhere to go off the chip in order to sink, say, the energy of an ESD event somewhere. It would have to go off this. He discusses ESD and designing the chip for the ESD, but he doesn't discuss the necessary part of it is not part of his -- what he's teaching of -- that has to go somewhere to be sunk, that energy. The sewer pipe's got to go somewhere basically.

Q So what you're saying is Yoshinaga does not disclose the plurality of ESD buses that are connected to the pads; is that fair?

A He doesn't disclose anything being

connected to the pads, per se. He just shows -- he stops at the pads in IC.

Q Okay. Let's pull up Yoshinaga actually. Let's go to Exhibit 1006. Let's pull up Exhibit 6.

A Yeah. I've got it on paper.

MR. WATSON: Can we pull up Exhibit 1006 on screen?

REMOTE TECHNICIAN: I apologize. Let me fix this. Something went wrong here. Just a moment, please.

It should be back now.

THE WITNESS: There it is, that's -- okay. It's back. That is correct. I saw the highlighting was on 1016 for a minute there and I thought something wasn't right. But this is 1006, the English translation of the Yoshinaga reference that was original in Japanese.

Q Let's go to Figure 6 of Yoshinaga.

Do you have Figure 6 of Yoshinaga in front of you?

A I have it on the screen. I also have it

in my paper copy.

Q So Figure 6 is a diagram of a circuit chip, correct?

A It's a chip-level depiction of what Yoshinaga is teaching with -- with what Yoshinaga says, for example, that he doesn't show the reference pads to simplify the drawing, as he calls it.

Q So Figure 6 of Yoshinaga does not show reference potential pads, correct?

A It doesn't show them. And he flat-out says he doesn't show them.

Q Okay.

A But they would have to be there in a real design. If this were going to be a real chip, you would have to include them somewhere.

Q So is it possible that Yoshinaga could have reference potential pads in the space between power supply pad 3 and 4?

MR. ANDERSON: Objection to form.

A Yoshinaga draws the pads for whatever particular reason. And so my take would be this

is exemplary, so there's no particular restriction where you would put those pads. So you would put them -- you would either add pads and expand this to accompany -- depends on how many pads the specific IC requires.

So the pads could be put -- could put in other places such as -- we do have a figure in there where we show two purple pads added at the bottom of the left side -- lower left corner and the lower right corner.

Q So there could be reference potential pads between Figure -- between 3 and 4 here at the top of Figure 6?

MR. ANDERSON: Objection to form.

A It's hard to say because, you know, he's got the gap between the buses so you probably wouldn't want to put something there the way he structured it, but he doesn't discuss that. It's -- his figure is exemplary and so for a real IC, if you needed more pads you would have to expand the footprint to include more pads based on what the ground rules are.

Q So Yoshinaga doesn't say one way or another whether you could have reference potential pads in the space between power supply pads 3 and 4?

A He's silent on that matter.

Q Now, Figure 6 does show power supply pads, correct?

A He does identify locations where you could put in -- put in power supply pads. He identifies those to show that you would connect to the particular rails for the power supply.

Q And how many power supply pads does Figure 6 show?

A At least 7. I'd have to look at what the other numbers are, but -- actually, let me check what -- what he says those are.

He identifies 3, 4, and 58 as power supplies so that would be is 1, 2, 3, 4, 5, 6, 7, it looks like he has nine identified power supply pads in this particular depiction.

Q Okay. So Figure 6 shows nine power supply pads; is that fair?

A As depicted, yes. Interestingly, from this depiction he has nine power supply pads and no reference voltage pads in this depiction.

Q So what are the other pads that are depicted here?

A Let's see, he does not label any other pads, so the pads could be anything he doesn't mention. They could be reference voltage pads. They could be -- obviously, there has to be some signal pads but the signal pads would depend on the circuitry. So that's why this figure is -- is basically exemplary because he just shows the pads being around the edge and the pads are not -- he has something he mentions about the pads could be added for particular things, I believe. I'm not sure if that's in there or not, but he only shows on the pads -- he only actually points to power supply pads. No signal pads pointed to, no -- no reference voltage pads pointed to.

Q Yoshinaga is silent on the purpose of the pads shown in Figure 6 other than those labeled with a 3, 4, or 58?

MR. ANDERSON: Objection to form.

A Those are the only pads for which he applies an explicit description. But obviously, if this was a real design, you'd have to have reference voltage pads and signal pads, etcetera, etcetera.

Q What's the purpose of the power supply pads in Yoshinaga?

A The generic notion would be that the power supply pads are where a power supply voltage is connected in so that the power supply bus which, I believe, is, like, on the left -- 17, I think is -- yes, 17, 18, and 59 are the inner of the two, you know, hash-marked lines. And those are, essentially, the power supply buses.

So the -- that -- the power supply lines would be energized when the chip is turned on so that the power supply voltage would be -- would be what's on those as the voltage there.

Q So the more power supply pads there are, the more power the circuit would have?

MR. ANDERSON: Objection to form.

A I don't think Yoshinaga discusses that detail, but if -- basically, the way that would work would be if you have the supply voltage, the voltage would be the same. It has to be. I mean, the bus is shorted together. It's a piece of metal. You can't have much voltage on that.

So having multiple power supply pads to that might, for example, allow more current to flow through by having the current go through multiple. If the particular IC has -- is current hungry, then you obviously have more pipes. You get more water into the -- into the pool, so to speak.

Q So the more power supply pads you have, the more current flows through the current; is that fair to say?

A I think --

MR. ANDERSON: Objection, form.

A I'd say it's the opposite. The -- you -- you create the number of power supply pads for many reasons and one of the reasons might be that you need to have higher current requirements met,

and a single pad might not meet that. So you would use multiple pads in order to provide -- essentially it's like having multiple pipes in order to get water into the pool faster. That would be a higher current. So it's the design demand for higher current that would cause you to have more pipes essentially.

Q Got it. So the more power supply pads you have, the more conduits you have to the current; is that fair?

A It would be -- it would make that possible. It depends on what the demands are. If the chip is sitting there not doing much and it's only consuming a low amount of current, the pad -- the extra pads are not needed. It's a question of what the requirements are.

If the requirements -- if there are high current requirements, one way you could address that would be with multiple pads to have multiple, essentially, pipes flowing in. So you have more pipes, you are -- you could bring water in more quickly which is a plumbing way of saying that the

current would be higher. You could -- you could support a higher current draw. Let's put it that way.

Q Got it. So the more power supply pads you have, the higher current draw your circuit can sustain; is that fair?

A Again --

MR. ANDERSON: Objection to the form.

THE WITNESS: Sorry, Shane. Go ahead.

MR. ANDERSON: Objection to form.

A I say, attorneys always seem to get cause and effect backwards in this space. I've noticed that.

It's a matter of what the circuit needs. So you would design the feeds for the amount of power and the -- which is since the voltage is constant, the amount of power would be reflected in the current draw.

And so if the circuit is going to have operating situations where you need -- you might need a larger amount of current, you have to accommodate the plumbing to be able to carry that

amount of current. If you're -- if you need to fill your swimming pool up in ten minutes, you need to design for the amount of pipes to have water flow in that would support a ten-minute fill. That -- it's the same idea here.

It depends on what the -- the current draw would look like in the circuit in the design level. So you have the -- the cause is the need for an amount of current and the effect is the number of -- of pipes coming in through the various pads to the bus. That's what the cause and effect are.

Q What would happen if you had less power supply pads than the need for current required?

A Well, then the circuit might have operating problems because the current wouldn't be able to -- the current draw wouldn't be met and you could -- for example, you could have voltage droop. The voltage would droop because you can't maintain the voltage on the bus.

Q Now, Figure 6 shows three different circuits, correct?

A I assume you mean the circuit blocks that are there.

Q Yes. That shows three different circuit blocks?

A I believe that it does. If you mean the one large rectangle on the left and the two smaller rectangles on the right, I believe Yoshinaga identifies those generically as circuit blocks. And he has some language I think that he's -- they could be a variety of things.

Q So let's go to the labeling.

So in paragraph 88, it labels 1, 2, and 67 as the circuits.

Do you see that?

A It just calls them circuits. Yes.

Q Okay. Let's go back to Figure 6 then. So on Figure 6, circuit 1 is the circuit on the left side of Figure 6, correct?

A Yes. He has the 1 and the 2 right down the middle alley there. If anyone is looking for it, it's a little hard to find.

Q Okay. So 1 is on the left, correct?

A Yes. And 2 is on the right. And he -- there 67 identifies the lower-right block. So those are his circuit blocks in this exemplary depiction.

Q And reference line 19 is in circuit 1, correct?

MR. ANDERSON: Objection to form.

A I would not agree it's in circuit 1. It's the ground rail for the circuit block 1.

Q So let me -- let me change my question.

Reference line 19 is the ground block for circuit 1?

A It's either the ground block or Yoshinaga doesn't call it a ground. He calls it the reference potential, which one of skill in the art would know that's -- essentially based on the way these things work, it's at least the low voltage. VDD is the high and VSS is the low. So reference potential is the low side of the voltage in the circuitry.

Q So reference potential line 19 is the reference potential line for circuitry 1?

A Yes. It's the reference potential bus, as it were.

Q Okay. And reference potential line 20 is the reference potential line for circuit 2?

A It's the reference potential bus line for 2, the low voltage bus line. I'll agree with that.

Q Okay. And reference potential line 60 is the reference potential line for circuit 67?

A It's the low -- reference potential low voltage bus for circuit block 3 in this depiction. Yes.

Q Now, in Figure 6, there is no connection shown between reference lines 19 and 20, correct?

A Yes. They're kept separate by design.

Q And there's no connection shown in Figure 6 between reference lines 20 and 67, correct?

A Sorry, there's no reference line 67.

Q One second.

A You said 67, correct? Because that's not a reference line. That's a circuit block.

Q 60. Sorry let me -- let me repeat my

question, okay.

There's no connection shown in Figure 6 between reference lines 20 and 60, correct?

A That is correct. Those are separate buses.

Q Okay. And there's no connection shown between reference lines 19 and 60 in Figure 6, correct?

A No. Again, at this level, these are separate buses inside the IC.

Q Okay. Now, let's turn to paragraph 81 of Yoshinaga.

Are you there?

A I'm there, yes.

Q Okay. In Figure 6, circuit 67 connects to circuit 1 in only two locations, correct?

A Well --

MR. ANDERSON: Objection to form.

A He doesn't say "only." He says circuit 67 is connected at two locations to circuit 1.

Q Okay. So circuit 67 is connected to circuit 1 in two locations in Figure 6, correct?

A That's what he says, and that's what the figure shows. Yes.

Q Okay. In Figure 6, circuit 67 connects to circuit 1 by signal line 56(3), correct?

A What are you pointing to here? It's not --

Q Let's go to paragraph 82. Sorry.

A Okay. I was looking at 81 and I didn't see that. I didn't see thinking there, so...

Q Yeah. Let's go to paragraph 82 of Yoshinaga.

Let me know when you're there.

A Yeah, I'm there. I just was -- I heard something I didn't see on the screen. That's why I asked.

Q In Figure 6, circuit 67 connects to circuit 1 by signal line 56(3), correct?

A Well, he refers to these boundary portion in the full sentence. He says signal boundary portion 15(3) and 67 and signal boundary portion 16(3) in circuit 1 are connected by signal line 56(3). So there are portions that are connected

between the two.

Q So one of the connections between circuit 67 and circuit 1 goes through signal line 56(3), correct?

A One of these what he calls the boundary portion signal goes through that, yes.

Q And if you turn to paragraph 83, let me know when you're there.

A I have it.

Q In Figure 6, circuit 67 connects to circuit 1 also through signal line 56(4), correct?

A Well, again, the full phrase in Yoshinaga refers to the signal boundary portions but that is provided by what he calls connect -- a signal line 56(4).

Q So according to paragraphs 81, 82, and 83, two -- the two connections of, circuit, 67 to circuit 1 are through signal lines 56(3) and 56(4)?

MR. ANDERSON: Objection to form.

A He specifically refers to what he calls the signal boundary portion. He doesn't refer

generally. He refers to these connections you described being between the signal boundary portions in 67 and 1, so those -- the connections --

Q Let me -- apologies. Let me try to clarify my question.

So in paragraph 81, it says circuit 67 is connected at two locations to circuit 1, correct?

A Yes. There are connections between those two circuit blocks. That's what he says there.

Q Where are those two circuit connections?

A Well, he refers to the signal boundary portions of the circuits connecting to each other. So the signal boundary presumably is the -- some sort of -- something at the edge of the block which has signal and could process a signal, and the same over in circuit block 1. And those are connected by the signal lines that we see there, the 56(3) and 56(4) we were just discussing.

Q So the two connections of circuit 67 to circuit 1 are through -- one is through signal line 56(3) and one is through signal line 56(4)?

A To the extent the signal boundary portions are part of it. He specifically identifies signal boundary portions, so I don't know if that means there could be other connections. But he specifically refers to these signal boundary portions.

Q Let's turn to paragraph 76 of your expert report.

A You mean my declaration?

Q Of your declaration, yeah. Apologies.

A I said, I'm not trying to be flippant. I just want to be sure that no one is going off looking for an expert report that doesn't exist.

Paragraph 76, you said?

Q Let's start with 75 actually.

A Okay.

Q Paragraph 75 in your expert report.

A Okay. I'm at 75.

Q Okay. So in paragraph 75, you discuss Figures 3 and 4 of Yoshinaga, correct?

A I actually discuss, 2, 1, and 3 in that paragraph. I don't see a reference to Figure 4

there.

Q Okay, fair. So in paragraph 75 you refer to Figures 1 through 3, is that fair?

A They're not referred to in 1-2-3 order, but 1, 2, and 3 are the three that are actually mentioned in paragraph 75.

Q Now turn to paragraph 76.

A Okay. I see paragraph 76 which then refers to a paragraph on the following page.

Q So paragraph 76 says, "Yoshinaga combines these disclosures together into an IC embodiment in Figure 6," correct?

A That's what it says and I -- that's what Yoshinaga teaches.

Q So does Figure 6 include the embodiment shown in Figures 1 through 3?

A It could include any of those as circuit blocks.

Q So Figure 6 could include any of the embodiments showing in Figures 1 through 3?

A As far as what I can tell from what Yoshinaga teaches, yes. The -- some of the patent

numbers, of course, correspond to each other as well.

Q Okay. Let's turn to Figure 1 of Yoshinaga now. Let's go back to -- to Exhibit 1006.

And if you don't mind I'm going to rotate the figure on the screen because it's hard to see it with the side view.

A I've already rotated the page on my desk, so...

Q I figured you already have that figured out. All right.

Do you have Figure 1 in front of you?

A Just, again, as we acknowledge that by flipping it this way, unfortunately, the -- we're going from right to left, but, again, this is a Japanese patent, so...

Q Okay. Now, in the diagram in Figure 1, what are the squiggly lines labeled 21 through 24?

A 21 through 24 are what Yoshinaga describes he's -- he's saying those lines have resistance. That's what the -- that's what the actual specification says and he depicts that by showing

a resistor. There's not a physical resistor there. The line has resistance, as to what he describes it.

By squiggly lines, I assume you mean what I think any POSITA or engineering student would recognize as a symbol of a resistor. And he says those lines have resistance, so he's putting a resistor in but he doesn't mean it's a physical resistor in one place.

Q Okay. In Figure 1, there's some boxes labeled 7 through 10 with arrows pointing in two ways.

Do you see those?

A Yes. I see those boxes, yes.

Q What are those boxes?

A My understanding are each of those boxes is a little circuit block that has two diodes that are connected in parallel pointing in opposite directions. I believe that's what that symbol is trying to convey.

Q Okay. Now, in Figure 1, take a look at -- at what's marked Number 17.

Do you see that?

A There's a line there, yes.

Q What does the line signify?

A Let's see what Yoshinaga says it is. I think I know, but let's see what he says.

Q Okay.

A He calls it a power supply line, meaning it's a wire. It's a wire, but it's the line goes that -- that line from pad 3 would be, in this depiction, would be energized from the voltage on pad 3 when a voltage is applied there.

Q Okay. So what do the two dots mean in these -- what do all the different dots mean on this diagram in Figure 1?

A What do you mean by "dot"? Do you mean at the -- where there's a -- there's a node of wires connecting together?

Q I mean, if you look at 17, there's a dot, then a line, then a dot.

What do the dots mean?

A The dots mean those are a node where essentially two wires connect together.

Q Okay.

A Or similar on, you know, like an IC, it would be a metal line or something, but those are essentially -- essentially, there's topological wiring description of what's connected to what.

Q And are those wires made of the metal top layer metal that we discussed before?

A I don't know if he says that or not. Three -- the pad would probably connect to the top metal, but he doesn't show anything about what happens as you move from the pad inward. And so presumably to go from the pad down to an actual transistor and a circuit, you would have to move down by vias and other metal lines to the bottom of the -- the material stack of the -- of the -- of the IC to get to the actual components at the bottom.

Q Okay. So are the wires depicted in Figure 1, are they one of the different metal layer wires that we discussed before?

A They would be comprised of the integrated circuit metallization in some way, shape, or form.

Somewhere between pad 3 and any component down in the silicon would have to step all the way down through the metal layers to get from the pad down to the silicon level. And that would depend --

Yoshinaga is silent on processes and what might be used. But just generically, you would have to move from the pad down to the silicon through the metallization of the IC. And that might involve going down through vias to a lower metal layer and continuing that process.

If you had 16 metals, you would have to step all the way down from the pad going to metal 16, going down to metal one which contacts something in the silicon.

Q So would you agree with me that typically the pads here would be connected via the top later of the metal, top metal layer?

MR. ANDERSON: Objection to form.

A I would only agree that the extent that somewhere between the pad and what goes to the circuitry, you have to go to the top metal at some point because that's what the ground rules demand.

I mean, basically it's a stack and the pad's at the very top. So the pad can't connect directly to a lower metal layer. It has to connect downward through the top metal and downward from there.

So pad 3 to connect in would have to connect to the top metal in the conventional use of this in integrated circuit engineering, but then where it would step down to get to lower-level components, Yoshinaga is silent on that level of detail.

Yoshinaga shows the pad connects to components. And so somewhere from the top metal down to the bottom metal, there has to be some -- some -- step -- you know, has to go through those layers but where that happens, Yoshinaga doesn't address that.

Q So the connection between pads 5 and 6 would have to go through the various metal layers; is that fair?

MR. ANDERSON: Objection to form.

A It's -- it's hard to say because 5 and 6

are directly connected to each other. So 5 and 6 could be connected to each other as depicted here by the top metal layer. That could be done because it's pad to pad. When you're going to go down into the -- you'll see, like, going into the circuit block 13 presumably to go from -- from that line, I believe, it's 19 connecting across there, you would actually have to step down in the metal layers to get to the bottom to talk to any of the actual in-silicon components.

But the line between 5 and 6 you see there which goes all the way across and shows a direct connection, it could be done in a top metal. Whether or not that's advisable or not would be a design choice.

You could do it at any metal level actually; you just have to optimize the design for where you wanted to do it or use one of those jumper bond wires to do it.

Q So 5 and 6 could be connected to each other as depicted here by the top metal layer; is that fair?

A It's one of numerous options, all the way from metal one up to the jumper bond wires to make that connection.

Q Okay. In Figure 1, are 5 and 6 adjacent to ESD buses?

A Saint is silent on that level of detail. This is a -- at least Figure 1, this is what I earlier call a topological depiction, not a physical depiction. So all he's showing here is the -- what's there and how they're topologically connected together. What are the components, what components are wired to each other. It's a purely topological description.

Q So Yoshinaga Figure 1 is silent about whether 5 and 6 are adjacent to ESD buses?

A It's silent by design because it's simply -- as I said, it's simply a topological depiction. It has nothing to do with any physical location of anything.

Q So the Figure 1 is a topological depiction that does not show whether 5 and 6 are adjacent to ESD buses?

MR. ANDERSON: Objection to form.

A By design, it doesn't. It simply does not even -- this diagram does not even contain any information of that sort. Figure 6 for example, actually shows where things are put in a physical design type of -- the physical design you do to actually instantiate the topological depiction into a real IC where you actually have to put things in real places and form things in real places.

Q In Figure 1, is there a saved area as discussed in the claims of '164 patent?

A Well, again, this is a topological depiction so it has no physical information at all in this figure and you would not expect to have any here. It's a stick diagram, a topological depiction.

Q Okay. So the embodiment in Figure 1 does not show a saved area as discussed by the claims of the '164 patent, correct?

A It is --

MR. ANDERSON: Objection to form.

THE WITNESS: Sorry, Shane. Go ahead.

MR. ANDERSON: Objection to form.

A It is incapable of showing any physical design information, a saved area, placement, or anything else. It's a completely different level of abstraction.

Q All right. Let's change -- let's go to a different one. Let me reverse back our -- our Yoshinaga, if that's okay. Let's go to paragraph 61.

Are you there with me?

A I'm at 61, yes.

Q Okay. So paragraph 61 referring to Figure 3, correct?

A That is correct. Yes.

Q So on Figure 32, the reference potential lines 19 and 20 are connected through reference potential line 41 and bidirectional diode pairs 37 and 38, correct?

A Yes. That's what he says.

Q Okay. And Figure 3 does not refer to using bonding wire to connect reference potential

lines 19 and 20, correct?

A Well, again, this is -- Figure 3 is a completely topological depiction. It's incapable of discussing that level of detail. It simply shows the two things connected together. It's silent on the method and -- of the many potential methods that could be used to provide that connection.

Q Now, looking again at paragraph 61, do you still have that in front of you?

A I can flip back to that.

Q Paragraph 61 of Yoshinaga, sorry.

A I'm there.

Q Okay. Do you agree that Figure 3 helps avoid noise due to the bidirectional diodes?

MR. ANDERSON: Objection to form.

A I would agree and, as I said earlier -- well, I may have said earlier but I'll say it now, this is the same thing that's taught in Exhibit 1007 for the same reasons.

Q So Figure 3 avoids noise due to the use of bidirectional diodes; is that fair?

A That's not what it says actually. It says it's to avoid noise between the reference potential lines, not the diodes.

Q Okay. So but you'd agree that the design of Figure 3 helps to avoid noise?

A It's one of the possible embodiments. He has, you know, four embodiments here. And in this particular one he's doing something similar that's done in reference 1007, where you push the connection further out. Which one you would choose depends on the type of circuit situation you face. You may want to connect them directly as shown in Figure 1 or you may want to push them out further as is shown in Figure 3. Again, it's a design choice based on the type of circuitry and the type of application you would be doing.

Q But I'm just asking you a yes-or-no question.

Do you agree that it helps avoid noise?

A Figure 3 can be used to reduce noise in certain situations. I'll agree with that.

Q I want to talk about some of the goals of

Yoshinaga. Let's turn to paragraph 5 of Yoshinaga, if that's okay.

Let me know when you're there.

A Yes, I'm there.

Q One of the goals of Yoshinaga is to avoid noise, correct?

MR. ANDERSON: Objection to form.

A Well, one of the goals of all circuit design is to avoid unwanted noise problems. And so, he discusses the use of, in particular here, I believe, the -- that diode arrangement he calls the bidirectional, provides a bit of noise immunity for reasons that are pretty clear.

Q Okay. So one of the specified and explicit goals of Yoshinaga is to avoid noise; fair to say?

MR. ANDERSON: Objection to form.

A Well, he uses the bidirectional diodes as a way to reduce noise. I'll agree with that because that's what he says there. It's one of the things he's trying to do is why he adds those bidirectional diodes. They provide -- they

basically screen out the voltage noise below a certain voltage level. That's what that diode arrangement does.

Q So one of the things Yoshinaga tries to do is avoid noise?

MR. ANDERSON: Objection to form.

A I don't know if "avoid" is the best word. Noise is inevitable, but you're trying to reduce the amount of noise and the -- he refers to the bidirectional diodes. And what the bidirectional diodes do is, they basically -- they prevent in either direction voltages below a certain amount from going through. That's just something we know about the diodes made in semiconductors. So it provides a degree of noise immunity or noise resistance but those don't remove all the noise.

I don't -- "avoid" is kind of a strange word to use there. I don't know if that's a translation problem, but it's clear from that, that the bidirectional diodes improve the noise immunity in that line by blocking lower voltage -- lower voltage noise signals.

Q Would it be fair to say that Yoshinaga tries to reduce the noise then?

MR. ANDERSON: Objection to form.

A He's trying to -- he's trying to reduce the noise that -- typically types of noise that can occur in a circuit of that type. That's why those bidirectional diodes are used. And Yoshinaga did not invent the bidirectional diode use for that purpose.

Q But Yoshinaga was specifically trying to reduce the noise; is that correct?

MR. ANDERSON: Objection to form.

A Well, again, the reducing noise in situations where you have switching noise from one block could go through the -- align and corrupt what's going on in another block, everyone tries to do that. And Yoshinaga is doing that, as everyone else does.

Q Okay. And the way Yoshinaga teaches to avoid noise is to connect the reference potential lines by bidirectional diodes that are connected to one another in the opposite direction; is that

fair?

A That reduces one type of noise. As I said earlier, the bidirectional diodes, what they will do is prevent low voltage noise from going either direction by going through the bidirectional diode. It will -- the diodes will -- reverse bias will block everything. Forward bias, the -- anything above a certain voltage goes through and anything below a certain voltage would be screened out.

So it's -- it's a little -- it's a little noise reduction technique that's being deployed. And, again, I'm pretty sure Yoshinaga is not claiming that as invented material. That's pretty well-known in the art.

Q But you'd agree with me that Yoshinaga is employing the technique described here in paragraph 5 to help reduce noise?

MR. ANDERSON: Objection to form.

A I would agree with that because it's a well-known technique he's deploying into his circuitry.

Q Okay. All right. Let's go to paragraph 84 of Yoshinaga.

A And, by the way, I don't know where you're going on the line of this. We've been on for an hour and fifteen minutes. I can go longer. It also depends if you want to take a lunch break. If you think, you know, you're not going to need not much more time and wrap it up without a lunch break, you know, I'll work to whatever you're -- you're in charge here.

Q Yeah. Let's -- let's finish this kind of line of questioning and then if you want to take a lunch break, we can do it. I know it's east coast time. You're at lunch. So if you want to take a longer break this next break, we can -- we can do that.

A It also depends, if you think you only have one more session, we can continue without a lunch break. If you think you're going to need two or more sessions after the lunch break, we can take a lunch break.

Q All right. Well, let's -- let's see where

we're at when we get there.

Are you at paragraph 84 of Yoshinaga?

A Yes, I am. I was just -- a little housekeeping. And of course, I'll have to go check on that situation that came up and I'll advise if anything changes because of an update on that.

Q Okay. So I want to go to the last sentence of paragraph 84.

Do you see that?

A If you're referring to the lengthy sentence that begins at "normally," it's two-thirds of the paragraph, but that's the last sentence; is that correct?

Q Yes. That's the one I'm referring to.

A It's a long sentence.

Q I agree. I'm just going to ask you a simple question about that sentence, if that's okay.

Do you have that sentence in front of you?

A I was just reading it because it's so lengthy. I wanted to read it before we get into

questions, at least give it one reading before we start.

Q Sure. Let me know when you're ready.

A Oh, I'm fine. I'm ready to go.

Q Okay. One of the goals of Yoshinaga is to improve the ESD resistance while keeping the chip size as small as possible, fair?

A Yes.

MR. ANDERSON: Objection to form.

A Sorry. Is -- by the way, just for clarity, when he says "resistance," he means that in the figurative sense, not literally a circuit resistance. So he's trying to improve the ESD hardness, shall we say, is what he's trying to do. His use of the word "resistance" could be confusing, so it's...

Q Okay. So one of the goals of Yoshinaga is to improve the ESD resistance, as you described it, while keeping the chip size as small as possible, right?

A That's what he says -- that's what he says and that's nothing atypical, of course.

Q Let's go to paragraph 85 now.
A Okay.
Q I'll give you a second to read -- that's basically a one -- one sentence one, so I'll let you read that.
A That's not a paragraph. That's a sentence.
Q Excuse me. Let's go to 86, sorry. I have the wrong paragraph.
Can I refer you down to 86?
A I haven't read that, but I'll read it now.
Okay. Noting there's some mangled English, we'll get through it. I've read 86. You can go ahead.
Q Another goal of Yoshinaga is to limit the unit price of the chip as much as possible?
A Yes. The way you understand this is, typically, when you buy a wafer started at a foundry you pay -- you pay so many dollars for the wafer. So the more chips you can put on a wafer, the lower price per chip you're paying, is what that essentially boils down to.

Q Okay. All right. Let's go to -- back to your declaration real quick, paragraph 153.

A I'm at 153.

Q Okay. All right. And I'm going to pull up the -- the image in paragraph 153.

Do you have that in front of you?

A I have, fortunately, both 153 and the figure on opposite pages and I have it on both sides in my printout, so I can look at both at the same time.

Q Okay. So in this modified Figure 6 of Yoshinaga found in paragraph 153, you have pin 5 and pin 6 connected with a bond wire, correct?

A There's more than one pin 6 but I assume you mean at the top there where the -- on the top of it where it shows pad 5 and pad 6 with the orange area between them and a jumper bond wire going across. I assume that's what you're referring to.

Q Correct.

A Yes. That's what it shows.

Q Now, pin 5 up at the top here can't be

connected with a bond wire to the package anymore, correct?

A Not necessarily. Beauchamp shows you if you do it carefully, you could actually do daisy-chaining and you could connect the bond wire on to the pad and then continue. You'd have one ball on the pad and you could continue to another pad. That's what Beauchamp definitely shows.

Q And so you could do the same thing with pin 6; is that fair?

A It's an option. These are a matter of what options you want to use. What this is showing is that one option is to do it because it's known in the art in the way that's shown here. That's the argument that's being made.

Q Now, you didn't refer to this type of daisy-chaining in your declaration, did you?

A I believe that I did when I referred to Beauchamp.

Q Well, let's go see real quick. I think it's paragraph -- paragraph 150. I just want to make sure I understand what you're referring to.

A Yes. Actually, I did use the phrase "daisy-chaining." I can't search the paper document, obviously, but if I searched on "daisy" I would have found this.

Q So you did refer to daisy-chaining in your declaration, correct?

A Yes, I did. And it's what Beauchamp shows there in the figure above, of being able to wire a wire onto a bond with one ball and then keep going to another pad. I call that daisy-chaining. I don't know if that's a term of the art, but I think it conveys what's going on there.

Q Now, do you rely on daisy-chaining the pins in Yoshinaga to reach your obviousness conclusion?

A I don't think it's necessary. You asked if you could -- you -- you asked me if you could -- actually doing that would prevent 5 from being used. And my answer there was if you daisy-chain, you could daisy-chain something, say, to 5 and then continue over to 6. You could do that.

But in here it's -- again, it's a design choice, it's -- what's -- how many pads do you have, what you need to do in the architecture. All I'm showing here is a person skilled in the art reading Yoshinaga knows that from Figure 1, for example, 5 and 6 are shown connected together.

Yoshinaga does not show how to do that. He doesn't -- he's silent on that. And one way to do this would be the place the pads because they're fungible where we show here and then to use a jumper bond to connect them together. That's one way to implement what Yoshinaga describes but doesn't depict.

Q But you don't rely on daisy-chaining those pads in Yoshinaga together and then to the ESD bus, correct?

A It's not depicted here but it's an option you could use in order to connect that pad to the ESD bus. The other way -- another way you could connect, that pad could be connected via one of the, like, the top level metal to another pad. There's different ways to do that, but this is one

option for doing it, either just the jumper or the jumper with a -- as a daisy-chain off to the package. It's just -- there's many options here, how to tackle this.

MR. WATSON: Okay. Well, let's -- let's take a lunch break then, Dr. Foty. And then we'll come back. And I don't know how much time I'll have, but I'll get you out by 5:00.

(Whereupon a break was had.)

BY MR. WATSON:

Q Welcome back, Dr. Foty.

A Welcome back, Counselor.

Q Did you discuss the substance of your testimony with anyone during the break?

A No, I did not.

Q Okay. Dr. Foty, for grounds 1 through 3 you rely on the Saint reference, correct?

A The Saint reference appears in the -- in the cited primary reference list for all three grounds. I just wanted to verify that and that is correct.

Q Now, Saint has over 400 pages, correct?

A If you include everything, yes, it's about 400 pages of text, about 450 if you include the index and blah, blah, blah.

Q Did you rely on the entirety of Saint to reach your opinions?

A To the extent I reviewed Saint and didn't see anything that contradicted my opinions, I looked through Saint. Saint has a great deal of material. And there were certain things about Saint that were why I found Saint in the first place. So I relied on Saint as I describe in my declaration to the extent necessary to reach conclusions and form opinions.

Q Okay. So the -- but the layouts you were relying on from Saint are all listed in your declaration, correct?

A Any material I relied on from Saint to reach conclusions and form opinions is cited in my declaration, yes, it is.

Q Well, let's pull up Saint. That's Exhibit 1008.

A And it will probably be easier if I use my

book rather than fight with the binding. The only caveat that is that the production page numbers in the lower right and the page numbers in the book are different, so we'll have to mediate between the two if it's easier for me to use the book copy for what we're doing here.

Q Okay. Agreed. So let's go to page 172 of Saint --

A Is this the page -- sorry.

Q Yeah. I was going to give you the other page. So let's go to page 172 of Saint which is page 157 if you look at the number in the top right.

A So the book page is 157?

Q Correct.

A Okay. This has Figure 716 -- okay. That is -- that's what I have in front of me.

I literally want to make sure when we do this we're on the same page.

Q Yeah. Let's -- let's make sure as we go through Saint that you look at my screen and make sure we're on the same -- same page here.

A Literally.

Q Yeah. So on page -- Saint page 172 or 157 if you look at the top right number, it discusses the general processes of laying out a chip; is that fair?

A Yes. And he seems to -- Saint has this colloquial way of describing of how the -- not just the -- you know, the engineering but actually how the people interact with each other in those situations. So that's what he does here.

Q Would you agree that this process of laying out a chip involves multiple steps and considerations?

A Shouldn't the -- the layout people are doing their jobs because, you know, there's a lot as -- as Shane -- sorry, Shane.

Saint makes very clear that there's a lot of negotiation you need to do among each other on a variety of issues. So that's what he's describing here, I believe.

Q So on page 172, Saint mentions committing to go a chip size and floor plan initially.

Do you see that?

A Yes. I see that as a -- as what he says there.

Q Do you agree that this commitment is just the beginning of the process?

A Well, it depends on a number of factors and on the situation. You might have -- for example, you might have a template of packages with particular pins you work to. But I would say that at some point you need to commit to what he describes there for those reasons but that doesn't mean that he won't come back later if there's a way to improve something. It's designed as iterative is a good way to put it. And speaking from industrial experience, my own part, it's very iterative.

Q So designing a floor plan of a chip is an iterative process, you'd say?

A I think that's a fair characterization. That means that you do something but then you may learn something further that something -- for example, you do the layout and then you have to do

what's called the LVS step. I don't know if this is mentioned in Saint, but I know this and that's where you do the layout and you run the layout through a tool which extracts, for example, the parasitic capacitances. And then you have to go back and run that through the circuit simulator and you have to see if that agrees with your original schematic. That's called layout versus schematic.

And that can be an iterative process because you may have to go back and change the circuit and then change the layout again. So it's a complicated process to do that. So at some point you commit to some things and then you may have to change them later.

Q You'd agree that designing a floor plan of a chip is a somewhat complicated process?

A It's comprehensible, but it's -- it's got its complexities which is why Saint wrote his book obviously. I should say the two Saints wrote the book.

Q Now, can you go to the second paragraph on

this page, page 172, where it says "...changes occur. We can't control everything." Or it starts with, "Naturally, changes occur. We can't control everything."

Do you see that?

A If you let me read the paragraph there, begins with "As each block."

Q Yeah.

A Well, I think that's fair. Describes the iterative process I just described where you may find that changes need to be made to the topological circuit, you know, construction and that would change the layout and so forth and so on.

Q So would you agree that this statement reflects the inherent unpredictability in chip layout design?

MR. ANDERSON: Objection to form.

A I wouldn't say it's unpredictable in the sense that it's random, but when you start doing a project, you may find that things happen you're not expecting. So you have to roll with the

punches essentially. I think that's what Saint is -- Saint clearly understands that from his own work -- or their own work, I should say.

Q So when you design a chip, you may find things happen that you're not expecting; is that fair?

A That's true of anything. If you build a shed, you find that out.

Q Okay. Given this statement, would you agree that a layout designer cannot control every aspect of chip design based on their initial design plan?

MR. ANDERSON: Objection to form.

A If you're lucky, you may only do one pass. If you're very good, you may only do one pass. If you're -- if the chip being designed is simple, you may do one pass. So it's a combination of the complexity and the skill of the people doing it and so forth, how many changes have to be made.

But in the design flow, which actually if you look at that figure from Uyemura that I mentioned earlier which is in my declaration, he

shows the general overall flow and the -- the layout and chip design is only part of it. And there may be -- there may be iterations back up to that. And let me see if I can --

Q So you would agree with Saint that changes occur and the designer can't control everything; is that fair?

A I would say you can't control everything, but that doesn't mean it's just, you know, a disaster every time, that you control what you can and you have to revise what you can. And the figure I referenced is at paragraph 44 and page 20 from Uyemura where he shows the design flow. He doesn't show the iterations where you have to go back and redo something up ahead. He shows it in the nice, clean, where everything just falls in sequence into your lap.

And that, in typical cases, does not happen. There's a lot of iteration, but at the end of the day, the idea is to get a circuit that works to specifications, worked as expected in a layout that can be manufactured and passes the

design rule checks.

Q So you'd agree that typically circuit design requires a number of iterations?

A I wouldn't call it circuit design. I would call it the whole process of creating an IC as per the -- I'm looking at that -- your -- the figure from Uyemura's textbook.

The circuit design is only one of the five phases he shows there. So the circuit design is the third phase. And when the circuit design is -- passes its specifications in the CAD tools, then it's passed on to layout, and that's when the layout converts it from the topologically abstract depiction into the actual physical shapes and levels that will be manufactured in silicon.

And when that's done, there are parasitic elements that occur naturally like capacitances between metal interconnect lines, and you may have to iterate back to change the layout or you may have to iterate back to change the circuit schematic, change the circuitry at the topological level.

So it's fair to say that the process is proceeding in a coherent way to a desired end but the story is not a straight line. It's sort of like history, I guess.

Q Designing the layout of a circuit is not a straightforward process then; is that fair?

A No. I don't think that's fair. I think it's a straightforward process. It's just that it's -- the -- it's part of a larger process. And so the larger pieces interact with each other so you may have to change things, do another pass to say, well, now, when we put this in this way in the layout, it caused parasitic capacitances which caused the circuit -- speed of critical circuits to be underperforming.

So you either have to redesign the circuit or change the layout using different layout techniques of the same circuit. So it's -- as I said, it's a controlled process that just has various ways you get to the end you're going to.

Q Can making a simple change to the layout affect other parts of the layout such that you

need to make additional changes?

A It could. That's the thing that makes this challenging. And good people -- good layout people are hard to find and they're great when you have them because they minimize that by their experience and their knowledge.

Q Let's go down to the paragraph where it starts, "However, no matter how good you think your final floorplan is, you are still not ready to begin your layout."

Do you see that?

A I see that.

Q Do you agree with that statement in Saint?

A Well, what Saint describes in that paragraph after that sentence is you might call it the social aspects of it. You go around to the other people in different -- with different parts of the whole chip design process and ask them things like he says: You know, where should this go in the circuit; where should the blocks be arranged for -- which blocks are going to be the ones that talk to each other and so forth and so

on.

That -- and sometimes even when circuit designers design their circuit schematics, they will actually write notes on the schematic for some of these kind of questions and answers. They actually will write "do this this way in layout," for example.

Q So would you agree that there's a need to collaborate during the design process with others?

A There usually is. You know, that's why you have large teams of engineers designing large chips at large companies like, say, Qualcomm.

I think an example, I believe, Qualcomm from some things I know, they -- it takes them 4,000 man-months to design an IC, something like that. So it's -- these big, complicated ICs, it's a very talent-intensive process and a labor-intensive process, shall we say.

Q So designing an integrated circuit can take 4,000 man-hours? Is that what you said?

A Man-months.

Q Wow.

A I won't -- don't hold me to that because I've seen these things and it's -- it's rather stunning. By man-months, you know, that means if they have a big team doing it two -- for over two years, you can figure out how big the team is.

But these complicated chips require a lot of effort. And so, obviously, you know, Saint is someone who's had a lot of experience doing this. And the book is useful for helping people being better layout designers and be more efficient at making this -- the design -- design closure is a term used in the art when everything in the whole process, everything works, everything agrees with each other, the circuit schematics are fine, the layouts are fine, everything is fine, you have closure, you do the tapeout, you get the tape to the fab, and they make the mask and manufacture the chip.

Q So would you say integrated circuit design is simple?

A No.

MR. ANDERSON: Objection to form.

A No. I would say it's -- it's straightforward but it takes a lot of effort. It's sort of like winning a war. The objective is pretty straightforward but how you get there is -- takes a lot of talent and a lot of effort.

Q Let's turn to page 177 which is, using the blue numbers, page 162.

A Okay. I have that in front of me.

Q Let's go down to the paragraph that starts, "However, in modern processes there are 1500 to 2000 design rules."

Do you see that?

A I see that, yes.

Q Okay. Is it true that in modern processes there's 1500 to 2000 design rules?

A Saint was writing this in 2002. I'm sure that number is much larger now.

Q Okay. So there's thousands of design rules to consider when you're doing a chip design?

A Yes, which is why using, you know, libraries as I described earlier for that example, two-input CMOS NAND gate helps, because you can

make a -- instead of having to deal with a billion transistors, you can break things down into -- into blocks.

One thing about this technology, the silicon CMOS technology, it's very amenable to hierarchy in -- from blocks down to, you know, circuit functionalities and so forth. So you try to have as much as possible that essentially is reuse or precooked where you have a block that passes design rule check, and then you use it thousands of times in the chip.

That's not atypical, to have thousands of instances because that block has already passed design rule check and you can just use it and know it passes the design rule check.

Q Thousands of incidents -- instances of what? I just want to make sure I understood what you just said.

A Earlier, I pointed to that NAND gate we were looking at in the physical design with the blue metal and all that and I noted that was sort of a primitive. That was a NAND gate.

And so, for example, you could make a block of some sort. It's very common to have blocks on a menu that the designer brings in to build the chip up for blocks. And so the block might if -- it's a block that has passed design rule check, it's obviously to your advantage to reuse that. So it's not uncommon when you look at a chip to find some block that's literally used thousands of times in a single -- in the same chip.

Q Let's turn to page 207 of your -- of Saint, sorry, of Saint, which is page 193 on the top right.

A I have that in front of me, and we seem to literally be on the same page here looking at the screen.

Q So this page 207 states, "The general rule is to make it look nice, as with the chip layout. Evenly distribute the pads around the chip if you can. Keep them to the outside. Keep them separate apart."

Do you see that?

A I see that. Yes.

Q Do you agree with that statement?

A Well, I would break the statement into two. Because what he first describes is a good rule of thumb in a lot of things, including this kind of chip design at any of the levels, is if something's clean and nice and orderly, it's probably going to manufacture more easily.

The second part is evenly distributing the pads and keep them to the outside and spread apart, those essentially are ground-rule driven anyway. The pad sizes are specified by the ground rules. The separation between the pads is specified by the ground rules. And the -- the pads you would typically, as he shows in that figure that's peeking up from the bottom there, you want to have the pads have to be on the outside so that they can connect off to the traces in the package without going -- you don't want that going over the middle of the circuitry.

Q Okay. So do you agree that you want to evenly distribute the pads around the chip if you

can?

A If it's pad-limited, certainly. If it's core-limited, you might -- you have flexibility since you're going to not use some pads, you're not going to put them in. You have flexibility to choose where to put the gaps where you don't have pads, for example.

If you're going to push circuitry, as that 2010 microphotograph we've looked at earlier indicates, you could put it in -- you can arrange so you have enough space to put particular circuit blocks where the pads would be that you've removed in the core-limited design.

Q So if you have a pad-limited design, you want to evenly distribute the pads around the chip if you can, correct?

A I would say that I agree with that and I'll further note that it's actually not atypical in companies to have a template for what the pads are going to look like for a particular, you know, number of pads and so forth. So you might even start with a sort of a precooked pad distribution

because it, obviously, would meet the ground rules and you can use that as a starting point because you don't have to lay it out and worry about ground rules. It's precooked for you.

Q What do you mean by "ground rules"?

A Oh, the ground rules are what -- I thought since that came up earlier, I thought that was being taken as we knew it.

The ground rules are sort of like the building code for -- for a chip. What they basically tell you is how small shapes can be and how much space you have to put between shapes and so -- and they may even specify that a shape has to be a particular case.

So it may specify a pad has to be a square of so much length on either side of the square and the space between the next -- one pad and the next pad can't be any smaller than some distance. Those would be typical ground rules. Essentially, is a size of objects, minimum size, maybe specific shape, and also what's the minimum spacing you have to have between them to make sure the

lithography will print them. That's generally what ground rules are in layout design.

Q Who decides the ground rules for a chip?

A It's dependent. It depends on the manufacturing. Usually, there's some manufacturing process of what the rules are. Because, for example, the lithography being used would determine what's the smallest feature size you can make. When people refer to say -- I've used the phrase earlier, like, a 7-nanometer process. That means lithography is capable down to 7 nanometers to print shapes of that size and print two shapes of that size with that amount of distance between them. So the ground rules generally come from the manufacturer.

There's some ability to negotiate that with your foundry, but think of it as when you're going to build a house. You build it to the building code that the municipality has in place. Same idea as here.

Q So why would a designer want to evenly distribute power -- or strike that.

Why would a designer want to evenly distribute pads around a chip?

A In the first instance, it's because it's the simplest case and it would meet the ground rules as I just described and allow you to do what he does here. He basically shows - below, he shows a -- shows IC with -- exemplary IC with 16 pins and you put it in a package with more than 16 pins. And by having them evenly spaced, you're able to connect them in nice, straight lines to -- the pads to the traces in the package.

And you'll note if you look at that picture in Saint, it looks a great deal like the wire bond lines we see in that 2010 figure that I -- I have in my declaration in several places in which we've discussed a few times already.

Q Let's go to page 221 of your declaration.

A My declaration?

Q Sorry, excuse me. Let's go to page 221 of Saint.

A There's no 221 in my declaration. That's why I was -- that's why you caught me.

Q Yes, 221 of Saint which is page 207 if you look at the top right.

A I see that. And -- okay. Go ahead. I -- you're showing the bottom part of the page and I did use the figure in the upper part of that page more than once in my declaration.

Q On page 221 it says, "All these packaging decisions depend on many factors. How important is size for this application? How many pads do we need? How big is the circuitry? How large a chip will the package allow? Do we have the technology to manufacture chips in multi-tiers or with flipping? How important is it that we use a particular package? And so on."

Do you see that?

A I see that. Yes.

Q Are those part of the ground rules that you need to decide when you're developing a packaging in a chip?

A Well, ground rules apply, as I've described them, to the silicon manufacturing. Packages, generally, are sort of generic. A

package would have, you know, an opening for an IC that could be of a certain size and have a certain number of -- no more than a certain number of pads on it. You couldn't put -- if you want to connect -- you have an IC with 20 pads and you want to hook up all 20 to pins, you can't use a package with 16 pins, for example.

So I would say these are the kind of -- I wouldn't -- the ground rules impinge on these but these are sort of big-picture issues. For example, what does he say here? How important -- this is a good example: How important is it that we use a particular package? That's almost like a marketing type of answer. Because you often find the same chip is put in many different packages. It's the -- if you open it up, it's the same chip but different packages with different form factors; the pin's in different locations, different sizes, different materials, using a ceramic instead of plastic in some applications.

So the -- these are things that, again, in the big picture when you're going to do a package,

there are things driving that at a number of levels including, as I said, the application. The same chip could be deployed as products in multiple different types of package.

Q Are they factors that are listed here, an important factors in deciding how to package a particular chip?

MR. ANDERSON: Objection to form.

A What he's describing there is -- what he says is closure on packaging is answering these different questions. Size, again, will the package fit. If you have a package that is tall and you're going to put it in something narrow, that's not going to work.

How many pads do we need? That, again, is -- you know, if you have -- you want to have -- you need to have enough pins in the package to pick up all the pads you need to have come off the IC.

How big is the circuitry? That basically is if you have a package, it can only accommodate a chip up to a certain size. If your chip is much

bigger than the chip hole, essentially, in a package, that won't work.

And the same thing that's in the package rules. The same thing, the chip for the package rules. Again, for the chip -- how big can the chip get before it won't fit in the package anywhere. Those are -- again, those are the kind of things that you have to consider.

And also the last one there, to be complete, is how important is it that we have a -- I described that already because same chip, many different packages for different applications, different customers. And the technology to manufacture the chip in multi-tiers or flipping, he's -- what he's looking at there, are there going to be different situations where we use a technique like -- like ball grid, which I believe the microprocessor people use when they have a chip with, like, 500 pins.

Q Got it. Let's flip to a different part of Saint. Let's go to page 33 which is towards the beginning. It's page 15.

A Okay. I have that in front of me. So let me know where you're pointing.

Q We'll start at the very top paragraph. I'll let you read it and then I have a couple questions for you.

A Okay. Okay. I've read that. He's describing some history here basically.

Q Yes. Does the uniform spacing rule, did that apply to where you place the pads or did it affect it in any way?

MR. ANDERSON: Objection to form.

A I'd have to read, you know, more of the text here to nail it down, but I don't believe so. I believe what he's talking about here -- because he's referring to microns which are pretty small. That's, like, internally, is -- you would often just have -- I'm reading this to mean there was a time -- again, this is driven by the CAD tooling.

The CAD tooling wasn't sophisticated enough to include the use conditions: What's going on in the chip when it operates. And so you would just lay out these uniform power straps and

then use those. And he's saying here that the newer tools at the time that he wrote the book actually will look at how the chip is behaving, evaluate how the power demands, as we were talking about earlier which would be the current demands, are differently in different places, and that it would actually adjust the power straps to be bigger when you need more power. Again, it's like putting a bigger pipe in to fill up the water hole you need filled up more quickly.

Q So you would arrange your design so that you had the various power pads nearer to the areas that require more power; is that fair to say?

MR. ANDERSON: Objection to form.

A I don't think he's discussing that -- he's not discussing the pads here. He's discussing the -- the wiring that goes in from a power supply pad which he shows on the previous page and then how that's distributed.

So it's, again -- you think of it in a city, the factory might have a different power provision because it draws more power, draws more

current than your house does. And sort of the old way of doing it before the tools were sophisticated enough to know whether it's your house or a factory, they didn't discriminate that; whereas, the newer tools actually look at and say, okay, that's a house, that's a factory. I have to plan for having more power being drawn by the factory than the house.

Q Got it. All right. Let's turn to another portion of Saint. Let's go to page 220, which is page 206. And we're going to go to "Filling Pad Gaps" section here.

A I see that, yes. I have that open in front of me, these pages.

Q Okay. You -- do you rely on this section, "Filling Pad Gaps" on page 220 and 221 in reaching your conclusions in this case?

A Let me answer your question this way: I regard what is described here as, certainly by 2010, was a known technique. This just puts it down in writing that in 2002, the idea of in a core-limited design -- and notice he says

"core-limited" right there, if you have space where you don't need pads, you can actually put circuitry in there and reduce the overall size of the chip.

And so the corresponding piece that I cited was that 2010 microphotograph which actually shows a teardown of an IC where you can see that. You can see it's core-limited. There are places where pads are not used and circuitry is pushed in there.

And it's interesting, by the way, to read that article because the article has nothing to do with saving space. The article is just about something about that chip and they don't even regard that usage as remarkable in 2010. They don't even comment on that. So it was -- it seems like from that it was a known technique. And of course, Saint is 2002 describing precisely what we see here and in that microphotograph.

Q Which article are you referring to?

A I have several instances and we looked at them earlier, that microphotograph. I think last

time we looked at it we were talking about the ball bonds on the pads and that actually refers to a 2010 article about a particular IC. I believe it's from On Semiconductor. Whoever was writing the article did a teardown and was looking at this and they were -- whatever they were looking at in the teardown, it had nothing to do with the pushing circuitry into the saved spaces between the pads, it's just in there. They didn't even remark on it. They seemed to regard it as unremarkable.

I can find the reference. It's -- it's in my -- it's in my declaration. The figure appears multiple times, but the first instance has an URL to an article.

Q Let's -- we'll go find the article in a second, if that's okay, Dr. Foty.

A I can find it pretty quickly when you need it because that picture is hard to miss.

Q Okay. If you can find it quickly, let me know.

What article are you referring to?

A I believe -- let me see if I've got this right. On page 25, it's Footnote 4. It refers to the JPEG which is on the next page which is the figure from 2010 we were looking at earlier.

Q And you rely on the article to say that the bond pads arranged -- are arranged around the periphery of the integrated circuit; is that right?

A In this particular usage of that figure, that's the reference I make. I -- this is the first time the figure appears which is why the URL goes to -- it has the URL pointer. And later, I make the reference to the obvious use in here of places where there are no pads on the edges, that circuitry goes right up to the edge of where the pads would have been if they had been there.

Q Got it. So let's go back to this portion of Saint on page 220 to 221.

A Which is the page we have in front of us, I assume.

Q Yes.

A Okay.

Q Are you there?
A Yes. I've been there the whole time. I'm using the book copy of Saint. It's right in front of me.
Q Pages 220 and 221 do not discuss saving space by converting supply pads into reference potential pads, correct?
MR. ANDERSON: Objection to form.
A It doesn't refer to the pads in any particular way. It simply says if you have places where you don't have pads for whatever reason, the pads are not used, you don't have a full complement of pads, you can push circuitry into there. It doesn't say why you have fewer pads than you could have, similar to what we see in that figure on page 26 of my declaration.
Q Okay. So pages 220 and 221 of Saint do not discuss saving space by converting supply pads into reference potential pads, correct?
MR. ANDERSON: Objection to form.
A It says nothing about what the pads are doing, just says --

Q Okay.

A -- they need fewer pads than you could have in the design. So since you freed up space you can push circuitry in there. That's all he's says.

Q Okay. Let's go to paragraph 104 of your declaration.

A Declaration, not Saint?

Q Yeah. This is declaration.

A I'm going to put Saint aside.

Q Yeah. We'll probably be back to it.

A Sorry, what paragraph were you looking for?

Q 104.

A 104. Got it. Okay. I'm finally there. Took a while to go there for some reason, but I'm there. It spans two pages.

Q In paragraph 106 of your declaration, you do not cite any portion of Saint to support the idea that a person of ordinary skill in the art would know how to wire bond pads directly to one another, correct?

A I don't discuss that here. That comes from Miller and Beauchamp reflecting the knowledge of a POSITA is my view of that.

Q Okay. So you're not aware of any teaching in Saint of using bonding wire to connect bonding pads to one another, correct?

A I'm not aware of anything in Saint about that. As I said, I regard that as demonstrably within the knowledge of a POSITA, is my argument.

Q Are you aware of any teaching in Saint that discusses using bond wire to connect pads on the underside of a circuit?

MR. ANDERSON: Objection to form.

A As far as I'm aware, Saint does not discuss that. And again, the scope of the '164 patent was simply the conventional, you know, plain or single IC with pads on the top. There's no discussion of any other architecture like circuitry on both sides, you know, multichip packages, stacked chips, things of that sort. That doesn't appear in -- doesn't appear in any of my references or at least to my knowledge simply

because '164 doesn't deal with any of that.

Q So it's your testimony that Yoshinaga says nothing about circuitry on the underside of the circuit?

MR. ANDERSON: Objection to form.

A Neither Saint nor Yoshinaga because that's not in the scope of what they're dealing with. And again, '164 is not within the scope of that either.

Q Okay. Let's go to page 162 of Saint.

A Do you have a blue page number, shall we say?

Q One second. Let me get it.

A I see you're getting there.

Q Page 147.

A I have that in front of me.

Q Okay. So this Figure 7-7 is found in Chapter 7 of Saint, right?

A That is correct, yes. Figure 7.7 is what we're looking at.

Q And 7-7 is showing a pin-out simplification, correct?

A What he's showing here is -- the pin-out is simplified not by showing the pins, but by showing that you will arrange the pads based on lining it up for these -- these buses. So the pin-out just refers to where the pads will be placed. They'll be placed consistent with keeping the pads that need to be protected to the particular power and ground rails that need to be protected to keeping them grouped and close to each other just to make that easier.

Q But Figure 7-7 is described as a pin-out simplification showing like protects grouped together?

A Yes. He calls them "projects." I believe that he means by that the blocks that are being put in.

Q Now, pins are not wires, correct?

A "Pin-out" is a term used to indicate where things come off the circuit. It's not a pin of the package. It's the pin-out of the -- the pin-out of the IC.

Sorry. I got a visitor here.

It's the pin-out of the IC essentially. So what he's just saying there is, he's saying in a different language that you move the -- you move things around so that the circuitry is close to the pads you want to go together, and then those pads are grouped so that they're closer to the bus where you want to hook the protection up as per those other figures like on the previous page where he shows the different signal pins being connected to the different rails, the different three sets of rails.

Q Does Figure 7-7 show any pads?

A It does not, but it's implicit from the way this figure is put in that he's starting with the figure on Figure 7-6. He's showing how the driving force for grouping them is where the buses are which is reflected in where the circuitry is placed and I don't know if he shows in this particular instance the final version where he has the pins all moved to, but it's implicit that, like, for example, the blue pins in 7.6 on the previous page will all be moved over to somewhere

on the left half in order to be closer to -- excuse me, the -- the white pins with the blue surrounding will be moved over to the left side in order to group them together to be near VCC in ground 3.

Q Does Figure 7-7 show any pins?

A It doesn't show them there, but it's part of what he's discussing there of where you're grouping things based on where the voltage and ground buses are.

Q Does Figure 7-7 show EDS buses?

A Those are effectively E -- I mean, I assume you mean ESD, not EDS.

Q Apologies, yes.

Does Figure 7-7 show EDS -- excuse me, strike that.

Does Figure 7-7 show ESD buses?

A Third time's the charm.

Effectively, it's showing where they are because now you're going to connect the -- as they show -- shown in, like, Figure 7-4 and 7-5 on the previous page, you're going to use those rails to

provide the ESD protection for the inputs of particular pads.

For example, 7.4 shows that pin 6, 8, 10, and 14 will be connected to the VCC 2 and the ground 2 for the ESD protection where you shunt an ESD event to the power rail of the ground if it strikes one of those pads.

Q Okay. Is it correct that the fact that a pin -- pins are grouped together does not mean that the pins are then connected to a single bus?

A What matters is what's on the previous page where he's showing the part of the design which is implicit also in Figure 7-6. This is what he's showing is that the circuitry demands that in the -- in the 7.6, he's saying the pads are assigned to different VCC and ground rails as per there, but this arrangement is not efficient.

So you can shuffle the pads around. The pads are -- the pad placement is fungible and so you -- you identify the pads differently. You change their assignments in order to be more compatible with the different -- they group the

pads together and the circuitry together that would use particular VCC and ground bus as ESD discharge rails.

Q I'm not sure that answered my question.

Yes or no: The fact that pins are grouped together does not mean that the pins are connected to a single bus?

MR. ANDERSON: Objection to form.

A Well, I'm trying to make sure I understand -- the reason my answer was long is because you group the pins -- you group the pads together in order to keep them as close as possible to the target bus you're going to use for an ESD protection scheme.

Q But you're not required to have all the pins that are grouped together -- strike that.

You are not required to connect the pins that are grouped together to a single bus, correct?

A Well, there's no requirement you have to do it correctly, but you're -- you're only -- you're meeting a design requirement that he

describes elsewhere of you want to connect, like, digital stuff all goes to one and analog to another. So you could do that differently, but he's teaching here an optimum way of doing it that gives you the best layout and the best circuit performance, particularly for mitigating this interblock interference because of stuff, signals, noise going through a, like I say, a common ground line.

Q Okay. Would you agree that the fact that a pin is grouped together does not mean that those same pins share the same conductive path?

A Well, again --

MR. ANDERSON: Objection to form.

THE WITNESS: Go ahead, Shane.

MR. ANDERSON: Objection to form.

A The thing is, again, it's not a requirement, but you group them together as much as possible to go to the same bus. And it's just a matter of how many pins and how many blocks how you sort that out. So hopefully, you can move the pads around so that the pads for the digital block

will all be together to make the connection between the -- the circuitry and the -- what you'll use for ESD buses close together as possible. He's describing the best design method for doing that. You can do it many ways but this is a better way. It's more efficient.

Q Could each pin have its own diode to the VDD?

MR. ANDERSON: Objection to form.

A Well, do you mean a pin or a pad? Because the pin is an abstract term. The pad is the -- is the physical -- physical thing.

Q Okay. Could each pad have its own diode to VDD?

MR. ANDERSON: Same objection.

A Well, actually, each pin does have its own diode. That's depicted in 74 and 75 on the previous page.

Q So each pin does have its own diode connected to VDD, correct?

A As he shows here for the ESD protection, you have to protect ESD at each pad because if you

have ESD protection on pad 1 and none on 2 and 2 gets hit by an ESD event, 2 isn't protected. So every pad, somewhere between the pad and the signal going into the input signal of the input terminal of a circuit will have this double diode construction. One goes to the power supply rail and one goes to the ground rail. That's the standard ESD protection which is that Oti [sic] paper, or whatever it is, 1026.

So every pad has the dual diode depiction he shows on the previous page. That's -- but, again, that's the typical standard way of providing ESD protection.

Q Now, on Figure 7-7 of Saint, there's three different ground signals, correct?

A In this particular instantiation. I guess in the patent world, you call it an embodiment. He shows a particular design where he has three different power supplying ground buses due to the circuit blocks that will be inside there.

Q And those three different ground signals in Figure 7-7 of Saint are GND 1, GND 2, and GND

3, correct?

A At this level, he has three different ground buses to connect directly into the -- into the IC at some point.

Q Saint Figure 7.7 does not involve one signal ground signal that has been segmented, correct?

A In -- at this level, Saint shows them as three. Saint doesn't really go outside the pins other than to just discuss the basic ideas of wire bonding. But the basic problem you face is that eventually ground -- if you're using ground literally is somewhere all those wires have to go somewhere where they come together in an iron bar that's pounded into the ground or something similar to that. The grounds have to be united somewhere. Saint doesn't discuss that, but that's why Haralabidis is useful because he does provide how you unify those because, as I say, at some point in time they all have to go to the ground, which is Earth.

Q Now, Figure 7-7 involves three separate

ground rails, correct?

A At the chip level, yes. There's three separate ground rails and three separate power rails.

Q Okay. My next question is: In Chapter 7 of Saint, is the word "bus" ever used?

A I would have to look. I don't know if he uses that term for VCC 1, 2, and 3, but certainly would be appropriate to use it because those would be understood by someone as being a bus. It's a power bus because you have a rail with a particular voltage on it that's connected and parallel to many different circuits which is roughly the definition of a bus to my understanding.

Q Would you agree with me that Saint Chapter 7 does not teach a common ESD bus adjacent to the plurality of pad groups?

MR. ANDERSON: Objection to form.

A Sorry, could you run that question by me again?

Q Sure.

A Something I want to be sure I answer it correctly.

Q Do you agree that Saint Chapter 7 does not teach a common ESD bus adjacent to the plurality of pad groups?

A This --

MR. ANDERSON: Same objection.

A This particular instantiation has three. It does not have a common ESD bus. He has --

Q Okay.

A -- one somewhere else, but he doesn't teach it here.

Q Okay. Now let's turn to paragraph 363 of your declaration. Paragraph 363 of your declaration, which is on page 176.

A I'm there now in my paper copy.

Q So you refer to in paragraph 363 of your declaration a case study chapter found on page 261 of Saint, correct?

A Let's see. Saint has two long case studies in the back of the book, and I don't know if 261 is the figure we have or where the case

study starts, but it -- just for clarity, but he does have a long case study that includes the figure on page 177. The figure ID is CS. It begins with Charlie Sierra, which indicates it's from the case study.

Q So if I refer to this example as "case study 1," you'll understand I'm referring to the case study chapter found on page 261 of Saint?

A Case study 1 begins on page 248 in the blue numbers, so if that's -- that's pretty close to what 261 should be in the production. So I believe 261 is referring to the case study where it begins in Saint, the long case study, the CMOS amplifier.

Q I just want to make sure we're -- when I use the shorthand "case study 1," you know that I'm referring to this particular case study that you mention here in paragraph 363 of your declaration.

A Yes. Within the constraint that we're not pinning a page where it starts and we can find that if we need to, yes, "case study 1" is

referred to the case study one, the CMOS amplifier.

Q So let's go down in paragraph 363 to case study 1, Figure CS1-1.

Do you see that? I think it's on page 177 of your expert declaration.

A I see that, and have the figure in Saint if I need to do anything with it.

Q This figure CS1-1 shows a pin-out diagram with one common ground pin; is that fair?

A In this particular case study, yes, he has a single ground pad pin connection to the package.

Q The figure here, however, does not show any wiring; is that fair?

A It only shows the circuit blocks and it shows the -- where the wire bonds will go from the pads of the IC to the traces in the package is what it shows here. It's a 24-pin package, is what he's saying there.

Q But this Figure CS1-1 does not show wiring, correct?

A Well, I'm wondering what you mean by

wiring because it's showing bond wires. But by wiring, do you mean wiring inside the chip?

Q Let me ask this question: Figure CS1-1 does not show wiring between the various pads, correct?

A No. It only shows the bond wires going from a pad out to a package trace.

Q And much like Figure 7-7, this figure on Saint page 261 is a pin-out design, correct?

A I think it's a little more than that. What he's showing is that he's showing the package pin-out, if you want to go to that, the 24 on the package what they would be. This is -- I presume it's a package which has some sort of a square shape and has six pins on each side. So he would be -- a person looking at, say, the data sheet would see a basically just that black square with the pins showing what each pin is, as shown here which is, like IN3, IN3B, and so forth.

So in that part, you can call that a pin-out. That would be on the data sheet for the product.

Q Is the common ground marked GND the common ESD bus you use in your obviousness combinations?

A It's certainly part of it because you use both the power supply and the ground as -- as the shunt paths for an ESD event.

Here, Saint discusses this. He has one ground for the entire circuit because basically these are all amplifiers, so they're similar structure, similar signal. So in this situation, you need only one ground for -- for that situation. It's a good one to have because you only need one ground. You don't have a digital block in there to noise pollute everything.

Q But you don't identify any other ground in Figure 7 -- or Figure CS1-1 as the common ESD bus, correct?

A Figure -- this figure shows the single ground. He has a figure somewhere elsewhere where he shows a ground, a common ground, a single one going entirely around the inside of the IC. It's later in this case study and I have it in my declaration.

Q Let's go to page 367 of your -- or paragraph 367 of your declaration.

A Okay. I have that in front of me.

Q Okay. In paragraph -- or 368, excuse me.

Do you have paragraph 368 in front of you?

A That's on the facing page in my binder, so it's in front of me as well.

Q Okay. This -- this annotation of Figure 7-7 of Saint has been modified to add a common ESD bus, correct?

A Yes. This is the common ESD bus that's provided from Exhibit 1007. It might have been helpful if some bond wires were shown going from, like, a ground bus out to the common ESD bus, but this is combining 1007 with this figure in Saint.

Q But Saint Figure dash 7 -- strike that.

Saint Chapter 7 does not describe a common ESD bus, correct?

A Saint in this particular instance doesn't go outside the -- the IC, other than to note there's wire bondings. He does not describe when you get outside the chip how you unify all the

grounds, as I said earlier, because they've got to meet some place. That's just basic physics.

Q Let's go to paragraph 317 of your declaration.

A I have 317 in front of me.

Q Okay. In paragraph 317, you note that Saint concentrates almost entirely on the IC alone and rarely ventures outside of the IC bond pads, correct?

A Yes. And the title of mass design implies that. He's describing physical design of shapes in order to make the mask for the IC fabrication.

Q So if you go to paragraph 391 of your declaration.

A I'm there. You're catching up, I see, but I am there on paper.

Q Paragraph 391 is about claim 3, correct?

A Yes, it is.

Q You don't rely on Saint for the teaching that's of the limitation disclosed in claim 3, correct?

A Yes. I refer to reference -- Exhibit 1007

for that purpose because that's clearly disclosed in that exhibit reference.

Q That's because Saint does not disclose the common ESD bus, correct?

MR. ANDERSON: Objection to form.

A In the Figure 7-7 description, he doesn't show how or where the difference, say, the three ground lines are unified. They have to be unified somewhere; whereas, Exhibit 1007 actually shows that.

Q But Saint does not explicitly describe how the ground lines are unified, correct?

A Not in 7-7. In the case study, he unifies them at the IC level. In the 7 -- Chapter 7 instantiation, he doesn't unify them. He has them separate for the design reasons and he does not show how or where they eventually are unified to go to true ground.

Q So Chapter 7 of Saint does not describe how the ground lines are unified, correct?

A Does not describe a common ESD bus. He doesn't show how or where the necessary

unification happens.

Q Okay. Let's go now to Exhibit 1007.

A Give me a moment. There's a cat sleeping on it. And if you want to have another try at his name, I'll let you.

(Reporter clarification.)

Q All right. Well, let's talk about Haralabidis.

A I'll call it Haralabidis, but it will be spelled the same in the transcript.

Q Can you turn to the abstract of Haralabidis?

A I have that open in front of me. The print is a little small, but I think I can read it.

Q Haralabidis describes an integrated circuit assembly, correct?

A His inventive embodiment, I think, in particular I would call that an integrated circuit assembly.

Q So Haralabidis includes the packaging associated with an integrated circuit as well?

A He includes both the packaging and the PC board in his Figure 5, which what he's claiming is the inventive material.

Q So Haralabidis involves interactions with components beyond just the integrated circuit?

A Yes. He involves the package as well as the PC board onto which it is mounted and he explains why he does that.

Q And Haralabidis focuses on aspects of the entire electronic device, not just the integrated circuit?

MR. ANDERSON: Objection to form.

A He focuses on the integrated circuit and the package it's in and the PC board onto which it's mounted, at least for his inventive material. He describes prior art that's more constricted than that, but his particular inventive material covers those things, or what I should say, he claims his inventive material, to be fair.

Q Let's go to Figure 5 of Haralabidis.

Are you there?

A Sorry, I'm there. And this one is in my

paper copy somebody already rotated it for me so it looks the same to me.

Q In Figure 5 Haralabidis, what's labeled 540, 545, 550, and 555 are the segmented ground rails, correct?

A It's the segmented ground rails inside the IC.

Q Okay. What does it mean that the ground rails are segmented?

A He has them set up, he has four of them so each block has its own rail and the rails are connected together using the double diode configuration for some noise protection.

Q Does that mean that there's a single ground signal that's been segmented?

A Ultimately, you go out to a single ground signal for particular reasons he does describe in column 5. But here, he also -- you also notice he shows that each of those four segments has an independent connection to a rail in the package substrate. He's got one at each corner there of those four.

Q Okay. So Haralabidis teaches one signal, ground signal, these through four ground rails; is that fair?

A I wouldn't call it a ground signal because the ground is ground. It's what it's connected to. The signals might be what propagates through them. For example, that's the noise feature. I wouldn't call -- I don't know what you call that, but noise moving through the ground wiring is what he focuses on in his patent.

Q Does Figure 5 show any bond pads?

A It does not show them, but the -- the most simple way to connect those corner connections you see to the rails in the package substrate would be with bond pads and bond wires going to traces. So that would be a way to do it.

There may be others, but you certainly would expect that the bond pads being bond wired to package traces would be what is going on with those four corners there where, like, 582 and 588 are.

Q But Haralabidis does not disclose anything

about bond pads, correct?

A He is -- he may make a comment somewhere about possible options, but he does not show a particular technology to connect the -- those rails inside the IC out to the package substrate. However, obviously, much is -- much art is known of how you would do that. There's many ways you could do that.

Q But Haralabidis does not disclose bond pads?

A Not explicitly, but something has to.

Q So is it your opinion that bond pads are implied by Haralabidis?

A My conclusion and opinion, again, is based on also experience, is that there has to be some method of connecting the internal bus inside the IC out to the trace on a package using pads, and bond wires is a very common way of doing that.

There are other possible methods like ball grid and so on and so forth that can be used, but some method of that sort would be used here. His inventive material is not dependent on the method

that's used. He merely shows the essential, for lack of a better term, the topological connection there.

Q So to be clear, none of the disclosures in Haralabidis explicitly describe bond pads?

MR. ANDERSON: Objection to form.

A He's silent on the method used to connect from the inside the IC of the package substrate. He says nothing about any particular method.

Q Okay. Similarly, he says -- Haralabidis says nothing about bond pads themselves, correct?

A He's completely silent on that issue. I assume he doesn't regard that as part of his inventive material and that seems to be from examining Haralabidis of what's going on.

Q Let's go to paragraph 407 of your declaration.

MR. ANDERSON: Before we move to that, it's been over an hour so, again, just a good breaking spot.

THE WITNESS: It has been about an hour and 15 or 20 minutes, so probably if we come to a

good break spot, you know, or if you're going to finish up in the next five or ten minutes, it's up to you, but...

MR. WATSON: Yeah. We'll get to a break in a -- in just a little bit. I think I've got a good breaking spot.

THE WITNESS: Okay. Great.

Q Are you at paragraph 407 of your report -- or your declaration? Excuse me.

A I'm there. Yes.

Q Okay. Paragraph 407 through 411 discusses limitation 6d correct?

A Yes. 6 delta, that's correct.

Q Okay. And you do not rely on Haralabidis to teach limitation 6d, correct?

A That is correct. This is knowledge of a POSITA, as it says below, as reflected in my view in Miller and Beauchamp and such references. So that's -- this is met by the knowledge of a POSITA to add this piece in.

Q Now, let me just ask you a couple of hypothetical questions, if I may.

You ready?

A Oh, you asked me a question so I didn't know if I should answer it or not. So there's actually two questions there. I guess you can do that and I'm ready, so I'll see if I can even answer them or not.

Q Okay. If I have a chip with two supplies and two ground wires, can I short the two supplies on chip?

MR. ANDERSON: Objection to form.

A Well, by "short," I assume you mean connect together?

Q Correct.

A It's an option. You could do it. In fact, Saint does that in his case study 1. He actually connects all ground buses together for his ESD bus, the ground side of the ESD bus. It's a design option, doesn't mean it's a good one, but it's an option. It would have to be evaluated based on the tactical situation of what you would want to do to -- and, actually, Haralabidis actually addresses that there's many ways to do

that. So it's a design option, certainly.

Q If I have a chip with two supplies and two grounds, can I short the two ground wires on chip?

A Well, again, you could in the same way. It's a design choice if -- if it's between the layout and the blocks you have in the circuit, you could connect those two together. And again, Saint in his case study 1 does that. He doesn't in the 7.7 -- Figure 7.7 implementation, but he does that in his case study.

So again, it's a design option that would be a tactical decision based on where the wiring is and what kind of blocks you have. The type of blocks will define if you want to do that or not.

Q If I have a chip with two supplies and two grounds, can I short the two supplies off chip at the package level?

MR. ANDERSON: Objection, form.

A I don't know if the word "short" is what I'd call it, but you could have -- and again, in Saints, both in the 7.7 figure and in his case study you can have multiple power supply pads and

power supply pins on your package in particular situations. And in Saint's case study 1, he has four of them. He has a different power supply for each amplifier block in his design.

Q If I have a chip with two supplies and two grounds, can I short the two ground wires off chip on the printed circuit board?

MR. ANDERSON: Objection to form.

A You could do that, and that's what Haralabidis teaches. He pushes the -- as he describes in, I believe it's column 5, he pushes the unification out onto the printed circuit board because the traces are much bigger there. And because the traces are bigger, they have much lower resistance which means two things; it's a two-fer. You get better ESD shunting with less resistance because it goes through more readily; and any noise that's trying to propagate, say, between a noisy aggressor digital block and an analog block, by having it go out through that low-resistance pathway before it could sneak back it to the IC, it will be attenuated in that path

by going outside it.

So again, these are all design choices depending on the tactical situation of what your chip looks like and also what block you're using in that chip.

Q Would you agree with me that there's thousands of different design choices you could make when designing an integrated circuit?

MR. ANDERSON: Objection to form.

A Well, it would depend on the level you're discussing things, but there are a large number at each level in how you would tackle the logic design, how you would tackle the circuit design, the layout. There's options -- again, that's why a good layout person, they're sort of unsung heros of the business. But a good layout person is a gold mine. It's gold to have somebody like that on your team because they can optimize the design. They know from experience how to make it as small as possible and also how to make it robust so it doesn't get -- you don't have to do too much iteration.

So there's a lot of choices. It's a complicated matter, but the choices aren't random. It's a -- it's a driven process to get to a conclusion of a single chip that works well.

Q So you'd agree with me that there's thousand of designs choices that have to be made in the design of the layout; is that fair to say?

MR. ANDERSON: Objection to form.

A Well, I don't know if I characterize it by thousands, but there's many choices to be made. Many of the choices are in the individual blocks. Again, citing that figure from Uyemura's book, they're inside each one of those compartments: The physical design, the circuit design, the logic design, things like that. There's many choices.

That's why the process is driven in a particular direction, so the choices aren't being done sort of willy-nilly and independently. It's a very driven process and it obviously works because we're all today using a large number of successful ICs to have this call and to do this.

So many choices, but it's not just

randomly picking things out of thin air.

Q How many design choices would you say are made when designing a layout?

MR. ANDERSON: Objection to form.

A I don't know if I could quantify them because ultimately, again, it's almost like an art of who is the best artist at putting a layout together. A good -- it's like with anything, a good -- a good layout designer is almost like your maestro, a master painter who knows how to put things together in the best way.

How many choices there are? I haven't thought about it that way. The designer has to make -- the layout designer has to make numerous choices based on the ground rules, and also how you're going to place blocks and things of that nature.

So many choices are made but I don't know if I could quantify it because the process just is done by a talented person to get the conclusion you need.

Q So you want a talented person designing

your layout; is that fair to say?

A I would --

MR. ANDERSON: Objection to form.

A I would say that having done layout and learned a lot about it when I was a young engineer, a good layout person is very good to have because they can do that efficiently, quickly, optimally, and require -- it minimizes the iteration. And the iteration, particularly in the RF world, is what destroys companies if you never get out of the iteration loop. And a good layout designer will help you avoid the iteration hell you could get into.

Q A good layout person will help you avoid numerous -- numerous iterations of a particular layout or design --

A It will reduce --

Q -- is that fair?

A It will reduce that. A good layout person lets things get to the tapeout and getting -- remember, the objective is to get the chip finalized, the tapeout done, sent to the foundry

so they can make mask and make products. Because you're there to design the product, and if you don't design a product, you don't have a company basically.

Q Now, would you characterize the number of design choices a layout engineer has to make in the hundreds or in the thousands?

MR. ANDERSON: Objection to form.

A I wouldn't even care to quantify it. It's like asking, you know, how many choices did Michael Angelo make when he carved The David. It's similar to that. How do you quantify that? He made many choices obviously to create a masterpiece and it's the same thing here. A good layout designer is creating a masterpiece by making many decisions. I've never thought about it in terms of numbers of them.

MR. WATSON: Well, let's take our break. Let's take our break. Let's go off the record.

(Whereupon a break was had.)

BY MR. WATSON:

Q Dr. Foty, welcome back.

A Thank you.
Q Did you discuss the substance of your testimony with anyone during the break?
A I did not.
Q Let's pull up Exhibit 1001.
A That's the '164 patent.
REMOTE TECHNICIAN: Stand by, Counsel. I have my paper copy in front of me.
Q Do we have that on the screen?
A One second, please.
REMOTE TECHNICIAN: Did you say --
MR. WATSON: 1001.
REMOTE TECHNICIAN: My apologies. Loading that up right now.
Q Let's go down to claim 6. Are you at claim 6?
A Yes, I am. And I have it. It's in front of me on the screen and paper copy.
Q Claim 6 requires a plurality of pad groups adjacent and connected to the plurality of ESD buses.
Do you see that?

A I see that. Yes.
Q That limitation is not expressly taught by Yoshinaga, correct?
MR. ANDERSON: Objection to form.
A I would agree with that, why -- why it's done by obvious combinations.
Q You rely on obviousness to find that a plurality of pad groups adjacent and connected to the plurality of ESD buses was obvious?
A Yes. In the grounds where claim 6 is discussed, that is my conclusion and opinion is obvious by combinations.
Q Okay. Yoshinaga did not disclose a plurality of pad groups adjacent and connected to the plurality of ESD buses?
A He does not. And I actually don't even assert that he does.
Q Okay. Let's turn to your report, paragraph 13.
A I assume you mean declaration.
Q Declaration, yes.
A Again, I'm worried about somebody chasing

after me next week for this report which does -- which doesn't exist.

Q I deal with so many reports, Dr. Foty, that I just call it reports. But you're right, your declaration.

Let's turn to your declaration, paragraph 13.

A We should name everything "report" and make this easier for all of us anyway.

I have paragraph 13 open in front of me.

Q Okay. Paragraph 13 is the legal -- part of the legal standard you applied regarding anticipation, correct?

A Yes. That is correct. And I've, you know, obviously, been doing this a while so I've encountered this legal standard in one form or another before this matter.

Q I want to read the last sentence, if that's okay.

A Of paragraph 13?

Q Yes. "I have been informed that a prior art reference may anticipate a claim without

disclosing a feature of the claimed invention if that missing characteristic is necessarily present or inherent in the single anticipating reference as would have been understood by one of ordinary skill in the art."

Do you see that?

A I see that. Yes.

Q Are there any limitations that you -- strike that.

Are there any limitations in the claims of the '164 patent that you rely on these inherency doctrine to satisfy?

A No. Because my understanding is the inherency would have to be something like a well-known physical principle that doesn't need to be -- to be elucidated. For example, if you shine light on a wall and turn the flashlight, the beam is going to spread out. That would be something inherently a physical principle, which is why I didn't use anticipation in this analysis. I used -- I used the documentary evidence that I cited in some cases to show obviousness to

demonstrate what the knowledge of a POSITA was at the time, which is why it's an obviousness analysis in all three grounds, not an anticipation one.

Q So if any of the prior art references we just discussed does not explicitly disclose a limitation, that prior art reference does not anticipate that particular limitation; is that fair?

A I think that's fair. And that's why I did not use anticipation. I used the obviousness based on combinations and the demonstrated knowledge of a POSITA which meets the, I believe you folks call it the 103 standard.

Q Okay. And Dr. Foty, you didn't identify any objective indicia of nonobviousness in your declaration, correct?

A No, I did not. And there's something at the end, I believe, we're saying I don't -- at this point, I don't have any secondary considerations or things of that sort. It's all analysis is based on the obviousness, with the

caveat if something appears later, if that has to be revised based on something that YMTC brings up, then I reserve the right to address that as appropriate.

But I don't see any need to do that at this point. I don't cite any of those indicia or secondary considerations in my analysis answer.

MR. WATSON: I don't have any further questions.

THE WITNESS: Thank you, Counselor.

MR. ANDERSON: I think I'm going to take five to just review my notes and come back. And if I don't have any questions, I don't have any questions and we can wrap up.

(Whereupon a break was had.)

EXAMINATION

BY MR. ANDERSON:

Q Dr. Foty, I think moments ago you were talking with counsel regarding a limitation of claim 6 reciting a plurality of pad groups adjacent and connected to the plurality of ESD buses.

Do you recall that?

MR. WATSON: Objection, form.

A Yes, I recall that.

Q I just wanted you to open your declaration and we go ahead can look at a few paragraphs.

If you look at paragraph 132 of your declaration. Let me know when you have a second --

A It's element 6 Charlie, and it's broken up into claim said elements in my declaration.

Q Correct. Correct. And I believe if I remember correctly, you were saying that this was rendered obvious but not necessarily that Yoshinaga discloses it.

Do you recall testimony about that?

MR. WATSON: Objection, form.

A Yes. I recall that.

Q Okay. And so, if we step through the paragraphs here related to 6c, first, can you just review paragraphs 134 and 135? Then if you need more context, feel free to review other material there before I ask my question.

A Okay. Go ahead. I reviewed a little ahead because there's also 6 Charlie 1 and 6 Charlie 2.

Q Correct. And so for 6 Charlie 1, reciting a plurality of pad groups, does Yoshinaga disclose a plurality of pad groups?

A Yes.

MR. WATSON: Objection, form.

A Sorry. Yes, he does. He shows a plurality of pad groups, yes.

Q Okay. And for the next piece of this claim, let's move down, I believe, to paragraph 1 starting at 140.

Let me know when you're there.

A I have that in front of me.

Q And is it your opinion that Yoshinaga discloses the limitation adjacent and connected to the plurality of ESD buses?

MR. WATSON: Objection, form.

A Yes, it is because in this case, we're defining the ES -- we're allowing ESD buses to be defined by the, like, shape 19 in Yoshinaga. It's

not outside Yoshinaga but it's inside Yoshinaga, in fact.

Q Okay. And just to wrap it all up for this limitation 6 Charlie, it's your opinion that Yoshinaga discloses and/or renders obvious this limitation?

MR. WATSON: Objection, form.

A Yes, it is for the reason I said earlier, that in this particular case, we're -- we're saying it's met because it's referring to the, like, shape 19 in Yoshinaga where it's inside the pads. It's not outside the pads, but it's inside so it meets that based on the bus being inside of the pads inside the IC.

Q Okay.

MR. ANDERSON: No further questions from me, thank you.

MR. WATSON: Just a couple of redirect questions Dr. Foty.

FURTHER EXAMINATION

BY MR. WATSON:

Q Figure 6 does not show any potential

reference pads adjacent or connected to the ESD buses, correct?

MR. ANDERSON: Objection to form.

A It does not literally show them because as Yoshinaga said, the reference voltage pads are not shown to simplify the drawing, for whatever that means.

Q So there's no -- there's no express disclosure in Yoshinaga that pads 5 and 6 are adjacent and connected to the plurality of ESD buses, correct?

A There are no specific teachings regarding anything involving the reference voltage pads other than Yoshinaga essentially notes they have to be somewhere, but he says nothing about where. Doesn't even show suggestions. There's nothing.

Q So Yoshinaga does not teach pads that are adjacent and connected to the plurality of ESD buses, fair?

MR. ANDERSON: Objection to form.

A So -- sorry, what was that again? I --

Q Let me --

A Might have missed something in there.

Q No, no, no. Let me, let me rephrase the question.

Yoshinaga does not teach anything about the location of the reference potential pads, fair?

MR. ANDERSON: Objection to form.

A The -- he teaches that they have to be in there somewhere, but explicitly says nothing about them by saying he doesn't -- he wants to keep the drawing simple, for whatever that's worth.

MR. WATSON: No further questions for me.

MR. ANDERSON: I think that's it.

(Whereupon the proceedings were concluded at 3:51 p.m. EDT)

CERTIFICATE OF SHORTHAND REPORTER - NOTARY PUBLIC

I, Karisa Ekenseair, Certified Reporter and Notary Public within and for the State of Arkansas do hereby certify: That DANIEL FOTY, PHD, the witness whose deposition is hereinbefore set forth, was duly sworn by me before the commencement of such deposition and that such deposition was taken before me and is a true record of the testimony given by such witness.

I further certify that the adverse party, Petitioner was represented by counsel at the deposition.

I further certify that the deposition of DANIEL FOTY, PHD, occurred virtually on August 6 28, 2025, commencing at 9:03 A.M. EDT to 3:51 P.M. EDT.

I further certify the inspection, reading and signing of said deposition was not waived on the record by agreement of all parties.

I further certify that I am not related to any

of the parties to this action by blood or marriage, I am not employed by or an attorney to any of the parties to this action, and that I am in no way interested, financially or otherwise, in the outcome of this matter.

IN WITNESS WHEREOF, I have hereunto set my hand and affixed my notarial seal this 18th day of August, 2025.

My commission expires: 6-18-2028



Karisa Ekenseair, CCR, RPR RMR RDR LS#802
Notary Public in and for
Pulaski County, Arkansas
Commission No. 12704567

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