

P/G PAD PLACEMENT OPTIMIZATION: PROBLEM FORMULATION FOR BEST IR DROP

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ABSTRACT

IR drop minimization has become very difficult for non-flip chip packaged designs due to technology shrink and increasing design frequencies. Different constituents of IR drop on a wire-bond chip (where pads are placed at the die-periphery) are “Package-ball to bond-pad drop”, “bond-pad to internal global power ring drop” and “internal local power ring drop”. Optimization equations are developed to minimize IR drop from the lead-finger-frame to the standard cell power rails on the die by placing the P/G pads optimally for a given power network. Further, optimization equations are developed to minimize trace wire length on package for P/G pads drawing highest current. The cost functions in the optimization equations target minimum IR drop for those regions of the chip that are switching at maximum speed. By use of our cost function for optimizing P/G pad placement, results on the representative chip with about 15 million gates and several hard macros show an improvement of 10% to 15% in worst IR drop value for different floorplans (one floorplan with uniform power density, and the other floorplan with maximum power density much higher than the average power density of the design).

1 INTRODUCTION

With reducing chip dimensions and increasing frequency requirements, IR drop is fast becoming a dominant factor in determining the chip frequency. Due to on-chip IR drop, the voltage available across standard cells' supply rails is less than the power-supply voltage resulting into lesser drive current capability and therefore slower switching speeds. Worse, chip might not work at all due to hold violations, if due care is not taken in estimating the clock tree delays accurately with a given IR drop. This problem is hard to solve, as the voltage available at any spatial point in the chip is time varying and is dependent on the state of rest of the circuit. For making absolutely sure that the chip will function in all the use scenarios, it is suggested to perform dynamic IR drop analysis coupled with timing analysis for all possible use cases. Besides being computationally intensive, dynamic IR drop is a theoretically unsolvable problem as use cases are also dependent upon software, that is written for a particular application. However, all the applications of the chip might not even be known at design-

time. Due to these reasons, the most accepted method of designing-for-IR-drop includes following steps:

- Do worst case power consumption based static IR drop analysis.
- Build extra timing margin on setup and hold, assuming worst-case IR drop across the chip.

According to this methodology, design teams are required to ensure a given IR drop budget during worst case power consumption, depending upon the process and design parameters. Then, to build timing margin according to the IR drop budget, either cell libraries are characterized accordingly or a flat margin is built on top of the required chip functional frequency during physical synthesis and STA.

This methodology is also not completely error free. In [1], [2] authors prove that, assuming a static IR drop at the power grid is risky, as the results can be optimistic or pessimistic depending upon the circuit topology. Also, this approach of considering worst case IR drop requires designers to close timing at a much higher frequency than required across the chip. This over designing almost always causes higher power consumption. Worse, the circuit might remain under-designed (even with this approach) at the places where big supply spikes may remain undetected during static IR drop analysis. In [3] authors insist on the importance of dynamic IR drop analysis even though computationally expensive. In [4], [5] authors talk about the amount of decoupling capacitors needed on chip to counter the dynamic current spikes. In [6], using flip-chip packaging is considered to be the most effective solution for IR drop problems, which is more expensive than normal peripheral wire-bonded chips. In [7], authors discuss about the optimal planning for power mesh design, given a certain P/G pad placement.

Due to these accurate analysis problems, it is extremely necessary to limit the chip (static) IR drop to a minimum possible value for every given chip and its' design constraints. A very important factor that helps reduce the on-chip IR drop is the optimum placement of P/G pads at the chip periphery. In most cases, the number of P/G pads that can be assigned to power/ground signals is limited due to a constrained number of package pins. More the number of pins on the package, more is the package cost. On the other hand, for a given power ring structure, once the number of current sink points and general topology is

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decided, the problem of “power/ground I/O cell placement for minimum IR drop” can be solved as an optimization problem.

2 PROBLEM FORMULATION

Total IR drop on a wire-bond chip can be divided into following constituents (figure 1)

- Package ball to bond pad drop
- Bond pad to internal global ring drop (drop inside the I/O cell)
- Chip internal global ring to standard cell rail drop

The optimization equations developed as part of this work can be used to minimize all parts of chip IR drop. Power/ground pad placement directly affects all these components of IR drop because proximity of a P/G pad to chip internal current sinks affects the internal power ring drop. Also, length of the power and ground connecting bond wires on lead frame and therefore their resistance is determined by where these pads are placed on-die and therefore IR drop on package can be reasonably minimized by optimum pad placement.

The problem is formulated in two different parts. In first part optimization equations are developed for optimal pad placement depending upon the spatial current draw inside the chip. In the second part two different scenarios are considered. In first scenario the package design is assumed to be flexible, such that there is complete independence in placing the P/G pads on the periphery with sole intention of minimizing “global power ring” IR drop. In another scenario, package is assumed to be less flexible and therefore cost function optimization requires us to take care of the ball assignment constraints. Also, the equations only represent the power pad placement optimization, since the ground pad placement optimization problem is analogous to this.

2.1 Power ring structure

The representative power ring structure that has been considered is shown in figure 2. There is a global power ring all across the chip perimeter. Internal power network taps into this peripheral ring. P/G pads are placed all across the chip periphery. The tap points at which the internal power ring taps into this global/peripheral power ring are also shown. Typically, the global power ring is drawn in higher metal layers for two reasons. Firstly, the resistance of the higher metal layers is relatively less as compared to the lower layers, and secondly, all the current that flows in the chip passes through the global power ring, therefore making these wires a candidate for higher IR drop.

2.2 Power ring modeling

In figure 3 different power pads are shown at their respective locations. Similarly, the points at which internal chip power ring taps into the global power rings are shown as current drain sources. Figure 4 shows the “internal

current sources”, “voltage pads” and “global power ring” modeled as a simple “resistive circuit”. The segments of global ring connecting each voltage pad and current source can be replaced by the equivalent resistive value that is proportional to the segment length. Though, the value of the current sinks shown is dependent on the voltage potential that they receive from the global power ring, still for our problem formulation, they can be assumed as constant sinks of current without affecting the generality of the equations. This will also become evident from the subsequent discussion outlining the formal problem statement and its’ mathematical representation.

2.3 Cost function formulation for best IR drop

The objective of the pad placement is to make maximum voltage potential available at the current drain tap points on the global power ring. This can be achieved, if the current pumped in from the power pads is distributed in such a manner so as to minimize the current flowing in different segments of the global ring. This ensures that the IR drop from P/G cell to the current tap points is minimized and subsequently equivalent resistance seen from any power pad towards standard cell rails also decreases. To do this, it

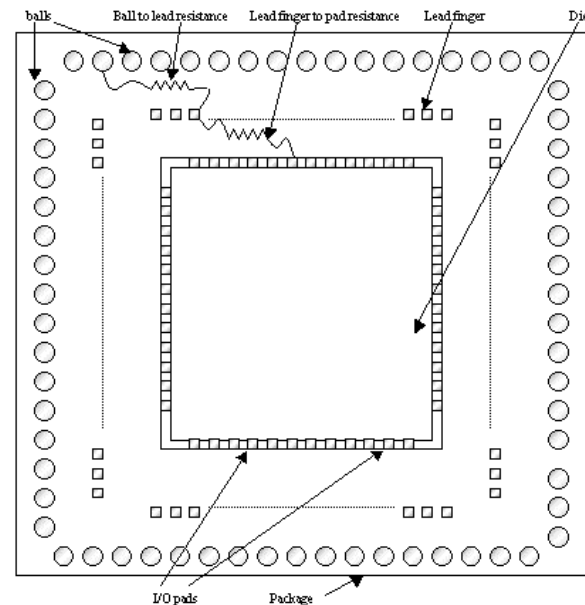


Figure 1 (Different components of IR drop)

is important that the resistance of the segments (and therefore its’ length) connecting any current tap point from the P/G pad be minimized. In other words, pad placement should be such that maximum part of the total current flows through minimum resistance i.e. minimum length of the global power ring.

Let us assume that a given global power ring has “m” pads as voltage sources according to the model developed in preceding section. Similarly the number of current tap points sinking off current from power ring are “n”.

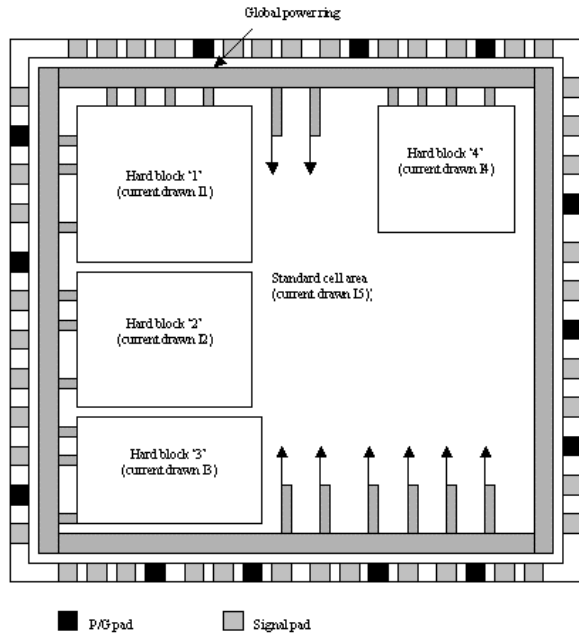


Figure 2 (Power ring structure)

Therefore for any given current drain source C_i , where “i” varies from 1 to “n”, the total current being fed in should encounter minimum possible resistance i.e. length of wire segments (On peripheral ring) from all the P/G pads to the current source location should be minimum i.e. minimize

$$\sum_{j=1}^m d_{ij}, \text{ where } d_{ij} \text{ is the distance of voltage pad } V_j \text{ from current source } C_i \dots (1)$$

Generalizing this over all the current drain sources and voltage pads we get to minimize the following term:

$$\text{minimize } \sum_{i=1}^n \sum_{j=1}^m d_{ij}, \text{ where “n” is the total number of current drain points and “m” is the total number of P/G pads} \dots (2)$$

If we try to optimize only equation (1) and (2) to achieve a good P/G pad placement then this will be an oversimplification of the problem. Figure 3 shows a typical model of a wire bond chip floorplan. The key thing to take note of is that the amount of current drawn by current sources from the global power ring is not equal spatially. Typically, different blocks in the design consume different power and consequently the current source that represents the highest power consuming block draws in the biggest current from the global power ring. Also, typically the block that consumes the highest power (and therefore draws the maximum current) also toggles at maximum frequency. This is because of the fact that active power is

directly proportional to the frequency of operation. In most of the chips, the blocks that toggle at the maximum frequency are most restrictive from IR drop perspective i.e. the IR drop in the maximum frequency region has to be minimized. This disparity in the current sources requires us to make sure that more power pads sit near to the highest current sources. To do this a weightage factor can be introduced in the optimization equation (2) such that:

$$\text{Minimize } \sum_{i=1}^n \sum_{j=1}^m w_i \cdot d_{ij} \dots (3)$$

In equation (3):

$$w_i = \frac{C_i}{\sum_{i=1}^n C_i}, \text{ Here } C_i \text{ is the amount of current being drawn by the current source “i”}.$$

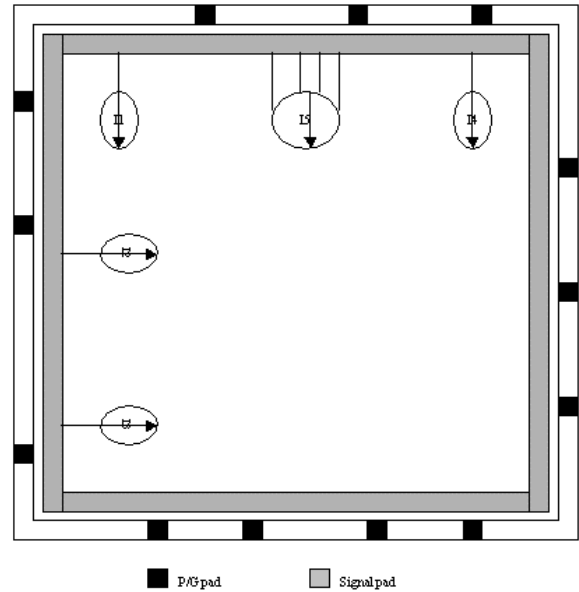


Figure 3 (taps from internal power network to global ring shown as current sources of different strength)

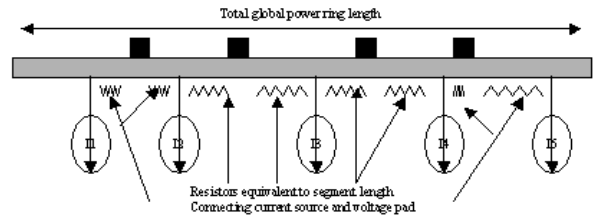


Figure 4 (global ring/current taps as resistive network)

2.3.1 Problem of multiple minimum values

Let us consider figure 5 (a) and (b). As indicated the value of optimization equation (3) in both figure 5(a) and figure

5(b) is $2.5R$, while the IR drop at the point where the current sinks connect to the global ring for these two cases are different.

In figure 5(a), IR drop for I_1 is $20/3R$, for I_2 it is 0, while for I_3 the number is $5/3R$. These numbers in figure 5(b), for I_1 , I_2 and I_3 are 0, $5/2R$ and $15/4R$ respectively. It is clear that for same values of optimization cost function in equation (3), the IR drop obtained is different. Therefore, something more needs to be added to refine the optimization equations. This is done by considering distances only to the “most effective pad” for any given current sink. Here, “most effective pad” is the pad sitting nearest to any current sink. The idea is that “nearer a P/G pad to a particular current sink, more the current that it will supply towards that sink”.

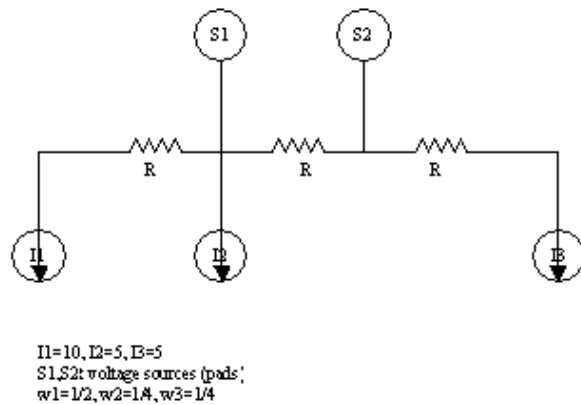


Figure 5(a)

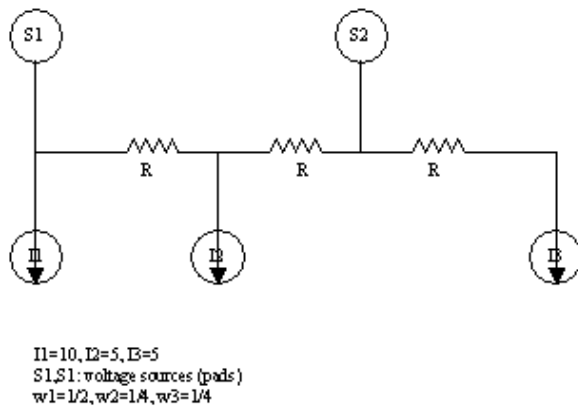


Figure 5(b)

2.3.2 Modified optimization equation

The intent of the optimization equation should be to make sure that:

“Maximum current encounters minimum resistance in the global power ring”

If we minimize the “minimum distance” of a power-pad from a current sink (i.e. minimizing distance to the “most effective pad” then we can achieve this objective. Therefore the modified optimization equation can be:

$$\text{Minimize } \sum_{i=1}^n \sum_{j=1}^m w_i d_{ij} a_{ij}, \text{ here } a_{ij}=1, \text{ if and only if the}$$

distance of power pad “j” from current source “i” is minimum i.e. for a particular solution:

$$a_{ik}=1, \text{ if } d_{ik} \leq d_{ij}, \forall j \text{ between 1 and m and for one and only one k. } \dots (4)$$

If we optimize cost function in equation (4) then, the intention of allowing maximum part of the chip current to pass through minimum resistance in the global grid can be satisfied. This is also inline with the “theory of superposition in passive electrical networks” as we are considering to minimize resistance encountered by each current-sink/voltage-pad pair independent of other current-sink/voltage-pad pairs.

The value of cost function in equation (4), in the two different cases shown in figure 5 (a) and 5 (b) is $3R$ and $2R$ respectively. Also, in 5(b), worst case IR drop is lesser than the IR drop in 5 (a) ($15/4R$ and $20/3R$ in 5 (b) and 5 (a) respectively).

This cost function can be optimized in multiple ways to achieve minimal IR drop in global power ring. If the number of power pads are already known then the problem formulation for minimal IR drop in global power ring is indicated by cost function in equation (4). On the other hand, if the number of P/G pads is not fixed and consequently an optimal number as well as locations of the pads need to be determined then problem formulation consists of optimizing cost function in equation (4) with an extra constraint on maximum number of P/G pads allowed on the package. i.e.

$$\text{Minimize } \sum_{i=1}^n \sum_{j=1}^m w_i d_{ij} a_{ij}, \text{ such that } m \leq M, \text{ here “M” is}$$

the maximum number of power pads allowed on the chip package. here $a_{ij}=1$, if and only if the distance of power pad “j” from current source “i” is minimum i.e. for a particular solution:

$$a_{ik}=1, \text{ if } d_{ik} \leq d_{ij}, \forall j \text{ between 1 and m and for one and only one k } \dots (5)$$

If we optimize (5), for a given number and value of current sources and the constraints on number of P/G pads, then an optimum placement as well as number of pads can be achieved.

2.3 Package considerations

As indicated by the figure (1), package lead frame to pad traces also contribute toward IR drop. As these traces are

much wider than the die-internal power geometries, therefore the skin effect in them is much more pronounced. This physical phenomena leads to these traces becoming one of the main contributors for inductive voltage drop, when current being drawn through the power rails changes abruptly. To reduce these effects as well as the normal static IR drop across the package traces it is important to consider them in our optimization equations. Two different scenarios can be considered for developing optimization equations.

2.3.1 Complete Package Flexibility

In this case, package design is done simultaneously with I/O ring design. Consequently, there is more flexibility in terms of

- Lead frame design
- Lead-frame-finger to P/G pad assignment

The bond wire resistive drop can be minimized, if the P/G pad assignment to lead-frame/ball is done judiciously. More the current being drawn from the I/O pad associated with the lead frame, more is the need for that particular bond wire to be short. The current drawn from any pad in turn is dependent upon the pad placement on the die periphery. Therefore, one possible way to reduce IR drop is the lead-finger to I/O pad reassignment. The intention should be to make sure that the bonding wire length for the I/O pad drawing maximum current should be minimized. Simultaneous optimization can be done for equation (4) with

$$\text{Minimize, } \sum_{i=1}^n a_i \cdot w_i \cdot l_i \dots\dots (6)$$

Here,

$a_i = 1$ if a pad is assigned to a particular lead-finger and 0 otherwise,

l_i is the length of a particular bond-wire from lead-finger to I/O pad, and

w_i is the weightage assigned to the P/G pad depending upon the amount of current that it sinks.

Equation (4) and (6) together can be optimized to minimize the lead-finger to global power ring IR drop. Alternatively equation (5) and (6) together can be optimized to determine the optimum number and the placement for P/G pads, given the maximum number of pads.

The problem of multiple minimums though theoretically possible is not considered here because of the following reasons:

- Typically each P/G pad is supported by one ball only

- Typically length minimization on traces is good enough, the extra factor of w_i is added to take care of corner cases for pads sitting close but still feeding in different amount of current.

2.3.2 No Package Flexibility

In many cases, the package for the part is already decided. This can happen due to legacy design or board development issues. In this case the ball locations and lead frame is already designed and is known. The little flexibility that is available is:

- the ability of the assembly house to bond to the different pad locations from the given lead frame.
- The flexibility of reassignment for lead-finger to P/G pad mapping

In case ball reassignment can be done, then cost function shown in equation (6) can be used with corresponding ball assignment constraints.

3 RESULTS

A floorplan for our chip is shown in figure (6). Numbers written within the blocks represent the power consumption of respective hard blocks. In the white region core standard cells are placed. *Most of the power pads in this design are to sit on top and bottom side of the die and therefore the primary current distribution network is vertical.* With this constraint on power network for the floorplan shown in figure (6), maximum power density is in the left side of the chip as 3 blocks with maximum power consumption ($I=660, 100$ and 440 respectively) are drawing current from pads sitting in the same region on top and bottom side of the die respectively. The maximum switching speed of the cells is also in this high power density region and that is where the maximum IR drop occurs as well. The total number of VDD pads allowed on top and bottom side are 18 and 17 respectively. All the results and numbers are calculated using AstroRail (Synopsys commercial tool)

In Table (1), worst case IR drop numbers for the floorplan in figure (6) with different P/G pad placement configurations is shown with respective values of cost function proposed in equation (4). As the value of cost function decreases from 836.36 to 448.96, worst case IR drop comes down from a worst value of ~ 75 mV to the best case value of ~ 63 mV. For a cost function reduction of about 50%, the gain in IR drop is about 16%. To make sure that this gain is not specific to the floorplan that we had, another set of experiments were done for a different floorplan shown in figure (7). The worst power density across this floorplan is lesser than the floorplan in figure (6). Also, the power distribution across the floorplan is more uniform. Table (2) captures the IR drop results that we obtained for different pad configurations. Here also, a decrease in value of cost function from 876.26 to 513.12, brings the IR drop down from 77.76 mV to 65.26 mV.

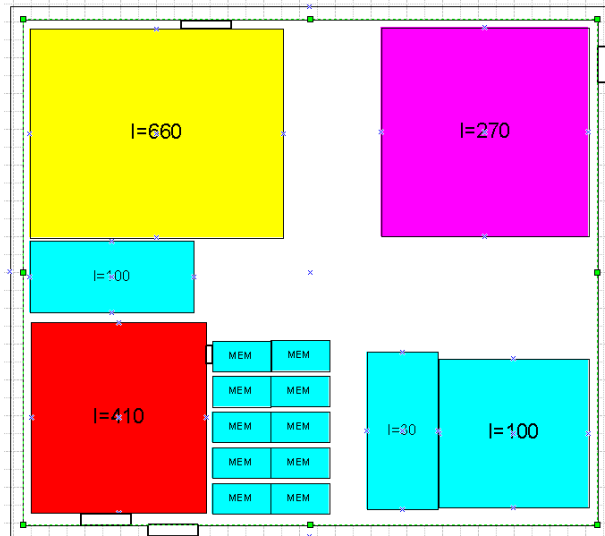


Figure 6: Floorplan '1' with max power density on left

Pad Configuration	Cost Function Value	IR-drop Value (mV)
1	836.36	75.18
2	766.36	74.52
3	646.31	73.32
4	551.12	69.29
5	501.23	66.4
6	480.3	65.4
7	448.96	63.5

Table (1): Results for Floorplan '1'

4 CONCLUSION AND FUTURE WORK

Optimization equations for better P/G pad placements are developed for least IR drop. The optimization equations are proved to give better results for a 15 million gate chip example. Any power network can be modeled as a current/voltage sink/source network and the optimization equation developed in this work can be solved to realize good P/G pad placement. The optimization equations can be solved by standard optimization algorithms.

As part of future work, optimization equations and methods are to be developed for "package ball reassignment" for IR drop minimization on package and die simultaneously.

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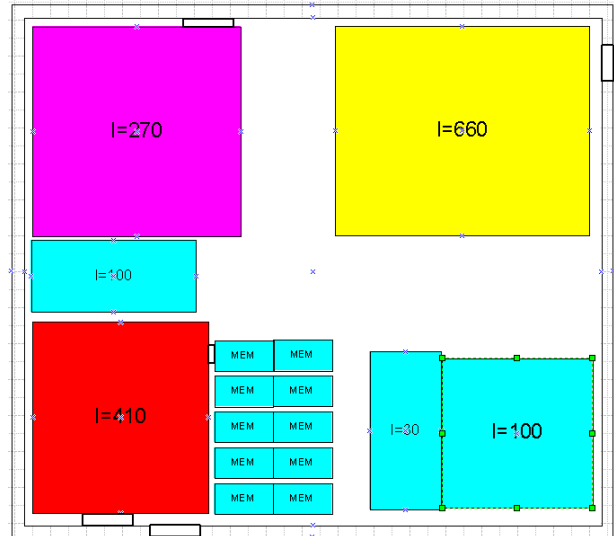


Figure (7): Floorplan '2' with equalized power density

Pad Configuration	Cost Function Value	IR-drop Value (mV)
1	876.26	77.76
2	840.67	76.31
3	730.92	76.06
4	658.45	73.12
5	628.81	72.94
6	548.69	69.38
7	513.12	65.26

Table (2): Results for Floorplan '2'

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