

Power Supply Pads Assignment for Maximum Timing Yield

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Abstract—The design of power distribution networks significantly impacts the timing of very large scale integrated chips. Process variations induce uncertainty in the current drawn off the network and, therefore, impose statistical measures on the supply voltage. This brief presents an optimization methodology for assigning power supply pads across the chip for maximizing the timing yield. A mixed-integer nonlinear programming optimization problem subject to the voltage drop and current constraints is efficiently solved to find the optimum number and location of the pads. The experimental results for ISCAS89 benchmark circuits demonstrate as much as a 30% improvement in the timing yield.

Index Terms—Leakage current, pad assignment, very large scale integration, voltage variations, yield optimization.

I. INTRODUCTION

POWER distribution networks must be designed with great care to ensure the delivery of the correct functionalities within a limited time. The increasing process variations, lower noise margins, and high electromigration in modern technologies make it even more challenging to design a robust power distribution network. The high number of power supply pads in such a design and the significant impact of their assignments to different nodes call for a robust solution.

The analysis and verification of power grids start from the early design phases [1], [2]. In recent years, the design of a power grid has been investigated in different areas and design stages. A wire-sizing optimization is discussed in [3], where the locality of the power grid is utilized to optimize the partitioned grid. The authors of [4] explained their method for floor planning and power network cosynthesis. Here, the area and the wire length are minimized while fixing the IR drop violations.

The authors of [5] and [6] optimized the topology of the power distribution network by including the routing congestion and area in their cost function. The optimization of a multilayer topology is studied in [7] and [8]. The objective is to minimize the IR drops by optimizing the wire width and reducing the mesh layer impedance. The authors of [9]–[11] optimized the number and location of the supply pads in order to bound the IR drop within its constraint. The optimization of the wire width in a power grid is discussed in [12] while addressing the reliability and the current density of the circuits.

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The deterministic approaches in the aforementioned work are no longer reliable under process variations. These variations impose statistical measures on the voltage drop due to the variations in the power consumption of the chip blocks [13]. The variations in supply voltage V_{dd} then introduce new sources of variations in the circuits' delay. The impact of the IR drop on the circuits' timing is examined in [14] and [15]. Here, the timing analysis is carried out to investigate the effect of the supply voltage variations on the critical path delay.

The location of the power supply pads, pins, and voltage regulators, hereafter referred to as pads, substantially affects the design. The magnitude of the voltage drops and their variations depend on the number and location of the pads. Consequently, the delay of the gates on a critical path can change with the pads' location. Therefore, it is critical to take into account the chip timing yield while assigning the pads on the power grid. Ignoring such dependence, under process variations, leads to unreliable designs that do not meet their timing objectives.

This brief formulates the pad assignment optimization as a mixed-integer nonlinear programming (MINLP) problem. Here, the objective is to minimize the timing yield loss. To the best of our knowledge, this is the first paper on pad assignment in presence of process variations. The constraint on the voltage drop ensures a sufficient noise margin and correct functionality. In addition, the maximum current constraints limit the current of the voltage regulator and guarantee the mean time to failure (MTTF) due to electromigration. The well-known macromodeling technique [17] is chosen in our method to increase efficiency, specifically for large power grids.

The proposed optimization methodology can be employed for finding either the best pad number and location at the chip level or for the pad/pin assignment at the block level. In addition, both wire-bond and flip-chip packages can use the methodology for locating the optimal pads on the peripheral power ring in the former case or for the over-the-block supply pins in the latter.

The rest of this brief is organized as follows. Section II explains the extraction of the voltage drop statistical moments. In Section III, the optimization constraints are detailed, and the timing yield loss is elaborated on as the objective function, respectively. The results are discussed in Section IV, followed by the conclusion in Section V.

II. VOLTAGE DROP AND SUPPLY CURRENT STATISTICS

The objective of this section is to model the supply voltage variations across the power grid. This is to accurately map the process variations to the statistics of the voltage drop across the power grid.

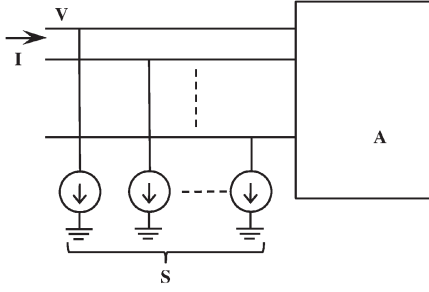


Fig. 1. Macromodel schematic.

In this brief, an RC network that is distributed over the die in multiple metal layers is considered. Each branch of the grid is modeled with a resistor, and all the nodes have a capacitor to the ground. In addition, an ideal current source is assumed to be connected to the nodes in the first metal layer (M1). The modified nodal analysis governs the relationship between the current and the voltage of each node, and it is expressed as

$$GV(t) + C \frac{V(t)}{dt} = -i(t) + GV_{dd} \quad (1)$$

where $V(t)$ is the vector of the voltages at each node, and $i(t)$ is the vector of the current sources. G and C are the conductance and capacitance matrices, respectively. An alternating-current (ac) analysis of the power grid provides more detailed information regarding the voltage drop waveform. It is useful to include the transient behavior of the power grid, specifically for studying the package, inductive noise, and decoupling capacitance. However, an ac analysis for pad assignment is expensive and can introduce error in the absence of detailed circuit information. Here, the supply pad currents follow the changes in power consumption at a lower frequency than the clock cycle [16]. In fact, for the reliable operation of the chip and in presence of a sound decoupling capacitance, the dynamic voltage of a power grid node remains close to the direct-current (dc) voltage level [9]. In addition, including transient data requires assumptions that can lead to inaccurate results. This occurs because there are various modes that the circuits can operate in. Therefore, a dc analysis is considered in this brief. Nevertheless, the methodology is flexible enough to take the trace of the dynamic power as the input and use the transient data for the ac analysis. To account for the temporal fluctuation in the currents, the methodology can be extended by applying the backward Euler integration formula [17]. Here, the macromodel idea can be extended by applying the backward Euler integration formula.

The matrix format of (1) is

$$GV = -I + GV_{dd} \quad (2)$$

where V is the vector of supply voltages, and I is the vector of the currents drawn off the power grid.

However, solving (2), as a part of an optimization problem, is very expensive due to the large number of nodes. Therefore, the macromodel idea in [17] is applied to reduce the number of nodes to a subset of selected nodes referred to as ports. The transfer characteristic of the macromodel, as shown in Fig. 1, is given by

$$I = A \cdot V + S, \quad I, V, S \in R^m, \quad A \in R^{m \times m} \quad (3)$$

where A is the port conductance matrix, S is the vector of all current sources connected to the ports, I is the vector of currents flowing into the model through the ports, V is a vector representing the port voltages, and m is the number of ports. In the macromodel, the internal nodes of the local grids are abstracted, and the current sources connected to these nodes are moved to the ports. In the proposed optimization, all the ports of the multiport model are considered as candidates for assigning the supply pads. The relationship between the components of the macromodel and those of the modified nodal system is determined by rearranging the original equations [17], such that

$$\begin{bmatrix} G_{11} & G_{12} \\ G_{12}^T & G_{22} \end{bmatrix} \begin{bmatrix} U \\ V \end{bmatrix} = \begin{bmatrix} J_1 \\ J_2 + I \end{bmatrix} \quad (4)$$

where G_{ij} is the submatrix of the conductance matrix, U is the vector of the internal nodes' voltage, and V is the vector of the ports' voltage. In addition, J_1 is the vector of current sources connected to the internal nodes, and J_2 denotes the current sources connected to the ports. A and S are obtained from

$$A = G_{22} - G_{12}^T G_{11}^{-1} G_{12} \quad S = G_{12}^T G_{11}^{-1} J_1 - J_2. \quad (5)$$

To avoid computing the inverse of a large matrix in the previous equation, as explained in [17], the submatrices of the Cholesky factors are used. The ports of the macromodel are partitioned to the assigned and observation ports. It is assumed that the assigned ports have an ideal voltage of V_{dd} . By rearranging the matrices, (3) is restated as follows:

$$\begin{bmatrix} A_{11} & A_{12} \\ A_{12}^T & A_{22} \end{bmatrix} \begin{bmatrix} V \\ V_{dd} \end{bmatrix} + \begin{bmatrix} S_1 \\ S_2 \end{bmatrix} = \begin{bmatrix} 0 \\ I \end{bmatrix} \quad (6)$$

where A_{ij} are the submatrices of A , V is the vector of the voltages at the observation ports, and S_1 and S_2 are the vectors of the current sources connected to the observation ports and the supply pads, respectively. In addition, I is the vector of the currents flowing into the model through the supply pads. Note that no current flows into the model through the observation ports. Let $\nu = V_{dd} - V$ be the vector of the voltage drops at the observation ports. From (6)

$$A_{11}\nu = A_{11}V_{dd} + A_{12}V_{dd} + S_1$$

$$I = A_{12}^T V_{dd} + A_{22}V_{dd} + S_2 - A_{12}^T \nu. \quad (7)$$

By applying the $E[\cdot]$ and $\text{Var}[\cdot]$ operators, as similarly done in [19], the statistical moments of the voltage drop are extracted by

$$E[\nu] = A_{11}^{-1} (A_{11}V_{dd} + A_{12}V_{dd} + E[S_1])$$

$$\text{Var}(\nu) = A_{11}^{-1(2)} \text{Var}(S_1) \quad (8)$$

where $A_{11}^{-1(2)}$ denotes a matrix whose elements are the square of each element in the inverse of A_{11} . In addition, from (7), the statistical moments of the currents, flowing into the model through the supply pads, are given by

$$\begin{aligned} E[I] &= A_{12}^T V_{dd} + A_{22}V_{dd} + E[S_2] - A_{12}^T E[\nu] \\ \text{Var}(I) &= \text{Var}(S_2 - A_{12}^T \nu). \end{aligned} \quad (9)$$

The locality of the grid problem (see [20]) states that the voltage drop is closely related to the variations in the neighboring current sources. Therefore, it is safe to assume that the two components in (9), i.e., S_2 and $A_{12}^T \nu$, are not highly correlated. Here, S_2 is the vector of the current sources connected to the power pads, and ν denotes the voltage drops at the observation ports. Consequently

$$\text{Var}(I) = \text{Var}(S_2) + A_{12}^{T(2)} \text{Var}(\nu). \quad (10)$$

The statistics of the voltage drops and currents are used in the next section to put an upper bound on their respective constraints.

III. DESIGN CONSTRAINTS AND YIELD OPTIMIZATION

Assigning the power pads changes the voltage drop profile across the chip. The delay of the gates on the critical paths is sensitive to these voltage drops. Under process variations, the voltage drops have statistical measures, which, in turn, introduce new sources of uncertainty in the delay. Therefore, the pad assignment impacts the delay, such that a noncritical path can become critical.

To optimally assign the supply pad to the correct ports, the die area is discretized into tiles. The candidate pads are selected from each tile, where the selection depends on the package design. For example, in a flip-chip package, the C4 bump locations determine the candidate power pads. In a wire-bound package, the location of the terminals, routed to the peripheral power ring, determines where the candidate pads should be located.

To capture the impact of the voltage drop variations on the delay, the objective function is formulated by the linear regression

$$f = \sum_{j=1}^n a_j w_j (\mu_{\nu_j} + r \sigma_{\nu_j}) \quad (11)$$

where n is the number of tiles, w_j is the weighting factor, a_j is the delay sensitivity to the voltage drop in tile j , μ_{ν_j} is the expected value, and σ_{ν_j} is the standard deviation of the voltage drop distribution in tile j . In addition, r is determined by the distribution confidence level in the ν upper bound. For minimizing the delay, all the potential critical paths are taken into account. Many of them pass through different tiles. Assigning a supply pad in a tile with a larger number of critical paths has a larger effect on the delay. Therefore, in the cost function, a weighting factor, which is given to each tile, is used to take this point into consideration. In addition, note that cumulative distribution function and its inverse are monotonically increasing functions, and therefore, minimizing the upper confidence level of the delay distribution is equivalent to maximizing the timing yield.

In regard to the constraints, for the limited number of pads, the power grid should meet the maximum voltage drop constraint ($\mu_{\nu_j} + r \sigma_{\nu_j} \leq \nu_t$). This ensures valid functionalities, as well as acceptable noise margins across the chip.

In addition, the current that flows through the supply pad must not exceed the threshold value ($\mu_{I_j} + r \sigma_{I_j} \leq I_t$). This constraint guarantees that the MTF, due to electromigration,

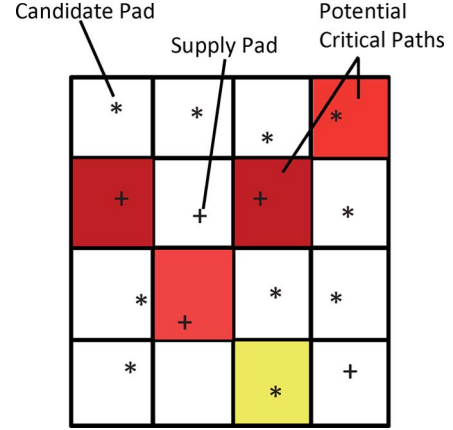


Fig. 2. Discretized die area, tiles that share the critical paths, and candidate pads. The darker color represents a larger weighting factor for the respective tile, where it shares a larger number of critical paths.

in the respective wires and contacts, meets the requirement. In addition, the upper bound on the supply current leads to a more uniform current density profile and, thus, more reliable circuits [23]. Note that, because the currents have statistical measures, we have to constrain their upper bound. In addition, not all candidate nodes are connected to a pad. Therefore, integer variable y_j is used to enforce this requirement. This only suggests increasing the number of pads if required, where the location of the pads is mainly suggested by the other constraints.

Moreover, the expected values and variance of the voltage drops and the currents must satisfy (8) and (9). Finally, the number of pads is limited.

In the optimization problem, the following MINLP problem is formed:

$$\min \sum_{j=1}^n a_j w_j (\mu_{\nu_j} + r \sigma_{\nu_j}) (1 - y_j), \quad y_j \in \{0, 1\}$$

subject to:

$$\begin{aligned} \mu_{\nu_j} + r \sigma_{\nu_j} &\leq \nu_t (1 - y_j) \\ \mu_{\nu_j} &= [A_{11}^{-1} (A_{11} V_{dd} + A_{12} V_{dd} + \mu_{S_1})]_j (1 - y_j) \\ \sigma_{\nu_j}^2 &= [A_{11}^{-1(2)} \sigma_{S_1}^2]_j (1 - y_j) \\ \mu_{I_j} + r \sigma_{I_j} &\leq I_t y_j \\ \mu_{I_j} &= [A_{12}^T V_{dd} + A_{22} V_{dd} + \mu_{S_2} - A_{12}^T \mu_{\nu}]_j y_j \\ \sigma_{I_j}^2 &= [\sigma_{S_2}^2 + A_{12}^{T(2)} \sigma_{\nu}^2]_j y_j \\ \sum_{j=1}^n y_j &\leq N \\ \mu_{\nu_j}, \sigma_{\nu_j}, \mu_{I_j}, \sigma_{I_j} &\geq 0 \\ \forall k, l \in \{1, 2\} : \\ A_{kl} &= \{A\}_{kl}^y \\ \mu_{S_k} &= \{\mu_S\}_k^y, \text{ and} \\ \sigma_{S_k} &= \{\sigma_S\}_k^y \end{aligned} \quad (12)$$

where N is the number of candidate pads. The output of the MINLP problem consists of the values for the continuous variables, i.e., μ_{ν_j} and σ_{ν_j} , as well as the integer variable y_j for $\forall j = 1, \dots, N$. The use of y_j and $1 - y_j$ in the respective constraints enforces port partitioning to the assigned ports

TABLE I
TIMING YIELD AND STATISTICS OF DELAY, COMPARING THE OPTIMAL AND RANDOM SUPPLY PAD ASSIGNMENTS

Circuit			Power Grid		Our Optimization Method			Random Assignment		Target Delay (picosecond)	Yield Improvement (%)
Name	Number of Cells	Number of Candidate Pads	Number of Nodes	Maximum Number of Pads	Delay Mean (picosecond)	Delay Std (picosecond)	Optimal Number of Pads	Delay Mean (picosecond)	Delay Std (picosecond)		
s1196	547	16	4,762	8	480.26	48.56	6	490.81	52.21	436.58	3.5
s5378	2958	64	16,642	16	381.59	33.27	15	406.72	37.05	363.51	17.2
s9234	5825	64	16,642	16	679.74	57.02	16	746.61	59.60	602.36	8.0
s13207	8260	64	16,642	24	1073.23	96.87	24	1171.74	129.12	1058.08	24.9
s15850	10369	64	82,370	24	1286.26	111.98	23	1383.60	121.89	1194.87	14.6
s35932	17793	64	82,370	24	1081.22	88.47	20	1104.10	90.32	1046.10	8.5
s38417	23815	100	434,282	32	886.02	77.02	27	985.55	101.85	875.50	30.6
s38584	20705	100	434,282	32	1534.06	130.98	32	1618.38	134.05	1530.94	23.3

($y = 1$) and to the observation ports ($y = 0$) and ensures the feasibility of the solution. The submatrices of A and subvectors of μ_S and σ_S change during the optimization process by repartitioning their elements using the integer variables in y . Here, $\{.\}^y$ denotes partitioning a matrix/vector according to vector y . In addition, $[\cdot]_j$ represents mapping of an element in the partitioned vector back to the original vector.

IV. RESULTS AND DISCUSSION

The proposed method is implemented in C++ and MATLAB and executed on a 3.4-GHz Pentium-4 personal computer with 2-GB random access memory. The experiments are performed on edge-triggered ISCAS89 benchmarks by using 65-nm technology parameters. The process parameters are adapted from [21]. In regard to the power grid, the metal layers, pitch, and width per layer are selected according to the IBM benchmarks [22], scaled for 65-nm technology.

To set up the MINLP problem and test it on the benchmark circuits, the following steps are adhered to.

- Step 1. Place and route the circuits. They are initially placed by using Capo [24], and a global routing is performed for all the nets. Then, the die area is discretized into a number of tiles by the tool for both the delay calculation and pad assignment. The number of tiles is selected according to the size of the circuits.
- Step 2. Estimate the statistical moments of the current sources in each tile. The simulation data are chosen for the benchmark circuit instead of random current sources (see [15]). This makes the results more accurate. This step is performed by using an in-house tool set.
- Step 3. Extract the potential critical paths. Monte Carlo simulations are executed for each circuit under process variations, and the critical paths are stored in each run. In the end, the tiles' weighting factors are calculated, based on the total number of the critical paths in all the runs, for each tile. Fig. 2 reflects an example of the discretized die area, the tiles that share critical paths, and the candidate pads. The darker color represents a larger weighting factor for the respective tile, where it shares a larger number of critical paths.
- Step 4. Reduce the size of the problem by employing the macromodel technique, where the components of the macromodel are extracted according to (5). We

TABLE II
RUNTIME OF THE PAD ASSIGNMENT OPTIMIZATION AND MACROMODEL EXTRACTION

Circuit			Runtime		
Name	Number of Candidate Pads	Number of Nodes	Macro Model Extraction (second)	Optimization (second)	Total (second)
s1196	16	4,762	1	4	5
s5378	64	16,642	1	14	15
s9234	64	16,642	1	16	17
s13207	64	16,642	1	22	23
s15850	64	82,370	1	19	20
s35932	64	82,370	1	20	22
s38417	100	434,282	16	136	152
s38584	100	434,282	16	138	154

assume that only one connection exists per tile. For larger number of pad candidates, the number of tiles must be increased.

- Step 5. Solve the optimization problem with additional partitioning, as described in the previous section. TOMLAB is used as the optimization engine, where its minlpBB solver utilizes the branch-and-bound search scheme.
- Step 6. Estimate the timing yield for the optimal supply pad assignment. Here, the statistical timing analysis is carried out for the circuits by taking into account the statistical moments of the voltage drop in each tile.

The previous steps are followed for different circuits and power grids. Table I demonstrates the delay statistics for the optimal and random pad assignments. The number of candidate pads is chosen according to the size of the circuit. In addition, the target delay is assumed to be the upper bound ($\mu + 3\sigma$) of the circuit delay, where each node has an ideal supply voltage. It is observed that the optimal pad assignment can significantly improve the timing yield. For example, the yield increases by 30.6% in the case of the s38417 circuit.

The runtime of the optimization method consists of the time spent on macromodel extraction and the time required to solve the MINLP problem. As summarized in Table II, the components of the macromodel are efficiently extracted by using the submatrices of the Cholesky factors [17]. However, for a large number of pad candidates, a few minutes is needed to find the optimal pad assignment. This can be improved by defining the priority order in which the noninteger variables are selected.

The magnitude of the yield enhancement depends on several parameters, including the number of pads, size of the power

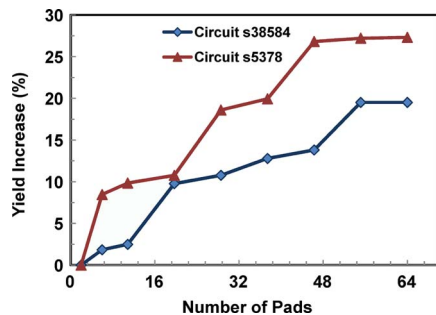


Fig. 3. Timing yield sensitivity of two test circuits as a function of the number of supply pads.

grid, and current sources. In addition to the pads, a larger yield is observed for the larger power grids. When the size of the power grid increases, the effective impedance of the grid is reduced such that the voltage drop decreases. However, as depicted in Fig. 3, the circuits demonstrate a different yield sensitivity in respect to the total number of supply pads. However, for all the circuits, the effectiveness of the pad assignment decreases as the number of pads increases.

The most effective fixes must be made early in the design cycle to utilize the higher degrees of freedom. The supply pad assignment can be performed as early as floor planning. However, the assignment greatly depends on the power density map. Therefore, in the absence of the detailed information, the designer must deal with some uncertainties. Here, there is a large number of working modes for the circuit blocks to be considered. One can conduct a worst case analysis and assume that all the blocks are on simultaneously. To avoid the false alarm due to the pessimistic assumption, as explained in [1] for the power grid, a set of power and synchronization constraints can be specified. The power constraints limit the blocks' power, as well as the total design power, and the synchronization constraint demands that two blocks work together. According to these constraints, the distributions of the block's current are approximated, and the optimal pad locations are selected. Subsequently, as more information becomes available, routing paths, wire sizes, and the power grids are modified. As a result, the fine-grain power density map is obtained, and the locations of the pads are adjusted so that the timing yield is enhanced.

Note that, to find the optimal pad assignment considering the temporal fluctuation in the current, the macromodel idea is used to model the system with matrix A in the first time step. Then, the extracted matrix A is rearranged in the subsequent time steps to find the local optimal solution. Here, the optimization problem is extended to a number of successive time steps where the global optimal pad assignment is found.

V. CONCLUSION

The supply pad assignment significantly impacts the chip performance and reliability. Under process variations, a nonoptimal pad selection can result in a design that does not meet its set objective. This brief has proposed an optimization methodology for supply pad assignment. Here, the statistics of the currents, drawn off the power grid, have been used to bound the voltage drops and supply currents across the die. An MINLP problem is formed to maximize the timing yield while addressing the noise margin and electromigration concerns. The results

demonstrate large yield improvements. Finally, by utilizing the macromodel technique, the optimal solution converges in a few minutes.

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