

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2025-00118
Patent 10,879,164

**DECLARATION OF SUNIL KHATRI
IN SUPPORT OF
PATENT OWNER'S RESPONSE**

Table of Contents

I.	Background and Qualifications	1
II.	Summary Of Materials Reviewed And Considered	14
III.	Understanding of Legal Standards	15
IV.	Level of Ordinary Skill in the Art	20
V.	The '164 Patent	21
VI.	Claim Construction.....	24
VII.	Ground 1	24
A.	Ground 1: Yoshinaga, Saint, and POSITA Knowledge Do Not Render Obvious “a plurality of pad groups, adjacent and connected to the plurality of ESD buses” (claims 6-7) or “wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses” (claims 12 and 14)	24
B.	Ground 1: Yoshinaga, Saint, and POSITA Knowledge Do Not Render Obvious “a plurality of bonding wires configured to connect one to another of the plurality of pad groups” (claims 6 and 7) or “connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires” (claims 12 and 14)	48
C.	Ground 1: Yoshinaga, Saint, and POSITA Knowledge Do Not Render Obvious “wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area” (claims 6-7, 12, 14).....	63
VIII.	Ground II	72
A.	Ground 2: Yoshinaga, Saint, Haralabidis, and POSITA Knowledge Do Not Render Obvious “plurality of pad groups” “adjacent and connected to the plurality of ESD buses” (claims 1-6, 8-11, and 13)	72

B.	Ground 2: Yoshinaga, Saint, Haralabidis, and POSITA Knowledge Do Not Render Obvious “a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus”, “connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires,” and “connecting” pad groups “to another of the plurality of pad groups” (claims 1-6, 8-11, and 13).....	73
C.	Ground 2: Yoshinaga, Saint, Haralabidis and POSITA Knowledge Do Not Render Obvious “wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area” (claims 1-6, 8-11, and 13).....	78
IX.	Ground III.....	79
A.	Ground 3: Saint, Haralabidis, and POSITA Knowledge Does Not Disclose Or Render Obvious “a common ESD bus” (claims 1-5, 8-11).....	79
B.	Ground 3: Saint, Haralabidis, and POSITA Knowledge Do Not Render Obvious “connecting” the “pad groups” to either “another of the plurality of pad groups” (claims 6-7, 12-14) or “to the common ESD bus” by “bonding wires,” (claims 1-5, 8-11)	86
C.	Ground 3: Saint, Haralabidis and POSITA Knowledge Do Not Render Obvious “wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area” (claims 1-14).....	88
X.	Conclusion.....	95

1. I have been retained on behalf of YMTC (“YMTC”), and its counsel, Latham & Watkins LLP, to provide expert opinions relating to U.S. Patent 10,879,164 (“Asserted Patent” or “’164 Patent” (Ex.1001)) in connection with Micron’s Petition for *inter partes* review. I am personally knowledgeable about the matters stated herein and am competent to make this declaration.

2. I am being compensated for my time at my standard hourly rate of \$800 per hour.

3. This declaration, including the exhibits hereto and cited materials, identifies my opinions to date, although I may provide further testimony and opinions if asked to testify in court or at a deposition. I also reserve the right to supplement or amend my opinions, as well as the bases for those opinions, if I receive additional relevant information or to respond to opinions offered by other experts in this case. I may rely on demonstrative exhibits, including pictures, figures, and drawings that appear in this declaration and the referenced exhibits and materials.

I. Background and Qualifications

4. I have over thirty-five years of experience with electronics, electrical engineering, and computer engineering. A copy of my latest curriculum vitae (CV) was submitted as Exhibit 2006 and provides further

details regarding my background and qualifications.

5. During my career, I have acquired extensive knowledge and experience with VLSI circuits, computer architecture, testing, computer-aided design (CAD) algorithms and algorithm acceleration, logic synthesis, semiconductor memory, redundancy, synchronous and asynchronous circuits, and related software and hardware topics. Most relevant to the Asserted Patent my technical expertise includes extensive work with semiconductor integrated circuits (ICs), including the design and layout of input/output (IO) drivers and their electrostatic discharge (ESD) circuits. This work was performed for a commercial microprocessor IC, as well as 3 ICs whose fabrication I led at Texas A&M University, each of which utilized ESD circuitry. I have one US patent in the area of IO driver design. My work on semiconductor memory devices has included work on 3D integration and novel ring-based memory architectures, power and speed tradeoffs using selective body bias, architectures and circuit approaches for processing-in-memory, radiation hardening analysis for memories, the use of flash transistors for designing logic circuits (such as ternary Content-addressable Memories (CAMs), Field Programmable Gate Arrays (FPGAs), and traditional binary-valued as well as ternary-valued digital logic, secure logic circuits, analog circuits like Finite Impulse Response (FIR) filters, Discrete Fourier Transform (DFT) circuits, and in-memory mixed-signal

computing architectures like Convolutional Neural Networks (CNNs)), large language models (LLMs) and clocking and source-synchronous design. I recently was awarded a research grant by the Air Force Research Laboratory (AFRL) in Rome, New York, to conduct research in secure digital circuits using flash-based digital design approaches.

6. Another recent research grant from the National Science Foundation (NSF) is funding research on the use of flash transistors for general purpose mixed-signal arithmetic. Additionally, I have led-authored a book chapter on the use of flash transistors in novel Very Large Scale Integrated (VLSI) design applications. My Master of Science (“M.S.”) thesis involved designing a memory interface for a multi-threaded Reduced Instruction Set Computing (RISC) microprocessor.

7. The following describes some of my relevant experience. I earned my Bachelor of Science (“B.S.”) in Electrical Engineering in 1987 from the Indian Institute of Technology, Kanpur, India. After graduating with my B.S. degree, I was a candidate for a M.S. degree in Electrical and Computer Engineering at the University of Texas from 1987–89. At the University of Texas, I held the Microelectronics and Computer Development (MCD) Fellowship from 1987–89. I also conducted my M.S. research and wrote my thesis on the design of the METRIC memory interface and memory system.

METRIC was one of the first super-scalar processors that was developed in the world. I earned an M.S. degree in 1989 from the University of Texas, Austin.

8. After leaving the University of Texas, I worked at Motorola Inc., from 1989–93 as a design engineer for the MC88110 and PowerPC 603 reduced instruction set computing (RISC) microprocessor teams. My duties included the design of digital and analog circuitry, test logic and circuits, JTAG boundary scan design, input/output driver design (including ESD circuits in these drivers), and clock phase-locked loop (PLL) logic. During my time at Motorola, I was independently responsible for the design of the factory test controller of the MC88110 microprocessor. I performed all attendant tasks in a “vertical” VLSI design methodology, which included high-level modeling, circuit and layout design and verification, as well as global and detailed routing. I also helped in the design of the Translation Lookaside Buffer (TLB) unit, which included a static random-access memory (SRAM) block.

9. In 1999, I earned a Doctor of Philosophy degree in Electrical Engineering and Computer Sciences from the University of California, Berkeley. While at Berkeley, I held the California Microelectronics (MICRO) Fellowship in 1993.

10. I joined the faculty at the University of Colorado, Boulder, in 2000 as an Assistant Professor of Electrical and Computer Engineering. At the

University of Colorado my research focused on VLSI logic design automation, VLSI layout design automation, and VLSI design methodologies to address Deep Submicron (DSM) issues such as crosstalk and power.

11. I joined the faculty at Texas A&M University in 2004 as an Assistant Professor in Electrical and Computer Engineering. In 2010, I was promoted to Associate Professor in Electrical and Computer Engineering. In 2015, I was promoted to full Professor in Electrical and Computer Engineering. My research focuses on three primary areas: the first is computer systems, including computer architecture from the circuits up, and algorithm acceleration using GPUs, FPGAs and custom ICs. The second is logic and its applications, while the third area consists of interdisciplinary extensions of the first two. Some specific recent research topics include circuit design using floating gate (flash) devices, wireless power delivery and battery-less electronic systems, machine learning architectures, secure computing approached from both a hardware and software perspective, a formal framework for designing and verifying cryptographic hash functions, and extreme high-speed serial interfaces for Artificial Intelligence / Machine Learning (AI/ML) systems such as those used in Large Language Models (LLMs) like ChatGPT. One of my new focus areas is intelligent and secure computing viewed from the hardware (circuit) as well as the software levels. I have conducted research on tamper-

proof memory techniques, as well as multi-row read architectures for SRAM, DRAM and flash memory arrays.

12. At Texas A&M I teach classes that cover circuit design and memories extensively, featuring thorough discussion of sense amplifiers, row and column decoders, and different types of memory circuits. For example, in Electrical and Computer Engineering (ECEN) 752 “Advances in VLSI Circuit Design,” a graduate level course, I cover all aspects of VLSI design, including memory design for various types of memories as well as IO drivers and ESD. In this course, (and also in ECEN 449/749 “Microprocessor System Design”), I cover memories, including flash memories, the design of flash memory cells, the organization of memories into multiple banks, and the division of data across multiple banks of memory, as well as other design techniques that can be used to optimize and manage memories. The ECEN 449/749 course is attended by both undergraduate (ECEN 449) and graduate (ECEN 749) students. In ECEN 454 “Digital Circuit Design,” a senior undergraduate course, I cover circuit design techniques for memory in detail. The Ph.D. thesis dissertation topic for three of my current Ph.D. students covers the use of flash memory transistors for analog and digital applications. The Ph.D. thesis of one of my recent doctoral students dealt with the use of flash transistors to design logic circuits. The research of a recent M.S. student entailed a new ring-based

source synchronous architecture for 3D DRAM technologies, which has been published at a conference and in a journal and is being submitted for dissemination as a research monograph. In the past, I have conducted research into new topologies for efficient memory redundancy as part of a course project for my graduate course.

13. Since 2000, I have earned at least 24 research contracts from funders including Intel, the National Science Foundation, the National Security Agency, Altera Corporation, the National Center for Atmospheric Research, National Semiconductor Corporation, and several private sources. The total amount for these research grants is at least \$17.53 million, of which my portion is at least \$2.85 million.

14. I have authored or co-authored over 289 peer-reviewed publications. Among these papers, five received a best paper award, while seven others received best paper nominations (including one journal best paper nomination). An additional six journal papers and three conference paper are currently undergoing peer review. I have co-authored nine research monographs, one edited research monograph, and four book chapters. Additionally, I have seven awarded U.S. Patents (two of which were filed during my tenure at Texas A&M), two filed provisional U.S. Patents, and another U.S. Patent, which is currently under review and was also submitted

during my tenure at Texas A&M. I have co-authored one invited journal paper and 13 invited conference or workshop papers (including one from Design Automation Conference (DAC) and one from Allerton). Moreover, I was invited to serve as a panelist at a conference seven times and have presented four conference tutorials. I received the “Outstanding Professor Award” in the ECE Department at Texas A&M University in 2007 and also in 2020. In 2009 and in 2019, I received a university-level and a college-level teaching award respectively, at Texas A&M. My H-index is 36 (per Google Scholar).

15. Since 2003, I have published numerous research monographs, journal papers, and conference papers on flash transistors and memory systems, as well as IO drivers, as detailed in my CV (Ex.2006). A few papers on relevant subject areas authored or co-authored by me include:

- “*Flash - A ‘Forgotten’ Technology in VLSI Design*,” Khatri, Vrudhula, Abusultan, Bharathi, Chu, Lee, Scott, Singh, Wagle. Appears “Frontiers of Quality Electronic Design (QED).” Springer publishers, Sept. 2022, pp. 67-136. Ali Iranmanesh, ed. ISBN: 978-3-031-16344-9;
- “*Flash – An Overlooked Technology in VLSI Design*,” Khatri, Vrudhula. Monday Tutorial to be presented at the ACM/CEDA

Design Automation Conference (DAC), San Francisco, CA, June 2024;

- “*A Mixed-Signal Quantized Neural Network Accelerator Using Flash Transistors*,” Scott, Lee, Khatri, Vrudhula. IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 71, no. 3, pp. 1025-1038, Mar. 2024;
- “*An ASIC Accelerator for QNN With Variable Precision and Tunable Energy-Efficiency*,” Wagle, Singh, Khatri Vrudhula. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Jan. 2024;
- “*A Digital Low Dropout (LDO) Voltage Regulator Using Pseudoflash Transistors*,” Lee, Khatri. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 31, no. 12, pp. 1960-1969, Dec. 2023;
- “*A Novel ASIC Design Flow using Weight-tunable Binary Neurons as Standard Cells*,” Wagle, Singh, Khatri, Vrudhula. IEEE Transactions on Circuits and Systems I (Regular Papers), vol. 69, no. 7, pp. 2968-2981, Sept. 2022;

- “*CIDAN-XE: Computing in DRAM with Artificial Neurons*,” Singh, Wagle, Khatri, Vrudhula. *Frontiers in Electronics*, section Integrated Circuits and VLSI. vol. 3, Feb. 2022;
- “*An Extremely Low-Voltage Floating Gate Artificial Neuron*,” Scott, Khatri. 2023 IEEE International Conference on Circuits and Systems (ISCAS), May 21-25, 2023, Monterey, CA;
- “*A Novel Pseudo-Flash Based Digital Low Dropout (LDO) Voltage Regulator*,” Lee, Khatri, Vrudhula. 2023 International Symposium on Quality Electronic Design (ISQED), Apr. 5-7 2023, San Francisco, CA;
- “*A Flash-based Digital to Analog Converter for Low Power Applications*,” Scott, Khatri. IEEE 40th International Conference on Computer Design (ICCD), pp. 1-8, Oct. 2022, Lake Tahoe, CA;
- “*A Flash-based Current-mode IC to Realize Quantized Neural Networks*,” Scott, Lee, Khatri, Vrudhula. IEEE Design Automation and Test in Europe Conference, pp. 1029-1034, Mar. 2022, Antwerp, Belgium;
- “*CIDAN: Computing in DRAM with Artificial Neurons*,” Singh, Wagle, Vrudhula, Khatri. 39th IEEE International Conference on

Computer Design (ICCD) 2021, pp 349-356, Oct. 2021 (virtual conference);

- “*A Statistical Methodology for Post-Fabrication Weight Tuning in a Binary Perceptron*,” Azari, Wagle, Khatri, Vrudhula. IEEE 21st International Symposium on Quality Electronic Design (ISQED) 2020, pp. 141-148, Mar. 25-26, 2020, Santa Clara, CA;
- “*Threshold Logic in a Flash*,” Wagle, Singh, Yang, Khatri, Vrudhula. 37th IEEE International Conference on Computer Design (ICCD), 2019, pp. 550-558, Nov. 17-20, 2019, Abu Dhabi, UAE;
- “*Fast, Ring-based Design of 3D Stacked DRAM*,” IEEE Transactions on Very Large Scale Integrated Circuits (TVLSI), IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 27, no. 8, pp. 1731-1741, Aug. 2019;
- “*Fast, Ring-Based Design of 3D Stacked DRAM*,” IEEE International Conference on Computer Design 2017, pp. 665-672;
- “*Selective Forward Body Bias for High Speed and Low Power SRAMs*,” Journal of Low Power Electronics, vol. 5, no. 2, pp. 185-195, Aug. 2009;

- *“Low Power and High Performance SRAM Design using Bank-based Selective Forward Body Bias,”* IEEE/ACM Great Lakes Symposium on VLSI, pp. 441-444, May 10-12, 2009, Boston, MA;
- *“Modeling Dynamic Stability of SRAMs in the Presence of Single Event Upsets (SEUs),”* IEEE International Symposium on Circuits and Systems, pp. 1788-1791, May 18-21, 2008, Seattle, WA;
- *“Design of a Flash-based Circuit for Multi-valued Logic,”* Proceedings of the Great Lakes Symposium on VLSI (GLSVLSI) 2017, pp. 41-46, May 10-12, 2017, Banff, Canada;
- *“SAT-Based Optimization for Flash-Based Digital Designs,”* IEEE/ACM Design Automation Conference (DAC), June 18-22, 2017, Austin, TX;
- *“A Flash-based Digital Circuit Design Flow,”* IEEE/ACM International Conference on Computer-Aided Design (ICCAD) 2016, Nov. 2016, Austin, TX;
- *“Implementing low power digital circuits using flash devices,”* 2016 IEEE 34th International Conference on Computer Design (ICCD), pp. 109-116, Oct. 3-5, 2016, Phoenix, AZ;

- “*Exploring Flash Devices to Implement Digital Circuits*,” IEEE/ACM Design Automation Conference (DAC), June 2016, Austin, TX;
- “*FTCAM: An Area-efficient Flash-based Ternary CAM Design*,” IEEE Transactions on Computers, vol. 65, no. 8, pp. 2642-2658, Aug. 2016;
- “*An Area-efficient Ternary CAM Design Using Floating Gate Transistors*,” IEEE International Conference on Computer Design, pp. 55-60, Oct. 19-22, 2014, Seoul, S. Kor.;
- “*A Fast Ternary CAM Design for IP Networking Applications*,” International Conference on Computer Communications and Networks, pp. 434-439, Oct. 22, 2003, Dallas, TX (awarded best paper); and
- U.S. Patent 05448182: “*Driver Circuit with Self-adjusting Impedance Matching*,” Countryman, Khatri, issued September 1995.

16. In addition to my work on the papers listed above, I have also served as an editor for IEEE Transactions on Computers, ACM Transactions on Design Automation of Electronic Systems, and MDPI Journal of Electronics.

17. I have served as EDA Track Co-Chair for ICECS 2014, Panel

Chair for TexasWISE 2014, Track Co-Chair (VLSI Systems, Applications and Computer Aided Design track) for ICECS 2013, Poster Session Chair for TexasWISE 2013, Advisory Committee for HotPI 2013, Panel Session Chair for SLiP 2013, Track Chair (Logic track) for ICCAD 2009-10, 2015-17, Track Chair (logic track) for DAC 2016-17, General Chair for IWLS 2009, Technical Program Chair for IWLS 2008, Track Co-Chair, Computer Aided Network Design (CANDE) Track, for ISCAS 2008-10, Track Co-Chair, Test and Methodologies Track, for ICCD 2007, Panel Chair for ITSW 2009, Publicity Co-Chair for GLS-VLSI 2009, and as a member of the TPC for several conferences.

II. Summary Of Materials Reviewed And Considered

18. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, while drawing on my experience in the field of semiconductor circuit design, I reviewed the Petition and all exhibits attached thereto that are cited herein.

19. In support of my opinions, I also reviewed the Transcript of the Deposition of Daniel Foty, Ph.D., taken August 6, 2025, *Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.*, IPR2025-00118 (P.T.A.B.), which I understand is being attached as Exhibit 2011 (“Foty

Dep.”). I also reviewed Exhibits 2012, 2013, 2014, and 2015. Exhibit 2012 is a true and correct copy of excerpts from *Interconnect Technology and Design for Gigascale Integration* (Jeffrey A. Davis & James D. Meindl eds., 2003) (“Davis”). Exhibit 2013 is a true and correct copy of Aishwarya Dubey, *P/G Pad Placement Optimization: Problem Formulation for Best IR Drop*, Proc. of the Sixth Int’l Symp. on Quality Elec. Design (ISQED), San Jose, CA, pp. 340-345 (Mar. 21-23, 2005) (“Dubey”). Exhibit 2014 is a true and correct copy of Howard Johnson, *Chip-Scale Transmission Lines*, High-Speed Digit. Design Online Newsl. (Signal Consulting, Inc.) (2003), https://www.sigcon.com/Pubs/news/7_01.htm (“Signal Consulting”). Exhibit 2015 is a true and correct copy of Kian Haghdad & Mohab Anis, *Power Supply Pads Assignment for Maximum Timing Yield*, 58 IEEE Transactions Circ. Sys. 697 (2011) (“Haghdad”).

20. My opinions are additionally guided by my appreciation of how a person of ordinary skill in the art would have understood the claims of the ’164 Patent at the time of the invention, which I have been asked to assume is November 1, 2018.

III. Understanding of Legal Standards

21. I am not an attorney, and in this Declaration, I do not opine on matters of law. For the purposes of this Declaration, I have been informed about

certain aspects of the law that are relevant to my analysis and opinions. My understanding of these principles is set forth below.

22. I have been informed by Counsel that the validity analysis is a two-step process. First, the patent claims are construed to ascertain their proper scope. Second, the construed claims are compared to the identified prior art to determine if the claims are valid over the prior art.

23. I have been informed by Counsel that patent claims can be deemed invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. While such conclusions are often based on more than one piece of prior art, only one is required. It is not sufficient that a collection of prior art references merely recites the various elements of a challenged patent claim. Rather, as I have been informed by Counsel, there must have been a motivation or reason to combine the prior art in a manner that renders the whole invention, including the claimed arrangement or use of the various elements, obvious. I have been informed by Counsel that obviousness cannot be based on the hindsight-driven combination of components selectively culled from the prior art.

24. I have been informed by Counsel that a person having ordinary

skill in the art (i.e., a POSITA), is a hypothetical person who is presumed to have known the relevant art at the time the invention was made. I have been informed by Counsel that the condition “at the time the invention was made” is imposed to rule out impermissible hindsight. I also have been informed by Counsel that an expert is to analyze the prior art from the perspective of a person of ordinary skill in the art at the time the invention was made, and not simply to provide his/her own personal conclusions.

25. I also have been informed by Counsel that an obviousness determination includes several factual inquiries, including: (1) determining the scope and content of the prior art; (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the pertinent art; and (4) taking into consideration any objective indicia of nonobviousness.

26. I have been informed by Counsel that obviousness must be determined as of the date of the invention (i.e., the effective filing date or priority date of the patent, which in this case is November 1, 2018). In considering the reason or motivation to combine references, it is essential to avoid using hindsight. For example, the problem examined when considering obviousness is the general problem that confronted the inventor before the invention was made, not the specific problem solved by the invention. Defining

the problem in terms of its solution leads to improper hindsight in the selection of the prior art relevant to obviousness. Further, an overly narrow statement of the problem can represent a form of hindsight, because often the inventive contribution lies in defining the problem in a new revelatory way. Similarly, a conclusory assertion that a person of ordinary skill could combine the references, rather than a showing that they would have been motivated to do so, is an impermissible form of hindsight. Moreover, the knowledge of a problem and the motivation to solve it are entirely different from motivation to combine particular references to reach the particular claimed invention.

27. I have been informed by Counsel that obviousness can be established where a skilled artisan merely pursues known options from a finite number of identified, predictable solutions. I have been further informed by Counsel that evidence of obviousness, especially when that evidence is proffered in support of an “obvious-to-try” theory, is insufficient unless it indicates that the possible options skilled artisans would have encountered were finite, small, or easily traversed, and that a POSITA would have had a reason to select the route that produced the claimed invention.

28. I have been informed by Counsel that a motivation to solve a problem (or issue) is not the same as a motivation to have combined references.

29. I have been informed by Counsel that the analysis of the

motivation to combine should be explicit. Additionally, it must include articulated reasoning with rational underpinnings to support the conclusion of obviousness. Providing a full explanation of the motivation to combine the references and the reasonable expectation of success is a necessary component of the obviousness inquiry, as inventions in most, if not all, instances rely upon building blocks long since known, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. However, conclusory statements fail to adequately explain why a person of ordinary skill would have a motivation to combine the potential prior art references.

30. I have been informed by Counsel that common sense, common wisdom, and common knowledge may be used to support a motivation to combine, so long as the use of common sense in the analysis is explained with sufficient reasoning. But, common sense can only be used to supply a limitation missing from the prior art where the technology is unusually simple and straightforward.

31. I also have been informed by Counsel that evidence suggesting reasons to combine cannot be viewed apart from evidence suggesting reasons not to combine. In analyzing motivation, both advantages and disadvantages must be considered. Teaching away, for example, is a statement in the prior art that either (i) discourages one from following the path of the claimed invention,

or (ii) encourages one to follow a path that diverges from the path of the claimed invention. The concept of teaching away bears directly on whether there was a reason to combine prior art.

IV. Level of Ordinary Skill in the Art

32. Dr. Foty defines a person of ordinary skill in the art (“POSITA”) as a person having “a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience with the design, layout, and manufacture of integrated circuits containing ESD circuitry and buses. A Master’s or Ph.D. degree in a relevant field may substitute for some work experience and vice versa.” Ex.1003 ¶ 32.

33. For the purposes of this declaration, I have not been asked to provide an opinion on the level of ordinary skill in the art, or to opine on Dr. Foty’s definition on this issue. In view of my educational background and work experience, I surpass Dr. Foty’s definition of a POSITA and did so at the time of the claimed inventions. Using Dr. Foty’s definition of a POSITA, the Petition does not show the challenged claims obvious. I reserve the right to opine as to an alternative level of a POSITA in other proceedings, and to amend my opinions if the Board provides an alternate definition of level of ordinary skill in the art.

V. The '164 Patent

34. The '164 Patent discloses “an integrated circuit electrostatic discharge bus structure and related method.” '164 Patent 1:17-20. In the prior art, an integrated circuit electrostatic discharge or “ESD” structure comprises a “circuit area 10,” “I/O (input/output) pads 12,” and an “electrostatic discharge (ESD) bus 11” as shown in Figure 1. *Id.* 1:24-37. But it was “commonly [known] to place filler cells F1 and F2 at empty spaces between the I/O pads 12, and connect the filler cells F1 and F2 to an electrostatic discharge (ESD) bus 11.” *Id.* 1:30-37. The ESD bus is a “layout trace connected to a ground or a system voltage.” *Id.*

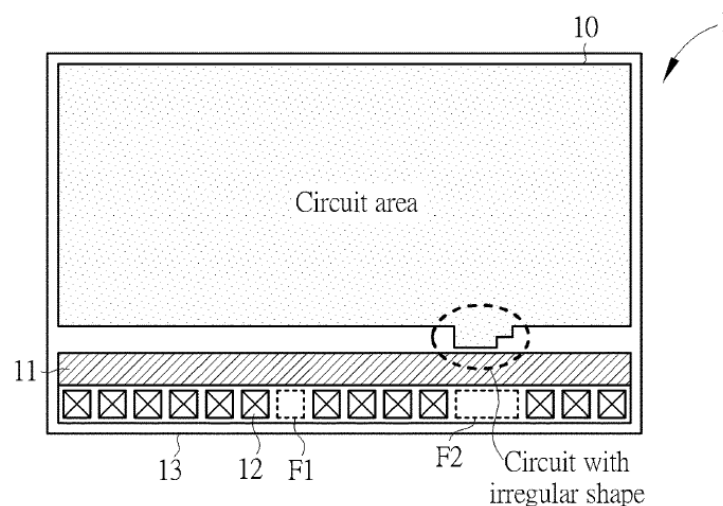


FIG. 1 PRIOR ART

35. A drawback of the prior art approach is that “filler cells F1 and F2 take a portion of the circuit area 10 to be wasteful to the integrated ESD bus structure 1.” '164 Patent 1:38-43. Further, as shown in Figure 1, “when there

are circuits with irregular shapes and different areas, the circuit area 10 must be increased in order to contain the circuits with irregular shapes and different areas, which increases production cost.” *Id.* 1:44-47. The '164 Patent teaches two configurations for overcoming the drawbacks of the prior art.

36. As shown in Figure 2, the '164 Patent teaches one configuration where a “plurality of pad groups G1, G2 and G3 is formed inside the chip edges 23, adjacent and connected to the plurality of ESD buses E1, E2, and E3.” '164 Patent 2:61-63. A “common ESD bus 24 is formed outside the chip edges 23.” *Id.* 2:63-65. Each of the “plurality of pad groups G1, G2 and G3 includes at least one pad 22” that is “connected to a ground or a system low voltage.” *Id.* 3:6-9. Bonding wires 25 connect “pads 22 of the pad groups G1, G2 and G3 to the common ESD bus.” *Id.* 3:17-22.

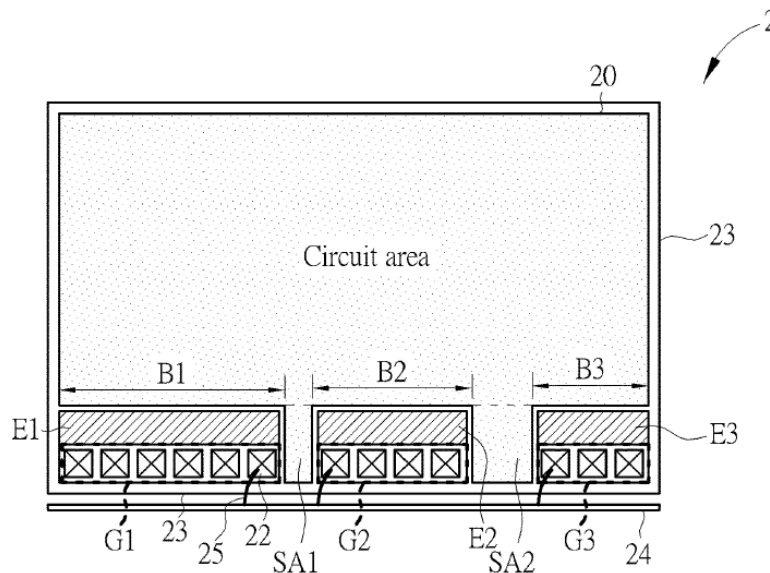


FIG. 2

37. As a result, “the discontinuous ESD buses E1, E2 and E3 may be connected together by connecting pads 22 of the pad groups G1, G2 and G3 to the common ESD bus 24 through bonding wires¹ 25.” ’164 Patent 3:17-22. In this way, “spaces between the discontinuous ESD buses E1 and E2 (or, E2 and E3) may be configured with circuit elements to make full use of the integrated circuit ESD bus structure 2.” *Id.* 3:23-26. The ’164 Patent refers to those “spaces” as “saved areas SA1 and SA2.” *Id.* 3:29-32.

38. As shown in Figure 3, an alternative embodiment also includes “circuit area 30,” a “plurality of ESD buses E1, E2 and E3,” a “plurality of pad groups G1, G2 and G3,” and “a plurality of bonding wire 35.” ’164 Patent 3:36-41. Unlike the Figure 2 embodiment where the “bonding wires 25” connect pads 22 to a “common ESD bus,” the “bonding wires 35” of the Figure 3 embodiment connect “pads 32 of one group to another group.” *Id.* 3:64-65. This also results in the “saved areas” for adding additional circuitry.

¹ For purposes of the declaration, I use the terms “bonding wire” and “bond wire” interchangeably, just like Dr. Foty. *See, e.g.*, Ex.1003 ¶ 194 (example of using “bond wire” to refer to “bonding wire”).

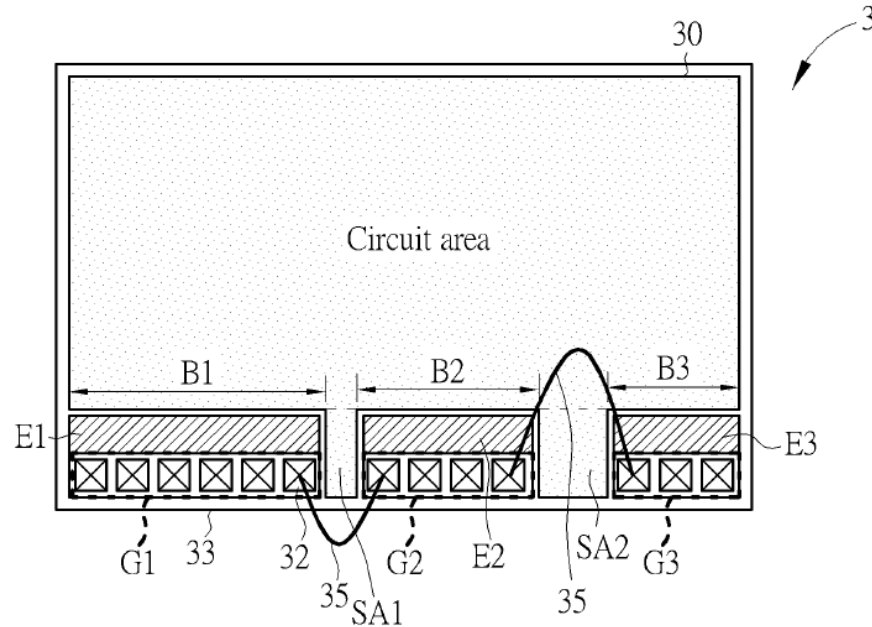


FIG. 3

VI. Claim Construction

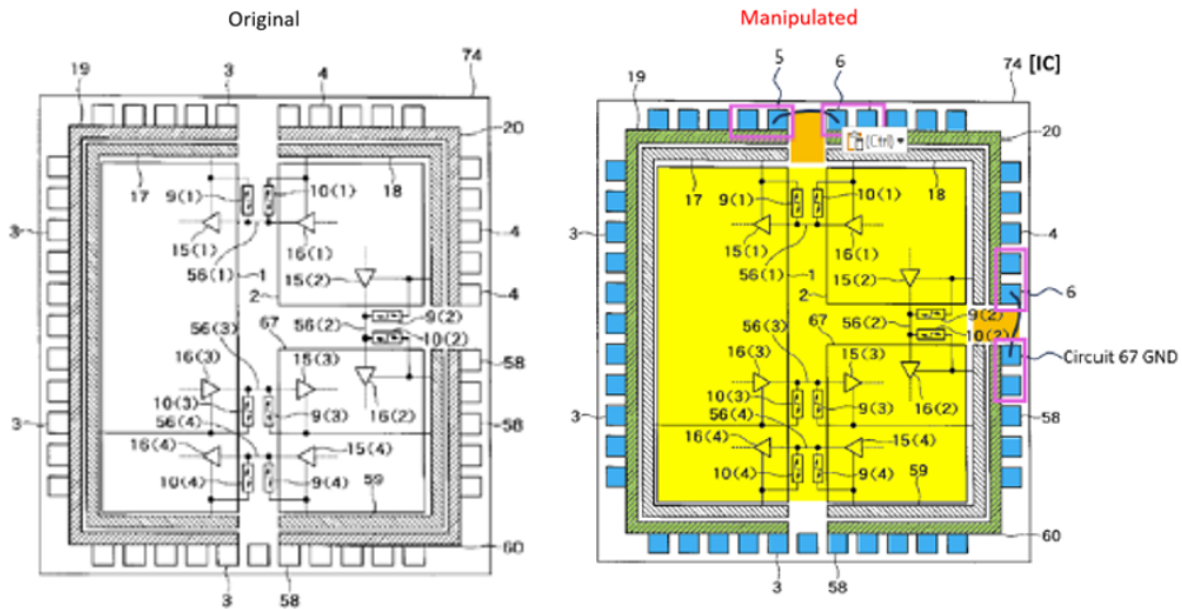
39. Dr. Foty asserts that the terms of the '164 Patent's claims have their plain and ordinary meaning. Ex.1003 ¶ 71. I have applied such a meaning for purposes of this IPR. I reserve the right to propose alternative constructions in other proceedings, or to amend my opinions if the Board provides an alternate claim construction.

VII. Ground 1

- A. Ground 1: Yoshinaga, Saint, and POSITA Knowledge Do Not Render Obvious “a plurality of pad groups, adjacent and connected to the plurality of ESD buses” (claims 6-7) or “wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses” (claims 12 and 14)**

40. Petitioner and Dr. Foty modify Yoshinaga Figure 6 by replacing a supply pad 3, an unlabeled pad, a supply pad 4, and a supply pad 58, with a

reference potential pad 5, 6, 6 and Circuit 67 GND respectively. Pet. 31; Ex.1003 ¶¶ 136-139, 144-153. They also remove a supply pad 4 (shown in the top right circuit block). Their justification for such modifications is that a “POSITA would also have understood the pads labelled 3, 4, and 58 could just as readily be used as reference pads.” Pet. 31; Ex.1003 ¶ 137. I have shown Yoshinaga’s Figure 6 alongside Dr. Foty’s modifications below. I disagree that a POSITA would have been motivated to make these modifications.



Ex.1003 ¶ 153.

41. Yoshinaga Figure 6 does not show reference potential pads. Yoshinaga, [0078]. Instead, Dr. Foty argues that “[a]s it relates to the reference pads (such as pads 5 and 6 in Figures 1-4), a POSITA would have understood that those pads are connected to ground rails 19, 20, and 60.” Ex.1003 ¶ 137.

But Figures 1-4 of Yoshinaga are block diagrams and are thus topological depictions that do not disclose the physical locations of the reference pads.

Yoshinaga, [0087]. Dr. Foty confirmed as much at his deposition about Figure 1.

Q. So Yoshinaga Figure 1 is silent about whether 5 and 6 are adjacent to ESD buses?

A. It's silent by design because it's simply -- as I said, it's simply a topological depiction. **It has nothing to do with any physical location of anything.**

Q. So the Figure 1 is a topological depiction that does not show whether 5 and 6 are adjacent to ESD buses?

A. By design, it doesn't. It simply does not even -- **this diagram does not even contain any information of that sort.** Figure 6 for example, actually shows where things are put in a physical design type of -- the physical design you do to actually instantiate the topological depiction into a real IC where you actually have to put things in real places and form things in real places. Foty Dep. 168:14-169:10.

42. Given that Yoshinaga Figures 1-4 does not show the physical location of the reference pads and Figure 6 does not show reference pads at all, Petitioner and Dr. Foty have failed to provide any disclosure of the reference pads in Yoshinaga as being adjacent and connected to the ESD buses.

43. Dr. Foty argues that “[t]he exemplary pad groups in Yoshinaga

Figure 6 are located adjacent to the reference potential lines 19, 20, and 60 – and Yoshinaga Figure 6 shows the reference lines in close proximity (“adjacent”) to the pad groups.” Ex.1003 ¶ 142. But he has provided no disclosure in Yoshinaga that the reference potential lines 19, 20 and 60 are located adjacent to reference potential pads, and this statement in his declaration contradicts his deposition testimony cited above. Neither Dr. Foty nor the Petitioner points to any evidence in Yoshinaga of reference potential pads being adjacent to reference potential lines. Nor do they provide any reason it would be obvious to do so.

44. Dr. Foty asserts that “the pads in Yoshinaga Figure 6 are largely fungible when it comes to their specific assigned connections – and their assigned locations among the available pads; for example, a POSITA would have understood that the pads labeled 3, 4, and 58 could just as readily be used for reference pads.” Ex.1003 ¶ 137. Based on that, Dr. Foty asserts that “reference pads (e.g., pads 5, 6, etc.) are located as shown below near the orange saved spaces.” *Id.* ¶ 138. I disagree. Even if Figure 6 is “an illustrative rendering” as Dr. Foty asserts (*id.* ¶ 136), that does not mean a POSITA would disregard that the pads deliberately and specifically labeled as “power supply

pads” (3, 4, and 58)² are *not* power supply pads as Dr. Foty suggests. Dr. Foty provides no reason why a POSITA would use pads 3, 4, 58 and a certain unlabeled pad specifically as “reference potential pads” when Yoshinaga teaches that pads labeled 3, 5 and 58 are to be used as power supply pads. Power supply pads and reference potential pads are very different. Power supply pads supply power and reference potential pads serve as the “reference” or “ground” for the circuit. Dr. Foty does not provide any reason a POSITA would have been motivated to change Yoshinaga’s layout and replace its power supply pads with reference potential pads. In fact, Yoshinaga states that the “reference potential pads” are “not shown,” which a POSITA would understand means they are not located at any of the pads locations that *are* shown.

45. I also disagree that “pads ... are largely fungible.” The precise location of pads in an integrated circuit has a tremendous impact on inductive and capacitive parasitics, and several design performance metrics such as noise, power consumption and delay. Replacing the “power supply pad[s]” 3, 4, and 58 by “reference potential pads” 5, 6, and “Circuit 67 GND” is an exercise that

² A POSITA would not disregard that certain pads are deliberately labeled by Yoshinaga as power supply pads, particularly when Yoshinaga does not label any other pads. *See* Yoshinaga, [0078].

could have a detrimental effect on design performance metrics. Furthermore, Dr. Foty does not discuss where the replaced power supply pads 3, 4 and 58 are moved to, a decision which would impact design metrics.

46. A POSITA would have understood that Dr. Foty's replacement of power supply pads 3, 4, 58 and an additional unlabeled pad would negatively affect the operation of the chip. Yoshinaga Figure 6 depicts 10 power supply pads, which a POSITA would have understood are each necessary to meet the power supply needs of the chip. When designing chips, a POSITA does not add unnecessary components. Thus each component shown in Yoshinaga Figure 6 would be understood to be necessary for the chip to perform its function. I understand that Dr. Foty confirmed as much at his deposition.

Q. Okay. So you wouldn't agree that adding unnecessary components could complicate a design and increase costs?

A. Well, I'd have to know what is specifically meant by unnecessary component, but **in this business, you only put on what you need.** And then you have to cope if there are issues with -- like, in a pad-limited design if you have a bunch of empty space, then you have to do something to, you know, deal with manufacturing rules. But in the business you don't generally put in more than you need, but I don't know if there are cases where people put in filler and things like that for various reasons.

Q. So in your experience, is it standard practice to add components only when they are necessary for the design's function?

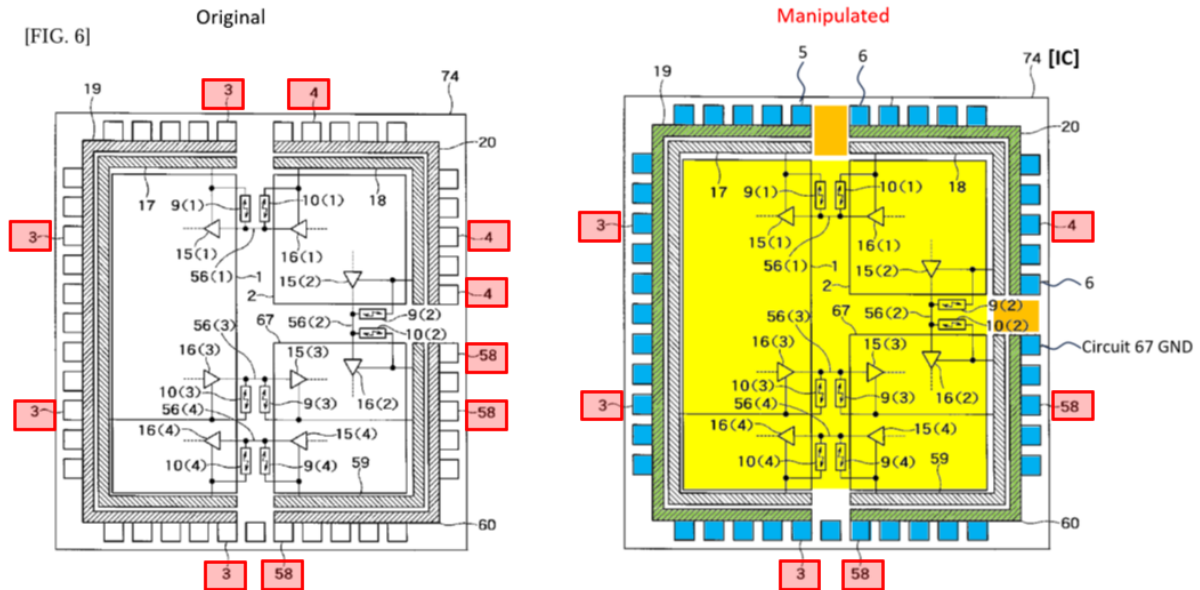
A. I think that's a fair statement. I will note that sometimes when there's space, people put little cartoons and things in. There's entire websites dedicated to the little cartoons that appear when chips are torn down. But I don't know if those are considered necessary by the designers. Maybe some do. Sarcasm alert. Foty Dep. 71:7-72:5 (objections omitted).

47. Further, a POSITA would have understood that the 10 power supply pads shown in Yoshinaga Figure 6 are placed in areas of the circuit in Yoshinaga that require more power, particularly since they are specifically labeled while reference pads are explicitly not shown (*see* Yoshinaga, [0078]). Pads are not fungible – their placement is based in part on the needs of the circuit. Different circuits have different power requirements. For power supply pads, they are placed where there is a need for power. Petitioner's reference Saint recognizes this when it states that “newer tools actually look at the drive strengths in the cells before they place their power straps” and that “in certain areas that require more power ... more power strapping” is provided. Saint, 15.³

³ Note, for purposes of this declaration, I cite the actual page numbers of Saint, on the upper left or right hand corner.

Further, Dubey teaches that the “length of the power and ground ... bond wires ... and therefore their resistance is determined by where these pads are placed on-die and therefore IR drop ... can be ... minimized by optimum pad placement.” Ex.2013 (Dubey), 2. Additionally, Dubey also states that “[bond wire] traces” are “one of the main contributors for inductive voltage drop.” *Id.*, 5. Thus, a POSITA would have understood that the power supply pads in Yoshinaga Figure 6 were placed as shown intentionally, to meet the power needs of the circuits depicted.

48. The effective result of Petitioner and Dr. Foty’s modification of Yoshinaga Figure 6 is the loss of four supply pads. Neither Dr. Foty nor the Petitioner suggest modifying Yoshinaga by replacing the power supply pads and then adding additional supply pads. As shown below (with the supply pads highlighted in red), Petitioner’s modified Yoshinaga Figure 6 (taken from Pet. 32), includes only 6 supply pads, as opposed to the 10 in the original Yoshinaga Figure 6, a reduction of 40% of power supply pads in the chip. In particular, circuit 2 in the figure below had 3 supply pads labeled 4 before Petitioner’s modification, and only 1 supply pad labeled 4 after the modification, a full 66% reduction in power supply pads.



49. The Petition only suggests replacement of the supply pads with reference potential pads. Pet. 31 (“A POSITA would also have understood the pads labelled 3, 4, and 58 could just as readily be used as reference pads.”). It says nothing about adding pads or moving pads or replacing unlabeled (possibly input, output, or inout, which I refer to as IO) pads with reference pads. Dr. Foty similarly only argues that certain pads shown in Yoshinaga 6 would be replaced, and does not say that a POSITA would replace these pads and then add additional supply pads, or where the unlabeled (possibly IO) pads would move to once they were replaced by reference pads. Dr. Foty states “the pads in Yoshinaga Figure 6 are largely fungible when it comes to their specific assigned connections – and their assigned locations **among the available pads**; for example, a POSITA would have understood that the pads labeled 3, 4, and

58 **could just as readily** be used for reference pads.” Ex.1003 ¶ 137. During his deposition, Dr. Foty confirmed, when discussing his modifications of Yoshinaga Figure 6, he “changed the power supply pad 3 into a reference pad labeled 5,” “labeled the pad immediately to the right of the orange area at the top of the chip with a 6,” “changed the label on the pad above the orange area on the right side of the chip from a 4 to a 6,” and “changed the label on the pad below the orange on the right side of the chip from 58 to circuit 67 GND.” Foty Dep. 123:2-125:12.

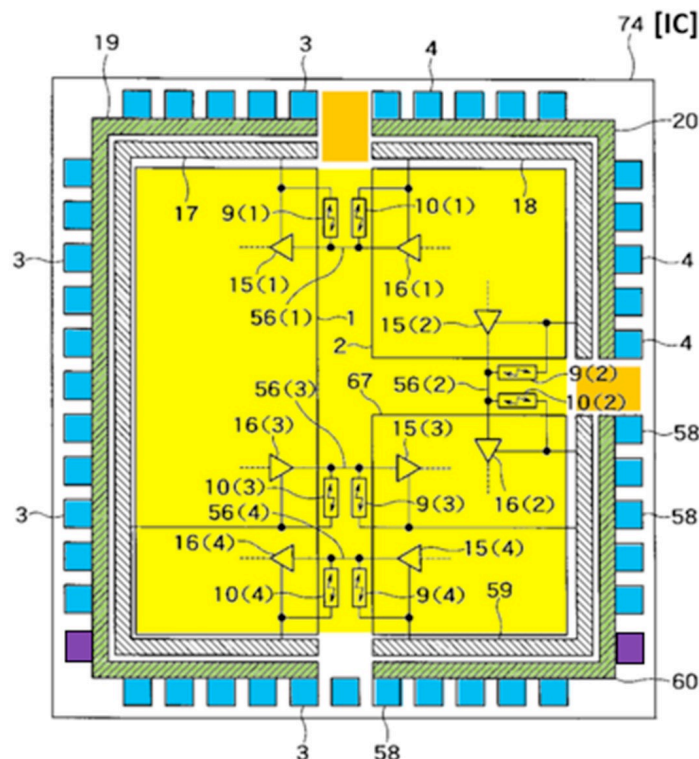
50. Each supply pad offers a resistance (R) to the power supply terminal. When a current (I) flows through the supply pad, there is a voltage drop through the supply pad, which is computed by the product IR . When there are n supply pads, the effective resistance reduces by a factor n , thereby reducing the IR drop through the pads. Therefore, reducing the number of supply pads in this manner (by 40%) would increase the IR (also called voltage) drop, which could cause the chip to run slower, or the “chip might not work at all due to hold violations.” Dubey, Abstract, 1, 5.

51. Further, the unlabeled (potentially an input, output or inout) pad that Dr. Foty proposes removing could possibly even be a critical pad such as a clock signal pad, placed specifically in its location to minimize package wiring lengths and inductive parasitics. As Saint states, long wiring “will droop or flap

around.” Saint, 195. This pad is located near the center of the top row of pads, resulting in more efficient wiring to the package. By moving this pad to an undisclosed location, the manipulated design could also result in less efficient wiring to the package for the relocated pad, and therefore increased noise on the critical signal, possibly making the manipulated design slower, or even non-functional. *See* Dubey, Abstract (observing “IR drop” caused by package wiring components). Since any wire has a certain resistance, when a current flows through a packaging wire, there would be an IR drop through the packaging wire. As a consequence, the packaging “wire length for the I/O pad ... should be minimized.” *Id.*, 5. Therefore, when this pad is moved to a different location with a longer packaging wire, there would be a greater IR drop and degraded speed, since “IR drop is ... a dominant factor in determining the chip frequency.” *Id.*, 1. Further, with the reduced number of supply pads in the modified Figure 6 compared to the original Figure 6 (I note that the modified Figure 6 has 6 supply pads, while the original Figure 6 had 10), the effective supply resistance of the circuits would increase since there are fewer pads connected in parallel to the supply, thus increasing the IR drop. This increased “on-chip IR drop” can cause “slower switching speeds” for the chip, and even make the “chip might not work at all due to hold violations.” *Id.*, 1.

52. I note that Dr. Foty also argues, for the “saved space” limitation,

that “a POSITA would know that, if required, Yoshinaga’s floorplan could be expanded to include more silicon floorspace – and thus (among other things) space for additional pads.” Ex.1003 ¶ 172. But neither Dr. Foty nor Petitioner propose modifying Yoshinaga Figure 6 to add additional supply pads to compensate for the 40% deficit in supply pads that was created by their modification. At most, Dr. Foty shows (reproduced from Ex.1003 ¶ 172), the addition of two pads (in purple below), but does not argue that these purple pads would be supply pads, that a POSITA would add such pads to Yoshinaga Figure 6, or provide a reason that a POSITA would modify Yoshinaga in such a way.



53. A result of Petitioner and Dr. Foty’s proposed modification of

Yoshinaga Figure 6 is that there will be 4 less power supply pads in the chip. That results in a 40% overall reduction. For Circuit block 1, the number of power supply pads will decrease from 4 to 3 power supply pads, resulting in a 25% reduction. For Circuit block 2, the number of power supply pads will decrease from 3 to 1 power supply pad, resulting in a 66% reduction. For Circuit block 67, there will be a reduction in power supply pads from 3 to 2 power supply pads, resulting in a 33% reduction.

54. Additionally, an unlabeled pad (located to the right of the top orange region) in the center of the top row of pads is converted to a reference pad. Petitioner or Dr. Foty do not discuss where the unlabeled pad will be relocated to. The unlabeled pad could possibly even be a critical signal pad such as a clock signal pad, placed specifically in the center of the row of pads to minimize packaging wire lengths and inductive parasitics. By moving this pad to a location at the edge of a row of pads, which results in long packaging wires, the manipulated design could also result in excessive noise on a critical signal, making the manipulated design non-functional. *See* Dubey, Abstract, 1, 5 (stating that “IR drop” is caused by package wiring components, and that as a consequence, “wire length for the I/O pad drawing maximum current should be minimized,” and “on-chip IR drop” can cause “slower switching speeds” for the chip, and even that the “chip might not work at all due to hold violations.”).

55. A POSITA would have understood Petitioner's proposed reduction in power supply pads would negatively affect the operation of Yoshinaga's Figure 6 chip and possibly render Yoshinaga inoperable. The effective reduction in power supply pads proposed by Petitioner will result in a slower chip because there are less supply pads providing power to the circuit. Having a smaller number of power supply pads than are necessary (as Petitioner and Dr. Foty propose), will also cause operating problems and potentially result in the failure of all three circuit blocks and the chip itself. Further, Petitioner's changes remove power supply pads from areas that need them, such that even if supply pads were added in other locations, they may not adequately meet the circuit's needs. Neither Dr. Foty nor the Petition address these problems.

56. Dr. Foty confirmed these consequences of having less power supply pads than are required by a circuit.

Q. What would happen if you had less power supply pads than the need for current required?

A. Well, then **the circuit might have operating problems** because the current wouldn't be able to -- the current draw wouldn't be met and you could -- for example, you could have voltage droop. The

voltage would droop because you can't maintain the voltage on the bus. Foty Dep. 151:13-20.⁴

57. In other words, Dr. Foty is admitting in his deposition that pads are not fungible. Foty Dep. 151:13-20. These power supply problems are an example of why pads are not “fungible” like Dr. Foty claims in his declaration, and why, as Saint teaches, “[y]ou cannot just blindly put your input/output pads wherever you feel like it.” Saint, 187. They also demonstrate why a POSITA would have been discouraged from manipulating the pads in Yoshinaga Figure 6 as Petitioner suggests. Indeed, changing the pad's organization as Petitioner and Dr. Foty propose would interfere with the operation of Yoshinaga's chip. A POSITA would have understood that the placement of power supply pads is not random and that pads are not fungible.

58. Even if some of the supply pads were redundant, a POSITA would still understand that removal of the supply pads from Yoshinaga without replacing them would cause power problems. That is because the pads (along with the so-called redundant pads) are placed based on local power requirements of the chip, as I discuss above. Once the pads are placed, each pad is placed in a specific spot corresponding to the power supply needs. Removing

⁴ Note that I have added emphases unless I note otherwise.

supply pads from their designated locations in Yoshinaga would result in operating problems (such as increased IR drop that could cause “slower switching speeds ... [or] ... hold violations”) to the Yoshinaga chip. *See* Dubey, 1.

59. A power pad (or reference pad) can provide only a certain amount of current (power) to the chip. Once a pad is designed, it cannot be operated in a manner that provides more power. So a POSITA could not just use fewer pads that each support a higher current to achieve the same amount of total current to the chip. For “wire-bond ... packages,” “the current that flows through the supply pad must not exceed the threshold value.” *See* Ex.2015 (Haghdad), 1, 3. This is because supply and reference pads use maximally wide on-chip wiring to connect to the internal circuitry of the chip. Thus, a POSITA would understand that they cannot use fewer pads that each support a larger current. To provide more current to the chip, one needs to provide more power supply pads. As such, the removal of supply pads (even the so-called redundant pads) without their replacement would increase the IR drop, and have detrimental effects on circuit operation. Thus a POSITA would not remove these pads (even if they were so-called “redundant”). Similarly, Saint teaches that “[y]ou can have 20 to 30 milliamps in one power supply [pad],” again indicating to the POSITA that the current provided by a single pad is limited. Saint, 88.

60. Dr. Foty suggests only that one reason for locating reference potential pads 5 and 6 “immediately next to the saved areas” as shown in his modified figure is to “preserve Yoshinaga’s saved area for other circuitry.” Ex.1003 ¶ 137. I disagree. Preserving the saved area does not require a POSITA to place reference pads where the power supply pads of Yoshinaga are located. Specifically, it does not provide any motivation for a POSITA to take Yoshinaga’s power supply pads 3, 4, and 58 (as well as an unlabeled pad) and change them into reference potential pads as proposed, nor does it explain how such a significant change would impact the performance metrics of the design. At most, preserving Yoshinaga’s alleged saved area (and I do not agree that there is a saved area) would only motivate a POSITA to not place any pads in Yoshinaga’s alleged “saved area.”

61. Petitioner’s proposal of changing an already existing pad into a reference potential pad does not by itself save space. Yoshinaga already teaches that there are pads (not reference potential pads) in the areas that Petitioner proposes modifying. So the mere replacement of those pads would do nothing to “save space.” In fact, if a POSITA were to try and save space, they would avoid making the modifications Petitioner argues because the modifications would require finding more space to add in supply pads, since Petitioner only discusses replacing 4 pads (3 supply pads labeled 3, 4 and 58, and one unlabeled

pad) with reference pads, which would require them to, at the very least, reintroduce these 4 pads in the chip so as not to reduce the number of supply pads by 40%.

62. Yoshinaga does not discuss changing pad assignments. Saint says nothing about changing pad designations to “save space” as Petitioner and Dr. Foty argue. Pet. 31-32; Ex.1003 ¶ 137. And Dr. Foty and the Petition do not point to any teaching in the prior art that suggests or motivates a POSITA to change the pad assignments in Yoshinaga Figure 6 as they propose in their modified version.

63. For the reasons I discuss above, Dr. Foty’s decision to replace the “power supply pad[s]” 3, 4, and 58 with “reference potential pads” 5, 6, and “Circuit 67 GND,” as well as the unlabeled pad to the right of the top orange region by a reference pad 6, appears to be guided by no more than hindsight, to meet the claim limitations of the ’164 Patent, rather than any actual reason a POSITA would have been motivated to make that modification, let alone with any reasonable expectation of success.

64. Dr. Foty also ignores that the Saint textbook he cites includes entire sections about how to properly place pads for “powers” and “grounds.” Saint, 143-149 (“Pin-Driven Planning”). Even for a simple change of placement of power and ground pins (shown in Figures 7-1 and 7-2, Saint states that both

are “totally valid pin-out[s],” but each “directly affects how you floorplan your chip,” since a “good choice of pin-out could reduce parasitics,” and “pin-out drives the complexity of the ... blocks.” Saint, 144-145.

65. While Dr. Foty acknowledges that “[t]he choice of selecting which pads to assign for ground [and] power ... depend[s] on factors such as the size of the chip, whether the chip is pad-limited or core-limited, the number of I/O signals, and the number of available pads.” Ex.1003 ¶ 137. This contradicts his statements just a few lines above in the same paragraph, where he says that “the pads ... are largely fungible when it comes to their specific assigned connections.” Dr. Foty’s recognition that various considerations go into choosing appropriate pads for power and ground confirm that pads are not “fungible” and that a POSITA could not simply change power supply pads into ground/reference pads. Dr. Foty does not address any of those considerations for pad selection while proposing to change Yoshinaga’s power supply pads, along with an unlabeled pad on the right of the top orange region, into ground or reference pads. A POSITA would understand that you cannot just arbitrarily make this change, without other modifications to the layout and design, and extensive simulations to quantify the effect of this change on design performance metrics such as noise, power consumption and delay. As just one example, Dr. Foty does not explain where the power supply pads 3, 4 and 58,

along with the unlabeled pad on the right of the top orange region (which he replaces) would be relocated to after he replaces them with reference potential pads 5, 6 and “Circuit 67 GND.” As I discussed in this section, Dr. Foty’s failure to add in additional power supply pads after replacing them could be fatal to the operation of the chip, and at the very least could result in “slower switching speeds.” Dubey, 1.

66. The Petitioner and Dr. Foty’s modification of Yoshinaga Figure 6 appears to be driven by hindsight. The arrangement, location and type of pads used in circuit design involve a vast number of design choices. There are almost an infinite number of permutations for arranging the pads in Yoshinaga Figure 6, with some examples of design variables including the number of pads, the types of pads, the location of each pad relative to each other and other components, the current requirements of different sections of the chip, the type of connection the pad has to other components, and how the pads interact with the rest of the circuitry in the chip. Indeed, with the 42 pad positions shown in Yoshinaga’s Figure 6, assuming the pads are fungible as Dr. Foty incorrectly argues, and with each pad being chosen from one of 5 pad types (input, output, inout, supply, reference), there would be an upper bound of 5^{42} (or 2×10^{29}) permutations just of how these pads could be arranged in a layout. A precise number of permutations of pad configurations in Yoshinaga Figure 6 cannot be

derived, since Yoshinaga does not describe details about the design variables I mentioned above. Thus, the number of design choices and options for selecting pads is very large and not easily traversed.

67. Dr. Foty at his deposition agreed that the number of design choices for a circuit are not quantifiable. He likened circuit design (which includes the selection and placement of pads) to Michaelangelo creating the David, confirming that arriving at a particular circuit design requires “numerous choices” by “a talented person.” Such a statement directly contradicts any suggestion by Petitioner or Dr. Foty that their modified Yoshinaga Figure 6 would be an obvious design choice.

Q. How many design choices would you say are made when designing a layout?

A. **I don't know if I could quantify them** because ultimately, again, it's almost like an art of who is the best artist at putting a layout together. A good -- it's like with anything, a good -- a good layout designer is almost like your maestro, a master painter who knows how to put things together in the best way. How many choices there are? I haven't thought about it that way. The designer has to make -- the layout designer has to make numerous choices based on the ground rules, and also how you're going to place blocks and things of that nature. **So many choices are made but I don't know if I could quantify it because the process just is done by a talented person to get the conclusion you need.** Foty Dep. 251:2-21.

Q. Now, would you characterize the number of design choices a layout engineer has to make in the hundreds or in the thousands?

A. **I wouldn't even care to quantify it.** It's like asking, you know, **how many choices did Michael Angelo make when he carved The David.** It's similar to that. How do you quantify that? He made many choices obviously to create a masterpiece and it's the same thing here. A good layout designer is creating a masterpiece by making many decisions. I've never thought about it in terms of numbers of them. Foty Dep. 255:5-17.

68. A POSITA cannot control everything, and an initial layout will not necessarily be successful. As Saint teaches, "changes occur" during chip design and a layout designer "can't control everything." Saint, 157. Indeed, one change of a pad can cascade into requiring additional changes to the circuit. Saint states that "what is better for one example could be a worse pin-out for a second example ... pinout drives the complexity of the cross wiring of the blocks." *Id.*, 145-146. Circuit design and layout is an iterative process. When a single pad is changed or added, it can affect other parts of the layout, requiring additional changes and extensive simulations to quantify the effect of these changes and ensure that they do not cause the chip to operate at a slower speed, or become non-functional altogether.

69. For example, Dr. Foty's changes to Yoshinaga Figure 6 involve

removing two supply pads and one other type of pad from circuit block 2. By removing supply pads, there will no longer be sufficient amount of power, and an increased IR drop, as I discussed above. So supply pads would need to be added. But if a POSITA added in added more supply pads (something Dr. Foty and the Petition never suggest), that could increase circuit size, despite Yoshinaga wanting to keep “the chip size as small as possible.” Yoshinaga, [0084]. So something else would have to change. Likewise, Petitioner proposes changing the unlabeled pad to the right of the top orange space, to a reference potential pad. That removal could snowball into another set of problems that would require additional changes to the chip, either to the pad designations themselves or to some other components. This pad could possibly even be a critical signal pad such as a clock signal pad, placed specifically in the center of the row of pads to minimize packaging wire lengths and inductive parasitics. Moving this pad to a different location would result in longer packaging wire connections, increased IR drop, and higher inductance and noise, as I have discussed earlier. Thus, going from Yoshinaga Figure 6 to Petitioner’s modified Figure 6 is not the result of a simple design choice or a predictable solution. Indeed, each change would snowball into requiring significant other changes to ultimately get the chip to work. Such changes are not predictable and the results cannot always be controlled, just as Saint states. Saint, 157.

70. Dr. Foty confirmed the iterative and complex nature of designing the floor plan of a chip.

Q. So designing a floor plan of a chip is an iterative process, you'd say?

A. **I think that's a fair characterization.** That means that you do something but then you may learn something further that something – for example, you do the layout and then you have to do what's called the LVS step. I don't know if this is mentioned in Saint, but I know this and that's where you do the layout and you run the layout through a tool which extracts, for example, the parasitic capacitances. And then you have to go back and run that through the circuit simulator and you have to see if that agrees with your original schematic. That's called layout versus schematic. And **that can be an iterative process because you may have to go back and change the circuit and then change the layout again.** So it's a **complicated process** to do that. So at some point you commit to some things and then you may have to change them later. Foty Dep. 189:17-190:15.

71. But neither Dr. Foty nor the Petition identify or analyze the factors that would lead a POSITA to modify the pads in Yoshinaga Figure 6 as they have done, why such changes would be advantageous or successful, or a problem that making these changes to the pads would solve. The lack of such information only confirms the hindsight in Petitioner and Dr. Foty's modification of pads in Yoshinaga Figure 6.

B. Ground 1: Yoshinaga, Saint, and POSITA Knowledge Do Not Render Obvious “a plurality of bonding wires configured to connect one to another of the plurality of pad groups” (claims 6 and 7) or “connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires” (claims 12 and 14)

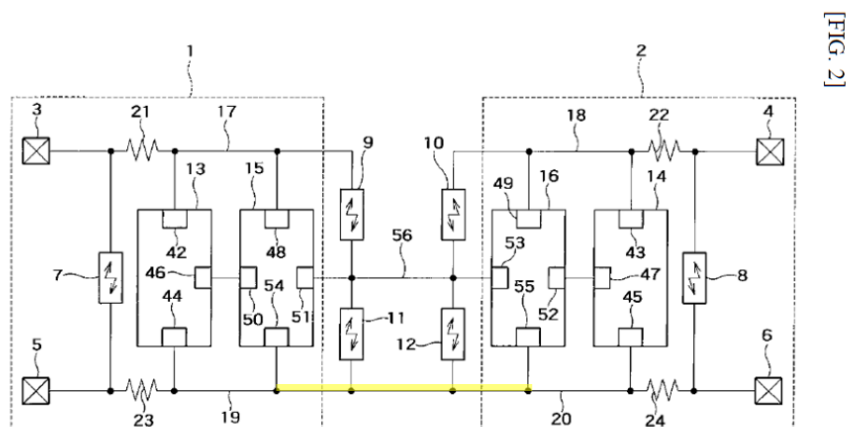
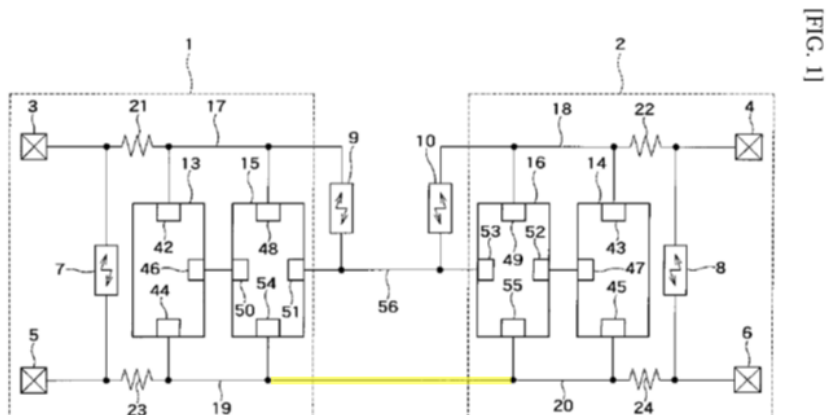
72. I also disagree with Dr. Foty’s proposed modification of using bonding wires to connect the reference potential pads as shown in his modified figure (Ex.1003 ¶ 153) as well. According to Dr. Foty, “Yoshinaga is silent on the details of how the bond pads (in Figure 6) are used and connected.” Ex.1003 ¶ 103. Based on that, Dr. Foty asserts that “it would have been obvious to a POSITA to connect together the disparate ESD buses of Yoshinaga by using the POSITA’s knowledge as reflected in Miller, Beauchamp, and others – that is, by using a ‘jumper’ bond wire to connect a pad of one pad group to a pad of another pad group, across the space that intervenes between them.” *Id.* ¶ 153.

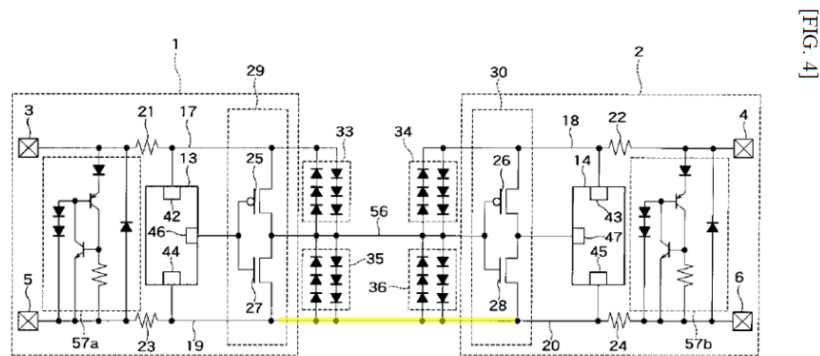
73. Dr. Foty overlooks that Yoshinaga expressly discloses that “[t]he reference potential lines *may be connected by bidirectional diodes* that are connected in parallel to one another in the opposite direction *to avoid noise*.” Yoshinaga, [0005] (emphasis added). A POSITA would know that using bidirectional diodes between reference potential pads would reduce the injection of noise from one circuit into the other, while providing ESD protection. A POSITA would also know that using “jumper” bond wires between such reference potential pads would negate the noise reduction feature

of the bidirectional diodes, and also that “jumper” wires would cause the bidirectional diodes to never conduct and therefore never provide ESD protection. Moreover, because bond wires have inductance, using bond wires would actually add noise, which is contrary to Yoshinaga’s teachings that bidirectional diodes should be used to “avoid noise.” Dr. Foty does not explain why a POSITA would disregard Yoshinaga’s disclosure of connecting the reference potential lines “by directional diodes to avoid noise” and use bond wires to connect the reference potential pads instead. He does not identify any advantages with using bond wires over bidirectional diodes or any drawbacks with the use of bidirectional diodes that bond wires would solve. From an ESD protection viewpoint, connecting reference potential pads with bond wires would be redundant given Yoshinaga’s express disclosure of using of bidirectional diodes to connect reference potential lines, as well as its discussion regarding “major features” of the invention being the “ESD protective elements 9 and 10.” Yoshinaga, [0084].

74. He also ignores that the disclosures in Figures 1, 2, and 4 of Yoshinaga show a short circuit connection between the reference potential lines 19 and 20 (in yellow below). Since Yoshinaga’s teaching is about a “semiconductor integrated circuit,” and does not mention packaging, or bond wires, this shorted connection would be understood by a POSITA to be through

one of the metal layers used in the manufacture of the circuit. Yoshinaga, Abstract. No figure or disclosure in Yoshinaga discusses or shows the usage of bond wires to make any connection.





75. Dr. Foty confirmed that the typical pad to pad connection is made through the top most metal layer, and thus not using bonding wire.

Q. So you mentioned that typically the pads are connected via these different metal layers; is that correct?

A. **The typical design would be the pads would be connected to the top metal layer** and then, typically, that's required because if you think of it like a sandwich, you know, the bread on the bottom and the cheese on the top of the cheeseburger are separated from each other. So you stack the things up. And so the -- as you build the IC up in layers, you would build metal 1, metal 2, metal 3 to the top metal, and then the pads go above that. And so you typically would connect the pad downward to the top metal in order to start the process of having the pad -- you know, you have a -- essentially you have a metal path down to a transistor in order to have the circuit have functionality. Foty Dep. 90:2-20

Q. All right. So we -- for this example, I want to refer to a three-metal layer, okay?

A. Three-metal layer process?

Q. Yes. Three-metal layer process. Yes.

A. Okay.

Q. So we have a three-metal layer process with metal 1, 2, and 3. Okay?

A. Correct.

Q. Okay. Metal layer 1 is the bottom layer connection; is that fair?

A. In the -- in the inner connect stack which is above the circuitry, it would be the bottom layer. And in this figure we're looking at, this metal 1 is actually the highest layer you see depicted here in this vertical stack, but then metal 2 and metal 3 would be above that.

Q. Okay. And then metal 3 would be the topmost layer, correct?

A. If it's a three-metal process, yes, it would be the topmost layer.

Q. **And metal 3 would be what connects the different pads;** is that right?

A. That would be -- **That would be the typical implementation scenario.** *Id.* 91:13-92:18 (objections omitted).

76. He also confirmed that there is a wire that connects the two nodes and that wire would be made of “the integrated circuit metallization in some way, shape or form.” Integrated circuit metallization involves the metal used for manufacturing the circuit, not a bond wire.

Q. Okay. So what do the two dots mean in these -- what do all the different dots mean on this diagram in Figure 1?

A. What do you mean by "dot"? Do you mean at the -- where there's a -- there's a node of wires connecting together?

Q. I mean, if you look at 17, there's a dot, then a line, then a dot. What do the dots mean?

A. The dots mean those are a node where essentially two wires connect together. Foty Dep. 163:12-22.

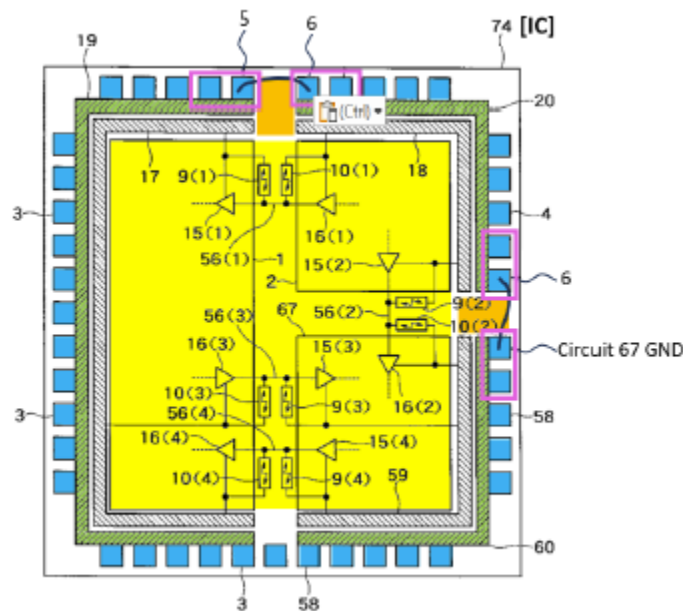
Q. Okay. So are the wires depicted in Figure 1, are they one of the different metal layer wires that we discussed before?

A. **They would be comprised of the integrated circuit metallization in some way, shape, or form.** Somewhere between pad 3 and any component down in the silicon would have to step all the way down through the metal layers to get from the pad down to the silicon level. And that would depend -- Yoshinaga is silent on processes and what might be used. But just generically, you would have to move from the pad down to the silicon through the metallization of the IC. And that might involve going down through vias to a lower metal layer and continuing that process. If you had 16 metals, you would have to step all the way down from the pad going to metal 16, going down to metal one which contacts something in the silicon. *Id.* 164:18-165:14.

77. In the deposition testimony cited above, Dr. Foty acknowledges

that the wires depicted in Figure 1 of Yoshinaga (which would include the wire connecting reference potential lines 19 and 20), are “comprised of the integrated circuit metallization.” In his declaration, however, he directly contradicts this when he says “... it would be obvious to a POSITA to connect together the disparate ESD buses of Yoshinaga (referring to nodes 19, 20 and 60), by using ... ‘jumper’ bond wire[s].” Ex.1003 ¶ 153.

78. While Dr. Foty cites references to show the use of bond wires was well-known, he ignores what they teach about the use of bond wires. For example, the Saint textbook he cites in this Ground would discourage POSITAs from using bond wires between pads 5 and 6 and between pad 6 and circuit 67 GND as Petitioner proposes (shown below).



79. First, Saint says nothing about using bonding wiring to connect

pads to other pads or to a common ESD bus. It only discusses using bond wires where direct integrated circuit metallization based wiring (like is shown in Yoshinaga, and acknowledged by Dr. Foty in his deposition at 164:18-165:14), is not possible, such as when connecting chip pads to external pins of the package. Saint, 188-197. None of the claims of the '164 Patent require the use of bond wires as they are used in Saint.

80. Second, Saint teaches that bond wires should only be used where there is “minimal silicon overlap” Saint, 195. According to Saint, “the bond wire could sag or droop, causing a short in the circuit” and “[s]o, you have to keep the overlap of the bond wire over the unused silicon as short as possible.” *Id.* In view of Saint’s teachings, a POSITA would be discouraged from deliberately forming the bond wire to overlap entirely with “unused silicon” (the alleged “saved areas” shown in orange) as Dr. Foty proposes.

81. Third, there are inherent contradictions with the numerous changes Dr. Foty and the Petition propose making to Figure 6 of Yoshinaga. Creating a space without a pad between two pads would increase the amount of “unused silicon” that an added bond wire would overlap with. But Saint teaches a POSITA would “keep the overlap of the bond wire over unused silicon as short as possible” because “the bond wire could sag or droop, causing a short in the circuit.” Saint, 195. Similarly, a POSITA would want to keep the bond

wire as short as possible to reduce voltage drops. Dubey, 2 (“length of the power and ground connecting bond wires ... and therefore their resistance is determined by where these pads are placed on-die and therefore IR drop on package can be reasonably minimized by optimum pad placement). As such, Petitioner’s addition of a space between pads does not keep the overlap of bond wire “as short as possible.” But if a POSITA followed Saint’s instruction to keep the length of bonding wire “as short as possible,” then it would not seek to add space between pads since that space would increase the length of bonding wire. These two goals are in contradiction; on one hand, if a POSITA creates a space, a POSITA would not want to use a bond wire because of the additional distance increasing the chance of a short circuit. On the other hand, if the POSITA want to use a bond wire, they would not want to add any space between pads, because otherwise it will short-circuit.

82. Unable to identify any teaching Yoshinaga or Saint about connecting bond pads together via bonding wire, Dr. Foty relies on a number of other references not listed in any of his Grounds. He argues a POSITA would combine this knowledge of the art of connecting pads via bond wires “with the layout embodiment (i.e., Figure 6 embodiment) of Yoshinaga– so as to connect together the separated ESD buses of Yoshinaga, which Yoshinaga teaches are electrically connected as shown in Figures 1-4.” Ex.1003 ¶ 152. But he provides

no reason a POSITA would have been motivated to do so.

83. Petitioner argues that a POSITA “would have been encouraged to use bonding wires because they ‘fuse[] the wire to the bond pad’ and result in firmly attache[ed] connection” that is “low resistance.”⁵ Pet. 50. But the connection from bonding wire is no more firmly attached than the connections already taught in Yoshinaga. And the “low resistance” connections discussed in the Petition (and in the cited Beauchamp, [0027]), is irrelevant to the obviousness of the invention claimed because the “low resistance” referred to by Beauchamp is only for the connection between “the bond pad 104 and the ball at the end of the bond wire 110,” (i.e. the contact resistance), not the sum of the bond wire resistance and the contact resistances (which is the relevant resistance in this instance). Beauchamp, [0027]. Thus, this “low resistance” that the Petitioner cites is not the pertinent resistance and thus is not an improvement or advantage over alternative connection methods.

84. The only reason Dr. Foty provides for using bond wire is it “was a commonplace and well-established technique.” Ex.1003 ¶¶ 144-154.

85. However, I understand from Counsel that the fact that a technique was commonplace and well-established does mean it would be obvious to try.

⁵ I note that Dr. Foty does not make such an argument in his declaration.

Neither the Petition nor Dr. Foty ever establish that there are only a finite, small or easily traversable number of options for connecting pads. And even if they did, they did not provide a reason a POSITA would select the specific route of using bond wires. In fact, for the reasons I discuss below, a POSITA would not select the use of bond wires when modifying Yoshinaga.

86. As I discussed above in paragraph 73, bonding wire has inductive parasitics which increase noise. When a changing current flows through an inductor, a voltage develops across the inductor, which manifests as voltage noise. The rate of change of current (di/dt), when multiplied by the inductance of the inductor (L) is the voltage (V) that develops across the inductor. In other words $V = L di/dt$. This V is an undesirable quantity, because it reduces the voltage seen at the end of the inductor in the case of a supply pad (“voltage droop,” as discussed in Foty Dep. 151:13-20) or causes noise on the reference signal of the chip (“ground bounce”). Since bond wires are highly inductive, they are particularly problematic in terms of this type of $L di/dt$ noise. Inductance can be of the form of self-inductance of a wire (denoted as L) or mutual inductance between a pair of wires (denoted as M). The voltage induced on the inductance is proportional to di/dt in both cases. This drawback of bond wires was well-known to a POSITA as of 2017. *See* Ex.2012 (Davis), 204 (“because of severe IR-drop and switching noise problems, conventional wire-

bonding technology is not a scalable concept for deep submicron technology”),
296 (“Numerous problems developed with the perimeter I/O and wire bonded
packages.”).

87. Even Miller, one of the references Petitioner relies on, recognizes inductance from using bonding wire is inevitable.

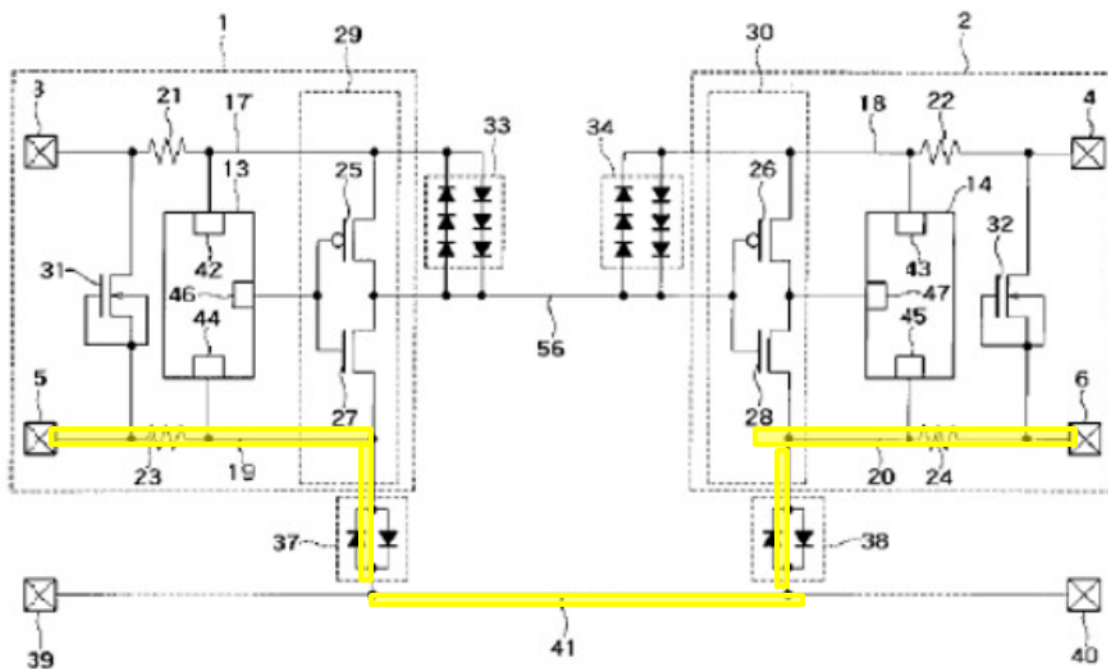
In high frequency applications a combination of series inductances and shunt capacitances in the signal path provided by the interconnect system attenuate and distort signals. **The bond wire and package leg typically contribute most of the series inductance.** The capacitance of any IC driver, receiver and/or ESD device connected to the bond pad and the capacitance of any device connected to the PCB trace (such as for example, a via) provide most of the interconnect system capacitance. The conventional approach to reducing the amount of signal distortion and attenuation caused by the interconnect system has been to minimize the series inductance and shunt capacitance of the interconnect system. The inductance of bond wires and package legs can be minimized by keeping them as small as possible. Driver, receiver and ESD capacitances can be controlled to some extent by controlling shapes and dimensions of structures within the IC. The PCB trace impedance can be controlled by appropriately choosing physical characteristics of the trace such as its width and length, its spacing from ground planes and dielectric nature of the insulating material forming the circuit board. Vias, conductors passing vertically through a circuit board to interconnect PCB traces on various layers of the PCB, can be a source of

capacitance along the PCB trace. Designers avoid the use of vias in high frequency applications in order to limit the shunt capacitance of the interconnect system. When vias are unavoidable, designers typically structure them so as minimize their capacitance. Although minimizing the inductance of the bond wire and package leg, the capacitances of the trace, drivers, receivers and ESD devices can help increase the bandwidth, flatten frequency response and reduce the signal distortion, **it is not possible to completely eliminate interconnect system inductance and capacitance. Thus some level of signal distortion and attenuation is inevitable when signal frequencies are sufficiently high.** Ex.1014 (Miller), [0007].

88. The inductance and associated noise brought by use of bonding wire would lead a POSITA away from using bonding wire in Yoshinaga. As I explained in paragraph 73, Yoshinaga already teaches a connection between pads; through bidirectional diodes in a way that “avoids noise,” or by integrated circuit metallization as Dr. Foty states. Foty Dep. 164:18-165:14. Yoshinaga says “[t]he reference potential lines may be connected by bidirectional diodes that are connected in parallel to one another in the opposite direction to avoid noise.” Yoshinaga, [0005]. Both the on-chip integrated circuit metallization and diode connections taught in Yoshinaga are less inductive than bond wires. Ex.2014 (Signal Consulting, available at https://www.sigcon.com/Pubs/news/7_01.htm), 3 (stating that “[s]eries resistance, not inductance, mostly dominates on-chip interconnections”). As

such, adding bonding wire would contradict one of the goals of Yoshinaga: to avoid noise.

89. The use of bond wires would also render the bidirectional diodes taught in Yoshinaga redundant. Figure 3 shows reference potential lines 19 and 20 connected to each other through bidirectional diode pairs 37 and 38. I have annotated this connection in yellow below.



90. Further, since the reference potential pads are connected via bond wires in Petitioner's modified Figure 6, the diode pairs 37 and 38 will never turn on, such that the diodes will not activate. The result is a circuit that has increased noise due to both (1) the inactivation of diode pairs 37 and 38, the components Yoshinaga uses to "avoid noise," and (2) the addition of bond

wires, which is known to increase inductance and noise. Additionally, this modification would result in diodes becoming superfluous, and thereby altering the design contemplated by Yoshinaga, in addition to resulting in a design that had excessive unused components which Dr. Foty says designs avoid. Foty Dep. 71:7-72:5 (“in this business, you only put ... what you need”).

91. Meanwhile, adding bonding wire to Figures 1-2 and 4 would be redundant, since there is already a metal connection between the reference potential lines, as Dr. Foty agrees. Foty Dep 164:18-165:14 (“[the wires depicted in Figure 1] would be comprised of the integrated circuit metallization in some way, shape, or form”). Accordingly, there is no advantage to connecting the pads or reference potential lines through bonding wire as opposed to through “integrated circuit metallization” (metal layers of the circuit).

92. Since bonding wires would be redundant with Yoshinaga’s teachings (for any of the connections shown in Yoshinaga, Figures 1-4), adding bonding wires would add unnecessary manufacturing steps and increased complexity during the packaging step of chip manufacturing, in addition to the deleterious electrical effects I have already mentioned.

93. Another problem with connecting pads with bonding wire across “extra space” as proposed by Dr. Foty and the Petitioner, as opposed connecting

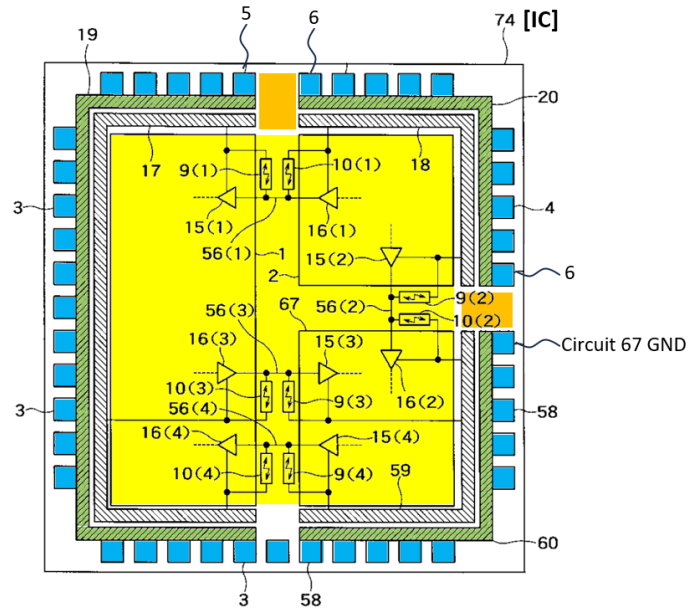
them using the method shown in Yoshinaga Figure 3 or through the “integrated circuit metallization” from Figures 1-2 and 4, is that the bonding wires are exposed to the elements, and thus are less protected than the connections already taught or shown in Yoshinaga. Saint, 187-208.

94. Further, the use of bonding wires has increased reliability issues compared to the method shown in Yoshinaga Figure 3 or through the “integrated circuit metallization” in Figures 1-2 and 4. Unlike the connection methods shown in Yoshinaga, bonding wires can cause a short circuit, since the bonding wires “could sag or droop, causing a short in the circuit.” Saint, 195.

95. As such, these facts, which were readily known to a POSITA, would discourage the POSITA from using bonding wires with Yoshinaga to make the connections Dr. Foty and Petitioner propose. Indeed, a POSITA would not have been motivated to add bonding wire to Yoshinaga’s Figure 6 nor would they have had a reasonable expectation of success in doing so.

C. Ground 1: Yoshinaga, Saint, and POSITA Knowledge Do Not Render Obvious “wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area” (claims 6-7, 12, 14)

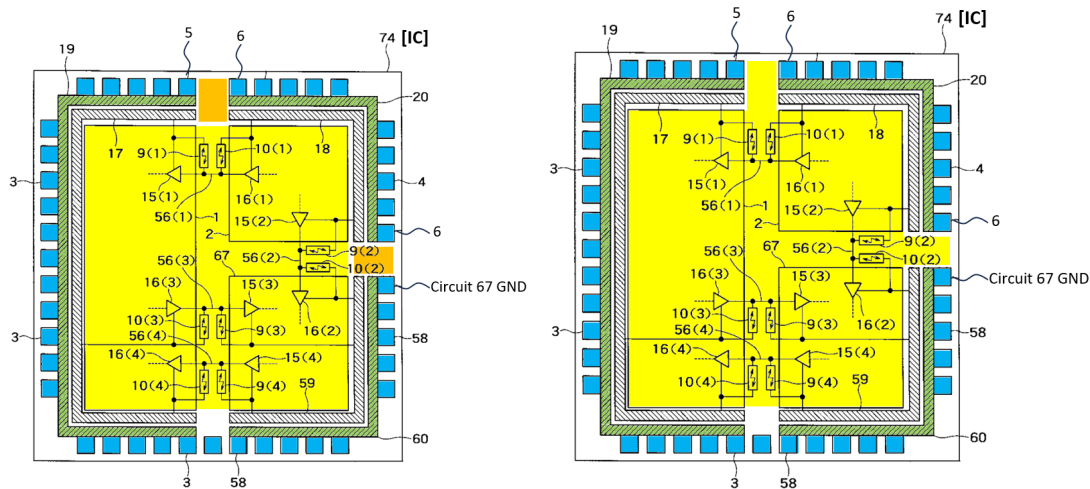
96. The Petition and Dr. Foty allege that Yoshinaga Figure 6 shows the claimed “saved area” and identify it with orange as shown below.



97. But the supposed “saved area[s]” identified by Petitioner and Dr. Foty are not disclosed by Yoshinaga to be in the “circuit area.” The Petition and Dr. Foty identify the “circuit area” in yellow and the purported “saved area[s]” in orange. Pet. 27-28, 39-41. The yellow circuit area does not include an orange “saved area.” And in its discussion of the “saved area” limitation, the Petition never alleges that the “circuit area comprises at least one saved area” in Yoshinaga nor that it would be obvious to include a circuit area with such a saved area. *Id.* 39-41.

98. At most, Dr. Foty argues that “The orange areas depicted here (in Yoshinaga’s Figure 6 embodiment, in the left-hand figure below) between the pads and power supply/reference lines disclose the ‘saved areas’ of claim sub-element [6e-1] of Claim 6. Another way to conceptualize this is shown in a

differently-annotated version of Figure 6 (on the right-hand side) – where the ‘saved areas’ are also shown in yellow, so as to indicate that they are actually part of the available ‘circuit area.’”



Ex.1003 ¶ 158.

99. But Dr. Foty’s conclusion is unsupported by Yoshinaga. Yoshinaga is silent on whether the orange area in Dr. Foty’s modified Figure 6 is part of the circuit area. There is no evidence or disclosure in Yoshinaga that this area can contain circuitry. Notably, the Petition says nothing about the claimed “saved space” being part of the “circuit area,” and only parrots Dr. Foty’s conclusion that “[t]he areas between the pads and power supply/reference lines are saved spaces (orange) where additional circuitry can be placed. Pet. 19 (citing Ex.1003 ¶¶ 157-161). But Dr. Foty’s say-so is unsupported by any disclosure in Yoshinaga. In fact, the chip in Figure 6 has three major circuits: circuit 1, circuit 2, and circuit 67 but the purported saved

area is not shown to be in any of those circuits. Yoshinaga, [0075]. And there is no description of the purported orange area being in a circuit area. As such, a POSITA would have no reason to think that the areas highlighted in orange on Yoshinaga's Figure 6 were part of the circuit area and would have understood that the orange areas in Yoshinaga's Figure 6 were likely not part of the circuit area.

100. Further, there is no evidence that the Petition's purported "saved area" has "no ESD bus and no pad" and is also "adjacent to two respective ESD buses" and "respective pads of two respective pad groups." As I discussed above in paragraph 41, Yoshinaga Figure 6 does not depict reference potential pads. Yoshinaga, [0078] (stating that "Reference potential pads are not shown"). And neither Dr. Foty nor the Petition identify any evidence that the areas they identify as a "saved space" do not include reference potential pads. Yoshinaga is silent on whether reference potential pads are in the orange spaces highlighted by Dr. Foty and the Petition. Dr. Foty confirmed as much at his deposition.

Q. So Yoshinaga doesn't say one way or another whether you could have reference potential pads in the space between power supply pads 3 and 4?

A. He's silent on that matter. Foty Dep. 145:1-5.

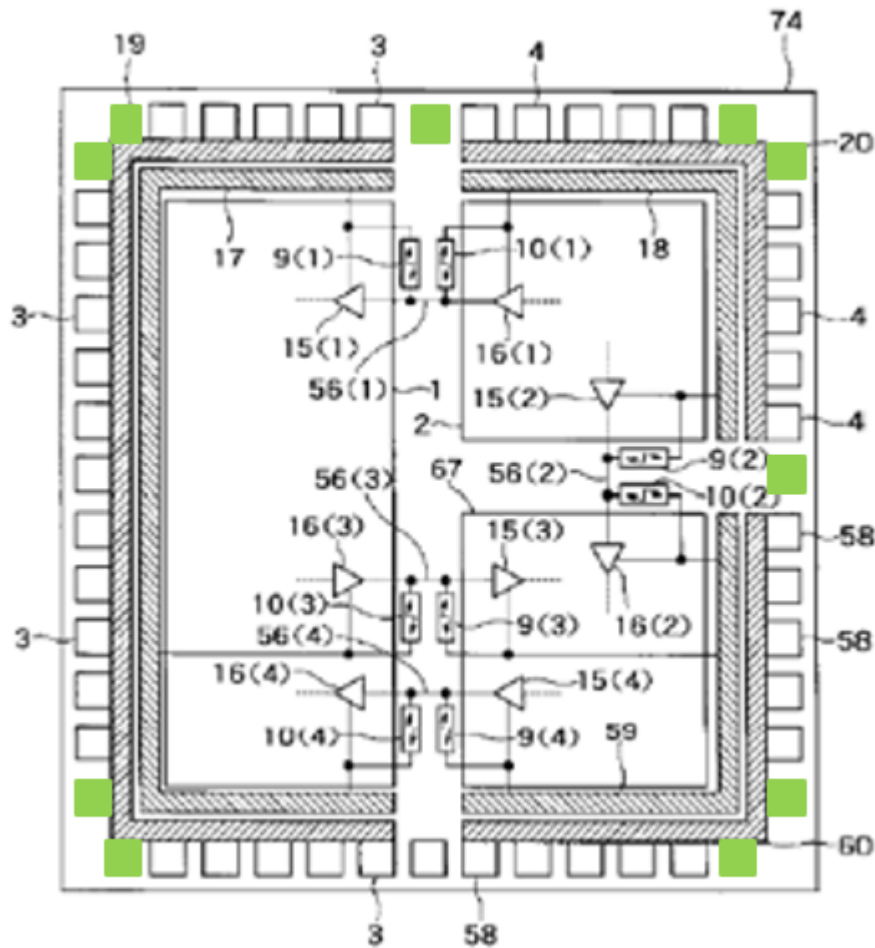
101. The pads that are shown in Figure 6 include 10 supply pads. The

remaining 32 pads are unmarked. Since Yoshinaga expressly states that the reference potential pads are not shown, that means the other 32 pads must be neither supply nor reference potential pads. Yoshinaga, [0078]. These other unmarked pads would have been understood by a POSITA to likely be IO pads.

102. Since reference potential pads are not shown in Yoshinaga Figure 6, at least one would likely be located in each of these purported “saved spaces.” Using the layout of Yoshinaga Figure 6, I can locate only 10 potential locations (shown in green below) for the reference potential pads because pads should be kept “to the outside” (as taught in Saint, 193). But as taught in Saint, a POSITA generally does not “use the corner spaces” because “with minimum pad spacing, the two pads that would neighbor the corner pad are so close to each other that we have no room to run a wire between them to a corner pad.” *Id.*, 198.

103. A POSITA would have understood that each of the 10 green spaces could be occupied by reference potential pads. A POSITA would also understand that the green spaces that are at the center of their respective rows or columns of pads would be preferred choices for reference potential pads, since they would require shorter wiring. Therefore, the first and second choices of reference potential pads would be the center pad (shown as a gap) on the top row and right column of Yoshinaga’s Figure 6. As a result, unlike what Dr. Foty

and the Petition claim, it is unlikely a “saved area” exists in view of the Figure 6 disclosure. This is especially true given Figure 6 is organized to “greatly improve the ESD resistance while keeping the chip size as small as possible,” which would require placing the reference potential pads in these purported “saved areas.” Yoshinaga, [0084].



104. Figures 1-4 similarly do not teach that there is a saved space as claimed in the orange spaces marked by Petitioner and Dr. Foty. Instead, Figures 1-4 are topological or schematic depictions and thus do not show the

relative physical locations of the pads to each other. As such, they do not show a saved area. Dr. Foty confirmed as much.

Q. Okay. In Figure 1, are 5 and 6 adjacent to ESD buses?

A. Saint is silent on that level of detail. This is a -- at least Figure 1, this is what **I earlier call a topological depiction**, not a physical depiction. So all he's showing here is the -- what's there and how they're topologically connected together. What are the components, what components are wired to each other. It's a purely topological description.

Q. So Yoshinaga Figure 1 is silent about whether 5 and 6 are adjacent to ESD buses?

A. It's silent by design because it's simply -- as I said, it's simply a topological depiction. **It has nothing to do with any physical location of anything.**

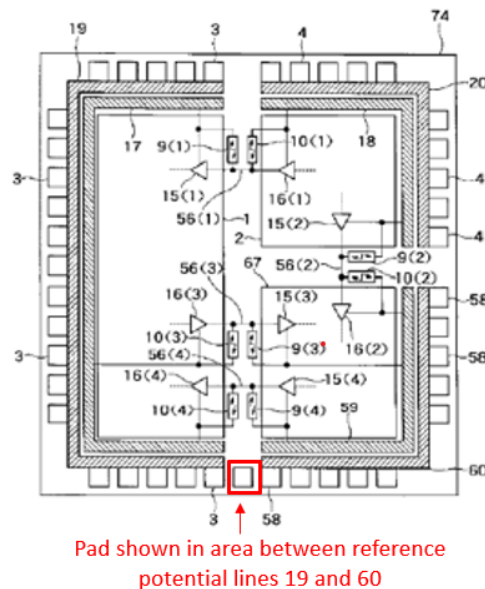
Q. So the Figure 1 is a topological depiction that does not show whether 5 and 6 are adjacent to ESD buses?

A. By design, it doesn't. It simply does not even -- this diagram does not even contain any information of that sort. Figure 6 for example, actually shows where things are put in a physical design type of -- the physical design you do to actually instantiate the topological depiction into a real IC where you actually have to put things in real places and form things in real places.

Q. In Figure 1, is there a saved area as discussed in the claims of '164 patent?

A. Well, again, **this is a topological depiction so it has no physical information at all in this figure and you would not expect to have any here.** It's a stick diagram, a topological depiction. Foty Dep. 168:4-169:17 (objections omitted).

105. As shown in Yoshinaga Figure 6, the existence of a space between circuits or reference potential lines does not mean no pad is present. As I have highlighted below in red, Yoshinaga shows a pad (one that is not a reference potential pad) between circuits and potential lines.



106. For these reasons, not only does Yoshinaga not teach a “saved area” with no pad, it also suggests that the orange areas marked by Petitioner includes pads. Indeed, a POSITA would have understood that the most likely place for such reference pads are Petitioner’s purported “saved areas.”

107. Dr. Foty argues that the availability “of some additional ‘saved

area(s) could be put to different uses depending on the needs of the particular IC” and that adding a “saved space” “would reduce size of the die – and thus, by increasing the number of dies per wafer, reduce the cost per die.” Ex.1003 ¶ 161 n.12. That is incorrect. The chip in Yoshinaga is described as being “as small as possible” Yoshinaga, [0084] and thus a POSITA would understand that there is no empty space to utilize between pads. This understanding would be further supported by the fact that Yoshinaga teaches that the “[r]eference potential pads are not shown.” Yoshinaga, [0078]. So to add a “saved space” to Yoshinaga would require expanding the size of the chip, antithetical to the goals of Yoshinaga, which would make the circuit bigger and more costly.

108. Saint also does not teach, suggest or motivate a POSITA to create “saved spaces” as claimed in the '164 Patent. In fact, it teaches the opposite. Saint encourages one to “try[] to get the chip as small as possible.” Saint, 207. But creating a space where there is no pad *increases* the size of the chip, which is why a POSITA would not want to modify Yoshinaga to add such a space. In fact, Saint calls spaces between pads “wasted space.” *Id.*, 206. It does not encourage a POSITA to make such spaces, let alone to create a saved space as claimed by the '164 Patent with no pads or ESD buses that is also adjacent to ESD buses and pads. Rather it says to avoid “wasted space around the edges between the pads ... you can push some of your circuitry into this wasted space

to try to use those gaps.” *Id.*, 206-207. No such gaps are taught in Yoshinaga Figure 6.

109. Neither Dr. Foty nor the Petition identify any reason a POSITA would be motivated to form a “saved space” that does not include a pad or ESD bus in Yoshinaga Figure 6. In fact, for the reasons I just described, a POSITA would not have been motivated to create the “saved space” claimed by the challenged claims in Yoshinaga Figure 6.

VIII. Ground II

A. **Ground 2: Yoshinaga, Saint, Haralabidis, and POSITA Knowledge Do Not Render Obvious “plurality of pad groups” “adjacent and connected to the plurality of ESD buses” (claims 1-6, 8-11, and 13)**

110. I note that Petitioner’s obviousness arguments regarding limitations [1.C] and [8.C] are identical to their arguments made for limitations [6.C] and [12.C] in Ground 1. Pet. 55, 63. As a result, Yoshinaga, Saint, Haralabidis, and POSITA knowledge do not render obvious a “plurality of pad groups” “adjacent and connected to the plurality of ESD buses” as required in claims 1-6, 8-11, and 13 for the same reasons that Ground I does not render obvious “a plurality of pad groups, adjacent and connected to the plurality of ESD buses” or “wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses.” *Supra* Section VII.A. Indeed, the addition of Haralabidis does not change my obviousness analysis, since Haralabidis is

completely silent about bond pads. Dr. Foty agreed in his deposition.

Q. But Haralabidis does not disclose bond pads?

A. Not explicitly, but something has to. Foty Dep. 243:9-11.

Q. So to be clear, none of the disclosures in Haralabidis explicitly describe bond pads?

A. He's silent on the method used to connect from the inside the IC of the package substrate. He says nothing about any particular method.

Q. Okay. Similarly, he says – Haralabidis says nothing about bond pads themselves, correct?

A. He's completely silent on that issue. I assume he doesn't regard that as part of his inventive material and that seems to be from examining Haralabidis of what's going on. *Id.* 244:4-15 (objections omitted).

B. Ground 2: Yoshinaga, Saint, Haralabidis, and POSITA Knowledge Do Not Render Obvious “a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus”, “connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires,” and “connecting” pad groups “to another of the plurality of pad groups” (claims 1-6, 8-11, and 13)

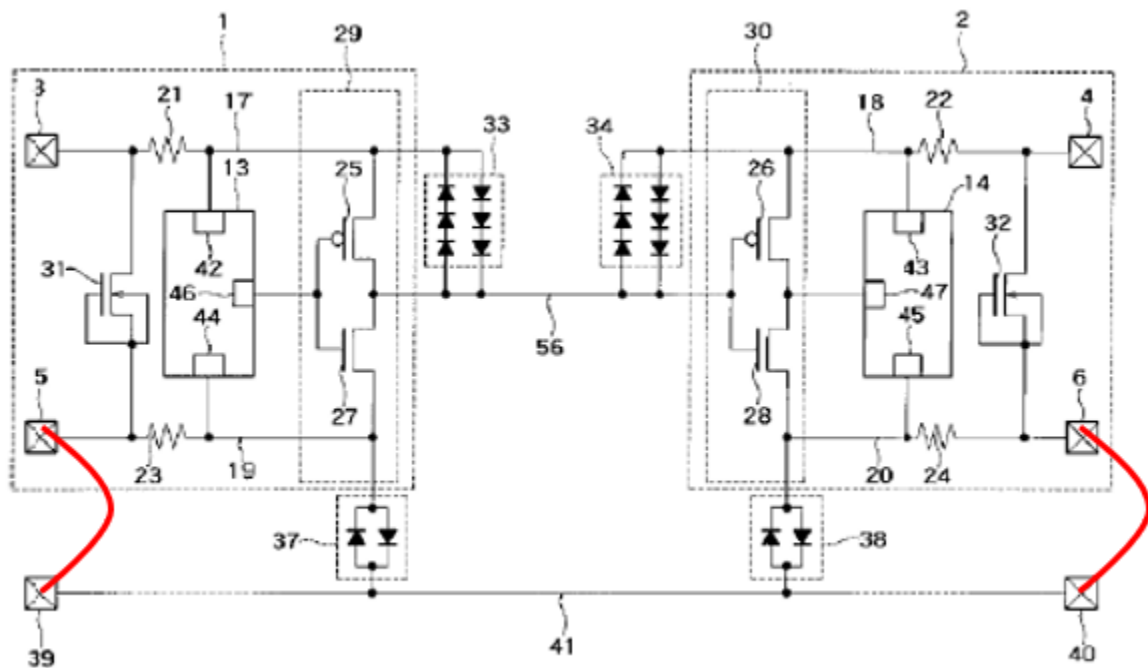
111. While admitting that “Yoshinaga discloses a common ESD bus” (Ex.1003 ¶ 235), Dr. Foty asserts that a POSITA would have been motivated to combine Haralabidis with Yoshinaga because, according to him, “notably,

Yoshinaga discloses no teachings that involve what happens beyond the bond pads; thus, a POSITA would clearly be motivated to combine Yoshinaga with a reference that provides details on connecting the IC (via its bond pads) to external lines that could be used as destinations for the shunted energy of any ESD events,” such as Haralabidis. *Id.* ¶ 224.

112. Dr. Foty again ignores that Yoshinaga states that “reference potential lines *may be connected by bidirectional diodes* that are connected in parallel to one another in the opposite direction *to avoid noise*.” Yoshinaga, [0005] (emphasis mine). Yoshinaga further discloses how to connect reference potential lines 19 and 20 to a “third reference potential line 41 ... used as a [ESD] discharge path” (such as the alleged “common ESD bus” of Haralabidis)—namely, “via a bidirectional diode pair 37 and a bidirectional diode pair 38,” as shown in Figure 3. *Id.*, [0061], Fig. 3. According to Yoshinaga, this “avoid[s] noise between the reference potential lines.” *Id.* I have discussed supra how the use of bonding wires to connect reference potential pads would actually increase noise (due to the inductance of the bonding wires as well as the direct injection of noise from one reference potential pad to the other) and also would cause the bidirectional diodes to never conduct and therefore never provide ESD protection. As a result, the inclusion of the teaching of Haralabidis contradicts and negates the teaching of

Yoshinaga.

113. Dr. Foty's proposed modification of adding "bond wires" (red) to connect reference potential pads 5 and 6 of Yoshinaga is redundant in view of Yoshinaga's teachings. Ex.1003 ¶ 254. Dr. Foty's proposed modification is shown below in the modified version of Yoshinaga's Figure 3, with the proposed bonding wires shown in red:



114. As shown, reference potential lines 19 and 20 are already connected by the bidirectional diodes (circuit elements 37 and 38) to the third reference potential line 41 which is "used as a discharge path" for ESD events. Yoshinaga, Fig. 3, [0061]. Thus, the bond wires connecting reference potential pads 5 and 6 to the "third reference potential line 41" serve no beneficial

purpose. In fact, they negatively impact both the ESD and noise performance of the design, as I have stated above. These red bond wires add additional (and unnecessary) components, parasitics (and associated noise), and complexity. Dr. Foty does not explain this at all, let alone why a POSITA would have been motivated to use bond wires as required by the patent claims.

115. In my opinion, a POSITA would not have been motivated to look to other references like Haralabidis or Saint to connect reference potential lines 19 and 20 of Yoshinaga. Dr. Foty does not provide any reason that Yoshinaga's disclosures for connecting the reference potential lines 19 and 20 to a "third reference potential line 41" are inadequate or insufficient. Nor does Dr. Foty provide any reason why a POSITA would disregard Yoshinaga's disclosures of bidirectional diodes or the integrated circuit metallization and use bond wires instead—a fundamentally different connection method with disadvantages that I have mentioned supra. Dr. Foty does not identify any advantages with using bond wires or any drawbacks such "bond wires" would solve. And, as discussed above, Dr. Foty ignores the drawbacks of using bond wires altogether.

116. Further, the teaching of Yoshinaga achieves ESD protection entirely on-chip, with "ESD protective elements 9(1) to 9(4), 10(1) to 10(4), which are ... provided in the chip interior ... [such that] the size of the ESD protective element may be small," thereby providing ESD protection "while

keeping the chip size as small as possible.” Yoshinaga, [0084]. As such, Yoshinaga already accomplishes on-chip efficient and adequate ESD protection with a very low area, and is not looking for an off-chip solution by using the teaching of Haralabidis. Dr. Foty and Petitioner simply disregard this key inventive aspect of Yoshinaga. Indeed, adding Haralabidis’ common ground rail would increase chip size (by adding additional components without removing others) as well as noise, and complexity for the reasons I have already discussed.

117. Neither Yoshinaga, Saint nor Haralabidis teach the connection of bonding pads together using bonding wires. As I explained above in paragraph 79, Saint does not describe using bonding wires to connect pads to each other or to a common ESD bus. Dr. Foty appeared to agree with this at his deposition.

Q. Okay. So would you agree with me that Saint and the microphotograph image in paragraph 147 do not teach connecting a bond pad in one group to a bond pad in another group using bond wire?

A. There’s no -- **There is no depiction in Saint** or in this figure we're looking at here, which is why that was demonstrated with other art such as Miller and Beauchamp in my declaration. Foty Dep. 107:7-19 (objections omitted).

118. Similarly, Haralabidis says nothing about connecting pads to each other using bonding wire. It is also silent about bond pads in general, as I

discussed in paragraph 110. At most, Haralabidis only shows and teaches bond wire connections of segmented ground rails to a common ground rail through bond wire connections. Ex.1007 (Haralabidis), 3:9-18, 4:13-26. It is silent on the connection of pads to each other or to a common ESD bus through bonding wire.

119. And like with Ground 1, neither the Petition nor Dr. Foty claim that use of bonding wire was one of a finite, small or easily traversable number of options for connecting pads. And even if they did, they did not provide a reason a POSITA would select the route of using bond wires. For the reasons I discussed above in Section VII.B, a POSITA would not select the use of bonding wire when modifying Yoshinaga.

C. Ground 2: Yoshinaga, Saint, Haralabidis and POSITA Knowledge Do Not Render Obvious “wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area” (claims 1-6, 8-11, and 13)

120. I note that Petitioner’s obviousness arguments regarding [1.F], [6.E], [8.F] and [12.E] in Ground 2 are identical to their arguments made for limitations [6.E] and [12.E] in Ground 1. Pet. 55, 63. As a result, Yoshinaga, Saint, Haralabidis, and POSITA knowledge do not render obvious a ““each of at least one saved area is adjacent to two respective ESD buses of the plurality

of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area” as required in claims 1-6, 8-11, and 13 for the same reasons that Ground I does not render obvious the same claim limitation. *Supra* Section VII.C. Indeed, the addition of Haralabidis does not change my obviousness analysis, since Haralabidis is completely silent about bond pads or saved areas, let alone the locations where bond pads are and are not located.

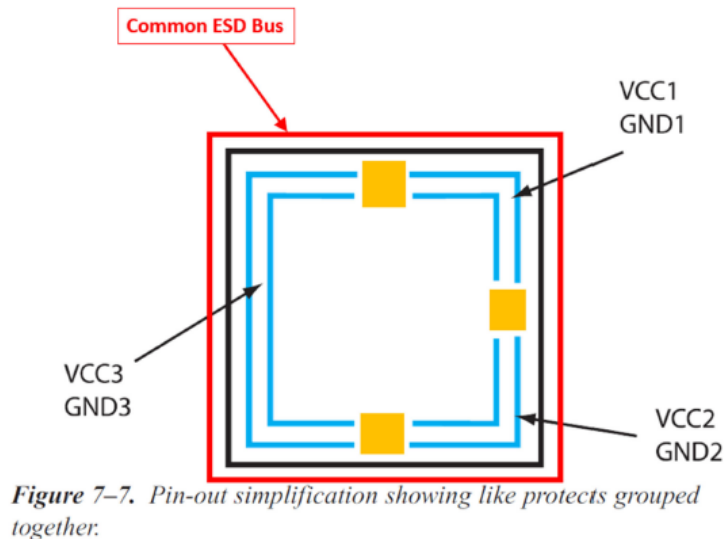
IX. Ground III

A. Ground 3: Saint, Haralabidis, and POSITA Knowledge Does Not Disclose Or Render Obvious “a common ESD bus” (claims 1-5, 8-11)

121. Dr. Foty argues that Saint and Haralabidis render obvious claims 1-14. I disagree. The independent claims of the '164 Patent require either (i) “a common ESD bus” (claims 1 and 8), or (ii) “a plurality of pad groups ... connected to the plurality of ESD buses,” wherein the “plurality of pad groups” are connected “to another” (claims 6 and 12).

122. Dr. Foty states that “it is a fairly simple exercise (and would have been a simple exercise for a POSITA) to add the common ESD bus described by Haralabidis to the Figure 7-7 presentation of Saint – and (*since they have to connect somewhere*) to connect the segmented rails of Saint’s Figure 7-7 presentation to this common ESD bus.” Ex.1003 ¶ 368 (emphasis added). Dr.

Foty's proposed modification is shown below.



123. As an initial matter, the segmented rails of Haralabidis are electrically the same terminal, since they are connected together either at the package substrate or the printed circuit board (PC Board). In contrast, the reference rails of Saint are distinct and separate electrical terminals (GND1, GND2 and GND3) and are as such not segmented reference rails. Therefore it is incorrect to refer to these as “the segmented rails of Saint’s Figure 7-7.” Ex.1003 ¶ 368.

124. Saint’s Figure 7-7 is derived from Figures 7-3, 7-4 and 7-5, which clearly show that the three reference rails GND1, GND2 and GND3 are separate and distinct electrical terminals, with separate and distinct voltages, and therefore it would be an error to connect them as Dr. Foty suggests. Saint, 145-149. As these three figures from Saint show, the rails GND1, GND2 and GND3

are separate rails, that do not correspond to the same electrical terminal, and are therefore not “segmented rails” as Dr. Foty claims. Ex.1003 ¶ 368.

125. In the Saint reference, per Figure 7-3, pins 1, 5, 7 and 9 are protected against the VCC1 supply and the GND1 reference terminal. In Figure 7-4, pins 6, 8, 10 and 14 are protected against the VCC2 supply and the GND2 reference terminal, while in Figure 7-5, pins 2, 3, 4, 11, 12, 13, 15 and 16 are protected against the VCC3 supply and the GND3 reference terminal. If these pins are connected to the alleged “common ESD bus” in Dr. Foty’s modification, all these 16 pins would be protected against a common reference terminal (the common terminal in Dr. Foty’s modification), which would result in a different electrical design than contemplated by Saint. Dr. Foty provides no analysis as to why a POSITA would make such a drastic design change. In fact, a POSITA would not make such a change.

126. Dr. Foty overlooks that a POSITA would not have been motivated to add any “common ESD bus” to Figure 7-7 of Saint because the Figure 7-7 layout discloses three separate and distinct power supply voltages and reference potentials—namely VCC1/GND1, VCC2/GND2, and VCC3/GND3. Saint, 145-148. Figure 7-7 of Saint illustrates one way to arrange a circuit so that the pins 1 through 16, that are “protected to the same supply” are moved “close together” because the chip design has three *different* VCC

and GND signals. *Id.*, 147. In other words, pins 1, 5, 7 and 9 are moved close together and protected against VCC1 and GND1, while pins 6, 8, 10 and 14 are moved close together and protected against VCC2 and GND2, and pins 2, 3, 4, 11, 12, 13, 15 and 16 are moved close together and protected against VCC3 and GND3. Saint never teaches connecting the different GND1, GND2, and GND3 signals together to a “common ground” as Dr. Foty proposes. Ex.1003 ¶ 367. In fact, a POSITA would have understood from Figure 7-3, 7-4, 7-5 and 7-7 that GND1, GND2, and GND3 are separate reference potentials that should *not* be connected together as Dr. Foty proposes.

127. Dr. Foty tries to justify his proposal to use a common ground by pointing to “Case Study 1” at the end of Saint on page 332 and arguing that Saint also contemplates the use of a “single ground rail.” Ex.1003 ¶¶ 359-360. As a preliminary matter, the case study Dr. Foty refers to starts on page 247 of Saint and walks through the design of a specific CMOS amplifier circuit. Saint does not say that the specific example of Case Study 1 can be generally applicable to all designs of Saint, let alone that it is applicable to Figure 7-7. In fact, this “single ground rail” is not applicable in general, and not applicable to Figure 7-7 in particular. Regardless, the exemplary CMOS amplifier design of Case Study 1 includes only one “GND” signal. Saint, 249, 250 and 261 (CS1-1, CS-2, CS1-10). That is why CS1-99—the figure Dr. Foty relies on that is

part of Case Study 1 (below)—shows the use of a single, “continuous ring” ESD ground wiring. *Id.*, 332. Dr. Foty himself recognizes that Figure 7-7 depicts “a design where there are three separate power supply and three separate ground lines,” while the design of Case Study 1 is “*not* using the three-ground-rails (which provide three ESD buses) configuration of the Chapter 7 design” and instead “use[s] a *single* ground rail.” Ex.1003 ¶¶ 359-360.

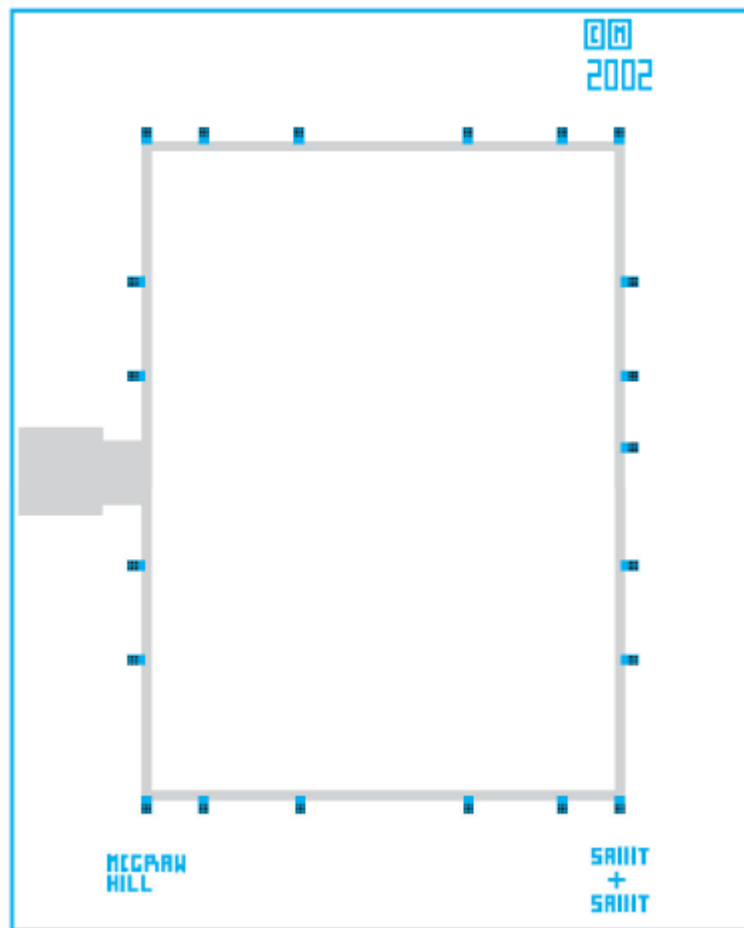


Figure CSI-99

128. Dr. Foty provides no reason that a POSITA would have been motivated by the disclosures of Saint’s Case Study 1 that relate to a single

ground signal design to modify the Figure 7-7 design to connect its three separate signals GND1, GND2, and GND3 together to a “common ESD bus,” like the one Dr. Foty points to in Haralabidis. Connecting three separate signals together to a “common ESD ground” would drastically alter the electrical characteristics of the design and require other modifications as well. Such a modification would result in noise from one circuit being injected into another, which would result in a degradation of circuit performance. Further, the use of a “common ground rail (360)” in the package substrate as taught by Haralabidis, with wire bond connections to the chip (*see* Ex.1003 ¶ 367), would result in increased inductive and resistive parasitics, resulting in degraded reference impedances and increased noise. As a result, a POSITA would be discouraged to combine the teaching of Saint with Haralabidis, as Dr. Foty proposes.

129. Similarly, Haralabidis teaches the use of a “common ground rail” to connect “segmented ground rails.” Haralabidis, 3:9-22, 3:34-40, 3:65-4:12. A POSITA would understand “segmented ground rails” to refer to a single ground signal that has been “segmented.” That is fundamentally different from the design of Saint’s Figure 7-7 that Dr. Foty relies on, which uses three *different* ground signals, GND1, GND2, and GND3—not a single ground signal that has been “segmented.” Because of that, a POSITA would not have been motivated to change the Figure 7-7 design completely to connect three separate

signals (GND1, GND2 and GND3) together as Dr. Foty proposes. Ex.1003 ¶ 368. Indeed, for these reasons, a POSITA would have understood Haralabidis' teachings of a "common ground rail" are inapplicable to Saint's Figure 7-7.

130. The Petition and Dr. Foty argues a POSITA would have been motivated "to adapt Saint's IC teachings to include Haralabidis' package common ground rail 360' (Fig. 3) to further reduce die size and costs." Pet. 97; Ex.1003 ¶¶ 321-324. That is simply not true. Even assuming that this change would not cause a drastic electrical modification, adding an external common ground rail, and not removing VCC1/GND1, VCC2/GND2, and VCC3/GND3 shown in Saint 7-7, will not reduce the size of the die. Nor will costs decrease because adding the bonding wire and common ground rail without removing the other components would be an added and unnecessary expense.

131. There is no reason a POSITA would be motivated to use the "common ground rail" connection of Haralabidis with Saint 7-7 because they serve fundamentally different purposes. Haralabidis teach an entire "electronic device" that includes a printed circuit board (PCB), where the ESD buses are outside the chip. Haralabidis, Abstract, 3:65-4:2. But Saint Figure 7-7 is a chip design that seeks to include components, such as ESD buses, inside the chip. As such, a POSITA would not look to Haralabidis when modifying Saint since

Haralabidis focuses on the components and circuitry outside, not inside, the chip.

132. The Petition states Ground 3 “relies on a set of teachings (primarily from Saint) applied to Saint’s IC in Fig. 7-7, but the results are the same if Saint’s IC in Fig. 9-21 is used as a baseline.” Pet. 68. I agree that the challenged claims are nonobvious in view of using Saint’s Figure 9-21 as a baseline for the same reasons as I list in this declaration for Saint Figure 7-7. Further, the Petition and Dr. Foty do not establish how every limitation of each claim would be taught or obvious in view of Saint Figure 9-21, and never even mentions Saint Figure 9-21 in connection with what the Petition identifies as claim limitations 1.B, 1.C, 1.D, 1.E, claim 2, claim 3, claim 4, claim 5, 6.B, 6.C, 6.D, claim 7, 8.B, 8.C, 8.D, 8.E, claim 9, claim 10, claim 11, 12.B, 12.C, 12.D, and claim 14.

B. Ground 3: Saint, Haralabidis, and POSITA Knowledge Do Not Render Obvious “connecting” the “pad groups” to either “another of the plurality of pad groups” (claims 6-7, 12-14) or “to the common ESD bus” by “bonding wires,” (claims 1-5, 8-11)

133. The independent claims of the '164 Patent require “a plurality of pad groups ... connected to the plurality of ESD buses,” wherein the “plurality of pad groups” are connected “to another” (claims 6-7 and 12-14) or “to the common ESD bus” (claims 1-5, 8-11) by “bonding wires” (claims 1-14).

134. As I discussed above, a POSITA would not be motivated to short three separate GNDs to a common ground rail as Dr. Foty and Petitioner claim. *Supra* Section IX.A.

135. Further, neither Saint nor Haralabidis teach the connection of bonding pads together or to a common ESD bus using bond wires, as I discussed above in paragraphs 117-118.

136. For the claims that require the “plurality of pad groups” connected “to another,” Dr. Foty references his discussion with respect to the “common ESD bus” claim elements and cites to Case Study 1 of Saint, without any additional analysis. Ex.1003 ¶¶ 409, 448-49. Dr. Foty’s analysis fails for the same reason I discussed above in Section IX.A—namely, a POSITA would not have been motivated to connect the “plurality of pad groups” of Dr. Foty’s proposed modification of Figure 7-7 to each other because each of the pad groups correspond to an entirely distinct and separate reference signal (GND1, GND2, or GND3). Further, given that Case Study 1 has an on-chip “continuous ring around the active circuitry,” there would be no “plurality of pad groups,” and therefore no need to utilize a “plurality of bonding wires configured to connect one to another of the plurality of pad groups,” as taught by the ’164 Patent.

137. As I have mentioned *supra*, Saint states that bond wires should

only be used where there is “minimal silicon overlap.” Saint, 195. According to Saint, “the bond wire could sag or droop, causing a short in the circuit” and “[s]o, you have to keep the overlap of the bond wire over the unused silicon as short as possible.” *Id.* In view of Saint’s teachings, a POSITA would preferentially use integrated circuit metallization and be discouraged from deliberately forming the bond wire to overlap entirely with “unused silicon” (the alleged “saved areas” shown in orange) as Dr. Foty proposes. Ex.1003 ¶¶ 144-154, 369-373.

138. Like with Grounds 1 and 2, neither the Petition nor Dr. Foty claim that use of bonding wire was one of a finite, small or easily traversable number of options for connecting pads. And even if they did, they did not provide a reason a POSITA would select the route of using bonding wire. For the reasons I discussed earlier in Sections VII.B and VIII.B, a POSITA would not select the use of bonding wire when modifying Saint.

C. Ground 3: Saint, Haralabidis and POSITA Knowledge Do Not Render Obvious “wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area” (claims 1-14)

139. Dr. Foty and Petitioner point out three areas in Figure 7-7 that they claim are “saved spaces,” as shown below in orange. Pet. 81-82; Ex.1003

¶ 384.

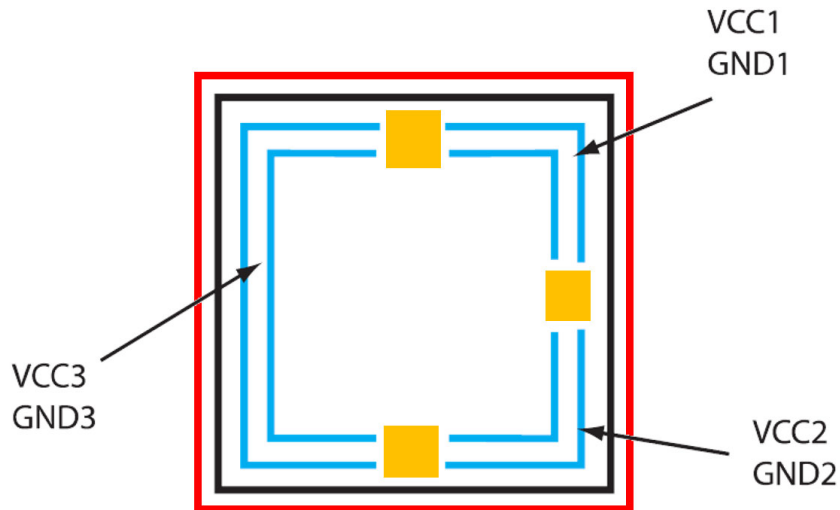


Figure 7-7. Pin-out simplification showing like protects grouped together.

140. But Saint Figure 7-7 does not say that those areas in orange have “no pads” as required by the claims of the ’164 patent. Saint Figure 7-7 does not even show pads, let alone their relative location to each other. As a result, Dr. Foty and Petitioner’s claim that the orange areas are “saved spaces” is conclusory and without support.

141. Saint Figure 7-7 improves upon Saint Figure 7-6 (shown below), which shows an undesirable arrangement of pins that are “scattered” around the chip. Saint, 146-147. Note that in Saint Figure 7-6 there are 16 pins (which would each have an accompanying pad) surrounding the chips, but there is no “saved area” between any of these pins.

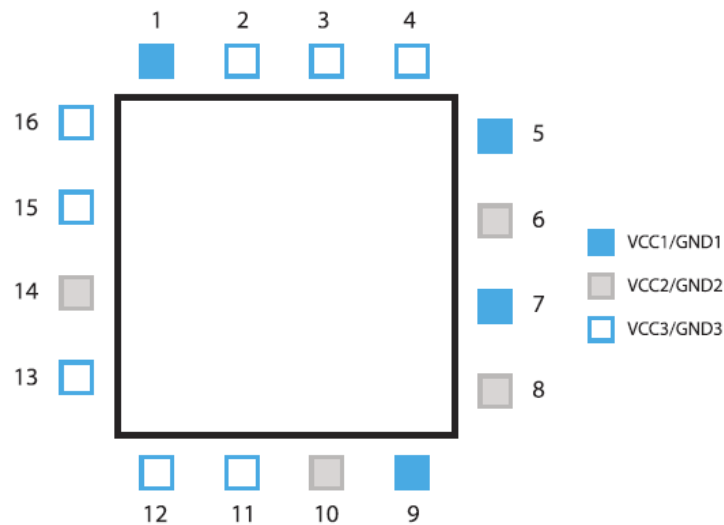


Figure 7-6. Scattered pins on the same protect circuit.

142. Saint Figure 7-7 (below) involves moving “pins 1, 5, 7, and 9” (GND1) in Figure 7-6 “close to each other” and “do[ing] the same for the other supply pin sets” so that the pins corresponding to GND1, GND2, and GND3 are all “located close to each other.” Saint, 147. The resulting Figure 7-7 is a “[p]in-out simplification showing like protects grouped together.”

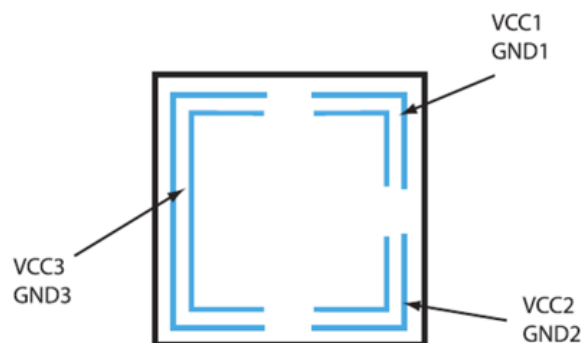


Figure 7-7. Pin-out simplification showing like protects grouped together.

143. Dr. Foty attempts to rectify that lack of disclosure by including

the Figure below, which he says “includes deployment of typical bond pad layouts around the periphery of the IC.” Ex.1003 ¶ 384. While he states this is an “illustrative” image “not drawn to scale,” he also argues that it “clearly shows that Saint’s separate teachings of pad placement and using ‘wasted space’ (in a core-limited IC design situation) would have been (combined with the knowledge of a POSITA) obvious to a POSITA.” *Id.*

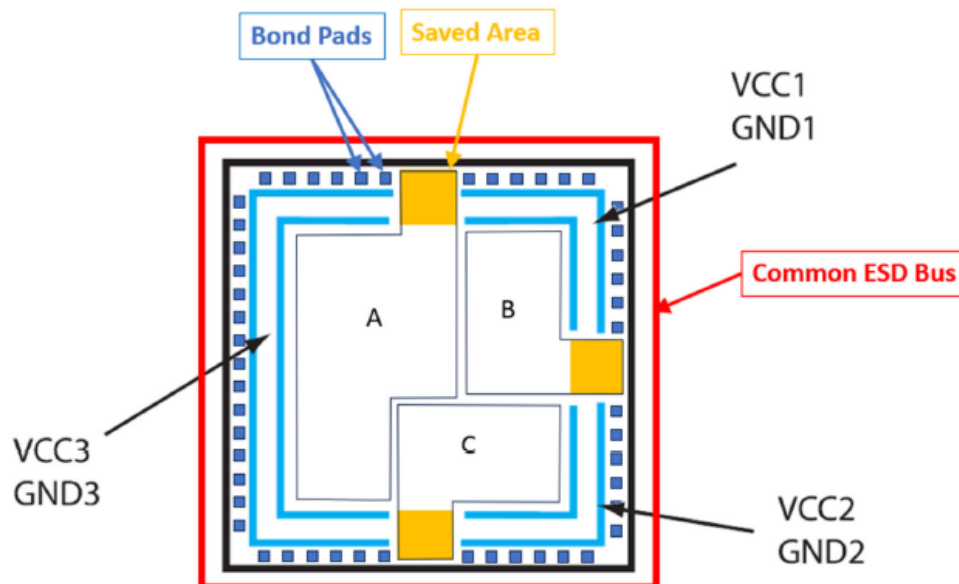


Figure 7-7. Pin-out simplification showing like protects grouped together.

144. When compared to Saint Figure 7-6, which Saint Figure 7-7 is based off, it is clear that the placement of bond pads in Dr. Foty’s “illustrated” figure is completely fabricated and based on hindsight. Instead of 16 pads, Dr. Foty’s modified Figure 7-7 has 51. Instead of the pins (and associated pads) being evenly separated, as shown Figure 7-6, Dr. Foty creates, with no justification, a “saved area” with no pads. Indeed, this very figure contradicts

the teachings of Saint, which teaches to “evenly distribute the pads around the chip if you can.” Saint, 193.

145. Dr. Foty also argues this manipulation of Saint Figure 7-7 is supported “by comparing this combined depiction” with the below “exemplary 2010 microphotograph of a product IC.” Ex.1003 ¶ 384.

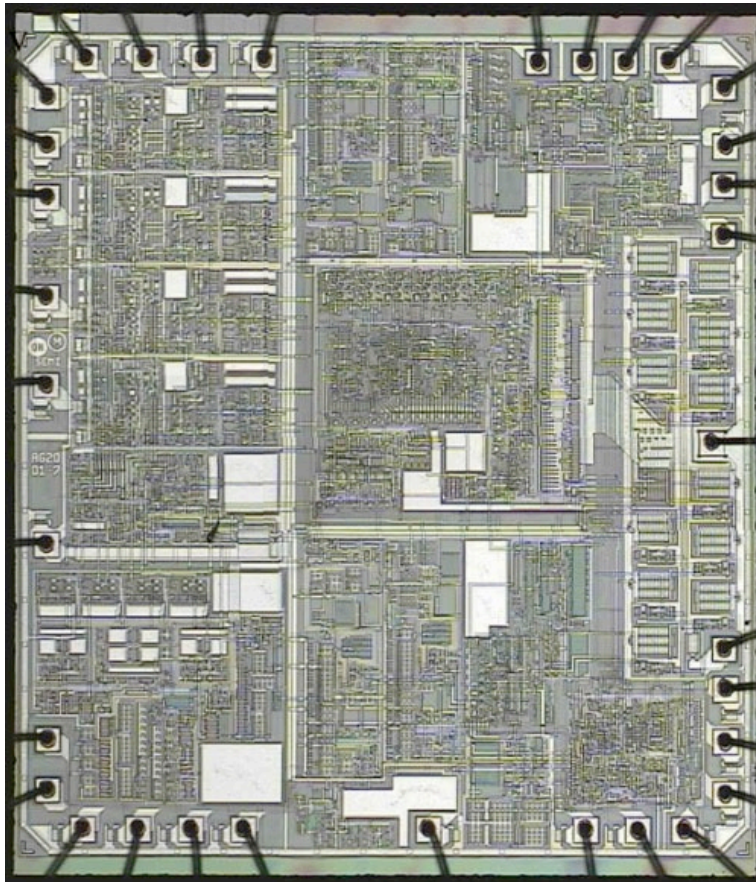


Image from Ex.1003 ¶ 379.

146. Not only is this random image of an IC not listed in Ground 3, it is not clearly the same IC footprint structure as Saint Figure 7-7. There is no indication why this IC has this arrangement of pads, especially since it directly

contradicts Saint's teaching of "evenly distribut[ing] the pads around the chip if you can." Saint, 193. It has a different number of pins and pads than Figure 7-6 and 7-7 of Saint and those pads spaced in a way that is not taught in Saint or Haralabidis. Further, if bond wires were used to connect pads in this microphotograph, they would possibly "caus[e] a short in the circuit." Saint, 195. Dr. Foty or the Petition do not analyze or discuss this possibility.

147. Dr. Foty suggests Saint Figure 7-7 would look like this random image because they are both "core-limited IC designs." Ex.1003 ¶ 384. But Saint Figure 7-7 is never described as a "core-limited IC design," and Dr. Foty does not provide any citation to suggest that it is. Instead, he seems to be combining it also with Figure 9-28, though Figure 7-7 is different from Figure 9-28. *Id.* But even if Saint Figure 7-7 were a "core-limited IC design," such a similarity is a general characterization that would not suggest to a POSITA that Saint Figure 7-7 discloses or renders obvious a design with the claimed "saved space" that does not have a pad or ESD bus in it.

148. Dr. Foty claims that the both the random IC in the photograph and Saint Figure 7-7 "have wasted/saved spaces between the bond pads," and depict "circuitry being deployed into those wasted/saved spaces," but for the reasons I stated in the proceeding paragraphs that is simply not true; Saint Figure 7-7 does not disclose having wasted/saved spaces between bond pads and thus does

not disclose having circuitry in such an alleged space. Ex.1003 ¶ 384. Indeed, a POSITA would avoid creating “wasted space” to minimize chip size.

149. Petitioner is incorrect in claiming that a POSITA would have formed the “saved area” in order “to achieve the benefits of smaller chip size and ESD protection.” Pet. 81. This claim is made without showing why Saint’s ESD protection in Figure 7-7 needs to be improved. A POSITA would understand that Saint’s ESD protection is accomplished in a manner that “makes the chip smaller, keeps parasitics down, and keeps cross talk down from one supply to another.” Saint, 147. Further, a POSITA would not be motivated to add an area that Petitioner shows in their modification of Figure 7-7 of Saint, adjacent to pads without pads or an ESD bus because it would make the chip larger, not smaller, due to the insertion of the alleged “saved area.”

150. Petitioner and Dr. Foty provide no reason a POSITA would have modified Saint Figure 7-7 so that there are spaces without pads, let alone a “saved space” that is both free of pads and ESD buses while also being located adjacent to two ESD buses and two pad groups. I refer to my discussion above in Section VII.C for why a POSITA would not be motivated to form “saved spaces” with “no pad” when the primary references (such as Yoshinaga and Saint’s chapter 7 discussion) do not disclose such a space.

X. Conclusion

All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under penalty of perjury that the foregoing is true and correct.

Executed September 17, 2025, in Boulder, Colorado.



Dr. Sunil Khatri