

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: September 17, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2025-00118
Patent 10,879,164

PATENT OWNER'S RESPONSE

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Exhibit List

Ex.	Description
2001	Micron's Motion to Stay the Case Pending Inter Partes Review and Post Grant Review Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Jan. 16, 2025), ECF No. 200
2002	Plaintiff/Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s and Counterclaim Defendant Yangtze Memory Technologies, Inc.'s Opposition to Micron's Motion to Stay Case Pending Inter Partes Review and Post-Grant Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Feb. 3, 2025), ECF No. 221
2003	Docket Entry Order (issuing temporary stay), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Mar. 3, 2025), ECF No. 242
2004	U.S. District Courts—Time Intervals from Filing Date to Beginning Date for Completed Civil Trials, by District, During the 12-Month Period Ending September 30, 2024 (https://www.uscourts.gov/sites/default/files/2025-01/jb_t3_0930.2024.pdf)
2005	RESERVED
2006	Curriculum Vitae of Dr. Sunil Khatri
2007	Declaration of Dr. Sunil Khatri ("Khatri")
2008	Civil Minutes, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Sept. 18, 2024), ECF No. 141
2009	Defendants' Preliminary Invalidity Contentions and Document Production Accompanying Invalidity Contentions re YMTC II Asserted Patents (Patent Local Rules 3-3 and 3-4), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Nov. 25, 2024) (excerpts)

Ex.	Description
2010	Declaration of Dr. Sunil Khatri in Support of Patent Owner's Response ("Khatri2")
2011	Transcript of the Deposition of Daniel Foty, Ph.D., taken August 6, 2025, <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , IPR2025-00118 (P.T.A.B.) ("Foty Dep.")
2012	Interconnect Technology and Design for Gigascale Integration (Jeffrey A. Davis & James D. Meindl eds., 2003) (excerpts) ("Davis")
2013	Aishwarya Dubey, <i>P/G Pad Placement Optimization: Problem Formulation for Best IR Drop</i> , Proc. of the Sixth Int'l Symp. on Quality Elec. Design (ISQED), San Jose, CA, pp. 340-345 (Mar. 21-23, 2005) ("Dubey")
2014	Howard Johnson, <i>Chip-Scale Transmission Lines</i> , High-Speed Digit. Design Online Newsl. (Signal Consulting, Inc.) (2003), https://www.sigcon.com/Pubs/news/7_01.htm ("Signal Consulting")
2015	Kian Haghdad & Mohab Anis, <i>Power Supply Pads Assignment for Maximum Timing Yield</i> , 58 IEEE Transactions Circ. Sys. 697 (2011) ("Haghdad")

I. Introduction

Patent Owner Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Patent Owner”) respectfully submits this Patent Owner Response to the Petition for inter partes review of U.S. Patent 10,879,164 (“’164 Patent”). As explained below, Petitioner fails to carry its burden to show that any of the challenged claims are unpatentable.

The ’164 Patent discloses a novel “integrated circuit electrostatic discharge bus structure” that comprises a “plurality of pad groups” connected to a “plurality of ESD buses.” ’164 Patent Abstract. The pad groups are connected either “one to another” or to a “common ESD bus” using “bonding wires.” This results in “saved areas” between the “plurality of pad groups” and “plurality of ESD buses” so that additional circuitry can be placed therein.

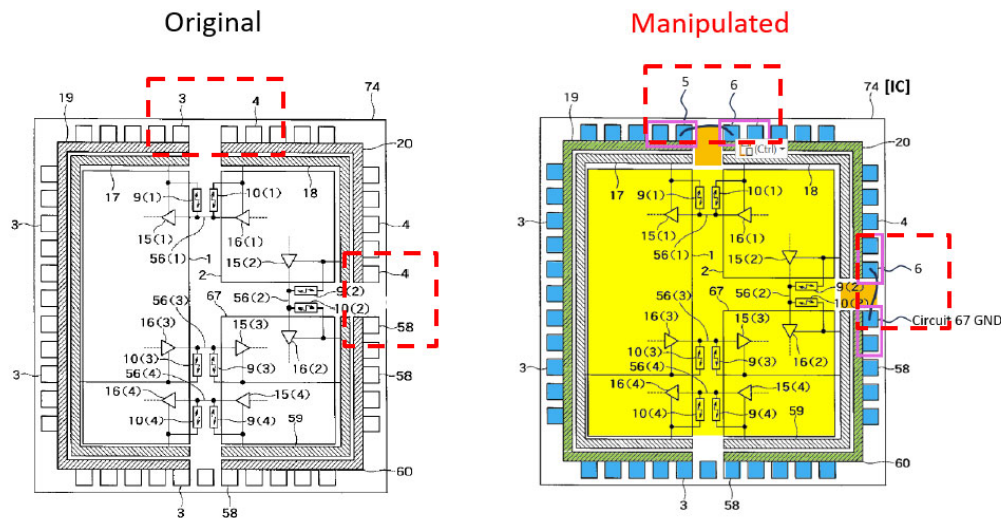
Petitioner relies on two primary references for its three obviousness grounds: Yoshinaga (Ex.1006) (Grounds 1-2), and Saint (Ex.1008) (Ground 3). Each of Petitioner’s proposed Grounds fails.

For Grounds 1 and 2, Petitioner relies on Yoshinaga but concedes that Yoshinaga does not disclose the location of any reference potential pads, let alone a plurality of pad groups, adjacent and connected to the plurality of ESD buses, as claimed. It also admits that Yoshinaga does not teach using bonding wire or the

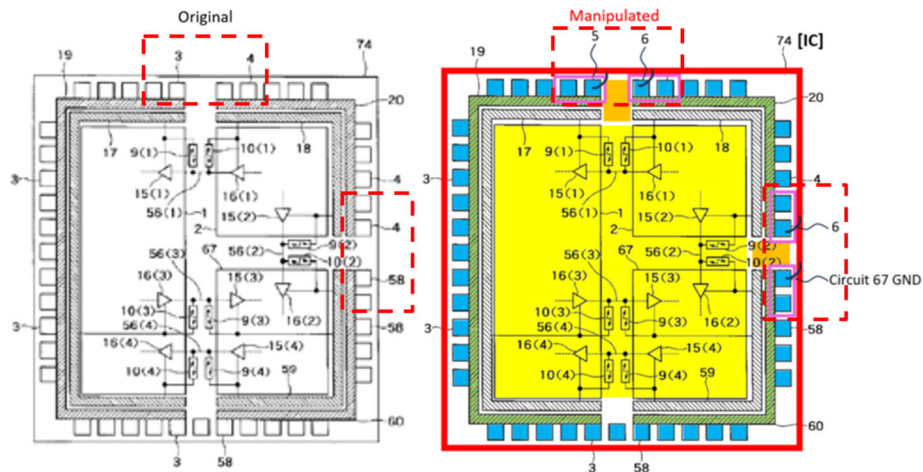
claimed “plurality of bonding wires configured to connect one to another of the plurality of pad groups.” ’164 Patent cl. 6.

Faced with a lack of disclosure in the prior art, Petitioner redraws Yoshinaga's figures to: (i) change “power supply pads” 3, 4, and 58 and an unlabeled pad to “reference potential pads” 5, 6, and “Circuit 67 GND”; and (ii) add bonding wires across the newly added reference potential pads, as shown below:

Petitioner's Ground 1 Manipulations



Petitioner's Ground 2 Manipulations



Petitioner's arguments for Grounds 1 and 2 fail for three reasons. **First**, Petitioner fails to explain why a POSITA would be motivated to convert power supply pads and an unlabeled pad into reference pads nor does it establish that a POSITA would have had a reasonable expectation of success in doing so. Instead, Petitioner merely asserts that a POSITA "could" make such a change. Pet. 31; Ex.1003 ¶137. But even if a POSITA **could** make a change to the prior art, that is not enough to render the claimed inventions obvious. *See, e.g., Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) ("[O]bviousness concerns whether

a skilled artisan not only could have made but *would have* been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”).¹

Second, while Petitioner proposes modifying Yoshinaga by using bonding wire to connect reference pads to each other, it again fails to provide any reason why a POSITA would have allegedly made that modification. Notably, Yoshinaga already teaches connecting potential pads to each other through bidirectional diodes and a common reference potential line, as shown in Yoshinaga Figure 3, or through integrated circuit metallization, as shown in Figures 1-2 and 4. Using bonding wire with Yoshinaga Figure 6 would be redundant and increase noise, undermining Yoshinaga's goals of avoiding noise and reducing cost.

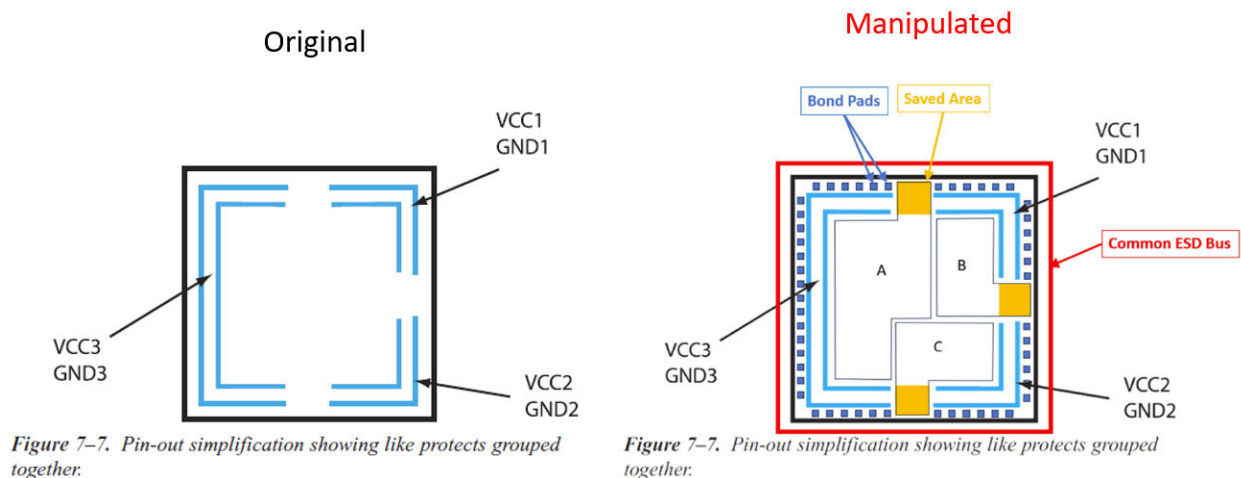
Third, even if Petitioner's modified version of Yoshinaga Figure 6 were proper (it is not), that modified figure in combination with Petitioner's secondary references still fails to render obvious the claimed “saved space” limitations. Petitioner identifies two purported “saved spaces” in its modified version of Figure 6 of Yoshinaga in orange. However, Petitioner provides no support for its assertion that these are the claimed “saved areas.” Yoshinaga expressly teaches that there are reference pads “not shown to simplify the drawing.” Yoshinaga [0078]. POSITAs

¹ Unless otherwise noted, emphases/annotations are added and internal quotation marks/citations omitted.

would have understood that the most likely place for such reference pads are Petitioner's purported "saved areas." Khatri2 (Ex.2010) ¶106.

Petitioner's Ground 3 fares no better. In Ground 3, Petitioner relies on Figure 7-7 of Saint, but it acknowledges that Figure 7-7 does not depict pads, include a common ESD bus, or use bonding wire. Pet. 72-73, 76-81, 92. Instead, as in Grounds 1 and 2, Petitioner redraws Figure 7-7 based on impermissible hindsight, as illustrated below:

Petitioner's Ground 3 Manipulations



But Petitioner's redrawing of Figure 7-7 is based on a fundamental mischaracterization of that figure. Each blue line in Saint Figure 7-7 represents a *different* signal—VCC1/GND1, VCC2/GND2, VCC3/GND3—such that a POSITA would not be motivated to connect them together to form a common ESD bus as Petitioner suggests. In fact, Saint avoids placing any common ESD bus in Figure 7-7 to "make layout easier, make[] the chip smaller, keep[] parasitics down, and keep[]

cross talk down from one supply to another.” Saint 147. Notably, the Board in its Institution Decision recognized the “merit” of this argument and “question[ed] whether a POSITA would have been motivated to apply Saint’s ‘ESD Ground wiring’ or Haralabidis’ common ground rail teachings to Saint’s Figure 7-7 with a reasonable expectation of success.” Inst. Decision, Paper 22 (“ID”), 33-34.

The Board should find claims 1-14 of the ’164 Patent nonobvious.

II. Background

A. The ’164 Patent (Ex.1001)

The ’164 Patent discloses “an integrated circuit electrostatic discharge [ESD] bus structure and related method.” ’164 Patent 1:17-20; Khatri2 ¶¶34-38.

As discussed in the ’164 Patent, it was “commonly [known] to place filler cells F1 and F2 at empty spaces between the I/O pads 12, and connect the filler cells F1 and F2 to an electrostatic discharge (ESD bus) 11.” ’164 Patent 1:30-37. Figure 1 of the ’164 Patent shows an example of this common knowledge, where an integrated circuit electrostatic discharge or “ESD” structure comprises a “circuit area 10,” “I/O pads 12,” and an “electrostatic discharge (ESD) bus 11.” *Id.* 1:24-37.

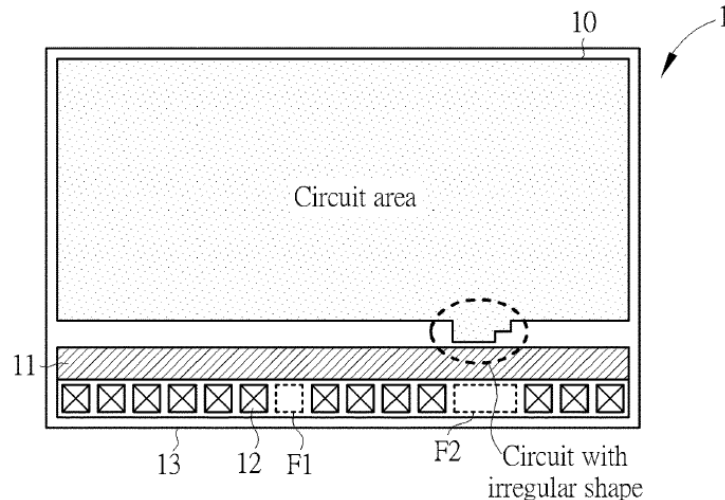


FIG. 1 PRIOR ART

The problem with this arrangement is the “filler cells F1 and F2 take a portion of the circuit area 10 to be wasteful to the integrated ESD bus structure 1.” *Id.* 1:38-43. Likewise, the prior art arrangement “causes the lack of flexibility for internal circuit layout design.” *Id.* 1:40-43. Further, as shown in Figure 1, “when there are circuits with irregular shapes and different areas, the circuit area 10 must be increased in order to contain the circuits with irregular shapes and different areas, which increases production cost.” *Id.* 1:44-47.

The '164 Patent teaches two embodiments where the arrangement of pads and various connections overcome the drawbacks of the prior art. Khatri2 ¶¶36-38.

Figure 2 Embodiment. In Figure 2, there are a “plurality of pad groups G1, G2 and G3” “formed inside the chip edges 23, adjacent and connected to the plurality of ESD buses E1, E2, and E3.” '164 Patent 2:61-63. A “common ESD bus 24 is formed outside the chip edges 23.” *Id.* 2:63-65. Each of the “plurality of pad groups

G1, G2 and G3 includes at least one pad 22” that is “connected to a ground or a system low voltage.” *Id.* 3:6-8. With this arrangement, “the discontinuous ESD buses E1, E2 and E3 may be connected together by connecting pads 22 of the pad groups G1, G2 and G3 to the common ESD bus 24 through bonding wires 25.” *Id.* 3:17-22.

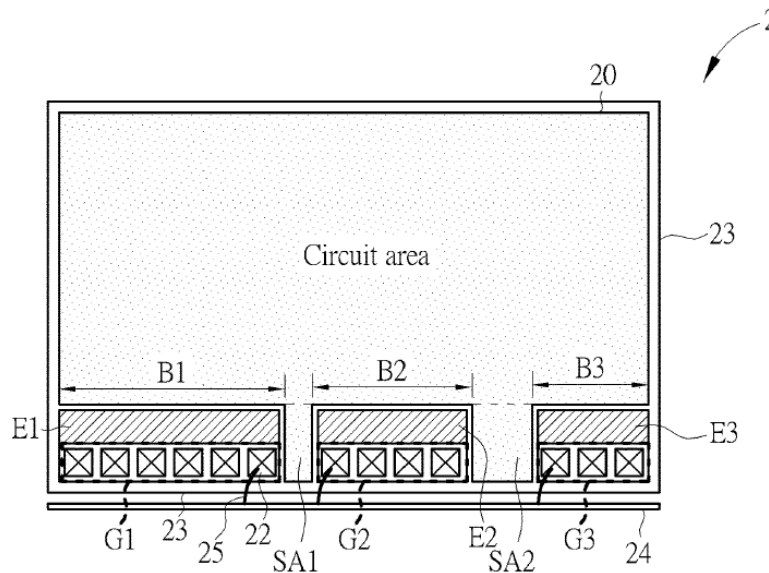


FIG. 2

This resulting inventive arrangement of pads, ESD buses, and their connections may remove “the filler cells of the prior art” and creates “spaces between the discontinuous ESD buses E1 and E2 (or, E2 and E3)” that “may be configured with circuit elements to make full use of the integrated circuit ESD bus structure 3.” *Id.* 3:23-26. Those spaces are identified as “saved areas SA1 and SA2” in the ’164 Patent. *Id.* 3:29-32. Those “saved areas SA1 and SA2” allow for “circuits

with irregular shapes and different areas without increasing its area, which saves production cost. *Id.* 3:20-25.

Figure 3 Embodiment. Figure 3 shows an alternative embodiment with a “circuit area 30,” a “plurality of ESD buses E1, E2 and E3,” a “plurality of pad groups G1, G2 and G3,” and “a plurality of bonding wires 35.” ’164 Patent 3:36-46. Unlike Figure 2, the Figure 3 embodiment includes “bonding wires 35” connecting “pads 32 of one group to another group.” *Id.* 3:64-65. The arrangement in Figure 3 similarly results in the “saved areas” for adding additional circuitry, allowing for “full use of the integrated circuit ESD bus structure.” *Id.* 5:1-7.

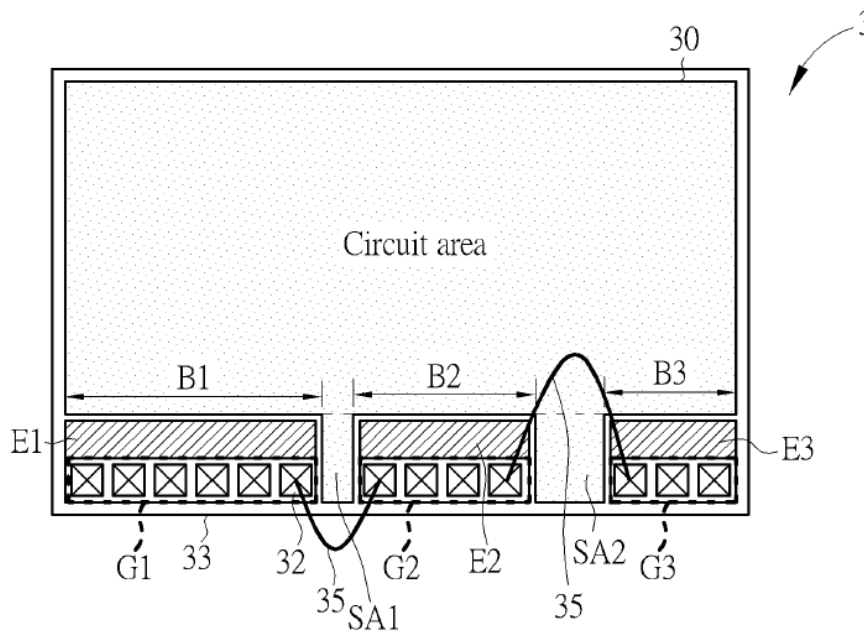


FIG. 3

B. Prosecution History

For brevity, Patent Owner does not address the prosecution history in this Response. Patent Owner's decision to not address the prosecution history here

should not be understood as agreement or acquiescence with the statements made by Petitioner regarding the prosecution history. *See* Pet. 17-18.

C. Person of Ordinary Skill in the Art

Patent Owner does not dispute Petitioner's proposed level of a person of ordinary skill in the art ("POSITA") for purposes of this IPR.² Pet. 27. Regardless of the precise definition of a POSITA, Petitioner's grounds do not render any challenged claims unpatentable.

D. Claim Construction

The prior art relied on in the Petition fails to disclose the subject matter of the challenged claims under any reasonable construction, including their plain meaning.³

E. Petitioner's Cited Prior Art

Petitioner's Grounds rely on three pieces of purported prior art: (1) "Yoshinaga" (Ex.1006), (2) "Saint" (Ex.1008), and (3) "Haralabidis" (Ex.1007).

² Patent Owner reserves the right to argue an alternative level of a POSITA in other proceedings.

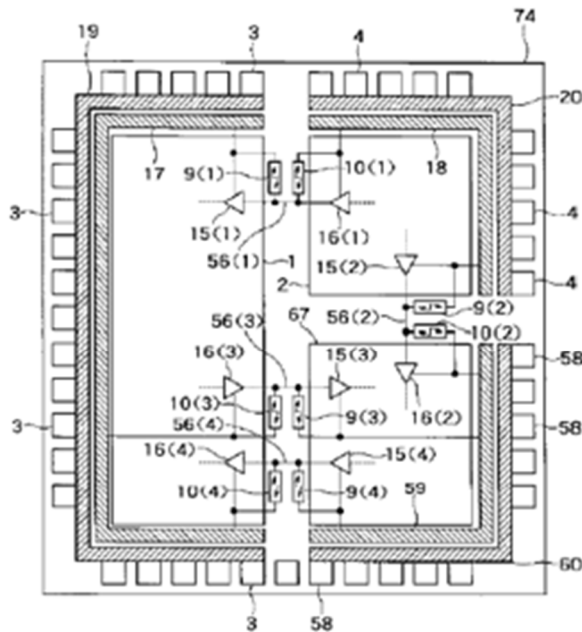
³ Patent Owner reserves the right to advocate for claim constructions in any subsequent district court proceedings.

Below is a general overview of these references, though other disclosures may be referred to in other sections of this response.

1. Yoshinaga (Ex.1006)

Unlike the '164 Patent, Yoshinaga does not disclose a plurality of pads adjacent to a plurality of ESD buses, bonding wire, nor any “saved area.” Instead, Yoshinaga describes a “semiconductor integrated circuit” that “avoids noise” and ensures “there is little increase in the chip size and the total number of wiring” while preventing “increase in the unit price of the chip ... as much as possible.” Yoshinaga [0005], [0086].

Yoshinaga's Figure 6 (shown below) is a schematic diagram of an integrated circuit chip. *Id.* [0087]. “The integrated circuit chip consists of three major circuits: circuit 1, circuit 2 and circuit 67.” *Id.* [0075]. Figure 6 depicts “rectangular power supply pad 3, power supply pad 4, and power supply pad 58 ... disposed near each circuit 1, 2, 67 at the periphery of the chip.” *Id.* [0076]. It further depicts a “reference potential line 19, reference potential line 20 and reference potential line 60,” but no “reference potential pads.” *Id.* [0077]-[0078]. Figure 6 also depicts ESD protective elements 7-10, with ESD protective elements 9 and 10 being “one of the major features” of Yoshinaga. *Id.* [0084].



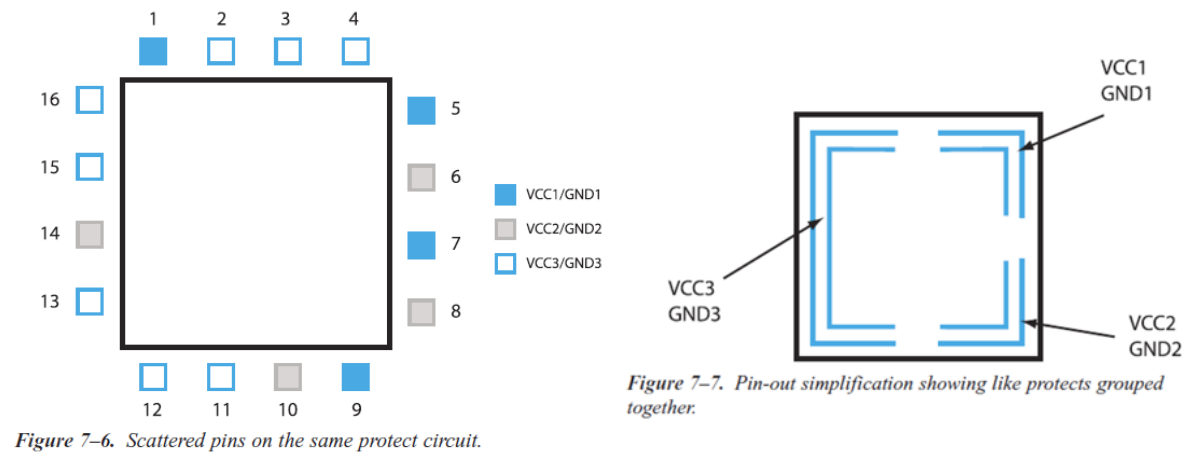
2. Saint (Ex.1008)

Unlike the '164 Patent, Saint is silent on connecting pads to each other or to a common ESD bus using bonding wire. Saint 187-199. At most, Saint discusses “several ways to attach bond pads to package pins,” and identifies “wire bonding” as a possibility for this particular type of connection. *Id.* 189-191.

Saint is also silent on the reassignment of pads and the use of bonding wire to connect pad groups. *Foty Dep.* (Ex.2011) 218:18-219:9; *Khatri2 ¶¶62, 79*. Instead, Saint describes a chip where pins 1, 5, 7, and 9 are protected to VCC1 and GND1 (shown in Figure 7-3), pins 6, 8, 10, and 14 are protected to VCC2 and GND2 (shown in Figure 7-4), and all other pins “protected to VCC3 and GND3.” (shown in Figure 7-5). Saint 145-47. Saint then discloses in Figure 7-6, “a final pin-out for

the package, show[ing] the coordinated colors for each of these protection schemes.”

Id. 146. It then advises reorganizing the pin-out such that “the four signals that were on pins 1, 5, 7, and 9” are moved “close to each other” and then repeating the same with the other grouping of pins. *Id.* 147. The result is shown in Figure 7-7, which is a pinout simplification of that reorganization. *Id.*



Further, Saint does not teach including a “saved space” adjacent to pads and ESD buses. Khatri2 ¶108. Rather, it encourages “evenly distribut[ing] the pads around the chip if you can,” and to avoid “wasted space.” Saint 193, 206-07. It states “[m]aybe you can push some of your circuitry into this wasted space to try to use those gaps” when there is “wasted space around the edges between the pads.” Pet. 40-41; Saint 206-07. Saint’s disclosure is silent on forming a defined “saved area” between two ESD buses and pad groups as claimed in the ’164 Patent. Khatri2 ¶108.

3. Haralabidis (Ex.1007)

Likewise, Haralabidis does not disclose a plurality of pads adjacent to a plurality of ESD buses, connecting pads via bonding wire, nor any “saved area.” Indeed, Haralabidis does not focus on the chip itself but rather an entire “electronic device,” including a PCB. Haralabidis Abstract.

Petitioner relies on two embodiments discussed in Haralabidis, Figures 3 and 5 (reproduced below), both of which include a “common ground rail” connected to a “segmented”—but common—ground signal. Haralabidis 3:9-22, 3:65-4:20; Khatri2 ¶¶118, 129.

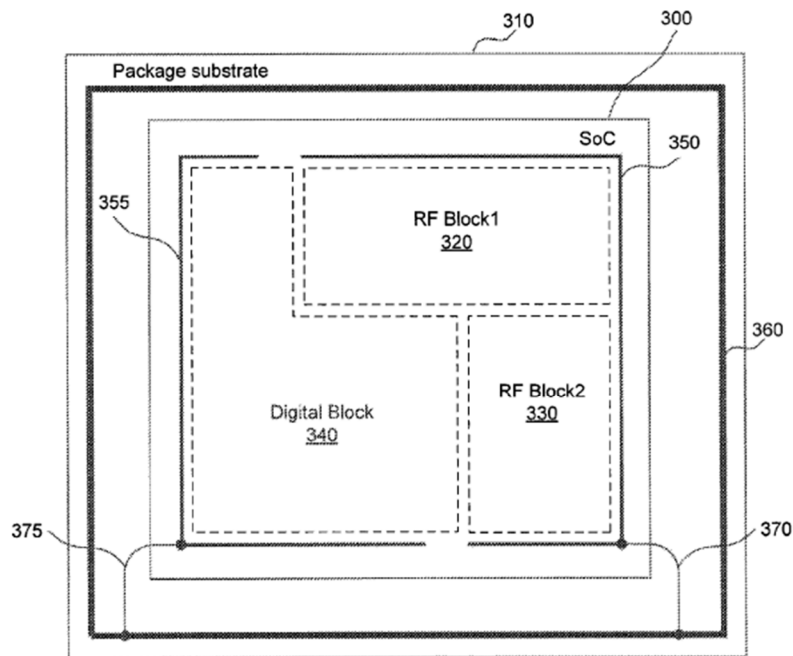


FIG. 3
Conventional Art

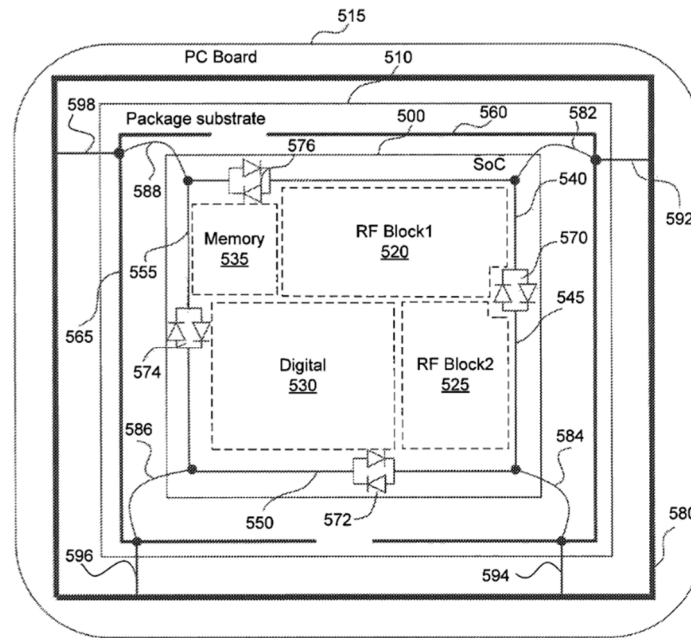


FIG. 5

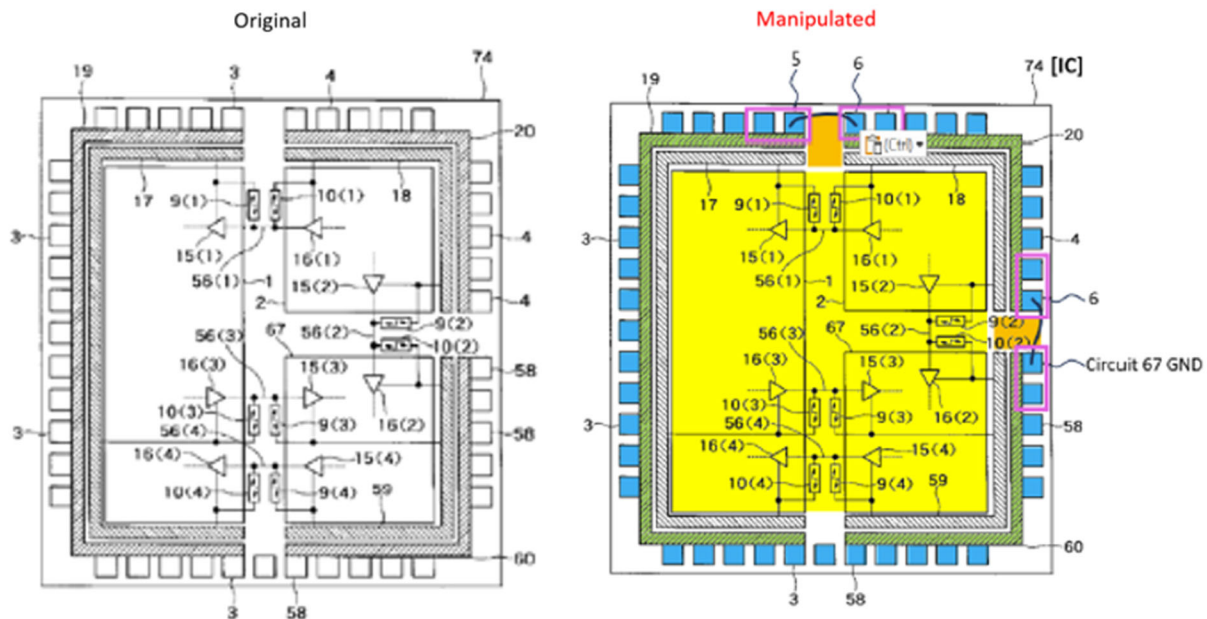
III. Ground 1: Petitioner fails to demonstrate that Yoshinaga, Saint, and knowledge of a POSITA would render obvious claims 6-7, 12 and 14

Yoshinaga in view of Saint and knowledge of a POSITA does not teach and would not have rendered obvious (1) a “plurality of pad groups” “adjacent and connected to the plurality of ESD buses,” (2) “connecting” the “pad groups” by “bonding wires,” or (3) “one saved area” as is required by claims 6-7, 12 and 14.

Petitioner's obviousness arguments rely on its redrawn version of Yoshinaga's Figure 6, which makes six modifications to the prior art's disclosure:

(1) "chang[ing] the label on the pad (blue) to the left of the alleged saved area (orange) at the top of the chip from '3' to '5'," (2) "remov[ing] the '4' label from the pad (blue) to the right of the alleged saved area (orange) at the top of the chip," (3) "label[ing] the pad (blue) immediately to the right of the saved area (orange) at

the top of the chip '6',” (4) “chang[ing] the label on the pad (blue) above the alleged saved area (orange) on the right side of the chip from '4' to '6',” (5) “chang[ing] the label on the pad (blue) below the saved area (orange) on the right side of the chip from '58' to 'Circuit 67 GND',” and (6) adding bond wire between the newly labeled 5 and 6 and between the newly labeled 6 and 67. ID 14-15; Pet. 31-32, 45; Foty Dep. 123:2-125:12, 128:19-129:5. Petitioner's redrawn figure is not prior art and its modifications, both independently and in combination, constitute impermissible hindsight.



- A. Petitioner fails to show that “a plurality of pad groups, adjacent and connected to the plurality of ESD buses” as claimed in claims 6-7, 12, and 14 would have been obvious in view of Yoshinaga, Saint, and knowledge of a POSITA**

Each of the Challenged Claims recites a plurality of pad groups “adjacent and connected to the plurality of ESD buses.” ’164 Patent cls. 6-7, 12, 14.

1. Yoshinaga does not disclose a plurality of pad groups, adjacent and connected to the plurality of ESD buses

It is undisputed that Yoshinaga does not disclose a plurality of pad groups adjacent and connected to a plurality of ESD buses. Petitioner identifies Yoshinaga's "[r]eference potential pads" as the claimed "plurality of pad groups" but acknowledges that Yoshinaga does not disclose reference potential pads adjacent to the plurality of ESD buses. Pet. 30-31; Foty Dep. 262:22-264:11. Indeed, Petitioner's expert admits that "Yoshinaga [does] not disclose a plurality of pad groups adjacent and connected to a plurality of ESD buses." Foty Dep. 255:13-17; *see also id.* 168:14-169:10. He also admits that Yoshinaga "explicitly says nothing" about "the location of the reference potential pads." *Id.* 264:4-11; *see also id.* 257:10-258:14. Petitioner claims "Yoshinaga Figure 6 is an illustrative rendering, not intended to necessarily reflect the exact number of pads present or their electrical connections," and thus it cannot reflect the adjacency and connection of the pads. Pet. 31.

Petitioner argues that "Yoshinaga Figs. 1-4 confirm that pad groups [are] connected to reference potential lines 19, 20, and 60." *Id.* 33. But the claims require a plurality of pad groups that are **adjacent** as well as connected to ESD buses. '164 Patent cls. 6-7, 12, 14. Petitioner does not (and cannot) assert that Yoshinaga's Figures 1-4 meet this limitation. Indeed, Petitioner's own expert explained that Yoshinaga Figure 1 "is silent by design" "about whether 5 and 6 are adjacent to ESD

buses” and “does not show whether reference potential pads 5 and 6 are adjacent to ESD buses.” Foty Dep. 168:14-19; Khatri2 ¶41. Figures 1-4 are simply “topological depiction[s]” that “ha[ve] nothing to do with any physical location of anything,” and thus do not (and cannot) show whether pads are located adjacent to ESD buses. Foty Dep. 168:14-170:6; Khatri2 ¶¶41-42. None of the Figures in Yoshinaga depict the physical location of the reference potential pads, let alone where they are physically located relative to the ESD buses, and thus do not disclose reference potential pads “adjacent ... to the plurality of ESD buses.”⁴ Khatri2 ¶¶41-44.

Faced with this complete lack of prior art disclosure, Petitioner relies on attorney argument and expert testimony to redraw Yoshinaga's Figure 6, modifying the prior art's disclosure in an effort to more closely approximate the claimed inventions. Pet. 30-34. But Petitioner's argument violates the PTAB's rules, which require petitions to “specify where each element of the claim is found in the prior art patents or printed publications relied upon.” *See* 37 C.F.R. § 42.104(b)(4); *cf. Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1373-77 (Fed. Cir. 2022) (vacating

⁴ Petitioner suggests, without explanation or support, that “adjacent” may not require “the claimed pad groups and plurality of ESD buses to share a border or endpoint.” Pet. 33. But Petitioner fails to establish that the claimed pad groups are “adjacent” to the plurality of ESD buses under any reasonable construction.

and remanding to determine whether applicant admitted prior art improperly formed the basis of petitioner's patentability challenge). Here, it is undisputed that this limitation is not disclosed in the prior art relied upon by Petitioner and the Board should reject Petitioner's effort to substitute attorney argument and expert testimony for actual prior art disclosure.

2. Petitioner fails to identify any motivation to replace power supply pads in Yoshinaga Figure 6 with reference potential pads

Petitioner relies on its redrawn version of Yoshinaga's Figure 6 to argue that the prior art renders obvious a "plurality of pad groups" "adjacent and connected to the plurality of ESD buses." Pet. 30-34, 44-46. However, Petitioner fails to establish that a POSITA would have been motivated to modify Yoshinaga's Figure 6 as it proposes.

Petitioner argues that it would have been obvious "to use the pads immediately next to the saved areas as reference pads" because a POSITA "could" have done so and "pad assignments were left to the designer's discretion." *Id.* 31. Petitioner is wrong. As a preliminary matter, Petitioner's assertion that Yoshinaga's power supplies "could" be replaced with reference potential pads (*id.*) is legally insufficient to establish a motivation to modify Yoshinaga. *See Belden*, 805 F.3d at 1073 ("[O]bviousness concerns whether a skilled artisan not only could have made but

would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”).

Nor does Petitioner's reliance on “design choice” excuse it from establishing that there would have been a motivation to modify Yoshinaga's Figure 6 as it proposes. *See* Pet. 31. “Merely stating that a particular placement of an element is a design choice does not make it obvious” as there must be a “reason for why a person of ordinary skill would have made the specific design choice” in question. *Cutsforth, Inc. v. MotivePower, Inc.*, 636 F. App'x 575, 578 (Fed. Cir. 2016) (vacating and remanding for further proceedings); *Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1069 n.4 (Fed. Cir. 2018) (“[m]erely stating that a particular placement of an element is a design choice does not make it obvious”); *Fanduel, Inc. v. Interactive Games LLC*, 966 F.3d 1334, 1344 (Fed. Cir. 2020) (affirming PTAB rejection of argument that adding a look-up table was “an obvious design choice” due to “a gap between the concept of a look-up table being well-known and the beneficial application of that concept to” the prior art).

Tellingly, Petitioner asserts that “selecting which pads to use for ground, power, signals, etc. is a design choice that depends on factors like chip size, the number of I/O signals, and the number of pads available.” Pet. 31. But Petitioner and its expert neither consider nor analyze any of these factors when determining whether a POSITA would be able to support changing power supply pads 3, 4, and

58 or other pads in Yoshinaga Figure 6 into reference potential pads. Khatri2 ¶¶63-71. Instead, Petitioner concludes based only on expert say-so that “[a] POSITA would also have understood the pads labelled 3, 4, and 58 could just as readily be used as reference pads.” Pet. 31 (citing Ex.1003 ¶¶137-139). Such “[g]eneral and conclusory testimony ... does not suffice as substantial evidence” of obviousness. *Juniper Networks, Inc. v. Correct Transmission, LLC*, 2024 WL 3517862, at *6 (Fed. Cir. July 24, 2024) (citing *Koito Mfg. Co. v. Turn-Key-Tech, LLC*, 381 F.3d 1142, 1152 (Fed. Cir. 2004)).

Next, Petitioner asserts that a POSITA would have modified Yoshinaga's Figure 6 as it proposes “to preserve Yoshinaga's saved area for other circuitry.” Pet. 31-32. Petitioner is wrong and fails to explain why replacing a power supply pad with a reference pad would preserve a saved area. “[P]reserv[ing] Yoshinaga's saved area” would, at most, motivate a POSITA not to place the reference potential pads in Yoshinaga's alleged “saved area” (highlighted orange by petitioner). Khatri2 ¶¶60-63. It does not provide any motivation for a POSITA to take Yoshinaga's power supply pads 3, 4, and 58 and change them into reference potential pads, as proposed, nor does it explain how such a significant change would work. *Id.* To the contrary, the purported saved area, if it exists in Yoshinaga's unmodified Figure 6, would remain even without the changes Petitioner proposes. *Id.* ¶61; *see also Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017) (“[A]

clear, evidence-supported account of the contemplated workings of the combination is a prerequisite to adequately explaining and supporting a conclusion that a relevant skilled artisan would have been motivated to make the combination....”). Indeed, power supply pads and reference potential pads are fundamentally different: they are connected to different circuit elements and serve entirely different purposes. Khatri2 ¶¶44-45.

Further, Yoshinaga expressly states that “[r]eference potential pads are not shown to simplify the drawing” in Figure 6. Yoshinaga [0078]. Thus, the pads that are shown in Figure 6—such as power supply pads 3, 4, and 58—are not reference potential pads. Khatri2 ¶¶41-44. Petitioner attempts to sidestep this flaw by asserting that “in Yoshinaga’s vernacular, the statement that ‘[r]eference potential pads are not shown’ ... simply means they are not labelled.” Pet. 20. Petitioner cites no support for its assertion that “not shown” actually means “not labeled.” As Petitioner recognizes, there are many other pads that are “not labelled” in Figure 6 (*id.*), yet Yoshinaga does not state that those other types of pads are all “not shown” merely because they are “not labelled.”

Indeed, Yoshinaga consistently uses the term “not shown” to refer to elements that do not appear in a figure. Yoshinaga [0084] (“previous ESD protective elements” are “not shown in Fig. 6” because they are “provided in the underside” and not depicted), [0066] (“short[ing]” the “[t]he internal circuit reference potential terminal

44 and the signal terminal 46 in the internal circuit 14” is “not shown” in Figure 4 and the internal circuitry of 14 is not depicted).

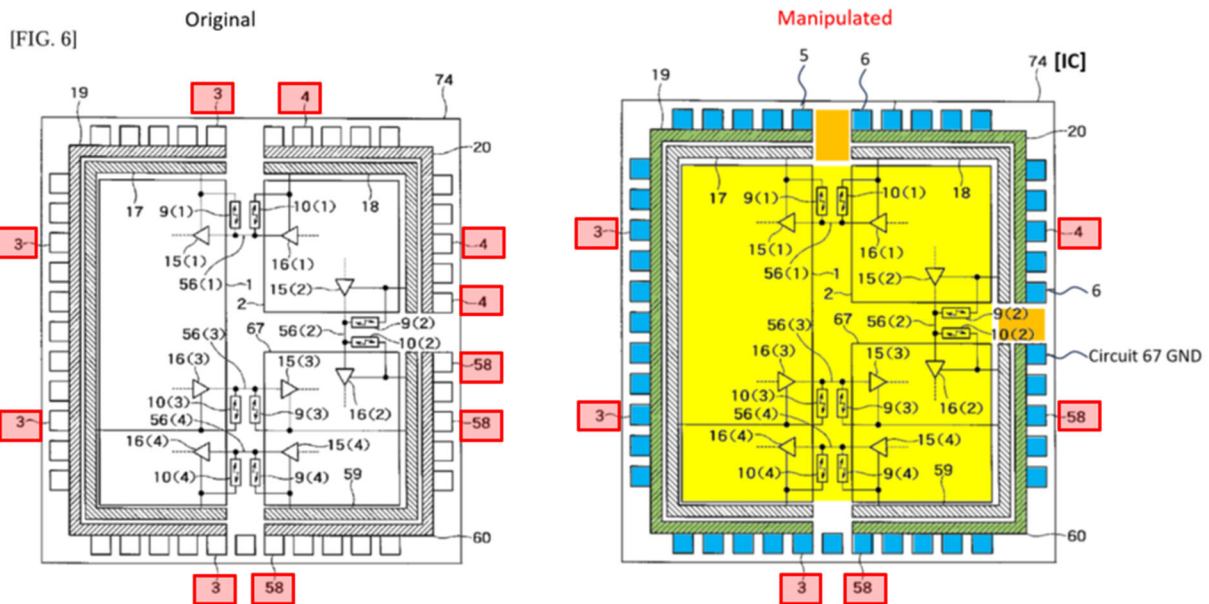
3. POSITAs would not have been motivated to change Yoshinaga's power supply pads into reference pads

In addition to failing to identify a sufficient motivation to modify Yoshinaga's Figure 6 as it proposes, Petitioner also fails to appreciate or address the disadvantages of its proposed modifications. Power supply pads and reference potential pads are fundamentally different—they are connected to different circuit elements and serve entirely different purposes. Khatri2 ¶¶44-45. A POSITA would have understood there was good reason *not* to make the modifications Petitioner proposes and that the Petitioner cannot arbitrarily change pads from unlabeled or supply pads to reference potential pads. *See* Saint 187 (“[y]ou cannot just blindly put your input/output pads wherever you feel like it”); Khatri2 ¶¶44-71.

Replacing “power supply pads 3, 4, and 58” with reference supply pads and a Circuit 67 GND (a reference line) (Pet. 31) would have fundamentally altered and negatively affected the electrical operation of the chip in Figure 6. Petitioner proposes replacing four of the ten power supply pads identified in Yoshinaga's Figure 6 (as annotated with red highlight below) with either a reference supply pad or connection to ground. Yoshinaga [0088]; Pet. 32. Petitioner's redrawn version of Figure 6 would thus have a 40% overall reduction in power supply pads, with a 25% reduction in Circuit block 1 (4 to 3 power supply pads), a 66% reduction in Circuit

block 2 (3 to 1 power supply pads), and a 33% reduction in Circuit block 67 (3 to 2 power supply pads). Khatri2 ¶¶46, 48, 53.

Moreover, because each supply pad provides only a certain amount of current (power), it would not be possible to use fewer power pads that each provide a larger amount of power to provide the same total amount of power to the chip. *Id.* ¶59; Saint 88. Supply and reference pads use maximally wide on-chip wiring to connect to the internal circuitry of the chip. Khatri2 ¶59; Haghdad (Ex.2015) 1, 3. Thus, a POSITA cannot use fewer pads that support a larger current. Khatri2 ¶59.



POSITAs understood that the placement of power supply pads is not random. Khatri2 ¶¶44-57. Petitioner's own prior art reference, Saint, teaches that a POSITA would "look at the drive strengths in the cells" and place "more power strapping" in "certain areas that require more power." Saint 15. Importantly, a POSITA would

have understood that Yoshinaga's Figure 6 included the number of power supply pads necessary to power each of the respective circuit blocks. Khatri2 ¶¶46-47. POSITAs understood that doing so would have been standard practice: only components necessary for a circuit to function are included. *Id.* ¶46; Foty Dep. 69:11-71:25 ("in this business, you only put on what you need"), 72:1-11 ("Q. So in your experience, is it standard practice to add components only when they are necessary for the design's function? A. I think that's a fair statement.").

Even if redundant supply pads existed in Yoshinaga (and a POSITA would not understand these pads to be redundant), their placement would be based on the localized power consumption of the chip. Those "redundant" pads would be needed for the system to function correctly and a POSITA would not remove them. Khatri2 ¶¶58-59. Removing "redundant" pads without replacing them would increase the IR drop, and have detrimental effects on circuit operation. *Id.* Thus, even "redundant" pads cannot just be removed without affecting the performance of the circuit. *Id.*

The drastic reduction in power to the circuits that Petitioner proposes would negatively impact the chip's operation, resulting in the chip running slower, "operating problems," and potentially circuit failure. Foty Dep. 151:13-20 (explaining that, with less power supply pads than the need for current required, "the

circuit might have operating problems” and “[t]he voltage would droop because you can’t maintain the voltage on the bus”); Khatri2 ¶¶48-59; Dubey (Ex.2013) 1, 5.

With a reduced number of supply pads, the effective supply resistance would increase, increasing the IR (also called voltage) drop, which can cause “slower switching speeds” and potential make the chip “not work at all due to hold violations. Khatri2 ¶¶48-59; Dubey 1. Further, the change of the unlabeled pad (possibly a critical pad like a clock signal pad) to reference potential pad 6 could also result in excessive noise. The unlabeled pad is located toward the center of the row, where its wiring to the package would be more efficient. But by removing or relocating this pad, Petitioner’s modified design would have less efficient wiring, resulting in increased noise of critical signal and possibly rendering Petitioner’s manipulated design non-functional. Khatri2 ¶51. Thus, a POSITA would have been discouraged from manipulating Figure 6 as Petitioner alleges because those changes would negatively affect operation of Figure 6’s chip. *Id.* ¶¶44-59.

Indeed, Petitioner’s modification would “interfere with [Yoshinaga’s] stated purpose” of “avoid[ing] noise” (Yoshinaga [0005]) and “gives in to the very hindsight bias the obviousness inquiry is designed to avoid.” *Medtronic, Inc. v. Teleflex Innovations S.a.r.l.*, 69 F.4th 1341, 1349 (Fed. Cir. 2023) (the “destruction of a device’s primary purpose” is “at odds with common sense and gives in to the very hindsight bias the obviousness inquiry is designed to avoid”).

Notably neither Petitioner nor its expert provide for the addition of supply pads to replace the power loss that would come from changing supply pads 3, 4 and 58 to reference potential pads. Khatri2 ¶49. To the contrary, Petitioner expressly relies on the *replacement* of “pads 3, 4, and 58” as those pads “could just as readily be used as reference pads.” Pet. 31; *see also* Ex.1003 ¶137; Foty Dep. 123:2-125:12 (describing modifications of Yoshinaga Figure 6). Petitioner cannot now modify its obviousness theory to now add power supply pads to Yoshinaga. *See Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.*, 853 F.3d 1272, 1286 (Fed. Cir. 2017) (“Continental’s subsequent arguments amount to an entirely new theory of prima facie obviousness absent from the petition. Shifting arguments in this fashion is foreclosed by statute, our precedent, and Board guidelines.”).

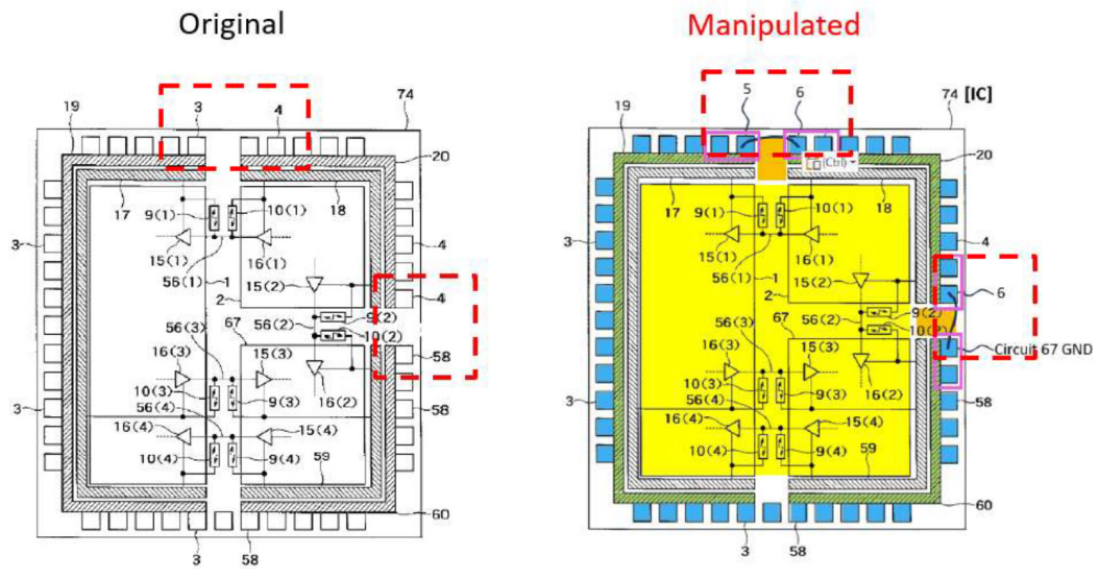
B. Petitioner fails to show that “a plurality of bonding wires configured to connect one to another of the plurality of pad groups” as claimed in claims 6-7, 12, and 14 would have been obvious in view of Yoshinaga, Saint, and knowledge of a POSITA

Each of the Challenged Claims in Ground 1 (claims 6, 7, 12, and 14) recites “a plurality of bonding wires configured to connect one to another of the plurality of pad groups” (claims 6 and 7) or “connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires” (claims 12 and 14). As discussed above, Petitioner identifies Yoshinaga’s “[r]eference potential pads” as the claimed “plurality of pad groups” (Pet. 30-31), and redraws

Yoshinaga's Figure 6, modifying the prior art's disclosure so that it includes reference pads that are adjacent and connected to "ESD buses."

However, Petitioner acknowledges that Yoshinaga does not disclose any "bonding wires"—let alone "bonding wires" that connect reference pads. *Id.* 34-35. Petitioner nevertheless asserts that Yoshinaga, Saint, and the knowledge of a POSITA render obvious "a plurality of bonding wires configured to connect one to another of the plurality of pad groups." *Id.* To support its arguments, Petitioner proposes a further modification of Yoshinaga's Figure 6, drawing bonding wires between its newly added reference potential pads 5 and 6 and between added pad 6 and Circuit 67 GND.⁵ Pet. 36.

⁵ Circuit 67 GND is not a pad per Petitioner's expert but rather "a reference line for circuit 67." Ex.1003 ¶138. Thus modifying Figure 6 to use bonding wire to connect Circuit 67 GND (a reference line), to pad 6 does not satisfy the requirement that "a plurality of pad groups" be connected through bonding wire.



As explained below, a POSITA would not have been motivated to add bonding wires to Figure 6 or had a reasonable expectation of success in doing so. Khatri2 ¶¶72-95. As such, Petitioner fails to meet its burden to show that these limitations would have been obvious.

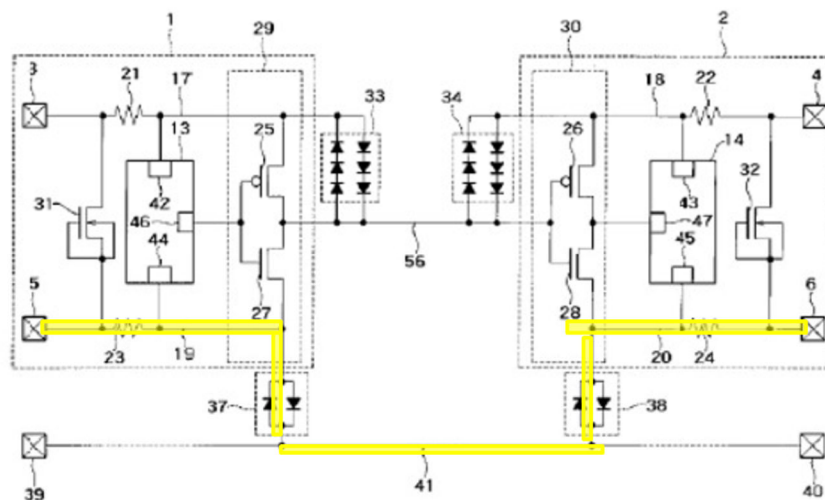
1. There is no motivation to combine Yoshinaga with Saint and knowledge of a POSITA to connect reference potential pads with bonding wires

Petitioner acknowledges that Yoshinaga fails to disclose the use of “bonding wire” to “connect the reference lines” and “to connect pad groups” but argues that “an obvious way to connect Yoshinaga’s reference potential lines ... is by wire bonding the pads connected to the respective buses” as shown in Petitioner’s modified version of Figure 6. Pet. 34-35; Foty Dep. 136:8-137:9. Petitioner is wrong. Petitioner fails to establish that a POSITA would have been motivated to connect

reference potential lines by bonding wire to arrive at the claimed limitations of the '164 Patent for at least five reasons.

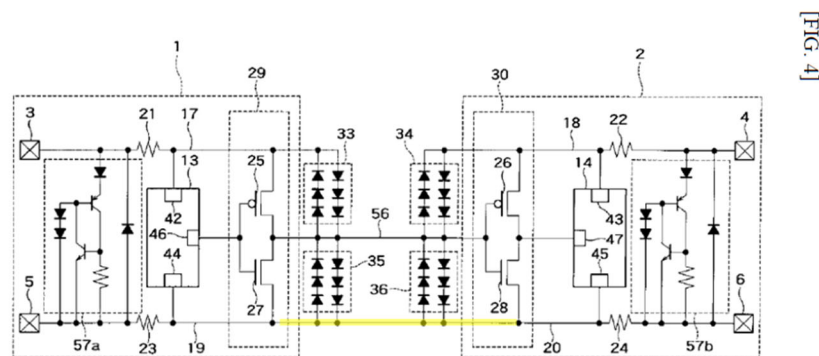
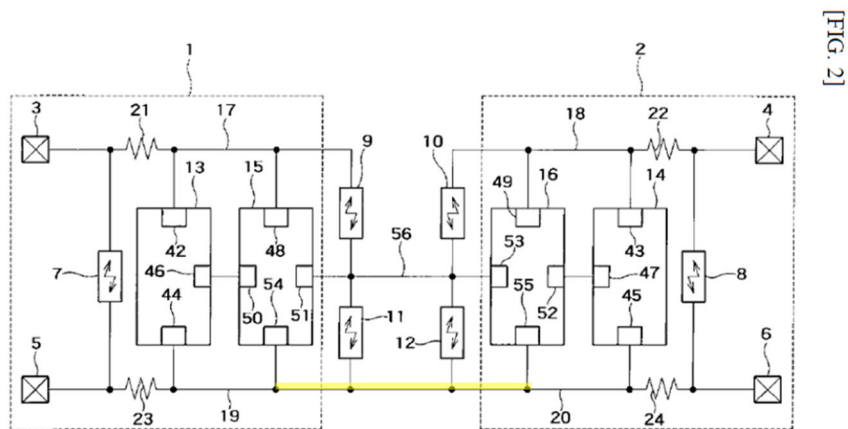
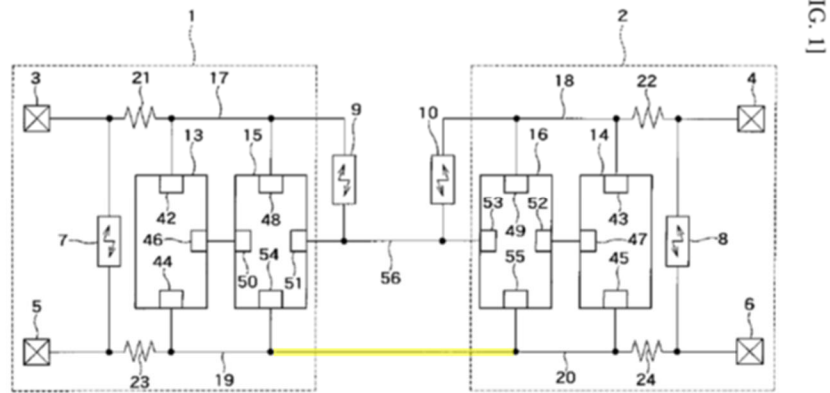
First, Petitioner asserts that Yoshinaga “is silent regarding the mechanism used to connect the reference lines.” Pet. 35. Petitioner is wrong. In fact, Figures 1-4 each include a connection between the reference lines that is **not** made using bonding wire. Yoshinaga Figs. 1-4; Khatri2 ¶¶74.

For instance, Yoshinaga Figure 3 shows reference potential lines 19 and 20 connected to each other through bidirectional diode pairs, as annotated below. Yoshinaga [0061], Figure 3; Foty Dep. 160:15-18; Pet. 22; Ex.1003 ¶¶75-76; Khatri2 ¶¶73, 86-90. Yoshinaga expressly discloses that “[t]he reference potential lines may be connected by bidirectional diodes that are connected in parallel to one another in the opposite direction to avoid noise.” Yoshinaga [0005]; *see also id.* [0061]; Khatri2 ¶¶73, 86-90. An annotated version of Figure 3 is duplicated below:



Yoshinaga Fig. 3 (annotated).

Similarly, Yoshinaga Figures 1, 2, and 4 each show a shorted connection (highlighted in yellow below) that is comprised of the integrated circuit metallization, i.e. the layers of metal used to form the circuit. Khatri2 ¶¶74-76, 91-92. A POSITA would understand that when looking at topological diagrams like Figures 1-4, connections between nodes (depicted as dots on these figures) are metal wires formed from the metal layers in the circuit. Khatri2 ¶¶74-77; Foty Dep. 163:12-164:5. Dr. Foty, during his deposition, confirmed that the wires depicted in Yoshinaga Figure 1 “would be comprised of the integrated circuit metallization in some way, shape, or form.” Foty Dep. 164:18-165:14.



Yoshinaga Figs. 1, 2, and 4 (annotated).

Figures 1-4 are directly relevant to Petitioner's arguments regarding Figure 6. Yoshinaga discloses that Figure 6 "include[es] the semiconductor integrated circuit of FIG. 1" and thus Figure 1's connection of the reference potential lines through the shorted metal connection shown. Yoshinaga [0087]. Further, Petitioner asserts that Figure 6 includes the design principles of Figures 1-4. Pet. 22 ("Although Figs. 1-4 focus on ESD circuitry and connections for circuits 1 and 2, a POSITA would have understood the same design principles and ESD connections apply to circuit 67 in Fig. 6."); Ex.1003 ¶76 ("Yoshinaga combines these disclosures [including those regarding Figure 3] into an IC embodiment in Figure 6."); Foty Dep. 160:10-161:2 (Figure 6 "could include any of those [Figures 1 through 3] as circuit blocks.").

Despite its insistence that Figures 1-4 apply the same design principles as Figure 6, Petitioner ignores Yoshinaga's disclosures in those figures and fails to explain why a POSITA would have been motivated to replace the bidirectional diodes or integrated circuit metallization with bonding wire, as it proposes. Indeed, POSITAs would not have been motivated to do so—adding bonding wire would have been redundant, and as explained in detail below, introduced noise into the circuit. *See infra* Section III.B.2.

Second, Petitioner's obviousness arguments fail to identify why a POSITA would have allegedly been motivated to use bonding wire to connect a plurality of pad groups. The only alleged benefit of using bonding wire that Petitioner identifies

is that it “result[s] in ‘firmly attach[ed]’ connections. Pet. 50. But Petitioner identifies no advantage that would arise from using such purportedly “firmly attach[ed] connection[s]” in Yoshinaga, nor does it provide any reason why it would constitute an improvement over the specific connections Yoshinaga teaches. Without any identified advantage of using bonding wire over what is taught in Yoshinaga, the disadvantages of using bonding wire, which include increased and unnecessary noise, costs, and complexity (as discussed below), “yield an unappetizing combination” which “supports [a] ... finding of no motivation to combine.” *See Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1332 (Fed. Cir. 2019).

Petitioner relies on a single prior art reference, Beauchamp, to argue that a POSITA would have used bonding wire due to their “low resistance connection.” Pet. 50. But the “low resistance” connections referred to Beauchamp are inapposite: they involve the connection between “the bond pad 104 and the ball at the end of the bond wire 110,” not the connection between pads or to a common ESD bus. Beauchamp (Ex.1016) [0027]; Foty Dep. 118:9-22; Khatri2 ¶83. As such, this “connection” with “low resistance” is not an improvement or advantage over other connection methods because it refers just to the contact resistance between ball and pad, not the complete resistance in the connection between pads. Khatri2 ¶83.

Third, lacking a reason why a POSITA would have chosen to replace Yoshinaga's connections with bonding wire, Petitioner instead offers a conclusory argument that "an obvious way to connect Yoshinaga's reference potential lines ... is by wire bonding the pads connected to the respective buses." Pet. 35. But the fact that bond wires were well-known does not mean that a POSITA would have been motivated to use them in this specific manner—especially in view of Yoshinaga's teachings of other connections. *Adidas AG v. Nike, Inc.*, 963 F.3d 1355, 1359 (Fed. Cir. 2020) ("The obviousness inquiry does not merely ask whether a skilled artisan could combine the references, but instead asks whether 'they would have been motivated to do so.'"); *see also Forest Laboratories, LLC v. Sigmapharm Laboratories, LLC*, 918 F.3d 928, 934 (Fed. Cir. 2019) ("[a]n invention is not obvious simply because all of the claimed limitations were known in the prior art at the time of the invention. Instead, we ask 'whether there is a reason, suggestion, or motivation in the prior art that would lead one of ordinary skill in the art to combine the references, and that would also suggest a reasonable likelihood of success'").

Further, to the extent Petitioner relies on an "obvious to try" argument, it fails to provide any support that: (1) "the possible options skilled artisans would have encountered were 'finite,' 'small,' or 'easily traversed;'" or (2) "that skilled artisans would have had a reason to select the route that produced the claimed invention." *In re Cyclobenzaprine Hydrochloride Extended-Release Capsule Pat. Litig.*, 676 F.3d

1063, 1072 (Fed. Cir. 2012); Khatri2 ¶¶82-85. To the contrary, as discussed below, a POSITA would not have selected the bonding wire because it adds noise, unnecessary complexity, and cost to Yoshinaga's chip. *See also Virtek Vision Int'l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 887-88 (Fed. Cir. 2024) (reversing the Board's obviousness determination when "[t]here was no evidence that there are a finite number of identified, predictable solutions" nor "a reason for combining" the "known" element into the prior art)

Fourth, Petitioner's modification to add bonding wires to connect reference potential pads 5 and 6 in Yoshinaga is redundant as these pads are already connected, as described above. Khatri2 ¶¶73-77, 89-92. Connecting reference potential pads 5 and 6 through bonding wire would have been redundant and would have added unnecessary components, parasitics (and associated noise), and complexity. *Id.* ¶¶73, 85-92; Signal Consulting (Ex.2014) 3. As Petitioner's expert confirmed, it is "standard practice to add components **only** when they are necessary for the design's function." Foty Dep. 72:1-11; *see Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1368-69 (Fed. Cir. 2012) ("[B]oth of these references independently accomplish similar functions ... [b]ecause each device independently operates effectively, a person having ordinary skill in the art ... would have no reason to combine the features of both devices into a single device.).

Finally, all three of Petitioner's Grounds argue there is a motivation to combine because Yoshinaga, Saint, and/or Haralabidis purportedly are "analogous art" that "address similar concepts and issues." Pet. 48-49,66, 96-97. But the purported fact that prior art falls "within the same alleged field ... without more, is not enough for [Petitioner] to meet its burden of presenting a sufficient rationale to support an obviousness conclusion." *See Securus Techs., Inc. v. Glob. Tel*Link Corp.*, 701 F. App'x 971, 977 (Fed. Cir. 2017); *Microsoft Corp. v. Enfish, LLC*, 662 F. App'x 981, 990 (Fed. Cir. 2016) (finding no motivation to combine when "references were directed to the same art or same techniques").

2. POSITAs would not have been motivated to modify Yoshinaga to use bonding wire connections between reference lines

Moreover, a POSITA would not have been motivated to use bonding wire to connect potential reference lines for at least two reasons.

First, doing so would have increased the noise in the circuit. But Yoshinaga emphasizes the importance of reducing noise—indeed, Petitioner admits that "Yoshinaga noted the need to 'prevent noise' that may impede IC circuit operation." Pet. 49. Yoshinaga teaches connecting "[t]he reference potential lines" "by bidirectional diodes that are connected in parallel to one another in the opposite direction *to avoid noise*." Yoshinaga [0005]; *see also id.* Fig. 3.

But bonding wire includes inductive parasitics which *increase* noise due to changing current flow through the bonding wire. See Khatri2 ¶¶73, 86-88; Davis (Ex.2012) 200 (“because of severe IR-drop and *switching noise problems, conventional wire-bonding technology is not a scalable concept* for deep submicron technology”), 296 (“Numerous problems developed with the perimeter I/O and wire bonded packages”); Foty Dep. 111:8-112:9. Miller, one of the three references Petitioner cites regarding use of bonding wire to connect pads, teaches “bond wire ... contribute[s] most of the series inductance,” and that while the “inductance of bond wires ... can be minimized by keeping them as small as possible,” “some level of signal distortion and attenuation is inevitable when signal frequencies are sufficiently high.” Miller (Ex.1014) [0007]. Thus, POSITAs would have understood that by introducing bond wire connections into Yoshinaga’s circuit, the noise in the circuit would have been increased, contrary to Yoshinaga’s teachings. Khatri2 ¶¶86-88.

A POSITA would have recognized that using bonding wire with Yoshinaga instead of the connections already described in Yoshinaga (via diodes or integrated circuit metallization wire) would result in comparatively (1) increased noise (both the diode and on-chip integrated circuit metallization wire are less inductive than bond wires) (Khatri2 ¶88; Signal Consulting 3), (2) reduced protection due to exposure of the bonding wires to the elements across “extra space,” and (3) increased

reliability issues because the bonding wire is more prone to sagging or drooping, which can “caus[e] a short in the circuit.” Saint 195; Khatri2 ¶¶90-94. Thus, a POSITA would not have been motivated to use bonding wire to connect pads in Yoshinaga. Khatri2 ¶¶86-95.

Second, Saint's teachings would have discouraged POSITAs from using bonding wire to connect pads. Indeed, Saint teaches using bonding wires only when there is “minimal silicon overlap” and does not mention using them to connect pads. Saint 195. It cautions that “the bond wire could sag or droop, causing a short in the circuit,” and therefore, “you have to keep the overlap of the bond wire over the unused silicon as short as possible.” *Id.* Thus, Saint would discourage a POSITA from intentionally designing the bonding wire to completely overlap with active circuits (which are what Petitioner purports to be “saved areas” depicted in orange) as suggested by the Petitioner. Khatri2 ¶¶78-81. Petitioner does not explain why a POSITA would disregard Saint's teachings and use bonding wires over active circuits in the saved areas. Nor does Petitioner argue or identify any reason that the space the bonding wire would span over unused silicon in its modified Yoshinaga Figure 6 would be minimal.

C. Petitioner fails to show that “one saved area,” as claimed in claims 6-7, 12, and 14 would have been obvious in view of Yoshinaga, Saint, and knowledge of a POSITA

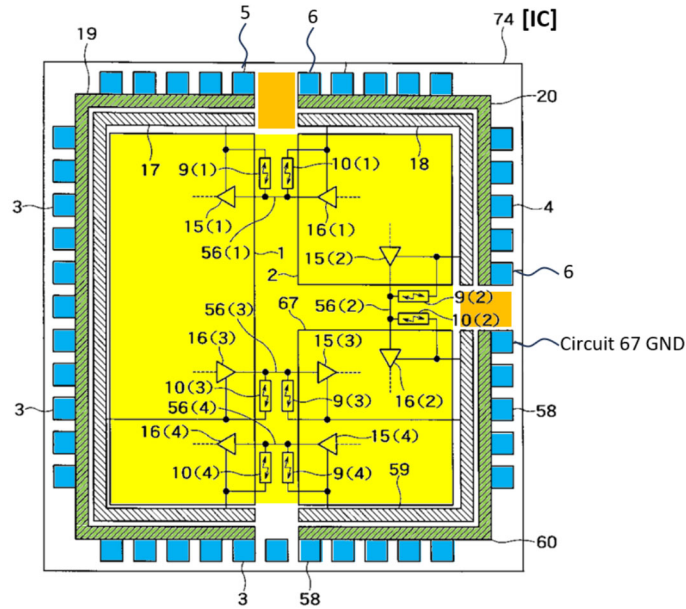
Each of the Challenged Claims recites:

wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

'164 Patent cls. 6, 7, 12, 14. Petitioner fails to establish the prior art teaches or renders obvious the claimed “saved area.”

1. Yoshinaga fails to disclose the claimed “saved area”

Petitioner argues (pointing to its redrawn version of Yoshinaga's Figure 6) that “Yoshinaga Fig. 6 discloses several spaces (each a saved area, orange) adjacent to ‘reference potential lines 19, 20, and 60,’ (ESD buses, green), and adjacent to two pad groups (two respective pad groups, blue).” Pet. 40. Petitioner is wrong for several reasons.



Pet. 40.

First, Petitioner fails to establish—or even allege—that Yoshinaga discloses that “the circuit area comprises at least one saved area” as required by each Challenged Claim. ’164 Patent cls. 6, 7, 12, 14. Indeed, Petitioner entirely ignores the requirement that the claimed “saved area” must be within the circuit area, failing to show—or even assert—that the alleged saved area is within the circuit area. To the contrary, Petitioner identifies the claimed “circuit area” as the area it highlights in yellow in its redrawn version of Yoshinaga’s Figure 6, reproduced above. *See, e.g.*, Pet. 27-28. In contrast, it identifies the orange areas as the alleged “saved areas,” but these orange (“saved”) areas that are expressly **not** included in Petitioner’s yellow (“circuit”) area. *Id.* 27-28, 39-41.

Further, Petitioner's purported "saved areas" are not included in circuit areas that Yoshinaga expressly describes, namely "circuit 1, circuit 2, and circuit 67." Yoshinaga [0075]. Petitioner does not identify any disclosure in Yoshinaga that suggests the purported "saved area" between the pads can contain circuitry and be part of the circuit area. No such disclosure exists. Khatri2 ¶¶96-99.

Instead, Petitioner relies on conclusory expert testimony that additional circuitry can be placed in the area between the pads. Pet. 19, 39; Ex.1003 ¶158. That is not enough to establish disclosure of a "circuit area" that "comprises at least one saved space" in Yoshinaga. *See, e.g., Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) ("[Petitioner's] expert testimony in support of this theory is equally unavailing, adding nothing beyond the conclusory statements in [the] petition."). Indeed, POSITAs would have understood that the areas highlighted in orange on Yoshinaga's Figure 6 were likely not part of the circuit area. Khatri2 ¶99. In fact, the orange areas identified by Petitioner are not part of circuit areas 1, 2 and 67 taught by Yoshinaga and are not described as being contained in any circuit area. *Id.*

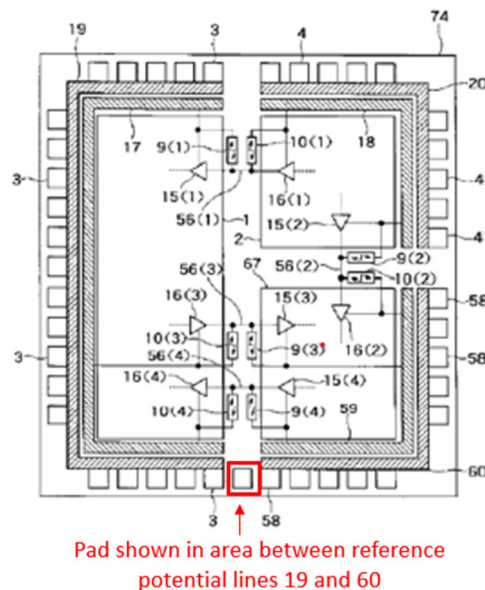
Second, even if *arguendo* Petitioner had asserted or shown that its alleged saved spaces were in the circuit area (it did not), Petitioner assumes, without support, that those spaces do not include a pad. Petitioner ignores that in Yoshinaga Figure 6, "[r]eference potential pads are not shown to simplify the drawing." Yoshinaga

[0078]. In fact, reference potential pads could and likely would be found in Petitioner's purported "saved areas" due to the limited space available for reference potential pads shown in Figure 6. Khatri2 ¶¶100-106. There are only 10 potential locations for these reference potential pads in Yoshinaga Figure 6, and the most probable locations are the two "saved spaces" identified by the Petitioner. *Id.* ¶¶102-106. Petitioner's expert admitted that Yoshinaga is "silent" on "whether you could have reference potential pads in the space between power supply pads 3 and 4" and that Yoshinaga imposes "no particular restriction where you would put those pads." Foty Dep. 143:17-144:10, 145:1-5.

As shown in Yoshinaga Figure 6, the existence of a space between circuits or reference potential lines does not mean no pad or ESD bus is present. To the contrary, Figure 6 of Yoshinaga identifies a pad in such a location (as shown in annotated Figure 6 below). Khatri2 ¶¶105-106. Given that reference supply pads are not illustrated in Figure 6 at all,⁶ Yoshinaga does not disclose nor suggest that the

⁶ The unlabeled pads in Figure 6 of Yoshinaga would not be considered to be reference potential pads because Yoshinaga teaches that "reference potential pads *are not shown* to simplify the drawing." Yoshinaga [0078]. And since they are not labeled as power supply pads either, the unlabeled pads would be understood to be another type of pad. Khatri2 ¶¶44, 101.

areas identified by Petitioner as “saved spaces” have “no pads” in them. Meanwhile, Figures 1-4 are “simply ... topological depiction[s]” that “ha[ve] nothing to do with any physical location of anything,” and thus do not show whether there is saved area without an ESD bus and pad. *Foty Dep.* 168:14-170:6; *Khatri2* ¶104. Thus Petitioner fails to establish that Yoshinaga discloses the claimed “one saved area.”



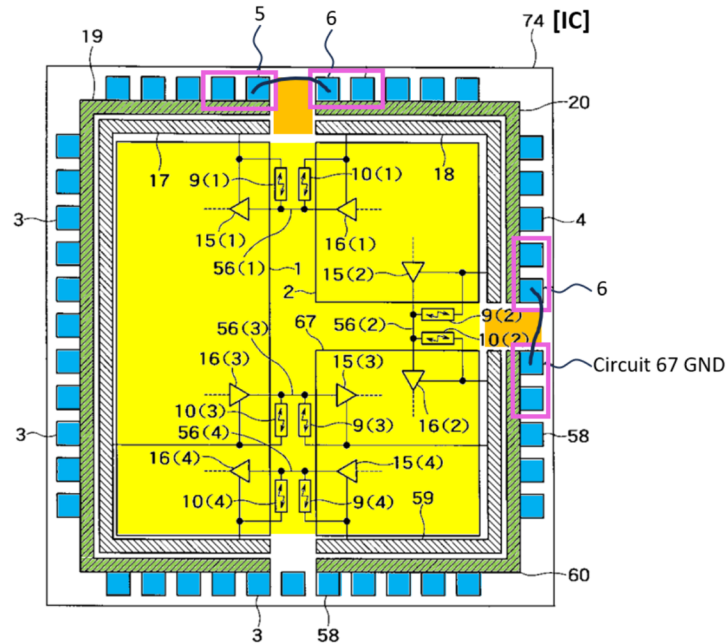
2. Petitioner fails to establish that a POSITA would have been motivated to combine Yoshinaga with Saint and knowledge of a POSITA to form the claimed “one saved area”

Petitioner fails to establish why a POSITA would have been motivated to include “one saved area” as required by claims 6 and 12 in Figure 6 of Yoshinaga for three reasons.

First, Petitioner fails to identify any teachings in Yoshinaga or Saint about forming a “saved space” that is both “adjacent to two respective ESD buses and

respective pads of two respective pad groups” and has “no ESD bus and no pad.” Yoshinaga is completely silent about an area without pads and says nothing about the spacing of pads, especially the reference potential pads. Yoshinaga [0078]; Foty Dep. 145:1-5. Likewise, nothing in Saint suggests forming the claimed saved area. At most, Saint teaches that to avoid “wasted space around the edges between the pads ... you can push some of your circuitry into this wasted space to try to use those gaps.” Pet. 40-41; Saint 206-07. But Saint only addresses what to do with wasted space—it provides no motivation to create such a space, let alone to create a saved area as claimed with no pads or ESD buses that is also adjacent to ESD buses and pads. Khatri2 ¶¶107-109; *infra* Section V.C. In fact, Saint teaches away from creating such a space, since it teaches “trying to get the chip as small as possible.” Saint 207; Khatri2 ¶108. Creating a “saved space” adjacent to two respective pad groups with no pads or ESD buses would require increasing the size of the chip in Yoshinaga so that pads and ESD buses where the “saved space” is being created could be included elsewhere. Khatri2 ¶107. Petitioner identifies no other art disclosing the claimed “saved area,” or providing a motivation to create such an area.

Second, Petitioner premises its arguments on adding a bonding wire such that it extends over a space between the added reference potential pads 5 and 6 and reference potential pad 6 and reference potential line Circuit 67 GND, as shown below.



But Petitioner's proposed changes contradict each other. On one hand, if a POSITA created a saved space without a pad or ESD bus (as Petitioner argues), she would not have used bonding wire to connect the pads. POSITAs would have understood that bonding wire should be kept as short as possible to decrease the chance of a short circuit and reduce voltage drops. Saint 195 ("keep the overlap of the bond wire over unused silicon as short as possible" because "the bond wire could sag or droop, causing a short in the circuit"); Dubey 2 ("length of the power and ground connecting bond wires ... and therefore their resistance is determined by where these pads are placed on-die and therefore IR drop on package can be reasonably minimized by optimum pad placement"); Khatri2 ¶81. But running bonding wire over a saved space would have required a long bonding wire and risked a short circuit and voltage drop. As such, POSITAs would have looked to another

option to connect pads on opposite sides of a saved space. *Id.* On the other hand, if a POSITA wanted to connect pads using bonding wire (as Petitioner also argues), it would avoid adding space, because doing so would require a longer bonding wire, thereby increasing risk of a short-circuit and voltage drop. *Id.* These two goals are in contradiction and further confirm the Petitioner's hindsight.

Third, Petitioner argues that creating a “saved space”⁷ would be obvious “to obtain a smaller chip/die and increase profits by fitting more chips on each wafer.” Pet. 41. That is incorrect. Yoshinaga teaches Figure 6 already “keep[s] the chip size as small as possible.” Yoshinaga [0084]. As such, a POSITA would understand that the chip is already as small as possible and thus there would be no empty space to utilize between pads and ESD buses. Khatri2 ¶107. Saint similarly focuses on “trying to get the chip as small as possible.” Saint 207. But adding or forming a “saved area” with no pads or ESD buses to Yoshinaga Figure 6 would increase the size of the chip, not decrease it, because a POSITA would need additional space to reinstate the pads removed to create the “saved area.” Khatri2 ¶107. Petitioner provides no other reason a POSITA would want to add such a space to Yoshinaga since it would make the circuit bigger and more costly. *Id.* ¶¶107-109.

⁷ The Petition refers to “saved area” and “saved space” interchangeably. Pet. 41.

IV. Ground 2 Petitioner fails to demonstrate that Yoshinaga, Saint, Haralabidis and knowledge of a POSITA would render obvious claims 1-6, 8-11, and 13

Petitioner relies on many of the same arguments it raised in Ground 1 for Ground 2, adding Haralabidis for the disclosure of additional limitations reciting a “common ESD bus.” ’164 Patent cls. 1-6, 8-11, and 13. But Petitioner’s Ground 2 arguments fail to correct the deficiencies of Ground 1 and, its added secondary reference, Haralabidis, fails to teach or render obvious “connecting” the “pad groups” to the “common ESD bus” by “bonding wires” as required by claims 1-5, 8-11, and 13.

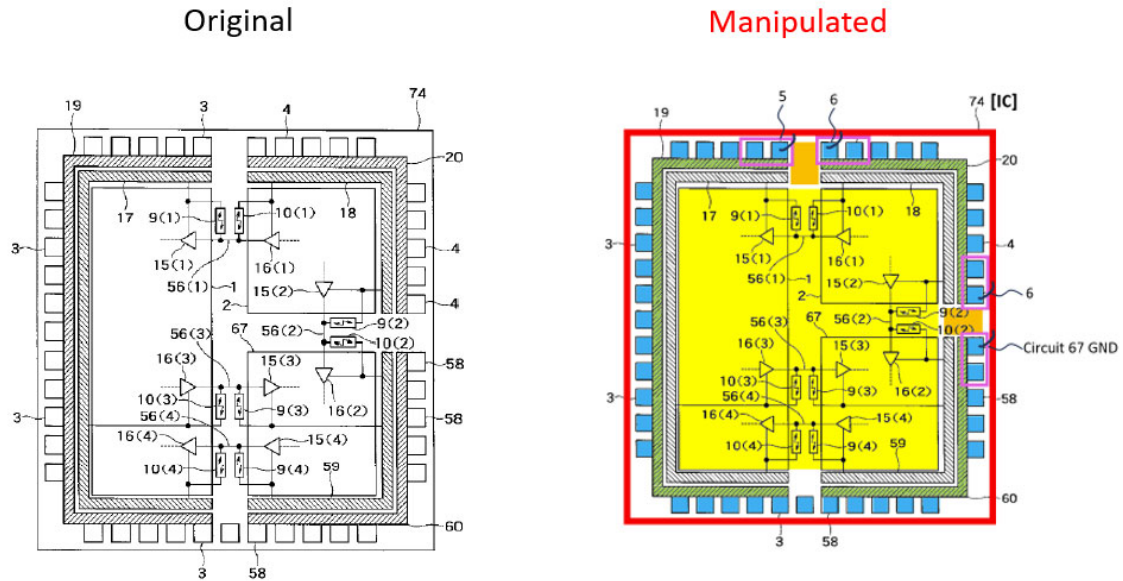
A. Petitioner fails to show that Yoshinaga, Saint, Haralabidis, and the knowledge of a POSITA would have rendered obvious “a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus” and “connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires”

Claims 1-5, 8-11 of Ground 2 each recite “a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus” (claims 1-5), and “connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires” (claims 8-11).⁸

⁸ Claim 6 does not recite using “bonding wires” to connect pad groups to a “common ESD bus.” Yet Petitioner asserts, with no explanation, that “Element [1.D] applies Haralabidis’ common ESD bus approach” and “[t]his same configuration meets

Petitioner acknowledges that Yoshinaga does not disclose “bonding wires.” Pet 34-35. It also acknowledges that Yoshinaga does not disclose a “common ESD bus.” *Id.* 52-53. However, Petitioner argues that Yoshinaga combined with Saint and Haralabidis renders using “bonding wires” to connect a “plurality of pad groups” to a “common ESD bus” obvious. *Id.* 56. To support this argument, Petitioner redraws Yoshinaga’s Figure 6 again. As discussed in Ground 1, Petitioner first changes Yoshinaga’s power supply pads 3, 4, and 58 into “reference potential pads” 5, 6, and “Circuit 67 GND.” *Supra* Section III.A. Petitioner next adds a “common bus” (red) and “wire bonds” to “connect pad groups (via respective pads) to the common bus.” Pet. 57-58.

[6.D] under PO’s overly broad interpretation.” Pet. 63. Petitioner appears to treat element [1.D] identically as [6.D], and therefore, Petitioner’s assertions as to claim 6 fail for the same reasons discussed for claim 1.



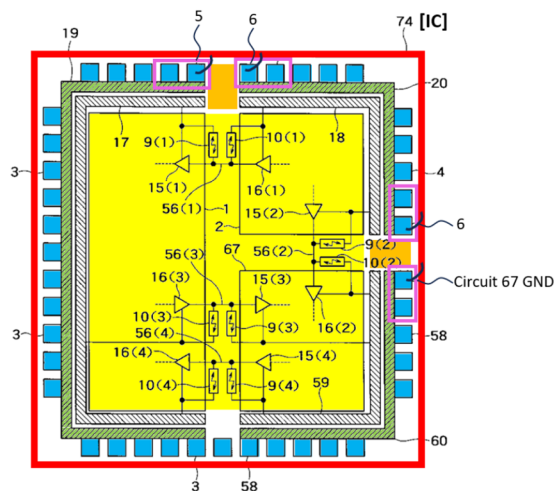
As explained below, these modifications, both by themselves and together, constitute impermissible hindsight.

1. **Petitioner fails to show that a “plurality of pad groups” “adjacent and connected to the plurality of ESD buses,” as claimed in claims 1-6, 8-11, and 13 would have been obvious in view of Yoshinaga, Saint, Haralabidis and knowledge of a POSITA**

Petitioner's obviousness arguments regarding limitations [1.C], [6.C], [8.C] and [12.C] are identical to their arguments made for limitations [6.C] and [12.C] in Ground 1. Pet. 55, 63. As such, they fail for the same reasons discussed above because they do not disclose or render obvious the claimed “plurality of pad groups” “adjacent and connected to the plurality of ESD buses.” *Supra* Section III.A. Indeed, Haralabidis is “completely silent” about “bond pads themselves” (Foty Dep. 243:9-11, 244:4-15), and thus does not alter the obviousness analysis. Khatri2 ¶110.

2. POSITAs would not have been motivated to connect a “plurality of pad groups” to a “common ESD bus” with “bonding wires”

Petitioner agrees that none of the Ground 2 references disclose connecting “a plurality of pad groups” to a “common ESD bus” using “bonding wires.” Per Petitioner’s expert, “Yoshinaga[] doesn’t go beyond the pads, so [Yoshinaga] has to be combined with another reference to get” “using bonding wire to connect reference pads to the common ground rails.” Foty Dep. 131:1-7, 136:5-137:1. Meanwhile, Saint is silent about connecting a common ESD to reference pads as discussed above. *Supra* Section III.B. And Haralabidis “does not disclose bond pads” and is “silent on the method used to connect from the inside the IC of the package substrate.” Foty Dep. 243:9-11, 244:4-15. Thus, Haralabidis also does not disclose connecting bond pads to a common ESD bus using bonding wire. Khatri2 ¶118.



Because none of its prior art references teach this limitation, Petitioner instead cherry-picks elements from each reference to argue that Yoshinaga combined with

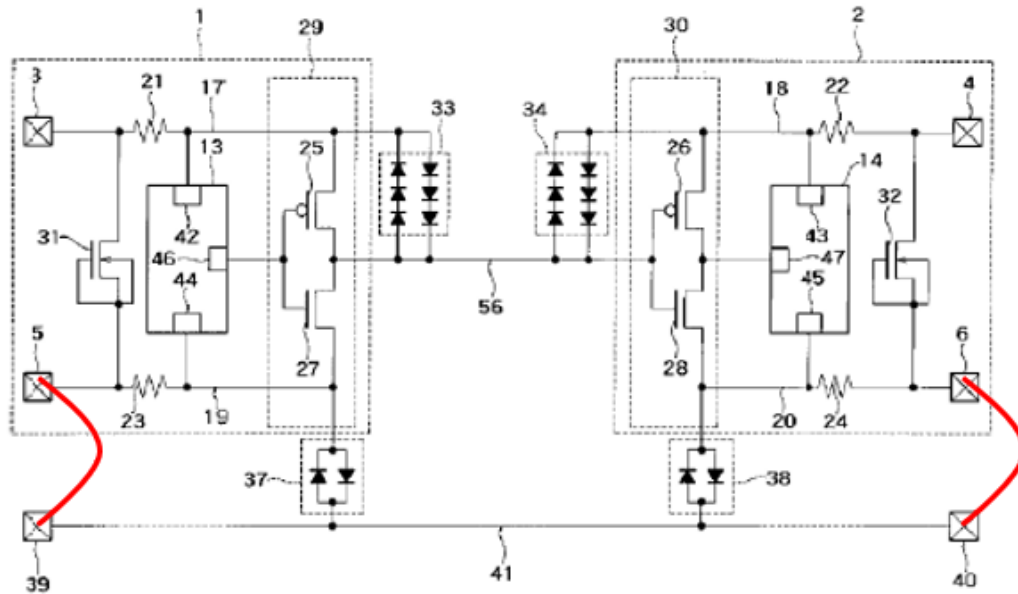
Haralabidis' "common ground rail 360" and "bond wires" from Saint and the knowledge of a POSITA (as shown in the modified Figure 6 below), renders obvious connecting a "plurality of pad groups" to a "common ESD bus." Pet. 56-58. Petitioner is wrong for several reasons.

First, Petitioner asserts that Yoshinaga "does not teach any specific connection technique/implementation" for connecting the reference voltage lines. *Id.* 52, 66-67. That is incorrect. As explained above, Yoshinaga teaches specific connections for its reference voltage lines. *See supra* Section III.B.1. Notably, Yoshinaga's Figure 3 depicts and teaches connecting reference potential lines 19 and 20 to a "third reference potential line" 41 (such as the alleged "common ESD bus" of Haralabidis in Petitioner's proposed combination) "via a bidirectional diode pair 37 and a bidirectional diode pair 38." Yoshinaga [0061], Fig. 3. Petitioner asserts that the "ESD circuitry and connections" of Figure 3 apply to the layout shown in Figure 6 and Petitioner's own expert admits that "Yoshinaga combines these disclosures [including those regarding Figure 3] into an IC embodiment in Figure 6." Pet. 22; Ex.1003 ¶76; Foty Dep. 160:10-161:2.

Petitioner provides no reason why a POSITA would have looked to other references like Saint or Haralabidis to connect reference potential lines 19 and 20 in view of Yoshinaga's disclosure. Yoshinaga [0005], [0061]; Foty Dep. 175:1-9. Petitioner identifies no drawback in Yoshinaga's specific scheme for connecting the

reference voltage lines that would motivate a POSITA to seek any modifications. Nor has Petitioner articulated any advantage of the proposed modification over Yoshinaga's specific scheme for connecting the reference voltage lines. To the contrary, as discussed above, replacing Yoshinaga's bidirectional diodes with bonding wire would increase noise, negatively impacting the operation of the circuit. *Supra* Section III.B; Khatri2 ¶¶112-115. Moreover, Petitioner's proposed combination fails to meet the "obvious to try" requirements for the reasons discussed in Ground 1. *Supra* Section III.B.1.

Second, Petitioner's proposed modification is redundant because it burdens Yoshinaga's circuit with additional and unnecessary components, parasitics, and complexity. As explained, Yoshinaga already teaches connection using circuit elements 37 and 38 to a third reference potential line using a different method that already reduces noise, namely using bidirectional diodes. Yoshinaga Fig. 3, [0061]; Foty Dep. 172:19-21; Khatri2 ¶¶112-115. Petitioner's proposed manipulation requires adding bonding wires (shown in red) between the reference potential pads 5 and 6 to a common reference potential line. Pet. 56-58. This modification of adding bonding wires (red) is shown in the below modified Yoshinaga Figure 3.



Petitioner provides no reason why a POSITA would allegedly disregard Yoshinaga's teachings in favor of bonding wire, particularly because replacing the diodes with bonding wire would increase noise due to both the removal or inactivation of the diodes (which remove noise) and the usage of bonding wire (which increases noise). *Supra* Section III.B. Indeed, a POSITA would not have been motivated to endure the extra expense, complexities, and noise associated with adding bonding wire. Khatri2 ¶¶90-94, 112-119.

Third, Petitioner argues that a "POSITA would have been motivated to use Haralabidis' common ground rail teaching to 'ensure a solid return path for ESD protection' and 'achieve Yoshinaga's goal of improve[d] ESD protection.'" Pet. 66-67. That is incorrect. Yoshinaga already has sufficient ESD protection and Petitioner does not provide any reason why it would need more. Yoshinaga's Figure 3 provides

ESD protection by connecting reference potential lines 19 and 20 to circuit elements 37 and 38 through a third reference potential line 41. *Id.*; Khatri2 ¶¶112-115; Yoshinaga Fig. 3, [0061] (describing using reference potential line 41 “as a discharge path” for ESD events). In addition, “one of the major features” of Yoshinaga are ESD protective elements 9 and 10. Yoshinaga [0084]. Those protective elements 9 and 10 “are provided in the chip interior” and are “small,” making it “possible to greatly improve the ESD resistance while keeping the chip size as small as possible.” *Id.* The Petition does not describe why either of these ESD protections are insufficient or why a POSITA would add an additional common ground rail (making the chip larger) when Yoshinaga’s chip is “as small as possible” while providing ESD protection. Khatri2 ¶¶112-116; Yoshinaga [0084]. Therefore, a POSITA would not be motivated to use Haralabidis’ common ground rail with Yoshinaga, since Yoshinaga’s ESD protection is already efficient and adequate, and adding Haralabidis’ common ground rail would increase chip size, noise, and complexity. Khatri2 ¶¶114-116.

Finally, Petitioner is wrong to argue “POSITA would have had a reasonable expectation of success combining Haralabidis’ common reference voltage teachings with Yoshinaga and Saint’s reference voltage lines” merely because “Haralabidis expressly states its Fig. 3 (and 4) common ESD ground ring was ‘conventional art.’”

Pet. 67. “[V]ery well known” features “alone do[] not demonstrate a reasonable expectation of success.” *See Juniper Networks*, 2024 WL 3517862, at *5 n.3.

Haralabidis does not discuss pads while Yoshinaga and Saint both do not discuss connecting pads to a common ESD bus using bond wire. Khatri2 ¶¶111, 117-119. As such, Petitioner points to **zero** disclosure in the prior art where pads are connected to a common ESD bus using bonding wires. Instead, Petitioner clings onto unsupported conclusory expert testimony to salvage its obviousness argument. Pet. 67. But “[g]eneral and conclusory testimony ... does not suffice as substantial evidence” of obviousness. *Juniper Networks*, 2024 WL 3517862, at *6 (citing *Koito Mfg. Co.*, 381 F.3d at 1152).

3. Petitioner fails to show that “one saved area,” as claimed in claims 1-6, 8-11, and 13 would have been obvious in view of Yoshinaga, Saint, Haralabidis and knowledge of a POSITA

Petitioner's obviousness arguments regarding limitations [1.F], [6.E], [8.F] and [12.E] in Ground 2 are identical to their arguments made for limitations [6.E] and [12.E] in Ground 1. Pet. 55, 63. As such, they fail for the same reasons discussed above. *See supra* Section III.C. Indeed, Haralabidis does not explicitly disclose a saved area at all and thus does not alter the obviousness analysis. Khatri2 ¶120.

B. Claim 13 is not obvious in view of Yoshinaga, Saint, Haralabidis, and knowledge of a POSITA for the same reasons discussed regarding Ground 1

As explained above, Yoshinaga in view of Saint and POSITA knowledge do not render obvious claim 12. Claim 13 depends from claim 12 and recites “a common ESD bus ... parallel to the plurality of ESD buses and the plurality of pad groups.” As explained above, Yoshinaga in view of Saint and POSITA knowledge do not render obvious claim,12. Petitioner alleges only that Haralabidis discloses claim 13’s additional “common ESD bus” limitation but does not correct any of the deficiencies in its proposed combination’s disclosure of claim 12. Thus, Petitioner fails to meet its burden to establish that claim 13 is obvious for the same reasons discussed above with respect to Ground 1, i.e., Yoshinaga, Saint, Haralabidis, and POSITA knowledge fail to render obvious “connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires,” as claim 12 requires.

V. Ground 3: Petitioner fails to demonstrate that Saint, Haralabidis, and knowledge of a POSITA would render obvious claims 1-14

Petitioner's Ground 3 is based on cobbling together discrete, cherry-picked disclosures from the Saint textbook and Haralabidis, and then redrawing and manipulating Figure 7-7⁹ in Saint as shown the Figure below:

⁹ Petitioner argues that “[t]his Ground relies on a set of teachings (primarily from Saint) applied to Saint’s IC in Fig. 7-7, but the results are the same if Saint’s IC in Fig. 9-21 is used as the baseline.” Pet. 68. However, the Petitioner only refers to Saint Figure 9-21 in Ground 3 concerning the preamble (found in each independent claim), the “saved space” limitation (found in each independent claim), “a circuit area” (found in each independent claim), and claim 13—and none of the other limitations. *Id.* 68-69, 94; Khatri2 ¶132. Thus, the Petitioner has not demonstrated the obviousness of the challenged claims based on Saint Figure 9-21, for this reason and the same reasons discussed regarding Saint Figure 7-7. Khatri2 ¶132.

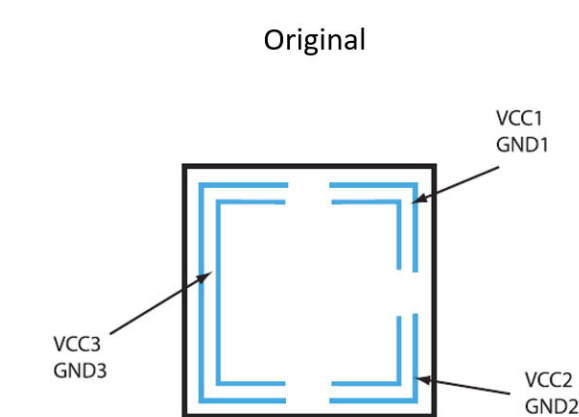


Figure 7-7. Pin-out simplification showing like protects grouped together.

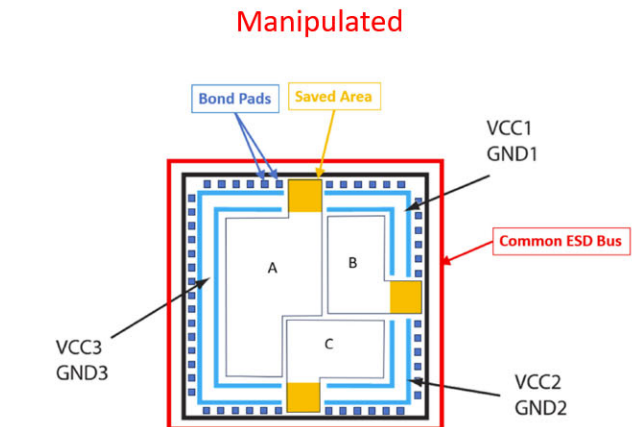


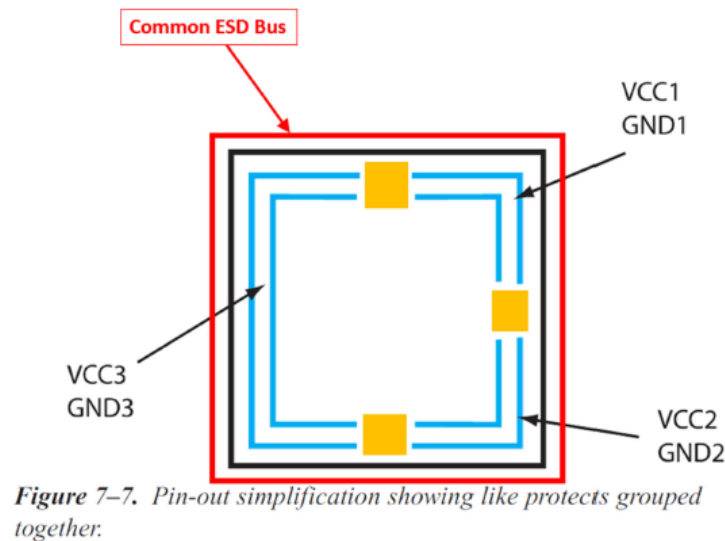
Figure 7-7. Pin-out simplification showing like protects grouped together.

As shown in the figures above, Petitioner makes several changes to Saint, adding (1) pads (shown as squares on the outside of the blue VCC and GND lines), (2) a common ground rail (in red), and (3) circuit blocks A, B and C. Pet. 83. Further, Petitioner also modifies Saint Figure 7-7 by connecting the common reference line (red box) to the reference potential pads (labeled in blue) using bonding wire (not labeled). *Id.* 78-79.

Petitioner's manipulations of Figure 7-7 are based on a fundamental misunderstanding of Saint and fail for three reasons. Saint in view of Haralabidis and knowledge of a POSITA does not teach and would not have rendered obvious: (1) a "plurality of pad groups" "adjacent and connected to the plurality of ESD buses;" (2) "connecting" the "pad groups" by "bonding wires;" or (3) "one saved area," as is required by claims 1-14.

A. Petitioner fails to show that Saint, Haralabidis, and the knowledge of a POSITA discloses or renders obvious “a common ESD bus” (claims 1-5, 8-11)

Claims 1-5 and 8-11 require “a common ESD bus, adjacent to the plurality of pad groups.” Petitioner asserts, “[a]pplying either Saint’s ‘ESD Ground Wiring’ or Haralabidis’ common ground rail teachings” renders obvious a “common ESD bus” as shown in Petitioner’s modified version of Figure 7-7 from Saint. Pet. 76-77. But, in its Institution Decision, the Board properly “question[ed] whether a POSITA would have been motivated to apply Saint’s ‘ESD Ground Wiring’ or Haralabidis’ common ground rail teachings to Saint’s Figure 7-7 with a reasonable expectation of success.” ID 34. The answer is a resounding no for at least the following reasons.



First, Petitioner ignores the actual disclosures regarding Saint Figure 7-7. Saint’s Figure 7-7 discloses the use of three separate and distinct ground signals—GND1, GND2, and GND3—not a “common ESD bus” as required by the challenged

claims. Saint 145-47. These three separate ground signals—GND1, GND 2, GND3—each separately protect one of three groups of pins, with each group of pins having separate and distinct ESD protection. *Id.* Figs. 7-3, 7-4, 7-5. Saint does not teach nor contemplate shorting together these three distinct ground signals as Petitioner proposes, let alone using a “common ESD bus” to do so. *Id.* 145-147. To the contrary, POSITAs would have understood that the three separate signals GND1, GND2, and GND3 should **not** be connected together as Petitioner proposes. Khatri2 ¶¶121-126.

Petitioner argues a POSITA would add “Haralabidis’ common package or common PCB ground rail approach to provide robust ESD protection and noise suppression/immunity for Saint’s IC in Fig. 7-7.” Pet. 98. That is incorrect. Saint does not teach, as Petitioner suggests, connecting the different GND1, GND2, and GND3 signals in the layout of Figure 7-7, nor does it consider using a “common ESD bus” for ESD protection and noise suppression. Instead, Saint Figure 7-7 teaches three separate GND signals conducted by three separate GND wires, which fundamentally contradicts Petitioner’s characterization of Saint. Foty Dep. 228:14-230:4; Khatri2 ¶¶123-126. To be clear, Saint teaches that the three separate signals GND1, GND2, and GND3 should remain unconnected to each other to prevent noise and maintain ESD protection. Saint 147; Khatri2 ¶¶123-128. By shorting GND1/VCC1, GND2/VCC2, and GND3/VCC3 to a common ground rail (as

Petitioner proposes), noise is injected from one circuit to another. Khatri2 ¶128. As such, Petitioner's modification of Saint 7-7 would achieve the exact opposite of "robust ESD protection and noise suppression/immunity" as Petitioner claims. Pet. 98.

Second, Petitioner argues that "Saint discloses 'ESD Ground Wiring' that 'creates a continuous ring around the active circuitry' to which ESD diodes are connected," citing Figure CS1-99 from "Case Study 1" of the Saint textbook. *Id.* 85-86. But Case Study 1 is a completely separate embodiment from Saint Figure 7-7 with fundamentally incompatible teachings. For example, Case Study 1 incorporates only one "GND" signal and includes a single "continuous ring" that can be used as an "ESD Ground Wiring." Saint 249 (CS1-1), 332. CS1-99 does not disclose connecting the segmented ESD to the ESD ground wiring. *Id.* In contrast, in Saint's Figure 7-7, there are three *separate* ground signals: GND1, GND2, and GND3. Saint Fig. 7-7. Indeed, Petitioner's expert recognizes that Figure 7-7 depicts "a design where there are three separate power supply and **three separate ground lines**" while the design of Case Study 1 is "**not** using the three-ground-rails (which provide three ESD buses) configuration of the Chapter 7 design" and instead "use[s] a **single** ground rail." Ex.1003 ¶¶359-360. Petitioner provides no explanation for why or how a POSITA would have allegedly combined these two distinct—and incompatible—embodiments.

Petitioner asserts that a POSITA would have been motivated by Saint's "Case Study 1" to connect the three separate ground signals of Figure 7-7 together to a "common ESD bus." Pet. 75-77, 98. But connecting separate signals GND1, GND2, and GND3 of Saint Figure 7-7 together to a "common ESD ground" would result in noise injection and performance degradation, making it an undesirable design choice. Khatri2 ¶¶127-129. Petitioner's combination of cherry-picked embodiments without an adequate motivation to do so is legal error. *In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017) ("combining multiple embodiments in a single reference" requires "a motivation to make the combination").

Third, a POSITA would have understood Haralabidis' teachings of a "common ground rail" are inapplicable to Saint's Figure 7-7. Khatri2 ¶129. Haralabidis contemplates a single "segmented," ground signal, not three separate reference potentials. Haralabidis 3:9-22, 3:34-40, 3:65-4:12; Khatri2 ¶¶127-131. To be clear, Haralabidis' "common ground rail 360" connects the segmented—but common—ground signal together. It does not disclose or suggest using a "common ground rail" to connect together three *different* and separate ground signals, as in Saint Figure 7-7. Haralabidis 3:9-22, 3:34-40, 3:65-4:12; Khatri2 ¶129. Petitioner fails to address these fundamental differences and does not explain why a POSITA would have been motivated or reasonably expect success in modifying Saint 7-7's three separate GND signals to form a common ground rail.

Fourth, Petitioner alleges that “it was common practice to place ‘package common ground rail 360’ around an IC.” Pet. 75, 98. But that alone is insufficient to establish a motivation to combine or reasonable expectation of success. *Juniper Networks*, 2024 WL 3517862, at *5 n.3 (testimony that features was “very well known,” “alone does not demonstrate a reasonable expectation of success”); *Forest Laboratories*, 918 F.3d at 934 (requiring a motivation in prior art even when all claimed limitations were known).

Finally, Petitioner argues that a POSITA would “adapt Saint’s IC teachings to include Haralabidis’ package common ground rail 360’ (Figure 3) to further reduce die size and costs.” Pet. 97. That is incorrect. Adding an external common ground rail (and not removing VCC1/GND1, VCC2/GND2, and VCC3/GND3), would not reduce die size or costs. Khatri2 ¶130. To the contrary, die size and cost would increase due to the addition of both bonding wire and a common ground rail without removal of other components. *Id.*

B. Petitioner fails to show that “connecting” the “pad groups” to either “another of the plurality of pad groups” (claims 6-7, 12-14) or “to the common ESD bus” by “bonding wires,” (claims 1-5, 8-11) would have been obvious in view of Saint, Haralabidis, and knowledge of a POSITA

Petitioner argues that a POSITA would combine Saint’s Figure 7-7 with Haralabidis’ “common ground rail 360” and bonding wires from Saint to render

obvious connecting a “plurality of pad groups” together or to a “common ESD bus” with “bonding wire.” Pet. 74-77. That is wrong for three reasons.

First, Petitioner fails to identify any disclosures in Saint or Haralabidis disclosing the use of bonding wires to connect bond pads, as required by claims 6-7 and 12-14. Foty Dep. 107:7-19; Pet. 86. Petitioner's expert concedes that neither Saint nor Haralabidis describe this connection method. Foty Dep. 107:7-19, 133:21-134:14. Instead, Petitioner asserts that it was “well-known to use bond wires to connect other elements” within a chip. Pet. 86. However, as discussed in Ground 1, Petitioner fails to provide any reason why a POSITA would have allegedly used bonding wires. *Supra* Section III.B.¹⁰

Second, a POSITA would not have been motivated to modify Saint's Figure 7-7 to use bonding wire to connect pads to a “common ground rail” or other pads in view of Haralabidis. Khatri2 ¶¶117-118, 134-138. As an initial matter, Haralabidis does not disclose pads or their connection to a common ESD bus. Foty Dep. 243:9-244:15; Khatri2 ¶¶117-118, 135. And even if it did, a POSITA would not have been motivated to use the “common ground rail” connection of Haralabidis with Saint 7-

¹⁰ Petitioner and its expert rely on the same arguments for bonding wire connections in claims 6-7 and 12-14 as they do for claims 1-5 and 8-11, despite the former not requiring a connection to a “common ESD bus.” Pet. 86, 93.

7, since they serve different purposes. Saint's Figure 7-7 focuses on designing a chip with internal ESD buses (Khatri2 ¶131), while Haralabidis describes an entire "electronic device," with ESD buses external to the chip. Therefore, a POSITA would not have been motivated to look to Haralabidis' discussion of external ESD buses when Saint Figure 7-7 focuses on internal ESD buses. *Id.*

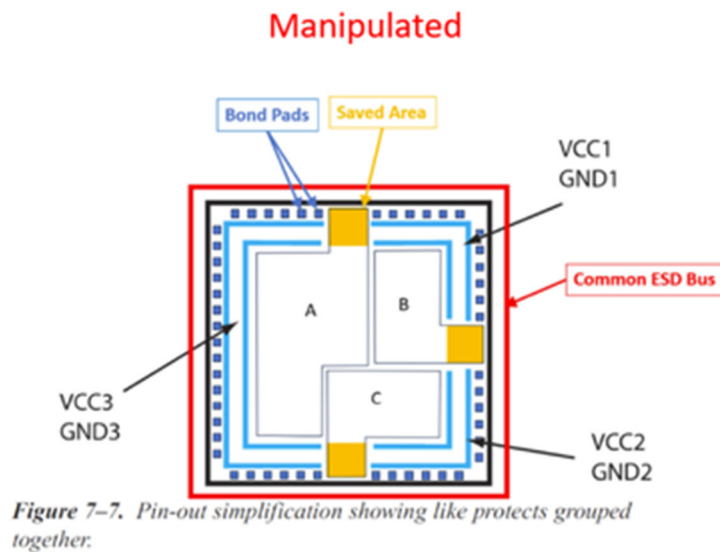
Third, Saint's disclosure would have lead POSITAs away from using bonding wire to connect reference potential pads to a common ESD bus or other reference potential pads, as discussed above in Section III.B.2. Notably, the Petitioner's references to bonding wire in Saint pertain to connecting chip pads with external pins during packaging, where direct connection is impossible since the package pins are outside the chip. Pet. 79; Khatri2 ¶¶79, 137-138. Saint never teaches using bonding wiring when integrated circuit mentalization based wiring is possible, such as with Saint's Figure 7-7. Khatri2 ¶¶79, 137.

C. Petitioner fails to show that "one saved area," as recited in claims 1-14 would have been obvious in view of Saint, Haralabidis and knowledge of a POSITA

Claims 1-14 each require "at least one saved area" where "each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area." '164 Patent cls. 1, 6, 8, 12. However, as Petitioner's expert admits, Saint's Figure 7-7 does not show nor

disclose the location of pads. Foty Dep. 222:12-223:5. Instead, Petitioner relies on “Saint and a POSITA’s knowledge” to assert that this limitation would have been obvious.¹¹ Pet. 80-83, 85-86, 92, 92-93. Petitioner is wrong for three reasons.

First, Saint Figure 7-7 is a pin-out simplification that does not show pads or their relative locations. Foty Dep. 222:12-223:5; Khatri2 ¶¶139-140. Thus, Figure 7-7 does not show a “saved area,” since it does not show pad locations. Despite this, Petitioner inserts pads into a manipulated Saint Figure 7-7 to show a purported “saved area.” Pet. 83.



¹¹ Petitioner does not cite any reference other than Saint for knowledge of a POSITA in its discussion of the “saved area” limitations. Pet. 80-83, 85-86, 92, 92-93.

But Saint's disclosures establish that Petitioner's added pads and alleged "saved spaces" are based on hindsight and that a POSITA would not have made the modifications it proposes. Khatri2 ¶¶139-150.

For instance, Petitioner adds 51 bond pads and identifies three alleged "saved areas" between bond pads in its modified version of Saint's Figure 7-7. Petitioner ignores the fact there are only 16 pins (which would be associated with 16 pads) in Saint's Figure 7-6, with no "saved area" between those pads. But Saint teaches that Figures 7-6 and 7-7 are related: Figure 7-6 shows the pins scattered about the chip where Figure 7-7 groups pins with common grounds together. Saint 145-47. Therefore, Figures 7-6 and 7-7 must both have the same 16 pins and pads. As another example of Petitioner's unsupported changes, while Figure 7-6 has the pins evenly spaced, Petitioner modifies Figure 7-7 to create additional "saved areas" between pads. But there is no basis for that. Even Petitioner's expert admits that Saint teaches having the pads "evenly spaced." Foty Dep. 206:1-16; Saint 147; Khatri2 ¶¶139-143.

Petitioner provides no reason why a POSITA would have understood there would be such a dramatic increase in the number of pads or why those pads would have a "saved area" between them in Figure 7-7. Khatri2 ¶¶139-149. At most, Petitioner's expert refers to an unrelated IC image not listed in the Grounds to suggest a similar pad structure in Figure 7-7. Ex.1003 ¶384. But he fails to provide

a valid reason for structuring pads in Saint Figure 7-7 in the same manner. Khatri2 ¶¶145-149.

Second, Petitioner's claim that a POSITA would have been motivated to form the "saved area" "to achieve the benefits of smaller chip size and ESD protection" is incorrect. Pet. 81. Saint's Figure 7-7 already offers ESD protection that "makes the chip smaller, keeps parasitics down, and keeps cross talk down from one supply to another." Saint 147; Khatri2 ¶¶134-142. Petitioner identifies no reason that Saint's ESD protection is insufficient. Khatri2 ¶¶134-142. Moreover, adding an area adjacent to pads without pads or an ESD bus to Saint Figure 7-7 would increase chip size, as additional space would be needed to reinsert the pads removed to create the "saved area." *Id.* ¶¶134-144, 149-150.

Third, while Saint suggests using "wasted space around the edges between the pads" for circuitry (Pet. 80 (citing Saint 220)), it does not address saving spaces between ESD buses or pad groups. Khatri2 ¶¶143-150. Nor does it describe why or how a POSITA would create a "saved area" both free of pads and ESD buses and adjacent to two ESD buses and two pad groups. *Id.* ¶¶143-144, 148-150. In fact, a POSITA would avoid "wasted space" between pads to minimize chip size. *Id.* ¶¶108, 148-150; *supra* Section III.C.2. Thus the "extra space" teachings in Saint 80-81 do not motivate the formation of the claimed "saved area" in Saint Figure 7-7.

Fourth, Petitioner's modification of Saint Figure 7-7 by adding bonding wire over the "saved space" (Pet. 78-83), relies on two modifications that are contradictory for the reasons already discussed earlier in Section III.C.2.

VI. Conclusion

For the reasons set forth above, the Board should deny the Petition for Inter Partes Review.

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Patent Owner's Response complies with the word count limitation of 37 C.F.R. § 42.24(b)(2) because the Patent Owner's Response contains a total of 13,369 words, which is the sum of 13,341 words calculated by Microsoft Word's word-count feature and 28 words hand counted in the figures. This total excludes the cover page, signature block, and the parts of the Patent Owner's Response exempted by 37 C.F.R. § 42.24(b)(2).

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 17th day of September, 2025, a true and correct copy of the foregoing **Patent Owner's Response and all Exhibits** were served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

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