

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00118
U.S. Patent No. 10,879,164
Issue Date: December 29, 2020

Title: INTEGRATED CIRCUIT ELECTROSTATIC DISCHARGE BUS
STRUCTURE AND RELATED METHOD

PETITIONER'S REPLY BRIEF

	<u>Page</u>
<u>TABLE OF CONTENTS</u>	
TABLE OF EXHIBITS	v
LISTING OF CHALLENGED CLAIMS.....	ix
I. INTRODUCTION	1
II. PO’S BONDWIRE/PADS ARGUMENTS FAIL.....	2
A. PO’s Ground 1 Arguments Fail.....	2
1. PO’s Fig. 3 Argument Fails	2
2. PO’s “Metallization” Argument Fails.....	3
3. PO’s Noise/Inductance Arguments Fail	5
4. Jumper Bondwires Were Well-Known.....	6
5. PO’s Bondwire “Exposure” Argument Fails	8
6. PO’s “Cost” and “Complexity” Arguments are Baseless	9
7. PO’s Cases Are Unavailing	9
8. PO’s “Droop” Argument Fails.....	10
B. PO’s Ground 2 Arguments Fail.....	10
C. PO’s Ground 3 Arguments Fail.....	12
III. PO’S “ESD BUS” ARGUMENTS FAIL.....	13
A. PO’s Ground 3 “Common ESD Bus” Arguments Fail	13
B. PO’s Ground 1 and 2 “ESD Bus” Arguments Fail	17
1. Yoshinaga Fig. 6 Has Unlabeled Grounds Pads	17
2. PO’s Strawman Pad Placement Argument Fails	18
3. Assigning Grounds Pads Adjacent Yoshinaga’s Saved Areas Was Obvious.....	19
4. PO’s Strawman “Disadvantages” Argument Fails	23
IV. PO’s “SAVED AREA” ARGUMENTS FAIL.....	25
A. The Claims Do Not Require “Creating” a Saved Area.....	26
B. PO’s “Droop” Argument Fails	27
C. PO’s “Circuit Area” Argument Fails	29
D. PO’s Imaginary Pad Argument Fails	31

E.	PO’s Hindsight Argument Fails	33
F.	PO’s Bodily Incorporation Argument Fails	34
G.	PO’s Chip Size Argument Fails	34
V.	CONCLUSION.....	35

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>Adidas AG v. Nike, Inc.</i> , 963 F.3d 1355 (Fed. Cir. 2020)	9
<i>Cutsforth, Inc. v. MotivePower, Inc.</i> , 636 F. App’x 575 (Fed. Cir. 2016)	22
<i>In re Epstein</i> , 32 F.3d 1559 (Fed. Cir. 1994)	24
<i>In re Etter</i> , 756 F.2d 852 (Fed. Cir. 1985)	34
<i>Forest Labs., LLC v. Sigmapharm Labs., LLC</i> , 918 F.3d 928 (Fed. Cir. 2019)	9, 16
<i>GUI Glob. Prods., Ltd. v. Samsung Elecs. Co.</i> , 2024 WL 1564694 (Fed. Cir. Apr. 11, 2024)	21, 22
<i>Intel Corp. v. PACT XPP Schweiz AG</i> , 61 F.4th 1371 (Fed. Cir. 2023)	16
<i>Intel Corp. v. Qualcomm Inc.</i> , 21 F.4th 801 (Fed. Cir. 2021)	17
<i>Juniper Networks, Inc. v. Correct Transmission, LLC</i> , 2024 WL 3517862 (Fed. Cir. July 24, 2024).....	16
<i>Koninklijke Philips N.V. v. Google LLC</i> , 948 F.3d 1330 (Fed. Cir. 2020)	19
<i>KSR Int’l Co. v. Teleflex Inc.</i> , 550 U.S. 398 (2007).....	20, 21, 35
<i>In re Mouttet</i> , 686 F.3d 1322 (Fed. Cir. 2012)	12
<i>Nera Innovations Ltd. v. Squires</i> , No. 2024-1079, 4-5 (Fed. Cir., Oct. 24, 2025)	16

<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005)	26
<i>Polaris Indus., Inc. v. Arctic Cat, Inc.</i> , 882 F.3d 1056 (Fed. Cir. 2018)	22
<i>Purdue Pharma L.P. v. Accord Healthcare Inc.</i> , 2024 U.S. Dist. LEXIS 161403 (D. Del. Sept. 9, 2024).....	17
<i>Securus Techs., Inc. v. Glob. Tel*Link Corp.</i> , 701 F. App’x 971 (Fed. Cir. 2017)	9, 10

TABLE OF EXHIBITS

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 10,879,164 to Li ("the '164 Patent")
1002	File History of U.S. Patent No. 10,879,164
1003	Declaration of Dr. Daniel Foty ("Foty")
1004	<i>Curriculum Vitae</i> of Dr. Daniel Foty
1005	Japanese Unexamined Patent Application Publication No. JP2006-93598 to Yoshinaga ("Yoshinaga")
1006	Certified Translation of Japanese Unexamined Patent Application Publication No. JP2006-93598 to Yoshinaga ("Yoshinaga")
1007	U.S. Patent No. 9,070,700 to Haralabidis ("Haralabidis")
1008	IC Mask Design: Essential Layout Techniques, Christopher Saint and Judy Saint, McGraw-Hill (2002) ("Saint")
1009	Library of Congress Catalog Record for IC Mask Design: Essential Layout Techniques, Christopher Saint and Judy Saint, McGraw-Hill (2002)
1010	United States Copyright Office Record for IC Mask Design: Essential Layout Techniques, Christopher Saint and Judy Saint, McGraw-Hill (2002)
1011	U.S. Patent No. 6,078,068 ("Tamura")
1012	U.S. Patent No. 7,129,574 ("Wu")
1013	U.S. Patent No. 6,144,542 ("Ker")
1014	U.S. Patent Publ. No. 2004/0140860 ("Miller")
1015	U.S. Patent No. 7,880,310 ("Mathew")

EXHIBIT NO.	DESCRIPTION
1016	U.S. Patent Publ. No. 2007/0215994 (“Beauchamp”)
1017	Comprehensive Dictionary of Electrical Engineering, 2nd Ed. (2005)
1018	Wiley Electrical and Electronics Engineering Dictionary (2004)
1019	The Authoritative Dictionary of IEEE Standards Terms, 7th Ed. (2000)
1020	U.S. Patent No. 6,097,098 (“Ball”)
1021	Minute Order (case schedule), Dkt. No. 141, dated September 18, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1022	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1023	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, LTD.’s Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1024	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:24-cv-04223-RFL which has been consolidated with Case No. 3:23-cv-05792-RFL
1025	YMTC’s October 2, 2024 Infringement Contentions for the ’164 Patent [FILED UNDER SEAL]

EXHIBIT NO.	DESCRIPTION
1026	C. Ito, K. Banerjee, and R. Dutton, "Analysis and Design of ESD Protection Circuits for High-Frequency/RF Applications," Proceedings of the International Symposium on Quality of Electronic Design, pp. 117-122 (2001).
1027	Uyemura, "Chip Design for Submicron VLSI," Thomson, 2006.
1028	Declaration of Jared Bobrow in Support of Petitioner's Motion for Admission <i>Pro Hac Vice</i>
1029	Email from Franchesca I. Alicea Villanueva (PTAB) regarding IPR2025-00118 – Preliminary Reply Request, dated April 8, 2025
1030	Order Granting Motion to Stay Pending <i>Inter Partes</i> Review, dated March 14, 2025 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1031	RESERVED
1032	Datasheet for Philips 80C31/80C32 Microcontroller, Aug. 7, 2000
1033	Datasheet for Silicon Labs C8051F020/1/2/3 Microcontroller, Rev. 1.4, December 2003
1034	Datasheet for Texas Instruments MSP430G2x53 Mixed-Signal Microcontroller, May 2013
1035	Datasheet for Zilog Z8 Encore! XP® F64xx Series, 2014
1036	Datasheet for PL-2303HX Edition USB to Serial Bridge Controller, Prolific, May 23, 2006
1037	<i>Getting to the Bottom of Deep Submicron II: A Global Wiring Paradigm</i> , D. Sylvester et al., 1999

EXHIBIT NO.	DESCRIPTION
1038	Deposition Transcript of Dr. Sunil Khatri, December 3, 2025
1039	U.S. Patent No. 6,424,263 (“Lee”)
1040	U.S. Patent No. 7,375,978 (“Conner”)
1041	U.S. Patent Publ. No. 2007/0029661 (“Beddingfield”)
1042	Supplemental Declaration of Dr. Daniel Foty (“Foty_Supp.”)
1043	<i>The Microelectronic Wire Bond: Past, Present, and Future</i> , H.K. Charles <i>et al.</i> , IMAPS 2010 - 43rd International Symposium on Microelectronics
1044	U.S. Patent No. 6,110,816 (“Huang”)
1045	<i>Research Progress on Bonding Wire for Microelectronic Packaging</i> , H. Zhou <i>et al.</i> , Micromachines vol. 14, pp. 232 – 255 (2023)

LISTING OF CHALLENGED CLAIMS

Ref. #	Listing of Challenged Claims
claim 1:	
[1.PRE]	An integrated circuit structure, comprising:
[1.A]	a circuit area;
[1.B]	a plurality of ESD buses;
[1.C]	a plurality of pad groups, adjacent and connected to the plurality of ESD buses;
[1.D]	a common ESD bus, adjacent to the plurality of pad groups; and
[1.E]	a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus;
[1.F]	wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.
claim 2:	
[2]	The integrated circuit structure of claim 1, wherein each of the plurality of pad groups comprises at least one pad, and the plurality of bonding wires is configured to connect the at least one pad to the common ESD bus.
claim 3:	
[3]	The integrated circuit structure of claim 1, wherein common ESD bus comprises a plurality discontinuous ESD bus groups.

Ref. #	Listing of Challenged Claims
claim 4:	
[4]	The integrated circuit structure of claim 1, wherein the common ESD bus is formed outside the plurality of chip edges or inside the plurality of chip edges.
claim 5:	
[5]	The integrated circuit structure of claim 1, wherein the common ESD bus is parallel to the plurality of ESD buses.
claim 6:	
[6.PRE]	An integrated circuit structure, comprising:
[6.A]	a circuit area;
[6.B]	a plurality of ESD buses;
[6.C]	a plurality of pad groups, adjacent and connected to the plurality of ESD buses; and
[6.D]	a plurality of bonding wires configured to connect one to another of the plurality of pad groups;
[6.E]	wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.
claim 7:	
[7]	The integrated circuit structure of claim 6, wherein each of the plurality of pad groups comprises a connecting pad, and the plurality of bonding wires are configured to connect the connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups.

Ref. #	Listing of Challenged Claims
claim 8:	
[8.PRE]	A method of integrated circuit structure, comprising:
[8.A]	forming a circuit area;
[8.B]	forming a plurality of ESD buses;
[8.C]	forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses;
[8.D]	forming a common ESD bus adjacent to the plurality of pad groups; and
[8.E]	connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires;
[8.F]	wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.
claim 9:	
[9]	The method of integrated circuit structure of claim 8, wherein each of the plurality of pad groups comprises at least one pad, and the plurality of bonding wires is configured to connect the at least one pad to the common ESD bus.
claim 10:	
[10]	The method of integrated circuit structure of claim 8, further comprising: forming the common ESD bus outside the plurality of chip edges or inside the plurality of chip edges.

Ref. #	Listing of Challenged Claims
claim 11:	
[11]	The method of integrated circuit structure of claim 8, wherein the common ESD bus is parallel to the plurality of ESD buses.
claim 12:	
[12.PRE]	A method of integrated circuit structure, comprising:
[12.A]	forming a circuit area;
[12.B]	forming a plurality of ESD buses;
[12.C]	forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses; and
[12.D]	connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires across the circuit area;
[12.E]	wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.
claim 13:	
[13]	The method of integrated circuit structure of claim 12, wherein a common ESD bus is parallel to the plurality of ESD buses and the plurality of pad groups.

Ref. #	Listing of Challenged Claims
claim 14:	
[14]	The method of integrated circuit structure of claim 12, wherein each of the plurality of pad groups comprises a connecting pad, and the plurality of bonding wires are configured to connect the connecting pad of one of the plurality of pad groups to the connecting pad of another of the plurality of pad groups.

TABLE OF ABBREVIATIONS

ABBREVIATION	TERM
'164 patent	U.S. Patent No. 10,879,164 (EX1001)
Foty	Declaration of Dr. Daniel Foty (EX1003)
Yoshinaga	Japanese Unexamined Patent Application Publication No. JP2006-93598 (EX1005)
	Certified Translation of Japanese Unexamined Patent Application Publication No. JP2006-93598 (EX1006)
Haralabidis	U.S. Patent No. 9,070,700 (EX1007)
Saint	IC Mask Design: Essential Layout Techniques, Christopher Saint and Judy Saint, McGraw-Hill (2002) (EX1008)
Miller	U.S. Patent Publ. No. 2004/0140860 (EX1014)
Mathew	U.S. Patent No. 7,880,310 (EX1015)
Beauchamp	U.S. Patent Publ. No. 2007/0215994 (EX1016)
Lee	U.S. Patent No. 6,424,263 (EX1039)
Conner	U.S. Patent No. 7,375,978 (EX1040)
Beddingfield	U.S. Patent Publ. No. 2007/0029661 (EX1041)
Foty_Supp.	Supplemental Declaration of Dr. Daniel Foty (EX1042)
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,879,164 (IPR2025-00118, Paper 1)
POR	Patent Owner's Response (IPR2025-00118, Paper 31)
PO or Patent Owner	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.

I. INTRODUCTION

The file history makes clear that the *saved area* limitation resulted in allowance. Pet. 17-18 (citing EX1002, 216-218, 230-233). Saint (and Yoshinaga) plainly disclose *saved area[s]*. Saint, Fig. 9-28 (left); Yoshinaga, Fig. 6 (right). Saint expressly teaches placing circuitry in “wasted spaced” (orange areas) “between the [bond] pads” (blue) to “get the chip as small as possible.” Saint, 220-221.

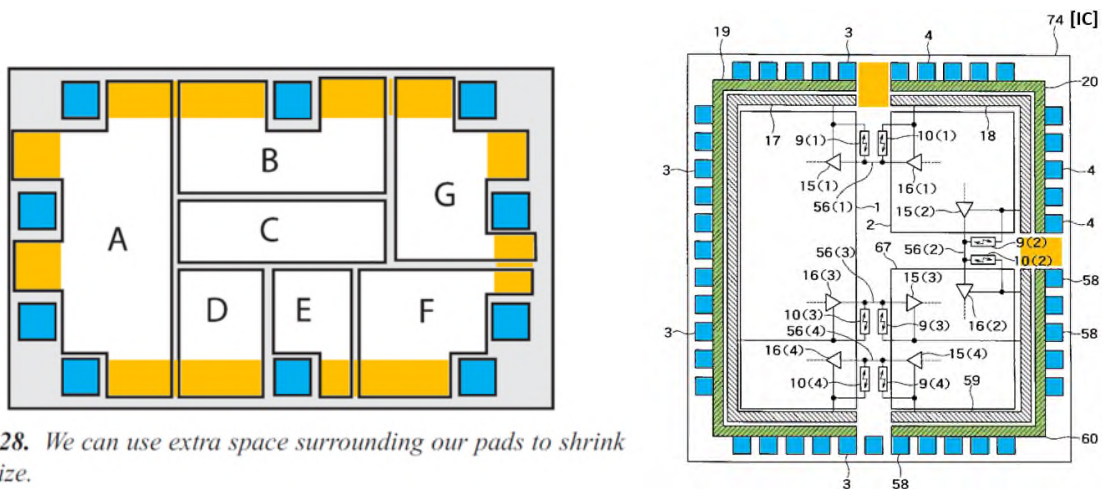


Figure 9–28. We can use extra space surrounding our pads to shrink our chip size.

Rather than address the file history, which it concededly ignored (POR, 9-10), PO takes a kitchen-sink approach, presenting numerous half-baked and unsupported assertions, and misrepresenting Petitioner's positions to set up strawman arguments. But no amount of misdirection or mudslinging¹ changes the fact that Yoshinaga,

¹ PO disparages Petitioner’s figures as “manipulations” (POR, 2), but Petitioner illustrated its modifications for ease of understanding, and expressly noted the changes.

Saint, and Haralabidis render the Challenged Claims obvious. Foty_Supp., ¶¶5-10, 20-21, 184.

II. PO'S BONDWIRE/PADS ARGUMENTS FAIL

A. PO's Ground 1 Arguments Fail

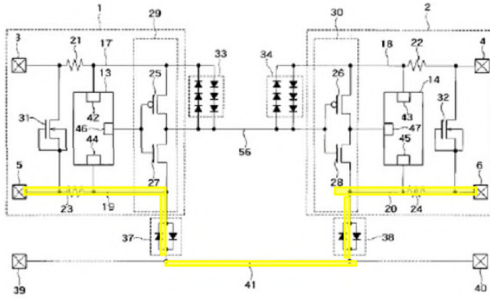
PO is wrong that no motivation or reasonable expectation of success exists to connect Yoshinga's ground pads with bondwires. POR, §§III.B.1-2.

1. PO's Fig. 3 Argument Fails

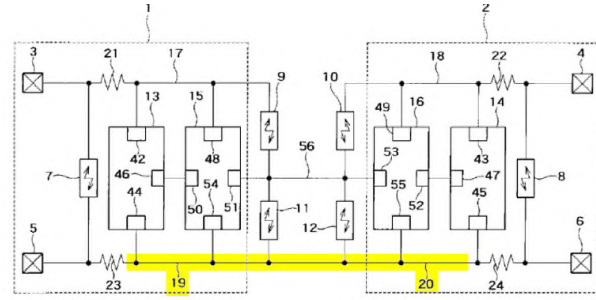
PO argues that Yoshinaga Figs. 1-2, 4, and 6 cannot connect ground pads 5 and 6 with a bondwire because Figure 3 (which illustrates only one possible implementation of Fig. 1) "shows reference potential lines 19 and 20 connected to each other through bidirectional diode pairs [37 and 38]." POR, 30. This argument fails because: (1) none of Figs. 1-2 or 4 has "bidirectional diode pairs [37 and 38]"; and (2) Yoshinaga Fig. 6 implements "the semiconductor [IC] of **FIG. 1**," which lacks such diodes. Yoshinaga, [0087], [0074]. PO's Fig. 3 reliance is both misplaced and irrelevant.

PO annotates Fig. 3 (left image), but Petitioner relies on Fig. 2² (right image). Notably, Fig. 3 includes bidirectional diodes 37 and 38 in the connection path. Fig. 2 (and Figs. 1 and 4) do not.

² Figs. 1-2 and 4 have the same relevant disclosure (*viz.*, ground pad 5 and 6 connection).



POR, 31 (Yoshinaga, Fig. 3)
(annotated by PO)



Pet., 35 (Yoshinaga, Fig. 2)
(annotated by Petitioner)

PO's attempt to generalize Fig. 3 to Figs. 1-2 and 4 is misdirection. PO misstates Petitioner's position by asserting that Petitioner "replace[d] [Fig. 3's] bidirectional diodes" with bondwires. POR, 33. Petitioner did no such thing. Yoshinaga Figs. 1-2 and 4 themselves disclose that ground pads 5 and 6 are electrically connected *without intervening diodes*. Foty_Supp., ¶¶181-182.

2. PO's "Metallization" Argument Fails

PO argues that a POSITA would not use bondwires to connect ground pads 5 and 6 because Figs. 1-2 and 4 "show a shorted connection ... comprised of the integrated circuit metallization, *i.e.* [an on-chip metal trace]." POR, 31. While Figs. 1-2 and 4 show electrically connecting ground pads 5 and 6, the figures do *not* disclose (let alone require) a metal trace. Pet., 35; Foty_Supp., ¶¶140-144. PO cites

nothing in Yoshinaga for its “metallization” argument.³ Indeed, Dr. Khatri calls Figs. 1-4 “block diagrams.” EX2010, ¶41. This also resolves PO’s gripe that bondwires do not “improve[] over the specific connections Yoshinaga teaches.” POR, 33-34.

Of course, the ground connections must be implemented somehow, and one obvious way is bondwires. §II.A.4; Foty_Supp., ¶¶129-134. And implementing an expressly disclosed connection does not “add” something not contemplated by the reference. If PO’s metallization argument were correct, Fig. 6 would show a metal trace connecting reference lines 19, 20, and 60, but it does not. Foty_Supp., ¶143; EX1038, 157:19-22, 179:25-180:23.

PO’s insinuation that numerous bondwire alternatives exist (POR, 35-36) is unsupported, and contradicted by its expert who testified that only “two options [exist] for the matter at hand.” EX1038, 157:23-158:20, *see also* 161:19-162:5. Thus, there are finite options a POSITA would try. Foty_Supp., ¶144.

³ PO excerpts Dr. Foty’s testimony out of context. POR, 31 (citing EX2011, 163:12-164:5, 164:18-165:14). Dr. Foty testified about connecting “[a] pad down to an actual transistor,” not connecting pads 5 and 6. EX2011, 164:6-17, 165:1-4, 168:14-169:17.

3. PO's Noise/Inductance Arguments Fail

PO's argument that bondwires would "introduce[] noise" (POR, 33) by connecting ground pads 5 and 6 is baseless. Foty_Supp., ¶¶69-78. PO's premise is that bidirectional diodes 37 and 38 in Fig. 3 reduce noise, so removing them increases noise. POR, 37-38. But Petitioner starts from Figs. 1-2 and 4, which connect ground pads 5 and 6 *without intervening diodes* and work fine. The lack of diodes is unsurprising given that modest noise in average chips is irrelevant, just like modest signal noise did not stop AM/FM radio from proliferating. Foty_Supp., ¶¶76, 181-182.

PO's "noise" argument (POR, 38) is belied by its expert who used bondwires without problems in his three Texas A&M chips between 2010-2020. EX1038, 104:9-105:6, 118:19-119:4, 120:12-121:2, 121:18-24, 132:8-16, 133:25-134:16. Moreover, because Petitioner's jumper bondwire is short, its inductance (and associated noise) is small. §IV.B. The '164 patent's silence regarding bondwire "noise" confirms that PO's concern is overblown.

PO's cite to EX2012 (POR, 38) is unavailing, as Davis discusses large microprocessors, not "deep sub-micron" chips generally. EX2012, 49; Foty_Supp., ¶¶92-111. And PO ignores wirebonding advances that, for decades, disproved prognostication that "conventional wire-bonding technology is not [scalable]." Foty_Supp., ¶¶97-111. PO further ignores that Davis' concern is inapplicable to

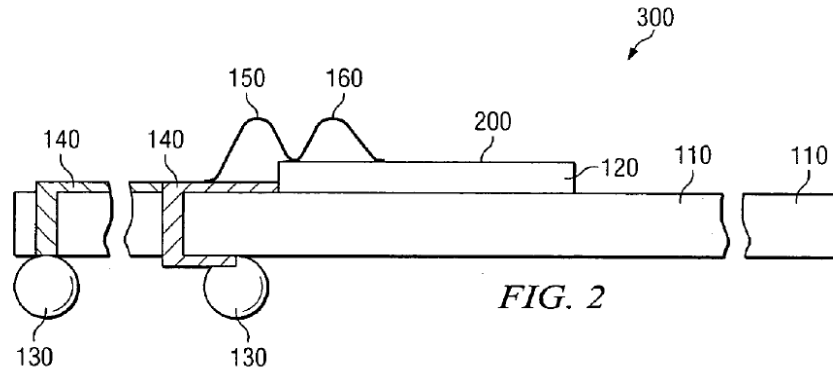
core-limited chips (like Yoshinaga). *Id.* Indeed, roughly 80% of chips worldwide use bondwires. EX1043, 1. Dr. Khatri did not know this (EX1038, 162:18-169:6, 178:20-179:4), but admitted that manufacturing techniques “improve over the years,” and “so it’s completely not surprising to me that what was considered [] in the conventional wisdom as a bad idea has been solved in multiple ways.” EX1038, 254:16-255:2, 248:23-249:21.

Dr. Khatri ignores that “[p]ractical transmission circuits always combine some amount of both resistance and inductance” (EX2014, 2), making bondwires a compelling option (Foty_Supp., ¶78). PO’s concern about bondwire inductance at “high [frequencies]” (POR, 38) ignores (1) billions of chips that operate at lower frequencies; and (2) Miller’s solution is keeping bondwires short (precisely what Petitioner proposes). §IV.B; Foty_Supp., ¶77.

4. Jumper Bondwires Were Well-Known

PO concedes bondwires were “well-known.” POR, 35. Dr. Khatri’s admission that bondwire technology “was known for a while” (EX1038, 138:25-139:4) vastly understates its decades-long history. Foty_Supp., ¶¶45-54. Contrary to PO’s assertion, this includes “jumper” bondwires. In addition to Beauchamp, Miller, and Mathew, other references confirm this common practice. *Id.*, ¶¶55-59, 79-82. For example, Beddingfield is titled “Power Plane Design and Jumper Wire Bond for Voltage Drop Minimization.” EX1041. Fig. 2 shows jumper bondwire

160 “over a surface of the die 120” to provide a “lower resistance” path for power and ground connections. *Id.*, [0015]; *see also* [0016]-[0018], [0022].



Id., Fig. 2.

Lee Fig. 4 uses jumper bondwires 206a and 206b to hop over other circuit components. EX1039, 2:61-3:5 (“The jumper may be a bondwire ... This form of construction is easy to manufacture and low in cost”).

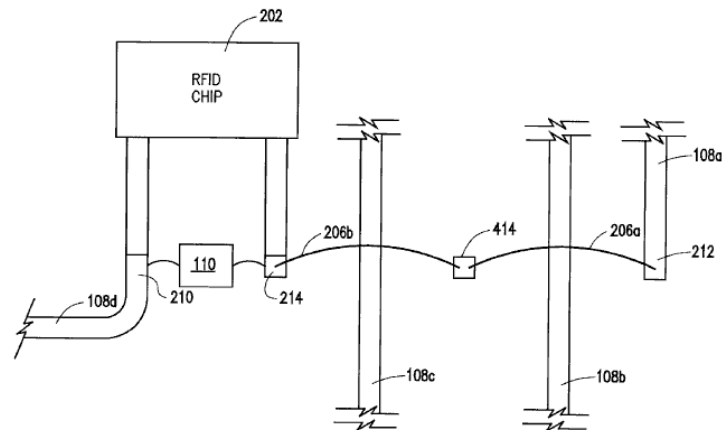
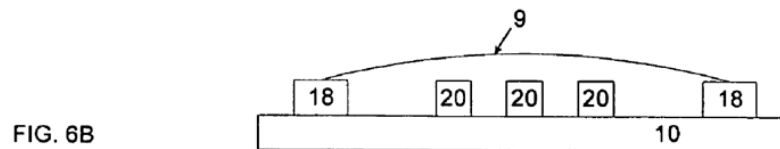
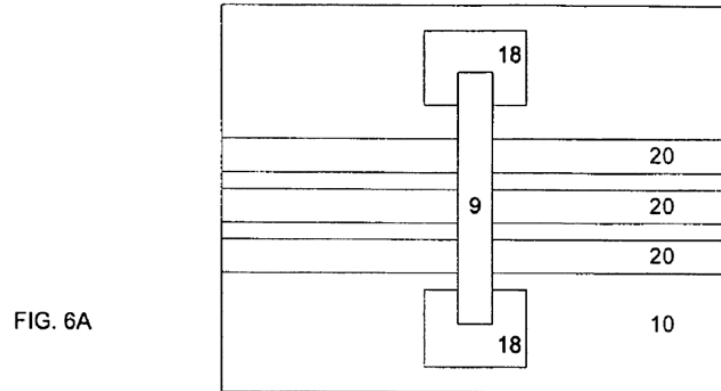


FIGURE 4

Id., Fig. 4.

In Conner Fig. 6, jumper bondwire 9 “bridges a number of signal traces 20” and provides “improved trace routing capability.” EX1040, 3:37-59.



Id., Figs. 6A-6B. PO’s unsupported argument that jumper bondwires were unknown or disfavored contradicts voluminous record evidence.

5. PO’s Bondwire “Exposure” Argument Fails

PO’s argument that bondwires would not be used because of “exposure ... to the elements” (POR, 38) is baseless. Saint teaches that “[bond]wires are covered in plastic, which also covers the chip.” Saint, 202-203.

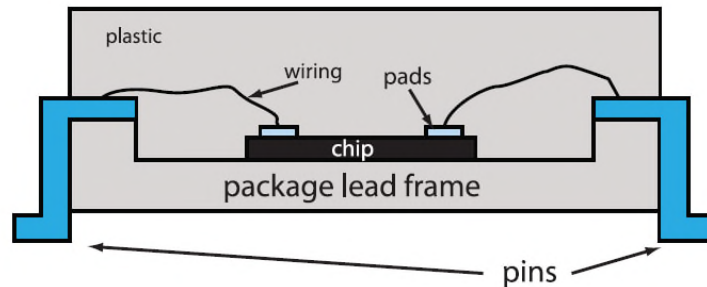


Figure 9-2. The top plastic is molten when deposited. The wires are surrounded before it hardens.

Id., Fig. 9-2 (bondwires “surrounded before [the molten plastic] hardens”); EX1039, 3:1-5 (“After the bondwires are installed, an encapsulation (glop top) cover ... [protects the] bondwires”); Foty_Supp., ¶¶50-53.

6. PO’s “Cost” and “Complexity” Arguments are Baseless

Bondwires have no active circuitry/components and are, literally, just metal wires. Far from being “complex,” bondwires are relatively simple, especially compared to fabricating metal traces. Foty_Supp., ¶¶45-46. PO’s assertion that cost would deter bondwire usage is baseless. POR, 36. PO’s expert admitted low cost encouraged bondwire use. EX1038, 132:8-16 (“we use[d] bondwires because we’re poor ... on a shoestring budget”).

7. PO’s Cases Are Unavailing

Adidas turned on undisputed “fundamental differences” in the combined references. 963 F.3d 1355 at 1359. No such “fundamental differences” exist here. And *Forest Labs* recognizes that motivation can be found “implicitly in the prior art references themselves.” 918 F.3d at 934. Here, PO’s expert admits Yoshinaga

discloses bond pads (for connecting bondwires). EX1038, 283:5-11. Given the ubiquity of bondwires as a well-known, suitable option, Yoshinaga's disclosure provides sufficient motivation.

Citing *Securus*, PO argues analogous art is insufficient motivation to combine. POR, 37. But *Securus* merely states that analogous art "without more" is not enough. 701 F.App'x at 976-977. Here, Petitioner provided far more. Pet., §X.E (48-51) (five motivations); §XI.J (65-67) (four motivations); §XII.M (94-98) (five reasons).

8. PO's "Droop" Argument Fails

Section IV.B addresses PO's "droop" argument.

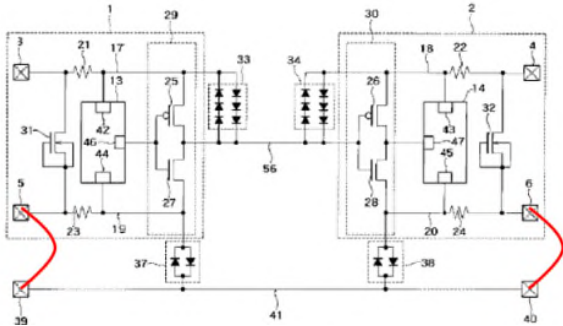
B. PO's Ground 2 Arguments Fail

PO's only non-cumulative Ground 2 argument (§IV.A.2) is lack of motivation to connect Haralabidis' common ESD bus with bondwires. POR, 51-56. This argument fails.

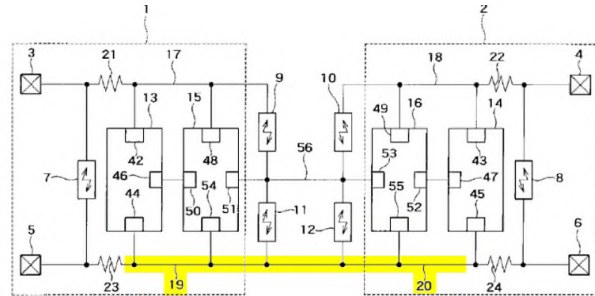
First, PO misleadingly suggests that Haralabidis' lack of explicit "bond pad" disclosure equates to a lack of bondwire disclosure. POR, 51. That is false. Haralabidis expressly discloses "wirebond[]" ground rail connections. Haralabidis, 1:61-2:4, 2:38-41; Foty_Supp., ¶180.

Second, PO's Yoshinaga Fig. 3 argument (POR, 52-53) is misdirection. PO adds bondwires to Fig. 3 (left) and attributes them to Petitioner. POR, 53-54; EX1038, 330:16-22. The Petition contains no such figure. By contrast, Petitioner

relies on Yoshinaga Fig. 2 (right), showing an electrical connection between ground pads 5 and 6 (through ESD buses 19 and 20). Pet., 35.



POR, 54 (Yoshinaga, Fig. 3)
(PO annotated)



Pet., 35 (Yoshinaga, Fig. 2)
(Petitioner annotated)

PO continues its smoke-and-mirrors tactics by generalizing Fig. 3's use of bidirectional diodes 37 and 38 as the means of connecting ground pads 5 and 6 to Figs. 1-2 and 4, which lacks such diodes. POR, 52. PO's "noise" argument (POR, 53-54) fails as noted *supra* §§II.A.1, II.A.3.

Third, PO argues against using Haralabidis' ESD teachings because Yoshinaga Fig. 3 "has sufficient⁴ ESD protection." POR, 54. This is more misdirection. Petitioner cites Fig. 3 only in passing or when generically referencing "Figs. 1-4." By contrast, Petitioner repeatedly and expressly shows, annotates, and discusses, *e.g.*, Fig. 2, which lacks diodes 37 and 38. Pet., 22, 30, 34-35. PO's

⁴ PO fails to explain what "sufficient" means. It cannot mean Yoshinaga solved all ESD problems because engineers today continue improving ESD.

argument also relies on the incorrect legal premise that disclosing an alternative embodiment forecloses obviousness. *In re Mouttet*, 686 F.3d 1322, 1334 (Fed. Cir. 2012).

PO's assertion that "Haralabidis' common ground rail would increase chip size, noise, and complexity" is baseless. POR, 55. Haralabidis' common ground rail is **off-chip** in the package (Fig. 3) or PCB (Fig. 5), and thus cannot "increase chip size." Contrary to PO's noise assertion, Haralabidis expressly teaches its "common ground rail ... assists greatly in attenuating [] noise/interference." Haralabidis, 5:3-31, Fig. 6.

Fourth, PO argues Petitioner must provide express disclosure of bond pads "connected to a common ESD bus using bonding wires." POR, 55-56. PO's argument misapprehends that Petitioner argues obviousness, not anticipation. PO's reasonable expectation of success argument (*id.*) fails because Haralabidis discloses connecting bondwires to ESD buses, and Saint discloses connecting bondwires to bond pads. No more is required.

C. PO's Ground 3 Arguments Fail

PO's Ground 3 arguments (POR, §V.B) are repetitive. **First**, for claims 6-7 and 12-13, PO repeats its jumper bondwire argument (POR, 65), which fails as §II.A explains. **Second**, PO argues a POSITA would not have combined Saint with Haralabidis because Saint employs an ESD bus "internal" to the chip while

Haralabidis describes off-chip circuitry (*viz.*, an “external” ESD bus). POR, 65-66. PO’s logic is backwards—Saint’s focus on chip-level circuitry and Haralabidis emphasis on off-chip circuitry ***supports combining the references***. Haralabidis teaches pushing internal ESD bus circuitry (as in Saint) off chip (*viz.*, to the package or PCB) for improved noise resistance and ESD protection. Haralabidis, 5:20-25, 5:49-66. ***Third***, PO repeats its teaching away and “mentalization” [sic] arguments (POR, 66), addressed in §II.A.

III. PO’S “ESD BUS” ARGUMENTS FAIL

A. PO’S Ground 3 “Common ESD Bus” Arguments Fail

POR §V.A argues that Ground 3 lacks the ***common ESD bus*** that independent claims 1 and 8 require. PO’s expert (EX2010, §IX.A) applies a similar analysis to independent claims 6 and 12, which require connecting the ***plurality of ESD buses*** with bondwires. Petitioner addresses both arguments together.

PO’s arguments (framed several ways) amount to the same issue—whether it would have been obvious for Saint Fig. 7-7’s ground buses to connect to ground. POR, 60-63. The answer is a resounding yes! That is the most common meaning of “ground,” so named because it literally uses the earth (*i.e.*, “ground”) as the reference voltage. Foty_Supp., ¶¶112-119. To conclude otherwise runs counter to long-standing engineering conventions. *Id.*, ¶¶112-139 (esp. 114-128).

According to PO, three different “ground” voltages exist for the same chip.

This makes little sense and would complicate (if not eliminate) inter-domain communication. Foty_Supp., ¶¶137-139. At a minimum, it would have been obvious for GND1/GND2/GND3 to unite per common engineering practice. *Id.*, ¶¶119-123, 126.

PO's primary basis for arguing that Saint Fig. 7-7 uses "three separate and distinct" ground voltages is Saint's GND1/GND2/GND3 nomenclature. POR, 60-62. But Saint contradicts this unsupported assumption and shows "GND1" and "GND2" contacts in a singular "ring of ground substrate contacts" (*i.e.*, connected to the same ground substrate). Saint, 142; Foty_Supp., ¶¶120-121.

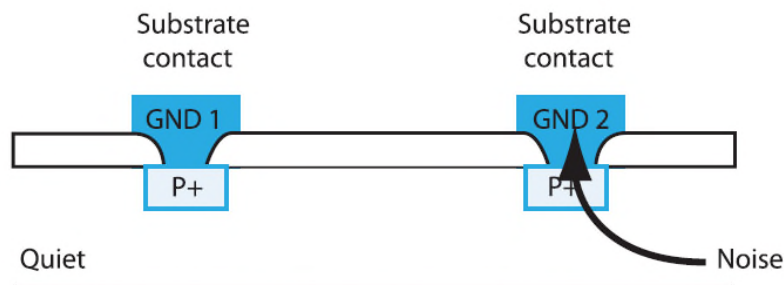


Figure 6-2. Placing some slippery exits in the way helps eliminate traveling noise.

Saint, Fig. 6-2. A POSITA would have understood Fig. 7-7's GND1/GND2/GND3 designations simply reflect that they correspond to VCC1/VCC2/VCC3, respectively. Foty_Supp., ¶¶122-123. Differing supply voltages (*e.g.*, VCC1=3V, VCC2=5V, etc.) does not mean reference voltages differ. To the contrary, as Saint Fig. 6-2 shows, GND1, GND2, etc. are the same. Haralabidis confirms this. *Id.* Haralabidis has "respective ground connections VSS1, VSS2, VSSN," analogous to

Saint's GND1/GND2/GND3. Haralibidis, 5:42-6:2. Haralabidis explains that "each ground connection VSS1, VSS2, VSSN is connected to ... the PC board common ground rail 670." *Id.* Similarly, Yoshinaga labels the same reference lines with different numerals (*e.g.*, 19, 20, 60) based on their corresponding power domain. Yoshinaga, Fig. 6, [0088].

PO's contrary assertion is like saying shower and sink drains do not connect before exiting a house. While possible, such an approach is rare. Likewise, in electronics, the far more common (and obvious) approach is connecting ground buses on (or near) the chip as Saint Case Study 1 discloses. *Foty_Supp.*, ¶124; Saint, 333 ("hook[] up all [] ESD grounds to each other").

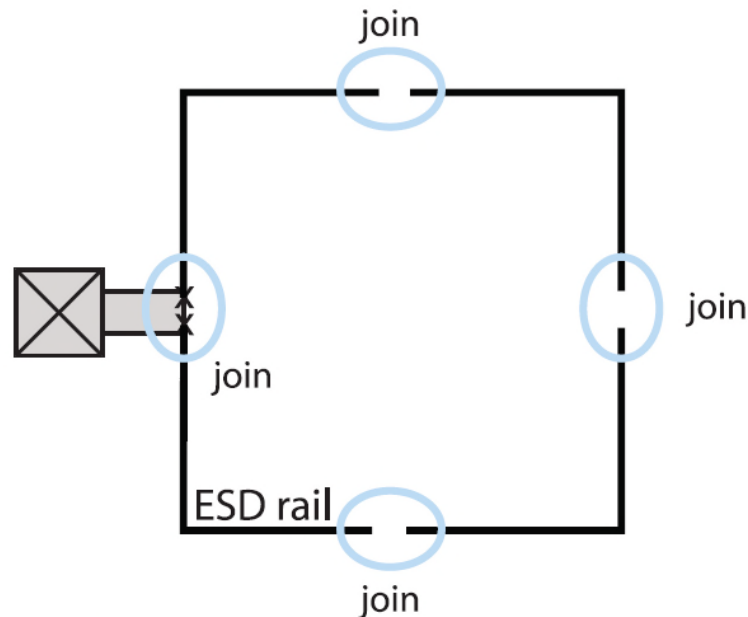


Figure CS1-87. ESD ground wiring connections.

Id., Fig. CS1-87.

Far from an “incompatible teaching” (POR, 62-63), Case Study 1 supports Petitioner's shared/common ground point. Like Fig. 7-7, Case Study 1 discloses various power domains (*e.g.*, VCC1, VCC2, etc.), and expressly discloses “join[ing]” the corresponding ground buses. Saint, Fig. CS1-1, CS1-87 (shown above). PO fundamentally misunderstands the nature of Fig. 7-7 (a conceptual illustration showing power domain groupings) and Case Study 1 (an actual layout/implementation). Illustrating different abstraction levels does not make them “incompatible.” *Foty_Supp.*, ¶¶125-127; *Nera Innovations Ltd. v. Squires*, No. 2024-1079, 4-5 (Fed. Cir., Oct. 24, 2025).

Saint Fig. CS1-1 shows segmented power domains (VCC1/VCC2/VCC3/VCC4) and CS1-99 shows a “continuous [ground] ring.” This is analogous to Saint Fig. 7-7, which shows separate power domains (VCC1/VCC2/VCC3), but does not concern itself with where or how the ground buses connect. *Foty_Supp.*, ¶¶125-126.

PO's *Juniper* case is easily distinguished. POR, 64. Unlike *Juniper's* “conclusory” expert testimony, Petitioner presents multiple references that expressly disclose a common ground. Saint, Fig. CS1-99; Haralabidis, Figs. 3, 5, 5:43-6:2. And *Forest Labs* (POR, 35, 64) is unavailing because the Federal Circuit merely remanded to assess motivation to combine in the first instance. 918 F.3d at 935. PO also ignores authority, like *Intel Corp. v. PACT XPP Schweiz AG*, which clarified

that a “known technique” need only be a “suitable option,” not the best option. 61 F.4th 1373, 1381 (Fed. Cir. 2023); *Purdue Pharma*, 2024 WL 4120717, *19.

PO's assertion that a bondwire and common ground rail would increase “die size and cost” (POR, 64) fails because Haralabidis' common ESD bus is located off-chip. Haralabidis, Fig. 3, 5. Thus, die size is unchanged, and PO's expert admitted bondwires are inexpensive. Foty_Supp., ¶128; EX1038, 132:8-16.

B. PO's Ground 1 and 2 “ESD Bus” Arguments Fail

Yoshinaga discloses that reference pads 5 and 6 connect. Yoshinaga, Figs. 1-2, 4. Thus, PO cannot make the same baseless argument it did for Ground 3—*viz.*, that ground rails have different voltages. But POR §III.A makes three equally baseless arguments.

PO does not dispute that Yoshinaga discloses *a plurality of ESD buses* (*viz.*, reference lines 19, 20, and 60) connected together (Yoshinaga, Figs. 1-2, 4, [0077]), or that pads 5 and 6 are bond pads (EX1038, 283:5-11) electrically connected to reference lines 19 and 20 (Yoshinaga, Figs. 1-2, 4).

1. Yoshinaga Fig. 6 Has Unlabeled Grounds Pads

The parties dispute whether Fig. 6 shows ground pads at all. PO says they are missing. POR, 22. Petitioner says a POSITA would have understood the ground pads are present in Fig. 6, just not labelled. Pet., 20 (“the statement that ‘[r]eference

potential pads are not shown' (Yoshinaga, [0078]) in Fig. 6 simply means they are not labelled").

Ground pads 5 and 6 are expressly shown and labelled in Fig. 1 (and Figs. 2 and 4). Yoshinaga, Fig. 1, [0055]. PO ignores that Fig. 6 implements Fig. 1, and thus has ground pads. *Id.*, [0087] (Fig. 6 is "semiconductor [IC] of FIG. 1."). Dr. Khatri conceded this. EX1038, 298:16-299:2, 213:21-214:9, 195:20-196:8.

PO's hyper-literal reading of Yoshinaga [0078]—divorced from the context of surrounding paragraphs and Fig. 6—fails. After describing power pads 3, 4, and 58 (labelled in Fig. 6) and corresponding reference lines 17, 18 and 59 (Yoshinaga, [0076]-[0077]), Yoshinaga says "[r]eference potential pads are not shown to simplify the drawing" (*id.*, [0078]). Given Fig. 6—showing numerous unassigned pads—and paragraphs [0076]-[0077] (describing reference numerals present in Fig. 6), a POSITA would have understood that Yoshinaga is simply saying the ground pad **labels** are not shown, not that ground pads are missing. Foty_Supp., ¶¶145-148, 163, 179. PO's arguments about what "not shown" means elsewhere in Yoshinaga (POR, 22-23) cannot supplant Fig. 6's context.

2. PO's Strawman Pad Placement Argument Fails

POR §III.A.1 quibbles primarily with Yoshinaga's reference/ground pad locations, not their existence, size, or electrical connections. PO argues Yoshinaga fails to satisfy claims 6-7, 12, and 14 because Figs. 1-4 do not show physical pad

placement. POR, 17. But Petitioner never argued they did. Rather, Petitioner noted the **electrical** ground pad connection in, *e.g.*, Fig. 2 (Pet., 35) connoted a corresponding physical pad, discussed vis-à-vis Fig. 6 (Pet., 35-39).

PO attempts to extrapolate the topological nature of Figs. 1-4 to Fig. 6 by suggesting Fig. 6 conveys nothing regarding physical pad location. POR, 18; Foty_Supp., ¶¶141-142. While Fig. 6 is not a complete implementation and is conceptual in some respects, no matter which pads are assigned as ground, each is **adjacent and connected to the ... ESD buses** (*viz.*, buses 19, 20, and 60) as elements 6[c] and 12[c] provide. PO's contrary assertion (POR, 17)—supported only by out-of-context deposition testimony—fails the red-face test. *Id.*, ¶157. So does PO's assertion that Petitioner failed to “specify where each [claim element] is found.” POR, 18. The Petition plainly does so. Pet., 33. And PO's attempt to excise POSITA knowledge from the obviousness inquiry violates §103 and well-established case law. *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330 at 1337 (Fed. Cir. 2020). Petitioner addresses the **adjacent** requirement vis-à-vis the **saved area** limitation of 6[e] and 12[e] *infra* §III.B.3.

3. Assigning Grounds Pads Adjacent Yoshinaga's Saved Areas Was Obvious

PO disputes whether it would have been obvious to assign the existing bond pads immediately adjacent Yoshinaga Fig. 6's **saved area** as ground pads. POR, 19-23. PO's argument fails because: (1) Yoshinaga's pads are identical; (2) it

contradicts *KSR* and its progeny, which clarified that a “known technique” need only be a suitable option, not the best option; and (3) Petitioner ***did*** explain why a POSITA would have made the pad assignments. Pet., 31-32, 34-39; Foty_Supp., ¶¶149-157.

First, like the '164 patent's pads, Yoshinaga's bond pads are identical. Yoshinaga's Fig. 6 pads are illustrated identically, and Fig. 6 shows “the semiconductor [IC] of FIG. 1,” which plainly includes ground pads 5 and 6.

Nevertheless, PO asserts “[p]ower supply pads and reference potential pads are fundamentally different.” POR, 23. Dr. Khatri testified just the opposite at his deposition. EX1038, 186:14-21 (“pads are all similar [] if not completely identical”), 204:25-205:19, 185:18-186:4, 203:24-204:7, 215:8-216:6. The fact that power and ground connect to different circuit elements says nothing about the pads themselves, and does not make them “fundamentally different.” *Id.* No difference in size, dimension, material, etc. exists between ground and power pads. Foty_Supp., ¶¶64-68, 149-153. And both dissipate ESD current. Saint, Fig. 7-3 (ESD protection “to VCC1 and GND1”). The Board should reject PO's attempt to conflate pads with the circuitry connected thereto.

Among other data points (*e.g.*, datasheets EX1032-EX1036), Saint confirms pad assignment flexibility, including that pad assignments dictate floor-planning, not the other way around as PO misleadingly suggests. Saint, 159-160, 209;

Foty_Supp., ¶¶166-173. Figs. 7-1 and 7-2 illustrate two different, but “totally valid,” pad assignments for the same chip. *Id.* Petitioner's Yoshinaga pad assignments are also “totally valid.” *Id.*, ¶¶153-154.

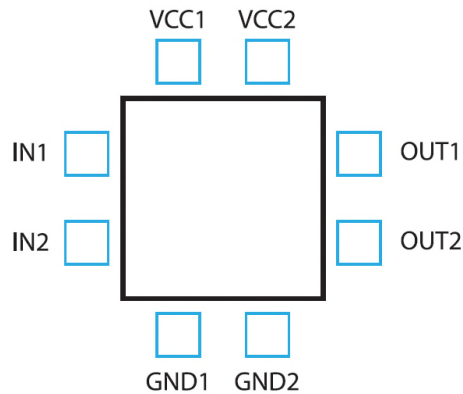


Figure 7-1. Like items set side by side. One possible pin-out.

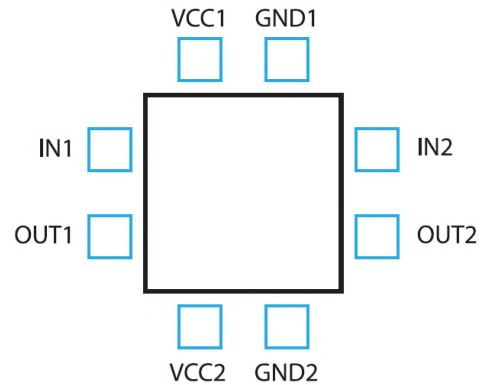


Figure 7-2. Very different pin placement will produce a very different layout.

Saint, Figs. 7-1, 7-2.

Second, if Petitioner is correct on the law (and it is), there can be no legitimate dispute that Petitioner's proposed ground pad assignments were “suitable.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 415 (2007); *GUI Glob. Prods., Ltd. v. Samsung Elecs. Co.*, 2024 WL 1564694, at *4 (Fed. Cir. Apr. 11, 2024). Here, jumper bondwires were a “known technique” that “address[ed] a known problem” (viz., connecting pads) according to their “established function” as electrical conductors. Foty_Supp., ¶¶55-59, 79-82. Accordingly, “there is a motivation to combine.” *Intel*, 61 F.4th at 1380.

Moreover, real-life datasheets show flexible ground pad assignments. EX1032, 5 (various VSS/ground locations); EX1033, 38-41 (ground pads in middle

of row); EX1036, 9 (similar); EX1034, 3-4 (multiple ground pad configurations); EX1035, 28-33 (multiple VSS/ground pad configurations, including examples for the same chip with more and fewer VSS/ground pins); Foty_Supp., ¶¶166-173. PO's exhibit recognizes "package design is assumed to be flexible, such that there is complete independence in placing the [power and ground] pads." EX2013, 2; *id.*, 6 (showing multiple assignment options); EX1038, 169:25-170:11 (pad assignment is iterative), 171:17-24 (similar). Dubey is premised on re-assigning power/ground pads. EX2013, Abstract.

PO's cases (POR, 20) are easily distinguished. In *Polaris*, the proposed modification "undisputed[ly]" "[ran] contrary to one of Denney's stated purposes." 882 F.3d at 1069 n.4. By contrast, Petitioner's pad assignments further (rather than defeat) Yoshinaga's goal to "keep the chip [] small." Yoshinaga, [0084]. This also distinguishes *Fanduel*. And *Cutsforth* stands for the proposition that design choice turns on case facts. Here, the facts favor Petitioner. Unlike *Cutsforth*—where the modification rationale was "not alter[ing device] operation"—Yoshinaga discloses the connection between pads 5 and 6.

Third, Petitioner **did** explain why a POSITA would have made the proposed pad assignments. Pet., 31-32, 34-39. For example: (1) Yoshinaga shows ground pads electrically connected; (2) bondwires are a ubiquitous, affordable, and reliable means of connecting bond pads; (3) Saint teaches minimizing bondwire distance;

and (4) Petitioner's pad assignments preserve Yoshinaga's **saved area**, which Saint teaches is desirable to reduce die size. *Id.*, 46-47, 49-50; Foty, ¶¶200-204; Saint, 206-210 (“Keep your [bond]wires [short]”), Fig. 9-28; Foty_Supp., ¶155. Contrary to PO's assertion that Yoshinaga's **saved area** would “remain even without [Petitioner's] changes” (POR, 21), a metallization trace would defeat Saint's **saved area** rationale.

PO's assertion that Petitioner did not consider “chip size, the number of I/O signals, and the number of pads available” is baseless. POR, 20. The Petition, Dr. Foty, and Saint all discuss “core-limited” versus “pad-limited” designs (determined by chip size and pin/pad count) and their impact on pad location/assignment. Pet., 13; Foty, ¶¶49-50, 61, 100, 137, 322, 384, fns.12-13, 28, 30; Saint, 211-214; Foty_Supp., ¶¶26-33, 156. Yoshinaga's Fig. 6 IC is self-evidently core-limited; otherwise, it would depict more pads. Pet., 20-21.

4. PO's Strawman “Disadvantages” Argument Fails

PO asserts that Petitioner ignored “disadvantages” of its pad assignments. POR, 23-27. But the '164 patent identified no “disadvantages” of ground pads near

saved area[s].⁵ This is because PO's purported "disadvantages" are, at best, vastly overblown. Foty_Supp., ¶¶60-63, 69-78, 83-91, 158-173.

Citing Saint, PO asserts you "cannot arbitrarily change pads from unlabeled or supply pads to reference potential pads." POR, 23. But Saint Chapter 9 (titled "Packaging") merely says pads must align with package pins, so you cannot "blindly put [pads] wherever you feel like." Saint, 201-202. This comment about pad/pin **alignment** says nothing about pad **assignments**.

PO argues that "[r]eplacing 'power supply pads 3, 4, and 58' with reference supply pads and a Circuit 67 GND ... would have fundamentally altered and negatively affected [Fig. 6's] electrical operation." POR, 23. This argument fails for two reasons.

First, if Petitioner removed (instead of reassigned) power pads, modified Fig. 6 would show fewer pads, but it does not. *Compare* Yoshinaga Fig. 6 (42 pads) with Pet., 36 (modified Fig. 6 has 42 pads); EX1038, 292:19-293:5. Because supply pads could be assigned numerous locations among unused pads (Pet., 30-34, 20-23), Petitioner did not restrict reassignments to particular pad locations, nor is that material to the claims. Foty_Supp., ¶¶158-161. PO's cited testimony makes

⁵ Requiring more disclosure from the prior art than the Challenged Patent provides would create a double standard. *In re Epstein*, 32 F.3d 1559, 1568 (Fed. Cir. 1994).

Petitioner's point. POR, 27 (citing EX2011, 123:2-125:12). Far from removing power pads, Dr. Foty testified about relocating (*i.e.*, reassigning) them. EX2001, 123:19-21.

Second, because this kills PO's argument (POR, 23-27) about purported performance differences, power loss, noise, etc., PO misframes Petitioner's position as **removing** power pads. Foty_Supp., ¶¶158-161. But even with fewer power pads, many designs/chips function fine (*i.e.*, not all chips need 11 power pads, just like a house and apartment complex have different water needs). *Id.*, ¶¶161-173.

Yoshinaga is silent regarding block 1, 2, and 67 functionality. Dr. Khatri admits "Yoshinaga's teaching is not about ... circuit[s] 1, 2 and 67," which are "flexible." EX1038, 312:19-313:10. PO's contrary assertion is unsupported and relies on speculation that Fig. 6's generic chip is power limited. Accordingly, PO artificially restricts ground pad assignment based on unknown current requirements, "drive strength" limitations, power requirements, etc. that "possibly render[]" Fig. 6 "non-functional." POR, 24-26; EX2010, ¶¶51, 54; Foty_Supp., ¶¶161-173.

IV. PO's "SAVED AREA" ARGUMENTS FAIL

The file history makes clear that the **saved area** limitation was the reason for allowance. Pet. 17-18; EX1002, 230-239. PO and its expert ignore this. POR, 9-10; EX1038, 50:20-51:6, 279:18-23; Foty_Supp., ¶¶11-14, 26-33. But Saint disclosed this concept in 2002 (Saint, Fig. 9-28), and Dr. Khatri admitted "this is a

term that I’ve come across all through my career in my industry career, in my academic career, in my teaching career.” EX1038, 272:7:11; *id.*, 270:17-271:19, 264:8-20, 269:14-20. Nevertheless, notwithstanding that the POR never mentions Saint Fig. 9-28, PO attempts to distinguish each Ground as lacking a **saved area**. POR, §§III.C (Ground 1), IV.A.3 (Ground 2), V.C (Ground 3); Foty_Supp. ¶¶15-19.

A. The Claims Do Not Require “Creating” a Saved Area

PO argues the cited art fails to teach “**creat[ing]** a saved area.” POR, 45. But the Challenged Claims do not require “creating,” “forming,” or “adding” a **saved area**. Foty_Supp., ¶¶38, 43-44. Rather, they require that **the circuit area comprises at least one saved area**. See 1[f], 6[e], 8[f], 12[e].

If PO means that “creating” a **saved area** requires removing “filler cells” (POR, 8, 47), that improperly imports a limitation from the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1320 (Fed. Cir. 2005). Regardless, doing so would have been obvious using a pad template (explained *infra*). PO repackages the same argument as a lack of “motivation to combine,” asserting that “Saint teaches away from **creating** such a space, since it teaches ‘[making] the chip as small as possible.’” POR, 45, 47. But Saint teaches placing circuitry between pads to reduce chip size. Saint, 221.

PO asserts that “Petitioner fails to ... allege[] that Yoshinaga discloses [a *saved area*].” POR, 41. But the Petition says Yoshinaga’s orange highlighted areas are “each a *saved area*.” Pet. 39.

B. PO’s “Droop” Argument Fails

PO’s argument that running a bondwire over a *saved area* “contradict[s]” Saint and “risk[s] a short circuit and voltage drop” (POR, 45-47) is baseless. Foty_Supp., ¶¶83-91.

Because bondwires typically have lower resistance than metallization, they *reduce* voltage drop. EX1041, [0014]-[0015] (“jumper wire 160 ... may have a lower resistance than [on-chip paths]”); Foty_Supp., ¶¶61-63; EX1038, 143:3-12 (“metallization [resistance] dominates”).

PO asserts Saint “discouraged” Petitioner’s jumper bondwires because Saint teaches that “long” bondwires could “droop, causing a short [] circuit.” POR, 39 (citing Saint, 209). Understood in context, Saint says no such thing. Saint explains what it means for wirebonds to be “too long”:

[Y]ou cannot have a pad in the middle of the chip. The [bond]wires would be too long. If you were to route a long bondwire from the center of the chip out to the metal pins, the wire could droop down and short.

Saint, 204-205. Saint Fig. 9-16 provides another “too long” bondwire example. *Id.*, 210.

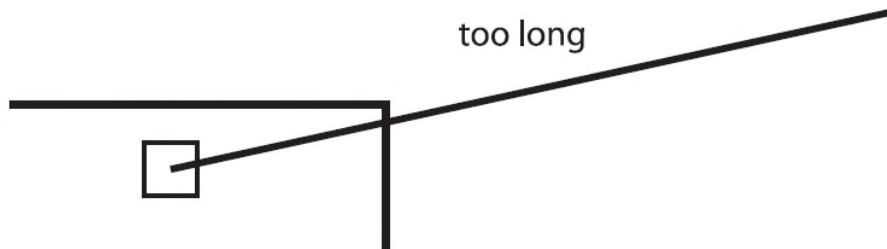
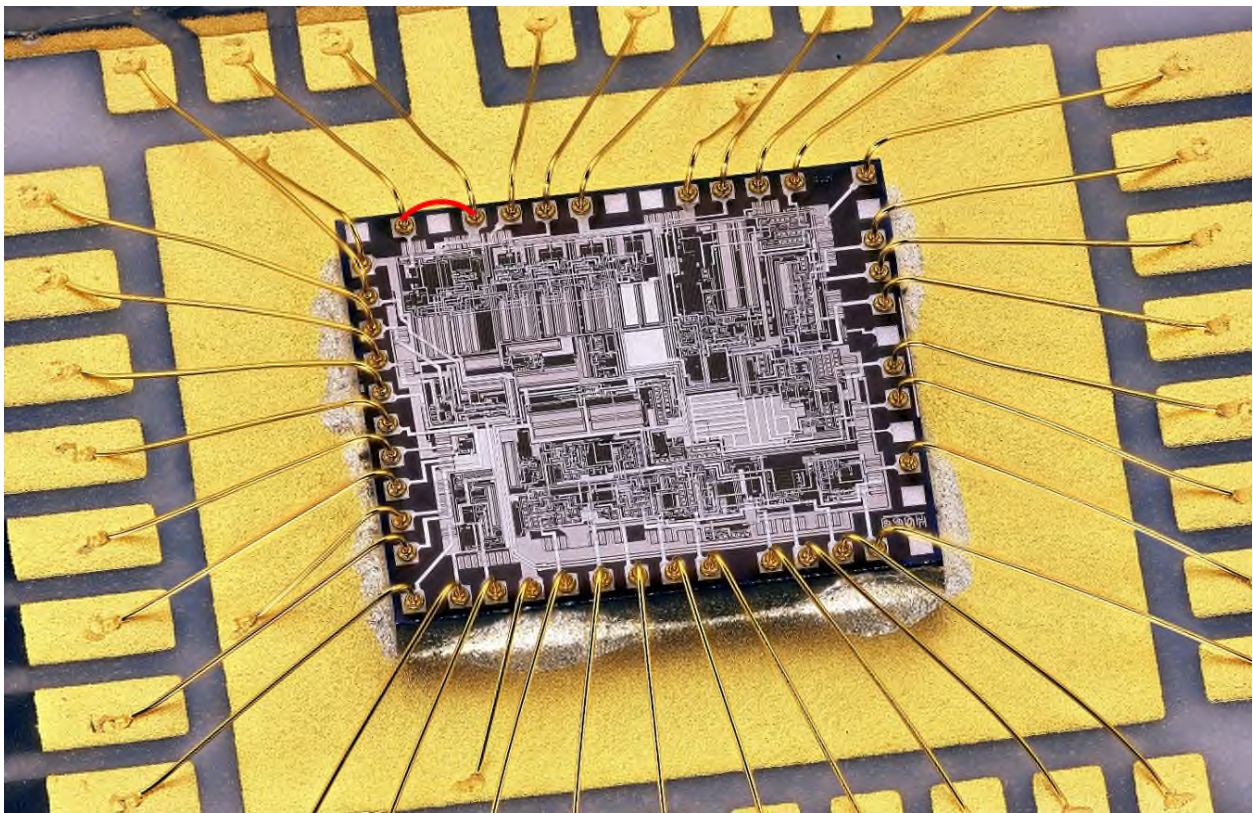


Figure 9–16. Keep your wires as short as you can. This stretch is probably not necessary. Plan your bond out before you begin your chip layout.

Id., Fig. 9-16.

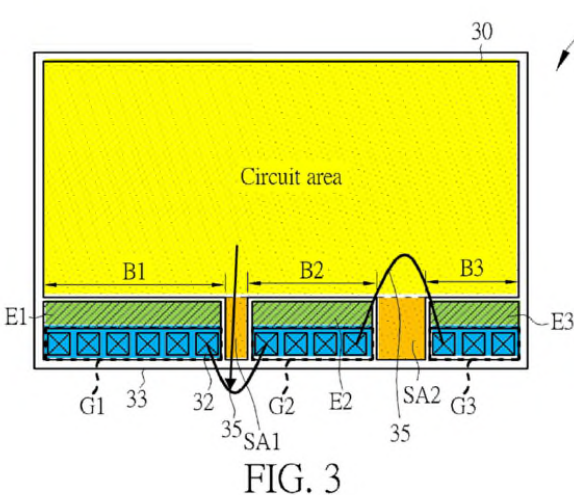
But the image below (at Pet., 13) shows the red jumper bondwire between bond pads (like Petitioner's proposal in Yoshinaga Fig. 6) is comparatively short and not susceptible to droop.



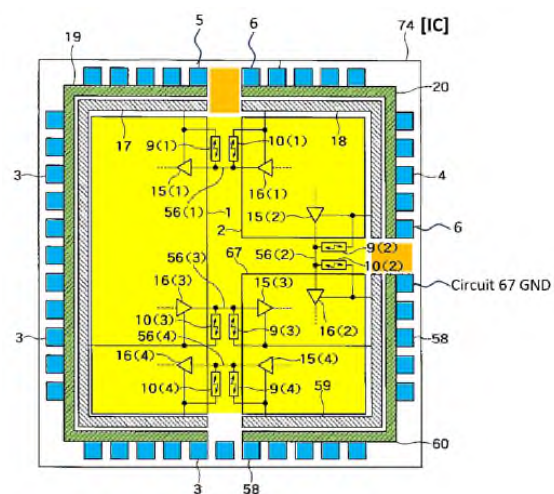
Moreover, Dr. Khatri admitted wirebond droop/sag concerns were solved by 2018. EX1038, 247:19-248:13 (“running bondwires ... had gotten good enough that conventional wisdom was not true anymore”), 246:13-247:8 (similar).

C. PO's “Circuit Area” Argument Fails

PO argues that Petitioner “ignores the requirement that the claimed ‘saved area’ must be within the circuit area.” POR, 41. But just as Petitioner highlighted '164 patent Fig. 3 (left) with orange to easily identify the *saved areas*, it did so with Yoshinaga (right).



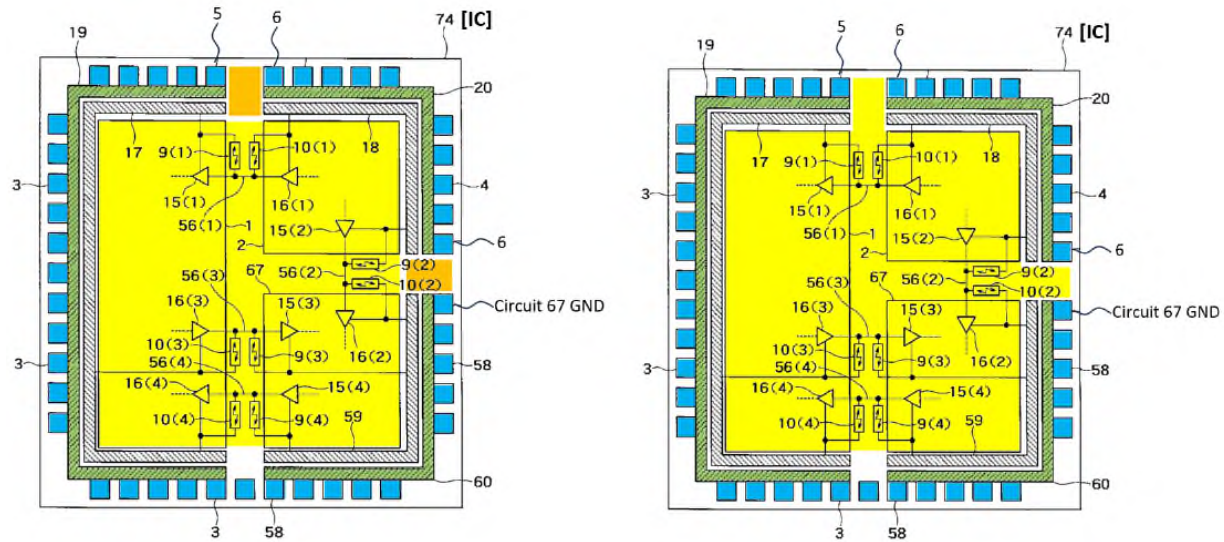
Pet., 16
(EX1001, Fig. 3, annotated)



Pet., 40
(Yoshinaga Fig. 6, annotated)

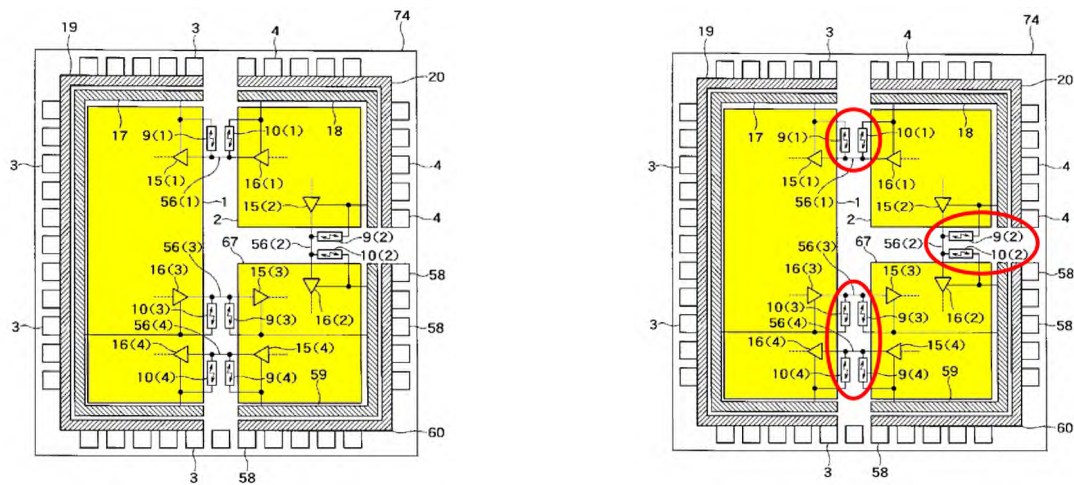
This does not “ignore” or contradict the requirement that *the circuit area comprises [a] saved area*. Indeed, “[a]nother way to conceptualize this is shown in a differently-annotated version of Figure 6 (on the right-hand side) – where the ‘saved

‘circuit area.’” Foty, ¶158.



Id. (side-by-side images of Yoshinaga Fig. 6).

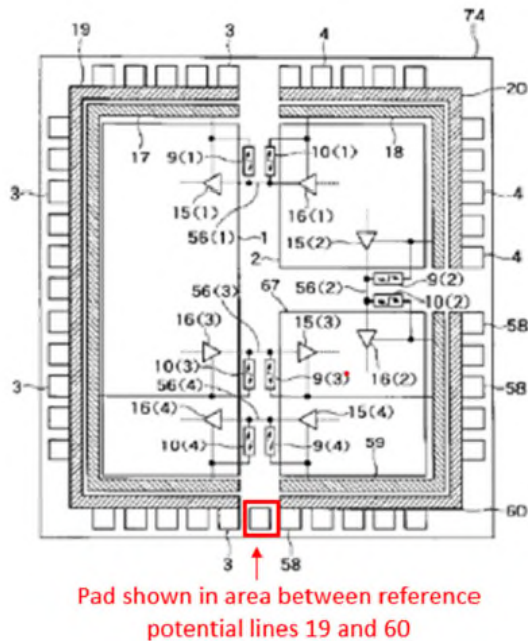
PO argues nothing outside of Yoshinaga's boxes 1, 2, and 67 (left image) can include circuitry. POR, 42. But Fig. 6 shows circuitry (*e.g.*, diodes 9-1, 10-1, etc.) (right image) outside those areas.



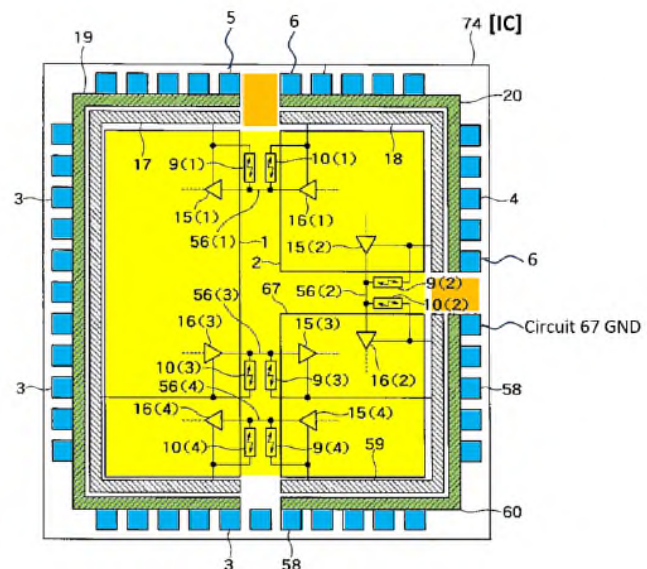
Yoshinaga, Fig. 6 (annotated).

D. PO’s Imaginary Pad Argument Fails

PO argues Petitioner “assumes, without support,” that Yoshinaga’s “[saved] spaces do not include a pad,” and thus fail the requirement of *no pad[s] in the ... saved area*. POR, 42. PO highlights a pad in Yoshinaga Fig. 6 (left image). But Petitioner never identified that region as a *saved area* (right image). PO’s red pad *contrasts* with Petitioner’s empty, orange *saved areas*, where PO implies a pad must exist.



POR, 44 (Yoshinaga, Fig. 6)
(PO annotation)

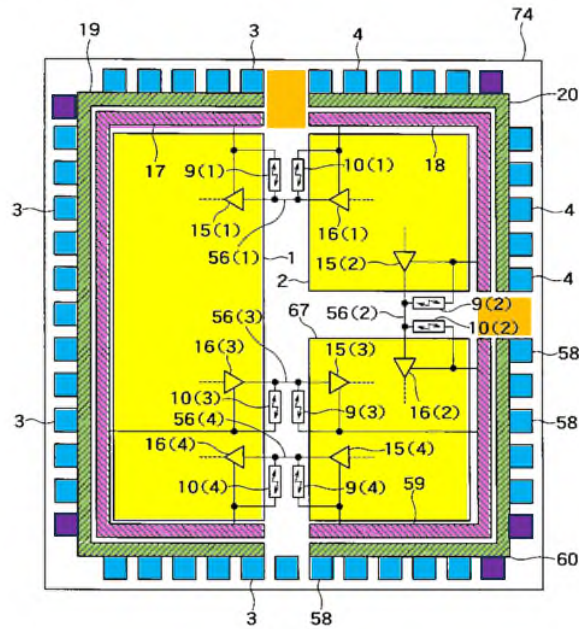


Pet., 40 (Yoshinaga, Fig. 6)
(Petitioner annotation)

Section III.B.4 addresses PO’s false premise that reference pads must be added. Even if more pads were necessary (they are not), Fig. 6 has room. Foty_Supp., ¶¶174-179. PO’s expert admits Yoshinaga has “10 potential locations”

for reference pads (EX2010, ¶102), including the purple locations below *outside* the *saved areas*.

【 図 6 】



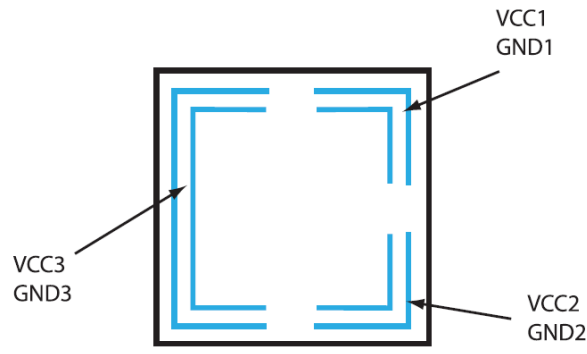
Yoshinaga, Fig. 6 (annotated).

PO's argument also fails because it incorrectly assumes Yoshinaga Fig. 6 is pad-limited.⁶ If so, pads would be illustrated in the purple locations and/or between the reference buses, but they are not.

⁶ Dr. Khatri failed to grasp the pad-limited vs. core-limited distinction. EX1038, 342:13-343:10.

E. PO's Hindsight Argument Fails

PO argues that Petitioner's pad assignments in modified Fig. 7-7 is "hindsight." POR, 67-69. Not so. This is neither "manipulation" nor "hindsight" because unmodified Fig. 7-7 shows a gap (viz. **saved area**) between ESD buses.



Saint, Fig. 7-7. Moreover, PO ignores that Fig. 9-28 places circuitry between pads.

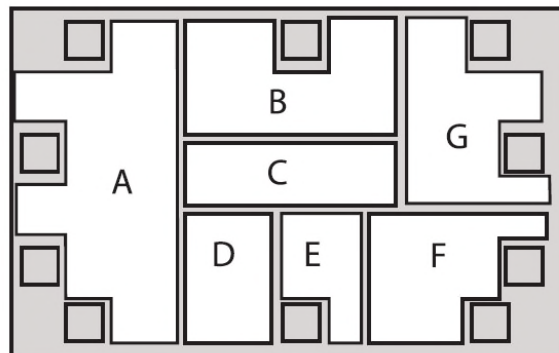


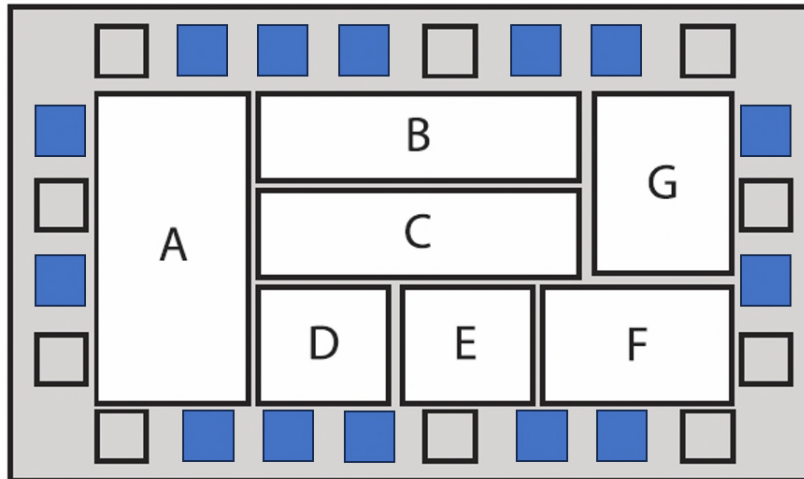
Figure 9-28. We can use extra space surrounding our pads to shrink our chip size.

Id., Fig. 9-28. Applying Fig. 9-28's pad placement teachings to Fig. 7-7 to preserve Saint's "extra space" benefit is quintessential obviousness, not hindsight. Foty_Supp., ¶25.

F. PO's Bodily Incorporation Argument Fails

PO's argument that Petitioner's modified Fig. 7-7 exceeds 16 pads (POR, 68) misses the point entirely. Foty_Supp., ¶¶17, 34-42. Like unmodified Fig. 7-7 (and '164 Figs. 2 and 3), Petitioner's modified figure is conceptual and not a bodily incorporation. *In re Etter*, 756 F.2d 852, 859 (Fed. Cir. 1985). Pad count is immaterial—**saved area** is what matters.

PO argues Petitioner's combination is improper because Saint teaches “evenly spaced” pads. POR, 68. But this ignores Fig. 9-28, which shows unevenly spaced pads. Illustrating blue dummy/filler pads (akin to empty parking lot stalls) shows that the actual pads (grey) are unevenly spaced.



Saint, Fig. 9-21 (annotated); Foty_Supp., ¶¶39-40.

G. PO's Chip Size Argument Fails

PO contends a POSITA would not apply Fig. 9-28's **saved area** teachings to reduce chip size because Fig. 7-7's pad groupings already “make[] the chip smaller.”

POR, 69. This makes Petitioner's point—*i.e.*, reducing chip size (and increasing profits) motivated IC design, as Dr. Khatri confirmed. EX1038, 257:9-14, 270:24-271:10. PO's assertion that Petitioner "add[ed]" area to Fig. 7-7 that "increase[s] chip size" misrepresents the Petition and Saint. POR, 69. Saint's *saved area* "shrink[s] chip size." Saint, 221.

PO argues Saint "does not address saving spaces between ESD buses or pad groups." POR, 68. But Fig. 9-28 discloses saved spaces between pads, and Fig. 7-7 illustrates empty space between ESD buses. Suggesting that a POSITA would not and/or could not combine these complementary teachings violates *KSR*. *KSR*, 550 U.S. at 418 (POSITA is not an "automaton"); *Foty_Supp.*, ¶¶25.

V. CONCLUSION

The Board should find the Challenged Claims unpatentable.

Respectfully submitted,

Dated: December 23, 2025

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITIONER'S REPLY BRIEF complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 5,598 words.

Dated: December 23, 2025

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