UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

vs.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case No. IPR2025-00118
U.S. Patent No. 10,879,164

REMOTE DEPOSITION OF SUNIL KHATRI

Wednesday, December 3, 2025

9:00 a.m. (MT)

Stenographically Reported by:

Joan Ferrara, RMR, FCRR

Job No. 2025-1001578

December 3, 2025

9:00 a.m. (MT)

Deposition of SUNIL KHATRI, held remotely via Zoom, before Joan Ferrara, a Registered Merit Reporter, Certified Realtime Reporter, and Notary Public.

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REMOTE APPEARANCES:

ORRICK HERRINGTON & SUTCLIFFE LLP
Attorneys for Petitioner
1000 Marsh Road
Menlo Park, California 94025
BY: TRAVIS JENSEN, ESQ.
tjensen@orrick.com

LATHAM & WATKINS LLP
Attorneys for Patent Owner
12670 High Bluff Drive
San Diego, California 92130
BY: B. TOM WATSON, ESQ.
thomas.watson@lw.com

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(REPORTER'S NOTE: All quotations from exhibits are reflected in the manner in which they were read into the record and do not necessarily denote an exact quote from the document.)

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SUNIL KHATRI,

called as a witness, having been duly sworn by a Notary Public, was examined and testified as follows:

EXAMINATION BY

MR. JENSEN:

Q. Good morning, Dr. Khatri. My name is Travis Jensen. I represent the Petitioner in this IPR proceeding and I'll be taking your deposition today.

A. Good morning.

Q. Let me just pull up the IPR number and just kind of read that into the record so we have the case number correct.

This is IPR No. 2025-00118.

Dr. Khatri, could you state and spell your name, please?

A. Yeah, my name is Sunil Khatri. My first name is Sunil, that's S-U-N-I-L. And my last name is Khatri, that's K-H-A-T-R-I.

Q. And where do you normally reside?

A. I normally reside in College Station, Texas.

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Q. And where are you located today?

A. I am today in Boulder, Colorado.

Q. Is anyone else physically present with you?

A. No.

Q. Approximately how many times have you been deposed as an expert witness?

A. That's a difficult question to answer, but I think it would be easily in the 30s, 30, 40 times maybe.

Q. Were those primarily patent cases?

A. Yes.

Q. Have you ever testified as a fact witness before?

A. Can you explain what that is? I think I know, but I just want to be sure I understand what the meaning of that term is.

Q. Let me just ask this: Have you ever testified in any capacity other than an expert witness?

A. I don't -- no, I don't think so.

Q. Okay. Have you ever been --

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well, strike that.

The patent being challenged in this IPR is U.S. Patent 10,879,164.

And I my refer to that as "the '164 Patent," is that okay?

A. That's perfectly okay.

Q. Have you ever been deposed on the '164 Patent before?

A. No, I have not.

Q. Have you and I ever met previously?

A. Say that again, please?

Q. Have you and I ever met previously?

A. I don't believe so, Travis.

Q. Do you understand that you are giving testimony today for an inter partes review proceeding?

A. That's correct, I do understand that.

Q. Even though none of us are in a courtroom today, are you aware that your testimony may be used as evidence before a panel of judges in this proceeding?

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A. I am aware of that, yes.

Q. Is there any reason you cannot give truthful testimony today?

A. No, there isn't.

Q. Even though you've been deposed a number of times, Dr. Khatri, I'd like to briefly review a few basics of how the deposition works so we're on the same page.

First off, this deposition is being conducted virtually, correct?

A. Yes, you're right.

Q. Using the Zoom app?

A. Yes, it is the Zoom app.

Q. Have any of your prior depositions been conducted remotely?

A. Yes, several of them.

Q. Okay. Will you let me know if you experience any technical difficulties today so we can address those?

A. I will, of course, yeah.

Q. And I'll just note that my internet, I get the little thing that says it's unstable, so I may be -- I may have

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my own technical difficulties just so folks are aware. Hopefully not.

A. And just also to let you know that I'm, you know, up in the mountains, so my internet might be unstable, particularly because it snowed about six inches last night. It is still snowing, actually.

Q. Well, I love to ski. I even have my sweater on. So I'm glad to hear that.

A. It's really pretty, yeah.

Q. All right. We had sent over -- and I apologize for the lateness of it -- a set of exhibits, basically PDF files that we wanted you to have available for you.

Were you able to access and download a copy of the PDF files?

A. Yes. I did receive a zip folder. I downloaded it and I have it open in front of me on my computer.

Q. Okay.

A. The folder open with all the, you know, the PDFs in it.

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Q. And there's a number of PDFs. Those are basically the exhibits that have been filed in the IPR. I know we'll use some of them, I doubt we'll use all of them, but we wanted you to have local access for any of the materials that we may ask about.

A. Okay.

Q. And I may use the screen share feature today to, you know, direct your attention to certain areas of the exhibits just by way of preview.

So the format of the deposition, as you know, is question and answer. If you find any of my questions unclear, will you let me know so I can try to clarify or rephrase?

A. I will do that.

Q. Throughout the course of the deposition, counsel for the Patent Owner may raise objections. If he does so, he's objecting to my question, not your answer.

However, unless you are instructed by your counsel not to answer

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on the basis of privilege, you must still answer my question.

Do you understand that?

A. Yes, I do.

Q. Okay. And importantly, we'll be taking periodic breaks. If you'd like a break at any time, just let me know and we'll do our best to accommodate as long as there is not a question pending.

Is that all right?

A. That's all right.

Q. Apart from the Zoom program and the, you know, File Explorer window where you have the PDF files, do you have any other applications open on your computer?

A. Let me just double-check. No. I have -- let's see, hang on. I had my email open. I'll close that.

So at this point, I have nothing open except the folder which, you know, the sort of the viewer that shows me the exhibits that you guys sent me and the Zoom window. That's still two applications that are opened on my screen.

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Q. Do you have any physical materials with you, like in printed hard copy?

A. Yes. You know, I did have the -- a physical hard copy unmarked, of course, of my declaration and that's something I printed and, you know, like beforehand. And I also have a physical copy of the '164 Patent. So I have these two physical objects in front of me.

And if you wish, if you prefer that I don't have them, I can take -- you know, but I'd like to have them, if possible.

Q. No, that's just fine.

Did you say there's no -- other than the documents themselves, there's no markings or annotations that you've added?

A. No. They just, you know, directly printed out and then stapled and that's it.

Q. What is the exhibit number on the '164 Patent that you have?

A. I don't know. Let's see. It

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doesn't say an exhibit number. I guess it must be the copy of the patent that I was using when I was doing all my review. At that time maybe it didn't have exhibit number and maybe I just download it or something from the internet. But, you know, it doesn't have an exhibit number.

Q. Okay. I believe that corresponds to Exhibit 1001 in this proceeding. Maybe just check in your local copies that 1001 is the same '164 Patent that you have the printed copy of.

A. Okay. Let me -- I just opened the Exhibit 1001 from the exhibits that you all sent me and it's the same as what I have, except that it has the exhibit number in the corner, you know, in the production. I mean, in my printout, I don't have that exhibit number. Let me just double-check. Seven pages. It's same thing, yes.

Q. And do you recognize that Exhibit 1001, the '164 Patent, as the YMTC patent being challenged in this proceeding?

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A. That's correct.

Q. Okay. Is this -- is the '164 Patent -- let me take one step back.

There are a number of IPR proceedings challenging various YMTC patents.

Are you generally familiar with that?

A. I mean, I'm not familiar with any of the details of that, but I'm broadly familiar with the fact that there's more than one YMTC patent.

Q. And you're serving as an expert in the IPR proceedings for some of the other YMTC patents that are being challenged, correct?

A. That's correct.

Q. Okay.

A. I --

Q. Go ahead.

A. No, that's -- that's a correct statement you made.

Q. And is it fair to say that the other proceedings where you're an expert

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on the YMTC patents, at a high level, deal with what's called, you now, 3D NAND flash memory?

A. That's a fair statement.

Q. Okay. And is the '164 Patent a 3D NAND flash memory patent?

MR. WATSON: Objection. Vague.

A. So, you know, the '164 Patent, you know, as the abstract, for example, says, right -- these were integrated circuit ESD bus structure -- just I'm reading the first line of the abstract -- you know, which includes a circuit area, plurality of ESD buses, plurality of pad groups adjacent and connected to the plurality of ESD buses, a common ESD bus and a plurality of bond wires configured to connect the plurality of pad groups to the common ESD bus.

So that's basically the abstract of the, you know, '164 Patent, talks broadly about what the space of technology that it addresses.

Q. Does it say anything about 3D

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NAND flash memory in the abstract that you just read?

A. In the abstract, I didn't see the words "3D" or "NAND" or "flash."

Q. Do you see those anywhere in the patent?

A. Off the back, I don't recall seeing them, but, you know, I doubt that there is -- and if you want, I can kind of double-check and look at -- look through the patent and see if I find that.

Q. We don't need to take the time to do that. I just wanted to make sure that we are on the same page, that this deposition concerns the '164 Patent and the IPR proceeding around that patent as opposed to the other IPR proceedings and the other patents where you're an expert that are, you know, more in the realm of 3D NAND flash.

A. I see. Yes, it is true that my understanding is that this deposition is about the '164 Patent.

Q. We're on the same page then.

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A. Excellent.

Q. Okay. Who is the named inventor listed on the '164 Patent, Dr. Khatri?

A. Let me see. The named inventor is listed as Zhiguo Li, and I'll spell that, it's Z-H-I-G-U-O. I'm not sure if I'm pronouncing it -- if I pronounced it right, but it's Zhiguo, and the last name is Li, L-I.

Q. Do you know that inventor?

A. No, I do not know that inventor.

Q. Before being contacted about working on this case, Dr. Khatri, had you ever heard of the '164 Patent?

A. I had not heard of, you know, of the '164 Patent before being contacted -- you know, before starting to work on this matter.

Q. Let's introduce a couple of more exhibits, and these are exhibits that have been premarked --

A. You mean from the folder, correct?

Q. From the folder and they've been

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filed in the proceeding, correct.

A. Okay.

Q. The first one is Exhibit 1006.

A. Just a second, 1006. Okay, I see it. And the numbers are all unique, correct?

Q. I believe so.

A. Yeah, okay. I have 1006 opened.

Q. Do you recognize that exhibit?

A. Let me look at it really quickly.

Yes, I do recognize Exhibit 1006.

Q. What is it?

A. It's a patent by, you know -- which is, where the inventor is someone called Yoshinaga and, you know, it's a patent that's used in some of the grounds of the, you know, of the petitioner.

Q. And this is the English translation of, I believe it was a Japanese --

A. Correct.

Q. Correct?

A. That's correct.

Q. Okay.

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A. It is an English translation and the original patent is Japanese.

Q. Do you know the inventor, Mr. Yoshinaga?

A. I do not know Mr. Yoshinaga.

Q. Next let's go to Exhibit 1007.

A. I'm going to close 1006, is that okay?

Q. Yeah, that's fine.

A. 1007, I'm just opening that. I see it. It's open now.

Q. Do you recognize Exhibit 1007?

A. I'll go over it really quickly before I answer that.

Yes, I do recognize Exhibit 1007.

Q. What is Exhibit 1007?

A. Exhibit 1007 is a U.S. Patent 9,070,700, which -- in which the inventor, one of the inventors is Haralabidis. That's H-A-R-A-L-A-B-I-D-I-S.

Q. And who is the other inventor listed on Exhibit 1007?

A. The other inventor is someone by the last name of Kokolakis. That's

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K-O-K-O-L-A-K-I-S, Kokolakis.

Q. Do you know either of the inventors on Exhibit 1007?

A. No, I don't know either of the inventors of Exhibit 1007.

Q. And going back for a moment, you don't need to open it, but Exhibit 1006, would it be okay if I refer to that as the "Yoshinaga reference" during the deposition?

A. That would be more than okay because that's how I've been referring to it in my head as well, so...

Q. Yeah, and pronunciation aside, I'll refer to Exhibit 1007 as the "Harold reference," is that okay?

A. That's perfectly fine as well.

Q. Okay. Let's look next at, if you can pull up Exhibit 1008.

A. Okay. Let me do that. Okay, I just opened that.

Q. Do you recognize Exhibit 1008?

A. Yes, I do.

Q. What is Exhibit 1008?

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A. So Exhibit 1008 is a book on, you know, IC mask design techniques and it's authored by Saint -- and Saint, like the two authors, both with the last name Saint.

Q. And are those Christopher Saint and Judy Saint?

A. That's correct.

Q. Do you know either Christopher Saint or Judy Saint?

A. No, I do not know them, either of them.

Q. Apart from your work in this proceeding, do you know Dr. Daniel Foty?

A. No, I didn't know of, you know, Dr. Daniel -- I don't know Dr. Daniel Foty. The only time I've come across him is when I read his declaration in this matter.

Q. Did you render any opinion on whether Dr. Foty qualifies as an expert in the subject matter of the '164 Patent?

A. I was not asked to and I did not provide any opinion about whether he,

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Dr. Foty, would qualify as -- you mean as a person of ordinary skill in the art, is that what you mean? Can I ask you to repeat your question because it was not completely clear to me.

Q. So you mentioned, I think at the outset, that you're testifying in the capacity of an expert witness in this proceeding, correct?

A. Yes.

Q. What is your understanding of what it means to be an expert witness?

A. It means that it's someone who is more than a person of ordinary skill in the art and who is familiar with the art at the time of the invention.

Q. Using that definition, did you render any opinion on whether Dr. Daniel Foty qualifies as an expert in the subject matter of the '164 Patent?

A. I see. So that was not something I was asked to do and I haven't provided such an opinion.

Q. Before I forget, you mentioned

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that you have a hard copy of your declaration with you, is that right?

A. That's correct, yes.

Q. What is the exhibit number on that document?

A. So that document -- I'm holding it up right now -- that document has the exhibit number stamp at the bottom right and it says it's Exhibit 2010.

Q. Okay. Thank you.

Are you aware there is a related District Court case involving the '164 Patent?

A. You know, I'm sort of familiar with the fact that there is because that's typically the case whenever there's an IPR, there's a District Court case that's filed on the same patent. So I'm aware to that extent and I might have heard -- I might have heard about it or something like this.

Q. Have you issued an expert report on the '164 Patent in the District Court case?

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A. No, I have not.

Q. Have you been deposed in the District Court case?

A. Do you mean the District Court case for the '164 Patent?

Q. Yes.

A. I have not been deposed for the District Court case for the '164 Patent.

Q. How many declarations did you prepare for this IPR proceeding?

MR. WATSON: I'll just counsel the witness just to avoid revealing any privileged information and just answer the number of declarations that were provided to the PTAB.

THE WITNESS: Understood.

A. So the number of declarations that was submitted to the PTAB would be two, you know, this being the second.

Q. And when you say "this being the second," are you referring to Exhibit 2010 that you have with you?

A. Yeah, I'm glad you clarified that. Yes, Exhibit 2010 is the second

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declaration that I filed in regard to the '164 IPR, and there was one declaration I filed before this one.

Q. Was your declaration, Exhibit 2010, intended to replace your previous declaration?

A. In a sense. You know, the previous declaration was just the declaration of the -- you know, for the preliminary response, preliminary -- the POPR. So it was a declaration in support of the POPR.

And this, you know, this declaration 2010 is a declaration in response to the DIPR as instituted.

Q. And can you confirm that the hard copy, Exhibit 2010 that you have, is the same as the electronic version that we provided?

A. Let me do that real quick. Hang on.

I'm going to randomly look at some pages and see if they match completely with the hard copy that I have.

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(Pause.)

So I randomly checked maybe about 20 pages in my hard copy of the 2010, Exhibit 2010, as well as the soft copy of the Exhibit 2010, and they seem to be matching. So it looks like my hard copy here matches with the soft copy of Exhibit 2010.

Q. And those are both 95 pages long?

A. I did verify that, yes.

Q. And that's your signature -- I'm sorry, go ahead.

A. I did verify the total page count and also several pages. Like, I did verify that about 15 or 20 pages matched exactly, and I do confirm that it's my signature at the last page, page 95, on both documents.

Q. If we need to refer to your POPR declaration, Exhibit 2007, I'll specifically note that, but will you understand otherwise that if I refer to your declaration, that I'm referring to the Exhibit 2010?

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A. That's a fair -- that's fair.

Q. When you submitted your declaration, did it contain a complete and accurate statement of your opinions regarding the validity of the challenged claims in the '164 Patent?

A. May I ask you to repeat that question, please?

Q. When you submitted your declaration, did it contain a complete and accurate statement of your opinions regarding the validity of the challenged claims in the '164 Patent?

MR. WATSON: Objection. Vague.

A. So when you say the exhibit, just to confirm, you mean -- sorry, when you say the declaration, you mean the Exhibit 2010, the POR declaration, correct?

Q. Yes, that's -- maybe I can take one step back and just double confirm.

Going forward, will you understand that if I refer to your declaration, I mean Exhibit 2010?

A. Yes. But just, I know you said

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that, but I just wanted to double-check.

Q. That's fine.

A. So yes, Exhibit 2010, all the declaration, is a -- you know, represents my opinions, you know, in response to the petition and the declaration of Dr. Foty.

Q. What is the date that you signed and submitted your declaration?

A. I'm going to have to look at the last page, page 95 of the declaration. It was on September the 17th of this year.

Q. Have any of your opinions regarding the validity of the '164 Patent changed since submitting your declaration?

A. No. My opinions haven't changed.

Q. When was the last time that you reviewed your declaration?

A. The last time I reviewed the declaration would have been yesterday. Just a brief eyeballing of it today as well.

Q. At the outset, I always like to ask if there are any errors, I'll say apart from typos, that you'd like to

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correct. So is there anything that has come to your attention that you would like to correct in your declaration?

A. There's nothing that I want to correct. I mean, there are no factual errors that I found while reviewing the declaration. So I don't have any other -- you know, any corrections. There my be a typo here or there, but unsubstantial. And if we run across that, I'll point it out.

Q. Thank you.

Have you submitted any errata sheets to your declaration?

A. No, I have not.

Q. When preparing your declaration, were there any materials that you would like to have reviewed, but did not have access to?

A. Did you say this was while preparing the declaration?

Q. Yes.

A. No, I didn't have -- I mean, I had all of the material, you know, and

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documents and such that I, you know, would have needed to prepare this declaration.

Q. Without revealing any privileged information, what did you do to prepare your declaration?

A. So, you know, I -- you know, I'll sort of, you know, the steps I followed, right, are sort of partially described in my declaration. So let me point you to that one paragraph which gives you sort of an idea of how I went about this.

I'm just looking for that. One second.

So if you look at my declaration, page 16, paragraph 22, you know, it's about the legal section, talks about -- it tells me -- it talks about my understanding of the law, because I'm not a lawyer. And it says that, you know, the first thing I did was I, you know, is -- the steps of checking validity is a two-step process. The first step is that the patent claims are construed to ascertain the proper scope.

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And then the second step is that the construed claims now are compared to be identified prior art to determine if the claims are valid with the prior art.

So broadly, I did those two steps. The first step is, you know, I construed the claims, which means I read the '164 Patent, you know, you know, in the spec, as well as the claims.

And, you know, construed the claims, that's the first step. Then I looked at the, you know, the declaration of Dr. Foty, as well as the petition to see if those construed claims when compared with the prior art that they cited are valid with the prior art.

So that's the overall steps I followed in preparing the report.

Q. Who prepared the first draft of your declaration?

A. So the declaration, the words of the declaration are all mine, you know. This is basically, you know, I formed theories based on reading the petition --

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on the patent, the petition and Dr. Foty's declaration and any supporting documents.

You know, I formed the theories, I formed the opinions about, you know, about what you find in the report.

So these words are mine. There may have been some portions of it where the attorneys gave me some help in terms of draft, you know, formatting and, you know, writing it in a nice legal manner and so on, and making the citations nice and legal and that kind of stuff. But the words are mine and the opinions here are all mine.

Q. Who else, if anyone, assisted in preparing your declaration?

A. I mean, if they had some paralegals' help in checking cites and so on, I have no idea.

So, you know -- you know, I mean, I don't know, you know, if there were paralegals involved in that. So I could not answer your question precisely.

Q. Did any lawyers assist in

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preparing your declaration?

A. Again, like I said, you know, there was formatting help and like, you know, citations, using the citations in the right way -- I mean, in the right sort of formatting and stuff.

So who did that exactly, I'm not completely sure.

Q. Did Mr. Watson, who is here at your deposition today, assist in preparing your declaration?

A. It's possible that he did some of it. He might have handed it over to someone else. I don't know. I don't have a clear view as to how the, you know, the -- how things were sort of done in -- how do you say -- in the law firm, I guess.

Q. Were there any non-legal personnel that assisted in preparing your declaration?

A. Did you mean legal personnel or non-legal personnel, sorry?

Q. Were there any non-legal

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personnel that assisted in preparing your declaration?

A. I have no idea if there were -- you know, I mean, nobody assisted me. These are my words and my opinions.

Q. Yeah, that's what I was getting at, you don't have an assistant or a grad student or somebody like that that helped you?

A. No, absolutely not, no.

Q. Okay. Is it fair to say that if there are any errors or mistakes in your declaration that those are your errors and mistakes?

A. Yes. These words are mine and so any errors are mine.

Q. Did you rely on anything the patent owner's counsel told you when preparing your declaration?

A. I think that -- that's too vague of a question to answer. Can you rephrase it? I don't understand what you're trying to ask.

Q. Yeah, let me take another crack

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at that.

A. Okay.

Q. And maybe it's easiest to give an example.

In your report, you set forth a -- I don't recall the specific title, but I'll call it a legal standard section. Is that correct?

A. Okay, yes.

Q. Where did the legal standards that you used in your declaration come from?

A. So the legal standards is something that I was -- that were explained to me, correct. So this is like a few pages of legal standard questions that I have.

Let me just go to those pages really quick. So that starts page 15 and goes through, you know, page 19.

So these were -- you know, these were standards that were explained to me. Some of the standards, you know, I asked them to draft because I didn't understand.

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And I made sure that I understood what was being, you know, what was written. And if I had any doubts, you know, I would sort of ask to change the language and make sure that before I approve and sign, I understood the words in this section.

Q. And you're referring to the section that spans paragraphs 21 to 31 in your declaration?

A. Let me double-check. The section titled "Understanding of Legal Standards" at Section 3 starts paragraph 21 and, correct, it ends on paragraph 31.

Q. Who informed you of the legal standards that are included in paragraphs 21 to 31 of your declaration?

A. So this was something that the attorney I'm working with, you know, told me about. And some of these I already knew from past cases and stuff. I mean, substantially these are something I already knew.

So some of them are not new to me. You know, and therefore, you know,

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this section is not something that -- having done some IPRs and other district court cases and such, you know, these paragraphs from 21 to 31 weren't completely foreign to me.

And I say that while I freely admit that I'm not a lawyer. So these are things I've encountered before, is what I'm saying.

Q. So you mentioned that you have experience in other IPRs and proceedings and so have some familiarity with the legal standards in that section, correct?

A. With some of the legal standards. I wouldn't say all of them. But, you know, I have some familiarity, but not a lawyer's familiarity with any of this, of course.

Q. When forming the opinions in your declaration, did you apply any other legal standards not listed in your declaration?

A. Any legal standards that I've applied would be listed here.

So as a follow-up to the last

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question, can you give me an example of what you're referring to? Like, you know, you said something about did I apply any legal standards that are not listed here. Can you give me an example maybe?

Q. I didn't have anything particular in mind.

A. Okay. Because I just want to make sure if it's just a commonsense standard that it's fair to be, you know, like fairness is important, something like this. And if I didn't write it here, I don't want to say that that's something I didn't opine on. Do you know what I'm saying?

So if it's a tautological sort of standard, right, which is just commonsense, then I want to make sure that I don't -- you know, I mean, I want to say that I applied my commonsense as well.

Q. Is your commonsense a substitute for a legal standard?

A. Absolutely not.

Q. Okay. And I didn't have anything

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particular in mind.

A. Okay.

Q. Just because you've mentioned you've done a lot of other proceedings, so I wanted to make sure if you were bringing along something from another matter that I had the chance to ask you about it and be aware of what that was.

A. I understand the question now and thank you for clarifying.

Q. Going back to Exhibit 1008 for just a moment -- let me make sure you've got that in front of you if you'd like to look at it.

A. I'm just going to open that. That's the same exhibit, correct?

Q. That's correct. I should say, is it okay if I refer to Exhibit 1008 as "Saint"?

A. That would be great.

Q. Did you render any opinion in your declaration on whether the Saint reference does or does not qualify as prior art?

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A. I did -- I mean, I responded to the use of Saint in, I guess, all the grounds of the petitioner and in Dr. Foty's declaration.

So, you know, I responded to it because they had used it as prior art. They had cited it as prior art -- "they," as in the petitioner and Dr. Foty.

So they had cited it as prior art, and I responded to that as it being prior art.

I don't believe I explicitly, you know, provided an opinion about whether Saint qualifies as prior art.

And if I'm incorrect about it, you know, you're welcome to show me in my declaration where it says that I opine on whether Saint is prior art or not.

Q. No, I didn't see it, but I just wanted to --

A. Okay.

Q. -- because I didn't see it.

Can you look at -- and the page numbers I'll use here kind of throughout

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the deposition, or the page numbers that are in the bottom right-hand corner, kind of we call that the endorsed or the stamped page numbers -- so can you turn to page 4 of Saint?

A. Hold on just one second.

So, by the way, my declaration uses the page number on the top left, the blue numbers, right. So, you know, I will have to translate those when I, you know, when I talk about my page numbers in Saint.

Sorry, you said let's look at page 4?

Q. Yeah, page 4. I think this one should be easy because there is no other page number on it.

A. Yeah, yeah. So this is on the right side, correct?

Q. Yeah, on the lower right.

A. I see that now.

Q. What is the copyright date that is listed on page 4 of Saint?

A. The copyright date is 2002.

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Q. Do you have any basis on which to dispute that copyright date?

A. Disputed as in -- I mean, in what sense, "dispute"?

Q. In the sense that the Saint reference was not published as of the copyright date in 2002.

A. Oh, I see. I have no reason to say or to opine on whether Saint was published or not published by that copyright date of 2002 on page 4.

Q. You could put that aside or close it if you'd like.

A. Okay.

Q. Going back to some questions about your declaration, approximately when did you first start working on this IPR?

A. That's really a difficult question. I really wish I could answer it, but, you know, my memory is hazy about that.

I mean, clearly it would be before September the 17th, that's kind of obvious. And so before the date of my

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POPR response. So I wouldn't be able to answer that.

Q. When did you first begin working on your declaration?

A. Let's see. Sometime before it was submitted. So again, you know, I don't kind of keep track of these things because they're sort of -- sometimes I work in bursts, you know, there will be more activity today, then there will be a little gap, and then I'll work again.

So if you ask me when I started working on this particular declaration, I wouldn't be able to give you a good clear answer.

But, you know, it's -- this is a long-drawn process of reviewing things and coming up with theories and then starting the declaration, the drafts and such.

And then there be a little bit, there will be bits of gaps between them because I might have been moving from College Station to Boulder or, you know, or, you know, or I had some other cases I

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was working on, or I had some academic duties I was working on.

So, it's kind of like a big mix and it's hard to really tell when exactly I started to work on something.

Q. Who is the patent owner in this proceeding?

A. I wouldn't -- this is sort of a legal question. I'll tell you why it's hard for me to answer. Because I have been -- I've sort of been an expert in cases where whenever it says assignee, the patent owner is somebody else because the patent has changed hands and has been sold or something.

So I really don't know technically and precisely who the patent owner would be.

What I can tell you is that the patent assignee for the '164 Patent, which is listed on the front page of the patent -- and I have this here, the printout of it, as I mentioned to you.

But that patent owner -- I'm

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sorry, that assignee is, applicant and assignee, is listed as Yangtze Memory Corp. -- Technologies Corporation Limited. So that would be the YMTC company, I think.

Q. Who is the patent owner that you list on the first page of your declaration?

A. Oh, yeah. That's the Yangtze Memory Technologies Company Limited. So that sort of matches with the assignee. So that makes me assume that the patent owner and the assignee here are the same.

Q. And that's who you refer to with the abbreviation YMTC?

A. That's how I -- you know, that's how I've been, like, in my documents, my folders and so on, I just say YMTC.

Q. And I do the same, so I'm happy to use that acronym, it's a little bit shorter.

A. Right.

Q. And approximately how many legal matters have you been retained by YMTC?

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A. This is the first time I've been retained by YMTC for any legal -- I mean, for my patent matter. That would be the, you know, the two IPRs that I'm currently an expert on.

Q. So just to make sure I understood that correctly, you've only been hired by YMTC in two legal matters?

A. I believe that's correct, yes. And that's the -- you know, that's the '164 Patent and then there's this other patent. So there's just two IPR matters.

Q. What did you do, Dr. Khatri, to prepare for today's deposition?

MR. WATSON: I'll just counsel the witness not to reveal any privileged communications between him and legal counsel.

THE WITNESS: Sounds good.

A. So to prepare for today's deposition, you know, I read, you know, the material of the IPR -- you know, I read my declaration. You know, I read any supporting documents that I cite in my

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declaration. Just kind of went over that and made my notes and such.

That's sort of the methodology I used on my own when I was preparing for this deposition.

Q. Approximately how much time did you spend preparing for today's deposition?

A. I don't know if I'd be able to tell you that precisely, but it was spread out over a bunch of days. You know, there would be days I'd work a little bit and I'd get tired and stop, or some days I work a little more.

Overall, I don't know because it was spread over several days. And then there was Thanksgiving in between, so...

I don't have a good, precise, you know, like amount of time that I could tell you in terms of how much I worked in preparation for this case, for this deposition.

Q. Would you say it's more or less than 10 hours?

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A. I mean, I think it would be certainly more than 10 hours, but I don't know -- I mean, I wouldn't know more precisely than that.

Q. Would it be more than 30 hours?

A. No. It's hard for me to sort of give you a more precise number, so...

But definitely more than 10 hours. I think that's a fair statement.

Q. Could it have been more than 100 hours?

A. Again, I've not logged all this stuff, so I couldn't really tell you. But 100 hours does sound like an awful lot. But again, I just don't know.

Q. Did you meet with anyone to prepare for your deposition?

A. Yes, I did.

Q. Who did you meet with?

A. I met with counsel, you know, Tom Watson.

Q. Anyone else?

A. That's all.

Q. How many times did you meet with

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Mr. Watson?

A. I guess, let's see, this probably would be two times, two times that we met.

Q. Were those meetings in person or remote?

A. No, they were remote. I actually don't know where he is. But yeah, it was remote on Zoom.

Q. And approximately how much time did you and Mr. Watson spend in these meetings?

A. I think it would have been a few hours, on the first day maybe two or three hours, and then the next day five or six hours, something like this.

Q. Apart from Mr. Watson, did you mean with anyone else to prepare for your deposition?

A. No, I did not.

Q. In preparing for your deposition, did you review any documents that were not already part of the proceeding?

A. Let's see. I'm trying to understand what you might mean by that.

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So are you saying any references that were not part of what was filed?

Q. Correct.

A. For example, what is not in one of your -- one of the PDFs that you have sent me?

Q. That's a good way to ask it. In preparing for your deposition, did you review any documents or materials that are not among the PDF files that we provided?

A. No, I didn't review anything that's outside of what I say is my materials considered.

Q. Did you review the '164 Patent to prepare for your deposition?

A. Yeah, the '164 Patent was also part of what I considered in -- you know, in my -- in my declaration.

Q. Did you review the file history for the '164 Patent in preparing for your declaration or your deposition?

A. Let me see. I don't -- I've gone over it tangentially at one point, but I don't think that was an issue that was

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brought up and is not something that I've opined on.

So, I didn't look at it in any great detail. But I do recall seeing it a long time ago.

Q. Can you turn to paragraph 23 of your declaration.

A. Okay. Let me do that. Yes, I'm on page -- paragraph 23.

Q. And this is in the Section 3 titled, "Understanding of Legal Standards," correct?

A. That's correct, yes.

Q. Okay. And in paragraph 23 you set forth your understanding of the legal standard for obviousness, is that correct?

A. Let me read this -- let me read this paragraph again before I answer your question.

So I've read this paragraph. May I ask you to repeat your question?

Q. Yeah.

Is this the paragraph where you set forth your understanding of the legal

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standard for obviousness?

A. It does talk about obviousness and, you know, how that works.

Q. Let me ask you to open Exhibit 2007.

A. 7?

Q. Yes, 2007.

A. Okay, I'm opening 2007. I have it open now.

Q. And what is Exhibit 2007?

A. Let's see. So 2007 looks like the declaration I filed as part of the patent owner preliminary response. It's kind of what it looks like. Let me look at it real quick.

Yeah, I do think it looks like the first thing -- the first declaration that I filed along with -- it's sort of supporting the POPR.

Q. And what is contained in paragraph 22 of Exhibit 2007?

A. So, in Exhibit 2007, there's a section called Understanding of Legal Standards that starts paragraph 20 and

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finishes on paragraph 29.

And you're asking about paragraph 22? And I'm going to just read that really quick.

Okay. I've looked at that. May I ask you to repeat your question -- or did you have a question yet or --

Q. Yeah. What is paragraph 22 of Exhibit 2007?

A. Paragraph 22 is another paragraph in the Understanding of Legal Standards, you know, that was presented to me or that was explained to me.

Q. Was paragraph 22 in Exhibit 2007 provided to you by counsel?

A. Correct. This was something that was presented -- this was something that was explained by counsel, you know. And essentially that was repeated to me.

Now, maybe in transcribing it, I might have changed -- you know, might have used slightly different language or something. But basically this is what was described to me about the legal standards

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for, you know, for being obvious.

Q. And is that the legal standard that you applied when forming your opinions in Exhibit 2007?

A. You know, this would have been the standard I applied. And I mean, you know, again, like I said, I'm not a lawyer. So the language I use might have been, you know, not completely the same in both -- in Exhibit 2007 versus 2010.

Q. Are paragraphs 22 in Exhibit 2007 and paragraph 23 in Exhibit 2010 the same?

A. It doesn't -- like, I mean, facially when I look at them, one of them looks a little bit larger. There's probably -- you know, there's a slight difference, it seems like.

Q. Yeah, so that was my question. Why is there a difference in the obviousness legal standard you provide in Exhibit 2010 and the one provided in Exhibit 2007?

A. Yeah. So it's, again, you know, like I said, you know, when I transcribe

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some of this, I use -- you know, I mean, I use my knowledge of my recollection of the discussion. It might not be the same.

But so one difference that I see in paragraph 23 of Exhibit 2010 to paragraph 22 of Exhibit 2007, you know, is it says that -- Exhibit -- sorry, paragraph 23 of Exhibit 2010 says: While such conclusions are often based on more than one piece of prior art, only one is required.

Now, that's something that I didn't say in paragraph 22 of Exhibit 2007.

But then, you know, in my past work, you know, using -- in my past work as an expert, I have seen that, you know, sometimes people use one prior art reference and sometimes they use more. So I kind of know this.

And in some sense, this difference is moot because in the matter at hand, you know, there is no ground that the petitioner has used, which only uses

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one prior art reference.

So this difference that I see is sort of a, you know, a moot difference. It's a minor difference, but it's a moot difference for the matter at hand.

Q. If it's irrelevant, why did you go to the trouble of adding it to Exhibit 2010?

A. It was like -- you know, I mean again, like I said, this is my -- you know, my recollection. So this is the fact -- you know, the fact that I added it has no consequence or bearing to this case. Because there is no ground in which the petitioner uses one prior art reference.

Q. Did you make that change based on something that patent owner's counsel told you or did you just pull that in from your experience in other cases?

A. It's just something that, you know, I added saying, you know, to just make it complete.

So it was not something that had

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any great, you know, sort of reasoning for it. It's just like, hey, you know, sometimes people use one draft, and so let me add that, you know.

There is no real -- there's no reasoning that caused that -- caused me to add that line.

Q. You just did it at random?

A. I wouldn't say it's random, but it's just that I thought let me make this more complete.

Q. You can put Exhibit 2007 to the side or close it if you'd like.

A. Okay, I'll do that.

THE WITNESS: We've been going for about an hour. May I request a little break?

MR. JENSEN: That's fine. Let's go off the record.

THE WITNESS: Okay.

THE COURT REPORTER: We're off the record at 10:03.

(Recess taken from 10:03 a.m. to 10:10 a.m. MT)

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BY MR. JENSEN:

Q. Welcome back, Dr. Khatri.

A. Thank you.

Q. Let me direct your attention to paragraph 26 of your declaration.

A. Okay. Let me see that. 26, correct?

Q. Yes.

A. Just one second. Yeah.

Q. And could you just read allowed the first sentence of paragraph 26, please.

A. Yes. It says, the first sentence of paragraph 26 of my declaration, Exhibit 2010, says: I have been informed by counsel that obviousness must be determined as of the date of the invention, i.e., the effective filing date or priority date of the patent, which in this case is November 1, 2018.

Q. So what is the relevance of the November 1, 2018 priority date?

MR. WATSON: Objection. Vague.

A. I don't know what you mean by

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that question, as in what's --

Q. Are you familiar with the term "effective filing date and priority date" that you use in paragraph 26?

A. This is something that, you know, it's a very patentee's kind of thing, it's very specific to patents. They have things like priority dates, filing dates and then, you know, branches of, I guess branches of patents and so on. And all this, not being a lawyer, but I've always had difficulty understanding those dates and how they're computed.

So I always defer to the attorneys for those dates. And so basically, you know, this paragraph -- this line of paragraph 26 just says that, you know, this is basically a result of what I would have asked the attorneys, like hey, what is this date that I am looking at. And they would have told me it's November 1, 2018.

Now if you ask me how I came up -- how I would come up with this or how

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someone comes up with this date, I wouldn't be able to give you a good answer, because usually on the face of a patent there are many dates and I have a hard time understanding which of them is the relevant one.

So whenever I do a new IPR or District Court matter, I always ask the attorneys just tell me what's the date that I'm supposed to, you know, that I'm supposed to use as my -- sort of the reference date, if you will.

And I was told that this is November 1, 2018.

Q. Yeah, and I'm not quibbling with the November 1, 2018 date.

A. Okay.

Q. The question I have is, why does that date, you know, whatever it is -- and here, let's just go with November 1, 2018 because that's what you list -- why is the November 1, 2018 date relevant in this case?

A. You know, like I said, right,

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like I'm trying -- you know, it's always my effort to be complete -- excuse me -- to be complete in my reports, in my declarations and reports.

So when there's something like this, you know, I'll say, you know, let's just mention it because that's the date I would use for determining if something is prior art or something is not. It's kind of a check -- it's kind of a way to check if something is a prior art, you know, artifact or not, I guess.

Q. What do you mean when you say in paragraph 26 that "obviousness must be determined as of the date of the invention"?

MR. WATSON: Objection. Vague.

A. So, you know, in my understanding, right, and this is my recollection of the discussion I had and the understanding that was provided to me -- so in my understanding is if you're checking for obviousness of, you know, of a patent, then you must -- there's a

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determination of obviousness that you're trying to do, right, which is basically, you know, like what I've described in paragraph 22.

So it says, you know, I first construe the claims to ascertain their proper scope. And second, the construed claims are compared to the identified prior art to determine if the claims are valid over the prior art.

So now, you know, what is prior art, for example? Like, in this exercise, you know, you have to put yourself in the -- in the timeframe that is basically the effective filing date or priority date of the patent that I've listed or described in paragraph 26.

Q. So in this case you would not perform the obviousness analysis as of, you know, December 3, 2025, which is today, correct?

A. I mean, yeah, that's kind of what it says. So it says that the obviousness must be determined as of the date of the

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invention, which is November 1.

So, for example, if you have a person of ordinary skill in the art, that would be someone who is defined as of this date. You know, all the entire process of doing the analysis should be sort of grounded in this date.

Q. So in this case you would not perform the obviousness analysis as of 1999, for example?

A. I mean, if it is -- you know, the statements that is quite clear, right. It says that you have to perform the obviousness -- that obviousness must be determined as of the date of the invention, which is November 1, 2018.

So if you took 1999 as your date, then the person of ordinary skill in the art would have different skills. That technology might not have even existed. That is why the date that is listed here is important.

Q. Okay. Let's move to paragraph 27 of your declaration, please.

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A. Okay, I'm there.

Q. What is set forth in paragraph 27 of your declaration?

A. Let me read that really quick and then I'll be ready to answer your question.

(Pause.)

Okay. And what was your question?

Q. Yeah. What is paragraph 27 of your declaration?

A. So let me read it first and then I'll tell you how I understand it.

So it says: I have been informed by counsel that obviousness can be established where a skilled artisan merely pursues known options from a finite number of identified predictable solutions.

So it essentially says that if you had a finite number of identifiable predictive solutions, then, you know, a skilled artist can pursue options from that to establish obviousness.

And it says: I have been further

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informed by counsel that evidence of obviousness, especially when that evidence is proffered in support of an "obvious-to-try" theory is insufficient unless it indicates that the possible options skilled artisans would have encountered for finite, small or easily traversed and that a POSITA would have a reason to select the route that produced the claimed invention.

And again, you know, this says what the words, you know, plainly describe, right. It says if there's evidence of obviousness, you know, if that evidence is offered, you know, as a theory that just says, oh, this would be obvious to try, it would be obvious to try something -- well, that's insufficient unless, you know, unless it indicates that the possible options that the skilled artisan would have had would have been small, would have been finite, small, and easy to sort of traverse or easy to explore.

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And also the person or ordinary skill in the art should have had a reason to select that, you know, to select those options.

So again, what is stated here is sort of like more or less -- you know, it's just what the words describe.

Q. Is there a similar paragraph that appears in the Legal Standards section of Exhibit 2007, which is your POPR declaration?

A. Let me see that. I'm not sure. I have to check. 2007, you said?

Q. Yes.

A. I don't believe I see such a paragraph here.

Q. I didn't see it either.

So the question I have is: Why did you include paragraph 27 in your POR declaration, Exhibit 2010?

A. Correct. So, you know, the reason was, like I was saying before, right, like, it's always to be more complete. So if I wanted to be more

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complete and if I added a paragraph or I added a clarification, you know, in my legal section of the Exhibit 2010 compared to 2007, that's just to be more accurate and more precise.

And in this case, in particular, there was -- you know, when I was reading -- when I was reading the petition and declaration of Dr. Foty in more detail, there was an instance that came up where they were saying something about, oh, this is just obvious to try.

So that's why I would have asked the attorneys like, wait a minute, is it just okay to have -- for someone to say it's obvious to try this or is there some legal sort of underpinning behind that, you know, is there some sort of legal requirement in that.

So that -- this paragraph came up as a result of that situation where I noticed that there was a place in the petition that said, well, this would be obvious to try, and Dr. Foty's

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declaration.

So I asked for a clarification of the standard around something like that, and this was explained to me.

Q. Is it fair --

A. Again, it's to make things more clear. That's about it.

Q. And we looked earlier at an example in paragraph 23 where there was a change and you said, well, it makes no difference to my opinions.

Is paragraph 27 similar or different than that example? In other words -- strike that, let me ask a better question.

A. Okay.

Q. Do any of your opinions in your declaration depend on the legal standards set forth in paragraph 27?

MR. WATSON: Objection. Vague.

A. So the opinions I feel depend on the entire Legal Standards section because I don't have -- I am not a lawyer, so I have no -- I mean, I don't have, you

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know -- I'm not informed about the law other than from this section.

So in some sense, this section, this section which is Understanding of Legal Standards, is my guideline, right. And as needed, sometimes I'll ask for clarifications. I think that's just me being more precise in my reports.

Q. Could applying an incorrect or incomplete legal standard affect your validity opinions?

MR. WATSON: Objection. Form.

A. You know, I would say that, you know, like in forming my opinions, I have used these, you know, the legal standards that I've listed in the Understanding of Legal Standards section.

So that's basically, you know what I've said, because that's something that I'm informed by the attorneys, by counsel to use as my, sort of like my guideline in my analysis.

Q. So if you were given a different legal standard, could your opinions be

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different?

MR. WATSON: Objection. Form.

A. You know, once again, right, as I've been saying, like, you know, my -- I'm not a lawyer myself. So basically the legal standards that I use are informed by the -- you know, by what the counsel sort of informed me about the legal standards.

MR. JENSEN: So I move to strike that as nonresponsive.

Q. I'll ask the question again: Could your opinions be different if you were provided a different legal standard?

MR. WATSON: Objection. Form.

A. The opinions I provided are based on the legal standard that you see here. I mean, the legal standards that you see here are basically, you know -- you know, the legal standards in Exhibit 2010 are from paragraph 21 through paragraph 31. And these are the standards I used to form my opinions.

You know, this is my understanding of the legal standards and

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that's what I've been -- that's what I've been -- that's what I've been using. It's not like they're any different than before. It's just that there have been clarifications of something that I didn't have an understanding before.

So these standards are quite consistent with, you know, with anything I've done in my past cases and so on. So there is no -- and these are the standards I use, but these standards aren't, you know, different than anything else I've been -- that has been told to me by counsel in the past or in this case.

Q. Have you rendered any opinions on obviousness in this case under a different standard than what is set forth in paragraphs 23 to 31 of your declaration?

A. Let me -- you mean 23 to 31, or 21 to 31? Can you repeat that question, please?

Q. Sure.

Have you rendered any opinions on obviousness in this case under a different

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legal standard than what is set forth in paragraphs 21 to 31 of your declaration?

A. So the opinions I provide in this declaration, Exhibit 2010, are based on the Understanding of Legal Standards that are presented in paragraphs 21 to 31, both inclusive.

Q. Were you informed of the legal standard that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results?

MR. WATSON: Objection. Form.

A. I don't understand, you know, what you're saying.

Now, it is quite possible -- so it's quite possible that you're citing from some book of law or some textbook of law or something, which as I said, I'm not an attorney. And it's quite possible that when parsed, that's exactly what something in my understanding of the legal standards says.

So it's possible you're using

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different legal language and I'm not a lawyer, so I won't be able to give you an opinion on what you just said because if I was to parse what you said. It's quite possible it's just something that I've already stated in my Understanding of Legal Standards in paragraphs 21 to 31.

So I won't be able to give you an opinion on that because it just says very lawyer-ish to me and it just sounds like something you're reading from a legal textbook, which I'm not familiar with.

Q. And I'll represent to you I'm reading it from the Supreme Court.

A. Which is extremely hard for me to respond to because I'm not an attorney.

Q. But you had no problem applying the legal standards as set forth, which may also come from legal text in paragraphs 21 to 31 of your report?

A. So the description in paragraphs 21 to 31 are, if you will, sort of the humanized version, I guess, of the legal standards that you all might be reading

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from Supreme Court guidance, you know.

But this is basically, you know, how it was explained to me and how I understood it as someone who is not an attorney.

Q. You mentioned that you've served as an expert in a number of other IPRs previously, correct?

A. That's a fair statement, yes.

Q. To your knowledge, has the PTAB ever given your testimony little weight because they found it not credible?

A. I have no idea. I don't have any idea about that.

Q. Did you serve as an expert in IPR 2021-179 between Google and Singular Computing?

A. I don't know the IPR number that you're talking about, but I did serve, you know, in the IPR of Google versus Singular.

Q. Do you know what the outcome of that IPR was?

A. Usually, I don't know. But I

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mean, the case went forward, that case went forward, and it went to trial. So I'm assuming that the IPR was, you know, was successful. But I don't know that for a fact. You know, all I'm saying is I know the case went to trial and I was the expert for the trial as well.

Q. Can you turn to paragraph 25 of your declaration?

A. Paragraph 25, yes, I'm there.

Q. You got there faster than I did.

A. Because I have a hard copy, so...

Q. What do you discuss in paragraph 25 of your declaration?

A. Let me read that real quick.

(Pause.)

I see. So it essentially says -- I'll just read it out and then I'll also like explain it.

I think your question was what was my understanding of paragraph 25, correct?

Q. Yeah, just what topic do you discuss there.

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A. Okay. In paragraph 25 -- I'll just read it to set the background. It says: I've been informed by counsel that an obviousness determination includes several factual inquiries, including, 1, determining the scope and content of the prior art; 2, ascertaining the differences between the claimed invention and the prior art; 3, resolving the level of ordinary skill in the pertinent art; and 4, taking into consideration any objective indicia of non-obviousness.

So essentially this is saying that when you went to, you know, when you want to do a determination of obviousness, that you need to take into account, you know, several facts -- you need to conduct several factual checks or inquiries and four of them are listed, you know -- you know, four of these inquiries are listed.

Q. And yeah, let me kind of drill down and focus your attention on the fourth one and that's the one that says: Taking into consideration any objective

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indicia of non-obviousness.

A. Okay.

Q. What are secondary considerations or objective indicia of non-obviousness?

A. Okay. So I don't know that they're also called secondary indications -- did you say indications?

Q. Well, let's just stick with the exact phrase.

A. Okay. So suppose we --

Q. What are objective indicia of non-obviousness.

A. Got it.

So objective indicia of non-obviousness are some objective indicia as in factors or indicators. They're objective indicators of non-obviousness of a patent.

So, for example, one of them could be, like, let's say there was -- I come up with an invention and people start copying it. Well, copying is considered an indicia of non-obviousness because if it was not obvious -- I mean, it's only

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then that someone -- some competition -- some competitors would start to copy it. So that's one objective indicia of non-obviousness.

I mean, there's a list of them. I might not remember them all. But another one, another objective indicia of non-obviousness is, you know, is something where people initially say, you know, your idea is really, really bad. So let's say there's a lot of press that says, Sunil comes up with some invention and there's a lot of press or sort of a lot of, you know, a lot of sort of other people in the field that say, oh, that's just really a dumb idea.

And then if I come up with -- you know, if I'm able to produce that invention and show that it's really successful, then that's, you know, that's basically another of the objective indicia.

Or also another objective indicia would be where there's praise. So

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industry experts, you know, write a blog or write an article that say, you know, someone came up with -- you know, what a fantastic idea or something like that. So that's another objective indicia.

All of these -- I mean, there are a few more maybe, I don't recall them all, but I think I've given you three -- two or three of those, but they are objective because they're verifiable and they're indicia or indicators that my invention was not obvious.

So this is sort of, like, if I parse this, right, it's like what are objective indicators that my patent was not obvious that -- you know, and some of these are what I listed.

There are a few others. I didn't write them all down, they were sort of explained to me, but I didn't see a need to write them all down.

But I think I've given an idea of what some them are and what the overall idea of these objective indicators of

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non-obviousness entails.

Is that -- is that sort of -- do you see what -- anyway...

Q. When forming the opinions in your declaration, did you take into account and analyze the objective indicia of non-obviousness that you just mentioned?

A. So, like I said, in forming my opinions, I used, you know, all the -- all the legal standards that I've described from paragraph 21 to paragraph 31 in my declaration, which is Exhibit 2010.

And, you know, you know, they all kind of contributed to my opinion.

Now, if I didn't explicitly write something about one of these standards, it just means that they were -- you know, it doesn't mean that I didn't use that standard. It just means that, you know, I used in totality all the legal standards that I've described from 21 to 31 -- from paragraph 21 to 31 in -- you know, as a whole.

Q. So you mentioned, you know, one

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example of an objective indicia of non-obviousness was copying, correct?

A. That's what I -- that's what I understand, yes.

Q. Where in your declaration did you discuss copying?

A. So, I mean, you just asked me, like, what is the meaning of objective indicia. Your question was what was the meaning of objective indicia of non-obviousness.

And my answer was, you know, what that generally means, it means objective indicators of non-obviousness, right. And I gave you a few examples.

Now, I didn't say that I explicitly use one example, you know, in forming my opinions or not.

I'm just saying here are what -- I mean, my answer was simply to provide with you some of the objective indicia that are commonly used.

Q. Yeah, so I want to make sure I understand, you know, if you do or do not

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have an opinion on the specific objective indicia of non-obviousness that you identify.

Starting with copying, do you render an opinion in your declaration that anyone copied the '164 Patent?

A. So, you know, as far as I recall, I don't think I've used that copying instance. But if you have something in my declaration that you'd like to point to me, I'll give you an opinion specifically on that, I'm happy to be directed to that paragraph of my declaration.

Q. All right. I didn't see anything about copying, which is why I wanted to ask, just to confirm.

Do you have an opinion, one way or the other, on whether anyone copied the '164 Patent that is included in your declaration?

A. So that's something that I'm not, you know, aware of in some sense because, you know, again -- you know, in terms of -- if we talk about the infringement

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matter, there may be a situation about copying, I have no opinion on that. So I'm not making any opinions about, you know, about copying in any context for this '164 -- for this '164 Patent.

You know, my opinions are restricted to what you find in the 95 pages of Exhibit 2010.

Q. Did you include anywhere in the 95 pages of Exhibit 2010 an opinion on whether anyone in the industry had praised the '164 Patent?

A. Once again, you know, if I didn't -- if I did say that, I'd like you to point me to where that, which paragraph that might be in. Could you point me to where in Exhibit 2010 it might say that there was praise?

Q. I didn't see it anywhere. I'm just asking if I overlooked something.

A. I see.

Q. Do you have an opinion on -- that anyone praised the '164 Patent?

A. Again, in the -- in the specific

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task that I was asked to do, which is to provide an opinion about this IPR, I have provided no opinion about whether there was, you know, whether there was copying or whether there was praise.

Now, there may have been praise or there may have been copying and this might be in documents I was not -- I haven't seen.

So I'm not saying that there was. I'm not saying there wasn't. I'm just saying that I have no opinion about those specific, you know, indicia.

Q. So let me ask the same question about, I think the other indicia that you mentioned, which is kind of skepticism.

Did you render any opinion in your declaration that people in the industry were skeptical of the solution that was presented in the '164 Patent?

A. Once again, if you interpret something that I wrote as an indication of skepticism, feel free to point it out to me and I'll opine on it.

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Q. Again, I didn't see it, but I just want to confirm because you did say that you took into account, you know, objective indicia of non-obviousness generally, and so I'm just drilling down on the specifics to understand, you know, whether there are individual instances of skepticism, praise, copying, et cetera, that you did opine on and, you know, I, for whatever reason, had just missed it in the declaration.

A. So I'll answer then in two ways. I don't believe I used the word "skepticism" specifically in my declaration.

Now, to the extent that, you know, to the extent -- I mean, so as you just said, you know, in your definition of skepticism, I haven't sort of given any evidence of skepticism. So there's really nothing for me to respond to in terms of the skepticism comment because, in your definition of skepticism, I've not expressed any skepticism in this

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declaration.

Q. Do you know if anyone has licensed the '164 Patent?

A. I am not aware of that, it's just something that -- I mean, I have no opinion. I mean, I have no opinion on it. I just don't know.

Q. And did you ask, did you investigate whether anyone had licensed the '164 Patent?

A. I didn't ask that and it was not part of -- it's not within the realm of the opinions I was asked to provide.

Q. And let me ask maybe just a broader question: Do you discuss anywhere in your report specific instances of the objective indicia of non-obviousness that support your conclusion that the challenged claims are not obvious?

A. It was a long question. I didn't quite parse it. Can you repeat it, please?

MR. JENSEN: Maybe, could the court reporter read that back so I

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don't mess it up?

(The requested portion was read back by the Court Reporter.)

THE WITNESS: Thank you.

A. So, you know, again, if -- so my response to that would be if you have a specific instance where you think I opined on -- where you think my opinion is based on any of the objective indicia, please feel free to point that out to me and I'll opine specifically on it.

Q. Yeah, and I didn't see any examples. That's the reason I'm asking. If I had one, I would direct you to it.

A. Perfectly fine.

So based on your response, you know, that you haven't seen anyplace in my report where there was -- where I was, you know, leaning on the objective indicia of non-obviousness to, you know, to form my opinion, based on that, I don't have any other way to respond to that because there's no -- there's nothing that you're pointing at to me to say that, you know,

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here's an instance of where you used one of the objective indicia.

So based on your response, I don't have anything to say.

Q. Yeah, so rather than rely on something I said, let me just ask you, Dr. Khatri: Can you point me to any examples in your report where you identify objective indicia of non-obviousness that supports your invalidity conclusions?

A. So in my conclusions, I don't explicitly, you know, cite objective indicia, any of the objective indicia of non-obviousness.

But that said, it is quite possible that I might have implicitly used it, but I just -- you know, not being a lawyer, I don't know that I am actually using one of these objective indicia. And that's why I asked you the question, because in your wisdom and in your sort of knowledge of the law, I wanted to know if there was anything you thought I was using which could be construed as me using one

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of the objective indicia.

So that's kind of why I'm leaning on that to answer your question.

Q. Did you perform any testing as part of forming your opinions?

A. Can you be more specific? I think that's very open-ended.

Q. Yeah. Did you test any products or devices when forming your opinions in your declaration?

A. No, I did not test devices or products.

Q. Why not?

MR. WATSON: Objection. Form.

A. In some sense, you know, like the -- in this IPR, the grounds that were used by petitioner and Dr. Foty, they were exclusively patents, they were exclusively, you know, patents and textbooks. So there were no products involved, so in the grounds that were cited by the petitioner or the -- or Dr. Foty.

So, therefore, I did not see any

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need to investigate products or to look at products. Because there were no products pointed to or referred to or used as -- or used as, you know, as references or artifacts that the petitioner or Dr. Foty used in support of their -- of their petition.

So therefore, I didn't -- I didn't see a need to do any testing of products because there were no products mentioned in the petition or in Dr. Foty's report.

Q. Did you perform any simulations when forming the opinions in your declaration?

MR. WATSON: Objection. Form.

A. I didn't perform any simulations, but I relied -- I mean, as I say in my, you know, in my report, I rely on my knowledge of about, I think it's maybe around 30-something years in the field to form my opinions.

And in this 30 years, I've done multiple simulations in multiple contexts.

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And, you know, and the task of doing those simulations and the difficulty it entails and so on is something that I'm aware of and that's -- I mean, I use my knowledge in forming my opinions.

Q. All right. Let me direct you in your declaration to paragraph 4.

A. Okay. I'm there.

Q. And this is under the heading Roman I, Background and Qualifications, correct?

A. Correct, the section is Background and Qualifications, yes.

Q. And that section spans paragraphs 4 to 17 in your declaration?

A. Let me check. Correct, the section called Background and Qualifications spans paragraphs 4 through 17, both inclusive.

Q. And you also submitted a CV, I believe it was with your POPR declaration -- and you could look at that as Exhibit 2006 if you'd like.

A. Okay. I mean, would you like me

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to look at it? Is there something specific about it you want to ask or --

Q. I have several general questions, but yeah, if you want to just open that up and confirm that Exhibit 2006 is your CV, that would be great.

A. Exhibit 2006 does seem to be my CV and just -- yes. It's one that's updated in 2024.

Q. Was that CV created for purposes of this IPR or is that a more general CV that you use across, you know, a broader range of matters?

A. It's a CV -- it's my academic CV. So it's my CV I use for academic matters and I update it two or three times a year. So this is a little old because it's updated in April of 2024.

Q. Are you an inventor on any patents, Dr. Khatri?

A. Yes, I am.

Q. And are those patents listed in your CV?

A. They should be. Let's see. Let

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me go find them.

Here they are. So let's see, what page is this -- page 30 of my CV lists patents. Some of them are applications -- like, sometimes I don't know the difference between all these, I don't know how you all classify these, but that's a list of patents and/or applications and there's a couple more provisional patents we have filed in the last year, which probably don't show up here.

Q. Do any of the patents or patent applications listed on page 30 of your CV deal with ESD circuitry?

A. I don't -- let me see. Let me look. I don't believe any of the patents -- let me look real quick. I doubt it, but I'll double-check.

So the patents listed on page 30 of my CV don't deal with ESD circuitry.

But that said, I have extensive industry experience. You know, this was at Motorola where we were designing the

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world's fastest microprocessor at the time. It was called the 88110 microprocessor.

And in that process, in the process of design, you know, I was -- I designed the I/O drivers for that chip -- we have a patent on that. You can see that as patent -- let me see where that is -- yeah, that's Patent 05448182, driver circuit with self-adjusting impedence matching.

Now, the subject of that patent was an I/O driver, which basically adjusted its impedence dynamically. It self-adjusted the output impedence.

But I implemented this for our chip as well. That was, you know, was something I did. And in doing that, I was -- you know, I designed the ESD structures for it. They were the fast structures, the slow ESD -- we designed all the ESD structures for the I/O driver that was the basis of the patent that you see which is self-adjusting impedence

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matching.

So I have familiarity with, you know, with ESD structures, you know, from my work -- from all the way back from my work at Motorola. So I'm familiar with the models they use for testing ESD structures like, you know, Yoshinaga mentions some these models as well.

And then after this, as part of a -- as a faculty member, I have done, one, two -- I think three, three -- let me just check -- three separate integrated circuits that we've fabricated interest my group.

So, in other words, you know, I have three chips, if you will, that we have fabricated. And in each of these chips we had, you know, we had I/O drivers, we had input pads, output pads, supply pads, reference pads and so on, all of which had ESD structures in them, and I was -- you know, I was directing the students in terms of designing the ESD structures for those -- you know, for the

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circuit pads for those three chips as well.

So even though the patent -- I don't have specific ESD patents. I have extensive familiarity with, you know, with ESD, the models for ESD, the qualifications for ESD, the testing of ESD and also the design of ESD structures that are efficient and, you know, that would -- that would survive -- you know, survive the -- survive the chip being out in the wild. Because once the chip is out in the wild, ESD does become a problem.

Q. And what does the acronym ESD stand for?

A. It stands for electrostatic discharge.

Q. I should have mentioned that before using the acronym.

A. Oh, that's all right.

Q. What were the three chips that you mentioned you supervise your students designing and fabricating?

A. Yeah. So actually, I think I

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supervise it and -- it's maybe more than supervise because there would be sometimes where I jump in and say let me just take care of and I show them and teach them how to do it because it's just too far away from their background and experience, so I'll just sort of get in there and get my fingers -- you know, get my hands dirty and have them out, right. So it's more than sort of supervise.

But back to your question, what were the three chips that we fabricated? I'll have to recall.

But the first chip -- let me see.

The first chip was a subthreshold, it was a subthreshold -- what do you call it -- like a subthreshold BFSK transmitter. So BFSK stands for binary -- actually, sorry, it was BPSK, so binary phase shift keying. That's a way of doing communication between two parties.

So this used subthreshold logic, which was something that we, you know, in

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my group we had done extensive work on and extensive papers and so on that we've submitted. So something that I'm pretty proud of.

So we did this binary BFSK transmitter chip, which actually, interestingly, was supposed to be put on the back of a cockroach. So we would basically use a cockroach to walk around and we have something that senses and then it transmits it through this little very low power chip which is a subthreshold chip.

So the property of subthreshold circuits is that they are extremely low power and that's why this research project would find itself on the back of a cockroach, sort of the real genesis of this project.

So that was the first chip. It was a BFSK transmitter, which we fabricated, came back, where the chip came back. And, of course, in doing this, we had to create the ESD structures for the

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I/Os of this chip.

The chip came back, it was successful, and so on. That was the first chip.

The second chip was something that they called an MCA, and that stands for a multichannel analyzer. And this is basically something they use in nuclear radiation detection. So when you have a radiation detector, you have some detection sort of circuit, which detects the strikes of alpha particles or beta particles or gamma particles or whatever. It detects individual strikes. And it converts those strikes into some physical quantity, like a pulse of light or a pulse of electricity or something like this.

So basically once you get these pulses, you want to determine how big were the pulses, because that tells you about the energy of the particle or how frequently are the pulses occurring, because that tells you about the flux of the radiation.

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And all that back-end competition is done by something called a multichannel analyzer. That kind of tracks the number of pulses and what energies they are and pins them and can give you a little histogram of the energies of the particles that you detected.

So I had this collaboration with folks in nuclear engineering and nuclear radiation detection lab, a government lab, and we built a full chip -- we built a single chip multichannel analyzer. Previously, this was a circuit that was scattered across many chips -- I mean, many chips. So it was bulky, it was clumsy to design, it consumed a lot of power.

So we took all that and shrunk it down to one chip, one chip, a single chip, multichannel analyzer, and that was sort of like the claim to fame of this circuit was, that it did everything in one -- it did everything in one chip.

And once again, in this chip,

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there was I/O pads, of course, there was power supply pads, reference pads and so on. And so there was always a need to do ESD structures, which we, you know, which we did.

And in these two chips that I mentioned, I was quite involved in the ESD stuff as well, among other things.

And then the third chip -- and there's going to be a fourth soon, but I won't talk about the fourth -- the third chip is an alpha detector.

So in some sense, it has these tall, long fingers of material in silicon processing that's called diffusion. So you have like these tall fingers of diffusion. And there's little things -- I mean, there's little structures sticking out of these fingers. And these are like, you know, I like to call them like a frog with a tongue sticking out.

So if there's an alpha particle that hits this chip, it will get -- it will strike one of these diffusion

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tongues, if you will.

And once it strikes a diffusion tongue, we have circuitry that will basically amplify that detection and send it to a central area in the chip where all these strikes are -- I mean, are counted, so we can know how many strikes we had and we can sort of talk about the flux of the alpha particle field, like the number of alpha particles per unit, per unit area and so on.

And the importance of this chip was that a normal alpha detector is pretty large and so we were basically able to shrink it down to a single chip which was literally about 5 millimeters by 5 millimeters. And so this large detector could now fit in the form factor of a credit card, for example.

So these were the three chips, all of which -- even in the third chip we had I/O pads, as any chip does, and power supply pads, reference pads, and so on.

So ESD structures are a common

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feature for all these chips, the three chips that I did as a professor as well as the chip that we did, you know, at Motorola, the 88110 disk microprocessor chip.

Q. And were those chips that you mentioned manufactured using a CMOS process?

A. Let's see. So the -- yes, all of them were CMOS, complimenting MOS chips.

The third chip, right, used sort of -- the diffusion sort of structures, the diffusion tongues that I talked about, which were capturing the alpha particle strikes, they were either PMOS or NMOS, I forget exactly which. So that chip was more leaning towards one or the other.

But, you know, the counting -- it did have a circuit area where all the strikes were counted and added up and stuff. That was purely CMOS.

But the actual detectors were analog and they were -- I forget, they were NMOS or PMOS, one of the two.

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Q. Roughly what were the time periods that you were working on these different chips? Starting, let's take the Motorola one first, sounds like maybe that was the one you mentioned first, what was the timeframe that you were working on the Motorola 88110 disk chip?

A. Again, the Motorola chip was -- when I was at Motorola was -- while I was working at Motorola, that was the time from 1987 to '93. So that would be that timeframe.

And then the first -- the subthreshold chip would be somewhere in the 2010s. I could be wrong. These are just guesses now.

And then the MCA chip, the multichannel analyzer chip, would have been in the late '20s.

Let's see. Late -- sorry, late 2010s, sorry. So it would be twenty -- I don't know what, '15, '16, '17, something like this.

And then the last chip, which was

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the alpha detector chip would be a little bit later than that, maybe close to 2020 or something.

So they kind of span about -- these chips span about 20-odd years.

You know, in addition to that, you know, these were the actual chips that they build. But I have a circuit design course that I've thought that -- I have an undergraduate circuit design course, which I've taught a few times and a graduate version of the circuit design course.

So in both these courses I've covered, you know, circuit design technique, including I/O drivers, including ESD, I kind of teach the students the different ways of doing ESD structures and so on.

So in addition to the four specific chips where we actually fabricate something, there's this continuous process of me in class, you know, covering ESD, among other things, in the process of teaching the students about -- teaching

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the students about chip design.

And also, you know, right now I'm on sabbatical, but when I go back and start teaching again in the fall semester of 2026, I'm currently developing a course which I'll offer in fall of 2026 to be a graduate and an undergraduate course. This course will have in it something -- it's called chiplet-based design. It's like those Chiclets which were the chewing gum, but it's with a "P," chiplet.

So this chiplet-based course will have -- you know, in designing chiplets, you have to deal with I/O drivers a lot. So it will basically have a section or a discussion, a significant -- I mean, I guess, let's say unit or two on ESD structures and how you handle ESD for the chiplet sort of paradigm.

So basically chiplets -- I mean, my ESD work will be part of this new course that I'm offering in the fall of 2026 as well.

So in some sense, ESD is an

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unavoidable thing. It kind of shows up in all kinds of -- in my courses, as well as in my -- in the chips that I fabricated.

Q. Let me direct your attention in your declaration to paragraphs 32 and 33.

A. I think it will be a good idea if I took a break soon because I'm kind of, like, losing my voice, which is why I keep having to sip on my water.

You said 32 and 33? Would it be okay after this question if we take a break?

Q. Yeah, I think this will be a fairly short line of questioning.

A. Okay.

Q. Are you there?

A. I'm at paragraph 32, yes.

Q. And this is where you discuss the level of ordinary skill in the art, correct?

A. Let's see. Yes, paragraph 32 and 33 are where I talk about the level of ordinary skill in the art, which is a section by itself.

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Q. And in paragraph 32, you quote Dr. Foty's definition of a POSITA, correct?

A. Yes, paragraph 32 says, you know, the definition of a POSITA that Dr. Foty presents.

Q. And in paragraph 33, you don't present an alternative definition of a POSITA, do you?

A. Let me read that paragraph and then, you know, respond.

So paragraph 33, you know, it says that I was not asked to provide, you know, a separate opinion about what a level -- what a POSITA would be -- or I wasn't even asked to opine on Dr. Foty's definition of a POSITA. So, you know, clearly, I far surpass the definition of a POSITA.

And also, it says that if I used Dr. Foty's definition of a POSITA, then, you know -- I mean, in other words, I'm saying I used Dr. Foty's definition of a POSITA and under that definition the

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petition does not show that the challenged claims are obvious.

Now, of course, you know, in case, you know -- excuse me -- in a separate, in a possible separate proceeding, I might, you know, provide an alternative, you know, definition of a POSITA if I'm asked to.

Or also, you know, if the board provides an alternative definition of a POSITA or of the ordinary, level of ordinary skill in the art, then I reserve my -- I reserve my rights to amend my opinions.

Q. So in this proceeding, in your declaration, did you render any opinions under a different definition of a POSITA than what is set forth in paragraph 32?

A. No. So the definition of a POSITA that I used for this declaration is what is shown in paragraph 32. As it says in paragraph 33, where it says: Using Dr. Foty's definition of a POSITA, the petition does not show the challenged

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claims obvious.

MR. JENSEN: Let's go off the record.

THE WITNESS: Okay. Thank you.

THE COURT REPORTER: We're off at 1:11.

(Recess taken from 11:11 a.m. to 11:22 a.m. MT)

BY MR. JENSEN:

Q. Welcome back, Dr. Khatri.

A. Thanks.

Q. Let me direct your attention to paragraph 19 of your declaration.

A. Okay. Let me go there.

19, okay, I'm there.

Q. And you can look at paragraph 18 as well.

In this section, you identify the materials that you considered in forming your opinions, is that right?

A. Yes, I do. That's the title of this section is: Summary Of Materials Reviewed And Considered. So yes.

Q. Were there any materials or

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documents that you identified yourself as opposed to being provided to you?

A. Oh, I think there was -- you know, in my reviewing, I found several and so these were just like -- many of these are mine.

Q. Can you identify for me which documents you located yourself?

A. I couldn't tell you that precisely because I don't have a complete recollection, but it's quite possible that they are all mine even. Let me look.

I think -- it's completely -- you know, again, there may be something that was shown to me as a possible candidate and I would have reviewed it and approved or not.

But as far as I can tell, everything in paragraph 19, of course except for the -- except for the deposition transcript, right, in paragraph 19, I list the deposition transcript and then there's other references that I have, which is twenty -- let me see -- 2012,

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which is the Meindl book, and 2013 which is a Dubey paper, 2014 is a transmission line thing -- and -- I think I got -- I think I would have, you know, like found out those.

Again, that's my recollection. It could be a little -- you know, hazy at this point.

Q. Are there any materials that you relied on in forming your opinion that are not identified in these paragraphs?

A. So what I -- the materials I reviewed and considered in forming my opinions in my declaration are listed in paragraphs 18, 19 and 20.

Q. And apart from the materials listed in this paragraph, there aren't any others that you used?

A. No, there wouldn't be anything else I used. I mean, of course, 20 is, you know, my -- it says, you know, my opinions -- I'll just read that where it says: My opinions are additionally guided by my appreciation of how a person of

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ordinary skill in the art would have understood the claims of the '164 Patent at the time of the invention.

So in some sense, that's my background and my experience and I'm sort of, you know, putting myself in the shoes of this person of ordinary skill in the art as of the date of the -- as of the time of the invention, which I was asked to assume is November 1, 2018.

So that's my background and experience. So with me putting myself in the shoes of a POSITA at the time frame I mentioned, at the November 1, 2018 timeframe.

Q. And at the top of page 15, you say: Exhibit 2012 is a true and correct copy of expert -- excerpts from interconnect technology and design for Gigascale Integration, and then you give the cite.

Do you see that?

A. I think -- yes, I see that.

Q. Okay. And what year do you

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list --

A. Oh, wait -- yeah, go ahead.

Q. What year do you list as the publication year for Exhibit 2012?

A. I don't know. I'd have to look. May I --

Q. It's right in paragraph 19.

A. Is it written in paragraph 19?

Q. Yeah, the third line down.

A. Oh, yeah. It says, you know, it says that this book from Davis and Meindl is -- it says it's listed as 2003. That's in the third line of page 15 of my Exhibit 2010.

Q. Is that a book that you have in your collection?

A. No, no, no. This is not a book I have in my collection. But, you know, I followed Meindl's work over the years. He's done some extensive work in this area.

Q. Were you familiar with his work in the 2003 timeframe?

A. I knew of his work around then,

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yeah. I mean, I knew broadly about his work, not very specifically.

So even in my thesis, which was in 1999, there was some work of his that I was citing to and so on -- I mean, not related to this patent or anything because my thesis was unrelated, but I was familiar with his work and, you know, he's been in this field for quite a while.

Q. And then continuing in paragraph 19, you next reference Exhibit 2013 and you say it's a true and correct copy of -- I'm going to butcher the name -- Aishwarya Dubey?

A. Yes.

Q. And then you give the citation for that. You list a publication date of March 2005.

Do you see that?

A. Yes.

Q. Do you know the author Dubey?

A. No, I don't know Dubey. I think he's with TI or something -- I'm not sure, the affiliation was Texas Instruments or

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something, if I recall from the paper.

Q. What is your basis for saying that Exhibit 2013 is a true and correct copy of that article published in 2005?

A. So I think this one I downloaded and I then sent it to counsel.

Now, I don't know if they separately downloaded it. If they did, I would have verified it with my download.

So I downloaded it and, you know, from IEEE or something -- you know, from -- it was an online download. And so that's -- and it did seem to be complete when I read it. So, you know, that's my -- I don't see any reason why where I downloaded it from would withhold some paper, some pages or alter the content of this paper.

Q. And then the next one is Exhibit 2014 and you say it's a true and correct copy of Howard Johnson chip-scale transmission lines, and you give a URL reference.

Do you see that?

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A. Yes.

Q. Are you familiar with the www.sigcon.com website?

A. I'm not specifically familiar with the website. You know, it's sort of a -- it would be odd if I was familiar with all these websites because there's literally thousands of or maybe even millions -- I don't know -- tens of thousands of these.

So I don't particularly, you know -- you know, I don't particularly know of this website, but I do -- I did read the article and it did seem to be -- you know, it did seem to be -- you know, the article that I downloaded did seem to be complete and unaltered.

Q. And when did you download that? Was that in the last year or two?

A. It would have been as a part of this case. So I would have done a -- you know, I would have done a search of, you know, of academic literature as well as technical literature online and then

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vetted what I found and, you know, and then, you know, done a search at that time.

So this would have been sometime before I turned in my report, not much -- not like, you know, a few years ago or something.

Q. So it wouldn't have been you downloaded that article back in 2003?

A. No, I don't think I would have done that.

Q. Okay.

A. It would be -- I mean, I'm not that organized, right -- yeah, so...

I couldn't -- I wouldn't remember something I downloaded in 2003 and bring it up for this declaration.

Q. Going back to the chips that we were talking about before, there was a Motorola chip and then several chips, you know, done in conjunction with your students. Did those chips use bond pads?

A. All of those chips -- let me see -- well, it's a mix. So the Motorola

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chip had -- you know, we had two versions of this. There was a bond pad version which is where the I/Os were peripheral.

And then we, with bond wires, we connected it to a package which was a ceramic package, I don't know, about 100 pins -- I don't know, pretty heavy and good package.

But that was one version of the model chip which was packaged through a ceramic, you know, square package.

And then somewhere down -- I was at Motorola for four years, so where along that four years timeframe, the company decided that they would also do a solder ball version of this same chip and that was -- you know, at the time and still is called a C4 technology, like the letter C and the numeral 4.

So C4 was something that was invented by IBM, which was -- they sort of like had -- if you had the chip area, you would have solubles all over the chip area. So we had to do a new spinning of

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the chip to make it compatible with the solder ball C4 pin out, right, the C4 package. And I was involved in the design changes needed for that.

So essentially there were two versions of the chip. There was the, you know, bond pad package version and then there was a C4 version.

So yes -- I mean, so one of these versions did use bond wires.

Now, the other three chips which we did at Texas A&M, the three chips I mentioned, subthreshold, BPSK transmitter, then I think it might have been BFSK -- anyway, but the subthreshold transmitter, then the multichannel analyzer, the MCA and the alpha detector, all of these had bond pads and bond wires and they were packaged using a regular, you know, plastic package, a square plastic package.

So the three chipset at Texas A&M used bond wires with, you know, with -- what's it called, sorry -- you know, with bond pads and bond wires in sort of a

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plastic package.

The Motorola ones had both packages, had two packages -- well, sorry, at least two packages. There was a third automated bonding or a tab package as well.

So we had three packages. I don't know why we had three packages but we had three packages. Different customers had different sort of needs or preferences or something.

But I wasn't involved in the design work for the tab stuff, for the tab package. But for the -- you know, for the -- for the C4 stuff, I was involved in that as well.

Q. For the Texas A&M chips, were the bond pads on those chips located around the periphery of the chip?

A. Yes. So the Texas A&M chip pad peripheral bond pads, on all four sides. That's all, three of the chips had peripheral bond pads.

Q. When -- and going back to the

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Motorola example that you gave, you said the initial version was, I'll call it the peripheral bond pad version and then you were involved in a second route where one of the changes was to make that the -- a C4, you know, compatible or a C4, you know, package version, is that right?

A. Yeah. So there were two packages, yeah.

Q. Okay. And I've heard the term ball grid array, or BGA, used before. Is that the same or different than what you refer to as the C4 package type?

A. So, you know, the ball grade array is like an array of solder balls, like, it generates, like, a two-dimensional. So if you looked at it, it would just be a bunch of dots in a two-dimensional grid, you know, like usually square.

So basically that would be a BGA. The BGA is basically the package. So, in other words, you could have a C4 -- the chip is C4, chip is implemented as C4. It

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has many balls, if you want to think of it like that.

Now, you have the option of just flipping that chip. That's why we call it "flip chip" sometimes. C4 is effectively called flip chip. But you could take the C4 chip and flip it and directly connect it to a substrate, to a PCB if you wanted. That means that's something that some people might do if -- depending on multiple electrical considerations, electrical and cost considerations.

But you could also say you'll take this flip chip and then you flip it onto another substrate and that substrate will present solder balls, but these are bigger solder balls with a bigger pitch and they're sort of like bulk, you know, like wider. So you could do one or the other. It's kind of like there are many ways to skin the cat.

So BGA is one, solder ball, I mean, C4 is one. So there's a lot of variety here in these packaging

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approaches.

Q. How difficult was it to convert the, you know, peripheral bond pad version of the Motorola chip to the C4 version?

A. It was extremely tricky because, see, you know, even if we had no constraints like -- so in some sense we already had a chip that was manufactured with a peripheral bond pad structure.

So that was a constraint that we had. We didn't -- I couldn't change that because we didn't want to do a completely different spin of the chip because that would be just too expensive and way too time consuming.

So we had this hard constraint that I'm sort of supposed to stay with the pin out that we had on the peripheral version of the chip. That was constraint number one.

Then there's a separate constraint saying, you know, like we've got to make sure that, you know, that the supply pads are sufficient in number and

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they're located at the right locations and also -- you know, so -- in other words, where do you locate them, and how many do you have, and what -- not you're constrained because you have to connect back to the peripheral pad. So it's just an extremely tricky process. It's not at all simple.

And then the same argument has to be applied to the ground -- to the reference pads. So there's reference pads and the supply pads, they all have to be placed correctly so that they will provide the right amount of supply to the right locations and the different locations in the chip consume different amounts of power, so you need to skew this. It's not just a uniform distribution. Extremely tricky process. Not at all something you just say, all right, let's just do it over -- you know, like let's write an automatic program and do this over two days or something. That would just lead to a really bad design.

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So this -- you are to correctly choose where and how many supply pads, where and how many reference pads, where should all the other pads, signal pads go in. Some signal pads are more critical than others. So the critical ones, they need to be close to where they -- you know, to where their main -- you know, where the peripheral pad is and so on.

It was an optimization -- I wouldn't say nightmare, but really an exciting project, but it was very, very tricky.

Now, this was because the peripheral pads were given to me as a constraint. If there was no constraint on the peripheral pads, if I was doing the C4 from scratch, it would be even more tricky. So this is basically a really tricky placement of pads.

You know, I've seen firsthand, you know, it's a significantly sweat-consuming process, right. It's time-consuming, it's sweat-consuming. You

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have to talk to a lot of people on the team saying, you know, like, because different signals have different timing requirements and criticality. Power supply needs to be where it's -- power supply pins and C4 bumps need to be where they need it most because the chips consumes power at non-uniform levels.

So reference pad, same story. So it's a really tricky process. And so this is definitely not something that is, you know, do it overnight, fungible type, you know, move around pins and nothing -- you know, everything is just going to work anyway.

It's an extremely delicate electrical exercise. And for an electrical exercise, it's a fun project. It's a really, really, exciting project because I've got to bring all your electrical engineering knowledge to bear into this one project.

So it was very -- it was hard, but it was fun.

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Q. Did converting the bond pad version of the Motorola chip to the C4 version degrade the performance of the chip?

A. Now, that's something I wouldn't be able to tell because I -- you know, once we did this and then we sold it, I wasn't -- you know, I wasn't in the company for that long. So if I had stayed a little longer, maybe I'd have gotten some customer feedback and so on.

So I don't know the firsthand, you know, like information about whether the performance was degraded or augmented.

But that said, based on my simulations and based on what I -- you know, based on the -- how do you say -- you know, based on my simulation and based on my analysis that I performed over the time that I was, you know, doing this transition, right, I had made sure that the performance was at least as good, you know.

And the reason it was -- the

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reason -- one reason it would be at least as good is as some of my references say -- in fact, the references that say this are the Meindl reference and also -- Meindl reference is 2003 and also the reference -- Meindl reference and also the reference by the chip scale transmission lines -- these references say -- and this is something I've seen firsthand -- they say that, you know, the bond wires are highly inductive, and also if they're long, they're resistive. That's what the Dubey reference also says.

So all these references that I have, which are mentioned in paragraph 19, they corroborate what I've seen firsthand, which is that, you know, the peripheral I/O version of the chip that we had with bond wires going out, that had some bond wires which were really long, you know, and those caused a lot of LDIDD noise, which I mention in my declaration as well -- I don't remember exactly which paragraph -- but I've mentioned that LDIDD

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noise is -- let me find that -- somewhere in the middle -- I can't seem to find it.

Q. I know what you're referring to. You don't need to --

A. Yeah, actually, so really quickly to close this loop, I'll really quickly look up the -- my declaration on the computer so that it's a little bit easier.

Okay, I seem to find the -- so if you look in my declaration, among other spots, but it's paragraph 86 where I describe the electrical sort of, you know, the electrical parasitic of inductance and how it causes a volt -- you know, how it causes noise, because it causes a voltage, which is the inductance L times the IDD, the rate of change of current.

So in this peripheral I/O chip, we had, you know, long bond wires. And bond wires tend to be highly inductive. So they have a large LDIDD noise.

So our chip, the peripheral version was noisier. But when we switched to the solder ball version, the

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inductances of the solder balls are dramatically lower because most of the connections that lead up to the solder ball are on-chip metallization connections. So those are not inductive. They're more resistant as the signal consulting reference says.

And also, you know, the Meindl reference says that as technology is advanced, the -- you know, people have avoided using, you know, bond wire packages. This is something that I cite from reference 2012. Again, that's something I saw firsthand from our chip -- from my Motorola experience.

And then also Dubey says that, you know, the IR drops of these long bond wires can be large. That can cause a slowdown of the chip and also chip failures.

So we had to design around that. But when we switched to the C4, we had to worry less about all those issues.

So going to C4, based on my

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simulations and based on my analysis was going to improve the performance of the chip.

You know, and all that is corroborated by these references, 2012, 2013, 2014 and 2015.

Q. Did the Texas A&M chips use bond wires?

A. Yes, we use bond wires because we're poor. So if I had the choice, I would use C4 or something like this, but that's a much more expensive packaging technology and, you know, we were literally, all my Texas A&M chips are on a shoestring budget. So we just do the -- the chip is everything, you know.

Even if it compromises performance. Because philosophically when I do a chip at Texas A&M, I'm not trying to, you know, beat a chip that someone else in the industry is making. So I'm not competing. I'm not making a product. But I'm trying to prove a technology that no one has tried. That's kind of

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philosophically what I do with my chips at A&M.

So I won't do a chip which is just like, oh, let's make a faster microprocessor or something, or let's make a faster X than what Intel does. I can't compete with them.

But what I will do is, oh, we have this new technology that no one is using, let's validate that you can actually build an op amp -- an amplifier, or a processor using this new technology. That's basically what we try to do.

So even this validating process, I'm not competing with industry chips, you know, because I mean, I'm not a business -- you know, it's a university, it's a research institution that I'm at.

So we're just trying to show a completely new technology -- a really, you know, technology that no one has seen before or is very sort of, you know, unexpected or non-conventional.

So, and so we don't -- I don't

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really try to, you know, let's say put all the fanciest packages because that will just add cost. So my Texas A&M chips are low budget.

Q. Were you able -- strike that.

Using your low budget Texas A&M chips, were you able to demonstrate sort of the proof of concept that you were trying to?

A. Yes, absolutely. The proof of concept, just to give you an idea, it's not about oh, here's the fastest way to do something. But it's just about a technique that no one has even tried -- sorry.

So for subthreshold chip, for example, the first of the chips I mentioned at A&M, subthreshold technology was something that was known. It was a boutique idea that people published a lot about. But the people also knew that you couldn't manufacture something with subthreshold because it's extremely sensitive to variations and temperature

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processing and voltage.

So we had this technique that says we could correct for those variations of temperature, voltage and process by adjusting what's called body bias.

So this was a brand new thing. No one's tried this. So we said let's go fabricate our chip using this subthreshold but with this sort of self-adjusted body buys, and we were able to successfully show that it works.

So the idea was this was a completely kind of crazy concept, but we wanted to validate it, right. So the goal was not to say here's the fastest this or the fastest that, but here's a way to do this extreme low-power circuit which you can make it predictable and put it on the back of a cockroach. That was kind of the idea.

So can we make it manufacturable, can we make it something that industry can pick up after us and run with it. That's the philosophy of the designs I do at A&M.

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It's not to compete -- compete with the industrial chip offerings of these -- of existing chips.

Q. How long --

A. Philosophically, that's what it ought to be at academia because we should come up, I think, with new ways of doing things that people can then later pick up and run with.

Q. How long has bond wire technology been around?

MR. WATSON: Objection. Form.

A. So, you know, again, you know, bond wire technology has been around -- so I'll answer the question in the context of our, you know, of the '164 Patent, right.

So yeah, although bond wire technology has been around, it has not -- you know, until the '164 Patent, it was considered disfavored to do bond wires between, you know, between I/O pads on the same chip, on the same piece of silicon.

Because, as you saw, you know, as Saint points out -- and Saint, and the

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page numbers of Saint where this is said, is something like, something in the 200s, right, page 200 of Saint -- and I'm referring to the blue page numbers, not the Bates numbers page numbers -- but Saint says that, look, if you have bond wires that are long, they can basically, you know, they can run over existing circuitry on your chip and they can sag. And once they sag or droop, then they can cause a short-circuit.

So this was well-known. This was the conventional wisdom in the art that even though bond wires were, you know, a common technology to connect peripheral pads off a chip to package pads off chip, right, that was well-known.

But to connect peripheral pads on one chip to another peripheral pad on the same chip, that was considered to be dangerous. That's as Saint says in, you know, as Saint says, you know, somewhere in the Saint reference.

So this is -- although bond wires

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for packaging, for connecting a chip to a package was well known, bond wires to connect pads on a packet -- sorry, on a chip to other pads on the same chip was considered dangerous.

And the conventional wisdom was don't go there because, you know, bond wires are inductive, they will introduce noise, you know, they will be -- they will also, you know, cause potentially droop and sag and cause short-circuit, as Saint teaches. And they're inductive and they're noisy as Dubey and, you know, and other references, and Meindl reference states.

So it was well-known that this is something you avoid. And whenever you can do on-chip metallization, you just go with that.

Q. And so are you distinguishing between using bond wires to connect a bond pad to a package versus using a bond wire to connect two bond pads on one chip?

A. Correct. So I'm saying bond

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wires to connect, you know, a bond pad to a package, that was a technology that was known for a while.

But bond wires to connect bond pads to bond pads on the same IC, on the same chip or the same die, was considered dangerous and considered, you know, a tricky thing to do because of what I just said, because of the Saint reference which -- among other references, Saint reference which says that this is basically something that would potentially cause a short-circuit.

And a short-circuit -- I mean, that comment of Saint, which is using bond wires, which, you know, they run over, you know, run over the chip, they can cause a short, that's an important comment because, you know, as an electrical engineer if you're designing a trip and there's a short-circuit, it's the end of the world. It's basically a chip is fried. You can literally see smoke and it's never going to work again.

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So a short-circuit, it might seem like, you know, on the face of it, it's sort of another detrimental effect, but it's fatal and it's irreversible.

So a short-circuit which Saint teaches as a possible consequence of using bond wires to, you know, which run over the chip for too long of a distance, those could be fatal, they could basically cause a short which is the end of the chip.

So that was conventional wisdom that you don't use bond wires on the same chip.

Q. Suppose that you had two bond wires of the same length, one that connected a bond pad to a package pin and another bond wire that connected two bond pads on a chip.

Is there any distinction or -- strike that.

Keeping the same assumptions, you have two bond wires the same length, one that connects a bond pad to a package pin and another that connects two bond pads

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together.

Why would the considerations about noise, inductance, et cetera, be any different when connecting two bond pads versus connecting a bond pad and a package pin?

MR. WATSON: Objection. Form.

A. So I'll say it in two way, right.

Let me look at my declaration to support what I'm going to say.

The first -- let's see. So I want to -- I want the -- let me look for the citation number.

And I'm going to search in my declaration for the citation number. That's sort of what I'm doing.

So the first part of my answer comes from 2015. So let me search 2015.

No, it's not 2015, sorry, it's 2014. Which one is -- signal consulting is 2014, that's what I was looking for.

So may I open -- so I'm going to point you -- this is sort of a first response to your question. It comes from

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paragraph 88 of my declaration.

And in paragraph 88, the last three lines on page 60, I cite to -- sorry, let's say the last five lines -- it says: Both the on-chip IC metallization and diode connections taught in Yoshinaga are less inductive than bond wires.

In other words, it's saying the alternatives that you have to using bond wires for connecting bond pads on a chip to other bond pads on the chip which would be, for example, integrated circuit metallization, those are less inductive than bond wires.

Now, remember, bond wires have a large inductance. Therefore, their LDIDD, which is the noise, the voltage that they produce, which is noise, that would be -- you know, that would be large, if the L is large.

So bond wires have a large L. Therefore, they have a large LDIDD. Therefore, they have a large noise. And that's what this statement is

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supporting -- is based on.

Also, the same statement cites to the signal consulting, the Exhibit 2014, and it quotes there saying series of resistance, not inductance, dominates on-chip connections.

On-chip connections means integrated circuit metallization. Integrated circuit metallization has resistance that dominates, but not inductance.

In other words, it's supporting what I say. Like, if you have a bond wire to connect the bond pad on a chip to another bond pad on a chip, that would have a large inductance and large noise.

But if you instead use the alternative, which is just to use integrated circuit metallization or on-chip interconnects, then you have less inductance and therefore less noise, and that's why that is a favored option.

So not using bond pads for connections that are from bond -- sorry.

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Not using bond wires for connections from one bond pad on the chip to another bond pad on a chip reduces the -- reduces the -- I mean, reduces the LDIDD noise or the inductive noise as supported by this -- by this discussion.

And I'll also point to another paragraph which is the end of -- which is paragraph 94 of my declaration, which says if you decided to use bond wires to connect the bond pad to another bond pad on the same chip, well, there's another downside to that. That other downside says that the use of bond wires, you know, has more reliability issues.

So it says increased reliability issues, and that might be easy to misread, it might suggest that it improves reliability. But what I mean is it increases reliability issues or increases reliability problems or causes more reliability problems. That's kind of what I mean by those words.

But using bond wires causes more

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reliability problems because, you know, these wires can cause a short-circuit. That's one reason, you know, as taught by Saint on page 195. So you can get a short-circuit.

But also paragraph 95 -- or was it before that -- says that -- oh, there's one more paragraph somewhere. There's a reliability -- oh, yeah, there we go, paragraph 93, which is also on page 63, which says that bonding wires are exposed to the elements and therefore they're less protected than the connections already taught in Yoshinaga.

So now we have three reasons so far why it's a bad idea to use bond wires to connect a bond pad on a chip to another bond pad on a chip.

The first, which is what I pointed out in the beginning of this discussion, was that they're inductive and so there's the LDIDD noise and the alternative which is on-chip metallization has lower inductance and less noise.

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Reason number one.

Reason number two comes from paragraph 94, you know, which says -- which cites to say and then says, you know, having a bond wire that goes from bond pad on a chip to another bond pad on a chip could cause a short-circuit, which is fatal for the chip.

This, you know, if I was a designer and someone said there's a possibility of a short -- if I took a certain route -- if I did a certain decision, it would basically be -- it would basically shut the shop down. People will say I am absolutely not taking that chance. Because a short-circuit is catastrophic and it's a really, really bad thing. So that was reason number two.

The third reason is what was on paragraph 93, which says bond wires are exposed to the elements and therefore they're less protected. And therefore, again, a chip using bond wires to connect bond pads to other bond pads would be

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considered less reliable, you know, because it was exposed to the element.

And if I had an alternative, I would choose it. And that alternative is readily available, which is the -- which is the on-chip metallization.

So there's multiple reasons why someone at the time of the patent would see that connecting bond pads to bond pads on the same die using bond wires was a bad -- was a bad engineering decision.

Q. Let me clarify my question because I think that was non-responsive and I'm not asking anything about metallization.

My question had a premise built into it which was you have two bond wires of equal lengths, one connecting to a package, one connecting to another bond pad.

Why would the noise, the inductance and the other problems that you mentioned for bond wires be anymore problematic when connecting two bond pads

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together than when connecting a bond pad to a package pin?

MR. WATSON: Objection. Form.

A. Yeah, so that question is too -- it's -- you know, a person of ordinary skill in the art when they were considering the choice of how to connect two bond pads would not only consider what you're saying.

See, in some sense, your question is extremely narrowly focused. But a person of ordinary skill in the art, when deciding whether to use a bond wire or something else to connect the bond pad to another bond pad, would not just consider one aspect what you're saying, they would consider all the three -- all the aspects that I, you know, that are out there before they make this important engineering decision.

And the aspects that I brought up in my last discussion are absolutely important aspects that they would consider.

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They would not make a decision purely and solely based on that one fact that you're hanging on to, which I think is extremely narrow. It would -- in some sense, blind to all the other downsides of bond wires.

A person of ordinary skill in the art would simply not just look at one factor and say that's this one factor I'm going to use to justify my use of bond wires. They're going to look at all the engineering factors. And when they look at all the engineering factors, they will look at, you know, the inductance, you know, and the alternative, which is on-chip metallization which gives you low inductance and necessary noise.

They would look at reliability issues because of, you know, because of the likelihood of a short-circuit.

And that would be a big deal for them. Because if anything is a possibility, if anything has a possibility of causing a short-circuit, they're

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running miles from that, from that engineering decision.

And then they'll also look at the, you know, the integrated -- I mean, the fact that bond wires are exposed to elements and therefore are problematic.

So they'd look at all of these things.

Now, it does say here that bond wires are exposed to the elements. On-chip metallization, I didn't say this, but I'll say it now, on-chip metallization is not exposed to the elements because --

Q. Let me just pause you there because this is completely --

MR. WATSON: You can let him finish his answer. I assume he's getting to what you were looking for. So go ahead. Sorry.

A. So on-chip metallization is not subject to environmental, you know, like the paragraph 93 where it says bond wires are exposed to the elements.

On-chip metallization is not

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exposed to the elements because after we manufacture a chip, we put on top of it kind of a blob of epoxy. Basically that keeps all the metallization and everything, you know, protected from the environment.

And that blob of epoxy, it only has openings. These are called passivation openings or holes in the epoxy right at the bond pads. That's where the bond wires would go and attach.

So that part is exposed to the elements. But the rest of the chip with the on-chip metallization is not exposed to the elements.

That's why on-chip metallization is favored because -- and it's not exposed to the elements. That's just sort of clarifying paragraph 93 a little bit more.

Q. Let me give you one more chance to try and answer the question. And without quibbling over whether it's narrow, I want to see -- I want to make sure you had a full opportunity to answer

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the actual question that I've asked.

A. Okay.

Q. Which has nothing to do with metallization. We can talk about that later, and we will.

The question I have asked is: Why would the noise inductance, you know, and droop problems that you identify for bond wires be any more problematic when you're connecting two bond pads than when you're connecting a bond pad to a pin?

MR. WATSON: Objection. Form.

A. Okay. So this is a false question, I think, because here's the reason why.

Let's say I have a -- you know, I'm connecting -- I'm using a bond wire to connect a package pin to a chip pin, right, scenario A, okay.

And scenario B is, I'm using a bond wire to connect a bond pad to another bond pad. That's the two scenarios that you're asking me to discuss.

In scenario A, if I'm using a

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peripheral I/O package and I -- you know, I don't have a choice, that's the only choice I have which is to use bond wires because I'm going to use a bond wire -- I mean, I'm going to use a package that uses bond wires, right.

On the other hand, for option B, it's not like there's no choice. There is a choice that is staring at the face of a person of ordinary skill in the art, which is to use on-chip metallization. There is a question of alternative.

See, option A has no other alternatives. Option B has alternatives. A person of ordinary skill in the art would look at all alternatives and say I'm going to make the decision based on all the alternatives I have.

In scenario A, no alternative. So I'm going to go use bond wires.

Scenario B, I have a better alternative which doesn't use bond wires, which is on-chip metallization, which has all the three advantages I just mentioned.

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A person of ordinary skill in the art would say that's a no-brainer, I'm going with on-chip metallization.

Because of the lack of danger of a short-circuit, because of a lack of the reduction in noise and because of the reduction in the exposure to elements.

These are compelling reasons why they would choose the alternative.

MR. JENSEN: I'll just note for the record that I gave the witness three opportunities to ask a question, even with bond pads and not metallization, and we reserve our right to compel an answer to that question.

We'll move on.

MR. WATSON: And we obviously disagree, on record.

MR. JENSEN: I suspected you would.

Q. Dr. Khatri, you mentioned that there were sort of two options --

A. May I ask a -- may I make a quick

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comment? It's around 12:10. I don't know, maybe we've gone for an hour.

So it will be -- if you're at a breaking point in your questions or a module or something, then maybe we could take a break now for lunch or we could do that maybe in the next few minutes, if that's okay.

Q. I think in the next few minutes should be fine.

A. Fair enough.

Q. You mentioned that -- you mentioned two options for connecting bond pads together, right, one of them was I think what you called metallization and the other one we have discussed is using a bond wire.

What are the other options for connecting two bond pads together?

MR. WATSON: Objection. Form.

A. So this is something that -- you know, when we have an integrated circuit, there are many ways to connect to circuit nodes together.

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So in general, I think your question is -- can I ask in your question is referring to, if there's an electrical node in a chip and another electrical node in a chip, what are the ways to connect them? Is that a fair way of characterizing your question?

Q. I would narrow it a little bit because we're talking about bond pads, right.

A. Okay.

Q. Right. So with specific reference to bond pads, you mentioned that, you know, one way to connect those two electrically would be to use a metallization, which is to say a metal trace. Is that fair?

A. You know, I'd be more careful with that answer, but to use a metal trace is sort of vague because everything's a metal trace. So I might -- I won't -- I disagree with that characterization of your question.

Q. Well, I'll use the term you use,

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"metallization." I heard the term "metal trace" and they're synonymous in my mind but I'll stick with the term "metallization" if you prefer then.

Is it fair to say that one way to connect two bond pads together electrically is to use metallization?

A. And I'll use the word -- I just want to qualify this a little bit. When I say on-chip metallization, I mean using one of the metal layers of the chip. A typical integrated circuit has multiple metal layers to connect different, you know, components together.

So using one of those metal layers is what I mean by on-chip metallization.

And typically, when we use on-chip metallization for bond pads, we're talking about the highest metal layer, which is the least resistive metal layer.

Q. Understood.

And apart from using those, the metal layers that you mentioned to connect

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bond pads, what are all of the other ways that an engineer could connect two bond pads together?

A. Yeah. So my answer to that would be, you know, I'm -- for this matter, right, I'm going to -- you know, the options that are sort of for this IPR, for the 164 IPR, the options on the table that we're considering, like using bond wires to connect to the two bond pads because that's what the petition is trying to teach, you know, and also -- so that's one option.

And then there are, you know, teachings in some of the references cited by the petitioner, which basically use on-chip metallization.

So those are sort of the two options for the matter at hand.

There are other possibilities as well, but that's not something I've given great thought to. So I will say them with some caution -- I'm sure I'm going to be missing some or others or maybe --

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depending -- so in some sense I'm qualifying my answers saying this is going outside what I have studied or what I have opined on in my declaration.

So with that caveat of your question, and therefore my answer, is going outside the realm of my declaration and the study that I've conducted for preparing my declaration, I'll answer it follows:

The choice of how you connect your two bond pads, it depends on many things and it's not a clear simple answer.

One of the two -- you know, one option, which is on-chip metallization is common and it's the first thing a certain POSA would think of and for the three reasons I provided a few minutes ago.

The other option would be using, using on-chip -- using bond wires to connect the two bond pads. Again, that's not a great idea. A person would run -- a person of ordinary skill in the art would shy away from that for the three reasons I

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mentioned.

For the other methods, what one would use depends highly on the type of design you have, the type of technology you're using, the type of performance, you know, requirements you have, the type of power -- you know, the power and energy requirements you have.

So a lot of design considerations of the final product would impact what are the choices you have.

So, for example, if your speed wasn't -- I mean, and this is just an example. It's not something that I've thought about a great deal because it's outside the scope of my declaration, but just to be complete, I'll give you one example.

If the speed requirements of the chip aren't very, very high, then maybe you could connect them with, you know, with a diffusion wire or a silicided poly wire. There may be many other ways to connect these two bond pads that are not

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directly one of the two that we are talking about.

Again, you know, if you gave me the constraints, if you gave me like, you know, the requirements of the chip, which is basically the power requirements, technology of the chip, the -- you know, the energy requirements, the speed requirements, I could probably give you a better answer, but this is just a sort of a first order answer that comes to my mind, you know, as you ask me this question.

For example, also now, if you have a different technology, there may be other ways to connect them. So there's no clear answer that I can give you.

But what I can give you is -- what I can say is for the 164 IPR, for the references that have been cited and are being discussed in the 164 IPR and for the cites that I present in my declaration, I only see the two choices on the consideration as the, you know, as the

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bond wire to connect two bond pads on the same chip or the on-chip metallization to connect, you know, to connect circuit nodes on the same chip.

MR. JENSEN: Let's go off the record.

THE WITNESS: Okay. Thank you.

(Recess taken from 12:17 p.m. to 1:00 p.m. MT)

BY MR. JENSEN:

Q. Welcome back, Dr. Khatri.

A. Thank you.

Q. So before the break, we were discussing kind of bond wires and bond pads and I want to continue with that topic a little bit.

Are bond wires still used in chips today?

A. I think we went through this, you know, this kind of questioning. I think you had asked about how long they've been around and that's when I said they use for, you know, connecting, you know, chips to packages. So that's still in use

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today.

Q. How prevalent is it?

A. I don't know. I don't really have market data as such, but, you know, I mean, it's not -- it's still used, yeah.

Q. Going back to your Texas A&M chips, when was the most -- and I think you said there's still one in the works, we can put that to the side -- when was the most recent chip done?

A. I'm not exactly sure, but the most recent chip would be the -- would be the -- would be the detector chip, the alpha particle detector chip, and I'm guessing that was done in the -- it would be in something like 10 years ago or something like this, in that neighborhood.

Q. Okay. Was it hard at that time to find a packaging company that would wire bond the chip to the package?

A. Sorry, the question again?

Q. Yeah. So when you packaged the alpha detector chip that at Texas A&M, was it difficult to find a company to perform

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the wire bonding?

A. I think the vendor through which we fabricated had a wire bonding sort of services part of it. There are not that many vendors, but the vendor was, I think, MOSIS, and MOSIS had a -- you had the option of saying, you know, wire bond this for me before -- you know, along with the chip.

Q. And MOSIS, that's the acronym M-O-S-I-S?

A. Yes, M-O-S-I-S, yes. I think at the time -- I don't know if they're still around, but yeah, that's the MOS implementation. So this is what it originally was.

Q. How does an engineer decide on the number of bond pads that are needed for a design?

A. They're multiple sort of design considerations that go into this -- excuse me -- that, you know, and there's some functional requirements that go into it.

Like the functional requirements

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might be that, you know, like you have a bus that's 8-bit wide, or 8-bit data bus, or then -- and a 8-bit address bus. So you know you need 16 bits, 16 bits, you know, off the back.

So there are certain functional requirements that you have, which, you know, which will tell you how many pins you need at the bare minimum.

But, of course, then you need part supply pins and reference pins and sometimes you have multiple part supplies, multiple references.

And so now it becomes a delicate and intricate and, you know -- it becomes an intricate task of even figuring out how many of these you need because there will be different numbers of power supply pads or reference pads of different types based on the power consumption of those circuits and where the locations of the circuits.

So now it becomes this kind of joint optimization problem, where are you going to place the circuit, where are you

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going to place the pads, how many pads are you going to need.

That's kind of like this, you know, pretty involved characterization and there are many simulations that go into this. There are many -- you know, there's a lot of analysis and simulation that goes into that.

Also deciding, you know, where to place these becomes a tricky issue. And many of the references that I've cited in my declarations point to that. For example, the -- you know, the Dubey reference, which is -- I forget the reference number -- that talks about methods to decide where to place power pins. And then also the last reference, which is the Haralabidis reference, it talks about, you know, algorithms and sort of approaches to do that.

So this is essentially a, you know, multiple sort of factors go into this decision-making and it's one of the tricky design -- tricky design steps in

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the deciding of the plan of the chip.

Q. When is the decision made on the number of bond pads that are needed?

A. I mean, it's decided based on a number of things, based on, you know, what package you're going to use, for example. It depends on the package. It depends on the -- you know, like the functional pins that I described. And it also depends on the different sections of the chip and how much power they need and what localized power consumption sort of profiles you have.

So all these factors are, you know, going to the decision of the number of power and supply pins.

You know, are the supply pins sufficient in number from a steady state current point of view. Is the rate of change of current sufficiently small so that the inductive noise doesn't get too loud too much.

So all these factors, I mean, it's just this multi-dimension signal

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multi-variate sort of decision-making that needs to get done.

Q. Yeah, so let me clarify my question. It wasn't so much what are the considerations. It was when in the process is that decision made. Is it made at the beginning, is it toward the end of the process, is it an iterative thing where it changes over time throughout the process? When along the way does an engineer decide on the number of pads that are needed?

A. So I don't know what you mean by "the process." Like, can you define this process? What does, in your mind, the word "process" entail?

Q. I'd say everything that's involved up to the point of manufacturing the chip.

A. So from the time of -- and what's the starting point?

Q. When the engineer either receives an assignment or decides that they're going to make a chip.

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A. Okay. First of all, it's not an engineer. It's usually --

Q. A team.

A. -- a team, yeah.

So from the time, you know, the project begins with the team to the time when it's fabricated -- and what was the question again? I kind of lost your question.

Q. I said when along the way is the decision made regarding how many bond pads are needed?

A. How many bond pads are needed? I don't know. I can't -- I don't see -- I can't see the question being -- I guess the question is not sufficiently well formed for me to give you an answer.

Q. Let me try to break it down and ask the question this way.

Does the engineering team decide how many bond pads are needed before or after they have done the layout for the design?

A. Does the engineering team decide

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how many bond pads they need before or after the layout is done? Is that what you said?

Q. Yes.

A. It's an iterative process and many times it's kind of like going back and forth because these things are happening. Lots of -- I mean, you're going to try to parallelize a lot of these activities as much as you can.

So, you know, there may be layouts of certain portions of the chip that are proceeding widely or deciding the number of supply pads and reference pads and I/O pads.

So a lot of it is iterative. A lot of it is changes, they're going to induce changes, efforts, and such. And like I said, it's an elaborate process, so...

Q. Would your answer be the same for the placement of bond pads?

MR. WATSON: Objection to form.

A. Would my answer be the same as

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what? I don't quite get -- again, I think the question is too brief for me to give you a brief answer. Can we expand it out maybe?

Q. Yeah. You said in response to my question about, you know, the number of bond pads, well, that's an iterative process and it happens in an iterative fashion. And so the next question is would your answer to the question about the placement of the bond pads, where they're located, be the same, that that's an iterative process, it's not done at the outset, it's not done at the end, it's done iteratively along the way?

A. I mean, it's done iteratively and it's done along with the decision of number of bond -- the number of reference pads and power supply pads and so on. This is in some sense all in one -- you know, it's one process. You know, I mean, it's in one sort of combined umbrella, if you will.

You know, that's why if you look

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at some of the papers I've cited, they're talking about both deciding the location as well as the positioning of the placement of the supply pins and so on. That was, I think, if I'm not mistaken, reference 2015.

Q. Okay. For each of the three chips you did at Texas A&M, approximately how many pins did each of those have?

A. I don't recall, but I think -- they might have -- I don't really recall this number, but -- yeah, I couldn't -- I couldn't tell you off the bat.

Q. Was it in, let's say, more the range of dozens or hundreds?

A. I don't know if it would be in the low hundreds -- between low hundreds or dozens or something like this. But again, I don't recall this.

Q. When designing the Texas A&M chip did you ever have to make any changes to the bond pad assignments?

A. I don't know that -- I don't understand that question.

S. KHATRI

Q. Did you have to change what signal was assigned to a particular bond pad?

MR. WATSON: Objection. Form.

A. I don't recall. But if that ever happened, it would be an event. It would take, you know, it would take a lot of effort to decide how to move something, you know, if you want to rearrange the, you know, assignment of pins on the chip or pin out of the chip. That would be something that would have, you know, entailed a lot of simulations and a lot of discussions, a lot of, you know, analysis and so on.

So if that happened, it would be something that tremendous, you know, effort and thought would have gone into.

So as a design team, we do everything to avoid that because we just don't want to sort of make these changes later on because it has huge impacts, not just to the pin out, but to the entire circuit. And it may require redesign. It

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could be -- I mean, that would be like a really problematic sort of event, you know.

Q. When a designer first begins or a team of designers first begins the design process and they are deciding where to, you know, locate the bond pads, what restrictions, if any, do they have on where they can place the bond pads?

MR. WATSON: Objection to form.

A. I mean, I cite so many of these restrictions, and many of these restrictions are cited, you know, even in the declaration that I have.

You know, there is -- for example, you know, I can go to some of my citations, they are kind of -- they are sort of saying these things.

There is a citation from Saint, you know, which talks about placement of pads and how tricky that can be.

Let me see...

I'm trying to see what's the best way to find it.

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If you know where it is, you're welcome -- I mean, I'll accept your help in finding it.

But Saint does talk about the intricacy and the importance of placing supply pads, particularly because power supply needs in different parts of the -- supply reference pads, because power supply needs in different parts of the chip are different. So that's one.

And Dubey talks about this as well, which I've cited to in my declaration.

And also the last reference, which is the -- which is the Haralabidis reference, that also talks about it.

So there's a -- you know, these references talk about the considerations that go in, which is localized, you know, power requirements of the chip, you know, the form factor requirements. You know, there's just many different requirements, like number of reference pads and number of power pads.

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You know, so lots of engineering decisions and electrical decisions go into choosing the locations of these pads.

Q. Are bond pads placed based on where the circuitry in the chip is located, or does an engineer place the circuitry in the chip based on where a bond pad is located?

MR. WATSON: Objection. Form.

A. That's just not a simple question to answer because both things affect each other.

That's kind of what I'm trying to say, is that all these things are like, you know, like intricately affect each other.

So depending on where you're -- you know, where your circuitry is placed, that would induce where you keep your bond pads.

But if your bond pads can't go into there, circuitry has to move elsewhere.

So all of this is kind of being

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optimized in one -- I mean, all at once. It's just a giant co-optimization problem that makes -- that's what makes chip design difficult and intricate and also rewarding.

Q. Do you know what technology node was used to make any of the Texas A&M chips? And by that I mean, there's 130 nanometer, 90 nanometer and various other technology nodes?

A. Yeah. So I don't have a clear recollection, but it would have been -- some of these would have been in the quantum micron node, you know -- but again, I don't remember the fine details of all the chips.

Q. What, if any, improvements in bond wire technology are you aware of in the last 20 years?

MR. WATSON: Objection. Form.

A. So, you know, bond wire technology basically is -- it has inherent -- I'm sorry, it has -- I'll scratch that word -- it has basically

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in-built limitations in some sense because it consists of a wire of a certain diameter.

And then once you have a wire of a certain diameter, there's an unavoidable inductance that's induced by that decision and also an unavoidable resistance.

So that technology hasn't moved much in the years. So in terms of, you know, in terms of its inductance and resistance characteristics, that hasn't moved much.

And that's why, for example, one of my reference is the Meindl references, what I'm calling the Davis reference in my declaration. That says that as technology advances, bond wire technology is being disfavored.

Q. Do you believe that bond wire technology has been disfavored across all categories of integrated circuits?

MR. WATSON: Objection. Form.

A. Again, I mean, this question speaks more to marketing decisions and

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marketing sort of, you know, requirements of the chips and I couldn't speak to that directly.

Q. What materials are bond wires made from?

A. I'm not 100% sure, but I think they're made out of gold. But I could be wrong on that.

Q. What materials are bond pads made from?

A. Bond pads are made from the metallization -- the metal that's used for metallization of the I/O pads and that depends -- excuse me -- depending on the technology you're using, that might change.

So earlier technologies had aluminum. More recent technologies have copper, which is clad and tungsten. So there's different metallurgicals of -- you know, there are different metallurgicals of building materials that they use for the bond pads.

Q. Why are bond pads made using the

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top metallization layer?

A. Well, because the top metallization layer is usually the thickest. That means it's least resistant, you know. And the lower metal layers are now deeper into the chip and they're thinner. As you go lower, they're thinner and deeper into the chip.

So if you use a low metal layer to do the bond pads, you know, you'll have a hard time for the bond wire to sort of -- to sort of, you know, probe it -- I mean, sort of to enter this cavity that, you know, that the -- the passivation cavity. So that will make it harder to attach the bond wire to the metal layer.

And also, once you attach it, now the metal layer is more resistive, so you'll have like your -- if it's a reference or supply pad, it will be able to carry less. So you're basically, you know, limiting yourself by going to lower metal layers.

Q. Let's shift gears a little bit

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and look at the '164 Patent.

A. Okay.

Q. And I'll share my screen, but you're welcome to look at your hard copy as well or your local electronic copy.

A. Okay.

Q. Let me know when you're able to see the screen there.

A. I see it now. I see two pages.

Q. Have you read the '164 Patent, Dr. Khatri?

A. Yes, as part of -- you know, as part of writing my declaration, I have reviewed the '164 Patent.

Q. Is there anything you didn't understand in the '164 Patent?

A. Not that I recall, no.

Q. What's shown in Figure 1 of the '164 Patent?

MR. WATSON: Objection. Form.

A. So, you know, let me read from my copy of it, which Figure 1 is described. Let's see.

So, you know, in column 2, around

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lines 30, it says Figure 1 is a schematic diagram of an integrated circuit ESD bus structure according to the prior art.

So that's what Figure 1 would describe.

And then there's a further description of Figure 1, you know, in the actual spec under the description of prior art at this time.

Q. Figure 1 includes some text, a label that says circuit with irregular shape.

Do you see that?

A. Yes, I do see that.

Q. Does the '164 Patent only apply to circuits with irregular shapes?

A. I don't think that that's something you could say because this is just sort of a depiction of, you know, of the prior art. It doesn't say anything about -- you know, it doesn't limit itself to circuits with irregular shape.

Q. And what are the objects labeled 12 in Figure 1?

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A. So I'll read from, you know, column 1, something like lines 24 onwards, right, where it says the -- you know, for an integrated circuit ESD structure 1 -- that's the entirety of Figure 1 -- I/O pads 12 are placed around a circuit area 10 inside a plurality of chip edge 13.

So 12 are I/O pads. So 12 represent the I/O -- you know, the label 12 represents the I/O pads of the design.

And the -- you know, and sort of the -- yeah, and it's talking about the ESD structure 1 of this particular -- sorry, ESD structure, the ESD structure on this figure is labeled as label 1.

Q. Are the pads 12 in Figure 1 bond pads?

A. Let's see. I'll have to read more carefully to give you an answer.

It does say I/O pads 12.

So in the patent, they're referred to as pads. And, you know, the wires that are used to connect to as bonding wires.

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So there's no -- the patent itself does not use the word bond pads. But a person of ordinary skill in the art looking at these pads, you know, and also knowing that bonding wires were attaching to them, they would think of them as bond pads. But it's sufficient to just call them pads, as the patent does.

And ultimately, the patent is the -- the patent is the lexicographer here, the inventor.

Q. Does Figure 1 show any power pads?

A. A person of ordinary skill in the art would know that there was -- you know, that some of these pads were power pads because that's an essential requirement, you know, in any chip.

Q. Does Figure 1 show any ground pads?

A. You know, Figure 1 talks about the -- let me see, sort of -- it was in column 1, let me see.

I'll look at my declaration

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because I have that citation in my declaration someplace. Give me one second.

Okay. If you look at column 1 -- let's see, hold on.

Column 1, lines 32 to line 35 talks about the electrostatic discharge or ESD bus 11. And it defines that. It says a layout trace connected to a ground or system voltage.

So the ESD bus 11, you know, is a layout trace, but it's connected to a ground voltage or a system voltage.

And the way it would get connected to a ground or system voltage is by way of some pads.

Q. Can you tell by looking at Figure 1 which of the pads 12 is a ground pad?

A. You know, Figure 1 doesn't show that. But, you know, it would be clear to a person of ordinary skill in the art that some of them, you know, one or more of them would be ground pads. Because Figure 1 is just generally, it's just generally

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showing, you know, pads. And it's only labeling to one, but of course there are many pads there.

Q. Are the pads 12 shown in Figure 1 identical to one another?

A. You know, one couldn't be sure visually just by looking at this, because in general a chip has many features and what -- a number of features shown in this diagram is maybe 10 or 15 features, right, or 15 shapes. In general, a chip has millions or even billions of shapes.

So there's a certain amount of detail that's missing in this figure. But a person of ordinary skill in the art, again -- and again, based on the chips I've done, you know, the pads are all similar and if not completely identical, but pads of the same type are identical, other pads are very similar to each other.

So a person of ordinary skill in the art would know that pads are -- you know, that they're at least similar.

Q. Do you see the labels F1 and F2

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in Figure 1?

A. Yes, I do see those.

Q. What are those?

A. So let me, you know, let me again go to the spec where it describes F1 and F2. This is, again, in column 1, around line -- starting around line 30 where it says: In general, it is common to place filler cells, F1 and F2, at empty spaces between I/O pads 12 and connect the filler cells F1 and F2 to an electrostatic discharge bus or an ESD bus 11.

And then later on it says, you know, this makes each portion of the circuit area 10 and the filler cells F1 and F2 are connected to the continuous ESD bus to provide ESD protection to the integrated circuit.

So the filler cells F1 and F2, according to the specification, are -- I mean, sorry, the labels F1 and F2, according to the specification, are filler cells.

Q. What is a filler cell?

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MR. WATSON: Objection to form.

A. I mean, a filler cell is just like the name suggests. It's a cell that's -- just a special name given to the cell, F1 and F2, just called a filler cell.

And its purpose is, you know, it's basically filler cells F1 and F2, they connect to the continuous ESD bus 11 that you see in Figure 1 and this provides -- this is, again, provides ESD protection to the whole chip.

Q. So Figure 1 is labeled prior art, correct?

A. Yes, I see that. It says Figure 1 prior art.

Q. And what's shown in Figure 2?

A. Figure 2, let's -- you know, I'm going to go to the description for Figure 2.

So if I look at the brief description of drawings, this is column 2, lines like 32 onwards. So Figure 2 is a schematic diagram of an integrated circuit

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ESD structure according to one embodiment of the present invention.

Q. So unlike Figure 1, which is prior art, Figure 2 is an embodiment of the invention in the '164 Patent?

A. That's what -- that's what this language says.

Q. What does the numeral 25 represent in Figure 2?

A. Let me see, look at this, look at numeral 25. Once again, I'm going to look at the specification where it says -- let's see, this is column 2, lines 46-ish where it says Figure 2 is a schematic diagram of an ESD structure 2 according to an embodiment of the invention. And it describes different structures.

And a little bit later it says that the integrated circuit bus structure includes -- and I'm skipping a few elements -- and it says includes up to a plurality of bonding wires 25.

So 25 represents a plurality of bonding wires.

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Q. How many bond wires are shown in Figure 2?

A. In Figure 2, I can see three such bonding wires. These are these dark curve lines, you know, that all look similar. And one of them is labeled 25.

Q. What is numeral 24 in Figure 2?

A. Once again, if I look at the description of Figure 2, lines 47 to like 53, it says -- let's see -- let me just go through the whole thing.

So it says the integrated circuit ESD bus structure 2 includes a circuit area 20 -- which we can see -- a plurality of ESD buses, E1, E2 and E3 -- so there's like in this case a plurality of ESD buses -- a plurality of pad groups, G1, G2 and G3 -- you know, which are also labeled -- and then it says a common ESD bus 24. So the label -- the element labeled 24 is a common ESD bus.

Q. What is the difference between an ESD bus and a common ESD bus?

MR. WATSON: Objection. Form.

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A. I mean, it's basically just a feature that's shown in the figure. And so that's basically how it -- you know, different features in this figure are described. That is, there are three -- you know, there are three integrated circuit ESD -- sorry.

There are three ESD buses among the plurality of ESD buses that are labeled E1, E2 and E3. And then there's also a common ESD bus which is labeled 24. So that's just the description of the diagram that we see here.

Q. Does the common ESD bus 24 electrically connect the ESD buses E1, E2 and E3?

MR. WATSON: Objection. Form.

A. You know, to confirm this, I'd like to look at the specification more carefully.

Q. Okay. And I can point you to something if it would be helpful, Dr. Khatri.

A. Yes.

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Q. Let me just direct your attention to column 3 starting at around line, you know, maybe 17 to 21?

A. Okay. Thank you. In fact, I just reached there.

But what this is describing is that the -- I mean, I'm reading lines, column 3, line 17 on. It says the discontinuous ESD buses E1, E2 and E3, which we can see in Figure 2, may be connected together by connecting the pads 22 of the pad groups G1, G2 and G3. So pads 22 of the pad groups which are labeled G1, G2 and G3 you can see on the figure on the left. And these are connected to the common ESD bus 24 through the bonding wires 25.

So this disclosure shows that the discontinuous ESD buses, E1, E2 and E3 are connected to the common ESD bus 24 by way of the bonding wires 25 through specific pads in the pad groups G1, G2 and G3.

Q. How are the discontinuous ESD buses E1, E2 and E3 connected to the pads

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22?

MR. WATSON: Objection. Form.

A. So, you know, I think I mentioned to you earlier that, you know, where I cited the '164 Patent defining an ESD bus -- this was column 1, lines 32 to like 34 where it says, you know, an ESD -- sorry -- an electrostatic discharge (ESD bus 11) and then defines that bus, it says an example, a layout trace connected to a ground or system voltage.

In other words, the buses E1, E2 and E3, which are labeled as ESD buses, are connected to a ground or a system voltage.

The way in any chip that you connect anything to any voltage is by way of pads because that's the only electrical connection into the chip.

So when a person of ordinary skill in the art reads that an ESD bus E1, E2 and E3 is a layout trace connected to a ground or a system voltage, they know that this connection is made by way of a ground

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pad or a system -- I mean or a reference pad that would connect the ESD bus, E1, E2 and E3, to the ground terminal.

Q. Yeah, so my question is a little bit different, Dr. Khatri. Maybe I can try to ask it a little bit better.

I'll zoom in a little bit here on Figure 2. So Figure 2 shows a bond wire 25, correct, going between pad 22 and the common ESD bus 24.

Do you see that?

A. I mean, I think I see what you're pointing at.

Q. And so, you know, you just read a passage that said, you know, E1, E2 and E3 are electrically connected to one another by the ESD bus 24.

The question I have is: How is the ESD bus E1 connected to pad 22?

A. I see. Again, like I said, a person of ordinary skill in the art knows that -- it knows that based on the '164 Patent the ESD bus is defined as a layout trace connected to a ground or system

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voltage.

In other words, they know that the ESD bus, let's say E1, is connected to a ground or system voltage.

Person of ordinary skill in the art looks at E1 and says, oh, that's an ESD bus. According to the patent, you know, it says an ESD bus is a layout trace connected to a ground or system voltage.

So step one, the person of ordinary skill in the art understands that the bus labeled E1 is connected to a ground or system voltage.

The person of ordinary skill in the art also knows that these little squares with Xs in them are labeled as pads because that's disclosed in the patent as well.

And a person of ordinary skill in the art also knows that, you know, certain amount -- some certain of these pads are ground pads in any chip. So those ground pads would have an electrical connection to the ESD bus E1 and that's something

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that a person of ordinary skill in the art would just know from having made chips.

And like I said, you know, the level of detail in these figures is not sufficient to know that connection, but that's something a person of ordinary skill in the art would readily understand.

Q. Would a person of ordinary skill in the art understand that all of the pads at 22 corresponding to ESD bus E1 are connected to the ESD bus E1 or only certain of the pads?

MR. WATSON: Objection. Form.

A. So, you know, once again, I lean on the specification.

So if you look at the place in the specification for Figure 2 where pads 22 are introduced -- I'll just sort of look for that and read it to you.

Let's see. I'm trying to find it.

Q. You may be referring to column 3 around line, starting at line 6.

A. Yes, okay.

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So if you look at column 3, line 6 or 7, it says: Each of the plurality of pad groups G1, G2 and G3 -- and we're looking at Figure 2, so we see three labeled pad groups, G1, G2 and G3. So it's talking about each of these pad groups. It says it includes at least one pad 22.

So there could be, you know, one of them has 6 pads, one of them has 4 pads, et cetera.

Has at least one pad 22 wherein pad 22 is an input/output pad connected to a ground or a system low voltage.

So a person of ordinary skill in the art reading this knows that one pad -- at least -- sorry, at least one pad 22 is, in each of the pad groups, is such that it's connected to a system low voltage.

Q. And the connection between, you know, the one or more pads 22 and E1 is not expressly shown in Figure 2, is it?

A. Can you repeat that question?

Q. Yeah, is the connection between

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the one or more pads 22 that are connected to E1, is that connection shown in Figure 2?

A. Yeah, so I mean, you know, the description is, you know, it augments the figure. The figure, you know, clearly, like I said, could not show all the details because in a real integrated circuit, you know, there would be millions of different rectangles and structures and features. So you simply couldn't show them all in detail in a figure like this.

So a person of ordinary skill in the art would look at Figure 2 and would look at the specification together and make -- you know, and with their understanding as a person of ordinary skill in the art, they would make, you know, a reasonable conclusion about what is disclosed in the patent based on looking at the specification and the figures, not just one of them in isolation are.

Q. What is numeral 23 in Figure 2?

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A. Let's see. Again, I'll sort of, like, scan through the beginning of the description of Figure 2. So let's see.

Numeral 23 first occurs or appears on line -- column 2, line 55 and I'll read that. It says the circuit area 20 -- if we look at Figure 2, there's a label 20 which is a circuit area -- the circuit area 20 is formed by a plurality of chip edges 23.

So if you look at -- so 23 are chip edges and there are, I believe, two labels are called 23, which are the edges of the chip that is described in Figure 2.

Q. In Figure 2 is a common ESD bus 24 part of the chip or external to the chip?

A. Let's see. So let's look at the description for common ESD bus 24.

The first description of common ESD bus 24 occurs on column 2, line 52 where it just says -- it just enumerates the objects that are present in the, in Figure 2. It's just listed as a common

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ESD bus 24, among other components inside Figure 2.

But if we look further at column 2, lines like 63 or 64, it says: A common ESD bus 24 -- that's what we're talking about -- is formed outside the chip edges 23 -- we just described what the chip edges were in this figure.

So the common ESD bus is formed outside the chip edges 23, and it says, which is not limited. So that's basically our description of the common ESD bus and it says that it was formed outside the chip edges 23, which is not limited.

Q. Keep the '164 Patent open and turn to paragraph 66 in your declaration, please.

A. Okay.

Q. And I'll share that on the screen as well.

A. Okay, I have paragraph 66 open.

Q. Kind of toward the bottom of that paragraph there's a reference to or discussion of five pad types.

S. KHATRI

Do you see that?

A. Let me read this part.

Okay, I read that paragraph.

Q. Yeah, and in that paragraph you identify five pad types, correct?

A. Yes, it does say one of five pad types. It enumerates five pad types.

Q. And what are the five pad types that you list in paragraph 66?

A. So, you know, as you see in paragraph 66, the five pad types are described to be of type input, output, in/out, supply and reference.

Q. And what are the -- in terms of the bond pads themselves, what are the differences between an input pad, an output pad, an in/out pad, a supply pad and a reference pad?

A. I'd like you to repeat the question. Are you saying what's the difference between these five in terms of the bond pad?

Q. Correct, yeah, with respect to the bond pad itself, what is the

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difference between an input pad, an output pad, a supply pad, a reference pad and an in/out pad?

A. So I think that question is not completely formed -- not answerable as cast.

Q. I guess what don't you understand about the question?

A. So I don't know when you say with respect to bond pads, it's just like that's just sort of a very -- it's one piece of these pads. So it sort of sounds like -- it sounds like an odd way of characterizing the -- you know, of characterizing a question.

Q. So let me maybe drill down a little bit.

Suppose you have a design and there is a pad that is going to be an input pad and there's another pad right next to it that's going to be an output pad.

Before those pads are connected to a bond wire, what is the difference

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between the pads?

MR. WATSON: Objection. Form.

A. Right. So I mean, the reason the question is hard to answer is, I don't know what you mean by a pad. Because, you know, in common use pad can be -- I think you might be just referring to a portion of the pad or the entirety of the pad, or I don't know really what you mean by "pad."

Q. Well, let's use the pad as described in the '164 Patent and I'll point you to Figure 2, you know, numeral 22, which is the patent identified as a pad.

A. Okay. Let's see. So the numeral 22, let me just go to column 3. It says the pad 22 is connected to a ground or system low voltage. So it's basically a ground pad, it's one kind of pad.

Q. And yeah, so that's what I wanted to ask. What makes pad 22 a ground pad?

A. What makes pad 22 a ground pad is the fact that it has a connection, you

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know, to the -- you know, to the ESD bus or the ground reference -- you know, to the ground reference line inside the chip. So it basically connects to the ground reference inside of the chip. That's what would make it a ground pad.

Now, also you want to basically, you know -- this ground pad basically connects to the ground terminal inside the chip, which is basically all over the chip.

Q. If pad 22 is connected it a power rail instead of a ground rail, would it then be a power pad?

A. So I want to be careful about that because pad 22 in the '164 Patent is specifically taught as something that's connected to the system low voltage. So I don't want to change the language of the patent in my answer because I think, you know, that can be misconstrued in terms of what I say. So I can't answer your question as posed.

Q. What if the pad just to the left

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of pad 22 is connected to a power rail? What type of pad would it be in that circumstance?

MR. WATSON: Objection. Form.

A. So, you know, like I said, you know, in my declaration, in paragraph 66, pads can be of, you know, five types, input, output, in/out, supply and reference.

So if any pad was connected to the reference, you know, the reference terminal inside the chip, which can be, you know, all over the chip, then it will become -- it would be called a reference pad.

And if a pad was connected to the supply terminal inside the chip, it would be called a supply pad.

Now, of course, there may be more than one type of supply or more than one type of reference. But this is just something I'm saying in a general sense.

I think we've been going for a good -- for about an hour. I think it

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might be a nice time for me to take a break.

Q. Yeah, let me just ask maybe one or two more questions and then we can take a break.

A. Okay.

Q. So keeping with Figure 2 in the '164 Patent, right, in the pad group G1, rightmost pad 22 is shown as being connected to the ESD bus 24 via a bond wire, correct?

A. You know, in Figure 2, you know, as described -- let me just make sure that the text matches what we're saying here.

In Figure 2, let me see, where's that -- I'm looking for this. Oh, there we go, I think. Okay.

So Figure 2, you know, column 3, lines like 6 onwards say each of the plurality of pad things G1, G2 and G3 includes at least one pad 22. So you highlighted one of them in the -- on the screen.

And then it says: Wherein the

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pad 22 is a pad -- and I'll skip a few words just to make it brief -- is wherein the pad 22 is connected to a ground or a system low voltage. So this pad is connected to a ground or a system low voltage.

And then, you know, it also says later that -- oh, yeah, there we go, on lines 17 of column 3 again, it says, you know, ESD buses E1, E2 and E3 may be connected together by connecting the pads 22 of pad groups G1, G2, G3. That's the ground reference terminal pads, reference pads, to the common ESD bus 24.

So pad 22, if it's highlighted as disclosed by the spec of the patent in lines -- in columns 3, lines 18 to 20 says that, you know, pads 22 of the pad group G1, G2, G3 are connected to the common ESD bus 24.

Q. And because the rightmost pad in group G1 is connected to the system low voltage, that's what makes it a reference pad?

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MR. WATSON: Objection to form.

A. Well, I mean, you know, the specific disclosure of the patent is in lines 3 -- sorry, in column 3, lines 7 to 9 where it says the pad 22 is a pad connected to a ground or a system low voltage. So it's explicitly stated in the patent.

Q. So you bring up a good point there, right. The patent characterizes pad 22 as an input/output pad, correct?

A. It's just characterized as one of the pads of the design. It just says it's an input/output pad.

Q. And it goes on to say that that's connected to a ground or a system low voltage, correct?

A. Correct, it's connected to a ground or a system low voltage. That's basically how the pad 22 connects to, you know, the system reference. So it's sort of what you were just asking a little while ago.

Q. Yeah, so that's what I'm trying

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to understand is, you draw a distinction in paragraph 66 of your report between input pads, output pads, supply pads, reference pads, but the patent calls it, you know, pad 22, an input/output pad that is connected to ground.

So I'm trying to understand, what is the distinction you were attempting to draw in paragraph 66 between an input pad, an output pad, a supply pad and a reference pad?

MR. WATSON: Objection to form.

A. Yeah, so, you know, paragraph 66 refers to the disclosure of Yoshinaga. So basically the language that's used in Yoshinaga, you know, is what I'm referring -- I mean, what I'm leaning -- I mean, what I'm using here in paragraph 66. And I'm responding to the language of Yoshinaga.

So, in particular, Yoshinaga says, you know -- Yoshinaga labels -- if you look at Yoshinaga -- Yoshinaga labels certain pads as supply pads.

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These are shown in Figure 6 and these labels are labels 3 -- well, let's see, I'm going to look at unmodified, unaltered Figure 6 in my declaration. So let's see. Let me find that. There we go.

So, you know, if you look at page 32 of my declaration on the figure on the left, which is the unmodified figure from Yoshinaga, you know, Yoshinaga discloses that pads labeled 3, 4 and 58 are supply pads, and this is in paragraph 88.

And also Yoshinaga specifies that there are certain pads that are ground reference pads, but they are not -- they're not shown in this Figure 6.

So those are not shown here. But it does label them again in paragraph 88 and it has -- let me just open Yoshinaga -- and those labels -- if you tell me the number of Yoshinaga, please, the reference number?

Q. Yeah, it's Exhibit 1006 and I can just go ahead and show that on the screen.

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A. Okay, 1006, I got that here.

And if you look at paragraph 88, so paragraph 88 says labels 3, 4 and 58 are power supply pads, like I just showed you on Figure 6.

And Figure 6, you know, Yoshinaga in paragraph, I think it's 84 -- let me see -- let's see, it was 86, I think. Let me search....

Okay, there you go, it's 78, sorry. Paragraph 78 says: Reference potential pads are not shown for simplicity.

So we know that in Figure 6, reference potential pads are not shown. And these reference potential pads as shown in paragraph 88 are numerals 5, 6, 39 and 40. So 5, 6, 39 and 40 are not shown in Figure 6, but they are reference potential pads.

So Yoshinaga has described reference pads and power pads, and that's why in the list of pads that I have on page 66 -- sorry, in paragraph 66 of my

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declaration, I have supply and reference pads as two of them.

And this paragraph 66, as I was saying, refers to, you know, refers to Yoshinaga.

And then I have three other kinds of pads, inputs, outputs and in/out.

And again, in Yoshinaga, there are -- if you look at Figure 6, there are certain unlabeled pads.

So these pads, by them not being labeled, they're clearly not supply pads. They're clearly not reference pads, because reference pads are not shown.

So that any of the other kinds of pads that a person of ordinary skill in the art would use in a chip design.

And a person of ordinary skill in the art, when they're designing a chip, they know that pads, you know, they're functional pads or the signal pads would be -- some of them would be input pads that drive input signals into the chip, some of them are output pads that drive

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signals out of the chip and some are pads that drive inputs or outputs depending on, you know, whether the chip is driving out something or reading something.

So a person of ordinary skill in the art would know that the unlabeled pads in this figure, Figure 6, are input or output or in/out. And that's why I have those three types of pads, plus reference, plus supply. But that's pertinent to Yoshinaga, which is one of the references that Dr. Foty and the petition, you know, cite to or use as one of -- as the grounds.

Q. Is it your testimony then, Dr. Khatri, that the Yoshinaga reference uses pads in a manner different than the '164 Patent?

MR. WATSON: Objection to form.

A. So a person of ordinary skill in the art, when they look at -- when they look at these, you know, the pads as described by Yoshinaga, they would know that basically that, you know, that any

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chip needs -- that needs supply pads, they need reference pads and they also need inputs and outputs and in/outs.

There's nothing in here that's basically, you know, that's basically different than what a person of ordinary skill in the art would readily understand about chips.

I think we've gone much about one hour. So I'd like to request a break at this point.

MR. JENSEN: Sure. Let's go off the record.

THE WITNESS: Okay. Thank you.

(Recess taken from 2:09 p.m. to 2:19 p.m. MT)

BY MR. JENSEN:

Q. Before the break, Dr. Khatri, we were looking at the '164 Patent in column 3, lines 6 to 9. So let me direct your attention there.

A. Okay. Let me open that as well. Column 3, yeah, okay.

I'm at column 3, line 6-ish of

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the 164.

Q. And in that passage, it says that a pad that is connected to ground is an input/output pad.

Do you see that?

MR. WATSON: Objection to form.

A. Right. So in some sense, you know, like, I'll just read this out to you aloud. It says: Each of the plurality of pad groups G1, G2 and G3 includes at least one pad 22, wherein the pad 22 is an input/output pad connected to a ground or a system low voltage.

So a person of ordinary skill in the art, again, when they're reading this, particularly when they have read that this is an ESD patent, particularly also when they see that the ESD bus is defined as a layout trace connected to a ground or system voltage, when they see all this, they say this is an ESD patent where the ESD bus is some electrical trace that's connected to a system or ground voltage, and also when they read this disclosure

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that pad 22 is an input/output pad connected to a ground or a low system voltage, they would readily understand that pad 22 is basically what we've been talking of as a ground pad.

So this is something, again, that a person of ordinary skill in the art, with their background and also with the intrinsic disclosures of this '164 Patent would readily conclude.

Q. Would you agree that pad 22 in the '164 Patent, when it's connected to ground, is an input/output pad?

MR. WATSON: Objection to form.

A. I have no idea what you're asking. And so that's something that I don't know -- I mean, it's a question that's not well formed.

Q. I'll try to form it better then.

A. So as I've been saying, you know, the form -- the way I interpret this, right, this line, that's column 3, lines 6 through 9 -- 6 through, I guess, 9, yeah, is that a person of ordinary skill in the

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art would look at this and say, oh, pad 22 is something that's -- and then connected to a ground or system low voltage.

That means that pad 22 is connected to the system low voltage or ground. And that's why they'd say, okay, that makes sense because it's been connected to the ESD bus as shown in Figure -- was it 2, I forget -- was it 2? We were talking about Figure 2, not 3, I think. Yeah, Figure -- let me just double-check -- yeah, Figure 2.

So as shown in Figure 2, they also see -- see they're putting all this together, right, they're putting everything together in the context of the patent, it's all about ESD.

And when it's about ESD, you know, I, a person of ordinary skill in the art, knows that there's going to be a discussion about ground voltages. And the patent clearly says that. It says that ESD bus is a layout trace connected to a ground or system voltage. That's one

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thing in the mind of a POSA, is basically there's going to be a discussion of ground pads.

And then they also look at the Figure 2 when they actually see that, you know, this is connected to an external -- I'm sorry, it's connected to a common ESD bus 24.

Common ESD bus 24 is, again, an ESD bus. And so a person of ordinary skill in the art looks at the definition of an ESD bus, says that's a layout trace connected to a ground or a system voltage.

So therefore, it all makes sense to them that pad 22, which is connected to common ESD bus 24, is a ground pad. Which also this disclosure says, where it says wherein pad 22, you know, is connected to a ground or a system low voltage.

A person of ordinary skill in the art reading this readily understands that, you know, that pad 22 is a pad that's connected to, you know, a ground or a system low voltage.

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Q. Let me try asking the question this way.

In the '164 Patent, what is the difference between an input/output pad and a ground pad?

A. See, I think this is the, I think this is the confusion or conflation, I don't know which. But here's the situation.

Yoshinaga, for example, is very explicit about all the different kinds of pads that they have. Yoshinaga talks about specifically reference pads, talks about, you know, reference pads, of course, that are not shown in Figure 6. But it also talks about supply pads.

And then, of course, it's actually drawing locations of other pads which a person of ordinary skill in the art would infer input or output or in/out.

And also locations of these pads are specifically designed. Yoshinaga is very explicit about the pads and where they are located.

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The '164 Patent is only concerned about talking, you know, is only concerned about the -- it's concerned about ESD. And because it's concerned about ESD and ESD buses, which are ground, you know, which are, as I just read from the disclosure of the '164 Patent, right, that ESD bus from column 1, lines 34 -- 33 to 34 are layout traces connected to a ground or system voltage.

So the '164 Patent is concerned about ground and system low voltage. That's basically all it's focused about because that's what's pertinent to ESD.

ESD is, you know, basically an event where excessive sort of voltages which come from a human body or a machine model, they're discharged through the ground terminal. That's why ESD -- ESD buses are, quote, a layout trace connected to a ground or system voltage.

So the '164 Patent is just focused on ground. It is not talking about other voltages. It's not talking

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about, you know, what's the functionality of the -- it's very narrowly focused to the ground. It is not disclosing all these other pads and their locations or anything like that because its focus is different.

Yoshinaga, on the other hand, explicitly shows Figure 6, which has specifically designated, you know, pads which are at different locations, which have different functionalities and so on.

So that's, I think, what's causing the possible sort of conclusion -- confusion.

MR. JENSEN: Yeah, so we'll move to strike that as nonresponsive. My question was specifically limited to the '164 Patent and I'm not asking about Yoshinaga. So we'll reserve our rights on that and move on.

MR. WATSON: Well, we, of course, disagree, but we'll continue.

Q. Let me direct your attention, Dr. Khatri, to Figure 3 in the '164

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Patent.

A. Okay. Let me -- I'm going to go there. Would you like to share it on the screen so I can look at the text of it, so I have both on the same monitor?

Q. I'm happy to do that.

A. Thank you.

Q. Let me know when you're able to see that.

A. I'll tell you when I can see it. I see it now.

Meanwhile, let me go to the spec where it talks about Figure 3. I'm trying to find that.

Okay. Here we go. I've located the spec for description of Figure 3.

Q. Is Figure 3 an embodiment of the invention in the '164 Patent?

A. Let me confirm that by looking at the patent. I am in column 2, line 35 to 37, where it says: Figure 3 is a schematic diagram of an integrated circuit ESD bus according to an embodiment of the present invention.

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So, yes, Figure 3 is an embodiment of the present invention.

Q. And what does numeral 35 represent in Figure 3?

A. Okay, let me see. I'm going to now go to the spec. It was column 3, I think. The first time numeral 35 was described is on line 40 and 41 where it's listing the list of elements in the schematic diagram of Figure 3 and it says, you know, that one of the -- one of the elements inside ESD bus structure 3 is "a plurality of bonding wires 35." And this is on line 40 and 41.

So Figure -- I'm sorry, numeral 35, and there are two of them described here, but these are a plurality of bonding wires or equivalently bond wires 35.

Q. How many bond wires are shown in Figure 3?

A. Figure 3 -- again, you know, when a person of ordinary skill in the art reads this, they won't literally look at Figure 3. They'll look at the figures and

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the spec because they're both intrinsic data, intrinsic evidence.

But in Figure 3, there are two bonding wires labeled 35. However, the specification says a plurality of bonding wires 35, which means there could be more than two bonding wires 35. Figure 3 being just an example.

Q. And we talked earlier when we were discussing bond wires more generally about some of the problems you identified in your declaration related to bond wires.

Do you recall that discussion?

A. Yes, I do recall that.

Q. And one of the problems that you identified with using bond wires was that a bond wire could droop or sag and cause a short-circuit.

Do you recall that?

A. I do recall that, yes. And the important thing that I wanted to sort of mention here is that, you know, that -- you know, all the problems that I described about bond wires, and as I

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recall, there was this discussion where we talked about, you know, on-chip metallization and bond wires.

And I showed that basically out of the two, the choice of bond wires, right, to connect bond pads to bond pads, in the conventional wisdom, this is before the '164 Patent, before the '164 Patent the conventional wisdom was, you know, bond wires are not even an option.

So in some sense, right, bond wires was not even a design choice. The only option really was on-chip metallization and anybody of the other ways of connecting bond pads, which I described to you were many among them being connecting by diffusion or by other means, right.

So what I'm trying to say is that, you know, the only reason we discussed bond wires at that time was that -- particularly Dr. Foty brought it up. And I was trying to say bond wires to connect I/O pads was not an option based

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on the conventional wisdom that a person of ordinary skill in the art understood at that time -- at the time of the patent, you know.

So what I was trying to tell you is out of the two sort of alternatives, the bond wire alternative -- and I gave up multiple reasons -- was a non-starter. It was not even an option. It was not a choice that someone would even -- a person of ordinary skill in the art would have considered. Because bond wires had those problems we talked about, you know, the drooping and sagging and shorting, which is fatal, and also the exposure to the elements, you know, and also the high inductance and the high noise.

So that was the conventional wisdom. That's what people understood before the '164 Patent.

But the '164 Patent, the inventive feature of it was to use these, but that's basically -- that's kind of the teaching, if you will, of the '164 Patent.

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Q. And Figure 3 shows the bond wire 35 on the right-hand side going over part of the circuit area 30, correct?

A. Again, you know, Figure 3 is, you know, as I said before, Figure 3 is not a literal figure. Like, for example, you know, just the fact that Figure 3 shows two bond wires doesn't mean that the patent is limited to two bond wires.

So Figure 3 showing basically the bond wires in a certain shape doesn't limit the patent to the bond wires being in a particular shape, because that's not what the patent even describes, the shape of the bond wires.

All that the patent discusses is what I was showing you in column 3, line 40 and 41, which is a plurality of bond wires 35.

Q. Yeah, so my question, I think, was much simpler than that, is does Figure 3 show a bond wire 35 connecting pad group G2 and G3 go across part of the circuit area 30?

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MR. WATSON: Objection to form.

A. You know, again, I'll say this one more time, right. Like this, the fact that this patent -- this patent is teaching something new and the inventive feature of the patent was to use bond wires to make the connections, you know, between pad groups.

So that's the inventive feature. That's basically how it -- you know, how it was different from the conventional wisdom, which I described to you a person of ordinary skill in the art knew and would know that based on the conventional wisdom this would be, you know, the use of bond wires would be a non-starter.

But the '164 Patent exhibits the conventional wisdom and says, you know, this could be a way to do, you know, to do ESD designs, particularly for ESD designs.

MR. JENSEN: Yes, again, non-responsive.

Q. I'm just trying to -- we're looking at Figure 3 in the '164 Patent?

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Do you see the figure?

A. I do see the figure, yeah.

Q. Okay. Does Figure 3 show a bond wire 35 connecting a pad in pad group G2 to a pad in pad group G3?

A. I do see a bond wire labeled 35 connecting the rightmost pad of pad group G2 to the leftmost pad of pad group G3.

Q. Does Figure 3 show that bond wire going over or across part of circuit area 30?

MR. WATSON: Objection to form.

A. Once again, a person of ordinary skill in the art seeing this would not necessarily assume that this is -- the length and the shape and the actual contour of the bond wire is literally.

A person of ordinary skill in the art would see Figure 3 as having lots of sort of abstract features.

And all that they would take home is saying that this bond wire is used to connect a pad of pad group G2 with a pad of pad group G3.

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And they wouldn't take this figure and the disclosure of the figure as literally as you're suggesting.

Q. By that same token, Dr. Khatri, would you agree that the figure reproduced in paragraph 40 of your declaration taken from the petition, which shows a bond wire between the pads labeled 5 and 6, would you agree, using your same logic, that the bond wire shown in connecting pads what are labeled 5 and 6 in your declaration is not going over part of the circuit area designated in orange?

MR. WATSON: Objection to form.

A. Okay. So, that was a long question I didn't quite catch it. So can you repeat the question, please?

Q. I can. And let me find maybe better example.

Actually, let's look at the petition itself -- or since that's not in the materials you have, let's look at Dr. Foty's declaration, which I believe is Exhibit 1003. And I'll share that on the

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screen.

A. Okay. I have opened that.

Q. And you reviewed Dr. Foty's declaration when forming your opinions, correct?

A. Yes, I have reviewed it and responded to portions of it.

Q. And I'll direct you to a specific paragraph. Let's look at paragraph 153 of Dr. Foty's declaration. I'm sharing that on the screen.

A. Wait, I think you're on paragraph 154, though, correct?

Q. 154 follows the figure.

A. I see. So you're referring to the figure, I think, in your discussion?

Q. Yes, the figure.

A. I see, okay.

Q. Did you recognize this as a modified version of Figure 6 from the Yoshinaga reference?

A. This is the -- let me go to my declaration where I show this figure. Just give me one second. I'm going to go

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find it.

Q. If you prefer to use the one in your declaration, let's just go to paragraph 40 of your declaration and I'll zoom there.

A. Yeah, let's do that.

Q. And this is a figure that you copied from Dr. Foty's declaration or the petition, correct?

A. Correct. The figure on the right, which is covered, is the manipulated figure that Dr. Foty provides, which manipulates the figure on the left which is the original figure in Yoshinaga.

And there are multiple ways it's been manipulated which I describe in my paragraph in this section, which is around G1.

Q. And one of the modifications that was made was the addition of this kind of black curved line at the top which represents a bond wire, correct?

A. Well, one of the many modifications was made that, you know, is

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the two pads that are like at the -- you know, you know there are 10 pads on the top row. So the fifth pad from the left and the sixth pad from the left have been labeled 5 and 6, which are labels for reference potential pads. So that's one change, among many.

And then these pads have been -- these pads 5 and 6 have been connected by that sort of like the curved black line, which, you know, which Dr. Foty discloses is a bond wire.

Q. Yeah, is it your understanding of this figure that the curved black line representing a bond wire is going over the area of the circuit colored in orange?

A. You know, first of all, as I mentioned, right, like the modifications are not legal, okay. And the second observation is that, you know, I -- you know, Dr. Foty claims that this orange area is a saved area, which I also contest.

So there's a lot of stuff I

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contest about this area. So in some sense, right when you ask me in this figure, which is fundamentally broken or fundamentally hyper-modified and then incorrectly, you know, incorrectly characterized, you know, does a black line, you know, go over an orange area -- I mean, visually it seems to, but it maybe not because it sort of goes slightly over the orange area.

That said, you know, I contest everything about this modification. I contest everything about the construction of the orange area. And I contest, you know, like whether a person of ordinary skill in the art in the context of Yoshinaga would be even motivated to go through this entire exercise that Dr. Foty has gone through, which seems to be an exercise of pure hindsight.

Q. So yeah, I'm just trying to ask a very specific question.

Do you agree that in the figure we're looking at, the modified version of

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Yoshinaga Figure 6, that the curved black line representing a bond wire is crossing over the orange part of the image?

A. Okay. So once again, right, this -- you know, I disagree that this figure would be something that a person of ordinary skill in the art would ever come up with or even consider, and that this figure, the construction of it is flawed.

So in some sense, right, you know, whether or not in this figure there's a curved line touching an orange area is sort of moot. But visually in this flawed and non-functional figure, which a person of ordinary skill in the art would never want to implement, there is a curved line, which seems to be touching an orange area.

That doesn't mean -- that doesn't mean -- that doesn't mean that I'm saying it's a valid circuit. It is simply an invalid circuit that a person of ordinary skill in the art would never consider.

Q. And if we come back to Figure 3

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of the '164 Patent, I want to ask basically the same question.

Does Figure 3 of the '164 Patent show a bond wire 35 on the right-hand side of the image crossing over a portion of the circuit area 30?

A. The big difference is that this is an inventive feature of the patent. This is a patent going against conventional wisdom and saying let's do things differently.

But before this patent is what the IPR is talking about. The IPR, the references in the IPR, which would be Saint, Haralabidis and also Yoshinaga, is something that the petitioner and Dr. Foty are presenting as evidence that there's something like what is taught by the patent would be obvious.

But what I'm trying to tell you is that before this patent, you know, everyone thought that this was a really bad idea, and I've given you -- I'm sorry, everyone thought that connecting bond pads

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to bond pads with bond wires was a bad idea, and I gave you multiple reasons for that earlier in this -- I've given specifically three reasons.

So the conventional wisdom was don't go there, don't do this. So that's why all the prior art references, you know, you know, that the petitioner and Dr. Foty present are something that a person of ordinary skill in the art would not even consider. It would not even be a design choice or an option that they would even think about.

But that's what the patent very inventively says, wait a minute, let's stop and revisit this and see and then shows that this is something -- this option is something in the context of ESD that makes a lot of sense to do.

MR. JENSEN: So, strike that as nonresponsive.

Q. I'm not asking whether something's inventive or not inventive, or conventional or not conventional.

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S. KHATRI

I'm simply asking, what is shown in Figure 3 and --

MR. WATSON: Objection to form.

Q. Would you agree --

MR. JENSEN: Let me ask the question.

Q. Would you agree with me, Dr. Khatri, that Figure 3 shows a bond wire 35 on the right-hand side of the image that is crossing over the top of at least part of the circuit area 30?

A. The important --

Q. Or was it going around it or under it? Right? I'm just trying to figure out what is shown. Is it going over it, around it, under it, or something else?

MR. WATSON: Objection to form.

A. Sorry, now the question was a little too long. So I didn't quite understand it. May I ask you to repeat it?

Q. Let me try and ask it this way.

A. Yes.

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Q. Is bond wire 35 on the right-hand side of Figure 3 going over, under, around or something else part of the circuit area 30?

MR. WATSON: Objection to form.

A. So a person of ordinary skill in the art looking at Figure 3 and knowing that many aspects of Figure 3 are sort of notional, they're not exact, they're not something that's an exact die photograph or something -- so a person of ordinary skill in the art looking at Figure 3 would look at the -- you know, would look at the shape that's labeled 35 on the right and just conclude that that's a shape that's used -- I mean, that's a shape that represents a bond wire and it's used to connect the rightmost pad of pad group G2, with the leftmost pad of pad group G3, and that's it.

And that's just the -- that's what they would take from it because they would take that abstract idea away from this figure.

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They won't be, they won't consider this to be a literally figure because it's not a photograph of a chip, it's not a specific layout diagram of a chip. It's a notional diagram. It's just saying this is how this -- you know, it's showing connections in an abstract, you know, in an abstract fashion.

And so that's all that the person of ordinary skill in the art would take away from it. And they would take away from it that idea and say, well, that's the inventive feature of this patent.

That's what -- you know, if I was a person of ordinary skill in the art reading it, it's like, oh, that's what this patent teaches, hmm, this goes against my conventional wisdom because I've been taught by all these prior art references that this is something you shouldn't do. But this is showing me a new way of looking at things. This is the inventiveness aspect, which I think is important.

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I know you said that's unresponsive, but I think it's important to understanding the distinction between Figure 3 here in the '164 Patent and Yoshinaga -- or the massively manipulated version of Yoshinaga that Dr. Foty provides.

They're kind of qualitatively different. One of them is prior -- one of them is alleged prior art. One of them is an inventive feature of a patent.

So in some sense, you know, you can't really be comparing them is what I'm trying to say.

Q. Let me try it this way because I think we're still at the nonresponsive stage.

What is the label SA 2 in Figure 3 intended to reflect?

A. So let's look at the patent to -- before we make that -- so we can make that accurate determination accurately.

I'm looking at patent 2 -- sorry, I'm looking at Patent '164 and column 3.

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Let me find it. Let's see.

I'm having difficulty. I don't see the label directly. So it may be just expanded out maybe.

Sorry, I think it's -- this is the first occurrence, which I believe is on column 4. So let's see. I think I'll go there.

Column 4 -- and if I'm not mistaken, this is not described earlier -- but column 4 sets at lines-- line 20-ish. I'll read that.

It says: For example, ESD bus 11 and the filler cells F1 and F2 shown in Figure 1 -- we've gone over those -- are replaced by saved areas SA1 and SA2 in Figure 2. And that's the circuit area 20 may contain the circuits with irregular shapes in different areas without increasing its area, which saves production cost.

Q. Would you agree with me, Dr. Khatri, that the bonding wire 35 on the right of Figure 3 is formed across

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circuit area 30?

A. Again, to answer that question, I would put myself in the shoes of a person of ordinary skill in the art. That person would look at this figure and, first of all, not take this figure literally. If they're going to look that the figure and say, you know, these are notional diagram -- I mean, these are notional diagrams, these are sort of -- you know, these are not layout diagrams, they're not photographs that basically teach the teaching of the inventiveness or teaching of the '164 Patent.

So they take this figure and say, all that I'll take away from this figure is that this bonding wire 35 on the right is something that connects the right terminal of pad group G2, the rightmost terminal pad group G2, with the leftmost terminal of pad group G3.

Again, they wouldn't take this to be literally as you're suggesting, particularly because if they look at the

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other bonding wire 35, this other bonding wire 35, which connects the rightmost group of pad group G1 with the leftmost group of pad G2, that's going in a different direction.

So they understand that this is basically a notional idea, these are not to be taken literally.

Q. Let me -- I was just reading from the patent, Dr. Khatri. So let me direct you to where I'm reading from the patent because I think you're fighting against something that is really not controversial and expressly stated in the patent.

So let me direct your attention to column 3, lines 54 to 55, and I'll just read the first part of that: The plurality of bonding wires 35 -- this is discussing Figure 3, by the way, with specific reference to Figure 3, it says: The plurality of bonding wires 35 is formed across the circuit area 30.

So let me just ask, do you agree with that statement in the patent

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describing Figure 3 that the plurality of bonding wires 35 is formed across the circuit area 30?

A. Yeah, so if you -- if I read this, right, I read this section, it says the plurality of bonding wires 35 is formed across a circuit area 30, I certainly agree with it, but I also --

Q. We can pause right there then. I'll let you finish, but that's all I wanted to establish, is that the bond wire is going across circuit area 30 so I can ask another question.

A. But I also see that a person of ordinary skill in the art would not look at Figure 3 and interpret it literally.

Because, you know, one of the plurality of bonding wires that's SA1 -- sorry, that's 35 on the left, does not explicitly, you know, form -- is not formed explicitly across the circuit area.

So the actual figures are notional, but the text is something that they would use and supplement their

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understanding of the figure.

Q. And we talked earlier about, you know, problems that can be caused when a bond wire sags or droops and then you say, for example, it could cause a short-circuit, correct?

A. And that's what I said, was the conventional wisdom. That's the sort of conventional wisdom that Saint thought, that's conventional wisdom that was prevalent before this patent.

Q. And so what does the '164 Patent teach to avoid the problems of sagging, drooping and short-circuits that can be caused due to bond wires?

A. So, you know, once again, right, these problems are conventional wisdom problems. And so in some -- you know, these problems might be something that once the inventors of this patent tried them out they realized or they were able to realize that they were not as, you know -- these conventional wisdom issues were not what they were, you know, what

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not were they were made out to be.

And that could be one -- I mean, I'm sort of saying that that's something that they could have solved this technology issue. That's something that's completely possible because technology advances.

And then, you know, if, for example, in the future someone hypothetically again, you know, if they used this idea or they copy this idea, that would be, again that would be evidence that this was a good idea.

So the inventiveness of the '164 Patent, the '164 Patent is to use this thing which conventionally everybody thought was a bad idea.

Q. How did the '164 Patent solve the problem of bond wire sagging and droop?

MR. WATSON: Objection to form.

A. You know, once again, this -- you know, the problem of bond wire dragging and drooping was something that conventional wisdom thought was the

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situation.

It's also possible that, you know, the technology of bond -- of applying -- sorry, of running bond wires in the meanwhile had gotten good enough that that conventional wisdom was not true anymore.

I am -- you know, these are all sort of possibilities. I am not saying that one or the other is the actual situation. Because that's not what I've studied.

But the point is that this is the inventive feature and this goes against conventional wisdom, you know, which before this patent was don't do this type of wire bond connection between bond pads and bond pads. But the '164 Patent specifically teaches doing that particularly in the case of, you know, of -- in an ESD context.

Q. How did the '164 Patent involve the problems you described earlier of inductance and noise associated with bond

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wires?

A. You know, once again, depending -- you know, in a design situation, in an example of a design where, for example, the -- you know, where maybe you saw the inductive problem due to bond wires, with other means by having alternate ways of creating power supplies or supplying these power supplies.

There could be many alternatives that a person of ordinary skill in the art would employ to counteract any of the, you know, the conventional wisdom problems that were, you know, that people thought about using these, using these techniques.

So that's not basically part of my study. That's not part of my, you know, that's not part of my -- what I was asked to study in this matter or what I was asked to respond to.

What I was asked to respond to is narrowly what I've described in my patent, which is to review Dr. Foty's declaration, to review the petition, and respond to

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whether the, you know, the grounds that they had with the references they cited, which was Yoshinaga, Saint and Haralabidis, whether those, you know, whether those grounds were, you know -- you know, whether the patent claims were valid or not valid with respect to those grounds.

Now, why the patent -- why the '164 Patent, you know, you know, how it would counteract the problems that you're asking, that's not part of my study and that's not even part of what I'm trying to, you know -- that's not what I'm -- that's not part of the -- of my declaration. That's not something I've studied.

So maybe, you know, if I studied it, I would come up with many more techniques. But this is just what comes to mind at this moment.

Q. Does the '16 Patent disclose or illustrate connecting bond pads via metallization layers?

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A. One more time?

Q. Does the '16 Patent disclose connecting bond pads via metallization layers?

A. I mean, the '164 Patent describes what it does. If you're asking this question whether it uses metallization to connect bond pads, if there's any disclosure in it, then I'd request you to point me to it and I'll give you an opinion.

But that's not basically -- that's not even the inventive feature of it, so I don't see a need for it to do that. The inventive feature is what, you know, what the claims describe.

Q. Why would an engineer use a bond wire to connect bond pads as shown in Figure 3 instead of metallization layer?

MR. WATSON: Objection to form.

A. Again, this is the inventive feature of the patent. That's, you know, a person of ordinary skill in the art before this patent might not have

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considered this. They would have thought it was a bad idea. They would have used all the conventional wisdom, you know, ideas and said that this is something I wouldn't do.

But once they read this patent, they would say that -- they would revisit their, you know, their original opinion and reconsider this and know that this is something that works and that's what is the inventive feature of this patent.

Q. Does the '164 Patent discuss bond wire inductance anywhere?

A. If it does, I'd like you to point out -- point that out to me. Can you sort of show me where it describes that and I'll be happy to give you an opinion on this?

Q. I couldn't find it. That's why I'm asking.

A. I see. Once again, right, like the '164 Patent, you know, describes what it describes in the claims, which are the inventive feature. And the person of

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ordinary skill in the art would realize that when they read these claims that all their previous conventional wisdom ideas about inductance and, you know, the sagging bond wires and so on could be corrected and could be addressed and they might try it out.

And perfect evidence of that would be if someone actually implemented it and used it. That's sort of like, you know, the further evidence of the patent being non-obviousness.

So a lot of this is non-obviousness because it goes against conventional wisdom and that's basically the novelty that's taught in this patent, in this '164 Patent.

Q. How did the '164 Patent solve the problems introduced -- strike that.

How did the '164 Patent solve the noise problems that you mentioned earlier that are introduced by the use of bond wires?

MR. WATSON: Objection to form.

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A. You know, once again, the task that I was asked to do was to look at the validity of the different grounds and the different references that the petitioner and Dr. Foty present, which is Yoshinaga, Saint and Haralabidis.

It was not part of my task to determine how the '164 Patent solved this problem or that problem.

So in some sense the questions you're asking me here are outside the scope of what I've studied for this -- you know, for my -- based on the task I was given to do here.

But as an electrical engineer, we all know that, you know, circuit techniques and manufacturing techniques can improve over the years. And so it's completely not surprising to me that what was considered as, you know, in the conventional wisdom as a bad idea has been solved in multiple ways. And I could come up with some ways to solve it, you know as well as a person of, you know, of

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experience in this space.

But again, that's not part of -- that's not part of my, you know, of my declaration and it's not part of the study that I'm conducting.

Q. Sticking with Figure 3, but switching gears just a little bit, would you agree with me that the areas that are labeled SA1 and SA2 are saved area 1 and saved area 2?

A. So if I look at the patent and I look at the disclosure about the areas labeled SA1 and SA2, it says that -- you know, it calls them saved areas SA1 and SA2, you know, and so that's the names that they've been given, literally called saved areas SA1 and SA2.

Q. And does the addition of saved area 1 and saved area 2 in Figure 3 make the overall chip bigger or smaller?

A. So specifically if I look at the patent specification, it says that, you know, the -- I'll read column 4, lines 20 to like 25.

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It says: For example, the ESD bus 11 and the filler cells F1 and F2 shown in Figure 1 are replaced by saved areas SA1 and SA2 in Figure 2 and thus the circuit area -- sorry -- and thus the circuit area 20 -- I think they're talking about Figure 2 here -- thus the circuit area 20 may contain the circuits with irregular shapes and different areas without increasing its area which saves production cost.

Q. Why does that save production costs?

A. I'm sorry?

Q. Why does adding a saved area, whether it's one saved area or two saved areas, why does adding a saved area save production cost?

MR. WATSON: Objection to form.

A. So if you look at the language that's shown here, it says like -- you know, the circuit area may contain circuits with irregular shapes and different areas. As you can see, there's

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sort of irregular shapes in the circuit area on Figure 3.

So, you know, this doesn't increase the area. You know, the only statement that's made is that the area doesn't increase, which leaves open the possibility that it's decreased.

And of course, if it's decreased, then that would save production cost. Because production cost is more when the circuit area is more -- when the chip area is more. And production cost is less when the chip area is less.

Q. Are you familiar, Dr. Khatri, with what the preamble of a claim is?

A. Yes, I'm familiar with that. It's like the beginning part of the claim.

Q. Did you render an opinion anywhere in your declaration that the claim preambles are limiting?

A. I mean, I've heard the term, but let me see, let me look at the -- you know, this is sort of a legal term, so I'm clearly not an expert in that, but I'm

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going to look at my declaration and just confirm or not if I provide an opinion on that.

So I don't see the word "preamble," nor do I see the word "limiting" in my declaration for the '164 Patent.

Incidentally, I think we've been going again for about an hour and now I'm beginning to get a little more tired. So I think I'd like to request a break and maybe we can come back and continue this.

MR. JENSEN: Yeah, let's go off the record.

THE WITNESS: Okay. Thank you.

(Recess taken from 3:09 p.m. to 3:20 p.m. MT)

BY MR. JENSEN:

Q. Dr. Khatri, I'm going to drop an exhibit into the chat. This is what's been labeled as Exhibit 1037.

Let me know when you're able to download and open a copy of that exhibit.

A. I don't see it yet.

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Q. I think I have to push the button, that's why.

A. Okay, I see something called 1037. Let's see. Just a second. I'm going to move it to my folder of exhibits.

It won't let me do that. So I'm just going to open it. I have it open now.

Q. What's the title of this article?

A. The title says, "Getting to the Bottom of Deep Submicron II: A Global Wiring Paradigm."

Q. And who are the authors of this article?

A. The authors are Dennis Sylvester and Kurt Keutzer.

Q. Do you know either of these two individuals?

A. Yes, I know them both.

Q. And how do you know them?

A. So Dennis Sylvester was doing his Ph.D. at Berkeley, I think along the same time as me. But he was in a different group and with a different research focus.

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And Kurt Keutzer was a professor that joined Berkeley somewhere around halfway during my Ph.D. at Berkeley.

Q. Do you keep in contact with them?

A. Not particularly, no.

Q. Do you know what their reputation is in the field?

A. You know, I don't know. I mean, I wouldn't be able to talk about that for other folks. But, you know, I mean, I know them.

Q. Did you consider this article, Exhibit 1037, when forming your opinions?

A. Let's see. So this was -- as I said in my declaration, in my list of materials considered, it was, you know, in all the materials that -- let me see, let me just get to that section -- so it says, you know in forming -- this is on paragraph 18 of my declaration -- in forming the opinions expressed in this declaration, while drawing on my experience in the field of semiconductor design, I reviewed the petition and all

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the exhibits attached thereto that are cited herein.

So this paper, in particular, is not cited herein, as in it's not cited in my reference.

Q. Okay. You can put that to the side.

A. Okay. You mean the reference 1037?

Q. Yes.

A. Okay.

Q. Dr. Khatri, did you construe any claim terms in your declaration?

A. So again, let me go to the section where, in my declaration where it talks about that. There's a section on page 24, paragraph 39 that talks about claim construction and it says that Dr. Foty asserts that the terms of the '164 Patent's claims have their plain and ordinary meaning. That's kind of what he says, is what I'm saying.

And then I'm saying I have applied such a meaning for the purposes of

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this IPR. And it also says that I reserve the right to propose alternative construction in other proceedings or to amend my opinions if the board provides an alternative claim construction.

Q. So based on that paragraph, did you construe any claim terms?

A. So based on that paragraph, you know, I applied the plain and ordinary meaning, you know, for the purposes of the IPR for claim terms.

Q. Let me direct your attention to the '164 Patent and we'll look at claim 6 as an example. I can share that on the screen, but you're welcome to look at a local copy if you'd like.

A. Let me get to this. Hold on. Just one second. Okay, I think I'm in the '164 Patent at claim 6.

Q. Claim 6 is an independent claim, correct?

A. Yes, it is.

Q. And in the last limitation, the wherein clause at the end, it refers to

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"at least one saved area."

Do you see that?

A. Yes, I see that claim limitation.

Q. Is the term "saved area" a term of art?

A. You know, when a person of ordinary -- I mean, it's a such, for example, if I put myself in the shoes of a person of ordinary skill in the art and if they see the word "saved area," they'd have a notion of the plain and ordinary meaning of the term "saved area."

Q. And what is the understanding a POSITA would have of the plain and ordinary meaning of "saved area"?

MR. WATSON: Objection to form.

A. So when I saw this, like when I putting myself in the shoes of a POSITA, right, saw this, you know, notion of saved area, you know, I had the standard plain and ordinary meaning that I assigned to it, which is literally an area that's saved, sort of -- you know, it's a saved area, right.

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And so in some sense, right, that's basically the plain and ordinary meaning that I applied, which is a saved area is, you know, you know, a saved area, you know. That's kind of the meaning that I applied to the term "saved area."

Q. Had you heard of the term "saved area" prior to reading this patent?

A. I mean, in my work we -- you know, when we're doing chip design, we have some area that, you know, saved area, we call it -- it's not like -- it's a term -- I mean, it's a term, the "saved area" term is a term that has a plain and ordinary meaning. And I would have encountered it, you know, definitely more than once in my career and not thought much about it because it has a plain and ordinary meaning.

Q. And what is the plain and ordinary meaning of "saved area" to a person of skill in the art prior to 2018?

MR. WATSON: Objection to form.

A. So once again, like I said, you

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know, it's such a simple term that, you know, its meaning is the saved area.

Now, I didn't think or I didn't think of a need to express it or to sort of, you know, construe a saved area and kind of provide a definition of saved area in my declaration. I didn't see a need to do that. I didn't sort of put thought into that because I just thought it was, you know, too self-evident a term.

But I did look at Dr. Foty's definition of "saved area" in his declaration and I think it comes -- I think it's in paragraph 160-something.

So under the application of his definition of "saved area," under the application of Dr. Foty's definition of saved area, you know, I concluded that the -- you know, that the claim elements here are not obvious under the definition that, you know, Dr. Foty uses.

And that was basically my, you know, my task was actually to look at the declaration of Dr. Foty and the

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interpretation and opine on that.

So, you know, under any definition of saved area, the plain and ordinary meaning that I have was, and also the definition that Dr. Foty provides, I didn't see that the claim element was met by the citations -- I mean by the references that Dr. Foty and the petitioner present.

Q. So is it your understanding that petitioner and Dr. Foty rendered a claim construction of the term "saved area"?

MR. WATSON: Objection to form.

A. Well, you know, Dr. Foty describes what he thinks of as a saved area and then he -- I guess he uses that definition in, you know, when he talks about these claim elements.

So I used that because I was responding to Dr. Foty's declaration and also the petition. And under that definition, the claim elements are not met by the references that are cited by the petitioner and by Dr. Foty.

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Q. Just to make sure I understand, did you render two opinions in your report, Dr. Khatri, one under your definition of the plain and ordinary meaning of "saved area" and another opinion under the definition that Dr. Foty and petitioner used for "saved area"?

MR. WATSON: Objection to form.

A. No. So what I'm saying is under, you know, either definition, the plain and ordinary meaning definition or Dr. Foty's definition, under either of these the claim elements are the claim elements here are not met by the references that they cite.

Q. Where in your declaration did you give those two separate opinions?

MR. WATSON: Objection to form.

A. You know, once again, right, like the plain and ordinary meaning of "saved area" is something that I didn't explicitly cite because I -- you know, its plain and ordinary -- and my response was a response to Dr. Foty's, you know,

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Dr. Foty's definition of this notion of this term "saved area."

Under the plain and ordinary meaning of "saved area," it was not -- you know, the claim elements or the claims are not met.

Q. Where do you say that in your declaration?

A. Once again, I'm telling you now that basically under the obvious definition, because when you look at the obvious definition, you know, these claim elements were not met. And even under the definition of Dr. Foty's definition of "saved area," these are not met.

Q. Yeah, and my question, because it sounds like you're making a new opinion right now, so I'm just trying to find out if this opinion was in your declaration and I'm affording you an opportunity to show me where in your declaration you rendered an opinion under what you call the plain and ordinary meaning of "saved area" and another opinion under Dr. Foty's

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definition of "saved area."

MR. WATSON: Objection.

Objection to form.

Q. Where is that in your declaration?

MR. WATSON: Objection to form.

A. So like I said, to me the term "saved area" is a plain and ordinary meaning and, you know, I would count a person of ordinary skill in the art would have, again, a plain and ordinary, you know, meaning for that.

And in my career, I've run into this term, you know, when we're doing chip designs and such, the notion of a saved area.

So this is basically the simple obvious notion of what constitutes a "saved area."

I didn't see a need to write it down because it's the plain and ordinary meaning of the word "saved area."

So, you know, the arguments that I make would be unaltered by regard -- you

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know, whether I chose the plain and ordinary meaning of "saved area" as a person of ordinary skill in the art would understand it or whether I chose Dr. Foty's interpretation or Dr. Foty's meaning of the word plain -- you know, of the word "saved area."

So under either interpretation, the plain and ordinary meaning or Dr. Foty's construction of "saved area," the arguments -- you know, the arguments I have to show that these claim elements are not met are unaltered.

Q. You mentioned --

A. Go ahead.

Q. You mentioned a couple of times that you've run into the term "saved area," you know, in the past. When did you come across that term?

A. I mean, you know, like I said, right, like I've done -- you know, I've been in the industry for four years with Motorola. So in that, when we're talking about a chip, we're routinely trying to

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minimize the area of the chip because that minimizes manufacturing cost and that's something that Yoshinaga teaches, that's something that Saint teaches as well, that minimizing the area is something that minimizes -- you know, that's desirable.

So that's something that, you know, in industry when we were at Motorola we were always trying to do that. So we were always trying to save areas. So this term would have come up multiple times during that.

Now, of course, that was 30-something, something like more than 30 years ago, but that term is a common term and it's just a commonplace term that we use when we talk about -- when we talk about chip designs.

And then, once again, when I'm teaching courses, I mean I'm teaching the importance of saving area, so that's something that's again, you know, a first order goal of chip design.

And then when we were doing these

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three chips that I talked about, we're always talking about, you know, saving chip area so that we can basically put in the most -- you know, we can optimize our chips basically.

So this is a term that I've come across all through my career in my industry career, in my academic career, in my teaching career, as well as in my -- in the chips that we made from the group.

Q. Let's come back to claim 6 of the '164 Patent.

Do you recall we had a brief discussion earlier, Dr. Khatri, about what the '164 Patent described as filler cells?

A. Can you please repeat that? I didn't hear you too well.

Q. Yeah.

Do you recall that we had a brief discussion earlier about what the '164 Patent called filler cells?

A. I believe so. I think we read something from the '164 Patent. I think it was -- I don't remember. Let me see.

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I think it was Figure 1 that talks about filler cells and we sort of discussed and read the specification of the '164 Patent where it describes the filler cell, if I'm not mistaken.

Q. Does claim 6 of the '164 Patent require filler cells?

A. I don't know what you mean by "require filler cells," you know.

Q. Let me rephrase then.

Does claim 6 of the '164 Patent say anything about filler cells at all?

A. Let me have a look at that.

So I looked over claim 6 and I don't see the word "filler" or "filler cell" in there.

Q. Do you see the term "filler" or "filler cells" in any of the claims of the '164 Patent?

A. Let me check really quick.

I have a little bit left to read.

Based on my inspection of the claims of the '164 Patent, I don't see the term "filler cell" in any of claims 1

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through 14, both inclusive.

Q. Do the claims of the '164 Patent require the inclusion of power pads?

MR. WATSON: Objection to form.

A. A person of ordinary skill in the art reading claims 1 through 14 and reading -- you know, reading, knowing that this patent talks about an integrated circuit, they would know that, you know, reference pads or power pads are something that would be part of such a circuit. And they would also know that there may be, you know, more than one reference pad of more than -- sorry, more than one reference or more than one supply pad of more than one type each.

So that's something that a person of ordinary skill in the art would just know because they were a person of ordinary skill in the art.

And, you know, and the patent itself -- I should verify if the patent says anything about power or supply, so I'm going to go look through the claims --

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I'm talking about the claims -- I'm going to look through the claims really quick and make sure whether that's the case or not. Just give me one second.

So I've gone through the claims 1 through 14 both inclusive of the '164 Patent and I don't see the word "power" or "supply" in that.

Now, of course, a person of ordinary skill in the art -- again, I'll put myself in the shoes of that person -- a person of ordinary skill in the art sees the reference of, you know, to pad groups and they also understand that the fact that the patent doesn't talk about power or supply, doesn't preclude the patent -- I mean, doesn't preclude there being, you know, power pads or supply pads.

And so in some sense they also know that, you know, the fact that the claims don't say anything about power or supply pads doesn't -- you know, allows power and supply pads to exist and the patent claims would still be met.

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Q. Do you know what claim limitation was the reason that the '164 Patent was allowed?

MR. WATSON: Objection to form.

A. I don't understand your question.

Q. Let me maybe try it again and come at it a different way.

Are you familiar with the term "file history"?

A. Yes, I am.

Q. What is the file history of a patent?

A. So the file history of a patent is the sequence of back and forth communication between the inventor and whoever, you know, drafts the patent for the inventor, and the Patent Board, the U.S. Patent Office. So something like, you know, they'd send a communication and there would be a response saying, you know, the opinion of the U.S. Patent Office.

And then, I mean, again, I'm not a lawyer so I don't know the fine details

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of the rules and how all this works and the timelines and such, but there's some opportunity for the inventor to respond and then there's sort of these back and forths that are -- that occur in the process of -- which can result in the end of where the inventor says, forget it, I'm giving up on this patent, or it can result in the U.S. Patent Office saying, yes, we -- I don't know, issue or award or whatever -- I don't really know the words -- but that's the kind of the communication that goes back and forth between the patent -- the inventor and the Patent Office, the U.S. Patent Office.

Q. That's a fair summary.

As you noted, sometimes a patent is, whether they use the term allowed or issued or granted, and like you said sometimes the ultimate result is a patent does not issue, right? Those are sort of the two outcomes.

A. There may be more outcomes, but I'm just not a lawyer. I don't know these

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details, so...

Q. So I want to focus on the scenario where a patent is grant order awarded.

Before that happens, the patent examiner will send a communication to the inventor or his lawyers or her lawyers explaining why they are allowing the patent, and that's what's referred to as the reasons for allowance. It's the stated reasons the patent examiner says why they're allowing the patent.

And so my question was, kind of with that background or understanding of what, you know, a reason for allowance is, do you know in this case why the examiner stated that he allowed the '164 Patent to issue?

MR. WATSON: Objection to form.

A. So, you know, once again, right, I think, you know, I'm not a lawyer. So if I look at the legal words that the Patent Office presents and saying this is, as you're suggesting, this is why we

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allowed it, I don't even know if that would be meaningful to me because it's basically the legal back and forth, you know, that's going on between the U.S. Patent Office and the inventor.

So whenever something like this is at issue, I reach out to, you know, counsel and say explain this to me because I'm not -- I'm not an attorney and I don't understand that.

So I have no idea or opinion about what this "allowance" -- I think you said -- reason would be or was. You know, that's just something that is outside the realm of my expertise because I'm not a lawyer.

Q. Did you review the file history in this case?

A. I might have eyeballed it, but I don't think it was something that was brought up. So, you know, it's not part of my declaration.

Q. Okay. Let's switch to another exhibit here and let's go to Exhibit 1006.

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A. Okay. So let's see, is there things that I can delete, although it's easy to open again, but are there things I can delete? I'll keep my petition open.

Q. I think you can close everything except your declaration.

A. I'll keep that, okay. And I also have a hard copy.

So 1006, okay, I see it. I've opened 1006. It seems to be Yoshinaga.

Q. Yeah, this is the Yoshinaga reference, correct?

A. Yes, it is.

Q. Okay. And let's maybe focus on Figure 6 of Yoshinaga. Are you familiar with that figure?

A. Yes, I've seen Figure 6 of Yoshinaga.

Q. And there's a number of squares on the periphery, the four sides of the chip 74.

Do you see those kind of squares around the outside of the chip in Yoshinaga Figure 6?

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MR. WATSON: Objection to form.

A. Just to be unambiguous, I think, you know, I think you're referring to the, you know, squares, small squares that appear in the top row and the bottom row and in the right column and the left column.

And, for example, if I'm, just to be sure we're talking about the same squares, the squares on the top row are broken up into two groups and the rightmost square of the first group is labeled 3. And the second square from the left of the second group of the right group on the top row is labeled 4. And that's the top row of squares where there's 10 of them. There's 10 rows -- 10 squares again in two rows on the right column.

And I think 11 squares on the left column in one contiguous section. And in the bottom row there is again 11 squares in one contiguous. So are these the squares you're talking about?

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Q. Those are the ones.

A. Okay.

Q. What are those squares?

A. So, you know, these are the squares that, you know, are the different pads that Yoshinaga talks about.

And the reason I can say that, one reason I can say that is in paragraph 88, which I cited to before, paragraph 88 of Yoshinaga, it says that, you know, objects labeled 3, 4 and 58 are power supply pads.

So these are pads. And when I look at Figure 6, I see, you know, four different pads which have labels 3 on them. And, you know, looking at paragraph 88, I can see that label 3 corresponds to power supply pads. So I know that these are four instances of power supply pads, which are labeled three. And similarly, there are three differences of power supply pads that are labeled 4 on the top right side of this figure.

And finally, the three power

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supply pads labeled 58 on sort of the southeast corner of the figure or the bottom right part of the figure.

Q. Are the pads that you just described in Yoshinaga Figure 6 bond pads?

A. Yeah, well, these are the pads that would be used to connect the chip. And so, you know, because they're peripheral pads, you know, they'd also be, you know, they would be these bond pads.

Q. Let's look at paragraph 41 of your declaration.

A. Okay. Oh, you said page 41?

Q. I may have. If I did, I meant paragraph 41.

A. Sorry, let me go to paragraph 41. Okay, I'm there.

Q. Actually, let's back up one paragraph, kind of to the beginning of this section, so paragraph 40.

In this paragraph, you're discussing Yoshinaga Figure 6, correct?

A. You're talking about paragraph 40, yes?

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Q. Yes.

A. Yeah. So in paragraph 40, I'm responding to ground 1 and specifically to this ground 1 of the petition that, you know, uses Yoshinaga, Saint and the knowledge of the POSITA.

And I'm saying that that combination, the Yoshinaga, Saint and knowledge of the POSITA doesn't render of course the "a plurality of pad groups adjacent to and connected to a plurality of ESD buses" -- that's for claims 6 and 7, and also "wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses for claims 12 and 14."

So that's what I'm responding to in general in this whole section.

And in paragraph 40, in particular, I'm talking about the changes that Dr. Foty and the petitioner make to, you know, to basically manipulate Figure 6 -- there is no Figure 6 of Yoshinaga.

Q. And the first sentence in

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paragraph 40 says: Petitioner and Dr. Foty modify Yoshinaga Figure 6 by replacing a supply pad 3, an unlabeled pad, a supply pad 4 and a supply pad 58 with a reference potential pad 5, 6, 6 and circuit 67 ground respectively.

Do you see that sentence?

A. Yes, I do see it.

Q. Can you explain to me what you mean when you say replacing a supply pad, you know, unlabeled pad, supply pad, et cetera?

A. Okay. So, you know, to answer that, I'm going to -- let me go to my version of -- my soft copy version of my declaration so I can zoom in a little bit.

You know, let's look at these two figures that are shown here. The figure on the left is the original figure in Yoshinaga.

The figure on the right is the manipulated figure that Dr. Foty and the petitioner, you know, manipulate, okay.

So if you look at the top row of

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pads, you know, the top row of pads in the original figure has two groups. There's a left group, in which the right most pad is labeled 3. And there is a right group of topmost pads in which the leftmost pad is unlabeled, has no label.

So now if I look at the top row of pads in the manipulated design of Dr. Foty and the petitioner, you can see that the -- that again there are, you know, there's one top row of pads, which is in two groups, there's a left group and a right group.

But if you look at the left group and you look at the rightmost pad of it, it is now a pad 5, it's now labeled 5.

And if you look at the right group of pads and you look at the leftmost pad of it, it has a label 6.

So a person of ordinary skill in the art looking at this is saying, well, in the original design there used to be pad labeled 3 in the rightmost group of the left -- in the rightmost pad of the

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left group of pads in the top row and that is now in the manipulated design, the rightmost pad of the left group is a group 35.

So in chip design, when we see something like this, a person of ordinary skill in the art says, well, that used to be a pad 3, which is a supply pad, it's now pad 5, which paragraph 88 of Yoshinaga says is a reference pad.

So a person of ordinary skill in the art readily and easily makes the conclusion that pad 3, which was a supply pad on the left -- on the rightmost part of the left row of the top row of pads, has been replaced by a reference pad 5 in the same location, that is in the topmost -- in the left -- in the rightmost pad of left group of the topmost row of the design.

So this is literally a replacement. If I was doing a chip design, if I was actually doing a chip design here, I -- when I'm making a change

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like this, I literally need to take out one pad and replace it by another pad.

So the word "replacement" to a person who has designed a chip is completely appropriate in this situation.

In other words, pad 3 has been replaced by pad 5 in the top row.

Similarly, if you look at the right group of pad, the right group of pads in the top row, the leftmost pad has no label in the original design. And that's been replaced by a pad with a label 6.

So if you read my sentence, it says, you know, petitioner and Foty, Dr. Foty, modify Figure 6 by replacing a supply pad, an unlabeled pad -- that's referring to the two pads I just talked about -- and they have been respectively replaced by reference potential pads 5 and 6, as we just saw. That's on the top row.

And then the last two pads that are listed in my sentence in paragraph 40 talk about a supply pad 4 and a supply pad

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58.

And supply pad 4 is the bottom pad of the top group on the right-hand side row of pads. And the pad 58 is the top pad in the bottom group in the right-hand column of, you know, of the original design.

So those pads labeled 4 and 58, these are on the right side of the original figure, in the manipulated figure they have been replaced by pads labeled 6 and circuit 67 ground.

And, of course, the reference -- sorry, the paragraphs 88 of Yoshinaga teaches that 6 is a reference pad. And circuit 67 ground is just a made-up name that the petitioner and Dr. Foty have, but that's basically, you know -- that's something that they claim is a ground pad.

So these are the replacements that are done, you know, in Dr. Foty and petitioner's design.

But in addition, there's one more replacement, which I talk about later, is

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that pad 4 in the top row, in the top -- the right side of the top row, the second pad from the left is called pad 4, and this pad has no label in the manipulated design. So in some sense, that's another replacement that has been done.

So there's just been a large amount of pads that are just sort of like replaced by other pads in this picture.

A person of ordinary skill in the art knowing chip design would know that the only way you do it is by replacing one type of pad by another type of pad to accomplish this manipulation.

Q. So let me ask one follow-up question on something you just mentioned, and I'll just read the sentence in paragraph 40 of your declaration that says: "They also remove a supply pad 4 (shown in the top right circuit block)."

Do you see that?

A. Correct.

Q. Is it your understanding that petitioner was proposing to physically

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remove a pad from Yoshinaga Figure 6?

A. The petitioner and Dr. Foty talk about the manipulated design, they talk about the original design. And when a person of ordinary skill in the art looks at these two, they can make no other conclusion then to say that there was a replacement of one pad type with another as I've stated in paragraph 40.

And also, you know, like with the highlighted line that you have, which is, just for the record, it's the second line on page 25 of my declaration and it reads: "They also remove a supply pad 4 (shown on the top right circuit block)."

So that's referring to the pad number 4 in the right side group of pads on the top row. That's second pad from the left.

You can see that that pad on the manipulated figure has no label, that corresponding pad. In other words, supply pad 4 has been removed and has been replaced by a -- you know, by a pad that's

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not a supply pad and is definitely, you know, not labeled. So, you know, it's not a ground pad. And therefore, it is basically an I/O pad.

In other words, at the bottom of it, it has been replaced by something else.

So there are -- you know, there's a large number of pads in this situation that are described in paragraph 40 in my declaration that have been replaced by something else.

Q. And that's what I want to tease out is kind of the distinction between this concept of replacement and removal and I'll just throw in the idea of adding pads.

Would you agree with me that looking at the left image, so that's the unmodified Yoshinaga Figure 6 and the right image which is the modified version of Yoshinaga Figure 6, that in both images there are the same number of bond pads?

A. I can see that the number of bond

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pads, you know, in the two images on page 25 of my declaration, which basically comes from Exhibit 1003, the number of total pads has not changed.

Q. Okay. All right. That's what I was trying to --

A. So essentially what has happened is, you know, they've basically removed pads. And as I say in the remainder of this section, they have said nothing about where the pads that got removed have been moved to. So there's no discussion about that. There's no discussion about an analysis about, you know, how hard that process would be or whether the removal of these pads would cause a, you know, circuit electrical sort of characteristics to worsen.

And I cite to why it would worsen because there's a 40% reduction in the power supply pads, which would basically cause the circuit to slow down and possibly fail. And I cite to Dubey for that.

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So there are multiple reasons why when you just do this replacement and don't talk about where these pads went, it can cause serious problems with the chip.

And even doing the replacement, just doing the replacement needs careful analysis, which was not conducted by Dr. Foty or the petition.

Q. How many I/O pads in your opinion, Dr. Khatri, are shown in the unmodified version of Yoshinaga Figure 6?

MR. WATSON: Objection to form.

A. Okay. So again, this is -- you know, this is described in my declaration, but let me tell you the methodology I would find. I don't know the number off the bat, but we can calculate it.

Q. Just count it. That's all my question is. Just what is the number.

A. I'll give you a methodology, just so you know, in case I give a wrong number then it's on the record as to how I computed this.

So in the Yoshinaga disclosure,

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there are 11 pads on the left side, 10 pads on the right side, that makes 21. 11 pads on the bottom and 10 pads on the top, so that's 42 pads in all.

Now, Yoshinaga, you know, explicitly labels the supply pads which are in paragraph 88 Yoshinaga says have labels 3, 4 and 58.

So I'm going to count all the pads that are labeled either 3 or 4 or 58. That total is -- there are four 3 pads labeled 3 on the left side of the chip, three pads labeled 4 on the right side of the chip, that makes 7 in all, and 3 pads labeled 58 on the bottom right of the chip, so that makes 10 supply pads.

So I subtract from my original count, which was 42, I subtract, then I get 32 unlabeled pads in Yoshinaga.

And Yoshinaga explicitly says, and this is in paragraph 78, that reference pads are not shown. In other words, none of these pads that we see in Figure 6 have a label of a reference pad.

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So therefore, all the 32 pads that I just described are necessarily either input or output or I/O.

And in my declaration, I call them as I/O, like upper case I, upper case O, I just gave them a short name, I suppose.

So there are a total of 32 I/O pads in Yoshinaga.

THE WITNESS: Incidentally, I think we've been going for about an hour if I'm not mistaken so, I'd like to request a break if this is a good time for you to take a break.

MR. JENSEN: We can take a break. I always try to accommodate the witness.

THE WITNESS: Thank you so much. I appreciate that. How about 10 minutes?

MR. JENSEN: Okay.

THE WITNESS: Thank you.

(Recess taken from 4:10 p.m. to 4:20 p.m. MT)

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BY MR. JENSEN:

Q. So before the break, Dr. Khatri, we were looking at Yoshinaga Figure 6 and the modified version of Figure 6 that are reproduced in paragraph 40 of your declaration.

A. Yes.

Q. Is it your opinion that in the unmodified version of Yoshinaga Figure 6, that none of the pads that are shown can be used as ground pads?

A. May I ask you to repeat that question?

MR. JENSEN: Could the court reporter read that back?

THE COURT REPORTER: Sure.

(The requested portion was read back by the Court Reporter.)

A. In response to this, right, it's not a matter of my opinion. It's a matter of what Yoshinaga explicitly states. So let me point you to paragraph, I think it's 78 of Yoshinaga. Let me just go there real quick.

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If you look at paragraph 78 of Yoshinaga, there is an explicit statement, the first line there says: Reference potential pads are not shown.

So when a person of ordinary skill in the art looks at this Figure 6, they know that Yoshinaga is saying that reference potential pads are not shown.

So they know that whatever is shown is anything other than reference potential pads. That's kind of a clear conclusion that a person of ordinary skill in the art makes when they read the first line of paragraph 78 of Yoshinaga.

Q. Is it -- well, let me ask this: Would you agree with me that a person of ordinary skill in the art would understand that in a physical embodiment of the chip shown in Figure 6 that there would be ground pads present?

A. A person of ordinary skill in the art would know that the physical embodiment of the chip shown in -- I mean, of the chip shown in Figure 6 must have

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ground pads.

So they would know. And I sort of describe that in some detail in my declaration. And this is, I think, on page something like 68, as a discussion of where the possible ground pads might be located based on a person of ordinary skill in the art, analyzing the pad arrangement and labels of Figure 6 in the original Yoshinaga and comparing -- and using the statement in the first line of paragraph 78 of Yoshinaga.

Q. Is it your understanding that petitioner's proposal was to have fewer overall power pads in the modified version of Yoshinaga Figure 6?

A. Can you repeat that, please?

Q. Yeah.

Is it your understanding that petitioner's proposal was to have fewer overall power pads in the modified version of Yoshinaga Figure 6?

A. Okay. So I can't put myself in the petitioner's head and ascribe intent

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to what they did, but I can only look at what -- you know, of the petition that they presented and Dr. Foty's declaration.

And in the petition and Dr. Foty's declaration, I see that there is a reduction in the number of power pads and I see no discussion about where they might be moved to. I see no analysis about -- you know, in fact, I see a very haphazard -- I mean, I see a very casual sort of treatment of pads calling pad placements as fungible in some sense, right. That's literally that word that was used. And it's just not fungible.

So there is -- you know, the changing of pads from the original to the manipulated design in which I sort of excerpt, which I sort of show in page 25 of my declaration, which comes from paragraph 153 of Exhibit 1003, that's done in a very casual manner.

There is no discussion about -- you know, a thorough analysis there would have said here's the reason why a person

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of ordinary skill in the art would have made this change, here are the electrical impacts they would have considered, here are the functional impacts they would have considered, here are the terminal impacts they would have considered, here are the inductive and resistant impacts they would have considered.

And where these replaced pads go, there would have been an analysis of that if this was more than -- if this was a thorough analysis. There's absolutely no discussion like that.

Now, I don't know what their intent was. But certainly what the petitioner's document, the petition document and Dr. Foty's declaration do not describe any of these things that I've said.

And, in fact, you know, it just sounds like, you know, the discussion -- and I've said this somewhere in my declaration -- this manipulation just sounds like a hindsight-driven exercise

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because, you know, in some sense everything is done to just match the claims, you know, of the '164 Patent, right.

Without that hindsight, you know, I mean, I don't see why any of these massive modifications that they are making, why that -- why those are needed. But the only explanation for that, that I could come up with, is hindsight. And, of course, that's sort of my -- that's an opinion that I form.

But the facts on the ground are that there's no analysis that's done as to why this manipulation is electrically a good decision and where these pads would go, you know, what are the impacts. And all of that is described in my petition in the paragraphs corresponding to ground 1A, which is basically paragraphs 40 through -- it's quite a few paragraphs, maybe something like 60, but let me just -- paragraphs 40 to 63, tell you, I mean, describe all the technical reasons

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why this exercise of, this manipulation exercise is something a POSITA would simply never do.

Q. Did you render --

A. So paragraphs 40 to 71, yeah.

Q. Did you render an opinion in your declaration under the scenario where the number of power pads is the same in the unmodified and modified versions of Yoshinaga Figure 6?

MR. WATSON: Objection to form.

A. My response -- my declaration is responsive to what, you know, what is written in the petition and what is written in Dr. Foty's declaration.

So it's not my task to actually, you know, come up with a situation where the petitioner or Dr. Foty would have made an alternative modification. I could not come up with a space of modifications that they could conjure up.

So I could not come up with a modification like you're saying in which the petitioner does -- you know, keeps

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some number of pads different or same. It's up to the petitioner to teach me that and it's up to me to opine on that rather than me coming up with arguments for the petitioner.

If I did what you're saying, I'm coming up with arguments for the petitioner, which is just not my task in this exercise.

Q. So just to be clear, you did not, Dr. Khatri, analyze a scenario where the number of power pads remains the same in the unmodified and modified versions of Figure 6?

MR. WATSON: Objection to form.

A. You know, yeah, if that was an argument that was made, if there was a discussion that petitioner and Dr. Foty, you know, had precisely showing this is exactly how we're going to make our modification, this is exactly how we keep, you know, whatever you're saying, the number of power pads the same, then I would have opined on it.

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But absent them mentioning this, you know, I don't see a need for me to opine on it.

It's in some sense like me -- the argument is almost saying did you opine on every possible argument they could have hypothetically made. And I mean I have no idea sort of coming up with all the hypothetical arguments that petitioner and Dr. Foty could have potentially made but did not make in their petition.

Q. And I just -- that was a long answer, tough to follow. I'm just trying to understand if you did or did not render an opinion under that scenario where the number of power pads is the same.

Back up. We clearly have a disagreement on what was disclosed in the petition, and I just want to know if you did render an opinion under that scenario where the number of power pads remains constant.

MR. WATSON: Objection.

Objection to form.

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A. So I responded to the petition in Dr. Foty's declaration. And if they had in there a precise argument about how they would have, you know, gone about a certain manipulation, I would respond to that.

But absent such -- absent such a detailed description or a detailed explanation of how, you know, how that manipulation, you know, how the manipulation works in detail, you know, I have no way of coming up with their arguments and then responding to those, you know, to their -- you know, coming up with their arguments from them and responding to exactly those hypothetical arguments. There's no way to do that.

Q. So you didn't address that scenario?

MR. WATSON: Objection. Asked and answered.

A. You know, my petition responds to whatever is argued or presented in the declaration of Dr. Foty and the petition.

You know, my declaration is

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responsive to those two items and what is contained in them.

Q. And in your view, you didn't address the constant number of power pads scenario because you believe it was not present in the petition and Dr. Foty's declaration?

MR. WATSON: Objection to form.

A. So like I just said, I have -- you know, from paragraph, I think it was 40 to 71, you know, which is responding to exactly this issue that you're talking about, which is the manipulation that they're talking about, there are multiple reasons I present why the manipulations presented in the petition and Dr. Foty's declaration, you know, are technically unsound. And they're all presented in my declaration from paragraphs 40 through 71.

Q. Can you point me in those paragraphs, Dr. Khatri, to anywhere where you address the scenario where the number of power pads remains constant?

A. Even if there's no spot where the

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number of power pads remain constant -- because if that's the case, they should have had, Dr. Foty in his declaration should have had a description of where these new power pads move, what exactly these locations are for -- and there are three kinds of power pads, so they should be new pads labeled 3 and -- let me see -- they should be new pads described in some figure of the petition or Dr. Foty's declaration that are labeled 3 or 4 or 58. Because these, pads of this type have been removed in the manipulation.

I see no -- I see no figure in Dr. Foty's declaration or in the petition where new pads labeled 3 and 4 and 58 are added which replace these pads.

And even if they did, as I said, you know, the treatment of manipulation of pads in the petition and Dr. Foty's declaration is, they're treated as if they're fungible.

And I've given multiple arguments in paragraphs 40 to 71 where moving of

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pads is absolutely not a fungible exercise.

And so there is basically no -- you know, there's basically this whole power pad movement issue or manipulation issue is treated very casually without any details of the repercussions of the manipulation, you know, how it impacts terminal issues, electrical issues, delay issues, possible failure of the whole chip, possible reanalysis that you have to do and movement of blocks to adjust for the manipulation of supply and power pads.

So there's just a lot that's simply not addressed, that's not even contemplated or not even brought up. And that I'm describing in paragraphs 40 to 71 in my declaration.

In exercise of manipulation is, it just seems to be a pure hindsight-driven exercise.

Q. What is the underlying circuit that is being implemented in Yoshinaga Figure 6?

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MR. WATSON: Objection to form.

A. I mean, in Yoshinaga Figure 6 there are sort of three designs that are discussed. They're called -- let me sort of -- let me search in Yoshinaga and point you to that.

Let me look through this. Just give me a minute, please.

Q. And maybe I can clarify my question, Dr. Khatri.

You know, we talked earlier about your Texas A&M design chips and you said one of them was a subthreshold BFSK transmitter, another one was a multichannel analyzer and another one was an alpha detector.

Does Yoshinaga identify, you know, what type of circuit it's implementing in Figure 6?

A. Yeah, so I'm trying to answer that. I see your question and I'm trying to answer that.

You know, so far something that I found was that it's talking about, you

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know, CMOS circuits. That's shown in paragraph 2.

It says in particular in a CMOS circuit, you know, that the film element would have a certain voltage and so on. So it's talking about it being responsive to CMOS circuits.

Also paragraph 3, you know, talks about, you know, that there may be some analog circuits which needs separate power supplies. So it's contemplating a chip in which you have multiple circuits inside, some of which could be analog and require separate power supplies, and you can see those different power supplies in Figure 6 because there's power supplies 3, 4 and 58.

Let's see. And it does talk about multiple circuits where, I sort of remember that, but I'm trying to find you that.

So if you look at the abstract, it talks about improving ESD resistance in a semiconductor integrate circuit, having

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a plurality of circuits inside it. So this would have -- you know, the integrated circuit has multiple circuits inside it.

And Figure 6 discloses, you know, a plurality of such circuits because it discloses circuit 1, circuit 2 and circuit 67. So the context of Yoshinaga is where you have multiple circuits inside an integrated circuit as Figure 6 clearly shows. And some of these can be analog.

So it's a very broad context. It's not saying that the circuit should be of this type or that type. It's kind of, you know, a pretty broad type of circuit -- types of circuits that it contemplates.

Q. Does Yoshinaga disclose what function any of the circuits 1, 2 and 67 perform?

A. So a person of ordinary skill in the art when they look at Yoshinaga, they will understand that these circuits can be flexible, that Yoshinaga's teaching is not

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about the type of circuits in circuit 1, 2 and 67, but, in fact, it's about how you might do, you know, ESD improvement in an integrated circuit where you have multiple circuits.

That's basically the teaching. The teaching is not focused on a specific circuit. And a person of ordinary skill in the art would readily understand that.

Q. Let me take you back to Yoshinaga Figure 6 and I'll share my screen, but you're welcome to look at whatever copy you would like.

In Yoshinaga Figure 6, do you see the buses labeled 19, 20 and 60?

A. Yes, I do see that.

Q. And what does Yoshinaga paragraph 88 say those buses are?

A. Let's see. Yoshinaga paragraph 88 shows that the labels 19, 20, 41 and 60 are reference potential lines. You know, so, in particular 19, 20 and 60 are reference potential lines.

Q. Are those reference potential

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lines 19, 20 and 60 implemented using an on-chip metallization layer?

A. So, you know, this is something that Dr. Foty also admitted in his deposition, I believe. But, you know, again, a person of ordinary skill in the art looking at the disclosure of Yoshinaga, you know, looking at the disclosure talking about right in the abstract, you know, a semiconductor integrated circuit, right, they would understand that all the features shown in Yoshinaga pertain to a single semiconductor integrated circuit, which means all the features and all the wire connections use on-chip metallization for the wiring.

This in the opinion of the person of ordinary skill in the art would be reinforced by the fact that there's no discussion of bond wires and such, and that would make sense that the person of ordinary skill in the art because there's no, you know, non-wires or packaging

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described here. The focus is all about the semiconductor integrate circuit as is shown in the abstract.

Q. Yes, I don't think that answered my question at all.

MR. JENSEN: Could the court reporter read the question back, please?

(The requested portion was read back by the Court Reporter.)

A. And my answer was that a person of ordinary skill in the art reading the disclosure of Yoshinaga would understand that, you know, all the metallization in Yoshinaga uses the on-chip metallization, particularly because Yoshinaga in the abstract itself says that the -- you know, that the problem they're solving pertains to semiconductor integrated circuits which have a plurality of circuits inside them.

Q. Yeah, I still don't understand that answer.

Would you agree with me that a person of ordinary skill in the art would

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understand that the reference potential lines 19, 20 and 60 shown in Yoshinaga Figure 6 are implemented using a metallization layer?

A. So, you know, what I just said is that, you know -- I sort of gave you the reason why a person of ordinary skill in the art would conclude that all wiring shown in Yoshinaga uses on-chip metallization, you know, which is something that Dr. Foty agreed with as well.

Q. Yeah, and I guess let me -- I'm specifically referring to what's illustrated and shown in Figure 6.

So with respect to Figure 6, in particular, would you agree that a person of ordinary skill in the art would understand that reference potential lines 19, 20 and 60 are implemented using a metallization layer?

A. So, you know, my response is that a person of ordinary skill in the art would understand that all wiring in

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Yoshinaga uses metallization, you know, on-chip metallization.

And Figure 6 is part of Yoshinaga. So they would understand that Figure 6 also uses, you know, on-chip metallization.

And I also gave you the reasons for that, which I gave you -- I repeat in two answers before this one.

And further, I'll respond saying that, you know, anybody who has done a chip, when they see features like, this features like 19, 20 and 60, they know these are on-chip metallization features because that's how commonly we implement, you know, implement reference potential lines and supply lines on-chip using on-chip metallization.

Q. Would you agree with me that Yoshinaga Figure 6 does not show an electrical connection between reference lines 19, 20 and 60?

A. Again, you know, Yoshinaga's Figure 19 is not showing every metal shape

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that there might be, I think I mentioned earlier if this was an actual layout, you would see maybe millions, maybe billions of rectangles and, you know, electrical shapes.

The number of shapes you're seeing here are maybe in the hundreds, you know, something like in the hundreds.

So there's a lot of detail that in this figure, Figure 6 of Yoshinaga, is omitted. And that, a person of ordinary skill in the art would readily understand that in a real chip there would be way more features in it than what are shown here.

In fact, a person of ordinary skill in the art -- and this was, I think, observed by Dr. Foty -- would also realize that, you know, that like pad 3 and 4 and so on are actually touching these shapes 20 and 60 and 19, which in reality if they were touching that would be a short-circuit because, you know, pads 3, 4 and 58 are power supply pads. And

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reference potential lines 19, 20 and 58 are ground. So if they were touching, that would be a short-circuit.

So seeing this, a person of ordinary skill in the art would know that there are missing features. There are missing details in Figure 6 of Yoshinaga.

So just by looking at, you know, lines 19 and 20, they wouldn't readily make any conclusion about whether they're connected or not. Because, in fact, other figures in Yoshinaga show that 19 and 20, for example, are connected.

So a person of ordinary skill in the art would look at Figure 6 and say, well, that detail is just missing in Figure 6.

Q. And that's the point I wanted to get at, there are other figures, like Figure 1, Figure 2, et cetera, in Yoshinaga that show that, in fact, the reference potential lines, you know, 19 and 20 are in fact connected to one another, correct?

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A. Well, yes, it's sort of more intricate than that in a sense because, you know, Figures 1, 2 and 4 show that -- 1, 2 and 4 show that 19 and 20 are connected. But Figure 3 shows that 19 and 20 are not connected. So in some sense, you know, Figure 6 is trying to accommodate all of that and that's basically why, you know, certain details of Figure 6, you know, would not be shown in Figure 6.

And a person of ordinary skill in the art reading Figures 1, 2, 3 and 4 and looking at -- I'm sorry, looking at Figures 1, 2, 3, 4 and 6 would make this observation, would make the observation. Yoshinaga clearly says the reference potential pads are not shown.

So a person of ordinary skill in the art knows that there are certain details or certain shapes that are missing from Figure 6.

Q. Do you know -- so I'm showing Yoshinaga Figures 1 through 4.

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Do you see those figures?

A. Yes, I do.

Q. Do you know which of those figures is being implemented in Yoshinaga Figure 6?

A. So, you know, to answer that I would look at the brief description of drawings, which is in paragraphs 87 of Yoshinaga. So I'll sort of go over that with you, right.

So it says Figure 1 is a block diagram showing the configuration of a semiconductor integrated circuit according to an embodiment of the invention.

Figure 2, it says -- again, the same thing I think -- it says a block diagram showing -- sorry, it says other configurations of semiconductor integrated circuits according to an embodiment.

Figure 3 says a block diagram showing a specific example of the semiconductor integrated circuit of Figure 1.

And then Figure 4 says a block

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diagram showing the configuration of a circuit for performing a simulation to conform -- to confirm the effect of the present embodiment.

Now, when I look at Figure 6 in this description, it says a schematic diagram of an integrated circuit chip, including the semiconductor integrated circuit of Figure 1.

So when I put all this together, I see that Figure 6 is a schematic representation, so physical representation of an integrated circuit chip, which we can clearly see it's physical, it has I/O pads -- you know, it has pads, so on and so on. And it says it includes the semiconductor integrated circuit of Figure 1.

In other words, a person of ordinary skill in the art reading this line knows that Figure 1 resides in Figure 6. And if Figure 1 has a connection between 19 and 20, the reference potential lines, then Figure 6 must have them, but

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it's just not visually shown because Figure 6 does omit some features such as the reference potential pads as was taught in paragraph 78.

Now, it also says that Figure 3 is a block diagram showing a specific example of a semiconductor integrated circuit of Figure 1.

In other words, Figure 3 is also something that resides inside Figure 6.

Q. Okay. Thank you.

Is there anything in Yoshinaga that expressly says that the connection between reference potential lines 19 and 20 is implemented via a metallization layer or are you relying on the knowledge and understanding of a POSITA for that opinion?

A. Okay. So in response to that, I'll say two things.

First of all, you know, the POSITA would clearly understand that all wiring that's shown in Yoshinaga is implemented using on-chip metallization

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because, you know, because Yoshinaga repeatedly says that it's teaching a semiconductor integrated circuit. So that's the first response to that.

The second response is that, you know, Dr. Foty himself said that, you know, metallization in Yoshinaga would be, you know, would be using on-chip -- I mean, wires in Yoshinaga would be using on-chip metallization.

So Dr. Foty also agrees with the POSITA's analysis. And I think that the POSITA would readily make such a conclusion.

Q. Let me direct your attention to paragraph 145 of your declaration.

A. Let me see. I see that.

Q. And paragraph 145 includes a picture of a chip, is that right?

A. Below paragraph 145, I do see an image of a chip, which is from paragraph 379 of Exhibit 1003.

Q. Do you know what chip that is?

A. It's a chip that -- let me see

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if -- I mean, it's just a chip that Dr. Foty includes in his declaration. You know, he just says that, you know -- I mean, it's quoted -- I mean, it's cited as an exemplary 2010 microphotograph of a product IC. It's just a generic, you know, chip which is "product IC" based on Dr. Foty's, you know, based on Dr. Foty's paragraph.

Q. Do you know what manufacturing technology node was used to fabricate the chip shown in paragraph 145?

A. I'm sorry. I can see Dr. Foty's declaration and see if he's got any detail on that. Give me one second. I'll just have a quick look.

This is paragraph 79, correct. Okay, I'm just going to read out paragraph 79. It says for completeness, it should be noted that the use of space between pad groups for circuitry is broadly known. For example, the 2010 article -- and it cites to a Spark Fund article, okay -- mentioned earlier contains a figure -- one

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that was not shown earlier, that's a microphotograph of an IC that has been toned down to show its -- you know, as can be seen by simple inspection, the circuit deployed spaces, et cetera.

So Dr. Foty doesn't describe the details of what this chip was.

In some sense, I don't really see a connection between including this chip and the previous arguments that he was making. But it's just a chip that he's included in his declaration.

And it comes from sparkfund.com. Sparkfund.com is a hobby electronics sort of sales website, you know, which basically talks about which cells, you know, simple hobby electronics that, you know, that in fact before my nephew went to college he used to get chips from Sparkfund to do little projects and stuff.

So it's basically a little article from the hobby -- you know, from the young people hobby website called Sparkfund.

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So there are no further details about what this chip is and anymore details that Dr. Foty has disclosed.

Q. Does the image in paragraph 145 of your declaration show any bond pads?

A. Sorry, let me go back to that. Oh, you said page 145?

Q. Paragraph 145.

A. Sorry, yeah, paragraph 145.

So the image on paragraph 145, can you please repeat your question?

Q. Yeah, does it show bond pads?

A. Let me see that carefully.

So if you look at this image, right, like at the peripheries, you see these dark lines that are coming in, you know. And they're almost like they're -- they're -- you know, the ones near the top of sort of vertical and the ones at the edges are more angular. I think -- am I being clear as to what lines I'm referring to?

Q. Yes.

A. The dark line on the periphery of

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the chip.

Now, these dark lines all end in one spot, which is sort of like a black dot. And below the black dot you see, you see the end of the black dot that's sitting on sort of a whitish looking square.

Q. Yes.

A. So each of those whitish-looking squares are passivation openings where there's the bond pad. So that's where the passivation or the epoxy is open, so you can -- you can make a bond wire contact into them.

So those wires are bond wires, and the squares that they land on are the bond pads.

Q. Okay. Let me direct your attention to paragraph 113 of your declaration.

A. Paragraph 1 --

Q. 113.

A. Excuse me. I'm going to read it really quick.

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Excuse me, I see that.

Q. And you include an annotated version of Yoshinaga Figure 3, correct?

A. Correct. I mean, that's the figure you're referring to in this page, correct?

Q. Yes.

A. Okay.

Q. And do you see there's two red lines shown in that figure?

A. Yes, I see two red lines.

Q. What are the red lines supposed to represent?

A. So the red lines are supposed to represent what Dr. Foty's, you know, construction would have resulted in if we were using -- if we were using Yoshinaga with Figure 3 in it. Remember, there was Figure 1, Figure 2 or Figure 3 or Figure 4. But if we had used Yoshinaga, which was, you know, with Figure 3, and I'm recall that Figure 3 says a block diagram showing a specific example of the semiconductor integrated circuit of Figure

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1.

So Figure 3 is like a, you know, a block diagram. That's an example of Figure 1, which resides in Figure 6.

So this is Figure 3, which has two cross-couple diodes 37 shown in it. 37 is one cross-couple diode and 38, I think -- let me just check really quick -- and 38 is the other cross-couple diode.

So, you know, Dr. Foty's construction says that you would connect the supply, the reference to the common ESD bus. And so that's basically those two red lines that you see on this page.

Q. Who added the red lines in this figure?

A. If I'm not mistaken, these red lines were added, you know, in this declaration. I don't believe that they were included, the red lines were included in Dr. Foty's declaration. But the red lines are faithful to what Dr. Foty teaches in his declaration, faithful to the construction that he proposes.

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Q. Let's go to Exhibit 1008, which is the Saint reference.

A. Okay. What may I close at this point, if anything?

Q. I think you can close everything except your declaration.

A. Okay, I see. Let me do that. Just so I can reduce the number of open things on my computer and I'm sorry, you said Exhibit --

Q. Exhibit 1008.

A. -- 1008. Okay, I have opened it.

Q. And give me just a moment.

A. Yes.

Q. And if you could turn to Figure 7-7 in Saint, and I'll share that on the screen as well.

A. Okay. I'm just trying to find it. Sorry, I overshot it, so I'm almost there. Okay, I'm at 7-7 now.

Q. And the caption for Figure 7-7 reads pin-out simplification as showing like protects group together, correct?

A. Yes, the captions says pin out

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simplification showing like protects grouped together.

Q. Does Figure 7-7 show any bond pads?

A. Figure 7-7 doesn't show any bond pads, but it just shows, like the title says, you know, like protects group together.

And like protects means, you know, circuitry that's protected to the same supply and reference rails shown together. That's why you could see VCC1 and ground 1 together. You see VCC2 and ground 2 together. VCC3 and ground 3 together.

Q. Would a person of ordinary skill in the art understand that a chip implementing Figure 7-7 would have bond pads?

MR. WATSON: Objection to form.

A. A person of ordinary skill in the art looking at Figure 7-7 and also the disclosure that precedes it, they would look at everything before they would make

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any conclusions about Figure 7-7.

Q. And that would include, for example, what's shown in Figure 7-6, correct?

A. Well, not just that. They'd also look at other figures before that.

Q. And in view of the entirety of the disclosure and the other surrounding context and figures around Figure 7-7, would a person of ordinary skill in the art understand that a chip implementing Figure 7-7 would have bond pads?

A. So let me, sort of let me give you sort of like the methodology that a person of ordinary skill in the art might follow.

So, you know, maybe start with, you know, the blue page 145, you know, shown in blue, I guess.

Do you prefer the page numbers in the bottom right? I can use that.

Q. The bottom right, yeah.

A. Okay, so let's use the bottom right page numbers. So then look at page

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160. You'll see that what we're talking about is an example. That's what's described in 168. It talks about a chip with four pins per side. That's kind of what is being contemplated.

So that means right upfront they're saying that the person of ordinary skill in the art understand that there are a total of 16 pins, because there are four on each sides, and there are four sides.

And then they see this disclosure that pins 1, 5, 7 and 9 are protected against VCC1 and ground 1. That's shown in Figure 7-3.

Then Figures 7-4 and 7-5 similarly show that, you know, pins 6, 8, 10 and 14 are protected to VCC2 and ground 2 -- VCC1 and ground 1; VCC2, ground 2; VCC3 and ground 3 are completely distinct and different supply and ground, you know, terminals -- supply and ground nodes.

And finally, if I look at page 160, the person of ordinary skill in the art is learning that all the pins have

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signals that are protected to VCC and ground 3, and that's shown in Figure 7-5. And clearly those are pins 2, 3, 4, 11, 12, 13, 15 and 16.

So now between these three figures that we just saw, 7-3, 7-4 and 7-5, a person of ordinary skill in the art understands that there are a total of 16 pins as, you know, as the textbook originally started off by describing.

And then, you know, a person of ordinary skill in the art would read Figure 7-6 showing the final pin out of the package shows coordinated colors for each of the protected schemes.

So Figure 7-6 is showing a pin out because it's showing the 16 pins labeled 1 through 16.

And it's also showing them with three colors, that is, you know, all the colors of Figure 1 are shown in the top color, which I think is blue -- I happen to be color blind, I can't tell you what that color is, but there's a topmost color

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which I think is blue perhaps.

Q. Yes.

A. And then there's a middle color which looks like green or gray or something.

Q. Gray, yeah.

A. So there's a gray color.

And then if they look at the gray pins, these are the same pins that are shown in Figure 7-4.

And all the remaining pins, which are the hollow pins, the no color pins, the white-colored pins, are the pins that are shown in Figure 7-5.

So now, you know, this person of ordinary skill in the art sees as being described as a final pin-out.

And now the -- you know, from 7-6, you know, they moved to Figure 7-7. And the reason for that is basically described in the top of page 162 where it says, you know, Figures 1, 5 -- sorry, pins 1, 5, 7, 9 are scattered all over, you can literally see that in Figure 7-6.

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So they went through the exercise of moving them together so that they're all, you know, they're VCC1 and ground 1 are near to each other.

And similarly, they moved the other pins, you know, and basically they go through some logic as to why this becomes tricky.

But they also show that -- you know, in some sense, right, without -- I could kind of go through that paragraph, if you'd like. But this paragraph is saying that pins 1, 5, 7 and 9 are scattered all over.

So you do need diodes to protect them as shown in Figure 7-3. So this means you have to get VCC1 and ground 1 to these four pins, and you have to kind of move them together.

So by protecting 1, 5, 7 and 9 to a supply would run wiring past 6 and 8, if you looked at Figure 7-6. Because 6 and 8 are protected on a different supply.

So the supply wiring would then

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run past 2, 3 and 4, which are protected on a third supply.

So this basically a wiring mess that they're kind of describing and they're saying you create all these wires running past each other all getting in the way of each other and that's not a good thing.

So this is basically now what motivates them to come up with Figure 7-7. But before that, you know, they also described the wires must be large because they're ESD protection buses, ESD protection wires and they must take -- must support a lot of current. So this pin out is going to place a lot of heavy supply wiring all around and there's going to be a lot of wires in the chip over and around, all sorts of heavy supply wiring is going to make the chip, you know, bigger than it needs to be.

Sorry, go ahead.

Q. So my question is much simpler. How are the pins 1 through 16 shown in

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Figure 7-6 connected to the power and ground supply shown in Figure 7-7?

A. So the circuitry for how -- for example, you know, in the VCC1 and ground 1, you know, wiring that's shown in Figure 7-7, the pins would be connected as shown -- I mean, the electrical connections to the ESD diodes would be as shown in Figure 7-3.

The electrical and circuitry connection for the pin -- for the pins that are protected by VCC2 and ground 2 will be connected as shown in Figure 7-4.

And finally, the electrical connectivity of the pins that are protected by VCC3 and ground 3 will be as described in the circuit diagram of Figure 7-5.

Q. And are those connections implemented using bond wires?

A. Of which connections described using bond wires?

Q. Yeah, so Figure 7-6 shows 16 pins, right?

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A. Correct.

Q. The pins are external to the chip, correct?

A. That's not true. The pins are always internal to the chip.

Q. So it's your testimony that what's shown in Figure 7-6, pins 1 through 16, are actually on the chip?

A. That's correct. You know, the pins -- 1 through 16 are pads and the bonding wires would land and connect to these pads.

Q. Okay. Thank you for that.

MR. JENSEN: I think we've been going about an hour. Why don't we take a short break.

THE WITNESS: Okay.

(Recess taken from 7:14 p.m. to 7:23 p.m. MT)

BY MR. JENSEN:

Q. Dr. Khatri, what is the difference between a pad limited design and a core limited design?

A. Can you point me to a place in my

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declaration where you're referring to?

Q. I don't have a specific reference.

A. Okay. Then let me look. I think I might have talked about that in my declaration.

Okay. So this idea about a pad limited and a code limited design had come up extensively in Dr. Foty's deposition.

And I've cited to this in multiple places in my declaration, in particular. So this is paragraph 65 or paragraph, you know, 143 as well -- 65, 143, 147 and also 46. So it appears in many places.

There was no satisfactory definition of it that I found in any of this. So I looked up Saint, because I know Saint does discuss -- does talk about pad limited and core limited designs.

And Saint does define this on page 211 by your notation of the pages, page 211 and 212 and 213. So there's a couple -- I mean, there's two or three

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pages where Saint describes or defines a pad limited design.

So, you know, so this is basically the idea that, you know, in a pad limited design, the pads, you know, and how closely that you can pack them, that determines the size of the chip.

And in a core limited designs, the core or the actual chip determines the size of the chip and the pads are fewer.

Q. Does the 164 -- strike that.

Does the invention in the '164 Patent have any application in the pad limited design context?

MR. WATSON: Objection to form.

A. So the -- let me look at the '164 Patent really quick. And I'm going to do a little -- I'm going to search. I'm having some difficulty with my PDF app for some reason. Okay, there we go.

So the -- let me just look one more thing.

Yeah, so I did look at the '164 Patent and I did a search for, you know,

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core or limited and it doesn't talk about anything about a core limited design or a pad limited design, which to me, you know, reading that, you know, and also to a person of ordinary skill in the art would make sense because nothing that it teaches is restricted to one type of design or another. It's contemplated to be applicable to all designs.

Q. Let's go back to Saint Figure 7-6 and 7-7.

A. Let me open that really quick. What was Saint, the number?

Q. Exhibit 1008.

A. 1008, okay. And you said 7 -- okay, I have to go back to it because I moved away from it.

Q. And I'll share the screen, to, just to make it easier.

A. Oh, thank you.

Q. Do you see Saint Figure 7-7?

A. Just one second. I'll kind of track it with mine. Yes, I do see 7-7 in your screen as well as mine.

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Q. Okay. And in 7 -- Figure 7-7, it labels, you know, various buses as VCC3, ground 3, VCC2, ground 2, and VCC1, ground 1.

Do you see those labels?

A. Yes, I do see the labels that are VCC1 and ground 1 on the top right and VCC and ground 2 on the top -- on the bottom right. And VCC3 and ground 3 on the left side.

Q. Is it your opinion that the ground 1, ground 2 and ground 3 buses in Saint Figure 7-7 do not connect to one another?

MR. WATSON: Objection. Form.

A. So a person of ordinary skill in the art reading -- you know, I've mentioned this extensively in my declaration and, you know -- let me find that, kind of like point you to where I'm referring to in this respect. So just give me one second.

Q. And I might be able to help you. There's one place at least in paragraph

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124 where you discuss this.

A. Yeah. So there are multiple place, but let's see, let me choose a good one. So 124 is one but also 123 is another place.

So basically, you know, in the -- 124 says that Haralabidis teaches segmented rails. In fact, there's explicit disclosure about segmented rails in Haralabidis.

And these are electrically the same terminal but they are kind of discontinuous and they're connected either together at a package or at a circuit board level.

So these are something that are on the chip separated, but at the end of the day through the package or through the printed circuit board they end up getting connected.

Now, that's what is called a segmented terminal. On the other hand, the reference rails of Saint in Figure 7-7, 7-6 and so on, right, they are

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actually not segmented rails. They are not a single ground rail that's segmented, but they're actually multiple different electrically distinct, you know, ground and supply rails.

So I also say in paragraph 124 that Figure 7-7 of Saint is derived from Figure 7-3, 7-4 and 7-5.

And if we look really quickly at those three figure, you can see that in Figure 7-3, 7-4 and 7-5, VCC, the three VCCs and the three ground 3s are completely distinct terminals and they're used to connect or to protect completely different pins, like VCC1 and ground 1 are protecting 1, 5, 7 and 9. VCC2 and ground 2 are connecting 6, 8, 10 and 11. And VCC3 and ground 3 are protecting 2, 3, 4, 11, 12, 13, 15 and 16.

So these are completely different electrical terminals. They have nothing to do with each other.

And, in fact, if I was to short them, if a person of ordinary skill in the

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art -- you know, I mean, if Dr. Foty or the petition was to short them, a person of ordinary skill in the art would, you know, would not approve that because they're not meant to be shorted.

So I do say that, you know, in paragraph 124, the three reference rails, ground 1, ground 2, ground 3, and also VCC1, VCC2, and VCC3, are separate and distinct electrically with separate and distinct voltages and it would be a fundamental error to connect them as Dr. Foty suggests.

Connecting them would result in a completely wrong operation of the circuit, and this would be something that's kind of anathema to chip designers.

Q. Yeah, that's exactly what I wanted to ask you about is the passage you just read, Dr. Khatri, in paragraph 124 of your declaration where you say ground 1, ground 2 and ground 3 are separate and distinct electrical terminals with separate and distinct voltages.

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Where in the Saint reference does it say that ground 1, ground 2 and ground 3 are separate and distinct voltages?

A. So a person of ordinary -- I mean, I've sort of described this extensively, but a person of ordinary skill in the art looking at this, right, would read this clearly and say let's look at page 160 of Saint, right, and I'm going to read the text that begins with: Let's look at an example.

It says: Let's look at an example. Suppose we have a chip with 4 pins per side. In the pin-out discussion for this chip we learn that pins 1, 5, 7, 9 are protected by VCC1 and ground 1.

These are VCC1 and ground 1, they're given different names. A person of ordinary skill in the art knows that when I give a signal a different name than another signal, they are different. This is something that I would teach my undergraduate students and any electrical engineer would know.

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Similarly, continuing on, the Saint textbook continues to say we learn that signals on pins 6, 8, 10 and 14 are protected to VCC2 and ground 2.

Again, a person of ordinary skill in the art reads VCC2 and VCC1 and ground 1 and ground 2 and says these are four different things. There's no way that they should be shorted. These are, you know, separate and distinct terminals with separate and distinct voltages.

And finally, you know, the last paragraph says and finally we learn that other pins, which is 2, 3, 4, 11, 12, 13, 15 and 16 have signals that are protected on VCC3 and ground 3.

So in these three small paragraphs, a person of ordinary skill in the art is taught by Saint that there are six separate terminals. You know, three of them are supply terminals; that's VCC1, VCC2 and VCC3.

The other three are ground 1, ground 2 and ground 3.

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And there's clear disclosure by them having different names and also by the circuitry of these three different, you know, these three different terminals being separately described in Figure 7-3, 7-4 and 7-5.

So a person of ordinary skill in the art looking at these three figures and the text corresponding to these three figures has really no doubt in their mind that these are separate and distinct terminals that should not be shorted together.

Q. Is there anywhere in Saint that you're aware that have actually says that ground 1, ground 2 and ground 3 are separate voltages or are you relying on the knowledge of a POSITA and the naming convention used?

A. So I'm relying on a number of things. I'm relying on Figure 7-3, 7-4 and 7-5. I'm relying on the knowledge of a POSITA. I'm relying on, you know, what is taught in an undergraduate classroom in

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electrical engineering.

And I'm also relying on the fact that when you look at Figure 7-6 with the three different colors, if these colors could be short-circuited, then there would be no need to create a Figure 7-7 because it will be perfectly fine to, you know, to short these terminals together.

But because it's not appropriate to short, let's say, ground 1, ground 2 and ground 3 and also VCC1, VCC2 and VCC3, because it's not appropriate to short them, that is why the exercise of transforming Figure 7-6 to Figure 7-7 was even undergone.

And a person of ordinary skill in the art would readily understand that, that the reason why, you know, we had to do the rearrangement of moving "like protect" -- sorry, by moving like protects to group them together, which is the caption of Figure 7-7 -- the reason that exercise had to be undertaken is because you cannot short VCC -- I mean ground 1,

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ground 2 and ground 3. Otherwise this exercise would not have been needed.

So there's so much evidence in Saint as well as in the common knowledge of a person of ordinary skill in the art that would clearly, you know, indicate to them that these terminals cannot -- are separate and distinct terminals which should not be shorted together.

Q. Does Figure 7-7 in Saint show what happens to the ground 1, ground 2 and ground 3 signals off chip?

MR. WATSON: Objection to form.

A. See, the point of Figure 7-7, and in fact it's preceding figures all the way from 7-3, 7-4, 7-5, 7-6 and 7-7 -- the point of all of them, you know, the section that they're in is a section that's called ESD supply strategies. You see that on page 160.

So all these figures we're talking about are pertinent to ESD supply strategies.

The description of these figures

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and the text that goes with them is corresponding to ESD supply strategies. It is not to describe about packaging or bond wires or anything like that.

So it's not necessary for these figures to describe packaging or bond wires or anything like that because these figures pertain to the technical topic of, you know, how you do ESD supply strategies, which is described on page 160 of Saint.

And then one last thing I would say, is that in my experience, right, of chip design, it is frequently the case that you have distinct supply and ground, you know, terminals like this VCC1, VCC2, ground 1, ground 2.

Most of the chips, maybe not all, but most of the chips that I've done had separated VCCs and grounds and we were super careful not to short them because that would be -- that would basically damage the electrical performance of the chip.

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So a person of ordinary skill in the art would also know that and they would know that, you know, it would be seriously inappropriate, electrically inappropriate to short ground 1, ground 2 and ground 3.

MR. JENSEN: I don't want to cut you off, Dr. Khatri, but I think we're out of time.

THE WITNESS: I see.

MR. JENSEN: I'll reserve our rights as noted on the record include to go compel further testimony and will pass the witness at this time.

EXAMINATION BY
MR. WATSON:

Q. Dr. Khatri, earlier in this deposition you were asked about the plain and ordinary meaning of the term "save space."

Do you remember that?

A. I do remember that.

Q. And in your answer you referred to paragraph 39 of your declaration. Did

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you refer to -- strike that.

Did you refer to paragraph 39 of your declaration in answering that question?

MR. JENSEN: Object to form. Leading.

A. I don't clearly remember, but I do remember that I have some paragraph or paragraphs discussing the plain and ordinary meaning.

Q. Can you please turn to paragraph 39 of your declaration?

Can you let me know when you're there?

A. Yeah, I'm here.

Q. How many construction of saved area did you apply in your invalidity analysis?

A. So let me read this. I'm just going to read out this paragraph.

Paragraph 39 says: Dr. Foty asserts that the terms of the '164 Patent's claims have their plain and ordinary meaning. I have applied such a

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meaning for the purposes of this IPR. I reserve the right to propose alternative construction in other proceedings or to amend my opinions if the Board provides an alternative claim construction.

Q. Dr. Khatri, how many construction of saved area did you apply in your invalidity analysis?

A. So the construction of saved area that I applied were the constructions that Dr. Foty presents, and I think he presents them in paragraph 161 in his declaration.

Q. Did you apply any other plain and ordinary meanings in reaching your obviousness analysis?

A. No. I applied Dr. Foty's construction, which is from paragraph 160-something -- I think it's 161 or 160.

Q. Did you offer any opinions about whether Dr. Foty's plain and ordinary meaning was correct?

A. So I don't have an opinion of whether, about whether his construction is correct or not, but I just use his

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construction, you know, because that's the construction he presented. So I used his construction for my declaration.

Q. Earlier you were asked about whether you offered opinions about obviousness if the Yoshinaga modified Figure 6 had the same number of power supply pads as the original version.

Do you remember that?

A. Yes, I do remember a discussion about that.

Q. Can you turn to paragraph 55 of your declaration?

A. Yes. Yes, I'm there now.

Q. Can you read that real quick?

A. Okay. So paragraph 55 says that a POSITA would have understood petitioner's proposed reduction in power supply pads would negatively affect the operation of Yoshinaga's Figure 6 chip and possibly render Yoshinaga inoperable. The effective reduction in power supply pads proposed by petitioner will result in a slower chip because there are less supply

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pads providing power to the circuit. Having a smaller number of power supply pads than are necessary (as petitioner and Dr. Foty propose NN, will also cause operating problems and potentially result in the failure of all three circuit blocks and the chip itself. Further, petitioner's changes remove power supply pads from area that need them, such that even if supply pads were added in other locations, they may not adequately meet the circuit's needs. Neither Dr. Foty nor the petition address these problems.

Q. What are the opinions you offered about obviousness if Yoshinaga modified Figure 6 had the same number of power supply pads as the original Yoshinaga Figure 6?

A. So the opinions are in the last, I guess the last couple of lines where it says that further petitioner's changes remove power supply pads from areas that need them such that even if supply pads were added in other locations, they may

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not adequately meet the circuit's needs.

In other words, even if the supply pads were added back, they won't meet the circuit's needs.

Now, in general, I was referring to paragraphs 41 to 70, I remember think, and I knew there was somewhere where I wrote this, but I didn't remember exactly where it was, but -- yeah, I mean -- you know, because it was buried in one of these paragraphs. But this is exactly what I meant by that argument.

Q. And what do you mean by that argument?

A. Sorry, this is what I meant by, you know, what will happen if, for example, supply pads were added back in other locations. Even if we did that, you know, they may not adequately meet the circuit's power supply needs just because, you know, pads are non-fungible and they may not be in the right location.

So the IR drops might be increased or the LDIDD noise might

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increase, or the -- problems might increase. There might be all kinds of electrical problems. A chip might slow down or fail altogether.

So that's what I meant, that even if you were to add back power supply pads, that's what the last two lines here say, even if you were to add back the two power supply pads, the chip might not function as it should.

MR. WATSON: Okay. I don't have any other questions.

MR. JENSEN: Thank you for your time, Dr. Khatri.

THE WITNESS: Thank you, Travis.

MR. JENSEN: You have our order and turnaround time?

THE COURT REPORTER: Yes, I do. Tom, would you like a rough draft?

(Continued on next page to include signature and jurat.)

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MR. WATSON: I don't need a rough. Just send us a final. Standard time is fine.

(Time noted: 5:48 p.m. MT)

_____

SUNIL KHATRI

Subscribed and sworn to before me this ___ day of _____, 2025.

_____

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REPORTER CERTIFICATE

I, JOAN FERRARA, do hereby certify:

That said proceedings were taken at the time and place herein named; and that the transcript is a true record of the testimony as reported by me, a disinterested person, and was thereafter transcribed.

I further certify that I am not interested in the outcome of the said action, nor connected with, nor related to any of the parties in said action, nor to their respective counsel.

IN WITNESS WHEREOF, I have hereunto set my hand this 8th day of December, 2025.

Joan Ferrara

JOAN FERRARA, RMR, FCRR

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DEPOSITION ERRATA SHEET

Case Caption: Micron Technology

DECLARATION UNDER PENALTY OF PERJURY

I declare under penalty of perjury that I have read the entire transcript of my Deposition taken in the captioned matter or the same has been read to me, and the same is true and accurate, save and except for changes and/or corrections, if any, as indicated by me on the DEPOSITION ERRATA SHEET hereof, with the understanding that I offer these changes as if still under oath.

_____

SUNIL KHATRI

Subscribed and sworn to on the _____ day of _____, 2025, before me,

_____

Notary Public,in and for the State of _____

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