

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00118
U.S. Patent No. 10,879,164

REPLY DECLARATION OF DR. DANIEL FOTY

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I. INTRODUCTION

1. I have been retained by counsel for Micron Technology, Inc. (“Micron” or “Petitioner”) in the above-captioned matter as an independent consultant to offer opinions regarding the patentability claims 1-14 (the “Challenged Claims”) of U.S. Patent No. 10,879,164 (the “’164 patent” or the “Challenged Patent”).

2. I have been asked to reply to the Patent Owner Response (“POR”) and certain opinions in Dr. Sunil Khatri’s declaration (Ex. 2010). Thus, I submit this declaration in support of the Reply filed by Petitioner. Since the Reply length is constrained by PTAB rules, this declaration will similarly be constrained in scope. As such, the fact that I do not respond to particular assertions made by Patent Owner or opinions expressed by Dr. Khatri should not be considered in any way to indicate agreement with those assertions and/or opinions.

3. My opening declaration (Ex. 1003) (which I incorporate by reference), sets forth (among other topics) my compensation, educational background and professional experience, etc. In reaching my conclusions and forming my opinions in this Reply Declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, my work with those of ordinary skill at the time of the alleged invention, and my general experience in the field of art.

4. I have also reviewed and considered the materials listed in my prior declaration, the Board's Institution Decision (Paper 22), Patent Owner's Response (Paper 31) and exhibits thereto (including the Khatri Declaration of Ex. 2010), and the materials listed in Petitioner's Reply, and any other materials cited herein.

II. OVERVIEW OF CONCLUSIONS

5. After reviewing the POR and accompanying declaration of Dr. Khatri (and related materials as listed above), it is my conclusion and opinion that Patent Owner failed to rebut the analysis and conclusions provided-by and reached-by (respectively) Petitioner in the Petition and by myself in my opening Declaration. The reasons for my conclusions and opinions will be explained in the analysis section which follows; however, it should be noted here that both Patent Owner and Dr. Khatri simply ignored large amounts of evidence and analysis that was presented in the Petition and in my opening Declaration – as well as the teachings and disclosure of Patent Owner's own references.

6. For example, both Patent Owner and Dr. Khatri ignored the Prosecution History of the '164 patent (which is very germane to this matter), including the reason why the '164 patent was issued (*i.e.*, material which, as it turns out, was actually (and demonstrably), well-known in the art prior to the filing of the patent application in 2018). As a result, Patent Owner and Dr. Khatri incorrectly identified other material as the alleged inventive concept, and have ignored references supplied

by Petitioner (and myself) which demonstrate that this alleged inventive material was already well-known in the art. Patent Owner and Dr. Khatri have also misinterpreted several of their own references – by failing to properly read them and to perform suitable due-diligence on them.

7. My conclusion and opinion remain that the '164 patent claims are indeed unpatentable.

III. ANALYSIS AND OPINIONS

8. In reviewing the POR, Dr. Khatri's declaration, and other materials (as listed above), I found that Patent Owner's and Dr. Khatri's various assertions could conveniently be grouped into five categories; thus, although there is naturally some interrelation among those five categories, my analysis is grouped into modules that consider each category in turn.

A. Patent Owner's POR is Marred by a Number of Glaring Omissions

1. Patent Owner Avoids Discussing Key Materials and Evidence

9. The POR completely ignores key materials from the Petition – as well as the analysis-of and conclusions-drawn-from those materials. Three notable instances will be mentioned here; in two of those instances Patent Owner simply ignored key evidence, while in another the Patent Owner provided a “rebuttal” of sorts – but it was actually directed at other materials introduced for other reasons.

10. These three instances effectively amount to three situations of the proverbial “dog that did not bark.”¹ As such, Patent Owner has provided no response to this evidence and its analysis – leaving the conclusions drawn from that evidence unchallenged.

a. Patent Owner Avoids Discussing the '164 Patent Prosecution History – and the Implications Drawn from It

11. In my opening Declaration, in the discussion associated with claim element [6e], I discussed the Prosecution History of the '164 patent, including the “saved area” limitation that was the reason for allowance. Ex. 1003, ¶¶167-168. It was (and still is) my conclusion and opinion that the Examiner erred in his assessment of the “saved area”² as being inventive material – since this exact concept was explicitly taught in 2002 in Saint Figure 9-28 (with the reasoning leading up to this figure clearly beginning on p. 213 of Saint and Figure 9-21 of Saint).

¹ This is a reference to the Sherlock Holmes novel “The Adventure of Silver Blaze” where the fact that a dog remained silent while a horse was stolen was a significant event – as it meant that the thief was not a stranger to the dog. Here, Patent Owner’s silence on key evidence is also very telling.

² It is also notable that Patent Owner attempts an assertion that the “saved area” of the '164 patent and the “wasted space” of Saint are somehow different; as will be discussed below, this assertion is demonstrably false.

12. Faced with this challenge, Patent Owner simply refused to respond – providing only a statement that space constraints precluded Patent Owner from discussing the Prosecution History of the '164 patent. However, it is notable that Patent Owner's POR came in at a total of 13,341 words – which is 659 words below the required limit. This plainly indicates a decision to ignore the issue.

13. At his deposition, Dr. Khatri was asked if he had reviewed the Prosecution History of the '164 patent during the preparation of his Declaration:

Q. Did you review the file history for the '164 Patent in preparing for your declaration or your deposition?

A. Let me see. I don't -- I've gone over it tangentially at one point, but I don't think that was an issue that was brought up and is not something that I've opined on. So I didn't look at it in any great detail. But I do recall seeing it a long time ago.

Ex. 1038 (Khatri Tr.), 50:20-51:6. This is a rather circuitous response to a simple question – but the answer indicates that Dr. Khatri did not meaningfully review the Prosecution History in the preparation of his Declaration.³

14. Dr. Khatri was asked the same question later in his deposition, with the following testimonial result:

³ On this point, Dr. Khatri later opines (repeatedly) that he believes that the supposed invention of the '164 patent is using a pad-to-pad bondwire connection. This issue will be considered in more detail in Section III.C.

Q: Did you review the file history in this case?

A: I might have eyeballed it, ***but I don't think it was something that was brought up.*** So, you know, it's not part of my declaration.

Ex. 1038 (Khatri Tr.) 279:18-23 (emphasis added). In addition to corroborating Dr. Khatri's earlier testimony, this testimony includes an assertion that is simply incorrect—contrary to Dr. Khatri's testimony, the Prosecution History ***was*** “brought up” in both the Petition and my opening Declaration. For both Patent Owner and Dr. Khatri to simply ignore these findings is a true “dog that did not bark.”

b. Patent Owner Ignores Figure 9-28 of the Saint Reference – While Directing a “Rebuttal” of Sorts at Different Material

15. With respect to Saint Figure 9-28, a similar situation arises. As described in my opening Declaration, Figure 9-28 of Saint (and the discussion leading up to it) clearly discloses the presence of a “saved area” (what Saint calls “wasted space” is the same thing). However, in its POR, Patent Owner actually (and literally) makes no mention at all⁴ of Figure 9-28 of Saint – and thus leaves the conclusions I drew (as explained in my opening Declaration) from this figure (and the discussion leading up to it) unchallenged. Given how prominently Saint Figure

⁴ In his declaration, Dr. Khatri mentions Saint Figure 9-28 only once; however, even this passing-mention makes no challenge to my conclusion and opinion that Figure 9-28 of Saint clearly discloses the “saved area” of the '164 patent.

9-28 figured in both the Petition and my opening Declaration, the Patent Owner's decision to ignore it is another notable "dog that did not bark."

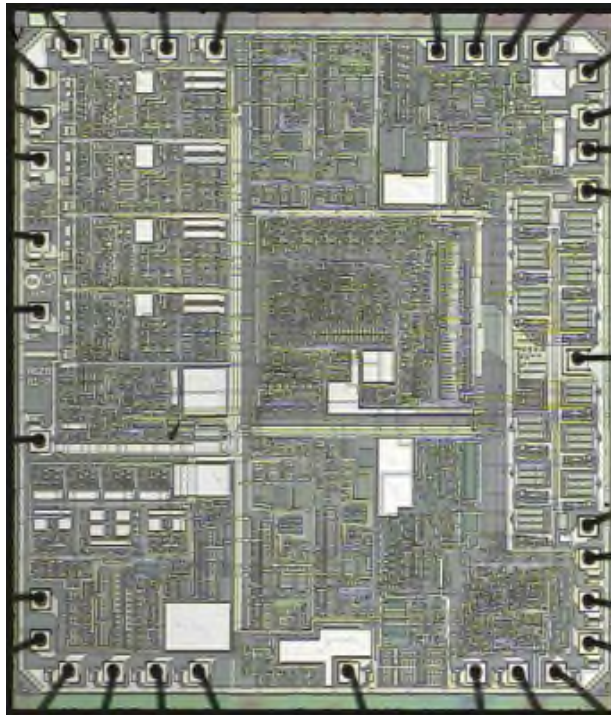
16. Tellingly, in its POR Patent Owner attempts to "rebut" the saved area conclusions Petitioner reached with regard to Figure 9-28 – but without even mentioning Figure 9-28 of Saint; rather, Patent Owner's "rebuttal" focuses on Figure 7-7 of Saint rather than Figure 9-28 of Saint. This is a bait-and-switch argument as Petitioner (and myself) clearly relied on Saint Figure 9-28 to show prior art for placing circuitry in the "saved area" between bond pads.

17. Patent Owner's argument that modified Saint Figure 7-7⁵ has more than 16 pads (POR, 68) misses the forest for the trees. Like unmodified Figure 7-7 (and Figures 2 and 3 in the '164 patent – which are not drawn to scale nor limited to a specific number of pads), Petitioner's modified figure is conceptual and not a bodily incorporation. The exact pad count is immaterial—what matters is the presence of a saved area. Patent Owner argues that the Saint combination is improper because Saint teaches "evenly spaced" pads (POR, 68); however, this assertion ignores the simple fact that Saint Figure 9-28 has unevenly spaced pads, and so the argument fails; this topic is further addressed in §III.B.5 (discussing the use of a pad template).

⁵ Patent Owner sometimes argues that Saint Fig. 7-7 "does not show ... pads" (POR, 66-67), but elsewhere Patent Owner discusses "restructuring [the] pads in Fig. 7-7" (*id.*, 68-69), recognizing that they are present.

c. Patent Owner Ignores a Microphotograph of an Actual IC Product that Clearly Shows Circuitry Placed in Spaces Between the Pad Groups

18. Finally, in my opening declaration, I included a simple microphotograph⁶ which depicted an IC from a product part that had been exposed during a “reverse-engineering” teardown:



In this microphotograph, the bonding pads (and the bondwires connected to them) are clearly visible. This microphotograph clearly shows a core-limited IC, where circuitry has been placed between bond pads.

⁶ <https://cdn.sparkfun.com/r/4000-400/assets/e/f/1/b/8/51c0d009ce395ff933000000.jpg>

19. Despite the microphotograph explicitly showing circuitry being placed in the “saved areas” between pad groups in a core-limited situation, Patent Owner makes no mention of this image in its POR – and simply avoids discussing it.

2. Patent Owner’s Accusations of “Manipulation” are Inappropriate

20. Finally, in terms of a dog that *did* bark, Patent Owner reproduces a figure that was included in both the Petition and my opening Declaration – and refers to this figure as having been “manipulated.” This accusation is not only false – it is inappropriate to the point of being scurrilous.

21. The figure in question depicts a typical obviousness analysis where one reference is either combined with another reference *or* with the demonstrated knowledge of a POSITA. Here, the figure in question is from Yoshinaga. Nothing was “manipulated”⁷ in any way, shape, or form. Rather, the proposed changes were explicitly discussed and annotated, and colors were used to assist in mapping to the claims. Patent Owner (and Dr. Khatri’s) insinuations of foul-play are inappropriate.

3. Patent Owner’s Attempted Rebuttals are Weak and Superficial

22. In addition to simply ignoring evidence as discussed above, Patent Owner’s attempts to rebut Petitioner’s evidence, analysis, and assertions are

⁷ The Merriam-Webster dictionary defines “manipulate” as “to change by deceptive or unfair means so as to serve one's purpose.” Clearly this did *not* occur with the figure in question. www.merriam-webster.com/dictionary/manipulate.

superficial and very weak. For example, Patent Owner’s assertions rely on “analysis” that amounts to, e.g., cherry-picking offhand comments in a reference (even with respect to ***their own*** references) and misconstruing them and/or treating them as broadly applicable definitive statements (*e.g.*, an engineering design choice does ***not*** imply that it is the only way to do something).

23. Patent Owner’s “analysis” is (as will be demonstrated below) readily-shown to be incorrect – and even a minimal amount of investigation demonstrates this. It is further-notable that if various Patent Owner assertions were true (which they are not), ***Patent Owner’s own patent would be inoperable.***

B. Pad-Limited vs. Core-Limited Chips

1. Patent Owner Misunderstands the Nature of a “Pad-Limited” Situation vs. a “Core-Limited” Situation – Even Though Those Two Concepts are Fundamental in This Matter

24. In my opening Declaration, I described the concepts of “pad-limited” IC design and “core-limited” IC design – and explained why these concepts are fundamental to this matter. However, in its POR, Patent Owner clearly does not grasp these concepts – or their importance – even though these concepts have been known for decades. Saint (from 2002) provides an excellent description of these concepts, ***and*** their importance in IC design and manufacturing.

2. Smaller ICs Reduce the Cost Per Manufactured IC

25. To begin, it should again be noted (as it was in my opening Declaration) that it is desirable to make an IC (i.e., a silicon “chip”) as small as possible. The main reason for this goal is simple economics. The cost of an IC is based on the cost-per-finished-wafer that a foundry (or similar) charges for a particular manufacturing process – and so, for the IC designers, that per-wafer cost is fixed; further; the number of chips that fit on a wafer is a function of chip size. Simply put, the smaller the chip, the more chips fit on a wafer - and the lower the cost per chip. The strong desire for smaller chips (which results in lower per-unit-product cost) has driven the semiconductor industry for decades, and did not stop in 2018 when the ’164 patent was filed. And, importantly, the reduced-size benefits flowing from grouping power domain pins together are additive/complementary with Saint Figure 9-28’s saved area teachings. Indeed, the pin groupings disclosed in Saint Figure 7-7 which create empty spaces between buses dovetail perfectly with Figure 9-28’s teachings of using empty space between pads.

3. Pad-Limited IC Design

26. A “pad-limited” design is an IC design where the overall IC size is limited by the need to include a minimum number of pads (as opposed to the area consumed by the actual circuitry). This has long been a well-known concept in the IC industry and is well-explained by Saint:

First, identify your signal requirements. From that, you can determine the minimum size of the chip, based just on the number of signals, and hence bond pads, needed.

Find the minimum required spacing between the pads, and squeeze those pads as close together as you can in a rectangular shape. Then you say, “That’s my chip. That’s pad-limited.”

Saint, pp. 211-212. By “squeeze those pads as close together as you can,” Saint is describing the well-known concept that the bond pad size and minimum pad-spacing distance are dictated by the ground rules for the manufacturing process that will be used to fabricate the IC.

27. Saint then includes a graphical depiction of such an IC floorplan – where in this example it has been determined that 18 bond pads are required (i.e., 18 off-chip connections to package pins are required):

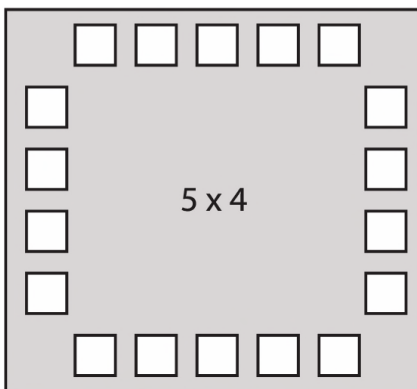


Figure 9–20. The minimum size of an 18-pad chip, based on the number of pads.

As Saint explains with regard to this exemplary IC floorplan,

Irrespective of how much circuitry you have in the middle of this chip, this is the smallest that you can make it using your given number of pads.

Saint, p. 212. In this particular situation, the pads are as small as possible (and thus are all identical), and all the pads are separated by the minimum-allowed inter-pad spacing (so that all the pads are evenly-spaced from each other).

28. If the available space inside of the pad-periphery is greater than the amount of space required for the circuitry, then the design is said to be “pad-limited.”

Saint provides several examples of full pad-limited IC floorplans.

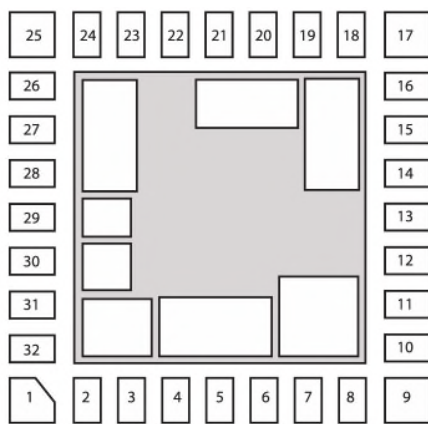


Figure 8-5. Tempting pinup poster, popular with circuit designers.³

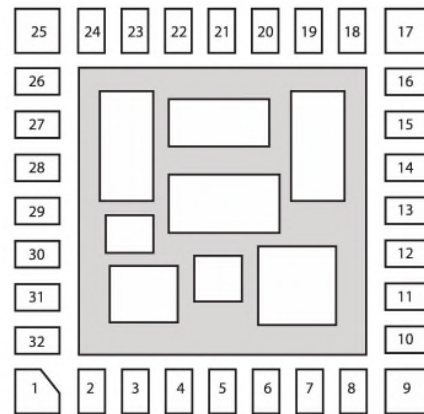


Figure 8-6. Instead submit this. Keep the fresh air for yourself. Don't let them find it. You will need it for those last second additions.

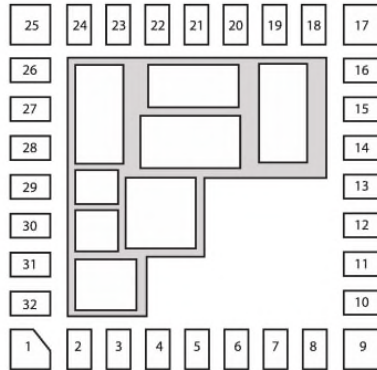


Figure 8-7. It's difficult to combine this with other blocks, but it might just open some free space you need on the chip. It's an option.

Saint, pp. 188-189. Saint notes that these various options reflect engineering flexibility, including the ease with which circuitry blocks can be rearranged.

4. Core-Limited IC Design

29. A “core-limited” design situation is essentially the opposite of the pad-limited case – *i.e.*, the amount of circuitry (rather than the required number of bond pads) determines the minimum-possible size of the IC. Saint explains this situation very succinctly:

[S]ometimes you do not need quite as many pads, compared to the amount of circuitry you will need.

In this case, you would want to better examine the circuitry requirements to determine a rough sizing estimate. This is called a **core-limited design**, or **circuit-limited design**. ... The number of pads is no longer the most limiting issue. The rest of the chip is. The circuitry is driving how big the chip will be. Once you have an idea about the sizes of your required circuitry, place the pads around the outside.

Saint, p. 213 (emphasis in the original).

30. Along with this discussion, Saint depicts an exemplary core-limited IC:

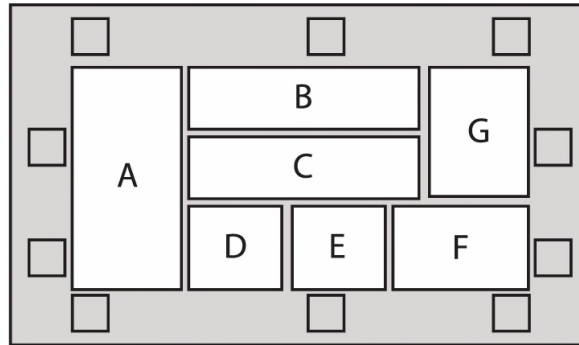


Figure 9-21. The minimum size of the chip limited by the anticipated sizes of the blocks.

The interior circuit area is completely occupied (i.e., filled) by the circuitry blocks; meanwhile, the pads that are required are placed around the periphery.

31. One type of design flexibility available in core-limited designs that is well-known in the art (as will be shown below) is succinctly explained by Saint:

Filling Pad Gaps

If you do have a core-limited circuit design, ***you will have wasted space around the edges between the pads. Maybe you can push some of your circuitry into this wasted space to try to use those gaps.***

If you are reusing circuits, then you can re-lay parts of your circuit elements in and around these pads trying to get the chip as small as possible.

Saint, pp. 220-221 (emphasis added).

32. Saint provides an exemplary floorplan for a core-limited IC design that takes advantage of this flexibility by pushing circuitry into those empty spaces (of the Figure 9-21 depiction) to reduce the size of the overall IC

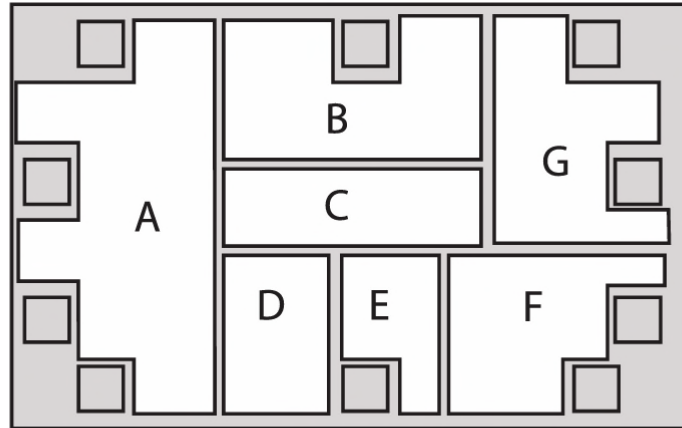
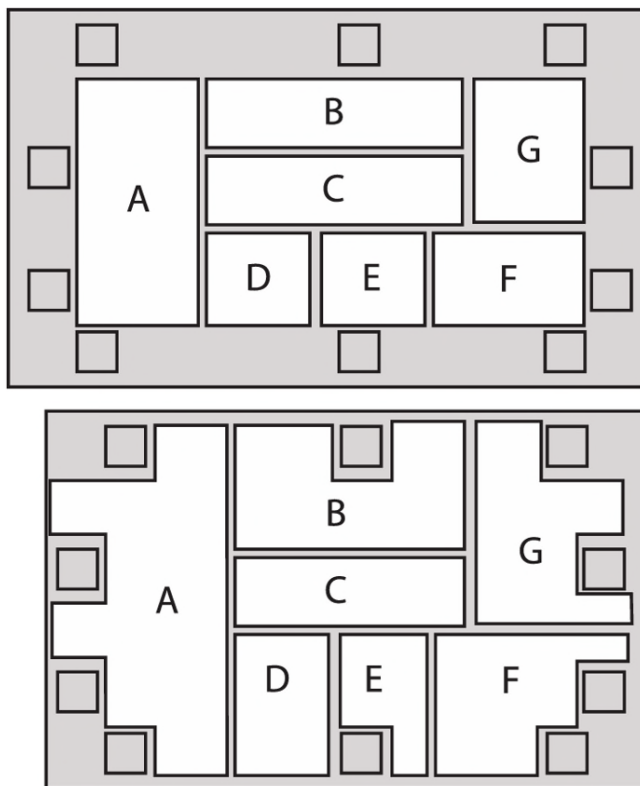


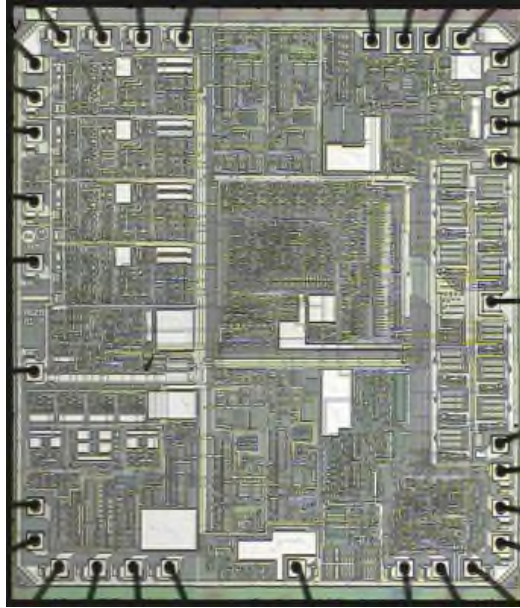
Figure 9–28. *We can use extra space surrounding our pads to shrink our chip size.*

The previously-empty space between the pads has now been put to good use, as the circuitry blocks have been modified so as to push circuitry into those previously-empty spaces. Further, comparison of Figures 9-21 and 9-28 shows that Saint depicts this ability to reduce the size of the IC in these exemplary depictions – as the IC footprint of Figure 9-28 is indeed smaller than the IC footprint of Figure 9-21. A top-and-bottom comparison of Figure 9-21 and Figure 9-28 confirms this difference.



As can readily be seen, the IC size has been reduced by pushing circuitry into the space between the pads; note also that this is literally what Saint is showing – since in both figures the pad size remains the same (providing a “scale” for the two figures), which confirms that the Figure 9-28 IC is indeed notably-smaller.

33. The IC microphotograph from my opening Declaration provides another example of the placement of circuitry in saved areas between pads. It is interesting to note that the (2010) article in which this microphotograph appears makes no mention of this placement of circuitry in the regions between the pads – indicating that this type of layout (in a core-limited situation) was commonplace in the industry by that time.



5. Because Patent Owner Fundamentally Misunderstands the Pad-Limited and Core-Limited Concepts, Its Analysis Misfires Badly

34. As noted, Patent Owner (and its expert) shows no indication of understanding the basic nature of “pad-limited” IC design and “core-limited” IC design – despite the obvious importance of these concepts to this matter. This was the impetus for repeating the explanation above. Because of this fundamental misunderstanding, Patent Owner’s assertions against Petitioner’s analysis and conclusions misfire badly – for several reasons.

35. First, as noted in §II.A.1.a, Patent Owner simply ignored important aspects of the file history of their own patent *and* of the analysis provided by Petitioner. And, as §II.A.1.b notes, Patent Owner *completely* ignored Figure 9-28 of Saint – and the analysis and conclusions Petitioner provided regarding that figure.

36. Figure 9-28 of Saint – and the explanations provided by Saint of the progression from Figure 9-21 to Figure 9-28 – clearly shows that the concept of using “saved area” between bond pads to reduce chip size was known in the prior art well before 2018.

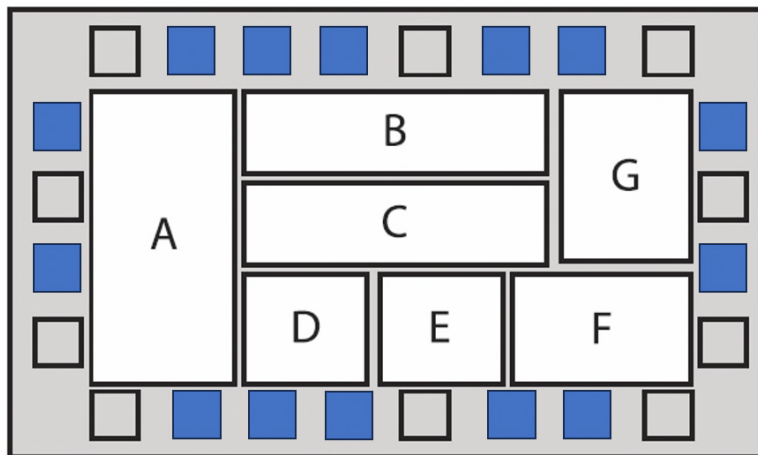
37. Rather than engage with Figure 9-28, Patent Owner engages in misdirection. Patent Owner attempts to dispute Petitioner’s Saint-related conclusions by leveling criticism **not** at Petitioner’s analysis of Figure 9-28, but rather by directing it at Petitioner’s analysis of Saint Figure 7-7; this is an attempt to give the reader the (incorrect) impression that Petitioner’s Saint-related conclusions regarding “saved area” originate with Figure 7-7 (rather than from Figure 9-28). This misdirection by Patent Owner is incorrect, as Petitioner invoked Saint Figure 7-7 primarily to show the disclosure of **segmented ESD buses**. Given pad flexibility in a core limited design (like that in Figure 9-28), it was obvious to align the empty space between the segmented ESD bus portions with empty space between pad groups for the provision of a desirable area of empty space into which circuitry could be pushed (for the purpose of reducing the overall size of the IC).

38. Patent Owner also tries to give the misimpression that the “saved area” of the ’164 patent and the “wasted space” of Saint are different things – when, in fact, they are the same thing. Patent Owner repeatedly (e.g., at POR, 45-47) asserts that the “saved area” of the ’164 patent is “created,” “added,” or “formed” in some

way; however, this does not appear in the claims of the '164 patent.

39. The only situation where pads ***might*** be “removed” would be if the IC designers began their floorplan with a blank template that included a set of pads (in the design layout) that filled the periphery of the IC floorplan – and from which pads were then “removed” (from the layout) for the core-limited situation at hand. While the '164 patent mentions this approach in connection with the “filler” cells, it is just an example - and, notably, no mention of adding/removing “filler” cells appears in the claims. Moreover, the '164 specification says that “the present invention ***may*** get rid of the filler cells,” reflecting that it is just one option. Ex. 1001, 4:16.

40. Interestingly, Saint Figure 9-21 actually renders this approach obvious. If one takes the pads in Figure 9-21 and repeats them around the periphery of the chip, the following results:



Saint, Figure 9-21 (annotated to add/show blue pads). As can be seen, the pads are arranged with identical size, shape, and spacing. It is common for IC designers to

begin with such a simple template for an IC design – and to then “remove” (in the layout) pads that are extraneous to the core-limited design in question. It is thus clear that the depiction of Figure 9-21 of Saint would produce the core-limited pad arrangement by simply removing unnecessary pads from a pad template.

41. Patent Owner’s fundamental misunderstanding of pad-limited versus core-limited designs is reflected in the testimony of Dr. Khatri, who erroneously believes that the ’164 patent applies to both types of designs. Because adding a “saved area” to a **pad-limited** design (which already has more space than needed for circuit blocks) would make the chip bigger (and thus increase the per-chip cost due to fitting fewer chips on a wafer), nobody in their right mind would ever do it.

42. At his deposition, Dr. Khatri was asked a simple question about these concepts with respect to the ’164 patent:

Q: Does the invention in the ’164 Patent have any application in the pad limited design context?

A: ... Yeah, so I did look at the ’164 Patent and I did a search for, you know, core or limited and it doesn’t talk about anything about a core limited design or a pad limited design, which to me, you know, reading that, you know, and also to a person of ordinary skill in the art would make sense because nothing that it teaches is restricted to one type of design or another. It’s contemplated to be applicable to all designs.

Ex. 1038 (Khatri Tr.), 342:13-343:10. As per what was discussed above, this is simply incorrect. Neither Patent Owner nor Dr. Khatri understands the implications of this concept to either the '164 patent or the cited prior art.

6. My Opening Declaration Did Not “Construe” the Term “Saved Area”

43. During his deposition, with respect to the term “saved area,” Dr. Khatri made reference to a construction of this term that I had supposedly introduced and used. *E.g.*, Ex. 1038 (Khatri Tr.), 265:16-22, 267:2-16, 356:7-357:4. Notably, during his redirect examination Dr. Khatri said:

Q: Dr. Khatri, how many construction [sic] of saved area did you apply in your invalidity analysis?

A: So the construction of saved area that I applied were ***the constructions that Dr. Foty presents***, and I think he presents them in paragraph 161 in his declaration.

Q: Did you apply any other plain and ordinary meanings in reaching your obviousness analysis?

A: No. I applied ***Dr. Foty's construction***, which is from paragraph 160-something -- I think it's 161 or 160.

Q: Did you offer any opinions about whether Dr. Foty's plain and ordinary meaning was correct?

A: So I don't have an opinion of whether, about whether ***his construction*** is correct or not, but I just use ***his construction***, you know, because that's ***the construction***

he presented. So I used his construction for my declaration.

Ex. 1038 (Khatri Tr.), 356:7-357:4 (emphasis added). Particularly given the number of times (both here and earlier) that Dr. Khatri made reference to a “saved area” construction that I supposedly offered, this warrants clarification.

44. In my opening Declaration, I neither requested construction of the term “saved area,” nor did I provide any proposed construction for this term; the same can be said of Petitioner and the Petition. It is unclear why Dr. Khatri kept bringing this topic up.

C. Wire Bonding Basics

1. Patent Owner Misunderstands the Basic Nature of Wire Bonding – Even Though This Technology Has Been Used for Decades

45. In its POR, Patent Owner displays a surprising degree of misunderstanding of both the basic nature of wire bonding technology **and** its use in IC design and development – even though this technology has been in widespread use for decades. This shortcoming causes Patent Owner to make assertions that are simply incorrect – and to draw unsupported conclusions. Further, these errors are so significant that it can readily be seen that if Patent Owner’s assertions were correct (and they are not), they would indicate that wire bonding is not (and could never have been) a viable technology – even though it is obvious that wire bonding has long been a viable and in-use technology; in addition, if these assertions were

correct, they clearly would render Patent Owner's own patent inoperable.

46. As an initial matter, I note that bond wires have no active circuitry or components and are, literally, just metal wires. Far from being "complex" (as Patent Owner asserts), bond wires are relatively simple, especially when compared to the processes required to fabricate metal traces on a chip.

2. Wire Bonding has Long Been Used in IC Technology for Packaging and to Connect Two Bond Pads – and Continues in Wide Use Today

47. A core aspect of a silicon IC is that the small feature sizes make them inaccessible to the outside world – because transistor terminals are too tiny to be contacted directly. Thus, a silicon IC requires some way of connecting signals, power, and ground to the outside world; further, the "raw" IC is typically packaged for use in real electronics products. Early on in the development of ICs, a method was developed that addressed these problems – and in a manner which was (and remains) simple, robust, reliable, repeatable, and cost-effective.⁸

48. To provide points of external contact on the IC, large metal "pads" are often placed around the periphery of the IC – pads which connect to internal chip circuitry and metal traces.

⁸ Among other things, "cost-effective" means that the incremental costs associated with wiring bonding are small – and the wire cost itself is negligible. Dr. Khatri agreed wire bonding is low-cost. Ex. 1038 (Khatri Tr.), 132:8-16, 133:25-134:16.

49. Packages are typically constructed of either plastic or (for some situations) a ceramic material. But the basic notion of a package (of any type) is that it contains pins – pins that are connected to the pads of the IC as shown above. While numerous package styles are used, Saint provides a depiction of a typical package:

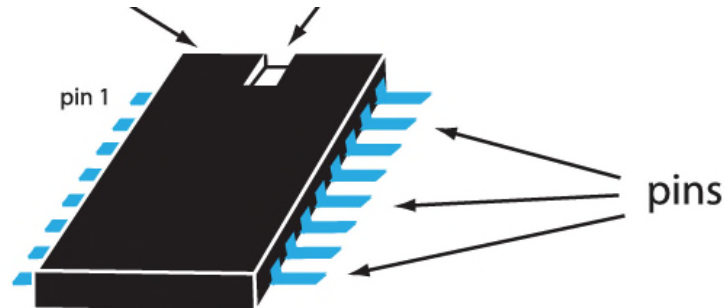


Figure 9–1. *The plastic or ceramic package is all you see when you install a chip.*

50. The simple method of providing the connections that are depicted in Saint Figure 9-3 (above) is wire bonding – which is basically what the name says.

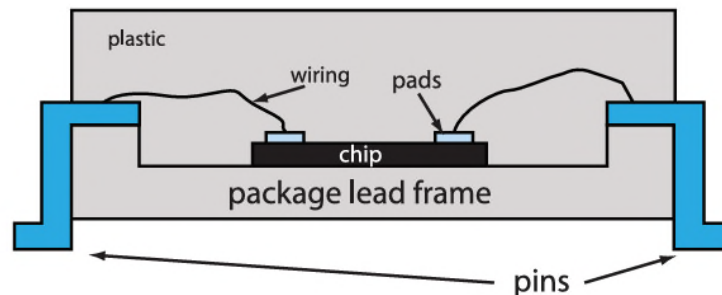


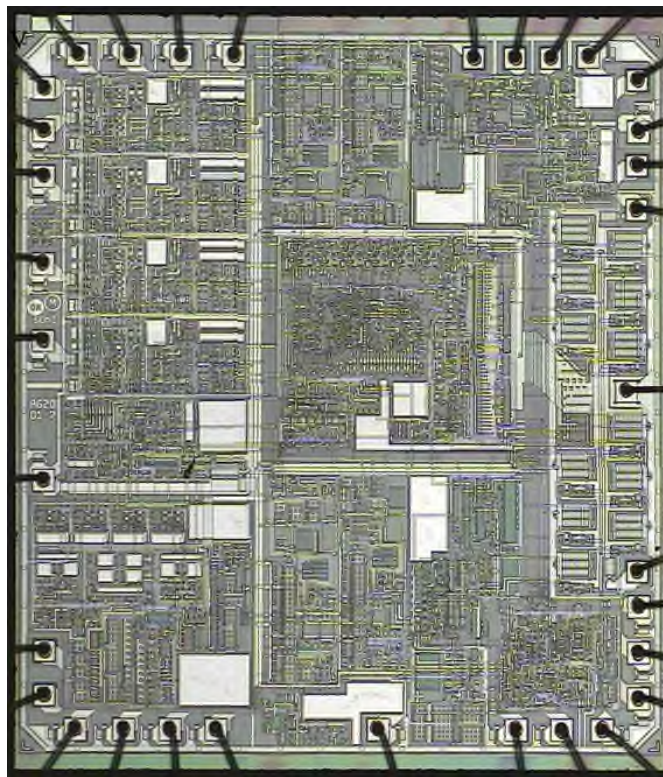
Figure 9–2. *The top plastic is molten when deposited. The wires are surrounded before it hardens.*

The IC is placed in the middle of the package, and bond wires are connected between the IC pads and the package traces.

51. Wire bonding is done with equipment designed to do exactly this job. Very low resistance materials are used for the wires – with gold having long been

the most-common choice; despite the high price of gold, the tiny amount of material used for the wiring makes the expense a non-factor – although other metals have also been used, including copper in more recent times. When used in wire bonding, these wires have very low resistance⁹, are robust and reliable, and are inexpensive.

52. This is also a good place to note that the purpose of bond pads in an IC design is simply to host bond wire connections. In my opening Declaration, I provided an example of what an IC product looks like at this point – with the bond wires connecting to the bond pads:



⁹ This topic is considered in more detail below.

As can readily be seen, this (real product) IC has bond pads, the bond wires (which connect to the package traces outside the microphotograph) connect to the bond pads, and the connection on each bond pad shows the low-contact-resistance “bond ball” that is formed by the methods (mentioned above) that are used to connect the bond wire to the bond pad. (Note also that the bond wires are much larger (in diameter) than the size of the (basically invisible at this scale) on-chip features, such as transistors.)

53. Returning to Saint Figure 9-2 (included above), this figure also shows that after the wire-bonding has been completed, the IC and the bond wiring must be protected – so that in the product, neither the IC nor the wiring can be disturbed by external elements in the real world; this is usually done (as shown) by sealing up the IC and the wiring in plastic – by pouring molten plastic into the space, and then letting that plastic solidify by cooling. This leads to the final form of the package-protected IC product that is then ready for sale as a component.

54. Saint also explains the “setback requirement,” which specifies a minimum distance between the chip and package pins:

Usually you will see *a setback requirement* keeping the chip away from the metal pins by a certain distance. Determine from the package the largest size allowable for the chip. (Saint, p. 214; emphasis added.)

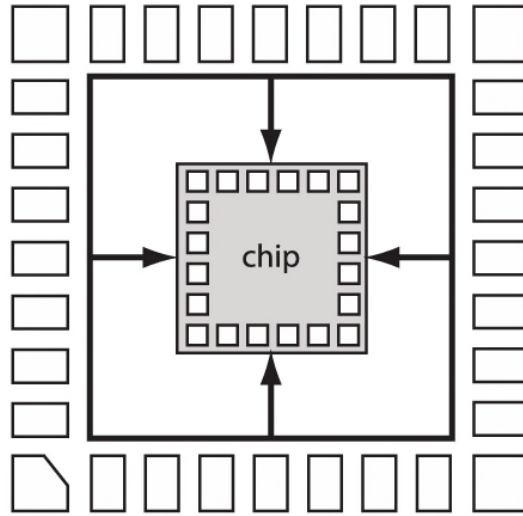
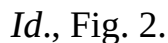


Figure 9–22. The maximum size of the chip is given by the dimensions of the package design.

Because the resistance of bonding wire is so low, this “setback” distance is not a problem for IC packaging.

55. While wire bonding in ICs frequently involves providing connections between IC bond pads and package traces, the use of wire bonding to provide direct pad-to-pad connections or direct package-trace-to-package-trace connections was also well-known in the art prior to 2018; as described in my opening Declaration, numerous references (such the Beauchamp reference, the Miller reference, and the Mathew reference) describe the use of bond wires (and wiring bonding technology) for this purpose. Because Patent Owner contests this assertion, I provide here some additional examples that confirm this common practice.

56. One such example is the Beddingfield reference (Ex. 1041), which is titled “Power Plane Design and Jumper Wire Bond for Voltage Drop Minimization.” Ex. 1041. The title speaks for itself. Beddingfield (which was filed in 2005)



57. Another example is the Lee reference (Ex, 1039). Lee Fig. 4 illustrates the use of jumper bondwires 206a and 206b to cross over (i.e., above) other circuit components. Ex. 1039, 2:61-3:5 (“The jumper may be a bondwire ... This form of construction is easy to manufacture and low in cost”).

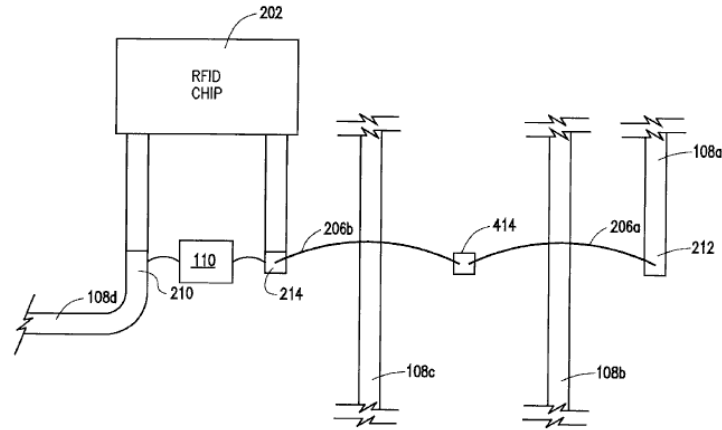


FIGURE 4

Id., Fig. 4.

58. A third example is the Conner reference (Ex. 1040). Conner Fig. 6 shows a jumper bondwire 9 that “bridges a number of signal traces 20” and provides “improved trace routing capability.” Ex. 1040, 3:37-59.

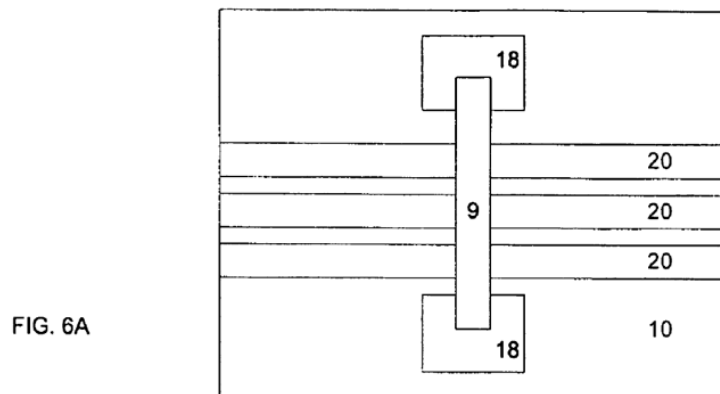


FIG. 6A

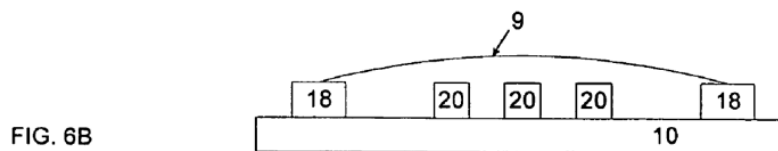


FIG. 6B

Id., Figs. 6A-6B.

59. Patent Owner's assertion that jumper bondwires were unknown or disfavored is totally unsupported – and is contradicted by all the evidence of record.

3. Patent Owner Makes Numerous Assertions About Basic Wire Bonding Technology That are Both Poorly-Sourced and Wrong

60. Unfortunately, Patent Owner seems to be unfamiliar with these basic aspects of wire bonding (as described above) as used in IC technology (and in manufacturing real, packaged IC products). Many of these knowledge-omissions were already addressed above; however, a few of them warrant further analysis.

a. Issue 1 (bond wire resistance)

61. Patent Owner asserts that there would be no motivation to use pad-to-pad wire bonding – claiming that the total bond wire resistance would be prohibitively high. POR, 34. Patent Owner faults Petitioner for citing Beauchamp [0027] which states that certain bond wire attachment techniques “create[] a low resistance connection between the bond pad 104 and the ball at the end of the bond wire 110.” Patent Owner contends that Petitioner ignored “the complete resistance in the connection between pads.” POR, 34. This is baseless.

62. If this assertion were actually correct, then wire bonding would be (and would always have been) an unacceptable technology – and would not have been able to be used in IC product packaging. However, this is demonstrably *not* the case – as wire bonding has long (for decades) been (and continues to be) a widely-used technology for providing external connections for IC products when the “bare” IC

is wired and packaged. On this count, Patent Owner has clearly misread the excerpt that they cited from Beauchamp (above); Beauchamp is describing how a low-resistance wire is bonded to a bond pad in a manner that has a low contact resistance between the bond wire and the bond pad – so that the entire path (i.e., bond wire and bond pad connection) is low-resistance.

63. Second, Patent Owner cites nothing to support the inference it wishes to draw – that bond wires have high resistance; as just explained above, this is completely incorrect – as they do not. Due to their relatively large diameter,¹⁰ bondwires typically have negligible resistance, as recognized in references like Beddingfield which states that “the resistance through the jumper wire 160 to the portion of the circuitry 200 may have a lower resistance than through the paths of

¹⁰ As noted above, this is apparent even to the naked eye - which can perceive bond wires in the microphotographs I discuss, but can hardly make out the individual metal traces on chip (let alone the individual transistors at that scale). When gold is used for the wire material, wires with a diameter of 10 μm are considered “ultra-fine” (see: <https://tanaka-preciousmetals.com/en/products/detail/bonding-wires/>; Tanaka is the world’s largest supplier of bonding wire), while wires with a diameter of 25 μm are regarded as being of a typical diameter (see: <https://www.venkel.com/technical/wire-bonding-recommendations-and-guidelines>). In cross-sectional area, these wire diameters are enormous in comparison to the cross-sectional areas of on-chip metal traces (which are both much narrower and much thinner); thus, bond wire resistance is clearly negligible.

circuitry 200.” Ex. 1041, [0014]-[0015]; *see also* Ex. 1038 (Khatri Tr.), 143:3-12 (“metallization [resistance] dominates”). Because bond wires are typically much larger in diameter than metal traces, bond wires have lower resistance than metal traces, so the voltage drop across bond wires is also lower. Ex. 1041, [0014]-[0015].

b. Issue 2 (pad identity)

64. Patent Owner makes an unsupported assertion that power-supply and ground pads are “fundamentally different.” That is simply not true – ground pads and power pads are typically identical to each other. While they may connect to different points on a circuit, the pads themselves are the same.

65. IC bond pads are designed to be (as required) consistent with the ground rules for the particular fabrication process in which an IC will be manufactured. The ground rules specify that a pad must be of at least a particular area in size (in order to be large enough to accommodate a bond wire connection, of the type discussed above), and the pad-to-pad separation must be no less than some minimum-allowed distance between any two adjacent pads. These ground rules are minimum-spacing requirements; there are usually no maximum pad-spacing requirements. The examples below from Saint show that the pads themselves are identical.

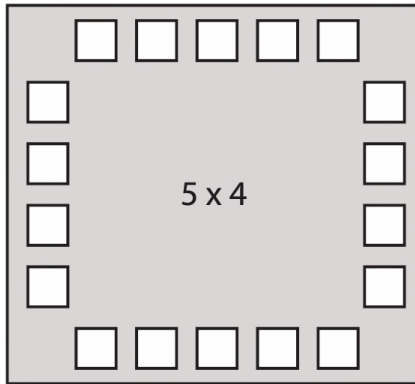


Figure 9-20. The minimum size of an 18-pad chip, based on the number of pads.

66. In the core-limited situation – where fewer pads are needed than the amount of space in the periphery would otherwise accommodate – there is more flexibility to spread pads out from each other, in order to achieve some particular objective. One example from Saint is provided in Figure 9-18 and Figure 9-19. But doing so changes nothing about the size, shape, or material of the pads. Patent Owner’s unsupported assertion that pads are “fundamentally different” with fixed assignments is directly contradicted by Saint.

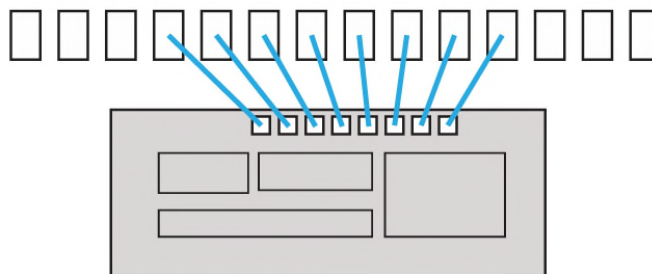


Figure 9-18. Crowded pad placement.

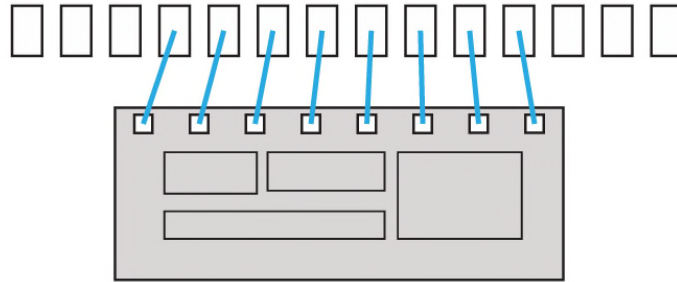
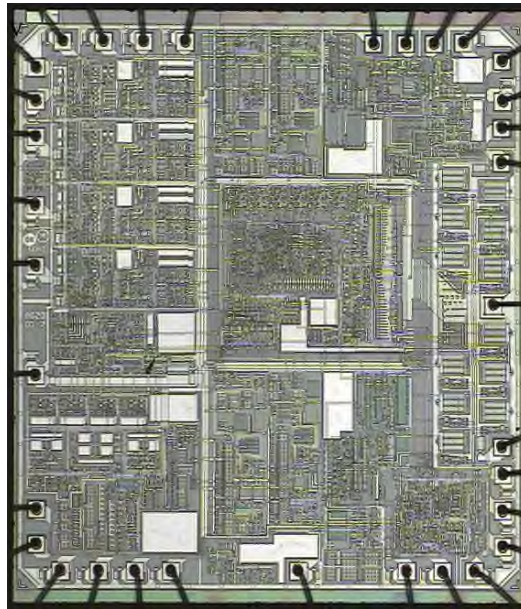


Figure 9-19. Improved pad spacing.

67. This flexibility in a core-limited case is also readily-observed in real product ICs – such as in the microphotograph already discussed.



It can readily be seen that all the pads in this IC are of the same size and shape. ***There is no way to tell just by examination of this microphotograph which pad (or pads) is a power-supply pad and/or which pad (or pads) is a ground pad.*** In general (as illustrated repeatedly in this discussion), pads are pads – and there is nothing unique about either the power-supply pads or the ground pads.

68. If Patent Owner’s concern is that ground pads could not be assigned as Petitioner (and I) proposed, that concern is not legitimate. As explained in §III.E.7.e, a designer has complete freedom at the start of a design to assign bond pads, and substantial freedom later on to assign (or re-assign) bond pads.

c. Issue 3 (inductance/noise and resistance)

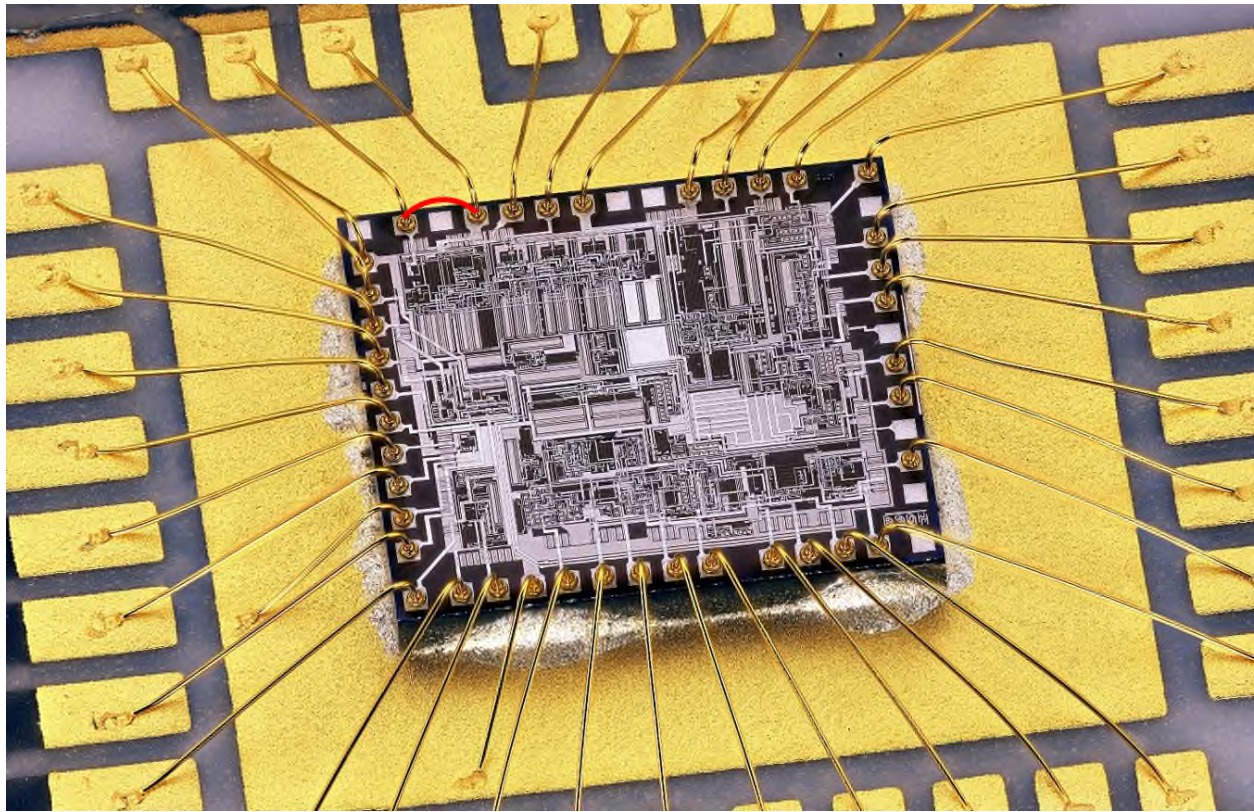
69. Patent Owner asserts that a POSITA would not have been motivated to use pad-to-pad “jumper” bond wires to connect two bond pads together – because such connections would suffer fatally from high resistance and excessive inductance. This assertion is easily shown to be incorrect.

70. First, if Patent Owner’s assertion were correct, once again it would mean that wire bonding is not (and never could have been) a viable technology for IC packaging; however, simple observation shows that this is not the case – as wire bonding is (and long has been) a very successful and very widely-used method in IC packaging. Patent Owner’s assertion also collapses because it would mean that ***Patent Owner’s own patent would be inoperable.***

71. Second, simple observation of actual IC products shows that Patent Owner is wrong. For example, the image below from the Petition¹¹ shows that bond wires connecting package pins to bond pads are far longer than a “jumper” bond

¹¹ https://en.wikipedia.org/wiki/Wire_bonding#/media/File:07R01.jpg

wire would be.¹²



An exemplary jumper bond wire (shown in red) was added to this figure for illustrative purposes. Given that the two pads are already connected to other signals, one would not actually connect these pads with a jumper bondwire (which was illustrated merely to show the relative length compared to other bondwires).

72. In summary, the length of a pad-to-pad jumper wire would be much less than the length of the wire connection between a pad and a package trace. Therefore, if Patent Owner's assertion that the pad-to-pad jumper wire would not

¹² As will be discussed below, this actual IC and its packaging is an instantiation of what Haralabidis describes in his (prior art) embodiment in his Figure 3.

work properly due to high resistance, excessive inductance/noise, droop/sag, and the other parade of horrors that Patent Owner speculates exists, then the wire connections between package traces and bond pads would suffer even more badly from these supposed problems. However, the longer wire runs between the package traces and the bond pads clearly provide acceptable performance in product ICs. Therefore, it is clear that the shorter-length pad-to-pad jumper wires would also provide acceptable performance.

73. Further, at his deposition, Dr. Khatri was explicitly asked why these problems (*e.g.*, high resistance and/or excessive inductance) would be problematic in pad-to-pad wire bonding – when they clearly had not been a general problem in wire bonding to that point; Dr. Khatri simply refused to answer the question. *See* Ex. 1038 (Khatri Tr.), 151:21-154:22.

74. Later in his deposition, Dr. Khatri was asked a similar question – and simply talked in circles without providing a substantive answer, eventually conceding “[t]hat’s not something I’ve studied.” Ex. 1038 (Khatri Tr.), 248:23-249:21. When asked again, he finally admitted that “conventional wisdom” about bond wire shortcomings no longer applied:

Q: How did the '164 Patent solve the noise problems that you mentioned earlier that are introduced by the use of bond wires?

A: ... But as an electrical engineer, we all know that, you know, circuit techniques and manufacturing techniques can improve over the years. And so it's completely not surprising to me that what was considered as, you know, in the conventional wisdom as a bad idea has been solved in multiple ways. And I could come up with some ways to solve it, you know as well as a person of, you know, of experience in this space.

Id., 253:21-255:6. This is consonant with the long-running and continuing suitability of wire bonding technology generally, for both pad-to-package and pad-to-pad connections; however, it should also be noted that Dr. Khatri's invocation of "conventional wisdom" is unsupported – and that, in fact, the prior art clearly shows that the "conventional wisdom" on this topic is the exact opposite of what Dr. Khatri said that it is.

75. Patent Owner "noise" argument (POR, 38) is further belied by its own expert – who used bondwires without problems in three chips he supervised at Texas A&M between 2010-2020. Ex. 1038 (Khatri Tr.), 104:9-105:6, 118:19-119:4, 120:12-121:2, 121:18-24, 132:8-16, 133:25-134:16. These chips spanned a breadth of technologies. *Id.*, 95:5-96:3, 97:16-23, 101:10-22, 102:13-24.

76. To recapitulate, in the Petitioner, Petitioner relies on Figure 1, Figure 2, and Figure 4 embodiments of Yoshinaga – all of which show the reference potential pads (5 and 6) connected directly to each other, without any intervening

circuitry. These embodiments do not include the bidirectional-diode circuitry that appears in Figure 3; it is clear that by **not** including this circuitry in Figures 1, 2, and 4, noise is not a problem in these embodiment – and thus bidirectional diode circuitry is not included. This is consistent with well-known IC design practice – since many ICs do not have noise problems that need to be protected against; that is, the magnitude of the noise is negligible, and does not warrant extra circuitry to protect against a problem that, effectively, does not exist. This is similar to how modest engine noise did not stop people from buying and using cars and aircraft, or how modes noise did not prevent AM radio, FM radio, or television from proliferating.

77. Patent Owner makes much of Miller’s statement that bondwires add inductance, and that “some level of signal distortion and attenuation is inevitable when signal frequencies are sufficiently high.” POR, 38 (citing Miller, [0007]); Ex. 2010, ¶87. But this only applies at “sufficiently high” frequencies, which is inapplicable to billions of chips.¹³ Additionally, Miller teaches “[t]he inductance of bond wires and package legs can be minimized by keeping them [] small” ([0007]), which is precisely what Petitioner’s proposed jumper bond wire does.

78. Dr. Khatri cites Ex. 2014 for the proposition that on-chip metal traces are “less inductive than bond wires.” Ex. 2010, ¶88. Putting aside that Ex. 2014

¹³ As will be discussed below, wire bonding has – and has long had – about an 80% “market share” among IC products.

predates the '164 patent by 15 years and ignores intervening wirebond technology improvements, Patent Owner's article explains that "[on-chip metal traces] are so tiny (i.e., have such a small cross-section) that the resistance of the connections, at modest operating speeds, overwhelms the effect of series inductance." Ex. 2014, 3. In other words, Patent Owner ignores the resistance/inductance trade-off between metal traces and bondwires. Ex. 1038 (Khatri Tr.), 131:6-8 (metallization has higher resistance than bondwires), 143:3-12, 180:18-24. Patent Owner erroneously presumes only inductance matters. Ex. 2014, 2 ("Practical transmission circuits always combine some amount of both resistance and inductance; they are never purely one or the other"). Especially when both inductance and resistance are considered, bondwires are a compelling option (as their commonplace use shows).

d. Issue 4 (pad-to-pad bondwires)

79. Further to these points, at his deposition, Dr. Khatri repeatedly asserted that the '164 patent's use of wiring bonding between pads (i.e., pad-to-pad) in an IC was inventive material:

[T]his patent is teaching something new and the inventive feature of the patent was to use bond wires to make the connections, you know, between pad groups. So that's the inventive feature. That's basically how it -- you know, how it was different from the conventional wisdom.

Ex. 1038 (Khatri Tr.), 228:5-13.

The big difference is that [pad-to-pad bond wire] is an inventive feature of the patent. This is a patent going against conventional wisdom and saying let's do things differently.

Id., 236:8-12.

But the point is that this is the inventive feature and this goes against conventional wisdom, you know, which before this patent was don't do this type of wire bond connection between bond pads and bond pads. But the '164 Patent specifically teaches doing that particularly in the case of, you know, of -- in an ESD context.

Id., 248:14-22; *see also id.*, 246:13-248:22, 251:22-23, 136:11-23 (similar). This assertion is flat-out wrong for the reasons discussed in my opening Declaration regarding Beachamp, Miller, and Mathew. Dr. Khatri's assertion also contradicts other prior art (such as Beddingfield, Conner, and Lee) discussed in §III.C.2.

80. Patent Owner attempts to disparage the jumper bond wire as introduced in Beauchamp and Miller as somehow being unworkable (and thus was something that a POSITA would not use) for several reasons, with an attempt to corroborate this assertion by referencing various items described in Saint; however, as demonstrated above, the "problems" Patent Owner identifies either don't exist at all or had at least been easily overcome by 2018.

81. Notably, the '164 patent introduced pad-to-pad wire bonding with **no** discussion of any prior problems with using wire bonding (either in general, or with respect to pad-to-pad bonding), **no** teachings regarding why pad-to-pad wire-bonding was “disfavored” prior to the '164 patent, and **no** teaching of any techniques to be used to overcome any alleged problems that had prevented pad-to-pad wire bonding from being used prior to the '164 patent.

82. Dr. Khatri’s repeated assertions that pad-to-pad wire bonding was inventive material in the '164 patent thus cannot be a correct assertion – since numerous prior art references disclose pad-to-pad wire bonding, and the '164 patent teaches nothing that states how the '164 patent overcomes earlier problems that caused pad-to-pad wire bonding to be non-viable. Dr. Khatri’s assertions are completely unsupported.

e. Issue 5 (bond wire length - “sag” and “droop”)

83. Patent Owner’s bond wire “sag” and “droop” arguments are easily dispelled. To begin, these purported “issues” are not discussed at all in the '164 patent. When asked why at deposition, Dr. Khatri admitted they weren’t real problem by 2018 when the '164 patent was filed.

Q: And so what does the '164 Patent teach to avoid the problems of sagging, drooping and short circuits that can be caused due to bond wires?

A So, you know, once again, right, these problems are conventional wisdom problems. And so in some -- you know, these problems might be something that once the inventors of this patent tried them out they realized or they were able to realize that they were not as, you know -- ***these conventional wisdom issues were not what they were, you know, what not were they were made out to be.*** And that could be one -- I mean, I'm sort of saying that that's something that they could have solved this technology issue. ***That's something that's completely possible because technology advances.*** ...

Q: How did the '164 Patent solve the problem of bond wire sagging and droop?

A. You know, once again, this -- you know, the problem of bond wire dragging and drooping was something that conventional wisdom thought was the situation. It's also possible that, you know, the technology of bond -- of applying -- sorry, of running bond wires in the meanwhile had gotten good enough that that conventional wisdom was not true anymore. I am -- you know, these are all sort of possibilities. I am not saying that one or the other is the actual situation. Because that's not what I've studied.

Ex. 1038 (Khatri Tr.), 246:13-248:22 (emphasis added); note again that Dr. Khatri's comments about "conventional wisdom" are unsupported ("I am -- you know, these are all sort of possibilities. I am not saying that one or the other is the actual situation.

Because that's not what I've studied”) – because, as noted above, the “conventional wisdom” was the exact opposite of what Dr. Khatri said that it was.

84. Next, Patent Owner seemingly does not understand the Saint reference – or the intent of the authors of this reference. The Saint book is a practical guide meant to improve the skills of IC layout designers – so that they apply good design techniques (rather than poor design techniques) to IC layout design.

85. Citing Saint Fig. 9-15, Patent Owner asserts that a POSITA reading Saint would be “discouraged” from using a “jumper” bond wire to make a pad-to-pad connection.

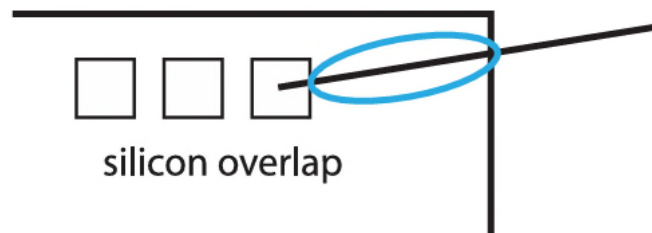


Figure 9–15. Don't overlap any more silicon than you have to.

[T]he bond wire could sag or droop, causing a short in the circuit. So, ***you have to keep the overlap of the bond wire over unused silicon as short as possible.***

Saint, p. 209 (emphasis added). But that is precisely what Petitioner (and myself) proposed doing by reassigning the ground pads to be located immediately adjacent

to Yoshinaga’s “saved area.” Thus, Saint actually supports the proposed combination, rather than teaching away from it.¹⁴

86. This is further confirmed by the rest of the content of Saint on this topic:

If you are using any of the wire bonding technologies, then you cannot have a pad in the middle of the chip. ***The wires would be too long.*** If you were to route a long bond wire from the center of the chip out to the metal pins, ***the wire could droop down and short to something in the circuit.*** So, most bonding manufacturers insist that wire bond pads be located at the outer edges only.

Saint, pp. 204-205 (emphasis added). This is nothing like the short jumper bond wires in the proposed prior art combinations.

87. The section in Saint titled “Wire Length” is intended to discourage the reader from using bond wire runs that are too long.

¹⁴ Patent Owner has missed the entire point of Saint’s book – which is to teach IC designers how to use good design practices rather than poor design practices; the “examples” which Patent Owner has cited from Saint are not intractable problems; rather, they describe poor design techniques which are simply overcome by using good design techniques.

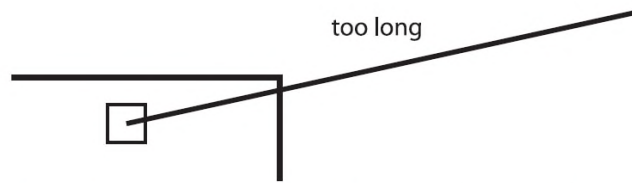


Figure 9-16. Keep your wires as short as you can. This stretch is probably not necessary. Plan your bond out before you begin your chip layout.

Saint, Figure 9-16. Again, this is nothing like Petitioner’s proposed combinations.

88. The Saint section titled “45 Degree Rule” is intended to discourage the reader from using bond wire runs that approach a target bond pad from an angle (relatively to the pad row in which the target pad is located) greater than 45 degrees. But Petitioner does not do this either.

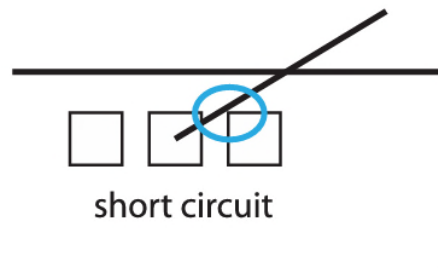
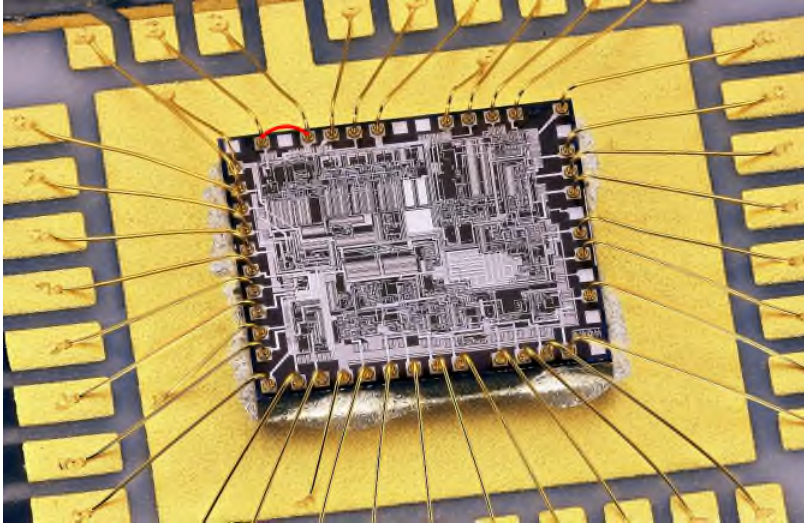


Figure 9-13. A little too close for comfort. A likely short.

89. It is clear that Patent Owner’s and Dr. Khatri’s assertions fail badly. Given that the pad-to-pin bondwires in the image below do not suffer from “droop” or “sagging,” the illustrative red jumper bondwire would be even less susceptible.



Exemplary jumper bond wire added to this figure, and illustrated in red.

90. Patent Owner says that Petitioner failed to explain how the jumper bondwire length is “minimal.” POR, 39. But the Petition explained that locating the ground pads immediately next to the saved area minimizes the bondwire length. Pet., 46-48. Given three opportunities to explain why bondwires would work well for connecting bond pads to package pins but would **not** work well for connecting two bond pads, Dr. Khatri had no substantive answer. Ex. 1038 (Khatri Tr.), 154:11-17, 140:15-147:12 (first chance, talking for 6-pages without answering the question), 147:13-151:20 (second chance), 151:21-154:10 (third chance).

91. This is a good place to note that what is shown above is basically the external ground bus architecture described in Haralabidis Figure 3. Three bond pads (on the top, bottom, and left edges) are connected to a common ground bus (in the package) that surrounds the chip.

D. Deep Submicron Wire Bonding

1. Patent Owner's Assertion That Integrated Circuits Manufactured Using a Deep Submicron Process Cannot Use Wire Bonding is Irrelevant, Mischaracterizes Their Own References, and is Demonstrably False.

92. Patent Owner asserts that wire bonding cannot be used for integrated circuits manufactured in a “deep submicron process”; the term “submicron process” is a term that refers to manufacturing processes where the minimum feature size (in terms of both the features created and the spacing between them) that can be successfully created (via photolithography) is less than one micron (where a “micron” is a “micrometer” – that is 1.0×10^{-6} meters) – while the term “deep submicron process” refers to a process with a much lower (but not precisely defined) minimum geometry size. However, this assertion fails badly for multiple reasons.

a. Relevance

93. First, even if one accepts that this assertion is correct (which it is not), it has no relevance. Neither the '164 patent nor any of the art cited by Petitioner restricts its teachings based on the lithographic-size limits of a particular silicon IC manufacturing process; in particular, the claims of the '164 patent do not mention such geometric considerations at all. Further, this is a strange assertion for Patent Owner to make – since it implies that the teachings of the '164 patent (which was filed in 2018) are inapplicable to silicon manufacturing technologies both of that time *and* of many prior years; this would imply that the '164 patent cannot be

practiced under such a restriction.

94. While (as mentioned above) the geometric limit that separates “submicron” from “deep submicron” does not have (and never has had) a specific definition, it can be noted that minimum-feature-size manufacturing processes such as 0.25 μm (250 nm), 0.18 μm (180 nm), 0.13 μm (130 nm), and 0.09 μm (90 nm) have long been regarded as being “deep submicron” minimum-feature-size dimensions.¹⁵ Further, even minimum-feature-size manufacturing processes such as 0.35 μm (350 nm) are often regarded as representing a “deep submicron process” – as will be demonstrated by example below.

95. As a temporal reference point, silicon fabrication processes using minimum feature sizes of 0.25 μm were widely implemented by 1998, and the other three minimum-feature-size processes mentioned above were implemented rapidly over the next few years (as will be demonstrated conclusively below).

96. Thus, if wire bonding could not be used in “deep submicron technology” (as Patent Owner asserts), then the ’164 patent at the time of its filing would have only been applicable to much older manufacturing processes (predating the filing of the application that led to the ’164 patent by at least 20 years). If this were indeed the case (and it is not), then there would have been little reason to file

¹⁵ See, e.g., <https://siliconvlsi.com/deep-sub-micron/>.

the patent application in the first place.

b. Patent Owner's "Deep Submicron" Assertion is Contradicted by Patent Owner's Own References

97. Patent Owner's assertion is contradicted by its own references – as would have been clear if Patent Owner had bothered to carry out any due diligence that went further than simply quoting a single sentence in a single reference source. Patent Owner's assertion that wire bonding was "disfavored" is based on a single sentence from a single reference (Davis¹⁶) that in fact refers to the Sylvester reference. Even a cursory examination of either reference clearly shows that the statement applies only to a single category of IC product parts (large microprocessor ICs) and is not a general statement. Both Patent Owner and Dr. Khatri are simply wrong in this assertion – as their own references make clear.

98. The sentence in question comes from a 2003 compendium book (Ex. 2012)¹⁷; this book is a "compendium" in that various authors contributed various chapters (a total of 10 of them). The chapter in question here is Chapter 5 – which

¹⁶ Herein, I call this reference "Davis" simply because Patent Owner has so-described this reference; however, as will be explained below, "Davis" is a compendium book (with Davis being mainly the editor) – while the material that Patent Owner cited in the POR was actually taken from a chapter authored by (and contributed by) Zarkesh-Ha.

¹⁷ *Interconnect Technology and Design for Gigascale Integration* (ed. by J. Davis and J. Meindl), Springer, 2003.

is entitled “Power, Clock, and Global Signal Distribution.”

99. The sentence in question (on Ex. 2012, p. 49) states that:

Because of severe IR-drop and switching noise problems, it has been shown that conventional wire-bonding technology, which constrains the power pads to be located at the chip periphery, is not a scalable concept for deep submicron technology [24].

This sentence is the entire basis for Patent Owner’s assertion regarding the alleged unsuitability of wire bonding for deep submicron technology; however, it is easily demonstrated that the disembodied quotation of this sentence actually is mischaracterizing the situation with wire bonding and deep submicron technology (and, as will be explained below, is also mischaracterizing the 2003 reference from which this sentence was drawn) – something that becomes obvious when the Sylvester reference (Ex. 1037) that the author of this 2003 sentence has cited (as [24]) is reviewed.¹⁸

100. Sylvester is a conference paper published in 1999. Contrary to Patent Owner’s implication, this paper does **not** provide a broad conclusion that applies to

¹⁸ Dr. Khatri was shown the Sylvester reference at his deposition – and testified that he did not review this reference when preparing his declaration. Ex. 1038 (Khatri Tr.), 261:4-6. This is despite the fact that the single sentence that both Patent Owner and Dr. Khatri cite from Davis cites as **its** source the Sylvester reference.

any-and-all IC products that are manufactured using “deep submicron technology.”

Rather, the authors of that 1999 paper state clearly (repeatedly) that their study applies only to large-scale, leading-edge microprocessor ICs:

Specifically, *this work focuses on microprocessors* as these designs achieve the highest performance and will meet the limitations of global interconnect first. ... To demonstrate, a representative back-end process for 50-nm *microprocessors* is suggested.

Ex. 1037 (Sylvester), p. 1.

With rising power consumption yet dropping V_{dd} values, the supply current in future *microprocessors* will increase quickly.

Id., p. 7.

In this study we used a comprehensive analysis of routing resources in a 50-nm *microprocessor* to determine whether the fat wiring scheme (with $P = 2 \mu m$) is feasible.

Id., p. 8.

101. This clarifies that the sentence that Patent Owner has cited from Davis has been mischaracterized by Patent Owner; what the cited Sylvester study involved was **not** a general analysis of deep submicron technology; rather, it is a narrower study confined to microprocessor ICs. A microprocessor is indeed (as Sylvester states) a large-and-complex IC that will likely be the first to run into any limitations

that are concomitant with their inherent size (in terms of both the literal areal size *and* the number of transistors in the IC); however (and as will demonstrated below), there is a vast universe of integrated circuits which are *not* microprocessors – and it can also thus be concluded (by implication from Sylvester) that less-complex ICs will not run into the kinds of difficulties that Sylvester describes in his study. In fact, Sylvester’s main objection to the use of wire bonding in deep-submicron microprocessors is not that there is something inherent in the process technology in which they were manufactured that prevents the use of wire bonding at all; rather, Sylvester’s conclusion is that with bond pads confined to the periphery of a large (e.g., microprocessor) IC, the long (on-chip) metal lines required to provide power supply connections to circuitry in the middle of the microprocessor IC will encounter problems (such as IR drop and excessive parasitic inductance) that may degrade the speed of that microprocessor. Sylvester recommends that future microprocessors use connection techniques (such as “flip chip”) to avoid these problems.

102. Further, the very title of the chapter (“Power, Clock, and Global Signal Distribution”) clearly refers to functionalities that must be implemented in large, complex integrated circuits (such as microprocessors) – rather than generally or universally across the broader landscape of integrated circuit products.

103. Thus, it can readily be seen that Patent Owner has cherry-picked a single sentence from Davis – with the intent of trying to pass this single sentence off

as providing a generalized conclusion that it does not in fact provide.

104. This is further confirmed via examination of a 2010 conference paper (Charles, Ex. 1043) which notes that even in 2010 (when deep-submicron ICs had long become the overwhelming norm in IC production), flip-chip bonding was a relatively small percentage of the packaging technology that was being used for ICs:

This increased density coupled with ease of repair and high frequency performance has allowed flip chipping to become the second major form of first level interconnect (despite its cost and lack of flexibility) with over a 15% market share [4].

Ex. 1043, p. 2. The cited reference [4] was published in 2008.

105. Thus, Charles further confirms that wire bonding is quite viable for “deep-submicron technology” – and that even in 2008/2010, wire bonding was the dominant (80%) method that was used in product IC packages.

106. To summarize, both Patent Owner and Dr. Khatri have mischaracterized Davis for the purpose of asserting a conclusion that neither Davis (2003) nor its subsidiary reference (Sylvester, 1999) provides; in addition, Charles (2010) provides further confirmation of this mischaracterization by Patent Owner and Dr. Khatri – and further shows that wire bonding has long been the dominant package-connection method in use for IC products.

**c. Many Deep Submicron IC Products Use Wire Bonding –
As Is Well-Known in the Art**

107. Many examples further show that Patent Owner’s “deep submicron” argument is unfounded. Confirmation can readily be found in the patent art. For example, U.S. Patent No. 6,110,816 (Ex. 1044) – the application of which was filed in 1999, with the patent issued in 2000 (to TSMC) – is entitled “Method for Improving Bondability for **Deep-Submicron Integrated Circuit Package.**” (emphasis added.) While the title of this (prior-art) patent speaks for itself, examination of the specification provides additional confirming details. For example, the patentee states that:

In accordance with the present invention, a method for forming a top metal layer to improve interconnect bondability for deep-submicron integrated circuit packages is provided.

Ex. 1044, 2:48-51. Also:

A semiconductor integrated circuit structure includes a semiconductor substrate with **deep-submicron electronic elements formed therein.**

Id., 2:52-54 (emphasis added). This sentence is sufficient to override any doubt that the “deep-submicron” of this patent is referring to the size of features that are formed in the silicon IC during manufacturing.

108. Finally, the patentee even states (in the Abstract) what is meant (in their view) by “deep-submicron” feature sizes:

The textured cavities increase the surface area of the bond pads and provide improved bondability for the **0.35 and 0.3 um IC devices**.

Id., Abstract (emphasis added).

109. Thus, this issued patent further confirms that wire bonding has long been widely used in “deep-submicron” silicon manufacturing processes – and that Patent Owner’s assertion to the contrary is simply incorrect.

110. Further, a more recent (2023) article¹⁹ describes how wire bonding technology has been improved and extended – so that it is still used today:

The Underdog That Refuses to Die:

If you think wire bonding is dead, you’re missing one of the biggest revolutions in semiconductor packaging. For decades, industry experts have predicted that Flip-Chip and Through-Silicon Vias (TSV) would render wire bonding obsolete. As semiconductor devices pushed towards higher density and performance, the conventional wisdom was clear: wire bonding—once the workhorse of chip interconnects—was too slow, too bulky and too

¹⁹ <https://www.mckinsey-electronics.com/post/the-silent-revolution-how-ultra-precise-wire-bonding-is-reshaping-semiconductor-packaging>.

limited for the future.

Yet, something unexpected has happened. Rather than fading into obsolescence, wire bonding is experiencing a technological renaissance. Semiconductor giants are re-investing heavily in ultra-precise wire bonding techniques, leveraging its cost advantages, flexibility and newfound precision to compete with modern interconnect technologies. ...

Where Wire Bonding Still Wins: Despite Flip-Chip and TSV advancements, wire bonding remains the preferred choice for:

- Automotive electronics (*long-term reliability*)
- MEMS and RF modules (cost-sensitive and performance-balanced)
- Aerospace and military applications (*proven durability*)

With ultra-precise bonding techniques, wire bonding is proving to be a formidable contender in semiconductor packaging. (emphases added.)

These excerpts speak for themselves regarding the use of wire bonding in deep submicron processes to this day – and in the future, as wire bonding is an ongoing subject in research and innovation.

111. In that vein, final confirmation of all of the above is provided by a paper published in 2023²⁰ (Ex. 1045, “Zhou”) – which provides an overview of wire bonding technology, its history, and its continued use in even present-day integrated circuits. As the Abstract of Zhou states,

Wire bonding is still the most popular chip interconnect technology in microelectronic packaging and will not be replaced by other interconnect methods for a long time in the future.

Further, as the Introduction to Zhou begins,

Wire bonding has been the most cost-effective, mature, and flexible interconnect technology in microelectronic packaging since its invention in the 1960s, which is still used to assemble more than 80% semiconductor packages in the microelectronic packaging industry [7,8].
(emphasis added.)

It is particularly notable that the 80% “market share” number above is identical to that cited in the Charles reference (which was published in 2010 and cites a publication from 2008 for that number) – while in the case of Zhou, the two references cited ([7] and [8]) were published in (respectively) 2015 and 2020. This indicates that not only was wire bonding viable for “deep-submicron technology” in

²⁰ H. Zhou et al., “Research Progress on Bonding Wire for Microelectronic Packaging,” *Micromachines* vol. 14, pp. 232 – 255 (2023).

years gone by; wire bonding is **still** the overwhelming “market share” winner in contemporary integrated circuit packaging (and has retained that “market share” number for at least the past 15 years).

E. Ground and Power Distribution Networks

1. Patent Owner Does Not Understand the Nature of Either Ground Networks or Power-Distribution Network – Nor Their Importance to this Matter

112. In its POR, Patent Owner demonstrates that it does not understand the concept of “ground” in electronic circuits – with that non-understanding encompassing both a general failure of basic understanding **and** a failure to understand the importance of this concept to (and its usage in) the circuitry at issue in this matter; this is particularly notable, as ground buses are used as ESD buses in circuitry (including in circuitry at the heart of this matter). Further, Patent Owner demonstrates that it does not understand the nature of power-distribution networks in integrated circuits – which are also used as ESD buses in circuitry.

113. Therefore, an overview of these concepts will be provided here to clarify Patent Owner’s misconceptions– after which some examples of Patent Owner’s misunderstandings (which lead Patent Owner to incorrect assertions and incorrect conclusions) will be considered.

2. “Ground” is Typically the Electrical Potential of the Earth

114. The need for a universal reference of some sort is not unique to electrical engineering. For example, the same problem arises when trying to specify the elevation of a location somewhere on the Earth. This is addressed by providing a “zero”-value reference against which all elevations can be referenced – so that a single number can be provided when referring to “elevation.” The zero-value reference is provided by mean sea level (MSL) – which is defined²¹ as:

Mean Sea Level is defined as the average height of the sea surface over a specific period, typically 19 years for global averages or shorter periods for regional or local scales. This value represents the equilibrium level of the sea surface, unaffected by tidal fluctuations.

Thus, an “elevation” of (say) 4000 feet means that the location in question is 4000 above the elevation of mean sea level. MSL is put to the same use in aviation – where the “altitude” of an aircraft is given relative to mean sea level – rather than the altitude above ground level (AGL).²²

²¹ https://blog.truegeometry.com/tutorials/education/7ed685786bdb995ea685cdc68d86e2d5/JSON_TO_ARTCL_What_is_Mean_Sea_Level_MSL_in_context_of_how_do_you_calculate_t.html ; see also, <https://www.wordnik.com/words/mean%20sea%20level>.

²² Photograph by the author, taken while flying eastward over the upper peninsula of Michigan, 12 June 2025.



(annotations added.) The altimeter setting indicates that the aircraft is 13,000 feet above mean sea level (MSL).

115. In the same way, “ground” voltage (*i.e.*, the electric potential of the earth) provides a zero-value point against which to measure the “voltage” of other objects. In a way that is similar to what is done with elevation/altitude, this reference is also provided by the Earth itself.

116. Just as mean sea level (MSL) is very stable with time, in the same way (and because the Earth is so large) the total charge on the Earth is very stable with time. This allows the charge state of the Earth to provide a zero-value reference for charge – against which the charge on any object can be referenced. The Earth thus provides the charge level that defines “0V” – and thus provides the universal

reference for voltage.

3. In Electronic Circuits, the Term “Ground” Has Broader Meaning and the Cited Art Teaches (and Renders Obvious) a Common Ground

117. Thus, at the level of first-principles, “ground” has a rather specific definition. However, in the practices associated with electronic circuits (such as integrated circuits), “ground” has broader meaning – as well-explained in the glossary provide in Saint:

ground—The lowest voltage potential in any circuit. To be grounded means to be connected to the ground voltage.
Saint, p. 438.

This is consistent with basic circuit physiology – where the high voltage potential (VDD or VCC) provides the source of current (and also, as discussed below, provides the input of energy/power to the circuitry so that that the circuitry can actually function), while the low voltage potential (ground) provides the sink of current; this is conceptually similar to household plumbing – where all water in a house eventually drains to the same sewer pipe.

118. Further, “ground” is sometimes used interchangeably with “VSS” – which Saint defines as:

VSS—A signal name for the most negative voltage in your circuit, usually used in digital circuitry.

Saint, p. 451. These two definitions are effectively identical for purposes of this proceeding. By definition, there can only be one “most negative voltage” in a circuit.

119. In my opening Declaration, I explained that it is common engineering practice for ICs to have multiple ground connections. However, this is **not** because each “ground voltage” is different; rather, it is common (as will be further explained below) to have multiple ground connections (to the same ground voltage) to improve the noise resistance and signal integrity. Indeed, using a common/shared ground is more than **a** common engineering practice, it is **the most common** engineering practice vis-à-vis ground signals. To assert otherwise runs counter to long-standing engineering practices.

120. In fact, note that Saint’s definition of “ground” (presented above) actually states that a single ground voltage exists (“To be grounded means to be connected to **the** ground voltage”). Saint, 438 (emphasis added).

121. The Patent Owner’s main reason for saying that Saint Figure 7-7 has “three separate and distinct” ground voltages is that Saint refers to “GND1, “GND2,” and “GND3.” POR, 60-62. But Saint shows otherwise in Figure 6.2 – where there are two ground signals (GND1 and GND2), but both are connected (via contacts) to the substrate of the IC:

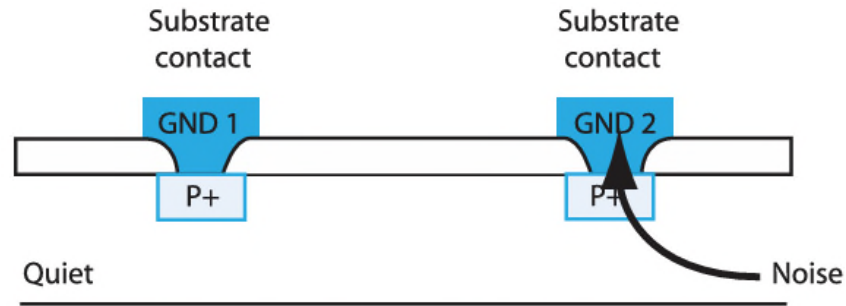


Figure 6–2. *Placing some slippery exits in the way helps eliminate traveling noise.*

Here, it can be seen that although GND1 and GND are separate ground connection buses for connection to circuitry, they are connected together by connecting them to the substrate – which clearly means that they both will have the same voltage as each other at all times.

122. An engineer would readily understand that Figure 7-7’s GND1, GND2, and GND3 labels simply reflect that they are associated with the respective VCC1, VCC2, and VCC3 power domains (which may or may not have different voltages). But even when different power domains have different supply voltages (e.g., VCC1=3V, VCC2=5V, etc.), that in no way means the reference/ground voltages are different. To the contrary, as Saint Figure 6-2 shows, GND1, GND2, etc. are the same. Both Haralabidis and Yoshinaga reinforce this common engineering principle. For example, Haralabidis has “respective ground connections VSS1, VSS2, VSSN,” which are analogous to Saint’s GND1, GND2, GND3. Haralibidis, 5:42-6:2. Haralabidis explains that “each ground connection VSS1, VSS2, VSSN is connected to ... the PC board common ground rail 670.” *Id.* In a similar fashion,

Yoshinaga labels the same ground reference lines with different numbers (e.g., 19, 20, 60) based on which power domain they correspond to. Yoshinaga, Figure 6, [0088]. But the differently-numbered ground rails all connect to the same ground, as shown in, e.g., Figure 1.

123. In short, Patent Owner's naming convention arguments fails, and a POSITA would have understood (or at least would have found it obvious) that Saint's GND1, GND2, and GND3 connect to each other.

124. Patent Owner's contrary assertion is like saying that the shower and sink drains in a house do not connect before going outside. While such an approach is possible, it is rarely used. By far, the more common (and obvious) approach is to connect the drain pipes inside instead of running separate lines to the street. Likewise, the far more common (and obvious) approach in the electrical engineering context is to connect ground buses on (or near) the chip. At a minimum, it would have been obvious for GND1, GND2, and GND3 to unite per common engineering practice. This is exactly what Saint's Case Study 1 (and Haralabidis, and Saint elsewhere) disclose – as shown in the figure below from Saint.

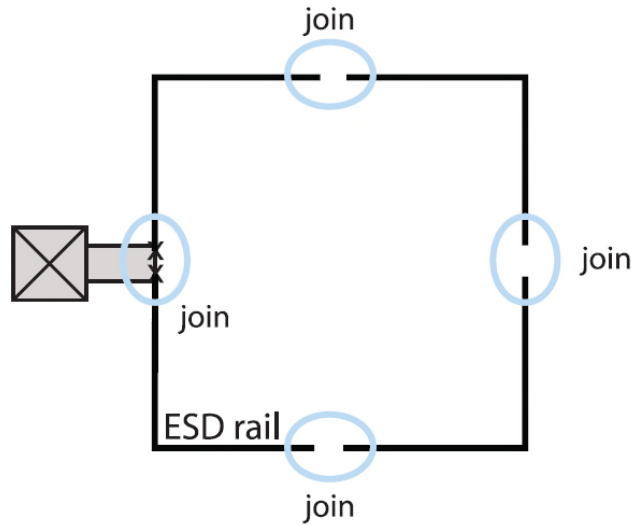


Figure CS1-87. ESD ground wiring connections.

125. Far from representing an “incompatible teaching” (POR, 62-63) vis-à-vis Figure 7-7, Saint’s Case Study 1 supports that there is a common ground point. Just like Saint’s Figure 7-7, Case Study 1 discloses multiple power domains (e.g., VCC1, VCC2, etc.), and expressly discloses “join[ing]” the corresponding ground buses. Saint, Figure CS1-1, CS1-87 (shown above). The Patent Owner fundamentally misunderstands the nature of Figure 7-7 (which is a conceptual illustration intended to illustrate the idea of grouping signals by power domain) and Case Study 1 (which is an actual layout/implementation). The fact that the two figures are intended to illustrate different aspects of a design (and thus are presented at different levels of abstraction), does not make them “incompatible.” Just the opposite, the two are mutually compatible – with Case Study 1 providing additional detail on how segmented power domains are implemented in real life.

126. Saint Figure CS1-1 shows segmented power domains (VCC1/VCC2/VCC3/VCC4) and CS1-99 shows a “continuous [ground] ring.” This is analogous to Saint Figure 7-7, which shows separate power domains (VCC1/VCC2/VCC3), but does not concern itself with where or how the ground buses connect. Far from showing an “incompatib[ility]” as Patent Owner suggests (POR, 62), Saint Case Study 1 demonstrates that a common ground *is compatible* with segmented power domains, including a reasonable expectation of success. In addition to being the most common approach, a POSITA would have been motivated to use a common ground to avoid the extra circuitry required to maintain three independent “ground” voltages – much as a builder would avoid running separate sewer pipes to the street for every drain in a house.

127. Patent Owner’s assertion that “Saint teaches ... GND1, GND2, and GND3 should remain unconnected to [] prevent noise and maintain ESD protection” is a flat-out mischaracterization. POR, 61. Saint says no such thing. Saint teaches that power domain grouping “makes the chip smaller ... and keeps cross talk down.” Saint, p. 162. This is because doing so avoids long, parallel wire runs which would otherwise be susceptible to cross-talk (i.e., noise). *Id.*

128. Patent Owner’s assertion that a bondwire and common ground rail would increase “die size and cost” (POR, 64) fails – because Haralabidis’ common ESD bus is located off-chip. Haralabidis, Figure 3, Figure 5. Thus, die size is

unchanged, and Patent Owner's expert admitted bondwires are inexpensive. Ex. 1038 (Khatri Tr.), 132:8-16. Patent Owner also makes a false comparison. While it is true that a shared drain pipe (analogous to a common ground bus) costs something, the cost is much less compared to the alternative of running multiple different drain pipes to the street (akin to Patent Owner's proposal of maintaining multiple independent ground paths). Patent Owner tacitly admits as much by qualifying that its assertion is only true "without removal of other components." POR, 64. The "other components" that would be removed are all the bond wires, wire traces, etc. necessary for maintaining multiple, isolated ground paths.

4. Where the Ground Voltages Connect is a Design Choice

129. As can be seen, it is common practice for different ground connections to have a common voltage – so that in this situation, it is common practice to connect those disparate ground connections together – always in a manner that is consistent with the simple physics-based requirement of reference against some explicit Earth ground; this is required to provide a reference voltage point for all voltages in the circuitry.²³ The particular implementation is a design choice – based on the specific situations of an IC design; Saint actually provides two very good examples that show two possible ways to deal with this issue.

²³ In mobile devices, a "ground" reference is provided by a suitably-designed "chassis ground," so as to provide the equivalent.

130. “Case Study 1” describes the design situation for an IC that consists of four operational amplifiers (“opamps”). In the initial design, each opamp has its own independent ground connection and ground wiring; however, based on the above, it is well-known and advantageous to connect all of these independent ground connections together into a single ground connection. Doing so on-chip allows all four ground connections to be unified together at a single pad. In fact, this is exactly what Saint depicts in the study:

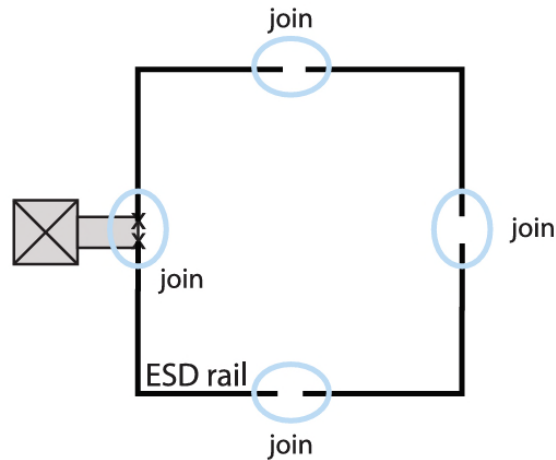


Figure CS1-87. ESD ground wiring connections.

As this figure shows, in the design process these four ground buses are unified together – and connected to a single pad.

131. This is entirely compatible with Figure 7-7, which merely shows the ground buses at the “chip” level before they have been connected (either on-chip as Case Study 1 describes, or off-chip as Haralabidis describes).

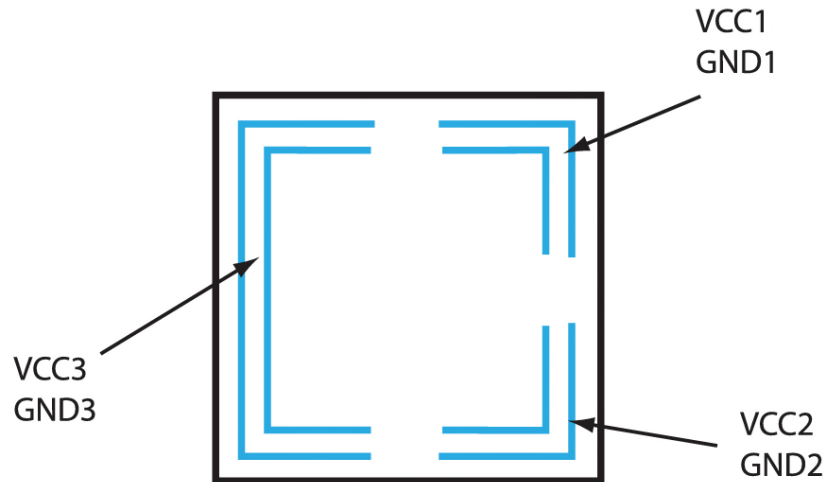


Figure 7-7. Pin-out simplification showing like protects grouped together.

132. Both Patent Owner and Dr. Khatri assert that the GND1, GND2, and GND3 must have separate and distinct voltages. At his deposition, Dr. Khatri was asked a simple question regarding this assertion:

Q. Where in the Saint reference does it say that ground 1, ground 2 and ground 3 are separate and distinct voltages?

Ex. 1038 (Khatri Tr.), 347:19-348:4. In response, Dr. Khatri talks in circles at length (348:5-350:14), but ultimately could not point to anything in Saint that supports his baseless assertion that GND1, GND2, and GND3 have **separate voltages**.

133. There is simply no indication from Saint that different “ground” voltages are used – and Haralabidis describes the various scenarios involving a single ground voltage being separated into different ground connections – with the precise unification architecture used being a design choice.

134. As a final point, Dr. Khatri also asserts that “ground 1, ground 2, ground 3 ... are separate and distinct electrically with separate and distinct voltages and it would be a fundamental error to connect them as Dr. Foty suggests.” Ex. 1038 (Khatri Tr.), 347:9-14. Dr. Khatri seems to not understand that ground unification is not a “suggestion” from me – but rather common practice in the art, as also described by both Saint and (in particular) Haralabidis.

5. Power Distribution Networks

135. Power distribution networks are designed to supply current (and thus power) to integrated circuits; further, power distributions networks source charge to the circuitry – while ground networks sink that charge.

136. Power supply voltage connections in IC design are usually represented with the label of either VCC or VDD; as was the situation with GND and VSS (described above), the power supply voltages (VCC and VDD) are defined (in the same way) to reflect their usage in electronic circuits. Again citing Saint’s glossary,

VCC—A signal name for the most positive voltage in your circuit, usually used in analog circuitry.

VDD—A signal name for the most positive voltage in your circuit, usually used in digital circuitry.

Saint, p. 450. These two definitions are essentially identical – with the only difference being cosmetic.

137. Returning to Saint Figure 7-7 (and the associated discussion), in this situation Saint has three different power supply voltage connections – VCC1, VCC2, and VCC3; Saint describes how the circuit blocks are arranged in the floorplan so that each particular power supply voltage connection is closest to the circuit blocks to which it will be supplying power:

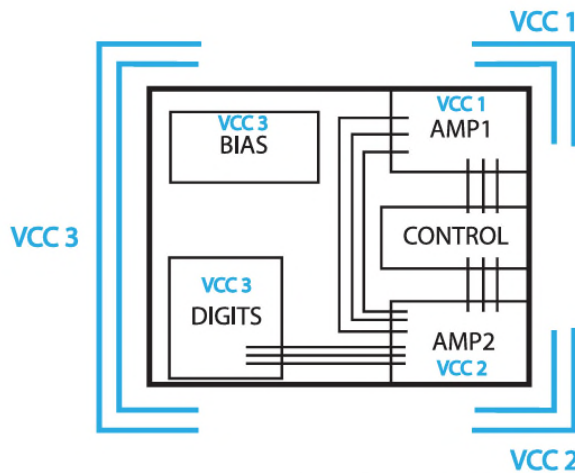


Figure 7-11. Rearranged blocks now align with our premiere pin-out plan.

Each VCC (and its companion GND) and the circuit block(s) to be connected to it (them) are placed in close proximity to each other – in order to simplify the wiring, and also to reduce the length of the wires running from VCC and GND to each block.

138. Importantly, Figure 7-11 shows signals/communication between the “DIGITS” block (in the VCC3 power domain) and “AMP2” (in the VCC2 power domain). A POSITA would readily understand that communication between these two blocks would in practice be extremely complicated if their respective ground voltages (GND2 and GND3) were not the same – as this would undermine the ability

to define VCC1, VCC2, and VCC3 against a common reference voltage (and thus against each other). For example, if GND2 and GND3 differed by 10 volts and AMP2 sent a signal that it thought was 5V to DIGITS, the DIGITS block would not receive a 5V signal, but would instead receive a 15V signal due relative to GND3. This is a dreadful design practice – and could lead to all sort of problems, such as communication issues and circuit malfunctions.

139. In the same way, to return to aviation, if three different locations defined “zero altitude” using three different references (instead of the single universal MSL reference that is actually used), it would be impossible for air traffic controllers to assign an aircraft to a particular (referenced-to-MSL) altitude – or for a pilot to understand what “altitude” (referenced to... what exactly?) his aircraft is actually at. In both electronic circuits *and* aviation, the need for (and use of) a common “zero” reference is fundamental to the art.

6. Patent Owner Misunderstands and/or Misinterprets Several Important Aspects of This Topic

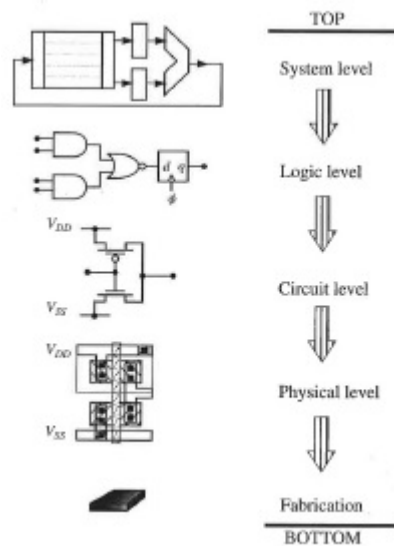
140. As noted at the outset of this section, there are many aspects of this topic that Patent Owner either misunderstands or misinterprets; some of these have already been clarified above – but a few of these issues remain to be addressed.

a. Issue 1 (Yoshinaga Figures 1, 2, and 4 are Topological)

141. Patent Owner asserts that Figure 1, Figure 2, and Figure 4 of Yoshinaga show that the reference potential (i.e., VSS/GND) pads 5 and 6 are connected to each

other using an on-chip “metal trace” (which Patent Owner calls “metallization”); however, this is not correct - as Patent Owner seems to not understand the basic nature of these figures in Yoshinaga.

142. As I explained in my opening Declaration, Figures 1 – 4 of Yoshinaga are what are known as “topological descriptions” (rather than “physical descriptions” of circuitry); this level of design is circuit level, where what is shown are the components of the circuit and the connections between them – but no details on how those connections are made or implemented are provided.²⁴



As can be seen from this depiction of the IC design and development process, the circuit components and connections between them are described – but no implementation details are provided; those details come at the physical design level;

²⁴ J. Uyemura, *Chip Design for Deep Submicron VLSI*, Thomson, 2006, p. 19.

indeed, that is the purpose of the physical design stage. In this vein, Yoshinaga describes the connections (19 and 20) between pad 5 and pad 6 as simply a “reference potential line” – with no details about how this connection is made.

143. In contrast, Figure 6 of Yoshinaga provides some physical implementation details (but is not intended as a complete implementation as no information about the chip’s intended function is provided). Tellingly, even though Figure 6 shows the ground buses (typically implemented in the top metal layer), it does **not** show a metal trace connecting the reference voltage (i.e., VSS/GND) buses together. If Yoshinaga intended to connect the ground buses with a metal trace, a POSITA would expect to see a top-level metal trace in Figure 6 – since the ground buses themselves are shown. Yoshinaga is thus silent on the specific method that is used to connect these buses together.

144. It also bears noting that there are a limited number of options that could be deployed to connect the ground buses. Possible options include simply extending the bus lines to unify them into a continuous ring around the periphery of the entire IC (such as Saint does with the ground bus in his Case Study 1), using “jumper” bond wires to connect two pads together (as per the several prior art references cited above), or connecting the ground buses together off-chip (in the two possible manners described by Haralabidis). No other viable options exist. The specific option to be used would, as described above, be a choice based on the chip design

(*e.g.*, all digital design, all analog design, or mixed-signal design).

b. Issue 2 (Yoshinaga Figure 6 Has Ground Pads)

145. Patent Owner asserts that Yoshinaga Figure 6 does not show the presence of reference voltage (i.e., VSS/GND) pads, and that they do not exist and cannot be present. POR, 22. This assertion is incorrect.

146. A POSITA would have understood that ground pads are present and illustrated in Figure 6, just not labeled. To begin, ground pads 5 and 6 are expressly shown and labeled in Yoshinaga Figure 1 (and Figures 2 and 4). Yoshinaga, Figure 1, [0055]. Patent Owner ignores that Figure 6 is an implementation of Figure 1, and thus must have ground pads. *Id.*, [0087] (Figure 6 is “semiconductor [IC] of FIG. 1.”). Even Dr. Khatri acknowledged this point. Ex. 1038 (Khatri Tr.), 298:16-299:2, 213:21-214:9, 195:20-196:8.

147. Patent Owner’s position is based on an incorrect, super-literal reading of Yoshinaga [0078] – which is divorced from the context of the surrounding paragraphs and Figure 6. After Yoshinaga describes power pads 3, 4, and 58 (which are all labelled in Figure 6) and their corresponding reference lines 17, 18 and 59 (Yoshinaga, [0076]-[0077]), Yoshinaga states that the associated “[r]eference potential pads are not shown to simplify the drawing” (*id.*, [0078]). Taking into account that Figure 6 shows numerous unassigned bond pads (and that paragraphs [0076]-[0077] describe reference numerals present in Figure 6), a POSITA would

easily understand that Yoshinaga was simply saying that the ground pad **labels** are not shown, not that the ground pads themselves are missing from Figure 6.

148. The reason Yoshinaga Figure 6 bothers to label the supply pads (but does not label the ground pads) is because circuit blocks 1, 2, and 67 may operate on different supply voltages (e.g., 3V, 5V, etc.) and thus must be assigned to their corresponding circuits. By contrast, Yoshinaga's reference potential pads are electrically connected as depicted in Figures 1, 2, and 4, so there is no reason to label them in Figure 6.

c. Issue 3 (Pad Assignments are Flexible and Petitioner's Proposed Ground Pad Placements Were Obvious)

149. Patent Owner contests whether it would have been obvious for a POSITA to assign the existing bond pads which are immediately next to Yoshinaga Figure 6's saved area as ground pads. POR, 19-23. This challenged fails for multiple reasons.

150. First, the bond pads in Yoshinaga Figure 6 are all the same. This is similar to how all of the bond pads in the '164 patent (e.g., Figures 1, 2, and 3) are all the same. Yoshinaga's Figure 6 illustrates the pads identically. And, because Figure 6 is an implementation of "the semiconductor [IC] of FIG. 1," it plainly includes ground pads 5 and 6.

151. Against this backdrop, Patent Owner still asserts that "[p]ower supply pads and reference potential pads are fundamentally different." POR, 23. But even

Dr. Khatri contradicted this at his deposition. Ex. 1038 (Khatri Tr.), 186:14-21 (“pads are all similar [] if not completely identical”), 204:25-205:19, 185:18-186:4, 203:24-204:7, 215:8-216:6. There is simply no difference in the size, shape, dimensions, material, etc. of ground and power pads. They are the same. The fact that one pad may connect to a power rail and another pad may connect to a ground rail says nothing about the actual pads themselves, and does not make them “fundamentally different.”

152. Just like the ’164 patent, Patent Owner never explains the purported “entirely different purposes” of power and ground pads. One source current while the other sinks current. Saint, Figure 7-3 (ESD protection “to VCC1 and GND1”). That’s all there is to it. And, in the ESD context, they both serve to dissipate current from an ESD event. Patent Owner’s contrary position is like saying someone’s feet “serve entirely different purposes.” Just as one’s feet are mirror images of one another and work together in a complementary fashion, so do ground and power pads. Patent Owner assertions to the contrary are baseless.

153. Patent Owner’s attempt to conflate bond pads with the circuitry they connect to is misleading. Numerous instances confirm pad assignment flexibility. Saint itself confirms pad assignment flexibility, including that pad assignments dictate floor-planning, not the other way around as the Patent Owner suggests. Saint, pp. 159-160, 209. For example, Saint teaches it is often the best design practice to

“plan your bond out before you begin chip layout.” *Id.*, pp. 209-210.

154. Saint Figs. 7-1 and 7-2 (shown below) illustrate two different, but “totally valid,” pad assignments for the same chip. In Figure 7-1, the “powers [are] on the top and [] grounds [are] on the bottom.” Saint, p. 159. Saint teaches that “you could use the same package and the same signals, but dictate the various signals to be in very different places,” which is “also a totally valid pin-out.” *Id.*

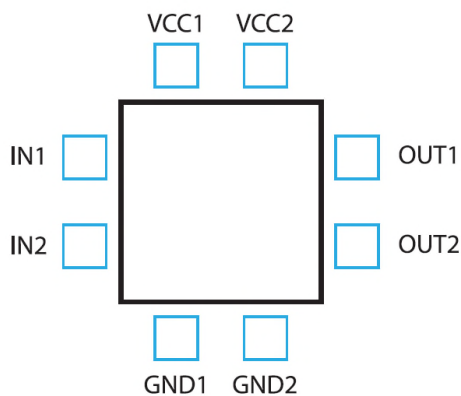


Figure 7-1. Like items set side by side. One possible pin-out.

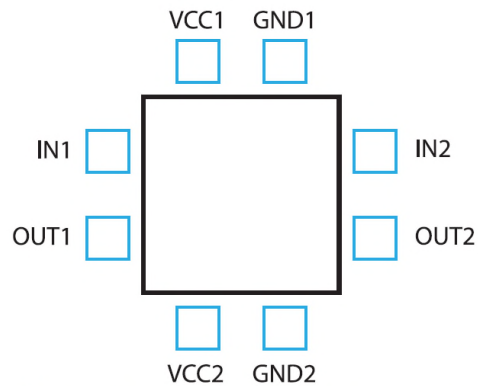


Figure 7-2. Very different pin placement will produce a very different layout.

Id. While the assignments may “affect[] how you floorplan your chip,” the pad assignments in the first instance are fungible. *Id.*, 209-210 (“plan your bond out before you begin chip layout”). Stated another way, Saint teaches that pad assignments are often made first, which then impacts other aspects of the design (viz., circuit location), not the other way around as the Patent Owner would have the Board believe. *Id.*, p. 160. Just as Saint Figure 7-2 is “a totally valid pin-out” (*id.*, p. 159), Petitioner’s pad assignments in Yoshinaga are also “totally valid.”

155. Second, there are numerous reasons why a POSITA would have made the proposed pad assignments in Yoshinaga. As outlined in my opening Declaration, some of these include: (1) that Yoshinaga shows that its ground pads are electrically connected in Figures 1, 2, and 4; (2) that bondwires are an affordable, reliable, and ubiquitous means for connecting to a bond pad; (3) Saint's teaching to minimize bondwire distances would have motivated a POSITA to make Petitioner's proposed ground pad assignments because doing so is the shortest distance for a bondwire connection (particularly for a pad-to-pad jumper bond wire); and (4) Petitioner's proposed pad assignments preserve Yoshinaga's saved area for other circuitry, which Saint teaches is desirable to reduce die size and decrease per-IC cost.

156. Contrary to Patent Owner's assertion that Yoshinaga's saved area would "remain even without [Ppetitioner's] changes" (POR, 21), using an on-chip metal trace would defeat the very purpose of Saint's saved area. Patent Owner's assertion that Petitioner ignored considerations such as "chip size, the number of I/O signals, and the number of pads available" is baseless. POR, 20. I discussed the concepts of "core-limited" versus "pad-limited" designs (which are necessarily determined by chip size and pin/pad count) and their impact on pad location/assignment in my opening Declaration. Ex. 1003, ¶¶49-50, 61, 100, 137, 322, 384, fns.12-13, 28, 30 – and provided an extended discussion of these topics above (in Section III.B). It is Patent Owner that ignored these considerations. I also

explained why Yoshinaga Figure 6 is self-evidently a core-limited design (*e.g.*, otherwise, it would depict additional pads in the other available areas on the periphery of the chip).

157. I further wish to note that Patent Owner’s argument that I said Yoshinaga did not disclose ground pads “adjacent” to the ground bus grossly mischaracterizes my testimony. POR, 17. Read in context, all I said was that Yoshinaga Figure 6 does not expressly show the ground pad connection to the ground rail. But, in the context of the ’164 patent, even Dr. Khatri admitted that a POSITA would know such a connection exists – even though Figure 2 does not show the pad 22 connection to the ground bus. Ex. 1038 (Khatri Tr.), 195:20-196:8. The same is true in Yoshinaga.

d. Issue 4 (Patent Owner Misunderstands the Proposed Yoshinaga Modification; Figure 6 is Not Inoperable)

158. Saint’s teachings (discussed above) that circuitry is placed (*i.e.*, in a layout) in view of pad assignments rebuts Patent Owner’s unsupported assertion that Petitioner’s proposed ground pad assignments mean that Yoshinaga Figure 6 “would [not] work.” POR, 21. By making the pad assignments first and then laying out the blocks, the design has far more than a reasonable expectation of success.

159. Next, Patent Owner argues that “[r]eplacing ‘power supply pads 3, 4, and 58’ with reference supply pads and a Circuit 67 GND ... would have fundamentally altered and negatively affected [Figure 6’s] electrical operation.”

POR, 23. This argument fails because: (1) Petitioner never proposed eliminating any pads or otherwise reducing the number of power pads (Pet., 30-34, 20-23); and (2) Patent Owner's assertion is wholesale speculation because Patent Owner knows nothing about the function (or power requirements) of Figure 6's generic chip (Ex. 1038 (Khatri Tr.), 312:19-313:10). Patent Owner's argument also relies on the false premise that circuit blocks 1, 2, and 67 each need multiple power pads (something Yoshinaga never says). It was (and is) common practice to use extra pads (if available) to provide additional power/ground access points for redundancy, even if not necessary for functionality.

160. First, Patent Owner's argument relies on the false premise that Petitioner **removed** (instead of **reassigned**) power pads. If that was Petitioner's proposal (it was not), then the modified version of Yoshinaga Figure 6 would show fewer pads; however, it shows the full complement of pads present in the unmodified version of Yoshinaga Figure 6. This is apparent by comparing Yoshinaga Figure 6 (42 pads) with modified Figure 6 in my opening Declaration (which also has 42 pads). Indeed, Dr. Khatri admitted this at deposition. Ex. 1038 (Khatri Tr.), 292:19-293:5. Because Yoshinaga's supply pads could be assigned (or re-assigned) to numerous locations among unused pads, neither Petitioner nor I restricted the power pad assignments to any specific pad locations. Nor does that matter to the claims, which are silent regarding power pads. I note here that Patent Owner takes my

deposition testimony out of context and grossly mischaracterizes it. POR, 27 (citing Ex. 2011, 123:2-125:12). Far from saying that any power pads were eliminated, I testified about relocating (i.e., reassigning) the pads. Ex. 2001, 123:19-21 (“[pad] 3 is a power supply pad but the pad could go somewhere else. It could be relocated elsewhere”). This has been my opinion all along.

161. Given that the number of pads in the unmodified and modified versions of Yoshinaga Figure 6 are the same, there is no basis for Patent Owner to say I removed or eliminated any pads. The only apparent reason for making such an assertion is to setup a strawman argument. But even if there were fewer power pads, many designs/chips would function properly and the claims are still obvious (i.e., not all chips need 11 power pads, just like a house and an apartment complex have different water needs).

162. I note that Yoshinaga says nothing about the functionality that its chip is supposed to perform; this is because it is a generic example with applicability to a wide variety of integrated circuits. Indeed, Dr. Khatri admits that “Yoshinaga’s teaching is not about the type of circuits in circuit 1, 2 and 67,” which are “flexible.” Ex. 1038 (Khatri Tr.), 312:19-313:10. Patent Owner’s contrary assertion is totally unsupported and relies on speculation that Figure 6’s generic chip is somehow power limited. As such, Patent Owner lacks any basis to artificially restrict the ground pad assignments based on unknown current requirements, unstated “drive strength”

limitations, unknown power requirements, etc. that “possibly render[]” Figure 6 “non-functional.” POR, 24-26; Ex. 2010, ¶¶51, 54.

163. Patent Owner makes far too much of the power pad labels 3, 4, and 58 in Figure 6. The reason Yoshinaga labeled these pads was to indicate which circuit block (viz., 1, 2, or 67) is associated with each power domain (Yoshinaga, [0076]-[0077]), which makes sense because each power domain could, for example, have its own power supply voltage level, such as 3V, 5V, etc. Stated differently, Yoshinaga is merely indicating that the power pads 3 (which correspond to circuit 1’s power domain) are located among the pads associated with (and nearest) circuit 1, not that they must be the specific pads labeled 3 in Figure 6. Likewise, power pads 4 (which correspond to the power domain for circuit 2) are located among the pads associated with (and nearest) circuit block 2. This does not mean that the exact pads labeled 4 are material in any way as Patent Owner incorrectly suggests. The same holds true for pads 58 vis-a-vis circuit 67.

164. Patent Owner contends that Petitioner ignored the purported “disadvantages” of its pad assignments. POR, 23-27. But the ’164 patent identified no “disadvantages” of assigning ground pads near the saved area. The reason for this is that Patent Owner’s alleged “disadvantages” are, at best, greatly overstated.²⁵

²⁵ Citing Saint, Patent Owner asserts that one “cannot arbitrarily change pads from

165. Patent Owner appeals to Saint for the idea that “a POSITA would ‘look at the drive strengths in the cells and place ‘more power strapping’ in ‘certain areas that require more power.’” POR, 24 (quoting Saint, p. 33). While that may be true, it is irrelevant to the matter at hand. The prior page in Saint explains what “power strapping” is—laying wide, low-resistance metal traces from the already placed power pads to deliver power where needed. Saint, p. 32; *see also id.*, p. 33 (automated tools “place[] more power strapping in [high-power demand] area[s]”). Again, the power traces are placed based on where the power pads are located, not the other way around as Patent Owner wants the Board to believe. The “power straps” are merely the distribution wires in the chip, not the power pads - and Patent Owner’s argument fails.

e. Issue 5 (Real-life Data Sheets Confirm Flexible Pad Assignments)

166. Numerous product datasheets (*e.g.*, Ex. 1032 to Ex. 1036) show that there is great flexibility in ground and power pin/pad locations. These datasheets show varying numbers of power/ground signals in a multitude of pad assignments. Ex. 1032, 5 (shows various VSS/ground locations); Ex. 1033, 38-41 (shows ground

unlabeled or supply pads to reference potential pads.” POR, 23. But this section of Saint (titled “Packaging”) just says that bond pads need to align with package pins, so you cannot “blindly put [pads] wherever you feel like.” Saint, pp. 201-202. This observation about pad/pin ***alignment*** says nothing about pad ***assignments***.

pins (which correspond to ground pads) in the middle of a row); Ex. 1036, 9 (similar); EX1034, 3-4 (shows multiple different ground configurations/assignments); Ex. 1035, 28-33 (shows multiple VSS/ground configurations). This is just a small sampling of the variety of ground and power assignments. There are literally thousands upon thousands of power and ground assignments in existence, spanning all sorts of chips of differing sizes, functionalities, and pin counts.

167. Ex. 1035 is a good example – as pp. 28-29 show two different package configurations for the same IC. Notably, in the configuration on pg. 29, there are 3 VDD pins and 3 VSS (ground) pins. But, in the configuration on pg. 28, there are only 2 VDD pins and 2 VSS (ground) pins. This shows that, contrary to Patent Owner’s assertion (POR, 23-26), chips often have differing numbers of ground and power connections, and these differences in the number of power and ground pins obviously does not make a chip “non-functional.”

168. With respect to pad changes, Dr. Khatri described how he had worked on an IC design at Motorola where the IC in question was converted from a wirebond-connection package with peripheral bond pads to a C4 “flip-chip” connection package. Ex. 1038 (Khatri Tr.), 118:19-119:4, 120:6-9 (“there were two versions of the chip, there was the, you know, bond pad package version and then there was a C4 version”); 123:6-7 (“C4 is effectively called flip chip”); 124:3-16.

The Motorola chip was the 88110 microprocessor (*id.*, 94:3-4) which had hundreds of pins (https://en.wikipedia.org/wiki/Motorola_88110#/media/File:KL_Motorola_MC88110RC40.jpg).

169. Dr. Khatri testified that while converting the peripheral bond-pad version to a flip-chip package required a great deal of effort, it proved readily possible to relocate the bond pads to accommodate the different packaging form without compromising chip performance. Ex. 1038 (Khatri Tr.), 128:2-24 (“I had made sure that the performance was at least as good” when we changed all the pads); 124:3-16. While it may have required non-trivial engineering effort to convert a peripheral bond pad chip to a flip-chip arrangement (which required physically moving all of the bond pads) for the Motorola 88110 microprocessor with hundreds of pads, reassigning several existing power and ground pads on a chip with a modest pin count is clearly a much-less-onerous task.

170. A customer using an IC product would (justifiably) expect the same IC behavior across all packages and pinouts – even if the package pins (and their corresponding bond pad assignments) were changed to accommodate different packaging configurations. There is simply no reason why pins and pads cannot be easily re-assigned for the vast majority of chips (as the datasheet discussion above clearly shows).

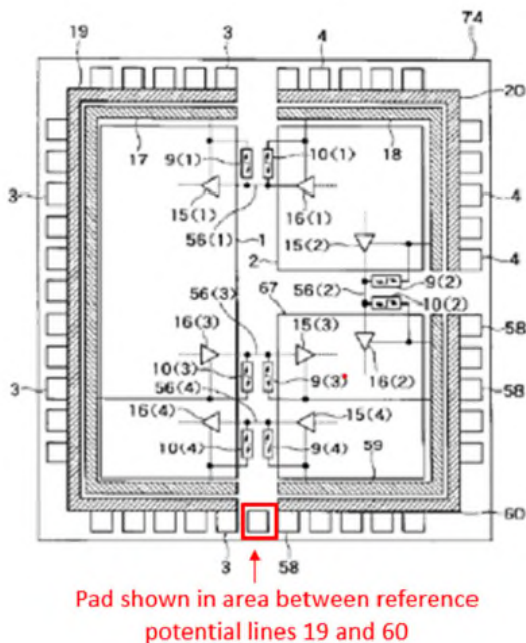
171. All of this confirms that Petitioner’s proposed ground pad assignments were “suitable.” Additionally, Patent Owner’s own exhibit recognizes that “package design is assumed to be flexible, such that there is complete independence in placing [power and ground] pads.” Ex. 2013, 2; *id.*, 6 (multiple placement options); Ex. 1038 (Khatri Tr.), 169:25-170:11 (pad placement is iterative), 171:17-24 (similar). Dubey is premised on re-assigning power/ground pads. Ex. 2013, Abstract. A further premise of Dubey is that “[power and ground] pads are placed all across the chip periphery.” *Id.*, 2. Dubey recognizes some designs have “uniform power density,” meaning no optimal power/ground pad assignment exists. *Id.*, Abstract.

172. Making any minor adjustments necessary to pad re-assignments is easy to do for multiple reasons. For example, automated design tools exist to perform signal routing; for a modest-sized chip, these tools run quickly and perform their task at the push of a button; well-known companies such as Cadence, Siemens (which acquired Mentor Graphics), and Synopsys provide such tools. Additionally, Yoshinaga (and Saint) shows a ground bus that substantially surrounds the entire chip periphery, making bond pad connections to the ground rail(s) easy to implement; the same is true for the power rail(s). Thus, even if pads are re-assigned post-layout, doing so can be done with little effort.

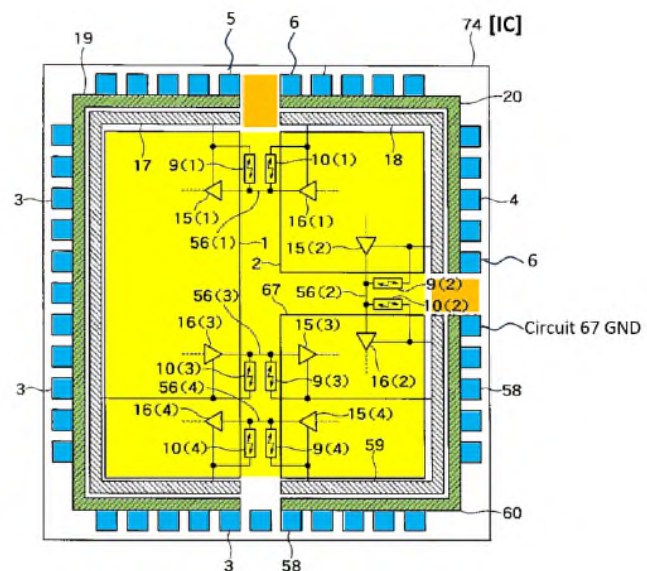
173. Moreover, the ’164 patent recognizes that “multiple pads” from the same group can be wire bonded to the common ESD bus. Ex. 1001, 3:11-15.

f. Issue 6 (Patent Owner Creates an Imaginary Pad)

174. Patent Owner argues that Petitioner “assumes, without support,” that Yoshinaga’s “[saved] spaces do not include a pad,” and thus fail the requirement of no pad[s] in the ... saved area. POR, 42. This argument fails the red-face test. Patent Owner highlights a pad in red in Yoshinaga Figure 6 (left image). But Petitioner never identified that region as a saved area (the right-hand image shows the saved areas in orange). Patent Owner’s red pad stands in stark contrast to Petitioner’s empty, orange saved areas - where Patent Owner implies an imaginary pad must exist.

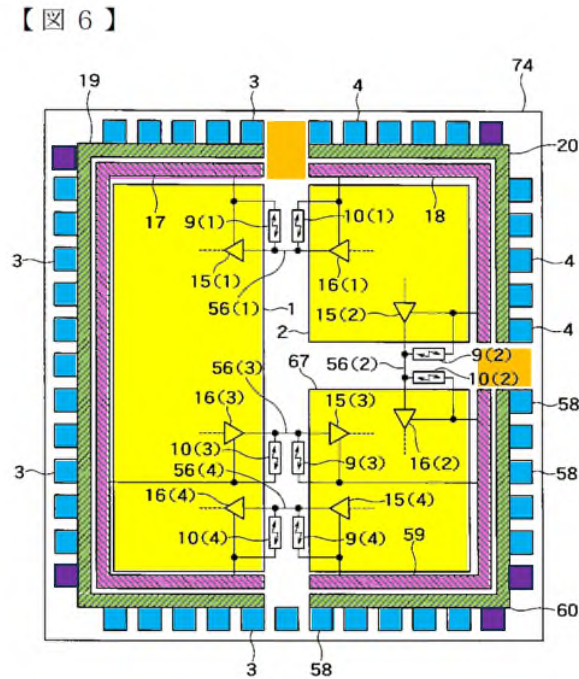


POR, 44 (Yoshinaga, Figure 6)
(Annotated by Patent Owner)



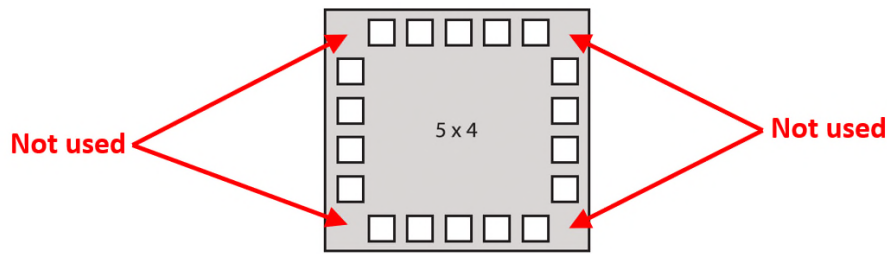
Pet., 40 (Yoshinaga, Figure 6)
(Annotated by Petitioner)

175. Even if more pads were necessary (they are not), Figure 6 has sufficient space. Dr. Khatri admits Yoshinaga has “10 potential locations” for reference pads (Ex. 2010, ¶102), including the purple locations below *outside* the saved areas. Yoshinaga, Figure 6 (annotated).

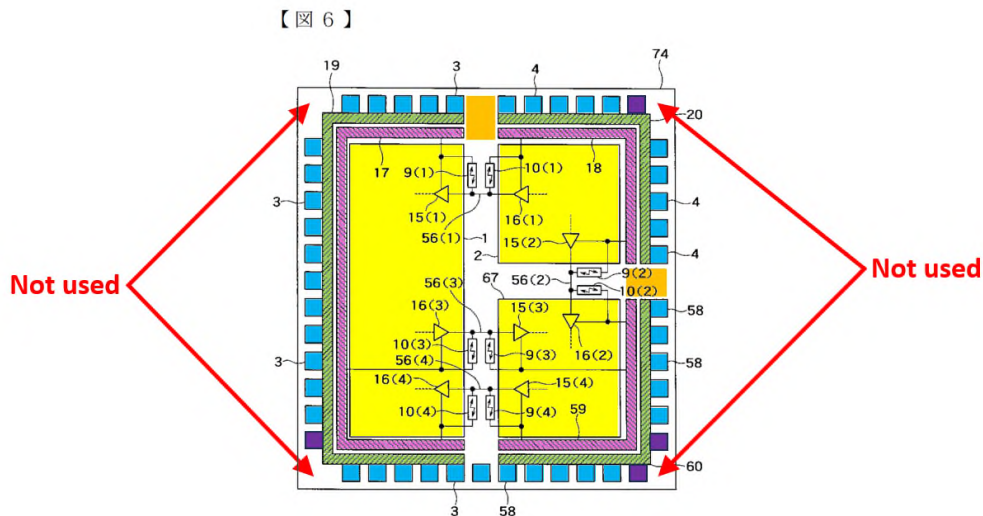


Yoshinaga, Figure 6 (annotated).

176. Dr. Khatri’s argument that the only place for more pads is in the saved areas is belied by the figure above. Citing Saint Figure 9-20, Dr. Khatri discounts “corner” locations.



Saint, Figure 9-20 (annotated). However, this differs from Yoshinaga Figure 6, where sufficient space exists for additional pads (purple) while leaving the corners open (red arrows). Thus, Patent Owner’s “corner” argument fails.



Yoshinaga, Figure 6 (annotated); *see also* Pet., 20 (similar).

177. Moreover, Patent Owner’s argument ignores Saint’s teachings to “***use extra space surrounding our pads to shrink our chip size.***” Saint, p. 221 (emphasis added). And further, Saint ***does*** include IC floorplans that have pads placed in the corners (*see* Saint, Figure 8.5 – Figure 8.7)²⁶ – as an option that can be helpful in,

²⁶ These figures appeared earlier – in Section III.B.3.

for example, a pad-limited situation.

178. Patent Owner’s argument also fails because it incorrectly assumes Yoshinaga Figure 6 is pad-limited. If so, pads would be illustrated in the purple locations and/or between the reference buses (or even in the corners) – but they are not.

179. Contradicting the clear import of the Yoshinaga reference itself, Patent Owner baselessly asserts that “the existence of a space between [Yoshinaga’s] circuits or reference potential lines does not mean no pad or ESD bus is present,” and that “reference potential pads could and likely would be found in Petitioner’s purported ‘saved areas.’” POR, 43. Patent Owner relegates its sole support for this speculation to a footnote, where it contends that “[t]he unlabeled pads in Figure 6 of Yoshinaga would not be considered to be reference potential pads because Yoshinaga teaches that ‘reference potential pads *are not shown* to simplify the drawing.’” *Id.* (emphasis by Patent Owner). This is incorrect, especially when evaluating Yoshinaga as a whole (as was explained earlier, in Section III.B.3). In context, Yoshinaga was simply saying that the reference pads are not *labeled* in Figure 6; that is apparent from even a cursory review of Figure 6. There can be no dispute that Yoshinaga discloses in numerous places that pads 5 and 6 are both “reference potential pads.” Yoshinaga, [0088]; *id.*, Figs. 1, 2, and 4, [0014] (“reference potential pad 5”), [0025] (“the reference potential pad 6”), [0055]

(“reference potential pad 5” and “reference potential pad 6”). And given that Yoshinaga Figure 6 implements Figure 1 (*id.*, [0087]), it follows that reference pads 5 and 6 are present in Figure 6. Tellingly, the power supply pads 3 and 4 and reference potential pads 5 and 6 are illustrated identically in Yoshinaga Figs. 1, 2 and 4. Likewise, all of the pads in Yoshinaga Figure 6 appear identical to one another. By far, the most logical interpretation of Yoshinaga’s statement is that the reference pads are present, but not labelled, in Figure 6. Thus, there is no need to “add” reference pads in Yoshinaga’s saved areas.

g. Issue 7 (Haralabidis Discloses Bondwires)

180. Patent Owner suggests that Haralabidis’ lack of explicit “bond pad” disclosure equates to a lack of bondwire disclosure. POR, 51. That is misleading at best. Haralabidis expressly discloses that “segments of the IC ground rail are coupled to corresponding segments of the package ground rail by corresponding first electrical connections that could be, for example: wirebonds.” Haralabidis, 1:61-64; *see also id.*, 1:65-2:4 (same for common ground rail on PCB); 2:38-41 (“The SoC common ground rail 150 is connected to the package common ground rail via a plurality of electrical connections 170 that can be any of, but not limited to: wirebonds”). And it was well-known to POSITAs that bondwires connect to bond pads. As such, whether Haralabidis expressly illustrated “bond pads” is irrelevant.

h. Issue 8 (Patent Owner Does Not Understand Why the Bidirectional-Diode Circuitry is Used in These Circuits

181. Patent Owner employs smoke-and-mirror tactics by attempting to generalize Yoshinaga Figure 3's use of bidirectional diodes 37 and 38 as the means of connecting ground pads 5 and 6 in Figures 1, 2, and 4, which lack such diodes. POR, 52. Patent Owner attempts to assert that this bidirectional-diode circuit is included to improve noise immunity; however, if "noise" were such a concern that Figure 3 was configured to cope with it, then that same noise would require a similar configuration in Figures 1, 2, and 4 to cope with it; however, Figures 1, 2, and 4 do not include such a configuration – indicating that the alleged "noise" was not of sufficient concern to preclude Yoshinaga from disclosing three non-diode-connected embodiments (viz., Figs. 1, 2, and 4). Further, the '164 patent is notably silent regarding bondwire "noise" concerns – indicating that either these concerns are overblown by Patent Owner, or Patent Owner's own patent would be inoperable. Clearly, something else is going on in the use of such bidirectional-diode circuits.

182. Patent Owner does not understand that the reason for including the bidirectional-diode circuitry serves to separate noise from an ESD discharge (by causing the circuitry to react differently to noise than it does to an ESD event). This all serves to allow the more-complex ESD circuitry to function properly-and-optimally – while not reducing the degree of signal integrity protection (against noise) that is designed into the circuitry. This is something that is actually explained

very clearly by Haralabidis at col. 5:8-30; the same thing is done in Yoshinaga (see Yoshinaga at [0061]).

IV. SECONDARY CONSIDERATIONS

183. As explained in my opening Declaration, I am unaware of any secondary considerations of non-obviousness having been identified in connection with the patent's claims – nor am I otherwise aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, or the like relating to the '164 patent. To date and (more particularly) in its POR, Patent Owner has not identified any such secondary considerations of non-obviousness.

V. SUMMARY

184. It is my conclusion and opinion that Patent Owner has failed to rebut the analysis presented in Petition and in my opening Declaration – and that because of this failure by Patent Owner, Petitioner has demonstrated that the challenged claims of the '164 patent are indeed unpatentable. It should again be noted that Patent Owner (and its expert) have ignored a great deal of the material cited in both the Petition and in my opening Declaration. Further, Patent Owner (and its expert) also failed to perform adequately analyze their own materials and references – with consequences that were also explained in various parts of Section III. As a result, the Board should find that the challenged claims of the '164 patent are unpatentable.

VI. CONCLUSION

185. I am aware that this declaration will be filed as evidence in an IPR proceeding before the PTAB. I am aware that making willfully false statements in my declaration are punishable by fine or imprisonment, or both (under 18 U.S.C. § 1001), and thus such actions may compromise the validity of the IPR Petition. All statements herein made by me of my own knowledge are true, and all statements made on information and belief are believed to be true.

186. I declare under penalty of perjury that the foregoing is true and correct.

Executed this 23rd day of December, 2025 in Fletcher, Vermont.



Daniel Foty, Ph.D.