

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: January 21, 2026

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2025-00118
Patent 10,879,164

PATENT OWNER'S SUR-REPLY

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Exhibit List

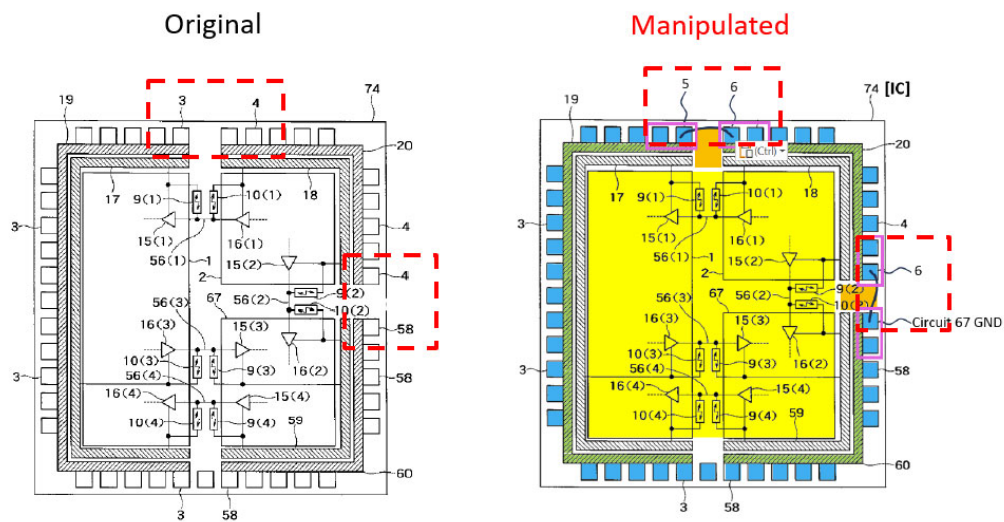
Ex.	Description
2001	Micron's Motion to Stay the Case Pending Inter Partes Review and Post Grant Review Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Jan. 16, 2025), ECF No. 200
2002	Plaintiff/Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s and Counterclaim Defendant Yangtze Memory Technologies, Inc.'s Opposition to Micron's Motion to Stay Case Pending Inter Partes Review and Post-Grant Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Feb. 3, 2025), ECF No. 221
2003	Docket Entry Order (issuing temporary stay), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Mar. 3, 2025), ECF No. 242
2004	U.S. District Courts—Time Intervals from Filing Date to Beginning Date for Completed Civil Trials, by District, During the 12-Month Period Ending September 30, 2024 (https://www.uscourts.gov/sites/default/files/2025-01/jb_t3_0930.2024.pdf)
2005	RESERVED
2006	Curriculum Vitae of Dr. Sunil Khatri
2007	Declaration of Dr. Sunil Khatri ("Khatri")
2008	Civil Minutes, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Sept. 18, 2024), ECF No. 141
2009	Defendants' Preliminary Invalidity Contentions and Document Production Accompanying Invalidity Contentions re YMTC II Asserted Patents (Patent Local Rules 3-3 and 3-4), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Nov. 25, 2024) (excerpts)

Ex.	Description
2010	Declaration of Dr. Sunil Khatri in Support of Patent Owner's Response ("Khatri2")
2011	Transcript of the Deposition of Daniel Foty, Ph.D., taken August 6, 2025, <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , IPR2025-00118 (P.T.A.B.) ("Foty Dep.1")
2012	Interconnect Technology and Design for Gigascale Integration (Jeffrey A. Davis & James D. Meindl eds., 2003) (excerpts) ("Davis")
2013	Aishwarya Dubey, <i>P/G Pad Placement Optimization: Problem Formulation for Best IR Drop</i> , Proc. of the Sixth Int'l Symp. on Quality Elec. Design (ISQED), San Jose, CA, pp. 340-345 (Mar. 21-23, 2005) ("Dubey")
2014	Howard Johnson, <i>Chip-Scale Transmission Lines</i> , High-Speed Digit. Design Online Newsl. (Signal Consulting, Inc.) (2003), https://www.sigcon.com/Pubs/news/7_01.htm ("Signal Consulting")
2015	Kian Haghdad & Mohab Anis, <i>Power Supply Pads Assignment for Maximum Timing Yield</i> , 58 IEEE Transactions Circ. Sys. 697 (2011) ("Haghdad")
2016	Declaration of B. Thomas Watson In Response To Petitioner's Objections to Evidence [<i>served, not filed</i>]
2017	Transcript of the Deposition of Daniel Foty, Ph.D., taken January 9, 2026, <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , IPR2025-00118 (P.T.A.B.) ("Foty Dep.2")

I. Introduction

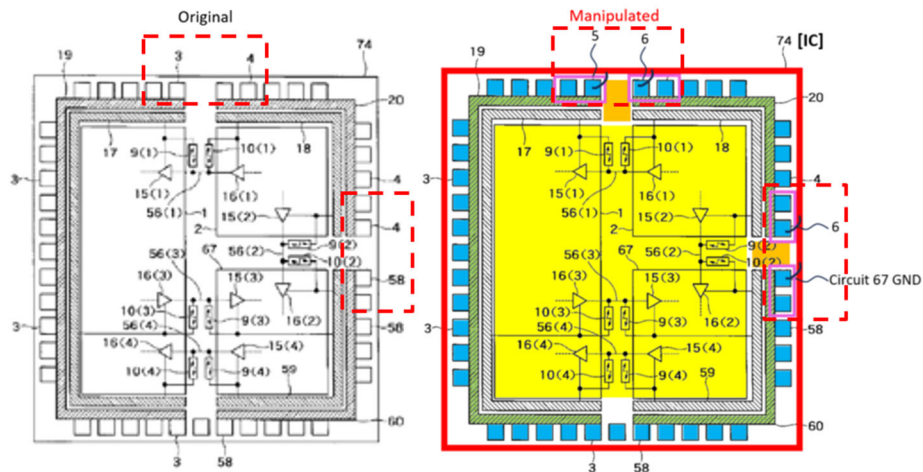
In the Patent Owner's ("PO") Response ("POR"), PO showed that Petitioner's positions rely on hindsight rather than the knowledge of a POSITA, as evidenced by Petitioner's manipulations to Yoshinaga Figure 6 (Grounds 1-2) and Saint Figure 7-7 (Ground 3). Petitioner's Reply does not overcome these defects.

Ground 1 Manipulations¹



¹ Dotted red squares highlight pad manipulations.

Ground 2 Manipulations



Ground 3 Manipulations

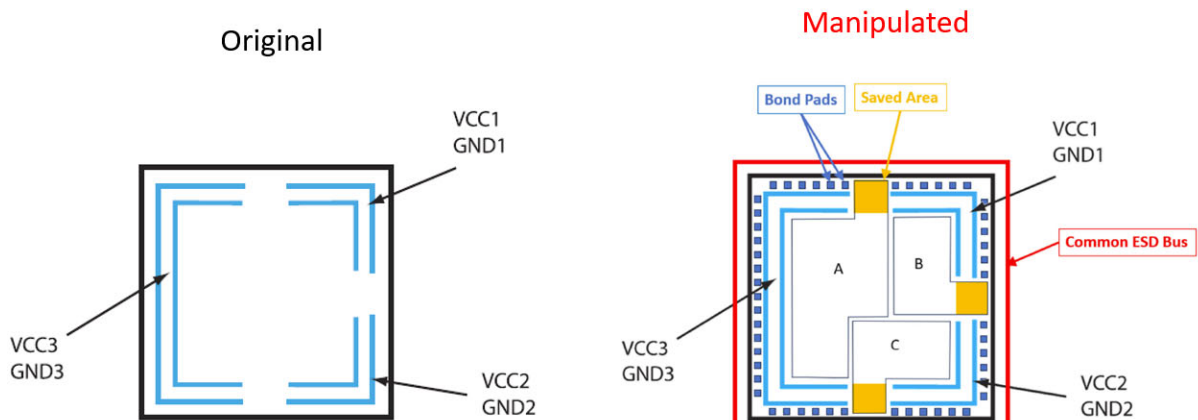


Figure 7-7. Pin-out simplification showing like protects grouped together.

Figure 7-7. Pin-out simplification showing like protects grouped together.

The Petition did not identify the claimed “circuit area compris[ing] ... a saved area” in Yoshinaga (POR 41-42), and the Reply does not cure this fatal failure. Petitioner also failed to show that the prior art discloses a “saved area” “adjacent” to “ESD buses” and “pad groups” or that a POSITA would be motivated to add one. Thus, Grounds 1-3 fail.

Grounds 1-2 also do not render obvious “a plurality of pad groups” “adjacent and connected to the plurality of ESD buses.” POR 16-27. In Reply, Petitioner misreads Yoshinaga by asserting that ground pads are depicted, but unlabeled, contrary to Yoshinaga’s express statement. Ex.1006 (“Yoshinaga”) [0078]. Because ground pads are not shown in Figure 6, adjacency to the ESD buses cannot be established. Petitioner’s fallback—reassigning Figure 6’s pads as shown above—contradicts electrical realities. Pad assignments follow power needs. Thus, reducing supply pads as Petitioner suggests would degrade power delivery, potentially rendering Yoshinaga inoperable. Confronted with this fatal error, Petitioner asserts for the first time that a POSITA would reassign the supply pads—an improper shift that ignores Yoshinaga’s electrical requirements.

Ground 3 fares no better. As the Institution Decision and the POR explained, Saint’s Figure 7-7 maintains multiple distinct grounds for ESD protection—not a single common ground. ID 33-34; POR 58-64. Saint therefore teaches away from connecting ESD buses to a common ESD bus on the chip. The Reply’s effort to retrofit Figure 7-7 with a common ESD ground ignores Saint Figure 7-7’s core teaching.

Finally, as the POR noted, none of Petitioner’s references suggest using bonding wire to form pad-to-pad connections over a “saved area” as Petitioner proposes. POR 27-39, 64-66. Such pad-to-pad bonding wire connections risk sag

and shorts, making bonding wire “not even an option.” Ex.1038 224:16-226:25. Petitioner's proffered motivations for using bonding wire to connect pads to a common ESD bus similarly fail. Grounds 1-3 therefore do not render obvious the claimed bonding wire connections.

For these reasons, Grounds 1-3 fail.

II. The prosecution history confirms the '164 patent's validity

Petitioner's Reply overplays the prosecution history, claiming the “saved area limitation was the reason for allowance.” Reply 1, 25-26 (emphasis omitted). That history, if anything, underscores that the “saved area” limitation was not obvious. It does nothing to show that the claimed “saved area,” or any other claim limitation, would have been obvious in view of Yoshinaga, Saint, or Haralabidis for several reasons.

First, obviousness must be assessed for the invention “as a whole,” not by isolating a single limitation. *See Sanofi-Synthelabo v. Apotex, Inc.*, 550 F.3d 1075, 1085-86 (Fed. Cir. 2008).² Recasting allowance as hinging on a single limitation as Petitioner does (Reply 1, 25), is legal error.

Second, Yoshinaga, Saint, and Haralabidis were never before the Examiner, so the history does not show those references—individually or in combination—

² Unless otherwise noted, all internal quotation marks and citations are omitted.

render any claim limitation obvious, consistent with the POR and Dr. Khatri's testimony. *See* POR 9-10; Ex.1038 50:20-51:6.

Third, even accepting *arguendo* Petitioner's premise that the patent's allowance turned on the "saved area" limitation, Petitioner still identifies no prior-art implementation of that limitation. As shown in the POR and further explained below, neither Yoshinaga, Saint, nor Haralabidis discloses the claimed "saved area" both "adjacent to two respective ESD buses and respective pads of two respective groups" and with "no ESD bus and no pad." POR 40-45, 56, 66-67. Petitioner's failure to identify such implementations confirms the Examiner's allowance of the '164 patent.

III. Grounds 1-3 do not render obvious the claimed "saved area"

A. Grounds 1-2 fail because Petitioner fails to establish Yoshinaga renders obvious a "circuit area compris[ing] ... [a] saved area"

The Petition never identified a "circuit area compris[ing] ... [a] saved area" in Yoshinaga. POR 41. The Reply does not cure this defect. It cites a single Figure in the Petition³ labeling a purported "saved area," but that Figure does not identify

³ Petitioner relies on one drawing in Dr. Foty's declaration that (1) the Petition never refers to, and (2) comes from a paragraph cited once in the Petition within a generic 19-paragraph citation. Pet. 39. That is insufficient. 37 C.F.R. § 42.6(a)(3)

that “saved area” as part of a “circuit area,” and the Board should reject Petitioner’s attempt to rewrite its Petition on Reply. Reply 29-30 (citing Pet. 40). That omission is dispositive. *See MModal LLC v. Nuance Commc’ns, Inc.*, 846 F. App’x 900, 906 (Fed. Cir. 2021) (requiring the petition provide “the element-by-element specifics of the unpatentability challenges”).

The Reply also does not establish that Yoshinaga discloses a “circuit area” that includes a “saved area.” Instead, it mischaracterizes PO’s position as asserting that only Yoshinaga’s circuits 1, 2, and 67 contain circuitry. Reply 30. Not so. PO explained—and Petitioner does not meaningfully contest—that Petitioner “does not identify any disclosure in Yoshinaga that suggests the purported ‘saved area’ between the pads can contain circuitry and be part of the circuit area” and contains no pads. POR 42. The purported “saved area” contains no circuit components; both the expressly identified circuit areas 1, 2, and 67 and diodes 9 and 10 (discussed at Reply 30), lie outside that area. Yoshinaga Figure 6. Even if circuitry could be placed in that purported “saved area”—which Petitioner has not shown—it still would not establish the purported “saved area” is used as a “circuit area.” Consistent with that

(“[a]rguments must not be incorporated by reference from one document into another document”).

absence of evidence, Dr. Khatri testified that a POSITA would have no reason to treat the highlighted “saved areas” as within a circuit area. Ex.2010 ¶¶99.

B. Grounds 1-3 do not render obvious the claimed “saved area”

Contrary to Petitioner's assertion that pads in the “saved area” are “imaginary” (Reply 31), a POSITA would treat those purported “saved areas” as preferred locations for ground pads in Yoshinaga. Yoshinaga aims to make the circuit “as small as possible,” and, as Dr. Khatri explained, the spaces Petitioner labels “saved areas” would be preferred for reference potential pads. Ex.2010 ¶¶102-103. This aligns with Petitioner's expert, who testified that a POSITA would “keep pads close to the blocks” they serve. Ex.2011 76:19-77:9. Because ground pads connect to nearby ESD grounds, they would be placed in the purported “saved area,” not in the locations Petitioner posits (Reply 32). Thus, Petitioner fails to establish Yoshinaga's purported “saved area” is pad-free as the claims require.

Petitioner fails to show that Saint's Figure 7-7 discloses the claimed saved area. At most, Petitioner points to a gap “between ESD buses” in Figure 7-7, which is not a pad-free gap as shown in Figure 7-6. *Id.* 33. As Dr. Khatri explained, Figure 7-7—read with the VCC/GND configurations of Figures 7-3 through 7-6—does not describe any “extra space” free of pads or ESD buses that could house circuitry. Ex.2010 ¶¶140-144.

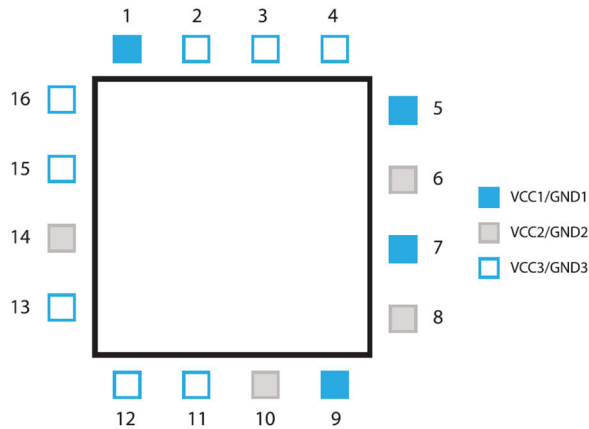


Figure 7-6. Scattered pins on the same protect circuit.

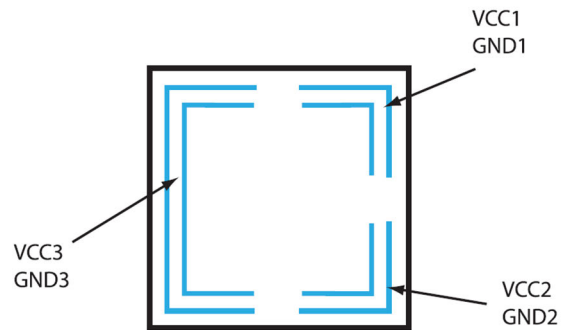


Figure 7-7. Pin-out simplification showing like protects grouped together.

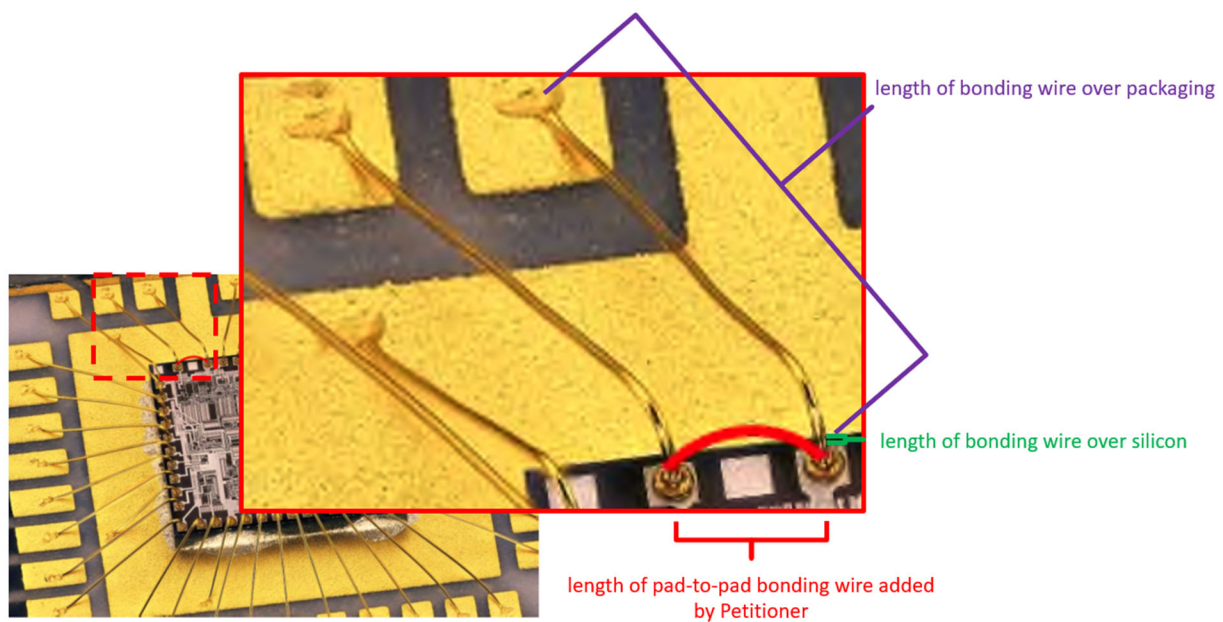
Ex.1008 (“Saint”) Figs. 7-6, 7-7. In Reply, Petitioner ignores how Saint incorporates Figures 7-3 through 7-6 into Figure 7-7 and that the “saved area” must be adjacent to pad groups and ESD buses.

Because neither Yoshinaga’s Figure 6 nor Saint’s Figure 7-7⁴ discloses the claimed “saved area,” Petitioner must rely on obviousness to create one in Yoshinaga and Saint. POR 44-47. Petitioner misunderstands this point as evidenced by its incorrect assertion that PO argues the claims require “creating a ‘saved area’” or “removing ‘filler cells.’” Reply 26-27.

As the POR explained, Petitioner’s proposal to span a “saved area” with pad-to-pad bonding wire contradicts its premise of adding that “saved area.” POR 46-47. In Reply, Petitioner argues there is no contradiction because the pad-to-pad bonding wire would be short, comparing pad-to-package bonding wire lengths to the length

⁴ Saint Figure 9-28 is not the same embodiment as Figure 7-7.

needed to cross a purported “saved area.” Reply 27-28. This comparison is misleading: it does not show sag would not be a problem when spanning an added saved area. The only wires shown run pad-to-package, with virtually all length over the package substrate (purple) and almost none over silicon, as shown below. Meanwhile, a pad-to-pad bonding wire (red) has a substantially larger silicon overlap than the pad-to-package bonding wires (green).



Reply 28 (annotated; concentrated).

This distinction matters. As Dr. Khatri and Saint explain, sag creates a shorting risk where there is “silicon overlap,” hence “you cannot have a pad in the middle of the chip” or use wires “too long.” Saint 190, 195; Ex.2010 ¶80. Short circuits occur when the bonding wire sags onto the integrated circuit. Ex.2017 67:13-68:11. That concern is negligible for pad-to-package connections because the wire

runs off-chip with minimal silicon overlap—which explains why bonding wire is conventionally used. Comparing pad-to-package length to a hypothetical pad-to-pad span is irrelevant; the issue is silicon overlap, not total bonding wire length. Using bonding wires to connect pads across an added “saved area” would create substantially more silicon overlap than conventional pad-to-package wires—the only usage Saint describes.

For that reason, a POSITA would not adopt Petitioner's proffered modification absent hindsight. As Dr. Khatri testified, running a bonding wire over a saved space would have required a long bonding wire and risks a short circuit. Ex.2010 ¶81. Petitioner's own expert corroborated this conventional wisdom: pads should be kept at the periphery and evenly distributed “so that they can connect off to the traces in the package without ... going over the middle of the circuitry.” Ex.2011 201:17-202:20. Unsurprisingly, the physical circuits depicted in Dr. Foty's Reply Declaration (Ex.1042 ¶18) and the Reply's image (at 28), do not show bonding wire pad-to-pad or pad-to-common ESD bus connections, let alone connections over a saved area. Ex.2017 21:11-23:17, 24:10-15, 97:16-98:10, 100:16-101:13. They only show bonding wire pad-to-package connections. *Id.* 21:11-16, 23:11-17, 100:16-21. A pad-to-pad span across a saved area would place significantly more wire over silicon than the pad-to-package connections in the cited prior art.

Petitioner's attempt to defuse the sag problem by misquoting Dr. Khatri fails. Reply 29. He explained sag was a known problem that, under conventional wisdom, barred pad-to-pad wire bonding, and that the '164 patent's inventiveness was embracing what went contrary to that conventional wisdom. Ex.1038 246:3-248:22.

Petitioner next argues that applying Saint Figure 9-28's "pad placement" to Figure 7-7 "to preserve Saint's 'extra space' benefit" is "obviousness, not hindsight." Reply 33. The record shows otherwise. As discussed above, Petitioner fails to identify any gap between pads in Figure 7-7 free of pads and ESD buses that could constitute a "saved area." Combining Saint Figure 9-28 with Figure 7-7 does not cure that defect. Figure 9-28 does not disclose "saved areas" adjacent to two ESD buses or pads. Ex.2017 76:10-18. Figure 9-28 says nothing about gaps between pads and ESD buses (necessary to create the claimed "saved areas") that would permit reliable bonding wire connections without shorting. Saint 206-207. Without a disclosure tying "saved area" location to ESD bus and pad groups, Petitioner's proposal reconstructs the invention with hindsight rather than a POSITA's knowledge or Saint's teachings.

Even setting aside the lack of a disclosed "saved area," Petitioner's combination lacks a reasoned motivation because Saint Figures 7-7 and 9-28 embody materially different integrated circuits. Saint Figure 7-7 employs three separate grounds that cannot be shorted and a pad distribution that leaves no "saved

areas.” Ex.2010 ¶¶122-126. By contrast, Figure 9-28 does not describe ESD buses or even pad spacing. Ex.2017 76:10-18. These are not interchangeable choices; they are incompatible designs with different pad counts. A POSITA would have no technical reason—and significant reasons not—to import Figure 9-28’s pad placement with 10 pads into the multi-ground, evenly spaced pad scheme of Figure 7-7 with 16 pads, where shorting cannot be risked and the even distribution of pads negates the premise of available “extra space.” Ex.2010 ¶¶139-150. Petitioner’s theory ignores Saint’s operative teachings of Figure 7-7 (including Figures 7-3 through 7-6) and selectively invokes Figure 9-28 for a result-oriented reconstruction—classic hindsight.

Petitioner’s reliance on Saint Figure 9-21 is likewise misplaced. Reply 34. Figure 9-21 is a distinct embodiment from Figure 7-7 and conflicts with Saint’s teachings (and Figure 7-7’s disclosures), that pads should be evenly spread. Ex.2011 206:1-16; Saint 145-147, 193; POR 68; Ex.2010 ¶¶139-144. A POSITA would not separate the pads in Figure 7-7 to create the claimed “saved area” in view of Figure 9-21 because there is no room to separate them. Ex.2010 ¶¶139-150.

No one disputes that POSITAs wanted smaller chips. Reply 34-35. But Petitioner never establishes why adding a “saved area” to Saint Figure 7-7 and Yoshinaga Figure 6 would reduce size. While Figure 9-28 had “wasted space,” both Saint Figure 7-7 and Yoshinaga Figure 6 do not. They are described as being “as

small as possible,” even without a “saved area.” Yoshinaga [0084]; Saint 147 (describing Figure 7-7 as having a “small ... area” with a “smaller” chip). Because both are already as small as possible, adding a “saved area” would only increase—not decrease—chip size. Ex.2010 ¶¶107-109, 148-150.

Petitioner fails to identify any reference teaching the claimed “saved area” and fails to supply an adequate motivation to create it in Yoshinaga and Saint. Grounds 1-3 must fail.

IV. Grounds 1-3 do not render obvious the claimed “plurality of pad groups” “adjacent and connected to the plurality of ESD buses”

Petitioner asserts the “ground pad *labels* are not shown, not that ground pads are missing” in Yoshinaga Figure 6. Reply 18 (original emphasis). But Yoshinaga states ground pads “are not shown” in Figure 6, so Figure 6 does not depict ground pads, let alone pads “adjacent” to ESD buses. Yoshinaga [0078]. As Dr. Foty explains, “Fig. 6 is merely an illustrative rendering[.]” Ex.1003 ¶136. Accordingly, Figure 6 cannot establish pad adjacency to ESD buses.

PO’s reading is consistent with Yoshinaga and not “divorced from the context,” as Petitioner claims. Reply 18. In Yoshinaga, “not shown” means not depicted, not merely unlabeled. POR 22-23 (citing Yoshinaga [0084] (Figure 6 does not depict “previous ESD protective elements” because they are “provided in the underside”), [0066] (“internal circuit reference potential terminal 44” and “signal terminal 46”

are “not shown” in Figure 4)). Petitioner does not explain why “not shown” means “not labeled” for ground pads but something different in the other cited passages.

Petitioner's reliance on Figures 1-4 fares no better. Reply 19. Petitioner's expert conceded these topological figures “ha[ve] nothing to do with any physical location” and thus cannot supply the missing disclosure of adjacency. Ex.2011 168:4-169:10.

A. Reassigning Yoshinaga's ground pads to be adjacent to its ESD buses was not obvious

Having failed to show adjacency, Petitioner claims a POSITA would reassign pads to create the claimed adjacency for three reasons. Reply 19-23. None withstands scrutiny.

First, Petitioner asserts that Yoshinaga's pads are identical. *Id.* 19. They are not. Even if fabricated from the same material, ground and supply pads have “fundamentally different” functions “and serve entirely different purposes.” POR 23; Ex.1038 204:25-205:23; Ex.2010 ¶¶43-65. Petitioner conflates pad material (not at issue) with pad function. Its citations to Saint Figures 7-1 and 7-2, Ex.2013, and datasheets (Exs.1032-1036)⁵ likewise do not rebut that flexibility in pad assignments

⁵ These references show pad count varies due to functionality differences. *Compare* Ex.1035 28 (40-pad chip not supporting T2OUT feature), *with* 29 (44-pad chip supporting T2OUT feature).

is still constrained by electrical needs. POR 23-27; Ex.2010 ¶45. As Dr. Foty testified, too few supply pads can cause “operating problems.” Ex.2011 151:13-20. Dr. Khatri likewise explained that pad assignments are not fungible and that, given Yoshinaga’s electrical needs, a POSITA would not change pad assignments as Petitioner proposes because doing so would drastically reduce power and cause “operating problems.” Ex.2010 ¶¶45-56.

Second, Petitioner invokes caselaw that a “known technique” need only be a suitable option. Reply 19-20.⁶ But Petitioner’s proposed pad reassignment is not suitable. Dr. Khatri demonstrated that such changes would create power issues by replacing supply pads and eliminate needed signal pads, slowing speeds and causing inoperability. Yoshinaga [0008]; Ex.2010 ¶¶46-56. Such changes are “inappropriate for an obviousness inquiry” when they render the reference inoperable for its intended purpose. *In re Fritch*, 972 F.2d 1260, 1265 n.12 (Fed. Cir. 1992); *Medtronic, Inc. v. Teleflex Innovations S.a.r.l.*, 69 F.4th 1341, 1348-50 (2023). The same principle applies as in *Polaris Industries, Inc. v. Arctic Cat, Inc.*, where the change “render[ed] the vehicle less stable[.]” 882 F.3d 1056, 1069 (Fed. Cir. 2018). Likewise, Petitioner never bridges the gap between a “well-known” ability to

⁶ Petitioner cites this “known technique” caselaw for using “jumper bondwires,” not for modifying Yoshinaga’s pad assignments. Reply 21.

reassign pads and any “beneficial application” to Yoshinaga’s Figure 6, just like in *FanDuel, Inc. v. Interactive Games LLC*, 966 F.3d 1334, 1344 (Fed. Cir. 2020). Nor does it show why a POSITA “would have made the specific design choice” to relocate ground pads into supply and signal locations, just as the petitioner failed in *Cutsforth, Inc. v. MotivePower, Inc.*, 636 F. App’x 575, 578 (Fed. Cir. 2016). Thus, Petitioner’s distinctions of PO’s cases (Reply 22) fail.

Third, Petitioner introduces, for the first time in Reply, four supposed motivations for modifying Yoshinaga’s pad assignments. Reply 22-23 (citing Pet. 46-50). These new arguments should be rejected. *See Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016). In any event, none of these rationales pertain to altering pad assignments. The first—Yoshinaga’s ground-pad electrical connections—says nothing about converting supply pads into ground pads. Reply 22-23. The second and third—supposed general knowledge of pad-to-pad bonding wires and “minimizing bondwire distances”—do not explain why a POSITA would reassign pad functions in Yoshinaga. *Id.* The fourth—preserving a “saved area”—fails because Yoshinaga does not teach any “saved area.” *Supra* §III; POR 40-45, 66-70. A POSITA would not preserve what does not exist.

Petitioner's "core-limited" versus "pad-limited" argument is similarly irrelevant. Reply 23. Even assuming Yoshinaga is "core-limited,"⁷ electrical and layout constraints still apply, and the proposed reassignments would degrade operability. POR 23-27; Ex.2010 ¶¶41-71.

B. Petitioner's proposed modifications were not suitable options

Petitioner's attempt to dismiss PO's concerns about its modified pad assignments fails. Reply 23-25.

First, Petitioner argues that the '164 patent identifies no disadvantages of placing ground pads near saved areas. *Id.* 23-24. That is irrelevant. Obviousness is determined "at the time the invention was made," not in view of "[t]he inventor's own path." *Millennium Pharms., Inc. v. Sandoz Inc.*, 862 F.3d 1356, 1367 (Fed. Cir. 2017). In view of Yoshinaga, a POSITA would have no motivation to assign supply pads into ground pads. POR 19-27.

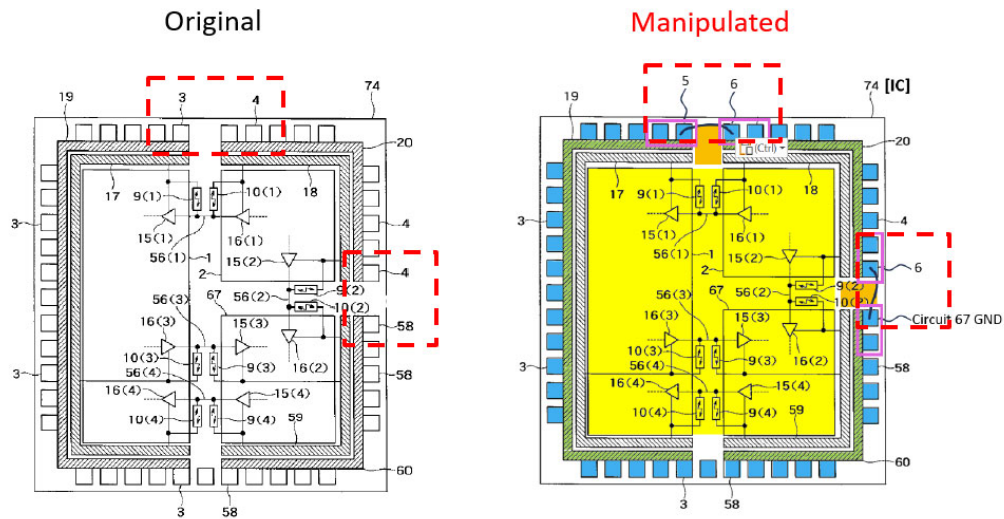
Petitioner argues there is "more disclosure from the prior art than the Challenged Patent." Reply 24 n.5. Not so. The '164 patent labels ground pads and shows their adjacency to a common ESD bus. '164 patent 3:6-16, Figs. 2-3;

⁷ Dr. Foty admits Yoshinaga does not say if it is core or pad limited. Ex.2011 66:12-69:2. Figure 6 does not show ground pads and thus may be pad-limited. Yoshinaga [0078].

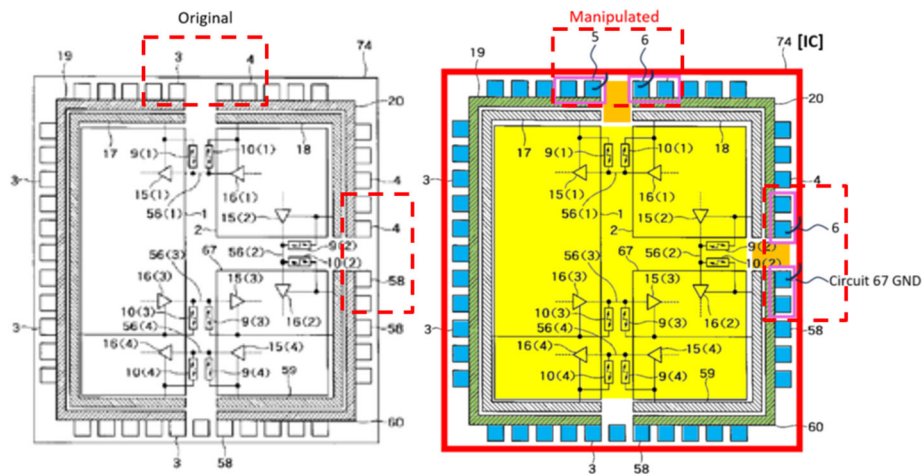
Ex.2017 37:4-10. Yoshinaga Figure 6 does not disclose the ground pads' locations, let alone the claimed adjacency to ESD buses. Yoshinaga [0078]. Thus, the '164 patent discloses *more than* Yoshinaga on ground pad location relative to ESD buses.

Second, Petitioner argues that if it had removed (instead of reassigned) power pads, modified Figure 6 would show fewer pads, but it does not. Reply 24. Yet, Petitioner's own manipulations show fewer power pads but the same overall pad count. So any reassignment contemplated by the Petition did not include reassigning supply pads.

Ground 1 Manipulations



Ground 2 Manipulations



Even in Reply, Petitioner does not identify where the removed supply pads are allegedly reassigned—indeed, they were not. Dr. Foty confirmed that pads 3, 4, and 58 are supply pads and that unlabeled pads must be something else. Ex.2011 145:12-146:19. Yet Petitioner labels only six supply pads while keeping the same total pad count in its modifications. Ex.2010 ¶48. It effectively removes supply pads

(and one in/out pad) by relabeling them as ground, without showing where a POSITA would relocate them. As the “master of its complaint,”⁸ Petitioner’s own proposed modifications control; it cannot use its Reply to change theories to relocate—rather than effectively remove—supply pads. *Acceleration Bay, LLC v. Activision Blizzard Inc.*, 908 F.3d 765, 775 (Fed. Cir. 2018) (rejecting new obviousness arguments not raised in Petition).

Even if Petitioner had argued reassignment of supply pads, it still fails on the merits. Pads are not fungible. Ex.2010 ¶¶45-57; Saint 187. A POSITA would not repurpose any pad as a supply pad without a careful electrical analysis, which the Petition and Reply lack. Ex.2010 ¶¶45-57; Saint 187. As Dr. Foty testified, pad placement is based on the circuit’s needs. Ex.2017 27:22-28:13 (number of pads is based on what “the circuitry [is] doing”), 29:3-8 (same).

Third, the POR explained that Petitioner’s modifications removed 40% of Yoshinaga’s power supply pads. POR 23-27. But Petitioner never explains how Yoshinaga would remain operable with fewer power-supply pads. Instead, it speculates the chip would “function fine” because “many designs/chips function fine” with fewer pads. Reply 25. That generalization does not apply here and

⁸ The fact that Petitioner’s expert discussed reassignment at his deposition (Reply 25), is irrelevant to whether it was disclosed in the Petition.

contradicts both experts. Ex.2010 ¶¶48-49; Ex.2011 69:11-72:11 (testifying a POSITA would not add unnecessary components); Ex.1042 ¶40 (admitting that in a “core-limited pad arrangement,” “unnecessary pads” are removed); Ex.2017 29:9-30:1 (same). A POSITA would read Figure 6 as depicting the necessary supply pads; changing four of them without adding more (as Petitioner proposes) would impair operability. Ex.2010 ¶¶46-49. Petitioner's failure to modify based on electrical needs shows hindsight.

Fourth, Dr. Foty's view that a POSITA “mak[es] the pad assignments first and then lay[s] out the blocks” (Ex.1042 ¶158), contradicts his testimony that pad assignments are adjusted to group pads with corresponding circuitry and ESD rails. Ex.2011 224:8-225:3. Saint likewise depicts changing pad assignments based on the circuit needs, not moving blocks to match pads. Saint 145-148. This supports that Yoshinaga Figure 6 included supply pads based on the circuit needs. Ex.2010 ¶¶46-60, 64-65, 69. Thus Petitioner's relocation of those supply pads impairs operability. *Id.*

C. Ground 3 fails to render obvious a “common ESD bus” or connecting the “plurality of ESD buses”

Ground 3 fails because Saint's Figure 7-7 uses multiple, distinct grounds, teaching away from shorting them into a common ESD bus. POR 60-64. Petitioner recasts GND1/GND2/GND3 as one and the same “voltage,” i.e., a single ground. Reply 13-16. That is an impermissible new argument first raised in Reply, and

contradicts its expert's prior testimony, who identified Figure 7-7 as having "three separate power supply and three separate ground lines," as opposed to Case Study Figure CS1-99's "single ground rail." Ex.1003 ¶¶359-360. This is not about "abstraction levels" (Reply 16); it is a fundamental architectural distinction that defeats Ground 3. The Board found this distinction had "merit" when questioning whether a POSITA would modify Figure 7-7 using Saint's ESD Ground Wiring or Haralabidis's common ground teachings to form a "common ESD bus" (claims 1-5, 8-11) or connect the "plurality of ESD buses" (claims 6-7, 12-14). ID 31-34.

Saint does not disclose a single common ground in Figure 7-7; GND1, GND2, and GND3 are separate references. Ex.2010 ¶¶124-126. Figure 7-7 evolves from Figures 7-3 through 7-6, where some pins are protected to VCC2/GND2 and others to VCC3/GND3, reflecting distinct ground and VCC rails for different signal groups. *Id.*; Saint 145-148. If all grounds were the same signal, there would be no reason to group them together from Figure 7-6 to Figure 7-7—ESD behavior would be uniform—contrary to Saint's rationale for grouping distinct reference signals to improve ESD protection. Ex.2010 ¶¶124-126; Saint 145-148. If Petitioner were right, Figure 7-7 would look different; the GND1/GND2/GND3 would be shown to be connected (which they are not).

Petitioner's analogies of Saint Figure 7-7 to Saint Case Study 1, Figure 6-2, and Haralabidis all fail. Reply 14-16. The Saint Case Study figures it cites (e.g.,

CS1-1 and CS1-87), disclose a single, common ground with separate VCC rails, confirmed by CS1-86 and CS1-84 identifying “GND (common).” Saint 320-321; Reply 15-16. Haralabidis likewise addresses segmented rails within a single ground, not multiple different ground references as in Figure 7-7. Ex.2010 ¶¶129; Ex.1007 3:9-21, 3:34-40, 3:65-4:12. And Saint’s Figure 6-2 (Reply 14), does not suggest Figure 7-7’s GND1/GND2/GND3 are the same signal. It is a separate embodiment depicting a guard band with substrate contacts to reduce “traveling noise” from a “noisy block.” Saint 126-127. By contrast, Saint Chapter 7 discusses moving previously separate reference lines “close to each other,” not connecting them into one ground. Ex.2010 ¶¶124-126; Saint 147.

Saint’s Figure 7-7 teaches away from a single common ground by optimizing ESD protection around multiple, distinct ground references, and corresponding VCC rails. Saint 147-148; Ex.2010 ¶¶124-129. Where the prior art teaches away, the taught-against feature is not a “suitable option” and is not obvious. *See Millennium Pharms.*, 862 F.3d at 1366. Because Figure 7-7 teaches away from adding a common ground rail, Petitioner’s proposed modification fails. POR 60-64; ID 33-34.

Petitioner’s cited cases (Reply 16-17) are inapposite. Unlike the proposed modification in *Intel Corp. v. PACT XPP Schweiz AG*, adding a common ground rail would not be a “suitable option” because Saint Figure 7-7 is incompatible with—and teaches away from—a common ground. 61 F.4th 1373, 1381 (Fed. Cir. 2023);

Ex.2010 ¶¶126-129. *Purdue Pharma L.P. v. Accord Healthcare Inc.*, is also inapposite as a nonprecedential district court decision, and because the prior art there did not teach away. 2024 WL 4120717, at *19 (D. Del. Sept. 9, 2024). Here, Figure 7-7 expressly discourages shorting the three separate signals to a common ground because separate signals “keep parasitics down, and keep cross talk down from one supply to another.” Saint 147. Shorting them would inject noise and defeat the design, thereby “counsel[ing] against a motivation to make such modifications.” *Medtronic*, 69 F.4th at 1348-50.

Petitioner fails to identify any reference teaching the claimed pad groups “adjacent and connected” to “ESD buses” or to supply an adequate motivation to modify Yoshinaga and Saint to do so. Grounds 1-3 must fail.

V. Grounds 1-3 do not render obvious the claimed “bonding wire” connections

A. Yoshinaga’s connection techniques contradict using pad-to-pad bonding wire connections

Yoshinaga’s reference to a “semiconductor integrated circuit” confirms that the pad-to-pad connections shown in Figures 1-2 and 4 are implemented by integrated circuit metallization. Ex.2010 ¶¶74-77; Yoshinaga Abstract, [0087]. Dr. Foty agreed: when asked about “the wires depicted in Figure 1” (not pad-transistor connections)—including wires between pads 5 and 6—he confirmed such wires

“would be comprised of the integrated circuit metallization in some way, shape, or form.” Ex.2011 164:18-165:14. While Figure 2 is a separate embodiment from Figures 1 and 6, it employs the same metallization connections. *See* Ex.2010 ¶¶91-93; Ex.1003 ¶130; Yoshinaga [0087].

Petitioner claims Figure 6's lack of connection between lines 19, 20, and 60 contradicts Dr. Khatri's and Dr. Foty's testimony. Reply 4. Not so. Dr. Foty admitted Figure 6 does not depict pads' “specific electrical connections.” Ex.1003 ¶136. Those connections appear in Figures 1-4, which depict pad connections through integrated circuit metallization or diodes.⁹ Ex.1003 ¶143; Ex.2010 ¶¶73-77.

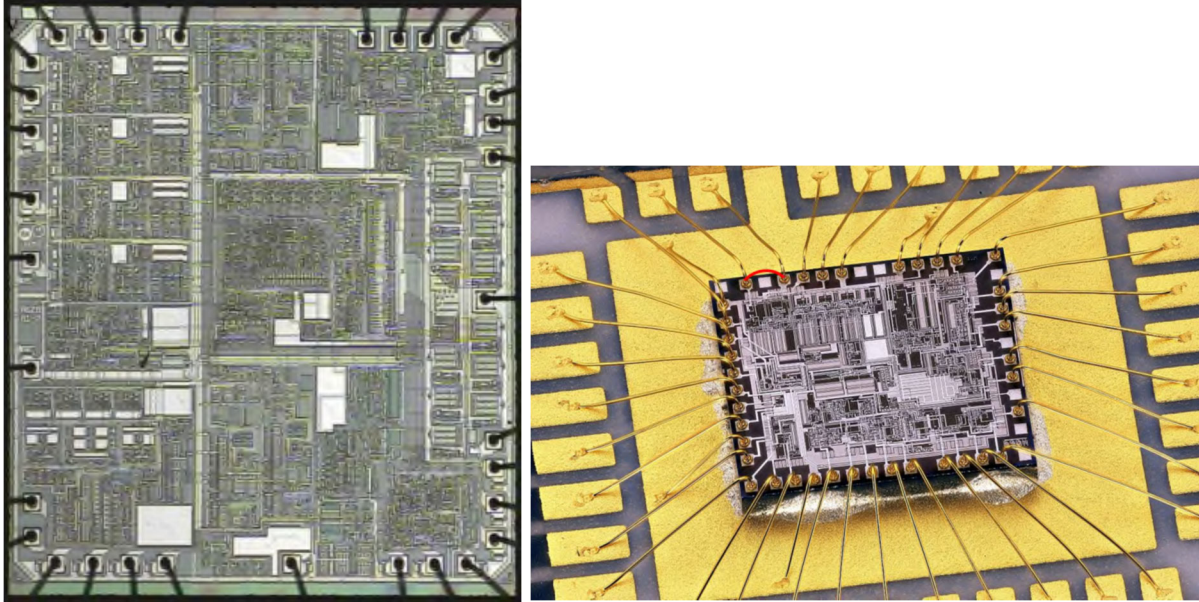
Petitioner incorrectly ignores Yoshinaga Figure 3. Reply 2-3. “[A] reference must [be] considered for all it taught.” *Polaris*, 882 F.3d at 1096 (second alteration in original). Yoshinaga teaches using bidirectional diodes to connect pads through line 41 to “avoid noise.” Yoshinaga [0061]. Adding bonding wire between pads 5 and 6 would be redundant because Yoshinaga already employs integrated circuit

⁹ Petitioner argues for the first time in Reply that there are only a finite number of connection options. Reply 4; Ex.2010 ¶85 (noting the Petition never established “there are only a finite, small or easily traversable number of options for connecting pads”). Such new arguments must be rejected. *See Intelligent Bio-Systems*, 821 F.3d at 1369.

metallization or bidirectional diode connections. *See In re Anova Hearing Labs, Inc.*, 809 F. App'x 840, 843 (Fed. Cir. 2020) (reversing obviousness when modification was redundant of features already included); Ex.2010 ¶¶86-94.

B. Bonding wire was not a suitable pad-to-pad connection option

Shorting, inductance, and exposure risks made bonding wire unsuitable for pad-to-pad and pad-to-common ESD bus connections. POR 37-39, 51-56. Petitioner's Reply cites no new art to the contrary, instead invoking Dr. Khatri's bonding wire experience to downplay bonding wire's inductance and parasitic concerns. Reply 5-7. But it omits critical context: Dr. Khatri's experience concerns pad-to-package connections—where bonding wire is often the only practical option—not pad-to-pad. Ex.1038 152:7-154:17. Petitioner's statistics, Saint's Figure 9-2, and Dr. Foty's circuit images (below) similarly address pad-to-package, not pad-to-pad, bonding wire connections. Reply 5-6, 8-9; Saint 202-203; Ex.1043 1 (describing “chip to package or chip to board” connections); Ex.2017 23:11-17, 100:16-21.



Ex.1042 ¶¶18, 70. Consistent with Yoshinaga, Saint and Dr. Foty's images (above), pad-to-pad connections in integrated circuits use on-circuit metallization (unavailable for pad-to-package) to avoid bonding wires' "fatal" shorting and inductance problems.¹⁰ Ex.1038 141:3-154:17; Ex.2012 296; Ex.2010 ¶¶73, 86-89; *supra* §III.B.

Petitioner's additional references do not establish that pad-to-pad bonding wire was a known, suitable option. Reply 6-7. Beddingfield uses "jumper wire[s]" to connect a pad with inner circuitry, not other pads, to form an additional path parallel to the on-chip metallization connections. Ex.1041 [0015], [0022], Figs. 2-4;

¹⁰ Petitioner's expert relies on a website (not cited as an Exhibit) that emphasizes bonding wires' "[h]igher inductance." Ex.1042 ¶110.

Ex.2017 82:9-85:20. Lee addresses RFID tags on a single layer substrate, unlike the multi-layer integrated circuits in Yoshinaga and Saint. Ex.1039 Abstract; Ex.2017 87:2-12. Conner concerns bonding wire connections to bond fingers on flex substrates and PCBs, not on-chip pad-to-pad connections. Ex.1040 Figs. 4-6, 2:30-35, 3:37-50; Ex.2017 90:10-94:3.

None of these shows a POSITA would deem pad-to-pad bonding wire suitable for multi-layer integrated circuits like Yoshinaga or Saint. As Dr. Khatri testified, it was a “non-starter” and “not even an option” due to shorting, exposure, and inductance. Ex.1038 224:16-226:25; *see also id.* 138:21-140:14; POR 37-39; Ex.2010 ¶¶73-95. Using bonding wire for pad-to-pad connections despite those risks was an “inventive feature” that went “against conventional wisdom” before the ’164 patent. Ex.1038 224:16-226:25, 246:3-250:22, 253:21-255:6.

C. Petitioner misunderstands PO's Ground 2 arguments

Petitioner's Ground 2 arguments rest on misreadings of the record.

First, Dr. Foty's testimony contradicts Petitioner's argument that Haralabidis discloses the claimed bonding wire connection between pads and a common ESD bus. Ex.2011 243:9-11, 244:4-15 (admitting Haralabidis does not disclose “bond pads” or methods “to connect from the inside [of] the IC of the package substrate”).

Second, PO is not asserting that Petitioner proposes “adding” bonding wire to Figure 3. Reply 10-11. Rather, Yoshinaga teaches an integrated, on-chip ESD

solution; adding an external bonding wire connection to a common ESD would be redundant such that Yoshinaga teaches away from doing so. *See South-Tek Sys., LLC v. Engineered Corrosion Sols., LLC*, 748 F. App'x 1003, 1006-07 (Fed. Cir. 2018) (finding claims non-obvious because “South-Tek only argued that a person of ordinary skill would have been motivated to use Wood’s drain to allow water to drain from Viking’s system. ***Viking’s system already includes a drum drip drain that serves this purpose.***”) (emphasis added).

Third, even setting aside Figure 3, Yoshinaga already provides sufficient ESD protection. As Dr. Khatri explained, and Petitioner does not refute, Figure 6 describes a compact and efficient ESD protection approach that eliminates the need for a common ESD bus. Yoshinaga [0084]-[0086]; Ex.2010 ¶116. Adding a common ESD bus via bonding wire would be redundant, increase noise and parasitics, and introduce inductance and reliability risks. Ex.2010 ¶¶113-119.

Fourth, Petitioner asserts that it is enough that Haralabidis discloses connecting bonding wire to ESD buses and Saint discloses connecting bonding wire to pads to establish obviousness. Reply 12. But Petitioner cites no legal authority for that proposition. Nor could it. The law requires more than the existence of “general use” of bonding wire to connect pads to a common ESD bus in the prior art; it demands an adequate “motiva[ion] to add” bonding wire connections between pads

and a common ESD bus in Yoshinaga. *FanDuel*, 966 F.3d at 1343-44. Petitioner provides none. POR 29-39.

D. Ground 3 fails for similar reasons as Grounds 1-2

Petitioner's only additional Ground 3 argument is that Saint's on-chip focus and Haralabidis's off-chip focus justify combining them. Reply 12-13. But Saint Figure 7-7 teaches three separate grounds that already provide adequate ESD protection, leaving no reason to modify Saint. Ex.2010 ¶¶134-138, 149. Shorting those grounds to a common ESD bus with bonding wire would defeat Figure 7-7's purpose of "keep[ing] parasitics" and "cross talk" down. Saint 147; Ex.2010 ¶149; *Medtronic*, 69 F.4th at 1349-50 ("it was error for the Board to ignore evidence that a proposed modification would interfere with a reference's stated purpose").

Petitioner has not shown that a POSITA would be motivated to use bonding wire to connect pad-to-pad or to a common ESD bus in Yoshinaga or Saint, or that doing so would be a suitable option. Accordingly, Grounds 1-3 fail.

VI. Conclusion

For the reasons above, the Board should find claims 1-14 nonobvious.

Respectfully submitted,

Dated: January 21, 2026

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CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Patent Owner's Sur-Reply complies with the word count limitation of 37 C.F.R. § 42.24(c)(4) because the Patent Owner's Sur-Reply contains a total of 5,599 words, which is the sum of 5,579 words calculated by using Microsoft Word's word-count feature and 20 words hand-counted in the figures. This total excludes the cover page, signature block, and the parts of the Patent Owner's Sur-Reply exempted by 37 C.F.R. § 42.24(c).

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 21st day of January, 2026, a true and correct copy of the foregoing **Patent Owner's Sur-Reply and Exhibit 2017** were served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

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