

1 UNITED STATES PATENT AND TRADEMARK OFFICE
2 BEFORE THE PATENT TRIAL AND APPEAL BOARD
Case IPR2025-00118, Patent 10,879,164

3 MICRON TECHNOLOGY, INC.,

4 Petitioner,

5 vs.

6 YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

7 Patent Owner.

8 _____/
V/C DEPOSITION OF: DANIEL FOTY, Ph.D.

9
10 TAKEN: Pursuant to Notice by
Counsel for Patent Owner

11 DATE: January 9, 2026

12 TIME: 6:04 a.m. to 8:54 a.m. PST

13 LOCATION: Witness's Residence
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Fletcher, Vermont 05444

15 VIA: Zoom Videoconferencing

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S T I P U L A T I O N S

It is hereby stipulated and agreed by and between the
counsel for the respective parties and the witness
that the reading and signing of the deposition
transcript be reserved.

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1	I N D E X	
2	EXAMINATION OF DANIEL FOTY, Ph.D.: January 9, 2026	PAGE
3	DIRECT EXAMINATION BY MR. WATSON	6
4	CERTIFICATE OF OATH	104
5	CERTIFICATE OF REPORTER	105
6	DEPOSITION ERRATA SHEET	106
7	DEPOSITION ERRATA PAGE #1	107
8	DEPOSITION ERRATA PAGE #2	108
9		
10		INITIAL
11	DEPOSITION EXHIBITS	REFERENCE
12	Exhibit 1001 United States Patent	35
13	No. 10,879,164 dated 12/29/20	
14	by Applicant: Yangtze Memory	
	Technologies Co., Ltd.;	
	Inventor: Zhiguo Li, Wuhan	
15	Exhibit 1003 Declaration of Dr. Daniel Foty	13
16	in Support of Petition for	
17	Inter Partes Review of U.S.	
	Patent No. 10,879,164 dated	
	11/14/24	
18	Exhibit 1008 McGraw-Hill Professional	62
19	Engineering - IC Mask Design	
20	Essential Layout Techniques, by	
	Christopher Saint & Judy Saint	
21	Exhibit 1039 United States Patent No.	86
22	6,424,263 B1 dated 7/23/02,	
	Lee et al.	

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I N D E X (Continued)

DEPOSITION EXHIBITS	INITIAL REFERENCE
Exhibit 1040 United States Patent No. 7,375,978 B2 dated 5/20/08, Connor, et al.	88
Exhibit 1041 United States Patent Application Publication No. 2007/0029661 A1 dated 2/8/07, Beddingfield, et al.	80
Exhibit 1042 Reply Declaration of Dr. Daniel Foty in the Micron Technology, Inc., vs. Yangtze Memory Technologies Company, Ltd., case dated 12/23/25	11

PREVIOUSLY MARKED DEPOSITION EXHIBITS: (None)	INITIAL REFERENCE
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QUESTIONS WITNESS INSTRUCTED NOT TO ANSWER
(None)

INFORMATION TO BE PROVIDED
(None)

1 P R O C E E D I N G S

2 *****

3 THE CONCIERGE: Thank you to everyone for
4 attending this proceeding remotely, which we
5 anticipate will run smoothly.

6 Please remember to speak slowly and do your
7 best not to talk over one another. Please be aware
8 that we are recording the proceeding for backup
9 purposes.

10 Any off-the-record discussions should be had
11 away from the computer. Please remember to mute your
12 mic for those conversations. Please have your video
13 enabled to help the reporter identify who is speaking.

14 If you are unable to connect with video and
15 are connecting via phone, please identify yourself
16 each time before speaking.

17 We will provide a complimentary recording of
18 this deposition with the purchase of a transcript. I
19 apologize in advance for any technical related drops.

20 Thank you.

21 THE COURT REPORTER: Would you raise your
22 right hand, please.

1 Do you solemnly swear or affirm that the
2 testimony you're about to give in this cause is the
3 truth, the whole truth, and nothing but the truth?

4 THE WITNESS: Yes, I do.

5 THE COURT REPORTER: Thank you kindly.

6 You may proceed.

7 DIRECT EXAMINATION

8 BY MR. WATSON:

9 Q. Good morning, Dr. Foty.

10 A. Good morning, Counselor. I guess it's very
11 early where you are. Thank you for getting up so
12 early for this.

13 Q. It is. Can you please state your full name
14 for the record.

15 A. Sure. My name is Daniel Patrick Foty, spelled
16 F-o-t-y, Foxtrot, Oscar, Tango, Yankee.

17 Q. And can you please state your home address for
18 the record.

19 A. It's the same as the one I just described.
20 452 Black Mountain Road. Physical location is
21 Fletcher, Vermont. Mailing address would be
22 Cambridge, Vermont, due to a lack of a post office in

1 Fletcher.

2 Q. And where are you located right now?

3 A. Oh, that's the location where I am right now.

4 Q. Do you understand that your testimony today is
5 under oath and under penalty of perjury?

6 A. Yes, I do.

7 Q. And is there any reason you cannot provide
8 full and truthful testimony today?

9 A. Not that I'm aware of, no.

10 Q. Based on what I can see, it does not look like
11 you have any materials with you today; is that
12 correct?

13 A. No. Actually, you can't see it, but I have
14 clean copies of all the documents, a clean copy of my
15 Declaration. I have some -- I just have some blank
16 Post-it notes in case I need to use bookmarks, and I
17 have also -- since I have a copy of it, I have my
18 clean copy of Saint in book form, if it's easier for
19 me to look in the book than rummage through the
20 binders.

21 Q. So for the record, can you just describe which
22 clean documents you have in front of you.

1 A. Sure, I'll do my best. It's the -- the -- I
2 guess the executive summary would be that it's all the
3 exhibits and copies of my Declaration and the
4 materials from our prior go-around several months ago.

5 So I have on my desk here a clean copy of my
6 Declaration, again, to make it easier for me to --
7 you know, to -- to find things rather than poking
8 around on the screen.

9 Q. When you say "the exhibits," which exhibits
10 are you referring to?

11 A. This is the list of exhibits in my Declaration
12 of things, like, the -- the various references that
13 were cited and -- and things of that nature that were
14 not in the or -- the exhibits of the first deposition
15 back a few months ago.

16 I also have copies of your materials and your
17 exhibits from the POR.

18 Q. Do you have any materials with you, other than
19 the materials you've cited in your Declaration?

20 A. Well, assuming you're not counting my coffee.
21 I assume you mean these materials for this matter.
22 That's all I have. If anything strange happens, I'll

1 let you know, but all of them are clean. There's no
2 marks on them.

3 Q. And is there anyone else in the room with you?

4 A. No humans, just cats. They may, as you know,
5 make an appearance.

6 Q. Okay. And can -- can you agree that during
7 this deposition, you will not open any of these
8 documents, aside from those that we've provided and
9 discussed?

10 MR. JENSEN: Object to form.

11 THE WITNESS: Well, I have the documents
12 for -- from all these matters, so I may go to a
13 document if you ask me a question without citing a
14 document, for example, but other than that, I'll just
15 use those documents as necessary and as I see fit.

16 BY MR. WATSON:

17 Q. Can you agree with me, then, to not refer to
18 any documents that you don't have with you at this
19 moment? Is that fair?

20 MR. JENSEN: Object to form.

21 THE WITNESS: I don't think there's any
22 missing, but if something comes up and it's missing,

1 I'll let you know.

2 As far as I know, my paper copies are
3 complete, but, of course, you know, there may be
4 something that didn't get in the mix.

5 BY MR. WATSON:

6 Q. Okay. Now, what did you do to prepare for
7 your deposition today?

8 A. Oh, I reviewed my materials over the past few
9 weeks as time permitted over the holiday, and I had
10 two sessions with Mr. Jensen this week.

11 Q. Okay. And about how long were those meetings
12 with Mr. Jensen?

13 A. Hmm. Each one was two, two and a half hours.

14 Q. Uh-huh. Have you discussed your deposition
15 with anyone, other than Mr. Jensen?

16 A. I don't think so. I think it was just -- I
17 worked with Mr. Jensen, so that was the only person
18 I'd need to discuss this with.

19 MR. WATSON: By the way, Counselor, your --
20 your signal on my end is blinking yellow and red, so I
21 don't know if you've got -- now it's white again, so
22 you may have a signal issue, just to let you know.

1 MR. JENSEN: Thank you.

2 MR. WATSON: Could we pull up Exhibit 1042.

3 BY MR. WATSON:

4 Q. And I'll -- I'll have this on the screen, but
5 you can pull up your own copy as well, Dr. Foty.

6 A. Yep. I have my copy here to my left, which on
7 the screen looks like my right.

8 THE CONCIERGE: Counselor, do you want me to
9 drop it in the chat as well; is that correct?

10 MR. WATSON: Sure, but I think he has a
11 physical copy, so he can -- he can refer to whichever
12 one he -- he prefers.

13 (Deposition Exhibit 1042 was marked for
14 identification.)

15 THE CONCIERGE: You have control now, Counsel.

16 BY MR. WATSON:

17 Q. Dr. Foty, do you have Exhibit 1042 in front of
18 you?

19 A. I have my paper copy, and I have the one you
20 put up on the screen, and they appear to be identical.

21 Q. Okay. Exhibit 1042 is the Reply Declaration
22 you provided in case number IPR2025-00118, correct?

1 A. That app- -- that is correct. That appears to
2 be what we have in front of us.

3 Q. And to make it easier in this deposition, if I
4 refer to "this case" or "this proceeding," will you
5 understand that I'm referring to IPR2025-00118?

6 A. I'll understand that. And, of course, if you
7 stick to that, it'll be easy. If, for some reason, I
8 think that the language has deviated, I'll -- I'll
9 ask.

10 Q. Perfect. Thank you.

11 Now, Dr. Foty, you prepared -- you've prepared
12 two declarations in relation to -- well, strike that.

13 Dr. Foty, Exhibit 1042 relates to U.S. Patent
14 Number 10,879,164, correct?

15 A. That is correct, yes.

16 Q. And for purposes of this deposition, if I
17 refer to the "'164 patent," you'll understand I'm
18 referring to the -- the U.S. Patent 10,879,164. Okay?

19 A. Yes. To my knowledge, there's no other
20 mat- -- other reference with the same number, which I
21 did have happen once. So if you say "'164," I believe
22 that's the only '164 that is even involved here, so

1 that's helpful.

2 Q. Now, you've prepared two declarations in
3 relation to the '164 patent, correct?

4 A. That is correct, yes.

5 MR. WATSON: Let's pull up Exhibit 1003.

6 THE CONCIERGE: All right. Stand by.

7 (Deposition Exhibit 1003 was marked for
8 identification.)

9 BY MR. WATSON:

10 Q. Dr. Foty, Exhibit 1003 was the Declaration you
11 submitted in this proceeding back in November of 2024,
12 correct?

13 A. Yes, that appears to be the case. And I have
14 my paper copy of that from our last go-around with me
15 as well.

16 Q. Would it be okay if we refer to this
17 Declaration as your Original Declaration, for purposes
18 of this deposition?

19 A. Original Declaration or Opening Declaration.
20 I believe, in my reply, I -- I refer to it as the
21 "Opening Declaration," so if -- again, if I'm
22 confused, I'll ask.

1 Q. Okay. If -- if -- if I use the term "Opening
2 Declaration," you'll understand I'm referring to
3 Exhibit 1003, correct?

4 A. Yes, I'll assume that, unless I -- something
5 seems strange, in which case, I'll -- I'll say
6 something.

7 Q. Okay. All right.

8 MR. WATSON: Let's pull back up Exhibit 1042.
9 BY MR. WATSON:

10 Q. Exhibit 1042's the Declaration you submitted
11 this year, in December of 2025, correct?

12 A. Well, technically that's last year, but it was
13 December 23rd or something like that it was sub- -- it
14 was filed with the -- the package.

15 Q. Okay. And is it okay if I refer to
16 Exhibit 1042 as your "Reply Declaration"?

17 A. That should be fine. And, again, if I think
18 that there's something that's gone amiss, I'll -- I'll
19 say something.

20 Q. Is there anything that has come to your
21 attention that you would like to correct in your Reply
22 Declaration?

1 A. There are a few minor typos, like a word is
2 misspelled or left out, but other than that, at this
3 point I don't think there's anything in there I need
4 to preemptively correct today.

5 Q. There's nothing substantive that's come to
6 your attention that you'd like to correct in your
7 Reply Declaration?

8 A. Not at this point, no.

9 Q. Okay. And when you were preparing your Reply
10 Declaration, were there any materials that you would
11 have liked to have reviewed but did not have access
12 to?

13 A. I don't believe so. I think I had enough to
14 reach -- to draw a conclusion and form -- conclusions
15 and form opinions.

16 Q. Now, in your Reply Declaration, you're
17 responding to opinions offered by Dr. Khatri, correct?

18 A. In part --

19 MR. JENSEN: Object to form.

20 THE WITNESS: -- yes.

21 Whoops. Sorry. Was there an objection?

22 MR. JENSEN: Object to the form.

1 THE WITNESS: Oh, yes. I saw you go green
2 there. I didn't know if I stepped on you.

3 But to answer the question, I responded in
4 part to Dr. Khatri and in part to the POR that was
5 filed with it.

6 BY MR. WATSON:

7 Q. Apart from your work in this proceeding, do
8 you know Dr. Khatri?

9 A. No, I've never met him, and I don't think I
10 was aware of him until this proceeding.

11 Q. Did you render any opinion on whether
12 Dr. Khatri qualifies as an expert in the subject
13 matter of the '164 patent?

14 A. I offered no opinions regarding that.

15 Q. Okay. Do your Original and Reply Declarations
16 con- -- contain a complete and accurate statement of
17 your opinions regarding the validity of the claims of
18 the '164 patent?

19 A. I believe that they do, yes.

20 Q. Okay. Have any of your opinions regarding the
21 validity of the claims of the '164 patent changed
22 since submitting your Reply Declaration?

1 A. No, they have not.

2 Q. And when was the last time you reviewed your
3 Reply Declaration?

4 A. I did a final quick review last evening.

5 Q. Dr. Khat- -- or, excuse me -- Dr. Foty, can
6 you describe for me the process that you went through
7 in preparing this Reply Declaration, obviously
8 avoiding any -- revealing any privileged information?

9 A. I reviewed the materials, the POR, Khatri's
10 Declaration and his deposition testimony and various
11 exhibits and formed -- reached conclusions and formed
12 opinions and constructed my reply based on doing that,
13 in the conventional way. There was nothing
14 unconventional about how I did this.

15 Q. And did you write the words in your
16 Declaration?

17 A. Yes, I did. I had of course back and forth
18 with counsel, but I wrote this Declaration.

19 Q. Okay. Let's go to Paragraph 18 of your
20 Declaration -- or, actually, let's -- let's go first
21 to -- let's go to Paragraph 4 of your Declaration
22 first.

1 A. (Witness perused document.)

2 Q. Do you have that in front of you?

3 A. Oh, sorry. Yes, I do. I have Paragraph 4 in
4 front of me.

5 Q. Okay. You list a number of materials here in
6 Paragraph 4, including your prior Declaration, the
7 Board's institution material -- or Board -- Board's
8 Institution Decision, Patent Owner's Response, and the
9 exhibits thereto, and the materials listed in
10 Petitioner's Reply, and any other materials cited in
11 this Reply Declaration.

12 You see that?

13 A. Well, I say, "Cited herein," but I assume it
14 means the same thing.

15 Q. Okay. You did not rely on any materials
16 beyond the materials you list in Paragraph 4, correct,
17 in forming your opinions here?

18 A. In terms of the materials, no. Of course, I
19 relied on my own knowledge and experience in preparing
20 this.

21 Q. Okay. All right. Now let's go to
22 Paragraph 18 of your Declaration.

1 A. (Witness perused document.) I have that in
2 front of me, by the way.

3 Q. Okay. There's a photograph that you provide,
4 in Paragraph 18 of your Reply Declaration.

5 What is that a photograph of?

6 A. This is a photograph of a silicon IC or
7 silicon chip, whatever terminology you use. It was
8 put through a teardown, and so that means that layers
9 were removed so that it could be examined in various
10 ways.

11 So this is a re- -- I called it a
12 "reverse-engineering teardown" in order to be able to
13 expose the IC, and in this particular level of the
14 teardown, you can see the wires running into the
15 bond pads.

16 Q. Who performed the teardown shown in this
17 image?

18 A. The teardown was performed by the outfit named
19 at the link below. It's called -- strangely it's
20 called SparkFun. It's actually a pretty serious
21 operation. They tore this down as part of an article
22 that they wrote in 2010 or 2011.

1 Q. Okay. Were you involved in any way in the
2 teardown of this particular circuit?

3 A. No, I was not. I mainly included this photo
4 in my first Declaration to just provide a visual
5 example of the core-limited design. There are
6 other -- other things we can learn from this photo,
7 but that was the principal reason for providing it.

8 Q. Okay. In this photo, there's a black line
9 that surrounds the entire photo.

10 Do you see that?

11 A. (Witness perused document.) I see that, yes.

12 Q. What is that?

13 A. As far as I know, that isn't anything
14 physical; it's just a line that was drawn when the
15 photo was prepared. It -- as far as I know, that's
16 what that is.

17 Q. In this photograph, in Paragraph 18, what are
18 the pads being connected to with the bond -- bonding
19 wire?

20 A. As per conventional practice, the -- those
21 wires go out to the package, and the package has metal
22 traces to which those wires are bonded, and those

1 metal traces essentially are contiguous with the pins
2 of the package.

3 So that the -- as is usual practice in the IC
4 business, the IC is in a package with pins so that the
5 pins can be -- so that the packaged IC, as a product,
6 can be plugged into a circuit board or similar.

7 So those bond wires should be going in the --
8 and the article indicates that's the case -- to the
9 traces, the package traces, which go to the package
10 pins.

11 Q. So in this photograph, in Paragraph 18, the
12 bonding wire connects the pad to the packaging; is
13 that fair?

14 A. I think it has to be more specific. It
15 connects to the package traces, which are the same
16 metal piece as the pins.

17 Q. Got it.

18 So in -- in Paragraph 18, this photograph
19 shows the bonding wire connecting the package traces
20 to the pads?

21 A. Well, this particular photograph doesn't show
22 where they go, but A, it's fairly obvious where they

1 go, and the rest of the article discussed the
2 teardown, and it shows the bond pack- -- wires going
3 out and connecting to package traces.

4 Q. Now, in this photograph, in Paragraph 18, the
5 pads are located on the edges of the chip, correct?

6 A. I believe the term I use is the one of the art
7 "periphery," but I think we mean the same thing.

8 Q. Okay. But the pads are on the periphery of
9 the -- the chip; is that fair?

10 A. Yeah, that's -- that's fair, yes. And I also
11 think I said I believe "periphery" is the term of the
12 art. It's the one I've used forever, so --

13 Q. In this photograph, in Paragraph --
14 Paragraph 18, is there any circuitry beneath the
15 bonding wire?

16 A. (Witness perused document.) Examining the
17 photo here, all the bond wires, in this particular
18 instance, run to package traces, so there does not
19 appear to be any circuitry under the bond wires here.

20 Q. In this figure in Paragraph 18, how are the
21 pads connected?

22 A. Well, the pads are connected to the bond

1 wires, which go to the package traces.

2 Q. Is there any connection on the pads between --
3 or strike that.

4 In this photograph, in Paragraph 18, are the
5 pads connected to each other on the chip?

6 A. That's a difficult question to answer from an
7 engineering point of view, simply because there's not
8 enough detail here to see how things are wired at the
9 IC level, so it's possible that two pads are connected
10 together in here somewhere, but it's just not visible.

11 Q. This figure shown in Paragraph 18 doesn't show
12 a bonding wire connecting the pads together?

13 A. If you mean, Does this photo show or not show
14 a direct connection between two pads using a jumper
15 bond wire, this particular instantiation does not show
16 that, and I did not -- of course, I did not claim this
17 one did.

18 Q. In this photo on Paragraph 18, are the pads
19 connected to each other using metal layers?

20 A. That's a possibility, but at this level of
21 viewing, we can't tell that level of detail. Those
22 features are too small at this -- at this depiction.

1 Q. And in this photograph in Paragraph 18, are
2 there any ESD buses shown?

3 A. Again, at this scale of the figure, we can't
4 see the metal traces at the -- at the IC level. All
5 we can see here is the macro level of the pads and
6 the -- and some block natures of the circuitry, but
7 not at the level -- we'd have to -- you'd have to go
8 to a more detailed ex- -- examination of the IC to
9 look at the -- the metallization at the chip level.

10 Q. Well, you're not aware of there being any
11 ESD buses in this particular photograph, correct?

12 A. I'm not aware of that. And, again, I provided
13 this photo in my Opening Declaration as a
14 demonstration, a -- a real demonstration of a real
15 product that was a core-limited IC.

16 THE WITNESS: Excuse me.

17 BY MR. WATSON:

18 Q. Let's turn to Paragraph 40 of your
19 Reply Declaration.

20 A. 4-0?

21 Q. Yes, 4-0.

22 A. (Witness perused document.)

1 (Pause in the proceedings.)

2 THE WITNESS: Oh, sorry. I have that in front
3 of me on paper as well, Counselor.

4 BY MR. WATSON:

5 Q. Yeah. I want to direct your attention to the
6 last sentence of that paragraph.

7 Do you see that?

8 A. Is this the sentence that begins, "as can be
9 seen," or the one that begins as a partial sentence?

10 Q. It's the one that begins, [as read]:

11 It is thus clear that the depiction of
12 Figure 9-21...

13 Do you see that sentence?

14 A. Hang on. Is it on the following page? Is it
15 actually on Page 24?

16 Q. Yeah, it's on Page 24.

17 A. Okay.

18 Q. But the same paragraph, Paragraph 40.

19 A. Sorry, you can straddle -- on the screen you
20 can straddle pages. Of course, on the paper copy, I
21 can't. I had to turn the page --

22 Q. Of course. Let --

1 A. So you were referring to --

2 Q. Let -- let me know if I -- I don't direct you
3 to the right -- the right spot. I'm happy to -- to
4 clarify.

5 A. Well, I just did, so that helped.

6 Q. Uh-huh.

7 A. But I assume you're not -- you're referring to
8 the final paragraph of -- the final sentence of
9 Paragraph 40, as we see it toward the bottom of the
10 screen here, which begins, [as read]:

11 It is thus clear...

12 Q. Correct.

13 A. Okay.

14 Q. That's the sentence I'm referring to.

15 A. We're finally in the same place, Counselor.
16 Thank you.

17 Q. You say there that, [as read]:

18 This depiction would produce the core-limited
19 pad arrangement by simply removing unnecessary pads
20 from a pad template.

21 What makes a pad "unnecessary"?

22 A. Well, for reference, I actually discuss this

1 entire issue in Section 3, Subsection B,
2 Sub-Subsection 4, which is the issue -- and it's also
3 wonderfully explained by Saint. Saint was 2002.

4 And just for the record, I was aware of this
5 concept prior to 2002 from my own work, but basically
6 what I'm saying there is that the core-limited
7 arrangement occurs when you have so much circuitry
8 that you have more space on the periphery for pads
9 than you need.

10 And so you obviously don't -- you -- you don't
11 put useless pads there, and all I'm showing in this
12 figure is that if you start with a template, as many
13 designers do, you remove those pads.

14 You simply -- and, again, Saint is marvelous
15 for describing this, that you have -- the circuitry
16 requires some number of pads, and you just have more
17 space than you need.

18 So when you're trying to make the chip as
19 small as possible, the limiting factor is the
20 circuitry, not the number of pads around the
21 periphery.

22 Q. What determines the number of -- the pads that

1 you need?

2 A. Basically what is the circuitry doing, and
3 what is the whole chip working together supposed to
4 do? You'd have power pads, ground pads, some signal
5 pads, maybe some other reference pads, but you have
6 the number of pads you need in the product you're
7 developing.

8 The number of pads, which refer, also, to the
9 number of pins on the -- the package. And so you see
10 how many pads you need, see how much circuit area you
11 need, and then you determine if your design is
12 core-limited or pad-limited, and this is a case of a
13 core-limited design we see in front of us.

14 Q. So is it fair to say that the number of pads
15 you need is based on the needs of the circuitry?

16 A. Are you -- are you -- are -- I didn't know if
17 you were going to continue there, Counselor. That's
18 why I didn't respond.

19 Are you finished with that?

20 Q. Yeah.

21 A. Okay. Could I -- could I ask you to repeat
22 it, then? You paused like there was more coming, so I

1 want to make sure we have -- I have the question
2 correct there.

3 Q. Is it fair to say that the number of pads
4 needed is based on the needs of the circuitry?

5 A. It's based on the needs of the circuitry and
6 the -- and the product you're designing. Because the
7 product, when you sell it, will have some number of --
8 of pins in its package, for example.

9 Q. So would a person of ordinary skill in the art
10 remove any pads that are unnecessary in a core-limited
11 design?

12 A. They would either be removed from the template
13 or simply never placed in the first place, with the
14 result being the same. It's --

15 Again, it's the con- -- sometimes the practice
16 is that you start with a template and remove the pads
17 you don't need; other times, you would put the
18 circuitry in, cram it together like you see here, put
19 down some periphery for the pads and then only include
20 the pads you need, which here are the ones that are
21 just the blackout lines.

22 So there are different ways to get to the same

1 result.

2 Q. In your Declaration, you refer to "power pads"
3 and "ground pads" in -- in numerous places, and you
4 can go to Paragraph 64, if you want, but you refer to
5 it generally in numerous places, correct?

6 A. Yes, I'm sure I do. That's been something
7 that comes up quite often, in our materials and your
8 materials.

9 Q. Is there a difference in purpose between a
10 ground pad and a power pad?

11 A. Well, I'm a little confused by your question
12 in a way because, you know, we're talk- -- if we're
13 talking about the pads or the functionality, the
14 functionality is different because a power pad is
15 where -- it's, like, the water pipe coming in your
16 house. You know, it brings water in. That brings
17 power and current into the IC.

18 The ground connections would be the sink.
19 It's the sewer pipe, so it would sink the -- the
20 current that comes into the chip.

21 In terms of the pads themselves, the same pads
22 are generally used.

1 Q. Okay. So ground pads and power pads have
2 different functionality, correct?

3 A. They serve different purposes, but in terms of
4 different functionalities that -- the pads are not
5 different. It's -- if you look, for example, at that
6 microphotograph we were looking at earlier, you can't
7 tell from that -- we can't point to that and say,
8 That's a ground pad, that's a power pad, because they
9 all look the same.

10 So they serve different functions, but that
11 doesn't mean the pads have to be different in any way;
12 they're still just metal.

13 Q. Okay. So -- so ground pads and power pads
14 serve different functions; is that fair?

15 A. At the chip level, they serve different
16 functions, but, again, it's the -- you know, the same
17 PVC pipe can be used for a -- for your water pipe
18 coming in or your sewer pipe going out, and in both
19 cases, don't get the two mixed up.

20 Q. And one difference between power pads and
21 ground pads is where they're connected to the circuit;
22 is that fair?

1 A. Well, again, that's a functional difference.
2 If I look, again, at that microphotograph we were
3 looking at earlier, the -- the power pads and the
4 ground pads obviously would be containing the
5 functions I was just describing of sourcing current
6 and sinking current.

7 But their actual -- the pads themselves are
8 the same; they're just metal squares.

9 Q. What are -- are there any other functional
10 differences between power pads and ground pads?

11 A. Not that I'm aware of.

12 Q. How does a person of ordinary skill in the art
13 determine whether to des- -- designate a pad as a
14 ground pad or a power supply pad?

15 A. (Witness perused document.)

16 Oh, I was rummaging there a bit. Could I
17 please have the question again, Counselor?

18 I apologize. I had to think a bit and study.

19 Q. How does a person of ordinary skill in the art
20 determine how to designate a pad as a ground pad or a
21 supply pad?

22 A. It would be something that would be driven by

1 the design of the product; that you would designate
2 which pads for a particular situation you want to
3 serve as the -- as a ground pad or as a power pad so
4 that you could wire them up to the outside world.

5 You would choose that designation based on the
6 needs of the product and the locations of the
7 circuitry inside the IC.

8 Again, Saint is quite -- Saint is remarkably
9 good at describing these things because like myself,
10 he did this for real.

11 Q. Go down to Paragraph 41 of your
12 Reply Declaration.

13 A. (Witness perused document.)

14 Q. Is it your opinion that the '164 patent only
15 applies to core-limited designs?

16 A. Well, as per something I said in Paragraph 41,
17 let me answer your question this way: Using the '164
18 patent's teachings with a pad-limited design would
19 make no sense because all you would do is make the
20 chip bigger without really -- you already have more
21 space than you need. Saint shows that and -- when he
22 describes a pad-limited design.

1 And so there's no reason to use that. You
2 already have more space than you need, and creating
3 space between pads could only be done because the
4 design is pad-limited, which means that you have so
5 many pads you can't -- you have empty space inside the
6 circuit area already.

7 So it doesn't make any sense. That would
8 probably be a firing offense for an engineer to make
9 the chip bigger, without any -- without any benefit
10 from it.

11 So in practice, it really only has practical
12 application to a core-limited situation where you
13 could actually have space between the pads out in the
14 periphery. You have more space than needed for the
15 pads you need; otherwise, there's no reason to create
16 space out there. You already have more space than you
17 need for circuits, as Saint, again, shows in
18 Chapter 8.

19 Q. Does the '164 patent ever mention a
20 core-limited design?

21 A. As far as I know -- and, again, I think
22 Dr. Khatri said the same thing. I -- I think I agree

1 with him on this: It does not mention it, but that's
2 been a term of the art since at least the 1990s.

3 And so if you look at a pad-limited design,
4 you, by definition, cannot have space between the
5 pads, unless you -- again, unless you foolishly make
6 the IC bigger, so there seems to be no reason to use
7 '164 in a pad-limited situation.

8 MR. WATSON: Let's pull up the '164 patent.
9 That's Exhibit 1001.

10 THE WITNESS: I have a pap- -- a clean paper
11 copy of that as well.

12 MR. WATSON: Let's put that on the screen, so
13 we can all make sure we're referring to the same
14 parts.

15 THE CONCIERGE: 1001, Counsel?

16 MR. WATSON: Correct.

17 THE CONCIERGE: Stand by.

18 (Deposition Exhibit 1001 was marked for
19 identification.)

20 BY MR. WATSON:

21 Q. All right. So, Dr. Foty, I want to direct
22 your attention to Column 3, Lines 15 (sic) through 16

1 of the '164 patent.

2 A. (Witness perused document.)

3 Column 3, 15 to 16?

4 Q. Lines 5 through 16. Sorry.

5 A. 5 through 16. Sorry. I thought you said 15.

6 Q. Okay. Then let me know when you're there and
7 had a chance to read it.

8 A. I'm there. I was just doing a quick read, and
9 I see it's on the screen. It's blown up enough I can
10 read it on the screen now as well.

11 Q. Okay. So the '164 patent here describes
12 multiple pad groups, G1, G2, and G3, correct?

13 A. That is referring to some particular figure
14 which, I believe, is -- Figure 2 and Figure 3 seem to
15 be the ones that refer to the -- what we're seeing
16 here.

17 Q. Okay. So this -- this paragraph refers to
18 Figures 2 and 3, correct?

19 A. At least in terms of the reference to G1, G2,
20 and G3.

21 Q. Okay. And in these pad groups, at least one
22 pad, 22, [as read]:

1 Is an input/output pad connected to a ground.

2 Do you see that?

3 A. I see that, yes.

4 Q. Okay. So would you agree with me that the
5 '164 patent expressly states that at least one pad,
6 22, is a ground pad?

7 A. Well, it says, [as read]:

8 To a ground or a system low voltage.

9 So what that's saying is that the pad is used
10 as a ground pad. I'll agree with that.

11 Q. Okay. All right. You can put that to the
12 side.

13 Let's go back to --

14 MR. WATSON: Actually, let's pull up
15 Exhibit 1006.

16 THE WITNESS: What is that?

17 (Deposition Exhibit 1006 was marked for
18 identification.)

19 BY MR. WATSON:

20 Q. That's the Yoshinaga translation in English.

21 A. I'll have to dig for my paper copy if -- if
22 you're going to use this for very long.

1 Q. I'm going to mainly refer to Figure 2,
2 generally, but I'll -- I'll give you a second to dig.

3 A. (Witness perused document.) Let's see.

4 I have found it in this big binder from last
5 time. Just give me a moment here to -- to pull it up.

6 Okay. If I need it, I have my paper copy of
7 Yoshinaga.

8 Q. Okay. Do you have Figure 2 in front of you?

9 A. I have it on the screen. And if need be, I
10 can have it on my paper copy as well.

11 Q. And Figure 2, can you explain to me how the
12 pads, 3 and 4, are connected?

13 A. I'm not sure I understand your question there.
14 These are topological depictions showing connections
15 into the circuitry. That's what it shows.

16 Q. Uh-huh. Let me clarify it a little bit, make
17 that a little simpler.

18 What is the circuitry shown between Pads 3 and
19 4?

20 A. Well, if I take -- well, it was actually --
21 interestingly, there's more than one direct route you
22 can take, but they're between them. One path would be

1 to go through Resistor 21, Dual Diode Structure 9 to
2 56, and then up through Dual Diode 10 through
3 Resistor 22 to Pad 4.

4 Q. You say that's one path.

5 Is there another path?

6 A. It looks like you could go through Dual
7 Diode -- I believe that's 7. It looks like you could
8 go through 7 down to 23 and then come back up
9 through 1 of the Dual Diodes there to -- to get
10 eventually to 10 and across through 22 to 4.

11 Q. What is the purpose of what you're referring
12 to as "Dual Diodes" in Figure 2?

13 A. The -- before I discuss that, I do want to
14 point out that we didn't cite this in our analysis.
15 We didn't use Figure 2; we used 1, 3, and 4.

16 Q. Oh, okay.

17 A. I just want to -- to make that note because --
18 In any case, the Dual Diode structure you're
19 referring to there -- I need to make some space.

20 So -- I'm sorry. Could you ask -- refer to
21 the question about the Dual Diode structure again?

22 Q. Yeah. What is the purpose of what you

1 referred to as the "Dual Diodes" in Figure 2?

2 A. Well, before I answer, I just want to note
3 that I did make reference to -- Yoshinaga describes
4 the functionality of Paragraph 61, and Haralabidis
5 also has a description of that.

6 The purpose of the Dual Diode is basically to
7 allow an ESD discharge event to pass through the
8 Dual Diode structure, yet not allow, for example,
9 digital noise, digital switching noise, to propagate
10 through.

11 So it allows the ESD functionality to function
12 without compromising the intra-block noise protection
13 that the Dual Diode structure provides. It allows --
14 the Dual Diode allows noise immunity to continue but
15 allows ESDs -- blah -- ESD discharge to proceed.

16 Q. And when you refer to the Dual Diodes in
17 Figure 2, are you referring to what's been marked as 9
18 and 10?

19 A. I believe Yoshinaga's figure there for 9 and
20 10, for example, is -- those are the Dual Diode. He
21 uses a particular symbol for those.

22 Q. Now, earlier I thought you had said that

1 you're not relying on Figure 2 of Yoshinaga; is that
2 correct?

3 MR. JENSEN: Object to form.

4 THE WITNESS: (Perused document.)

5 No, I -- I take that back. It was 1, 2, and
6 4. We were not relying on 3 (sic). Yoshinaga's
7 figures are kind of screwy the way they're in the --
8 his -- his patent application.

9 BY MR. WATSON:

10 Q. Okay. Thanks. Thanks for clarifying that. I
11 just wanted to make sure that we were clear on that.

12 Okay. So on the -- can you turn to Figure 1?

13 A. Okay. Figure 1. (Witness perused document.)

14 Okay. It's on the left there, and I have it
15 in front of me on paper.

16 Q. Okay. Figure 1 also includes these
17 bidirectional diodes, 9 and 10, correct?

18 A. That appears to be the case, yes.

19 Q. Okay. And would you agree with me that the
20 functionality of these bidirectional diodes, 9 and 10,
21 is the same in any of these figures, 1 through -- I
22 guess, 1 through 4?

1 Or excuse me. Strike that. I'm going to
2 change that question.

3 Would you agree with me that the function of
4 these die direct -- strike that. Blah.

5 Would you agree with me that the functionality
6 of these bidirectional diodes 9 and 10 in Figures 1,
7 2, and 4 is the same?

8 MR. JENSEN: Object to form.

9 THE WITNESS: I'd expect it to be the same,
10 based on what Yoshinaga says at Paragraph 61, that
11 they serve the function of allowing noise immunity to
12 function while not --

13 (Unstable Internet caused an interruption.)

14 BY MR. WATSON:

15 Q. So the purpose --

16 THE COURT REPORTER: He cut out for me. I'm
17 sorry.

18 Yes, he's frozen, so his answer cut off in the
19 middle.

20 MR. JENSEN: He's frozen for me as well.

21 MR. WATSON: Let's -- let's go off the record,
22 if that's okay, and we'll see if we can get him back

1 on.

2 MR. JENSEN: Yeah. We're almost at an hour.
3 I'm fine taking a break here.

4 (Recess taken from 6:54 a.m. to 7:06 a.m.)

5 MR. WATSON: All right. Let's put on the --
6 let's -- if we could, Mike, let's put on the exhibits
7 we had before, since we just kind of went dark real
8 fast there, and then we can go back on the record.

9 Are we on the record?

10 THE COURT REPORTER: I started writing.

11 MR. WATSON: Oh, sorry. I didn't realize we
12 were on the record.

13 BY MR. WATSON:

14 Q. All right. Welcome back, Dr. Foty.

15 A. Good to be back.

16 And, again, I don't remember where it cut out,
17 and so we'll have -- you know, we might have to
18 reconstruct some of what happened before my router
19 crashed.

20 Q. Yeah, yeah. So -- so before the break, your
21 router had crashed, and so I didn't give you a chance
22 to finish -- you weren't able to finish your

1 question (sic), so let me re-ask the question, if
2 that's okay.

3 A. That should be okay. If I'm lost of --
4 because of a -- you know, a string there or a thread,
5 I'll let you know.

6 Q. Okay.

7 A. It just seems disembodied at this point. It's
8 been, you know, 10, 15 minutes.

9 Q. Would you agree with me that the functional --
10 functionality of the bidirectional diodes 9 and 10 in
11 the Yoshinaga figures is the same?

12 MR. JENSEN: Object to form.

13 THE WITNESS: (Perused document.) I'm looking
14 at Yoshinaga Paragraph 13, and he refers to Element 9
15 and Element 10. He refers to both of them as "ESD
16 protective element," so he identifies them as being
17 the same thing.

18 So it's not unreasonable to assume the
19 functionality of the circuitry would be the same. It
20 would respond differently to different stimuli, but
21 that's another issue.

22 BY MR. WATSON:

1 Q. And so the functionality of the bidirectional
2 diodes 9 and 10 is to function as an ESD protective
3 element, correct?

4 A. Yoshinaga identifies both as being "ESD
5 protective elements."

6 In terms of what they do, the actual
7 functioning of them would differ based on different
8 stimuli being applied to them, of course.

9 Q. All right. And let's turn to Figure 6.

10 MR. WATSON: Actually, can I get control of
11 the screen, please.

12 THE WITNESS: And I do have my paper copy in
13 front of me with Figure 6, if needed.

14 BY MR. WATSON:

15 Q. In Figure 6 of Yoshinaga, does it show the top
16 metal layer of the circuit?

17 MR. JENSEN: Object to form.

18 THE WITNESS: I'm not sure what you mean by
19 "circuit," Counselor, because there's -- circuit
20 blocks are identified, but the circuitry inside them
21 is not identified.

22 BY MR. WATSON:

1 Q. Fair. Does Yoshinaga Figure 6 show the top
2 metal layer of the chip?

3 MR. JENSEN: Same objection.

4 THE WITNESS: Well, let me answer your
5 question this way: He -- in -- in terms of the three
6 circuit blocks he has, which are -- I'm not sure if he
7 has the three circuit blocks numbered in this figure.

8 Oh, yeah. Well, I know he has like -- the
9 lower right circuit block is 57, for example. Is that
10 57 or 67? It's hard to see. 67 you can see there,
11 and so he has 1, 2, and 67. Sorry. He does number
12 the circuit blocks; they're just a little hard to see.

13 He does not show any metallization is in
14 there, in the -- in the -- in the circuit blocks. He
15 does appear to show metallization, obviously, for the
16 buses that -- the three paired bus segments that run
17 around the peripheral area.

18 BY MR. WATSON:

19 Q. The Yoshinaga Figure 6 doesn't show all of the
20 metallization in the chip?

21 MR. JENSEN: Object to the form.

22 THE WITNESS: He doesn't provide that level of

1 detail in the circuit blocks, and I believe he says
2 so; they're illustrative.

3 BY MR. WATSON:

4 Q. And could the elements of the circuit blocks
5 be connected by metal layers, other than the top
6 layer?

7 A. Do you mean the circuit blocks being connected
8 to each other?

9 Q. Yes.

10 A. Well, Yoshinaga is silent on that specific
11 topic. He just shows that there are connections
12 between the blocks, and he has the Dual Diode
13 structure to provide noise protection between the
14 blocks for different signals while still allowing ESD
15 events to be discharged collectively to get it off the
16 chip.

17 Q. Let's pull back up your Declaration, your
18 Reply Declaration, Exhibit 1042.

19 A. Just give me a moment to clean up the mess.

20 Q. Uh-huh.

21 A. (Witness perused document.) Okay.

22 I have my Declaration back now on my desk.

1 Q. Let's go to Paragraph 144.

2 A. (Witness complied.)

3 Q. And I want to refer to the last sentence that
4 starts, [as read]:

5 The specific option to be used...

6 A. (Witness perused document.) Yes. That spans
7 two pages, I believe.

8 THE WITNESS: It's Pages 79 and 80, for the
9 videographer (sic) to find it, by the way.

10 Thank you.

11 BY MR. WATSON:

12 Q. Yep. So you say that, [as read]:

13 The specific option to be used would, as
14 described above, be a choice based on the chip design,
15 (e.g., all digital design, all analog design, or
16 mixed-signal design.

17 Do you see that?

18 A. Yes, I see that. And again it's "e.g.,"
19 meaning it's an example, not the only -- the only one.

20 Q. How would a person of ordinary skill in the
21 art decide which connection method to use with an all
22 digital design?

1 A. Well, again, there are many factors that would
2 be considered, and, for example, there are different
3 power supply voltages. You would have to provide
4 mediation circuitry between the blocks. You would
5 have to do simulation and analysis, for example, of
6 digital switching noise. And what risk do you have
7 for, say, a -- a nonchip ground bus being able to
8 propagate noise from one digital block to another, and
9 is that a risk of signal integrity?

10 Those are two of the considerations, but in
11 reality, there's a large number of them.

12 Q. Okay. And would you agree there's a large
13 number of considerations when deciding which
14 connection method to use with an all analog design?

15 MR. JENSEN: Object to form.

16 THE WITNESS: There would be considerations,
17 but they'd be of a different type.

18 And Saint actually describes this in his case
19 study one, for example, the trade-offs you have to
20 make and the decisions you have to make, particularly
21 with a pad-limited situation.

22 BY MR. WATSON:

1 Q. How would a person of ordinary skill in the
2 art decide which connecting -- connection method to
3 use with an analog design?

4 MR. JENSEN: Object to form.

5 THE WITNESS: Was that the question just
6 asked?

7 BY MR. WATSON:

8 Q. No, no, it was not, so let me -- let me repeat
9 the question.

10 How would a person of ordinary skill in the
11 art decide which connection method to use with an
12 analog design?

13 MR. JENSEN: Object to form.

14 THE WITNESS: Okay. Sorry. I thought the
15 prior question was --

16 Sorry, Travis, go ahead.

17 MR. JENSEN: I object to form.

18 THE WITNESS: I thought your previous question
19 was about an analog design because I referred to Saint
20 Case Study 1, which is an analog design.

21 So was this a -- I'm trying to -- maybe
22 something got mixed up here, but what was the previous

1 question?

2 Because I thought I just answered the question
3 you just asked previously.

4 BY MR. WATSON:

5 Q. Oh, my previous question was: Is there a
6 large number of considerations when deciding which
7 connection method to use with an all analog design?

8 So one was about the number of -- you know,
9 the number of considerations; one was about what those
10 considerations are, if that makes sense.

11 A. Thank you for that clarification. I thought
12 it was the same question again, so I said it in my
13 first response. I said that there are various
14 considerations. They're different for analog design.

15 And, again, it would be the same sorts of
16 considerations. Do you have different power supplies
17 for the different analog blocks?

18 Analog circuitry tends to be less noisy
19 because of the waveforms are sinusoidal rather than
20 square waves, so there's another group of
21 considerations.

22 And, again, that's what is very nice about

1 Saint Case Study 1. In Saint's book, it's very
2 illuminating about in reality, speaking from
3 experience, what those considerations are like,
4 particularly with analog chips, typically in the past,
5 frequently being pad-limited.

6 Q. So you keep referring to "Saint's Case
7 Study 1."

8 What does Saint Case Study 1 say about the
9 connection methods used to connect ground buses?

10 A. I actually discuss this somewhere in my
11 Declaration, and I am trying to find that discussion.
12 (Witness perused document.)

13 I was getting my copy of Saint in front of me,
14 if needed, Counselor, so could -- could I have --
15 please have the question repeated for -- to refresh my
16 recollection.

17 Q. What does Saint Case Study 1 say about the
18 connection methods used to connect to ground buses?

19 A. What Saint describes specifically, in Case
20 Study 1, is that he has four analog blocks, and his
21 design is pad-limited; those are the constraints he
22 starts with.

1 And because of those two considerations, his
2 judgment or the judgment of the design team is that
3 the risk of connecting all the grounds together
4 on-chip is worth doing because you can make the chip
5 smaller; you can have a single ground pad.

6 So in that instance, he does the connections
7 on-chip rather than off-chip for the grounds. He
8 keeps the -- the power domains for the four analog
9 blocks separate, but the grounds are unified on-chip
10 to con- -- to make the pad-limited situation, to
11 relieve the pressure from the pad-limited situation.

12 And he has a figure, which I have in my
13 Declaration. It's on Page 70, where it actually shows
14 the -- he starts with four separate ground buses for
15 the different -- for the different analog blocks, and
16 he literally says "join." (Witness perused document.)

17 There. Literally -- he literally says "join,"
18 to join them together into one. And so that way he
19 has one pad, and he doesn't have to make the chip
20 bigger to accommodate three more pads.

21 Q. Does Saint Case Study 1 describe how to
22 connect these blocks?

1 MR. JENSEN: Object to form.

2 THE WITNESS: He shows, at Figure CS1-97 (sic),
3 that he unifies them with an on-chip ground ring, so
4 he lit -- when he says "join," in figure CS1-87, he
5 literally joins them at the chip level because here,
6 that's the best -- the best way to tackle this design
7 problem.

8 BY MR. WATSON:

9 Q. So on Saint Case Study 1, does he use bond
10 wire to connect these different blocks?

11 A. In this particular case study, he does not.

12 Q. Does he use the metallization layers to
13 connect the different blocks?

14 A. In this particular design situation, because
15 it's a pad-limited analog design, he connects them as
16 one bus all the way around. He does not segment the
17 buses. He has one on-chip bus for the grounds. He
18 was four buses for the voltages, one bus for the
19 grounds, and that lets him maintain a small chip.

20 Q. And is that -- strike that.

21 And does he connect these blocks into one bus
22 all the way around, using the metallization layers on

1 the chip?

2 MR. JENSEN: Object to form.

3 THE WITNESS: In this particular instance as
4 shown in Figure CS1-92, in particular, which is the
5 final floor plan, he does. He connects one because he
6 can. He joins them as the Figure 87 shows, and then
7 they all go out together to one pad on the left side
8 of the floor plan.

9 So he has one ground pad on the outside
10 connected to metallization inside the IC, again, for
11 this particular design situation. That's the -- for
12 this situation, this is the specific answer that's
13 used.

14 BY MR. WATSON:

15 Q. Let's go to Paragraph 78 of your
16 Reply Declaration.

17 A. Again, 78, we seem to be on a roll on this.
18 78 spans two pages, by the way, so just -- just so --
19 since, you know, it's on the screen, but I may have to
20 flip pages here.

21 Q. It was not intentional to choose paragraphs
22 that were on two pages, I assure you.

1 A. I thought it was intentional, just to screw
2 around with me.

3 Q. So in Paragraph 78, you refer to, [as read]:
4 Intervening wire bond technology improvements.
5 Do you see that? It's at the top of Page 44.

6 A. I see that, yes.

7 Q. What intervening wire bond technology
8 improvements are you aware of between 2003 and 2018?

9 A. Well, before I answer that question, I did
10 also want to point out that Exhibit 2014, which is the
11 Johnson reference, Dr. Khatri says, [as read]:

12 Less inductive than bond wires.

13 He cites this reference, but this reference
14 never discusses bond wires, by the way, if you look at
15 it. It doesn't even appear in there, so I just wanted
16 to make sure we noted that first.

17 Various improvements have been made, for
18 example, that you can now for -- over the years, you
19 can -- you can make smaller pads and -- and things of
20 that sort. I would have to review the literature in
21 detail about what the -- somewhere in here I have some
22 articles about how that's improved over the years.

1 So I would have to review those, but clearly
2 the articles describe how wire bonding technology,
3 which many people thought was simply going to not work
4 anymore over the years, has continued to work and had
5 about an 80 percent market share.

6 During 2003 to 2018, it -- clearly, there's
7 three or four reference points for 80 percent market
8 share for bond wiring.

9 Q. Are you aware of any technological
10 improvements that improved the inductance of wire bond
11 technology?

12 A. Well, let me answer your question this way: I
13 don't think we have any evidence presented in front of
14 us that that was ever a problem for wire bonds.

15 As I said, Khatri's reference to that and the
16 one that was used was 2014 -- I'll call it the
17 "Johnson reference," that was the name of the
18 author -- that article does not discuss bond wire
19 inductance or bond wires at all.

20 So there hasn't been anything to examine here
21 about any problems with wire bonds involving
22 inductance. I have nothing to respond to on that

1 because nothing was presented to that effect.

2 Q. Okay. My question was simply: Are you aware
3 of any technological improvements that improved the
4 inductance of wire bond technology, though?

5 MR. JENSEN: I object to form.

6 THE WITNESS: Well, I'm not aware of any
7 problem existing to even be solved, so the wire bonds
8 are used. They're still used.

9 And so inductance clearly has never been a
10 problem to worry about.

11 BY MR. WATSON:

12 Q. Okay. Now, in the -- in that same paragraph,
13 you refer to the, [as read]:

14 In- -- resistance/inductance trade-off between
15 metal traces and bond wires.

16 Do you see that?

17 A. Yes, I see that.

18 Q. Well, what do you mean by a "trade-off"?

19 A. Basically, the trade-offs would be -- and,
20 again, I'll cite the article, the 2014 reference.
21 He's discussing in that article that any wire or
22 connection will have some resistance inherently and

1 some self-inductance. That's just physics. You will
2 have some. It's a question in the practical world of
3 what the magnitude is.

4 And on-chip, as he describes, the metal
5 traces, for the most part, the resistance is enough
6 because of their small size that the inductance is
7 negligible.

8 In terms of -- the article talks about in
9 package traces, the -- sorry. Not package traces.
10 The article is talking about inductance in PC board
11 traces.

12 In that case, the inductance -- or, sorry --
13 the resistance is so low that inductance does matter
14 on a PC board, and the discussion there is about,
15 because of that, you need to worry about load
16 reflections and doing phase matching and termination
17 and all that Smith chart stuff you get as an
18 undergraduate.

19 And so the trade-off would be that the
20 resistance is low enough that they're useful, but the
21 wires are so short that it really doesn't -- it isn't
22 a problem. It's -- there's just nothing to worry

1 about there.

2 Q. How does the length of the wire affect the
3 amount of inductance?

4 A. Beg your pardon?

5 Q. How does the length of the wire affect the
6 amount of inductance?

7 A. I forget off the top of my head. You're
8 getting back to electromagnetic theory, but the bottom
9 line basically is that inductance is just not a
10 problem in bond wires, and I haven't seen anything
11 presented from the POR or Dr. Khatri that it ever was
12 a problem.

13 And obviously people use wire bonds and have
14 used them successfully.

15 Q. Are you aware -- is there any correlation
16 between the length of the wire and the amount of
17 inductance?

18 A. I didn't study that level of detail of the --
19 there would -- there -- that's possible. I did not --
20 I just don't remember my electromagnetic theory
21 because the current goes through, and the current
22 causes a magnetic field.

1 So I'm not -- I just don't off the top of my
2 head recall if just the length matters for inductance.

3 Again, what matters here is that the article
4 cited actually is talking about PC board traces, and
5 in that situation, what matters is the resistance
6 versus the inductance.

7 So the real trade-off is resistance versus
8 inductance, and on-chip, it's generally not a problem,
9 as the Johnson reference, 2014, says.

10 And in terms of wire bonds, no one's reported
11 any problems that are showstoppers, so --

12 Q. So sitting here today, you're not aware of any
13 correlation between the length of a wire and the
14 amount of inductance; is that fair?

15 MR. JENSEN: Object to form.

16 THE WITNESS: I would have to go -- again, go
17 back to my electromagnetic theory. You know,
18 that's -- I'd have to go back and examine that, but I
19 do know that it's a function of the current flowing
20 through a wire, so --

21 MR. WATSON: Okay. Well, let's pull up
22 Exhibit 1008, which is the Saint reference.

1 (Deposition Exhibit 1008 was marked for
2 identification.)

3 THE WITNESS: Okay. I have my paper copy.

4 The one thing I want to note, since it's
5 easier to look at the book than to go through this --
6 this production, if you're referring to numbers in the
7 production, it'll be different than the page numbers,
8 so we just will have to correlate that if we look at
9 particular pages.

10 BY MR. WATSON:

11 Q. Sure, yeah. I'll -- I'll try and -- I'll --
12 I'll announce both the number in the top left/top
13 right, which is in blue, which is your page number,
14 and then the page number of the -- the exhibit that's
15 in the litigation.

16 Let's go to Saint Page 195, on the top
17 right-hand corner, and on the Bates version, Page 209,
18 and that's Figure 9-15 in it.

19 A. Okay. I have that in front of me, and I also
20 have this figure in my Declaration, so --

21 I'll slide this over here and go --

22 So you have this figure, and it appears in my

1 Declaration, at Paragraph 85, on Page 48, for what
2 that's worth. I have that in front of me as well.

3 Q. Sure, that's -- that's totally fine.

4 So in -- on this page, Page 195, it says -- at
5 the bottom of the paragraph section that says,
6 [as read]:

7 Minimal silicon overlap.

8 A. (Witness perused document.)

9 Q. It says, [as read]:

10 So, you have to the keep the overlap of the
11 bond wire over unused silicon as short as possible.

12 Do you see that?

13 A. Yes, I see that. Saint is recommending
14 replacing poor design practices with good design
15 practices.

16 Q. Okay. What is "unused silicon"?

17 A. Well, in the context of this figure and given
18 his other discussions of this topic, it seems here
19 that he means the silicon between the bond pad and the
20 chip edge.

21 Q. And in Figure 9-15, the blue circle shows the
22 "silicon overlap" with the bonding wire, correct?

1 A. He shows a really horrible design practice of
2 running a wire off -- off-chip very indirectly, which
3 is why above he has what he calls the
4 "45-Degree Rule," which is actually a good rule.

5 Q. So what is the blue circle intended to
6 indicate in Figure 9-15?

7 A. It's intended to indicate a very poor design
8 practice that is easily overcome by simply not doing
9 it.

10 He shows a good version of this in
11 Figure 9-11, where he avoids that. He actually --
12 that's a good reference point because if you see -- if
13 you take his Figure 9-15 and you examine it in the
14 context of 9-11, Figure 9-11, you can see that that
15 upper right corner, it makes no sense to route it way
16 over to the right, to one of the pads on the right
17 side.

18 It makes much more sense to route it as
19 quickly as possible off directly to a pad and have a
20 short connection.

21 Q. So in this figure, 9-5 (sic), is it saying
22 it's best practice to limit the amount of bonding wire

1 that goes over the silicon?

2 A. You said --

3 MR. JENSEN: Object to form.

4 THE WITNESS: You said, "Figure 9-5."

5 I believe you mean "9-15," just so we're not
6 changing figures here.

7 BY MR. WATSON:

8 Q. Correct, correct.

9 A. Just for the record, yeah, the -- the question
10 was about Figure 9-15 --

11 Q. How --

12 A. -- not 9-5.

13 Q. How about if I repeat the question --

14 A. If --

15 Q. -- is that fair?

16 A. If that makes the record clearer for everyone,
17 I'm happy to let you do that, Counselor --

18 Q. Okay.

19 A. -- and we can see.

20 Q. In Figure 9-15, it's saying the best practice
21 is to limit the amount of bonding wire that goes over
22 the silicon, correct?

1 MR. JENSEN: Object to form.

2 THE WITNESS: That's what it says.

3 And, again, if you compare Figure 9-11, which
4 is the good result, and 9-12, which is
5 the gets-the-engineer-fired design, you can see what
6 he's saying is that pad in the top row, the right most
7 pad -- he's saying don't do what you see in 9-12; do
8 what you see in 9-11, where you can see that the
9 connection in 9-12 is like the one you see in 9-15,
10 which is poor practice, and the connection for that
11 pad to a package trace and a pin in 9-11 is good
12 design practice.

13 So he's saying, Don't do -- don't do this
14 particular excerpt from 9-12 and 9-15. Don't do that.
15 It's poor design practice.

16 BY MR. WATSON:

17 Q. Why would someone not want to overlap the bond
18 wire with too much silicon?

19 MR. JENSEN: Object to form.

20 THE WITNESS: Because you want to keep the
21 bond wire as short as possible. That's all this is
22 about, and --

1 BY MR. WATSON:

2 Q. Why do you want to keep the bond wire as short
3 as possible?

4 A. Particularly back in 2002 -- this is a
5 condition which today has been mediated, to some
6 extent, but the longer the bond wire, the higher the
7 risk of something -- say, you getting sag or droop, as
8 he discusses.

9 And so Saint is just saying if you do good
10 design practice, you minimize that risk. It's a --
11 it's a free lunch, essentially. It's just doing it
12 well rather than doing it poorly.

13 Q. And what happens if the bond wire contacts the
14 metal layers of the circuit?

15 A. Well, he actually shows an example in
16 Figure 9-13 on the previous page, which is Page 194 of
17 the text. He shows that if you're running a bond
18 wire, for example, that goes over some other metal
19 layer, it can -- if it can cause a short, that's --
20 that's the risk you're avoiding.

21 And if you make a direct line, like he shows
22 in Figure 9-11, you're minimizing that -- that risk;

1 that's 9-12 there. You can see that's -- I think he's
2 got one there, the -- 9-14, I believe, is excerpted
3 from 9-12 there. It's the second most -- the pad
4 second from the right on the top. Because you can
5 short to another pad.

6 So this is a -- this is a matter of go
7 straight out and make them short so that you minimize
8 drooping, and you have noth- -- you have nothing or as
9 little as possible underneath for them to short to.

10 Again, Saint is teaching good design practice.
11 That's why he wrote his book.

12 Q. So it's good design practice to limit the
13 amount of bonding wire that goes over the metal; is
14 that fair?

15 A. I think it's fair to say you want to make the
16 bond wires as direct and as short as possible, but
17 that doesn't mean, you know, they can't be fairly
18 lengthy compared to other features on-chip, but the --
19 Saint teaches very good design practices here.

20 And, again, it's a free lunch. You don't have
21 to pay any money or solve any problems; you just do it
22 right.

1 Q. And so the way this discusses avoid
2 shirt-circuits (sic) is by minimizing the amount of
3 wire with circuit board underneath it; is that fair?

4 MR. JENSEN: Object to form.

5 THE WITNESS: Oh, it's not circuit board.
6 We're not out at that level yet. We're just
7 connecting pads to package traces.

8 BY MR. WATSON:

9 Q. Oh, fair.

10 So the way this avoids -- strike that.

11 The way this discusses avoiding short circuits
12 is by minimizing the amount of wire with metal
13 underneath it; is that fair?

14 MR. JENSEN: Object to form.

15 THE WITNESS: Well, that's -- one haz- -- one
16 hazard would be if the -- the bond pad -- you can see
17 in Figure 9-13, as the bond wire comes diving in to go
18 to the middle pad, it's coming real close, as it
19 descends, to -- to the other pad. It's like an
20 obstruction hazard on final in an aircraft. I speak
21 from experience.

22 So you want to avoid that in this particular

1 situation. You want to keep your metal lines away
2 from other pads. You want to make sure that they
3 don't droop and short to other things.

4 That's basically all he's showing here is --
5 particularly in the 2002 context -- the ability to
6 do -- is, again, do a nice Figure 9-11 connection to
7 your -- your package pins.

8 BY MR. WATSON:

9 Q. Let's go now to Saint Figure 6-2 and direct
10 your attention there real quick, which is on Page 126
11 in the top left corner and Exhibit Page 142.

12 A. (Witness perused document.) Yes. And this
13 figure does also appear in my Declaration. It's on
14 Page 68, at Paragraph 121, just for the record.

15 And I have that in front of me, but I also
16 have the Saint figure in front of me, so --

17 Q. Okay.

18 A. -- please proceed.

19 Q. In Saint Figure 6-2, what does the "P+" mean?

20 A. P+ is a heavily doped pocket, doped --
21 heavily doped P type, such as in silicon, it would be
22 with boron. This is conventional practice because you

1 put that in in order to create a -- make sure you have
2 an ohmic contact between the metal contact and the
3 silicon.

4 If you just put the contact down to lightly
5 doped silicon, put a metal contact, you'll -- you
6 won't get an ohmic contact; you likely will get a
7 diotic contact.

8 And so that's conventional practice in all
9 contacts is you bring contacts down to silicon on to a
10 P+ or an N+ pocket to ensure a low resistance on the
11 contact.

12 Q. And what is this P pock- -- plus pocket
13 sitting in?

14 A. It's sit- -- sitting in silicon. The silicon
15 could -- is probably P-type silicon because you're
16 making an ohmic contact. If you had the P+ going to
17 end-type silicon, you would have a diode rather than
18 an -- you know, a conscious to simple -- a simple
19 resistive path in the silicon.

20 So, again, that's very standard practice in
21 the art, of -- of -- it's just standard practice in
22 the art of making silicon MOS transistor structures

1 and similar.

2 Q. Now, the line that says "quiet," that's the
3 substrate, correct?

4 MR. JENSEN: Object to form.

5 THE WITNESS: Yes, I believe that's the
6 substrate which, in conventional parlance, would refer
7 to the bulk of the silicon. That would be a chip cut
8 out of a wafer, for example.

9 BY MR. WATSON:

10 Q. Okay. So it's your opinion that the P+ pocket
11 is sitting -- well, strike that.

12 Let's go down to Para- -- to the bottom of
13 page -- we'll go down here -- 143, on the bottom
14 right. It's 127 on the top right.

15 A. Okay. I have that. That's the next page in
16 the book, so it's quite easy for me here.

17 Q. Uh-huh. Okay. It says here, at the bottom,
18 that, [as read]:

19 These rings are referred to as guard bands.

20 Do you see that?

21 A. I see that, yes.

22 Q. Well, what is a "guard band"?

1 A. Well, before I answer your question, just to
2 note that the term "guard band" is used for many
3 different things in the semiconductor business just --
4 so the guard band we're discussing here is one
5 particular usage of that phrase.

6 And he basically describes this on the
7 following page. He shows guard bands around the
8 different blocks, in order to provide noise protection
9 so that the noisy block doesn't disturb the quiet
10 block.

11 Q. So in Figure 6-2, that shows a guard band
12 around these two signals, correct?

13 MR. JENSEN: Object to form.

14 THE WITNESS: What he's showing here, in
15 6.2 (sic), is that you have -- he's showing a simpler
16 version of what he shows later. He's showing
17 essentially a one-dimensional version.

18 If you have a guard band and it's metal, it's
19 going to have to sink whatever it picks up, and so
20 what he's showing here is the guard band around the
21 noisy block would be directed to be pulled out of the
22 circuitry through the separate contact for that.

1 It would -- would -- becomes a guard band
2 further in the next few pages, showing -- he's
3 essentially showing a way to shunt noise from the
4 noisy block out before it can get to the quiet block.

5 BY MR. WATSON:

6 Q. Now, earlier you referred to an open (sic)
7 contact.

8 What -- what is an "open contact"?

9 MR. JENSEN: Object to form.

10 THE WITNESS: Actually, I didn't say "open."
11 I said "ohmic."

12 Yea, all my discussion --

13 BY MR. WATSON:

14 Q. An ohmic contact?

15 A. Yes. All my discussion was ohmic contact,
16 Oscar, Hotel, Mike, India, Charlie; not open, "ohmic."

17 Q. Got it.

18 What is an "ohmic contact"?

19 A. Oh, okay. I can explain that, and hopefully
20 that will clarify my earlier testimony, if that needs
21 to be corrected in the record for the typo -- if
22 there's a typo.

1 An "ohmic contact" just means that the IV
2 profile is linear. As I said earlier -- to clarify in
3 that context what I said earlier, if you do not put
4 the little P+ pocket there and you put metal on
5 lightly doped silicon, you will produce probably a
6 Shockley diode, which is not ohmic.

7 The IV curve would not be linear, which is not
8 good because the resistivity would vary with voltage
9 and current and things like that.

10 So an ohmic contact simply means that the IV
11 is, like, Ohm's law. It's just a straight line. IV
12 is a straight line, and the other reason for that is
13 not just that it's ohmic, but it makes a very low
14 resistance contact, so you can -- you -- the contact
15 resistance between the contact and the P+ pocket is
16 effectively negligible.

17 Q. All right. Let's go to Figure 9-28. And I
18 know you refer to this a bunch of places in your
19 Declaration, but we'll -- we'll pull up the figure.

20 A. Got it. I will find that in my Declaration
21 somewhere as well.

22 Q. It's on Page 207, on the top right numbering

1 of Saint page --

2 A. Oh, I had that, but I'd like to pull it up in
3 my Declaration if I need it as well.

4 Q. It's also on Page 221 of the -- the -- the
5 exhibit numbering.

6 A. Okay. I wanted to find it in my Declaration
7 now rather than in the middle of a line of questions,
8 so I have it in my Declaration, and I have -- excuse
9 me -- Page 207 of Saint.

10 Q. Okay. In Saint Figure 9-28, are there any
11 ESD buses shown?

12 A. In this particular teaching, in Saint when
13 he's -- he's describing here, he doesn't show the
14 ESD buses in this particular version.

15 Q. In Saint Figure 9-28, are there any
16 connections shown between the pads?

17 A. That not being the purpose of
18 Figure 9.28 (sic), he doesn't show that.

19 Q. Okay.

20 A. He does not show that here.

21 Q. Okay. Now, let's go -- and I think you make
22 reference, a little bit earlier in this chapter, to

1 Figure 9-2.

2 A. Okay. That's -- that's a separate discussion
3 from 9.28, so -- you mean 9.2 (sic) or a different
4 one?

5 Q. Yeah. Yeah, let's just go to Figure 9-2.

6 A. Okay.

7 Q. I'm just saying earlier in the chapter is what
8 I was referring to.

9 A. (Witness perused document.)

10 Q. Are you there?

11 A. Yeah, I'm just trying to put bookmarks in my
12 Declaration so I -- but I want to make sure if I need
13 it, I said I can have that in my Declaration rather
14 than be digging for it in the middle of a line of
15 questions.

16 So I do have the -- anyway, I do have the page
17 in Saint, which is -- I believe Page 189 is the page
18 number of -- actually in the book.

19 Q. Okay. In Figure 9-2, the pads are connected
20 by bond wire to the package traces, correct?

21 A. Yes, he shows that here. And as I said
22 earlier, the package traces are continuous pieces --

1 contiguous pieces of metal to the pins on the outside
2 of the package that are used to say plug the packaged
3 IC product into a PC board.

4 Q. So would you agree with me that Figure 9-2
5 does not show connecting pads together using bonding
6 wire?

7 A. I mean, it does not show that. The purpose of
8 this figure is to show the encapsulation method that's
9 used with plastic packages for protection.

10 Q. So it mentions a "top plastic" which, I think,
11 you were just referring to.

12 What is the "top plastic"?

13 A. I assume you're referring to the figure
14 caption, by the way, or is it somewhere in the text?

15 Q. Correct, correct. The figure caption,
16 Figure 9-2, that's right. So let me -- let me re-ask
17 the question.

18 In the caption for Figure 9-2, it refers to
19 the "top plastic."

20 What is the "top plastic" being referred to
21 here?

22 A. Well, this is what I described a moment ago.

1 I referred to the term in the art that's generally
2 used for finishing off a -- the package for
3 protection. It's called "encapsulation."

4 And the encapsulation method here as he
5 describes is that, once the wire bonding is done, then
6 this, the plast- -- molten plastic is poured in, and
7 that cools and -- and -- and hardens.

8 And so this flows in everywhere and
9 encapsulates things and protects them, once the --
10 the -- the bonding is done. It's a way of
11 encapsulating the circuit and protecting things from
12 the outside environment and freezing things in place,
13 a common method used.

14 Q. So after the bonding wire is added, plastic is
15 poured into it to help protect everything?

16 A. I wouldn't say "help."

17 Q. Is that what this is --

18 A. It's basically the -- the key protection. The
19 key protection is to encapsulate.

20 In other types of packaging and bonding,
21 there's other methods of encapsulation used, but
22 that's basically -- it's a finished product at that

1 point, so whatever you've done is done, and you don't
2 do any more. You're finished with the IC. You're
3 finished with the bonding. You encapsulate it, and --
4 and if it passes the final test, then you have a
5 product you can -- you can sell to a real paying
6 customer.

7 Q. All right. Let's turn now to your
8 Reply Declaration, Paragraph 56.

9 Do you have that in front of you?

10 A. That's the Beddingfield reference, I assume,
11 because I have to dig that out of a different binder.

12 Q. Yeah, I'm going to pull up the --

13 MR. WATSON: Let's pull up Exhibit 1041 and
14 put that on the screen.

15 THE CONCIERGE: Counsel, exhibit number again?
16 Sorry.

17 MR. WATSON: 1041.

18 (Deposition Exhibit 1041 was marked for
19 identification.)

20 THE WITNESS: I -- I disappeared because I'm
21 fighting with a big binder, but I'll come back in a
22 moment with my paper Beddingfield.

1 BY MR. WATSON:

2 Q. Okay.

3 A. After much struggle, I tore it out of the
4 binder, so I have Beddingfield's paper copy if we need
5 it.

6 Q. So, Dr. Foty, what's been marked as
7 Exhibit 1041 is the Beddingfield reference you refer
8 to in your Reply Declaration?

9 A. That appears to be the case, yes.

10 Q. And if you will look at the list of invent- --
11 inventors on the cover, you'll see Stanley Craig
12 Beddingfield, Kevin Peter, and Peter Harper.

13 Do you see that?

14 A. I see that. That's correct.

15 Q. Do you know any of those inventors?

16 A. No, I do not. I was unaware of them until I
17 saw this reference.

18 Q. And had you seen this reference prior to this
19 litigation?

20 A. No, I had not.

21 Q. Let's turn to Paragraph 15 of Beddingfield.

22 A. What paragraph number?

1 Q. 15.

2 A. 15? Okay. 1-5. I thought you said 5-0.

3 Sorry.

4 Q. And I'll give you a second to read that, and
5 then I'll ask you some questions.

6 A. (Witness perused document.) Okay. I've read
7 the paragraph. I may reread, just depending on what
8 your question is, of course.

9 Q. In Beddingfield, the jumper wire 160 is listed
10 as a parallel path of communication, correct?

11 A. In this particular instance, that's -- that's
12 what he calls it.

13 Q. Okay. And in this instance, the jumper wire
14 connects the inner portions of the circuitry 200 on
15 the die 120 with a pad, correct?

16 A. (Witness perused document.) He says that's
17 one option, yes.

18 Q. Okay. Well, what are the inner portions of
19 circuitry 200?

20 A. Well, I presume that's referring to circuitry
21 that is not near the periphery.

22 Q. Okay. Does that include circuitry that's on

1 the metal layers of the circuit?

2 A. In this particular instance, you would need
3 enough of a landing spot for a bond pad type of
4 structure to put the wire -- the jumper wire's other
5 end down.

6 Q. Okay. Now, the jumper wire allows for current
7 to not only flow through circuitry 200 but also
8 through the jumper wire 160, correct?

9 A. That's literally what he says.

10 Q. Okay. So when it talks about circuitry 200,
11 how is that different from a jumper wire?

12 A. He -- he seems to be referring to circuitry
13 200 as being the on-chip structures.

14 Q. And are those on-chip structures integrated --
15 involved -- strike that.

16 Do those on-chip structures involve integrated
17 circuit metallization?

18 A. That's presumably an inclusion. It refers to
19 the circuitry, which could ref- -- which could go
20 from -- all the way from the top down to the
21 transistor level in the silicon.

22 So he makes sort of a generic reference there,

1 but he basically is referring to a resistance path
2 running through on to the chip via the metal traces
3 and then down to the transistors and other structures.

4 Q. Now, let's go to Figure 2 of Bennington (sic).

5 A. You said "Bennington." I believe it's
6 Beddingfield.

7 Q. Beddingfield, excuse me.

8 A. I want to make sure that we don't have another
9 reference everyone's looking for next week.

10 Q. Yeah. Let's turn to Figure 2 of Beddingfield
11 and let me know when you're there.

12 A. Oh, I have that in front of me.

13 Q. Okay. Now, in Figure 2, what's marked as 140
14 is a package trace, correct?

15 A. He refers to them in Paragraph 13 as traces
16 140.

17 Q. And is trace 140 off package -- or -- excuse
18 me -- strike that. Let me rephrase that.

19 Is trace 140 off-chip?

20 A. (Witness perused document.) It appears that
21 it's off-chip. It's a trace in the package of some
22 sort.

1 Q. Okay. And connection 150 is a wire bond
2 connection, correct?

3 A. Beddingfield identifies it as such.

4 Q. Okay. Now, let's go to Paragraph 22 of this
5 Beddingfield reference.

6 A. 22, you said?

7 Q. Correct.

8 A. Okay. I've -- I've read the paragraph, so,
9 again, and I may reread parts, depending on your
10 questions.

11 Q. So in Paragraph 22, that also discusses how
12 jumper wires 160 provide a parallel path for
13 communications to various interior portions of the
14 grid, correct?

15 A. (Witness perused document.) Well, again, he
16 specifically says that in the paragraph with -- and he
17 seems to be referring to Figure 4.

18 Q. And then it also describes connecting
19 bond pads 580 with metallized rails 560, correct?

20 A. He seems to be showing that here.

21 Q. Okay. All right. You can put that to the
22 side.

1 A. (Witness perused document.)

2 MR. WATSON: Let's pull up Exhibit 1039.

3 (Deposition Exhibit 1039 was marked for
4 identification.)

5 THE WITNESS: After another struggle, I have
6 it.

7 BY MR. WATSON:

8 Q. What is Exhibit 1039?

9 A. It's a U.S. patent issued in 2002.

10 Q. Okay. And prior to this case, had you seen
11 this patent before?

12 A. No, I had not.

13 Q. And if you look at the list of inventors on
14 Exhibit 1039, do you recognize the names of any of
15 those inventors?

16 A. Well, I recognize them from exam- -- having
17 examined this patent before, but I do not personally
18 know any of them.

19 Q. Okay. Let's turn to the Abstract.

20 A. (Witness perused document.)

21 Q. Are you at the Abstract?

22 A. Oh, I'm at the Abstract. I was just starting

1 to read it.

2 Q. Okay. So according to the Abstract, Lee is
3 about a, [as read]:

4 Radiofrequency identification tag on a single
5 layer substrate.

6 Do you see that?

7 A. I see that, yes.

8 Q. What does it mean that there's a single layer
9 substrate?

10 A. I didn't consider that in great detail, but he
11 seems, in the summary of the invention, to describe
12 that as being one side of a dielectric substrate.

13 Q. And this refers to a "radiofrequency
14 identification tag."

15 Do you see that?

16 A. I see that, yes.

17 Q. Is a radiofrequency identification tag the
18 same thing as an integrated circuit?

19 A. It's a type of integrated circuit. They're
20 marketed -- or they're designed and marketed by many
21 companies as an integrated circuit.

22 Q. Okay.

1 A. He also --

2 Q. All right.

3 A. You know, just before -- just to -- actually,
4 he just -- this is -- again, we're looking at the
5 reference. He refers --

6 At Column 2, in the summary of the invention,
7 he refers to, [as read]:

8 RFID tag comprising a semiconductor integrated
9 circuit, which is the RFID tag device.

10 And so the RFID tag is con- -- it contains an
11 integrated circuit, as well as some other things, so
12 the "RFID tag device," as he calls it, is what I
13 described earlier.

14 It's an integrated circuit, and many of them
15 are made and marketed, and entire companies are
16 dedicated to their existence.

17 Q. All right. You can put that one away.

18 MR. WATSON: Let's go now to Exhibit 1040.

19 (Deposition Exhibit 1040 was marked for
20 identification.)

21 THE WITNESS: Whoops. Geez.

22 Okay. After another struggle, I have that

1 exhibit out in front of me.

2 (Coughing caused an interruption.)

3 THE WITNESS: Excuse me.

4 BY MR. WATSON:

5 Q. Okay. Do you recognize Exhibit 1040 as the
6 "Connor reference" you refer to in your Declaration?

7 A. Yes, it is. It's a U.S. patent. It was
8 issued in 2008.

9 Q. Okay. And prior to this case, were you aware
10 of any of the inventors listed in Exhibit 1040?

11 A. No, I was not. And I do not know them
12 personally.

13 Q. Okay. And were you aware of this patent prior
14 to this case?

15 A. No, I was not.

16 Q. Let's turn to Column 2 of Connor.

17 Okay. And let's go to Lines 40 through 46.

18 A. (Witness perused document.)

19 Q. And let me know when you're there.

20 A. Oh, I'm there. And I'm referring to Figure 4,
21 so I want to make sure I have access to Figure 4 as
22 well.

1 Q. Great. Yeah. I just want to make sure we're
2 on the same page of -- of what Connor labels things.

3 A. And I'll just note we -- we are coming up on a
4 need for a break before too long, when you get a good
5 place.

6 Q. Sounds good. We'll try and -- we'll try and
7 break after this reference, if that's okay. I know
8 you want one, so --

9 A. That's fine. I just can't go too much longer.

10 Q. Okay. All right. So, Dr. Foty, Connor labels
11 the flexible substrate as 10, correct?

12 A. He refers to 10 as the flexible substrate,
13 yes.

14 Q. And he labels the die as 14?

15 A. Yes. In looking at Figure 4, that makes
16 sense.

17 Q. Okay. And when he says a "die," is that
18 referring to a chip?

19 A. That's a term that's often used for an
20 integrated circuit, yes.

21 Q. Okay. And then he labels the -- Connor labels
22 the signal pads on the die as 16, correct?

1 A. Yes. And, again, this makes perfect sense in
2 the context of it being an integrated circuit, the
3 die 14.

4 Q. And then he labels the bond fingers, on the
5 circuit, as 18.

6 A. He refers to 18 as the bond fingers on the
7 substrate.

8 Q. Okay. Now let's go to Column 2, lines 50
9 through 52.

10 A. (Witness perused document.)

11 Q. Are you there?

12 A. Yes, I have that in front of me.

13 Q. Okay. So Connor labels the jumper wire bond
14 as "9," correct?

15 A. He says that in the text, but I'm looking for
16 9 in the figures. (Witness perused document.)

17 He inf- -- he refers to that here. He's
18 discussing Figure 4. As far as I can tell, he does
19 not, in Figure 4, have a 9, but he has a 9 back in
20 Figure 1, for example; Figures 1A and 1B show 9.

21 Q. Are you aware of Connor labeling the jumper
22 wire bond as anything, other than 9?

1 A. I'm not aware of it, and I would be surprised,
2 but I see he certainly does refer, in that paragraph,
3 to jumper bond wire 9.

4 Q. And looking -- again, at Lines 50 through 52
5 of Connor, in Column 2 -- in Connor, the bonding wire
6 connects the signal pads on the chip to the bond
7 fingers on the substrate, correct?

8 A. In Figure 2, for example, he shows the jumper
9 wire 9 connected between the trace, 18, and a -- a
10 pad, 16.

11 Q. And in Figures 6A and 6B of Connor, the bond
12 fingers, 18, are connected by a jumper wire bond, 9,
13 correct?

14 A. Sorry. Could I have that question again?
15 I lost track of all the paper on my desk.

16 Q. Uh-huh.

17 MR. WATSON: Can you, Court Reporter, repeat
18 the question?

19 THE COURT REPORTER: One moment, please.

20 MR. WATSON: Uh-huh.

21 THE COURT REPORTER: "And in Figures 6A and 6B
22 of Connor, the bond fingers, 18, are connected by a

1 jumper wire bond, 9, correct?"

2 THE WITNESS: Yes. I'm looking, now, at 6A
3 and 6B and reading the text regarding that, and he
4 refers to, [as read]:

5 The different bond wires are connected to each
6 other, using the jumper wire, 9.

7 BY MR. WATSON:

8 Q. So in Connor, Figures 6A and 6B, the bond
9 fingers -- strike that.

10 So on Figures 6A and 6B, the bond wire
11 connects the bond figures to the signal traces --
12 well, strike that. Sorry.

13 Let's go to Column 3, Lines 41 through 50.

14 A. Yes. That's where I went to when I was
15 examining 6A and 6B.

16 Q. Yeah. Yeah. So in figures 6A and 6B, the
17 bond fingers are connected with the jumping wire,
18 bond 9, reaching the signal traces, 20, correct?

19 A. Yes. He's connecting with a bond jump -- a
20 jumper bond wire, for example, two different traces,
21 18.

22 And so what he says in there is he's

1 essentially using that to allow -- he's using that to
2 connect the different bond figures, 18, together
3 for -- for the power provision, for example.

4 MR. WATSON: Okay. All right. Let's take our
5 break. I know you were asking for one, so let's take
6 our break.

7 THE WITNESS: I'd appreciate one. It's been
8 an hour and a half, so --

9 MR. WATSON: Yeah, I was going to take a break
10 anyways.

11 Let's go off the record.

12 THE WITNESS: Ten minutes?

13 MR. WATSON: Sure, that's fine.

14 THE WITNESS: Okay.

15 MR. WATSON: A ten-minute break sounds good.

16 (Recess taken from 8:27 a.m. to 8:39 a.m.)

17 BY MR. WATSON:

18 Q. Dr. Foty, welcome back.

19 A. Welcome back, Counselor.

20 Q. And did -- did you discuss your testimony with
21 anyone during the break?

22 A. No, I did not.

1 Q. Okay. Let's turn to Paragraph 70 of your
2 Reply Declaration.

3 MR. WATSON: And if we can put that on the
4 screen.

5 THE CONCIERGE: Is that the last document we
6 were on before break, Counsel?

7 MR. WATSON: The Declaration, Exhibit 1042.

8 THE CONCIERGE: Got it.

9 THE WITNESS: And by the way, I do have that
10 up on paper. And in a rare instance for today, this
11 paragraph is confined to one page.

12 BY MR. WATSON:

13 Q. Or -- excuse me -- let's go to page --
14 Paragraph 71. Sorry. Paragraph 71.

15 A. Now that one does split pages.

16 Q. Dr. Foty, in Paragraph 71, there's an image
17 shown.

18 What is that image of?

19 A. This is an image of a silicon IC, which is
20 glued or pasted or something or it's somehow placed --
21 connected physically to be in this package, this
22 package which hasn't been closed up yet.

1 And then there are wire bond traces running
2 from the bond pads out to the package traces, which
3 each one of those traces goes to a package pin.

4 Q. Where did this image come from?

5 A. This is an image of a Motorola part, which --
6 I believe the image does actually come from Wikipedia.

7 Q. So you nev- -- you did not take the picture in
8 this image, correct?

9 A. No, I did not. And this is exemplary. There
10 are -- you can find many images like this online.

11 Q. And do you know when this image was taken?

12 A. I don't know when the image was exactly taken,
13 but that's a Motorola part that's been around since
14 the 1990s.

15 Q. Now, in the original image you took from the
16 Internet, there is no wi- -- bonding wire that
17 connects the pads to each other, correct?

18 A. That is correct. This is illustrative to show
19 the lengths of bond wires versus the length of any
20 pad-to-pad jumper wires that would be included.

21 Q. And in Paragraph 71, you say that you add a
22 red line as an example of how bonding wire would

1 connect two pads together; is that fair?

2 A. That's fair. Again, we're trying to
3 illustrate the length of the bond pad to wire -- to
4 package trace lines versus the distance between two
5 pads that would be jumpered together, for example.

6 Q. So in this figure in Paragraph 71, the bonding
7 wires connect the pads to the packaging, correct?

8 A. They visibly connect to the package traces,
9 including the -- the ring which is a -- several are
10 connected to that ground ring which goes off to its
11 own pin.

12 Q. Okay. And the pads in this image in
13 Paragraph 70 (sic) are on the periphery of the chip,
14 correct?

15 A. Yes, that appears to be the case.

16 Q. And would you agree with me that most of the
17 bonding wire shown does not go over the chip?

18 A. In this particular part, consistent with what
19 Saint said earlier, it uses good practices for
20 connecting the pads to the package traces as directly
21 as possible.

22 Q. And would you agree with me that there is not

1 any circuitry beneath the bonding wire in this image?

2 A. In this particular instance, there -- there's
3 no circuitry underneath any of the particular bond
4 wires we see here. I'll agree with that.

5 Q. And is there any circuitry beneath the red
6 bonding wire that you drew?

7 A. There's no circuitry beneath there.

8 And before you continue there, my counsel -- I
9 don't know if he's -- if we've lost him or not, if
10 he's closed his video down or not.

11 THE WITNESS: Are you still there, Travis?

12 MR. JENSEN: Yes, I am. Sorry. I was just --

13 THE WITNESS: Sorry. I didn't know if I --
14 I -- you weren't there, if you dropped off because of
15 some technical issue, I wanted to make sure because
16 then that would be -- you know, obviously we'd have to
17 fix that. So sorry about that.

18 MR. JENSEN: I appreciate the concern. I was
19 just finishing a bite of breakfast due to the
20 West Coast time difference, so I took my video off.
21 But I'm back. I'm here.

22 THE WITNESS: No, no.

1 MR. JENSEN: I never left. I've always been
2 here.

3 THE WITNESS: Sorry. I just wanted to make
4 sure, Counselor, because if my counsel has
5 disappeared, then we'd have to fix that before we
6 continue.

7 MR. WATSON: Of course, of course.

8 And I'm glad, Travis, that you were there for
9 the whole thing, so that's good.

10 BY MR. WATSON:

11 Q. Dr. Foty, in this figure in Paragraph 71, how
12 are the pads connected to each other?

13 MR. JENSEN: Object to form.

14 THE WITNESS: They would only be connected, in
15 this particular instance -- exemplary instance of an
16 IC, in the conventional way where, you know, current
17 would flow in through a power pad and out through a
18 ground pad, so all connections here between pads would
19 have intervening circuitry.

20 Again, this is just exemplary to show the
21 length of bond wires, packaged trace -- packaged trace
22 bond wires compared to inter-pad spacing.

1 BY MR. WATSON:

2 Q. And in this instance, in the figure in
3 Paragraph 71, the connections between pads, would
4 those be made up of the metal layers of the chip?

5 MR. JENSEN: Object to form.

6 THE WITNESS: In this instance, the pads
7 likely, as I said, would be connected through complete
8 intervening circuitry, such as you have circuitry
9 between a power pad and a ground pad.

10 Again, this is just conventional for how a --
11 you know, a silicon chip behaves. And, again, the
12 purpose of this figure is exemplary. Again, it's to
13 show the difference in length between the pad spacing
14 and the trace to bond pad spacing.

15 BY MR. WATSON:

16 Q. And this figure you show in Paragraph 71 does
17 not show using bonding wire to connect pads to each
18 other, correct?

19 A. This particular figure raw does not show that.

20 Again, it was a -- a figure, exemplary figure,
21 to show scale.

22 Q. Now, is there any circuitry shown between

1 adjacent pads in this figure?

2 A. In this particular figure, unlike the other
3 microphotograph we look at -- looked at earlier here,
4 there is not circuitry between the pads in this
5 particular instance.

6 But, again, it's -- the purpose is the one I
7 stated several times already, the scale of the things.

8 Q. And does this figure show any ESD buses?

9 A. Like that earlier microphotograph, we can't
10 see into that level of detail because now you're
11 getting inside the chip.

12 Again, the purpose of this figure was what I
13 said earlier.

14 THE WITNESS: I need ten seconds to go close
15 the damper on the wood stove. You don't have to
16 pause. I'll be right back.

17 MR. WATSON: Well, I -- I was actually going
18 to say: I think I'm done with my questions.

19 I don't know if Travis has any.

20 THE WITNESS: Oh, okay. Sorry. I just --

21 I had -- during the break, I had put wood on
22 the stove and forgot to turn the damper, so I wanted

1 to make sure it didn't go too high, so I apologize.

2 That's happened in depositions before.

3 So sorry, Counselor. Go ahead.

4 MR. WATSON: Yeah.

5 Unless Travis has questions, I think I'm done.

6 THE WITNESS: Oh, thank you.

7 MR. JENSEN: Yeah. Give me -- give me just --

8 So you're passing the witness; is that right?

9 MR. WATSON: Yeah, I'll pass the witness.

10 MR. JENSEN: Okay.

11 THE WITNESS: Do you want to take a
12 five-minute break, Travis, to get your notes together
13 or anything like that, or --

14 MR. JENSEN: Yeah.

15 Why don't we just do five minutes.

16 THE WITNESS: Okay.

17 MR. JENSEN: I may not have any questions, but
18 let me just review.

19 THE WITNESS: Yeah.

20 MR. JENSEN: And if I have any, they won't --
21 it won't be very long.

22 MR. WATSON: Okay. Sounds good.

1 THE WITNESS: Okay. Thank you.

2 (Recess taken from 8:49 a.m. to 8:54 a.m.)

3 THE COURT REPORTER: Back on the
4 record, Counsel.

5 MR. JENSEN: No further questions from me.

6 MR. WATSON: Thank you so much, Dr. Foty.

7 THE WITNESS: Thank you, Counselor.

8 (Discussion had off the record.)

9 THE COURT REPORTER: And there is a three-day
10 expedite on this.

11 Would you like to receive it then, Mr. Jensen?

12 MR. JENSEN: No.

13 We'll just take the normal, standard delivery.

14 THE COURT REPORTER: And there's also a rough
15 draft, if you would like that.

16 MR. JENSEN: I don't think we need that.

17 (Deposition concluded at 8:54 a.m.)

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1 CERTIFICATE OF SHORTHAND REPORTER - NOTARY PUBLIC

2
3 I, COURTNEY N. LANGHOFF, CSR, RDR, CRR, FPR-C,
4 Notary Public within and for the States of Florida and
5 Wisconsin do hereby certify:

6 That DANIEL FOTY, Ph.D., the witness whose
7 deposition is hereinbefore set forth, was duly sworn
8 by me before the commencement of such deposition and
9 that such deposition was taken before and is a true
10 record of the testimony given by such witness.

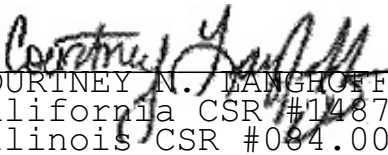
11 I further certify that the adverse party,
12 MICRON TECHNOLOGY, INC., was
13 represented by counsel at the deposition.

14 I further certify that the deposition of
15 DANIEL FOTY, Ph.D., occurred remotely via Zoom
16 videoconferencing on Friday, January 9, 2026,
17 commencing at 6:04 a.m. to 8:54 a.m. PST.

18 I further certify that I am not related to any of
19 the parties to this action by blood or marriage, I am
20 not employed by or an attorney to any of the parties
21 to this action, and that I am in no way interested,
22 financially or otherwise, in the outcome of this

1 matter.

2 IN WITNESS WHEREOF, I have hereunto set my hand
3 this 14th day of January, 2026.
4
5

6 
7 COURTNEY N. LANGHOFF, CSR, RDR, CRR, FPR-C
8 California CSR #14876
Illinois CSR #084.004996

9 Notary Public, State of Wisconsin
10 My Commission No.: 190335
Expires: 08/01/2029

11 Notary Public, State of Florida
12 My Commission No.: HH 609936
Expires: 03/05/2029
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DEPOSITION ERRATA SHEET

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Case Caption: MICRON TECH vs. YANGTZE MEMORY TECH.

DECLARATION UNDER PENALTY OF PERJURY

I declare under penalty of perjury that I have read the entire transcript of my deposition taken in the above-captioned matter or the same has been read to me, and the same is true and accurate, save and except for changes and/or corrections, if any, as indicated by me on the DEPOSITION ERRATA SHEET hereof, with the understanding that I offer these changes as if still under oath.

Signed on the _____ day of _____, 2026.

DANIEL FOTY, Ph.D.

Subscribed and sworn to on the ____ day of _____, 2026, before me _____
Notary Public, in and for the State of _____.

1 DEPOSITION ERRATA PAGE #1

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22 DANIEL FOTY, Ph.D.

Transcript of Daniel Foty, Ph.D.
Conducted on January 9, 2026

109

A			
al	19:20, 25:15,	85:9, 85:15,	94:4, 99:18
4:11	26:22, 34:13,	88:4, 91:1,	allow
ability	37:14, 38:20,	92:4, 92:14,	40:7, 40:8,
70:5	45:10, 49:18,	97:2, 99:20,	94:1
able	52:10, 53:13,	100:10, 100:11,	allowing
19:12, 43:22,	61:4, 64:4,	100:12, 100:20,	42:11, 47:14
49:7	64:11, 67:15,	101:6, 101:12	allows
about	74:10, 77:18,	ago	40:11, 40:13,
6:2, 10:11,	88:3, 96:6,	8:4, 8:15,	40:14, 40:15,
17:14, 30:13,	101:17	78:22	83:6
39:21, 50:19,	add	agree	almost
51:8, 51:9,	96:21	9:6, 9:17,	43:2
51:22, 52:2,	added	34:22, 37:4,	already
52:8, 52:17,	79:14	37:10, 41:19,	33:20, 34:2,
56:21, 56:22,	address	42:3, 42:5,	34:6, 34:16,
57:5, 57:21,	6:17, 6:21	44:9, 49:12,	101:7
58:10, 59:8,	adjacent	78:4, 97:16,	also
59:10, 59:14,	101:1	97:22, 98:4	2:19, 7:17,
59:15, 60:1,	advance	agreed	8:16, 22:10,
61:4, 65:10,	5:19	2:24	27:2, 28:8,
65:13, 66:22,	adverse	ahead	40:5, 41:16,
83:10, 87:3,	104:11	50:16, 102:3	56:10, 62:19,
98:17	affect	aircraft	70:13, 70:15,
above	60:2, 60:5	69:20	76:4, 83:7,
48:14, 64:3	affirm	al	85:11, 85:18,
above-captioned	6:1	3:37, 4:7, 4:12	88:1, 103:14
106:7	after	all	always
abstract	79:14, 81:3,	7:14, 8:2,	99:1
86:19, 86:21,	86:5, 88:22,	8:22, 9:1, 9:12,	amiss
86:22, 87:2	90:7	13:6, 14:7,	14:18
access	again	18:21, 22:17,	amount
15:11, 89:21	8:6, 10:21,	24:4, 27:11,	60:3, 60:6,
accommodate	13:21, 14:17,	31:9, 33:19,	60:16, 61:14,
53:20	24:3, 24:12,	35:13, 35:21,	64:22, 65:21,
according	27:14, 29:15,	37:11, 43:5,	68:13, 69:2,
87:2	31:16, 32:1,	43:14, 45:9,	69:12
accurate	32:2, 32:17,	46:19, 48:15,	analog
16:16, 106:8	33:8, 34:17,	48:21, 49:14,	48:15, 49:14,
across	34:21, 35:5,	51:7, 53:3,	50:3, 50:12,
39:10	39:21, 43:16,	54:16, 54:22,	50:19, 50:20,
action	48:18, 49:1,	55:7, 57:19,	51:7, 51:14,
104:19, 104:21	51:12, 51:15,	59:17, 66:21,	51:17, 51:18,
actual	51:22, 55:10,	70:4, 71:8,	52:4, 52:20,
32:7, 45:6	55:17, 58:20,	74:12, 74:15,	53:8, 53:15,
actually	61:3, 61:16,	75:17, 80:7,	54:15
7:13, 17:20,	66:3, 68:10,	83:20, 85:21,	analysis
	68:20, 70:6,	88:2, 88:17,	39:14, 49:5
	71:20, 80:15,	90:10, 92:15,	announce
			62:12

another 5:7, 39:5, 44:21, 49:8, 51:20, 68:5, 84:8, 86:5, 88:22 answer 4:25, 16:3, 23:6, 33:17, 40:2, 42:18, 46:4, 55:12, 56:9, 57:12, 73:1 answered 51:2 anticipate 5:5 any 5:10, 5:19, 7:7, 7:11, 8:18, 9:7, 9:18, 9:21, 15:10, 16:11, 16:20, 17:8, 18:10, 18:15, 20:1, 22:14, 22:19, 23:2, 24:2, 24:10, 29:10, 31:11, 32:9, 34:7, 34:9, 39:18, 41:21, 46:13, 57:9, 57:13, 57:21, 58:3, 58:6, 58:21, 60:15, 61:11, 61:12, 68:21, 76:10, 76:15, 80:2, 81:15, 86:14, 86:18, 89:10, 96:19, 98:1, 98:3, 98:5, 100:22, 101:8, 101:19, 102:17, 102:20, 104:18, 104:20, 106:9 anymore 57:4	anyone 9:3, 10:15, 94:21 anything 8:22, 14:20, 15:3, 20:13, 57:20, 60:10, 91:22, 102:13 anyway 77:16 anyways 94:10 apart 16:7 apologize 5:19, 32:18, 102:1 app 12:1 appeal 1:2 appear 11:20, 22:19, 46:15, 56:15, 70:13 appearance 9:5 appearing 2:8, 2:17 appears 12:1, 13:13, 41:18, 62:22, 81:9, 84:20, 97:15 applicant 3:22 application 4:10, 34:12, 41:8 applied 45:8 applies 33:15 appreciate 94:7, 98:18 area 28:10, 34:6, 46:17	around 8:8, 27:20, 46:17, 54:16, 54:22, 56:2, 73:7, 73:12, 73:20, 96:13 arrangement 26:19, 27:7 art 22:6, 22:12, 29:9, 32:12, 32:19, 35:2, 48:21, 50:2, 50:11, 71:21, 71:22, 79:1 article 19:21, 21:8, 22:1, 57:18, 58:20, 58:21, 59:8, 59:10, 61:3 articles 56:22, 57:2 aside 9:8 asked 50:6, 51:3 asking 94:5 assignment 106:2 assume 8:21, 14:4, 18:13, 26:7, 44:18, 78:13, 80:10 assuming 8:20 assure 55:22 attending 5:4 attention 14:21, 15:6, 25:5, 35:22, 70:10 attorney 104:20	author 57:18 avoid 69:1, 69:22 avoiding 17:8, 67:20, 69:11 avoids 64:11, 69:10 aware 5:7, 7:9, 16:10, 24:10, 24:12, 27:4, 32:11, 56:8, 57:9, 58:2, 58:6, 60:15, 61:12, 89:9, 89:13, 91:21, 92:1 away 5:11, 70:1, 88:17 B b1 3:36 b2 4:6 back 8:15, 13:11, 14:8, 17:17, 37:13, 39:8, 41:5, 42:22, 43:8, 43:14, 43:15, 47:17, 47:22, 60:8, 61:17, 61:18, 67:4, 80:21, 91:19, 94:18, 94:19, 98:21, 101:16, 103:3 backup 5:8 band 72:22, 73:2, 73:4, 73:11, 73:18, 73:20, 74:1
---	--	---	---

bands 72:19, 73:7 based 7:10, 17:12, 28:15, 29:4, 29:5, 33:5, 42:10, 45:7, 48:14 basically 27:5, 28:2, 40:6, 58:19, 60:9, 70:4, 73:6, 79:18, 79:22, 84:1 bates 62:17 because 23:7, 29:6, 30:12, 30:14, 31:8, 33:9, 33:19, 34:3, 39:17, 44:4, 45:19, 50:19, 51:2, 51:19, 53:1, 53:4, 54:5, 54:14, 55:5, 58:1, 59:6, 59:15, 60:21, 64:12, 66:20, 68:4, 70:22, 71:15, 75:8, 80:11, 80:20, 98:14, 98:15, 99:4, 101:10 becomes 74:1 beddingfield 4:12, 80:10, 80:22, 81:7, 81:12, 81:21, 82:9, 84:6, 84:7, 84:10, 85:3, 85:5 beddingfield's 81:4 been 30:6, 35:2,	40:17, 44:8, 56:17, 57:20, 58:9, 67:5, 81:6, 94:7, 95:22, 96:13, 99:1, 106:7 before 1:2, 5:16, 39:13, 40:2, 43:7, 43:18, 43:20, 56:9, 73:1, 74:4, 86:11, 86:17, 88:3, 90:4, 95:6, 98:8, 99:5, 102:2, 104:8, 104:9, 106:20 beg 60:4 begins 25:8, 25:9, 25:10, 26:10 behalf 1:29, 2:8, 2:17 behaves 100:11 being 20:18, 24:10, 29:14, 44:16, 45:4, 45:8, 47:7, 49:7, 52:5, 76:17, 78:20, 83:13, 87:12, 91:2 believe 12:21, 13:20, 15:13, 16:19, 22:6, 22:11, 36:14, 39:7, 40:19, 47:1, 48:7, 65:5, 68:2, 72:5, 77:17, 84:5, 96:6 below 19:19 beneath 22:14, 98:1,	98:5, 98:7 benefit 34:9 bennington 84:4, 84:5 best 5:7, 8:1, 54:6, 64:22, 65:20 between 2:24, 23:2, 23:14, 30:9, 31:20, 32:10, 34:3, 34:13, 35:4, 38:18, 38:22, 47:12, 47:13, 49:4, 56:8, 58:14, 60:16, 61:13, 63:19, 71:2, 75:15, 76:16, 92:9, 97:4, 99:18, 100:3, 100:9, 100:13, 100:22, 101:4 beyond 18:16 bidirectional 41:17, 41:20, 42:6, 44:10, 45:1 big 38:4, 80:21 bigger 33:20, 34:9, 35:6, 53:20 binder 38:4, 80:11, 80:21, 81:4 binders 7:20 bit 32:16, 32:18, 38:16, 76:22 bite 98:19 black 1:20, 6:20, 20:8	blackout 29:21 blah 40:15, 42:4 blank 7:15 blinking 10:20 block 24:6, 46:9, 49:8, 73:9, 73:10, 73:21, 74:4 blocks 45:20, 46:6, 46:7, 46:12, 46:14, 47:1, 47:4, 47:7, 47:12, 47:14, 49:4, 51:17, 52:20, 53:9, 53:15, 53:22, 54:10, 54:13, 54:21, 73:8 blood 104:19 blown 36:9 blue 62:13, 63:21, 64:5 bluff 2:13 board 1:2, 18:7, 21:6, 59:10, 59:14, 61:4, 69:3, 69:5, 78:3 board's 18:7 bond 19:15, 20:18, 21:7, 22:2, 22:17, 22:19, 22:22, 23:15, 54:9, 56:4, 56:7, 56:12, 56:14, 57:8,
--	--	--	---

57:10, 57:18, 57:19, 58:4, 58:15, 60:10, 63:11, 63:19, 66:17, 66:21, 67:2, 67:6, 67:13, 67:17, 68:16, 69:16, 69:17, 77:20, 83:3, 85:1, 85:19, 91:4, 91:6, 91:13, 91:22, 92:3, 92:6, 92:11, 92:12, 92:22, 93:1, 93:5, 93:8, 93:10, 93:11, 93:17, 93:18, 93:19, 93:20, 94:2, 96:1, 96:2, 96:19, 97:3, 98:3, 99:21, 99:22, 100:14 bonded 20:22 bonding 20:18, 21:12, 21:19, 22:15, 23:12, 57:2, 63:22, 64:22, 65:21, 68:13, 78:5, 79:5, 79:10, 79:14, 79:20, 80:3, 92:5, 96:16, 96:22, 97:6, 97:17, 98:1, 98:6, 100:17 bonds 57:14, 57:21, 58:7, 60:13, 61:10 book 7:18, 7:19, 52:1, 62:5, 68:11, 72:16, 77:18	bookmarks 7:16, 77:11 boron 70:22 both 31:18, 44:15, 45:4, 62:12 bottom 26:9, 60:8, 63:5, 72:12, 72:13, 72:17 break 43:3, 43:20, 90:4, 90:7, 94:5, 94:6, 94:9, 94:15, 94:21, 95:6, 101:21, 102:12 breakfast 98:19 bring 71:9 brings 30:16 bulk 72:7 bunch 75:18 bus 46:16, 49:7, 54:16, 54:17, 54:18, 54:21 buses 24:2, 24:11, 46:16, 52:9, 52:18, 53:14, 54:17, 54:18, 76:11, 76:14, 101:8 business 21:4, 73:3 C california 1:27, 2:5, 2:14, 105:9 call 57:16	called 19:11, 19:19, 19:20, 79:3 calls 64:3, 82:12, 88:12 cambridge 6:22 can't 7:13, 23:21, 24:3, 25:21, 31:6, 31:7, 34:5, 68:17, 90:9, 101:9 cannot 7:7, 35:4 caption 78:14, 78:15, 78:18, 106:3 case 1:3, 4:17, 7:16, 11:22, 12:4, 13:13, 14:5, 21:8, 28:12, 39:18, 41:18, 49:18, 50:20, 52:1, 52:6, 52:8, 52:17, 52:19, 53:21, 54:9, 54:11, 59:12, 81:9, 86:10, 89:9, 89:14, 97:15, 106:3 cases 31:19 cats 9:4 cause 6:2, 67:19 caused 42:13, 89:2 causes 60:22 certainly 92:2 certificate 3:7, 3:9, 104:1	certify 104:5, 104:11, 104:14, 104:18 chance 36:7, 43:21 change 42:2, 107:2, 107:5, 107:8, 107:11, 107:14, 107:17, 108:2, 108:4, 108:5, 108:8, 108:11, 108:14, 108:17 change: 107:4, 107:7, 107:10, 107:13, 107:16, 107:19, 108:7, 108:10, 108:13, 108:16, 108:19 changed 16:21 changes 106:9, 106:12 changing 65:6 chapter 34:18, 76:22, 77:7 charlie 74:16 chart 59:17 chat 11:9 chip 19:7, 22:5, 22:9, 23:5, 24:9, 27:18, 28:3, 30:20, 31:15, 33:20, 34:9, 46:2, 46:20, 47:16, 48:14, 53:4, 53:19, 54:5, 54:19, 55:1, 63:20, 72:7, 84:2, 90:18,
--	---	--	---

92:6, 97:13, 97:17, 100:4, 100:11, 101:11 chips 52:4 choice 48:14 choose 33:5, 55:21 christopher 3:33 circle 63:21, 64:5 circuit 20:2, 21:6, 28:10, 31:21, 34:6, 45:16, 45:19, 46:6, 46:7, 46:9, 46:12, 46:14, 47:1, 47:4, 47:7, 67:14, 69:3, 69:5, 79:11, 83:1, 83:17, 87:18, 87:19, 87:21, 88:9, 88:11, 88:14, 90:20, 91:2, 91:5 circuitry 22:14, 22:19, 24:6, 27:7, 27:15, 27:20, 28:2, 28:15, 29:4, 29:5, 29:18, 33:7, 38:15, 38:18, 44:19, 45:20, 49:4, 51:18, 73:22, 82:14, 82:19, 82:20, 82:22, 83:7, 83:10, 83:12, 83:19, 98:1, 98:3, 98:5, 98:7, 99:19, 100:8, 100:22, 101:4	circuits 34:17, 69:11 cite 39:14, 58:20 cited 8:13, 8:19, 18:10, 18:13, 61:4 cites 56:13 citing 9:13 claim 23:16 claims 16:17, 16:21 clarification 51:11 clarify 26:4, 38:16, 74:20, 75:2 clarifying 41:10 clean 7:14, 7:18, 7:22, 8:5, 9:1, 35:10, 47:19 clear 25:11, 26:11, 41:11 clearer 65:16 clearly 57:1, 57:6, 58:9 close 69:18, 101:14 closed 95:22, 98:10 coast 98:20 coffee 8:20 collectively 47:15 column 35:22, 36:3, 88:6, 89:16,	91:8, 92:5, 93:13 com 2:7, 2:16 come 14:20, 15:5, 39:8, 80:21, 96:4, 96:6 comes 9:22, 30:7, 30:20, 69:17 coming 28:22, 30:15, 31:18, 69:18, 90:3 commencement 104:8 commencing 104:17 commission 105:12, 105:15 common 79:13 communication 82:10 communications 85:13 companies 87:21, 88:15 company 1:7, 2:18, 4:16 compare 66:3 compared 68:18, 99:22 complete 10:3, 16:16, 100:7 complied 48:2 complimentary 5:17 comprising 88:8 compromising 40:12 computer 5:11	con 16:16, 29:15, 53:10, 88:10 concept 27:5 concern 98:18 concierge 2:20, 5:3, 11:8, 11:15, 13:6, 35:15, 35:17, 80:15, 95:5, 95:8 concluded 103:17 conclusion 15:14 conclusions 15:14, 17:11 condition 67:5 confined 95:11 confused 13:22, 30:11 connect 5:14, 52:9, 52:18, 53:22, 54:10, 54:13, 54:21, 94:2, 97:1, 97:7, 97:8, 100:17 connected 20:18, 22:21, 22:22, 23:5, 23:9, 23:19, 31:21, 37:1, 38:12, 47:5, 47:7, 55:10, 77:19, 92:9, 92:12, 92:22, 93:5, 93:17, 95:21, 97:10, 99:12, 99:14, 100:7 connecting 5:15, 21:19, 22:3, 23:12,
---	---	--	--

50:2, 53:3, 69:7, 78:5, 85:18, 93:19, 97:20 connection 23:2, 23:14, 48:21, 49:14, 50:2, 50:11, 51:7, 52:9, 52:18, 58:22, 64:20, 66:9, 66:10, 70:6, 85:1, 85:2 connections 30:18, 38:14, 47:11, 53:6, 76:16, 99:18, 100:3 connects 21:12, 21:15, 54:15, 55:5, 82:14, 92:6, 93:11, 96:17 connor 4:7, 89:6, 89:16, 90:2, 90:10, 90:21, 91:13, 91:21, 92:5, 92:11, 92:22, 93:8 conscious 71:18 consider 87:10 considerations 49:10, 49:13, 49:16, 51:6, 51:9, 51:10, 51:14, 51:16, 51:21, 52:3, 53:1 considered 49:2 consistent 97:18 constraints 52:21 constructed 17:12	contact 71:2, 71:4, 71:5, 71:6, 71:7, 71:11, 71:16, 73:22, 74:7, 74:8, 74:14, 74:15, 74:18, 75:1, 75:10, 75:14, 75:15 contacts 67:13, 71:9 contain 16:16 containing 32:4 contains 88:10 context 63:17, 64:14, 70:5, 75:3, 91:2 contiguous 21:1, 78:1 continue 28:17, 40:14, 98:8, 99:6 continued 4:1, 57:4 continuous 77:22 control 11:15, 45:10 conventional 17:13, 20:20, 70:22, 71:8, 72:6, 99:16, 100:10 conversations 5:12 cools 79:7 copies 7:14, 8:3, 8:16, 10:2 copy 7:14, 7:17, 7:18, 8:5, 11:5, 11:6, 11:11,	11:19, 13:14, 25:20, 35:11, 37:21, 38:6, 38:10, 45:12, 52:13, 62:3, 81:4 core-limited 20:5, 24:15, 26:18, 27:6, 28:12, 28:13, 29:10, 33:15, 34:12, 34:20 corner 62:17, 64:15, 70:11 correct 7:12, 11:9, 11:22, 12:1, 12:14, 12:15, 13:3, 13:4, 13:12, 14:3, 14:11, 14:21, 15:4, 15:6, 15:17, 18:16, 22:5, 24:11, 26:12, 29:2, 30:5, 31:2, 35:16, 36:12, 36:18, 41:2, 41:17, 45:3, 63:22, 65:8, 65:22, 72:3, 73:12, 77:20, 78:15, 81:14, 82:10, 82:15, 83:8, 84:14, 85:2, 85:7, 85:14, 85:19, 90:11, 90:22, 91:14, 92:7, 92:13, 93:1, 93:18, 96:8, 96:17, 96:18, 97:7, 97:14, 100:18 corrected 74:21 corrections 106:9	correlate 62:8 correlation 60:15, 61:13 coughing 89:2 could 11:2, 19:9, 28:21, 32:16, 33:4, 34:3, 34:13, 39:6, 39:7, 39:20, 43:6, 47:4, 52:14, 71:15, 83:19, 92:14 counsel 1:14, 2:25, 11:15, 17:18, 35:15, 80:15, 95:6, 98:8, 99:4, 103:4, 104:13 counselor 6:10, 10:19, 11:8, 25:3, 26:15, 28:17, 32:17, 45:19, 52:14, 65:17, 94:19, 99:4, 102:3, 103:7 counting 8:20 course 10:3, 12:6, 17:17, 18:18, 23:16, 25:20, 25:22, 45:8, 82:8, 99:7 court 5:21, 6:5, 42:16, 43:10, 92:17, 92:19, 92:21, 103:3, 103:9, 103:14 courtney 1:26, 104:3, 105:8 cover 81:11
---	---	---	---

craig 81:11 cram 29:18 crashed 43:19, 43:21 create 34:15, 71:1 creating 34:2 crr 1:26, 104:3, 105:8 cs1 54:2, 54:4, 55:4 csr 1:26, 1:27, 104:3, 105:8, 105:9, 105:10 current 30:17, 30:20, 32:5, 32:6, 60:21, 61:19, 75:9, 83:6, 99:16 curve 75:7 customer 80:6 cut 42:16, 42:18, 43:16, 72:7	3:36, 4:6, 4:11, 4:17 day 105:3, 106:13, 106:19 december 14:11, 14:13 decide 48:21, 50:2, 50:11 deciding 49:13, 51:6 decision 18:8 decisions 49:20 declaration 3:25, 4:13, 7:15, 8:3, 8:6, 8:11, 8:19, 11:21, 13:10, 13:17, 13:19, 13:21, 14:2, 14:10, 14:16, 14:22, 15:7, 15:10, 15:16, 16:22, 17:3, 17:7, 17:10, 17:16, 17:18, 17:20, 17:21, 18:6, 18:11, 18:22, 19:4, 20:4, 24:13, 24:19, 30:2, 33:12, 47:17, 47:18, 47:22, 52:11, 53:13, 55:16, 62:20, 63:1, 70:13, 75:19, 75:20, 76:3, 76:6, 76:8, 77:12, 77:13, 80:8, 81:8, 89:6, 95:2, 95:7, 106:4 declarations 12:12, 13:2,	16:15 declare 106:5 dedicated 88:16 definition 35:4 degree 64:4 delivery 103:13 demonstration 24:14 depending 82:7, 85:9 depiction 23:22, 25:11, 26:18 depictions 38:14 depo 2:20 depos 1:30, 106:2 deposition 1:11, 2:26, 3:11, 3:13, 3:15, 3:19, 4:3, 4:22, 5:18, 8:14, 9:7, 10:7, 10:14, 11:13, 12:3, 12:16, 13:7, 13:18, 17:10, 35:18, 37:17, 62:1, 80:18, 86:3, 88:19, 103:17, 104:7, 104:8, 104:9, 104:13, 104:14, 106:1, 106:6, 106:10, 107:1, 108:1 depositions 102:2 des 32:13 descends 69:19	describe 7:21, 17:6, 53:21, 57:2, 87:11 described 6:19, 48:14, 78:22, 88:13 describes 33:22, 36:11, 40:3, 49:18, 52:19, 59:4, 73:6, 79:5, 85:18 describing 27:15, 32:5, 33:9, 76:13 description 40:5 design 3:31, 20:5, 28:11, 28:13, 29:11, 33:1, 33:18, 33:22, 34:4, 34:20, 35:3, 48:14, 48:15, 48:16, 48:22, 49:14, 50:3, 50:12, 50:19, 50:20, 51:7, 51:14, 52:21, 53:2, 54:6, 54:14, 54:15, 55:11, 63:14, 64:1, 64:7, 66:5, 66:12, 66:15, 67:10, 68:10, 68:12, 68:19 designate 32:13, 32:20, 33:1 designation 33:5 designed 87:20 designers 27:13 designing 29:6
D			
damper 101:15, 101:22 daniel 1:11, 3:2, 3:25, 4:14, 6:15, 104:6, 104:15, 106:16, 107:21, 108:22 dark 43:7 date 1:16 dated 3:21, 3:28,			

designs 33:15 desk 8:5, 47:22, 92:15 detail 23:8, 23:21, 47:1, 56:21, 60:18, 87:10, 101:10 detailed 24:8 determine 28:11, 32:13, 32:20 determines 27:22 developing 28:7 deviated 12:8 device 88:9, 88:12 die 42:4, 82:15, 90:14, 90:17, 90:22, 91:3 diego 2:14 dielectric 87:12 differ 45:7 difference 30:9, 31:20, 32:1, 98:20, 100:13 differences 32:10 different 29:22, 30:14, 31:2, 31:3, 31:4, 31:5, 31:10, 31:11, 31:14, 31:15, 44:20, 45:7, 47:14, 49:2, 49:17, 51:14,	51:16, 51:17, 53:15, 54:10, 54:13, 62:7, 73:3, 73:8, 77:3, 80:11, 83:11, 93:5, 93:20, 94:2 differently 44:20 difficult 23:6 dig 37:21, 38:2, 80:11 digging 77:14 digital 40:9, 48:15, 48:22, 49:6, 49:8 diode 39:1, 39:2, 39:7, 39:18, 39:21, 40:6, 40:8, 40:13, 40:14, 40:20, 47:12, 71:17, 75:6 diodes 39:9, 39:12, 40:1, 40:16, 41:17, 41:20, 42:6, 44:10, 45:2 diotic 71:7 direct 3:5, 6:7, 23:14, 25:5, 26:2, 35:21, 38:21, 42:4, 67:21, 68:16, 70:9 directed 73:21 directly 64:19, 97:20 disappeared 80:20, 99:5	discharge 40:7, 40:15 discharged 47:15 discuss 10:18, 26:22, 39:13, 52:10, 57:18, 94:20 discussed 9:9, 10:14, 22:1 discusses 56:14, 67:8, 69:1, 69:11, 85:11 discussing 58:21, 73:4, 91:18 discussion 52:11, 59:14, 74:12, 74:15, 77:2, 103:8 discussions 5:10, 63:18 disembodied 44:7 distance 97:4 disturb 73:9 diving 69:17 document 9:13, 9:14, 18:1, 19:1, 20:11, 22:16, 24:22, 32:15, 33:13, 36:2, 38:3, 41:4, 41:13, 44:13, 47:21, 48:6, 52:12, 53:16, 63:8, 70:12, 77:9, 82:6, 82:16, 84:20, 85:15, 86:1, 86:20, 89:18, 91:10, 91:16,	95:5 documents 7:14, 7:22, 9:8, 9:11, 9:15, 9:18 doing 17:12, 28:2, 36:8, 53:4, 59:16, 64:8, 67:11, 67:12 domains 53:8 done 34:3, 79:5, 79:10, 80:1, 101:18, 102:5 doped 70:20, 70:21, 71:5, 75:5 down 19:21, 29:19, 33:11, 39:8, 71:4, 71:9, 72:12, 72:13, 83:5, 83:20, 84:3, 98:10 dr 3:25, 4:13, 6:9, 11:5, 11:17, 12:11, 12:13, 13:10, 15:17, 16:4, 16:8, 16:12, 17:5, 34:22, 35:21, 43:14, 56:11, 60:11, 81:6, 90:10, 94:18, 95:16, 99:11, 103:6 draft 103:15 draw 15:14 drawn 20:14 drew 98:6 drive 1:31, 2:13
--	--	---	--

driven 32:22 droop 67:7, 70:3 drooping 68:8 drop 11:9 dropped 98:14 drops 5:19 dual 39:1, 39:2, 39:6, 39:9, 39:12, 39:18, 39:21, 40:1, 40:6, 40:8, 40:13, 40:14, 40:16, 40:20, 47:12 due 6:22, 98:19 duly 104:7 during 9:6, 57:6, 94:21, 101:21 E e 48:15, 48:18 each 5:16, 10:13, 23:5, 23:19, 47:8, 93:5, 96:3, 96:17, 99:12, 100:17 earlier 31:6, 32:3, 40:22, 74:6, 74:20, 75:2, 75:3, 76:22, 77:7, 77:22, 88:13, 97:19, 101:3, 101:9, 101:13 early 6:11, 6:12	easier 7:18, 8:6, 12:3, 62:5 easily 64:8 easy 12:7, 72:16 edge 63:20 edges 22:5 effect 58:1 effectively 75:16 either 29:12 electromagnetic 60:8, 60:20, 61:17 element 44:14, 44:15, 44:16, 45:3 elements 45:5, 47:4 else 9:3 employed 104:20 empty 34:5 enabled 5:13 encapsulate 79:19, 80:3 encapsulates 79:9 encapsulating 79:11 encapsulation 78:8, 79:3, 79:4, 79:21 end 10:20, 83:5 end-type 71:17 engineer 34:8	engineering 3:31, 23:7 english 37:20 enough 15:13, 23:8, 36:9, 59:5, 59:20, 83:3 ensure 71:10 entire 20:9, 27:1, 88:15, 106:6 environment 79:12 errata 3:11, 3:13, 3:15, 106:1, 106:10, 107:1, 108:1 esd 24:2, 24:11, 40:7, 40:11, 40:15, 44:15, 45:2, 45:4, 47:14, 76:11, 76:14, 101:8 esds 40:15 esquire 2:2, 2:11 essential 3:32 essentially 21:1, 67:11, 73:17, 74:3, 94:1 et 3:37, 4:7, 4:12 even 12:22, 56:15, 58:7 evening 17:4 event 40:7 events 47:15	eventually 39:10 ever 34:19, 57:14, 60:11 everyone 5:3, 65:16 everyone's 84:9 everything 79:15 everywhere 79:8 evidence 57:13 ex 24:8 exactly 96:12 exam 86:16 examination 3:2, 3:5, 6:7, 24:8 examine 57:20, 61:18, 64:13 examined 19:9, 86:17 examining 22:16, 93:15 example 9:14, 20:5, 29:8, 31:5, 40:8, 40:20, 46:9, 48:19, 49:2, 49:5, 49:19, 56:18, 67:15, 67:18, 72:8, 91:20, 92:8, 93:20, 94:3, 96:22, 97:5 except 106:9 excerpt 66:14 excerpted 68:2
--	--	--	---

Transcript of Daniel Foty, Ph.D.
Conducted on January 9, 2026

118

excuse 17:5, 24:16, 42:1, 76:8, 84:7, 84:17, 89:3, 95:13 executive 8:2 exemplary 96:9, 99:15, 99:20, 100:12, 100:20 exhibit 3:20, 3:25, 3:30, 3:35, 4:5, 4:9, 4:13, 11:2, 11:13, 11:17, 11:21, 12:13, 13:5, 13:7, 13:10, 14:3, 14:8, 14:10, 14:16, 35:9, 35:18, 37:15, 37:17, 47:18, 56:10, 61:22, 62:1, 62:14, 70:11, 76:5, 80:13, 80:15, 80:18, 81:7, 86:2, 86:3, 86:8, 86:14, 88:18, 88:19, 89:1, 89:5, 89:10, 95:7 exhibits 3:19, 4:3, 4:22, 8:3, 8:9, 8:11, 8:14, 8:17, 17:11, 18:9, 43:6 existence 88:16 existing 58:7 expect 42:9 expedite 103:10 experience 18:19, 52:3,	69:21 expert 16:12 expires 105:13, 105:16 explain 38:11, 74:19 explained 27:3 expose 19:13 expressly 37:5 extent 67:6 F f-o-t-y 6:16 factor 27:19 factors 49:1 fair 9:19, 21:13, 22:9, 22:10, 28:14, 29:3, 31:14, 31:22, 46:1, 61:14, 65:15, 68:14, 68:15, 69:3, 69:9, 69:13, 97:1, 97:2 fairly 21:22, 68:17 far 10:2, 20:13, 20:15, 34:21, 91:18 fast 43:8 fax- (2:6, 2:15 features 23:22, 68:18 few 8:15, 10:8, 15:1, 74:2	field 60:22 fighting 80:21 figure 22:20, 23:11, 24:3, 25:12, 27:12, 36:13, 36:14, 38:1, 38:8, 38:11, 39:12, 39:15, 40:1, 40:17, 40:19, 41:1, 41:12, 41:13, 41:16, 45:9, 45:13, 45:15, 46:1, 46:7, 46:19, 53:12, 54:2, 54:4, 55:4, 55:6, 62:18, 62:20, 62:22, 63:17, 63:21, 64:6, 64:11, 64:13, 64:14, 64:21, 65:4, 65:10, 65:20, 66:3, 67:16, 67:22, 69:17, 70:6, 70:9, 70:13, 70:16, 70:19, 73:11, 75:17, 75:19, 76:10, 76:15, 76:18, 77:1, 77:5, 77:19, 78:4, 78:8, 78:13, 78:15, 78:16, 78:18, 84:4, 84:10, 84:13, 85:17, 89:20, 89:21, 90:15, 91:18, 91:19, 91:20, 92:8, 97:6, 99:11, 100:2, 100:12, 100:16, 100:19, 100:20, 101:1,	101:2, 101:8, 101:12 figures 36:18, 41:7, 41:21, 42:6, 44:11, 65:6, 91:16, 91:20, 92:11, 92:21, 93:8, 93:10, 93:11, 93:16, 94:2 filed 14:14, 16:5 final 17:4, 26:8, 55:5, 69:20, 80:4 finally 26:15 financially 104:22 find 8:7, 48:9, 52:11, 75:20, 76:6, 96:10 fine 14:17, 43:3, 63:3, 90:9, 94:13 fingers 91:4, 91:6, 92:7, 92:12, 92:22, 93:9, 93:17 finish 43:22 finished 28:19, 79:22, 80:2, 80:3 finishing 79:2, 98:19 firing 34:8 first 8:14, 17:20, 17:22, 20:4, 29:13, 51:13, 56:16
---	--	---	---

fit 9:15 five 102:15 five-minute 102:12 fix 98:17, 99:5 fletcher 1:21, 6:21, 7:1 flexible 90:11, 90:12 flip 55:20 floor 55:5, 55:8 florida 1:28, 104:4, 105:14 flow 83:7, 99:17 flowing 61:19 flows 79:8 following 25:14, 73:7 foolishly 35:5 forever 22:12 forget 60:7 forgot 101:22 form 7:18, 9:10, 9:20, 15:14, 15:15, 15:19, 15:22, 41:3, 42:8, 44:12, 45:17, 46:21, 49:15, 50:4, 50:13, 50:17, 54:1, 55:2, 58:5, 61:15, 65:3, 66:1, 66:19, 69:4,	69:14, 72:4, 73:13, 74:9, 99:13, 100:5 formed 17:11 forming 18:17 forth 17:17, 104:7 foty 1:11, 3:2, 3:25, 4:14, 6:9, 6:15, 11:5, 11:17, 12:11, 12:13, 13:10, 17:5, 35:21, 43:14, 81:6, 90:10, 94:18, 95:16, 99:11, 103:6, 104:6, 104:15, 106:16, 107:21, 108:22 found 38:4 four 52:20, 53:8, 53:14, 54:18, 57:7 foxtrot 6:16 fpr-c 1:26, 104:3, 105:8 free 67:11, 68:20 freezing 79:12 frequently 52:5 friday 104:16 front 7:22, 11:17, 12:2, 18:2, 18:4, 19:2, 25:2, 28:13, 38:8, 41:15, 45:13, 52:13,	57:13, 62:19, 63:2, 70:15, 70:16, 80:9, 84:12, 89:1, 91:12 frozen 42:18, 42:20 full 6:13, 7:8 function 40:11, 42:3, 42:11, 42:12, 45:2, 61:19 functional 32:1, 32:9, 44:9 functionalities 31:4 functionality 30:13, 30:14, 31:2, 40:4, 40:11, 41:20, 42:5, 44:10, 44:19, 45:1 functioning 45:7 functions 31:10, 31:14, 31:16, 32:5 further 74:2, 103:5, 104:11, 104:14, 104:18 G g1 36:12, 36:19 g2 36:12, 36:19 g3 36:12, 36:20 geez 88:21 generally 30:5, 30:22, 38:2, 61:8, 79:1 generic 83:22	gets-the-enginee- r-fired 66:5 getting 6:11, 52:13, 60:8, 67:7, 101:11 give 6:2, 38:2, 38:5, 43:21, 47:19, 82:4, 102:7 given 63:17, 104:10 glad 99:8 glued 95:20 go 9:12, 16:1, 17:19, 17:20, 17:21, 18:21, 20:21, 21:9, 21:22, 22:1, 23:1, 24:7, 30:4, 33:11, 37:13, 39:1, 39:6, 39:8, 42:21, 43:8, 48:1, 50:16, 55:7, 55:15, 61:16, 61:18, 62:5, 62:16, 62:21, 68:6, 69:17, 70:9, 72:12, 72:13, 75:17, 76:21, 77:5, 83:19, 84:4, 85:4, 88:18, 89:17, 90:9, 91:8, 93:13, 94:11, 95:13, 97:17, 101:14, 102:1, 102:3 go-around 8:4, 13:14 goes 60:21, 65:1,
---	--	--	--

Transcript of Daniel Foty, Ph.D.
Conducted on January 9, 2026

120

65:21, 67:18, 68:13, 96:3, 97:10 going 21:7, 22:2, 28:17, 31:18, 37:22, 38:1, 42:1, 57:3, 71:16, 73:19, 80:12, 94:9, 101:17 gone 14:18 good 6:9, 6:10, 33:9, 43:15, 63:14, 64:4, 64:10, 64:12, 66:4, 66:11, 67:9, 68:10, 68:12, 68:19, 75:8, 90:4, 90:6, 94:15, 97:19, 99:9, 102:22 great 87:10, 90:1 green 16:1 grid 85:14 ground 28:4, 30:3, 30:10, 30:18, 31:1, 31:8, 31:13, 31:21, 32:4, 32:10, 32:14, 32:20, 33:3, 37:1, 37:6, 37:8, 37:10, 49:7, 52:9, 52:18, 53:5, 53:14, 54:3, 55:9, 97:10, 99:18, 100:9 grounds 53:3, 53:7,	53:9, 54:17, 54:19 group 51:20 groups 36:12, 36:21 guard 72:19, 72:22, 73:2, 73:4, 73:7, 73:11, 73:18, 73:20, 74:1 guess 6:10, 8:2, 41:22 H half 10:13, 94:8 hand 5:22, 105:2 hang 25:14 happen 12:21 happened 43:18, 102:2 happens 8:22, 67:13 happy 26:3, 65:17 haralabidis 40:4 hard 46:10, 46:12 hardens 79:7 harper 81:12 haz 69:15 hazard 69:16, 69:20 head 60:7, 61:2 heavily 70:20, 70:21 help 5:13, 79:15,	79:16 helped 26:5 helpful 13:1 here 8:5, 11:6, 12:22, 18:5, 18:17, 22:17, 22:19, 23:8, 23:10, 24:5, 26:10, 29:18, 29:20, 36:11, 36:16, 38:5, 43:3, 50:22, 54:5, 55:20, 56:21, 57:20, 61:3, 61:12, 62:21, 63:18, 65:6, 68:19, 70:4, 72:13, 72:16, 72:17, 73:4, 73:14, 73:20, 76:13, 76:20, 77:21, 78:21, 79:4, 85:20, 91:17, 98:4, 98:21, 99:2, 99:18, 101:3 hereby 2:24, 104:5 herein 18:13 hereinbefore 104:7 hereof 106:11 hereunto 105:2 herrington 2:3 hh 105:15 high 2:13, 102:1 higher 67:6	hmm 10:13 holiday 10:9 home 6:17 hopefully 74:19 horrible 64:1 hotel 74:16 hour 43:2, 94:8 hours 10:13 house 30:16 humans 9:4 hungerford 1:31 I ic 3:31, 19:6, 19:13, 21:3, 21:4, 21:5, 23:9, 24:4, 24:8, 24:15, 30:17, 33:7, 35:6, 55:10, 78:3, 80:2, 95:19, 99:16 identical 11:20 identification 11:14, 13:8, 35:19, 37:18, 62:2, 80:19, 86:4, 87:4, 87:14, 87:17, 88:20 identified 45:20, 45:21 identifies 44:16, 45:4, 85:3
---	---	--	--

identify 5:13, 5:15 illinois 1:27, 105:10 illuminating 52:2 illustrate 97:3 illustrative 47:2, 96:18 image 19:17, 95:16, 95:18, 95:19, 96:4, 96:5, 96:6, 96:8, 96:11, 96:12, 96:15, 97:12, 98:1 images 96:10 immunity 40:14, 42:11 improved 56:22, 57:10, 58:3 improvements 56:4, 56:8, 56:17, 57:10, 58:3 inc 1:4, 2:9, 4:15, 104:12 include 29:19, 82:22 included 20:3, 96:20 includes 41:16 including 18:6, 97:9 inclusion 83:18 india 74:16 indicate 64:6, 64:7 indicated 106:10	indicates 21:8 indirectly 64:2 inductance 57:10, 57:19, 57:22, 58:4, 58:9, 58:14, 59:6, 59:10, 59:12, 59:13, 60:3, 60:6, 60:9, 60:17, 61:2, 61:6, 61:8, 61:14 inductive 56:12 inf 91:17 information 4:27, 17:8 inherently 58:22 initial 3:18, 4:2, 4:21 inner 82:14, 82:18 input 37:1 inside 33:7, 34:5, 45:20, 55:10, 101:11 instance 22:18, 53:6, 55:3, 82:11, 82:13, 83:2, 95:10, 98:2, 99:15, 100:2, 100:6, 101:5 instantiation 23:15 institution 18:7, 18:8 instructed 4:25 integrated 83:14, 83:16, 87:18, 87:19,	87:21, 88:8, 88:11, 88:14, 90:20, 91:2 integrity 49:9 intended 64:5, 64:7 intentional 55:21, 56:1 inter 3:27 inter-pad 99:22 interested 104:21 interestingly 38:21 interior 85:13 internet 42:13, 96:16 interruption 42:13, 89:2 intervening 56:4, 56:7, 99:19, 100:8 intra-block 40:12 invent 81:10 invention 87:11, 88:6 inventor 3:24 inventors 81:11, 81:15, 86:13, 86:15, 89:10 involve 83:16 involved 12:22, 20:1, 83:15 involving 57:21 ipr 1:3, 11:22, 12:5	issue 10:22, 27:1, 27:2, 44:21, 98:15 issued 86:9, 89:8 it'll 12:7, 62:7 iv 75:1, 75:7, 75:10, 75:11 J january 1:15, 3:3, 104:16, 105:3 jensen 2:2, 9:10, 9:20, 10:10, 10:12, 10:15, 10:17, 11:1, 15:19, 15:22, 41:3, 42:8, 42:20, 43:2, 44:12, 45:17, 46:3, 46:21, 49:15, 50:4, 50:13, 50:17, 54:1, 55:2, 58:5, 61:15, 65:3, 66:1, 66:19, 69:4, 69:14, 72:4, 73:13, 74:9, 98:12, 98:18, 99:1, 99:13, 100:5, 102:7, 102:10, 102:14, 102:17, 102:20, 103:5, 103:11, 103:12, 103:16 job 1:30 johnson 56:11, 57:17, 61:9 join 53:16, 53:17,
--	--	--	---

Transcript of Daniel Foty, Ph.D.
Conducted on January 9, 2026

122

53:18, 54:4 joins 54:5, 55:6 judgment 53:2 judy 3:33 jump 93:19 jumper 23:14, 82:9, 82:13, 83:4, 83:6, 83:8, 83:11, 85:12, 91:13, 91:21, 92:3, 92:8, 92:12, 93:1, 93:6, 93:20, 96:20 jumpered 97:5 jumping 93:17	know 8:7, 9:1, 9:4, 10:1, 10:2, 10:3, 10:21, 10:22, 16:2, 16:8, 20:13, 20:15, 26:2, 28:16, 30:12, 30:16, 31:16, 34:21, 36:6, 43:17, 44:4, 44:5, 44:8, 46:8, 51:8, 55:19, 61:17, 61:19, 68:17, 71:18, 75:18, 81:15, 84:11, 86:18, 88:3, 89:11, 89:19, 90:7, 94:5, 96:11, 96:12, 98:9, 98:13, 98:16, 99:16, 100:11, 101:19 knowledge 12:19, 18:19	17:2, 17:4, 25:6, 38:4, 48:3, 95:5 later 73:16 latham 2:12 law 75:11 layer 45:16, 46:2, 47:6, 67:19, 87:5, 87:8 layers 19:8, 23:19, 47:5, 54:12, 54:22, 67:14, 83:1, 100:4 layout 3:32 learn 20:6 least 35:2, 36:19, 36:21, 37:5 lee 3:37, 87:2 left 11:6, 15:2, 41:14, 55:7, 62:12, 70:11, 99:1 length 60:2, 60:5, 60:16, 61:2, 61:13, 96:19, 97:3, 99:21, 100:13 lengths 96:19 lengthy 68:18 less 51:18, 56:12 let's 13:5, 14:8, 17:19, 17:20, 17:21, 18:21,	24:18, 35:8, 35:12, 37:13, 37:14, 38:3, 42:21, 43:5, 43:6, 45:9, 47:17, 48:1, 55:15, 61:21, 62:16, 70:9, 72:12, 75:17, 76:21, 77:5, 80:7, 80:13, 81:21, 84:4, 84:10, 85:4, 86:2, 86:19, 88:18, 89:16, 89:17, 91:8, 93:13, 94:4, 94:5, 94:11, 95:1, 95:13 level 19:13, 23:9, 23:20, 23:21, 24:4, 24:5, 24:7, 24:9, 31:15, 46:22, 54:5, 60:18, 69:6, 83:21, 101:10 li 3:24 lightly 71:4, 75:5 liked 15:11 likely 71:6, 100:7 limit 64:22, 65:21, 68:12 limiting 27:19 line 20:8, 20:14, 60:9, 67:21, 72:2, 75:11, 75:12, 76:7, 77:14, 96:22, 107:2, 107:5,
K	L		
keep 52:6, 63:10, 66:20, 67:2, 70:1 keeps 53:8 kevin 81:12 key 79:18, 79:19 khat 17:5 khatrri 15:17, 16:4, 16:8, 16:12, 34:22, 56:11, 60:11 khatrri's 17:9, 57:15 kind 41:7, 43:7 kindly 6:5	labeling 91:21 labels 90:2, 90:10, 90:14, 90:21, 91:4, 91:13 lack 6:22 landing 83:3 langhoff 1:26, 104:3, 105:8 language 12:8 large 49:11, 49:12, 51:6 last 13:14, 14:12,		

107:8, 107:11, 107:14, 107:17, 108:2, 108:5, 108:8, 108:11, 108:14, 108:17 linear 75:2, 75:7 lines 29:21, 35:22, 36:4, 70:1, 89:17, 91:8, 92:4, 93:13, 97:4 link 19:19 list 8:11, 18:5, 18:16, 81:10, 86:13 listed 18:9, 82:9, 89:10 lit 54:4 literally 53:16, 53:17, 54:5, 83:9 literature 56:20 litigation 62:15, 81:19 little 30:11, 38:16, 38:17, 46:12, 68:9, 75:4, 76:22 llc 1:30 llp 2:3, 2:12 load 59:15 located 7:2, 22:5 location 1:20, 6:20, 7:3 locations 33:6	long 10:11, 37:22, 90:4, 102:21 longer 67:6, 90:9 look 7:10, 7:19, 24:9, 31:5, 31:9, 32:2, 35:3, 56:14, 62:5, 62:8, 81:10, 86:13, 101:3 looked 101:3 looking 31:6, 32:3, 44:13, 84:9, 88:4, 90:15, 91:15, 92:4, 93:2 looks 11:7, 39:6, 39:7 lost 44:3, 92:15, 98:9 low 37:8, 59:13, 59:20, 71:10, 75:13 lower 46:9 lunch 67:11, 68:20 M macro 24:5 made 56:17, 88:15, 100:4 magnetic 60:22 magnitude 59:3 mailing 6:21	mainly 20:3, 38:1 maintain 54:19 make 8:6, 9:5, 12:3, 27:18, 29:1, 33:19, 34:7, 34:8, 35:5, 35:13, 38:16, 39:17, 39:19, 40:3, 41:11, 49:20, 53:4, 53:10, 53:19, 56:16, 56:19, 67:21, 68:7, 68:15, 70:2, 71:1, 76:21, 77:12, 84:8, 89:21, 90:1, 98:15, 99:3, 102:1 makes 26:21, 51:10, 64:15, 64:18, 65:16, 75:13, 83:22, 90:15, 91:1 making 71:16, 71:22 many 27:12, 28:10, 34:5, 49:1, 57:3, 73:2, 87:20, 88:14, 96:10 mark 2:20 marked 4:22, 11:13, 13:7, 35:18, 37:17, 40:17, 62:1, 80:18, 81:6, 84:13, 86:3, 88:19 market 57:5, 57:7 marketed 87:20, 88:15	marks 9:2 marriage 104:19 marsh 2:4 martinez 2:20 marvelous 27:14 maryland 1:32 mask 3:31 mat 12:20 matching 59:16 material 18:7 materials 7:11, 8:4, 8:16, 8:18, 8:19, 8:21, 10:8, 15:10, 17:9, 18:5, 18:9, 18:10, 18:15, 18:16, 18:18, 30:7, 30:8 matter 8:21, 16:13, 59:13, 68:6, 105:1, 106:7 matters 9:12, 61:2, 61:3, 61:5 maybe 28:5, 50:21 mcgraw-hill 3:30 mean 8:21, 22:7, 23:13, 31:11, 45:18, 47:7, 58:18, 65:5, 68:17, 70:19, 77:3, 78:7, 87:8
---	---	---	--

Transcript of Daniel Foty, Ph.D.
Conducted on January 9, 2026

124

meaning 48:19 means 18:14, 19:8, 34:4, 63:19, 75:1, 75:10 mediated 67:5 mediation 49:4 meetings 10:11 memory 1:7, 2:18, 3:22, 4:16, 106:3 menlo 2:5 mention 34:19, 35:1 mentions 78:10 mess 47:19 met 16:9 metal 20:21, 21:1, 21:16, 23:19, 24:4, 31:12, 32:8, 45:16, 46:2, 47:5, 58:15, 59:4, 67:14, 67:18, 68:13, 69:12, 70:1, 71:2, 71:5, 73:18, 75:4, 78:1, 83:1, 84:2, 100:4 metallization 24:9, 46:13, 46:15, 46:20, 54:12, 54:22, 55:10, 83:17 metallized 85:19 method 48:21, 49:14,	50:2, 50:11, 51:7, 78:8, 79:4, 79:13 methods 52:9, 52:18, 79:21 mic 5:12 micron 1:4, 2:8, 4:14, 104:12, 106:3 microphotograph 31:6, 32:2, 101:3, 101:9 middle 42:19, 69:18, 76:7, 77:14 might 43:17 mike 43:6, 74:16 minimal 63:7 minimize 67:10, 68:7 minimizing 67:22, 69:2, 69:12 minor 15:1 minutes 44:8, 94:12, 102:15 missing 9:22 misspelled 15:2 mix 10:4 mixed 31:19, 50:22 mixed-signal 48:16 molten 79:6 moment 9:19, 38:5, 47:19, 78:22,	80:22, 92:19 money 68:21 months 8:4, 8:15 more 21:14, 24:8, 27:8, 27:16, 28:22, 33:20, 34:2, 34:14, 34:16, 38:21, 53:20, 64:18, 80:2 morning 6:9, 6:10 mos 71:22 most 59:5, 66:6, 68:3, 97:16 motorola 96:5, 96:13 mountain 1:20, 6:20 much 27:7, 28:10, 64:18, 66:18, 81:3, 90:9, 103:6 multiple 36:12 mute 5:11 myself 33:9	natures 24:6 near 82:21 necessary 9:15 need 7:16, 10:18, 15:3, 27:9, 27:17, 28:1, 28:6, 28:10, 28:11, 28:15, 29:17, 29:20, 33:21, 34:2, 34:15, 34:17, 38:6, 38:9, 39:19, 59:15, 76:3, 77:12, 81:4, 83:2, 90:4, 101:14, 103:16 needed 29:4, 34:14, 45:13, 52:14 needs 28:15, 29:4, 29:5, 33:6, 74:20 negligible 59:7, 75:16 nev 96:7 never 16:9, 29:13, 56:14, 58:9, 99:1 next 72:15, 74:2, 84:9 nice 51:22, 70:6 noise 40:9, 40:12, 40:14, 42:11, 47:13, 49:6, 49:8, 73:8, 74:3 noisy 51:18, 73:9,
N			
		n+ 71:10 name 6:13, 6:15, 57:17 named 19:18 names 86:14 nature 8:13	

Transcript of Daniel Foty, Ph.D.
Conducted on January 9, 2026

125

73:21, 74:4 nonchip 49:7 none 4:23, 4:26, 4:28 normal 103:13 notary 1:28, 104:1, 104:4, 105:11, 105:14, 106:21 note 39:17, 40:2, 62:4, 73:2, 90:3 noted 56:16 notes 7:16, 102:12 noth 68:8 nothing 6:3, 15:5, 17:13, 57:22, 58:1, 59:22, 68:8 notice 1:13 november 13:11 number 11:22, 12:14, 12:20, 18:5, 27:16, 27:20, 27:22, 28:6, 28:8, 28:9, 28:14, 29:3, 29:7, 46:11, 49:11, 49:13, 51:6, 51:8, 51:9, 62:12, 62:13, 62:14, 77:18, 80:15, 81:22 numbered 46:7 numbering 75:22, 76:5	numbers 62:6, 62:7 numerous 30:3, 30:5 O oath 3:7, 7:5, 106:12 object 9:10, 9:20, 15:19, 15:22, 41:3, 42:8, 44:12, 45:17, 46:21, 49:15, 50:4, 50:13, 50:17, 54:1, 55:2, 58:5, 61:15, 65:3, 66:1, 66:19, 69:4, 69:14, 72:4, 73:13, 74:9, 99:13, 100:5 objection 15:21, 46:3 obstruction 69:20 obvious 21:22 obviously 17:7, 27:10, 32:4, 46:15, 60:13, 98:16 occurred 104:15 occurs 27:7 off-chip 53:7, 64:2, 84:19, 84:21 off-the-record 5:10 offense 34:8 offer 106:11 offered 15:17, 16:14	office 1:1, 6:22 often 30:7, 90:19 oh 7:3, 10:8, 16:1, 18:3, 25:2, 32:16, 39:16, 43:11, 46:8, 51:5, 69:5, 69:9, 74:19, 76:2, 84:12, 86:22, 89:20, 101:20, 102:6 ohm's 75:11 ohmic 71:2, 71:6, 71:16, 74:11, 74:14, 74:15, 74:16, 74:18, 75:1, 75:6, 75:10, 75:13 on-chip 53:4, 53:7, 53:9, 54:3, 54:17, 59:4, 61:8, 68:18, 83:13, 83:14, 83:16 once 12:21, 79:5, 79:9 one 5:7, 6:19, 10:13, 11:12, 11:19, 22:6, 22:12, 23:17, 25:9, 25:10, 31:20, 36:21, 37:5, 38:21, 38:22, 39:4, 48:19, 49:8, 49:19, 51:8, 51:9, 53:18, 53:19, 54:16, 54:17, 54:18,	54:21, 55:5, 55:7, 55:9, 57:16, 62:4, 64:16, 66:9, 68:2, 69:15, 73:4, 77:4, 82:17, 87:12, 88:17, 90:8, 92:19, 94:5, 94:7, 95:11, 95:15, 96:3, 101:6 one's 61:10 one-dimensional 73:17 ones 29:20, 36:15 online 96:10 only 10:17, 12:22, 29:19, 33:14, 34:3, 34:11, 48:19, 83:7, 99:14 open 9:7, 74:6, 74:8, 74:10, 74:16 opening 13:19, 13:21, 14:1, 24:13 operation 19:21 opinion 16:11, 33:14, 72:10 opinions 15:15, 15:17, 16:14, 16:17, 16:20, 17:12, 18:17 option 48:5, 48:13, 82:17 order 19:12, 71:1,
---	--	--	---

Transcript of Daniel Foty, Ph.D.
Conducted on January 9, 2026

126

73:8 ordinary 29:9, 32:12, 32:19, 48:20, 50:1, 50:10 original 13:17, 13:19, 16:15, 96:15 orrick 2:3 oscar 6:16, 74:16 other 8:18, 9:14, 10:15, 12:19, 12:20, 15:2, 18:10, 20:6, 23:5, 23:19, 28:5, 29:17, 32:9, 47:5, 47:8, 63:18, 67:18, 68:18, 69:19, 70:2, 70:3, 75:12, 79:20, 79:21, 83:4, 84:3, 88:11, 91:22, 93:6, 96:17, 99:12, 100:18, 101:2 otherwise 34:15, 104:22 out 15:2, 20:21, 22:3, 31:18, 34:13, 34:16, 39:14, 42:16, 43:16, 55:7, 56:10, 68:7, 69:6, 72:8, 73:21, 74:4, 80:11, 81:3, 89:1, 96:2, 99:17 outcome 104:22 outfit 19:18	output 37:1 outside 33:4, 55:9, 78:1, 79:12 over 5:7, 10:8, 10:9, 56:18, 56:22, 57:4, 62:21, 63:11, 64:16, 65:1, 65:21, 67:18, 68:13, 97:17 overcome 64:8 overlap 63:7, 63:10, 63:22, 66:17 own 11:5, 18:19, 27:5, 97:11 owner 1:8, 1:14, 2:17 owner's 18:8 P p+ 70:19, 70:20, 71:10, 71:16, 72:10, 75:4, 75:15 p-type 71:15 pack 22:2 package 14:14, 20:21, 21:2, 21:4, 21:9, 21:15, 21:19, 22:3, 22:18, 23:1, 28:9, 29:8, 59:9, 66:11, 69:7, 70:7, 77:20, 77:22, 78:2, 79:2, 84:14, 84:17,	84:21, 95:21, 95:22, 96:2, 96:3, 97:4, 97:8, 97:20 packaged 21:5, 78:2, 99:21 packages 78:9 packaging 21:12, 79:20, 97:7 pad 21:12, 26:19, 26:20, 26:21, 30:10, 30:14, 31:8, 32:13, 32:14, 32:20, 32:21, 33:3, 36:12, 36:21, 36:22, 37:1, 37:5, 37:6, 37:9, 37:10, 39:3, 53:5, 53:19, 55:7, 55:9, 63:19, 64:19, 66:6, 66:7, 66:11, 68:3, 68:5, 69:16, 69:18, 69:19, 82:15, 83:3, 92:10, 97:3, 99:17, 99:18, 100:9, 100:13, 100:14 pad-limited 28:12, 33:18, 33:22, 34:4, 35:3, 35:7, 49:21, 52:5, 52:21, 53:10, 53:11, 54:15 pad-to-pad 96:20 pads 19:15, 20:18, 21:20, 22:5, 22:8, 22:21,	22:22, 23:2, 23:5, 23:9, 23:12, 23:14, 23:18, 24:5, 26:19, 27:8, 27:11, 27:13, 27:16, 27:20, 27:22, 28:4, 28:5, 28:6, 28:8, 28:10, 28:14, 29:3, 29:10, 29:16, 29:19, 29:20, 30:2, 30:3, 30:13, 30:21, 31:1, 31:4, 31:11, 31:13, 31:20, 31:21, 32:3, 32:4, 32:7, 32:10, 33:2, 34:3, 34:5, 34:13, 34:15, 35:5, 38:12, 38:18, 53:20, 56:19, 64:16, 69:7, 70:2, 76:16, 77:19, 78:5, 85:19, 90:22, 92:6, 96:2, 96:17, 97:1, 97:5, 97:7, 97:12, 97:20, 99:12, 99:18, 100:3, 100:6, 100:17, 101:1, 101:4 page 3:2, 3:13, 3:15, 25:14, 25:15, 25:16, 25:21, 53:13, 56:5, 62:7, 62:13, 62:14, 62:16, 62:17, 63:1, 63:4, 67:16, 70:10, 70:11, 70:14,
--	--	--	--

Transcript of Daniel Foty, Ph.D.
Conducted on January 9, 2026

127

72:13, 72:15, 73:7, 75:22, 76:1, 76:4, 76:9, 77:16, 77:17, 90:2, 95:11, 95:13, 107:1, 107:2, 107:5, 107:8, 107:11, 107:14, 107:17, 108:1, 108:2, 108:5, 108:8, 108:11, 108:14, 108:17 pages 1:34, 25:20, 48:7, 48:8, 55:18, 55:20, 55:22, 62:9, 74:2, 95:15 paired 46:16 pap 35:10 paper 10:2, 11:19, 13:14, 25:3, 25:20, 35:10, 37:21, 38:6, 38:10, 41:15, 45:12, 62:3, 80:22, 81:4, 92:15, 95:10 para 72:12 paragraph 17:19, 17:21, 18:3, 18:6, 18:16, 18:22, 19:4, 20:17, 21:11, 21:18, 22:4, 22:13, 22:14, 22:20, 23:4, 23:11, 23:18, 24:1, 24:18, 25:6, 25:18, 26:8, 26:9, 30:4, 33:11, 33:16,	36:17, 40:4, 42:10, 44:14, 48:1, 55:15, 56:3, 58:12, 63:1, 63:5, 70:14, 80:8, 81:21, 81:22, 82:7, 84:15, 85:4, 85:8, 85:11, 85:16, 92:2, 95:1, 95:11, 95:14, 95:16, 96:21, 97:6, 97:13, 99:11, 100:3, 100:16 paragraphs 55:21 parallel 82:10, 85:12 pardon 60:4 park 2:5 parlance 72:6 part 15:18, 16:4, 19:21, 59:5, 96:5, 96:13, 97:18 partes 3:27 partial 25:9 particular 19:13, 20:2, 21:21, 22:17, 23:15, 24:11, 33:2, 36:13, 40:21, 54:11, 54:14, 55:3, 55:4, 55:11, 62:9, 66:14, 69:22, 73:5, 76:12, 76:14, 82:11, 83:2, 97:18, 98:2,	98:3, 99:15, 100:19, 101:2, 101:5 particularly 49:20, 52:4, 67:4, 70:5 parties 2:25, 104:19, 104:20 parts 35:14, 85:9 party 104:11 pass 40:7, 102:9 passes 80:4 passing 102:8 past 10:8, 52:4 pasted 95:20 patent 1:1, 1:2, 1:3, 1:8, 1:14, 2:17, 3:20, 3:28, 3:35, 4:5, 4:9, 12:13, 12:17, 12:18, 13:3, 16:13, 16:18, 16:21, 18:8, 33:14, 34:19, 35:8, 36:1, 36:11, 37:5, 41:8, 86:9, 86:11, 86:17, 89:7, 89:13 patent's 33:18 path 38:22, 39:4, 39:5, 71:19, 82:10, 84:1, 85:12 patrick 6:15 pause 25:1, 101:16	paused 28:22 pay 68:21 paying 80:5 pc 59:10, 59:14, 61:4, 78:3 penalty 7:5, 106:4, 106:5 people 57:3, 60:13 percent 57:5, 57:7 perfect 12:10, 91:1 performed 19:16, 19:18 peripheral 46:17 periphery 22:7, 22:8, 22:11, 27:8, 27:21, 29:19, 34:14, 82:21, 97:13 perjury 7:5, 106:4, 106:5 permitted 10:9 person 10:17, 29:9, 32:12, 32:19, 48:20, 50:1, 50:10 personally 86:17, 89:12 perused 18:1, 19:1, 20:11, 22:16, 24:22, 32:15, 33:13, 36:2, 38:3, 41:4, 41:13, 44:13, 47:21, 48:6,
--	---	--	---

52:12, 53:16, 63:8, 70:12, 77:9, 82:6, 82:16, 84:20, 85:15, 86:1, 86:20, 89:18, 91:10, 91:16 peter 81:12 petition 3:26 petitioner 1:5, 2:8 petitioner's 18:10 ph 1:11, 3:2, 104:6, 104:15, 106:16, 107:21, 108:22 phase 59:16 phone 5:15 photo 20:3, 20:6, 20:8, 20:9, 20:15, 22:17, 23:13, 23:18, 24:13 photograph 19:3, 19:5, 19:6, 20:17, 21:11, 21:18, 21:21, 22:4, 22:13, 23:4, 24:1, 24:11 phrase 73:5 physical 6:20, 11:11, 20:14 physically 95:21 physics 59:1 picks 73:19	picture 96:7 piece 21:16 pieces 77:22, 78:1 pin 66:11, 96:3, 97:11 pins 21:1, 21:4, 21:5, 21:10, 21:16, 28:9, 29:8, 70:7, 78:1 pipe 30:15, 30:19, 31:17, 31:18 place 26:15, 29:13, 79:12, 90:5 placed 29:13, 95:20 places 30:3, 30:5, 75:18 plan 55:5, 55:8 planet 1:30, 2:20, 106:2 plast 79:6 plastic 78:9, 78:10, 78:12, 78:19, 78:20, 79:6, 79:14 please 5:6, 5:7, 5:11, 5:12, 5:15, 5:22, 6:13, 6:17, 32:17, 45:11, 52:15, 70:18, 92:19 plug 78:2 plugged 21:6	plus 71:12 pock 71:12 pocket 70:20, 71:10, 71:12, 72:10, 75:4, 75:15 point 15:3, 15:8, 23:7, 31:7, 39:14, 44:7, 56:10, 64:12, 80:1 points 57:7 poking 8:7 poor 63:14, 64:7, 66:10, 66:15 poorly 67:12 por 8:17, 16:4, 17:9, 60:11 portions 82:14, 82:18, 85:13 possibility 23:20 possible 23:9, 27:19, 60:19, 63:11, 64:19, 66:21, 67:3, 68:9, 68:16, 97:21 post 6:22 post-it 7:16 poured 79:6, 79:15 power 28:4, 30:2, 30:10, 30:14, 30:17, 31:1, 31:8, 31:13,	31:20, 32:3, 32:10, 32:14, 33:3, 49:3, 51:16, 53:8, 94:3, 99:17, 100:9 practical 34:11, 59:2 practice 20:20, 21:3, 29:15, 34:11, 64:1, 64:8, 64:22, 65:20, 66:10, 66:12, 66:15, 67:10, 68:10, 68:12, 70:22, 71:8, 71:20, 71:21 practices 63:14, 63:15, 68:19, 97:19 preemptively 15:4 prefers 11:12 prepare 10:6 prepared 12:11, 13:2, 20:15 preparing 15:9, 17:7, 18:19 present 2:19 presented 57:13, 58:1, 60:11 pressure 53:11 presumably 83:18 presume 82:20 pretty 19:20 previous 50:18, 50:22,
---	--	--	--

51:5, 67:16 previously 4:22, 51:3 principal 20:7 prior 8:4, 18:6, 27:5, 50:15, 81:18, 86:10, 89:9, 89:13 privileged 17:8 probably 34:8, 71:15, 75:5 problem 54:7, 57:14, 58:7, 58:10, 59:22, 60:10, 60:12, 61:8 problems 57:21, 61:11, 68:21 proceed 6:6, 40:15, 70:18 proceeding 5:4, 5:8, 12:4, 13:11, 16:7, 16:10 proceedings 25:1 process 17:6 produce 26:18, 75:5 product 21:5, 24:15, 28:6, 29:6, 29:7, 33:1, 33:6, 78:3, 79:22, 80:5 production 62:6, 62:7 professional 3:30 profile 75:2	propagate 40:9, 49:8 protect 79:15 protecting 79:11 protection 40:12, 47:13, 73:8, 78:9, 79:3, 79:18, 79:19 protective 44:16, 45:2, 45:5 protects 79:9 provide 5:17, 7:7, 19:3, 20:4, 46:22, 47:13, 49:3, 73:8, 85:12 provided 4:27, 9:8, 11:22, 24:12 provides 40:13 providing 1:29, 20:7 provision 94:3 pst 1:17, 104:17 public 1:28, 104:1, 104:4, 105:11, 105:14, 106:21 publication 4:10 pull 11:2, 11:5, 13:5, 14:8, 35:8, 37:14, 38:5, 47:17, 61:21, 75:19, 76:2, 80:12, 80:13, 86:2 pulled 73:21	purchase 5:18 purpose 30:9, 39:11, 39:22, 40:6, 42:15, 76:17, 78:7, 100:12, 101:6, 101:12 purposes 5:9, 12:16, 13:17, 31:3 pursuant 1:13 put 11:20, 19:8, 27:11, 29:17, 29:18, 35:12, 37:11, 43:5, 43:6, 71:1, 71:4, 71:5, 75:3, 75:4, 77:11, 80:14, 83:4, 85:21, 88:17, 95:3, 101:21 pvc 31:17 Q qualifies 16:12 question 9:13, 16:3, 23:6, 29:1, 30:11, 32:17, 33:17, 38:13, 39:21, 42:2, 44:1, 46:5, 50:5, 50:9, 50:15, 50:18, 51:1, 51:2, 51:5, 51:12, 52:15, 56:9, 57:12, 58:2, 59:2, 65:9, 65:13, 73:1, 78:17, 82:8, 92:14, 92:18	questions 4:25, 76:7, 77:15, 82:5, 85:10, 101:18, 102:5, 102:17, 103:5 quick 17:4, 36:8, 70:10 quickly 64:19 quiet 72:2, 73:9, 74:4 quite 30:7, 33:8, 72:16 R radiofrequency 87:4, 87:13, 87:17 rails 85:19 raise 5:21 rare 95:10 rather 8:7, 51:19, 53:7, 67:12, 71:17, 76:7, 77:13 raw 100:19 rd 14:13 rdr 1:26, 104:3, 105:8 re-ask 44:1, 78:16 reach 15:14 reached 17:11 reaching 93:18
---	---	---	--

read 25:10, 26:10, 26:17, 36:7, 36:8, 36:10, 36:22, 37:7, 48:4, 48:12, 56:3, 56:11, 58:13, 63:6, 63:9, 72:18, 82:4, 82:6, 85:8, 87:1, 87:3, 88:7, 93:4, 106:6, 106:7 reading 2:26, 93:3 real 24:14, 33:10, 43:7, 61:7, 69:18, 70:10, 80:5 reality 49:11, 52:2 realize 43:11 really 33:20, 34:11, 59:21, 64:1 reason 7:7, 12:7, 20:7, 34:1, 34:15, 35:6, 75:12, 107:4, 107:7, 107:10, 107:13, 107:16, 107:19, 108:4, 108:7, 108:10, 108:13, 108:16, 108:19 recall 61:2 receive 103:11 recess 43:4, 94:16, 103:2 recognize 86:14, 86:16,	89:5 recollection 52:16 recommending 63:13 reconstruct 43:18 record 6:14, 6:18, 7:21, 27:4, 42:21, 43:8, 43:9, 43:12, 65:9, 65:16, 70:14, 74:21, 94:11, 103:4, 103:8, 104:10 recording 5:8, 5:17 red 10:20, 96:22, 98:5 ref 83:19 refer 9:17, 11:11, 12:4, 12:17, 13:16, 13:20, 14:15, 28:8, 30:2, 30:4, 36:15, 38:1, 39:20, 40:16, 48:3, 56:3, 58:13, 72:6, 75:18, 81:7, 89:6, 92:2 reference 3:19, 4:3, 4:22, 12:20, 26:22, 28:5, 36:19, 40:3, 56:11, 56:13, 57:7, 57:15, 57:17, 58:20, 61:9, 61:22, 64:12, 76:22, 80:10, 81:7, 81:17, 81:18, 83:22, 84:9,	85:5, 88:5, 89:6, 90:7 references 8:12 referred 40:1, 50:19, 72:19, 74:6, 78:20, 79:1 referring 8:10, 12:5, 12:18, 14:2, 26:1, 26:7, 26:14, 35:13, 36:13, 39:11, 39:19, 40:17, 52:6, 62:6, 77:8, 78:11, 78:13, 82:20, 83:12, 84:1, 85:17, 89:20, 90:18 refers 36:17, 44:14, 44:15, 78:18, 83:18, 84:15, 87:13, 88:5, 88:7, 90:12, 91:6, 91:17, 93:4 reflections 59:16 refresh 52:15 regarding 16:14, 16:17, 16:20, 93:3 related 5:19, 104:18 relates 12:13 relation 12:12, 13:3 relied 18:19 relieve 53:11 rely 18:15	relying 41:1, 41:6 remarkably 33:8 remember 5:6, 5:11, 43:16, 60:20 remotely 5:4, 104:15 remove 27:13, 29:10, 29:16 removed 19:9, 29:12 removing 26:19 render 16:11 repeat 28:21, 50:8, 65:13, 92:17 repeated 52:15 rephrase 84:18 replacing 63:14 reply 4:13, 11:21, 13:20, 14:16, 14:21, 15:7, 15:9, 15:16, 16:15, 16:22, 17:3, 17:7, 17:12, 18:10, 18:11, 19:4, 24:19, 33:12, 47:18, 55:16, 80:8, 81:8, 95:2 reported 1:25, 61:10 reporter 3:9, 5:13, 5:21, 6:5, 42:16, 43:10, 92:17, 92:19, 92:21, 103:3, 103:9, 103:14,
--	--	---	--

104:1 represented 104:13 requires 27:16 reread 82:7, 85:9 reserved 2:27 residence 1:19 resistance 58:14, 58:22, 59:5, 59:13, 59:20, 61:5, 61:7, 71:10, 75:14, 75:15, 84:1 resistive 71:19 resistivity 75:8 resistor 39:1, 39:3 respective 2:25 respond 28:18, 44:20, 57:22 responded 16:3 responding 15:17 response 18:8, 51:13 rest 22:1 result 29:14, 30:1, 66:4 revealing 17:8 reverse-engineer- ing 19:12 review 3:27, 17:4, 56:20, 57:1,	102:18 reviewed 10:8, 15:11, 17:2, 17:9 rfid 88:8, 88:9, 88:10, 88:12 right 5:22, 7:2, 7:3, 11:7, 13:6, 14:7, 18:21, 26:3, 35:21, 37:11, 43:5, 43:14, 45:9, 46:9, 62:13, 64:15, 64:16, 66:6, 68:4, 68:22, 72:14, 75:17, 75:22, 78:16, 80:7, 85:21, 88:2, 88:17, 90:10, 94:4, 101:16, 102:8 right-hand 62:17 ring 54:3, 97:9, 97:10 rings 72:19 risk 49:6, 49:9, 53:3, 67:7, 67:10, 67:20, 67:22 road 1:20, 2:4, 6:20 rockville 1:32 roll 55:17 room 9:3 rough 103:14 route 38:21, 64:15,	64:18 router 43:18, 43:21 row 66:6 rule 64:4 rummage 7:19 rummaging 32:16 run 5:5, 22:18, 46:16 running 19:14, 64:2, 67:17, 84:2, 96:1 S s 2:1, 14:10 sag 67:7 said 22:11, 33:16, 34:22, 36:5, 40:22, 51:12, 51:13, 57:15, 65:2, 65:4, 74:11, 75:2, 75:3, 77:13, 77:21, 82:2, 84:5, 85:6, 97:19, 100:7, 101:13 saint 3:33, 7:18, 27:3, 27:14, 33:8, 33:21, 34:17, 49:18, 50:19, 52:1, 52:8, 52:13, 52:17, 52:19, 53:21, 54:9, 61:22, 62:16, 63:13, 67:9, 68:10, 68:19,	70:9, 70:16, 70:19, 76:1, 76:9, 76:10, 76:12, 76:15, 77:17, 97:19 saint's 52:1, 52:6 same 6:19, 12:20, 18:14, 21:15, 22:7, 25:18, 26:15, 29:14, 29:22, 30:21, 31:9, 31:16, 32:8, 34:22, 35:13, 41:21, 42:7, 42:9, 44:11, 44:17, 44:19, 46:3, 51:12, 51:15, 58:12, 87:18, 90:2, 106:7, 106:8 san 2:14 save 106:8 saw 16:1, 81:17 say 8:9, 12:21, 14:5, 14:19, 18:13, 26:17, 28:14, 29:3, 31:7, 39:4, 48:12, 49:7, 52:8, 52:17, 67:7, 68:15, 74:10, 78:2, 79:16, 96:21, 101:18 saying 27:6, 37:9, 64:21, 65:20, 66:6, 66:7, 66:13, 67:9, 77:7 says 37:7, 42:10,
---	--	---	--

47:1, 53:16, 53:17, 54:4, 56:11, 61:9, 63:4, 63:5, 63:9, 66:2, 72:2, 72:17, 82:16, 83:9, 85:16, 90:17, 91:15, 93:22 scale 24:3, 100:21, 101:7 screen 8:8, 11:4, 11:7, 11:20, 25:19, 26:10, 35:12, 36:9, 36:10, 38:9, 45:11, 55:19, 80:14, 95:4 screw 56:1 screwy 41:7 second 38:2, 68:3, 68:4, 82:4 seconds 101:14 section 27:1, 63:5 see 7:10, 7:13, 9:15, 18:12, 19:14, 20:10, 20:11, 23:8, 24:4, 24:5, 25:7, 25:13, 26:9, 28:9, 28:10, 28:13, 29:18, 36:9, 37:2, 37:3, 38:3, 42:22, 46:10, 46:12, 48:17, 48:18, 56:5, 56:6, 58:16, 58:17, 63:12, 63:13,	64:12, 64:14, 65:19, 66:5, 66:7, 66:8, 66:9, 68:1, 69:16, 72:20, 72:21, 81:11, 81:13, 81:14, 87:6, 87:7, 87:15, 87:16, 92:2, 98:4, 101:10 seeing 36:15 seem 36:14, 55:17 seems 14:5, 35:6, 44:7, 63:18, 83:12, 85:17, 85:20, 87:11 seen 25:9, 60:10, 81:18, 86:10 segment 54:16 segments 46:16 self-inductance 59:1 sell 29:7, 80:5 semiconductor 73:3, 88:8 sense 33:19, 34:7, 51:10, 64:15, 64:18, 90:16, 91:1 sentence 25:6, 25:8, 25:9, 25:13, 26:8, 26:14, 48:3 separate 53:9, 53:14, 73:22, 77:2 serious 19:20	serve 31:3, 31:10, 31:14, 31:15, 33:3, 42:11 services 1:29 sessions 10:10 set 104:7, 105:2 several 8:4, 97:9, 101:7 sewer 30:19, 31:18 share 57:5, 57:8 sheet 3:11, 106:1, 106:10 shirt-circuits 69:2 shockley 75:6 short 59:21, 63:11, 64:20, 66:21, 67:2, 67:19, 68:5, 68:7, 68:9, 68:16, 69:11, 70:3 shorthand 104:1 should 5:10, 14:17, 21:7, 44:3 show 21:21, 23:11, 23:13, 23:15, 45:15, 46:1, 46:13, 46:15, 46:19, 76:13, 76:18, 76:20, 78:5, 78:7, 78:8, 91:20, 96:18, 99:20, 100:13, 100:16, 100:17, 100:19,	100:21, 101:8 showing 27:11, 38:14, 70:4, 73:14, 73:15, 73:16, 73:20, 74:2, 74:3, 85:20 shown 19:16, 23:11, 24:2, 38:18, 55:4, 76:11, 76:16, 95:17, 97:17, 100:22 shows 21:19, 22:2, 33:21, 34:17, 38:15, 47:11, 53:13, 54:2, 55:6, 63:21, 64:1, 64:10, 67:15, 67:17, 67:21, 73:7, 73:11, 73:16, 77:21, 92:8 showstoppers 61:11 shunt 74:3 sic 35:22, 41:6, 44:1, 48:9, 54:2, 64:21, 69:2, 73:15, 74:6, 76:18, 77:3, 84:4, 97:13 side 37:12, 55:7, 64:17, 85:22, 87:12 signal 10:20, 10:22, 28:4, 49:9, 90:22, 92:6, 93:11, 93:18 signals 47:14, 73:12 signature-plkal 105:6
---	--	--	---

signature: __date- : __ 107:20, 108:21 signed 106:13 signing 2:26 silent 47:10 silicon 19:6, 19:7, 63:7, 63:11, 63:16, 63:19, 63:22, 65:1, 65:22, 66:18, 70:21, 71:3, 71:5, 71:9, 71:14, 71:15, 71:17, 71:19, 71:22, 72:7, 75:5, 83:21, 95:19, 100:11 similar 21:6, 72:1 simple 71:18 simpler 38:17, 73:15 simply 23:7, 26:19, 27:14, 29:13, 57:3, 58:2, 64:8, 75:10 simulation 49:5 since 7:17, 16:22, 35:2, 43:7, 55:19, 62:4, 96:13 single 53:5, 87:4, 87:8 sink 30:18, 30:19, 73:19 sinking 32:6	sinusoidal 51:19 sit 71:14 sitting 61:12, 71:13, 71:14, 72:11 situation 33:2, 34:12, 35:7, 49:21, 53:10, 53:11, 54:14, 55:11, 55:12, 61:5, 70:1 size 59:6 skill 29:9, 32:12, 32:19, 48:20, 50:1, 50:10 slide 62:21 slowly 5:6 small 23:22, 27:19, 54:19, 59:6 smaller 53:5, 56:19 smith 59:17 smoothly 5:5 solemnly 6:1 solve 68:21 solved 58:7 some 7:15, 12:7, 24:6, 27:16, 28:4, 28:5, 29:7, 29:19, 36:13, 39:19, 43:18, 56:21, 58:22, 59:1, 59:2, 67:5,	67:18, 82:5, 84:21, 88:11, 98:15 somehow 95:20 someone 66:17 something 9:22, 10:4, 14:4, 14:6, 14:13, 14:18, 14:19, 30:6, 32:22, 33:16, 50:22, 67:7, 95:20 sometimes 29:15 somewhere 23:10, 52:10, 56:21, 75:21, 78:14 sorry 15:21, 18:3, 25:2, 25:19, 36:4, 36:5, 39:20, 42:17, 43:11, 46:11, 50:14, 50:16, 59:9, 59:12, 80:16, 82:3, 92:14, 93:12, 95:14, 98:12, 98:13, 98:17, 99:3, 101:20, 102:3 sort 56:20, 83:22, 84:22 sorts 51:15 sounds 90:6, 94:15, 102:22 sourcing 32:5 space 27:8, 27:17, 33:21, 34:2,	34:3, 34:5, 34:13, 34:14, 34:16, 35:4, 39:19 spacing 99:22, 100:13, 100:14 spans 48:6, 55:18 sparkfun 19:20 speak 5:6, 69:20 speaking 5:13, 5:16, 52:2 specific 21:14, 47:10, 48:5, 48:13, 55:12 specifically 52:19, 85:16 spelled 6:15 split 95:15 spot 26:3, 83:3 square 51:20 squares 32:8 stand 13:6, 35:17 standard 71:20, 71:21, 103:13 stanley 81:11 start 27:12, 29:16 started 43:10 starting 86:22 starts 48:4, 52:22, 53:14
---	--	--	---

state 6:13, 6:17, 105:11, 105:14, 106:21 stated 101:7 statement 16:16 states 1:1, 1:28, 3:20, 3:35, 4:5, 4:9, 37:5, 104:4 stenographically 1:25 stepped 16:2 stick 12:7 still 31:12, 47:14, 58:8, 98:11, 106:12 stimuli 44:20, 45:8 stipulated 2:24 stove 101:15, 101:22 straddle 25:19, 25:20 straight 68:7, 75:11, 75:12 strange 8:22, 14:5 strangely 19:19 strike 12:12, 23:3, 42:1, 42:4, 54:20, 69:10, 72:11, 83:15, 84:18, 93:9, 93:12 string 44:4 structure 39:1, 39:18,	39:21, 40:8, 40:13, 47:13, 83:4 structures 71:22, 83:13, 83:14, 83:16, 84:3 struggle 81:3, 86:5, 88:22 study 32:18, 49:19, 50:20, 52:1, 52:7, 52:8, 52:17, 52:20, 53:21, 54:9, 54:11, 60:18 stuff 59:17 sub 14:13 sub-subsection 27:2 subject 16:12 submitted 13:11, 14:10 submitting 16:22 subscribed 106:19 subsection 27:1 substantive 15:5 substrate 72:3, 72:6, 87:5, 87:9, 87:12, 90:11, 90:12, 91:7, 92:7 successfully 60:14 suite 1:31 summary 8:2, 87:11, 88:6	supplies 51:16 supply 32:14, 32:21, 49:3 support 3:26 supposed 28:3 sure 6:15, 8:1, 11:10, 29:1, 30:6, 35:13, 38:13, 41:11, 45:18, 46:6, 56:16, 62:11, 63:3, 70:2, 71:1, 77:12, 84:8, 89:21, 90:1, 94:13, 98:15, 99:4, 102:1 surprised 92:1 surrounds 20:9 sutcliffe 2:3 swear 6:1 switching 40:9, 49:6 sworn 104:7, 106:19 symbol 40:21 system 37:8	41:5, 64:13, 94:4, 94:5, 94:9, 96:7, 102:11, 103:13 taken 1:13, 43:4, 94:16, 96:11, 96:12, 103:2, 104:9, 106:6 taking 43:3 talk 5:7, 30:12 talking 30:13, 59:10, 61:4 talks 59:8, 83:10 tango 6:16 teaches 68:19 teaching 68:10, 76:12 teachings 33:18 team 53:2 teardown 19:8, 19:12, 19:14, 19:16, 19:18, 20:2, 22:2 tech 106:3 technical 5:19, 98:15 technically 14:12 techniques 3:32 technological 57:9, 58:3 technologies 1:7, 2:18, 3:23, 4:16 technology 1:4, 2:9, 4:15,
T			
		tackle 54:6 tag 87:4, 87:14, 87:17, 88:8, 88:9, 88:10, 88:12 take 38:20, 38:22,	

56:4, 56:7, 57:2, 57:11, 58:4, 104:12 telephone 1:33 tell 23:21, 31:7, 91:18 template 26:20, 27:12, 29:12, 29:16 ten 94:12, 101:14 ten-minute 94:15 tends 51:18 term 14:1, 22:6, 22:11, 35:2, 73:2, 79:1, 90:19 termination 59:16 terminology 19:7 terms 18:18, 30:21, 31:3, 36:19, 45:6, 46:5, 59:8, 61:10 test 80:4 testimony 6:2, 7:4, 7:8, 17:10, 74:20, 94:20, 104:10 text 67:17, 78:14, 91:15, 93:3 th 105:3 thank 5:3, 5:20, 6:5, 6:11, 11:1, 12:10, 26:16, 48:10, 51:11, 102:6, 103:1,	103:6, 103:7 thanks 41:10 themselves 30:21, 32:7 theory 60:8, 60:20, 61:17 thereto 18:9 they'd 49:17 thing 18:14, 22:7, 34:22, 44:17, 62:4, 87:18, 99:9 things 8:7, 8:12, 8:13, 20:6, 23:8, 33:9, 56:19, 70:3, 73:3, 75:9, 79:9, 79:11, 79:12, 88:11, 90:2, 101:7 think 9:21, 10:16, 11:10, 12:8, 14:17, 15:3, 15:13, 16:9, 21:14, 22:7, 22:11, 32:18, 34:21, 34:22, 57:13, 68:1, 68:15, 76:21, 78:10, 101:18, 102:5, 103:16 thomas 2:11, 2:16 thought 36:5, 40:22, 50:14, 50:18, 51:2, 51:11, 56:1, 57:3, 82:2 thread 44:4 three 46:5, 46:7,	46:16, 53:20, 57:7 three-day 103:9 through 7:19, 17:6, 19:8, 35:22, 36:4, 36:5, 39:1, 39:2, 39:6, 39:8, 39:9, 39:10, 40:7, 40:10, 41:21, 41:22, 60:21, 61:20, 62:5, 73:22, 83:7, 83:8, 84:2, 89:17, 91:9, 92:4, 93:13, 99:17, 100:7 time 1:18, 5:16, 10:9, 17:2, 38:5, 98:20 times 29:17, 101:7 tjensen@orrick 2:7 to: 107:2, 107:5, 107:8, 107:11, 107:14, 107:17, 108:2, 108:5, 108:8, 108:11, 108:14, 108:17 today 7:4, 7:8, 7:11, 10:7, 15:4, 61:12, 67:5, 95:10 together 23:10, 23:12, 28:3, 29:18, 53:3, 53:18, 55:7, 78:5, 94:2, 97:1, 97:5, 102:12 took 96:15, 98:20	top 45:15, 46:1, 47:5, 56:5, 60:7, 61:1, 62:12, 62:16, 66:6, 68:4, 70:11, 72:14, 75:22, 78:10, 78:12, 78:19, 78:20, 83:20 topic 47:11, 63:18 topological 38:14 tore 19:21, 81:3 totally 63:3 toward 26:9 trace 66:11, 84:14, 84:17, 84:19, 84:21, 92:9, 97:4, 99:21, 100:14 traces 20:22, 21:1, 21:9, 21:15, 21:19, 22:3, 22:18, 23:1, 24:4, 58:15, 59:5, 59:9, 59:11, 61:4, 69:7, 77:20, 77:22, 84:2, 84:15, 93:11, 93:18, 93:20, 96:1, 96:2, 96:3, 97:8, 97:20 track 92:15 trade-off 58:14, 58:18, 59:19, 61:7 trade-offs 49:19, 58:19
--	---	---	--

trademark 1:1 transcript 2:27, 5:18, 106:6 transistor 71:22, 83:21 transistors 84:3 translation 37:20 travis 2:2, 50:16, 98:11, 99:8, 101:19, 102:5, 102:12 trial 1:2 true 104:9, 106:8 truth 6:3 truthful 7:8 try 62:11, 90:6 trying 27:18, 50:21, 52:11, 77:11, 97:2 turn 24:18, 25:21, 41:12, 45:9, 80:7, 81:21, 84:10, 86:19, 89:16, 95:1, 101:22 two 10:10, 10:13, 12:12, 13:2, 23:9, 23:14, 31:19, 48:7, 49:10, 53:1, 55:18, 55:22, 73:12, 93:20, 97:1, 97:4 type 49:17, 70:21,	83:3, 87:19 types 79:20 typically 52:4 typo 74:21, 74:22 typos 15:1 U uh-huh 10:14, 26:6, 38:16, 47:20, 72:17, 92:16, 92:20 unable 5:14 unaware 81:16 unconventional 17:14 under 7:5, 22:19, 106:4, 106:5, 106:12 undergraduate 59:18 underneath 68:9, 69:3, 69:13, 98:3 understand 7:4, 12:5, 12:6, 12:17, 14:2, 38:13 understanding 106:11 unified 53:9 unifies 54:3 united 1:1, 3:20, 3:35, 4:5, 4:9 unless 14:4, 35:5, 102:5 unlike 101:2	unnecessary 26:19, 26:21, 29:10 unreasonable 44:18 unstable 42:13 until 16:10, 81:16 unused 63:11, 63:16 upper 64:15 usage 73:5 use 7:16, 9:15, 14:1, 19:7, 22:6, 34:1, 35:6, 37:22, 39:15, 48:21, 49:14, 50:3, 50:11, 51:7, 54:9, 54:12, 60:13 useful 59:20 useless 27:11 uses 40:21, 97:19 using 23:14, 23:19, 33:17, 54:22, 78:5, 93:6, 94:1, 100:17 usual 21:3 V validity 16:17, 16:21 various 8:12, 17:10, 19:9, 51:13, 56:17, 85:13 vary 75:8	vermont 1:21, 6:21, 6:22 version 62:17, 64:10, 73:16, 73:17, 76:14 versus 61:6, 61:7, 96:19, 97:4 via 1:23, 2:2, 2:11, 2:21, 5:15, 84:2, 104:15 video 5:12, 5:14, 98:10, 98:20 videoconference 2:2, 2:11, 2:21 videoconferencing 1:22, 104:16 videographer 48:9 view 23:7 viewing 23:21 visible 23:10 visibly 97:8 visual 20:4 voltage 37:8, 75:8 voltages 49:3, 54:18 vs 1:6, 4:15, 106:3 W wafer 72:8 want 11:8, 25:5, 29:1, 30:4,
---	--	---	--

33:2, 35:21, 39:13, 39:17, 40:2, 48:3, 56:10, 62:4, 66:17, 66:20, 67:2, 68:15, 69:22, 70:1, 70:2, 77:12, 84:8, 89:21, 90:1, 90:8, 102:11 wanted 41:11, 56:15, 76:6, 98:15, 99:3, 101:22 water 30:15, 30:16, 31:17 watkins 2:12 watson 2:11, 3:5, 6:8, 9:16, 10:5, 10:19, 11:2, 11:3, 11:10, 11:16, 13:5, 13:9, 14:8, 14:9, 16:6, 24:17, 25:4, 35:8, 35:12, 35:16, 35:20, 37:14, 37:19, 41:9, 42:14, 42:21, 43:5, 43:11, 43:13, 44:22, 45:10, 45:14, 45:22, 46:18, 47:3, 48:11, 49:22, 50:7, 51:4, 54:8, 55:14, 58:11, 61:21, 62:10, 65:7, 66:16, 67:1, 69:8, 70:8, 72:9, 74:5, 74:13, 80:13, 80:17, 81:1,	86:2, 86:7, 88:18, 89:4, 92:17, 92:20, 93:7, 94:4, 94:9, 94:13, 94:15, 94:17, 95:3, 95:7, 95:12, 99:7, 99:10, 100:1, 100:15, 101:17, 102:4, 102:9, 102:22, 103:6 watson@lw 2:16 waveforms 51:19 waves 51:20 way 10:19, 17:13, 19:2, 20:1, 30:12, 31:11, 33:17, 41:7, 46:5, 48:9, 53:18, 54:6, 54:16, 54:22, 55:18, 56:14, 57:12, 64:15, 69:1, 69:10, 69:11, 74:3, 78:14, 79:10, 83:20, 95:9, 99:16, 104:21 ways 19:10, 29:22 we'll 42:22, 43:17, 72:13, 75:19, 90:6, 103:13 we're 26:15, 30:12, 35:13, 36:15, 43:2, 65:5, 69:6, 73:4, 88:4, 90:1, 97:2 we've 9:8, 98:9 week 10:10, 84:9	weeks 10:9 welcome 43:14, 94:18, 94:19 went 17:6, 43:7, 93:14 weren't 43:22, 98:14 west 98:20 whatever 19:7, 73:19, 80:1 whereof 105:2 whether 16:11, 32:13 whichever 11:11 white 10:21 whole 6:3, 28:3, 99:9 whoops 15:21, 88:21 wi 96:16 wikipedia 96:6 wire 20:19, 21:12, 21:19, 22:15, 23:12, 23:15, 33:4, 54:10, 56:4, 56:7, 57:2, 57:10, 57:14, 57:18, 57:21, 58:4, 58:7, 58:21, 60:2, 60:5, 60:13, 60:16, 61:10, 61:13, 61:20, 63:11, 63:22, 64:2, 64:22, 65:21, 66:18, 66:21,	67:2, 67:6, 67:13, 67:18, 68:13, 69:3, 69:12, 69:17, 77:20, 78:6, 79:5, 79:14, 82:9, 82:13, 83:4, 83:6, 83:8, 83:11, 85:1, 91:13, 91:22, 92:3, 92:5, 92:9, 92:12, 93:1, 93:6, 93:10, 93:17, 93:20, 96:1, 96:16, 96:22, 97:3, 97:17, 98:1, 98:6, 100:17 wire's 83:4 wired 23:8 wires 19:14, 20:21, 20:22, 21:7, 22:2, 22:17, 22:19, 23:1, 56:12, 56:14, 57:19, 58:15, 59:21, 60:10, 68:16, 85:12, 93:5, 96:19, 96:20, 97:7, 98:4, 99:21, 99:22 wiring 57:8 wisconsin 1:28, 104:5, 105:11 within 104:4 without 9:13, 33:20, 34:9, 40:12 witness 2:25, 4:25,
--	---	---	--

Transcript of Daniel Foty, Ph.D.
Conducted on January 9, 2026

138

6:4, 9:11, 9:21, 15:20, 16:1, 18:1, 19:1, 20:11, 22:16, 24:16, 24:22, 25:2, 32:15, 33:13, 35:10, 36:2, 37:16, 38:3, 41:4, 41:13, 42:9, 44:13, 45:12, 45:18, 46:4, 46:22, 47:21, 48:2, 48:6, 48:8, 49:16, 50:5, 50:14, 50:18, 52:12, 53:16, 54:2, 55:3, 58:6, 61:16, 62:3, 63:8, 65:4, 66:2, 66:20, 69:5, 69:15, 70:12, 72:5, 73:14, 74:10, 77:9, 80:20, 82:6, 82:16, 84:20, 85:15, 86:1, 86:5, 86:20, 88:21, 89:3, 89:18, 91:10, 91:16, 93:2, 94:7, 94:12, 94:14, 95:9, 98:11, 98:13, 98:22, 99:3, 99:14, 100:6, 101:14, 101:20, 102:6, 102:8, 102:9, 102:11, 102:16, 102:19, 103:1, 103:7, 104:6, 104:10, 105:2 witness's 1:19 wonderfully 27:3	wood 101:15, 101:21 word 15:1 words 17:15 work 16:7, 27:5, 57:3, 57:4 worked 10:17 working 28:3 world 33:4, 59:2 worry 58:10, 59:15, 59:22 worth 53:4, 63:2 wouldn't 79:16 write 17:15 writing 43:10 wrote 17:18, 19:22, 68:11 wuhan 3:24 Y yangtze 1:7, 2:17, 3:22, 4:15, 106:3 yankee 6:16 yea 74:12 yeah 22:10, 25:5, 25:16, 28:20, 39:22, 43:2, 43:20, 46:8, 62:11, 65:9, 77:5, 77:11,	80:12, 84:10, 90:1, 93:16, 94:9, 102:4, 102:7, 102:9, 102:14, 102:19 year 14:11, 14:12 years 56:18, 56:22, 57:4 yellow 10:20 yep 11:6, 48:12 yoshinaga 37:20, 38:7, 40:3, 41:1, 42:10, 44:11, 44:14, 45:4, 45:15, 46:1, 46:19, 47:10 yoshinaga's 40:19, 41:6 yourself 5:15 Z zhiguo 3:24 zoom 1:22, 104:15 0 00118 1:3, 11:22, 12:5 0029661 4:11 01 105:13 02 3:36 03 105:16 04 1:17, 104:17 05 105:16	05444 1:21 06 43:4 08 4:6, 105:13 084.004996 1:27, 105:10 1 1-5 82:2 10 39:2, 39:10, 40:18, 40:20, 41:17, 41:20, 42:6, 44:8, 44:10, 44:15, 45:2, 90:11, 90:12 10,879,164 1:3, 3:21, 3:28, 12:14, 12:18 1000 2:4 1001 3:20, 35:9, 35:15, 35:18 1003 3:25, 13:5, 13:7, 13:10, 14:3 1006 37:15, 37:17 1008 3:30, 61:22, 62:1 1039 3:35, 86:2, 86:3, 86:8, 86:14 104 3:7 1040 4:5, 88:18, 88:19, 89:5, 89:10
---	--	---	---

Transcript of Daniel Foty, Ph.D.
Conducted on January 9, 2026

139

1041 4:9, 80:13, 80:17, 80:18, 81:7 1042 4:13, 11:2, 11:13, 11:17, 11:21, 12:13, 14:8, 14:10, 14:16, 47:18, 95:7 105 3:9 106 3:11 107 3:13 108 1:34, 3:15 11 3:29, 4:13, 64:11, 64:14, 66:3, 66:8, 66:11, 67:22, 70:6 12 3:21, 4:17, 66:4, 66:7, 66:9, 66:14, 68:1, 68:3 120 82:15 121 70:14 126 70:10 12670 2:13 127 72:14 13 3:25, 44:14, 67:16, 69:17, 84:15 14 3:29, 68:2, 90:14, 91:3, 105:3	140 84:13, 84:16, 84:17, 84:19 142 70:11 143 72:13 144 48:1 14876 1:27, 105:9 15 35:22, 36:3, 36:5, 44:8, 62:18, 63:21, 64:6, 64:13, 65:5, 65:10, 65:20, 66:9, 66:14, 81:21, 82:1, 82:2 150 85:1 16 35:22, 36:3, 36:4, 36:5, 90:22, 92:10 160 82:9, 83:8, 85:12 164 12:17, 12:21, 12:22, 13:3, 16:13, 16:18, 16:21, 33:14, 33:17, 34:19, 35:7, 35:8, 36:1, 36:11, 37:5 18 17:19, 18:22, 19:4, 20:17, 21:11, 21:18, 22:4, 22:14, 22:20, 23:4, 23:11, 23:18, 24:1, 91:5, 91:6, 92:9, 92:12, 92:22,	93:21, 94:2 189 77:17 190335 105:12 194 67:16 195 62:16, 63:4 1990 35:2, 96:14 1a 91:20 1b 91:20 2 2 39:15 2/8/07 4:12 20 3:21, 4:6, 93:18 200 82:14, 82:19, 83:7, 83:10, 83:13 2002 27:3, 27:5, 67:4, 70:5, 86:9 2003 56:8, 57:6 2007 4:11 2008 89:8 2010 19:22 2011 19:22 2014 56:10, 57:16, 58:20, 61:9 2018 56:8, 57:6 2024 13:11	2025 1:3, 11:22, 12:5, 14:11 2026 1:15, 3:3, 104:16, 105:3, 106:14, 106:20 2029 105:13, 105:16 207 75:22, 76:9 20850 1:32 209 62:17 21 25:12, 39:1 22 36:22, 37:6, 39:3, 39:10, 85:4, 85:6, 85:11 221 76:4 23 3:36, 4:17, 14:13, 39:8 24 3:29, 25:15, 25:16 25 4:17 27 94:16 28 75:17, 76:10, 76:15 29 3:21 3 35 3:20 376 1:33 39 94:16 4 4-0 24:20, 24:21
---	--	--	--

Transcript of Daniel Foty, Ph.D.
Conducted on January 9, 2026

140

40 24:18, 25:18, 26:9, 89:17 400 1:31 41 33:11, 33:16, 93:13 433 1:33 44 56:5 45 64:4 451 1:31 452 1:20, 6:20 46 89:17 48 63:1 49 103:2 5 5-0 82:2 50 91:8, 92:4, 93:13 52 91:9, 92:4 523 2:15 54 1:17, 43:4, 103:2, 103:17, 104:17 5400 2:15 5450 2:15 56 39:2, 80:8 560 85:19 57 46:9, 46:10	580 85:19 6 6 1:17, 43:4, 104:17 6,424,263 3:36 6-2 70:9, 70:19, 73:11 6.2 73:15 609936 105:15 61 40:4, 42:10 614 2:6 614493 1:30, 106:2 62 3:30 64 30:4 650 2:6 67 46:10, 46:11 68 70:14 6a 92:11, 92:21, 93:2, 93:8, 93:10, 93:15, 93:16 6b 92:11, 92:21, 93:3, 93:8, 93:10, 93:15, 93:16 7 7 43:4 7,375,978 4:6	70 53:13, 95:1, 97:13 71 95:14, 95:16, 96:21, 97:6, 99:11, 100:3, 100:16 7400 2:6 7401 2:6 78 55:15, 55:17, 55:18, 56:3 79 48:8 8 8 1:17, 94:16, 103:2, 103:17, 104:17 80 4:9, 48:8, 57:5, 57:7 85 63:1 858 2:15 86 3:35 87 54:4, 55:6 88 4:5 888 1:33 9 9 25:12, 62:18, 63:21, 64:6, 64:11, 64:13, 64:14, 65:5, 65:10, 65:20, 66:3, 66:4, 66:8, 66:9,	66:11, 66:14, 67:16, 67:22, 68:1, 68:2, 68:3, 69:17, 70:6, 75:17, 76:10, 76:15, 91:14 9- 66:7 9-2 77:1, 77:5, 77:19, 78:4, 78:16, 78:18 9-5 64:21, 65:4, 65:12 9.2 77:3 9.28 76:18, 77:3 92 55:4 92130 2:14 94025 2:5 97 54:2
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