Agenda

- '164 Patent And The Challenged Claims
- **Yoshinaga Grounds (Grounds 1-2)**
  - Saved Area Limitations
  - Pad Group Limitations
  - **Common ESD Bus Limitations (Ground 2)**
  - Bonding Wire Limitations
- Saint Ground (Ground 3)
  - Saved Area Limitations
  - Common ESD Bus Limitations

"common ESD bus" (Claims 1-5, 8-11, 13)

1. An integrated circuit structure, comprising:
a circuit area;
a plurality of ESD buses;
a plurality of pad groups, adjacent and connected to the plurality of ESD buses;
a common ESD bus, adjacent to the plurality of pad groups; and
a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus;
wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

Ex. 1001 ('164 Patent), Claim 1

8. A method of integrated circuit structure, comprising:
forming a circuit area;
forming a plurality of ESD buses;
forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses;
forming a common ESD bus adjacent to the plurality of pad groups; and
connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires;
wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

Ex. 1001 ('164 Patent), Claim 8

13. The method of integrated circuit structure of claim **12**, wherein a common ESD bus is parallel to the plurality of ESD buses and the plurality of pad groups.

Ex. 1001 ('164 Patent), Claim 13

No Motivation To Add Haralabidis's Common Ground Rail To Yoshinaga

Petition

Third, a POSITA would have been motivated to use Haralabidis' common ground rail teaching to "ensure a solid return path for ESD protection" (Haralabidis, 2:55-61) and achieve Yoshinaga's goal of improve ESD protection (*see* Yoshinaga, [0007]-[0008]). Foty, ¶¶ 221-230. Yoshinaga already teaches connecting reference

Pet. 66

- **Yoshinaga already provides ESD protection**
- **Petition provides no evidence or reason why Yoshinaga's ESD protection was allegedly insufficient**

Yoshinaga

[0084]

Thus, in the chip shown in FIG. 6, ESD protective elements 9 (1) to 9 (4), 10 (1) to 10 (4), which are one of the major features of the present invention, are provided in the chip interior (previous ESD protective elements (not shown in FIG. 6) are provided in the underside of the power supply ring near the periphery of the chip as described above). Normally, it is difficult to use a large ESD protective element inside the chip, but in the present embodiment, the size of the ESD protective element may be small, as described above, so it is possible to greatly improve the ESD resistance while keeping the chip size as small as possible.

Ex. 1006 (Yoshinaga), [0084]

No Motivation To Add Haralabidis's Common Ground Rail To Yoshinaga

Petition

Third, a POSITA would have been motivated to use Haralabidis' common ground rail teaching to "ensure a solid return path for ESD protection" (Haralabidis, 2:55-61) and achieve Yoshinaga's goal of improve ESD protection (*see* Yoshinaga, [0007]-[0008]). Foty, ¶¶ 221-230. Yoshinaga already teaches connecting reference

Pet. 66

Patent Owner's Expert, Dr. Khatri

115. In my opinion, a POSITA would not have been motivated to look to other references like Haralabidis or Saint to connect reference potential lines 19 and 20 of Yoshinaga. Dr. Foty does not provide any reason that Yoshinaga's disclosures for connecting the reference potential lines 19 and 20 to a "third reference potential line 41" are inadequate or insufficient. Nor does Dr. Foty provide any reason why a POSITA would disregard Yoshinaga's disclosures of bidirectional diodes or the integrated circuit metallization and use bond wires instead—a fundamentally different connection method with disadvantages that I have mentioned supra. Dr. Foty does not identify any advantages with using bond wires or any drawbacks such "bond wires" would solve. And, as discussed above, Dr. Foty ignores the drawbacks of using bond wires altogether.

Ex. 2010 (Khatri Suppl. Decl.) ¶ 115

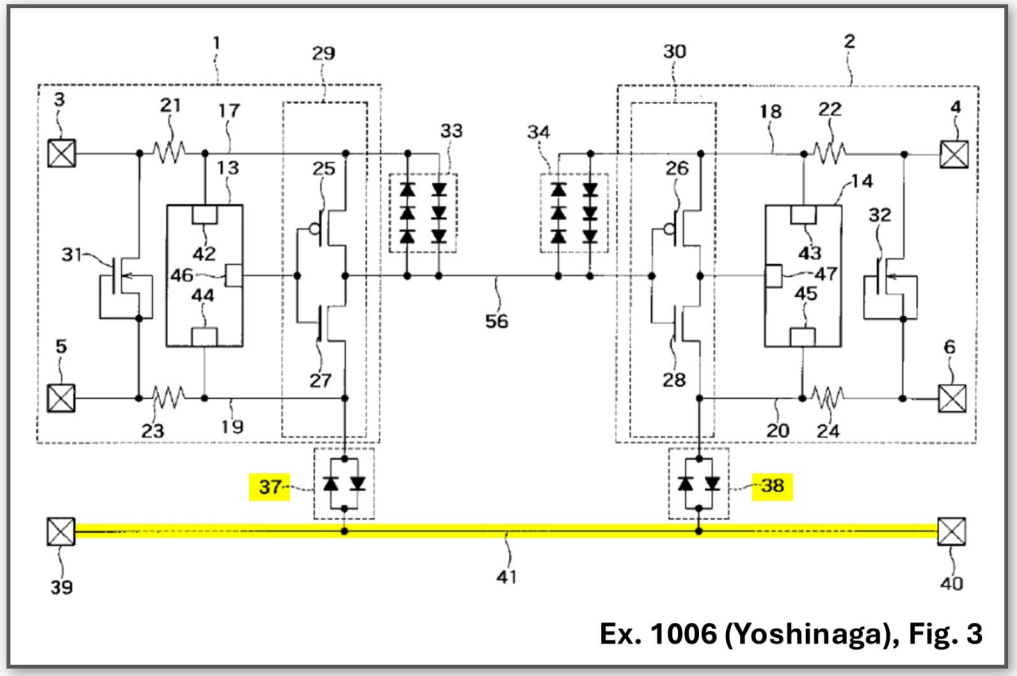
No Motivation To Add Haralabidis's Common Ground Rail To Yoshinaga

Petition

007]-[0008]). Foty, ¶¶ 221-230. Yoshinaga already teaches connecting reference potential lines for different circuits, but does not specifically teach how. Yoshinaga, Figs. 1-4, [0005], [0009], [0061]. A POSITA would have been motivated to look to

Pet. 66-67

- **Yoshinaga teaches connecting to a third reference potential line using a bidirectional diode pair to avoid noise**
- **Petition provides no evidence or reason why a POSITA would have allegedly ignored this teaching and its benefits**



Ex. 1006 (Yoshinaga), Fig. 3

[0061]

Also, unlike FIG. 1, in FIG. 3, the respective reference potential lines are separated between circuit 1 and circuit 2 to avoid noise between the reference potential lines and are connected to the third reference potential line 41 via a bidirectional diode pair 37 and a bidirectional diode pair 38. This third reference potential line 41 is used as a discharge path. A third reference potential line 41 is connected to the reference potential pad 39 and the reference potential pad 40. In this way, if reference potential line 41 is the discharge path for ESD, the ESD withstand capacity is lower due to the voltage drop due to forward characteristics of bidirectional diode pair 137 and bidirectional diode pair 38.

Ex. 1006 (Yoshinaga), [0061]

Agenda

- '164 Patent And The Challenged Claims
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  - Saved Area Limitations
  - Pad Group Limitations
  - Common ESD Bus Limitations (Ground 2)
  - **Bonding Wire Limitations**
- Saint Ground (Ground 3)
  - Saved Area Limitations
  - Common ESD Bus Limitations

Each Challenged Claim Recites Bonding Wires

1. An integrated circuit structure, comprising:
a circuit area;
a plurality of ESD buses;
a plurality of pad groups, adjacent and connected to the plurality of ESD buses;
a common ESD bus, adjacent to the plurality of pad groups; and
a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus;
wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

Ex. 1001 ('164 Patent), Claim 1

6. An integrated circuit structure, comprising:
a circuit area;
a plurality of ESD buses;
a plurality of pad groups, adjacent and connected to the plurality of ESD buses; and
a plurality of bonding wires configured to connect one to another of the plurality of pad groups;
wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

Ex. 1001 ('164 Patent), Claim 6

Each Challenged Claim Recites Bonding Wires

8. A method of integrated circuit structure, comprising:
forming a circuit area;
forming a plurality of ESD buses;
forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses;
forming a common ESD bus adjacent to the plurality of pad groups; and
connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires;
wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

Ex. 1001 ('164 Patent), Claim 8

12. A method of integrated circuit structure, comprising:
forming a circuit area;
forming a plurality of ESD buses;
forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses; and
connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires across the circuit area;
wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

Ex. 1001 ('164 Patent), Claim 12

Yoshinaga Uses Shorted Connections And Bidirectional Diodes To Connect The Reference Lines

Petition

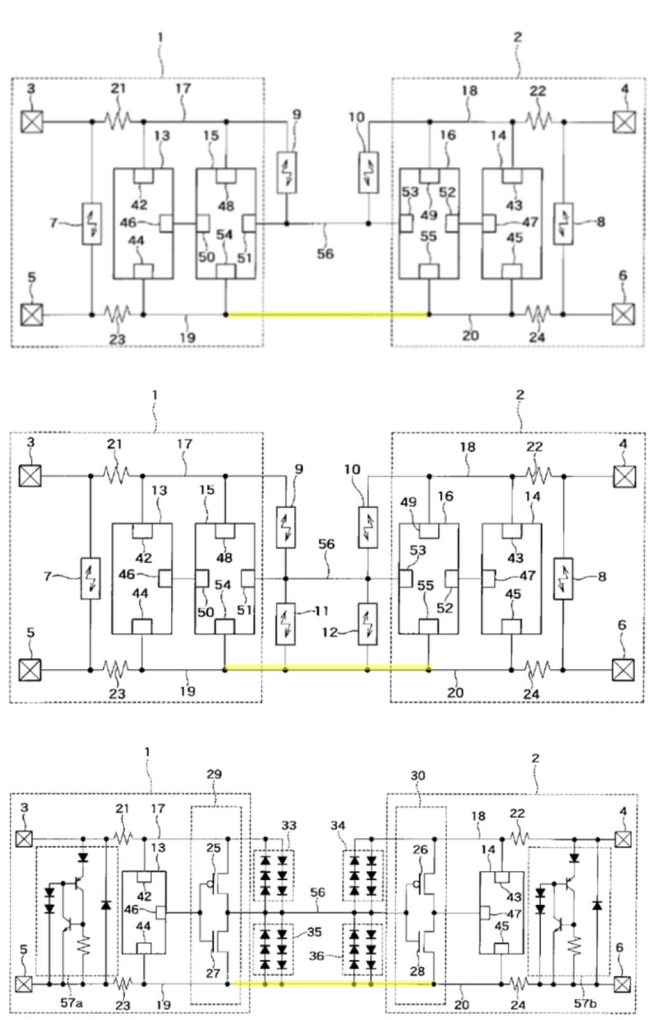
electrically connected to reference lines 19 and 20. Foty, ¶ 152, 130. Yoshinaga is silent regarding the mechanism used to connect the reference lines. An obvious way

Pet. 35

Patent Owner's Expert, Dr. Khatri

74. He also ignores that the disclosures in Figures 1, 2, and 4 of Yoshinaga show a short circuit connection between the reference potential lines 19 and 20 (in yellow below). Since Yoshinaga's teaching is about a "semiconductor integrated circuit," and does not mention packaging, or bond wires, this shorted connection would be understood by a POSITA to be through one of the metal layers used in the manufacture of the circuit. Yoshinaga, Abstract. No figure or disclosure in Yoshinaga discusses or shows the usage of bond wires to make any connection.

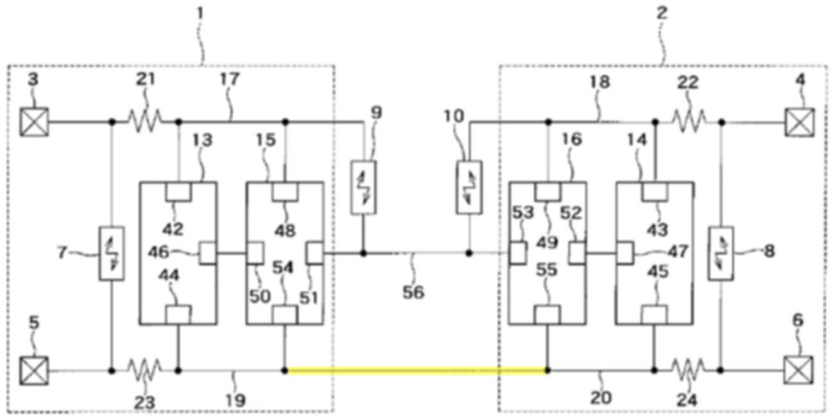
Ex. 2010 (Khatri Suppl. Decl.) ¶ 74



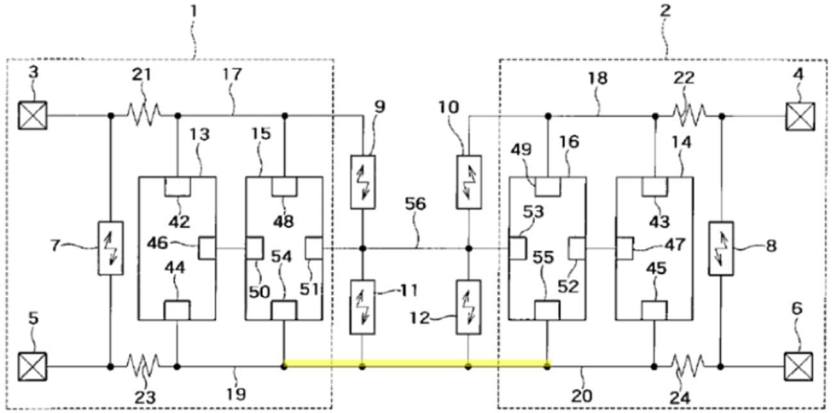
Ex. 2010 (Khatri Suppl. Decl.) ¶ 74

Yoshinaga Uses Shorted Connections And Bidirectional Diodes To Connect The Reference Lines

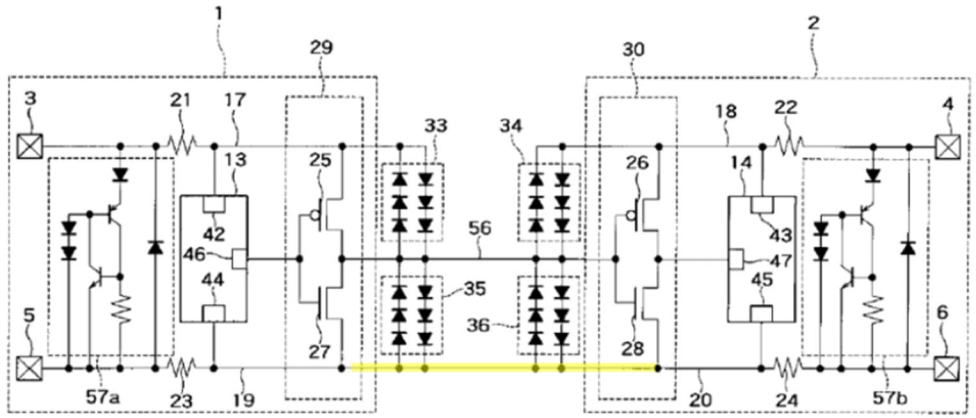
- **Yoshinaga's Figures 1, 2, and 4 show a shorted connection comprised of integrated circuit metallization**



[FIG. 1]



[FIG. 2]



[FIG. 4]

Ex. 2010 (Khatri Suppl. Decl.) ¶ 74

Yoshinaga Uses Shorted Connections And Bidirectional Diodes To Connect The Reference Lines

- **Dr. Foty agrees metallization is the "typical design" for connecting pads**

Patent Owner's Expert, Dr. Khatri

75. Dr. Foty confirmed that the typical pad to pad connection is made through the top most metal layer, and thus not using bonding wire.

Q. So you mentioned that typically the pads are connected via these different metal layers; is that correct?

A. **The typical design would be the pads would be connected to the top metal layer** and then, typically, that's required because if you think of it like a sandwich, you know, the bread on the bottom and the cheese on the top of the cheeseburger are separated from each other. So you stack the things up. And so the -- as you build the IC up in layers, you would build metal 1, metal 2, metal 3 to the top metal, and then the pads go above that. And so you typically would connect the pad downward to the top metal in order to start the process of having the pad -- you know, you have a -- essentially you have a metal path down to a transistor in order to have the circuit have functionality. Foty Dep. 90:2-20

Q. All right. So we -- for this example, I want to refer to a three-metal layer, okay?

A. Three-metal layer process?

Q. Yes. Three-metal layer process. Yes.

A. Okay.

Q. So we have a three-metal layer process with metal 1, 2, and 3. Okay?

A. Correct.

Q. Okay. Metal layer 1 is the bottom layer connection; is that fair?

A. In the -- in the inner connect stack which is above the circuitry, it would be the bottom layer. And in this figure we're looking at, this metal 1 is actually the highest layer you see depicted here in this vertical stack, but then metal 2 and metal 3 would be above that.

Q. Okay. And then metal 3 would be the topmost layer, correct?

A. If it's a three-metal process, yes, it would be the topmost layer.

Q. **And metal 3 would be what connects the different pads**; is that right?

A. That would be -- **That would be the typical implementation scenario**. *Id.* 91:13-92:18 (objections omitted).

Ex. 2010 (Khatri Suppl. Decl.) ¶ 75 (citing Ex. 2011, 90:2-20, 91:13-92:18)

Yoshinaga Uses Shorted Connections And Bidirectional Diodes To Connect The Reference Lines

- **Dr. Foty concedes Yoshinaga's Figure 1 includes integrated circuit metallization**

Petitioner's Expert, Dr. Foty

Q. Okay. So are the wires depicted in Figure 1, are they one of the different metal layer wires that we discussed before?

A. They would be comprised of the integrated circuit metallization in some way, shape, or form.

Ex. 2011 (Foty Tr.), 164:18-22

Yoshinaga Uses Shorted Connections And Bidirectional Diodes To Connect The Reference Lines

- **Yoshinaga's Figure 3 uses bidirectional diode pairs to avoid noise**

Yoshinaga

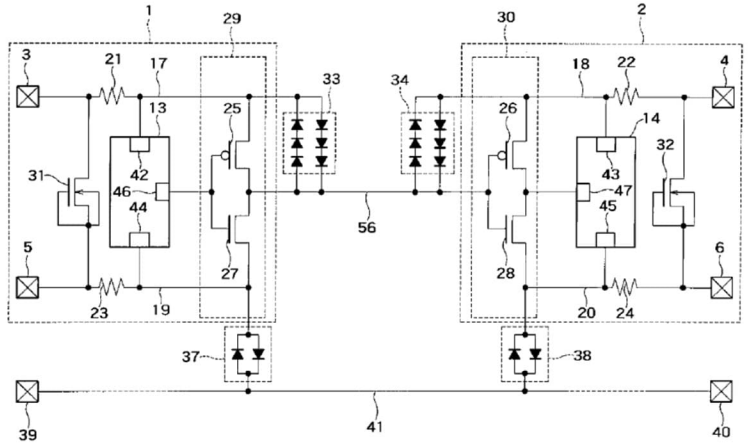
[0061]

Also, unlike FIG. 1, in FIG. 3, the respective reference potential lines are separated between circuit 1 and circuit 2 to avoid noise between the reference potential lines and are connected to the third reference potential line 41 via a bidirectional diode pair 37 and a bidirectional diode pair 38. This third reference potential line 41 is used as a discharge path. A third reference potential line 41 is connected to the reference potential pad 39 and the reference potential pad 40. In this way, if reference potential line 41 is the discharge path for ESD, the ESD withstand capacity is lower due to the voltage drop due to forward characteristics of bidirectional diode pair 137 and bidirectional diode pair 38.

Ex. 1006 (Yoshinaga), [0087]

Yoshinaga

[FIG. 3]



Ex. 1006 (Yoshinaga), Fig. 3

Yoshinaga Uses Shorted Connections And Bidirectional Diodes To Connect The Reference Lines

- **The shorted metallization connections in Yoshinaga's Figures 1-4 are relevant to Figure 6**

Yoshinaga

[0087]

[FIG. 1] A block diagram showing the configuration of a semiconductor integrated circuit according to an embodiment of the present invention.

[FIG. 2] A block diagram showing other configurations of semiconductor integrated circuits according to an embodiment of the invention.

[FIG. 3] A block diagram showing a specific example of the semiconductor integrated circuit of FIG. 1.

[FIG. 4] A block diagram showing the configuration of a circuit for performing a simulation to confirm the effect of the present embodiment.

[FIG. 5] A graph showing the results of simulation using the circuit in 4.

[FIG. 6] A schematic diagram of an integrated circuit chip including the semiconductor integrated circuit of FIG. 1.

Ex. 1006 (Yoshinaga), [0087]

Bonding Wires Would Have Increased Circuit Noise

Patent Owner's Expert, Dr. Khatri

protection. Moreover, because bond wires have inductance, using bond wires would actually add noise, which is contrary to Yoshinaga's teachings that bidirectional diodes should be used to "avoid noise." Dr. Foty does not explain why a POSITA would disregard Yoshinaga's disclosure of connecting the reference potential lines "by directional diodes to avoid noise" and use bond wires to connect the reference potential pads instead. He does not identify any

Ex. 2010 (Khatri Suppl. Decl.) ¶ 73

Davis

Because of severe IR-drop and switching noise problems, it has been shown that conventional wire-bonding technology, which constrains the power pads to be located at the chip periphery, is not a scalable concept for deep sub-micron technology [24]. On the other hand, utilizing area-array-bonding pads,

Ex. 2012 (Davis), 201

Bonding Wires Would Have Introduced Reliability Issues

Saint

Minimal Silicon Overlap

We have another issue in that corner. In Figure 9–15, the end pad is not in the corner of the chip, so the bond wire is overlapping too much of the silicon.

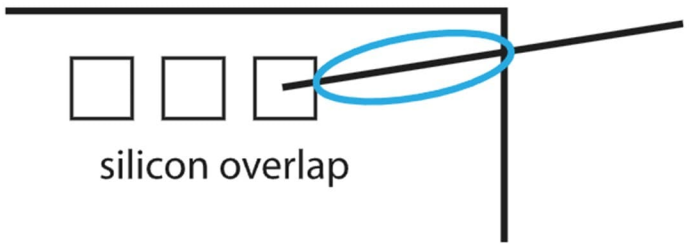


Figure 9–15. *Don't overlap any more silicon than you have to.*

Again, the bond wire could sag or droop, causing a short in the circuit. So, you have to keep the overlap of the bond wire over unused silicon as short as possible.

Ex. 1008 (Saint), 195

Petitioner's Expert, Dr. Foty

51. Note also how the bond wires exit the area of the IC as directly as possible; this is considered to be good practice – as wires that run above silicon circuit areas (particularly if the wires are relatively long – which they will more likely be if they exit the IC area less directly) can droop down onto the silicon and cause short-circuiting. *See* Saint, pp. 209-210 – and especially Figures 9-15, 9-16, and 9-17. Due to the nature of how bonding machines work – i.e., "pulling" a wire from one point to another – the resulting bond wires are typically straight (when viewed from above).

Ex. 1003 (Foty Decl.) ¶ 51

That Bond Wires Were "common" Does Not Mean They Would Have Been Obvious To Use In Yoshinaga



Forest Labs v. Sigmapharm Labs

An invention is not obvious simply because all of the claimed limitations were known in the prior art at the time of the invention. Instead, we ask "whether there is a reason, suggestion, or motivation in the prior art that would lead one of ordinary skill in the art to combine the references, and that would also suggest a reasonable likelihood of success." *Smiths Indus. Med. Sys., Inc. v. Vital Signs, Inc.*, 183 F.3d 1347, 1356 (Fed. Cir. 1999). The motivation "can be found explicitly or implicitly in the prior art references themselves, in market forces, in design incentives, or in 'any need or problem known in the field of endeavor at the time of invention and addressed by the patent.'" *Arctic Cat*, 876 F.3d at 1359 (quoting *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 420-21, 127 S. Ct. 1727, 167 L. Ed. 2d 705 (2007))."

***Forest Labs., LLC v. Sigmapharm Labs., LLC*, 918 F.3d 928, 934 (Fed. Cir. 2019)**

Board Should Reject Petitioner's New Obvious To Try Argument

Petitioner Reply

PO's insinuation that numerous bondwire alternatives exist (POR, 35-36) is unsupported, and contradicted by its expert who testified that only "two options [exist] for the matter at hand." EX1038, 157:23-158:20, *see also* 161:19-162:5. Thus, there are finite options a POSITA would try. Foty_Supp., ¶144.

Reply 4

Patent Owner's Expert, Dr. Khatri

85. However, I understand from Counsel that the fact that a technique was commonplace and well-established does mean it would be obvious to try. Neither the Petition nor Dr. Foty ever establish that there are only a finite, small or easily traversable number of options for connecting pads. And even if they did, they did not provide a reason a POSITA would select the specific route of using bond wires. In fact, for the reasons I discuss below, a POSITA would not select the use of bond wires when modifying Yoshinaga.

Ex. 2010 (Khatri Suppl. Decl.) ¶ 85

Yoshinaga's Uses Metallization To Connect Reference Lines

Petitioner Reply

reference. If PO's metallization argument were correct, Fig. 6 would show a metal trace connecting reference lines 19, 20, and 60, but it does not. Foty_Supp., ¶143; EX1038, 157:19-22, 179:25-180:23.

Reply 4

Petitioner's Expert, Dr. Foty

5, 6, 39, 40. *Id.*, [0078], Figs. 1-4. As such, a POSITA would understand that Yoshinaga Fig. 6 is merely an illustrative rendering, and is not intended to reflect the exact number of pads which may be present – or to convey their specific electrical connections. This is apparent, for example, by looking at the "power supply pads" 3, 4, and 58 in Figure 6 which are shown next to the ground rail; a POSITA would understand that those pads are connected to the power rails 17, 18, and 59 (as is shown in the schematics of Figures 1-4) – and are not connected to the ground rails 19, 20, and 60 (because such a connection would create a short circuit).

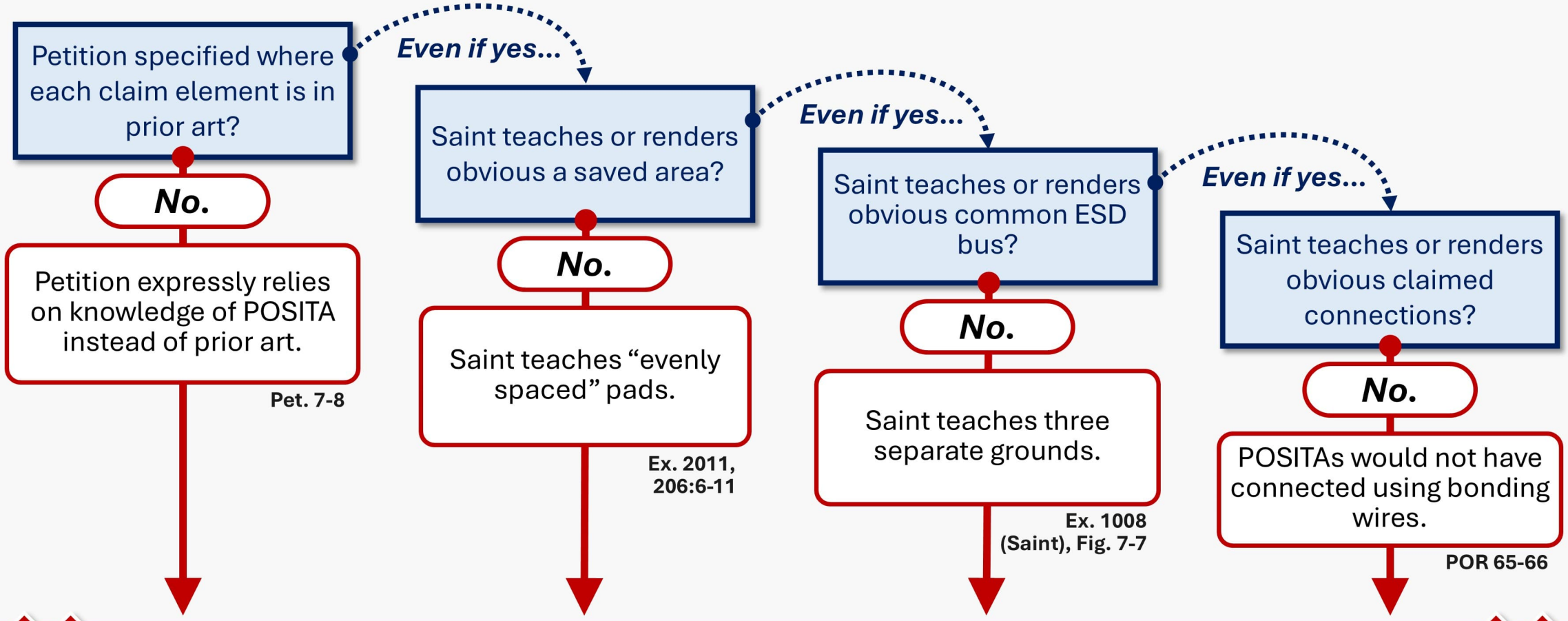
Ex. 1003 (Foty Decl.) ¶ 136

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- Yoshinaga Grounds (Grounds 1-2)
  - Saved Area Limitations
  - Pad Group Limitations
  - Common ESD Bus Limitations (Ground 2)
  - Bonding Wire Limitations
- **Saint Ground (Ground 3)**
  - **Saved Area Limitations**
  - Common ESD Bus Limitations

Saint-Based Grounds Fail For Multiple Reasons

Petitioner fails each hurdle to demonstrate obviousness on Saint grounds



Each Challenged Claim Recites A Saved Area

1. An integrated circuit structure, comprising:

* * *

wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

Ex. 1001 ('164 Patent), Claims 1, 6, 7, 12, 14

The claimed "saved area" must be:

- Within a "circuit area"
- Adjacent to "two respective ESD buses"
- Adjacent to "respective pads of two respective pad groups"
- Include "no ESD bus"
- Include "no pad"

Saint's Figure 7-7 Does Not Disclose The Location Of Pads

Saint

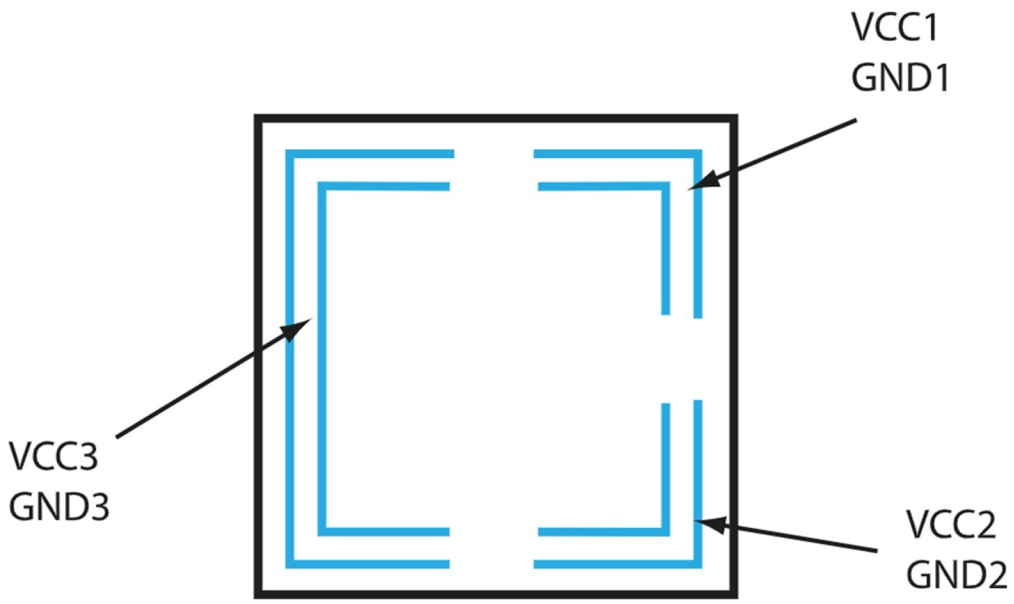


Figure 7–7. Pin-out simplification showing like protects grouped together.

Ex. 1008 (Saint), Fig. 7-7

Petitioner's Expert, Dr. Foty

Q. Does Figure 7-7 show any pads?

A. It does not, but it's implicit from the way this figure is put in that he's starting with the figure on Figure 7-6.

Ex. 2011 (Foty Tr.), 222:12-15

Petition relies exclusively on "Saint and a POSITA's knowledge" to assert obviousness for the saved area limitations

Petitioner Relies On Its Redrawn Version Of Saint's Figure 7-7 To Assert Obviousness

Saint

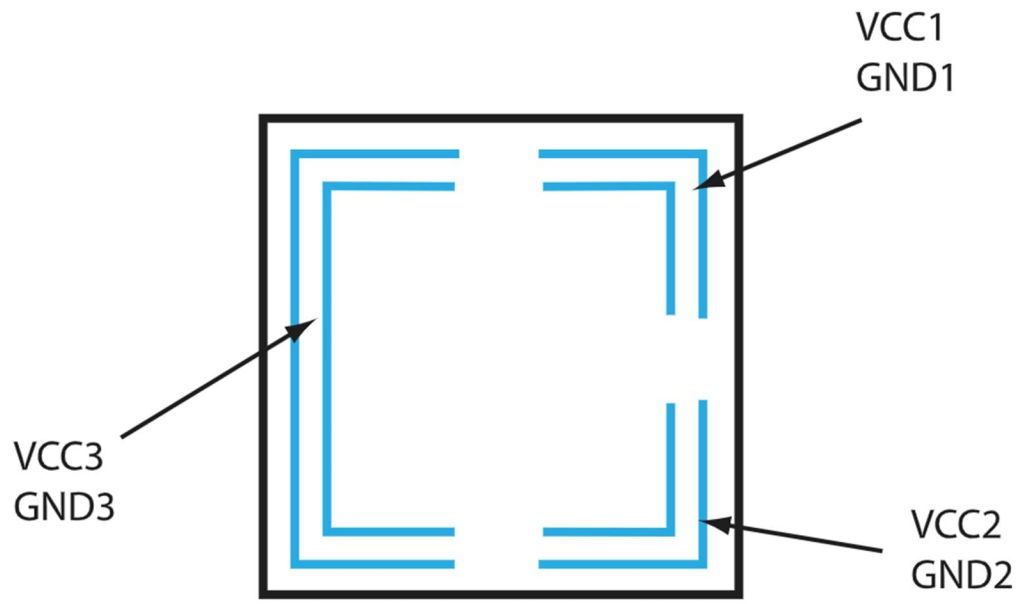


***Figure** 7–7. Pin-out simplification showing like protects grouped together.*

Ex. 1008 (Saint), Fig. 7-7

Petition

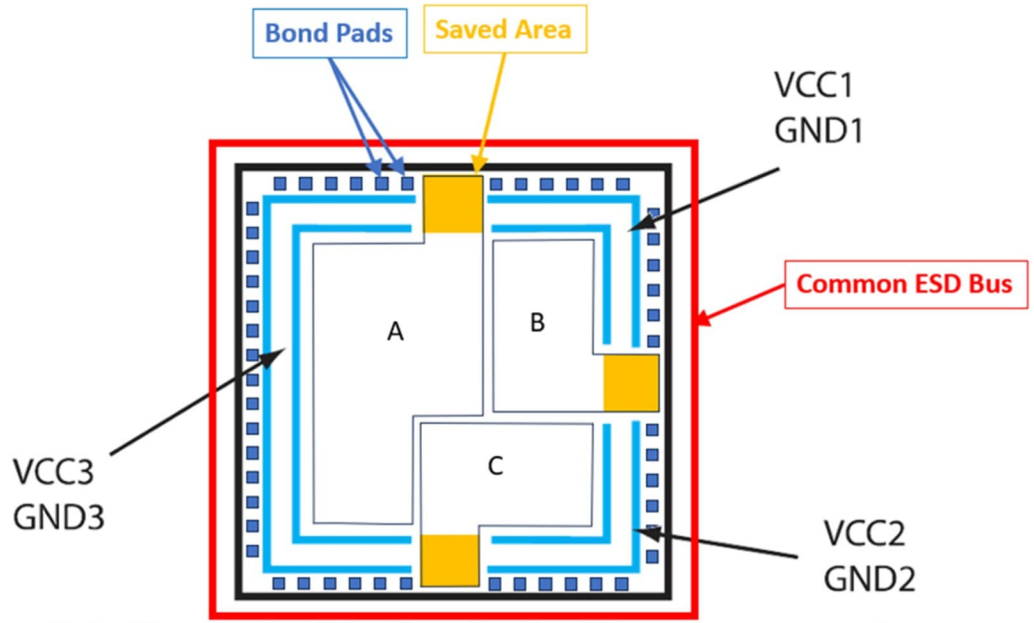


***Figure** 7–7. Pin-out simplification showing like protects grouped together.*

Pet. 83

Saint's Figure 7-6 Shows No Saved Area

Saint

Figure 7–6, showing the final pin-out for the package, shows the coordinated colors for each of these protection schemes.

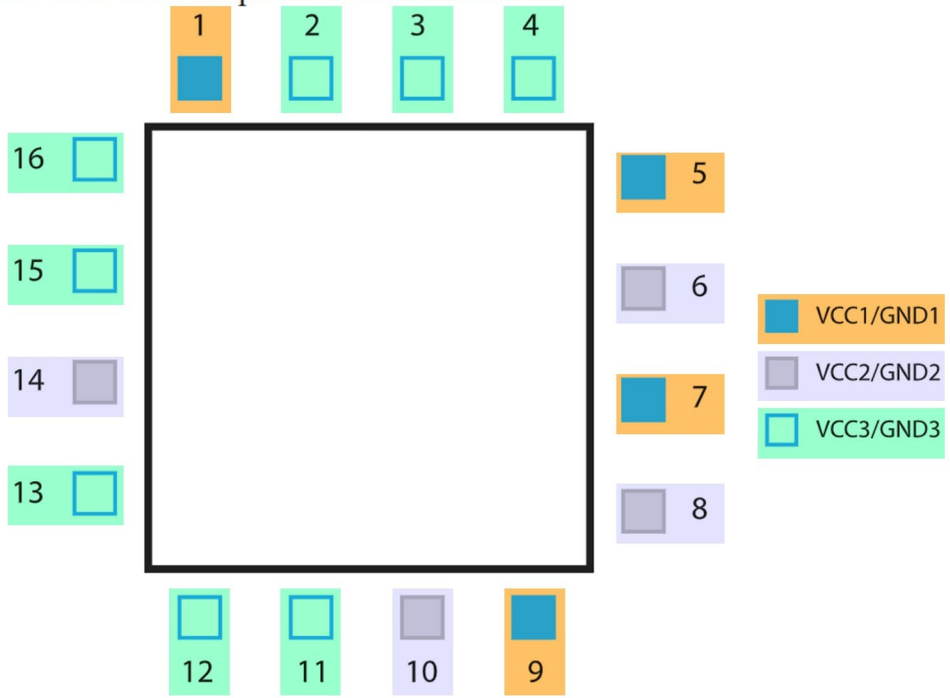


Figure 7–6. *Scattered pins on the same protect circuit.*

Ex. 1008 (Saint), Fig. 7-6

Saint

A nicer way to prepare for this chip's layout is to try to renegotiate the pin-out with the circuit designers. Let's ask our circuit designer to take the four signals that were on pins 1, 5, 7, and 9 and move them close to each other. With that change, we get all those signals that were protected to the same supply close to each other. We end up with this nice, small, short, self-contained area for the set of signals. We do the same for the other supply pin sets.

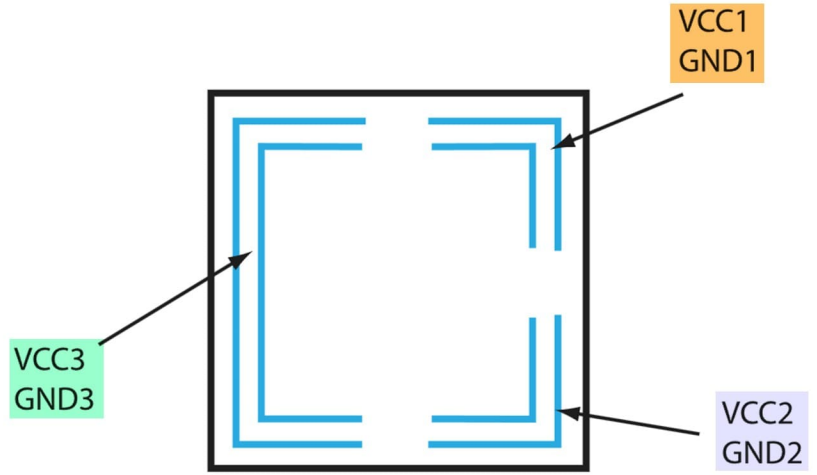


Figure 7–7. *Pin-out simplification showing like protects grouped together.*

Ex. 1008 (Saint), 147, Fig. 7-7

Saint Teaches Having The Pads "evenly spaced"

Saint

Figure 7–6, showing the final pin-out for the package, shows the coordinated colors for each of these protection schemes.

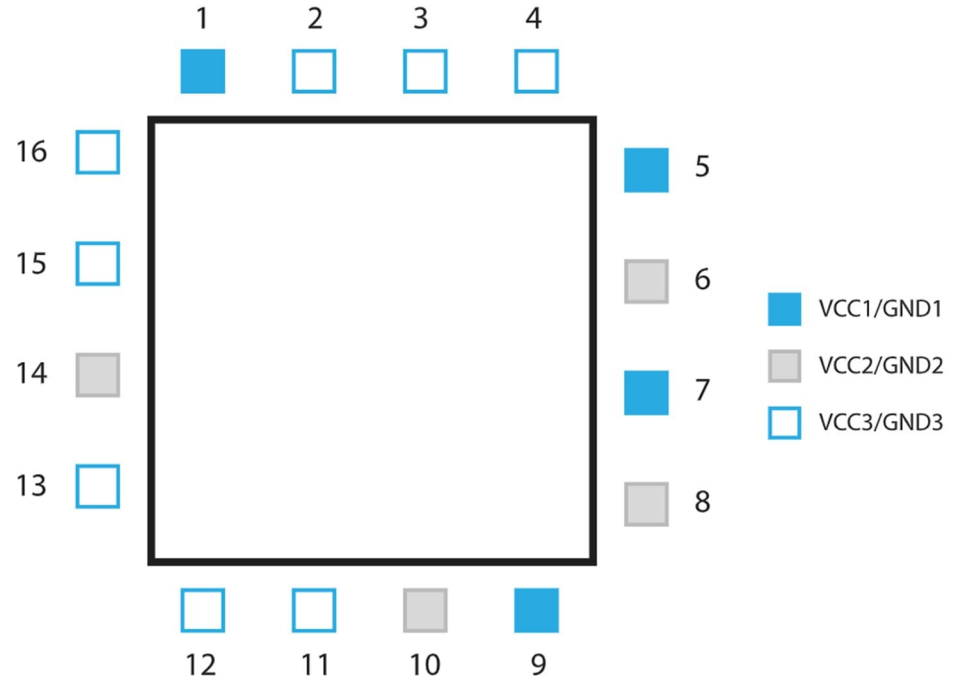


Figure 7–6. *Scattered pins on the same protect circuit.*

Ex. 1008 (Saint), Fig. 7-6

Petitioner's Expert, Dr. Foty

A. …He basically shows - below, he shows a -- shows IC with -- exemplary IC with 16 pins and you put it in a package with more than 16 pins. And by having them evenly spaced, you're able to connect them in nice, straight lines to -- the pads to the traces in the package.

Ex. 2011 (Foty Tr.), 206:6-11

No Motivation To Add A Saved Area

- **Adding a saved area would not reduce chip size or provide ESD protection**

Saint

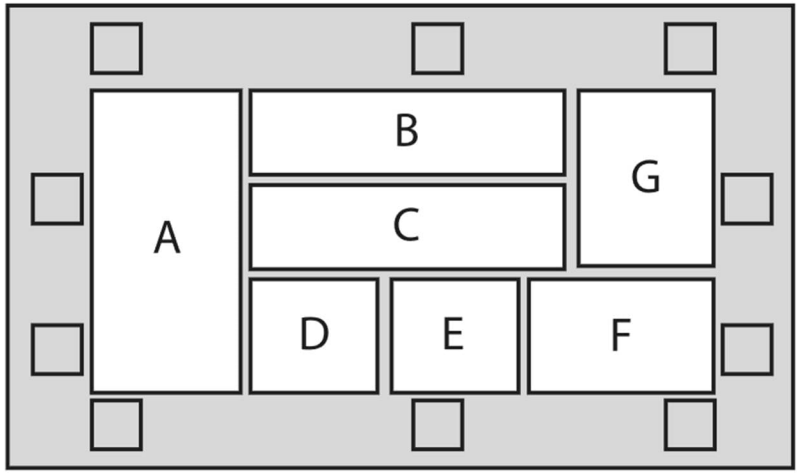


Figure 9–21. *The minimum size of the chip limited by the anticipated sizes of the blocks.*

Ex. 1008 (Saint), 199, Fig. 9-21

Saint

Filling Pad Gaps

If you do have a core-limited circuit design, you will have wasted space around the edges between the pads. Maybe you can push some of your circuitry into this wasted space to try to use those gaps.

If you are reusing circuits, then you can re-lay parts of your circuit elements in and around these pads trying to get the chip as small as possible.

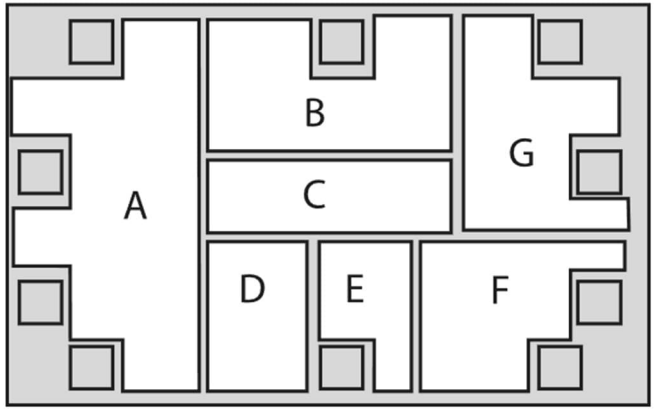


Figure 9–28. *We can use extra space surrounding our pads to shrink our chip size.*

Ex. 1008 (Saint), 207-208, Fig. 9-28

No Motivation To Add A Saved Area

- **Adding a saved area would not reduce chip size or provide ESD protection**

Saint

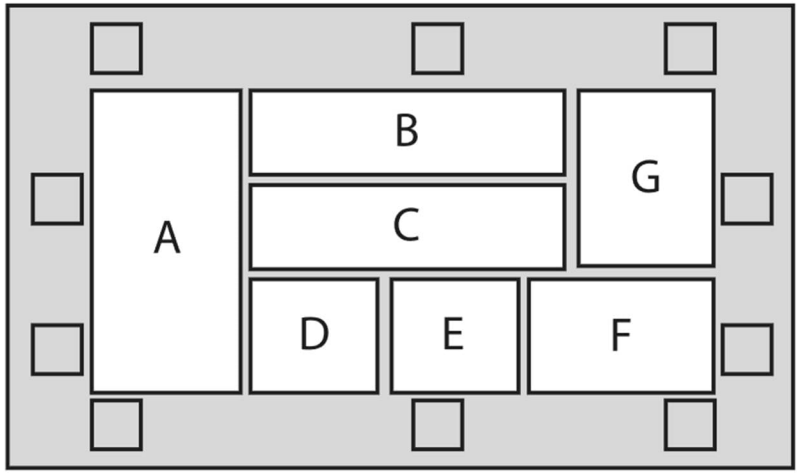


Figure 9–21. *The minimum size of the chip limited by the anticipated sizes of the blocks.*

Ex. 1008 (Saint), 199, Fig. 9-21

≠

Saint

Figure 7–6, showing the final pin-out for the package, shows the coordinated colors for each of these protection schemes.

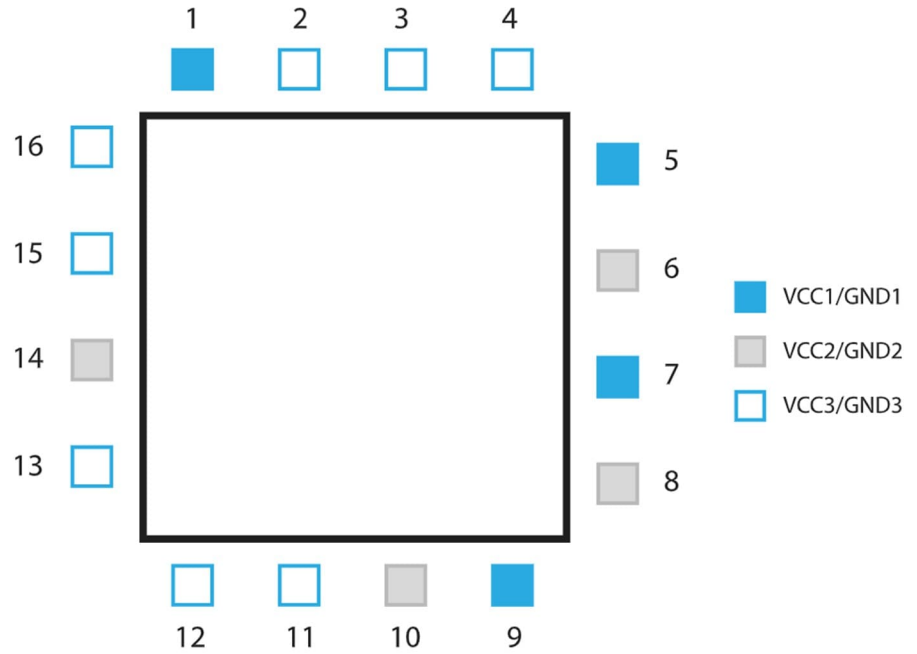


Figure 7–6. *Scattered pins on the same protect circuit.*

Ex. 1008 (Saint), Fig. 7-6

No Motivation To Add A Saved Area

- **Adding a saved area would not reduce chip size or provide ESD protection**

Saint

Find the minimum required spacing between the pads, and squeeze those pads as close together as you can in a rectangular shape. Then you say, "That's my chip. That's pad-limited."

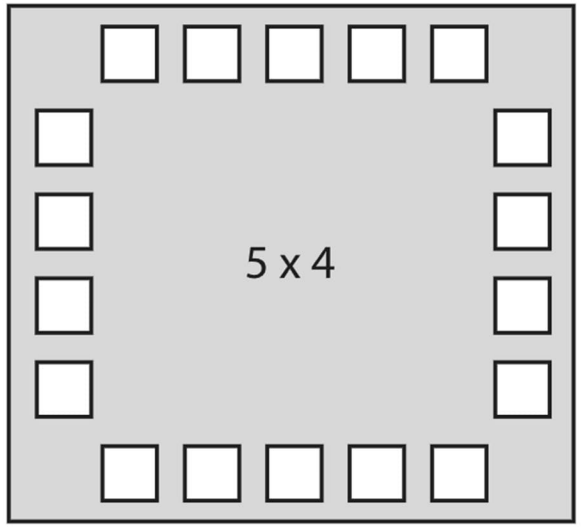


Figure 9–20. *The minimum size of an 18-pad chip, based on the number of pads.*

Ex. 1008 (Saint), 198, Fig. 9-20

Saint

Figure 7–6, showing the final pin-out for the package, shows the coordinated colors for each of these protection schemes.

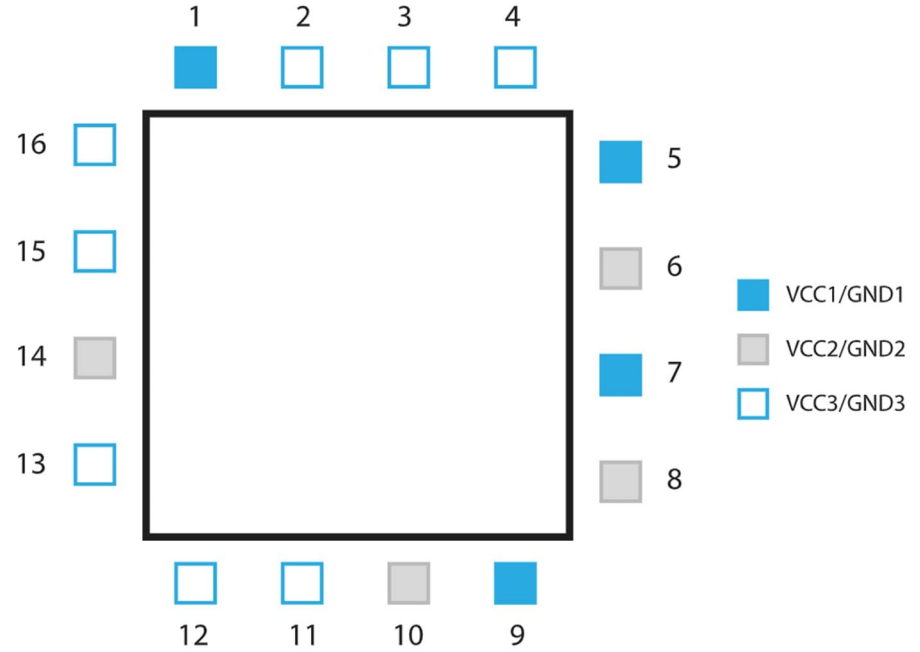


Figure 7–6. *Scattered pins on the same protect circuit.*

Ex. 1008 (Saint), Fig. 7-6

No Motivation To Add A Saved Area

- **Adding a saved area would not reduce chip size or provide ESD protection**

Patent Owner's Expert, Dr. Khatri

image because they are both "core-limited IC designs." Ex.1003 ¶ 384. But Saint Figure 7-7 is never described as a "core-limited IC design," and Dr. Foty does not provide any citation to suggest that it is. Instead, he seems to be

Ex. 2010 (Khatri Suppl. Decl.) ¶ 147

Patent Owner's Expert, Dr. Khatri

149. Petitioner is incorrect in claiming that a POSITA would have formed the "saved area" in order "to achieve the benefits of smaller chip size and ESD protection." Pet. 81. This claim is made without showing why Saint's ESD protection in Figure 7-7 needs to be improved. A POSITA would understand that Saint's ESD protection is accomplished in a manner that "makes the chip smaller, keeps parasitics down, and keeps cross talk down from one supply to another." Saint, 147. Further, a POSITA would not be motivated to add an area that Petitioner shows in their modification of Figure 7-7 of Saint, adjacent to pads without pads or an ESD bus because it would make the chip larger, not smaller, due to the insertion of the alleged "saved area."

Ex. 2010 (Khatri Suppl. Decl.) ¶ 149

Petition Fails To Show That Saint Figure 9-21 Renders Any Claim Obvious

Patent Owner's Expert, Dr. Khatri

132. The Petition states Ground 3 "relies on a set of teachings (primarily from Saint) applied to Saint's IC in Fig. 7-7, but the results are the same if Saint's IC in Fig. 9-21 is used as a baseline." Pet. 68. I agree that the challenged claims are nonobvious in view of using Saint's Figure 9-21 as a baseline for the same reasons as I list in this declaration for Saint Figure 7-7. Further, the Petition and Dr. Foty do not establish how every limitation of each claim would be taught or obvious in view of Saint Figure 9-21, and never even mentions Saint Figure 9-21 in connection with what the Petition identifies as claim limitations 1.B, 1.C, 1.D, 1.E, claim 2, claim 3, claim 4, claim 5, 6.B, 6.C, 6.D, claim 7, 8.B, 8.C, 8.D, 8.E, claim 9, claim 10, claim 11, 12.B, 12.C, 12.D, and claim 14.

Ex. 2010 (Khatri Suppl. Decl.) ¶ 132

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Agenda

- '164 Patent And The Challenged Claims
- Yoshinaga Grounds (Grounds 1-2)
  - Saved Area Limitations
  - Pad Group Limitations
  - Common ESD Bus Limitations (Ground 2)
  - Bonding Wire Limitations
- **Saint Ground (Ground 3)**
  - Saved Area Limitations
  - **Common ESD Bus Limitations**

"common ESD bus" (Claims 1-5, 8-11, 13)

1. An integrated circuit structure, comprising:
a circuit area;
a plurality of ESD buses;
a plurality of pad groups, adjacent and connected to the plurality of ESD buses;
a common ESD bus, adjacent to the plurality of pad groups; and
a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus;
wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

Ex. 1001 ('164 Patent), Claim 1

8. A method of integrated circuit structure, comprising:
forming a circuit area;
forming a plurality of ESD buses;
forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses;
forming a common ESD bus adjacent to the plurality of pad groups; and
connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires;
wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

Ex. 1001 ('164 Patent), Claim 8

13. The method of integrated circuit structure of claim **12**, wherein a common ESD bus is parallel to the plurality of ESD buses and the plurality of pad groups.

Ex. 1001 ('164 Patent), Claim 13

Ground 3 Fails To Establish A Common ESD Bus Was Obvious For 3 Reasons

1. Saint Fig. 7-7 lacks a common ESD bus
2. Saint Fig. 7-7 teaches away from adding a common ESD bus
3. No motivation to add a common ESD Bus to Saint Fig. 7-7 in view of Case Study 1 or Haralabidis due to design differences

Ground 3 Fails To Establish A Common ESD Bus Was Obvious For 3 Reasons

1. **Saint Fig. 7-7 lacks a common ESD bus**
2. Saint Fig. 7-7 teaches away from adding a common ESD bus
3. No motivation to add a common ESD Bus to Saint Fig. 7-7 in view of Case Study 1 or Haralabidis due to design differences

Saint Fig. 7-7 Lacks A Common ESD Bus

Saint

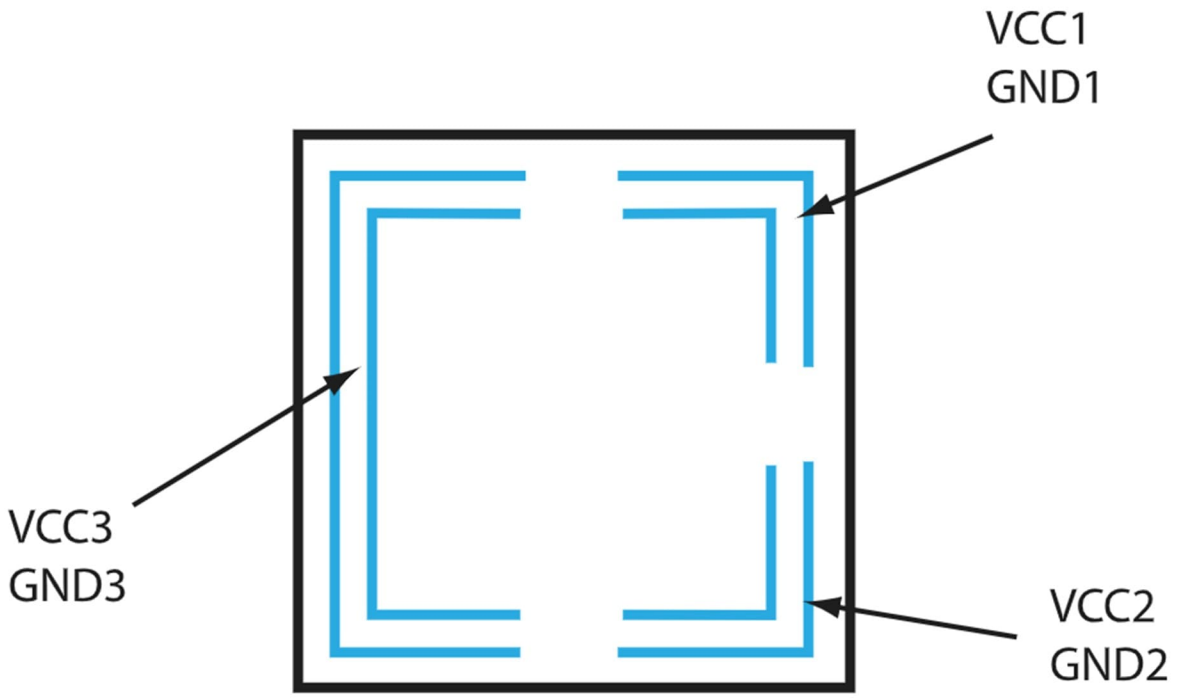


Figure 7–7. *Pin-out simplification showing like protects grouped together.*

Ex. 1008 (Saint), Fig. 7-7

Petitioner's Expert Admits Saint Chapter 7 Describes "separate" And "different" Grounds

Petitioner's Expert, Dr. Foty

359. As explained above (in the discussion associated with claim element [1c]), in the Chapter 7 discussion Saint has depicted a design where there are three separate power supply and three separate ground lines – with each ground buss (i.e., GND 1, GND 2, and GND 3) providing a ground bus which is connected to the "diode inner terminals (anodes)" of the ESD protection circuitry of the pins associated with the particular tandem (e.g., VCC 1 and GND 1) of power supply rail and ground rail.

Ex. 1003 (Foty Decl.) ¶ 359

Saint

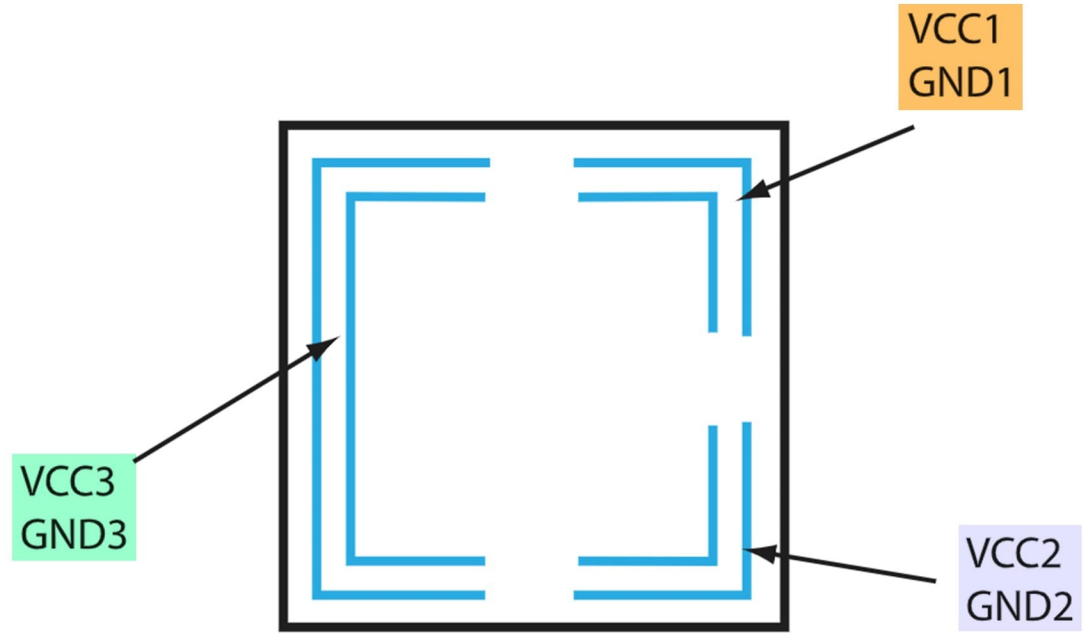


Figure 7–7. *Pin-out simplification showing like protects grouped together.*

Ex. 1008 (Saint), Fig. 7-7

Petitioner's Expert Admits Saint Chapter 7 Describes "separate" And "different" Grounds

Petitioner's Expert, Dr. Foty

Q. Now, on Figure 7-7 of Saint, there's three different ground signals, correct?

A. In this particular instantiation. I guess in the patent world, you call it an embodiment. He shows a particular design where he has three different power supplying ground buses due to the circuit blocks that will be inside there.

Ex. 2011 (Foty Tr.), 228:14-20

Saint

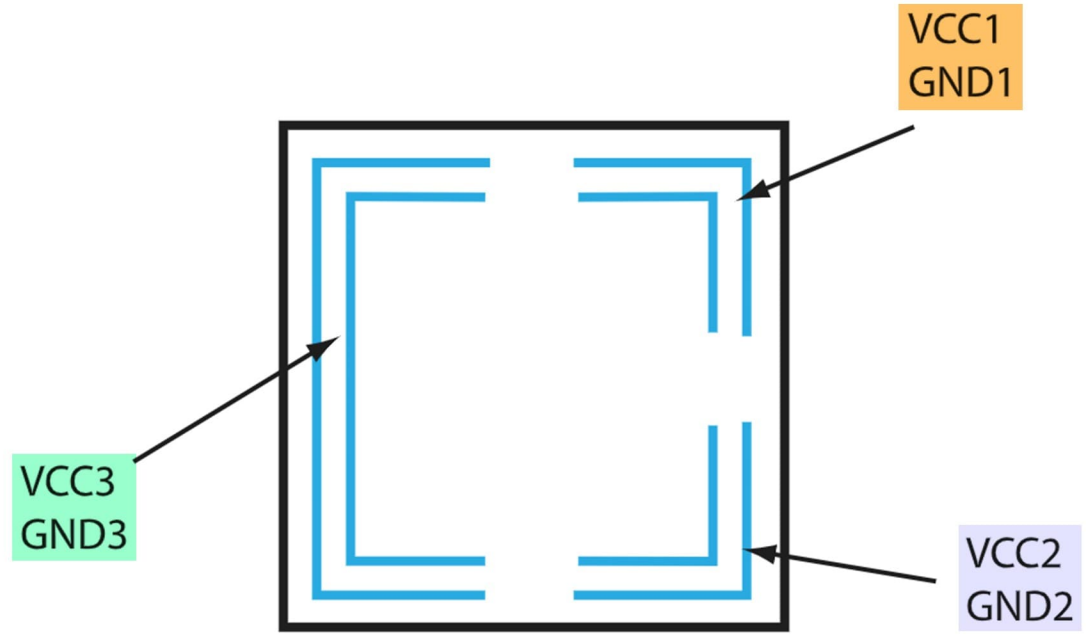


Figure 7–7. *Pin-out simplification showing like protects grouped together.*

Ex. 1008 (Saint), Fig. 7-7

Board Should Reject Petitioner's New Argument That Fig. 7-7 Involves A Single Ground

Petitioner Reply

Saint, Fig. 6-2. A POSITA would have understood Fig. 7-7's GND1/GND2/GND3 designations simply reflect that they correspond to VCC1/VCC2/VCC3, respectively. Foty_Supp., ¶¶122-123. Differing supply voltages (*e.g.*, VCC1=3V, VCC2=5V, etc.) does not mean reference voltages differ. To the contrary, as Saint Fig. 6-2 shows, GND1, GND2, etc. are the same. Haralabidis confirms this. *Id.*

Reply 14

- **Petition only relied on Haralabidis and Case Study 1 for teaching a common ESD bus**

Figs. 7-3, 7-4, And 7-5 Confirms Three Separate And Distinct ESD Buses

Saint

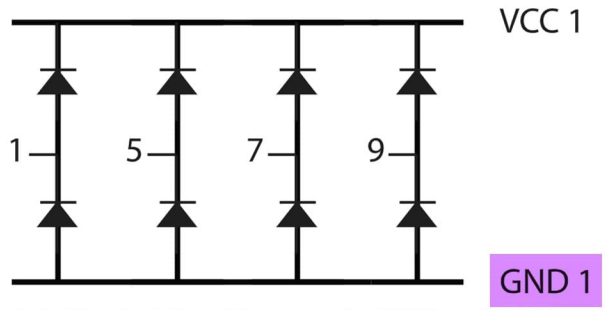


Figure 7–3. Pins 1, 5, 7, and 9 protected to VCC1 and GND1.

Ex. 1008 (Saint), Fig. 7-3

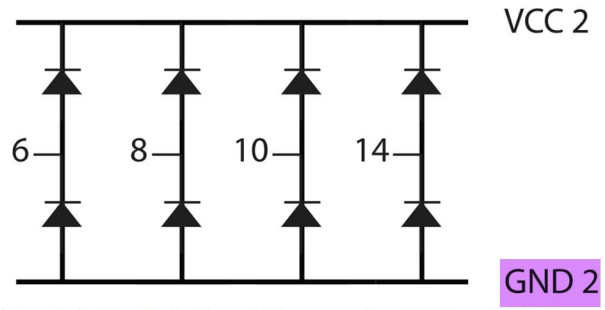


Figure 7–4. Pins 6, 8, 10, and 14 protected to VCC2 and GND2.

Ex. 1008 (Saint), Fig. 7-4

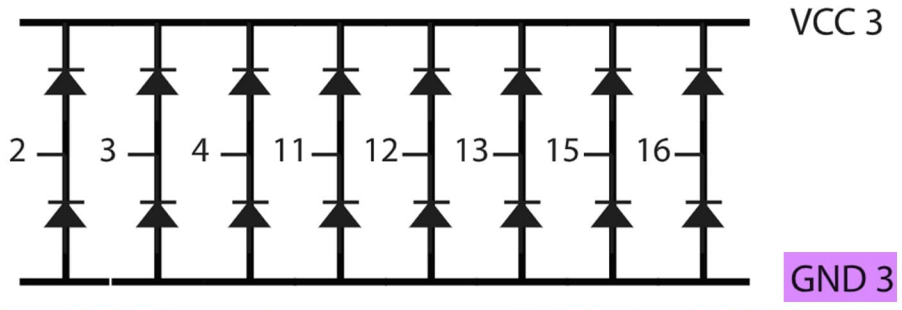


Figure 7–5. The remaining pins protected to VCC3 and GND3.

Ex. 1008 (Saint), Fig. 7-5

Fig. 7-6 Confirms Three Separate And Distinct ESD Buses

Saint

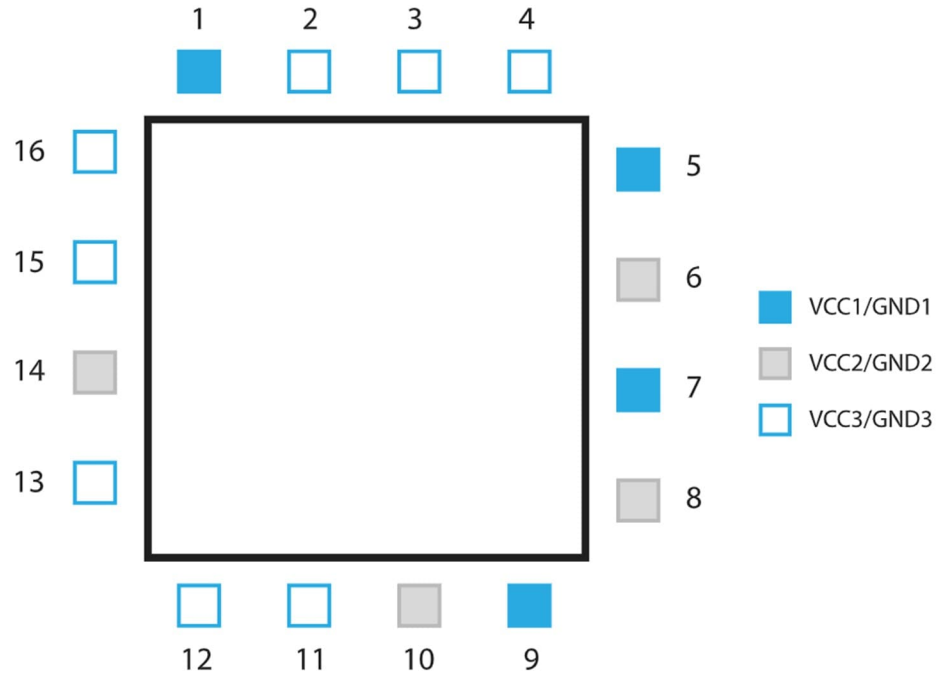


Figure 7–6. Scattered pins on the same protect circuit.

Ex. 1008 (Saint), Fig. 7-6

Saint

with the circuit designers. Let's ask our circuit designer to take the four signals that were on pins 1, 5, 7, and 9 and move them close to each other. With that change, we get all those signals that were protected to the same supply close to each other. We end up with this nice, small, short, self-contained area for the set of signals. We do the same for the other supply pin sets.

Ex. 1008 (Saint), 147

Fig. 7-7 Are Different And Separate Ground Signals

Saint

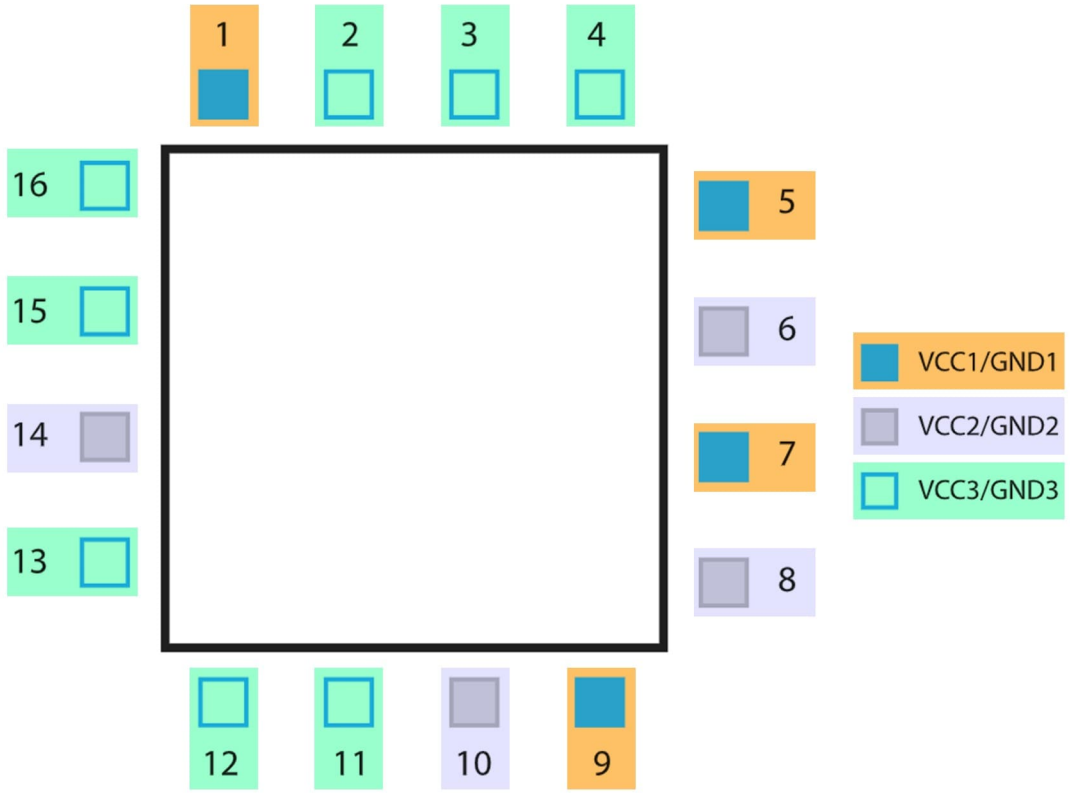


Figure 7–6. *Scattered pins on the same protect circuit.*

Ex. 1008 (Saint), Fig. 7-6

Saint

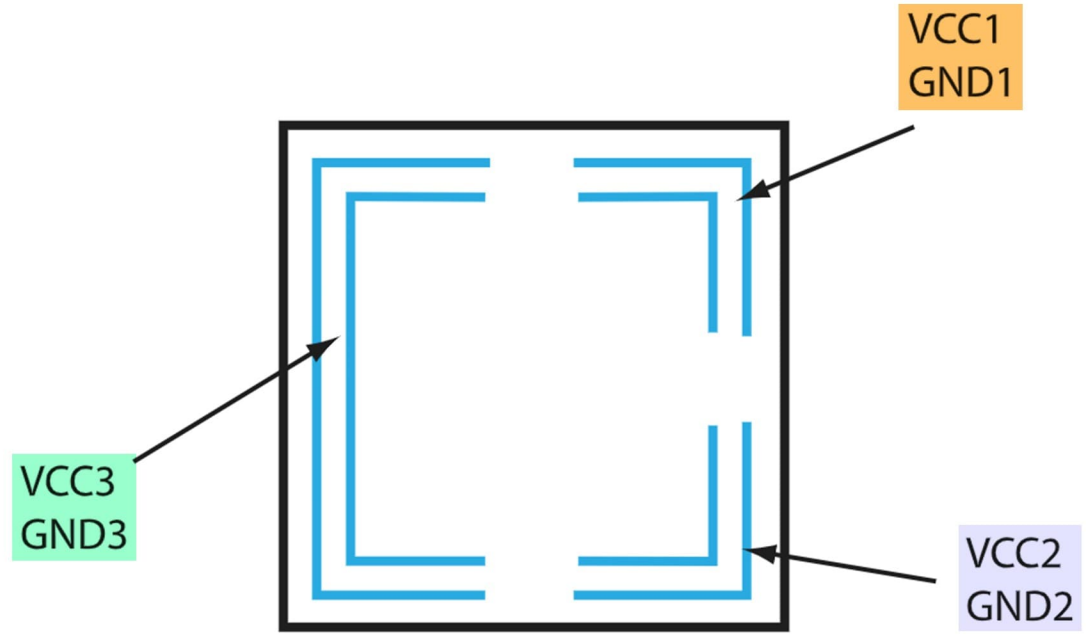


Figure 7–7. *Pin-out simplification showing like protects grouped together.*

Ex. 1008 (Saint), Fig. 7-7

Saint Fig. 6-2 Is A Separate Embodiment From Fig. 7-7

So, you make a wall. You make all the noisy circuitry go inside its own little house.

There are various layout techniques to make that wall. How you build your wall depends on who you are, what process you have, and what test chips have been made. The method is variable, but one easy way is to wrap a big ring of ground substrate contacts around the whole block. Remember, noise travels through substrate very easily.

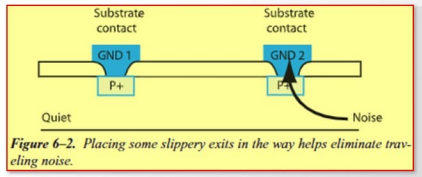


Figure 6–2. Placing some slippery exits in the way helps eliminate traveling noise.

As the noise tries to escape the block through the substrate, it first encounters a ground substrate contact. Hopefully, any noise voltages or noise currents will be attracted to this contact since it is grounded.

If we were to have a very small substrate contact as our ring, noise could work its way around or underneath it. A big contact means the noise can't get through. So make it a decent size.

Here's a bond pad in Figure 6–3, labeled GND. We put a voltage source on the pad, which measures zero volts. Then, as you can see, we have a thin, skinny resistive wire that connects to the substrate ring around our noisy area.



Figure 6–3. You might think it's grounded, but with what size wire?

This must be the work of someone new who hasn't read their books yet. They think they have grounded the substrate ring, their noisy source, adequately.

Micron Ex. 1008, p. 142
Micron v. YMTC
IPR2025-00118

CHAPTER 6

Saint

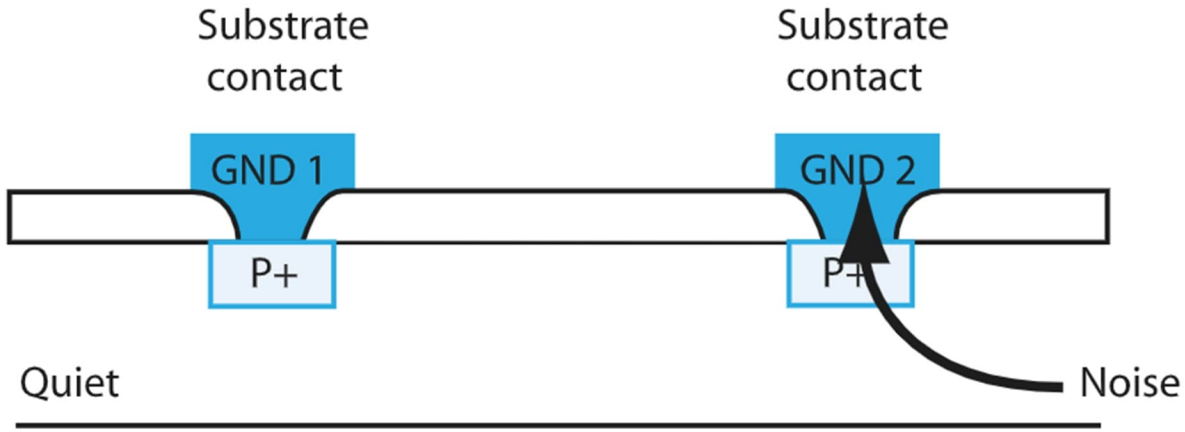


Figure 6–2. *Placing some slippery exits in the way helps eliminate traveling noise.*

Ex. 1008 (Saint), 126, Fig. 6-2

Ground 3 Fails To Establish A Common ESD Bus Was Obvious For 3 Reasons

1. Saint Fig. 7-7 lacks a common ESD bus
2. **Saint Fig. 7-7 teaches away from adding a common ESD bus**
3. No motivation to add a common ESD Bus to Saint Fig. 7-7 in view of Case Study 1 or Haralabidis due to design differences

Saint Chapter 7 Teaches Away From A Common ESD Bus

Saint

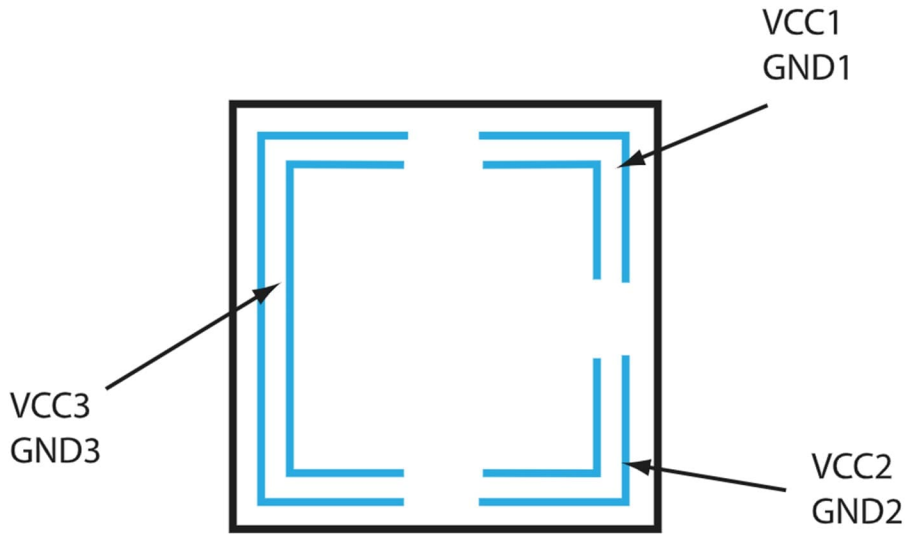


Figure 7–7. *Pin-out simplification showing like protects grouped together.*

Ex. 1008 (Saint), Fig. 7-7

Saint

We have all the pins that are protected to VCC 2 and GND 2 now located close to each other. It makes layout easier, makes the chip smaller, keeps parasitics down, and keeps cross talk down from one supply to another.

Ex. 1008 (Saint), 147

Saint Chapter 7 Teaches Away From A Common ESD Bus

Saint

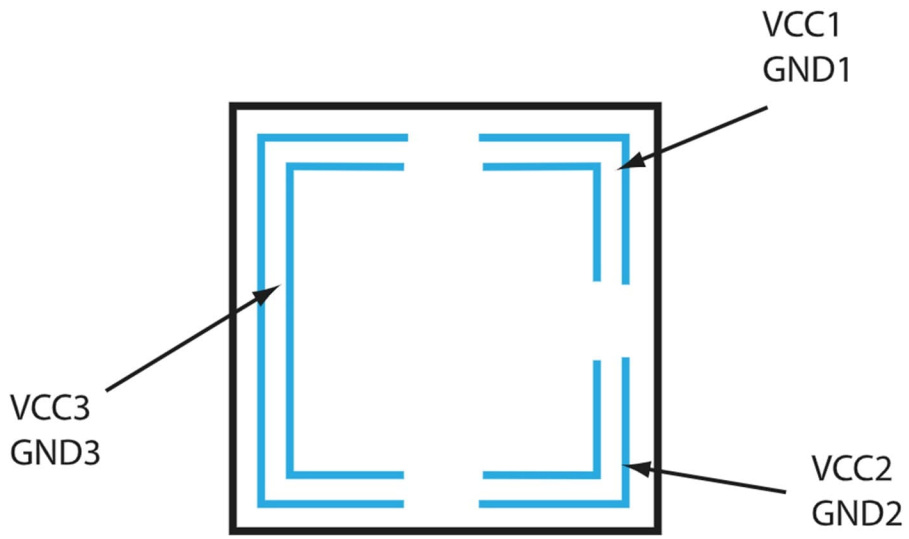


Figure 7–7. *Pin-out simplification showing like protects grouped together.*

Ex. 1008 (Saint), Fig. 7-7

Patent Owner Expert, Dr. Khatri

like the one Dr. Foty points to in Haralabidis. Connecting three separate signals together to a "common ESD ground" would drastically alter the electrical characteristics of the design and require other modifications as well. Such a modification would result in noise from one circuit being injected into another, which would result in a degradation of circuit performance. Further, the use of

Ex. 2010 (Khatri Suppl. Decl.) ¶ 128

Saint Chapter 7 Teaches Away From A Common ESD Bus

Saint

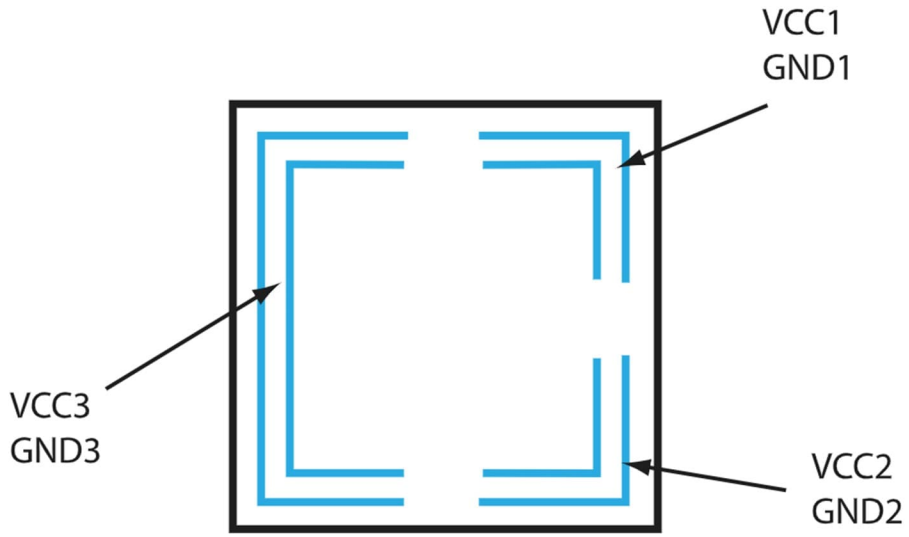


Figure 7–7. *Pin-out simplification showing like protects grouped together.*

Ex. 1008 (Saint), Fig. 7-7

Patent Owner Expert, Dr. Khatri

like the one Dr. Foty points to in Haralabidis. Connecting three separate signals together to a "common ESD ground" would drastically alter the electrical characteristics of the design and require other modifications as well. Such a modification would result in noise from one circuit being injected into another, which would result in a degradation of circuit performance. Further, the use of

Ex. 2010 (Khatri Suppl. Decl.) ¶ 128

Adding A Common ESD Bus Is Not A Suitable Option Because Saint Teaches Away

Millennium Pharms., Inc. v. Sandoz Inc.

The district court also clearly erred in its determination that lyophilizing bortezomib with mannitol to form an ester was a "suitable option from which the prior art did not teach away." Dist. Ct. Op. *7 (citing *Par Pharm.*, 773 F.3d at 1198). "A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant."

***Millennium Pharms., Inc. v. Sandoz Inc.*, 862 F.3d 1356, 1366 (Fed. Cir. 2017) (citations omitted)**

Unlike *Intel*, Petitioner's Change Defeats Saint Chapter 7's Purpose

Medtronic, Inc. v. Teleflex Innovations S.A.R.L.

In *Intel*, we rejected the Board's reasoning that a proposed rationale for modifying a circuit was insufficient because it "would have resulted in the circuit not being suitable for its intended purpose."[…] We did not hold, however, that a proposed modification's destruction of a device's primary purpose is always legally irrelevant to obviousness. Such a conclusion is equally at odds with common sense and gives in to the very hindsight bias the obviousness inquiry is designed to avoid. Indeed, we have held it was error for the Board to ignore evidence that a proposed modification would interfere with a reference's stated purpose.

***Medtronic, Inc. v. Teleflex Innovations S.A.R.L.*, 69 F.4th 1341, 1350 (Fed. Cir. 2023) (citations omitted)**

Unlike *Intel*, Petitioner's Change Defeats Saint Chapter 7's Purpose

Medtronic, Inc. v. Teleflex Innovations S.A.R.L.

Further, unlike in *Intel*, in which the reference contemplated use cases beyond the "intended purpose," the Board found Ressemann's "entire premise" was founded on the sealing devices Medtronic's proposed modifications would remove. We conclude the Board did not err in determining the destruction of Ressemann's entire purpose, shared with the challenged claims, was probative of whether Medtronic's modifications would have been obvious.

Medtronic, Inc. v. Teleflex Innovations S.A.R.L., 69 F.4th 1341, 1350 (Fed. Cir. 2023) (citations omitted)

Ground 3 Fails To Establish A Common ESD Bus Was Obvious For 3 Reasons

1 Saint Fig. 7-7 lacks a common ESD bus

2 Saint Fig. 7-7 teaches away from adding a common ESD bus

3 No motivation to add a common ESD Bus to Saint Fig. 7-7 in view of Case Study 1 or Haralabidis due to design differences

Institution Decision Understood Distinction Between Figure 7-7 And Case Study 1 And Haralabidis

Institution Decision

We find Patent Owner's arguments in this regard have merit on this record. As Patent Owner notes, Saint's Case Study 1 is directed to a design with a single GND signal, and Haralabidis is directed to a single GND signal that is segmented into three different reference potentials; neither includes multiple, separate GND signals as shown in Saint's Figure 7-7. Ex. 1008, 160–163, 344; Ex. 1007, 3:9–22, 3:34–40, 3:65–4:12; Ex. 1003 ¶¶ 359–360; Ex. 2007 ¶¶ 60, 62. In light of these disclosures in Saint and Haralabidis, we question whether a POSITA would have been motivated to apply Saint's "ESD Ground Wiring" or Haralabidis' common ground rail teachings to Saint's Figure 7-7 with a reasonable expectation of success.

Institution Decision 33-34

Institution Decision Recognized "merit" In Lack Of Motivation Argument

Institution Decision

We find Patent Owner's arguments in this regard have merit on this record. As Patent Owner notes, Saint's Case Study 1 is directed to a design with a single GND signal, and Haralabidis is directed to a single GND signal that is segmented into three different reference potentials; neither includes multiple, separate GND signals as shown in Saint's Figure 7-7. Ex. 1008, 160–163, 344; Ex. 1007, 3:9–22, 3:34–40, 3:65–4:12; Ex. 1003 ¶¶ 359–360; Ex. 2007 ¶¶ 60, 62. In light of these disclosures in Saint and Haralabidis, we question whether a POSITA would have been motivated to apply Saint's "ESD Ground Wiring" or Haralabidis' common ground rail teachings to Saint's Figure 7-7 with a reasonable expectation of success.

Institution Decision 33-34

Saint Case Study 1 Refers To A Single Ground With Separate VCC Rails

Saint

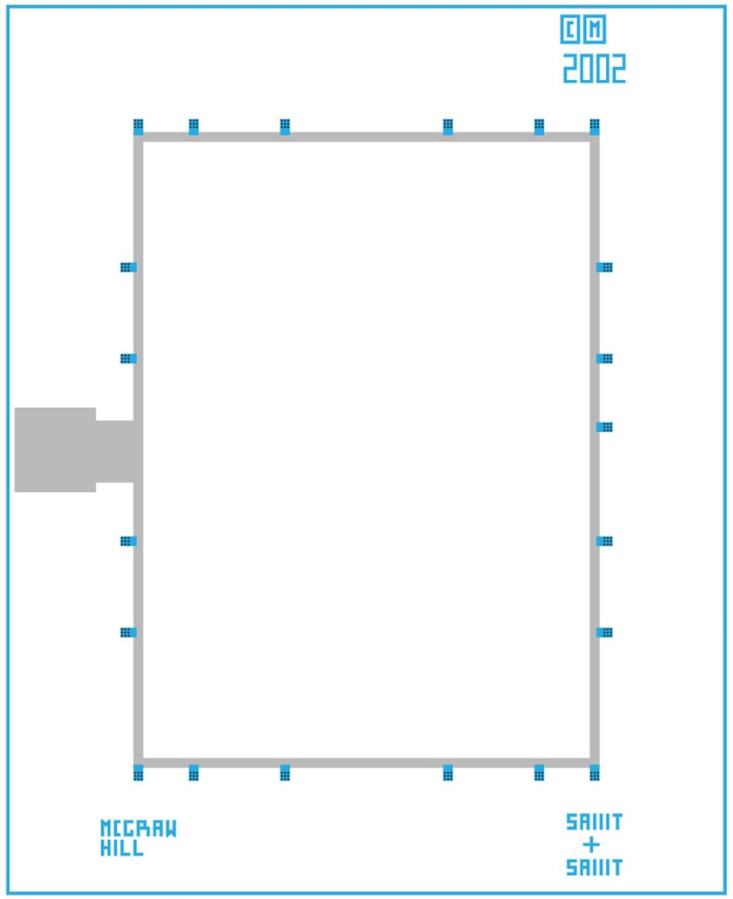


Figure CS1–99

Ex. 1008 (Saint), Fig. CS1-99

Petitioner's Expert, Dr. Foty

360. However, in the different design of the case study depicted (in part) on p. 344, Saint is *not* using the three-ground-rails (which provide three ESD buses) configuration of the Chapter 7 design – rather, Saint is using a *single* ground rail which provides a single ESD bus; this single ground rail – by providing a single ESD bus to which *all* of the anode-sides-connected-to-ground of the ESD protection circuit diodes are connected – provides the recited "common ESD bus" of claim element [1d].

Ex. 1003 (Foty Decl.) ¶ 360

Saint Case Study 1 Has A Common Ground Implemented In Segments

Saint

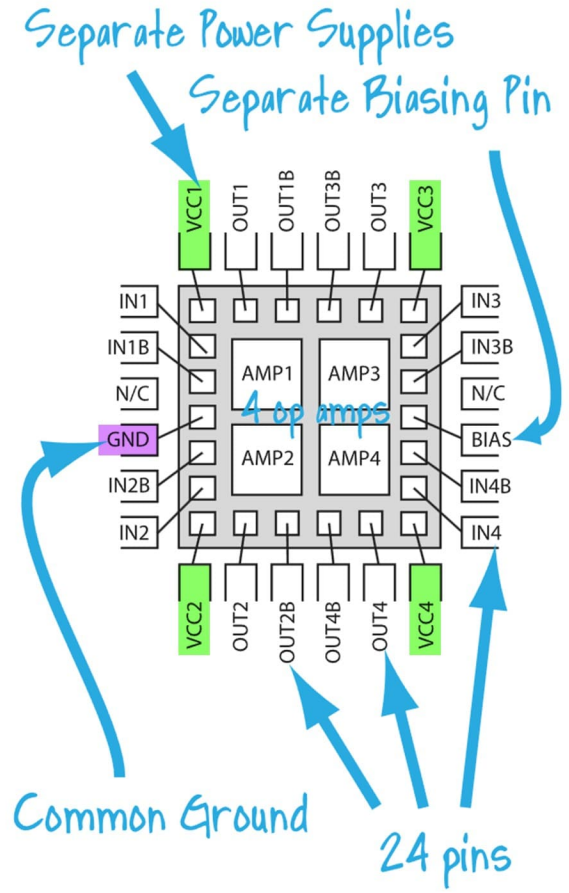


Figure CS1–1. Bond-out design using a 24-pin package.

Ex. 1008 (Saint), Fig. CS1-1

Saint

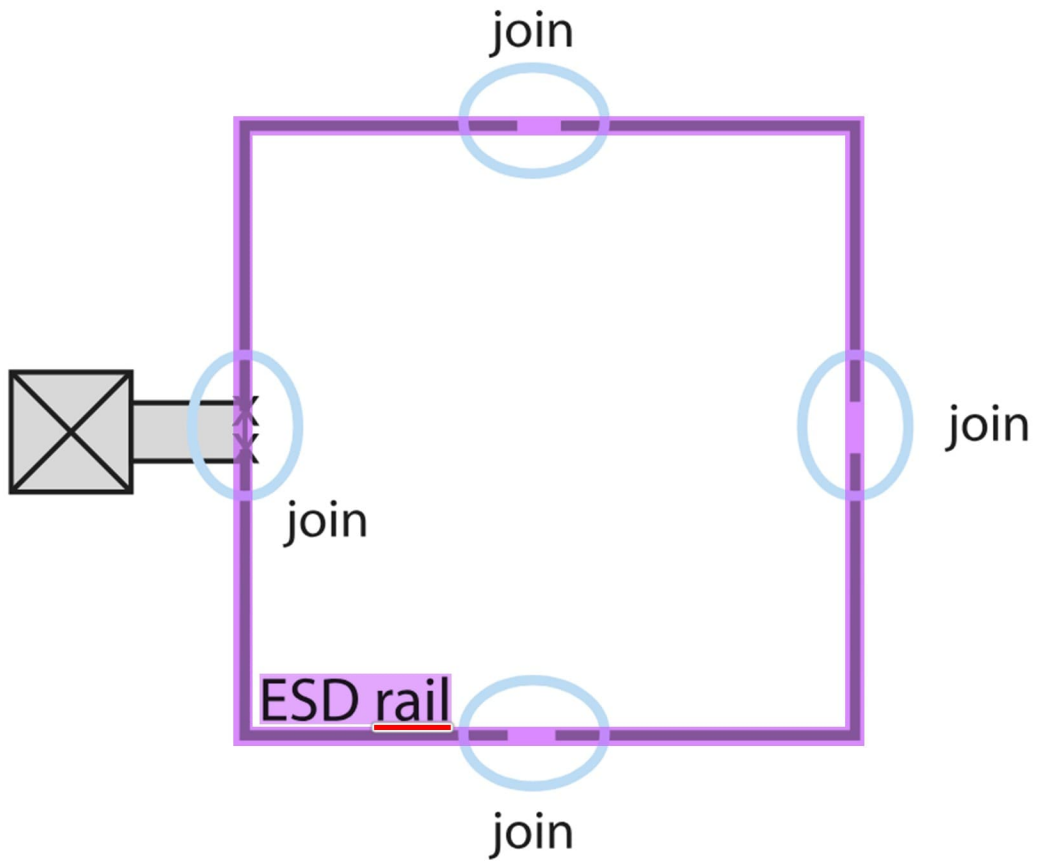


Figure CS1–87. *ESD ground wiring connections.*

Ex. 1008 (Saint), Fig. CS1-87

Case Study 1 And Figure 7-7 Fundamentally Differ

Saint

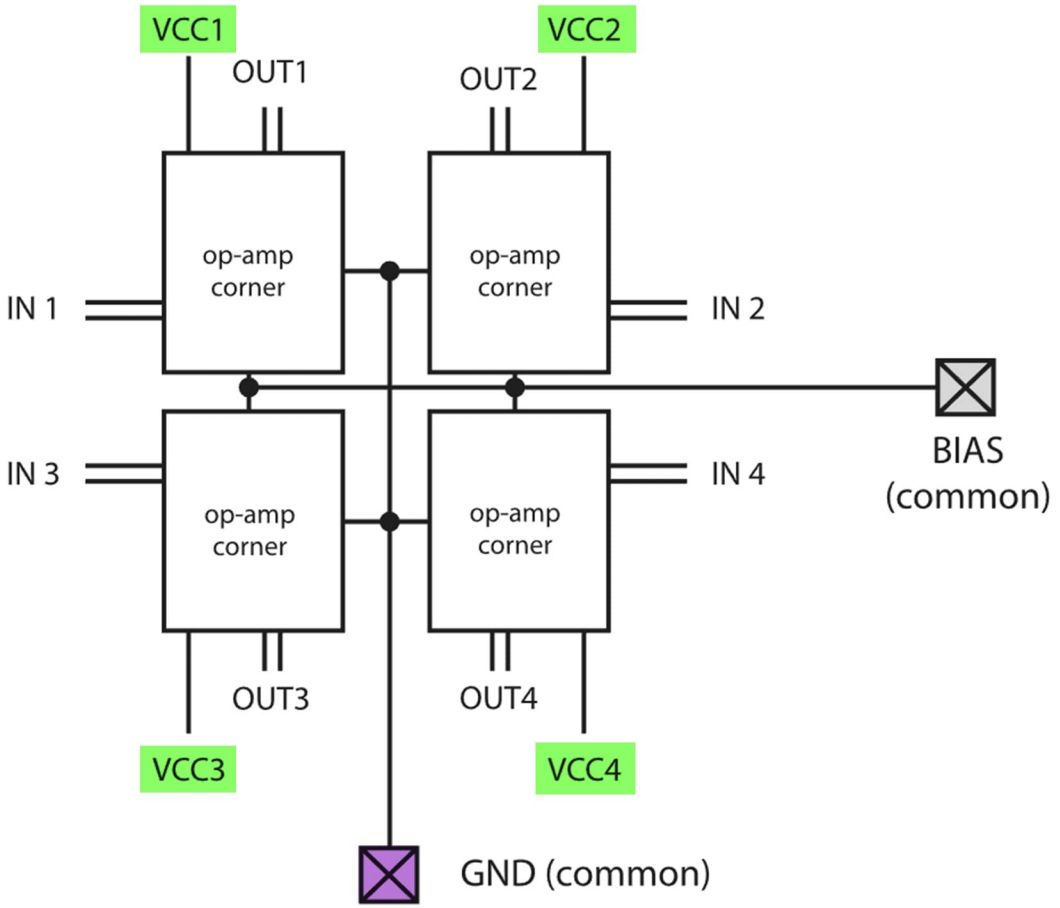


Figure CS1–84. Top level schematic.

Ex. 1008 (Saint), Fig. CS1-84

Saint

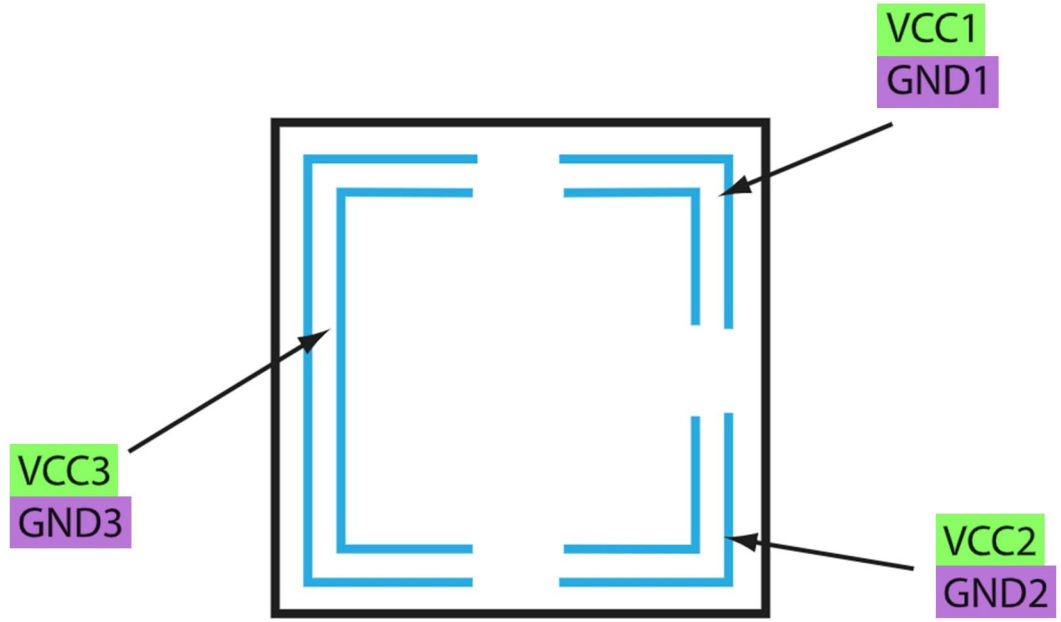


Figure 7–7. Pin-out simplification showing like protects grouped together.

Ex. 1008 (Saint), Fig. 7-7

Saint Case Study 1's Common ESD Bus Is Inapplicable To Saint Fig. 7-7

Saint

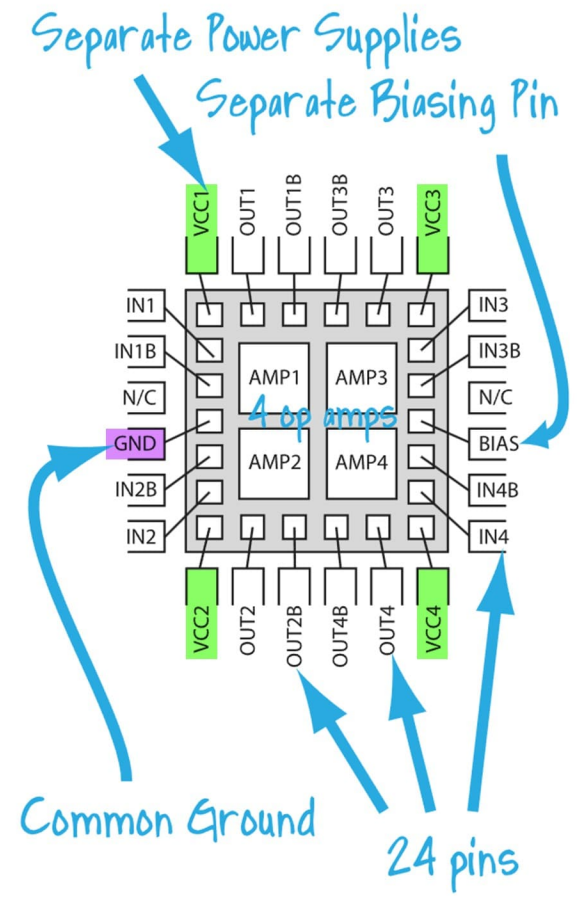


Figure CS1–1. Bond-out design using a 24-pin package.

Ex. 1008 (Saint), Fig. CS-1

Patent Owner Expert, Dr. Khatri

Saint and walks through the design of a specific CMOS amplifier circuit. Saint does not say that the specific example of Case Study 1 can be generally applicable to all designs of Saint, let alone that it is applicable to Figure 7-7. In fact, this "single ground rail" is not applicable in general, and not applicable to Figure 7-7 in particular. Regardless, the exemplary CMOS amplifier design of Case Study 1 includes only one "GND" signal. Saint, 249, 250 and 261 (CS1-

Ex. 2010 (Khatri Suppl. Decl.) ¶ 127

Haralabidis Includes A Single Segmented Ground Signal

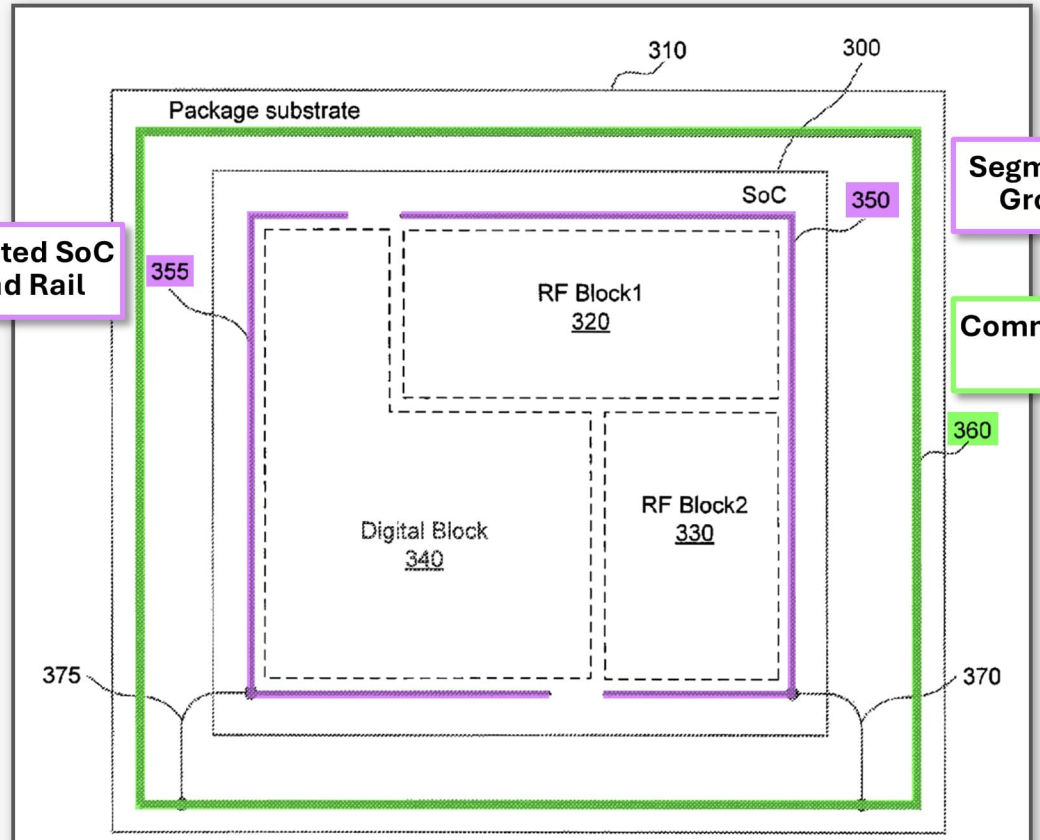


FIG. 3
Conventional Art

Ex. 1007 (Haralabidis), Fig. 3

Segmented SoC Ground Rail

Segmented SoC Ground Rail

Common Ground Rail

Haralabidis

SoC 100. The package substrate **310** includes a package common ground rail **360**, and the segmented SoC ground rails **350, 355** are independently connected to the package common ground rail **360** via separate connections **370, 375** respectively.

Ex. 1007 (Haralabidis), 3:14-18

Haralabidis Includes A Single Segmented Ground Signal

Haralabidis

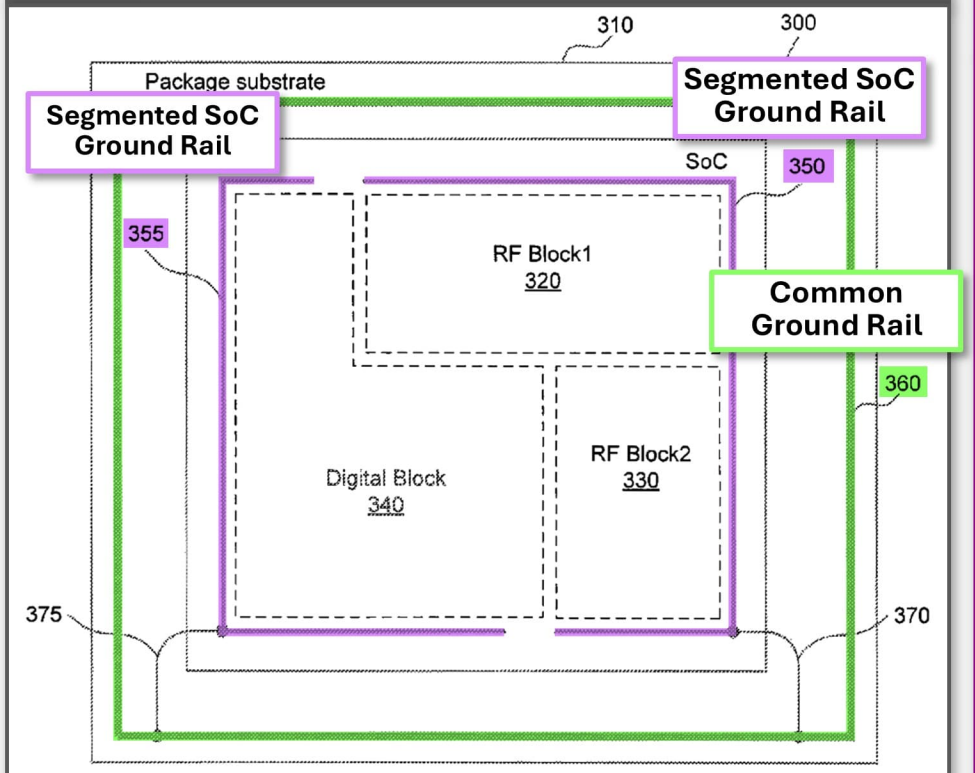


FIG. 3
Conventional Art

Ex. 1007 (Haralabidis), Fig. 3

Patent Owner Expert, Dr. Khatri

129. Similarly, Haralabidis teaches the use of a "common ground rail" to connect "segmented ground rails." Haralabidis, 3:9-22, 3:34-40, 3:65-4:12. A POSITA would understand "segmented ground rails" to refer to a single ground signal that has been "segmented." That is fundamentally different from the design of Saint's Figure 7-7 that Dr. Foty relies on, which uses three *different* ground signals, GND1, GND2, and GND3—not a single ground signal that has been "segmented." Because of that, a POSITA would not have been

Ex. 2010 (Khatri Suppl. Decl.) ¶ 129

Haralabidis Includes A Single Segmented Ground Signal

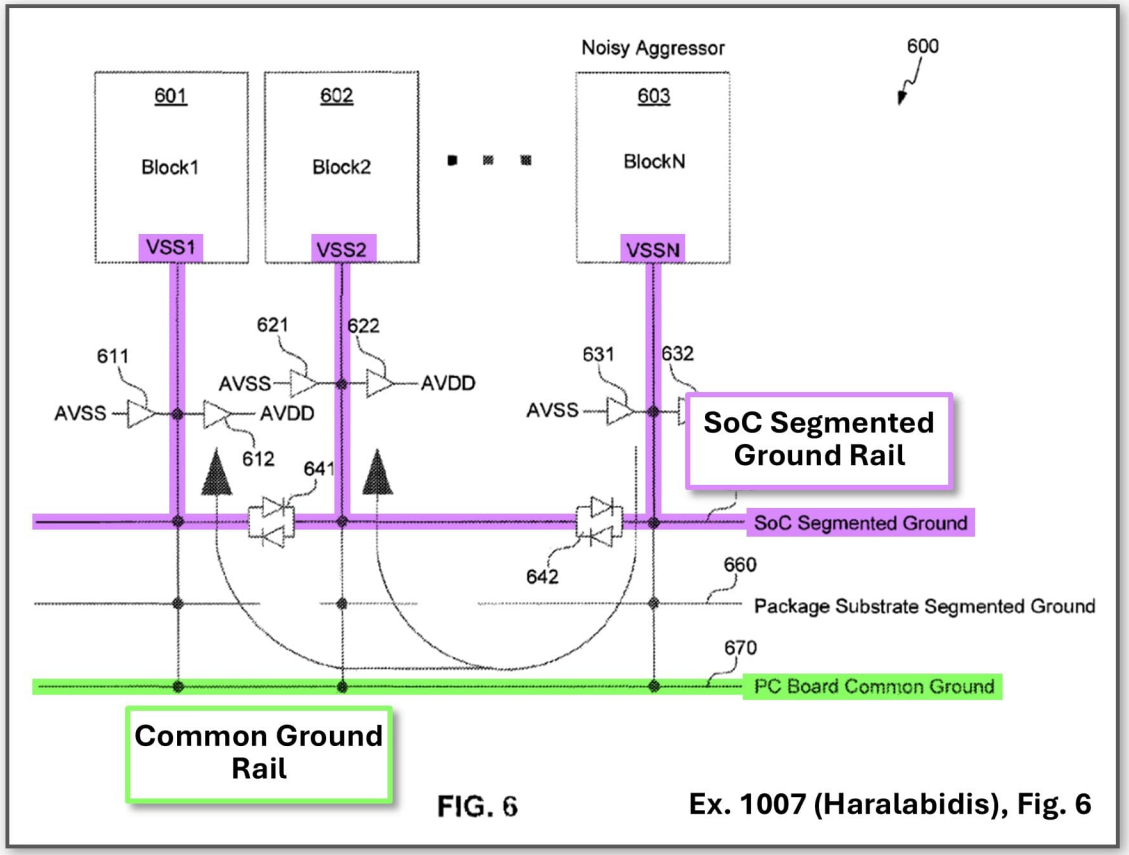


FIG. 6

Ex. 1007 (Haralabidis), Fig. 6

Haralabidis

vided with (ESD) protection diodes **631**, **632**. Further, each ground connection VSS1, VSS2, VSSN is connected to its respective SoC segmented ground rail **650**, to its respective segmented package ground rail **660**, and to the PC board common ground rail **670**. The individual ground connections

Ex. 1007 (Haralabidis), 5:49-53

Haralabidis Is Fundamentally Different From Saint Fig. 7-7

Patent Owner Expert, Dr. Khatri

129. Similarly, Haralabidis teaches the use of a "common ground rail" to connect "segmented ground rails." Haralabidis, 3:9-22, 3:34-40, 3:65-4:12. A POSITA would understand "segmented ground rails" to refer to a single ground signal that has been "segmented." That is fundamentally different from the design of Saint's Figure 7-7 that Dr. Foty relies on, which uses three *different* ground signals, GND1, GND2, and GND3—not a single ground signal that has been "segmented." Because of that, a POSITA would not have been

Ex. 2010 (Khatri Suppl. Decl.) ¶ 129

Ground 3 Fails To Establish A Common ESD Bus Was Obvious For 3 Reasons

1. Saint Fig. 7-7 lacks a common ESD bus
2. Saint Fig. 7-7 teaches away from adding a common ESD bus
3. No motivation to add a common ESD Bus to Saint Fig. 7-7 in view of Case Study 1 or Haralabidis due to design differences

Appendix

Independent Claims

1. An integrated circuit structure, comprising:
a circuit area;
a plurality of ESD buses;
a plurality of pad groups, adjacent and connected to the plurality of ESD buses;
a common ESD bus, adjacent to the plurality of pad groups; and
a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus;
wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

Ex. 1001 ('164 Patent), Claim 1

6. An integrated circuit structure, comprising:
a circuit area;
a plurality of ESD buses;
a plurality of pad groups, adjacent and connected to the plurality of ESD buses; and
a plurality of bonding wires configured to connect one to another of the plurality of pad groups;
wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

Ex. 1001 ('164 Patent), Claim 6

Independent Claims

8. A method of integrated circuit structure, comprising:
forming a circuit area;
forming a plurality of ESD buses;
forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses;
forming a common ESD bus adjacent to the plurality of pad groups; and
connecting a plurality of pads corresponding to the plurality of pad groups to the common ESD bus by a plurality of bonding wires;
wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

Ex. 1001 ('164 Patent), Claim 8

12. A method of integrated circuit structure, comprising:
forming a circuit area;
forming a plurality of ESD buses;
forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses; and
connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires across the circuit area;
wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

Ex. 1001 ('164 Patent), Claim 12