

Micron Technology, Inc.
Petitioner
v.
Yangtze Memory Technologies Company, Ltd.
Patent Owner

Case No. IPR2025-00118
U.S. Patent No. 10,879,164

Petitioner's Hearing Demonstratives

March 12, 2025

Roadmap

- I. [Introduction and IPR Grounds](#)
- II. [Overview of the '164 Patent and Prior Art](#)
- III. [Pad Assignment & ESD Bus Disputes](#)
- IV. [Bond Wire Disputes](#)
- V. [Saved Area](#)

Roadmap

- I. Introduction and IPR Grounds
- II. Overview of the '164 Patent and Prior Art
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- V. Saved Area

Instituted Grounds

Ground	Prior Art	Claims
1	Yoshinaga + Saint	6-7, 12, and 14 are obvious
2	Yoshinaga + Saint + Haralabidis	1-6, 8-11, and 13 are obvious
3	Saint + Haralabidis	1-14 are obvious

Petition, 7-8.

The “Saved Area” was the Purported Point of Novelty

The file history makes clear that the *saved area* limitation resulted in allowance. Pet. 17-18 (citing EX1002, 216-218, 230-233). Saint (and Yoshinaga) plainly disclose *saved area[s]*. Saint, Fig. 9-28 (left); Yoshinaga, Fig. 6 (right). Saint expressly teaches placing circuitry in “wasted spaced” (orange areas) “between the [bond] pads” (blue) to “get the chip as small as possible.” Saint, 220-221.

Reply, 1
See also Petition 1-2, 17-18

Saint (left) and Yoshinaga (right) Both Discloses a “Saved Area” (orange)

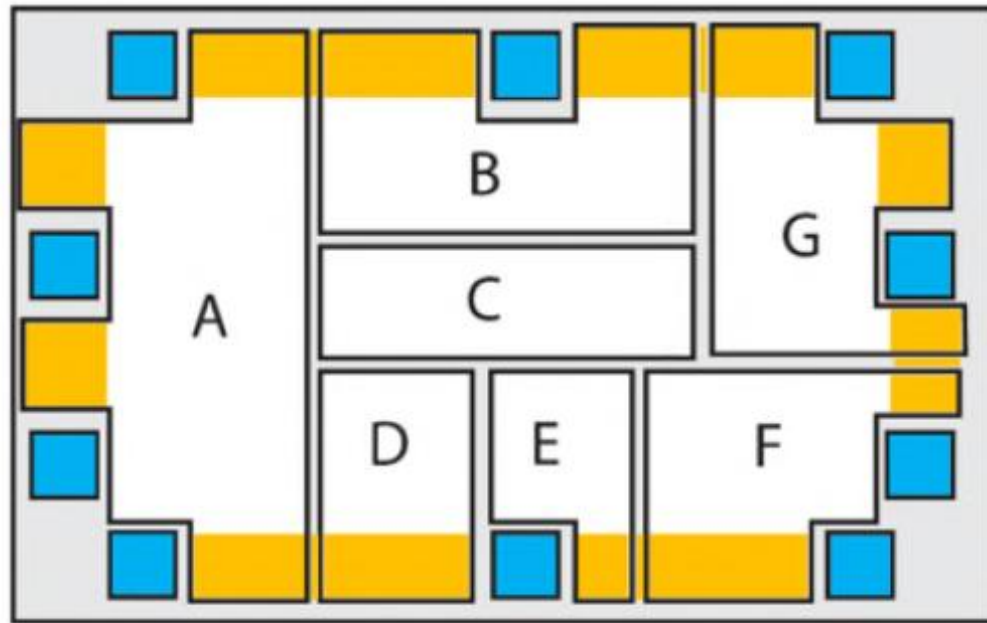
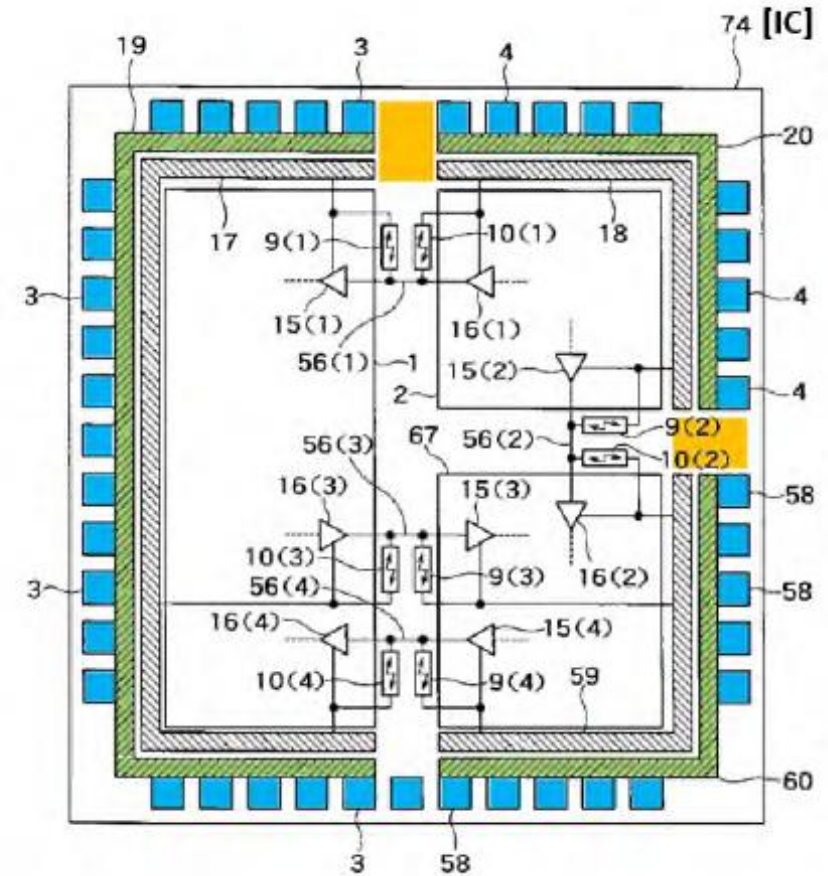


Figure 9-28. We can use extra space surrounding our pads to shrink our chip size.



Reply, 1; see also Petition 1-2

VIII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the field of the '164 Patent would have had a bachelor of science degree in electrical engineering or similar discipline, and 2-3 years of professional experience working with (*e.g.*, researching, analyzing, designing, or teaching) ICs, or equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience and vice versa). This POSITA would have been aware of and generally knowledgeable about IC design, layout, manufacturing, packaging, and ESD protection. *See* Foty, ¶¶ 29-33.

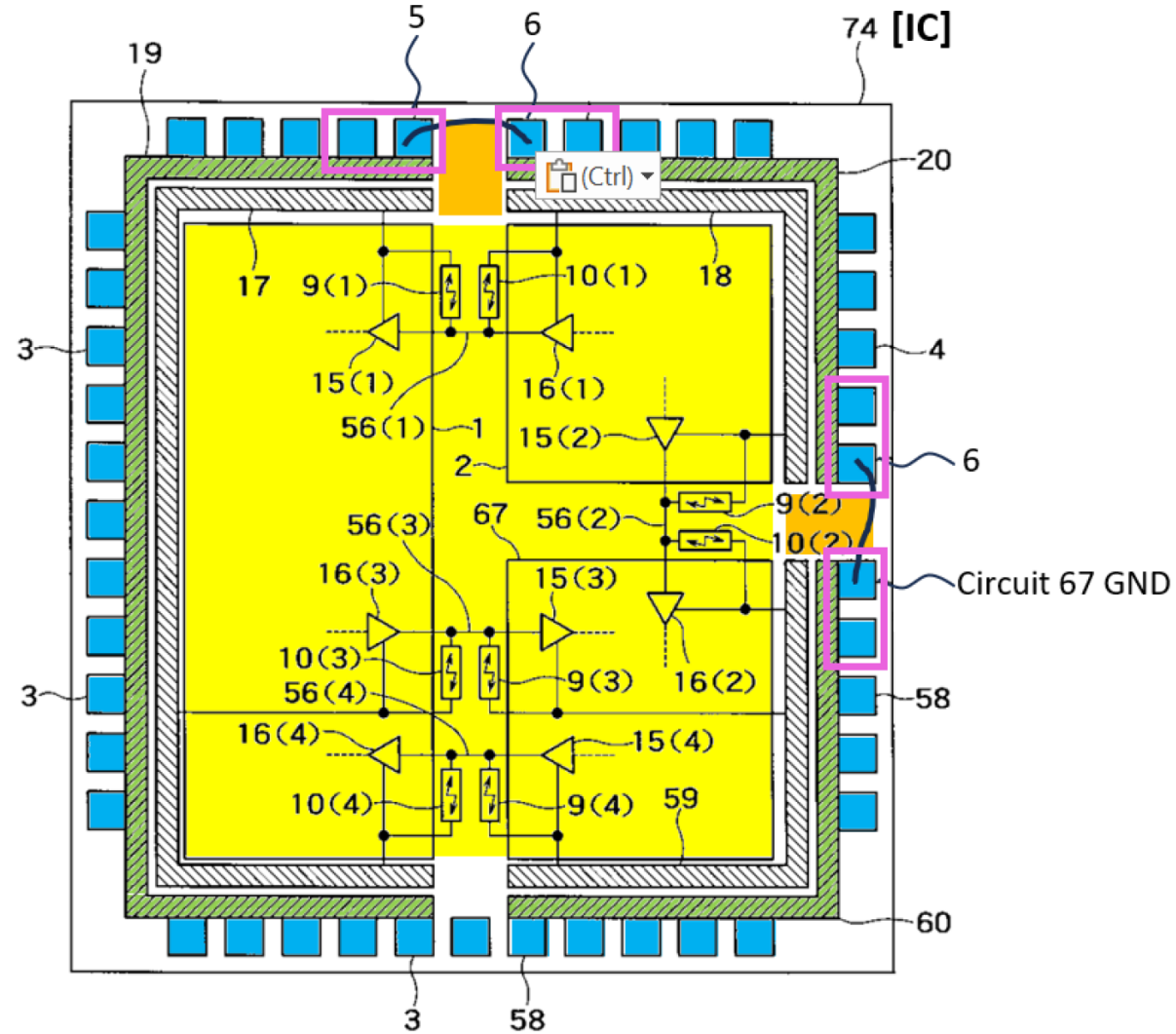
Level of Skill in the Art is Undisputed

C. Person of Ordinary Skill in the Art

Patent Owner does not dispute Petitioner's proposed level of a person of ordinary skill in the art ("POSITA") for purposes of this IPR.² Pet. 27. Regardless of the precise definition of a POSITA, Petitioner's grounds do not render any challenged claims unpatentable.

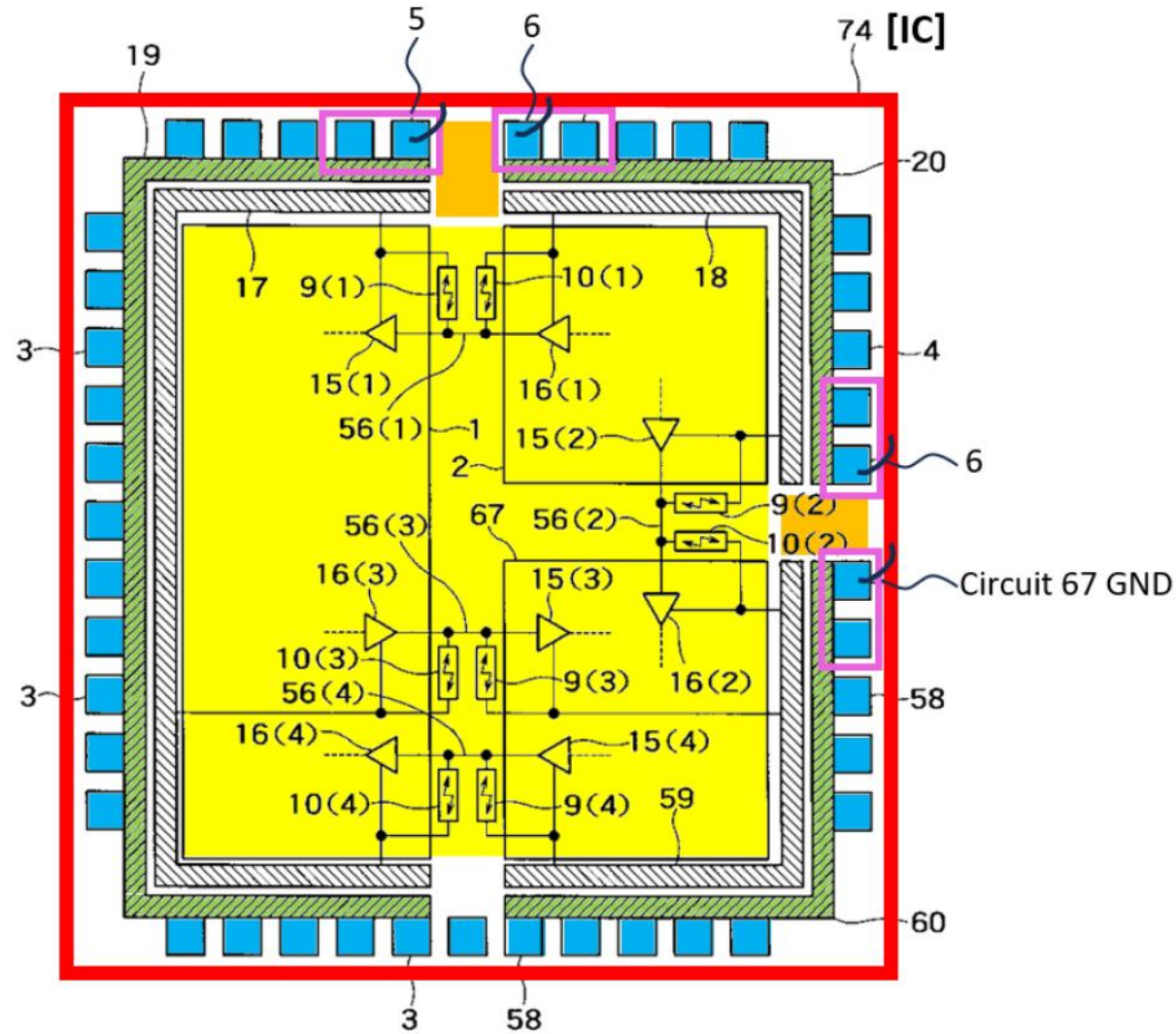
POR, 10

Ground 1 (Independent Claims 6 and 12)



Yoshinaga, Fig. 6 (annotated)
Petition, 36

Ground 2 (Independent Claims 1 and 8)



Yoshinaga, Fig. 6 (annotated)
Petition, 56

Ground 3 (Independent Claims 1 and 8)

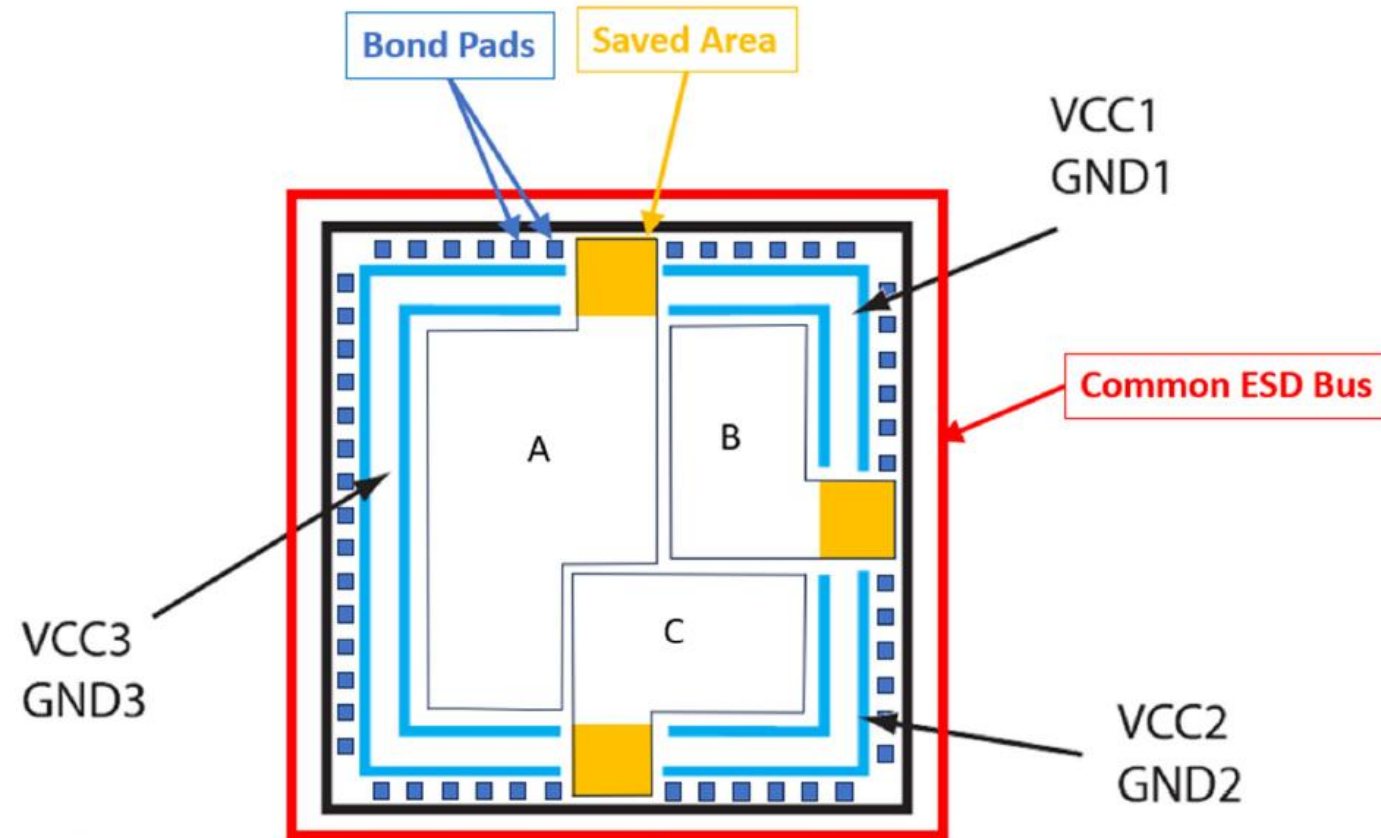


Figure 7-7. Pin-out simplification showing like protects grouped together.

*Saint, Fig. 7-7 (annotated)
Petition, 83*

Roadmap

- I. Introduction and IPR Grounds
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- III. Pad Assignment & ESD Bus Disputes
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Overview of the '164 Patent



US010879164B2

(12) **United States Patent**
Li

(10) **Patent No.:** US 10,879,164 B2
(45) **Date of Patent:** Dec. 29, 2020

(54) INTEGRATED CIRCUIT ELECTROSTATIC DISCHARGE BUS STRUCTURE AND RELATED METHOD

(56) **References Cited**

U.S. PATENT DOCUMENTS

(71) Applicant: **Yangtze Memory Technologies Co., Ltd.**, Wuhan (CN)

(72) Inventor: **Zhiguo Li**, Wuhan (CN)

(73) Assignee: **Yangtze Memory Technologies Co., Ltd.**, Wuhan (CN)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 30 days.

5,347,150	A *	9/1994	Sakai	H01L 27/0218	257/203
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7,129,574	B2 *	10/2006	Wu	H01L 23/50	257/355
7,692,247	B2 *	4/2010	Woo	H01F 17/0006	257/355

2014/0061881 A1 3/2014 Yeh

FOREIGN PATENT DOCUMENTS

(21) Appl. No.: 16/207,183

(22) Filed: Dec. 2, 2018

(65) **Prior Publication Data**

US 2020/0144174 A1 May 7, 2020

Related U.S. Application Data

(63) Continuation of application No. PCT/CN2018/113271, filed on Nov. 1, 2018.

CN	101097304	A	1/2008
CN	101221629	A	7/2008
CN	102054523	A	5/2011
CN	101097304	B	7/2011
CN	103000625	A	3/2013
CN	103681654	A	3/2014
KR	20020034470	A	5/2002
TW	201737459	A	10/2017
WO	0028664	A3	7/2001

* cited by examiner

(51) Int. Cl.
H01L 23/52 (2006.01)
H01L 23/50 (2006.01)
H01L 23/49 (2006.01)
H01L 27/02 (2006.01)

Primary Examiner — S. V. Clark
(74) Attorney, Agent, or Firm — Winston Hsu

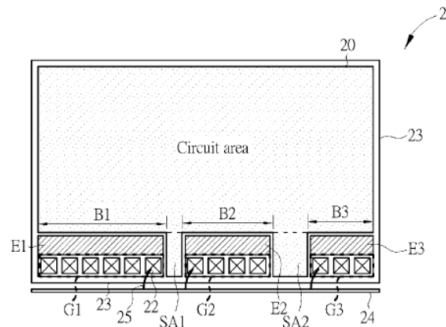
(57) **ABSTRACT**

An integrated circuit ESD bus structure includes a circuit area; a plurality of electrostatic discharge (ESD) buses; a plurality of pad groups adjacent and connected to the plurality of ESD buses; a common ESD bus; and a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus.

(52) U.S. Cl.
CPC *H01L 23/50* (2013.01); *H01L 23/49*
(2013.01); *H01L 27/0248* (2013.01)

(58) **Field of Classification Search**
CPC H01L 23/50; H01L 23/60; H01L 2924/14;
H01L 24/06; H01L 27/0292; H01L 23/62
USPC 257/691, 784; 438/106
See application file for complete search history.

14 Claims, 3 Drawing Sheets



- **U.S. Pat. 10,879,164**
- **Titled** "Integrated Circuit Electrostatic Discharge Bus Structure and Related Method"
- **Priority Date:** November 1, 2018
- Discloses an "integrated circuit structure" including a "circuit area," "ESD bus" structure, and "saved area" where the saved area is part of the integrated circuit's circuit area.

Ex. 1001 (164 Patent).

Overview of the '164 Patent

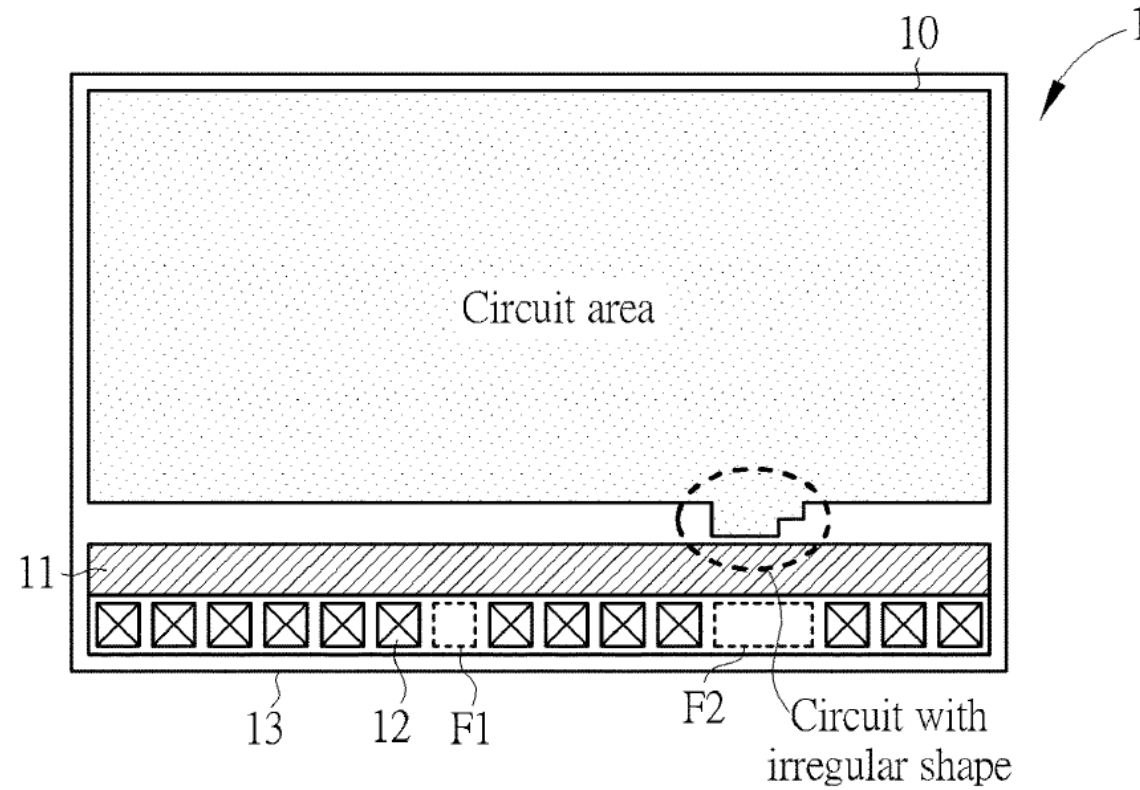


FIG. 1 PRIOR ART

*Ex. 1001 ('164 Patent), Fig. 1
Petition, 15*

Overview of the '164 Patent

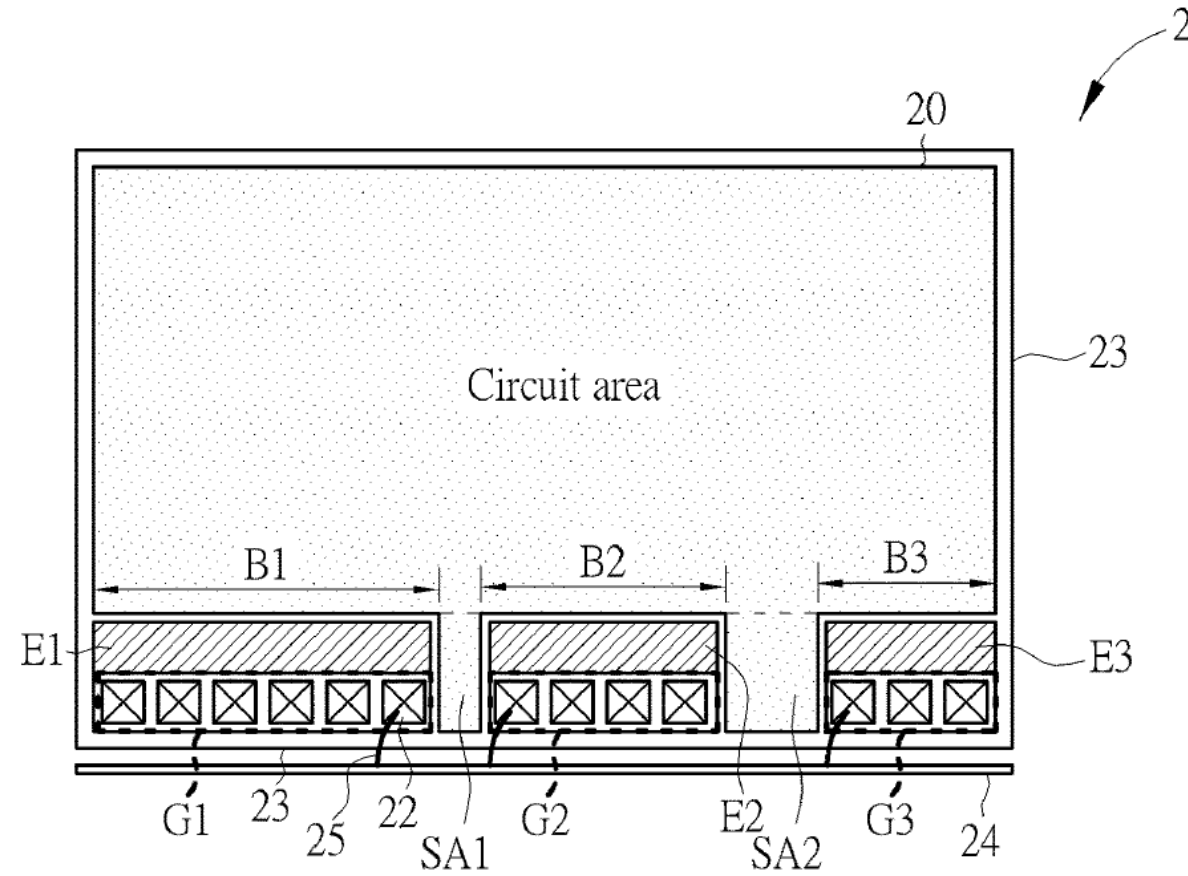


FIG. 2

Ex. 1001 ('164 Patent), Fig. 2
Petition, 17

Overview of the '164 Patent

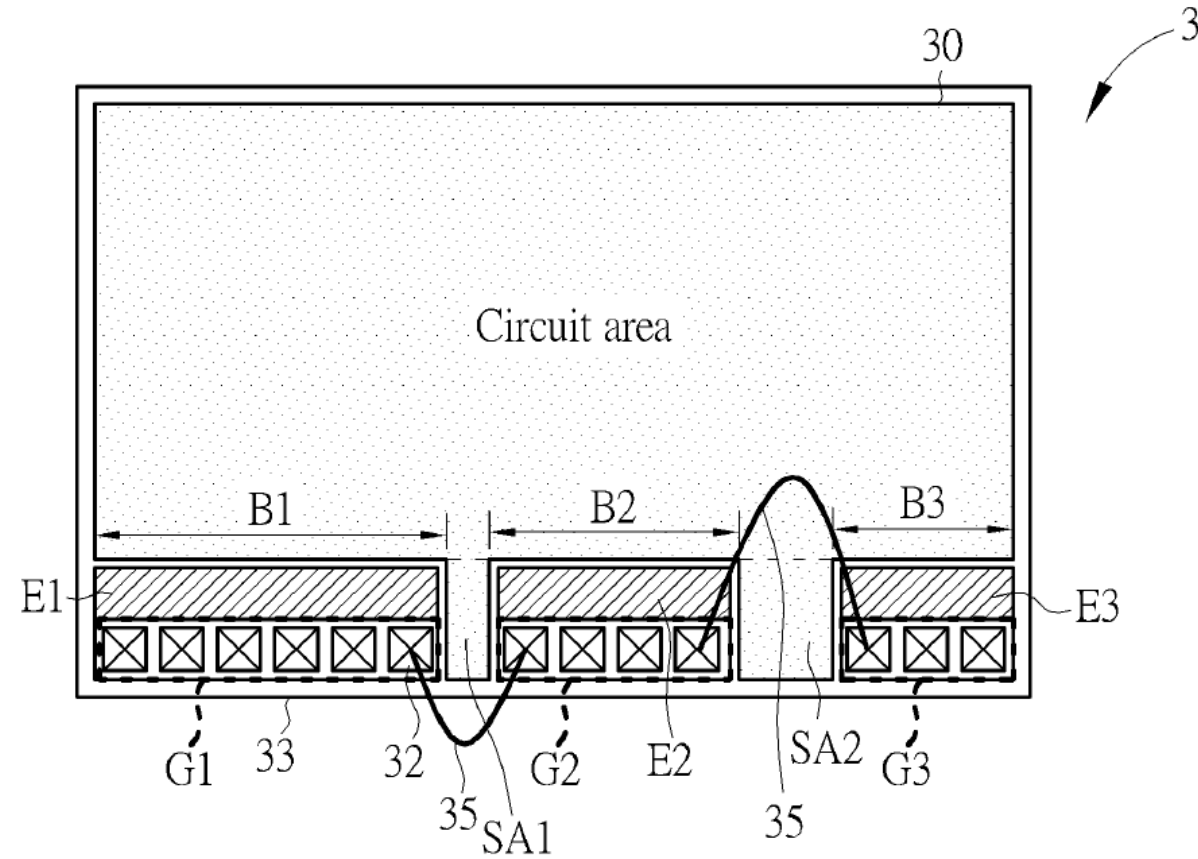


FIG. 3

Ex. 1001 ('164 Patent), Fig. 3
Petition, 16

Claim 6 of the '164 Patent

6. An integrated circuit structure, comprising:

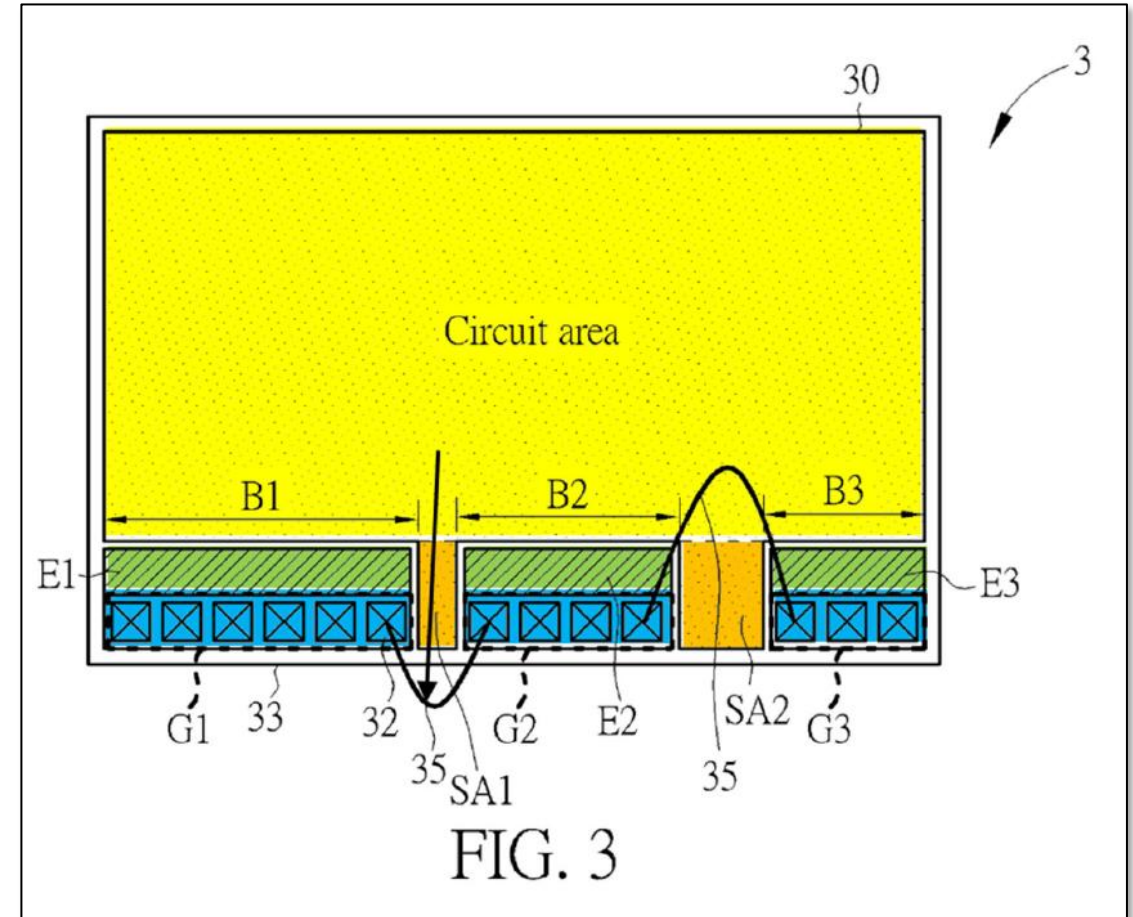
a circuit area;

a plurality of ESD buses;

a plurality of pad groups, adjacent and connected to the plurality of ESD buses; and

a plurality of bonding wires configured to connect one to another of the plurality of pad groups;

wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.



Ex. 1001 (164 Patent), Claim 1, Fig. 2
Petition, xi, 14-17

Claim 1 of the '164 Patent

1. An integrated circuit structure, comprising:

a circuit area;

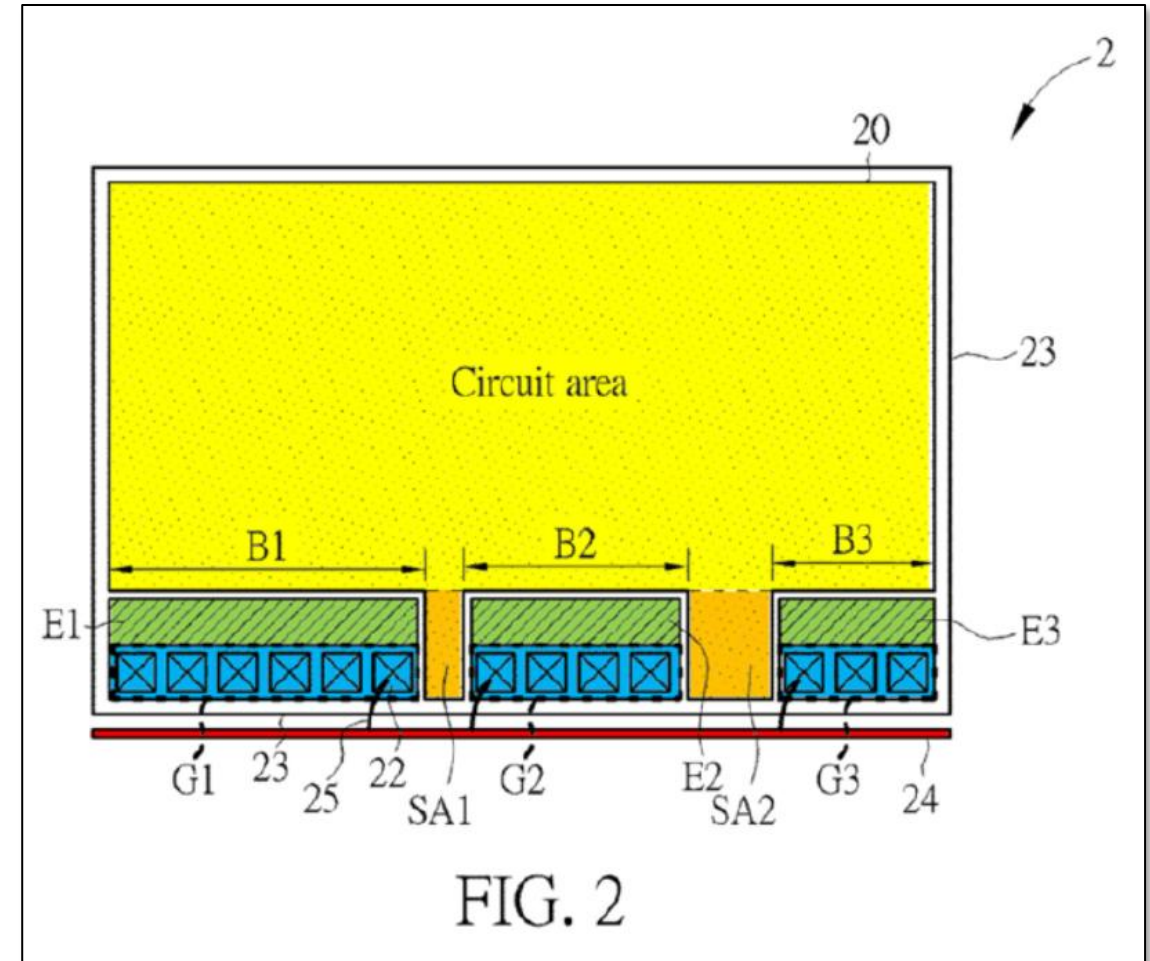
a plurality of ESD buses;

a plurality of pad groups, adjacent and connected to the plurality of ESD buses;

a common ESD bus, adjacent to the plurality of pad groups; and

a plurality of bonding wires configured to connect the plurality of pad groups to the common ESD bus;

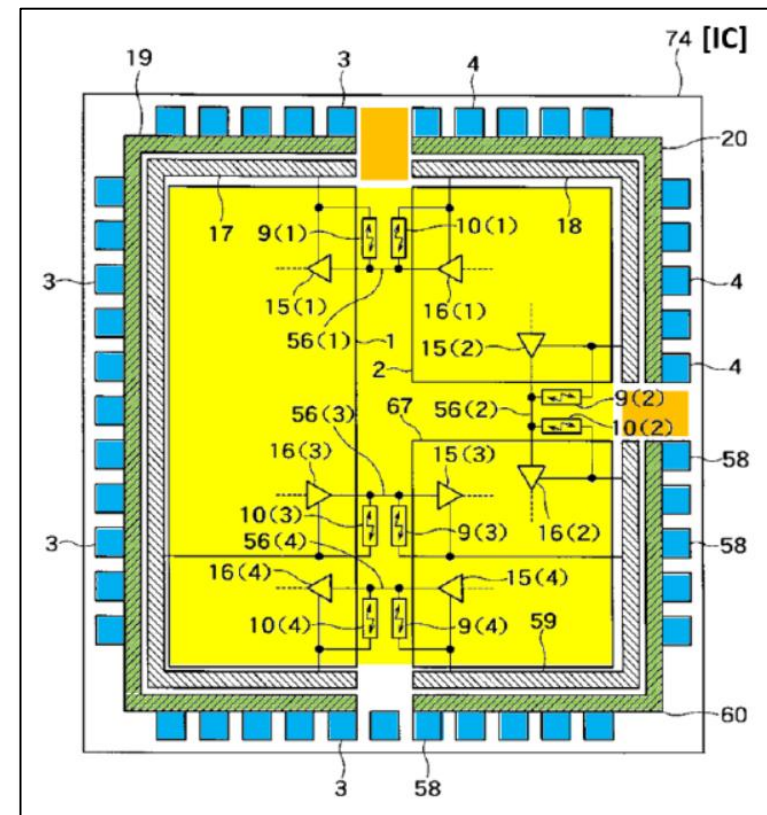
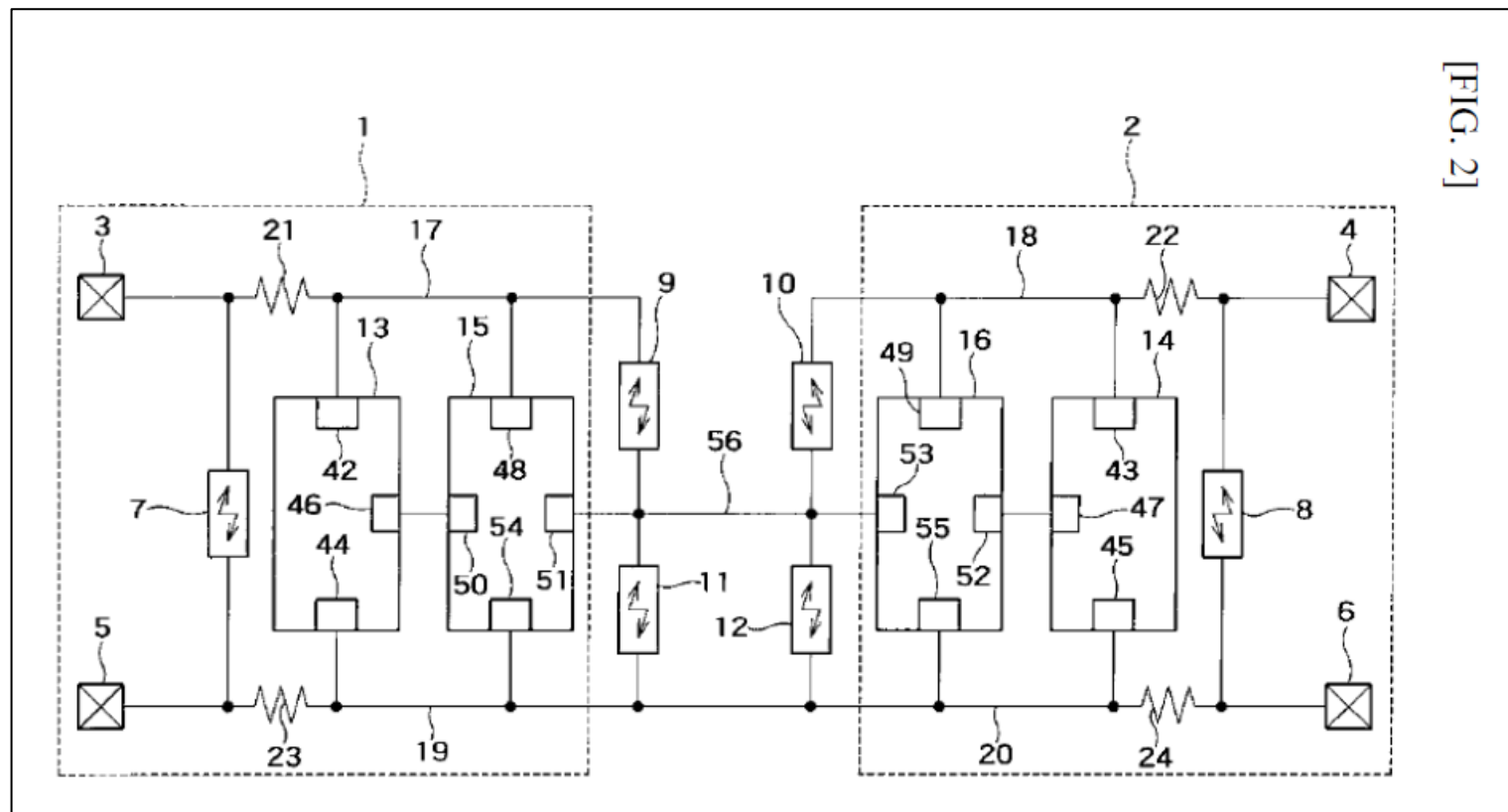
wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.



Ex. 1001 (164 Patent), Claim 1, Fig. 2
Petition, xi, 14-17

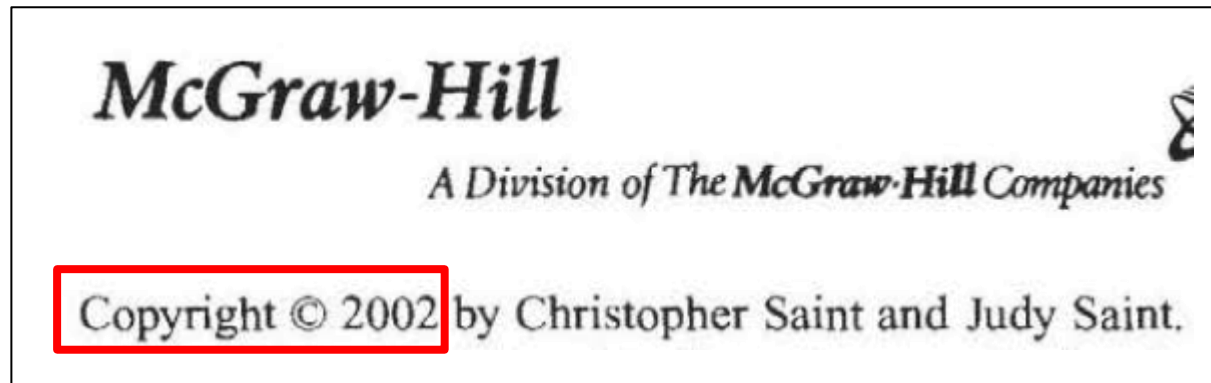
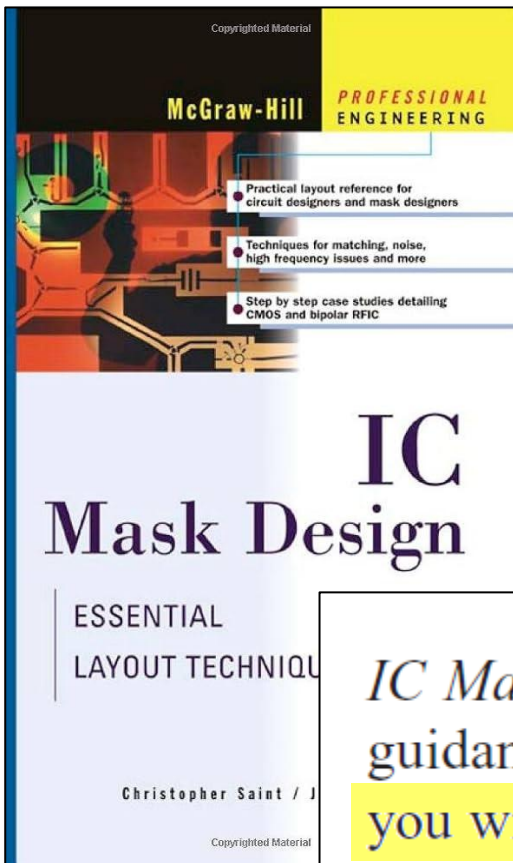
Overview of Yoshinaga (Grounds 1 and 2)

- Yoshinaga discloses “[ESD] protection circuit[ry]” in an integrated circuit, as Figs. 2 and 6 show:



Ex. 1006 (Yoshinaga), Figs. 2 and 6 (annotated)
Petition, 19-23, 35

Overview of Saint (Grounds 1-3)



Ex. 1008 (Saint), 4
Petition , 25

IC Mask Design: Essential Layout Techniques provides step-by-step detailed guidance on every aspect of the mask design process, including techniques you will use on a daily basis.

Ex. 1008 (Saint), 13
Institution Decision, 11

Overview of Saint (Grounds 1-3)

- The Saint textbook describes “development of superior integrated circuits,” including pinout, bond wires, ESD protection, and layout to maximize circuit area

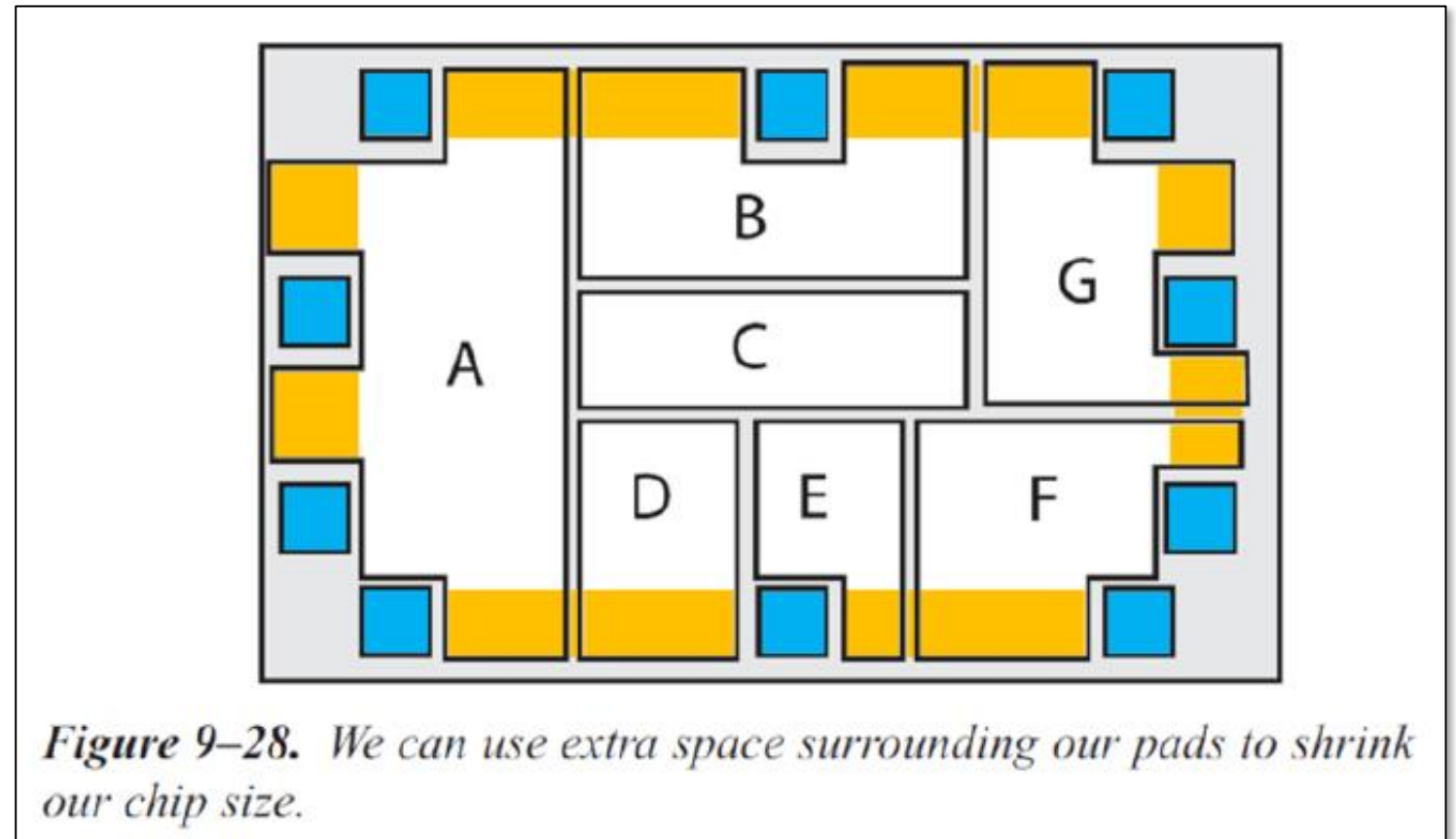
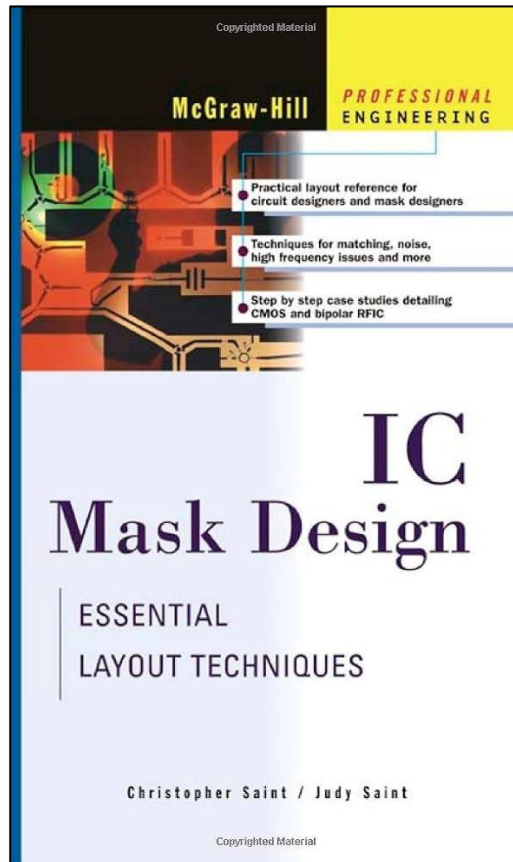


Figure 9–28. We can use extra space surrounding our pads to shrink our chip size.

Ex. 1008 (Saint), 220-221, Fig. 9-28 (annotated)
Petition, 25-26

Overview of Haralabidis (Grounds 2 and 3)

- Haralabidis discloses “Electrostatic Discharge Protection and Noise Suppression in Circuits” using segmented ground rails wirebonded to a common ground rail

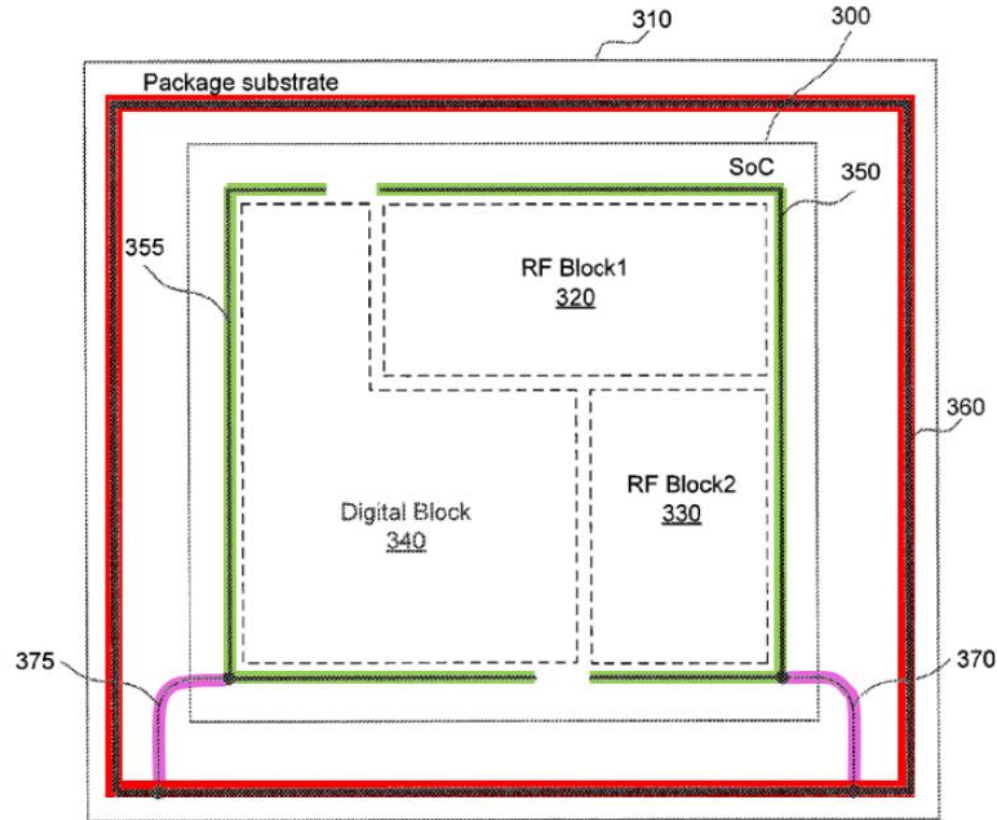


FIG. 3
Conventional Art

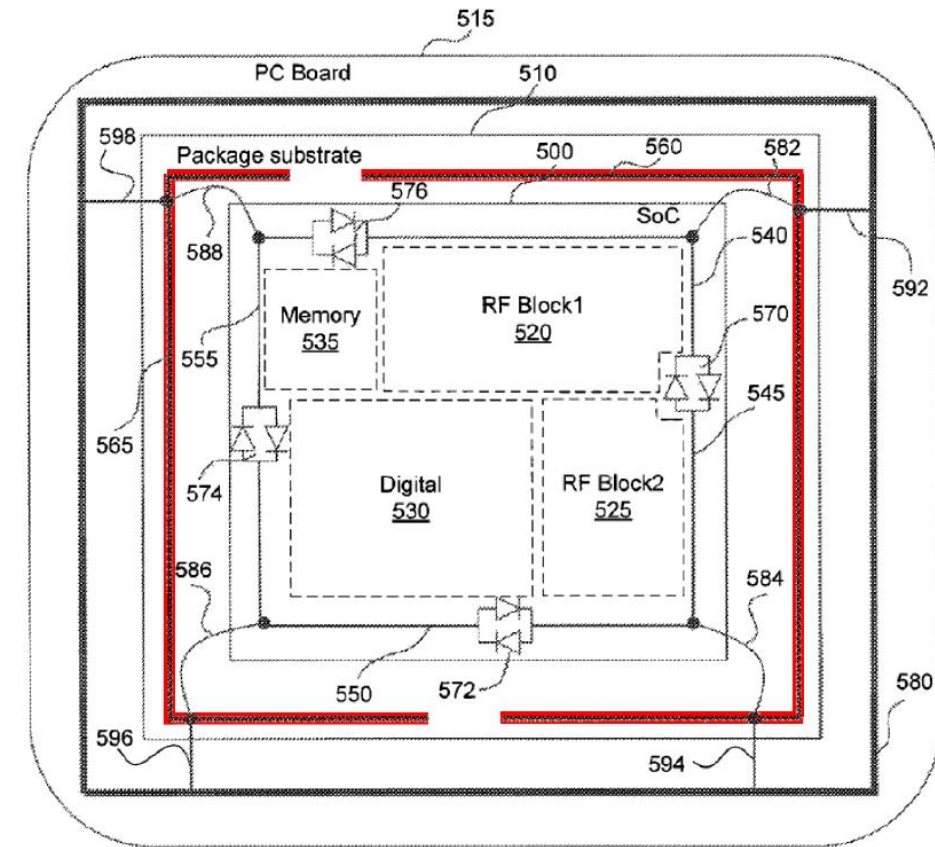
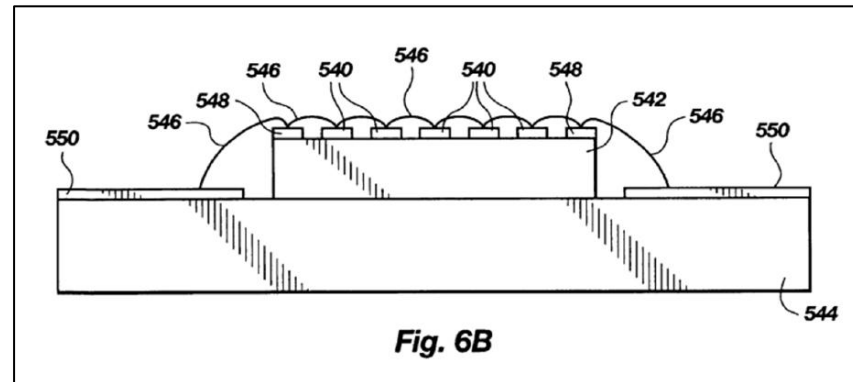
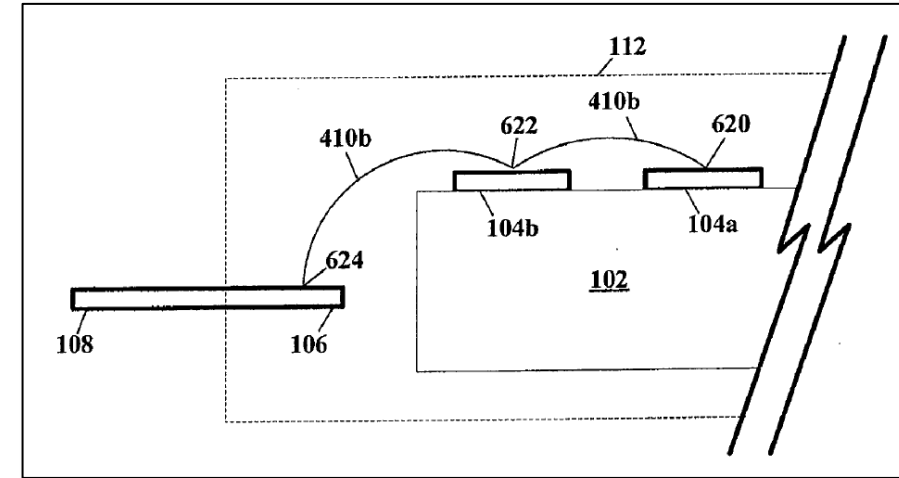
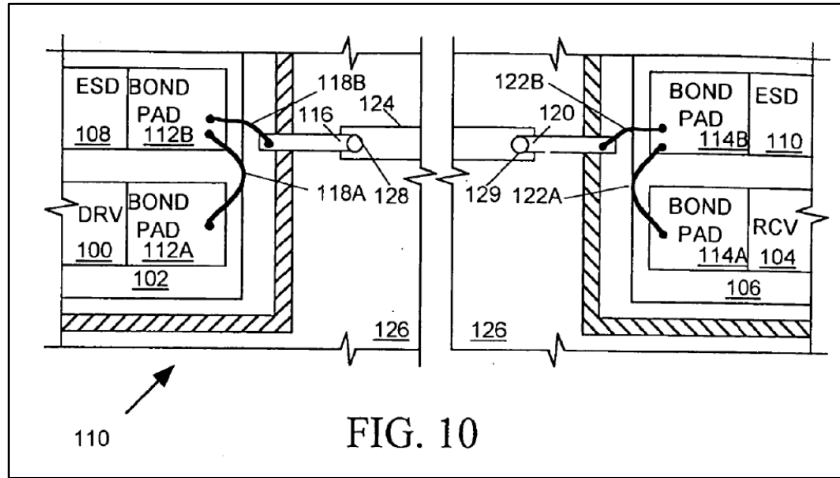


FIG. 5

Ex. 1007 (Haralabidis), Figs. 3 and 5 (annotated)
Petition, 23-25, 61, 79

Overview of Bond Wire References

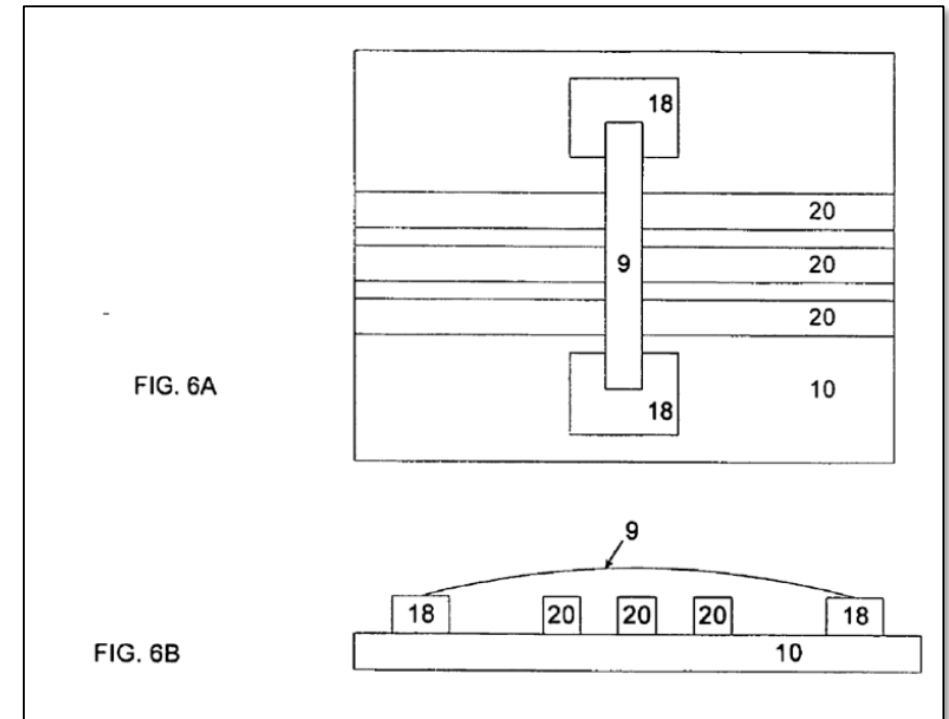
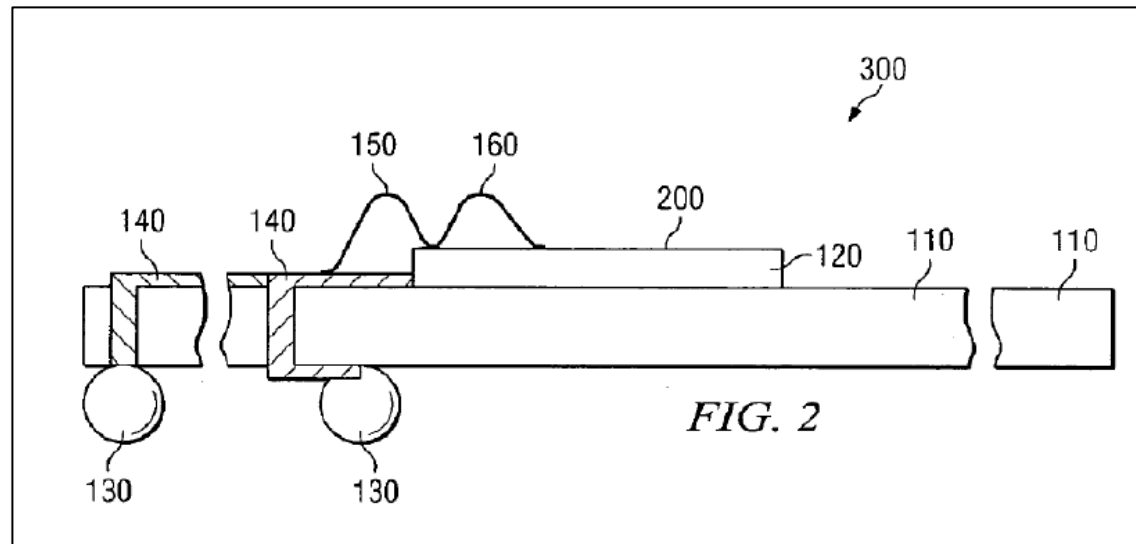
- Miller, Mathew, Beauchamp, Ball, Lee, Conner, and Beddingfield all discuss wire bonding



Ex. 1014 (Miller) Fig. 10 (left); Ex. 1016 (Beauchamp) Fig. 6 (right), Ex. 1020 (Ball) Fig. 6B (bottom)
Petition, 36-39, 88

Overview of Bond Wire References

- Miller, Mathew, Beauchamp, Ball, Lee, Conner, and Beddingfield all discuss wire bonding



Ex. 1041 (Beddingfield) Fig. 2, Ex. 1040 (Conner) Fig. 6
Reply, 6-8

Jumper Bond Wire Connections were Well-Known and Common

- “The ***contact pads are linked to one another and to the IC I/O terminal though inductive conductors such as bond wires***, metalization layer traces in the IC” (Miller (Ex. 1014), Abstract)
- “[V]arious embodiments may utilize ***many different wire-bonding patterns. ... [S]ome wires 50 are used to directly connect two conductive elements 40.*** Such wires may reduce a voltage drop in dual-mode die 10.” (Mathew (Ex. 1015), 7:1-8)
- “***A single wire may be ball or wedge (stitch) bonded between one or more die bond pads and one or more inner leads of a leadframe, and/or between a plurality of bond pads to create a common connection therebetween.***” (Beauchamp (Ex. 1016), [0007])

Jumper Bond Wire Connections were Well-Known and Common

- “**a jumper wire 160 has been provided over a surface of the die 120** to provide a parallel path of communication (e.g., communication of the circuit or power)” (Beddingfeld (Ex. 1041), [0015])
- “**The jumper may be a bond wire** connected by thermal compression bonding, ball bonding and the like.” (Lee (Ex. 1039), 2:61-3:5)
- “**two bond fingers 18 are connected with a jumper wire bond 9, thereby bridging the signal traces 20.** Accordingly, power, ground, or other desired signals may be provided to various locations of the substrate 10 without requiring rerouting” (Conner (Ex. 1040), 3:37-59)

Core-Limited vs. Pad-Limited Designs

When the amount of “circuitry is driving how big [a] chip will be,” the IC design is said to be “core-limited” (*i.e.*, plenty of room for bond pads on the chip’s perimeter but not enough space in the “core” for actual circuitry). Saint, 211-213. Conversely, a “pad-limited” design has extra room in the chip’s interior for circuitry, but not enough space around the perimeter for the necessary bond pads. *Id.* In core-limited designs, it is especially important to utilize all available space. Foty, ¶¶ 49-50.

Core-Limited vs. Pad-Limited Designs

Pad-Limited Design

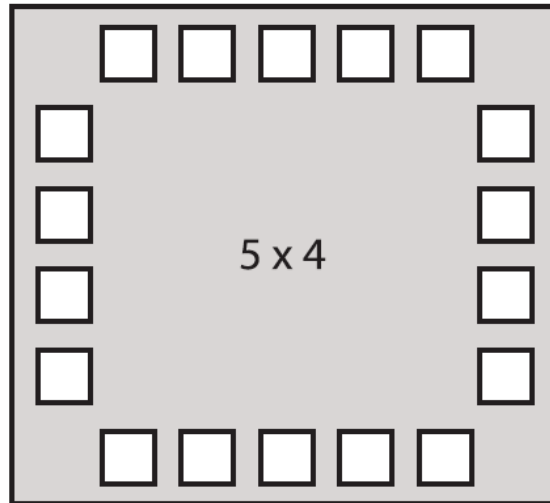


Figure 9–20. The minimum size of an 18-pad chip, based on the number of pads.

Core-Limited Design

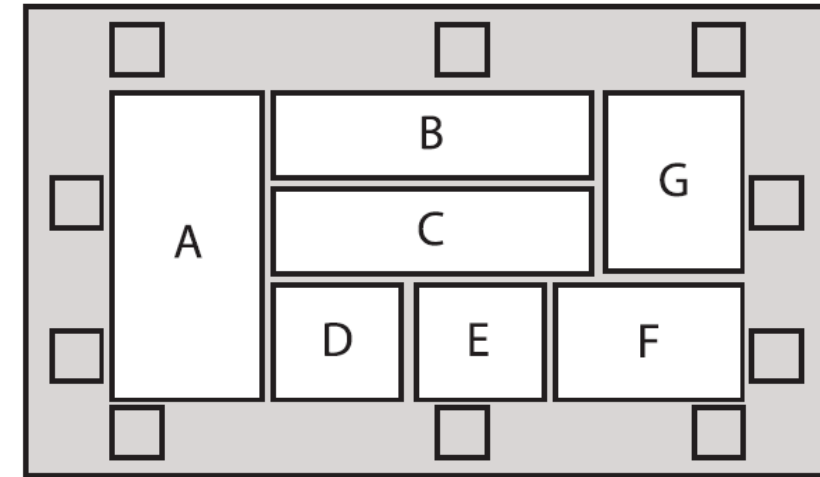


Figure 9–21. The minimum size of the chip limited by the anticipated sizes of the blocks.

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Obviousness Requires a “Flexible Approach”

[O]ur [obviousness] cases have set forth an **expansive and flexible approach.**

KSR Int’l Co. v. Teleflex Inc., 550 U.S. 398, 415 (2007)
Reply, 21

[A] court can consider the **inferences and creative steps** a [POSITA] would employ.

KSR Int’l Co. v. Teleflex Inc., 550 U.S. 398, 418 (2007)
Reply, 35

[I]t does not matter that there might be a better possible combination; **a combination only needs to be a suitable option.**

GUI Glob. Prods. v. Samsung Elecs. Co., 2024 WL 1564694, at *4 (Fed. Cir. Apr. 11, 2024) (emphasis original)
Reply, 21



It is Legal Error to Ignore a POSITA's Knowledge

Regardless of the tribunal, the inquiry into whether any 'differences' between the invention and the prior art would have rendered the invention obvious to a skilled artisan necessarily depends on such artisan's knowledge.

Koninklijke Philips N.V. v. Google LLC, 948 F.3d 1330 at 1337 (Fed. Cir. 2020)
Reply, 19



Saint Teaches Flexible Pad Assignments

Foty_Supp., ¶¶166-173. Figs. 7-1 and 7-2 illustrate two different, but “totally valid,” pad assignments for the same chip. *Id.* Petitioner’s Yoshinaga pad assignments are also “totally valid.” *Id.*, ¶¶153-154.

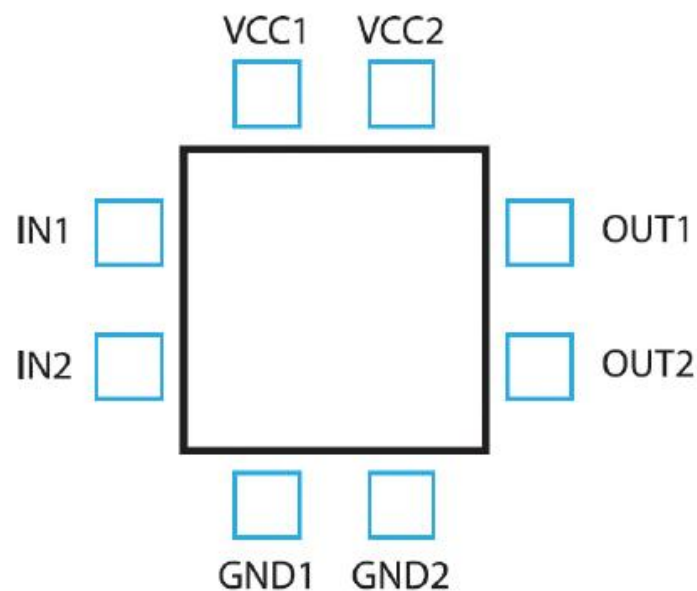


Figure 7-1. Like items set side by side. One possible pin-out.

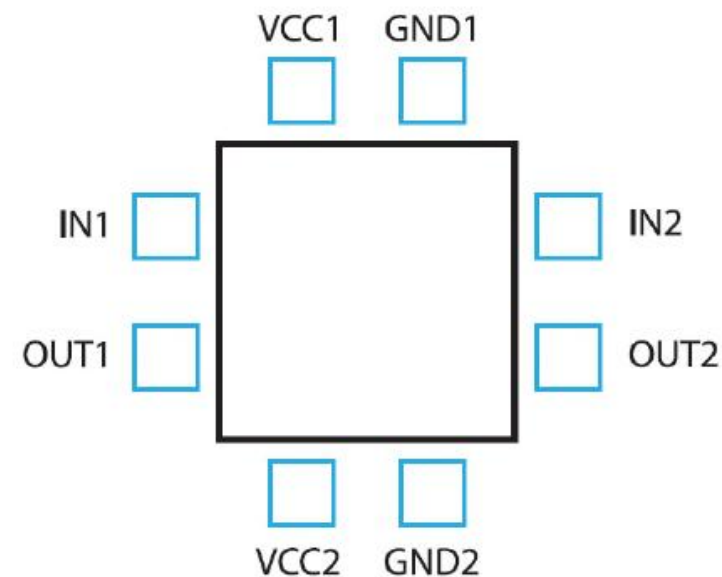


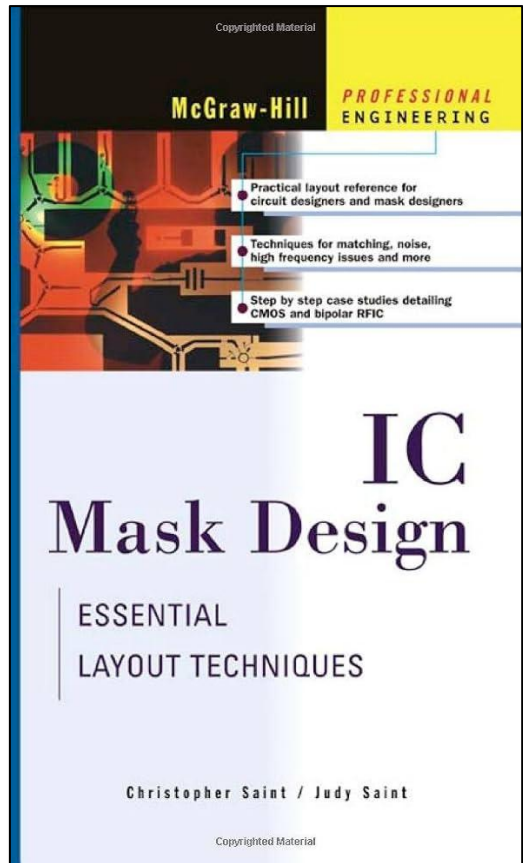
Figure 7-2. Very different pin placement will produce a very different layout.

Pad Placement is a Design Choice

labeled 3, 4, and 58 could just as readily be used for reference pads. The choice of selecting which pads to assign for ground, power, signals, etc. is left to the discretion of the designer - and may depend on factors such as the size of the chip, whether the chip is pad-limited or core-limited, the number of I/O signals, and the number available pads; however, there is no inherent restriction on how pads may be assigned. Indeed, Saint shows exactly this in its discussion of Figure 7-6 and 7-7,

Foty (Ex. 1003), ¶137

Saint Teaches “Pin-Driven Planning” (i.e. placing pads first)



Pin-Driven Planning

The first part of your floorplan that you can be involved in as a mask designer is the **pin-out**. Some people call it the **pad-out**. This is the step that defines where the input and output pins are placed that will surround the chip in its package.

The quality of your pin-out directly affects how good your chip floorplan will be and how easy the chip will be to lay out. I strongly recommend that mask designers attend the discussion about the pin-out for any chip they will be laying out. They will learn more about the function and structure of the chip, and be able to participate in the decisions. The pin-out directly affects your work.

*Saint, 158
Petition, 16; see also, ID, 17*

Patent Owner's Own Article (Ex. 2013, "Dubey) Recognizes Pad Flexibility

P/G PAD PLACEMENT OPTIMIZATION: PROBLEM FORMULATION FOR BEST IR DROP

Aishwarya Dubey, Texas Instruments (India)

Keywords
IR drop, P/G (Power/Ground) pad placement, current, package resistance, package inductance

ABSTRACT
IR drop minimization has become very difficult for chip packaged designs due to technology shrinking increasing design frequencies. Different constituent drop on a wire-bond chip (where pads are placed die-periphery) are "Package-ball to bond-pad", "bond-pad to internal global power ring drop", "internal local power ring drop". Optimization equations are developed to minimize IR drop from the lead frame to the standard cell power rails on the die by the P/G pads optimally for a given power network. Optimization equations are developed to minimize wire length on package for P/G pads drawing current. The cost functions in the optimization equations target minimum IR drop for those regions of the chip are switching at maximum speed. By use of a function for optimizing P/G pad placement, results representative chip with about 15 million gates and hard macros show an improvement of 10% to 15% in IR drop value for different floorplans (one floorplan with uniform power density, and the other floorplan with maximum power density much higher than the average power density of the design).

1 INTRODUCTION

With reducing chip dimensions and increasing frequency requirements, IR drop is fast becoming a dominant factor in determining the chip frequency. Due to on-chip IR drop, the voltage available across standard cells' supply rails is less than the power-supply voltage resulting into lesser drive current capability and therefore slower switching speeds. Worse, chip might not work at all due to hold violations, if due care is not taken in estimating the clock tree delays accurately with a given IR drop. This problem is hard to solve, as the voltage available at any spatial point in the chip is time varying and is dependent on the state of rest of the circuit. For making absolutely sure that the chip will function in all the use scenarios, it is suggested to perform dynamic IR drop analysis coupled with timing analysis for all possible use cases. Besides being computationally intensive, dynamic IR drop is a theoretically unsolvable problem as use cases are also dependent upon software, that is written for a particular application. However, all the applications of the chip might not even be known at design-

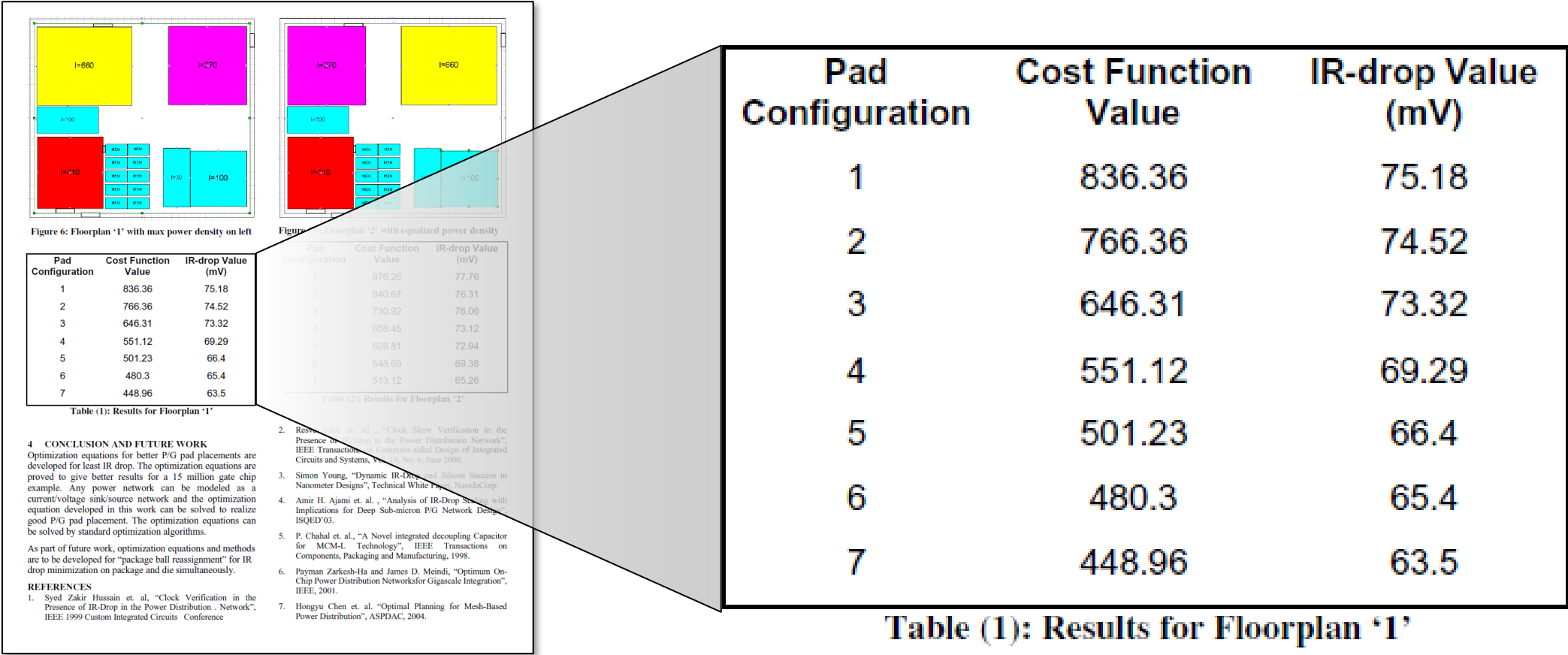
considered. In first scenario the package design is assumed to be flexible, such that there is complete independence in placing the P/G pads on the periphery with sole intention of minimizing "global power ring" IR drop. In another

causes higher power consumption. Worse, the circuit might remain under-designed (even with this approach) at the places where big supply spikes may remain undetected during static IR drop analysis. In [3] authors insist on the importance of dynamic IR drop analysis even though computationally expensive. In [4], [5] authors talk about the amount of decoupling capacitors needed on chip to counter the dynamic current spikes. In [6], using flip-chip packaging is considered to be the most effective solution for IR drop problems, which is more expensive than normal peripheral wire-bonded chips. In [7], authors discuss about the optimal planning for power mesh design, given a certain P/G pad placement.

Due to these accurate analysis problems, it is extremely necessary to limit the chip (static) IR drop to a minimum possible value for every given chip and its' design constraints. A very important factor that helps reduce the on-chip IR drop is the optimum placement of P/G pads at the chip periphery. In most cases, the number of P/G pads that can be assigned to power/ground signals is limited due to a constrained number of package pins. More the number of pins on the package, more is the package cost. On the other hand, for a given power ring structure, once the number of current sink points and general topology is

*Ex. 2013 (Dubey), 2
Reply, 22*

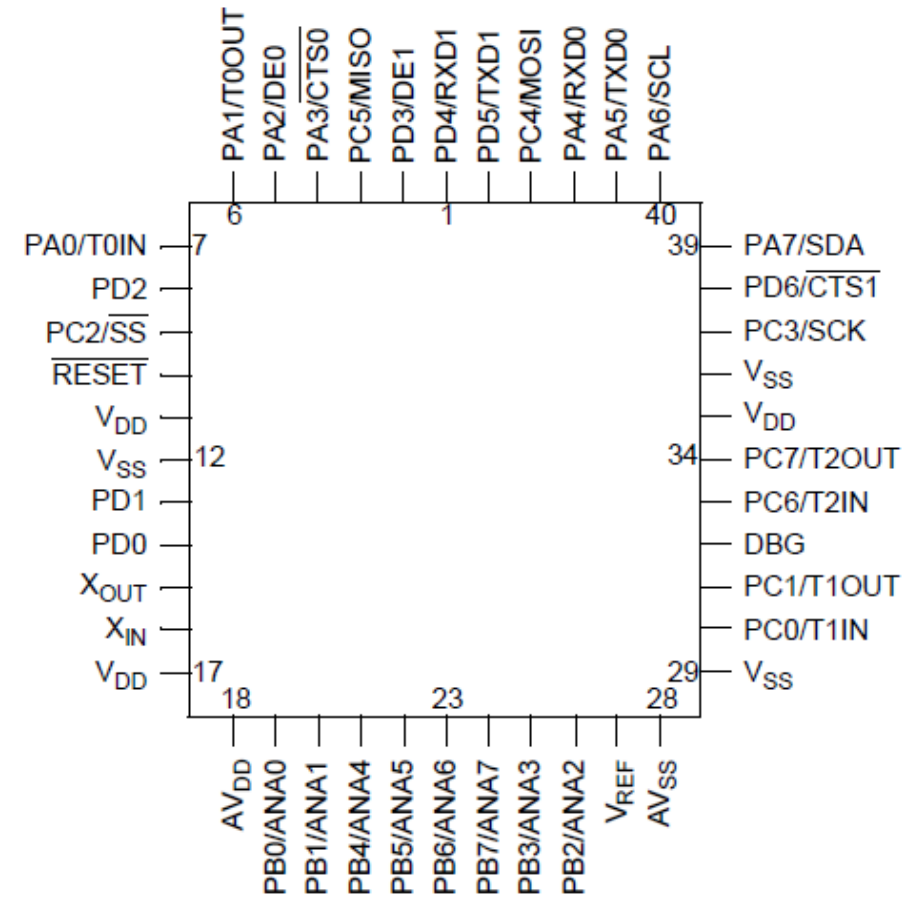
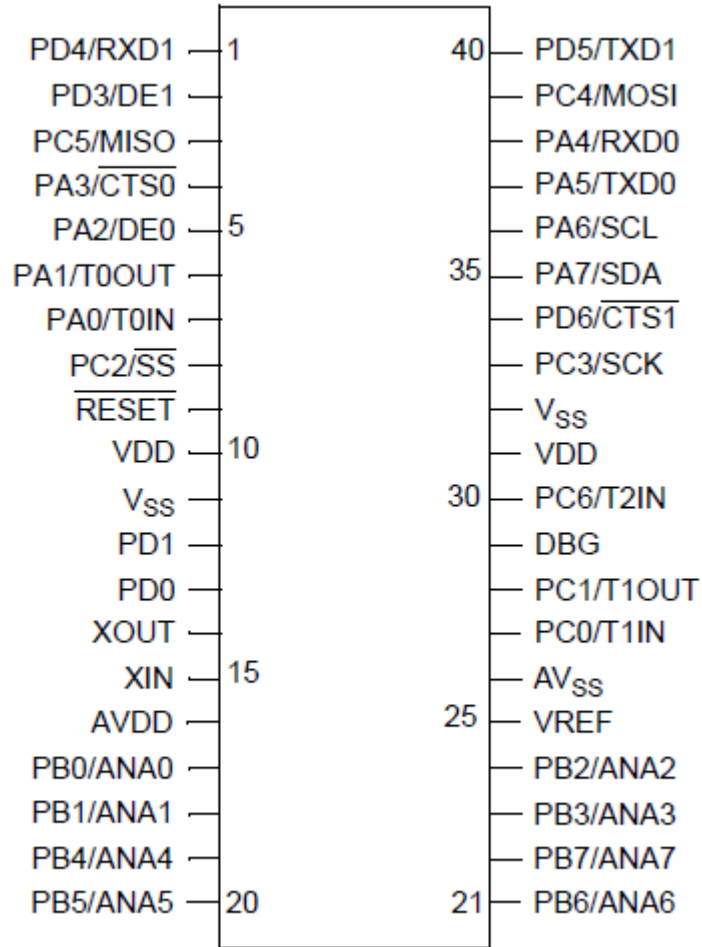
Patent Owner's Own Article (Dubey) Shows Different Pad Assignments



Ex. 2013 (Dubey), 6
Reply, 22

Real-life Datasheets (Ex. 1032-1036) Show Flexible Pad Assignments

- For the same chip, left image has 2 VDD and 2 GND pads vs 3 VDD and 3VSS on right



Ex. 1035, 28-29

Reply, 21-22; Foty Reply Dec. (Ex. 1042), ¶167

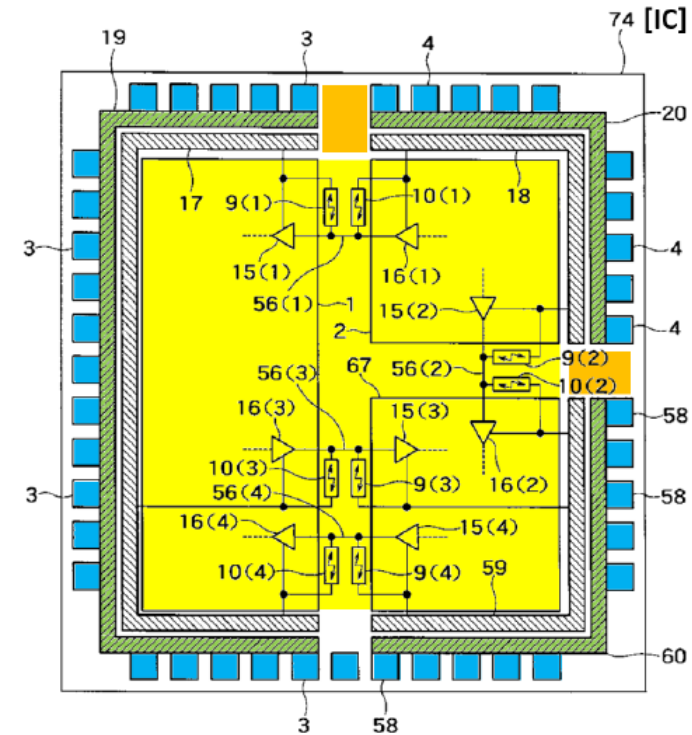
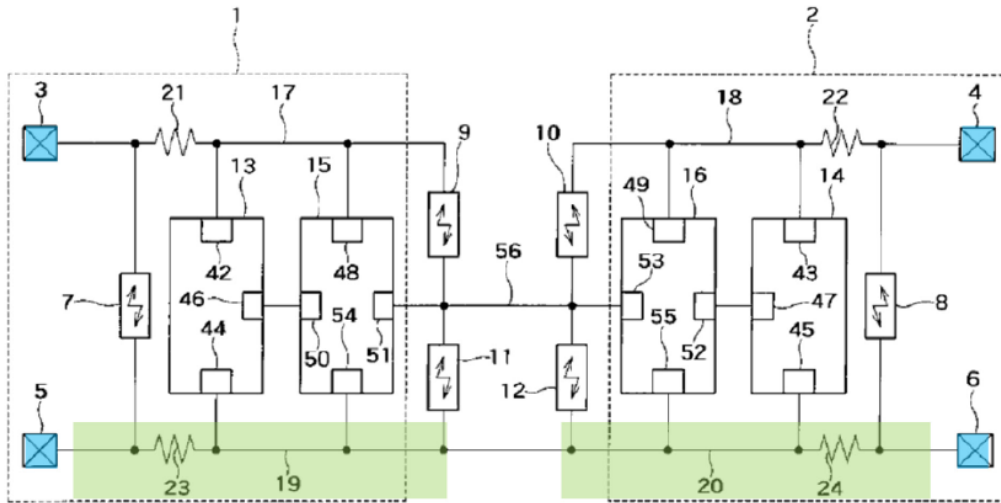
Patent Owner Misunderstands Saint's Pad Teachings

Citing Saint, PO asserts you “cannot arbitrarily change pads from unlabeled or supply pads to reference potential pads.” POR, 23. But Saint Chapter 9 (titled “Packaging”) merely says pads must align with package pins, so you cannot “blindly put [pads] wherever you feel like.” Saint, 201-202. This comment about pad/pin *alignment* says nothing about pad *assignments*.

Reply, 24 (discussing Saint, 201-202)

Pad Groups Adjacent and Connected To ESD Buses (Ground 1-2)

- Yoshinaga discloses pad groups (reference potential pads 5 and 6 colored blue below) adjacent and connected to ESD buses (e.g., reference potential lines 19 and 20 colored green below)



Yoshinaga, Figs. 2, 6 (annotated); Petition, 28, 30-34.

Pad Groups Adjacent and Connected To ESD Buses (Ground 1-2)

- Patent Owner incorrectly argues it would not have been obvious to assign bond pads beside Yoshinaga's saved area. *POR, 19-23.*

- As Patent Owner's expert admitted, whether a pad is a power supply pad, reference potential pad, or other pad, depends on its connection, and the pads themselves are basically the same.

pads are all similar [] if not completely identical

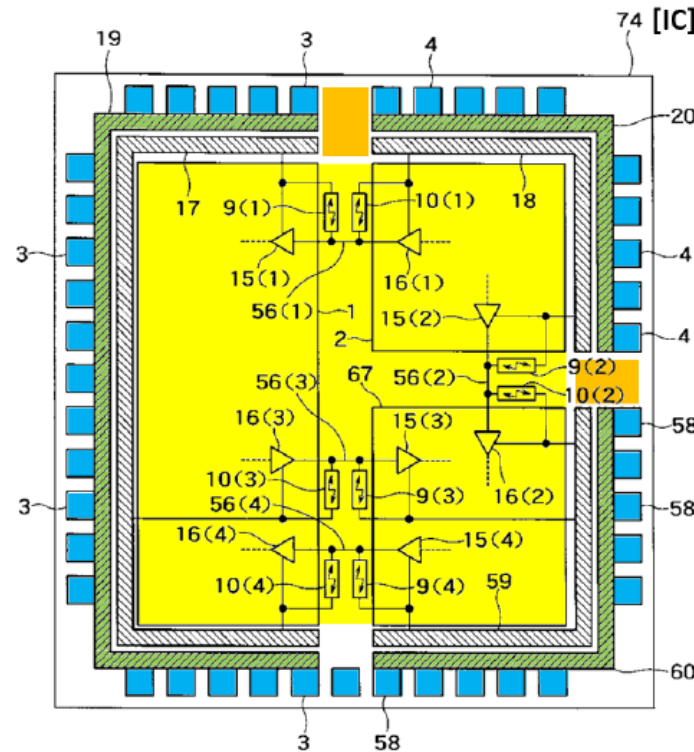
EX1038, 186:14-21; Reply, 20.

- To keep the bond wires short a POSITA would have assigned reference potential pads to be on each side of the "saved area." *Yoshinaga, Fig. 6 (annotated); Petition, 30-34.*

Yoshinaga's Unlabeled Ground Pads (Ground 1-2)

- Patent Owner argues that the pads of Yoshinaga Figure 6 do not include any ground pads. This is wrong. *POR, 22.*

- Most of Yoshinaga Fig. 6's pads are simply just not labelled, including the reference potential pads.



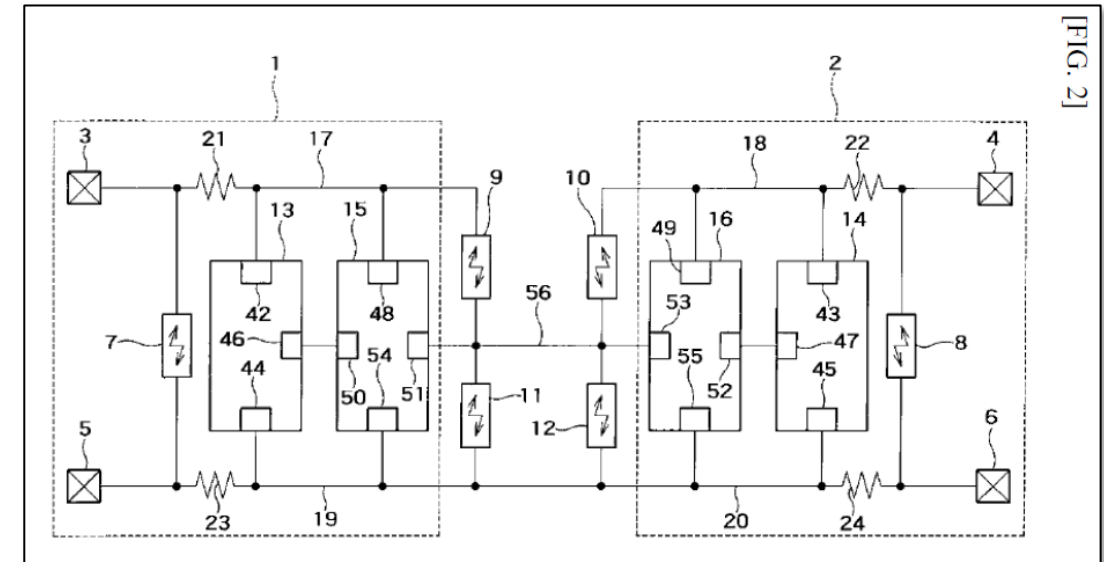
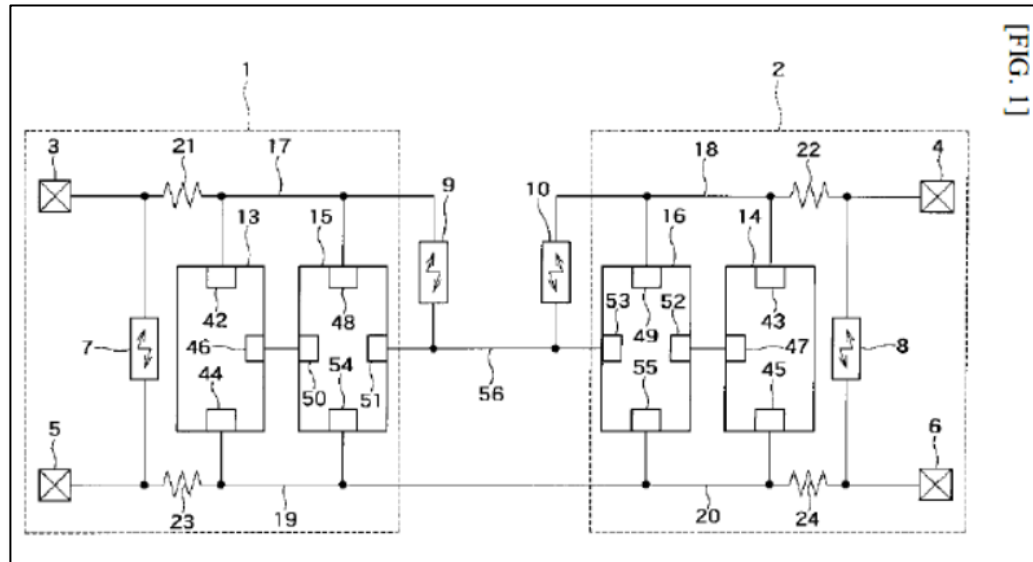
Yoshinaga, Fig. 6 (annotated); Reply, 17-18.

Yoshinaga's Unlabeled Ground Pads (Ground 1-2)

- Indeed, Yoshinaga states that Fig. 6 is a diagram of the “semiconductor [IC] of FIG. 1.”

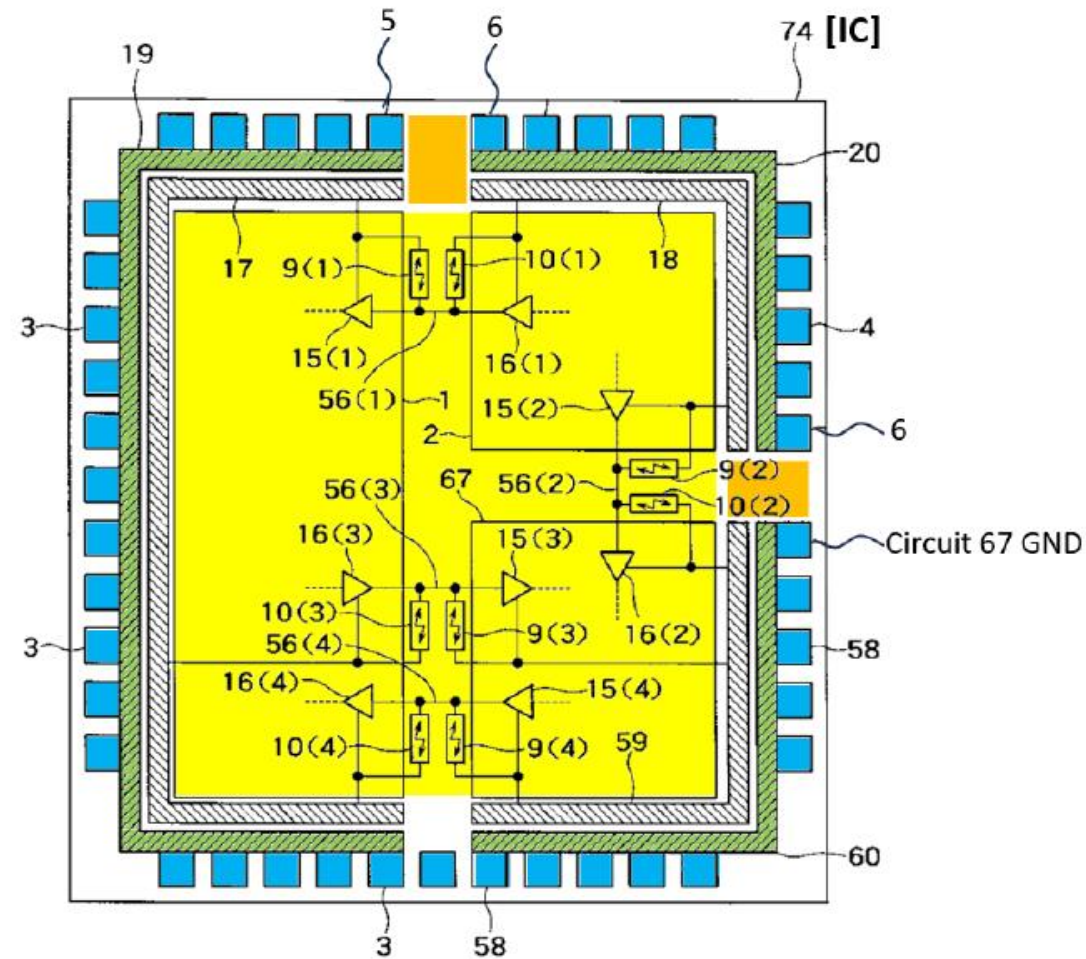
Yoshinaga, [0074]; Reply, 18.

- Yoshinaga Figs. 1 and 2 show that Yoshinaga's IC has reference potential pads (e.g., 5 and 6).



Yoshinaga, Fig. 1; Reply, 17-18.

Assigning Yoshinaga's Reference Potential Pads (Ground 1-2)



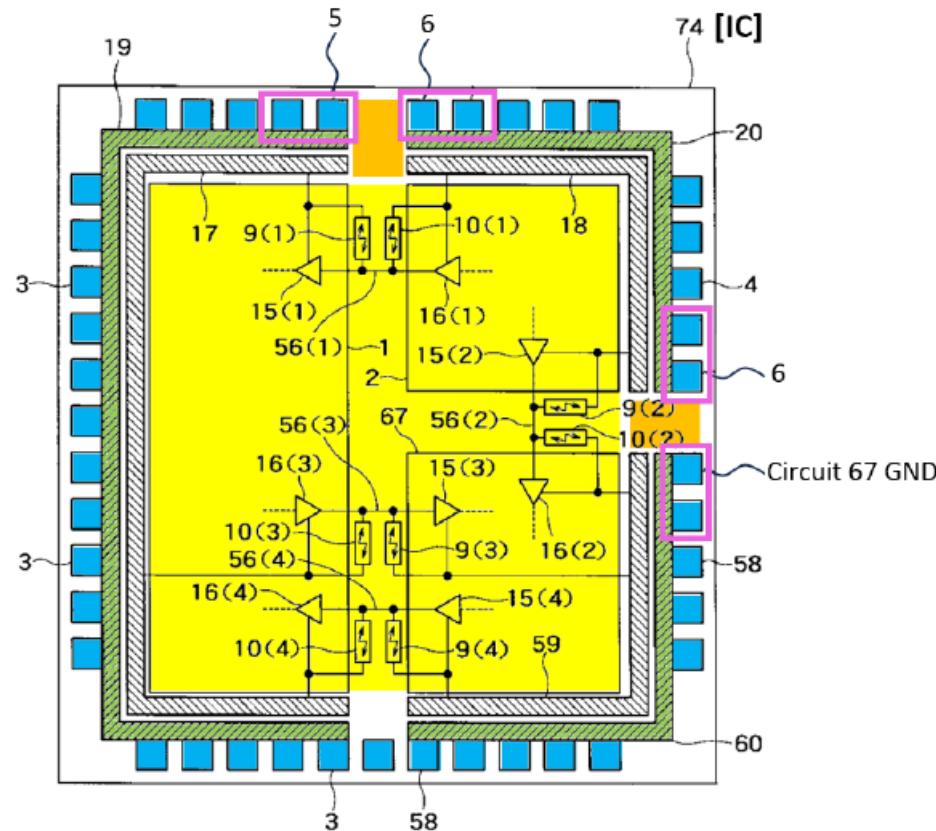
Yoshinaga, Fig. 6
Petition, 32

Yoshinaga's Unlabeled Ground Pads (Ground 1-2)

- Patent Owner continues in its Sur-Reply to argue an unduly literal reading of the combination provided in the Petition, arguing that the Petition removed supply pads.

Sur-Reply, 18-21.

- The Petition never proposed **removing** any pads – only assigning ground pads near the saved areas



*Yoshinaga, Fig. 6 (annotated);
Petition, 30-34;
Reply, 17-19.*

Petitioner Did Not “Remove” Any Pads from Yoshinaga

First, if Petitioner removed (instead of reassigned) power pads, modified Fig. 6 would show fewer pads, but it does not. *Compare* Yoshinaga Fig. 6 (42 pads) with Pet., 36 (modified Fig. 6 has 42 pads); EX1038, 292:19-293:5. Because supply pads could be assigned numerous locations among unused pads (Pet., 30-34, 20-23), Petitioner did not restrict reassignments to particular pad locations, nor is that material to the claims. Foty_Supp., ¶¶158-161. PO’s cited testimony makes

Reply, 24

Dr. Khatri Admits Yoshinaga's Pad Count Remains Unchanged



Q. Would you agree with me that looking at the left image, so that's the unmodified Yoshinaga Figure 6 and the right image which is the modified version of Yoshinaga Figure 6, that **in both images there are the same number of bond pads?**

A. I can see that the number of bond pads, you know, in the two images on page 25 of my declaration, which basically comes from Exhibit 1003, **the number of total pads has not changed.**

*Ex. 1038 (Khatri), 292:19-293:5
Reply, 24*

Dr. Khatri Admission re Ground Pads



What makes pad 22 a ground pad is the fact that it has a connection, you know, to the -- you know, to the ESD bus or the ground reference -- you know, to the ground reference line inside the chip. So it basically connects to the ground reference inside of the chip. That's what would make it a ground pad.

*Ex. 1038 (Khatri), 203:24-204:7
Reply, 20*

Dr. Khatri Can't Tell the Difference Between a Ground/Power Pad



Q. Can you tell by looking at Figure 1 which of the pads 12 is a ground pad?

A. You know, Figure 1 doesn't show that. But, you know, it would be clear to a person of ordinary skill in the art that some of them, you know, one or more of them would be ground pads. Because Figure 1 is just generally, it's just generally showing, you know, pads. And it's only labeling to one, but of course there are many pads there.

*Ex. 1038 (Khatri), 185:18-186:4
Reply, 20*

Dr. Khatri Admits Pads are Similar/Identical



But a person of ordinary skill in the art, again -- and again, based on the chips I've done, you know, the pads are all similar and if not completely identical, but pads of the same type are identical, other pads are very similar to each other.

*Ex. 1038 (Khatri), 186:14-21
Reply, 20*

So if any pad was connected to the ... reference terminal inside the chip, which can be, you know, all over the chip, then it will become -- it would be called a reference pad. And if a pad was connected to the supply terminal inside the chip, it would be called a supply pad.

Ex. 1038 (Khatri), 204:25-205:19Reply, 20

Dr. Khatri Admits Yoshinaga's Circuits are "Flexible"



Q. Does Yoshinaga disclose what function any of the circuits 1, 2 and 67 perform?

A. So a person of ordinary skill in the art when they look at Yoshinaga, they will understand that these circuits can be flexible, that Yoshinaga's teaching is not about the type of circuits in circuit 1, 2 and 67, but, in fact, it's about how you might do, you know, ESD improvement in an integrated circuit where you have multiple circuits. That's basically the teaching. The teaching is not focused on a specific circuit. And a person of ordinary skill in the art would readily understand that.

*Ex. 1038 (Khatri), 312:19-313:10
Reply, 25*

Dr. Khatri Admits Pad Assignments are Iterative



A. I mean, it's done iteratively and it's done along with the decision of number of bond -- the number of reference pads and power supply pads and so on. This is in some sense all in one -- you know, it's one process. You know, I mean, it's in one sort of combined umbrella, if you will.

*Ex. 1038 (Khatri), 171:17-24
Reply, 22*

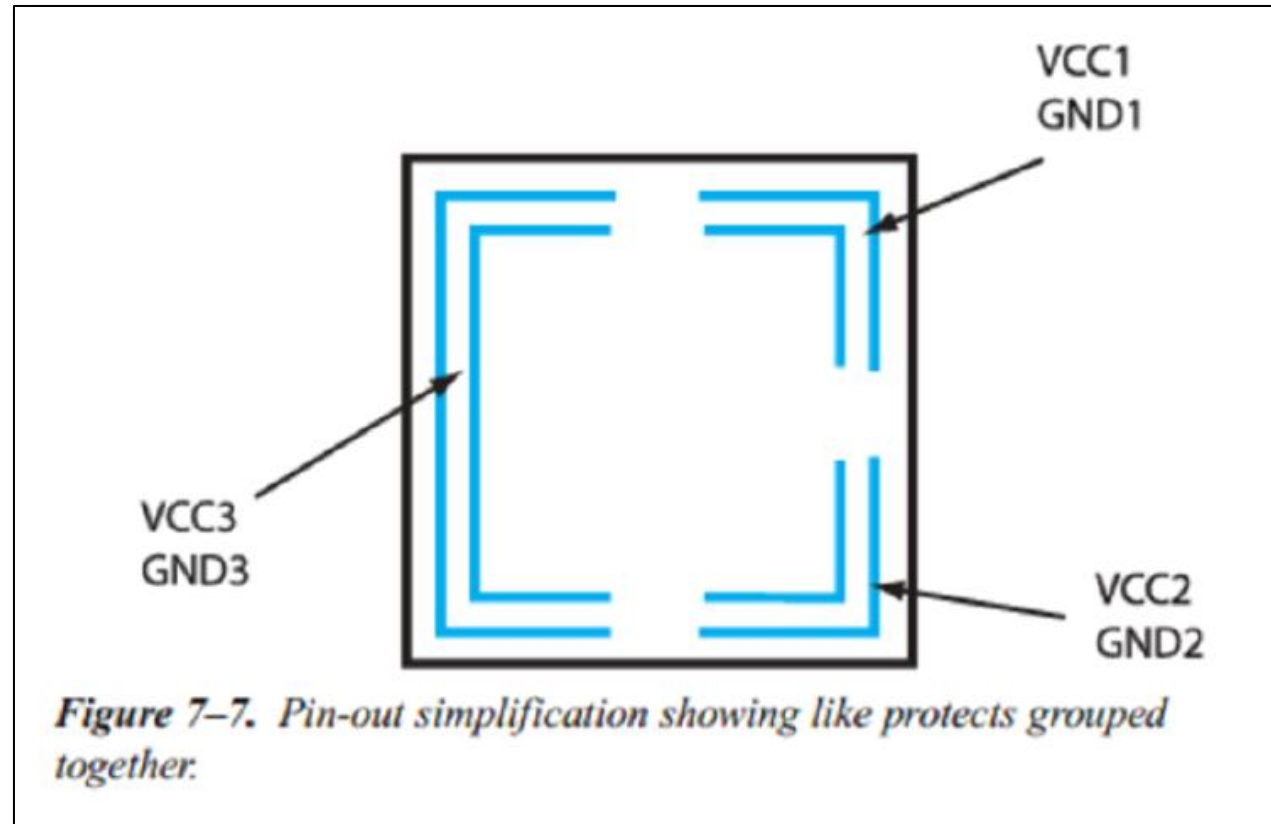
Petitioner Did Address Motivations for Pad Assignments

Third, Petitioner *did* explain why a POSITA would have made the proposed pad assignments. Pet., 31-32, 34-39. For example: (1) Yoshinaga shows ground pads electrically connected; (2) bondwires are a ubiquitous, affordable, and reliable means of connecting bond pads; (3) Saint teaches minimizing bondwire distance; and (4) Petitioner's pad assignments preserve Yoshinaga's *saved area*, which Saint teaches is desirable to reduce die size. *Id.*, 46-47, 49-50; Foty, ¶¶200-204; Saint, 206-210 (“Keep your [bond]wires [short]”), Fig. 9-28; Foty_Supp., ¶155. Contrary

Reply, 22-23

Saint and Haralabidis Disclose A Common ESD Bus (Ground 3)

- Saint plainly discloses multiple ESD buses (in blue below) in an integrated circuit:



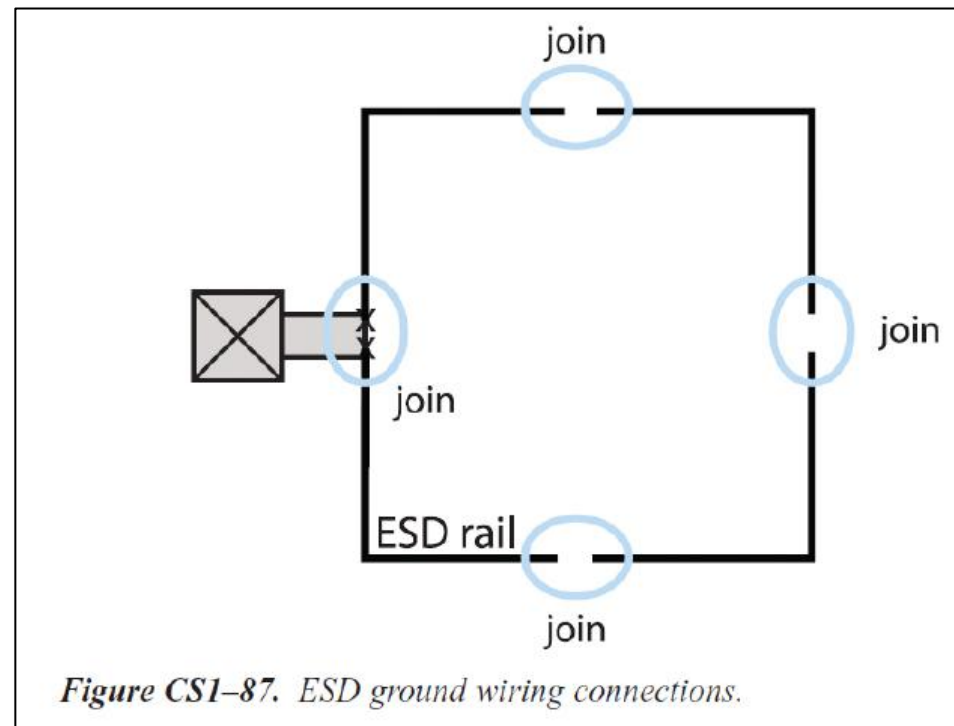
Saint, 162
Petition 71

Saint and Haralabidis Disclose A Common ESD Bus (Ground 3)

- Patent Owner argues a POSITA would not have connected ground lines together (e.g., GND1 through GND3 of Saint Fig. 7-7).

POR, 60-64
Sur-Reply, 21-24

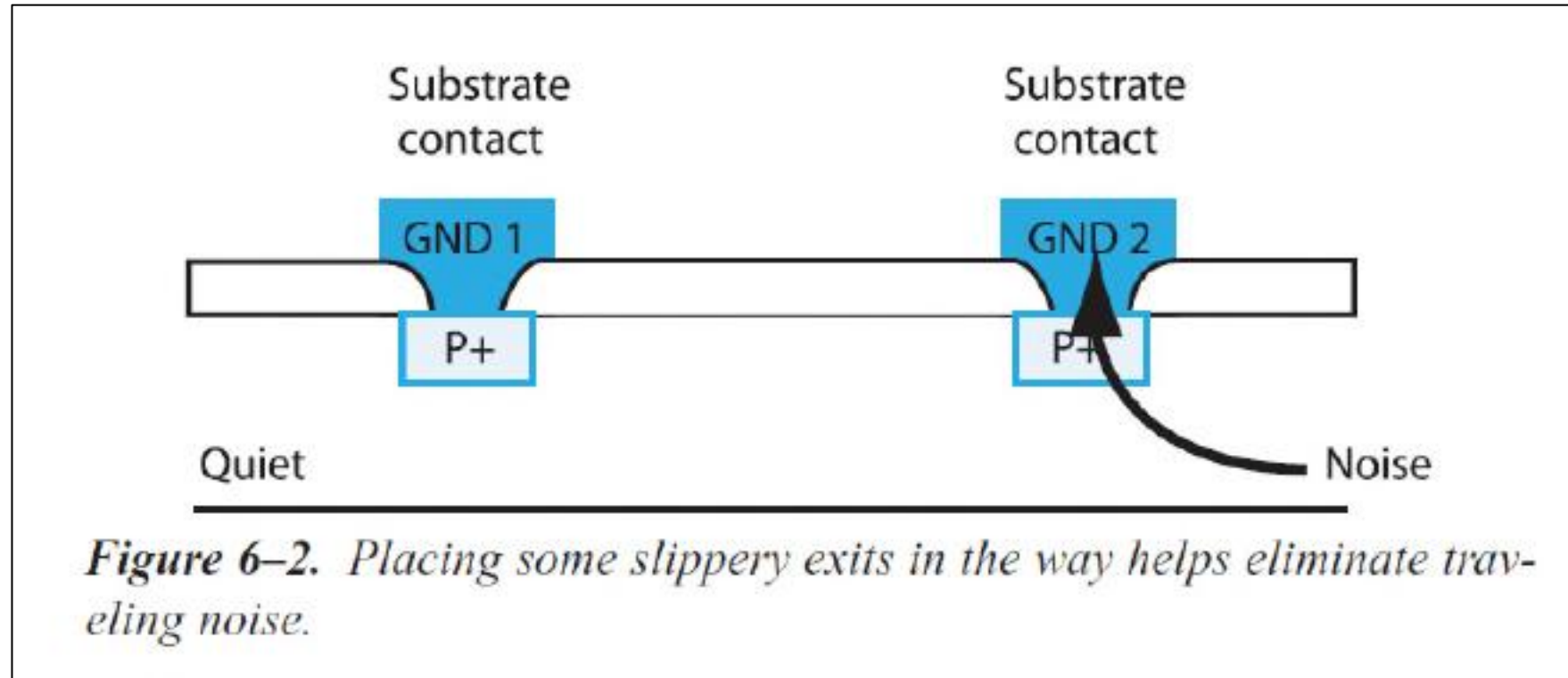
- But Saint directly controverts Patent Owner, teaching in a case study that one *would* connect the “ESD grounds to each other:”



Saint, 333, Fig. CS1-87
Reply, 15

Saint and Haralabidis Disclose A Common ESD Bus (Ground 3)

- Saint teaches connecting GND lines in a singular “ring of ground substrate contacts:”



Saint, 142, Fig. 6-2; Reply, 14.

Saint's "GND" Nomenclature is Analogous to Haralibidis and Yoshinaga

Saint, Fig. 6-2. A POSITA would have understood Fig. 7-7's GND1/GND2/GND3 designations simply reflect that they correspond to VCC1/VCC2/VCC3, respectively. Foty_Supp., ¶¶122-123. Differing supply voltages (*e.g.*, VCC1=3V, VCC2=5V, etc.) does not mean reference voltages differ. To the contrary, as Saint Fig. 6-2 shows, GND1, GND2, etc. are the same. Haralabidis confirms this. *Id.*

Haralabidis has "respective ground connections VSS1, VSS2, VSSN," analogous to Saint's GND1/GND2/GND3. Haralibidis, 5:42-6:2. Haralabidis explains that "each ground connection VSS1, VSS2, VSSN is connected to ... the PC board common ground rail 670." *Id.* Similarly, Yoshinaga labels the same reference lines with different numerals (*e.g.*, 19, 20, 60) based on their corresponding power domain. Yoshinaga, Fig. 6, [0088].

Reply, 14.-15

A POSITA Would Understand (of Find Obvious) that Saint's Ground Buses Connect

PO's contrary assertion is like saying shower and sink drains do not connect before exiting a house. While possible, such an approach is rare. Likewise, in electronics, the far more common (and obvious) approach is connecting ground buses on (or near) the chip as Saint Case Study 1 discloses. Foty_Supp., ¶124; Saint, 333 (“hook[] up all [] ESD grounds to each other”).

Reply, 15

Saint and Haralabidis Disclose A Common ESD Bus (Ground 3)

- Haralabidis teaches the same benefit—that doing so would lower resistance and noise. A POSITA would have known this.

low resistance to (earth) ground of the PC board ground rail [] relative to that of the connections, assists greatly in attenuating the noise/interference travelling through the same.

*Haralabidis, 5:3-31, Fig. 6
Reply, 12*

The *Polaris*, *Fanduel*, and *Cutsforth* Cases are Easily Distinguished

PO's cases (POR, 20) are easily distinguished. In *Polaris*, the proposed modification “undisputed[ly]” “[ran] contrary to one of Denney’s stated purposes.” 882 F.3d at 1069 n.4. By contrast, Petitioner’s pad assignments further (rather than defeat) Yoshinaga’s goal to “keep the chip [] small.” Yoshinaga, [0084]. This also distinguishes *Fanduel*. And *Cutsforth* stands for the proposition that design choice turns on case facts. Here, the facts favor Petitioner. Unlike *Cutsforth*—where the modification rationale was “not alter[ing device] operation”—Yoshinaga discloses the connection between pads 5 and 6.

Reply, 22

Patent Owner Employs a Double Standard re Purported “Disadvantages”

[T]he Board’s observation that appellant did not provide the type of detail in his specification that he now argues is necessary in prior art references supports the Board’s finding that [a POSITA] would have known how to implement the features of the references and would have concluded that the reference disclosures would have been enabling.

In re Epstein, 32 F.3d 1559, 1568 (Fed. Cir. 1994)
Reply, 24

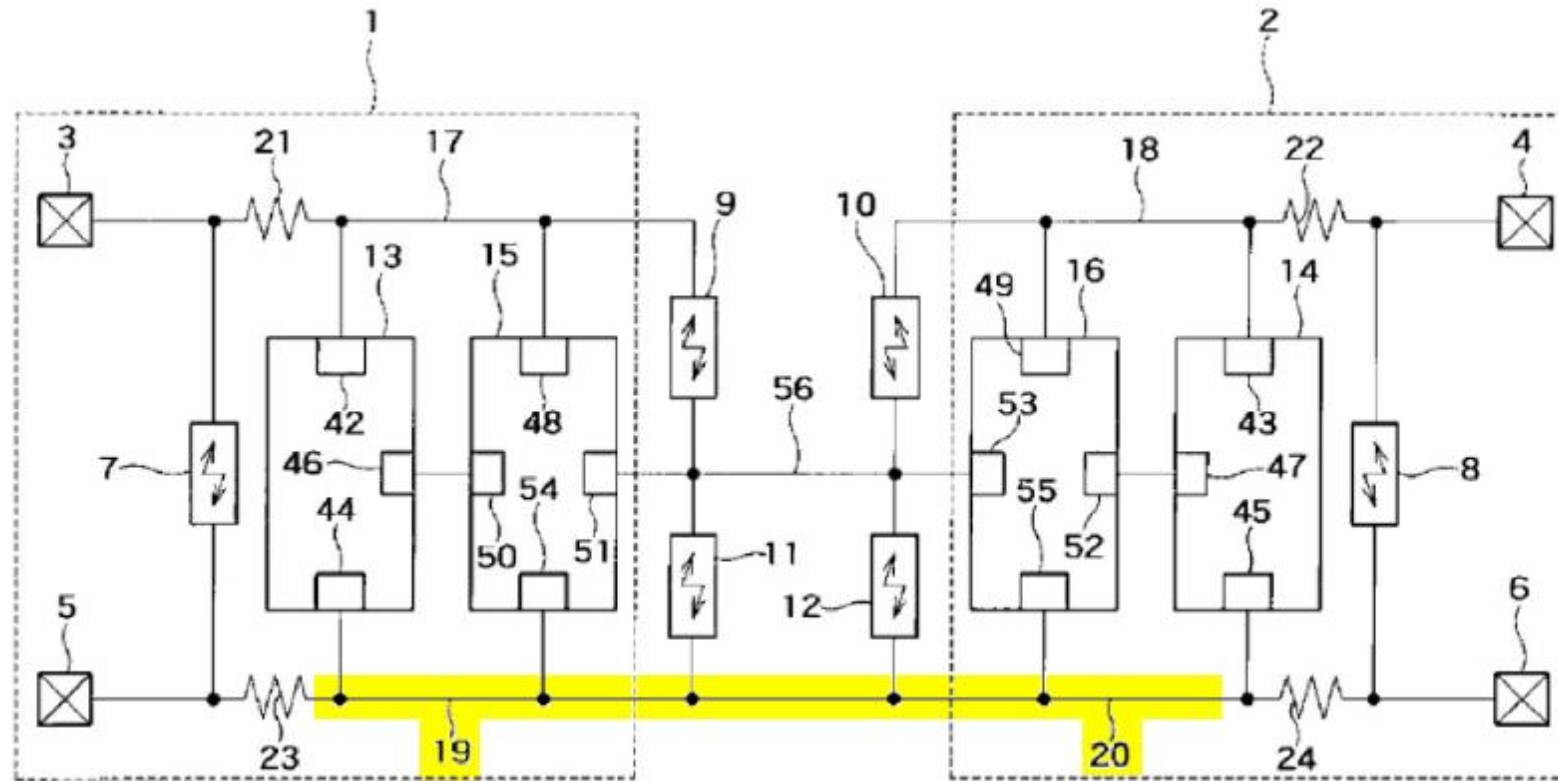


Roadmap

- I. Introduction and IPR Grounds
- II. Overview of the '164 Patent and Prior Art
- III. Pad Assignment & ESD Bus Disputes
- IV. Bond Wire Disputes**
- V. Saved Area

Obvious to Connect Ground Pads With Bondwires (Grounds 1-2)

- Yoshinaga expressly shows reference potential pads (5 and 6 below) are connected.
- But Yoshinaga's topological diagram does not show how the connection is implemented:



*E.g., Yoshinaga, Fig. 2 (annotated)
Petition, 35; Reply, 3*

Bond Wire Connections (Ground 1-2)

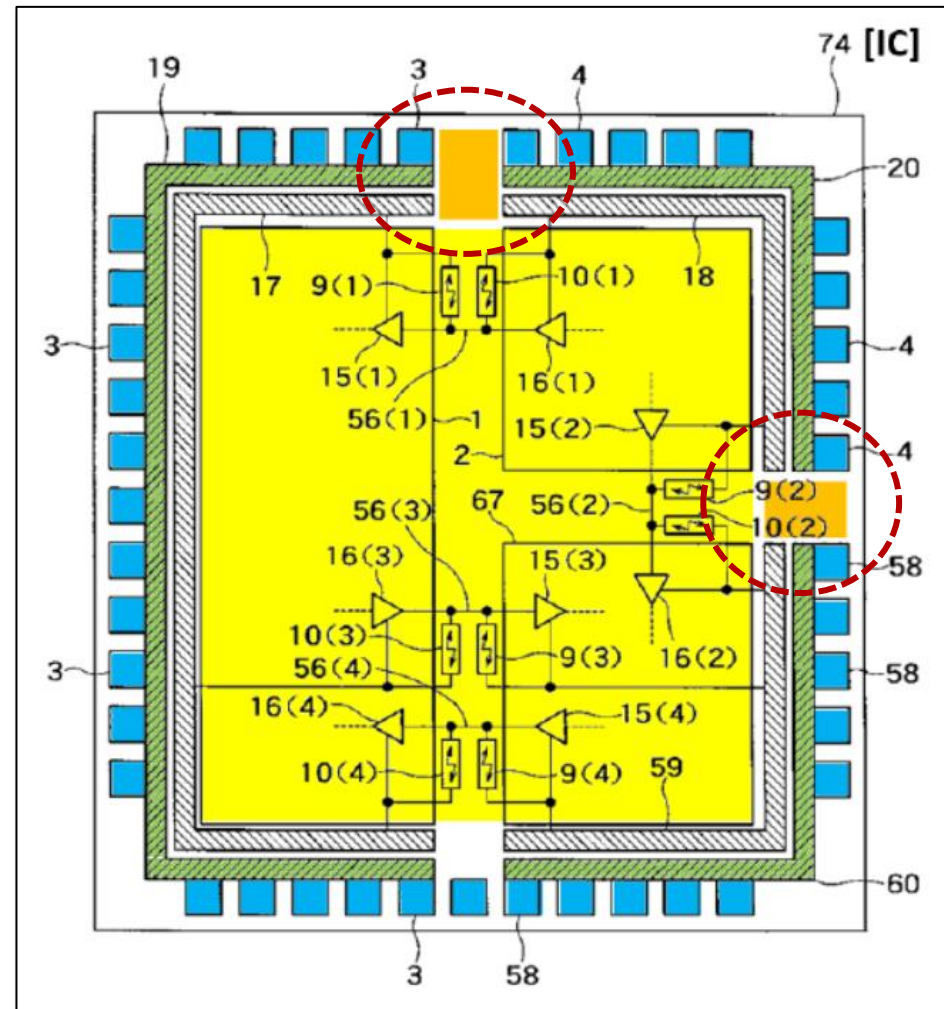
[0005]

Circuits having separated power supply lines are not usually completely separated from each other, and one of multiple reference potential lines is used as a main ESD discharge path, and multiple reference potential lines are connected to each other. The reference potential lines may be connected by bidirectional diodes that are connected in parallel to one another in the opposite direction to avoid noise.

*Yoshinaga, [0005]
Petition, 21, 34, 42*

Obvious to Connect Ground Pads With Bondwires (Grounds 1-2)

- Yoshinaga Fig. 6 shows metal traces for the ground and power buses, but leaves open the technique for connecting the ground buses (19, 20, and 60)



*E.g., Yoshinaga, Fig. 6 (annotated)
Petition, 34-39*

Bond Wire Connections (Ground 1-2)

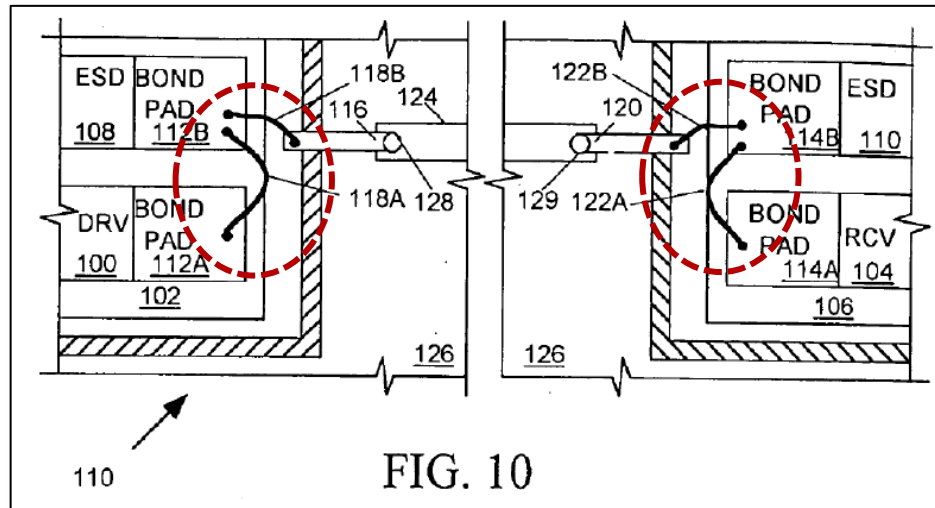
- An obvious way would be to use bond wires, as it was a well-known method of making connections in integrated circuits
- Recall, Patent Owner's expert admitted that bond wires was one of two such options:

A. ... using **bond wires** to connect to the two bond pads because that's what the petition is trying to teach, you know, and also -- **so that's one option.** And then there are, you know, teachings in some of the references cited by the petitioner, which basically use on-chip metallization. **So those are sort of the two options for the matter at hand.**

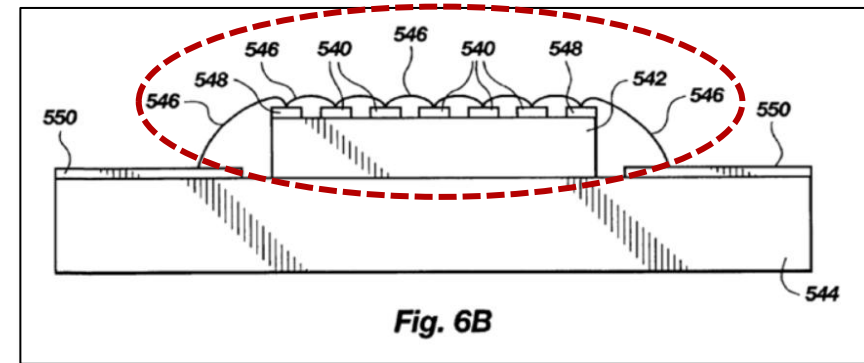
*E.g., Ex. 1038, 157:23-158:20
Reply, 4*

Obvious to Connect Ground Pads With Bondwires

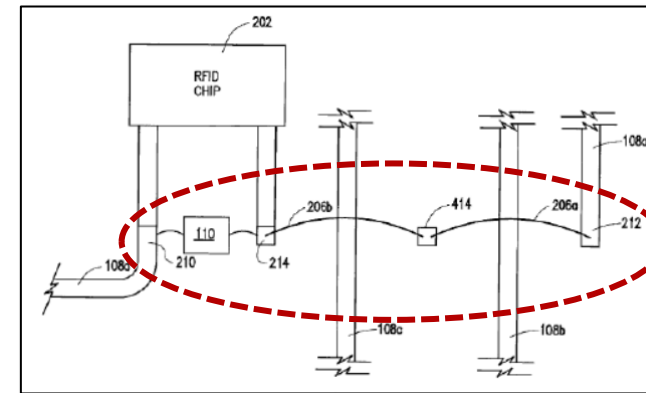
- Bonding wires were a well-known and commonly employed mechanism to connect to pads:



Ex. 1014, Fig. 10 (annotated)
Petition, 37



Ex. 1020, Fig. 6B (annotated)
Petition, 38



Ex. 1039, Fig. 4 (annotated)
Reply, 7

Obvious to Connect Ground Pads With Bondwires (Ground 3)

- Saint discloses using bond wires to make connections to pads

Wire bonding is the most common method of attaching a chip to a package.

*Saint, 202-207
Petition, 68*

- Similarly, Haralabidis discloses using “wirebonds” connections for the ESD bus

In a further aspect of the disclosure, the IC package substrate is disposed on a support substrate, such as a PC board, having a support ground rail, where the segments of the package ground rail are coupled to the support ground rail by corresponding second electrical connections that could be, for example, **wirebonds**, solder bumps, solder balls, and the like.

*Haralabidis, 1:65-2:4
Petition, 76*

Dr. Khatri Admits There Are Only Two Connection Options



But what I can give you is -- what I can say is for the 164 IPR, for the references that have been cited and are being discussed in the 164 IPR and for the cites that I present in my declaration, I only see the two choices on the consideration as the, you know, as the bond wire to connect two bond pads on the same chip or the on-chip metallization to connect, you know, to connect circuit nodes on the same chip.

*Ex. 1038 (Khatri), 161:19-162:5
Reply, 4*

Obvious to Make Connections Using Bond Wires

- Patent Owner's own expert confirmed that there were only two options to make the connections: bond wires and on-chip metallization.

A. ... using **bond wires** to connect to the two bond pads because that's what the petition is trying to teach, you know, and also -- **so that's one option**. And then there are, you know, teachings in some of the references cited by the petitioner, which basically use on-chip metallization. **So those are sort of the two options for the matter at hand.**

*E.g., Ex. 1038, 157:23-158:20
Reply, 4*

- Where there are two suitable options known to a POSITA, it is obvious to try either one.

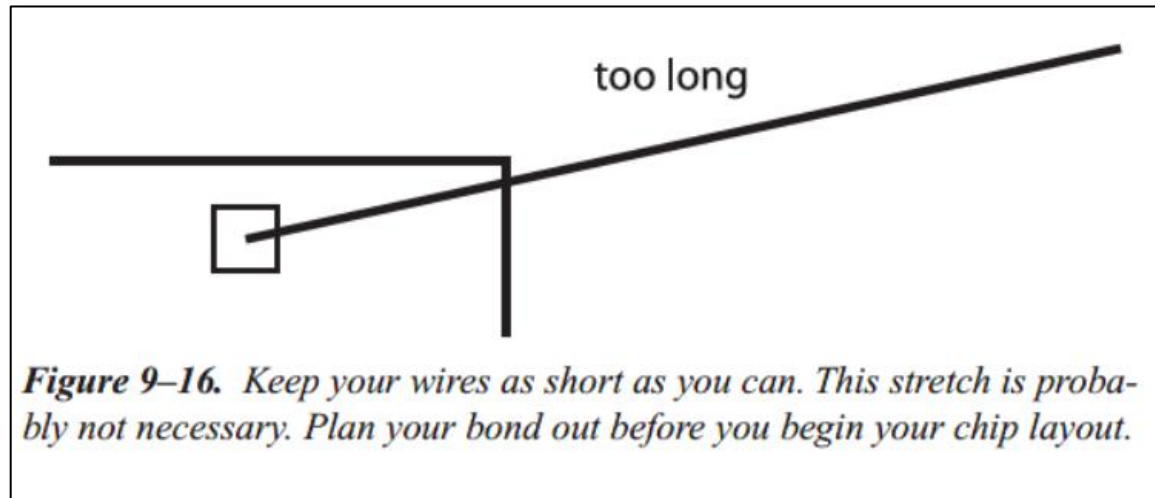
Furthermore, a POSITA would have found it obvious to place bond wires in this way because there are only two finite options for running the bond wires: over the circuit area or not over the circuit area. Foty, ¶ 201. And running the bond wires

Petition, 48

Bond Wire Connections

- A POSITA would have known to keep bond wires short as a general design principle.

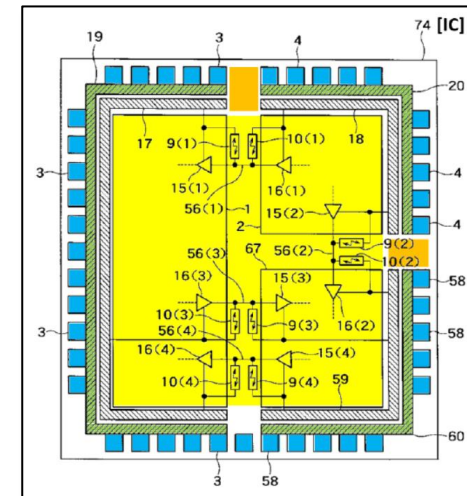
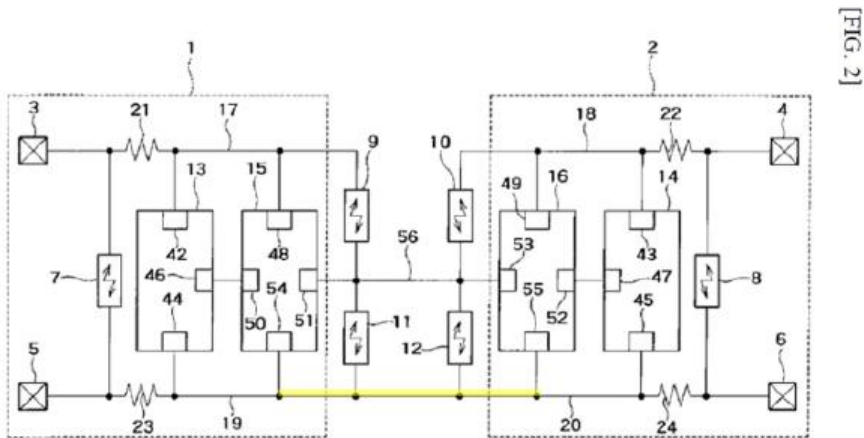
So, you have to keep the overlap of the bond wire over unused silicon as short as possible.



*Saint, 209-210, Fig. 9-16;
Petition, 47.*

Patent Owner's "Metallization" Argument Fails

- Patent Owner argues for all Grounds that a POSITA must have used on-chip metallization instead of bond wires when making connections between pads or a pad and an ESD bus.
POR, 31-34, 66.
- For Grounds 1-2, Patent Owner incorrectly says Yoshinaga discloses (and is limited to) using an on-chip metal trace.
POR, 31-34.
- But Patent Owner relies on *circuit schematics* (e.g., below, left) for this assertion, but the only layout image from Yoshinaga (below, right) shows no on-chip metal trace.



*Reply, 3-4; POR, 31-34
Sur-Reply, 24-27*

Ex. 1006, Figs. 2, 6; POR, 31-34; Sur-Reply, 24-27; Reply, 3-4

Dr. Khatri Admits “metallization [resistance] dominates”



Also, the same statement cites to the signal consulting, the Exhibit 2014, and it quotes there saying series of resistance, not inductance, dominates on-chip connections. On-chip connections means integrated circuit metallization. Integrated circuit metallization has resistance that dominates, but not inductance.

*Ex. 1038 (Khatri), 143:3-12
Reply, 27*

The Possible Use of Metallization is Irrelevant

[T]he mere disclosure of alternative designs does not teach away. This court has further explained that just because better alternatives exist in the prior art does not mean that an inferior combination is inapt for obviousness purposes.

In re Mouttet, 686 F.3d 1322, 1334 (Fed. Cir. 2012) (internal cites and quotes omitted)
Reply, 12



The Possible Use of Metallization is Irrelevant

[T]he fact that there are other possible solutions to a problem does not affect the obviousness analysis as to one of those possible solutions.

Purdue Pharma L.P. v. Accord Healthcare Inc., 2024 U.S. Dist. LEXIS 161403 (D. Del. Sept. 9, 2024)
Reply, 17



Using Bond Wires Was a Suitable Option



Intel just had to show that Bauman's secondary cache was a "suitable option" to replace Kabemoto's secondary cache. ... It's enough for Intel to show that there was a known problem of cache coherency in the art, that Bauman's secondary cache helped address that issue, and that combining the teachings of Kabemoto and Bauman wasn't beyond the skill of an ordinary artisan. Nothing more is required to show a motivation to combine under *KSR*, so we reverse the Board's finding to the contrary.

Intel Corp. v. PACT XPP Schweiz AG, F.4th 1373, 1381 (Fed. Cir. 2023)
Reply, 16-17

Using Bond Wires Was a Suitable Option

[I]f there's a known technique to address a known problem using prior art elements according to their established functions, then there is a motivation to combine. [] And we specify *address* a known problem because **it's not necessary to show that a combination is the best option, only that it be a *suitable* option.**

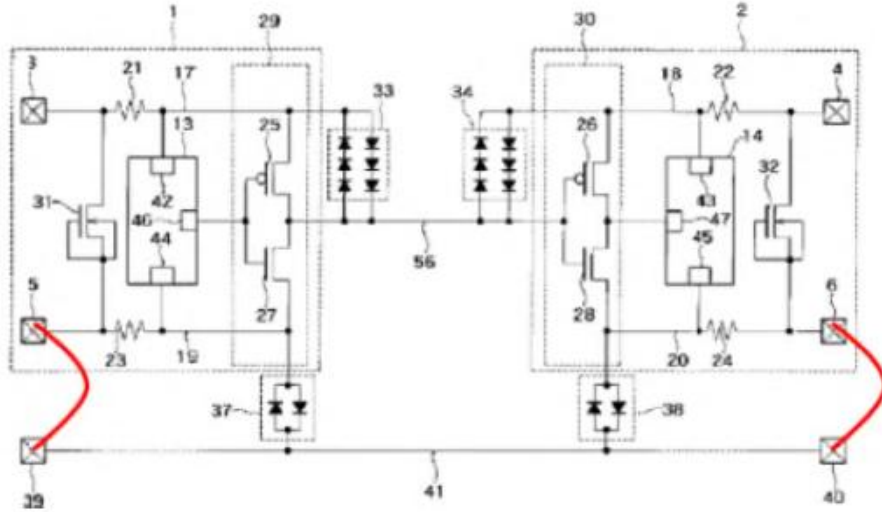
Intel Corp. v. PACT XPP Schweiz AG, F.4th 1373, 1380 (Fed. Cir. 2023) (emphasis original, cites omitted)
Reply, 21



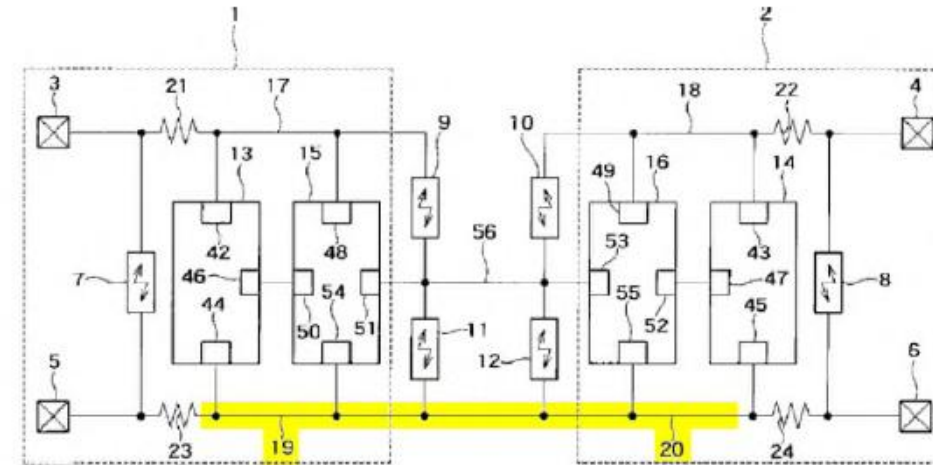
Patent Owner Relies on the Wrong Yoshinaga Figure (Grounds 1 and 2)

- Patent Owner relies on Yoshinaga **Figure 3** despite the Petition relying on Figure 2.

POR, 31; Sur-Reply, 24-26, 28-29



POR, 54 (Yoshinaga, Fig. 3)
(PO annotated)



Pet., 35 (Yoshinaga, Fig. 2)
(Petitioner annotated)

*Yoshinaga, Fig. 3 (from POR, 54) vs. Fig. 2 (from Petition, 35)
Reply, 11*

Patent Owner's Noise/Inductance Argument Fails

- Patent Owner contends a POSTA would not use bondwires due to “noise” and “inductance”
POR, 4, 33-34, 36-38; Sur-Reply, 26-28.

- But this ignores the prevalence of bondwires, which show noise/inductance do not limit use

Wire bonds account for over 80% of first-level chip interconnections made by the microelectronic industry each year

Ex. 1043, 1; Reply, 5-6

- This also ignores that circuits already combine these electrical characteristics, and merely having some noise or inductance does not mean an element cannot or should not be used.

Practical transmission circuits always combine some amount of both resistance and inductance.

Ex. 2014, 2; Reply, 6

- The '164 patent is silent regarding bondwire “noise” and “inductance,” confirming they were not real concerns

Reply, 6

Patent Owner's Noise/Inductance Argument Fails (Grounds 1-2)

3. PO's Noise/Inductance Arguments Fail

PO's argument that bondwires would "introduce[] noise" (POR, 33) by connecting ground pads 5 and 6 is baseless. Foty_Supp., ¶¶69-78. PO's premise is that bidirectional diodes 37 and 38 in Fig. 3 reduce noise, so removing them increases noise. POR, 37-38. But Petitioner starts from Figs. 1-2 and 4, which connect ground pads 5 and 6 *without intervening diodes* and work fine. The lack of diodes is unsurprising given that modest noise in average chips is irrelevant, just like modest signal noise did not stop AM/FM radio from proliferating. Foty_Supp., ¶¶76, 181-182.

Reply, 5

Dr. Khatri Admits “Noise” Problem was Solved



Q. How did the '164 Patent solve the noise problems that you mentioned earlier that are introduced by the use of bond wires?

A. But as an electrical engineer, we all know that, you know, circuit techniques and manufacturing techniques can improve over the years. And so it's completely not surprising to me that what was considered as, you know, in the conventional wisdom as a bad idea has been solved in multiple ways. And I could come up with some ways to solve it, you know as well as a person of, you know, of experience in this space.

*Ex. 1038 (Khatri), 254:16-255:2
Reply, 6*

Dr. Khatri Admits His Own Chips Use Bond Wires



Now, the other three chips which we did at Texas A&M, the three chips I mentioned, subthreshold, BPSK transmitter, then I think it might have been BFSK -- anyway, but the subthreshold transmitter, then the multichannel analyzer, the MCA and the alpha detector, **all of these had bond pads and bond wires and they were packaged using a regular, you know, plastic package, a square plastic package.** So the three chipset at Texas A&M used bond wires with, you know, with – what's it called, sorry -- you know, with bond pads and bond wires in sort of a plastic package.

*Ex. 1038 (Khatri), 120:12-121:2
Reply, 5*

Dr. Khatri Admits Bond Wires Are Still Used Even Today



Q. Are bond wires still used in chips today?

A. I think we went through this, you know, this kind of questioning. I think you had asked about how long they've been around and that's when I said they use for, you know, connecting, you know, chips to packages. So that's still in use today.

Q. How prevalent is it?

A. I don't know. I don't really have market data as such, but, you know, I mean, it's not – it's still used, yeah.

*Ex. 1038 (Khatri), 162:18-169:6
Reply, 6*

Dr. Khatri Admits Bond Wires are Inexpensive



Q. Did the Texas A&M chips use bond wires?

A. Yes, we use bond wires because we're poor. So if I had the choice, I would use C4 or something like this, but that's a much more expensive packaging technology and, you know, we were literally, all my Texas A&M chips are on a shoestring budget.

*Ex. 1038 (Khatri), 132:8-16
Reply, 9, 17*

Patent Owner's "Droop" Argument Fails (Grounds 1-2)

- Patent Owner also argues that a POSITA would not have used bond wires because they could "droop" and cause a short circuit.

POR, 38-39; Sur-Reply, 26-28.

- Patent Owner's Sur-reply ignores that concerns about shorting or droop are baseless because, as Saint teaches, "[bond]wires are covered in plastic, which also covers the chip" and prevents the bond wire from drooping and causing shorts.

*Saint, 202-203;
Reply, 8-9; Sur-Reply, 26-28.*

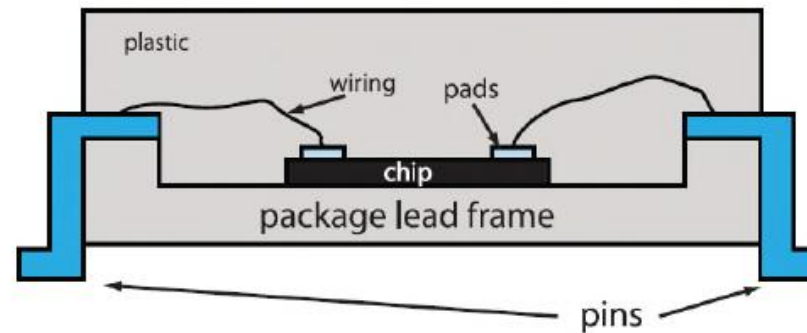
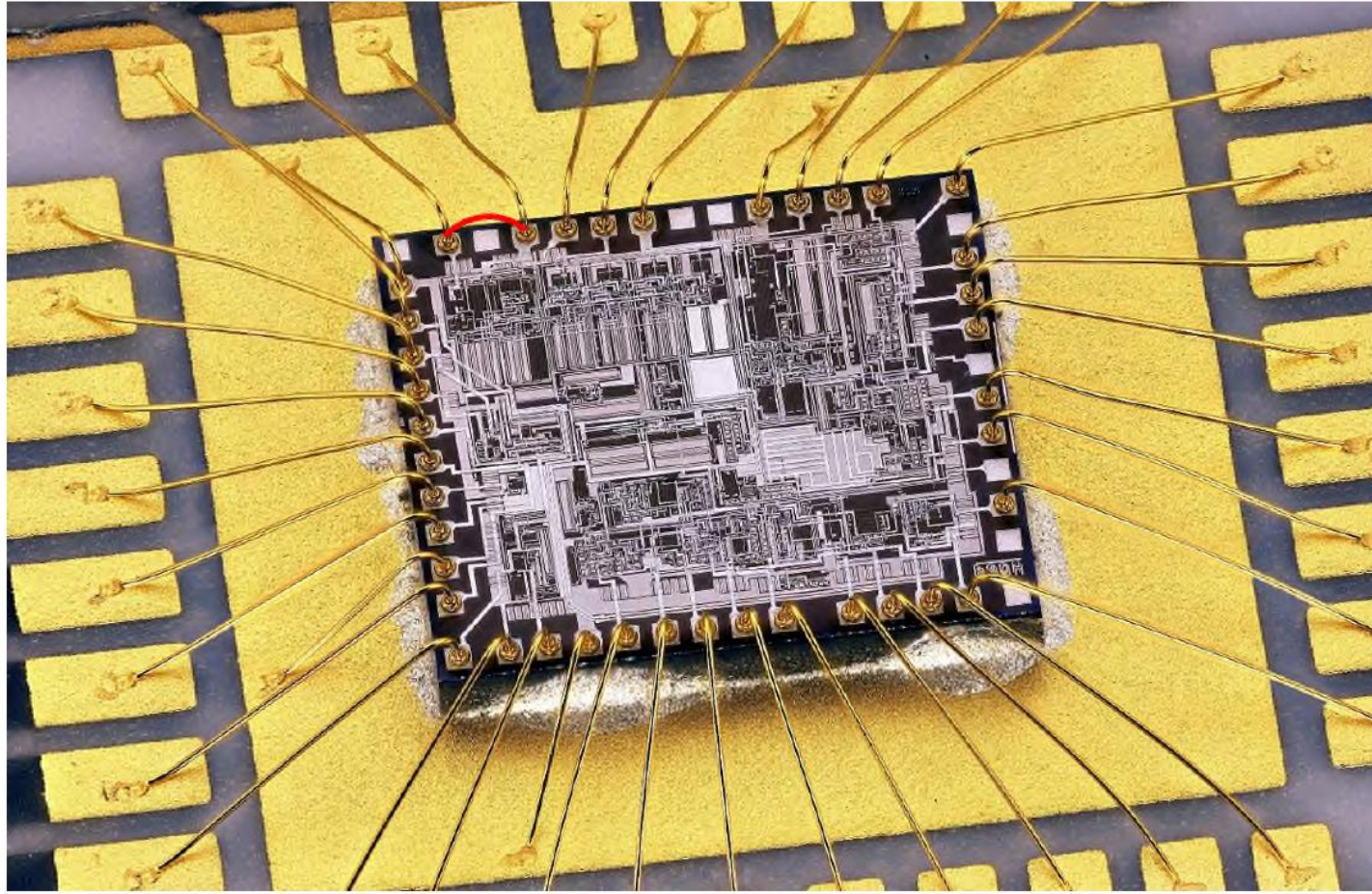


Figure 9-2. The top plastic is molten when deposited. The wires are surrounded before it hardens.

Saint, 202-203, Fig. 9-2; Reply, 8-9.

Patent Owner's “Droop” Argument Fails (Grounds 1-2)

- Petitioner's jumper bondwires are short and do not suffer from “droop”



Reply, 28

Patent Owner's "Droop" Argument Fails (Grounds 1-2)



Q. How did the '164 Patent solve the problem of bond wire sagging and droop?

...

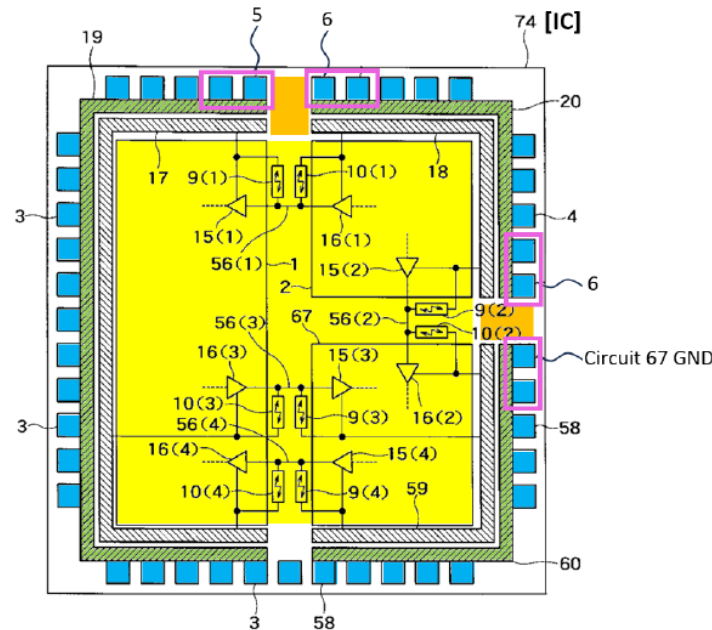
A. It's also possible that, you know, the technology of bond -- of applying -- sorry, of running bond wires in the meanwhile had gotten good enough that that conventional wisdom was not true anymore.

*Ex. 1038 (Khatri), 247:19-248:13
Reply, 29*

Patent Owner Fails to Rebut MTC for Ground 2 Regarding Haralabidis

- Patent Owner argues that Dr. Foty allegedly admitted Haralabidis does not disclose “bond pads” or methods “to connect from the inside [of] the IC of the package substrate.” But this ignores the combination.
Sur-Reply, 28.
- Ground 2 presents Yoshinaga in combination with Haralabidis. PO did not dispute that Yoshinaga discloses bond pads (blue) in Yoshinaga Fig. 6, including reference potential pads connected to reference potential lines (green).

Sur-Reply, 28.



*Yoshinaga, Fig. 6 (annotated);
Petition, 30-34; Sur-Reply, 28.*

Patent Owner Fails to Rebut MTC for Ground 2 Regarding Haralabidis

- Haralabidis discloses connecting ground rails (green) on the IC to a common ground rail (red) using bond wires.

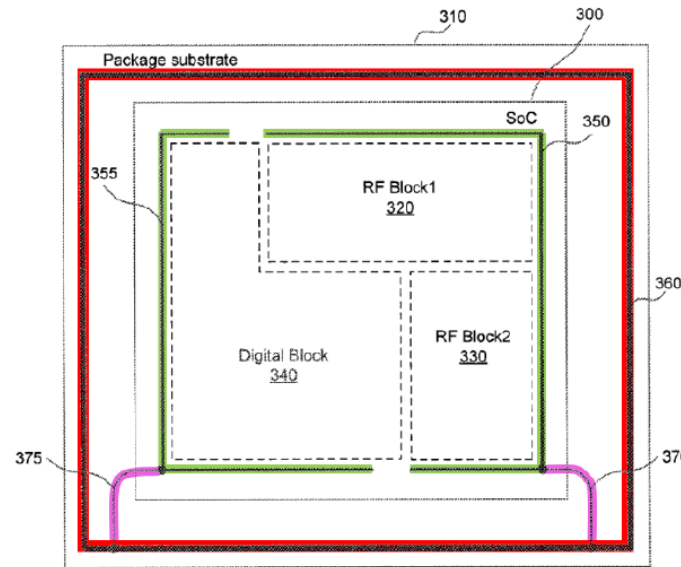


FIG. 3
Conventional Art

Haralabidis, Fig. 3, 3:14-18, 1:59-65
Petition, 56-57

- Patent Owner's argument focuses solely on Haralabidis and ignores that Haralabidis's teachings here are combined with Yoshinaga's IC.

Patent Owner Fails to Rebut MTC for Ground 2 Regarding Haralabidis

- Patent Owner misstates the Petition and the law arguing that the Petition provides no “motiva[tion]” to use bond wires to connect pads with a common ESD bus. *Sur-Reply, 29-30*
- The Petition provided motivations to use bond wires, applicable to the use of bond wires for the combination with Haralabidis and as well.

A POSITA also would have been encouraged to use bonding wires because they “fuse[] the wire to the bond pad” and result in “firmly attach[ed]” connections. Saint, 204. A POSITA would have been further encouraged to use bond wires as they “create[] a low resistance connection.” Beauchamp, [0027].

Petition, 50

Patent Owner Fails to Rebut MTC for Ground 2 Regarding Haralabidis

- Patent Owner argues Haralabidis's common ground rail would increase chip size, noise, and complexity.

POR, 55

- But this is baseless. First, Haralabidis discloses its common ground rail is off-chip in the package or PCB and thus cannot increase chip size.

*Haralabidis, 5:3-31, Fig. 6
Reply, 12*

- Second, Haralabidis explicitly teaches its common ground rail *reduces* noise/interference

low resistance to (earth) ground of the PC board ground rail [] relative to that of the connections, assists greatly in attenuating the noise/interference travelling through the same.

*Haralabidis, 5:3-31, Fig. 6
Reply, 12*

Patent Owner Fails to Rebut MTC for Ground 3 Regarding Haralabidis

- Patent Owner's only argument regarding bond wires unique to Ground 3 is that a POSITA would not have combined Saint with Haralabidis because Saint uses three an ESD buses "internal" to the chip while Haralabidis describes an off-chip common ESD bus, and allegedly a POSITA would not have "shorted" internal ESD buses to a common bus.

*POR, 65-66
Sur-Reply, 30*

- But in doing so Patent Owner again overlooks that Haralabidis teaches doing this will help reduce noise/interference, an issue Patent Owner itself repeatedly raises as a concern in arguing against using bond wires.

low resistance to (earth) ground of the PC board ground rail [] relative to that of the connections, assists greatly in attenuating the noise/interference travelling through the same.

*Haralabidis, 5:3-31, Fig. 6
Reply, 12*

- Patent Owner cannot argue against using bond wires due to alleged (unsupported) noise issues then ignore Haralabidis's disclosure that its common ESD attenuates noise

The *Juniper* and *Forest Labs* Cases are Easily Distinguished

PO's *Juniper* case is easily distinguished. POR, 64. Unlike *Juniper's* "conclusory" expert testimony, Petitioner presents multiple references that expressly disclose a common ground. Saint, Fig. CS1-99; Haralabidis, Figs. 3, 5, 5:43-6:2. And *Forest Labs* (POR, 35, 64) is unavailing because the Federal Circuit merely remanded to assess motivation to combine in the first instance. 918 F.3d at 935. PO

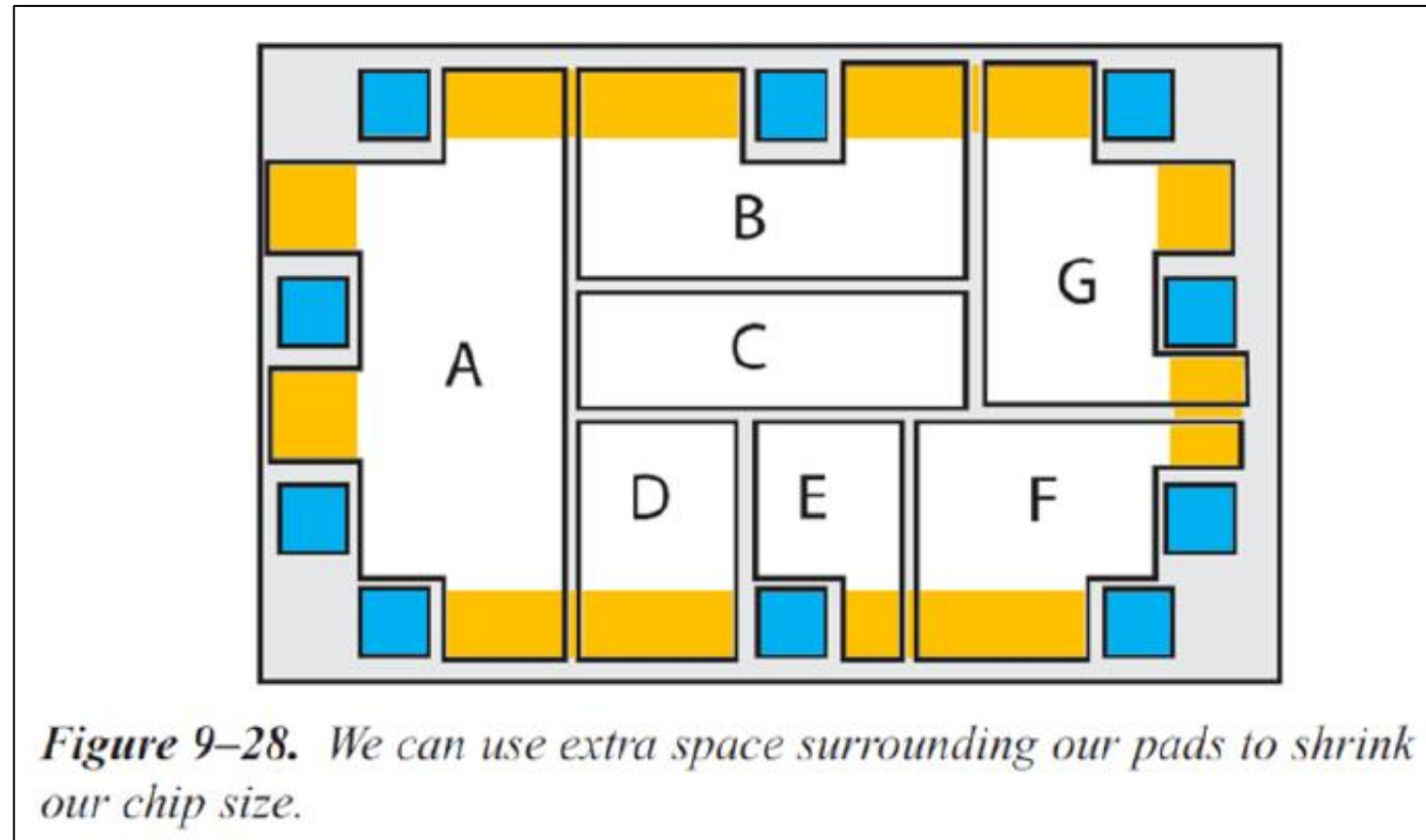
Reply, 16

Roadmap

- I. Introduction and IPR Grounds
- II. Overview of the '164 Patent and Prior Art
- III. Pad Assignment & ESD Bus Disputes
- IV. Bond Wire Disputes
- V. **Saved Area**

Overview of Saint (Grounds 1-3)

- Saint Fig. 9-28 expressly discloses using “extra space” between bond pads for circuitry to reduce chip size



*Ex. 1008 (Saint), 220-221, Fig. 9-28 (annotated)
Petition, 25-26*

Dr. Khatri Glossed Over the Prosecution History re “Saved Area”



Q. Did you review the file history in this case?

A. I might have eyeballed it, but I don't think it was something that was brought up. So, you know, it's not part of my declaration.

*Ex. 1038 (Khatri), 279:18-23
Reply, 25*

Q. Did you review the file history for the '164 Patent in preparing for your declaration or your deposition?

A. Let me see. I don't – I've gone over it tangentially at one point, but I don't think that was an issue that was brought up and is not something that I've opined on. So, I didn't look at it in any great detail.

*Ex. 1038 (Khatri), 50:20-51:6
Reply, 25*

Dr. Khatri Admits “saved area” was Well-Known



So this is a term that I've come across all through my career in my industry career, in my academic career, in my teaching career, as well as in my -- in the chips that we made from the group.

*Ex. 1038 (Khatri), 272:7-11
Reply, 26*

And in my career, I've run into this term, you know, when we're doing chip designs and such, the notion of a saved area.

*Ex. 1038 (Khatri), 269:14-20
Reply, 26*

The Claims Do Not Require “Creating” a Saved Area

A. The Claims Do Not Require “Creating” a Saved Area

PO argues the cited art fails to teach “*creat[ing]* a saved area.” POR, 45. But the Challenged Claims do not require “creating,” “forming,” or “adding” a *saved area*. Foty_Supp., ¶¶38, 43-44. Rather, they require that *the circuit area comprises at least one saved area*. See 1[f], 6[e], 8[f], 12[e].

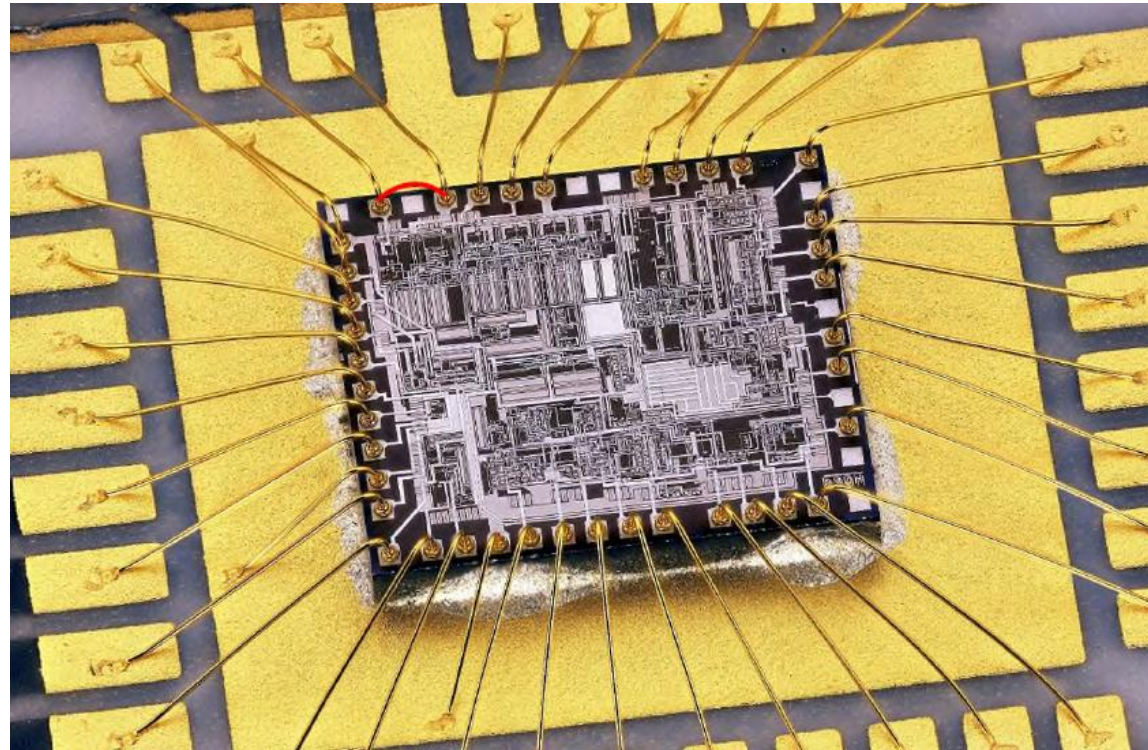
Reply, 26

Patent Owner's “Droop” Argument is a Red Herring

- Patent Owner says Saint “discouraged” jumper bond wires because long bond wires may “droop, causing a short [] circuit.”

POR, 39, 46; Sur-Reply, 8-11.

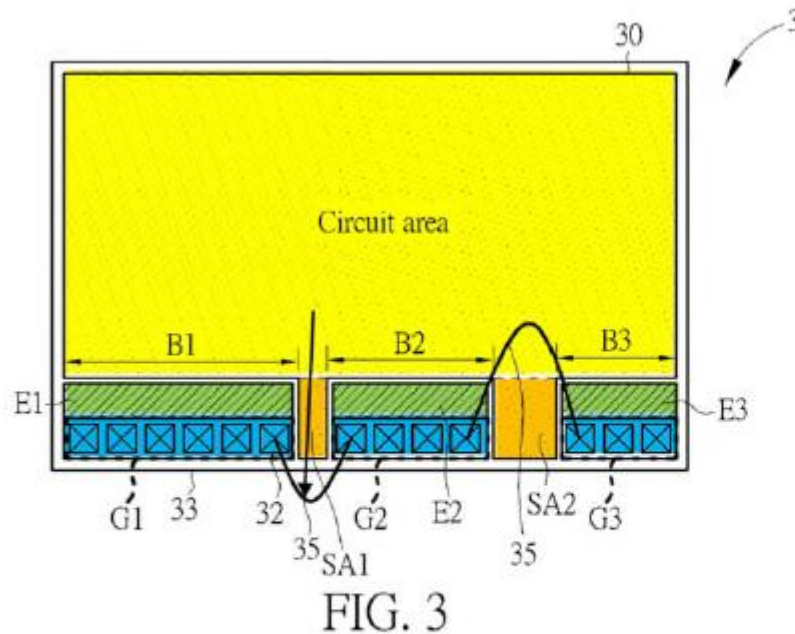
- But Petitioner's proposed bond wires are short, not long and do not “droop”



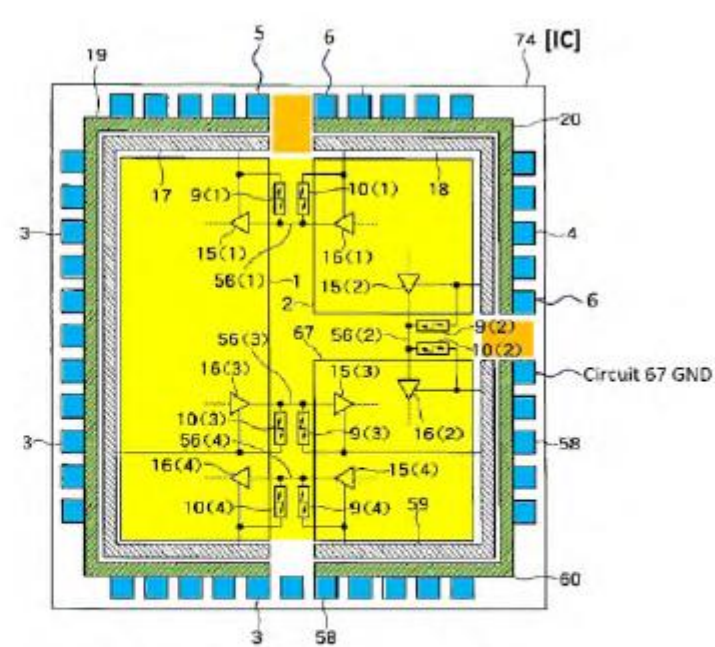
Petition, 13; Reply, 28.

Patent Owner's "Circuit Area" Argument Fails (Grounds 1 and 2)

- PO argues that Petitioner “ignores the requirement that the claimed ‘saved area’ must be within the circuit area.” POR, 41. But just as Petitioner highlighted ’164 patent Fig. 3 (left) with orange to easily identify the ***saved areas***, it did so with Yoshinaga (right).



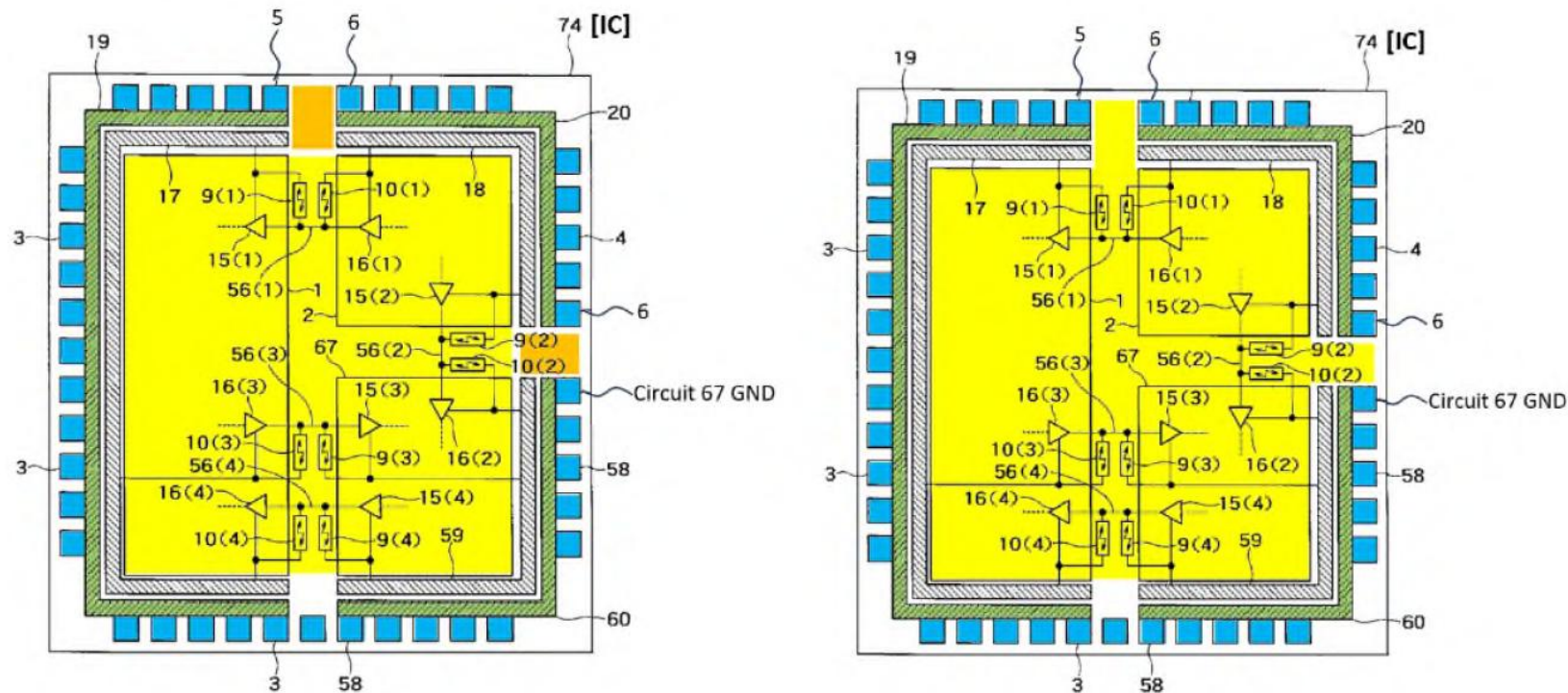
Pet., 16
(EX1001, Fig. 3, annotated)



Pet., 40
(Yoshinaga Fig. 6, annotated)

Patent Owner's "Circuit Area" Argument Fails (Grounds 1 and 2)

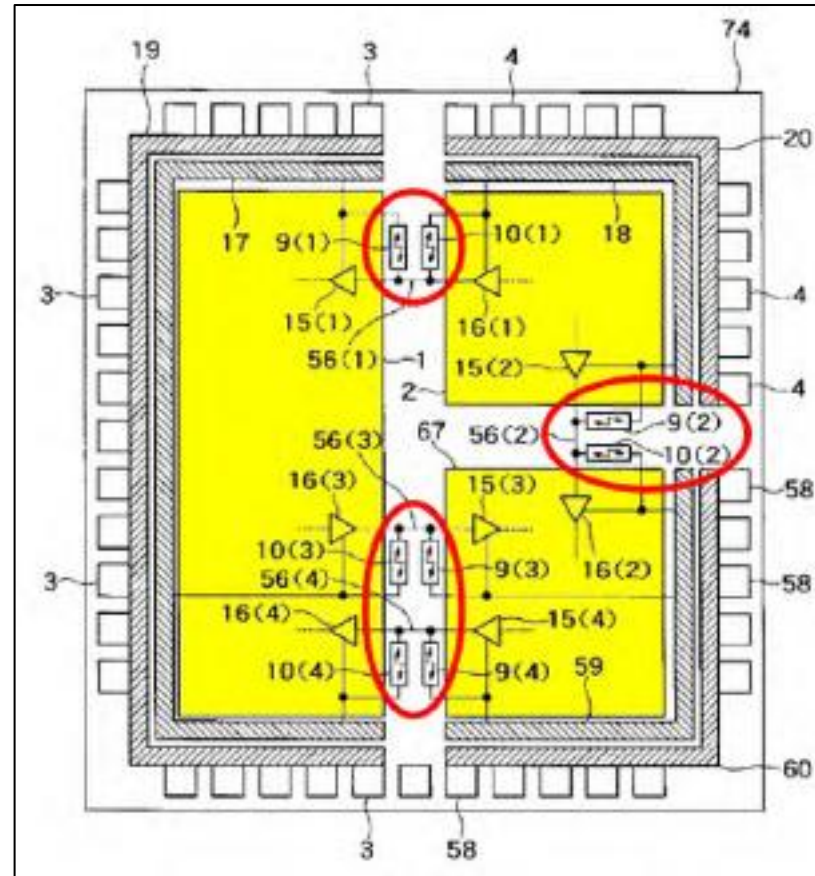
- Petitioner expressly illustrated how the claimed "saved area" was actually part of the "circuit area"



*Foty Dec. (Ex. 1003), ¶58 (Yoshinaga Fig. 6 comparison (annotated))
Reply, 29-30*

Patent Owner's "Circuit Area" Argument Fails (Grounds 1 and 2)

- While Yoshinaga Fig. 6 explains that the three blocks (highlighted in yellow below) are "circuits," Yoshinaga shows circuitry placed in between them.

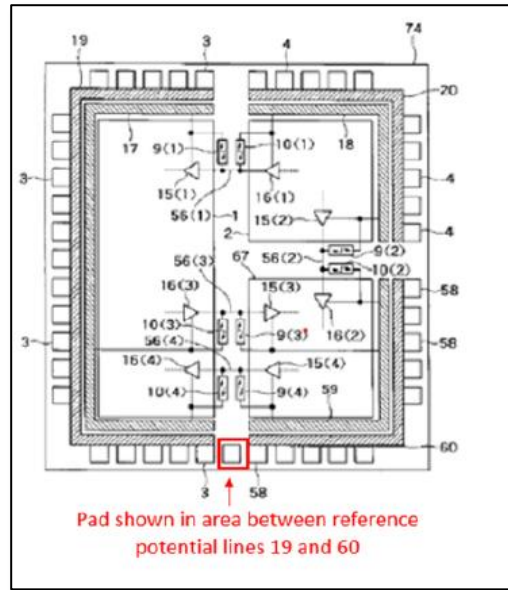


Yoshinaga, Fig. 6 (annotated); Reply, 30.

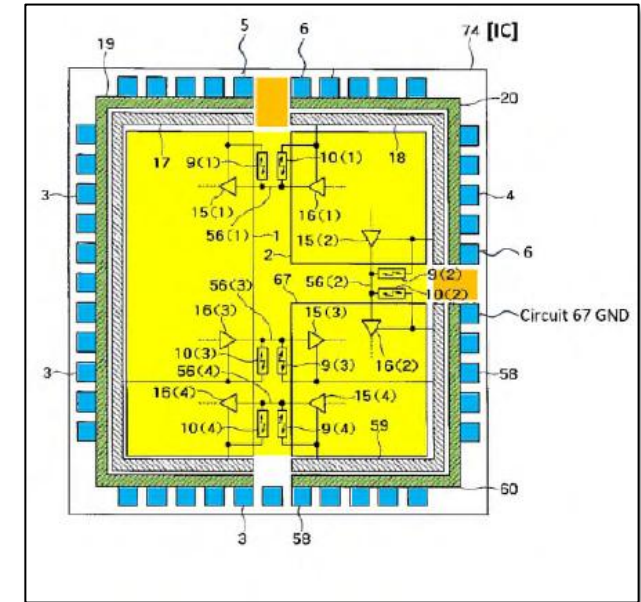
Patent Owner's “Imaginary Pad” Arguments Fails (Grounds 1-2)

- Patent Owner argues that Yoshinaga's “saved areas” included “reference potential pads” because Fig. 6 shows a pad between buses 19 and 60 (boxed in red in left figure).

POR, 42-44; Sur-Reply, 7.
- This proves Petitioner's point that ***no pads exist*** in the orange “saved areas” (right figure). Yoshinaga showed pads where the actually exist.



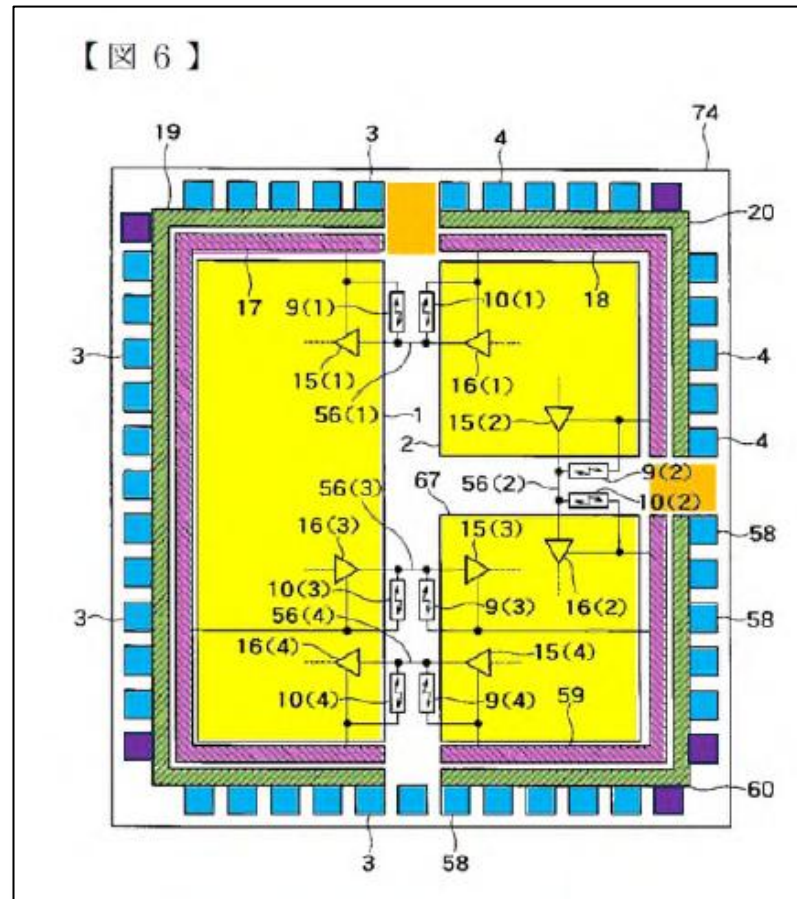
Yoshinaga, Fig. 6 (annotated)
POR, 44



Yoshinaga, Fig. 6 (annotated)
Reply, 31

Patent Owner's Extra Pad Argument Fails (Grounds 1-2)

- Even if more pads were needed, Yoshinaga Fig. 6 shows multiple other spaces where they could be added (shown in purple in the figure below)

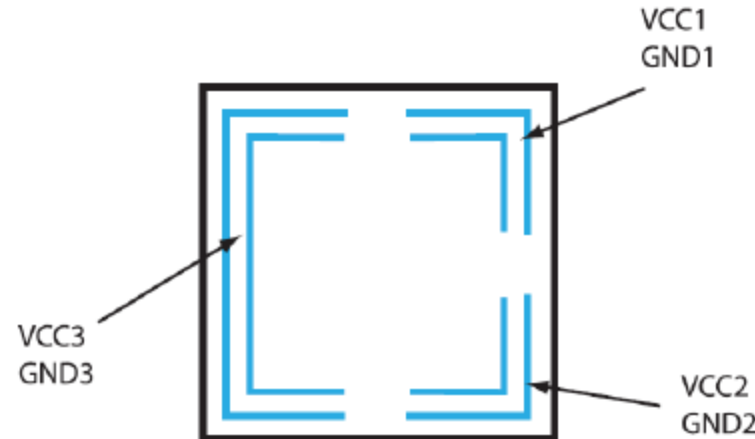


Yoshinaga, Fig. 6 (annotated); Reply, 32.

Patent Owner's "Hindsight" Argument Fails

E. PO's Hindsight Argument Fails

PO argues that Petitioner's pad assignments in modified Fig. 7-7 is "hindsight." POR, 67-69. Not so. This is neither "manipulation" nor "hindsight" because unmodified Fig. 7-7 shows a gap (*viz. saved area*) between ESD buses.



Patent Owner's Bait-and-Switch Argument Fails (Ground 3)

- Patent Owner argues Saint (Ground 3) doesn't disclose a saved area because it is not shown in Figures 7-3 through 7-6.

Sur-Reply, 7-8.

- But Petitioner did not rely on those figures to show circuitry in the saved areas. Rather, Saint Fig. 9-28 discloses placing circuitry in the “extra space surrounding [] pads”

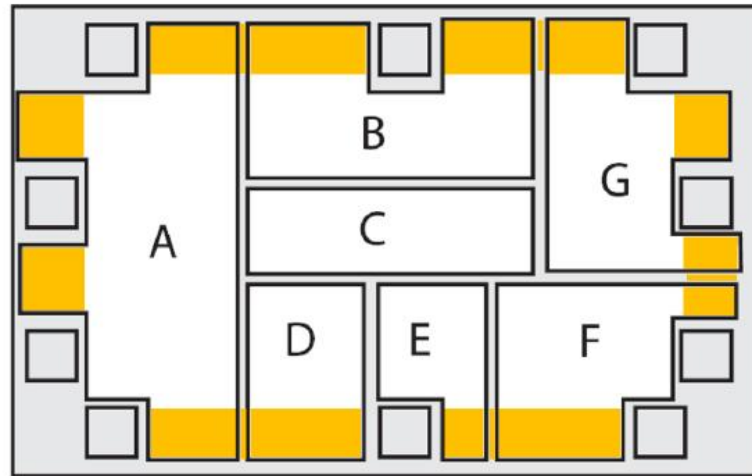


Figure 9–28. We can use extra space surrounding our pads to shrink our chip size.

Saint, 221, Fig. 9-28 (annotated); Petition 80; Reply, 33.

Patent Owner's Bodily Incorporation Argument Fails (Ground 3)

- Patent Owner argues that Saint Figs. 9-28 and 7-7 are “not the same embodiment” and thus, apparently, that the teachings cannot be combined. *Sur-Reply, 8.*
- But Petitioner never proposed bodily incorporating the figures. Rather, Petitioner proposed to ***apply the teachings*** of Fig. 9-28 to Fig. 7-7. *Petition 80-83; Reply 34*

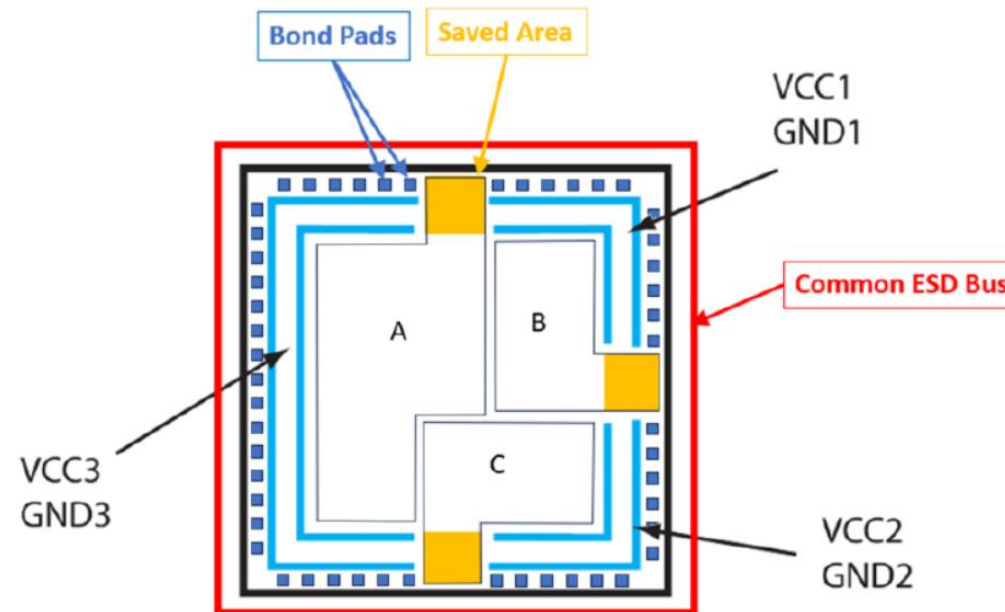


Figure 7-7. Pin-out simplification showing like protects grouped together.

Saint, Fig 7-7 (annotated); Petition 80-83.

Bodily Incorporation is Not the Test for Obviousness

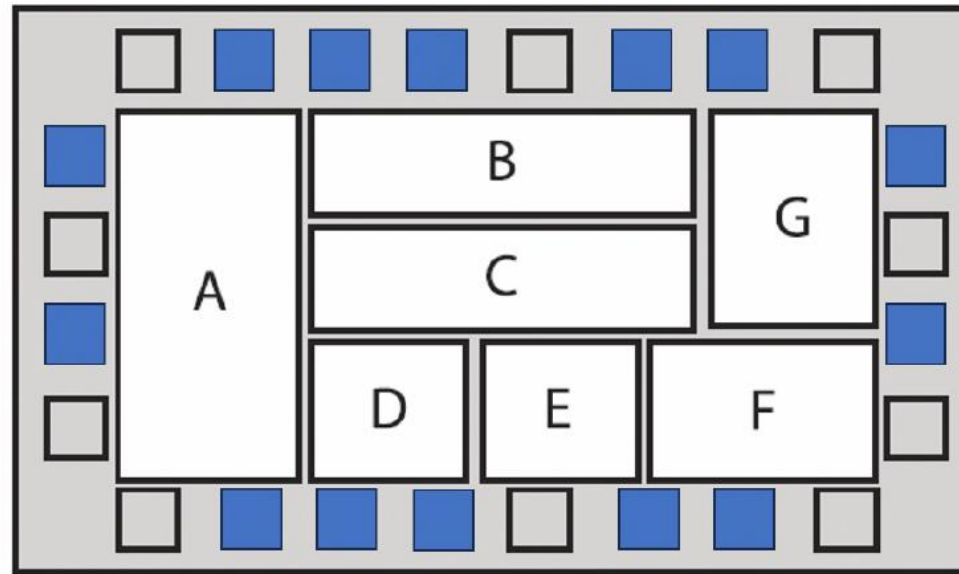
Etter's assertions that Azure cannot be incorporated in Ambrosio are basically irrelevant, the criterion being not whether the references could be physically combined but whether the claimed inventions are rendered obvious by the teachings of the prior art as a whole.

In re Etter, 756 F.2d 852, 859 (Fed. Cir. 1985)
Reply, 34



Patent Owner's "Evenly Spaced" Pad Argument Fails

PO argues Petitioner's combination is improper because Saint teaches "evenly spaced" pads. POR, 68. But this ignores Fig. 9-28, which shows unevenly spaced pads. Illustrating blue dummy/filler pads (akin to empty parking lot stalls) shows that the actual pads (grey) are unevenly spaced.



Saint Fig. 9-21 (annotated)
Reply, 34

Reducing Chip Size (and Increasing Profits) Motivated IC Design



So in that, when we're talking about a chip, we're routinely trying to minimize the area of the chip because that minimizes manufacturing cost and that's something that Yoshinaga teaches, that's something that Saint teaches as well, that minimizing the area is something that minimizes -- you know, that's desirable. So that's something that, you know, in industry when we were at Motorola we were always trying to do that. So we were always trying to save areas.

Ex. 1038 (Khatri), 270:24-271:11

Reply, 35

Reducing Chip Size (and Increasing Profits) Motivated IC Design



And of course, if [chip size is] decreased, then that would save production cost. Because production cost is more when the circuit area is more -- when the chip area is more. And production cost is less when the chip area is less.

*Ex. 1038 (Khatri), 257:9-14
Reply, 35*

Dr. Khatri Misunderstand Pad-Limited and Core-Limited Designs



Q. Does the invention in the '164 Patent have any application in the pad limited design context? ...

A. Yeah, so I did look at the '164 Patent and I did a search for, you know, core or limited and it doesn't talk about anything about a core limited design or a pad limited design, which to me, you know, reading that, you know, and also to a person of ordinary skill in the art would make sense because nothing that it teaches is restricted to one type of design or another. It's contemplated to be applicable to all designs.

Ex. 1038 (Khatri), 342:13-343:10

Reply, 32

