

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2025-00118
Patent 10,879,164 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

KOKOSKI, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

We have jurisdiction to conduct this *inter partes* review under 35 U.S.C. § 6 and issue this Final Written Decision pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Micron Technology, Inc. (“Petitioner”) does not show by a preponderance of the evidence that claims 1–14 (the “challenged claims”) of U.S. Patent No. 10,879,164 B2 (“the ’164 patent,” Ex. 1001) are unpatentable.

A. Procedural Background

Petitioner filed a Petition to institute an *inter partes* review of claims 1–14 of the ’164 patent. Paper 1 (“Pet.”). Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) filed a Preliminary Response. Paper 11. With Board authorization, Petitioner filed a Preliminary Reply (Paper 12), and Patent Owner filed a Preliminary Sur-reply (Paper 14). Pursuant to 35 U.S.C. § 314(a), we instituted an *inter partes* review of claims 1–14 on the grounds advanced in the Petition. Paper 22 (“Institution Decision” or “Dec.”). After institution of trial, Patent Owner filed a Patent Owner Response (“PO Resp.,” Paper 31), Petitioner filed a Reply (“Pet. Reply,” Paper 38), and Patent Owner filed a Sur-reply (“PO Sur-reply,” Paper 41).

We held an oral hearing on March 12, 2026, and a transcript is included in the record. Paper 49 (“Tr.”).

B. Real Parties in Interest

Petitioner identifies “Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC” as the real parties in interest. Pet. 5. Patent Owner identifies itself as the real party in interest. Paper 5 (Mandatory Notice), 1.

C. Related Matters

The parties indicate that the '164 patent is asserted in *Yangtze Memory Techs. Co., Ltd. v. Micron Tech. Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.). Pet. 5; Paper 5, 1.

D. The '164 Patent

The '164 patent, titled “Integrated Circuit Electrostatic Discharge Bus Structure and Related Method,” relates to an integrated circuit electrostatic discharge (“ESD”) structure and method that makes “full use of the circuit area.” Ex. 1001, code (54), 1:48–50. The '164 patent explains that filler cells are commonly placed at empty spaces between the input/output (“I/O”) pads and connected to an ESD bus to provide ESD protection to the integrated circuit ESD bus structure. *Id.* at 1:30–37. The filler cells, however, occupy a portion of the circuit area, which is “wasteful to the integrated circuit ESD bus structure,” and “causes the lack of flexibility for internal circuit layout design” under the “strict requirement” that the integrated circuit ESD bus structure have a rectangular shape. *Id.* at 1:38–43. To address these issues, the '164 patent provides an integrated circuit (“IC”) ESD structure that includes a circuit area, a plurality of ESD buses, a plurality of pad groups, and a plurality of bond wires configured to connect one another to another of the plurality of pad groups. *Id.* at 1:65–2:4.

Figure 3 is reproduced below.

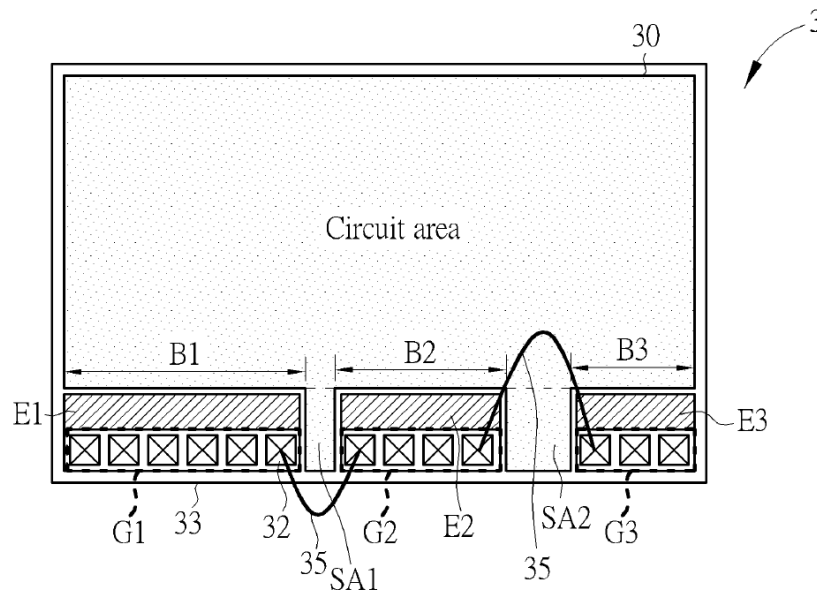


FIG. 3

Figure 3 is a schematic diagram of an integrated circuit ESD bus structure described in the '164 patent. Ex. 1001, 2:35–37. Integrated circuit ESD bus structure 3 includes circuit area 30, plurality of ESD buses E1, E2, and E3, plurality of pad groups G1, G2, and G3, and plurality of bond wires 35. *Id.* at 3:36–41. Circuit area 30 is contained within a rectangular area formed by four chip edges 33. *Id.* at 3:42–44. ESD buses E1, E2, and E3 are formed inside chip edges 33, corresponding to adjacent discontinuous boundaries B1, B2, and B3. *Id.* at 3:46–48. Saved areas SA1 (adjacent to ESD buses E1 and E2 and pads 32 of pad groups G1 and G2) and SA2 (adjacent to ESD buses E2 and E3 and pads 32 of pad groups G2 and G3) replace the filler cells commonly used in the prior art. *Id.* at 3:27–32; 4:20–22. Pad groups G1, G2, and G3 are also formed inside chip edges 33, adjacent and connected to ESD buses E1, E2, and E3. *Id.* at 3:51–54. Each of pad groups G1, G2, and G3 includes plurality of pads 32, wherein each pad 32 is an I/O pad connected to a ground or system low voltage. *Id.* at 3:61–64. One of

bonding wires 35 is configured to connect the rightmost pad 32 of pad group G1 to the leftmost pad 32 of pad group G2, and another one of bonding wires 35 is configured to connect the rightmost pad 32 of pad group G2 to the leftmost pad of pad group G3, thus “equivalently form[ing] a continuous ESD bus for the integrated circuit ESD bus structure 3.” *Id.* at 4:14–15.

According to the ’164 patent, saved areas SA1 and SA2 may be configured with circuit elements to make full use of integrated circuit ESD bus structure 3. Ex. 1001, 4:17–20. As a result, circuit area 30 “may contain the circuits with irregular shapes and different areas without increasing its area, which saves production cost.” *Id.* at 4:23–25.

E. Challenged Claims

Claims 1, 6, 8, and 12 are the independent challenged claims. Claims 6 and 12 are illustrative of the claimed subject matter, and are reproduced below.

- 6. [6.PRE] An integrated circuit structure, comprising:
 - [6.A] a circuit area;
 - [6.B] a plurality of ESD buses;
 - [6.C] a plurality of pad groups, adjacent and connected to the plurality of ESD buses; and
 - [6.D] a plurality of bonding wires configured to connect one to another of the plurality of pad groups;
 - [6.E] wherein the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

Ex. 1001, 5:42–54 (bracketed material added by Petitioner).

12. [12.PRE] A method of integrated circuit structure, comprising:

[12.A] forming a circuit area;

[12.B] forming a plurality of ESD buses;

[12.C] forming a plurality of pad groups corresponding to a plurality of discontinuous boundaries of the circuit area, wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses; and

[12.D] connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bonding wires across the circuit area;

[12.E] wherein the circuit area comprises at least one save area, each of at least one save area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area.

Id. at 6:32–47 (bracketed material added by Petitioner).

F. Asserted Grounds

Petitioner asserts that claims 1–14 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
6, 7, 12, 14	103	Yoshinaga, ¹ Saint ²
1–6, 8–11, 13	103	Yoshinaga, Saint, Haralabidis ³
1–14	103	Saint, Haralabidis

¹ Yoshinaga, JP2006-93598, published April 6, 2006 (Ex. 1006).

² Christopher Saint & Judy Saint, IC MASK DESIGN: ESSENTIAL LAYOUT TECHNIQUES (2002) (Ex. 1008).

³ Haralabidis, US 9,070,700 B2, issued June 30, 2015 (Ex. 1007).

Pet. 7–8. Petitioner relies on the Declarations of Dr. Daniel Foty (Ex. 1003; Ex. 1042) to support its contentions. Patent Owner relies on the Declaration of Dr. Sunil Khatri (Ex. 2010).

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art (“POSITA”)

would have had a bachelor of science degree in electrical engineering or similar discipline, and 2–3 years of professional experience working with (*e.g.*, researching, analyzing, designing, or teaching) ICs, or equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience and vice versa). This POSITA would have been aware of and generally knowledgeable about IC design, layout, manufacturing, packaging, and ESD protection.

Pet. 18 (citing Ex. 1003 ¶¶ 29–33). Patent Owner states that it “does not dispute Petitioner’s proposed level of a” POSITA “for purposes of this IPR.” PO Resp. 10.

In the Institution Decision, we adopted the assessment offered by Petitioner. Dec. 7. Because Petitioner’s definition of the level of skill in the art is consistent with the ’164 patent and the asserted prior art, we maintain it for purposes of this Final Written Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

B. Claim Construction

We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain

and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

Based on our review of the complete trial record and the arguments raised by the parties, we determine that it is not necessary to expressly construe any claim terms to resolve the parties' dispute. *Realtime Data*, 912 F.3d at 1375.

C. Ground 1: Asserted Obviousness over Yoshinaga and Saint

Petitioner contends that claims 6, 7, 12, and 14 would have been obvious over the combined teachings of Yoshinaga and Saint. Pet. 27–52.

1. Overview of Yoshinaga

Yoshinaga relates to a semiconductor integrated circuit having an ESD protection circuit. Ex. 1006 ¶ 1.

Figure 6 is reproduced below.

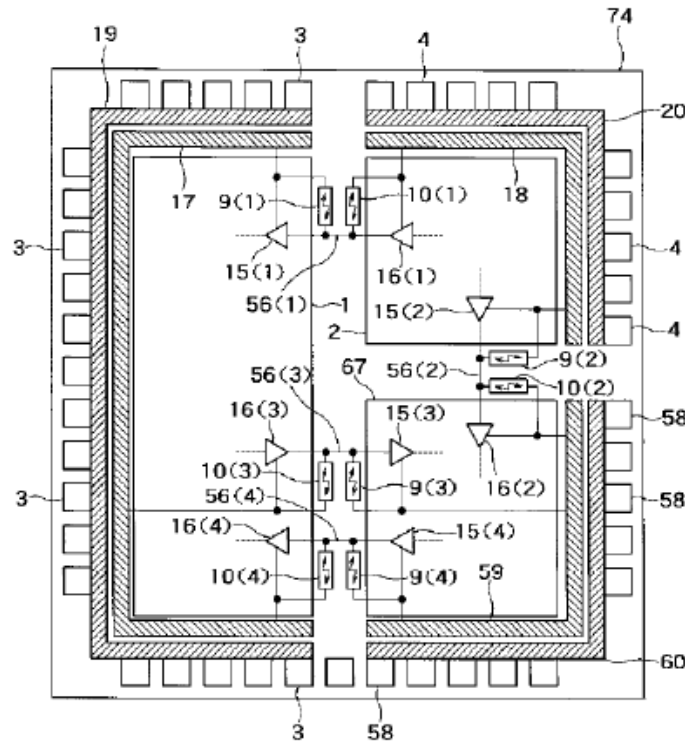


Figure 6 is a schematic diagram of an integrated circuit chip included in a semiconductor integrated circuit described in Yoshinaga. *Id.* ¶ 87.

Integrated circuit chip 74 consists of three major circuits: circuit 1, circuit 2, and circuit 67. *Id.* ¶¶ 74–75. Rectangular power supply pad 3, power supply pad 4, and power supply pad 58 are disposed near each circuit 1, 2, 67 at the periphery of the chip. *Id.* ¶ 76. The power supply line is divided into power supply line 17, power supply line 18, and power supply line 59. *Id.* ¶ 77.

The reference potential line is divided into reference potential line 19, reference potential line 20, and reference potential line 60, and is positioned outside the power supply line parallel to power supply lines 17, 18, 59. *Id.*

Signal boundary portion 15 (1) in circuit 1 is connected at signal boundary portion 16 (1) and signal line 56 (1) in circuit 2. Ex. 1006 ¶ 79. Signal line 56 (1) is connected to power supply line 17 via ESD protective

element 9 (1) and to power supply line 18 via ESD protective element 10 (1), which provides protection from ESD at the signal boundary. *Id.* Signal boundary portion 15 (2) in circuit 2 is connected at signal boundary portion 16 (2) and signal line 56 (2) in circuit 67. *Id.* ¶ 80. Signal line 56 (2) is connected to power supply line 18 via ESD protective element 9 (2) and to power supply line 59 via ESD protective element 10 (2), which provides protection from ESD at the signal boundary. *Id.* Signal boundary portion 15 (3) in circuit 67 and signal boundary portion 16 (3) in circuit 1 are connected by signal line 56 (3). *Id.* ¶ 82. Signal line 56 (3) is connected to power supply line 59 via ESD protective element 9 (3) and is connected to power supply line 17 via ESD protective element 10 (3). *Id.* ¶ 82. Signal boundary portion 15 (4) in circuit 67 and signal boundary portion 16 (4) in circuit 1 are connected by signal line 56 (4). *Id.* ¶ 83. Signal line 56 (4) is connected to power supply line 59 via ESD protective element 9 (4) and to power supply line 17 via ESD protective element 10 (4). *Id.*

ESD protective elements 9 (1) to 9 (4) and 10 (1) to 10 (4) are provided in the chip interior as shown in Figure 6. Ex. 1006 ¶ 84. Yoshinaga explains that “[n]ormally, it is difficult to use a large ESD protective element inside the chip,” but in the chip shown in Figure 6, “the size of the ESD protective element may be small . . . so it is possible to greatly improve the ESD resistance while keeping the chip size as small as possible.” *Id.* Therefore, Yoshinaga teaches,

a significant improvement in ESD resistance can be achieved by providing ESD protective elements that can be energized bi-directionally between one power supply line and the signal line and between the other power supply line and the signal line, respectively, between circuits in which the power supply lines

are separated from each other and have signal propagation paths (signal lines).

Id. ¶ 85. Yoshinaga also explains that, because the size of the ESD protective element may be small, “there is little increase in the chip size and the total number of wiring” and “increase in the unit price of the chip can be prevented as much as possible.” *Id.* ¶ 86.

2. Overview of Saint

Saint, titled *IC Mask Design: Essential Layout Techniques*, is a textbook “that provides step-by-step detailed guidance on every aspect of the mask design process.” Ex. 1008, 13.⁴ For example, Saint teaches that “[w]ire bonding is the most common method of attaching a chip to a package.” *Id.* at 207. Saint also teaches that, in a core-limited circuit design, there will be “wasted space around the edges between pads,” but if circuits are being reused, parts of the circuit elements can be re-laid in around the pads to try “to get the chip as small as possible.” *Id.* at 220–221.

3. Claim 6

Petitioner contends that the combination of Yoshinaga and Saint discloses all of the limitations of claim 6. Pet. 27–41. Petitioner relies on an annotated version of Yoshinaga’s Figure 6, reproduced below, to illustrate some of its contentions.

⁴ We refer to the page numbers added by Petitioner to the bottom right corner of the page.

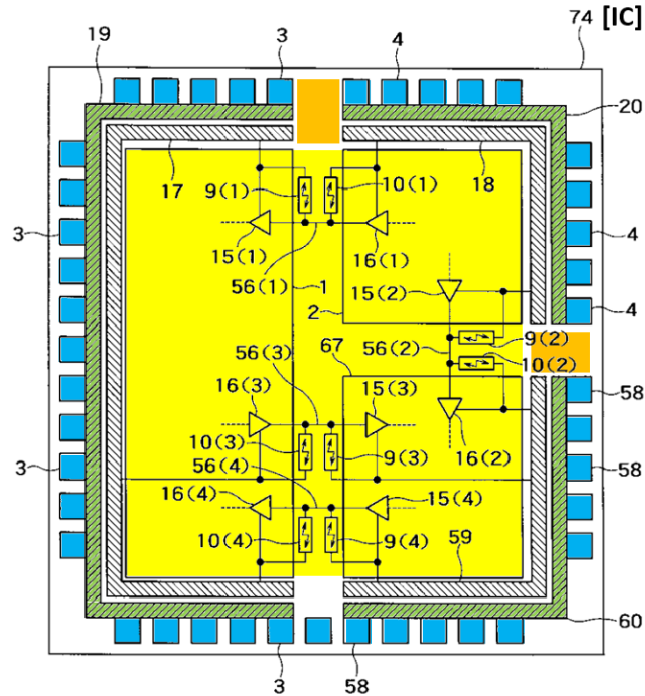


Figure 6 is a schematic diagram of an integrated circuit chip included in a semiconductor integrated circuit described in Yoshinaga with Petitioner’s addition of blue shading to the rectangles surrounding the chip, green shading to the border area below the blue rectangles, orange shading at the top and right side of the chip in the open area between ends of the green shaded area, and yellow shading to the interior of the chip. Pet. 28; Ex. 1006

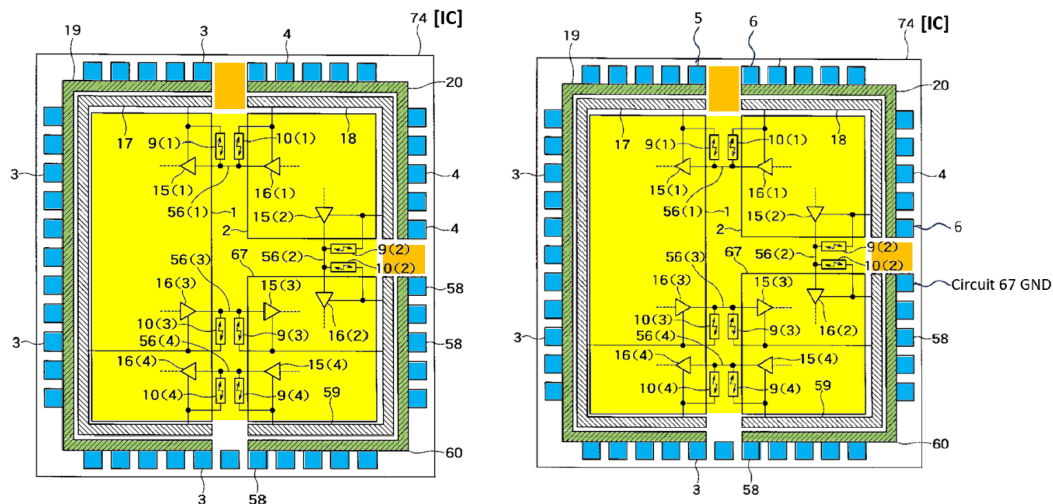
¶ 87. Referring to annotated Figure 6, Petitioner contends that Yoshinaga teaches “a circuit area” (area containing circuits 1, 2, and 67 (yellow)), “a plurality of ESD buses” (reference potential lines 19, 20, and 60 (green)), and “the circuit area comprises at least one saved area, each of at least one saved area is adjacent to two respective ESD buses of the plurality of ESD buses and respective pads of the two respective pad groups of the plurality of pad groups, and there is no ESD bus and no pad in the at least one saved area” (orange shaded area representing the saved area shown adjacent to reference potential lines 19, 20, 60 (ESD buses, green) and two respective

pad groups (blue)). Pet. 27–30, 39–41 (and evidence cited therein). Patent Owner argues in response that the combination of Yoshinaga and Saint does not teach the following limitations of claim 6: (1) “a plurality of pad groups, adjacent and connected to the plurality of ESD buses” (PO Resp. 15–27); (2) “a plurality of bonding wires configured to connect one to another of the plurality of pad groups” (*id.* at 27–39); and (3) “the circuit area comprises at least one saved area” (*id.* at 40–47). We focus our analysis on the “a plurality of pad groups, adjacent and connected to the plurality of ESD buses” limitation, as it is dispositive of the controversy between the parties.

With respect to the “a plurality of pad groups, adjacent and connected to the plurality of ESD buses” limitation of claim 6, Petitioner asserts that Yoshinaga’s Figure 6 “shows various ‘pads’ (blue), such as power supply pads 3, 4, and 58.” Pet. 31 (citing Ex. 1006 ¶¶ 76–77, Fig. 6). Petitioner further asserts that “Yoshinaga explains that ‘[r]eference potential pads are not shown [in Fig. 6] to simplify the drawing,’ but they are shown in Figs. 1–4 (numerals 5, 6, 39, 40).” *Id.* (citing Ex. 1006 ¶ 78, Figs. 1–4) (alteration in original). Petitioner notes that “Yoshinaga Fig. 6 is an illustrative rendering, not intended to necessarily reflect the exact number of pads present or their electrical connections,” and, “even though ‘power supply pads’ 3, 4, and 58 are shown next to the ground rail, a POSITA would have understood they are connected to the power rails 17, 18, and 59 (shown in Figs. 1–4) and not ground rails 19, 20, and 60, as doing so would create a short circuit between power and ground.” *Id.* (citing Ex. 1003 ¶ 136). Accordingly, Petitioner contends, “a POSITA would have understood the reference pads (*e.g.*, pads 5 and 6) were connected to ground rails 19, 20, and 60” and “the pads labelled 3, 4, and 58 could just as readily be used as reference pads, and selecting which pads to use for ground,

power, signals, etc. is a design choice that depends on factors like chip size, the number of I/O signals, and the number of pads available.” *Id.* (citing Ex. 1003 ¶¶ 137–139).

Petitioner then contends that “a POSITA would have understood, or at least found it obvious, to use the pads immediately next to the saved areas as reference pads (*e.g.*, pads 5 and 6) as pad assignments were left to the designer’s discretion” in order “to preserve Yoshinaga’s saved area for other circuitry as taught by Saint.” Pet. 31–32 (citing Ex. 1003 ¶¶ 137–139; Pet. 19–23 (§ IX.A)). Petitioner alters the labels on its annotated version of Yoshinaga’s Figure 6 to illustrate its contentions. Reproduced below is Petitioner’s annotated version of Figure 6 before Petitioner’s alteration (left) and after (right).



Annotated Figure 6, on the left, maintains the labels provided in Yoshinaga, and altered annotated Figure 6, on the right, (a) changes the label on the pad (blue) to the left of the saved area (orange) at the top of the chip from “3” to “5”, (b) removes the “4” label from the pad (blue) to the right of the saved area (orange) at the top of the chip, (c) labels the pad (blue) immediately to the right of the saved area (orange) at the top of the chip “6”, (d) changes the

label on the pad (blue) above the saved area (orange) on the right side of the chip from “4” to “6”, and (e) changes the label on the pad (blue) below the saved area (orange) on the right side of the chip from “58” to “Circuit 67 GND.” Pet. 29, 31–32; Ex. 1006, Fig. 6. Referring to altered annotated Figure 6 and Yoshinaga Figure 2, Petitioner concludes that “Yoshinaga discloses a plurality of pad groups (*e.g.*, pads in Fig. 6 corresponding to voltage reference pads 5, 6, 39, and/or 40) connected to the plurality of ESD buses (*e.g.*, reference lines 19, 20, and 60, each with wiring resistors 21, 22, 23, and 24).” Pet. 34 (citing Ex. 1006 ¶¶ 35, 36, 53–62, 88, Fig. 2; Ex. 1003 ¶ 143) (emphases omitted); Tr. 11:13–16 (“If you look at Figure 2 on the left, which is the schematic. Down here in the lower left, there's a bond pad 5. In the lower right, there's a bond pad 6, and Yoshinaga says these are the reference potential pads.”).

Petitioner contends that Yoshinaga Figure 6 “does not identify the ‘[r]eference potential pads’ (*e.g.*, pads 5, 6, 39, 40 in Figs. 1–4)” in order “to simplify the drawing,” but a POSITA would have understood that reference pads were present in the areas shown by the blue pads in annotated Figure 6 and not located in the orange saved spaces. Pet. 20 (citing Ex. 1006 ¶¶ 76, 78; Ex. 1003 ¶¶ 136–139, 171–172). Petitioner contends that Yoshinaga’s statement that “[r]eference potential pads are not shown” in Figure 6 “simply means they are not labelled.” *Id.* (citing Ex. 1006 ¶ 78; Ex. 1003 ¶ 172). Petitioner contends that a POSITA would have understood that “the pads labelled 3, 4, and 58 could just as readily be used as reference pads, and selecting which pads to use for ground, power, signals, etc. is a design choice that depends on factors like chip size, the number of I/O signals, and the number of pads available.” *Id.* at 31 (citing Ex. 1003 ¶¶ 137–139). Petitioner also contends that “a POSITA would have

understood, or at least found it obvious, to use the pads immediately next to the saved areas as reference pads (*e.g.*, pads 5 and 6) as pad assignments were left to the designer’s discretion.” *Id.* (citing Ex. 1003 ¶¶ 137–139). According to Petitioner, a POSITA would have placed the reference pads next to the saved areas “to preserve Yoshinaga’s saved area for other circuitry as taught by Saint.” *Id.* at 31–32 (citing Ex. 1003 ¶ 137).

Patent Owner argues that Petitioner has not met its burden to show that its combination of Yoshinaga and Saint teaches pad groups that are “*adjacent* as well as connected to ESD buses.” PO Resp. 17 (citing Pet. 33). Patent Owner points to the testimony of Dr. Foty, who “admits that Yoshinaga ‘explicitly says nothing’ about ‘the location of the reference potential pads.’” *Id.* (citing Ex. 2011, 264:4–11). Patent Owner argues that Petitioner’s contention that Yoshinaga’s power supply pads “could” be replaced with reference potential pads is not sufficient to establish a motivation to modify Yoshinaga.” PO Resp. 19 (citing Pet. 31). Patent Owner also argues that “Petitioner’s reliance on ‘design choice’ [does not] excuse it from establishing that there would have been a motivation to modify Yoshinaga’s Figure 6 as it proposes.” *Id.* at 20 (citing Pet. 31). Patent Owner notes that Petitioner identifies a number of factors that would inform a designer’s choice of pad placement, but does not “consider or analyze any of these factors when determining whether a POSITA would be able to support changing power supply pads 3, 4, and 58 or other pads in Yoshinaga Figure 6 into reference potential pads.” *Id.* at 20–21 (citing Ex. 2010 ¶¶ 63–71).

Patent Owner further argues that power supply pads and reference potential pads “are connected to different circuit elements and serve entirely different purposes.” PO Resp. 22 (citing Ex. 2010 ¶¶ 44–45). In that regard,

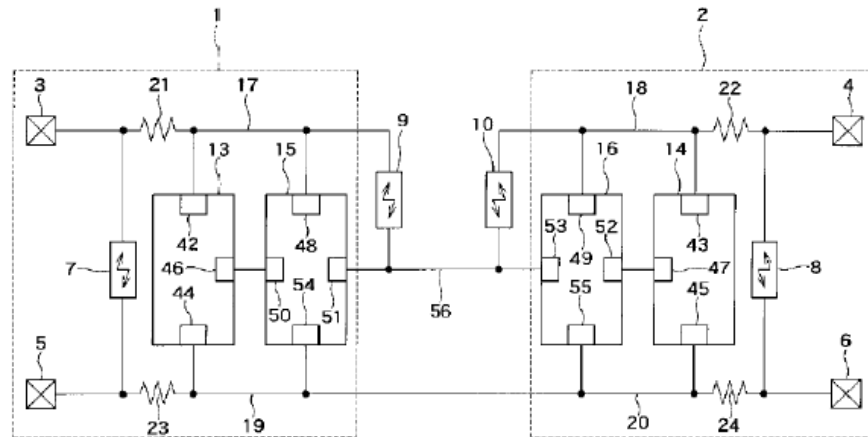
Patent Owner argues that Yoshinaga's statement that "reference potential pads are not shown to simplify the drawing" in Figure 6 means that the pads shown in Figure 6 (such as power supply pads 3, 4, and 58) are not reference potential pads. *Id.* (citing Ex. 1006 ¶ 78; Ex. 2010 ¶¶ 41–44). Patent Owner argues that Petitioner's assertion that "not shown" means "not labelled" is unsupported, and that "there are many other pads that are 'not labelled' in Figure 6" that Yoshinaga does not identify as being "not shown" because they are "not labelled." *Id.* According to Patent Owner, "Yoshinaga consistently uses the term 'not shown' to refer to elements that do not appear in a figure." *Id.* (citing Ex. 1006 ¶¶ 84, 66).

After considering the parties' arguments and evidence of record, and weighing the testimony of Dr. Foty and Dr. Khatri, we are not persuaded that Petitioner establishes, by a preponderance of the evidence, that Yoshinaga discloses "a plurality of pad groups, adjacent and connected to the plurality of ESD buses" or that a POSITA would have been motivated to substitute reference pads for the power supply pads shown in Yoshinaga Figure 6.

As an initial matter, we note that Patent Owner does not dispute that Yoshinaga discloses reference pads or pad groups, or that Yoshinaga's reference pads are connected to ESD buses. The parties' dispute is centered on the physical location of Yoshinaga's reference pads, namely, whether they are adjacent to the ESD buses. *See* PO Resp. 18 ("None of the Figures in Yoshinaga depict the physical location of the reference potential pads, let alone where they are physically located relative to the ESD buses, and thus do not disclose reference potential pads 'adjacent . . . to the plurality of ESD buses.'") Because Petitioner's contentions in this regard are based on

Yoshinaga Figure 6, we turn first to the question of whether reference pads are depicted but not labeled in Figure 6 as Petitioner asserts.

Yoshinaga states that the schematic diagram in Figure 6 includes the semiconductor integrated circuit of Figure 1, which is reproduced below:



Ex. 1006 ¶ 74, Fig. 1. Figure 1 is a block diagram showing the configuration of a semiconductor integrated circuit according to one of Yoshinaga's embodiments. *Id.* ¶¶ 12, 87. Figure 1 includes, in relevant part, circuits 1 and 2, power supply pads 3 and 4, reference potential pads 5 and 6, ESD protective elements 7 and 8, and internal circuits 13 and 14. *Id.* ¶¶ 13, 14, 24, 25, 88. It follows, then, that the integrated circuit chip schematically depicted in Figure 6 includes the elements of the circuit in Figure 1.

Yoshinaga explains, however, that Figure 6 does not illustrate all of the elements of the integrated circuit chip:

Reference potential pads are not shown to simplify the drawing. In addition, ESD protective elements (e.g., ESD protective elements 7, 8 in FIG. 1) connected between the power supply pad and the reference potential pad are usually located on the underside of the power supply ring (in a direction perpendicular to the paper surface), but the illustration has been omitted to simplify the drawing.

Ex. 1006 ¶ 78.

Based on these disclosures in Yoshinaga, we disagree with Petitioner that the reference potential pads are simply not labelled in Yoshinaga Figure 6. *See* Pet. 20–21. Yoshinaga likens its statement that reference potential pads are not shown in Figure 6 to its statement that ESD protective elements shown in Figure 1 are omitted from Figure 6 “in order to simplify” Figure 6. Ex. 1006 ¶ 78. Likening “not shown” to “omitted” is consistent with the ordinary understanding that “not shown” indicates that the element is not depicted. It is also consistent with Yoshinaga’s subsequent description of the omitted ESD protective elements as being “not shown” in Figure 6. *See id.* ¶ 84 (stating that “previous ESD protective elements (not shown in FIG. 6) are provided in the underside of the power supply ring near the periphery of the chip as described above.”).

Moreover, Petitioner does not direct us to, nor do we discern, anything in Yoshinaga that supports its contention that “not shown” means “not labelled.” Pet. 20–21; Ex. 1003 ¶¶ 136, 172. In that regard, Petitioner contends that “[g]round pads 5 and 6 are expressly shown and labelled in Fig. 1 (and Figs. 2 and 4)” and “Fig. 6 implements Fig. 1, and thus has ground pads.” Pet. Reply 18 (citing Ex. 1006 ¶¶ 55, 87, Fig. 1). Although it is true that the *integrated circuit chip* described by Yoshinaga Figure 6 has the reference pads (and other elements) shown in Figure 1, it does not necessarily follow that those references pads are shown in *the schematic diagram* of the integrated circuit chip shown in Figure 6.

Petitioner also argues that because Yoshinaga identifies the elements in Figure 6 by reference numeral in the paragraphs immediately prior to the paragraph that states that reference pads are “not shown,” “a POSITA would have understood that Yoshinaga is simply saying the ground pad *labels* are

not shown, not that ground pads are missing.” Pet. Reply 18 (citing Ex. 1006 ¶¶ 76, 77; Ex. 1042 ¶¶ 145–148, 163, 179). Petitioner does not adequately explain, however, why the order of the paragraphs identifying the elements of Yoshinaga Figure 6 would have lead a POSITA to understand “not shown” to mean “not labelled.” Petitioner’s argument also overlooks Yoshinaga’s statement that reference pads are not shown “in order to simplify the drawing.” *Id.*; Ex. 1006 ¶ 78. Not labelling additional pads (such as reference pads 5 and 6) in Yoshinaga Figure 6 would not “simplify the drawing” in the same way that omitting reference pads (or other elements) from the drawing would.

For these reasons, we find that Yoshinaga’s statement that “[r]eference potential pads are not shown to simplify the drawing” indicates that reference potential pads are not depicted in Yoshinaga Figure 6, and determine that Yoshinaga Figure 6 does not disclose “a plurality of pad groups, adjacent and connected to the plurality of ESD buses” as recited in claim 6.

Petitioner also argues that a POSITA would have understood that power supply pads 3, 4, and 58 in Yoshinaga “could just as readily be used as reference pads” and it would have been obvious “to use the pads immediately next to the saved areas as reference pads (*e.g.*, pads 5 and 6) as pad assignments were left to the designer’s discretion.” Pet. 31 (citing Ex. 1003 ¶¶ 137–139). Petitioner asserts that “selecting which pads to use for ground, power signals, etc. is a design choice that depends on factors like chip size, the number of I/O signals, and the number of pads available.” Pet. 31 (citing Ex. 1003 ¶ 137–139). Petitioner states that such discretion would be to preserve Yoshinaga’s saved area for other circuitry as taught by Saint. Pet. 31–32 (citing Ex. 1003 ¶¶ 137–139; Pet. 19–23 (§ IX.A)).

Neither Petitioner nor Dr. Foty adequately explain, however, why a POSITA would have made this specific design choice, namely, replacing power supply pads 3, 4, and 58 with reference pads. Pet. 31; Ex. 1003 ¶¶ 137–139; *see also Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1069 n.4 (Fed. Cir. 2018) (“Merely stating that a particular placement of an element is a design choice does not make it obvious.” (quoting *Cutsforth, Inc. v. MotivePower, Inc.*, 636 Fed. Appx. 575, 578 (Fed. Cir. 2016))). Petitioner offers the general proposition that pad assignments are left to the designer’s discretion, but this does not provide a reason why a POSITA would have been motivated to modify Yoshinaga Figure 6 as proposed. Pet. 31; Ex. 1003 ¶¶ 137–139. We have determined that Yoshinaga does not show (rather than does not label) reference pads. Because all of Yoshinaga’s illustrated pads are power supply pads, Petitioner’s proposed reassignment of pads would not be a simple matter of rearrangement of an existing mixture of power supply and reference pads, but require that reference pads be imported from elsewhere, and power supply pads be moved to some unspecified location. Petitioner’s arguments and Dr. Foty’s testimony with respect to the modification of Yoshinaga Figure 6 leave an analytical gap that does not apprise us of why a POSITA would have modified Yoshinaga Figure 6 to include reference pads in the place of power supply pads 3, 4, and 58.

We agree with Patent Owner that none of Petitioner’s rationales explain why replacing any given power supply pad with a reference pad would preserve a saved area. As Patent Owner states,

“[P]reserv[ing] Yoshinaga’s saved area” would, at most, motivate a POSITA not to place the reference potential pads in Yoshinaga’s alleged “saved area” (highlighted orange by petitioner). Khatri2 ¶¶60-63. It does not provide any motivation

for a POSITA to take Yoshinaga's power supply pads 3, 4, and 58 and change them into reference potential pads, as proposed, nor does it explain how such a significant change would work.

PO Resp. 21.

In its Reply, Petitioner lists explanations of “why a POSITA would have made the proposed pad assignments” in Yoshinaga Figure 6 and where in the Petition those arguments were made. Pet. Reply 22–23 (citing Pet. 31–32, 34–39, 46–47, 49–50; Ex. 1003 ¶¶ 200–204; Ex. 1008, 206–210, Fig. 9-28; Ex. 1042 ¶ 155). As Patent Owner notes, “none of these rationales pertain to altering pad assignments.” PO Sur-reply 16. For example, Petitioner argues that “Yoshinaga shows ground pads electrically connected.” *Id.* at 22. Petitioner does not adequately explain, however, how Yoshinaga's ground-pad electrical connections would have motivated a POSITA to replace Yoshinaga's supply pad with ground pads as Petitioner contends. *See* Pet. 33 (“Yoshinaga Figs. 1–4 confirm that pad groups (comprising reference voltage pads 5 and 6 (shown in Fig. 2 below) and/or pads 39 and 40 (from Fig. 3)) *connected to* reference potential lines 19, 20, and 60 (green).”). Petitioner also contends that “bondwires are a ubiquitous, affordable and reliable means of connecting bond pads.” Pet. Reply 22. Petitioner's arguments in this respect are directed to Petitioner's contentions that it would have been obvious to wire-bond Yoshinaga's pad groups to each other as required by the “a plurality of bonding wires configured to connect one to another of the plurality of pad groups” limitation of claim 6. *See* Pet. 35–38 (arguing that wire bonding pads to one another was known to a POSITA). In any event, that wire bonding was well known does not support Petitioner's argument that it would have been obvious to locate Yoshinaga's reference pads adjacent to the ESD buses. Likewise,

Petitioner’s argument that “Saint teaches minimizing bondwire distance” does not provide any motivation for a POSITA to take Yoshinaga’s power supply pads 3, 4, and 58 and change them into reference potential pads, as proposed.

For these reasons,⁵ after considering Petitioner’s and Patent Owner’s positions, as well as their supporting evidence, we determine that Petitioner does not show, by a preponderance of the evidence, that claim 6 would have been obvious over the combined teachings of Yoshinaga and Saint.

4. Claims 7, 12, and 14

Petitioner also contends that the combined teachings of Yoshinaga and Saint disclose or suggest all of the limitations of claim 7, which depends from claim 6, independent claim 12, and claim 14, which depends from claim 12. Pet. 43–48. Independent claim 12 recites that “the plurality of pad groups are adjacent and connected to the plurality of ESD buses.” Ex. 1001, 6:37–38. Petitioner relies on the same arguments with respect to this limitation in claims 12 as it does for the similar limitation in claim 6 discussed above. Pet. 44 (“The part of this limitation claiming *a plurality of pad groups . . . wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses* contains the same limitation as recited in [6.C], and Yoshinaga discloses it for the same reasons.”).

⁵ Because we determine that Petitioner does not adequately establish that Yoshinaga teaches “a plurality of pad groups, adjacent and connected to the plurality of ESD buses” or that a POSITA would have been motivated to substitute reference pads for the power supply pads shown in Yoshinaga Figure 6, we do not reach Patent Owner’s arguments that the combination of Yoshinaga and Saint does not teach the “a plurality of bonding wires configured to connect one to another of the plurality of pad groups” or “the circuit area comprises at least one saved area” limitations of claim 6.

Accordingly, for the same reasons set forth above with respect to claim 6, we determine that Petitioner does not establish by a preponderance of the evidence that claims 7, 12, and 14 would have been obvious over the combined teachings of Yoshinaga and Saint. *See* Section II.C.3, *supra*.

D. Ground 2: Asserted Obviousness over Yoshinaga, Saint, and Haralabidis

Petitioner contends that claims 1–6, 8–11, and 13 would have been obvious over the combined teachings of Yoshinaga, Saint, and Haralabidis. Pet. 52–67.

1. Overview of Haralabidis

Haralabidis “is directed to an electronic device with electrostatic discharge (ESD) and interference suppression.” Ex. 1007, 1:16–18. Haralabidis teaches that “[t]he ESD configuration can be used in integrated circuits configured for system-on-chip (SoC) and system-in-package (SiP) implementations,” and that “electronic interference from both internal and external sources is reduced with respect to the integrated circuits included in the SoC and SiP implementations.” *Id.* at 1:35–41.

Figure 3 is reproduced below.

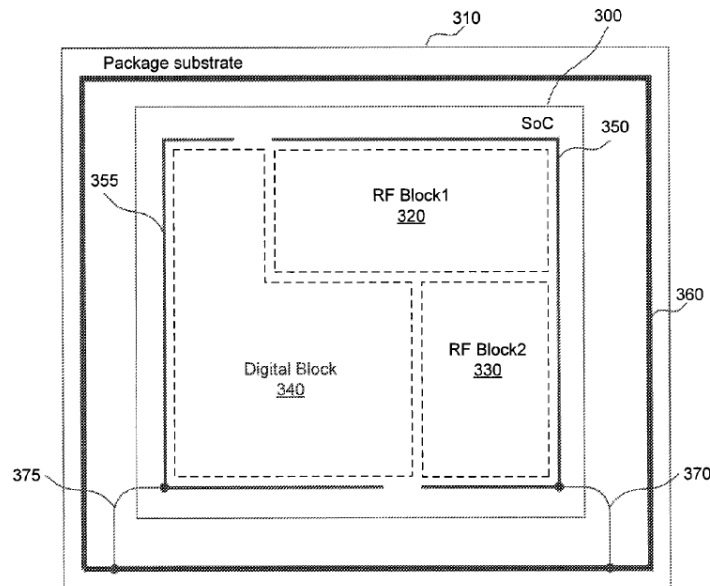


FIG. 3
Conventional Art

Figure 3 illustrates conventional SoC 300 encapsulated in package substrate 310. Ex. 1007, 2:13–14, 3:9–10. SoC 300 includes RF block1 320, RF block2 330, digital block 340, segmented ground rails 350 and 355, and common ground rail 360. *Id.* at 3:11–15. Segmented ground rails 350 and 355 are independently connected to common ground rail 360 via separate connections 370 and 375, respectively. *Id.* at 3:15–18.

Haralabidis teaches that segmented ground rails 350 and 355 minimize interference from a noisy aggressor block to other blocks on the SoC. *Id.* at 3:19–21. For example, Haralabidis explains that known noisy aggressor blocks like digital block 340 are connected to segmented ground rail 355, and are thereby isolated from another block like RF block1 or RF block2, which are susceptible to noise/interference and are connected to segmented ground rail 350. *Id.* at 3:21–26.

Figure 5 is reproduced below.

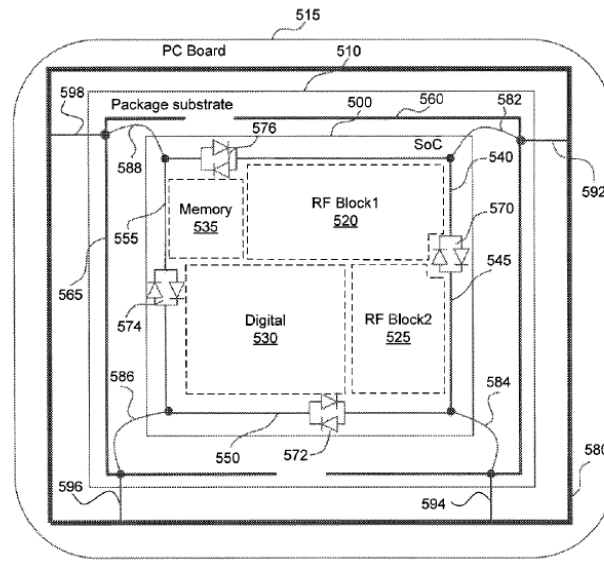


FIG. 5

Figure 5 illustrates an exemplary SoC according to an embodiment described in Haralabidis. Ex. 1007, 2:17–18. SoC 500 is encapsulated in package substrate 510, which is placed on and/or connected to printed circuit (PC) board 515. *Id.* at 3:65–4:2. Soc 500 includes RF block1 520, RF block2 525, digital block 530, memory block 535, and segmented ground rails 540, 545, 550, and 555 that are connected to the respective ground node of RF block1 520, RF block2 525, digital block 530, and memory block 535. *Id.* at 4:2–6. Segmented ground rails 540, 545, 550, and 555 are connected to each other via anti-parallel diodes 570, 572, 574, and 576, and are also connected to segmented package ground rails 560 and 565 through connections 582, 584, 586, and 588, respectively. *Id.* at 4:13–17. Segmented package ground rails 560 and 565 are connected to PC board common ground rail 580 through connections 592, 594, 596, and 598. *Id.* at 4:17–20. Haralabidis explains that “[t]he assembly, including the SoC 500 and package substrate, with or without the PC board may be

referred to as an IC assembly, or electronic device, as will be understood by those skilled in the arts.” *Id.* at 4:23–26.

2. Analysis

Petitioner contends that “most elements of claims 1 and 6 are identical and are satisfied for the same reasons” set forth with respect to Petitioner’s contention that claim 6 would have been obvious over the combined teachings of Yoshinaga and Saint. Pet. 55; Ex. 1003 ¶¶ 242–247, 256–257. Petitioner argues that “when Haralabidis’ common rail (***common ESD bus***) teachings are combined with Yoshinaga, the common rail is both ***adjacent to*** and ***parallel to the plurality of pad groups***, thus satisfying” the “a common ESD bus, adjacent to the plurality of pad groups” limitation of claim 1. Pet. 55 (citing Ex. 1003 ¶¶ 248–250).

Petitioner relies on Yoshinaga with respect to the “a plurality of pad groups, adjacent and connected to the plurality of ESD buses” limitation of claim 1 for the same reasons discussed above with respect to the same limitation in claim 6. *Id.* (identifying the “a plurality of pad groups, adjacent and connected to the plurality of EDS buses” limitation of claim 1 (limitation [1.C]) as identical to and “satisfied for the same reasons” as the “a plurality of pad groups, adjacent and connected to the plurality of ESD buses” limitation of claim 6 (limitation [6.C])). Accordingly, for the reasons set forth above with respect to Petitioner’s Ground 1 challenge of claim 6, we determine that Petitioner does not establish by a preponderance of the evidence that claim 1, claims 2–5 that depend therefrom, and claim 6 would have been obvious over the combined teachings of Yoshinaga, Saint, and Haralabidis. *See* § II.C.3, *supra*.

Similarly, Petitioner contends that “most elements of claim 8 are identical to claim 12 and are satisfied for the same reasons” set forth above with respect to Petitioner’s contention that claim 12 would have been obvious over the combined teachings of Yoshinaga and Saint. Pet. 63; Ex. 1003 ¶¶ 288–296, 302. Petitioner relies on Yoshinaga with respect to the “a plurality of pad groups are adjacent and connected to the plurality of ESD buses” limitation of claim 8 (limitation [8.C]) for the same reasons it made with respect to the “the plurality of pad groups are adjacent and connected to the plurality of ESD buses” limitation in claim 12 (limitation [12.C] in Ground 1. Pet. 63 (identifying the limitation [8.C] as “identical to” and “satisfied for the same reasons” as limitation [12.C])). In Ground 1, Petitioner argues that the part of limitation [12.C] “claiming ‘a plurality of pad groups . . . wherein the plurality of pad groups are adjacent and connected to the plurality of ESD buses’ contains the same limitation recited in [6.C], and Yoshinaga discloses it for the same reasons.” Pet. 44 (citing Ex. 1003 ¶¶ 186–192). Accordingly, for the reasons set forth above with respect to Petitioner’s Ground 1 challenge of claim 6, we determine that Petitioner does not establish by a preponderance of the evidence that claim 8, claims 9–11 that depend therefrom, and claim 13 that depends from claim 12 would have been obvious over the combined teachings of Yoshinaga, Saint, and Haralabidis. See §§ II.C.3–C.4, *supra*.

E. Ground 3: Asserted Obviousness over Saint and Haralabidis

Petitioner contends that claims 1–14 would have been obvious over the combined teachings of Saint and Haralabidis. Pet. 68–99.

1. Claim 1

Petitioner contends that the combination of Saint and Haralabidis discloses all of the limitations of claim 1. Pet. 68–83. For example,

Petitioner contends that Saint discloses “a circuit area” (often a rectangular or square space in the middle of the integrated circuit that is divided into various functional areas referred to as blocks), “a plurality of ESD buses” (three ground buses GND1, GND2, and GND3 shown in Saint Figure 7-7), and “a plurality of pad groups, adjacent and connected to the plurality of ESD buses” (ground/power supply pins 1–16 shown in Saint Figures 7-3 through 7-7). *Id.* at 69–74 (and exhibits cited therein).

Petitioner contends that Saint discloses the claimed “a plurality of ESD buses” because it “discloses three GND (known as ground or reference voltage) buses shown in blue in Figure 7-7,” which is reproduced below. Pet. 70 (citing Ex. 1008, 162).

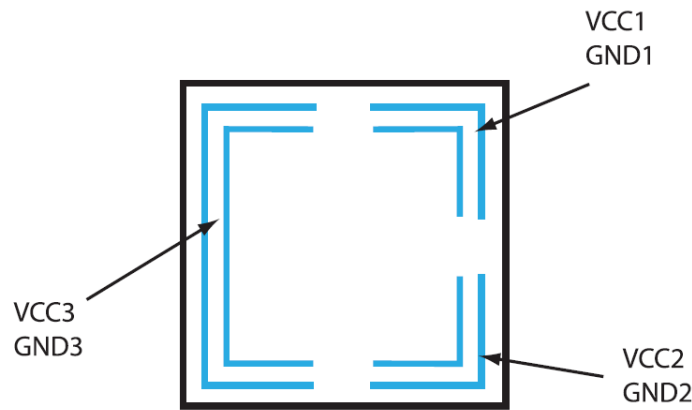


Figure 7-7. Pin-out simplification showing like protects grouped together.

Figure 7-7 is a simplified floorplan depicting power supply voltages VCC1, VCC2, and VCC3, and ground voltages GND1, GND2, and GND3. Ex. 1008, 162. Petitioner contends that “a POSITA would have understood that Saint’s GND (and VCC) buses are ‘ESD buses’ because they serve as ground and power supply buses, respectively, and further because Saint explicitly discloses ESD protection connected to these buses.” Pet. 71 (citing Ex. 1008, 160–164; Ex. 1003 ¶¶ 350, 359).

Petitioner asserts that Saint and Haralabidis disclose “a common ESD bus, adjacent to the plurality of pad groups” because “Saint discloses ‘ESD Ground Wiring’ that ‘creates a continuous ring around the active circuitry’ to which ESD diodes are connected,” and “Haralabidis discloses that it was common practice to place ‘package common ground rail 360’ around an IC” to connect “‘segmented . . . ground rails 350, 355’ via connections 370 and 374.” Pet. 74–76 (citing Ex. 1008, 344, Fig. CS1-99; Ex. 1007, 3:9–18, Fig. 3). Petitioner provides an annotated version of Saint’s Figure 7-7, reproduced below, to illustrate its contentions.

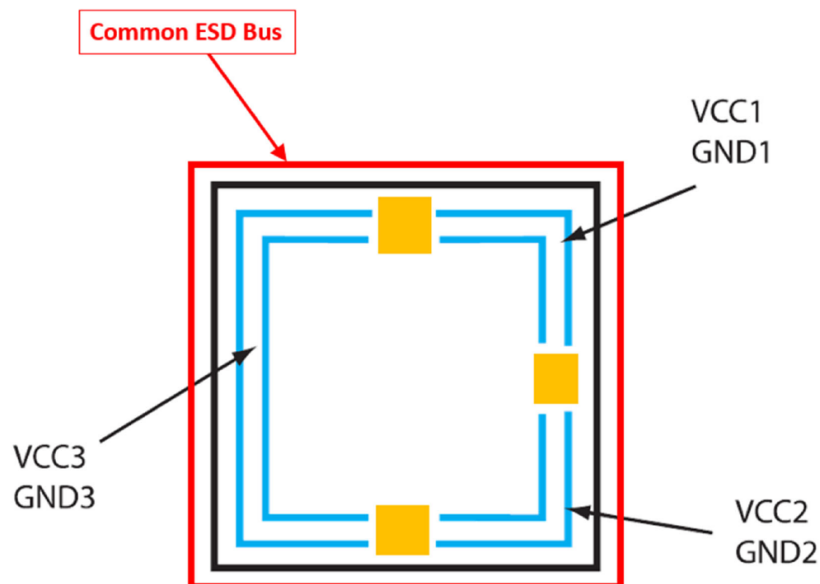


Figure 7-7. Pin-out simplification showing like protects grouped together.

Petitioner’s annotations to Figure 7-7 include the addition of a red box labelled “Common ESD bus” around the entire package, and the addition of orange shading in the spaces between the ends of GND1 and GND2 (right side), GND2 and GND3 (bottom), and GND3 and GND 1 (top). Pet. 77 (citing Ex. 1008, 162, Fig. 7-7; Ex. 1003 ¶ 368). Petitioner contends that, as the “conceptual implementation” depicted in annotated Figure 7-7 shows, “[a]pplying either Saint’s ‘ESD Ground Wiring’ or Haralabidis’ common

ground rail teachings results in a common ESD bus[] [red box] adjacent to the plurality of ESD buses [blue segments] and the plurality of pad groups [not shown but present as explained previously].” *Id.* at 76–77 (citing Ex. 1003 ¶¶ 356–367) (second to fourth alterations in original). According to Petitioner, “[t]he common rail allows circuits to source the reference voltage from the same line, so the PCB (or other external circuitry) need only feed the common line which propagates the reference voltage to all appropriate internal IC circuits.” *Id.* at 77–78 (citing Ex. 1003 ¶ 368).

Patent Owner argues that Petitioner ignores that “Saint’s Figure 7-7 discloses the use of three separate and distinct ground signals—GND1, GND2, and GND3—not a ‘common ESD bus’ as required by the challenged claims.” PO Resp. 60–31 (citing Ex. 1008, 145–147). Patent Owner argues that “POSITAs would have understood that the three separate signals GND1, GND2, and G[ND]3 should **not** be connected together as Petitioner proposes.” *Id.* at 61 (citing Ex. 2010 ¶¶ 121–126). Patent Owner also argues that Saint does not teach “connecting GND1, GND2, and GND3 signals in the layout of Figure 7-7, nor does it consider using a ‘common ESD bus’ for ESD protection and noise suppression.” *Id.* Instead, Patent Owner argues, “Saint teaches that the three separate signals GND1, GND2, and GND3 should remain unconnected to each other to prevent noise and maintain EDS protection.” *Id.* (citing Ex. 1008, 147; Ex. 2010 ¶¶ 123–128).

Patent Owner further argues that Saint’s Case Study 1, upon which Petitioner relies to support its contentions, “is a completely separate embodiment from Saint Figure 7-7 with fundamentally incompatible teachings.” PO Resp. 62. In particular, Patent Owner argues that “Case Study 1 incorporates only one ‘GND’ signal and includes a ‘continuous ring’ that can be used as an ‘ESD Ground Wiring.’” *Id.* (citing Ex. 1008, 249,

332). Patent Owner argues that “connecting separate signals GND1, GND2, and GND3 of Saint Figure 7-7 together to a ‘common ESD ground’ would result in noise injection and performance degradation, making it an undesirable design choice.” *Id.* at 63 (citing Ex. 2010 ¶¶ 127–129).

Similarly, Patent Owner argues that “Haralabidis’ ‘common ground rail 360’ connects the segmented—but common—ground signal together” and “does not disclose or suggest using a ‘common ground rail’ to connect three *different* and separate ground signals as in Saint Figure 7-7.” *Id.* (citing Ex. 1007, 3:9–22, 3:34–40, 3:65–4:12; Ex. 2010 ¶ 129).

Having considered the complete trial record, we determine that Petitioner fails to sufficiently demonstrate by a preponderance of the evidence that Saint alone, or the combined teachings of Saint and Haralabidis, disclose “a common ESD bus, adjacent to the plurality of pad groups” limitation of claim 1.

Saint Figure 7-7 is built from Saint Figure 7-6, reproduced below.

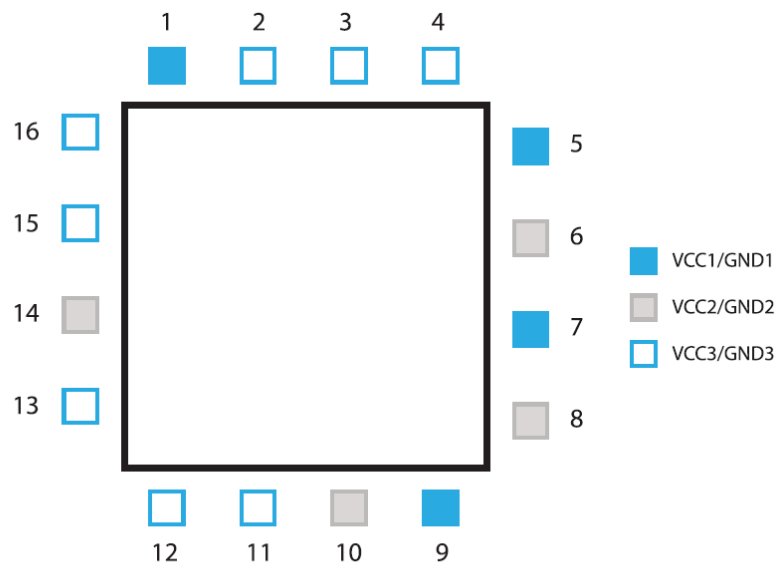


Figure 7–6. Scattered pins on the same protect circuit.

Ex. 1008, 146. Saint Figure 7-6 depicts the final pin-out for the package where the signals on pins 1, 5, 7, and 9 are protected to VCC1 and GND1, the signals on pins 6, 8, 10, and 14 are protected to VCC2 and GND2, and the signals on the remaining pins are protected to VCC 3 and GND3. *Id.* at 145. Saint explains that because pins 1, 5, 7, and 9 are scattered all over the package, protecting them to VCC1 and GND1 “would run wires past pins 6 and 8, which are protected on another supply. The supply wiring also would run past pins 2, 3, and 4 which are protected on a third supply.” *Id.* at 147. Saint further explains that “these wires must be fairly large, since they are all ESD protection” and “must be able to take a reasonable chunk of current.” *Id.* Saint teaches that the pin-out depicted in Figure 7-6 “is going to place a lot of heavy supply wiring all around this chip, in, over, and around all sorts of other heavy supply wiring,” which will make the “chip much bigger than it needs to be.” *Id.* Saint Figure 7-7 depicts a redesign of the pin-out in Figure 7-6 in which the signals protected to the same supply are close to each other, resulting in a “nice, small, short, self-contained area for the set of signals.” *Id.* Saint teaches that this “makes the chip smaller, keeps parasitics down, and keeps cross talk down from one supply to another.” *Id.*

Saint’s Case Study 1, in contrast, has four separate power supplies but a single common ground. Ex. 1008, 248–249, Fig. CS1-1. The case study, which is directed to a CMOS amplifier, provides the “simplified plot [that] shows the ground wires associated with the ESD protection system,” reproduced below.

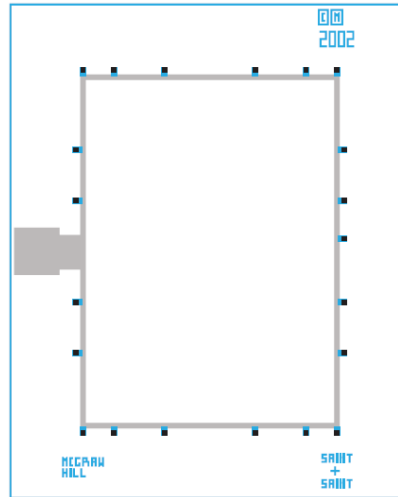


Figure CS1-99

Id. at 332, Fig. CS1-99. Saint notes that “this wire creates a continuous ring around the active circuitry” and “the ESD diode inner terminals (anodes) are connected.” *Id.* It is this “Ex. 1003 ¶ 360.

Despite recognizing that the design in Saint Figure 7-7 has three separate power supply and three separate ground lines and the design in Case Study 1 uses a single ground rail and single ESD bus, neither Petitioner nor Dr. Foty adequately explain why a POSITA would have used the common ground bus of Case Study 1 to modify the design in Saint Figure 7-7 in the first instance. Pet. 74–78; Ex. 1003 ¶¶ 354–364. For example, Dr. Foty testifies that in chapter 7, Saint “depict[s] a design where there are three separate power supply and three separate ground lines,” and in the “different design of” Case Study 1, “Saint is *not* using the three-ground rails (which provided three ESD buses) configuration.” Ex. 1003 ¶¶ 359–360. Instead, Dr. Foty testifies, “Saint is using a *single* ground rail which provides a single ESD bus; this single ground rail – by providing a single ESD bus to which *all* the anode-sides-connected-to-ground of the ESD protection circuit diodes are connected – provides the recited ‘common ESD bus’ of claim element [1d].” *Id.* ¶ 360. This testimony does not apprise us of a sufficient

reason *why* a POSITA would have used a common ESD ground in a design that already has three separate ground lines providing ESD protection. Petitioner does state that “[t]he common rail allows circuits to source the reference voltage from the same line, so the PCB (or other external circuitry) need only feed the common line which propagates the reference voltage to all appropriate internal IC circuits.” Pet. 77–78 (citing Ex. 1003 ¶ 368). Petitioner, however, does not sufficiently explain the advantages of using a single line.

In an obviousness determination, we must avoid analyzing the prior art through the prism of hindsight. Instead, we must “cast the mind back to the time the invention was made” and “occupy the mind of one skilled in the art who is presented with only the references, and who is normally guided by then-accepted wisdom in the art.” *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554 (Fed. Cir. 1983); *see also Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1368 (Fed. Cir. 2012) (quoting *Innogenetics*, 521 F.3d at 1374 n.3 (“We must still be careful not to allow hindsight reconstruction of the references to reach the claimed invention without any explanation as to how or why the references would be combined to produce the claimed invention.”)). Here, Petitioner attempts to imbue a POSITA with the knowledge of the claimed invention, when no prior art reference, references of record, or other evidence conveys or suggests that knowledge. Petitioner’s argument that a POSITA would have modified Saint Figure 7-7 with Saint Case Study 1 in this way appears to be premised on Petitioner’s knowledge of the ’164 patent disclosure. This is improper hindsight reasoning. Petitioner needed to explain what would have led a POSITA at the time of the invention to consider modifying Saint Figure 7-7

to include a common ESD bus. Petitioner fails to provide such an explanation.

Petitioner's reliance on Haralabidis with respect to the claimed common ESD bus does not fare better. Dr. Foty testifies that "Haralabidis describes the common ground line (360) as being the line to which the energy of ESD events (that are first shunted to the segmented ground lines (350 and 355)) is finally shunted" and "thus, Haralabidis describes (and thus renders obvious) a common ESD bus." Ex. 1003 ¶ 367. Dr. Foty goes on to testify that

it is a fairly simple exercise (and would have been a simple exercise for a POSITA) to add the common ESD bus described by Haralabidis to the Figure 7-7 presentation of Saint—and (since they have to connect somewhere) to connect the segmented rails of Saint's Figure 7-7 presentation to this common ESD bus. Using a common rail allows circuits to source the reference voltage from the same line (as discussed above for Saint Figure CS1-1), so that the printed circuit board (or other external circuitry) only needs to feed the common line – which then shares the reference voltage with all of the internal IC circuits. Therefore, Saint in combination with Haralabidis also renders obvious this claim element of Claim 1 of the '164 patent.

Id. ¶ 368 (internal diagram omitted); *see* Pet. 76–78.

Unlike the three separate ground lines in Saint Figure 7-7, Haralabidis describes a single ground rail that is divided into a plurality of segments, each of which is coupled to another segment of the ground rail by one or more diodes. Ex. 1007, 1:56–59; *see also id.* at 1:50–54 ("[A]n integrated circuit assembly includes an integrated circuit (IC) package substrate including a package ground rail that is divided into a plurality of segments that are physically separate from each other."), 3:10–18 ("The SoC 300 [in Figure 3] is similar to the SoC 100 shown in FIG. 1, except that the SoC 300

includes segmented ground rails 350, 355. . . . The package substrate 310 includes a package common ground rail 360, and the segmented SoC ground rails 350, 355 are independently connected to the package common ground rail 360 via separate connections 370, 375 respectively.”). As set forth above, Dr. Foty describes the three ground lines in Saint Figure 7-7 as “segmented rails” when discussing the combination of Saint and Haralabidis, thus equating the three ground lines in Saint Figure 7-7 with Haralabidis’ segmented ground rail. Ex. 1003 ¶ 368. Neither Petitioner nor Dr. Foty, however, adequately addresses how or why a POSITA would have understood that the three separate ground lines in Saint Figure 7-7 were “segmented rails” like the segments of the single ground line described in Haralabidis. In contrast, Dr. Khatri credibly testifies:

Haralabidis teaches the use of a “common ground rail” to connect “segmented ground rails.” Haralabidis, 3:9–22, 3:34–40, 3:65–4:12. A POSITA would understand “segmented ground rails” to refer to a single ground signal that has been “segmented.” That is fundamentally different from the design of Saint’s Figure 7-7 that Dr. Foty relies on, which uses three *different* ground signals, GND1, GND2, and GND3—not a single ground signal that has been “segmented.” Because of that, a POSITA would not have been motivated to change the Figure 7-7 design completely to connect three separate signals (GND1, GND2, and GND3) together as Dr. Foty proposes. Ex. 1003 ¶ 368. Indeed, for these reasons, a POSITA would have understood Haralabidis’ teachings of a “common ground rail” are inapplicable to Saint’s Figure 7-7.

Ex. 2010 ¶ 129. Petitioner’s arguments and Dr. Foty’s testimony with respect to the modification of Saint Figure 7-7 leave an analytical gap that does not apprise us of why a POSITA would have modified Saint Figure 7-7 to include a common ESD bus as described in Haralabidis.

We note that Petitioner argues for the first time in its Reply that Patent Owner's assumption that Saint Figure 7-7 uses three separate and distinct grounds is contradicted by Saint itself. Pet. Reply 14–15 (citing Ex. 1008, 142; Ex. 1042 ¶¶ 120–123). In particular, Petitioner points to Figure 6-2, which Petitioner asserts “shows ‘GND1’ and ‘GND2’ contacts in a singular ‘ring of ground substrate contacts’ (*i.e.*, connected to the same ground substrate).” *Id.* at 14 (citing ex. 1008, 142; Ex. 1042 ¶¶ 120–121). Dr. Foty testifies that Saint Figure 6-2 shows “two ground signals (GND1 and GND2)” that are both “connected (via contacts) to the substrate of the IC,” which “means that they both will have the same voltage as each other at all times.” Ex. 1042 ¶ 121. Dr. Foty goes on to testify that “[a]n engineer would readily understand that Figure 7-7's GND1, GND2, and GND3 labels simply reflect that they are associated with the respective VCC1, VCC2, and VCC3 power domains” and does not mean that “the reference/ground voltages are different.” *Id.* ¶ 122.

But Petitioner and Dr. Foty do not adequately explain why a POSITA would have considered Saint Figure 6-2 in connection with Saint Figure 7-7, or that GND1, GND2, and GND3 share a common ground. In that regard, the figures appear in different chapters of Saint and illustrate different examples and concepts. *Compare* Ex. 1008, 142 (Figure 6-2) *with id.* at 162 (Figure 7-7). As Patent Owner notes with supporting testimony from Dr. Khatri, Saint's Figure 7-7 optimizes “ESD protection around multiple, distinct ground references, and corresponding VCC rails.” PO Sur-reply 23 (citing Ex. 1008, 147–148; Ex. 2010 ¶¶ 124–129). Dr. Khatri credibly testifies:

Figure 7-7 of Saint illustrates one way to arrange a circuit so that the pins 1 through 16, that are “protected to the same

supply” are moved “close together” because the chip design has three *different* VCC and GND signals. In other words, pins 1, 5, 7 and 9 are moved close together and protected against VCC1 and GND1, while pins 6, 8, 10 and 14 are moved close together and protected against VCC2 and GND2, and pins 2, 3, 4, 11, 12, 13, 15 and 16 are moved close together and protected against VCC3 and GND3. Saint never teaches connecting the different GND1, GND2, and GND3 signals together to a “common ground” as Dr. Foty proposes. In fact, a POSITA would have understood from Figure 7-3, 7-4, 7-5 and 7-7 that GND1, GND2, and GND3 are separate reference potentials that should *not* be connected together as Dr. Foty proposes.

Ex. 2010 ¶ 126 (internal citations omitted). Moreover, Dr. Foty previously testified that “in the Chapter 7 discussion Saint has depicted a design where there are three separate power supply and three separate ground lines,” which he contrasted to Saint Case Study 1 where “Saint is *not* using the three-ground-rails (which provide three ESD buses) configuration of the Chapter 7 design” and is instead “using a *single* ground rail which provides a single ESD bus.” Ex. 1003 ¶¶ 359–360. Dr. Foty’s argument in reply that “a POSITA would have understood (or at least would have found obvious) that Saint’s GND1, GND2, and GND3 connect to each other” does not appear to be completely consistent with his previous acknowledgement that GND1, GND2, and GND3 are three separate grounds.

Accordingly, we determine that Petitioner does not demonstrate, by a preponderance of the evidence, that claim 1 would have been obvious over the combined teachings of Saint and Haralabidis.

2. Claims 2–5

Petitioner also contends that the combined teachings of Saint and Haralabidis discloses all of the elements of claims 2–5. Pet. 83–85. Claims 2–5 directly depend from claim 1, and therefore include the “a

common ESD bus adjacent to the plurality of pad groups” limitation of claim 1. Ex. 1001, 5:30–42. Thus, for the same reasons given above with respect to Petitioner’s challenge of claim 1, we also conclude that Petitioner does not demonstrate, by a preponderance of the evidence, that claims 2–5 would have been obvious over the combined teachings of Saint and Haralabidis.

3. *Claims 6 and 7*

Petitioner asserts that “most claim 6 elements are identical to claim 1, and are satisfied for the same reasons.” Pet. 85 (citing Ex. 1003 ¶¶ 401–406, 412, 413). With respect to the “a plurality of bonding wires configured to connect one to another of the plurality of pad groups” limitation of claim 6, Petitioner contends that “Saint discloses ‘ESD Ground Wiring’ that ‘creates a continuous ring around the active circuitry’ to which ESD diodes are connected, as shown in Fig. CS1-99” and also “discloses ‘bond wires’ connect to ‘bond pads on the chip.’” *Id.* at 86 (citing Ex. 1008, 202–204, 344. Petitioner asserts that “Saint also discloses ‘[w]ire bonding is the most common method of attaching a chip to a package.’” *Id.* (citing Ex. 1008, 207) (alterations in original). Petitioner contends that “[w]hile bond wires often connect IC pads to package pins, it was also well-known to use bond wires to connect other elements (*e.g.*, other pads, components, conductors, etc. within a chip).” *Id.* (citing Ex. 1003 ¶ 410). Petitioner contends that “a POSITA would have understood pad-to-pad bond wire connections were common” and “would have been encouraged to use bonding wires because they ‘fuse[] the wire to the bond pad’ and result in ‘firmly attach[ed] connections.” *Id.* at 50 (citing Ex. 1014, Figs. 7, 10, 13, Abstract; Ex. 1015, 6:67–7:7; Ex. 1016 ¶¶ 7, 27–30, 34–36, Figs. 4–6; Ex. 1003 ¶¶ 106–107; Ex. 1008, 204).

Patent Owner responds that Petitioner does not “identify any disclosures in Saint or Haralabidis disclosing the use of bonding wires to connect bond pads.” PO Resp. 65 (citing Ex. 2011, 107:7–19; Pet. 86). Patent Owner argues that “the fact that bond wires were well-known does not mean that a POSITA would have been motivated to use them in this specific manner.” *Id.* at 35. Patent Owner further argues that “Saint teaches using bonding wires only when there is ‘minimal silicon overlap’ and does not mention using them to connect pads” and “cautions that ‘the bond wire could sag or droop, causing a short in the circuit,’ and therefore, ‘you have to keep the overlap of the bond wire over the unused silicon as short as possible.’” *Id.* at 39 (citing Ex. 1008, 139). Patent Owner argues that “the Petitioner’s references to bonding wire in Saint pertain to connecting chip pads with external pins during packaging, where direct connection is impossible since the package pins are outside the chip.” *Id.* at 66 (citing Pet. 79; Ex. 2010 ¶¶ 79, 137, 138). According to Patent Owner, “Saint never teaches using bonding wiring when integrated circuit [metallization] based wiring is possible, such as with Saint’s Figure 7-7.” *Id.* (citing Ex. 2010 ¶¶ 79, 137).

It is Petitioner’s burden to establish facts supporting its challenge that claim 6 would have been obvious over the combined teachings of Saint and Haralabidis by a preponderance of the evidence. 35 U.S.C. § 316(e) (2018); *see also Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring inter partes review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). After considering the parties’ arguments and evidence of record, and weighing the testimony of Dr. Foty and Dr. Khatri, we are not persuaded that Petitioner meets its burden of establishing, by a

preponderance of the evidence, that the combined teachings of Saint and Haralabidis disclose “a plurality of bonding wires configured to connect one to another of the plurality of pad groups” as recited in claim 6.

Saint does not discuss using bond wires to connect pads to other pads on the integrated circuit structure as is required by claim 6. *See* Ex. 2010 ¶ 79 (Explaining that Saint “only uses bond wires where direct integrated circuit metallization based wiring . . . is not possible, such as when connecting chip pads to external pins of the package.”). Saint’s discussion of bond wires is directed to using wire bonding to attach bond pads to package pins. *See* Ex. 1008, 203 (“There are several ways to attach bond pads to package pins.”), 207 (“Wire bonding is the most common method of attaching a chip to a package.”). Saint, however, does identify several problems associated with the use of wire bonding. For example, Saint cautions that “bond wires might tend to dangle all over the place in a poor bonding design,” and care must be taken to avoid shorting those wires to other signals. *Id.* at 207. Saint also explains that bonding wires that are too long “could droop down and short to something in the circuit.” *Id.* at 204–205. Similarly, Saint teaches that bond wires that overlap too much silicon “could sag or droop, causing a short in the circuit” and thus it is necessary to “keep the overlap of the bond wire over unused silicon as short as possible.” *Id.* at 209.

In light of these disclosures in Saint, Petitioner does not adequately explain why a POSITA would have been motivated to use bonding wires to attach pad groups in Saint Figure 7-7. Although Petitioner points to prior art such as Miller⁶ showing that pad-to-pad wire bonding was one of many

⁶ Miller, US 2004/0140860 A1, published July 22, 20014 (Ex. 1014).

known alternatives, other evidence indicates that wire bonding would be disfavored when doing so would add bond wires that overlap the alleged “at least one saved area.” *See* Pet. 36 (citing Ex. 1014, code (57), Figures 7, 10, 13). In particular, Miller merely states that the “contact pads are linked to one another and the IC I/O terminal th[r]ough inductive conductors such as bond wires, metallization layer traces in the IC, or legs of a forked, lithographically-defined spring contact formed on the IC.” Ex. 1014 at code (57). We find that this statement does not sufficiently support that a POSITA would have had reason to use bonding wires to attach pad groups to one another in Saint Figure 7-7, as asserted by Petitioner, given the persuasive record evidence to the contrary.

Referring to Saint Figure 7-7, Petitioner contends that the spaces between the ends of GND1 and GND2 (right side), GND2 and GND3 (bottom), and GND3 and GND 1 (top) are “saved areas” as recited in claim 6. Pet. 80–83 (addressing claim 1), 85–86 (relying on arguments made with respect to claim 1 for similar elements in claim 6). Using bond wires to connect the pads in Saint Figure 7-7 requires spanning the saved areas (unused silicon) with bond wires. Saint, however, teaches that bond wires over unused silicon “could sag or droop, causing a short in the circuit,” and the overlap between bond wires and unused silicon should be kept as short as possible. Ex. 1008, 209. Considering that there are other methods of connecting the pad groups that would avoid overlapping bond wires and unused silicon (such as integrated circuit metallization based wiring), Petitioner does not adequately explain why a POSITA would have been motivated to use bonding wires as recited in claim 6. *See* Ex. 2010 ¶ 137 (“In view of Saint’s teachings, a POSITA would preferentially use integrated circuit metallization and be discouraged from deliberately forming the bond

wire to overlap entirely with ‘unused silicon’ (the alleged ‘saved areas’ shown in orange’ as Dr. Foty proposes.”)); Ex. 1038, 138:21–140:14 (Dr. Khatri testifying that “bond wires to connect bond pads to bond pads on the same IC, on the same chip or the same die, was considered dangerous and considered, you know, a tricky thing to do because” it is “something that would potentially cause a short circuit”), 224:16–226:25 (Dr. Khatri testifying that “before the ’164 patent, conventional wisdom was, you know, bond wires are not even an option” and “[i]t was not a choice” that a POSITA “would have considered”).

And, as Patent Owner notes, other references cited by Petitioner regarding the knowledge of pad-to-pad wire bonding in the prior art “do not establish that pad-to-pad bonding wire was a known, suitable option.” PO Sur-reply 27. Patent Owner states:

Beddingfield uses “jumper wire[s]” to connect a pad with inner circuitry, not other pads, to form an additional path parallel to the on-chip metallization connections. Ex. 1041 [0015], [0022], Figs. 2–4; Ex. 2017 82:9–85:20. Lee addresses RFID tags on a single layer substrate, unlike the multi-layer integrated circuits in Yoshinaga and Saint. Ex. 1039 Abstract; Ex. 2017 87:2–12. Conner concerns bonding wire connections to bond fingers on flex substrates and PCBs, not on-chip pad-to-pad connections. Ex. 1040 Figs. 4–6, 2:30–35, 3:37–50; Ex. 2017 90:10–94:3.

Id. at 27–28. Thus, Petitioner’s argument that using bond wires to connect pads to each other and “the manufacturing techniques to connect pads with wire bonding were well-known and routine to implement” appears to be nothing more than a statement that a POSITA could have made the proposed modification. Pet. 36–38 (and references cited therein), 86–87.

Obviousness, however, “concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or

modifications of prior art to arrive at the claimed invention.” *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015); *see also Forest Labs., LLC v. Sigmapharm Labs., LLC*, 918 F.3d 928, 934 (Fed. Cir. 2019) (“An invention is not obvious simply because all of the claimed limitations were known in the prior art at the time of the invention.”).

For these reasons, after considering Petitioner’s and Patent Owner’s positions, as well as their supporting evidence, we are not persuaded that Petitioner sufficiently demonstrates that the combined teachings of Saint and Haralabidis teaches or suggests “a plurality of bonding wires configured to connect one to another of the plurality of pad groups” recited in claim 6. Accordingly, we determine that Petitioner does not show by a preponderance of the evidence, that claim 6, and claim 7 that depends directly therefrom, would have been obvious over the combined teachings of Saint and Haralabidis.

4. *Claims 8–11*

Petitioner asserts that the combined teachings of Saint and Haralabidis disclose all of the elements of independent claim 8. Pet. 88–92. In particular, Petitioner argues that the “forming a common ESD bus adjacent to the plurality of pad groups” limitation of claim 8 is “nearly identical” to the “a common ESD bus adjacent to the plurality of pad groups” limitation of claim 1 and “is met for the same reasons.” *Id.* at 91 (citing Ex. 1003 ¶ 428). Petitioner argues that the “difference is inconsequential,” because Petitioner “explains how Saint and Haralabidis render obvious *a common ESD bus, adjacent to the plurality of pad groups*” for claim 1, and it “must necessarily have been ‘*form[ed]*’ to exist.” *Id.*

Accordingly, for the same reasons given above with respect to Petitioner’s challenge of claim 1, we also conclude that Petitioner does not

demonstrate by a preponderance of the evidence that claim 8, and claims 9–11 that depend directly therefrom, would have been obvious over the combined teachings of Saint and Haralabidis.

5. *Claims 12–14*

Petitioner contends that the combined teachings of Saint and Haralabidis disclose all of the elements of claim 12. Pet. 92–94. Petitioner contends that the “connecting one of the plurality of pad groups to another of the plurality of pad groups by one of a plurality of bond wires across the circuit area” limitation of claim 12 is “nearly identical to” the “a plurality of bonding wires configured to connect one to another of the plurality of pad groups” limitation of claim 6, “and Saint with a POSITA’s knowledge renders much of it obvious for the same reasons.” *Id.* at 92 (citing Ex. 1003 ¶¶ 448–449). Petitioner contends that the difference between claim 12’s “connecting” and claim 6’s “configured to connect” is inconsequential and does not change the prior art analysis.” *Id.* (citing Ex. 1003 ¶ 449).

For the reasons set forth above with respect to claim 6,⁷ we also conclude that Petitioner does not demonstrate by a preponderance of the evidence that claim 12, and claims 13 and 14 that depend directly therefrom, would have been obvious over the combined teachings of Saint and Haralabidis.

⁷ Because we determine that Petitioner does not adequately establish that a POSITA would have been motivated to connect the pad groups in Saint Figure 7-7 to each other, we do not reach Petitioner’s contention that it would have been obvious to run the bond wires across the circuit area.

III. CONCLUSION

After reviewing the parties' arguments and weighing the evidence offered by both parties, we determine that Petitioner does not show, by a preponderance of the evidence, that claims 1–14 of the '164 patent are unpatentable.

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
6, 7, 12, 14	103	Yoshinaga, Saint		6, 7, 12, 14
1–6, 8–11, 13	102	Yoshinaga, Saint, Haralabidis		1–6, 8–11, 13
1–14	103	Saint, Haralabidis		1–14
Overall Outcome				1–14

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has not established by a preponderance of the evidence that claims 1–14 of the '164 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Patent 10,879,164 B2

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