

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: March 12, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00119
Patent 10,879,254

PATENT OWNER'S PRELIMINARY RESPONSE

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Exhibit List

Ex.	Description
2001	Micron's Motion to Stay the Case Pending Inter Partes Review and Post Grant Review Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Jan. 16, 2025), ECF No. 200
2002	Plaintiff/Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.'s and Counterclaim Defendant Yangtze Memory Technologies, Inc.'s Opposition to Micron's Motion to Stay Case Pending Inter Partes Review and Post-Grant Proceedings, <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Feb. 3, 2025), ECF No. 221
2003	Docket Entry Order (issuing temporary stay), <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , No. 3:23-cv-05792-RFL (N.D. Cal. Mar. 3, 2025), ECF No. 242
2004	U.S. District Courts–Time Intervals from Filing Date to Beginning Date for Completed Civil Trials, by District, During the 12-Month Period Ending September 30, 2024 (https://www.uscourts.gov/sites/default/files/2025-01/jb_t3_0930.2024.pdf)
2005	Statutory Disclaimer of Claims 1, 5, and 6 of U.S. Patent 10,879,254 Under 37 C.F.R. § 1.321(a) (Filed Feb. 21, 2025)
2006	Curriculum Vitae of Stephen Campbell, Ph.D.
2007	Declaration of Stephen Campbell, Ph.D. ("Campbell")
2008	<i>Springer Series in Advanced Microelectronics: Inside Solid State Drives (SSDs)</i> (Rino Micheloni et al. eds., 2nd ed. 2018), as-filed by Petitioner as Exhibit 1014 in IPR2025-00035
2009	<i>Simultaneous</i> , THE MERRIAM-WEBSTER DICTIONARY, NEW EDITION (2004)

I. Introduction

Patent Owner Yangtze Memory Technologies Company, Ltd. (“YMTC”) respectfully submits this Preliminary Response to the Petition for *inter partes* review of U.S. Patent 10,879,254 (“’254 patent”). As explained below, Petitioner has failed to carry its burden to show a reasonable likelihood that at least one of the challenged claims is unpatentable. Thus, the Board should deny the Petition and no IPR proceeding should be instituted.

As a threshold issue, the Board should use its discretion to deny this Petition because Petitioner has already filed another petition challenging the exact same claims. *See* IPR2025-00034, Paper 1 (Oct. 11, 2024). As discussed in Patent Owner’s Response to Petitioner’s Ranking of Petitions, no exceptional circumstances exist to warrant the rare granting of two petitions on the same patent. *See id.*, Paper 10 (Feb. 21, 2025). Indeed, Micron’s petitions both used far fewer words (*id.*, Paper 1; Pet. 85 (9,596 and 12,083 words, respectively)), than the word count allowed for IPR petitions (14,000). IPR2025-00034, Paper 6 at 2 (Nov. 7, 2024). Micron could and should have presented both grounds in one petition instead of filing two petitions, requiring the Board to decide institution twice and, if instituted, conduct two oral hearings and issue two final decisions.

On the merits, the ’254 patent describes and claims innovative methods for forming 3D memory structures with a vertical “through array contact” or “TAC”

that goes through a stack of dielectric and sacrificial layers. '254 patent, 5:3-6.

The '254 patent further claims such memory structures with (i) “dummy channel[s]” that provide mechanical support, (ii) “simultaneously etch[ed]” openings “through the stack” and “outside of the stack,” and (iii) “shallow recesses” formed in the TAC openings. *See id.*, cls. 2-4, 7-15, 17-18, and 20.

Petitioner asserts a single invalidity ground based on a single reference, Fujiki, in view of the knowledge of a POSITA. But Fujiki does not disclose “dummy channels,” “simultaneously etch[ed]” openings through and outside the stack, or “shallow recesses” in the TAC opening. Petitioner attempts to supply those missing limitations by invoking the “general knowledge” of a POSITA. But “[t]he Court of Appeals for the Federal Circuit has held that the Board is permitted to rely on general knowledge to supply a missing claim limitation in an *inter partes* review, such as when ‘the missing limitation in question [is] **unusually simple** and the technology **particularly straightforward**.’” *Motorola Mobility LLC v. Largan Precision Co.*, IPR2024-00688, Paper 7 at 29 (Oct. 28, 2024) (original alteration and emphases) (denying institution).

The claimed processes for manufacturing “dummy channels,” “simultaneously etch[ed]” openings through and outside the stack, and “shallow recesses” are not “unusually simple” and the field of 3D NAND memory manufacturing is not “particularly straightforward.” Campbell (Ex. 2007) ¶28.

They are highly technical and complex. *See DSS Tech. Mgmt., Inc. v. Apple Inc.*, 885 F.3d 1367, 1374 (Fed. Cir. 2018) (rejecting Board's reliance on "common knowledge" to "supply a missing claim limitation" because wireless communications is not "particularly straightforward" technology). Petitioner's attempt to avoid asserting actual prior art combinations, and instead, generally reference the "knowledge of a POSITA" to supply missing limitations is legal error.

The Board should deny the Petition.

II. Background

A. 3D NAND Memories

3D NAND memory devices are "memory arrays" with memory cells stacked one on top of the other. Memory cells can be written or read by applying a voltage to corresponding conductors that run horizontally across the memory array, called "wordlines." Figure 5.20 of Exhibit 2008, reproduced below, shows an exemplary 3D NAND memory, which includes a series of vertically stacked memory cells, each controlled by a "Control Gate" (the wordline) shown in red as "CG0" through "CG3." Ex. 2008, 119. The ends of the "Control Gates" form a staircase that allows vertical vias to access and contact each wordline (CG0 to CG3) and connect them to peripheral devices.

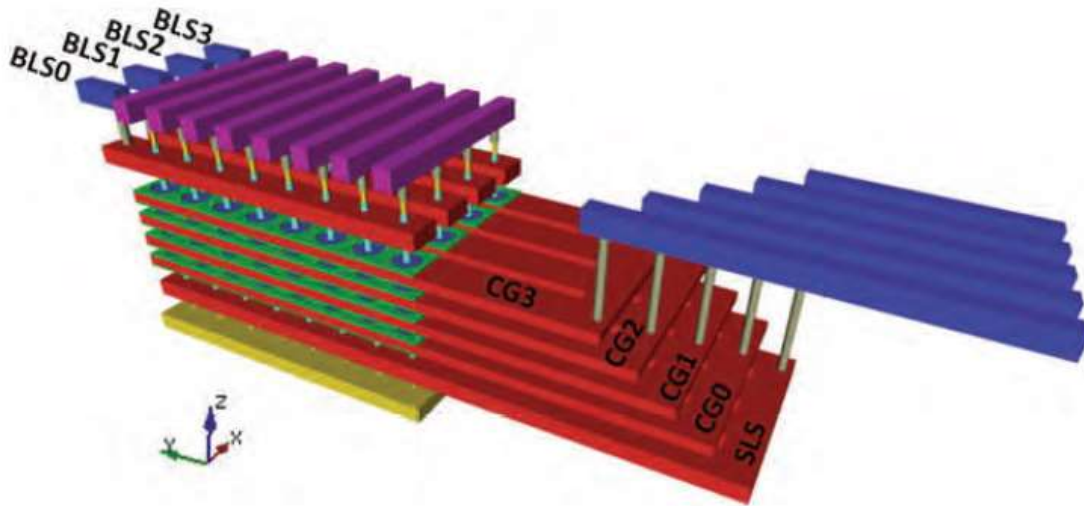


Fig. 5.20 C-FG NAND Flash array with fan-out

B. The '254 Patent (Ex. 1001)

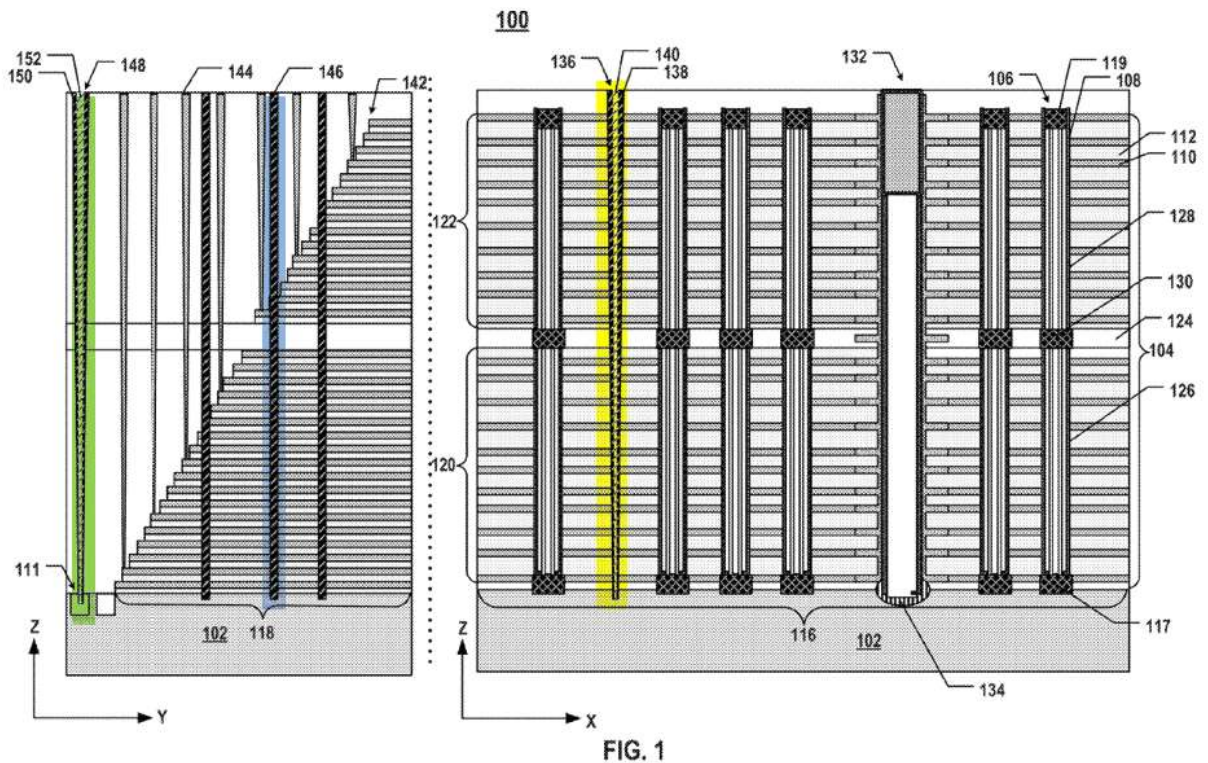
The '254 patent recognized that 3D memory devices require contacts that go vertically through the memory stack called “through array contacts” or “TACs” for “providing vertical interconnects between the stacked memory array device and peripheral device (e.g., for power bus and metal routing).” '254 patent, 4:55-59. In the past, these TACs were formed within a “barrier structure[]” to “preserve[] a dielectric stack region within a memory stack for ease of etching the openings of the TACs.” *Id.*, 4:59-62. The drawbacks of a “barrier structure[]” is that “the regions enclosed by the barrier structures take up large area in the core array region where memory strings can be formed.” *Id.*, 4:59-65. TACs within a barrier structure “also have a negative impact on the resistance of word lines.” *Id.* “Moreover, the existing fabrication processes for forming the barrier structures

become more challenging for the next-generation 3D memory devices” which “have less process margin.” *Id.*, 4:66-5:2.

The '254 patent discloses a novel “3D memory device having TACs not enclosed by barrier structures, which resolves the above-noted issues associated with the barrier structures.” *Id.*, 5:3-6. The '254 patent explains that “by removing the barrier structures, the areas for TACs can be reduced while keeping their functions, thereby increasing memory cell density and decreasing process cost.” *Id.*, 5:6-9. In addition, “[m]ore process margin”—i.e., room for error—may “be obtained due to the elimination of etching and alignment steps for making the barrier structures.” *Id.*, 5:10-15. To “further simplify the fabrication flow and reduce process cost,” the '254 patent teaches that the non-barrier structure TACs can be “formed in the same fabrication process(es) for making other structures” such as “peripheral contacts” outside of the memory stack. *Id.*, 5:14-20.

Figure 1, annotated below, illustrates a cross-section of an embodiment of a “memory stack 104” and a “staircase structure” 142. *Id.*, 5:32-37, 8:61-63. As shown below, the memory device 100 includes a TAC 136 (yellow) that extends vertically through the stack to carry electrical signals to/from the memory device 100. *Id.*, 8:28-39. Unlike the prior art, TAC 136 is not “enclosed by barrier structures.” *Id.*, 5:3-20. This allows the TACs to be “formed in the same fabrication process(es) for making other structures,” including those *outside* the

memory array such as “peripheral contact[]” 148 (green). *Id.*, 5:3-20, 12:24-45. In addition, “dummy channel structures 146” are “disposed in the outer region 118 of memory stack 104 as shown in FIG. 1” to “provide mechanical support to the memory array structures, e.g., memory stack 104.” *Id.*, 9:39-49. An annotated version of Figure 1 is shown below.



The '254 patent discloses additional details about forming the claimed TACs not enclosed by a “barrier structure.” Instead of forming the TACs in a “barrier structure” to isolate the TACs from other electrical components, the process for forming the TACs of the '254 patent start by forming openings in the memory stack itself for the TAC and then depositing “spacer[s]” on the sidewalls of the openings. *Id.*, 12:64-67. Figure 7B, reproduced below, is a flowchart of an

exemplary method for forming such a spacer for the first opening. *Id.*, 13:34-40.

The method includes forming a plurality of shallow recesses by removing parts of the sacrificial layers the memory stack abutting the sidewall of the first opening.

Id., 13:36-40.

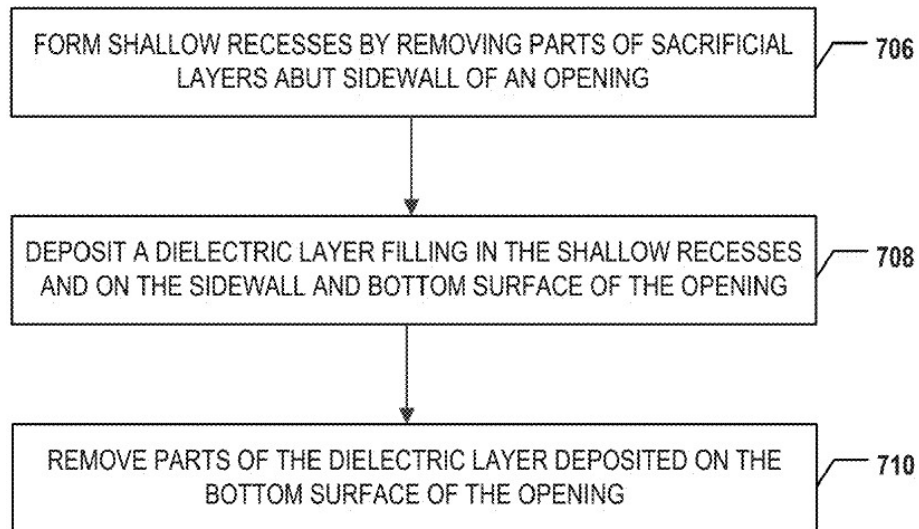


FIG. 7B

Exemplary recesses 312 are shown in Figure 3D, annotated below. *Id.*, 13:52-57. These recesses provide space for a thicker dielectric spacer deposition in step 708, resulting in improved electrical isolation, even without a barrier structure. *Id.*, 13:59-61.

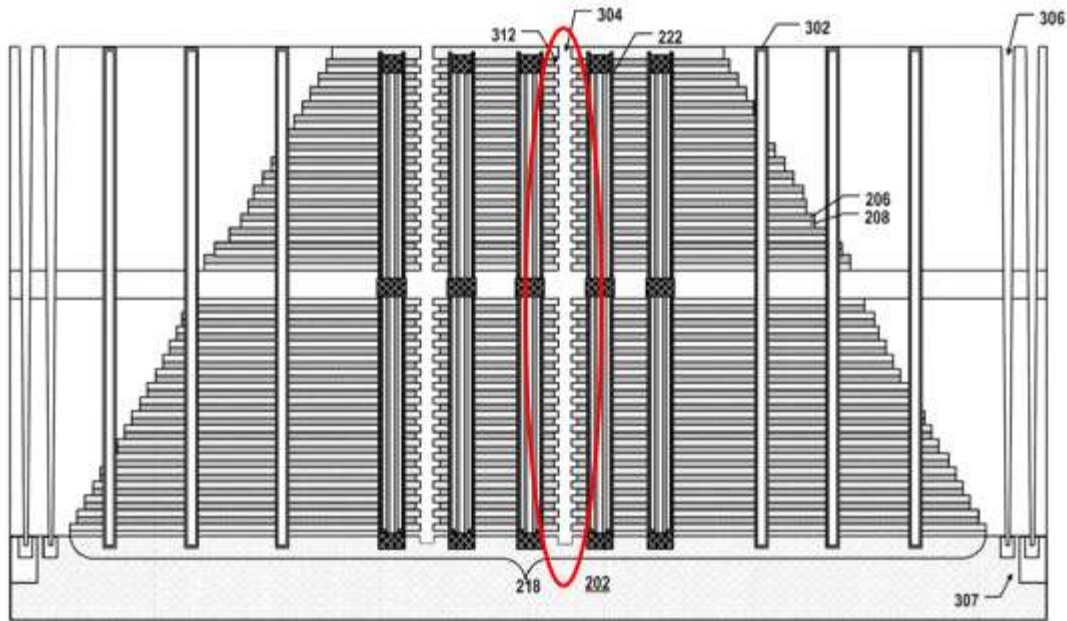


FIG. 3D

C. Person of Ordinary Skill in the Art

YMTC takes no position on the level of ordinary skill in the art for the purposes of this Preliminary Response, as the Petition has failed to establish a reasonable likelihood of prevailing under any reasonable definition of POSITA.

D. Claim Construction

The prior art relied on in the Petition fails to disclose the subject matter of the challenged claims under any reasonable construction, including their plain meaning.¹

¹ Patent Owner reserves the right to advocate for claim constructions in the event the Board institutes review in this case.

III. Ground 1: Claims 2-4, 7-15, 17-18, and 20 are not obvious based on Fujiki and the knowledge of a POSITA.²

A. Fujiki and the POSITA's knowledge do not teach or suggest a "dummy channel ... through the stack" (claims 2, 11-15, 17).

Claim 2 recites "prior to forming the first opening, forming a dummy channel structure extending vertically through the stack." Claim 11 similarly recites "forming a dummy channel structure extending vertically through the stack." Claims 12-15 and 17 depend from claim 11.

Petitioner acknowledges that Fujiki does not disclose any dummy channels. Pet. 44. Fujiki thus does not disclose forming a dummy channel structure extending vertically through the stack as claimed.

Petitioner asserts that "a POSITA would have been motivated, with a high expectation of success, to also form dummy channels." *Id.* Petitioner does not rely on combining Fujiki's teachings with any other prior art. Instead, Petitioner relies exclusively on "the knowledge of a [POSITA]" to support its proposed

² YMTC disclaimed claims 1, 5, and 6. *See* Disclaimer in Patent Under 37 C.F.R. § 1.321(a) (Ex. 2005). The Board cannot institute an IPR on a disclaimed claim. 37 C.F.R. § 42.107(e); *Intuitive Surgical, Inc. v. Ethicon LLC*, IPR2018-01248, Paper 7 at 2 n.1, 9-10 (Feb. 7, 2019). Thus, the Board cannot institute an IPR on claims 1, 5, and 6.

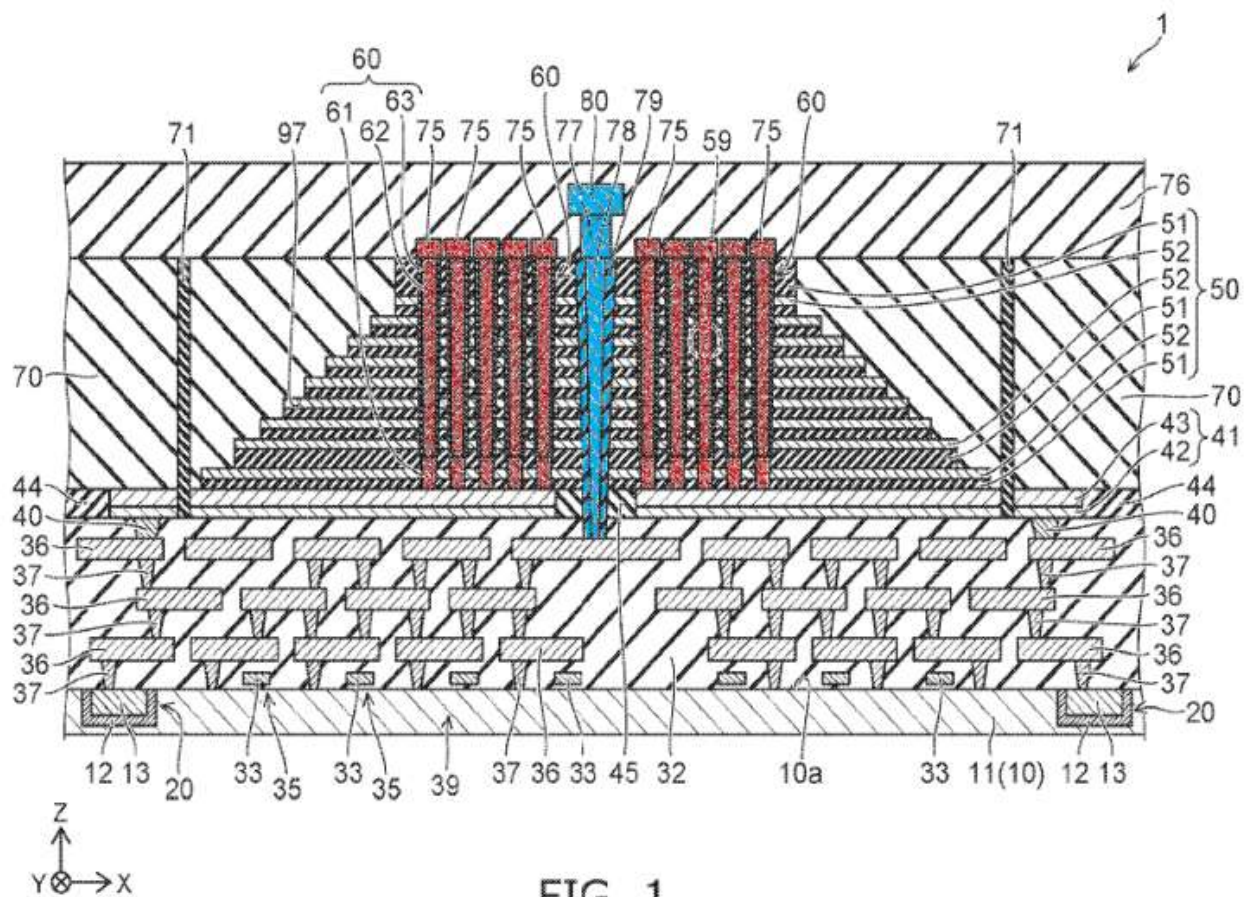
modification of Fujiki “to also form dummy channels” that are indisputably missing from Fujiki. Pet. 44.

As an initial matter, Petitioner's reliance on general knowledge is misplaced because it has failed to demonstrate that “the missing limitation in question [is] *unusually simple* and the technology *particularly straightforward*.” *Motorola*, IPR2024-00688, Paper 7 at 29 (original alteration and emphases) (denying institution). To the contrary, forming a dummy channel structure involves complex semiconductor manufacturing processes, including “wet etching, and/or dry etching, such as DRIE” and “thin film deposition processes, such as ALD, CVD, PVD.” Campbell ¶30; '254 patent, 12:7-23. And 3D NAND technology is plainly not “particularly straightforward.” *See DSS Tech. Mgmt.*, 885 F.3d at 1374 (rejecting Board's reliance on “common knowledge” to “supply a missing claim limitation” because wireless communications is not “particularly straightforward” technology); Campbell ¶50. Petitioner's reliance on “general knowledge” to supply the indisputably missing limitations directed to forming “dummy channels” is legal error. Petitioner's arguments as to claims 2, 11-15, and 17 fail for this reason alone.

Petitioner asserts that it would have been obvious to “form dummy channels” to provide structural support. Pet. 44-45. According to Petitioner, “support pillars” are “necessary” in order to “perform [Fujiki's] gate replacement

process.” Pet. 44. Petitioner is wrong. A POSITA would not be motivated to modify Fujiki as proposed.

First, Fujiki already discloses structures that provide support during its gate replacement process. *Cf.* Pet. 44 (citing Fujiki (Ex. 1006) [0055]), 45 (quoting Ex. 1019, 30:14-27); Campbell ¶32. As annotated in Figure 1 below, Fujiki includes columnar portions 60 (shown in red) and through-via 78 (shown in blue). Fujiki [0036], [0042]; Campbell ¶32.



During the gate replacement process of Fujiki, shown in Figure 10 as annotated below, “spaces 97” (yellow) are “formed where the sacrificial films 91”

once were. Fujiki [0054]; Campbell ¶32. The columnar portions 60 (red) and through-via 78 (blue) provide support to maintain spaces 97 (yellow) in the structure even after removal of the “sacrificial films 91.” Campbell ¶32. If they did not, the insulating films 51 would collapse into the spaces 97 below and the Figure 10 structure could not exist. *Id.* Indeed, Petitioner has not alleged that columnar portions 60 and through-via 78 are inadequate to provide the required support as expressly shown in Figure 10. A POSITA would not be motivated to “also form dummy channels” as Petitioner proposes because they would serve no purpose. *Id.*

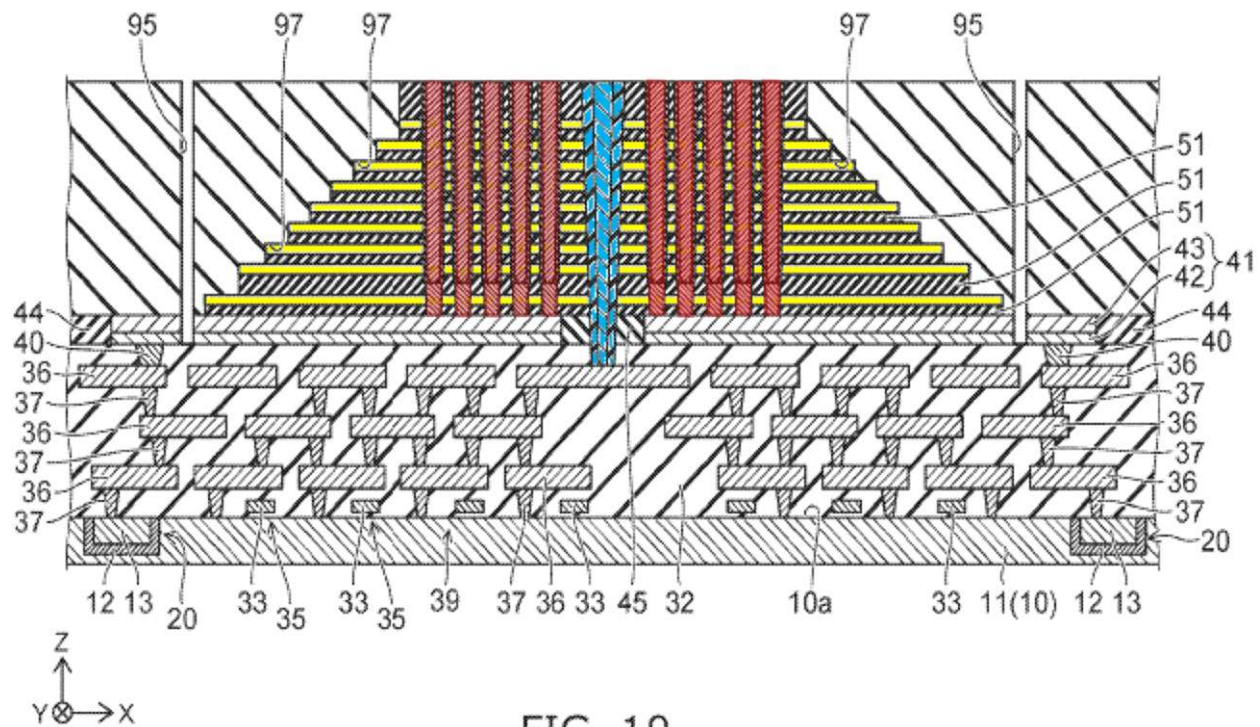


FIG. 10

Second, Petitioner does not provide any explanation about where (or how) the alleged dummy channels would be formed.³ As discussed, Fujiki already discloses columnar portions 60 (shown in red) and through-via 78 (shown in blue) formed “through the stack” as shown below.

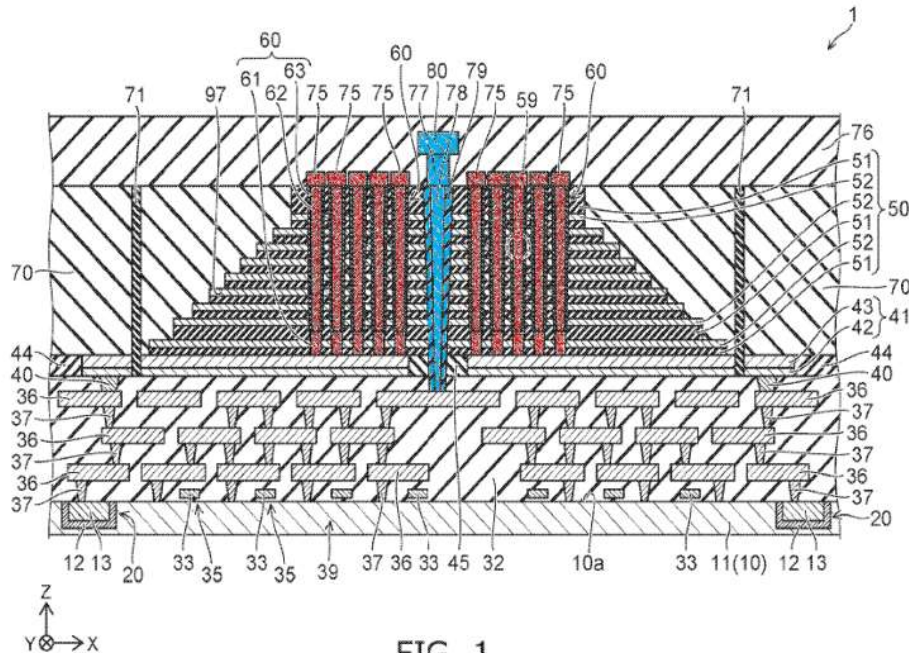


FIG. 1

³ In its prior petition challenging the '254 patent, Petitioner asserts that “it would have been obvious to implement some of [the prior art reference]’s channels as dummy channels.” IPR2025-00034, Paper 1 at 39. Here, Petitioner does not propose modifying any existing structures to be “dummy channels” and instead asserts only that a POSITA would “also form dummy channels” with no further explanation about where or how such structures would be implemented. Pet. 44.

The Petition provides no explanation of where the additional proposed “dummy channels” would be purportedly formed “through the stack”—especially in view of the other structures that provide structural support already formed through the stack. Accommodating dummy channels “through the stack” would require either (1) increasing the size of the stack to create space for the dummy structures, or (2) decreasing the memory’s storage capacity by replacing functional “columnar portions 60” (which serve as channels for the memory cells (Fujiki [0044])) or “contacts 81” (which provide external access to the word lines (*id.* [0043])) with *non*-functional dummy channels. Campbell ¶34. A POSITA would recognize that both results would be undesirable—especially where there is no need for the dummy channels at all, as discussed above. *Id.*

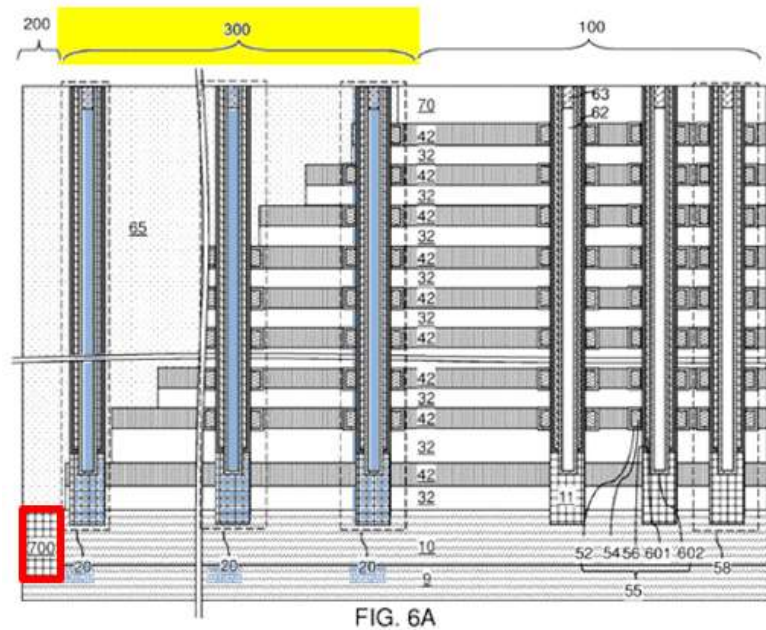
Third, adding dummy channels will add more processing steps and more complexity to the Fujiki process. *Id.* ¶35. For example, forming dummy channels would require adding additional process steps. *Id.* Petitioner’s proposed modification therefore increases manufacturing complexity, without serving any beneficial purpose—while also either increasing device size or decreasing storage capacity. *See supra.*

Petitioner resorts to citing three references—Kai, Kim, and Park—that purportedly “confirm[] the knowledge of a POSITA” that “it was well known that one common option for such support pillars were dummy channels.” Pet. 44-45.

But just because dummy channels were purportedly “well known” does not mean a POSITA “would have been motivated to make the combinations or modifications” to Fujiki to use dummy channels—especially when other structures already provide structural support. *See Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”); *Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993-94 (Fed. Cir. 2017) (conclusion that a combination “would have allowed for” a claimed limitation “is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention”) (citations omitted).

Regardless, none of the three references Petitioner cites show that a POSITA would have added dummy channels to Fujiki, where columnar portions 60 and through-via 78 already provide adequate structural support as discussed above. Campbell ¶¶36-40. Instead, all three references disclose, at most, devices with “regions” (that Fujiki lacks) to accommodate the alleged “dummy channels.”

For example, Kai's Figure 6A, annotated below, discloses a “contact region 300” (yellow) where “support pillar structure[s] 20” (blue) are formed. Kai (Ex. 1015), 6:2-5, 16:28-31; *see also id.*, Fig. 15A (showing “support pillar structure 20” only in the connection region).



Kim similarly discloses that its “dummy holes DH” (blue) are in a “connection region CTR” (yellow). Kim (Ex. 1017) [0047] (“The stack structure ST may be penetrated with a plurality of dummy holes DH on the connection region CTR”). And Park is about a “semiconductor device” that includes “dummy regions,” separate from the rest of the memory. Park (Ex. 1016), Abstract.

Thus, at most, the cited references, Kai, Kim, nor Park, teach forming dummy channels in regions designed to accommodate dummy channels, such as a “contact region” (Kai), “connector region CTR” (Kim), or “dummy region” (Park). Campbell ¶40. The Fujiki device does not include any such regions, and Petitioner provides no explanation as to how, why, or where a POSITA would form such regions in the Fujiki device for unnecessary dummy channels. Campbell ¶¶36-40.

Petitioner's remaining arguments fail as well. Petitioner points to various alleged reasons why dummy channels are suitable to use as "support structures"—e.g., that they "can be made by the same process and at the same time as the active channels," "do not require connections to upper-level devices," "provide[] additional structural support," and improve "uniform[ity]." Pet. 45-46. Petitioner misses the point. As discussed, Fujiki already discloses that its columnar portions 60 and through-via 78 provide structural support for the memory array during the replacement gate process. *See supra*; Fujiki, Fig. 9. Petitioner does not (as it cannot) argue that those columnar portions 60 and through-via 78 do not serve that purpose. *See supra*.⁴ Thus, even if dummy channels may be suitable "support structures," a POSITA would not be motivated to implement them in Fujiki as proposed.

Finally, Petitioner argues that "adding dummy structures would result in reducing the likelihood of defective bits on the edge of the memory cell region,

⁴ To the extent dummy structures may have benefits such as improving uniformity, such benefits are the result of evenly spacing dummy structures throughout the device. Petitioner provides no explanation how this would be implemented in Fujiki, which already discloses columnar portions 60 and through-via 78 extending through the stack. *See supra*.

because the inclusion of the additional rows extends the memory cell pattern for those respective columns into the dummy region.” Pet. 45. Petitioner cites nothing in Kai, Kim, Park, or anything else from the relevant timeframe that teaches “the inclusion of the additional rows” that “extends the memory cell pattern.” *Id.* To the contrary, as discussed, those references do not disclose dummy structures in the memory cell area at all; they disclose only dummy channels *outside* of the memory cell. *See supra*; Campbell ¶¶36-40, 42.⁵ And Petitioner ignores the fact that adding “additional rows” in the “memory cell pattern” will increase device size, which a POSITA would understand is not desirable. Campbell ¶¶36-40, 42.

In short, a POSITA would not be motivated to modify Fujiki to add dummy channels as Petitioner proposes.

⁵ Although Dr. Lee asserts that dummy channels can be employed “at the edge of the array” to provide support to mitigate against abnormalities (Ex. 1003 ¶117), he fails to show that this is a concern in Fujiki, which employs a peripheral-under-channel (PUC) design and has sufficient support structure. Campbell ¶42.

B. Fujiki and the POSITA's knowledge do not teach or suggest "simultaneously etching" a "first opening through the stack" and a "second opening outside of the stack" (claims 3, 4, 9-10, 18, 20).

Claim 3 recites "wherein forming the first opening comprises simultaneously etching the first opening through the stack and a second opening outside of the stack." Claim 4 depends from claim 3. Claim 9 similarly recites "simultaneously etching the first opening through the stack, a second opening outside of the stack, and a third opening through the stack." Claim 10 depends from claim 9. Claim 18 also recites "simultaneously etching a first opening through the stack, a second opening outside of the stack, and a third opening through the stack." Claim 20 depends from claim 18.

Petitioner identifies Fujiki's "through-vias in the middle of the stack" and "contacts 81 to 83" outside of the stack. Pet. 46-47 (citing Ex. 1003 ¶125). Petitioner acknowledges that Fujiki does not disclose "simultaneously etching" the "through-vias" and "contacts 81 to 83." Pet. 47. Petitioner nevertheless alleges that "it would have been understood, and certainly obvious, that Fujiki would (or could) simply etch all contact holes for Fujiki's TAC and contacts 82 or 83 at once." *Id.* Petitioner is wrong.

First, Petitioner asserts that "through-vias" and "contacts 81 to 83" could be formed simultaneously "just as Fujiki does with its channel holes." *Id.* Not so. Fujiki discloses simultaneously etching "channel holes" (referred to as "memory

holes 93”) that are all formed “through the stack.” Fujiki, Fig. 7. Petitioner provides no explanation as to how or why simultaneously etching holes “through the stack” means “all contact holes”—both “through the stack” *and* “outside of the stack”—may be “simultaneously” etched. And although Petitioner cites to Dr. Lee’s Declaration for support (Pet. 47 (citing Ex. 1003 ¶¶124-126)), Dr. Lee does not even mention channel holes in the cited paragraphs, let alone justify how their formation relates to through-vias and contacts 81-83. Campbell ¶47.

To the contrary, Fujiki’s disclosed etching process for the memory holes 93 *cannot* form openings “through the stack” and “outside the stack” simultaneously. To form the “memory holes 93” simultaneously, Fujiki discloses a “reactive ion etching (RIE)” process where ions “*collide selectively* with the stacked body 50.” Fujiki [0051] (emphasis added), Fig. 7; Campbell ¶48. That etching process cannot simultaneously etch openings outside of the “stacked body” because the ions “selectively” etch only the “stacked body.” Campbell ¶48. In other words, Fujiki’s etching process deliberately avoids etching openings “outside of the stack” when selectively etching the openings “through the stack.” *Id.* ¶¶48-49. That is the opposite of what the claims require. Petitioner does not address Fujiki’s disclosed etching process.

Second, Petitioner cites other references purportedly showing the general knowledge of a POSITA with respect to simultaneously formed openings. But as

discussed above, this is not a case where the missing limitation in question is “unusually simple” or “the technology particularly straightforward,” and therefore not a case where general knowledge of a POSITA can supply a missing limitation in Fujiki. *Motorola*, IPR2024-00688, Paper 7 at 29 (denying institution). The claimed simultaneous etching absent from Fujiki involves complex semiconductor processes, such as DRIE (deep reactive ion etching). ’254 patent, 12:24-45; *DSS Tech. Mgmt.*, 885 F.3d at 1374 (rejecting Board’s reliance on “common knowledge” to “supply a missing claim limitation” because wireless communications is not “particularly straightforward” technology). And 3D NAND technology is plainly not “particularly straightforward.” *See DSS Tech. Mgmt.*, 885 F.3d at 1374 (rejecting Board’s reliance on “common knowledge” to “supply a missing claim limitation” because wireless communications is not “particularly straightforward” technology); *Campbell* ¶50. Petitioner’s reliance on “general knowledge” to supply the missing limitations directed to “simultaneously etching” openings “through the stack” and “outside of the stack” is legal error.

Third, even if the cited references can supply the missing limitation, none of the cited references disclose simultaneously etching openings “through the stack” and “outside of the stack.”

Tessariol. Petitioner cites Figure 9 of Tessariol and alleges that Tessariol discloses forming “dummy-structure openings 56” and “via openings 54” “at the

same time.” Pet. 53-54 (citing Tessariol (Ex. 2023) [0037], Fig. 9). But openings 56 and 54 are both “through the stack” as shown in Figure 8. Tessariol does not disclose simultaneously etching a hole “through a stack” *and* a second hole “outside the stack” as claimed. Campbell ¶51. Even Petitioner only characterizes Tessariol as teaching that “it was known to form openings for different structures at the same time.” Pet. 48 (citing Tessariol, Fig. 9).

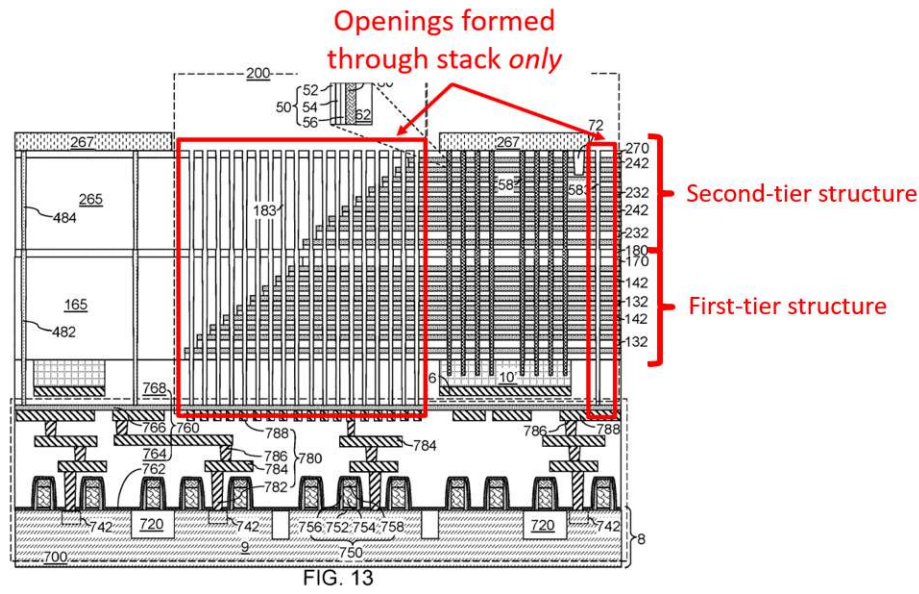
Mushiga. Petitioner cites Figure 5 of Mushiga, which shows structures 588 inside and outside the stack. Pet. 48-49. But Mushiga does not disclose anything about the timing of forming the openings that become structures 588—let alone teach “simultaneously” etching openings both “through the stack” and “outside of the stack.” *Id.* 43 (citing Mushiga (Ex. 1010), Fig. 5, 10:31-58).⁶

Masamori. Petitioner next cites Figure 13A of Masamori and alleges that Masamori disclosing forming contacts 86, 84 and 82 simultaneously. Pet. 49-50. As shown in Figure 13A, none of those contacts extend “through the stack.” *Id.* (citing Masamori (Ex. 1019), Fig. 13A). Petitioner cites, as another example,

⁶ Mushiga, at most, discloses the timing of the formation of the cavities in relation to the formation of the conductive layers 146, 246, but this does not teach simultaneous formation of cavities through and outside the stack. Mushiga, 10:49-57; Campbell ¶52.

Figure 8A of Masamori and alleges that structures 26, 28, 126, and 128 are formed simultaneously. *Id.* (citing Masamori, Fig. 8A). Those structures, however, all extend “through the stack.” *Id.* Thus, Masamori discloses, at most, forming openings that are not “through the stack” simultaneously and *separately* forming openings “through the stack” simultaneously—not simultaneously etching openings *both* “through the stack” *and* “outside of the stack” as claimed. Campbell ¶53.

Kai II. Petitioner cites Figure 4A of Kai II and Kai II's disclosure that “various first-tier openings (149, 181, 481, 581)” are formed “concurrently, i.e., during the first anisotropic etch process.” Pet. 52 (citing Kai II (Ex. 1038), 17:3-44). But Petitioner ignores that this is just an intermediate step that forms openings in an intermediate structure (i.e., the first-tier structure). Kai II, 20:56-60; Campbell ¶55. As shown in Figure 13, annotated below, later steps of Kai II's manufacturing process form openings for TACs through both first- and second-tier structures by masking the areas “outside of the stack” with mask 267 while etching the openings “through the stack”—i.e., the openings are formed sequentially, not simultaneously. Campbell ¶¶55-56.



Additionally, the cited disclosures of Kai II disclose that the intermediate openings 149, 181, 481, and 581 are merely formed during the same “first anisotropic etch process”—not that the openings are all formed “simultaneously.”⁷ Kai II contemplates that an etch processes may be performed “iteratively” or comprise “a series of reactive ion etch processes.” Kai II, 16:42-49, 23:18-26. Thus, Kai II’s disclosure of forming intermediate openings “during the first anisotropic etch process” does not mean the actual openings are formed “simultaneously” as Petitioner suggests.

⁷ Petitioner asserts that all terms should be given their “plain and ordinary meaning.” Pet. 25. The plain and ordinary meaning of “simultaneously” is “at the same time” (Ex. 2009-003)—not “during the same etch process.”

Finally, Petitioner asserts that “it was known when implementing *TACs*, the typical configuration includes multiple TACs” and cites references about “multiple *TACs*.” Pet. 53 (emphases added) (citing Mushiga, Nakajima (Ex. 1005)). TACs are “*through-array* contacts.” Campbell ¶23. Such “through-array” contacts, by definition, are only etched “through the stack.”⁸ Campbell ¶23. Forming “multiple TACs” that are all “through the stack” does not disclose also simultaneously forming openings “outside of the stack” as Petitioner baldly suggests. *Id.* ¶46.⁹ Although Petitioner cites paragraph 126 of Dr. Lee’s declaration for support, Dr. Lee merely parrots the conclusory allegations of the Petition. Pet. 53.

In short, none of the references Petitioner cites as purportedly demonstrating the “general knowledge of a POSITA” teach “simultaneously etching” openings

⁸ Petitioner cites Nakajima, which is the primary reference relied on in its first-filed Petition. As discussed in Patent Owner’s Preliminary Response, Nakajima teaches etching all H1 holes for the C4 structures “through the stack.” Campbell ¶46.

⁹ Even if Petitioner were correct that Fujiki contemplates simultaneously etching “through-vias” (it does not), that does not disclose or suggest that the “through-vias” *and* “contacts 82 and 83” (which are not “through-vias”) are etched simultaneously. Campbell ¶46.

both “through the stack” *and* “outside the stack.” If anything, they confirm that it was neither routine nor predictable to do so.

Petitioner has failed to establish that Fujiki renders obvious “simultaneously etching” a “first opening through the stack” and a “second opening outside of the stack.”

C. Fujiki and the POSITA's knowledge do not teach or suggest “forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening” (claims 7, 8, 14, 15).

Claim 7 recites “forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening.” Claim 8 depends from claim 7. Claim 14 depends from claim 11, which is unpatentable for the reasons shown above with respect to the dummy channel. Further, claim 14 also recites “forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening.” Claim 15 depends from claim 14. Notably, “the first opening” in claims 7 and 14 is the opening through which the “through array contact (TAC)” is formed in independent claims 1 and 11.

Petitioner acknowledges that Fujiki does not explicitly disclose this limitation. *See* Pet. 62.

Petitioner instead asserts that Fujiki alone renders this limitation obvious under two interpretations of the claim: (i) where the “shallow recesses” may be

“unintentional recesses,” and (ii) where the “shallow recesses” must be “intentional” and “actual” recesses. Both fail.

1. Ground 1 fails under a claim interpretation that includes “undetectable and unintentional recesses.”

Petitioner asserts that “PO interprets this claim to include largely undetectable and unintentional alleged recesses.” Pet. 63. Although purporting to cite one page of YMTC’s infringement contentions, those contentions say nothing about “undetectable and unintentional” recesses. *See* Ex. 1029.

As an initial matter, Petitioner cannot meet its burden under a construction that it agrees is wrong. *See Samsung Elecs. Am., Inc. v. UNILOC 2017 LLC*, IPR2020-00046, Paper 6 at 7-8 (Apr. 1, 2020) (declining to address grounds based on constructions Petitioner asserted were wrong).

Petitioner cannot establish obviousness under this interpretation either. Petitioner asserts that “typical prior art etches ... were also known to result in lateral recesses in either the dielectric spacers or sacrificial layers.” Pet. 63-64. As support, Petitioner cites a patent that says the opposite: In “3D NAND memory, *it is important to have an etching gas* which can etch both SiO₂ and SiN layers ... *without selectivity*.” *Id.* 64 (emphasis added) (citing Ex. 1030, 2:59-67). Etching gasses “without selectivity” etches the layer stack evenly, without recesses. Campbell ¶60.

To the extent Petitioner relies on the cited patent's statement that "it is a challenge to find" a gas that can etch "without selectivity," that does not mean POSITAs would be motivated to use gases *with* selectivity that would result in unintentional recesses. Ex. 1030, 2:59-67. In fact, the opposite is true: "[I]t is *important*" to use a gas "*without selectivity*" that therefore avoids recesses. *Id.* (emphases added).

Thus, Petitioner failed to meet its burden to show that a POSITA would ignore the teachings of Exhibit 1030 and use a gas with selectivity to form undetectable and unintentional recesses.

2. Ground 1 fails under a claim interpretation that requires "intentional" formation of "actual recesses."

Petitioner acknowledges that Fujiki does not disclose "forming a plurality of shallow recesses" based on Petitioner's "interpretation" of the claim that requires the "intentional" forming of "actual recesses." Pet. 63 ("[T]he '254 Patent makes clear that these limitations relate to an intentional etch that forms actual recesses in the sacrificial layers.").

Under this interpretation, Petitioner asserts that "[i]t was well known that an option for a TAC or other through-memory structures was to have a ribbed shape, that is, forming recesses in one of the stack layers." *Id.* 64. As discussed above, this is not a case where the missing limitation in question is "unusually simple" or "the technology particularly straightforward," and therefore not a case where

general knowledge of a POSITA can supply a missing claim limitation in Fujiki. *Motorola*, IPR2024-00688, Paper 7 at 29 (denying institution). Forming “recesses” in “sacrificial layers” during the manufacture of 3D NAND devices requires, among other things, that “the lateral dimension of shallow recess” be “controlled by the etching rate and/or etching time.” ’254 patent, 13:48-61. It is a highly technical and complex process—the opposite of “unusually simple” or “particularly straightforward.” Campbell ¶61. Petitioner’s arguments again fail for this reason alone.

Petitioner’s reliance on the “the knowledge of a POSITA” fails on the merits as well.

First, according to Petitioner, Cui discloses an embodiment that “intentionally creates **large recesses** in the insulating layers”—Petitioner’s own words. Pet. 64 (emphasis added) (citing Cui (Ex. 1031), Fig. 16A, 26:23-33). Cui’s “**large** recesses” are plainly not “**shallow** recesses.” They are the opposite. Petitioner makes no attempt to explain why Cui’s “large recesses” somehow render obvious forming “shallow recesses” in Fujiki.

Second, Cui discloses recesses in **insulating** layers. Cui, 26:23-27 (“[A]n isotropic etch process can be performed to laterally recess the **insulating layers** (132, 232) with respect to the spacer material layers such as the first and second sacrificial material layers (142, 242).”) (emphasis added). The claims, however,

require forming the “shallow recesses” by “removing parts of the *sacrificial layers*”—not “insulating layers.” In fact, Cui’s etching deliberately does *not* form recesses in the sacrificial layers 142 as required by the claims of the ’254 patent.

Id.; see also *id.*, Fig. 16A; Campbell ¶62.

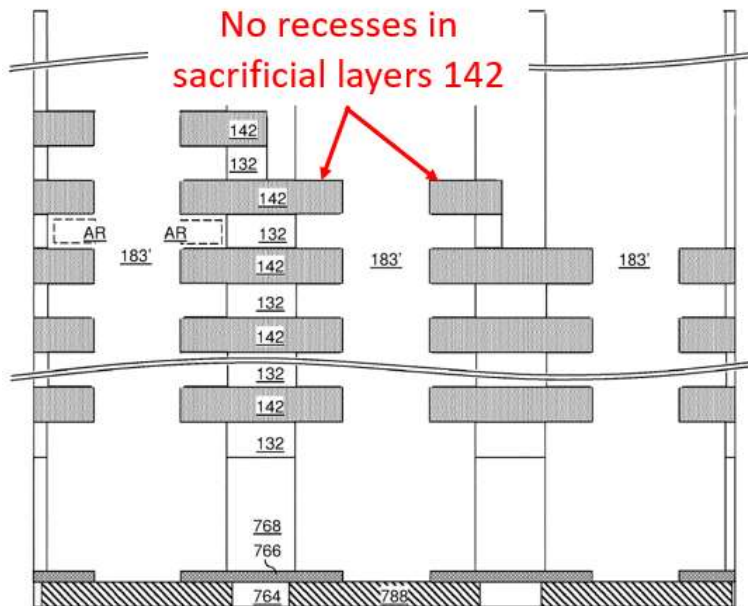


FIG. 16A

To remedy this deficiency, Petitioner further cites to Kai for disclosure of forming “recesses in sacrificial gates” not in relation to an opening for a TAC. Pet. 66 (citing Kai, 11:9-34). Kai says nothing about forming recesses in the “sacrificial layers” of an alternating stack of dielectric and sacrificial layers for openings associated with a TAC as claimed. Campbell ¶63. Regardless, Petitioner’s cursory citation to Kai with a parenthetical stating “recesses in sacrificial gates” fails to establish that a POSITA would implement the claimed

“shallow recesses” formed by “removing parts of the sacrificial layers” in Fujiki as claimed.

Third, Petitioner fails to establish that a POSITA would be motivated to modify Fujiki to form “shallow recesses” as claimed based on Cui or Kai. To the contrary, Petitioner blatantly relies on impermissible hindsight by cherry-picking “ribbed via cavity” of Cui and alleging that a POSITA would combine it with Fujiki because it “serves the same purpose as the ’254 Patent.” Pet. 65 (“The ribbed via cavity serves the same purpose as the ’254 Patent, namely, providing additional area for the dielectric liner.”). Indeed, after citing the ’254 patent’s disclosures Petitioner concludes: “Accordingly, in view of the knowledge of a POSITA, it would have been obvious, and a POSITA would have been motivated to create a ribbed via cavity in Fujiki’s through-array via holes.” *Id.* That is the epitome of hindsight.

IV. The Board should exercise its discretion and deny institution under 35 U.S.C. § 314.

Institution of an IPR is always discretionary. 35 U.S.C. § 314(a). Here, the Board should exercise its discretion to deny institution because the Petition will not serve as an effective and efficient alternative to litigation. Rather, the overall balance of the *Fintiv* factors shows that “efficiency, fairness, and the merits support the exercise of authority to deny institution.” *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (Mar. 20, 2020) (precedential).

A. Factor 1 favors denial if the district court denies Petitioner's motion to stay and lifts the temporary stay before institution.

The Court has temporarily stayed the Parallel Proceeding¹⁰ while it considers Petitioner's motion for a stay pending IPRs. Ex. 2001; Ex. 2003. The Parallel Proceeding involves 70 asserted claims from 19 patents. Ex. 2002 at 006. Of those, the Board has only instituted IPRs against 23 claims from 8 patents. Ex. 2002 at 006. And 11 claims from one patent have had IPR institution denied across the board. *Id.*; see, e.g., *Entangled Media, LLC v. Dropbox Inc.*, 732 F. Supp. 3d 1120, 1124 (N.D. Cal. 2024) (characterizing arguments about simplification as “premature” “[b]ecause the PTO has not yet instituted proceedings,” and denying motion to stay); *Skillz Platform Inc. v. Aviagames Inc.*, No. 21-cv-02436-BLF, 2022 WL 1189882, at *3–4, *5 (N.D. Cal. Apr. 21, 2022) (denying motion to stay, stating that any simplification from IPRs “is purely speculative at this stage,” and “the cost of non-institution would be delay without benefit”).

¹⁰ *Yangtze Memory Technologies Company, Ltd. V. Micron Technology, Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.).

It is not clear how long the temporary stay will remain in effect.¹¹ However, if the district court denies Petitioner's stay motion and lifts the temporary stay, Factor 1 would favor denial. *Inergy Tech., Inc. v. Force MOS Tech. Co.*, IPR2024-00094, Paper 9 at 32 (May 21, 2024) (denial of stay motion favors discretionary denial of IPR petition); *see also Fintiv*, Paper 11 at 7-8 (similar).

For these reasons, this factor favors discretionary denial of institution.

B. Factor 2 is neutral because the trial date is three days after Final Written Decision.

Trial is set to begin in the Parallel Proceeding on June 15, 2026.¹² Ex. 1033 at 002. That is three days after the statutory deadline for a Final Written Decision in this case (June 12, 2026). And it is *well before* the expected Final Written Decisions that would issue in *eight* other proceedings filed by Micron against patents at issue in the Parallel Proceeding. *See* IPR2025-00190, -00191, -00228, -

¹¹ YMTC reserves its rights to address changes in the district court proceeding as they relate to discretionary denial in future briefs.

¹² Petitioner's assertion of a 48.9-month median time to trial (Pet. 11 (citing Ex. 1034)), misleadingly includes non-jury trials, which have a significantly longer time-to-trial. *See* Ex. 2004 at 003. The corresponding number for jury trials is 32.8 months. Ex. 2004 at 003.

00229, -00244, -00245, -00294, and PGR2025-00021. This factor therefore favors denial of institution, or is at worst neutral. *Fintiv*, IPR2020-00019, Paper 11 at 9 (“If the court’s trial date is at or around the same time as the projected statutory deadline, ... the decision whether to institute will likely implicate other factors”); *Catalyst Orthoscience Inc. v. Shoulder Innovations, Inc.*, PGR2024-00042, Paper 17 at 12-14 (Dec. 19, 2024) (finding Factor 2 neutral where scheduled trial was “just weeks” after the scheduled conclusion of the PGR). A Final Written Decision here would issue after expert discovery, after dispositive motions, and after the pretrial conference. Ex. 1033 at 002.

C. Factor 3 favors denial because substantial effort will have been expended by the deadline for institution.

The parties have expended, and continue to expend, substantial resources into the Parallel Proceeding. In that case, the parties have collectively propounded, responded to, and supplemented responses to 38 interrogatories and 117 requests for production. The parties have already produced over 113,000 pages of documents and are continuing to produce thousands more pages of documents. Ex. 2002 at 012. They have also engaged in extensive source code discovery, which has involved 14 days of YMTC expert and/or attorney review of code in this District and, more recently, three weeks and counting of code review at Micron’s headquarters in Boise, ID. Ex. 2002 at 012. And upon order of the Court, YMTC

has narrowed its claims of infringement to 70 asserted claims, which has required extensive analysis of infringement, validity, and damages issues. Ex. 2002 at 012.

The parties have also devoted, and continue to devote, substantial effort to claim construction, including exchanging claim terms and proposed constructions and filing a Joint Claim Construction and Prehearing Statement. The parties have also exchanged expert declarations in connection with claim construction and conducted two claim construction expert depositions.

Petitioner's assertion that the parties and district court have invested "very little" in the Parallel Proceeding is both wrong and, at the time of this filing and the institution decision, outdated. Pet. 11. Petitioner does not even address the substantial effort invested in the Parallel Proceeding in the more than 7 months between filing and the Board's institution decision. Because the parties and the Court will expend significant effort in the parallel litigation *before institution*, this factor favors discretionary denial of institution. *See, e.g., Comcast Cable Commc'ns, LLC v. Touchstream Techs., Inc.*, IPR2024-00323, Paper 13 at 9-10, 2024 WL 3530021, at *4 ("Factor 3 favor[ed] denial" where "substantial work on claim construction [had] happened," and "the related district court litigation ha[d] progressed in other aspects as well," including with respect to contentions); *10x Genomics, Inc. v. President & Fellows of Harvard Coll.*, IPR2023-01299, Paper 15 at 18, 2024 WL 993828, at *8 (similar, noting that the parties had exchanged

contentions, “completed claim construction briefing,” and that the “district court ha[d] also considered two motions to dismiss and presided over several discovery disputes”); *Boe Tech. Grp. Co. v. Element Cap. Com. Co. Pte. Ltd.*, IPR2023-00808, Paper 9 at 23, 2023 WL 7715885, at *8 (finding “the parties and the District Court ha[d] invested substantial resources in th[e] litigation” because, among other things, “[s]ignificant discovery ha[d] been completed, including the exchange of infringement and invalidity contentions, document requests and interrogatories, and proposed claim terms for construction”).

D. Factor 4 favors denial because there is significant overlap between the issues raised in the Petition and the district court proceeding.

Petitioner Micron has served invalidity contentions identifying the same art from its Petition, and explicitly incorporating its IPR petition by reference. Petitioner has also not filed a *Sotera*-type stipulation in this proceeding. *Cf. Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (Dec. 1, 2020) (precedential). Although Petitioner stipulates in its Petition that “[s]hould the Board institute, Micron... will not advance in District Court any ground asserted in this Petition,” no such stipulation has been made in the district court. Pet. 12. Such a narrow stipulation runs the risk of significant overlap both in consideration of the same evidence and arguments framed as “different grounds” than the Petition. Because such a narrow stipulation risks having the district court address substantially the same evidence and arguments that the Board will have to address

should it institute an IPR, and on a similar timeline, an IPR of the '254 patent would be an inefficient use of the Board's resources and would risk conflicting decisions. *See 10x Genomics*, IPR2023-01299, Paper 15 at 20, 2024 WL 993828, at *9 (“[W]e agree with Patent Owner that the overlapping art and arguments presented in the parallel proceeding weigh in favor of exercising our discretion to deny institution.”) (footnote omitted); *see also Comcast*, IPR2024-00323, Paper 13 at 12, 2024 WL 3530021, at *5 (questioning whether a narrower stipulation “not to pursue in the District Court any ground that utilizes the same combination of prior art references relied upon in the instituted petition” adequately addressed “concerns of inefficiency and the possibility of conflicting decisions”).

E. Factor 5 favors denial because Micron is the defendant in the district court proceeding.

Petitioner is the defendant and counterclaimant in the parallel district court case and, as such, will have a full and fair opportunity to litigate its (overlapping) invalidity contentions in that forum. Thus, this factor favors discretionary denial. *Comcast*, IPR2024-00323, Paper 13 at 13, 2024 WL 3530021, at *5 (“Petitioner is the defendant in the related district court case.... We find that this factor favors denial.”) (citations omitted); *Boe Tech.*, IPR2023-00808, Paper 9 at 24-27, 2023 WL 7715885, at *9.

F. Factor 6: The limited resources of the Board favors denial.

“The sixth *Fintiv* factor takes into account other circumstances that may bear on the decision to exercise discretion to deny, such as the merits of the patentability challenges.” *Comcast*, IPR2024-00323, Paper 13 at 13, 2024 WL 3530021, at *5 (citation omitted). For the reasons explained in Section III, the Petition fails on the merits for numerous reasons, including because Petitioner fails in its repeated attempts to fill Fujiki’s holes with alleged “knowledge of a POSITA,” and thus does not present a “particularly strong” showing that can tip the scales in favor of institution. *Fintiv*, IPR2020-00019, Paper 11 at 14-15 (“[I]f the merits of a ground raised in the petition seem particularly strong on the preliminary record, this fact has favored institution.... [I]f the merits of the grounds raised in the petition are a closer call, then that fact has favored denying institution when other factors favoring denial are present.”) (citations omitted); *see also USPTO Rescinds Memorandum Addressing Discretionary Denial Procedures* (Feb. 28, 2025), available at <https://www.uspto.gov/about-us/news-updates/uspto-rescinds-memorandum-addressing-discretionary-denial-procedures> (compelling merits analysis no longer applicable).

As five of the six *Fintiv* factors favor discretionary denial of institution, and the remaining factor is, at worst, neutral, Patent Owner respectfully requests that the Board exercise its discretion to deny institution.

V. Conclusion

For the reasons set forth above, the Board should deny the Petition for Inter Partes Review.

Respectfully submitted,

Dated: March 12, 2025

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CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

I hereby certify that this Patent Owner's Preliminary Response complies with the word count limitation of 37 C.F.R. § 42.24(b)(1) because the Patent Owner's Preliminary Response contains 7,219 words using Microsoft Word's counting feature, excluding the cover page, signature block, and the parts of the Patent Owner's Preliminary Response exempted by 37 C.F.R. § 42.24(b)(1).

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 12th day of March, 2025, a true and correct copy of the foregoing **Patent Owner's Preliminary Response and all Exhibits** were served by electronic mail on Petitioner's lead and backup counsel at the following email addresses:

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