

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: March 12, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00119
Patent 10,879,254

**DECLARATION OF STEPHEN CAMPBELL
IN SUPPORT OF
PATENT OWNER'S PRELIMINARY RESPONSE**

Table of Contents

I.	Introduction and Qualifications	2
II.	Summary Of Materials Reviewed And Considered	4
III.	Understanding of Legal Standards.....	5
A.	Claim construction	6
B.	Obviousness	7
IV.	Level of Ordinary Skill in the Art.....	11
V.	Overview of the '254 patent	11
VI.	A POSITA would not have found claims 2-4, 7-15, 17-18, and 20 obvious in view of Fujiki.....	15
A.	Claims 2, 11-15, 17 (“dummy channel...through the stack”).....	16
B.	Claims 3-4, 9-10, 18, 20 (“simultaneously etching” a “first opening through the stack” and a “second opening outside of the stack”)	25
C.	Claims 7-8, 14-15 (“forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening”)	34
VII.	CONCLUSION.....	39

I. Introduction and Qualifications

1. I have been retained by Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Petitioner”) to provide my opinion concerning the validity of U.S. Patent No. 10,879,254 (Ex. 1001).

2. I received my Bachelor's degree in Physics from the University of St. Thomas (St. Paul, Minnesota) in 1975, and my M.S. and Ph.D. in Physics from Northwestern University (Evanston, Illinois) in 1978 and 1981, respectively. I then joined Sperry, now called Unisys, in 1981 as a CMOS process development engineer. In 1982, I was assigned the lead engineer for the 1.2 μm technology process development effort. In 1984 I was promoted to head of silicon research for the company. This involved a wide variety of process technologies for submicron CMOS.

3. In 1986, I joined the University of Minnesota as an Assistant Professor in the Electrical Engineering Department. My research at the University involved semiconductor processing, materials, and device structures. I raised more than \$100M in various grants and successful submissions to companies and industry consortiums such as the Semiconductor Research Association, as well as State and US government agencies including DARPA and the National Science Foundation. The first ten years of my career at the University concentrated on the development of rapid thermal annealing for 200

mm wafers, particle control in CVD systems, and the development of high uniformity rapid wafer annealing systems. The next ten years were dedicated to the invention and development of high permittivity (aka high-k) films for use as gate insulators. This is necessary to allow the development of deeply scaled CMOS devices. This technology has been widely adopted for nanoscale CMOS devices. In the last fifteen years at the University, my work involved the development of low-cost tandem photovoltaics and micro electromechanical systems (MEMS). The latter included a chronic deep brain sense/stimulation system and very high-speed mechanical switches. Finally, I developed processes for the fabrication of novel 2D materials such as black arsenic, and fabricated transistors using these materials. I retired from the University in 2021.

4. A brief summary of my work at the University would include:

- Approximately 200 publications
- The leading textbook on semiconductor technology. Currently in its fourth edition, *Fabrication Engineering at the Micro and Nanoscale* (Oxford 1996, 2000, 2008, 2013) is the dominant text on the topic.
- Honors from outside the University such as being named a Presidential Young Investigator by the National Science

Foundation and a Life Fellow by the Institute of Electrical and Electronic Engineers (IEEE).

- Honors within the University including outstanding service and outstanding teaching.
- As the Director of the University's Nanofabrication Center, I increased lab usage from 30 to more than 300 users, enabling millions of dollars research awards annually by Minnesota faculty, and leading to the construction of a new \$80M building with an expansive cleanroom facility.

5. Since retiring from the University, I have consulted with semiconductor companies including patent litigation.

6. Additional information regarding my education, technical experience and publications, including a list of the U.S. patents of which I am an inventor/coinventor, is included in my *Curriculum Vitae*, which I understand is attached as Exhibit 2006.

II. Summary Of Materials Reviewed And Considered

7. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, while drawing on my experience in the field of semiconductor fabrication, I reviewed the following documents:

Ex.	Description
1001	United States Patent No. 10,879,256 (“the ’254 patent”)
1002	File History for the ’254 patent (“’254 FH”)
1003	Declaration of Jack C. Lee
1004	Curriculum Vitae of Jack C. Lee
1005	U.S. Patent 10,777,501 to Nakajima et al. (“Nakajima”)
1006	U.S. Patent Appl. Publ. 2019/0198524 to Fujiki et al. (“Fujiki”)
1010	U.S. Patent 10,354,980 to Mushiga et al. (“Mushiga”)
1015	U.S. Patent 10,290,643 to Kai et al. (“Kai”)
1016	U.S. Patent 9,859,297 to Park et al. (“Park”)
1017	U.S. Patent Appl. Publ. 2018/0308559 to Kim et al. (“Kim”)
1018	U.S. Patent No. 10,115,632 to Masamori et al. (“Masamori”)
1023	U.S. Patent Appl. Publ. 2019/0081061 to Tessariol et al. (“Tessariol”)
1031	U.S. Patent 10,304,852 to Cui et al. (“Cui”)
1038	U.S. Patent 10,388,666 to Kai et al. (“Kai II”)

8. My opinions are additionally guided by my appreciation of how a person of ordinary skill in the art would have understood the claims of the ’254 patent at the time of the invention, which I have been asked to assume is August 21, 2018.

III. Understanding of Legal Standards

9. I am not an attorney, and in this Declaration, I do not opine on matters of law. For the purposes of this Declaration, I have been informed about

certain aspects of the law that are relevant to my analysis and opinions. My understanding of these principles is set forth below.

10. I have been informed by Counsel that the validity analysis is a two-step process. First, the patent claims are construed to ascertain their proper scope. Second, the construed claims are compared to the identified prior art to determine if the claims are valid over the prior art.

A. Claim construction

11. I have been informed by Counsel that the claims of a patent define the limits of the patentee's exclusive rights. I have been informed by Counsel that to determine the scope of the claimed invention, courts typically construe claim terms, the meaning of which the parties may dispute. I have been informed by Counsel that claim terms should generally be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of filing of the patent application, after reading the patent and its prosecution history. I also have been informed by Counsel that a basic tenet of claim construction presumes that different words in a claim have different meanings, unless there is evidence to the contrary.

12. I have been informed by Counsel that claims must be construed in light of, and consistent with, the intrinsic evidence. In this context, I have been informed by Counsel that intrinsic evidence includes the claims themselves, the

written disclosure in the specification, and the patent's prosecution history, including prior art that was considered by the United States Patent and Trademark Office ("USPTO"). I have been informed by Counsel that the specification is always highly relevant to the claim construction analysis and often is the single best guide to the meaning of a disputed term. I have been informed by Counsel that extrinsic evidence may also be considered when construing claims and may include, for example, technical dictionaries, technical publications and books, treatises, and expert testimony.

B. Obviousness

13. I have been informed by Counsel that patent claims can be deemed invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. While such conclusions are often based on more than one piece of prior art, only one is required. It is not sufficient that a collection of prior art references merely recites the various elements of a challenged patent claim. Rather, as I have been informed by Counsel, the prior art must present the elements in a manner that is consistent with their arrangement or use in the challenged claims. I have been informed by Counsel that obviousness cannot be based on the hindsight combination of components selectively culled from the prior art.

14. I have been informed by Counsel that a person having ordinary skill in the art (i.e., a POSITA) is a hypothetical person who is presumed to have known the relevant art at the time the invention was made. I have been informed by Counsel that the condition “at the time the invention was made” is imposed to rule out impermissible hindsight. I also have been informed by Counsel that an expert is to analyze the prior art from the perspective of a person of ordinary skill in the art at the time the invention was made, and not simply to provide his/her own personal conclusions.

15. I also have been informed by Counsel that an obviousness determination includes several factual inquiries, including (1) determining the scope and content of the prior art; (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the pertinent art; and (4) taking into consideration any objective indicia of nonobviousness.

16. I have been informed by Counsel that obviousness must be determined as of the date of the invention (i.e., the effective filing date or priority date of the patent). Thus, in considering the reason or motivation to combine references, it is essential to avoid using hindsight. For example, the problem examined when considering obviousness is the general problem that confronted the inventor before the invention was made, not the specific problem solved by

the invention. Defining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness. Further, an overly narrow statement of the problem can represent a form of hindsight, because often the inventive contribution lies in defining the problem in a new revelatory way. Similarly, an assertion that a person of ordinary skill could combine the references, rather than that they would have been motivated to do so, is an impermissible form of hindsight. Moreover, knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references to reach the particular claimed invention.

17. I have been informed by Counsel that a motivation to solve a problem (or issue) is not the same as a motivation to have combined references. I have been informed by Counsel that whether a skilled artisan would be motivated to make a combination includes whether he/she would select particular references in order to combine their elements.

18. I have been informed by Counsel that the analysis of the motivation to combine should be explicit. Additionally, it must include articulated reasoning with rational underpinnings to support the conclusion of obviousness. Providing a full explanation of the motivation to combine the references and the reasonable expectation of success is a necessary component of the obviousness inquiry, as inventions in most, if not all, instances rely upon building blocks long since

uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. However, conclusory statements fail to adequately explain why a person of ordinary skill would have a motivation to combine the potential prior art references.

19. I have been informed by Counsel that common sense, common wisdom, and common knowledge may be used to support a motivation to combine, so long as the use of common sense in the analysis is explained with sufficient reasoning. But, common sense can only be used to supply a limitation missing from the prior art where the technology is unusually simple and straightforward.

20. I also have been informed by Counsel that evidence suggesting reasons to combine cannot be viewed apart from evidence suggesting reasons not to combine. In analyzing motivation, both advantages and disadvantages must be considered. Teaching away, for example, is a statement in the prior art that either (i) discourages one from following the path of the claimed invention, or (ii) encourages one to follow a path that diverges from the path of the claimed invention. The concept of teaching away bears directly on whether there was a reason to combine prior art. Known disadvantages in prior art technology or devices which would naturally discourage a search for new inventions may also be taken into account in determining obviousness.

IV. Level of Ordinary Skill in the Art

21. Dr. Lee defines a person of ordinary skill in the art (“POSITA”) as a person having “a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience).” Ex. 1003 ¶ 36.

22. For the purposes of this declaration, I have not been asked to provide an opinion on the level of ordinary skill in the art. In view of my educational background and work experience, I surpass Dr. Lee’s definition of a POSITA, and did so before August 21, 2018. Regardless of the precise definition of a POSITA, Ground 1 of the Petition does not show the challenged claims obvious. I reserve the right to opine as to an alternative level of a POSITA in other proceedings or if the Board institutes review in this proceeding.

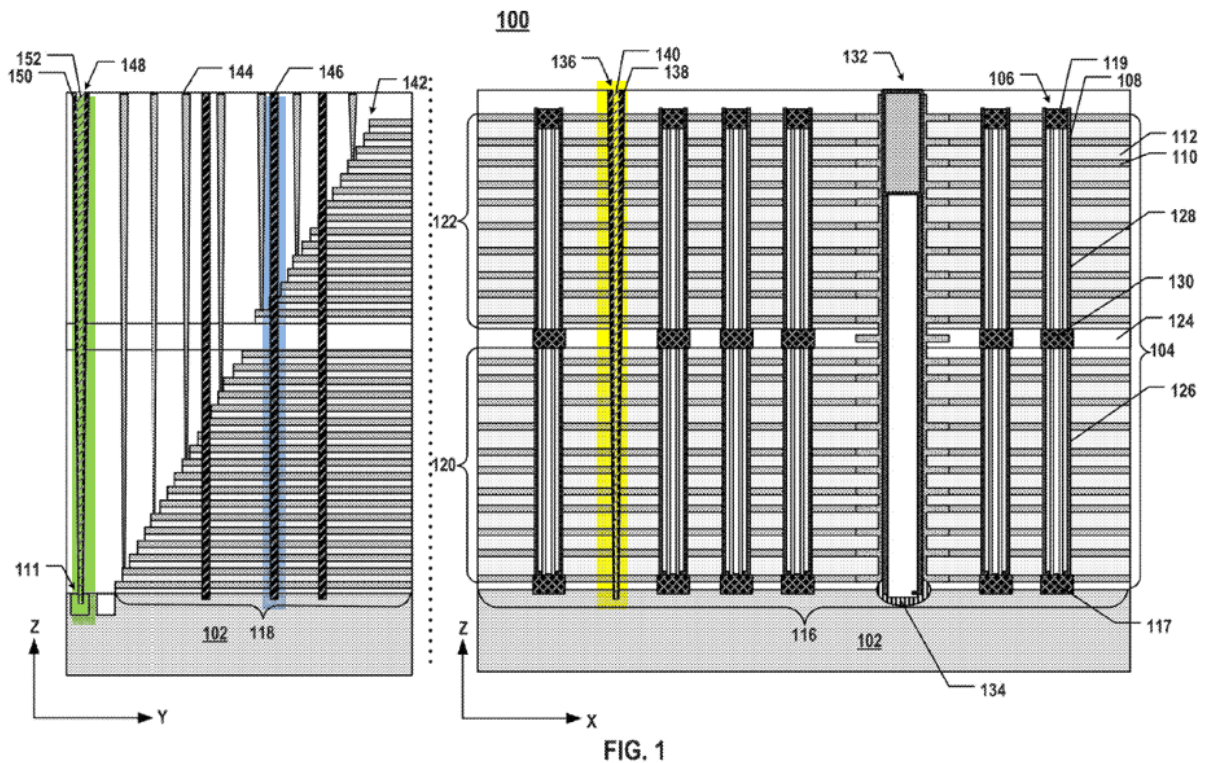
V. Overview of the ’254 patent

23. The ’254 patent recognized that 3D memory devices require contacts that go vertically through the memory stack called “through array contacts” or “TACs” for “providing vertical interconnects between the stacked memory array device and peripheral device (*e.g.*, for power bus and metal routing).” ’254 patent, 4:55-59. In the past, these TACs were formed within a “barrier structure”

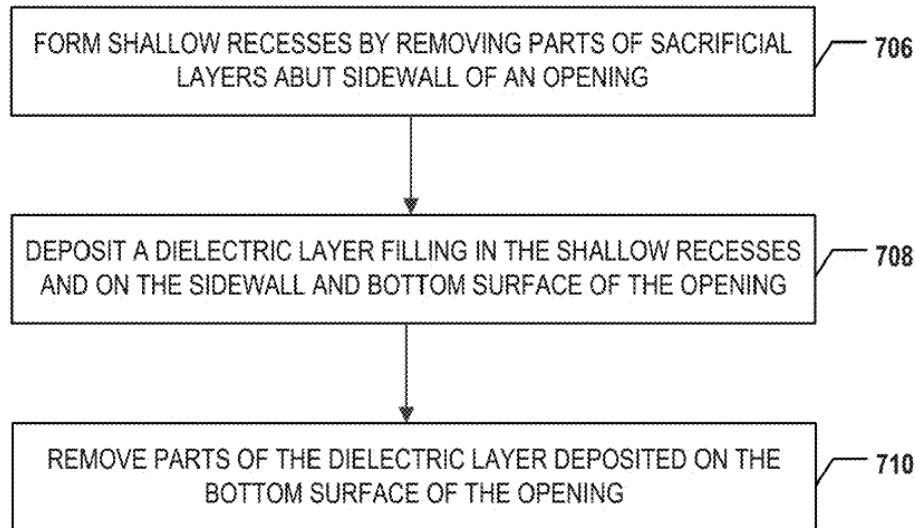
preserving a “dielectric stack region within a memory stack.” *Id.*, 4:59-62. The drawback of such a “barrier structure” is that “the regions enclosed by the barrier structures take up large area in the core array region where memory strings can be formed.” *Id.* at 4:59-65. TACs within a barrier structure “also have a negative impact on the resistance of word lines.” *Id.*, 4:59-65. “Moreover, the existing fabrication processes for forming the barrier structures become more challenging for the next generation 3D memory devices” which “have less process margin.” *Id.*, 4:66-5:2.

24. The '254 patent discloses a novel “3D memory device having TACs not enclosed by barrier structures, which resolves the above-noted issues associated with the barrier structures.” *Id.*, 5:3-6. The '254 patent explains that “by removing the barrier structures, the areas for TACs can be reduced while keeping their functions, thereby increasing memory cell density and decreasing process cost.” *Id.*, 5:6-9. In addition, “[m]ore process margin”—i.e., room for error—“may be obtained due to the elimination of etching and alignment steps for making the barrier structures.” *Id.*, 5:11-15. To “further simplify the fabrication flow and reduce process cost,” the '254 patent teaches that the non-barrier structure TACs can be “formed in the same fabrication process(es) for making other structures” such as “peripheral contacts” outside of the memory stack. *Id.*, 5:15-20.

25. Figure 1, reproduced below, illustrates a cross-section of an embodiment of a “memory stack 104” and a “staircase structure” 142. *Id.*, 8:61-63. As shown below, the memory device 100 includes a TAC 136 (yellow) that extends vertically through the stack to carry electrical signals to/from the memory device 100. *Id.*, 8:28-39. Unlike the prior art, TAC 136 is not “enclosed by barrier structures.” *Id.*, 5:3-20. This allows the TACs to be “formed in the same fabrication process(es) for making other structures,” including those *outside* the memory array such as “peripheral contact 148” (green). *Id.*, 5:3-20; 12:24-45. In addition, “dummy channel structures 146” are “disposed in the outer region 118 of memory stack 104 as shown in Fig. 1” to “provide mechanical support to the memory array structures, e.g., memory stack 104.” *Id.*, 9:39-49.



26. The '254 patent discloses additional details about forming the claimed TACs not enclosed by a “barrier structure.” Instead of forming the TACs in a “barrier structure” to isolate the TACs from other electrical components, the process for forming the TACs of the '254 patent start by forming openings in the memory stack itself for the TAC and then depositing “spacers” on the sidewalls of the openings. *Id.*, 12:64-67. Figure 7B, reproduced below, is a flowchart of an exemplary method for forming such a spacer for the first opening. *Id.*, 13:34-40. The method includes forming a plurality of shallow recesses by removing parts of the sacrificial layers the memory stack abutting the sidewall of the first opening. *Id.*, 13:36-40.

**FIG. 7B**

27. Exemplary recesses 312 are shown in Figure 3D, reproduced below. '254 patent 13:52-57. These recesses provide space for a thicker dielectric spacer deposition in step 708, resulting in improved electrical isolation, even without a barrier structure. '254 patent 13:59-61.

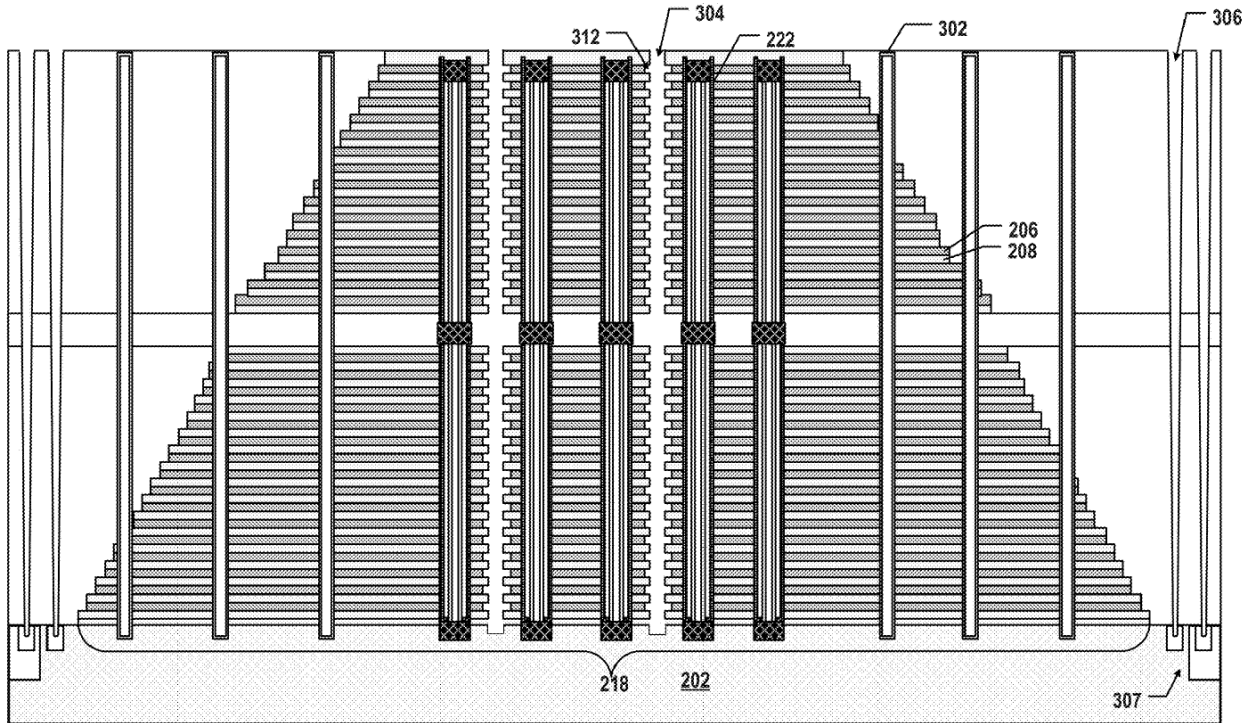


FIG. 3D

VI. A POSITA would not have found claims 2-4, 7-15, 17-18, and 20 obvious in view of Fujiki.

28. As a general matter, Dr. Lee relies on the knowledge of a POSITA to supply at least three features missing from Fujiki in relation to the challenged claims. In doing so, he relies on several patent documents from around the same time as the '254 patent. As I discuss further below, I do not agree that these documents supply the missing features, and none of the missing features are

simple. In fact, as I discuss more below, the field of 3D NAND memory manufacturing is not simple, as it pushes the limits of semiconductor fabrication in terms of size and complexity, and even seemingly small modifications can result in unforeseen problems.

A. Claims 2, 11-15, 17 (“dummy channel...through the stack”)

29. Claim 2 recites “prior to forming the first opening, forming a dummy channel structure extending vertically through the stack.”

30. Dr. Lee opines that “a POSITA would have been motivated, with a high expectation of success, to also form dummy channels for several reasons.”

Ex. 1003 ¶ 116. As an initial matter, I note that forming a dummy channel structure is not unusually simple, and involves complex semiconductor manufacturing processes, including “wet etching, and/or dry etching, such as DRIE” and “thin film deposition processes, such as ALD, CVD, PVD.” ’254 patent, 12:7-23.

31. I disagree with Dr. Lee. A POSITA would not have had any reason to add dummy channels to Fujiki.

32. Dr. Lee asserts that “dummy channels provide structure support, which is important during the gate line replacement process.” Ex. 1003 ¶ 119. But Dr. Lee omits that Fujiki explicitly illustrates gate line replacement and shows the existing pillars as providing sufficient structural support during this

process. Specifically, Figure 10, annotated below, illustrates an intermediate step during gate replacement after the sacrificial films 91 have been removed via wet etching. Fujiki [0054]. The layers highlighted yellow, below are “spaces 97” between the insulating films 51. Fujiki [0054].

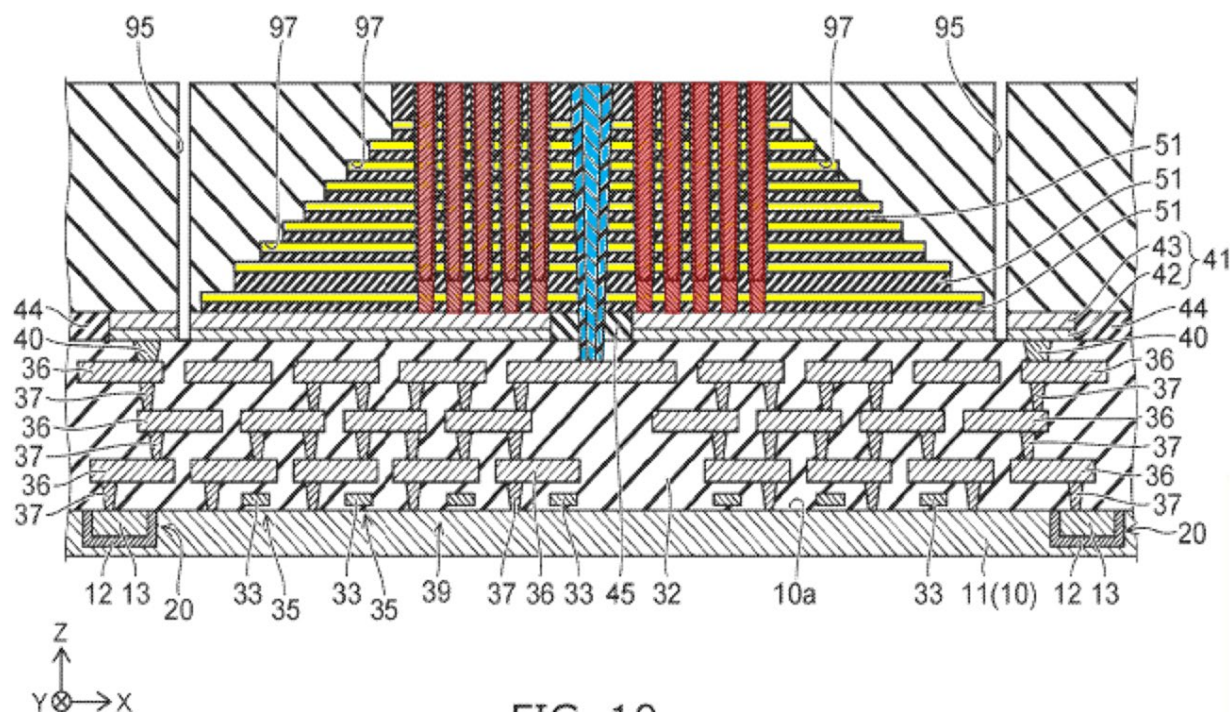


FIG. 10

The existing pillars, including columnar portions 60 (shown in red) and through-via 78 (shown in blue) provide structural support to prevent the stack from collapsing during this intermediate step when spaces 97 are formed between insulating films 51. *See also* Figure 1 (showing columnar portions 60 and through-via 78 after further processing).

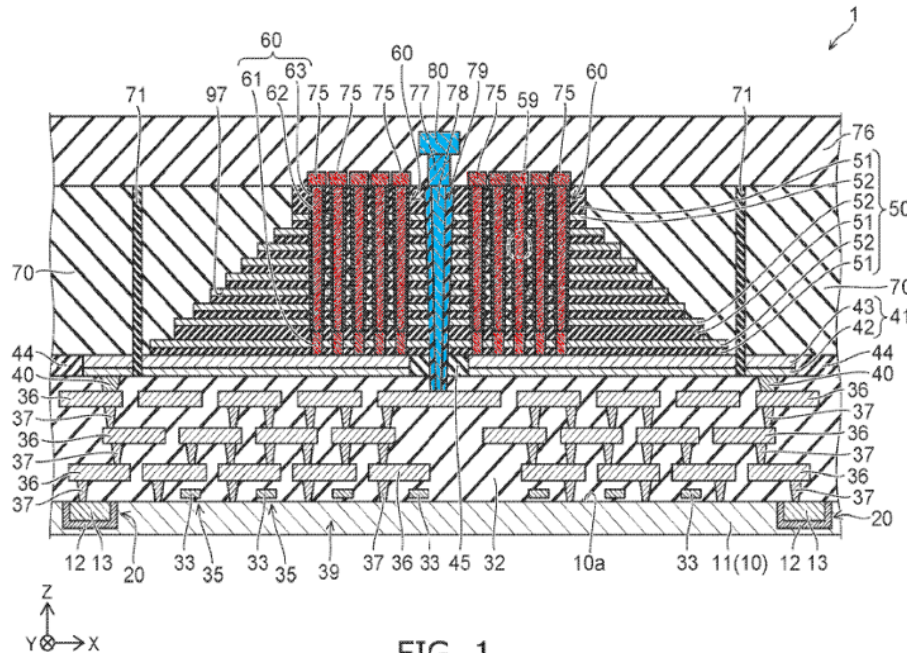


FIG. 1

Dr. Lee does not assert any need for additional support, and does not assert that these pillars are unable to perform this function (which would be contrary to Fujiki's explicit disclosure, as shown in Figure 10). Thus, there is no need for dummy channels, as they would serve no purpose.

33. Dr. Lee further asserts that a dummy channel could "extend through the entire stack or partially through the stack" and, "[f]or example, the dummy channels may be on the edge of the array or in the staircase region." Ex. 1003 ¶ 119. Dr. Lee does not motivate actual dummy channels in any location, but merely asserts that they "may be" on the edge or in the staircase. Fujiki does not disclose dummy channels, however, so this is a hypothetical from Dr. Lee with no motivation. Dr. Lee also omits the fact that these regions are already occupied by structures. Fujiki, Figures 1 and 2. Figure 1, annotated above, shows columnar

portions 60 (red) and through-via 78 (blue) in the array region of the device.

Figure 2, annotated below, shows that the staircase region includes contacts 81 (green), though these are omitted for clarity in Figure 1. Fujiki [0043], [0024].

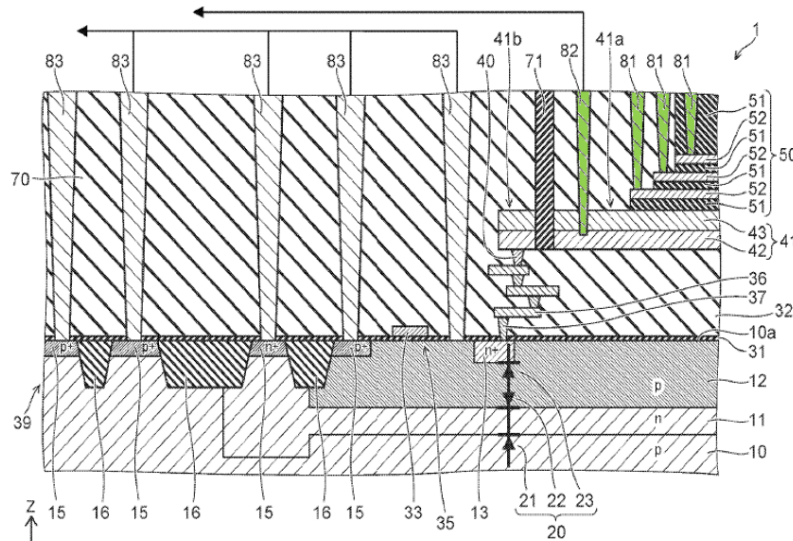


FIG. 2

34. Dr. Lee makes no attempt to account for the fact that these areas are already occupied by structures. He does not assert, for example, that these functional structures would be modified to become dummy structures. This is important because accommodating dummy channels through the stack would require either (1) increasing the size of the stack to create space for the dummy structures while maintaining the existing structures, or (2) decreasing the memory's storage capacity by replacing functional structures (i.e., "columnar portions 60," which serve as channels for the memory cells, Fujiki [0044], or "contacts 81," which provide external access to the word lines, *id.* [0043]) with **non**-functional dummy channels. For example, replacing channels with dummy

structures will significantly decrease the memory's storage capacity because channels are a part of every memory cell. Either approach gives undesirable results, and especially so when no benefit is provided by the dummy structures because the device already has sufficient structural support.

35. And adding dummy channels to Fujiki would require additional processing steps because these new structures would be formed with different structure than others. Notably, Dr. Lee asserts (relative to claim 3) that etching holes at the same time “would significantly reduce processing time” (¶ 129). But he does not address that making some structures as dummy channels would require a separate process to deposit the different materials needed to form dummy channels rather than functional pillars.

36. The Petition cites to three references—Kai, Kim, and Park—that purportedly confirm “the knowledge of a POSITA.” Petition at 44-45. None of these references motivate adding dummy channels to Fujiki, where existing, functional structures provide adequate structural support. Instead, all three references disclose, at most, devices with specific “regions” (that Fujiki lacks) to accommodate what Dr. Lee describes as “dummy channels.” Ex. 1003 ¶ 120.

37. For example, the Kai reference (Exhibit 1015) discloses “support pillars 20” (blue) in a “contact region 300” (yellow) that is “between the memory

array region 100 and the peripheral device region 200.” Kai, 6:2-5, Fig. 6A; *see also* Fig. 15A (showing “support pillars 20” only in the contact region).

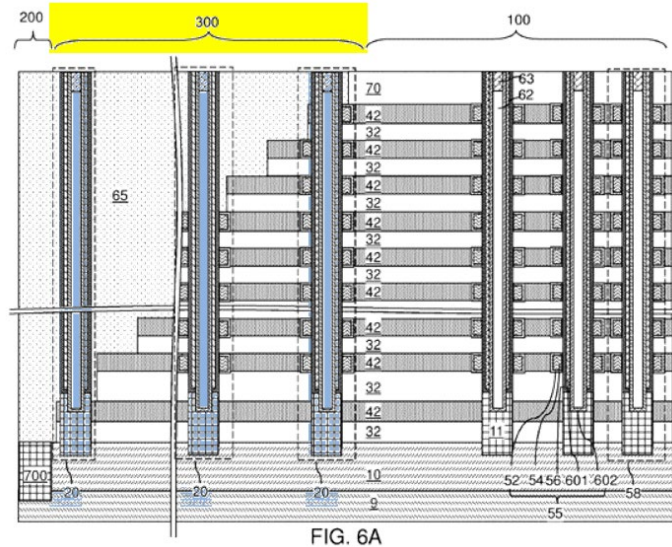
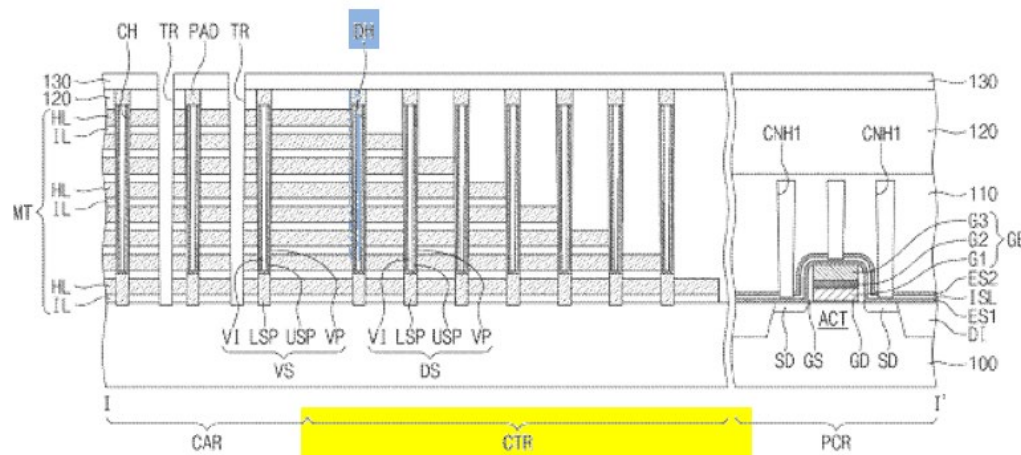


FIG. 6A

38. Similarly, the Kim reference (Exhibit 1017) discloses “dummy holes DH” (blue) in a “connection region CTR” (yellow). Kim, Figure 13 (below), [0047]; *see* Petition at 44 (citing Kim [0047]) (“The stack structure ST may be penetrated with a plurality of dummy holes DH on the connection region STR”); *see also* Kim [0070] (“On the connection region CTR, a plurality of dummy holes DH may be formed.”).

FIG. 13



39. For its part, Park (Exhibit 1016), discloses separate “cell and dummy regions.” Park, Abstract. Park discloses “second channel structure 120b” that are “disposed on the wiring region” and “may not be provided as the portion of the memory cell.” *Id.*, 7:38-44.

40. To summarize, Kai, Kim, or Park, teach forming dummy channels in regions designed to accommodate dummy channels. These separate areas include a “contact region” (Kai), “connector region CTR” (Kim), or “dummy regions” (Park). The Petition does not explain how, where, or why a POSITA would have formed such regions in Fujiki. None of Kai, Kim, or Park would have motivated a POSITA to add dummy channels to Fujiki, which already has functional structures that provide the structural support that the Petition asserts is provided by the dummy structures, and modifying structures within the memory cell array

would require (1) additional processes to form the different pillar structure and (2) either removing functional pillars from the device or increasing the size of the device to accommodate additional structures.

41. The Petition asserts other supposed benefits to forming dummy channels in Fujiki. For example, the Petition states that dummy channels are suitable to use as support structures because they “can be made by the same process and at the same time as the active channels,” they “do not require connections to upper-level devices,” they provide “additional structural support,” and improve “uniform[ity].” Pet. 45-46. But these supposed benefits all pre-suppose that there is a need for additional support structures in Fujiki. For example, the fact that dummy structures do not require connections to upper-level devices means they are not functional within the device, and take up extra space where a functional pillar would be placed as Fujiki illustrates. Further, the supposed “uniformity” only seems to be provided pre-assuming a need for dummy structures in the first place, and specifically on when they are evenly spaced throughout the device, resulting in potentially enormous spatial expansion of Fujiki’s device. I disagree that these supposed benefits would have motivated a POSITA to make the proposed modification to Fujiki, which has no need for additional structural support.

42. The Petition also asserts that “adding dummy structures would result in reducing the likelihood of defective bits on the edge of the memory cell region, because the inclusion of the additional rows extends the memory cell pattern for those respective columns into the dummy region.” Petition at 45. It is not clear what the Petition means by “inclusion of the additional rows” in this sentence. Further, Fujiki does not include a dummy region. Nevertheless, this does not motivate adding dummy structures to Fujiki, for similar reasons that Kai, Kim, and Park don’t. Additionally, to the extent Dr. Lee discusses employing dummy channels “at the edge of the array” to provide support to mitigate against abnormalities, I disagree. *See* Ex. 1003 ¶ 117. Specifically, Dr. Lee does not show that this is a concern in Fujiki, which has a peripheral-under-channel (PUC) design (rather than having the peripheral circuitry adjacent to the channel), which results in a lower footprint in the x direction and has sufficient support structure as illustrated in Fujiki.

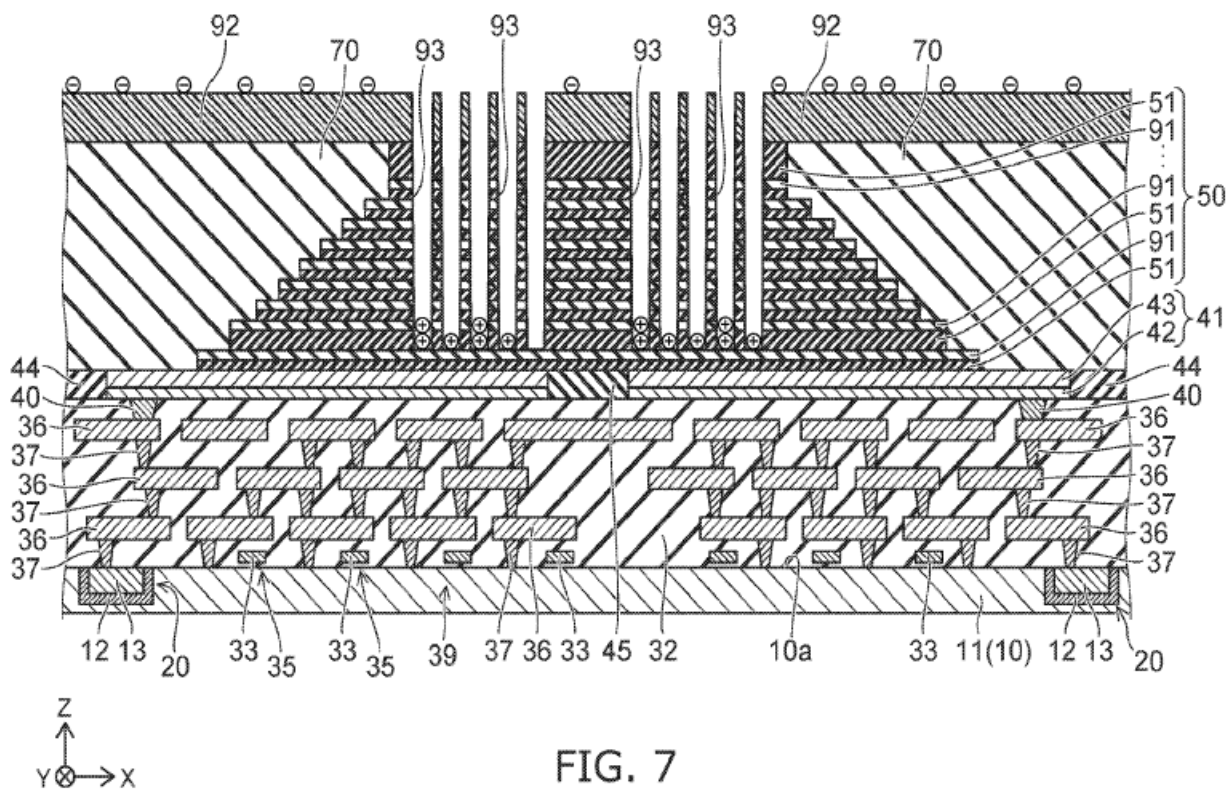
43. Although I focused on claim 2 above, these opinions also apply to claim 11 for the same reasons as claim 2, because claim 11 similarly recites “forming a dummy channel structure extending vertically through the stack.” Claims 12-15 and 17 depend from claim 11.

46. I disagree. Nothing in Fujiki suggests forming contacts 82, 83 at the same time as through-via. As Dr. Lee acknowledges, Fujiki describes the formation of through-via 78. Ex. 1003 ¶ 126 [0050]. There is no suggestion that this description applies to any other opening. For example, Fujiki does not describe contacts 82, 83 as “through-vias” and in fact they are not through-vias. And although Dr. Lee asserts that “conventional 3D NAND configuration with TACs includes multiple TACs” (Ex. 1003 ¶ 126),¹ that does not suggest (and Dr. Lee does not contend) that the contacts 82, 83 are through-vias or that they would be etched simultaneously as through-via holes. Nor does it suggest the existence of some undisclosed through-vias located outside the stack.

47. The Petition asserts that “Fujiki would (or could) simply etch all contact holes for Fujiki’s TAC and contacts 82 or 83 at once, just as Fujiki does with its channel holes.” Pet. 47 (citing Ex. 1003 ¶¶ 124-126). Dr. Lee does not

¹ Dr. Lee cites Nakajima, Figures 1-2 as showing multiple TACs. I previously submitted a declaration in IPR2025-00034 relating to a ground based on Nakajima against the '254 patent. There I showed that Nakajima only discloses forming holes for the C4 pillars through the stack and does not teach or suggest simultaneous etching of such holes through and outside the stack. Nakajima, 7:37-43. IPR2025-00034, Exhibit 2007, ¶¶ 46-48.

provide any support for the notion that Fujiki's formation of channel holes provides any motivation or expectation of success in forming through-vias and contacts 82-83 at the same time. *See* Ex. 1003 ¶¶ 124-126. And in fact, Fujiki's channel holes don't motivate the Petition's modification of Fujiki. Specifically, Fujiki's memory holes 93 (which the Petition refers to as "channel holes") are all formed through the stack as shown in Figure 7, below.



48. Additionally, the Fujiki discloses that the etching process used to form memory holes 93 is a "reactive ion etching process" where ions "collide selectively with the stacked body 50." Fujiki [0051]. In other words, this process is specifically used to etch holes through the stack. By being "selective" to the

stacked body, a POSITA would not expect the same process to be able to be used to etch openings outside of the stacked body because such selectivity deliberately avoids etching other materials outside the stack.

49. Fujiki does not even disclose the through-via hole 94 being formed simultaneously to these memory holes 93, even though they would both be etched through the stack. *See* Fujiki [0053]. The Petition's assertion that a POSITA would simply form all the holes simultaneously is baseless and contradicted by Fujiki itself.

50. I also note that the claimed simultaneous etching is not unusually simple, and involves complex semiconductor manufacturing processes, including DRIE (deep reactive ion etching). '254 patent, 12:24-45. And 3D NAND technology is not a particularly straightforward technology. Rather, it involves the intersection of chemistry, physics, and engineering at the smallest of scales. As Petitioner's Exhibit 1008 describes:

It would be shortsighted to dismiss 3D semiconductor processing as just an incremental step in the progression of micro/nano-electronic fabrication. This new dimension multiplies the number of elements that can be created with the same number of photolithographic steps. As experience in manufacturing is gained, this multiplier grows from dozens, to hundreds, and possibly beyond. Fabricating devices in the third dimension provides a new degree of freedom for creativity in designs, architectures, and layouts. It offers challenges to create

breakthroughs in testing, integration, power density, heat dissipation, and systems-on-chip.

Ex. 1008 at 7.

51. Dr. Lee cites Tessariol (Exhibit 1023) as teaching simultaneous etching of openings, it's clear from the passage Dr. Lee cites that both sets of openings are formed *through* the stack unlike the claimed first and second openings of claim 3. Ex. 1003 ¶ 129 (citing Tessariol [0037] and Figure 9). Dr. Lee does not assert otherwise.

52. Dr. Lee asserts that Mushiga (Exhibit 1010) demonstrates that “forming holes for through-array contacts...at the same time in various portions of the memory device was routine and well understood.” Ex. 1003 ¶ 130 (citing Mushiga Fig. 5, 10:31-58). But Mushiga never describes the cavities for these contacts as being formed simultaneously through and outside of the stack. *See* Mushiga 10:31-58. The most Mushiga discloses about the topic of timing is that the “cavities can be formed before or after formation of the electrically conductive layers (146, 246).” Mushiga 10:49-57. But this does not require or suggest forming the cavities at the same time through the different materials that the two cavities penetrate. *See* Mushiga, Fig. 5, 10:31-38. Nor does it provide any motivation to a POSITA to (1) form Fujiki's *contacts* (not through-vias) 82-83

simultaneous to its through-via 94, or (2) modify Fujiki's explicit disclosure of forming its through-via hole 94 through the stack.

53. Dr. Lee further asserts that Masamori (Ex. 1019) “discloses forming holes for multiple contacts... at the same time.” Ex. 1003 ¶ 131. He first cites contacts 82, 84, and 86, and he annotates Figure 13A of Masamori to highlight these three contacts. Ex. 1003 ¶¶ 131-132. As the figure shows, however, none of these contacts are formed in holes etched through the stack.

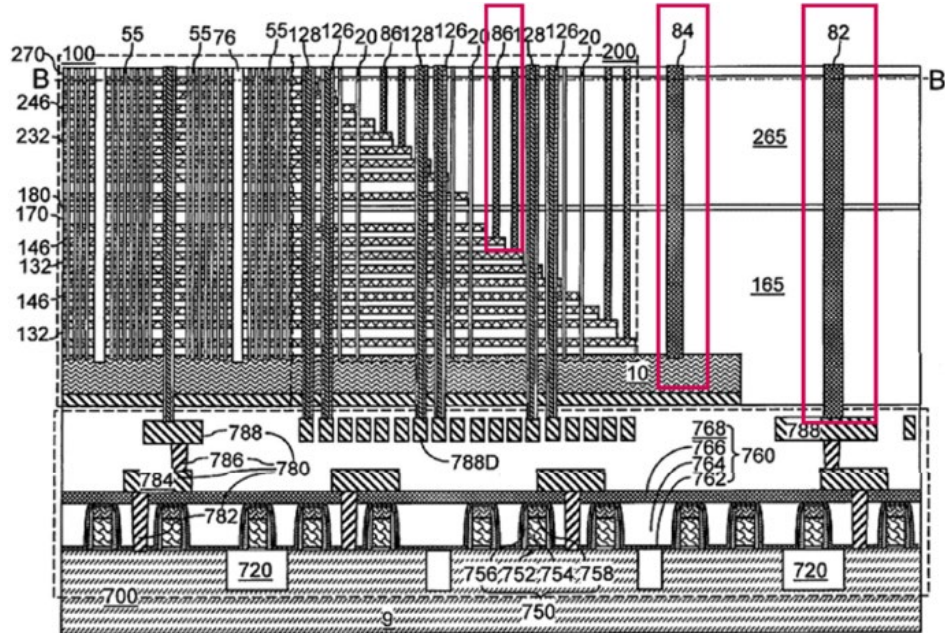


FIG. 13A

He also annotates Figure 8A to highlight structures (26, 28) and (126, 128), and quotes Masamori as teaching that these structures can be “formed concurrently.” Ex. 1003 ¶ 132. However, as shown below, these structures are all formed in holes etched through the stack. Dr. Lee does not assert, and Masamori does not teach, that these holes are formed concurrently without any holes outside the

stack. Thus, Masamori teaches simultaneous etching of holes through the stack, but not simultaneous etching of holes *both* through and outside the stack.

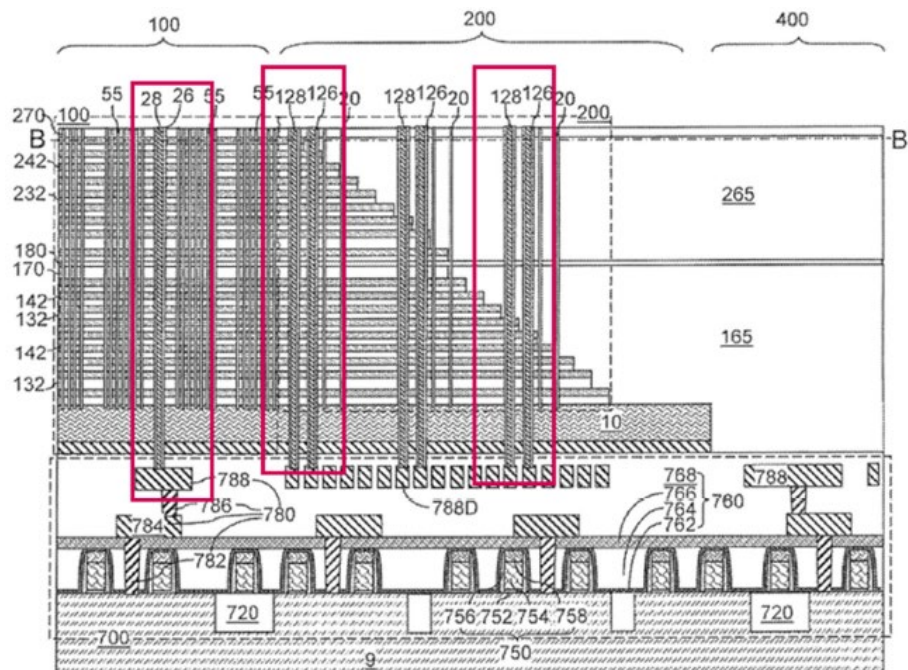


FIG. 8A

54. Finally, Dr. Lee cites to Kai II (Ex. 1038) as “forming openings for various contacts and memory structure openings in a single step.” Ex. 1003

¶ 133. Dr. Lee annotates Figure 4A of Kai II, below, as purportedly showing these openings. *Id.*

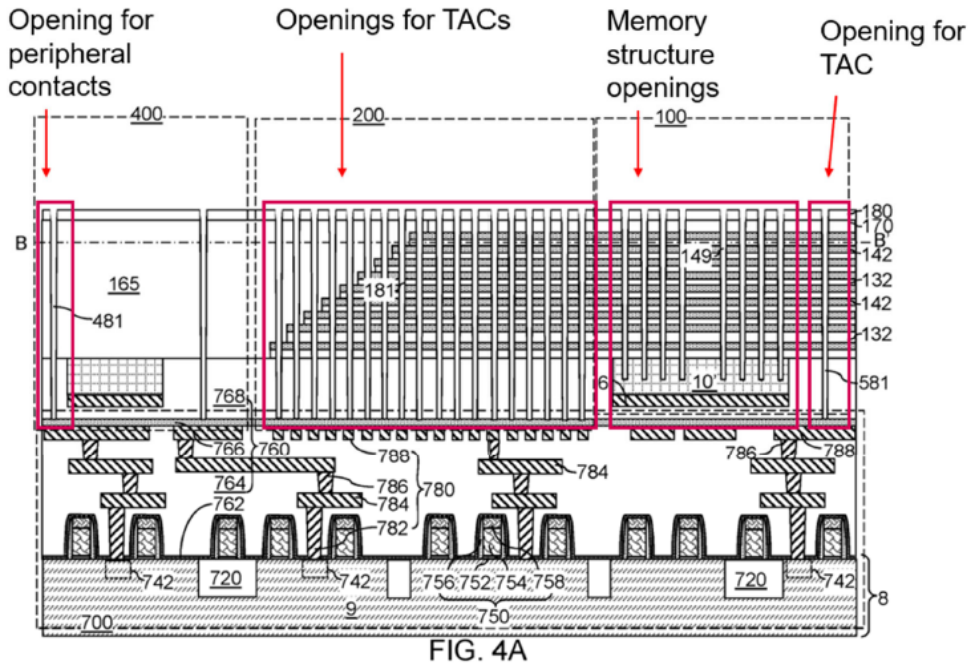
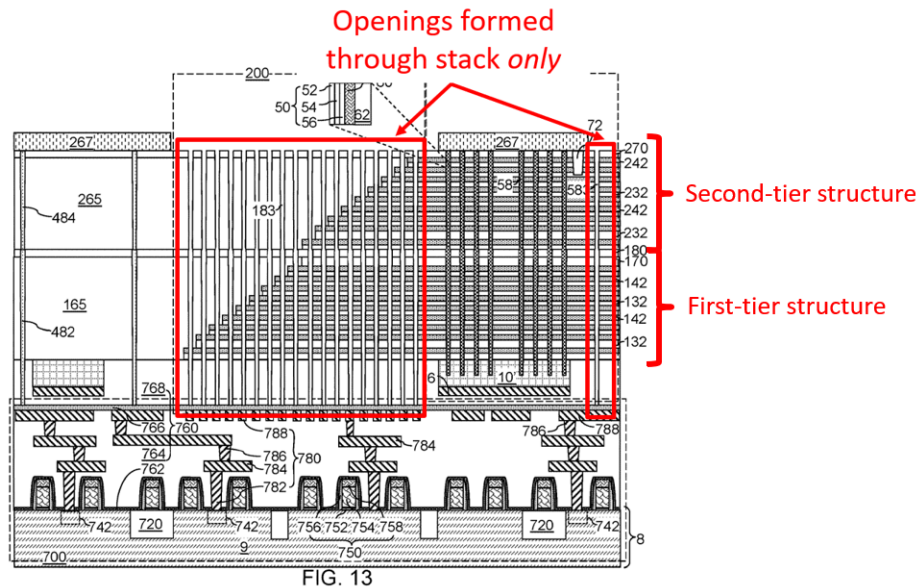


FIG. 4A

55. Dr. Lee does not assert that Kai II discloses the claim 3 limitation and does not propose combining Kai II with Fujiki. And Dr. Lee omits that Figure 4A is an intermediate step and forms openings in an intermediate structure (i.e., the “first-tier structure”) of Kai II. In subsequent steps, these holes are filled, a second-tier structure is added, and then, in Figure 13, annotated below, new holes are etched *separately* for structures in the stack and outside the stack.



56. Dr. Lee also does not address how Kai II’s disclosure of forming openings during the same process requires that the openings are all formed “simultaneously.” Kai II explicitly discloses that etch process may be performed “iteratively” or comprise “a series of reactive ion etch processes.” Kai II 16:42-49; 23:18-26.

57. Although the above discussion focused on claim 3, it also applies to claims 4, 9-10, 18, and 20. Specifically, claim 9 similarly recites “simultaneously etching the first opening through the stack, a second opening outside of the stack, and a third opening through the stack.” Claim 10 depends from claim 9. Claim 18 also recites “simultaneously etching a first opening through the stack, a second opening outside of the stack, and a third opening through the stack.” Claim 20 depends from claim 18; claim 4 depends from claim 3; and claim 10 depends from claim 9.

C. Claims 7-8, 14-15 (“forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening”)

58. Claim 7 recites “forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening.” Notably, “the first opening” in claim 7 is the opening through which the “through array contact (TAC)” is formed in independent claim 1.

59. Dr. Lee discusses claim 7 under two interpretations: first, an interpretation that “include[s] largely undetectable and unintentional alleged recesses” (Ex. 1003 ¶¶ 164-165); and second, an interpretation that requires “[c]reating intentional lateral recesses.” Ex. 1003 ¶ 166. In my opinion, neither interpretation is rendered obvious based on Fujiki.

60. First, Dr. Lee cites Exhibit 1030 for support that “typical prior art etches that effectively create a hole through th[e] stack result in very small lateral recesses in either the dielectric spacers or sacrificial layers.” Ex. 1003 ¶ 165. The cited passage of 1030 says no such thing. Rather, the passage describes “a lack of etching a plurality of alternating layers of SiO and SiN layers in a 3D NAND application using a nontraditional hydrofluorocarbon etching gas.” Ex. 1030 2:56-58. “Although there are numbers of prior arts for SiO₂ etching with high selectivity to SiN, for certain applications, it is important to have an etching gas which can etch both SiO₂ and SiN layers...without selectivity.” Ex. 1030 2:59-

63. “In another word, it is a challenge to find an etch gas that has similar high etch rates of SiO₂ and SiN in terms of getting a smooth sidewall of high aspect ratio holes in 3D NAND memory.” Ex. 1030 2:63-67. This passage describes that it is important to have an etching gas without selectivity (which etches the layers evenly) and the patent itself purports to provide a solution. As Exhibit 1030 further explains, its proposed solution mitigates against sidewall bowing or barreling as depicted in Figure 1d, below. Ex. 1030 18:38-63. Exhibit 1030 further describes bowing as undesirable, and does not motivate or inform a POSITA that such a pattern would be formed in Fujiki. Ex. 1030 18:42-44. Nor does it suggest forming a plurality of shallow recesses.

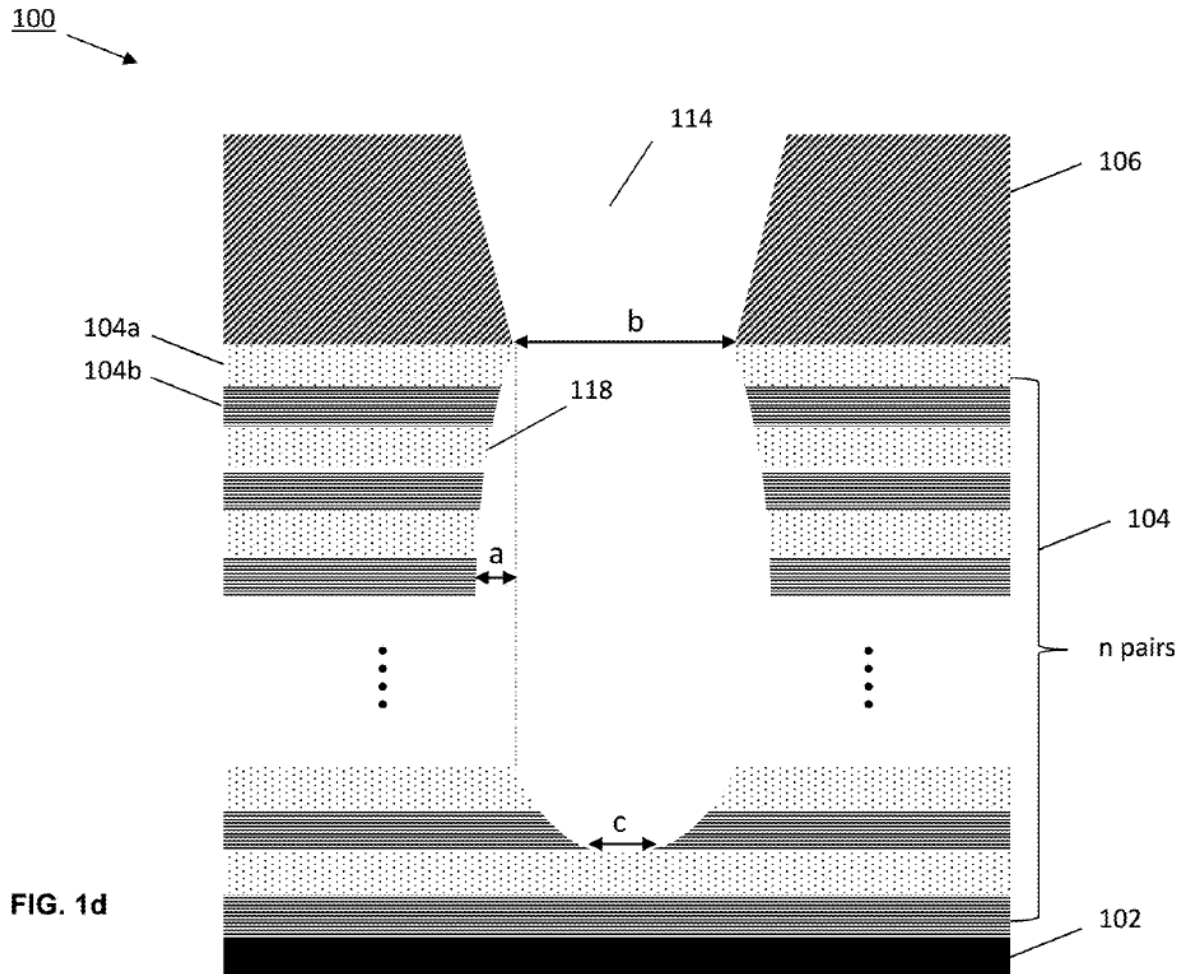


FIG. 1d

Ex. 1030 Fig. 1d

61. Second, with respect to what Dr. Lee asserts to be the “correct” claim interpretation, Dr. Lee asserts that intentional lateral recesses in a hole “for a contact” was also known. Ex. 1003 ¶¶ 166-169. For support, Dr. Lee relies on Cui (Ex. 1031) and Kai (Ex. 1015). However, neither Cui nor Kai disclose or suggest forming shallow recesses by removing parts of the *sacrificial layers* abutting the sidewall of an opening for a “through array contact (TAC)” as

required by claim 7. And doing so is not unusually simple or particularly straightforward. Forming recesses in sacrificial layers is highly technical and complex, and requires, among other things, that “the lateral dimension of shallow recess” be “controlled by the etching rate and/or etching time.” ’254 patent, 13:48-61.

62. Cui, for example, discloses forming ribbed cavities by removing portions of *insulating* layers, leaving the sacrificial layers intact. Cui 26:23-25 (“[A]n isotropic etch process can be performed to laterally recess the *insulating layers* (132, 232) with respect to the spacer material layers such as the first and second sacrificial material layers (142, 242).”). The claims, however, require forming the “shallow recesses” by “removing parts of the *sacrificial layers*”—not “insulating layers.” In fact, as shown by Figure 16A (reproduced below), Cui’s etching deliberately does *not* form recesses in the sacrificial layers 142 as required by the claims of the ’254 patent. *Id.*; *see also* Cui Fig. 16A.

VII. CONCLUSION

All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under penalty of perjury that the foregoing is true and correct.

Executed on March 11, 2025, in Arden Hills, Minnesota.

Stephen Campbell
Stephen Campbell