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(54) **PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS**

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(60) Provisional application No. 61/614,275, filed on Mar. 22, 2012.

(51) **Int. Cl.**
H01L 27/146 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 27/1463*** (2013.01); ***H01L 27/1462*** (2013.01); ***H01L 27/14607*** (2013.01); ***H01L 27/14625*** (2013.01); ***H01L 27/14627*** (2013.01); ***H01L 27/14629*** (2013.01); ***H01L 27/14645*** (2013.01); ***H01L 27/14685*** (2013.01); ***H01L 27/14689*** (2013.01)

(58) **Field of Classification Search**
None
See application file for complete search history.

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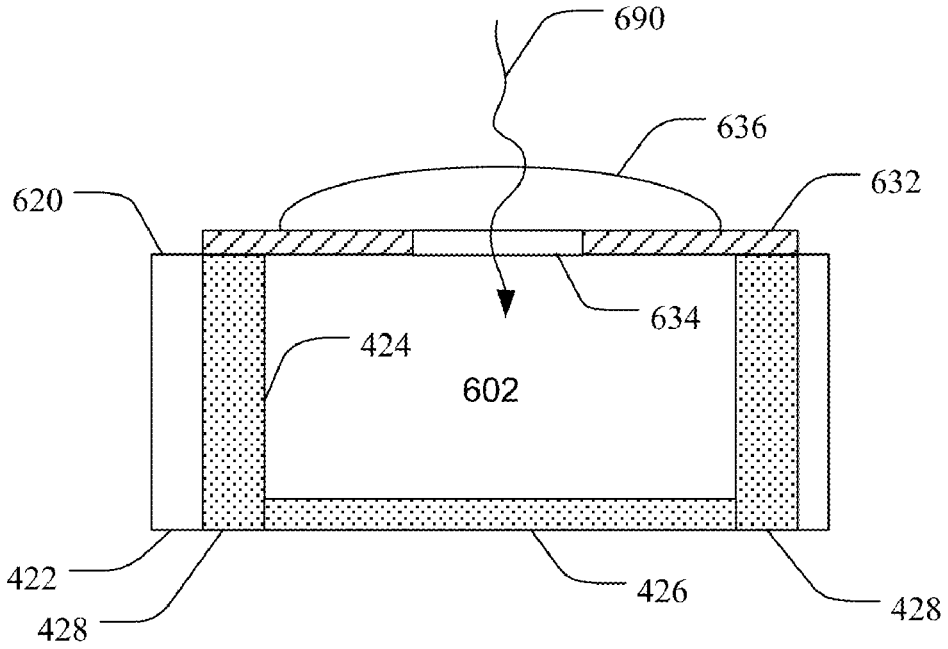
(57) **ABSTRACT**

Light trapping pixels, devices incorporating such pixels, and various associated methods are provided. In one aspect, for example, a light trapping pixel device can include a light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery. The pixel can also include a backside light trapping material substantially covering the backside surface and a peripheral light trapping material substantially covering the peripheral sidewall. The light contacting the backside light trapping material or the peripheral light trapping material is thus reflected back toward the pixel.

18 Claims, 4 Drawing Sheets



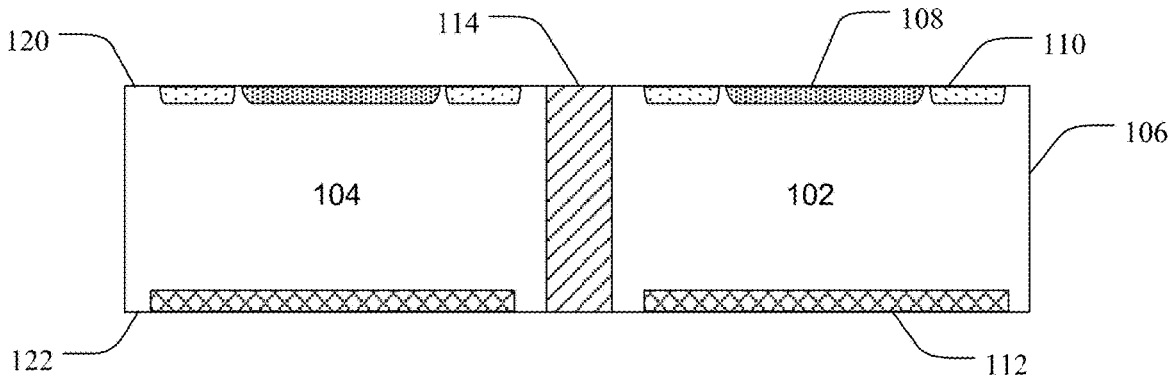

120
114
108
110
106
104
102
122
112

FIG. 1

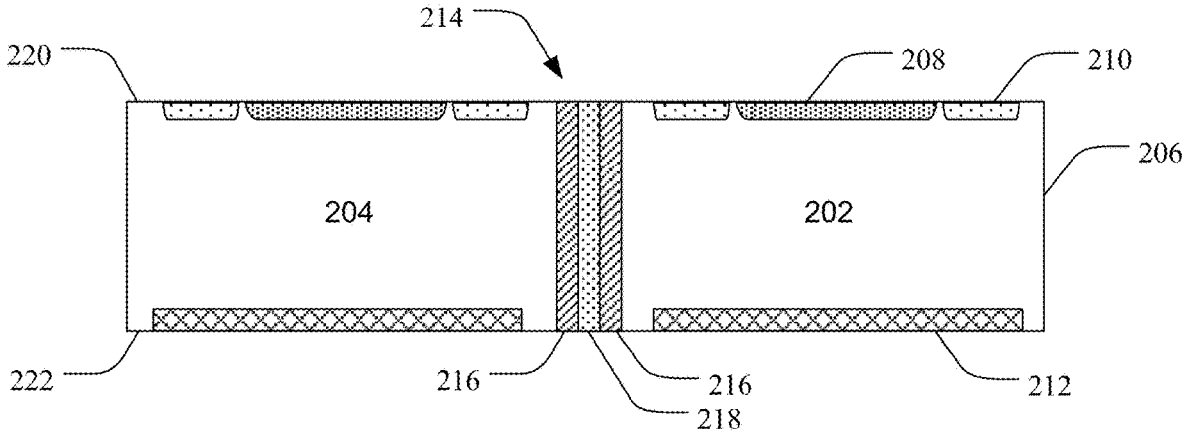

214
220
208
210
206
204
202
222
216
216
218
212

FIG. 2

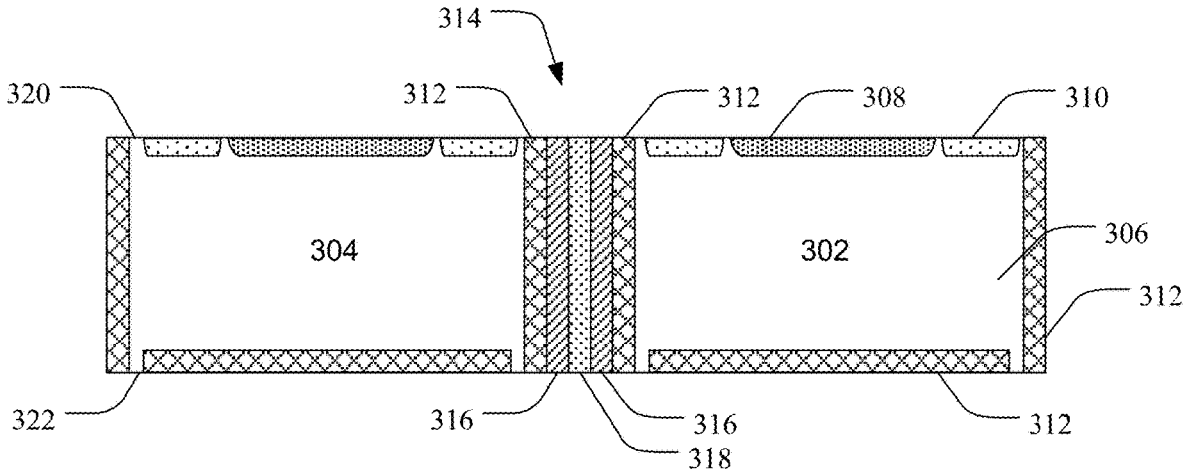


FIG. 3

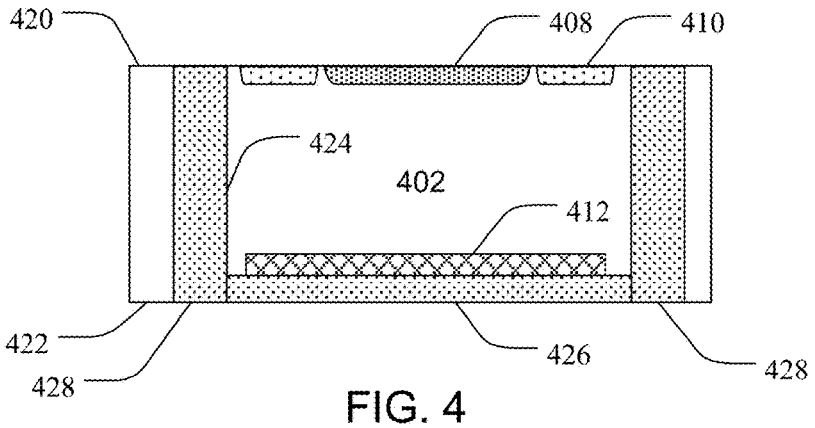


FIG. 4

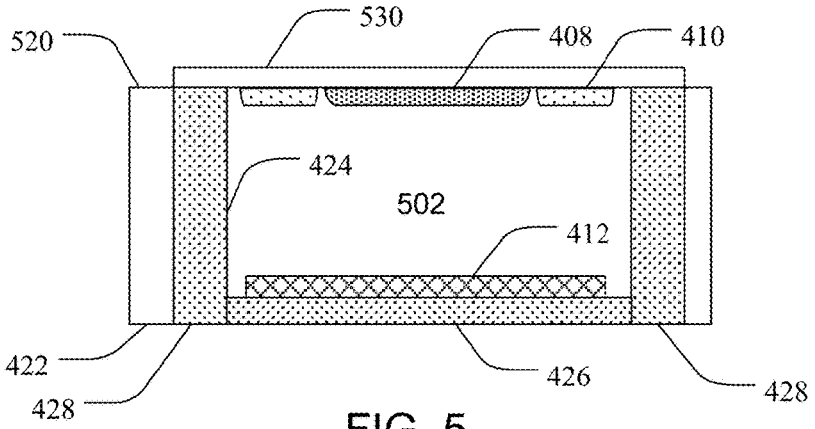


FIG. 5

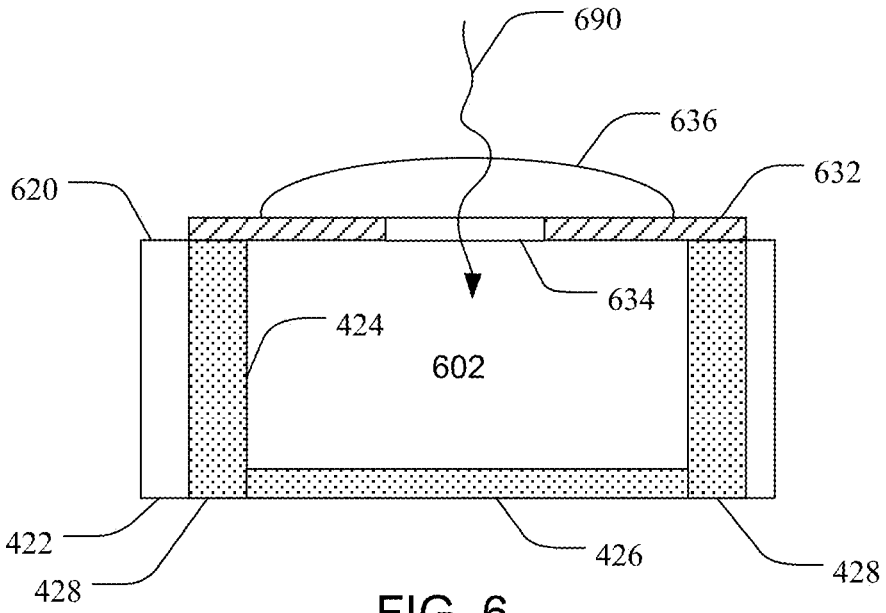


FIG. 6

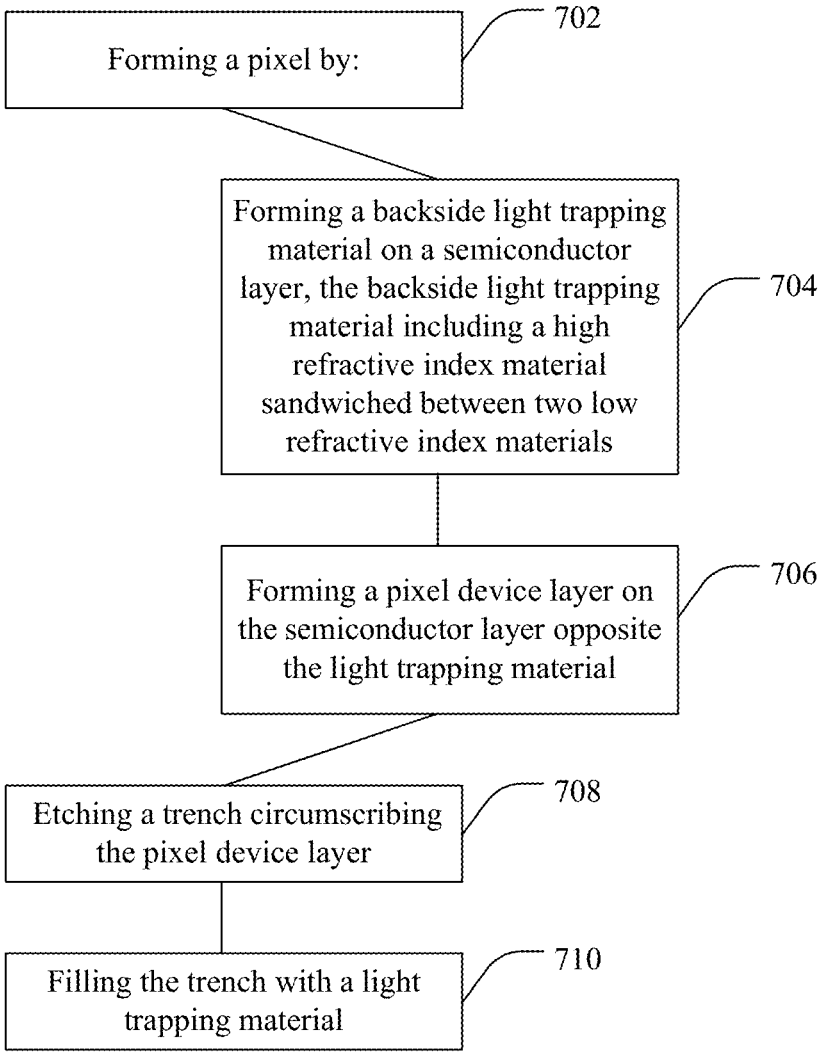

Forming a pixel by:
702
Forming a backside light trapping material on a semiconductor layer, the backside light trapping material including a high refractive index material sandwiched between two low refractive index materials
704
Forming a pixel device layer on the semiconductor layer opposite the light trapping material
706
Etching a trench circumscribing the pixel device layer
708
Filling the trench with a light trapping material
710

FIG. 7

PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS

PRIORITY DATA

This application is a continuation of U.S. patent application Ser. No. 16/290,740, filed Mar. 1, 2019, which is a continuation of U.S. patent application Ser. No. 15/216,244, filed Jul. 21, 2016, which is a continuation of U.S. patent application Ser. No. 14/747,875, filed Jun. 23, 2015, which is a continuation of U.S. patent application Ser. No. 13/841,120, filed Mar. 15, 2013, which claims the benefit of U.S. Provisional Patent Application No. 61/614,275, filed on Mar. 22, 2012, each of which are incorporated herein by reference.

BACKGROUND

Image sensors are typically formed on various forms of semiconductor materials such as, for example, silicon. Imagers can be incorporated into a variety of devices, including digital cameras, camcorders, computers, cell phones, etc. Due to the ever decreasing size (foot print) of these devices, image sensors have correspondingly seen a decrease in size. Backside illuminated (BSI) image sensors have increased in importance due to the small size of these imagers as compared to front side illuminated (FSI) image sensors. However, pixel size reduction can lead to a significant sacrifice in image quality. As pixel sizes continue to decrease, image signal to noise tends to decrease while electrical and optical cross-talk between adjacent sensor pixels tends to increase. Traditional attempts to reduce the impact of these effects have included adding microlenses above each image sensor in front side pixel sensors to focus the light on the active detector regions, thereby increasing efficiency and reducing cross-talk. Backside illuminated pixel sensors can present different design considerations. For example, significant cross-talk can be generated due to reflection off the often planar back surface of the device.

SUMMARY

The present disclosure provides for light trapping pixels, devices incorporating such pixels, photovoltaic solar cells, and other optoelectronic devices, including various associated methods. In one aspect, for example, a light trapping device can include at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery. The pixel can also include a backside light trapping material substantially covering the backside surface and a peripheral light trapping material substantially covering the peripheral sidewall. The light contacting the backside light trapping material or the peripheral light trapping material is thus reflected back toward the pixel. In another aspect, the present disclosure additionally provides an array of light trapping pixels.

A variety of light trapping materials can be utilized and are contemplated, and any such material capable of being used to trap light in a pixel is considered to be within the present scope. In one aspect, at least one of the backside light trapping material and the peripheral light trapping material can include a high refractive index material sandwiched between two low refractive index materials. In another aspect, the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials. It is contemplated that the two low refractive index materials have a refractive index of less than about 2.1. Non-limiting examples of low refractive index material can include nitrides, oxynitrides, gasses, at least a partial vacuum, and the like, including appropriate combinations thereof. Other non-limiting examples of low refractive index materials can include silicon oxide, silicon nitride, silicon dioxide, and the like. Furthermore, in another aspect a light trapping material can include a higher refractive index material sandwiched between two materials having a refractive index that is at least 0.2 lower as compared to the higher refractive index material. In this case, the materials are not limited by the definition of low vs. high refractive index outlined above, but are rather defined by the relative difference in refractive index.

Furthermore, it is contemplated that high refractive index materials have a refractive index of greater than or equal to about 2.1. Non-limiting examples of high refractive index material can include polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and the like, including appropriate combinations thereof.

In one aspect, the peripheral sidewall can extend completely around the pixel periphery. In another aspect, the peripheral sidewall can extend from the light incident surface towards the backside surface.

In some aspects it is also contemplated that the light incident surface can include a frontside light trapping material at least partially covering the surface thereof. In one aspect, the frontside light trapping material can be an antireflective layer coating. In another aspect, the frontside light trapping material can be a reflective layer having an aperture to allow entry of light into the pixel, wherein the reflective layer is operable to reflect light impinging thereupon from inside the pixel back into the pixel. In some aspects it can be beneficial to include a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.

In another aspect the present disclosure additionally provides a substantially light trapping pixel device including a light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending from the light incident surface to the backside surface and extending around the pixel periphery. The pixel additionally includes a backside light trapping material substantially covering the backside surface, and a peripheral light trapping material substantially covering the peripheral sidewall. Furthermore, an internally reflective frontside light trapping material can cover at least a portion of the light incident surface that is operable to allow entrance of light into the pixel and is operable to reflect light impinging thereupon from inside the pixel back into the pixel, and the light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

In yet another aspect, the present disclosure provides a method of making a light trapping device, including forming at least one pixel by forming a backside light trapping material on a semiconductor layer, the backside light trapping material including a high refractive index material sandwiched between two low refractive index materials, and forming a pixel device layer on the semiconductor layer opposite the light trapping material. The method can additionally include etching a trench circumscribing the pixel device layer and filling the trench with a light trapping material. In some aspects, the trench can be etched to a depth

that contacts at least the first low refractive index material. In some aspects, an incident light trapping material can be applied to the pixel device layer. It is also noted that the light trapping material can be located anywhere in the backside region of the device, and that the current scope is not limited to the location of materials or the manufacturing method described above.

In another aspect, filling the trench with the light trapping material can further include depositing a low refractive index material into the trench to fill a portion of the trench from the trench walls inward, ceasing deposition of the low refractive index material to leave an internal space within the trench, and depositing a high refractive index material into the trench to fill the internal space.

In another aspect, the method can include forming a textured region on at least a portion of the semiconductor layer between the semiconductor layer and the first low refractive index prior to depositing the first low refractive index material onto the semiconductor layer. Non-limiting examples of techniques for forming the textured region include plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, the like, including appropriate combinations thereof. In one specific aspect, forming the textured region includes laser texturing.

BRIEF DESCRIPTION OF THE DRAWINGS

For a further understanding of the nature and advantage of the present disclosure, reference is being made to the following detailed description of embodiments and in connection with the accompanying drawings, in which:

FIG. **1** is a cross-sectional view of multiple image sensor pixels in accordance with an embodiment of the present disclosure;

FIG. **2** is a cross-sectional view of multiple image sensor pixels in accordance with another embodiment of the present disclosure;

FIG. **3** is a cross-sectional view of multiple image sensor pixels in accordance with another embodiment of the present disclosure;

FIG. **4** is a cross-sectional view of a light trapping pixel in accordance with another embodiment of the present disclosure;

FIG. **5** is a cross-sectional view of a light trapping pixel in accordance with another embodiment of the present disclosure;

FIG. **6** is a cross-sectional view of a light trapping pixel in accordance with another embodiment of the present disclosure; and

FIG. **7** is a depiction of a method of making a light trapping pixel in accordance with yet another aspect of the present disclosure.

DETAILED DESCRIPTION

Before the present disclosure is described herein, it is to be understood that this disclosure is not limited to the particular structures, process steps, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting.

Definitions

The following terminology will be used in accordance with the definitions set forth below.

It should be noted that, as used in this specification and the appended claims, the singular forms "a," and, "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a dopant" includes one or more of such dopants and reference to "the layer" includes reference to one or more of such layers.

As used herein, the terms "light" and "electromagnetic radiation" can be used interchangeably and can refer to electromagnetic radiation in the ultraviolet, visible, near infrared and infrared spectra. The terms can further more broadly include electromagnetic radiation such as radio waves, microwaves, x-rays, and gamma rays. Thus, the term "light" is not limited to electromagnetic radiation in the visible spectrum. Many examples of light described herein refer specifically to electromagnetic radiation in the visible and infrared (and/or near infrared) spectra. For purposes of this disclosure, visible range wavelengths are considered to be from approximately 350 nm to 800 nm and non-visible wavelengths are considered to be longer than about 800 nm or shorter than about 350 nm. Furthermore, the infrared spectrum is considered to include a near infrared portion of the spectrum including wavelengths of approximately 800 to 1100 nm, a short wave infrared portion of the spectrum including wavelengths of approximately 1100 nm to 3 micrometers, and a mid-to-long wavelength infrared (or thermal infrared) portion of the spectrum including wavelengths greater than about 3 micrometers up to about 30 micrometers. These are generally and collectively referred to herein as "infrared" portions of the electromagnetic spectrum unless otherwise noted.

As used herein, "quantum efficiency" (QE) is typically referring to "external quantum efficiency" (EQE) which is defined as the ratio of electrons collected per photons incident on an optoelectronic device. "Internal quantum efficiency" is defined as the ratio of electrons collected per photons absorbed by an optoelectronic device.

As used herein, the terms "3D" and "three dimensional" can be used interchangeably, and refer to obtaining distance information using electromagnetic radiation.

As used herein, the terms "disordered surface" and "textured surface" can be used interchangeably, and refer to a surface having a topology with nano- to micron-sized surface variations. Such a surface topology can be formed by the irradiation of a laser pulse or laser pulses, chemical etching, wet or dry etching including masked or maskless etching, lithographic patterning, interference of multiple simultaneous laser pulses, reactive ion etching, plasma etching or any other technique that can be used to form such a topology. While the characteristics of such a surface can be variable depending on the materials and techniques employed, in one aspect such a surface can be several hundred nanometers thick and made up of nanocrystallites (e.g. from about 10 to about 50 nanometers), nanopores, and the like. In another aspect, such a surface can include micron-sized structures (e.g. about 1 μm to about 60 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 500 μm. A variety of criteria can be utilized to measure the size of such structures. For example, for cone-like structures the above ranges are intended to be measured from the peak of a structure to the valley formed between that structure and an adjacent neighboring structure. For structures such as nanopores, the above ranges are intended to be approximate diameters. Additionally, the surface structures can be spaced at various average distances from one another. In one aspect, neighboring structures can be spaced at a distance of from about 50 nm to about 50 μm. In another aspect, neighboring

structures can be spaced at a distance of from about 50 nm to about 2 μm. Such spacing is intended to be from a center point of one structure to the center point of a neighboring structure.

As used herein, the term "fluence" refers to the amount of energy from a single pulse of laser radiation that passes through a unit area. In other words, "fluence" can be described as the energy density of one laser pulse.

As used herein, the term "target region" refers to an area of a semiconductor material that is intended to be doped or surface modified. The target region of a semiconductor material can vary as the surface modifying process progresses. For example, after a first target region is doped or surface modified, a second target region may be selected on the same semiconductor material.

As used herein, the term "absorptance" refers to the fraction of incident electromagnetic radiation absorbed by a material or device.

As used herein, the term "monolithic" refers to an electronic device in which electronic components are formed on the same substrate. For example, two monolithic pixel elements are pixel elements that are formed on the same semiconductor substrate.

As used herein, the term "substantially" refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is "substantially" enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use of "substantially" is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is "substantially free of" particles would either completely lack particles, or so nearly completely lack particles that the effect would be the same as if it completely lacked particles. In other words, a composition that is "substantially free of" an ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

As used herein, the term "about" is used to provide flexibility to a numerical range endpoint by providing that a given value may be "a little above" or "a little below" the endpoint.

As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of "about 1 to about 5" should be interpreted to include not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

THE DISCLOSURE

The present disclosure provides semiconductor devices and associated methods that can exhibit various enhanced properties, such as, for example, enhanced light detection properties. More specifically, in one aspect the disclosure relates to image sensor pixels and elements for trapping light within such pixels. In other aspects, various light trapping elements can additionally isolate neighboring pixels in an image sensor. Isolation elements can be configured to optically and/or electrically isolate neighboring pixels from one another in addition to trapping light with in the pixel. It is additionally contemplated that the present disclosure is applicable to other optoelectronic devices such as solar cells, and that all such should be included in the present scope.

In various aspects, image sensors can be front side or backside illuminated, 3D sensors, or any other device or system that incorporate a unique isolation element configured to reduce cross-talk between pixel elements. For example, in one aspect an image sensor can be capable of detecting visible and infrared light, whereas an isolation element associated with such an imager can be designed and configured to reduce and in some cases eliminate electrical and/or optical cross-talk between neighboring pixels from straying visible and infrared light. In some cases, isolation elements can be doped with a dopant that enables the repelling of electrical carriers from the isolation elements or in other words from the side walls of the device. In other cases, isolation elements can include light trapping or reflective materials to optically isolate neighboring pixels. It is additionally contemplated that isolation elements can include both a dopant and a light trapping or reflective material to both electrically and optically isolate the pixels. Moreover, isolation elements can also include surface features formed thereon or associated therewith. Additionally, in some cases a pixel can include a textured region to enhance the detection of infrared light among other things.

In one aspect, a variety of optoelectronic devices are provided such as, without limitation, photosensitive diodes, pixels, and imagers capable of detecting visible and infrared light while exhibiting reduced optical and electrical cross-talk between neighboring pixels or diodes. It is also contemplated that the present scope include methods associated with such devices, including methods of making and using. The present devices can additionally exhibit enhanced absorption and quantum efficiencies. Such devices can also include a plurality of photodiodes or pixels. In some cases, the present devices can achieve a quantum efficiency of 10% for wavelengths at 1064 nm and having a thickness of less than 10 microns. In another embodiment, the present device can achieve a quantum efficiency of about 20% for wavelengths at 940 nm and a thickness of less than 10 microns.

In one aspect, a device can include at least a semiconductor substrate having a first side for receiving incident light and a second side opposite the first side. Either or both the first or second sides can include at least one doped region. Furthermore, the image sensor can include at least

one isolation element or feature for at least partially separating and isolating neighboring pixels. FIG. **1** illustrates a simplified drawing of an imager having a first pixel **102** and a second pixel **104**, that are formed monolithically on a common semiconductor substrate **106** and are isolated from one another by an isolation element **114**. Doped regions **108** and **110** can be disposed on either the first side **120** or second side **122** of the semiconductor substrate, or in some cases on opposite sides of the device. In the present figure, the device is configured such that the first side is capable of receiving incident light. A textured region **112** having surface features is shown on the second side **122** of the semiconductor substrate **106**. This architecture having the texture region **112** on the back side **122** can enable enhanced detection and absorption of electromagnetic radiation having wavelengths in the range of about 600 nm to about 1200 nm. It should be noted that this architecture can be used in either a FSI or BSI image sensor architecture. Furthermore, the textured region can be located on the first side **120**, the second side **122**, or both the first and second sides.

In a typical FSI imager, incident light enters the semiconductor device by first passing by transistors and metal circuitry. The light, however, scatters off of the transistors and circuitry prior to entering the light sensing portion of the imager, thus causing optical loss and noise. A lens can be disposed on the topside of a FSI pixel to direct and focus the incident light to the light sensing active region of the device, thus partially avoiding the circuitry. BSI imagers, one the other hand, are configured to have the light sensing portion of the device opposite the circuitry. Incident light enters the device via the light sensing portion and is at least partially absorbed by the device prior to reaching the circuitry. BSI designs allow for smaller pixel architecture and a high fill factor for the imager. As mentioned, the devices according to aspects of the present disclosure can be adapted for either configuration. It should also be understood that devices according to aspects of the present disclosure can be incorporated into complimentary metal-oxide-semiconductor (CMOS) imager architectures or charge-coupled device (CCD) imager architectures, as well as other optoelectronic devices.

Regarding isolation elements, also referred to herein as trench isolation features or sidewalls, various processes can be employed to form the isolation elements. It is contemplated that the isolation features can extend from either the first surface or the second surface into the semiconductor material and depending on the depth of the trench can be considered either deep trench isolation or shallow trench isolation. The dimensions of the trench can vary, depending on the application. For example, trenches can have parallel walls, or they can have sloping walls, bottle neck architecture, or any other useful configuration. The depth of the trench isolation feature can be in the range of from about 100 nm to about 50 μm depending on the design of the device. The width can be in the range of from about 100 nm to about 10 μm. For simplicity, the figures in this disclosure show deep trench isolation but it should be understood that shallow trench isolation architectures can be utilized, and that deep trench isolation need not completely extend from one side to the other. The processes contemplated for forming trenches or other isolation features can include, reactive ion etch, isotropic plasma etch, wet chemical etch, laser irradiation, or any other known etch technique.

A variety of reflective materials can be utilized in constructing the isolation features in order to provide optical isolation, light trapping, and/or electrical isolation, and any such material capable of incorporation into a photosensitive device is considered to be within the present scope. Non-limiting examples of such materials include a Bragg reflector, a metal reflector, a metal reflector over a dielectric material, a transparent conductive oxide such as zinc oxide, indium oxide, or tin oxide, and the like, including combinations thereof. Non-limiting examples of metal reflector materials can include silver, aluminum, gold, platinum, reflective metal nitrides, reflective metal oxides, and the like, including combinations thereof. In one specific aspect, the dielectric layer can include an oxide layer and the reflecting region can include a metal layer. The surface of the metal layer on an oxide acts as a mirror-like reflector for the incident electromagnetic radiation. In addition, in some aspects trench isolation features can be doped to further affect the properties of the material with respect to electrical isolation.

In one specific aspect, a reflective region can include a transparent conductive oxide, an oxide, and a metal layer. The transparent oxide can be textured and a metal reflector deposited thereupon. The textured surface of the metal on a roughened transparent conductive oxide can act as a diffusive scattering site for the incident electromagnetic radiation.

In some cases, materials having disparate properties can be utilized in the trench isolation features in order to derive a useful combined interaction. As is shown in FIG. **2**, for example, an imager having at least two pixels or photodiodes (**202** and **204**) and at least one isolation element **214**. The pixels are shown formed monolithically on a common semiconductor substrate **206**. Doped regions **208** and **210** can be disposed on either the first side **220** or second side **222** of the semiconductor substrate. A textured region **212** having surface features is created on the second side **222** of the semiconductor substrate **206**.

In some aspects, the isolation element **214** can be designed to function as a Bragg reflector. In such cases, the isolation element **214** includes at least two layers **216** comprised of material having a lower refractive index (n) as compared to the material of the third layer **218** disposed or sandwiched therebetween. In other words, the isolation element includes a high refractive index material sandwiched between two low refractive index materials, and such a configuration forms a Bragg reflector. Additionally, in some aspects the low reflective index materials can be chosen to have a lower refractive index as compared to the semiconductor substrate **206**.

Furthermore, in another aspect an isolation element or light trapping material can include a higher refractive index material sandwiched between two materials having a refractive index that is at least 0.2 lower as compared to the higher refractive index material. In this case, the materials are not limited by the definition of low vs. high refractive index outlined below, but are rather defined by the relative difference in refractive index. For example, in one aspect a light trapping material can include silicon dioxide/silicon nitride/silicon dioxide, each material of which would be considered to be a low refractive index material. There is, however, a greater than 0.2 difference in the refractive indexes between silicon dioxide and silicon nitride, and thus such an isolation element would be included within the present scope. It is also noted that the light trapping material can have greater than three layers. As one non-limiting example, a material can have silicon dioxide/silicon nitride/polysilicon/silicon nitride/silicon dioxide.

As has been described, in some aspects a Bragg reflector can be utilized as an isolation element to trap electromagnetic radiation within the pixel. A Bragg reflector is a

structure formed from multiple layers of alternating materials with varying refractive indexes, or by a periodic variation of some characteristic (e.g. height) of a dielectric waveguide, resulting in periodic variation in the effective refractive index in the guide. Each layer boundary causes a partial reflection of an optical wave. For waves whose wavelength is close to four times the optical thickness of the layers, the many reflections combine with constructive interference, and the layers act as a high-quality reflector. Thus the coherent super-positioning of reflected and transmitted light from multiple interfaces in the structure interfere so as to provide the desired reflective, transmissive, and absorptive behavior. In one aspect, a Bragg reflector can be made as in FIG. **2**, whereby a high refractive index material sandwiched between two low refractive index materials. In one specific aspect, for example, the Bragg reflector can be constructed of a layer of polysilicon sandwiched between two layers of silicon dioxide. Because of the high refractive index difference between silicon and silicon dioxide, and the thickness of these layers, this structure can be fairly low loss even in regions where bulk silicon absorbs appreciably. Additionally, because of the large refractive index difference, the optical thickness of the entire layer set can be thinner, resulting in a broader-band behavior and fewer fabrications steps.

In terms of optical isolation from pixel to pixel, the large index of refraction mismatch can result in total reflection at the trench side walls. To prevent excessive dark current in the pixels, a passivation layer may be disposed on the side walls of the trench to prevent the generation of carriers and leakage current. Silicon nitride deposited over a thin grown oxide layer is also commonly used, in this case the oxide may be a low temperature grown plasma oxide.

It can be shown through calculations that a low recombination velocity of silicon oxide and silicon nitride is the result of moderately high positive oxide charge (5×10^{11} to 1×10^{12} cm^{-2}) and relatively low midgap interface state density (1×10^{10} to 4×10^{10} cm^{-2} eV^{-1}). The addition of silicon oxide or nitride can reduce surface recombination and surface generation. Reducing the surface recombination can increase quantum efficiency of photon collection and surface generation can cause excessive dark current in the imagers thereby reducing the quality of the image.

Since the positive oxide charge of silicon nitride or silicon oxynitride is relatively low on silicon on insulator imagers a p-type layer can be adjacent the silicon oxide, silicon oxynitride and/or silicon nitride layers as an alternative embodiment. In this case the p-type layer will accumulate the surface or the backside of the p-type silicon layer and p-type sidewalls.

Other possible passivation techniques include a hot steam anneal of hydrogenated silicon nitride or the use of amorphous silicon.

Aluminum oxide can also be deposited in the trench to form an isolating barrier. Aluminum oxide can have low stress, a negative fixed charge and higher index of refraction than silicon oxide or low stress silicon oxynitride nitride. Low surface recombination velocities, as low as 10 cm/s can be obtained through various deposition processes of Al_2O_3 layers on the silicon substrate. Low surface recombination can be achieved by field induced surface passivation due to a high density of negative charges stored at the interface. PECVD aluminum oxide is described here for the backside passivation of the backside and backside trenches in backside illuminated image sensors.

The index of refraction of the aluminum oxide can be increased slightly as required by the addition of other metallic elements to make ternary insulators like Aluminum Oxynitride (AlON), Hafnium Aluminum Oxide (HfAlO), Zirconium Aluminum Oxide (ZrAlO), Lanthanum Aluminum Oxide (LaAlO), Titanium Aluminum Oxide (TiAlO) or quaternary dielectrics like Hafnium Aluminum Oxynitride (HfAlON), Tantalum Aluminum Oxynitride (TaAlON), Lanthanum Aluminum Oxynitride (LaAlON).

Low temperature PECVD deposition processes are contemplated for the backside passivation of the backside and backside trenches in backside illuminated image sensors. As previously mentioned the large index of refraction mismatch between silicon and the insulators in the trenches results in reflection of the incident light and provides optical isolation. The trenches also provide electrical isolation. Additionally, it can also be beneficial to dope the sidewalls to create a surface field that will improve electrical isolation between the pixels. In one aspect, it can also be beneficial to dope the low refractive index material of the Bragg-type reflectors to increase such electrical isolation.

Returning to FIG. **2**, layers the silicon oxide and polysilicon can optically and electrically isolate the adjacent pixels, as well as function to trap light within the pixel. While any thicknesses capable of forming such a reflector are considered to be within the present scope, layer **216** can have a thickness in the range of from about 50 nm to about 500 nm. Layer **118** can have a thickness in the range of from about 5 nm to about 100 nm. Thus, the difference in refractive indexes and thickness can determine the intensity of the internal reflection of electromagnetic radiation. Notably, other materials such as metals, as well as other material not listed herein can be used to increase internal reflection of the light.

It is noted that, for the purposes of the present disclosure, in one aspect a low refractive index material can have a refractive index of less than about 2.1. In the case of the sandwiched materials, the two low refractive index materials can be the same or different materials having a refractive index of less than about 2.1. Non-limiting examples of low refractive index materials can include oxides, nitrides, oxynitrides, gasses, at least a partial vacuums, and the like, including appropriate combinations thereof. Non-limiting specific examples of such materials can include silicon oxide, silicon nitride, silicon oxynitride, and the like, including combinations thereof. Additionally, a high K dielectric material can also make a suitable low reflective index material due to their low refractive index properties and good dielectric properties, and as such, are considered to be within the present scope. One example is Hafnium oxide, which has a refractive index of about 1.9. Other examples of high K dielectrics include hafnium silicate, zirconium silicate, zirconium dioxide, and the like.

Additionally, in another aspect a high refractive index material can include a material having a refractive index of greater than or equal to about 2.1. Thus, in the case of the sandwiched materials, the high refractive index material disposed between the low refractive index materials has a refractive index of about 2.1 or greater. Non-limiting examples of high refractive index materials can include polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and the like, including appropriate combinations thereof.

In still another aspect of the present disclosure, a photosensitive imager having at least two pixels (**302** and **304**) and at least one trench isolation region **314** is shown in FIG. **3**. The pixels can include a semiconductor substrate **306**, having a first and second surface, **320** and **322** respectively;

at least two doped regions **308** and **310**, and a textured region **312** formed at least on the opposite side of the light incident surface (i.e. the second side **322**). The textured region **312** can have surface features configured to reflect and disperse light. Further, the sidewalls can include a texture region **312** to increase the internal reflections of light. Regarding the isolation element **314** in FIG. **3**, the isolation element can include several layers of materials that can passivate the sidewalls and each have a different index of refraction, as was described in FIG. **2**. Further, a textured region **312** can be formed on the side walls of the isolation element(s) **314**.

The present disclosure additionally provides pixels and imager devices, including imager arrays, which trap light therewithin. In one aspect as is shown in FIG. **4**, for example, a light trapping pixel device can include a light sensitive pixel or device **402** having a light incident surface **420**, a backside surface **422** opposite the light incident surface **420**, and a peripheral sidewall **424** disposed into at least a portion of the pixel **402** and extending at least substantially around the pixel periphery. It is noted that the pixel sidewall is also known as a trench. The pixel can also include a backside light trapping material **426** substantially covering, partially covering, or completely covering the backside surface **422**. A peripheral light trapping material **428** can be substantially covering, partially covering, or completely covering the peripheral sidewall **424**. As such, light contacting the backside light trapping material **426** or the peripheral light trapping material **428** is reflected back toward the pixel **402**. Also shown in FIG. **4** are at least two doped regions **408** and **410** and an optional textured region **412**. It is noted that, in addition to a single pixel as shown, pixel arrays are also contemplated and are to be included in the present scope.

The light trapping materials of FIG. **4** can be as described above, either single or multiple layer structures. In one aspect, for example, at least one of the backside light trapping material **426** and the peripheral light trapping material **428** includes a high refractive index material sandwiched between two low refractive index materials. In another aspect, the backside light trapping material **426** and the peripheral light trapping material **428** includes a high refractive index material sandwiched between two low refractive index materials. It is noted that these light trapping materials are shown in FIG. **4** as a single layer for clarity, and that multiple layers are contemplated. Furthermore, the peripheral sidewall can extend for a portion, a substantial portion, or completely around the pixel periphery. Additionally, as has been described herein, the peripheral sidewall can extend partially into the pixel, substantially through the pixel, or completely through the pixel to the backside surface. Thus, both deep and shallow trenches are contemplated.

In another aspect, as is shown in FIG. **5**, a pixel **502** can include a frontside light trapping material **530** that at least partially covers, substantially covers, or completely covers the light incident surface **520**. The frontside light trapping material **530** can be multiple layer of materials have a variety of properties and uses, including passivation, anti-reflection, light trapping, and the like, including combinations thereof. Note that numerical indicators in FIG. **5** from previous figures are intended to reflect the previous descriptions for those elements, and as such, reference is made to FIG. **4**.

In another aspect, as is shown in FIG. **6**, a pixel **602** can include a frontside light trapping material **632** associated with the light incident surface **620** that is an internal reflective layer having an aperture **634** to allow entry of light **690** into the pixel **602**. The frontside light trapping material **632** is thus operable to reflect light impinging thereupon from inside the pixel **602** back into the pixel. Additionally, in some aspects a lens **636** can be functionally coupled to the aperture **634** to focus incident light **690** through the aperture **634** and into the pixel **602**. The effective surface area of the aperture compared to the frontside surface area of the pixel can vary depending on the design of the device and the presence, absence, or particular properties of a lens. In one aspect, however, the aperture can be large enough to accept and trap incoming light to a degree that increases the efficiency of the pixel. In one specific aspect, the aperture has an effective surface area of less than about 90% of the incident light surface total surface area. It is noted that various elements such as the doped regions and the optional textured layer are not shown in FIG. **6** for clarity. Furthermore, numerical indicators in FIG. **6** from previous figures are intended to reflect the previous descriptions for those elements, and as such, reference is made to FIG. **4**.

The frontside light trapping material can be made of a variety of materials including metals as have been described herein with respect to other light trapping materials. As such, any material that can be applied to the light incident surface and that is internally reflective toward the inside of the pixel is considered to be within the present scope. Thus, the aforementioned pixel is reflective on 6 internal sides, and as such, light entering the pixel that is not absorbed will interact with and be reflected internally be either the backside, peripheral sidewall, or frontside light trapping materials. Light is thus effectively maintained inside the pixel until it is absorbed.

In another aspect of the present disclosure, a method of making a light trapping pixel device is provided. Such a method can include, as is shown in FIG. **7**, **702** forming a pixel by: **704** forming a backside light trapping material on a semiconductor layer, the backside light trapping material including a high refractive index material sandwiched between two low refractive index materials, and **706** forming a pixel device layer on the semiconductor layer opposite the light trapping material. The method can additionally include **708** etching a trench circumscribing the pixel device layer and **710** filling the trench with a light trapping material. Further details regarding the wafer bonding and wafer-bonded structures described can be found in copending U.S. application Ser. No. 13/069,135, filed on Mar. 22, 2011, which is incorporated herein by reference.

The formation of the backside light trapping material can be accomplished by a variety of techniques, all of which are considered to be within the present scope. In one aspect, for example, depositing a first low refractive index material onto the semiconductor layer, bonding the first low refractive index material to a high refractive index material having a second low refractive index material coupled thereto such that the high refractive index material is sandwiched in between the first and second low refractive index materials. In some cases the second low refractive index material can be coupled to a carrier wafer. In another aspect, the first low refractive index can be deposited onto the semiconductor layer followed by deposition of the high refractive index material and then the second low refractive index material. In another aspect, the layered structure can be formed on a carrier wafer, and the outermost low refractive index material can then be bonded to the semiconductor layer. The carrier wafer can then be optionally removed. In yet another aspect, the first refractive index material can be deposited onto the semiconductor layer, the second refractive index

material can be deposited onto a carrier wafer, and the high refractive index material can be deposited onto either the first or second refractive index material, followed by bonding of the structure together.

As has been described, the trench can be a shallow trench or a deep trench. In one aspect, however, etching the trench circumscribing the pixel device layer can further include etching the trench to a depth that contacts at least the first low refractive index material. Furthermore, the method can also include applying an incident light trapping material to the pixel device layer.

In some aspects the various trenches can be filled with a material, or they can be gas filled or have a partial vacuum applied thereto. For those aspects whereby the trenches will be filled in with a non-gas material, a variety of deposition techniques are contemplated and all are considered to be within the present scope. In one aspect, however, the trench can be filled with a high refractive index material and a low refractive index material in a sandwich structure as has been described. In one exemplary technique, the filling of the trench with such light trapping material can include depositing a low refractive index material into the trench to fill a portion of the trench from the trench walls inward, ceasing deposition of the low refractive index material to leave an internal space within the trench, and depositing a high refractive index material into the trench to fill the internal space. As such, the sandwiched layer of low-high-low refractive index materials is thus created in the trench.

In another aspect, the method can also include forming a textured region on at least a portion of the semiconductor layer between the semiconductor layer and the first low refractive index prior to depositing the first low refractive index material onto the semiconductor layer. Non-limiting examples of texture formation techniques can include plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof. In one specific aspect, the textured region includes laser texturing.

A device design having a textured region located on, for example, the back surface of a photodetector, provides significant performance benefits. The textured region can have surface features that can lead to higher recombination of photocarriers for short wavelengths (e.g. in the blue green part of the spectrum) due to the very shallow penetration of those wavelengths into the detecting volume of the device. By physically locating the textured on the back surface of the device, a pristine surface is provided for the collection of short wavelengths on the top surface (i.e. the light incident surface), and the longer wavelengths that penetrate deep into or through the detecting region of the semiconductor material are collected by or with the help of the textured region opposite the light incident surface.

The textured region can be of various thicknesses, depending on the desired use of the material. In one aspect, for example, the textured region has a thickness of from about 500 nm to about 100 μm. In another aspect, the textured region has a thickness of from about 500 nm to about 15 μm. In yet another aspect, the textured region has a thickness of from about 500 nm to about 2 μm. In a further aspect, the textured region has a thickness of from about 500 nm to about 1 μm. In another aspect, the textured region has a thickness of from about 200 nm to about 2 μm.

The textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and/or to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device. The textured region can include surface features to further increase the effective absorption length of the device. Non-limiting examples of shapes and configurations of surface features include cones, pillars, pyramids, micolenses, quantum dots, inverted features, gratings, protrusions, sphere-like structures, and the like, including combinations thereof. Additionally, surface features can be micron-sized, nano-sized, or a combination thereof. For example, cones, pyramids, protrusions, and the like can have an average height within this range. In one aspect, the average height would be from the base of the feature to the distal tip of the feature. In another aspect, the average height would be from the surface plane upon which the feature was created to the distal tips of the feature. In one specific aspect, a feature (e.g. a cone) can have a height of from about 50 nm to about 2 μm. As another example, quantum dots, microlenses, and the like can have an average diameter within the micron-sized and/or nano-sized range.

In addition to or instead of surface features, the textured region can include a textured film layer. In one aspect, for example, the textured region can include a substantially conformal textured film layer. Such a textured film layer can have an average thickness of from about 1 nm to about 20 μm. In those aspects where the textured region includes surface features, the conformal textured film layer can have a varying thickness relative to the location on the surface features upon which is deposited. In the case of cones, for example, the conformal textured film layer can become thinner toward the tips of the cones. Such a conformal film layer can include various materials, including, without limitation, SiO_2, Si_3N_4, amorphous silicon, polysilicon, a metal or metals, and the like, including combinations thereof. The conformal textured film layer can also be one or more layers of the same or different materials, and can be formed during the creation of surface features or in a separate process.

Textured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared). Such internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor layer. This increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.

The texturing process can texture the entire substrate to be processed or only a portion of the substrate. In one aspect, for example, a substrate such as the semiconductor layer can be textured and patterned by an appropriate technique over an entire surface to form the texture region. In another aspect, a substrate such as the semiconductor layer can be textured and patterned across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch or a laser process to define a specific structure or pattern.

In addition to surface features, the textured region can have a surface morphology that is designed to focus or otherwise direct electromagnetic radiation. For example, in one aspect the textured region has a surface morphology operable to direct electromagnetic radiation into the semiconductor layer. Non-limiting examples of various surface morphologies include sloping, pyramidal, inverted pyramidal, spherical, square, rectangular, parabolic, asymmetric, symmetric, and the like, including combinations thereof.

The textured region, including surface features as well as surface morphologies, can be formed by various techniques, including plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching (e.g. anisotropic etch-

ing, isotropic etching), nanoimprinting, material deposition, selective epitaxial growth, and the like.

One effective method of producing a textured region is through laser processing. Such laser processing allows discrete target areas of a substrate to be textured, as well as entire surfaces. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope. Laser treatment or processing can allow, among other things, enhanced absorption properties and thus increased electromagnetic radiation focusing and detection.

In one aspect, for example, a target region of the substrate to be textured can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Pat. Nos. 7,057,256, 7,354,792 and 7,442,629, which are incorporated herein by reference in their entireties. Briefly, a surface of a substrate material is irradiated with laser radiation to form a textured or surface modified region. Such laser processing can occur with or without a dopant material. In those aspects whereby a dopant is used, the laser can passed through a dopant carrier and onto the substrate surface. In this way, dopant from the dopant carrier is introduced into the target region of the substrate material. Such a region incorporated into a substrate material can have various benefits in accordance with aspects of the present disclosure. For example, the textured region typically has a textured surface that increases the surface area and increases the probability of radiation absorption. In one aspect, such a textured region is a substantially textured surface including micron-sized and/or nano-sized surface features that have been generated by the laser texturing. In another aspect, irradiating the surface of a substrate material includes exposing the laser radiation to a dopant such that irradiation incorporates the dopant into the substrate. Various dopant materials are known in the art, and are discussed in more detail herein.

Thus the surface of the substrate at the target region is thus chemically and/or structurally altered by the laser treatment, which may, in some aspects, result in the formation of surface features appearing as structures or patterned areas on the surface and, if a dopant is used, the incorporation of such dopants into the substrate material. In some aspects, the features or structures can be on the order of 50 nm to 20 μm in size and can assist in the absorption of electromagnetic radiation. In other words, the textured surface can increase the probability of incident radiation being absorbed.

A variety of semiconductor materials are contemplated for use with the pixel devices and methods according to aspects of the present disclosure. Such materials can be utilized as the semiconductor layer and/or the semiconductor substrate, as well as for the secondary semiconductor layer and the epitaxially grown semiconductor layer. Non-limiting examples of such semiconductor materials can include group IV materials, compounds and alloys comprised of materials from groups II and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can include silicon carbide (SiC) and silicon germanium (SiGe). In one specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum gallium arsenide, and combinations thereof.

Exemplary combinations of group II-VI materials can include cadmium selenide (CdSe), cadmium sulfide (CdS), cadmium telluride (CdTe), zinc oxide (ZnO), zinc selenide (ZnSe), zinc sulfide (ZnS), zinc telluride (ZnTe), cadmium zinc telluride (CdZnTe, CZT), mercury cadmium telluride (HgCdTe), mercury zinc telluride (HgZnTe), mercury zinc selenide (HgZnSe), and combinations thereof.

Exemplary combinations of group III-V materials can include aluminum antimonide (AlSb), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum phosphide (AlP), boron nitride (BN), boron phosphide (BP), boron arsenide (BAs), gallium antimonide (GaSb), gallium arsenide (GaAs), gallium nitride (GaN), gallium phosphide (GaP), indium antimonide (InSb), indium arsenide (InAs), indium nitride (InN), indium phosphide (InP), aluminum gallium arsenide (AlGaAs, $Al_xGa_{1-x}As$), indium gallium arsenide (InGaAs, $In_xGa_{1-x}As$), indium gallium phosphide (InGaP), aluminum indium arsenide (AlInAs), aluminum indium antimonide (AllnSb), gallium arsenide nitride (GaAsN), gallium arsenide phosphide (GaAsP), aluminum gallium nitride (AlGaN), aluminum gallium phosphide (AlGaP), indium gallium nitride (InGaN), indium arsenide antimonide (InAsSb), indium gallium antimonide (InGaSb), aluminum gallium indium phosphide (AlGaInP), aluminum gallium arsenide phosphide (AlGaAsP), indium gallium arsenide phosphide (InGaAsP), aluminum indium arsenide phosphide (AlInAsP), aluminum gallium arsenide nitride (AlGaAsN), indium gallium arsenide nitride (InGaAsN), indium aluminum arsenide nitride (InAlAsN), gallium arsenide antimonide nitride (GaAsSbN), gallium indium nitride arsenide antimonide (GaInNAsSb), gallium indium arsenide antimonide phosphide (GaInAsSbP), and combinations thereof.

The semiconductor material can be of any thickness that allows the desired property or functionality of the semiconductor device, and thus any such thickness of semiconductor material is considered to be within the present scope. The textured region can increase the efficiency of the device such that, in some aspects, the semiconductor material can be thinner than has previously been possible. Decreasing the thickness reduces the amount of semiconductor material used to make such a device. In one aspect, for example, a semiconductor material such as the semiconductor layer has a thickness of from about 500 nm to about 50 μm. In another aspect, the semiconductor material has a thickness of less than or equal to about 500 μm. In yet another aspect, the semiconductor material has a thickness of from about 1 μm to about 10 μm. In a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 750 μm. In yet a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 100 μm.

Additionally, various configurations of semiconductor materials are contemplated, and any such material configuration that can be incorporated into a semiconductor device is considered to be within the present scope. In one aspect, for example, the semiconductor material can include monocrystalline materials. In another aspect, the semiconductor material can include multicrystalline materials. In yet another aspect, the semiconductor material can include microcrystalline materials. It is also contemplated that the semiconductor material can include amorphous materials.

As has been described, the semiconductor substrate can be of any size, shape, and material capable of supporting the semiconductor layer and associated components during

manufacture and/or use. The semiconductor substrate can be made from various materials, including the semiconductor materials described above, as well as non-semiconductor materials. Non-limiting examples of such materials can include metals, polymeric materials, ceramics, glass, and the like. In some aspects, the semiconductor substrate and the semiconductor layer have the same or substantially the same thermal expansion properties.

Furthermore, the semiconductor material according to aspects of the present disclosure can comprise multiple layers. In some aspects, layers can vary in majority carrier polarity (i.e. donor or acceptor impurities). The donor or acceptor impurities are typically determined by the type of dopant/impurities introduced into the device either through a growth process, deposition process, epitaxial process, implant process, lasing process or other known process to those skilled in the art. In some aspects such semiconductor materials can include an n-type layer, an intrinsic (i-type) layer, and a p-type layer, thus forming a p-i-n semiconductor material stack that creates a junction and/or depletion region. A semiconductor material devoid of an i-type layer is also contemplated in accordance with the present disclosure. In other aspects the semiconductor material may include multiple junctions. Additionally, in some aspects, variations of n(−−), n(−), n(+), n(++), p(−−), p(−), p(+), or p(++) type semiconductor layers can be used. The minus and positive signs are indicators of the relative magnitude of the doping of the semiconductor material.

A variety of dopant materials are contemplated for both the formation of doped regions in the semiconductor layer and for doping of the textured region, and any dopant that can be used in such processes to modify a material is considered to be within the present scope. It should be noted that the particular dopant utilized can vary depending on the material being doped, as well as the intended use of the resulting material.

A dopant can be either a charge donating or a charge accepting dopant species. More specifically, an electron donating or a hole donating species can cause a region to become more positive or negative in polarity as compared to the substrate upon which the rests. In one aspect, for example, the doped region can be p-doped. In another aspect the doped region can be n-doped.

In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof. It should be noted that the scope of dopant materials should include, not only the dopant materials themselves, but also materials in forms that deliver such dopants (i.e. dopant carriers). For example, S dopant materials includes not only S, but also any material capable being used to dope S into the target region, such as, for example, H_2S, SF_6, SO_2, and the like, including combinations thereof. In one specific aspect, the dopant can be S. Sulfur can be present at an ion dosage level of from about 5×10^{14} to about 3×10^{20} ions/cm^2. Non-limiting examples of fluorine-containing compounds can include ClF_3, PF_5, F_2 SF_6, BF_3, GeF_4, WF_6, SiF_4, HF, CF_4, CHF_3, CH_2F_2, CH_3F, C_2F_6, C_2HF_5, C_3F_8, C_4F_8, NF_3, and the like, including combinations thereof. Non-limiting examples of boron-containing compounds can include $B(CH_3)_3$, BF_3, BCl_3, BN, $C_2B_{10}H_{12}$, borosilica, B_2H_6, and the like, including combinations thereof. Non-limiting examples of phosphorous-containing compounds can include PF_5, PH_3, $POCl_3$, P_2O_5, and the like, including combinations thereof. Non-limiting examples of chlorine-containing compounds can include Cl_2, SiH_2Cl_2, HCl, $SiCl_4$, and the like, including combinations thereof. Dopants can also include arsenic-containing compounds such as AsH_3 and the like, as well as antimony-containing compounds. Additionally, dopant materials can include mixtures or combinations across dopant groups, i.e. a sulfur-containing compound mixed with a chlorine-containing compound. In one aspect, the dopant material can have a density that is greater than air. In one specific aspect, the dopant material can include Se, H_2S, SF_6, or mixtures thereof. In yet another specific aspect, the dopant can be SF_6 and can have a predetermined concentration range of about 5.0×10^{-8} mol/cm^3 to about 5.0×10^{-4} mol/cm^3. As one non-limiting example, SF_6 gas is a good carrier for the incorporation of sulfur into a substrate via a laser process without significant adverse effects on the material. Additionally, it is noted that dopants can also be liquid solutions of n-type or p-type dopant materials dissolved in a solution such as water, alcohol, or an acid or basic solution. Dopants can also be solid materials applied as a powder or as a suspension dried onto the wafer.

In another aspect, the band structure optimization can be realized by forming a heterojunction along a modified semiconductor interface. For example, a layer of amorphous silicon can be deposited on the textured region interface, thus forming a heterojunction that bends the minority carrier band towards the desired energy direction.

What is claimed is:

1. A light trapping device, comprising:

at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

a backside light trapping material at least partially covering the backside surface; and

a peripheral light trapping material substantially covering the peripheral sidewall;

wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel;

wherein at least one of the backside light trapping material or the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.

2. The device of claim **1**, wherein the two low refractive index materials have a refractive index of less than about 2.1.

3. The device of claim **2**, wherein at least one of the two low refractive index material includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.

4. The device of claim **2**, wherein the at least one of the two low refractive index materials includes a member selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.

5. The device of claim **1**, wherein the high refractive index material includes a material having a refractive index of greater than or equal to about 2.1.

6. The device of claim **5**, wherein the high refractive index material includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and combinations thereof.

7. The device of claim **1**, wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field.

8. The device of claim **7**, wherein the dopant is boron or antimony.

9. The device of claim **1**, wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials, and wherein the difference in refractive index between the first material and the two second materials is at least 0.2.

10. The device of claim **1**, wherein the peripheral sidewall extends completely around the pixel periphery.

11. The device of claim **1**, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

12. The device of claim **1**, further comprising a frontside light trapping material at least partially covering the light incident surface.

13. The device of claim **12**, wherein the frontside light trapping material is an antireflective layer coating.

14. The device of claim **12**, wherein the frontside light trapping material is a reflective layer having an aperture to allow entry of light into the pixel, wherein the reflective layer is operable to reflect light impinging thereupon from inside the pixel back into the pixel.

15. The device of claim **14**, further comprising a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.

16. The device of claim **14**, wherein the aperture has an effective surface area of 90% of the incident light surface total surface area.

17. The device of claim **1**, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

18. The device of claim **1**, wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface.

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