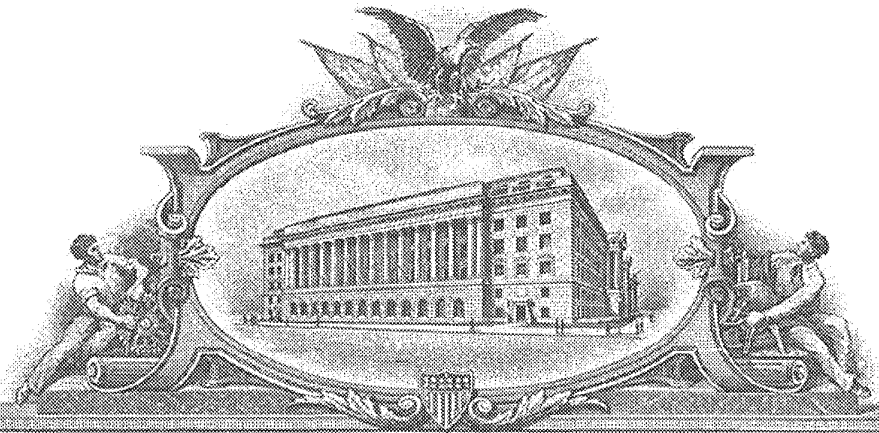


8448986



THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

January 16, 2024

**THIS IS TO CERTIFY THAT ANNEXED IS A TRUE COPY FROM THE
RECORDS OF THIS OFFICE OF THE FILE WRAPPER AND CONTENTS
OF:**

APPLICATION NUMBER: 17/214,333
FILING DATE: March 26, 2021
PATENT NUMBER: 11721714
ISSUE DATE: August 08, 2023



Certified by

Kathi

Performing the Functions and Duties of the
Under Secretary of Commerce
for Intellectual Property
and Director of the United States
Patent and Trademark Office

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Martin Pralle *et al.*

Application No.: Not yet assigned

Filed: Concurrently herewith

For: PIXEL ISOLATION ELEMENTS, DEVICES AND
ASSOCIATED METHODS

Confirmation No.: Not yet assigned

Art Unit: Not yet assigned

Examiner: Not yet assigned

VIA EFS-WEB

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

Certificate of Mailing

I hereby certify that this correspondence is being electronically filed via EFS-Web to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

March 26, 2021

Dated

Electronic Signature: /Andrew W. Schultz/

Andrew Schultz, Reg. No. 66,869

FIRST PRELIMINARY AMENDMENT UNDER 37 C.F.R. § 1.115

Dear Sir,

Prior to examination on the merits, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 5.

AMENDMENTS TO THE CLAIMS

1. (Original) A light trapping device, comprising:
at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;
a backside light trapping material substantially covering the backside surface;
and
a peripheral light trapping material substantially covering the peripheral sidewall;
wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.
2. (Original) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.
3. (Original) The device of claim 1, wherein the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.
4. (Original) The device of claim 3, wherein the two low refractive index materials have a refractive index of less than about 2.1.
5. (Original) The device of claim 4, wherein at least one of the two low refractive index material includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.
6. (Original) The device of claim 4, wherein the at least one of the two low refractive index materials includes a member selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.

7. (Original) The device of claim 3, wherein the high refractive index material includes a material having a refractive index of greater than or equal to about 2.1.
8. (Original) The device of claim 7, wherein the high refractive index material includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and combinations thereof.
9. (Original) The device of claim 2, wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field.
10. (Original) The device of claim 9, wherein the dopant is boron or antimony.
11. (Original) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials, and wherein the difference in refractive index between the first material and the two second materials is at least 0.2.
12. (Original) The device of claim 1, wherein the peripheral sidewall extends completely around the pixel periphery.
13. (Original) The device of claim 1, wherein the peripheral sidewall extends from the light incident surface to the backside surface.
14. (Original) The device of claim 1, further comprising a frontside light trapping material at least partially covering the light incident surface.
15. (Original) The device of claim 14, wherein the frontside light trapping material is an antireflective layer coating.
16. (Original) The device of claim 14, wherein the frontside light trapping material is a reflective layer having an aperture to allow entry of light into the pixel, wherein the reflective layer is operable to reflect light impinging thereupon from inside the pixel back into the pixel.

17. (Original) The device of claim 16, further comprising a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.

18. (Original) The device of claim 16, wherein the aperture has an effective surface area of 90% of the incident light surface total surface area.

19. (Original) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

20. (Original) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface.

21-33. (Canceled)

App. No.: Not yet assigned
Art Unit: Not yet assigned

Docket No.: SXM-052CN4
Examiner: Not yet assigned

REMARKS

Prior to examination on the merits, Applicant respectfully requests that claims 21-33 be canceled as shown on the attached sheets. No new matter is added.

The Director is authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 50-1196, under Docket No. SXM-052CN4.

Dated: March 26, 2021

Respectfully submitted,
Electronic Signature: /Andrew W. Schultz/
Andrew W. Schultz, Reg. No. 66,869
Attorney for Applicant
Nelson Mullins Riley & Scarborough LLP
One Financial Center, Suite 3500
Boston, MA 02109
Tel: (617) 217-4674
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	Not Yet Assigned		
Filing Date	Concurrently Herewith		
First Named Inventor	Martin U. PRALLE		
Title	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS		
Art Unit	Not Yet Assigned		
Examiner Name	Not Yet Assigned		
Attorney Docket Number	SXM-052CN4		
SIGNATURE of Applicant or Patent Practitioner			
Signature	/Andrew W. Schultz/	Date (Optional)	March 26, 2021
Name	Andrew Schultz	Registration Number	66,869
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			
NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.			
☐	*Total of <u>1</u> forms are submitted.		

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4).

Dated: March 26, 2021

Electronic Signature for Andrew Schultz: /Andrew W. Schultz/

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

00959

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☒ Firm or Individual Name NELSON MULLINS RILEY & SCARBOROUGH LLP

Address One Post Office Square, 30th Floor

City	Boston	State	MA	Zip	02109-2127
Country	US				
Telephone	800-237-2000	Email	ipboston.docketing@nelsonmullins.com		

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

SiOnyx, LLC

☐ Inventor or Joint Inventor (title not required below)

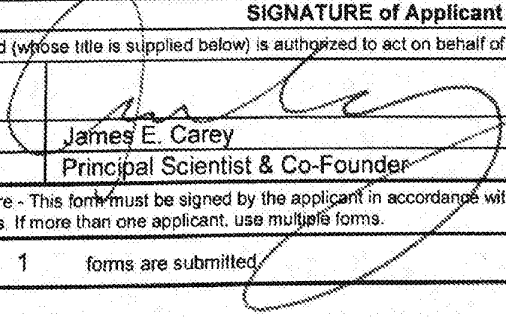
☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	
Name	James E. Carey		
Title	Principal Scientist & Co-Founder		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of 1 forms are submitted

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SXM-052CN4
		Application Number	
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--------------------------	---

Inventor Information:

Inventor	1				Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Martin	U.	Pralle			
Residence Information (Select One) • US Residency Non US Residency Active US Military Service						
City	Wayland	State/Province	MA	Country of Residence	US	
Mailing Address of Inventor:						
Address 1		15 Rice Spring Lane				
Address 2						
City	Wayland	State/Province	MA			
Postal Code	01778	Country	US			
Inventor	2				Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Jeffrey		McKee			
Residence Information (Select One) • US Residency Non US Residency Active US Military Service						
City	Tualatin	State/Province	OR	Country of Residence	US	
Mailing Address of Inventor:						
Address 1		22850 SW. Eno Place				
Address 2						
City	Tualatin	State/Province	OR			
Postal Code	97062	Country	US			
Inventor	3				Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Jason		Sickler			
Residence Information (Select One) • US Residency Non US Residency Active US Military Service						

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		SXM-052CN4	
		Application Number			
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS				
City	Arlington	State/Province	MA	Country of Residence	US
Mailing Address of Inventor:					
Address 1	53 Varnum Street				
Address 2					
City	Arlington	State/Province	MA		
Postal Code	02474	Country	US		
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.					Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number	00959		
Email Address	ipboston.docketing@nelsonmullins.com	Add Email	Remove Email

Application Information:

Title of the Invention	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS		
Attorney Docket Number	SXM-052CN4	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	4	Suggested Figure for Publication (if any)	
Filing By Reference:			
Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").			
For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).			
Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SXM-052CN4
		Application Number	
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS		

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	00959		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
	Continuation of	16290740	2019-03-01		
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16290740	Continuation of	15216244	2016-07-21	10224359	2019-03-05
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15216244	Continuation of	14747875	2015-06-23	9905599	2018-02-27
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14747875	Continuation of	13841120	2013-03-15	9064764	2015-06-23
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
13841120	Claims benefit of provisional	61614275	2012-03-22		
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.					Add

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SXM-052CN4
		Application Number	
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS		

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)ⁱ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ⁱ (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SXM-052CN4
		Application Number	
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SXM-052CN4
		Application Number	
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant	1 Remove		
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section. Clear			
☒ Assignee		☐ Legal Representative under 35 U.S.C. 117	
☐ Joint Inventor			
Person to whom the inventor is obligated to assign.		Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor:			
If the Applicant is an Organization check here. ☒			
Organization Name	SiOnyx LLC		
Mailing Address Information For Applicant:			
Address 1	100 Cummings Center, Suite 303B		
Address 2			
City	Beverly	State/Province	MA
Country	US	Postal Code	01915
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button. Add			

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SXM-052CN4
		Application Number	
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS		

Assignee	1			
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
				Remove
If the Assignee or Non-Applicant Assignee is an Organization check here.				☐
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country i		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.				Add

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the **INITIAL** filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Andrew W. Schultz/		Date (YYYY-MM-DD)	2021-03-26
First Name	Andrew	Last Name	Schultz	Registration Number
				66,869
Additional Signature may be generated within this form by selecting the Add button.				Add

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SXM-052CN4
		Application Number	
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS		
First Named Inventor/Applicant Name:		Martin U. Pralle		
Filer:		Andrew W. Schultz		
Attorney Docket Number:		SXM-052CN4		
Filed as Large Entity				
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Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	320	320
UTILITY SEARCH FEE	1111	1	700	700
UTILITY EXAMINATION FEE	1311	1	800	800
Pages:				
Claims:				
Miscellaneous-Filing:				
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Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
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Total in USD (\$)				1820

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RAM confirmation Number	E20213PG56522303
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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Specification.pdf	212218	yes	32
			9bf3c9e9b4f3339b679b78ad2fdc5e3834be1fb5		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	26	
	Claims		27	31	
	Abstract		32	32	
Warnings:					
Information:					
2	Drawings-other than black and white line drawings	Figures.pdf	164327	no	4
			24cf75db75ad8773936ab895560dcb7bed582dc0		
Warnings:					
Information:					
3	Oath or Declaration filed	Declarations.pdf	138183	no	3
			7d5bba9d67102f4806eb99e9ebf93716ad07c1		
Warnings:					
Information:					
4		Preliminary_Amendment.pdf	38494	yes	5
			b9a4a6b0bc62f89935a0c0bf09e3b94cb89f10f7		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Preliminary Amendment		1	1	

	Claims		2	4
	Applicant Arguments/Remarks Made in an Amendment		5	5
Warnings:				
Information:				
5	Power of Attorney	POA.pdf	2869147 43b285617d5acdac92b1111493d0379a00944c4	no 2
Warnings:				
Information:				
6	Application Data Sheet	ADS.pdf	1608816 6a527810594436cabf7a84487138b53c6ad98424	no 9
Warnings:				
Information:				
7	Fee Worksheet (SB06)	fee-info.pdf	35044 79db338e34b04c0a984e84ef99dfda3d8d8368ae	no 2
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PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS**PRIORITY DATA**

This application is a continuation of U.S. Patent Application No. 16/290,740, filed
5 March 1, 2019, which is a continuation of U.S. Patent Application No. 15/216,244, filed
July 21, 2016, which is a continuation of U.S. Patent Application No. 14/747,875, filed
June 23, 2015, which is a continuation of U.S. Patent Application No. 13/841,120, filed
March 15, 2013, which claims the benefit of U.S. Provisional Patent Application No.
61/614,275, filed on March 22, 2012, each of which are incorporated herein by reference.

10

BACKGROUND

Image sensors are typically formed on various forms of semiconductor materials
such as, for example, silicon. Imagers can be incorporated into a variety of devices,
including digital cameras, camcorders, computers, cell phones, etc. Due to the ever
15 decreasing size (foot print) of these devices, image sensors have correspondingly seen a
decrease in size. Backside illuminated (BSI) image sensors have increased in importance
due to the small size of these imagers as compared to front side illuminated (FSI) image
sensors. However, pixel size reduction can lead to a significant sacrifice in image
quality. As pixel sizes continue to decrease, image signal to noise tends to decrease
20 while electrical and optical cross-talk between adjacent sensor pixels tends to increase.
Traditional attempts to reduce the impact of these effects have included adding
microlenses above each image sensor in front side pixel sensors to focus the light on the
active detector regions, thereby increasing efficiency and reducing cross-talk. Backside
illuminated pixel sensors can present different design considerations. For example,
25 significant cross-talk can be generated due to reflection off the often planar back surface
of the device.

SUMMARY

The present disclosure provides for light trapping pixels, devices incorporating
30 such pixels, photovoltaic solar cells, and other optoelectronic devices, including various
associated methods. In one aspect, for example, a light trapping device can include at

least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery. The pixel can also include a backside light trapping material substantially covering the backside surface and a peripheral light trapping material substantially covering the peripheral sidewall. The light contacting the backside light trapping material or the peripheral light trapping material is thus reflected back toward the pixel. In another aspect, the present disclosure additionally provides an array of light trapping pixels.

A variety of light trapping materials can be utilized and are contemplated, and any such material capable of being used to trap light in a pixel is considered to be within the present scope. In one aspect, at least one of the backside light trapping material and the peripheral light trapping material can include a high refractive index material sandwiched between two low refractive index materials. In another aspect, the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials. It is contemplated that the two low refractive index materials have a refractive index of less than about 2.1. Non-limiting examples of low refractive index material can include nitrides, oxynitrides, gasses, at least a partial vacuum, and the like, including appropriate combinations thereof. Other non-limiting examples of low refractive index materials can include silicon oxide, silicon nitride, silicon dioxide, and the like. Furthermore, in another aspect a light trapping material can include a higher refractive index material sandwiched between two materials having a refractive index that is at least 0.2 lower as compared to the higher refractive index material. In this case, the materials are not limited by the definition of low vs. high refractive index outlined above, but are rather defined by the relative difference in refractive index.

Furthermore, it is contemplated that high refractive index materials have a refractive index of greater than or equal to about 2.1. Non-limiting examples of high refractive index material can include polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and the like, including appropriate combinations thereof.

In one aspect, the peripheral sidewall can extend completely around the pixel periphery. In another aspect, the peripheral sidewall can extend from the light incident surface towards the backside surface.

In some aspects it is also contemplated that the light incident surface can include a
5 frontside light trapping material at least partially covering the surface thereof. In one aspect, the frontside light trapping material can be an antireflective layer coating. In another aspect, the frontside light trapping material can be a reflective layer having an aperture to allow entry of light into the pixel, wherein the reflective layer is operable to reflect light impinging thereupon from inside the pixel back into the pixel. In some
10 aspects it can be beneficial to include a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.

In another aspect the present disclosure additionally provides a substantially light trapping pixel device including a light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending
15 from the light incident surface to the backside surface and extending around the pixel periphery. The pixel additionally includes a backside light trapping material substantially covering the backside surface, and a peripheral light trapping material substantially covering the peripheral sidewall. Furthermore, an internally reflective frontside light trapping material can cover at least a portion of the light incident surface that is operable
20 to allow entrance of light into the pixel and is operable to reflect light impinging thereupon from inside the pixel back into the pixel, and the light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

In yet another aspect, the present disclosure provides a method of making a light
25 trapping device, including forming at least one pixel by forming a backside light trapping material on a semiconductor layer, the backside light trapping material including a high refractive index material sandwiched between two low refractive index materials, and forming a pixel device layer on the semiconductor layer opposite the light trapping material. The method can additionally include etching a trench circumscribing the pixel
30 device layer and filling the trench with a light trapping material. In some aspects, the trench can be etched to a depth that contacts at least the first low refractive index

material. In some aspects, an incident light trapping material can be applied to the pixel device layer. It is also noted that the light trapping material can be located anywhere in the backside region of the device, and that the current scope is not limited to the location of materials or the manufacturing method described above.

5 In another aspect, filling the trench with the light trapping material can further include depositing a low refractive index material into the trench to fill a portion of the trench from the trench walls inward, ceasing deposition of the low refractive index material to leave an internal space within the trench, and depositing a high refractive index material into the trench to fill the internal space.

10 In another aspect, the method can include forming a textured region on at least a portion of the semiconductor layer between the semiconductor layer and the first low refractive index prior to depositing the first low refractive index material onto the semiconductor layer. Non-limiting examples of techniques for forming the textured region include plasma etching, reactive ion etching, porous silicon etching, lasing,
15 chemical etching, nanoimprinting, material deposition, selective epitaxial growth, the like, including appropriate combinations thereof. In one specific aspect, forming the textured region includes laser texturing.

BRIEF DESCRIPTION OF THE DRAWINGS

20 For a further understanding of the nature and advantage of the present disclosure, reference is being made to the following detailed description of embodiments and in connection with the accompanying drawings, in which:

FIG. 1 is a cross-sectional view of multiple image sensor pixels in accordance with an embodiment of the present disclosure;

25 FIG. 2 is a cross-sectional view of multiple image sensor pixels in accordance with another embodiment of the present disclosure;

FIG. 3 is a cross-sectional view of multiple image sensor pixels in accordance with another embodiment of the present disclosure;

FIG. 4 is a cross-sectional view of a light trapping pixel in accordance with
30 another embodiment of the present disclosure;

FIG. 5 is a cross-sectional view of a light trapping pixel in accordance with another embodiment of the present disclosure;

FIG. 6 is a cross-sectional view of a light trapping pixel in accordance with another embodiment of the present disclosure; and

5 FIG. 7 is a depiction of a method of making a light trapping pixel in accordance with yet another aspect of the present disclosure.

DETAILED DESCRIPTION

Before the present disclosure is described herein, it is to be understood that this
10 disclosure is not limited to the particular structures, process steps, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting.

15 Definitions

The following terminology will be used in accordance with the definitions set forth below.

It should be noted that, as used in this specification and the appended claims, the singular forms “a,” and, “the” include plural referents unless the context clearly dictates
20 otherwise. Thus, for example, reference to “a dopant” includes one or more of such dopants and reference to “the layer” includes reference to one or more of such layers.

As used herein, the terms “light” and “electromagnetic radiation” can be used interchangeably and can refer to electromagnetic radiation in the ultraviolet, visible, near infrared and infrared spectra. The terms can further more broadly include
25 electromagnetic radiation such as radio waves, microwaves, x-rays, and gamma rays. Thus, the term “light” is not limited to electromagnetic radiation in the visible spectrum. Many examples of light described herein refer specifically to electromagnetic radiation in the visible and infrared (and/or near infrared) spectra. For purposes of this disclosure, visible range wavelengths are considered to be from approximately 350 nm to 800 nm
30 and non-visible wavelengths are considered to be longer than about 800 nm or shorter than about 350 nm. Furthermore, the infrared spectrum is considered to include a near

infrared portion of the spectrum including wavelengths of approximately 800 to 1100 nm, a short wave infrared portion of the spectrum including wavelengths of approximately 1100 nm to 3 micrometers, and a mid-to-long wavelength infrared (or thermal infrared) portion of the spectrum including wavelengths greater than about 3 micrometers up to about 30 micrometers. These are generally and collectively referred to herein as “infrared” portions of the electromagnetic spectrum unless otherwise noted.

As used herein, “quantum efficiency” (QE) is typically referring to “external quantum efficiency” (EQE) which is defined as the ratio of electrons collected per photons incident on an optoelectronic device. “Internal quantum efficiency” is defined as the ratio of electrons collected per photons absorbed by an optoelectronic device..

As used herein, the terms “3D” and “three dimensional” can be used interchangeably, and refer to obtaining distance information using electromagnetic radiation.

As used herein, the terms “disordered surface” and “textured surface” can be used interchangeably, and refer to a surface having a topology with nano- to micron-sized surface variations. Such a surface topology can be formed by the irradiation of a laser pulse or laser pulses, chemical etching, wet or dry etching including masked or maskless etching, lithographic patterning, interference of multiple simultaneous laser pulses, reactive ion etching, plasma etching or any other technique that can be used to form such a topology. While the characteristics of such a surface can be variable depending on the materials and techniques employed, in one aspect such a surface can be several hundred nanometers thick and made up of nanocrystallites (e.g. from about 10 to about 50 nanometers), nanopores, and the like. In another aspect, such a surface can include micron-sized structures (e.g. about 1 μm to about 60 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 500 μm . A variety of criteria can be utilized to measure the size of such structures. For example, for cone-like structures the above ranges are intended to be measured from the peak of a structure to the valley formed between that structure and an adjacent neighboring structure. For structures such as nanopores, the above ranges are intended to be approximate diameters. Additionally, the surface structures can be spaced at various average distances from one another. In one aspect, neighboring structures can be spaced

at a distance of from about 50nm to about 50 μm . In another aspect, neighboring structures can be spaced at a distance of from about 50nm to about 2 μm . Such spacing is intended to be from a center point of one structure to the center point of a neighboring structure.

5 As used herein, the term “fluence” refers to the amount of energy from a single pulse of laser radiation that passes through a unit area. In other words, “fluence” can be described as the energy density of one laser pulse.

 As used herein, the term “target region” refers to an area of a semiconductor material that is intended to be doped or surface modified. The target region of a
10 semiconductor material can vary as the surface modifying process progresses. For example, after a first target region is doped or surface modified, a second target region may be selected on the same semiconductor material.

 As used herein, the term “absorptance” refers to the fraction of incident electromagnetic radiation absorbed by a material or device.

15 As used herein, the term “monolithic” refers to an electronic device in which electronic components are formed on the same substrate. For example, two monolithic pixel elements are pixel elements that are formed on the same semiconductor substrate.

 As used herein, the term “substantially” refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or
20 result. For example, an object that is “substantially” enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use
25 of “substantially” is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is “substantially free of” particles would either completely lack particles, or so nearly completely lack particles that the effect would be the same as if it completely lacked particles. In other words, a composition that
30 is “substantially free of” an ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

As used herein, the term “about” is used to provide flexibility to a numerical range endpoint by providing that a given value may be “a little above” or “a little below” the endpoint.

As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of “about 1 to about 5” should be interpreted to include not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

The Disclosure

The present disclosure provides semiconductor devices and associated methods that can exhibit various enhanced properties, such as, for example, enhanced light detection properties. More specifically, in one aspect the disclosure relates to image sensor pixels and elements for trapping light within such pixels. In other aspects, various light trapping elements can additionally isolate neighboring pixels in an image sensor. Isolation elements can be configured to optically and/or electrically isolate neighboring

pixels from one another in addition to trapping light within the pixel. It is additionally contemplated that the present disclosure is applicable to other optoelectronic devices such as solar cells, and that all such should be included in the present scope.

5 In various aspects, image sensors can be front side or backside illuminated, 3D sensors, or any other device or system that incorporate a unique isolation element configured to reduce cross-talk between pixel elements. For example, in one aspect an image sensor can be capable of detecting visible and infrared light, whereas an isolation element associated with such an imager can be designed and configured to reduce and in some cases eliminate electrical and/or optical cross-talk between neighboring pixels from straying visible and infrared light. In some cases, isolation elements can be doped with a dopant that enables the repelling of electrical carriers from the isolation elements or in other words from the side walls of the device. In other cases, isolation elements can include light trapping or reflective materials to optically isolate neighboring pixels. It is additionally contemplated that isolation elements can include both a dopant and a light trapping or reflective material to both electrically and optically isolate the pixels. 10 Moreover, isolation elements can also include surface features formed thereon or associated therewith. Additionally, in some cases a pixel can include a textured region to enhance the detection of infrared light among other things.

In one aspect, a variety of optoelectronic devices are provided such as, without 20 limitation, photosensitive diodes, pixels, and imagers capable of detecting visible and infrared light while exhibiting reduced optical and electrical cross-talk between neighboring pixels or diodes. It is also contemplated that the present scope include methods associated with such devices, including methods of making and using. The present devices can additionally exhibit enhanced absorption and quantum efficiencies. 25 Such devices can also include a plurality of photodiodes or pixels. In some cases, the present devices can achieve a quantum efficiency of 10% for wavelengths at 1064nm and having a thickness of less than 10 microns. In another embodiment, the present device can achieve a quantum efficiency of about 20% for wavelengths at 940nm and a thickness of less than 10 microns.

30 In one aspect, a device can include at least a semiconductor substrate having a first side for receiving incident light and a second side opposite the first side. Either or

both the first or second sides can include at least one doped region. Furthermore, the image sensor can include at least one isolation element or feature for at least partially separating and isolating neighboring pixels. FIG. 1 illustrates a simplified drawing of an imager having a first pixel 102 and a second pixel 104, that are formed monolithically on a common semiconductor substrate 106 and are isolated from one another by an isolation element 114. Doped regions 108 and 110 can be disposed on either the first side 120 or second side 122 of the semiconductor substrate, or in some cases on opposite sides of the device. In the present figure, the device is configured such that the first side is capable of receiving incident light. A textured region 112 having surface features is shown on the second side 122 of the semiconductor substrate 106. This architecture having the texture region 112 on the back side 122 can enable enhanced detection and absorption of electromagnetic radiation having wavelengths in the range of about 600 nm to about 1200 nm. It should be noted that this architecture can be used in either a FSI or BSI image sensor architecture. Furthermore, the textured region can be located on the first side 120, the second side 122, or both the first and second sides.

In a typical FSI imager, incident light enters the semiconductor device by first passing by transistors and metal circuitry. The light, however, scatters off of the transistors and circuitry prior to entering the light sensing portion of the imager, thus causing optical loss and noise. A lens can be disposed on the topside of a FSI pixel to direct and focus the incident light to the light sensing active region of the device, thus partially avoiding the circuitry. BSI imagers, on the other hand, are configured to have the light sensing portion of the device opposite the circuitry. Incident light enters the device via the light sensing portion and is at least partially absorbed by the device prior to reaching the circuitry. BSI designs allow for smaller pixel architecture and a high fill factor for the imager. As mentioned, the devices according to aspects of the present disclosure can be adapted for either configuration. It should also be understood that devices according to aspects of the present disclosure can be incorporated into complimentary metal-oxide-semiconductor (CMOS) imager architectures or charge-coupled device (CCD) imager architectures, as well as other optoelectronic devices.

Regarding isolation elements, also referred to herein as trench isolation features or sidewalls, various processes can be employed to form the isolation elements. It is

contemplated that the isolation features can extend from either the first surface or the second surface into the semiconductor material and depending on the depth of the trench can be considered either deep trench isolation or shallow trench isolation. The dimensions of the trench can vary, depending on the application. For example, trenches
5 can have parallel walls, or they can have sloping walls, bottle neck architecture, or any other useful configuration. The depth of the trench isolation feature can be in the range of from about 100 nm to about 50 μm depending on the design of the device. The width can be in the range of from about 100 nm to about 10 μm . For simplicity, the figures in this disclosure show deep trench isolation but it should be understood that shallow trench
10 isolation architectures can be utilized, and that deep trench isolation need not completely extend from one side to the other. The processes contemplated for forming trenches or other isolation features can include, reactive ion etch, isotropic plasma etch, wet chemical etch, laser irradiation, or any other known etch technique.

A variety of reflective materials can be utilized in constructing the isolation
15 features in order to provide optical isolation, light trapping, and/or electrical isolation, and any such material capable of incorporation into a photosensitive device is considered to be within the present scope. Non-limiting examples of such materials include a Bragg reflector, a metal reflector, a metal reflector over a dielectric material, a transparent conductive oxide such as zinc oxide, indium oxide, or tin oxide, and the like, including
20 combinations thereof. Non-limiting examples of metal reflector materials can include silver, aluminum, gold, platinum, reflective metal nitrides, reflective metal oxides, and the like, including combinations thereof. In one specific aspect, the dielectric layer can include an oxide layer and the reflecting region can include a metal layer. The surface of the metal layer on an oxide acts as a mirror-like reflector for the incident electromagnetic
25 radiation. In addition, in some aspects trench isolation features can be doped to further affect the properties of the material with respect to electrical isolation.

In one specific aspect, a reflective region can include a transparent conductive oxide, an oxide, and a metal layer. The transparent oxide can be textured and a metal reflector deposited thereupon. The textured surface of the metal on a roughened
30 transparent conductive oxide can act as a diffusive scattering site for the incident electromagnetic radiation.

In some cases, materials having disparate properties can be utilized in the trench isolation features in order to derive a useful combined interaction. As is shown in FIG. 2, for example, an imager having at least two pixels or photodiodes (202 and 204) and at least one isolation element 214. The pixels are shown formed monolithically on a common semiconductor substrate 206. Doped regions 208 and 210 can be disposed on either the first side 220 or second side 222 of the semiconductor substrate. A textured region 212 having surface features is created on the second side 222 of the semiconductor substrate 206.

In some aspects, the isolation element 214 can be designed to function as a Bragg reflector. In such cases, the isolation element 214 includes at least two layers 216 comprised of material having a lower refractive index (n) as compared to the material of the third layer 218 disposed or sandwiched therebetween. In other words, the isolation element includes a high refractive index material sandwiched between two low refractive index materials, and such a configuration forms a Bragg reflector. Additionally, in some aspects the low reflective index materials can be chosen to have a lower refractive index as compared to the semiconductor substrate 206.

Furthermore, in another aspect an isolation element or light trapping material can include a higher refractive index material sandwiched between two materials having a refractive index that is at least 0.2 lower as compared to the higher refractive index material. In this case, the materials are not limited by the definition of low vs. high refractive index outlined below, but are rather defined by the relative difference in refractive index. For example, in one aspect a light trapping material can include silicon dioxide/silicon nitride/silicon dioxide, each material of which would be considered to be a low refractive index material. There is, however, a greater than 0.2 difference in the refractive indexes between silicon dioxide and silicon nitride, and thus such an isolation element would be included within the present scope. It is also noted that the light trapping material can have greater than three layers. As one non-limiting example, a material can have silicon dioxide/silicon nitride/polysilicon/silicon nitride/silicon dioxide.

As has been described, in some aspects a Bragg reflector can be utilized as an isolation element to trap electromagnetic radiation within the pixel. A Bragg reflector is a structure formed from multiple layers of alternating materials with varying refractive

indexes, or by a periodic variation of some characteristic (e.g. height) of a dielectric waveguide, resulting in periodic variation in the effective refractive index in the guide. Each layer boundary causes a partial reflection of an optical wave. For waves whose wavelength is close to four times the optical thickness of the layers, the many reflections
 5 combine with constructive interference, and the layers act as a high-quality reflector. Thus the coherent super-positioning of reflected and transmitted light from multiple interfaces in the structure interfere so as to provide the desired reflective, transmissive, and absorptive behavior. In one aspect, a Bragg reflector can be made as in FIG. 2, whereby a high refractive index material sandwiched between two low refractive index
 10 materials. In one specific aspect, for example, the Bragg reflector can be constructed of a layer of polysilicon sandwiched between two layers of silicon dioxide. Because of the high refractive index difference between silicon and silicon dioxide, and the thickness of these layers, this structure can be fairly low loss even in regions where bulk silicon absorbs appreciably. Additionally, because of the large refractive index difference, the
 15 optical thickness of the entire layer set can be thinner, resulting in a broader-band behavior and fewer fabrications steps.

In terms of optical isolation from pixel to pixel, the large index of refraction mismatch can result in total reflection at the trench side walls. To prevent excessive dark current in the pixels, a passivation layer may be disposed on the side walls of the trench
 20 to prevent the generation of carriers and leakage current. Silicon nitride deposited over a thin grown oxide layer is also commonly used, in this case the oxide may be a low temperature grown plasma oxide.

It can be shown through calculations that a low recombination velocity of silicon oxide and silicon nitride is the result of moderately high positive oxide charge (5×10^{11} to
 25 $1 \times 10^{12} \text{ cm}^{-2}$) and relatively low midgap interface state density (1×10^{10} to $4 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$). The addition of silicon oxide or nitride can reduce surface recombination and surface generation. Reducing the surface recombination can increase quantum efficiency of photon collection and surface generation can cause excessive dark current in the imagers thereby reducing the quality of the image.

30 Since the positive oxide charge of silicon nitride or silicon oxynitride is relatively low on silicon on insulator imagers a p-type layer can be adjacent the silicon oxide,

silicon oxynitride and/or silicon nitride layers as an alternative embodiment. In this case the p-type layer will accumulate the surface or the backside of the p-type silicon layer and p-type sidewalls.

Other possible passivation techniques include a hot steam anneal of hydrogenated
5 silicon nitride or the use of amorphous silicon.

Aluminum oxide can also be deposited in the trench to form an isolating barrier. Aluminum oxide can have low stress, a negative fixed charge and higher index of refraction than silicon oxide or low stress silicon oxynitride nitride. Low surface recombination velocities, as low as 10 cm/s can be obtained through various deposition
10 processes of Al_2O_3 layers on the silicon substrate. Low surface recombination can be achieved by field induced surface passivation due to a high density of negative charges stored at the interface. PECVD aluminum oxide is described here for the backside passivation of the backside and backside trenches in backside illuminated image sensors.

The index of refraction of the aluminum oxide can be increased slightly as
15 required by the addition of other metallic elements to make ternary insulators like Aluminum Oxynitride (AlON), Hafnium Aluminum Oxide (HfAlO), Zirconium Aluminum Oxide (ZrAlO), Lanthanum Aluminum Oxide (LaAlO), Titanium Aluminum Oxide (TiAlO) or quaternary dielectrics like Hafnium Aluminum Oxynitride (HfAlON), Tantalum Aluminum Oxynitride (TaAlON),
20 (LaAlON).

Low temperature PECVD deposition processes are contemplated for the backside passivation of the backside and backside trenches in backside illuminated image sensors. As previously mentioned the large index of refraction mismatch between silicon and the insulators in the trenches results in reflection of the incident light and provides optical
25 isolation. The trenches also provide electrical isolation. Additionally, it can also be beneficial to dope the sidewalls to create a surface field that will improve electrical isolation between the pixels. In one aspect, it can also be beneficial to dope the low refractive index material of the Bragg-type reflectors to increase such electrical isolation.

Returning to FIG. 2, layers the silicon oxide and polysilicon can optically and
30 electrically isolate the adjacent pixels, as well as function to trap light within the pixel. While any thicknesses capable of forming such a reflector are considered to be within the

present scope, layer 216 can have a thickness in the range of from about 50 nm to about 500 nm. Layer 118 can have a thickness in the range of from about 5 nm to about 100 nm. Thus, the difference in refractive indexes and thickness can determine the intensity of the internal reflection of electromagnetic radiation. Notably, other materials such as metals, as well as other material not listed herein can be used to increase internal reflection of the light.

It is noted that, for the purposes of the present disclosure, in one aspect a low refractive index material can have a refractive index of less than about 2.1. In the case of the sandwiched materials, the two low refractive index materials can be the same or different materials having a refractive index of less than about 2.1. Non-limiting examples of low refractive index materials can include oxides, nitrides, oxynitrides, gasses, at least a partial vacuums, and the like, including appropriate combinations thereof. Non-limiting specific examples of such materials can include silicon oxide, silicon nitride, silicon oxynitride, and the like, including combinations thereof.

Additionally, a high K dielectric material can also make a suitable low reflective index material due to their low refractive index properties and good dielectric properties, and as such, are considered to be within the present scope. One example is Hafnium oxide, which has a refractive index of about 1.9. Other examples of high K dielectrics include hafnium silicate, zirconium silicate, zirconium dioxide, and the like.

Additionally, in another aspect a high refractive index material can include a material having a refractive index of greater than or equal to about 2.1. Thus, in the case of the sandwiched materials, the high refractive index material disposed between the low refractive index materials has a refractive index of about 2.1 or greater. Non-limiting examples of high refractive index materials can include polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and the like, including appropriate combinations thereof.

In still another aspect of the present disclosure, a photosensitive imager having at least two pixels (302 and 304) and at least one trench isolation region 314 is shown in FIG. 3. The pixels can include a semiconductor substrate 306, having a first and second surface, 320 and 322 respectively; at least two doped regions 308 and 310, and a textured region 312 formed at least on the opposite side of the light incident surface (i.e. the

second side 322). The textured region 312 can have surface features configured to reflect and disperse light. Further, the sidewalls can include a texture region 312 to increase the internal reflections of light. Regarding the isolation element 314 in FIG. 3, the isolation element can include several layers of materials that can passivate the sidewalls and each have a different index of refraction, as was described in FIG. 2. Further, a textured region 312 can be formed on the side walls of the isolation element(s) 314.

The present disclosure additionally provides pixels and imager devices, including imager arrays, which trap light therewithin. In one aspect as is shown in FIG. 4, for example, a light trapping pixel device can include a light sensitive pixel or device 402 having a light incident surface 420, a backside surface 422 opposite the light incident surface 420, and a peripheral sidewall 424 disposed into at least a portion of the pixel 402 and extending at least substantially around the pixel periphery. It is noted that the pixel sidewall is also known as a trench. The pixel can also include a backside light trapping material 426 substantially covering, partially covering, or completely covering the backside surface 422. A peripheral light trapping material 428 can be substantially covering, partially covering, or completely covering the peripheral sidewall 424. As such, light contacting the backside light trapping material 426 or the peripheral light trapping material 428 is reflected back toward the pixel 402. Also shown in FIG. 4 are at least two doped regions 408 and 410 and an optional textured region 412. It is noted that, in addition to a single pixel as shown, pixel arrays are also contemplated and are to be included in the present scope.

The light trapping materials of FIG. 4 can be as described above, either single or multiple layer structures. In one aspect, for example, at least one of the backside light trapping material 426 and the peripheral light trapping material 428 includes a high refractive index material sandwiched between two low refractive index materials. In another aspect, the backside light trapping material 426 and the peripheral light trapping material 428 includes a high refractive index material sandwiched between two low refractive index materials. It is noted that these light trapping materials are shown in FIG. 4 as a single layer for clarity, and that multiple layers are contemplated. Furthermore, the peripheral sidewall can extend for a portion, a substantial portion, or completely around the pixel periphery. Additionally, as has been described herein, the

peripheral sidewall can extend partially into the pixel, substantially through the pixel, or completely through the pixel to the backside surface. Thus, both deep and shallow trenches are contemplated.

In another aspect, as is shown in FIG. 5, a pixel 502 can include a frontside light trapping material 530 that at least partially covers, substantially covers, or completely covers the light incident surface 520. The frontside light trapping material 530 can be multiple layer of materials have a variety of properties and uses, including passivation, antireflection, light trapping, and the like, including combinations thereof. Note that numerical indicators in FIG. 5 from previous figures are intended to reflect the previous descriptions for those elements, and as such, reference is made to FIG. 4.

In another aspect, as is shown in FIG. 6, a pixel 602 can include a frontside light trapping material 632 associated with the light incident surface 620 that is an internal reflective layer having an aperture 634 to allow entry of light 690 into the pixel 602. The frontside light trapping material 632 is thus operable to reflect light impinging thereupon from inside the pixel 602 back into the pixel. Additionally, in some aspects a lens 636 can be functionally coupled to the aperture 634 to focus incident light 690 through the aperture 634 and into the pixel 602. The effective surface area of the aperture compared to the frontside surface area of the pixel can vary depending on the design of the device and the presence, absence, or particular properties of a lens. In one aspect, however, the aperture can be large enough to accept and trap incoming light to a degree that increases the efficiency of the pixel. In one specific aspect, the aperture has an effective surface area of less than about 90% of the incident light surface total surface area. It is noted that various elements such as the doped regions and the optional textured layer are not shown in FIG. 6 for clarity. Furthermore, numerical indicators in FIG. 6 from previous figures are intended to reflect the previous descriptions for those elements, and as such, reference is made to FIG. 4.

The frontside light trapping material can be made of a variety of materials including metals as have been described herein with respect to other light trapping materials. As such, any material that can be applied to the light incident surface and that is internally reflective toward the inside of the pixel is considered to be within the present scope. Thus, the aforementioned pixel is reflective on 6 internal sides, and as such, light

entering the pixel that is not absorbed will interact with and be reflected internally be either the backside, peripheral sidewall, or frontside light trapping materials. Light is thus effectively maintained inside the pixel until it is absorbed.

In another aspect of the present disclosure, a method of making a light trapping pixel device is provided. Such a method can include, as is shown in FIG. 7, 702 forming a pixel by: 704 forming a backside light trapping material on a semiconductor layer, the backside light trapping material including a high refractive index material sandwiched between two low refractive index materials, and 706 forming a pixel device layer on the semiconductor layer opposite the light trapping material. The method can additionally include 708 etching a trench circumscribing the pixel device layer and 710 filling the trench with a light trapping material. Further details regarding the wafer bonding and wafer-bonded structures described can be found in copending US Application Serial No. 13/069,135, filed on March 22, 2011, which is incorporated herein by reference.

The formation of the backside light trapping material can be accomplished by a variety of techniques, all of which are considered to be within the present scope. In one aspect, for example, depositing a first low refractive index material onto the semiconductor layer, bonding the first low refractive index material to a high refractive index material having a second low refractive index material coupled thereto such that the high refractive index material is sandwiched in between the first and second low refractive index materials. In some cases the second low refractive index material can be coupled to a carrier wafer. In another aspect, the first low refractive index can be deposited onto the semiconductor layer followed by deposition of the high refractive index material and then the second low refractive index material. In another aspect, the layered structure can be formed on a carrier wafer, and the outermost low refractive index material can then be bonded to the semiconductor layer. The carrier wafer can then be optionally removed. In yet another aspect, the first refractive index material can be deposited onto the semiconductor layer, the second refractive index material can be deposited onto a carrier wafer, and the high refractive index material can be deposited onto either the first or second refractive index material, followed by bonding of the structure together.

As has been described, the trench can be a shallow trench or a deep trench. In one aspect, however, etching the trench circumscribing the pixel device layer can further include etching the trench to a depth that contacts at least the first low refractive index material. Furthermore, the method can also include applying an incident light trapping material to the pixel device layer.

In some aspects the various trenches can be filled with a material, or they can be gas filled or have a partial vacuum applied thereto. For those aspects whereby the trenches will be filled in with a non-gas material, a variety of deposition techniques are contemplated and all are considered to be within the present scope. In one aspect, however, the trench can be filled with a high refractive index material and a low refractive index material in a sandwich structure as has been described. In one exemplary technique, the filling of the trench with such light trapping material can include depositing a low refractive index material into the trench to fill a portion of the trench from the trench walls inward, ceasing deposition of the low refractive index material to leave an internal space within the trench, and depositing a high refractive index material into the trench to fill the internal space. As such, the sandwiched layer of low-high-low refractive index materials is thus created in the trench.

In another aspect, the method can also include forming a textured region on at least a portion of the semiconductor layer between the semiconductor layer and the first low refractive index prior to depositing the first low refractive index material onto the semiconductor layer. Non-limiting examples of texture formation techniques can include plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof. In one specific aspect, the textured region includes laser texturing.

A device design having a textured region located on, for example, the back surface of a photodetector, provides significant performance benefits. The textured region can have surface features that can lead to higher recombination of photocarriers for short wavelengths (e.g. in the blue green part of the spectrum) due to the very shallow penetration of those wavelengths into the detecting volume of the device. By physically locating the textured on the back surface of the device, a pristine surface is provided for the collection of short wavelengths on the top surface (i.e. the light incident surface), and

the longer wavelengths that penetrate deep into or through the detecting region of the semiconductor material are collected by or with the help of the textured region opposite the light incident surface.

The textured region can be of various thicknesses, depending on the desired use of the material. In one aspect, for example, the textured region has a thickness of from about 500 nm to about 100 μm . In another aspect, the textured region has a thickness of from about 500 nm to about 15 μm . In yet another aspect, the textured region has a thickness of from about 500 nm to about 2 μm . In a further aspect, the textured region has a thickness of from about 500 nm to about 1 μm . In another aspect, the textured region has a thickness of from about 200 nm to about 2 μm .

The textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and/or to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device. The textured region can include surface features to further increase the effective absorption length of the device. Non-limiting examples of shapes and configurations of surface features include cones, pillars, pyramids, microlenses, quantum dots, inverted features, gratings, protrusions, sphere-like structures, and the like, including combinations thereof. Additionally, surface features can be micron-sized, nano-sized, or a combination thereof. For example, cones, pyramids, protrusions, and the like can have an average height within this range. In one aspect, the average height would be from the base of the feature to the distal tip of the feature. In another aspect, the average height would be from the surface plane upon which the feature was created to the distal tips of the feature. In one specific aspect, a feature (e.g. a cone) can have a height of from about 50 nm to about 2 μm . As another example, quantum dots, microlenses, and the like can have an average diameter within the micron-sized and/or nano-sized range.

In addition to or instead of surface features, the textured region can include a textured film layer. In one aspect, for example, the textured region can include a substantially conformal textured film layer. Such a textured film layer can have an average thickness of from about 1 nm to about 20 μm . In those aspects where the textured region includes surface features, the conformal textured film layer can have a varying thickness relative to the location on the surface features upon which is deposited.

In the case of cones, for example, the conformal textured film layer can become thinner toward the tips of the cones. Such a conformal film layer can include various materials, including, without limitation, SiO₂, Si₃N₄, amorphous silicon, polysilicon, a metal or metals, and the like, including combinations thereof. The conformal textured film layer
5 can also be one or more layers of the same or different materials, and can be formed during the creation of surface features or in a separate process.

Textured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared). Such internal
10 reflection increases the effective absorption length to be greater than the thickness of the semiconductor layer. This increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.

The texturing process can texture the entire substrate to be processed or only a portion of the substrate. In one aspect, for example, a substrate such as the
15 semiconductor layer can be textured and patterned by an appropriate technique over an entire surface to form the texture region. In another aspect, a substrate such as the semiconductor layer can be textured and patterned across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch or a laser process to define a specific structure or pattern.

In addition to surface features, the textured region can have a surface morphology that is designed to focus or otherwise direct electromagnetic radiation. For example, in
20 one aspect the textured region has a surface morphology operable to direct electromagnetic radiation into the semiconductor layer. Non-limiting examples of various surface morphologies include sloping, pyramidal, inverted pyramidal, spherical,
25 square, rectangular, parabolic, asymmetric, symmetric, and the like, including combinations thereof.

The textured region, including surface features as well as surface morphologies, can be formed by various techniques, including plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching (e.g. anisotropic etching, isotropic
30 etching), nanoimprinting, material deposition, selective epitaxial growth, and the like.

One effective method of producing a textured region is through laser processing. Such laser processing allows discrete target areas of a substrate to be textured, as well as entire surfaces. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope. Laser treatment or processing can allow, among other things, enhanced absorption properties and thus increased electromagnetic radiation focusing and detection.

In one aspect, for example, a target region of the substrate to be textured can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Patents 7,057,256, 7,354,792 and 7,442,629, which are incorporated herein by reference in their entireties. Briefly, a surface of a substrate material is irradiated with laser radiation to form a textured or surface modified region. Such laser processing can occur with or without a dopant material. In those aspects whereby a dopant is used, the laser can be passed through a dopant carrier and onto the substrate surface. In this way, dopant from the dopant carrier is introduced into the target region of the substrate material. Such a region incorporated into a substrate material can have various benefits in accordance with aspects of the present disclosure. For example, the textured region typically has a textured surface that increases the surface area and increases the probability of radiation absorption. In one aspect, such a textured region is a substantially textured surface including micron-sized and/or nano-sized surface features that have been generated by the laser texturing. In another aspect, irradiating the surface of a substrate material includes exposing the laser radiation to a dopant such that irradiation incorporates the dopant into the substrate. Various dopant materials are known in the art, and are discussed in more detail herein.

Thus the surface of the substrate at the target region is thus chemically and/or structurally altered by the laser treatment, which may, in some aspects, result in the formation of surface features appearing as structures or patterned areas on the surface and, if a dopant is used, the incorporation of such dopants into the substrate material. In some aspects, the features or structures can be on the order of 50 nm to 20 μ m in size and can assist in the absorption of electromagnetic radiation. In other words, the textured surface can increase the probability of incident radiation being absorbed.

A variety of semiconductor materials are contemplated for use with the pixel devices and methods according to aspects of the present disclosure. Such materials can be utilized as the semiconductor layer and/or the semiconductor substrate, as well as for the secondary semiconductor layer and the epitaxially grown semiconductor layer. Non-limiting examples of such semiconductor materials can include group IV materials, compounds and alloys comprised of materials from groups II and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can include silicon carbide (SiC) and silicon germanium (SiGe). In one specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum gallium arsenide, and combinations thereof.

Exemplary combinations of group II-VI materials can include cadmium selenide (CdSe), cadmium sulfide (CdS), cadmium telluride (CdTe), zinc oxide (ZnO), zinc selenide (ZnSe), zinc sulfide (ZnS), zinc telluride (ZnTe), cadmium zinc telluride (CdZnTe, CZT), mercury cadmium telluride (HgCdTe), mercury zinc telluride (HgZnTe), mercury zinc selenide (HgZnSe), and combinations thereof.

Exemplary combinations of group III-V materials can include aluminum antimonide (AlSb), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum phosphide (AlP), boron nitride (BN), boron phosphide (BP), boron arsenide (BAs), gallium antimonide (GaSb), gallium arsenide (GaAs), gallium nitride (GaN), gallium phosphide (GaP), indium antimonide (InSb), indium arsenide (InAs), indium nitride (InN), indium phosphide (InP), aluminum gallium arsenide (AlGaAs, $\text{Al}_x\text{Ga}_{1-x}\text{As}$), indium gallium arsenide (InGaAs, $\text{In}_x\text{Ga}_{1-x}\text{As}$), indium gallium phosphide (InGaP), aluminum indium arsenide (AlInAs), aluminum indium antimonide (AlInSb), gallium arsenide nitride (GaAsN), gallium arsenide phosphide (GaAsP), aluminum gallium nitride (AlGaN), aluminum gallium phosphide (AlGaP), indium gallium nitride (InGaN),

indium arsenide antimonide (InAsSb), indium gallium antimonide (InGaSb), aluminum gallium indium phosphide (AlGaInP), aluminum gallium arsenide phosphide (AlGaAsP), indium gallium arsenide phosphide (InGaAsP), aluminum indium arsenide phosphide (AlInAsP), aluminum gallium arsenide nitride (AlGaAsN), indium gallium arsenide nitride (InGaAsN), indium aluminum arsenide nitride (InAlAsN), gallium arsenide antimonide nitride (GaAsSbN), gallium indium nitride arsenide antimonide (GaInNAsSb), gallium indium arsenide antimonide phosphide (GaInAsSbP), and combinations thereof.

The semiconductor material can be of any thickness that allows the desired property or functionality of the semiconductor device, and thus any such thickness of semiconductor material is considered to be within the present scope. The textured region can increase the efficiency of the device such that, in some aspects, the semiconductor material can be thinner than has previously been possible. Decreasing the thickness reduces the amount of semiconductor material used to make such a device. In one aspect, for example, a semiconductor material such as the semiconductor layer has a thickness of from about 500 nm to about 50 μm . In another aspect, the semiconductor material has a thickness of less than or equal to about 500 μm . In yet another aspect, the semiconductor material has a thickness of from about 1 μm to about 10 μm . In a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 750 μm . In yet a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 100 μm .

Additionally, various configurations of semiconductor materials are contemplated, and any such material configuration that can be incorporated into a semiconductor device is considered to be within the present scope. In one aspect, for example, the semiconductor material can include monocrystalline materials. In another aspect, the semiconductor material can include multicrystalline materials. In yet another aspect, the semiconductor material can include microcrystalline materials. It is also contemplated that the semiconductor material can include amorphous materials.

As has been described, the semiconductor substrate can be of any size, shape, and material capable of supporting the semiconductor layer and associated components during manufacture and/or use. The semiconductor substrate can be made from various

materials, including the semiconductor materials described above, as well as non-semiconductor materials. Non-limiting examples of such materials can include metals, polymeric materials, ceramics, glass, and the like. In some aspects, the semiconductor substrate and the semiconductor layer have the same or substantially the same thermal expansion properties.

Furthermore, the semiconductor material according to aspects of the present disclosure can comprise multiple layers. In some aspects, layers can vary in majority carrier polarity (i.e. donor or acceptor impurities). The donor or acceptor impurities are typically determined by the type of dopant/impurities introduced into the device either through a growth process, deposition process, epitaxial process, implant process, lasing process or other known process to those skilled in the art. In some aspects such semiconductor materials can include an n-type layer, an intrinsic (i-type) layer, and a p-type layer, thus forming a p-i-n semiconductor material stack that creates a junction and/or depletion region. A semiconductor material devoid of an i-type layer is also contemplated in accordance with the present disclosure. In other aspects the semiconductor material may include multiple junctions. Additionally, in some aspects, variations of n(--), n(-), n(+), n(++), p(--), p(-), p(+), or p(++) type semiconductor layers can be used. The minus and positive signs are indicators of the relative magnitude of the doping of the semiconductor material.

A variety of dopant materials are contemplated for both the formation of doped regions in the semiconductor layer and for doping of the textured region, and any dopant that can be used in such processes to modify a material is considered to be within the present scope. It should be noted that the particular dopant utilized can vary depending on the material being doped, as well as the intended use of the resulting material.

A dopant can be either a charge donating or a charge accepting dopant species. More specifically, an electron donating or a hole donating species can cause a region to become more positive or negative in polarity as compared to the substrate upon which the rests. In one aspect, for example, the doped region can be p-doped. In another aspect the doped region can be n-doped.

In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof. It should be noted that the

scope of dopant materials should include, not only the dopant materials themselves, but also materials in forms that deliver such dopants (i.e. dopant carriers). For example, S dopant materials includes not only S, but also any material capable being used to dope S into the target region, such as, for example, H₂S, SF₆, SO₂, and the like, including combinations thereof. In one specific aspect, the dopant can be S. Sulfur can be present at an ion dosage level of from about 5×10^{14} to about 3×10^{20} ions/cm². Non-limiting examples of fluorine-containing compounds can include ClF₃, PF₅, F₂ SF₆, BF₃, GeF₄, WF₆, SiF₄, HF, CF₄, CHF₃, CH₂F₂, CH₃F, C₂F₆, C₂HF₅, C₃F₈, C₄F₈, NF₃, and the like, including combinations thereof. Non-limiting examples of boron-containing compounds can include B(CH₃)₃, BF₃, BCl₃, BN, C₂B₁₀H₁₂, borosilica, B₂H₆, and the like, including combinations thereof. Non-limiting examples of phosphorous-containing compounds can include PF₅, PH₃, POCl₃, P₂O₅, and the like, including combinations thereof. Non-limiting examples of chlorine-containing compounds can include Cl₂, SiH₂Cl₂, HCl, SiCl₄, and the like, including combinations thereof. Dopants can also include arsenic-containing compounds such as AsH₃ and the like, as well as antimony-containing compounds. Additionally, dopant materials can include mixtures or combinations across dopant groups, i.e. a sulfur-containing compound mixed with a chlorine-containing compound. In one aspect, the dopant material can have a density that is greater than air. In one specific aspect, the dopant material can include Se, H₂S, SF₆, or mixtures thereof. In yet another specific aspect, the dopant can be SF₆ and can have a predetermined concentration range of about 5.0×10^{-8} mol/cm³ to about 5.0×10^{-4} mol/cm³. As one non-limiting example, SF₆ gas is a good carrier for the incorporation of sulfur into a substrate via a laser process without significant adverse effects on the material. Additionally, it is noted that dopants can also be liquid solutions of n-type or p-type dopant materials dissolved in a solution such as water, alcohol, or an acid or basic solution. Dopants can also be solid materials applied as a powder or as a suspension dried onto the wafer.

In another aspect, the band structure optimization can be realized by forming a heterojunction along a modified semiconductor interface. For example, a layer of amorphous silicon can be deposited on the textured region interface, thus forming a heterojunction that bends the minority carrier band towards the desired energy direction.

CLAIMS

What is claimed is:

- 5 1. A light trapping device, comprising:
at least one light sensitive pixel having a light incident surface, a backside surface
opposite the light incident surface, and a peripheral sidewall disposed into at least a
portion of the pixel and extending at least substantially around the pixel periphery;
a backside light trapping material substantially covering the backside surface; and
10 a peripheral light trapping material substantially covering the peripheral sidewall;
wherein light contacting the backside light trapping material or the peripheral
light trapping material is reflected back toward the pixel.
2. The device of claim 1, wherein at least one of the backside light trapping material and
15 the peripheral light trapping material includes a high refractive index material
sandwiched between two low refractive index materials.
3. The device of claim 1, wherein the backside light trapping material and the peripheral
light trapping material includes a high refractive index material sandwiched between two
20 low refractive index materials.
4. The device of claim 3, wherein the two low refractive index materials have a
refractive index of less than about 2.1.
- 25 5. The device of claim 4, wherein at least one of the two low refractive index material
includes a member selected from the group consisting of an oxide, a nitride, oxynitrides,
a gas, at least a partial vacuum, and combinations thereof.
6. The device of claim 4, wherein the at least one of the two low refractive index
30 materials includes a member selected from the group consisting of silicon oxide, silicon
nitride, silicon dioxide, and combinations thereof.

7. The device of claim 3, wherein the high refractive index material includes a material having a refractive index of greater than or equal to about 2.1.
- 5 8. The device of claim 7, wherein the high refractive index material includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and combinations thereof.
- 10 9. The device of claim 2, wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field.
10. The device of claim 9, wherein the dopant is boron or antimony.
- 15 11. The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials, and wherein the difference in refractive index between the first material and the two second materials is at least 0.2.
- 20 12. The device of claim 1, wherein the peripheral sidewall extends completely around the pixel periphery.
13. The device of claim 1, wherein the peripheral sidewall extends from the light
25 incident surface to the backside surface.
14. The device of claim 1, further comprising a frontside light trapping material at least partially covering the light incident surface.
- 30 15. The device of claim 14, wherein the frontside light trapping material is an antireflective layer coating.

16. The device of claim 14, wherein the frontside light trapping material is a reflective layer having an aperture to allow entry of light into the pixel, wherein the reflective layer is operable to reflect light impinging thereupon from inside the pixel back into the pixel.

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17. The device of claim 16, further comprising a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.

18. The device of claim 16, wherein the aperture has an effective surface area of 90% of the incident light surface total surface area.

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19. The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

20. The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface.

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21. The device of claim 1, further comprising a textured layer positioned to interact with light proximal to the backside surface.

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22. The device of claim 21, wherein the textured layer is located between the backside surface and the backside light trapping material.

23. An array of light trapping pixel devices of claim 1.

25

24. A substantially light trapping device, comprising:

at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending from the light incident surface to the backside surface and extending around the pixel periphery;
a backside light trapping material substantially covering the backside surface;

30

a peripheral light trapping material substantially covering the peripheral sidewall;
and

an internally reflective frontside light trapping material covering at least a portion
of the light incident surface operable allow entrance of light into the pixel and operable to
5 reflect light impinging thereupon from inside the pixel back into the pixel, and wherein
light contacting the backside light trapping material or the peripheral light trapping
material is reflected back toward the pixel.

25. The device of claim 24, wherein the internally reflective frontside light trapping
10 material includes an aperture to allow entry of light into the pixel.

26. The device of claim 25, further comprising a lens functionally coupled to the
aperture and operable to focus incident light through the aperture and into the pixel.

15 27. A method of making a light trapping device, comprising:

forming a pixel by:

forming a backside light trapping material on a semiconductor
layer, the backside light trapping material including a high refractive index
material sandwiched between two low refractive index materials; and

20 forming a pixel device layer on the semiconductor layer opposite
the light trapping material;

etching a trench circumscribing the pixel device layer; and
filling the trench with a peripheral light trapping material.

25 28. The method of claim 27, wherein etching the trench circumscribing the pixel device
layer can further include etching the trench to a depth that contacts at least the backside
light trapping material.

29. The method of claim 27, further comprising applying an incident light trapping
30 material to the pixel device layer.

30. The method of claim 27, wherein filling the trench with the peripheral light trapping material further includes:

depositing a low refractive index material into the trench to fill a portion of the trench from the trench walls inward;

5 ceasing deposition of the low refractive index material to leave an internal space within the trench; and

depositing a high refractive index material into the trench to fill the internal space.

31. The method of claim 27, further comprising forming a textured region on at least a
10 portion of the semiconductor layer between the semiconductor layer and the backside light trapping material.

32. The method of claim 31, wherein forming the textured region includes a technique selected from the group consisting of plasma etching, reactive ion etching, porous silicon
15 etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.

33. The method of claim 32, wherein forming the textured region includes laser texturing.

20

25

ABSTRACT OF THE DISCLOSURE

Light trapping pixels, devices incorporating such pixels, and various associated methods are provided. In one aspect, for example, a light trapping pixel device can include a light sensitive pixel having a light incident surface, a backside surface opposite
5 the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery. The pixel can also include a backside light trapping material substantially covering the backside surface and a peripheral light trapping material substantially covering the peripheral sidewall. The light contacting the backside light trapping material or the peripheral light trapping
10 material is thus reflected back toward the pixel.

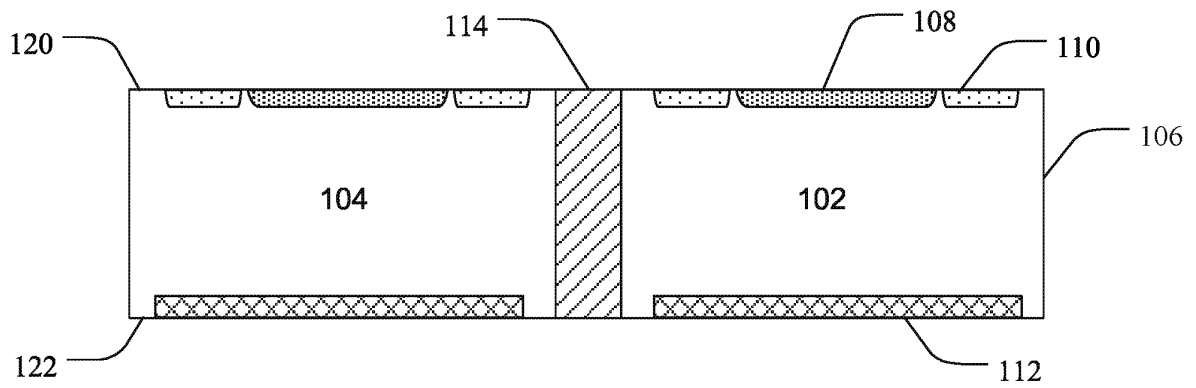


FIG. 1

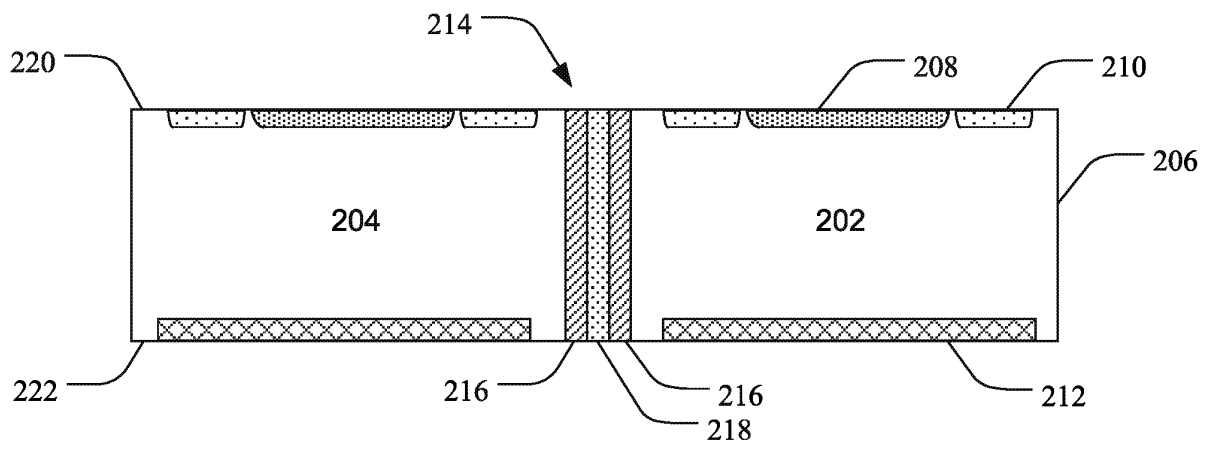


FIG. 2

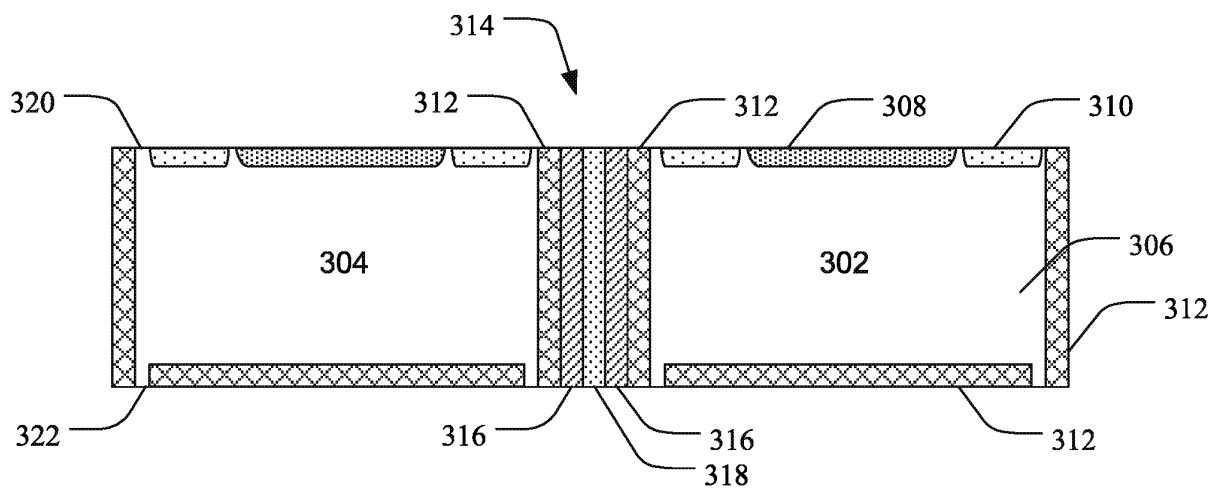


FIG. 3

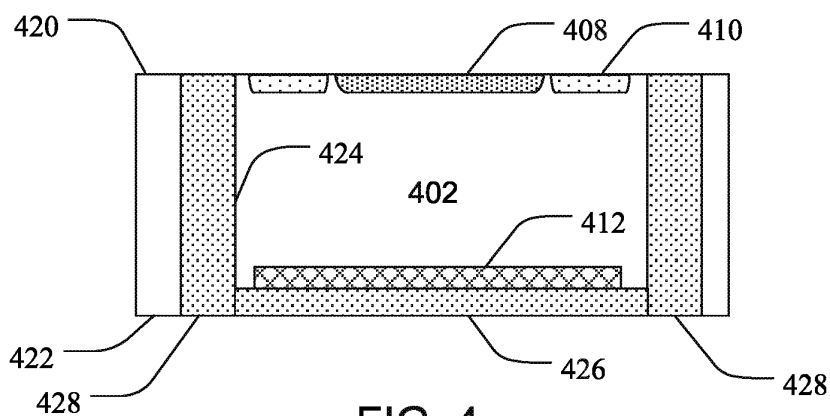


FIG. 4

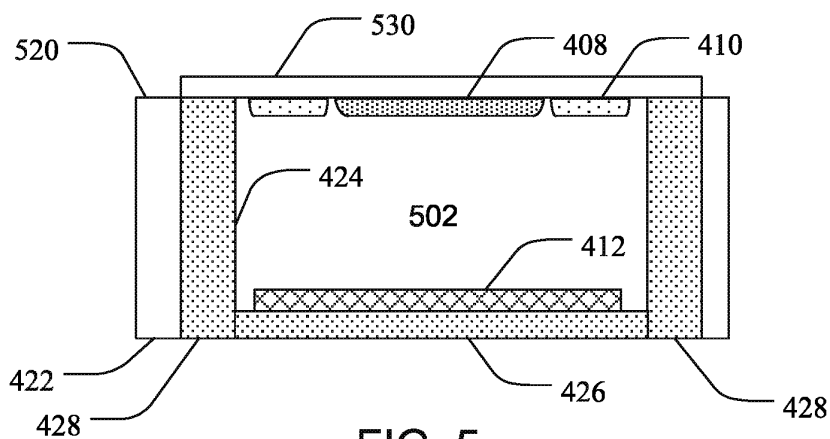


FIG. 5

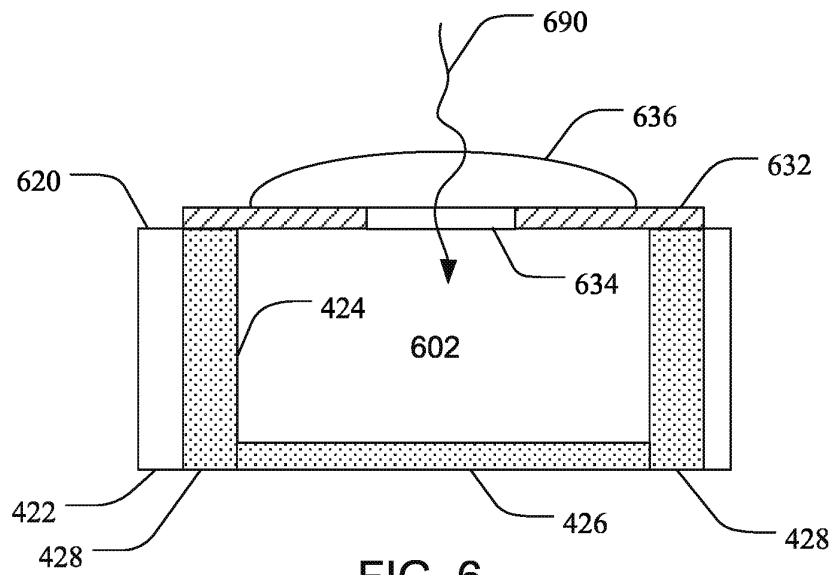


FIG. 6

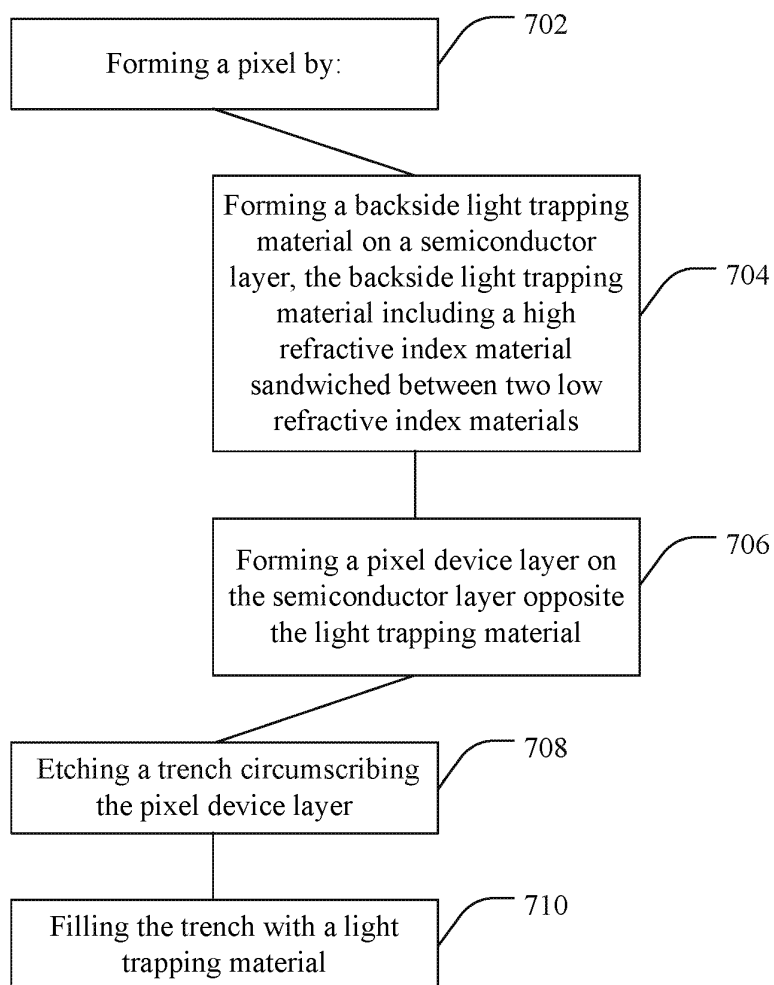


FIG. 7

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING
AN APPLICATION DATA SHEET (37 CFR 1.76)****Title of
Invention**

Pixel Isolation Elements, Devices and Associated Methods

As the below named inventor, I hereby declare that:

This declaration
is directed to:

The attached application or,

United States application or PCT international application number 13/841,120filed on 3/15/2013.

The above-identified application was made or authorized to be made by me.

I have reviewed and understand the contents of the above-identified application, including the claims. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

LEGAL NAME OF INVENTOR

Inventor: Martin U. Pralle

Date (Optional):

4/3/14Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING
AN APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	<i>Pixel Isolation Elements, Devices and Associated Methods</i>
-------------------------------	---

As the below named inventor, I hereby declare that:

This declaration
is directed to:☐

The attached application or,

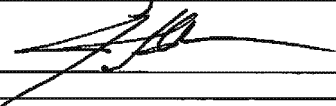
☒United States application or PCT international application number 13/841,120filed on 3/15/2013

The above-identified application was made or authorized to be made by me.

I have reviewed and understand the contents of the above-identified application, including the claims. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

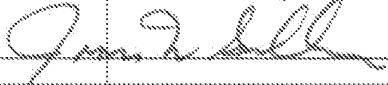
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LEGAL NAME OF INVENTORInventor: Jeffrey McKee Date (Optional): 4-7-14Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING
AN APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	Pixel Isolation Elements, Devices and Associated Methods	
As the below named inventor, I hereby declare that: This declaration is directed to: ☐ The attached application or, ☒ United States application or PCT international application number <u>13/841,120</u> filed on <u>3/15/2013</u> The above-identified application was made or authorized to be made by me. I have reviewed and understand the contents of the above-identified application, including the claims. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.		
LEGAL NAME OF INVENTOR		
Inventor: <u>Jason Sickler</u> Date (Optional): <u>4/3/2014</u>		
Signature: 		
Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.		

SCORE Placeholder Sheet for IFW Content

Application Number: 17214333

Document Date: 03/26/2021

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 17/214,333			
APPLICATION AS FILED - PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	700		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800		
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 = *				x 100 =	0.00		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *				x 480 =	0.00		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00		
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	1820		
APPLICATION AS AMENDED - PART II									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =		
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =		
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
				TOTAL ADD'L FEE		TOTAL ADD'L FEE			
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =		
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =		
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
				TOTAL ADD'L FEE		TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.									



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
17/214,333	03/26/2021	2852	1820	SXM-052CN4	20	1

CONFIRMATION NO. 1018

FILING RECEIPT



CC000000124624289

959

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BOSTON, MA 02111

Date Mailed: 04/06/2021

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

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Inventor(s)

Martin U. Pralle, Wayland, MA;
Jeffrey McKee, Tualatin, OR;
Jason Sickler, Arlington, MA;

Applicant(s)

SiOnyx LLC, Beverly, MA;

Power of Attorney: The patent practitioners associated with Customer Number 00959

Domestic Priority data as claimed by applicant

This application is a CON of 16/290,740 03/01/2019 PAT 10985198
which is a CON of 15/216,244 07/21/2016 PAT 10224359
which is a CON of 14/747,875 06/23/2015 PAT 9905599
which is a CON of 13/841,120 03/15/2013 PAT 9064764
which claims benefit of 61/614,275 03/22/2012

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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Permission to Access Search Results: Yes

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/214,333**

Projected Publication Date: 07/15/2021

Non-Publication Request: No

Early Publication Request: No

Title

PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS

Preliminary Class

396

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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page 2 of 4

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Application	Document	Mailroom Date	Attorney Docket No.
17214333	APP.FILE.REC	04/06/2021	SXM-052CN4

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/214,333	03/26/2021	Martin U. Pralle	SXM-052CN4

CONFIRMATION NO. 1018

PUBLICATION NOTICE



OC000000127001194

959

NELSON MULLINS RILEY & SCARBOROUGH LLP
ONE FINANCIAL CENTER
SUITE 3500
BOSTON, MA 02111

Title:PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS

Publication No.US-2021-0217788-A1

Publication Date:07/15/2021

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Application	Document	Mailroom Date	Attorney Docket No.
17214333	NTC.PUB	07/15/2021	SXM-052CN4

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/214,333	03/26/2021	Martin U. Pralle	SXM-052CN4	1018
959 7590 07/11/2022 NELSON MULLINS RILEY & SCARBOROUGH LLP ONE FINANCIAL CENTER SUITE 3500 BOSTON, MA 02111			EXAMINER PHAM, LONG	
			ART UNIT	PAPER NUMBER
			2814	
			NOTIFICATION DATE	DELIVERY MODE
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DETAILED ACTION

Election/Restrictions

This application contains claims directed to the following patentably distinct species: embodiment or species 1 of fig. 1, embodiment or species 2 of fig. 2, embodiment or species 3 of fig. 3, embodiment or species 4 of fig. 4, embodiment or species 5 of fig. 5, embodiment or species 6 of fig. 6, embodiment or species 7 of fig. 7. The species are independent or distinct because **the patentability or unpatentability of one species does not necessarily imply the patentability or unpatentability of another species**. In addition, these species are not obvious variants of each other based on the current record.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species, or a single grouping of patentably indistinct species, for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no independent claim appears to be generic to other independent claims.

There is a search and/or examination burden for the patentably distinct species as set forth above because at least the following reason(s) apply: **The searches of the patentably distinct species are not co-extensive.**

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected species or grouping of patentably**

indistinct species, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species or grouping of patentably indistinct species.

Should applicant traverse on the ground that the species, or groupings of patentably indistinct species from which election is required, are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing them to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141. A telephone call was made to -- on -- to request an oral election to the above restriction requirement, but did not result in an election being made.

The examiner has required restriction between product or apparatus claims and process claims. Where applicant elects claims directed to the product/apparatus, and all product/apparatus claims are subsequently found allowable, withdrawn process claims that include all the limitations of the allowable product/apparatus claims should be considered for rejoinder. All claims directed to a nonelected process invention must include all the limitations of an allowable product/apparatus claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product/apparatus claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product/apparatus are found allowable, an otherwise proper restriction requirement between product/apparatus claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product/apparatus claim will not be rejoined. See MPEP § 821.04. Additionally, in order for rejoinder to occur, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product/apparatus claims. **Failure to do so may result in no rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

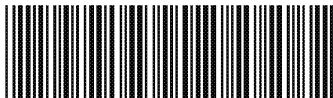
Any inquiry concerning this communication or earlier communications from the examiner should be directed to LONG PHAM whose telephone number is (571)272-1714. The examiner can normally be reached on Mon-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LONG . PHAM
Examiner
Art Unit 2814

/LONG PHAM/
Primary Examiner, Art Unit 2814

<i>Index of Claims</i> 	Application/Control No. 17/214,333	Applicant(s)/Patent Under Reexamination Pralle et al.
	Examiner LONG PHAM	Art Unit 2814

✓	Rejected
=	Allowed

-	Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	07/02/2022								
	1	÷								
	2	÷								
	3	÷								
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	14	÷								
	15	÷								
	16	÷								
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	20	÷								

To: ipboston.docketing@nelsonmullins.com,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 959

Jul 11, 2022 04:44:03 AM

Dear PAIR Customer:

NELSON MULLINS RILEY & SCARBOROUGH LLP
ONE FINANCIAL CENTER
SUITE 3500
BOSTON, MA 02111
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 959 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

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Application	Document	Mailroom Date	Attorney Docket No.
17214333	CTRS	07/11/2022	SXM-052CN4

To view your correspondence online or update your email addresses, please visit us anytime at <https://sportal.uspto.gov/secure/myportal/privatepair>.

If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE
PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	17/214,333
Filing Date	March 26, 2021
First Named Inventor	Martin U. Pralle
Title	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS
Art Unit	2814
Examiner Name	PHAM, LONG
Attorney Docket Number	143705.000335

SIGNATURE of Applicant or Patent Practitioner

Signature	/Gunnar G. Leinberg/	Date (Optional)	2022-07-25
Name	Gunnar G. Leinberg	Registration Number	35,584
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.



*Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

11951

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

SIONYX INC.

- ☐ Inventor or Joint Inventor (title not required below)
- ☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)
- ☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)
- ☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

Name

Steven D. Saylor

Title

President and CEO

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☒ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.132, and 1.133. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Electronic Acknowledgement Receipt

EFS ID:	46259821
Application Number:	17214333
International Application Number:	
Confirmation Number:	1018
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	959
Filer:	Gunnar G. Leinberg/Mary Frances Heeks
Filer Authorized By:	Gunnar G. Leinberg
Attorney Docket Number:	SXM-052CN4
Receipt Date:	25-JUL-2022
Filing Date:	26-MAR-2021
Time Stamp:	11:30:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	20220725_POA_with_Transmit tal_143705_000335.pdf	594773 9e966207a0d0a5d29445a09c7eb7aecf7d3 6eaab	no	2

Warnings:

Information:	
Total Files Size (in bytes):	594773
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/214,333	03/26/2021	Martin U. Pralle	SXM-052CN4

959
NELSON MULLINS RILEY & SCARBOROUGH LLP
ONE FINANCIAL CENTER
SUITE 3500
BOSTON, MA 02111

CONFIRMATION NO. 1018
IMPROPER CPOA LETTER



Date Mailed: 07/27/2022

NOTICE REGARDING POWER OF ATTORNEY

This is in response to the power of attorney filed 07/25/2022. The power of attorney in this application is not accepted for the reason(s) listed below:

- The power of attorney has not been accepted because the party who is giving power has not been identified. Power of attorney may only be signed by the applicant for patent (37 CFR 1.42) or the patent owner. A party who is not the applicant must become the applicant in accordance with 37 CFR 1.46(c) and appoint any power of attorney in compliance with 37 CFR 3.71 and 3.73. For a reissue application, reexamination proceeding, or supplemental examination proceeding, a patent owner who was not the applicant under 37 CFR 1.46 must appoint any power of attorney in compliance with 37 CFR 3.71 and 3.73. See 37 CFR 1.32(b)(4).

/snguyen/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

11951
Troutman Pepper Hamilton Sanders LLP (Rochester)
70 Linden Oaks
Suite 210
Rochester, NY 14625
UNITED STATES



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/214,333	03/26/2021	Martin U. Pralle	SXM-052CN4

CONFIRMATION NO. 1018

IMPROPER CFR REQUEST

959

NELSON MULLINS RILEY & SCARBOROUGH LLP
ONE FINANCIAL CENTER
SUITE 3500
BOSTON, MA 02111



Date Mailed: 07/27/2022

RESPONSE TO REQUEST FOR CORRECTED FILING RECEIPT

Power of Attorney, Claims, Fees, System Limitations, and Miscellaneous

In response to your request for a corrected Filing Receipt, the Office is unable to comply with your request because:

- Any request to correct or update the name of the applicant must include an application data sheet (ADS) in compliance with 37 CFR 1.76 specifying the correct or updated name of the applicant in the applicant information section. Any request to change the applicant after an original applicant has been specified under 37 CFR 1.46(b) must include a new ADS in compliance with 37 CFR 1.76 specifying the applicant in the applicant information section and comply with 37 CFR 3.71 and 3.73. See 37 CFR 1.46(c).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/snguyen/

To: ipboston.docketing@nelsonmullins.com,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 959

Jul 27, 2022 05:22:11 AM

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UNITED STATES

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Application	Document	Mailroom Date	Attorney Docket No.
17214333	N572	07/27/2022	SXM-052CN4
	M327	07/27/2022	SXM-052CN4

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NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	17/214,333
Filing Date	March 26, 2021
First Named Inventor	Martin U. Pralle
Title	PIXEL ISOLATION ELEMENTS, DEVICES AND METHODS OF MAKING THE SAME
Art Unit	2814
Examiner Name	PHAM, LONG
Attorney Docket Number	143705.000335

SIGNATURE of Applicant or Patent Practitioner

Signature	/Gunnar G. Leinberg/	Date (Optional)	2022-08-11
Name	Gunnar G. Leinberg	Registration Number	35,584
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.



*Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

11951

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

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☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

SiOnyx, LLC

- ☐ Inventor or Joint Inventor (title not required below)
- ☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)
- ☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)
- ☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

Name

Steven D. Saylor

Title

President and CEO

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☒ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Electronic Acknowledgement Receipt

EFS ID:	46392847
Application Number:	17214333
International Application Number:	
Confirmation Number:	1018
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	959
Filer:	Gunnar G. Leinberg/Mary Frances Heeks
Filer Authorized By:	Gunnar G. Leinberg
Attorney Docket Number:	SXM-052CN4
Receipt Date:	11-AUG-2022
Filing Date:	26-MAR-2021
Time Stamp:	14:55:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	20220811_Corrected_POA_wit h_Transmittal_143705_000335. pdf	328788 1726fadf072e01c22919aa389c8e0f6cac4ec 759	no	2

Warnings:

Information:	
Total Files Size (in bytes):	328788
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	



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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/214,333	03/26/2021	Martin U. Pralle	SXM-052CN4

959
NELSON MULLINS RILEY & SCARBOROUGH LLP
ONE FINANCIAL CENTER
SUITE 3500
BOSTON, MA 02111

CONFIRMATION NO. 1018
POWER OF ATTORNEY NOTICE



Date Mailed: 08/17/2022

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/11/2022.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/sleutchit/



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/214,333	03/26/2021	Martin U. Pralle	143705.000335

CONFIRMATION NO. 1018

POA ACCEPTANCE LETTER



11951
Troutman Pepper Hamilton Sanders LLP (Rochester)
70 Linden Oaks
Suite 210
Rochester, NY 14625

Date Mailed: 08/17/2022

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/11/2022.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/sleutchit/

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From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 11951

Aug 17, 2022 04:33:56 AM

Dear PAIR Customer:

Troutman Pepper Hamilton Sanders LLP (Rochester)
70 Linden Oaks
Suite 210
Rochester, NY 14625
UNITED STATES

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Application	Document	Mailroom Date	Attorney Docket No.
17214333	N570	08/17/2022	143705.000335
	N570	08/17/2022	143705.000335

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PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM



ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
17/214,333

RECEIPT DATE / TIME
09/08/2022 08:42:47 AM ET

ATTORNEY DOCKET #
143705.000335

Title of Invention

PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 1018

FILED BY Mark Jones

PATENT CENTER # 60947744

FILING DATE 03/26/2021

CUSTOMER # 11951

FIRST NAMED INVENTOR Martin U. Pralle

CORRESPONDENCE ADDRESS -

AUTHORIZED BY -

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
143705-000335_Restriction_Response_Election.pdf	6	Response to Election / Restriction Filed	174 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
143705-000335_Restriction_Response_Election.pdf	A1B12A6C00E29F5F90E698031FEBC394836B4FF600C077D80083D42B011A2F58946A85F87F9A87BDECD2A68626EF317846587EB2B97D79B44DF1656F83BE5D45

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Pralle, Martin U., et al.	)	EXAMINER:
	)	PHAM, Long
APPLICATION SERIAL NO.: 17/214,333	)	ART UNIT:
	)	2814
FILED: 26 March 2021	)	CONFIRMATION NO.:
	)	1018
TITLE: PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS	)	ATTY. DOCKET NO.:
	)	143705.000335
	)	

Certificate of E-Filing/Transmission under 37 CFR § 1.8

In accordance with 37 CFR § 1.8, I certify that this correspondence is being deposited and electronically filed with the USPTO via the USPTO's EFS-Web on 8 September 2022.

/Mark Lehi Jones, Reg. 63064/

Mark Lehi Jones, Registration No. 63,064

RESPONSE TO RESTRICTION REQUIREMENT

Mail Stop AMENDMENT
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Atlanta, GA 30308-2216

Sir:

The Restriction Requirement from Primary Examiner Pham of Group Art Unit 2814, dated 10 November 2020, has been received and carefully reviewed.

RESTRICTION

Applicant elects, without traverse, claims 1-20 represented by the species 6 of FIG. 6.

IN THE CLAIMS

1. (Original) A light trapping device, comprising:
 - at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;
 - a backside light trapping material substantially covering the backside surface; and
 - a peripheral light trapping material substantially covering the peripheral sidewall;
 - wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.
2. (Original) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.
3. (Original) The device of claim 1, wherein the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.
4. (Original) The device of claim 3, wherein the two low refractive index materials have a refractive index of less than about 2.1.
5. (Original) The device of claim 4, wherein at least one of the two low refractive index material includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.
6. (Original) The device of claim 4, wherein the at least one of the two low refractive index materials includes a member selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.
7. (Original) The device of claim 3, wherein the high refractive index material includes a material having a refractive index of greater than or equal to about 2.1.

8. (Original) The device of claim 7, wherein the high refractive index material includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and combinations thereof.
9. (Original) The device of claim 2, wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field.
10. (Original) The device of claim 9, wherein the dopant is boron or antimony.
11. (Original) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials, and wherein the difference in refractive index between the first material and the two second materials is at least 0.2.
12. (Original) The device of claim 1, wherein the peripheral sidewall extends completely around the pixel periphery.
13. (Original) The device of claim 1, wherein the peripheral sidewall extends from the light incident surface to the backside surface.
14. (Original) The device of claim 1, further comprising a frontside light trapping material at least partially covering the light incident surface.
15. (Original) The device of claim 14, wherein the frontside light trapping material is an antireflective layer coating.
16. (Original) The device of claim 14, wherein the frontside light trapping material is a reflective layer having an aperture to allow entry of light into the pixel, wherein the reflective layer is operable to reflect light impinging thereupon from inside the pixel back into the pixel.
17. (Original) The device of claim 16, further comprising a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.

18. (Original) The device of claim 16, wherein the aperture has an effective surface area of 90% of the incident light surface total surface area.

19. (Original) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

20. (Original) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface.

21-33. (Canceled)

REMARKS

By the Office Action of 11 July 2022, claims 1–20 are pending in the Application, and subject to restriction.

Applicant elects, without traverse, species 6 of FIG. 6.

Applicant submits this Response to Restriction Requirement solely to facilitate prosecution. As such, Applicant requests rejoinder upon examination. Applicant reserves the right to present new or additional claims in this Application that have similar or broader scope as originally filed. Applicant also reserves the right to present additional claims in a later-filed continuation application that have similar or broader scope as originally filed. Accordingly, any amendment, argument, or claim cancellation presented during prosecution is not to be construed as abandonment or disclaimer of subject matter.

This election is made without traverse.

Fees

This Response to Restriction Requirement is being filed within two months of the Office Action, thus no extension of time fee is believed due. No Claim fees are believed due, as the total number of independent Claims pending, and total Claims pending, are covered under the filing fee for the original set of Claims. Nonetheless, should any fees be due, authorization to charge or credit deposit account No. 500436 is hereby expressly given.

CONCLUSION

This Response is a full and complete response to the 11 July 2022 *Office Action*. It is respectfully submitted that all claims are in condition for allowance and that each point raised in the *Office Action* has been fully addressed. By the present *Response*, therefore, the Application has been placed in full condition for allowance. Accordingly, Applicant respectfully requests early and favorable action. Should Examiner have any further questions or reservations, Examiner is invited to telephone the undersigned Agent at 404.885.3652.

Respectfully submitted,

/Mark Lehi Jones/
Mark Lehi Jones, Ph.D.
Agent for the Assignee
USPTO Reg. No. 63,064

Troutman Sanders LLP
Bank of America Plaza
600 Peachtree Street, N.E., Suite 5200
Atlanta, Georgia 30308-2216
United States
Phone: 404.885.3652
Fax: 404.962.6650
8 September 2022

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 17/214,333		Filing Date 03/26/2021		☐ To be Mailed	
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO									
APPLICATION AS FILED - PART I									
		(Column 1)	(Column 2)						
FOR		NUMBER FILED	NUMBER EXTRA	RATE (\$)		FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A	N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))		N/A	N/A	N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A	N/A					
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*	x \$100 =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*	x \$480 =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL					
APPLICATION AS AMENDED - PART II									
AMENDMENT		(Column 1)		(Column 2)	(Column 3)	RATE (\$)		ADDITIONAL FEE (\$)	
	09/08/2022	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA				
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	x \$100 =		0	
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0	x \$480 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))								
AMENDMENT	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
	TOTAL ADD'L FEE							0	
		(Column 1)		(Column 2)	(Column 3)	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =			
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
TOTAL ADD'L FEE									
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						LIE			
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/VICTORIA JOHNSON/			
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".									
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/214,333	03/26/2021	Martin U. Pralle	143705.000335	1018
11951	7590	10/21/2022	EXAMINER	
Troutman Pepper Hamilton Sanders LLP (Rochester)			PHAM, LONG	
70 Linden Oaks				
Suite 210				
Rochester, NY 14625			ART UNIT	PAPER NUMBER
			2814	
			NOTIFICATION DATE	DELIVERY MODE
			10/21/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

BadumK@pepperlaw.com
USPTOinboxroc@pepperlaw.com

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Election/Restrictions

Applicant's election without traverse of claims 1-20 in the reply filed on 9/8/22 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –
(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claim(s) 1, 12-17, and 20 is/are rejected under pre-AIA 35 U.S.C. 102(a) as being anticipated by Haddad et al. (WO2011035188).

With respect to claim 1, Haddad et al. teach a light trapping device, comprising (see figs. 1-17, particularly figs. 1-6 and associated English text):

at least one light sensitive pixel having a light incident surface (top), a backside surface (bottom) opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

a backside light trapping material 18,20 substantially covering the backside surface; and a peripheral light trapping material 30 substantially covering the peripheral sidewall;

wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

With respect to claim 12, Haddad et al. teach the peripheral sidewall extends completely around the pixel periphery.

With respect to claim 13, Haddad et al. teach the peripheral sidewall extends from the light incident surface to the backside surface.

With respect to claim 14, Haddad et al. teach comprising a frontside light trapping material at least partially covering the light incident surface. See page 24, lines 15-30.

With respect to claim 15, Haddad et al. teach the frontside light trapping material is an antireflective layer coating. See page 24, lines 15-30.

With respect to claim 16, Haddad et al. teach the frontside light trapping material is a reflective layer having an aperture to allow entry of light into the pixel, wherein the reflective layer is operable to reflect light impinging thereupon from inside the pixel back into the pixel.

With respect to claim 17, Haddad et al. teach a lens 50 functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.

With respect to claim 20, Haddad et al. teach at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface. See fig. 4.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 18-19 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Haddad et al. (WO2011035188) (a reference of record).

With respect to claim 18, Haddad et al. fail to teach the range for the aperture surface area.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the aperture surface area through routine experimentation and optimization to obtain optimal or desired device performance because there is no evidence indicating that the claimed range is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claim 19, Haddad et al. fail to teach the light trap material is made of metal.

However, the use of metal as light trap material is well-known in semiconductor art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LONG PHAM whose telephone number is (571)272-1714. The examiner can normally be reached Mon-Friday.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: <https://patentcenter.uspto.gov>. Visit <https://www.uspto.gov/patents/apply/patent-center> for more information about Patent Center and <https://www.uspto.gov/patents/docx> for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LONG . PHAM
Examiner

Application/Control Number: 17/214,333
Art Unit: 2814

Page 6

Art Unit 2814

/LONG PHAM/
Primary Examiner, Art Unit 2814

<i>Notice of References Cited</i>	Application/Control No. 17/214,333	Applicant(s)/Patent Under Reexamination Pralle et al.	
	Examiner LONG PHAM	Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
	A					
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N	WO2011035188	03-2011	WO	Haddad	
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 17/214,333	Applicant(s)/Patent Under Reexamination Pralle et al.
	Examiner LONG PHAM	Art Unit 2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant					☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE								
Final	Original	07/02/2022	10/18/2022							
	1	÷	✓							
	2	÷	○							
	3	÷	○							
	4	÷	○							
	5	÷	○							
	6	÷	○							
	7	÷	○							
	8	÷	○							
	9	÷	○							
	10	÷	○							
	11	÷	○							
	12	÷	✓							
	13	÷	✓							
	14	÷	✓							
	15	÷	✓							
	16	÷	✓							
	17	÷	✓							
	18	÷	✓							
	19	÷	✓							
	20	÷	✓							

PHOTOSENSITIVE IMAGING DEVICES AND ASSOCIATED METHODS

DOCUMENT ID

WO-2011035188-A2

DATE PUBLISHED

2011-03-24

INVENTOR INFORMATION

NAME	CITY	STATE	ZIP CODE	COUNTRY
HADDAD HOMAYOON	N/A	N/A	N/A	US
JIANG JUTAO	N/A	N/A	N/A	US
MCKEE JEFFREY	N/A	N/A	N/A	US
MILLER DRAKE	N/A	N/A	N/A	US
FORBES LEONARD	N/A	N/A	N/A	US
PALSULE CHINTAMANI	N/A	N/A	N/A	US

DATE FILED

2010-09-17

CPC CURRENT

TYPE	CPC	DATE
CPCI	H01L27/14636	2013-01-01
CPCI	H01L27/14609	2013-01-01
CPCI	H01L27/14612	2013-01-01
CPCI	H01L27/14609	2013-01-01
CPCI	H01L27/14627	2013-01-01
CPCI	H01L27/14629	2013-01-01
CPCI	H01L27/14629	2013-01-01
CPCI	H01L27/14627	2013-01-01
CPCI	H01L27/1461	2013-01-01
CPCI	H01L27/1464	2013-01-01
CPCI	H01L27/14625	2013-01-01
CPCI	H01L27/1464	2013-01-01
CPCI	H01L27/14625	2013-01-01
CPCI	H01L27/14629	2013-01-01
CPCI	H01L27/14625	2013-01-01
CPCI	H01L27/1464	2013-01-01
CPCI	H01L27/14609	2013-01-01
CPCI	H01L27/14627	2013-01-01

Abstract

Photosensitive devices and associated methods are provided. In one aspect, for example, a photosensitive imager device can include a semiconductor substrate having multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. In one aspect, the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation. In another aspect, interacting with electromagnetic radiation further includes increasing the semiconductor substrate's effective absorption wavelength as compared to a semiconductor substrate lacking a textured region.

Description

PHOTOSENSITIVE IMAGING DEVICES AND ASSOCIATED METHODS PRIORITY DATA

This application claims the benefit of U.S. Provisional Patent Application Serial No. 61/243,434, filed on September 17, 2009, U.S. Provisional Patent Application Serial No. 61/311,004 filed on March 5, 2010, and U.S. Provisional Patent Application Serial No. 61/311,107, filed on March 5, 2010, each of which is incorporated herein by reference. BACKGROUND

The interaction of light with semiconductor materials has been a significant innovation. Silicon imaging devices are used in various technologies, such as digital cameras, optical mice, video cameras, cell phones, and the like. Charge-coupled devices (CCDs) were widely used in digital imaging, and were later improved upon by complementary metal-oxide-semiconductor (CMOS) imagers having increased performance. CMOS sensors are typically manufactured from silicon and can convert visible incident light into a photocurrent and ultimately into a digital image. Silicon-based technologies for detecting infrared incident electromagnetic radiation have been problematic, however, because silicon is an indirect bandgap semiconductor having a bandgap of about 1.1 eV. Thus the absorption of electromagnetic radiation having wavelengths of greater than about 1100 nm is, therefore, very low in silicon.

SUMMARY

The present disclosure provides photosensitive devices and associated methods. In one aspect, for example, a photosensitive imager device can include a semiconductor substrate having multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. In one aspect, the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation. In another aspect, interacting with electromagnetic radiation further includes increasing the semiconductor substrate's effective absorption length as compared to a semiconductor substrate lacking a textured region. In one specific aspect, the transfer --> element is selected from the group consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.

The textured region can be positioned in a variety of locations relative to the doped regions. In one aspect, for example, the textured region is positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions. In one specific aspect, the textured region has a surface morphology operable to direct electromagnetic radiation into or out of the semiconductor substrate. The surface morphology of the textured region relative to the semiconductor substrate can include a variety of configurations, including, without limitation, sloping, pyramidal, inverted pyramidal, spherical, parabolic, asymmetric, symmetric, and the like, including combinations thereof.

In another aspect, the textured region can be positioned on a surface of the semiconductor substrate that is adjacent the multiple doped regions. In a more specific aspect, an additional textured region can be positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions. In this manner, textured regions can thus be positioned adjacent to multiple doped regions and opposite the multiple doped regions.

Various aspects of the textured region can vary depending on the desired configuration of the device. In one

aspect, however, the textured region includes surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof. Numerous surface feature morphologies are contemplated, nonlimiting examples of which include cones, pillars, pyramids, microlenses, quantum dots, inverted features, and combinations thereof. Additionally, the textured region can be formed by a variety of processes. Nonlimiting examples of such texturing processes can include lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, and combinations thereof. Additional layers and/or structures can be included in various devices according to aspects present disclosure. In one aspect, for example, a reflective layer can be coupled to the semiconductor substrate and positioned to maintain the electromagnetic radiation in the semiconductor substrate. In another aspect, a lens can be optically coupled to the semiconductor substrate and positioned to focus incident electromagnetic radiation into the semiconductor substrate. --> In another aspect of the present disclosure, a method of making a

photosensitive imager device is provided. Such a method can include forming a textured region on a semiconductor substrate having multiple doped regions forming a least one junction, wherein the textured region is formed in a position to interact with electromagnetic radiation and coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction.

In one aspect, the photosensitive imager device can be tuned to be selected to filter out specific electromagnetic radiation wavelengths. In one specific aspect, tuning includes forming surface features to have dimensions that selectively diffuse or selectively absorb a desired wavelength of electromagnetic radiation. In another aspect, tuning is accomplished through a factor selected from the group consisting of placement of the textured region, material type and/or thickness of the textured region, dopant type of the textured region, doping profile of the texture region, dopant profile of the semiconductor substrate, material type and/or thickness of the semiconductor substrate, and combinations thereof.

In another aspect of the present disclosure, a photosensitive imager device is provided. Such a device can include a semiconductor substrate having multiple doped regions forming a least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and at least 4 transistors coupled to the semiconductor substrate and with at least one of the transistors electrically coupled to the at least one junction.

BRIEF DESCRIPTION OF THE DRAWINGS FIG. 1 is a schematic view of a photosensitive device in accordance with one aspect of the present disclosure;

FIG. 2 is a schematic view of a photosensitive device in accordance with another aspect of the present disclosure;

FIG. 3 is a schematic view of a photosensitive device in accordance with yet another aspect of the present disclosure;

FIG. 4 is a schematic view of a photosensitive device in accordance with a further aspect of the present disclosure;

FIG. 5 is a schematic view of a photosensitive device in accordance with yet a further aspect of the present disclosure; --> FIG. 6 is a schematic view of a photosensitive device in accordance with another aspect of the present disclosure;

FIG. 7 is a schematic view of a photosensitive pixel device in accordance with yet another aspect of the present disclosure;

FIG. 8 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

FIG. 9 is a schematic view of a photosensitive pixel device in accordance with yet a further aspect of the present disclosure;

FIG. 10 is a schematic view of a photosensitive pixel device in accordance with another aspect of the present disclosure;

FIG. 11 is a schematic view of a photosensitive pixel device in accordance with yet another aspect of the present disclosure;

FIG. 12 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

FIG. 13 is a schematic view of a photosensitive pixel device in accordance with another aspect of the

present disclosure;

FIG. 14 is a schematic view of a photosensitive imager device in accordance with yet another aspect of the present disclosure;

FIG. 15 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

FIG. 16 is a schematic view of a photosensitive pixel device in accordance with another aspect of the present disclosure; and

FIG. 17 is a depiction of a method of making a photosensitive imager device in accordance with yet another aspect of the present disclosure.

DETAILED DESCRIPTION

Before the present disclosure is described herein, it is to be understood that this disclosure is not limited to the particular structures, process steps, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting. --> Definitions

The following terminology will be used in accordance with the definitions set forth below.

It should be noted that, as used in this specification and the appended claims, the singular forms "a," and, "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a dopant" includes one or more of such dopants and reference to "the layer" includes reference to one or more of such layers.

As used herein, the term "low oxygen content" refers to any material having an interstitial oxygen content that is less than or equal to about 60 ppm atomic.

As used herein, the terms "disordered surface" and "textured surface" can be used interchangeably, and refer to a surface having a topology with nano- to micron- sized surface variations formed by the irradiation of laser pulses. While the characteristics of such a surface can be variable depending on the materials and techniques employed, in one aspect such a surface can be several hundred nanometers thick and made up of nanocrystallites (e.g. from about 10 to about 50 nanometers) and nanopores. In another aspect, such a surface can include micron-sized structures (e.g. about 2 μm to about 60 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 500 μm .

As used herein, the term "fluence" refers to the amount of energy from a single pulse of laser radiation that passes through a unit area. In other words, "fluence" can be described as the energy density of one laser pulse.

As used herein, the terms "surface modifying" and "surface modification" refer to the altering of a surface of a semiconductor material using laser radiation. In one specific aspect, surface modification can include processes using primarily laser radiation or laser radiation in combination with a dopant, whereby the laser radiation facilitates the incorporation of the dopant into a surface of the semiconductor material. Accordingly, in one aspect surface modification includes doping of a semiconductor material.

As used herein, the term "target region" refers to an area of a semiconductor material that is intended to be doped or surface modified using laser radiation. The target region of a semiconductor material can vary as the surface modifying process progresses. For example, after a first target region is doped or surface modified, a second target region may be selected on the same semiconductor material. --> As used herein, the term "detection" refers to the sensing, absorption, and/or collection of electromagnetic radiation.

As used herein, the term "substantially" refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is "substantially" enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use of "substantially" is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is "substantially free of particles" would either completely lack particles, or so nearly completely lack particles that the effect would be the

same as if it completely lacked particles. In other words, a composition that is "substantially free of an ingredient or element may still actually contain such item as long as there is no measurable effect thereof. As used herein, the term "about" is used to provide flexibility to a numerical range endpoint by providing that a given value may be "a little above" or "a little below" the endpoint.

As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience.

However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of "about 1 to about 5" should be interpreted to include --> not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

This same principle applies to ranges reciting only one numerical value as a minimum or a maximum.

Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

The Disclosure

Electromagnetic radiation can be present across a broad wavelength range, including visible range wavelengths (approximately 350nm to 800nm) and non- visible wavelengths (longer than about 800nm or shorter than 350 nm). The infrared spectrum is often described as including a near infrared portion of the spectrum including wavelengths of approximately 800 to 1300 nm, a short wave infrared portion of the spectrum including wavelengths of approximately 1300 nm to 3 micrometers, and a mid to long wave infrared (or thermal infrared) portion of the spectrum including wavelengths greater than about 3 micrometers up to about 30 micrometers. These are generally and collectively referred to herein as "infrared" portions of the electromagnetic spectrum unless otherwise noted.

Traditional silicon photodetecting imagers have limited light absorption/detection properties. For example, infrared light is mostly transparent to such silicon based detectors. While other materials (e.g. InGaAs) can be used to detect infrared electromagnetic radiation having wavelengths greater than about 1000 nm, silicon is still commonly used because it is relatively cheap to manufacture and can be used to detect wavelengths in the visible spectrum (i.e. visible light, 350 nm - 800 nm). Traditional silicon materials require substantial absorption depths to detect photons having wavelengths longer than approximately 700 nm. While visible light can be absorbed at relatively shallow depths in silicon, absorption of longer wavelengths (e.g. 900 nm) in silicon of a standard wafer depth (e.g. approximately 750 μ .Math. η) is poor if at all. The devices of the present disclosure increase the absorption of semiconductor materials by decreasing the effective absorption length to longer wavelengths as compared to traditional materials. For example, the absorption depth of silicon can be reduced such that these longer wavelengths can be absorbed at depths of less than or equal to about 850 μ .Math. η . In other words, by decreasing the --> effective absorption length these devices are able to absorb longer wavelengths (e.g. >1000 nm for silicon) within a thin semiconductor material. In addition to increasing the effective absorption length, the response rate or response speed can also be increased using thinner semiconductor materials.

The present disclosure additionally provides broadband photosensitive diodes, pixels, and imagers capable of detecting visible as well as infrared electromagnetic radiation, including associated methods of making such devices. A photosensitive diode can include a semiconductor substrate having multiple doped regions forming at least one junction, and at least one textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation. In one aspect the multiple doped regions can include at least one cathode region and at least one anode region. In some aspects, doped regions can include an n-

type dopant and/or a p-type dopant as is discussed below, thereby creating a p-n junction. In other aspects, a photosensitive device can include an i-type region to form a p-i-n junction.

A photosensitive pixel can include a semiconductor substrate having multiple doped regions forming at least one junction, at least one textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. A photosensitive imager can include multiple photosensitive pixels. Additionally, an electrical transfer element can include a variety of devices, including without limitation, transistors, sensing nodes, transfer gates, transfer electrodes, and the like.

Photosensitive or photodetecting imagers include photodiodes or pixels that are capable of absorbing electromagnetic radiation within a given wavelength range. Such imagers can be passive pixel sensors (PPS), active pixel sensors (APS), digital pixel sensor imagers (DPS), or the like, with one difference being the image sensor read out architecture. For example, a semiconducting photosensitive imager can be a three or four transistor active pixel sensor (3T APS or 4T APS). Various additional components are also contemplated, and would necessarily vary depending on the particular configuration and intended results. As an example, a 4T configuration can additionally include, among other things, a transfer gate, a reset, a source follower, and row select transistors. Additionally, devices having greater than 4 transistors are also within the present scope. --> Photosensitive imagers can be front side illumination (FSI) or back side illumination (BSI) devices, and there are advantages and disadvantages to both architecture types. In a typical FSI imager, incident light enters the semiconductor device by first passing by transistors and metal circuitry. The light, however, can scatter off of the transistors and circuitry prior to entering the light sensing portion of the imager, thus causing optical loss and noise. A lens can be disposed on the topside of a FSI pixel to direct and focus the incident light to the light sensing active region of the device, thus partially avoiding the circuitry. In one aspect the lens can be a microlens. BSI imagers, on the other hand, are configured to have the depletion region of the junction extending to the opposite side of the device. In one aspect, for example, incident light enters the device via the light sensing portion and is mostly absorbed prior to reaching the circuitry. BSI designs allow for smaller pixel architecture and a high fill factor for the imager. As mentioned, the present disclosure can be adapted for either configuration. It should also be understood that devices according to aspects of the present disclosure can be incorporated into complementary metal-oxide- semiconductor (CMOS) imager architectures or charge-coupled device (CCD) imager architectures. In one aspect, as is shown in FIG. 1, a photosensitive diode 10 can include a semiconductor substrate 12 having multiple doped regions 14, 16 forming at least one junction, and at least one textured region 18 coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation. The different doped regions can have the same doping profile or different doping profiles, depending on the device. Such an architecture is a FSI design where light enters the semiconductor substrate from the direction of the multiple doped regions. While the device shown in FIG. 1 contains three doped regions, it should be noted that aspects containing one or more doped regions are considered to be within the present scope. Additionally, the semiconductor substrate can be doped, and thus can be considered to be a doped region in some aspects. It should also be noted that the photosensitive diode can be configured with a BSI architecture, and thus electromagnetic radiation would enter the semiconductor substrate from the direction of the textured region.

The various devices according to aspects of the present disclosure can exhibit increased quantum efficiency over traditional photosensitive devices. Any increase in the quantum efficiency makes a large difference in the signal to noise ratio. More complex structures can provide not only increased quantum efficiency but also good --> uniformity from pixel to pixel. In addition, devices of the present disclosure exhibit increased responsivity as compared to traditional photosensitive devices. For example, in one aspect the responsivity can be greater than or equal to 0.8A/W for wavelengths greater than 1000 nm for semiconductor substrate that is less than 100 μm thick.

Photosensitive imagers can be maintained under constant conditions (fixed voltage or current) to provide enhanced linearity and uniformity. Connections between the imager and the underlying device layers can be achieved using vias fabricated from a refractory metal, such as tungsten or tantalum. Placing storage elements under the imager may provide various photonic benefits. For example, the entire pixel array may be dedicated to signal processing. This may enable higher performance by permitting access to low level

pixel signals. Furthermore, massively parallel operations can be performed by pixel processors. For example, analog to digital conversion, noise reduction (ie., true correlated double sampling), power conditioning, nearest neighbor pixel processing, compression, fusion, and color multiplexing operations can be performed.

A variety of semiconductor materials are contemplated for use with the devices and methods according to aspects of the present disclosure. Non-limiting examples of such semiconductor materials can include group IV materials, compounds and alloys comprised of materials from groups III and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can include silicon carbide (SiC) and silicon germanium (SiGe). In one specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum gallium arsenide, and combinations thereof.

Exemplary combinations of group II- VI materials can include cadmium selenide (CdSe), cadmium sulfide (CdS), cadmium telluride (CdTe), zinc oxide (ZnO), zinc selenide (ZnSe), zinc sulfide (ZnS), zinc telluride (ZnTe), cadmium zinc --> telluride (CdZnTe, CZT), mercury cadmium telluride (HgCdTe), mercury zinc telluride (HgZnTe), mercury zinc selenide (HgZnSe), and combinations thereof.

Exemplary combinations of group III-V materials can include aluminum antimonide (AlSb), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum phosphide (AlP), boron nitride (BN), boron phosphide (BP), boron arsenide (BAs), gallium antimonide (GaSb), gallium arsenide (GaAs), gallium nitride (GaN), gallium phosphide (GaP), indium antimonide (InSb), indium arsenide (InAs), indium nitride (InN), indium phosphide (InP), aluminum gallium arsenide (AlGaAs, Al_{sub.x}Ga_{1-x}As), indium gallium arsenide (InGaAs, In_{sub.x}Ga_{1-x}As), indium gallium phosphide (InGaP), aluminum indium arsenide (AlInAs), aluminum indium antimonide (AlInSb), gallium arsenide nitride (GaAsN), gallium arsenide phosphide (GaAsP), aluminum gallium nitride (AlGaN), aluminum gallium phosphide (AlGaP), indium gallium nitride (InGaN), indium arsenide antimonide (InAsSb), indium gallium antimonide (InGaSb), aluminum gallium indium phosphide (AlGaInP), aluminum gallium arsenide phosphide (AlGaAsP), indium gallium arsenide phosphide (InGaAsP), aluminum indium arsenide phosphide (AlInAsP), aluminum gallium arsenide nitride (AlGaAsN), indium gallium arsenide nitride (InGaAsN), indium aluminum arsenide nitride (InAlAsN), gallium arsenide antimonide nitride (GaAsSbN), gallium indium nitride arsenide antimonide (GaInNAsSb), gallium indium arsenide antimonide phosphide (GaInAsSbP), and combinations thereof.

The semiconductor material can be of any thickness that allows electromagnetic radiation detection and conversion functionality, and thus any such thickness of semiconductor material is considered to be within the present scope. In some aspects the laser processed region of the semiconductor increases the efficiency of the device such that the semiconductor material can be thinner than has previously been possible. Decreasing the thickness of the semiconductor reduces the amount of semiconductor material required to make such a device. In one aspect, for example, the semiconductor material has a thickness of from about 500 nm to about 50 μm . In another aspect, the semiconductor material has a thickness of less than or equal to about 500 μm . In yet another aspect, the semiconductor material has a thickness of from about 1 μm to about 10 μm . In a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 750 μm . In yet a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 100 μm . --> Additionally, various types of semiconductor material are contemplated, and any such material that can be incorporated into an electromagnetic radiation detection device is considered to be within the present scope. In one aspect, for example, the semiconductor material is monocrystalline. In another aspect, the semiconductor material is multicrystalline. In yet another aspect, the semiconductor material is microcrystalline. It is also contemplated that the semiconductor material can be amorphous. Specific nonlimiting examples include amorphous silicon or amorphous selenium.

The semiconductor materials of the present disclosure can also be made using a variety of manufacturing

processes. In some cases the manufacturing procedures can affect the efficiency of the device, and may be taken into account in achieving a desired result. Exemplary manufacturing processes can include Czochralski (Cz) processes, magnetic Czochralski (mCz) processes, Float Zone (FZ) processes, epitaxial growth or deposition processes, and the like. Whether or not low oxygen content is desired in the device can also affect the choice of a manufacturing process for the semiconductor material. Various processes produce semiconductor materials containing varying amounts of oxygen, and as such, some applications having more stringent tolerances with respect to oxygen levels may benefit more from specific manufacturing procedures as compared to others. For example, during CZ crystal growth oxygen from the containment vessel, usually a quartz crucible, can become incorporated into the crystal as it is pulled. Additionally, other sources of oxygen contamination are also possible with the CZ process. Such contamination may be reduced, however, through the use of non oxygen-containing crucible materials, as well as the development of other crystal growth methods that do not utilize a crucible. One such process is the FZ process.

Materials grown with the CZ method can also be made to have lowered oxygen concentration through enhancements to the crystal growth process, such as growing the crystal in the presence of a magnetic field (i.e. the mCz process). Also, gettering techniques can be employed to reduce the impact of oxygen or other impurities on the finished device. These gettering techniques can include thermal cycles to liberate or nucleate impurities, or selective ion implantation of species to serve as gettering sites for the impurities. For example, oxygen concentrated in the semiconductor can be removed by the performing a furnace cycle to form a denuded zone. During heating with an inert gas, oxygen near the surface of the semiconductor --> diffuses out of the material. During the furnace cycle but after the denuding step, nucleating and growing steps may be performed. Nucleating sites for precipitates are formed during the nucleating step, and the precipitates are grown from the nucleating sites during a growing step. The precipitates are formed from interstitial oxygen within the bulk of the semiconductor material and beneath the denuded zone. The precipitation of oxygen in the bulk of the semiconductor material can be desired because such precipitates can act as gettering sites. Such precipitate formation can also be performed to "lock up" interstitial oxygen into the precipitates and reduce the likelihood that such oxygen can migrate from the bulk of the semiconductor material into the denuded zone.

In those aspects where low oxygen content of the device is desired, further processing of the semiconductor material can be performed so as to minimize the introduction of oxygen. Oxygen can exist in different states or at different sites (for example, interstitially or substitutionally) within a semiconductor such as silicon, dependent upon the thermal processing the semiconductor has received. If the semiconductor is subjected to temperatures higher than, for example, about 1000° C, oxygen can form aggregates or clusters that serve as defect sites in the crystal lattice. These sites may result in trap states and a reduction in carrier lifetime within the semiconductor material and device can occur. At lower temperatures (for example, around 400° C to 700° C), oxygen can behave as electrically active thermal donors. Thus, oxygen can have a negative impact on carrier lifetime and on carrier mobility. In a device fabricated to have photoconductive gain, the presence of oxygen causing reduced carrier lifetime may result in reduced levels of photoconductive gain. It may be beneficial, therefore, to produce semiconductor devices such that a low oxygen content is obtained or maintained. This can be accomplished in a variety of ways, including using semiconductor materials having low levels of oxygen contained therein to begin with, processing these materials in a manner that minimizes the uptake of oxygen into the semiconductor lattice, and utilizing techniques that eliminate or reduce oxygen that may be present in the semiconductor. Such processes and techniques can include, for example, annealing the semiconductor material and any laser treated region to lower temperatures as compared to previous annealing procedures. Annealing processes are discussed more fully below. Additionally, texture processing of the semiconductor material and/or any annealing process can be performed in a substantially oxygen-depleted environment --> in order to minimize the introduction of oxygen into the semiconductor. An oxygen- depleted or substantially oxygen-depleted environment can include a variety of environments. In one aspect, for example, the oxygen-depleted environment can be an environment whereby oxygen from the air or other sources has been replaced with a gas or other fluid containing little to no oxygen. In another aspect, processing can occur in a vacuum environment, and thus contain little to no oxygen. Additionally, oxygen-containing materials or materials that introduce oxygen into the

semiconductor, such as, for example, quartz crucibles, can be avoided. As a practical matter, the term

"oxygen-depleted environment" can be used to describe an environment with low levels of oxygen, provided a semiconductor material can be processed therein within the desired tolerances. Thus, environments having low oxygen, or little to no oxygen, are environments in which a semiconductor can be processed as a low-oxygen content semiconductor while maintaining oxygen levels within the tolerances of the present disclosure. In one aspect, an oxygen-depleted environment can be an oxygen-free environment. Further details regarding low-oxygen content semiconductor materials can be found in US Patent Application No. 12/771848, filed on April 30, 2010, which is incorporated herein by reference.

The semiconductor material can have varying levels of interstitial oxygen depending on the desired efficiency of the device. In some aspects, oxygen content may be of no concern, and thus any level of oxygen within the lattice is acceptable. In other aspects, a low oxygen content is desired. In one aspect a semiconductor material can have an oxygen content that is less than or equal to about 50 ppm atomic. In another aspect, a semiconductor material can have an oxygen content that is less than or equal to about 30 ppm atomic. In yet another aspect, the semiconductor material can have an oxygen content less than or equal to about 10 ppm atomic. In another aspect the semiconductor can have an oxygen content less than about 5 ppm atomic. In yet another aspect the semiconductor can have an oxygen content less than about 1 ppm atomic.

As has been described, the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device. The textured region can include surface features to increase the effective absorption length of the photosensitive pixel. The surface features can be cones, pyramids, pillars, protrusions, microlenses, quantum dots, inverted features and the like. Factors such as --> as manipulating the feature sizes, dimensions, material type, dopant profiles, texture location, etc. can allow the diffusing region to be tunable for a specific wavelength. In one aspect, tuning the device can allow specific wavelengths or ranges of wavelengths to be absorbed. In another aspect, tuning the device can allow specific wavelengths or ranges of wavelengths to be reduced or eliminated via filtering.

Tuning can also be accomplished through the location of the texture region within the device, modifying the dopant profile(s) of regions within the device, dopant selection, and the like. Additionally, material composition near the textured region can create a wavelength specific photosensing pixel device. It should be noted that a wavelength specific photosensing pixel can differ from one pixel to the next, and can be incorporated into an imaging array. For example a 4 x 4 array can include a blue pixel, a green pixel, a red pixel, and infrared light absorbing pixel, or a blue pixel, two green pixels, and a red pixel.

Textured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared). Such internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor substrate. This increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.

The textured region can be formed by various techniques, including lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, additional material deposition, and the like. For example, pillar features can be incorporated into pixels by thinning or removing material from the backside of a FSI semiconductor substrate by using deep trench isolation and etching techniques. In one aspect material can be removed to a thickness of about 20 μm . Anisotropic etching can be used to produce a sloping backside pyramid structure, spherical, structure parabolic structure, a lens structure with reflectors, and the like. Such features on the backside of pillars will also serve to diffuse and reflect electromagnetic radiation.

In one aspect, the texturing process can be performed during the manufacture of the photosensitive device. In another aspect, the texturing process can be performed on a photosensitive device that has previously been made. For example, a CMOS, CCD, or other photosensitive element can be textured following manufacture. In this case, material layers may be removed from the photosensitive element to --> expose the semiconductor substrate or bulk material upon which a textured region may be formed.

One effective method of producing a textured region is through laser processing. Such laser processing allows discrete locations of the semiconductor substrate to be textured. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope. Laser treatment or processing can allow, among other

things, enhanced absorption properties and thus increased electromagnetic radiation focusing and detection. The laser treated region can be associated with the surface nearest the impinging electromagnetic radiation, or the laser treated surface can be associated with a surface opposite in relation to impinging electromagnetic radiation, thereby allowing the radiation to pass through the semiconductor material before it hits the laser treated region.

In one aspect, for example, a target region of the semiconductor material can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Patents 7,057,256, 7,354,792 and 7,442,629, which are incorporated herein by reference in their entireties. Briefly, a surface of a semiconductor material is irradiated with laser radiation to form a textured or surface modified region. Such laser processing can occur with or without a dopant material. In those aspects whereby a dopant is used, the laser can be directed through a dopant carrier and onto the semiconductor surface. In this way, dopant from the dopant carrier is introduced into the target region of the semiconductor material. Such a region incorporated into a semiconductor material can have various benefits in accordance with aspects of the present disclosure. For example, the target region typically has a textured surface that increases the surface area of the laser treated region and increases the probability of radiation absorption via the mechanisms described herein. In one aspect, such a target region is a substantially textured surface including micron-sized and/or nano-sized surface features that have been generated by the laser texturing. In another aspect, irradiating the surface of semiconductor material includes exposing the laser radiation to a dopant such that irradiation incorporates the dopant into the semiconductor. Various dopant materials are known in the art, and are discussed in more detail herein.

Thus the surface of the semiconductor material is chemically and/or structurally altered by the laser treatment, which may, in some aspects, result in the --> formation of surface features appearing as microstructures or patterned areas on the surface and, if a dopant is used, the incorporation of such dopants into the semiconductor material. In some aspects, the features or microstructures can be on the order of 50 nm to 20 μm in size and can assist in the absorption of electromagnetic radiation. In other words, the textured surface can increase the probability of incident radiation being absorbed by the semiconductor material.

The type of laser radiation used to surface modify a semiconductor material can vary depending on the material and the intended modification. Any laser radiation known in the art can be used with the devices and methods of the present disclosure. There are a number of laser characteristics, however, that can affect the surface modification process and/or the resulting product including, but not limited to the wavelength of the laser radiation, pulse width, pulse fluence, pulse frequency, polarization, laser propagation direction relative to the semiconductor material, etc. In one aspect, a laser can be configured to provide pulsed laser radiation of a semiconductor material. A short-pulsed laser is one capable of producing femtosecond, picosecond and/or nanosecond pulse durations. Laser pulses can have a central wavelength in a range of about from about 10 nm to about 8 μm , and more specifically from about 200 nm to about 1200 nm. The pulse width of the laser radiation can be in a range of from about tens of femtoseconds to about hundreds of nanoseconds. In one aspect, laser pulse widths can be in the range of from about 50 femtoseconds to about 50 picoseconds. In another aspect, laser pulse widths can be in the range of from about 50 picoseconds to 100 nanoseconds. In another aspect, laser pulse widths are in the range of from about 50 to 500 femtoseconds.

The number of laser pulses irradiating a target region can be in a range of from about 1 to about 2000. In one aspect, the number of laser pulses irradiating a semiconductor target region can be from about 2 to about 1000. Further, the repetition rate or frequency of the pulses can be selected to be in a range of from about 10 Hz to about 10 μHz , or in a range of from about 1 kHz to about 1 MHz, or in a range from about 10 Hz to about 1 kHz. Moreover, the fluence of each laser pulse can be in a range of from about 1 kJ/m^2 to about 20 kJ/m^2 , or in a range of from about 3 kJ/m^2 to about 8 kJ/m^2 .

A variety of dopant materials are contemplated, and any such material that can be used in the laser treatment process to surface modify a semiconductor material according to aspects of the present disclosure is considered to be within the present --> scope. It should be noted that the particular dopant utilized can vary depending on the semiconductor material being laser treated, as well as the intended use of the resulting semiconductor material. For example, the selection of potential dopants may differ depending on

whether or not tuning of the photosensitive device is desired.

A dopant can be either electron donating or hole donating. In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof. It should be noted that the scope of dopant materials should include, not only the dopant materials themselves, but also materials in forms that deliver such dopants (i.e. dopant carriers). For example, S dopant materials includes not only S, but also any material capable being used to dope S into the target region, such as, for example, H₂S, SF₆, SO₂, and the like, including combinations thereof. In one specific aspect, the dopant can be S. Sulfur can be present at an ion dosage level of between about 5×10^{14} and about 1×10^{16} ions/cm². Non-limiting examples of fluorine-containing compounds can include ClF₃, PF₅, F₂, SF₆, BF₃, GeF₄, WF₆, SiF₄, HF, CF₄, CHF₃, CH₂F₂, CH₃F, C₂F₆, C₂HF₅, C₃F₈, C₄F₈, NF₃, and the like, including combinations thereof. Non-limiting examples of boron-containing compounds can include B(CH₃)₃, BF₃, BC₁, BN, C₂Bi₀Hi₂, borosilica, B₂, and the like, including combinations thereof. Non-limiting examples of phosphorous-containing compounds can include PF₅, PH₃, and the like, including combinations thereof. Non-limiting examples of chlorine-containing compounds can include Cl₂, SiH₂Cl₂, HCl, SiC, and the like, including combinations thereof.

Dopants can also include arsenic-containing compounds such as AsH₃ and the like, as well as antimony-containing compounds. Additionally, dopant materials can include mixtures or combinations across dopant groups, i.e. a sulfur-containing compound mixed with a chlorine-containing compound. In one aspect, the dopant material can have a density that is greater than air. In one specific aspect, the dopant material can include Se, H₂S, SF₆, or mixtures thereof. In yet another specific aspect, the dopant can be SF₆ and can have a predetermined concentration range of about 5.0×10^{-8} mol/cm³ to about 5.0×10^{-4} mol/cm³. SF₆ gas is a good carrier for the incorporation of sulfur into the semiconductor material via a laser process without significant adverse effects on the semiconductor material. Additionally, it is noted that dopants can also be liquid solutions of n-type or p-type dopant materials dissolved in a solution such as water, alcohol, or an acid or basic solution. Dopants can also be solid materials applied as a powder or as a suspension dried onto the wafer. --> The semiconductor substrate can be annealed for a variety of reasons, including dopant activation, semiconductor material damage repair, and the like. In those aspects including a laser textured region, the semiconductor material can be annealed prior to laser treatment, following laser treatment, during laser treatment, or both prior to and following laser treatment. Annealing can enhance the

semiconductive properties of the device, including increasing the photoresponse properties of the semiconductor materials. Additionally, annealing can reduce damage done by the lasing process. Although any known anneal can be beneficial and would be considered to be within the present scope, annealing at lower temperatures can be particularly useful. Such a "low temperature" anneal can greatly enhance the photoconductive gain and external quantum efficiency of devices utilizing such materials. In one aspect, for example, the semiconductor material can be annealed to a temperature of from about 300° C to about 1100° C. In another aspect, the semiconductor material can be annealed to a temperature of from about 500° C to about 900° C. In yet another aspect, the semiconductor material can be annealed to a temperature of from about 700° C to about 800° C. In a further aspect, the semiconductor material can be annealed to a temperature that is less than or equal to about 850° C.

The duration of the annealing procedure can vary according to the specific type of anneal being performed, as well as according to the materials being used. For example, rapid annealing processes can be used, and as such, the duration of the anneal may be shorter as compared to other techniques. Various rapid thermal anneal techniques are known, all of which should be considered to be within the present scope. In one aspect, the semiconductor material can be annealed by a rapid annealing process for a duration of greater than or equal to about 1 μs. In another aspect, the duration of the rapid annealing process can be from about 1 μs to about 1 ms. As another example, a baking or furnace anneal process can be used having durations that may be longer compared to a rapid anneal. In one aspect, for example, the semiconductor material can be annealed by a baking anneal process for a duration of greater than or equal to about 1 ms to several hours. As has been described, if low oxygen content semiconductor materials are used it may be

beneficial to anneal such materials in a substantially oxygen-depleted environment.

As has been described, annealing can help reduce defects inherent to the semiconductor substrate and otherwise reduce electron/hole recombination. In other --> words, the annealing can help create electron states that effectively reduce the undesirable recombination processes. Annealing the semiconductor material may also improve the responsivity or photoconductive gain of the device. Photoconductive devices can have dopants, impurities, or defects that can introduce energy levels that can trap carriers. Trapping carriers and reducing recombination of photocarriers can lead to an increase in photoconductive gain of the device. The relationship of photoconductive gain and trapping time can be represented by Equation (I): $\text{Gain} = \tau / t$ where " τ " is the lifetime of an excess carrier and " t " is the transit time of the carriers across the device. It is understood that the lifetime of an excess carrier can be increased by trapping a carrier species and reducing the recombination rate. An increase in gain can be achieved by trapping centers in the semiconductor that have millisecond trapping times at room temperature and short transit times in thinned lightly doped wafers. These trapping locations can decrease the recombination of carriers and therefore improve or increase the photoconductive gain of the device by allowing more electrons to traverse the different regions without being recombined.

Turning to FIG. 2, a reflecting layer 20 can be coupled to the semiconductor substrate 12. The reflecting layer can be coupled to any side or portion of the semiconductor substrate in order to reflect electromagnetic radiation back into the device. Accordingly, in one aspect the reflecting layer can be located on the semiconductor substrate opposite the incoming electromagnetic radiation. Thus, as is shown in FIG. 2, electromagnetic radiation passing through the semiconductor substrate and the textured region 16 can be reflected back into the semiconductor substrate. Additionally, a passivation layer 22 can be coupled to the semiconductor substrate. The passivation layer is shown coupled to the side of the semiconductor substrate facing the incoming electromagnetic radiation, however a passivation layer can be located anywhere on the device and still be within the present scope.

As has been described, location of the textured region can be used to provide enhancement and/or filtering of the incoming electromagnetic radiation. For example, a textured region located at the point of entry of the electromagnetic radiation into the photosensitive device tends to bend the electromagnetic radiation, particularly the blue wavelengths. Accordingly, one level of tuning can be accomplished by locating --> the textured region on the surface adjacent the incident electromagnetic radiation to purposely effectuate the filtering of blue wavelengths. Additionally, absorption of particular wavelengths of electromagnetic radiation occurs at different depths in the semiconductor layer and/or textured region. By increasing the absorption to green wavelengths, for example, the electrical signal as a result of green wavelengths can be increased in a diode or pixel. Certain traditional 4 pixel imagers have one red, one blue, and two green pixels, with the greater number of green pixels to account for increased sensitivity of the human eye to green colors. Thus in one aspect, a 4 pixel imager can have one blue, one red, and one green pixel having an increased green wavelength absorption. The fourth pixel can be used for an IR or other wavelength selective pixel depending on the desired application of the imager.

FIG. 3 shows a photosensitive device having textured regions 30 located on the sides of the semiconductor substrate 12. Such a configuration allows electromagnetic radiation normally exiting through the sides of the device to be further defused and absorbed within semiconductor substrate. The textured region(s) can be located on one or more sides to facilitate the enhanced absorption.

FIG. 4 shows a photosensitive device having a textured region 40 having a nonparallel surface with respect to the semiconductor substrate 12. Thus the overall configuration of the textured region can be designed to further enhance absorption and/or selectively tune the device. As has been described, the nonparallel surface can have a variety of configurations, such as, without limitation, nonparallel slope, a pyramid, an inverted pyramid, a concave shape, a convex shape, and the like. In some cases the configuration of the textured region can function to direct or focus electromagnetic radiation into the semiconductor substrate, and in other cases the configuration of the textured region can function to direct or focus electromagnetic radiation away from the semiconductor substrate.

As is shown in FIG. 5, a lens 50 can be coupled to the semiconductor substrate 12 on a side facing incoming electromagnetic radiation. Thus the lens can focus the electromagnetic radiation into the semiconductor substrate. In those aspects having circuitry or other structures disposed on the incoming electromagnetic

radiation surface, the lens can further focus light around such structures, thereby reducing optical scattering and noise.

As is shown in FIG. 6, a textured region 60 is located on the semiconductor substrate 12 adjacent to the multiple doped regions 14, 16. The textured region can be --> associated with at least one of the doped regions as is shown, or the textured region can be distinct from the doped regions (not shown). Electromagnetic radiation can enter the photosensitive device at the side adjacent the doped regions, or alternatively at the side opposite the doped regions.

FIGs. 7-11 show various steps in the manufacture of a photosensitive pixel according to aspects of the present disclosure. FIG. 7 shows a cross-section of a front side illumination (FSI) photosensitive pixel device. The photosensitive pixel device can include a semiconductor substrate 72, and can be referred to as bulk semiconductor material. The semiconductor substrate includes at least one doped region 74 that can be doped with an electron donating or hole donating species to cause the region to become more positive or negative in polarity as compared to the semiconductor substrate. In one aspect, for example, the doped region can be p doped. In another aspect the doped region can be n doped. A highly doped region 76 can be formed on or near the doped region to create a pinned diode. In one example, the semiconductor substrate can be negative in polarity, and the doped region and the highly doped region can be doped with p+ and n-dopants respectively. In some aspects, variations of n(—), n(-), n(+), n(++), p(—), p(-), p(+), or p(++), type doping of the regions can be used. It should be noted that in one aspect the highly doped region can be the textured region. In other words, textured surface features can be formed on or in the highly doped region. The device of FIG. 7 can further include various metal regions 78, at least one via 80, a passivation layer 82, trench isolation 84, and an electrical transfer element 86. Trench isolation elements can maintain pixel to pixel uniformity by reducing optical and electrical crosstalk. The trench isolation can be shallow (FIG. 7) or deep (FIG. 12) trench isolation. The trench isolation can include various materials, including, without limitation, dielectric materials, reflective materials, conductive materials, light diffusing features, and the like. These trench isolation regions can be configured to reflect incident light until it is absorbed, thereby increase the effective absorption length of the device.

As is shown in FIG. 8, a carrier substrate or carrier wafer 88 can be coupled to the photosensing pixel. In one aspect, the carrier substrate can be disposed on the passivation layer 82, although the carrier substrate can be disposed on any surface of the device. In one aspect, for example, the carrier substrate can be disposed on the semiconductor substrate (not shown). The carrier substrate can be coupled to the --> photosensing pixel by various techniques, and any such coupling mechanism is within the present scope. In one aspect, for example, the coupling can occur by way of a bonding layer or adhesive layer disposed on the device, for example, on the passivation layer. The support substrate can provide support to the semiconductor device both during and after manufacture, depending on whether or not the support is removed. The carrier substrate can be made of a semiconductor material that is the same or similar to the bulk semiconductor material, or it can be made of a different material.

As is shown in FIG. 9, a textured region 90 is coupled to the semiconductor substrate 72 opposite the doped regions 74,76. Thus light entering from the direction of the doped regions passes through the semiconductor substrate prior to contacting the textured region. The textured region can be disposed across an entire surface of the semiconductor substrate, as is shown in FIG. 9, or it can be disposed on one or more discrete regions (not shown).

As is shown in FIG. 10, an additional carrier support substrate 100 can be coupled to the device on an opposing side from the carrier support substrate 88. The additional carrier support substrate can be utilized for a variety of purposes, including providing additional support to the device, facilitating the removal of the first carrier support substrate, and the like. A reflective layer 102 can be disposed between the textured region 90 and the carrier support substrate. Thus the reflective layer can reflect electromagnetic radiation that passes through the textured region back toward the semiconductor substrate 72, thus reducing optical loss and backscattering. Thus, in some aspects a reflective layer can increase the quantum efficiency of the device. The reflective layer material can be any reflective material that can be incorporated into such a device. Nonlimiting examples can include materials such as silver, aluminum, and the like.

As is shown in FIG. 11, the carrier support substrate can be removed to expose the passivation layer 82 or any other material layer that was previously covered by the carrier support substrate. The additional carrier

substrate 100 can be maintained in the device, removed from the device, or thinned to reduce the thickness of the substrate depending on the intended use of the device. The removal of material from the device, including the carrier support substrate and the additional carrier substrate, can be accomplished by a variety of methods including, without limitation, etching, chemical mechanical polishing, ion implanting (i.e. smart cut), and the like. --> Various types of trench isolation are contemplated, and any such isolation is considered to be within the present scope. As has been described, trench isolation can be shallow (FIG. 7, 84) or deep (FIG. 12, 120) trench isolation. The trench isolation can also include depths between shallow and deep, depending on the device design. Trench isolation can include dielectric materials, reflective materials, conductive materials, and combinations thereof, including textured regions and other light diffusing features. Thus the trench isolation layer can be configured to reflect incident electromagnetic radiation, in some cases until it is absorbed, thereby increasing the effective absorption length of the device. Additionally, in some aspects pillar features can be incorporated into pixels by thinning or removing material from the semiconductor substrate using deep trench isolation and etching techniques. As is shown in FIG. 13, the textured region 130 can have a nonparallel surface with respect to the semiconductor substrate 72 as has been described. This nonparallel morphology, when included with the deep trench isolation 120, can effectively focus electromagnetic radiation into the semiconductor substrate from multiple sides. It is also contemplated, that a non-bulk material can be formed or disposed near a doped region in the device. The addition of the non-bulk material can allow for electromagnetic radiation diffusing features to be formed on or in the non-bulk material. A metal layer defining an aperture can also be included in one aspect of the present disclosure. The metal layer can be formed near the doped regions and can have a light entering region that defines an aperture. This light entering region can also include an antireflecting material.

Fig. 14 shows a photosensitive imager comprising two photosensitive pixels 140. Each photosensitive pixel includes a boundary region 142 that can include metal circuitry and a textured region 144. Each photosensitive pixel can include at least one transistor 146 or other electrical transfer element. Additional read out and circuitry elements 148 can be utilized and shared by both photosensitive pixels.

Turning to FIG. 15, a backside illuminated (BSI) photosensitive pixel according to one aspect present disclosure is provided. A lens 150 and an anti-reflective coating 152 are disposed on the backside of the pixel following thinning and trench isolation. A color filter 154 can be optically coupled to the lens to allow specific wavelengths filtering of the electromagnetic radiation. A textured region 156 can be coupled to the semiconductor substrate 72 opposite the lens in order to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes --> through to the front side of the pixel. Thus the electromagnetic radiation can be focused within the semiconductor substrate to the combined action of the textured region and the trench isolation 120

Fig. 16 shows a front side illuminated (FSI) imager according to another aspect of the present disclosure. A lens 160 and an antireflecting passivation layer on 62 are coupled to the front side of the pixel. A textured region 90 and a reflecting layer 102 are coupled to the semiconductor substrate 72 opposite the lens to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes through the semiconductor substrate. An aperture 164 formed in a metal or other reflective material layer 166 can increase the effectiveness of the optical cavity. Thus the lens focuses electromagnetic radiation through the aperture.

In other aspects of the present disclosure, various methods of making photosensitive diodes, pixels, and imagers, are contemplated. In one aspect, as is shown in FIG. 17, a method of making a photosensitive imager device can include forming a textured region on a semiconductor substrate having multiple doped regions forming a least one junction, wherein the textured region is formed in a position to interact with electromagnetic radiation 170. The method also includes coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction 172. In one aspect, multiple pixels can be associated together to form an imager. A passivation layer can also be disposed on the photosensitive imager device to protect and/or reduce the dark current of the device.

In another aspect of the present disclosure, a method for making a photosensitive diode is provided. Such a method can include forming at least one cathode and at least one anode on a surface of a semiconductor substrate, coupling a textured region to the semiconductor substrate,

and coupling a support substrate to the semiconductor substrate. The textured region can be located adjacent to the anode and cathode, opposite the anode and cathode, or both adjacent and opposite the anode and cathode. An electrical transfer on the can be electrically coupled to at least one of the anode and cathode to form a photosensitive pixel. In another aspect, the semiconductor substrate can be thinned to improve the response rate and/or speed of the device. A passivation layer can also be disposed on the photosensitive diode to protect and/or reduce the dark current of the device. An additional support substrate can be attached to the device to provide additional support. In one aspect, the --> additional support substrate can be located on the opposite side of the photosensitive diode from the support substrate. The support substrate can subsequently be removed to allow for further processing.

Of course, it is to be understood that the above-described arrangements are only illustrative of the application of the principles of the present disclosure.

Numerous modifications and alternative arrangements may be devised by those skilled in the art without departing from the spirit and scope of the present disclosure and the appended claims are intended to cover such modifications and arrangements. Thus, while the present disclosure has been described above with particularity and detail in connection with what is presently deemed to be the most practical embodiments of the disclosure, it will be apparent to those of ordinary skill in the art that numerous modifications, including, but not limited to, variations in size, materials, shape, form, function and manner of operation, assembly and use may be made without departing from the principles and concepts set forth herein.

Claims

What is claimed is: 1. A photosensitive imager device, comprising:

a semiconductor substrate having multiple doped regions forming a least one junction;

a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation; and

an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction.

2. The device of claim 1, wherein the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation.

3. The device of claim 1, wherein interacting with electromagnetic radiation further includes increasing the semiconductor substrate's effective absorption length as compared to a semiconductor substrate lacking a textured region.

4. The device of claim 1, wherein the transfer element is selected from the group consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.

5. The device of claim 1, further comprising a reflective layer coupled to the semiconductor substrate and positioned to maintain the electromagnetic radiation in the semiconductor substrate.

6. The device of claim 1, wherein the textured region is positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions.

7. The device of claim 6, wherein the textured region has a surface morphology operable to direct electromagnetic radiation into or out of the semiconductor substrate. -->

8. The device of claim 7, wherein the surface morphology of the textured region relative to the semiconductor substrate is a member selected from the group consisting of sloping, pyramidal, inverted pyramidal, spherical, parabolic, asymmetric, symmetric, and combinations thereof.

9. The device of claim 1, wherein the textured region is positioned on a surface of the semiconductor substrate that is adjacent the multiple doped regions.

10. The device of claim 9, further comprising an additional textured region positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions.

11. The device of claim 1, wherein the textured region is coupled directly to at least one of the multiple doped regions.

12. The device of claim 1, wherein the textured region includes surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof.

13. The device of claim 12, wherein surface features include a member selected from the group consisting of

cones, pillars, pyramids, microlenses, quantum dots, inverted features, and combinations thereof.

14. The device of claim 1, wherein the textured region has been formed by a process selected from the group consisting of lasing, chemical etching, nano imprinting, material deposition, and combinations thereof.

15. The device of claim 1, further comprising a lens optically coupled to the semiconductor substrate and positioned to focus incident electromagnetic radiation into the semiconductor substrate.

16. A photosensitive imager array, comprising at least two photosensitive imager devices of claim 1. -->

17. The array of claim 16, further comprising at least one trench isolation positioned between the at least two photosensitive imager device.

18. A method of making a photosensitive imager device, comprising:

forming a textured region on a semiconductor substrate, wherein the semiconductor substrate has multiple doped regions forming a least one junction, and wherein the textured region is formed in a position to interact with electromagnetic radiation; and

coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction .

19. The method of claim 18, wherein forming the textured region is by a process selected from the group consisting of lasing, chemical etching, nano imprinting, material deposition, and combinations thereof.

20. The method of claim 18, wherein forming the textured region includes irradiating a target region with laser radiation to form surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof.

21. The method of claim 20, wherein irradiating the target region includes exposing the laser radiation to a dopant such that the irradiation incorporates the dopant into the textured region.

22. The method of claim 20, wherein the irradiation is performed using a pulsed laser including a member selected from the group consisting of a femtosecond laser, a picosecond laser, a nanosecond laser, and combinations thereof.

23. The method of claim 18, further comprising tuning an electrical response of the photosensitive imager device.

24. The method of claim 23, wherein tuning includes forming surface features to have dimensions that selectively diffuse or selectively absorb a desired wavelength of electromagnetic radiation. -->

25. The method of claim 23, wherein tuning is accomplished through a factor selected from the group consisting of placement of the textured region, material type of the textured region, thickness of the textured region, dopant type of the textured region, doping profile of the texture region, doping profile of the semiconductor substrate, thickness of the substrate, and combinations thereof.

26. The method of claim 18, wherein the transfer element is selected from the group consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.

27. The method of claim 18, further comprising annealing the semiconductor substrate to a temperature of from about 300° C to about 1 100° C.

28. A photosensitive imager device, comprising:

a semiconductor substrate having multiple doped regions forming a least one junction;

a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation; and

at least 4 transistors coupled to the semiconductor substrate and with at least one of the transistors electrically coupled to the at least one junction.

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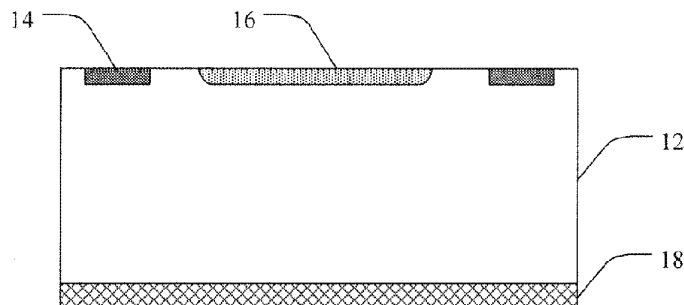


FIG. 1

(57) Abstract: Photosensitive devices and associated methods are provided. In one aspect, for example, a photosensitive imager device can include a semiconductor substrate having multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. In one aspect, the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation. In another aspect, interacting with electromagnetic radiation further includes increasing the semiconductor substrate's effective absorption wavelength as compared to a semiconductor substrate lacking a textured region.

WO 2011/035188 A2

PHOTOSENSITIVE IMAGING DEVICES AND ASSOCIATED METHODS**PRIORITY DATA**

This application claims the benefit of U.S. Provisional Patent Application
5 Serial No. 61/243,434, filed on September 17, 2009, U.S. Provisional Patent
Application Serial No. 61/3 11,004 filed on March 5, 2010, and U.S. Provisional
Patent Application Serial No. 61/3 11,107, filed on March 5, 2010, each of which is
incorporated herein by reference.

BACKGROUND

The interaction of light with semiconductor materials has been a significant
innovation. Silicon imaging devices are used in various technologies, such as digital
cameras, optical mice, video cameras, cell phones, and the like. Charge-coupled
devices (CCDs) were widely used in digital imaging, and were later improved upon
15 by complementary metal-oxide-semiconductor (CMOS) imagers having increased
performance. CMOS sensors are typically manufactured from silicon and can convert
visible incident light into a photocurrent and ultimately into a digital image. Silicon-
based technologies for detecting infrared incident electromagnetic radiation have been
problematic, however, because silicon is an indirect bandgap semiconductor having a
20 bandgap of about 1.1eV. Thus the absorption of electromagnetic radiation having
wavelengths of greater than about 1100 nm is, therefore, very low in silicon.

SUMMARY

The present disclosure provides photosensitive devices and associated
25 methods. In one aspect, for example, a photosensitive imager device can include a
semiconductor substrate having multiple doped regions forming at least one junction,
a textured region coupled to the semiconductor substrate and positioned to interact
with electromagnetic radiation, and an electrical transfer element coupled to the
semiconductor substrate and operable to transfer an electrical signal from the at least
30 one junction. In one aspect, the textured region is operable to facilitate generation of
an electrical signal from the detection of infrared electromagnetic radiation. In
another aspect, interacting with electromagnetic radiation further includes increasing
the semiconductor substrate's effective absorption length as compared to a
semiconductor substrate lacking a textured region. In one specific aspect, the transfer

element is selected from the group consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.

The textured region can be positioned in a variety of locations relative to the doped regions. In one aspect, for example, the textured region is positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions. In one specific aspect, the textured region has a surface morphology operable to direct electromagnetic radiation into or out of the semiconductor substrate. The surface morphology of the textured region relative to the semiconductor substrate can include a variety of configurations, including, without limitation, sloping, pyramidal, inverted pyramidal, spherical, parabolic, asymmetric, symmetric, and the like, including combinations thereof.

In another aspect, the textured region can be positioned on a surface of the semiconductor substrate that is adjacent the multiple doped regions. In a more specific aspect, an additional textured region can be positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions. In this manner, textured regions can thus be positioned adjacent to multiple doped regions and opposite the multiple doped regions.

Various aspects of the textured region can vary depending on the desired configuration of the device. In one aspect, however, the textured region includes surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof. Numerous surface feature morphologies are contemplated, nonlimiting examples of which include cones, pillars, pyramids, microlenses, quantum dots, inverted features, and combinations thereof. Additionally, the textured region can be formed by a variety of processes. Nonlimiting examples of such texturing processes can include lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, and combinations thereof.

Additional layers and/or structures can be included in various devices according to aspects present disclosure. In one aspect, for example, a reflective layer can be coupled to the semiconductor substrate and positioned to maintain the electromagnetic radiation in the semiconductor substrate. In another aspect, a lens can be optically coupled to the semiconductor substrate and positioned to focus incident electromagnetic radiation into the semiconductor substrate.

In another aspect of the present disclosure, a method of making a photosensitive imager device is provided. Such a method can include forming a textured region on a semiconductor substrate having multiple doped regions forming a least one junction, wherein the textured region is formed in a position to interact with electromagnetic radiation and coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction.

In one aspect, the photosensitive imager device can be tuned to be selected to filter out specific electromagnetic radiation wavelengths. In one specific aspect, tuning includes forming surface features to have dimensions that selectively diffuse or selectively absorb a desired wavelength of electromagnetic radiation. In another aspect, tuning is accomplished through a factor selected from the group consisting of placement of the textured region, material type and/or thickness of the textured region, dopant type of the textured region, doping profile of the texture region, dopant profile of the semiconductor substrate, material type and/or thickness of the semiconductor substrate, and combinations thereof.

In another aspect of the present disclosure, a photosensitive imager device is provided. Such a device can include a semiconductor substrate having multiple doped regions forming a least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and at least 4 transistors coupled to the semiconductor substrate and with at least one of the transistors electrically coupled to the at least one junction.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic view of a photosensitive device in accordance with one aspect of the present disclosure;

FIG. 2 is a schematic view of a photosensitive device in accordance with another aspect of the present disclosure;

FIG. 3 is a schematic view of a photosensitive device in accordance with yet another aspect of the present disclosure;

FIG. 4 is a schematic view of a photosensitive device in accordance with a further aspect of the present disclosure;

FIG. 5 is a schematic view of a photosensitive device in accordance with yet a further aspect of the present disclosure;

FIG. 6 is a schematic view of a photosensitive device in accordance with another aspect of the present disclosure;

FIG. 7 is a schematic view of a photosensitive pixel device in accordance with yet another aspect of the present disclosure;

5 FIG. 8 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

FIG. 9 is a schematic view of a photosensitive pixel device in accordance with yet a further aspect of the present disclosure;

10 FIG. 10 is a schematic view of a photosensitive pixel device in accordance with another aspect of the present disclosure;

FIG. 11 is a schematic view of a photosensitive pixel device in accordance with yet another aspect of the present disclosure;

FIG. 12 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

15 FIG. 13 is a schematic view of a photosensitive pixel device in accordance with another aspect of the present disclosure;

FIG. 14 is a schematic view of a photosensitive imager device in accordance with yet another aspect of the present disclosure;

20 FIG. 15 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

FIG. 16 is a schematic view of a photosensitive pixel device in accordance with another aspect of the present disclosure; and

FIG. 17 is a depiction of a method of making a photosensitive imager device in accordance with yet another aspect of the present disclosure.

25

DETAILED DESCRIPTION

Before the present disclosure is described herein, it is to be understood that this disclosure is not limited to the particular structures, process steps, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by
30 those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting.

Definitions

The following terminology will be used in accordance with the definitions set forth below.

It should be noted that, as used in this specification and the appended claims, the singular forms "a," and, "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a dopant" includes one or more of such dopants and reference to "the layer" includes reference to one or more of such layers.

As used herein, the term "low oxygen content" refers to any material having an interstitial oxygen content that is less than or equal to about 60 ppm atomic.

As used herein, the terms "disordered surface" and "textured surface" can be used interchangeably, and refer to a surface having a topology with nano- to micron-sized surface variations formed by the irradiation of laser pulses. While the characteristics of such a surface can be variable depending on the materials and techniques employed, in one aspect such a surface can be several hundred nanometers thick and made up of nanocrystallites (e.g. from about 10 to about 50 nanometers) and nanopores. In another aspect, such a surface can include micron-sized structures (e.g. about 2 μm to about 60 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 500 μm .

As used herein, the term "fluence" refers to the amount of energy from a single pulse of laser radiation that passes through a unit area. In other words, "fluence" can be described as the energy density of one laser pulse.

As used herein, the terms "surface modifying" and "surface modification" refer to the altering of a surface of a semiconductor material using laser radiation. In one specific aspect, surface modification can include processes using primarily laser radiation or laser radiation in combination with a dopant, whereby the laser radiation facilitates the incorporation of the dopant into a surface of the semiconductor material. Accordingly, in one aspect surface modification includes doping of a semiconductor material.

As used herein, the term "target region" refers to an area of a semiconductor material that is intended to be doped or surface modified using laser radiation. The target region of a semiconductor material can vary as the surface modifying process progresses. For example, after a first target region is doped or surface modified, a second target region may be selected on the same semiconductor material.

As used herein, the term "detection" refers to the sensing, absorption, and/or collection of electromagnetic radiation.

As used herein, the term "substantially" refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is "substantially" enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use of "substantially" is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is "substantially free of" particles would either completely lack particles, or so nearly completely lack particles that the effect would be the same as if it completely lacked particles. In other words, a composition that is "substantially free of" an ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

As used herein, the term "about" is used to provide flexibility to a numerical range endpoint by providing that a given value may be "a little above" or "a little below" the endpoint.

As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of "about 1 to about 5" should be interpreted to include

not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

- 5 This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

The Disclosure

- 10 Electromagnetic radiation can be present across a broad wavelength range, including visible range wavelengths (approximately 350nm to 800nm) and non-visible wavelengths (longer than about 800nm or shorter than 350 nm). The infrared spectrum is often described as including a near infrared portion of the spectrum including wavelengths of approximately 800 to 1300 nm, a short wave infrared
15 portion of the spectrum including wavelengths of approximately 1300 nm to 3 micrometers, and a mid to long wave infrared (or thermal infrared) portion of the spectrum including wavelengths greater than about 3 micrometers up to about 30 micrometers. These are generally and collectively referred to herein as "infrared" portions of the electromagnetic spectrum unless otherwise noted.

- 20 Traditional silicon photodetecting imagers have limited light absorption/detection properties. For example, infrared light is mostly transparent to such silicon based detectors. While other materials (e.g. InGaAs) can be used to detect infrared electromagnetic radiation having wavelengths greater than about 1000 nm, silicon is still commonly used because it is relatively cheap to manufacture and can be
25 used to detect wavelengths in the visible spectrum (i.e. visible light, 350 nm - 800 nm). Traditional silicon materials require substantial absorption depths to detect photons having wavelengths longer than approximately 700 nm. While visible light can be absorbed at relatively shallow depths in silicon, absorption of longer wavelengths (e.g. 900 nm) in silicon of a standard wafer depth (e.g. approximately
30 750 μm) is poor if at all. The devices of the present disclosure increase the absorption of semiconductor materials by decreasing the effective absorption length to longer wavelengths as compared to traditional materials. For example, the absorption depth of silicon can be reduced such that these longer wavelengths can be absorbed at depths of less than or equal to about 850 μm . In other words, by decreasing the

effective absorption length these devices are able to absorb longer wavelengths (e.g. >1000 nm for silicon) within a thin semiconductor material. In addition to increasing the effective absorption length, the response rate or response speed can also be increased using thinner semiconductor materials.

5 The present disclosure additionally provides broadband photosensitive diodes, pixels, and imagers capable of detecting visible as well as infrared electromagnetic radiation, including associated methods of making such devices. A photosensitive diode can include a semiconductor substrate having multiple doped regions forming at least one junction, and at least one textured region coupled to the semiconductor
10 substrate and positioned to interact with electromagnetic radiation. In one aspect the multiple doped regions can include at least one cathode region and at least one anode region. In some aspects, doped regions can include an n-type dopant and/or a p-type dopant as is discussed below, thereby creating a p-n junction. In other aspects, a photosensitive device can include an i-type region to form a p-i-n junction.

15 A photosensitive pixel can include a semiconductor substrate having multiple doped regions forming at least one junction, at least one textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. A photosensitive imager
20 can include multiple photosensitive pixels. Additionally, an electrical transfer element can include a variety of devices, including without limitation, transistors, sensing nodes, transfer gates, transfer electrodes, and the like.

 Photosensitive or photodetecting imagers include photodiodes or pixels that are capable of absorbing electromagnetic radiation within a given wavelength range.
25 Such imagers can be passive pixel sensors (PPS), active pixel sensors (APS), digital pixel sensor imagers (DPS), or the like, with one difference being the image sensor read out architecture. For example, a semiconducting photosensitive imager can be a three or four transistor active pixel sensor (3T APS or 4T APS). Various additional components are also contemplated, and would necessarily vary depending on the
30 particular configuration and intended results. As an example, a 4T configuration can additionally include, among other things, a transfer gate, a reset, a source follower, and row select transistors. Additionally, devices having greater than 4 transistors are also within the present scope.

Photosensitive imagers can be front side illumination (FSI) or back side illumination (BSI) devices, and there are advantages and disadvantages to both architecture types. In a typical FSI imager, incident light enters the semiconductor device by first passing by transistors and metal circuitry. The light, however, can
5 scatter off of the transistors and circuitry prior to entering the light sensing portion of the imager, thus causing optical loss and noise. A lens can be disposed on the top side of a FSI pixel to direct and focus the incident light to the light sensing active region of the device, thus partially avoiding the circuitry. In one aspect the lens can be a u-lens. BSI imagers, on the other hand, are configured to have the depletion region of the
10 junction extending to the opposite side of the device. In one aspect, for example, incident light enters the device via the light sensing portion and is mostly absorbed prior to reaching the circuitry. BSI designs allow for smaller pixel architecture and a high fill factor for the imager. As mentioned, the present disclosure can be adapted for either configuration. It should also be understood that devices according to
15 aspects of the present disclosure can be incorporated into complimentary metal-oxide-semiconductor (CMOS) imager architectures or charge-coupled device (CCD) imager architectures.

In one aspect, as is shown in FIG. 1, a photosensitive diode 10 can include a semiconductor substrate 12 having multiple doped regions 14, 16 forming at least one
20 junction, and at least one textured region 18 coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation. The different doped regions can have the same doping profile or different doping profiles, depending on the device. Such an architecture is a FSI design where light enters the semiconductor substrate from the direction of the multiple doped regions. While the device shown in
25 FIG. 1 contains three doped regions, it should be noted that aspects containing one or more doped regions are considered to be within the present scope. Additionally, the semiconductor substrate can be doped, and thus can be considered to be a doped region in some aspects. It should also be noted that the photosensitive diode can be configured with a BSI architecture, and thus electromagnetic radiation would enter the
30 semiconductor substrate from the direction of the textured region.

The various devices according to aspects of the present disclosure can exhibit increased quantum efficiency over traditional photosensitive devices. Any increase in the quantum efficiency makes a large difference in the signal to noise ratio. More complex structures can provide not only increased quantum efficiency but also good

uniformity from pixel to pixel. In addition, devices of the present disclosure exhibit increased responsivity as compared to traditional photosensitive devices. For example, in one aspect the responsivity can be greater than or equal to 0.8A/W for wavelengths greater than 1000 nm for semiconductor substrate that is less than 100
5 μm thick.

Photosensitive imagers can be maintained under constant conditions (fixed voltage or current) to provide enhanced linearity and uniformity. Connections between the imager and the underlying device layers can be achieved using vias fabricated from a refractory metal, such as tungsten or tantalum. Placing storage
10 elements under the imager may provide various photonic benefits. For example, the entire pixel array maybe dedicated to signal processing. This may enable higher performance by permitting access to low level pixel signals. Furthermore, massively parallel operations can be performed by pixel processors. For example, analog to digital conversion, noise reduction (ie., true correlated double sampling), power
15 conditioning, nearest neighbor pixel processing, compression, fusion, and color multiplexing operations can be performed.

A variety of semiconductor materials are contemplated for use with the devices and methods according to aspects of the present disclosure. Non-limiting examples of such semiconductor materials can include group IV materials,
20 compounds and alloys comprised of materials from groups II and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can include silicon carbide (SiC) and silicon germanium (SiGe). In one
25 specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum
30 gallium arsenide, and combinations thereof.

Exemplary combinations of group II-VI materials can include cadmium selenide (CdSe), cadmium sulfide (CdS), cadmium telluride (CdTe), zinc oxide (ZnO), zinc selenide (ZnSe), zinc sulfide (ZnS), zinc telluride (ZnTe), cadmium zinc

telluride (CdZnTe, CZT), mercury cadmium telluride (HgCdTe), mercury zinc telluride (HgZnTe), mercury zinc selenide (HgZnSe), and combinations thereof.

Exemplary combinations of group III-V materials can include aluminum antimonide (AlSb), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum phosphide (AlP), boron nitride (BN), boron phosphide (BP), boron arsenide (BAS),
 5 gallium antimonide (GaSb), gallium arsenide (GaAs), gallium nitride (GaN), gallium phosphide (GaP), indium antimonide (InSb), indium arsenide (InAs), indium nitride (InN), indium phosphide (InP), aluminum gallium arsenide (AlGaAs, $Al_xGa_{1-x}As$), indium gallium arsenide (InGaAs, $In_xGa_{1-x}As$), indium gallium phosphide (InGaP),
 10 aluminum indium arsenide (AlInAs), aluminum indium antimonide (AlInSb), gallium arsenide nitride (GaAsN), gallium arsenide phosphide (GaAsP), aluminum gallium nitride (AlGaN), aluminum gallium phosphide (AlGaP), indium gallium nitride (InGaN), indium arsenide antimonide (InAsSb), indium gallium antimonide (InGaSb), aluminum gallium indium phosphide (AlGalnP), aluminum gallium arsenide
 15 phosphide (AlGaAsP), indium gallium arsenide phosphide (InGaAsP), aluminum indium arsenide phosphide (AlInAsP), aluminum gallium arsenide nitride (AlGaAsN), indium gallium arsenide nitride (InGaAsN), indium aluminum arsenide nitride (InAlAsN), gallium arsenide antimonide nitride (GaAsSbN), gallium indium nitride arsenide antimonide (GalnNAsSb), gallium indium arsenide antimonide
 20 phosphide (GalnAsSbP), and combinations thereof.

The semiconductor material can be of any thickness that allows electromagnetic radiation detection and conversion functionality, and thus any such thickness of semiconductor material is considered to be within the present scope. In some aspects the laser processed region of the semiconductor increases the efficiency
 25 of the device such that the semiconductor material can be thinner than has previously been possible. Decreasing the thickness of the semiconductor reduces the amount of semiconductor material required to make such a device. In one aspect, for example, the semiconductor material has a thickness of from about 500 nm to about 50 μm . In another aspect, the semiconductor material has a thickness of less than or equal to
 30 about 500 μm . In yet another aspect, the semiconductor material has a thickness of from about 1 μm to about 10 μm . In a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 750 μm . In yet a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 100 μm .

Additionally, various types of semiconductor material are contemplated, and any such material that can be incorporated into an electromagnetic radiation detection device is considered to be within the present scope. In one aspect, for example, the semiconductor material is monocrystalline. In another aspect, the semiconductor material is multicrystalline. In yet another aspect, the semiconductor material is microcrystalline. It is also contemplated that the semiconductor material can be amorphous. Specific nonlimiting examples include amorphous silicon or amorphous selenium.

The semiconductor materials of the present disclosure can also be made using a variety of manufacturing processes. In some cases the manufacturing procedures can affect the efficiency of the device, and may be taken into account in achieving a desired result. Exemplary manufacturing processes can include Czochralski (Cz) processes, magnetic Czochralski (mCz) processes, Float Zone (FZ) processes, epitaxial growth or deposition processes, and the like. Whether or not low oxygen content is desired in the device can also affect the choice of a manufacturing process for the semiconductor material. Various processes produce semiconductor materials containing varying amounts of oxygen, and as such, some applications having more stringent tolerances with respect to oxygen levels may benefit more from specific manufacturing procedures as compared to others. For example, during CZ crystal growth oxygen from the containment vessel, usually a quartz crucible, can become incorporated into the crystal as it is pulled. Additionally, other sources of oxygen contamination are also possible with the CZ process. Such contamination may be reduced, however, through the use of non oxygen-containing crucible materials, as well as the development of other crystal growth methods that do not utilize a crucible. One such process is the FZ process.

Materials grown with the CZ method can also be made to have lowered oxygen concentration through enhancements to the crystal growth process, such as growing the crystal in the presence of a magnetic field (i.e. the mCz process). Also, gettering techniques can be employed to reduce the impact of oxygen or other impurities on the finished device. These gettering techniques can include thermal cycles to liberate or nucleate impurities, or selective ion implantation of species to serve as gettering sites for the impurities. For example, oxygen concentrated in the semiconductor can be removed by the performing a furnace cycle to form a denuded zone. During heating with an inert gas, oxygen near the surface of the semiconductor

diffuses out of the material. During the furnace cycle but after the denuding step, nucleating and growing steps may be performed. Nucleating sites for precipitates are formed during the nucleating step, and the precipitates are grown from the nucleating sites during a growing step. The precipitates are formed from interstitial oxygen
5 within the bulk of the semiconductor material and beneath the denuded zone. The precipitation of oxygen in the bulk of the semiconductor material can be desired because such precipitates can act as gettering sites. Such precipitate formation can also be performed to "lock up" interstitial oxygen into the precipitates and reduce the likelihood that such oxygen can migrate from the bulk of the semiconductor material
10 into the denuded zone.

In those aspects where low oxygen content of the device is desired, further processing of the semiconductor material can be performed so as to minimize the introduction of oxygen. Oxygen can exist in different states or at different sites (for example, interstitially or substitutionally) within a semiconductor such as silicon,
15 dependent upon the thermal processing the semiconductor has received. If the semiconductor is subjected to temperatures higher than, for example, about 1000° C, oxygen can form aggregates or clusters that serve as defect sites in the crystal lattice. These sites may result in trap states and a reduction in carrier lifetime within the semiconductor material and device can occur. At lower temperatures (for example,
20 around 400° C to 700° C), oxygen can behave as electrically active thermal donors. Thus, oxygen can have a negative impact on carrier lifetime and on carrier mobility. In a device fabricated to have photoconductive gain, the presence of oxygen causing reduced carrier lifetime may result in reduced levels of photoconductive gain.

It may be beneficial, therefore, to produce semiconductor devices such that a
25 low oxygen content is obtained or maintained. This can be accomplished in a variety of ways, including using semiconductor materials having low levels of oxygen contained therein to begin with, processing these materials in a manner that minimizes the uptake of oxygen into the semiconductor lattice, and utilizing techniques that eliminate or reduce oxygen that may be present in the semiconductor. Such processes
30 and techniques can include, for example, annealing the semiconductor material and any laser treated region to lower temperatures as compared to previous annealing procedures. Annealing processes are discussed more fully below.

Additionally, texture processing of the semiconductor material and/or any annealing process can be performed in a substantially oxygen-depleted environment

in order to minimize the introduction of oxygen into the semiconductor. An oxygen-depleted or substantially oxygen-depleted environment can include a variety of environments. In one aspect, for example, the oxygen-depleted environment can be an environment whereby oxygen from the air or other sources has been replaced with a gas or other fluid containing little to no oxygen. In another aspect, processing can occur in a vacuum environment, and thus contain little to no oxygen. Additionally, oxygen-containing materials or materials that introduce oxygen into the semiconductor, such as, for example, quartz crucibles, can be avoided. As a practical matter, the term "oxygen-depleted environment" can be used to describe an environment with low levels of oxygen, provided a semiconductor material can be processed therein within the desired tolerances. Thus, environments having low oxygen, or little to no oxygen, are environments in which a semiconductor can be processed as a low-oxygen content semiconductor while maintaining oxygen levels within the tolerances of the present disclosure. In one aspect, an oxygen-depleted environment can be an oxygen-free environment. Further details regarding low-oxygen content semiconductor materials can be found in US Patent Application No. 12/771848, filed on April 30, 2010, which is incorporated herein by reference.

The semiconductor material can have varying levels of interstitial oxygen depending on the desired efficiency of the device. In some aspects, oxygen content may be of no concern, and thus any level of oxygen within the lattice is acceptable. In other aspects, a low oxygen content is desired. In one aspect a semiconductor material can have an oxygen content that is less than or equal to about 50 ppm atomic. In another aspect, a semiconductor material can have an oxygen content that is less than or equal to about 30 ppm atomic. In yet another aspect, the semiconductor material can have an oxygen content less than or equal to about 10 ppm atomic. In another aspect the semiconductor can have an oxygen content less than about 5 ppm atomic. In yet another aspect the semiconductor can have an oxygen content less than about 1 ppm atomic.

As has been described, the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device. The textured region can include surface features to increase the effective absorption length of the photosensitive pixel. The surface features can be cones, pyramids, pillars, protrusions, microlenses, quantum dots, inverted features and the like. Factors such

as manipulating the feature sizes, dimensions, material type, dopant profiles, texture location, etc. can allow the diffusing region to be tunable for a specific wavelength. In one aspect, tuning the device can allow specific wavelengths or ranges of wavelengths to be absorbed. In another aspect, tuning the device can allow specific
5 wavelengths or ranges of wavelengths to be reduced or eliminated via filtering.

Tuning can also be accomplished through the location of the texture region within the device, modifying the dopant profile(s) of regions within the device, dopant selection, and the like. Additionally, material composition near the textured region can create a wavelength specific photosensing pixel device. It should be noted that a
10 wavelength specific photosensing pixel can differ from one pixel to the next, and can be incorporated into an imaging array. For example a 4 x 4 array can include a blue pixel, a green pixel, a red pixel, and infrared light absorbing pixel, or a blue pixel, two green pixels, and a red pixel.

Textured regions according to aspects of the present disclosure can allow a
15 photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared). Such internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor substrate. This increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.

The textured region can be formed by various techniques, including lasing,
20 chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, additional material deposition, and the like. For example, pillar features can be incorporated into pixels by thinning or removing material from the backside of a FSI semiconductor substrate by using deep trench isolation and etching techniques. In
25 one aspect material can be removed to a thickness of about 20 μm . Anisotropic etching can be used to produce a sloping backside pyramid structure, spherical, structure parabolic structure, a lens structure with reflectors, and the like. Such features on the backside of pillars will also serve to diffuse and reflect electromagnetic radiation.

In one aspect, the texturing process can be performed during the manufacture
30 of the photosensitive device. In another aspect, the texturing process can be performed on a photosensitive device that has previously been made. For example, a CMOS, CCD, or other photosensitive element can be textured following manufacture. In this case, material layers may be removed from the photosensitive element to

expose the semiconductor substrate or bulk material upon which a textured region may be formed.

One effective method of producing a textured region is through laser processing. Such laser processing allows discrete locations of the semiconductor substrate to be textured. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope. Laser treatment or processing can allow, among other things, enhanced absorption properties and thus increased electromagnetic radiation focusing and detection. The laser treated region can be associated with the surface nearest the impinging electromagnetic radiation, or the laser treated surface can be associated with a surface opposite in relation to impinging electromagnetic radiation, thereby allowing the radiation to pass through the semiconductor material before it hits the laser treated region.

In one aspect, for example, a target region of the semiconductor material can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Patents 7,057,256, 7,354,792 and 7,442,629, which are incorporated herein by reference in their entireties. Briefly, a surface of a semiconductor material is irradiated with laser radiation to form a textured or surface modified region. Such laser processing can occur with or without a dopant material. In those aspects whereby a dopant is used, the laser can be directed through a dopant carrier and onto the semiconductor surface. In this way, dopant from the dopant carrier is introduced into the target region of the semiconductor material. Such a region incorporated into a semiconductor material can have various benefits in accordance with aspects of the present disclosure. For example, the target region typically has a textured surface that increases the surface area of the laser treated region and increases the probability of radiation absorption via the mechanisms described herein. In one aspect, such a target region is a substantially textured surface including micron-sized and/or nano-sized surface features that have been generated by the laser texturing. In another aspect, irradiating the surface of semiconductor material includes exposing the laser radiation to a dopant such that irradiation incorporates the dopant into the semiconductor. Various dopant materials are known in the art, and are discussed in more detail herein.

Thus the surface of the semiconductor material is chemically and/or structurally altered by the laser treatment, which may, in some aspects, result in the

formation of surface features appearing as microstructures or patterned areas on the surface and, if a dopant is used, the incorporation of such dopants into the semiconductor material. In some aspects, the features or microstructures can be on the order of 50 nm to 20 μm in size and can assist in the absorption of electromagnetic radiation. In other words, the textured surface can increase the probability of incident radiation being absorbed by the semiconductor material.

The type of laser radiation used to surface modify a semiconductor material can vary depending on the material and the intended modification. Any laser radiation known in the art can be used with the devices and methods of the present disclosure. There are a number of laser characteristics, however, that can affect the surface modification process and/or the resulting product including, but not limited to the wavelength of the laser radiation, pulse width, pulse fluence, pulse frequency, polarization, laser propagation direction relative to the semiconductor material, etc. In one aspect, a laser can be configured to provide pulsatile lasing of a semiconductor material. A short-pulsed laser is one capable of producing femtosecond, picosecond and/or nanosecond pulse durations. Laser pulses can have a central wavelength in a range of about from about 10 nm to about 8 μm , and more specifically from about 200 nm to about 1200 nm. The pulse width of the laser radiation can be in a range of from about tens of femtoseconds to about hundreds of nanoseconds. In one aspect, laser pulse widths can be in the range of from about 50 femtoseconds to about 50 picoseconds. In another aspect, laser pulse widths can be in the range of from about 50 picoseconds to 100 nanoseconds. In another aspect, laser pulse widths are in the range of from about 50 to 500 femtoseconds.

The number of laser pulses irradiating a target region can be in a range of from about 1 to about 2000. In one aspect, the number of laser pulses irradiating a semiconductor target region can be from about 2 to about 1000. Further, the repetition rate or frequency of the pulses can be selected to be in a range of from about 10 Hz to about 10 μHz , or in a range of from about 1 kHz to about 1 MHz, or in a range from about 10 Hz to about 1 kHz. Moreover, the fluence of each laser pulse can be in a range of from about 1 kJ/m^2 to about 20 kJ/m^2 , or in a range of from about 3 kJ/m^2 to about 8 kJ/m^2 .

A variety of dopant materials are contemplated, and any such material that can be used in the laser treatment process to surface modify a semiconductor material according to aspects of the present disclosure is considered to be within the present

scope. It should be noted that the particular dopant utilized can vary depending on the semiconductor material being laser treated, as well as the intended use of the resulting semiconductor material. For example, the selection of potential dopants may differ depending on whether or not tuning of the photosensitive device is desired.

- 5 A dopant can be either electron donating or hole donating. In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof. It should be noted that the scope of dopant materials should include, not only the dopant materials themselves, but also materials in forms that deliver such dopants (i.e. dopant carriers). For example, S dopant
- 10 materials includes not only S, but also any material capable being used to dope S into the target region, such as, for example, H₂S, SF₆, SO₂, and the like, including combinations thereof. In one specific aspect, the dopant can be S. Sulfur can be present at an ion dosage level of between about 5×10^{14} and about 1×10^{16} ions/cm². Non-limiting examples of fluorine-containing compounds can include ClF₃, PF₅, F₂
- 15 SF₆, BF₃, GeF₄, WF₆, SiF₄, HF, CF₄, CHF₃, CH₂F₂, CH₃F, C₂F₆, C₂HF₅, C₃F₈, C₄F₈, NF₃, and the like, including combinations thereof. Non-limiting examples of boron-containing compounds can include B(CH₃)₃, BF₃, BCl₃, BN, C₂B₁₀H₁₂, borosilica, B₂^{3/4}, and the like, including combinations thereof. Non-limiting examples of phosphorous-containing compounds can include PF₅, PH₃, and the like, including
- 20 combinations thereof. Non-limiting examples of chlorine-containing compounds can include Cl₂, SiH₂Cl₂, HCl, SiCl₄, and the like, including combinations thereof. Dopants can also include arsenic-containing compounds such as AsH₃ and the like, as well as antimony-containing compounds. Additionally, dopant materials can include mixtures or combinations across dopant groups, i.e. a sulfur-containing compound
- 25 mixed with a chlorine-containing compound. In one aspect, the dopant material can have a density that is greater than air. In one specific aspect, the dopant material can include Se, H₂S, SF₆, or mixtures thereof. In yet another specific aspect, the dopant can be SF₆ and can have a predetermined concentration range of about 5.0×10^{-8} mol/cm³ to about 5.0×10^{-4} mol/cm³. SF₆ gas is a good carrier for the incorporation
- 30 of sulfur into the semiconductor material via a laser process without significant adverse effects on the semiconductor material. Additionally, it is noted that dopants can also be liquid solutions of n-type or p-type dopant materials dissolved in a solution such as water, alcohol, or an acid or basic solution. Dopants can also be solid materials applied as a powder or as a suspension dried onto the wafer.

The semiconductor substrate can be annealed for a variety of reasons, including dopant activation, semiconductor material damage repair, and the like. In those aspects including a laser textured region, the semiconductor material can be annealed prior to laser treatment, following laser treatment, during laser treatment, or
5 both prior to and following laser treatment. Annealing can enhance the semiconductive properties of the device, including increasing the photoresponse properties of the semiconductor materials. Additionally, annealing can reduce damage done by the lasing process. Although any known anneal can be beneficial and would be considered to be within the present scope, annealing at lower temperatures can be
10 particularly useful. Such a "low temperature" anneal can greatly enhance the photoconductive gain and external quantum efficiency of devices utilizing such materials. In one aspect, for example, the semiconductor material can be annealed to a temperature of from about 300° C to about 1100 C°. In another aspect, the semiconductor material can be annealed to a temperature of from about 500° C to
15 about 900° C. In yet another aspect, the semiconductor material can be annealed to a temperature of from about 700° C to about 800° C. In a further aspect, the semiconductor material can be annealed to a temperature that is less than or equal to about 850° C.

The duration of the annealing procedure can vary according to the specific
20 type of anneal being performed, as well as according to the materials being used. For example, rapid annealing processes can be used, and as such, the duration of the anneal may be shorter as compared to other techniques. Various rapid thermal anneal techniques are known, all of which should be considered to be within the present scope. In one aspect, the semiconductor material can be annealed by a rapid
25 annealing process for a duration of greater than or equal to about 1 μs. In another aspect, the duration of the rapid annealing process can be from about 1 μs to about 1 ms. As another example, a baking or furnace anneal process can be used having durations that may be longer compared to a rapid anneal. In one aspect, for example, the semiconductor material can be annealed by a baking anneal process for a duration
30 of greater than or equal to about 1 ms to several hours. As has been described, if low oxygen content semiconductor materials are used it maybe beneficial to anneal such materials in a substantially oxygen-depleted environment.

As has been described, annealing can help reduce defects inherent to the semiconductor substrate and otherwise reduce electron/hole recombination. In other

words, the annealing can help create electron states that effectively reduce the undesirable recombination processes. Annealing the semiconductor material may also improve the responsivity or photoconductive gain of the device. Photoconductive devices can have dopants, impurities, or defects that can introduce energy levels that can trap carriers. Trapping carriers and reducing recombination of photocarriers can lead to an increase in photoconductive gain of the device. The relationship of photoconductive gain and trapping time can be represented by Equation (I):

$$\text{Gain} = \tau_L / \tau_t \quad (I)$$

where " τ_L " is the lifetime of an excess carrier and " τ_t " is the transit time of the carriers across the device. It is understood that the lifetime of an excess carrier can be increased by trapping a carrier species and reducing the recombination rate. An increase in gain can be achieved by trapping centers in the semiconductor that have millisecond trapping times at room temperature and short transit times in thinned lightly doped wafers. These trapping locations can decrease the recombination of carriers and therefore improve or increase the photoconductive gain of the device by allowing more electrons to traverse the different regions without being recombined.

Turning to FIG. 2, a reflecting layer 20 can be coupled to the semiconductor substrate 12. The reflecting layer can be coupled to any side or portion of the semiconductor substrate in order to reflect electromagnetic radiation back into the device. Accordingly, in one aspect the reflecting layer can be located on the semiconductor substrate opposite the incoming electromagnetic radiation. Thus, as is shown in FIG. 2, electromagnetic radiation passing through the semiconductor substrate and the textured region 16 can be reflected back into the semiconductor substrate. Additionally, a passivation layer 22 can be coupled to the semiconductor substrate. The passivation layer is shown coupled to the side of the semiconductor substrate facing the incoming electromagnetic radiation, however a passivation layer can be located anywhere on the device and still be within the present scope.

As has been described, location of the textured region can be used to provide enhancement and/or filtering of the incoming electromagnetic radiation. For example, a textured region located at the point of entry of the electromagnetic radiation into the photosensitive device tends to bend the electromagnetic radiation, particularly the blue wavelengths. Accordingly, one level of tuning can be accomplished by locating

the textured region on the surface adjacent the incident electromagnetic radiation to purposely effectuate the filtering of blue wavelengths. Additionally, absorption of particular wavelengths of electromagnetic radiation occurs at different depths in the semiconductor layer and/or textured region. By increasing the absorption to green wavelengths, for example, the electrical signal as a result of green wavelengths can be increased in a diode or pixel. Certain traditional 4 pixel imagers have one red, one blue, and two green pixels, with the greater number of green pixels to account for increased sensitivity of the human eye to green colors. Thus in one aspect, a 4 pixel imager can have one blue, one red, and one green pixel having an increased green wavelength absorption. The fourth pixel can be used for an IR or other wavelength selective pixel depending on the desired application of the imager.

FIG. 3 shows a photosensitive device having textured regions 30 located on the sides of the semiconductor substrate 12. Such a configuration allows electromagnetic radiation normally exiting through the sides of the device to be further defused and absorbed within semiconductor substrate. The textured region(s) can be located on one or more sides to facilitate the enhanced absorption.

FIG. 4 shows a photosensitive device having a textured region 40 having a nonparallel surface with respect to the semiconductor substrate 12. Thus the overall configuration of the textured region can be designed to further enhance absorption and/or selectively tune the device. As has been described, the nonparallel surface can have a variety of configurations, such as, without limitation, nonparallel slope, a pyramid, an inverted pyramid, a concave shape, a convex shape, and the like. In some cases the configuration of the textured region can function to direct or focus electromagnetic radiation into the semiconductor substrate, and in other cases the configuration of the textured region can function to direct or focus electromagnetic radiation away from the semiconductor substrate.

As is shown in FIG. 5, a lens 50 can be coupled to the semiconductor substrate 12 on a side facing incoming electromagnetic radiation. Thus the lens can focus the electromagnetic radiation into the semiconductor substrate. In those aspects having circuitry or other structures disposed on the incoming electromagnetic radiation surface, the lens can further focus light around such structures, thereby reducing optical scattering and noise.

As is shown in FIG. 6, a textured region 60 is located on the semiconductor substrate 12 adjacent to the multiple doped regions 14, 16. The textured region can be

associated with at least one of the doped regions as is shown, or the textured region can be distinct from the doped regions (not shown). Electromagnetic radiation can enter the photosensitive device at the side adjacent the doped regions, or alternatively at the side opposite the doped regions.

5 FIGs. 7-11 show various steps in the manufacture of a photosensitive pixel according to aspects of the present disclosure. FIG. 7 shows a cross-section of a front side illumination (FSI) photosensitive pixel device. The photosensitive pixel device can include a semiconductor substrate 72, and can be referred to as bulk semiconductor material. The semiconductor substrate includes at least one doped region 74 that can be doped with an electron donating or hole donating species to cause the region to become more positive or negative in polarity as compared to the semiconductor substrate. In one aspect, for example, the doped region can be p doped. In another aspect the doped region can be n doped. A highly doped region 76 can be formed on or near the doped region to create a pinned diode. In one example, 10 the semiconductor substrate can be negative in polarity, and the doped region and the highly doped region can be doped with p+ and n- dopants respectively. In some aspects, variations of n(—), n(—), n(+), n(++), p(—), p(—), p(+), or p(++ type doping of the regions can be used. It should be noted that in one aspect the highly doped region can be the textured region. In other words, textured surface features can be formed on 15 or in the highly doped region.

20 The device of FIG. 7 can further include various metal regions 78, at least one via 80, a passivation layer 82, trench isolation 84, and an electrical transfer element 86. Trench isolation elements can maintain pixel to pixel uniformity by reducing optical and electrical crosstalk. The trench isolation can be shallow (FIG. 7) or deep (FIG. 12) trench isolation. The trench isolation can include various materials, including, without limitation, dielectric materials, reflective materials, conductive materials, light diffusing features, and the like. These trench isolation regions can be configured to reflect incident light until it is absorbed, thereby increase the effective absorption length of the device.

30 As is shown in FIG. 8, a carrier substrate or carrier wafer 88 can be coupled to the photosensing pixel. In one aspect, the carrier substrate can be disposed on the passivation layer 82, although the carrier substrate can be disposed on any surface of the device. In one aspect, for example, the carrier substrate can be disposed on the semiconductor substrate (not shown). The carrier substrate can be coupled to the

photosensing pixel by various techniques, and any such coupling mechanism is within the present scope. In one aspect, for example, the coupling can occur by way of a bonding layer or adhesive layer disposed on the device, for example, on the passivation layer. The support substrate can provide support to the semiconductor device both during and after manufacture, depending on whether or not the support is removed. The carrier substrate can be made of a semiconductor material that is the same or similar to the bulk semiconductor material, or it can be made of a different material.

As is shown in FIG. 9, a textured region 90 is coupled to the semiconductor substrate 72 opposite the doped regions 74,76. Thus light entering from the direction of the doped regions passes through the semiconductor substrate prior to contacting the textured region. The textured region can be disposed across an entire surface of the semiconductor substrate, as is shown in FIG. 9, or it can be disposed on one or more discrete regions (not shown).

As is shown in FIG. 10, an additional carrier support substrate 100 can be coupled to the device on an opposing side from the carrier support substrate 88. The additional carrier support substrate can be utilized for a variety of purposes, including providing additional support to the device, facilitating the removal of the first carrier support substrate, and the like. A reflective layer 102 can be disposed between the textured region 90 and the carrier support substrate. Thus the reflective layer can reflect electromagnetic radiation that passes through the textured region back toward the semiconductor substrate 72, thus reducing optical loss and backscattering. Thus, in some aspects a reflective layer can increase the quantum efficiency of the device. The reflective layer material can be any reflective material that can be incorporated into such a device. Nonlimiting examples can include materials such as silver, aluminum, and the like.

As is shown in FIG. 11, the carrier support substrate can be removed to expose the passivation layer 82 or any other material layer that was previously covered by the carrier support substrate. The additional carrier substrate 100 can be maintained in the device, removed from the device, or thinned to reduce the thickness of the substrate depending on the intended use of the device. The removal of material from the device, including the carrier support substrate and the additional carrier substrate, can be accomplished by a variety of methods including, without limitation, etching, chemical mechanical polishing, ion implanting (i.e. smart cut), and the like.

Various types of trench isolation are contemplated, and any such isolation is considered to be within the present scope. As has been described, trench isolation can be shallow (FIG. 7, 84) or deep (FIG. 12, 120) trench isolation. The trench isolation can also include depths between shallow and deep, depending on the device design.

5 Trench isolation can include dielectric materials, reflective materials, conductive materials, and combinations thereof, including textured regions and other light diffusing features. Thus the trench isolation layer can be configured to reflect incident electromagnetic radiation, in some cases until it is absorbed, thereby increasing the effective absorption length of the device. Additionally, in some aspects
10 pillar features can be incorporated into pixels by thinning or removing material from the semiconductor substrate using deep trench isolation and etching techniques. As is shown in FIG. 13, the textured region 130 can have a nonparallel surface with respect to the semiconductor substrate 72 as has been described. This nonparallel morphology, when included with the deep trench isolation 120, can effectively focus
15 electromagnetic radiation into the semiconductor substrate from multiple sides.

It is also contemplated, that a non-bulk material can be formed or disposed near a doped region in the device. The addition of the non-bulk material can allow for electromagnetic radiation diffusing features to be formed on or in the non-bulk material. A metal layer defining an aperture can also be included in one aspect of the
20 present disclosure. The metal layer can be formed near the doped regions and can have a light entering region that defines an aperture. This light entering region can also include an antireflecting material.

Fig. 14 shows a photosensitive imager comprising two photosensitive pixels 140. Each photosensitive pixel includes a boundary region 142 that can include metal
25 circuitry and a textured region 144. Each photosensitive pixel can include at least one transistor 146 or other electrical transfer element. Additional read out and circuitry elements 148 can be utilized and shared by both photosensitive pixels.

Turning to FIG. 15, a backside illuminated (BSI) photosensitive pixel according to one aspect present disclosure is provided. A lens 150 and an anti-
30 reflective coating 152 are disposed on the backside of the pixel following thinning and trench isolation. A color filter 154 can be optically coupled to the lens to allow specific wavelengths filtering of the electromagnetic radiation. A textured region 156 can be coupled to the semiconductor substrate 72 opposite the lens in order to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes

through to the front side of the pixel. Thus the electromagnetic radiation can be focused within the semiconductor substrate to the combined action of the textured region and the trench isolation 120

Fig. 16 shows a front side illuminated (FSI) imager according to another aspect of the present disclosure. A lens 160 and an antireflecting passivation layer on 62 are coupled to the front side of the pixel. A textured region 90 and a reflecting layer 102 are coupled to the semiconductor substrate 72 opposite the lens to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes through the semiconductor substrate. An aperture 164 formed in a metal or other 10 reflective material layer 166 can increase the effectiveness of the optical cavity. Thus the lens focuses electromagnetic radiation through the aperture.

In other aspects of the present disclosure, various methods of making photosensitive diodes, pixels, and imagers, are contemplated. In one aspect, as is shown in FIG. 17, a method of making a photosensitive imager device can include 15 forming a textured region on a semiconductor substrate having multiple doped regions forming a least one junction, wherein the textured region is formed in a position to interact with electromagnetic radiation 170. The method also includes coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one 20 junction 172. In one aspect, multiple pixels can be associated together to form an imager. A passivation layer can also be disposed on the photosensitive imager device to protect and/or reduce the dark current of the device.

In another aspect of the present disclosure, a method for making a photosensitive diode is provided. Such a method can include forming at least one 25 cathode and at least one anode on a surface of a semiconductor substrate, coupling a textured region to the semiconductor substrate, and coupling a support substrate to the semiconductor substrate. The textured region can be located adjacent to the anode and cathode, opposite the anode and cathode, or both adjacent and opposite the anode and cathode. An electrical transfer on the can be electrically coupled to at least one of 30 the anode and cathode to form a photosensitive pixel. In another aspect, the semiconductor substrate can be thinned to improve the response rate and/or speed of the device. A passivation layer can also be disposed on the photosensitive diode to protect and/or reduce the dark current of the device. An additional support substrate can be attached to the device to provide additional support. In one aspect, the

additional support substrate can be located on the opposite side of the photosensitive diode from the support substrate. The support substrate can subsequently be removed to allow for further processing.

Of course, it is to be understood that the above-described arrangements are
5 only illustrative of the application of the principles of the present disclosure.
Numerous modifications and alternative arrangements may be devised by those
skilled in the art without departing from the spirit and scope of the present disclosure
and the appended claims are intended to cover such modifications and arrangements.
Thus, while the present disclosure has been described above with particularity and
10 detail in connection with what is presently deemed to be the most practical
embodiments of the disclosure, it will be apparent to those of ordinary skill in the art
that numerous modifications, including, but not limited to, variations in size,
materials, shape, form, function and manner of operation, assembly and use maybe
made without departing from the principles and concepts set forth herein.

15

CLAIMS

What is claimed is:

- 5 1. A photosensitive imager device, comprising:
 a semiconductor substrate having multiple doped regions forming a least one
junction;
 a textured region coupled to the semiconductor substrate and positioned to
interact with electromagnetic radiation; and
10 an electrical transfer element coupled to the semiconductor substrate and
operable to transfer an electrical signal from the at least one junction.
2. The device of claim 1, wherein the textured region is operable to facilitate
generation of an electrical signal from the detection of infrared electromagnetic
15 radiation.
3. The device of claim 1, wherein interacting with electromagnetic radiation further
includes increasing the semiconductor substrate's effective absorption length as
compared to a semiconductor substrate lacking a textured region.
20
4. The device of claim 1, wherein the transfer element is selected from the group
consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.
5. The device of claim 1, further comprising a reflective layer coupled to the
25 semiconductor substrate and positioned to maintain the electromagnetic radiation in
the semiconductor substrate.
6. The device of claim 1, wherein the textured region is positioned on a surface of the
semiconductor substrate that is opposite the multiple doped regions.
30
7. The device of claim 6, wherein the textured region has a surface morphology
operable to direct electromagnetic radiation into or out of the semiconductor substrate.

8. The device of claim 7, wherein the surface morphology of the textured region relative to the semiconductor substrate is a member selected from the group consisting of sloping, pyramidal, inverted pyramidal, spherical, parabolic, asymmetric, symmetric, and combinations thereof.
- 5
9. The device of claim 1, wherein the textured region is positioned on a surface of the semiconductor substrate that is adjacent the multiple doped regions.
10. The device of claim 9, further comprising an additional textured region
- 10 positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions.
11. The device of claim 1, wherein the textured region is coupled directly to at least one of the multiple doped regions.
- 15
12. The device of claim 1, wherein the textured region includes surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof.
- 20 13. The device of claim 12, wherein surface features include a member selected from the group consisting of cones, pillars, pyramids, microlenses, quantum dots, inverted features, and combinations thereof.
14. The device of claim 1, wherein the textured region has been formed by a process
- 25 selected from the group consisting of lasing, chemical etching, nanoimprinting, material deposition, and combinations thereof.
15. The device of claim 1, further comprising a lens optically coupled to the semiconductor substrate and positioned to focus incident electromagnetic radiation
- 30 into the semiconductor substrate.
16. A photosensitive imager array, comprising at least two photosensitive imager devices of claim 1.

17. The array of claim 16, further comprising at least one trench isolation positioned between the at least two photosensitive imager device.

18. A method of making a photosensitive imager device, comprising:

- 5 forming a textured region on a semiconductor substrate, wherein the semiconductor substrate has multiple doped regions forming a least one junction, and wherein the textured region is formed in a position to interact with electromagnetic radiation; and
- coupling an electrical transfer element to the semiconductor substrate such that
- 10 the electrical transfer element is operable to transfer an electrical signal from the at least one junction .

19. The method of claim 18, wherein forming the textured region is by a process selected from the group consisting of lasing, chemical etching, nanoimprinting,

15 material deposition, and combinations thereof.

20. The method of claim 18, wherein forming the textured region includes irradiating a target region with laser radiation to form surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof.

20

21. The method of claim 20, wherein irradiating the target region includes exposing the laser radiation to a dopant such that the irradiation incorporates the dopant into the textured region.

22. The method of claim 20, wherein the irradiation is performed using a pulsed laser including a member selected from the group consisting of a femtosecond laser, a picosecond laser, a nanosecond laser, and combinations thereof.

23. The method of claim 18, further comprising tuning an electrical response of the

30 photosensitive imager device.

24. The method of claim 23, wherein tuning includes forming surface features to have dimensions that selectively diffuse or selectively absorb a desired wavelength of electromagnetic radiation.

25. The method of claim 23, wherein tuning is accomplished through a factor selected from the group consisting of placement of the textured region, material type of the textured region, thickness of the textured region, dopant type of the textured
5 region, doping profile of the texture region, doping profile of the semiconductor substrate, thickness of the substrate, and combinations thereof.

26. The method of claim 18, wherein the transfer element is selected from the group consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.
10

27. The method of claim 18, further comprising annealing the semiconductor substrate to a temperature of from about 300° C to about 1100° C.

28. A photosensitive imager device, comprising:
15 a semiconductor substrate having multiple doped regions forming a least one junction;
a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation; and
at least 4 transistors coupled to the semiconductor substrate and with at least
20 one of the transistors electrically coupled to the at least one junction.

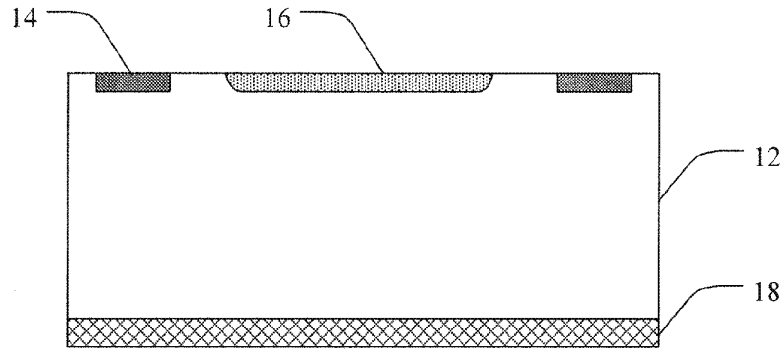


FIG. 1

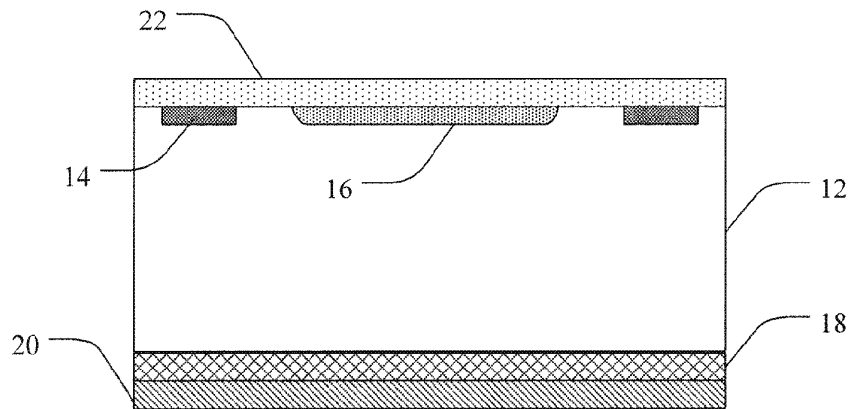


FIG. 2

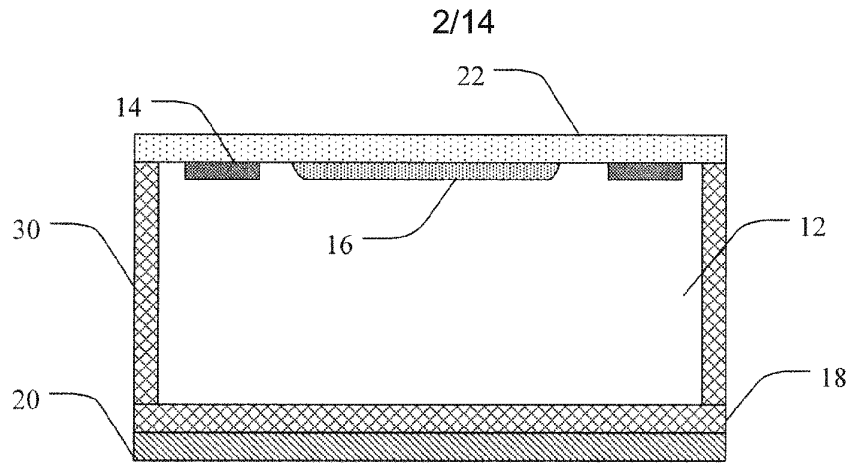


FIG. 3

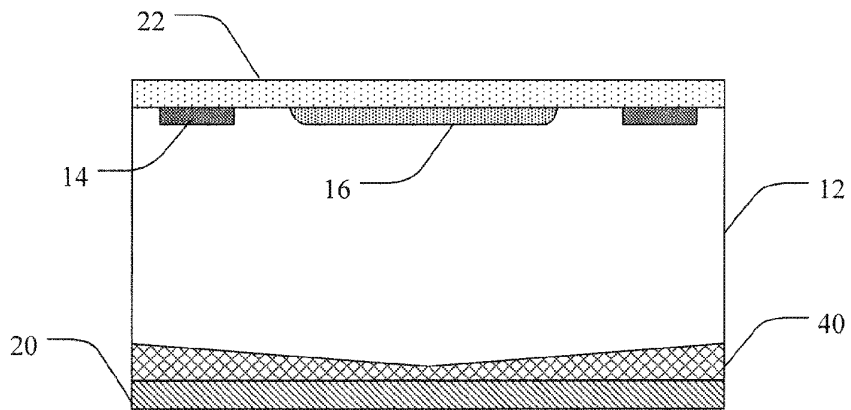


FIG. 4

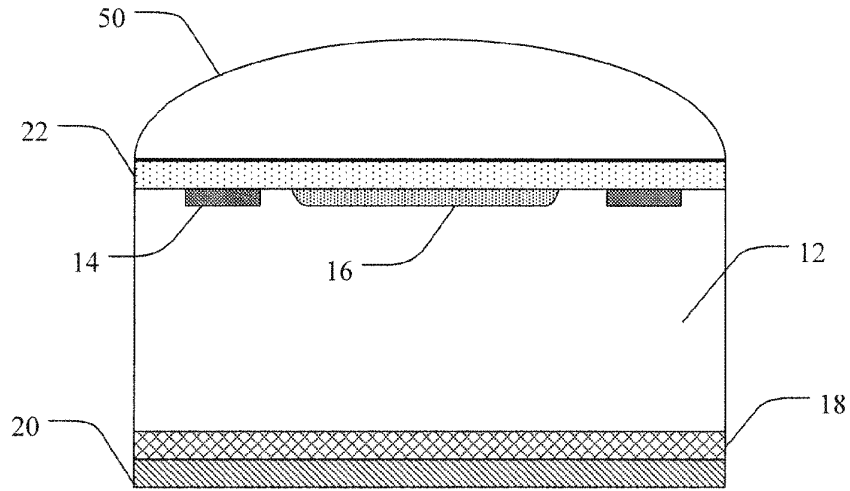


FIG. 5

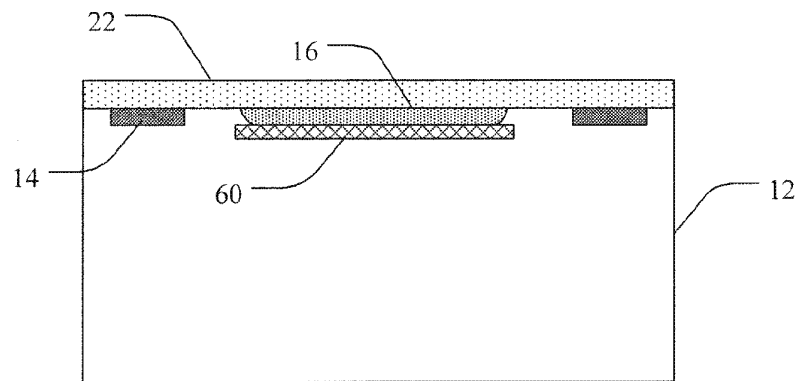


FIG. 6

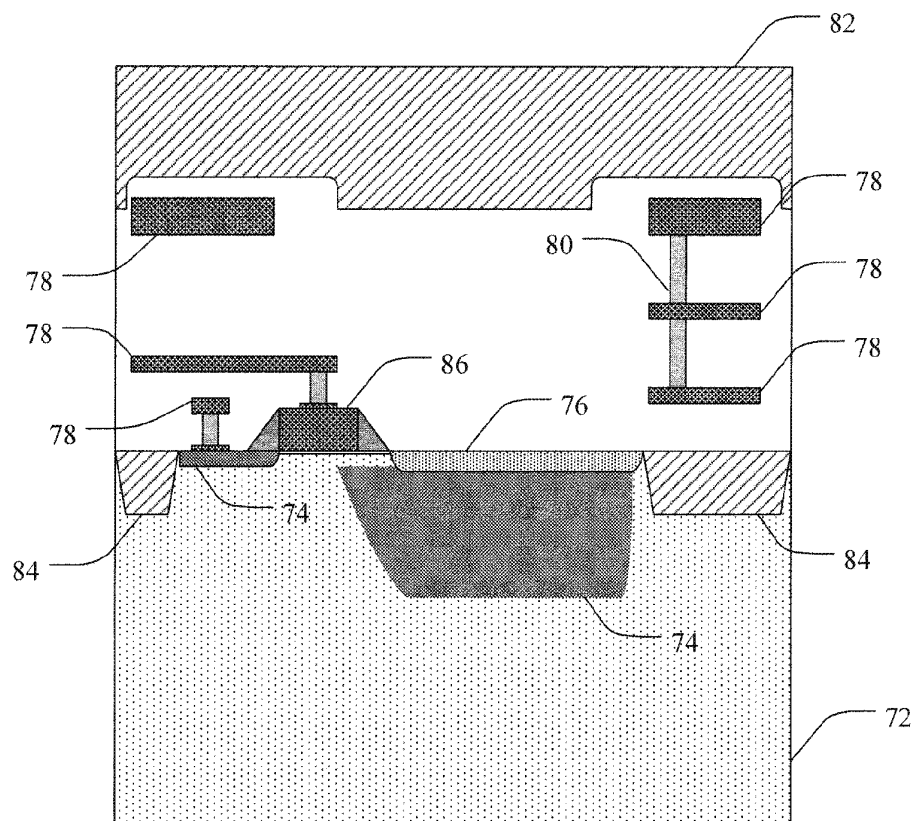


FIG. 7

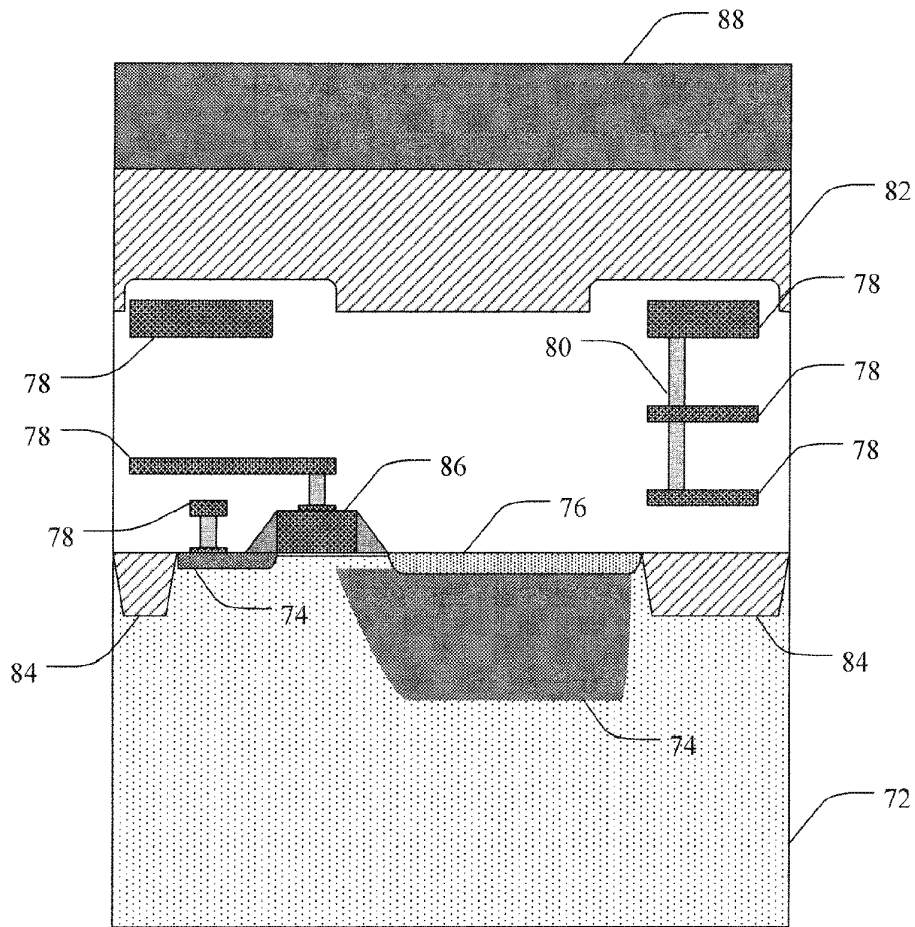


FIG. 8

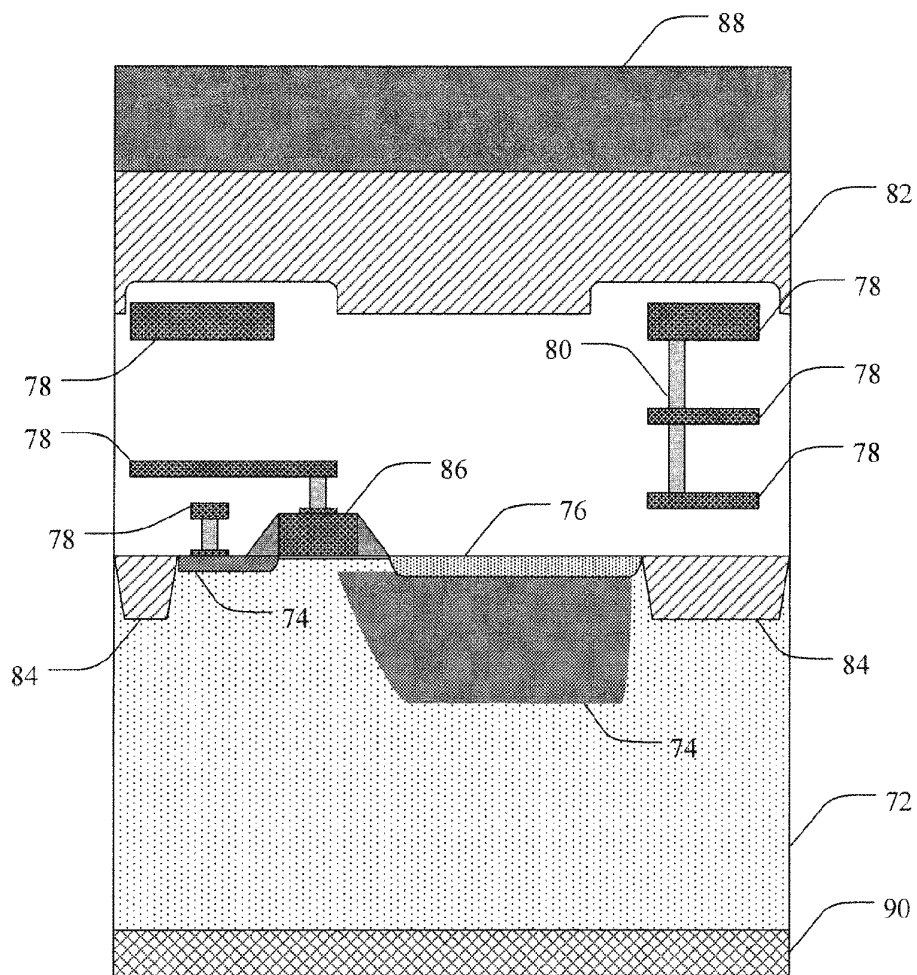


FIG. 9

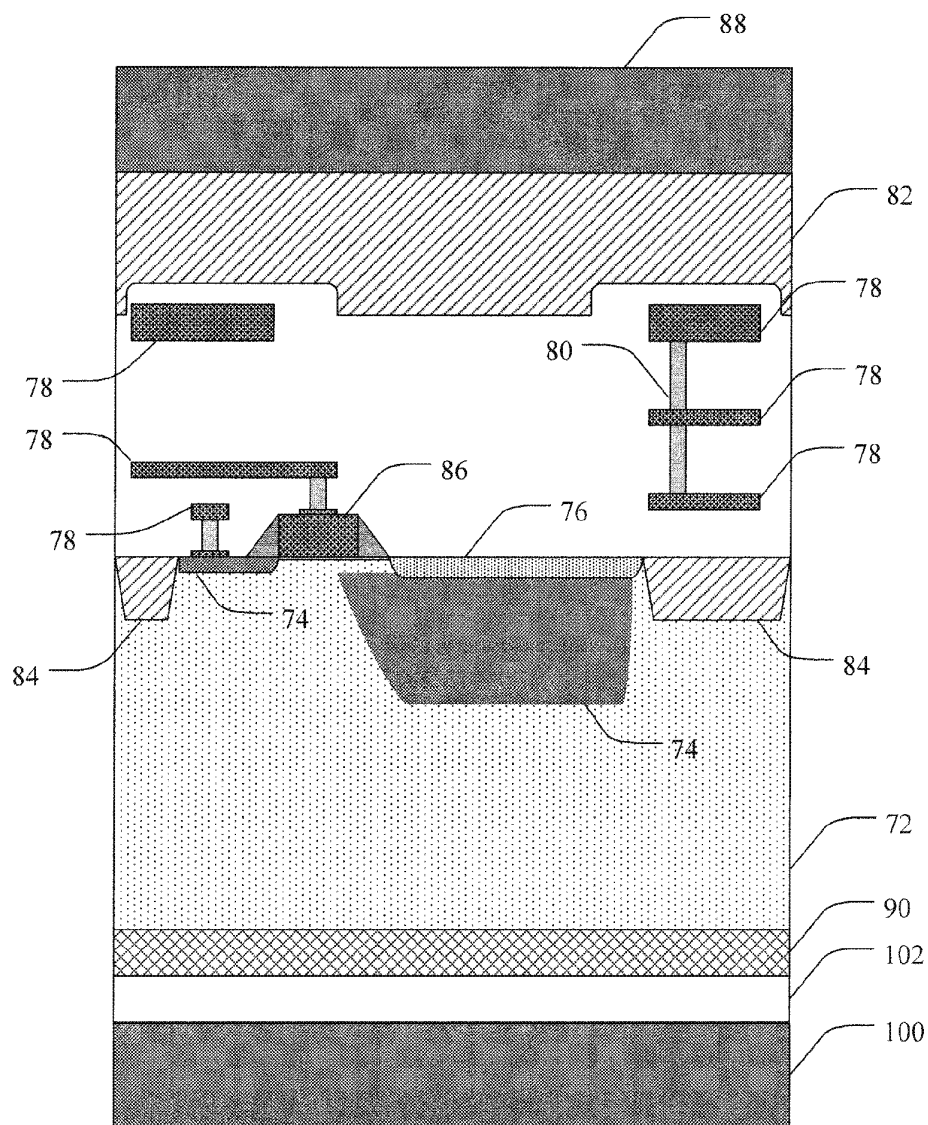


FIG. 10

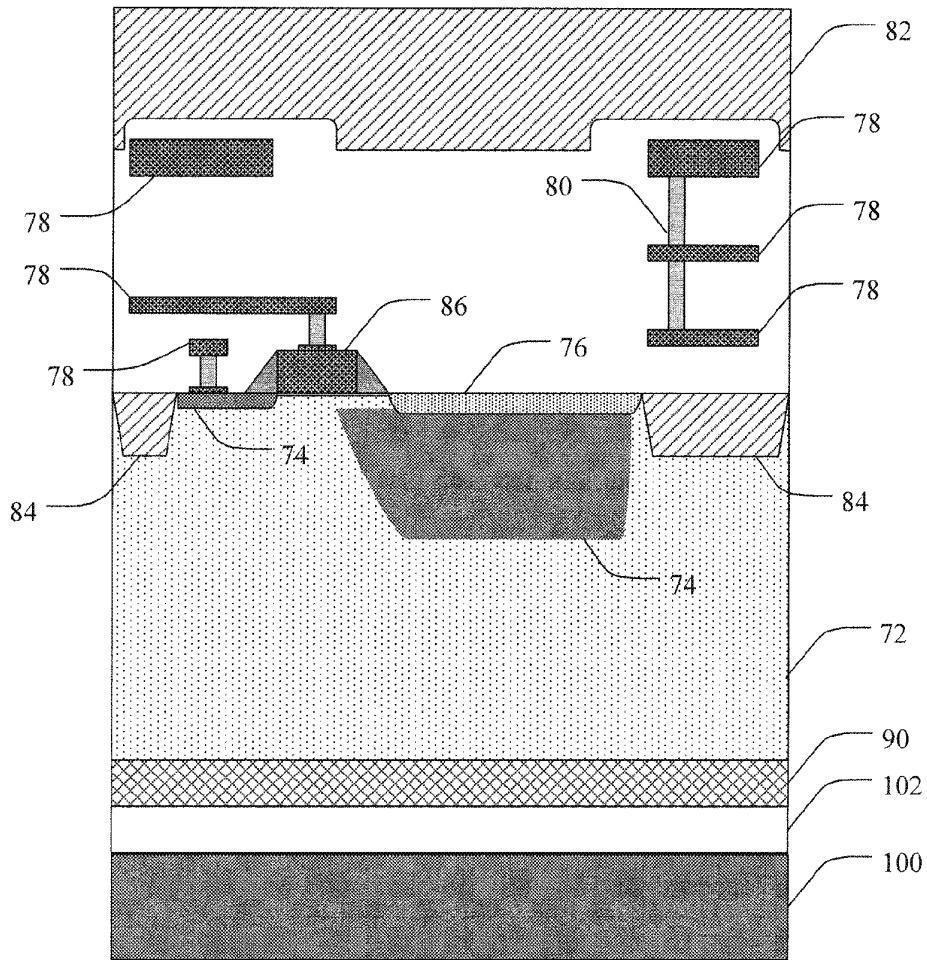


FIG. 11

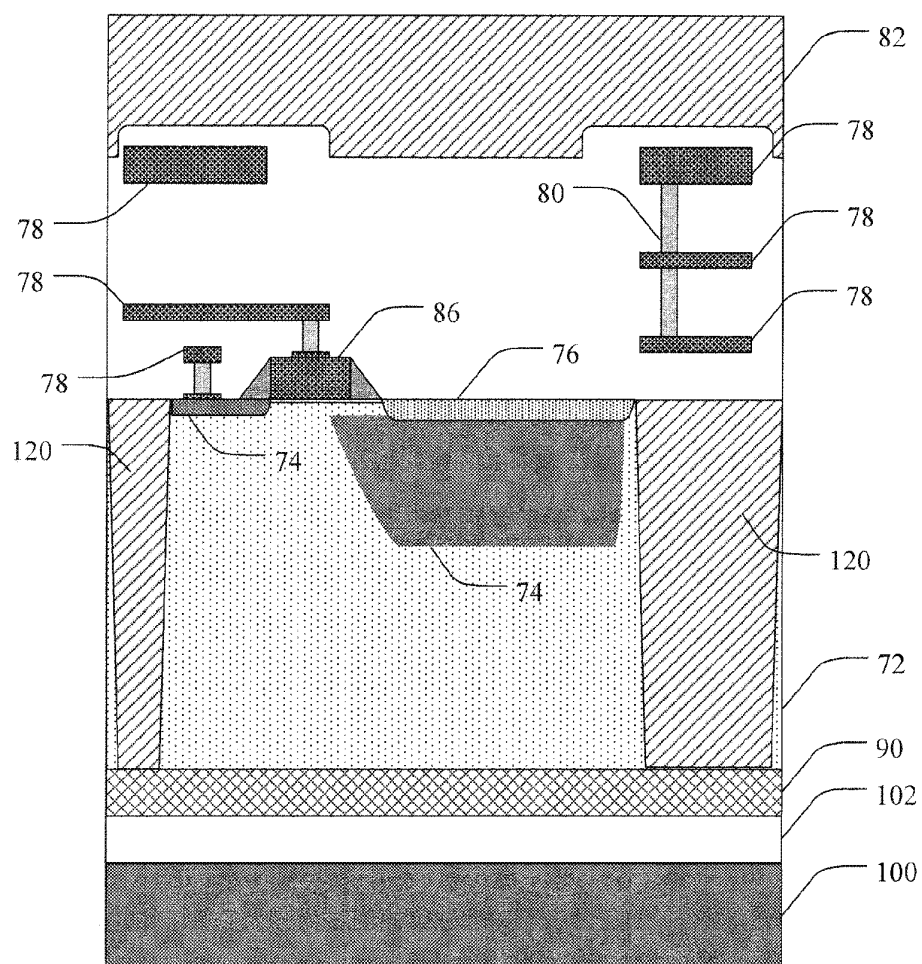


FIG. 12

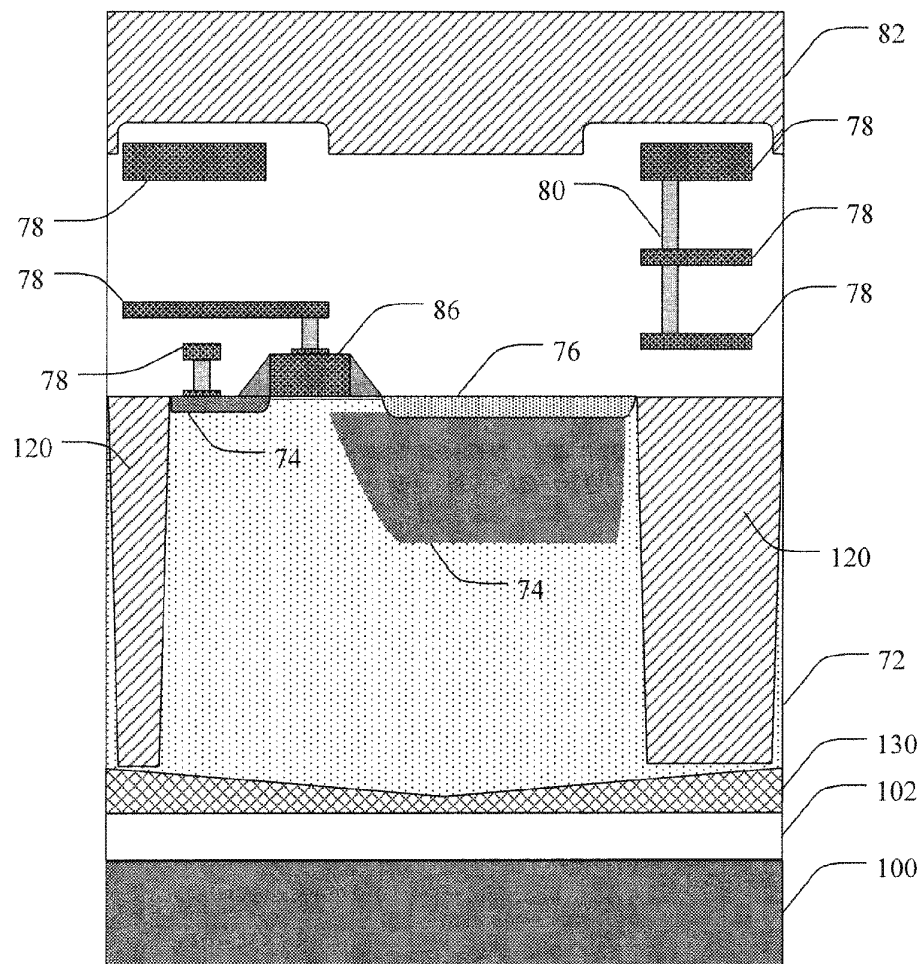


FIG. 13

11/14

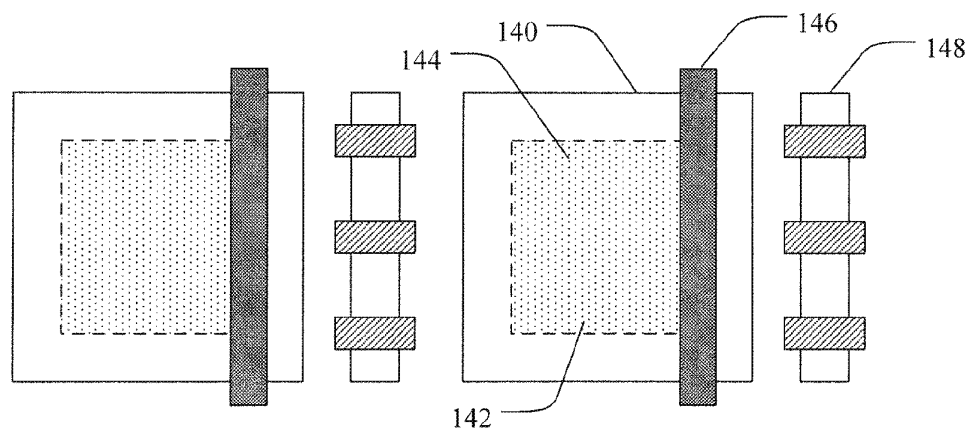


FIG. 14

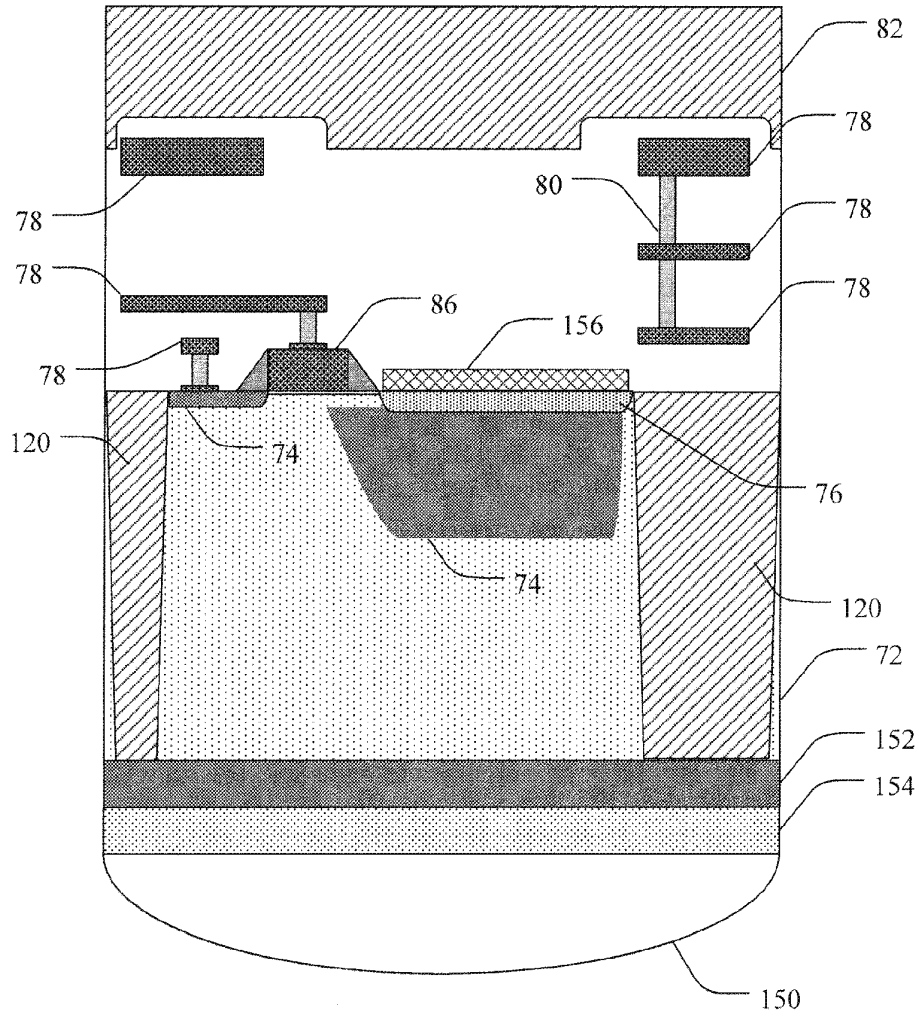


FIG. 15

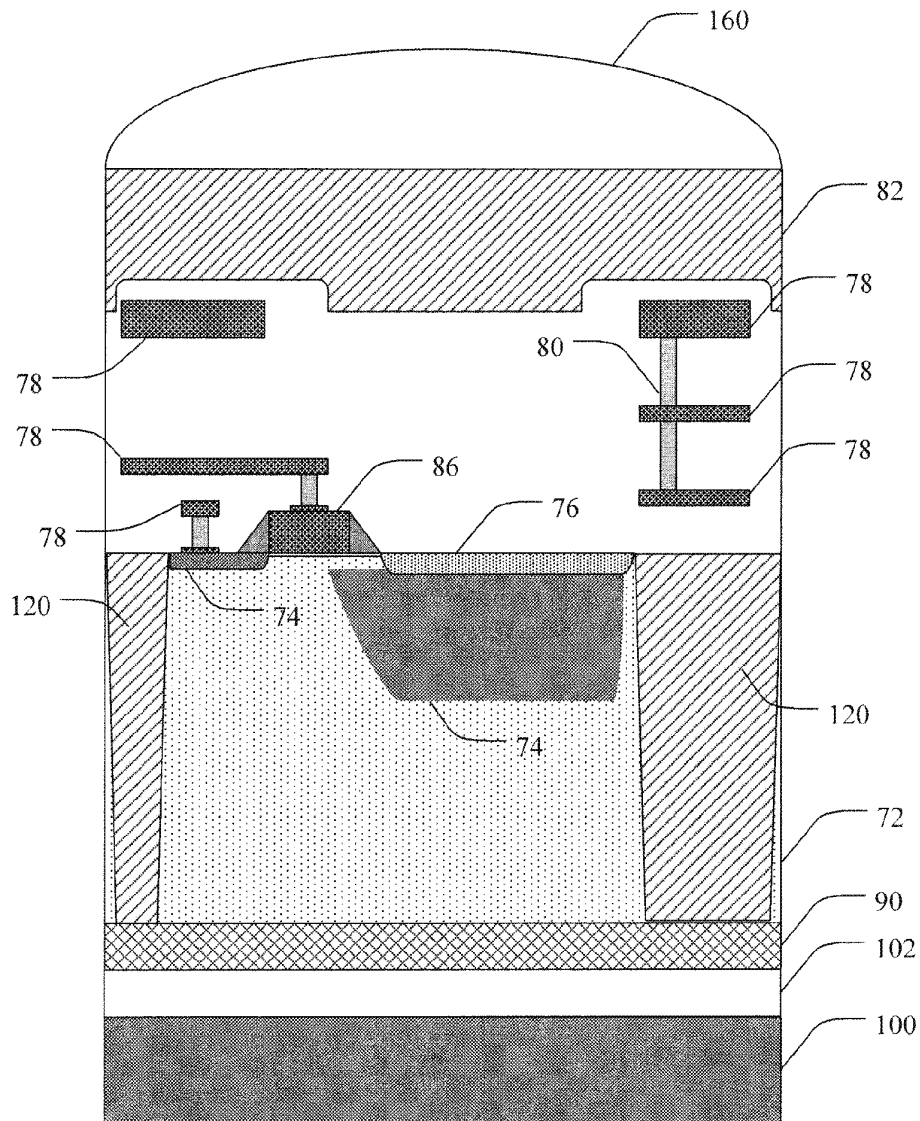


FIG. 16

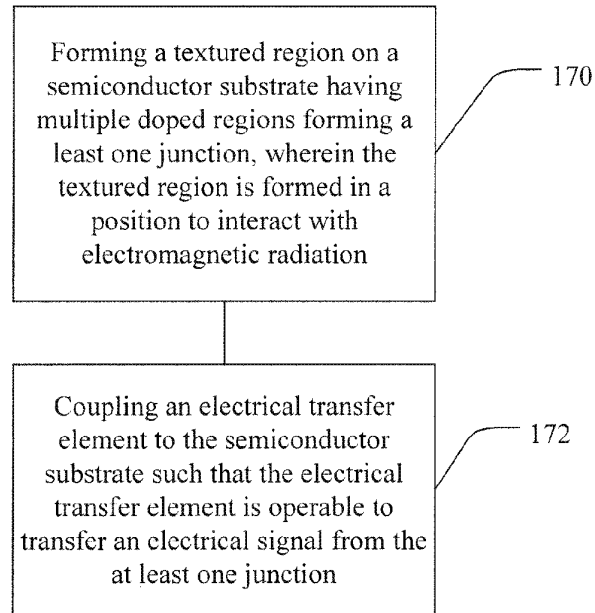


FIG. 17

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L2	84	US-3035052-\$.DID. OR US-20030029495- \$.DID. OR US- 20040222187-\$.DID. OR US-20050127401- \$.DID. OR US- 20050227390-\$.DID. OR US-20060011955- \$.DID. OR US- 20060079062-\$.DID. OR US-20060118781- \$.DID. OR US- 20060180885-\$.DID. OR US-20060231914- \$.DID. OR US- 20070145505-\$.DID. OR US-20080026550- \$.DID. OR US- 20080036022-\$.DID. OR US-20080044943- \$.DID. OR US- 20080076240-\$.DID. OR US-20080099804- \$.DID. OR US- 20080178932-\$.DID. OR US-20080258604- \$.DID. OR US- 20090065051-\$.DID. OR US-20090142879- \$.DID. OR US- 20090160983-\$.DID. OR US-20090194671- \$.DID. OR US- 20090200586-\$.DID. OR US-20090213883- \$.DID. OR US- 3487223-\$.DID. OR US-4277793-\$.DID. OR US-4419533-\$.DID. OR US-4493942-\$.DID. OR US-4514582-\$.DID. OR US-4536608-\$.DID. OR US-4663188-\$.DID. OR US-4829013-\$.DID. OR US-5080725-\$.DID. OR US-5081049-\$.DID. OR US-5100478-\$.DID. OR US-5114876-\$.DID. OR US-5164324-\$.DID. OR US-5322988-\$.DID. OR US-5346850-\$.DID. OR US-5597621-\$.DID. OR US-5714404-\$.DID. OR	(US-PGPUB; USPAT; USOCR; JPO; IBM_TDB)	OR	ON	ON	2014/06/25 02:14 PM

L3	7768	US-5731213-\$.DID. OR US-5792280-\$.DID. OR US-6147297-\$.DID. OR US-6498336-\$.DID. OR US-6580053-\$.DID. OR US-6583936-\$.DID. OR US-6667528-\$.DID. OR US-6759262-\$.DID. OR US-6800541-\$.DID. OR US-7057256-\$.DID. OR US-7091411-\$.DID. OR US-7109517-\$.DID. OR US-7247527-\$.DID. OR US-7314832-\$.DID. OR US-7354792-\$.DID. OR US-7390689-\$.DID. OR US-7442629-\$.DID. OR US-7456452-\$.DID. OR US-7482532-\$.DID. OR US-7498650-\$.DID. OR US-7504325-\$.DID. OR US-7504702-\$.DID. OR US-7511750-\$.DID. OR US-7745901-\$.DID. OR US-7781856-\$.DID. OR US-7816220-\$.DID. OR US-7847253-\$.DID. OR US-7884439-\$.DID. OR US-7884446-\$.DID. OR US-8030726-\$.DID. OR US-8058615-\$.DID. OR US-8207051-\$.DID. OR US-8476681-\$.DID. OR US-3666484-\$.DID. OR US-2030766-\$.DID. OR JP-07173484-\$.DID. OR JP-071734840721- \$.DID. OR JP- 2008187003-\$.DID. OR JP-2011091128-\$.DID. OR JP-2152226-\$.DID. OR JP-63116421- \$.DID. OR JP-9298308- \$.DID. OR KR- 20010061058-\$.DID. OR KR-20100118864- \$.DID. OR WO- 2006086014-\$.DID. OR WO-2009100023- \$.DID. OR WO- 2011035188-\$.DID. OR WO-2011119618- \$.DID. (light adj2 (trapping or trapped))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 02:16 PM
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L4	11	L2 and L3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 02:16 PM
L5	2251	(reflector or Bragg) and L3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:40 PM
L6	14	(reflector or Bragg) and L2	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:41 PM
L7	888	(reflector or Bragg) near3 backside	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:55 PM
L8	51623	(reflector or Bragg) near3 (side or sidewall or edge or wall)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:55 PM
L9	112640	pixel near5 (side or sidewall or edge or wall)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:56 PM
L10	143	L7 same L8	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:56 PM
L11	2	L9 same4 L10	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:56 PM
L12	3	L9 and L10	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:57 PM
L13	1	L12 not L11	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:57 PM
L14	179	L7 same4 L8	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:58 PM
L15	145	L14 and (photodiode or pixel or light)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:59 PM
L16	129	L14 same10 (photodiode or pixel or light)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:59 PM
L17	128	L14 same8 (photodiode or pixel or light)	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2014/06/25 03:59 PM

L18	1204	(reflector or Bragg) near5 backside	JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:09 PM
L19	71202	(reflector or Bragg) near5 (side or sidewall or edge or wall)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:09 PM
L20	280	L18 same4 L19	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:09 PM
L21	195	L20 same4 (photodiode or pixel or light)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:09 PM
L22	7	L18 same2 L9	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:10 PM
L23	7	L22 same4 (photodiode or pixel or light)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:10 PM
L24	217	L18 same L19	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:13 PM
L25	0	(light adj2 sensitive adj2 pixel) same4 L24	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:14 PM
L26	0	(light adj2 sensitive adj2 pixel) and L24	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:14 PM
L27	14	pixel same4 L24	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:14 PM
L28	7	L27 and index	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:18 PM
L29	26925	(high adj2 index) near3 (layer or film)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:48 PM
L30	27823	(low adj2 index) near3 (layer or film)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:48 PM

L31	12802	L29 near10 L30	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:48 PM
L32	1170	(reflector or Bragg) same L31	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:49 PM
L33	611	(reflector or Bragg) near10 L31	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:49 PM
L34	4200	L30 near5 ("between")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:49 PM
L35	1972	L34 near10 L29	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:50 PM
L36	81	(reflector or Bragg) near10 L35	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:50 PM
L37	188	L29 near5 (polysilicon or polycrystalline or poly or (amorphous adj2 silicon) or germanium)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:53 PM
L38	2500	L30 near5 (oxide or nitride or oxynitride or oxynitrides)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:53 PM
L39	14	L37 near20 L38	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:53 PM
L40	0	(reflector or Bragg) same L39	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:54 PM
L41	0	L39 near20 ("between")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:54 PM
L42	51	backside near6 (textured near2 (layer or film))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 01:12 PM
L43	10	L42 AND (H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 01:25 PM

L44	5	H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.) L39 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 01:25 PM
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L45	2	H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.) L36 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 01:25 PM
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L46	1	H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.) ("20140138785").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2015/01/05 11:26 AM
L47	3930	(257/432).CCLS.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2015/01/05 11:54 AM
L48	218	(257/228).CCLS.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2015/01/05 11:54 AM
L50	1	("9373732").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2016/07/13 03:10 PM
L51	1	("9373732").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2016/07/15 10:13 AM
L52	395	reflective near3 (aluminum adj oxide)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/15 01:07 PM
L53	35214	(rough or textured) near2 (layer or film)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:24 AM
L54	44833	light adj2 incident adj2 surface	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:24 AM
L55	38	L53 same L54	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:25 AM
L56	10	L55 same efficiency	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:25 AM
L57	0	L55 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:29 AM
L58	0	L55 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:30 AM
L59	3	L55 same (metal or polysilicon or amorphous)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:30 AM
L60	1864	L53 same efficiency	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:32 AM
L61	42	L60 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2017/02/06 01:32 AM

L62	351	"SiN") L60 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN" or metal or polysilicon or amorphous)	IBM_TDB) (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:32 AM
L63	85	L62 same4 incident	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:33 AM
L64	228102	(reflective near2 (material or layer or film))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 11:11 AM
L65	530599	("AlO" or (aluminum adj oxide)) or ("HfO" or (hafnium adj oxide))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 11:12 AM
L66	403	L64 near3 L65	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 11:12 AM
L67	2	L66 near4 (benefit or beneficial or advantages or advantageous or advantageously)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 11:13 AM
L68	2	L66 near10 (benefit or beneficial or advantages or advantageous or advantageously)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 11:13 AM
L69	31128	(anti or non) near2 L64	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 11:20 AM
L70	121	L65 near4 L69	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 11:20 AM
L71	2	L70 same (benefit or beneficial or advantages or advantageous or advantageously)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 11:20 AM
L72	2	(dope or doping or implanting or implant or implants implantation or dopes) near2 (light adj incident adj surface)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 12:04 PM
L73	6	(dope or doping or implanting or implant or implants implantation or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2017/02/06 12:05 PM

L74	13	dopes) near2 (light adj2 incident adj2 surface) (dope or doping or implanting or implant or implants implantation or dopes) near4 (light adj2 incident adj2 surface)	IBM_TDB) (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 12:05 PM
L75	167141	(doped or implanted) adj2 (region or section or portion or part)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 12:13 PM
L76	1	L75 near4 (light adj2 incident adj2 surface)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 12:13 PM
L77	26	L75 near10 (light adj2 incident adj2 surface)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 12:15 PM
L78	25	L77 not L76	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 12:15 PM
L79	1	("9064764").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2017/02/06 12:20 PM
L80	44833	(light adj2 incident adj2 surface)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 05:49 PM
L81	167141	(doped or implanted) adj2 (region or section or portion or part)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 05:49 PM
L82	9	L80 near6 L81	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 05:49 PM
L83	364064	(light adj2 surface)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 05:50 PM
L84	54	L83 near4 L81	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 05:50 PM
L85	53	L84 not L82	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 05:50 PM
L86	21	("20030214595" "20030228883" "20050093100" "20060086956" "20060128087" "20070189583" "20070237504" "200	(US-PGPUB; USPAT)	OR	ON	ON	2017/02/07 07:43 AM

L87	21	80158398 "20080192133 "20080284884 "20100200658 "20110194100 "20110292380 "20140198240 "5101260 "5600130 "5626687 "5635089 "6082858 "6204506 "6907135").PN . ("20030214595 "20030228883 "20050093100 "20060086956 "20060128087 "20070189583 "20070237504 "20080158398 "20080192133 "20080284884 "20100200658 "20110194100 "20110292380 "20140198240 "5101260 "5600130 "5626687 "5635089 "6082858 "6204506 "6907135").PN .	(US-PGPUB; USPAT)	OR	ON	ON	2017/02/07 07:44 AM
L88	20	("20010044266 "20050088634 "20080173620 "20090027640 "20090093100 "20090114630 "20090308457 "20100140768 "20130135439 "4886958 "5351446 "5641969 "5727096 "6327022 "6331885 "6340281 "7800684 "7897942 "9184204 "9369641").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2017/06/01 01:32 PM
L89	20	("20040256561 "20070063219 "20070103580 "20070125951 "20080142686 "20090009596 "20090174026 "20090242019 "20100102366 "20110003424 "20110019050 "20120080733 "20120274744 "20140352779 "20150076468 "5236863 "5410168 "8076746 "9419159 "9673250").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2018/02/15 10:41 AM
L90	24107	(layer or film) near3 (different near2 (refractive or refraction or refracting))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:45 AM
L91	18	L90 near4 isolation	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:45 AM

L92	5	L91 same4 (pixel or pixels)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:45 AM
L93	13	L91 not L92	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:47 AM
L94	22683	bragg adj2 (reflective or reflector)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:51 AM
L95	58	L94 near4 isolation	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:52 AM
L96	6	L95 same4 (pixel or pixels)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:52 AM
L97	52	L95 not L96	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:55 AM
L98	29452	(isolation or isolating or insulation or insulating) near2 (multi-layer or multiple)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:57 AM
L99	19	L98 near10 (different near2 (refractive or refraction or refracting))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:58 AM
L100	48	L98 near3 (silicon adj2 dioxide)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 01:05 PM
L101	1	L100 same4 (pixel or pixels)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 01:05 PM
L102	19531	(isolation or isolating or insulation or insulating) near2 (silicon adj2 dioxide)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 01:08 PM
L103	53	L102 near4 (benefit or advantage or beneficial or advantageous)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 01:08 PM
L104	4006	(isolation or isolating or insulation or insulating) near2 ("Al.sub.2O.sub.3")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 01:10 PM
L105	450872	aluminum adj oxide	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15

L106	57928	hafnium adj oxide	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	01:11 PM 2018/02/15 01:11 PM
L107	2014	(isolation or isolating or insulation or insulating) near6 L105 near6 L106	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 01:11 PM
L108	45	("0969984" "200501842 91" "20050184353" "20 080191296" "20080303 932" "20090090988" "2 0090096049" "2009020 0625" "20090278967" " 20100108864" "201001 28161" "20100201834" " 20110241148" "20110 241152" "20120025199 " "20120049306" "2012 0147241" "2012015312 7" "20120153128" "201 20188431" "201202176 02" "20120228473" "20 130020468" "20130207 212" "20140054662" "2 0140374868" "2017024 4920" "4546945" "5583 704" "5802091" "61315 11" "6131512" "647909 3" "6690968" "7315014" "7728274" "8268403" " 8445950" "8445985" "8 530264" "8604405" "87 29678" "8928784" "906 4762" "9478572").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2018/09/25 01:45 PM
L109	1	("20160329366").PN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2018/09/25 01:57 PM
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L111	0	H01L27/14637.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/09/25 02:06 PM
L112	17402	H01L27/14627.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/09/25 02:06 PM
L113	4188	H01L27/14629.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2018/09/25 02:06 PM

L114	12683	H01L27/14685.CPC.	IBM_TDB) (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/09/25 02:06 PM
L115	12130	H01L27/14625.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/09/25 02:06 PM
L116	4452	H01L27/1462.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/09/25 02:06 PM
L118	7967	H01L27/14645.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/09/25 02:07 PM
L119	11554	H01L27/14689.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/09/25 02:07 PM
L121	43	"2011035188"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2020/05/04 02:27 PM
L122	0	("2011035188").PN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/05/04 02:27 PM
L123	1	("20110035188").PN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/05/04 02:27 PM
L124	1	("20190198538").PN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/12/18 11:17 AM
L125	1	("20190198538").PN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/12/18 02:54 PM
L126	3741	H01L27/14607.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/12/18 04:06 PM
L127	12	(photosensitive ADJ imaging ADJ devices ADJ associated)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/18 11:23 AM
L128	1061	(interacting adj2	(US-PGPUB; USPAT;	OR	ON	ON	2022/10/18

		electromagnetic adj2 radiation)	USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				11:25 AM
L129	6296	(textured ADJ region)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/18 11:27 AM
L130	35	L129 near2 operable	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/18 11:27 AM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N49	1	(257/432).CCLS.	(US-PGPUB; USPAT)	OR	ON	ON	2015/01/05 11:54 AM
N120	1785	H01L27/1463.CPC.	(USPAT)	OR	ON	ON	2018/09/25 02:06 PM

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Application	Document	Mailroom Date	Attorney Docket No.
17214333	CTNF	10/21/2022	143705.000335
	892	10/21/2022	143705.000335

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PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors	:	Pralle et al.	)	
			)	Examiner:
Applicant	:	SiOnyx LLC	)	Long PHAM
			)	
Applicant No.	:	17/214,333	)	Art Unit:
			)	2814
Cnfrm. No.	:	1018	)	
			)	
Filed	:	March 26, 2021	)	
			)	
For	:	PIXEL ISOLATION ELEMENTS, DEVICES	)	
		AND ASSOCIATED METHODS	)	

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

In response to the October 21, 2022, non-final office action, please amend the above-identified patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 5 of this paper.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A light trapping device, comprising:
at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;
a backside light trapping material ~~substantially~~ at least partially covering the backside surface; and
a peripheral light trapping material substantially covering the peripheral sidewall;
wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel;
wherein at least one of the backside light trapping material or the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.

2-3. (Canceled).

4. (Currently Amended) The device of claim [[3]] 1, wherein the two low refractive index materials have a refractive index of less than about 2.1.

5. (Original) The device of claim 4, wherein at least one of the two low refractive index material includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.

6. (Original) The device of claim 4, wherein the at least one of the two low refractive index materials includes a member selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.

7. (Currently Amended) The device of claim [[3]] 1, wherein the high refractive index material includes a material having a refractive index of greater than or equal to about 2.1.

8. (Original) The device of claim 7, wherein the high refractive index material includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and combinations thereof.

9. (Currently Amended) The device of claim [[2]] 1, wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field.

10. (Original) The device of claim 9, wherein the dopant is boron or antimony.

11. (Original) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials, and wherein the difference in refractive index between the first material and the two second materials is at least 0.2.

12. (Original) The device of claim 1, wherein the peripheral sidewall extends completely around the pixel periphery.

13. (Original) The device of claim 1, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

14. (Original) The device of claim 1, further comprising a frontside light trapping material at least partially covering the light incident surface.

15. (Original) The device of claim 14, wherein the frontside light trapping material is an antireflective layer coating.

16. (Original) The device of claim 14, wherein the frontside light trapping material is a reflective layer having an aperture to allow entry of light into the pixel, wherein the reflective layer is operable to reflect light impinging thereupon from inside the pixel back into the pixel.

17. (Original) The device of claim 16, further comprising a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.

18. (Original) The device of claim 16, wherein the aperture has an effective surface area of 90% of the incident light surface total surface area.

19. (Original) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

20. (Original) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface.

21-33. (Canceled)

- 5 -

REMARKS

Applicant has cancelled claims 2-3 and has amended claims 1, 4, 7, and 9 as set forth above. No new matter has been added by way of these amendments. Applicant notes with appreciation the Office's clarification by phone that dependent claims 2-11 (not addressed in the outstanding Office Action) would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In view of the above amendments and the following remarks, reconsideration of the outstanding office action is respectfully requested.

The Office has rejected: claims 1, 12-17, and 20 under pre-AIA 35 U.S.C. 102(a) as being anticipated by Haddad et al. (WO2011035188); and claims 18-19 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Haddad et al. (WO2011035188). Accordingly, Applicant has amended claim 1 to substantially incorporate allowable dependent claim 2 as set forth above. In view of the foregoing amendments and remarks, the Office is respectfully requested to reconsider and withdraw the outstanding rejection and objection to the claims.

In view of all of the foregoing, Applicant submits that this case is in condition for allowance and such allowance is earnestly solicited.

Respectfully submitted,

Date: January 19, 2023

/Gunnar Leinberg/
Gunnar G. Leinberg
Registration No. 35,584

Troutman Pepper Hamilton Sanders LLP
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Rochester, NY 14625
Telephone: (585) 270-2103
Facsimile: (800) 521-1023

Electronic Acknowledgement Receipt

EFS ID:	47404175
Application Number:	17214333
International Application Number:	
Confirmation Number:	1018
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	11951
Filer:	Gunnar G. Leinberg
Filer Authorized By:	
Attorney Docket Number:	143705.000335
Receipt Date:	20-JAN-2023
Filing Date:	26-MAR-2021
Time Stamp:	15:39:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		20230120_Amendment_143705_000335.pdf	143491 e109bc735993953784f15ad8af3c657513d dec0	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Request for Reconsideration-After Non-Final Rejection	1	1
	Claims	2	4
	Applicant Arguments/Remarks Made in an Amendment	5	5
Warnings:			
Information:			
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 17/214,333		Filing Date 03/26/2021		☐ To be Mailed		
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO										
APPLICATION AS FILED - PART I										
		(Column 1)	(Column 2)							
FOR		NUMBER FILED	NUMBER EXTRA		RATE (\$)		FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))		N/A	N/A		N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A					
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*		x \$100 =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*		x \$480 =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL					
APPLICATION AS AMENDED - PART II										
		(Column 1)	(Column 2)		(Column 3)					
AMENDMENT	01/20/2023	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0		x \$100 =		0	
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0		x \$480 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
							TOTAL ADD'L FEE		0	
		(Column 1)	(Column 2)		(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=		x \$0 =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x \$0 =			
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
							TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.							LIE			
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".							/TINA M. BELL/			
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".										
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

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11951 7590 03/24/2023
Troutman Pepper Hamilton Sanders LLP (Rochester)
70 Linden Oaks
Suite 210
Rochester, NY 14625

EXAMINER

PHAM, LONG

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 03/24/2023

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/214,333	03/26/2021	Martin U. Pralle	143705.000335	1018

TITLE OF INVENTION: PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	06/26/2023

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

11951 7590 03/24/2023
Troutman Pepper Hamilton Sanders LLP (Rochester)
70 Linden Oaks
Suite 210
Rochester, NY 14625

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/214,333	03/26/2021	Martin U. Pralle	143705.000335	1018

TITLE OF INVENTION: PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	06/26/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAM, LONG	2814	257-432000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

- ☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/214,333	03/26/2021	Martin U. Pralle	143705.000335	1018
11951	7590	03/24/2023	EXAMINER	
Troutman Pepper Hamilton Sanders LLP (Rochester)			PHAM, LONG	
70 Linden Oaks			ART UNIT	
Suite 210			PAPER NUMBER	
Rochester, NY 14625			2814	
DATE MAILED: 03/24/2023				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.** Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b) (2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/214,333	Applicant(s) Pralle et al.	
	Examiner LONG PHAM	Art Unit 2814	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to AMENDMENT DATED 1/20/23.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1 and 4-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

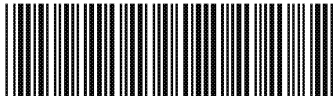
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.	6. ☐ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	

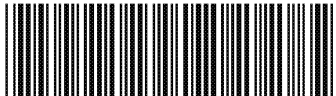
/LONG PHAM/ Primary Examiner, Art Unit 2814	
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Issue Classification 	Application/Control No. 17/214,333	Applicant(s)/Patent Under Reexamination Pralle et al.
	Examiner LONG PHAM	Art Unit 2814

CPC						
Symbol					Type	Version
H01L	/	27	/	1463	F	2013-01-01
H01L	/	27	/	14627	I	2013-01-01
H01L	/	27	/	14629	I	2013-01-01
H01L	/	27	/	14685	I	2013-01-01
H01L	/	27	/	14625	I	2013-01-01
H01L	/	27	/	1462	I	2013-01-01
H01L	/	27	/	14607	I	2013-01-01
H01L	/	27	/	14645	I	2013-01-01
H01L	/	27	/	14689	I	2013-01-01

CPC Combination Sets					
Symbol		Type	Set	Ranking	Version
	/				

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	18	
/LONG PHAM/ Primary Examiner, Art Unit 2814	21 March 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

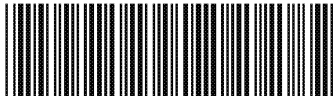
Issue Classification 	Application/Control No. 17/214,333	Applicant(s)/Patent Under Reexamination Pralle et al.
	Examiner LONG PHAM	Art Unit 2814

INTERNATIONAL CLASSIFICATION			
CLAIMED			
H01L	/	27	/ 146
NON-CLAIMED			
	/		/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	18	
/LONG PHAM/ Primary Examiner, Art Unit 2814	21 March 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

Issue Classification 	Application/Control No. 17/214,333	Applicant(s)/Patent Under Reexamination Pralle et al.
	Examiner LONG PHAM	Art Unit 2814

☐ Claims renumbered in the same order as presented by applicant
 ☐ CPA
 ☐ T.D.
 ☐ R.1.47

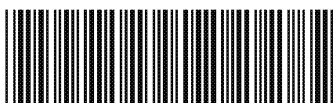
CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	10	12												
2	4	11	13												
3	5	12	14												
4	6	13	15												
5	7	14	16												
6	8	15	17												
7	9	16	18												
8	10	17	19												
9	11	18	20												

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	18	
/LONG PHAM/ Primary Examiner, Art Unit 2814 (Primary Examiner)	21 March 2023 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 6

U.S. Patent and Trademark Office

Part of Paper No.: 20230321

Search Notes 	Application/Control No. 17/214,333	Applicant(s)/Patent Under Reexamination Pralle et al.
	Examiner LONG PHAM	Art Unit 2814

CPC - Searched*		
Symbol	Date	Examiner
SEE ISSUE CLASSIFICATION	03/21/2023	LP

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

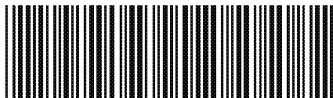
US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
UPDATED TEXT AND INTERFERENCE SEARCHES	03/21/2023	LP

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
H01L	27/1463	03/21/2023	LP

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<i>Index of Claims</i> 	Application/Control No. 17/214,333	Applicant(s)/Patent Under Reexamination Pralle et al.
	Examiner LONG PHAM	Art Unit 2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant					☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE								
Final	Original	07/02/2022	10/18/2022	03/21/2023						
	1	÷	✓	=						
	2	÷	○	-						
	3	÷	○	-						
	4	÷	○	=						
	5	÷	○	=						
	6	÷	○	=						
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	17	÷	✓	=						
	18	÷	✓	=						
	19	÷	✓	=						
	20	÷	✓	=						

Bibliographic Data

Application No: 17/214,333

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No ☐ Met After Allowance

Verified and Acknowledged:

/LONG PHAM/

Examiner's Signature

Initials

Title:

PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
03/26/2021	257	2814	143705.000335
RULE			

APPLICANTS

SiOnyx LLC, Beverly, MA,

INVENTORS

Martin U. Pralle, Wayland, MA, UNITED STATES

Jeffrey McKee, Tualatin, OR, UNITED STATES

Jason Sickler, Arlington, MA, UNITED STATES

CONTINUING DATA

This application is a CON of 16290740 03/01/2019 PAT 10985198

16290740 is a CON of 15216244 07/21/2016 PAT 10224359

15216244 is a CON of 14747875 06/23/2015 PAT 9905599

14747875 is a CON of 13841120 03/15/2013 PAT 9064764

13841120 has PRO of 61614275 03/22/2012

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

04/05/2021

STATE OR COUNTRY

UNITED STATES

ADDRESS

Troutman Pepper Hamilton Sanders LLP (Rochester)

70 Linden Oaks

Suite 210

Rochester, NY 14625

UNITED STATES

FILING FEE RECEIVED

\$1,820

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L2	84	US-3035052-\$.DID. OR US-20030029495- \$.DID. OR US- 20040222187-\$.DID. OR US-20050127401- \$.DID. OR US- 20050227390-\$.DID. OR US-20060011955- \$.DID. OR US- 20060079062-\$.DID. OR US-20060118781- \$.DID. OR US- 20060180885-\$.DID. OR US-20060231914- \$.DID. OR US- 20070145505-\$.DID. OR US-20080026550- \$.DID. OR US- 20080036022-\$.DID. OR US-20080044943- \$.DID. OR US- 20080076240-\$.DID. OR US-20080099804- \$.DID. OR US- 20080178932-\$.DID. OR US-20080258604- \$.DID. OR US- 20090065051-\$.DID. OR US-20090142879- \$.DID. OR US- 20090160983-\$.DID. OR US-20090194671- \$.DID. OR US- 20090200586-\$.DID. OR US-20090213883- \$.DID. OR US- 3487223-\$.DID. OR US-4277793-\$.DID. OR US-4419533-\$.DID. OR US-4493942-\$.DID. OR US-4514582-\$.DID. OR US-4536608-\$.DID. OR US-4663188-\$.DID. OR US-4829013-\$.DID. OR US-5080725-\$.DID. OR US-5081049-\$.DID. OR US-5100478-\$.DID. OR US-5114876-\$.DID. OR US-5164324-\$.DID. OR US-5322988-\$.DID. OR US-5346850-\$.DID. OR US-5597621-\$.DID. OR US-5714404-\$.DID. OR	(US-PGPUB; USPAT; USOCR; JPO; IBM_TDB)	OR	ON	ON	2014/06/25 02:14 PM

L3	7768	US-5731213-\$.DID. OR US-5792280-\$.DID. OR US-6147297-\$.DID. OR US-6498336-\$.DID. OR US-6580053-\$.DID. OR US-6583936-\$.DID. OR US-6667528-\$.DID. OR US-6759262-\$.DID. OR US-6800541-\$.DID. OR US-7057256-\$.DID. OR US-7091411-\$.DID. OR US-7109517-\$.DID. OR US-7247527-\$.DID. OR US-7314832-\$.DID. OR US-7354792-\$.DID. OR US-7390689-\$.DID. OR US-7442629-\$.DID. OR US-7456452-\$.DID. OR US-7482532-\$.DID. OR US-7498650-\$.DID. OR US-7504325-\$.DID. OR US-7504702-\$.DID. OR US-7511750-\$.DID. OR US-7745901-\$.DID. OR US-7781856-\$.DID. OR US-7816220-\$.DID. OR US-7847253-\$.DID. OR US-7884439-\$.DID. OR US-7884446-\$.DID. OR US-8030726-\$.DID. OR US-8058615-\$.DID. OR US-8207051-\$.DID. OR US-8476681-\$.DID. OR US-3666484-\$.DID. OR US-2030766-\$.DID. OR JP-07173484-\$.DID. OR JP-071734840721- \$.DID. OR JP- 2008187003-\$.DID. OR JP-2011091128-\$.DID. OR JP-2152226-\$.DID. OR JP-63116421- \$.DID. OR JP-9298308- \$.DID. OR KR- 20010061058-\$.DID. OR KR-20100118864- \$.DID. OR WO- 2006086014-\$.DID. OR WO-2009100023- \$.DID. OR WO- 2011035188-\$.DID. OR WO-2011119618- \$.DID. (light adj2 (trapping or trapped))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 02:16 PM
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L4	11	L2 and L3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 02:16 PM
L5	2251	(reflector or Bragg) and L3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:40 PM
L6	14	(reflector or Bragg) and L2	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:41 PM
L7	888	(reflector or Bragg) near3 backside	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:55 PM
L8	51623	(reflector or Bragg) near3 (side or sidewall or edge or wall)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:55 PM
L9	112640	pixel near5 (side or sidewall or edge or wall)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:56 PM
L10	143	L7 same L8	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:56 PM
L11	2	L9 same4 L10	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:56 PM
L12	3	L9 and L10	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:57 PM
L13	1	L12 not L11	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:57 PM
L14	179	L7 same4 L8	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:58 PM
L15	145	L14 and (photodiode or pixel or light)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:59 PM
L16	129	L14 same10 (photodiode or pixel or light)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 03:59 PM
L17	128	L14 same8 (photodiode or pixel or light)	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2014/06/25 03:59 PM

L18	1204	(reflector or Bragg) near5 backside	JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:09 PM
L19	71202	(reflector or Bragg) near5 (side or sidewall or edge or wall)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:09 PM
L20	280	L18 same4 L19	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:09 PM
L21	195	L20 same4 (photodiode or pixel or light)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:09 PM
L22	7	L18 same2 L9	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:10 PM
L23	7	L22 same4 (photodiode or pixel or light)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:10 PM
L24	217	L18 same L19	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:13 PM
L25	0	(light adj2 sensitive adj2 pixel) same4 L24	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:14 PM
L26	0	(light adj2 sensitive adj2 pixel) and L24	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:14 PM
L27	14	pixel same4 L24	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:14 PM
L28	7	L27 and index	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/25 04:18 PM
L29	26925	(high adj2 index) near3 (layer or film)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:48 PM
L30	27823	(low adj2 index) near3 (layer or film)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:48 PM

L31	12802	L29 near10 L30	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:48 PM
L32	1170	(reflector or Bragg) same L31	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:49 PM
L33	611	(reflector or Bragg) near10 L31	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:49 PM
L34	4200	L30 near5 ("between")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:49 PM
L35	1972	L34 near10 L29	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:50 PM
L36	81	(reflector or Bragg) near10 L35	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:50 PM
L37	188	L29 near5 (polysilicon or polycrystalline or poly or (amorphous adj2 silicon) or germanium)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:53 PM
L38	2500	L30 near5 (oxide or nitride or oxynitride or oxynitrides)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:53 PM
L39	14	L37 near20 L38	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:53 PM
L40	0	(reflector or Bragg) same L39	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:54 PM
L41	0	L39 near20 ("between")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 12:54 PM
L42	51	backside near6 (textured near2 (layer or film))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 01:12 PM
L43	10	L42 AND (H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 01:25 PM

L44	5	H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.) L39 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 01:25 PM
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L45	2	H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.) L36 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2014/06/26 01:25 PM
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L46	1	H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.) ("20140138785").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2015/01/05 11:26 AM
L47	3930	(257/432).CCLS.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2015/01/05 11:54 AM
L48	218	(257/228).CCLS.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2015/01/05 11:54 AM
L50	1	("9373732").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2016/07/13 03:10 PM
L51	1	("9373732").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2016/07/15 10:13 AM
L52	395	reflective near3 (aluminum adj oxide)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/15 01:07 PM
L53	35214	(rough or textured) near2 (layer or film)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:24 AM
L54	44833	light adj2 incident adj2 surface	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:24 AM
L55	38	L53 same L54	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:25 AM
L56	10	L55 same efficiency	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:25 AM
L57	0	L55 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:29 AM
L58	0	L55 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:30 AM
L59	3	L55 same (metal or polysilicon or amorphous)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:30 AM
L60	1864	L53 same efficiency	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:32 AM
L61	42	L60 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2017/02/06 01:32 AM

L62	351	"SiN") L60 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN" or metal or polysilicon or amorphous)	IBM_TDB) (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:32 AM
L63	85	L62 same4 incident	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 01:33 AM
L64	228102	(reflective near2 (material or layer or film))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 11:11 AM
L65	530599	("AlO" or (aluminum adj oxide)) or ("HfO" or (hafnium adj oxide))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 11:12 AM
L66	403	L64 near3 L65	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 11:12 AM
L67	2	L66 near4 (benefit or beneficial or advantages or advantageous or advantageously)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 11:13 AM
L68	2	L66 near10 (benefit or beneficial or advantages or advantageous or advantageously)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 11:13 AM
L69	31128	(anti or non) near2 L64	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 11:20 AM
L70	121	L65 near4 L69	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 11:20 AM
L71	2	L70 same (benefit or beneficial or advantages or advantageous or advantageously)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 11:20 AM
L72	2	(dope or doping or implanting or implant or implants implantation or dopes) near2 (light adj incident adj surface)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 12:04 PM
L73	6	(dope or doping or implanting or implant or implants implantation or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2017/02/06 12:05 PM

L74	13	dopes) near2 (light adj2 incident adj2 surface) (dope or doping or implanting or implant or implants implantation or dopes) near4 (light adj2 incident adj2 surface)	IBM_TDB) (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 12:05 PM
L75	167141	(doped or implanted) adj2 (region or section or portion or part)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 12:13 PM
L76	1	L75 near4 (light adj2 incident adj2 surface)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 12:13 PM
L77	26	L75 near10 (light adj2 incident adj2 surface)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 12:15 PM
L78	25	L77 not L76	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 12:15 PM
L79	1	("9064764").PN.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2017/02/06 12:20 PM
L80	44833	(light adj2 incident adj2 surface)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 05:49 PM
L81	167141	(doped or implanted) adj2 (region or section or portion or part)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 05:49 PM
L82	9	L80 near6 L81	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 05:49 PM
L83	364064	(light adj2 surface)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 05:50 PM
L84	54	L83 near4 L81	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 05:50 PM
L85	53	L84 not L82	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/02/06 05:50 PM
L86	21	("20030214595" "20030228883" "20050093100" "20060086956" "20060128087" "20070189583" "20070237504" "200	(US-PGPUB; USPAT)	OR	ON	ON	2017/02/07 07:43 AM

L87	21	80158398 "20080192133 "20080284884 "20100200658 "20110194100 "20110292380 "20140198240 "5101260 "5600130 "5626687 "5635089 "6082858 "6204506 "6907135").PN . ("20030214595 "20030228883 "20050093100 "20060086956 "20060128087 "20070189583 "20070237504 "20080158398 "20080192133 "20080284884 "20100200658 "20110194100 "20110292380 "20140198240 "5101260 "5600130 "5626687 "5635089 "6082858 "6204506 "6907135").PN .	(US-PGPUB; USPAT)	OR	ON	ON	2017/02/07 07:44 AM
L88	20	("20010044266 "20050088634 "20080173620 "20090027640 "20090093100 "20090114630 "20090308457 "20100140768 "20130135439 "4886958 "5351446 "5641969 "5727096 "6327022 "6331885 "6340281 "7800684 "7897942 "9184204 "9369641").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2017/06/01 01:32 PM
L89	20	("20040256561 "20070063219 "20070103580 "20070125951 "20080142686 "20090009596 "20090174026 "20090242019 "20100102366 "20110003424 "20110019050 "20120080733 "20120274744 "20140352779 "20150076468 "5236863 "5410168 "8076746 "9419159 "9673250").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2018/02/15 10:41 AM
L90	24107	(layer or film) near3 (different near2 (refractive or refraction or refracting))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:45 AM
L91	18	L90 near4 isolation	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:45 AM

L92	5	L91 same4 (pixel or pixels)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:45 AM
L93	13	L91 not L92	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:47 AM
L94	22683	bragg adj2 (reflective or reflector)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:51 AM
L95	58	L94 near4 isolation	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:52 AM
L96	6	L95 same4 (pixel or pixels)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:52 AM
L97	52	L95 not L96	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:55 AM
L98	29452	(isolation or isolating or insulation or insulating) near2 (multi-layer or multiple)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:57 AM
L99	19	L98 near10 (different near2 (refractive or refraction or refracting))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 10:58 AM
L100	48	L98 near3 (silicon adj2 dioxide)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 01:05 PM
L101	1	L100 same4 (pixel or pixels)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 01:05 PM
L102	19531	(isolation or isolating or insulation or insulating) near2 (silicon adj2 dioxide)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 01:08 PM
L103	53	L102 near4 (benefit or advantage or beneficial or advantageous)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 01:08 PM
L104	4006	(isolation or isolating or insulation or insulating) near2 ("Al.sub.2O.sub.3")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 01:10 PM
L105	450872	aluminum adj oxide	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15

L106	57928	hafnium adj oxide	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	01:11 PM 2018/02/15 01:11 PM
L107	2014	(isolation or isolating or insulation or insulating) near6 L105 near6 L106	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/15 01:11 PM
L108	45	("0969984" "200501842 91" "20050184353" "20 080191296" "20080303 932" "20090090988" "2 0090096049" "2009020 0625" "20090278967" " 20100108864" "201001 28161" "20100201834" " 20110241148" "20110 241152" "20120025199 " "20120049306" "2012 0147241" "2012015312 7" "20120153128" "201 20188431" "201202176 02" "20120228473" "20 130020468" "20130207 212" "20140054662" "2 0140374868" "2017024 4920" "4546945" "5583 704" "5802091" "61315 11" "6131512" "647909 3" "6690968" "7315014" "7728274" "8268403" " 8445950" "8445985" "8 530264" "8604405" "87 29678" "8928784" "906 4762" "9478572").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2018/09/25 01:45 PM
L109	1	("20160329366").PN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2018/09/25 01:57 PM
L110	9556	H01L27/1463.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/09/25 02:06 PM
L111	0	H01L27/14637.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/09/25 02:06 PM
L112	17402	H01L27/14627.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/09/25 02:06 PM
L113	4188	H01L27/14629.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2018/09/25 02:06 PM

L114	12683	H01L27/14685.CPC.	IBM_TDB) (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/09/25 02:06 PM
L115	12130	H01L27/14625.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/09/25 02:06 PM
L116	4452	H01L27/1462.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/09/25 02:06 PM
L118	7967	H01L27/14645.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/09/25 02:07 PM
L119	11554	H01L27/14689.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/09/25 02:07 PM
L121	43	"2011035188"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2020/05/04 02:27 PM
L122	0	("2011035188").PN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/05/04 02:27 PM
L123	1	("20110035188").PN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/05/04 02:27 PM
L124	1	("20190198538").PN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/12/18 11:17 AM
L125	1	("20190198538").PN.	(US-PGPUB; USPAT; USOCR)	OR	OFF	OFF	2020/12/18 02:54 PM
L126	3741	H01L27/14607.CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/12/18 04:06 PM
L127	12	(photosensitive ADJ imaging ADJ devices ADJ associated)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/18 11:23 AM
L128	1061	(interacting adj2	(US-PGPUB; USPAT;	OR	ON	ON	2022/10/18

		electromagnetic adj2 radiation)	USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				11:25 AM
L129	6296	(textured ADJ region)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/18 11:27 AM
L130	35	L129 near2 operable	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/18 11:27 AM
L131	2	"20210217788"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO,	OR	ON	ON	2023/03/21 07:33 PM

			NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
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PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N49	1	(257/432).CCLS.	(US-PGPUB; USPAT)	OR	ON	ON	2015/01/05 11:54 AM
N120	1785	H01L27/1463.CPC.	(USPAT)	OR	ON	ON	2018/09/25 02:06 PM
N121	6967	H01L27/1463.CPC.	(US-PGPUB; USPAT)	OR	ON	ON	2023/03/21 07:52 PM

To: USPTOinboxroc@pepperlaw.com,BadumK@pepperlaw.com,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 11951

Mar 24, 2023 03:24:08 AM

Dear PAIR Customer:

Troutman Pepper Hamilton Sanders LLP (Rochester)
70 Linden Oaks
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Rochester, NY 14625
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 11951 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

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Application	Document	Mailroom Date	Attorney Docket No.
17214333	NOA	03/24/2023	143705.000335

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If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

Monday - Friday 6:00 a.m. to 12:00 a.m.

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UNITED STATES PATENT AND TRADEMARK OFFICE
PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders, and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

11951 7590 03/24/2023
Troutman Pepper Hamilton Sanders LLP (Rochester)
70 Linden Oaks
Suite 210
Rochester, NY 14625

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/214,333	03/26/2021	Martin U. Pralle	143705.000335	1018

TITLE OF INVENTION: PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	06/26/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAM, LONG	2814	257-432000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Troutman Pepper Hamilton
Sanders LLP (Rochester)

2.....
3.....

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE (CITY and STATE OR COUNTRY)

SiOnyx, LLC

Beverly, MA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies

4b. Method of Payment: (Please first reuply any previously paid fee shown above)

- ☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

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5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature **/Gunnar G. Leinberg/**

Date **June 21, 2023**

Typed or printed name **Gunnar G. Leinberg**

Registration No. **35,584**

Electronic Patent Application Fee Transmittal				
Application Number:		17214333		
Filing Date:		26-Mar-2021		
Title of Invention:		PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS		
First Named Inventor/Applicant Name:		Martin U. Pralle		
Filer:		Gunnar G. Leinberg/Marlene Chappe		
Attorney Docket Number:		143705.000335		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1200

Electronic Acknowledgement Receipt

EFS ID:	48188248
Application Number:	17214333
International Application Number:	
Confirmation Number:	1018
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	11951
Filer:	Gunnar G. Leinberg/Marlene Chappe
Filer Authorized By:	Gunnar G. Leinberg
Attorney Docket Number:	143705.000335
Receipt Date:	21-JUN-2023
Filing Date:	26-MAR-2021
Time Stamp:	18:27:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 1200
RAM confirmation Number	E20236KI28337435
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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	20230621_Issue_Fee_Transmit al_143705_000335.pdf	125249 467332c5b24f42795e58885ee93768c432151578	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	37682 39d16f4642b70beb47b4fb89c59d2db1f918922f	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			162931		
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/214,333	08/08/2023	11721714	143705.000335	1018

11951 7590 07/19/2023

Troutman Pepper Hamilton Sanders LLP (Rochester)
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ISSUE NOTIFICATION

The projected patent number and issue date are specified above. The patent will issue electronically. The electronically issued patent is the official patent grant pursuant to 35 U.S.C. § 153. The patent may be accessed on or after the issue date through Patent Center at <https://patentcenter.uspto.gov/>. The patent will be available in both the public and the private sides of Patent Center. Further assistance in electronically accessing the patent, or about Patent Center, is available by calling the Patent Electronic Business Center at 1-888-217-9197.

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Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment is 46 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional inventors):

Martin U. Pralle, Wayland, MA;
Jeffrey McKee, Tualatin, OR;
Jason Sickler, Arlington, MA;

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

SiOnyx LLC, Beverly, MA;

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TO: BadumK@pepperlaw.com,USPTOinboxroc@pepperlaw.com
FROM: noreply@uspto.gov
CC: patentcenter_eofficeaction@uspto.gov
SUBJECT: USPTO: Patent Electronic System - Correspondence Notification for Customer Number 11951

Thu Jul 20 06:19:04 EDT 2023

Dear Patent Center Customer:

Correspondence Address:

Troutman Pepper Hamilton Sanders LLP (Rochester)
70 Linden Oaks
Suite 210
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Application	Document	Mailroom Date	Attorney Docket No.
17214333	ISSUE.NTF	07/19/2023	143705.000335

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/214,333	03/26/2021	Martin U. Pralle	143705.000335	1018
11951	7590	08/08/2023	EXAMINER	
Troutman Pepper Hamilton Sanders LLP (Rochester)			PHAM, LONG	
70 Linden Oaks				
Suite 210				
Rochester, NY 14625			ART UNIT	PAPER NUMBER
			2823	
			NOTIFICATION DATE	DELIVERY MODE
			08/08/2023	ELECTRONIC

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The time period for reply, if any, is set in the attached communication.

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APPLICATION NO.	ISSUE DATE	PATENT NO.
17/214,333	08-Aug-2023	11721714

Troutman Pepper Hamilton Sanders LLP (Rochester)
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TO: BadumK@pepperlaw.com,USPTOinboxroc@pepperlaw.com
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SUBJECT: USPTO: Patent Electronic System - eGrant Notification for Customer Number 11951

Tue Aug 08 06:20:08 EDT 2023

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17214333	11721714	EGRANT.NTF	08/08/2023	143705.000335

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