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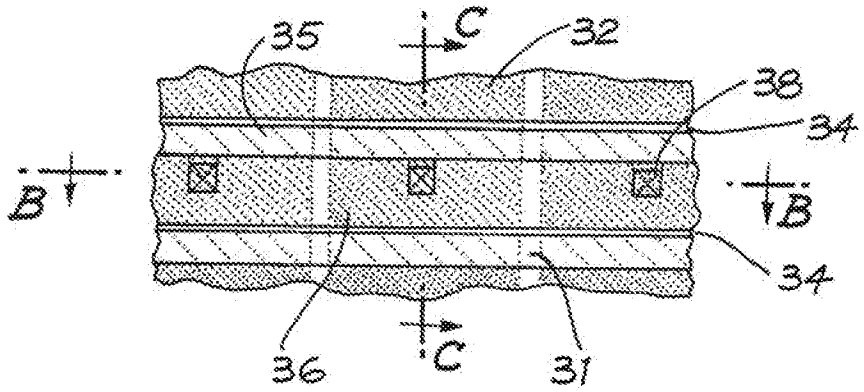
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(54) Title: SCHOTTKY JUNCTION CHARGE COUPLED DEVICE



(57) Abstract

The present invention provides a Schottky Junction CCD array comprising a plurality of adjacent Schottky Junction CCDs which are infra-red sensitive, and which are separated by a low dose impurity implant (31) of the same polarity as a higher dose implant (35, 36) within the CCD channel (32). The individual gates are comprised of a metal silicide layer on the semiconductor substrate. The silicide layer stretches all the way across the array. Also, these silicide strips are separated by gaps (34) of sub-micron dimensions. This construction leads to substantially a 100 % fill factor for the array. Nearly all of the array will be IR sensitive.

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Schottky Junction Charge Coupled Device

The present invention relates generally to the design and fabrication of a Schottky Junction Charge Coupled Device, and more particularly, but not exclusively, to a Schottky Junction Charge Coupled Device arranged as a photo-optic detector, particularly to the design and fabrication of detector arrangements using low Schottky barrier height metal silicide layers on a silicon substrate for infra-red (IR) detection, wherein each of the detector elements in the arrangement forms one of a plurality of Schottky gates for infra-red sensitive Schottky Charge Coupled Devices.

Prior art silicide infra-red detector arrays are known wherein vertical and horizontal Charge Coupled Device (CCD) shift registers are provided to transfer charges generated in separate infra-red detectors to the detector array output. This detector array architecture is known as the "interline transfer scheme". Due to the area occupied by the shift registers, the detector fill factor (the ratio of active detector area to the area of the whole device) is, in practice, in the order of less than 50%.

To overcome the problem of low detector fill factors several approaches have been suggested. One way to boost the fill factor is the use of separate planes, one for Schottky silicide IR detection, and the other one as a silicon multiplexer network, bonded together with indium bumps, as described in US Patent No. 4,531,055. Another approach is to use micro-lenses on the device backside. These approaches lead to almost 100% detector fill factors, but the fabrication of these detector arrays is very costly.

Yet another approach to increase the detector fill factor is the use of CCDs which are infra-red sensitive. In Australian Patent No. 579027, the disclosure of which is incorporated herein by reference, a device is described which uses Schottky metal silicide CCD gates for both

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infra-red detection and charge transfer. One device described comprises a series of Schottky silicide gates in a Junction CCD arrangement. The metal silicide layers of each gate are separated from each other by a gap of a few microns.

Another device described in Australian Patent No. 579027 comprises a series of Schottky silicide gates which are separated from each other by MOS-type poly-silicon gates of a few microns to form a linear CCD. The area required by the MOS gates decreases the available space for the infra-red sensitive Schottky silicide gates.

In both the above devices, the individual linear CCDs which are made up by the Schottky silicide gates are placed side by side to build a two-dimensional detector array. Each linear CCD column is separated by channel stop diffusions of the opposite polarity as the CCD channel implant. On p type silicon implants, each gate also requires a guard barrier of opposite polarity implant at either side of the CCD gate, to prevent edge leakage current. The areas under the MOS poly-silicon gates and gaps between the metal silicide layers, and the areas covered by the channel stop diffusion and guard barriers, are non infra-red sensitive.

A problem occurs in Schottky Junction CCD arrangements with edge leakage current from the metal silicide layers. The present invention addresses solutions to the problems associated with this edge leakage current of reversed bias low Schottky barrier height metal gates on p-type silicon, which is prevented in conventional Schottky infra-red detectors by implanted guard rings.

The present invention provides a Schottky Junction CCD array comprising a plurality of Schottky Junction transfer gates on a semiconductor substrate, the array comprising at least two adjacent linear CCDs, each CCD

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comprising a plurality of adjacent Schottky Junction transfer gates, the adjacent CCDs being separated by a low dose semiconductor impurity implant of the same polarity as a higher dose buried channel implant used in the CCD channel.

Defining the boundaries between adjacent CCDs by a low dose semiconductor impurity implant of the same polarity as a higher dose buried channel implant surprisingly obviates the need for guard barriers (where the CCD is made from p-type implants into silicon) and channel stop diffusions. Edge leakage does not substantially occur and anti-blooming properties of the Schottky gates are maintained. A further advantage is that substantially the entire area of the CCD will be sensitive to radiation where the CCD is arranged as a radiation detector.

Each Schottky Junction transfer gate preferably comprises a metal silicide layer over a semiconductor impurity implant. Preferably, the metal silicide layers of adjacent gates extend in strips across adjacent CCDs.

Preferably, adjacent Schottky Junction transfer gates in each CCD are separated from each other by only sub-micron wide gaps. Silicon dioxide spacers are preferably used to separate the adjacent gates. Previously, adjacent gates in each CCD were separated by gaps of a few microns. Preferably, the Schottky Junction transfer gates are infra-red sensitive gates which are arranged to operate in a first mode as IR detection elements and in a second mode as gates of a CCD shift register.

The Schottky Junction CCD array is preferably a "frame transfer device". Preferably, an array of infra-red sensitive Schottky CCD gates is connected to an array of non-sensitive Schottky CCD gates for frame storage. The frame of information can then be read out

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line by line through a Schottky gate read-out CCD. The frame storage array could comprise an array of infra-red sensitive Schottky CCD gates shielded from IR radiation so they act as a storage array for charge from the array exposed to IR.

The semiconductor substrate preferably comprises n-type silicon and the CCD is formed by a p-type implant on the n-type silicon.

The present invention further provides a Schottky Junction CCD array comprising a plurality of Schottky Junction transfer gates on a semiconductor substrate, the array comprising at least two adjacent linear CCDs, each CCD comprising a plurality of adjacent Schottky Junction transfer gates, each Schottky Junction transfer gate comprising a layer of metal silicide over a semiconductor impurity implant, the metal silicide layers of adjacent gates extending in strips across adjacent CCDs in the array.

Preferably, the adjacent CCDs are separated by a low dose semiconductor impurity implant of the same polarity as a higher dose buried channel implant used in the CCD channel.

The device may also include sub-micron wide gaps between adjacent gates and may be a frame transfer device, and preferably the gates are IR sensitive, as discussed above.

An advantage of having the layer of silicide extending all the way across the CCD array is that the whole array underneath the silicide strip will be IR sensitive, unlike the case in the prior art where silicide layers of adjacent CCD columns are separated by a channel stop diffusion and also by opposite polarity implant guard rings.

The present invention yet further provides a Schottky Junction CCD array comprising a plurality of Schottky

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Junction transfer gates, on a semiconductor substrate, the array comprising at least two adjacent linear CCDs, each CCD comprising a plurality of adjacent Schottky Junction transfer gates, adjacent Schottky Junction transfer gates within the CCD being separated from each other by a gap of a micron or less wide in the direction of charge transfer. The gap is preferably of sub-micron dimension. Silicon dioxide spacers are preferably used to separate adjacent gates.

Adjacent CCDs may be separated by a low dose semiconductor impurity implant, metal silicide layers forming the Schottky Junction transfer gates may extend across adjacent CCDs, and the array may be a frame transfer device, and preferably the gates are IR sensitive, as discussed above.

An advantage of having adjacent gates separated by gaps of sub-micron dimension is that inversion layers caused by the reverse bias voltage connected to the silicide gates are formed in an overlapping manner, and guard rings are not needed. This also leads to more efficient charge transfer.

In order to improve resistance to radiation damage, the silicon dioxide spacers may be removed by etching, i.e. the SiO_2 spacers would only be used during the manufacturing process for the array.

The present invention yet further provides a frame transfer Schottky Junction CCD array comprising an upper array and a lower array, the upper array comprising at least two adjacent linear CCDs, each CCD comprising a plurality of adjacent Schottky Junction transfer gates on a semiconductor substrate, said transfer gates being radiation sensitive and being arranged to operate in a first mode as radiation detection elements and in a second mode as gates of a CCD shift register, and the lower frame comprising at least two adjacent linear CCDs, each

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comprising a plurality of adjacent Schottky Junction transfer gates, each upper CCD being able to transfer charge into a respective lower frame CCD for storage.

The upper array gates are preferably IR sensitive. In at least the upper frame array it is preferred that adjacent CCDs are separated by a low dose semiconductor impurity implant. It is also preferred that, in at least the upper array, that adjacent transfer gates in each CCD are separated by a gap of sub-micron width dimension. It is also preferred that, in at least the upper array, that metal silicide layers forming part of the transfer gates extend across the array over adjacent CCDs.

Preferably, both arrays include all the above features. An advantage of arranging the device as a frame transfer device is that similar fabrication techniques may be used for each array of the frame, which leads to ease of manufacture. In order to prevent the lower array producing charge it may be shielded from incident radiation..

A CCD array comprising adjacent radiation sensitive CCDs which are separated by a low dose impurity implant, adjacent gates being separated by a silicon dioxide spacer, results in a "Fully Integrated Schottky Array" (FISA), with a detector array of almost 100% fill factor.

A further advantage is that the FISA does not need metal oxide semiconductor type gates for separating the individual Schottky gates.

With channel separation of adjacent CCDs being by lower implant polarity, of the same implant as for the CCD channel, only a lower dose, this leads to the surprising advantage that guard rings for each individual Schottky gate within the CCD matrix are not needed. Edge leakage current does not substantially occur.

With such an FISA array, the whole matrix of Schottky CCDs including the channel separation implant may be

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infra-red sensitive. Only a small fraction under the sub-micron spacers separating the Schottky gates is non-infra-red sensitive. This leads to almost 100% detector fill factor.

Such an FISA is also only minimally affected by solar radiation because of the lack of gate oxides. As discussed above, the SiO_2 spacers may be removed by etching in order to improve further resistance to solar radiation.

The present invention further provides a Schottky Junction charge coupled device infra-red imaging array having substantially continuous infra-red sensitive elements with a fill factor substantially greater than fifty percent, said imaging array comprising:

a plurality of substantially contiguous conductive transfer electrodes disposed along a semiconductor substrate above a buried implant channel and providing means for serially shifting charge packets within the buried channel of said substrate when a sequence of control voltages is applied thereto,

each of said substantially contiguous transfer elements forming a rectifying metal to semiconductor contact known as a Schottky contact and having a barrier height sufficiently low to cause the Schottky contact to respond to infra-red radiation of wavelength substantially greater than the band to band absorption cutoff wavelength of the semiconductor,

said Schottky contact acting in a first mode as an infra-red detector element by photoemission of charge carriers from the metallic region of said Schottky contact to said buried channel of said semiconductor substrate and, in a second mode, to control movement of charge packets within said buried channel, operating in said first or second mode being determined by voltage sequences applied to said transfer electrodes,

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a dielectric passivating layer located over the transfer electrodes, and

a mirror located above the dielectric layer,

the transfer electrodes being sufficiently thin to enable transmission of infra-red light and the dielectric layer forming an optical cavity on top of the transfer electrode,

the buried implant channel comprising a central region of relatively high concentration dopant extending along the channel and bounded by regions of relatively low concentration dopant of the same polarity at its edges.

The present invention yet further provides a Schottky Junction charge coupled device infra-red imaging array having substantially contiguous infra-red sensitive elements with a fill factor substantially greater than fifty percent, said imaging array comprising:

a plurality of substantially contiguous conductive transfer electrodes disposed along a semiconductor substrate above a buried implant channel and providing means for serially shifting charge packets within the buried channel of said substrates when a sequence of control voltages is applied thereto,

each of said substantially contiguous transfer electrodes forming a rectifying metal to semiconductor contact known as a Schottky contact and having a barrier height sufficiently low to cause the Schottky contact to respond to infra-red radiation of wavelength substantially greater than the band to band absorption cutoff wavelength of the semiconductor,

said Schottky contact acting in a first mode as an infra-red detector element by photoemission of charge carriers from the metallic region of said Schottky contact to said buried channel of said semiconductor substrate and, in a second mode, to control movement of charge packets within said buried channel, operating in said

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first or second mode being determined by voltage sequences applied to said transfer electrodes,

the buried implant channel comprising a central region of relatively high concentration dopant extending along the channel and bounded by regions of relatively low concentration dopant of the same polarity at its edges.

Features and advantages of the present invention will become apparent from the following description of an embodiment thereof, by way of example only, with reference to the accompanying drawings, in which:-

Figure 1 illustrates in cross section the basic structure of a single conventional metal-silicide Schottky barrier infra-red detector;

Figure 2 illustrates in plan view the structure of a prior art Schottky Junction Charge Coupled Device.

Figure 3 schematically illustrates the layout of a frame transfer detector array designed in accordance with an embodiment of the present invention, and

Figures 3 and 4 A, B and C, illustrate in plan view and cross-sections elements of the Fully Integrated Schottky Array in accordance with an embodiment of the present invention.

The basic structure of a conventional metal silicide Schottky barrier infra-red detector is illustrated in Figure 1, from which it will be noted that photons of incident infra-red radiation 11 are transmitted from the back surface 12 of the detector to the silicide layer 13 via a dielectric anti-reflection coating 14 and a p-type silicon substrate 15. Silicides of metals such as platinum or palladium are characterised by low Schottky barrier height for p-type silicon and are therefore suitable for the formation of infra-red sensitive detectors. The quantum efficiency of the silicide infra-red detector is improved by putting an optical cavity on top of the thin silicide layer 13 comprising a

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dielectric layer 16 and an aluminium mirror 17. Light passing through the silicide 13 traverses the dielectric layer 16 and is reflected by the aluminium mirror 17 thereby providing additional opportunities for transmitted photons to be absorbed by silicide layer 13. During the integration time, when photons due to the incoming infra-red radiation 11 are absorbed in the silicide layer 13 creating electron-hole pairs, the metal-silicide layer 13 is reverse biased. Holes are absorbed by the p-type silicon substrate 15, while electrons stay in the silicide layer 13 as photo-current. This reverse bias voltage creates a high electric field at the edge of the extremely thin silicide layer 13, which would cause high leakage currents in p-type silicon. Therefore, a n-type guard ring 18 is integrated into the silicon substrate surrounding the edge of the silicide layer 13. The metal-silicide having a low Schottky barrier height on p-type silicon is characterised by a high Schottky barrier height on n-type silicon, thus preventing leakage current within the n-type doped guard ring 18.

In conventional infra-red detector arrays, such detectors are placed as an array, and the photo current of each individual detector is read-out by shift registers placed between the rows of detectors. Valuable space occupied by the shift registers can not be used for infra-red detection, leading to detector fill factors of less than 50%.

Figure 2 is a plan view of a portion of a prior art infra-red sensitive Schottky Junction CCD array such as the types disclosed in Australian Patent No. 579027. The CCD array, designated generally by reference numeral 100, is formed by p-type implants 101 (to form the CCD columns) on an n-type silicone substrate. It wold be possible to form the CCDs from n-type implants on p-type silicon, but

the wavelength response for such a CCD will be unsatisfactory. To obtain the required wavelength sensitivity p-type implants on n-type silicon need to be used. Each CCD gate is formed by a layer of metal silicide 102 over the channel implants 101 (silicides of metals such as platinum or palladium are suitable). In order to prevent edge leakage from each gate it is necessary to form guard barriers 103 at either side of the silicide 102. These guard barriers 103 are formed by n-type channel implants. Further, to separate each CCD column 101 channel stop diffusions 104 are required. These are also formed by n-type diffusions. The guard barriers 103 and channel stop diffusions 104 take up space that would otherwise be responsive to IR radiation, and reduce the fill factor of the CCD array. Overlying the CCD array will be a dielectric layer (not shown) and metallic contact layers (also not shown) connecting the CCDs up to two alternate phases of electrical potential (dia. 1, dia. 2) for operation of the device. The opposite side of the detector array may be coated with an anti-reflective layer.

The device operation is divided into two modes; the integration or detection mode and the read-out mode respectively. During the integration mode the silicide gates, and their respective overlying dielectric and metal layers,. work, as infra-red detectors as described with reference to Fig. 1, where the silicide is an infra-red sensitive region and the dielectric with overlying metal may act as an optical cavity of the detector in addition to its main role. The infra-red radiation coming from the substrate direction generates charges in the infra-red sensitive region where positive charges (holes) are ejected to the p-type channel. When the phase 1 is "on" during the integration mode, the charges will accumulate in the well regions of the gates connected to that phase

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and they will choose the shortest way to go to these regions of lowest potential from the regions where they were generated. The size of the charge packages accumulated under the gates during the integration is proportional tothe amount of infra=red radiation falling in their close proximity. Thus an infra-red line image or two dimensional image is generated from a one or two dimensional array respectively.

After operating in the integration mode for a predetermined period, the second mode of operation is initiated, within which the accumulated charge is read out to the output stage. During this mode, the device has either to be covered from infra-red light (by a shutter) to prevent additional charge generation thus avoiding image "smear", or alternatively it is possible to avoid the use of the shutter by very fast transfer of the changes rom the horizontal lines into a conventional CCD array (non-detecting) for later slow read-out. In the read-out mode the silicide gates work as junction gates of a junction CCD. The silicide-silicon Schottky Junction behaves as a reverse biased p-n junction and is used in that capacity for charge transfer in the infra-red Schottky Junction CCD. Applying the proper phase voltages tothe IR SJ CCD gates we can transfer the whole infra-red generated image charge to the output stage. In the case of a two dimensional array the signal is transferred from all horizontal line IR SJ CCDs column by column, to either a frame storage CCD array (not shown), or a vertical CCD (which can be either an infra-red Schottky Junction CCD type or a conventional CC) which may then transport them to an output stage.

Referring to Figure 3, the Fully Integrated Schottky Array (FISA) should best be implemented as a frame transfer architecture, since metal-silicide Schottky CCDs in accordance with the present invention can be used for

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both infra-red detection and signal shift registers. An array of IR-sensitive Schottky silicide gates for IR imaging and frame transfer 21 is connected to an array of non-IR-sensitive CCDs for frame storage 22, before line-by-line read-out through a further CCD 23. For achieving detector fill factors close to 100%, the CCDs in the image part must abandon the use of MOS-type gates, and use Schottky gates only. For the infra-red sensitive image area 21, the Schottky gates would be formed by using low Schottky barrier height silicides such as platinum silicide for maximum infra-red response. On the other hand, silicide for the CCDs within the frame storage area 22, and for the read-out CCD 23, would be formed by using metals which have a high Schottky barrier height, for minimal infra-red response and low dark current.

By using Schottky gates for all active components of the detector array device, the FISA is easy to fabricate, leading to high fabrication yields. The lack of gate oxides increases the storage capacity of the Schottky CCDs compared to conventional buried channel CCDs, leads automatically to anti-blooming behaviour, and makes the device more radiation resistant.

Figure 4, A, B and C, in plan view (A) and cross section (Fig. 4B is a cross-section along line B-B of Fig. 4A, and Fig. 4C is a cross-section along line C-C of Fig. 4A) the layout of a detector cell of the proposed FISA device. Starting material for the detector device is n-type silicon 30. Boron is implanted across the CCD matrix. A SiO_2 layer, patterned between the CCD channels, masks against the first boron channel implant, while the silicon substrate 30 within the channel areas is uncovered by this masking oxide. This leads to a light boron dose 31 between the CCD channels and a heavier boron dose within the channel areas 32. The light boron dose area 31 willbe about a half of the concentration of the

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heavy boron dose area 32, for example, although it may vary from this. This distinct implant profile has two purposes: (1) The heavy implant keeps the charges within the CCD channel 32, while the light implant acts as a channel separation 31; (2) Schottky gates 33 formed later on this p-type implant do not need guard rings for each individual CCD gate, since silicide areas may stretch on uninterrupted p-implanted silicon across the whole device. Channel stop diffusions of the opposite polarity than the channel implant, as used in conventional CCDs (and in the CCDs of AU 579027), are not needed in Schottky CCDs because of the inbuilt anti-blooming features of this type of CCD. The light implant used in the present invention is also infra-red sensitive - leading to increased detector fill factor.

The gaps between adjacent Schottky gates 33 have to be made very small, preferably in the sub-micron range, if high transfer efficiency is to be achieved. Schottky gates which lie directly on silicon, can be separated by spacers 34 of grown or deposited silicon-dioxide (SiO_2), patterned by electron-beam exposure, X-ray exposure, deep UV exposure, or other patterning techniques leading to sub-micron wide SiO_2 lines 34 across the CCD matrix perpendicular to the CCD channel direction. Metals having low Schottky barrier heights such as platinum on p-type silicon, form platinum-silicide (PtSi) only on exposed silicon and not on SiO_2, and the PtSi Schottky gates are thus separated by sub-micron SiO_2-spacers 34. Other metals which form high Schottky barrier height silicides, would be suitable for the CCD matrix 22 (Figure 2) as frame storage CCDs or for the read-out CCD 23 (Figure 2).

If the Schottky CCD is supposed to be operated as a two-phase CCD shift register, then the CCD p-type channel implant needs two distinct regions under each Schottky gate for a unique charge transfer direction. This channel

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implant has to be aligned exactly to the sub-micron Schottky gate spacers 34. This second p-type implant leads to three distinguishable p-implanted areas; a light implant 31 between the CCD channels 32, a medium implant 35 for the charge barrier areas within the channel under each gate, and a heavy implant dose for the charge storage areas 36 under each Schottky gate.

In order to lower the resistivity of each silicide gate stretching across the whole device, an aluminium layer 39 is patterned as stripes over each silicide gate 33 on top of a dielectric layer 37, interconnecting the PtSi gates of the same phase through contact holes 38. In addition, the dielectric layer 37 acts, together with the aluminium layer 39 on top of it, as the optical cavity, enhancing the detector quantum efficiency (i.e. it provides an optical cavity and reflective layer, designed to reflect photos of light back towards the section layer). On the opposite, radiation receiving side of the device an anti-reflective coating 40 may be provided.The advantage of having uninterrupted silicide gates 33 lying on uninterrupted p-implanted silicon 31,35,36 across the entire width of the device is that the PtSi Schottky gates do not need guard rings for each individual pixel. Only at the edge of the CCD array a structure is needed to prevent edge leakage current and edge breakdown while the Schottky gates 33 are reverse biased during operation. This leakage current can be reduced by implanting a shallow n-type layer at the end of each Schottky gate at the edge of the array into the p-type channel implant, or by replacing the low Schottky barrier height PtSi at the end of each gate by a metal silicide having a high Schottky barrier height on p-type silicon. The silicide gate edges facing the silicon dioxide spacer 34 do not need guard rings, since the gates are only separated by sub-micron spacers, and therefore

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form overlapping depletion regions when reverse biased. The operation of the image part 21 (Figure 2) of the FISA is divided into two modes: the detection mode and the frame transfer mode. During the detection mode the Schottky gates of one phase (e.g. dia.1) would be reverse biased. The infra-red radiation coming from the substrate direction generates electron-hole pairs in the metal-silicide layer, as described for Figure 1. Electrons which stay in the silicide layer, are absorbed by the applied bias voltage, while positive charges (holes) are ejected into the p-type implanted layer and stored in the "buried" channel potential well. After the detection mode, the phases are alternatingly pulsed, as in conventional buried channel CCDs, thus shifting the potential wells and stored holes along the Schottky CCD channels. This way, the whole frame of an infra-red image is shifted into the storage CCDs 22 (Figure 2). While all charges are then read-out from the storage CCD matrix line-by-line through the read-out CCD 23, the next frame of an infra-red image is integrated in the image part 21.

A generalized process for the fabrication of a Schottky Junction CCD array in accordance with the present invention may include the following items:

1. A first p-type implant step on the n-type silicon substrate with no mask.

2. A second p-type implant to define the CCD channels, using a silicon dioxide or photoresist mask to define the areas of light and heavy concentration doping.

3. A third p-type implant to define the p-type concentration profile within each CCD channel, using masks to form the storage and barrier areas under each Schottky gate. [Note that this is only necessary for two phase CCD operation, as is described herein. It is also possible to have a four phase device, in which case the third p-type implant step is not necessary, although four different phases of electrical potential are]

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4. Silicone dioxide deposition and sub-micron patterning to form sub-micron spacers between Schottky gates. This submission patterning may be carried out using such techniques as electron-beam exposure, X-ray exposure, etc.
5. Deposition of SiO_2 or siO dielectric layer, patterning of contact holes for each Schottky gate.
6. Deposition and patterning of aluminium layer interconnecting all Schottky gates of the same phase, and acting together with the detective layer as "optical cavity".

The present invention cannot only be applied in the area of IR detection arrays, but is also applicable to Schottky Junction CCD arrays in general and also photo-optic detectors outside the IR range.

Note that the array in accordance with the present invention may be mounted in a device having a lens or other means for focussing radiation on the array.

It will be recognised by persons skilled in the art that numerous variations and modifications may be made to the invention as described above without departing from the spirit or scope of the invention as broadly described.

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THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A Schottky Junction CCD array comprising a plurality of Schottky Junction transfer gates on a semiconductor substrate, the array comprising at least two adjacent linear CCDs, each CCD comprising a plurality of adjacent Schottky Junction transfer gates, the adjacent CCDs being separated by a low dose semiconductor impurity implant of the same polarity as a higher dose buried channel implant in the CCD channel.

2. A Schottky Junction CCD array in accordance with claim 1, wherein each Schottky Junction transfer gate comprises a metal silicide layer formed over the semiconductor impurity implant.

3. A Schottky Junction CCD array in accordance with claim 2, wherein the metal silicide layers extend in strips across adjacent CCDs in the array.

4. A Schottky Junction CCD array in accordance with any of claims 1, 2 or 3, wherein adjacent Schottky Junction transfer gates in each CCD are separated from each other by micron or less width gaps.

5. A Schottky Junction CCD array in accordance with claim 4, wherein spacers of silicon dioxide separate adjacent gates within each CCD.

6. A Schottky Junction CCD array in accordance with any preceding claim, wherein each Schottky gate is of low barrier height, such that it is sensitive to infra-red radiation.

7. A Schottky Junction CCD array in accordance with any preceding claim, wherein the array is provided with an anti-reflective coating at least on the surface which is arranged to receive incident radiation.

8. A Schottky Junction CCD array comprising a plurality of Schottky Junction transfer gates on a semiconductor substrate, the array comprising at least two adjacent linear CCDs, each CCD comprising a plurality of adjacent

Schottky Junction transfer gates, each Schottky Junction transfer gate comprising a layer of metal silicide over a semiconductor impurity implant, the metal silicide layers extending in strips across adjacent CCDs in the array.

9. A Schottky Junction CCD array in accordance with claim 8, wherein adjacent CCDs are separated by a low dose semiconductor impurity implant of the same polarity as a higher dose buried channel implant in the CCD channel.

10. A Schottky Junction CCD array in accordance with claims 8 or 9, wherein adjacent Schottky Junction transfer gates in each CCD are separated from each other by micron or less width gaps.

11. A Schottky Junction CCD array in accordance with claim 10, wherein spacers of silicon dioxide separate adjacent gates within each CCD.

12. A Schottky Junction CCD array in accordance with any of claims 8 to 11, wherein each Schottky gate is of low barrier height, such that it is sensitive to infra-red radiation.

13. A Schottky Junction CCD array comprising a plurality of Schottky Junction transfer gates, on a semiconductor substrate, the array comprising at least two adjacent linear CCDs, each CCD comprising a plurality of adjacent Schottky Junction transfer gates, adjacent Schottky Junction transfer gates within the CCD being separated from each other by a gap of a micron or less wide in the direction of charge transfer.

14. A Schottky Junction CCD array in accordance with claim 13, wherein the gap is of sub-micron dimensions.

15. A Schottky Junction CCD array in accordance with claims 13 or 14, wherein adjacent CCDs are separated by a low dose semiconductor impurity implant of the same polarity as a higher dose buried channel implant in the CCD channel.

16. A Schottky Junction CCD array in accordance with

claims 13, 14 or 15, wherein each Schottky Junction transfer gate comprises a metal silicide layer formed over a semiconductor impurity implant.

17. A Schottky Junction CCD array in accordance with claim 16, wherein the metal silicide layers extend in strips across adjacent CCDs in the array.

18. A Schottky Junction CCD array in accordance with any of claims 13 to 17, wherein spacers of silicon dioxide separate adjacent gates within each CCD.

19. A Schottky Junction CCD array in accordance with any of claims 13 to 18, wherein each Schottky gate is of low barrier height, such that it is sensitive to infra-red radiation.

20. A Schottky Junction CCD array in accordance with any of claims 13 to 19, wherein the array is provided with an anti-reflective coating at least on the surface which is arranged to receive incident radiation.

21. A frame transfer Schottky Junction CCD array comprising an upper array and a lower array, the upper array comprising at least two adjacent linear CCDs, each CCD comprising a plurality of adjacent Schottky Junction transfer gates on a semiconductor substrate, said transfer gates being radiation sensitive and being arranged to operate in a first mode as radiation detection elements and in a second mode as gates of a CCD shift register, and the lower frame comprising at least two adjacent linear CCDs, each comprising a plurality of adjacent Schottky Junction transfer gates, each upper CCD being arranged to transfer charge into a respective lower frame CCD.

22. A frame transfer Schottky Junction CCD array in accordance with claim 21, wherein adjacent CCDs in at least the upper array are separated by a low dose semiconductor impurity implant of the same polarity as a higher dose buried channel implant in each CCD channel.

23. A frame transfer Schottky Junction CCD array in

accordance with claims 21 or 22, wherein each Schottky Junction transfer gate in at least the upper array comprises a metal silicide layer formed over the semiconductor impurity implant.

24. A Schottky CCD array in accordance with claim 23 wherein the metal silicide layers of the gates in at least the upper array, extend in strips across adjacent CCDs in the array.

25. A frame transfer Schottky Junction CCD array in accordance with any of claims 21 to 24, wherein adjacent Schottky Junction transfer gates in each CCD in at least the upper array are separated from each other by micron or less width gaps.

26. A frame transfer device in accordance with claim 25, wherein spacers of silicon dioxide separate adjacent gates within each CCD.

27. A frame transfer Schottky Junction CCD array in accordance with any of claims 21 to 26, wherein each Schottky gate of at least the upper array is of low barrier height, such that it is sensitive to infra-red radiation.

28. A frame transfer Schottky Junction CCD array in accordance with any of claims 21 to 27, wherein at least the upper array is provided with an anti-reflective coating at least on the surface which is arranged to receive incident radiation.

29. A Schottky Junction charge coupled device infra-red imaging array having substantially contiguous infra-red sensitive elements with a fill factor substantially greater than fifty percent, said imaging array comprising:

a plurality of substantially contiguous conductive transfer electrodes disposed along a semiconductor substrate above a buried implant channel and providing means for serially shifting charge packets within the buried channel of said substrate when a sequence of

control voltages is applied thereto,

each of said substantially contiguous transfer elements forming a rectifying metal to semiconductor contact known as a Schottky contact and having a barrier height sufficiently low to cause the Schottky contact to respond to infra-red radiation of wavelength substantially greater than the band to band absorption cutoff wavelength of the semiconductor,

said Schottky contact acting in a first mode as an infra-red detector element by photoemission of charge carriers from the metallic region of said Schottky contact to said buried channel of said semiconductor substrate and, in a second mode, to control movement of charge packets within said buried channel, operating in said first or second mode being determined by voltage sequences applied to said transfer electrodes,

a dielectric passivating layer located over the transfer electrodes, and

a mirror located above the dielectric layer,

the transfer electrodes being sufficiently thin to enable transmission of infra-red light and the dielectric layer forming an optical cavity on top of the transfer electrode,

the buried implant channel comprising a central region of relatively high concentration dopant extending along the channel and bounded by regions of relatively low concentration dopant of the same polarity at its edges.

30. A Schottky Junction charge coupled device infra-red imaging array having substantially contiguous infra-red sensitive elements with a fill factor substantially greater than fifty percent, said imaging array comprising:

a plurality of substantially contiguous conductive transfer electrodes disposed along a semiconductor substrate above a buried implant channel and providing means for serially shifting charge packets within the

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buried channel of said substrates when a sequence of control voltages is applied thereto,

each of said substantially contiguous transfer electrodes forming a rectifying metal to semiconductor contact known as a Schottky contact and having a barrier height sufficiently low to cause the Schottky contact to respond to infra-red radiation of wavelength substantially greater than the band to band absorption cutoff wavelength of the semiconductor,

said Schottky contact acting in a first mode as an infra-red detector element by photoemission of charge carriers from the metallic region of said Schottky contact to said buried channel of said semiconductor substrate and, in a second mode, to control movement of charge packets within said buried channel, operating in said first or second mode being determined by voltage sequences applied to said transfer electrodes,

the buried implant channel comprising a central region of relatively high concentration dopant extending along the channel and bounded by regions of relatively low concentration dopant of the same polarity at its edges.

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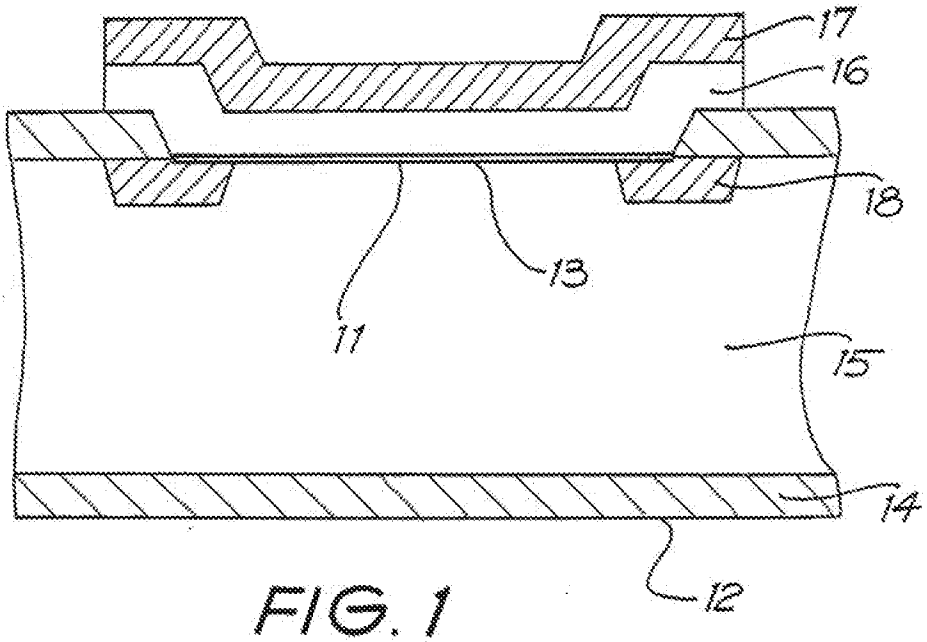


FIG. 1

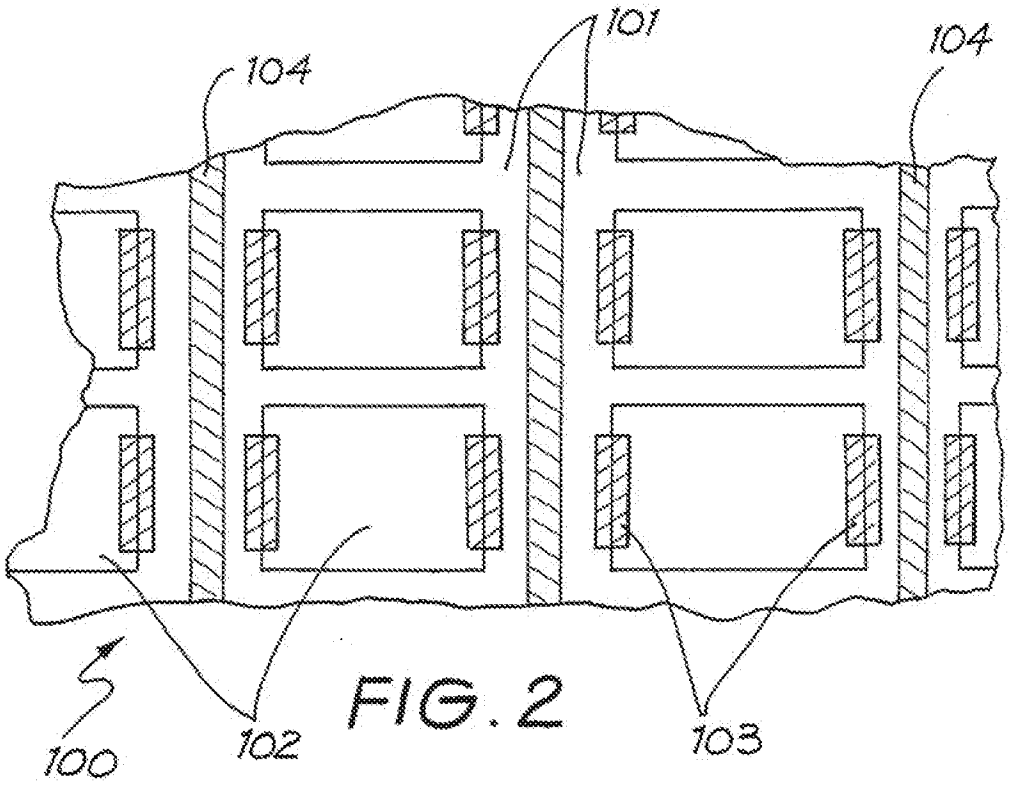


FIG. 2

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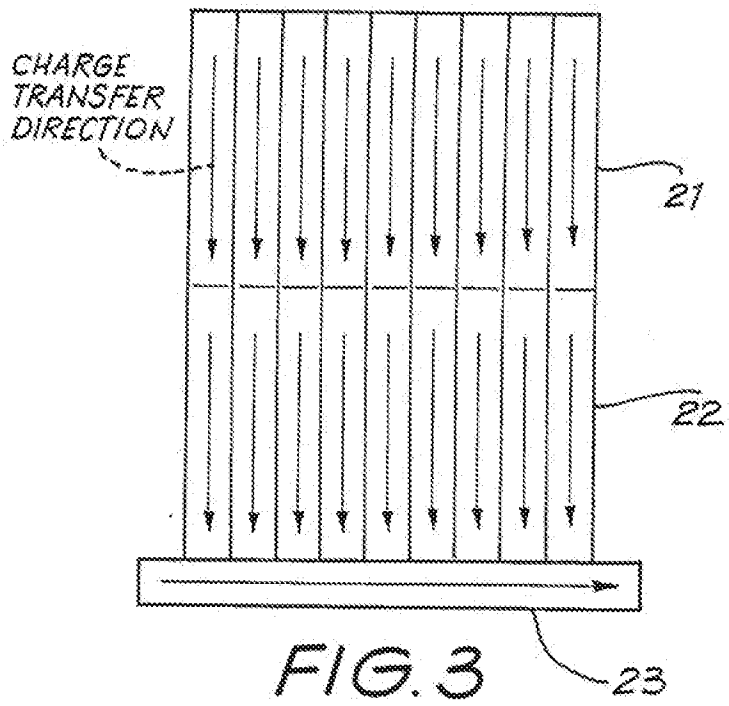


FIG. 3

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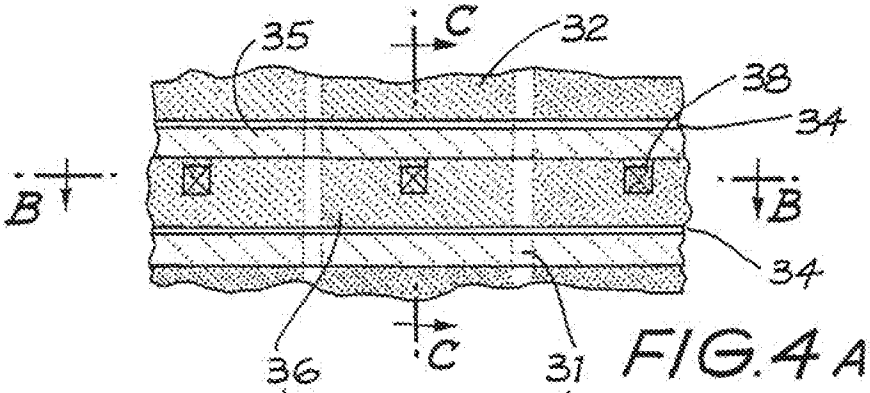


FIG. 4A

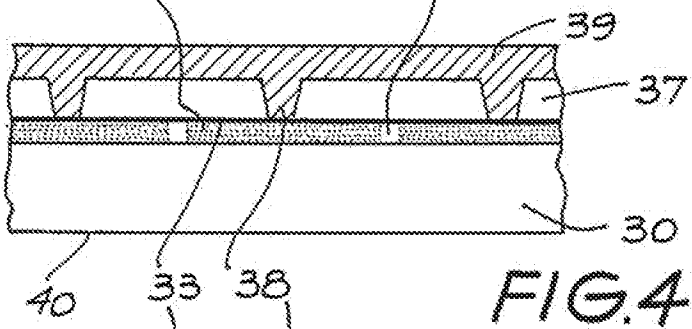


FIG. 4B

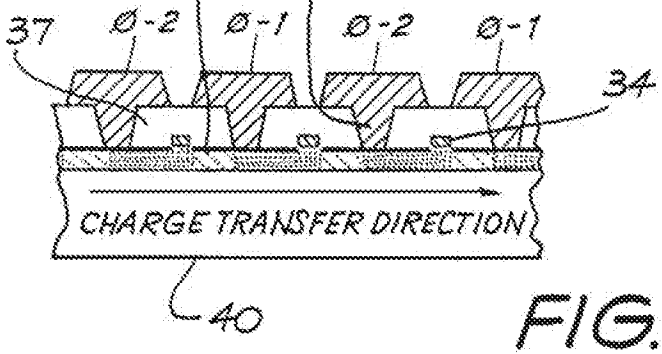


FIG. 4C

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INTERNATIONAL SEARCH REPORT

International Application No. PCT/AU 91/00078

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) 6

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl.[5] H01L 27/148, 27/085

II. FIELDS SEARCHED

Minimum Documentation Searched 7

Classification System	Classification Symbols
IPC	H01L 27/148, 27/085, 27/14, 27/08

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched 8

AU : H01L 27/148, 27/085, 27/14, 27/08

III. DOCUMENTS CONSIDERED TO BE RELEVANT 9

Category*	Citation of Document, [11] with indication, where appropriate, of the relevant passages 12	Relevant to Claim No 13
X,Y	US,A, 4675714 (HIGGINS) 23 June 1987 (23.06.87) (Column 3 line 33)	(13,14,16-20)
X,Y	US,A, 4264915 (BIERHENKE et al) 28 April 1981 (28.04.81) (Column 6 lines 37,38)	(13,14,16-20)
X,Y	AU,B, 62199/86 (579027) (UNISEARCH LTD) 5 March 1987 (05.03.87) (page 9 lines 2-4, Fig 4b,5b, page 10 lines 6-9)	(8,10-14,16-21,23, 26-28)
X,Y	CARLO H. SEQUIN and MICHAEL F. TOMPSETT "Charge & Transfer Devices", published 1975 by Academic Press, Inc. (pages 152-157, Fig 5.6(c), Fig 5.20, pages 197-198)	(8,10-14,16-21, 23-28)
A	US,A, 4779124 (HYNECEK) 18 October 1988 (18.10.88)	
A	US,A, 4273596 (GUTIERREZ et al) 16 June 1981 (16.06.81)	

* Special categories of cited documents: 10

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
13 June 1991 (13.06.91)	20 JUNE 1991
International Searching Authority	**Signature of Authorized Officer**
Australian Patent Office	M.E. DIXON

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FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

V. [ ] OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE 1

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1.[ ] Claim numbers ..., because they relate to subject matter not required to be searched by this Authority, namely:

2.[ ] Claim numbers , because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3.[ ] Claim numbers ..., because they are dependent claims and are not drafted in accordance with the second and third sentences of PCT Rule 6.4 (a):

VI. [X] OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING 2

This International Searching Authority found multiple inventions in this international application as follows:

SEE ATTACHED SHEET

1.[ ] As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2.[ ] As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3.[ ] No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. [X] As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

[ ] The additional search fees were accompanied by applicant's protest.

[ ] No protest accompanied the payment of additional search fees.

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FURTHER INFORMATION CONTINUED FROM THE THIRD SHEET

VI.[X] OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING:

All claims are to Schottky Junction CCDs. This alone is not a new invention.

(i) Claims 1-7,29 and 30 relate to the doping of impurity implants in the CCD.

(ii) Claims 8-12 specify metal silicide layers in strips across the CCD.

(iii) Claims 13-20 specify sub-micron separation of transfer gates in the CCD.

(iv) Claims 21-28 are to a frame transfer CCD.

Each of (i),(ii),(iii) and (iv) relate to a different improvement in a Schottky Junction CCD and are therefore different inventions.

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ANNEX TO THE INTERNATIONAL SEARCH REPORT ON
INTERNATIONAL APPLICATION NO. PCT/AU 91/00078

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report	Patent Family Members		
US 4675714			
US 4264915	DE 2743245 JP 54057869	FR 2404303	GB 2005074
AU 62199/86	US 5001530 JP 3121072	CA 2025077	EP 419282
US 4779124	EP 167756	JP 61044465	
US 4273596	US 4228365		

END OF ANNEX

PUB-NO: WO009114284A1
DOCUMENT-IDENTIFIER: WO 9114284 A1
TITLE: SCHOTTKY JUNCTION CHARGE COUPLED DEVICE
PUBN-DATE: September 19, 1991

INVENTOR-INFORMATION:

NAME	COUNTRY
THEDEN, ULRICH	AU

ASSIGNEE-INFORMATION:

NAME	COUNTRY
UNISEARCH LTD	AU

APPL-NO: AU09100078
APPL-DATE: March 6, 1991

PRIORITY-DATA: AUPJ896490A (March 6, 1990)

INT-CL (IPC): H01L027/085 , H01L027/148

EUR-CL (EPC): H01L027/148

US-CL-CURRENT: 257/216 , 257/280 , 257/E27.16

ABSTRACT:

The present invention provides a Schottky Junction CCD array comprising a plurality of adjacent Schottky Junction CCDs which are infra-red sensitive, and which are separated by a low dose impurity implant (31) of the same polarity as a higher dose implant (35, 36) within the CCD channel (32). The individual gates are comprised of a metal silicide layer on the semiconductor substrate. The silicide layer stretches all the way across the array. Also, these silicide strips are separated by gaps (34) of sub-micron dimensions. This construction leads to substantially a 100 % fill factor for the array. Nearly all of the array will be IR sensitive.

(12) 特許協力条約に基づいて公開された国際出願

(19) 世界知的所有権機関
国際事務局

(43) 国際公開日
2008 年8 月21 日 (21.08.2008)

PCT

(10) 国際公開番号
WO 2008/099524 A1

(51) 国際特許分類:
H01L 31/04 (2006.01)

(21) 国際出願番号: PCT/JP2007/065386

(22) 国際出願日: 2007 年8 月6 日 (06.08.2007)

(25) 国際出願の言語: 日本語

(26) 国際公開の言語: 日本語

(30) 優先権データ:
特願2007-036432 2007 年2 月16 日 (16.02.2007) JP

(71) 出願人 (米国を除く全ての指定国について): 三菱重工業株式会社 (MITSUBISHI HEAVY INDUSTRIES, LTD.) [JP/JP]; 〒1088215 東京都港区港南二丁目１６番５号 Tokyo (JP).

(72) 発明者; および

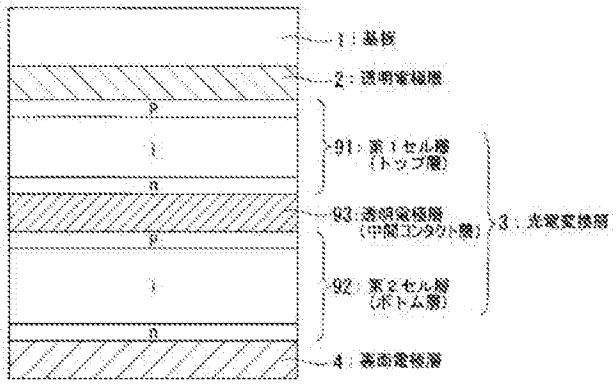
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(74) 代理人: 藤田 考晴, 外(FUJITA, Takaharu et al.); 〒2200012 神奈川県横浜市西区みなとみらい３－３－１ 三菱重工横浜ビル２４Ｆ Kanagawa (JP).

[続葉有]

(54) Title: PHOTOELECTRIC CONVERTER AND METHOD FOR FABRICATING THE SAME

(54) 発明の名称: 光電変換装置及びその製造方法



90 PHOTOELECTRIC CONVERTER
1 SUBSTRATE
2 TRANSPARENT ELECTRODE LAYER
3 PHOTOELECTRIC CONVERSION LAYER
91 FIRST CELL LAYER (TOP LAYER)
92 SECOND CELL LAYER (BOTTOM LAYER)
93 TRANSPARENT ELECTRODE LAYER (INTERMEDIATE CONTACT LAYER)
4 BACKSIDE ELECTRODE LAYER

(57) **Abstract:** A photoelectric converter satisfying both high photoelectric conversion efficiency and high productivity, and its fabrication method. The photoelectric converter (90) has a substrate with a transparent electrode where a transparent electrode layer (2) is provided on a transparent insulating substrate (1), and at least a photoelectric conversion layer (92) principally comprising a crystalline silicon based semiconductor and a backside electrode layer (4) that are formed sequentially on the transparent electrode layer (2) side of the substrate with a transparent electrode. The transparent electrode layer (2) on the substrate with a transparent electrode has a surface shape where large and small protrusions and recesses coexist and spectral haze rate is 20% or above at the wavelength of 550-800 nm. The photoelectric conversion layer principally comprising the crystalline silicon based semiconductor has a film thickness of 1.2-2 μm, and a Raman ratio of 3.0-8.0.

(57) 要約: 高い光電変換効率と高い生産性を両立した光電変換装置及びその製造方法を提供することを目的とする。透明絶縁性の基板１上に透明電極層２を設けてなる透明電極付き基板と、該透明電極付き基板の透明電極層２側に順次形成された、結晶質シリコン系半導体を主として有する光電変換層９２ならびに裏面電極層４とを少なくとも有してなる光電変換装置であって、前記透明電極付き基板の透明電極層２表面が、大小の凹凸が混在した形状であり、かつ分光ヘイズ率が５５０ｎｍ以上８００ｎｍ以下の波長で２０％以上であり、前記結晶質シリコン系半導体を主として有する光電変換層の膜厚が１．２μｍ以上２μｍ以下、かつラマン比が３．０以上８．０以下である光電変換装置９０を提供する。

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(81) 指定国 (表示のない限り、全ての種類の国内保護が可能): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) 指定国 (表示のない限り、全ての種類の広域保護が可能): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), ユーラシア (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), ヨーロッパ (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

添付公開書類:
— 国際調査報告書

明 細 書

光電変換装置及びその製造方法

技術分野

[0001] 本発明は、光電変換装置及びその製造方法に関し、特に発電層としてシリコンを用いる薄膜シリコン積層型太陽電池に関するものである。

背景技術

[0002] 従来より、太陽電池等の光電変換装置として、シリコン系薄膜光電変換装置が知られている。この光電変換装置は、一般に、基板上に、第1透明電極、シリコン系半導体層(光電変換層)、第2透明電極及び裏面電極膜を順次積層したものである。半導体層はp型、i型及びn型の半導体材料によって形成されるpin接合を有している。光電変換装置が太陽電池である場合においてはこのpin接合がエネルギー変換部となって、太陽光の光エネルギーを電気エネルギーに変換する。このように、光電変換層が1層の光電変換装置の構造は、シングル構造と呼ばれている。

[0003] また、光電変換装置の光電変換効率を高めるために、バンドギャップの異なる半導体からなる光電変換層を複数重ねて用いる方法がある。このように複数の光電変換層を重ねて用いた光電変換装置は多接合型光電変換装置と呼ばれ、吸収波長帯域が異なる光電変換層を2段重ねた構造はタンデム構造、3段重ねた構造はトリプル構造と呼ばれている。タンデム構造の光電変換装置を例にとると、太陽光入射側の光電変換層(以下、「トップセル」ともいう)としては短波長の光を吸収するアモルファス(非晶質)シリコンが用いられ、また、トップセルで吸収されなかった光を吸収するために、太陽光入射側とは反対側の光電変換層(以下、「ボトムセル」ともいう))としては長波長の光を吸収する微結晶シリコン等の結晶質シリコン系半導体を用いることができる。

[0004] このような光電変換装置を用いた太陽電池には、次のような技術課題(1)が存在する。

(1)高効率化:太陽光をエネルギー変換部にいかに効率よく取り込み、電気エネルギーに変換する効率をいかに高めるか。

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[0005] 上記技術課題(1)の高効率化としては、12%以上の発電効率を得ることが目安となるが、従来、例えばタンデム型太陽電池において12%以上の発電効率を得るためには、2μm以上のボトムセル膜厚が必要であった。更に発電効率を上げるためには、ボトムセルの厚膜化(3μm以上)が検討されている。

[0006] また、上記技術課題(1)の高効率化を実現するために、第1透明電極を含めた基板のヘイズ率を高めることが検討されている。従来は、第1透明電極を含めた基板のヘイズ率を大きくすると、入射光の光散乱による光閉じ込め効果が向上して発電電流は増大するが、第1透明電極を含めた基板表面の大きな凹凸の影響などで開放電圧と形状因子が大幅に低下するので、電池としては好ましくないと、一般的に考えられていた。これを解決するために、前記基板及び第1透明電極として、ガラス基板上に、不連続な複数の山部によるマクロな凹凸(テクスチャ)と、この山部間をうめる複数の平坦部とを有しており、該山部及び該平坦部の外表面が、ミクロの多数の凹凸(テクスチャ)を有する構造(ダブルテクスチャ構造)となっている透明導電性酸化物付き基体を用いることが提案されている(特許文献1、特許文献2参照)。特許文献1及び2の透明導電性酸化物付き基体は、太陽光の全波長域で良好な光散乱性能有するものであり、特許文献2には、これを用いて作製されたアモルファスシリコン太陽電池が、その実施例において、開放電圧と形状因子をほぼ維持しつつ光電変換効率が高められることが示されている。

特許文献1:国際公開第03/036657A1号公報

特許文献2:特開2005-347490号公報

発明の開示

[0007] 光電変換装置を用いた太陽電池を実用化するためには、前記技術課題(1)に加え、下記技術課題(2)も存在する。

(2)生産性向上:生産性のボトルネックとなる結晶質シリコン系光電変換層中のi層をいかに薄膜化できるか。

[0008] 太陽電池の製造時間は、ボトムセル等を構成する結晶質シリコン系光電変換層中のi層の製膜時間に律速するため、上記技術課題(2)の生産性の点からは、結晶質シリコン系光電変換層中のi層の膜厚の薄膜化が極めて有効である。ところが、例え

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ばタンデム型太陽電池においてボトムセルの膜厚を2μmより薄膜化すると、発電電流の低下が著しく、よって発電効率の低下が著しくなる。このため、太陽電池の製造時間が長時間かかっても、2μm以上のボトムセル膜厚が適用されている。

このように、前記技術課題(1)と(2)とは、互いにトレードオフの関係にあった。

[0009] 前記特許文献1に示された技術は、光の吸収波長特性が異なる結晶質シリコン系半導体からなる光電変換層の発電効率を特に考慮したものではなく、また、太陽電池の生産性向上について検討されたものでもなかった。従って、結晶質シリコン系半導体からなる光電変換層を有する太陽電池については、入射光の吸収波長域が特に長波長側で異なるため、透明電極の凹凸による光閉じ込め形状は違うものが必要となるが、結晶質シリコン系半導体の膜厚を薄膜化することを考慮して凹凸形状を適正化することが未確立であり、発電効率の高効率化(技術課題(1)の解決)と太陽電池の生産性向上(技術課題(2)の解決)を両立できる技術が依然として望まれていた。

[0010] また、特許文献1のように大きな凹凸と小さな凹凸の混在する透明導電性酸化膜付き基板を用いて太陽電池を作製すると、大きな凹凸構造のみで構成してヘイズ率を高めた透明導電性酸化物付き基板を用いる場合よりも開放電圧と形状因子の低下を小さくすることはできるものの、やはり開放電圧と形状因子の低下が認められる。

[0011] 本発明は、このような事情に鑑みてなされたものであって、高い光電変換効率と高い生産性を両立した光電変換装置及びその製造方法を提供することを目的とする。

[0012] また、本発明は、大小の凹凸が混在した形状によりヘイズ率を高めた透明電極付き基板を用いた光電変換装置において、開放電圧と形状因子の低下を抑制しつつ高い光電変換効率を実現すること、およびこのような光電変換装置の製造方法を提供することを目的とする。

[0013] 上記課題を解決するために、本発明の第1の態様にかかる光電変換装置は、以下の手段を採用する。

すなわち、本発明の第1の態様にかかる光電変換装置は、透明絶縁性の基板上に透明電極層を設けてなる透明電極付き基板と、該透明電極付き基板の透明電極層側に順次形成された、結晶質シリコン系半導体を主として有する光電変換層ならび

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に裏面電極層とを少なくとも有してなる光電変換装置であって、前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上であり、前記光電変換層の膜厚が1.2μm以上2μm以下であり、かつラマン比が3.0以上8.0以下である光電変換装置である。

[0014] 前記第1の態様にかかる光電変換装置において、結晶質シリコン系光電変換層のラマン比を3.0以上8.0以下とすることにより、結晶の粒界が適度に非晶質シリコンで充填された光電変換装置を得ることができる。これにより、結晶粒界の電流リークを抑制できるので、開放電圧(Voc)及び形状因子(FF)の低下が抑制された光電変換装置を得ることができる。前記透明電極付き基板を用いた場合には、基板の凹凸に起因して欠陥の多い結晶粒界が生成しやすいため、結晶粒界の非晶質シリコンによる充填が特に有効である。

[0015] また、膜厚が1.2μm以上2μm以下の前記結晶質シリコン系半導体を主として有する光電変換層を形成することにより、結晶質シリコン系半導体を主として有する光電変換層のi層の膜厚を薄膜としても、高い発電電流を生じる光電変換装置を製造することができ、更に欠陥数を膜厚分低下でき、また、膜厚方向の電位勾配が大きいので発生電荷が欠陥にトラップされにくくなるので、開放電圧(Voc)及び形状因子(FF)の低下が抑制された光電変換装置を製造することができる。従って、薄膜化と高効率化を同時に達成した光電変換装置を製造でき、さらに、結晶質シリコン系i層を薄膜化することで、この製膜によって律速される光電変換装置の製造時間を短縮することができるので、光電変換装置の生産性が向上する。

[0016] 一般にヘイズ率といえば、ヘイズメータで計測される、波長が約550nmの光のヘイズ率をさす。波長550nmのヘイズ率が高いと波長550nm程度の光はよく散乱されるが、長波長光は該波長のヘイズ率が高ければよく散乱されるが、該波長のヘイズ率が低ければ散乱されにくい。従来の一層の凹凸(テクスチャ)構造の場合、波長550nmのヘイズ率が30%であっても、波長800nmの分光ヘイズ率は5%以下となり、結晶質シリコン系の光電変換層で光を閉じ込めたい700～900nmの波長域の光の散乱増強による光閉じ込めは不十分であった。また、350nm以下の波長域では、前記透明電極基板の透過率が小さくなるためヘイズ率を正しく計測することができない

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。したがって、550nm以上800nm以下の波長のヘイズ率を、波長を特定した光を用いて計測する分光ヘイズ率で定義し、分光ヘイズ率20%以上、より好ましくは30%以上とすることにより、結晶質シリコン系の光電変換層で光閉じ込めの影響を強く受ける700～900nmの波長域の光の散乱、光閉じ込めを増強でき、発電電流を増大することができる。

[0017] 前記第1の態様にかかる光電変換装置において、前記透明電極付き基板と前記結晶質シリコン系半導体を主として有する光電変換層との間に、非晶質シリコン系半導体を主として有する光電変換層を形成してもよい。

[0018] このような構成とすることにより、非晶質シリコン系半導体を主として有する光電変換層では太陽光の短波長側成分の光電変換が行われ、結晶質シリコン系半導体を主として有する光電変換層では太陽光の長波長側成分の光電変換が行なわれるので、より光電変換効率の高い光電変換装置とすることができる。

[0019] 前記第1の態様にかかる光電変換装置において、前記非晶質シリコン系半導体を主として有する光電変換層と前記結晶質シリコン系半導体を主として有する光電変換層との間に、中間コンタクト層を形成してもよい。

[0020] 中間コンタクト層を構成とすることにより、非晶質シリコン系半導体を主として有する光電変換層を薄膜化し、劣化率を改善できる一方で、結晶質シリコン系半導体を主として有する光電変換層への入射光が低下し、電流値が低下する。したがって、非晶質シリコン系半導体を主とする光電変換層の劣化率改善と、結晶質シリコン系半導体を主とする光電変換層の発電電流の低下との相対関係から、中間コンタクト層の膜厚は、90nm以下とすることが好ましく、さらには50nm以上70nm以下とすることがより好ましい。また、中間コンタクト層としては、ZnO系膜（例えば、GZO膜）で形成され、ZnO系単膜での光吸収率がλ＝450nm以上1000nm以下の範囲で1%未満であることがより好ましい。中間コンタクト層の透明性が損なわれると、結晶質シリコン系半導体を主とする光電変換層へ入射する光が低下し、発電電流が低下するため、波長が450nm以上1000nm以下の波長領域に対しては、ほぼ透明であることが好ましい。

[0021] 前記第1の態様にかかる光電変換装置において、前記透明電極付き基板の透明

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電極層表面が、複数の山部と複数の平坦部とで構成され、該山部及び該平坦部の表面がミクロの多数の凸部を連続して有してなり、前記山部の前記基板面垂直方向における高さが0．4μm以上0．7μmであり、基板面10μm角における前記山部の数が15以上50以下であり、前記ミクロの多数の凸部の底面径が0.1μm以上0.3μm以下であり、高さ／底面径の比が0.7以上1.2以下であるものが好ましい。

[0022] 前記第1の態様にかかる光電変換装置は、前記特性を有する透明電極付き基板を適用することで、結晶質シリコン系半導体を主として有する光電変換層（例えば、タンデム型太陽電池のボトムセル）のi層の膜厚を例えば1．5μmの薄膜としても、高い発電電流を生じる。更に結晶質シリコン系半導体を主として有する光電変換層のi層を薄膜化することにより、開放電圧（Voc）及び形状因子（FF）の低下も抑制できる。すなわち、結晶質シリコン系半導体を主として有する光電変換層を薄膜とすることにより、欠陥数を膜厚分低下でき、また、膜厚方向の電位勾配が大きいので発生電荷が欠陥にトラップされにくくなる。従って、光電変換装置の薄膜化と高効率化を同時に達成できる。さらに、結晶質シリコン系光電変換層中のi層を薄膜化できることにより、この層の製膜時間によって律速される光電変換装置の製造時間を短縮することができるので、前記第1の態様にかかる光電変換装置は、生産性が向上したものとなる。

[0023] 従来の技術において開放電圧と形状因子が低下した原因の1つとして、透明電極の谷の部分から光電変換層の膜厚方向に膜成長相間の不連続な境界（その境界を「異相」と呼ぶことにする）が生じ、キャリアの再結合中心となるためと推定される。この異相は、下地の谷々の面からシリコン膜が製膜・成長する際に、その成長面が衝突し、衝突面が格子の欠陥或いは微細な隙間となったものと推定され、キャリアの再結合による損失の原因となる。尚、この光電変換層の膜厚方向の異相は、光電変換層の断面方向の透過顕微鏡分析によって、検出することができる。倍率8万倍以上で光電変換層を長さ100μmの範囲で観察し、亀裂が認められたとき異相がある、貫通する異相が1本でも認められたとき貫通する異相があると判断する。

[0024] この異相の発生自体を抑制するには、透明導電性酸化物基板の凹凸を単純に大型化するのではなく、大きな凹凸と小さな凹凸が混在することが有効である。しかしな

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がら、前記透明電極を用いた場合においても、例えば製膜速度が1nm／sec以上の高速で製膜すると完全に異相の発生を抑制することは難しく、異相発生の抑制には光電変換層を形成する製膜条件選定における制限がある。このため、本発明者らは、特に高速で製膜する場合において異相が発生しても光電変換層を貫通する異相を遮断する知見を得るに至った。

[0025] 従って、本発明者らは、この異相を抑制すること、または完全に抑制はできなくても光電変換層を貫通する異相を遮断できれば、開放電圧低下、形状因子低下を抑制できるという知見を得た。

[0026] この知見から、上記課題を解決するために、本発明の第2の態様にかかる光電変換装置及び第3の態様にかかる光電変換装置の製造方法は、以下の手段を採用する。

すなわち、本発明の第2の態様にかかる光電変換装置は、透明絶縁性の基板上に透明電極層を設けてなる透明電極付き基板と、該透明電極付き基板の透明電極層側に順次形成された、非晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも有し、前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上、特に好ましくは30%以上であり、前記非晶質シリコン系半導体を主として有する光電変換層中に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相（膜成長相間の不連続な境界）を遮断する層（異相遮断層と呼ぶこととする）を設けた光電変換装置、もしくは前記基板と前記非晶質シリコン系半導体を主として有する光電変換層の間に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相の形成を防止する異相防止層を設けた光電変換装置である。

[0027] 第2の態様にかかる光電変換装置によれば、非晶質シリコン系半導体を主として有する光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相を遮断または防止できるので、このような異相による電流リークを抑えることができ、開放電圧低下、形状因子低下が抑制される。

[0028] また、本発明の第3の態様にかかる光電変換装置の製造方法は、透明絶縁性の基

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板上に透明電極層を形成して透明電極付き基板を作製し、該透明電極付き基板の透明電極層側に非晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも順次形成する光電変換装置の製造方法であって、前記透明電極付き基板の透明電極層表面が多数の凸部を連続して有してなり、前記非晶質シリコン系半導体を主として有する光電変換層中に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相を遮断する異相遮断層を形成するか、もしくは前記透明電極層の形成と前記非晶質シリコン系半導体を主として有する光電変換層形成の間に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相の形成を防止する異相防止層を形成する、光電変換装置の製造方法である。

[0029] 第3の態様にかかる光電変換装置の製造方法によれば、非晶質シリコン系半導体を主として有する光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相が遮断または防止されるので、このような異相による電流リークが抑えられ、開放電圧低下、形状因子低下が抑制された光電変換装置を製造することができる。

[0030] 前記第2の態様にかかる光電変換装置及び第3の態様にかかる光電変換装置の製造方法において、前記非晶質シリコン系半導体を主として有する光電変換層をp層、i層、n層を順次形成してなる層とし、前記異相遮断層を前記i層の一部分において、p層、n層、あるいはi層の他の部分より低速で製膜された層とすることができる。低速で製膜することにより、製膜面表面での製膜粒子の拡散・移動時間が増大し、より安定なサイトに堆積して低欠陥の層、即ち異相が少ない層を形成することができる。また、低速で製膜された層はi層の一部分と薄いため、低速で製膜する製膜時間にかかる処理時間は、全体の生産時間に与える影響としては少なくなり、生産性を維持したまま異相が少ない層を形成することができる。

[0031] あるいは、前記非晶質シリコン系半導体を主として有する光電変換層をp層、i層、n層を順次形成してなる層とし、前記n層の一部或いは全体を非晶質の層として、前記n層が前記異相遮断層の機能を有することができる。なお、非晶質とは、ラマン分光分析で分析したとき、Si結晶のピークが全く検出されないものであり、製膜条件では、水素ガス／シランガス希釈率を低下する方向、又はRFパワーを低下する方向で得る

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ことができる。積層膜で再表面のみ非晶質膜にする場合は、ラマン分光分析で下地のSi結晶質膜のピークが検出されることがあり、ガラス基板又は透明電極つきガラス基板上に、単一条件の膜のみを形成してラマン分光分析を実施してSi結晶ピークの有無を判断することとする。非晶質の膜は、欠陥が水素で終端されるので、結晶質と比較して欠陥が連続しにくいために異相となりにくく、異相を遮断する機能を有するものである。

あるいは、前記非晶質シリコン系半導体を主として有する光電変換層をp層、i層、n層を順次形成してなる層とし、前記n層の少なくともその一部を200Pa以上の圧力下で製膜した層とすることにより、前記n層が異相遮断層の機能を有することができる。高圧で製膜すると、製膜される原料ガスの気相中での衝突拡散が促進され、下地の凹部にも原料ガスが到達しやすいために、凹部にも均一に製膜されるので、欠陥上にも均一に良好な膜が形成される、すなわち異相を抑制できると考えられる。

あるいは、前記異相防止層を、前記凸部を円滑化した前記透明電極層とすることができる。前記凸部の円滑化とは、凸部が連続して形成されることにより凸部の境界に生成する谷部について、通常は平面どおしの組合せのため谷の底は明瞭な線状であるが、その線がないように底面を円滑化したもの、例えば、スプーンカットのような形状を有することである。

[0032] 前記異相防止層を、前記透明電極層表面にイオン処理を施して形成してもよい。イオン処理とは、例えば真空中でのアルゴンイオン照射によるイオンエッチングであり、透明電極の表面形状を原子レベルのエッチング、再付着により制御できる。イオンエッチングのイオン照射角度とイオンエネルギーを調整することで、透明電極の凹凸の特に斜面部の原子をエッチング除去し、谷部の底に再付着させることができ、結果として鋭利な谷形状を円滑化することができる。

[0033] 前記第2の態様にかかる光電変換装置及び第3の態様にかかる光電変換装置の製造方法において、前記透明電極付き基板は、550nm以上800nm以下の波長における分光ヘイズ率が20%以上であるものが好ましい。前記分光ヘイズ率が30%以上であるものが特に好ましい。

上述のとおり、従来の凹凸(テクスチャ)構造の場合、波長550nmの分光ヘイズ率

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が30％であっても、波長800nmの分光ヘイズ率は5％以下となり、結晶質シリコン系半導体の光電変換層で光を閉じ込めたい700～900nmの波長域の光の散乱増強による光閉じ込めは不十分であった。そこで、前記第2の態様にかかる光電変換装置及び第3の態様にかかる光電変換装置の製造方法においては、凹凸を大型化して、長波長光に対しても高ヘイズとなるようにする。また、350nm以下の波長域では、前記透明電極の透過率が小さくなるためヘイズメータにより分光ヘイズ率を計測することができない。したがって、550nm以上800nm以下の波長の分光ヘイズ率を20％以上、好ましくは30％以上とすることにより、結晶質シリコン系半導体の光電変換層で光閉じ込めの影響を強く受ける700～900nmの波長域の光の散乱、光閉じ込め効果を増強でき、発電電流を増大することができる。

[0034] 前記第2の態様にかかる光電変換装置及び第3の態様にかかる光電変換装置の製造方法において、前記非晶質シリコン系半導体を主として有する光電変換層と前記裏面電極の間に、結晶質シリコン系半導体を主として有する光電変換層を形成してもよい。

[0035] このような構成とすることにより、非晶質シリコン系半導体を主として有する光電変換層では太陽光の短波長側成分の光電変換が行われ、結晶質シリコン系半導体を主として有する光電変換層では太陽光の長波長側成分の光電変換が行なわれるので、より光電変換効率の高い光電変換装置とすることができる。

[0036] また、結晶質シリコン系半導体を主として有する光電変換層は結晶質シリコン系半導体に限らず、結晶質もしくは非晶質シリコン系半導体、結晶質もしくは非晶質シリコンゲルマニウム系半導体を主として有しても同等の効果が得られる。

[0037] また、結晶質シリコン系半導体を主として有する光電変換層とさらに第3の光電変換層を積層して3層構造以上の光電変換装置としても良い。この場合、結晶質シリコン系半導体を主として有する光電変換層及び第3の光電変換層は、結晶質もしくは非晶質シリコン系半導体、結晶質もしくは非晶質シリコンゲルマニウム系半導体を主として有する光電変換層とすることともでき、非晶質シリコン系半導体を主として有する光電変換層、結晶質シリコン系半導体を主として有する光電変換層光電変換層、第3の光電変換層の順に長波長側成分へと吸収が増大するように、各光電変換層の

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材料や膜質、膜厚を設定すれば良い。

[0038] 本発明によれば、高い光電変換効率と高い生産性を両立した光電変換装置及びその製造方法を提供することができる。本発明の光電変換装置は、太陽電池として好適に利用することができる。

[0039] また、本発明によれば、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上、特に好ましくは30%以上である透明電極付き基板を用いた光電変換装置において、開放電圧と形状因子の低下を抑制しつつ高い光電変換効率を実現することができる。さらに、このように優れた光電変換装置の製造方法を提供することができる。本発明の光電変換装置は、太陽電池として好適に利用することができる。

[0040] また、光電変換層を薄膜化しても高い光電変換効率が得られる。薄膜化により、発電電流は多少は低下するが、従来の基板に対し薄膜化による発電電流低下は大幅に改善できている。また、薄膜化により、開放電圧と形状因子が向上される。薄膜化による光電変換層の薄膜化により、光電変換層に含まれる欠陥を膜厚相当分低下できること、および光電変換層内に発生する起電力に対する電位勾配が拡大することによる生成電荷の再結合(欠陥による消滅)確率を低下できるためである。

[0041] 薄膜化は、生産性の点でメリットが大きい。光電変換装置ひとつあたりの生産時間を短縮でき、さらに生産装置の製膜室内部のメンテナンス頻度も低下でき、結果として、時間あたり或いは装置あたりの生産量を薄膜化の膜厚の比率以上に増大できる。従って、生産を考慮すると、光電変換効率の向上以上に、生産性向上のメリットが大きいといえる。

図面の簡単な説明

[0042] [図1]本発明の光電変換装置の構成を示す概略図である。

[図2]本発明の第1実施形態で用いられる透明電極付き基板の形状及び構成を示す一部切欠き断面図である。

[図3]図2に示す山部112の拡大図である。

[図4]本発明の太陽電池パネルの製造方法の実施形態の一部を示す概略図である。

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[図5]本発明の太陽電池パネルの製造方法の実施形態の一部を示す概略図である。

[図6]本発明の太陽電池パネルの製造方法の実施形態の一部を示す概略図である。

[図7]本発明の太陽電池パネルの製造方法の実施形態の一部を示す概略図である。

[図8]本発明の第2実施形態のイオン処理前における透明電極付き基板の透明電極表面の電子顕微鏡写真である。

[図9]本発明の第2実施形態のイオン処理後における透明電極付き基板の透明電極表面の電子顕微鏡写真である

[図10]本発明の第2実施形態の透明電極付き基板を用いて作製したタンデム型太陽電池の断面の透過型電子顕微鏡写真である。

[図11]本発明の第2実施形態の透明電極付き基板を用いて作製したタンデム型太陽電池の断面の透過型電子顕微鏡写真である。実施例7に示したように非晶質Si—i層の製膜後期を位相遮断層として、非晶質Si層を貫通する異相を抑制したものである。

[図12]実施例11のタンデム型太陽電池における、ボトムセルのn層製膜後のラマン比と太陽電池特性の関係を示す図である。

符号の説明

[0043] 1 基板

2 透明電極層

3 光電変換層

4 裏面電極層

6 太陽電池モジュール

90 光電変換装置

91 第1セル層(トップ層)

92 第2セル層(ボトム層)

93 中間コンタクト層

110 透明電極付き基板

111 基板

112 山部

114 透明電極

115 小山部

116 連続層

117 凸部

H_a 山部の高さ

P_a 山部間の平均ピッチ

H_c 小山部H_cの高さ

P_c 小山部間の平均ピッチ

H_b 凸部の高さ

P_b 凸部間のピッチ

15 絶縁溝

21 バックシート

23 出力ケーブル

50 太陽電池パネル

発明を実施するための最良の形態

[0044] 第1実施形態

以下に、本発明の第1実施形態について、図面を参照して説明する。

[0045] まず、本実施形態の光電変換装置の製造方法により製造される光電変換装置の構成について説明する。

[0046] 図1は、本実施形態の光電変換装置の構成を示す概略図である。光電変換装置90は、シリコン系太陽電池であり、基板1、透明電極層2、太陽電池光電変換層3としての第1セル層(トップ層)91ならびに第2セル層(ボトム層)92、及び裏面電極層4を具備する。本実施形態において、第1セル層91は非晶質シリコン系半導体を主として有する光電変換層であり、第2セル層は結晶質シリコン系半導体を主として有する光電変換層である。第2セル層92は、膜厚が1.2μm以上2.0μm以下、かつ、第

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2セル層92のラマン比が3．0以上8．0以下であることが好ましい。より好ましくは、ラマン比が3．5以上8．0以下であり、更に好ましくは5．0以上7．5以下である。

[0047] 第2セル層92のラマン比を3．0以上8．0以下とすることにより、結晶の粒界が適度に非晶質シリコンで充填された光電変換装置を得ることができ、結晶粒界の電流リークを抑制できるので、開放電圧(Voc)及び形状因子(FF)の低下が抑制された光電変換装置を得ることができる。

[0048] ここで「ラマン比」とはラマン分光評価で520cm^{-1}の結晶Siの強度と480cm^{-1}の非晶質Siの強度の比(結晶Siの強度／非晶質Siの強度)をいう(以下同じ)。ラマン比の測定方法としては、光電変換装置の裏面電極を過酸化水素水等の溶剤で溶剤除去して供試体とする。まず、第2セル層92の膜面側から測定用光を照射する。測定用光としては、レーザー単色が用いられ、例えば、YAGレーザー光の2倍波(波長532nm)が好適に用いられる。第2セル層92の膜面側から測定用光を入射すると、ラマン散乱が観測されるが、測定用光、及び散乱光の一部は第2セル層92中で吸収される。したがって、例えば、YAGレーザー光の2倍波を測定用光として用いた場合は、入射面から約0．1μmの深さまでの情報を得ることができる。なお、第2セル層92と裏面電極層4との間に第2の透明電極層を形成している場合は、第2の透明電極層のラマンピークはバックグランドとして差し引くことができるので、第2の透明電極層を希塩酸等の溶剤により溶剤除去しなくてもしてもよい。

[0049] 上記したように、ラマン比は光電変換層i層(実質的に真性な層)を評価するが、一般的に用いられるレーザー波長532nmでは、0．1μmの侵入深さにより、表面から約0．1μmの膜の結晶化率を評価することとなる。本実施形態においては、第2セル層92のi層製膜後のラマン比が3．0以上8．0以下であることが直接的な意味であるが、最表面にn層が製膜されてもn層は膜厚が0．03μm程度と薄いのでi層からの情報が支配的であること、および一般的なn層の結晶性も2～10であることにより、n層製膜後にn層を含めたラマン比を計測してもn層製膜前と近い値となる。したがって、第2セル層92のラマン比は、3．0以上8．0以下が好ましい範囲となる。

また、ラマン比は製膜において製膜装置構造などにより基板1上で分布が発生する。例えば製膜時に基板1表面上での原料ガス組成変化による局所的なラマン比分布

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や、プラズマや温度分布による全体的なラマン比分布がある。このため、評価する基板1上で極力全体的な平均値として評価する。例えば、1m角以上の基板サイズであれば、均等に区分けした少なくとも10箇所以上の領域で計測し、この平均値で評価することが好ましい。

[0050] ラマン比が3.0以上8.0以下という値は、一般的に結晶化が進んだ結晶質シリコンの値より、非晶質シリコンを多く含むものである。特にダブルテクスチャ基板のような高ヘイズ基板を用いる場合、基板の凹凸に起因する結晶粒界の欠陥が生じるため、粒界を適度に非晶質シリコンで充填することが重要となる。ラマン比が3.0以上が好ましい理由は、結晶シリコン部で発生した電荷が断面方向につながった結晶構造を導通することができるように大部分の結晶構造が膜厚方向に連続するために必要なラマン比が3.0以上であるためで、これは断面観察により確認できる。ラマン比が8.0以下が好ましい理由は、柱状結晶の粒界が電流リークポイントとなり電圧が発生しなくなるのを抑制するために非晶質で結晶粒界を充填することが好ましく、実験的にその場合のラマン比が8.0以下であるためである。

[0051] なお、ここで、「シリコン系」とはシリコン(Si)やシリコンカーバイド(SiC)やシリコンゲルマニウム(SiGe)を含む総称である。また、「結晶質シリコン系」とは、アモルファスシリコン系すなわち非晶質シリコン系以外のシリコン系を意味するものであり、微結晶シリコンや多結晶シリコン系も含まれる。

[0052] 第1セル層91及び第2セル層92の間には、透明導電膜からなる中間コンタクト層93を設けても良い(但し、本発明の光電変換装置は、中間コンタクト層93を設けたものに限定されない)。中間コンタクト層93
を設けた場合、この中間コンタクト層93で入射太陽光の一部が反射されて、第1セル(トップ層)91に再度入射される。これにより、第1セル層(トップセル)91における発電電流が増加する。そして、第1セル層91の膜厚を薄くしても、中間コンタクト層93が積層されない場合と同等の発電電流を得ることができる。したがって、第1セル層91非晶質シリコン系半導体の膜厚を薄くすることにより、当該第1セル層91における光劣化を抑制でき、光電変換装置全体としての安定化効率を向上させることができる。

[0053] 中間コンタクト層93の膜厚を厚くすることにより、第1セル層91である非晶質シリコ

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ン系半導体の発電電流を増加させることができる。このとき，中間コンタクト層93により反射される太陽光の波長における第2セル層92での発電電流は減少する。実際には，第2セル層92である結晶質シリコン系半導体においては，第1セル層91である非晶質シリコン系半導体よりも長波長領域の太陽光による電気エネルギーへの変換が行われている。

[0054] 従って，中間コンタクト層93の膜厚を最適化することにより，中間コンタクト層93による，第2セル層92である結晶質シリコン系半導体が吸収すべき長波長領域の太陽光の吸収率を抑制することが必要になる。

[0055] 本実施の形態に係わる光電変換装置の中間コンタクト層93の膜厚と，第2セル層92における波長800nm（太陽光の長波長領域に対応）の量子効率（入射のうち発電に寄与する割合）との関係から，中間コンタクト層93の膜厚が厚くなると，中間コンタクト層93での長波長領域の太陽光の反射率も増大して，第2セル層92に入射する光量が減少する。中間コンタクト層93は，光吸収率がλ＝450nm以上1000nm以下の範囲で1％未満であることが好ましく，この波長領域に対しては，ほぼ透明であることが好ましい。

[0056] 一方，中間コンタクト層93の膜厚が厚くなると，中間コンタクト層93と裏面電極層4との間で光の閉じ込め効果が増大する。このため，第2セル層92に入射した光吸収率が増大する。波長800nmの太陽光に対して，第2セル層92における光の閉じ込め効果が有効に作用する（量子効率を一定の値に維持することができる）中間コンタクト層93の膜厚は100nm以下である。

[0057] 上述したように，第1セル層91と第2セル層92との発電電流バランスを考慮して，最適な中間コンタクト層93の膜厚値は実験的に90nm以下となり，より好ましくは50nm以上70nm以下となる。これにより，より高い安定化効率を有する光電変換装置が実現される。

[0058] 次に，本発明の第1実施形態による光電変換装置において用いられる，透明電極を形成した透明絶縁性基板（以下，「透明電極付き基板」ともいう）の形状及び構成を，図2及び図3を用いて詳細に説明するが，本発明の光電変換装置及びその製造方法は，これらの図面によって限定されない。

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[0059] 図2は、本実施形態で用いられる透明電極付き基板の形状及び構成を示す一部切欠き断面図であり、図3は、図2に示す山部112の拡大図である。図2に示すように、本実施形態において用いられる、透明電極付き基板110は、ガラス基板111上に、不連続な複数の山部112によるマクロな凹凸(テクスチャ)と、この山部間をうめる複数の平坦部113とを有しており、該山部112及び該平坦部113の外表面は、ミクロの多数の凹凸(テクスチャ)を有する構造となっている。以下、このような2つの凹凸を有する構造を、ダブルテクスチャ構造という。

[0060] また、本実施形態においては、図2に示すように、透明電極114は、第1の酸化物からなる不連続な小山部115と、その上に形成される第2の酸化物からなる連続層であって該連続層の表面にミクロの多数の凸部を連続して有する連続層116とからなるのが好ましい。小山部115の密度は、基板111面の10μm角あたり15以上50以下とされ、20以上45以下がより好ましい。この小山部115間の平均ピッチP_sは、1.0μm以上3μm以下に相当する。

第2の酸化物からなる連続層116は、小山部115上及び小山部115が形成されていない部分のガラス基板111上に連続的に形成されている。

[0061] 本実施形態においては、上記山部112の平均の高さH_s(平坦部上のミクロの凸部の頂部からの高さの平均値)は、0.4μm以上0.7μm以下であり、0.5μm以上0.6μm以下であることがより好ましい。

また、隣接する上記山部間の平坦部の距離(以下、単に「山部間の間隔」ともいう。)W_sは、直線上に0μm以上1.5μm以下であることが好ましく、0μm以上1.0μm以下であることがより好ましく、0.1μm以上0.4μm以下(いずれの山部112も不連続である)であることがさらに好ましい。本実施形態においては、複数の山部112は不連続である部分と連続している部分があってもよく、山部間の間隔W_sが0μm以上1.5μm以下であるということは、平坦部がないところがあってもよいということである。なお、平坦部が無い場合には、上記山部に隣接していなくても、上記山部付近の平坦部を用いてH_sを計測でき、または断面の顕微鏡観察を行うことでH_sは計測することができる。

さらに、上記山部112の密度は、小山部115の密度と同様の値となり、基板111面

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の10μm角あたり15以上50以下となり、20以上45以下がより好ましい。この山部112間の平均ピッチP_sは、1.0μm以上3μm以下に相当する。

[0062] 本実施形態においては、上記小山部115の高さH_cは、上記山部の高さH_sと同様の値、すなわち0.4μm以上0.7μm以下であり、0.5μm以上0.6μm以下であることがより好ましい。

[0063] 本実施形態においては、山部112及び平坦部113の表面、すなわち、第2の酸化物からなる連続層116の表面は、図3に示されるように、ミクロの多数の凸部117を有している。ミクロの多数の凸部の底面径が0.1μm以上0.3μm以下であり、高さ／底面径の比が0.7以上1.2以下である。尚、ミクロの凸部の連続層は、表面全体においてミクロの凸部が存在する状況を示していて、一部にミクロの凸部が欠損した領域が存在しても、連続している状況とみなすものである。

[0064] また、図3において、上記小山部115上の連続層116の厚さH_d(ミクロの凸部を含む)は、0.5μm以上1.0μm以下であることが好ましく、0.5μm以上0.7μm以下であることがより好ましい。同様に、上記ガラス基板111上の連続層116の厚さH_e(ミクロの凸部を含む)は0.5μm以上1.0μm以下であることが好ましく、0.5μm以上0.7μm以下であることがより好ましい。

[0065] 本実施形態においては、上記山部112及び上記平坦部113の外表面を、このような山部による凹凸(マクロな凹凸)よりも小さな凹凸(ミクロな凹凸)とすることにより、短波長の光を強く散乱することができ、全体として広い領域の光を有効に散乱することが可能になる。すなわち、大きな凹凸である山部により長波長の光を散乱し、小さな凹凸表面より短波長の光を散乱することができるため、全体として高い光散乱性を達成することができる。

特に本実施形態においては、山部112の高さと密度を制御することにより、長波長の光の散乱を最適化し、結晶質シリコン系半導体からなる光電変換層の発電効率の向上と、製膜時間の短縮が実現される。

[0066] 前記透明電極付き基板110におけるこのような表面性状は、例えば、以下に示す方法により確認することができる。

(1)表面形状の解析:膜表面の凸部を走査型電子顕微鏡(SEM)で観察し、得ら

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れる顕微鏡写真より、凸部の底面径を測定することができる。また、膜表面の凹凸形状をSEM、原子間力顕微鏡(AFM)により観察し、得られる顕微鏡写真より、膜表面の凹凸形及び凸部の高さを解析することができる。

(2)表面被覆率の測定:第1の酸化物からなる小山部の基板上への被覆率をSEM写真から測定し、基板上を小山部が占める面積を、基板の当該被覆面全体の面積で割った値を表面被覆率として評価することができる。

また、質量膜厚とは、基板上の一定面積中にある不連続の金属酸化物に対し、蛍光X線装置でその金属酸化物の金属量に比例する検出量を調べ、別途用意してある基板上に連続し、膜厚の既知の同種の金属酸化物における蛍光X線装置の検出量と比較して、不連続な酸化物の体積が連続になったと仮定して得られた膜厚を示す。

[0067] また、このような形状及び構成を有する透明電極付き基板110は、基板全体において、550nm以上800nm以下の波長における分光ヘイズ率が30%以上、好ましくは40%以上である。

[0068] ここで、「分光ヘイズ率」とは、透過光における散乱成分の割合を示すものである。分光ヘイズ率は波長に依存し、分光ヘイズ率をHz(λ)、全透過率を$T_{total}(\lambda)$、透過光の直進成分を$T_{direct}(\lambda)$、透過光の散乱成分を$T_{diffuse}(\lambda)$とすると、下記式に示す関係が成り立つ。

$$T_{total}(\lambda)=T_{direct}(\lambda)+T_{diffuse}(\lambda)$$

$$Hz(\lambda)=T_{diffuse}(\lambda)/T_{total}(\lambda)\times 100[\%]$$

[0069] 以下に、上述した本実施形態の透明電極付き基板の形状及び構成ならびに特性を満たす基板(透明基板)、第1の酸化物及び第2の酸化物について詳述する。

[0070] <基板(透明基板)>

本実施形態の透明電極付き基板に用いられる基板は、必ずしも平面で板状である必要はなく、曲面でも異型状でもよい。

このような基板としては、少なくともその表面が後述する第1の酸化物と異なる材料であることが好ましく、具体的には、ガラス基板、セラミックス基板、プラスチック基板、金属基板等や、これらの基板表面に酸化ケイ素膜、酸化アルミニウム膜、酸化ジルコ

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ニウム膜、酸化チタン膜などのアルカリバリヤ層を施したもの等が挙げられる。これらのうち、透光性に優れた透明の基板であることが好ましく、ガラス基板もしくはアルカリバリア層を施したガラス基板であることが強度及び耐熱性の点から好ましい。

また、このような基板は、光電変換層の主たる吸収波長域である550nm以上800nm以下の波長領域において高い透過率、例えば80%以上の透過率を有することが好ましく、十分絶縁性で、かつ化学的、物理的耐久性が高いことが望ましい。

[0071] 上記ガラス基板としては、具体的には、例えば、無色透明なソーダライムシリケートガラス、アルミノシリケートガラス、ボレートガラス、リチウムアルミノシリケートガラス、石英ガラス、ホウ珪酸ガラス基板、無アルカリガラス基板、その他の各種ガラスからなる透明ガラス板を用いることができる。

また、本実施形態の透明電極付き基板を太陽電池用基板に用いる場合においては、ガラス基板の厚さは0.2mm以上6.0mm以下であることが、強度及び透過率の点から好ましい。

[0072] なお、ソーダライムシリケートガラス等のナトリウムを含有するガラスからなるガラス基板または低アルカリ含有ガラスからなるガラス基板の場合には、ガラスからその上面に形成される透明電導膜へのアルカリ成分の拡散を最小限にするために、上述したアルカリバリヤ層を施したガラス基板を用いることが好ましい。

また、ガラス基板の表面に、ガラス基板の表面と、その上に設けられる層との屈折率の差異を軽減するための層をさらに有していてもよい。

[0073] <第1の酸化物>

本実施形態の透明電極付き基板の透明電極膜を構成する第1の酸化物は、可視光域で高透明な酸化物であれば特に限定されず、その具体例としては、TiO_2、SnO_2、In_2O_3、ZnO、CdO、$CdIn_2O_4$、$CdSnO_3$、$MgIn_2O_4$、$CdGa_2O_4$、$GaInO_3$、$InGaZnO_4$、$Cd_2Sb_2O_7$、Cd_2GeO_4、$CuAlO_2$、$CuGaO_2$、$SrCu_2O_2$、Al_2O_3等が挙げられる。これらのうち、TiO_2、SnO_2及びフッ素を含有するSnO_2からなる群より選択される少なくとも1種を用いることが好ましい。

本実施形態においては、小山部を形成するこのような第1の酸化物の屈折率は、波長400nm以上800nm以下において、1.8以上2.2以下であることが好ましく、さら

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に、1．9以上2．1以下であることが好ましい。

第1の酸化物の形成方法として一例を示す。上述したアルカリバリア層付きガラス基板をベルトコンベア炉において520℃に加熱し、四塩化錫、水、塩化水素ガスを同時にガラス基板に吹き付けて酸化錫核を形成する。この際，四塩化錫、水は，あらかじめ加熱し、窒素ガスをバブリングして塩化水素ガスと同時に移送することでガラス基板上に吹き付ける。

酸化錫核を形成した後、四塩化錫と水を同時にガラス基板に吹き付けることで第1の酸化物であるSnO_2を形成する。この際，四塩化錫、水は、あらかじめ加熱し、窒素ガスをバブリングして移送することでガラス基板上に吹き付けた。

[0074] なお、このような第1の酸化物からなる小山部は、上述したように，不連続な突起物であって連続膜ではないので、該突起物に覆われていない透明基板部分は、当然ながら小山部による入射光の吸収損はゼロであるため、光電変換層への入射光量を増やすことができる。

これらの小山部は、長波長光の分光ヘイズ率を高める(光の散乱度を上げる)部分であり、自由電子による吸収を抑えて、高透明にするために、電気導電性はないのが好ましい。したがって、上記第1の酸化物としてSnO_2を用いた場合は、SnO_2のみからなるか、フッ素を含有する場合でもフッ素は、SnO_2に対して0．01mol%以下の含有量であることが好ましく、0．005mol%以下の含有量であることがより好ましい。

[0075] ＜第2の酸化物＞

本実施形態の透明電極付き基板の透明電極膜を構成する第2の酸化物は、可視光域で透明であり、さらに導電性を有している透明導電性酸化物であることが必要であり、その具体例としては、SnO_2、ZnO、In_2O_3等が挙げられ、2種以上を併用してもよく、さらに、導電性発現のためのドーパントを含有していることが好ましい。

これらのうち、SnO_2はドーパントとしてフッ素またはアンチモンをSnO_2に対して0．01mol%以上4mol%以下含有することが好ましい。ZnOはドーパントとしてホウ素、Al及びGaからなる群から選択される少なくとも1種をZnOに対して0．02mol%以上5mol%以下含有することが好ましい。In_2O_3はドーパントとしてSnをIn_2O_3に対して0．02mol%以上4mol%以下含有することが好ましい。なお、これらのドーパントを用い

たドーピングは、ハロゲン化水素によるものであってもよい。このようなハロゲン化水素としては、具体的には、例えば、HF、HBr等が挙げられる。

本実施形態においては、連続層を形成するこのような第2の酸化物の屈折率は、波長400nm以上800nm以下において、1．8以上2．2以下であることが好ましく、さらに、1．9以上2．1以下であることが好ましい。

[0076] また、上記第2の酸化物としてフッ素を含有するSnO_2を用いることにより、導電電子密度が向上する。太陽電池に用いる基板としては、導電電子密度は、$5\times10^{19}cm^{-3}$以上$4\times10^{20}cm^{-3}$以下であることが好ましく、$1\times10^{20}cm^{-3}$以上$2\times10^{20}cm^{-3}$以下であることがより好ましい。導電電子密度がこの範囲であれば、第2の酸化物からなる連続層の光吸収量が少なく、高透明で、かつ活性水素種に対して高い耐久性があるので、薄膜シリコン系太陽電池を形成する際に一般に用いられる水素プラズマ照射によっても、透明性は損なわれないため好ましい。

[0077] 上述した第1の酸化物と第2の酸化物とは、同じ酸化物を用いてもよく、本実施形態においては、いずれもSnO_2を用いることが好ましい。また、第1の酸化物及び第2の酸化物層の屈折率は、同等程度であることが好ましく、具体的には、1．8以上2．2以下であることが好ましい。第1の酸化物と第2の酸化物の屈折率がともにこの範囲であると、第1の酸化物と第2の酸化物との界面における光の反射が制御され、透過率が低下しないことから好ましい。

[0078] また、本実施形態においては、上述した第1の酸化物からなる小山部と、上述した第2の酸化物からなる連続層との間に、該第1の酸化物及び該第2の酸化物とは組成が異なる酸化物からなる酸化物層（以下，単に「異なる酸化物層」ともいう。）を有していることが好ましい。

このような異なる酸化物層を有していることにより、第2の酸化物からなる連続層の表面にミクロの多数の凸部が形成されやすく、山部と平坦部とを有する構造を容易に形成することができる。

[0079] また、このような異なる酸化物層を有する多層構造の透明電極膜においては、各層の界面での反射を軽減し、後述する光電変換層への入射光量を最大にする必要がある。すなわち、ガラス基板、第1の酸化物からなる小山部、異なる酸化物層、第2の

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酸化物からなる連続層の各界面での光反射をできるだけ低減することが望ましい。そのためには、第1の酸化物、異なる酸化物及び第2の酸化物の屈折率ができるだけ近いこと、または屈折率が離れている場合は、異なる酸化物層ができるだけ薄いことが望ましい。

このような異なる酸化物としては、具体的には、例えば、Si、Sn、Al、Zr及びTiからなる群から選ばれる1種以上の原子の酸化物が挙げられ、これらのうち、Siの酸化物を主成分とすることが好ましい。また、上記異なる酸化物は、高い透光性を有する必要があるため、非結晶性であるSiO_2であることがより好ましい。

なお、異なる酸化物層の膜厚は2nm以上40nm以下であることが好ましく、10nm以上30nm以下であることがより好ましい。

[0080] 本実施形態の透明電極付き基板は、上述したように、複数の山部とその間をうめる複数の平坦部とで構成され、該山部及び外平坦部の表面がミクロの多数の凸部を連続して有するものであるが、基板上から山部の頂上(ミクロの凸部を含む)までの高さは0.8μm以上3.0μm以下であることが好ましく、0.8μm以上1.0μm以下であることがより好ましい。ミクロの多数の凸部の底面径が0.1μm以上0.3μm以下であり、高さ/底面径の比が0.7以上1.2以下であることが望ましい。また、膜全体のシート抵抗が8Ω/□以上20Ω/□以下であることが好ましく、8Ω/□以上12Ω/□以下であることがより好ましく、550nmにおける透過率(透明性)は、浸液法で測定した場合、80%以上90%以下であることが好ましく、85%以上90%以下であることがより好ましい。

また、上記構成からなる本実施形態の透明電極付き基板を、光電変換装置の透明電極に用いると、基板を経て入射された光は、透明電極により屈折、散乱されて光電変換部に入射し、光電変換部中を長い距離にわたって通過する。その結果、多くの光が光電変換部にて吸収され、光電変換効率が向上する効果を奏するものとなる。特に、太陽電池に用いた場合には、開放電圧及び曲線因子を低下させずに短絡電流を高く維持することが可能となるため、光電変換効率が向上するものとなる。

[0081] 次に、本実施形態の太陽電池パネルの製造方法について説明する。ここでは、基板1としてのガラス基板上に太陽電池光電変換層3として非晶質シリコン系半導体を

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主として有する光電変換層及び結晶質シリコン系半導体を主として有する光電変換層を順次積層する例について説明する。図4～図7は、本実施形態の太陽電池パネルの製造方法を示す概略図である。

[0082] (1)図4(a):

基板1としてソーダフロートガラス基板(1．4m×1．1m×板厚:4mm)を使用する。基板端面は破損防止にコーナー面取りやR面取り加工されていることが望ましい。

[0083] (2)図4(b):

前記実施形態に基づき、基板1上に透明電極層2を製膜し、透明電極付き基板を形成する。透明導電層2として，透明電極膜に加えて、基板1と透明電極膜との間にアルカリバリア膜(図示されず)を形成しても良い。アルカリバリア膜は、酸化シリコン膜(SiO_2)を50nm以上150nm以下、熱CVD装置にて約500℃で製膜処理する。

[0084] (3)図4(c):

その後、基板1をX－Yテーブルに設置して、YAGレーザーの第1高調波(1064nm)を、図の矢印に示すように、透明電極膜の膜面側から入射する。加工速度に適切となるようにレーザーパワーを調整して、透明電極膜を発電セル5の直列接続方向に対して垂直な方向へ、基板1とレーザー光を相対移動して，溝10を形成するように幅約6mm以上12mm以下の短冊状にレーザーエッチングする。

[0085] (4)図4(d):

プラズマCVD装置により、減圧雰囲気:30Pa以上150Pa以下、基板温度:約200℃、プラズマRF発生周波数:13MHz以上100MHz以下にて光電変換層3の第1セル層(トップ層)91として、非晶質シリコン薄膜からなるp層膜／i層膜／n層膜を順次製膜する。第1セル層91は、SiH_4ガスとH_2ガスとを主原料に，透明導電層2の上に製膜される。太陽光の入射する側からp層、i層、n層がこの順で積層される。

[0086] 本実施形態において、第1セル層91のp層は、SiH_4, H_2, CH_4, B_2H_6ガスをRFプラズマで反応生成させた、非晶質のBドープSiC膜であり、膜厚は4nm以上16nm以下とすることが好ましい。第1セル層91のi層は、SiH_4とH_2をRFプラズマで反応生成させた、非晶質Si膜であり、膜厚は100nm以上400nm以下とすることが好ましい。第1セル層91のn層は、SiH_4, H_2, PH_3ガスをRFプラズマで反応生成させた、結晶

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成分を含むSi膜であり、n層単膜のラマン比は2以上であり、膜厚は10nm以上80nm以下とすることが好ましい。なお、ここで「ラマン比」とはラマン分光評価で520cm^{-1}の結晶Siの強度と480cm^{-1}の非晶質Siの強度の比（結晶Siの強度／非晶質Siの強度）をいう（以下同じ）。また、前記p層（SiC膜）とi層（Si膜）の界面でのバンド不整合を抑制するために、バッファー層（図示略）として，バンドギャップが中間の物質を挿入しても良い。

[0087] 次に、第1セル層91の上に、プラズマCVD装置により、減圧雰囲気：3kPa以下，基板温度：約200℃、プラズマRF発生周波数：40MHz以上200MHz以下にて、第2セル層（ボトム層）92としての微結晶シリコン薄膜からなる微結晶p層膜／微結晶i層膜／微結晶n層膜を順次製膜する。

[0088] 本実施形態において、第2セル層92のp層は、SiH_4，H_2，B_2H_6ガスをRFプラズマで反応生成させた、結晶成分を含むSi膜であり、p層単膜のラマン比は2以上であり、膜厚は10nm以上60nm以下とすることが好ましい。第2セル層92のi層は、SiH_4とH_2をRFプラズマで反応生成させた，結晶成分を含むSi膜であり、このi層を1．5μm膜厚に積んだときのラマン比は3．0以上8．0以下であり，膜厚は1200nm以上2000nm以下とすることが好ましい。より好ましくは、ラマン比を3．5以上8．0以下、さらに好ましくは5．0以上8．0以下とすると好適である。ラマン比の下限値は，結晶シリコン部で発生した電荷が断面方向につながった結晶構造を導通することができるように、大部分の結晶構造が膜厚方向に連続するために必要なラマン比が3．0以上であることから決まり、これは断面観察により確認することができる。また、ラマン比の上限値は柱状結晶の粒界が電流リークポイントとなり、電圧が発生しなくなるのを抑制するために、非晶質で結晶粒界を充填することが好ましく、ラマン比が8．0以下であることが実験的に求められる。

[0089] 第2セル層92のn層は、SiH_4，H_2，PH_3ガスをRFプラズマで反応生成させた、結晶成分を含むSi膜であり、n層単膜のラマン比は2以上であり、膜厚は10nm以上80nm以下とすることが好ましい。

[0090] 微結晶シリコン薄膜、特に微結晶i層膜をプラズマCVD法で形成するにあたり、プラズマ放電電極と基板1の表面との距離dは、3mm以上10mm以下にすることが好ま

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しい。3mmより小さい場合、大型基板に対応する製膜室内の各構成機器精度から距離dを一定に保つことが難しくなるとともに、近過ぎて放電が不安定になる恐れがある。10mmより大きい場合、十分な製膜速度(1nm／s以上)を得難くなるとともに、プラズマの均一性が低下しイオン衝撃により膜質が低下する。第2セル層92のi層は、RF周波数40MHz以上200MHz以下、ガス圧力0.5kPa以上3kPa以下、製膜速度1nm／s以上3nm/s以下で製膜されることが好ましく、本実施形態においてはRF周波数60MHz、ガス圧力1.6kPa、製膜速度2nm／sで製膜される。

[0091] 第1セル層91と第2セル層92の間に電流整合性を取るために半反射膜となることを目的に、中間コンタクト層93として、膜厚0nm以上90nm以下のZnO系膜(例えばGZO(Gaドープ ZnO)膜)をスパッタリング装置により製膜して設けても良い。この中間コンタクト層93は、ZnO単膜での光吸収率がλ=450nm以上1000nm以下の範囲で1%未満であることが好ましい。

[0092] (5)図4(e)

基板1をX－Yテーブルに設置して、レーザーダイオード励起YAGレーザーの第2高調波(532nm)を、図の矢印に示すように、光電変換層3の膜面側から入射する。パルス発振:10kHz以上20kHz以下として加工速度に適切となるようにレーザーパワーを調整して、透明導電層2のレーザーエッチングラインの約100μm以上150μm以下の横側を狙い、溝11を形成するようにレーザーエッチングする。レーザーエッチングラインの位置は、逆転していなければ問題ないものであるが、位置決めの公差を考慮して、前記数値を狙ったものである。

[0093] (6)図5(a)

裏面電極層4としてAg膜をスパッタリング装置により減圧雰囲気、約150℃にて順次製膜する。裏面電極層4は本実施形態では、Ag膜を膜厚150nm以上で製膜し、さらにn層と裏面電極層4との接触抵抗低減と光反射向上を目的に、光電変換層3と裏面電極層4との間に膜厚10nm以上のZnO系膜(例えばGZO(Gaドープ ZnO)膜)をスパッタリング装置により製膜して設ける。

[0094] (7)図5(b)

基板1をX－Yテーブルに設置して、レーザーダイオード励起YAGレーザーの第2

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高調波(532nm)を、図の矢印に示すように、基板1側から入射する。レーザー光が光電変換層3で吸収され、このとき発生する高いガス蒸気圧を利用して裏面電極層4が爆裂して除去される。パルス発振:1kHz以上10kHz以下として加工速度に適切となるようにレーザーパワーを調整して、透明導電層2のレーザーエッチングラインの約250μm以上400μm以下の横側を狙い、溝12を形成するようにレーザーエッチングする。レーザーエッチングラインの位置は、逆転していなければ問題ないものであるが、位置決めの公差を考慮して、前記数値を狙ったものである。

[0095] (8)図5(c)

発電領域を区分して、基板端周辺の膜端部においてレーザーエッチングによる直列接続部分が短絡し易い影響を除去する。基板1をX－Yテーブルに設置して、レーザーダイオード励起YAGレーザーの第2高調波(532nm)を、基板1側から入射する。レーザー光が透明導電層2と光電変換層3で吸収され、このとき発生する高いガス蒸気圧を利用して裏面電極層4が爆裂して、裏面電極層4／光電変換層3／透明導電層2が除去される。パルス発振:1kHz以上10kHz以下として加工速度に適切となるようにレーザーパワーを調整して、基板1の端部から5mm以上15mm以下の位置を、X方向絶縁溝15を形成するようにレーザーエッチングする。このとき、Y方向絶縁溝は後工程で基板1周囲領域の膜面研磨除去処理を行うので、設ける必要がない。

絶縁溝15は基板1の端より5mm以上10mm以下の位置にてエッチングを終了させることにより、太陽電池パネル端部からの太陽電池モジュール6内部への外部湿分侵入の抑制に、有効な効果を呈するので好ましい。

[0096] (9)図6(a)

後工程のEVA等を介したバックシートとの健在な接着・シール面を確保するために、基板1周辺(周囲領域14)の積層膜は、段差があるとともに剥離し易いため、この膜を除去する。まず、基板の端から5mm以上20mm以下で、前述の図5(c)工程で設けた絶縁溝15よりも基板端側における裏面電極層4／光電変換層3／透明導電層2において、砥石研磨やブラスト研磨などを用いて除去を行う。研磨屑や砥粒は基板1を洗浄処理して除去した。

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[0097] (10)図6(b)

端子箱取付け部分はバックシートに開口貫通窓を設けて集電板を取出す。この開口貫通窓部分には絶縁材を複数層を設置して外部からの湿分などの浸入を抑制する。

直列に並んだ一方端の太陽電池発電セル5と、他方端部の太陽電池発電セル5とから銅箔を用いて集電して太陽電池パネル裏側の端子箱部分から電力が取出せるように処理する。銅箔は各部との短絡を防止するために銅箔幅より広い絶縁シートを配置する。

集電用銅箔などが所定位置に配置された後に、太陽電池モジュール6の全体を覆い、基板1からはみ出さないようにEVA(エチレン酢酸ビニル共重合体)等による充填材シートを配置する。

EVAの上に、防水効果の高いバックシート21を設置する。バックシート21は本実施形態では防水防湿効果が高いようにPTEシート/AL箔/PETシートの3層構造よりなる。

バックシート21までを所定位置に配置したものを、ラミネータにより減圧雰囲気で内部の脱気を行い約150℃でプレスしながら、EVAを架橋させて密着させる。

[0098] (11)図7(a)

太陽電池モジュール6の裏側24に端子箱を接着剤で取付ける。

[0099] (12)図7(b)

銅箔と端子箱の出力ケーブル23とをハンダ等で接続し、端子箱内部を封止剤(ポッティング剤)で充填して密閉する。これで太陽電池パネル50が完成する。

[0100] (13)図7(c)

図7(b)までの工程で形成された太陽電池パネル50について発電検査ならびに、所定の性能試験を行う。発電検査は、AM1.5、全天日射基準太陽光(1000W/m^2)のソーラシミュレータを用いて行う。

[0101] (14)図7(d)

発電検査(図7(c))に前後して、外観検査をはじめ所定の性能検査を行う。

[0102] 上記実施形態では太陽電池として、トップセルとして非晶質(アモルファス)シリコン

系光電変換層を有し、ボトムセルとして結晶質(微結晶)シリコン系光電変換層を有するタンデム型太陽電池を用いたものについて説明したが、本発明は、この例に限定されるものではない。

例えば、光電変換層として微結晶シリコンをはじめとする結晶質シリコン系光電変換層のみを有するシングル型太陽電池や、前記トップセルと前記ボトムセルに加えてさらに1層もしくは2層以上の別の光電変換層を設けた多接合型太陽電池のような他の種類の薄膜太陽電池にも同様に適用可能である。

[0103] [実施例及び比較例]

比較例1:

透明電極付き基板として、不連続な複数の山部によるマクロな凹凸(テクスチャ)は形成せず、ミクロの多数の凹凸(テクスチャ)を有する、一層のテクスチャ構造を用いた。ミクロの多数の凸部の底面径が0.2～0.3μm、凸部の高さは0.1～0.2μmであり、高さ／底面径の比が0.7～1.0であった。分光ヘイズ率は、波長550nmにおいて20%、波長800nmでは4%である。一層のテクスチャ構造の透明電極付き基板を用いた以外は、本発明の前記実施形態に従って、タンデム型太陽電池を作製した。

透明電極付き基板上に形成した各層において、トップセルp層は膜厚8nm、トップセルn層は膜厚40nm、ボトムセルp層は膜厚30nm、ボトムセルn層は膜厚30nm、裏面電極のZnO層は膜厚80nm、裏面電極のAg層は膜厚300nmで、各比較例及び実施例において共通とした。本例のトップセルi層、ボトムセルi層の膜厚は、表1に示す通りとし、中間コンタクト層は形成しなかった。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を2μmに設定した本例の太陽電池の発電効率初期値は12.0%だった。なお、このときのボトムセルi層の膜厚は、基板上の太陽電池として構成される領域における膜厚分布を考慮して、その平均値で評価したものである。

なお、表2において、電池性能評価項目であるIsc、Voc、FF、Effは、それぞれ短絡電流、開放電圧、形状因子、発電効率(初期値)を表す。Iscの(a－Si／c－Si)は、分光感度から求めたa－Si(非晶質)トップセルのIsc及びc－Si(結晶系)ボトムセルのIscである。タンデムのIscはトップセルIscとボトムセルIscの低い方で律速される

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。本実施例及び比較例は、ボトムセル律速であり、ボトムセルのIscがタンデムのIscとなっている。また、表2に示す比較例及び実施例において、電池性能評価結果は、比較例1を1とした相対値で記載する。本結果は、劣化前の初期値を記載したが、劣化率は本試験の範囲内では同等と考えられ、相対値で表すなら劣化後も同等である。

[0104] 比較例2:

トップセルi層、中間コンタクト層、ボトムセルi層を表1に示す膜厚で形成した以外は前記比較例1と同様の方法に従って、タンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚250nmとZnO中間コンタクト層の膜厚50nmに対し、ボトムセルi層の膜厚を2μmに設定した本例の太陽電池の発電効率初期値は12.0%だった。

[0105] 比較例3:

トップセルi層、ボトムセルi層を表1に示す膜厚で形成した以外は前記比較例1と同様の方法に従って、タンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を1.5μmに設定した本例の太陽電池の発電効率初期値は10.8%に低下した。これは、発電電流が大幅に低下したためであり、比較例で用いた基板ではボトムセル膜厚が2μmなければ所望の電流が得られないということが分かった。

[0106] 実施例1:

本発明の前記実施形態に従って、タンデム型太陽電池を作製した。透明電極付き基板として、不連続な小山部とミクロの多数の凸部を有する層状のSnO_2を積層したダブルテクスチャ構造の基板(山部の高さ500nm、山部の密度は10μm角に30個)を適用した。本例のトップセルi層、ボトムセルi層の膜厚は、表1に示す通りとし、中間コンタクト層は形成しなかった。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を2μmに設定した本例の太陽電池の発電効率初期値は13.3%に向上できた。これは、ボトムセルの電流を大幅に増大できた効果である。

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本発明においては、ダブルテクスチャ構造の透明電極により、山部による大きな凹凸(マクロな凹凸)と、これよりも小さな凹凸(ミクロな凹凸)とすることにより、大きな凹凸である山部により長波長の光を散乱し、小さな凹凸表面より短波長の光を散乱することができる。このため、透明電極全体として広い波長領域の光において高い光散乱性を達成することができる。また山部による大きな凹凸があるため、太陽電池層の裏面電極にまで大きな凹凸形状が発生する。これにより、裏面電極からの反射光が太陽電池層内で有効に散乱するので、ボトムセルの電流を大幅に増大させることができる。

特に本発明においては、透明電極の山部の高さと密度を制御して太陽電池層の膜厚を最適化したので、長波長の光の散乱を最適化して、結晶質シリコン系半導体からなる光電変換層の発電効率が向上している。

[0107] 実施例2:

トップセルi層、ボトムセルi層を表1に示す膜厚で形成した以外は前記実施例1と同様の方法に従って、実施例2(1)のタンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を1.5μmに設定した本例の太陽電池の発電効率初期値は12.8%であり、比較例1に対し効率向上とボトムセル膜厚の25%薄膜化を同時に達成できた。本実施形態による透明電極付き基板の適用により、実施例1に記載したものと同様な効果によりボトムセルを薄膜化しても高い発電電流が得られ、ボトムセルを薄膜化できたためにVocとFFを向上できたためである。また、ボトムセルi層を薄膜化により、ボトムセルi層が厚かったためにこの製膜時間によって律速されていた光電変換装置の製造時間を大幅に短縮することができる。これにより、高速製膜との相乗効果で光電変換装置の生産性を向上させることができる。

さらに、電池性能のボトムセルi層膜厚依存性を調べるために、前記実施例2(1)のボトムセルi層の膜厚を変えて実施例2(2)～実施例2(5)のタンデム型太陽電池を作製した。各実施例におけるボトムセルi層の膜厚を表1に示す。また、各実施例の太陽電池の電池性能を表2に示す。

実施例2において、ボトムセルi層の膜厚が1.2μm以上2.4μm以下の範囲で、

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比較例1のボトムセルi層膜厚が2μmの場合と同等以上の効率が得られた。ボトムセルi層の膜厚のさらに好ましい範囲は1．5μm以上2μm以下である。

低下するのを抑制でき)VocとFFを向上できたためである。

[0108] 実施例3：

トップセルi層、中間コンタクト層、ボトムセルi層を表1に示す膜厚で形成した以外は前記実施例2(1)と同様の方法に従って、タンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚250nmとZnO中間コンタクト層の膜厚50nmに対し、ボトムセルi層の膜厚を1．5μmに設定した本例の太陽電池の発電効率初期値は12．8％だった。効率向上とボトムセル薄膜化を同時に達成できた。

[0109] 実施例4：

透明電極付き基板の山部の高さを表1に示す値に変えた以外は実施例2(1)と同様の方法に従って、実施例4(1)～実施例4(5)のタンデム型太陽電池を作製し、山部の高さと電池性能の関係を調べた。

得られた太陽電池の電池性能を表2に示す。山部の高さは0．4μm以上0．7μm以下が適正であった。山部の高さが0．4μm以上で高い発電電流が得られ、0．7μmを超えるとVocとFFが著しく低下するためである。

[0110] 実施例5：

透明電極付き基板の山部の密度を表1に示す値に変えた以外は実施例2(1)と同様の方法に従って、実施例5(1)～実施例5(6)のタンデム型太陽電池を作製し、山部の密度と電池性能の関係を調べた。

得られた太陽電池の電池性能を表2に示す。山部の密度が10μm角内に15個以上50個以下のとき、比較例1のi層膜厚2μmの場合と同等以上の効率が得られる。さらに好ましい範囲は10μm角内に20個以上45個以下である。密度が低すぎるとJsc(電流密度)が低下し、高すぎるとJscは飽和しVocとFFが低下して、効率が低下する。

[0111] [表1]

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		透明電極付き基板の山部	トップセルi層膜厚	中間層	ボトムセルi層膜厚	ボトムセルn層製膜後ラマン比
比較例1		—	300nm	なし	2μm	6.5
比較例2		—	250nm	50nm	2μm	6.5
比較例3		—	300nm	なし	1.5μm	5.8
実施例1		高さ0.5μm,密度30	300nm	なし	2μm	6.5
実施例2	(1)	高さ0.5μm,密度30	300nm	なし	1.5μm	5.8
	(2)		↑	↑	1μm	6.0
	(3)		↑	↑	1.2μm	5.4
	(4)		↑	↑	1.7μm	6.2
	(6)		↑	↑	2.4μm	6.8
実施例3		高さ0.5μm,密度30	250nm	50nm	1.5μm	5.8
実施例4	(1)	高さ0.4μm,密度30	300nm	なし	1.5μm	5.8
	(2)	高さ0.5μm,密度30	↑	↑	↑	5.8
	(3)	高さ0.6μm,密度30	↑	↑	↑	5.8
	(4)	高さ0.7μm,密度30	↑	↑	↑	5.8
	(5)	高さ0.9μm,密度30	↑	↑	↑	5.8
実施例5	(1)	高さ0.5μm,密度10	300nm	なし	1.5μm	5.8
	(2)	高さ0.5μm,密度15	↑	↑	↑	5.8
	(3)	高さ0.5μm,密度20	↑	↑	↑	5.8
	(4)	高さ0.5μm,密度30	↑	↑	↑	5.8
	(5)	高さ0.5μm,密度45	↑	↑	↑	5.8
	(6)	高さ0.5μm,密度50	↑	↑	↑	5.8

[0112] [表2]

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		電池性能			
		Isc (a-Si/c-Si)	Voc	FF	Eff
比較例1		1 (1/1)	1	1	1
比較例2		1 (1/1)	1	1	1
比較例3		0.89(1/0.89)	1	1	0.89
実施例1		1.15(1/1.15)	0.99	0.97	1.11
実施例2	(1)	1.06(1/1.06)	1.00	1.01	1.07
	(2)	0.80(1/0.80)	1.02	1.04	0.86
	(3)	0.96(1/0.96)	1.01	1.02	0.99
	(4)	1.03(1/1.03)	0.99	1.01	1.03
	(5)	1.13(1/1.13)	0.97	0.92	1.02
実施例3		1.06(1/1.06)	1.00	1.01	1.07
実施例4	(1)	1.00(1/1.00)	1.01	1.01	1.02
	(2)	1.06(1/1.06)	1.00	1.01	1.07
	(3)	1.08(1/1.08)	0.99	0.99	1.06
	(4)	1.10(1/1.10)	0.97	0.96	1.03
	(5)	1.10(1/1.10)	0.92	0.88	0.90
実施例5	(1)	0.93(0.9/0.9)	1.00	0.99	0.92
	(2)	0.99(1/0.99)	1.00	1.00	0.99
	(3)	1.04(1/1.04)	1.00	1.01	1.05
	(4)	1.06(1/1.06)	1.00	1.01	1.07
	(5)	1.06(1/1.06)	0.98	0.98	1.02
	(6)	1.05(1/1.05)	0.97	0.96	0.98

[0113] 第2実施形態

以下に、本発明の第2実施形態について、説明する。

本実施形態において、透明電極つき基板は、大型の凹凸と小型の凹凸が混在する

ことが望ましく、小型の凹凸(ミクロな凹凸)と大型の凹凸(マクロな凹凸)により、ピッチが0．1μmから1．2μm、高さが0．1μmから1．0μmの凹凸が混在している。ピッチ0．8μm以上の大きな凹凸により800nm以上の長波長の光を拡散、閉じ込めでき、ピッチ0．3μm以下の小さな凹凸により500nm以下の短波長の光も有効に散乱、利用できる。すなわち、大きな凹凸により長波長の光を散乱し、小さな凹凸表面より短波長の光を散乱することができるため、全体として高い光散乱性を達成することができる。また分光ヘイズ率が550nm以上800nm以下の波長で20%以上である。

[0114] 本実施形態においても、透明電極つき基板は、第1実施形態と同様であり、透明電極つき基板は、大型の凹凸(マクロな凹凸)の山部112の平均の高さHa(平坦部上のミクロの凸部の頂部からの高さの平均値)が、0．4μm以上0．7μm以下であり、0．5μm以上0．6μm以下であることがより好ましい。山部の密度は、基板111面の10μm角あたり15以上50以下となり、この平均ピッチPaは、1．0μm以上3μm以下に相当する。一方、小型の凹凸(ミクロな凹凸)のミクロの多数の凸部の底面径が0.1μm以上0.3μm以下であり、高さ／底面径の比が0.7以上1.2以下である。

[0115] 前記透明電極付き基板におけるこのような表面性状は、例えば、前記第1実施形態で説明した表面形状の解析を行うことにより確認することができる。

[0116] また、このような形状及び構成を有する透明電極付き基板は、基板全体において、550nm以上800nm以下の波長における分光ヘイズ率が20%以上、好ましくは30%以上であることが好ましい。

ここで、「分光ヘイズ率」の定義は、上記第1実施形態において説明したとおりである。

[0117] 以下に、上述した本実施形態の透明電極付き基板の形状及び構成ならびに特性を満たす基板(透明基板)及び酸化物は、それぞれ前記第1実施形態で説明した基板および第1酸化物と同様であるので、これらの詳しい説明は省略する。

[0118] 本実施形態の透明電極付き基板は、大型の凹凸と小型の凹凸が混在することが望ましく、ピッチが0.1μmから1.2μm、高さが0.1μmから1．0μmの凹凸が混在している。ピッチ0.8μm以上の大きな凹凸により800nm以上の長波長の光を拡散、閉じ込めでき、ピッチ0.3μm以下の小さな凹凸により500nm以下の短波長の光も有効

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に散乱、利用できる。また、膜全体のシート抵抗が8Ω／□以上20Ω／□以下であることが好ましく、8Ω／□以上12Ω／□以下であることがより好ましく、550nmにおける透過率(透明性)は、浸液法で測定した場合、80%以上90%以下であることが好ましく、85%以上90%以下であることがより好ましい。

[0119] また、本実施形態の透明電極付き基板を、光電変換装置の透明電極に用いると、基板を経て入射された光は、透明電極により屈折、散乱されて光電変換部に入射し、光電変換部中を長い距離にわたって通過する。その結果、多くの光が光電変換部にて吸収され、光電変換効率が向上する効果を奏するものとなる。特に、太陽電池に用いた場合には、開放電圧及び曲線因子を低下させずに短絡電流を高く維持することが可能となるため、光電変換効率が向上するものとなる。

[0120] 本実施形態の光電変換装置の製造方法により製造される光電変換装置の構成および太陽電池パネルの製造方法は、後述の異相遮断層または異相防止層を設けたこと以外は前記第1実施形態と同様であるので、第1実施形態で用いた図1および図4ないし図7を参照する。前記第1実施形態と共通の部材については同一の参照符号を用いることとし、詳細な説明は省略する。

[0121] 本実施形態の光電変換装置においては、非晶質シリコン系半導体を主として有する光電変換層からなる第1セル層(トップ層)91の透明電極層側表面から裏面電極層側表面に貫通する異相を遮断または防止するために、後述の光電変換装置の製造方法に係る実施形態に示した方法により、第1セル層(トップ層)91中に異相遮断層(図示略)が設けられるか、もしくは、基板1と第1セル層(トップ層)91の間に異相防止層(図示略)が設けられる。

第1セル層(トップ層)91及び結晶質シリコン系半導体を主として有する光電変換層からなる第2セル層(ボトム層)92の間には、透明導電膜からなる中間コンタクト層93を設けても良い(但し、本発明の光電変換装置は、中間コンタクト層93を設けたものに限定されない)。

[0122] 本実施形態の太陽電池パネルの製造方法においては、まず、前記第1実施形態の図4の(a)および(b)と同様の方法を行い、透明電極基板が形成される。

[0123] 次に、製膜した透明電極層2の表面に対してイオン処理を行い、本実施形態の異

相防止層を形成することができる。イオン処理は、例えば真空中でのアルゴンイオン照射によるイオンエッチングとすることができる。イオン処理に用いられる装置としては、フィラメントタイプのイオン源を使用したイオンミリング装置が挙げられる。この装置を用いてイオン処理を行う場合は、例えば容器内を10^{-4}Pa台に真空排気し、アルゴンガスを供給して5×10^{-3}Paの条件で、Arイオンを発生させ、加速電圧1kVでイオン照射してイオン処理を行うことができる。イオンは透明電極付き基板の透明電極層2表面に垂直に照射することが好ましい。照射時間は例えば180sec程度とすることができる。

[0124] 次に、前記第1実施形態の図4の(e)と同様の方法により透明電極膜のレーザーエッチングを行い、次いで異相遮断層または異相防止層を設けたこと以外は図4の(d)と同様の方法を行い、光電変換層3を形成する。

光電変換層3の第1セル層(トップ層)91として、非晶質シリコン薄膜からなるp層膜／i層膜／n層膜を順次形成する。太陽光の入射する側からp層、i層、n層がこの順で積層される。

なお、第1セル層91を製膜する前に、透明電極付き基板を真空容器で10^{-1}Pa以下の圧力とし、ヒータで100℃以上の温度に予備加熱(ベーキング)することが、異相の発生を防ぐために特に好ましい。

[0125] 本実施形態において、第1セル層91のp層は、SiH_4, H_2, CH_4, B_2H_6ガスをRFプラズマで反応生成させた、非晶質のBドープSiC膜であり、膜厚は4nm以上16nm以下とすることが好ましい。

[0126] また本実施形態において、第1セル層91のi層は、標準構成としては非晶質Si膜であり、SiH_4とH_2をRFプラズマで反応生成される。膜厚は100nm以上400nm以下とすることが好ましい。標準の製膜条件として、SiH_4とH_2を1:5の比率で供給して圧力を600Paに制御し、60MHzの高周波0．15W／cm^2で放電して、非晶質のi層を製膜することができる。この標準の製膜条件における製膜速度は、例えば1．1nm／sとすることができる。

[0127] 本実施形態の異相遮断層として、第1セル層91のi層中に、標準製膜条件よりも低パワーで製膜された層(例えば、i層製膜の初期に製膜される初期層、あるいはi層製

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膜の後期に製膜される後期層）を設けてもよい。このような層を製膜する場合は、高周波出力を例えば0．02W／cm^2の低パワーにして、低速で製膜すればよい。製膜速度は例えば0．2nm／s程度である。初期層及び後期層は、例えば60s（膜厚12nm相当）～120s（膜厚24nm相当）で製膜される。初期層または後期層を設けたi層は、プラズマ放電中にパワーを変更することにより、連続膜として形成される。

[0128] また本実施形態において、第1セル層91（トップ層）のn層は、標準構成としては結晶質（結晶成分を含む）のSi膜であり，SiH_4，H_2，PH_3ガスをRFプラズマで反応生成される。このn層単膜のラマン比は2以上であり、膜厚は10nm以上80nm以下とすることが好ましい。標準の製膜条件として、SiH_4とH_2とPH_3を1：80：0．02の比率で供給して圧力を100Paに制御し、基板と電極の間の間隔を20mmとし、60MHzの高周波0．3W／cm^2で放電して、微結晶（結晶とアモルファスが混在する膜質）のn層を製膜することができる。製膜速度は0．2nm／sとすることができる。製膜速度は例えば0．2nm／s程度とすることができる。

[0129] 本実施形態の異相遮断層として非晶質（結晶成分は存在しない）のn層を形成してもよい。この場合は、前記結晶質のn層の前に非晶質のn層が製膜される。この非晶質n層は、SiH_4とH_2とPH_3を1：1：0．05の比率で供給して圧力を20Paに制御し、基板と電極の間の間隔を20mmとし、60MHzの高周波を0．04W／cm^2で放電して製膜される。製膜速度は例えば0．2nm／s程度とすることができる。非晶質Si－n層と微結晶Si－n層を積層するときは、一旦放電を停止して流量／圧力を変更し、安定後再度放電させて行われる。例えば、非晶質Si製膜条件で15nm程度製膜し、さらに標準の結晶質製膜条件で25nm程度製膜すればよい。

[0130] 本実施形態の異相遮断層として、結晶質（結晶成分を含む）のn層を標準製膜条件より高圧で製膜してもよい。この場合は、例えば、SiH_4とH_2とPH_3を1：80：0．02の比率で供給して、圧力を200Paに制御し、基板と電極の間の間隔を標準条件の1／2である10mmに狭くして、60MHzの高周波を出力0．1W／cm^2で放電して、微結晶Si（結晶とアモルファスが混在する膜質）のn層を製膜することができる。

[0131] 本実施形態において，前記p層膜とi層膜の間には界面特性の向上のためにバッファー層（図示略）を設けてもよい。バッファー層として、バンドギャップが中間の物質を

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挿入することにより、p層(SIC膜)とi層(Si膜)の界面でのバンド不整合を抑制することができる。

本実施形態において、p層の製膜ガス(SiH_4、H_2、CH_4、B_2H_6)に対し、i層ではSiH_4及びH_2しか用いないため、ドーパント(B_2H_6)濃度及びバンド調整のためのCH_4濃度を調整する。具体的には、p層製膜室において、B_2H_6ガスの供給を停止し、B_2H_6の供給は壁面吸着量のみとし、CH_4ガスの供給量をp層に対し1/10～1/3に調整することで0.02～0.1μmの膜厚のバッファー層を形成した。これにより、p層及びi層と原子拡散が進行した結果、膜厚方向の炭素含有率及びバンドエネルギー構造は滑らかに変化する状態となり、p層とi層との界面特性が向上されることとなる。

[0132] 次に、第1セル層(トップ層)91の上に、前記第1実施形態と同様の方法、製膜条件により、微結晶シリコン薄膜からなる微結晶p層膜／微結晶i層膜／微結晶n層膜を順次製膜し、前記第1実施形態と同様の第2セル層(ボトム層)92を形成する。

[0133] 前記第1実施形態と同様に、第1セル層(トップ層)91と第2セル層(ボトム層)92の間に電流整合性を取るために半反射膜となることを目的に、中間コンタクト層93として、膜厚0nm以上90nm以下、より好ましくは5nm以上50nm以下のZnO系膜(例えばGZO(Gaドープ ZnO)膜)をスパッタリング装置により製膜して設けても良い。この中間コンタクト層93は、ZnO単膜での光吸収率がλ＝450nm以上1000nm以下の範囲で1%未満であることが好ましい。

[0134] 第2セル層92を形成した後、第1実施形態における図4の(e)から図7の(b)と同様の方法により太陽電池パネル50が完成する。次いで第1実施形態における図7の(c)および(d)と同様の方法により、発電検査および所定の性能試験ならびに外観検査をはじめ所定の性能検査を行う。

[0135] 上記実施形態では太陽電池として、トップセルとして非晶質シリコン系光電変換層を有し、ボトムセルとして結晶質(微結晶)シリコン系光電変換層を有するタンデム型太陽電池を用いたものについて説明したが、本発明は、この例に限定されるものではない。

例えば、光電変換層として非晶質シリコン系光電変換層のみを有するシングル型太陽電池や、前記トップセルと前記ボトムセルに加えてさらに1層もしくは2層以上の

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別の光電変換層を設けた多接合型太陽電池のような他の種類の薄膜太陽電池にも同様に適用可能である。

[0136] [実施例、参考例及び比較例]

参考例1:

透明電極付き基板として、微細な凹凸のみのものを用いた。微細な凹凸の凸部の高さは0.1μm以上0.2μm以下、ピッチは0.1μm以上0.3μm以下、凸部の高さと底面径の比は0.7～1.0、波長550nmの分光ヘイズ率は20%、800nmの分光ヘイズ率は3%であった。透明電極付き基板が異なる以外は、本発明の前記実施形態における標準の製膜条件に従って、タンデム型太陽電池を作製した。

[0137] 透明電極付き基板上に形成した各層において、トップセルp層は膜厚8nm、トップセルn層は膜厚40nm、ボトムセルp層は膜厚30nm、ボトムセルn層は膜厚30nm、裏面電極のZnO層は膜厚80nm、裏面電極のAg層は膜厚300nmで、各参考例、比較例及び実施例において共通とした。本例のトップセルi層、トップセルn層の膜厚及び製膜条件は、表3に示す通りとし、中間コンタクト層は形成しなかった。

[0138] なお、表3に記載した各参考例、比較例及び実施例の「製膜条件」とは、以下の通りである。

トップセルi層の標準製膜条件: SiH_4とH_2を1:5の比率で供給して、圧力を600Paに制御し、60MHzの高周波を出力0.15W／cm^2で放電して、非晶質i層を製膜した。製膜速度は1.1nm／sとした。

[0139] トップセルi層の初期層または後期層の低速製膜条件: 標準条件と高周波出力のみを変更し、0.02W／cm^2とした。製膜速度は0.2nm／sとした。標準製膜条件による膜との積層は、プラズマ放電中にパワーを変更することにより、連続膜とした。

[0140] トップセルn層の標準製膜条件: SiH_4とH_2とPH_3を1:80:0.02の比率で供給して、圧力を100Paに制御し、基板と電極の間の間隔を7mmとし、60MHzの高周波を出力0.3W／cm^2で放電して、微結晶(結晶と非晶質が混在する膜質)のn層を製膜した。製膜速度は0.2nm／sとした。

[0141] トップセルn層の非晶質Si製膜条件: SiH_4とH_2とPH_3を1:1:0.05の比率で供給して、圧力を20Paに制御し、基板と電極の間の間隔を7mmとし、60MHzの高周波

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を出力0．04W／cm^{3}で放電して、非晶質Si(結晶成分は存在しない)のn層を製膜した。製膜速度は0．2nm／sとした。非晶質Si－n層と微結晶Si－n層を積層するときは、一旦放電を停止して流量／圧力を変更し、安定後再度放電させた。

[0142] トップセルn層の高圧製膜条件：SiH_4とH_2とPH_3を1:80:0．02の比率で供給して、圧力を200Paに制御し、基板と電極の間の間隔を標準条件の1／2である10mmに狭くして、60MHzの高周波を出力0．3W／cm^{3}で放電して、微結晶Si(結晶と非晶質が混在する膜質)のn層を製膜した。

[0143] 参考例1で得られた太陽電池の電池性能を表4に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を2μmに設定した本例の太陽電池の発電効率(初期値)は12%だった。

なお、表4において、電池性能評価項目であるIsc、Voc、FF、Effは、それぞれ短絡電流、開放電圧、形状因子、発電効率(初期値)を表す。また、表4に示す参考例、比較例及び実施例において、電池性能評価結果は、参考例1を1とした相対値で記載する。本結果は、劣化前の初期値を記載したが、劣化率は本試験の範囲内では同等と考えられ、相対値で表すなら劣化後も同等である。

[0144] 参考例2：

トップセルi層、ボトムセルi層を表3に示す膜厚で形成した以外は前記参考例1と同様の方法に従って、タンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表4に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を1．5μmに設定した本例の太陽電池の発電効率は10．8%に低下した。これは、発電電流が大幅に低下したためであり、参考例で用いた基板ではボトムセル膜厚が2μmなければ所望の電流が得られないということが分かった。

[0145] 比較例4：

本発明の前記実施形態における標準の製膜条件に従って、タンデム型太陽電池を作製した。透明電極付き基板として、実施例6と同じく大小の凹凸が混在する基板を適用した。本例のトップセルi層、トップセルn層の膜厚及び製膜条件は、表3に示す通りとし、中間コンタクト層は形成しなかった。すなわち、トップセルi層は製膜速度1．

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1nm／sで300nmの膜厚に、トップセルn層は結晶と非晶質が混在する微結晶となる条件で40nmの膜厚に製膜した。ボトムセルi層の膜厚は1．5μmとした。

[0146] 得られた太陽電池の電池性能を表4に示す。表4に示したように、本例の太陽電池は、電流は増大したものの、開放電圧と形状因子が低下して、発電効率初期値は参考例1のボトムセルi層膜厚が2μmの場合より低下していた。

[0147] 比較例4の太陽電池において開放電圧と形状因子が低下した原因を調査検討した。図10に大小の凹凸が混在する透明電極付き基板を用いて作製したタンデム型太陽電池の断面の透過型電子顕微鏡写真を示す。この電子顕微鏡写真において、透明電極の谷の部分（点線で囲んだ部分）でトップセルを上下に貫通する線が見える。これは、下地の隣接する面に製膜・成長する膜成長相間の不連続な境界が線状に見えるもので、異相と呼んでおり、キャリア再結合中心が集中すると考えられ、電流リーク箇所に相当する。この異相が生じた場合に開放電圧と形状因子が低下していた。従って、本発明者らは、この異相を抑制すること、または完全に抑制はできなくても透明電極から中間コンタクト層又はボトムセルに至るまでトップセルを貫通する異相を遮断できれば、開放電圧低下、形状因子低下を抑制できると考えた。

[0148] 実施例6～実施例9:

トップセルi層、トップセルn層の膜厚及び製膜条件を表3に示す通りとした以外は前記比較例4と同様の方法に従って、実施例6～実施例9のタンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表4に示す。

[0149] 実施例6においては、トップセルの非晶質Si－i層を製膜初期（p層との界面）のみ低パワーで製膜することにより、開放電圧低下、形状因子低下を抑制し、太陽電池性能を向上できた。これは、非晶質Si－i層の初期層によってトップセルを貫通する異相が遮断され、電流リークを抑制することができたためと考えられる。ボトムセルが膜厚1．5μmという薄膜で発電効率初期値13.0%という高効率が得られたことは、生産性と効率向上の両方で非常に大きな成果である。

[0150] 実施例7においては、トップセルの非晶質Si－i層を製膜後期（n層との界面）のみ低パワーで製膜することにより、開放電圧低下、形状因子低下を抑制し、太陽電池

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性能を向上できた。これは、非晶質Si－i層の後期層によってトップセルを貫通する異相が遮断され、電流リークを抑制することができたためと考えられる。この実施例7でも、ボトムセルが膜厚1．5μmという薄膜で発電効率初期値13.0%という高効率が得られたことは、生産性と効率向上の両方で非常に大きな成果である。

[0151] 実施例8においては、トップセルn層の製膜後期のみを標準製膜条件により製膜して結晶質とし、製膜初期の層を非晶質にすることで、開放電圧低下、形状因子低下を抑制し、太陽電池性能を向上できた。これは、トップセルn層において非晶質とした初期層がi層との界面で異相を埋めるため、トップセルを貫通する異相が遮断され、電流リークを抑制することができたためと推察される。ボトムセル膜厚1.5μmの薄膜で発電効率初期値13.2%が得られたのは、実施例6、実施例7と同様の異相遮断効果と、更にn層による界面改善効果が得られたためである。

[0152] 実施例9においては、トップセルn層を200Paの高圧で製膜して微結晶膜を形成することにより、開放電圧低下、形状因子低下を抑制し、太陽電池性能を向上できた。なお、実施例9において、トップセルn層の製膜の際の圧力を400Paとした場合も同様の効果が得られた。これは、高圧で製膜することによりトップセルn層がi層との界面の谷の部分に付きやすくなり、これによってトップセルを貫通する異相が遮断され、電流リークを抑制することができたためと考えられる。

[0153] [表3]

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	トップセルi層の製膜条件と膜厚	トップセルn層の製膜条件と膜厚
参考例1	標準製膜条件で300nm	標準製膜条件で2μm
参考例2	標準製膜条件で300nm	標準製膜条件で1.5μm
比較例4	標準製膜条件で300nm	標準製膜条件(結晶質)で40nm
実施例6	初期層：低速製膜条件で24nm(120s)；続けて標準製膜条件で残り276nm	標準製膜条件(結晶質)で40nm
実施例7	標準製膜条件で276nm；さらに後期層として低速製膜条件で24nm(120s)	標準製膜条件(結晶質)で40nm
実施例8	標準製膜条件で300nm	非晶質Si製膜条件で15nm；さらに標準製膜条件で25nm
実施例9	標準製膜条件で300nm	高圧製膜条件(結晶質)で40nm

[0154] 実施例10:

透明電極付き基板の透明電極表面に対してイオン処理を行った以外は、前記比較例4と同様の方法に従って、実施例10のタンデム型太陽電池を作製した。

イオン処理は、真空中でのアルゴンイオン照射によるイオンエッチングであり、装置としては、フィラメントタイプのイオン源を使用したイオンミリング装置を用いた。容器内を10^{-4}Pa台に真空排気し、アルゴンガスを供給して5×10^{-3}Paの条件で、Arイオンを発生させ、加速電圧1kVでイオン照射してイオン処理を行った。イオンは透明電極付き基板の透明電極表面に垂直に照射し、照射時間は180secとした。図8は、イオン処理前における透明電極付き基板の透明電極表面の電子顕微鏡写真(倍率5万倍)であり、図9は、イオン処理後における透明電極付き基板の透明電極表面の電子顕微鏡写真(倍率5万倍)である。

[0155] 得られた太陽電池の電池性能を表4に示す。なお、表4において、電池性能評価項目であるIsc、Voc、FF、Effは、それぞれ短絡電流、開放電圧、形状因子、発電効率を表す。Iscの(a－Si／c－Si)は、分光感度から求めたa－Si(非晶質)トップセルのIsc及びc－Si(結晶系)ボトムセルのIscである。

実施例10においては、前記イオン処理により、開放電圧低下、形状因子低下を抑

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制し、太陽電池性能を向上できた。これはイオン処理によって基板の凹形状が円滑になり、トップセルにおける異相の形成が抑制されたため、電流リークを抑制することができたためと考えられる。

実施例1～10においては、ボトムセルi層製膜条件は固定であり、ボトムセルn層製膜後のラマン比は表1に示すとおり、5.0～7.0の間にあった。

[0156] 実施例11；

ボトムセルi層のH_2/SiH_4希釈率比を表5に示すように変えた以外は、実施例1と同様の方法に従って実施例11(1)～実施例11(6)のタンデム型太陽電池を作製し、ボトムセルのn層製膜後のラマン比と太陽電池特性の関係を調べた。その結果を図12に示す。なお、表5、及び図12において、H_2希釈率比、及び電池性能結果は、比較例1を1とした場合の相対値である。本結果は、劣化前の初期値を記載したが、劣化率は本試験の範囲内では同等と考えられ、相対値で表すなら劣化後も同等である。

表5及び図12からわかるように、n層製膜後のラマン比でみて3.0以上8.0以下のとき、比較例1よりも太陽電池性能が向上している。これは、ラマン比が3.0より低下するとVocが向上する一方で、Iscが著しく低下していることから、非晶質成分が多すぎて抵抗損失が生じたと推定される。ラマン比が8.0より増大すると、VocとFFが大きく低下していることより電流リークによる電圧損失が生じたと考えられ、結晶粒界の電流リークが想定される。第2セル層において、適度な非晶質相が存在することにより、結晶質シリコンの粒界に存在する欠陥を不活性にし、これにより、Iscの低下を抑制することに寄与しているものと考えられる。

また、図12において、H_2希釈率比0．9でEffの上昇が緩和し、H_2希釈率比1．1でEffが低下している。H_2希釈率比0．9以上1．1以下でのEff値は、実施例11(3)～実施例11(5)に示すように、比較例1に対し1.1倍以上の性能を得ることができた。したがって、ラマン比は、H_2希釈率比と電池性能との相関関係からみて、実験的に5.0以上7.5以下が最適値となる。

[0157] [表4]

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	電池性能			
	Isc (a-Si/c-Si)	Voc	FF	Eff
参考例1	1 (1/1)	1	1	1
参考例2	0.89(1/0.89)	1	1	0.89
比較例4	1.10(1/1.10)	0.95	0.92	0.97
実施例6	1.10(1/1.10)	0.99	0.99	1.08
実施例7	1.10(1/1.10)	0.99	0.99	1.08
実施例8	1.10(1/1.10)	1.00	1.00	1.10
実施例9	1.10(1/1.10)	0.99	0.98	1.07
実施例10	1.03(1/1.03)	1.01	1.01	1.05

[0158] [表5]

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No	H2希釈率比	ラマン比	電池性能				
			(タンデム) Isc	(c-Si) Isc	Voc	FF	Eff
実施例11(1)	0.8	2	0.98	0.98	1.03	0.95	0.96
実施例11(2)	0.8	3	1.03	1.03	1.01	1.00	1.04
実施例11(3)	0.9	5	1.11	1.11	1.00	0.99	1.10
実施例11(4)	1.0	6.5	1.15	1.15	0.99	0.97	1.11
実施例11(5)	1.1	7.5	1.17	1.17	0.98	0.96	1.10
実施例11(6)	1.2	10	1.15	1.15	0.94	0.89	0.96
比較例1	1.0	6.5	1.00	1.00	1.00	1.00	1.00(12%)

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[0159] 以上、実施例6から実施例11によれば、分光ヘイズ率を高めた透明電極付き基板を適用しても開放電圧と形状因子の低下を抑制でき、薄いボトムセルで、高効率と高生産性を兼ね備えたタンデム太陽電池を作製可能となった。

なお、トップセル(非晶質Si層)全体を低パワーで製膜すると製膜速度が著しく低下するため、生産性が悪化する。しかし、上記実施例6、実施例7のように初期あるいは後期の20%程度の膜厚を低速で作製するだけであれば、生産性の悪化を極力抑えられて、高い生産効率で太陽電池を製造できる。また、実施例9のようにn層の製膜条件を改善した場合は、生産性の悪化はまったくなく、高い生産効率で太陽電池を製造できる。

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請求の範囲

[1] 透明絶縁性の基板上に透明電極層を設けてなる透明電極付き基板と、該透明電極付き基板の透明電極層側に順次形成された、結晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも有してなる光電変換装置であって、

前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上であり、

前記結晶質シリコン系半導体を主として有する光電変換層の膜厚が1.2μm以上2μm以下、かつラマン比が3.0以上8.0以下である光電変換装置。

[2] 前記透明電極付き基板と前記結晶質シリコン系半導体を主として有する光電変換層との間に、非晶質シリコン系半導体を主として有する光電変換層を有する請求項1に記載の光電変換装置。

[3] 前記非晶質シリコン系半導体を主として有する光電変換層と前記結晶質シリコン系半導体を主として有する光電変換層との間に中間コンタクト層を有する請求項2に記載の光電変換装置。

[4] 前記透明電極付き基板の透明電極層表面が、複数の山部と複数の平坦部とで構成され、該山部及び該平坦部の表面がミクロの多数の凸部を連続して有してなり、

前記山部の前記基板面垂直方向における高さが0.4μm以上0.7μm以下であり、

基板面10μm角における前記山部の数が15以上50以下であり、

前記ミクロの多数の凸部の底面径が0.1μm以上0.3μm以下であり、高さ／底面径の比が0.7以上1.2以下である請求項1から請求項3のいずれか1項に記載の光電変換装置。

[5] 透明絶縁性の基板上に透明電極層を形成して透明電極付き基板を作製し、

該透明電極付き基板の透明電極層側に非晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも順次形成する光電変換装置の製造方法であって、

前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘ

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イズ率が550nm以上800nm以下の波長で20%以上であり、

前記非晶質シリコン系半導体を主として有する光電変換層中に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相を遮断する異相遮断層を形成する光電変換装置の製造方法。

[6] 前記非晶質シリコン系半導体を主として有する光電変換層の形成においてp層、i層、n層を順次形成し、

前記i層の形成において該i層の他の部分より低速で製膜することにより前記異相遮断層を形成する、請求項5に記載の光電変換装置の製造方法。

[7] 前記非晶質シリコン系半導体を主として有する光電変換層の形成においてp層、i層、n層を順次形成し、

前記n層の形成において少なくともその一部に非晶質の層を形成することにより前記異相遮断層を形成する、請求項5に記載の光電変換装置の製造方法。

[8] 前記非晶質シリコン系半導体を主として有する光電変換層の形成においてp層、i層、n層を順次形成し、

前記n層の形成において少なくともその一部を200Pa以上の圧力下で製膜することにより前記異相遮断層を形成する、請求項5に記載の光電変換装置の製造方法。

[9] 透明絶縁性の基板上に透明電極層を形成して透明電極付き基板を作製し、

該透明電極付き基板の透明電極層側に非晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも順次形成する光電変換装置の製造方法であって、

前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上であり、

前記透明電極層の形成と前記光電変換層形成の間に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相の形成を防止する異相防止層を形成する光電変換装置の製造方法。

[10] 前記透明電極層の凸部を円滑化して前記異相防止層を形成する、請求項9に記載の光電変換装置の製造方法。

[11] 前記透明電極層表面にイオン処理を施して前記異相防止層を形成する、請求項9

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または請求項10に記載の光電変換装置の製造方法。

[12] 前記非晶質シリコン系半導体を主として有する光電変換層と前記裏面電極の間に、結晶質シリコン系半導体を主として有する光電変換層を形成する請求項5から請求項11のいずれか1項に記載の光電変換装置の製造方法。

[13] 透明絶縁性の基板上に透明電極層を設けてなる透明電極付き基板と、該透明電極付き基板の透明電極層側に順次形成された、非晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも有し、

前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上である光電変換装置であって、

前記非晶質シリコン系半導体を主として有する光電変換層中に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相を遮断する異相遮断層を設けた光電変換装置。

[14] 前記非晶質シリコン系半導体を主として有する光電変換層において、p層、i層、n層が順次形成され、

前記非晶質シリコン系半導体を主として有する光電変換層のn層が非晶質シリコン系半導体を主として有する層と、結晶質シリコン系半導体を主として有する層で形成される請求項2又は13に記載の光電変換装置。

[15] 前記非晶質シリコン系半導体を主として有する光電変換層のp層とi層との間にバッファー層を設けた請求項2、13又は14に記載の光電変換装置。

[16] 前記非晶質シリコン系半導体を主として有する光電変換層と前記裏面電極層との間に結晶質シリコン系半導体を主として有する光電変換層を有する請求項13に記載の光電変換装置。

[17] 前記結晶質シリコン系半導体を主として有する光電変換層の膜厚が1.2μm以上2μm以下、かつラマン比が3.0以上8.0以下である請求項16に記載の光電変換装置。

[18] 前記非晶質シリコン系半導体を主として有する光電変換層と前記裏面電極の間に、結晶質シリコン系半導体、結晶質もしくは非晶質シリコンゲルマニウム系半導体を

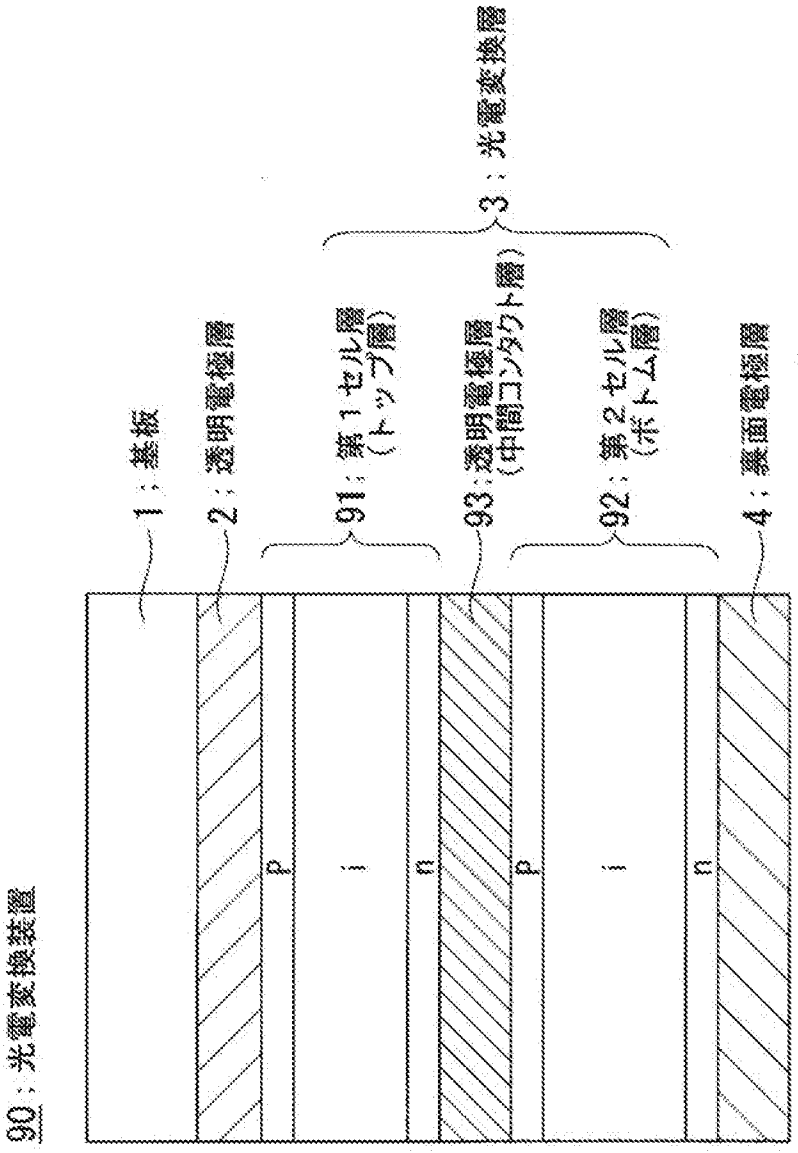
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主として有する光電変換層を有する請求項13に記載の光電変換装置。

[19] 前記非晶質シリコン系半導体を主として有する光電変換層と前記裏面電極の間に、結晶質もしくは非晶質シリコン系半導体、結晶質もしくは非晶質シリコンゲルマニウム系半導体を主として有する光電変換層を複数有する請求項13に記載の光電変換装置。

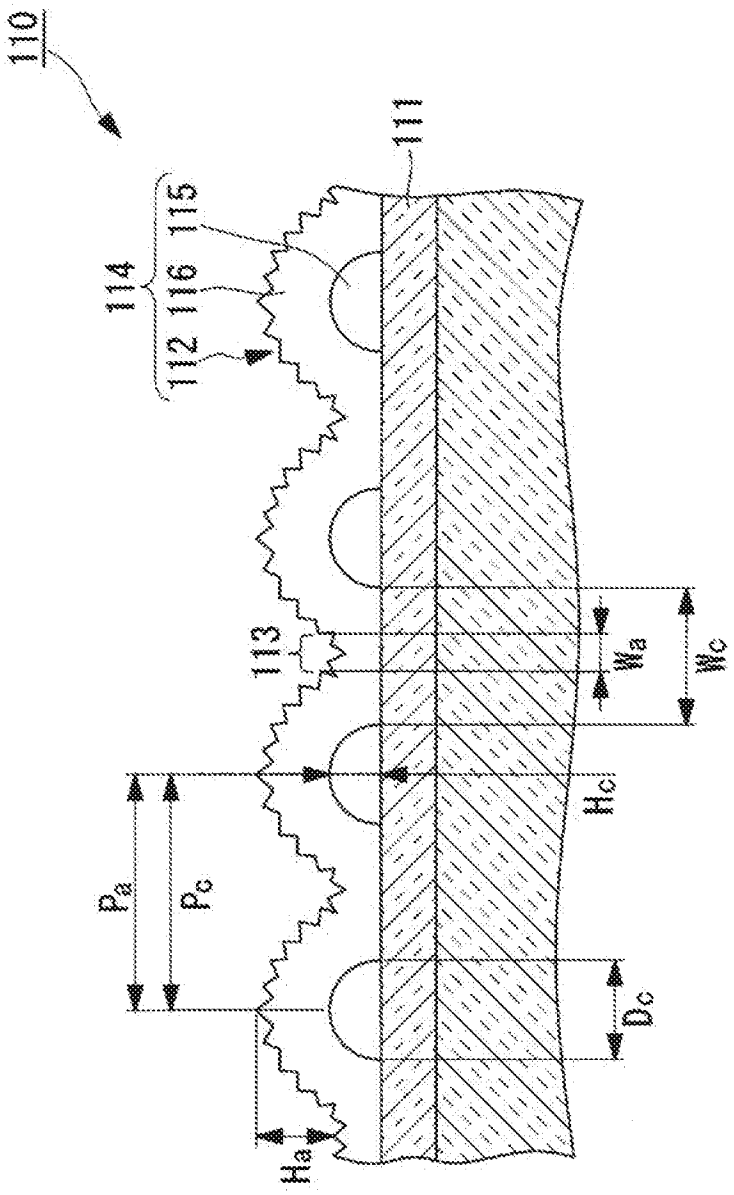
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[図1]

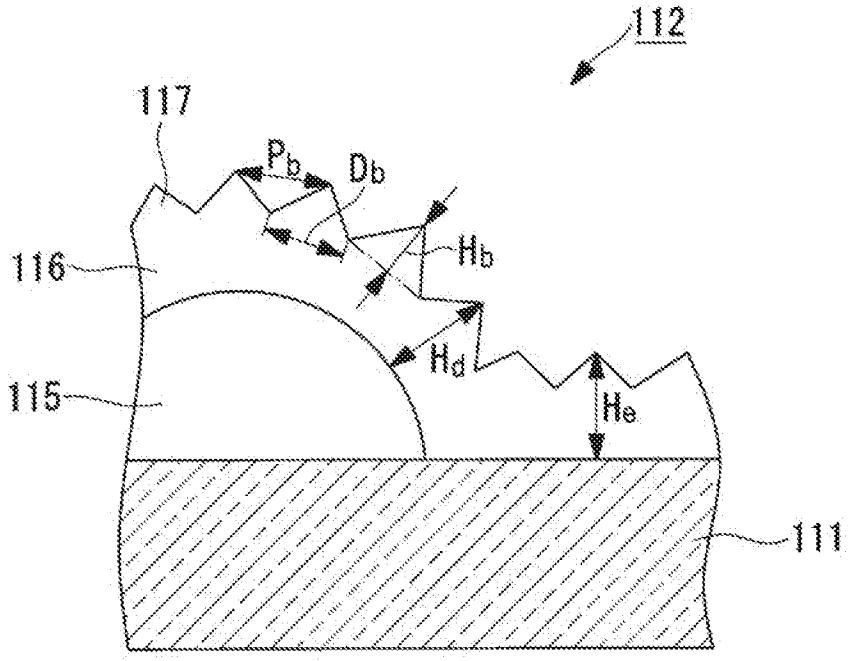


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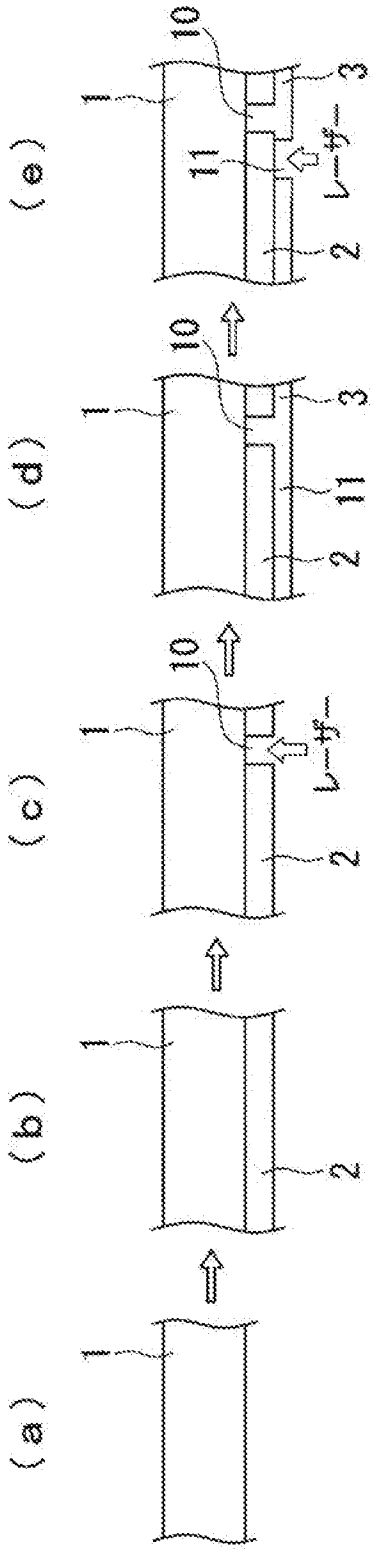
[図2]



[図3]

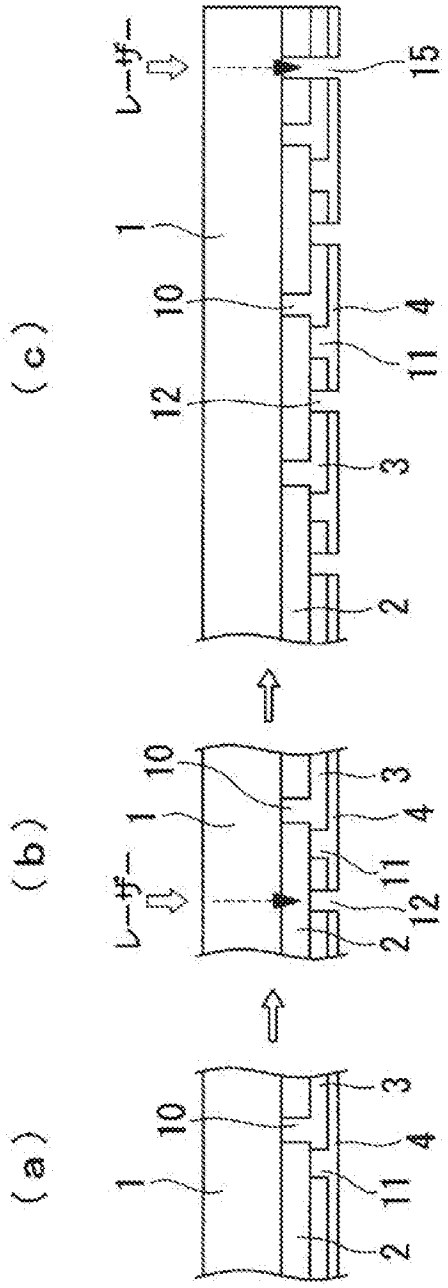


[図4]



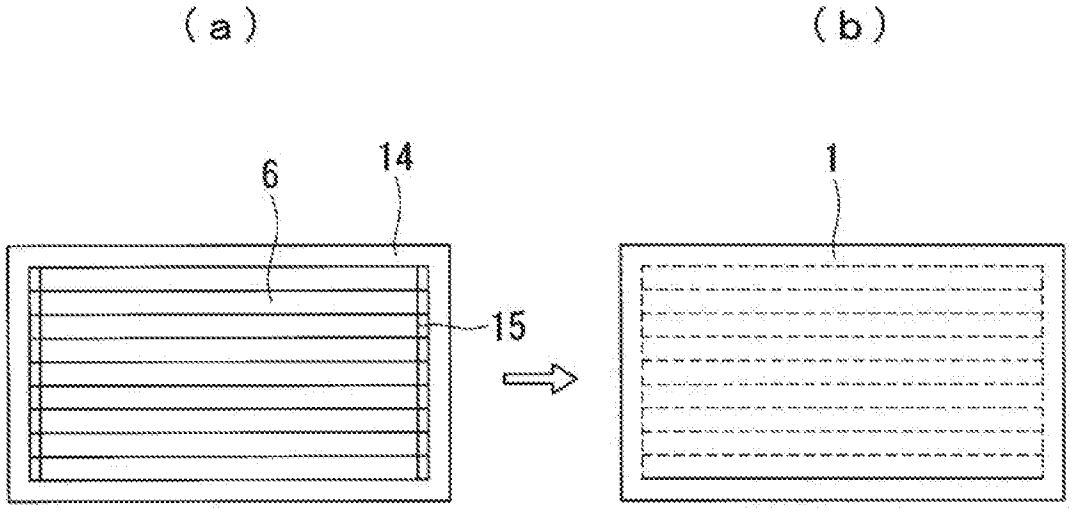
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[図6]



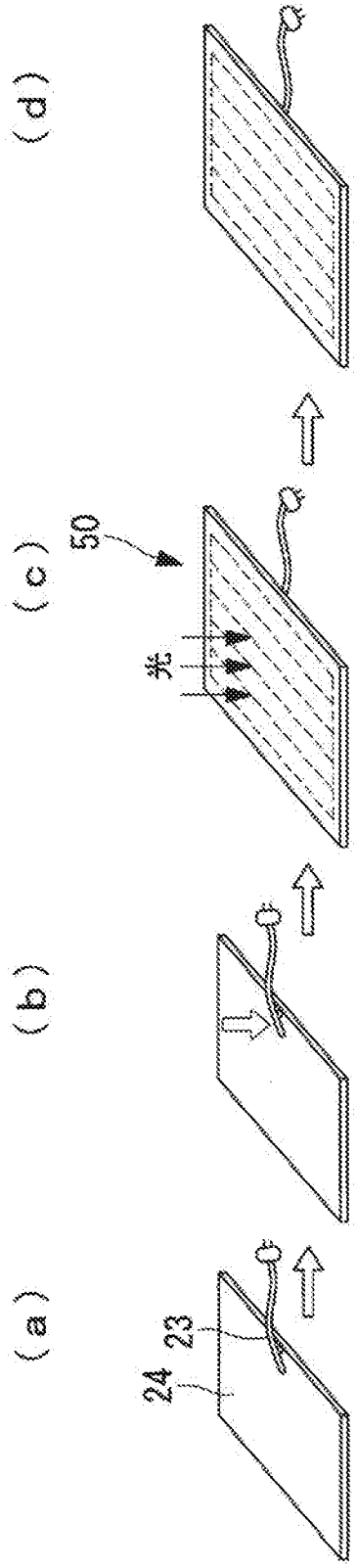
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[図6]



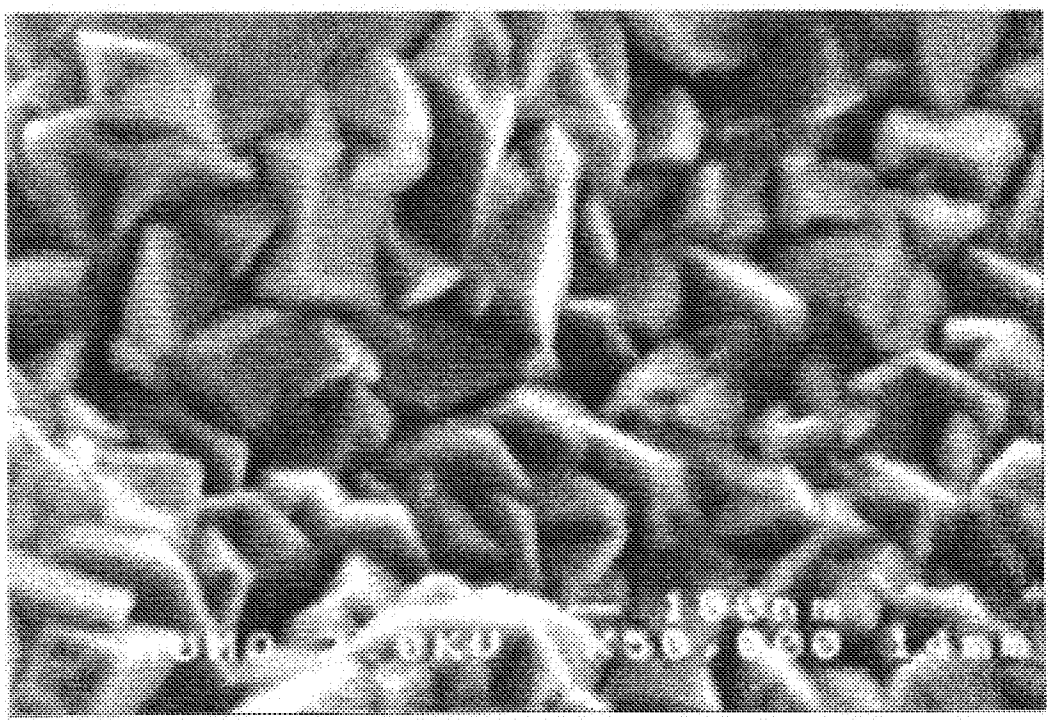
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[図7]

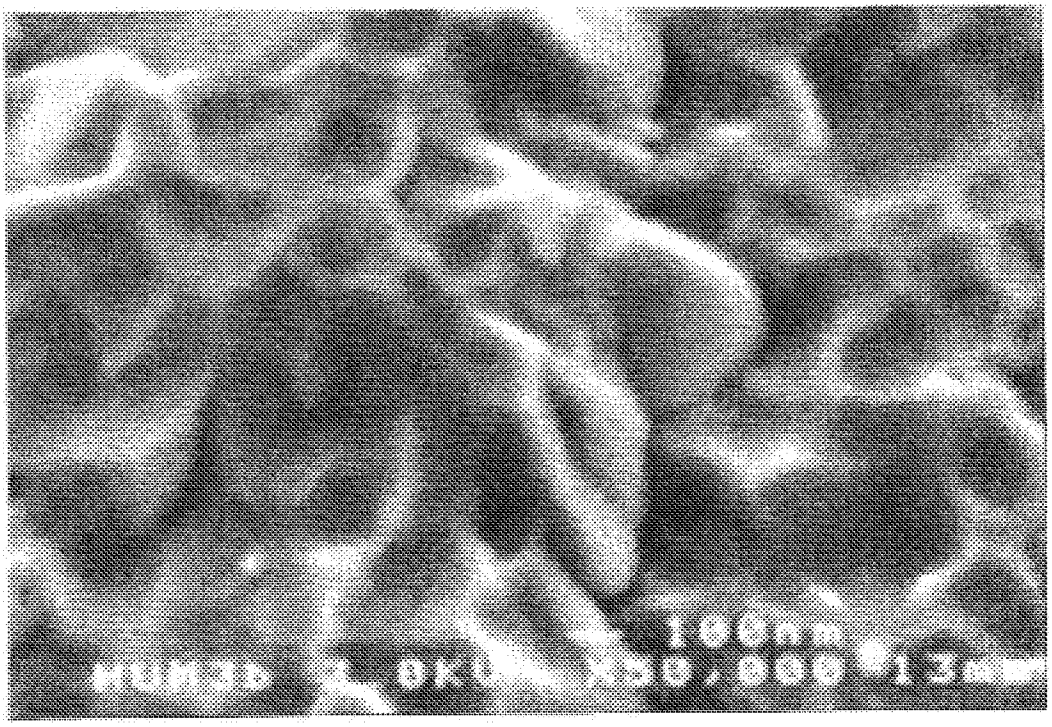


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[図8]

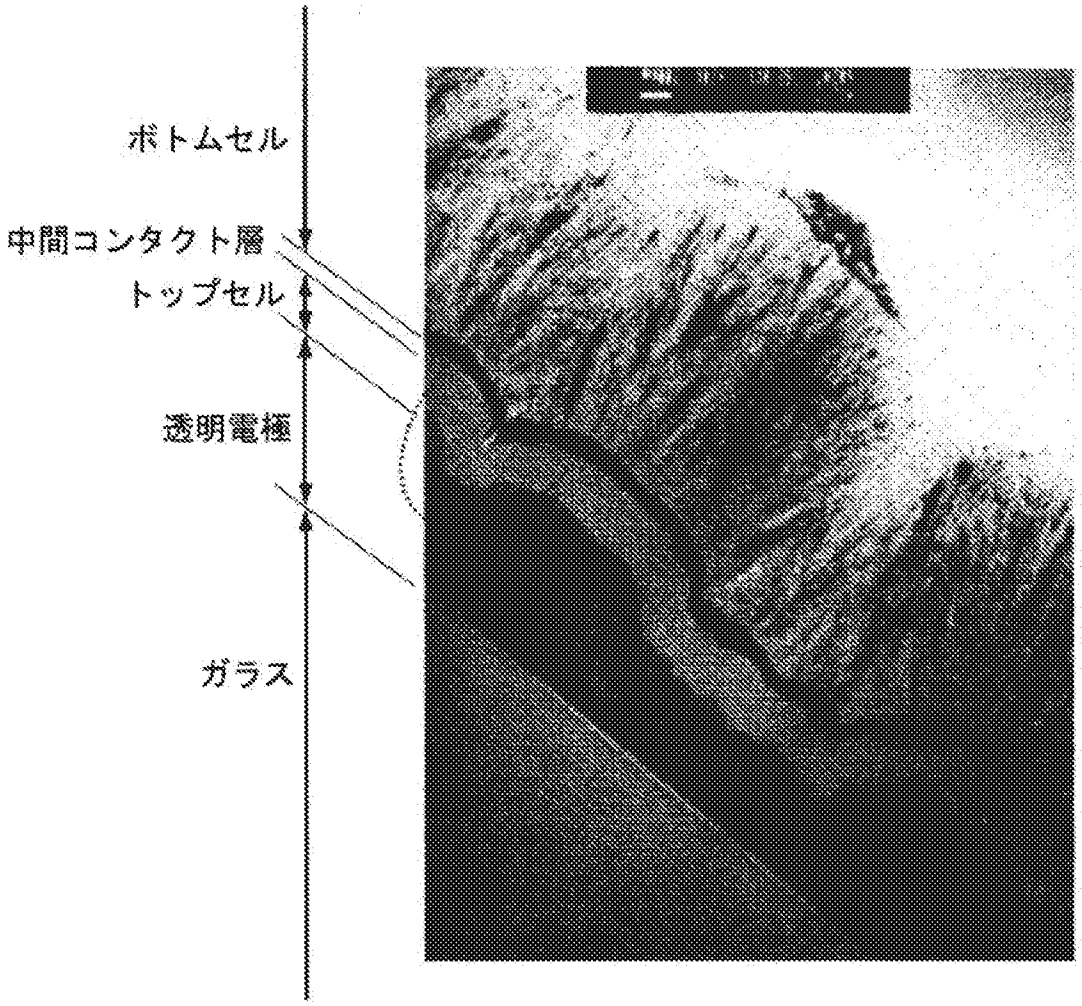


[図9]



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[図10]

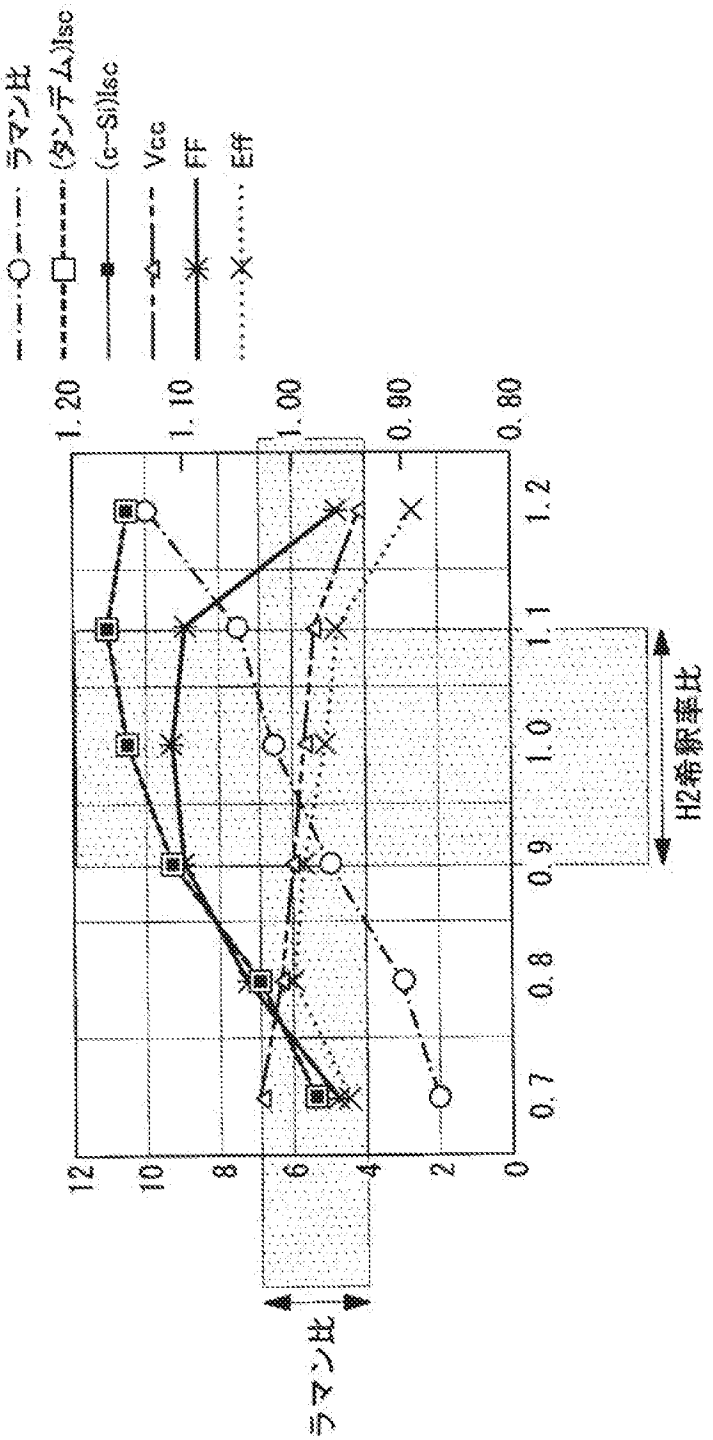


[図11]



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[図12]


ラマン比
(タンデムJsc
(c-Si)Isc
Vcc
FF
Eff
1.20
1.10
1.00
0.90
0.80
1.2
1.1
1.0
0.9
0.8
0.7
H2希釈率比
12
10
8
6
4
2
0
ラマン比

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2007/065386

A. CLASSIFICATION OF SUBJECT MATTER
H01L31/04(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L31/04

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Jitsuyo Shinan Toroku Koho	1996-2007
Kokai Jitsuyo Shinan Koho	1971-2007	Toroku Jitsuyo Shinan Koho	1994-2007

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2005-347490 A (Asahi Glass Co., Ltd.), 15 December, 2005 (15.12.05), Full text; all drawings (Family: none)	1-4,14,15
Y	JP 2002-26348 A (Mitsubishi Heavy Industries, Ltd.), 25 January, 2002 (25.01.02), Par. No. [0036] (Family: none)	1-4,14,15
Y	JP 2006-216921 A (Mitsubishi Heavy Industries, Ltd.), 17 August, 2006 (17.08.06), Par. No. [0044]; Fig. 5 (Family: none)	1-4,14,15

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search 30 October, 2007 (30.10.07)	Date of mailing of the international search report 13 November, 2007 (13.11.07)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (April 2007)

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2007/065386

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2007-5345 A (Mitsubishi Heavy Industries, Ltd.), 11 January, 2007 (11.01.07), Par. No. [0041]; Fig. 15 (Family: none)	1-4,14,15

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2007/065386

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
A matter common to the inventions in claims 1-19 is "a photoelectric converter comprising a substrate with a transparent electrode where a transparent electrode layer is provided on a transparent insulating substrate, and at least a photoelectric conversion layer principally comprising a silicon based semiconductor and a backside electrode layer that are formed sequentially on the transparent electrode layer side of the substrate with a transparent electrode, wherein the substrate with a transparent electrode has a surface shape where large and small protrusions and recesses coexist and spectral haze rate is 20% or above at the wavelength of 550-800 nm.
(Continued to extra sheet.)

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.: 1-4, 14, 15

Remark on Protest

the

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

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Continuation of Box No.III of continuation of first sheet(2)

However, our search has found the above "photoelectric converter" is disclosed in Japanese Laid-open No. 2005-347490, and therefore it is not clearly novel. Consequently the common matter is not a special technical feature within the meaning of PCT Rule 13.2, second sentence, because the above "photoelectric converter" makes no contribution over the prior art.

Therefore, there is no matter common to all the inventions in claims 1-19 as a special technical feature, and there exists no other common matter to be considered to be a special technical feature within the meaning of PCT Rule 13.2, second sentence, therefore no technical relationship within the meaning of PCT Rule 13 can be found among those different inventions.

Accordingly, the inventions in claims 1-19 do not fulfill the requirement of unity of invention.

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国際調査報告	国際出願番号 PCT／JP2007／066386

A. 発明の属する分野の分類（国際特許分類（IPC））

Int.Cl. H01L31/04(2006.01)i

B. 調査を行った分野

調査を行った最小限資料（国際特許分類（IPC））

Int.Cl. H01L31/04

最小限資料以外の資料で調査を行った分野に含まれるもの

日本国実用新案公報	1922－1996年
日本国公開実用新案公報	1971－2007年
日本国実用新案登録公報	1996－2007年
日本国登録実用新案公報	1994－2007年

国際調査で使用した電子データベース（データベースの名称、調査に使用した用語）

C. 関連すると認められる文献

引用文献のカテゴリー＊	引用文献名 及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
Y	JP 2005-347490 A(旭硝子株式会社), 2005.12.15, 全文, 全図 (ファミリーなし)	1-4, 14, 15
Y	JP 2002-26948 A(三菱重工業株式会社), 2002.01.25, [0036] (ファミリーなし)	1-4, 14, 15
Y	JP 2006-216921 A(三菱重工業株式会社), 2006.08.17, [0044], 図5 (ファミリーなし)	1-4, 14, 15

☑ C欄の続きにも文献が列挙されている。　　☐ パテントファミリーに関する別紙を参照。

＊ 引用文献のカテゴリー
「A」特に関連のある文献ではなく、一般的技術水準を示すもの
「E」国際出願日前の出願または特許であるが、国際出願日以後に公表されたもの
「L」優先権主張に疑義を提起する文献又は他の文献の発行日若しくは他の特別な理由を確立するために引用する文献（理由を付す）
「O」口頭による開示、使用、展示等に言及する文献
「P」国際出願日前で、かつ優先権の主張の基礎となる出願の日の後に公表された文献
「T」国際出願日又は優先日後に公表された文献であって出願と矛盾するものではなく、発明の原理又は理論の理解のために引用するもの
「X」特に関連のある文献であって、当該文献のみで発明の新規性又は進歩性がないと考えられるもの
「Y」特に関連のある文献であって、当該文献と他の1以上の文献との、当業者にとって自明である組合せによって進歩性がないと考えられるもの
「&」同一パテントファミリー文献

国際調査を完了した日	国際調査報告の発送日
30．10．2007	13．11．2007

国際調査機関の名称及びあて先	特許庁審査官（権限のある職員）	2K	9010
日本国特許庁（ISA／JP） 郵便番号100－8915 東京都千代田区霞が関三丁目4番3号	吉野 三寛		
	電話番号 03－3581－1101 内線 3255		

様式PCT／ISA／210（第2ページ）（2007年4月）

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Ｃ（続き）．　関連すると認められる文献

引用文献のカテゴリー＊	引用文献名　及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
Y	JP 2007-6345 A(三菱重工業株式会社), 2007.01.11, [0041], 図 15 (ファミリーなし)	1-4, 14, 15

SAMSUNG EX. 1002 - 929/2862

国際調査報告

国際出願番号 PCT/JP2007/065386

第II欄 請求の範囲の一部の調査ができないときの意見（第1ページの2の続き）

法第8条第3項（PCT17条(2)(a)）の規定により、この国際調査報告は次の理由により請求の範囲の一部について作成しなかった。

1. ☐ 請求の範囲＿＿＿＿＿＿＿＿ は、この国際調査機関が調査をすることを要しない対象に係るものである。
つまり、

2. ☐ 請求の範囲＿＿＿＿＿＿＿＿ は、有意義な国際調査をすることができる程度まで所定の要件を満たしていない国際出願の部分に係るものである。つまり、

3. ☐ 請求の範囲＿＿＿＿＿＿＿＿ は、従属請求の範囲であってPCT規則6.4(a)の第2文及び第3文の規定に従って記載されていない。

第III欄 発明の単一性が欠如しているときの意見（第1ページの3の続き）

次に述べるようにこの国際出願に二以上の発明があるとこの国際調査機関は認めた。

請求の範囲1－19に係る発明の共通の事項は、「透明絶縁性の基板上に透明電極層を設けてなる透明電極付き基板と、該透明電極付き基板の透明電極層側に順次形成された、シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも有してなる光電変換装置であって、前記透明電極付き基板は、表面が凸状の複数の錐状体が配した形状であり、かつ光パイプ半値幅が500nm以上800nm以下の波長で20%以上である光電変換装置」である。

しかしながら、調査の結果、上記「光電変換装置」は、特開2005－347490号公報に開示されており、新規でないことが明らかであり、結果として、上記「光電変換装置」は先行技術の域を出ないから、PCT規則13.2の第2文の意味において、この共通事項は特別な技術的特徴ではない。

それ故、特別な技術的特徴として請求の範囲1－19に係る発明全てに共通の事項はなく、PCT規則13.2の第2文の意味において特別な技術的特徴と考えられる他の共通の事項も存在しないので、それらの間違する発明の間にPCT規則13の意味における技術的な関連を見いだすことはできない。

よって、請求項1－19に係る発明は、発明の単一性の要件を満たしていない。

1. ☐ 出願人が必要な追加調査手数料をすべて期間内に納付したので、この国際調査報告は、すべての調査可能な請求の範囲について作成した。

2. ☐ 追加調査手数料を要求するまでもなく、すべての調査可能な請求の範囲について調査することができたので、追加調査手数料の納付を求めなかった。

3. ☐ 出願人が必要な追加調査手数料を一部のみしか期間内に納付しなかったので、この国際調査報告は、手数料の納付のあった次の請求の範囲のみについて作成した。

4. ☑ 出願人が必要な追加調査手数料を期間内に納付しなかったので、この国際調査報告は、請求の範囲の最初に記載されている発明に係る次の請求の範囲について作成した。

請求項1－4、14、15

追加調査手数料の異議の申立てに関する注意

☐ 追加調査手数料及び、該当する場合には、異議申立手数料の納付と共に、出願人から異議申立てがあった。

☐ 追加調査手数料の納付と共に出願人から異議申立てがあったが、異議申立手数料が納付命令書に示した期間内に支払われなかった。

☐ 追加調査手数料の納付はあったが、異議申立てはなかった。

様式PCT/ISA/210（第1ページの続葉（2））（2007年4月）

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(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

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21. Mai 2008 (21.05.2008)

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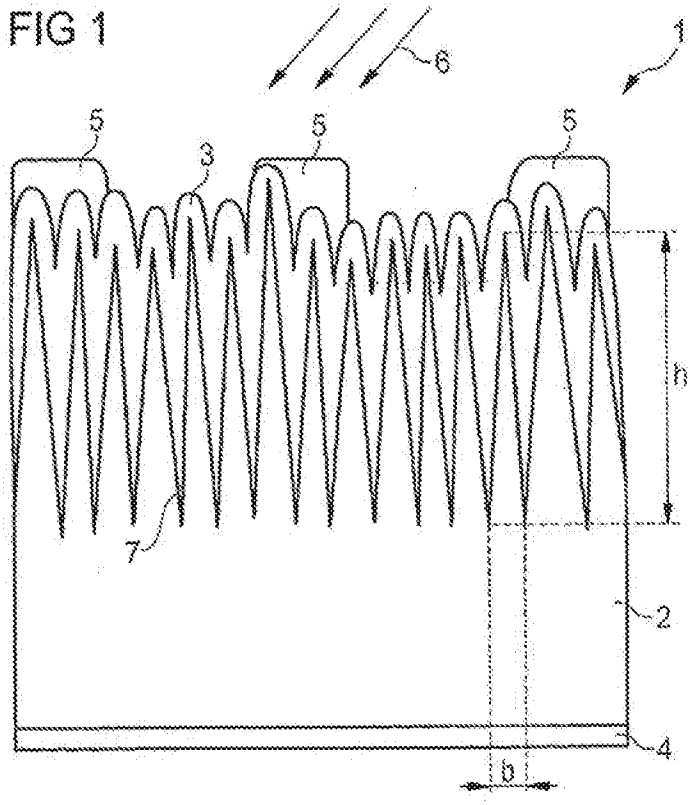
(81) Bestimmungsstaaten *(soweit nicht anders angegeben, für jede verfügbare nationale Schutzrechtsart)*: AE, AG, AL,

[Fortsetzung auf der nächsten Seite]

(54) Title: PHOTOSENSITIVE SEMICONDUCTOR COMPONENT

(54) Bezeichnung: FOTOEMPFINDLICHES HALBLEITERBAUELEMENT

FIG 1



(57) Abstract: The invention relates to a semiconductor component (1) comprising a photosensitive doped semiconductor layer (2), in which electric charge carriers are released during the absorption of electromagnetic radiation (6). The photosensitive semiconductor layer (2) has a structured boundary layer (7). The structured boundary layer (7) is positioned after at least one layer (3) that generates an electric field for separating the released charge carriers, said electric field extending over the structured boundary surface (7). The photosensitive semiconductor component (1) is characterised by a highly efficient charge carrier separation, in particular for generating an electric current.

(57) Zusammenfassung: Bei einem Halbleiterbauelement (1) mit einer fotoempfindlichen dotierten Halbleiterschicht (2), in der bei Absorption elektromagnetischer Strahlung (6) elektrische Ladungsträger freigesetzt werden, weist die fotoempfindliche Halbleiterschicht (2) eine strukturierte Grenzfläche (7) auf. Der strukturierten Grenzfläche (7) ist mindestens eine Schicht (3) nachgeordnet, die ein elektrisches Feld zur Trennung der freigesetzten Ladungsträger erzeugt, wobei sich das elektrische Feld über die strukturierte Grenzfläche (7) erstreckt. Das photoempfindliche Halbleiterbauelement (1) zeichnet sich durch eine hohe Effizienz der Ladungsträgertrennung, insbesondere zur Erzeugung eines elektrischen Stroms, aus.

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AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Bestimmungsstaaten** *(soweit nicht anders angegeben, für jede verfügbare regionale Schutzrechtsart)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), eurasisches (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), europäisches (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Veröffentlicht:

— *ohne internationalen Recherchenbericht und erneut zu veröffentlichen nach Erhalt des Berichts*

Beschreibung

Fotoempfindliches Halbleiterbauelement

Die Erfindung betrifft ein fotoempfindliches Halbleiterbauelement gemäß dem Oberbegriff des Patentanspruchs 1.

Diese Patentanmeldung beansprucht die Priorität der deutschen Patentanmeldung 102007024478.0, deren Offenbarungsgehalt hiermit durch Rückbezug aufgenommen wird.

Ein fotoempfindliches Halbleiterbauelement in Form einer Solarzelle ist zum Beispiel aus der Druckschrift US 4,177,093 bekannt. Die darin beschriebene Solarzelle umfasst ein dotiertes Halbleitersubstrat, eine darauf aufgebrachte Schicht aus Indiumzinnoxid (ITO) sowie elektrische Kontakte, die auf der Rückseite des Substrats und auf der Oberfläche der ITO-Schicht aufgebracht sind. Die ITO-Schicht wirkt mit dem Substrat derart zusammen, dass ähnlich wie bei einem pn-Übergang die im Substrat durch Absorption elektromagnetischer Strahlung freigesetzten elektrischen Ladungsträger zur Erzeugung eines elektrischen Stroms getrennt werden.

Eine weitere Solarzelle ist aus der Druckschrift US 5,949,123 bekannt. Diese Solarzelle basiert auf einem p-dotierten Siliziumsubstrat, in das ein n-Dotierstoff zur Erzeugung eines vergrabenen pn-Übergangs implantiert ist. Um die Reflexion der Oberfläche des Siliziumsubstrats zu vermindern, ist die Oberfläche des Siliziumsubstrats strukturiert. Auf diese Weise wird erreicht, dass ein höherer Lichtanteil in das Siliziumsubstrat eindringen kann.

In der Druckschrift WO 02/13279 A2 wird beschrieben, die

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Oberfläche einer Solarzelle mittels eines Ätzverfahrens zu strukturieren, um die Reflexion der Oberfläche zu vermindern.

Aus der Druckschrift M. Stubenrauch, M. Fischer, C. Kremin, S. Stoebenau, A. Albrecht, O. Nagel, „Black Silicon - New Functionalities in Microsystems", J. Michromech. Microeng. 16 (2006), S. S2-86, ist ein Plasmaätzverfahren zur Herstellung von nadelartigen Strukturen in Siliziumschichten bekannt. Weiterhin beschreibt auch die Druckschrift H. Jansen, M. De Boer, R. Legtenberg, M. Elwenspoek, „The black silicon method: a universal method for determining the parameter setting of a fluorine-based reactive ion etcher in deep silicon trench etching with profile control", J. Michromech. Microeng. 5 (1995), S. 115-120, ein Verfahren zur Herstellung von nadelartigen Strukturen in Silizium.

Der Erfindung liegt die Aufgabe zugrunde, ein verbessertes fotoempfindliches Halbleiterbauelement anzugeben, das sich insbesondere durch eine effizientere Ladungsträgertrennung der in einem fotoempfindlichen Halbleitermaterial erzeugten Ladungsträger auszeichnet.

Diese Aufgabe wird durch den Gegenstand des Patentanspruchs 1 gelöst. Vorteilhafte Ausgestaltungen und Weiterbildungen der Erfindung sind Gegenstand der abhängigen Ansprüche.

Bei einem erfindungsgemäßen Halbleiterbauelement mit einer fotoempfindlichen dotierten Halbleiterschicht, in der bei Absorption elektromagnetischer Strahlung elektrische Ladungsträger freigesetzt werden, weist die fotoempfindliche Halbleiterschicht eine strukturierte Grenzfläche auf. Der strukturierten Grenzfläche ist mindestens eine Schicht nachgeordnet, die ein elektrisches Feld zur Trennung der freigesetzten

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Ladungsträger erzeugt, wobei sich das elektrische Feld über die strukturierte Grenzfläche erstreckt.

Die der fotoempfindlichen Halbleiterschicht nachgeordnete Schicht kann unmittelbar auf die strukturierte Grenzfläche aufgebracht sein oder durch eine oder mehrere Zwischenschichten von der fotoempfindlichen Halbleiterschicht beabstandet sein. Dadurch, dass die zur Erzeugung eines elektrischen Feldes geeignete Schicht der fotoempfindlichen Halbleiterschicht nachgeordnet ist, wird erreicht, dass sich das elektrische Feld über die strukturierte Grenzfläche der fotoempfindlichen Schicht erstreckt. Somit ist der aktive Bereich, in dem eine Ladungsträgertrennung stattfindet, aufgrund der Strukturierung der photoempfindlichen Schicht wesentlich größer als bei herkömmlichen Bauelementen, bei denen der aktive Bereich beispielsweise aus einer ebenen Grenzfläche zwischen einem Siliziumsubstrat und einer ITO-Schicht oder aus einem innerhalb des Substrats ausgebildeten pn-Übergang gebildet ist. Durch die Strukturierung der fotoempfindlichen Schicht wird also nicht nur die Reflexion der Grenzfläche vermindert, sondern auch der aktive Bereich, in dem Ladungsträgertrennung stattfindet, vergrößert.

Die dem Substrat nachgeordnete Schicht enthält insbesondere ein transparentes elektrisch leitfähiges Material. Vorzugsweise ist das transparente elektrisch leitfähige Material ein transparentes leitfähiges Oxid, insbesondere Indiumzinnoxid (ITO), Indiumzinkoxid (IZO), Zinkoxid (ZnO) oder Cadmium-Stannat (CTO, Cd_2SnO_4).

Weiterhin kann das transparente elektrisch leitfähige Material auch ein transparentes leitfähiges Polymer sein.

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Bei einer weiteren bevorzugten Ausführungsform ist die der fotoempfindlichen Halbleiterschicht nachgeordnete Schicht eine Halbleiterschicht, die sich in ihren Dotierungstyp und/oder ihrer Dotierstoffkonzentration von der fotoempfindlichen Halbleiterschicht unterscheidet.

Insbesondere kann die der dotierten fotoempfindlichen Halbleiterschicht nachgeordnete Schicht den entgegengesetzten Dotierungstyp aufweisen, so dass zum Beispiel die fotoempfindliche Halbleiterschicht p-dotiert ist und die nachgeordnete Schicht n-dotiert ist oder umgekehrt. Auf diese Weise wird an der Grenzfläche der strukturierten fotoempfindlichen Halbleiterschicht ein pn-Übergang ausgebildet, wobei der pn-Übergang aufgrund der Strukturierung vorteilhaft größer ist als bei einer ebenen Grenzfläche zwischen den Halbleiterschichten entgegengesetzten Dotierungstyps.

Zwischen der fotoempfindlichen Schicht und der ihr nachgeordneten Schicht kann mindestens eine Zwischenschicht angeordnet sein. Insbesondere kann es sich bei der Zwischenschicht um eine Siliziumoxidschicht handeln, die sich beispielsweise auf der fotoempfindlichen Halbleiterschicht ausbilden kann, bevor die transparente leitfähige Schicht aufgebracht wird. Weiterhin kann es sich bei der Zwischenschicht auch um eine Schicht aus einem intrinsischen Halbleitermaterial handeln, insbesondere wenn es sich bei der fotoempfindlichen Halbleiterschicht und der nachgeordneten Schicht um zwei Halbleiterschichten mit verschiedenem Dotierungstyp handelt.

Die strukturierte Grenzfläche der fotoempfindlichen Halbleiterschicht ist vorzugsweise derart strukturiert, dass sie Strukturen mit einer Breite von weniger als 100 nm aufweist.

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Bevorzugt weist die strukturierte Grenzfläche Strukturen auf, die eine Breite zwischen 10 nm und 100 nm aufweisen.

Aufgrund der strukturierten Grenzfläche ist zwischen der fotoempfindlichen Schicht und der nachfolgenden Schicht ein Brechungsindexgradient ausgebildet, so dass die Grenzfläche zwischen den Schichten als effektives Medium wirkt.

Weiterhin ist es vorteilhaft, wenn die an der Grenzfläche der fotoempfindlichen Halbleiterschicht erzeugten Strukturen eine Höhe von mehr als 100 nm aufweisen. Insbesondere kann die Höhe der an der strukturierten Grenzfläche erzeugten Strukturen zwischen 1,5 µm und 10 µm betragen.

Die an der Grenzfläche der fotoempfindlichen Halbleiterschicht erzeugten Strukturen zeichnen sich insbesondere durch ein hohes Aspektverhältnis aus. Dies hat den Vorteil, dass die Grenzfläche im Vergleich zu einer nahezu glatten Grenzfläche erheblich vergrößert wird. Bevorzugt beträgt die Höhe der Strukturen im Mittel mindestens das 10-fache der Breite, besonders bevorzugt sogar mindestens das 50-fache der Breite.

Bei einer vorteilhaften Ausgestaltung weist die strukturierte Grenzfläche der fotoempfindlichen Halbleiterschicht Strukturen auf, die überwiegend, also mehr als zur Hälfte, eine Flankensteilheit von mehr als 45° aufweisen. Beispielsweise können die Flanken der Strukturen Winkel im Bereich von 80° bis 85° mit einer Hauptebene der photoempfindlichen Halbleiterschicht einschließen. Insbesondere kann es sich bei den Strukturen um nadelförmige Strukturen handeln.

Die strukturierte Grenzfläche kann insbesondere eine stochastische Struktur aufweisen, also eine Struktur, bei der

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die Strukturhöhen und Strukturbreiten im Gegensatz zu deterministischen Strukturen, die beispielsweise mit lithografischen Techniken erzeugt werden, eine statistische Verteilung aufweisen.

Bevorzugt ist die strukturierte Grenzfläche mittels eines Ätzverfahrens strukturiert. Dazu wird vorzugsweise ein Plasmaätzverfahren eingesetzt, wie insbesondere ein ICP-Ätzverfahren (inductively coupled plasma). Alternativ können aber auch andere Verfahren der physikalischen Abtragung wie beispielsweise Laserstrukturierung eingesetzt werden.

Die Anwendung eines Ätzverfahrens zur Erzeugung einer stochastischen Struktur ist im Vergleich zu lithographischen Strukturierungsverfahren vorteilhaft, weil der Herstellungsaufwand vergleichsweise gering ist.

Alternativ ist es aber auch möglich, dass die Grenzfläche der fotoempfindlichen Halbleiterschicht eine deterministische, also vorbestimmte Struktur aufweist, die beispielsweise lithografisch, insbesondere unter Verwendung einer Ätzmaske, hergestellt ist.

Die Erfindung wird im Folgenden anhand von Ausführungsbeispielen näher erläutert.

Es zeigen:

Figur 1 eine schematische Darstellung eines Halbleiterbauelements gemäß einem ersten Ausführungsbeispiel der Erfindung,

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Figur 2 eine grafische Darstellung der Reflexion einer strukturierten Siliziumschicht im Vergleich zu einer unstrukturierten Siliziumschicht und

Figur 3 eine schematische Darstellung eines Halbleiterbauelements gemäß einem zweiten Ausführungsbeispiel der Erfindung.

Gleiche oder gleich wirkende Elemente sind in den Figuren mit den gleichen Bezugszeichen versehen. Die Figuren sind nicht als maßstabsgerecht anzusehen, vielmehr können einzelne Elemente zur Verdeutlichung übertrieben groß dargestellt sein.

Das in Figur 1 dargestellte Halbleiterbauelement 1 gemäß einem ersten Ausführungsbeispiel der Erfindung ist eine Solarzelle, die eine fotoempfindliche Halbleiterschicht 2, zum Beispiel eine p-dotierte Siliziumschicht, enthält. Die Halbleiterschicht 2 kann insbesondere ein Silizium-Wafer sein, der typischerweise eine Dicke von mehr als 100 µm aufweist. Alternativ kann die Halbleiterschicht 2 aber auch eine auf ein Substrat aufgebrachte Halbleiterschicht sein, zum Beispiel eine auf einen metallischen Reflektor (nicht dargestellt) aufgebrachte Halbleiterschicht.

In der fotoempfindlichen Halbleiterschicht 2 werden beim Auftreffen elektromagnetischer Strahlung, die durch die Pfeile 6 angedeutet ist, elektrische Ladungsträger freigesetzt. Insbesondere kann es sich bei dem Halbleiterbauelement 1 um eine Solarzelle handeln, bei der durch Absorption von Sonnenlicht in der fotoempfindlichen Halbleiterschicht 2 Elektron-Loch-Paare als freie Ladungsträger erzeugt werden.

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Auf die fotoempfindliche Halbleiterschicht 2 ist eine Schicht 3 aufgebracht, mittels der ein elektrisches Feld zur Trennung der freigesetzten Ladungsträger erzeugt wird. Auf diese Weise kann insbesondere ein elektrischer Strom aus den freigesetzten Ladungsträgern erzeugt werden. Um den elektrischen Strom aus dem Halbleiterbauelement 1 abzuführen, kann ein erster elektrischer Kontakt 4 an einer von der Schicht 3 abgewandten Rückseite der Halbleiterschicht 2 und ein weiterer elektrischer Kontakt 5 auf der Schicht 3 angeordnet sein. Der zweite elektrische Kontakt 5 kann beispielsweise streifenförmig über die Grenzfläche der Schicht 3 geführt sein.

Die fotoempfindliche Halbleiterschicht 2 weist eine strukturierte Grenzfläche 7 auf. Die strukturierte Grenzfläche 7 kann beispielsweise mit einem Plasmaätzverfahren, insbesondere durch induktiv gekoppeltes Plasmaätzen (ICP) erzeugt werden. Dabei werden beispielsweise SF_6 und O_2 als Ätzgase verwendet. Die Form der erzeugten Strukturen kann dabei durch die Wahl der Ätzparameter, insbesondere der Zusammensetzung der Ätzgase, gezielt eingestellt werden. Geeignete Plasmaätzverfahren, insbesondere zur Erzeugung nadelförmiger Strukturen, sind an sich aus den in der Einleitung zitierten Druckschriften bekannt und werden daher nicht näher erläutert.

Bevorzugt werden mit dem Ätzverfahren an der Grenzfläche 7 Strukturen erzeugt, die ein hohes Aspektverhältnis aufweisen. Die Grenzflächenstrukturen weisen bevorzugt eine Höhe h auf, die größer als ihre Breite b ist. Bevorzugt beträgt die Höhe der Strukturen h im Mittel mindestens das 10-fache der Breite b, besonders bevorzugt sogar mindestens das 50-fache der Breite b. Insbesondere zeichnen sich die Strukturen vorteilhaft durch eine hohe Flankensteilheit auf. Bevorzugt weisen

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die Strukturen überwiegend, das heißt mindestens zur Hälfte, eine Flankensteilheit von mehr als 45° auf.

Die Breite b der Strukturen beträgt bevorzugt weniger als 100 nm, insbesondere zwischen einschließlich 10 nm und einschließlich 100 nm. Die Höhe h der Strukturen der Grenzfläche 7 beträgt vorzugsweise zwischen einschließlich 1,5 µm und einschließlich 5 µm.

Die Strukturierung der Grenzfläche 7 der Halbleiterschicht 2 wirkt sich in zweifacher Hinsicht positiv auf die Effizienz des Halbleiterbauelements 1 aus. Zum einen wird die Reflexion der Grenzfläche der Halbleiterschicht 2 durch die Strukturierung vermindert. Aufgrund der Strukturierung der fotoempfindlichen Halbleiterschicht 2 vermindert sich auch die Reflexion der Oberfläche des Halbleiterbauelements, wenn die mindestens eine der Halbleiterschicht nachfolgende Schicht 3 derart dünn ist, dass auch ihre Oberfläche die Strukturierung aufweist. Die Verminderung der Reflexion der Grenzfläche 7 der Halbleiterschicht 2 wird in Figur 2 verdeutlicht, in der die Reflexion einer Siliziumschicht vor und nach der Strukturierung in Abhängigkeit von der Wellenlänge dargestellt ist. Die Kurve 9 stellt die Reflexion der Siliziumschicht vor der Strukturierung und die Kurve 10 die Reflexion der Siliziumschicht nach der Strukturierung dar. Da die strukturierte Schicht eine wesentliche geringere Reflexion als eine unstrukturierte Schicht aufweist, kann ein größerer Anteil der auftreffenden Strahlung in die photoempfindliche Schicht eindringen, wodurch die Effizienz des photoempfindlichen Halbleiterbauelements verbessert wird.

Ein weiterer Vorteil der Strukturierung der Halbleiterschicht 2 ergibt sich daraus, dass die Schicht 3, mittels der ein

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elektrisches Feld zur Trennung der in der fotoempfindlichen Halbleiterschicht 2 freigesetzten Ladungsträger erzeugt wird, der Halbleiterschicht 2 nachgeordnet ist, d.h. auf oder über der photoempfindlichen Halbleiterschicht 2 angeordnet ist. Auf diese Weise wird erreicht, dass sich das elektrische Feld, mit dem die freigesetzten Ladungsträger getrennt werden, über die strukturierte Grenzfläche 7 der Halbleiterschicht 2 erstreckt. Der Bereich, in dem die Ladungsträgertrennung stattfindet, ist daher größer als im Fall einer unstrukturierten Grenzfläche zwischen einer Halbleiterschicht 2 und der ihr nachgeordneten Schicht 3. Beispielsweise kann durch die Strukturierung die Grenzfläche 7 der fotoempfindlichen Halbleiterschicht um einen Faktor 10 oder mehr vergrößert werden.

Die der strukturierten Halbleiterschicht 2 nachgeordnete Schicht 3 enthält vorzugsweise ein transparentes elektrisch leitfähiges Material, insbesondere ein transparentes leitfähiges Oxid oder ein transparentes leitfähiges Polymer. Die Schicht 3 kann zum Beispiel eine Dicke von etwa 1 µm aufweisen.

Geeignete transparente leitfähige Oxide sind insbesondere Indiumzinnoxid (ITO) und Indiumzinkoxid (IZO). Weiterhin sind Zinkoxid (ZnO), das insbesondere mit Al dotiert sein kann, oder Cadmium-Stannat (Cd_2SnO_4) geeignet.

Alternativ ist es auch möglich, dass die Schicht 3 ein Halbleitermaterial aufweist, das einen zu der Halbleiterschicht 2 entgegengesetzten Dotierungstyp aufweist. Beispielsweise kann die Halbleiterschicht 2 p-dotiert und die Schicht 3 n-dotiert sein. In diesem Fall ist zwischen der Halbleiterschicht 2 und der Schicht 3 ein pn-Übergang ausgebildet, der sich über die

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strukturierte Grenzfläche 7 der Halbleiterschicht 2 erstreckt. Der Bereich des pn-Übergangs ist aufgrund der Strukturierung vorteilhaft wesentlich größer als im Fall einer ebenen Grenzfläche zwischen einer p-dotierten Halbleiterschicht und einer n-dotierten Halbleiterschicht. Bei den Schichten 2, 3 kann es sich beispielsweise um Siliziumschichten mit unterschiedlicher Dotierung handeln. Alternativ können aber auch andere Halbleitermaterialien eingesetzt werden, beispielsweise III-V-Halbleitermaterialien wie insbesondere GaAs oder InAs.

Das in Figur 3 dargestellte Ausführungsbeispiel eines Halbleiterbauelements unterscheidet sich von dem in Figur 1 dargestellten dadurch, dass zwischen der fotoempfindlichen Halbleiterschicht 2 und der ihr nachgeordneten Schicht 3, mittels der das elektrische Feld zur Ladungsträgertrennung erzeugt wird, eine Zwischenschicht 8 angeordnet ist. Insbesondere kann die fotoempfindliche Halbleiterschicht 2 eine Siliziumschicht und die Zwischenschicht 8 eine Siliziumoxidschicht sein. Die Siliziumoxidschicht 8 kann insbesondere eine natürliche Oxidschicht sein, die sich auf der Siliziumschicht 2 ausbildet, wenn die Halbleiterschicht 2 vor dem Aufbringen der Schicht 3 in Kontakt mit Luft gerät.

Weiterhin kann es sich bei der Zwischenschicht 8 auch um eine Schicht aus einem intrinsischen Halbleitermaterial handeln, die beispielsweise zwischen zwei entgegengesetzten dotierten Halbleiterschichten eingefügt ist, um die Rekombination der Ladungsträger zu vermindern.

Die Erfindung ist nicht durch die Beschreibung anhand der Ausführungsbeispiele beschränkt. Vielmehr umfasst die Erfindung jedes neue Merkmal sowie jede Kombination von Merkmalen,

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was insbesondere jede Kombination von Merkmalen in den Patentansprüchen beinhaltet, auch wenn dieses Merkmal oder diese Kombination selbst nicht explizit in den Patentansprüchen oder Ausführungsbeispielen angegeben ist.

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Patentansprüche

1. Halbleiterbauelement (1) mit einer fotoempfindlichen dotierten Halbleiterschicht (2), in der bei Absorption elektromagnetischer Strahlung (6) elektrische Ladungsträger freigesetzt werden, wobei die fotoempfindliche Halbleiterschicht (2) eine strukturierte Grenzfläche (7) aufweist,
dadurch gekennzeichnet, dass
der strukturierten Grenzfläche (7) mindestens eine Schicht (3) nachgeordnet ist, die ein elektrisches Feld zur Trennung der freigesetzten Ladungsträger erzeugt, wobei sich das elektrische Feld über die strukturierte Grenzfläche (7) erstreckt.

2. Halbleiterbauelement nach Anspruch 1,
dadurch gekennzeichnet, dass
die der fotoempfindlichen Halbleiterschicht (2) nachgeordnete Schicht (3) ein transparentes elektrisch leitfähiges Material enthält.

3. Halbleiterbauelement nach Anspruch 2,
dadurch gekennzeichnet, dass
das transparente elektrisch leitfähige Material ein transparentes leitfähiges Oxid ist.

4. Halbleiterbauelement nach Anspruch 3,
dadurch gekennzeichnet, dass
das transparente leitfähige Oxid Indiumzinnoxid, Indiumzinkoxid, Zinkoxid oder Cadmium-Stannat ist.

5. Halbleiterbauelement nach Anspruch 2,
dadurch gekennzeichnet, dass

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das transparente elektrisch leitfähige Material ein transparentes leitfähiges Polymer ist.

6. Halbleiterbauelement nach Anspruch 2, dadurch gekennzeichnet, dass die der fotoempfindlichen Halbleiterschicht (2) nachgeordnete Schicht (3) eine Halbleiterschicht ist, die sich in ihrem Dotierungstyp und/oder ihrer Dotierstoffkonzentration von der fotoempfindlichen Halbleiterschicht (2) unterscheidet.

7. Halbleiterbauelement nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass zwischen der fotoempfindlichen Schicht (2) und der ihr nachgeordneten Schicht (3) mindestens eine Zwischenschicht (8) angeordnet ist.

8. Halbleiterbauelement nach Anspruch 7, dadurch gekennzeichnet, dass die Zwischenschicht (8) ein Siliziumoxid oder ein intrinsisches Halbleitermaterial enthält.

9. Halbleiterbauelement nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (3) Strukturen mit einer Breite (b) von weniger als 100 nm aufweist.

10. Halbleiterbauelement nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass

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die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (2) Strukturen mit einer Höhe (h) von mehr als 100 nm aufweist.

11. Halbleiterbauelement nach Anspruch 10, dadurch gekennzeichnet, dass die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (2) Strukturen mit einer Höhe (h) zwischen 1,5 µm und 10 µm aufweist.

12. Halbleiterbauelement nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (2) Strukturen aufweist, deren Höhe mindestens das 50-fache der Breite beträgt.

13. Halbleiterbauelement nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (2) Strukturen mit einer Flächendichte von mindestens 10^4 cm^{-2} aufweist.

14. Halbleiterbauelement nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (2) Strukturen aufweist, die überwiegend eine Flankensteilheit von mehr als 45° aufweisen.

15. Halbleiterbauelement nach einem der vorhergehenden Ansprüche,

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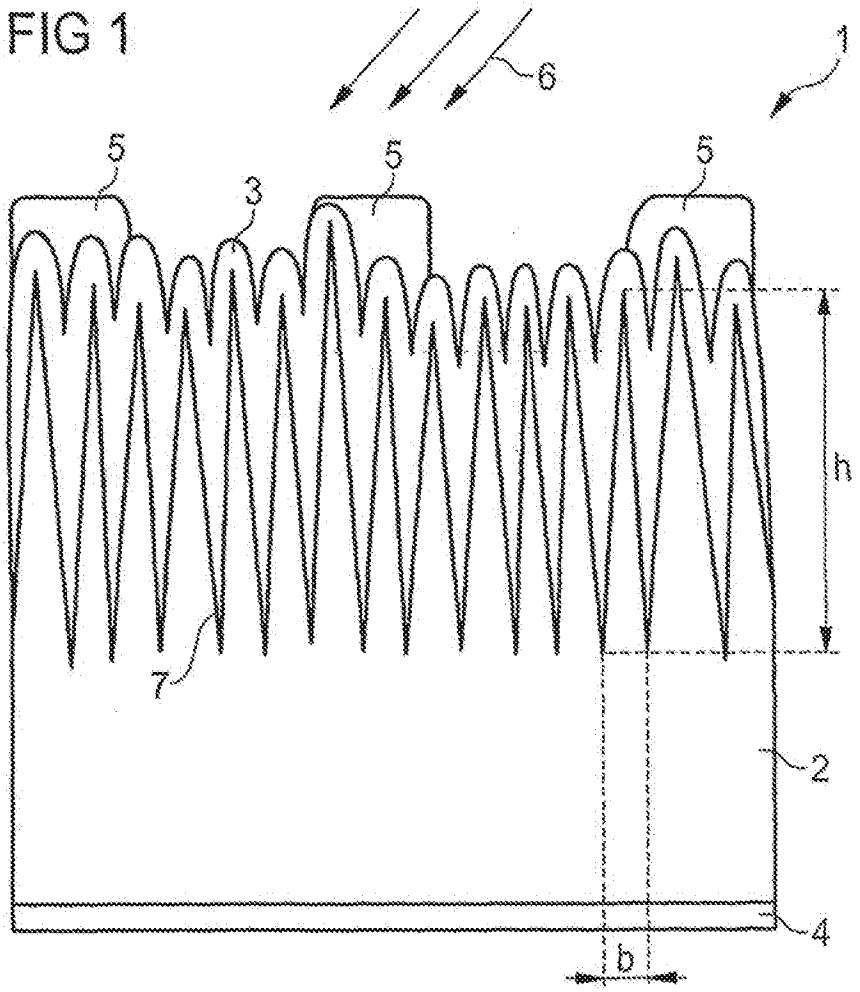
dadurch gekennzeichnet, dass
die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (2) eine stochastische Struktur aufweist.

16. Halbleiterbauelement nach einem der Ansprüche 1 bis 14, dadurch gekennzeichnet, dass
die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (2) eine deterministische Struktur aufweist.

17. Halbleiterbauelement nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass
die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (2) mittels eines Ätzverfahrens strukturiert ist.

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FIG 1



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FIG 2

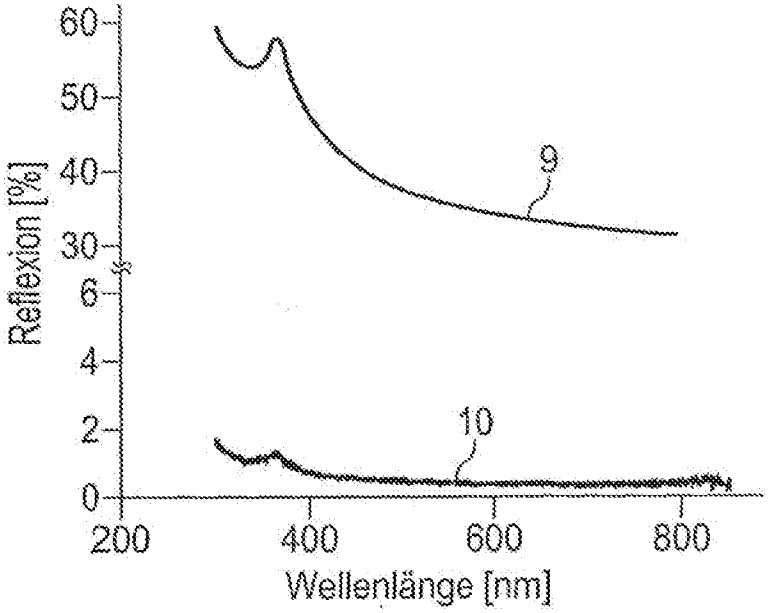
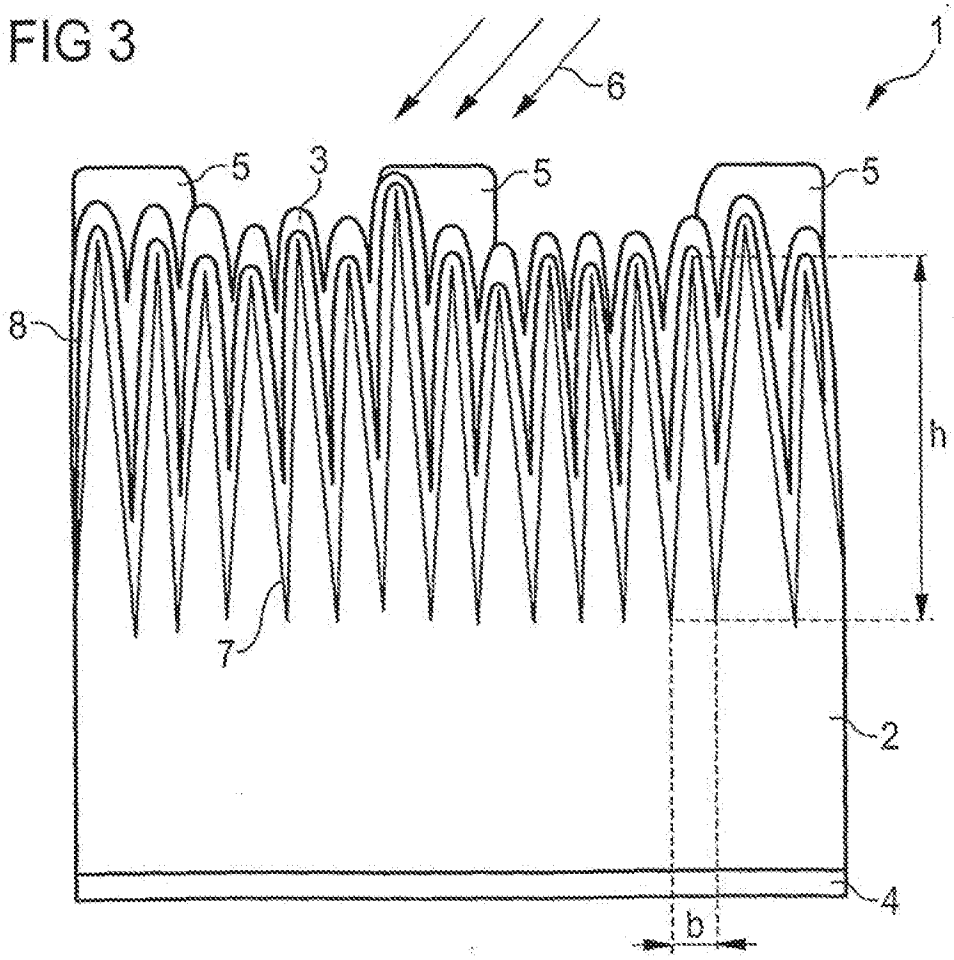


FIG 3



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Espacenet

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SYSTEM AND METHODS FOR LASER ASSISTED DEPOSITION

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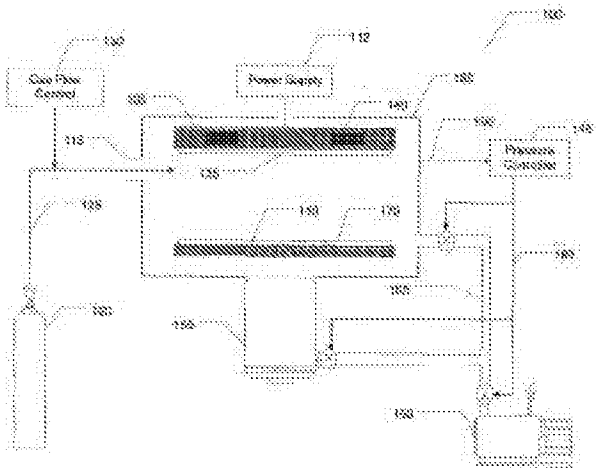
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Abstract of WO0241363 (A2)

Systems and methods for laser assisted deposition use an energy source such as a laser to simultaneously deposit and anneal a thin film of semiconductor or metal material on a substrate. The uniform heating of the deposited material while the layer is being sputtered obviates a subsequent annealing stage. The laser can be pulsed or continuous wave. The substrate can be plastic such as tedlar, mylar, teflon, or tefzel. The systems and methods for laser assisted deposition can be used to manufacture solar cells, such as a cadmium telluride (CdTe) solar cell having a cadmium sulfide (CdS) window layer. Both the techniques of sputtering and sublimation can be used to grow the layer.



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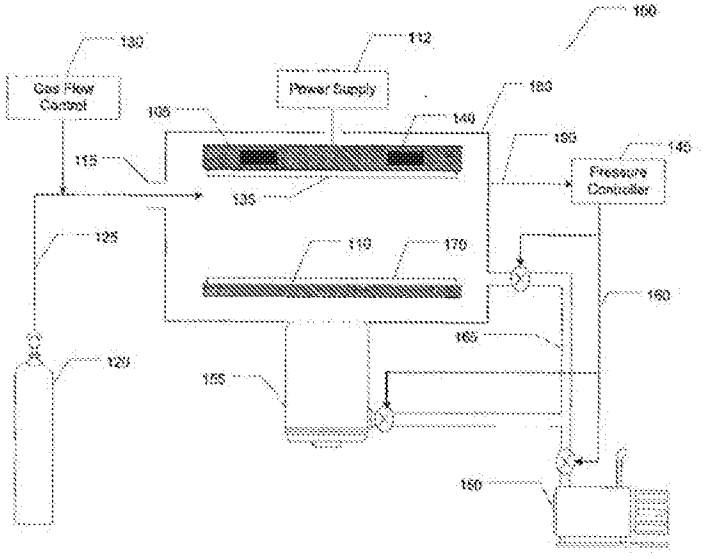
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(54) Title: SYSTEM AND METHODS FOR LASER ASSISTED DEPOSITION



(57) Abstract: Systems and methods for laser assisted deposition use an energy source such as a laser to simultaneously deposit and anneal a thin film of semiconductor or metal material on a substrate. The uniform heating of the deposited material while the layer is being sputtered obviates a subsequent annealing stage. The laser can be pulsed or continuous wave. The substrate can be plastic such as tedlar, mylar, teflon, or tefzel. The systems and methods for laser assisted deposition can be used to manufacture solar cells, such as a cadmium telluride (CdTe) solar cell having a cadmium sulfide (CdS) window layer. Both the techniques of sputtering and sublimation can be used to grow the layer.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

SYSTEMS AND METHODS FOR LASER ASSISTED DEPOSITION

Related Applications

[01] This application claims the benefit of United States Provisional Application Serial No. 60/249,367, filed November 16, 2000, and United States Provisional Application Serial No. 60/254,760, filed December 12, 2000, and this application is a continuation-in-part of United States Patent Application Serial No. 09/892,131 filed June 25, 2001.

Field of the Invention

[02] The present invention relates generally to the deposition of thin films and, more particularly relates to methods and systems for laser assisted deposition.

Background of the Invention

[03] The fabrication of solar cells presents unique manufacturability challenges to the solar energy industry. Chief among them is the difficulty often encountered in depositing the semiconductor layers that form a cell's pn-junction onto a substrate material capable of withstanding high processing temperatures. In the past, this challenge has prevented the manufacture of solar cells on flexible materials such as plastic because many plastics break down or become damaged during high temperature deposition and annealing.

[04] Known deposition systems for creating thin films include evaporation, chemical vapor deposition and sublimation. Deposition is a physical vapor deposition process in which a target material is bombarded by high-energy ions, causing the target material to eject atoms or molecules that are then deposited in a thin layer on the substrate. Deposition is relied on heavily in the solar cell industry for at least two reasons: First, deposition permits the deposition of complex alloys, such as CdTe, CdS, and other compound semiconductors. Second, deposition is ideal for depositing controlled, uniform films onto substrates having large surface area, such as the substrates used to

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produce solar cells and panels. Sublimation is an alternative technique for depositing a solid state material onto a surface that is also widely used to manufacture solar cells.

[05] In semiconductor wafer manufacturing, annealing has traditionally been performed as a follow-on step subsequent to ion implantation or other process step known to damage the crystal lattice. In contrast, thin film manufacturing uses annealing primarily to improve crystalinity of the amorphous deposited layer. In both cases, annealing usually takes place at a temperature of about 500°C. Most plastics break down when exposed to such high heat. As a result, thin film solar cell construction has required a heat tolerant substrate material such as glass. Unfortunately, glass solar cells have limited applications due to their cost and bulkiness. Thus, a manufacturing process and apparatus capable of depositing thin film layers onto a flexible and low-cost plastic or polymeric substrate is desirable.

Summary of the Invention

[06] The present invention addresses the drawbacks of prior art thin film deposition techniques noted above and provides systems and methods for laser assisted deposition of thin films.

[07] The systems and methods for laser assisted deposition use a thin film deposition technique that combines thin film deposition and annealing into one processing stage. In one embodiment, the target material for deposition is mounted to a negatively charged cathode in a magnetron or similar processing apparatus having a plasma within a chamber and sputter-depositing the target material onto a substrate to build a thin film layer thereon. In one embodiment the substrate material is a plastic or polymeric material such as tedlar, mylar, tefzel, or teflon.

[08] The processing apparatus can be modified to contain an energy source. In one implementation of the invention, the energy source is a laser. The energy source could be any homogenized beam energy source producing electromagnetic energy of any wavelength sufficient to anneal the thin film layer without overheating or damaging the substrate. The energy source can be a pulsed source of very short duration so as to prevent the beam from damaging the substrate. Alternatively, the energy source can be a continuous wave source that is scanned back and forth across the film surface in order

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to evenly heat the target material as it gets deposited onto the substrate. In both cases, the majority of the energy from the source is ideally absorbed by the film before being passed on to the substrate.

[09] In one embodiment of the invention, the systems and methods for laser assisted deposition are used to manufacture a solar cell, for example a cadmium telluride solar cell having cadmium telluride (CdTe) as the absorption layer and cadmium sulfide (CdS) as the window layer. Other layers utilizing laser assisted deposition, such as current collection layers, may be necessary to complete the solar cell.

[10] The systems and methods for laser assisted deposition may incorporate a radio frequency system, a magnetron, or any other similar apparatus designed for depositing thin films.

Brief Description of the Drawings

[11] The details of the present invention, both as to its structure and operation, may be gleaned in part by study of the accompanying drawings, in which like reference numerals refer to like parts, and in which:

[12] **Figure 1** is a diagram of a typical system using a parallel plate DC magnetron used to sputter-deposit thin films.

[13] **Figure 2** is an enlarged view of a process chamber used in a typical parallel plate DC magnetron showing the details of particle interaction.

[14] **Figure 3** is a flow diagram of the basic steps involved in thin film deposition.

[15] **Figure 4** is a diagram of a parallel plate DC magnetron as modified to include an energy source according to one embodiment of the systems and methods for laser assisted deposition.

[16] **Figure 5** is a flow diagram of one embodiment of the systems and methods for laser assisted deposition which employs sputtering.

[17] **Figure 6** is a diagram of a sublimation chamber modified to include an energy source according to one embodiment of the systems and methods for laser assisted deposition.

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Detailed Description of the Invention

[18] The systems and methods for laser assisted deposition overcome the aforementioned manufacturability problem by providing an energy source with a deposition apparatus that simultaneously deposits and anneals a target material onto a substrate. In one embodiment, the deposition systems and methods employ a simple parallel plate DC diode deposition apparatus. In other embodiments, the deposition apparatus may be a magnetron, an RF system, a sublimation chamber, or any other apparatus designed for manufacturing thin films.

[19] **Figure 1** is a diagram of a typical system using a parallel plate DC magnetron 100 used to sputter-deposit thin films. Cathode 105 is equipped with magnets 140 and is held at a negative potential with respect to anode 110 by DC power supply 112. Target material 135 is mounted to cathode 105 and substrate material 170 lays atop anode 110. Pressure controller 145 is attached to sputter chamber 180 via pressure control line 190. Gas inlet 115 is connected to gas supply 120 via gas supply line 125. Gas flow controller 130 also connects to gas supply line 125. Pressure controller 145 is also coupled to roughing pump 150 and turbo pump 155 via vacuum control lines 160. Finally, a network of vacuum outtake tubes 165 connects turbo pump 155 and roughing pump 150 to process chamber 180.

[20] **Figure 2** is an expanded view of process chamber 180 showing the details of particle interaction within magnetron system 100. Positively charged gas ions 205 interact with target material 135 in plasma 215. Dislodged particles 210 from target material 135 migrate toward substrate 170 through plasma 215. Target material 135 can be, for instance, a semiconductor material such as cadmium sulfide, or a metal such as copper, both used in the manufacture of solar cells. Excess matter 220 is removed from process chamber 180 through vacuum outtake 165.

[21] Cathode 105 of parallel plate DC magnetron 100 houses magnets 140 configured around and behind target material 135 to capture and restrict electrons 225 near target material 135. The purpose of magnets 140 is to cause electrons 225 from cathode 105 to spin in the magnetic field created by cathode 180 and anode 110. A single electron 225 can liberate as many as thirty new electrons 225 by impacting and ionizing inert gas atoms 205. Thus, in the dark space near the face of target material

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135, spinning electrons 225 ionize the flood of inert gas atoms 205. Ionized inert gas atoms 205, now positively charged, accelerate to collide with the surface of target material 135. The result is a higher overall deposition rate of magnetron 100 due to a greater number of positively charged ions 205 bombarding target material 135.

[22] Other embodiments of process chamber 180 include a simple parallel plate DC diode deposition apparatus having no magnets 140. As just described, magnets 140 are preferable to the extent that they improve the deposition rate. Process chamber 180, so modified to include magnets 140, is commonly called a magnetron. However, process chamber 180 may be further modified such that the electric field between cathode 105 and anode 110 is an RF (radio frequency) field. In this RF embodiment, the deposition apparatus uses RF energy to create the plasma instead of the DC field described above.

[23] The basic steps to deposition are depicted in **Figure 3**. In step 305, positively charged ions of inert gas 205 are generated in plasma 215 in high vacuum chamber 180 and accelerated toward target material 135 at a negative potential. Argon is often the inert gas of choice due to its relative abundance in earth's atmosphere. In step 310, positively charged ions 205 gain momentum and accelerate toward target material 135. Upon physical impact with target material 135 in step 315, particles from target material 135 are physically dislodged. In step 320, the dislodged particles migrate toward the surface of substrate 170. In step 325, the sputtered particles condense and form a thin film on substrate 170 with essentially the same material composition as target material 135. In step 330, excess material 320 is removed from the chamber by vacuum outtake 165. Finally, a typical thin film device manufacturing method also usually comprises a subsequent annealing phase 335 wherein the deposited layer is annealed at high temperature in order to eliminate film irregularity or repair any damage caused to the layer during deposition.

[24] The systems and methods thus far described are suitable for thin film deposition in semiconductor device fabrication situations of all types, including building metallization layers in silicon wafer processing and deposition of the thin film layers comprising a solar cell. In the manufacture of thin film solar cells in particular, annealing step 335 can serve the special purpose of crystallizing an amorphous deposited layer. Deposited layers are often amorphous; hence, the subsequent

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annealing of such a layer acts to improve the electrical and physical properties of the film by decreasing the number of defects and grain boundaries as the layer progresses toward polycrystal.

[25] Annealing is a thermal treatment usually accomplished in furnaces following layer deposition, or multi-layer deposition. Annealing furnaces typically expose devices to high heat for very long duration. Where the device is a thin film solar cell built on a plastic substrate, both high heat and long duration can cause permanent damage to the substrate. Rapid thermal annealing is an example of a technique that has been developed by process engineers to minimize the exposure of a device to extreme annealing temperatures. However, the high target temperatures reached in a rapid anneal can cause damage to plastic even though the exposure is limited in time.

[26] The systems and methods for laser assisted deposition permit the deposition of thin films on plastic substrates by merging the deposition and annealing together in one step. Combined deposition and annealing eliminates the subsequent anneal stage 335 of the thin film process of **figure 3**. Process chamber 180 is able to simultaneously deposit and anneal the thin film because the system for laser assisted deposition includes an energy source for uniformly heating the target material while it is deposited as further illustrated below.

[27] **Figure 4** is a diagram of the process chamber of **figure 2** as modified to include energy source 410 according to one implementation of the systems and methods for laser assisted deposition. In one embodiment, energy source 410 is designed to emit energy through a port 420 provided in cathode 105 and aimed at substrate 170. However, energy source 410 could be provided at any suitable position within process chamber 180. Also, the vacuum conditions created in process chamber 180 are designed to have negligible effect on the output of energy source 410.

[28] Energy source 410 may be, for instance, any of a number of tunable lasers or masers. Also, the particular type of source selected may be modulated in both beam energy density and beam center frequency. The energy density used is varied in time in synchronization with the particular layer thickness. The high level of control of the energy density is best achieved with a cw (continuous wave) laser with long temporal coherence length. It is often necessary to deposit only a very small total energy per

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square centimeter of deposition layer. Additionally, the cw beam intensity also may be slowly modulated as cell layer depth increases, using only an amount of intensity that will result in the desired temperature in the selected layer. Control over beam intensity prevents destroying the layer, which could occur if the temperature were to rise too quickly.

[29] Energy source 410 may also be a pulse laser. However, pulse lasers are much more difficult to control in energy delivery to substrate 170 since their energy is delivered in a pulse that has poor temporal coherence by comparison with cw beams. The peaked pulse of the pulse laser output makes it far less desirable as a controlled power source.

[30] In one implementation, energy source 410 is a modified solid state laser such as a Yttrium-Aluminum-Garnet (YAG) laser. In other implementations, energy source 410 is a continuous wave laser. However, the system and method for laser assisted deposition contemplates any of the many types of lasers available including those lasers categorized by the physical state of the active medium employed (i.e., gas, liquid, and solid-state), as well as those lasers categorized by their wavelength (i.e., infrared, visible, and ultraviolet). Energy source 410 is chiefly responsible for ensuring that the deposited layer is adequately annealed at the same time as it gets deposited. In effect, annealing takes place in a layer-by-layer fashion while the thin film is sputtered onto substrate 170.

[31] If energy source 410 is a continuous wave laser light source, the beam emanating from source 410 could be rapidly and continuously scanned back and forth across the film. A stationary continuous beam may cause damage to substrate 170 or to the deposited film if allowed to irradiate an isolated portion of substrate 170 or deposited layer for too long. In whatever implementation of source 410, either continuous wave or pulsed, the energy directed at the thin film surface must be substantially absorbed by the thin film layer itself with as little energy as possible passing to substrate 170. Both the fine tuning of the laser's output and/or a cooling circuit can help to achieve optimal energy absorption and protect substrate 170 in case of excessive exposure. A cooling circuit would contact the reverse side of substrate

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170 and provide a temperature differential that can be controlled to keep substrate 170 within the acceptable temperature range.

[32] In one embodiment, port 420 is a clear opening (not shown) in cathode 105 through which a laser beam is able to pass. A window covering port 420 and interfacing with chamber 180 could be used but would have to be frequently cleaned in order to prevent build-up of target material 135 and other matter from obscuring the passage of the beam. In another embodiment, the window is covered with a transparent conductive layer such as indium-tin-oxide (ITO) and charged to a negative potential for repelling particles from target material 135. This repulsion would help control or eliminate the potential build-up of matter on the window and would ease the burden of having to clean the window as frequently.

[33] The systems and methods of laser assisted deposition are easily understood from the process flow diagram of **figure 5**. In step 505, positively charged ions of inert gas 205 are generated in plasma 215 in high vacuum chamber 180 and accelerated toward target material 135 held at a negative potential. As before, argon gas is frequently chosen for inert gas 205 because it is abundant and inexpensive. In step 510, positively charged ions 205 gain momentum and accelerate toward target material 135. Upon physical impact with target material 135 in step 515, atoms from target material 135 are physically dislodged and upon arriving at the growing thin film layer, are uniformly heated by energy source 410.

[34] Step 520 represents a significant departure from the conventional systems and methods of deposition. Whereas deposition and annealing were two distinct steps in the method and systems of **figures 1-3**, the systems and methods of laser assisted deposition combine deposition and annealing into one step to produce a thin film layer that is simultaneously annealed while being deposited onto the substrate. The controlled heating of the deposited material in this step anneals the sputtered material at the same time it is being deposited onto substrate 170. Control of the temperature at this stage is critical. The laser light source must generate energy just adequate to ensure that the target material is annealed but without causing harm to the substrate.

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[35] In step 525, the sputtered atoms condense and form a thin film on substrate 170 with essentially the same material composition as target material 135. Finally, in step 530, excess material 220 is removed from chamber 180 by vacuum pump 165.

[36] In addition to controlling the output of energy source 410, the temperature at which laser assisted deposition is carried out must be kept sufficiently low to avoid damaging the plastic or polymer substrate 170. In one embodiment, the systems and methods for laser assisted deposition are carried out at room temperature. In another embodiment, the systems and methods for laser assisted deposition are carried out at or below the temperature above which the thin film of material crystallizes, so long as this temperature does not melt or damage substrate 170. In another embodiment, the systems and methods for laser assisted deposition are carried out below the critical temperature of substrate 170. The critical temperature of substrate 170 is the temperature at which substrate 170 begins to sustain permanent damage.

[37] The systems and methods for laser assisted deposition also allow each layer of a cell to be annealed separately as it is produced, rather than annealing an entire stack of layers simultaneously. This advantage means that less energy is used to anneal a single layer; hence, the substrate temperature rise as well as the temperature rise of the underlying layers is minimized. Individual layer annealing also reduces problems that arise due to differences in thermal expansion coefficients of the various layers because the temperature rise of the underlying layers is kept to a minimum. In another embodiment, simultaneous deposition and anneal permits annealing of a portion of the thickness of a layer at a time, further reducing the amount of heat to which the substrate is exposed.

[38] A principle purpose of the systems and methods for laser assisted deposition is to optimize the sheet resistance of the deposited layer. Since sheet resistance causes electrical losses in the cell, deposited thin films should have a sheet resistance as low as possible. One way to reduce sheet resistance involves increasing the thickness of the film. The disadvantage to thicker films, at least in the context of solar cells, is reduced flexibility; and in some instances, a thicker cell may undesirably alter the cell's optical absorption properties. Laser assisted deposition is a superior method of improving sheet resistance, which uses a laser beam to control annealing energy without causing

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the substrate to overheat. All else being equal, the simultaneous annealing disclosed as part of the systems and methods for laser assisted deposition generates films of very low sheet resistance without increasing the thickness of the film. The result is a film of superior crystalline structure having, in addition to a low sheet resistance, a finer structure and larger grain size without high temperature processing.

[39] The systems and methods for laser assisted deposition can be used to create thin film solar cells on a flexible or plastic substrate such as disclosed in pending U.S. Patent Application Serial No. 09/892,131 and said Application is fully incorporated by reference herein as though included in its entirety. Sputter depositing a thin film of the compound semiconductor CdTe has proven difficult; therefore, the systems and methods for laser assisted deposition contemplate the use of sublimation techniques to grow a CdTe absorption layer. Sublimation can be used, however, to grow any layers of a cell, including metallization layers, as an alternative or companion process to sputtering.

[40] **Figure 6** is a diagram of a typical sublimation chamber 600 modified to include an energy source according to one embodiment of the system and method for laser assisted deposition. Sublimation chamber 600 comprises crucible 610, sublimation material 620, energy source 630, and vacuum outtake 660. Sublimation material 620 can be, for instance, solid state CdTe for use in depositing a CdTe thin film onto substrate 170, according to one embodiment. Sublimation can also be carried out using pure cadmium and pure telluride rather than depositing compound CdTe. Sublimation in this manner could require two crucibles 610 to separately store the cadmium and the telluride.

[41] Sublimation includes converting a substance directly from a solid to a gas. Solid material 620 is thus converted to a gas 670 in chamber 600 wherein appropriate vacuum pumps are attached to chamber 600.

[42] Energy source 630 simultaneously anneals gas particles 670 concurrent with their deposition onto substrate 170. As before, energy source 610 can be a maser or laser or any other source regardless of categorization by active medium or wavelength. Continuous wave, rasterized, or pulsed energy is likewise acceptable.

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[43] Temperature control can be accomplished using a cooling circuit that would maintain a temperature differential at substrate 170 in order to prevent damage to substrate 170. Cooling is also critical during sublimation to ensure that the deposited layer of gas particles 670 are annealed without causing harm to substrate 170.

[44] One or more metallization layers using the systems and methods for laser assisted deposition may also be necessary to provide current collection for the cells. Metallization layers as well as semiconductor layers may be deposited using sublimation. Proof-of-principle lab results have yielded solar cells built on high temperature flexible substrates such as mylar, tedlar, teflon, and tefzel using the techniques described herein. By flexible is meant a sheet of finished cells that can be rolled to a minimum inside radius of about four inches such that when unrolled, the cells will not suffer degradation or damage. Also, the selection of a very heat tolerant substrate will produce a cell with higher efficiency because it is possible to raise annealing temperature to higher levels.

[45] The description and drawings contained herein represent the presently preferred embodiment of the invention and are, as such, a representative of the subject matter which is broadly contemplated by the present invention. The scope of the present invention fully encompasses other embodiments that may become obvious to those skilled in the art, and the scope of the present invention is accordingly limited by nothing other than the appended claims.

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WHAT IS CLAIMED IS

1. A system for depositing a thin film comprising:

a chamber having a cathode and an anode for generating an electric field therebetween;

a gas intake for injecting an inert gas into the chamber;

a target material affixed to the cathode and exposed to the inert gas whereby positively charged inert gas particles dislodge particles from the target material;

an energy source for generating energy inside the chamber; and

a substrate affixed to the anode on which substrate the dislodged particles from the target material are deposited to form the thin film and on which the energy from the energy source simultaneously anneals the thin film without damaging the substrate.

2. The system of claim 1, wherein the cathode contains magnets.

3. The system of claim 1, wherein the electric field is an RF (radio frequency) field.

4. The system of claim 1, wherein the electric field is a DC (direct current) field.

5. The system of claim 1, wherein the energy source is a laser.

6. The system of claim 5, wherein the laser is a pulsed laser.

7. The system of claim 6, wherein the pulsed laser is activated for a duration short enough to avoid damaging the substrate.

8. The system of claim 5, wherein the laser is a continuous wave laser.

9. The system of claim 8, wherein the continuous wave laser is scanned back and forth over an upper surface of the thin film to avoid damaging the substrate.

10. The system of claim 1, wherein the inert gas is argon (Ar).

11. The system of claim 1, further comprising a pump for creating and maintaining vacuum conditions in the chamber.

12. The system of claim 1, further comprising a vacuum outtake for removing excess matter from the chamber.

13. The system of claim 1, further comprising a cooling circuit for controlling the temperature of the substrate.

14. The system of claim 1, wherein the substrate is plastic.

15. The system of claim 14, wherein the plastic substrate is one of the group consisting of tedlar, tefzel, mylar, and teflon.

16. The system of claim 1, wherein the target material is a semiconductor.

17. The system of claim 16, wherein the semiconductor target material is one of the group consisting of cadmium telluride (CdTe) and cadmium sulfide (CdS).

18. The system of claim 1, wherein the target material is a metal.

19. The system of claim 18, wherein the metal target material is one of the group consisting of indium-tin-oxide (ITO), copper (Cu), and silver (Ag).

20. A system for depositing a thin film comprising:

a chamber;

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a crucible housed within the chamber for storing a sublimation material;

an energy source for generating energy inside the chamber; and

a substrate mounted in the chamber, on which substrate gas particles from the sublimation material are deposited to form the thin film and on which the energy from the energy source simultaneously anneals the thin film without damaging the substrate.

21. The system of claim 20, wherein the energy source is a laser.

22. The system of claim 21, wherein the laser is a pulsed laser.

23. The system of claim 22, wherein the pulsed laser is activated for a duration short enough to avoid damaging the substrate.

24. The system of claim 21, wherein the laser is a continuous wave laser.

25. The system of claim 20, further comprising a pump for creating and maintaining vacuum conditions in the chamber.

26. The system of claim 20, further comprising a vacuum outtake for removing excess matter from the chamber.

27. The system of claim 20, further comprising a cooling circuit for controlling the temperature of the substrate.

28. The system of claim 20, wherein the substrate is plastic.

29. The system of claim 20, wherein the sublimation material is a semiconductor.

30. The system of claim 29, wherein the semiconductor material is cadmium telluride (CdTe).

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31. A method of depositing a thin film comprising:
sputtering a thin film of material onto a substrate; and
simultaneously directing energy from an energy source at the thin film for annealing of the thin film.

32. The method of claim 31, wherein the substrate is a polymer or plastic.

33. The method of claim 31, wherein the energy source is a laser.

34. The method of claim 33, wherein the laser is a pulsed laser.

35. The method of claim 33, wherein the laser is a continuous wave laser.

36. The method of claim 31, wherein energy from the energy source is directed at the thin film and is at a temperature below the critical temperature of the substrate to avoid damaging the substrate.

37. The method of claim 31, wherein the thin film of material is a semiconductor.

38. The method of claim 37, wherein the semiconductor is one of the group consisting of cadmium telluride (CdTe) and cadmium sulfide (CdS).

39. The method of claim 31, wherein the thin film of material is a metal.

40. The method of claim 39, wherein the metallization layer is one of the group consisting of Indium-Tin-Oxide (ITO), Copper (Cu), and Silver (Ag).

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41. The method of claim 31, wherein the steps of sputtering the thin film and directing an energy source both occur in a process chamber having a cathode and an anode for creating an electric field therebetween.

42. The method of claim 41, wherein the electric field is an RF (radio frequency) field.

43. The method of claim 41, wherein the electric field is a DC (direct current) field.

44. A method of depositing a thin film comprising:

sublimating a thin film of material onto a substrate; and

simultaneously directing energy from an energy source at the thin film for annealing of the thin film.

45. The method of claim 44, wherein the substrate is a polymer or plastic.

46. The method of claim 44, wherein the energy source is a laser.

47. The method of claim 46, wherein the laser is a pulsed laser.

48. The method of claim 46, wherein the laser is a continuous wave laser.

49. The method of claim 44, wherein energy from the energy source is directed at the thin film and is at a temperature below the critical temperature of the substrate to avoid damaging the substrate.

50. The method of claim 44, wherein the thin film of material is a semiconductor.

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51. The method of claim 50, wherein the semiconductor is cadmium telluride (CdTe).

52. The method of claim 44, wherein the thin film of material is a metal.

53. The method of claim 52, wherein the metal is one of the group consisting of Indium-Tin-Oxide (ITO), Copper (Cu), and Silver (Ag).

54. A method of manufacturing solar cells comprising the steps of:

depositing a semiconductor layer onto a substrate;

simultaneously annealing the semiconductor layer as the layer is deposited on the substrate by directing energy from an energy source onto the semiconductor layer; and

depositing a current-collecting metallization layer onto the semiconductor layer or substrate.

55. The method of claim 54, wherein simultaneously annealing comprises directing the energy from the energy source onto the semiconductor layer for a duration long enough to noticeably increase the grain size of the semiconductor layer.

56. The method of claim 54, wherein the energy source is a laser.

57. The method of claim 54, wherein the substrate is plastic.

58. The method of claim 57, wherein the plastic substrate is one of the group consisting of mylar, tedlar, teflon, and tefzel.

59. A solar cell comprising:

a flexible substrate;

an n-type window layer deposited at a temperature sufficiently low so as not to damage the substrate; and

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a p-type absorption layer deposited using sublimation at a temperature sufficiently low so as not to damage the substrate.

60. The solar cell of claim 59, wherein the p-type absorption layer comprises cadmium telluride deposited at a temperature sufficiently low to avoid crystallization of the cadmium telluride.

61. The solar cell of claim 59, wherein the n-type window layer comprises cadmium sulfide sputter deposited at a temperature sufficiently low to avoid crystallization of the cadmium sulfide.

62. A thin film flexible solar cell comprising:

a plastic or polymer substrate;

a thin film of n-type cadmium sulfide deposited at a temperature sufficiently low so as not to damage the substrate; and

a comparatively thicker film of p-type cadmium telluride deposited using sublimation at a temperature sufficiently low so as not to damage the substrate.

63. A thin film flexible solar cell comprising:

a flexible substrate;

a current collection layer deposited onto the substrate;

an n-type semiconductor film that is deposited onto the current collection layer and has an amorphous atomic structure;

a p-type semiconductor film having a bandgap energy less than the n-type semiconductor film that is deposited using sublimation onto the n-type semiconductor film and has an amorphous atomic structure; and

a metallization layer deposited onto the p-type semiconductor film.

64. The thin film flexible solar cell of claim 61 wherein:

the substrate is a transparent polymer or plastic;

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the n-type semiconductor film is cadmium sulfide deposited at a temperature sufficiently low to avoid melting or damaging the substrate; and

the p-type semiconductor film is cadmium telluride deposited at a temperature sufficiently low to avoid melting or damaging the substrate.

65. A thin film flexible solar cell comprising:

a flexible substrate;

a metallization layer deposited onto the substrate;

a p-type semiconductor film that is deposited using sublimation onto the metallization layer and has an amorphous atomic structure;

an n-type semiconductor film having a bandgap energy greater than the p-type semiconductor film that is deposited onto the p-type semiconductor layer and has an amorphous atomic structure; and

a current collection layer deposited onto the n-type semiconductor film.

66. The thin film flexible solar cell of claim 65 wherein:

the substrate is a transparent polymer or plastic;

the p-type semiconductor film is cadmium telluride deposited at a temperature sufficiently low to avoid melting or damaging the substrate; and

the n-type semiconductor film is cadmium sulfide sputter deposited at a temperature sufficiently low to avoid melting or damaging the substrate.

67. A method for manufacturing a thin film flexible solar cell comprising the following steps:

(a) providing a plastic or polymer substrate;

(b) depositing a layer of an n-type semiconductor on the substrate at a temperature sufficiently low to avoid melting or damaging the substrate; and

(c) sublimating a layer of a p-type semiconductor on the n-type semiconductor layer at a temperature sufficiently low to avoid melting or damaging the substrate.

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68. The method of claim 67, wherein:

after step (a), a transparent conductive oxide layer is deposited on the substrate and a metal bar bus network is deposited on the transparent conductive oxide layer; and

after step (c), a metallization layer is deposited on the p-type semiconductor layer.

69. The method of claim 68, wherein the n-type semiconductor is cadmium sulfide and the p-type semiconductor is cadmium telluride.

70. A method for manufacturing a thin film flexible solar cell comprising the following steps:

(a) providing a plastic or polymer substrate;

(b) sublimating a layer of a p-type semiconductor on the substrate at a temperature sufficiently low to avoid melting or damaging the substrate; and

(c) depositing a layer of an n-type semiconductor on the p-type semiconductor at a temperature sufficiently low to avoid melting or damaging the substrate.

71. A method as claimed in claim 70, wherein steps (b) and (c) are carried out at a temperature sufficiently low to avoid crystallization of the semiconductors.

72. A method as claimed in claim 70, wherein the p-type semiconductor is cadmium telluride and the n-type semiconductor is cadmium sulfide.

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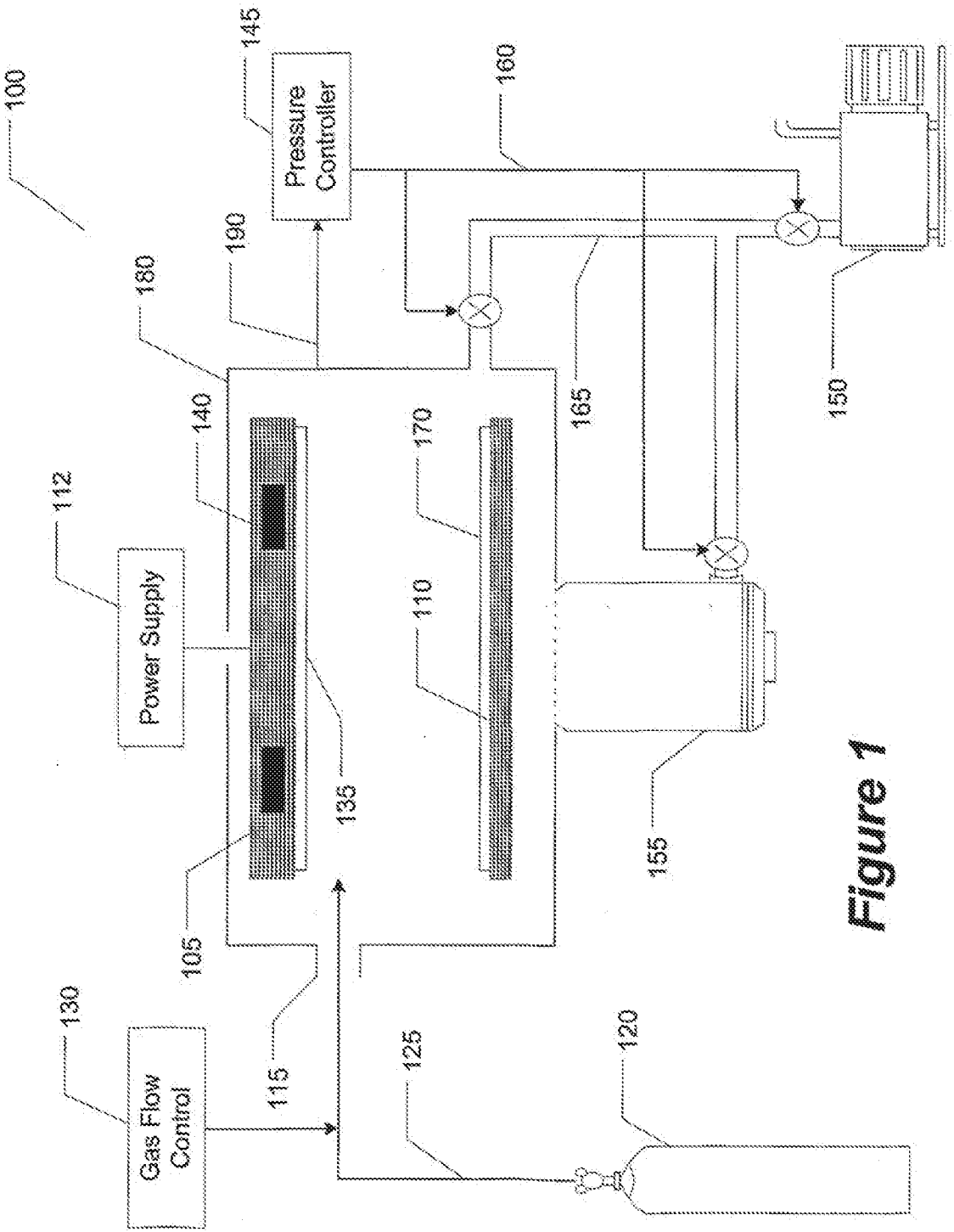


Figure 1

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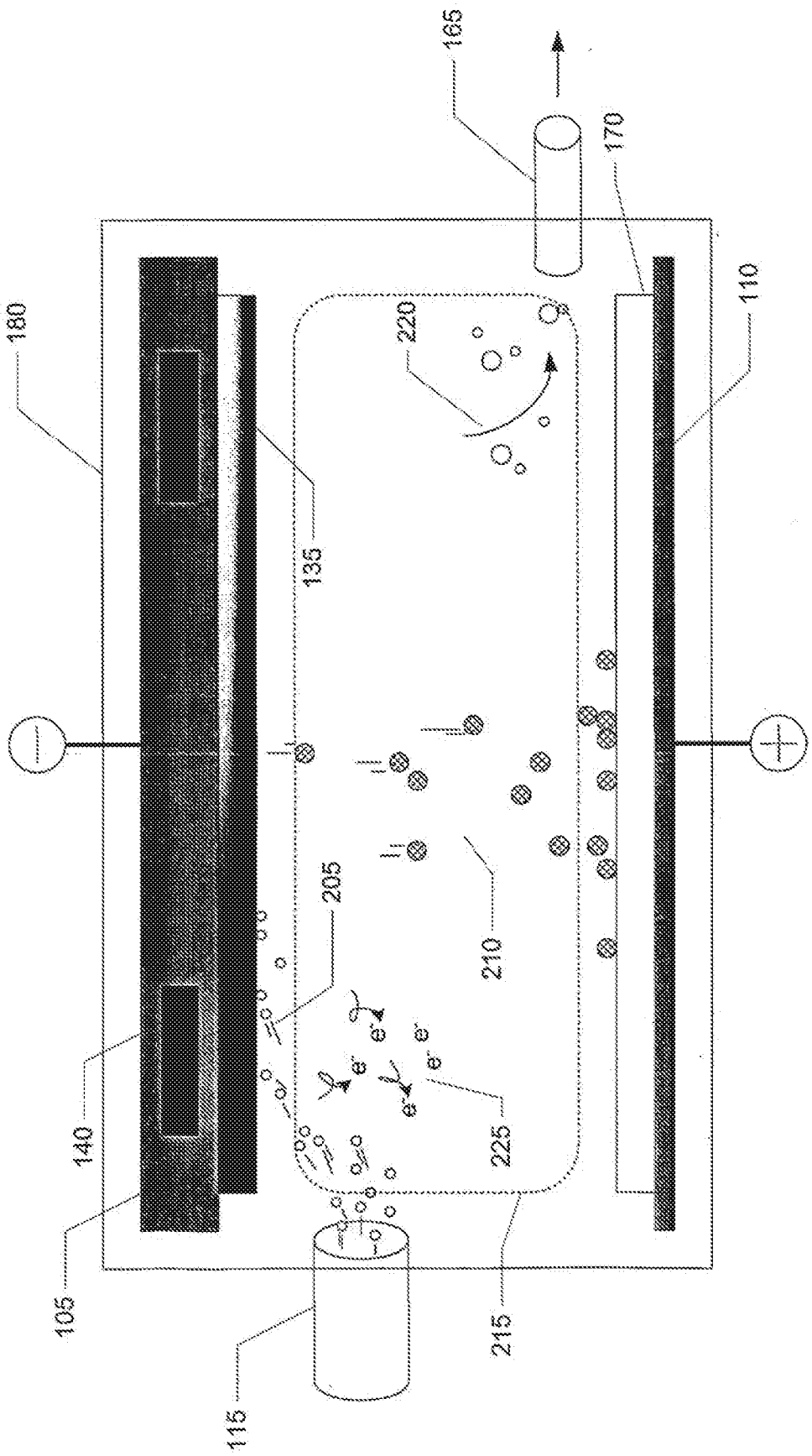


Figure 2

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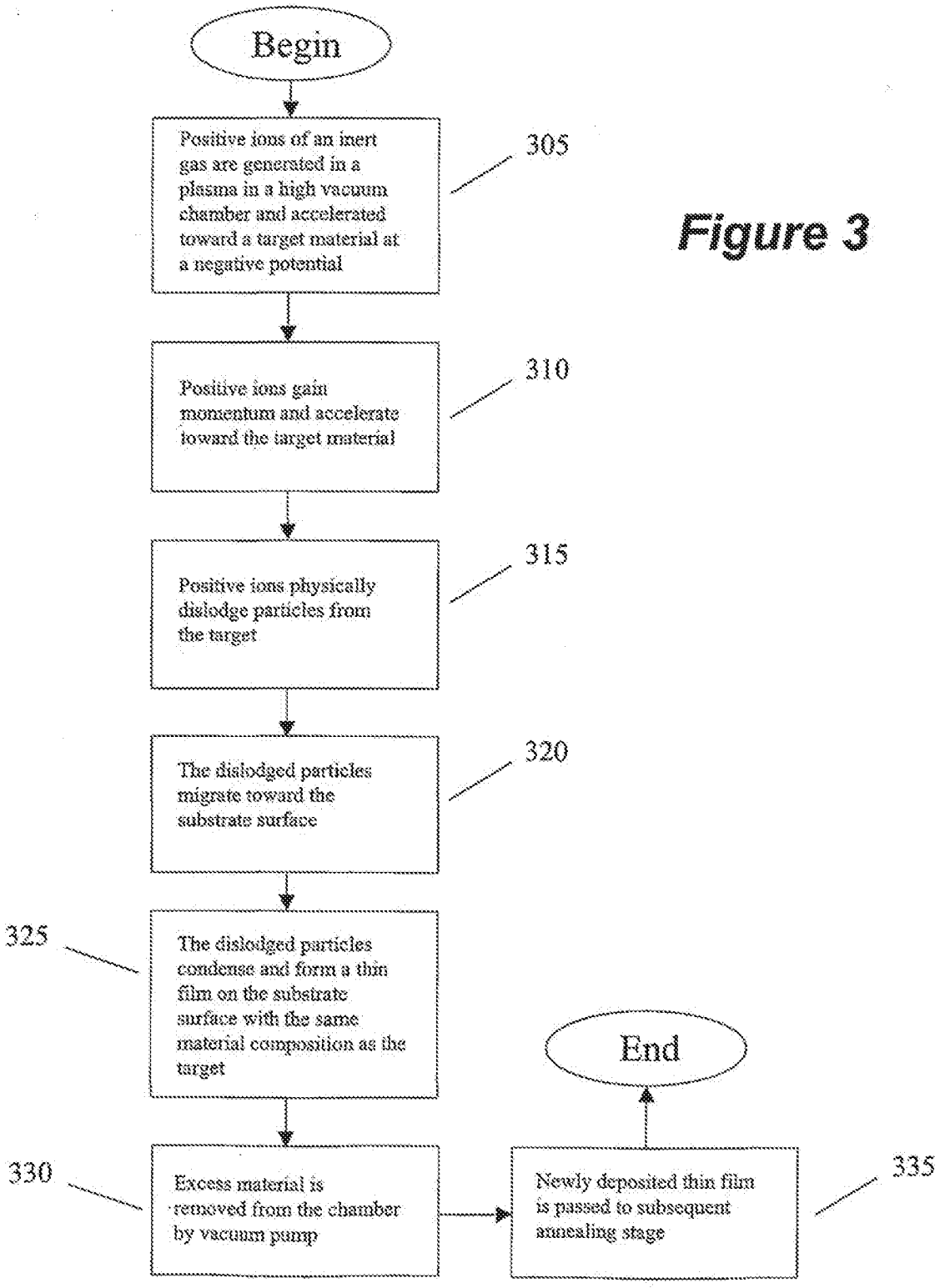


Figure 3

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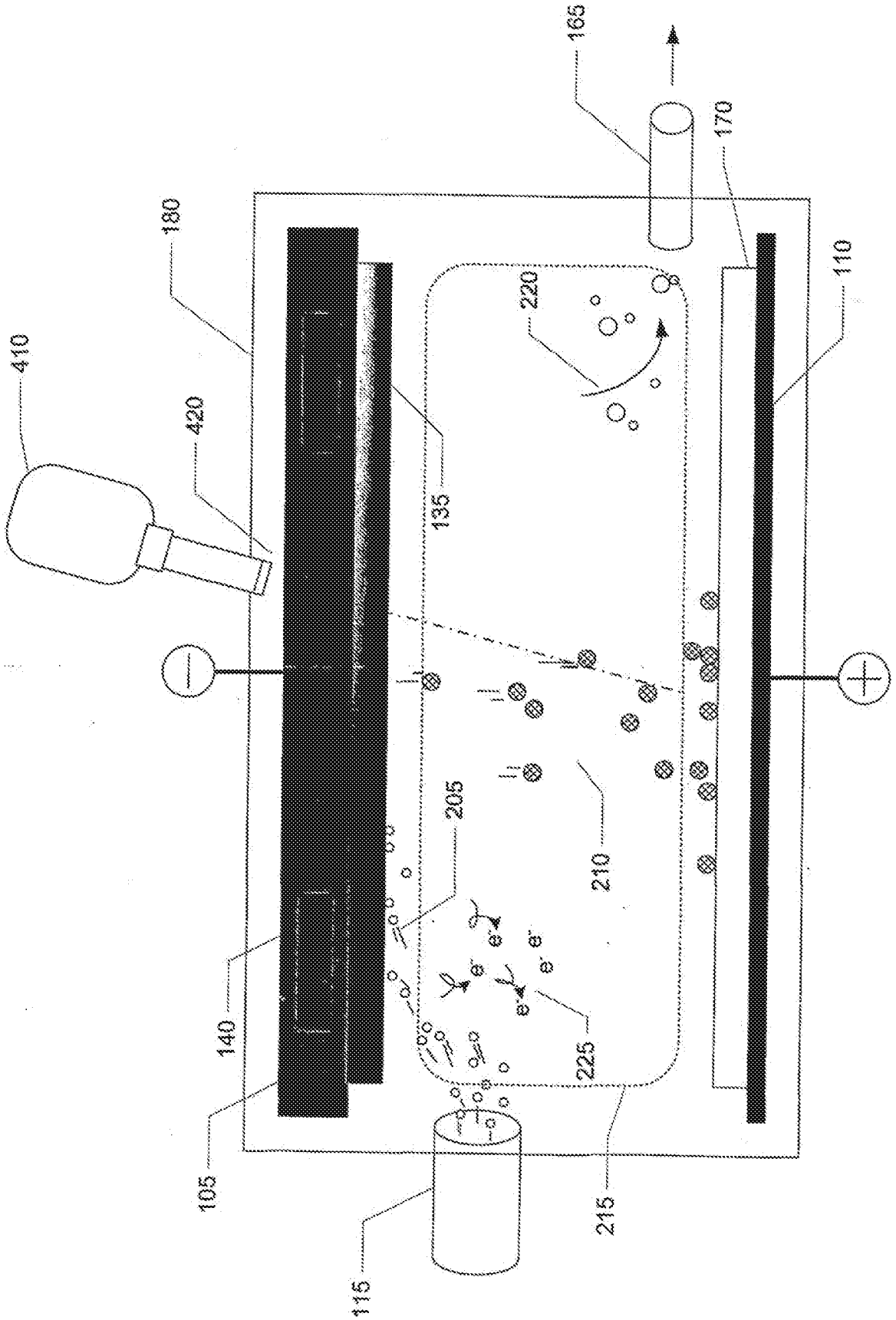


Figure 4

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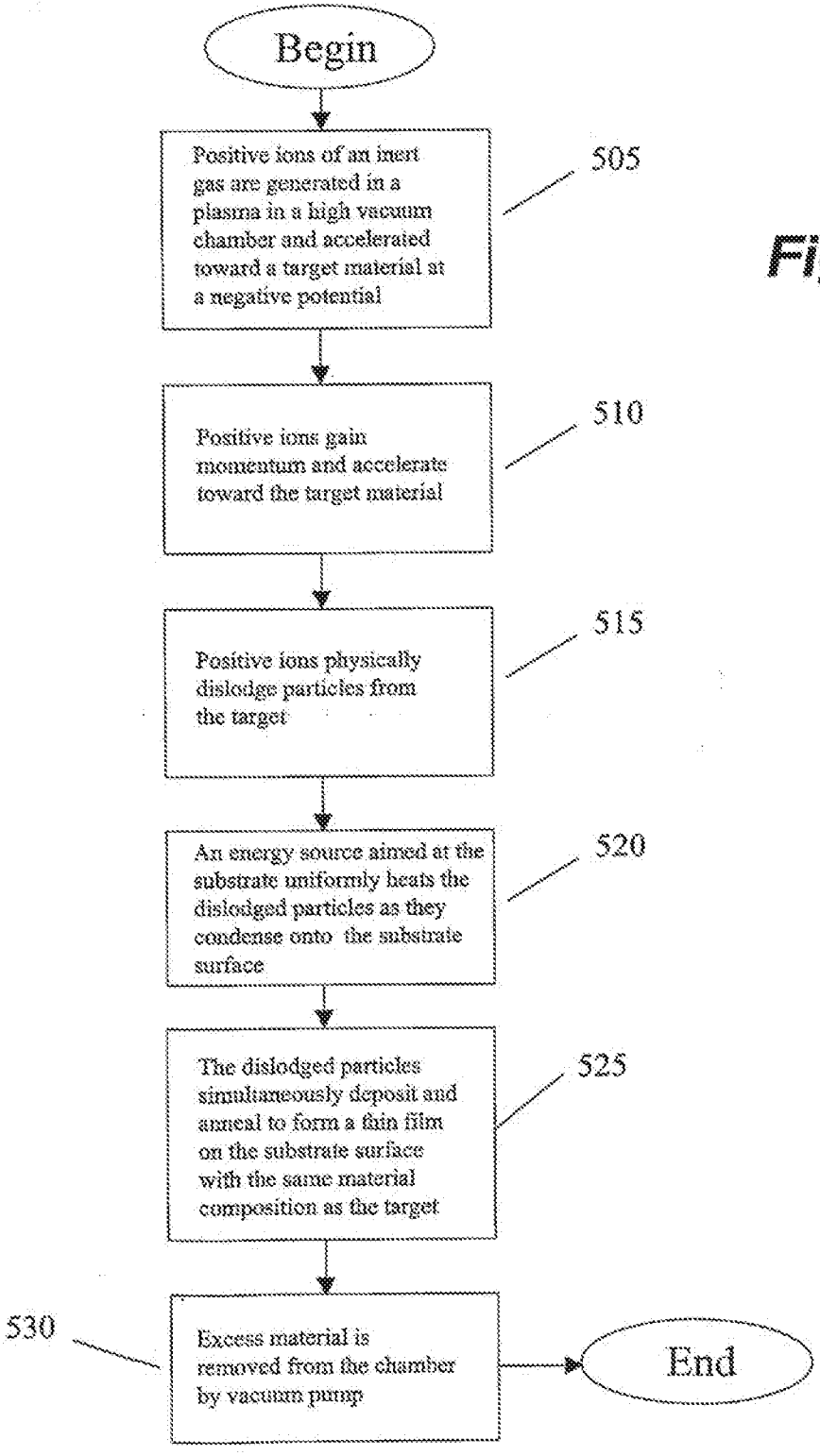


Figure 5

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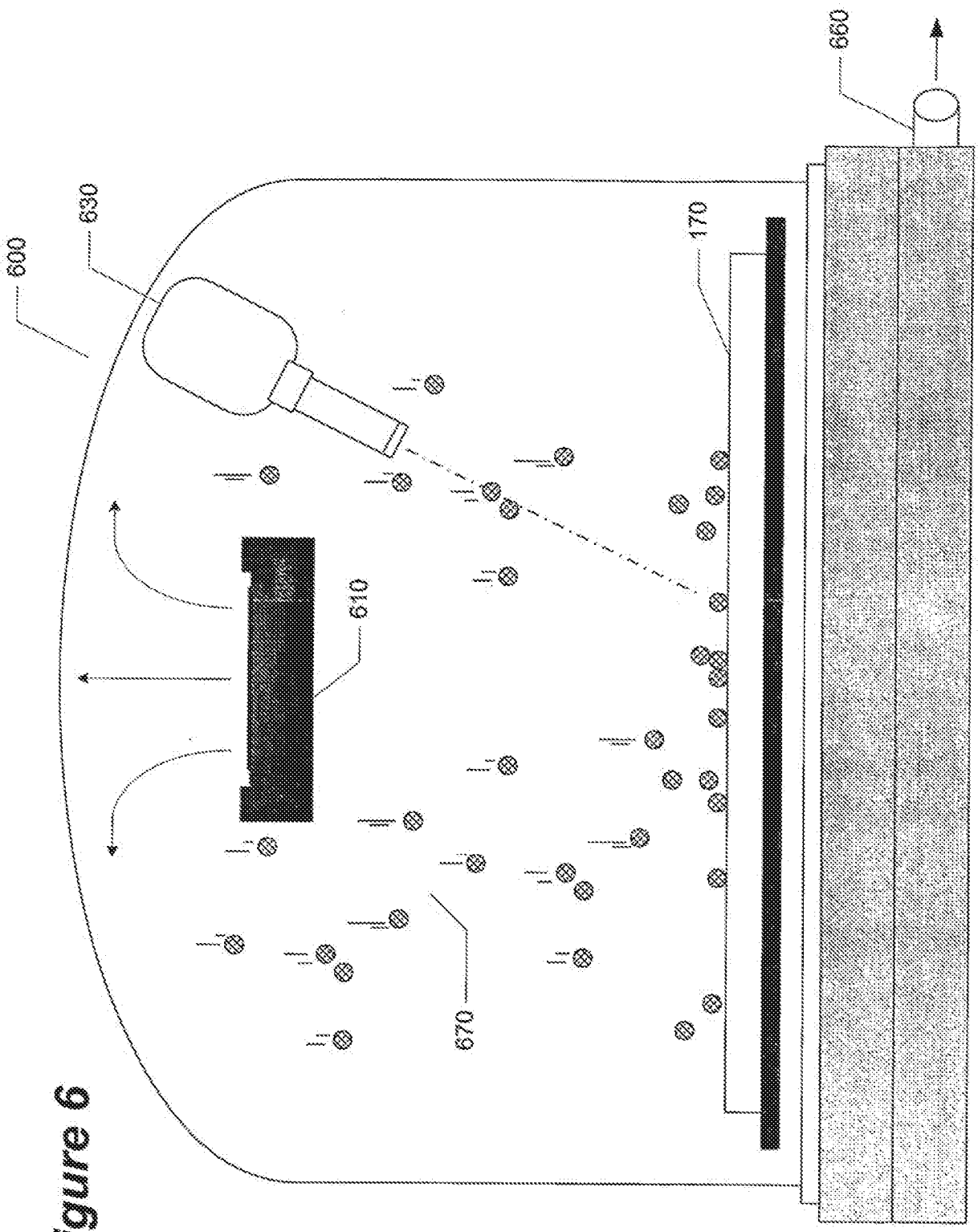


Figure 6

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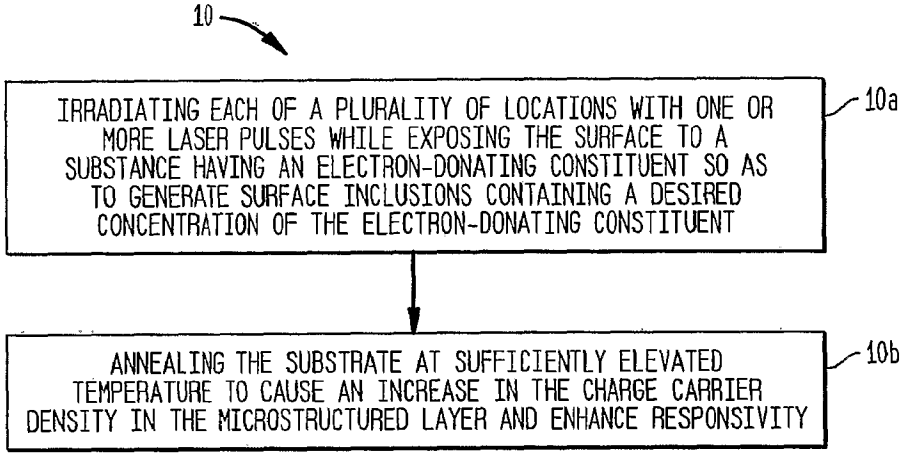
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(54) Title: MANUFACTURE OF SILICON-BASED DEVICES HAVING DISORDERED SULFUR-DOPED SURFACE LAYERS



(57) Abstract: The present invention provides methods of fabricating a radiation-absorbing semiconductor wafer by irradiating at least one surface location of a silicon substrate, e.g., an n-doped crystalline silicon, by a plurality of temporally short laser pulses, e.g., femtosecond pulses, while exposing that location to a substance, e.g., SF_6, having an electron-donating constituent so as to generate a substantially disordered surface layer (i.e., a microstructure layer) that incorporates a concentration of that electron -donating constituent e.g., sulfur. The substrate is also annealed at an elevated temperature and for a duration selected to enhance the charge carrier density in the surface layer. For example, the substrate can be annealed at a temperature in a range of about 700 K to about 900 K.

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MANUFACTURE OF SILICON-BASED DEVICES HAVING DISORDERED SULFUR-DOPED SURFACE LAYERS

Federally Sponsored Research

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Related Applications

The present application is a continuation-in-part (CIP) of co-pending patent application entitled "Systems and Methods for Light Absorption and Field Emission Using Microstructured Silicon," filed on May 24, 2002, and having a Serial No. 10/155,429, which is herein incorporated by reference in its entirety.

Background of the Invention

The present invention relates generally to methods for fabricating radiation-absorbing semiconductor wafers, and more particularly, to methods for fabricating silicon wafers that can absorb radiation and exhibit diodic current-voltage characteristics.

Modern semiconductor circuits are predominantly based on silicon, which can be readily procured at a lower cost than any other semiconductor and can be easily oxidized. Further, a band gap of 1.05 eV renders silicon suitable for detection of visible light and conversion of sunlight into electricity. Silicon, however, has several shortcomings. For example, it is an indirect band-gap material, and hence it is a relatively poor light emitter. In addition, silicon is not particularly suitable for use in detecting radiation having long wavelengths, such as, infrared radiation employed for telecommunications. Although other semiconductor materials are available that can detect long wavelength radiation better than silicon, they are generally more costly and cannot be readily integrated in optoelectronic circuits that are primarily silicon-based.

Hence, there is a need for silicon-based semiconductor structures and wafers with enhanced radiation-absorbing properties, particularly in wavelengths beyond the band-gap of crystalline silicon. There is also a need for such wafers that can be utilized

in fabricating photodetectors that exhibit enhanced responsivity in detecting radiation over a wide wavelength range. Further, there is a need for methods of manufacturing such silicon-based wafers.

Summary of the Invention

In one aspect, the present invention provides a method of fabricating a radiation-absorbing semiconductor wafer by irradiating at least one surface location of a silicon substrate, e.g., a crystalline silicon, with a plurality of temporally short laser pulses while exposing that location to a substance having an electron-donating constituent so as to generate a substantially disordered surface layer that incorporates a desired concentration of the electron-donating constituent, e.g., a concentration in a range of about 0.5 atom percent to about 5 atom percent, or from about 0.5 atom percent to about 1 atom percent. The substrate is preferably annealed at an elevated temperature and for a duration selected to enhance charge carrier density, e.g., electron carrier density, in the disordered surface layer.

In a related aspect, an annealing temperature and duration can be selected to cause re-arrangement of atomic bonds in the surface layer so as to increase the concentration of free electrons in the surface layer. Further, the annealing temperature and duration can be selected to cause the surface layer to form a diode junction, e.g., a p-n junction, with the underlying silicon substrate. The term "diode junction" is known in the art and generally refers to a junction that can exhibit current rectification (e.g., a junction that exhibits drastically different conductivities in one bias direction relative to the other). Moreover, the annealing temperature and duration can be selected such that the annealed substrate would exhibit a responsivity in a range of about 1 Ampere/Watt (A/W) to about 200 A/W, or preferably in a range of about 10 A/W to about 200 A/W, upon exposure of the surface layer to visible radiation having wavelengths in a range of about 250 nm to about 1050 nm and application of a reverse bias in a range of about 0.1 V to about 15 V, or about 0.5 to about 15 V, to the substrate. Further, the annealing temperature and duration can be selected such that the annealed substrate will exhibit a responsivity in a range of about 0.1 Ampere/Watt (A/W) to about 100 A/W upon exposure of the surface layer to visible radiation having at least a wavelength in a range

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of about 1050 nm to about 3500 nm and application of a reverse bias in a range of about 0.1 V to about 15 V to the substrate.

In a related aspect, the laser pulses irradiating the substrate's surface have pulse widths in a range of about a few nanoseconds to about 10 femtoseconds, and more preferably in a range of about 50 to about 500 femtoseconds. The laser pulse fluences can range from about 1 kJ/m^2 to about 30 kJ/m^2, or from about 3 kJ/m^2 to about 15 kJ/m^2, or from about 3 to about 8 kJ/m^2. The annealing temperature can be in a range of about 500 K to about 1100 K, preferably in a range of about 500 K to about 900 K, and more preferably in a range of about 700 K to about 900 K, and the annealing duration can be from about a few seconds to about a few hours.

In another aspect, the substance containing an electron-donating constituent can be a gas, a fluid or a solid. Some examples of such substances include, without limitation, SF_6, H_2S, Cl_2, and N_2. For example, when SF_6 is utilized, the exposure of the silicon surface to the laser pulses generates sulfur inclusions in a surface layer of the substrate. The silicon substrate is preferably n-doped, but it can also be p-doped. The substrate's bulk doping level can be in a range of about 10^{11} to about 10^{18} cm^{-3}.

In another aspect, the present invention provides a method of fabricating a radiation-absorbing semiconductor structure that calls for irradiating each of a plurality of locations on a surface of a silicon substrate with one or more femtosecond laser pulses while exposing the surface to a sulfur-containing substance so as to generate a plurality of sulfur inclusions in a surface layer of the substrate. The substrate is annealed at a temperature in a range of about 500 K to about 1100 K for a time duration in a range of about a few seconds to about a few hours. The annealing step can be performed subsequent to, or simultaneously, with irradiation of the substrate's surface with laser pulses. Further, the annealing step can be performed in an inert atmosphere or in vacuum (i.e., a low-pressure atmosphere).

In a related aspect, the light emitted in each laser pulse can have a narrow spectrum and a central wavelength in a range of about 200 nm to about 1200 nm (e.g., 800 nm or 1064 nm), fluences in a range of about 1 kJ/m^2 to about 30 kJ/m^2, and more preferably in a range of about 1 kJ/m^2 to about 10 kJ/m^2 ,and a repetition rate in a range of about 1 kHz to about 50 MHz, or in a range of about 1 kHz to about 1 MHz.

In another aspect, the invention provides a method of fabricating a semiconductor wafer by irradiating a plurality of locations on a surface of a silicon substrate with one or more laser pulses having pulse widths in a range of about 50 to about 500 femtoseconds while exposing the surface to a substance having an electron-donating constituent so as to generate a microstructured surface comprising inclusions that incorporate the electron-donating constituent. The laser pulses can be directed at the substrate in a direction forming a selected angle relative to the substrate's surface, e.g., normal to the surface. The substrate is annealed at an elevated temperature in range of about 500 K to about 1100 K for a selected time duration, e.g., in a range of about a few seconds to about a few hours. In certain applications, the annealing temperature can be between about 500 K and 1000 K, and more preferably between 575 K and 875 K.

In another aspect, the invention provides a method of fabricating a semiconductor wafer by irradiating at least one location on a surface of a silicon substrate with temporally short laser pulses, e.g., femtosecond pulses, while exposing the surface to a substance having an electron-donating constituent so as to generate a microstructured surface layer having inclusions containing the electron-donating constituent. The substrate can be annealed, either following the laser irradiation or simultaneous therewith, at a temperature and for a duration selected to enhance the responsivity of the microstructured substrate to electromagnetic radiation having at least one wavelength in a range of about 250 nm to about 1100 nm by a factor of about 10, or preferably about 20, or more preferably about 100, relative to a similarly microstructed substrate but without annealing. The responsivity can be measured upon application of a reverse bias voltage in a range of about 0.5 V to about 15 V to the substrate. A suitable annealing temperature for effecting such enhancement of the wafer's responsivity lies in a range of about 600 K to about 900 K, and more preferably in a range of about 700 K to about 900 K, and a suitable annealing duration lies in a range of about a few seconds to about a few hours.

In another aspect, the present invention provides a photodetector that includes a silicon substrate having a surface layer, configured for exposure to external radiation, that is doped with sulfur inclusions with an average concentration in a range of about 0.5 atom percent to about 5 atom percent so as to exhibit a diodic current-voltage characteristic. The photodetector further includes a plurality of electric contacts, e.g., in

the form of metallic coatings, that are disposed on selected portions of the substrate for applying a selected reverse bias voltage, e.g., in a range of about 0.1 to about 15 volts, to the surface layer for facilitating generation of an electrical signal, e.g., a photocurrent, in response to exposure of the surface layer to electromagnetic radiation. The surface layer is configured such that an electrical signal in response to an incident radiation having at least a wavelength in a range of about 250 nm to about 1050 nm can be generated at a responisivity greater than about 1 A/W. Preferably, the responsivity over the entire range of about 250 nm to about 1050 nm is greater than about 1 A/W. For example, the responsivity to at least one wavelength in this wavelength span, and preferably to all wavelengths in this span, can be in a range of about 1 A/W to about 100 A/W, or in a range of about 10 A/W to about 100 A/W, or in a range of about 10 A/W to about 200 A/W.

In another aspect, the photodetector can exhibit an average responsivity (i.e., responsivity averaged over a wavelength range) to wavelengths in a range of about 250 nm to about 1050 nm that is greater than about 1 A/W, e.g., an average responsivity in a range of about 1 A/W to about 100 A/W, or an average responsivity in a range of about 10 A/W to about 200 A/W.

In another aspect, the photodetector can exhibit a responsivity greater than about 1 A/W (e.g., in a range of about 1 A/W to about 100 A/W) for wavelengths in a range of about 250 nm to about 600 nm, as well as in a range of about 600 nm to about 1050 nm. In a related aspect, the photodetector can exhibit a responsivity greater than about 0.1 A/W for incident radiation having at least one wavelength in a range of about 1050 nm to about 2000 nm, and preferably in a range of about 1050 nm to about 3500 nm. Preferably, the photodetector's responsivity to all wavelengths in this range (about 1050 nm to about 3500 nm) is greater than about 0.1 A/W. For example, the detector's responsivity in this wavelength span can be in a range of about 0.1 A/W to about 100 A/W.

In another aspect, the photodetector can exhibit an average responsivity greater than about 0.1 A/W (e.g., a responsivity in a range of about 0.1 A/W to about 100 A/W) for radiation having wavelengths in a range of about 1050 nm to about 2000 nm, and preferably in a range of about 1050 nm to about 3500 nm.

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Photodetectors according to the teachings of the invention, such as those described above, provide a marked improvement over conventional silicon photodiodes where responsivities greater than 1 A/W for wavelengths in a range of about 250 nm to about 1050 nm are unknown. Further, responsivities of conventional silicon photodiodes degrade drastically for wavelengths beyond 1050 nm, and are significantly less than those that can be achieved by photodetectors of the present invention.

In another aspect, the surface layer can have a thickness in a range of about 10 nanometers to about 1 micron, and a microstructured morphology. For example, the microstructured layer can be formed by a plurality of conical microstructures, each of which can be composed of a core silicon portion forming a junction with a surface portion that is doped with sulfur. A term "conical structure or microstructure" as used herein refers to a generally cone-like or columnar protrusion above the silicon surface that can have vertical walls, or slanted walls that taper in the vertical direction. The microstructures can have a height in a range of about 0.5 micron to about 30 microns protruding from a base portion on the surface of the silicon substrate to a tip portion having a radius of curvature of about a few hundred nanometers. The gradient of sulfur concentration across the junction is substantially abrupt, although in some cases it can be gradual with the core portion having some sulfur dopants. The sulfur-doped surface layer can comprise silicon nanocrystals having diameters in a range of about 10 about 50 nanometers.

In another aspect, the invention provides a photodetector that includes a silicon substrate having a microstructured layer incorporating inclusions containing an electron-donating constituent. The microstructured layer is adjacent an underlying bulk silicon portion and forms a diode junction therewith. The term "diode junction" is known in the art and generally refers to a junction that can exhibit current rectification (e.g., a junction that exhibits drastically different conductivities in one bias direction relative to the other). A well-known example of a diode junction is a p-n junction. An electrical contact is disposed on a surface portion of the microstructured layer such that at least another surface portion of that layer remains available for receiving incident electromagnetic radiation. The photodetector can further include another electrical contact disposed on a surface of the bulk silicon portion opposed to the microstructured layer. The electrical contact layers allow application of a reverse bias voltage to the

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substrate to facilitate generation of an electrical signal, e.g., a photocurrent, in response to exposure of the microstructured layer to incident radiation having wavelengths in range of about 250 nm to about 1050 nm at a responsivity in a range of about 1 A/W to about 200 A/W.

In a related aspect, the substrate can generate a photocurrent in response to irradiation of the microstructured layer with radiation having wavelengths in a range of about 1050 nm to about 3500 nm at a responsivity in a range of about 0.1 A/W to about 100 A/W.

In another aspect, the electron-donating constituent can be, for example, sulfur, chlorine or nitrogen, and can be present in the microstructured layer at a concentration in a range of about 0.5 to about 5 atom percent, or in a range of about 0.5 to about 1.5 atom percent, or in a range of about 0.5 to about 1 atom percent.

In another aspect, the present invention provides a photodetector for use in the visible and the infrared regions of the electromagnetic spectrum that includes a crystalline silicon substrate having a microstructured surface layer characterized by a plurality of substantially conical microstructures. The microstructured layer includes a doped layer having a plurality of silicon nanocrystals that contain an electron-donating dopant, such as sulfur, chlorine or nitrogen, with an average concentration in a range of about 0.5 to about 1.5 atom percent. The microstructured layer exhibits a diodic current-voltage curve and is configured to receive an external radiation. A plurality of electrical contacts are disposed on selected portions of the substrate for applying a reverse bias voltage to the microstructured layer in order to facilitate generation of an electrical signal in response to irradiation of at least a portion of that layer. The photodetector exhibits a responsivity greater that about 1 amperes/watt (A/W) for radiation wavelengths in a range of about 250 nm to about 1050 nm and a responsivity greater than about 0.1 amperes/watt for radiation wavelengths in a range of about 1050 nm to about 3500 nm.

Further understanding of the invention can be obtained by reference to the following detailed description in conjunction with the associated drawings, which are briefly described below.

Brief Description of the Drawings

FIGURE 1 is a flow chart depicting various steps in an exemplary embodiment for generating a microstructured silicon wafer suitable for absorbing radiation,

FIGURE 2 is a schematic diagram of an exemplary apparatus for microstructuring silicon wafers in accordance with one aspect of the invention,

FIGURE 3 is a scanning electron micrograph of a silicon surface, obtained at a 45-degree angle relative to the surface, after irradiation of the surface with 100 fsec pulses having a central wavelength of 800 nm and a fluence of about 5 kJ/m^2,

FIGURE 4 schematically illustrates an experimental set-up for performing resistivity and Hall effect measurements on a silicon sample microstructured in accordance with the teachings of the invention,

FIGURE 5 presents a plurality of graphs depicting wavelength absorptance of prototype microstructured silicon wafers as a function of an average number of 100 laser shots (8 kJ/m^2) per location employed for microstructuring the wafers in the presence of SF_6,

FIGURE 6 presents a plurality of graphs depicting wavelength dependence of absorptance of a plurality of prototype silicon wafers annealed at different temperatures subsequent to their microstructuring by a plurality of femtosecond laser pulses (the room temperature (300 K) data corresponds to a wafer that was not annealed),

FIGURE 7 presents graphs depicting wavelength dependence of absorptance for exemplary femtosecond-laser-formed and nanosecond-laser-formed microstuctured silicon wafers, before and after thermal annealing at 875 K for about 30 minutes (the absorptance of an unstructured silicon substrate as a function of wavelength is also shown for comparative purposes),

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FIGURE 8A presents graphs depicting absorptance as a function of wavelength for a plurality of prototype silicon wafers microstructured by exposure to 500 laser shots of femtosecond pulses (fluence of 8 kJ/m^2) in the presence of different gases in the absence of annealing (the graph designated vacuum relates to wafer microstructured in a vacuum chamber at a base pressure less than about 10^{-6} bar),

FIGURE 8B presents absorptance data as a function of wavelength for a plurality of prototype silicon wafers microstructured by exposure to 500 shots of 100 femtosecond laser pulses (fluence of 8 kJ/m^2 in the presence of sulfur-bearing and non-sulfur-bearing gases) indicating the positive effects of sulfur incorporation in enhancing below band-gap absorptance,

FIGURE 9 presents graphs depicting wavelength dependence of absorptance for a plurality of prototype silicon wafers microstructured by femtosecond laser pulses in the presence of SF_6 at different partial pressures,

FIGURE 10 schematically illustrates a p-n junction in thermal equilibrium,

FIGURE 11A is a perspective view of a photodetector formed in accordance with one embodiment of the invention,

FIGURE 11B is a side view of the photodetector depicted in FIGURE 11A,

FIGURE 12 presents graphs depicting current-voltage characteristics of a plurality of exemplary silicon wafer microstructured by exposure to femtosecond laser pulses in the absence of annealing as well as in the presence of annealing at different annealing temperatures,

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FIGURE 13 presents graphs depicting responsivity of a plurality of silicon wafers microstructured by exposure to femtosecond laser pulses in the presence of SF_6 (with no annealing and with annealing at different temperatures) as a function of wavelength in comparison with that of a commercial photodiode illustrating that a significantly enhanced responsivity can be obtained by judicious annealing of wafers subjected to laser microstructuring,

FIGURE 14 present graphs depicting current-voltage characteristics of a plurality of exemplary prototype silicon wafers microstructured by femtosecond laser pulses at different laser fluences and each annealed at 825 K,

FIGURE 15A presents comparative responsivity measurements for prototype silicon wafers microstructured by femtosecond laser pulses at different fluences and each annealed at 825 K for about 30 minutes,

FIGURE 15B presents comparative responsivity measurements for prototype silicon wafers microstructured by femtosecond laser pulses at different fluences and each annealed at 1075 K for about 30 minutes,

FIGURE 16A presents current-voltage characteristics for n-doped and p-doped silicon substrates microstructured by exposure to femtosecond laser pulses at a fluence of 6 kJ/m^2 followed by annealing at 825 K for about 30 minutes,

FIGURE 16B presents current-voltage characteristics for n-doped and p-doped silicon substrates microstructured by exposure to femtosecond laser pluses at a fluence of 4 kJ/m^2 followed by annealing at 1075 K for about 30 minutes,

FIGURE 17A presents responsivity measurements for prototype exemplary n-doped and p-doped silicon substrates microstructured at two different laser fluences (4 kJ/m^2 and 6 kJ/m^2) and annealed at 825 K for about 30 minutes,

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FIGURE 17B presents responsivity measurements for prototype exemplary n-doped and p-doped silicon substrates microstructured by femtosecond laser pulses at a fluence of 4 kJ/m^2 and annealed at 1075 K for about 30 minutes,

FIGURE 18 presents a graph depicting responsivity as a function of back bias for an n-doped silicon substrate microstructured via irradiation by femtosecond laser pulses at a fluence of 4 kJ/m^2 and annealed at 825 K for about 30 minutes (the measurement was performed by employing a white light source with an approximate power of 50 microwatts),

FIGURE 19A presents graphs depicting current-voltage characteristics of an n-doped silicon sample microstructuured by femtosecond laser pulses at a fluence of 4 kJ/m^2 and annealed at 825 K as a function of operating temperature,

FIGURE 19B presents a graph depicting the responsivity of a microstructured silicon wafer to incident radiation having a wavelength of 1064 nm as a function of operating temperature,

FIGURE 20 illustrates current-voltage characteristics for a high resistivity (resistivity greater than 1 Ohm-m) microstructured silicon wafer that can be utilized as a solar cell, with and without one sun illumination,

FIGURE 21 illustrates current-voltage characteristics for a low resistivity (e.g., a resistivity in a range of about 0.01 to about 0.1 Ohm-m) microstructured silicon wafer that can be utilized as solar, with and without one sun illumination,

FIGURE 22 schematically depicts an exemplary experimental set-up for measuring field emission of a silicon substrate microstructured in accordance with the teachings of the invention, and

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FIGURE 23 shows a graph depicting field emission current generated by a silicon wafer microstructured by exposure to femtosecond laser pulses in the presence of SF_6 as a function of a potential difference applied thereto.

Detailed Description

With reference to a flow chart 10 of FIGURE 1, in one aspect, the present invention provides a method of fabricating a radiation-absorbing semiconductor structure in which, in an initial step 10a, each of a plurality of locations on a surface of a silicon substrate is irradiated with one or more laser pulses while exposing the surface to a substance having an electron-donating constituent so as to generate surface inclusions containing a concentration of the electron-donating constituent. The laser pulses can have a central wavelength in a range of about 200 nm to about 1200 nm, and a pulse width in a range of about tens of femtoseconds to about hundreds of nanometers. Preferably, the laser pulse widths are in a range of about 50 femtoseconds to about 50 picoseconds. More preferably, the laser pulse widths are in the range of about 50 to 500 femtoseconds. The number of laser pulses irradiating the silicon surface can be in a range of about 2 to about 2000, and more preferably, in a range of about 20 to about 500. Further, the repetition rate of the pulses can be selected to be in a range of about 1 kHz to about 50 MHz, or in a range of about 1 kHz to about 1 MHz. Moreover, the fluence of each laser pulse can be in a range of about 1 kJ/m^2 to about 12 kJ/m^2, and more preferably in a range of about 3 kJ/m^2 to about 8 kJ/m^2.

While in some embodiments, the electron donating constituent is a fluid (gas or liquid), in other embodiments it can be a solid deposited over the silicon surface exposed to laser pulses. By way of example, in some embodiments, the silicon surface can be exposed to a sulfur-containing gas (e.g., SF_6 or H_2S) while irradiated with the laser pulses. In some other embodiments, Cl_2 or N_2 is employed as the electron-donating substance with which the silicon surface is in contact during laser irradiation. In yet other embodiments, selenium or tellurium can be employed. Without any loss of generality, in the following discussion, it is assumed that SF_6 is employed as the substance containing an electron-donating constituent, and that the irradiating pulses have femtosecond pulse widths, unless otherwise indicated. However, it should be clear to those having ordinary skill in the art that various embodiments of the invention

described below can also be practiced with other fluids or solids and laser pulses having other pulse widths, such as those listed above.

In some embodiments, the silicon substrate is p-doped (e.g., doped with Boron) with a doping level in a range of about 10^{11} to about 10^{18}. In other embodiments, the silicon substrate is slightly n-doped (e.g., doped with Phosphorus) with a doping level in a range of about 10^{11} to about 10^{18}, and preferably in a range of about 10^{12} to about 10^{15}. The substrate thickness is not typically a critical parameter, and can be in a range of about 2 microns to about 1000 microns. The substrate can have an electrical resistivity in a range of about 0.001 ohm-m to about 10 ohm-m.

FIGURE 2 schematically depicts an exemplary apparatus 12 that can be utilized for irradiating a silicon sample with a plurality of femtosecond pulses. The apparatus 12 includes a sample processing chamber 14 that comprises a stainless steel cube 16 with Conflat flange connections on each of its six sides. A three-axis, precision motion controller 18 is attached to the back side of the cube. This controller contains two orthogonal micrometer precision axes driven by computer controlled motors. The third axis is hand-controlled with about 1 mil precision. The controller can translate a one-inch diameter stainless steel rod 20 that supports a 2-inch diameter mounting magnet 22 in the center of the cube to which a magnetizable sample holder can be mounted. A two-stage roughing pump 24 is coupled to the cube to evacuate the chamber to a base pressure of approximately 10^{-3} torr. Two pressure gauges 26 and 28 are employed to monitor the chamber's pressure. A leak valve 30 and a gas-handling manifold (not shown) allow introduction of gases of interest into the chamber. An optical grade, 4.5 inch quartz window 32 is attached to the front of the chamber for providing laser access. Further, a quick-access viewport door 34 allows rapid loading and removal of samples as well as safe viewing of the sample during microstructuring.

In this exemplary apparatus, a regeneratively amplified, femtosecond Ti:Sapphire laser system (not shown) provides approximately 100 fs laser pulses having a central wavelength of 800 nm at a repetition rate of 1 kHz. The laser pulses are focused by a anti-reflection coated, plano-convex lens 36 (e.g., having a focal length of about 250-nm) through the quartz window onto the sample surface. In this exemplary embodiment, the lens is mounted on a single axis linear translation stage and positioned such that its focal point is behind the sample. By moving the lens, and hence its focal

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point, the laser spot size can be varied at the sample surface (e.g., from a diameter of about 30 microns to 250 microns). In order to measure the laser spot size, a CCD (charge coupled device) camera 38 can be placed at the same distance as the sample surface from the lens. A flipper mounted mirror 40 can redirect the laser beam onto the camera to determine its spot size on the sample surface. A second CCD camera 42 can measure reflections of light generated by a white light fiber lamp 44 from the sample surface to monitor progress during microstructuring.

In one exemplary mode of operation, samples attached to a magnetizable sample holder can be loaded through the access door and attached to the mounting magnet. Samples can be then positioned in the center of the magnet to allow for maximum translation. The chamber can be evacuated to a base pressure of 10^{-3} torr and then filled to the desired pressure with an ambient gas (e.g., 0.67 bar of sulfur hexafluoride). The sample can then be irradiated with a 1-kHz train of 100-femtosecond 800-nm laser pulses. The fluence of each pulse can be set by selecting a spot size (e.g., 150 microns) and employing a waveplate/polarizing cube combination to vary the pulse energy. Either a single spot can be irradiated, or more typically the sample can be translated by utilizing the motion controller relative to the laser beam. For example, the sample can be translated in a raster scan pattern. An average number of pulses irradiating a given spot on the sample can be controlled by utilizing a shutter and varying the horizontal translation speed.

The irradiation of the silicon surface with the laser pulses in the presence of SF_6 at a selected partial pressure, for example, a partial pressure in a range of about 0.005 bar to about 1 bar, can cause formation of a sulfur-rich layer having a sulfur concentration in a range of about 0.1 atom percent to about 5 atom percent, and more preferably, in a range of about 0.5 atom percent to about 1 atom percent. This sulfur-rich layer exhibits an undulating surface morphology (topography) with micron-sized surface height variations. Such a textured surface obtained by irradiating a silicon surface with a plurality of temporally short laser pulses in the presence SF_6 (or other substances having an electron-donating constituent) is herein referred to as a micro-structured surface. By way of example, FIGURE 3 shows a scanning electron micrograph (SEM) of a such a micro-structured silicon surface (obtained in a direction forming a 45 degree angle relative to the surface) after irradiation of the silicon surface

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with an average of 5 shots of femtosecond laser pluses (100 femtoseconds) at a wavelength of 800 nm and having a fluence of 8 kJ/m2 in 0.67 bar of SF_6.

The sulfur-rich layer can be a substantially disordered layer that is several hundred nanometers thick and made up of nanocrystallites (e.g., about 10 – 50 nm in diameter) and nanopores. Selected area diffraction (SAD) measurements indicate that the surface layer retains a substantial crystalline order with a strong possibility that amorphous-like material is present between the nanocrystalline grains. Further, SAD measurements performed on silicon substrates exposed to either 10 or 500 pulses per location indicate that the substrate below the disordered layer comprises substantially undisturbed crystalline silicon (when a crystalline silicon substrate is utilized). Further, Rutherford backscattering spectroscopy (RBS) and energy dispersive X-ray (EDX) emission spectroscopy performed on such exemplary substrates show a large concentration of sulfur is present in the disordered layer (about 1 atom percent). Further, RBS spectra obtained from silicon samples exposed to different femtosecond (100 femtoseconds) laser shots per irradiation location show that the concentration of sulfur increases with increasing laser pulse numbers up to about 50 pulses. In particular, thc measured sulfur concentration increases from about 0.2 atom percent for a sample exposed to 2 pulses per location to about 0.7 atom percent for a sample exposed to 50 laser pulses per location with the sulfur concentration exhibiting a plateau for laser pulses higher than about 50. It should be, however, understood that the above experimental results are provided simply for further elucidation of salient features of the invention, and not as limiting the scope of the invention. For example, higher sulfur concentrations in the disordered layer than those described above can also be obtained, and higher laser shots per location can be utilized.

A number of factors can affect the morphology of the microstructured surface. For example, samples microstructured by irradiating a portion thereof with laser pulses, without moving them relative to the laser beam (i.e., single spot irradiation), exhibit a subtle difference in their morphology relative to samples microstructured by irradiating a plurality of their surface locations via translation relative to the laser beam. With the rest of the experimental parameters left the same, there are two visible differences between translated and stationary samples. The microstructures in the stationary samples have a micrometer-sized sphere at the tip while the translated samples are

sharper and lack the spheres. Further, the translated samples have a larger amount of nanoscale particles spread across the microstructured surface.

In addition, the wavelength of the irradiating laser pulses, their fluence, and pulsewidths can also affect the morphology of the microstructured surface. For example, in a number of prototype samples microstructured by femtosecond pulses, with increasing the fluence (at constant shot number) the morphology showed a transition from laser-induced periodic surface structures, to a coarsened surface, to sharp microstructures, such as those depicted in the above FIGURE 3. As the laser pulse fluence increases, there is typically an increase in both the microstructure height and distance between the microstructures. In general, the fluence is preferably selected to be above a threshold fluence that would cause melting (e.g., 1.5 kJ/m^2). At very high fluences (e.g., greater than 12 kJ/m^2), material removal can become extreme and gaussian-shaped holes, rather than conical structures, can be formed in the surface.

Although in many embodiments described herein, femtosecond laser pulses are employed, in other embodiments, the microstructuring of the surface can also be achieved by employing picosecond or nanosecond pulses. For example, a number of silicon samples were microstructured by utilizing a train of 248-nm, 30-ns laser pulses with a flat-top spatial profile and a fluence of 30 kJ/m^2 generated by a KrF+ excimer laser in the presence of 1 bar of SF_6 (an average of 1500 pulses per spot were employed). The nanosecond-laser-formed microstructures showed some similarities and some differences relative to the femtosecond-laser-formed microstructures. In both cases, the microstructures were roughly conical, but the structures formed with the femtosecond laser pulses were smaller and more densely packed. For example, the femtosecond structures were roughly 8 microns tall and separated by about 4 microns while the nanosecond-formed structures were roughly 40 microns tall and separated by about 20 microns. Further, the femtosecond-formed structures were covered with nanoparticles 10 – 50 nm in diameter while the surface of the nanosecond-formed structures were much smoother.

Sample silicon wafers exposed to picosecond pulses (e.g., 10 picosecond) in the presence of SF_6 also showed a microstructured surface. The average separation between the microstructures exhibited a decrease from about 100 femtosecond pulse widths to

about 5 picosecond pulse widths but then showed an increase for pulse widths longer than about 5 picoseconds.

The laser wavelength can also affect the final morphology of the microstructures. By way of example, a prototype silicon sample microstructured with a train of 400 nm pulses exhibited a higher density of microstructures (but smaller) than those generated by 800 nm pulses at a similar fluence.

Other factors that can affect the microstructures' morphology include laser polarization and laser propagation direction relative to the irradiated silicon surface. For example, the direction of microstructure growth is parallel to the direction of incident light, and appears to be independent of the substrate's crystallographic planes. The base of microstructure can have an elliptical shape with the long axis perpendicular to the polarization of the irradiating laser light. Without being limited to any theory, this elliptical shape can be understood as being due to a higher absorption of p-polarized light relative to s-polarized light. For circularly polarized light, there is no preferential ablation, and the base of the microstructures can be substantially circular.

The fluid or solid in contact with the silicon surface during its microstructuring can also affect the resultant surface morphology. For example, utilizing SF_6 or Cl_2 as the ambient gas can lead to sharp-tipped conical structures with a radius of curvature of about 500 nm. In contrast, structures made in air, N_2 or vacuum are much more rounded (the radius of curvature of their tips is approximately 2 – 3 microns) than those made in these halogen-containing gases. In a number of exemplary samples microstructured in the presence of different gases, those made in SF_6 exhibited the greatest density of microstructures followed by those made in Cl_2. The microstruture densities produced in the presence of N_2 were approximately equal to those made in air, but approximately a factor of two less than the densities obtained by employing SF_6.

In some embodiments, the laser microstructuring of a silicon wafer is performed in the presence of a mixture of two or more substances. For example, samples microstructured in the presence of a mixture of SF_6 and Cl_2 exhibited an increase in the microstructure density at higher partial pressure of SF_6.

The sulfur-rich mircrostructured layer has unique optical and electrical properties. For example, it can exhibit a sheet charge carrier density in a range of about 10^{12} cm^{-2} to about 10^{14} cm^{-2}. By way of example and only for illustrative purposes, the

results of some resistivity and Hall effect measurements performed on a number of exemplary microstructured samples, each formed in an n-doped silicon substrate in accordance with the teachings of the invention, such as those described above, are presented below. For resistivity and Hall effect measurements, the van der Pauw technique, well-known to those having ordinary skill in the art, was employed. Briefly, four ohmic electrical contacts were formed on the disordered microstructured layer. The electrical contacts were formed by initially dipping a microstructured sample in a 5% HF solution for 5 minutes to remove any native oxide layer. Subsequently, with a mask covering all but the very corners of a selected microstructured surface area (e.g., a 10 x 10 mm^2 surface area), chromium/gold (Cr/gold) was evaporated onto the surface to form metal contacts at the exposed corners. A dicing saw was then used to cut slivers (e.g., 0.25 mm slivers) from each side. Cutting the sample edges ensures that the contacts are only connected to the surface layer and not the substrate layer. Finally, a wire bonder is utilized to connect the contacts on the corners of the sample to four Cr/Au contact pads evaporated onto a glass slide. It should be understood that this experimental arrangement, shown schematically in FIGURE 4, is sensitive primarily to the electronic properties of the microstructured layer, and not that of the substrate.

With continued reference to FIGURE 4, the resistivity measurements can be performed by applying a small DC current (e.g., 10 microamperers) from corner 2 to corner 1 while measuring a voltage from corner 3 to corner 4. Hall effect measurements can be performed by placing the sample in a strong magnetic field (e.g., a field of several thousand gauss) with the magnetic field perpendicular to the silicon surface. In one experiment, a small AC current (about 1-2 microamperes) was then applied from contact 1 to contact 3 while measuring an induced voltage across contacts 2 and 4. Control measurements were also performed on an n-doped (resistivity = 8 – 12 ohm-m) unstructured silicon wafer. Table 1 below lists the results of these measurements for microstructured layers formed in an n-doped silicon wafer having a resistivity in a range of about 8 – 12 ohm-m at a number of different laser pulse fluences.

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Original doping	Average fluence (kJ/m^2)	Doping after structuring	Sheet resistance Rs (Ohm)	Sheet carrier density n_s (cm^{-2})	Hall mobility μ ($cm^2V^{-1}s^{-1}$)
n	unstructured	-	31931	$1.78x10^{11}$	1101
n	4.0	n	4865	$7.37x10^{12}$	174
n	6.0	n	4992	$7.15x10^{12}$	175
n	8.0	n	6253	$4.52x10^{12}$	221
n	10.0	n	4554	$8.83x10^{12}$	155

This data shows that microstructured layer exhibits a higher sheet carrier density than the original substrate, but a lower carrier mobility – presumably as a result of the disorder in the microstructured layer.

Referring again to the flow chart 10 of FIGURE 1, subsequent to irradiation of the silicon surface with a plurality of laser pulses (step 10a), the substrate can annealed (step 10b) at a sufficiently elevated temperature for a selected time duration so as to cause an increase in the charge carrier density in the microstructured layer, e.g., by a factor in a range of about 10 percent to about 200 percent. For example, the substrate can be annealed at a temperature in a range of about 500 K to about 1100 K, and more preferably, in a range of about 500 K to about 900 K, for a selected time duration, e.g., a time duration in a range of about a few minutes to about a few hours (e.g., one-half hour).

The annealing step can be performed by employing a variety of different techniques. For example, the substrate can be placed in a thermal oven to be exposed to an elevated temperature for a selected duration. Alternatively, the substrate can be exposed to laser radiation, e.g., radiation having a wavelength in a range of about 200 to about 1200 nm, to cause its heating to a desired temperature. Further, the annealing step can be performed, for example, in an inert atmosphere (e.g., an argon atmosphere) or in a vacuum (a low-pressure environment). Alternatively, the annealing step can be applied simultaneously with the irradiation step. That is, the irradiation of the silicon substrate with the laser pulses can be performed while the substrate is maintained at an elevated temperature.

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Without being limited to any theory, the annealing step is designed to cause a rearrangement of the atomic bonds within the metastable microstructured layer to enhance the density of charge carriers – electrons – within that layer. The term "charge carrier density" is known to those having ordinary skill in the art. To the extent that any further explanation may be required, it refers to density of those charged particles, e.g., electrons, that are primarily responsible for current conduction, e.g., electrons in the conduction band states or in shallow impurity states below the conduction band. Such charged carriers are also herein referred to as free electrons or holes.

In other words, the annealing temperature and duration are selected to cause structural changes in the microstructured layer that result in increasing the carrier density in that layer while substantially maintaining responsivity of the layer for generating an electrical current when exposed to radiation within a selected wavelength range at a given applied back bias voltage, as discussed in more detail below. The structural changes caused in the microstructured sulfur-rich layer by an annealing step according to the teachings of the invention can be appreciated by considering that in many embodiments in which a p-doped silicon substrate is exposed to a plurality of laser pulses to generate a microstructured surface layer thercin, holes, rather than electrons, constitute the dominant charge carriers even after incorporation of about 1 atom percent sulfur having two possible donor electrons per atom. However, after annealing, electrons can constitute the dominant charge carriers in the microstructured layer. Without being limited to any particular theory, such observations suggest that sulfur in the microstructured layer, before annealing, is incorporated in silicon such that its donor electrons do not substantially contribute to conduction (the donor electrons are likely locked up in a trap, or perhaps the coordination number of the implanted sulfur is larger than four). An annealing step according to the teachings of the invention causes atomic bond rearrangements in the microstructured layer so as to free up donor electrons for contributing to electrical conduction. In fact, in case of p-doped silicon substrates, the number of donor electrons released during annealing can be sufficiently large to eliminate the holes as the dominant charge carriers and turn the microstructured layer into an n-doped layer having a sheet carrier concentration on the order of about 10^{14} cm^{-2}.

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A microstructured silicon wafer formed in accordance with the teachings of the invention exhibits absorption of incident electromagnetic radiation, particularly radiation having wavelengths in a range of about 250 nm to about 2500 nm. By way of example, FIGURE 5 presents absorption data for a microstructured silicon wafer (an n-Si (111) wafer having a thickness of about 260 microns and a resistivity in a range of about 8 – 12 ohm-m), each of which was generated by exposing its surface to 100 femtosecond laser pulses (2 to 500 shots per location) having a central wavelength of 800 nm and a fluence of about 8 kJ/m^2. This exemplary absorption data was recorded in a manner known in the art, prior to annealing the wafer, by employing an spectrophotometer equipped with an integrating sphere. The absorption data for an unstructured silicon wafer is also provided for comparative purposes.

This exemplary data indicates that the microstructured wafers exhibit an enhanced absorption of incident electromagnetic radiation, relative to unstructured silicon, across the entire recorded wavelength range, and particularly for wavelengths above about 1050 nm, which corresponds to the band-gap energy of crystalline silicon (1.05 eV). In the unstructured silicon, light photons having wavelengths longer than a wavelength corresponding to the band-gap energy do not contain sufficient energy to promote an electron from the valence band to the conduction band, leading to a drastic drop in absorption.

In contrast, the silicon wafers microstructured in accordance with the teachings of the invention exhibit significant absorption not only for wavelengths below the band-gap but also for those above it. In fact, the exemplary data of FIGURE 5 shows that silicon wafers structured by exposure to 20 pulses per location or higher (e.g., 500 pulses in this exemplary data set) exhibit near-unity, featureless absorption of wavelengths from about 0.4 micron to about 1 micron, a small decrease in absorption for wavelengths around about 1.05 micron (a wavelength corresponding to the band edge of unstructured silicon), and strong featureless absorption from about 1.05 microns to about 2.5 microns. It should be understood that this data is presented only for illustrative purposes, and is not necessarily intended to present the optimal absorption of a silicon wafer structured in accordance with the teachings of the invention.

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As noted above, in many embodiments of the invention, a microstructured wafer is annealed at a temperature and for a duration designed to enhance the charge carrier concentration in its microstructured layer. Such annealing can be performed at a variety of different temperatures. By way of example, FIGURE 6 schematically illustrates electromagnetic radiation absorptance data for a plurality of microstructured silicon wafers generated by utilizing 500 laser pulses per surface location (100 fs pulses at a central wavelength of 800 nm and a fluence of 8 kJ/m2) in the presence of 0.67 bar of SF_6 relative to that of unstructured silicon. Each structured wafer was annealed at a selected temperature in a range of about 575 K to about 875 K for about 30 minutes. This exemplary data shows that annealing at temperatures below about 575 K has little effect on the observed absorptance. On the other hand, such annealing performed at a temperature between about 575 K and 875 K does not substantially affect absorptance above the bandgap, but lowers the below band-gap absoptance – the higher the annealing temperature, the greater is the reduction in absorptance. It should, however, be understood that this data is only exemplary, and different results may be obtained for microstructured wafers generated by employing different parameters (e.g., difference fluence or laser shot numbers).

A microstructured silicon wafer according to the teachings of the invention can be generated not only by utilizing femtosecond pulses, but also other pulse widths (e.g., nanosecond and picosecond pulse widths). By way of example and only for illustrative purposes, FIGURE 7 illustrates exemplary absorptance graphs as a function of incident radiation wavelength for femtosecond-laser-formed and nanosecond-laser-formed microstructured silicon surfaces, before and after annealing at about 875 K for about 30 minutes, as well as that of an unstructured silicon wafer. The femtosecond-formed mircrostructures were generated by employing 100 fs laser pulses (500 shots per location) having a central wavelength of about 800 nm and a fluence of about 8 kJ/m^2. The nanosecond-formed microstructures were generated by employing 30 ns laser pulses (about 1500 shots per location) having a central wavelength of 248 nm and a fluence of about 30 kJ/m^2. It should be understood that this data is presented only for illustrative purposes and is not intended to necessarily indicate absorptance exhibited by a microstructured silicon formed in accordance with the teachings of the invention under all circumstances.

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In some embodiments of the invention, microstructuring of a silicon wafer can be accomplished in the presence of a background fluid rather than SF_6. For example, H_2S, Cl_2, N_2 or air can be utilized. By way of example, FIGURE 8A and 8B compare absorptance of some exemplary prototype microstructured silicon wafers generated by employing femtosecond laser pulses (100 fs, 800 nm, 8 kJ/m^2 and 500 shots per location) in the presence of various fluids – without an annealing step – with that of unstructured silicon. The vacuum data corresponds to microstructuring the wafer in a chamber evacuated to a base pressure that is less than about 10^{-6} bar. While all microstructured samples exhibit an enhanced absorption relative to unstructured silicon, this exemplary data shows the microstructuring in SF_6 and H_2S brings about the most dramatic change in absorptance relative to unstructured silicon. In particular, samples structured with SF_6 exhibit near-unity, substantially featureless absorptance across the entire measured spectrum.

A variety of background fluid pressures can be employed in many embodiments of the invention for generating microstructured silicon wafers. By way of example, FIGURE 9 shows absorptance data for a number of exemplary prototype microstructured silicon wafers generated in SF_6 (100 fs pulses, 800 nm, 500 shots per location) at different ambient pressures, as well as a wafer microstructured in vacuum (e.g., a pressure of less than 10^{-6}). The greatest rate of increase is observed at low pressures. In this exemplary data set, at pressures above about 27 mbar, the below band-gap absorptance does not show much variation with wavelength, while at lower pressures, it decreases with increasing wavelength.

The microstructured silicon wafers generated in accordance with the teachings of the invention, particularly those subjected to an annealing step at an elevated temperature in a range of about 500 K to about 900 K, not only exhibit enhanced absorption of electromagnetic radiation over a wide range (e.g., from ultraviolet wavelengths to near infrared), but they also exhibit voltage-versus-current profiles that are characteristic of diodes. As discussed in more detail below, these properties allow the use of such microstructured silicon wafers in fabricating photodetectors that exhibit enhanced responsivity relative to conventional silicon photodetectors.

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More specifically, a microstructured silicon layer formed in accordance with the teachings of the invention, particularly one formed by exposure of a wafer surface to laser pulses followed by, or simultaneous with, an annealing step designed to release electrons in the layer structured by the pulses, forms a diode junction, e.g., a p-n junction, with the underlying silicon substrate. It should be understood that a diode junction as used herein can also refer a junction formed between two n-doped portions having different free electron densities. As shown schematically in FIGURE 10, a p-n junction can be formed by bringing a semiconductor material having acceptor impurity atoms (p-doped) into contact with a semiconductor material having donor impurity atoms (n-doped). The difference in charge carrier concentration between the p-doped and the n-doped portions generates a diffusion potential across the junction – electrons and holes begin to diffuse across the junction to portions having a respective lower concentration. As they cross to the other side of the junction, they recombine with their oppositely charged electrical counterparts in a region very close to the junction. This migration of charge carries across the junction causes formation of space charges (immobile ions) with opposite polarities on the two sides of junction. As the number of space charges increases (positively charged for the n-type side and negatively changed for the p-type side), a potential difference builds up across the junction, which results in an electric field in a direction opposite that of the diffusion potential.

Upon reaching thermal equilibrium, a thin insulating layer is present near the junction in which charge carriers have been depleted by recombination (depletion region). A strong electric field is present in the depletion region and a large electric potential exists across this region. The junction can be reverse-biased by applying an electric field across it that reinforces this internal electric field. Such a reverse-bias voltage expands the insulating depletion region and enhances both the internal electric field and the potential difference across the junction. The junction can also be forward-biased by applying an electric field that is opposite to the internal field across it. Such a forward-bias voltage shrinks the depletion region, thereby diminishing the internal electric field and the potential difference across the junction. When forward-biased, a current flows across the junction with electrons injected into the n-doped portion and leaving from the p-doped portion. In other words, the p-n junction can act as a rectifier

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by allowing current flow in only one direction. This behavior gives rise to a current-voltage (I-V) curve characteristic of a diode.

As discussed above, a silicon wafer in which a microstructured layer is formed according to the teachings of the invention can exhibit an I-V curve characteristic of that obtained by a diode junction. Without being limited to any theory, such a current-voltage behavior can be understood by considering that the wafer includes two adjacent, yet distinct, layers: a surface layer in which a concentration of an electron-donating constituent is incorporated and an underlying substantially undisturbed silicon substrate layer. These two layers exhibit different crystalline structures, chemical compositions, and charge carrier doping concentrations. In addition, the microstructured layer has unique optical properties including high absorptance of incident electromagnetic radiation from the near ultraviolet into the near-infrared wavelengths. In one aspect, the invention employs such microstructured silicon wafers for fabricating photodiodes, as discussed in more detail below.

By way of example, FIGURE 11A schematically illustrates a photodetector 46 according to one embodiment of the invention that includes a microstructured silicon wafer 48 having a microstructured surface layer 50 that is formed in a silicon substrate 51 by irradiating a plurality of locations on a substrate's surface with short laser pulses (e.g., pulse widths in a range of about tens of femtoseconds to tens of nanoseconds) while exposing the surface to a substance having an electron-donating consitutent (e.g., SF_6). The laser-irradiated wafer is then annealed under conditions (e.g., at an elevated temperature and for a selected duration) designed to enhance concentration of electrons in the microstructured surface layer (e.g., annealing at a temperature in a range of about 500 K to about 900 K for a duration of a few minutes to a few hours).

The exemplary photodetector 46, functioning as a photodiode, also includes a plurality of metallic electrical contacts 52, which have a finger grid geometry, that are disposed on the microstructured surface layer. In addition, an electrical contact 54, in the form of a metallic coating layer, is disposed on the back surface of the silicon substrate (i.e., the undisturbed silicon surface opposite the microstructured surface) that substantially covers the entire surface. In this exemplary embodiment, a chromium/gold alloy (Cr/Au) is employed for fabricating the electrical contact. However, those having

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ordinary skill in the art will appreciate that the contacts can be formed of other metals, as well.

The metallic contacts 52 and 54 allow applying a bias voltage, e.g., a reverse bias voltage, across the wafer by employing, for example, a voltage source 56. The reverse bias voltage can reinforce the internal electrical field in the depletion layer of a diode junction formed between the microstructured layer 50 and the underlying silicon substrate 51. As discussed in detail below, the photodetector 46 can operate with small bias voltages, e.g., voltages in a range of about 0.1 V to about 15 V, with a responsivity (i.e., photocurrent generated per unit of power of incident light (amperes/watts)) that is considerably better than that typically exhibited by a conventional silicon photodetector. These attributes allow incorporating silicon photodetectors formed according to the teachings of the invention, such as the exemplary photodetector 46, into integrated silicon photo-electronic circuits as high sensitivity detectors.

In operation, radiation (i.e., photons) incident on the microstructured surface layer of the photodiode's silicon wafer is absorbed (when the radiation wavelength is in the operating range of the photodetector), e.g., by valence electrons, in the microstructured layer. The absorption of the incident radiation causes generation of electron-hole pairs. The electric field within the depletion region causes separation of the generated electron-hole pairs, especially those created at or in proximity of the diode junction, which is formed between the microstructured silicon layer and the underlying silicon substrate. The separated electron-hole pairs provide a photocurrent that is proportional to the number of incident photons (those skilled in the art appreciate that such a photocurrent is added to a generation current and a recombination current that can be inherently present in a diode junction). Hence, incident radiation can be detected, and quantified, by measuring the induced photocurrent.

A photodetector formed according to the teachings of the invention not only exhibits absorptance across a wide range of wavelengths (the absoptance is generally commensurate with that exhibited by the photodetector's microstructured silicon wafer), but it also exhibits a diodic I-V behavior. By way of example and further elucidation of the salient features of a photodetector of the invention, FIGURE 12 illustrates a plurality of graphs, each representing current as a function of bias voltage for a plurality of microstructured silicon samples prepared under different conditions in an n-doped

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silicon substrate for use as the active component of photodetectors. All samples were irradiated with a plurality of femtosecond laser pulses (800 nm, 100 fs, fluence of 4 kJ/m^2) in the presence of SF_6, but were subjected to different annealing conditions. The graph A represents the current-voltage curve associated with a microstructured sample that was not annealed. This curve is substantially linear, indicating that the junction between the microstructured layer and the underlying silicon substrate in this sample is not diodic, but is merely resistive. In other words, such a wafer is not optimal for fabricating a photodetector.

In contrast, graphs B, C, and D illustrate current-versus-voltage behavior of those microstructured silicon samples that were subjected to annealing at different temperatures (the annealing duration was about 30 minutes in all cases). This exemplary data indicates that with an increase in the annealing temperature, the measured I-V curve approaches one expected from a diode. For example, at an annealing temperature of about 825 K, the I-V curve is diodic, characterized by an exponentially increasing current for a forward bias and a smaller, less rapidly increasing current for a reverse bias. The I-V curve corresponding to an annealing temperature of about 1075 K is also diodic. However, annealing a microstructured silicon wafer for a significant duration at a very elevated temperature can lead to a degradation of the below-band gap absorptance, and hence a degradation in the performance of a photodetector utilizing such a microstructured wafer in the near-infrared. In this exemplary data set, the substrate annealed at 825 K exhibit an optimal I-V characteristic. It should, however, be understood that such very elevated annealing temperatures may be employed so long as the annealing duration is sufficiently short. In general, the annealing of a microstructured silicon wafer to be employed in a photodetector of the invention should be carefully designed (i.e., annealing temperature and duration) to cause release of electrons in the microstructured surface layer without significantly degrading the wafer's absorptance of and responsivity to incident radiation.

A photodetector of the invention, such as the above exemplary photodetector 46, exhibits a responsivity that can be superior across a wavelength range of about 250 nm to about 10 microns to that of a conventional silicon photodiode. By way of example and only for illustration and corroboration purposes, FIGURE 13 presents experimental graphs representing responsivity of exemplary photodetectors formed in accordance with

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the teachings of the invention, over a selected wavelength range, in comparison with a conventional photodiode and those fabricated by employing microstructured silicon, but with no annealing or annealing at too high a temperature. In particular, graphs A and B show that photodetecotors of the invention that employ silicon wafers microstructured by femtosecond laser pulses in the presence of SF_6 (100 fs, 800 nm central wavelength and a fluence of 4 kJ/m^2) followed by annealing at 825 K or 725 K, exhibit a significantly enhanced responsivity relative to that of a conventional commercially available silicon photodiode. In particular, these photodetectors exhibit a responsivity that is more than an order of magnitude greater that that of the conventional photodiode in a wavelength range of about 250 nm to about 1050 nm. Although the responsivity shows a decrease for wavelengths longer than the band-gap edge (i.e., wavelengths longer than about 1050 nm), nonetheless, it remains significantly higher than that exhibited by a conventional silicon detector. In fact, conventional silicon detectors typically do not operate at useful levels of responsivity at wavelengths that are longer than the band-gap edge. For example, in this exemplary illustration, the responsivity of the commercial photodiode drops steeply to about 10^{-6} A/W for wavelengths longer than about 1050 nm

Further, the responsitivy data for wafers formed according to the teachings of the invention (e.g., graphs A and B) were obtained by applying small bias voltages (e.g., a bias voltage of about –0.5 volts in this exemplary embodiment). In contrast, conventional silicon photodetectors exhibit much lower responsivities, or require much higher bias voltages (e.g., 100 to 1000 volts) and/or have more complex structures. This indicates that while photodetectors formed in accordance with the teachings of the invention can be readily incorporated in integrated silicon circuitry, the incorporation of conventional silicon detectors, which require large bias voltages, into integrated silicon circuits can be impractical.

The data depicted in FIGURE 13 also shows that proper annealing of a silicon wafer irradiated by a plurality of short laser pulses, as described above, can considerably enhance the responsivity of a photodetector that employs that wafer. In particular, a photodetector fabricated by utilizing a wafer that, though exposed to laser pulses, was not annealed, exhibits a much degraded responsivity relative to those that were subjected to an annealing step at appropriate temperatures, e.g., at 725 K or 825 K. This

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exemplary data also shows that a photodetector that incorporates a microstructured wafer annealed, subsequent to irradiation by laser pulses, at a temperature of 1075 for thirty minutes exhibits a much degraded responsitivy relative to those annealed at 725 K or 825 K.

Hence, one aspect of the invention relates to annealing a silicon wafer, subsequent to – or simultaneous with – its irradiation by a plurality of short pulses in the presence of a substance having an electron-donating constituent, under conditions that would release electrons in the microstructured layer while preserving the responsivity of the wafer for detecting electromagnetic radiation. For example, in some embodiments of the invention, the annealing temperature is selected to be in range of about 500 K to about 1100 K, and more preferably in a range of about 700 K to about 900 K, and the annealing duration is selected to be in a range of about 1 minute to about several hours, and more preferably in a range of about 5 minutes to about 30 minutes. Alternatively, higher annealing temperatures can be employed so long as the annealing duration is properly selected to avoid degrading the responsivity of the resultant annealed wafer. For example, although the above data indicates that annealing the wafer at temperature of about 1075 K for about 30 minutes may not be desirable, this annealing temperature with a lower annealing duration can be suitable for practicing the invention in certain applications. To certain extent, annealing temperature and duration are inter-related. For example, shorter annealing time at a higher temperature can be employed in certain applications.

In other words, it is not simply annealing at an elevated temperature that is required. Rather, the annealing temperature and its duration need to be properly selected to ensure that a photodetector exhibiting enhanced responsivity over a wide wavelength range can be fabricated by utilizing the annealed wafer. It has been discovered that annealing a silicon wafer subsequent to, or simultaneous with, its exposure to short laser pulses in presence of a substance having an electron-donating constituent at a temperature that is too low can lead to noisy photodiode and annealing at too high a temperature and duration can lower the wafer's response to both visible and infrared wavelengths. More specifically, the annealing temperature and duration are preferably selected to enhance the concentration of carrier electrons in the microstructured layer – formed by laser irradiation in presence of a substance having an electron-donating

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constituent – by a factor in a range of about 10% to about 200% while ensuring that the resultant annealed wafer exhibits a responsivity greater than about 20 A/W at least at one wavelength, and preferably over the entire span, of a wavelength range of about 250 nm to about 1050 nm, and a responsivity greater than about 0.1 A/W at least at one wavelength, and preferably over the entire span, of a wavelength range of about 1050 nm to about 3500 nm. By way of example, in some embodiments of the invention, the annealing temperature is preferably selected to be in a range of about 700 to about 900 K.

The choice of the fluence of laser pulses irradiating a silicon wafer to generate a microstructured layer therein can also affect the performance characteristics of a photodetector that incorporates the microstructured wafer for detecting radiation. By way of example, FIGURE 14 presents exemplary data corresponding to current-voltage characteristics of a plurality of silicon wafers irradiated with a plurality of femtosecond laser pulses (100 fs, 800 nm central wavelength, 200 pulses per location) in the presence of SF_6 followed by annealing at 825 K for about 30 minutes. The laser pulse fluences, however, differed from one wafer to another. More particularly, the following laser fluences were employed: 4 kJ/m^2, 6 kJ/m^2, 8 kJ/m^2, and 10 kJ/m^2. This exemplary data indicates that increasing the fluence decreases the dark current for a given reverse bias voltage.

FIGURE 15A illustrates the responsivity of a plurality of photodetectors incorporating the above silicon wafers that were microstructured with different laser pulse flunces (the wafers were annealed at 825 K for 30 minutes). This exemplary responsivity data indicates that, in this sample set, the photodetector's responsivity decreases, and the wavelength of peak response shifts to longer wavelengths, with increasing fluence (the sample made with a fluence of 4 kJ/m^2 exhibits the highest response). By way of further illustration, FIGURE 15B presents responsivity data for photodetectors made with microstructured silicon wafers that were generated through irradiation with femtosecond pulses (100 fs, 800 nm central wavelength, 200 pulses per location) in the presence of SF_6 followed by annealing at 1075 K for about 30 minutes. The laser pulse fluences, however, varied from one sample to the next (4 kJ/m^2, 6 kJ/m^2, 8 kJ/m^2, and 10 kJ/m^2). A comparison of this data with the data presented in FIGURE 15A shows that the responsivity exhibited by the samples subjected to the higher

annealing temperature of 1075 is much lower that that of the samples annealed at 825 K. However, the samples annealed at the higher temperature exhibit much less variation in responsivity as a function of fluence. Further, the samples annealed at 1075 K – though exhibiting a lower responsivity – are less noisy and have a higher quantum efficiency.

It should be understood that the above data is presented only for illustration purposes, and is not intended to necessarily indicate an optimal fluence under all conditions. For example, the above exemplary samples were made with an average laser shot number of about 200 pulses, and may exhibit improved characteristics with a greater shot number. In general, in various embodiments of the invention, the laser pulse fluence is selected to be greater than about 3 kJ/m^2. More preferably, the fluence is chosen to be in a range of about 3 kJ/m^2 to about 10 kJ/m^2, or a range of about 3 kJ/m^2 to about 8 kJ/m^2.

In many embodiments of the invention an n-doped silicon substrate is employed for forming a microstructured wafer, as described above. Alternatively, a p-doped silicon wafer can be utilized. By way of example, FIGURE 16A presents graphs comparing the diodic characteristics of a microstructured wafer generated according to the teachings of the invention, such as those described above, employing a p-doped silicon substrate (p-Si(100), 350 micron thick, resistivity (ρ) greater than 1 ohm-cm) with one fabricated utilizing an n-doped silicon substrate. In both cases, a laser pulse fluence of about 6 kJ/m^2, an annealing temperature of about 825 K, and an annealing duration of about 30 minutes were utilized. Similar data is presented in FIGURE 16B for p-dopend and n-doped samples annealed at 1075 K for about 30 minutes.

This exemplary data shows that the p-doped samples annealed at 825 K exhibit a higher forward bias current than equivalently generated n-doped samples. The dark current for back biases also increases more rapidly for p-doped samples. Upon annealing at 1075 K, the p-doped samples exhibit very good diodic properties with the back bias decreasing to substantially the same level as that in equivalently generated n-doped samples. Further, the forward bias current increases more rapidly, resulting in good rectification ratios. As noted above, annealing at higher temperatures can increase donor concentration from sulfur doping. Such increase in the donor concentration can lead p-doped samples annealed at higher temperature to exhibit better rectification.

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A silicon substrate's doping can also affect the responsivity of a silicon wafer formed by microstructuring that substrate in accordance with the teachings of the invention. By way of example, FIGURE 17A shows measured responsivity data for two n-doped microstructured wafers and two p-doped microstructured wafers, both of which were annealed at 825 K for about 30 minutes. This exemplary data indicates that the responsivity of n-doped substrates is higher over the measured spectral range. However, FIGURE 17B shows that the responsivities of microsturctured wafers formed in p-doped and n-doped substrates, via laser irradiation and annealing at a higher temperature of about 1075 K, are nearly identical.

In general, the above illustrative data indicates that microstructured p-doped samples have a lower response but exhibit a better quantum efficiency. It should be understood that the above data is presented only for illustrative purposes and is not intended to limit the scope of the invention. In general, both p-doped and n-doped substrates can be employed in the practice of the invention, and the resultant diodic characteristics and responsivity of microstuctured wafers generated by utilizing such substrates can be different than those depicted above based on selection of other parameters, such as laser fluence, number of pulses, etc.

In addition to responsivity, another parameter of interest associated with performance of a photodetector can be its quantum efficiency. The term 'quantum efficiency' is known in the art, and is generally defined as the number of electron-hole pairs generated per incident photon at a zero applied voltage. In some cases, a microstructured sample that exhibits a high level of responsivity may not show a correspondingly high level of quantum efficiency. For example, in the above exemplary prototype microstructured silicon wafers, samples fabricated by employing n-doped substrates, laser pulses having a fluence of 4 kJ/m^2, and an annealing temperature of about 825 K exhibit the highest responsivity, but not the highest quantum efficiency. In fact, samples fabricated by employing similar conditions but a higher annealing temperature of 1075 K show higher quantum efficiencies, though lower responsivities. Similarly, the measured responsivities of samples made on p-doped substrates and annealed at 825 K or 1075 K are lower, but their quantum efficiencies are higher. Such variations of responsivity and quantum efficiency are preferably considered when

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selecting various parameters in practicing the teachings of the invention for fabricating a silicon photodetector.

The responsivity of a photodetector fabricated in accordance with the teachings of the invention can also vary as a function of a back bias applied thereto. Typically, the responsivity increases as the applied back bias increases. By of example, FIGURE 18 exhibits the responsivity of a silicon wafer microstructured in accordance with the teachings of the invention through irradiation by a plurality of femtosecond pulses at a fluence of $4kJ/m^2$ followed by annealing at 825 K for about 30 minutes, as a function of an applied back bias voltage. The sample was illuminated with a white light source with an approximate power of 50 microwatts. The responsivity, and hence gain, increases quickly up to a bias voltage of –5 volts and more slowly up to –15 volts. At voltages beyond –15 volts, the responsivity begins to fall. In some cases, the responsivity of a photodetector that exhibits a large gain may not be sufficiently linear for certain applications. Hence, in selecting a proper back voltage, in addition to responsivity, other factors, such as the linearity of the response should be considered. In addition, in applications in which the photodetectors are incorporated in an integrated silicon circuit, the bias voltage should be compatible with the requirements of that circuit.

A photodetector formed according to the teachings of the invention can operate within a wide range of temperatures. In some cases, it may be advantageous to cool the photodetector to decrease its average noise level. By way of example, FIGURE 19A presents current-voltage curves corresponding to an n-doped microstructured silicon sample made with femtosecond pulses at a fluence of about 4 kJ/m^2 and annealed at 825 K at different operating temperatures. The measured current in both the back bias and forward bias conditions decreases with decreasing the temperature. At very low temperatures (below 100 K), conduction becomes very low for both forward and back biases. FIGURE 19B shows the responsivity of such a microstructured wafer to incident radiation having a wavelength of 1064 nm (a wavelength close to the band gap of silicon at room temperature) at a back bias of –0.5 V as a function of operating temperature. The measured responsivity drops with temperature. This behavior may be, however, different if the wavelength of the illuminating light is far from the silicon band gap. A graph of the dark current at a bias voltage of –0.5 V as a function of temperature, however, shows that the noise decreases much more rapidly that the responsivity.

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In sum, photodiodes formed according to the teachings of the invention can exhibit responsivities in a wide region of the electromagnetic spectrum (e.g., wavelengths in a range of about 250 nm to about 1100 nm) that are nearly two orders of magnitude higher than those exhibited by conventional commercial silicon photodiodes. Further, responsivities at longer wavelengths, e.g., as long as 1600 nm, can be nearly five orders of magnitude greater than those exhibited by conventional silicon photodiodes in this range. In some of the above prototype samples fabricated according to the teachings of the invention for illustration purposes, the carrier mobility in the surface layer was measured to be about 101 $cm^2V^{-1}s^{-1}$; the response times included a rise time of about 10 ns and a fall time of about 30 ns; and a diode capacitance of about 63.9 nF at a back bias of –0.5 V was measured. A photodiode of the invention can exhibit a large gain at very small applied bias voltages, e.g., a gain greater than 1000 for an applied bias voltage of – 0.5 V.

A silicon photodetector according to the teachings of the invention, such as the above exemplary photodetector 46 (FIGURE 11A), can be fabricated by employing a variety of techniques. By way of example, in one exemplary method of fabricating such a photodetector, a selected portion of a silicon wafer, e.g., a 5 x 5 mm^2 area, is microstructured via exposure to short laser pulses in the presence of a suitable material, e.g., SF_6, in a manner described above. The wafer is then dipped in a solution of HF (e.g., a 5% solution) in order to remove any native oxide layer before forming electric contacts with the microstructured layer. Subsequently, a mask is deposited over the surface of the microstructued layer having exposed portions which correspond to a desired pattern of a conductive electrode to be formed on that surface. A selected metal, e.g., a Cr/Au alloy, is then evaporated over the masked surface, and the mask is removed to leave behind a patterned conductive layer, such as the conductive layer 52 shown in FIGURE 11A, and uncoated portions suitable for receiving radiation. Further, a conductive layer can be formed on a back surface of the wafer, an unstructured surface opposed to the microstructured layer, such as the layer 54 shown in FIGURE 11A. In many embodiments, the entire back surface is coated with the metal. The wafer can be then be coupled to a voltage source, such as the source 56 shown in FIGURE 11A, that can apply a bias voltage thereto and optionally other electronic elements, e.g.,

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capacitors, in a manner known in the art. Further, a the wafer and its associated circuitry can be placed in an appropriate housing by employing techniques known in the art.

The applications of microstructured silicon wafers formed according to the teachings of the invention, such as those discussed above, are not limited to photodetectors. For example, such silicon wafers can be employed in fabricating solar cells. In some cases, the optimal values of various parameters, such as substrate doping, associated with the microstructured wafer utilized in generating solar cells can be different than those in fabricating silicon photodetectors. A solar cell can be considered a p-n junction photodiode with high quantum efficiency. The conversion of photons into photocarriers is the physical mechanism by which light is converted in a solar cell into electricity. However, there is a fundamental difference between a photodetector and a solar cell. A photodetector is generally operated in a "photoconductive" mode: a back bias is applied thereto and a current is measured. In contrast, a solar cell is operated in a "photovoltaic" mode: it is operated in an open circuit mode or attached to a load without application of a bias voltage.

In one embodiment, a microstructured layer is formed in a p-doped crystalline silicon substrate by initially irradiating a plurality of locations on a surface thereof with femtosecond (e.g., 100 fs, and a central wavelength of 800 nm) laser pulses having a fluence of about 4 kJ/m^2 followed by annealing at 1075 K for about one hour. The wafer can then be utilized in fabricating a solar cell. More specifically, metal contacts, e.g., Cr/Au contacts, can be evaporated on the microstructure layer's surface so as to coat selected portions thereof while leaving at least a portion of the surface uncovered for receiving radiation, e.g., a finger grid metallic pattern can be disposed on the surface. In addition, the back surface of the substrate, the unstructured surface opposing the structured surface, can be coated, e.g., via evaporation, with a metallic coating. A load can be attached the wafer via electrical coupling to the metallic layers on the both sides of the wafer.

FIGURE 20 presents data comparing current-voltage (*I-V*) behavior of such a wafer, formed in a high resistivity (resistivity greater than about 1 ohm-m) silicon substrate, that can be utilized as a solar cell in the presence and in the absence of illumination. And FIGURE 21 presents a similar comparative data for a wafer formed in low resistivity silicon substrate (resistivity in a range of about 0.01 – 0.1 ohm-m). The

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solar cell fabricated by employing the high resistivity substrate has an open circuit voltage of 0.4 volts and a short circuit current of 13.4 mA while the solar cell fabricated by utilizing the low resistivity substrate has an open circuit voltage of 0.31 volts and a short circuit current of 13.45 mA. It should be understood that this data is presented only for illustration purposes, and to show the possibility of utilizing a wafer microstructured in accordance with the teachings of the invention in forming a solar cell. However, this data is not intended to indicate optimal performance of a solar cell generated in accordance with the teachings of the invention. For example, the deposition of electrical contacts on the substrate can be optimized to obtain better performance than that described above.

In another application, a silicon wafer microstructured in accordance with the teachings of the invention can be utilized as a field emitter. In other words, an electric field can be applied to the microstructured surface to cause emission of electrons therefrom. To show the possibility of utilizing a microstructured wafer for generating field emission current, a number of prototype exemplary microstructured wafers were fabricated and field emission currents generated by them were measured. The experimental step-up for performing these measurements is shown schematically in FIGURE 22. A microstructured silicon sample 58 with a gold coating 60 evaporated on a back surface is mounted to a silicon wafer 62 having a gold coating 64, which functions as an anode, and is separated therefrom by a pair of mica spacers 66 and 68. The mounted sample is placed in a vacuum chamber, which is evacuated to a pressure of about 10^{-6} torr. A potential difference can be applied between the microstructured sample 58 and the gold-coated anode. And emission current can be measured at each applied voltage, e.g., via a picoammeter 70, a resistive elements 72 placed in series with the ammeter to protect it from unexpected surges in current.

FIGURE 23 shows exemplary results of field emission currents measured for silicon samples microstructured in SF_6. The typical figures of merit for a field emitting surface are turn-on-field, defined as the electric field (bias voltage divided by the tip-to-anode spacing) for which a current density of 0.01 microampere/mm^2 is observed, and threshold field, defined as the field at which a current density of 0.1 microamperes/mm^2 is produced. The turn-on field for a plurality of exemplary prototype substrates microstructured in SF_6 was measured as 1.3 V/micrometer, and the threshold field was

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measured as 2.15 V/micrometer – excellent values that are on par with those exhibited by nanotubes.

Those having ordinary skill in the art will appreciate that various modifications can be made to the above embodiments without departing from the scope of the invention. It should also be understood that various exemplary data presented above are intended only for illustrating salient features of various aspects of the invention, and is not intended to limit the scope of the invention.

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What is claimed is:

1. A method of fabricating a radiation-absorbing semiconductor structure, comprising:

irradiating each of a plurality of locations on a surface of a silicon substrate with one or more femtosecond laser pulses while exposing said surface to a sulfur-containing substance so as to generate a plurality of sulfur inclusions in a surface layer of said substrate, and

annealing said substrate at a temperature in a range of about 500 K to about 1100 K for a time duration in a range of about a few seconds to about a few hours.

2. The method of claim 1, further comprising selecting a duration of each laser pulse to be in a range of about 50 femtoseconds to about 500 femtoseconds.

3. The method of claim 1, further comprising selecting a fluence of each pulse to be in a range of about 1 kJ/m^2 to about 15 kJ/m^2.

4. The method of claim 1, further comprising selecting a central wavelength of said laser pulses to be in a range of about 200 nm to about 800 nm.

5. The method of claim 1, wherein said irradiating step comprises exposing each location to a number of laser pulses ranging from 2 to about 500.

6. The method of claim 1, further comprising subjecting each of said surface locations to successive laser pulses separated from one another by a time interval in a range of about 1 microsecond to about 1 millisecond.

7. The method of claim 1, further comprising performing said annealing step in any of an inert atmosphere or a low-pressure atmosphere.

8. The method of claim 1, further comprising selecting said sulfur-containing substance to be any of SF_6 and H_2S.

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9. The method of claim 1, wherein said semiconductor structure absorbs radiation having wavelength components in a range of about 0.25 to about 10 microns.

10. The method of claim 1, wherein said semiconductor structure absorbs radiation having wavelength components in a range of about 0.35 to about 2.5 microns.

11. The method of claim 1, wherein said semiconductor structure exhibits a substantially uniform absorption for wavelength components in a range of about 1.2 to about 2.5 microns.

12. A method of fabricating a photodetector, comprising:

forming a semiconductor structure absorbing radiation in a wavelength range of about 0.25 to about 3.5 microns and exhibiting a diodic current-voltage characteristic in said wavelength range, said forming step comprising:

irradiating a surface of a silicon substrate at one or more locations thereof with one or more laser pulses having short pulse widths while exposing said surface to a sulfur-containing gas to generate a micro-structured layer having sulfur inclusions,

annealing said substrate at a temperature in a range of about 500 K to about 1000 K for a time duration in a range of about a few seconds to about a few hours, and

depositing a plurality of metallic contacts on selected portions of said semiconductor structure to allow applying a reverse bias voltage thereto.

13. The method of claim 12, wherein said pulse widths are selected to be in a range of about tens of femtoseconds to about tens of nanoseconds.

14. The method of claim 12, further comprising selecting said sulfur-containing substance to be any of SF_6 and H_2S.

15. The method of claim 12, further comprising performing said annealing step in an inert atmosphere.

16. The method of claim 12, wherein said depositing step comprises thermally evaporating one or more selected metals on said selected portions of the semiconductor structure.

17. The method of claim 12, further comprising selecting a thickness of said metal contacts to be in a range of about 5 nm to about 100 nm.

18. The method of claim 16, wherein said depositing step comprises thermally evaporating a chromium layer followed by thermally evaporating a gold layer on a selected portion of said semiconductor structure to generate at least one of said metal contacts.

19. The method of claim 18, further comprising selecting a thickness of said chromium layer to be in a range of about 1 nm to about 5 nm.

20. The method of claim 19, further comprising selecting a thickness of said gold layer to be in a range of about 4 nm to about 100 nm.

21. The method of claim 12, further comprising configuring said metal contacts so as to ensure that at least a portion of said micro-structured layer remains capable of receiving an external radiation.

22. A method of fabricating a semiconductor structure, comprising

irradiating a plurality of locations on a surface of a silicon substrate with one or more laser pulses having pulse widths in a range of about 50 to about 500 femtoseconds while exposing said surface to a substance having an electron-donating constituent so as to generate a micro-structured surface layer comprising inclusions incorporating said electron-donating constituent, and

annealing said substrate at an elevated temperature in a range of about 500 K to about 1100 K for a selected time period.

23. The method of claim 22, further comprising selecting said electron-donating constituent to be any of chlorine (Cl_2), nitrogen (N_2) and air.

24. The method of claim 22, wherein said irradiating step further comprises directing said laser pulses at said surface along a direction substantially perpendicular to said surface.

25. The method of claim 22, wherein said selected annealing period is in a range of about a few seconds to about a few hours.

26. The method of claim 22, wherein said annealing step is performed in an inert atmosphere.

27. A method of fabricating a radiation-absorbing semiconductor wafer, comprising:

irradiating at least one surface location of a silicon substrate with a plurality of temporally short laser pulses while exposing said location to a substance having an electron-donating constituent so as to generate a substantially disordered surface layer incorporating a concentration of said electron-donating constituent, and

annealing said substrate at an elevated temperature and for a duration selected to enhance charge carrier density in said substantially disordered surface layer.

28. The method of claim 27, wherein said elevated temperature and duration are selected to cause re-arrangement of atomic bonds in said surface layer so as to increase concentration of carrier electrons in surface layer.

29. The method of claim 27, wherein said elevated temperature and duration are selected to enhance electron carrier density in the surface layer by a factor of about 10% to about 200% relative to a pre-annealing level.

30. The method of claim 27, wherein said elevated temperature and duration are selected to cause said surface layer to form a diode junction with underlying silicon substrate.

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31. The method of claim 27, wherein said elevated temperature and duration are selected such that said annealed substrate exhibits a responsivity in a range of about 1 A/W to about 200 A/W upon exposure of said surface layer to radiation having wavelengths in a range of about 250 nm to about 1100 nm and application of a reverse bias in a range of about 0.1 V to about 15 V to said wafer.

32. The method of claim 27, wherein said elevated temperature is selected to be in a range of about 500 K to about 1100 K.

33. The method of claim 33, wherein said duration is selected to be in a range of about a few seconds to about few hours.

34. The method of claim 27, further comprising selecting said short laser pulses to have pulse widths in a range of about tens of femtoseconds to about tens of nanoseconds.

35. The method of claim 27, further comprising selecting a fluence of said pulses and a partial pressure of said substance having an electron-donating constituent such that the concentration of said electron-donating constituent incorporated in said surface layer ranges from about 0.5 to about 5 atom percent.

36. A method of fabricating a radiation-absorbing semiconductor wafer, comprising

irradiating at least one surface location of a silicon substrate with temporally short laser pulses while exposing the substrate to a substance having an electron-donating constituent so as to generate a microstructured surface layer having inclusions containing the electron-donating constituent, and

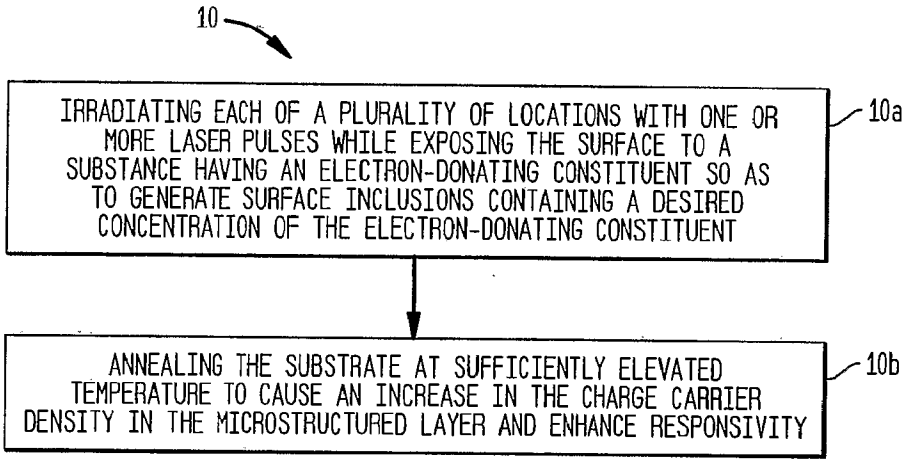
annealing the substrate at an elevated temperature and for a duration selected to enhance a responsivity of the microstructured substrate to radiation having at least one wavelength in a range of about 250 nm to about 1100 nm incident on the microstructured surface layer by at least a factor of about 10.

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37. The method of claim 37, wherein the annealing temperature lies in a range of about 700 K to about 900 K.

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FIG. 1



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FIG. 2

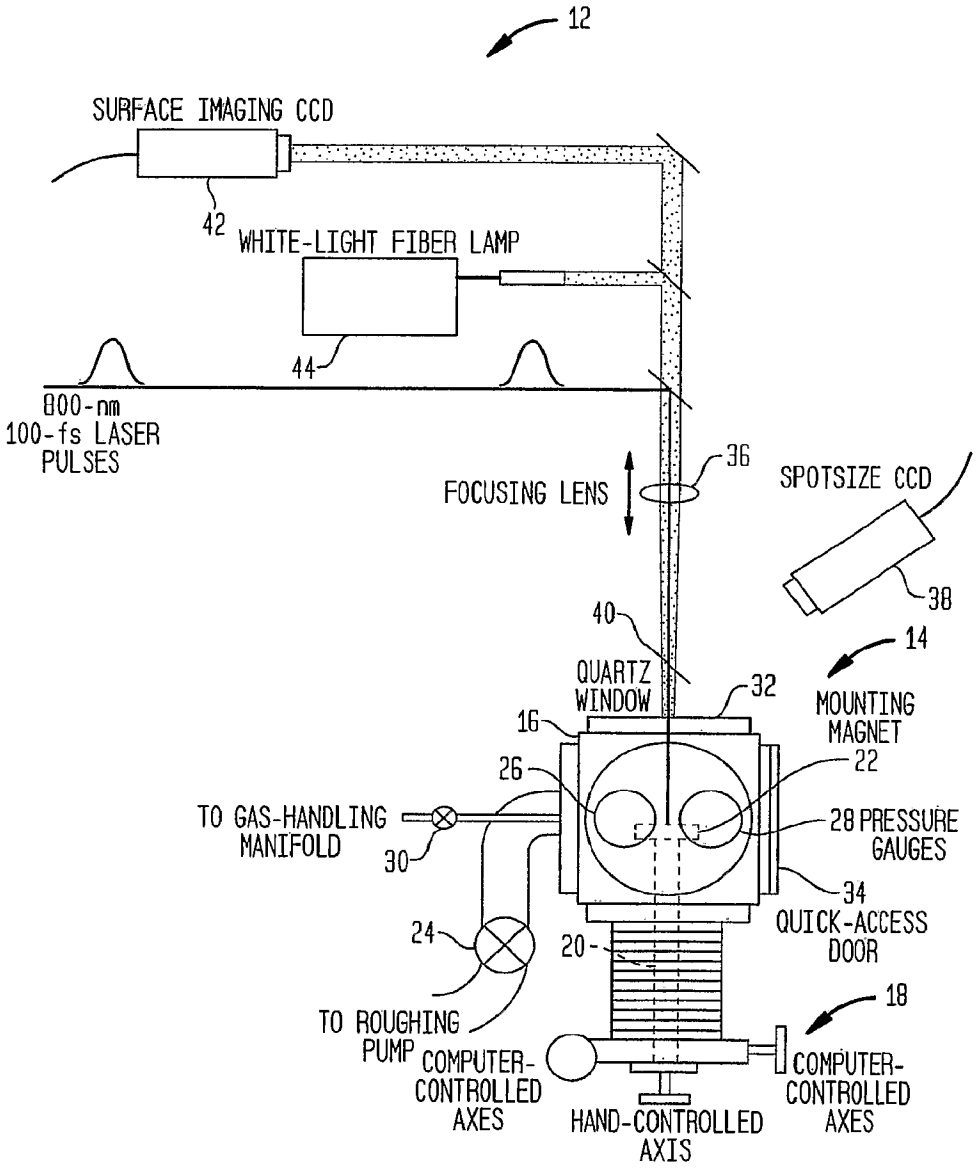
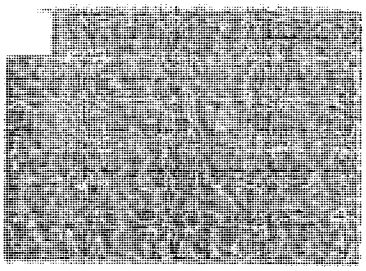

12
SURFACE IMAGING CCD
42
WHITE-LIGHT FIBER LAMP
44
800-nm
100-fs LASER
PULSES
FOCUSING LENS
36
SPOTSIZE CCD
38
40
14
QUARTZ
WINDOW
32
MOUNTING
MAGNET
16
26
22
TO GAS-HANDLING
MANIFOLD
30
28 PRESSURE
GAUGES
34
QUICK-ACCESS
DOOR
24
20
18
TO ROUGHING
PUMP
COMPUTER-
CONTROLLED
AXES
HAND-CONTROLLED
AXIS
COMPUTER-
CONTROLLED
AXES

FIG. 3



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FIG. 4

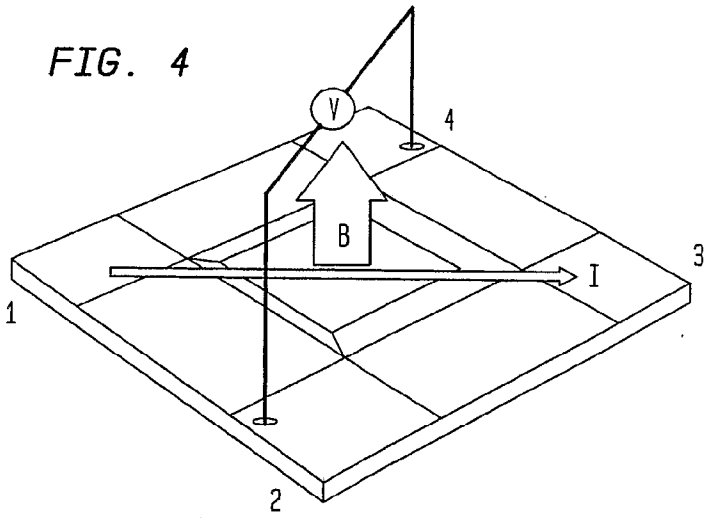

V
4
B
I
3
1
2

FIG. 5

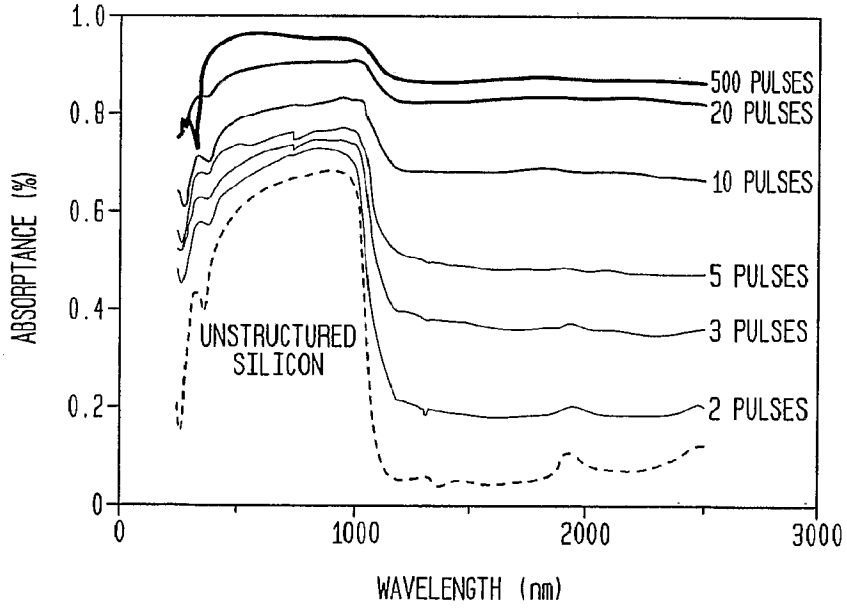

1.0
0.8
0.6
0.4
0.2
0
ABSORPTANCE (%)
500 PULSES
20 PULSES
10 PULSES
5 PULSES
3 PULSES
2 PULSES
UNSTRUCTURED
SILICON
0
1000
2000
3000
WAVELENGTH (nm)

FIG. 6

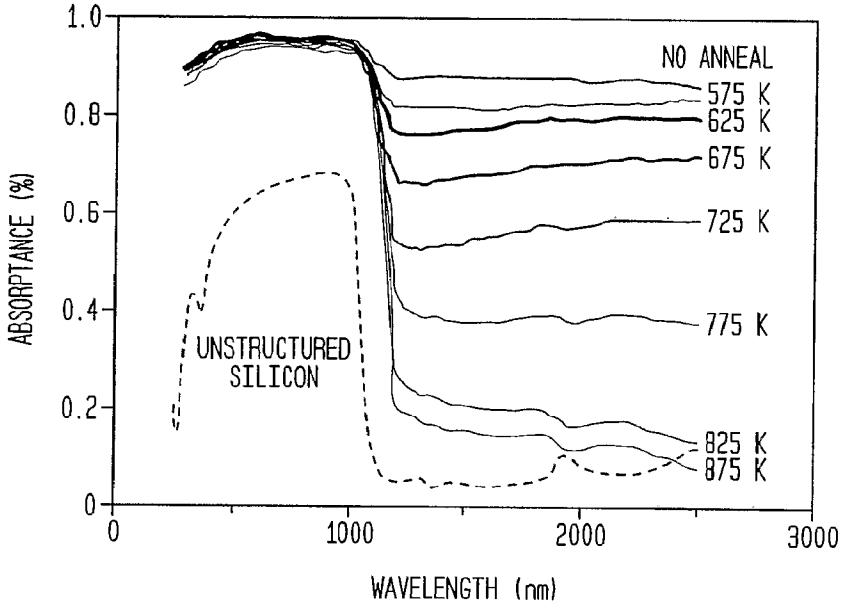
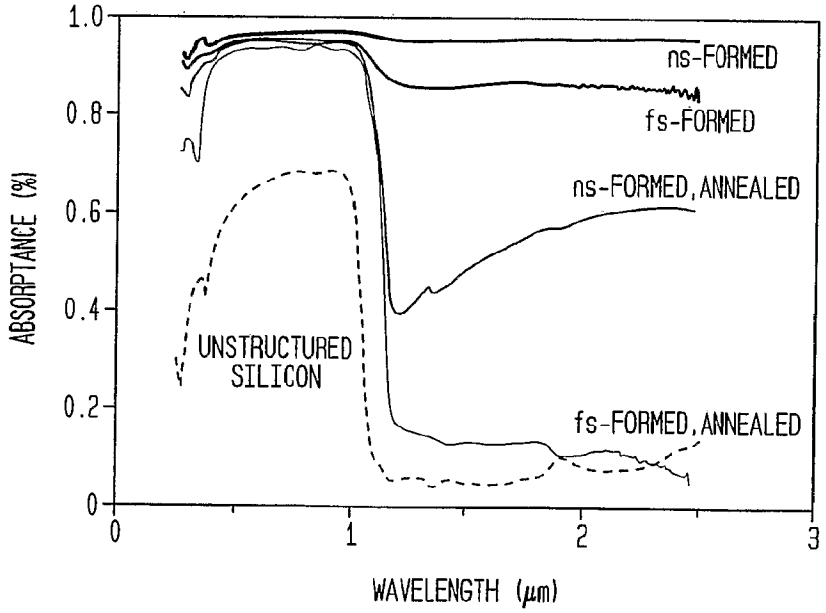


FIG. 7



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FIG. 8A

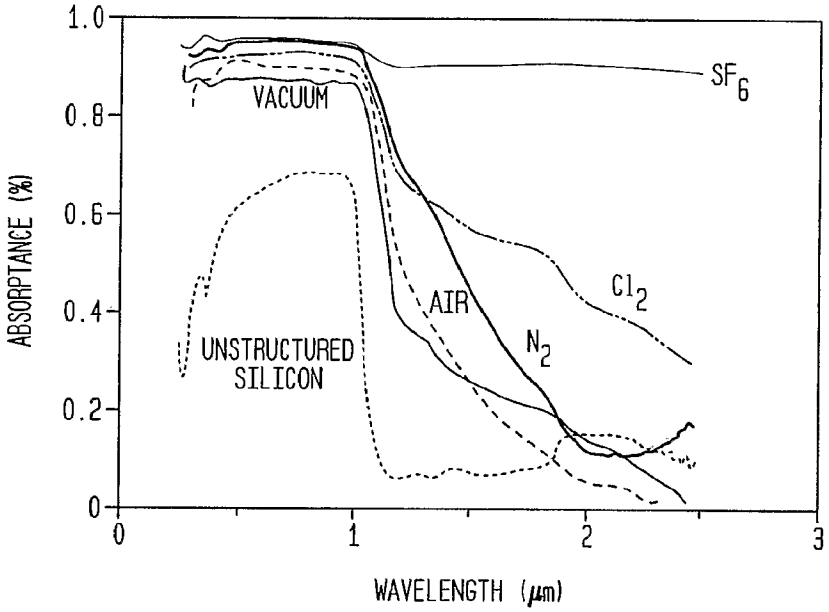

1.0
0.8
0.6
0.4
0.2
0
ABSORPTANCE (%)
VACUUM
SF6
AIR
Cl2
N2
UNSTRUCTURED SILICON
0
1
2
3
WAVELENGTH (μm)

FIG. 8B

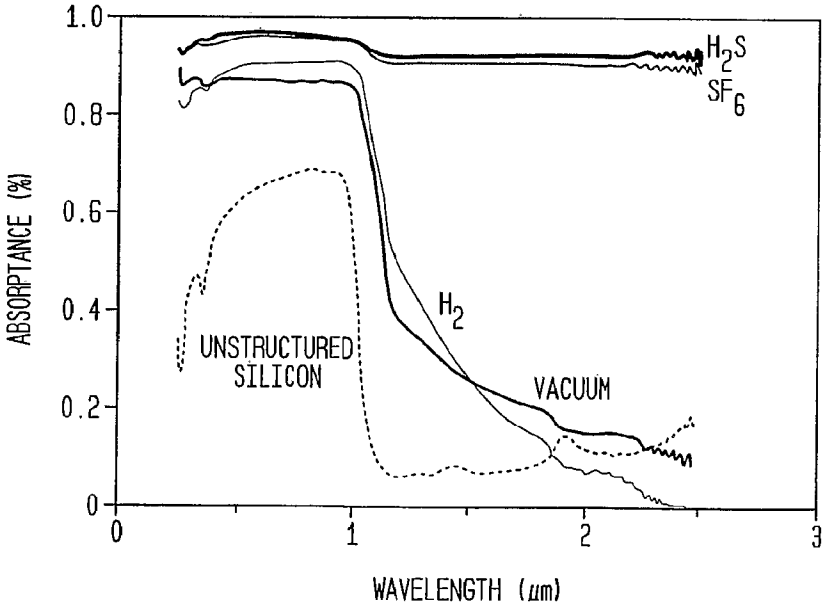

1.0
0.8
0.6
0.4
0.2
0
ABSORPTANCE (%)
H2S
SF6
H2
UNSTRUCTURED SILICON
VACUUM
0
1
2
3
WAVELENGTH (μm)

FIG. 9

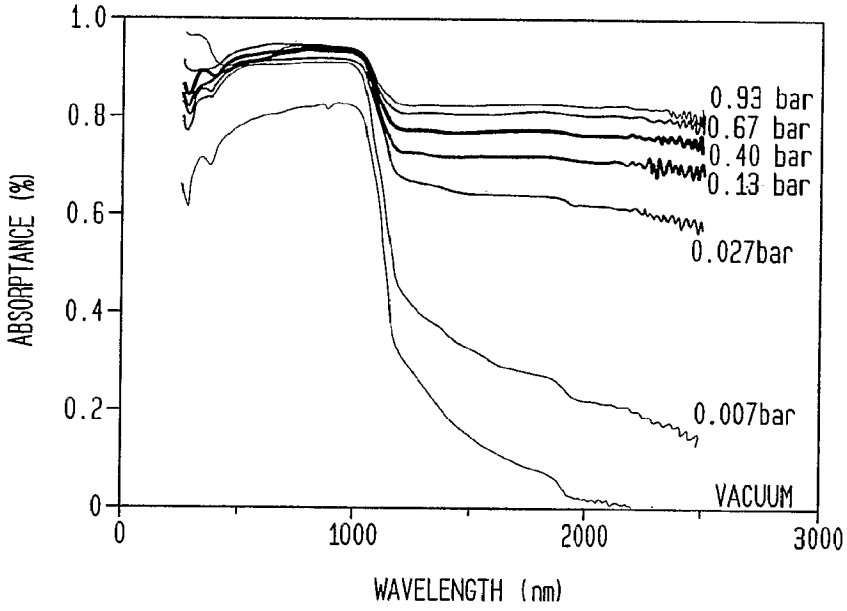

1.0
0.8
0.6
0.4
0.2
0
ABSORPTANCE (%)
0
1000
2000
3000
WAVELENGTH (nm)
0.93 bar
0.67 bar
0.40 bar
0.13 bar
0.027bar
0.007bar
VACUUM

FIG. 10

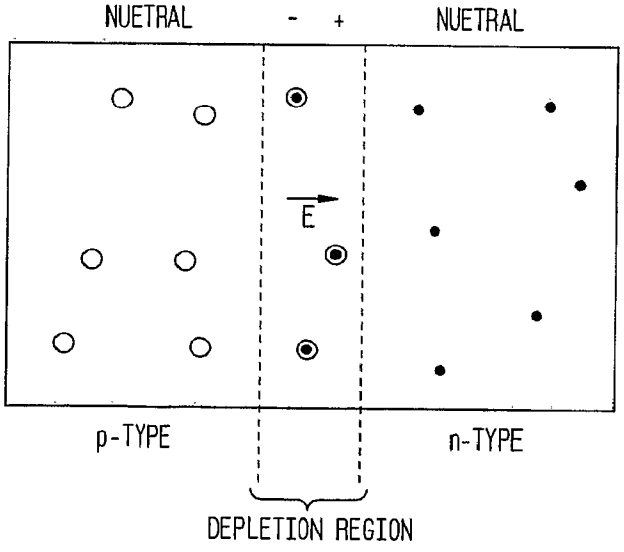

NUETRAL
-
+
NUETRAL
E
p-TYPE
n-TYPE
DEPLETION REGION

FIG. 11A

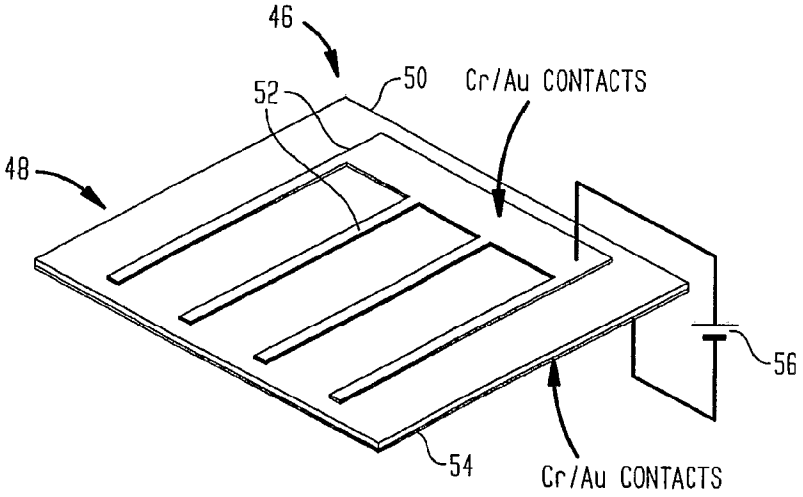


FIG. 11B

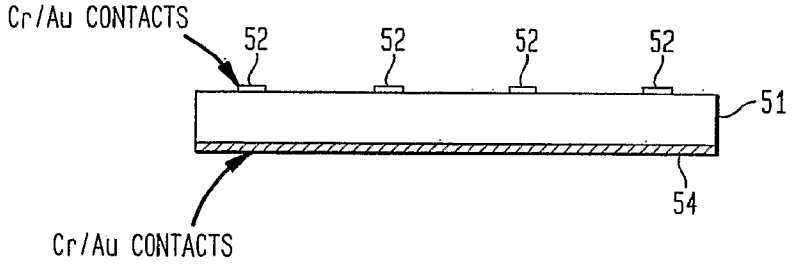


FIG. 12

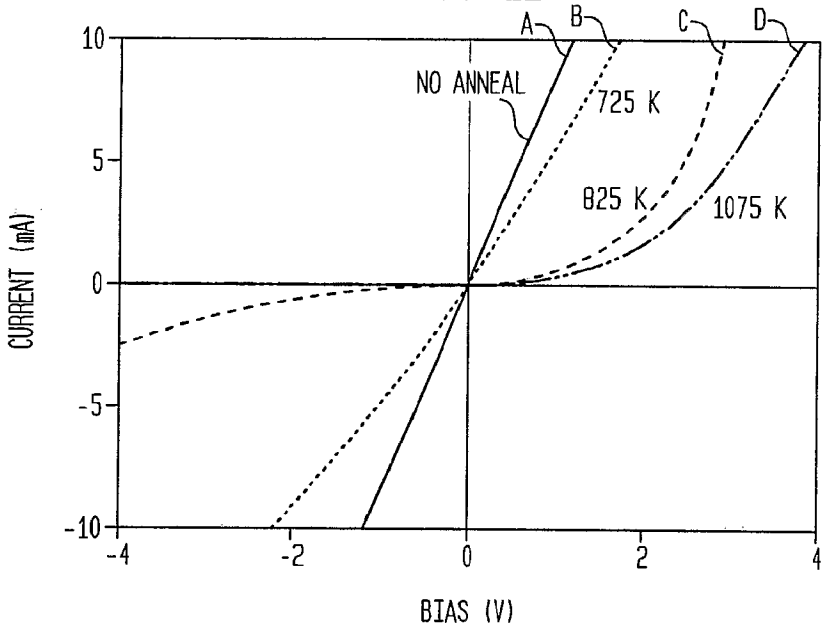

A
B
C
D
NO ANNEAL
725 K
825 K
1075 K
10
5
0
-5
-10
-4
-2
0
2
4
CURRENT (mA)
BIAS (V)

FIG. 13

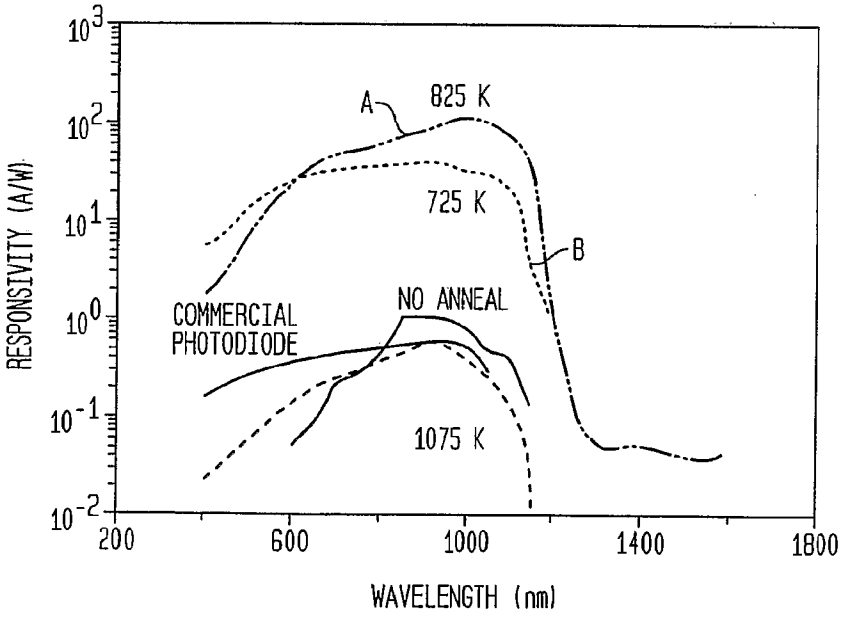

10^3
10^2
10^1
10^0
10^{-1}
10^{-2}
A
825 K
725 K
B
NO ANNEAL
COMMERCIAL
PHOTODIODE
1075 K
200
600
1000
1400
1800
RESPONSIVITY (A/W)
WAVELENGTH (nm)

FIG. 14

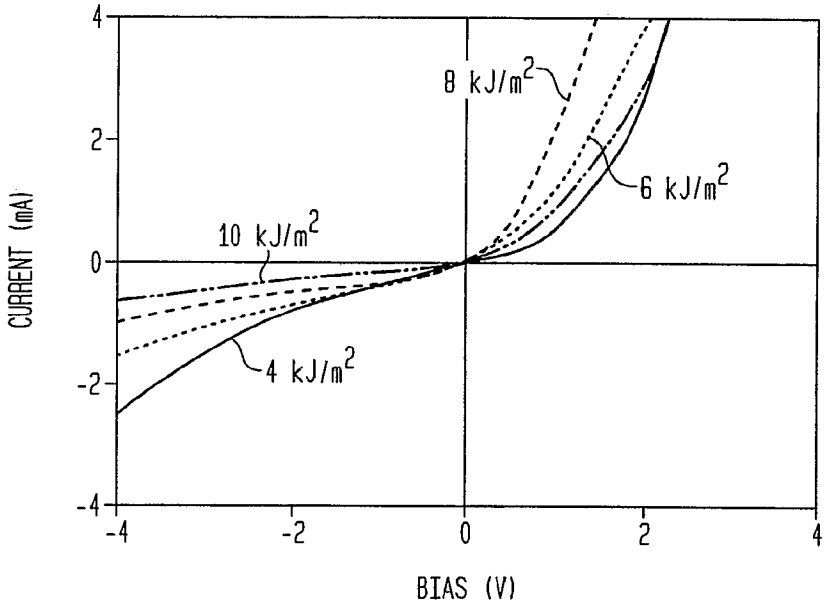


FIG. 15A

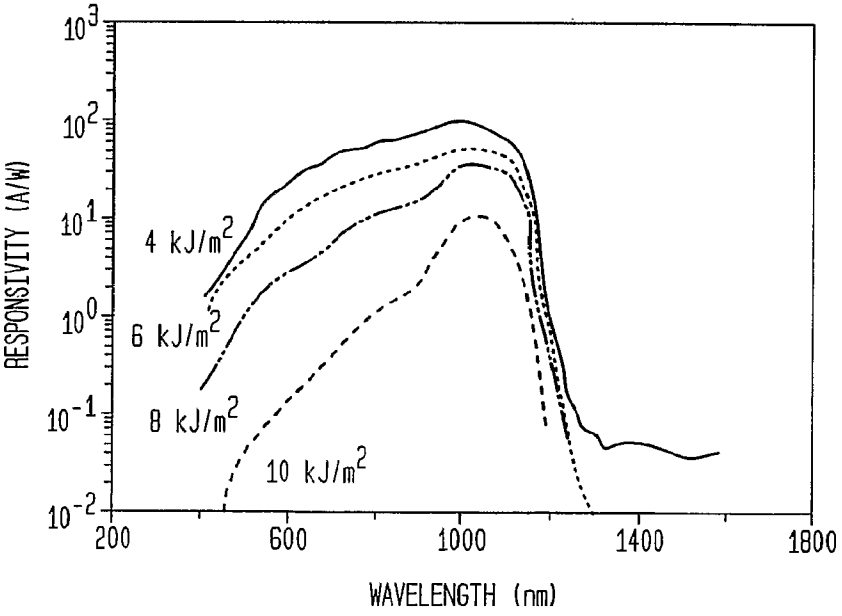


FIG. 15B

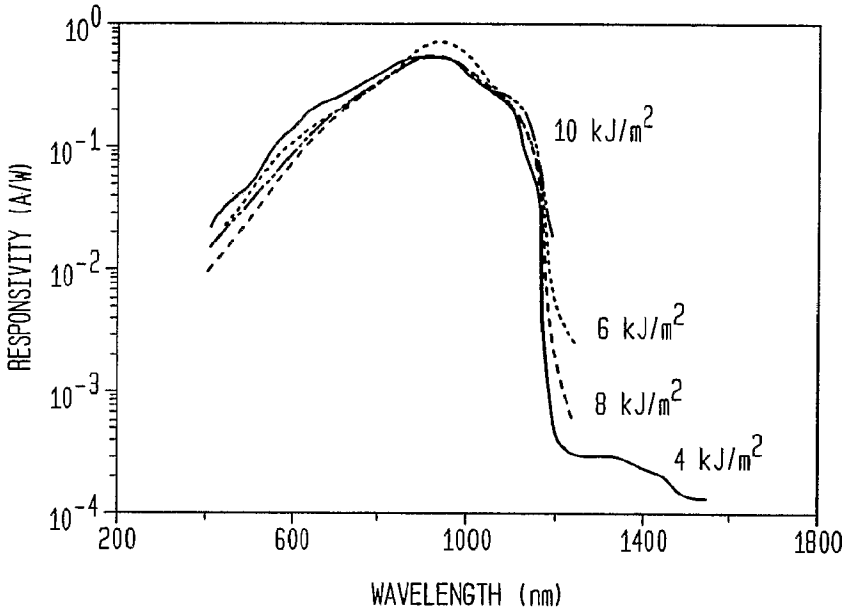


FIG. 16A

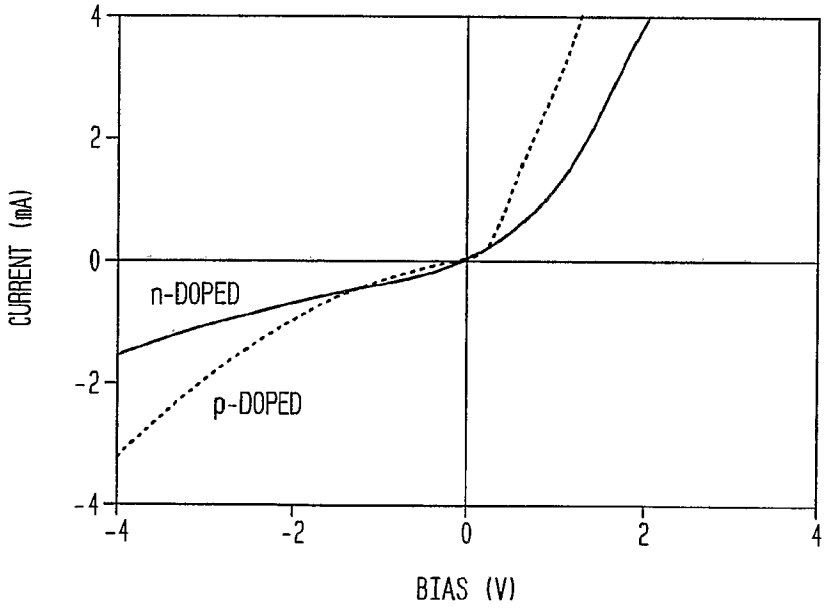


FIG. 16B

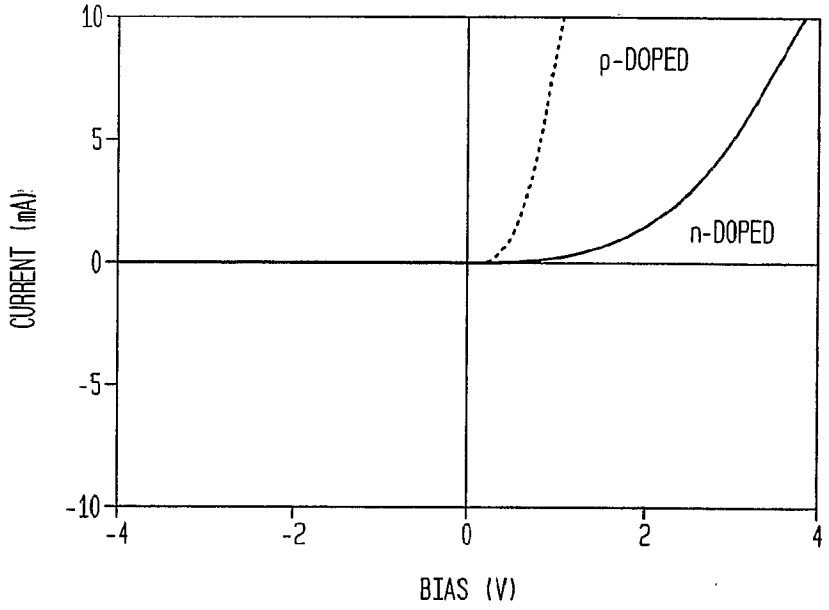


FIG. 17A

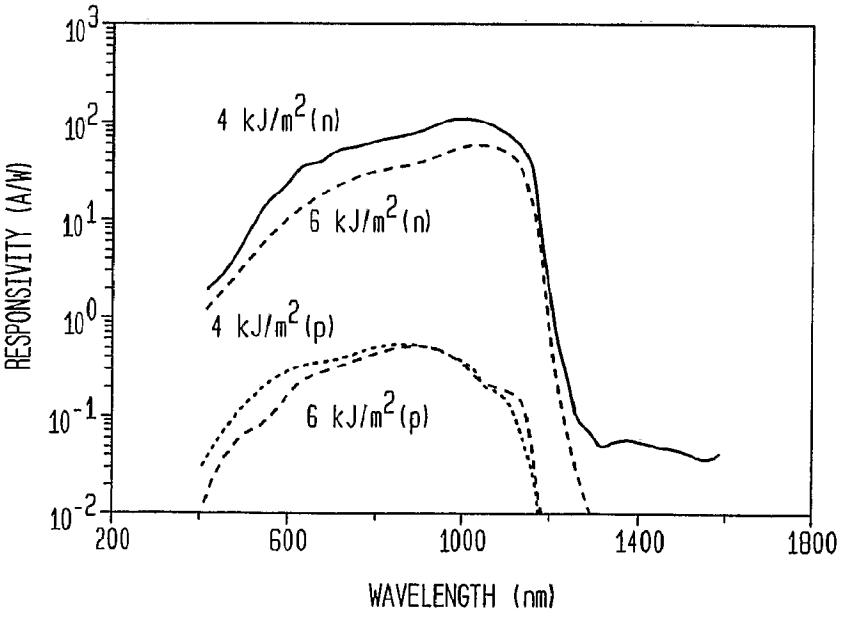


FIG. 17B

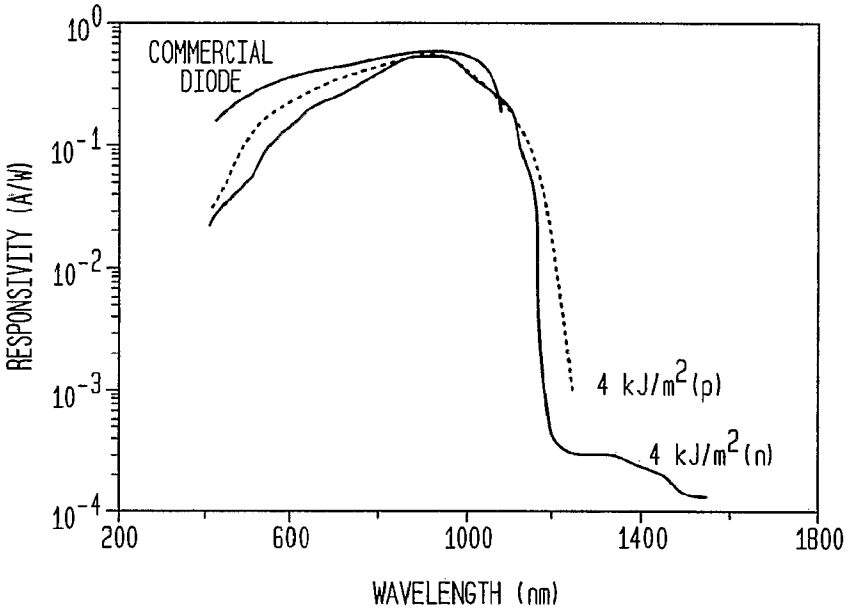


FIG. 18

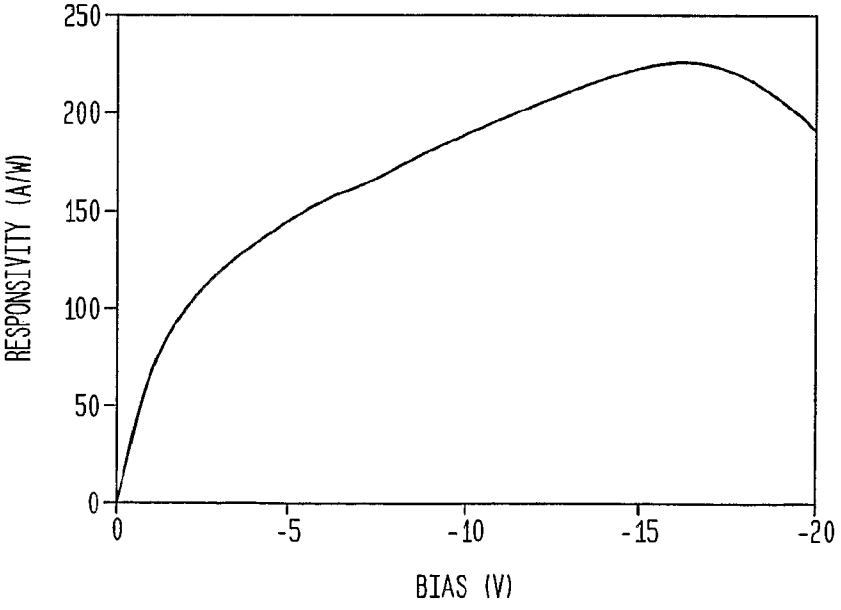


FIG. 19A

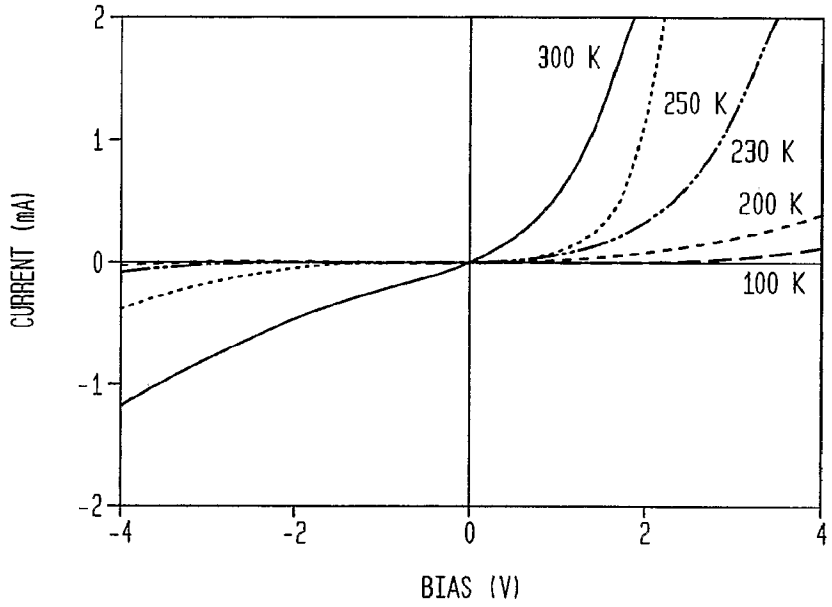


FIG. 19B

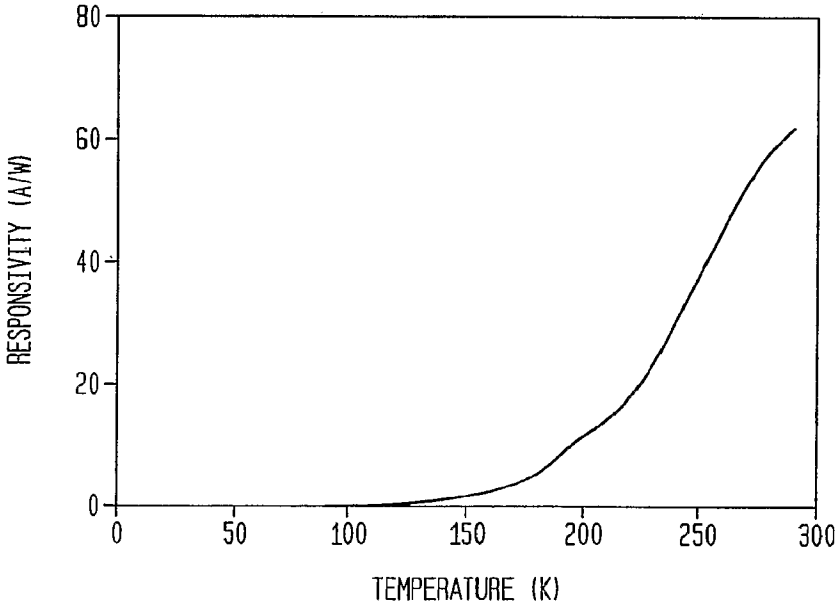


FIG. 20

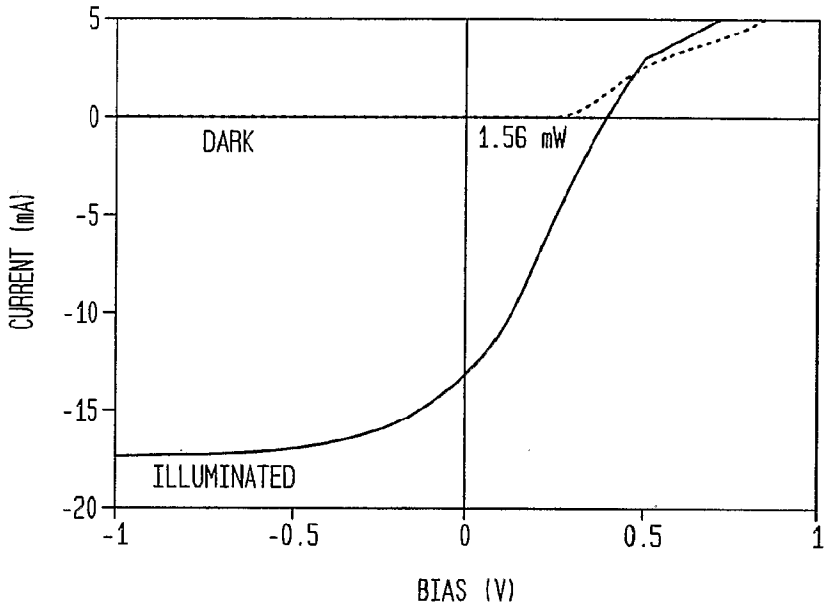

5
0
-5
-10
-15
-20
-1
-0.5
0
0.5
1
DARK
1.56 mW
ILLUMINATED
CURRENT (mA)
BIAS (V)

FIG. 21

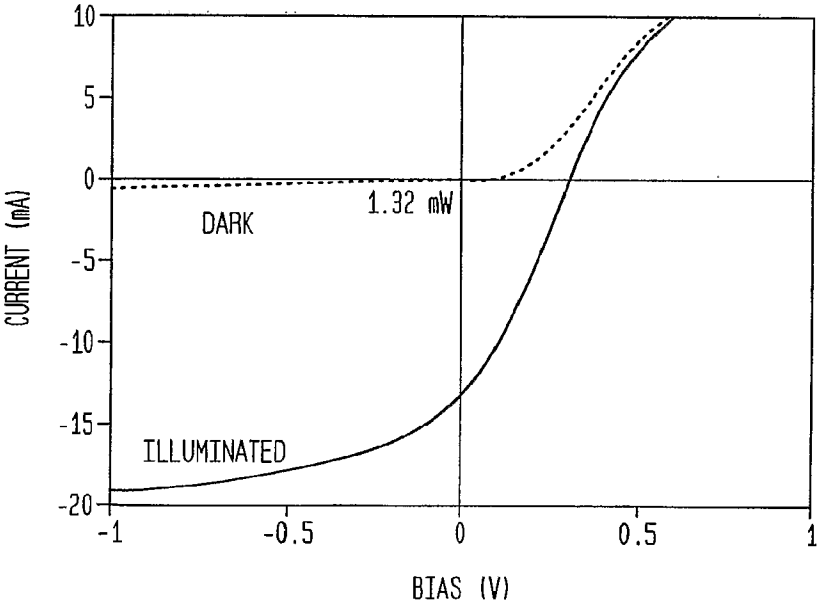

10
5
0
-5
-10
-15
-20
-1
-0.5
0
0.5
1
DARK
1.32 mW
ILLUMINATED
CURRENT (mA)
BIAS (V)

FIG. 22

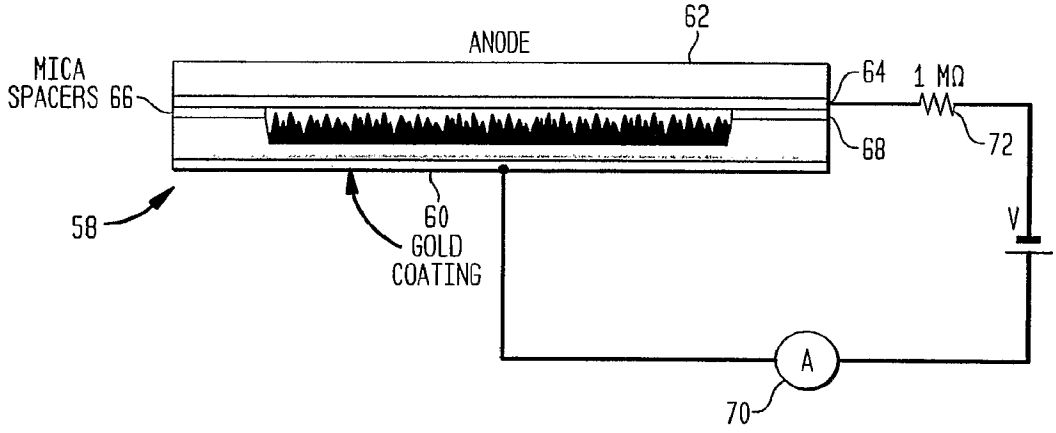
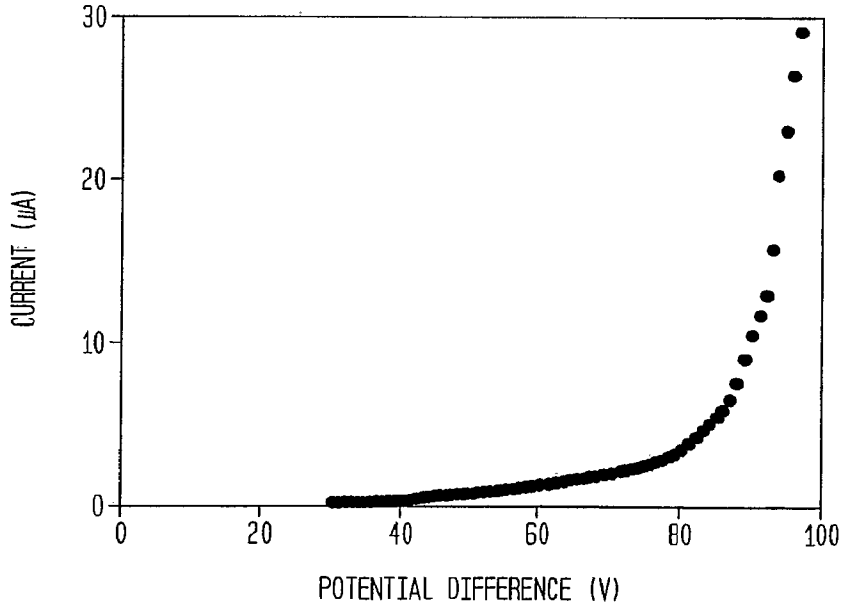

62
ANODE
MICA
SPACERS 66
64
1 MΩ
68
72
58
60
GOLD
COATING
V
A
70

FIG. 23


30
20
10
0
CURRENT (μA)
0
20
40
60
80
100
POTENTIAL DIFFERENCE (V)

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60/860,735	22 November 2006 (22.11.2006)	US

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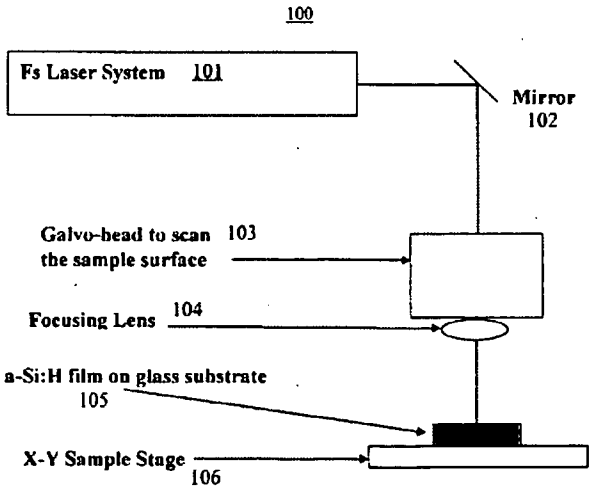


FIG. 1

(57) Abstract: The surface of a material is textured and crystallized in a single step by exposing the surface to pulses from an ultrafast laser. The laser treatment causes pillars to form on the treated surface. These pillars provide for greater light absorption. The crystallization of the material provides for higher electric conductivity and changes in optical properties of the material. The method may be performed in a gaseous environment, so that laser assisted chemical etching will aid in the texturing of the surface. This method may be used on various material surfaces, such as semiconductors, metals, ceramics, polymers, and glasses.

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SYSTEMS AND METHODS OF LASER TEXTURING AND CRYSTALLIZATION OF MATERIAL SURFACES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from U.S. Provisional Patent Application No. 60/752,545, filed on December 21, 2005; U.S. Provisional Patent Application No. 60/843,874, filed on September 12, 2006; and U.S. Provisional Patent Application No. 60/860,735, filed on November 22, 2006. The full disclosures of these provisional applications are incorporated herein by reference.

STATEMENT OF GOVERNMENT INTEREST

[0002] The present invention was developed under National Science Foundation Grant No. GA10507-31335 427250. The government has certain rights in the invention.

FIELD OF THE INVENTION

[0003] Apparatuses and methods consistent with the present invention relate to modifying surfaces, and more particularly, to modifying surfaces of thin films in order to alter their thermal, structural, optical, and electrical properties.

BACKGROUND OF THE INVENTION

[0004] Laser processing provides a unique method of modifying materials by depositing large amounts of energy onto the surface of a material in an extremely controlled manner. Laser processing enables the precisely localized treatment of a material. Laser processing is particularly useful after thin-film deposition of amorphous materials, which usually involves low temperature processing, and allows for the use of flexible and low melting temperature

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substrates for large area device fabrication. However, these devices lack better performance, usually due to poor electrical, optical, and/or structural properties. Laser processing of these devices with ultra-short laser pulses has been found to improve the properties of the devices, because the high peak intensities of the laser pulses rapidly texture the surface, and a subsequent quenching process induces crystallization in the material. The texturing of the surface leads to more light absorption in the material, and the subsequent crystallization improves the electronic properties of the material.

[0005] For example, thin film amorphous silicon (a-Si) based devices are inexpensive compared to their crystalline counterparts because of low temperature processing, which is suitable for deposition on large substrates, such as glass, plastic, and steel foils. However, solar cell devices fabricated using a-Si thin-films lack efficiency, have a high reflectivity across the electromagnetic spectrum, possess a larger band gap (~ 1.7 eV), and have limited carrier mobility. In order to improve the efficiency and sensitivity of a-Si based devices, post-deposition laser processing is usually recommended. This includes texturing and subsequent crystallization of the surface. Pulsed laser crystallization of thin a-Si films on various substrates has potential applications in the fabrication of thin film transistors for active matrix liquid crystal displays and efficient solar cells. Typically, nanosecond or microsecond lasers are utilized to crystallize such films through a rapid melting and solidification process. Methods of using a laser to crystallize a material surface are also disclosed by U.S. Patent No. 6,169,014 to McCulloch, U.S. Patent No. 6,451,631 to Grigoropoluos et al., U.S. Patent No. 6,489,188 to Jung, and U.S. Patent No. 6,635,932 to Grigoropoluos et al.

[0006] Methods of using an ultrafast laser to texture the surface of crystalline bulk silicon are disclosed in U.S. Patent Application No. 10/155,429 to Mazur. Mazur discloses a method of texturing the surface of a silicon substrate by irradiating the surface with ultra-short laser

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pulses in the presence of a background gas, such as SF_6. After texturing, the silicon surface in Mazur contains cone-like microstructures that are up to 50 μm high, and have widths of about 0.8 μm near the tip and up to 10 μm near the base. Also, Mills and Kolasinski disclose nanospikes formed atop silicon pillars when the sample is exposed to SF_6 gas diluted with helium (17 Nanotechnology 2471, 2006). Further, Vorobyev and Guo disclose the formation of nanoprotrusions with spherical tips on copper, gold, and platinum surfaces by using a femtosecond laser ablation technique (14 Optics Express 2164, 2006).

[0007] While the prior art discussed above provides important advantages, it suffers from a number of drawbacks. The prior art fails to disclose a method of producing periodic arrays of pillar structures on a surface of a material by texturing the surface. Further, the prior art does not teach a method of texturing and crystallizing a surface in one step. Also, the prior art does not teach a method of forming pillar structures on metal surfaces. In addition, the prior art fails to disclose a method of utilizing laser texturing and crystallization in many novel applications.

SUMMARY OF THE INVENTION

[0008] Exemplary embodiments of the present invention overcome the above disadvantages and other disadvantages not described above. Also, the present invention is not required to overcome the disadvantages described above, and an exemplary embodiment of the present invention may not overcome any of the problems described above.

[0009] The present invention provides a method for texturing a surface of a semiconductor material, including providing an etching gas in an area around the surface of the material, irradiating a portion of the surface with short laser pulses, and translating at least one of the surface and a laser beam to allow the short laser pulses to impact another portion

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of the surface. This method produces a periodic array of pillar structures on the surface, resulting in changes in properties of the surface.

[0010] According to an aspect of the present invention, the method additionally produces nanospikes atop the pillar structures.

[0011] Also, the present invention provides a method for texturing a surface of a semiconductor material, including providing an etching gas in an area around the surface of the material; irradiating a portion of the surface with short laser pulses while simultaneously crystallizing the portion of the surface; and translating at least one of the surface and a laser beam to allow the short laser pulses to impact another portion of the surface. This method produces pillar structures on the surface, resulting in changes in properties of the surface.

[0012] In addition, the present invention provides a method for texturing a metallic surface, including irradiating a portion of the metallic surface with short laser pulses, and translating at least one of the surface and a laser beam to allow the short laser pulses to impact another portion of the surface. This method produces pillar structures on the surface, resulting in changes in properties of the surface.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The above and other aspects of the present invention will be better understood from a consideration of the following detailed description of exemplary embodiments of the present invention, and the accompanying drawings, in which:

[0014] **FIG. 1** illustrates the components in a surface modification system, according to an exemplary embodiment of the present invention;

[0015] **FIG. 2** illustrates an example of a sample material to which surface modification is performed, according to an exemplary embodiment of the present invention;

[0016] **FIG. 3** is a photograph of a hydrogenated amorphous silicon (a-Si:H) surface, with **FIG. 3(a)** illustrating a non-modified portion, and **FIG. 3(b)** illustrating a modified portion, according to an exemplary embodiment of the present invention;

[0017] **FIG. 4** illustrates scanning electron microscopy (SEM) images of an a-Si:H surface, with **FIG. 4(a)** illustrating a non-modified portion, and **FIG. 4(b)** illustrating a modified portion, according to an exemplary embodiment of the present invention;

[0018] **FIG. 5** illustrates graphical results of absorption versus wavelength for an a-Si:H surface, with **FIG. 5(a)** illustrating the absorption for an untreated sample, and **FIG. 5(b)** illustrating the absorption for a treated sample, according to an exemplary embodiment of the present invention;

[0019] **FIG. 6** illustrates graphical results of an X-ray diffraction pattern for an a-Si:H surface, with **FIG. 6(a)** illustrating the results for an untreated sample, and **FIG. 6(b)** illustrating the results for a treated sample, according to an exemplary embodiment of the present invention;

[0020] **FIG. 7** illustrates graphical results of current versus voltage for an a-Si:H surface with varying light levels, with **FIG. 7(a)** illustrating the results for an untreated control sample,

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and **FIG. 7(b)** illustrating the results for a treated sample, according to an exemplary embodiment of the present invention;

[0021] FIG. 8 illustrates an atomic force microscope image of an a-Si:H surface that has been treated according to an exemplary embodiment of the present invention;

[0022] FIG. 9 is a graph illustrating the average roughness of laser treated a-Si:H surfaces at different laser fluences, according to an exemplary embodiment of the present invention;

[0023] FIG. 10 illustrates results of X-ray photoelectron spectroscopy (XPS) measurements of a-Si:H surfaces, with **FIG. 10(a)** illustrating the XPS measurement of untreated control surfaces, **FIG. 10(b)** illustrating the XPS measurement of treated surfaces, and **FIG. 10(c)** illustrating depth profiles of oxygen concentration for untreated control and treated surfaces, according to an exemplary embodiment of the present invention;

[0024] FIG. 11 is a graph illustrating the reflectivity of surfaces of polished silicon, unpolished silicon, and treated a-Si:H surfaces, according to an exemplary embodiment of the present invention;

[0025] FIG. 12 is a graph illustrating the transmission of samples of unpolished silicon and treated a-Si:H surfaces, according to an exemplary embodiment of the present invention;

[0026] FIG. 13 illustrates SEM images of germanium surfaces, with **FIG. 13(a)** illustrating an SEM image viewed at 45° from the surface normal, **FIG. 13(b)** illustrating a higher magnification SEM image showing nanospikes formed on each germanium pillar, **FIG. 13(c)** illustrating a single nanospike of a treated sample, and **FIG. 13(d)** illustrating a nanotip formed after brief chemical etching, according to exemplary embodiments of the present invention;

[0027] FIG. 14 shows a comparison of SEM images viewed at 45° from the surface normal of Ge (100) surfaces irradiated at different laser power levels, with **FIG. 14(a)** showing a surface irradiated with a laser power of 0.66 J/cm^2, **FIG. 14(b)** showing a surface irradiated

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with a laser power of 0.56 J/cm^2, **FIG. 14(c)** showing a surface irradiated with a laser power of 0.3 J/cm^2, and **FIG. 14(d)** showing a surface irradiated with a laser power of 0.2 J/cm^2, according to embodiments of the present invention;

[0028] FIG. 15 is graphical representation of an X-ray diffraction pattern of a laser treated germanium surface having nanospikes, according to an exemplary embodiment of the present invention;

[0029] FIG. 16 illustrates SEM images of treated surfaces, with **FIG. 16(a)** illustrating an image taken towards the edge of the scanned line for a Ge (100) surface, **FIG. 16(b)** indicating ball formation instead of spikes for a Ge (100) surface, and **FIG. 16(c)** illustrating an image taken in the middle of the scanned line for a Si (100) surface, according to exemplary embodiments of the present invention;

[0030] FIG. 17 illustrates SEM images of pillars, viewed at 45° from the surface normal, formed on a silicon surface, with **FIG. 17(a)** illustrating an SF_6 gaseous environment, and **FIG. 17(b)** illustrating an HCl gaseous environment, according to exemplary embodiments of the present invention;

[0031] FIG. 18 illustrates SEM images of pillars, viewed 45° from the surface normal, formed on a germanium surface, with **FIG. 18(a)** illustrating an SF_6 gaseous environment, and **FIG. 18(b)** illustrating an HCl gaseous environment, according to exemplary embodiments of the present invention;

[0032] FIG. 19 illustrates SEM images periodic structures formed on a silicon surface, with **FIG. 19(a)** illustrating a one-dimensional periodic structure, and **FIG. 19(b)** illustrating a two-dimensional periodic structure, according to embodiments of the present invention;

[0033] FIG. 20 illustrates SEM images of titanium surfaces, with **FIG. 20(a)** illustrating a titanium surface treated in air, **FIG. 20(b)** illustrating a titanium surface treated in vacuum, **FIG. 20(c)** illustrating a titanium surface treated in helium, and **FIG. 20(d)** illustrating a

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titanium surface treated in SF_6, according to exemplary embodiments of the present invention;

[0034] FIG. 21 illustrates SEM images of stainless steel surfaces, with **FIG. 21(a)** illustrating a stainless steel surface treated in air, **FIG. 21(b)** illustrating a stainless steel surface treated in vacuum, **FIG. 21(c)** illustrating a stainless steel surface treated in helium, and **FIG. 21(d)** illustrating a stainless steel surface treated in SF_6, according to exemplary embodiments of the present invention;

[0035] FIG. 22 illustrates SEM images viewed at 45° from the surface normal, with **FIG. 22(a)** illustrating a treated SiC surface, **FIG. 22(b)** illustrating a treated GaAs surface, **FIG. 22(c)** illustrating a treated titanium surface, and **FIG. 22(d)** illustrating a treated stainless steel surface, according to exemplary embodiments of the present invention;

[0036] FIG. 23 is a schematic representation of field emission from the treated surface, according to exemplary embodiments of the present invention;

[0037] FIG. 24 is a schematic representation of reflectivity and absorption of the treated surface, according to exemplary embodiments of the present invention;

[0038] FIG. 25 is a schematic representation of the effect on external flow by the treated surface, according to exemplary embodiments of the present invention;

[0039] FIG. 26 is a schematic representation of photovoltaic and photodetection applications using the treated surface, according to exemplary embodiments of the present invention;

[0040] FIG. 27 is a schematic representation of heat dissipation using the treated surface, according to exemplary embodiments of the present invention;

[0041] FIG. 28 is a schematic representation of surface marking created by surface alternations, according to exemplary embodiments of the present invention; and

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[0042] **FIG. 29** is a schematic representation of the placement of chemical or biochemical materials at the tips on the treated surface, according to exemplary embodiments of the present invention.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS OF THE INVENTION

[0043] In describing an exemplary embodiment of the present invention illustrated in the drawings, certain specific terminology will be used for the sake of clarity. However, the invention is not intended to be limited to that specific terminology, and it is to be understood that the terminology includes all technical equivalents that operate in a similar manner to accomplish the same or a similar result.

[0044] Apparatuses and methods consistent with the present invention texture and crystallize the surface of a material in one step by exposing the surface of the material to an ultrafast laser. In order to expose an area of the surface that is larger than the beam spot size, the material may be translated relative to the laser. The texturing causes pillars to form on the surface of the material, increasing the light absorption of the treated material. Pillars are height variations over a surface, including valleys and hills. Pillars can be formed in a variety of shapes, including conical, arrowhead, pyramid, and spheroid structures. The top of the pillar has a narrower diameter than the bottom of the pillar. Additionally, crystallization increases the electrical conductivity of the treated material. Texturing and crystallizing the surface of the material in a single step allows for faster manufacturing and lower costs than performing these steps separately.

[0045] The texturing and crystallization may be performed under atmospheric conditions, or while the material to be treated is in a non-atmospheric gaseous environment. In such a gaseous environment, additional surface texturing will occur through chemical etching. Sulfur hexafluoride and hydrogen chloride gases have been examined, and have been shown

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to be suitable gases in which to perform the surface texturing. Hydrogen chloride is advantageous over sulfur hexafluoride, because when sodium hexafluoride is used, impurities in the material may result. In contrast, when hydrogen chloride is used, no impurities are created, and the material remains in its pure form. It is to be understood that other gases may also be used. Surface texturing and crystallization have also been achieved in a helium gas environment and in a vacuum.

[0046] The materials that have undergone surface texturing and crystallization are also within the scope of the present invention. For amorphous materials, the surface will become textured and the material will become crystallized. Hydrogenated amorphous silicon has been examined using the method of the invention, and has been shown to be well-suited to benefit from this method. Thin-film, poly-crystalline, and single crystal materials may also be used. These materials will benefit from the surface texturing methods of the present invention. Silicon and germanium have been studied, and have been shown to be suitable materials to undergo the laser treatment method in the presence of sodium hexafluoride gas and hydrogen chloride gas. Metals, dielectrics, and polymers have also been shown to be suited to be textured using the method of the present invention. However, it is to be appreciated that other materials are suited to undergo the laser treatment methods of the present invention.

[0047] Additionally, the use of materials that have undergone the treatment methods of the present invention is within the scope of the present invention. The present invention has many useful applications. The methods described herein will provide for a material with a higher light absorption capacity and a higher electrical conductivity than an untreated material. These two properties are desirable in photovoltaic applications. Enhanced light trapping capabilities are also useful in photo-sensing applications. Photodetectors utilizing

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the present invention will be more sensitive to light, and will be able to detect a broader spectrum of electromagnetic waves.

[0048] The surface texturing greatly enhances the heat transfer capability of a given material. A material that has been textured can dissipate more heat through convection because of the increased surface area of the material that is exposed to a fluid flowing over the material. Additionally, the texturing will ensure a turbulent flow of the fluid, which is advantageous in convection heat transfer. For radiation heat transfer, the increased surface area will allow for more heat dissipation.

[0049] In an exemplary embodiment of the present invention, the surface alteration process was performed on hydrogenated amorphous silicon (a-Si:H), in particular a-Si:H thin films. Thin films with thicknesses from 1.5 to 2 μm were deposited on glass substrates, using a low temperature Plasma Enhanced Chemical Vapor Deposition (PECVD) technique. The a-Si:H films were deposited at a rate of around 1 Å/s in a hydrogen diluted silane environment at about 200°C. The samples were then treated using a femtosecond Ti:Sapphire laser system (Spectra-Physics Spitfire). The laser system delivered pulses at a repetition rate of 1 kHz, with a pulse energy that could vary from 0-1.2 mJ, and a wavelength of 800 nm. The wavelength of the laser can also be frequency doubled or halved to achieve wavelengths from 200 to 1600 nm. The temporal profile of the pulses was measured to be 110 fs using a background free, scanning second-order auto-correlator. The sample was placed on a stationary stage, and the laser beam was deflected by a Scanlab galvo-head to scan the sample surface. The beam spot on the sample surface was circular, with a beam diameter of 0.5 mm. The beam scanning speed was around 12.5 cm/sec. Scanning electron micrographs of treated and untreated surfaces of the a-Si:H films were taken using a Cambridge Instruments high resolution electron microscope for a surface texture study.

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Surface roughness and formation of spikes in the treated films were also examined with an atomic force microscope (Digital Instruments Nanoscope III).

[0050] The optical transmission and reflection of a 20 mm × 30 mm laser treated area of the sample was measured using a PERKIN-ELMER LAMBDA 9 spectrophotometer. The reflectance and transmittance percentages were then used to obtain the absorption percentage in the material: $A = 100 - R - T$. Light from a He-Ne laser source was incident on the treated sample at different angles, and the scattered light was measured by a silicon sensor with an active region of around 4 cm^2 to estimate the scattering of light due to texturing. It was observed from the measurements that scattering might contribute to a 5-10% variation in the reflection measured by the spectrophotometer. In addition to the optical properties, X-ray diffraction (XRD) was performed on the untreated and laser treated samples to study the structural modification induced by the laser treatment. The Rigaku Miniflex 2005 X-ray diffractometer with a Cu target (CuK_{α}-line) was used for the XRD measurements. The grain size of the treated films was estimated from the X-ray data. Also, the oxygen incorporation into silicon films during this ultrafast laser treatment was studied using a Physical Electronics Inc. 560 XPS/SAM spectrophotometer with a dual source anode (Mg/Al) radiating 1253.6 eV X-ray photons.

[0051] FIG. 1 shows an exemplary system 100 that can be used to provide surface modifications. The femtosecond laser system 101 provides a laser pulse incident on the a-Si:H sample 105, which is supported by an X-Y sample stage 106. The system 100 uses a mirror 102 to direct the laser pulse to a galvo-head unit 103, which scans the sample surface. A focusing lens 104 is used to focus the pulses on the surface. An exemplary a-Si:H sample 200 is illustrated in FIG. 2, with a glass slide 205, an intervening layer 204, and amorphous silicon layers 201-203.

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[0052] FIG. 3 illustrates that the change in the surface of the a-Si:H film deposited on the glass substrate can be observed optically. FIG. 3(a) shows a photograph of the untreated surface, and FIG. 3(b) shows a photograph of the treated surface. After treatment, the a-Si:H films turned completely dark, in contrast with their original shiny reddish gray color. FIG. 4(a) shows an SEM image of the untreated surface, and FIG. 4(b) shows an SEM image of the treated surface. FIG. 4(b) shows that microstructures and small spikes have been spontaneously formed upon laser treatment.

[0053] In order to study the optical characteristics, the reflectance and transmittance of a treated 20 × 30 mm^2 area were measured using a spectrophotometer. FIG. 5 shows the absorptance of treated and untreated a-Si:H films. FIG. 5(b) that there is a significant enhancement in the optical absorption below a-Si:H band gap (1.7 eV) for treated films, when compared to the untreated films in FIG. 5(a). Since the experiments were carried out under atmospheric conditions, XPS spectra of a treated sample (FIG. 10(b)) and an untreated control sample (FIG. 10(a)) were also obtained. SiO_x formation was observed in the treated sample. The oxygen concentration was estimated by taking XPS measurements at different depths of the sample. Depth profiles of the oxygen concentration in the treated and untreated control samples are shown in FIG. 10(c). Traces of oxygen were observed up to a depth of around 50 nm in treated samples, compared to a depth of 10 nm in the untreated control sample. The samples appeared to be pitch black after treatment, and it is suggested that the below-band edge absorption might be due to trapping the light, which is caused by multiple reflections from the textured surface. Also, structural defects induced during the micro-structuring process most likely produce bands of defect and impurity states in the bandgap, and further enhance the overall absorption.

[0054] FIG. 6(a) shows the X-ray diffraction pattern for an untreated a-Si:H sample, and FIG. 6(b) shows an X-ray diffraction pattern for a treated a-Si:H sample. Peaks around 2θ =

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30° and 56° are observed for the treated sample. These peaks are absent in the untreated control sample, indicating a structural change after laser treatment. The X-ray wavelength used for these measurements was the CuK_{α} line at 1.54 Å. The observed peaks are due to the (111) and (311) orientations of crystalline silicon. Regardless of the fluence conditions, the (111) orientation dominated in the crystallized films, as the (111) plane has least surface energy. Dominant (111) and (311) peak formation is typically observed in nanosecond laser crystallization. The (111) peak was fitted with a Gaussian curve and the full width at half-maximum (FWHM) was determined. The particle size was determined to be around 85 nm using the Scherrer's formula: $L = k^{*}\lambda / \Gamma \cos\theta$; where λ is the X-ray wavelength for measurement; Γ is the X-ray line width (FWHM) (measured in radians); θ is the Bragg angle of diffracted rays (measured in degrees); and k is a constant equal to 0.9.

[0055] The current-voltage characteristics of the treated and untreated a-Si:H samples were also examined, as shown in FIG. 7. FIG. 7(a) shows a graph of the current density as a function of voltage for several light levels for the untreated sample. As illustrated in FIG. 7(b), the current-voltage characteristics change considerably, due to the surface modification and changes in the properties of the material. The transmission and reflectivity of the treated and untreated surfaces were also examined. The reflectivity of polished silicon, unpolished silicon, and treated silicon with pillars is shown in FIG. 11. Similarly, the transmission of the treated silicon versus the rough silicon surface is presented in FIG. 12. The changes in the optical properties shown in FIG. 3 are further substantiated by the changes in reflectivity and transmission as functions of wavelength. These results impact the use of silicon in many applications, as discussed below.

[0056] In order to measure the roughness and spike distribution, atomic force microscopy (AFM) images of the treated a-Si:H samples were obtained. FIG. 8 shows that spikes of a height of about 300 nm were formed, with a spacing between the tips of around 1 μm. The

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heights of these spikes were found to increase with laser fluence. The average height of the microstructures was 150 nm at a laser fluence of 0.3 J/cm^2, and the height increased nearly linearly with the laser fluence. Microstructures with a height of around 350 nm were observed at a fluence of 0.5 J/cm^2. Beyond 0.5 J/cm^2, the films became very rough, and material ablation deteriorated the texturing. Also, the average roughness of the surface correlates with the laser fluence, as illustrated in the graph in FIG. 9. FIG. 9 shows that the surface roughness increases approximately linearly with the laser fluence.

[0057] Increasing the efficiency of a-Si:H thin film solar cells requires more light absorption and a reduction in carrier recombination. A thick i-layer increases the light absorption, but recombination deteriorates the performance. On the other hand, for sufficiently thin film solar cells, the light absorption becomes an issue. Keeping a thin micro or nano crystalline phase with surface texturing could both reduce recombination and improve light trapping. The treated surface had a silicon oxide formation layer of about 50 nm, and was found to be semiconducting. This layer could be used as an n-layer in a p-i-n type solar cell, and an active layer for other optoelectronic devices. The simultaneous formation of light trapping structures and crystallization might find applications in devices such as thin film solar cells, large area sensors, and display devices.

[0058] As discussed previously, the femtosecond laser treatment results in the enhancement of optical absorption in a-Si:H thin films. The high absorption of the film is suggested to be due to the light trapping occurring in the silicon spikes formed at the surface after laser treatment, and the structural defects induced during micro structuring process most likely producing bands of defect and impurity states in the band gap. Also, crystallization in the film after femtosecond laser treatment is attributed to a non-thermal ultrafast phase transition and subsequent surface-initiated crystallization. By performing the surface

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texturing and crystallization as a one-step laser process, optoelectronic devices can be fabricated efficiently.

[0059] Exemplary embodiments of the present invention also form nanospiked, nearly periodic microstructures, by exposing a germanium surface to femtosecond laser pulses in a gaseous sulfur hexafluoride (SF_6) environment. The microstructures that are formed in germanium have a different aspect ratio than the microstructures formed on silicon. Because reducing light reflection and increasing absorption are key issues in improving optoelectronic device performance, this type of microstructure formation in germanium could lead to the fabrication of highly responsive infrared photodetectors and solar cells. In addition, these textured surfaces might find potential applications in the fabrication of biomedical devices and sensors.

[0060] The surface modification of germanium can occur according to the following process. Undoped Ge (100) wafers are cleaved into small chips and ultrasonically cleaned with acetone and methanol. One or more chips are put on a stage inside a vacuum chamber with a base pressure of around 1 mTorr, which is mounted on a high-precision computer-controlled X-Y stage. The chamber is rinsed with SF_6 at least twice, and then backfilled with SF_6 at 400 mbar. The samples are exposed to 1.4 mJ pulses of light with a wavelength of 800 nm, a pulse duration of 130 fs, and a repetition rate of 1 kHz from a regeneratively amplified Spectra-Physics Ti-sapphire laser system. The wavelength of the laser can be frequency doubled or halved to achieve wavelengths from 200 to 1600 nm. Short laser pulse widths can also be used, including 1 fs to 1 μs pulses. Ultrafast laser pulses are a subcategory of short pulses, and can range from 1 femtosecond to hundreds of picoseconds. The laser beam is focused along the surface normal onto the sample surface by a coated lens with a focal length of 1 m, and the laser fluence is adjusted with a Glan laser calcite polarizer.

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[0061] The spatial profile of the laser pulse is nearly Gaussian, but is elongated in one axis, creating an elliptical profile. The fluence is calculated by using the laser spot size, which is determined by exposing a point on the sample surface to thousands of shots. In order to scan an area that is bigger than the laser spot size, the samples are translated using a motorized X-Y stage. Scanning also assists in making the surface structure more uniform by smoothing out any shot-to-shot irregularities in the beam profile. By varying the scanning speed of the X-Y stage, the number of laser pulses impinging on the sample surface at a particular location is controlled. The spot size is 0.3 mm along the minor axis and 0.6 mm along the major axis. Scanning is performed parallel to the minor axis.

[0062] Samples are produced with isolated single line scans, or with large areas created by overlapping several line scans. The step size between the scan lines is chosen to be sufficiently small (generally 0.38 mm), so that successive lines overlap substantially. This further improves layer homogeneity. Homogeneity is further enhanced by performing two overlapping scans in orthogonal directions, rather than one overlapping scan with an exposure of the same total number of shots. After laser processing, the samples are analyzed with a scanning electron microscope (Zeiss SUPRA 40).

[0063] FIG. 13 shows an SEM image at increasing levels of magnification, viewed at 45° from the surface normal line of a germanium surface after exposing the surface to femtosecond laser pulses. Sharp conical structures with nanospikes are formed when the sample is under a pressure of 400 mbar SF_6, and is scanned by a laser beam with a fluence of about 0.6 J/cm^2. FIG. 13 shows that these structures are almost regular in position, are 10 to 15 μm tall, and have a base diameter around 5 μm, which tapers down to around 100 nm near the tip. The areal density of pillars in FIG. 13(a) is 0.027 μm^{-2}, which corresponds to a mean spacing of roughly 6 μm between pillars. The sizes of the microstructures vary across the scanned line, indicating a response to the spatial profile of the laser pulse. In the region of

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low fluence towards the edge of the irradiated line, the structures have a smaller height and are more densely packed than in the center.

[0064] FIG. 13(b) shows that the microstructures have two distinct features: (a) a conical shape (b) that is crowned with a very sharp spike, which has a radius of about 400 nm (about 100 nm at the tip), and is up to about 2 μm long (see FIG.13(c)). The tips can be sharpened further by a brief chemical etching with 100 ml H_2O_2 (10 vol %), 8g NaOH for 10 seconds at room temperature. Alternatively, the tips can be sharpened further by ion etching, including etching with an Argon ion beam. Nanoclusters, which are formed during laser ablation and deposited on the surface, are also evident from FIG. 13(b).

[0065] The SEM images of FIG. 14 show the effect of laser fluence on the surface texturing of germanium. In this figure, the average number of laser shots at each point on the sample surface is 400. The germanium surface in FIG. 14(a) was irradiated with laser pulses with a fluence of 0.66 J/cm^2, and the germanium surface in FIG. 14(b) was irradiated with laser pulses with a fluence of 0.56 J/cm^2. In contrast, the germanium surface in FIG. 14(c) was irradiated with laser pulses with a fluence of 0.3 J/cm^2, and the germanium surface in FIG. 14(d) was irradiated with laser pulses with a fluence of 0.2 J/cm^2. FIG. 14(d) shows that texturing is observed at fluences as low as 0.2 J/cm^2, resulting in features are smaller in width and height, less regular, less smooth, and densely populated, with very tiny or no spike formation. However, for higher fluence conditions, such as those in Figs. 14(a) and 14(b), the structures are more well-developed, sharper, and more conical, and spike-formation takes place atop the pillars. Also, increasing the number of laser shots from 400 to 600 and keeping the fluence almost the same wipes out all the spikes.

[0066] Germanium expands upon freezing. When a shell of germanium material starts freezing and expanding, it exerts pressure on the liquid trapped inside, causing the liquid to shoot upward and solidify to form nanospikes. As Mills and Kolasinski disclose, in order to

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obtain nanospikes in silicon, it is necessary to dilute the SF_6 with He. This reduces the chemical etching that results from the interaction of fluoride with the silicon surface. If the etching is too aggressive, it can remove the nanospikes. In contrast, it is unnecessary to dilute the SF_6 in order to obtain nanospikes on a germanium sample, probably because of differences in the chemistry of etching in the F/Ge system compared to the F/Si system. Another possible reason why germanium appears to be more conducive for nanospike formation might be that the thermal conductivity of undoped germanium is less than half of the thermal conductivity of undoped silicon. Therefore, the heat dissipation to the pillar in germanium is slower, and the liquid bulb remains in a molten state for a longer time, as compared to silicon.

[0067] In order to investigate the properties of the textured germanium surfaces, an X-ray diffraction study was conducted. FIG. 15 shows an X-ray diffraction spectrum of a laser textured germanium surface. The sharp high-intensity peak corresponds to the (400) plane, because the starting material is Ge (100). However, two relatively weak peaks at (111) and (220) are also observed. This indicates that the textured pillars and the nanospikes remain predominantly crystalline.

[0068] The SEM images of FIGs. 16(a) and 16(b) show the structural formations in germanium, and FIG. 16(c) compares the structural formations in silicon, after laser treatment under similar conditions. For all three samples the laser fluence was around 0.56 J/cm^2, the number of laser shots was around 600, the sample was in a gaseous SF_6 environment at 400 mbar, and an orthogonal scanning mode was used. The SEM image in FIG. 16(a) was taken toward the edge of the scanned line, while the SEM image in FIG. 16(b) was taken in the middle of the scanned line. FIG. 16 shows that the germanium pillars are not as smooth as the silicon pillars. Also, the aspect ratio, defined as the ratio of the tip height to the tip width, is higher in silicon than germanium for a given laser condition. For example, at a fluence of

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0.5 J/cm^2, silicon has an aspect ratio of around 200, whereas germanium has an aspect ratio of around 100. Also, as mentioned previously, spikes were not formed on germanium under higher laser shot conditions. However, pillars formed under higher laser shot conditions are taller than pillars formed under fewer shots, as shown in FIGs. 13 and 14. In contrast, silicon shows a well-developed smooth structure under a greater variety of shot conditions.

[0069] FIG. 16(a) shows that toward the edge of the laser scanned line on the germanium surface, pyramidal structures were formed, which tend to form a small spherical cap at the top, instead of the nanospikes formed in FIG. 16(b). This spherical cap formation is typical of silicon. The spherical shape of the cap suggests that a liquid germanium drop resolidified before it could spill over the pillar. The lack of nanospikes in FIG. 16(a) might be due to three possible reasons: (a) the fluence is low to achieve the high melting condition necessary for nanospike formation; (b) the higher number of laser shots destroyed nanospikes that were already formed; or (c) an insufficient density of nanostructures was formed. With further regard to (c), deposition of nanoclusters has been implicated in the formation of nanospikes. A sufficient nanoclusters deposition rate is required, and because fewer nanoclusters are formed at a lower fluence, there may be a critical fluence for the formation of nanospikes, not only because a sufficient melt must be formed, but also because a sufficient density of nanoclusters must be created.

[0070] FIG. 17 shows SEM images viewed at 45° from the surface normal of sharp conical pillars formed on the surface of B-doped Si (100) wafers. The pillars were produced with 240 shots of 130-fs laser pulses at a fluence of 0.6 J/cm^2. FIG. 17(a) shows the results for a sample in 400 mbar of SF_6, and FIG. 17(b) shows the results for a sample in 400 mbar of HCl. The pillar size varies across the scanned laser line, indicating the intensity variation of the laser fluence across the spatial profile of the laser pulse. The scan lines were

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overlapped to minimize height variation over a large area on the sample surface. The spikes that are obtained in SF_6 are around 15 μm tall and have a base diameter of around 5 μm.

[0071] On the other hand, the structures formed under similar laser conditions in the presence of HCl are composed of taller and wider pillars, with a height of around 20 μm and a base diameter of around 7 μm. FIGs. 17(a) and 17(b) show that the pillars formed in SF_6 are narrower towards the tips, compared to the pillars formed in HCl. Although the pillar density is comparable in both cases, the pillars formed in HCl look stronger and are relatively blunt towards the tip, indicating that differences in the etch chemistry of the F/Si system and the Cl/Si system are responsible for significant structural differences.

[0072] The role of chemistry in structure formation is not well understood, and it is a significant result that regular conical pillars are formed during femtosecond irradiation in SF_6 as well as HCl. Regular conical pillars can be formed during nanosecond irradiation of silicon in the presence of SF_6, but they are not formed for nanosecond irradiation of silicon in the presence of HCl. Nanosecond irradiation of silicon in HCl produces significantly blunter tips, the pillars are much taller, with a height greater than 50 μm, and the pillars are porous, instead of having a solid core. This is a further indication that the mechanisms of pillar formation are different for the femtosecond and nanosecond irradiation regimes. This result is also significant because chemical impurities, namely sulfur, incorporated during laser processing have been implicated in changing the optical and electronic properties of the textured surfaces.

[0073] FIG. 18 shows SEM images taken for germanium samples treated under similar laser and gaseous conditions as described above for silicon. A very different surface texturing was created for germanium. FIG. 18(a) shows that for germanium processed in SF_6, there were two distinct features that were not observed for silicon treated under similar conditions: (a) conical pillar formation with a higher cone angle up to a neck; and (b) very

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sharp spikes, up to about 2 μm in length with a tip radius of about 100 nm, formed atop the pillars. Nanoclusters formed during laser ablation are more abundant in germanium than silicon under similar laser conditions, which might be due to the lower melting temperature of germanium. On the other hand, FIG. 18(b) shows that the germanium structures formed in the presence of HCl are less densely populated, shorter, have a higher cone angle and a wider base, and exhibit greater variations in pillar height than the silicon structures shown in FIG. 17(b). Gas phase silicon etching is anisotropic in HCl, and the etch rate is around 20 μm min^{-1} for the (100) plane at temperatures in the range of 1050–1250°C, whereas in germanium the etch rate is around 3 μm min^{-1}, the etch rate is independent of temperature beyond 800°C, and etching leads to the development of square pits for the (100) orientation. The differences in etch chemistry are involved in determining the different structure formation dynamics, which result in more regular spike formation in HCl for silicon than for germanium.

[0074] Laser induced surface texturing that produces regular structures on materials in the presence of reactive species is a complex process involving: (1) interactions between the plume and the process gas, and the plume and the surface, such as decomposition of the reactive gas, chemical etching enhanced by laser heating of the material and the formation of radicals, and deposition out of the plume; (2) laser ablation of the material; and (3) optical phenomena that initiate the formation of regular structures. The laser parameters, gaseous environment, and nature of the substrate all play a role in the final outcome of the surface morphology. Structure formation is ultimately a convoluted dynamical process involving all three factors. The dimensions and character of the pillars formed in silicon have been shown to depend critically on the temporal pulse width of the laser beam. While pillar production with pulse durations in the range of 100 fs to 20 ns has been demonstrated, with much smaller pillars being formed in the case of femtosecond irradiation, pillars were not producible with a

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300 ns Nd:VO_4 laser. It appears that laser pulses significantly shorter than the melt lifetime of about 250 ns are required for sharp pillar formation.

[0075] FIG. 19(a) illustrates an SEM image of a one-dimensional periodic structure made on a silicon substrate, according to exemplary embodiments of the present invention. FIG. 19(b) illustrates an SEM image of a two-dimensional periodic structure made on a silicon substrate, according to exemplary embodiments of the present invention. Periodic structures can be produced by controlling the laser intensity distribution on the surface of the sample. The laser intensity distribution can be controlled by using interference and diffraction. For example, interference fringes are created by placing a metal wire in a portion of the laser beam. The light diffracted by the wire interferes to produce an intensity distribution on the sample surface that results in a periodic structure of pillars. Alternatively, the incident laser beam is split into two components, and then recombined at various angles to control the periodicity. It is also possible to place several pinholes in the path of the laser beam to create a periodic circular pattern of pillars on the surface. By using laser beams with different wavelengths and controlling the interference patterns, the periodicity of the pillars can be adjusted from tens of nanometers to tens of micrometers.

[0076] In an exemplary embodiment of the present invention, copper or tungsten wires with diameters from 100 to 250 μm are used to create interference fringes. The sample is exposed to 1.4 mJ pulses of light with a wavelength of 800 nm, a pulse duration of 130 fs, and a repetition rate of 1 kHz. The laser scan speed is 0.1 in/sec, and scanning is performed after placing the sample inside a vacuum chamber filled with SF_6 at a pressure of 400 mbar. In order to create a two-dimensional array of pillars, the metal wires are crossed orthogonally and placed in the path of the laser beam. Also, the spacing between adjacent pillars can be controlled by changing the wavelength of the laser pulses. For example, when the laser wavelength is decreased, the spacing between adjacent pillars also decreases.

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[0077] In another exemplary embodiment of the present invention, the laser texturing method was performed on various metallic surfaces. A metal is defined as an electrically conducting material. For example, titanium and stainless steel sheets are cut into small square-inch sized chips and cleaned with acetone and methanol. One such chip is put on a stage inside a vacuum chamber with a base pressure of around 1 mTorr, which is mounted on a high-precision computer-controlled X-Y stage. The chamber is rinsed and then backfilled with air at atmospheric pressure, SF_6 in a pressure range from 75 to 800 mbar, or helium in a pressure range from 75 to 800 mbar. The laser texturing method can also be conducted with a mixture of gases in different proportions and at different pressures, or in vacuum, with a chamber pressure of around 1 mbar. The samples are exposed to ultrafast laser pulses with a pulse energy of 0.95 mJ, a wavelength of 800 nm, a pulse width of 130 fs, and a repetition rate of 1 kHz from a regeneratively amplified Spectra-Physics Ti-sapphire laser system. Short laser pulse widths can also be used, including 1 fs to 1 μs pulses. Ultrafast laser pulses are a subcategory of short pulses, and can range from 1 femtosecond to hundreds of picoseconds. The laser beam is focused onto the sample surface by a coated lens with a focal length of 1 m, and the laser fluence is adjusted by using a Glan calcite polarizer.

[0078] The spatial profile of the laser pulse is Gaussian, and the fluence is calculated by using the laser spot size, which is determined by exposing a point on the sample surface to thousands of shots. In order to scan an area that is bigger than the laser spot size, the samples are translated using a motorized X-Y stage. Scanning also assists in making the surface structure more uniform by smoothing out any shot-to-shot irregularities in the beam profile. By varying the scanning speed of the X-Y stage, the number of laser pulses impinging on the sample surface at a particular spot is controlled. The spot size is about 0.3 mm.

[0079] Samples are produced with isolated single line scans, or with large areas created by overlapping several line scans. The step size between scan lines is chosen to be

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sufficiently small (less than 0.38 mm), so that successive lines overlap substantially. This further improves layer homogeneity. Homogeneity is further enhanced by performing two overlapping scans in orthogonal directions, rather than one overlapping scan with an exposure of the same total number of shots. After laser processing, the samples are analyzed with a scanning electron microscope (Zeiss SUPRA 40).

[0080] FIG. 20 shows SEM images of titanium surfaces treated with the laser texturing method for different background gas conditions. FIG. 20(a) shows an SEM image of a titanium surface treated in air, and FIG. 20(b) shows an SEM image of a titanium surface treated in vacuum. FIG. 20(c) shows an SEM image of a titanium surface treated in helium at a pressure less than 200 mbar, and FIG. 20(d) shows an SEM image of a titanium surface treated in SF_6 at a pressure greater than 400 mbar. As these figures show, pillar formation occurs in titanium that is treated with a laser fluence from 0.6 to 1.0 J/cm^2, and in vacuum or gas at low pressures less than 200 mbar. In order to create a well-developed pillar on titanium, it is necessary to irradiate the sample with around 1000 shots. However, increasing the number of shots or the laser fluence destroys the pillars.

[0081] FIG. 21 shows SEM images of stainless steel surfaces treated with the laser texturing method for different background gas conditions. FIG. 21(a) shows an SEM image of a stainless steel surface treated in air, and FIG. 21(b) shows an SEM image of a stainless steel surface treated in vacuum. FIG. 21(c) shows an SEM image of a stainless steel surface treated in helium at a pressure less than 200 mbar, and FIG. 21(d) shows an SEM image of a stainless steel surface treated in SF_6 at a pressure greater than 400 mbar. As shown in the figures, laser texturing forms pillars on stainless steel surfaces in air, vacuum, helium, and SF_6. However, in order to create a well-developed pillar on stainless steel, it is necessary to irradiate the sample with around 2000 shots. Both the stainless steel samples and the titanium

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samples turn pitch black after laser treatment. However, unlike titanium, pillar formation occurs on stainless steel in air.

[0082] FIG. 22 shows a series of SEM images viewed at 45° from the surface normal, which compares the results of the laser texturing method for various semiconductors and metals. In each case the surface of the material is treated with ultrafast laser pulses with a pulse width of 130 fs. FIG. 22(a) shows an SEM image of SiC treated with 260 shots at a laser fluence of around 1 J/cm^2 in 400 mbar of SF_6. FIG. 22(b) shows an SEM image of GaAs treated with 260 shots at a laser fluence of around 0.5 J/cm^2 in 400 mbar of SF_6. FIG. 22(c) shows an SEM image of titanium treated with 2000 shots at a laser fluence of around 0.3 J/cm^2 in 400 mbar of SF_6. FIG. 22(d) shows an SEM image of stainless steel treated with 2500 shots at a laser fluence of around 4.5 J/cm^2 in 400 mbar of SF_6. These figures show that the laser texturing method can form pillars on various semiconductors and metals.

[0083] In addition, the laser texturing method is likely to form pillars on ceramics, polymers, and alloys. By controlling the processing conditions of the laser texturing method for each material, the thermal, structural, optical, and electronic properties of the material can be tailored. Further, the formation of pillars can be controlled by changing the polarization state of the laser beam. A polarizer can change the output from the laser to be linearly, circularly, elliptically, or randomly polarized. The laser texturing method can be performed on surfaces of any geometrical shape, and is not limited to planar surfaces.

[0084] Similarly, the laser texturing method could also be used to process transparent materials, such as glass. The incident light could be absorbed by a two-photon process, or an appropriate wavelength could be selected for absorption by the transparent material. The altered surfaces formed by this method could be used in magnetic disk drives, because the disk drive and the head are spaced very closely together for data writing and reading.

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[0085] The altered surfaces formed by the apparatuses and methods of the present invention can have great utility in photovoltaic technologies, as schematically illustrated in FIG. 26. The increased light trapping and the control of photogenerated charges can provide improved efficiency. In particular, the altered surfaces would be beneficial in photodetectors, because the surfaces allow for the development of more sensitive detectors with a high responsivity, and extend the spectral range into the infrared region of the spectrum. This could also enable the building of infrared sensors for various applications.

[0086] The altered surfaces would also be beneficial in heat dissipation, as schematically illustrated in FIG. 27. A large surface area is created by texturing, which allows gas molecules to exchange energy with the surface, and increases heat dissipation. Such a high-efficiency heat sink could be very important for microelectronics, power electronics, optoelectronics, and other devices that require efficient heat dissipation.

[0087] The altered surfaces can also be used in field emission, as schematically illustrated in FIG. 23. Due to the sharp geometry of pillars formed by the laser texturing process, very high electric fields can be generated at relatively low voltages. These high electric fields can be used for electron emission from surfaces, providing an efficient source of electrons for various electronic and optoelectronic device applications, such as field emission displays, sensors, and instruments.

[0088] The altered surfaces would also be beneficial in surface property control, as schematically illustrated in FIG. 25. Laser textured surfaces can be made hydrophobic or hydrophilic by controlling the texture and surface coating. This can affect the air or fluid flow across the surface of the material.

[0089] The altered surfaces would also be beneficial in micro fluidic applications. There is an increasing number of micro fluidic applications for chemical and biomedical applications of chips. As schematically illustrated in FIG. 25, textured surfaces in micro

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channels can provide a good method of controlling the fluid flow, which can impact DNA sequencing and other applications. The altered surfaces would also be beneficial in turbulence control for aerodynamic applications. The flow of gases can be controlled by inserting a textured surface into the flow path. Also, turbulence can be generated by using of textured surfaces. This effect can be used in aerospace applications.

[0090] The altered surfaces would also be beneficial in an optical beam block, as schematically illustrated in FIG. 24. The laser textured surface has an extremely low reflectance and transmittance in the visible to the far infrared region, allowing the surface to be an efficient beam block for various optical and manufacturing applications. The altered surfaces would also be beneficial in controlling the visual appearance of products, including the surface color. The laser texturing process provides a completely black surface, hence it can be used to control the color of the surface without using any paints, dyes, or pigments.

[0091] The altered surfaces would also be beneficial in catalytic activity, as schematically illustrated in FIG. 29. The large surface area created by texturing provides many sites for enhanced chemical activity, such as catalytic activity. These catalytic activities would be useful in fuel cell technology, chemical plants, and biomedical applications, including conversion of carbon monoxide to carbon dioxide. The large surface area can also be used for enhanced tissue growth and control. The altered surfaces would also be beneficial in bond strength improvement. The large surface area created by texturing allows more sites for bonding and interlocking, and improves the overall bond strength.

[0092] The altered surfaces would also be beneficial in thin film or fibrous whisker growth. Due to the formation of nanospikes or microspikes, it is possible to utilize a large number of tips for growth of other materials atop these tips, as schematically illustrated in FIG. 29. Also, because a small voltage can provide a high electric field, the growth can be controlled by the electric field.

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[0093] The altered surfaces would also be beneficial in the production of nano or micro tips, as schematically illustrated in FIG. 29. Because the texturing process produces a large array of two-dimensional structures, micro or nano ordered tips can be fabricated. The nanospikes can be solid or hollow. These tips can be used in atomic force microscopy, optical data storage, and fluid control for automobiles and drug delivery.

[0094] The altered surfaces would also be beneficial in surface-enhanced Raman scattering. The Raman scattering method can be used to detect chemical or biochemical species. Usually Raman scattering signals are relatively low, but a Raman signal can be enhanced by many orders of magnitude by surface-enhanced Raman scattering. Laser textured surfaces coated with metals could provide an ideal template for surface-enhanced Raman scattering for sensor applications, such as single molecule detection. The altered surfaces would also be beneficial in biosensor applications. As schematically illustrated in FIG. 29, specific molecules can be attached atop the tips, and can be used for chemical or biochemical detection, by using methods such as fluorescence and phosphorescence.

[0095] The altered surfaces would also be beneficial in manufacturing optical elements. As schematically illustrated in FIGs. 24 and 28, various optical elements, such as diffraction gratings, low scattering surfaces, and antireflection surfaces can be prepared by texturing the optical element surface. Also, light absorption properties can be tailored by adjusting the laser parameters and thermal annealing conditions.

[0096] The altered surfaces would also be beneficial in photonic crystals. Photonic crystals are increasingly used for optoelectronic applications, such as wavelength selection and fabrication of negative refractive index materials. Periodic textured surfaces fabricated by laser texturing would be useful in these photonic crystals. The altered surfaces would also be beneficial in producing masters for replication. A textured surface can be used as template for transferring a pattern to a softer material by using mechanical pressure, with or without

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heat. This can provide a very low cost process for pattering surfaces such as compact discs. This process can also be used for transferring patterns to polymerics and biomaterials.

[0097] The altered surfaces would also be beneficial in fabricating mask-less periodic structures. By using an optical interference technique, periodic textured surfaces can be fabricated with a sub-micron period, without any mask fabrication. The altered surfaces would also be beneficial in pixelated devices. Some optoelectronic and microelectronic devices, such as CCD cameras, diode lasers, and light emitting diodes, require a two-dimensional geometry. Two-dimensional textured surfaces can be easily fabricated for optoelectronic and microelectronic applications. The altered surfaces would also be beneficial in producing substrates for single crystal film or nanoparticle growth.

[0098] The altered surfaces would also be beneficial in nano or micro pores. Textured surfaces can be further processed with chemical etching to provide a large number of nano or micro pores, which can be used for filtration or fluid flow control. Pores can be made by the laser texturing process if thin substrates are used, or if longer processing times are used. The altered surfaces would also be beneficial in controlling surface emissivity. By adjusting the surface texture, the surface emissivity and spectral properties can be controlled. This can provide camouflage objects, because such objects are harder to detect if they emit a low radiation signal.

[0099] The altered surfaces would also be beneficial in art and photography applications. As schematically illustrated in FIG. 28, laser texturing of surfaces can be used to write text and images on surfaces by controlling the light reflectivity of the surface. This technique can be used to produce name plates, part identification, hidden logos, trademarks, logos, and images. The texturing provides a black color, which produces a very high contrast between the written and unwritten areas. The process of the present invention can also be used to control the gray level in forming high definition images.

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[00100] The altered surfaces would also be beneficial in radiation shielding. Laser textured surfaces provide a very good method for controlling radiation scattering, reflection, absorption, and transmission over a broad spectral range, including visible, infrared, microwave, terahertz, and radio waves.

[00101] The altered surfaces would also be beneficial in plasma applications. Sharp tips can provide a very high electric field, and hence can be used for localized or large area generation of plasma sources. These plasma sources can be used to purify water, kill germs, and destroy bio-chemical agents.

[00102] The altered surfaces would also be beneficial in protecting substrates from corrosion, and improving adhesion, such as epoxy adhesion to a metal surface. They can also be used to improve the adhesion of thin films to a surface, such as a TiN coating on drill bits, which would extend the lifetime of the drill bits.

[00103] The altered surfaces would also be beneficial in bone grafting applications. Body implants can become detached from the host tissue, due to inadequate biocompatibility and poor osteointegration. Using laser texturing to change the surface chemistry and physical texture of the implants can improve the biocompatibility and adhesion.

[00104] The altered surfaces would also be beneficial in controlling the tribological properties of materials, such as friction, wear resistance, load-bearing properties, and lubrication. The textured surface can act as a micro-hydrodynamic bearing, a micro-reservoir for a lubricant, or a trap for debris particles generated during a sliding or other motion. This could result in significant friction reduction in piston rings. Similarly, laser texturing of cylinder liners in the interior of an engine compartment could reduce wear, friction, oil consumption, and gas emissions.

[00105] Instead of performing the laser texturing method in chemical gases, the method could be performed in the presence of gaseous plasma. Because charged species in gaseous

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plasma can be very reactive, laser irradiation in the presence of gaseous plasma will provide a much faster speed for texture formation, and further enable control of surface properties. Plasma sources can be created by various methods, such as excitation with a radio frequency (RF) source, direct current (DC), alternating current (AC), or a laser system. This approach provides a method for multi-energy processing technology, where electrical energy for plasma or discharge creation, laser irradiation for melting and ablation, and chemical energy by the gaseous environment are utilized to enhance the process and the control of the surface properties. Also, the sample can be kept at elevated temperatures, or the sample surface can be irradiated by an infrared lamp to raise the surface temperature, in order to enhance the chemical reactions or reduce the laser energy. In addition, plasma or ion etching methods are commonly used for semiconductor chip fabrication and preparation of samples for transmission electron microscopy. The addition of ultrafast pulsed laser energy could be used to further enhance this process.

[00106] Combining the laser texturing method with various other processes would also be beneficial. For example, a one-step process for doping, texturing, and crystallization would be advantageous from a manufacturing standpoint. Also, laser texturing and laser surface cleaning could be combined to provide a one-step process. In addition, laser texturing and surface passivation could be performed as a one-step process. The chemical gas used in laser texturing could provide the surface passivation by sulfur or phosphorous diffusion. Finally, laser texturing could be performed in a one-step process with surface hardening. For example, the surface of steel can be textured, and if a reactive gas such as ammonia or nitrogen plasma is used, surface nitridation can be achieved. This provides improved surface properties, such as wear, wetting characteristics, and chemical interactions.

[00107] The foregoing description and drawings should be considered as only illustrative of the principles of the present invention. The present invention may be configured and

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performed in a variety of ways, and is not intended to be limited by the exemplary embodiments discussed herein. Numerous applications of the present invention will readily occur to those skilled in the art who consider the foregoing description. Therefore, the present invention is not to be limited to the specific examples disclosed, or the construction and operation shown and described. Rather, all suitable modifications and equivalents are within the scope of the present invention, as defined in the appended claims.

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WHAT IS CLAIMED IS:

1. A method for texturing a surface of a semiconductor material, comprising:

providing an etching gas in an area around the surface of the material;

irradiating a portion of the surface with short laser pulses; and

translating at least one of the surface and a laser beam to allow the short laser pulses to irradiate another portion of the surface;

wherein the method produces a periodic array of pillars on the surface, resulting in changes in properties of the surface.

2. The method of claim 1, wherein the method additionally produces nanospikes atop the pillars.

3. The method of claim 2, further comprising sharpening the nanospikes by at least one of chemical etching and ion etching after irradiating the surface.

4. The method of claim 1, wherein the laser pulses have a duration of between one femtosecond and one microsecond.

5. The method of claim 4, wherein the laser pulses have a duration of between one femtosecond and hundreds of picoseconds.

6. The method of claim 1, wherein the laser pulses have a laser pulse energy density of between 0.1 J/cm^2 and 1.4 J/cm^2.

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7. The method of claim 1, wherein the laser pulses have a wavelength of between 200 and 1600 nm.

8. The method of claim 1, wherein irradiating the surface further comprises scanning the surface in a plurality of directions.

9. The method of claim 1, wherein irradiating the surface further comprises scanning the surface in a single direction a plurality of times.

10. The method of claim 1, further comprising controlling a surface texture by controlling a polarization state of the laser pulses.

11. The method of claim 1, further comprising controlling an electrical conductivity of the material by controlling texturing parameters.

12. The method of claim 1, wherein irradiating the surface comprises at least partially crystallizing the irradiated surface.

13. The method of claim 1, further comprising controlling a spacing between adjacent pillars by controlling a wavelength of the laser pulses, a laser pulse energy density, and a number of laser pulses.

14. The method of claim 1, wherein the etching gas comprises at least one of sulfur hexafluoride gas, hydrogen chloride gas, helium gas, and argon gas.

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15. The method of claim 1, wherein the etching gas has a pressure of no more than 0.1 atmospheres.

16. The method of claim 1, wherein the etching gas comprises a gaseous plasma.

17. A method for texturing a surface of a semiconductor material, comprising:

providing an etching gas in an area around the surface of the material;

irradiating a portion of the surface with short laser pulses while simultaneously crystallizing the portion of the surface; and

translating at least one of the surface and a laser beam to allow the short laser pulses to irradiate another portion of the surface while simultaneously crystallizing the other portion of the surface;

wherein the method produces pillars on the surface, resulting in changes in properties of the surface.

18. A method for texturing a metallic surface, comprising:

irradiating a portion of the metallic surface with short laser pulses; and

translating at least one of the surface and a laser beam to allow the short laser pulses to irradiate another portion of the surface;

wherein the method produces pillars on the surface, resulting in changes in properties of the surface.

19. The method of claim 18, wherein the pillars are produced in a periodic array.

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20. The method of claim 18, further comprising providing an etching gas in an area around the surface.

21. The method of claim 20, wherein the etching gas comprises at least one of sulfur hexafluoride gas, hydrogen chloride gas, helium gas, and argon gas.

22. The method of claim 20, wherein the etching gas has a pressure of no more than 0.1 atmospheres.

23. The method of claim 20, wherein the etching gas comprises a gaseous plasma.

24. The method of claim 18, wherein the surface is in air at atmospheric pressure.

25. The method of claim 18, wherein the laser pulses have a duration of between one femtosecond and one microsecond.

26. The method of claim 25, wherein the laser pulses have a duration of between one femtosecond and hundreds of picoseconds.

27. The method of claim 18, wherein the laser pulses have a laser pulse energy density of between 0.1 J/cm^2 and 1.4 J/cm^2.

28. The method of claim 18, wherein the laser pulses have a wavelength of between 200 and 1600 nm.

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29. The method of claim 18, wherein irradiating the surface further comprises scanning the surface in a plurality of directions.

30. The method of claim 18, further comprising controlling a surface texture by controlling a polarization state of the laser pulses.

31. The method of claim 18, further comprising controlling an electrical conductivity of the material by controlling texturing parameters.

32. A semiconductor surface, comprising a portion on which pillars are formed with nanospikes atop the pillars by irradiating the surface with short laser pulses while a substantially pure sulfur hexafluoride gas is provided around the surface.

33. A metallic surface, comprising a portion on which pillars are formed by irradiating the surface with short laser pulses.

34. A method of using the textured surface of claim 1 to provide a photovoltaic device.

35. A method of using the textured surface of claim 1 to provide a photodetector.

36. A method of using the textured surface of claim 1 or 18 to provide a high-efficiency heat sink for an electronic device.

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37. A method of using the textured surface of claim 1 or 18 to provide a very high electric field for electron emission.

38. A method of using the textured surface of claim 1 or 18 to generate catalytic activity.

39. A method of using the textured surface of claim 1 or 18 to perform osteointegration of a body implant.

40. A method of using the textured surface of claim 1 or 18 to control the flow of air or fluid over the surface.

41. A method of using the textured surface of claim 1 or 18 to create a two-dimensional array of micro or nano dimensioned ordered tips.

42. A method of using the textured surface of claim 1 or 18 to manufacture an optical beam block which absorbs substantially all light from the visible to the far-infrared.

43. A method of using the textured surface of claim 1 or 18 in micro fluidic applications.

44. The method of claim 1 or 18, further comprising controlling a color of the surface.

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45. A method of using the textured surface of claim 1 or 18 to produce a master for replication.

46. The method of claim 1 or 18, further comprising processing the surface with chemical etching to provide nano or micro pores on the surface.

47. The method of claim 1 or 18, further comprising controlling an emissivity of the surface.

48. The method of claim 1 or 18, further comprising writing text or images on the surface by controlling a light reflectivity.

49. A method of using the textured surface of claim 1 or 18 to provide a radiation shield which operates in a broad spectral range.

50. A method of using the textured surface of claim 1 or 18 to provide an infrared sensor.

51. A method of using the textured surface of claim 18 to prevent corrosion and provide adhesion.

52. The method of claim 1, wherein the changed properties are at least one of optical properties, thermal properties, and electrical properties.

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53. The method of claim 18, wherein the changed properties are at least one of optical properties, thermal properties, and electrical properties.

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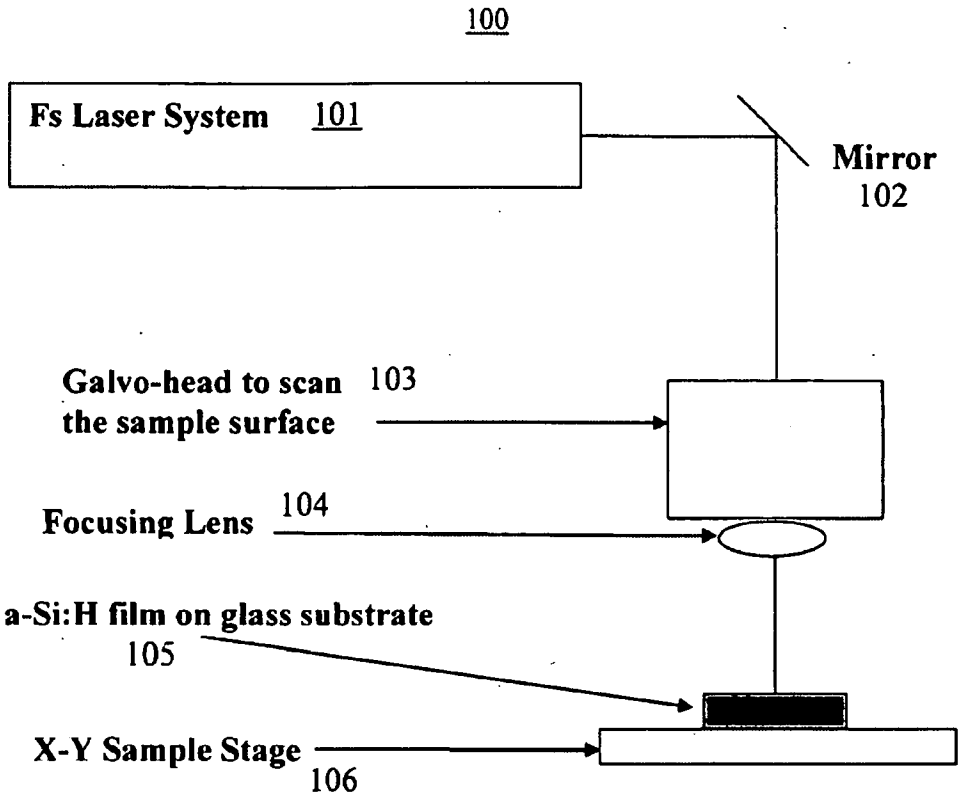


FIG. 1

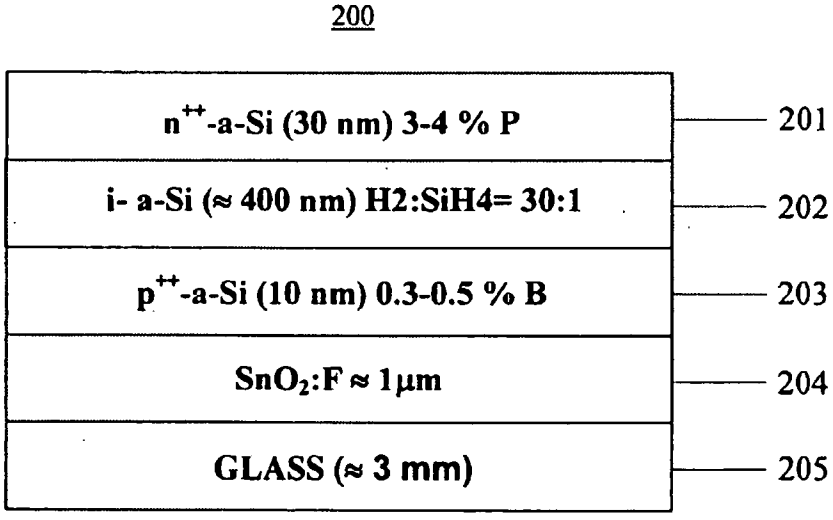


FIG. 2

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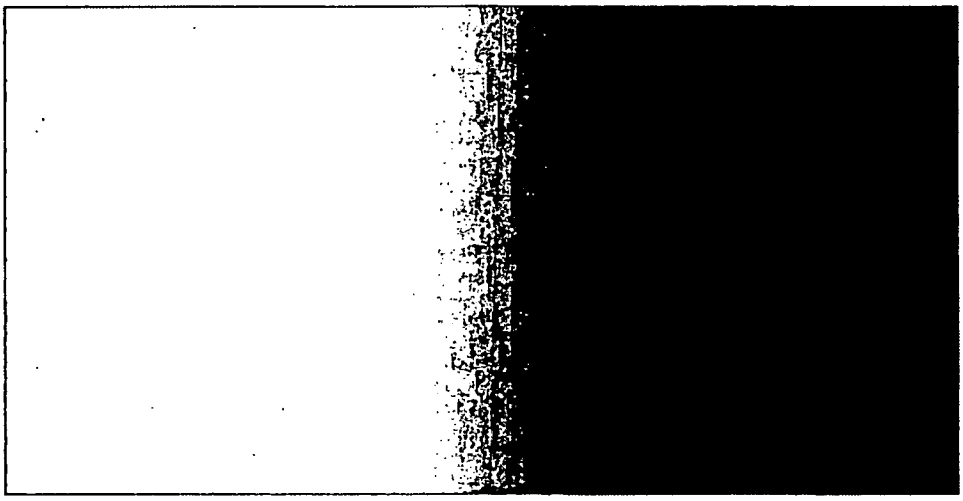
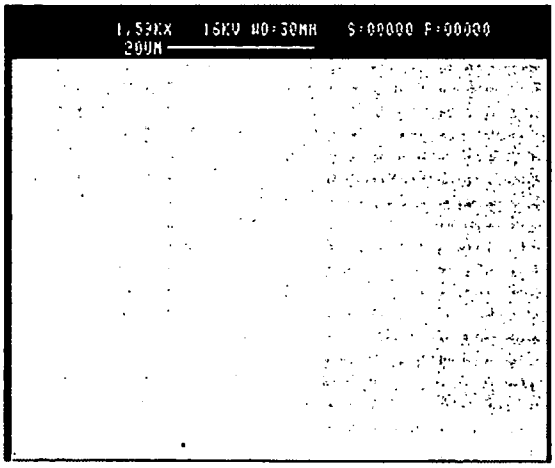


FIG. 3(a) FIG. 3(b)



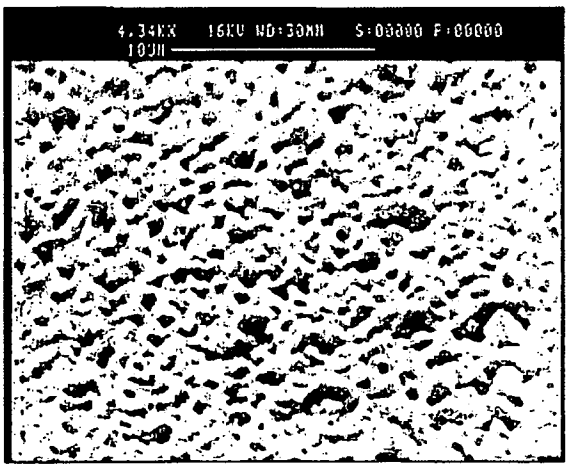


FIG. 4(a) FIG. 4(b)

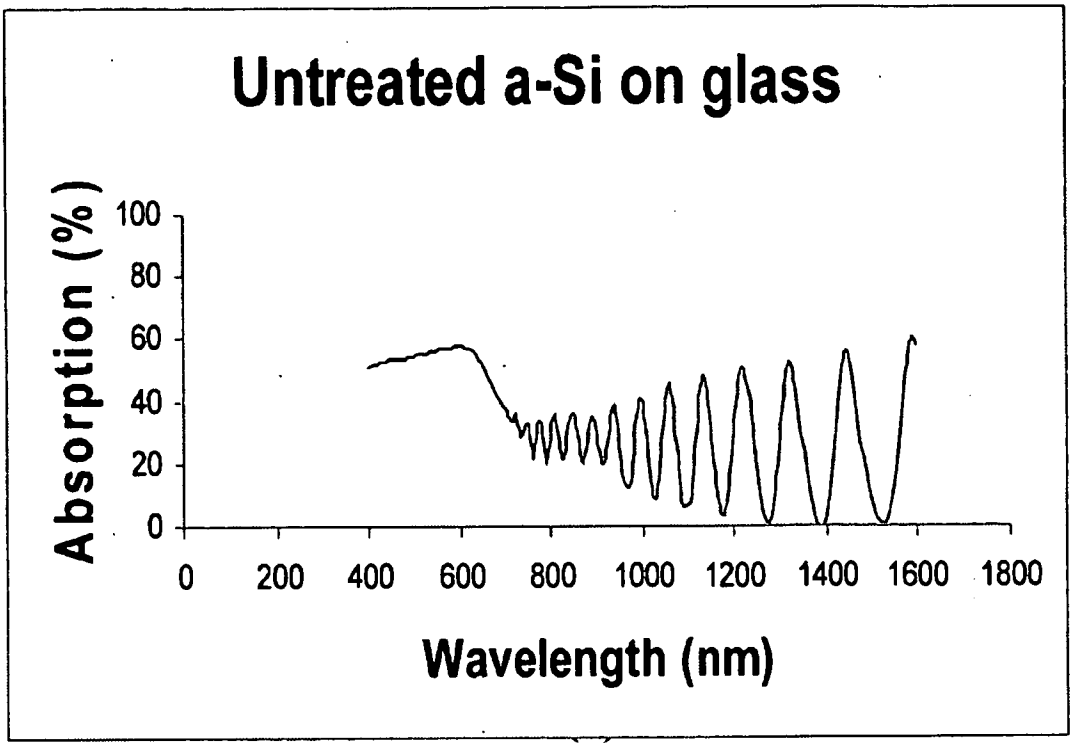


FIG. 5(a)

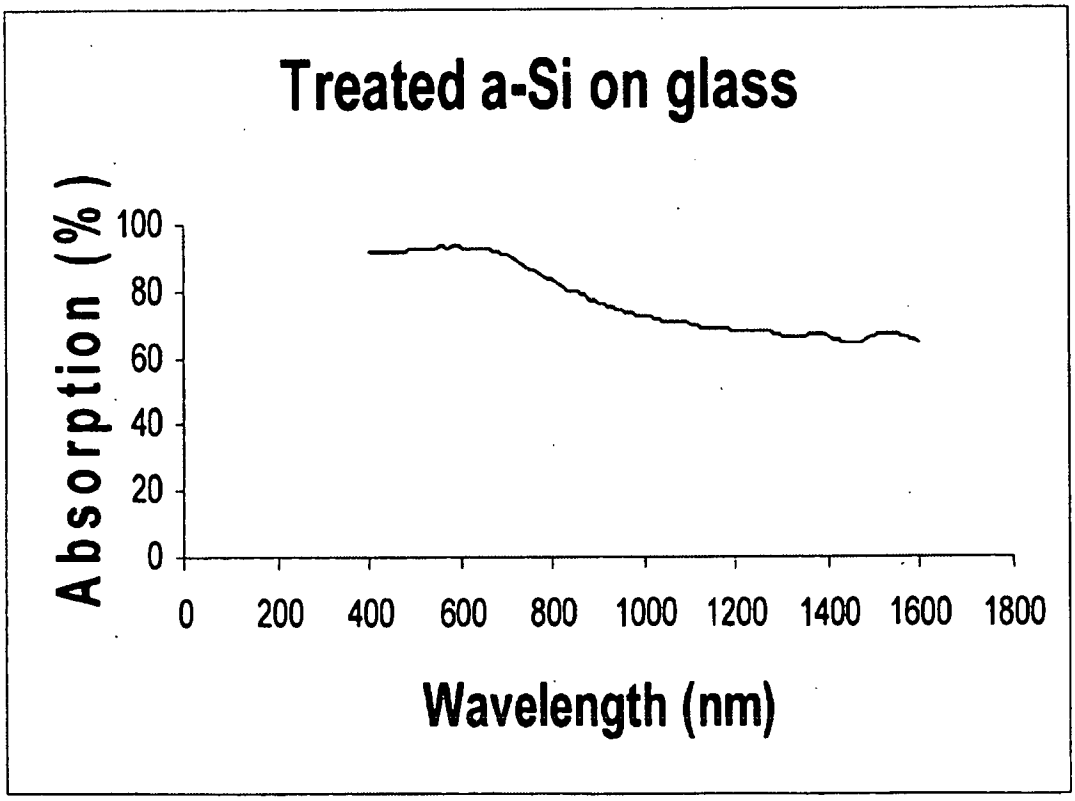


FIG. 5(b)

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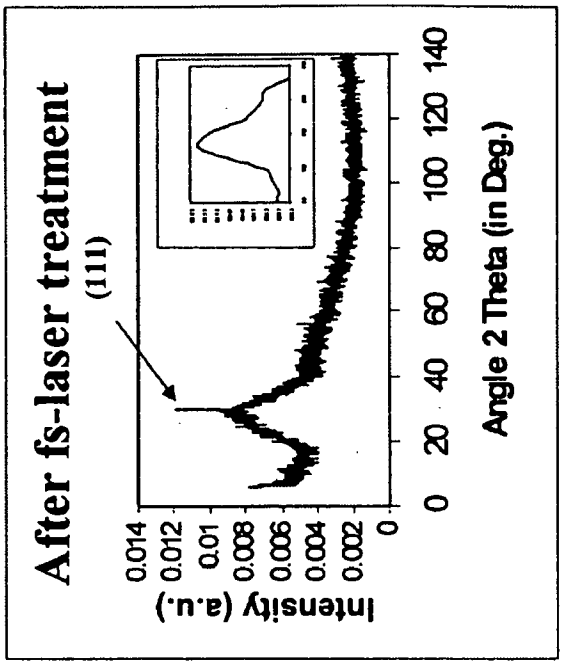


FIG. 6(b)

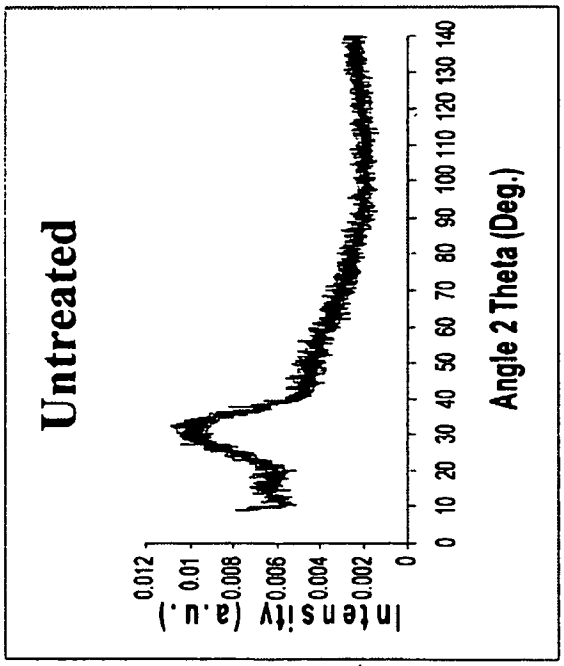


FIG. 6(a)

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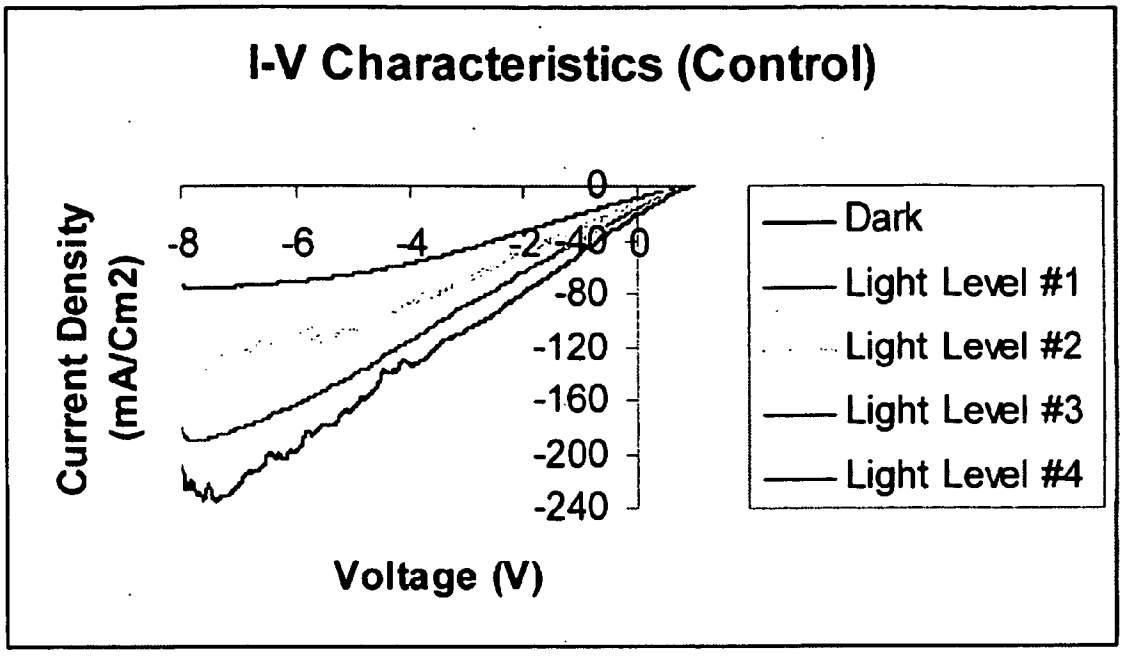

I-V Characteristics (Control)
Current Density (mA/Cm2)
0
-8
-6
-4
-2
-40
0
-80
-120
-160
-200
-240
Voltage (V)
Dark
Light Level #1
Light Level #2
Light Level #3
Light Level #4

FIG. 7(a)

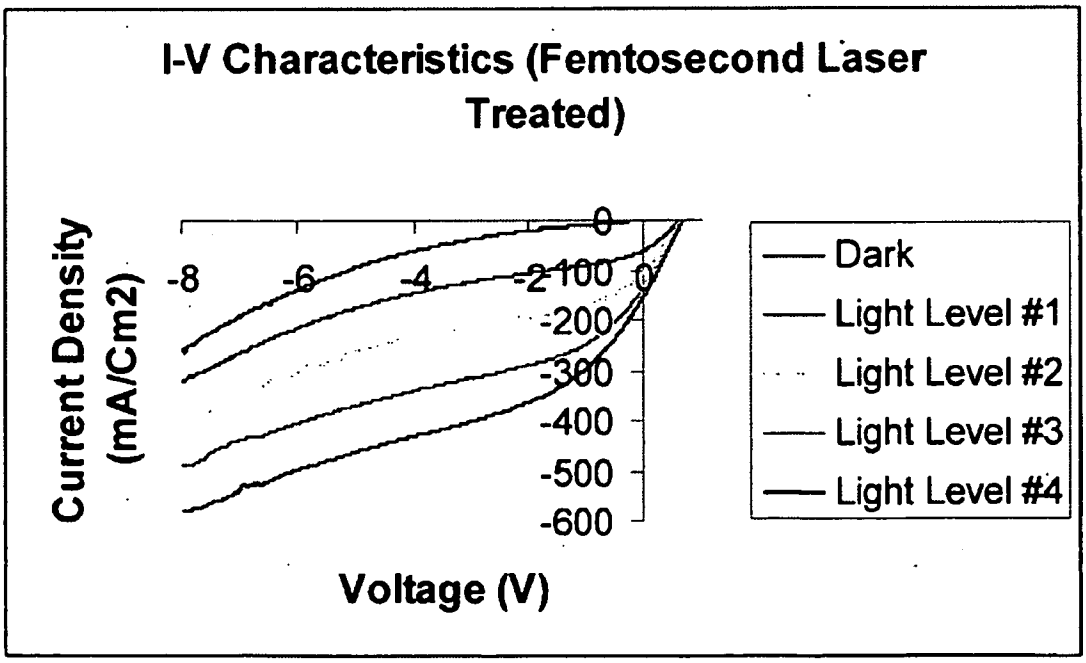

I-V Characteristics (Femtosecond Laser Treated)
Current Density (mA/Cm2)
0
-8
-6
-4
-2
-100
0
-200
-300
-400
-500
-600
Voltage (V)
Dark
Light Level #1
Light Level #2
Light Level #3
Light Level #4

FIG. 7(b)

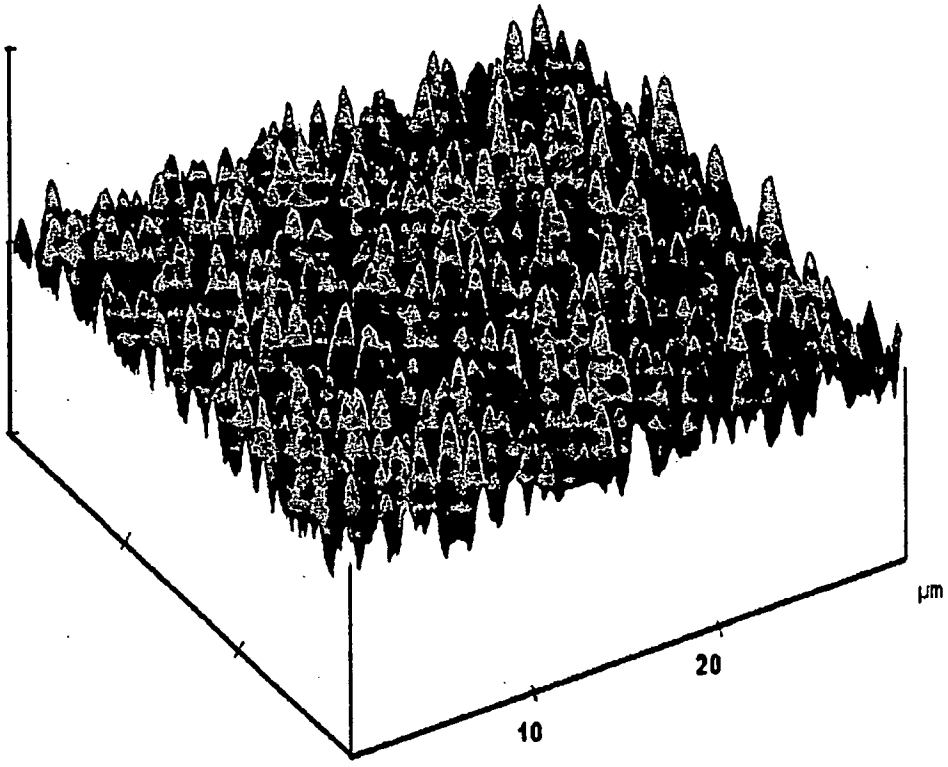

μm
20
10

FIG. 8

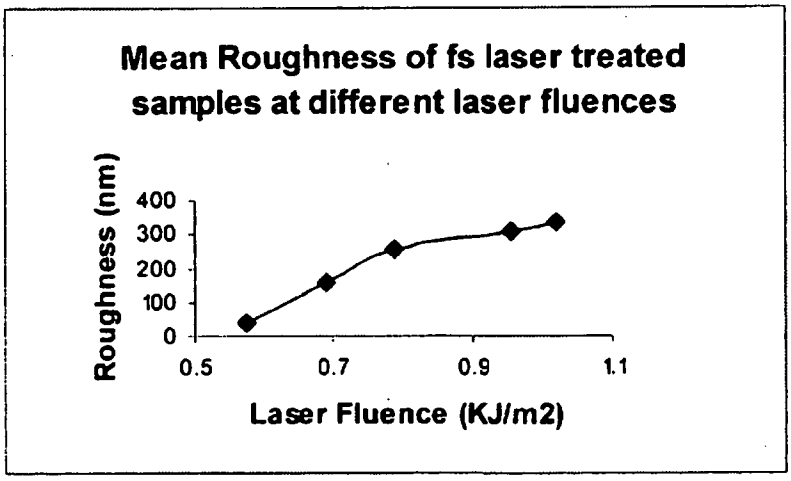

Mean Roughness of fs laser treated samples at different laser fluences
Roughness (nm)
400
300
200
100
0
0.5
0.7
0.9
1.1
Laser Fluence (KJ/m2)

FIG. 9

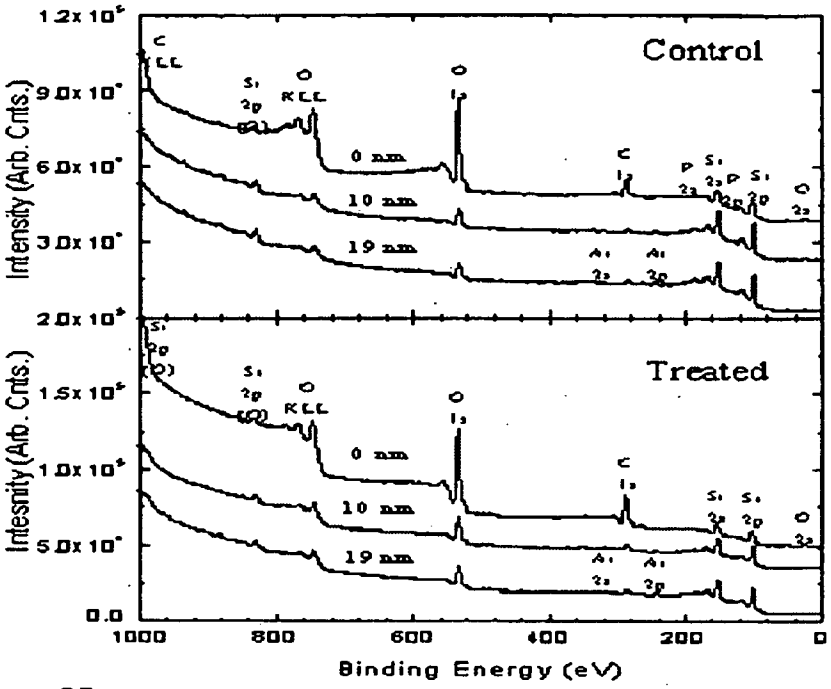


FIG. 10(a)

FIG. 10(b)

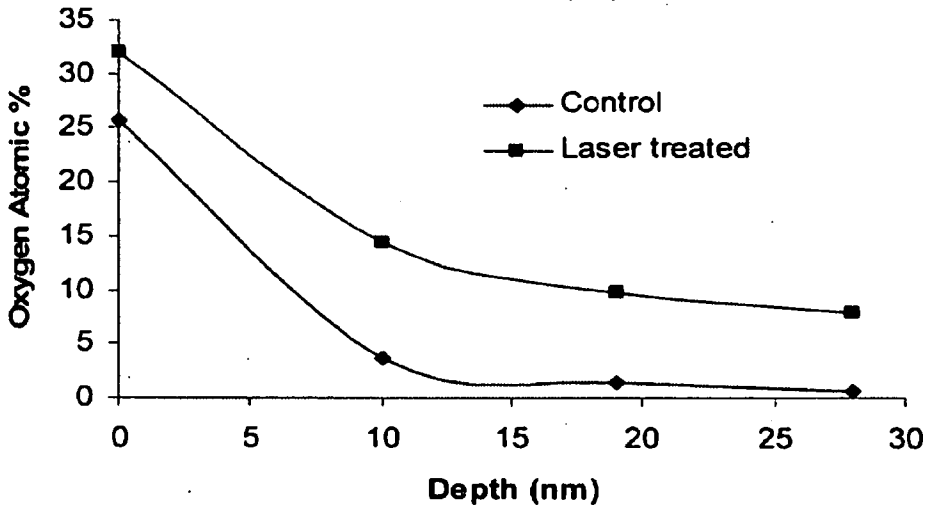


FIG. 10(c)

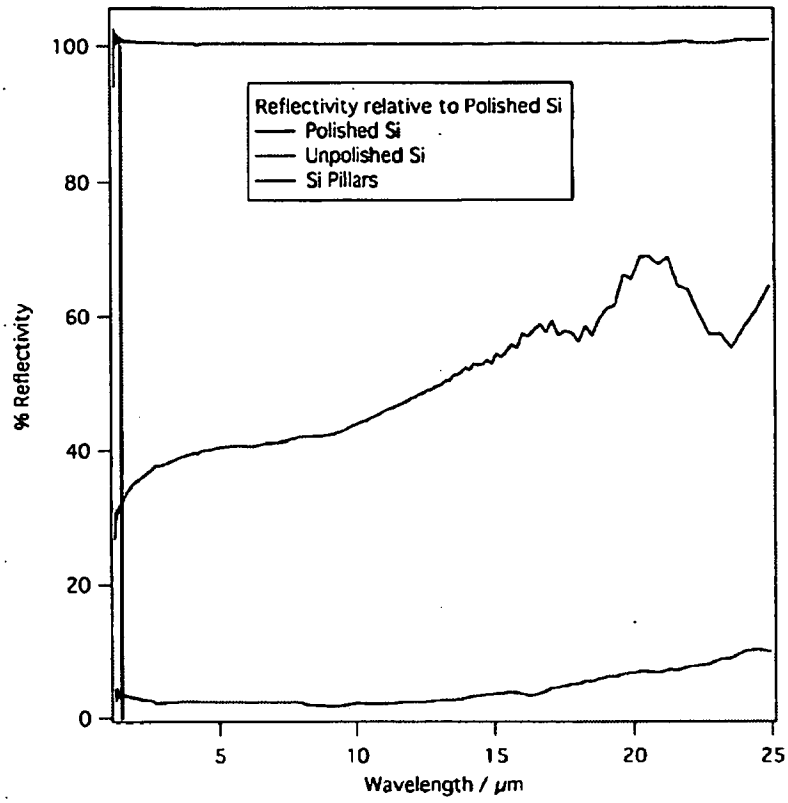


FIG. 11

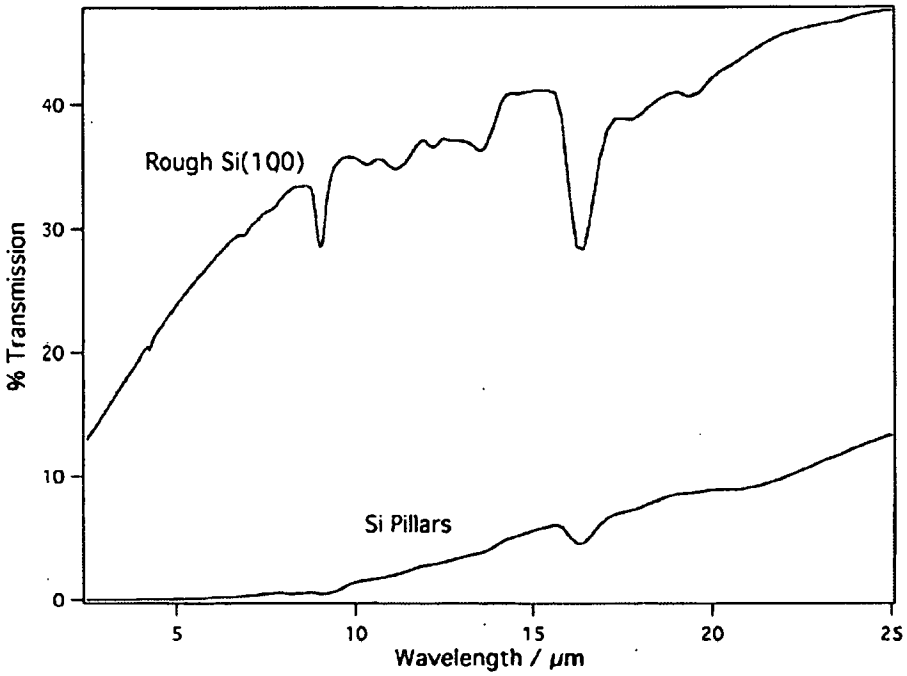


FIG. 12

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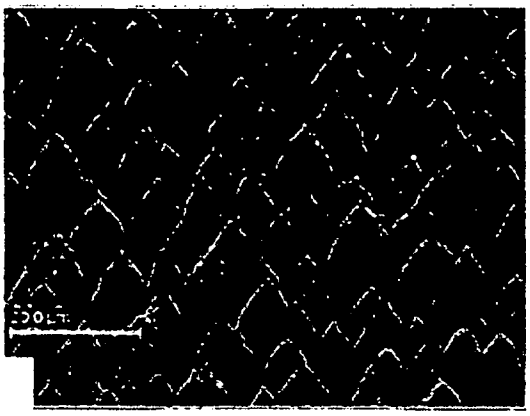


FIG. 13(a)

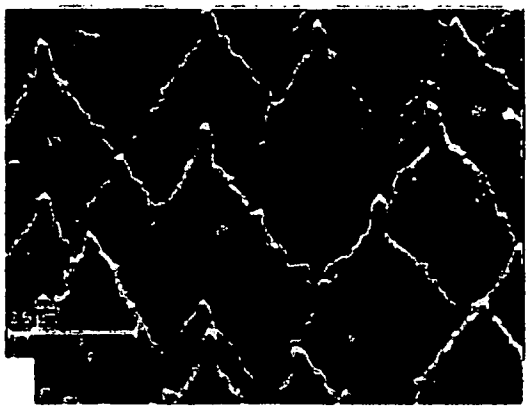


FIG. 13(b)

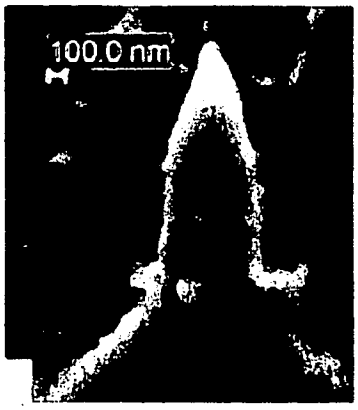


FIG. 13(c)

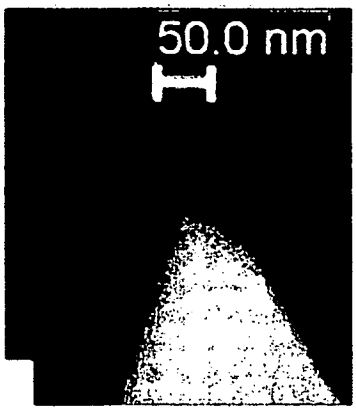


FIG. 13(d)

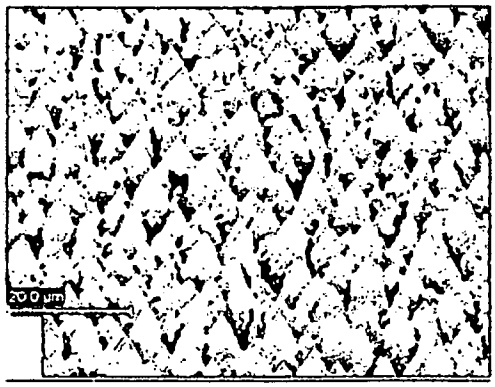


FIG. 14(a)

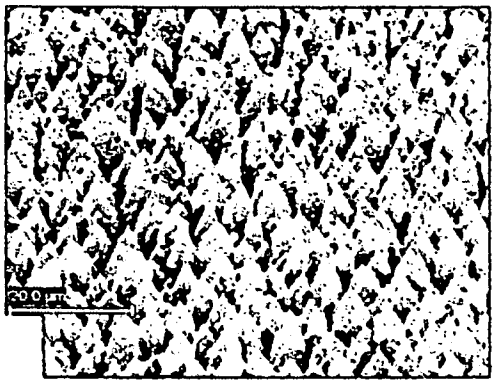


FIG. 14(b)

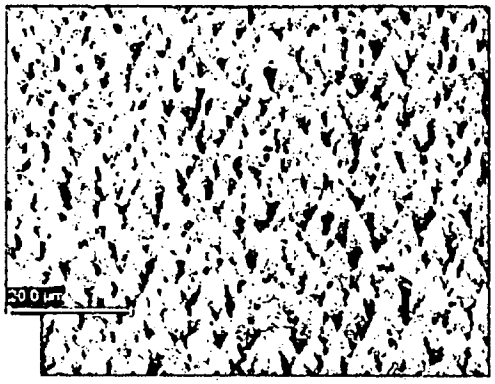


FIG. 14(c)

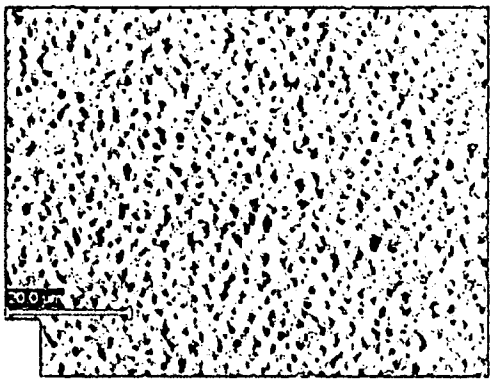


FIG. 14(d)

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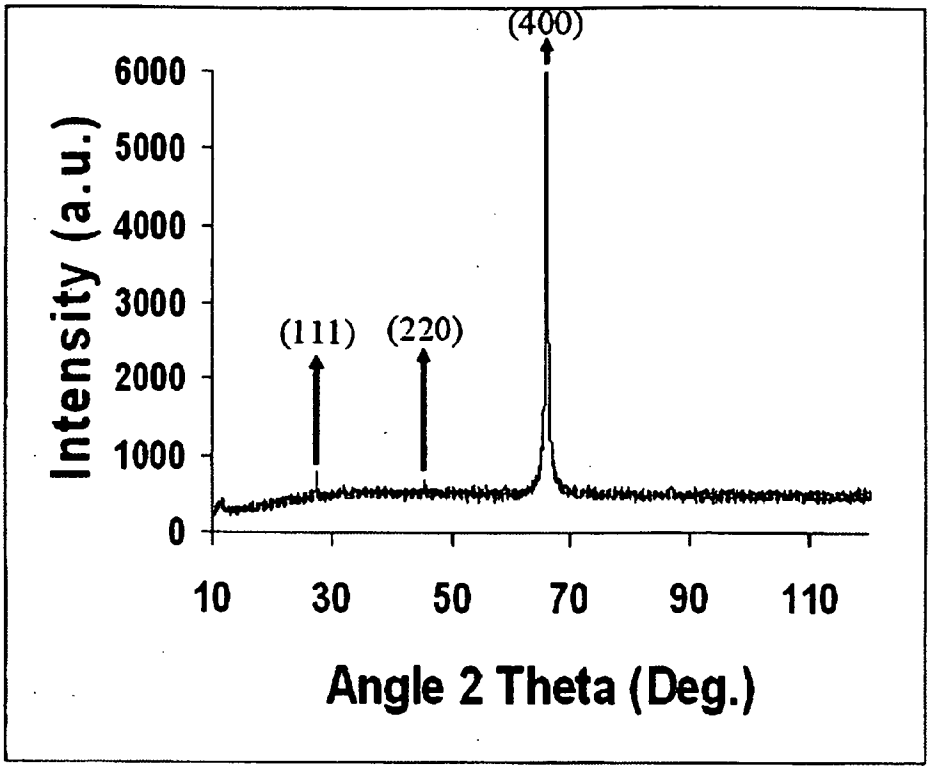


FIG. 15

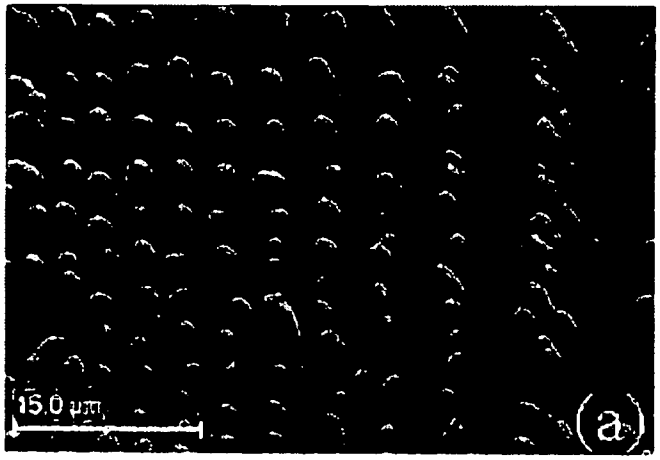


FIG. 19(a)

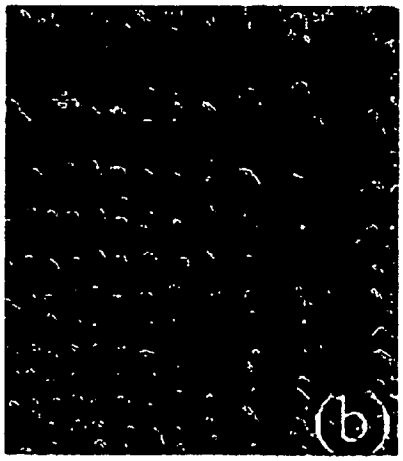


FIG. 19(b)

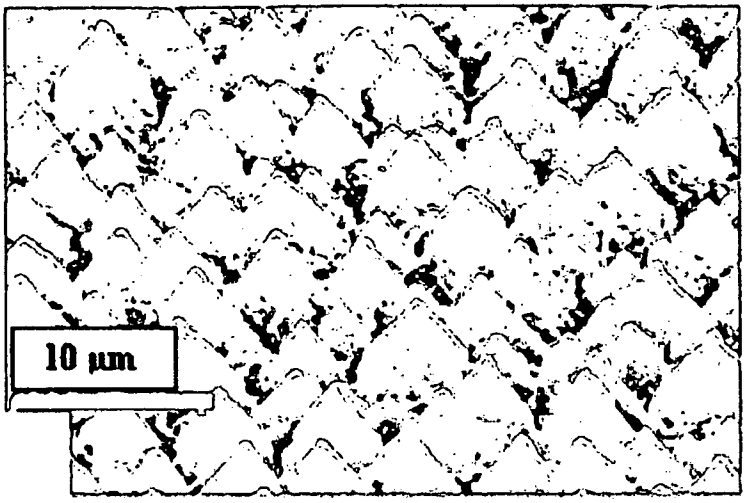


FIG. 16(a)

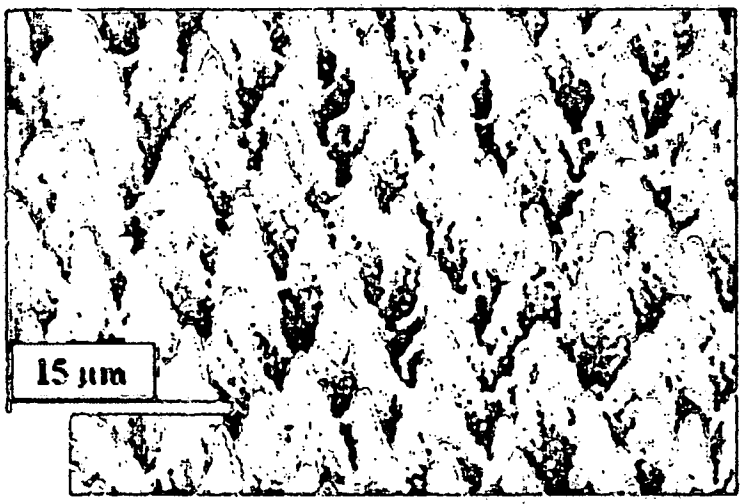


FIG. 16(b)

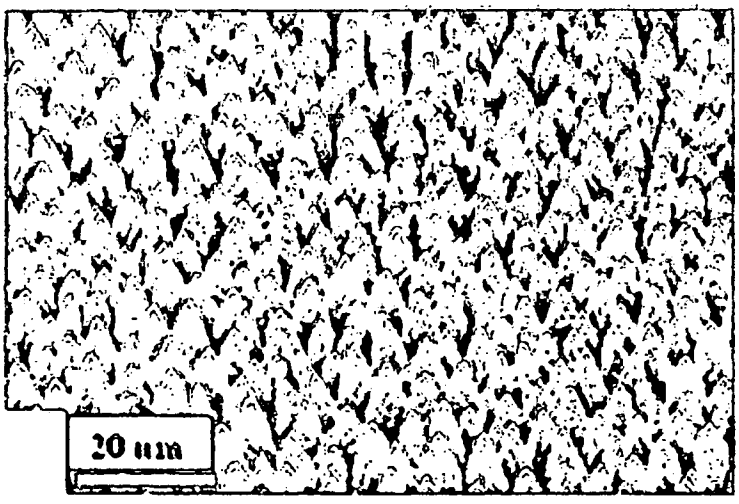


FIG. 16(c)

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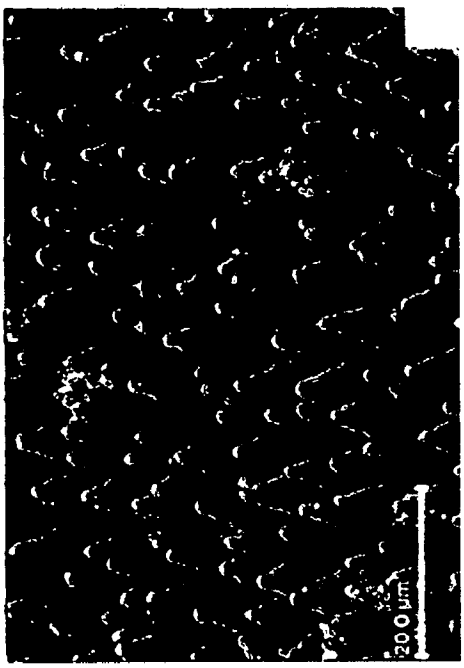


FIG. 17(b)

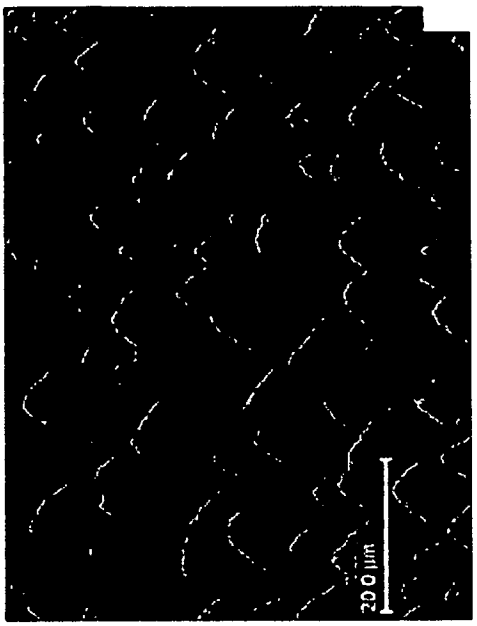


FIG. 18(b)



FIG. 17(a)

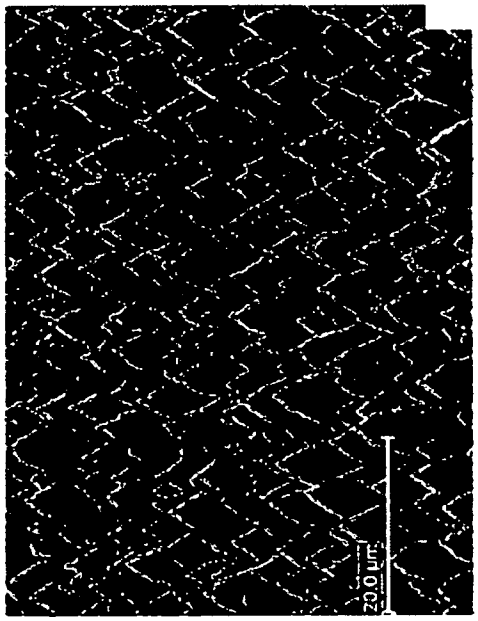


FIG. 18(a)

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FIG. 20(a)

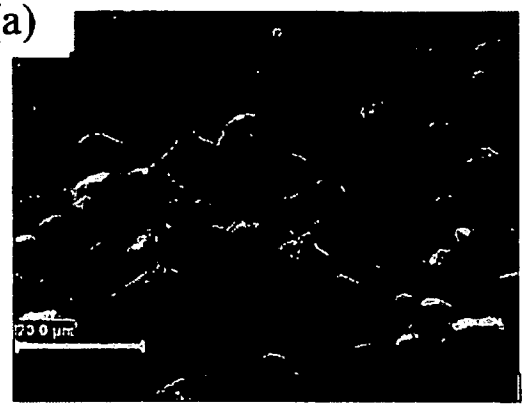


FIG. 20(b)

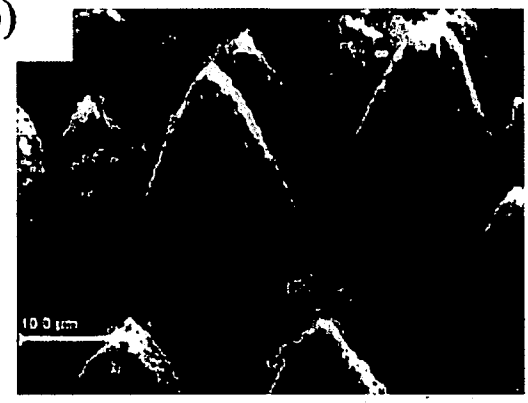


FIG. 20(c)

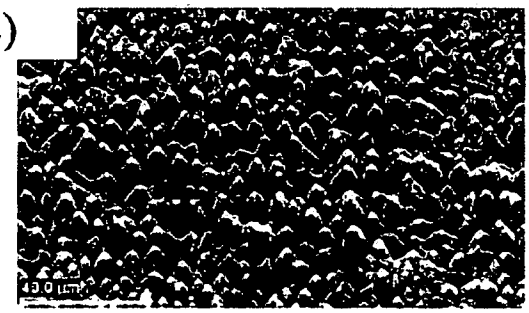


FIG. 20(d)

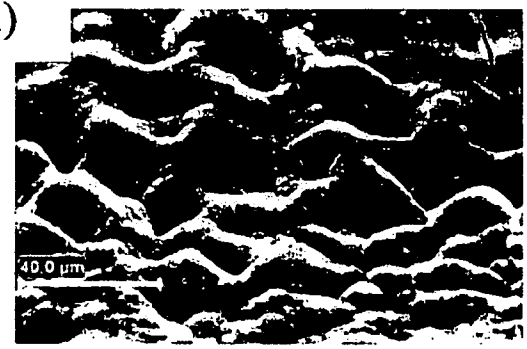


FIG. 21(a)



FIG. 21(b)

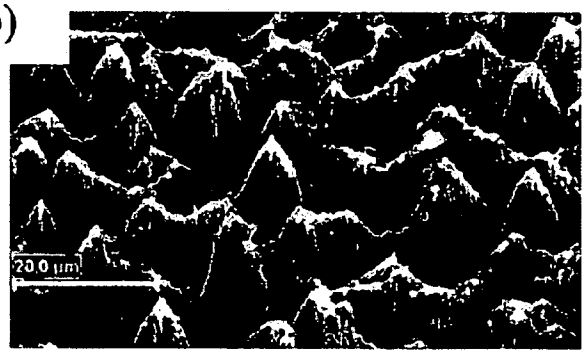
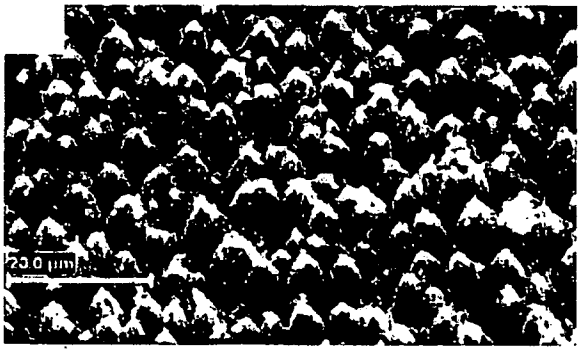


FIG. 21(c)



FIG. 21(d)



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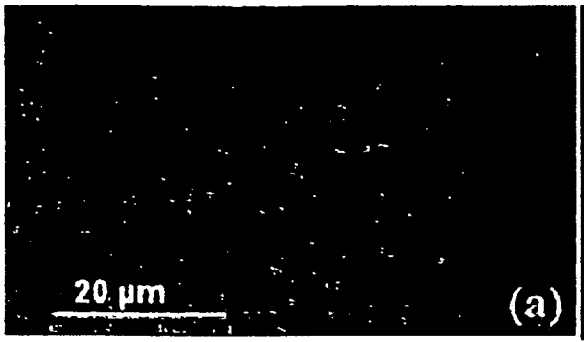


FIG. 22(a)

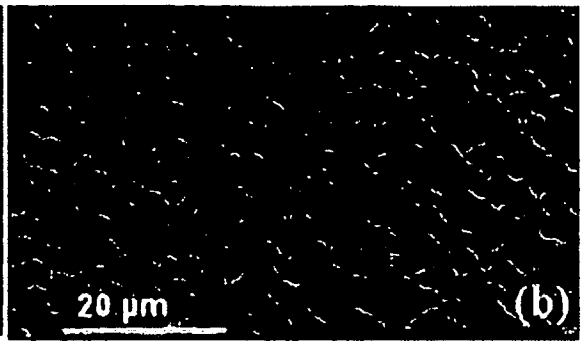


FIG. 22(b)

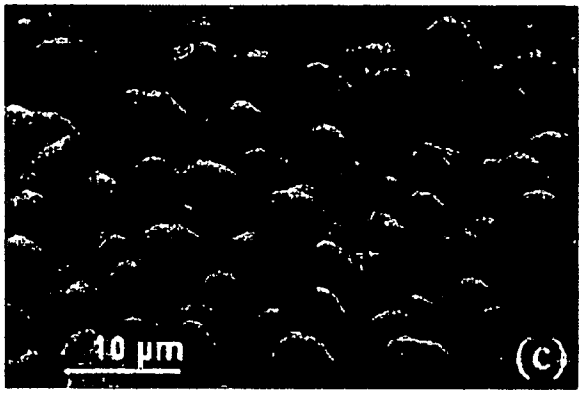


FIG. 22(c)



FIG. 22(d)

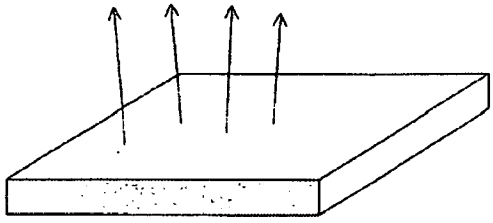


FIG. 23

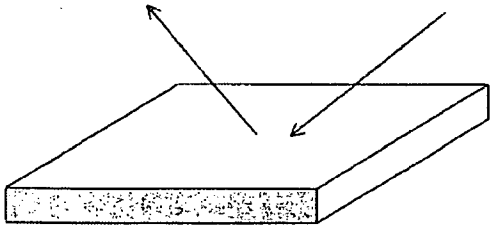


FIG. 24

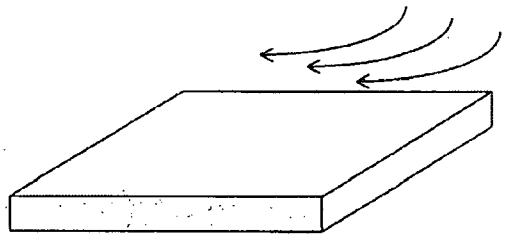


FIG. 25

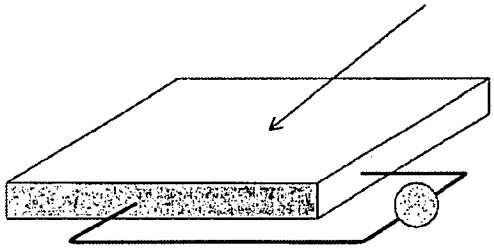


FIG. 26

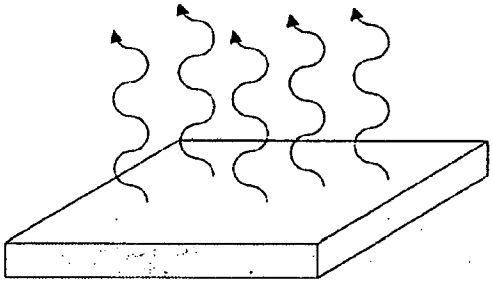


FIG. 27

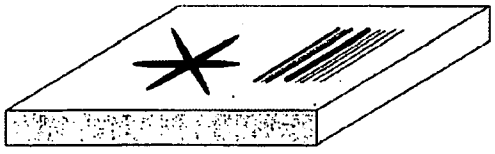


FIG. 28

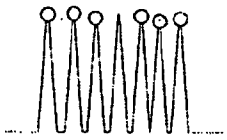


FIG. 29

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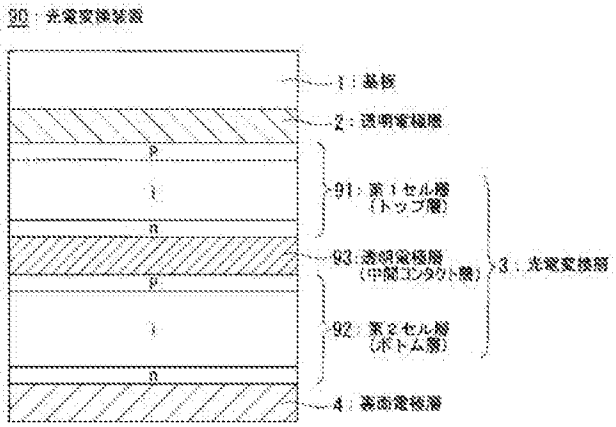
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[続葉有]

(54) Title: PHOTOELECTRIC CONVERTER AND METHOD FOR FABRICATING THE SAME

(54) 発明の名称: 光電変換装置及びその製造方法



90 PHOTOELECTRIC CONVERTER
1 SUBSTRATE
2 TRANSPARENT ELECTRODE LAYER
3 PHOTOELECTRIC CONVERSION LAYER
91 FIRST CELL LAYER (TOP LAYER)
92 SECOND CELL LAYER (BOTTOM LAYER)
93 TRANSPARENT ELECTRODE LAYER (INTERMEDIATE CONTACT LAYER)
4 BACKSIDE ELECTRODE LAYER

(57) **Abstract:** A photoelectric converter satisfying both high photoelectric conversion efficiency and high productivity, and its fabrication method. The photoelectric converter (90) has a substrate with a transparent electrode where a transparent electrode layer (2) is provided on a transparent insulating substrate (1), and at least a photoelectric conversion layer (92) principally comprising a crystalline silicon based semiconductor and a backside electrode layer (4) that are formed sequentially on the transparent electrode layer (2) side of the substrate with a transparent electrode. The transparent electrode layer (2) on the substrate with a transparent electrode has a surface shape where large and small protrusions and recesses coexist and spectral haze rate is 20% or above at the wavelength of 550-800 nm. The photoelectric conversion layer principally comprising the crystalline silicon based semiconductor has a film thickness of 1.2-2 μm, and a Raman ratio of 3.0-8.0.

(57) 要約: 高い光電変換効率と高い生産性を両立した光電変換装置及びその製造方法を提供することを目的とする。透明絶縁性の基板１上に透明電極層２を設けてなる透明電極付き基板と、該透明電極付き基板の透明電極層２側に順次形成された、結晶質シリコン系半導体を主として有する光電変換層９２ならびに裏面電極層４とを少なくとも有してなる光電変換装置であって、前記透明電極付き基板の透明電極層２表面が、大小の凹凸が混在した形状であり、かつ分光ヘイズ率が５５０ｎｍ以上８００ｎｍ以下の波長で２０％以上であり、前記結晶質シリコン系半導体を主として有する光電変換層の膜厚が１．２μｍ以上２μｍ以下、かつラマン比が３．０以上８．０以下である光電変換装置９０を提供する。

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(81) 指定国 (表示のない限り、全ての種類の国内保護が可能): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) 指定国 (表示のない限り、全ての種類の広域保護が可能): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), ユーラシア (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), ヨーロッパ (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

添付公開書類:
— 国際調査報告書

明 細 書

光電変換装置及びその製造方法

技術分野

[0001] 本発明は、光電変換装置及びその製造方法に関し、特に発電層としてシリコンを用いる薄膜シリコン積層型太陽電池に関するものである。

背景技術

[0002] 従来より、太陽電池等の光電変換装置として、シリコン系薄膜光電変換装置が知られている。この光電変換装置は、一般に、基板上に、第1透明電極、シリコン系半導体層(光電変換層)、第2透明電極及び裏面電極膜を順次積層したものである。半導体層はp型、i型及びn型の半導体材料によって形成されるpin接合を有している。光電変換装置が太陽電池である場合においてはこのpin接合がエネルギー変換部となって、太陽光の光エネルギーを電気エネルギーに変換する。このように、光電変換層が1層の光電変換装置の構造は、シングル構造と呼ばれている。

[0003] また、光電変換装置の光電変換効率を高めるために、バンドギャップの異なる半導体からなる光電変換層を複数重ねて用いる方法がある。このように複数の光電変換層を重ねて用いた光電変換装置は多接合型光電変換装置と呼ばれ、吸収波長帯域が異なる光電変換層を2段重ねた構造はタンデム構造、3段重ねた構造はトリプル構造と呼ばれている。タンデム構造の光電変換装置を例にとると、太陽光入射側の光電変換層(以下、「トップセル」ともいう)としては短波長の光を吸収するアモルファス(非晶質)シリコンが用いられ、また、トップセルで吸収されなかった光を吸収するために、太陽光入射側とは反対側の光電変換層(以下、「ボトムセル」ともいう))としては長波長の光を吸収する微結晶シリコン等の結晶質シリコン系半導体を用いることができる。

[0004] このような光電変換装置を用いた太陽電池には、次のような技術課題(1)が存在する。

(1)高効率化:太陽光をエネルギー変換部にいかに効率よく取り込み、電気エネルギーに変換する効率をいかに高めるか。

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[0005] 上記技術課題(1)の高効率化としては、12%以上の発電効率を得ることが目安となるが、従来、例えばタンデム型太陽電池において12%以上の発電効率を得るためには、2μm以上のボトムセル膜厚が必要であった。更に発電効率を上げるためには、ボトムセルの厚膜化(3μm以上)が検討されている。

[0006] また、上記技術課題(1)の高効率化を実現するために、第1透明電極を含めた基板のヘイズ率を高めることが検討されている。従来は、第1透明電極を含めた基板のヘイズ率を大きくすると、入射光の光散乱による光閉じ込め効果が向上して発電電流は増大するが、第1透明電極を含めた基板表面の大きな凹凸の影響などで開放電圧と形状因子が大幅に低下するので、電池としては好ましくないと、一般的に考えられていた。これを解決するために、前記基板及び第1透明電極として、ガラス基板上に、不連続な複数の山部によるマクロな凹凸(テクスチャ)と、この山部間をうめる複数の平坦部とを有しており、該山部及び該平坦部の外表面が、ミクロの多数の凹凸(テクスチャ)を有する構造(ダブルテクスチャ構造)となっている透明導電性酸化物付き基体を用いることが提案されている(特許文献1、特許文献2参照)。特許文献1及び2の透明導電性酸化物付き基体は、太陽光の全波長域で良好な光散乱性能有するものであり、特許文献2には、これを用いて作製されたアモルファスシリコン太陽電池が、その実施例において、開放電圧と形状因子をほぼ維持しつつ光電変換効率が高められることが示されている。

特許文献1:国際公開第03/036657A1号公報

特許文献2:特開2005-347490号公報

発明の開示

[0007] 光電変換装置を用いた太陽電池を実用化するためには、前記技術課題(1)に加え、下記技術課題(2)も存在する。

(2)生産性向上:生産性のボトルネックとなる結晶質シリコン系光電変換層中のi層をいかに薄膜化できるか。

[0008] 太陽電池の製造時間は、ボトムセル等を構成する結晶質シリコン系光電変換層中のi層の製膜時間に律速するため、上記技術課題(2)の生産性の点からは、結晶質シリコン系光電変換層中のi層の膜厚の薄膜化が極めて有効である。ところが、例え

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ばタンデム型太陽電池においてボトムセルの膜厚を2μmより薄膜化すると、発電電流の低下が著しく、よって発電効率の低下が著しくなる。このため、太陽電池の製造時間が長時間かかっても、2μm以上のボトムセル膜厚が適用されている。

このように、前記技術課題(1)と(2)とは、互いにトレードオフの関係にあった。

[0009] 前記特許文献1に示された技術は、光の吸収波長特性が異なる結晶質シリコン系半導体からなる光電変換層の発電効率を特に考慮したものではなく、また、太陽電池の生産性向上について検討されたものでもなかった。従って、結晶質シリコン系半導体からなる光電変換層を有する太陽電池については、入射光の吸収波長域が特に長波長側で異なるため、透明電極の凹凸による光閉じ込め形状は違うものが必要となるが、結晶質シリコン系半導体の膜厚を薄膜化することを考慮して凹凸形状を適正化することが未確立であり、発電効率の高効率化(技術課題(1)の解決)と太陽電池の生産性向上(技術課題(2)の解決)を両立できる技術が依然として望まれていた。

[0010] また、特許文献1のように大きな凹凸と小さな凹凸の混在する透明導電性酸化膜付き基板を用いて太陽電池を作製すると、大きな凹凸構造のみで構成してヘイズ率を高めた透明導電性酸化物付き基板を用いる場合よりも開放電圧と形状因子の低下を小さくすることはできるものの、やはり開放電圧と形状因子の低下が認められる。

[0011] 本発明は、このような事情に鑑みてなされたものであって、高い光電変換効率と高い生産性を両立した光電変換装置及びその製造方法を提供することを目的とする。

[0012] また、本発明は、大小の凹凸が混在した形状によりヘイズ率を高めた透明電極付き基板を用いた光電変換装置において、開放電圧と形状因子の低下を抑制しつつ高い光電変換効率を実現すること、およびこのような光電変換装置の製造方法を提供することを目的とする。

[0013] 上記課題を解決するために、本発明の第1の態様にかかる光電変換装置は、以下の手段を採用する。

すなわち、本発明の第1の態様にかかる光電変換装置は、透明絶縁性の基板上に透明電極層を設けてなる透明電極付き基板と、該透明電極付き基板の透明電極層側に順次形成された、結晶質シリコン系半導体を主として有する光電変換層ならび

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に裏面電極層とを少なくとも有してなる光電変換装置であって、前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上であり、前記光電変換層の膜厚が1.2μm以上2μm以下であり、かつラマン比が3.0以上8.0以下である光電変換装置である。

[0014] 前記第1の態様にかかる光電変換装置において、結晶質シリコン系光電変換層のラマン比を3.0以上8.0以下とすることにより、結晶の粒界が適度に非晶質シリコンで充填された光電変換装置を得ることができる。これにより、結晶粒界の電流リークを抑制できるので、開放電圧(Voc)及び形状因子(FF)の低下が抑制された光電変換装置を得ることができる。前記透明電極付き基板を用いた場合には、基板の凹凸に起因して欠陥の多い結晶粒界が生成しやすいため、結晶粒界の非晶質シリコンによる充填が特に有効である。

[0015] また、膜厚が1.2μm以上2μm以下の前記結晶質シリコン系半導体を主として有する光電変換層を形成することにより、結晶質シリコン系半導体を主として有する光電変換層のi層の膜厚を薄膜としても、高い発電電流を生じる光電変換装置を製造することができ、更に欠陥数を膜厚分低下でき、また、膜厚方向の電位勾配が大きいので発生電荷が欠陥にトラップされにくくなるので、開放電圧(Voc)及び形状因子(FF)の低下が抑制された光電変換装置を製造することができる。従って、薄膜化と高効率化を同時に達成した光電変換装置を製造でき、さらに、結晶質シリコン系i層を薄膜化することで、この製膜によって律速される光電変換装置の製造時間を短縮することができるので、光電変換装置の生産性が向上する。

[0016] 一般にヘイズ率といえば、ヘイズメータで計測される、波長が約550nmの光のヘイズ率をさす。波長550nmのヘイズ率が高いと波長550nm程度の光はよく散乱されるが、長波長光は該波長のヘイズ率が高ければよく散乱されるが、該波長のヘイズ率が低ければ散乱されにくい。従来の一層の凹凸(テクスチャ)構造の場合、波長550nmのヘイズ率が30%であっても、波長800nmの分光ヘイズ率は5%以下となり、結晶質シリコン系の光電変換層で光を閉じ込めたい700～900nmの波長域の光の散乱増強による光閉じ込めは不十分であった。また、350nm以下の波長域では、前記透明電極基板の透過率が小さくなるためヘイズ率を正しく計測することができない

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。したがって、550nm以上800nm以下の波長のヘイズ率を、波長を特定した光を用いて計測する分光ヘイズ率で定義し、分光ヘイズ率20%以上、より好ましくは30%以上とすることにより、結晶質シリコン系の光電変換層で光閉じ込めの影響を強く受ける700～900nmの波長域の光の散乱、光閉じ込めを増強でき、発電電流を増大することができる。

[0017] 前記第1の態様にかかる光電変換装置において、前記透明電極付き基板と前記結晶質シリコン系半導体を主として有する光電変換層との間に、非晶質シリコン系半導体を主として有する光電変換層を形成してもよい。

[0018] このような構成とすることにより、非晶質シリコン系半導体を主として有する光電変換層では太陽光の短波長側成分の光電変換が行われ、結晶質シリコン系半導体を主として有する光電変換層では太陽光の長波長側成分の光電変換が行なわれるので、より光電変換効率の高い光電変換装置とすることができる。

[0019] 前記第1の態様にかかる光電変換装置において、前記非晶質シリコン系半導体を主として有する光電変換層と前記結晶質シリコン系半導体を主として有する光電変換層との間に、中間コンタクト層を形成してもよい。

[0020] 中間コンタクト層を構成とすることにより、非晶質シリコン系半導体を主として有する光電変換層を薄膜化し、劣化率を改善できる一方で、結晶質シリコン系半導体を主として有する光電変換層への入射光が低下し、電流値が低下する。したがって、非晶質シリコン系半導体を主とする光電変換層の劣化率改善と、結晶質シリコン系半導体を主とする光電変換層の発電電流の低下との相対関係から、中間コンタクト層の膜厚は、90nm以下とすることが好ましく、さらには50nm以上70nm以下とすることがより好ましい。また、中間コンタクト層としては、ZnO系膜（例えば、GZO膜）で形成され、ZnO系単膜での光吸収率がλ＝450nm以上1000nm以下の範囲で1%未満であることがより好ましい。中間コンタクト層の透明性が損なわれると、結晶質シリコン系半導体を主とする光電変換層へ入射する光が低下し、発電電流が低下するため、波長が450nm以上1000nm以下の波長領域に対しては、ほぼ透明であることが好ましい。

[0021] 前記第1の態様にかかる光電変換装置において、前記透明電極付き基板の透明

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電極層表面が、複数の山部と複数の平坦部とで構成され、該山部及び該平坦部の表面がミクロの多数の凸部を連続して有してなり、前記山部の前記基板面垂直方向における高さが0．4μm以上0．7μmであり、基板面10μm角における前記山部の数が15以上50以下であり、前記ミクロの多数の凸部の底面径が0.1μm以上0.3μm以下であり、高さ／底面径の比が0.7以上1.2以下であるものが好ましい。

[0022] 前記第1の態様にかかる光電変換装置は、前記特性を有する透明電極付き基板を適用することで、結晶質シリコン系半導体を主として有する光電変換層（例えば、タンデム型太陽電池のボトムセル）のi層の膜厚を例えば1．5μmの薄膜としても、高い発電電流を生じる。更に結晶質シリコン系半導体を主として有する光電変換層のi層を薄膜化することにより、開放電圧（Voc）及び形状因子（FF）の低下も抑制できる。すなわち、結晶質シリコン系半導体を主として有する光電変換層を薄膜とすることにより、欠陥数を膜厚分低下でき、また、膜厚方向の電位勾配が大きいので発生電荷が欠陥にトラップされにくくなる。従って、光電変換装置の薄膜化と高効率化を同時に達成できる。さらに、結晶質シリコン系光電変換層中のi層を薄膜化できることにより、この層の製膜時間によって律速される光電変換装置の製造時間を短縮することができるので、前記第1の態様にかかる光電変換装置は、生産性が向上したものとなる。

[0023] 従来の技術において開放電圧と形状因子が低下した原因の1つとして、透明電極の谷の部分から光電変換層の膜厚方向に膜成長相間の不連続な境界（その境界を「異相」と呼ぶことにする）が生じ、キャリアの再結合中心となるためと推定される。この異相は、下地の谷々の面からシリコン膜が製膜・成長する際に、その成長面が衝突し、衝突面が格子の欠陥或いは微細な隙間となったものと推定され、キャリアの再結合による損失の原因となる。尚、この光電変換層の膜厚方向の異相は、光電変換層の断面方向の透過顕微鏡分析によって、検出することができる。倍率8万倍以上で光電変換層を長さ100μmの範囲で観察し、亀裂が認められたとき異相がある、貫通する異相が1本でも認められたとき貫通する異相があると判断する。

[0024] この異相の発生自体を抑制するには、透明導電性酸化物基板の凹凸を単純に大型化するのではなく、大きな凹凸と小さな凹凸が混在することが有効である。しかしな

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がら、前記透明電極を用いた場合においても、例えば製膜速度が1nm／sec以上の高速で製膜すると完全に異相の発生を抑制することは難しく、異相発生の抑制には光電変換層を形成する製膜条件選定における制限がある。このため、本発明者らは、特に高速で製膜する場合において異相が発生しても光電変換層を貫通する異相を遮断する知見を得るに至った。

[0025] 従って、本発明者らは、この異相を抑制すること、または完全に抑制はできなくても光電変換層を貫通する異相を遮断できれば、開放電圧低下、形状因子低下を抑制できるという知見を得た。

[0026] この知見から、上記課題を解決するために、本発明の第2の態様にかかる光電変換装置及び第3の態様にかかる光電変換装置の製造方法は、以下の手段を採用する。

すなわち、本発明の第2の態様にかかる光電変換装置は、透明絶縁性の基板上に透明電極層を設けてなる透明電極付き基板と、該透明電極付き基板の透明電極層側に順次形成された、非晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも有し、前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上、特に好ましくは30%以上であり、前記非晶質シリコン系半導体を主として有する光電変換層中に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相（膜成長相間の不連続な境界）を遮断する層（異相遮断層と呼ぶこととする）を設けた光電変換装置、もしくは前記基板と前記非晶質シリコン系半導体を主として有する光電変換層の間に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相の形成を防止する異相防止層を設けた光電変換装置である。

[0027] 第2の態様にかかる光電変換装置によれば、非晶質シリコン系半導体を主として有する光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相を遮断または防止できるので、このような異相による電流リークを抑えることができ、開放電圧低下、形状因子低下が抑制される。

[0028] また、本発明の第3の態様にかかる光電変換装置の製造方法は、透明絶縁性の基

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板上に透明電極層を形成して透明電極付き基板を作製し、該透明電極付き基板の透明電極層側に非晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも順次形成する光電変換装置の製造方法であって、前記透明電極付き基板の透明電極層表面が多数の凸部を連続して有してなり、前記非晶質シリコン系半導体を主として有する光電変換層中に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相を遮断する異相遮断層を形成するか、もしくは前記透明電極層の形成と前記非晶質シリコン系半導体を主として有する光電変換層形成の間に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相の形成を防止する異相防止層を形成する、光電変換装置の製造方法である。

[0029] 第3の態様にかかる光電変換装置の製造方法によれば、非晶質シリコン系半導体を主として有する光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相が遮断または防止されるので、このような異相による電流リークが抑えられ、開放電圧低下、形状因子低下が抑制された光電変換装置を製造することができる。

[0030] 前記第2の態様にかかる光電変換装置及び第3の態様にかかる光電変換装置の製造方法において、前記非晶質シリコン系半導体を主として有する光電変換層をp層、i層、n層を順次形成してなる層とし、前記異相遮断層を前記i層の一部分において、p層、n層、あるいはi層の他の部分より低速で製膜された層とすることができる。低速で製膜することにより、製膜面表面での製膜粒子の拡散・移動時間が増大し、より安定なサイトに堆積して低欠陥の層、即ち異相が少ない層を形成することができる。また、低速で製膜された層はi層の一部分と薄いため、低速で製膜する製膜時間にかかる処理時間は、全体の生産時間に与える影響としては少なくなり、生産性を維持したまま異相が少ない層を形成することができる。

[0031] あるいは、前記非晶質シリコン系半導体を主として有する光電変換層をp層、i層、n層を順次形成してなる層とし、前記n層の一部或いは全体を非晶質の層として、前記n層が前記異相遮断層の機能を有することができる。なお、非晶質とは、ラマン分光分析で分析したとき、Si結晶のピークが全く検出されないものであり、製膜条件では、水素ガス／シランガス希釈率を低下する方向、又はRFパワーを低下する方向で得る

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ことができる。積層膜で再表面のみ非晶質膜にする場合は、ラマン分光分析で下地のSi結晶質膜のピークが検出されることがあり、ガラス基板又は透明電極つきガラス基板上に、単一条件の膜のみを形成してラマン分光分析を実施してSi結晶ピークの有無を判断することとする。非晶質の膜は、欠陥が水素で終端されるので、結晶質と比較して欠陥が連続しにくいために異相となりにくく、異相を遮断する機能を有するものである。

あるいは、前記非晶質シリコン系半導体を主として有する光電変換層をp層、i層、n層を順次形成してなる層とし、前記n層の少なくともその一部を200Pa以上の圧力下で製膜した層とすることにより、前記n層が異相遮断層の機能を有することができる。高圧で製膜すると、製膜される原料ガスの気相中での衝突拡散が促進され、下地の凹部にも原料ガスが到達しやすいために、凹部にも均一に製膜されるので、欠陥上にも均一に良好な膜が形成される、すなわち異相を抑制できると考えられる。

あるいは、前記異相防止層を、前記凸部を円滑化した前記透明電極層とすることができる。前記凸部の円滑化とは、凸部が連続して形成されることにより凸部の境界に生成する谷部について、通常は平面どおしの組合せのため谷の底は明瞭な線状であるが、その線がないように底面を円滑化したもの、例えば、スプーンカットのような形状を有することである。

[0032] 前記異相防止層を、前記透明電極層表面にイオン処理を施して形成してもよい。イオン処理とは、例えば真空中でのアルゴンイオン照射によるイオンエッチングであり、透明電極の表面形状を原子レベルのエッチング、再付着により制御できる。イオンエッチングのイオン照射角度とイオンエネルギーを調整することで、透明電極の凹凸の特に斜面部の原子をエッチング除去し、谷部の底に再付着させることができ、結果として鋭利な谷形状を円滑化することができる。

[0033] 前記第2の態様にかかる光電変換装置及び第3の態様にかかる光電変換装置の製造方法において、前記透明電極付き基板は、550nm以上800nm以下の波長における分光ヘイズ率が20%以上であるものが好ましい。前記分光ヘイズ率が30%以上であるものが特に好ましい。

上述のとおり、従来の凹凸(テクスチャ)構造の場合、波長550nmの分光ヘイズ率

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が30％であっても、波長800nmの分光ヘイズ率は5％以下となり、結晶質シリコン系半導体の光電変換層で光を閉じ込めたい700～900nmの波長域の光の散乱増強による光閉じ込めは不十分であった。そこで、前記第2の態様にかかる光電変換装置及び第3の態様にかかる光電変換装置の製造方法においては、凹凸を大型化して、長波長光に対しても高ヘイズとなるようにする。また、350nm以下の波長域では、前記透明電極の透過率が小さくなるためヘイズメータにより分光ヘイズ率を計測することができない。したがって、550nm以上800nm以下の波長の分光ヘイズ率を20％以上、好ましくは30％以上とすることにより、結晶質シリコン系半導体の光電変換層で光閉じ込めの影響を強く受ける700～900nmの波長域の光の散乱、光閉じ込め効果を増強でき、発電電流を増大することができる。

[0034] 前記第2の態様にかかる光電変換装置及び第3の態様にかかる光電変換装置の製造方法において、前記非晶質シリコン系半導体を主として有する光電変換層と前記裏面電極の間に、結晶質シリコン系半導体を主として有する光電変換層を形成してもよい。

[0035] このような構成とすることにより、非晶質シリコン系半導体を主として有する光電変換層では太陽光の短波長側成分の光電変換が行われ、結晶質シリコン系半導体を主として有する光電変換層では太陽光の長波長側成分の光電変換が行なわれるので、より光電変換効率の高い光電変換装置とすることができる。

[0036] また、結晶質シリコン系半導体を主として有する光電変換層は結晶質シリコン系半導体に限らず、結晶質もしくは非晶質シリコン系半導体、結晶質もしくは非晶質シリコンゲルマニウム系半導体を主として有しても同等の効果が得られる。

[0037] また、結晶質シリコン系半導体を主として有する光電変換層とさらに第3の光電変換層を積層して3層構造以上の光電変換装置としても良い。この場合、結晶質シリコン系半導体を主として有する光電変換層及び第3の光電変換層は、結晶質もしくは非晶質シリコン系半導体、結晶質もしくは非晶質シリコンゲルマニウム系半導体を主として有する光電変換層とすることともでき、非晶質シリコン系半導体を主として有する光電変換層、結晶質シリコン系半導体を主として有する光電変換層光電変換層、第3の光電変換層の順に長波長側成分へと吸収が増大するように、各光電変換層の

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材料や膜質、膜厚を設定すれば良い。

[0038] 本発明によれば、高い光電変換効率と高い生産性を両立した光電変換装置及びその製造方法を提供することができる。本発明の光電変換装置は、太陽電池として好適に利用することができる。

[0039] また、本発明によれば、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上、特に好ましくは30%以上である透明電極付き基板を用いた光電変換装置において、開放電圧と形状因子の低下を抑制しつつ高い光電変換効率を実現することができる。さらに、このように優れた光電変換装置の製造方法を提供することができる。本発明の光電変換装置は、太陽電池として好適に利用することができる。

[0040] また、光電変換層を薄膜化しても高い光電変換効率が得られる。薄膜化により、発電電流は多少は低下するが、従来の基板に対し薄膜化による発電電流低下は大幅に改善できている。また、薄膜化により、開放電圧と形状因子が向上される。薄膜化による光電変換層の薄膜化により、光電変換層に含まれる欠陥を膜厚相当分低下できること、および光電変換層内に発生する起電力に対する電位勾配が拡大することによる生成電荷の再結合(欠陥による消滅)確率を低下できるためである。

[0041] 薄膜化は、生産性の点でメリットが大きい。光電変換装置ひとつあたりの生産時間を短縮でき、さらに生産装置の製膜室内部のメンテナンス頻度も低下でき、結果として、時間あたり或いは装置あたりの生産量を薄膜化の膜厚の比率以上に増大できる。従って、生産を考慮すると、光電変換効率の向上以上に、生産性向上のメリットが大きいといえる。

図面の簡単な説明

[0042] [図1]本発明の光電変換装置の構成を示す概略図である。

[図2]本発明の第1実施形態で用いられる透明電極付き基板の形状及び構成を示す一部切欠き断面図である。

[図3]図2に示す山部112の拡大図である。

[図4]本発明の太陽電池パネルの製造方法の実施形態の一部を示す概略図である。

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[図5]本発明の太陽電池パネルの製造方法の実施形態の一部を示す概略図である。

[図6]本発明の太陽電池パネルの製造方法の実施形態の一部を示す概略図である。

[図7]本発明の太陽電池パネルの製造方法の実施形態の一部を示す概略図である。

[図8]本発明の第2実施形態のイオン処理前における透明電極付き基板の透明電極表面の電子顕微鏡写真である。

[図9]本発明の第2実施形態のイオン処理後における透明電極付き基板の透明電極表面の電子顕微鏡写真である

[図10]本発明の第2実施形態の透明電極付き基板を用いて作製したタンデム型太陽電池の断面の透過型電子顕微鏡写真である。

[図11]本発明の第2実施形態の透明電極付き基板を用いて作製したタンデム型太陽電池の断面の透過型電子顕微鏡写真である。実施例7に示したように非晶質Si—i層の製膜後期を位相遮断層として、非晶質Si層を貫通する異相を抑制したものである。

[図12]実施例11のタンデム型太陽電池における、ボトムセルのn層製膜後のラマン比と太陽電池特性の関係を示す図である。

符号の説明

[0043] 1 基板

2 透明電極層

3 光電変換層

4 裏面電極層

6 太陽電池モジュール

90 光電変換装置

91 第1セル層(トップ層)

92 第2セル層(ボトム層)

93 中間コンタクト層

110 透明電極付き基板

111 基板

112 山部

114 透明電極

115 小山部

116 連続層

117 凸部

H_a 山部の高さ

P_a 山部間の平均ピッチ

H_c 小山部H_cの高さ

P_c 小山部間の平均ピッチ

H_b 凸部の高さ

P_b 凸部間のピッチ

15 絶縁溝

21 バックシート

23 出力ケーブル

50 太陽電池パネル

発明を実施するための最良の形態

[0044] 第1実施形態

以下に、本発明の第1実施形態について、図面を参照して説明する。

[0045] まず、本実施形態の光電変換装置の製造方法により製造される光電変換装置の構成について説明する。

[0046] 図1は、本実施形態の光電変換装置の構成を示す概略図である。光電変換装置90は、シリコン系太陽電池であり、基板1、透明電極層2、太陽電池光電変換層3としての第1セル層(トップ層)91ならびに第2セル層(ボトム層)92、及び裏面電極層4を具備する。本実施形態において、第1セル層91は非晶質シリコン系半導体を主として有する光電変換層であり、第2セル層は結晶質シリコン系半導体を主として有する光電変換層である。第2セル層92は、膜厚が1.2μm以上2.0μm以下、かつ、第

2セル層92のラマン比が3．0以上8．0以下であることが好ましい。より好ましくは、ラマン比が3．5以上8．0以下であり、更に好ましくは5．0以上7．5以下である。

[0047] 第2セル層92のラマン比を3．0以上8．0以下とすることにより、結晶の粒界が適度に非晶質シリコンで充填された光電変換装置を得ることができ、結晶粒界の電流リークを抑制できるので、開放電圧(Voc)及び形状因子(FF)の低下が抑制された光電変換装置を得ることができる。

[0048] ここで「ラマン比」とはラマン分光評価で520cm^{-1}の結晶Siの強度と480cm^{-1}の非晶質Siの強度の比(結晶Siの強度／非晶質Siの強度)をいう(以下同じ)。ラマン比の測定方法としては、光電変換装置の裏面電極を過酸化水素水等の溶剤で溶剤除去して供試体とする。まず、第2セル層92の膜面側から測定用光を照射する。測定用光としては、レーザー単色が用いられ、例えば、YAGレーザー光の2倍波(波長532nm)が好適に用いられる。第2セル層92の膜面側から測定用光を入射すると、ラマン散乱が観測されるが、測定用光、及び散乱光の一部は第2セル層92中で吸収される。したがって、例えば、YAGレーザー光の2倍波を測定用光として用いた場合は、入射面から約0．1μmの深さまでの情報を得ることができる。なお、第2セル層92と裏面電極層4との間に第2の透明電極層を形成している場合は、第2の透明電極層のラマンピークはバックグランドとして差し引くことができるので、第2の透明電極層を希塩酸等の溶剤により溶剤除去しなくてもしてもよい。

[0049] 上記したように、ラマン比は光電変換層i層(実質的に真性な層)を評価するが、一般的に用いられるレーザー波長532nmでは、0．1μmの侵入深さにより、表面から約0．1μmの膜の結晶化率を評価することとなる。本実施形態においては、第2セル層92のi層製膜後のラマン比が3．0以上8．0以下であることが直接的な意味であるが、最表面にn層が製膜されてもn層は膜厚が0．03μm程度と薄いのでi層からの情報が支配的であること、および一般的なn層の結晶性も2～10であることにより、n層製膜後にn層を含めたラマン比を計測してもn層製膜前と近い値となる。したがって、第2セル層92のラマン比は、3．0以上8．0以下が好ましい範囲となる。

また、ラマン比は製膜において製膜装置構造などにより基板1上で分布が発生する。例えば製膜時に基板1表面上での原料ガス組成変化による局所的なラマン比分布

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や、プラズマや温度分布による全体的なラマン比分布がある。このため、評価する基板1上で極力全体的な平均値として評価する。例えば、1m角以上の基板サイズであれば、均等に区分けした少なくとも10箇所以上の領域で計測し、この平均値で評価することが好ましい。

[0050] ラマン比が3.0以上8.0以下という値は、一般的に結晶化が進んだ結晶質シリコンの値より、非晶質シリコンを多く含むものである。特にダブルテクスチャ基板のような高ヘイズ基板を用いる場合、基板の凹凸に起因する結晶粒界の欠陥が生じるため、粒界を適度に非晶質シリコンで充填することが重要となる。ラマン比が3.0以上が好ましい理由は、結晶シリコン部で発生した電荷が断面方向につながった結晶構造を導通することができるように大部分の結晶構造が膜厚方向に連続するために必要なラマン比が3.0以上であるためで、これは断面観察により確認できる。ラマン比が8.0以下が好ましい理由は、柱状結晶の粒界が電流リークポイントとなり電圧が発生しなくなるのを抑制するために非晶質で結晶粒界を充填することが好ましく、実験的にその場合のラマン比が8.0以下であるためである。

[0051] なお、ここで、「シリコン系」とはシリコン(Si)やシリコンカーバイド(SiC)やシリコンゲルマニウム(SiGe)を含む総称である。また、「結晶質シリコン系」とは、アモルファスシリコン系すなわち非晶質シリコン系以外のシリコン系を意味するものであり、微結晶シリコンや多結晶シリコン系も含まれる。

[0052] 第1セル層91及び第2セル層92の間には、透明導電膜からなる中間コンタクト層93を設けても良い(但し、本発明の光電変換装置は、中間コンタクト層93を設けたものに限定されない)。中間コンタクト層93
を設けた場合、この中間コンタクト層93で入射太陽光の一部が反射されて、第1セル(トップ層)91に再度入射される。これにより、第1セル層(トップセル)91における発電電流が増加する。そして、第1セル層91の膜厚を薄くしても、中間コンタクト層93が積層されない場合と同等の発電電流を得ることができる。したがって、第1セル層91非晶質シリコン系半導体の膜厚を薄くすることにより、当該第1セル層91における光劣化を抑制でき、光電変換装置全体としての安定化効率を向上させることができる。

[0053] 中間コンタクト層93の膜厚を厚くすることにより、第1セル層91である非晶質シリコ

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ン系半導体の発電電流を増加させることができる。このとき，中間コンタクト層93により反射される太陽光の波長における第2セル層92での発電電流は減少する。実際には，第2セル層92である結晶質シリコン系半導体においては，第1セル層91である非晶質シリコン系半導体よりも長波長領域の太陽光による電気エネルギーへの変換が行われている。

[0054] 従って，中間コンタクト層93の膜厚を最適化することにより，中間コンタクト層93による，第2セル層92である結晶質シリコン系半導体が吸収すべき長波長領域の太陽光の吸収率を抑制することが必要になる。

[0055] 本実施の形態に係わる光電変換装置の中間コンタクト層93の膜厚と，第2セル層92における波長800nm（太陽光の長波長領域に対応）の量子効率（入射のうち発電に寄与する割合）との関係から，中間コンタクト層93の膜厚が厚くなると，中間コンタクト層93での長波長領域の太陽光の反射率も増大して，第2セル層92に入射する光量が減少する。中間コンタクト層93は，光吸収率がλ＝450nm以上1000nm以下の範囲で1%未満であることが好ましく，この波長領域に対しては，ほぼ透明であることが好ましい。

[0056] 一方，中間コンタクト層93の膜厚が厚くなると，中間コンタクト層93と裏面電極層4との間で光の閉じ込め効果が増大する。このため，第2セル層92に入射した光吸収率が増大する。波長800nmの太陽光に対して，第2セル層92における光の閉じ込め効果が有効に作用する（量子効率を一定の値に維持することができる）中間コンタクト層93の膜厚は100nm以下である。

[0057] 上述したように，第1セル層91と第2セル層92との発電電流バランスを考慮して，最適な中間コンタクト層93の膜厚値は実験的に90nm以下となり，より好ましくは50nm以上70nm以下となる。これにより，より高い安定化効率を有する光電変換装置が実現される。

[0058] 次に，本発明の第1実施形態による光電変換装置において用いられる，透明電極を形成した透明絶縁性基板（以下，「透明電極付き基板」ともいう）の形状及び構成を，図2及び図3を用いて詳細に説明するが，本発明の光電変換装置及びその製造方法は，これらの図面によって限定されない。

[0059] 図2は、本実施形態で用いられる透明電極付き基板の形状及び構成を示す一部切欠き断面図であり、図3は、図2に示す山部112の拡大図である。図2に示すように、本実施形態において用いられる、透明電極付き基板110は、ガラス基板111上に、不連続な複数の山部112によるマクロな凹凸(テクスチャ)と、この山部間をうめる複数の平坦部113とを有しており、該山部112及び該平坦部113の外表面は、ミクロの多数の凹凸(テクスチャ)を有する構造となっている。以下、このような2つの凹凸を有する構造を、ダブルテクスチャ構造という。

[0060] また、本実施形態においては、図2に示すように、透明電極114は、第1の酸化物からなる不連続な小山部115と、その上に形成される第2の酸化物からなる連続層であって該連続層の表面にミクロの多数の凸部を連続して有する連続層116とからなるのが好ましい。小山部115の密度は、基板111面の10μm角あたり15以上50以下とされ、20以上45以下がより好ましい。この小山部115間の平均ピッチP_sは、1.0μm以上3μm以下に相当する。

第2の酸化物からなる連続層116は、小山部115上及び小山部115が形成されていない部分のガラス基板111上に連続的に形成されている。

[0061] 本実施形態においては、上記山部112の平均の高さH_s(平坦部上のミクロの凸部の頂部からの高さの平均値)は、0.4μm以上0.7μm以下であり、0.5μm以上0.6μm以下であることがより好ましい。

また、隣接する上記山部間の平坦部の距離(以下、単に「山部間の間隔」ともいう。)W_sは、直線上に0μm以上1.5μm以下であることが好ましく、0μm以上1.0μm以下であることがより好ましく、0.1μm以上0.4μm以下(いずれの山部112も不連続である)であることがさらに好ましい。本実施形態においては、複数の山部112は不連続である部分と連続している部分があってもよく、山部間の間隔W_sが0μm以上1.5μm以下であるということは、平坦部がないところがあってもよいということである。なお、平坦部が無い場合には、上記山部に隣接していなくても、上記山部付近の平坦部を用いてH_sを計測でき、または断面の顕微鏡観察を行うことでH_sは計測することができる。

さらに、上記山部112の密度は、小山部115の密度と同様の値となり、基板111面

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の10μm角あたり15以上50以下となり、20以上45以下がより好ましい。この山部112間の平均ピッチP_sは、1.0μm以上3μm以下に相当する。

[0062] 本実施形態においては、上記小山部115の高さH_cは、上記山部の高さH_sと同様の値、すなわち0.4μm以上0.7μm以下であり、0.5μm以上0.6μm以下であることがより好ましい。

[0063] 本実施形態においては、山部112及び平坦部113の表面、すなわち、第2の酸化物からなる連続層116の表面は、図3に示されるように、ミクロの多数の凸部117を有している。ミクロの多数の凸部の底面径が0.1μm以上0.3μm以下であり、高さ／底面径の比が0.7以上1.2以下である。尚、ミクロの凸部の連続層は、表面全体においてミクロの凸部が存在する状況を示していて、一部にミクロの凸部が欠損した領域が存在しても、連続している状況とみなすものである。

[0064] また、図3において、上記小山部115上の連続層116の厚さH_d(ミクロの凸部を含む)は、0.5μm以上1.0μm以下であることが好ましく、0.5μm以上0.7μm以下であることがより好ましい。同様に、上記ガラス基板111上の連続層116の厚さH_e(ミクロの凸部を含む)は0.5μm以上1.0μm以下であることが好ましく、0.5μm以上0.7μm以下であることがより好ましい。

[0065] 本実施形態においては、上記山部112及び上記平坦部113の外表面を、このような山部による凹凸(マクロな凹凸)よりも小さな凹凸(ミクロな凹凸)とすることにより、短波長の光を強く散乱することができ、全体として広い領域の光を有効に散乱することが可能になる。すなわち、大きな凹凸である山部により長波長の光を散乱し、小さな凹凸表面より短波長の光を散乱することができるため、全体として高い光散乱性を達成することができる。

特に本実施形態においては、山部112の高さと密度を制御することにより、長波長の光の散乱を最適化し、結晶質シリコン系半導体からなる光電変換層の発電効率の向上と、製膜時間の短縮が実現される。

[0066] 前記透明電極付き基板110におけるこのような表面性状は、例えば、以下に示す方法により確認することができる。

(1)表面形状の解析:膜表面の凸部を走査型電子顕微鏡(SEM)で観察し、得ら

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れる顕微鏡写真より、凸部の底面径を測定することができる。また、膜表面の凹凸形状をSEM、原子間力顕微鏡(AFM)により観察し、得られる顕微鏡写真より、膜表面の凹凸形及び凸部の高さを解析することができる。

(2)表面被覆率の測定:第1の酸化物からなる小山部の基板上への被覆率をSEM写真から測定し、基板上を小山部が占める面積を、基板の当該被覆面全体の面積で割った値を表面被覆率として評価することができる。

また、質量膜厚とは、基板上の一定面積中にある不連続の金属酸化物に対し、蛍光X線装置でその金属酸化物の金属量に比例する検出量を調べ、別途用意してある基板上に連続し、膜厚の既知の同種の金属酸化物における蛍光X線装置の検出量と比較して、不連続な酸化物の体積が連続になったと仮定して得られた膜厚を示す。

[0067] また、このような形状及び構成を有する透明電極付き基板110は、基板全体において、550nm以上800nm以下の波長における分光ヘイズ率が30%以上、好ましくは40%以上である。

[0068] ここで、「分光ヘイズ率」とは、透過光における散乱成分の割合を示すものである。分光ヘイズ率は波長に依存し、分光ヘイズ率をHz(λ)、全透過率をT_{total}(λ)、透過光の直進成分をT_{direct}(λ)、透過光の散乱成分を$T_{diffuse}$(λ)とすると、下記式に示す関係が成り立つ。

$$T_{total}(\lambda)=T_{direct}(\lambda)+T_{diffuse}(\lambda)$$

$$Hz(\lambda)=T_{diffuse}(\lambda)/T_{total}(\lambda)\times 100[\%]$$

[0069] 以下に、上述した本実施形態の透明電極付き基板の形状及び構成ならびに特性を満たす基板(透明基板)、第1の酸化物及び第2の酸化物について詳述する。

[0070] <基板(透明基板)>

本実施形態の透明電極付き基板に用いられる基板は、必ずしも平面で板状である必要はなく、曲面でも異型状でもよい。

このような基板としては、少なくともその表面が後述する第1の酸化物と異なる材料であることが好ましく、具体的には、ガラス基板、セラミックス基板、プラスチック基板、金属基板等や、これらの基板表面に酸化ケイ素膜、酸化アルミニウム膜、酸化ジルコ

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ニウム膜、酸化チタン膜などのアルカリバリヤ層を施したもの等が挙げられる。これらのうち、透光性に優れた透明の基板であることが好ましく、ガラス基板もしくはアルカリバリア層を施したガラス基板であることが強度及び耐熱性の点から好ましい。

また、このような基板は、光電変換層の主たる吸収波長域である550nm以上800nm以下の波長領域において高い透過率、例えば80%以上の透過率を有することが好ましく、十分絶縁性で、かつ化学的、物理的耐久性が高いことが望ましい。

[0071] 上記ガラス基板としては、具体的には、例えば、無色透明なソーダライムシリケートガラス、アルミノシリケートガラス、ボレートガラス、リチウムアルミノシリケートガラス、石英ガラス、ホウ珪酸ガラス基板、無アルカリガラス基板、その他の各種ガラスからなる透明ガラス板を用いることができる。

また、本実施形態の透明電極付き基板を太陽電池用基板に用いる場合においては、ガラス基板の厚さは0.2mm以上6.0mm以下であることが、強度及び透過率の点から好ましい。

[0072] なお、ソーダライムシリケートガラス等のナトリウムを含有するガラスからなるガラス基板または低アルカリ含有ガラスからなるガラス基板の場合には、ガラスからその上面に形成される透明電導膜へのアルカリ成分の拡散を最小限にするために、上述したアルカリバリヤ層を施したガラス基板を用いることが好ましい。

また、ガラス基板の表面に、ガラス基板の表面と、その上に設けられる層との屈折率の差異を軽減するための層をさらに有していてもよい。

[0073] <第1の酸化物>

本実施形態の透明電極付き基板の透明電極膜を構成する第1の酸化物は、可視光域で高透明な酸化物であれば特に限定されず、その具体例としては、TiO_2、SnO_2、In_2O_3、ZnO、CdO、$CdIn_2O_4$、$CdSnO_3$、$MgIn_2O_4$、$CdGa_2O_4$、$GaInO_3$、$InGaZnO_4$、$Cd_2Sb_2O_7$、Cd_2GeO_4、$CuAlO_2$、$CuGaO_2$、$SrCu_2O_2$、Al_2O_3等が挙げられる。これらのうち、TiO_2、SnO_2及びフッ素を含有するSnO_2からなる群より選択される少なくとも1種を用いることが好ましい。

本実施形態においては、小山部を形成するこのような第1の酸化物の屈折率は、波長400nm以上800nm以下において、1.8以上2.2以下であることが好ましく、さら

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に、1．9以上2．1以下であることが好ましい。

第1の酸化物の形成方法として一例を示す。上述したアルカリバリア層付きガラス基板をベルトコンベア炉において520℃に加熱し、四塩化錫、水、塩化水素ガスを同時にガラス基板に吹き付けて酸化錫核を形成する。この際，四塩化錫、水は，あらかじめ加熱し、窒素ガスをバブリングして塩化水素ガスと同時に移送することでガラス基板上に吹き付ける。

酸化錫核を形成した後、四塩化錫と水を同時にガラス基板に吹き付けることで第1の酸化物であるSnO_2を形成する。この際，四塩化錫、水は、あらかじめ加熱し、窒素ガスをバブリングして移送することでガラス基板上に吹き付けた。

[0074] なお、このような第1の酸化物からなる小山部は、上述したように，不連続な突起物であって連続膜ではないので、該突起物に覆われていない透明基板部分は、当然ながら小山部による入射光の吸収損はゼロであるため、光電変換層への入射光量を増やすことができる。

これらの小山部は、長波長光の分光ヘイズ率を高める(光の散乱度を上げる)部分であり、自由電子による吸収を抑えて、高透明にするために、電気導電性はないのが好ましい。したがって、上記第1の酸化物としてSnO_2を用いた場合は、SnO_2のみからなるか、フッ素を含有する場合でもフッ素は、SnO_2に対して0．01mol%以下の含有量であることが好ましく、0．005mol%以下の含有量であることがより好ましい。

[0075] ＜第2の酸化物＞

本実施形態の透明電極付き基板の透明電極膜を構成する第2の酸化物は、可視光域で透明であり、さらに導電性を有している透明導電性酸化物であることが必要であり、その具体例としては、SnO_2、ZnO、In_2O_3等が挙げられ、2種以上を併用してもよく、さらに、導電性発現のためのドーパントを含有していることが好ましい。

これらのうち、SnO_2はドーパントとしてフッ素またはアンチモンをSnO_2に対して0．01mol%以上4mol%以下含有することが好ましい。ZnOはドーパントとしてホウ素、Al及びGaからなる群から選択される少なくとも1種をZnOに対して0．02mol%以上5mol%以下含有することが好ましい。In_2O_3はドーパントとしてSnをIn_2O_3に対して0．02mol%以上4mol%以下含有することが好ましい。なお、これらのドーパントを用い

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たドーピングは、ハロゲン化水素によるものであってもよい。このようなハロゲン化水素としては、具体的には、例えば、HF、HBr等が挙げられる。

本実施形態においては、連続層を形成するこのような第2の酸化物の屈折率は、波長400nm以上800nm以下において、1．8以上2．2以下であることが好ましく、さらに、1．9以上2．1以下であることが好ましい。

[0076] また、上記第2の酸化物としてフッ素を含有するSnO_2を用いることにより、導電電子密度が向上する。太陽電池に用いる基板としては、導電電子密度は、$5\times10^{19}cm^{-3}$以上$4\times10^{20}cm^{-3}$以下であることが好ましく、$1\times10^{20}cm^{-3}$以上$2\times10^{20}cm^{-3}$以下であることがより好ましい。導電電子密度がこの範囲であれば、第2の酸化物からなる連続層の光吸収量が少なく、高透明で、かつ活性水素種に対して高い耐久性があるので、薄膜シリコン系太陽電池を形成する際に一般に用いられる水素プラズマ照射によっても、透明性は損なわれないため好ましい。

[0077] 上述した第1の酸化物と第2の酸化物とは、同じ酸化物を用いてもよく、本実施形態においては、いずれもSnO_2を用いることが好ましい。また、第1の酸化物及び第2の酸化物層の屈折率は、同等程度であることが好ましく、具体的には、1．8以上2．2以下であることが好ましい。第1の酸化物と第2の酸化物の屈折率がともにこの範囲であると、第1の酸化物と第2の酸化物との界面における光の反射が制御され，透過率が低下しないことから好ましい。

[0078] また、本実施形態においては、上述した第1の酸化物からなる小山部と、上述した第2の酸化物からなる連続層との間に、該第1の酸化物及び該第2の酸化物とは組成が異なる酸化物からなる酸化物層（以下，単に「異なる酸化物層」ともいう。）を有していることが好ましい。

このような異なる酸化物層を有していることにより、第2の酸化物からなる連続層の表面にミクロの多数の凸部が形成されやすく、山部と平坦部とを有する構造を容易に形成することができる。

[0079] また、このような異なる酸化物層を有する多層構造の透明電極膜においては、各層の界面での反射を軽減し、後述する光電変換層への入射光量を最大にする必要がある。すなわち、ガラス基板、第1の酸化物からなる小山部、異なる酸化物層、第2の

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酸化物からなる連続層の各界面での光反射をできるだけ低減することが望ましい。そのためには、第1の酸化物、異なる酸化物及び第2の酸化物の屈折率ができるだけ近いこと、または屈折率が離れている場合は、異なる酸化物層ができるだけ薄いことが望ましい。

このような異なる酸化物としては、具体的には、例えば、Si、Sn、Al、Zr及びTiからなる群から選ばれる1種以上の原子の酸化物が挙げられ、これらのうち、Siの酸化物を主成分とすることが好ましい。また、上記異なる酸化物は、高い透光性を有する必要があるため、非結晶性であるSiO_2であることがより好ましい。

なお、異なる酸化物層の膜厚は2nm以上40nm以下であることが好ましく、10nm以上30nm以下であることがより好ましい。

[0080] 本実施形態の透明電極付き基板は、上述したように、複数の山部とその間をうめる複数の平坦部とで構成され、該山部及び外平坦部の表面がミクロの多数の凸部を連続して有するものであるが、基板上から山部の頂上(ミクロの凸部を含む)までの高さは0.8μm以上3.0μm以下であることが好ましく、0.8μm以上1.0μm以下であることがより好ましい。ミクロの多数の凸部の底面径が0.1μm以上0.3μm以下であり、高さ/底面径の比が0.7以上1.2以下であることが望ましい。また、膜全体のシート抵抗が8Ω/□以上20Ω/□以下であることが好ましく、8Ω/□以上12Ω/□以下であることがより好ましく、550nmにおける透過率(透明性)は、浸液法で測定した場合、80%以上90%以下であることが好ましく、85%以上90%以下であることがより好ましい。

また、上記構成からなる本実施形態の透明電極付き基板を、光電変換装置の透明電極に用いると、基板を経て入射された光は、透明電極により屈折、散乱されて光電変換部に入射し、光電変換部中を長い距離にわたって通過する。その結果、多くの光が光電変換部にて吸収され、光電変換効率が向上する効果を奏するものとなる。特に、太陽電池に用いた場合には、開放電圧及び曲線因子を低下させずに短絡電流を高く維持することが可能となるため、光電変換効率が向上するものとなる。

[0081] 次に、本実施形態の太陽電池パネルの製造方法について説明する。ここでは、基板1としてのガラス基板上に太陽電池光電変換層3として非晶質シリコン系半導体を

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主として有する光電変換層及び結晶質シリコン系半導体を主として有する光電変換層を順次積層する例について説明する。図4～図7は、本実施形態の太陽電池パネルの製造方法を示す概略図である。

[0082] (1)図4(a):

基板1としてソーダフロートガラス基板(1．4m×1．1m×板厚:4mm)を使用する。基板端面は破損防止にコーナー面取りやR面取り加工されていることが望ましい。

[0083] (2)図4(b):

前記実施形態に基づき、基板1上に透明電極層2を製膜し、透明電極付き基板を形成する。透明導電層2として，透明電極膜に加えて、基板1と透明電極膜との間にアルカリバリア膜(図示されず)を形成しても良い。アルカリバリア膜は、酸化シリコン膜(SiO_2)を50nm以上150nm以下、熱CVD装置にて約500℃で製膜処理する。

[0084] (3)図4(c):

その後、基板1をX－Yテーブルに設置して、YAGレーザーの第1高調波(1064nm)を、図の矢印に示すように、透明電極膜の膜面側から入射する。加工速度に適切となるようにレーザーパワーを調整して、透明電極膜を発電セル5の直列接続方向に対して垂直な方向へ、基板1とレーザー光を相対移動して，溝10を形成するように幅約6mm以上12mm以下の短冊状にレーザーエッチングする。

[0085] (4)図4(d):

プラズマCVD装置により、減圧雰囲気:30Pa以上150Pa以下、基板温度:約200℃、プラズマRF発生周波数:13MHz以上100MHz以下にて光電変換層3の第1セル層(トップ層)91として、非晶質シリコン薄膜からなるp層膜／i層膜／n層膜を順次製膜する。第1セル層91は、SiH_4ガスとH_2ガスとを主原料に，透明導電層2の上に製膜される。太陽光の入射する側からp層、i層、n層がこの順で積層される。

[0086] 本実施形態において、第1セル層91のp層は、SiH_4, H_2, CH_4, B_2H_6ガスをRFプラズマで反応生成させた、非晶質のBドープSiC膜であり、膜厚は4nm以上16nm以下とすることが好ましい。第1セル層91のi層は、SiH_4とH_2をRFプラズマで反応生成させた，非晶質Si膜であり、膜厚は100nm以上400nm以下とすることが好ましい。第1セル層91のn層は、SiH_4, H_2, PH_3ガスをRFプラズマで反応生成させた、結晶

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成分を含むSi膜であり、n層単膜のラマン比は2以上であり、膜厚は10nm以上80nm以下とすることが好ましい。なお、ここで「ラマン比」とはラマン分光評価で520cm^{-1}の結晶Siの強度と480cm^{-1}の非晶質Siの強度の比（結晶Siの強度／非晶質Siの強度）をいう（以下同じ）。また、前記p層（SiC膜）とi層（Si膜）の界面でのバンド不整合を抑制するために、バッファー層（図示略）として，バンドギャップが中間の物質を挿入しても良い。

[0087] 次に、第1セル層91の上に、プラズマCVD装置により、減圧雰囲気：3kPa以下，基板温度：約200℃、プラズマRF発生周波数：40MHz以上200MHz以下にて、第2セル層（ボトム層）92としての微結晶シリコン薄膜からなる微結晶p層膜／微結晶i層膜／微結晶n層膜を順次製膜する。

[0088] 本実施形態において、第2セル層92のp層は、SiH_4，H_2，B_2H_6ガスをRFプラズマで反応生成させた、結晶成分を含むSi膜であり、p層単膜のラマン比は2以上であり、膜厚は10nm以上60nm以下とすることが好ましい。第2セル層92のi層は、SiH_4とH_2をRFプラズマで反応生成させた，結晶成分を含むSi膜であり、このi層を1．5μm膜厚に積んだときのラマン比は3．0以上8．0以下であり，膜厚は1200nm以上2000nm以下とすることが好ましい。より好ましくは、ラマン比を3．5以上8．0以下、さらに好ましくは5．0以上8．0以下とすると好適である。ラマン比の下限値は，結晶シリコン部で発生した電荷が断面方向につながった結晶構造を導通することができるように、大部分の結晶構造が膜厚方向に連続するために必要なラマン比が3．0以上であることから決まり、これは断面観察により確認することができる。また、ラマン比の上限値は柱状結晶の粒界が電流リークポイントとなり、電圧が発生しなくなるのを抑制するために、非晶質で結晶粒界を充填することが好ましく、ラマン比が8．0以下であることが実験的に求められる。

[0089] 第2セル層92のn層は、SiH_4，H_2，PH_3ガスをRFプラズマで反応生成させた、結晶成分を含むSi膜であり、n層単膜のラマン比は2以上であり、膜厚は10nm以上80nm以下とすることが好ましい。

[0090] 微結晶シリコン薄膜、特に微結晶i層膜をプラズマCVD法で形成するにあたり、プラズマ放電電極と基板1の表面との距離dは、3mm以上10mm以下にすることが好ま

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しい。3mmより小さい場合、大型基板に対応する製膜室内の各構成機器精度から距離dを一定に保つことが難しくなるとともに、近過ぎて放電が不安定になる恐れがある。10mmより大きい場合、十分な製膜速度(1nm／s以上)を得難くなるとともに、プラズマの均一性が低下しイオン衝撃により膜質が低下する。第2セル層92のi層は、RF周波数40MHz以上200MHz以下、ガス圧力0．5kPa以上3kPa以下、製膜速度1nm／s以上3nm/s以下で製膜されることが好ましく、本実施形態においてはRF周波数60MHz、ガス圧力1．6kPa、製膜速度2nm／sで製膜される。

[0091] 第1セル層91と第2セル層92の間に電流整合性を取るために半反射膜となることを目的に、中間コンタクト層93として、膜厚0nm以上90nm以下のZnO系膜(例えばGZO(Gaドープ ZnO)膜)をスパッタリング装置により製膜して設けても良い。この中間コンタクト層93は、ZnO単膜での光吸収率がλ＝450nm以上1000nm以下の範囲で1％未満であることが好ましい。

[0092] (5)図4(e)

基板1をX－Yテーブルに設置して、レーザーダイオード励起YAGレーザーの第2高調波(532nm)を、図の矢印に示すように、光電変換層3の膜面側から入射する。パルス発振:10kHz以上20kHz以下として加工速度に適切となるようにレーザーパワーを調整して、透明導電層2のレーザーエッチングラインの約100μm以上150μm以下の横側を狙い、溝11を形成するようにレーザーエッチングする。レーザーエッチングラインの位置は、逆転していなければ問題ないものであるが、位置決めの公差を考慮して、前記数値を狙ったものである。

[0093] (6)図5(a)

裏面電極層4としてAg膜をスパッタリング装置により減圧雰囲気、約150℃にて順次製膜する。裏面電極層4は本実施形態では、Ag膜を膜厚150nm以上で製膜し、さらにn層と裏面電極層4との接触抵抗低減と光反射向上を目的に、光電変換層3と裏面電極層4との間に膜厚10nm以上のZnO系膜(例えばGZO(Gaドープ ZnO)膜)をスパッタリング装置により製膜して設ける。

[0094] (7)図5(b)

基板1をX－Yテーブルに設置して、レーザーダイオード励起YAGレーザーの第2

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高調波(532nm)を、図の矢印に示すように、基板1側から入射する。レーザー光が光電変換層3で吸収され、このとき発生する高いガス蒸気圧を利用して裏面電極層4が爆裂して除去される。パルス発振:1kHz以上10kHz以下として加工速度に適切となるようにレーザーパワーを調整して、透明導電層2のレーザーエッチングラインの約250μm以上400μm以下の横側を狙い、溝12を形成するようにレーザーエッチングする。レーザーエッチングラインの位置は、逆転していなければ問題ないものであるが、位置決めの公差を考慮して、前記数値を狙ったものである。

[0095] (8)図5(c)

発電領域を区分して、基板端周辺の膜端部においてレーザーエッチングによる直列接続部分が短絡し易い影響を除去する。基板1をX－Yテーブルに設置して、レーザーダイオード励起YAGレーザーの第2高調波(532nm)を、基板1側から入射する。レーザー光が透明導電層2と光電変換層3で吸収され、このとき発生する高いガス蒸気圧を利用して裏面電極層4が爆裂して、裏面電極層4／光電変換層3／透明導電層2が除去される。パルス発振:1kHz以上10kHz以下として加工速度に適切となるようにレーザーパワーを調整して、基板1の端部から5mm以上15mm以下の位置を、X方向絶縁溝15を形成するようにレーザーエッチングする。このとき、Y方向絶縁溝は後工程で基板1周囲領域の膜面研磨除去処理を行うので、設ける必要がない。

絶縁溝15は基板1の端より5mm以上10mm以下の位置にてエッチングを終了させることにより、太陽電池パネル端部からの太陽電池モジュール6内部への外部湿分侵入の抑制に、有効な効果を呈するので好ましい。

[0096] (9)図6(a)

後工程のEVA等を介したバックシートとの健在な接着・シール面を確保するために、基板1周辺(周囲領域14)の積層膜は、段差があるとともに剥離し易いため、この膜を除去する。まず、基板の端から5mm以上20mm以下で、前述の図5(c)工程で設けた絶縁溝15よりも基板端側における裏面電極層4／光電変換層3／透明導電層2において、砥石研磨やブラスト研磨などを用いて除去を行う。研磨屑や砥粒は基板1を洗浄処理して除去した。

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[0097] (10)図6(b)

端子箱取付け部分はバックシートに開口貫通窓を設けて集電板を取出す。この開口貫通窓部分には絶縁材を複数層を設置して外部からの湿分などの浸入を抑制する。

直列に並んだ一方端の太陽電池発電セル5と、他方端部の太陽電池発電セル5とから銅箔を用いて集電して太陽電池パネル裏側の端子箱部分から電力が取出せるように処理する。銅箔は各部との短絡を防止するために銅箔幅より広い絶縁シートを配置する。

集電用銅箔などが所定位置に配置された後に、太陽電池モジュール6の全体を覆い、基板1からはみ出さないようにEVA(エチレン酢酸ビニル共重合体)等による充填材シートを配置する。

EVAの上に、防水効果の高いバックシート21を設置する。バックシート21は本実施形態では防水防湿効果が高いようにPTEシート/AL箔/PETシートの3層構造よりなる。

バックシート21までを所定位置に配置したものを、ラミネータにより減圧雰囲気で内部の脱気を行い約150℃でプレスしながら、EVAを架橋させて密着させる。

[0098] (11)図7(a)

太陽電池モジュール6の裏側24に端子箱を接着剤で取付ける。

[0099] (12)図7(b)

銅箔と端子箱の出力ケーブル23とをハンダ等で接続し、端子箱内部を封止剤(ポッティング剤)で充填して密閉する。これで太陽電池パネル50が完成する。

[0100] (13)図7(c)

図7(b)までの工程で形成された太陽電池パネル50について発電検査ならびに、所定の性能試験を行う。発電検査は、AM1.5、全天日射基準太陽光(1000W/m^2)のソーラシミュレータを用いて行う。

[0101] (14)図7(d)

発電検査(図7(c))に前後して、外観検査をはじめ所定の性能検査を行う。

[0102] 上記実施形態では太陽電池として、トップセルとして非晶質(アモルファス)シリコン

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系光電変換層を有し、ボトムセルとして結晶質(微結晶)シリコン系光電変換層を有するタンデム型太陽電池を用いたものについて説明したが、本発明は、この例に限定されるものではない。

例えば、光電変換層として微結晶シリコンをはじめとする結晶質シリコン系光電変換層のみを有するシングル型太陽電池や、前記トップセルと前記ボトムセルに加えてさらに1層もしくは2層以上の別の光電変換層を設けた多接合型太陽電池のような他の種類の薄膜太陽電池にも同様に適用可能である。

[0103] [実施例及び比較例]

比較例1:

透明電極付き基板として、不連続な複数の山部によるマクロな凹凸(テクスチャ)は形成せず、ミクロの多数の凹凸(テクスチャ)を有する、一層のテクスチャ構造を用いた。ミクロの多数の凸部の底面径が0.2～0.3μm、凸部の高さは0.1～0.2μmであり、高さ／底面径の比が0.7～1.0であった。分光ヘイズ率は、波長550nmにおいて20%、波長800nmでは4%である。一層のテクスチャ構造の透明電極付き基板を用いた以外は、本発明の前記実施形態に従って、タンデム型太陽電池を作製した。

透明電極付き基板上に形成した各層において、トップセルp層は膜厚8nm、トップセルn層は膜厚40nm、ボトムセルp層は膜厚30nm、ボトムセルn層は膜厚30nm、裏面電極のZnO層は膜厚80nm、裏面電極のAg層は膜厚300nmで、各比較例及び実施例において共通とした。本例のトップセルi層、ボトムセルi層の膜厚は、表1に示す通りとし、中間コンタクト層は形成しなかった。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を2μmに設定した本例の太陽電池の発電効率初期値は12.0%だった。なお、このときのボトムセルi層の膜厚は、基板上の太陽電池として構成される領域における膜厚分布を考慮して、その平均値で評価したものである。

なお、表2において、電池性能評価項目であるIsc、Voc、FF、Effは、それぞれ短絡電流、開放電圧、形状因子、発電効率(初期値)を表す。Iscの(a－Si／c－Si)は、分光感度から求めたa－Si(非晶質)トップセルのIsc及びc－Si(結晶系)ボトムセルのIscである。タンデムのIscはトップセルIscとボトムセルIscの低い方で律速される

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。本実施例及び比較例は、ボトムセル律速であり、ボトムセルのIscがタンデムのIscとなっている。また、表2に示す比較例及び実施例において、電池性能評価結果は、比較例1を1とした相対値で記載する。本結果は、劣化前の初期値を記載したが、劣化率は本試験の範囲内では同等と考えられ、相対値で表すなら劣化後も同等である。

[0104] 比較例2:

トップセルi層、中間コンタクト層、ボトムセルi層を表1に示す膜厚で形成した以外は前記比較例1と同様の方法に従って、タンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚250nmとZnO中間コンタクト層の膜厚50nmに対し、ボトムセルi層の膜厚を2μmに設定した本例の太陽電池の発電効率初期値は12.0%だった。

[0105] 比較例3:

トップセルi層、ボトムセルi層を表1に示す膜厚で形成した以外は前記比較例1と同様の方法に従って、タンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を1.5μmに設定した本例の太陽電池の発電効率初期値は10.8%に低下した。これは、発電電流が大幅に低下したためであり、比較例で用いた基板ではボトムセル膜厚が2μmなければ所望の電流が得られないということが分かった。

[0106] 実施例1:

本発明の前記実施形態に従って、タンデム型太陽電池を作製した。透明電極付き基板として、不連続な小山部とミクロの多数の凸部を有する層状のSnO_2を積層したダブルテクスチャ構造の基板(山部の高さ500nm、山部の密度は10μm角に30個)を適用した。本例のトップセルi層、ボトムセルi層の膜厚は、表1に示す通りとし、中間コンタクト層は形成しなかった。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を2μmに設定した本例の太陽電池の発電効率初期値は13.3%に向上できた。これは、ボトムセルの電流を大幅に増大できた効果である。

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本発明においては、ダブルテクスチャ構造の透明電極により、山部による大きな凹凸(マクロな凹凸)と、これよりも小さな凹凸(ミクロな凹凸)とすることにより、大きな凹凸である山部により長波長の光を散乱し、小さな凹凸表面より短波長の光を散乱することができる。このため、透明電極全体として広い波長領域の光において高い光散乱性を達成することができる。また山部による大きな凹凸があるため、太陽電池層の裏面電極にまで大きな凹凸形状が発生する。これにより、裏面電極からの反射光が太陽電池層内で有効に散乱するので、ボトムセルの電流を大幅に増大させることができる。

特に本発明においては、透明電極の山部の高さと密度を制御して太陽電池層の膜厚を最適化したので、長波長の光の散乱を最適化して、結晶質シリコン系半導体からなる光電変換層の発電効率が向上している。

[0107] 実施例2:

トップセルi層、ボトムセルi層を表1に示す膜厚で形成した以外は前記実施例1と同様の方法に従って、実施例2(1)のタンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を1.5μmに設定した本例の太陽電池の発電効率初期値は12.8%であり、比較例1に対し効率向上とボトムセル膜厚の25%薄膜化を同時に達成できた。本実施形態による透明電極付き基板の適用により、実施例1に記載したものと同様な効果によりボトムセルを薄膜化しても高い発電電流が得られ、ボトムセルを薄膜化できたためにVocとFFを向上できたためである。また、ボトムセルi層を薄膜化により、ボトムセルi層が厚かったためにこの製膜時間によって律速されていた光電変換装置の製造時間を大幅に短縮することができる。これにより、高速製膜との相乗効果で光電変換装置の生産性を向上させることができる。

さらに、電池性能のボトムセルi層膜厚依存性を調べるために、前記実施例2(1)のボトムセルi層の膜厚を変えて実施例2(2)～実施例2(5)のタンデム型太陽電池を作製した。各実施例におけるボトムセルi層の膜厚を表1に示す。また、各実施例の太陽電池の電池性能を表2に示す。

実施例2において、ボトムセルi層の膜厚が1.2μm以上2.4μm以下の範囲で、

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比較例1のボトムセルi層膜厚が2μmの場合と同等以上の効率が得られた。ボトムセルi層の膜厚のさらに好ましい範囲は1．5μm以上2μm以下である。

低下するのを抑制でき)VocとFFを向上できたためである。

[0108] 実施例3：

トップセルi層、中間コンタクト層、ボトムセルi層を表1に示す膜厚で形成した以外は前記実施例2(1)と同様の方法に従って、タンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚250nmとZnO中間コンタクト層の膜厚50nmに対し、ボトムセルi層の膜厚を1．5μmに設定した本例の太陽電池の発電効率初期値は12．8％だった。効率向上とボトムセル薄膜化を同時に達成できた。

[0109] 実施例4：

透明電極付き基板の山部の高さを表1に示す値に変えた以外は実施例2(1)と同様の方法に従って、実施例4(1)～実施例4(5)のタンデム型太陽電池を作製し、山部の高さと電池性能の関係を調べた。

得られた太陽電池の電池性能を表2に示す。山部の高さは0．4μm以上0．7μm以下が適正であった。山部の高さが0．4μm以上で高い発電電流が得られ、0．7μmを超えるとVocとFFが著しく低下するためである。

[0110] 実施例5：

透明電極付き基板の山部の密度を表1に示す値に変えた以外は実施例2(1)と同様の方法に従って、実施例5(1)～実施例5(6)のタンデム型太陽電池を作製し、山部の密度と電池性能の関係を調べた。

得られた太陽電池の電池性能を表2に示す。山部の密度が10μm角内に15個以上50個以下のとき、比較例1のi層膜厚2μmの場合と同等以上の効率が得られる。さらに好ましい範囲は10μm角内に20個以上45個以下である。密度が低すぎるとJsc(電流密度)が低下し、高すぎるとJscは飽和しVocとFFが低下して、効率が低下する。

[0111] [表1]

		透明電極付き基板の山部	トップセルi層膜厚	中間層	ボトムセルi層膜厚	ボトムセルm層製膜後ラマン比
比較例1		—	300nm	なし	2μm	6.5
比較例2		—	250nm	50nm	2μm	6.5
比較例3		—	300nm	なし	1.5μm	5.8
実施例1		高さ0.5μm,密度30	300nm	なし	2μm	6.5
実施例2	(1)	高さ0.5μm,密度30	300nm	なし	1.5μm	5.8
	(2)		↑	↑	1μm	6.0
	(3)		↑	↑	1.2μm	5.4
	(4)		↑	↑	1.7μm	6.2
	(6)		↑	↑	2.4μm	6.8
実施例3		高さ0.5μm,密度30	250nm	50nm	1.5μm	5.8
実施例4	(1)	高さ0.4μm,密度30	300nm	なし	1.5μm	5.8
	(2)	高さ0.5μm,密度30	↑	↑	↑	5.8
	(3)	高さ0.6μm,密度30	↑	↑	↑	5.8
	(4)	高さ0.7μm,密度30	↑	↑	↑	5.8
	(5)	高さ0.9μm,密度30	↑	↑	↑	5.8
実施例5	(1)	高さ0.5μm,密度10	300nm	なし	1.5μm	5.8
	(2)	高さ0.5μm,密度15	↑	↑	↑	5.8
	(3)	高さ0.5μm,密度20	↑	↑	↑	5.8
	(4)	高さ0.5μm,密度30	↑	↑	↑	5.8
	(5)	高さ0.5μm,密度45	↑	↑	↑	5.8
	(6)	高さ0.5μm,密度50	↑	↑	↑	5.8

[0112] [表2]

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		電池性能			
		Isc (a-Si/c-Si)	Voc	FF	Eff
比較例1		1 (1/1)	1	1	1
比較例2		1 (1/1)	1	1	1
比較例3		0.89(1/0.89)	1	1	0.89
実施例1		1.15(1/1.15)	0.99	0.97	1.11
実施例2	(1)	1.06(1/1.06)	1.00	1.01	1.07
	(2)	0.80(1/0.80)	1.02	1.04	0.86
	(3)	0.96(1/0.96)	1.01	1.02	0.99
	(4)	1.03(1/1.03)	0.99	1.01	1.03
	(5)	1.13(1/1.13)	0.97	0.92	1.02
実施例3		1.06(1/1.06)	1.00	1.01	1.07
実施例4	(1)	1.00(1/1.00)	1.01	1.01	1.02
	(2)	1.06(1/1.06)	1.00	1.01	1.07
	(3)	1.08(1/1.08)	0.99	0.99	1.06
	(4)	1.10(1/1.10)	0.97	0.96	1.03
	(5)	1.10(1/1.10)	0.92	0.88	0.90
実施例5	(1)	0.93(0.9/0.9)	1.00	0.99	0.92
	(2)	0.99(1/0.99)	1.00	1.00	0.99
	(3)	1.04(1/1.04)	1.00	1.01	1.05
	(4)	1.06(1/1.06)	1.00	1.01	1.07
	(5)	1.06(1/1.06)	0.98	0.98	1.02
	(6)	1.05(1/1.05)	0.97	0.96	0.98

[0113] 第2実施形態

以下に、本発明の第2実施形態について、説明する。

本実施形態において、透明電極つき基板は、大型の凹凸と小型の凹凸が混在する

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ことが望ましく、小型の凹凸(ミクロな凹凸)と大型の凹凸(マクロな凹凸)により、ピッチが0．1μmから1．2μm、高さが0．1μmから1．0μmの凹凸が混在している。ピッチ0．8μm以上の大きな凹凸により800nm以上の長波長の光を拡散、閉じ込めでき、ピッチ0．3μm以下の小さな凹凸により500nm以下の短波長の光も有効に散乱、利用できる。すなわち、大きな凹凸により長波長の光を散乱し、小さな凹凸表面より短波長の光を散乱することができるため、全体として高い光散乱性を達成することができる。また分光ヘイズ率が550nm以上800nm以下の波長で20%以上である。

[0114] 本実施形態においても、透明電極つき基板は、第1実施形態と同様であり、透明電極つき基板は、大型の凹凸(マクロな凹凸)の山部112の平均の高さHa(平坦部上のミクロの凸部の頂部からの高さの平均値)が、0．4μm以上0．7μm以下であり、0．5μm以上0．6μm以下であることがより好ましい。山部の密度は、基板111面の10μm角あたり15以上50以下となり、この平均ピッチPaは、1．0μm以上3μm以下に相当する。一方、小型の凹凸(ミクロな凹凸)のミクロの多数の凸部の底面径が0.1μm以上0.3μm以下であり、高さ／底面径の比が0.7以上1.2以下である。

[0115] 前記透明電極付き基板におけるこのような表面性状は、例えば、前記第1実施形態で説明した表面形状の解析を行うことにより確認することができる。

[0116] また、このような形状及び構成を有する透明電極付き基板は、基板全体において、550nm以上800nm以下の波長における分光ヘイズ率が20%以上、好ましくは30%以上であることが好ましい。

ここで、「分光ヘイズ率」の定義は、上記第1実施形態において説明したとおりである。

[0117] 以下に、上述した本実施形態の透明電極付き基板の形状及び構成ならびに特性を満たす基板(透明基板)及び酸化物は、それぞれ前記第1実施形態で説明した基板および第1酸化物と同様であるので、これらの詳しい説明は省略する。

[0118] 本実施形態の透明電極付き基板は、大型の凹凸と小型の凹凸が混在することが望ましく、ピッチが0.1μmから1.2μm、高さが0.1μmから1．0μmの凹凸が混在している。ピッチ0.8μm以上の大きな凹凸により800nm以上の長波長の光を拡散、閉じ込めでき、ピッチ0.3μm以下の小さな凹凸により500nm以下の短波長の光も有効

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に散乱、利用できる。また、膜全体のシート抵抗が8Ω／□以上20Ω／□以下であることが好ましく、8Ω／□以上12Ω／□以下であることがより好ましく、550nmにおける透過率(透明性)は、浸液法で測定した場合、80%以上90%以下であることが好ましく、85%以上90%以下であることがより好ましい。

[0119] また、本実施形態の透明電極付き基板を、光電変換装置の透明電極に用いると、基板を経て入射された光は、透明電極により屈折、散乱されて光電変換部に入射し、光電変換部中を長い距離にわたって通過する。その結果、多くの光が光電変換部にて吸収され、光電変換効率が向上する効果を奏するものとなる。特に、太陽電池に用いた場合には、開放電圧及び曲線因子を低下させずに短絡電流を高く維持することが可能となるため、光電変換効率が向上するものとなる。

[0120] 本実施形態の光電変換装置の製造方法により製造される光電変換装置の構成および太陽電池パネルの製造方法は、後述の異相遮断層または異相防止層を設けたこと以外は前記第1実施形態と同様であるので、第1実施形態で用いた図1および図4ないし図7を参照する。前記第1実施形態と共通の部材については同一の参照符号を用いることとし、詳細な説明は省略する。

[0121] 本実施形態の光電変換装置においては、非晶質シリコン系半導体を主として有する光電変換層からなる第1セル層(トップ層)91の透明電極層側表面から裏面電極層側表面に貫通する異相を遮断または防止するために、後述の光電変換装置の製造方法に係る実施形態に示した方法により、第1セル層(トップ層)91中に異相遮断層(図示略)が設けられるか、もしくは、基板1と第1セル層(トップ層)91の間に異相防止層(図示略)が設けられる。

第1セル層(トップ層)91及び結晶質シリコン系半導体を主として有する光電変換層からなる第2セル層(ボトム層)92の間には、透明導電膜からなる中間コンタクト層93を設けても良い(但し、本発明の光電変換装置は、中間コンタクト層93を設けたものに限定されない)。

[0122] 本実施形態の太陽電池パネルの製造方法においては、まず、前記第1実施形態の図4の(a)および(b)と同様の方法を行い、透明電極基板が形成される。

[0123] 次に、製膜した透明電極層2の表面に対してイオン処理を行い、本実施形態の異

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相防止層を形成することができる。イオン処理は、例えば真空中でのアルゴンイオン照射によるイオンエッチングとすることができる。イオン処理に用いられる装置としては、フィラメントタイプのイオン源を使用したイオンミリング装置が挙げられる。この装置を用いてイオン処理を行う場合は、例えば容器内を10^{-4}Pa台に真空排気し、アルゴンガスを供給して5×10^{-3}Paの条件で、Arイオンを発生させ、加速電圧1kVでイオン照射してイオン処理を行うことができる。イオンは透明電極付き基板の透明電極層2表面に垂直に照射することが好ましい。照射時間は例えば180sec程度とすることができる。

[0124] 次に、前記第1実施形態の図4の(e)と同様の方法により透明電極膜のレーザーエッチングを行い、次いで異相遮断層または異相防止層を設けたこと以外は図4の(d)と同様の方法を行い、光電変換層3を形成する。

光電変換層3の第1セル層(トップ層)91として、非晶質シリコン薄膜からなるp層膜／i層膜／n層膜を順次形成する。太陽光の入射する側からp層、i層、n層がこの順で積層される。

なお、第1セル層91を製膜する前に、透明電極付き基板を真空容器で10^{-1}Pa以下の圧力とし、ヒータで100℃以上の温度に予備加熱(ベーキング)することが、異相の発生を防ぐために特に好ましい。

[0125] 本実施形態において、第1セル層91のp層は、SiH_4, H_2, CH_4, B_2H_6ガスをRFプラズマで反応生成させた、非晶質のBドープSiC膜であり、膜厚は4nm以上16nm以下とすることが好ましい。

[0126] また本実施形態において、第1セル層91のi層は、標準構成としては非晶質Si膜であり、SiH_4とH_2をRFプラズマで反応生成される。膜厚は100nm以上400nm以下とすることが好ましい。標準の製膜条件として、SiH_4とH_2を1:5の比率で供給して圧力を600Paに制御し、60MHzの高周波0．15W／cm^2で放電して、非晶質のi層を製膜することができる。この標準の製膜条件における製膜速度は、例えば1．1nm／sとすることができる。

[0127] 本実施形態の異相遮断層として、第1セル層91のi層中に、標準製膜条件よりも低パワーで製膜された層(例えば、i層製膜の初期に製膜される初期層、あるいはi層製

膜の後期に製膜される後期層）を設けてもよい。このような層を製膜する場合は、高周波出力を例えば0．02W／cm^2の低パワーにして、低速で製膜すればよい。製膜速度は例えば0．2nm／s程度である。初期層及び後期層は、例えば60s（膜厚12nm相当）～120s（膜厚24nm相当）で製膜される。初期層または後期層を設けたi層は、プラズマ放電中にパワーを変更することにより、連続膜として形成される。

[0128] また本実施形態において、第1セル層91（トップ層）のn層は、標準構成としては結晶質（結晶成分を含む）のSi膜であり，SiH_4，H_2，PH_3ガスをRFプラズマで反応生成される。このn層単膜のラマン比は2以上であり、膜厚は10nm以上80nm以下とすることが好ましい。標準の製膜条件として、SiH_4とH_2とPH_3を1：80：0．02の比率で供給して圧力を100Paに制御し、基板と電極の間の間隔を20mmとし、60MHzの高周波0．3W／cm^2で放電して、微結晶（結晶とアモルファスが混在する膜質）のn層を製膜することができる。製膜速度は0．2nm／sとすることができる。製膜速度は例えば0．2nm／s程度とすることができる。

[0129] 本実施形態の異相遮断層として非晶質（結晶成分は存在しない）のn層を形成してもよい。この場合は、前記結晶質のn層の前に非晶質のn層が製膜される。この非晶質n層は、SiH_4とH_2とPH_3を1：1：0．05の比率で供給して圧力を20Paに制御し、基板と電極の間の間隔を20mmとし、60MHzの高周波を0．04W／cm^2で放電して製膜される。製膜速度は例えば0．2nm／s程度とすることができる。非晶質Si－n層と微結晶Si－n層を積層するときは、一旦放電を停止して流量／圧力を変更し、安定後再度放電させて行われる。例えば、非晶質Si製膜条件で15nm程度製膜し、さらに標準の結晶質製膜条件で25nm程度製膜すればよい。

[0130] 本実施形態の異相遮断層として、結晶質（結晶成分を含む）のn層を標準製膜条件より高圧で製膜してもよい。この場合は、例えば、SiH_4とH_2とPH_3を1：80：0．02の比率で供給して、圧力を200Paに制御し、基板と電極の間の間隔を標準条件の1／2である10mmに狭くして、60MHzの高周波を出力0．1W／cm^2で放電して、微結晶Si（結晶とアモルファスが混在する膜質）のn層を製膜することができる。

[0131] 本実施形態において，前記p層膜とi層膜の間には界面特性の向上のためにバッファー層（図示略）を設けてもよい。バッファー層として、バンドギャップが中間の物質を

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挿入することにより、p層(SIC膜)とi層(Si膜)の界面でのバンド不整合を抑制することができる。

本実施形態において、p層の製膜ガス(SiH_4、H_2、CH_4、B_2H_6)に対し、i層ではSiH_4及びH_2しか用いないため、ドーパント(B_2H_6)濃度及びバンド調整のためのCH_4濃度を調整する。具体的には、p層製膜室において、B_2H_6ガスの供給を停止し、B_2H_6の供給は壁面吸着量のみとし、CH_4ガスの供給量をp層に対し1/10～1/3に調整することで0.02～0.1μmの膜厚のバッファー層を形成した。これにより、p層及びi層と原子拡散が進行した結果、膜厚方向の炭素含有率及びバンドエネルギー構造は滑らかに変化する状態となり、p層とi層との界面特性が向上されることとなる。

[0132] 次に、第1セル層(トップ層)91の上に、前記第1実施形態と同様の方法、製膜条件により、微結晶シリコン薄膜からなる微結晶p層膜／微結晶i層膜／微結晶n層膜を順次製膜し、前記第1実施形態と同様の第2セル層(ボトム層)92を形成する。

[0133] 前記第1実施形態と同様に、第1セル層(トップ層)91と第2セル層(ボトム層)92の間に電流整合性を取るために半反射膜となることを目的に、中間コンタクト層93として、膜厚0nm以上90nm以下、より好ましくは5nm以上50nm以下のZnO系膜(例えばGZO(Gaドープ ZnO)膜)をスパッタリング装置により製膜して設けても良い。この中間コンタクト層93は、ZnO単膜での光吸収率がλ＝450nm以上1000nm以下の範囲で1%未満であることが好ましい。

[0134] 第2セル層92を形成した後、第1実施形態における図4の(e)から図7の(b)と同様の方法により太陽電池パネル50が完成する。次いで第1実施形態における図7の(c)および(d)と同様の方法により、発電検査および所定の性能試験ならびに外観検査をはじめ所定の性能検査を行う。

[0135] 上記実施形態では太陽電池として、トップセルとして非晶質シリコン系光電変換層を有し、ボトムセルとして結晶質(微結晶)シリコン系光電変換層を有するタンデム型太陽電池を用いたものについて説明したが、本発明は、この例に限定されるものではない。

例えば、光電変換層として非晶質シリコン系光電変換層のみを有するシングル型太陽電池や、前記トップセルと前記ボトムセルに加えてさらに1層もしくは2層以上の

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別の光電変換層を設けた多接合型太陽電池のような他の種類の薄膜太陽電池にも同様に適用可能である。

[0136] [実施例、参考例及び比較例]

参考例1:

透明電極付き基板として、微細な凹凸のみのものを用いた。微細な凹凸の凸部の高さは0.1μm以上0.2μm以下、ピッチは0.1μm以上0.3μm以下、凸部の高さと底面径の比は0.7～1.0、波長550nmの分光ヘイズ率は20%、800nmの分光ヘイズ率は3%であった。透明電極付き基板が異なる以外は、本発明の前記実施形態における標準の製膜条件に従って、タンデム型太陽電池を作製した。

[0137] 透明電極付き基板上に形成した各層において、トップセルp層は膜厚8nm、トップセルn層は膜厚40nm、ボトムセルp層は膜厚30nm、ボトムセルn層は膜厚30nm、裏面電極のZnO層は膜厚80nm、裏面電極のAg層は膜厚300nmで、各参考例、比較例及び実施例において共通とした。本例のトップセルi層、トップセルn層の膜厚及び製膜条件は、表3に示す通りとし、中間コンタクト層は形成しなかった。

[0138] なお、表3に記載した各参考例、比較例及び実施例の「製膜条件」とは、以下の通りである。

トップセルi層の標準製膜条件: SiH_4とH_2を1:5の比率で供給して、圧力を600Paに制御し、60MHzの高周波を出力0.15W／cm^2で放電して、非晶質i層を製膜した。製膜速度は1.1nm／sとした。

[0139] トップセルi層の初期層または後期層の低速製膜条件: 標準条件と高周波出力のみを変更し、0.02W／cm^2とした。製膜速度は0.2nm／sとした。標準製膜条件による膜との積層は、プラズマ放電中にパワーを変更することにより、連続膜とした。

[0140] トップセルn層の標準製膜条件: SiH_4とH_2とPH_3を1:80:0.02の比率で供給して、圧力を100Paに制御し、基板と電極の間の間隔を7mmとし、60MHzの高周波を出力0.3W／cm^2で放電して、微結晶(結晶と非晶質が混在する膜質)のn層を製膜した。製膜速度は0.2nm／sとした。

[0141] トップセルn層の非晶質Si製膜条件: SiH_4とH_2とPH_3を1:1:0.05の比率で供給して、圧力を20Paに制御し、基板と電極の間の間隔を7mmとし、60MHzの高周波

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を出力0．04W／cm^{2}で放電して、非晶質Si(結晶成分は存在しない)のn層を製膜した。製膜速度は0．2nm／sとした。非晶質Si－n層と微結晶Si－n層を積層するときは、一旦放電を停止して流量／圧力を変更し、安定後再度放電させた。

[0142] トップセルn層の高圧製膜条件：SiH_4とH_2とPH_3を1:80:0．02の比率で供給して、圧力を200Paに制御し、基板と電極の間の間隔を標準条件の1／2である10mmに狭くして、60MHzの高周波を出力0．3W／cm^{2}で放電して、微結晶Si(結晶と非晶質が混在する膜質)のn層を製膜した。

[0143] 参考例1で得られた太陽電池の電池性能を表4に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を2μmに設定した本例の太陽電池の発電効率(初期値)は12%だった。

なお、表4において、電池性能評価項目であるIsc、Voc、FF、Effは、それぞれ短絡電流、開放電圧、形状因子、発電効率(初期値)を表す。また、表4に示す参考例、比較例及び実施例において、電池性能評価結果は、参考例1を1とした相対値で記載する。本結果は、劣化前の初期値を記載したが、劣化率は本試験の範囲内では同等と考えられ、相対値で表すなら劣化後も同等である。

[0144] 参考例2：

トップセルi層、ボトムセルi層を表3に示す膜厚で形成した以外は前記参考例1と同様の方法に従って、タンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表4に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を1．5μmに設定した本例の太陽電池の発電効率は10．8%に低下した。これは、発電電流が大幅に低下したためであり、参考例で用いた基板ではボトムセル膜厚が2μmなければ所望の電流が得られないということが分かった。

[0145] 比較例4：

本発明の前記実施形態における標準の製膜条件に従って、タンデム型太陽電池を作製した。透明電極付き基板として、実施例6と同じく大小の凹凸が混在する基板を適用した。本例のトップセルi層、トップセルn層の膜厚及び製膜条件は、表3に示す通りとし、中間コンタクト層は形成しなかった。すなわち、トップセルi層は製膜速度1．

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1nm／sで300nmの膜厚に、トップセルn層は結晶と非晶質が混在する微結晶となる条件で40nmの膜厚に製膜した。ボトムセルi層の膜厚は1．5μmとした。

[0146] 得られた太陽電池の電池性能を表4に示す。表4に示したように、本例の太陽電池は、電流は増大したものの、開放電圧と形状因子が低下して、発電効率初期値は参考例1のボトムセルi層膜厚が2μmの場合より低下していた。

[0147] 比較例4の太陽電池において開放電圧と形状因子が低下した原因を調査検討した。図10に大小の凹凸が混在する透明電極付き基板を用いて作製したタンデム型太陽電池の断面の透過型電子顕微鏡写真を示す。この電子顕微鏡写真において、透明電極の谷の部分（点線で囲んだ部分）でトップセルを上下に貫通する線が見える。これは、下地の隣接する面に製膜・成長する膜成長相間の不連続な境界が線状に見えるもので、異相と呼んでおり、キャリア再結合中心が集中すると考えられ、電流リーク箇所に相当する。この異相が生じた場合に開放電圧と形状因子が低下していた。従って、本発明者らは、この異相を抑制すること、または完全に抑制はできなくても透明電極から中間コンタクト層又はボトムセルに至るまでトップセルを貫通する異相を遮断できれば、開放電圧低下、形状因子低下を抑制できると考えた。

[0148] 実施例6～実施例9:

トップセルi層、トップセルn層の膜厚及び製膜条件を表3に示す通りとした以外は前記比較例4と同様の方法に従って、実施例6～実施例9のタンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表4に示す。

[0149] 実施例6においては、トップセルの非晶質Si－i層を製膜初期（p層との界面）のみ低パワーで製膜することにより、開放電圧低下、形状因子低下を抑制し、太陽電池性能を向上できた。これは、非晶質Si－i層の初期層によってトップセルを貫通する異相が遮断され、電流リークを抑制することができたためと考えられる。ボトムセルが膜厚1．5μmという薄膜で発電効率初期値13.0%という高効率が得られたことは、生産性と効率向上の両方で非常に大きな成果である。

[0150] 実施例7においては、トップセルの非晶質Si－i層を製膜後期（n層との界面）のみ低パワーで製膜することにより、開放電圧低下、形状因子低下を抑制し、太陽電池

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性能を向上できた。これは、非晶質Si－i層の後期層によってトップセルを貫通する異相が遮断され、電流リークを抑制することができたためと考えられる。この実施例7でも、ボトムセルが膜厚1．5μmという薄膜で発電効率初期値13.0%という高効率が得られたことは、生産性と効率向上の両方で非常に大きな成果である。

[0151] 実施例8においては、トップセルn層の製膜後期のみを標準製膜条件により製膜して結晶質とし、製膜初期の層を非晶質にすることで、開放電圧低下、形状因子低下を抑制し、太陽電池性能を向上できた。これは、トップセルn層において非晶質とした初期層がi層との界面で異相を埋めるため、トップセルを貫通する異相が遮断され、電流リークを抑制することができたためと推察される。ボトムセル膜厚1.5μmの薄膜で発電効率初期値13.2%が得られたのは、実施例6、実施例7と同様の異相遮断効果と、更にn層による界面改善効果が得られたためである。

[0152] 実施例9においては、トップセルn層を200Paの高圧で製膜して微結晶膜を形成することにより、開放電圧低下、形状因子低下を抑制し、太陽電池性能を向上できた。なお、実施例9において、トップセルn層の製膜の際の圧力を400Paとした場合も同様の効果が得られた。これは、高圧で製膜することによりトップセルn層がi層との界面の谷の部分に付きやすくなり、これによってトップセルを貫通する異相が遮断され、電流リークを抑制することができたためと考えられる。

[0153] [表3]

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	トップセルi層の製膜条件と膜厚	トップセルn層の製膜条件と膜厚
参考例1	標準製膜条件で300nm	標準製膜条件で2μm
参考例2	標準製膜条件で300nm	標準製膜条件で1.5μm
比較例4	標準製膜条件で300nm	標準製膜条件(結晶質)で40nm
実施例6	初期層：低速製膜条件で24nm(120s)；続けて標準製膜条件で残り276nm	標準製膜条件(結晶質)で40nm
実施例7	標準製膜条件で276nm；さらに後期層として低速製膜条件で24nm(120s)	標準製膜条件(結晶質)で40nm
実施例8	標準製膜条件で300nm	非晶質Si製膜条件で15nm；さらに標準製膜条件で25nm
実施例9	標準製膜条件で300nm	高圧製膜条件(結晶質)で40nm

[0154] 実施例10:

透明電極付き基板の透明電極表面に対してイオン処理を行った以外は、前記比較例4と同様の方法に従って、実施例10のタンデム型太陽電池を作製した。

イオン処理は、真空中でのアルゴンイオン照射によるイオンエッチングであり、装置としては、フィラメントタイプのイオン源を使用したイオンミリング装置を用いた。容器内を10^{-4}Pa台に真空排気し、アルゴンガスを供給して5×10^{-3}Paの条件で、Arイオンを発生させ、加速電圧1kVでイオン照射してイオン処理を行った。イオンは透明電極付き基板の透明電極表面に垂直に照射し、照射時間は180secとした。図8は、イオン処理前における透明電極付き基板の透明電極表面の電子顕微鏡写真(倍率5万倍)であり、図9は、イオン処理後における透明電極付き基板の透明電極表面の電子顕微鏡写真(倍率5万倍)である。

[0155] 得られた太陽電池の電池性能を表4に示す。なお、表4において、電池性能評価項目であるIsc、Voc、FF、Effは、それぞれ短絡電流、開放電圧、形状因子、発電効率を表す。Iscの(a－Si／c－Si)は、分光感度から求めたa－Si(非晶質)トップセルのIsc及びc－Si(結晶系)ボトムセルのIscである。

実施例10においては、前記イオン処理により、開放電圧低下、形状因子低下を抑

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制し、太陽電池性能を向上できた。これはイオン処理によって基板の凹形状が円滑になり、トップセルにおける異相の形成が抑制されたため、電流リークを抑制することができたためと考えられる。

実施例1～10においては、ボトムセルi層製膜条件は固定であり、ボトムセルn層製膜後のラマン比は表1に示すとおり、5.0～7.0の間にあった。

[0156] 実施例11；

ボトムセルi層のH_2/SiH_4希釈率比を表5に示すように変えた以外は、実施例1と同様の方法に従って実施例11(1)～実施例11(6)のタンデム型太陽電池を作製し、ボトムセルのn層製膜後のラマン比と太陽電池特性の関係を調べた。その結果を図12に示す。なお、表5、及び図12において、H_2希釈率比、及び電池性能結果は、比較例1を1とした場合の相対値である。本結果は、劣化前の初期値を記載したが、劣化率は本試験の範囲内では同等と考えられ、相対値で表すなら劣化後も同等である。

表5及び図12からわかるように、n層製膜後のラマン比でみて3.0以上8.0以下のとき、比較例1よりも太陽電池性能が向上している。これは、ラマン比が3.0より低下するとVocが向上する一方で、Iscが著しく低下していることから、非晶質成分が多すぎて抵抗損失が生じたと推定される。ラマン比が8.0より増大すると、VocとFFが大きく低下していることより電流リークによる電圧損失が生じたと考えられ、結晶粒界の電流リークが想定される。第2セル層において、適度な非晶質相が存在することにより、結晶質シリコンの粒界に存在する欠陥を不活性にし、これにより、Iscの低下を抑制することに寄与しているものと考えられる。

また、図12において、H_2希釈率比0．9でEffの上昇が緩和し、H_2希釈率比1．1でEffが低下している。H_2希釈率比0．9以上1．1以下でのEff値は、実施例11(3)～実施例11(5)に示すように、比較例1に対し1.1倍以上の性能を得ることができた。したがって、ラマン比は、H_2希釈率比と電池性能との相関関係からみて、実験的に5.0以上7.5以下が最適値となる。

[0157] [表4]

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	電池性能			
	Isc (a-Si/c-Si)	Voc	FF	Eff
参考例1	1 (1/1)	1	1	1
参考例2	0.89(1/0.89)	1	1	0.89
比較例4	1.10(1/1.10)	0.95	0.92	0.97
実施例6	1.10(1/1.10)	0.99	0.99	1.08
実施例7	1.10(1/1.10)	0.99	0.99	1.08
実施例8	1.10(1/1.10)	1.00	1.00	1.10
実施例9	1.10(1/1.10)	0.99	0.98	1.07
実施例10	1.03(1/1.03)	1.01	1.01	1.05

[0158] [表5]

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No	H2 希釈率比	ラマン比	電池性能				
			(タンデム) Isc	(c-Si) Isc	Voc	FF	Eff
実施例11(1)	0.8	2	0.98	0.98	1.03	0.95	0.96
実施例11(2)	0.8	3	1.03	1.03	1.01	1.00	1.04
実施例11(3)	0.9	5	1.11	1.11	1.00	0.99	1.10
実施例11(4)	1.0	6.5	1.15	1.15	0.99	0.97	1.11
実施例11(5)	1.1	7.5	1.17	1.17	0.98	0.96	1.10
実施例11(6)	1.2	10	1.15	1.15	0.94	0.89	0.96
比較例1	1.0	6.5	1.00	1.00	1.00	1.00	1.00(12%)

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[0159] 以上、実施例6から実施例11によれば、分光ヘイズ率を高めた透明電極付き基板を適用しても開放電圧と形状因子の低下を抑制でき、薄いボトムセルで、高効率と高生産性を兼ね備えたタンデム太陽電池を作製可能となった。

なお、トップセル(非晶質Si層)全体を低パワーで製膜すると製膜速度が著しく低下するため、生産性が悪化する。しかし、上記実施例6、実施例7のように初期あるいは後期の20%程度の膜厚を低速で作製するだけであれば、生産性の悪化を極力抑えられて、高い生産効率で太陽電池を製造できる。また、実施例9のようにn層の製膜条件を改善した場合は、生産性の悪化はまったくなく、高い生産効率で太陽電池を製造できる。

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請求の範囲

[1] 透明絶縁性の基板上に透明電極層を設けてなる透明電極付き基板と、該透明電極付き基板の透明電極層側に順次形成された、結晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも有してなる光電変換装置であって、

前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上であり、

前記結晶質シリコン系半導体を主として有する光電変換層の膜厚が1.2μm以上2μm以下、かつラマン比が3.0以上8.0以下である光電変換装置。

[2] 前記透明電極付き基板と前記結晶質シリコン系半導体を主として有する光電変換層との間に、非晶質シリコン系半導体を主として有する光電変換層を有する請求項1に記載の光電変換装置。

[3] 前記非晶質シリコン系半導体を主として有する光電変換層と前記結晶質シリコン系半導体を主として有する光電変換層との間に中間コンタクト層を有する請求項2に記載の光電変換装置。

[4] 前記透明電極付き基板の透明電極層表面が、複数の山部と複数の平坦部とで構成され、該山部及び該平坦部の表面がミクロの多数の凸部を連続して有してなり、

前記山部の前記基板面垂直方向における高さが0.4μm以上0.7μm以下であり、

基板面10μm角における前記山部の数が15以上50以下であり、

前記ミクロの多数の凸部の底面径が0.1μm以上0.3μm以下であり、高さ／底面径の比が0.7以上1.2以下である請求項1から請求項3のいずれか1項に記載の光電変換装置。

[5] 透明絶縁性の基板上に透明電極層を形成して透明電極付き基板を作製し、

該透明電極付き基板の透明電極層側に非晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも順次形成する光電変換装置の製造方法であって、

前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘ

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イズ率が550nm以上800nm以下の波長で20%以上であり、

前記非晶質シリコン系半導体を主として有する光電変換層中に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相を遮断する異相遮断層を形成する光電変換装置の製造方法。

[6] 前記非晶質シリコン系半導体を主として有する光電変換層の形成においてp層、i層、n層を順次形成し、

前記i層の形成において該i層の他の部分より低速で製膜することにより前記異相遮断層を形成する、請求項5に記載の光電変換装置の製造方法。

[7] 前記非晶質シリコン系半導体を主として有する光電変換層の形成においてp層、i層、n層を順次形成し、

前記n層の形成において少なくともその一部に非晶質の層を形成することにより前記異相遮断層を形成する、請求項5に記載の光電変換装置の製造方法。

[8] 前記非晶質シリコン系半導体を主として有する光電変換層の形成においてp層、i層、n層を順次形成し、

前記n層の形成において少なくともその一部を200Pa以上の圧力下で製膜することにより前記異相遮断層を形成する、請求項5に記載の光電変換装置の製造方法。

[9] 透明絶縁性の基板上に透明電極層を形成して透明電極付き基板を作製し、

該透明電極付き基板の透明電極層側に非晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも順次形成する光電変換装置の製造方法であって、

前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上であり、

前記透明電極層の形成と前記光電変換層形成の間に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相の形成を防止する異相防止層を形成する光電変換装置の製造方法。

[10] 前記透明電極層の凸部を円滑化して前記異相防止層を形成する、請求項9に記載の光電変換装置の製造方法。

[11] 前記透明電極層表面にイオン処理を施して前記異相防止層を形成する、請求項9

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または請求項10に記載の光電変換装置の製造方法。

[12] 前記非晶質シリコン系半導体を主として有する光電変換層と前記裏面電極の間に、結晶質シリコン系半導体を主として有する光電変換層を形成する請求項5から請求項11のいずれか1項に記載の光電変換装置の製造方法。

[13] 透明絶縁性の基板上に透明電極層を設けてなる透明電極付き基板と、該透明電極付き基板の透明電極層側に順次形成された、非晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも有し、

前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上である光電変換装置であって、

前記非晶質シリコン系半導体を主として有する光電変換層中に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相を遮断する異相遮断層を設けた光電変換装置。

[14] 前記非晶質シリコン系半導体を主として有する光電変換層において、p層、i層、n層が順次形成され、

前記非晶質シリコン系半導体を主として有する光電変換層のn層が非晶質シリコン系半導体を主として有する層と、結晶質シリコン系半導体を主として有する層で形成される請求項2又は13に記載の光電変換装置。

[15] 前記非晶質シリコン系半導体を主として有する光電変換層のp層とi層との間にバッファー層を設けた請求項2、13又は14に記載の光電変換装置。

[16] 前記非晶質シリコン系半導体を主として有する光電変換層と前記裏面電極層との間に結晶質シリコン系半導体を主として有する光電変換層を有する請求項13に記載の光電変換装置。

[17] 前記結晶質シリコン系半導体を主として有する光電変換層の膜厚が1.2μm以上2μm以下、かつラマン比が3.0以上8.0以下である請求項16に記載の光電変換装置。

[18] 前記非晶質シリコン系半導体を主として有する光電変換層と前記裏面電極の間に、結晶質シリコン系半導体、結晶質もしくは非晶質シリコンゲルマニウム系半導体を

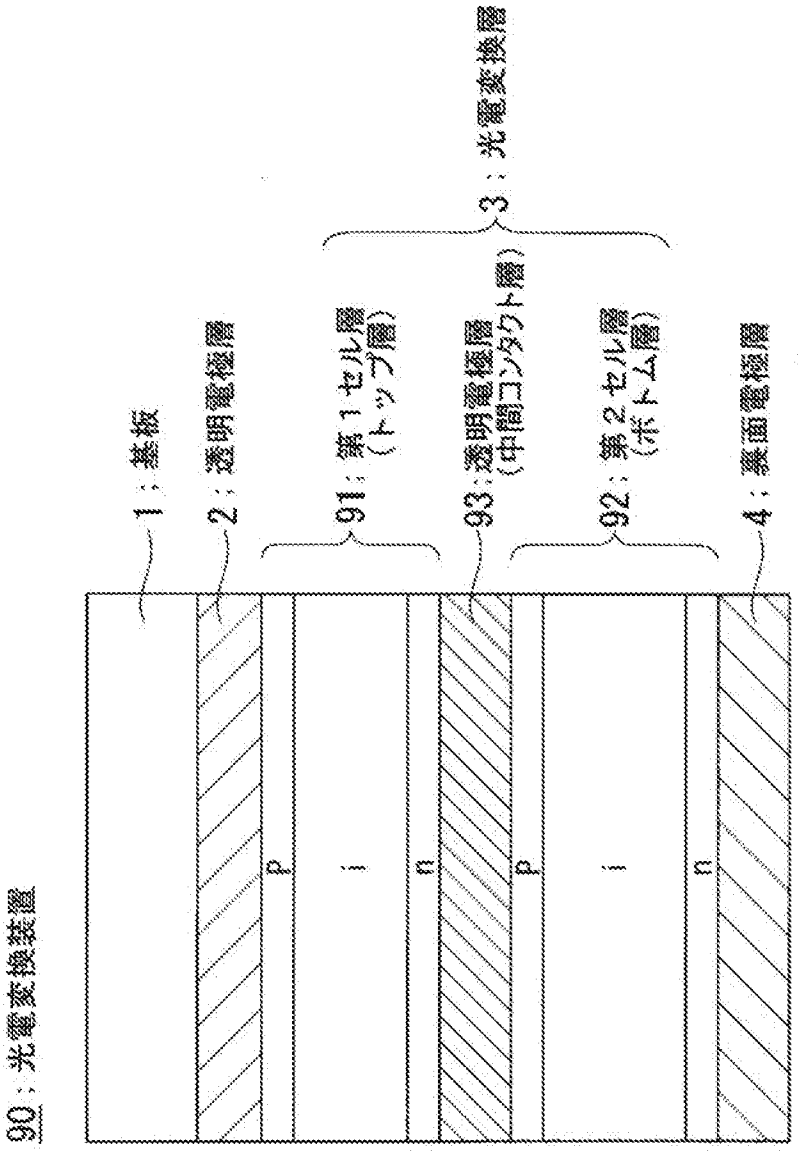
SAMSUNG EX. 1002 - 1153/2862

主として有する光電変換層を有する請求項13に記載の光電変換装置。

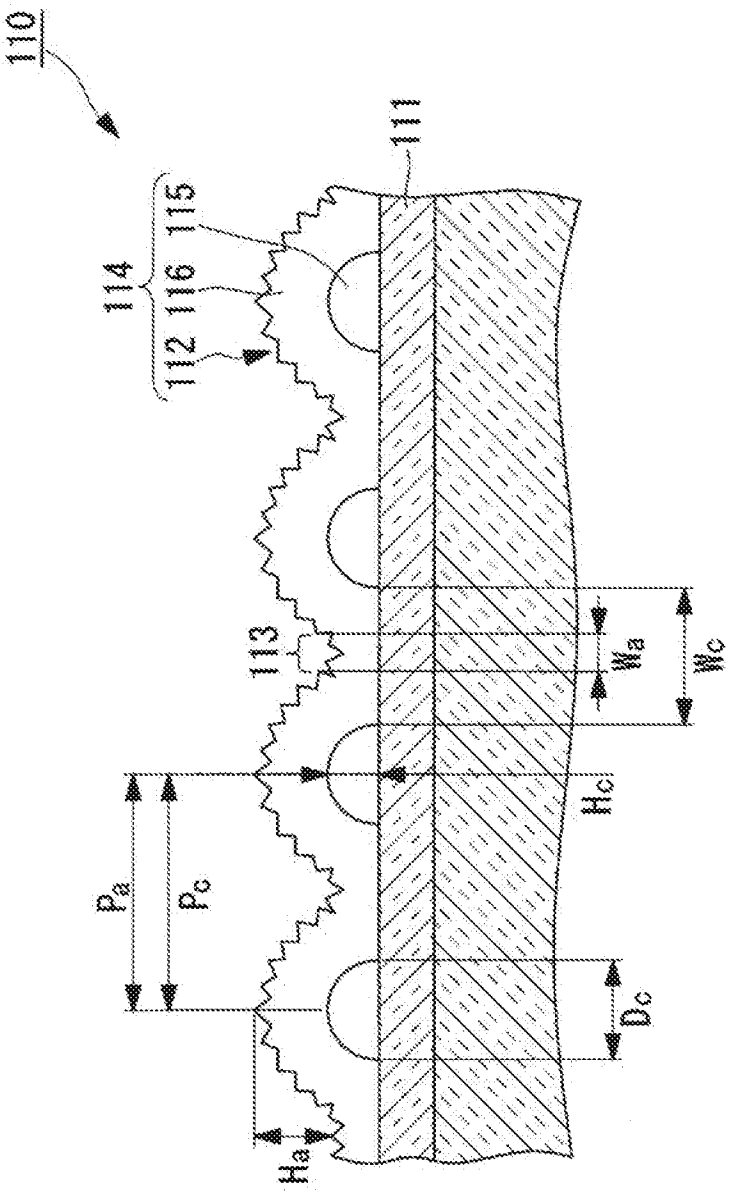
[19] 前記非晶質シリコン系半導体を主として有する光電変換層と前記裏面電極の間に、結晶質もしくは非晶質シリコン系半導体、結晶質もしくは非晶質シリコンゲルマニウム系半導体を主として有する光電変換層を複数有する請求項13に記載の光電変換装置。

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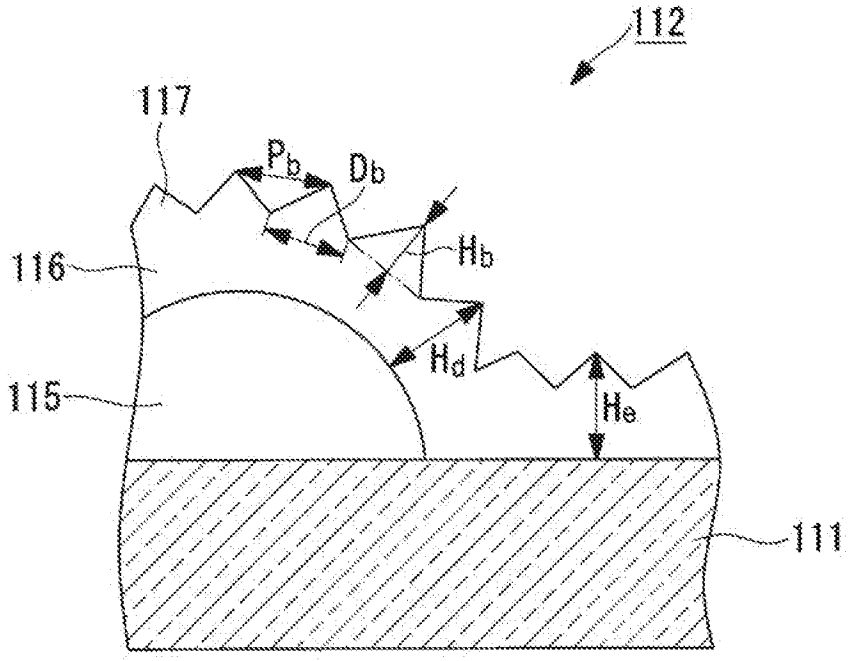
[図1]


90；光電変換装置
1；基板
2；透明電極層
91；第１セル層
（トップ層）
93；透明電極層
（中間コンタクト層）
92；第２セル層
（ボトム層）
4；裏面電極層
3；光電変換層
p
i
n
p
i
n

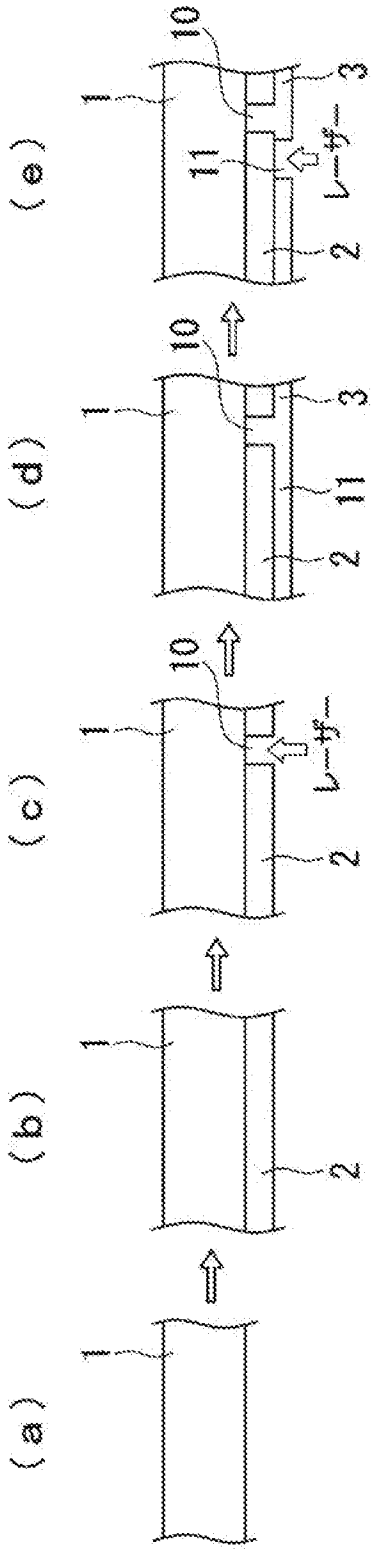
[図2]



[図3]

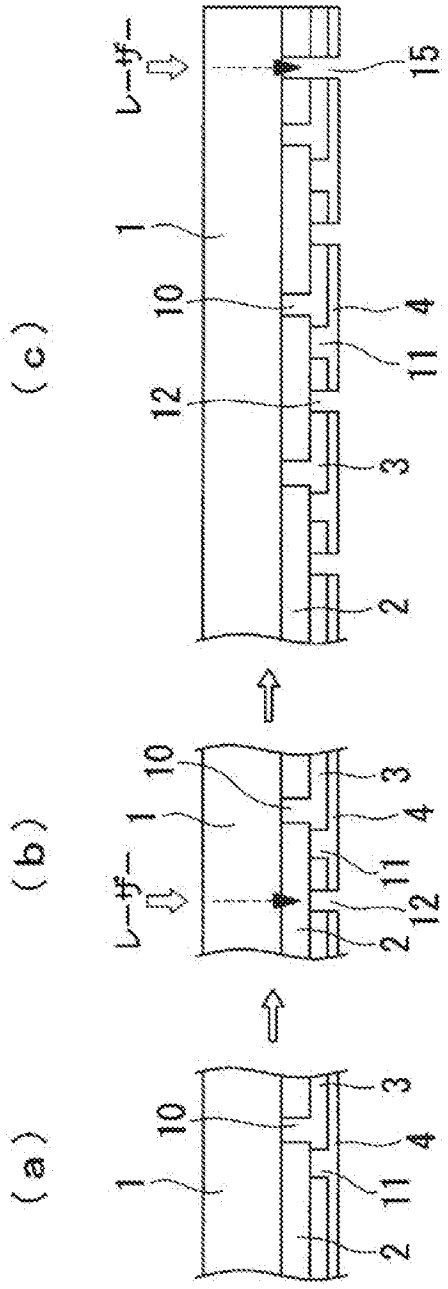


[図4]

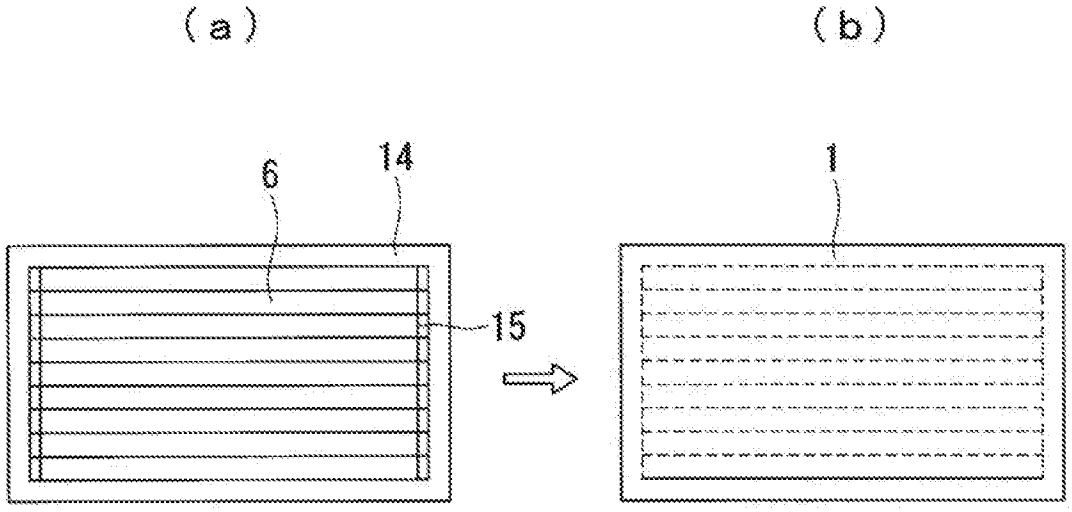


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[図5]

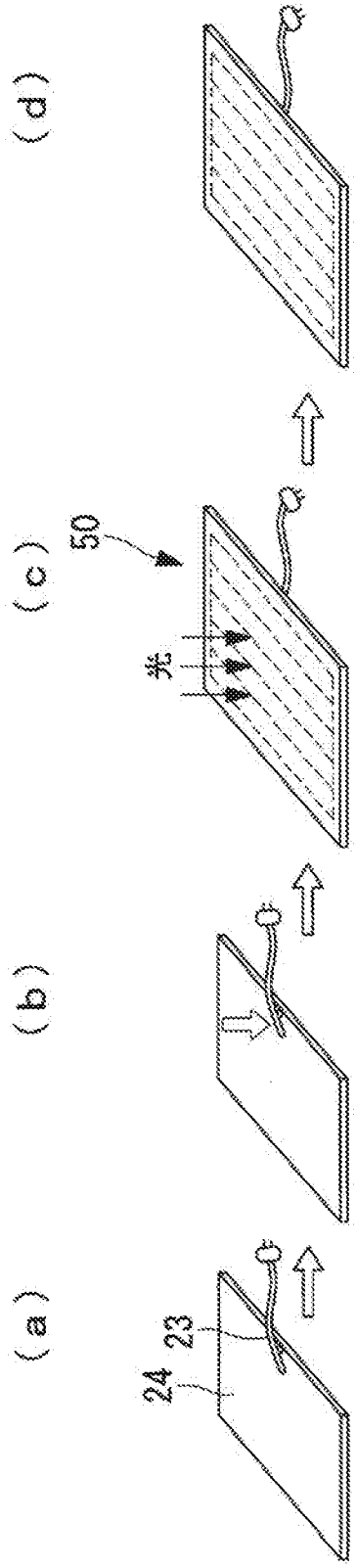


[図6]

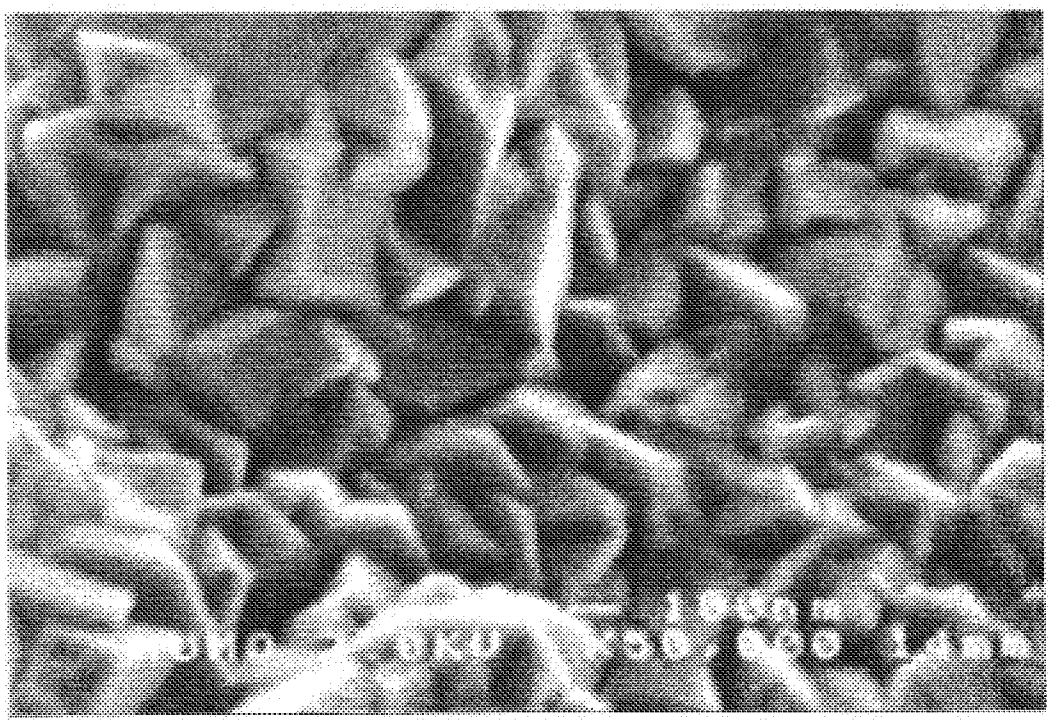


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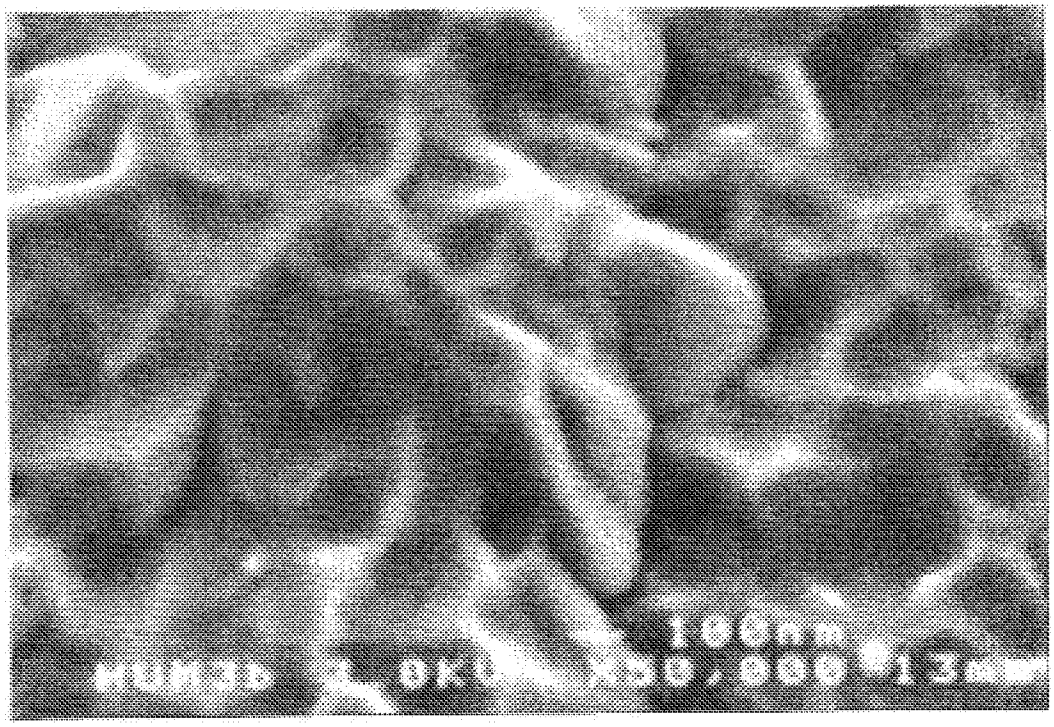
[図7]



[図8]

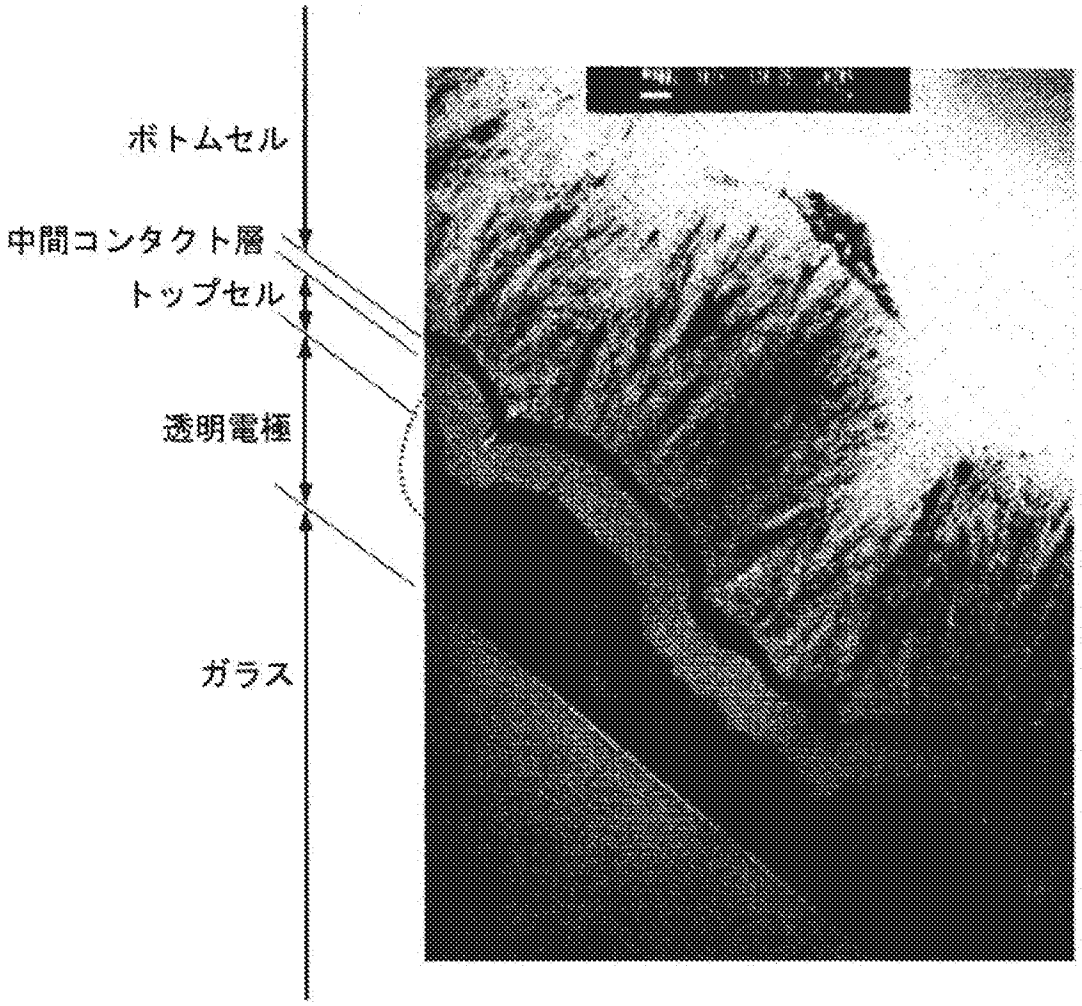


[図9]



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[図10]

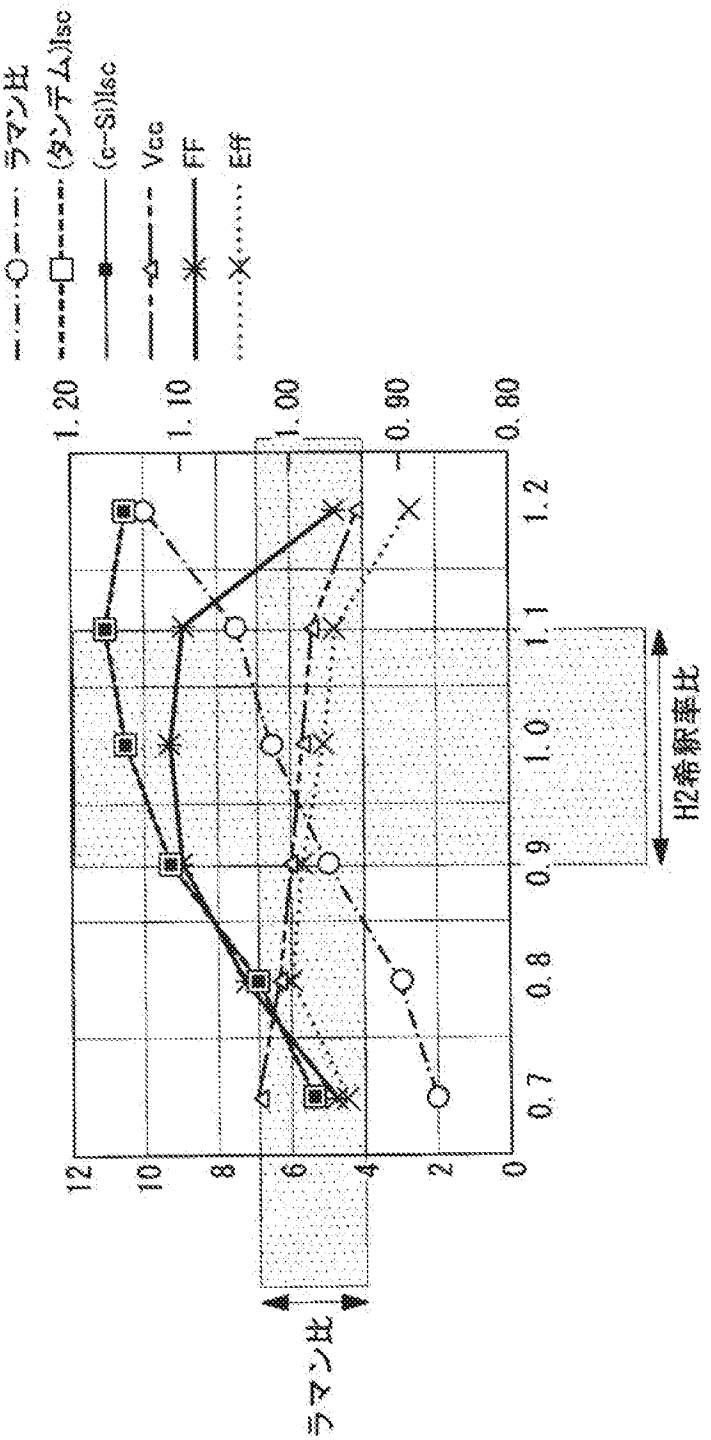


[図11]



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[図12]


ラマン比
(タンデムJ)Isc
(c-Si)Isc
Voc
FF
Eff
1.20
1.10
1.00
0.90
0.80
1.2
1.1
1.0
0.9
0.8
0.7
H2希釈率比
12
10
8
6
4
2
0
ラマン比

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2007/065386

A. CLASSIFICATION OF SUBJECT MATTER
H01L31/04(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L31/04

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2007
Kokai Jitsuyo Shinan Koho 1971-2007 Toroku Jitsuyo Shinan Koho 1994-2007

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2005-347490 A (Asahi Glass Co., Ltd.), 15 December, 2005 (15.12.05), Full text; all drawings (Family: none)	1-4,14,15
Y	JP 2002-26348 A (Mitsubishi Heavy Industries, Ltd.), 25 January, 2002 (25.01.02), Par. No. [0036] (Family: none)	1-4,14,15
Y	JP 2006-216921 A (Mitsubishi Heavy Industries, Ltd.), 17 August, 2006 (17.08.06), Par. No. [0044]; Fig. 5 (Family: none)	1-4,14,15

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 October, 2007 (30.10.07)	13 November, 2007 (13.11.07)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (April 2007)

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2007/065386

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2007-5345 A (Mitsubishi Heavy Industries, Ltd.), 11 January, 2007 (11.01.07), Par. No. [0041]; Fig. 15 (Family: none)	1-4,14,15

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2007/065386

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
A matter common to the inventions in claims 1-19 is "a photoelectric converter comprising a substrate with a transparent electrode where a transparent electrode layer is provided on a transparent insulating substrate, and at least a photoelectric conversion layer principally comprising a silicon based semiconductor and a backside electrode layer that are formed sequentially on the transparent electrode layer side of the substrate with a transparent electrode, wherein the substrate with a transparent electrode has a surface shape where large and small protrusions and recesses coexist and spectral haze rate is 20% or above at the wavelength of 550-800 nm.
(Continued to extra sheet.)

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.: 1-4, 14, 15

Remark on Protest

the

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

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Continuation of Box No.III of continuation of first sheet(2)

However, our search has found the above "photoelectric converter" is disclosed in Japanese Laid-open No. 2005-347490, and therefore it is not clearly novel. Consequently the common matter is not a special technical feature within the meaning of PCT Rule 13.2, second sentence, because the above "photoelectric converter" makes no contribution over the prior art.

Therefore, there is no matter common to all the inventions in claims 1-19 as a special technical feature, and there exists no other common matter to be considered to be a special technical feature within the meaning of PCT Rule 13.2, second sentence, therefore no technical relationship within the meaning of PCT Rule 13 can be found among those different inventions.

Accordingly, the inventions in claims 1-19 do not fulfill the requirement of unity of invention.

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国際調査報告

国際出願番号 PCT／JP2007／066386

A. 発明の属する分野の分類（国際特許分類（IPC））

Int.Cl. H01L31/04(2006.01)i

B. 調査を行った分野

調査を行った最小限資料（国際特許分類（IPC））

Int.Cl. H01L31/04

最小限資料以外の資料で調査を行った分野に含まれるもの

日本国実用新案公報	1922－1996年
日本国公開実用新案公報	1971－2007年
日本国実用新案登録公報	1996－2007年
日本国登録実用新案公報	1994－2007年

国際調査で使用した電子データベース（データベースの名称、調査に使用した用語）

C. 関連すると認められる文献

引用文献のカテゴリー＊	引用文献名 及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
Y	JP 2005-347490 A(旭硝子株式会社), 2005.12.15, 全文, 全図 (ファミリーなし)	1-4, 14, 15
Y	JP 2002-26948 A(三菱重工業株式会社), 2002.01.25, [0036] (ファミリーなし)	1-4, 14, 15
Y	JP 2006-216921 A(三菱重工業株式会社), 2006.08.17, [0044], 図5 (ファミリーなし)	1-4, 14, 15

☑ C欄の続きにも文献が列挙されている。　☐ パテントファミリーに関する別紙を参照。

＊ 引用文献のカテゴリー
「A」特に関連のある文献ではなく、一般的技術水準を示すもの
「E」国際出願日前の出願または特許であるが、国際出願日以後に公表されたもの
「L」優先権主張に疑義を提起する文献又は他の文献の発行日若しくは他の特別な理由を確立するために引用する文献（理由を付す）
「O」口頭による開示、使用、展示等に言及する文献
「P」国際出願日前で、かつ優先権の主張の基礎となる出願の日の後に公表された文献
「T」国際出願日又は優先日後に公表された文献であって出願と矛盾するものではなく、発明の原理又は理論の理解のために引用するもの
「X」特に関連のある文献であって、当該文献のみで発明の新規性又は進歩性がないと考えられるもの
「Y」特に関連のある文献であって、当該文献と他の1以上の文献との、当業者にとって自明である組合せによって進歩性がないと考えられるもの
「&」同一パテントファミリー文献

国際調査を完了した日	国際調査報告の発送日
30.10.2007	13.11.2007

国際調査機関の名称及びあて先	特許庁審査官（権限のある職員）	2K	9010
日本国特許庁（ISA／JP） 郵便番号100－8915 東京都千代田区霞が関三丁目4番3号	吉野 三寛		
	電話番号 03－3581－1101 内線 3255		

様式PCT／ISA／210（第2ページ）（2007年4月）

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Ｃ（続き）．　関連すると認められる文献

引用文献のカテゴリー＊	引用文献名　及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
Y	JP 2007-6345 A(三菱重工業株式会社),2007.01.11, [0041],図15（ファミリーなし）	1-4,14,15

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国際調査報告

国際出願番号 PCT／JP2007／065386

第II欄 請求の範囲の一部の調査ができないときの意見（第1ページの2の続き）

法第8条第3項（PCT17条(2)(a)）の規定により、この国際調査報告は次の理由により請求の範囲の一部について作成しなかった。

1. ☐ 請求の範囲＿＿＿＿＿＿＿＿ は、この国際調査機関が調査をすることを要しない対象に係るものである。
つまり、

2. ☐ 請求の範囲＿＿＿＿＿＿＿＿ は、有意義な国際調査をすることができる程度まで所定の要件を満たしていない国際出願の部分に係るものである。つまり、

3. ☐ 請求の範囲＿＿＿＿＿＿＿＿ は、従属請求の範囲であってPCT規則6.4(a)の第2文及び第3文の規定に従って記載されていない。

第III欄 発明の単一性が欠如しているときの意見（第1ページの3の続き）

次に述べるようにこの国際出願に二以上の発明があるとこの国際調査機関は認めた。

請求の範囲1－19に係る発明の共通の事項は、「透明絶縁性の基板上に透明導電層を設けてなる透明導電膜付き基板と、該透明導電膜付き基板の透明導電層側に順次形成された、シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも有してなる光電変換装置であって、前記透明導電膜付き基板は、表面が凸状の複数の窪みした形状であり、かつ光トイズ率が500nm以上800nm以下の波長で20%以上である光電変換装置」である。

しかしながら、調査の結果、上記「光電変換装置」は、特開2005－347490号公報に開示されており、新規でないことが明らかとなり、結果として、上記「光電変換装置」は先行技術の域を出ないから、PCT規則13.2の第2文の意味において、この共通事項は特別な技術的特徴ではない。

それ故、特別な技術的特徴として請求の範囲1－19に係る発明全てに共通の事項はなく、PCT規則13.2の第2文の意味において特別な技術的特徴と考えられる他の共通の事項も存在しないので、それらの間違する発明の間にPCT規則13の意味における技術的な関連を見いだすことはできない。

よって、請求項1－19に係る発明は、発明の単一性の要件を満たしていない。

1. ☐ 出願人が必要な追加調査手数料をすべて期間内に納付したので、この国際調査報告は、すべての調査可能な請求の範囲について作成した。

2. ☐ 追加調査手数料を要求するまでもなく、すべての調査可能な請求の範囲について調査することができたので、追加調査手数料の納付を求めなかった。

3. ☐ 出願人が必要な追加調査手数料を一部のみしか期間内に納付しなかったので、この国際調査報告は、手数料の納付のあった次の請求の範囲のみについて作成した。

4. ☑ 出願人が必要な追加調査手数料を期間内に納付しなかったので、この国際調査報告は、請求の範囲の最初に記載されている発明に係る次の請求の範囲について作成した。

請求項1－4，14，15

追加調査手数料の異議の申立てに関する注意

☐ 追加調査手数料及び、該当する場合には、異議申立手数料の納付と共に、出願人から異議申立てがあった。

☐ 追加調査手数料の納付と共に出願人から異議申立てがあったが、異議申立手数料が納付命令書に示した期間内に支払われなかった。

☐ 追加調査手数料の納付はあったが、異議申立てはなかった。

様式PCT／ISA／210（第1ページの続葉（2））（2007年4月）

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(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

(19) Weltorganisation für geistiges Eigentum
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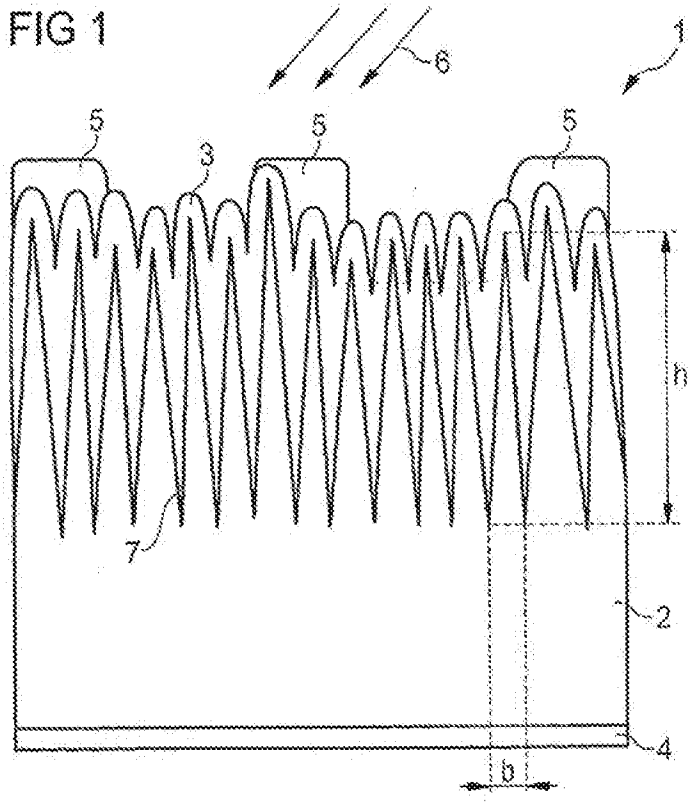
(81) Bestimmungsstaaten *(soweit nicht anders angegeben, für jede verfügbare nationale Schutzrechtsart)*: AE, AG, AL,

[Fortsetzung auf der nächsten Seite]

(54) Title: PHOTOSENSITIVE SEMICONDUCTOR COMPONENT

(54) Bezeichnung: FOTOEMPFINDLICHES HALBLEITERBAUELEMENT

FIG 1



(57) Abstract: The invention relates to a semiconductor component (1) comprising a photosensitive doped semiconductor layer (2), in which electric charge carriers are released during the absorption of electromagnetic radiation (6). The photosensitive semiconductor layer (2) has a structured boundary layer (7). The structured boundary layer (7) is positioned after at least one layer (3) that generates an electric field for separating the released charge carriers, said electric field extending over the structured boundary surface (7). The photosensitive semiconductor component (1) is characterised by a highly efficient charge carrier separation, in particular for generating an electric current.

(57) Zusammenfassung: Bei einem Halbleiterbauelement (1) mit einer fotoempfindlichen dotierten Halbleiterschicht (2), in der bei Absorption elektromagnetischer Strahlung (6) elektrische Ladungsträger freigesetzt werden, weist die fotoempfindliche Halbleiterschicht (2) eine strukturierte Grenzfläche (7) auf. Der strukturierten Grenzfläche (7) ist mindestens eine Schicht (3) nachgeordnet, die ein elektrisches Feld zur Trennung der freigesetzten Ladungsträger erzeugt, wobei sich das elektrische Feld über die strukturierte Grenzfläche (7) erstreckt. Das photoempfindliche Halbleiterbauelement (1) zeichnet sich durch eine hohe Effizienz der Ladungsträgertrennung, insbesondere zur Erzeugung eines elektrischen Stroms, aus.

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AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Bestimmungsstaaten** *(soweit nicht anders angegeben, für jede verfügbare regionale Schutzrechtsart)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), eurasisches (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), europäisches (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Veröffentlicht:

— *ohne internationalen Recherchenbericht und erneut zu veröffentlichen nach Erhalt des Berichts*

Beschreibung

Fotoempfindliches Halbleiterbauelement

Die Erfindung betrifft ein fotoempfindliches Halbleiterbauelement gemäß dem Oberbegriff des Patentanspruchs 1.

Diese Patentanmeldung beansprucht die Priorität der deutschen Patentanmeldung 102007024478.0, deren Offenbarungsgehalt hiermit durch Rückbezug aufgenommen wird.

Ein fotoempfindliches Halbleiterbauelement in Form einer Solarzelle ist zum Beispiel aus der Druckschrift US 4,177,093 bekannt. Die darin beschriebene Solarzelle umfasst ein dotiertes Halbleitersubstrat, eine darauf aufgebrachte Schicht aus Indiumzinnoxid (ITO) sowie elektrische Kontakte, die auf der Rückseite des Substrats und auf der Oberfläche der ITO-Schicht aufgebracht sind. Die ITO-Schicht wirkt mit dem Substrat derart zusammen, dass ähnlich wie bei einem pn-Übergang die im Substrat durch Absorption elektromagnetischer Strahlung freigesetzten elektrischen Ladungsträger zur Erzeugung eines elektrischen Stroms getrennt werden.

Eine weitere Solarzelle ist aus der Druckschrift US 5,949,123 bekannt. Diese Solarzelle basiert auf einem p-dotierten Siliziumsubstrat, in das ein n-Dotierstoff zur Erzeugung eines vergrabenen pn-Übergangs implantiert ist. Um die Reflexion der Oberfläche des Siliziumsubstrats zu vermindern, ist die Oberfläche des Siliziumsubstrats strukturiert. Auf diese Weise wird erreicht, dass ein höherer Lichtanteil in das Siliziumsubstrat eindringen kann.

In der Druckschrift WO 02/13279 A2 wird beschrieben, die

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Oberfläche einer Solarzelle mittels eines Ätzverfahrens zu strukturieren, um die Reflexion der Oberfläche zu vermindern.

Aus der Druckschrift M. Stubenrauch, M. Fischer, C. Kremin, S. Stoebenau, A. Albrecht, O. Nagel, „Black Silicon - New Functionalities in Microsystems", J. Michromech. Microeng. 16 (2006), S. S2-86, ist ein Plasmaätzverfahren zur Herstellung von nadelartigen Strukturen in Siliziumschichten bekannt. Weiterhin beschreibt auch die Druckschrift H. Jansen, M. De Boer, R. Legtenberg, M. Elwenspoek, „The black silicon method: a universal method for determining the parameter setting of a fluorine-based reactive ion etcher in deep silicon trench etching with profile control", J. Michromech. Microeng. 5 (1995), S. 115-120, ein Verfahren zur Herstellung von nadelartigen Strukturen in Silizium.

Der Erfindung liegt die Aufgabe zugrunde, ein verbessertes fotoempfindliches Halbleiterbauelement anzugeben, das sich insbesondere durch eine effizientere Ladungsträgertrennung der in einem fotoempfindlichen Halbleitermaterial erzeugten Ladungsträger auszeichnet.

Diese Aufgabe wird durch den Gegenstand des Patentanspruchs 1 gelöst. Vorteilhafte Ausgestaltungen und Weiterbildungen der Erfindung sind Gegenstand der abhängigen Ansprüche.

Bei einem erfindungsgemäßen Halbleiterbauelement mit einer fotoempfindlichen dotierten Halbleiterschicht, in der bei Absorption elektromagnetischer Strahlung elektrische Ladungsträger freigesetzt werden, weist die fotoempfindliche Halbleiterschicht eine strukturierte Grenzfläche auf. Der strukturierten Grenzfläche ist mindestens eine Schicht nachgeordnet, die ein elektrisches Feld zur Trennung der freigesetzten

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Ladungsträger erzeugt, wobei sich das elektrische Feld über die strukturierte Grenzfläche erstreckt.

Die der fotoempfindlichen Halbleiterschicht nachgeordnete Schicht kann unmittelbar auf die strukturierte Grenzfläche aufgebracht sein oder durch eine oder mehrere Zwischenschichten von der fotoempfindlichen Halbleiterschicht beabstandet sein. Dadurch, dass die zur Erzeugung eines elektrischen Feldes geeignete Schicht der fotoempfindlichen Halbleiterschicht nachgeordnet ist, wird erreicht, dass sich das elektrische Feld über die strukturierte Grenzfläche der fotoempfindlichen Schicht erstreckt. Somit ist der aktive Bereich, in dem eine Ladungsträgertrennung stattfindet, aufgrund der Strukturierung der photoempfindlichen Schicht wesentlich größer als bei herkömmlichen Bauelementen, bei denen der aktive Bereich beispielsweise aus einer ebenen Grenzfläche zwischen einem Siliziumsubstrat und einer ITO-Schicht oder aus einem innerhalb des Substrats ausgebildeten pn-Übergang gebildet ist. Durch die Strukturierung der fotoempfindlichen Schicht wird also nicht nur die Reflexion der Grenzfläche vermindert, sondern auch der aktive Bereich, in dem Ladungsträgertrennung stattfindet, vergrößert.

Die dem Substrat nachgeordnete Schicht enthält insbesondere ein transparentes elektrisch leitfähiges Material. Vorzugsweise ist das transparente elektrisch leitfähige Material ein transparentes leitfähiges Oxid, insbesondere Indiumzinnoxid (ITO), Indiumzinkoxid (IZO), Zinkoxid (ZnO) oder Cadmium-Stannat (CTO, Cd_2SnO_4).

Weiterhin kann das transparente elektrisch leitfähige Material auch ein transparentes leitfähiges Polymer sein.

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Bei einer weiteren bevorzugten Ausführungsform ist die der fotoempfindlichen Halbleiterschicht nachgeordnete Schicht eine Halbleiterschicht, die sich in ihren Dotierungstyp und/oder ihrer Dotierstoffkonzentration von der fotoempfindlichen Halbleiterschicht unterscheidet.

Insbesondere kann die der dotierten fotoempfindlichen Halbleiterschicht nachgeordnete Schicht den entgegengesetzten Dotierungstyp aufweisen, so dass zum Beispiel die fotoempfindliche Halbleiterschicht p-dotiert ist und die nachgeordnete Schicht n-dotiert ist oder umgekehrt. Auf diese Weise wird an der Grenzfläche der strukturierten fotoempfindlichen Halbleiterschicht ein pn-Übergang ausgebildet, wobei der pn-Übergang aufgrund der Strukturierung vorteilhaft größer ist als bei einer ebenen Grenzfläche zwischen den Halbleiterschichten entgegengesetzten Dotierungstyps.

Zwischen der fotoempfindlichen Schicht und der ihr nachgeordneten Schicht kann mindestens eine Zwischenschicht angeordnet sein. Insbesondere kann es sich bei der Zwischenschicht um eine Siliziumoxidschicht handeln, die sich beispielsweise auf der fotoempfindlichen Halbleiterschicht ausbilden kann, bevor die transparente leitfähige Schicht aufgebracht wird. Weiterhin kann es sich bei der Zwischenschicht auch um eine Schicht aus einem intrinsischen Halbleitermaterial handeln, insbesondere wenn es sich bei der fotoempfindlichen Halbleiterschicht und der nachgeordneten Schicht um zwei Halbleiterschichten mit verschiedenem Dotierungstyp handelt.

Die strukturierte Grenzfläche der fotoempfindlichen Halbleiterschicht ist vorzugsweise derart strukturiert, dass sie Strukturen mit einer Breite von weniger als 100 nm aufweist.

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Bevorzugt weist die strukturierte Grenzfläche Strukturen auf, die eine Breite zwischen 10 nm und 100 nm aufweisen.

Aufgrund der strukturierten Grenzfläche ist zwischen der fotoempfindlichen Schicht und der nachfolgenden Schicht ein Brechungsindexgradient ausgebildet, so dass die Grenzfläche zwischen den Schichten als effektives Medium wirkt.

Weiterhin ist es vorteilhaft, wenn die an der Grenzfläche der fotoempfindlichen Halbleiterschicht erzeugten Strukturen eine Höhe von mehr als 100 nm aufweisen. Insbesondere kann die Höhe der an der strukturierten Grenzfläche erzeugten Strukturen zwischen 1,5 µm und 10 µm betragen.

Die an der Grenzfläche der fotoempfindlichen Halbleiterschicht erzeugten Strukturen zeichnen sich insbesondere durch ein hohes Aspektverhältnis aus. Dies hat den Vorteil, dass die Grenzfläche im Vergleich zu einer nahezu glatten Grenzfläche erheblich vergrößert wird. Bevorzugt beträgt die Höhe der Strukturen im Mittel mindestens das 10-fache der Breite, besonders bevorzugt sogar mindestens das 50-fache der Breite.

Bei einer vorteilhaften Ausgestaltung weist die strukturierte Grenzfläche der fotoempfindlichen Halbleiterschicht Strukturen auf, die überwiegend, also mehr als zur Hälfte, eine Flankensteilheit von mehr als 45° aufweisen. Beispielsweise können die Flanken der Strukturen Winkel im Bereich von 80° bis 85° mit einer Hauptebene der photoempfindlichen Halbleiterschicht einschließen. Insbesondere kann es sich bei den Strukturen um nadelförmige Strukturen handeln.

Die strukturierte Grenzfläche kann insbesondere eine stochastische Struktur aufweisen, also eine Struktur, bei der

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die Strukturhöhen und Strukturbreiten im Gegensatz zu deterministischen Strukturen, die beispielsweise mit lithografischen Techniken erzeugt werden, eine statistische Verteilung aufweisen.

Bevorzugt ist die strukturierte Grenzfläche mittels eines Ätzverfahrens strukturiert. Dazu wird vorzugsweise ein Plasmaätzverfahren eingesetzt, wie insbesondere ein ICP-Ätzverfahren (inductively coupled plasma). Alternativ können aber auch andere Verfahren der physikalischen Abtragung wie beispielsweise Laserstrukturierung eingesetzt werden.

Die Anwendung eines Ätzverfahrens zur Erzeugung einer stochastischen Struktur ist im Vergleich zu lithographischen Strukturierungsverfahren vorteilhaft, weil der Herstellungsaufwand vergleichsweise gering ist.

Alternativ ist es aber auch möglich, dass die Grenzfläche der fotoempfindlichen Halbleiterschicht eine deterministische, also vorbestimmte Struktur aufweist, die beispielsweise lithografisch, insbesondere unter Verwendung einer Ätzmaske, hergestellt ist.

Die Erfindung wird im Folgenden anhand von Ausführungsbeispielen näher erläutert.

Es zeigen:

Figur 1 eine schematische Darstellung eines Halbleiterbauelements gemäß einem ersten Ausführungsbeispiel der Erfindung,

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Figur 2 eine grafische Darstellung der Reflexion einer strukturierten Siliziumschicht im Vergleich zu einer unstrukturierten Siliziumschicht und

Figur 3 eine schematische Darstellung eines Halbleiterbauelements gemäß einem zweiten Ausführungsbeispiel der Erfindung.

Gleiche oder gleich wirkende Elemente sind in den Figuren mit den gleichen Bezugszeichen versehen. Die Figuren sind nicht als maßstabsgerecht anzusehen, vielmehr können einzelne Elemente zur Verdeutlichung übertrieben groß dargestellt sein.

Das in Figur 1 dargestellte Halbleiterbauelement 1 gemäß einem ersten Ausführungsbeispiel der Erfindung ist eine Solarzelle, die eine fotoempfindliche Halbleiterschicht 2, zum Beispiel eine p-dotierte Siliziumschicht, enthält. Die Halbleiterschicht 2 kann insbesondere ein Silizium-Wafer sein, der typischerweise eine Dicke von mehr als 100 µm aufweist. Alternativ kann die Halbleiterschicht 2 aber auch eine auf ein Substrat aufgebrachte Halbleiterschicht sein, zum Beispiel eine auf einen metallischen Reflektor (nicht dargestellt) aufgebrachte Halbleiterschicht.

In der fotoempfindlichen Halbleiterschicht 2 werden beim Auftreffen elektromagnetischer Strahlung, die durch die Pfeile 6 angedeutet ist, elektrische Ladungsträger freigesetzt. Insbesondere kann es sich bei dem Halbleiterbauelement 1 um eine Solarzelle handeln, bei der durch Absorption von Sonnenlicht in der fotoempfindlichen Halbleiterschicht 2 Elektron-Loch-Paare als freie Ladungsträger erzeugt werden.

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Auf die fotoempfindliche Halbleiterschicht 2 ist eine Schicht 3 aufgebracht, mittels der ein elektrisches Feld zur Trennung der freigesetzten Ladungsträger erzeugt wird. Auf diese Weise kann insbesondere ein elektrischer Strom aus den freigesetzten Ladungsträgern erzeugt werden. Um den elektrischen Strom aus dem Halbleiterbauelement 1 abzuführen, kann ein erster elektrischer Kontakt 4 an einer von der Schicht 3 abgewandten Rückseite der Halbleiterschicht 2 und ein weiterer elektrischer Kontakt 5 auf der Schicht 3 angeordnet sein. Der zweite elektrische Kontakt 5 kann beispielsweise streifenförmig über die Grenzfläche der Schicht 3 geführt sein.

Die fotoempfindliche Halbleiterschicht 2 weist eine strukturierte Grenzfläche 7 auf. Die strukturierte Grenzfläche 7 kann beispielsweise mit einem Plasmaätzverfahren, insbesondere durch induktiv gekoppeltes Plasmaätzen (ICP) erzeugt werden. Dabei werden beispielsweise SF_6 und O_2 als Ätzgase verwendet. Die Form der erzeugten Strukturen kann dabei durch die Wahl der Ätzparameter, insbesondere der Zusammensetzung der Ätzgase, gezielt eingestellt werden. Geeignete Plasmaätzverfahren, insbesondere zur Erzeugung nadelförmiger Strukturen, sind an sich aus den in der Einleitung zitierten Druckschriften bekannt und werden daher nicht näher erläutert.

Bevorzugt werden mit dem Ätzverfahren an der Grenzfläche 7 Strukturen erzeugt, die ein hohes Aspektverhältnis aufweisen. Die Grenzflächenstrukturen weisen bevorzugt eine Höhe h auf, die größer als ihre Breite b ist. Bevorzugt beträgt die Höhe der Strukturen h im Mittel mindestens das 10-fache der Breite b, besonders bevorzugt sogar mindestens das 50-fache der Breite b. Insbesondere zeichnen sich die Strukturen vorteilhaft durch eine hohe Flankensteilheit auf. Bevorzugt weisen

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die Strukturen überwiegend, das heißt mindestens zur Hälfte, eine Flankensteilheit von mehr als 45° auf.

Die Breite b der Strukturen beträgt bevorzugt weniger als 100 nm, insbesondere zwischen einschließlich 10 nm und einschließlich 100 nm. Die Höhe h der Strukturen der Grenzfläche 7 beträgt vorzugsweise zwischen einschließlich 1,5 µm und einschließlich 5 µm.

Die Strukturierung der Grenzfläche 7 der Halbleiterschicht 2 wirkt sich in zweifacher Hinsicht positiv auf die Effizienz des Halbleiterbauelements 1 aus. Zum einen wird die Reflexion der Grenzfläche der Halbleiterschicht 2 durch die Strukturierung vermindert. Aufgrund der Strukturierung der fotoempfindlichen Halbleiterschicht 2 vermindert sich auch die Reflexion der Oberfläche des Halbleiterbauelements, wenn die mindestens eine der Halbleiterschicht nachfolgende Schicht 3 derart dünn ist, dass auch ihre Oberfläche die Strukturierung aufweist. Die Verminderung der Reflexion der Grenzfläche 7 der Halbleiterschicht 2 wird in Figur 2 verdeutlicht, in der die Reflexion einer Siliziumschicht vor und nach der Strukturierung in Abhängigkeit von der Wellenlänge dargestellt ist. Die Kurve 9 stellt die Reflexion der Siliziumschicht vor der Strukturierung und die Kurve 10 die Reflexion der Siliziumschicht nach der Strukturierung dar. Da die strukturierte Schicht eine wesentliche geringere Reflexion als eine unstrukturierte Schicht aufweist, kann ein größerer Anteil der auftreffenden Strahlung in die photoempfindliche Schicht eindringen, wodurch die Effizienz des photoempfindlichen Halbleiterbauelements verbessert wird.

Ein weiterer Vorteil der Strukturierung der Halbleiterschicht 2 ergibt sich daraus, dass die Schicht 3, mittels der ein

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elektrisches Feld zur Trennung der in der fotoempfindlichen Halbleiterschicht 2 freigesetzten Ladungsträger erzeugt wird, der Halbleiterschicht 2 nachgeordnet ist, d.h. auf oder über der photoempfindlichen Halbleiterschicht 2 angeordnet ist. Auf diese Weise wird erreicht, dass sich das elektrische Feld, mit dem die freigesetzten Ladungsträger getrennt werden, über die strukturierte Grenzfläche 7 der Halbleiterschicht 2 erstreckt. Der Bereich, in dem die Ladungsträgertrennung stattfindet, ist daher größer als im Fall einer unstrukturierten Grenzfläche zwischen einer Halbleiterschicht 2 und der ihr nachgeordneten Schicht 3. Beispielsweise kann durch die Strukturierung die Grenzfläche 7 der fotoempfindlichen Halbleiterschicht um einen Faktor 10 oder mehr vergrößert werden.

Die der strukturierten Halbleiterschicht 2 nachgeordnete Schicht 3 enthält vorzugsweise ein transparentes elektrisch leitfähiges Material, insbesondere ein transparentes leitfähiges Oxid oder ein transparentes leitfähiges Polymer. Die Schicht 3 kann zum Beispiel eine Dicke von etwa 1 µm aufweisen.

Geeignete transparente leitfähige Oxide sind insbesondere Indiumzinnoxid (ITO) und Indiumzinkoxid (IZO). Weiterhin sind Zinkoxid (ZnO), das insbesondere mit Al dotiert sein kann, oder Cadmium-Stannat (Cd_2SnO_4) geeignet.

Alternativ ist es auch möglich, dass die Schicht 3 ein Halbleitermaterial aufweist, das einen zu der Halbleiterschicht 2 entgegengesetzten Dotierungstyp aufweist. Beispielsweise kann die Halbleiterschicht 2 p-dotiert und die Schicht 3 n-dotiert sein. In diesem Fall ist zwischen der Halbleiterschicht 2 und der Schicht 3 ein pn-Übergang ausgebildet, der sich über die

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strukturierte Grenzfläche 7 der Halbleiterschicht 2 erstreckt. Der Bereich des pn-Übergangs ist aufgrund der Strukturierung vorteilhaft wesentlich größer als im Fall einer ebenen Grenzfläche zwischen einer p-dotierten Halbleiterschicht und einer n-dotierten Halbleiterschicht. Bei den Schichten 2, 3 kann es sich beispielsweise um Siliziumschichten mit unterschiedlicher Dotierung handeln. Alternativ können aber auch andere Halbleitermaterialien eingesetzt werden, beispielsweise III-V-Halbleitermaterialien wie insbesondere GaAs oder InAs.

Das in Figur 3 dargestellte Ausführungsbeispiel eines Halbleiterbauelements unterscheidet sich von dem in Figur 1 dargestellten dadurch, dass zwischen der fotoempfindlichen Halbleiterschicht 2 und der ihr nachgeordneten Schicht 3, mittels der das elektrische Feld zur Ladungsträgertrennung erzeugt wird, eine Zwischenschicht 8 angeordnet ist. Insbesondere kann die fotoempfindliche Halbleiterschicht 2 eine Siliziumschicht und die Zwischenschicht 8 eine Siliziumoxidschicht sein. Die Siliziumoxidschicht 8 kann insbesondere eine natürliche Oxidschicht sein, die sich auf der Siliziumschicht 2 ausbildet, wenn die Halbleiterschicht 2 vor dem Aufbringen der Schicht 3 in Kontakt mit Luft gerät.

Weiterhin kann es sich bei der Zwischenschicht 8 auch um eine Schicht aus einem intrinsischen Halbleitermaterial handeln, die beispielsweise zwischen zwei entgegengesetzten dotierten Halbleiterschichten eingefügt ist, um die Rekombination der Ladungsträger zu vermindern.

Die Erfindung ist nicht durch die Beschreibung anhand der Ausführungsbeispiele beschränkt. Vielmehr umfasst die Erfindung jedes neue Merkmal sowie jede Kombination von Merkmalen,

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was insbesondere jede Kombination von Merkmalen in den Patentansprüchen beinhaltet, auch wenn dieses Merkmal oder diese Kombination selbst nicht explizit in den Patentansprüchen oder Ausführungsbeispielen angegeben ist.

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Patentansprüche

1. Halbleiterbauelement (1) mit einer fotoempfindlichen dotierten Halbleiterschicht (2), in der bei Absorption elektromagnetischer Strahlung (6) elektrische Ladungsträger freigesetzt werden, wobei die fotoempfindliche Halbleiterschicht (2) eine strukturierte Grenzfläche (7) aufweist,
dadurch gekennzeichnet, dass
der strukturierten Grenzfläche (7) mindestens eine Schicht (3) nachgeordnet ist, die ein elektrisches Feld zur Trennung der freigesetzten Ladungsträger erzeugt, wobei sich das elektrische Feld über die strukturierte Grenzfläche (7) erstreckt.

2. Halbleiterbauelement nach Anspruch 1,
dadurch gekennzeichnet, dass
die der fotoempfindlichen Halbleiterschicht (2) nachgeordnete Schicht (3) ein transparentes elektrisch leitfähiges Material enthält.

3. Halbleiterbauelement nach Anspruch 2,
dadurch gekennzeichnet, dass
das transparente elektrisch leitfähige Material ein transparentes leitfähiges Oxid ist.

4. Halbleiterbauelement nach Anspruch 3,
dadurch gekennzeichnet, dass
das transparente leitfähige Oxid Indiumzinnoxid, Indiumzinkoxid, Zinkoxid oder Cadmium-Stannat ist.

5. Halbleiterbauelement nach Anspruch 2,
dadurch gekennzeichnet, dass

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das transparente elektrisch leitfähige Material ein transparentes leitfähiges Polymer ist.

6. Halbleiterbauelement nach Anspruch 2, dadurch gekennzeichnet, dass die der fotoempfindlichen Halbleiterschicht (2) nachgeordnete Schicht (3) eine Halbleiterschicht ist, die sich in ihrem Dotierungstyp und/oder ihrer Dotierstoffkonzentration von der fotoempfindlichen Halbleiterschicht (2) unterscheidet.

7. Halbleiterbauelement nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass zwischen der fotoempfindlichen Schicht (2) und der ihr nachgeordneten Schicht (3) mindestens eine Zwischenschicht (8) angeordnet ist.

8. Halbleiterbauelement nach Anspruch 7, dadurch gekennzeichnet, dass die Zwischenschicht (8) ein Siliziumoxid oder ein intrinsisches Halbleitermaterial enthält.

9. Halbleiterbauelement nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (3) Strukturen mit einer Breite (b) von weniger als 100 nm aufweist.

10. Halbleiterbauelement nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass

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die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (2) Strukturen mit einer Höhe (h) von mehr als 100 nm aufweist.

11. Halbleiterbauelement nach Anspruch 10, dadurch gekennzeichnet, dass die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (2) Strukturen mit einer Höhe (h) zwischen 1,5 µm und 10 µm aufweist.

12. Halbleiterbauelement nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (2) Strukturen aufweist, deren Höhe mindestens das 50-fache der Breite beträgt.

13. Halbleiterbauelement nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (2) Strukturen mit einer Flächendichte von mindestens 10^4 cm^{-2} aufweist.

14. Halbleiterbauelement nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (2) Strukturen aufweist, die überwiegend eine Flankensteilheit von mehr als 45° aufweisen.

15. Halbleiterbauelement nach einem der vorhergehenden Ansprüche,

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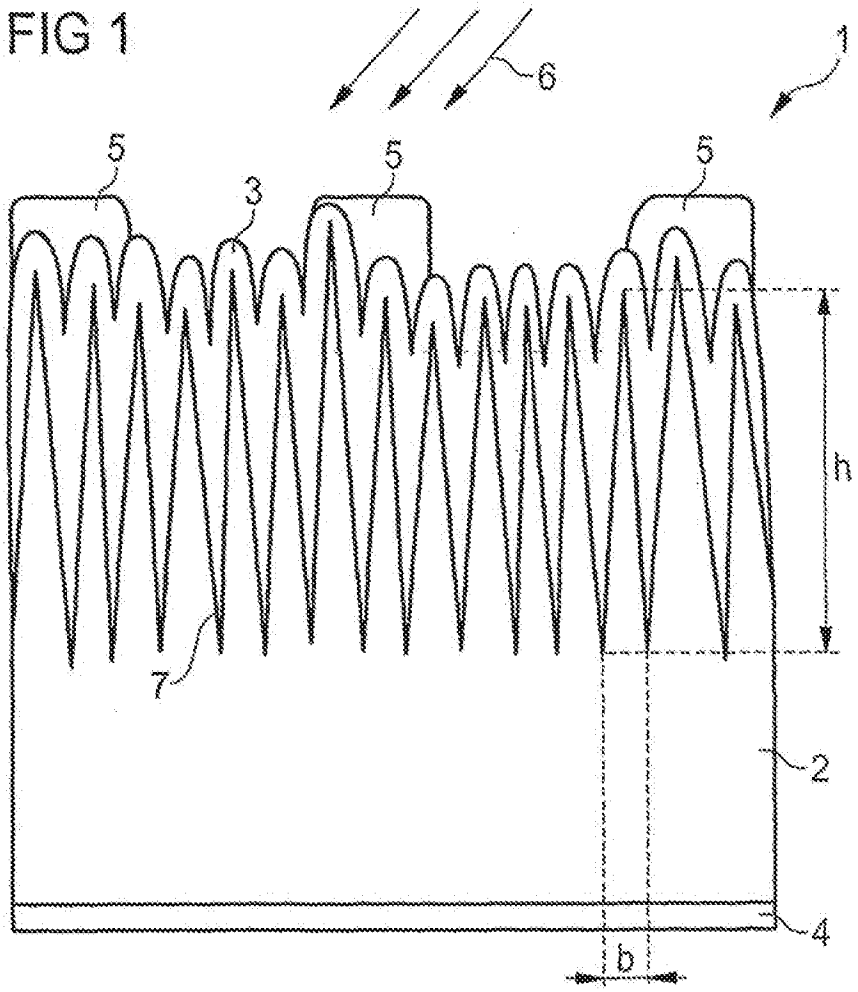
dadurch gekennzeichnet, dass
die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (2) eine stochastische Struktur aufweist.

16. Halbleiterbauelement nach einem der Ansprüche 1 bis 14, dadurch gekennzeichnet, dass
die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (2) eine deterministische Struktur aufweist.

17. Halbleiterbauelement nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass
die strukturierte Grenzfläche (7) der fotoempfindlichen Halbleiterschicht (2) mittels eines Ätzverfahrens strukturiert ist.

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FIG 1



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FIG 2

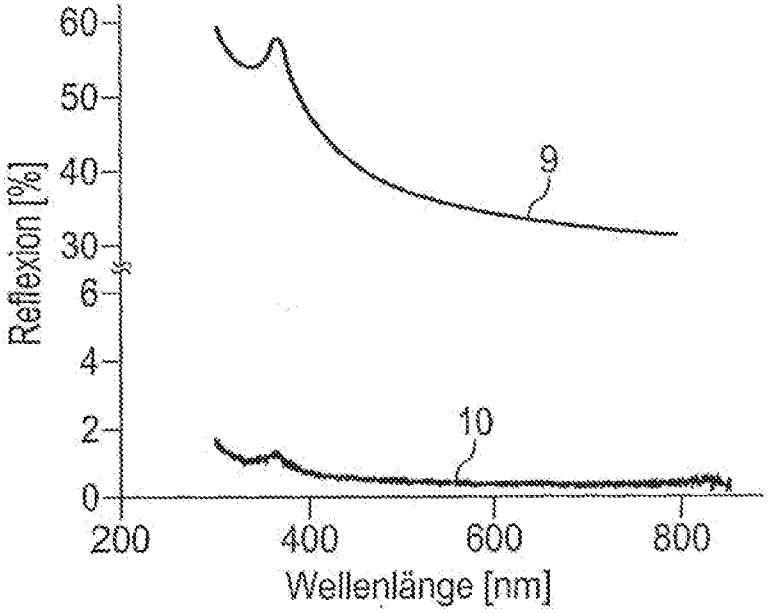
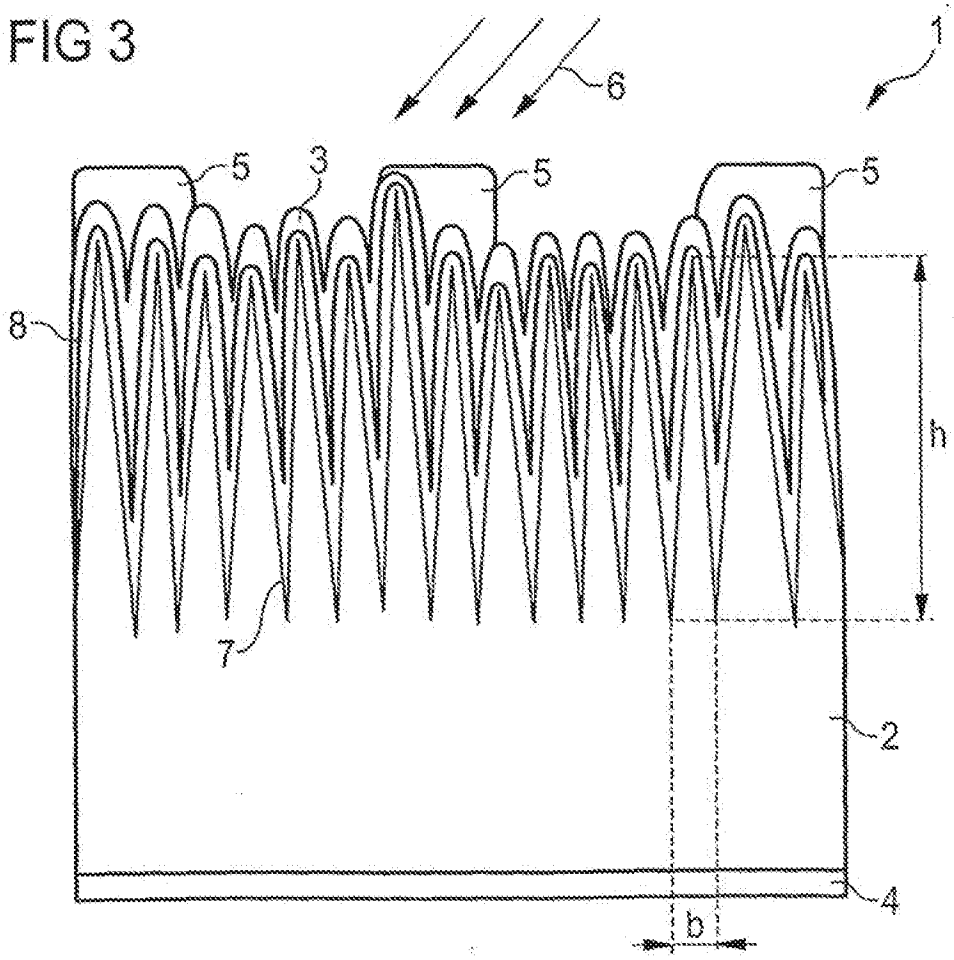


FIG 3



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Espacenet

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SYSTEM AND METHODS FOR LASER ASSISTED DEPOSITION

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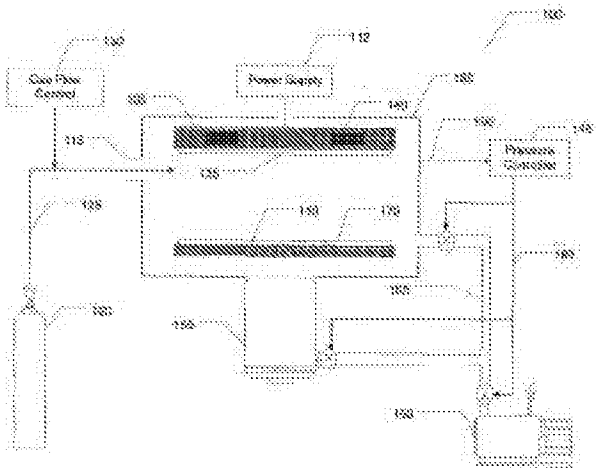
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Abstract of WO0241363 (A2)

Systems and methods for laser assisted deposition use an energy source such as a laser to simultaneously deposit and anneal a thin film of semiconductor or metal material on a substrate. The uniform heating of the deposited material while the layer is being sputtered obviates a subsequent annealing stage. The laser can be pulsed or continuous wave. The substrate can be plastic such as tedlar, mylar, teflon, or tefzel. The systems and methods for laser assisted deposition can be used to manufacture solar cells, such as a cadmium telluride (CdTe) solar cell having a cadmium sulfide (CdS) window layer. Both the techniques of sputtering and sublimation can be used to grow the layer.



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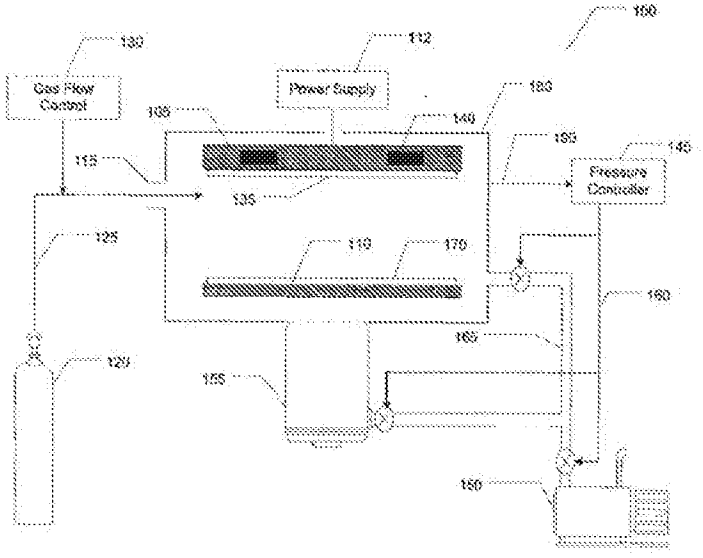
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(54) Title: SYSTEM AND METHODS FOR LASER ASSISTED DEPOSITION



(57) Abstract: Systems and methods for laser assisted deposition use an energy source such as a laser to simultaneously deposit and anneal a thin film of semiconductor or metal material on a substrate. The uniform heating of the deposited material while the layer is being sputtered obviates a subsequent annealing stage. The laser can be pulsed or continuous wave. The substrate can be plastic such as tedlar, mylar, teflon, or tefzel. The systems and methods for laser assisted deposition can be used to manufacture solar cells, such as a cadmium telluride (CdTe) solar cell having a cadmium sulfide (CdS) window layer. Both the techniques of sputtering and sublimation can be used to grow the layer.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

SYSTEMS AND METHODS FOR LASER ASSISTED DEPOSITION

Related Applications

[01] This application claims the benefit of United States Provisional Application Serial No. 60/249,367, filed November 16, 2000, and United States Provisional Application Serial No. 60/254,760, filed December 12, 2000, and this application is a continuation-in-part of United States Patent Application Serial No. 09/892,131 filed June 25, 2001.

Field of the Invention

[02] The present invention relates generally to the deposition of thin films and, more particularly relates to methods and systems for laser assisted deposition.

Background of the Invention

[03] The fabrication of solar cells presents unique manufacturability challenges to the solar energy industry. Chief among them is the difficulty often encountered in depositing the semiconductor layers that form a cell's pn-junction onto a substrate material capable of withstanding high processing temperatures. In the past, this challenge has prevented the manufacture of solar cells on flexible materials such as plastic because many plastics break down or become damaged during high temperature deposition and annealing.

[04] Known deposition systems for creating thin films include evaporation, chemical vapor deposition and sublimation. Deposition is a physical vapor deposition process in which a target material is bombarded by high-energy ions, causing the target material to eject atoms or molecules that are then deposited in a thin layer on the substrate. Deposition is relied on heavily in the solar cell industry for at least two reasons: First, deposition permits the deposition of complex alloys, such as CdTe, CdS, and other compound semiconductors. Second, deposition is ideal for depositing controlled, uniform films onto substrates having large surface area, such as the substrates used to

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produce solar cells and panels. Sublimation is an alternative technique for depositing a solid state material onto a surface that is also widely used to manufacture solar cells.

[05] In semiconductor wafer manufacturing, annealing has traditionally been performed as a follow-on step subsequent to ion implantation or other process step known to damage the crystal lattice. In contrast, thin film manufacturing uses annealing primarily to improve crystalinity of the amorphous deposited layer. In both cases, annealing usually takes place at a temperature of about 500°C. Most plastics break down when exposed to such high heat. As a result, thin film solar cell construction has required a heat tolerant substrate material such as glass. Unfortunately, glass solar cells have limited applications due to their cost and bulkiness. Thus, a manufacturing process and apparatus capable of depositing thin film layers onto a flexible and low-cost plastic or polymeric substrate is desirable.

Summary of the Invention

[06] The present invention addresses the drawbacks of prior art thin film deposition techniques noted above and provides systems and methods for laser assisted deposition of thin films.

[07] The systems and methods for laser assisted deposition use a thin film deposition technique that combines thin film deposition and annealing into one processing stage. In one embodiment, the target material for deposition is mounted to a negatively charged cathode in a magnetron or similar processing apparatus having a plasma within a chamber and sputter-depositing the target material onto a substrate to build a thin film layer thereon. In one embodiment the substrate material is a plastic or polymeric material such as tedlar, mylar, tefzel, or teflon.

[08] The processing apparatus can be modified to contain an energy source. In one implementation of the invention, the energy source is a laser. The energy source could be any homogenized beam energy source producing electromagnetic energy of any wavelength sufficient to anneal the thin film layer without overheating or damaging the substrate. The energy source can be a pulsed source of very short duration so as to prevent the beam from damaging the substrate. Alternatively, the energy source can be a continuous wave source that is scanned back and forth across the film surface in order

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to evenly heat the target material as it gets deposited onto the substrate. In both cases, the majority of the energy from the source is ideally absorbed by the film before being passed on to the substrate.

[09] In one embodiment of the invention, the systems and methods for laser assisted deposition are used to manufacture a solar cell, for example a cadmium telluride solar cell having cadmium telluride (CdTe) as the absorption layer and cadmium sulfide (CdS) as the window layer. Other layers utilizing laser assisted deposition, such as current collection layers, may be necessary to complete the solar cell.

[10] The systems and methods for laser assisted deposition may incorporate a radio frequency system, a magnetron, or any other similar apparatus designed for depositing thin films.

Brief Description of the Drawings

[11] The details of the present invention, both as to its structure and operation, may be gleaned in part by study of the accompanying drawings, in which like reference numerals refer to like parts, and in which:

[12] **Figure 1** is a diagram of a typical system using a parallel plate DC magnetron used to sputter-deposit thin films.

[13] **Figure 2** is an enlarged view of a process chamber used in a typical parallel plate DC magnetron showing the details of particle interaction.

[14] **Figure 3** is a flow diagram of the basic steps involved in thin film deposition.

[15] **Figure 4** is a diagram of a parallel plate DC magnetron as modified to include an energy source according to one embodiment of the systems and methods for laser assisted deposition.

[16] **Figure 5** is a flow diagram of one embodiment of the systems and methods for laser assisted deposition which employs sputtering.

[17] **Figure 6** is a diagram of a sublimation chamber modified to include an energy source according to one embodiment of the systems and methods for laser assisted deposition.

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Detailed Description of the Invention

[18] The systems and methods for laser assisted deposition overcome the aforementioned manufacturability problem by providing an energy source with a deposition apparatus that simultaneously deposits and anneals a target material onto a substrate. In one embodiment, the deposition systems and methods employ a simple parallel plate DC diode deposition apparatus. In other embodiments, the deposition apparatus may be a magnetron, an RF system, a sublimation chamber, or any other apparatus designed for manufacturing thin films.

[19] **Figure 1** is a diagram of a typical system using a parallel plate DC magnetron 100 used to sputter-deposit thin films. Cathode 105 is equipped with magnets 140 and is held at a negative potential with respect to anode 110 by DC power supply 112. Target material 135 is mounted to cathode 105 and substrate material 170 lays atop anode 110. Pressure controller 145 is attached to sputter chamber 180 via pressure control line 190. Gas inlet 115 is connected to gas supply 120 via gas supply line 125. Gas flow controller 130 also connects to gas supply line 125. Pressure controller 145 is also coupled to roughing pump 150 and turbo pump 155 via vacuum control lines 160. Finally, a network of vacuum outtake tubes 165 connects turbo pump 155 and roughing pump 150 to process chamber 180.

[20] **Figure 2** is an expanded view of process chamber 180 showing the details of particle interaction within magnetron system 100. Positively charged gas ions 205 interact with target material 135 in plasma 215. Dislodged particles 210 from target material 135 migrate toward substrate 170 through plasma 215. Target material 135 can be, for instance, a semiconductor material such as cadmium sulfide, or a metal such as copper, both used in the manufacture of solar cells. Excess matter 220 is removed from process chamber 180 through vacuum outtake 165.

[21] Cathode 105 of parallel plate DC magnetron 100 houses magnets 140 configured around and behind target material 135 to capture and restrict electrons 225 near target material 135. The purpose of magnets 140 is to cause electrons 225 from cathode 105 to spin in the magnetic field created by cathode 180 and anode 110. A single electron 225 can liberate as many as thirty new electrons 225 by impacting and ionizing inert gas atoms 205. Thus, in the dark space near the face of target material

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135, spinning electrons 225 ionize the flood of inert gas atoms 205. Ionized inert gas atoms 205, now positively charged, accelerate to collide with the surface of target material 135. The result is a higher overall deposition rate of magnetron 100 due to a greater number of positively charged ions 205 bombarding target material 135.

[22] Other embodiments of process chamber 180 include a simple parallel plate DC diode deposition apparatus having no magnets 140. As just described, magnets 140 are preferable to the extent that they improve the deposition rate. Process chamber 180, so modified to include magnets 140, is commonly called a magnetron. However, process chamber 180 may be further modified such that the electric field between cathode 105 and anode 110 is an RF (radio frequency) field. In this RF embodiment, the deposition apparatus uses RF energy to create the plasma instead of the DC field described above.

[23] The basic steps to deposition are depicted in **Figure 3**. In step 305, positively charged ions of inert gas 205 are generated in plasma 215 in high vacuum chamber 180 and accelerated toward target material 135 at a negative potential. Argon is often the inert gas of choice due to its relative abundance in earth's atmosphere. In step 310, positively charged ions 205 gain momentum and accelerate toward target material 135. Upon physical impact with target material 135 in step 315, particles from target material 135 are physically dislodged. In step 320, the dislodged particles migrate toward the surface of substrate 170. In step 325, the sputtered particles condense and form a thin film on substrate 170 with essentially the same material composition as target material 135. In step 330, excess material 320 is removed from the chamber by vacuum outtake 165. Finally, a typical thin film device manufacturing method also usually comprises a subsequent annealing phase 335 wherein the deposited layer is annealed at high temperature in order to eliminate film irregularity or repair any damage caused to the layer during deposition.

[24] The systems and methods thus far described are suitable for thin film deposition in semiconductor device fabrication situations of all types, including building metallization layers in silicon wafer processing and deposition of the thin film layers comprising a solar cell. In the manufacture of thin film solar cells in particular, annealing step 335 can serve the special purpose of crystallizing an amorphous deposited layer. Deposited layers are often amorphous; hence, the subsequent

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annealing of such a layer acts to improve the electrical and physical properties of the film by decreasing the number of defects and grain boundaries as the layer progresses toward polycrystal.

[25] Annealing is a thermal treatment usually accomplished in furnaces following layer deposition, or multi-layer deposition. Annealing furnaces typically expose devices to high heat for very long duration. Where the device is a thin film solar cell built on a plastic substrate, both high heat and long duration can cause permanent damage to the substrate. Rapid thermal annealing is an example of a technique that has been developed by process engineers to minimize the exposure of a device to extreme annealing temperatures. However, the high target temperatures reached in a rapid anneal can cause damage to plastic even though the exposure is limited in time.

[26] The systems and methods for laser assisted deposition permit the deposition of thin films on plastic substrates by merging the deposition and annealing together in one step. Combined deposition and annealing eliminates the subsequent anneal stage 335 of the thin film process of **figure 3**. Process chamber 180 is able to simultaneously deposit and anneal the thin film because the system for laser assisted deposition includes an energy source for uniformly heating the target material while it is deposited as further illustrated below.

[27] **Figure 4** is a diagram of the process chamber of **figure 2** as modified to include energy source 410 according to one implementation of the systems and methods for laser assisted deposition. In one embodiment, energy source 410 is designed to emit energy through a port 420 provided in cathode 105 and aimed at substrate 170. However, energy source 410 could be provided at any suitable position within process chamber 180. Also, the vacuum conditions created in process chamber 180 are designed to have negligible effect on the output of energy source 410.

[28] Energy source 410 may be, for instance, any of a number of tunable lasers or masers. Also, the particular type of source selected may be modulated in both beam energy density and beam center frequency. The energy density used is varied in time in synchronization with the particular layer thickness. The high level of control of the energy density is best achieved with a cw (continuous wave) laser with long temporal coherence length. It is often necessary to deposit only a very small total energy per

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square centimeter of deposition layer. Additionally, the cw beam intensity also may be slowly modulated as cell layer depth increases, using only an amount of intensity that will result in the desired temperature in the selected layer. Control over beam intensity prevents destroying the layer, which could occur if the temperature were to rise too quickly.

[29] Energy source 410 may also be a pulse laser. However, pulse lasers are much more difficult to control in energy delivery to substrate 170 since their energy is delivered in a pulse that has poor temporal coherence by comparison with cw beams. The peaked pulse of the pulse laser output makes it far less desirable as a controlled power source.

[30] In one implementation, energy source 410 is a modified solid state laser such as a Yttrium-Aluminum-Garnet (YAG) laser. In other implementations, energy source 410 is a continuous wave laser. However, the system and method for laser assisted deposition contemplates any of the many types of lasers available including those lasers categorized by the physical state of the active medium employed (i.e., gas, liquid, and solid-state), as well as those lasers categorized by their wavelength (i.e., infrared, visible, and ultraviolet). Energy source 410 is chiefly responsible for ensuring that the deposited layer is adequately annealed at the same time as it gets deposited. In effect, annealing takes place in a layer-by-layer fashion while the thin film is sputtered onto substrate 170.

[31] If energy source 410 is a continuous wave laser light source, the beam emanating from source 410 could be rapidly and continuously scanned back and forth across the film. A stationary continuous beam may cause damage to substrate 170 or to the deposited film if allowed to irradiate an isolated portion of substrate 170 or deposited layer for too long. In whatever implementation of source 410, either continuous wave or pulsed, the energy directed at the thin film surface must be substantially absorbed by the thin film layer itself with as little energy as possible passing to substrate 170. Both the fine tuning of the laser's output and/or a cooling circuit can help to achieve optimal energy absorption and protect substrate 170 in case of excessive exposure. A cooling circuit would contact the reverse side of substrate

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170 and provide a temperature differential that can be controlled to keep substrate 170 within the acceptable temperature range.

[32] In one embodiment, port 420 is a clear opening (not shown) in cathode 105 through which a laser beam is able to pass. A window covering port 420 and interfacing with chamber 180 could be used but would have to be frequently cleaned in order to prevent build-up of target material 135 and other matter from obscuring the passage of the beam. In another embodiment, the window is covered with a transparent conductive layer such as indium-tin-oxide (ITO) and charged to a negative potential for repelling particles from target material 135. This repulsion would help control or eliminate the potential build-up of matter on the window and would ease the burden of having to clean the window as frequently.

[33] The systems and methods of laser assisted deposition are easily understood from the process flow diagram of **figure 5**. In step 505, positively charged ions of inert gas 205 are generated in plasma 215 in high vacuum chamber 180 and accelerated toward target material 135 held at a negative potential. As before, argon gas is frequently chosen for inert gas 205 because it is abundant and inexpensive. In step 510, positively charged ions 205 gain momentum and accelerate toward target material 135. Upon physical impact with target material 135 in step 515, atoms from target material 135 are physically dislodged and upon arriving at the growing thin film layer, are uniformly heated by energy source 410.

[34] Step 520 represents a significant departure from the conventional systems and methods of deposition. Whereas deposition and annealing were two distinct steps in the method and systems of **figures 1-3**, the systems and methods of laser assisted deposition combine deposition and annealing into one step to produce a thin film layer that is simultaneously annealed while being deposited onto the substrate. The controlled heating of the deposited material in this step anneals the sputtered material at the same time it is being deposited onto substrate 170. Control of the temperature at this stage is critical. The laser light source must generate energy just adequate to ensure that the target material is annealed but without causing harm to the substrate.

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[35] In step 525, the sputtered atoms condense and form a thin film on substrate 170 with essentially the same material composition as target material 135. Finally, in step 530, excess material 220 is removed from chamber 180 by vacuum pump 165.

[36] In addition to controlling the output of energy source 410, the temperature at which laser assisted deposition is carried out must be kept sufficiently low to avoid damaging the plastic or polymer substrate 170. In one embodiment, the systems and methods for laser assisted deposition are carried out at room temperature. In another embodiment, the systems and methods for laser assisted deposition are carried out at or below the temperature above which the thin film of material crystallizes, so long as this temperature does not melt or damage substrate 170. In another embodiment, the systems and methods for laser assisted deposition are carried out below the critical temperature of substrate 170. The critical temperature of substrate 170 is the temperature at which substrate 170 begins to sustain permanent damage.

[37] The systems and methods for laser assisted deposition also allow each layer of a cell to be annealed separately as it is produced, rather than annealing an entire stack of layers simultaneously. This advantage means that less energy is used to anneal a single layer; hence, the substrate temperature rise as well as the temperature rise of the underlying layers is minimized. Individual layer annealing also reduces problems that arise due to differences in thermal expansion coefficients of the various layers because the temperature rise of the underlying layers is kept to a minimum. In another embodiment, simultaneous deposition and anneal permits annealing of a portion of the thickness of a layer at a time, further reducing the amount of heat to which the substrate is exposed.

[38] A principle purpose of the systems and methods for laser assisted deposition is to optimize the sheet resistance of the deposited layer. Since sheet resistance causes electrical losses in the cell, deposited thin films should have a sheet resistance as low as possible. One way to reduce sheet resistance involves increasing the thickness of the film. The disadvantage to thicker films, at least in the context of solar cells, is reduced flexibility; and in some instances, a thicker cell may undesirably alter the cell's optical absorption properties. Laser assisted deposition is a superior method of improving sheet resistance, which uses a laser beam to control annealing energy without causing

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the substrate to overheat. All else being equal, the simultaneous annealing disclosed as part of the systems and methods for laser assisted deposition generates films of very low sheet resistance without increasing the thickness of the film. The result is a film of superior crystalline structure having, in addition to a low sheet resistance, a finer structure and larger grain size without high temperature processing.

[39] The systems and methods for laser assisted deposition can be used to create thin film solar cells on a flexible or plastic substrate such as disclosed in pending U.S. Patent Application Serial No. 09/892,131 and said Application is fully incorporated by reference herein as though included in its entirety. Sputter depositing a thin film of the compound semiconductor CdTe has proven difficult; therefore, the systems and methods for laser assisted deposition contemplate the use of sublimation techniques to grow a CdTe absorption layer. Sublimation can be used, however, to grow any layers of a cell, including metallization layers, as an alternative or companion process to sputtering.

[40] **Figure 6** is a diagram of a typical sublimation chamber 600 modified to include an energy source according to one embodiment of the system and method for laser assisted deposition. Sublimation chamber 600 comprises crucible 610, sublimation material 620, energy source 630, and vacuum outtake 660. Sublimation material 620 can be, for instance, solid state CdTe for use in depositing a CdTe thin film onto substrate 170, according to one embodiment. Sublimation can also be carried out using pure cadmium and pure telluride rather than depositing compound CdTe. Sublimation in this manner could require two crucibles 610 to separately store the cadmium and the telluride.

[41] Sublimation includes converting a substance directly from a solid to a gas. Solid material 620 is thus converted to a gas 670 in chamber 600 wherein appropriate vacuum pumps are attached to chamber 600.

[42] Energy source 630 simultaneously anneals gas particles 670 concurrent with their deposition onto substrate 170. As before, energy source 610 can be a maser or laser or any other source regardless of categorization by active medium or wavelength. Continuous wave, rasterized, or pulsed energy is likewise acceptable.

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[43] Temperature control can be accomplished using a cooling circuit that would maintain a temperature differential at substrate 170 in order to prevent damage to substrate 170. Cooling is also critical during sublimation to ensure that the deposited layer of gas particles 670 are annealed without causing harm to substrate 170.

[44] One or more metallization layers using the systems and methods for laser assisted deposition may also be necessary to provide current collection for the cells. Metallization layers as well as semiconductor layers may be deposited using sublimation. Proof-of-principle lab results have yielded solar cells built on high temperature flexible substrates such as mylar, tedlar, teflon, and tefzel using the techniques described herein. By flexible is meant a sheet of finished cells that can be rolled to a minimum inside radius of about four inches such that when unrolled, the cells will not suffer degradation or damage. Also, the selection of a very heat tolerant substrate will produce a cell with higher efficiency because it is possible to raise annealing temperature to higher levels.

[45] The description and drawings contained herein represent the presently preferred embodiment of the invention and are, as such, a representative of the subject matter which is broadly contemplated by the present invention. The scope of the present invention fully encompasses other embodiments that may become obvious to those skilled in the art, and the scope of the present invention is accordingly limited by nothing other than the appended claims.

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WHAT IS CLAIMED IS

1. A system for depositing a thin film comprising:

a chamber having a cathode and an anode for generating an electric field therebetween;

a gas intake for injecting an inert gas into the chamber;

a target material affixed to the cathode and exposed to the inert gas whereby positively charged inert gas particles dislodge particles from the target material;

an energy source for generating energy inside the chamber; and

a substrate affixed to the anode on which substrate the dislodged particles from the target material are deposited to form the thin film and on which the energy from the energy source simultaneously anneals the thin film without damaging the substrate.

2. The system of claim 1, wherein the cathode contains magnets.

3. The system of claim 1, wherein the electric field is an RF (radio frequency) field.

4. The system of claim 1, wherein the electric field is a DC (direct current) field.

5. The system of claim 1, wherein the energy source is a laser.

6. The system of claim 5, wherein the laser is a pulsed laser.

7. The system of claim 6, wherein the pulsed laser is activated for a duration short enough to avoid damaging the substrate.

8. The system of claim 5, wherein the laser is a continuous wave laser.

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9. The system of claim 8, wherein the continuous wave laser is scanned back and forth over an upper surface of the thin film to avoid damaging the substrate.

10. The system of claim 1, wherein the inert gas is argon (Ar).

11. The system of claim 1, further comprising a pump for creating and maintaining vacuum conditions in the chamber.

12. The system of claim 1, further comprising a vacuum outtake for removing excess matter from the chamber.

13. The system of claim 1, further comprising a cooling circuit for controlling the temperature of the substrate.

14. The system of claim 1, wherein the substrate is plastic.

15. The system of claim 14, wherein the plastic substrate is one of the group consisting of tedlar, tefzel, mylar, and teflon.

16. The system of claim 1, wherein the target material is a semiconductor.

17. The system of claim 16, wherein the semiconductor target material is one of the group consisting of cadmium telluride (CdTe) and cadmium sulfide (CdS).

18. The system of claim 1, wherein the target material is a metal.

19. The system of claim 18, wherein the metal target material is one of the group consisting of indium-tin-oxide (ITO), copper (Cu), and silver (Ag).

20. A system for depositing a thin film comprising:

a chamber;

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a crucible housed within the chamber for storing a sublimation material;

an energy source for generating energy inside the chamber; and

a substrate mounted in the chamber, on which substrate gas particles from the sublimation material are deposited to form the thin film and on which the energy from the energy source simultaneously anneals the thin film without damaging the substrate.

21. The system of claim 20, wherein the energy source is a laser.

22. The system of claim 21, wherein the laser is a pulsed laser.

23. The system of claim 22, wherein the pulsed laser is activated for a duration short enough to avoid damaging the substrate.

24. The system of claim 21, wherein the laser is a continuous wave laser.

25. The system of claim 20, further comprising a pump for creating and maintaining vacuum conditions in the chamber.

26. The system of claim 20, further comprising a vacuum outtake for removing excess matter from the chamber.

27. The system of claim 20, further comprising a cooling circuit for controlling the temperature of the substrate.

28. The system of claim 20, wherein the substrate is plastic.

29. The system of claim 20, wherein the sublimation material is a semiconductor.

30. The system of claim 29, wherein the semiconductor material is cadmium telluride (CdTe).

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31. A method of depositing a thin film comprising:
sputtering a thin film of material onto a substrate; and
simultaneously directing energy from an energy source at the thin film for annealing of the thin film.

32. The method of claim 31, wherein the substrate is a polymer or plastic.

33. The method of claim 31, wherein the energy source is a laser.

34. The method of claim 33, wherein the laser is a pulsed laser.

35. The method of claim 33, wherein the laser is a continuous wave laser.

36. The method of claim 31, wherein energy from the energy source is directed at the thin film and is at a temperature below the critical temperature of the substrate to avoid damaging the substrate.

37. The method of claim 31, wherein the thin film of material is a semiconductor.

38. The method of claim 37, wherein the semiconductor is one of the group consisting of cadmium telluride (CdTe) and cadmium sulfide (CdS).

39. The method of claim 31, wherein the thin film of material is a metal.

40. The method of claim 39, wherein the metallization layer is one of the group consisting of Indium-Tin-Oxide (ITO), Copper (Cu), and Silver (Ag).

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41. The method of claim 31, wherein the steps of sputtering the thin film and directing an energy source both occur in a process chamber having a cathode and an anode for creating an electric field therebetween.

42. The method of claim 41, wherein the electric field is an RF (radio frequency) field.

43. The method of claim 41, wherein the electric field is a DC (direct current) field.

44. A method of depositing a thin film comprising:

sublimating a thin film of material onto a substrate; and

simultaneously directing energy from an energy source at the thin film for annealing of the thin film.

45. The method of claim 44, wherein the substrate is a polymer or plastic.

46. The method of claim 44, wherein the energy source is a laser.

47. The method of claim 46, wherein the laser is a pulsed laser.

48. The method of claim 46, wherein the laser is a continuous wave laser.

49. The method of claim 44, wherein energy from the energy source is directed at the thin film and is at a temperature below the critical temperature of the substrate to avoid damaging the substrate.

50. The method of claim 44, wherein the thin film of material is a semiconductor.

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51. The method of claim 50, wherein the semiconductor is cadmium telluride (CdTe).

52. The method of claim 44, wherein the thin film of material is a metal.

53. The method of claim 52, wherein the metal is one of the group consisting of Indium-Tin-Oxide (ITO), Copper (Cu), and Silver (Ag).

54. A method of manufacturing solar cells comprising the steps of:

depositing a semiconductor layer onto a substrate;

simultaneously annealing the semiconductor layer as the layer is deposited on the substrate by directing energy from an energy source onto the semiconductor layer; and

depositing a current-collecting metallization layer onto the semiconductor layer or substrate.

55. The method of claim 54, wherein simultaneously annealing comprises directing the energy from the energy source onto the semiconductor layer for a duration long enough to noticeably increase the grain size of the semiconductor layer.

56. The method of claim 54, wherein the energy source is a laser.

57. The method of claim 54, wherein the substrate is plastic.

58. The method of claim 57, wherein the plastic substrate is one of the group consisting of mylar, tedlar, teflon, and tefzel.

59. A solar cell comprising:

a flexible substrate;

an n-type window layer deposited at a temperature sufficiently low so as not to damage the substrate; and

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a p-type absorption layer deposited using sublimation at a temperature sufficiently low so as not to damage the substrate.

60. The solar cell of claim 59, wherein the p-type absorption layer comprises cadmium telluride deposited at a temperature sufficiently low to avoid crystallization of the cadmium telluride.

61. The solar cell of claim 59, wherein the n-type window layer comprises cadmium sulfide sputter deposited at a temperature sufficiently low to avoid crystallization of the cadmium sulfide.

62. A thin film flexible solar cell comprising:

a plastic or polymer substrate;

a thin film of n-type cadmium sulfide deposited at a temperature sufficiently low so as not to damage the substrate; and

a comparatively thicker film of p-type cadmium telluride deposited using sublimation at a temperature sufficiently low so as not to damage the substrate.

63. A thin film flexible solar cell comprising:

a flexible substrate;

a current collection layer deposited onto the substrate;

an n-type semiconductor film that is deposited onto the current collection layer and has an amorphous atomic structure;

a p-type semiconductor film having a bandgap energy less than the n-type semiconductor film that is deposited using sublimation onto the n-type semiconductor film and has an amorphous atomic structure; and

a metallization layer deposited onto the p-type semiconductor film.

64. The thin film flexible solar cell of claim 61 wherein:

the substrate is a transparent polymer or plastic;

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the n-type semiconductor film is cadmium sulfide deposited at a temperature sufficiently low to avoid melting or damaging the substrate; and

the p-type semiconductor film is cadmium telluride deposited at a temperature sufficiently low to avoid melting or damaging the substrate.

65. A thin film flexible solar cell comprising:

a flexible substrate;

a metallization layer deposited onto the substrate;

a p-type semiconductor film that is deposited using sublimation onto the metallization layer and has an amorphous atomic structure;

an n-type semiconductor film having a bandgap energy greater than the p-type semiconductor film that is deposited onto the p-type semiconductor layer and has an amorphous atomic structure; and

a current collection layer deposited onto the n-type semiconductor film.

66. The thin film flexible solar cell of claim 65 wherein:

the substrate is a transparent polymer or plastic;

the p-type semiconductor film is cadmium telluride deposited at a temperature sufficiently low to avoid melting or damaging the substrate; and

the n-type semiconductor film is cadmium sulfide sputter deposited at a temperature sufficiently low to avoid melting or damaging the substrate.

67. A method for manufacturing a thin film flexible solar cell comprising the following steps:

(a) providing a plastic or polymer substrate;

(b) depositing a layer of an n-type semiconductor on the substrate at a temperature sufficiently low to avoid melting or damaging the substrate; and

(c) sublimating a layer of a p-type semiconductor on the n-type semiconductor layer at a temperature sufficiently low to avoid melting or damaging the substrate.

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68. The method of claim 67, wherein:

after step (a), a transparent conductive oxide layer is deposited on the substrate and a metal bar bus network is deposited on the transparent conductive oxide layer; and

after step (c), a metallization layer is deposited on the p-type semiconductor layer.

69. The method of claim 68, wherein the n-type semiconductor is cadmium sulfide and the p-type semiconductor is cadmium telluride.

70. A method for manufacturing a thin film flexible solar cell comprising the following steps:

(a) providing a plastic or polymer substrate;

(b) sublimating a layer of a p-type semiconductor on the substrate at a temperature sufficiently low to avoid melting or damaging the substrate; and

(c) depositing a layer of an n-type semiconductor on the p-type semiconductor at a temperature sufficiently low to avoid melting or damaging the substrate.

71. A method as claimed in claim 70, wherein steps (b) and (c) are carried out at a temperature sufficiently low to avoid crystallization of the semiconductors.

72. A method as claimed in claim 70, wherein the p-type semiconductor is cadmium telluride and the n-type semiconductor is cadmium sulfide.

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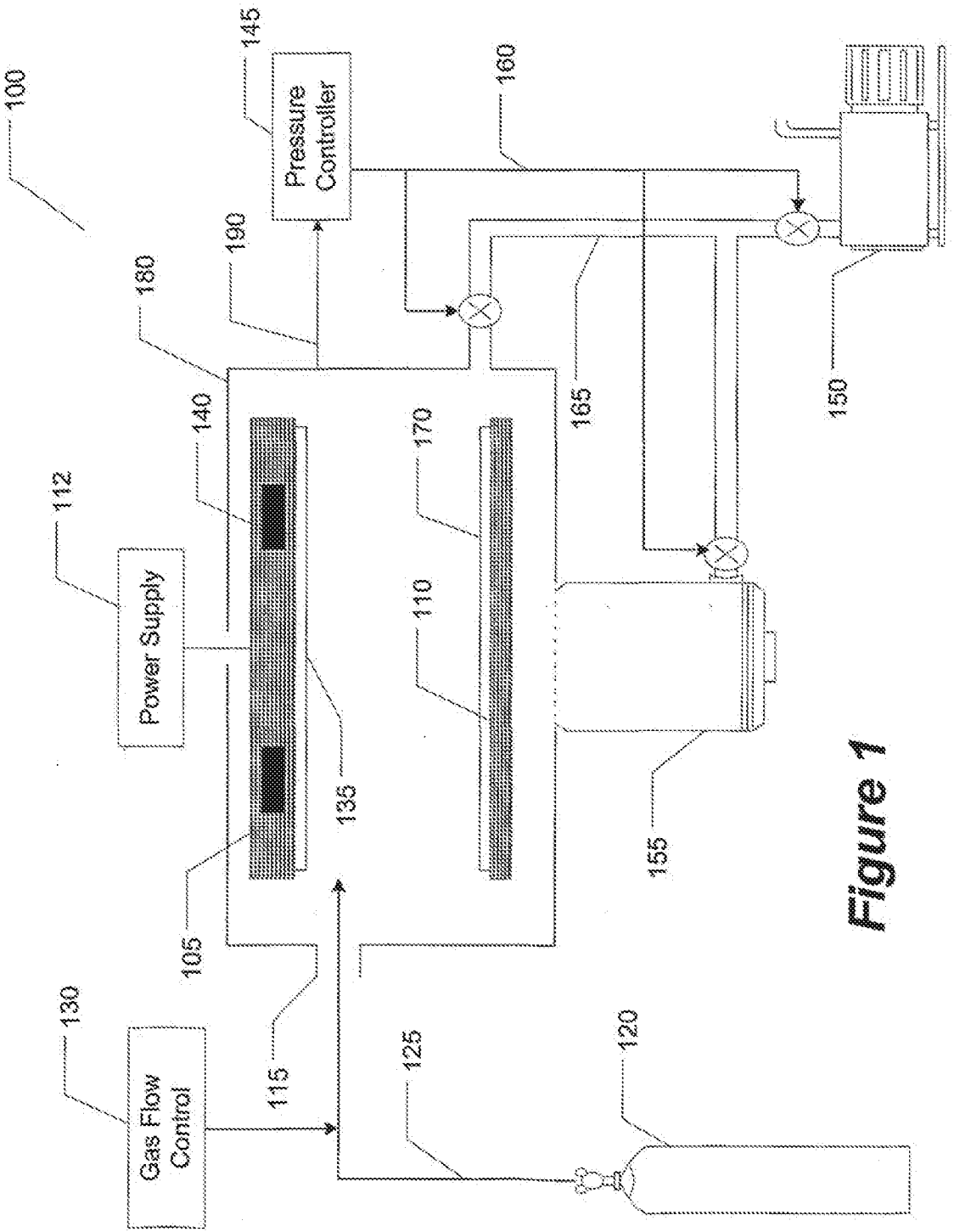


Figure 1

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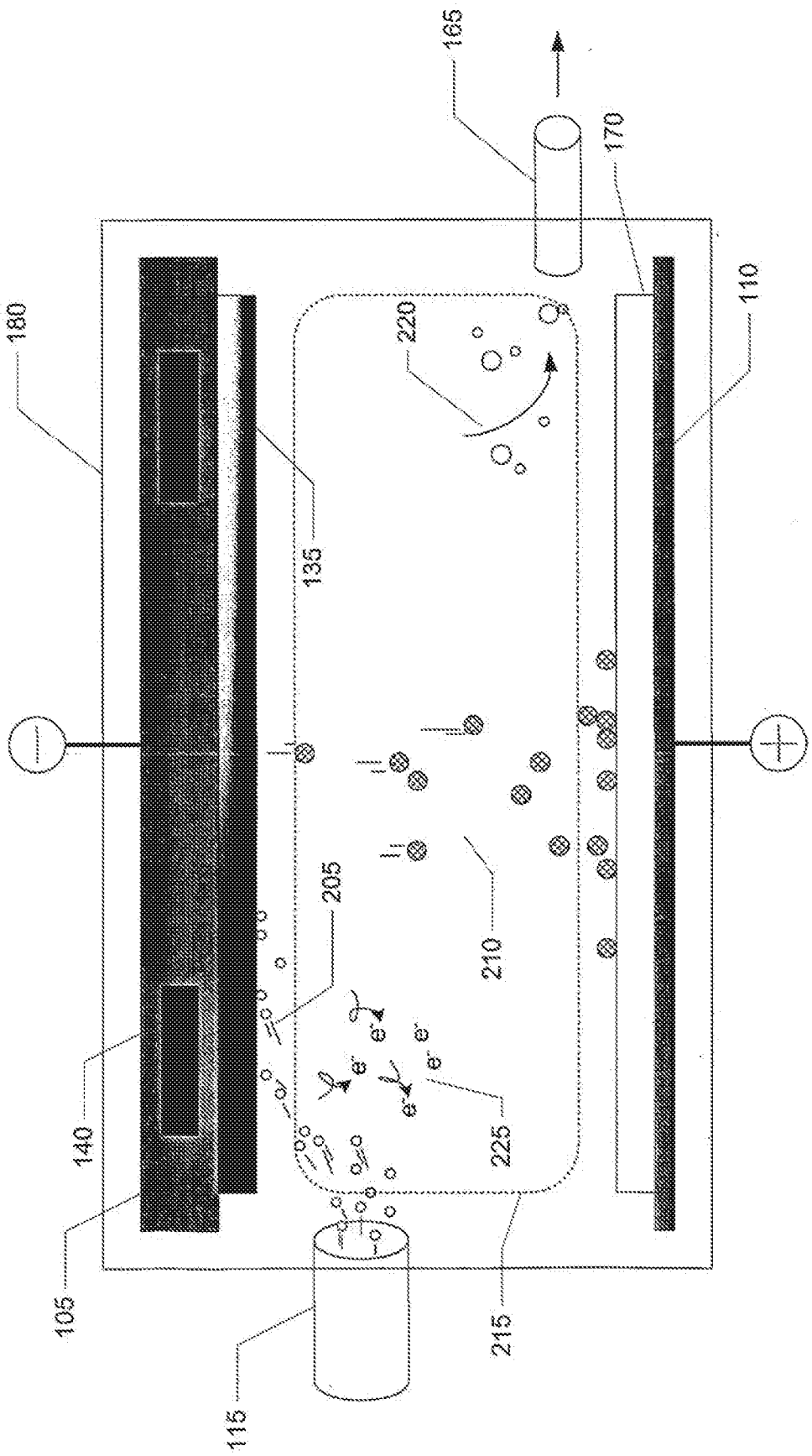


Figure 2

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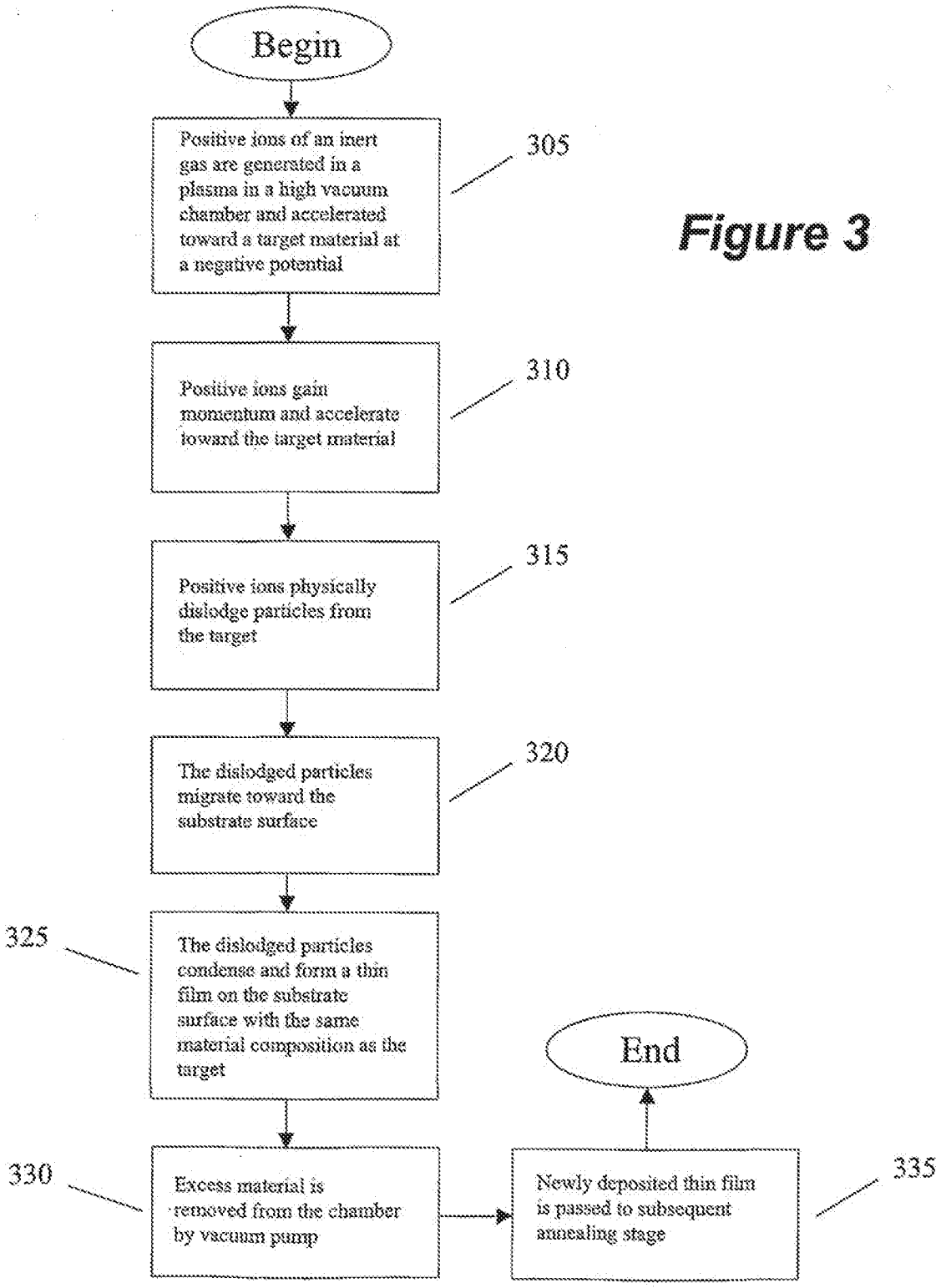

Begin
Positive ions of an inert gas are generated in a plasma in a high vacuum chamber and accelerated toward a target material at a negative potential
305
Positive ions gain momentum and accelerate toward the target material
310
Positive ions physically dislodge particles from the target
315
The dislodged particles migrate toward the substrate surface
320
The dislodged particles condense and form a thin film on the substrate surface with the same material composition as the target
325
Excess material is removed from the chamber by vacuum pump
330
Newly deposited thin film is passed to subsequent annealing stage
335
End

Figure 3

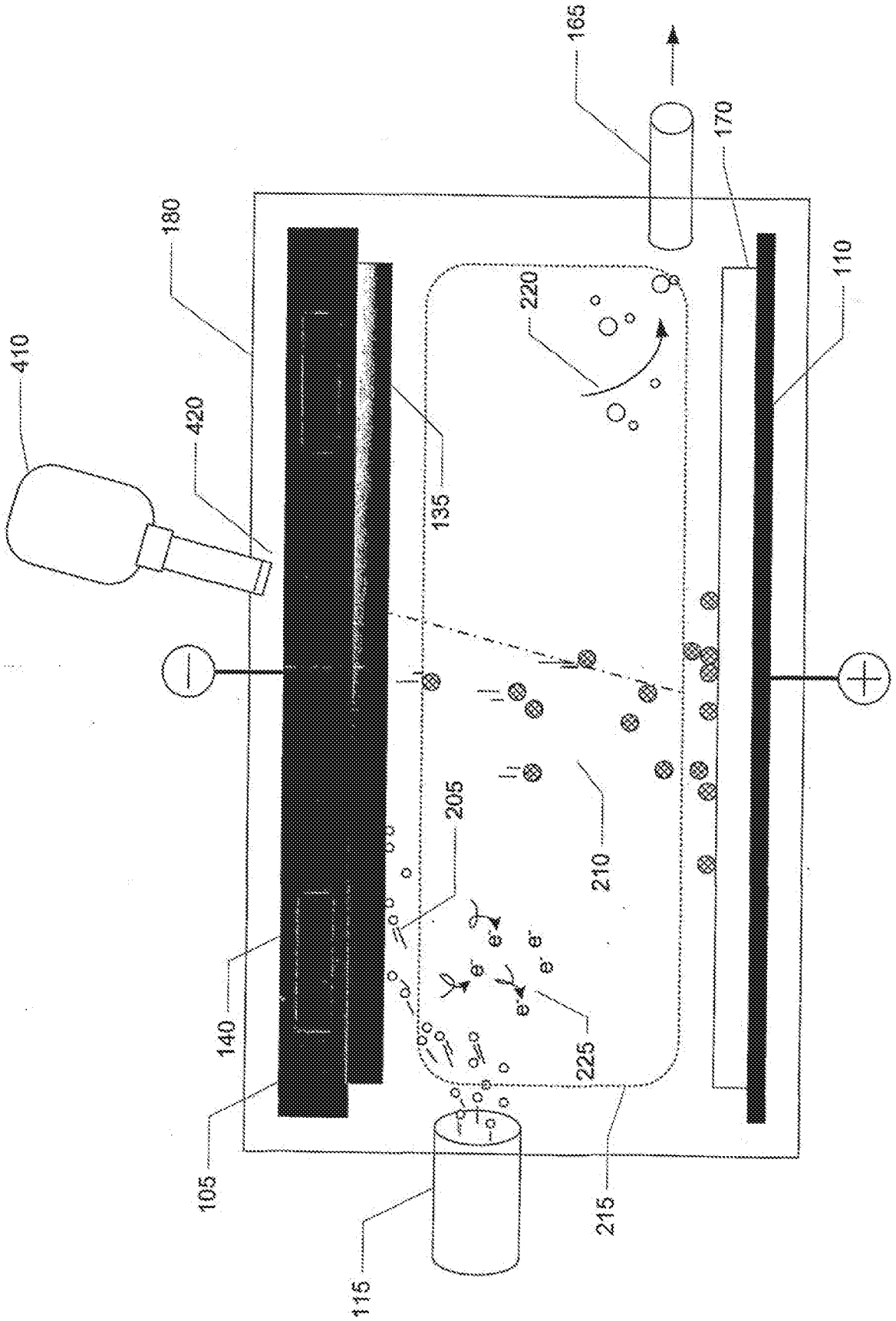


Figure 4

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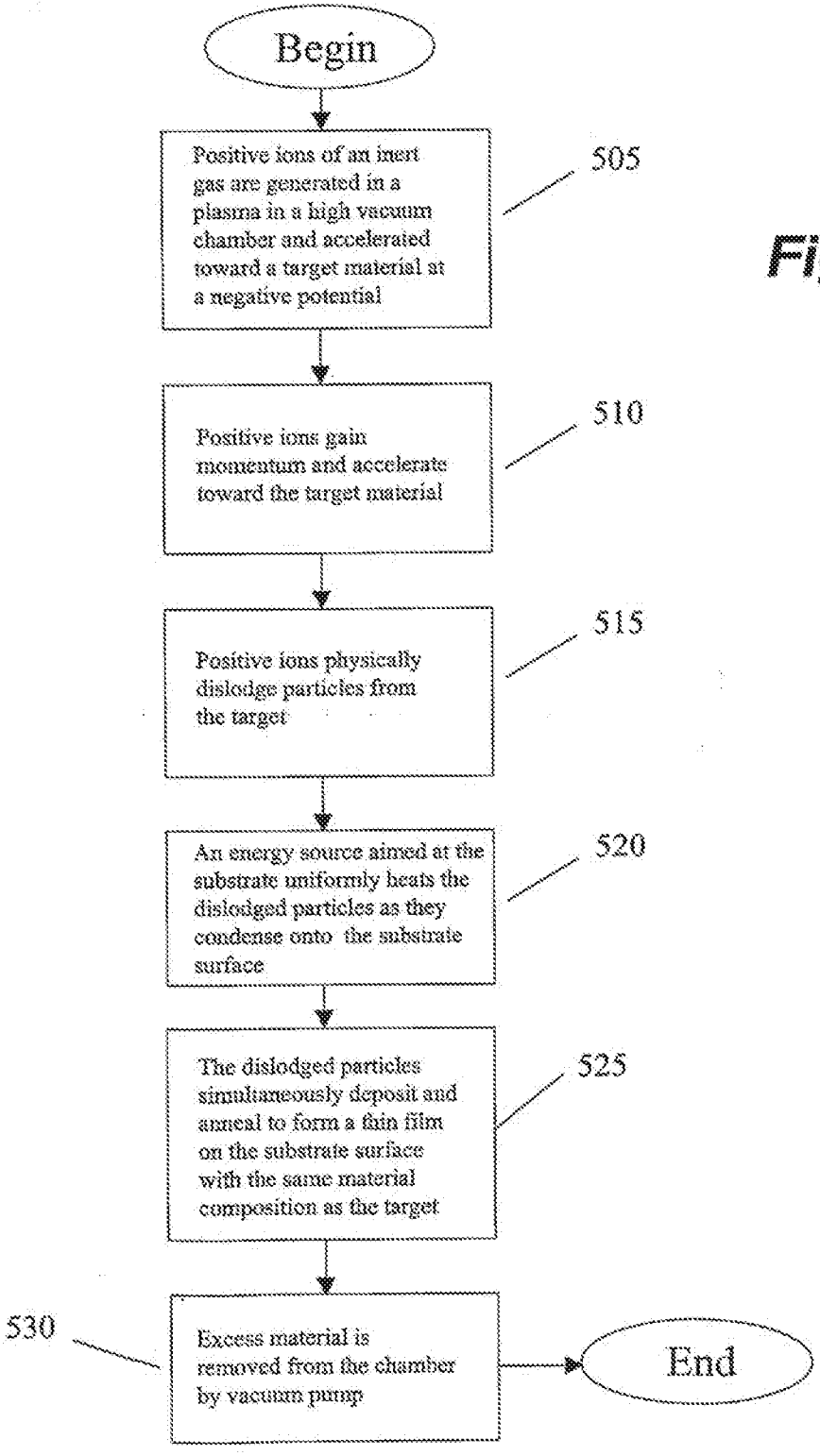


Figure 5

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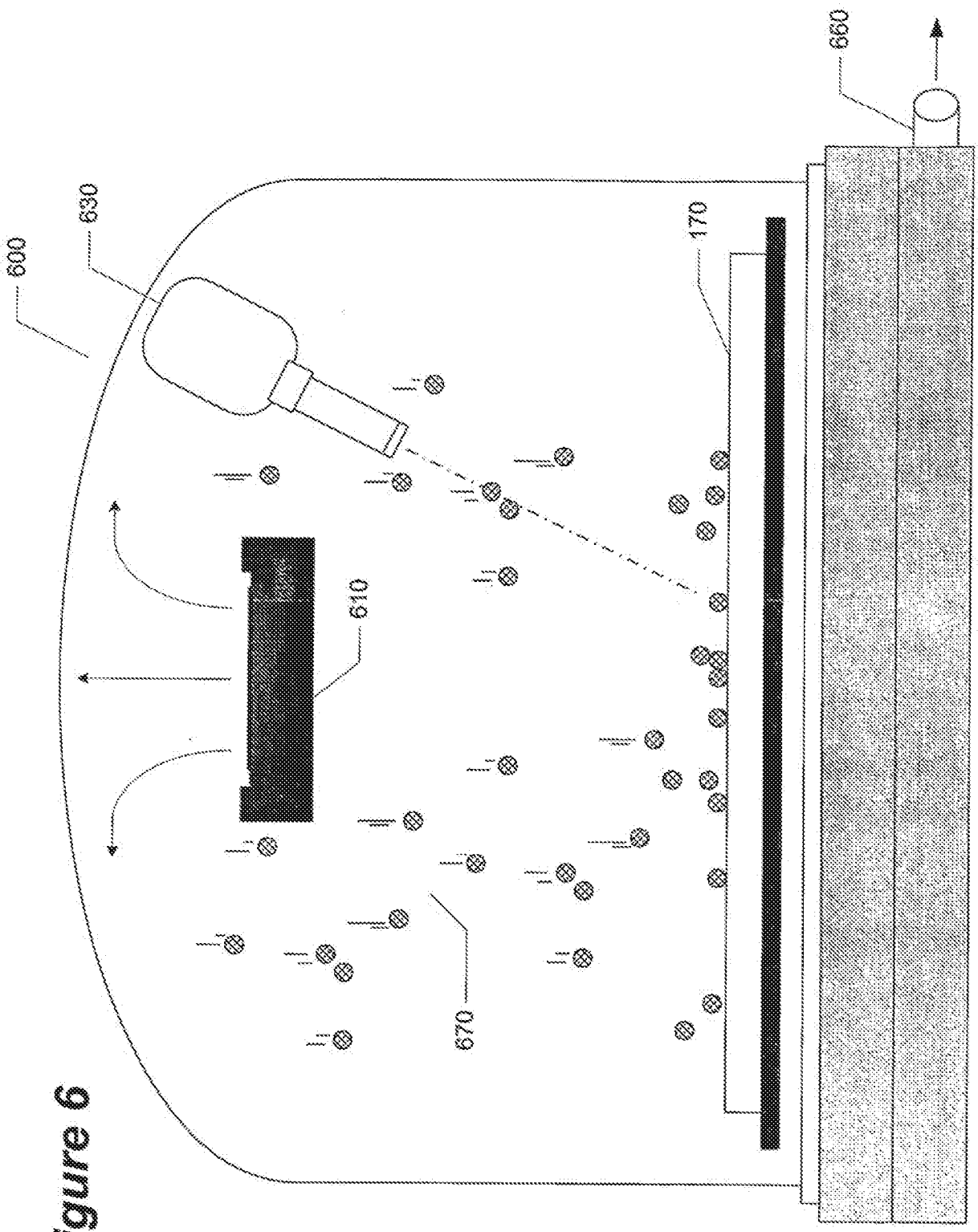


Figure 6

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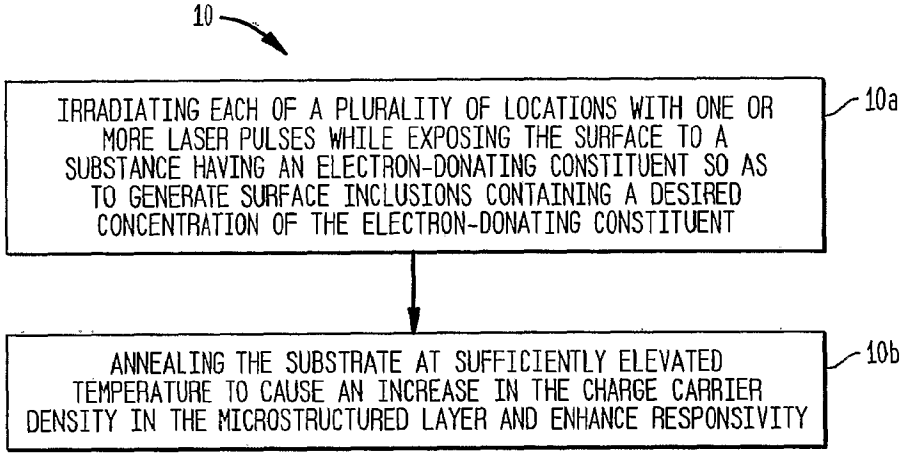
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(54) Title: MANUFACTURE OF SILICON-BASED DEVICES HAVING DISORDERED SULFUR-DOPED SURFACE LAYERS



(57) Abstract: The present invention provides methods of fabricating a radiation-absorbing semiconductor wafer by irradiating at least one surface location of a silicon substrate, e.g., an n-doped crystalline silicon, by a plurality of temporally short laser pulses, e.g., femtosecond pulses, while exposing that location to a substance, e.g., SF_6, having an electron-donating constituent so as to generate a substantially disordered surface layer (i.e., a microstructure layer) that incorporates a concentration of that electron -donating constituent e.g., sulfur. The substrate is also annealed at an elevated temperature and for a duration selected to enhance the charge carrier density in the surface layer. For example, the substrate can be annealed at a temperature in a range of about 700 K to about 900 K.

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MANUFACTURE OF SILICON-BASED DEVICES HAVING DISORDERED SULFUR-DOPED SURFACE LAYERS

Federally Sponsored Research

The invention was made with Government support under contract DE-FC36-016011051 awarded by Department of Energy (DOE). The Government has certain rights in the invention.

Related Applications

The present application is a continuation-in-part (CIP) of co-pending patent application entitled "Systems and Methods for Light Absorption and Field Emission Using Microstructured Silicon," filed on May 24, 2002, and having a Serial No. 10/155,429, which is herein incorporated by reference in its entirety.

Background of the Invention

The present invention relates generally to methods for fabricating radiation-absorbing semiconductor wafers, and more particularly, to methods for fabricating silicon wafers that can absorb radiation and exhibit diodic current-voltage characteristics.

Modern semiconductor circuits are predominantly based on silicon, which can be readily procured at a lower cost than any other semiconductor and can be easily oxidized. Further, a band gap of 1.05 eV renders silicon suitable for detection of visible light and conversion of sunlight into electricity. Silicon, however, has several shortcomings. For example, it is an indirect band-gap material, and hence it is a relatively poor light emitter. In addition, silicon is not particularly suitable for use in detecting radiation having long wavelengths, such as, infrared radiation employed for telecommunications. Although other semiconductor materials are available that can detect long wavelength radiation better than silicon, they are generally more costly and cannot be readily integrated in optoelectronic circuits that are primarily silicon-based.

Hence, there is a need for silicon-based semiconductor structures and wafers with enhanced radiation-absorbing properties, particularly in wavelengths beyond the band-gap of crystalline silicon. There is also a need for such wafers that can be utilized

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in fabricating photodetectors that exhibit enhanced responsivity in detecting radiation over a wide wavelength range. Further, there is a need for methods of manufacturing such silicon-based wafers.

Summary of the Invention

In one aspect, the present invention provides a method of fabricating a radiation-absorbing semiconductor wafer by irradiating at least one surface location of a silicon substrate, e.g., a crystalline silicon, with a plurality of temporally short laser pulses while exposing that location to a substance having an electron-donating constituent so as to generate a substantially disordered surface layer that incorporates a desired concentration of the electron-donating constituent, e.g., a concentration in a range of about 0.5 atom percent to about 5 atom percent, or from about 0.5 atom percent to about 1 atom percent. The substrate is preferably annealed at an elevated temperature and for a duration selected to enhance charge carrier density, e.g., electron carrier density, in the disordered surface layer.

In a related aspect, an annealing temperature and duration can be selected to cause re-arrangement of atomic bonds in the surface layer so as to increase the concentration of free electrons in the surface layer. Further, the annealing temperature and duration can be selected to cause the surface layer to form a diode junction, e.g., a p-n junction, with the underlying silicon substrate. The term "diode junction" is known in the art and generally refers to a junction that can exhibit current rectification (e.g., a junction that exhibits drastically different conductivities in one bias direction relative to the other). Moreover, the annealing temperature and duration can be selected such that the annealed substrate would exhibit a responsivity in a range of about 1 Ampere/Watt (A/W) to about 200 A/W, or preferably in a range of about 10 A/W to about 200 A/W, upon exposure of the surface layer to visible radiation having wavelengths in a range of about 250 nm to about 1050 nm and application of a reverse bias in a range of about 0.1 V to about 15 V, or about 0.5 to about 15 V, to the substrate. Further, the annealing temperature and duration can be selected such that the annealed substrate will exhibit a responsivity in a range of about 0.1 Ampere/Watt (A/W) to about 100 A/W upon exposure of the surface layer to visible radiation having at least a wavelength in a range

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of about 1050 nm to about 3500 nm and application of a reverse bias in a range of about 0.1 V to about 15 V to the substrate.

In a related aspect, the laser pulses irradiating the substrate's surface have pulse widths in a range of about a few nanoseconds to about 10 femtoseconds, and more preferably in a range of about 50 to about 500 femtoseconds. The laser pulse fluences can range from about 1 kJ/m^2 to about 30 kJ/m^2, or from about 3 kJ/m^2 to about 15 kJ/m^2, or from about 3 to about 8 kJ/m^2. The annealing temperature can be in a range of about 500 K to about 1100 K, preferably in a range of about 500 K to about 900 K, and more preferably in a range of about 700 K to about 900 K, and the annealing duration can be from about a few seconds to about a few hours.

In another aspect, the substance containing an electron-donating constituent can be a gas, a fluid or a solid. Some examples of such substances include, without limitation, SF_6, H_2S, Cl_2, and N_2. For example, when SF_6 is utilized, the exposure of the silicon surface to the laser pulses generates sulfur inclusions in a surface layer of the substrate. The silicon substrate is preferably n-doped, but it can also be p-doped. The substrate's bulk doping level can be in a range of about 10^{11} to about 10^{18} cm^{-3}.

In another aspect, the present invention provides a method of fabricating a radiation-absorbing semiconductor structure that calls for irradiating each of a plurality of locations on a surface of a silicon substrate with one or more femtosecond laser pulses while exposing the surface to a sulfur-containing substance so as to generate a plurality of sulfur inclusions in a surface layer of the substrate. The substrate is annealed at a temperature in a range of about 500 K to about 1100 K for a time duration in a range of about a few seconds to about a few hours. The annealing step can be performed subsequent to, or simultaneously, with irradiation of the substrate's surface with laser pulses. Further, the annealing step can be performed in an inert atmosphere or in vacuum (i.e., a low-pressure atmosphere).

In a related aspect, the light emitted in each laser pulse can have a narrow spectrum and a central wavelength in a range of about 200 nm to about 1200 nm (e.g., 800 nm or 1064 nm), fluences in a range of about 1 kJ/m^2 to about 30 kJ/m^2, and more preferably in a range of about 1 kJ/m^2 to about 10 kJ/m^2 ,and a repetition rate in a range of about 1 kHz to about 50 MHz, or in a range of about 1 kHz to about 1 MHz.

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In another aspect, the invention provides a method of fabricating a semiconductor wafer by irradiating a plurality of locations on a surface of a silicon substrate with one or more laser pulses having pulse widths in a range of about 50 to about 500 femtoseconds while exposing the surface to a substance having an electron-donating constituent so as to generate a microstructured surface comprising inclusions that incorporate the electron-donating constituent. The laser pulses can be directed at the substrate in a direction forming a selected angle relative to the substrate's surface, e.g., normal to the surface. The substrate is annealed at an elevated temperature in range of about 500 K to about 1100 K for a selected time duration, e.g., in a range of about a few seconds to about a few hours. In certain applications, the annealing temperature can be between about 500 K and 1000 K, and more preferably between 575 K and 875 K.

In another aspect, the invention provides a method of fabricating a semiconductor wafer by irradiating at least one location on a surface of a silicon substrate with temporally short laser pulses, e.g., femtosecond pulses, while exposing the surface to a substance having an electron-donating constituent so as to generate a microstructured surface layer having inclusions containing the electron-donating constituent. The substrate can be annealed, either following the laser irradiation or simultaneous therewith, at a temperature and for a duration selected to enhance the responsivity of the microstructured substrate to electromagnetic radiation having at least one wavelength in a range of about 250 nm to about 1100 nm by a factor of about 10, or preferably about 20, or more preferably about 100, relative to a similarly microstructed substrate but without annealing. The responsivity can be measured upon application of a reverse bias voltage in a range of about 0.5 V to about 15 V to the substrate. A suitable annealing temperature for effecting such enhancement of the wafer's responsivity lies in a range of about 600 K to about 900 K, and more preferably in a range of about 700 K to about 900 K, and a suitable annealing duration lies in a range of about a few seconds to about a few hours.

In another aspect, the present invention provides a photodetector that includes a silicon substrate having a surface layer, configured for exposure to external radiation, that is doped with sulfur inclusions with an average concentration in a range of about 0.5 atom percent to about 5 atom percent so as to exhibit a diodic current-voltage characteristic. The photodetector further includes a plurality of electric contacts, e.g., in

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the form of metallic coatings, that are disposed on selected portions of the substrate for applying a selected reverse bias voltage, e.g., in a range of about 0.1 to about 15 volts, to the surface layer for facilitating generation of an electrical signal, e.g., a photocurrent, in response to exposure of the surface layer to electromagnetic radiation. The surface layer is configured such that an electrical signal in response to an incident radiation having at least a wavelength in a range of about 250 nm to about 1050 nm can be generated at a responisivity greater than about 1 A/W. Preferably, the responsivity over the entire range of about 250 nm to about 1050 nm is greater than about 1 A/W. For example, the responsivity to at least one wavelength in this wavelength span, and preferably to all wavelengths in this span, can be in a range of about 1 A/W to about 100 A/W, or in a range of about 10 A/W to about 100 A/W, or in a range of about 10 A/W to about 200 A/W.

In another aspect, the photodetector can exhibit an average responsivity (i.e., responsivity averaged over a wavelength range) to wavelengths in a range of about 250 nm to about 1050 nm that is greater than about 1 A/W, e.g., an average responsivity in a range of about 1 A/W to about 100 A/W, or an average responsivity in a range of about 10 A/W to about 200 A/W.

In another aspect, the photodetector can exhibit a responsivity greater than about 1 A/W (e.g., in a range of about 1 A/W to about 100 A/W) for wavelengths in a range of about 250 nm to about 600 nm, as well as in a range of about 600 nm to about 1050 nm. In a related aspect, the photodetector can exhibit a responsivity greater than about 0.1 A/W for incident radiation having at least one wavelength in a range of about 1050 nm to about 2000 nm, and preferably in a range of about 1050 nm to about 3500 nm. Preferably, the photodetector's responsivity to all wavelengths in this range (about 1050 nm to about 3500 nm) is greater than about 0.1 A/W. For example, the detector's responsivity in this wavelength span can be in a range of about 0.1 A/W to about 100 A/W.

In another aspect, the photodetector can exhibit an average responsivity greater than about 0.1 A/W (e.g., a responsivity in a range of about 0.1 A/W to about 100 A/W) for radiation having wavelengths in a range of about 1050 nm to about 2000 nm, and preferably in a range of about 1050 nm to about 3500 nm.

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Photodetectors according to the teachings of the invention, such as those described above, provide a marked improvement over conventional silicon photodiodes where responsivities greater than 1 A/W for wavelengths in a range of about 250 nm to about 1050 nm are unknown. Further, responsivities of conventional silicon photodiodes degrade drastically for wavelengths beyond 1050 nm, and are significantly less than those that can be achieved by photodetectors of the present invention.

In another aspect, the surface layer can have a thickness in a range of about 10 nanometers to about 1 micron, and a microstructured morphology. For example, the microstructured layer can be formed by a plurality of conical microstructures, each of which can be composed of a core silicon portion forming a junction with a surface portion that is doped with sulfur. A term "conical structure or microstructure" as used herein refers to a generally cone-like or columnar protrusion above the silicon surface that can have vertical walls, or slanted walls that taper in the vertical direction. The microstructures can have a height in a range of about 0.5 micron to about 30 microns protruding from a base portion on the surface of the silicon substrate to a tip portion having a radius of curvature of about a few hundred nanometers. The gradient of sulfur concentration across the junction is substantially abrupt, although in some cases it can be gradual with the core portion having some sulfur dopants. The sulfur-doped surface layer can comprise silicon nanocrystals having diameters in a range of about 10 about 50 nanometers.

In another aspect, the invention provides a photodetector that includes a silicon substrate having a microstructured layer incorporating inclusions containing an electron-donating constituent. The microstructured layer is adjacent an underlying bulk silicon portion and forms a diode junction therewith. The term "diode junction" is known in the art and generally refers to a junction that can exhibit current rectification (e.g., a junction that exhibits drastically different conductivities in one bias direction relative to the other). A well-known example of a diode junction is a p-n junction. An electrical contact is disposed on a surface portion of the microstructured layer such that at least another surface portion of that layer remains available for receiving incident electromagnetic radiation. The photodetector can further include another electrical contact disposed on a surface of the bulk silicon portion opposed to the microstructured layer. The electrical contact layers allow application of a reverse bias voltage to the

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substrate to facilitate generation of an electrical signal, e.g., a photocurrent, in response to exposure of the microstructured layer to incident radiation having wavelengths in range of about 250 nm to about 1050 nm at a responsivity in a range of about 1 A/W to about 200 A/W.

In a related aspect, the substrate can generate a photocurrent in response to irradiation of the microstructured layer with radiation having wavelengths in a range of about 1050 nm to about 3500 nm at a responsivity in a range of about 0.1 A/W to about 100 A/W.

In another aspect, the electron-donating constituent can be, for example, sulfur, chlorine or nitrogen, and can be present in the microstructured layer at a concentration in a range of about 0.5 to about 5 atom percent, or in a range of about 0.5 to about 1.5 atom percent, or in a range of about 0.5 to about 1 atom percent.

In another aspect, the present invention provides a photodetector for use in the visible and the infrared regions of the electromagnetic spectrum that includes a crystalline silicon substrate having a microstructured surface layer characterized by a plurality of substantially conical microstructures. The microstructured layer includes a doped layer having a plurality of silicon nanocrystals that contain an electron-donating dopant, such as sulfur, chlorine or nitrogen, with an average concentration in a range of about 0.5 to about 1.5 atom percent. The microstructured layer exhibits a diodic current-voltage curve and is configured to receive an external radiation. A plurality of electrical contacts are disposed on selected portions of the substrate for applying a reverse bias voltage to the microstructured layer in order to facilitate generation of an electrical signal in response to irradiation of at least a portion of that layer. The photodetector exhibits a responsivity greater that about 1 amperes/watt (A/W) for radiation wavelengths in a range of about 250 nm to about 1050 nm and a responsivity greater than about 0.1 amperes/watt for radiation wavelengths in a range of about 1050 nm to about 3500 nm.

Further understanding of the invention can be obtained by reference to the following detailed description in conjunction with the associated drawings, which are briefly described below.

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Brief Description of the Drawings

FIGURE 1 is a flow chart depicting various steps in an exemplary embodiment for generating a microstructured silicon wafer suitable for absorbing radiation,

FIGURE 2 is a schematic diagram of an exemplary apparatus for microstructuring silicon wafers in accordance with one aspect of the invention,

FIGURE 3 is a scanning electron micrograph of a silicon surface, obtained at a 45-degree angle relative to the surface, after irradiation of the surface with 100 fsec pulses having a central wavelength of 800 nm and a fluence of about 5 kJ/m^2,

FIGURE 4 schematically illustrates an experimental set-up for performing resistivity and Hall effect measurements on a silicon sample microstructured in accordance with the teachings of the invention,

FIGURE 5 presents a plurality of graphs depicting wavelength absorptance of prototype microstructured silicon wafers as a function of an average number of 100 laser shots (8 kJ/m^2) per location employed for microstructuring the wafers in the presence of SF_6,

FIGURE 6 presents a plurality of graphs depicting wavelength dependence of absorptance of a plurality of prototype silicon wafers annealed at different temperatures subsequent to their microstructuring by a plurality of femtosecond laser pulses (the room temperature (300 K) data corresponds to a wafer that was not annealed),

FIGURE 7 presents graphs depicting wavelength dependence of absorptance for exemplary femtosecond-laser-formed and nanosecond-laser-formed microstuctured silicon wafers, before and after thermal annealing at 875 K for about 30 minutes (the absorptance of an unstructured silicon substrate as a function of wavelength is also shown for comparative purposes),

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FIGURE 8A presents graphs depicting absorptance as a function of wavelength for a plurality of prototype silicon wafers microstructured by exposure to 500 laser shots of femtosecond pulses (fluence of 8 kJ/m^2) in the presence of different gases in the absence of annealing (the graph designated vacuum relates to wafer microstructured in a vacuum chamber at a base pressure less than about 10^{-6} bar),

FIGURE 8B presents absorptance data as a function of wavelength for a plurality of prototype silicon wafers microstructured by exposure to 500 shots of 100 femtosecond laser pulses (fluence of 8 kJ/m^2 in the presence of sulfur-bearing and non-sulfur-bearing gases) indicating the positive effects of sulfur incorporation in enhancing below band-gap absorptance,

FIGURE 9 presents graphs depicting wavelength dependence of absorptance for a plurality of prototype silicon wafers microstructured by femtosecond laser pulses in the presence of SF_6 at different partial pressures,

FIGURE 10 schematically illustrates a p-n junction in thermal equilibrium,

FIGURE 11A is a perspective view of a photodetector formed in accordance with one embodiment of the invention,

FIGURE 11B is a side view of the photodetector depicted in FIGURE 11A,

FIGURE 12 presents graphs depicting current-voltage characteristics of a plurality of exemplary silicon wafer microstructured by exposure to femtosecond laser pulses in the absence of annealing as well as in the presence of annealing at different annealing temperatures,

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FIGURE 13 presents graphs depicting responsivity of a plurality of silicon wafers microstructured by exposure to femtosecond laser pulses in the presence of SF_6 (with no annealing and with annealing at different temperatures) as a function of wavelength in comparison with that of a commercial photodiode illustrating that a significantly enhanced responsivity can be obtained by judicious annealing of wafers subjected to laser microstructuring,

FIGURE 14 present graphs depicting current-voltage characteristics of a plurality of exemplary prototype silicon wafers microstructured by femtosecond laser pulses at different laser fluences and each annealed at 825 K,

FIGURE 15A presents comparative responsivity measurements for prototype silicon wafers microstructured by femtosecond laser pulses at different fluences and each annealed at 825 K for about 30 minutes,

FIGURE 15B presents comparative responsivity measurements for prototype silicon wafers microstructured by femtosecond laser pulses at different fluences and each annealed at 1075 K for about 30 minutes,

FIGURE 16A presents current-voltage characteristics for n-doped and p-doped silicon substrates microstructured by exposure to femtosecond laser pulses at a fluence of 6 kJ/m^2 followed by annealing at 825 K for about 30 minutes,

FIGURE 16B presents current-voltage characteristics for n-doped and p-doped silicon substrates microstructured by exposure to femtosecond laser pluses at a fluence of 4 kJ/m^2 followed by annealing at 1075 K for about 30 minutes,

FIGURE 17A presents responsivity measurements for prototype exemplary n-doped and p-doped silicon substrates microstructured at two different laser fluences (4 kJ/m^2 and 6 kJ/m^2) and annealed at 825 K for about 30 minutes,

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FIGURE 17B presents responsivity measurements for prototype exemplary n-doped and p-doped silicon substrates microstructured by femtosecond laser pulses at a fluence of 4 kJ/m^2 and annealed at 1075 K for about 30 minutes,

FIGURE 18 presents a graph depicting responsivity as a function of back bias for an n-doped silicon substrate microstructured via irradiation by femtosecond laser pulses at a fluence of 4 kJ/m^2 and annealed at 825 K for about 30 minutes (the measurement was performed by employing a white light source with an approximate power of 50 microwatts),

FIGURE 19A presents graphs depicting current-voltage characteristics of an n-doped silicon sample microstructuured by femtosecond laser pulses at a fluence of 4 kJ/m^2 and annealed at 825 K as a function of operating temperature,

FIGURE 19B presents a graph depicting the responsivity of a microstructured silicon wafer to incident radiation having a wavelength of 1064 nm as a function of operating temperature,

FIGURE 20 illustrates current-voltage characteristics for a high resistivity (resistivity greater than 1 Ohm-m) microstructured silicon wafer that can be utilized as a solar cell, with and without one sun illumination,

FIGURE 21 illustrates current-voltage characteristics for a low resistivity (e.g., a resistivity in a range of about 0.01 to about 0.1 Ohm-m) microstructured silicon wafer that can be utilized as solar, with and without one sun illumination,

FIGURE 22 schematically depicts an exemplary experimental set-up for measuring field emission of a silicon substrate microstructured in accordance with the teachings of the invention, and

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FIGURE 23 shows a graph depicting field emission current generated by a silicon wafer microstructured by exposure to femtosecond laser pulses in the presence of SF_6 as a function of a potential difference applied thereto.

Detailed Description

With reference to a flow chart 10 of FIGURE 1, in one aspect, the present invention provides a method of fabricating a radiation-absorbing semiconductor structure in which, in an initial step 10a, each of a plurality of locations on a surface of a silicon substrate is irradiated with one or more laser pulses while exposing the surface to a substance having an electron-donating constituent so as to generate surface inclusions containing a concentration of the electron-donating constituent. The laser pulses can have a central wavelength in a range of about 200 nm to about 1200 nm, and a pulse width in a range of about tens of femtoseconds to about hundreds of nanometers. Preferably, the laser pulse widths are in a range of about 50 femtoseconds to about 50 picoseconds. More preferably, the laser pulse widths are in the range of about 50 to 500 femtoseconds. The number of laser pulses irradiating the silicon surface can be in a range of about 2 to about 2000, and more preferably, in a range of about 20 to about 500. Further, the repetition rate of the pulses can be selected to be in a range of about 1 kHz to about 50 MHz, or in a range of about 1 kHz to about 1 MHz. Moreover, the fluence of each laser pulse can be in a range of about 1 kJ/m^2 to about 12 kJ/m^2, and more preferably in a range of about 3 kJ/m^2 to about 8 kJ/m^2.

While in some embodiments, the electron donating constituent is a fluid (gas or liquid), in other embodiments it can be a solid deposited over the silicon surface exposed to laser pulses. By way of example, in some embodiments, the silicon surface can be exposed to a sulfur-containing gas (e.g., SF_6 or H_2S) while irradiated with the laser pulses. In some other embodiments, Cl_2 or N_2 is employed as the electron-donating substance with which the silicon surface is in contact during laser irradiation. In yet other embodiments, selenium or tellurium can be employed. Without any loss of generality, in the following discussion, it is assumed that SF_6 is employed as the substance containing an electron-donating constituent, and that the irradiating pulses have femtosecond pulse widths, unless otherwise indicated. However, it should be clear to those having ordinary skill in the art that various embodiments of the invention

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described below can also be practiced with other fluids or solids and laser pulses having other pulse widths, such as those listed above.

In some embodiments, the silicon substrate is p-doped (e.g., doped with Boron) with a doping level in a range of about 10^{11} to about 10^{18}. In other embodiments, the silicon substrate is slightly n-doped (e.g., doped with Phosphorus) with a doping level in a range of about 10^{11} to about 10^{18}, and preferably in a range of about 10^{12} to about 10^{15}. The substrate thickness is not typically a critical parameter, and can be in a range of about 2 microns to about 1000 microns. The substrate can have an electrical resistivity in a range of about 0.001 ohm-m to about 10 ohm-m.

FIGURE 2 schematically depicts an exemplary apparatus 12 that can be utilized for irradiating a silicon sample with a plurality of femtosecond pulses. The apparatus 12 includes a sample processing chamber 14 that comprises a stainless steel cube 16 with Conflat flange connections on each of its six sides. A three-axis, precision motion controller 18 is attached to the back side of the cube. This controller contains two orthogonal micrometer precision axes driven by computer controlled motors. The third axis is hand-controlled with about 1 mil precision. The controller can translate a one-inch diameter stainless steel rod 20 that supports a 2-inch diameter mounting magnet 22 in the center of the cube to which a magnetizable sample holder can be mounted. A two-stage roughing pump 24 is coupled to the cube to evacuate the chamber to a base pressure of approximately 10^{-3} torr. Two pressure gauges 26 and 28 are employed to monitor the chamber's pressure. A leak valve 30 and a gas-handling manifold (not shown) allow introduction of gases of interest into the chamber. An optical grade, 4.5 inch quartz window 32 is attached to the front of the chamber for providing laser access. Further, a quick-access viewport door 34 allows rapid loading and removal of samples as well as safe viewing of the sample during microstructuring.

In this exemplary apparatus, a regeneratively amplified, femtosecond Ti:Sapphire laser system (not shown) provides approximately 100 fs laser pulses having a central wavelength of 800 nm at a repetition rate of 1 kHz. The laser pulses are focused by a anti-reflection coated, plano-convex lens 36 (e.g., having a focal length of about 250-nm) through the quartz window onto the sample surface. In this exemplary embodiment, the lens is mounted on a single axis linear translation stage and positioned such that its focal point is behind the sample. By moving the lens, and hence its focal

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point, the laser spot size can be varied at the sample surface (e.g., from a diameter of about 30 microns to 250 microns). In order to measure the laser spot size, a CCD (charge coupled device) camera 38 can be placed at the same distance as the sample surface from the lens. A flipper mounted mirror 40 can redirect the laser beam onto the camera to determine its spot size on the sample surface. A second CCD camera 42 can measure reflections of light generated by a white light fiber lamp 44 from the sample surface to monitor progress during microstructuring.

In one exemplary mode of operation, samples attached to a magnetizable sample holder can be loaded through the access door and attached to the mounting magnet. Samples can be then positioned in the center of the magnet to allow for maximum translation. The chamber can be evacuated to a base pressure of 10^{-3} torr and then filled to the desired pressure with an ambient gas (e.g., 0.67 bar of sulfur hexafluoride). The sample can then be irradiated with a 1-kHz train of 100-femtosecond 800-nm laser pulses. The fluence of each pulse can be set by selecting a spot size (e.g., 150 microns) and employing a waveplate/polarizing cube combination to vary the pulse energy. Either a single spot can be irradiated, or more typically the sample can be translated by utilizing the motion controller relative to the laser beam. For example, the sample can be translated in a raster scan pattern. An average number of pulses irradiating a given spot on the sample can be controlled by utilizing a shutter and varying the horizontal translation speed.

The irradiation of the silicon surface with the laser pulses in the presence of SF_6 at a selected partial pressure, for example, a partial pressure in a range of about 0.005 bar to about 1 bar, can cause formation of a sulfur-rich layer having a sulfur concentration in a range of about 0.1 atom percent to about 5 atom percent, and more preferably, in a range of about 0.5 atom percent to about 1 atom percent. This sulfur-rich layer exhibits an undulating surface morphology (topography) with micron-sized surface height variations. Such a textured surface obtained by irradiating a silicon surface with a plurality of temporally short laser pulses in the presence SF_6 (or other substances having an electron-donating constituent) is herein referred to as a micro-structured surface. By way of example, FIGURE 3 shows a scanning electron micrograph (SEM) of a such a micro-structured silicon surface (obtained in a direction forming a 45 degree angle relative to the surface) after irradiation of the silicon surface

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with an average of 5 shots of femtosecond laser pluses (100 femtoseconds) at a wavelength of 800 nm and having a fluence of 8 kJ/m2 in 0.67 bar of SF_6.

The sulfur-rich layer can be a substantially disordered layer that is several hundred nanometers thick and made up of nanocrystallites (e.g., about 10 – 50 nm in diameter) and nanopores. Selected area diffraction (SAD) measurements indicate that the surface layer retains a substantial crystalline order with a strong possibility that amorphous-like material is present between the nanocrystalline grains. Further, SAD measurements performed on silicon substrates exposed to either 10 or 500 pulses per location indicate that the substrate below the disordered layer comprises substantially undisturbed crystalline silicon (when a crystalline silicon substrate is utilized). Further, Rutherford backscattering spectroscopy (RBS) and energy dispersive X-ray (EDX) emission spectroscopy performed on such exemplary substrates show a large concentration of sulfur is present in the disordered layer (about 1 atom percent). Further, RBS spectra obtained from silicon samples exposed to different femtosecond (100 femtoseconds) laser shots per irradiation location show that the concentration of sulfur increases with increasing laser pulse numbers up to about 50 pulses. In particular, thc measured sulfur concentration increases from about 0.2 atom percent for a sample exposed to 2 pulses per location to about 0.7 atom percent for a sample exposed to 50 laser pulses per location with the sulfur concentration exhibiting a plateau for laser pulses higher than about 50. It should be, however, understood that the above experimental results are provided simply for further elucidation of salient features of the invention, and not as limiting the scope of the invention. For example, higher sulfur concentrations in the disordered layer than those described above can also be obtained, and higher laser shots per location can be utilized.

A number of factors can affect the morphology of the microstructured surface. For example, samples microstructured by irradiating a portion thereof with laser pulses, without moving them relative to the laser beam (i.e., single spot irradiation), exhibit a subtle difference in their morphology relative to samples microstructured by irradiating a plurality of their surface locations via translation relative to the laser beam. With the rest of the experimental parameters left the same, there are two visible differences between translated and stationary samples. The microstructures in the stationary samples have a micrometer-sized sphere at the tip while the translated samples are

sharper and lack the spheres. Further, the translated samples have a larger amount of nanoscale particles spread across the microstructured surface.

In addition, the wavelength of the irradiating laser pulses, their fluence, and pulsewidths can also affect the morphology of the microstructured surface. For example, in a number of prototype samples microstructured by femtosecond pulses, with increasing the fluence (at constant shot number) the morphology showed a transition from laser-induced periodic surface structures, to a coarsened surface, to sharp microstructures, such as those depicted in the above FIGURE 3. As the laser pulse fluence increases, there is typically an increase in both the microstructure height and distance between the microstructures. In general, the fluence is preferably selected to be above a threshold fluence that would cause melting (e.g., 1.5 kJ/m^2). At very high fluences (e.g., greater than 12 kJ/m^2), material removal can become extreme and gaussian-shaped holes, rather than conical structures, can be formed in the surface.

Although in many embodiments described herein, femtosecond laser pulses are employed, in other embodiments, the microstructuring of the surface can also be achieved by employing picosecond or nanosecond pulses. For example, a number of silicon samples were microstructured by utilizing a train of 248-nm, 30-ns laser pulses with a flat-top spatial profile and a fluence of 30 kJ/m^2 generated by a KrF+ excimer laser in the presence of 1 bar of SF_6 (an average of 1500 pulses per spot were employed). The nanosecond-laser-formed microstructures showed some similarities and some differences relative to the femtosecond-laser-formed microstructures. In both cases, the microstructures were roughly conical, but the structures formed with the femtosecond laser pulses were smaller and more densely packed. For example, the femtosecond structures were roughly 8 microns tall and separated by about 4 microns while the nanosecond-formed structures were roughly 40 microns tall and separated by about 20 microns. Further, the femtosecond-formed structures were covered with nanoparticles 10 – 50 nm in diameter while the surface of the nanosecond-formed structures were much smoother.

Sample silicon wafers exposed to picosecond pulses (e.g., 10 picosecond) in the presence of SF_6 also showed a microstructured surface. The average separation between the microstructures exhibited a decrease from about 100 femtosecond pulse widths to

about 5 picosecond pulse widths but then showed an increase for pulse widths longer than about 5 picoseconds.

The laser wavelength can also affect the final morphology of the microstructures. By way of example, a prototype silicon sample microstructured with a train of 400 nm pulses exhibited a higher density of microstructures (but smaller) than those generated by 800 nm pulses at a similar fluence.

Other factors that can affect the microstructures' morphology include laser polarization and laser propagation direction relative to the irradiated silicon surface. For example, the direction of microstructure growth is parallel to the direction of incident light, and appears to be independent of the substrate's crystallographic planes. The base of microstructure can have an elliptical shape with the long axis perpendicular to the polarization of the irradiating laser light. Without being limited to any theory, this elliptical shape can be understood as being due to a higher absorption of p-polarized light relative to s-polarized light. For circularly polarized light, there is no preferential ablation, and the base of the microstructures can be substantially circular.

The fluid or solid in contact with the silicon surface during its microstructuring can also affect the resultant surface morphology. For example, utilizing SF_6 or Cl_2 as the ambient gas can lead to sharp-tipped conical structures with a radius of curvature of about 500 nm. In contrast, structures made in air, N_2 or vacuum are much more rounded (the radius of curvature of their tips is approximately 2 – 3 microns) than those made in these halogen-containing gases. In a number of exemplary samples microstructured in the presence of different gases, those made in SF_6 exhibited the greatest density of microstructures followed by those made in Cl_2. The microstruture densities produced in the presence of N_2 were approximately equal to those made in air, but approximately a factor of two less than the densities obtained by employing SF_6.

In some embodiments, the laser microstructuring of a silicon wafer is performed in the presence of a mixture of two or more substances. For example, samples microstructured in the presence of a mixture of SF_6 and Cl_2 exhibited an increase in the microstructure density at higher partial pressure of SF_6.

The sulfur-rich mircrostructured layer has unique optical and electrical properties. For example, it can exhibit a sheet charge carrier density in a range of about 10^{12} cm^{-2} to about 10^{14} cm^{-2}. By way of example and only for illustrative purposes, the

results of some resistivity and Hall effect measurements performed on a number of exemplary microstructured samples, each formed in an n-doped silicon substrate in accordance with the teachings of the invention, such as those described above, are presented below. For resistivity and Hall effect measurements, the van der Pauw technique, well-known to those having ordinary skill in the art, was employed. Briefly, four ohmic electrical contacts were formed on the disordered microstructured layer. The electrical contacts were formed by initially dipping a microstructured sample in a 5% HF solution for 5 minutes to remove any native oxide layer. Subsequently, with a mask covering all but the very corners of a selected microstructured surface area (e.g., a 10 x 10 mm^2 surface area), chromium/gold (Cr/gold) was evaporated onto the surface to form metal contacts at the exposed corners. A dicing saw was then used to cut slivers (e.g., 0.25 mm slivers) from each side. Cutting the sample edges ensures that the contacts are only connected to the surface layer and not the substrate layer. Finally, a wire bonder is utilized to connect the contacts on the corners of the sample to four Cr/Au contact pads evaporated onto a glass slide. It should be understood that this experimental arrangement, shown schematically in FIGURE 4, is sensitive primarily to the electronic properties of the microstructured layer, and not that of the substrate.

With continued reference to FIGURE 4, the resistivity measurements can be performed by applying a small DC current (e.g., 10 microamperers) from corner 2 to corner 1 while measuring a voltage from corner 3 to corner 4. Hall effect measurements can be performed by placing the sample in a strong magnetic field (e.g., a field of several thousand gauss) with the magnetic field perpendicular to the silicon surface. In one experiment, a small AC current (about 1-2 microamperes) was then applied from contact 1 to contact 3 while measuring an induced voltage across contacts 2 and 4. Control measurements were also performed on an n-doped (resistivity = 8 – 12 ohm-m) unstructured silicon wafer. Table 1 below lists the results of these measurements for microstructured layers formed in an n-doped silicon wafer having a resistivity in a range of about 8 – 12 ohm-m at a number of different laser pulse fluences.

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Original doping	Average fluence (kJ/m^2)	Doping after structuring	Sheet resistance Rs (Ohm)	Sheet carrier density n_s (cm^{-2})	Hall mobility μ ($cm^2V^{-1}s^{-1}$)
n	unstructured	-	31931	$1.78x10^{11}$	1101
n	4.0	n	4865	$7.37x10^{12}$	174
n	6.0	n	4992	$7.15x10^{12}$	175
n	8.0	n	6253	$4.52x10^{12}$	221
n	10.0	n	4554	$8.83x10^{12}$	155

This data shows that microstructured layer exhibits a higher sheet carrier density than the original substrate, but a lower carrier mobility – presumably as a result of the disorder in the microstructured layer.

Referring again to the flow chart 10 of FIGURE 1, subsequent to irradiation of the silicon surface with a plurality of laser pulses (step 10a), the substrate can annealed (step 10b) at a sufficiently elevated temperature for a selected time duration so as to cause an increase in the charge carrier density in the microstructured layer, e.g., by a factor in a range of about 10 percent to about 200 percent. For example, the substrate can be annealed at a temperature in a range of about 500 K to about 1100 K, and more preferably, in a range of about 500 K to about 900 K, for a selected time duration, e.g., a time duration in a range of about a few minutes to about a few hours (e.g., one-half hour).

The annealing step can be performed by employing a variety of different techniques. For example, the substrate can be placed in a thermal oven to be exposed to an elevated temperature for a selected duration. Alternatively, the substrate can be exposed to laser radiation, e.g., radiation having a wavelength in a range of about 200 to about 1200 nm, to cause its heating to a desired temperature. Further, the annealing step can be performed, for example, in an inert atmosphere (e.g., an argon atmosphere) or in a vacuum (a low-pressure environment). Alternatively, the annealing step can be applied simultaneously with the irradiation step. That is, the irradiation of the silicon substrate with the laser pulses can be performed while the substrate is maintained at an elevated temperature.

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Without being limited to any theory, the annealing step is designed to cause a rearrangement of the atomic bonds within the metastable microstructured layer to enhance the density of charge carriers – electrons – within that layer. The term "charge carrier density" is known to those having ordinary skill in the art. To the extent that any further explanation may be required, it refers to density of those charged particles, e.g., electrons, that are primarily responsible for current conduction, e.g., electrons in the conduction band states or in shallow impurity states below the conduction band. Such charged carriers are also herein referred to as free electrons or holes.

In other words, the annealing temperature and duration are selected to cause structural changes in the microstructured layer that result in increasing the carrier density in that layer while substantially maintaining responsivity of the layer for generating an electrical current when exposed to radiation within a selected wavelength range at a given applied back bias voltage, as discussed in more detail below. The structural changes caused in the microstructured sulfur-rich layer by an annealing step according to the teachings of the invention can be appreciated by considering that in many embodiments in which a p-doped silicon substrate is exposed to a plurality of laser pulses to generate a microstructured surface layer thercin, holes, rather than electrons, constitute the dominant charge carriers even after incorporation of about 1 atom percent sulfur having two possible donor electrons per atom. However, after annealing, electrons can constitute the dominant charge carriers in the microstructured layer. Without being limited to any particular theory, such observations suggest that sulfur in the microstructured layer, before annealing, is incorporated in silicon such that its donor electrons do not substantially contribute to conduction (the donor electrons are likely locked up in a trap, or perhaps the coordination number of the implanted sulfur is larger than four). An annealing step according to the teachings of the invention causes atomic bond rearrangements in the microstructured layer so as to free up donor electrons for contributing to electrical conduction. In fact, in case of p-doped silicon substrates, the number of donor electrons released during annealing can be sufficiently large to eliminate the holes as the dominant charge carriers and turn the microstructured layer into an n-doped layer having a sheet carrier concentration on the order of about 10^{14} cm^{-2}.

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A microstructured silicon wafer formed in accordance with the teachings of the invention exhibits absorption of incident electromagnetic radiation, particularly radiation having wavelengths in a range of about 250 nm to about 2500 nm. By way of example, FIGURE 5 presents absorption data for a microstructured silicon wafer (an n-Si (111) wafer having a thickness of about 260 microns and a resistivity in a range of about 8 – 12 ohm-m), each of which was generated by exposing its surface to 100 femtosecond laser pulses (2 to 500 shots per location) having a central wavelength of 800 nm and a fluence of about 8 kJ/m^2. This exemplary absorption data was recorded in a manner known in the art, prior to annealing the wafer, by employing an spectrophotometer equipped with an integrating sphere. The absorption data for an unstructured silicon wafer is also provided for comparative purposes.

This exemplary data indicates that the microstructured wafers exhibit an enhanced absorption of incident electromagnetic radiation, relative to unstructured silicon, across the entire recorded wavelength range, and particularly for wavelengths above about 1050 nm, which corresponds to the band-gap energy of crystalline silicon (1.05 eV). In the unstructured silicon, light photons having wavelengths longer than a wavelength corresponding to the band-gap energy do not contain sufficient energy to promote an electron from the valence band to the conduction band, leading to a drastic drop in absorption.

In contrast, the silicon wafers microstructured in accordance with the teachings of the invention exhibit significant absorption not only for wavelengths below the band-gap but also for those above it. In fact, the exemplary data of FIGURE 5 shows that silicon wafers structured by exposure to 20 pulses per location or higher (e.g., 500 pulses in this exemplary data set) exhibit near-unity, featureless absorption of wavelengths from about 0.4 micron to about 1 micron, a small decrease in absorption for wavelengths around about 1.05 micron (a wavelength corresponding to the band edge of unstructured silicon), and strong featureless absorption from about 1.05 microns to about 2.5 microns. It should be understood that this data is presented only for illustrative purposes, and is not necessarily intended to present the optimal absorption of a silicon wafer structured in accordance with the teachings of the invention.

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As noted above, in many embodiments of the invention, a microstructured wafer is annealed at a temperature and for a duration designed to enhance the charge carrier concentration in its microstructured layer. Such annealing can be performed at a variety of different temperatures. By way of example, FIGURE 6 schematically illustrates electromagnetic radiation absorptance data for a plurality of microstructured silicon wafers generated by utilizing 500 laser pulses per surface location (100 fs pulses at a central wavelength of 800 nm and a fluence of 8 kJ/m2) in the presence of 0.67 bar of SF_6 relative to that of unstructured silicon. Each structured wafer was annealed at a selected temperature in a range of about 575 K to about 875 K for about 30 minutes. This exemplary data shows that annealing at temperatures below about 575 K has little effect on the observed absorptance. On the other hand, such annealing performed at a temperature between about 575 K and 875 K does not substantially affect absorptance above the bandgap, but lowers the below band-gap absoptance – the higher the annealing temperature, the greater is the reduction in absorptance. It should, however, be understood that this data is only exemplary, and different results may be obtained for microstructured wafers generated by employing different parameters (e.g., difference fluence or laser shot numbers).

A microstructured silicon wafer according to the teachings of the invention can be generated not only by utilizing femtosecond pulses, but also other pulse widths (e.g., nanosecond and picosecond pulse widths). By way of example and only for illustrative purposes, FIGURE 7 illustrates exemplary absorptance graphs as a function of incident radiation wavelength for femtosecond-laser-formed and nanosecond-laser-formed microstructured silicon surfaces, before and after annealing at about 875 K for about 30 minutes, as well as that of an unstructured silicon wafer. The femtosecond-formed mircrostructures were generated by employing 100 fs laser pulses (500 shots per location) having a central wavelength of about 800 nm and a fluence of about 8 kJ/m^2. The nanosecond-formed microstructures were generated by employing 30 ns laser pulses (about 1500 shots per location) having a central wavelength of 248 nm and a fluence of about 30 kJ/m^2. It should be understood that this data is presented only for illustrative purposes and is not intended to necessarily indicate absorptance exhibited by a microstructured silicon formed in accordance with the teachings of the invention under all circumstances.

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In some embodiments of the invention, microstructuring of a silicon wafer can be accomplished in the presence of a background fluid rather than SF_6. For example, H_2S, Cl_2, N_2 or air can be utilized. By way of example, FIGURE 8A and 8B compare absorptance of some exemplary prototype microstructured silicon wafers generated by employing femtosecond laser pulses (100 fs, 800 nm, 8 kJ/m^2 and 500 shots per location) in the presence of various fluids – without an annealing step – with that of unstructured silicon. The vacuum data corresponds to microstructuring the wafer in a chamber evacuated to a base pressure that is less than about 10^{-6} bar. While all microstructured samples exhibit an enhanced absorption relative to unstructured silicon, this exemplary data shows the microstructuring in SF_6 and H_2S brings about the most dramatic change in absorptance relative to unstructured silicon. In particular, samples structured with SF_6 exhibit near-unity, substantially featureless absorptance across the entire measured spectrum.

A variety of background fluid pressures can be employed in many embodiments of the invention for generating microstructured silicon wafers. By way of example, FIGURE 9 shows absorptance data for a number of exemplary prototype microstructured silicon wafers generated in SF_6 (100 fs pulses, 800 nm, 500 shots per location) at different ambient pressures, as well as a wafer microstructured in vacuum (e.g., a pressure of less than 10^{-6}). The greatest rate of increase is observed at low pressures. In this exemplary data set, at pressures above about 27 mbar, the below band-gap absorptance does not show much variation with wavelength, while at lower pressures, it decreases with increasing wavelength.

The microstructured silicon wafers generated in accordance with the teachings of the invention, particularly those subjected to an annealing step at an elevated temperature in a range of about 500 K to about 900 K, not only exhibit enhanced absorption of electromagnetic radiation over a wide range (e.g., from ultraviolet wavelengths to near infrared), but they also exhibit voltage-versus-current profiles that are characteristic of diodes. As discussed in more detail below, these properties allow the use of such microstructured silicon wafers in fabricating photodetectors that exhibit enhanced responsivity relative to conventional silicon photodetectors.

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More specifically, a microstructured silicon layer formed in accordance with the teachings of the invention, particularly one formed by exposure of a wafer surface to laser pulses followed by, or simultaneous with, an annealing step designed to release electrons in the layer structured by the pulses, forms a diode junction, e.g., a p-n junction, with the underlying silicon substrate. It should be understood that a diode junction as used herein can also refer a junction formed between two n-doped portions having different free electron densities. As shown schematically in FIGURE 10, a p-n junction can be formed by bringing a semiconductor material having acceptor impurity atoms (p-doped) into contact with a semiconductor material having donor impurity atoms (n-doped). The difference in charge carrier concentration between the p-doped and the n-doped portions generates a diffusion potential across the junction – electrons and holes begin to diffuse across the junction to portions having a respective lower concentration. As they cross to the other side of the junction, they recombine with their oppositely charged electrical counterparts in a region very close to the junction. This migration of charge carries across the junction causes formation of space charges (immobile ions) with opposite polarities on the two sides of junction. As the number of space charges increases (positively charged for the n-type side and negatively changed for the p-type side), a potential difference builds up across the junction, which results in an electric field in a direction opposite that of the diffusion potential.

Upon reaching thermal equilibrium, a thin insulating layer is present near the junction in which charge carriers have been depleted by recombination (depletion region). A strong electric field is present in the depletion region and a large electric potential exists across this region. The junction can be reverse-biased by applying an electric field across it that reinforces this internal electric field. Such a reverse-bias voltage expands the insulating depletion region and enhances both the internal electric field and the potential difference across the junction. The junction can also be forward-biased by applying an electric field that is opposite to the internal field across it. Such a forward-bias voltage shrinks the depletion region, thereby diminishing the internal electric field and the potential difference across the junction. When forward-biased, a current flows across the junction with electrons injected into the n-doped portion and leaving from the p-doped portion. In other words, the p-n junction can act as a rectifier

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by allowing current flow in only one direction. This behavior gives rise to a current-voltage (I-V) curve characteristic of a diode.

As discussed above, a silicon wafer in which a microstructured layer is formed according to the teachings of the invention can exhibit an I-V curve characteristic of that obtained by a diode junction. Without being limited to any theory, such a current-voltage behavior can be understood by considering that the wafer includes two adjacent, yet distinct, layers: a surface layer in which a concentration of an electron-donating constituent is incorporated and an underlying substantially undisturbed silicon substrate layer. These two layers exhibit different crystalline structures, chemical compositions, and charge carrier doping concentrations. In addition, the microstructured layer has unique optical properties including high absorptance of incident electromagnetic radiation from the near ultraviolet into the near-infrared wavelengths. In one aspect, the invention employs such microstructured silicon wafers for fabricating photodiodes, as discussed in more detail below.

By way of example, FIGURE 11A schematically illustrates a photodetector 46 according to one embodiment of the invention that includes a microstructured silicon wafer 48 having a microstructured surface layer 50 that is formed in a silicon substrate 51 by irradiating a plurality of locations on a substrate's surface with short laser pulses (e.g., pulse widths in a range of about tens of femtoseconds to tens of nanoseconds) while exposing the surface to a substance having an electron-donating consitutent (e.g., SF_6). The laser-irradiated wafer is then annealed under conditions (e.g., at an elevated temperature and for a selected duration) designed to enhance concentration of electrons in the microstructured surface layer (e.g., annealing at a temperature in a range of about 500 K to about 900 K for a duration of a few minutes to a few hours).

The exemplary photodetector 46, functioning as a photodiode, also includes a plurality of metallic electrical contacts 52, which have a finger grid geometry, that are disposed on the microstructured surface layer. In addition, an electrical contact 54, in the form of a metallic coating layer, is disposed on the back surface of the silicon substrate (i.e., the undisturbed silicon surface opposite the microstructured surface) that substantially covers the entire surface. In this exemplary embodiment, a chromium/gold alloy (Cr/Au) is employed for fabricating the electrical contact. However, those having

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ordinary skill in the art will appreciate that the contacts can be formed of other metals, as well.

The metallic contacts 52 and 54 allow applying a bias voltage, e.g., a reverse bias voltage, across the wafer by employing, for example, a voltage source 56. The reverse bias voltage can reinforce the internal electrical field in the depletion layer of a diode junction formed between the microstructured layer 50 and the underlying silicon substrate 51. As discussed in detail below, the photodetector 46 can operate with small bias voltages, e.g., voltages in a range of about 0.1 V to about 15 V, with a responsivity (i.e., photocurrent generated per unit of power of incident light (amperes/watts)) that is considerably better than that typically exhibited by a conventional silicon photodetector. These attributes allow incorporating silicon photodetectors formed according to the teachings of the invention, such as the exemplary photodetector 46, into integrated silicon photo-electronic circuits as high sensitivity detectors.

In operation, radiation (i.e., photons) incident on the microstructured surface layer of the photodiode's silicon wafer is absorbed (when the radiation wavelength is in the operating range of the photodetector), e.g., by valence electrons, in the microstructured layer. The absorption of the incident radiation causes generation of electron-hole pairs. The electric field within the depletion region causes separation of the generated electron-hole pairs, especially those created at or in proximity of the diode junction, which is formed between the microstructured silicon layer and the underlying silicon substrate. The separated electron-hole pairs provide a photocurrent that is proportional to the number of incident photons (those skilled in the art appreciate that such a photocurrent is added to a generation current and a recombination current that can be inherently present in a diode junction). Hence, incident radiation can be detected, and quantified, by measuring the induced photocurrent.

A photodetector formed according to the teachings of the invention not only exhibits absorptance across a wide range of wavelengths (the absoptance is generally commensurate with that exhibited by the photodetector's microstructured silicon wafer), but it also exhibits a diodic I-V behavior. By way of example and further elucidation of the salient features of a photodetector of the invention, FIGURE 12 illustrates a plurality of graphs, each representing current as a function of bias voltage for a plurality of microstructured silicon samples prepared under different conditions in an n-doped

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silicon substrate for use as the active component of photodetectors. All samples were irradiated with a plurality of femtosecond laser pulses (800 nm, 100 fs, fluence of 4 kJ/m^2) in the presence of SF_6, but were subjected to different annealing conditions. The graph A represents the current-voltage curve associated with a microstructured sample that was not annealed. This curve is substantially linear, indicating that the junction between the microstructured layer and the underlying silicon substrate in this sample is not diodic, but is merely resistive. In other words, such a wafer is not optimal for fabricating a photodetector.

In contrast, graphs B, C, and D illustrate current-versus-voltage behavior of those microstructured silicon samples that were subjected to annealing at different temperatures (the annealing duration was about 30 minutes in all cases). This exemplary data indicates that with an increase in the annealing temperature, the measured I-V curve approaches one expected from a diode. For example, at an annealing temperature of about 825 K, the I-V curve is diodic, characterized by an exponentially increasing current for a forward bias and a smaller, less rapidly increasing current for a reverse bias. The I-V curve corresponding to an annealing temperature of about 1075 K is also diodic. However, annealing a microstructured silicon wafer for a significant duration at a very elevated temperature can lead to a degradation of the below-band gap absorptance, and hence a degradation in the performance of a photodetector utilizing such a microstructured wafer in the near-infrared. In this exemplary data set, the substrate annealed at 825 K exhibit an optimal I-V characteristic. It should, however, be understood that such very elevated annealing temperatures may be employed so long as the annealing duration is sufficiently short. In general, the annealing of a microstructured silicon wafer to be employed in a photodetector of the invention should be carefully designed (i.e., annealing temperature and duration) to cause release of electrons in the microstructured surface layer without significantly degrading the wafer's absorptance of and responsivity to incident radiation.

A photodetector of the invention, such as the above exemplary photodetector 46, exhibits a responsivity that can be superior across a wavelength range of about 250 nm to about 10 microns to that of a conventional silicon photodiode. By way of example and only for illustration and corroboration purposes, FIGURE 13 presents experimental graphs representing responsivity of exemplary photodetectors formed in accordance with

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the teachings of the invention, over a selected wavelength range, in comparison with a conventional photodiode and those fabricated by employing microstructured silicon, but with no annealing or annealing at too high a temperature. In particular, graphs A and B show that photodetecotors of the invention that employ silicon wafers microstructured by femtosecond laser pulses in the presence of SF_6 (100 fs, 800 nm central wavelength and a fluence of 4 kJ/m^2) followed by annealing at 825 K or 725 K, exhibit a significantly enhanced responsivity relative to that of a conventional commercially available silicon photodiode. In particular, these photodetectors exhibit a responsivity that is more than an order of magnitude greater that that of the conventional photodiode in a wavelength range of about 250 nm to about 1050 nm. Although the responsivity shows a decrease for wavelengths longer than the band-gap edge (i.e., wavelengths longer than about 1050 nm), nonetheless, it remains significantly higher than that exhibited by a conventional silicon detector. In fact, conventional silicon detectors typically do not operate at useful levels of responsivity at wavelengths that are longer than the band-gap edge. For example, in this exemplary illustration, the responsivity of the commercial photodiode drops steeply to about 10^{-6} A/W for wavelengths longer than about 1050 nm

Further, the responsitivy data for wafers formed according to the teachings of the invention (e.g., graphs A and B) were obtained by applying small bias voltages (e.g., a bias voltage of about –0.5 volts in this exemplary embodiment). In contrast, conventional silicon photodetectors exhibit much lower responsivities, or require much higher bias voltages (e.g., 100 to 1000 volts) and/or have more complex structures. This indicates that while photodetectors formed in accordance with the teachings of the invention can be readily incorporated in integrated silicon circuitry, the incorporation of conventional silicon detectors, which require large bias voltages, into integrated silicon circuits can be impractical.

The data depicted in FIGURE 13 also shows that proper annealing of a silicon wafer irradiated by a plurality of short laser pulses, as described above, can considerably enhance the responsivity of a photodetector that employs that wafer. In particular, a photodetector fabricated by utilizing a wafer that, though exposed to laser pulses, was not annealed, exhibits a much degraded responsivity relative to those that were subjected to an annealing step at appropriate temperatures, e.g., at 725 K or 825 K. This

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exemplary data also shows that a photodetector that incorporates a microstructured wafer annealed, subsequent to irradiation by laser pulses, at a temperature of 1075 for thirty minutes exhibits a much degraded responsitivy relative to those annealed at 725 K or 825 K.

Hence, one aspect of the invention relates to annealing a silicon wafer, subsequent to – or simultaneous with – its irradiation by a plurality of short pulses in the presence of a substance having an electron-donating constituent, under conditions that would release electrons in the microstructured layer while preserving the responsivity of the wafer for detecting electromagnetic radiation. For example, in some embodiments of the invention, the annealing temperature is selected to be in range of about 500 K to about 1100 K, and more preferably in a range of about 700 K to about 900 K, and the annealing duration is selected to be in a range of about 1 minute to about several hours, and more preferably in a range of about 5 minutes to about 30 minutes. Alternatively, higher annealing temperatures can be employed so long as the annealing duration is properly selected to avoid degrading the responsivity of the resultant annealed wafer. For example, although the above data indicates that annealing the wafer at temperature of about 1075 K for about 30 minutes may not be desirable, this annealing temperature with a lower annealing duration can be suitable for practicing the invention in certain applications. To certain extent, annealing temperature and duration are inter-related. For example, shorter annealing time at a higher temperature can be employed in certain applications.

In other words, it is not simply annealing at an elevated temperature that is required. Rather, the annealing temperature and its duration need to be properly selected to ensure that a photodetector exhibiting enhanced responsivity over a wide wavelength range can be fabricated by utilizing the annealed wafer. It has been discovered that annealing a silicon wafer subsequent to, or simultaneous with, its exposure to short laser pulses in presence of a substance having an electron-donating constituent at a temperature that is too low can lead to noisy photodiode and annealing at too high a temperature and duration can lower the wafer's response to both visible and infrared wavelengths. More specifically, the annealing temperature and duration are preferably selected to enhance the concentration of carrier electrons in the microstructured layer – formed by laser irradiation in presence of a substance having an electron-donating

constituent – by a factor in a range of about 10% to about 200% while ensuring that the resultant annealed wafer exhibits a responsivity greater than about 20 A/W at least at one wavelength, and preferably over the entire span, of a wavelength range of about 250 nm to about 1050 nm, and a responsivity greater than about 0.1 A/W at least at one wavelength, and preferably over the entire span, of a wavelength range of about 1050 nm to about 3500 nm. By way of example, in some embodiments of the invention, the annealing temperature is preferably selected to be in a range of about 700 to about 900 K.

The choice of the fluence of laser pulses irradiating a silicon wafer to generate a microstructured layer therein can also affect the performance characteristics of a photodetector that incorporates the microstructured wafer for detecting radiation. By way of example, FIGURE 14 presents exemplary data corresponding to current-voltage characteristics of a plurality of silicon wafers irradiated with a plurality of femtosecond laser pulses (100 fs, 800 nm central wavelength, 200 pulses per location) in the presence of SF_6 followed by annealing at 825 K for about 30 minutes. The laser pulse fluences, however, differed from one wafer to another. More particularly, the following laser fluences were employed: 4 kJ/m^2, 6 kJ/m^2, 8 kJ/m^2, and 10 kJ/m^2. This exemplary data indicates that increasing the fluence decreases the dark current for a given reverse bias voltage.

FIGURE 15A illustrates the responsivity of a plurality of photodetectors incorporating the above silicon wafers that were microstructured with different laser pulse flunces (the wafers were annealed at 825 K for 30 minutes). This exemplary responsivity data indicates that, in this sample set, the photodetector's responsivity decreases, and the wavelength of peak response shifts to longer wavelengths, with increasing fluence (the sample made with a fluence of 4 kJ/m^2 exhibits the highest response). By way of further illustration, FIGURE 15B presents responsivity data for photodetectors made with microstructured silicon wafers that were generated through irradiation with femtosecond pulses (100 fs, 800 nm central wavelength, 200 pulses per location) in the presence of SF_6 followed by annealing at 1075 K for about 30 minutes. The laser pulse fluences, however, varied from one sample to the next (4 kJ/m^2, 6 kJ/m^2, 8 kJ/m^2, and 10 kJ/m^2). A comparison of this data with the data presented in FIGURE 15A shows that the responsivity exhibited by the samples subjected to the higher

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annealing temperature of 1075 is much lower that that of the samples annealed at 825 K. However, the samples annealed at the higher temperature exhibit much less variation in responsivity as a function of fluence. Further, the samples annealed at 1075 K – though exhibiting a lower responsivity – are less noisy and have a higher quantum efficiency.

It should be understood that the above data is presented only for illustration purposes, and is not intended to necessarily indicate an optimal fluence under all conditions. For example, the above exemplary samples were made with an average laser shot number of about 200 pulses, and may exhibit improved characteristics with a greater shot number. In general, in various embodiments of the invention, the laser pulse fluence is selected to be greater than about 3 kJ/m^2. More preferably, the fluence is chosen to be in a range of about 3 kJ/m^2 to about 10 kJ/m^2, or a range of about 3 kJ/m^2 to about 8 kJ/m^2.

In many embodiments of the invention an n-doped silicon substrate is employed for forming a microstructured wafer, as described above. Alternatively, a p-doped silicon wafer can be utilized. By way of example, FIGURE 16A presents graphs comparing the diodic characteristics of a microstructured wafer generated according to the teachings of the invention, such as those described above, employing a p-doped silicon substrate (p-Si(100), 350 micron thick, resistivity (ρ) greater than 1 ohm-cm) with one fabricated utilizing an n-doped silicon substrate. In both cases, a laser pulse fluence of about 6 kJ/m^2, an annealing temperature of about 825 K, and an annealing duration of about 30 minutes were utilized. Similar data is presented in FIGURE 16B for p-dopend and n-doped samples annealed at 1075 K for about 30 minutes.

This exemplary data shows that the p-doped samples annealed at 825 K exhibit a higher forward bias current than equivalently generated n-doped samples. The dark current for back biases also increases more rapidly for p-doped samples. Upon annealing at 1075 K, the p-doped samples exhibit very good diodic properties with the back bias decreasing to substantially the same level as that in equivalently generated n-doped samples. Further, the forward bias current increases more rapidly, resulting in good rectification ratios. As noted above, annealing at higher temperatures can increase donor concentration from sulfur doping. Such increase in the donor concentration can lead p-doped samples annealed at higher temperature to exhibit better rectification.

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A silicon substrate's doping can also affect the responsivity of a silicon wafer formed by microstructuring that substrate in accordance with the teachings of the invention. By way of example, FIGURE 17A shows measured responsivity data for two n-doped microstructured wafers and two p-doped microstructured wafers, both of which were annealed at 825 K for about 30 minutes. This exemplary data indicates that the responsivity of n-doped substrates is higher over the measured spectral range. However, FIGURE 17B shows that the responsivities of microsturctured wafers formed in p-doped and n-doped substrates, via laser irradiation and annealing at a higher temperature of about 1075 K, are nearly identical.

In general, the above illustrative data indicates that microstructured p-doped samples have a lower response but exhibit a better quantum efficiency. It should be understood that the above data is presented only for illustrative purposes and is not intended to limit the scope of the invention. In general, both p-doped and n-doped substrates can be employed in the practice of the invention, and the resultant diodic characteristics and responsivity of microstuctured wafers generated by utilizing such substrates can be different than those depicted above based on selection of other parameters, such as laser fluence, number of pulses, etc.

In addition to responsivity, another parameter of interest associated with performance of a photodetector can be its quantum efficiency. The term 'quantum efficiency' is known in the art, and is generally defined as the number of electron-hole pairs generated per incident photon at a zero applied voltage. In some cases, a microstructured sample that exhibits a high level of responsivity may not show a correspondingly high level of quantum efficiency. For example, in the above exemplary prototype microstructured silicon wafers, samples fabricated by employing n-doped substrates, laser pulses having a fluence of 4 kJ/m^2, and an annealing temperature of about 825 K exhibit the highest responsivity, but not the highest quantum efficiency. In fact, samples fabricated by employing similar conditions but a higher annealing temperature of 1075 K show higher quantum efficiencies, though lower responsivities. Similarly, the measured responsivities of samples made on p-doped substrates and annealed at 825 K or 1075 K are lower, but their quantum efficiencies are higher. Such variations of responsivity and quantum efficiency are preferably considered when

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selecting various parameters in practicing the teachings of the invention for fabricating a silicon photodetector.

The responsivity of a photodetector fabricated in accordance with the teachings of the invention can also vary as a function of a back bias applied thereto. Typically, the responsivity increases as the applied back bias increases. By of example, FIGURE 18 exhibits the responsivity of a silicon wafer microstructured in accordance with the teachings of the invention through irradiation by a plurality of femtosecond pulses at a fluence of $4kJ/m^2$ followed by annealing at 825 K for about 30 minutes, as a function of an applied back bias voltage. The sample was illuminated with a white light source with an approximate power of 50 microwatts. The responsivity, and hence gain, increases quickly up to a bias voltage of –5 volts and more slowly up to –15 volts. At voltages beyond –15 volts, the responsivity begins to fall. In some cases, the responsivity of a photodetector that exhibits a large gain may not be sufficiently linear for certain applications. Hence, in selecting a proper back voltage, in addition to responsivity, other factors, such as the linearity of the response should be considered. In addition, in applications in which the photodetectors are incorporated in an integrated silicon circuit, the bias voltage should be compatible with the requirements of that circuit.

A photodetector formed according to the teachings of the invention can operate within a wide range of temperatures. In some cases, it may be advantageous to cool the photodetector to decrease its average noise level. By way of example, FIGURE 19A presents current-voltage curves corresponding to an n-doped microstructured silicon sample made with femtosecond pulses at a fluence of about 4 kJ/m^2 and annealed at 825 K at different operating temperatures. The measured current in both the back bias and forward bias conditions decreases with decreasing the temperature. At very low temperatures (below 100 K), conduction becomes very low for both forward and back biases. FIGURE 19B shows the responsivity of such a microstructured wafer to incident radiation having a wavelength of 1064 nm (a wavelength close to the band gap of silicon at room temperature) at a back bias of –0.5 V as a function of operating temperature. The measured responsivity drops with temperature. This behavior may be, however, different if the wavelength of the illuminating light is far from the silicon band gap. A graph of the dark current at a bias voltage of –0.5 V as a function of temperature, however, shows that the noise decreases much more rapidly that the responsivity.

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In sum, photodiodes formed according to the teachings of the invention can exhibit responsivities in a wide region of the electromagnetic spectrum (e.g., wavelengths in a range of about 250 nm to about 1100 nm) that are nearly two orders of magnitude higher than those exhibited by conventional commercial silicon photodiodes. Further, responsivities at longer wavelengths, e.g., as long as 1600 nm, can be nearly five orders of magnitude greater than those exhibited by conventional silicon photodiodes in this range. In some of the above prototype samples fabricated according to the teachings of the invention for illustration purposes, the carrier mobility in the surface layer was measured to be about 101 $cm^2V^{-1}s^{-1}$; the response times included a rise time of about 10 ns and a fall time of about 30 ns; and a diode capacitance of about 63.9 nF at a back bias of –0.5 V was measured. A photodiode of the invention can exhibit a large gain at very small applied bias voltages, e.g., a gain greater than 1000 for an applied bias voltage of – 0.5 V.

A silicon photodetector according to the teachings of the invention, such as the above exemplary photodetector 46 (FIGURE 11A), can be fabricated by employing a variety of techniques. By way of example, in one exemplary method of fabricating such a photodetector, a selected portion of a silicon wafer, e.g., a 5 x 5 mm^2 area, is microstructured via exposure to short laser pulses in the presence of a suitable material, e.g., SF_6, in a manner described above. The wafer is then dipped in a solution of HF (e.g., a 5% solution) in order to remove any native oxide layer before forming electric contacts with the microstructured layer. Subsequently, a mask is deposited over the surface of the microstructued layer having exposed portions which correspond to a desired pattern of a conductive electrode to be formed on that surface. A selected metal, e.g., a Cr/Au alloy, is then evaporated over the masked surface, and the mask is removed to leave behind a patterned conductive layer, such as the conductive layer 52 shown in FIGURE 11A, and uncoated portions suitable for receiving radiation. Further, a conductive layer can be formed on a back surface of the wafer, an unstructured surface opposed to the microstructured layer, such as the layer 54 shown in FIGURE 11A. In many embodiments, the entire back surface is coated with the metal. The wafer can be then be coupled to a voltage source, such as the source 56 shown in FIGURE 11A, that can apply a bias voltage thereto and optionally other electronic elements, e.g.,

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capacitors, in a manner known in the art. Further, a the wafer and its associated circuitry can be placed in an appropriate housing by employing techniques known in the art.

The applications of microstructured silicon wafers formed according to the teachings of the invention, such as those discussed above, are not limited to photodetectors. For example, such silicon wafers can be employed in fabricating solar cells. In some cases, the optimal values of various parameters, such as substrate doping, associated with the microstructured wafer utilized in generating solar cells can be different than those in fabricating silicon photodetectors. A solar cell can be considered a p-n junction photodiode with high quantum efficiency. The conversion of photons into photocarriers is the physical mechanism by which light is converted in a solar cell into electricity. However, there is a fundamental difference between a photodetector and a solar cell. A photodetector is generally operated in a "photoconductive" mode: a back bias is applied thereto and a current is measured. In contrast, a solar cell is operated in a "photovoltaic" mode: it is operated in an open circuit mode or attached to a load without application of a bias voltage.

In one embodiment, a microstructured layer is formed in a p-doped crystalline silicon substrate by initially irradiating a plurality of locations on a surface thereof with femtosecond (e.g., 100 fs, and a central wavelength of 800 nm) laser pulses having a fluence of about 4 kJ/m^2 followed by annealing at 1075 K for about one hour. The wafer can then be utilized in fabricating a solar cell. More specifically, metal contacts, e.g., Cr/Au contacts, can be evaporated on the microstructure layer's surface so as to coat selected portions thereof while leaving at least a portion of the surface uncovered for receiving radiation, e.g., a finger grid metallic pattern can be disposed on the surface. In addition, the back surface of the substrate, the unstructured surface opposing the structured surface, can be coated, e.g., via evaporation, with a metallic coating. A load can be attached the wafer via electrical coupling to the metallic layers on the both sides of the wafer.

FIGURE 20 presents data comparing current-voltage (*I-V*) behavior of such a wafer, formed in a high resistivity (resistivity greater than about 1 ohm-m) silicon substrate, that can be utilized as a solar cell in the presence and in the absence of illumination. And FIGURE 21 presents a similar comparative data for a wafer formed in low resistivity silicon substrate (resistivity in a range of about 0.01 – 0.1 ohm-m). The

solar cell fabricated by employing the high resistivity substrate has an open circuit voltage of 0.4 volts and a short circuit current of 13.4 mA while the solar cell fabricated by utilizing the low resistivity substrate has an open circuit voltage of 0.31 volts and a short circuit current of 13.45 mA. It should be understood that this data is presented only for illustration purposes, and to show the possibility of utilizing a wafer microstructured in accordance with the teachings of the invention in forming a solar cell. However, this data is not intended to indicate optimal performance of a solar cell generated in accordance with the teachings of the invention. For example, the deposition of electrical contacts on the substrate can be optimized to obtain better performance than that described above.

In another application, a silicon wafer microstructured in accordance with the teachings of the invention can be utilized as a field emitter. In other words, an electric field can be applied to the microstructured surface to cause emission of electrons therefrom. To show the possibility of utilizing a microstructured wafer for generating field emission current, a number of prototype exemplary microstructured wafers were fabricated and field emission currents generated by them were measured. The experimental step-up for performing these measurements is shown schematically in FIGURE 22. A microstructured silicon sample 58 with a gold coating 60 evaporated on a back surface is mounted to a silicon wafer 62 having a gold coating 64, which functions as an anode, and is separated therefrom by a pair of mica spacers 66 and 68. The mounted sample is placed in a vacuum chamber, which is evacuated to a pressure of about 10^{-6} torr. A potential difference can be applied between the microstructured sample 58 and the gold-coated anode. And emission current can be measured at each applied voltage, e.g., via a picoammeter 70, a resistive elements 72 placed in series with the ammeter to protect it from unexpected surges in current.

FIGURE 23 shows exemplary results of field emission currents measured for silicon samples microstructured in SF_6. The typical figures of merit for a field emitting surface are turn-on-field, defined as the electric field (bias voltage divided by the tip-to-anode spacing) for which a current density of 0.01 microampere/mm^2 is observed, and threshold field, defined as the field at which a current density of 0.1 microamperes/mm^2 is produced. The turn-on field for a plurality of exemplary prototype substrates microstructured in SF_6 was measured as 1.3 V/micrometer, and the threshold field was

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measured as 2.15 V/micrometer – excellent values that are on par with those exhibited by nanotubes.

Those having ordinary skill in the art will appreciate that various modifications can be made to the above embodiments without departing from the scope of the invention. It should also be understood that various exemplary data presented above are intended only for illustrating salient features of various aspects of the invention, and is not intended to limit the scope of the invention.

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What is claimed is:

1. A method of fabricating a radiation-absorbing semiconductor structure, comprising:

irradiating each of a plurality of locations on a surface of a silicon substrate with one or more femtosecond laser pulses while exposing said surface to a sulfur-containing substance so as to generate a plurality of sulfur inclusions in a surface layer of said substrate, and

annealing said substrate at a temperature in a range of about 500 K to about 1100 K for a time duration in a range of about a few seconds to about a few hours.

2. The method of claim 1, further comprising selecting a duration of each laser pulse to be in a range of about 50 femtoseconds to about 500 femtoseconds.

3. The method of claim 1, further comprising selecting a fluence of each pulse to be in a range of about 1 kJ/m^2 to about 15 kJ/m^2.

4. The method of claim 1, further comprising selecting a central wavelength of said laser pulses to be in a range of about 200 nm to about 800 nm.

5. The method of claim 1, wherein said irradiating step comprises exposing each location to a number of laser pulses ranging from 2 to about 500.

6. The method of claim 1, further comprising subjecting each of said surface locations to successive laser pulses separated from one another by a time interval in a range of about 1 microsecond to about 1 millisecond.

7. The method of claim 1, further comprising performing said annealing step in any of an inert atmosphere or a low-pressure atmosphere.

8. The method of claim 1, further comprising selecting said sulfur-containing substance to be any of SF_6 and H_2S.

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9. The method of claim 1, wherein said semiconductor structure absorbs radiation having wavelength components in a range of about 0.25 to about 10 microns.

10. The method of claim 1, wherein said semiconductor structure absorbs radiation having wavelength components in a range of about 0.35 to about 2.5 microns.

11. The method of claim 1, wherein said semiconductor structure exhibits a substantially uniform absorption for wavelength components in a range of about 1.2 to about 2.5 microns.

12. A method of fabricating a photodetector, comprising:

forming a semiconductor structure absorbing radiation in a wavelength range of about 0.25 to about 3.5 microns and exhibiting a diodic current-voltage characteristic in said wavelength range, said forming step comprising:

irradiating a surface of a silicon substrate at one or more locations thereof with one or more laser pulses having short pulse widths while exposing said surface to a sulfur-containing gas to generate a micro-structured layer having sulfur inclusions,

annealing said substrate at a temperature in a range of about 500 K to about 1000 K for a time duration in a range of about a few seconds to about a few hours, and

depositing a plurality of metallic contacts on selected portions of said semiconductor structure to allow applying a reverse bias voltage thereto.

13. The method of claim 12, wherein said pulse widths are selected to be in a range of about tens of femtoseconds to about tens of nanoseconds.

14. The method of claim 12, further comprising selecting said sulfur-containing substance to be any of SF_6 and H_2S.

15. The method of claim 12, further comprising performing said annealing step in an inert atmosphere.

16. The method of claim 12, wherein said depositing step comprises thermally evaporating one or more selected metals on said selected portions of the semiconductor structure.

17. The method of claim 12, further comprising selecting a thickness of said metal contacts to be in a range of about 5 nm to about 100 nm.

18. The method of claim 16, wherein said depositing step comprises thermally evaporating a chromium layer followed by thermally evaporating a gold layer on a selected portion of said semiconductor structure to generate at least one of said metal contacts.

19. The method of claim 18, further comprising selecting a thickness of said chromium layer to be in a range of about 1 nm to about 5 nm.

20. The method of claim 19, further comprising selecting a thickness of said gold layer to be in a range of about 4 nm to about 100 nm.

21. The method of claim 12, further comprising configuring said metal contacts so as to ensure that at least a portion of said micro-structured layer remains capable of receiving an external radiation.

22. A method of fabricating a semiconductor structure, comprising

irradiating a plurality of locations on a surface of a silicon substrate with one or more laser pulses having pulse widths in a range of about 50 to about 500 femtoseconds while exposing said surface to a substance having an electron-donating constituent so as to generate a micro-structured surface layer comprising inclusions incorporating said electron-donating constituent, and

annealing said substrate at an elevated temperature in a range of about 500 K to about 1100 K for a selected time period.

23. The method of claim 22, further comprising selecting said electron-donating constituent to be any of chlorine (Cl_2), nitrogen (N_2) and air.

24. The method of claim 22, wherein said irradiating step further comprises directing said laser pulses at said surface along a direction substantially perpendicular to said surface.

25. The method of claim 22, wherein said selected annealing period is in a range of about a few seconds to about a few hours.

26. The method of claim 22, wherein said annealing step is performed in an inert atmosphere.

27. A method of fabricating a radiation-absorbing semiconductor wafer, comprising:

irradiating at least one surface location of a silicon substrate with a plurality of temporally short laser pulses while exposing said location to a substance having an electron-donating constituent so as to generate a substantially disordered surface layer incorporating a concentration of said electron-donating constituent, and

annealing said substrate at an elevated temperature and for a duration selected to enhance charge carrier density in said substantially disordered surface layer.

28. The method of claim 27, wherein said elevated temperature and duration are selected to cause re-arrangement of atomic bonds in said surface layer so as to increase concentration of carrier electrons in surface layer.

29. The method of claim 27, wherein said elevated temperature and duration are selected to enhance electron carrier density in the surface layer by a factor of about 10% to about 200% relative to a pre-annealing level.

30. The method of claim 27, wherein said elevated temperature and duration are selected to cause said surface layer to form a diode junction with underlying silicon substrate.

31. The method of claim 27, wherein said elevated temperature and duration are selected such that said annealed substrate exhibits a responsivity in a range of about 1 A/W to about 200 A/W upon exposure of said surface layer to radiation having wavelengths in a range of about 250 nm to about 1100 nm and application of a reverse bias in a range of about 0.1 V to about 15 V to said wafer.

32. The method of claim 27, wherein said elevated temperature is selected to be in a range of about 500 K to about 1100 K.

33. The method of claim 33, wherein said duration is selected to be in a range of about a few seconds to about few hours.

34. The method of claim 27, further comprising selecting said short laser pulses to have pulse widths in a range of about tens of femtoseconds to about tens of nanoseconds.

35. The method of claim 27, further comprising selecting a fluence of said pulses and a partial pressure of said substance having an electron-donating constituent such that the concentration of said electron-donating constituent incorporated in said surface layer ranges from about 0.5 to about 5 atom percent.

36. A method of fabricating a radiation-absorbing semiconductor wafer, comprising

irradiating at least one surface location of a silicon substrate with temporally short laser pulses while exposing the substrate to a substance having an electron-donating constituent so as to generate a microstructured surface layer having inclusions containing the electron-donating constituent, and

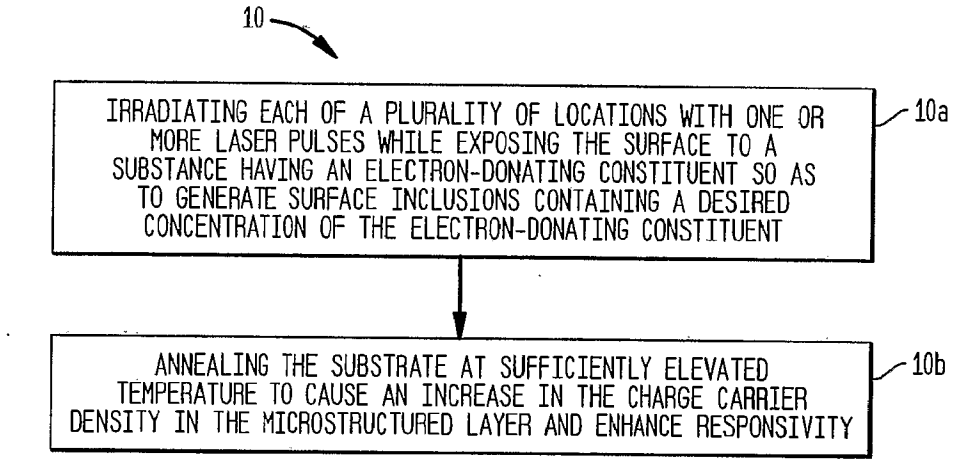
annealing the substrate at an elevated temperature and for a duration selected to enhance a responsivity of the microstructured substrate to radiation having at least one wavelength in a range of about 250 nm to about 1100 nm incident on the microstructured surface layer by at least a factor of about 10.

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37. The method of claim 37, wherein the annealing temperature lies in a range of about 700 K to about 900 K.

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FIG. 1



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FIG. 2

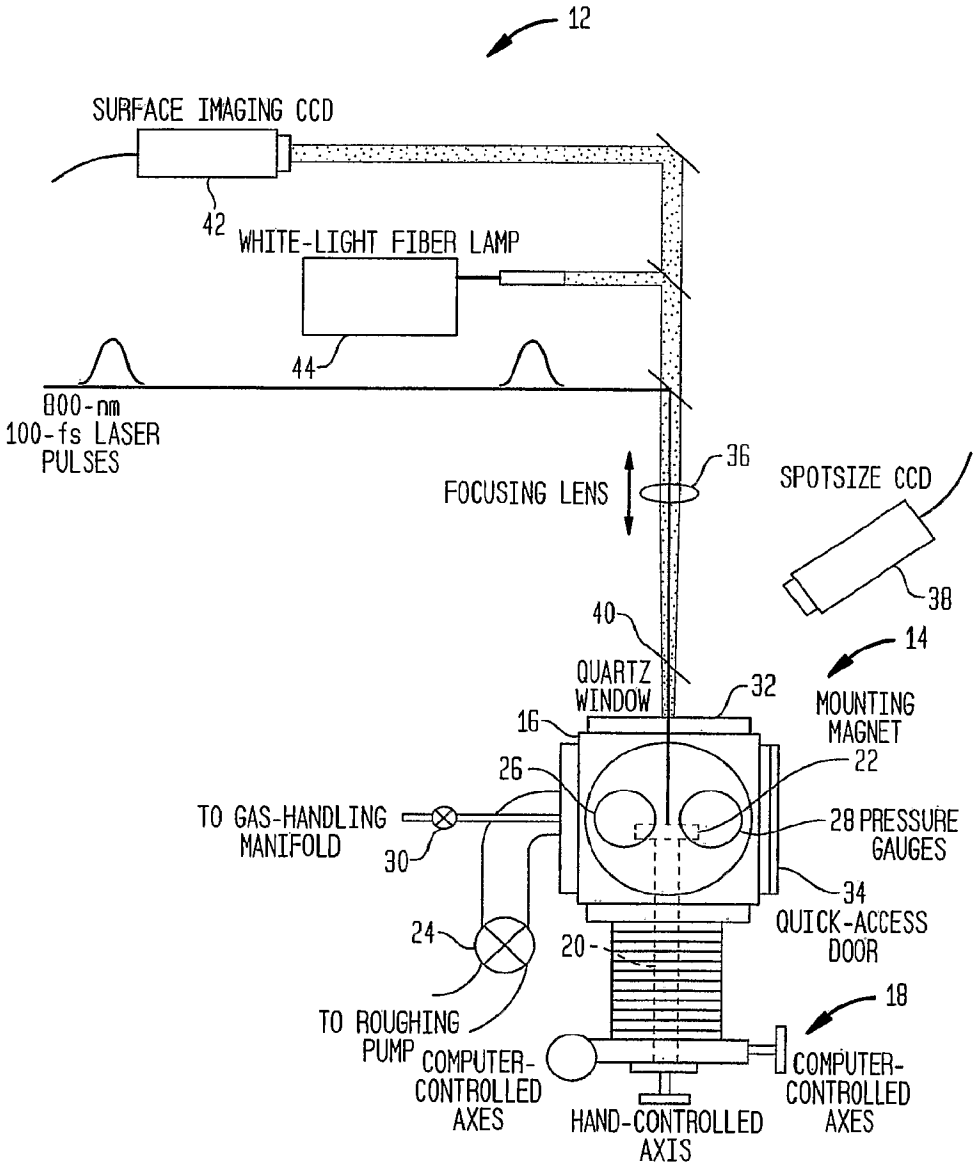
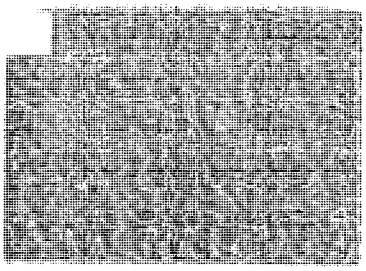

12
SURFACE IMAGING CCD
42
WHITE-LIGHT FIBER LAMP
44
800-nm
100-fs LASER
PULSES
FOCUSING LENS
36
SPOTSIZE CCD
38
40
14
QUARTZ
WINDOW
32
MOUNTING
MAGNET
16
26
22
TO GAS-HANDLING
MANIFOLD
30
28 PRESSURE
GAUGES
34
QUICK-ACCESS
DOOR
24
20
18
TO ROUGHING
PUMP
COMPUTER-
CONTROLLED
AXES
HAND-CONTROLLED
AXIS
COMPUTER-
CONTROLLED
AXES

FIG. 3



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FIG. 4

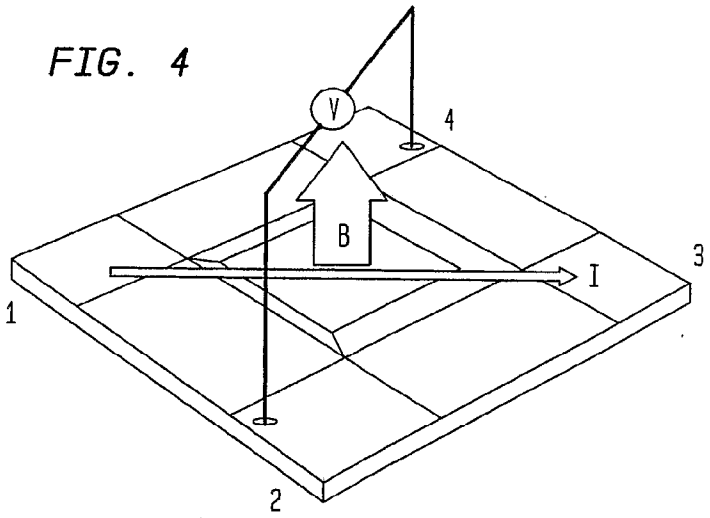

V
4
B
I
3
1
2

FIG. 5

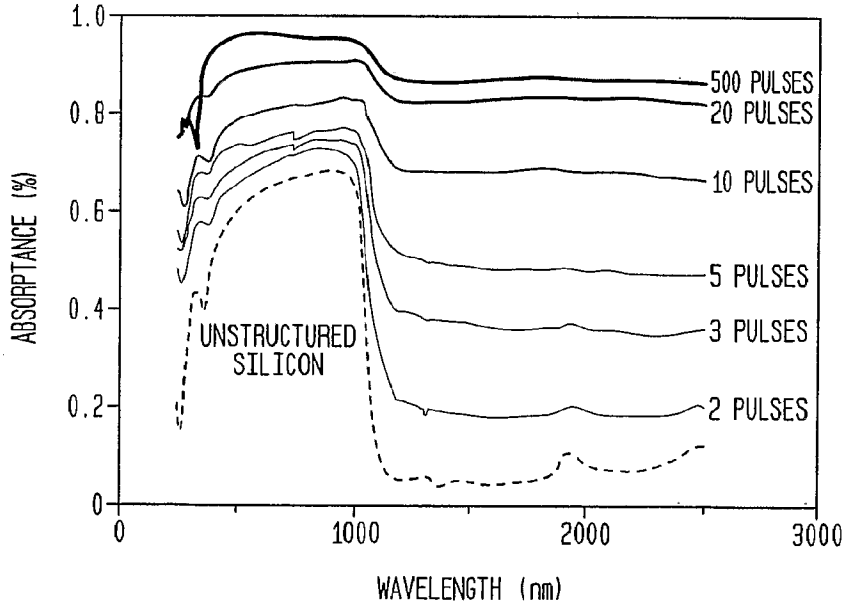

1.0
0.8
0.6
0.4
0.2
0
ABSORPTANCE (%)
500 PULSES
20 PULSES
10 PULSES
5 PULSES
3 PULSES
2 PULSES
UNSTRUCTURED SILICON
0
1000
2000
3000
WAVELENGTH (nm)

FIG. 6

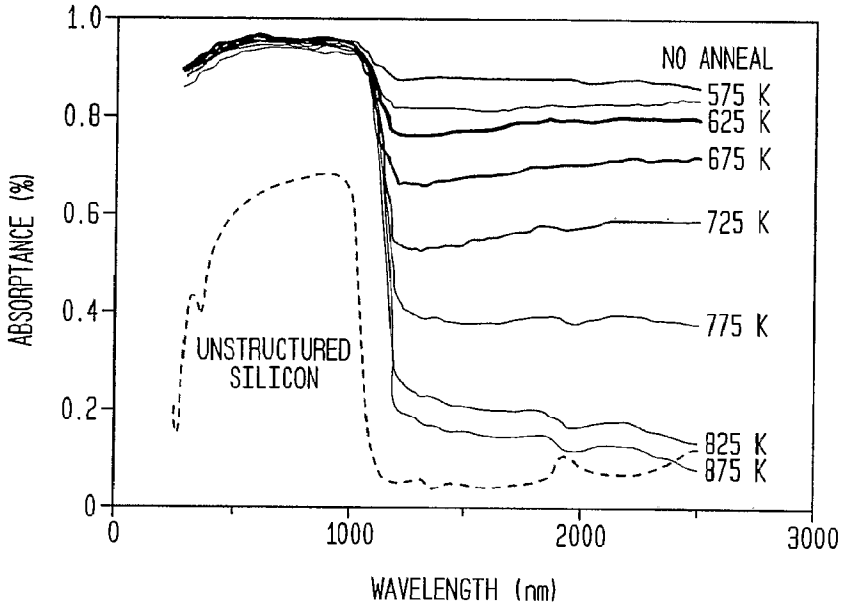
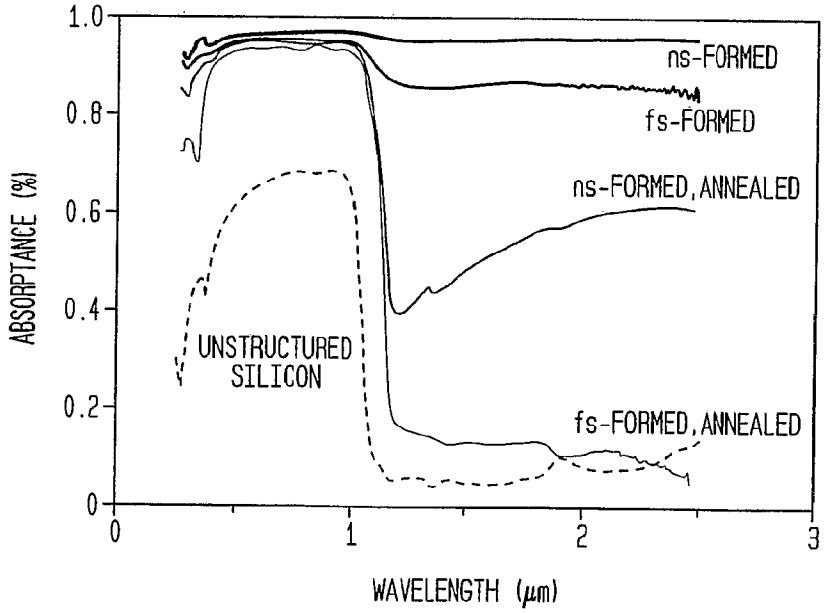


FIG. 7



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FIG. 8A

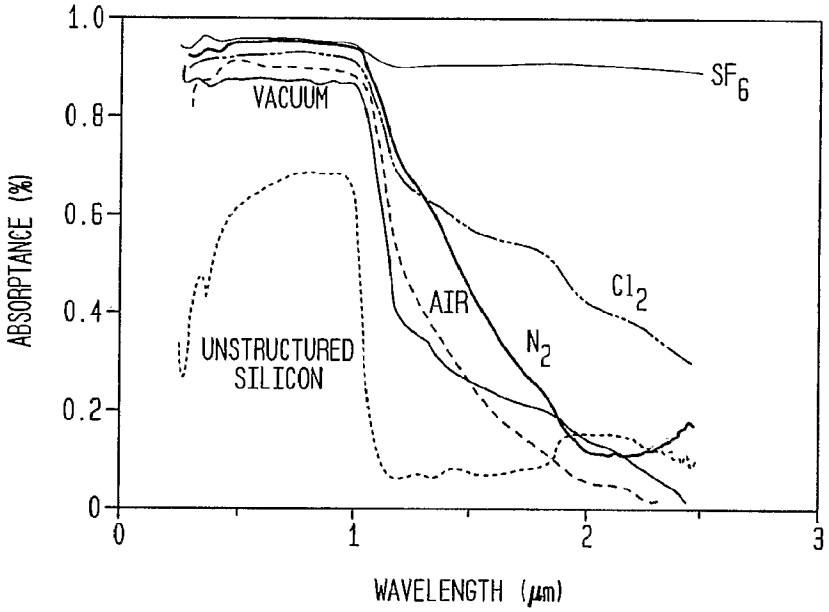

1.0
0.8
0.6
0.4
0.2
0
ABSORPTANCE (%)
VACUUM
SF6
AIR
Cl2
N2
UNSTRUCTURED
SILICON
0
1
2
3
WAVELENGTH (μm)

FIG. 8B

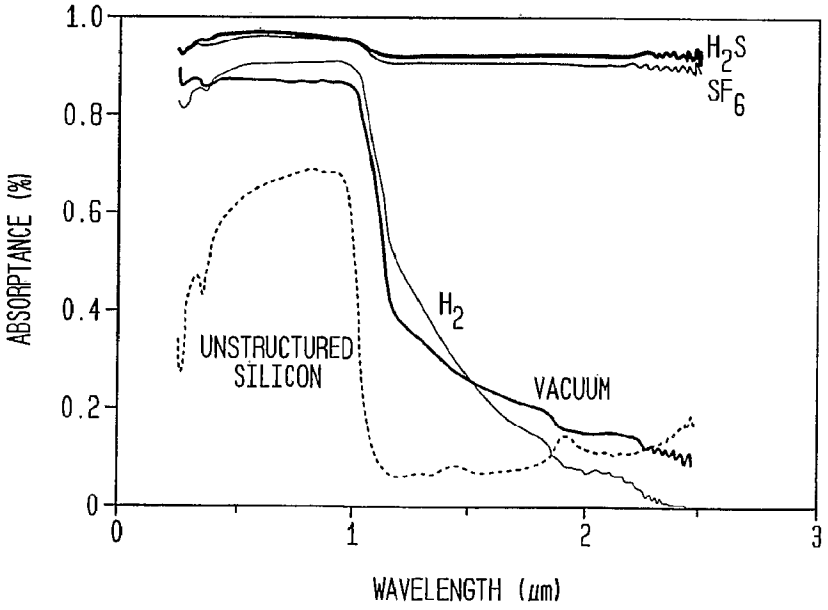

1.0
0.8
0.6
0.4
0.2
0
ABSORPTANCE (%)
H2S
SF6
H2
UNSTRUCTURED
SILICON
VACUUM
0
1
2
3
WAVELENGTH (μm)

FIG. 9

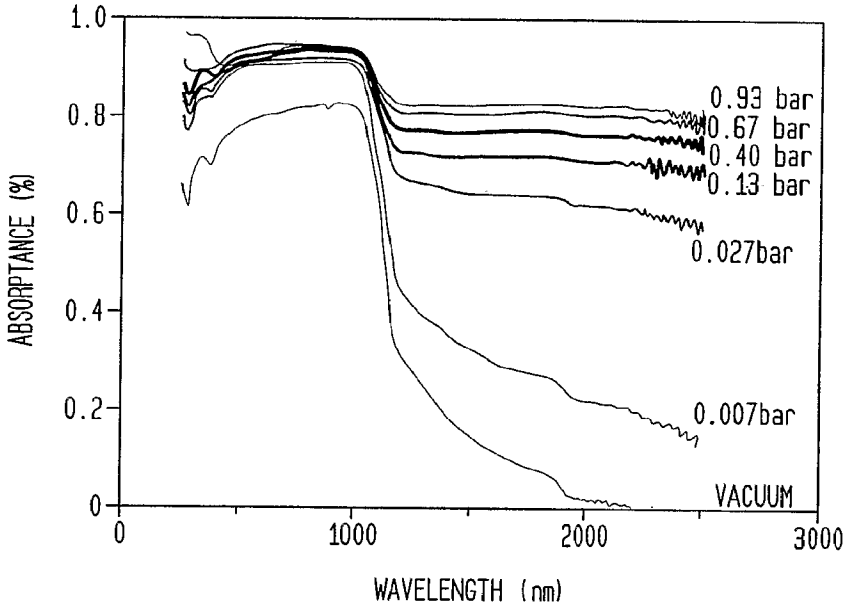

1.0
0.8
0.6
0.4
0.2
0
ABSORPTANCE (%)
0
1000
2000
3000
WAVELENGTH (nm)
0.93 bar
0.67 bar
0.40 bar
0.13 bar
0.027bar
0.007bar
VACUUM

FIG. 10

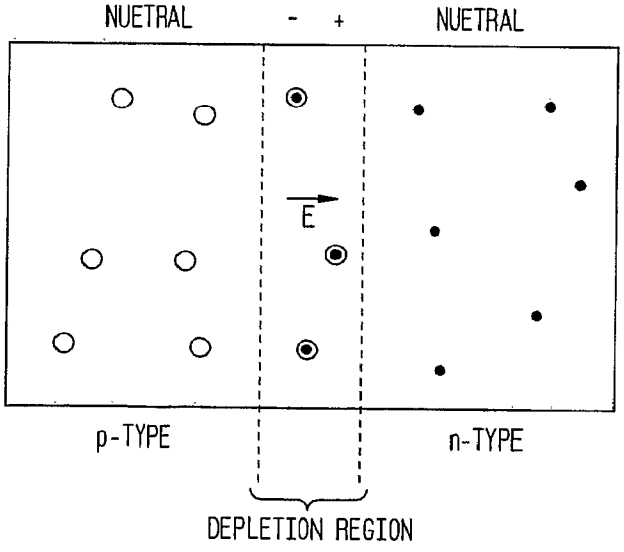

NUETRAL
-
+
NUETRAL
E
p-TYPE
n-TYPE
DEPLETION REGION

FIG. 11A

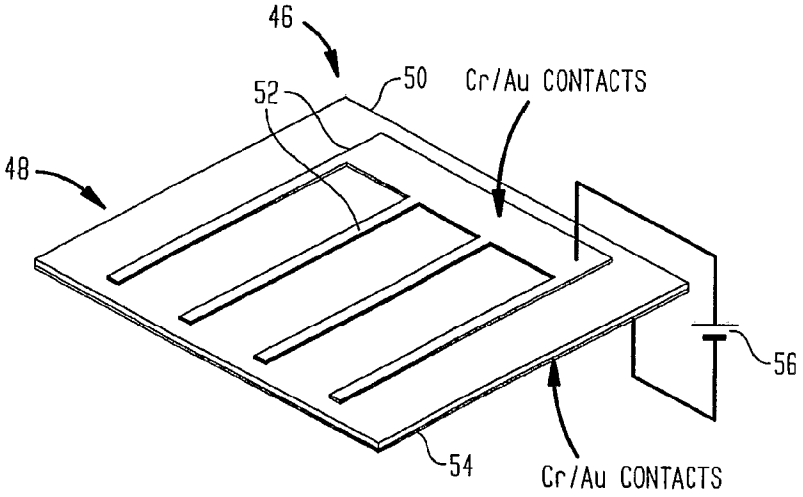


FIG. 11B

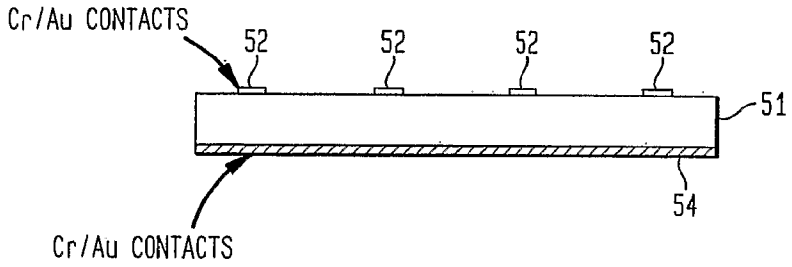


FIG. 12

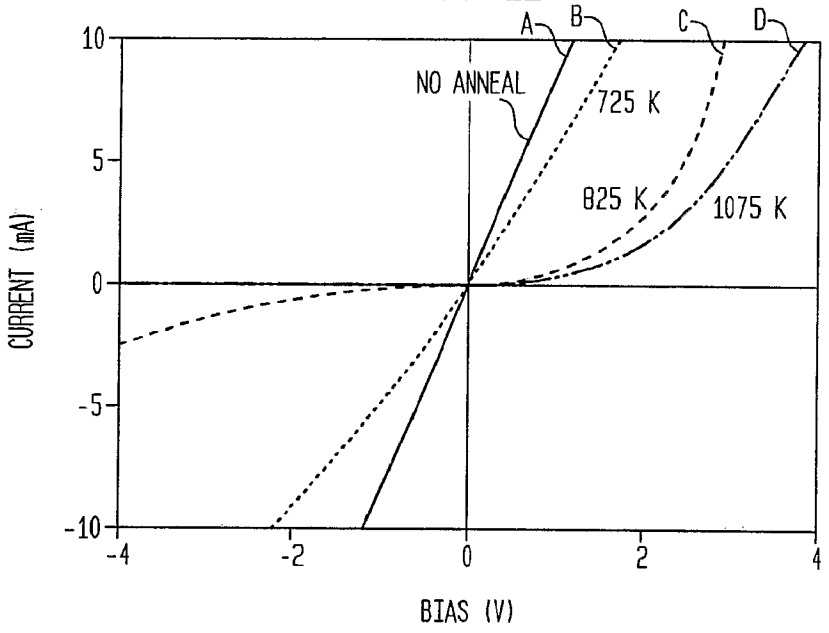

A
B
C
D
NO ANNEAL
725 K
825 K
1075 K
10
5
0
-5
-10
-4
-2
0
2
4
CURRENT (mA)
BIAS (V)

FIG. 13

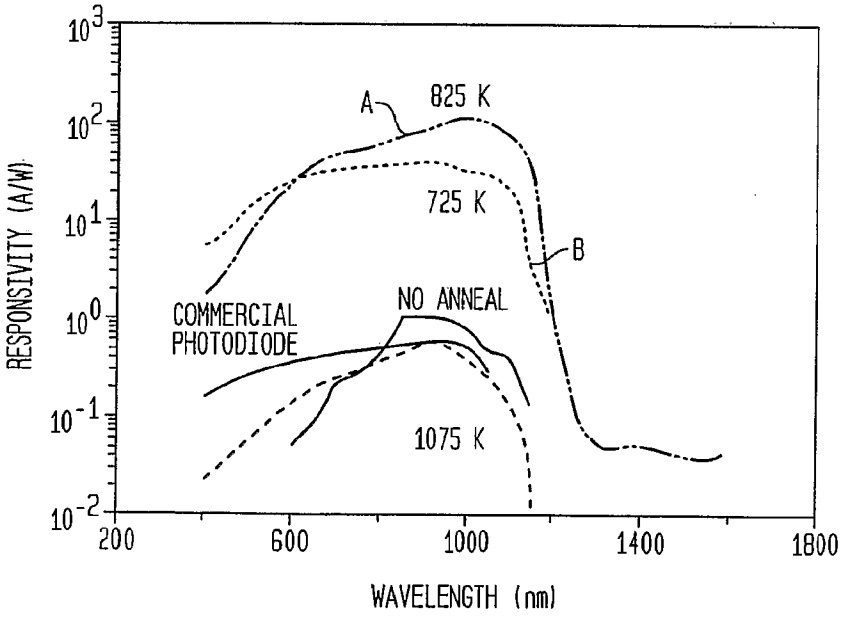

10^3
10^2
10^1
10^0
10^{-1}
10^{-2}
A
825 K
725 K
B
NO ANNEAL
COMMERCIAL
PHOTODIODE
1075 K
200
600
1000
1400
1800
RESPONSIVITY (A/W)
WAVELENGTH (nm)

FIG. 14

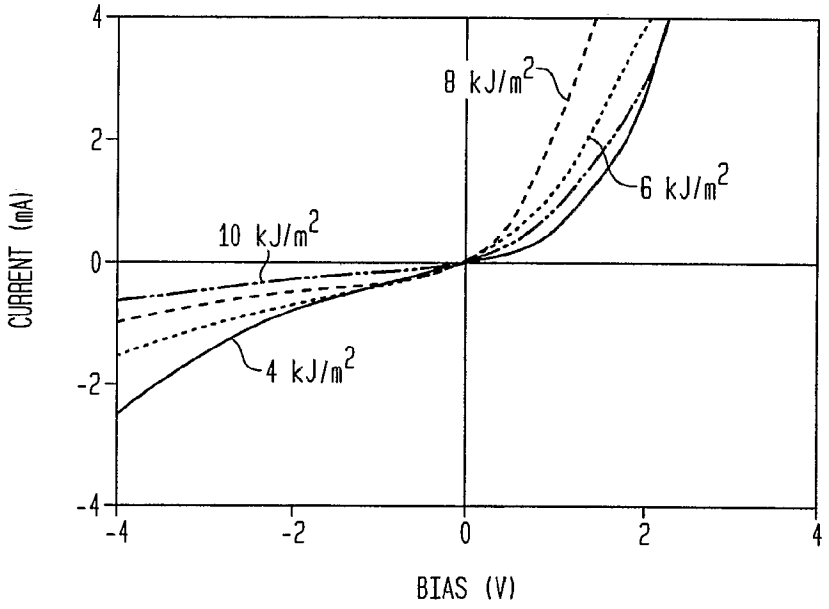


FIG. 15A

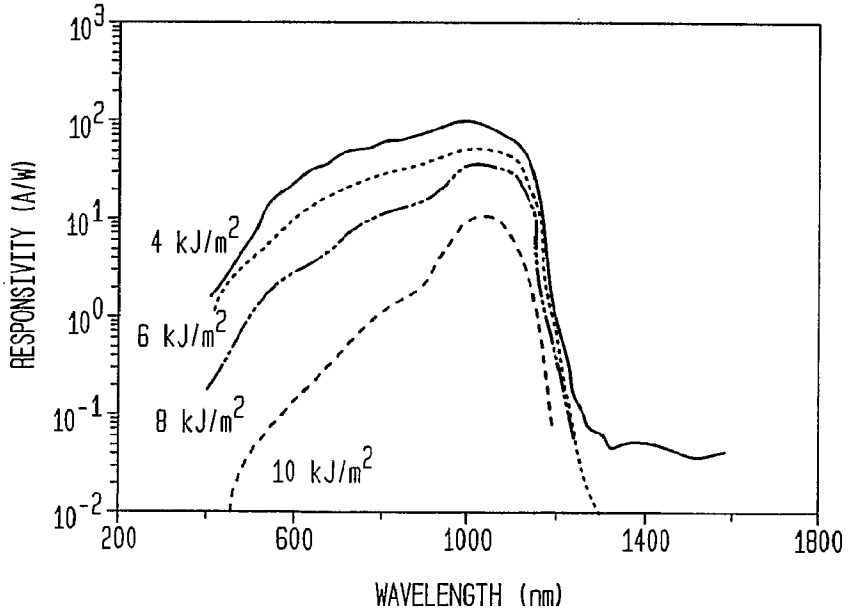


FIG. 15B

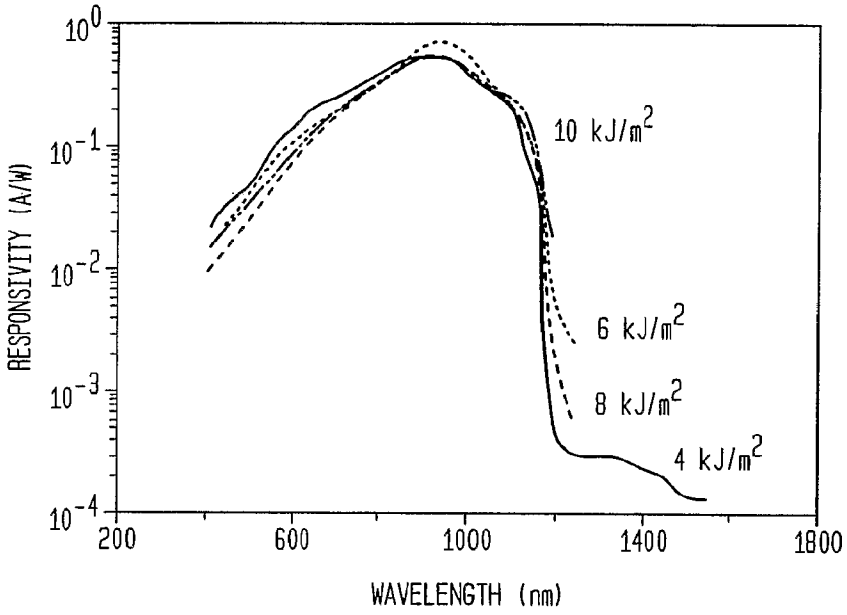


FIG. 16A

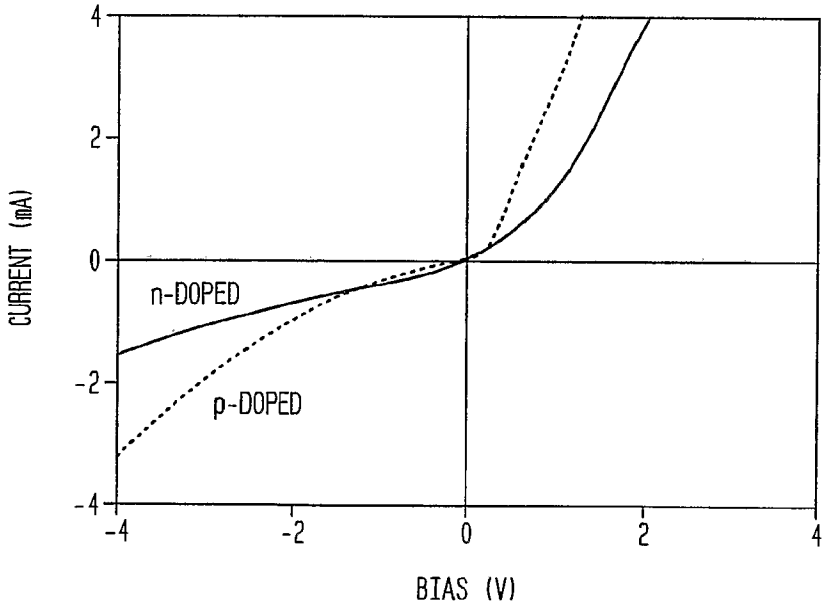


FIG. 16B

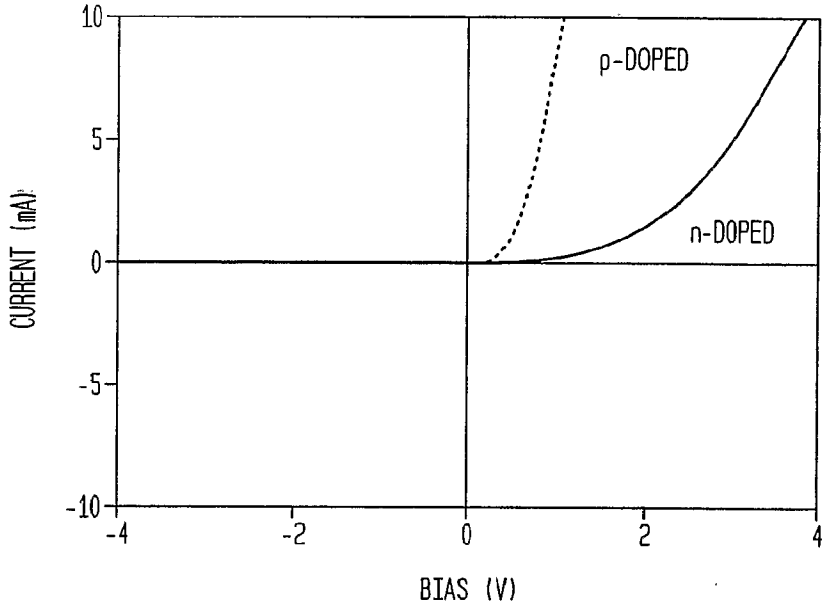


FIG. 17A

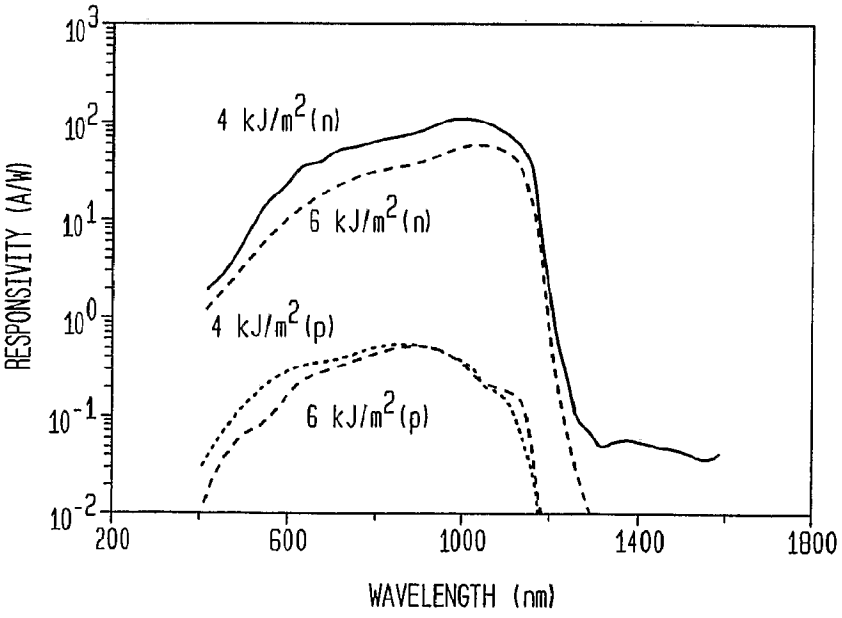


FIG. 17B

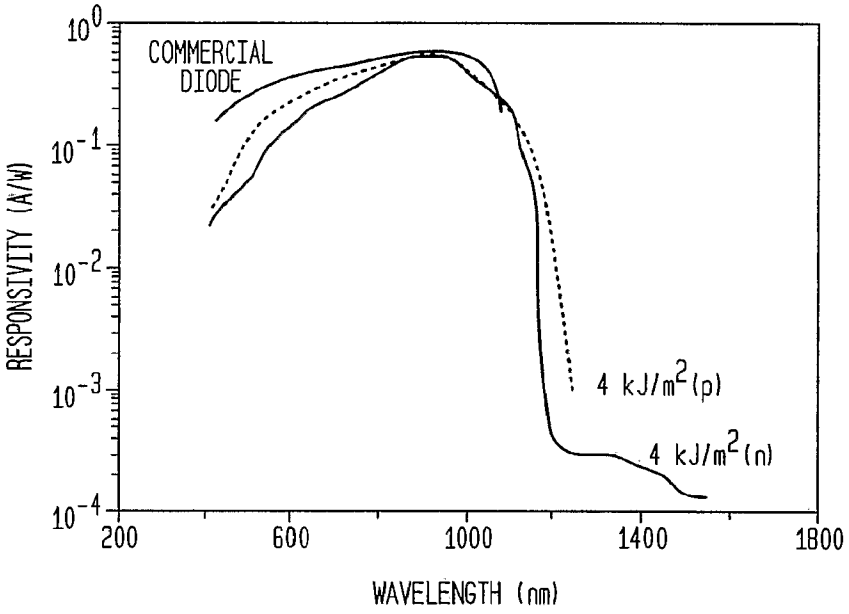


FIG. 18

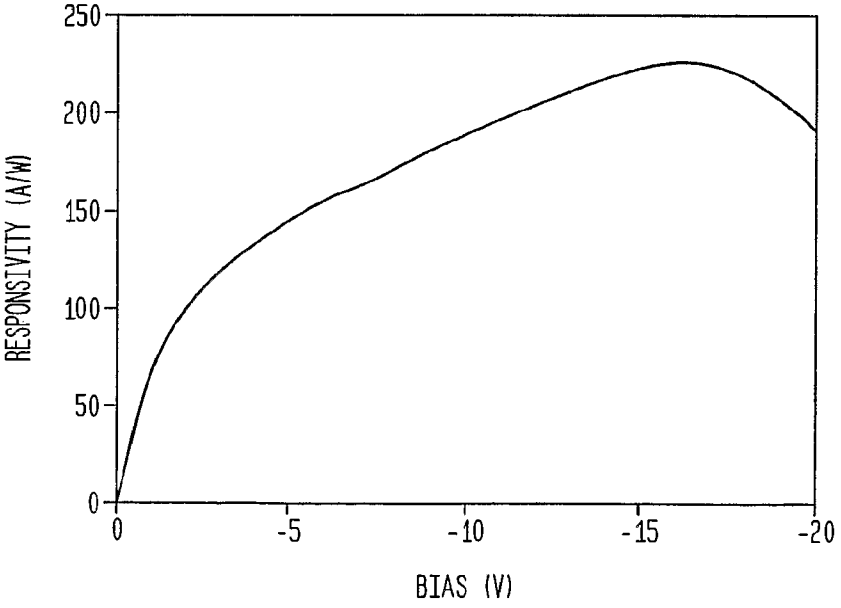


FIG. 19A

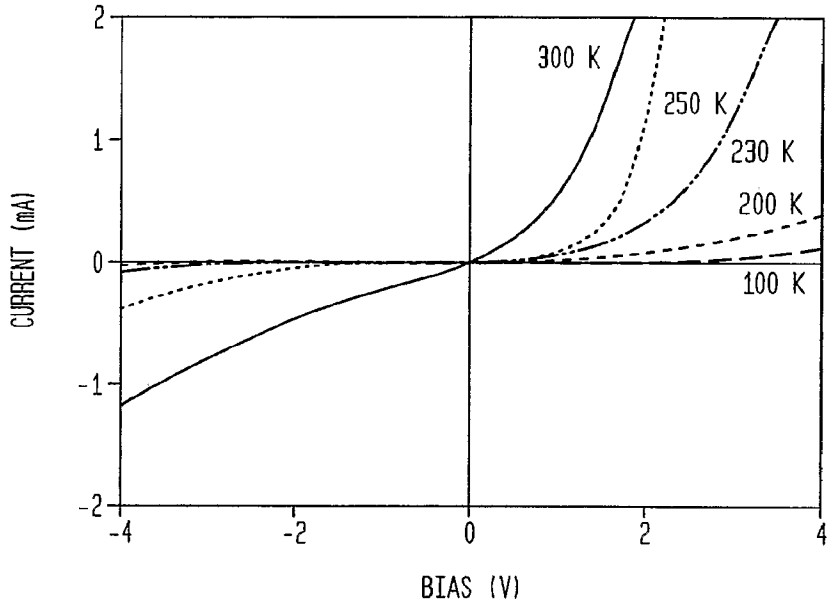


FIG. 19B

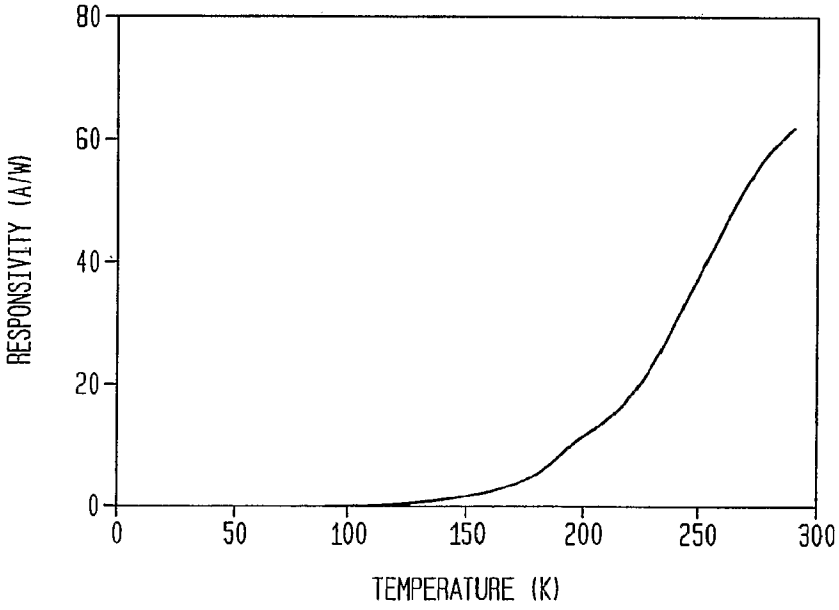


FIG. 20

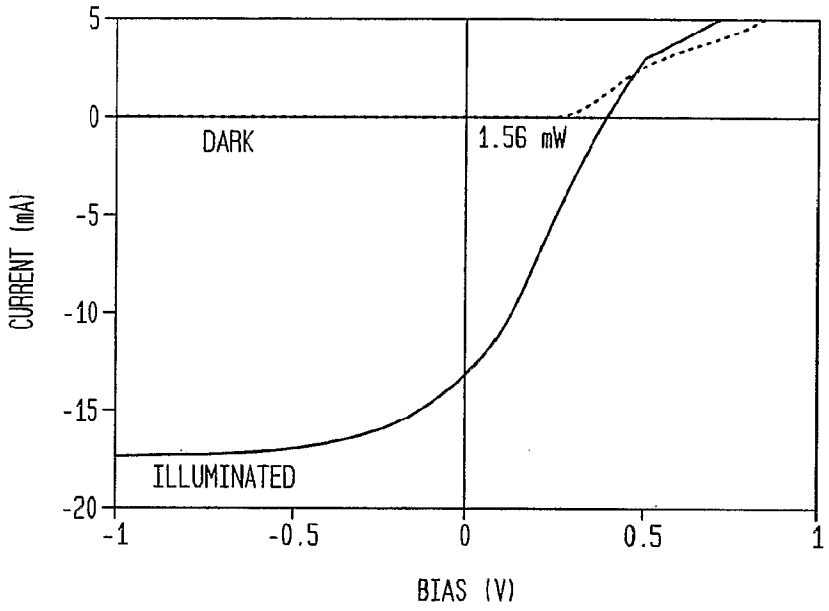

5
0
-5
-10
-15
-20
-1
-0.5
0
0.5
1
DARK
1.56 mW
ILLUMINATED
CURRENT (mA)
BIAS (V)

FIG. 21

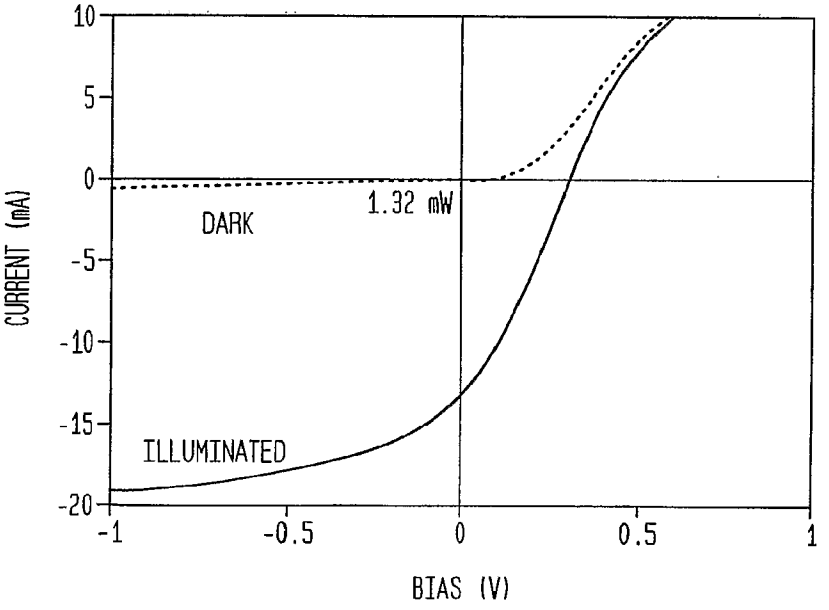

10
5
0
-5
-10
-15
-20
-1
-0.5
0
0.5
1
DARK
1.32 mW
ILLUMINATED
CURRENT (mA)
BIAS (V)

FIG. 22

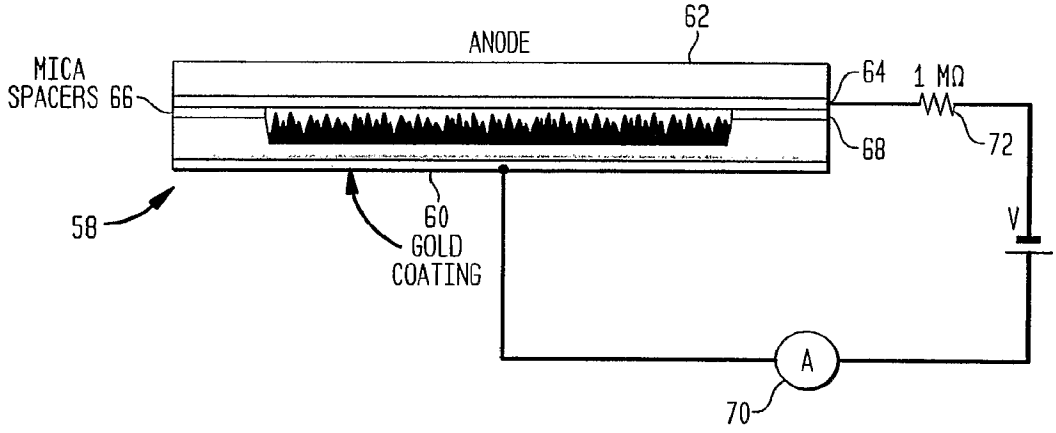
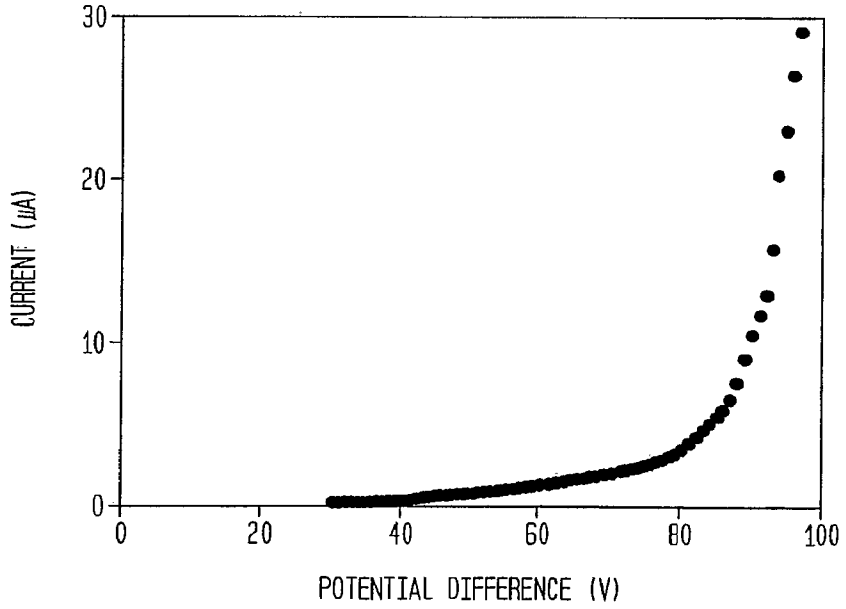

62
ANODE
MICA
SPACERS 66
64
1 MΩ
68
72
58
60
GOLD
COATING
V
A
70

FIG. 23


30
20
10
0
CURRENT (μA)
0
20
40
60
80
100
POTENTIAL DIFFERENCE (V)

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60/860,735	22 November 2006 (22.11.2006)	US

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(54) Title: SYSTEMS AND METHODS OF LASER TEXTURING AND CRYSTALLIZATION OF MATERIAL SURFACES

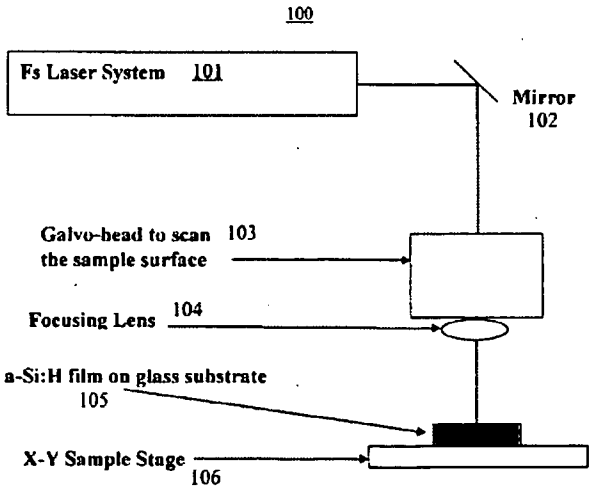


FIG. 1

(57) Abstract: The surface of a material is textured and crystallized in a single step by exposing the surface to pulses from an ultrafast laser. The laser treatment causes pillars to form on the treated surface. These pillars provide for greater light absorption. The crystallization of the material provides for higher electric conductivity and changes in optical properties of the material. The method may be performed in a gaseous environment, so that laser assisted chemical etching will aid in the texturing of the surface. This method may be used on various material surfaces, such as semiconductors, metals, ceramics, polymers, and glasses.

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SYSTEMS AND METHODS OF LASER TEXTURING AND CRYSTALLIZATION OF MATERIAL SURFACES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from U.S. Provisional Patent Application No. 60/752,545, filed on December 21, 2005; U.S. Provisional Patent Application No. 60/843,874, filed on September 12, 2006; and U.S. Provisional Patent Application No. 60/860,735, filed on November 22, 2006. The full disclosures of these provisional applications are incorporated herein by reference.

STATEMENT OF GOVERNMENT INTEREST

[0002] The present invention was developed under National Science Foundation Grant No. GA10507-31335 427250. The government has certain rights in the invention.

FIELD OF THE INVENTION

[0003] Apparatuses and methods consistent with the present invention relate to modifying surfaces, and more particularly, to modifying surfaces of thin films in order to alter their thermal, structural, optical, and electrical properties.

BACKGROUND OF THE INVENTION

[0004] Laser processing provides a unique method of modifying materials by depositing large amounts of energy onto the surface of a material in an extremely controlled manner. Laser processing enables the precisely localized treatment of a material. Laser processing is particularly useful after thin-film deposition of amorphous materials, which usually involves low temperature processing, and allows for the use of flexible and low melting temperature

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substrates for large area device fabrication. However, these devices lack better performance, usually due to poor electrical, optical, and/or structural properties. Laser processing of these devices with ultra-short laser pulses has been found to improve the properties of the devices, because the high peak intensities of the laser pulses rapidly texture the surface, and a subsequent quenching process induces crystallization in the material. The texturing of the surface leads to more light absorption in the material, and the subsequent crystallization improves the electronic properties of the material.

[0005] For example, thin film amorphous silicon (a-Si) based devices are inexpensive compared to their crystalline counterparts because of low temperature processing, which is suitable for deposition on large substrates, such as glass, plastic, and steel foils. However, solar cell devices fabricated using a-Si thin-films lack efficiency, have a high reflectivity across the electromagnetic spectrum, possess a larger band gap (~ 1.7 eV), and have limited carrier mobility. In order to improve the efficiency and sensitivity of a-Si based devices, post-deposition laser processing is usually recommended. This includes texturing and subsequent crystallization of the surface. Pulsed laser crystallization of thin a-Si films on various substrates has potential applications in the fabrication of thin film transistors for active matrix liquid crystal displays and efficient solar cells. Typically, nanosecond or microsecond lasers are utilized to crystallize such films through a rapid melting and solidification process. Methods of using a laser to crystallize a material surface are also disclosed by U.S. Patent No. 6,169,014 to McCulloch, U.S. Patent No. 6,451,631 to Grigoropoluos et al., U.S. Patent No. 6,489,188 to Jung, and U.S. Patent No. 6,635,932 to Grigoropoluos et al.

[0006] Methods of using an ultrafast laser to texture the surface of crystalline bulk silicon are disclosed in U.S. Patent Application No. 10/155,429 to Mazur. Mazur discloses a method of texturing the surface of a silicon substrate by irradiating the surface with ultra-short laser

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pulses in the presence of a background gas, such as SF_6. After texturing, the silicon surface in Mazur contains cone-like microstructures that are up to 50 μm high, and have widths of about 0.8 μm near the tip and up to 10 μm near the base. Also, Mills and Kolasinski disclose nanospikes formed atop silicon pillars when the sample is exposed to SF_6 gas diluted with helium (17 Nanotechnology 2471, 2006). Further, Vorobyev and Guo disclose the formation of nanoprotrusions with spherical tips on copper, gold, and platinum surfaces by using a femtosecond laser ablation technique (14 Optics Express 2164, 2006).

[0007] While the prior art discussed above provides important advantages, it suffers from a number of drawbacks. The prior art fails to disclose a method of producing periodic arrays of pillar structures on a surface of a material by texturing the surface. Further, the prior art does not teach a method of texturing and crystallizing a surface in one step. Also, the prior art does not teach a method of forming pillar structures on metal surfaces. In addition, the prior art fails to disclose a method of utilizing laser texturing and crystallization in many novel applications.

SUMMARY OF THE INVENTION

[0008] Exemplary embodiments of the present invention overcome the above disadvantages and other disadvantages not described above. Also, the present invention is not required to overcome the disadvantages described above, and an exemplary embodiment of the present invention may not overcome any of the problems described above.

[0009] The present invention provides a method for texturing a surface of a semiconductor material, including providing an etching gas in an area around the surface of the material, irradiating a portion of the surface with short laser pulses, and translating at least one of the surface and a laser beam to allow the short laser pulses to impact another portion

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of the surface. This method produces a periodic array of pillar structures on the surface, resulting in changes in properties of the surface.

[0010] According to an aspect of the present invention, the method additionally produces nanospikes atop the pillar structures.

[0011] Also, the present invention provides a method for texturing a surface of a semiconductor material, including providing an etching gas in an area around the surface of the material; irradiating a portion of the surface with short laser pulses while simultaneously crystallizing the portion of the surface; and translating at least one of the surface and a laser beam to allow the short laser pulses to impact another portion of the surface. This method produces pillar structures on the surface, resulting in changes in properties of the surface.

[0012] In addition, the present invention provides a method for texturing a metallic surface, including irradiating a portion of the metallic surface with short laser pulses, and translating at least one of the surface and a laser beam to allow the short laser pulses to impact another portion of the surface. This method produces pillar structures on the surface, resulting in changes in properties of the surface.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The above and other aspects of the present invention will be better understood from a consideration of the following detailed description of exemplary embodiments of the present invention, and the accompanying drawings, in which:

[0014] **FIG. 1** illustrates the components in a surface modification system, according to an exemplary embodiment of the present invention;

[0015] **FIG. 2** illustrates an example of a sample material to which surface modification is performed, according to an exemplary embodiment of the present invention;

[0016] **FIG. 3** is a photograph of a hydrogenated amorphous silicon (a-Si:H) surface, with **FIG. 3(a)** illustrating a non-modified portion, and **FIG. 3(b)** illustrating a modified portion, according to an exemplary embodiment of the present invention;

[0017] **FIG. 4** illustrates scanning electron microscopy (SEM) images of an a-Si:H surface, with **FIG. 4(a)** illustrating a non-modified portion, and **FIG. 4(b)** illustrating a modified portion, according to an exemplary embodiment of the present invention;

[0018] **FIG. 5** illustrates graphical results of absorption versus wavelength for an a-Si:H surface, with **FIG. 5(a)** illustrating the absorption for an untreated sample, and **FIG. 5(b)** illustrating the absorption for a treated sample, according to an exemplary embodiment of the present invention;

[0019] **FIG. 6** illustrates graphical results of an X-ray diffraction pattern for an a-Si:H surface, with **FIG. 6(a)** illustrating the results for an untreated sample, and **FIG. 6(b)** illustrating the results for a treated sample, according to an exemplary embodiment of the present invention;

[0020] **FIG. 7** illustrates graphical results of current versus voltage for an a-Si:H surface with varying light levels, with **FIG. 7(a)** illustrating the results for an untreated control sample,

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and **FIG. 7(b)** illustrating the results for a treated sample, according to an exemplary embodiment of the present invention;

[0021] FIG. 8 illustrates an atomic force microscope image of an a-Si:H surface that has been treated according to an exemplary embodiment of the present invention;

[0022] FIG. 9 is a graph illustrating the average roughness of laser treated a-Si:H surfaces at different laser fluences, according to an exemplary embodiment of the present invention;

[0023] FIG. 10 illustrates results of X-ray photoelectron spectroscopy (XPS) measurements of a-Si:H surfaces, with **FIG. 10(a)** illustrating the XPS measurement of untreated control surfaces, **FIG. 10(b)** illustrating the XPS measurement of treated surfaces, and **FIG. 10(c)** illustrating depth profiles of oxygen concentration for untreated control and treated surfaces, according to an exemplary embodiment of the present invention;

[0024] FIG. 11 is a graph illustrating the reflectivity of surfaces of polished silicon, unpolished silicon, and treated a-Si:H surfaces, according to an exemplary embodiment of the present invention;

[0025] FIG. 12 is a graph illustrating the transmission of samples of unpolished silicon and treated a-Si:H surfaces, according to an exemplary embodiment of the present invention;

[0026] FIG. 13 illustrates SEM images of germanium surfaces, with **FIG. 13(a)** illustrating an SEM image viewed at 45° from the surface normal, **FIG. 13(b)** illustrating a higher magnification SEM image showing nanospikes formed on each germanium pillar, **FIG. 13(c)** illustrating a single nanospike of a treated sample, and **FIG. 13(d)** illustrating a nanotip formed after brief chemical etching, according to exemplary embodiments of the present invention;

[0027] FIG. 14 shows a comparison of SEM images viewed at 45° from the surface normal of Ge (100) surfaces irradiated at different laser power levels, with **FIG. 14(a)** showing a surface irradiated with a laser power of 0.66 J/cm^2, **FIG. 14(b)** showing a surface irradiated

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with a laser power of 0.56 J/cm^2, **FIG. 14(c)** showing a surface irradiated with a laser power of 0.3 J/cm^2, and **FIG. 14(d)** showing a surface irradiated with a laser power of 0.2 J/cm^2, according to embodiments of the present invention;

[0028] FIG. 15 is graphical representation of an X-ray diffraction pattern of a laser treated germanium surface having nanospikes, according to an exemplary embodiment of the present invention;

[0029] FIG. 16 illustrates SEM images of treated surfaces, with **FIG. 16(a)** illustrating an image taken towards the edge of the scanned line for a Ge (100) surface, **FIG. 16(b)** indicating ball formation instead of spikes for a Ge (100) surface, and **FIG. 16(c)** illustrating an image taken in the middle of the scanned line for a Si (100) surface, according to exemplary embodiments of the present invention;

[0030] FIG. 17 illustrates SEM images of pillars, viewed at 45° from the surface normal, formed on a silicon surface, with **FIG. 17(a)** illustrating an SF_6 gaseous environment, and **FIG. 17(b)** illustrating an HCl gaseous environment, according to exemplary embodiments of the present invention;

[0031] FIG. 18 illustrates SEM images of pillars, viewed 45° from the surface normal, formed on a germanium surface, with **FIG. 18(a)** illustrating an SF_6 gaseous environment, and **FIG. 18(b)** illustrating an HCl gaseous environment, according to exemplary embodiments of the present invention;

[0032] FIG. 19 illustrates SEM images periodic structures formed on a silicon surface, with **FIG. 19(a)** illustrating a one-dimensional periodic structure, and **FIG. 19(b)** illustrating a two-dimensional periodic structure, according to embodiments of the present invention;

[0033] FIG. 20 illustrates SEM images of titanium surfaces, with **FIG. 20(a)** illustrating a titanium surface treated in air, **FIG. 20(b)** illustrating a titanium surface treated in vacuum, **FIG. 20(c)** illustrating a titanium surface treated in helium, and **FIG. 20(d)** illustrating a

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titanium surface treated in SF_6, according to exemplary embodiments of the present invention;

[0034] FIG. 21 illustrates SEM images of stainless steel surfaces, with **FIG. 21(a)** illustrating a stainless steel surface treated in air, **FIG. 21(b)** illustrating a stainless steel surface treated in vacuum, **FIG. 21(c)** illustrating a stainless steel surface treated in helium, and **FIG. 21(d)** illustrating a stainless steel surface treated in SF_6, according to exemplary embodiments of the present invention;

[0035] FIG. 22 illustrates SEM images viewed at 45° from the surface normal, with **FIG. 22(a)** illustrating a treated SiC surface, **FIG. 22(b)** illustrating a treated GaAs surface, **FIG. 22(c)** illustrating a treated titanium surface, and **FIG. 22(d)** illustrating a treated stainless steel surface, according to exemplary embodiments of the present invention;

[0036] FIG. 23 is a schematic representation of field emission from the treated surface, according to exemplary embodiments of the present invention;

[0037] FIG. 24 is a schematic representation of reflectivity and absorption of the treated surface, according to exemplary embodiments of the present invention;

[0038] FIG. 25 is a schematic representation of the effect on external flow by the treated surface, according to exemplary embodiments of the present invention;

[0039] FIG. 26 is a schematic representation of photovoltaic and photodetection applications using the treated surface, according to exemplary embodiments of the present invention;

[0040] FIG. 27 is a schematic representation of heat dissipation using the treated surface, according to exemplary embodiments of the present invention;

[0041] FIG. 28 is a schematic representation of surface marking created by surface alternations, according to exemplary embodiments of the present invention; and

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[0042] FIG. 29 is a schematic representation of the placement of chemical or biochemical materials at the tips on the treated surface, according to exemplary embodiments of the present invention.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS OF THE INVENTION

[0043] In describing an exemplary embodiment of the present invention illustrated in the drawings, certain specific terminology will be used for the sake of clarity. However, the invention is not intended to be limited to that specific terminology, and it is to be understood that the terminology includes all technical equivalents that operate in a similar manner to accomplish the same or a similar result.

[0044] Apparatuses and methods consistent with the present invention texture and crystallize the surface of a material in one step by exposing the surface of the material to an ultrafast laser. In order to expose an area of the surface that is larger than the beam spot size, the material may be translated relative to the laser. The texturing causes pillars to form on the surface of the material, increasing the light absorption of the treated material. Pillars are height variations over a surface, including valleys and hills. Pillars can be formed in a variety of shapes, including conical, arrowhead, pyramid, and spheroid structures. The top of the pillar has a narrower diameter than the bottom of the pillar. Additionally, crystallization increases the electrical conductivity of the treated material. Texturing and crystallizing the surface of the material in a single step allows for faster manufacturing and lower costs than performing these steps separately.

[0045] The texturing and crystallization may be performed under atmospheric conditions, or while the material to be treated is in a non-atmospheric gaseous environment. In such a gaseous environment, additional surface texturing will occur through chemical etching. Sulfur hexafluoride and hydrogen chloride gases have been examined, and have been shown

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to be suitable gases in which to perform the surface texturing. Hydrogen chloride is advantageous over sulfur hexafluoride, because when sodium hexafluoride is used, impurities in the material may result. In contrast, when hydrogen chloride is used, no impurities are created, and the material remains in its pure form. It is to be understood that other gases may also be used. Surface texturing and crystallization have also been achieved in a helium gas environment and in a vacuum.

[0046] The materials that have undergone surface texturing and crystallization are also within the scope of the present invention. For amorphous materials, the surface will become textured and the material will become crystallized. Hydrogenated amorphous silicon has been examined using the method of the invention, and has been shown to be well-suited to benefit from this method. Thin-film, poly-crystalline, and single crystal materials may also be used. These materials will benefit from the surface texturing methods of the present invention. Silicon and germanium have been studied, and have been shown to be suitable materials to undergo the laser treatment method in the presence of sodium hexafluoride gas and hydrogen chloride gas. Metals, dielectrics, and polymers have also been shown to be suited to be textured using the method of the present invention. However, it is to be appreciated that other materials are suited to undergo the laser treatment methods of the present invention.

[0047] Additionally, the use of materials that have undergone the treatment methods of the present invention is within the scope of the present invention. The present invention has many useful applications. The methods described herein will provide for a material with a higher light absorption capacity and a higher electrical conductivity than an untreated material. These two properties are desirable in photovoltaic applications. Enhanced light trapping capabilities are also useful in photo-sensing applications. Photodetectors utilizing

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the present invention will be more sensitive to light, and will be able to detect a broader spectrum of electromagnetic waves.

[0048] The surface texturing greatly enhances the heat transfer capability of a given material. A material that has been textured can dissipate more heat through convection because of the increased surface area of the material that is exposed to a fluid flowing over the material. Additionally, the texturing will ensure a turbulent flow of the fluid, which is advantageous in convection heat transfer. For radiation heat transfer, the increased surface area will allow for more heat dissipation.

[0049] In an exemplary embodiment of the present invention, the surface alteration process was performed on hydrogenated amorphous silicon (a-Si:H), in particular a-Si:H thin films. Thin films with thicknesses from 1.5 to 2 μm were deposited on glass substrates, using a low temperature Plasma Enhanced Chemical Vapor Deposition (PECVD) technique. The a-Si:H films were deposited at a rate of around 1 Å/s in a hydrogen diluted silane environment at about 200°C. The samples were then treated using a femtosecond Ti:Sapphire laser system (Spectra-Physics Spitfire). The laser system delivered pulses at a repetition rate of 1 kHz, with a pulse energy that could vary from 0-1.2 mJ, and a wavelength of 800 nm. The wavelength of the laser can also be frequency doubled or halved to achieve wavelengths from 200 to 1600 nm. The temporal profile of the pulses was measured to be 110 fs using a background free, scanning second-order auto-correlator. The sample was placed on a stationary stage, and the laser beam was deflected by a Scanlab galvo-head to scan the sample surface. The beam spot on the sample surface was circular, with a beam diameter of 0.5 mm. The beam scanning speed was around 12.5 cm/sec. Scanning electron micrographs of treated and untreated surfaces of the a-Si:H films were taken using a Cambridge Instruments high resolution electron microscope for a surface texture study.

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Surface roughness and formation of spikes in the treated films were also examined with an atomic force microscope (Digital Instruments Nanoscope III).

[0050] The optical transmission and reflection of a 20 mm x 30 mm laser treated area of the sample was measured using a PERKIN-ELMER LAMBDA 9 spectrophotometer. The reflectance and transmittance percentages were then used to obtain the absorption percentage in the material: $A = 100 - R - T$. Light from a He-Ne laser source was incident on the treated sample at different angles, and the scattered light was measured by a silicon sensor with an active region of around 4 cm^2 to estimate the scattering of light due to texturing. It was observed from the measurements that scattering might contribute to a 5-10% variation in the reflection measured by the spectrophotometer. In addition to the optical properties, X-ray diffraction (XRD) was performed on the untreated and laser treated samples to study the structural modification induced by the laser treatment. The Rigaku Miniflex 2005 X-ray diffractometer with a Cu target (CuK_{α} -line) was used for the XRD measurements. The grain size of the treated films was estimated from the X-ray data. Also, the oxygen incorporation into silicon films during this ultrafast laser treatment was studied using a Physical Electronics Inc. 560 XPS/SAM spectrophotometer with a dual source anode (Mg/Al) radiating 1253.6 eV X-ray photons.

[0051] FIG. 1 shows an exemplary system 100 that can be used to provide surface modifications. The femtosecond laser system 101 provides a laser pulse incident on the a-Si:H sample 105, which is supported by an X-Y sample stage 106. The system 100 uses a mirror 102 to direct the laser pulse to a galvo-head unit 103, which scans the sample surface. A focusing lens 104 is used to focus the pulses on the surface. An exemplary a-Si:H sample 200 is illustrated in FIG. 2, with a glass slide 205, an intervening layer 204, and amorphous silicon layers 201-203.

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[0052] FIG. 3 illustrates that the change in the surface of the a-Si:H film deposited on the glass substrate can be observed optically. FIG. 3(a) shows a photograph of the untreated surface, and FIG. 3(b) shows a photograph of the treated surface. After treatment, the a-Si:H films turned completely dark, in contrast with their original shiny reddish gray color. FIG. 4(a) shows an SEM image of the untreated surface, and FIG. 4(b) shows an SEM image of the treated surface. FIG. 4(b) shows that microstructures and small spikes have been spontaneously formed upon laser treatment.

[0053] In order to study the optical characteristics, the reflectance and transmittance of a treated 20 × 30 mm^2 area were measured using a spectrophotometer. FIG. 5 shows the absorptance of treated and untreated a-Si:H films. FIG. 5(b) that there is a significant enhancement in the optical absorption below a-Si:H band gap (1.7 eV) for treated films, when compared to the untreated films in FIG. 5(a). Since the experiments were carried out under atmospheric conditions, XPS spectra of a treated sample (FIG. 10(b)) and an untreated control sample (FIG. 10(a)) were also obtained. SiO_x formation was observed in the treated sample. The oxygen concentration was estimated by taking XPS measurements at different depths of the sample. Depth profiles of the oxygen concentration in the treated and untreated control samples are shown in FIG. 10(c). Traces of oxygen were observed up to a depth of around 50 nm in treated samples, compared to a depth of 10 nm in the untreated control sample. The samples appeared to be pitch black after treatment, and it is suggested that the below-band edge absorption might be due to trapping the light, which is caused by multiple reflections from the textured surface. Also, structural defects induced during the micro-structuring process most likely produce bands of defect and impurity states in the bandgap, and further enhance the overall absorption.

[0054] FIG. 6(a) shows the X-ray diffraction pattern for an untreated a-Si:H sample, and FIG. 6(b) shows an X-ray diffraction pattern for a treated a-Si:H sample. Peaks around 2θ =

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30° and 56° are observed for the treated sample. These peaks are absent in the untreated control sample, indicating a structural change after laser treatment. The X-ray wavelength used for these measurements was the CuK_{α} line at 1.54 Å. The observed peaks are due to the (111) and (311) orientations of crystalline silicon. Regardless of the fluence conditions, the (111) orientation dominated in the crystallized films, as the (111) plane has least surface energy. Dominant (111) and (311) peak formation is typically observed in nanosecond laser crystallization. The (111) peak was fitted with a Gaussian curve and the full width at half-maximum (FWHM) was determined. The particle size was determined to be around 85 nm using the Scherrer's formula: $L = k^{*}\lambda / \Gamma \cos\theta$; where λ is the X-ray wavelength for measurement; Γ is the X-ray line width (FWHM) (measured in radians); θ is the Bragg angle of diffracted rays (measured in degrees); and k is a constant equal to 0.9.

[0055] The current-voltage characteristics of the treated and untreated a-Si:H samples were also examined, as shown in FIG. 7. FIG. 7(a) shows a graph of the current density as a function of voltage for several light levels for the untreated sample. As illustrated in FIG. 7(b), the current-voltage characteristics change considerably, due to the surface modification and changes in the properties of the material. The transmission and reflectivity of the treated and untreated surfaces were also examined. The reflectivity of polished silicon, unpolished silicon, and treated silicon with pillars is shown in FIG. 11. Similarly, the transmission of the treated silicon versus the rough silicon surface is presented in FIG. 12. The changes in the optical properties shown in FIG. 3 are further substantiated by the changes in reflectivity and transmission as functions of wavelength. These results impact the use of silicon in many applications, as discussed below.

[0056] In order to measure the roughness and spike distribution, atomic force microscopy (AFM) images of the treated a-Si:H samples were obtained. FIG. 8 shows that spikes of a height of about 300 nm were formed, with a spacing between the tips of around 1 μm. The

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heights of these spikes were found to increase with laser fluence. The average height of the microstructures was 150 nm at a laser fluence of 0.3 J/cm^2, and the height increased nearly linearly with the laser fluence. Microstructures with a height of around 350 nm were observed at a fluence of 0.5 J/cm^2. Beyond 0.5 J/cm^2, the films became very rough, and material ablation deteriorated the texturing. Also, the average roughness of the surface correlates with the laser fluence, as illustrated in the graph in FIG. 9. FIG. 9 shows that the surface roughness increases approximately linearly with the laser fluence.

[0057] Increasing the efficiency of a-Si:H thin film solar cells requires more light absorption and a reduction in carrier recombination. A thick i-layer increases the light absorption, but recombination deteriorates the performance. On the other hand, for sufficiently thin film solar cells, the light absorption becomes an issue. Keeping a thin micro or nano crystalline phase with surface texturing could both reduce recombination and improve light trapping. The treated surface had a silicon oxide formation layer of about 50 nm, and was found to be semiconducting. This layer could be used as an n-layer in a p-i-n type solar cell, and an active layer for other optoelectronic devices. The simultaneous formation of light trapping structures and crystallization might find applications in devices such as thin film solar cells, large area sensors, and display devices.

[0058] As discussed previously, the femtosecond laser treatment results in the enhancement of optical absorption in a-Si:H thin films. The high absorption of the film is suggested to be due to the light trapping occurring in the silicon spikes formed at the surface after laser treatment, and the structural defects induced during micro structuring process most likely producing bands of defect and impurity states in the band gap. Also, crystallization in the film after femtosecond laser treatment is attributed to a non-thermal ultrafast phase transition and subsequent surface-initiated crystallization. By performing the surface

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texturing and crystallization as a one-step laser process, optoelectronic devices can be fabricated efficiently.

[0059] Exemplary embodiments of the present invention also form nanospiked, nearly periodic microstructures, by exposing a germanium surface to femtosecond laser pulses in a gaseous sulfur hexafluoride (SF_6) environment. The microstructures that are formed in germanium have a different aspect ratio than the microstructures formed on silicon. Because reducing light reflection and increasing absorption are key issues in improving optoelectronic device performance, this type of microstructure formation in germanium could lead to the fabrication of highly responsive infrared photodetectors and solar cells. In addition, these textured surfaces might find potential applications in the fabrication of biomedical devices and sensors.

[0060] The surface modification of germanium can occur according to the following process. Undoped Ge (100) wafers are cleaved into small chips and ultrasonically cleaned with acetone and methanol. One or more chips are put on a stage inside a vacuum chamber with a base pressure of around 1 mTorr, which is mounted on a high-precision computer-controlled X-Y stage. The chamber is rinsed with SF_6 at least twice, and then backfilled with SF_6 at 400 mbar. The samples are exposed to 1.4 mJ pulses of light with a wavelength of 800 nm, a pulse duration of 130 fs, and a repetition rate of 1 kHz from a regeneratively amplified Spectra-Physics Ti-sapphire laser system. The wavelength of the laser can be frequency doubled or halved to achieve wavelengths from 200 to 1600 nm. Short laser pulse widths can also be used, including 1 fs to 1 μs pulses. Ultrafast laser pulses are a subcategory of short pulses, and can range from 1 femtosecond to hundreds of picoseconds. The laser beam is focused along the surface normal onto the sample surface by a coated lens with a focal length of 1 m, and the laser fluence is adjusted with a Glan laser calcite polarizer.

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[0061] The spatial profile of the laser pulse is nearly Gaussian, but is elongated in one axis, creating an elliptical profile. The fluence is calculated by using the laser spot size, which is determined by exposing a point on the sample surface to thousands of shots. In order to scan an area that is bigger than the laser spot size, the samples are translated using a motorized X-Y stage. Scanning also assists in making the surface structure more uniform by smoothing out any shot-to-shot irregularities in the beam profile. By varying the scanning speed of the X-Y stage, the number of laser pulses impinging on the sample surface at a particular location is controlled. The spot size is 0.3 mm along the minor axis and 0.6 mm along the major axis. Scanning is performed parallel to the minor axis.

[0062] Samples are produced with isolated single line scans, or with large areas created by overlapping several line scans. The step size between the scan lines is chosen to be sufficiently small (generally 0.38 mm), so that successive lines overlap substantially. This further improves layer homogeneity. Homogeneity is further enhanced by performing two overlapping scans in orthogonal directions, rather than one overlapping scan with an exposure of the same total number of shots. After laser processing, the samples are analyzed with a scanning electron microscope (Zeiss SUPRA 40).

[0063] FIG. 13 shows an SEM image at increasing levels of magnification, viewed at 45° from the surface normal line of a germanium surface after exposing the surface to femtosecond laser pulses. Sharp conical structures with nanospikes are formed when the sample is under a pressure of 400 mbar SF_6, and is scanned by a laser beam with a fluence of about 0.6 J/cm^2. FIG. 13 shows that these structures are almost regular in position, are 10 to 15 μm tall, and have a base diameter around 5 μm, which tapers down to around 100 nm near the tip. The areal density of pillars in FIG. 13(a) is 0.027 μm^{-2}, which corresponds to a mean spacing of roughly 6 μm between pillars. The sizes of the microstructures vary across the scanned line, indicating a response to the spatial profile of the laser pulse. In the region of

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low fluence towards the edge of the irradiated line, the structures have a smaller height and are more densely packed than in the center.

[0064] FIG. 13(b) shows that the microstructures have two distinct features: (a) a conical shape (b) that is crowned with a very sharp spike, which has a radius of about 400 nm (about 100 nm at the tip), and is up to about 2 μm long (see FIG.13(c)). The tips can be sharpened further by a brief chemical etching with 100 ml H_2O_2 (10 vol %), 8g NaOH for 10 seconds at room temperature. Alternatively, the tips can be sharpened further by ion etching, including etching with an Argon ion beam. Nanoclusters, which are formed during laser ablation and deposited on the surface, are also evident from FIG. 13(b).

[0065] The SEM images of FIG. 14 show the effect of laser fluence on the surface texturing of germanium. In this figure, the average number of laser shots at each point on the sample surface is 400. The germanium surface in FIG. 14(a) was irradiated with laser pulses with a fluence of 0.66 J/cm^2, and the germanium surface in FIG. 14(b) was irradiated with laser pulses with a fluence of 0.56 J/cm^2. In contrast, the germanium surface in FIG. 14(c) was irradiated with laser pulses with a fluence of 0.3 J/cm^2, and the germanium surface in FIG. 14(d) was irradiated with laser pulses with a fluence of 0.2 J/cm^2. FIG. 14(d) shows that texturing is observed at fluences as low as 0.2 J/cm^2, resulting in features are smaller in width and height, less regular, less smooth, and densely populated, with very tiny or no spike formation. However, for higher fluence conditions, such as those in Figs. 14(a) and 14(b), the structures are more well-developed, sharper, and more conical, and spike-formation takes place atop the pillars. Also, increasing the number of laser shots from 400 to 600 and keeping the fluence almost the same wipes out all the spikes.

[0066] Germanium expands upon freezing. When a shell of germanium material starts freezing and expanding, it exerts pressure on the liquid trapped inside, causing the liquid to shoot upward and solidify to form nanospikes. As Mills and Kolasinski disclose, in order to

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obtain nanospikes in silicon, it is necessary to dilute the SF_6 with He. This reduces the chemical etching that results from the interaction of fluoride with the silicon surface. If the etching is too aggressive, it can remove the nanospikes. In contrast, it is unnecessary to dilute the SF_6 in order to obtain nanospikes on a germanium sample, probably because of differences in the chemistry of etching in the F/Ge system compared to the F/Si system. Another possible reason why germanium appears to be more conducive for nanospike formation might be that the thermal conductivity of undoped germanium is less than half of the thermal conductivity of undoped silicon. Therefore, the heat dissipation to the pillar in germanium is slower, and the liquid bulb remains in a molten state for a longer time, as compared to silicon.

[0067] In order to investigate the properties of the textured germanium surfaces, an X-ray diffraction study was conducted. FIG. 15 shows an X-ray diffraction spectrum of a laser textured germanium surface. The sharp high-intensity peak corresponds to the (400) plane, because the starting material is Ge (100). However, two relatively weak peaks at (111) and (220) are also observed. This indicates that the textured pillars and the nanospikes remain predominantly crystalline.

[0068] The SEM images of FIGs. 16(a) and 16(b) show the structural formations in germanium, and FIG. 16(c) compares the structural formations in silicon, after laser treatment under similar conditions. For all three samples the laser fluence was around 0.56 J/cm^2, the number of laser shots was around 600, the sample was in a gaseous SF_6 environment at 400 mbar, and an orthogonal scanning mode was used. The SEM image in FIG. 16(a) was taken toward the edge of the scanned line, while the SEM image in FIG. 16(b) was taken in the middle of the scanned line. FIG. 16 shows that the germanium pillars are not as smooth as the silicon pillars. Also, the aspect ratio, defined as the ratio of the tip height to the tip width, is higher in silicon than germanium for a given laser condition. For example, at a fluence of

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0.5 J/cm^2, silicon has an aspect ratio of around 200, whereas germanium has an aspect ratio of around 100. Also, as mentioned previously, spikes were not formed on germanium under higher laser shot conditions. However, pillars formed under higher laser shot conditions are taller than pillars formed under fewer shots, as shown in FIGs. 13 and 14. In contrast, silicon shows a well-developed smooth structure under a greater variety of shot conditions.

[0069] FIG. 16(a) shows that toward the edge of the laser scanned line on the germanium surface, pyramidal structures were formed, which tend to form a small spherical cap at the top, instead of the nanospikes formed in FIG. 16(b). This spherical cap formation is typical of silicon. The spherical shape of the cap suggests that a liquid germanium drop resolidified before it could spill over the pillar. The lack of nanospikes in FIG. 16(a) might be due to three possible reasons: (a) the fluence is low to achieve the high melting condition necessary for nanospike formation; (b) the higher number of laser shots destroyed nanospikes that were already formed; or (c) an insufficient density of nanostructures was formed. With further regard to (c), deposition of nanoclusters has been implicated in the formation of nanospikes. A sufficient nanoclusters deposition rate is required, and because fewer nanoclusters are formed at a lower fluence, there may be a critical fluence for the formation of nanospikes, not only because a sufficient melt must be formed, but also because a sufficient density of nanoclusters must be created.

[0070] FIG. 17 shows SEM images viewed at 45° from the surface normal of sharp conical pillars formed on the surface of B-doped Si (100) wafers. The pillars were produced with 240 shots of 130-fs laser pulses at a fluence of 0.6 J/cm^2. FIG. 17(a) shows the results for a sample in 400 mbar of SF_6, and FIG. 17(b) shows the results for a sample in 400 mbar of HCl. The pillar size varies across the scanned laser line, indicating the intensity variation of the laser fluence across the spatial profile of the laser pulse. The scan lines were

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overlapped to minimize height variation over a large area on the sample surface. The spikes that are obtained in SF_6 are around 15 μm tall and have a base diameter of around 5 μm.

[0071] On the other hand, the structures formed under similar laser conditions in the presence of HCl are composed of taller and wider pillars, with a height of around 20 μm and a base diameter of around 7 μm. FIGs. 17(a) and 17(b) show that the pillars formed in SF_6 are narrower towards the tips, compared to the pillars formed in HCl. Although the pillar density is comparable in both cases, the pillars formed in HCl look stronger and are relatively blunt towards the tip, indicating that differences in the etch chemistry of the F/Si system and the Cl/Si system are responsible for significant structural differences.

[0072] The role of chemistry in structure formation is not well understood, and it is a significant result that regular conical pillars are formed during femtosecond irradiation in SF_6 as well as HCl. Regular conical pillars can be formed during nanosecond irradiation of silicon in the presence of SF_6, but they are not formed for nanosecond irradiation of silicon in the presence of HCl. Nanosecond irradiation of silicon in HCl produces significantly blunter tips, the pillars are much taller, with a height greater than 50 μm, and the pillars are porous, instead of having a solid core. This is a further indication that the mechanisms of pillar formation are different for the femtosecond and nanosecond irradiation regimes. This result is also significant because chemical impurities, namely sulfur, incorporated during laser processing have been implicated in changing the optical and electronic properties of the textured surfaces.

[0073] FIG. 18 shows SEM images taken for germanium samples treated under similar laser and gaseous conditions as described above for silicon. A very different surface texturing was created for germanium. FIG. 18(a) shows that for germanium processed in SF_6, there were two distinct features that were not observed for silicon treated under similar conditions: (a) conical pillar formation with a higher cone angle up to a neck; and (b) very

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sharp spikes, up to about 2 μm in length with a tip radius of about 100 nm, formed atop the pillars. Nanoclusters formed during laser ablation are more abundant in germanium than silicon under similar laser conditions, which might be due to the lower melting temperature of germanium. On the other hand, FIG. 18(b) shows that the germanium structures formed in the presence of HCl are less densely populated, shorter, have a higher cone angle and a wider base, and exhibit greater variations in pillar height than the silicon structures shown in FIG. 17(b). Gas phase silicon etching is anisotropic in HCl, and the etch rate is around 20 μm min^{-1} for the (100) plane at temperatures in the range of 1050–1250°C, whereas in germanium the etch rate is around 3 μm min^{-1}, the etch rate is independent of temperature beyond 800°C, and etching leads to the development of square pits for the (100) orientation. The differences in etch chemistry are involved in determining the different structure formation dynamics, which result in more regular spike formation in HCl for silicon than for germanium.

[0074] Laser induced surface texturing that produces regular structures on materials in the presence of reactive species is a complex process involving: (1) interactions between the plume and the process gas, and the plume and the surface, such as decomposition of the reactive gas, chemical etching enhanced by laser heating of the material and the formation of radicals, and deposition out of the plume; (2) laser ablation of the material; and (3) optical phenomena that initiate the formation of regular structures. The laser parameters, gaseous environment, and nature of the substrate all play a role in the final outcome of the surface morphology. Structure formation is ultimately a convoluted dynamical process involving all three factors. The dimensions and character of the pillars formed in silicon have been shown to depend critically on the temporal pulse width of the laser beam. While pillar production with pulse durations in the range of 100 fs to 20 ns has been demonstrated, with much smaller pillars being formed in the case of femtosecond irradiation, pillars were not producible with a

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300 ns Nd:VO_4 laser. It appears that laser pulses significantly shorter than the melt lifetime of about 250 ns are required for sharp pillar formation.

[0075] FIG. 19(a) illustrates an SEM image of a one-dimensional periodic structure made on a silicon substrate, according to exemplary embodiments of the present invention. FIG. 19(b) illustrates an SEM image of a two-dimensional periodic structure made on a silicon substrate, according to exemplary embodiments of the present invention. Periodic structures can be produced by controlling the laser intensity distribution on the surface of the sample. The laser intensity distribution can be controlled by using interference and diffraction. For example, interference fringes are created by placing a metal wire in a portion of the laser beam. The light diffracted by the wire interferes to produce an intensity distribution on the sample surface that results in a periodic structure of pillars. Alternatively, the incident laser beam is split into two components, and then recombined at various angles to control the periodicity. It is also possible to place several pinholes in the path of the laser beam to create a periodic circular pattern of pillars on the surface. By using laser beams with different wavelengths and controlling the interference patterns, the periodicity of the pillars can be adjusted from tens of nanometers to tens of micrometers.

[0076] In an exemplary embodiment of the present invention, copper or tungsten wires with diameters from 100 to 250 μm are used to create interference fringes. The sample is exposed to 1.4 mJ pulses of light with a wavelength of 800 nm, a pulse duration of 130 fs, and a repetition rate of 1 kHz. The laser scan speed is 0.1 in/sec, and scanning is performed after placing the sample inside a vacuum chamber filled with SF_6 at a pressure of 400 mbar. In order to create a two-dimensional array of pillars, the metal wires are crossed orthogonally and placed in the path of the laser beam. Also, the spacing between adjacent pillars can be controlled by changing the wavelength of the laser pulses. For example, when the laser wavelength is decreased, the spacing between adjacent pillars also decreases.

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[0077] In another exemplary embodiment of the present invention, the laser texturing method was performed on various metallic surfaces. A metal is defined as an electrically conducting material. For example, titanium and stainless steel sheets are cut into small square-inch sized chips and cleaned with acetone and methanol. One such chip is put on a stage inside a vacuum chamber with a base pressure of around 1 mTorr, which is mounted on a high-precision computer-controlled X-Y stage. The chamber is rinsed and then backfilled with air at atmospheric pressure, SF_6 in a pressure range from 75 to 800 mbar, or helium in a pressure range from 75 to 800 mbar. The laser texturing method can also be conducted with a mixture of gases in different proportions and at different pressures, or in vacuum, with a chamber pressure of around 1 mbar. The samples are exposed to ultrafast laser pulses with a pulse energy of 0.95 mJ, a wavelength of 800 nm, a pulse width of 130 fs, and a repetition rate of 1 kHz from a regeneratively amplified Spectra-Physics Ti-sapphire laser system. Short laser pulse widths can also be used, including 1 fs to 1 μs pulses. Ultrafast laser pulses are a subcategory of short pulses, and can range from 1 femtosecond to hundreds of picoseconds. The laser beam is focused onto the sample surface by a coated lens with a focal length of 1 m, and the laser fluence is adjusted by using a Glan calcite polarizer.

[0078] The spatial profile of the laser pulse is Gaussian, and the fluence is calculated by using the laser spot size, which is determined by exposing a point on the sample surface to thousands of shots. In order to scan an area that is bigger than the laser spot size, the samples are translated using a motorized X-Y stage. Scanning also assists in making the surface structure more uniform by smoothing out any shot-to-shot irregularities in the beam profile. By varying the scanning speed of the X-Y stage, the number of laser pulses impinging on the sample surface at a particular spot is controlled. The spot size is about 0.3 mm.

[0079] Samples are produced with isolated single line scans, or with large areas created by overlapping several line scans. The step size between scan lines is chosen to be

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sufficiently small (less than 0.38 mm), so that successive lines overlap substantially. This further improves layer homogeneity. Homogeneity is further enhanced by performing two overlapping scans in orthogonal directions, rather than one overlapping scan with an exposure of the same total number of shots. After laser processing, the samples are analyzed with a scanning electron microscope (Zeiss SUPRA 40).

[0080] FIG. 20 shows SEM images of titanium surfaces treated with the laser texturing method for different background gas conditions. FIG. 20(a) shows an SEM image of a titanium surface treated in air, and FIG. 20(b) shows an SEM image of a titanium surface treated in vacuum. FIG. 20(c) shows an SEM image of a titanium surface treated in helium at a pressure less than 200 mbar, and FIG. 20(d) shows an SEM image of a titanium surface treated in SF_6 at a pressure greater than 400 mbar. As these figures show, pillar formation occurs in titanium that is treated with a laser fluence from 0.6 to 1.0 J/cm^2, and in vacuum or gas at low pressures less than 200 mbar. In order to create a well-developed pillar on titanium, it is necessary to irradiate the sample with around 1000 shots. However, increasing the number of shots or the laser fluence destroys the pillars.

[0081] FIG. 21 shows SEM images of stainless steel surfaces treated with the laser texturing method for different background gas conditions. FIG. 21(a) shows an SEM image of a stainless steel surface treated in air, and FIG. 21(b) shows an SEM image of a stainless steel surface treated in vacuum. FIG. 21(c) shows an SEM image of a stainless steel surface treated in helium at a pressure less than 200 mbar, and FIG. 21(d) shows an SEM image of a stainless steel surface treated in SF_6 at a pressure greater than 400 mbar. As shown in the figures, laser texturing forms pillars on stainless steel surfaces in air, vacuum, helium, and SF_6. However, in order to create a well-developed pillar on stainless steel, it is necessary to irradiate the sample with around 2000 shots. Both the stainless steel samples and the titanium

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samples turn pitch black after laser treatment. However, unlike titanium, pillar formation occurs on stainless steel in air.

[0082] FIG. 22 shows a series of SEM images viewed at 45° from the surface normal, which compares the results of the laser texturing method for various semiconductors and metals. In each case the surface of the material is treated with ultrafast laser pulses with a pulse width of 130 fs. FIG. 22(a) shows an SEM image of SiC treated with 260 shots at a laser fluence of around 1 J/cm^2 in 400 mbar of SF_6. FIG. 22(b) shows an SEM image of GaAs treated with 260 shots at a laser fluence of around 0.5 J/cm^2 in 400 mbar of SF_6. FIG. 22(c) shows an SEM image of titanium treated with 2000 shots at a laser fluence of around 0.3 J/cm^2 in 400 mbar of SF_6. FIG. 22(d) shows an SEM image of stainless steel treated with 2500 shots at a laser fluence of around 4.5 J/cm^2 in 400 mbar of SF_6. These figures show that the laser texturing method can form pillars on various semiconductors and metals.

[0083] In addition, the laser texturing method is likely to form pillars on ceramics, polymers, and alloys. By controlling the processing conditions of the laser texturing method for each material, the thermal, structural, optical, and electronic properties of the material can be tailored. Further, the formation of pillars can be controlled by changing the polarization state of the laser beam. A polarizer can change the output from the laser to be linearly, circularly, elliptically, or randomly polarized. The laser texturing method can be performed on surfaces of any geometrical shape, and is not limited to planar surfaces.

[0084] Similarly, the laser texturing method could also be used to process transparent materials, such as glass. The incident light could be absorbed by a two-photon process, or an appropriate wavelength could be selected for absorption by the transparent material. The altered surfaces formed by this method could be used in magnetic disk drives, because the disk drive and the head are spaced very closely together for data writing and reading.

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[0085] The altered surfaces formed by the apparatuses and methods of the present invention can have great utility in photovoltaic technologies, as schematically illustrated in FIG. 26. The increased light trapping and the control of photogenerated charges can provide improved efficiency. In particular, the altered surfaces would be beneficial in photodetectors, because the surfaces allow for the development of more sensitive detectors with a high responsivity, and extend the spectral range into the infrared region of the spectrum. This could also enable the building of infrared sensors for various applications.

[0086] The altered surfaces would also be beneficial in heat dissipation, as schematically illustrated in FIG. 27. A large surface area is created by texturing, which allows gas molecules to exchange energy with the surface, and increases heat dissipation. Such a high-efficiency heat sink could be very important for microelectronics, power electronics, optoelectronics, and other devices that require efficient heat dissipation.

[0087] The altered surfaces can also be used in field emission, as schematically illustrated in FIG. 23. Due to the sharp geometry of pillars formed by the laser texturing process, very high electric fields can be generated at relatively low voltages. These high electric fields can be used for electron emission from surfaces, providing an efficient source of electrons for various electronic and optoelectronic device applications, such as field emission displays, sensors, and instruments.

[0088] The altered surfaces would also be beneficial in surface property control, as schematically illustrated in FIG. 25. Laser textured surfaces can be made hydrophobic or hydrophilic by controlling the texture and surface coating. This can affect the air or fluid flow across the surface of the material.

[0089] The altered surfaces would also be beneficial in micro fluidic applications. There is an increasing number of micro fluidic applications for chemical and biomedical applications of chips. As schematically illustrated in FIG. 25, textured surfaces in micro

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channels can provide a good method of controlling the fluid flow, which can impact DNA sequencing and other applications. The altered surfaces would also be beneficial in turbulence control for aerodynamic applications. The flow of gases can be controlled by inserting a textured surface into the flow path. Also, turbulence can be generated by using of textured surfaces. This effect can be used in aerospace applications.

[0090] The altered surfaces would also be beneficial in an optical beam block, as schematically illustrated in FIG. 24. The laser textured surface has an extremely low reflectance and transmittance in the visible to the far infrared region, allowing the surface to be an efficient beam block for various optical and manufacturing applications. The altered surfaces would also be beneficial in controlling the visual appearance of products, including the surface color. The laser texturing process provides a completely black surface, hence it can be used to control the color of the surface without using any paints, dyes, or pigments.

[0091] The altered surfaces would also be beneficial in catalytic activity, as schematically illustrated in FIG. 29. The large surface area created by texturing provides many sites for enhanced chemical activity, such as catalytic activity. These catalytic activities would be useful in fuel cell technology, chemical plants, and biomedical applications, including conversion of carbon monoxide to carbon dioxide. The large surface area can also be used for enhanced tissue growth and control. The altered surfaces would also be beneficial in bond strength improvement. The large surface area created by texturing allows more sites for bonding and interlocking, and improves the overall bond strength.

[0092] The altered surfaces would also be beneficial in thin film or fibrous whisker growth. Due to the formation of nanospikes or microspikes, it is possible to utilize a large number of tips for growth of other materials atop these tips, as schematically illustrated in FIG. 29. Also, because a small voltage can provide a high electric field, the growth can be controlled by the electric field.

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[0093] The altered surfaces would also be beneficial in the production of nano or micro tips, as schematically illustrated in FIG. 29. Because the texturing process produces a large array of two-dimensional structures, micro or nano ordered tips can be fabricated. The nanospikes can be solid or hollow. These tips can be used in atomic force microscopy, optical data storage, and fluid control for automobiles and drug delivery.

[0094] The altered surfaces would also be beneficial in surface-enhanced Raman scattering. The Raman scattering method can be used to detect chemical or biochemical species. Usually Raman scattering signals are relatively low, but a Raman signal can be enhanced by many orders of magnitude by surface-enhanced Raman scattering. Laser textured surfaces coated with metals could provide an ideal template for surface-enhanced Raman scattering for sensor applications, such as single molecule detection. The altered surfaces would also be beneficial in biosensor applications. As schematically illustrated in FIG. 29, specific molecules can be attached atop the tips, and can be used for chemical or biochemical detection, by using methods such as fluorescence and phosphorescence.

[0095] The altered surfaces would also be beneficial in manufacturing optical elements. As schematically illustrated in FIGs. 24 and 28, various optical elements, such as diffraction gratings, low scattering surfaces, and antireflection surfaces can be prepared by texturing the optical element surface. Also, light absorption properties can be tailored by adjusting the laser parameters and thermal annealing conditions.

[0096] The altered surfaces would also be beneficial in photonic crystals. Photonic crystals are increasingly used for optoelectronic applications, such as wavelength selection and fabrication of negative refractive index materials. Periodic textured surfaces fabricated by laser texturing would be useful in these photonic crystals. The altered surfaces would also be beneficial in producing masters for replication. A textured surface can be used as template for transferring a pattern to a softer material by using mechanical pressure, with or without

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heat. This can provide a very low cost process for pattering surfaces such as compact discs. This process can also be used for transferring patterns to polymerics and biomaterials.

[0097] The altered surfaces would also be beneficial in fabricating mask-less periodic structures. By using an optical interference technique, periodic textured surfaces can be fabricated with a sub-micron period, without any mask fabrication. The altered surfaces would also be beneficial in pixelated devices. Some optoelectronic and microelectronic devices, such as CCD cameras, diode lasers, and light emitting diodes, require a two-dimensional geometry. Two-dimensional textured surfaces can be easily fabricated for optoelectronic and microelectronic applications. The altered surfaces would also be beneficial in producing substrates for single crystal film or nanoparticle growth.

[0098] The altered surfaces would also be beneficial in nano or micro pores. Textured surfaces can be further processed with chemical etching to provide a large number of nano or micro pores, which can be used for filtration or fluid flow control. Pores can be made by the laser texturing process if thin substrates are used, or if longer processing times are used. The altered surfaces would also be beneficial in controlling surface emissivity. By adjusting the surface texture, the surface emissivity and spectral properties can be controlled. This can provide camouflage objects, because such objects are harder to detect if they emit a low radiation signal.

[0099] The altered surfaces would also be beneficial in art and photography applications. As schematically illustrated in FIG. 28, laser texturing of surfaces can be used to write text and images on surfaces by controlling the light reflectivity of the surface. This technique can be used to produce name plates, part identification, hidden logos, trademarks, logos, and images. The texturing provides a black color, which produces a very high contrast between the written and unwritten areas. The process of the present invention can also be used to control the gray level in forming high definition images.

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[00100] The altered surfaces would also be beneficial in radiation shielding. Laser textured surfaces provide a very good method for controlling radiation scattering, reflection, absorption, and transmission over a broad spectral range, including visible, infrared, microwave, terahertz, and radio waves.

[00101] The altered surfaces would also be beneficial in plasma applications. Sharp tips can provide a very high electric field, and hence can be used for localized or large area generation of plasma sources. These plasma sources can be used to purify water, kill germs, and destroy bio-chemical agents.

[00102] The altered surfaces would also be beneficial in protecting substrates from corrosion, and improving adhesion, such as epoxy adhesion to a metal surface. They can also be used to improve the adhesion of thin films to a surface, such as a TiN coating on drill bits, which would extend the lifetime of the drill bits.

[00103] The altered surfaces would also be beneficial in bone grafting applications. Body implants can become detached from the host tissue, due to inadequate biocompatibility and poor osteointegration. Using laser texturing to change the surface chemistry and physical texture of the implants can improve the biocompatibility and adhesion.

[00104] The altered surfaces would also be beneficial in controlling the tribological properties of materials, such as friction, wear resistance, load-bearing properties, and lubrication. The textured surface can act as a micro-hydrodynamic bearing, a micro-reservoir for a lubricant, or a trap for debris particles generated during a sliding or other motion. This could result in significant friction reduction in piston rings. Similarly, laser texturing of cylinder liners in the interior of an engine compartment could reduce wear, friction, oil consumption, and gas emissions.

[00105] Instead of performing the laser texturing method in chemical gases, the method could be performed in the presence of gaseous plasma. Because charged species in gaseous

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plasma can be very reactive, laser irradiation in the presence of gaseous plasma will provide a much faster speed for texture formation, and further enable control of surface properties. Plasma sources can be created by various methods, such as excitation with a radio frequency (RF) source, direct current (DC), alternating current (AC), or a laser system. This approach provides a method for multi-energy processing technology, where electrical energy for plasma or discharge creation, laser irradiation for melting and ablation, and chemical energy by the gaseous environment are utilized to enhance the process and the control of the surface properties. Also, the sample can be kept at elevated temperatures, or the sample surface can be irradiated by an infrared lamp to raise the surface temperature, in order to enhance the chemical reactions or reduce the laser energy. In addition, plasma or ion etching methods are commonly used for semiconductor chip fabrication and preparation of samples for transmission electron microscopy. The addition of ultrafast pulsed laser energy could be used to further enhance this process.

[00106] Combining the laser texturing method with various other processes would also be beneficial. For example, a one-step process for doping, texturing, and crystallization would be advantageous from a manufacturing standpoint. Also, laser texturing and laser surface cleaning could be combined to provide a one-step process. In addition, laser texturing and surface passivation could be performed as a one-step process. The chemical gas used in laser texturing could provide the surface passivation by sulfur or phosphorous diffusion. Finally, laser texturing could be performed in a one-step process with surface hardening. For example, the surface of steel can be textured, and if a reactive gas such as ammonia or nitrogen plasma is used, surface nitridation can be achieved. This provides improved surface properties, such as wear, wetting characteristics, and chemical interactions.

[00107] The foregoing description and drawings should be considered as only illustrative of the principles of the present invention. The present invention may be configured and

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performed in a variety of ways, and is not intended to be limited by the exemplary embodiments discussed herein. Numerous applications of the present invention will readily occur to those skilled in the art who consider the foregoing description. Therefore, the present invention is not to be limited to the specific examples disclosed, or the construction and operation shown and described. Rather, all suitable modifications and equivalents are within the scope of the present invention, as defined in the appended claims.

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WHAT IS CLAIMED IS:

1. A method for texturing a surface of a semiconductor material, comprising:

providing an etching gas in an area around the surface of the material;

irradiating a portion of the surface with short laser pulses; and

translating at least one of the surface and a laser beam to allow the short laser pulses to irradiate another portion of the surface;

wherein the method produces a periodic array of pillars on the surface, resulting in changes in properties of the surface.

2. The method of claim 1, wherein the method additionally produces nanospikes atop the pillars.

3. The method of claim 2, further comprising sharpening the nanospikes by at least one of chemical etching and ion etching after irradiating the surface.

4. The method of claim 1, wherein the laser pulses have a duration of between one femtosecond and one microsecond.

5. The method of claim 4, wherein the laser pulses have a duration of between one femtosecond and hundreds of picoseconds.

6. The method of claim 1, wherein the laser pulses have a laser pulse energy density of between 0.1 J/cm^2 and 1.4 J/cm^2.

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7. The method of claim 1, wherein the laser pulses have a wavelength of between 200 and 1600 nm.

8. The method of claim 1, wherein irradiating the surface further comprises scanning the surface in a plurality of directions.

9. The method of claim 1, wherein irradiating the surface further comprises scanning the surface in a single direction a plurality of times.

10. The method of claim 1, further comprising controlling a surface texture by controlling a polarization state of the laser pulses.

11. The method of claim 1, further comprising controlling an electrical conductivity of the material by controlling texturing parameters.

12. The method of claim 1, wherein irradiating the surface comprises at least partially crystallizing the irradiated surface.

13. The method of claim 1, further comprising controlling a spacing between adjacent pillars by controlling a wavelength of the laser pulses, a laser pulse energy density, and a number of laser pulses.

14. The method of claim 1, wherein the etching gas comprises at least one of sulfur hexafluoride gas, hydrogen chloride gas, helium gas, and argon gas.

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15. The method of claim 1, wherein the etching gas has a pressure of no more than 0.1 atmospheres.

16. The method of claim 1, wherein the etching gas comprises a gaseous plasma.

17. A method for texturing a surface of a semiconductor material, comprising:

providing an etching gas in an area around the surface of the material;

irradiating a portion of the surface with short laser pulses while simultaneously crystallizing the portion of the surface; and

translating at least one of the surface and a laser beam to allow the short laser pulses to irradiate another portion of the surface while simultaneously crystallizing the other portion of the surface;

wherein the method produces pillars on the surface, resulting in changes in properties of the surface.

18. A method for texturing a metallic surface, comprising:

irradiating a portion of the metallic surface with short laser pulses; and

translating at least one of the surface and a laser beam to allow the short laser pulses to irradiate another portion of the surface;

wherein the method produces pillars on the surface, resulting in changes in properties of the surface.

19. The method of claim 18, wherein the pillars are produced in a periodic array.

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20. The method of claim 18, further comprising providing an etching gas in an area around the surface.

21. The method of claim 20, wherein the etching gas comprises at least one of sulfur hexafluoride gas, hydrogen chloride gas, helium gas, and argon gas.

22. The method of claim 20, wherein the etching gas has a pressure of no more than 0.1 atmospheres.

23. The method of claim 20, wherein the etching gas comprises a gaseous plasma.

24. The method of claim 18, wherein the surface is in air at atmospheric pressure.

25. The method of claim 18, wherein the laser pulses have a duration of between one femtosecond and one microsecond.

26. The method of claim 25, wherein the laser pulses have a duration of between one femtosecond and hundreds of picoseconds.

27. The method of claim 18, wherein the laser pulses have a laser pulse energy density of between 0.1 J/cm^2 and 1.4 J/cm^2.

28. The method of claim 18, wherein the laser pulses have a wavelength of between 200 and 1600 nm.

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29. The method of claim 18, wherein irradiating the surface further comprises scanning the surface in a plurality of directions.

30. The method of claim 18, further comprising controlling a surface texture by controlling a polarization state of the laser pulses.

31. The method of claim 18, further comprising controlling an electrical conductivity of the material by controlling texturing parameters.

32. A semiconductor surface, comprising a portion on which pillars are formed with nanospikes atop the pillars by irradiating the surface with short laser pulses while a substantially pure sulfur hexafluoride gas is provided around the surface.

33. A metallic surface, comprising a portion on which pillars are formed by irradiating the surface with short laser pulses.

34. A method of using the textured surface of claim 1 to provide a photovoltaic device.

35. A method of using the textured surface of claim 1 to provide a photodetector.

36. A method of using the textured surface of claim 1 or 18 to provide a high-efficiency heat sink for an electronic device.

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37. A method of using the textured surface of claim 1 or 18 to provide a very high electric field for electron emission.

38. A method of using the textured surface of claim 1 or 18 to generate catalytic activity.

39. A method of using the textured surface of claim 1 or 18 to perform osteointegration of a body implant.

40. A method of using the textured surface of claim 1 or 18 to control the flow of air or fluid over the surface.

41. A method of using the textured surface of claim 1 or 18 to create a two-dimensional array of micro or nano dimensioned ordered tips.

42. A method of using the textured surface of claim 1 or 18 to manufacture an optical beam block which absorbs substantially all light from the visible to the far-infrared.

43. A method of using the textured surface of claim 1 or 18 in micro fluidic applications.

44. The method of claim 1 or 18, further comprising controlling a color of the surface.

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45. A method of using the textured surface of claim 1 or 18 to produce a master for replication.

46. The method of claim 1 or 18, further comprising processing the surface with chemical etching to provide nano or micro pores on the surface.

47. The method of claim 1 or 18, further comprising controlling an emissivity of the surface.

48. The method of claim 1 or 18, further comprising writing text or images on the surface by controlling a light reflectivity.

49. A method of using the textured surface of claim 1 or 18 to provide a radiation shield which operates in a broad spectral range.

50. A method of using the textured surface of claim 1 or 18 to provide an infrared sensor.

51. A method of using the textured surface of claim 18 to prevent corrosion and provide adhesion.

52. The method of claim 1, wherein the changed properties are at least one of optical properties, thermal properties, and electrical properties.

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53. The method of claim 18, wherein the changed properties are at least one of optical properties, thermal properties, and electrical properties.

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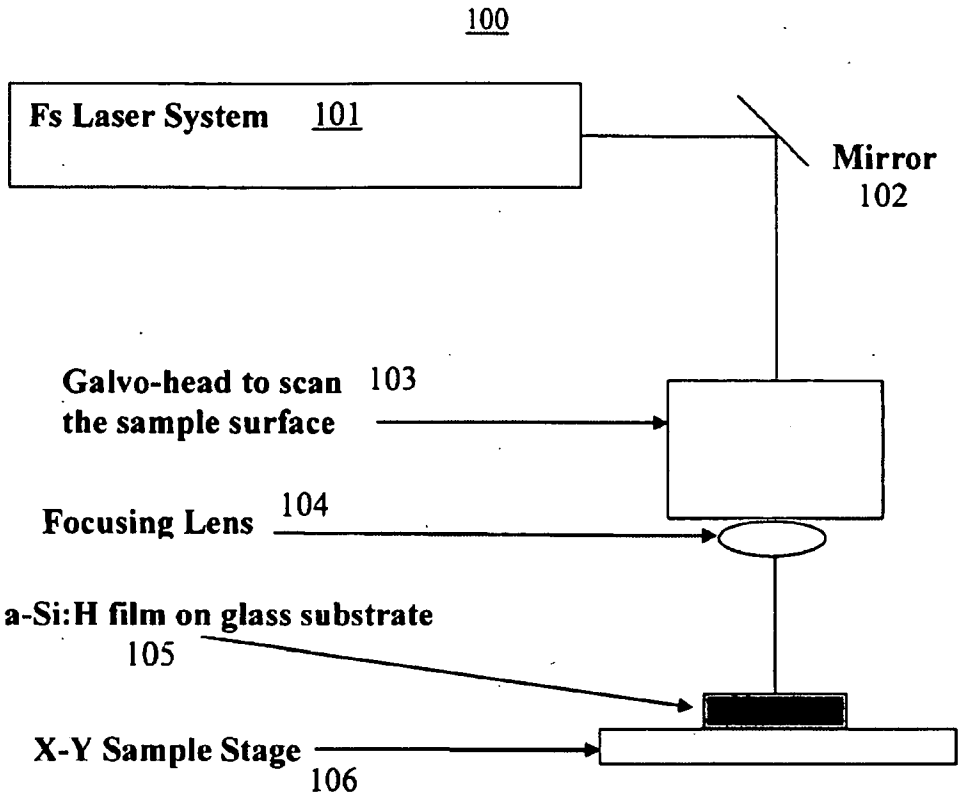


FIG. 1

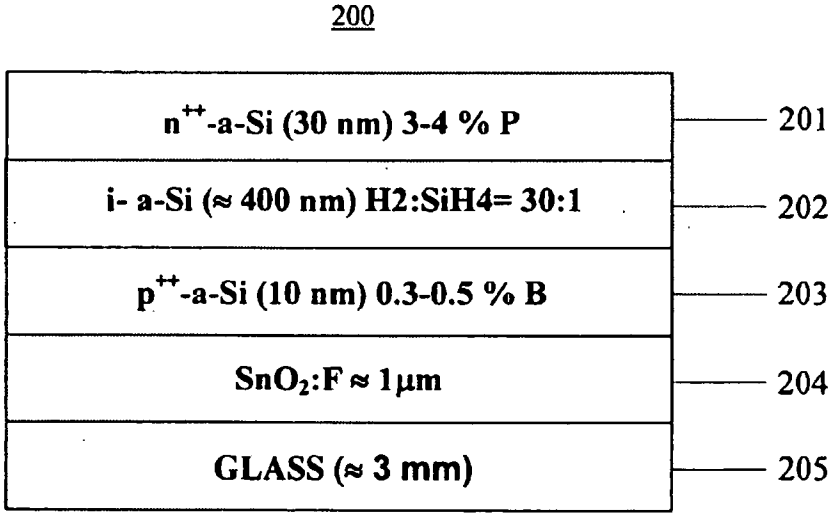


FIG. 2

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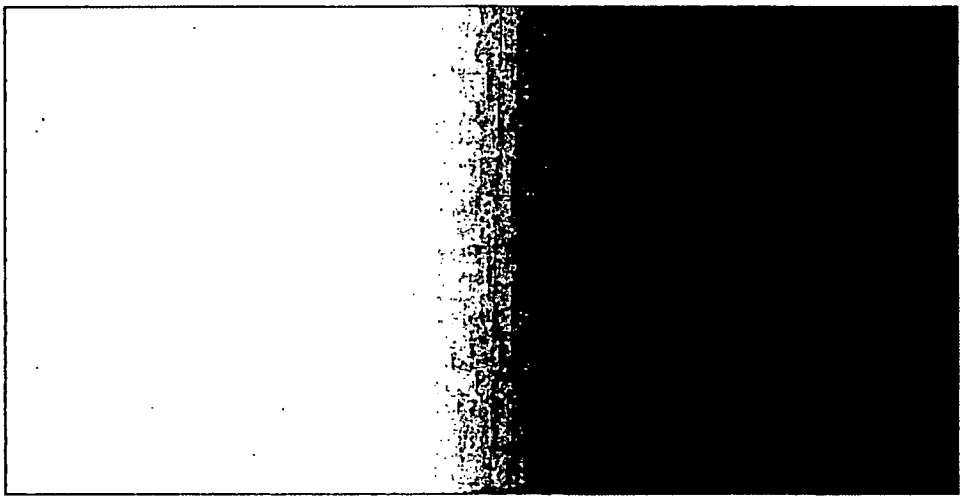
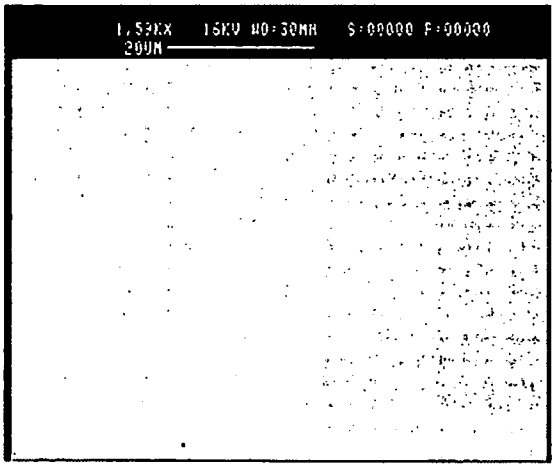


FIG. 3(a) FIG. 3(b)



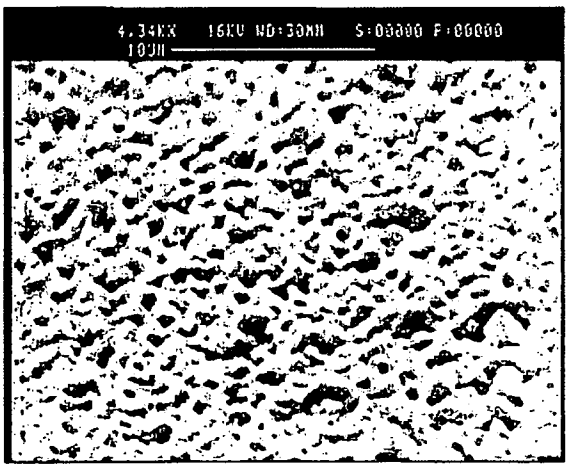


FIG. 4(a) FIG. 4(b)

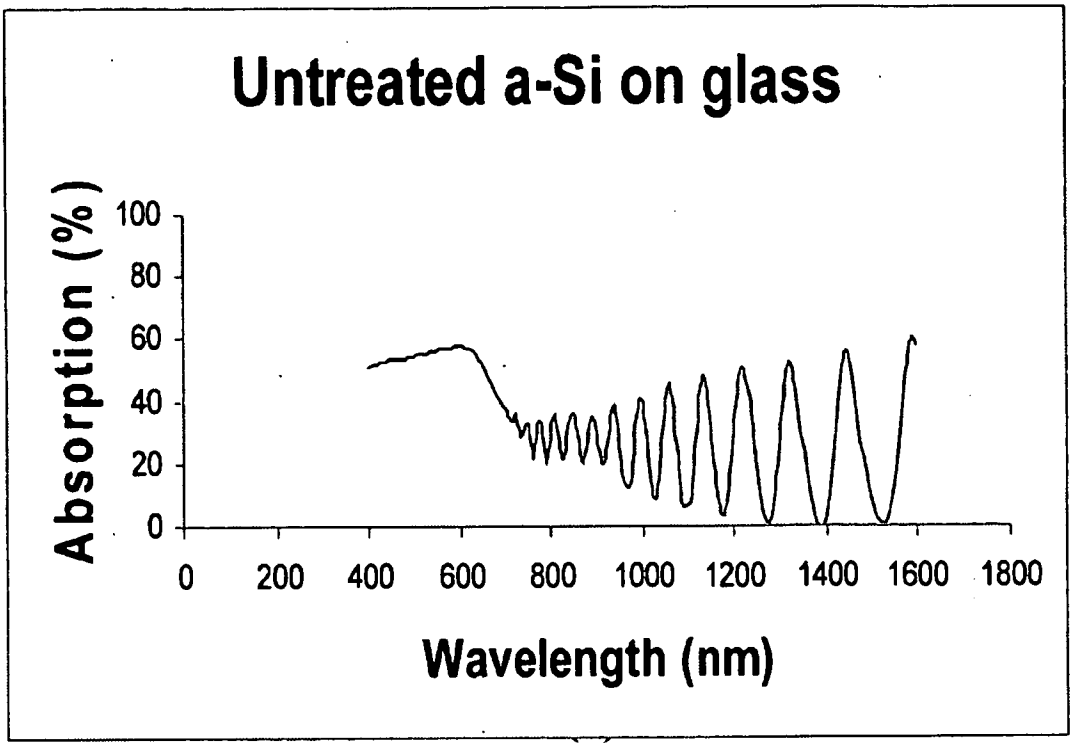

Untreated a-Si on glass
Absorption (%)
100
80
60
40
20
0
0
200
400
600
800
1000
1200
1400
1600
1800
Wavelength (nm)

FIG. 5(a)

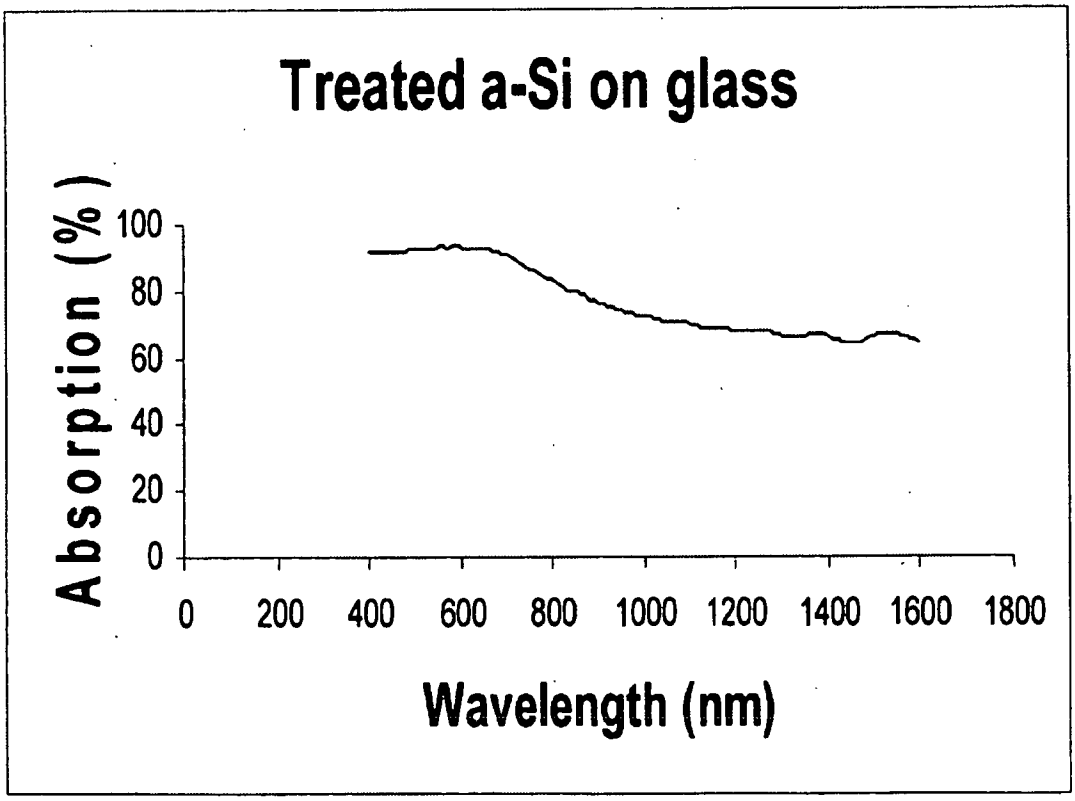

Treated a-Si on glass
Absorption (%)
100
80
60
40
20
0
0
200
400
600
800
1000
1200
1400
1600
1800
Wavelength (nm)

FIG. 5(b)

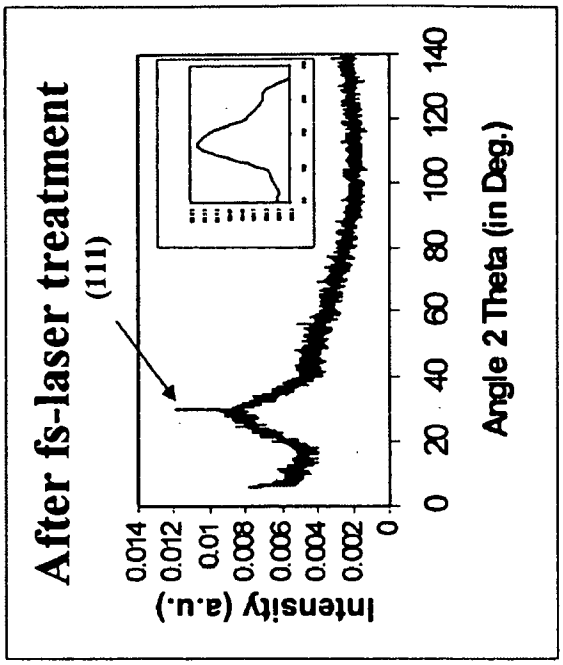


FIG. 6(b)

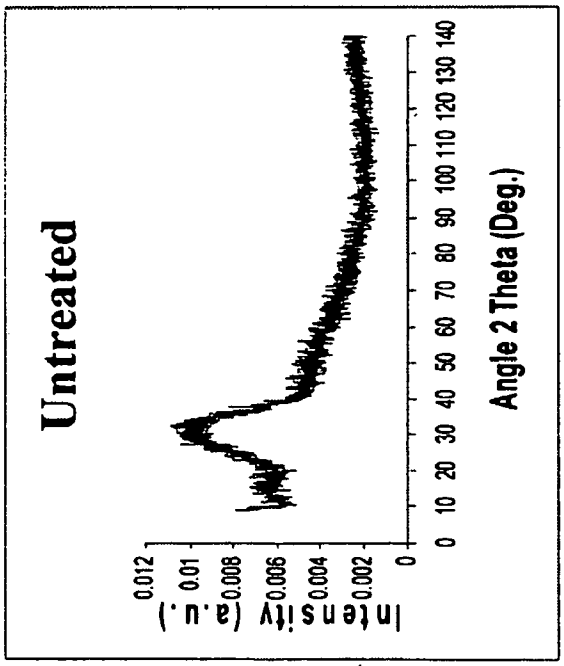


FIG. 6(a)

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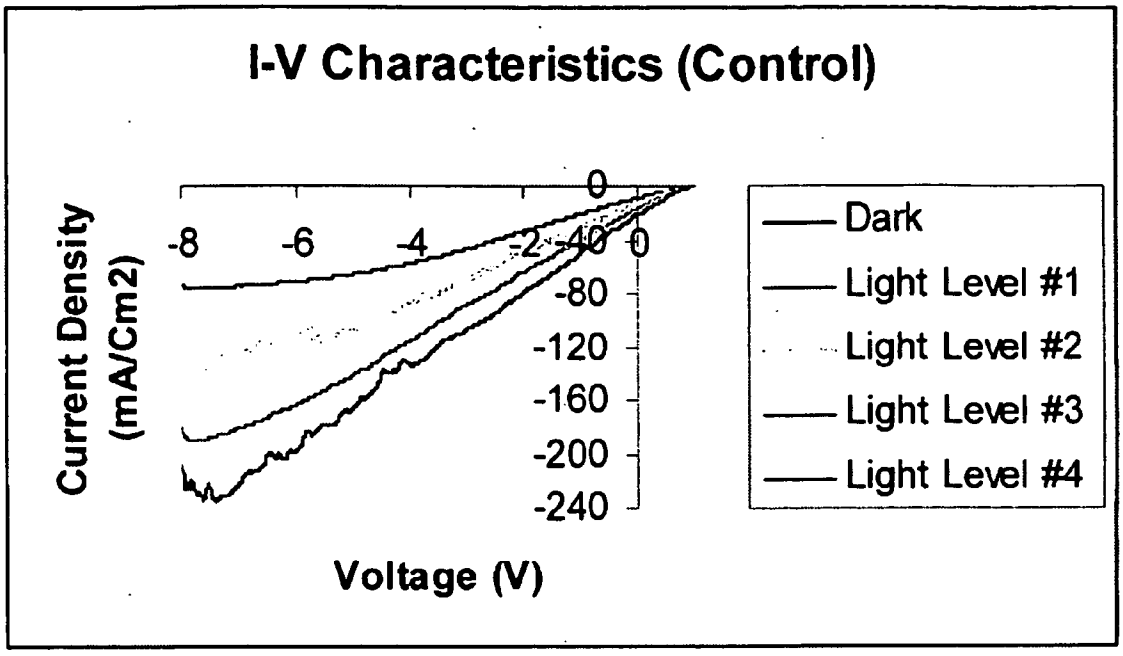

I-V Characteristics (Control)
Current Density (mA/Cm2)
0
-8
-6
-4
-2
-40
0
-80
-120
-160
-200
-240
Voltage (V)
Dark
Light Level #1
Light Level #2
Light Level #3
Light Level #4

FIG. 7(a)

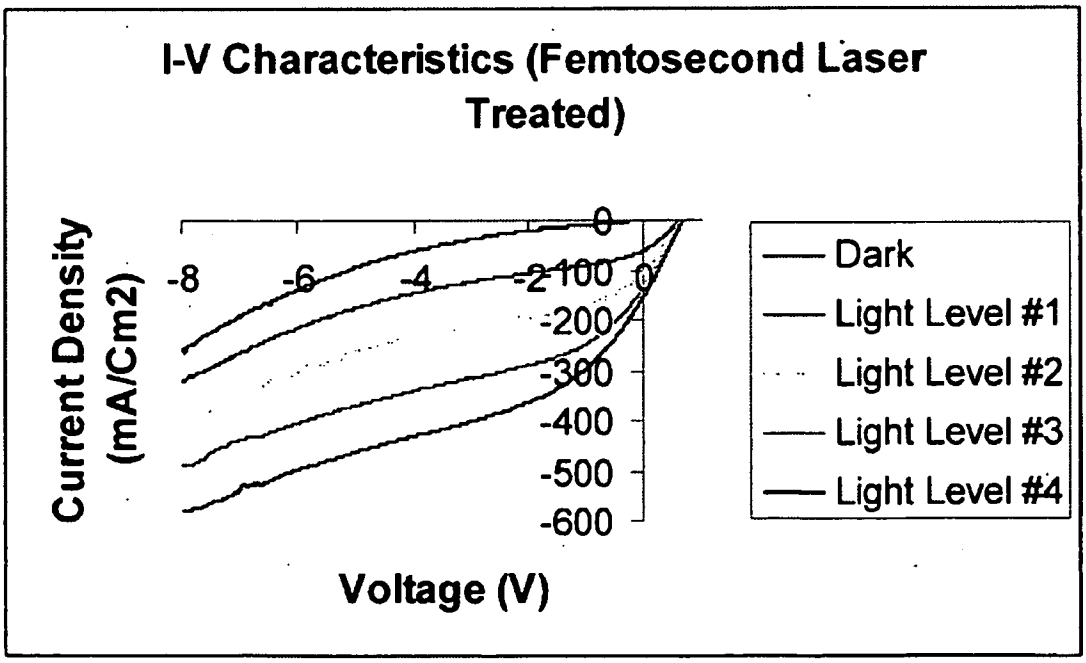

I-V Characteristics (Femtosecond Laser Treated)
Current Density (mA/Cm2)
0
-8
-6
-4
-2
-100
0
-200
-300
-400
-500
-600
Voltage (V)
Dark
Light Level #1
Light Level #2
Light Level #3
Light Level #4

FIG. 7(b)

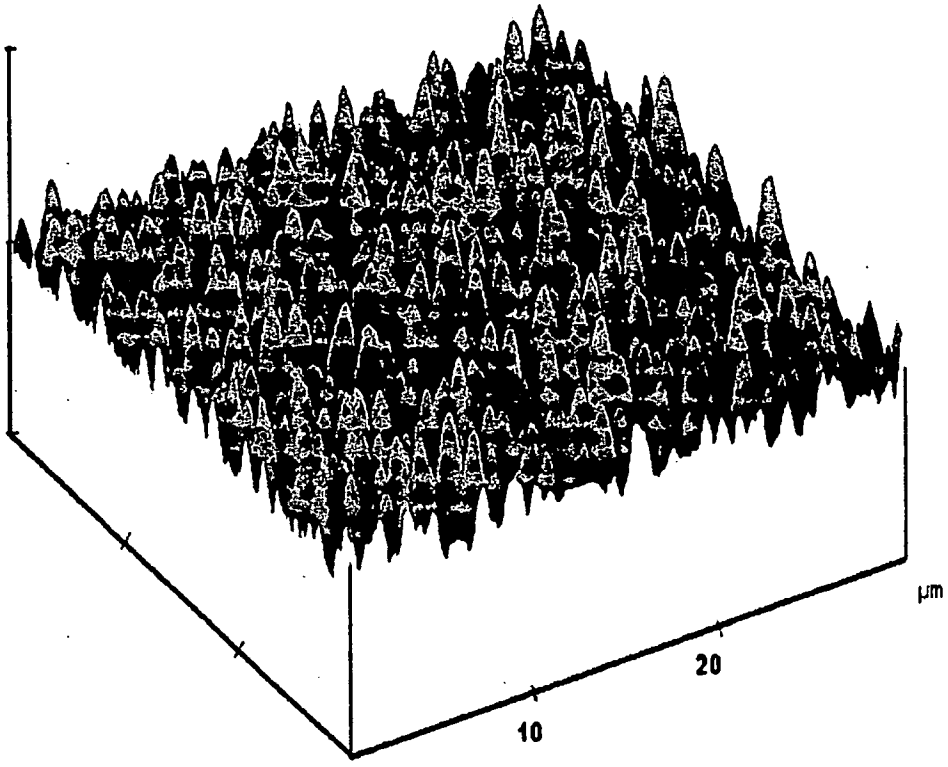

μm
20
10

FIG. 8

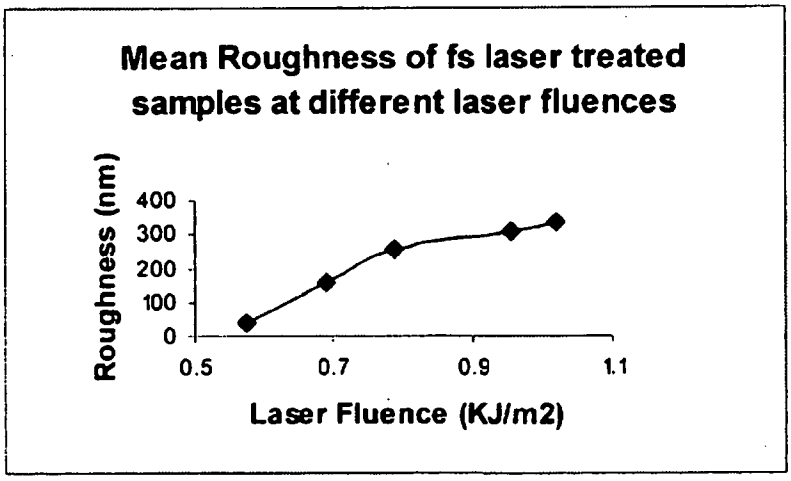

Mean Roughness of fs laser treated samples at different laser fluences
Roughness (nm)
400
300
200
100
0
0.5
0.7
0.9
1.1
Laser Fluence (KJ/m2)

FIG. 9

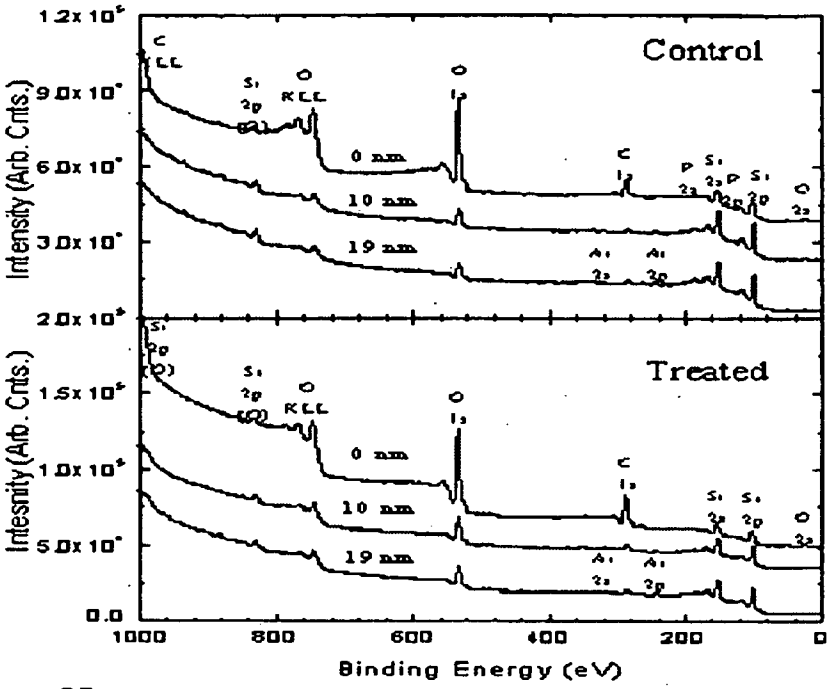


FIG. 10(a)

FIG. 10(b)

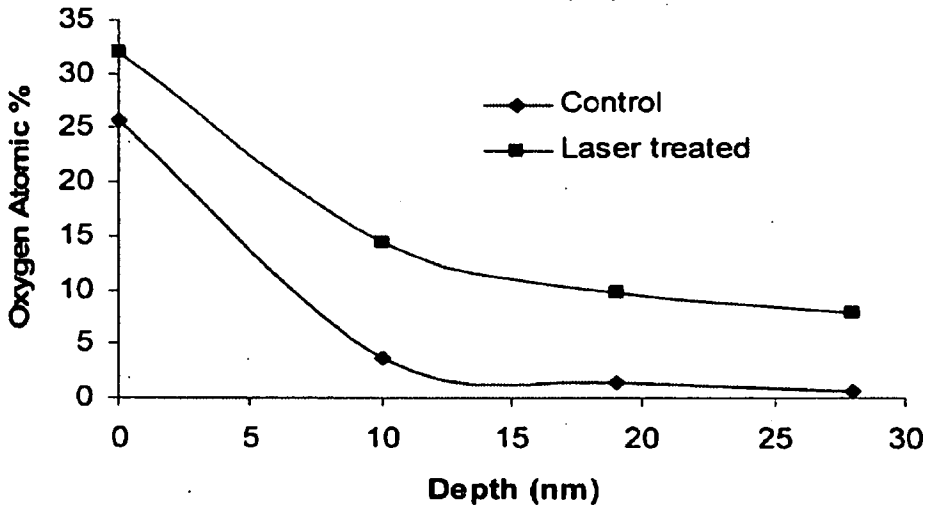


FIG. 10(c)

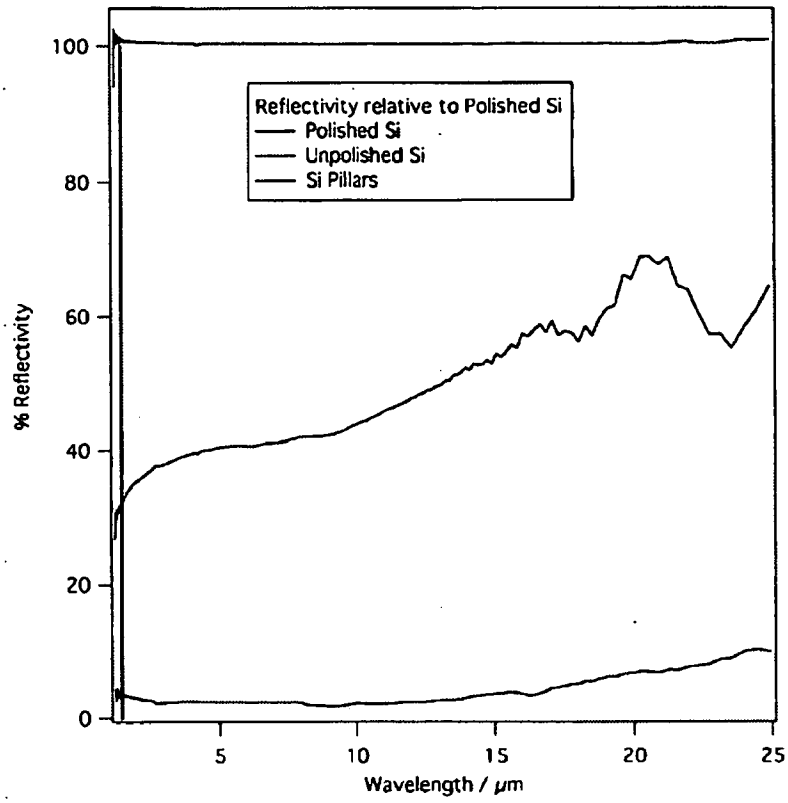


FIG. 11

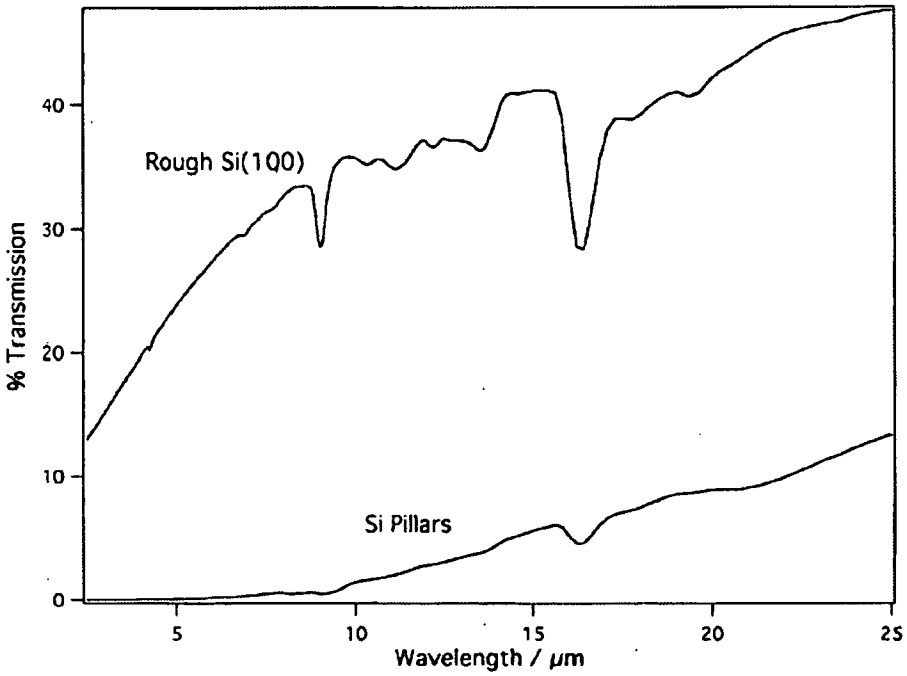


FIG. 12

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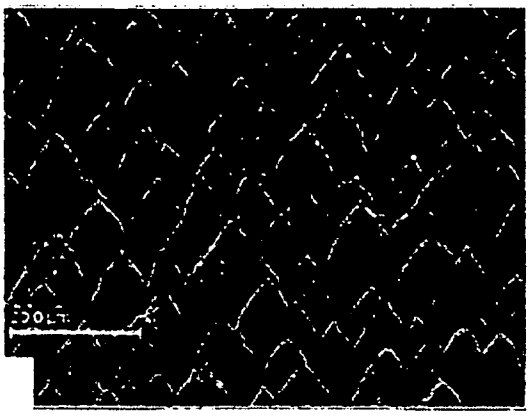


FIG. 13(a)

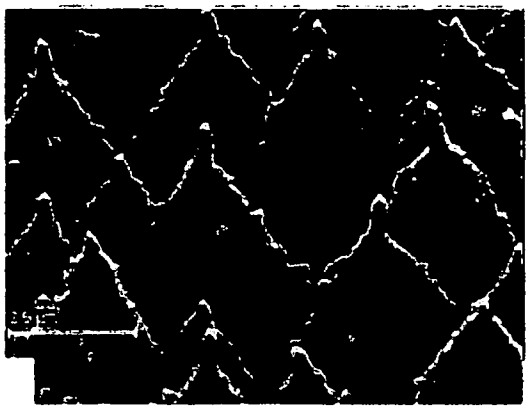


FIG. 13(b)

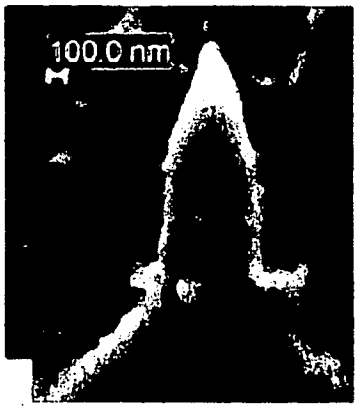


FIG. 13(c)

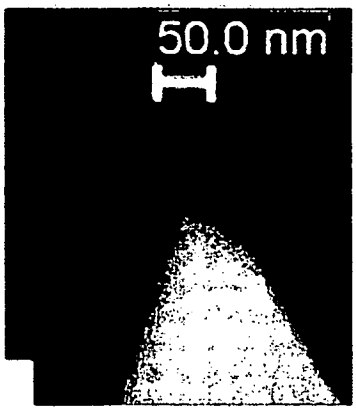


FIG. 13(d)

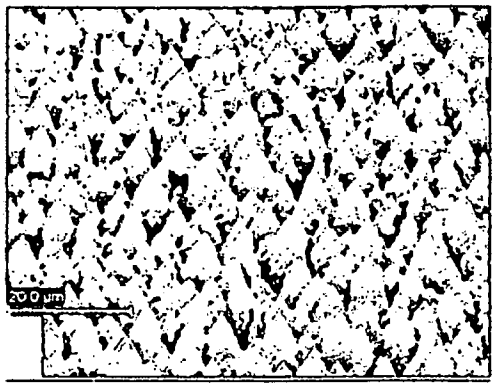


FIG. 14(a)

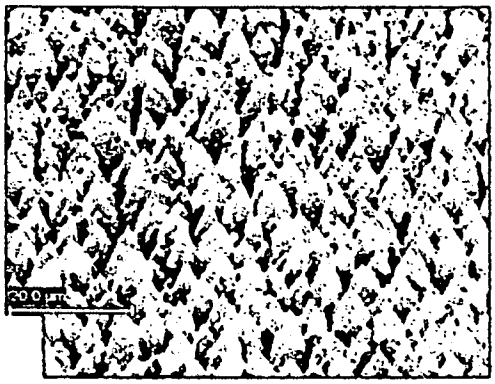


FIG. 14(b)

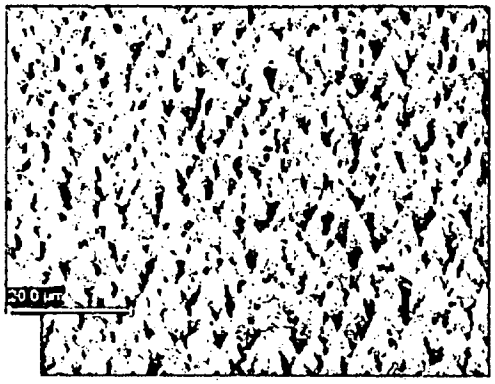


FIG. 14(c)

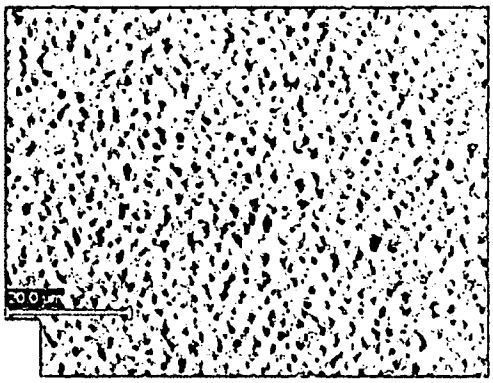


FIG. 14(d)

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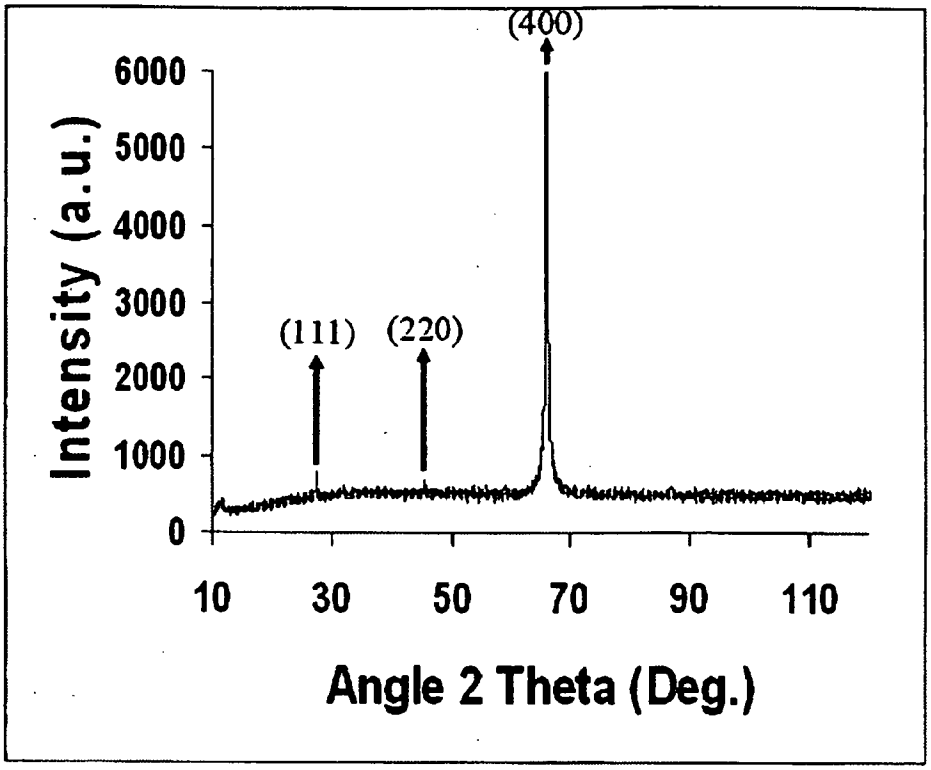


FIG. 15

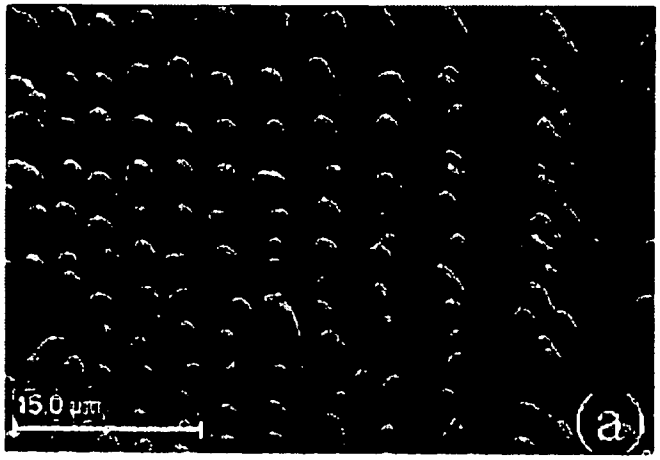


FIG. 19(a)

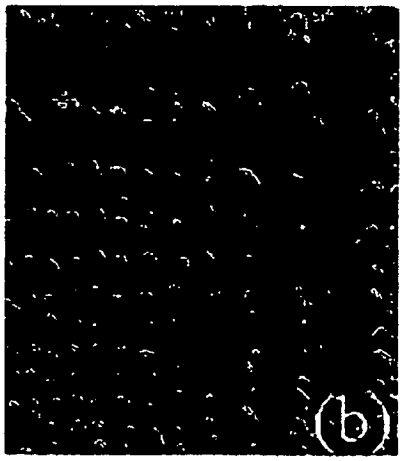


FIG. 19(b)

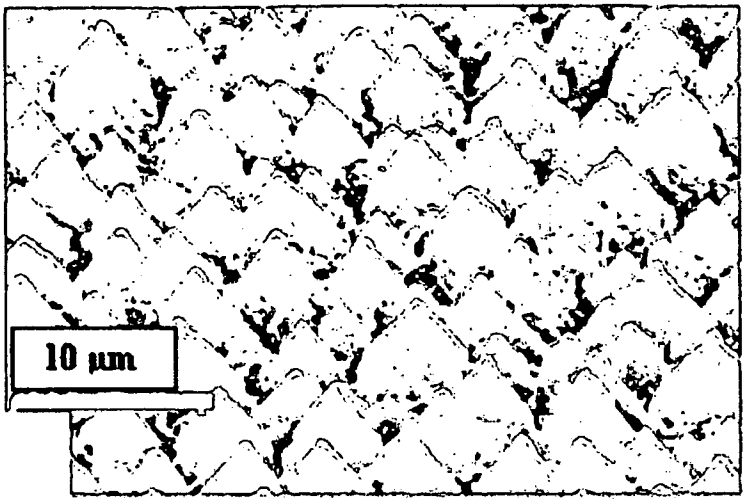


FIG. 16(a)

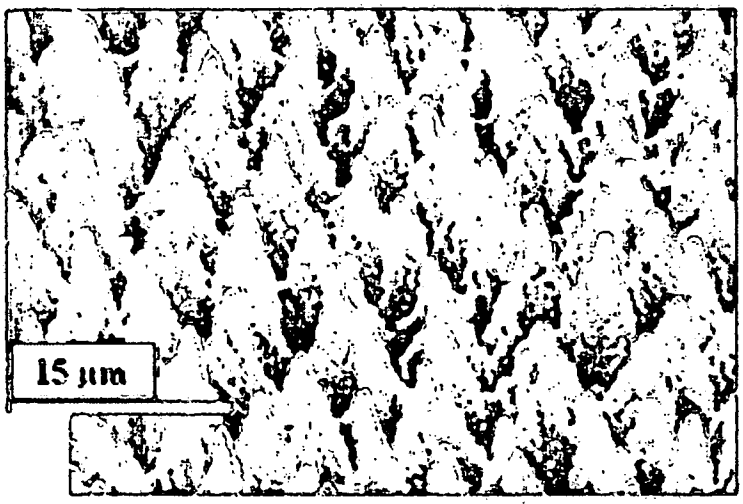


FIG. 16(b)

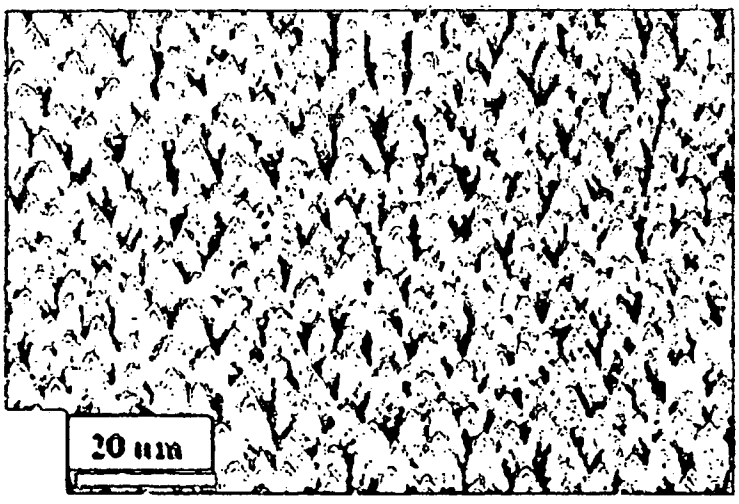


FIG. 16(c)

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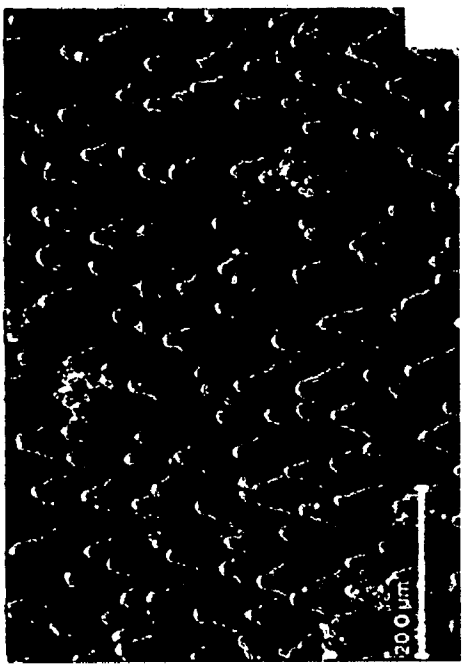


FIG. 17(b)

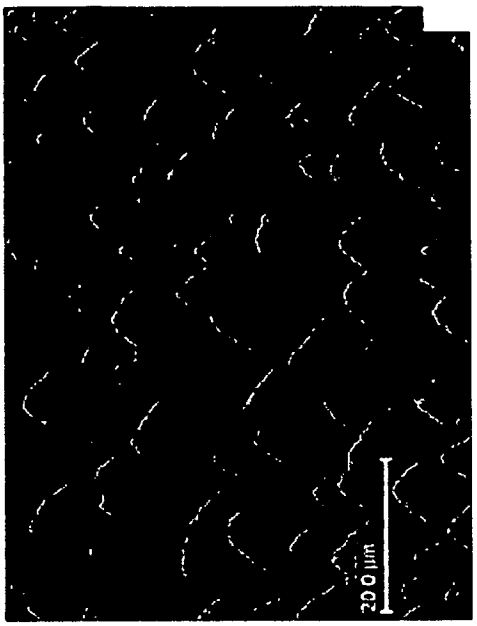


FIG. 18(b)



FIG. 17(a)

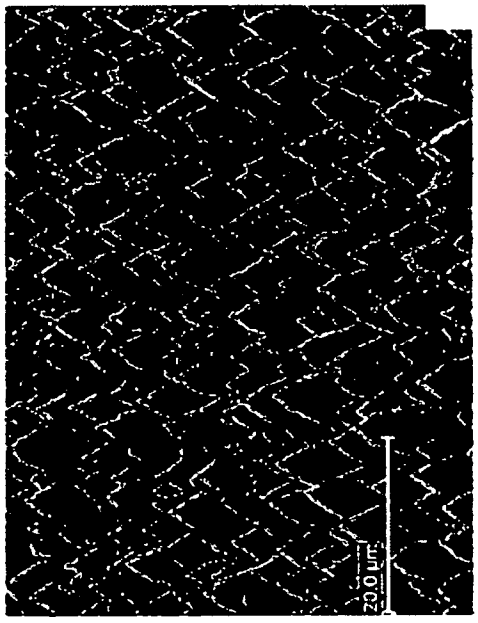


FIG. 18(a)

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FIG. 20(a)

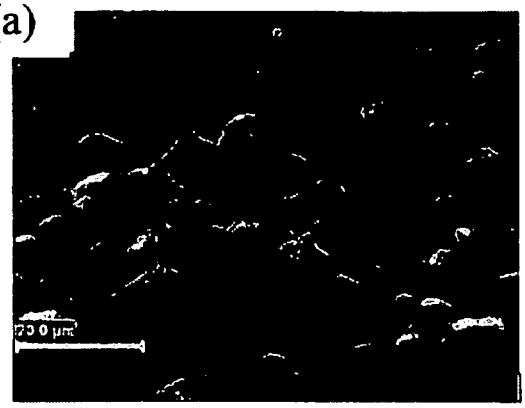


FIG. 20(b)

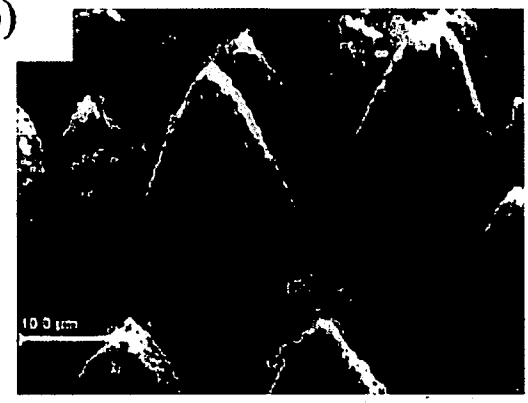


FIG. 20(c)

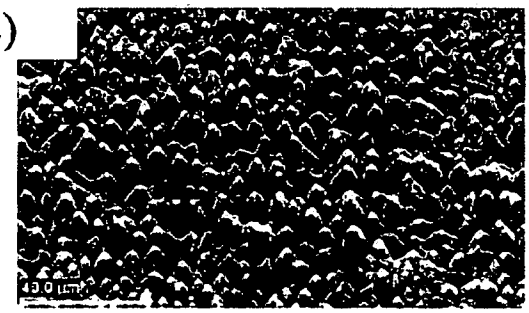
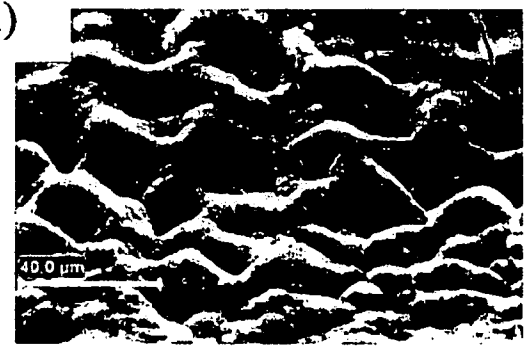


FIG. 20(d)



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FIG. 21(a)



FIG. 21(b)

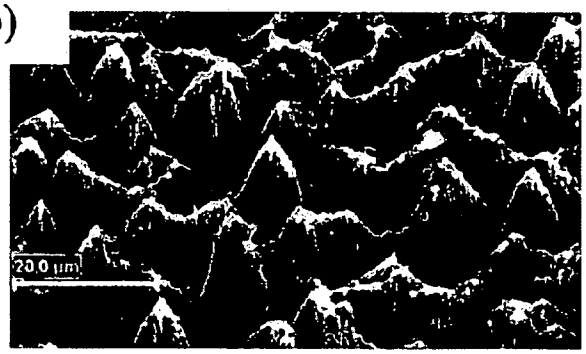
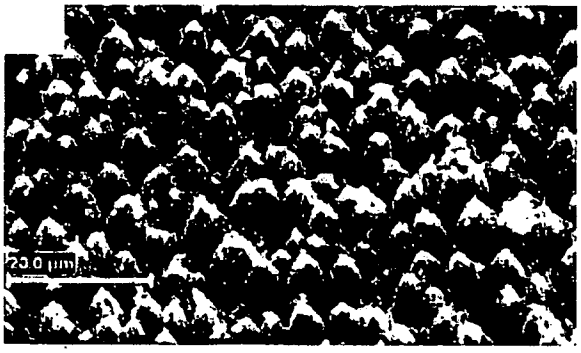


FIG. 21(c)



FIG. 21(d)



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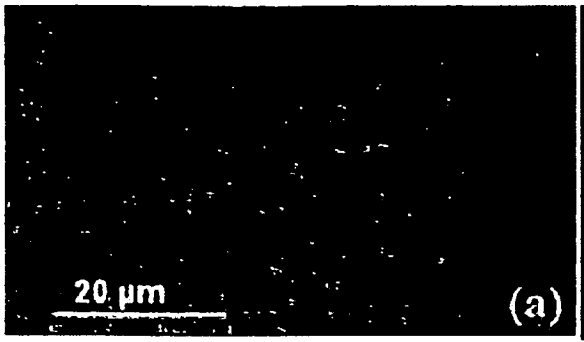


FIG. 22(a)

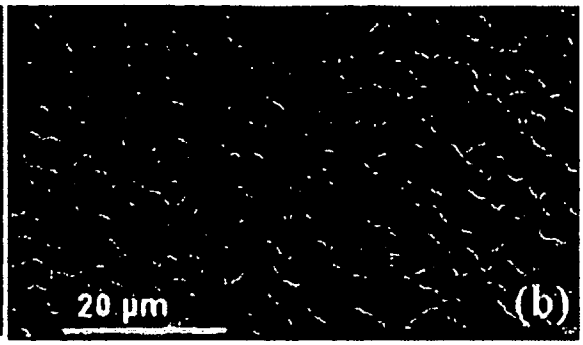


FIG. 22(b)

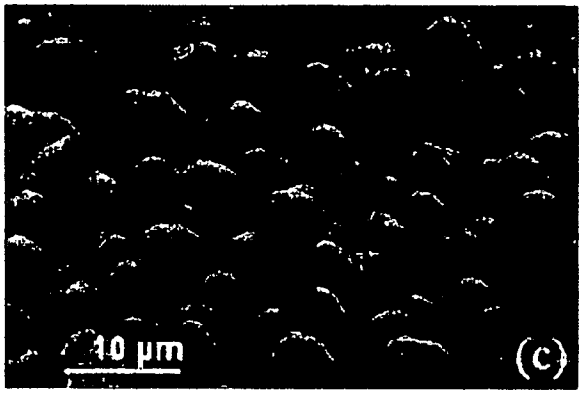


FIG. 22(c)



FIG. 22(d)

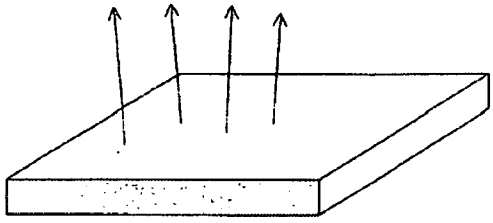


FIG. 23

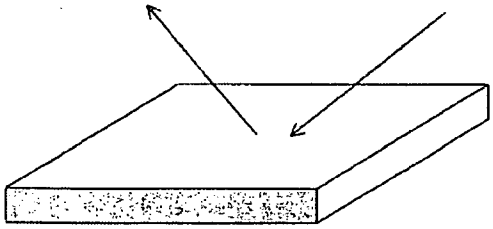


FIG. 24

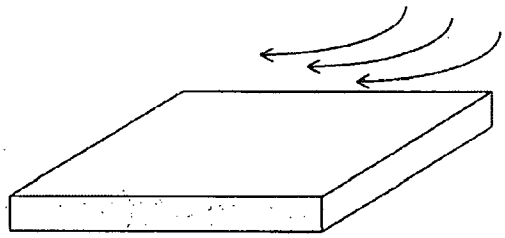


FIG. 25

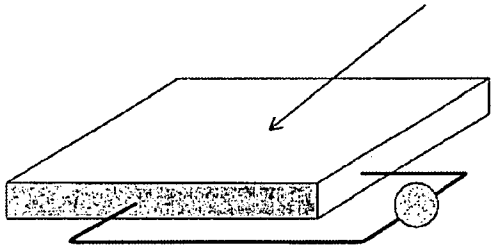


FIG. 26

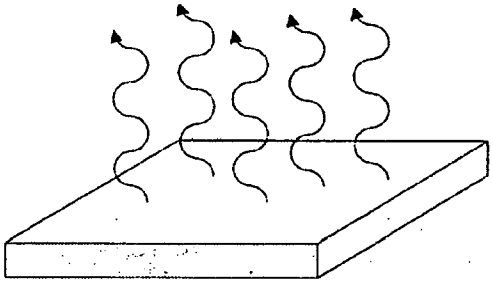


FIG. 27

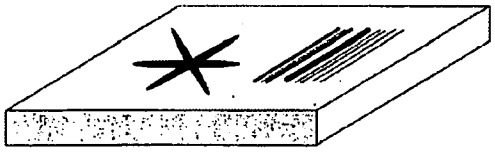


FIG. 28

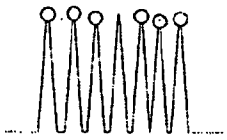


FIG. 29