

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Samsung Electronics Co., Ltd.,
Petitioner,

v.

SiOnyx, LLC,
Patent Owner.

Case No. IPR2025-00162
Patent No. 10,224,359

**DECLARATION OF DR. MICHAEL LEBBY IN SUPPORT OF PETITION
FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,224,359**

Petition A, Based on Primary Reference of Iida

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I. INTRODUCTION

1. I, Michael Lebby, declare as follows.

2. I have been retained as a technical consultant on behalf of Samsung Electronics Co., Ltd. (“Samsung” or “Petitioner”), which I understand to be the petitioner in the present proceeding. I have been asked to consider whether the references listed as Exhibits 1005 and 1007-1009 below disclose or render obvious the limitations recited in claims 1-30, 32, 34, 36, and 38-83 of U.S. Patent No. 10,224,359 (Ex-1001, “’359 patent”). I have also been asked to consider the state of the art and the “prior art,” i.e., references, available before the time of the alleged invention of the ’359 patent. My opinions are provided in this declaration.

3. I am being compensated at my standard consulting rate for my time. My compensation is in no way contingent on the results of these or any other proceedings relating to the ’359 patent.

II. BACKGROUND AND QUALIFICATIONS

4. A description of my professional background and qualifications is provided below. An additional account of my work experience and qualifications is included in my *curriculum vitae*, which is Ex-1004 (“CV”).

5. I am currently the CEO and CTO at GenusTechnik Inc., which provides consulting services in areas that include image sensors, photonics, optoelectronics, semiconductors as used in image sensors and other optical applications.

6. In addition, I am currently the Chairman, CEO, and Director of the Board of Directors for Lightwave Logic. As CEO, I successfully guided Lightwave Logic to up-list to NASDAQ in September 2021 organically (i.e., without the raising of financing), and I led the company to acceptance in the Russell 3000 index in 2022.

7. I have led and run optoelectronics start-ups, and I have commercialized optoelectronic and photonics technologies into volume manufacturing. I have also worked as a Corporate Venture Capitalist specializing in optical communications, photonics, sensing, electronics, and semiconductors, and I am currently a technical expert advising the European Commission regarding evaluation of numerous photonic technology proposals, including image sensor proposals. I am a Fellow Member of the National Academy of Inventors (NAI), the IEEE, and Optica (OSA), and I was voted Photonic Integrated Circuit (PIC) business leader of the year by the PIC International Conference in 2018.

8. In particular, my technical expertise has included the design of components for photonics technology that can source light as well as receive and detect light. These components include LEDs, ICs, lasers, photodetectors, diodes, image sensors, etc. In many of my industrial and commercial roles in the photonics industry I have used, designed, optimized, and improved photonic materials, components, and packages both through solutions of engineering problems as well as patents and publications.

9. Over the course of my career in photonics, optoelectronics, and optical technology in general, I have worked in nearly every aspect of the field, including optical assembly, laser diodes, photodetectors, image sensors, LEDs, integrated circuits (e.g. drivers, and other basic electronic digital and analog functions), as well as fiber optics. In particular, I have designed optoelectronic devices such as LEDs, laser diodes (VCSELs – vertical cavity surface emitting lasers), photodiodes, image sensors, and solar cells with a focus on efficient optical device design that maximizes device performance. For example, I have worked on improving light extraction efficiency in laser diodes as well as LEDs, where these devices are utilized in modules. I have also worked on arrays of detectors for sensing applications.

10. I started my career in 1977 at the Ministry of Defense (United Kingdom), in the Royal Electrical and Mechanical Engineers as a telecommunications apprentice. At the Ministry of Defence, I studied material and characterization issues relating to Gallium Arsenide (GaAs) and Indium Phosphide (InP) optoelectronic devices, as well as semiconductor device design, fabrication, and characterization, particularly with materials using III-V semiconductors. I also worked with silicon for integrated circuits, silicon photonics, and ceramic-based radio-frequency (RF) electronic packaging that included low-temperature co-fired ceramic. These devices and materials were utilized in photonic-based transceiver

packages and modules. I also worked on electronics, motors, sensors, and other technologies that combined photonics with electronics.

11. I attended the University of Bradford, where I obtained a Bachelor's of Engineering (Electrical Engineering), with honors, in 1984, an MBA in 1985 and a Ph.D. (Electrical Engineering) in 1987. My Ph.D. thesis related to the characterization and fabrication of both optoelectronic and electronic semiconductor devices that included the detection of light. In 2004, I was awarded a Doctor of Engineering (a Doctorate degree higher than a Ph.D.) from the University of Bradford for my "Technical Contributions to Optoelectronics." This was only the second time in the University of Bradford's history that a Doctor of Engineering was granted based on industry experience.

12. While attending the University of Bradford and for a few years thereafter, i.e., from 1985 to 1989, I worked as a researcher in the Photonics Research Department of AT&T Bell Labs ("Bell Labs"). At Bell Labs, I focused my research on novel device designs using III-V semiconductor material systems including FETs, bipolar transistors, LEDs, laser diodes, and photodetectors. My research at Bell Labs became the subject of my Ph.D. thesis.

13. After completing my Ph.D. at the University of Bradford and my work at Bell Labs, I became a Research and Development Manager ("R&D Manager") in the photonics division of Motorola's Corporate R&D Labs ("Motorola"). I worked

at Motorola from 1989 to 1998, where my responsibilities included research and development in optical interconnects, electrical and fiber optic connectors, optical/electrical engines, electronic ICs, displays, laser devices, LEDs, optical lenses, image sensors, and optical waveguides, as well as the packaging and reliability of mobile product prototypes. Some of the prototypes on which I worked included moving parts with motors (both standard as well as semiconductor MEMs based), and phased array optical beams that could direct and re-direct optical beams. While at Motorola, I was the inventor or co-inventor on over 150 utility patents, and I received a special award from the Chairman of Motorola in 1998 for exemplary patent accomplishments. At that time, I had the highest number of issued utility patents in the history of Motorola.

14. As an R&D Manager at Motorola, I initiated Motorola's work in optical interconnect technology (known at Motorola as "Optobus"TM) and associated optical connectors, electronics, and photonics components, and I was also involved in research and development on the IC chip designs that this parallel interconnect module utilized. In this project, transparent plastics were developed and molded onto standard metallic lead frames for both light-emitting devices (e.g., LEDs, VCSELs) and photodetectors, which collect light and convert it into an electronic signal. These transparent lead frame packages were developed in volume production at Motorola. I also worked on various techniques to improve both photonics-based detectors such

as photodetectors, image sensors, as well as photonics-based emitters such as lasers and LEDs, both as individual components as well as in arrays of multiple components.

15. In 1998, I left Motorola to join TE Connectivity (previously Tyco Electronics) as Director of Technology and Business Development. In that role, I helped develop technology strategy for optical communications, optoelectronic transceivers, and fiber optic connector and adapter products for the Global Optoelectronics Division. My work included designing and characterizing photodetectors, sensors, LEDs, laser-based photonic packages and modules for product manufacturing.

16. In 1999, I joined Intel Capital (“Intel”) as Director of Business Development and as a corporate investor. My work at Intel included sourcing, negotiating, and closing private placement equity deals in the optical networking, photonic component, interconnect, optical lens, image sensor, and semiconductor industries. My work at Intel also included investigating the investment of Intel Capital equity in photonic devices, optical beams, and other technologies to support the physical movement of optical signals. I also was one of the founders of Intel’s silicon photonics division, which worked to establish a fabrication facility in South San Jose to investigate silicon-based image sensors and the integration of silicon FET electronics with optoelectronics into the same silicon semiconductor wafer.

17. From 2005 to 2010, I served as the Executive Director, President, and CEO of the Optoelectronic Industry Development Association (OIDA) – a trade association that represented photonics manufacturers in the fields of photonic sensing fiber optics, display, defense, aerospace, LED lighting and automotive/motor vehicles. I was responsible for organizing technical conferences, workshops and forecasts using industry roadmaps, all of which featured a portfolio of photonics technology that included: optical sensors, free-space optics, optical interconnects, fiber optics, optical communications, automotive photonic technologies, wavelength division multiplexing, LEDs, displays and their associated packaging.

18. In 2010, I became the General Manager and CTO of Translucent, Inc., a start-up company that developed and manufactured silicon and rare earth oxide-based epitaxial semiconductor wafers.

19. I was employed by Glyndŵr University from 2013 to 2015 as a Professor of Optoelectronics, where I focused on the design, simulation, and testing of high-speed, low-power photonic integrated circuits, optoelectronic integrated circuits, laser diodes, optics, and solar cells for applications that included communications, automotive, displays, sensing, and energy.

20. From 2013 to 2015, I was also employed as the President and CEO of OneChip Photonics Corporation, where I additionally served as an elected

independent board member. In these roles, I focused on technical, business, and operational strategy for fiber optic communications based on InP photonic integrated circuits, as well as optoelectronic integrated circuits for fiber optic transceivers that incorporated electrical and optical multiplexing schemes using fiber optic connectors.

21. Over the course of my career, I have also led panels and given numerous keynote and invited presentations, speeches, and talks at workshops and conferences, including on photonic and optoelectronic materials, devices, components, packages as well as photonics technology in general.

22. Due to my passion for optics, I have been elected to the London Guild of Spectacle Makers. A more detailed description of my education, as well as my training and experience in the relevant technology, is included in my CV.

23. I hold over 340 combined issued USPTO patents and published USPTO patent applications that have been derived from over 230 issued U.S. utility patents, mostly in the field of optoelectronics, photonics, electronics, and semiconductors. I have been cited by the USPTO to be in the most prolific seventy-five inventors in the United States from 1988 to 1997.

24. I have authored approximately 65 publications and have achieved over 400 media events that include: technical articles, books, chapters, invited speaker events at conferences as well as interviews that included TV, video, radio, and social,

industrial, professional media in general. This includes technical, business-related, and financial conferences as a contributing, invited, and keynote speaker. Details can be found in my CV. Over the past decade, I have been a project reviewer and technical expert for the European Commission on numerous occasions.

25. I have also served as an expert witness on numerous patent matters, including 50 IPR proceedings and 5 PGR proceedings. I have also been deposed on more than 60 occasions, including in ITC and District court proceedings.

26. A complete listing of these patents, publications, articles, lectures, and other public media is included with my CV.

27. On the basis of my education and the experience described above, I believe I am qualified to give the opinions set out herein.

III. MATERIALS REVIEWED

28. I am not an attorney and offer no legal opinions. However, in my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art. See Section VI.B below for the level of ordinary skill in the art for this declaration.

29. In preparing this declaration, I reviewed the '359 patent, including the claims of the patent in view of the specification; the prosecution history of the '359 patent; and numerous publications and technical references from and preceding the

time of the alleged invention. More specifically, I have reviewed each of the following:

Exhibit	Description
1001	U.S. Patent No. 10,224,359 (the “’359 patent”)
1002	File History for U.S. Patent No. 10,224,359
1003	Declaration of Dr. Michael Lebby
1004	Curriculum Vitae of Dr. Michael Lebby
1005	U.S. Patent Application Publication No. 2011/0156186 (Iida)
1006	U.S. Patent No. 7,675,099 (Hwang)
1007	International Publication No. WO 2011/035188 (Haddad188)
1008	U.S. Patent Application Publication No. 2012/0033119 (Shinohara)
1009	U.S. Patent Application Publication No. 2009/0266973 (Roy)
1010	P. Saint-Cast et al., “Very low surface recombination velocity on p-type c-Si by high-rate plasma-deposited aluminum oxide,” <i>Appl. Phys. Lett.</i> , 95, 151502 (2009), pp. 1-3, Oct. 14, 2009 (Saint-Cast)
1011	Samsung’s Proposed Constructions, Inv. No. 337-TA-1403 (Aug. 27, 2024)
1012	SiOnyx’s Proposed Constructions, Inv. No. 337-TA-1403 (Aug. 27, 2024)
1013	Email from N. Subhedar re: Claim Construction M&C Follow-Up (Sept. 8, 2024)
1014	Joint Claim Construction Chart, Inv. No. 337-TA-1403 (Nov. 1, 2024)
1015	Simon M. Sze, <i>Physics of Semiconductor Devices</i> (2nd ed. 1981)
1016	Georg Haas & Calvin D. Salzberg, “Optical Properties of Silicon Monoxide in the Wavelength Region from 0.24 to 14.0 Microns,” <i>J. Opt. Soc. Am.</i> , vol. 44, no. 3, pp. 181-87, Mar. 1954 (Haas)
1017	F. López & E. Bernabéu, “Refractive Index of Vacuum-Evaporated SiO Thin Films: Dependence on Substrate Temperature,” <i>Thin Solid Films</i> , 191 (1990), pp. 13-19 (Lopez)
1018	CRC Handbook of Chemistry and Physics (67th ed. 1986)
1019	Quick Reference Manual for Silicon (1985)
1020	A.X. Wei et al., “Electrical and optical properties of tantalum oxide thin films prepared by reactive magnetron sputtering,” <i>J. Alloys Compd.</i> , 509 (2011), pp. 9758-63 (Wei)
1021	Tero Pilvi (2008). <i>Atomic Layer Deposition for optical applications: metal fluoride thin films and novel devices</i> [Academic Dissertation University of Helsinki] ISBN 978-952-92-4814-8, 978-952-10-5133-3, http://ethesis.helsinki.fi .

IV. RELEVANT LEGAL STANDARDS

30. I am not an attorney. For the purposes of this declaration, I have been informed about certain aspects of the law that are relevant to forming my opinions. I have applied the following understanding of the law.

31. I have been informed that a patent claim may be “anticipated” if each element of that claim is present either explicitly or inherently in a single prior art reference, and that the elements should be arranged in the reference as in the claim. Petitioner’s counsel has informed me that for a claimed limitation to be inherently present, the prior art need not expressly disclose the limitation, so long as the claimed limitation necessarily flows from a disclosure in the prior art.

32. I have been informed that a patent claim can be considered to have been obvious to a person of ordinary skill in the art at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a person of ordinary skill in the art at the time the application was filed.

33. I have been informed that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and

- what differences, if any, existed between the claimed invention and the prior art.

34. I have been informed that a single reference can render a patent claim obvious if any differences between that reference and the claims would have been obvious to a person of ordinary skill in the art. Alternatively, the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to one having ordinary skill in the art. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider, among other factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, and when combined, would yield predictable results;
- whether a person of ordinary skill in the art could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by those skilled in the art;
- whether a person of ordinary skill would have recognized a reason to combine known elements in the manner described in the claim;

- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

35. I have been informed that one of ordinary skill in the art has ordinary creativity and is not an automaton. I have been informed that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

36. I understand that various objective or “real world” factors may be indicative of non-obviousness. I understand that such factors include:¹

- the commercial success of the claimed invention;
- the existence of a long-felt, unresolved need for a solution to the problem solved by the claimed invention;
- failed attempts to solve the problem solved by the claimed invention;
- copying of the claimed invention;
- unexpected results of the claimed invention;
- praise for the claimed invention by others in the relevant field; and

¹ I am not aware of any objective evidence of non-obviousness having been identified in connection with the '359 patent.

- willingness of others to accept a license under the patent because of the merits of the claimed invention.

V. TECHNOLOGY BACKGROUND

37. Since the early 2000s, digital cameras and camcorders have become increasingly popular, largely due to the development of advanced image sensors. These sensors play a critical role in converting visual information into electrical signals, which are then processed to create digital images or videos. At the heart of an image sensor lies an array of light-sensitive pixels, each of which is a photodiode capable of detecting light. The photodiode's function is to convert incoming light photons into electrons; the quantity of electrons collected at each pixel determines the pixel's brightness. By assembling this data across all pixels, the sensor constructs a coherent image or video corresponding to the captured scene.

38. In an ideal scenario, an image sensor would achieve perfect efficiency, converting every photon that strikes it into a collected electron. However, in practice, some photons are lost during the conversion process. The efficiency of this conversion is quantified by a metric known as external quantum efficiency, or quantum efficiency for short. Quantum efficiency is defined as the percentage of photons incident on an image sensor that are converted into collected electrons. '359 patent, 4:31-34. Some incident photons may be lost because they are reflected off before reaching the semiconductor layer including a photodiode; others may be lost

because they pass through the semiconductor layer without being absorbed. To mitigate such losses, it is common practice to include in an image sensor microstructures that let more light into the semiconductor layer including a photodiode, as well as microstructures that reflect and scatter light that leaves the semiconductor layer back into the semiconductor layer.

39. Photodiodes are typically fabricated by doping a semiconductor layer to create a junction, which is used for sensing light. A photodiode junction is then connected to a neighboring metallization layer, which carries the electrical signal to external circuits that integrate the signals from all pixels to form a complete image. In the design of image sensors, the side of the semiconductor layer where the photodiode junction and the metallization layer are located is referred to as the “front side,” while the opposite side is known as the “backside.” Image sensors can be designed to receive light from either the front side (front side illuminated, or FSI) or the backside (backside illuminated, or BSI), each offering different advantages and trade-offs.

40. Front side illuminated sensors are easier and less costly to manufacture, but they suffer from greater light loss because the incident light must pass through the metallization layer before reaching the photodiode junction. This can reduce the sensor’s overall efficiency and image quality, especially in low-light conditions. Conversely, backside illuminated sensors are more challenging and expensive to

produce but offer superior performance because the incident light directly reaches the photodiode junction without passing through the metallization layer. This design reduces light loss and improves the sensor's quantum efficiency, leading to better image quality, particularly in demanding lighting environments.

VI. OVERVIEW OF U.S. PATENT NO. 10,224,359

A. Summary

41. The '359 patent relates to image sensor pixels and elements for trapping light within such pixels. '359 patent, 6:16-20. The patent states that a reduction in the size of pixels in an image sensor can sacrifice image quality. '359 patent, 1:24-26. According to the patent, reduced pixel size for image sensors tends to increase electrical and optical crosstalk between adjacent pixels, and image signal-to-noise tends to decrease. '359 patent, 1:26-28. The patent purportedly provides for semiconductor devices with, for example, "enhanced light detection properties." '359 patent, 6:13-16.

42. The patent refers to "light trapping elements" that can "isolate neighboring pixels in an image sensor." '359 patent, 6:18-20. The isolation elements can be configured "to optically and/or electrically isolate neighboring pixels from one another in addition to trapping light within the pixel." '359 patent, 6:20-22. The patent also refers to isolation elements as "trench isolation features" or "sidewalls." '359 patent, 7:42-43.

43. The patent broadly asserts that a “variety of reflective materials can be utilized in constructing the isolation features in order to provide optical isolation, light trapping, and/or electrical isolation,” and that “any such material capable of incorporation into a photosensitive device” is within the patent’s scope. ’359 patent, 7:64-8:1. Examples of such materials include a Bragg reflector or a metal reflector, including for example “silver, aluminum, gold, platinum, reflective metal nitrides, reflective metal oxides, and the like.” ’359 patent, 8:1-9. The isolation elements can be doped to affect properties of the material with respect to electrical isolation. ’359 patent, 8:13-16.

44. According to the patent, a light sensitive pixel can have “a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery.” ’359 patent, 1:43-48. Furthermore, the pixel can include “a backside light trapping material substantially covering the backside surface and a peripheral light trapping material substantially covering the peripheral sidewall.” ’359 patent, 1:48-51. Light that contacts the peripheral light trapping material or backside light trapping material is “reflected back toward the pixel.” ’359 patent, 1:51-54. The patent states that “light entering the pixel that is not absorbed will interact with and be reflected internally” by backside or peripheral sidewall light trapping materials, for example. ’359 patent, 12:26-31. Light is

“effectively maintained inside the pixel until it is absorbed.” ’359 patent, 12:31-32.

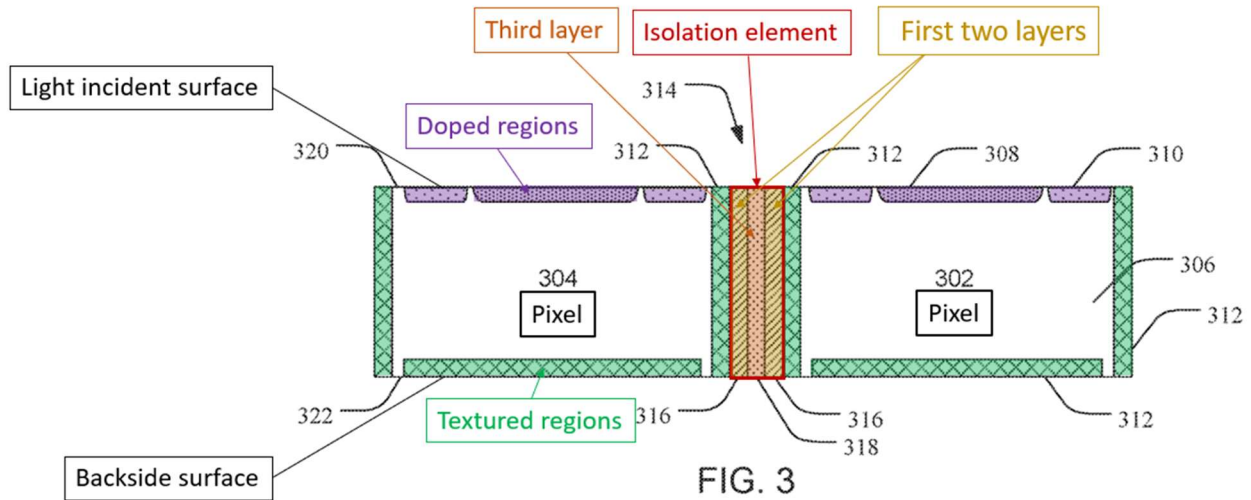
There may also be an “array” of light trapping pixels. ’359 patent, 1:54-55.

45. The isolation element can include at least two layers comprising material having a lower optical refractive index² as compared to the material of a third layer disposed or sandwiched between those two layers. ’359 patent, 8:36-40. In this case, the isolation element functions as a Bragg reflector. ’359 patent, 8:35-36. The patent states that a large index of refraction “mismatch” can result in “total reflection at the trench side walls.” ’359 patent, 9:26-28.

46. The pixel may also include a “textured region.” ’359 patent, 6:45-47. “[A] textured region typically has a textured surface that increases the surface area and increases the probability of radiation absorption.” ’359 patent, 15:27-30.

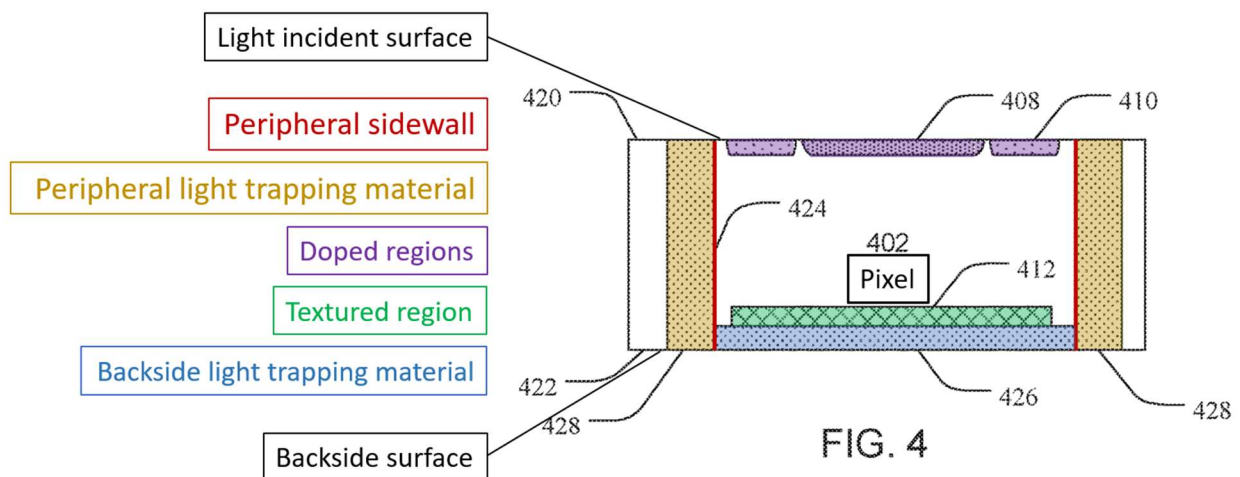
47. Figure 3 is a cross-sectional view of multiple image sensor pixels in accordance with an embodiment discussed in the patent. ’359 patent, 3:37-39. Figure 3 is provided below.

² Herein I use the term “refractive index” to refer to optical refractive index.



'359 patent, Fig. 3 (annotated); *see* '359 patent, 10:63-11:12.

48. Figure 4 is a cross-sectional view of a light trapping pixel discussed in the patent. '359 patent, 3:40-42. Figure 4 corresponds to the “Species 4” elected by the applicant during prosecution. Ex-1002 at 1696. Figure 4 differs from Figure 3 in that it depicts one pixel (rather than two), and in that it depicts “backside light trapping material.” '359 patent, 11:22-24. Figure 4 is provided below.



'359 patent, Fig. 4 (annotated); *see* '359 patent, 11:13-34.

B. Level of Ordinary Skill in the Art

49. It is my understanding that factors defining the level of ordinary skill in the art include: (1) the types of problems encountered in the art; (2) the prior art solutions to those problems; (3) the rapidity with which innovations are made; (4) the sophistication of technology; and (5) the educational level of active workers in the field.

50. A person of ordinary skill in the art (“POSITA”) as of March 2012 would have had a bachelor’s degree in engineering, physics, or a related or equivalent field, and two or more years of experience researching, developing, designing, and/or evaluating image sensors using photonics. A person with less or different education but more relevant practical experience, or vice versa, may also meet this standard.

51. I met this definition of a POSITA as of March 2012. I applied this definition of a POSITA in forming my opinion in this declaration. I understand that SiOnyx, LLC (“SiOnyx” or “Patent Owner”) asserted the ’359 patent in a related case, *Sensors with Pixels and Products Containing the Same*, Inv. No. 337-TA-1403 (the “Related Case”). I understand that Patent Owner’s expert in the Related Case opined that “[t]he level of ordinary skill for the Asserted Patents should be defined as a person having at least a bachelor’s degree in electrical engineering, materials science, or physics, (or an equivalent technical degree), at least two years of experience in

optoelectronics, and at least three years of work experience in semiconductor manufacturing. Further, a master's degree or Ph.D. in a relevant field may substitute for some work experience or vice versa." I met Patent Owner's definition of a POSITA as of March 2012. My opinions remain the same under Patent Owner's definition.

C. Claim Construction

52. I understand that in this proceeding, the claims should be construed in accordance with their ordinary and customary meaning in light of the specification, as understood by one of ordinary skill in the art. I have therefore applied those plain and ordinary meanings in my analysis.

53. I understand that, in the Related Case, Petitioner and Patent Owner have proposed competing constructions for certain terms of the '359 patent. *See* Ex-1011; Ex-1012; Ex-1013; Ex-1014.

54. For purposes of my opinions, I was asked to apply the parties' proposed constructions where both parties' proposed constructions were available and consistent with the plain and ordinary meaning. Where the parties' constructions may have impacted my analysis, I address each as is relevant below.

VII. CLAIMS ANALYSIS

A. **Ground 1: Claims 1-5, 7-8, 10-11, 18, 23, 25, 38-43, 45-50, 52-64, 67-70, 73-75, and 80-83 Are Anticipated or Rendered Obvious by Iida**

1. **Overview of Iida**

55. I understand that Iida is prior art because it was published on June 30, 2011, before the '359 patent's provisional application filing date of March 22, 2012.

56. Iida was not cited in any information disclosure statement (IDS) and was not discussed during prosecution of the '359 patent.³

57. Like the '359 patent, Iida is directed to light-sensitive pixels in imaging devices. Iida, Abstract (“Certain embodiments provide a solid-state imaging device including: a plurality of pixels provided on a semiconductor substrate, each of the pixels having a semiconductor region that converts incident light from a side of a first face of the semiconductor substrate into signal charges and stores the signal charges ...”). Furthermore, like the '359 patent, Iida is directed to addressing problems with smaller pixel sizes, including a reduction in the signal-to-noise ratio and the occurrence of electrical crosstalk between pixels. Iida, [0004]-[0005], [0010]-[0011]. Iida also refers to reducing optical crosstalk through “a separation

³ The patent that issued from Iida (U.S. Patent No. 8,445,950) was cited on the face of the '359 patent among hundreds of references and was cited in an IDS, but it was not discussed during prosecution.

with a trench in which a material to reflect incident light is buried,” Iida, [0013], like the disclosure in the ’359 patent. *See also* Iida, Abstract (referencing “a pixel separation structure provided between adjacent ones of the pixels in the semiconductor substrate”).

58. An exemplary embodiment from Iida is depicted below.

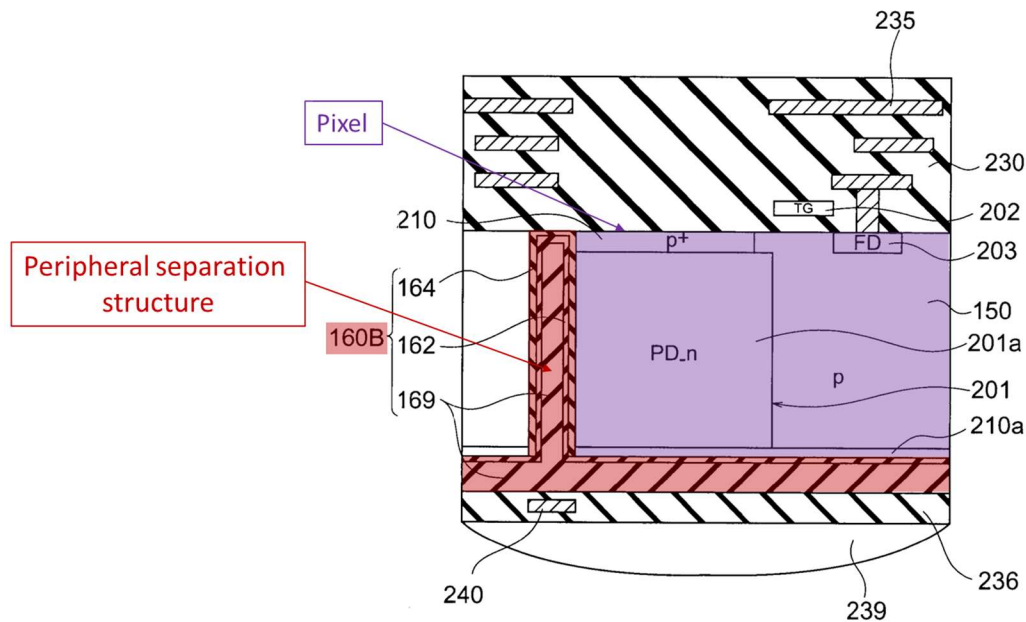


FIG. 10

Iida, Fig. 10.

59. Iida’s Figure 10 is a cross-sectional view of a solid-state imaging device. Iida, [0035]. Among other things, Figure 10 depicts microlens 239 (at the bottom of the figure) and insulating film 236, which transmits incident light. Iida, [0082]. Figure 10 also depicts trench-type pixel separation structure 160B, further comprising silicon oxide layer 164, negative fixed charge film 162 made of hafnium

oxide, and low refractive index film 169. Iida, [0099]. Figure 10 further depicts photodiode 201⁴ near the center of the figure. Iida, [0064]. Also shown are interlayer insulating film 230 and metal interconnect layers 235. Iida, [0082], [0084], [0094].

2. Claim 1

a) Element 1[pre]: “An imager device, comprising:”

60. Iida teaches or suggests this preamble.

61. For example, Iida’s “FIG 10 shows a solid-state imaging device.” as shown below. Iida, [0098].

⁴ While Iida calls element 201 a “photodiode,” POSITAs would understand that photodiode, i.e., the structure that converts light into an electrical signal, encompasses more than just element 201, and would further include the surrounding p-type semiconductor substrate 150. The photodiode comprises a junction created between the differently doped semiconductor regions. *See, e.g.*, Iida, [0049] (“Signal electrons generated through photoelectric conversions in the photodiode 201 having a pn junction formed with the PD_n-region 201a and the p-type semiconductor substrate 150 are stored in the PD_n-region 201a.”).



b) Element 1[a]: “at least two adjacent light sensitive image sensor pixels each having a light incident surface, and a backside surface opposite the light incident surface;”

25

63. Iida's imaging device comprises "a plurality of pixels provided on a semiconductor substrate." Iida, Abstract.⁵ As Iida further explains, a "pixel separation structure ... is provided between adjacent pixels in a silicon substrate 150 in which photodiodes 201 are formed." Iida, [0081].⁶ Thus, the imaging device includes *at least two adjacent light sensitive image sensor pixels* formed in the silicon substrate 150.

64. As annotated below, each pixel has a *light incident surface, and a backside surface opposite the light incident surface*:

⁵ All emphases in quotes have been added, unless otherwise stated.

⁶ Iida [0081] relates to Iida's Figure 9 embodiment. This embodiment "is the same" as Figure 10 "except that" in Figure 10, the "pixel separation structure 160 is replaced with ... pixel separation structure 160B." Iida, [0098]. Otherwise, Iida's disclosures for Figure 9 are equally pertinent to Figure 10. In my discussions of element 1[a] and other claim elements, I focus on the embodiment in Figure 10 but occasionally reference disclosures that describe Figure 9 and are equally applicable to Figure 10.

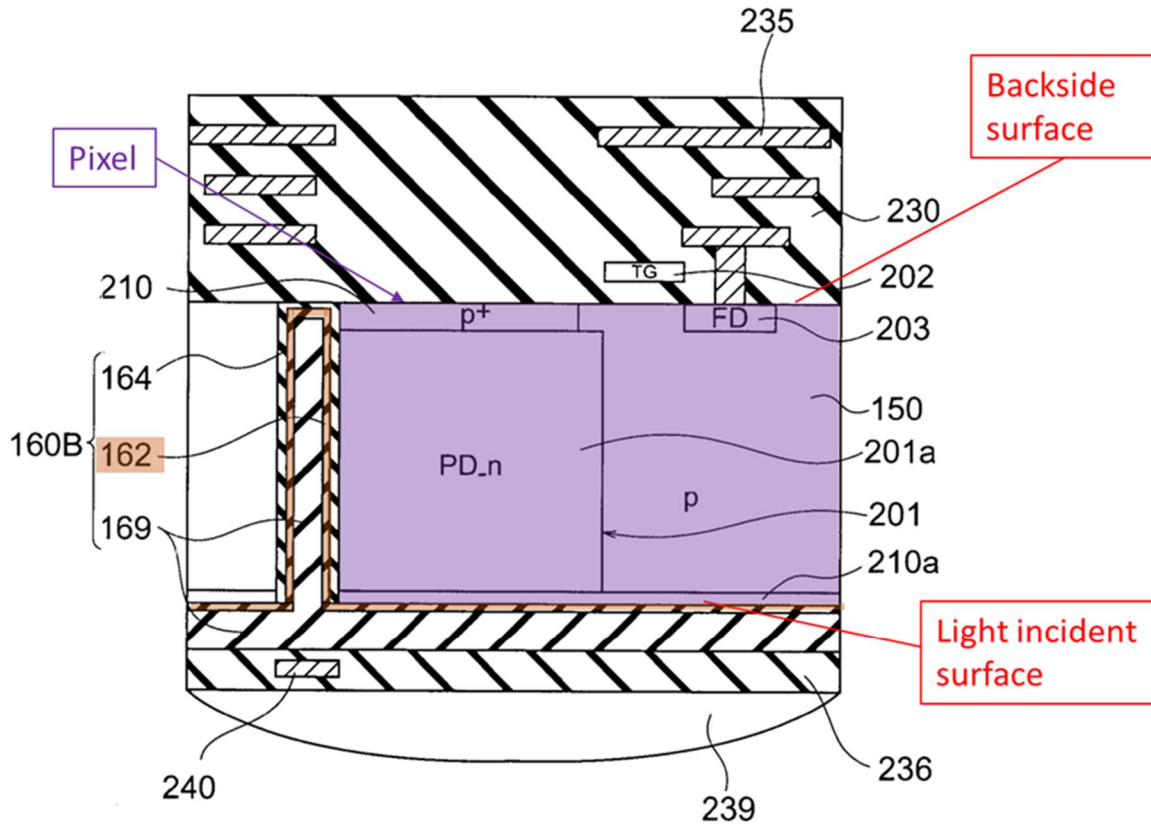


FIG. 10

Iida, Fig. 10 (annotated).

65. Figure 10 depicts a *light incident surface* for the pixels. In Figure 10, the interface between the pixel and the horizontal portion of fixed charge film is a *light incident surface* for the pixel. See Iida, [0080] (“Incident light enters a front-illuminated solid-state imaging device from the front face side. On the other hand, the solid-state imaging device of the third embodiment is of a back-illuminated type”).

66. Figure 10 also depicts a *backside surface opposite the light incident surface*. The interface between the pixel and insulating film 230 is a *backside surface*

opposite the light incident surface. See Iida, [0082] (“an interlayer insulating film 230 is provided on the front face of the silicon substrate 150”).

67. Finally, Iida discloses *adjacent pixels* in connection with the fourth embodiment depicted in Figure 10. Iida, [0101] (“According to this embodiment [depicted in Fig. 10], the effect to reduce optical crosstalk caused by obliquely incident light entering adjacent pixels is improved.”). Thus, Iida teaches *at least two adjacent light sensitive image sensor pixels*, each pixel having a *light incident surface* and a *backside surface opposite the light incident surface*. A POSITA would understand that all the pixels in Iida’s imaging device share the same structure shown in Figure 10. Iida, [0044]-[0045].

c) Element 1[b]: “a peripheral isolation element at least partially separating said two adjacent light sensitive pixels;”

68. Iida teaches or suggests this limitation.

69. Iida’s imaging device includes a “trench-type pixel separation structure 160B,” Iida, [0098], which comprises an *isolation element at least partially separating said two adjacent light sensitive pixels* as shown below in Figure 10. *See also* Iida, [0081] (explaining for Figure 9 that “each trench-type pixel separation structure 160 is provided between adjacent pixels”). Each such separation structure extends along the *peripher[y]* of the light sensitive pixel and isolates that pixel from adjacent light sensitive pixels.

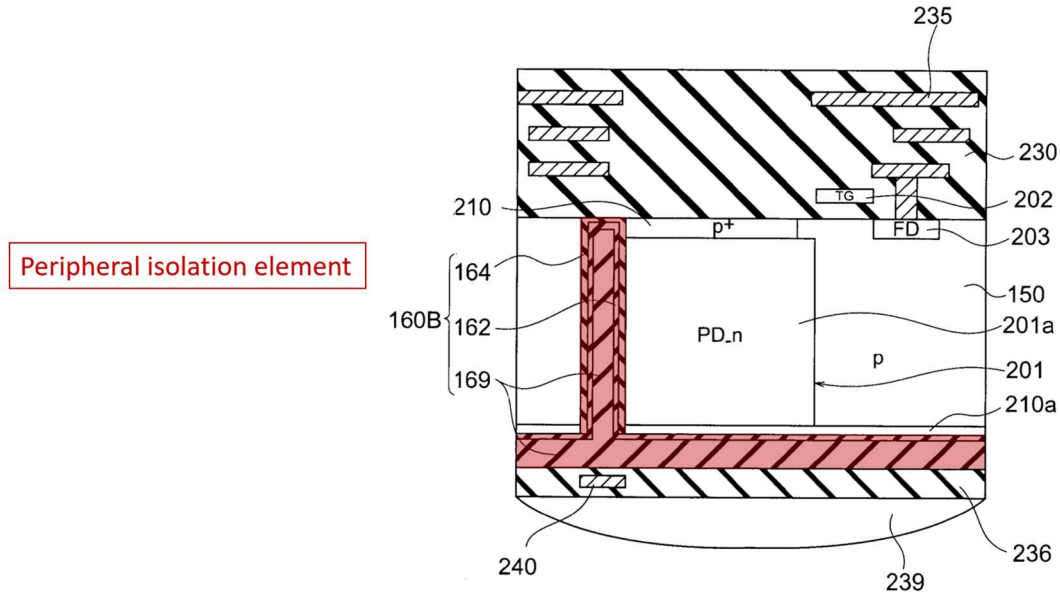


FIG. 10

- d) **Element 1[c]: “each of said pixels having at least one doped region disposed on at least one of the light incident surface and the backside surface,”**

70. Iida teaches or suggests this limitation.

71. The pixels in Iida’s imaging device include *at least one doped region*. Namely, Iida discloses that a “p⁺-type impurity diffused region 210 for preventing dark current from flowing into a PD_n-region 201a is provided in a region on the front face side of the silicon substrate 150 between the PD_n-region 201a and the interlayer insulating film 230.” Iida, [0082]. Iida’s region 210 is a *doped region*. The ’359 patent specifies that p⁺ semiconductor layers can be used, and that the “positive sign” in “p(+)” (as disclosed in Iida) is an “indicator[] of the relative magnitude of the doping of the semiconductor material.” ’359 patent, 17:24-28; *see also* ’359 patent, 17:11-17 (“In some aspects, layers can vary in majority carrier

72. Iida's doped region 210 is "disposed on at least one of the light incident surface and the backside surface" of the pixel. Iida discloses that region 210 is provided "on the front face side" of the substrate. Iida, [0082]. The "front face side" referenced by Iida corresponds to "the backside surface" of claim 1 of the '359 patent because the "front face side" is opposite the light incident surface, as shown in Figure 10.



30

e) Element 1[d]: “wherein the peripheral isolation element comprises at least two materials having different indices of refraction,”

73. Iida teaches or suggests this limitation.

74. With respect to the embodiment depicted in Figure 10, Iida discloses that “pixel separation structure 160B has a structure in which a silicon oxide layer 164, a fixed charge film 162 [made of hafnium oxide], and a film 169 made of a low refractive index material are buried in a trench formed in a silicon substrate.” Iida [0099]. The refractive index of Iida’s silicon oxide layer 164 is 1.4. Iida, [0052]. The refractive index of Iida’s hafnium oxide film 162 is 2.0. Iida, [0052], [0100]. Thus, *Iida teaches the peripheral isolation element comprises at least two materials having different indices of refraction*, as recited in this limitation.

f) Element 1[e]: “wherein said peripheral isolation element comprises a first, a second and a third layer,”

75. Iida teaches or suggests this limitation.

76. As shown below, Iida discloses that the pixel separation structure 160B of the embodiment depicted in Figure 10 (*peripheral isolation element*) comprises a trench in which three layers are buried: (1) a “silicon oxide layer 164” (*first layer*); (2) “a film 169 made of a low refractive index material” (*second layer*); and (3) a negative “fixed charge film 162 made of hafnium oxide” (*third layer*). Iida, [0099].

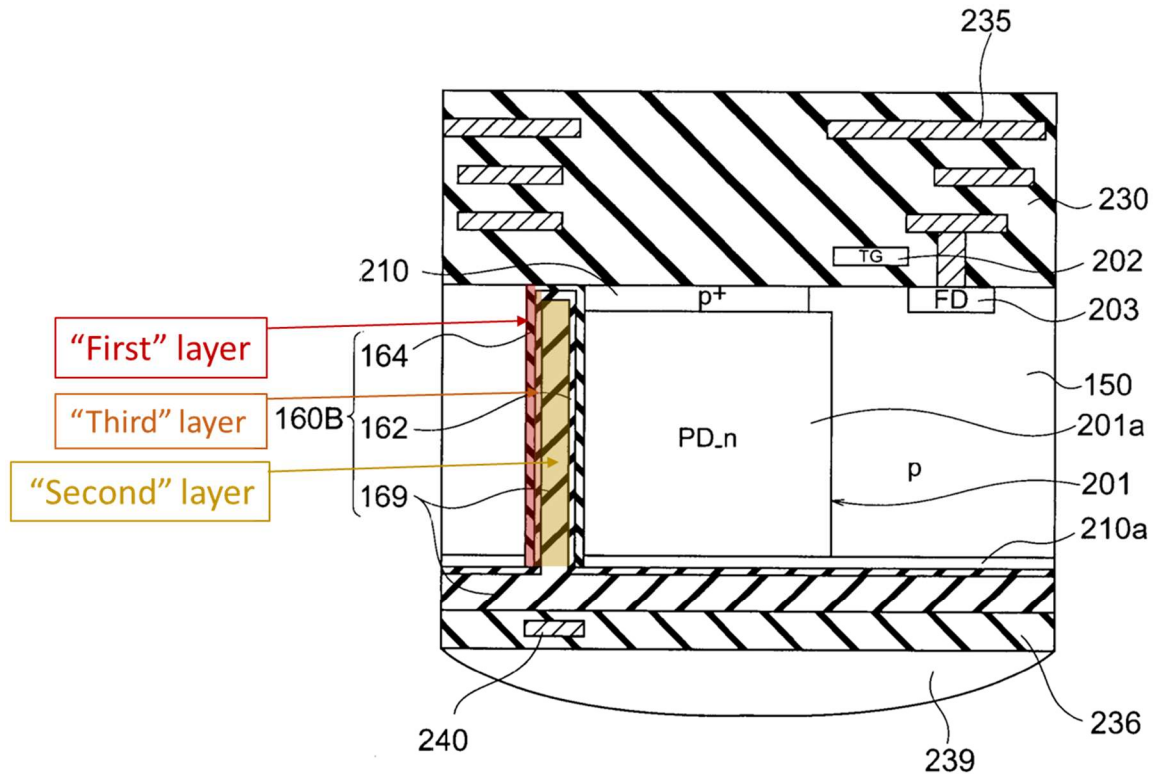


FIG. 10

Iida, Fig. 10 (annotated).

g) Element 1[f]: “wherein said third layer is disposed between said first and second layers, and”

77. Iida teaches or suggests this limitation.

78. As discussed above regarding limitation 1[e], Iida discloses a *third layer*, i.e., hafnium oxide film 162, *disposed between* the *first layer*, i.e., silicon oxide layer 164, and the *second layer*, i.e., low refractive index film 169.

h) Element 1[g]: “wherein each of said first and second layer exhibits an index of refraction less than an index of refraction of said third layer.”

79. Iida teaches or suggests this limitation.

80. The refractive index of Iida's silicon oxide layer 164 (*first layer*) is 1.4. Iida, [0052]. The refractive index of Iida's hafnium oxide film 162 (*third layer*) is 2.0. Iida, [0052], [0100]. The refractive index of Iida's low refractive index material (layer 169) "should preferably be ... lower ... than the refractive index of hafnium oxide, which is 2.0." Iida, [0100]. Thus, the refractive indices of Iida's silicon oxide layer 164 and low refractive index film 169 (*first and second layers*, 1.4 and <2.0) are less than the refractive index of Iida's hafnium oxide layer 162 (*third layer*, 2.0).

3. Claim 2: "The device of claim 1, wherein the index of refraction of at least one of said first and second layer is at least 0.2 lower relative to the refractive index of the third layer."

81. Iida teaches or suggests this limitation.

82. As discussed above regarding limitation 1[g], the refractive index of Iida's silicon oxide layer 164 (*first layer*) is 1.4 and the refractive index of Iida's hafnium oxide film 162 (*third layer*) is 2.0. Iida, [0052], [0100]. Thus, the refractive index of Iida's silicon oxide layer 164 *is at least 0.2 lower* than that of Iida's layer 162.

4. Claim 3: "The device of claim 1, wherein at least one of said at least two materials comprises silicon dioxide."

83. Iida teaches or suggests this limitation.

84. As discussed above regarding limitation 1[e], Iida discloses a "silicon oxide layer 164" corresponding to the *first layer* of the *peripheral isolation element*.

85. A POSITA would understand that, in disclosing silicon oxide layer 164, Iida uses the term “silicon oxide” to mean “silicon dioxide” (SiO_2) as opposed to “silicon monoxide” (SiO). Iida specifically refers to “ SiO_2 ” in describing the “oxide film buried in a trench structure” used to form the “trench separation structure ... applied to pixel separations in a solid-state imaging element.” Iida, [0007]. Moreover, a POSITA would know that the refractive index of silicon dioxide is around 1.4-1.5, whereas the refractive index of silicon monoxide is at least around 1.8-2.2. *See, e.g.*, Ex-1015, Appendix I at 852 (refractive index of SiO_2 is “1.46”); Ex-1016, Abstract (refractive index of “silicon monoxide” (“ SiO ”) ranges from 2.15 to 1.95 in the 0.40 to 0.70 micron wavelength range disclosed by Iida at [0104]); Ex-1017 at 17 & Fig. 2 (refractive index of “silicon monoxide” ranges from about 1.8 to about 1.9 in the 1 to 5 micron wavelength range); Ex-1019 at 2-60 (refractive index of “ SiO_2 ” ranges from about 1.5 to 1.4 in the 0.40 to 0.70 micron wavelength range). Iida specifies that its “silicon oxide layer ha[s] a refractive index of 1.4,” confirming that it is using silicon dioxide. Iida, [0104]. Consistent with such an understanding, the ’359 patent itself uses the term “silicon oxide” to mean “silicon dioxide,” as it alternatively refers to the layers depicted in its Figure 2 as including “silicon dioxide” and “silicon oxide.” ’359 patent, 9:13-18 (“[A] Bragg reflector can be made as in FIG. 2, whereby a high refractive index material sandwiched between two low refractive index materials. In one specific aspect, for example, the Bragg reflector can be constructed

of a layer of polysilicon sandwiched between two layers of silicon dioxide.’); ’359 patent, 10:20-22 (“Returning to FIG. 2, layers [of] the silicon oxide and polysilicon...”).

86. Thus, Iida teaches *silicon dioxide* as a *material* for its *peripheral isolation element*, as recited in this claim.

5. Claim 4: “The device of claim 1, wherein at least one of said first and second layers comprises silicon dioxide.”

87. Iida teaches or suggests this limitation.

88. As discussed above regarding limitation 1[e], Iida discloses a “silicon oxide layer 164” corresponding to the *first layer* of the *peripheral isolation element*.

89. As discussed above regarding claim 3, Iida’s disclosure of silicon oxide layer 164 discloses a *layer of silicon dioxide*.

6. Claim 5: “The device of claim 1, wherein the isolation element extends substantially from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels.”

90. Iida teaches or suggests this limitation.

91. Iida discloses that “pixel separation structure 160 has a trench that penetrates through the silicon substrate 150 from the back face side to the front face side.” Iida, [0081]. As discussed above regarding limitation 1[a], the interface between the pixel and the horizontal portion of negative fixed charge film 162 corresponds to the pixel’s *light incident surface*, and the interface between the pixel

and the interlayer insulating film 230 corresponds to the pixel's *backside surface*.

As shown in Figure 10, pixel separation structure 160B *extends substantially* from the pixel's *light incident surface* (162/210a interface) to the pixel's *backside surface* (150/230 interface).

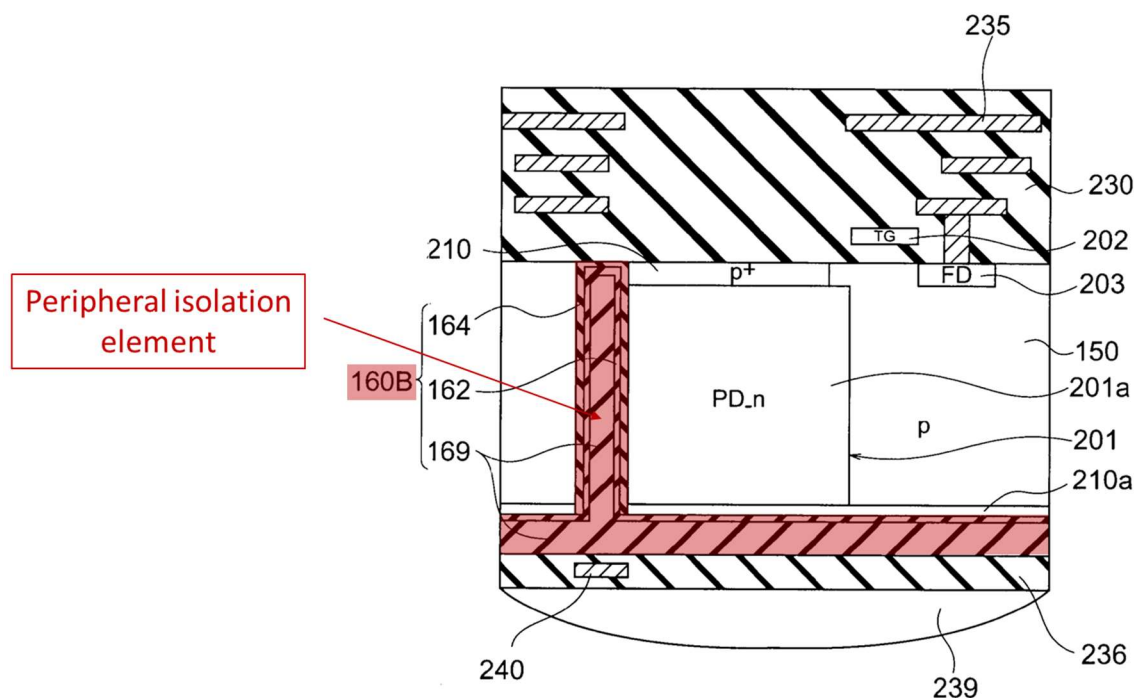


FIG. 10

Iida, Fig. 10 (annotated).

7. Claim 7: “The device of claim 1, wherein said peripheral isolation element comprises an oxide.”

92. Iida teaches or suggests this limitation.

93. As discussed above regarding limitation 1[e] and claim 3, Iida discloses a *peripheral isolation element 160B compris[ing] a silicon dioxide layer 164*. Silicon oxide is *an oxide*.

8. Claim 8: “The device of claim 1, wherein said peripheral isolation element provides a passivating negative charge.”

94. Iida teaches or suggests this limitation.

95. As discussed above regarding claim 1, Iida discloses a pixel separation structure 160B corresponding to the *peripheral isolation element*, and that pixel separation structure comprises a hafnium oxide “fixed charge” film 162.

96. The hafnium oxide negative fixed charge film 162 in Iida’s pixel separation structure *provides a passivating negative charge*. Iida discloses that, in each of its embodiments, “interfacial shield charges of the opposite conductivity type of signal charges are induced in the vicinity of the pixel separation region of each photodiode by each fixed charge film that retains fixed charges,” thereby “restrain[ing]” “generation of dark current.” Iida, [0136]. Iida specifies that whenever electrons are used as signal charges, the “hafnium oxide” “fixed charge film 162 retains negative charges, to form a hole storage region ... in the vicinity of the interface between the fixed charge film 162 and the silicon oxide layer 164.” Iida, [0051]. The negative “fixed charge area density is adjusted ... so that a sufficient hole storage layer is formed in the vicinity of the interface, and generation of dark current is restrained.” Iida, [0051]. A POSITA would understand that Iida’s use of a shielding negative fixed charge layer in its pixel separation structure to restrain dark current is a form of passivation. *See, e.g.*, Roy, [0058]-[0063]. Indeed, the ’359 patent itself describes the restraining of dark current as passivation, *see* ’359 patent,

9:28-30 (“To prevent excessive dark current in the pixels, a passivation layer may be disposed on the side walls of the trench to prevent the generation of carriers and leakage current”), and specifically describes achieving such passivation by including a negative charge layer in its trench isolation element such as hafnium oxide or aluminum oxide, *see* ’359 patent, 9:54-62, 10:44-49.

9. Claim 10: “The device of claim 1, wherein the peripheral isolation element comprises at least one material having an index of refraction of less than about 2.1.”

97. Iida teaches or suggests this limitation.

98. As discussed above regarding limitation 1[e], Iida discloses a silicon oxide layer 164 corresponding to the *first layer* of the *peripheral isolation element*. The refractive index of silicon oxide layer 164 is 1.4, Iida, [0052], [0100], which is *less than about 2.1*.

10. Claim 11: “The device of claim 1, wherein the peripheral isolation element comprises any of aluminum oxide and hafnium oxide.”

99. Iida teaches or suggests this limitation.

100. As discussed above regarding limitation 1[e], Iida discloses a negative fixed charge film 162 “made of hafnium oxide” corresponding to the *third layer* of the *peripheral isolation element*. Iida [0099].

11. Claim 18

a) Element 18[pre]: “An imager device, comprising:”

101. Iida teaches or suggests this preamble.

102. See discussion of 1[pre].

- b) Element 18[a]: “at least two adjacent light sensitive image sensor pixels each having a light incident surface, and a backside surface opposite the light incident surface;”**

103. Iida teaches or suggests this limitation.

104. See discussion of limitation 1[a].

- c) Element 18[b]: “a peripheral isolation element separating said at least two adjacent light sensitive pixels so as to reduce optical crosstalk therebetween,”**

105. Iida teaches or suggests this limitation.

106. As discussed above regarding limitation 1[b], Iida discloses a “trench-type pixel separation structure 160B” corresponding to the *peripheral isolation element*. Iida, [0098]-[0099].

107. Furthermore, “each trench-type pixel separation structure 160 is provided between adjacent pixels in a silicon substrate 150 in which photodiodes 201 ... are formed.” Iida, [0081]. Iida discloses that the pixel separation structure serves to reduce optical crosstalk between adjacent pixels. Iida, [0102] (“*Optical crosstalk is reduced* by each pixel separation structure as described above.”); Iida, [0013], [0022]-[0023].

- d) Element 18[c]: “said isolation element comprising at least two materials having different indices of refraction,”**

108. Iida teaches or suggests this limitation.

109. See discussion of limitation 1[d].

- e) **Element 18[d]: “at least one doped region disposed on at least one of the light incident surface and the backside surface,”**

110. Iida teaches or suggests this limitation.

111. See discussion of limitation 1[c].

- f) **Element 18[e]: “wherein said peripheral isolation element comprises a first, a second and a third layer,”**

112. Iida teaches or suggests this limitation.

113. See discussion of limitation 1[e].

- g) **Element 18[f]: “wherein said third layer is disposed between said first and second layers, and”**

114. Iida teaches or suggests this limitation.

115. See discussion of limitation 1[f].

- h) **Element 18[g]: “wherein each of said first and second layers exhibits an index of refraction less than an index of refraction of said third layer.”**

116. Iida teaches or suggests this limitation.

117. See discussion of limitation 1[g].

- 12. **Claim 23: “The device of claim 18, wherein the peripheral isolation element extends from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels.”**

118. Iida teaches or suggests this limitation.

119. Claim 23 is the same as claim 5, except that claim 23 omits the word “substantially.” As discussed above with respect to claim 5, and as shown in Figure 10, the pixel separation structure 160B *extends from the light incident surface to the backside surface of at least one of the two adjacent light sensitive pixels.* See Iida, [0081].

13. Claim 25: “The device of claim 19, wherein said at least two pixels are formed monolithically in a common semiconductor substrate.”

120. Iida teaches or suggests this limitation.

121. The ’359 patent specifies: “As used herein, the term ‘monolithic’ refers to an electronic device in which electronic components are formed on the same substrate. For example, two monolithic pixel elements are pixel elements that are formed on the same semiconductor substrate.” ’359 patent, 5:19-23.

122. Iida discloses forming *at least two pixels in a common semiconductor substrate*: “silicon substrate 150.” See Iida, [0081] (disclosing that pixel separation structures are “provided between adjacent pixels in a silicon substrate 150 in which photodiodes 201 ... are formed”), [0084] (disclosing that “the structure on the side of the metal interconnect layers 235 is completed on the silicon substrate 150”), [0100] (referencing “semiconductor substrate 150”). Thus, Iida teaches forming its pixels *monolithically in a common semiconductor substrate*.

14. **Claim 38: “The device of claim 1, wherein each of said at least two adjacent light sensitive image sensor pixels comprises a semiconductor portion providing said light incident surface and said backside surface, wherein said peripheral isolation element isolates the semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”**

123. Iida teaches or suggests this limitation.

124. First, the *light sensitive image sensor pixel* disclosed in Iida’s Figure 10 comprises *a semiconductor portion*: “silicon substrate 150.” Iida, [0081] (“[E]ach trench-type pixel separation structure 160 is provided between adjacent pixels in a silicon substrate 150 in which photodiodes 201 ... are formed.”).

125. Second, Iida’s silicon substrate 150 provides a *light incident surface* and a *backside surface*. As discussed above regarding limitation 1[a], (i) the *light incident surface* of the pixel depicted in Figure 10 is the interface between the pixel and the horizontal portion of negative fixed charge film 162, and (ii) the *backside surface* of the pixel depicted in Figure 10 is the interface between the pixel and insulating film 230. Iida, [0082].

126. Third, Iida discloses that the *peripheral isolation element isolates the semiconductor portions of said the at least two adjacent light sensitive image sensor pixels*. Iida discloses that “each trench-type pixel separation structure 160 is provided between adjacent pixels in a silicon substrate 150 in which photodiodes 201 ... are formed.” Iida, [0081].

15. Claim 39: “The device of claim 38, wherein said peripheral isolation element optically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”

127. Iida teaches or suggests this limitation.

128. Iida discloses that its pixel separation structure (*peripheral isolation element*) reduces optical crosstalk between adjacent pixels. *See* Iida, [0013] (“To restrain occurrences of optical crosstalk, a separation with a trench in which a material to reflect incident light is buried is effectively performed.”), [0022]-[0023] (“[T]o ... reduce optical crosstalk ..., pixel separation structures ... are needed...”), [0102] (“Optical crosstalk is reduced by each pixel separation structure as described above[.]”). Reducing optical crosstalk between adjacent pixels means that those pixels are optically isolated from each other.

129. As discussed above regarding claim 38, the *semiconductor portion* of each pixel is the silicon substrate 150 in which photodiodes 201 are formed. Iida discloses that the reduction of optical crosstalk is achieved through reflection of light incident at the interface between the pixel separation structure and the semiconductor silicon substrate 150. Iida, [0101]-[0107]. Thus, Iida’s pixel separation structure *optically isolates the semiconductor portions of adjacent pixels*.

16. Claim 40: “The device of claim 38, wherein said peripheral isolation element electrically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”

130. Iida teaches or suggests this limitation.

131. Iida discloses that its pixel separation structure 160B (*peripheral isolation element*) serves to *electrically isolate* the *semiconductor portions of adjacent pixels*. Indeed, Iida notes a problem in the existing art that as “the depths of pixel separations and photodiodes become smaller.... The charges generated due to light absorption in regions deeper than the pixel separations and the photodiodes enter adjacent pixels.” Iida, [0010]. To address this, Iida teaches that “pixel separation structures that can be formed at sufficiently deep locations are needed.” Iida, [0023].

132. Iida discloses that “pixel separation structure 160 has a trench that penetrates through the silicon substrate 150 from the back face side to the front face side.” Iida, [0081]. As discussed above regarding limitation 1[a], pixel separation structure 160B (including silicon dioxide layer 164) extends from the pixel’s light incident surface (162/210a interface) to the pixel’s backside surface (150/230 interface).

133. A POSITA would have known that a gap in sidewall reflection between the light incident surface and the backside surface can allow electrons to escape under the sidewall trench into a neighboring pixel. *See, e.g.,* Roy, [0039] (“Usually, trench

11 has a depth ranging between 0.3 and 0.7 μm . Thereby, this trench limits the crosstalk without however completely canceling it since electron/hole pairs may be photogenerated down to a depth from 3 to 10 μm Electrons can thus pass under trench 11 from the N area of a photodiode to the N area of a neighboring photodiode.”); Shinohara, [0064] (because “adjacent pixels are physically isolated from each other ... the leakage of charge in the photodiode PD into an adjacent pixel can be substantially prevented”).

134. As discussed above regarding claim 38, the *semiconductor portion* of each pixel is the silicon substrate 150 in which each trench-type pixel separation structure is provided. Iida, [0081], [0082]. Thus, Iida’s pixel separation structure *electrically isolates the semiconductor portions of adjacent pixels*.

17. Claim 41: “The device of claim 38, wherein an index of refraction of the semiconductor portion of each of said at least two adjacent image sensor pixels is different from indices of refraction of said layers of the peripheral isolation element such that light incident from each of said semiconductor portions on said peripheral isolation element is reflected, thereby providing optical isolation between the pixels.”

135. Iida teaches or suggests this limitation.

136. Iida discloses that the refractive index of silicon substrate 150 (*semiconductor portion* of each pixel) is 3.9. Iida, [0100]. As discussed above regarding limitation 1[g], the *indices of refraction* of the *layers* of Iida’s pixel separation structure 160B (*peripheral isolation element*) are 1.4 for silicon oxide

layer 164, 2.0 for negative fixed charge film 162, and preferably less than that of hafnium dioxide (i.e., $n < 2.0$) for low refractive index film 169. Iida, [0099]-[0100].

These *indices of refraction are different from* that of silicon substrate 150 ($n=3.9$).

137. Furthermore, the difference in indices of refraction is such that *light incident from each of said semiconductor portions on said peripheral isolation element is reflected, thereby providing optical isolation between the pixels*. In describing the embodiment depicted in Figure 10, Iida discloses that “[o]ptical crosstalk is reduced by each pixel separation structure as described above, and obliquely incident light is total-reflected by a structure that is filled with a material having a lower refractive index than 3.9, which is the refractive index of the single-crystal silicon of the semiconductor substrate.” Iida, [0102]; *see also, e.g.*, Iida, [0108] (“This embodiment can achieve ... the effect to reduce optical crosstalk.”).

18. Claim 42: “The device of claim 1, wherein said at least two adjacent light sensitive image sensor pixels are formed monolithically on a common semiconductor substrate and are isolated from one another by said peripheral isolation element.”

138. Iida teaches or suggests this limitation.

139. As discussed above regarding claim 25, Iida discloses that its *adjacent light sensitive image sensor pixels are formed monolithically on a common semiconductor substrate*.

140. Iida also discloses that its pixels are *isolated from one another* by its *peripheral isolation element* 160B. Iida discloses that “each trench-type pixel separation structure 160 is provided between adjacent pixels in a silicon substrate 150 in which photodiodes 201 ... are formed.” Iida, [0081].

19. Claim 43: “The device of claim 1, wherein said peripheral isolation element is a trench isolation element.”

141. Iida teaches or suggests this limitation.

142. Iida discloses that its pixel separation structure 160B (*peripheral isolation element*) is a *trench isolation element*. Iida, [0081] (with respect to Figure 9, disclosing a “trench-type pixel separation structure.... This pixel separation structure 160 has a trench that penetrates through the silicon substrate 150 from the back face side to the front face side.”), [0098] (with respect to Figure 10, disclosing that “the trench-type pixel separation structure 160 is replaced with a trench-type pixel separation structure 160B”).

20. Claim 45: “The device of claim 18, wherein each of said at least two adjacent light sensitive image sensor pixels comprises a semiconductor portion providing said light incident surface and said backside surface, wherein said peripheral isolation element isolates the semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”

143. Iida teaches or suggests this limitation.

144. See discussion of claim 38.

- 21. Claim 46: “The device of claim 45, wherein said peripheral isolation element optically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”**

145. Iida teaches or suggests this limitation.

146. See discussion of claim 39.

- 22. Claim 47: “The device of claim 46, wherein said peripheral isolation element electrically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”**

147. Iida teaches or suggests this limitation.

148. See discussion of claim 40.

- 23. Claim 48: “The device of claim 47, wherein an index of refraction of the semiconductor portion of each of said at least two adjacent image sensor pixels is different from indices of refraction of said layers of the peripheral isolation element such that light incident from each of said semiconductor portions on said peripheral isolation element is reflected, thereby providing optical isolation between the pixels.”**

149. Iida teaches or suggests this limitation.

150. See discussion of claim 41.

- 24. Claim 49: “The device of claim 18, wherein said at least two adjacent light sensitive image sensor pixels are formed monolithically on a common semiconductor substrate and are isolated from one another by said peripheral isolation element.”**

151. Iida teaches or suggests this limitation.

152. See discussion of claim 42.

25. Claim 50: “The device of claim 18, wherein said peripheral isolation element is a trench isolation element.”

153. Iida teaches or suggests this limitation.

154. See discussion of claim 43.

26. Claim 52: “The imager device of claim 38, wherein at least one of the first layer and the second layer of said peripheral isolation element and said semiconductor portion of each of said at least two adjacent pixels comprise different materials.”

155. Iida teaches or suggests this limitation.

156. As discussed above regarding limitation 1[e], the layers of Iida’s pixel separation structure 160B (*peripheral isolation element*) include silicon oxide layer 164 (*first layer*) and low refractive index film 169 (*second layer*). The *semiconductor portion* of Iida’s pixels *comprises a different material*: “p-type silicon substrate 150.” Iida, [0049].

27. Claim 53: “The imager device of claim 1, wherein the first layer and the second layer of said peripheral isolation element comprise different materials.”

157. Iida teaches or suggests this limitation.

158. As discussed regarding limitations 1[d] and 1[e], Iida teaches using a low refractive index material in film 169 (*second layer*) that differs from the silicon oxide material of layer 164 (*first layer*). Iida [0052], [0099], [0100].

28. Claim 54: “The imager device of claim 1, wherein the peripheral isolation element comprises at least three materials.”

159. Iida teaches or suggests this limitation.

160. As discussed above regarding limitations 1[e] and 1[g], Iida discloses a pixel separation structure 160B (*peripheral isolation element*) that *comprises three materials*: (1) silicon oxide layer 164 (*first layer*) with a refractive index of 1.4; (2) low refractive index film 169 (*second layer*) with a refractive index “preferably ... lower” than 2.0 and “to improve the effect to reduce optical crosstalk, it is preferable to use a material having a lower refractive index than 1.4”; and (3) hafnium oxide film 162 (*third layer*) with a refractive index of 2.0. Iida [0052], [0100]. Because Iida teaches three distinct layers, each with a different refractive index, Iida teaches a *peripheral isolation element* that *comprises at least three materials*.

29. Claim 55: “The imager device of claim 1, wherein the peripheral isolation element comprises more than three layers.”

161. Iida teaches or suggests this limitation.

162. Iida’s tenth embodiment, depicted in Iida’s Figure 16, is an imager device that is an obvious extension of Iida’s fourth embodiment, depicted in Figure 10.

163. Indeed, the pixel separation structure 160C of Figure 16 retains the same three layers as pixel separation structure 160B in Figure 10 (layers 164, 162, and 169) but adds two additional layers (layers 166 and 168). As shown below, the “pixel separation structure 160C” (*peripheral isolation element*) in Iida’s tenth embodiment comprises five layers: “the silicon oxide layer 164, the fixed charge

film 162, the silicon oxide layer 166, the polycrystalline silicon film 168, and the low refractive index material film 169.” Iida, [0126]. As can be seen from Figures 9-11 and 15-16, Iida’s pixel separation structure can be constructed from one or more of layers 162, 164, 166, 168, and 169. The addition of the silicon oxide layer 166 and polycrystalline silicon film 168 provides additional boundaries of varying indices of refraction, which results in reduced “optical crosstalk caused by obliquely incident light entering adjacent pixels” and an “imaging device with higher sensitivity” than the device of Figure 10. Iida, [0127].

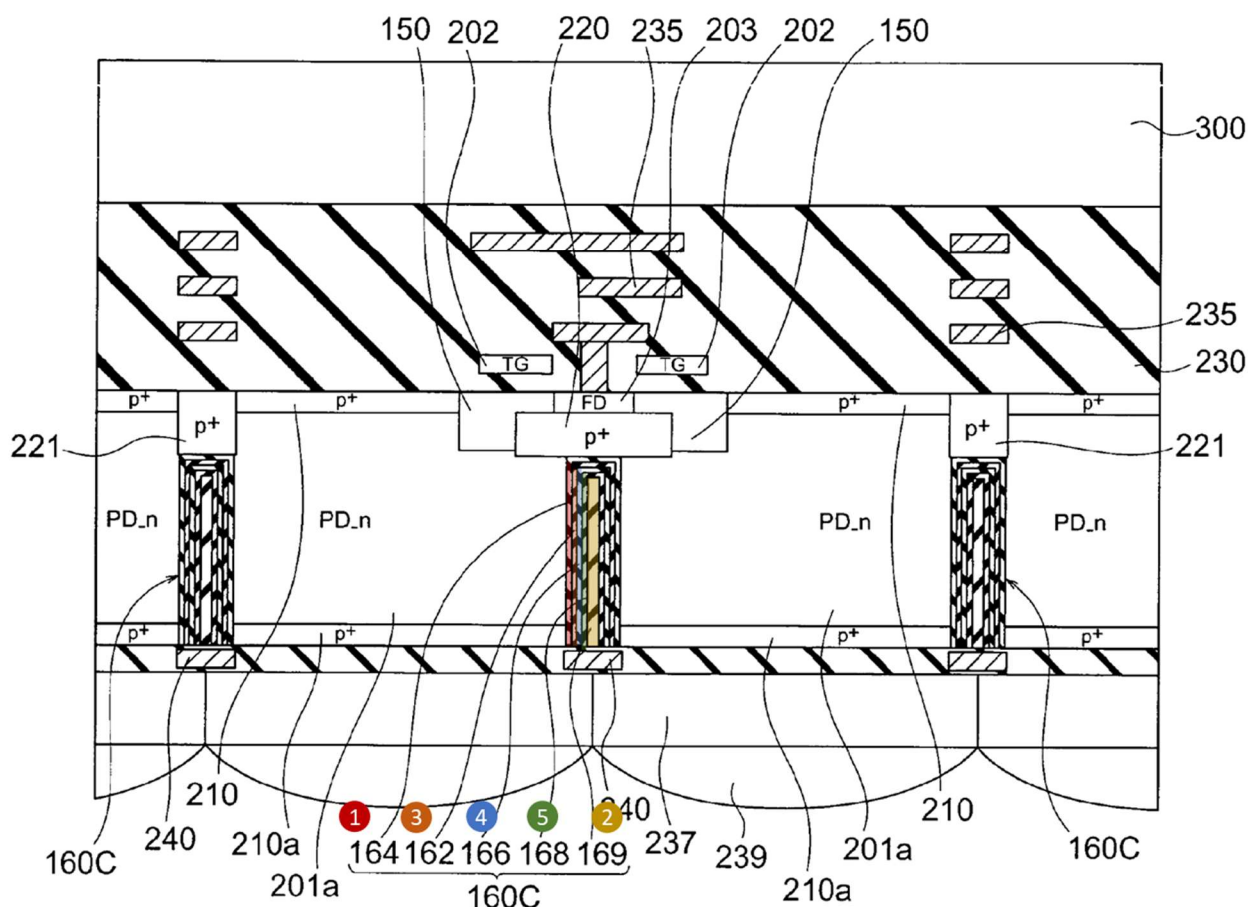


FIG. 16

Iida, Fig. 16 (annotated).

164. A POSITA would have applied the five-layer pixel separation structure of Figure 16 to the imager device of Figure 10 as an application of a known technique to a known device ready for improvement to yield predictable results. Specifically, when forming the layers of the pixel separation structure, a POSITA would know to repeat the application of film layers two additional times, including with the same material (silicon dioxide) already used in Figure 10's layer 164. As shown above, the resulting combination provides a *peripheral isolation element comprising more than three layers*.

165. Iida's tenth embodiment, depicted in Figure 16, itself meets all the limitations of claim 1 in addition to claim 55. Iida's Figure 16 "shows a solid-state imaging device" as recited in element 1[pre].

166. A "floating diffusion layer 203 is provided between the adjacent pixels." Iida, [0111]. Further, "an insulating film 236 that transmits incident light is provided on the back face side," Iida, [0112], and is a *light incident surface*. Figure 16 also depicts an interlayer insulating film 230 as a *backside surface opposite the light incident surface*. See Iida, [0082] ("an interlayer insulating film 230 is provided on the front face of the silicon substrate 150"). Thus, the tenth embodiment discloses *at least two adjacent light sensitive image sensor pixels each having a light incident surface, and a backside surface opposite the light incident surface*, as recited in element 1[a].

167. The tenth embodiment (Figure 16) also includes “a trench-type pixel separation structure 160C,” Iida, [0126], *at least partially separating adjacent pixels*, Iida, Fig. 16, as recited by element 1[b].

168. The tenth embodiment includes “[a] p⁺-type impurity diffused region 210 for preventing dark current from flowing into a PD_n-region 201a and the interlaying insulating film 230.” Iida, [0112]. For the same reasons provided in the discussion of limitation 1[c] above, the tenth embodiment of Iida discloses each pixel having *at least one doped region disposed on at least one of the light incident surface and the backside surface*.

169. The tenth embodiment discloses a pixel separation structure 160C with a “stack film being formed with the silicon oxide layer 164, the fixed charge film 162 [made of hafnium oxide, n=2.0], the silicon oxide layer 166, the polycrystalline silicon film 168, and the low refractive index material film 169.” Iida, [0126]. Iida elsewhere discloses that the refractive index of the “low refractive index material” in film 169 is “preferably ... lower ... than 2.0,” Iida, [0100] (*see also* Iida, [0052]). As such, the tenth embodiment discloses a pixel separation structure comprising *at least two materials having different indices of refraction* as recited by element 1[d].

170. For the reasons stated above regarding limitation 1[e], and because the tenth embodiment (Figure 16) and the fourth embodiment (Figure 10) share at least

layers 164, 162, and 169, the tenth embodiment discloses a pixel separation structure comprising *a first, a second and a third layer* as recited by element 1[e].

171. For the reasons stated above regarding limitation 1[f], and because the tenth embodiment (Figure 16) and the fourth embodiment (Figure 10) share at least layers 164, 162, and 169, the tenth embodiment discloses a *third layer*, i.e., hafnium oxide film 162, *disposed between the first layer*, i.e., silicon oxide layer 164, and the *second layer*, i.e., low refractive index film 169.⁷

172. The refractive index of Iida's silicon oxide layer 164 (*first layer*) is 1.4. Iida, [0052], [0100]. The refractive index of Iida's low refractive index film 169 (*second layer*) is "preferably ... lower ... than 2.0." Iida, [0100]. The refractive index of Iida's hafnium oxide film 162 (*third layer*) is 2.0. Iida, [0052], [0100]. Thus, the refractive indices of Iida's silicon oxide layer 164 and low refractive index film 169

⁷ In the Related Proceeding, Patent Owner proposed to construe *said third layer is disposed between said first and second layers* to mean "a third layer between the first and second layers, wherein the first and second layers can be different materials from one another," while Petitioner proposed that the third layer is in contact with the first and second layers on opposing sides. Ex-1011; Ex-1012. For purposes of this petition, my analysis adopts Patent Owner's construction, which is met by Iida's tenth embodiment, as explained in the main text.

(*first and second layers*, 1.4 and <2.0) are less than the refractive index of Iida's hafnium oxide layer 162 (*third layer*, 2.0), as recited by element 1[g].

30. Claim 56: “The imager device of claim 1, wherein the peripheral isolation element comprises a light trapping material filling a trench.”

173. Iida teaches or suggests this limitation.

174. Iida discloses that its pixel separation structure 160B (*peripheral isolation element*) is filled with material that traps light. In describing the embodiment depicted in Figure 10, Iida discloses that “the effect to reduce optical crosstalk caused by obliquely incident light entering adjacent pixels is improved, and a solid-state imaging device with higher sensitivity can be obtained.” Iida, [0101]. In particular, “[o]ptical crosstalk is reduced by each pixel separation structure as described above, and obliquely incident light is total-reflected by a structure that is filled with a material having a lower refractive index than 3.9.” Iida, [0102]. The referenced “structure” is pixel separation structure 160B, which is a “trench-type” structure. Iida, [0098]-[0099]; *see also* Iida, [0089] (describing “the filling of the trench portion”). The reflection of light by the material filling the trench-type structure, and the resulting higher sensitivity of the imaging device, demonstrate that the pixel separation structure 160B comprises *light trapping material filling a trench*.

175. Furthermore, in describing the embodiment depicted in Figure 3, Iida discloses that obliquely incident light reaching the pixel separation structure 160 “is reflected and does not enter the adjacent pixels.” This is because the refractive index of each of the silicon oxide layer 164 and the hafnium oxide film is lower than the refractive index of silicon.” Iida, [0052]. This reference to light reflection further confirms that Iida’s pixel separation structure 160 comprises “light trapping material filling a trench,” as recited in the claim. The foregoing disclosure with respect to Figure 3 is equally applicable to the embodiment in Figure 10 because Figure 10, like Figure 3, comprises a pixel separation structure with silicon oxide layer 164 and hafnium oxide film 162, and also comprises silicon substrate 150 and photodiode 201.

31. Claim 57: “The imager device of claim 56, wherein the trench is one of a shallow trench and a deep trench.”

176. Iida teaches or suggests this limitation.

177. In describing its pixel separation structure 160 in Figure 9, Iida discloses that “[a] trench extending from the light incidence side is ... formed, and a fixed charge film is formed in the trench.” Iida, [0085]. Iida depicts pixel separation structure 160B in Figure 10 as a similar trench, with the addition of low refractive index film 169. The ’359 patent states that, “[f]or simplicity, the figures in this disclosure show deep trench isolation but it should be understood that shallow trench

isolation architectures can be utilized, and that deep trench isolation need not completely extend from one side to the other.” ’359 patent, 7:56-60.

178. As discussed above regarding claim 5, pixel separation structure 160B extends from the claimed *light incident surface* to the claimed *backside surface*. Because the pixel separation structure 160B extends across the entire pixel, a POSITA would recognize the structure as a *deep trench*. See also Iida [0023] (emphasizing need for “pixel separation structures that ... can be formed at sufficiently deep locations ... so as not to compress the volumes of photodiodes”).

32. Claim 58: “The imager device of claim 45, wherein at least one of the first layer and the second layer of the peripheral isolation element and said semiconductor portion of each of said at least two adjacent pixels comprise different materials.”

179. Iida teaches or suggests this limitation.

180. See discussion of claim 52.

33. Claim 59: “The imager device of claim 18, wherein the first layer and the second layer of said peripheral isolation element comprise different materials.”

181. Iida teaches or suggests this limitation.

182. See discussion of claim 53.

34. Claim 60: “The imager device of claim 18, wherein the peripheral isolation element comprises at least three materials.”

183. Iida teaches or suggests this limitation.

184. See discussion of claim 54.

35. Claim 61: “The imager device of claim 18, wherein the peripheral isolation element comprises more than three layers.”

185. Iida teaches or suggests this limitation.

186. See discussion of claim 55.

187. Additionally, with respect to Iida’s tenth embodiment (Figure 16) itself meeting the limitations of claim 18, see the discussion of related claim 1 elements in claim 55. Further to element 18[b], Iida’s tenth embodiment (Figure 16) includes “a trench-type pixel separation structure 160C,” Iida, [0126], separating adjacent pixels, Iida, Fig. 16. Regarding the tenth embodiment, “the effect to reduce optical crosstalk caused by obliquely incident light entering adjacent pixels can be increased, and accordingly, a solid-state imaging device with higher sensitivity can be obtained.” Iida, [0127]. As such, Iida’s tenth embodiment teaches a pixel separation structure *separating said at least two adjacent light sensitive pixels so as to reduce optical crosstalk therebetween.*

36. Claim 62: “The imager device of claim 18, wherein the peripheral isolation element comprises a light trapping material filling a trench.”

188. Iida teaches or suggests this limitation.

189. See discussion of claim 56.

37. Claim 63: “The imager device of claim 62, wherein the trench is one of a shallow trench and a deep trench.”

190. Iida teaches or suggests this limitation.

191. See discussion of claim 57.

38. Claim 64: “The imager device of claim 1, wherein said peripheral isolation element comprises a trench isolation element formed by filling a trench with said first, said second, and said third layers.”

192. Iida teaches or suggests this limitation.

193. As discussed above regarding limitation 1[e], Iida discloses a pixel separation structure 160B (*peripheral isolation element*) comprising a silicon oxide layer 164 (*first layer*), a negative fixed charge film 162 (*third layer*), and a low refractive index film 169 (*second layer*). Iida discloses that silicon oxide layer 164, negative fixed charge film 162, and film 169 “are buried in a trench formed in a silicon substrate ... to fill the inside of the pixel separation structure 160B.” Iida, [0099]. Iida further explains that its pixel separation structure is formed by “filling” a “trench” with the “silicon oxide layer,” the “hafnium oxide film as a fixed charge film,” and the “low refractive index” film. Iida, [0106]-[0107], [0109]; *see also* Iida, [0089] (describing “filling of the pixel separation structure 160” as “filling of the trench portion”).

39. Claim 67: “The imager device of claim 1, wherein said peripheral isolation element is configured to reflect at least a portion of light incident thereon from any of said two adjacent light sensitive pixels back to that pixel.”

194. Iida teaches or suggests this limitation.

195. In describing the embodiment depicted in Figure 10, Iida discloses that “[o]ptical crosstalk is reduced by each pixel separation structure as described above, and obliquely incident light is total-reflected by a structure that is filled with a material having a lower refractive index than 3.9, which is the refractive index of the single-crystal silicon of the semiconductor substrate.” Iida, [0102]. Iida further discloses that the “interface that faces obliquely incident light first is the interface between the single-crystal silicon having a refractive index of 3.9 and the silicon oxide layer having a refractive index of 1.4, and the critical angle at this point is 21 degrees.” Iida, [0104]. “Accordingly, obliquely incident light that enters the solid-state imaging device at an incident angle of 69 degrees or smaller is total-reflected by this interface, and occurrences of optical crosstalk are restrained.” Iida, [0104].

196. *At least a portion of light incident on the pixel’s pixel separation structure is reflect[ed] back to that pixel*, as Iida discloses that the pixel separation structure reduces optical crosstalk by preventing the “obliquely incident light” from “entering adjacent pixels.” Iida, [0101]. Iida also discloses that the pixel separation structure “achieve[s] higher sensitivity” for the solid-state imaging device. Iida, [0100]. The higher sensitivity is achieved by reflecting light incident on the pixel separation structure 160B back into the pixel, thereby increasing the likelihood that the light is absorbed by the photodiode.

40. Claim 68: “The imager device of claim 67, wherein the peripheral isolation element is further configured to optically isolate said two adjacent light sensitive pixels.”

197. Iida teaches or suggests this limitation.

198. See discussion of claim 39.

41. Claim 69: “The imager device of claim 68, wherein the peripheral isolation element is further configured to electrically isolate said two adjacent light sensitive pixels.”

199. Iida teaches or suggests this limitation.

200. See discussion of claim 40.

42. Claim 70: “The imager device of claim 18, wherein said peripheral isolation element comprises a trench isolation element formed by filling a trench with said first, said second, and said third layers.”

201. Iida teaches or suggests this limitation.

202. See discussion of claim 64.

43. Claim 73: “The imager device of claim 18, wherein said peripheral isolation element is configured to reflect at least a portion of light incident thereon from any of said two adjacent light sensitive pixels back to that pixel.”

203. Iida teaches or suggests this limitation.

204. See discussion of claim 67.

44. Claim 74: “The imager device of claim 73, wherein the peripheral isolation element is further configured to optically isolate said two adjacent light sensitive pixels.”

205. Iida teaches or suggests this limitation.

206. See discussion of claim 39.

45. Claim 75: “The imager device of claim 74, wherein the peripheral isolation element is further configured to electrically isolate said two adjacent light sensitive pixels.”

207. Iida teaches or suggests this limitation.

208. See discussion of claim 40.

46. Claim 80: “The imager device of claim 1, wherein the peripheral isolation element comprises five layers.”

209. Iida teaches or suggests this limitation.

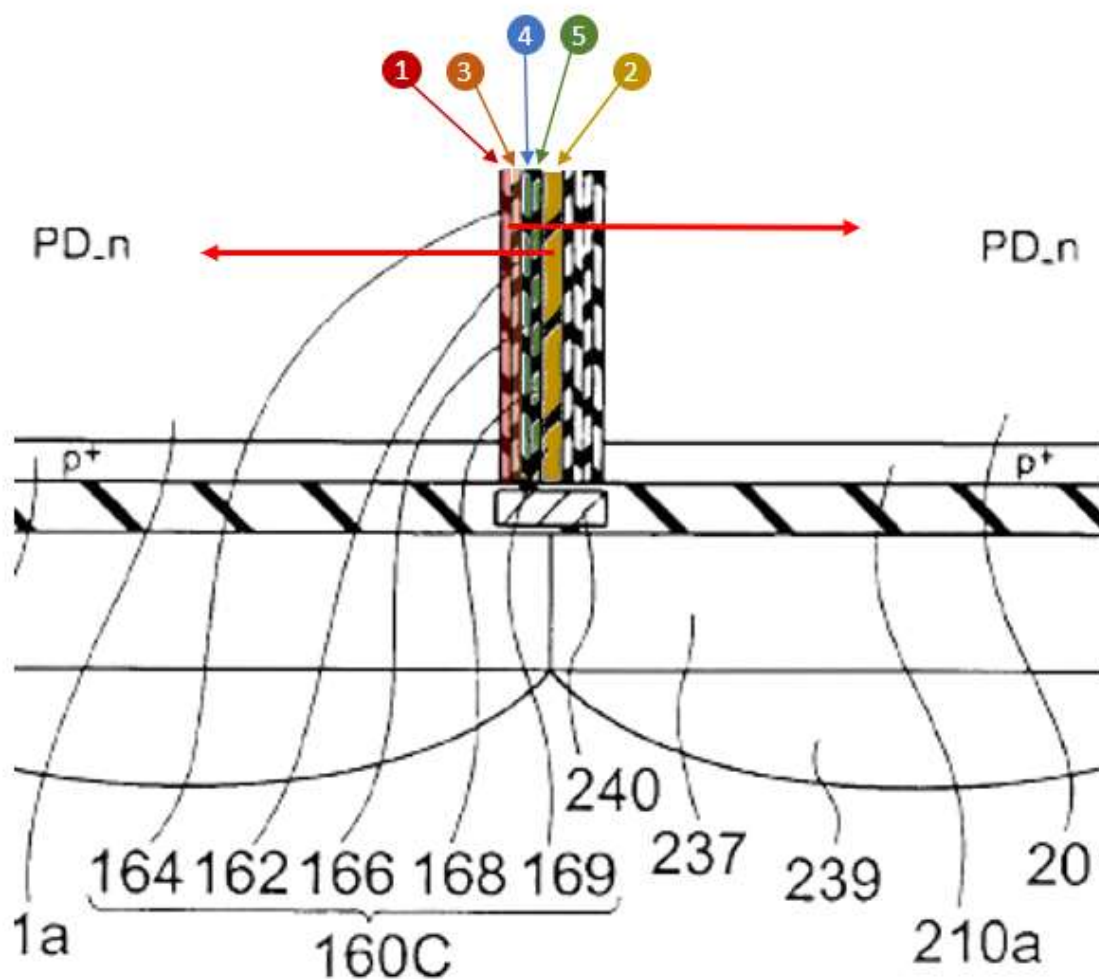
210. See discussion of claim 55.

47. Claim 81: “The imager device of claim 80, wherein the five layers include the first layer, the second layer, the third layer, a fourth layer disposed between the first layer and one of said adjacent pixels and a fifth layer disposed between the second layer and the other one of said adjacent pixels.”

211. Iida teaches or suggests this limitation.

212. As discussed above regarding claims 55 and 80, Iida’s tenth embodiment, depicted in Iida’s Figure 16, is an imager device that is an obvious extension of Iida’s fourth embodiment, depicted in Figure 10. A POSITA would have applied the five-layer pixel separation structure of Figure 16 to the imager device of Figure 10 as an application of a known technique to a known device ready for improvement to yield predictable results. Regardless, Iida’s tenth embodiment independently satisfies all the limitations of claims 1 and 80, as discussed regarding claim 55.

213. Iida's fourth embodiment (Figure 10) as modified by the teachings of Iida's tenth embodiment (Figure 16), or as taught directly by the tenth embodiment, discloses a silicon oxide layer 164 (*first layer*), the negative fixed charge film 162 (*third layer*), the silicon oxide layer 166 (*fourth layer*), the polycrystalline silicon film 168 (*fifth layer*), and the low refractive index material film 169 (*second layer*). Iida, [0126]; *see also* Iida, [0099].



Iida, Fig. 16 (excerpted and annotated).

214. As shown above, the *fourth layer* (blue) is *disposed between* the *first layer* (red) and the *adjacent pixel* to the right, and the *fifth layer* (green) is *disposed between* the *second layer* (gold) and the *adjacent pixel* to the left.

215. A POSITA would have had a reasonable expectation of success. It would have been well within the abilities of a POSITA to modify Figure 10 in Iida. It would have involved routine manufacturing steps that Iida had already used in its device with predictable results.

48. Claim 82: “The imager device of claim 18, wherein the peripheral isolation element comprises five layers.”

216. Iida teaches or suggests this limitation.

217. See discussion of claim 61.

49. Claim 83: “The imager device of claim 82, wherein the five layers include the first layer, the second layer, the third layer, a fourth layer disposed between the first layer and one of said adjacent pixels and a fifth layer disposed between the second layer and the other one of said adjacent pixels.”

218. Iida teaches or suggests this limitation.

219. See discussions of claims 81 and 82.

B. Ground 2: Claims 12-17, 19-22, 26-29, and 76-79 Are Obvious Based on Iida and Haddad188

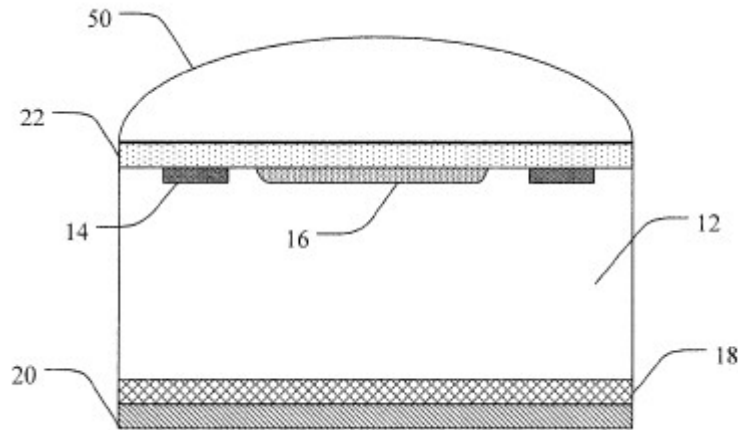
1. Overview of Haddad188

220. I understand that Haddad188 is prior art because it was published on March 24, 2011, before the '359 patent's provisional application filing date of March 22, 2012.

221. Haddad188 is cited on the face of the '359 patent (page 6, second column), among several hundred other references cited. Haddad188 was also cited in an IDS during prosecution of the '359 patent (again among many other references).

222. Like the '359 patent, Haddad188 is directed to light-sensitive pixels in imaging devices with pixel separation structures. Haddad188, 1:24-30 (“The present disclosure provides photosensitive devices and associated methods. In one aspect, for example, a photosensitive device can include a semiconductor substrate having multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction.”), 21:12-13. Haddad188 also discloses a “textured region at the point of entry of the electromagnetic radiation,” which “provide[s] enhancement and/or filtering of the incoming electromagnetic radiation.” Haddad188, 20:30-21:2. Haddad188’s “textured region includes surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof,” and contemplates “numerous surface feature morphologies.” Haddad188, 2:18-27.

223. An exemplary embodiment from Haddad188 is depicted below.



Haddad188, Fig. 5.

224. Haddad188's Figure 5 is a schematic view of a photosensitive device. Haddad188, 3:33-34. Among other things, it depicts a "textured region 18 coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation." Haddad188, 9:18-21.

2. Motivation to Combine Iida and Haddad188

225. It would have been obvious to combine Iida and Haddad188.

226. A POSITA would have been motivated to use Haddad188's textured regions with Iida's semiconductor substrate faces and pixel separation structures. Haddad188 teaches that a "textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device." Haddad188, 14:29-31. Haddad188 explains that "[t]extured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident

electromagnetic radiation within the device.... Such internal reflection causes the effective absorption length to be greater than the thickness of the substrate.” Haddad188, 15:14-18. As a result of increased absorption length, quantum efficiency of the device increases, “leading to an improved signal to noise ratio.” Haddad188, 15:18-19. For example, Haddad188 discloses a “photosensitive device having textured regions on the sides of the semiconductor substrate 12. Such a configuration allows electromagnetic radiation normally exiting through the sides of the device to be further diffused and absorbed within [the] semiconductor substrate.” Haddad188, 21:12-15, Fig. 3. “The textured region(s) can be located on one or more sides to facilitate the enhanced absorption.” Haddad188, 21:15-16. Whether to use Haddad188’s textured regions would have depended on the particular design needs regarding the cost of manufacture and the desired improvement in absorption and signal-to-noise ratio.

227. Haddad188 discloses that “[o]ne effective method of producing a textured region is through laser processing.” Haddad188, 16:3-4; 16:14-19 (“[A] surface of a semiconductor material is irradiated with laser radiation to form a textured or surface modified region.”). A POSITA would know that laser provides excellent control of the surface profile and may be programmed to offer optical performance that exceeds simple wet and dry etching of surfaces, especially when texturing is being implemented. Applying Haddad188’s processing to Iida’s pixel separation structure 160B would have yielded an Iida device such as the following:

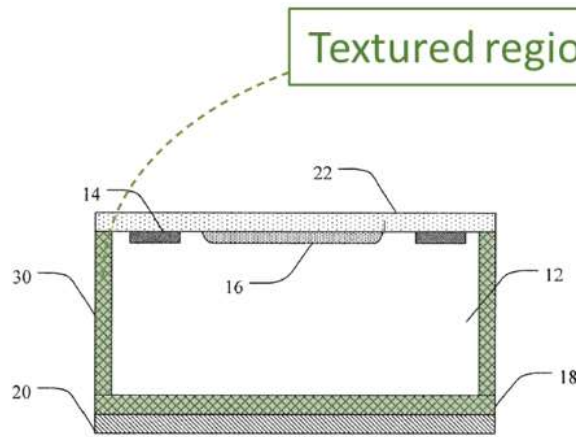


FIG. 3

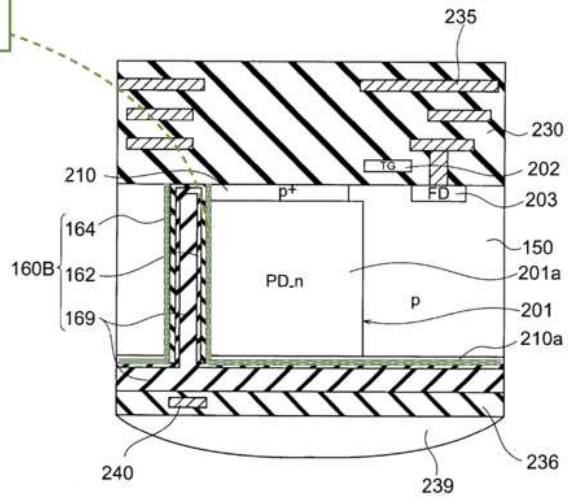


FIG. 10

Haddad188, Fig. 3 (annotated); Iida, Fig 10 (annotated and modified).

228. A POSITA would have known to apply Haddad188's textured regions to Iida's photosensitive device. For example, like Iida, Haddad188 also places trench isolation structures between adjacent pixels to reduce crosstalk. *See* Iida, [0057] ("As described above, according to this embodiment, the pixel separation structure 160 performs pixel separations. Accordingly, a solid-state imaging device that has less optical crosstalk and less electrical crosstalk can be obtained."); Haddad188, 22:21-29 ("Trench isolation elements can maintain pixel to pixel uniformity by reducing optical and electrical crosstalk."), 24:1-15 ("[T]he trench isolation layer can be configured to reflect incident electromagnetic radiation, in some cases until it is absorbed, thereby increasing the effective absorption length of the device.").

229. Using Haddad188's textured regions to further improve signal-to-noise ratio would have been a use of a known technique to improve similar devices in the same way. Both Iida and Haddad188 are directed to photosensitive imager devices. Iida, Abstract, [0044]; Haddad188, 1:24-30, 8:15-22. Both Iida and Haddad188 seek to minimize signal-to-noise ratio reduction as pixel size decreases. Iida discloses light trapping material on the light incident face to increase absorption. *See* Iida, [0099], Fig. 10 (showing negative fixed charge film 162 and low refractive index film 169 on the back side face). Iida also uses pixel separation structures with a stack film to minimize optical crosstalk. Iida, [0022] (“[T]o restrain a decrease in the S/N ratio (sensitivity) in the course of miniaturization of pixels, it is essential to reduce the noise components generated in the vicinity of each photodiode, and reduce optical crosstalk and electrical crosstalk”), [0023], [0044]. Haddad188's photosensitive devices include at least one textured region positioned within the semiconductor substrate to interact with electromagnetic radiation to improve efficiency over traditional photosensitive devices. Haddad188, 9:18-21, 9:32-33 (“The various devices according to aspects of the present disclosure can exhibit increased quantum efficiency over traditional photosensitive devices. Any increase in the quantum efficiency makes a large difference in the signal to noise ratio.”).

230. Given the similarities in structure and function of the image sensors described in Iida and Haddad188, a POSITA would have recognized that the

combination would have required nothing more than applying Haddad188's teachings about textured regions and trench isolation structures to Iida's teaching of trench structures to isolate image sensor pixels. Indeed, Haddad188 notes that "[t]rench isolation can include dielectric materials, reflective materials, conductive materials, and combinations thereof, including textured regions and other light diffusing features ... to reflect incident electromagnetic radiation." Haddad188, 24:5-8. Thus, applying Haddad188's textured regions to Iida's pixel isolation structures would have amounted to nothing more than applying a known technique to improve a similar device in the same way, and it would have yielded predictable results.

231. A POSITA would have recognized that incorporating Haddad188's textured regions into Iida's device would provide certain benefits. Haddad188 explains that "the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation," and can result in "increasing the semiconductor substrate's effective absorption length as compared to a semiconductor substrate lacking a textured region." Haddad188, 1:30-34. Haddad188 also explains that the trench isolation elements can further increase "the effective absorption length of the device." Haddad188, 22:27-29, 24:7-9. Additionally, Haddad188 explains that when textured regions are placed on the sides of the device, "electromagnetic radiation normally exiting through the sides of the

device” can be “further defused [diffused]⁸ and absorbed within semiconductor substrate,” resulting in “enhanced absorption.” Haddad188, 21:12-16, and that this benefit can be achieved when the textured region is included as part of the trench isolation elements. Haddad188, 24:5-9.

232. A POSITA would have had a reasonable expectation of success. It would have been well within the abilities of a POSITA to use the textured regions described in Haddad188 for Iida’s device. It would have involved routine manufacturing steps with predictable results. In particular, the fabrication process techniques used would involve standard modules, standard techniques, and standard processes. The fabrication of trench layers, including those with silicon materials and dielectrics, would have been well-known to a POSITA, as would the characteristic properties of the materials, such as optical refractive index, etch rates, and crystal quality. Fabrication processing techniques, including photolithography, etching deposition, and metallization, existed well before the relevant period.

⁸ Haddad188 clarifies that the textured region is used “to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes through to the front side of the pixel” so that the radiation can be “focused within the semiconductor substrate.” Haddad188, 24:34-25:3.

3. Claim 12: “The device of claim 1, wherein at least one of said two adjacent light sensitive pixels comprises a textured region.”

233. This limitation is obvious based on Iida in view of Haddad188.

234. Iida’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. As shown above, the modification would entail using *a textured region* in each of Iida’s *light sensitive pixels*. Haddad188 discloses “[i]n one aspect, as is shown in FIG. 1, a photosensitive diode 10 can include a semiconductor substrate 12 having multiple doped regions 14, 16 forming at least one junction, and at least one textured region 18 coupled to semiconductor substrate and positioned to interact with electromagnetic radiation.” Haddad188, 9:18-21; *see also* Haddad188, Fig. 5. Haddad188 further discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31.

235. It would have been obvious to combine Iida and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

236. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein at least one of the said two adjacent light sensitive pixels comprises a textured region.*

4. Claim 13: “The device of claim 12, wherein said textured region is coupled to the light incident surface.”

237. This limitation is obvious based on Iida in view of Haddad188.

238. Iida’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. The modification would entail a textured region that is *coupled to the light incident surface*, given that Haddad188 teaches “locating the textured region on the surface adjacent the incident electromagnetic radiation to purposely effectuate the filtering of blue wavelengths.” Haddad188, 20:32-21:2.

239. Haddad188 also discloses that at least one textured region is “positioned to interact with electromagnetic radiation.” Haddad188, 8:9-10. Haddad188 further discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31. Haddad188 also discloses that “a textured region 60 is located on the semiconductor substrate 12 adjacent to the multiple doped regions 14, 16,” Haddad188, 21:33-34, or “[a] textured region 156 can be coupled to the semiconductor 72 opposite the lens,” Haddad188, 24:32-33.

240. It would have been obvious to combine Iida and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

241. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein said textured region is coupled to the light incident surface.*

5. Claim 14: “The device of claim 13, wherein said light incident surface comprises said textured region.”

242. This limitation is obvious based on Iida in view of Haddad188.

243. Iida’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. The modification would entail the *light incident surface compris[ing] said textured region*, given that Haddad188 teaches that the “surface features” of the textured region can be formed directly in a semiconductor material.

244. Haddad188 discloses that “[v]arious aspects of the textured region can vary depending on the desired configuration of the device. In one aspect, however, the textured region includes surface features.... Numerous surface feature morphologies are contemplated, nonlimiting examples of which include cones, pillars, pyramids, microlenses, quantum dots, inverted features, and combinations thereof.” Haddad188, 2:18-23. Haddad188 discloses that these surface features of the textured region can be formed directly in a semiconductor material. Haddad188, 16:33-17:2 (“[T]he surface of the semiconductor material is chemically and/or structurally altered by the laser treatment, which may, in some aspects, result in the formation of surface features appearing as microstructures or patterned areas on the surface.”). Haddad188 further discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31.

245. It would have been obvious to combine Iida and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

246. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein said light incident surface comprises said textured region*.

6. Claim 15: “The device of claim 13, wherein said textured region comprises a textured film layer”

247. This limitation is obvious based on Iida in view of Haddad188.

248. Iida’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation using *a textured film layer*. Haddad188 discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31. Haddad188 further discloses that “[t]he textured region can be formed by various techniques, including lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, additional material deposition, and the like.” Haddad188, 15:20-29. Haddad188 further explains that “material can be removed to a thickness of about 20 μm ,” Haddad188, 15:25, which is in the ’359 patent’s suggested range of “1nm to 20 μm .” ’359 patent, 14:22-23. A POSITA would therefore understand that Haddad188’s textured region can be formed as a textured film layer through material deposition.

249. It would have been obvious to combine Iida and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

250. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein said textured region comprises a textured film layer*.

7. Claim 16: “The device of claim 15, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”

251. This limitation is obvious based on Iida in view of Haddad188.

252. Iida’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. Haddad188 discloses that “a passivation layer 22 ... is shown coupled to the side of the semiconductor substrate facing the incoming electromagnetic radiation, however a passivation layer can be located anywhere on the device and still be within the present scope.” Haddad188, 20:26-29, Fig.2. Further, “a textured region located at the point of entry of the electromagnetic radiation into the photosensitive device tends to bend the electromagnetic radiation, particularly the blue wavelengths. Accordingly, one level of tuning can be accomplished by locating the textured region on the surface adjacent the incident electromagnetic radiation.” Haddad188, 20:32-21:1. Taking these teachings together, a POSITA would have reason to make a textured film layer at the point of entry *compris[ing] silicon dioxide*, given its passivating quality.

253. Haddad188 further discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31. Haddad188 further discloses that “[a] variety of semiconductor materials are contemplated for use with [its] devices” and that the semiconductor material in which the textured region is formed “can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types.” Haddad188, 10:24-27. Accordingly, Haddad188 discloses a textured film layer comprising *any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof*.

254. A POSITA would seek a transparent material capable of texturing so as not to interfere with the reflective qualities of the layered pixel separation structure of Iida. Reviewing the groups of materials disclosed in Haddad188 at 10-11, a POSITA would have recognized amorphous silicon and multicrystalline silicon (also known as polysilicon), for example, as materials that may be readily textured and used in transparent applications, depending upon processing. As such, a POSITA would understand that Haddad188 would rely on such transparent materials for its textured regions, thereby making them obvious to try.

255. It would have been obvious to combine Iida and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

256. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein said textured region comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.*

8. Claim 17: “The device of claim 12, wherein said backside surface comprises said textured region.”

257. This limitation is obvious based on Iida in view of Haddad188.

258. Iida’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. The modification would entail the *backside surface compris[ing] a textured region*, given that “a textured region 90 is coupled to the semiconductor substrate 72 opposite the doped regions 74,76. Thus light entering from the direction of the doped regions passes through the semiconductor substrate prior to contacting the textured region. The textured region can be disposed across an entire surface of the semiconductor substrate, as is shown in FIG. 9, or it can be disposed on one or more discrete regions (not shown).” Haddad188, 23:9-14. Moreover, Haddad188 teaches that its textured regions can not only be coupled to the semiconductor substrate but can also be produced within the substrate. Haddad188, 16:3-5 (“One effective method of producing a textured region is through laser processing. Such laser processing allows discrete locations of the semiconductor substrate to be textured.”); 16:14-17 (“In one aspect, for example, a target region of

the semiconductor material can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Patents 7,057,256, 7,354,792, and 7,442,629, which are incorporated herein by reference in their entireties.”). Accordingly, a POSITA would have understood that the backside semiconductor substrate could have a textured region coupled thereto or have a textured region formed directly therein.

259. It would have been obvious to combine Iida and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

260. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein the backside surface comprises the textured region.*

9. Claim 19: “The device of claim 18, wherein at least one of said light incident surface and said backside surface of at least one of said two adjacent light sensitive pixels comprises a textured region.”

261. This limitation is obvious based on Iida in view of Haddad188.

262. As discussed above regarding claims 13 and 14, Iida in view of Haddad188 renders obvious the device of claims 1 and 18 wherein the *light incident surface comprises a textured region.*

263. As discussed above regarding claim 17, Iida in view of Haddad188 renders obvious the device of claims 1 and 18 wherein the *backside surface comprises a textured region.*

10. Claim 20: “The device of claim 19, wherein said textured region is a textured film layer.”

264. This limitation is obvious based on Iida in view of Haddad188.

265. See discussion of claim 15.

11. Claim 21: “The device of claim 20, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”

266. This limitation is obvious based on Iida in view of Haddad188.

267. See discussion of claim 16.

12. Claim 22: “The device of claim 19, wherein said textured region reflects at least a portion of light internally incident thereon into the at least one pixel.”

268. This limitation is obvious based on Iida in view of Haddad188.

269. Iida’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. The modification would provide a *textured region* that *reflects at least a portion of light internally incident thereon into the at least one pixel*, given that Haddad188 discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31. Haddad188 also discloses that, “[a]s is shown in FIG. 13, the textured region 130 can have a nonparallel [i.e., non-uniform] surface with respect to the semiconductor substrate 72 as has been described. This nonparallel morphology, when included with the deep trench isolation 120, can effectively focus

electromagnetic radiation into the semiconductor substrate from multiple sides.”

Haddad188, 24:11-15. Haddad188 further discloses that its textured regions achieve “internal reflection” of “incident electromagnetic radiation” to “allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device.” Haddad188, 15:14–18.

270. It would have been obvious to combine Iida and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

271. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein the textured region reflects at least a portion of light internally incident thereon into the pixel.*

13. Claim 26: “The device of claim 19, wherein the textured region is formed by laser radiation.”

272. This limitation is obvious based on Iida in view of Haddad188.

273. Iida’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. The modification would entail forming the *textured region* using *laser radiation*, given that Haddad188 discloses that “[o]ne effective method of producing a textured region is through laser processing. Such laser processing allows discrete locations of the semiconductor substrate to be textured. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope.” Haddad188, 16:3-7; 16:14-19 (“[A] surface of a semiconductor

material is irradiated with laser radiation to form a textured or surface modified region.”). Haddad188 further discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31. A POSITA would know that laser provides excellent control of the surface profile and may be programmed to offer optical performance that exceeds simple wet and dry etching of surfaces, especially when texturing is being implemented. A POSITA would have been familiar with using laser radiation as a normal processing fabrication tool.

274. It would have been obvious to combine Iida and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

275. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein the textured region is formed by laser radiation*.

14. Claim 27: “The device of claim 12, wherein the textured region is formed by one of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.”

276. This limitation is obvious based on Iida in view of Haddad188.

277. As discussed above regarding claim 12, Iida in view of Haddad188 renders obvious an imager device with a textured region. Modifying Iida’s imaging device according to Haddad188’s processing would satisfy this limitation. Haddad188

discloses that “[a]dditionally, the textured region can be formed by a variety of processes. Nonlimiting examples of such texturing processes can include lazing [i.e., lasing or laser processing],⁹ chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, and combinations thereof.” Haddad188, 2:18-27; *see also* Haddad188, 16:3-13.

278. It would have been obvious to combine Iida and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

279. Accordingly, it would have been obvious for a POSITA to make an imager device *wherein the textured region is formed by one of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.*

15. Claim 28: “The device of claim 12, wherein the textured region is formed by laser radiation.”

280. This limitation is obvious based on Iida in view of Haddad188.

281. See discussion of claim 26.

⁹ Haddad188 explains that “[o]ne effective method of producing a textured region is through laser processing” or “[l]aser treatment.” Haddad188, 16:3-4.

16. Claim 29: “The device of claim 12, wherein said textured region is coupled to the backside surface.”

282. This limitation is obvious based on Iida in view of Haddad188.

283. See discussion of claim 17.

17. Claim 76: “The imager device of claim 1, wherein the peripheral isolation element comprises a textured region.”

284. This limitation is obvious based on Iida in view of Haddad188.

285. As discussed above regarding limitation 1[b], Iida discloses a peripheral isolation element 160B at least partially separating said two adjacent light sensitive pixels. Iida [0081]. Iida’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. As discussed above, the modification would entail locating *a textured region* along the *peripheral isolation element*, given that Haddad188 discloses that “FIG. 3 shows a photosensitive device having textured regions 30 located on the sides of the semiconductor substrate 12. Such a configuration allows electromagnetic radiation normally exiting through the sides of the device to be further defused [diffused] and absorbed within semiconductor substrate. The textured region(s) can be located on one or more sides to facilitate the enhanced absorption.” Haddad188, 21:12-16; *see also* Haddad188, 22:21-29, 24:1-15. Haddad188 also discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb

electromagnetic radiation, thus increasing the quantum efficiency of the device.”

Haddad188, 14:29-31.

286. It would have been obvious to combine Iida and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

287. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein the peripheral isolation element comprises a textured region*.

18. Claim 77: “The imager device of claim 1, wherein the peripheral isolation element further comprises a first textured region between the first layer and one of said adjacent pixels and a second textured region between the second layer and the other one of said adjacent pixels.”

288. This limitation is obvious based on Iida in view of Haddad188.

289. As discussed above regarding limitation 1[b], Iida discloses a trench-type peripheral isolation element separating said two adjacent light sensitive pixels. Iida, [0081]. Haddad188 discloses that “[t]rench isolation can include dielectric materials, reflective materials, conductive materials, and combinations thereof, including textured regions and other light diffusing features. Thus, the trench isolation layer can be configured to reflect incident electromagnetic radiation, in some cases until it is absorbed, thereby increasing the effective absorption length of the device.” Haddad188, 24:5-9. Haddad188 further discloses that “FIG. 3 shows a photosensitive device having textured regions 30 located on the sides of the semiconductor substrate 12. Such a configuration allows electromagnetic radiation

normally exiting through the sides of the device to be further defused [diffused] and absorbed within semiconductor substrate. The textured region(s) can be located on one or more sides to facilitate the enhanced absorption.” Haddad188, 21:12-16.

290. Haddad188 further discloses providing a textured region between a pixel and reflective and passivation layers. Haddad188, 20:19-29 (“Thus, as is shown in FIG. 2, electromagnetic radiation passing through the semiconductor substrate and the textured region 16 can be reflected back [by reflecting layer 20] into the semiconductor substrate. Additionally, a passivation layer 22 can be coupled to the substrate. ... [A] passivation layer can be located anywhere on the device and still be within the present scope.”), Fig 2 (reproduced below).

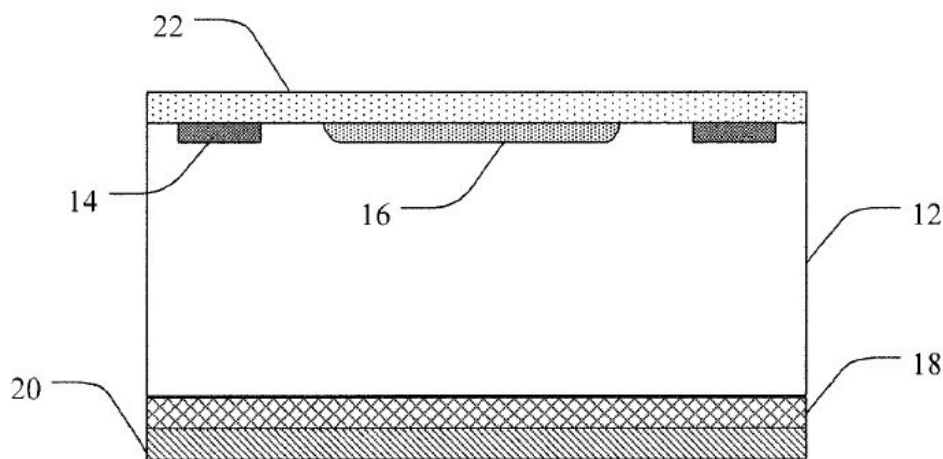
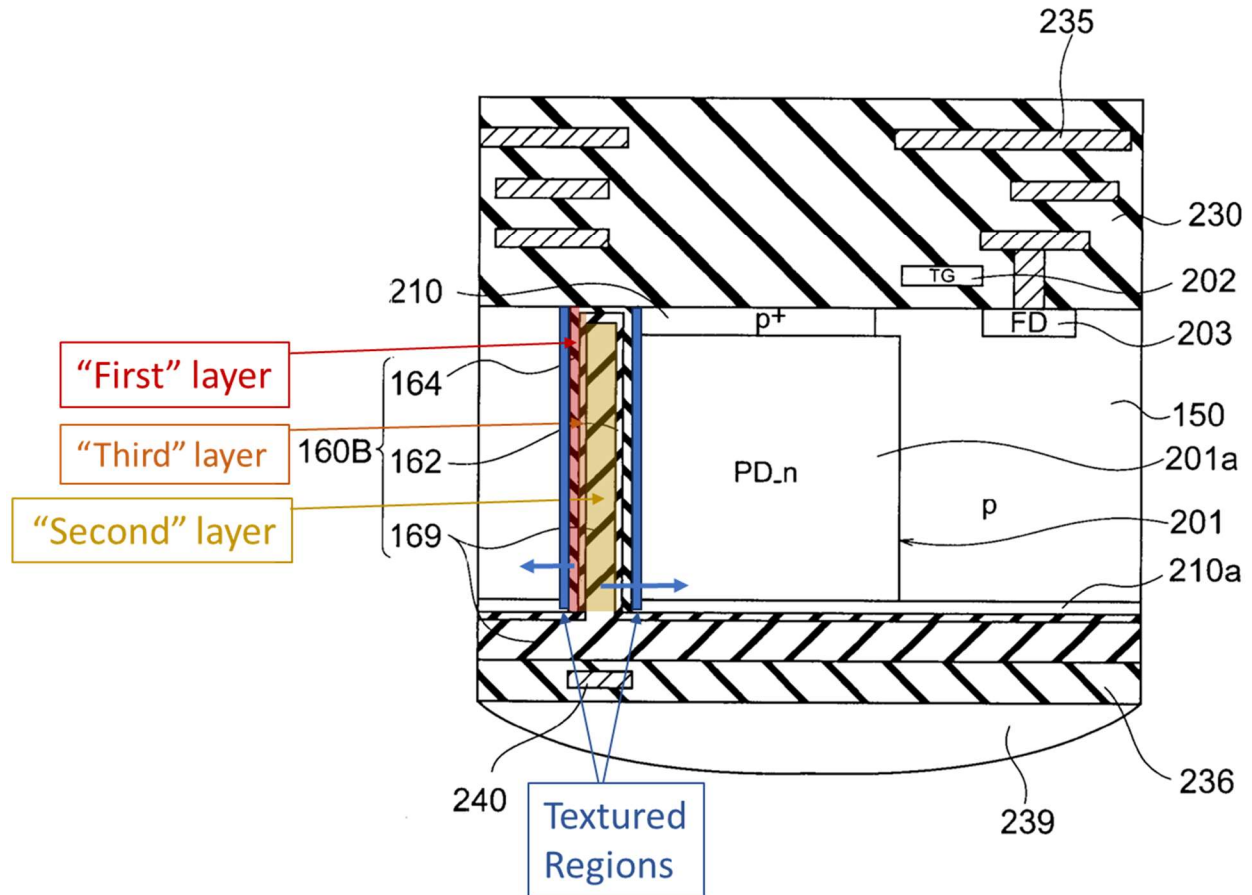


FIG. 2

291. As discussed above regarding limitation 1[e], Iida depicts in Figure 10 a silicon oxide layer 164 (*first layer*), a hafnium oxide film 162 (*third layer*), and a low refractive index film 169 (*second layer*). Iida, Fig. 10, [0099]. Iida further describes the importance of the variation in the refractive indices of these materials. *See* Iida, [0100] (“[T]he low refractive index material should preferably be a material having a lower refractive index than the refractive index of hafnium oxide, which is 2.0.”). Because the interfaces formed between these three layers of different refractive indices is an important characteristic of the quality of the isolation, it would be logical for a POSITA to put the textured region in between the outermost layer of the peripheral isolation element and the adjacent pixel to improve isolation. Haddad188 further discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31.

292. Adding a textured region on either side of Iida’s pixel separation structure, following the teaching of Haddad188’s Figure 2, is consistent with both references’ objective of increasing absorption of electromagnetic radiation and minimizing optical crosstalk.



Iida, Fig. 10 (annotated and modified).

293. It would have been obvious to combine Iida and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

294. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein the peripheral isolation element further comprises a first textured region between the first layer and one of said adjacent pixels and a second textured region between the second layer and the other one of said adjacent pixels.*

19. Claim 78: “The imager device of claim 18, wherein the peripheral isolation element comprises a textured region.”

295. This limitation is obvious based on Iida in view of Haddad188.

296. See discussion of claim 76.

20. Claim 79: “The imager device of claim 18, wherein the peripheral isolation element further comprises a first textured region between the first layer and one of said adjacent pixels and a second textured region between the second layer and the other one of said adjacent pixels.”

297. This limitation is obvious based on Iida in view of Haddad188.

298. See discussion of claim 77.

C. Ground 3: Claims 6, 9, 24, 30, 32, 34, and 36 Are Obvious Based on Iida and Shinohara

1. Overview of Shinohara

299. I understand that Shinohara is prior art because it was published on February 9, 2012, before the '359 patent's provisional application filing date of March 22, 2012.

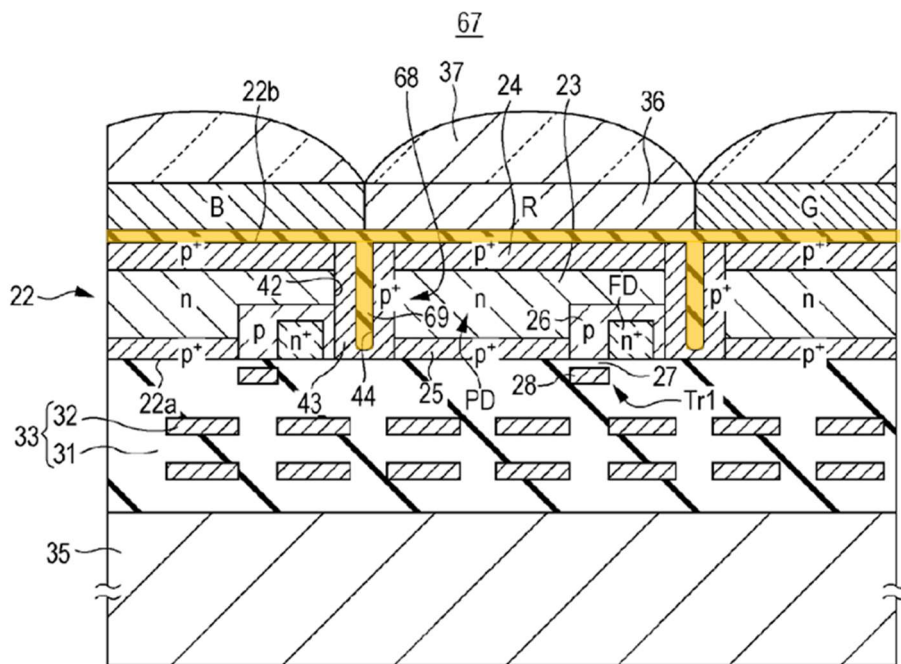
300. Shinohara was not listed in any IDS and was not discussed during prosecution of the '359 patent.¹⁰

301. Like the '359 patent, Shinohara is directed to light-sensitive pixels in imaging devices with pixel separation structures. Shinohara, Abstract (“A solid state

¹⁰ The patent that issued from Shinohara (U.S. Patent No. 8,749,679) also was not discussed during prosecution.

imaging device having a backside illuminated structure, includes: a pixel region in which pixels each having a plurality of pixel transistors are arranged in a two-dimensional matrix; an element isolation region isolating the pixels which is provided in the pixel region and which includes a semiconductor layer provided in a trench by an epitaxial growth; and a light receiving surface at a rear surface side of a semiconductor substrate which is opposite to a multilayer wiring layer.”). Like the '359 patent, Shinohara describes “an element isolation region for isolating pixels from each other.” Shinohara, [0006]. Shinohara also describes how “leakage of photoelectrically converted charge into an adjacent pixel can be prevented.” Shinohara, [0021].

302. An exemplary embodiment from Shinohara is depicted below.



Shinohara, Fig. 9A (annotated).

303. Shinohara's Figure 9A is a schematic structural view showing a section of a solid-state imaging device. Shinohara, [0032]. "As shown in FIG. 9A, the insulating film 69 can be formed over the entire surface containing the photodiode PD of the surface 22 a as well as in the void 44." Shinohara, [0090]. Shinohara teaches that using an insulating film having a negative fixed charge enhances the passivation characteristics of the element isolation region. Shinohara, [0095]. Accordingly, Shinohara discloses using "a film of hafnium dioxide (HfO_2), dialuminum trioxide (Al_2O_3), ditantalum pentaoxide (Ta_2O_5), dilanthanum trioxide (La_2O_3), or diyttrium trioxide (Y_2O_3)" as insulating film 69. Shinohara, [0091].

2. Motivation to Combine Iida and Shinohara

304. It would have been obvious to combine Iida and Shinohara.

305. A POSITA would have been motivated to select from Shinohara's insulating film materials to fill Iida's pixel separation structure. Shinohara notes a known method in which "an element isolation region which physically isolates pixels is formed by a trench method in a rear surface of a substrate so as to suppress leakage of charge into an adjacent pixel." Shinohara, [0011]. This leakage of charge results in a decrease in sensitivity of the pixel. Shinohara, [0012]. Accordingly, Shinohara teaches manufacturing a solid-state imaging device by "forming a trench having a predetermined depth in a semiconductor substrate from a surface thereof; and filling a

semiconductor layer in the trench by an epitaxial growth to form an element isolation region.” Shinohara, [0017].

306. For example, while Iida discloses a pixel separation structure 160B “in which silicon oxide layer 164, a fixed charge film 162, and a film 169 made of a low refractive index material are buried in a trench,” Iida, [0099], it does not specify a particular material for film 169. A POSITA would have considered Shinohara to identify suitable materials to use for Iida’s film 169.

307. For example, Shinohara teaches that an insulating film having a negative fixed charge can comprise materials such as “dialuminum trioxide (Al_2O_3).” Shinohara, [0091]. Al_2O_3 has a refractive index of 1.76 (*see* Ex-1018 at B-68)—the lowest of Shinohara’s options—and thus would be at least an obvious candidate for POSITAs to try for Iida’s low refractive index film 169. *See* Iida, [100] (“[T]he low refractive index should preferably be a material having a lower refractive index than the refractive index of hafnium oxide, which is 2.0, so as to improve the efficiency”).

308. Additionally, while Iida teaches that its negative fixed charge film 162 may be an “oxide dielectric film containing at least one element selected from the group consisting of hafnium (Hf), zirconium (Zr), and titanium (Ti) ... for example,” Iida, [0050], POSITAs would have recognized that other suitable materials may be

used, such as those taught in Shinohara, having their own respective benefits and considerations.

309. For example, POSITAs would consider using Shinohara's Al_2O_3 for Iida's negative fixed charge film 162 because, like hafnium oxide (*see* Iida, [0051]), aluminum oxide exhibits low surface velocity recombination. Ex-1010 at 2-3; *see also* '359 patent, 9:54-65. Moreover, a POSITA would also have known that aluminum oxide offers comparable interface-trap density mitigation, such that aluminum oxide would provide high-quality chemical passivation. Iida discloses forming a photodiode in a p-type silicon substrate. Iida, [0049]. Forming the pixel isolation trench results in an exposed surface of the p-type substrate. Iida discloses depositing a silicon oxide layer 164 "along the side faces and the bottom face of the trench." Iida, [0050] ("A silicon oxide layer 164 of an extremely small thickness equivalent to several atomic layers is provided between the fixed charge film 162 and the trench."). However, "the dark current generated from the interface state between Si and SiO_2 existing in the sidewalls of the trench separation structures generates large noises, and causes the S/N ratio to rapidly deteriorate." Iida, [0007]. Surface recombination contributes to dark current, which reduces image quality. POSITAs would seek to minimize surface recombination velocity along the side faces and the bottom face of the trench so that converted charge is retained longer in the silicon substrate for collection. Depositing Shinohara's Al_2O_3 in place of Iida's negative fixed charge film 162 would provide a

surface velocity recombination of about 10 cm/s, Ex-1010 at 2-3, thus improving the image quality of Iida's imager device.

310. Further, Shinohara teaches that an insulating film having a negative fixed charge can comprise materials such as "ditantalum pentaoxide (Ta_2O_5) [or] dilanthanum trioxide (La_2O_3)." Shinohara, [0091]. Ta_2O_5 has a refractive index of 2.11 (Ex-1020 at 9758; Ex-1021 at 46) and thus would offer greater reflectivity than Iida's hafnium oxide. Similarly, La_2O_3 is a high refractive index material with low dispersion frequently used in manufacturing high-quality camera and telescope lenses; it too would offer a high degree of reflectivity. Both are also negative fixed charge films like hafnium oxide, which is disclosed as Iida's negative fixed charge film 162. Iida, [0051].

311. Iida and Shinohara are directed to the same field of endeavor: semiconductor image sensors. Iida, [0044]; Shinohara, [0051]. Furthermore, Iida and Shinohara are specifically directed to placing trench isolation structures between adjacent pixels to reduce crosstalk. Iida, [0057] ("As described above, according to this embodiment, the pixel separation structure 160 performs pixel separations. Accordingly, a solid-state imaging device that has less optical crosstalk and less electrical crosstalk can be obtained."); Shinohara, [0021] ("[S]ince the semiconductor layer in the trench by an epitaxial growth functions as a pinning layer, the generation of white spots and dark current in the element isolation region can be

suppressed. Since the isolation power of the element isolation region is enhanced, the leakage of photoelectrically converted charge into an adjacent pixel can be prevented.”), [0090] (“[A]n element isolation region 68 for isolating pixels is formed such that the p-type semiconductor layer 43 is provided in the trench 42 by an epitaxial growth, and an insulating film 69 is filled in the void 44 inside this p-type semiconductor layer 43.”).

312. In addition to performance benefits, Shinohara’s disclosed process purports to yield a more efficient manufacturing process. Shinohara, [0093], [0096] (referencing [0088]-[0089]). Like Shinohara, Iida considers the fabrication and processing of a pixel separation structure. Specifically, Iida notes that “by filling the trench with a low refractive index material following a thin hafnium oxide film in a high-throughput procedure, the structure can be realized.” Iida, [0109]. Whether to use the materials identified in Shinohara for the insulating film (*see* Shinohara, [0091]) in Iida’s pixel separation structure would have depended on the particular design needs and manufacturing considerations to achieve the desired improvements in electrical and optical crosstalk.

313. Further, building an Iida imager device using the trench isolation structures and materials described in Shinohara (e.g., insulating film 69) would have been nothing more than a simple design choice. As Shinohara teaches, a POSITA understood that “it is important to suppress the occurrence of color mixture caused by

leakage of charge (such as electron) photoelectrically converted in the vicinity of the rear surface side into an adjacent pixel.” Shinohara, [0008]. “[S]ince the filled insulated film 69 has a refractive index different from that of the p-type semiconductor layer 43, even if inclined incident light is incident thereon, the light is not photoelectrically converted in an adjacent pixel after passing through the element isolation region 68.” Shinohara, [0094]. A POSITA would have looked to Shinohara’s insulating film 69 to identify a material for Iida’s pixel separation structure “to improve the efficiency of the antireflective structure on the light incident side and achieve higher sensitivity.” Iida, [0100]. In view of these recognized needs and similarity in structure and function of the isolation trenches in Iida and Shinohara, a POSITA would have been motivated to look to Shinohara’s alternative designs for trench isolation materials.

314. A POSITA would have had a reasonable expectation of success. It would have been well within the abilities of a POSITA to use the materials described in Shinohara for Iida’s device. It would have involved routine manufacturing steps that Iida had already used in its device with predictable results. In particular, the fabrication process techniques used would involve standard modules, standard techniques, and standard processes. The fabrication of trench layers, including those with silicon materials and dielectrics, would have been well-known to a POSITA, as would the characteristic properties of the materials, such as optical refractive index, etch rates, and crystal quality. Fabrication processing techniques, including

photolithography, etching deposition, and metallization, existed well before the relevant period.

3. Claim 6: “The device of claim 1, wherein at least one of the first and second layer comprises Al_2O_3 .”

315. This limitation is obvious based on Iida in view of Shinohara.

316. As explained above, it would have been obvious in light of Shinohara to use Al_2O_3 for Iida’s low refractive index film 169 (*second layer*).

317. Accordingly, it would have been obvious to a POSITA to build an imager device wherein *the second layer comprises Al_2O_3* .

4. Claim 9: “The device of claim 1, wherein said peripheral isolation element exhibits a surface recombination velocity as low as 10 cm/s.”

318. This limitation is obvious based on Iida in view of Shinohara.

319. As explained above, it would have been obvious in light of Shinohara to use Al_2O_3 for Iida’s negative fixed charge film 162 (*third layer*). Further, POSITAs would seek to lower the surface recombination velocity at the wall of Iida’s *peripheral isolation element* 160B to ensure that the accumulated charge can be collected before it recombines. To this end, POSITAs would be aware that an aluminum oxide negative fixed charge film 162 (*third layer*) would *exhibit a surface recombination velocity as low as 10 cm/s*. Ex-1010 at 2-3 *see also* ’359 patent, 9:58-60 (“Low surface recombination velocities, as low as 10 cm/s can be obtained through various deposition processes of Al_2O_3 layers on the silicon substrate”).

320. Accordingly, it would have been obvious to a POSITA to build an imager device *wherein said peripheral isolation element exhibits a surface recombination velocity as low as 10 cm/s.*

5. Claim 24: “The device of claim 18, wherein said at least two materials comprises silicon dioxide and aluminum oxide.”

321. This limitation is obvious based on Iida in view of Shinohara.

322. As discussed above regarding claim 3, Iida’s disclosure of silicon oxide layer 164 (*first layer*) teaches a layer of *silicon dioxide* in pixel separation structure 160B.

323. As explained above, it would have been obvious in light of Shinohara to use Al_2O_3 for Iida’s low refractive index film 169 (*second layer*). A POSITA would understand that dialuminum trioxide (Al_2O_3) is *aluminum oxide* and would use these terms interchangeably. *See* Ex-1018 at B-68 (defining formula of “aluminum oxide” as “ Al_2O_3 ”).

324. It would have been obvious to combine Iida and Shinohara, with a reasonable expectation of success, as discussed in Section VII.C.2 above.

325. Accordingly, it would have been obvious for a POSITA to make an imager device *wherein said at least two materials comprise silicon dioxide and aluminum oxide.*

6. Claim 30: “The device of claim 1, wherein said peripheral isolation element comprises tantalum oxide.”

326. This limitation is obvious based on Iida in view of Shinohara.

327. As explained above, it would have been obvious in light of Shinohara to use Ta₂O₅ for Iida’s negative fixed charge film 162 (*third layer*). A POSITA would understand that ditantalum pentaoxide (Ta₂O₅) is *tantalum oxide* and would use these terms interchangeably. *See* Ex-1018 at B-136 (defining formula of “tantalum oxide” as “Ta₂O₅”).

328. It would have been obvious to combine Iida and Shinohara, with a reasonable expectation of success, as discussed in Section VII.C.2 above.

329. Accordingly, it would have been obvious for a POSITA to make an imager device *wherein said peripheral isolation element comprises tantalum oxide*.

7. Claim 32: “The device of claim 1, wherein said peripheral isolation element comprises lanthanum oxide.”

330. This limitation is obvious based on Iida in view of Shinohara.

331. As explained above, it would have been obvious in light of Shinohara to use La₂O₃ for Iida’s negative fixed charge film 162 (*third layer*). A POSITA would understand that dilanthanum trioxide (La₂O₃) is *lanthanum oxide* and would use these terms interchangeably. *See* Ex-1018 at B-98-99 (defining formula of “lanthanum oxide” as “La₂O₃”).

332. It would have been obvious to combine Iida and Shinohara, with a reasonable expectation of success, as discussed in Section VII.C.2 above.

333. Accordingly, it would have been obvious for a POSITA to make an imager device *wherein said peripheral isolation element comprises lanthanum oxide*.

8. Claim 34: “The device of claim 18, wherein said peripheral isolation element comprises tantalum oxide.”

334. This limitation is obvious based on Iida in view of Shinohara.

335. See discussion of claim 30.

9. Claim 36: “The device of claim 18, wherein said peripheral isolation element comprises lanthanum oxide.”

336. This limitation is obvious based on Iida in view of Shinohara.

337. See discussion of claim 32.

D. Ground 4: Claims 44, 51, 65-66, and 71-72 Are Obvious Based on Iida and Roy

1. Overview of Roy

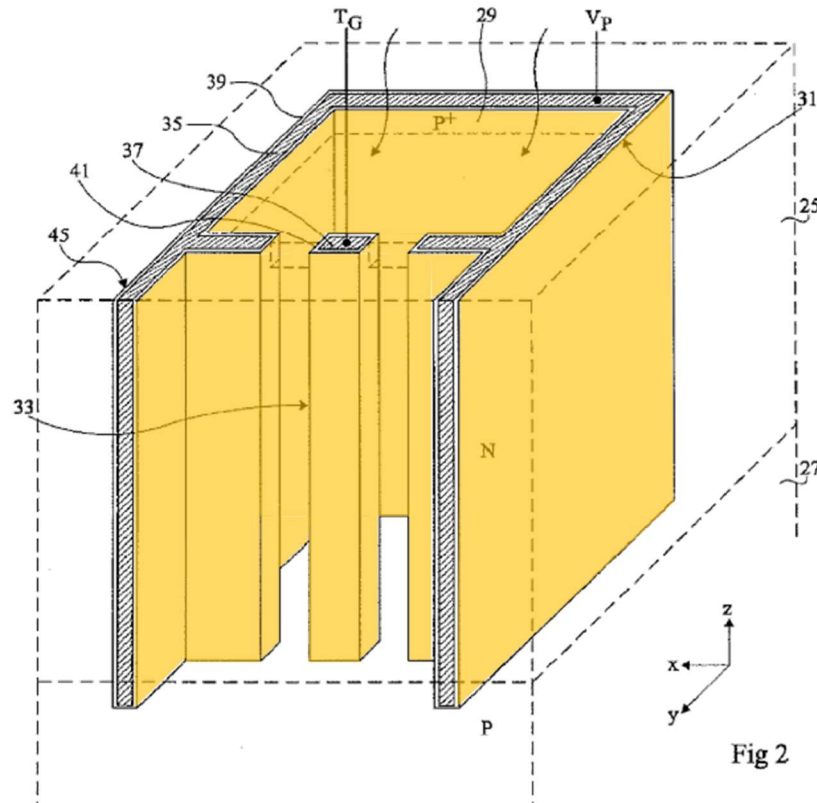
338. I understand that Roy is prior art because it was published on October 29, 2009, before the '359 patent's provisional application filing date of March 22, 2012.

339. Roy was not cited in any IDS and was not discussed during prosecution of the '359 patent.¹¹

340. Like the '359 patent, Roy is directed to light-sensitive pixels in imaging devices with pixel separation structures. Roy, Abstract (“An image sensor formed in a semiconductor stack of a lower region of a first conductivity type and of an upper region of a second conductivity type, including: a photodiode formed of a first portion of the stack...”). Roy refers to a “photodiode [that] is delimited by an enclosure comprising a trench.” Roy, [0050].

341. An exemplary embodiment from Roy is depicted below:

¹¹ The patent that issued from Roy (U.S. Patent No. 8,193,479) also was not discussed during prosecution.



Roy, Fig. 2 (annotated).

342. Roy's Figure 2 is a perspective view of a photodiode associated with a charge transfer system of an image sensor. Roy, [0029]. Among other things, Roy's Figure 2 depicts trenches 31 and 45 and column 33 that may have varying widths, and thin insulating films 39 and 41. Roy, [0050], [0057].

2. Motivation to Combine Iida and Roy

343. It would have been obvious to combine Iida and Roy. More specifically, a POSITA would have been motivated to apply Roy's teachings regarding dimensions of pixel separation structures to Iida's imaging device and would have had a reasonable expectation of success in doing so.

344. POSITAs were concerned with “decreas[ing] the size of image sensor pixels” to decrease volume constraints, Roy, [0007], and as products were becoming smaller, there was “a need for an image sensor comprising pixels of small dimensions,” Roy, [0011]. Indeed, Roy discloses a device in which “[h]eavily-doped P-ptype area 29 may have dimensions approximately equal to 1 x 1 μm .” Roy, [0057]. A POSITA would have recognized that smaller image sensors are particularly beneficial for mobile applications such as smartphones and other hand-held electronics because limited space must be shared between all components of the device (such as batteries, displays, antennas, and processing units, among others). Indeed, miniaturization has been a common goal and metric for consumer products for the past thirty to forty years.

345. With regard to sizing of image sensor pixels, Iida describes a “known ... trade-off relationship between the width and depth of each pixel separation structure” and crosstalk-related “problem[s]” associated with “increase[s] in pixel separation width” or “decrease[s] in the depth of each pixel separation structure.” Iida, [0009]-[0010] (describing how relatively shallow pixel separation structures result in greater “electrical crosstalk” and how relatively wide pixel separation structures cause a problematic relative “decrease in the volume of each photodiode”). To limit such problems, Iida teaches forming pixel separation structures that are relatively small but also relatively deep. *See* Iida, [0022]-[0023] (“[I]t is essential to

... reduce optical crosstalk and electrical crosstalk. To do so, pixel separation structures that can be formed in a very small size and can be formed at sufficiently deep locations are needed, so as not to compress the volumes of photodiodes.”), [0138] (teaching benefits of “pixel separation structures and photodiodes each having such a depth as to absorb a sufficient amount of incident light of ‘red’ or long wavelengths”).

346. Despite thus teaching that the dimensions of pixel separation structures are important design features, Iida only indicates a design in which “pixel pitch is reduced to approximately 1 μm ,” Iida, [0020], but does not expressly disclose dimensions of separation structures for any of the embodiments of its invention. Accordingly, a POSITA seeking to implement Iida’s imaging device would be motivated to look elsewhere for guidance for selecting the dimensions of the device’s pixel separation structures.

347. A POSITA would look to Roy for this purpose. Roy notes that the pixel dimensions of prior art imaging devices were “not optimized,” Roy, [0009]; notes, like Iida, the need to design such devices with “pixels of small dimensions and high storage capacities” with “insulation enabling limiting crosstalk,” Roy, [0011], [0012-0015]; and teaches pixel separation structure dimensions that achieve such objectives, Roy, [0057] (teaching specific depth and width ranges), [0045] (teaching that invention achieves “an image sensor having reduced dimensions ... with a low

crosstalk, with a low dark current, and enabling efficient transfer of the electrons”), [0053], [0069] (teaching that invention enables “photodiodes of very small dimensions having a significant electron accumulation capacity”).

348. A POSITA would have had a reasonable expectation of success in combining Iida and Roy in this manner. Both Iida and Roy are directed to imaging devices comprising light-sensitive pixels with similar scale, and more specifically to the design of trench isolation structures placed between adjacent pixels for reducing crosstalk. *See* Iida, Abstract, [0020]; Roy, Abstract, [0057]. Given the similarities in structure, scale, and function of the image sensors and pixel separation structures taught by Iida and Roy, building Iida’s imager device using the pixel isolation structure dimensions taught by Roy would have been a simple design choice for applying a known technique to yield a predictable result.

349. It would have been well within a POSITA’s abilities to use the dimensions taught by Roy in forming the pixel separation structures in Iida’s device; indeed, it would have involved routine manufacturing steps that both Iida and Roy disclose. *See, e.g.*, Iida, [0109] (“[B]y filling the trench with a low refractive index material following a thin hafnium oxide film in a high-throughput procedure, the structure of this embodiment can be realized”); Roy, [0082] (“forming, in trench(es) 31/45 in and column(s) 33, thin insulating layers 39 and 41, followed by polysilicon 35 and 37”). Roy also teaches that its pixel separation structure dimensions increase

“manufacturing simplicity,” Roy, [0079], further motivating a POSITA to use them for Iida’s device and further reinforcing a POSITA’s expectation of success. In particular, the fabrication process techniques used would involve standard modules, standard techniques, and standard processes. The fabrication of trench layers, including those with silicon materials and dielectrics, would have been well-known to a POSITA, as would the characteristic properties of the materials, such as optical refractive index, etch rates, and crystal quality. Fabrication processing techniques, including photolithography, etching deposition, and metallization, existed well before the relevant period.

3. Claim 44: “The device of claim 1, wherein said peripheral isolation element has a width in a range from about 100 nm to about 50 microns.”

350. This limitation is obvious based on Iida in view of Roy.

351. As discussed above regarding claim 1, Iida discloses a peripheral isolation element. Roy discloses that its trench 31/45 and column 33 “may have a width of approximately 0.2 μm and be separated, at the level of the interruption area of trench 31, by a distance approximately equal to 0.2 μm ,” i.e., 200 nm. Roy, [0057].

352. It would have been obvious to combine Iida and Roy, with a reasonable expectation of success, as discussed in Section VII.D.2 above.

353. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein the peripheral isolation element has a width in a range from about 100 nm to 50 microns.*

4. Claim 51: “The device of claim 18, wherein said peripheral isolation element has a width in a range from about 100 nm to about 50 microns.”

354. This limitation is obvious based on Iida in view of Roy.

355. See discussion of claim 44.

5. Claim 65: “The imager device of claim 64, wherein said trench isolation element has a depth in a range of about 100 nm to about 50 microns.”

356. This limitation is obvious based on Iida in view of Roy.

357. As discussed above regarding claim 64, Iida discloses a trench isolation element. Roy discloses that “[a]ccording to an embodiment, the trench and the column have depths ranging between 1 and 10 μm , the conductive material in the trench and in the column is polysilicon, and the material forming the insulated walls of the column and of the trench is selected from the group comprising silicon oxide, silicon nitride, silicon oxynitride, or is formed of a multiple-layer stack of these materials.” Roy [0020].

358. It would have been obvious to combine Iida and Roy, with a reasonable expectation of success, as discussed in Section VII.D.2 above.

359. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein said trench isolation element has a depth in a range of about 100 nm to 50 microns.*

6. Claim 66: “The imager device of claim 65, wherein said trench isolation element has a width in a range of about 100 nm to about 10 microns.”

360. This limitation is obvious based on Iida in view of Roy.

361. As discussed above regarding claim 65, Iida discloses a trench isolation element. Roy discloses that “[t]rench 31/45 and column 33 may have a width of approximately 0.2 μ m and be separated, at the level of the interruption area of trench 31, by a distance approximately equal to 0.2 μ m,” i.e., 200 nm. Roy, [0057].

362. It would have been obvious to combine Iida and Roy, with a reasonable expectation of success, as discussed in Section VII.D.2 above.

363. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein said trench isolation element has a width in a range of about 100 nm to 10 microns.*

7. Claim 71: “The imager device of claim 70, wherein said trench isolation element has a depth in a range of about 100 nm to about 50 microns.”

364. This limitation is obvious based on Iida in view of Roy.

365. See discussion of claim 65.

8. Claim 72: “The imager device of claim 71, wherein said trench isolation element has a width in a range of about 100 nm to about 10 microns.”

366. This limitation is obvious based on Iida in view of Roy.

367. See discussion of claim 66.

VIII. CONCLUSION

368. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on November 29, 2024

Respectfully submitted,



Michael Lebby