(12) 特許協力条約に基づいて公開された国際出願

(19) 世界知的所有権機関
国際事務局

(43) 国際公開日
2008 年8 月21 日 (21.08.2008)

PCT

(10) 国際公開番号
WO 2008/099524 A1

(51) 国際特許分類:
H01L 31/04 (2006.01)

(21) 国際出願番号: PCT/JP2007/065386

(22) 国際出願日: 2007 年8 月6 日 (06.08.2007)

(25) 国際出願の言語: 日本語

(26) 国際公開の言語: 日本語

(30) 優先権データ:
特願2007-036432 2007 年2 月16 日 (16.02.2007) JP

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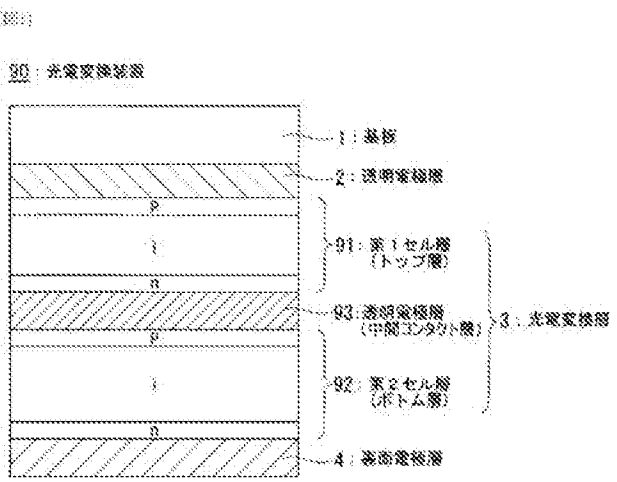
(54) Title: PHOTOELECTRIC CONVERTER AND METHOD FOR FABRICATING THE SAME

(54) 発明の名称: 光電変換装置及びその製造方法



90 PHOTOELECTRIC CONVERTER
1 SUBSTRATE
2 TRANSPARENT ELECTRODE LAYER
3 PHOTOELECTRIC CONVERSION LAYER
91 FIRST CELL LAYER (TOP LAYER)
92 SECOND CELL LAYER (BOTTOM LAYER)
93 TRANSPARENT ELECTRODE LAYER (INTERMEDIATE CONTACT LAYER)
4 BACKSIDE ELECTRODE LAYER

(57) **Abstract:** A photoelectric converter satisfying both high photoelectric conversion efficiency and high productivity, and its fabrication method. The photoelectric converter (90) has a substrate with a transparent electrode where a transparent electrode layer (2) is provided on a transparent insulating substrate (1), and at least a photoelectric conversion layer (92) principally comprising a crystalline silicon based semiconductor and a backside electrode layer (4) that are formed sequentially on the transparent electrode layer (2) side of the substrate with a transparent electrode. The transparent electrode layer (2) on the substrate with a transparent electrode has a surface shape where large and small protrusions and recesses coexist and spectral haze rate is 20% or above at the wavelength of 550-800 nm. The photoelectric conversion layer principally comprising the crystalline silicon based semiconductor has a film thickness of 1.2-2 μm, and a Raman ratio of 3.0-8.0.

(57) 要約: 高い光電変換効率と高い生産性を両立した光電変換装置及びその製造方法を提供することを目的とする。透明絶縁性の基板１上に透明電極層２を設けてなる透明電極付き基板と、該透明電極付き基板の透明電極層２側に順次形成された、結晶質シリコン系半導体を主として有する光電変換層９２ならびに裏面電極層４とを少なくとも有してなる光電変換装置であって、前記透明電極付き基板の透明電極層２表面が、大小の凹凸が混在した形状であり、かつ分光ヘイズ率が５５０ｎｍ以上８００ｎｍ以下の波長で２０％以上であり、前記結晶質シリコン系半導体を主として有する光電変換層の膜厚が１．２μｍ以上２μｍ以下、かつラマン比が３．０以上８．０以下である光電変換装置９０を提供する。

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(81) 指定国 (表示のない限り、全ての種類の国内保護が可能): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) 指定国 (表示のない限り、全ての種類の広域保護が可能): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), ユーラシア (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), ヨーロッパ (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

添付公開書類:
— 国際調査報告書

明 細 書

光電変換装置及びその製造方法

技術分野

[0001] 本発明は、光電変換装置及びその製造方法に関し、特に発電層としてシリコンを用いる薄膜シリコン積層型太陽電池に関するものである。

背景技術

[0002] 従来より、太陽電池等の光電変換装置として、シリコン系薄膜光電変換装置が知られている。この光電変換装置は、一般に、基板上に、第1透明電極、シリコン系半導体層(光電変換層)、第2透明電極及び裏面電極膜を順次積層したものである。半導体層はp型、i型及びn型の半導体材料によって形成されるpin接合を有している。光電変換装置が太陽電池である場合においてはこのpin接合がエネルギー変換部となって、太陽光の光エネルギーを電気エネルギーに変換する。このように、光電変換層が1層の光電変換装置の構造は、シングル構造と呼ばれている。

[0003] また、光電変換装置の光電変換効率を高めるために、バンドギャップの異なる半導体からなる光電変換層を複数重ねて用いる方法がある。このように複数の光電変換層を重ねて用いた光電変換装置は多接合型光電変換装置と呼ばれ、吸収波長帯域が異なる光電変換層を2段重ねた構造はタンデム構造、3段重ねた構造はトリプル構造と呼ばれている。タンデム構造の光電変換装置を例にとると、太陽光入射側の光電変換層(以下、「トップセル」ともいう)としては短波長の光を吸収するアモルファス(非晶質)シリコンが用いられ、また、トップセルで吸収されなかった光を吸収するために、太陽光入射側とは反対側の光電変換層(以下、「ボトムセル」ともいう))としては長波長の光を吸収する微結晶シリコン等の結晶質シリコン系半導体を用いることができる。

[0004] このような光電変換装置を用いた太陽電池には、次のような技術課題(1)が存在する。

(1)高効率化:太陽光をエネルギー変換部にいかに効率よく取り込み、電気エネルギーに変換する効率をいかに高めるか。

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[0005] 上記技術課題(1)の高効率化としては、12%以上の発電効率を得ることが目安となるが、従来、例えばタンデム型太陽電池において12%以上の発電効率を得るためには、2μm以上のボトムセル膜厚が必要であった。更に発電効率を上げるためには、ボトムセルの厚膜化(3μm以上)が検討されている。

[0006] また、上記技術課題(1)の高効率化を実現するために、第1透明電極を含めた基板のヘイズ率を高めることが検討されている。従来は、第1透明電極を含めた基板のヘイズ率を大きくすると、入射光の光散乱による光閉じ込め効果が向上して発電電流は増大するが、第1透明電極を含めた基板表面の大きな凹凸の影響などで開放電圧と形状因子が大幅に低下するので、電池としては好ましくないと、一般的に考えられていた。これを解決するために、前記基板及び第1透明電極として、ガラス基板上に、不連続な複数の山部によるマクロな凹凸(テクスチャ)と、この山部間をうめる複数の平坦部とを有しており、該山部及び該平坦部の外表面が、ミクロの多数の凹凸(テクスチャ)を有する構造(ダブルテクスチャ構造)となっている透明導電性酸化物付き基体を用いることが提案されている(特許文献1、特許文献2参照)。特許文献1及び2の透明導電性酸化物付き基体は、太陽光の全波長域で良好な光散乱性能有するものであり、特許文献2には、これを用いて作製されたアモルファスシリコン太陽電池が、その実施例において、開放電圧と形状因子をほぼ維持しつつ光電変換効率が高められることが示されている。

特許文献1:国際公開第03/036657A1号公報

特許文献2:特開2005-347490号公報

発明の開示

[0007] 光電変換装置を用いた太陽電池を実用化するためには、前記技術課題(1)に加え、下記技術課題(2)も存在する。

(2)生産性向上:生産性のボトルネックとなる結晶質シリコン系光電変換層中のi層をいかに薄膜化できるか。

[0008] 太陽電池の製造時間は、ボトムセル等を構成する結晶質シリコン系光電変換層中のi層の製膜時間に律速するため、上記技術課題(2)の生産性の点からは、結晶質シリコン系光電変換層中のi層の膜厚の薄膜化が極めて有効である。ところが、例え

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ばタンデム型太陽電池においてボトムセルの膜厚を2μmより薄膜化すると、発電電流の低下が著しく、よって発電効率の低下が著しくなる。このため、太陽電池の製造時間が長時間かかっても、2μm以上のボトムセル膜厚が適用されている。

このように、前記技術課題(1)と(2)とは、互いにトレードオフの関係にあった。

[0009] 前記特許文献1に示された技術は、光の吸収波長特性が異なる結晶質シリコン系半導体からなる光電変換層の発電効率を特に考慮したものではなく、また、太陽電池の生産性向上について検討されたものでもなかった。従って、結晶質シリコン系半導体からなる光電変換層を有する太陽電池については、入射光の吸収波長域が特に長波長側で異なるため、透明電極の凹凸による光閉じ込め形状は違うものが必要となるが、結晶質シリコン系半導体の膜厚を薄膜化することを考慮して凹凸形状を適正化することが未確立であり、発電効率の高効率化(技術課題(1)の解決)と太陽電池の生産性向上(技術課題(2)の解決)を両立できる技術が依然として望まれていた。

[0010] また、特許文献1のように大きな凹凸と小さな凹凸の混在する透明導電性酸化膜付き基板を用いて太陽電池を作製すると、大きな凹凸構造のみで構成してヘイズ率を高めた透明導電性酸化物付き基板を用いる場合よりも開放電圧と形状因子の低下を小さくすることはできるものの、やはり開放電圧と形状因子の低下が認められる。

[0011] 本発明は、このような事情に鑑みてなされたものであって、高い光電変換効率と高い生産性を両立した光電変換装置及びその製造方法を提供することを目的とする。

[0012] また、本発明は、大小の凹凸が混在した形状によりヘイズ率を高めた透明電極付き基板を用いた光電変換装置において、開放電圧と形状因子の低下を抑制しつつ高い光電変換効率を実現すること、およびこのような光電変換装置の製造方法を提供することを目的とする。

[0013] 上記課題を解決するために、本発明の第1の態様にかかる光電変換装置は、以下の手段を採用する。

すなわち、本発明の第1の態様にかかる光電変換装置は、透明絶縁性の基板上に透明電極層を設けてなる透明電極付き基板と、該透明電極付き基板の透明電極層側に順次形成された、結晶質シリコン系半導体を主として有する光電変換層ならび

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に裏面電極層とを少なくとも有してなる光電変換装置であって、前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上であり、前記光電変換層の膜厚が1.2μm以上2μm以下であり、かつラマン比が3.0以上8.0以下である光電変換装置である。

[0014] 前記第1の態様にかかる光電変換装置において、結晶質シリコン系光電変換層のラマン比を3.0以上8.0以下とすることにより、結晶の粒界が適度に非晶質シリコンで充填された光電変換装置を得ることができる。これにより、結晶粒界の電流リークを抑制できるので、開放電圧(Voc)及び形状因子(FF)の低下が抑制された光電変換装置を得ることができる。前記透明電極付き基板を用いた場合には、基板の凹凸に起因して欠陥の多い結晶粒界が生成しやすいため、結晶粒界の非晶質シリコンによる充填が特に有効である。

[0015] また、膜厚が1.2μm以上2μm以下の前記結晶質シリコン系半導体を主として有する光電変換層を形成することにより、結晶質シリコン系半導体を主として有する光電変換層のi層の膜厚を薄膜としても、高い発電電流を生じる光電変換装置を製造することができ、更に欠陥数を膜厚分低下でき、また、膜厚方向の電位勾配が大きいので発生電荷が欠陥にトラップされにくくなるので、開放電圧(Voc)及び形状因子(FF)の低下が抑制された光電変換装置を製造することができる。従って、薄膜化と高効率化を同時に達成した光電変換装置を製造でき、さらに、結晶質シリコン系i層を薄膜化することで、この製膜によって律速される光電変換装置の製造時間を短縮することができるので、光電変換装置の生産性が向上する。

[0016] 一般にヘイズ率といえば、ヘイズメータで計測される、波長が約550nmの光のヘイズ率をさす。波長550nmのヘイズ率が高いと波長550nm程度の光はよく散乱されるが、長波長光は該波長のヘイズ率が高ければよく散乱されるが、該波長のヘイズ率が低ければ散乱されにくい。従来の一層の凹凸(テクスチャ)構造の場合、波長550nmのヘイズ率が30%であっても、波長800nmの分光ヘイズ率は5%以下となり、結晶質シリコン系の光電変換層で光を閉じ込めたい700～900nmの波長域の光の散乱増強による光閉じ込めは不十分であった。また、350nm以下の波長域では、前記透明電極基板の透過率が小さくなるためヘイズ率を正しく計測することができない

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。したがって、550nm以上800nm以下の波長のヘイズ率を、波長を特定した光を用いて計測する分光ヘイズ率で定義し、分光ヘイズ率20%以上、より好ましくは30%以上とすることにより、結晶質シリコン系の光電変換層で光閉じ込めの影響を強く受ける700～900nmの波長域の光の散乱、光閉じ込めを増強でき、発電電流を増大することができる。

[0017] 前記第1の態様にかかる光電変換装置において、前記透明電極付き基板と前記結晶質シリコン系半導体を主として有する光電変換層との間に、非晶質シリコン系半導体を主として有する光電変換層を形成してもよい。

[0018] このような構成とすることにより、非晶質シリコン系半導体を主として有する光電変換層では太陽光の短波長側成分の光電変換が行われ、結晶質シリコン系半導体を主として有する光電変換層では太陽光の長波長側成分の光電変換が行なわれるので、より光電変換効率の高い光電変換装置とすることができる。

[0019] 前記第1の態様にかかる光電変換装置において、前記非晶質シリコン系半導体を主として有する光電変換層と前記結晶質シリコン系半導体を主として有する光電変換層との間に、中間コンタクト層を形成してもよい。

[0020] 中間コンタクト層を構成とすることにより、非晶質シリコン系半導体を主として有する光電変換層を薄膜化し、劣化率を改善できる一方で、結晶質シリコン系半導体を主として有する光電変換層への入射光が低下し、電流値が低下する。したがって、非晶質シリコン系半導体を主とする光電変換層の劣化率改善と、結晶質シリコン系半導体を主とする光電変換層の発電電流の低下との相対関係から、中間コンタクト層の膜厚は、90nm以下とすることが好ましく、さらには50nm以上70nm以下とすることがより好ましい。また、中間コンタクト層としては、ZnO系膜(例えば、GZO膜)で形成され、ZnO系単膜での光吸収率がλ＝450nm以上1000nm以下の範囲で1%未満であることがより好ましい。中間コンタクト層の透明性が損なわれると、結晶質シリコン系半導体を主とする光電変換層へ入射する光が低下し、発電電流が低下するため、波長が450nm以上1000nm以下の波長領域に対しては、ほぼ透明であることが好ましい。

[0021] 前記第1の態様にかかる光電変換装置において、前記透明電極付き基板の透明

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電極層表面が、複数の山部と複数の平坦部とで構成され、該山部及び該平坦部の表面がミクロの多数の凸部を連続して有してなり、前記山部の前記基板面垂直方向における高さが0．4μm以上0．7μmであり、基板面10μm角における前記山部の数が15以上50以下であり、前記ミクロの多数の凸部の底面径が0.1μm以上0.3μm以下であり、高さ／底面径の比が0.7以上1.2以下であるものが好ましい。

[0022] 前記第1の態様にかかる光電変換装置は、前記特性を有する透明電極付き基板を適用することで、結晶質シリコン系半導体を主として有する光電変換層（例えば、タンデム型太陽電池のボトムセル）のi層の膜厚を例えば1．5μmの薄膜としても、高い発電電流を生じる。更に結晶質シリコン系半導体を主として有する光電変換層のi層を薄膜化することにより、開放電圧（Voc）及び形状因子（FF）の低下も抑制できる。すなわち、結晶質シリコン系半導体を主として有する光電変換層を薄膜とすることにより、欠陥数を膜厚分低下でき、また、膜厚方向の電位勾配が大きいので発生電荷が欠陥にトラップされにくくなる。従って、光電変換装置の薄膜化と高効率化を同時に達成できる。さらに、結晶質シリコン系光電変換層中のi層を薄膜化できることにより、この層の製膜時間によって律速される光電変換装置の製造時間を短縮することができるので、前記第1の態様にかかる光電変換装置は、生産性が向上したものとなる。

[0023] 従来の技術において開放電圧と形状因子が低下した原因の1つとして、透明電極の谷の部分から光電変換層の膜厚方向に膜成長相間の不連続な境界（その境界を「異相」と呼ぶことにする）が生じ、キャリアの再結合中心となるためと推定される。この異相は、下地の谷々の面からシリコン膜が製膜・成長する際に、その成長面が衝突し、衝突面が格子の欠陥或いは微細な隙間となったものと推定され、キャリアの再結合による損失の原因となる。尚、この光電変換層の膜厚方向の異相は、光電変換層の断面方向の透過顕微鏡分析によって、検出することができる。倍率8万倍以上で光電変換層を長さ100μmの範囲で観察し、亀裂が認められたとき異相がある、貫通する異相が1本でも認められたとき貫通する異相があると判断する。

[0024] この異相の発生自体を抑制するには、透明導電性酸化物基板の凹凸を単純に大型化するのではなく、大きな凹凸と小さな凹凸が混在することが有効である。しかしな

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がら、前記透明電極を用いた場合においても、例えば製膜速度が1nm／sec以上の高速で製膜すると完全に異相の発生を抑制することは難しく、異相発生の抑制には光電変換層を形成する製膜条件選定における制限がある。このため、本発明者らは、特に高速で製膜する場合において異相が発生しても光電変換層を貫通する異相を遮断する知見を得るに至った。

[0025] 従って、本発明者らは、この異相を抑制すること、または完全に抑制はできなくても光電変換層を貫通する異相を遮断できれば、開放電圧低下、形状因子低下を抑制できるという知見を得た。

[0026] この知見から、上記課題を解決するために、本発明の第2の態様にかかる光電変換装置及び第3の態様にかかる光電変換装置の製造方法は、以下の手段を採用する。

すなわち、本発明の第2の態様にかかる光電変換装置は、透明絶縁性の基板上に透明電極層を設けてなる透明電極付き基板と、該透明電極付き基板の透明電極層側に順次形成された、非晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも有し、前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上、特に好ましくは30%以上であり、前記非晶質シリコン系半導体を主として有する光電変換層中に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相（膜成長相間の不連続な境界）を遮断する層（異相遮断層と呼ぶこととする）を設けた光電変換装置、もしくは前記基板と前記非晶質シリコン系半導体を主として有する光電変換層の間に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相の形成を防止する異相防止層を設けた光電変換装置である。

[0027] 第2の態様にかかる光電変換装置によれば、非晶質シリコン系半導体を主として有する光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相を遮断または防止できるので、このような異相による電流リークを抑えることができ、開放電圧低下、形状因子低下が抑制される。

[0028] また、本発明の第3の態様にかかる光電変換装置の製造方法は、透明絶縁性の基

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板上に透明電極層を形成して透明電極付き基板を作製し、該透明電極付き基板の透明電極層側に非晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも順次形成する光電変換装置の製造方法であって、前記透明電極付き基板の透明電極層表面が多数の凸部を連続して有してなり、前記非晶質シリコン系半導体を主として有する光電変換層中に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相を遮断する異相遮断層を形成するか、もしくは前記透明電極層の形成と前記非晶質シリコン系半導体を主として有する光電変換層形成の間に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相の形成を防止する異相防止層を形成する、光電変換装置の製造方法である。

[0029] 第3の態様にかかる光電変換装置の製造方法によれば、非晶質シリコン系半導体を主として有する光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相が遮断または防止されるので、このような異相による電流リークが抑えられ、開放電圧低下、形状因子低下が抑制された光電変換装置を製造することができる。

[0030] 前記第2の態様にかかる光電変換装置及び第3の態様にかかる光電変換装置の製造方法において、前記非晶質シリコン系半導体を主として有する光電変換層をp層、i層、n層を順次形成してなる層とし、前記異相遮断層を前記i層の一部分において、p層、n層、あるいはi層の他の部分より低速で製膜された層とすることができる。低速で製膜することにより、製膜面表面での製膜粒子の拡散・移動時間が増大し、より安定なサイトに堆積して低欠陥の層、即ち異相が少ない層を形成することができる。また、低速で製膜された層はi層の一部分と薄いため、低速で製膜する製膜時間にかかる処理時間は、全体の生産時間に与える影響としては少なくなり、生産性を維持したまま異相が少ない層を形成することができる。

[0031] あるいは、前記非晶質シリコン系半導体を主として有する光電変換層をp層、i層、n層を順次形成してなる層とし、前記n層の一部或いは全体を非晶質の層として、前記n層が前記異相遮断層の機能を有することができる。なお、非晶質とは、ラマン分光分析で分析したとき、Si結晶のピークが全く検出されないものであり、製膜条件では、水素ガス／シランガス希釈率を低下する方向、又はRFパワーを低下する方向で得る

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ことができる。積層膜で再表面のみ非晶質膜にする場合は、ラマン分光分析で下地のSi結晶質膜のピークが検出されることがあり、ガラス基板又は透明電極つきガラス基板上に、単一条件の膜のみを形成してラマン分光分析を実施してSi結晶ピークの有無を判断することとする。非晶質の膜は、欠陥が水素で終端されるので、結晶質と比較して欠陥が連続しにくいために異相となりにくく、異相を遮断する機能を有するものである。

あるいは、前記非晶質シリコン系半導体を主として有する光電変換層をp層、i層、n層を順次形成してなる層とし、前記n層の少なくともその一部を200Pa以上の圧力下で製膜した層とすることにより、前記n層が異相遮断層の機能を有することができる。高圧で製膜すると、製膜される原料ガスの気相中での衝突拡散が促進され、下地の凹部にも原料ガスが到達しやすいために、凹部にも均一に製膜されるので、欠陥上にも均一に良好な膜が形成される、すなわち異相を抑制できると考えられる。

あるいは、前記異相防止層を、前記凸部を円滑化した前記透明電極層とすることができる。前記凸部の円滑化とは、凸部が連続して形成されることにより凸部の境界に生成する谷部について、通常は平面どおしの組合せのため谷の底は明瞭な線状であるが、その線がないように底面を円滑化したもの、例えば、スプーンカットのような形状を有することである。

[0032] 前記異相防止層を、前記透明電極層表面にイオン処理を施して形成してもよい。イオン処理とは、例えば真空中でのアルゴンイオン照射によるイオンエッチングであり、透明電極の表面形状を原子レベルのエッチング、再付着により制御できる。イオンエッチングのイオン照射角度とイオンエネルギーを調整することで、透明電極の凹凸の特に斜面部の原子をエッチング除去し、谷部の底に再付着させることができ、結果として鋭利な谷形状を円滑化することができる。

[0033] 前記第2の態様にかかる光電変換装置及び第3の態様にかかる光電変換装置の製造方法において、前記透明電極付き基板は、550nm以上800nm以下の波長における分光ヘイズ率が20%以上であるものが好ましい。前記分光ヘイズ率が30%以上であるものが特に好ましい。

上述のとおり、従来の凹凸(テクスチャ)構造の場合、波長550nmの分光ヘイズ率

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が30％であっても、波長800nmの分光ヘイズ率は5％以下となり、結晶質シリコン系半導体の光電変換層で光を閉じ込めたい700～900nmの波長域の光の散乱増強による光閉じ込めは不十分であった。そこで、前記第2の態様にかかる光電変換装置及び第3の態様にかかる光電変換装置の製造方法においては、凹凸を大型化して、長波長光に対しても高ヘイズとなるようにする。また、350nm以下の波長域では、前記透明電極の透過率が小さくなるためヘイズメータにより分光ヘイズ率を計測することができない。したがって、550nm以上800nm以下の波長の分光ヘイズ率を20％以上、好ましくは30％以上とすることにより、結晶質シリコン系半導体の光電変換層で光閉じ込めの影響を強く受ける700～900nmの波長域の光の散乱、光閉じ込め効果を増強でき、発電電流を増大することができる。

[0034] 前記第2の態様にかかる光電変換装置及び第3の態様にかかる光電変換装置の製造方法において、前記非晶質シリコン系半導体を主として有する光電変換層と前記裏面電極の間に、結晶質シリコン系半導体を主として有する光電変換層を形成してもよい。

[0035] このような構成とすることにより、非晶質シリコン系半導体を主として有する光電変換層では太陽光の短波長側成分の光電変換が行われ、結晶質シリコン系半導体を主として有する光電変換層では太陽光の長波長側成分の光電変換が行なわれるので、より光電変換効率の高い光電変換装置とすることができる。

[0036] また、結晶質シリコン系半導体を主として有する光電変換層は結晶質シリコン系半導体に限らず、結晶質もしくは非晶質シリコン系半導体、結晶質もしくは非晶質シリコンゲルマニウム系半導体を主として有しても同等の効果が得られる。

[0037] また、結晶質シリコン系半導体を主として有する光電変換層とさらに第3の光電変換層を積層して3層構造以上の光電変換装置としても良い。この場合、結晶質シリコン系半導体を主として有する光電変換層及び第3の光電変換層は、結晶質もしくは非晶質シリコン系半導体、結晶質もしくは非晶質シリコンゲルマニウム系半導体を主として有する光電変換層とすることともでき、非晶質シリコン系半導体を主として有する光電変換層、結晶質シリコン系半導体を主として有する光電変換層光電変換層、第3の光電変換層の順に長波長側成分へと吸収が増大するように、各光電変換層の

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材料や膜質、膜厚を設定すれば良い。

[0038] 本発明によれば、高い光電変換効率と高い生産性を両立した光電変換装置及びその製造方法を提供することができる。本発明の光電変換装置は、太陽電池として好適に利用することができる。

[0039] また、本発明によれば、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上、特に好ましくは30%以上である透明電極付き基板を用いた光電変換装置において、開放電圧と形状因子の低下を抑制しつつ高い光電変換効率を実現することができる。さらに、このように優れた光電変換装置の製造方法を提供することができる。本発明の光電変換装置は、太陽電池として好適に利用することができる。

[0040] また、光電変換層を薄膜化しても高い光電変換効率が得られる。薄膜化により、発電電流は多少は低下するが、従来の基板に対し薄膜化による発電電流低下は大幅に改善できている。また、薄膜化により、開放電圧と形状因子が向上される。薄膜化による光電変換層の薄膜化により、光電変換層に含まれる欠陥を膜厚相当分低下できること、および光電変換層内に発生する起電力に対する電位勾配が拡大することによる生成電荷の再結合(欠陥による消滅)確率を低下できるためである。

[0041] 薄膜化は、生産性の点でメリットが大きい。光電変換装置ひとつあたりの生産時間を短縮でき、さらに生産装置の製膜室内部のメンテナンス頻度も低下でき、結果として、時間あたり或いは装置あたりの生産量を薄膜化の膜厚の比率以上に増大できる。従って、生産を考慮すると、光電変換効率の向上以上に、生産性向上のメリットが大きいといえる。

図面の簡単な説明

[0042] [図1]本発明の光電変換装置の構成を示す概略図である。

[図2]本発明の第1実施形態で用いられる透明電極付き基板の形状及び構成を示す一部切欠き断面図である。

[図3]図2に示す山部112の拡大図である。

[図4]本発明の太陽電池パネルの製造方法の実施形態の一部を示す概略図である。

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[図5]本発明の太陽電池パネルの製造方法の実施形態の一部を示す概略図である。

[図6]本発明の太陽電池パネルの製造方法の実施形態の一部を示す概略図である。

[図7]本発明の太陽電池パネルの製造方法の実施形態の一部を示す概略図である。

[図8]本発明の第2実施形態のイオン処理前における透明電極付き基板の透明電極表面の電子顕微鏡写真である。

[図9]本発明の第2実施形態のイオン処理後における透明電極付き基板の透明電極表面の電子顕微鏡写真である

[図10]本発明の第2実施形態の透明電極付き基板を用いて作製したタンデム型太陽電池の断面の透過型電子顕微鏡写真である。

[図11]本発明の第2実施形態の透明電極付き基板を用いて作製したタンデム型太陽電池の断面の透過型電子顕微鏡写真である。実施例7に示したように非晶質Si—i層の製膜後期を位相遮断層として、非晶質Si層を貫通する異相を抑制したものである。

[図12]実施例11のタンデム型太陽電池における、ボトムセルのn層製膜後のラマン比と太陽電池特性の関係を示す図である。

符号の説明

[0043] 1 基板

2 透明電極層

3 光電変換層

4 裏面電極層

6 太陽電池モジュール

90 光電変換装置

91 第1セル層(トップ層)

92 第2セル層(ボトム層)

93 中間コンタクト層

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110 透明電極付き基板

111 基板

112 山部

114 透明電極

115 小山部

116 連続層

117 凸部

H_a 山部の高さ

P_a 山部間の平均ピッチ

H_c 小山部H_cの高さ

P_c 小山部間の平均ピッチ

H_b 凸部の高さ

P_b 凸部間のピッチ

15 絶縁溝

21 バックシート

23 出力ケーブル

50 太陽電池パネル

発明を実施するための最良の形態

[0044] 第1実施形態

以下に、本発明の第1実施形態について、図面を参照して説明する。

[0045] まず、本実施形態の光電変換装置の製造方法により製造される光電変換装置の構成について説明する。

[0046] 図1は、本実施形態の光電変換装置の構成を示す概略図である。光電変換装置90は、シリコン系太陽電池であり、基板1、透明電極層2、太陽電池光電変換層3としての第1セル層(トップ層)91ならびに第2セル層(ボトム層)92、及び裏面電極層4を具備する。本実施形態において、第1セル層91は非晶質シリコン系半導体を主として有する光電変換層であり、第2セル層は結晶質シリコン系半導体を主として有する光電変換層である。第2セル層92は、膜厚が1.2μm以上2.0μm以下、かつ、第

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2セル層92のラマン比が3．0以上8．0以下であることが好ましい。より好ましくは、ラマン比が3．5以上8．0以下であり、更に好ましくは5．0以上7．5以下である。

[0047] 第2セル層92のラマン比を3．0以上8．0以下とすることにより、結晶の粒界が適度に非晶質シリコンで充填された光電変換装置を得ることができ、結晶粒界の電流リークを抑制できるので、開放電圧(Voc)及び形状因子(FF)の低下が抑制された光電変換装置を得ることができる。

[0048] ここで「ラマン比」とはラマン分光評価で520cm^{-1}の結晶Siの強度と480cm^{-1}の非晶質Siの強度の比(結晶Siの強度／非晶質Siの強度)をいう(以下同じ)。ラマン比の測定方法としては、光電変換装置の裏面電極を過酸化水素水等の溶剤で溶剤除去して供試体とする。まず、第2セル層92の膜面側から測定用光を照射する。測定用光としては、レーザー単色が用いられ、例えば、YAGレーザー光の2倍波(波長532nm)が好適に用いられる。第2セル層92の膜面側から測定用光を入射すると、ラマン散乱が観測されるが、測定用光、及び散乱光の一部は第2セル層92中で吸収される。したがって、例えば、YAGレーザー光の2倍波を測定用光として用いた場合は、入射面から約0．1μmの深さまでの情報を得ることができる。なお、第2セル層92と裏面電極層4との間に第2の透明電極層を形成している場合は、第2の透明電極層のラマンピークはバックグランドとして差し引くことができるので、第2の透明電極層を希塩酸等の溶剤により溶剤除去しなくてもしてもよい。

[0049] 上記したように、ラマン比は光電変換層i層(実質的に真性な層)を評価するが、一般的に用いられるレーザー波長532nmでは、0．1μmの侵入深さにより、表面から約0．1μmの膜の結晶化率を評価することとなる。本実施形態においては、第2セル層92のi層製膜後のラマン比が3．0以上8．0以下であることが直接的な意味であるが、最表面にn層が製膜されてもn層は膜厚が0．03μm程度と薄いのでi層からの情報が支配的であること、および一般的なn層の結晶性も2～10であることにより、n層製膜後にn層を含めたラマン比を計測してもn層製膜前と近い値となる。したがって、第2セル層92のラマン比は、3．0以上8．0以下が好ましい範囲となる。

また、ラマン比は製膜において製膜装置構造などにより基板1上で分布が発生する。例えば製膜時に基板1表面上での原料ガス組成変化による局所的なラマン比分布

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や、プラズマや温度分布による全体的なラマン比分布がある。このため、評価する基板1上で極力全体的な平均値として評価する。例えば、1m角以上の基板サイズであれば、均等に区分けした少なくとも10箇所以上の領域で計測し、この平均値で評価することが好ましい。

[0050] ラマン比が3.0以上8.0以下という値は、一般的に結晶化が進んだ結晶質シリコンの値より、非晶質シリコンを多く含むものである。特にダブルテクスチャ基板のような高ヘイズ基板を用いる場合、基板の凹凸に起因する結晶粒界の欠陥が生じるため、粒界を適度に非晶質シリコンで充填することが重要となる。ラマン比が3.0以上が好ましい理由は、結晶シリコン部で発生した電荷が断面方向につながった結晶構造を導通することができるように大部分の結晶構造が膜厚方向に連続するために必要なラマン比が3.0以上であるためで、これは断面観察により確認できる。ラマン比が8.0以下が好ましい理由は、柱状結晶の粒界が電流リークポイントとなり電圧が発生しなくなるのを抑制するために非晶質で結晶粒界を充填することが好ましく、実験的にその場合のラマン比が8.0以下であるためである。

[0051] なお、ここで、「シリコン系」とはシリコン(Si)やシリコンカーバイド(SiC)やシリコンゲルマニウム(SiGe)を含む総称である。また、「結晶質シリコン系」とは、アモルファスシリコン系すなわち非晶質シリコン系以外のシリコン系を意味するものであり、微結晶シリコンや多結晶シリコン系も含まれる。

[0052] 第1セル層91及び第2セル層92の間には、透明導電膜からなる中間コンタクト層93を設けても良い(但し、本発明の光電変換装置は、中間コンタクト層93を設けたものに限定されない)。中間コンタクト層93
を設けた場合、この中間コンタクト層93で入射太陽光の一部が反射されて、第1セル(トップ層)91に再度入射される。これにより、第1セル層(トップセル)91における発電電流が増加する。そして、第1セル層91の膜厚を薄くしても、中間コンタクト層93が積層されない場合と同等の発電電流を得ることができる。したがって、第1セル層91非晶質シリコン系半導体の膜厚を薄くすることにより、当該第1セル層91における光劣化を抑制でき、光電変換装置全体としての安定化効率を向上させることができる。

[0053] 中間コンタクト層93の膜厚を厚くすることにより、第1セル層91である非晶質シリコ

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ン系半導体の発電電流を増加させることができる。このとき，中間コンタクト層93により反射される太陽光の波長における第2セル層92での発電電流は減少する。実際には，第2セル層92である結晶質シリコン系半導体においては，第1セル層91である非晶質シリコン系半導体よりも長波長領域の太陽光による電気エネルギーへの変換が行われている。

[0054] 従って，中間コンタクト層93の膜厚を最適化することにより，中間コンタクト層93による，第2セル層92である結晶質シリコン系半導体が吸収すべき長波長領域の太陽光の吸収率を抑制することが必要になる。

[0055] 本実施の形態に係わる光電変換装置の中間コンタクト層93の膜厚と，第2セル層92における波長800nm（太陽光の長波長領域に対応）の量子効率（入射のうち発電に寄与する割合）との関係から，中間コンタクト層93の膜厚が厚くなると，中間コンタクト層93での長波長領域の太陽光の反射率も増大して，第2セル層92に入射する光量が減少する。中間コンタクト層93は，光吸収率がλ＝450nm以上1000nm以下の範囲で1％未満であることが好ましく，この波長領域に対しては，ほぼ透明であることが好ましい。

[0056] 一方，中間コンタクト層93の膜厚が厚くなると，中間コンタクト層93と裏面電極層4との間で光の閉じ込め効果が増大する。このため，第2セル層92に入射した光吸収率が増大する。波長800nmの太陽光に対して，第2セル層92における光の閉じ込め効果が有効に作用する（量子効率を一定の値に維持することができる）中間コンタクト層93の膜厚は100nm以下である。

[0057] 上述したように，第1セル層91と第2セル層92との発電電流バランスを考慮して，最適な中間コンタクト層93の膜厚値は実験的に90nm以下となり，より好ましくは50nm以上70nm以下となる。これにより，より高い安定化効率を有する光電変換装置が実現される。

[0058] 次に，本発明の第1実施形態による光電変換装置において用いられる，透明電極を形成した透明絶縁性基板（以下，「透明電極付き基板」ともいう）の形状及び構成を，図2及び図3を用いて詳細に説明するが，本発明の光電変換装置及びその製造方法は，これらの図面によって限定されない。

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[0059] 図2は、本実施形態で用いられる透明電極付き基板の形状及び構成を示す一部切欠き断面図であり、図3は、図2に示す山部112の拡大図である。図2に示すように、本実施形態において用いられる、透明電極付き基板110は、ガラス基板111上に、不連続な複数の山部112によるマクロな凹凸(テクスチャ)と、この山部間をうめる複数の平坦部113とを有しており、該山部112及び該平坦部113の外表面は、ミクロの多数の凹凸(テクスチャ)を有する構造となっている。以下、このような2つの凹凸を有する構造を、ダブルテクスチャ構造という。

[0060] また、本実施形態においては、図2に示すように、透明電極114は、第1の酸化物からなる不連続な小山部115と、その上に形成される第2の酸化物からなる連続層であって該連続層の表面にミクロの多数の凸部を連続して有する連続層116とからなるのが好ましい。小山部115の密度は、基板111面の10μm角あたり15以上50以下とされ、20以上45以下がより好ましい。この小山部115間の平均ピッチP_sは、1.0μm以上3μm以下に相当する。

第2の酸化物からなる連続層116は、小山部115上及び小山部115が形成されていない部分のガラス基板111上に連続的に形成されている。

[0061] 本実施形態においては、上記山部112の平均の高さH_s(平坦部上のミクロの凸部の頂部からの高さの平均値)は、0.4μm以上0.7μm以下であり、0.5μm以上0.6μm以下であることがより好ましい。

また、隣接する上記山部間の平坦部の距離(以下、単に「山部間の間隔」ともいう。)W_sは、直線上に0μm以上1.5μm以下であることが好ましく、0μm以上1.0μm以下であることがより好ましく、0.1μm以上0.4μm以下(いずれの山部112も不連続である)であることがさらに好ましい。本実施形態においては、複数の山部112は不連続である部分と連続している部分があってもよく、山部間の間隔W_sが0μm以上1.5μm以下であるということは、平坦部がないところがあってもよいということである。なお、平坦部が無い場合には、上記山部に隣接していなくても、上記山部付近の平坦部を用いてH_sを計測でき、または断面の顕微鏡観察を行うことでH_sは計測することができる。

さらに、上記山部112の密度は、小山部115の密度と同様の値となり、基板111面

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の10μm角あたり15以上50以下となり、20以上45以下がより好ましい。この山部112間の平均ピッチP_sは、1.0μm以上3μm以下に相当する。

[0062] 本実施形態においては、上記小山部115の高さH_cは、上記山部の高さH_sと同様の値、すなわち0.4μm以上0.7μm以下であり、0.5μm以上0.6μm以下であることがより好ましい。

[0063] 本実施形態においては、山部112及び平坦部113の表面、すなわち、第2の酸化物からなる連続層116の表面は、図3に示されるように、ミクロの多数の凸部117を有している。ミクロの多数の凸部の底面径が0.1μm以上0.3μm以下であり、高さ／底面径の比が0.7以上1.2以下である。尚、ミクロの凸部の連続層は、表面全体においてミクロの凸部が存在する状況を示していて、一部にミクロの凸部が欠損した領域が存在しても、連続している状況とみなすものである。

[0064] また、図3において、上記小山部115上の連続層116の厚さH_d(ミクロの凸部を含む)は、0.5μm以上1.0μm以下であることが好ましく、0.5μm以上0.7μm以下であることがより好ましい。同様に、上記ガラス基板111上の連続層116の厚さH_e(ミクロの凸部を含む)は0.5μm以上1.0μm以下であることが好ましく、0.5μm以上0.7μm以下であることがより好ましい。

[0065] 本実施形態においては、上記山部112及び上記平坦部113の外表面を、このような山部による凹凸(マクロな凹凸)よりも小さな凹凸(ミクロな凹凸)とすることにより、短波長の光を強く散乱することができ、全体として広い領域の光を有効に散乱することが可能になる。すなわち、大きな凹凸である山部により長波長の光を散乱し、小さな凹凸表面より短波長の光を散乱することができるため、全体として高い光散乱性を達成することができる。

特に本実施形態においては、山部112の高さと密度を制御することにより、長波長の光の散乱を最適化し、結晶質シリコン系半導体からなる光電変換層の発電効率の向上と、製膜時間の短縮が実現される。

[0066] 前記透明電極付き基板110におけるこのような表面性状は、例えば、以下に示す方法により確認することができる。

(1)表面形状の解析:膜表面の凸部を走査型電子顕微鏡(SEM)で観察し、得ら

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れる顕微鏡写真より，凸部の底面径を測定することができる。また、膜表面の凹凸形状をSEM、原子間力顕微鏡（AFM）により観察し，得られる顕微鏡写真より、膜表面の凹凸形及び凸部の高さを解析することができる。

（2）表面被覆率の測定：第1の酸化物からなる小山部の基板上への被覆率をSEM写真から測定し，基板上を小山部が占める面積を、基板の当該被覆面全体の面積で割った値を表面被覆率として評価することができる。

また、質量膜厚とは、基板上の一定面積中にある不連続の金属酸化物に対し、蛍光X線装置でその金属酸化物の金属量に比例する検出量を調べ、別途用意してある基板上に連続し，膜厚の既知の同種の金属酸化物における蛍光X線装置の検出量と比較して、不連続な酸化物の体積が連続になったと仮定して得られた膜厚を示す。

[0067] また、このような形状及び構成を有する透明電極付き基板110は、基板全体において、550nm以上800nm以下の波長における分光ヘイズ率が30％以上、好ましくは40％以上である。

[0068] ここで、「分光ヘイズ率」とは、透過光における散乱成分の割合を示すものである。分光ヘイズ率は波長に依存し、分光ヘイズ率をHz（λ）、全透過率をT_{total}（λ）、透過光の直進成分をT_{direct}（λ），透過光の散乱成分を$T_{diffuse}$（λ）とすると、下記式に示す関係が成り立つ。

$$T_{total}(\lambda)=T_{direct}(\lambda)+T_{diffuse}(\lambda)$$

$$Hz(\lambda)=T_{diffuse}(\lambda)/T_{total}(\lambda)\times 100[\%]$$

[0069] 以下に，上述した本実施形態の透明電極付き基板の形状及び構成ならびに特性を満たす基板（透明基板）、第1の酸化物及び第2の酸化物について詳述する。

[0070] ＜基板（透明基板）＞

本実施形態の透明電極付き基板に用いられる基板は、必ずしも平面で板状である必要はなく、曲面でも異型状でもよい。

このような基板としては，少なくともその表面が後述する第1の酸化物と異なる材料であることが好ましく，具体的には、ガラス基板、セラミックス基板、プラスチック基板，金属基板等や、これらの基板表面に酸化ケイ素膜、酸化アルミニウム膜、酸化ジルコ

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ニウム膜、酸化チタン膜などのアルカリバリヤ層を施したもの等が挙げられる。これらのうち、透光性に優れた透明の基板であることが好ましく、ガラス基板もしくはアルカリバリア層を施したガラス基板であることが強度及び耐熱性の点から好ましい。

また、このような基板は、光電変換層の主たる吸収波長域である550nm以上800nm以下の波長領域において高い透過率、例えば80%以上の透過率を有することが好ましく、十分絶縁性で、かつ化学的、物理的耐久性が高いことが望ましい。

[0071] 上記ガラス基板としては、具体的には、例えば、無色透明なソーダライムシリケートガラス、アルミノシリケートガラス、ボレートガラス、リチウムアルミノシリケートガラス、石英ガラス、ホウ珪酸ガラス基板、無アルカリガラス基板、その他の各種ガラスからなる透明ガラス板を用いることができる。

また、本実施形態の透明電極付き基板を太陽電池用基板に用いる場合においては、ガラス基板の厚さは0.2mm以上6.0mm以下であることが、強度及び透過率の点から好ましい。

[0072] なお、ソーダライムシリケートガラス等のナトリウムを含有するガラスからなるガラス基板または低アルカリ含有ガラスからなるガラス基板の場合には、ガラスからその上面に形成される透明電導膜へのアルカリ成分の拡散を最小限にするために、上述したアルカリバリヤ層を施したガラス基板を用いることが好ましい。

また、ガラス基板の表面に、ガラス基板の表面と、その上に設けられる層との屈折率の差異を軽減するための層をさらに有していてもよい。

[0073] <第1の酸化物>

本実施形態の透明電極付き基板の透明電極膜を構成する第1の酸化物は、可視光域で高透明な酸化物であれば特に限定されず、その具体例としては、TiO_2、SnO_2、In_2O_3、ZnO、CdO、$CdIn_2O_4$、$CdSnO_3$、$MgIn_2O_4$、$CdGa_2O_4$、$GaInO_3$、$InGaZnO_4$、$Cd_2Sb_2O_7$、Cd_2GeO_4、$CuAlO_2$、$CuGaO_2$、$SrCu_2O_2$、Al_2O_3等が挙げられる。これらのうち、TiO_2、SnO_2及びフッ素を含有するSnO_2からなる群より選択される少なくとも1種を用いることが好ましい。

本実施形態においては、小山部を形成するこのような第1の酸化物の屈折率は、波長400nm以上800nm以下において、1.8以上2.2以下であることが好ましく、さら

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に、1．9以上2．1以下であることが好ましい。

第1の酸化物の形成方法として一例を示す。上述したアルカリバリア層付きガラス基板をベルトコンベア炉において520℃に加熱し、四塩化錫、水、塩化水素ガスを同時にガラス基板に吹き付けて酸化錫核を形成する。この際，四塩化錫、水は、あらかじめ加熱し、窒素ガスをバブリングして塩化水素ガスと同時に移送することでガラス基板上に吹き付ける。

酸化錫核を形成した後、四塩化錫と水を同時にガラス基板に吹き付けることで第1の酸化物であるSnO_2を形成する。この際，四塩化錫、水は、あらかじめ加熱し、窒素ガスをバブリングして移送することでガラス基板上に吹き付けた。

[0074] なお、このような第1の酸化物からなる小山部は、上述したように，不連続な突起物であって連続膜ではないので、該突起物に覆われていない透明基板部分は、当然ながら小山部による入射光の吸収損はゼロであるため、光電変換層への入射光量を増やすことができる。

これらの小山部は、長波長光の分光ヘイズ率を高める（光の散乱度を上げる）部分であり、自由電子による吸収を抑えて、高透明にするために、電気導電性はないのが好ましい。したがって、上記第1の酸化物としてSnO_2を用いた場合は、SnO_2のみからなるか、フッ素を含有する場合でもフッ素は、SnO_2に対して0．01mol%以下の含有量であることが好ましく、0．005mol%以下の含有量であることがより好ましい。

[0075] ＜第2の酸化物＞

本実施形態の透明電極付き基板の透明電極膜を構成する第2の酸化物は，可視光域で透明であり、さらに導電性を有している透明導電性酸化物であることが必要であり、その具体例としては、SnO_2、ZnO、In_2O_3等が挙げられ、2種以上を併用してもよく、さらに，導電性発現のためのドーパントを含有していることが好ましい。

これらのうち、SnO_2はドーパントとしてフッ素またはアンチモンをSnO_2に対して0．01mol%以上4mol%以下含有することが好ましい。ZnOはドーパントとしてホウ素、Al及びGaからなる群から選択される少なくとも1種をZnOに対して0．02mol%以上5mol%以下含有することが好ましい。In_2O_3はドーパントとしてSnをIn_2O_3に対して0．02mol%以上4mol%以下含有することが好ましい。なお、これらのドーパントを用い

たドーピングは、ハロゲン化水素によるものであってもよい。このようなハロゲン化水素としては、具体的には、例えば、HF、HBr等が挙げられる。

本実施形態においては、連続層を形成するこのような第2の酸化物の屈折率は、波長400nm以上800nm以下において、1．8以上2．2以下であることが好ましく、さらに、1．9以上2．1以下であることが好ましい。

[0076] また、上記第2の酸化物としてフッ素を含有するSnO_2を用いることにより、導電電子密度が向上する。太陽電池に用いる基板としては、導電電子密度は、$5\times10^{19}cm^{-3}$以上$4\times10^{20}cm^{-3}$以下であることが好ましく、$1\times10^{20}cm^{-3}$以上$2\times10^{20}cm^{-3}$以下であることがより好ましい。導電電子密度がこの範囲であれば、第2の酸化物からなる連続層の光吸収量が少なく、高透明で、かつ活性水素種に対して高い耐久性があるので、薄膜シリコン系太陽電池を形成する際に一般に用いられる水素プラズマ照射によっても、透明性は損なわれないため好ましい。

[0077] 上述した第1の酸化物と第2の酸化物とは、同じ酸化物を用いてもよく、本実施形態においては、いずれもSnO_2を用いることが好ましい。また、第1の酸化物及び第2の酸化物層の屈折率は、同等程度であることが好ましく、具体的には、1．8以上2．2以下であることが好ましい。第1の酸化物と第2の酸化物の屈折率がともにこの範囲であると、第1の酸化物と第2の酸化物との界面における光の反射が制御され、透過率が低下しないことから好ましい。

[0078] また、本実施形態においては、上述した第1の酸化物からなる小山部と、上述した第2の酸化物からなる連続層との間に、該第1の酸化物及び該第2の酸化物とは組成が異なる酸化物からなる酸化物層（以下，単に「異なる酸化物層」ともいう。）を有していることが好ましい。

このような異なる酸化物層を有していることにより、第2の酸化物からなる連続層の表面にミクロの多数の凸部が形成されやすく、山部と平坦部とを有する構造を容易に形成することができる。

[0079] また、このような異なる酸化物層を有する多層構造の透明電極膜においては、各層の界面での反射を軽減し、後述する光電変換層への入射光量を最大にする必要がある。すなわち、ガラス基板、第1の酸化物からなる小山部、異なる酸化物層、第2の

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酸化物からなる連続層の各界面での光反射をできるだけ低減することが望ましい。そのためには、第1の酸化物、異なる酸化物及び第2の酸化物の屈折率ができるだけ近いこと、または屈折率が離れている場合は、異なる酸化物層ができるだけ薄いことが望ましい。

このような異なる酸化物としては、具体的には、例えば、Si、Sn、Al、Zr及びTiからなる群から選ばれる1種以上の原子の酸化物が挙げられ、これらのうち、Siの酸化物を主成分とすることが好ましい。また、上記異なる酸化物は、高い透光性を有する必要があるため、非結晶性であるSiO_2であることがより好ましい。

なお、異なる酸化物層の膜厚は2nm以上40nm以下であることが好ましく、10nm以上30nm以下であることがより好ましい。

[0080] 本実施形態の透明電極付き基板は、上述したように、複数の山部とその間をうめる複数の平坦部とで構成され、該山部及び外平坦部の表面がミクロの多数の凸部を連続して有するものであるが、基板上から山部の頂上(ミクロの凸部を含む)までの高さは0.8μm以上3.0μm以下であることが好ましく、0.8μm以上1.0μm以下であることがより好ましい。ミクロの多数の凸部の底面径が0.1μm以上0.3μm以下であり、高さ/底面径の比が0.7以上1.2以下であることが望ましい。また、膜全体のシート抵抗が8Ω/□以上20Ω/□以下であることが好ましく、8Ω/□以上12Ω/□以下であることがより好ましく、550nmにおける透過率(透明性)は、浸液法で測定した場合、80%以上90%以下であることが好ましく、85%以上90%以下であることがより好ましい。

また、上記構成からなる本実施形態の透明電極付き基板を、光電変換装置の透明電極に用いると、基板を経て入射された光は、透明電極により屈折、散乱されて光電変換部に入射し、光電変換部中を長い距離にわたって通過する。その結果、多くの光が光電変換部にて吸収され、光電変換効率が向上する効果を奏するものとなる。特に、太陽電池に用いた場合には、開放電圧及び曲線因子を低下させずに短絡電流を高く維持することが可能となるため、光電変換効率が向上するものとなる。

[0081] 次に、本実施形態の太陽電池パネルの製造方法について説明する。ここでは、基板1としてのガラス基板上に太陽電池光電変換層3として非晶質シリコン系半導体を

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主として有する光電変換層及び結晶質シリコン系半導体を主として有する光電変換層を順次積層する例について説明する。図4～図7は、本実施形態の太陽電池パネルの製造方法を示す概略図である。

[0082] (1)図4(a):

基板1としてソーダフロートガラス基板(1．4m×1．1m×板厚:4mm)を使用する。基板端面は破損防止にコーナー面取りやR面取り加工されていることが望ましい。

[0083] (2)図4(b):

前記実施形態に基づき、基板1上に透明電極層2を製膜し、透明電極付き基板を形成する。透明導電層2として，透明電極膜に加えて、基板1と透明電極膜との間にアルカリバリア膜(図示されず)を形成しても良い。アルカリバリア膜は、酸化シリコン膜(SiO_2)を50nm以上150nm以下、熱CVD装置にて約500℃で製膜処理する。

[0084] (3)図4(c):

その後、基板1をX－Yテーブルに設置して、YAGレーザーの第1高調波(1064nm)を、図の矢印に示すように、透明電極膜の膜面側から入射する。加工速度に適切となるようにレーザーパワーを調整して、透明電極膜を発電セル5の直列接続方向に対して垂直な方向へ、基板1とレーザー光を相対移動して，溝10を形成するように幅約6mm以上12mm以下の短冊状にレーザーエッチングする。

[0085] (4)図4(d):

プラズマCVD装置により、減圧雰囲気:30Pa以上150Pa以下、基板温度:約200℃、プラズマRF発生周波数:13MHz以上100MHz以下にて光電変換層3の第1セル層(トップ層)91として、非晶質シリコン薄膜からなるp層膜／i層膜／n層膜を順次製膜する。第1セル層91は，SiH_4ガスとH_2ガスとを主原料に，透明導電層2の上に製膜される。太陽光の入射する側からp層、i層、n層がこの順で積層される。

[0086] 本実施形態において、第1セル層91のp層は、SiH_4, H_2, CH_4, B_2H_6ガスをRFプラズマで反応生成させた、非晶質のBドープSiC膜であり、膜厚は4nm以上16nm以下とすることが好ましい。第1セル層91のi層は、SiH_4とH_2をRFプラズマで反応生成させた，非晶質Si膜であり、膜厚は100nm以上400nm以下とすることが好ましい。第1セル層91のn層は、SiH_4, H_2, PH_3ガスをRFプラズマで反応生成させた、結晶

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成分を含むSi膜であり、n層単膜のラマン比は2以上であり、膜厚は10nm以上80nm以下とすることが好ましい。なお、ここで「ラマン比」とはラマン分光評価で520cm^{-1}の結晶Siの強度と480cm^{-1}の非晶質Siの強度の比（結晶Siの強度／非晶質Siの強度）をいう（以下同じ）。また、前記p層（SiC膜）とi層（Si膜）の界面でのバンド不整合を抑制するために、バッファー層（図示略）として，バンドギャップが中間の物質を挿入しても良い。

[0087] 次に、第1セル層91の上に、プラズマCVD装置により、減圧雰囲気：3kPa以下，基板温度：約200℃、プラズマRF発生周波数：40MHz以上200MHz以下にて、第2セル層（ボトム層）92としての微結晶シリコン薄膜からなる微結晶p層膜／微結晶i層膜／微結晶n層膜を順次製膜する。

[0088] 本実施形態において，第2セル層92のp層は、SiH_4，H_2，B_2H_6ガスをRFプラズマで反応生成させた、結晶成分を含むSi膜であり、p層単膜のラマン比は2以上であり、膜厚は10nm以上60nm以下とすることが好ましい。第2セル層92のi層は、SiH_4とH_2をRFプラズマで反応生成させた，結晶成分を含むSi膜であり、このi層を1．5μm膜厚に積んだときのラマン比は3．0以上8．0以下であり，膜厚は1200nm以上2000nm以下とすることが好ましい。より好ましくは、ラマン比を3．5以上8．0以下、さらに好ましくは5．0以上8．0以下とすると好適である。ラマン比の下限値は，結晶シリコン部で発生した電荷が断面方向につながった結晶構造を導通することができるように、大部分の結晶構造が膜厚方向に連続するために必要なラマン比が3．0以上であることから決まり、これは断面観察により確認することができる。また、ラマン比の上限値は柱状結晶の粒界が電流リークポイントとなり、電圧が発生しなくなるのを抑制するために、非晶質で結晶粒界を充填することが好ましく、ラマン比が8．0以下であることが実験的に求められる。

[0089] 第2セル層92のn層は、SiH_4，H_2，PH_3ガスをRFプラズマで反応生成させた、結晶成分を含むSi膜であり、n層単膜のラマン比は2以上であり、膜厚は10nm以上80nm以下とすることが好ましい。

[0090] 微結晶シリコン薄膜、特に微結晶i層膜をプラズマCVD法で形成するにあたり、プラズマ放電電極と基板1の表面との距離dは、3mm以上10mm以下にすることが好ま

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しい。3mmより小さい場合、大型基板に対応する製膜室内の各構成機器精度から距離dを一定に保つことが難しくなるとともに、近過ぎて放電が不安定になる恐れがある。10mmより大きい場合、十分な製膜速度(1nm／s以上)を得難くなるとともに、プラズマの均一性が低下しイオン衝撃により膜質が低下する。第2セル層92のi層は、RF周波数40MHz以上200MHz以下、ガス圧力0.5kPa以上3kPa以下、製膜速度1nm／s以上3nm/s以下で製膜されることが好ましく、本実施形態においてはRF周波数60MHz、ガス圧力1.6kPa、製膜速度2nm／sで製膜される。

[0091] 第1セル層91と第2セル層92の間に電流整合性を取るために半反射膜となることを目的に、中間コンタクト層93として、膜厚0nm以上90nm以下のZnO系膜(例えばGZO(Gaドープ ZnO)膜)をスパッタリング装置により製膜して設けても良い。この中間コンタクト層93は、ZnO単膜での光吸収率がλ=450nm以上1000nm以下の範囲で1%未満であることが好ましい。

[0092] (5)図4(e)

基板1をX－Yテーブルに設置して、レーザーダイオード励起YAGレーザーの第2高調波(532nm)を、図の矢印に示すように、光電変換層3の膜面側から入射する。パルス発振:10kHz以上20kHz以下として加工速度に適切となるようにレーザーパワーを調整して、透明導電層2のレーザーエッチングラインの約100μm以上150μm以下の横側を狙い、溝11を形成するようにレーザーエッチングする。レーザーエッチングラインの位置は、逆転していなければ問題ないものであるが、位置決めの公差を考慮して、前記数値を狙ったものである。

[0093] (6)図5(a)

裏面電極層4としてAg膜をスパッタリング装置により減圧雰囲気、約150℃にて順次製膜する。裏面電極層4は本実施形態では、Ag膜を膜厚150nm以上で製膜し、さらにn層と裏面電極層4との接触抵抗低減と光反射向上を目的に、光電変換層3と裏面電極層4との間に膜厚10nm以上のZnO系膜(例えばGZO(Gaドープ ZnO)膜)をスパッタリング装置により製膜して設ける。

[0094] (7)図5(b)

基板1をX－Yテーブルに設置して、レーザーダイオード励起YAGレーザーの第2

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高調波(532nm)を、図の矢印に示すように、基板1側から入射する。レーザー光が光電変換層3で吸収され、このとき発生する高いガス蒸気圧を利用して裏面電極層4が爆裂して除去される。パルス発振:1kHz以上10kHz以下として加工速度に適切となるようにレーザーパワーを調整して、透明導電層2のレーザーエッチングラインの約250μm以上400μm以下の横側を狙い、溝12を形成するようにレーザーエッチングする。レーザーエッチングラインの位置は、逆転していなければ問題ないものであるが、位置決めの公差を考慮して、前記数値を狙ったものである。

[0095] (8)図5(c)

発電領域を区分して、基板端周辺の膜端部においてレーザーエッチングによる直列接続部分が短絡し易い影響を除去する。基板1をX-Yテーブルに設置して、レーザーダイオード励起YAGレーザーの第2高調波(532nm)を、基板1側から入射する。レーザー光が透明導電層2と光電変換層3で吸収され、このとき発生する高いガス蒸気圧を利用して裏面電極層4が爆裂して、裏面電極層4/光電変換層3/透明導電層2が除去される。パルス発振:1kHz以上10kHz以下として加工速度に適切となるようにレーザーパワーを調整して、基板1の端部から5mm以上15mm以下の位置を、X方向絶縁溝15を形成するようにレーザーエッチングする。このとき、Y方向絶縁溝は後工程で基板1周囲領域の膜面研磨除去処理を行うので、設ける必要がない。

絶縁溝15は基板1の端より5mm以上10mm以下の位置にてエッチングを終了させることにより、太陽電池パネル端部からの太陽電池モジュール6内部への外部湿分侵入の抑制に、有効な効果を呈するので好ましい。

[0096] (9)図6(a)

後工程のEVA等を介したバックシートとの健在な接着・シール面を確保するために、基板1周辺(周囲領域14)の積層膜は、段差があるとともに剥離し易いため、この膜を除去する。まず、基板の端から5mm以上20mm以下で、前述の図5(c)工程で設けた絶縁溝15よりも基板端側における裏面電極層4/光電変換層3/透明導電層2において、砥石研磨やブラスト研磨などを用いて除去を行う。研磨屑や砥粒は基板1を洗浄処理して除去した。

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[0097] (10)図6(b)

端子箱取付け部分はバックシートに開口貫通窓を設けて集電板を取出す。この開口貫通窓部分には絶縁材を複数層を設置して外部からの湿分などの浸入を抑制する。

直列に並んだ一方端の太陽電池発電セル5と、他方端部の太陽電池発電セル5とから銅箔を用いて集電して太陽電池パネル裏側の端子箱部分から電力が取出せるように処理する。銅箔は各部との短絡を防止するために銅箔幅より広い絶縁シートを配置する。

集電用銅箔などが所定位置に配置された後に、太陽電池モジュール6の全体を覆い、基板1からはみ出さないようにEVA(エチレン酢酸ビニル共重合体)等による充填材シートを配置する。

EVAの上に、防水効果の高いバックシート21を設置する。バックシート21は本実施形態では防水防湿効果が高いようにPTEシート/AL箔/PETシートの3層構造よりなる。

バックシート21までを所定位置に配置したものを、ラミネータにより減圧雰囲気で内部の脱気を行い約150℃でプレスしながら、EVAを架橋させて密着させる。

[0098] (11)図7(a)

太陽電池モジュール6の裏側24に端子箱を接着剤で取付ける。

[0099] (12)図7(b)

銅箔と端子箱の出力ケーブル23とをハンダ等で接続し、端子箱内部を封止剤(ポッティング剤)で充填して密閉する。これで太陽電池パネル50が完成する。

[0100] (13)図7(c)

図7(b)までの工程で形成された太陽電池パネル50について発電検査ならびに、所定の性能試験を行う。発電検査は、AM1.5、全天日射基準太陽光(1000W/m^2)のソーラシミュレータを用いて行う。

[0101] (14)図7(d)

発電検査(図7(c))に前後して、外観検査をはじめ所定の性能検査を行う。

[0102] 上記実施形態では太陽電池として、トップセルとして非晶質(アモルファス)シリコン

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系光電変換層を有し、ボトムセルとして結晶質(微結晶)シリコン系光電変換層を有するタンデム型太陽電池を用いたものについて説明したが、本発明は、この例に限定されるものではない。

例えば、光電変換層として微結晶シリコンをはじめとする結晶質シリコン系光電変換層のみを有するシングル型太陽電池や、前記トップセルと前記ボトムセルに加えてさらに1層もしくは2層以上の別の光電変換層を設けた多接合型太陽電池のような他の種類の薄膜太陽電池にも同様に適用可能である。

[0103] [実施例及び比較例]

比較例1:

透明電極付き基板として、不連続な複数の山部によるマクロな凹凸(テクスチャ)は形成せず、ミクロの多数の凹凸(テクスチャ)を有する、一層のテクスチャ構造を用いた。ミクロの多数の凸部の底面径が0.2～0.3μm、凸部の高さは0.1～0.2μmであり、高さ／底面径の比が0.7～1.0であった。分光ヘイズ率は、波長550nmにおいて20%、波長800nmでは4%である。一層のテクスチャ構造の透明電極付き基板を用いた以外は、本発明の前記実施形態に従って、タンデム型太陽電池を作製した。

透明電極付き基板上に形成した各層において、トップセルp層は膜厚8nm、トップセルn層は膜厚40nm、ボトムセルp層は膜厚30nm、ボトムセルn層は膜厚30nm、裏面電極のZnO層は膜厚80nm、裏面電極のAg層は膜厚300nmで、各比較例及び実施例において共通とした。本例のトップセルi層、ボトムセルi層の膜厚は、表1に示す通りとし、中間コンタクト層は形成しなかった。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を2μmに設定した本例の太陽電池の発電効率初期値は12.0%だった。なお、このときのボトムセルi層の膜厚は、基板上の太陽電池として構成される領域における膜厚分布を考慮して、その平均値で評価したものである。

なお、表2において、電池性能評価項目であるIsc、Voc、FF、Effは、それぞれ短絡電流、開放電圧、形状因子、発電効率(初期値)を表す。Iscの(a－Si／c－Si)は、分光感度から求めたa－Si(非晶質)トップセルのIsc及びc－Si(結晶系)ボトムセルのIscである。タンデムのIscはトップセルIscとボトムセルIscの低い方で律速される

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。本実施例及び比較例は、ボトムセル律速であり、ボトムセルのIscがタンデムのIscとなっている。また、表2に示す比較例及び実施例において、電池性能評価結果は、比較例1を1とした相対値で記載する。本結果は、劣化前の初期値を記載したが、劣化率は本試験の範囲内では同等と考えられ、相対値で表すなら劣化後も同等である。

[0104] 比較例2:

トップセルi層、中間コンタクト層、ボトムセルi層を表1に示す膜厚で形成した以外は前記比較例1と同様の方法に従って、タンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚250nmとZnO中間コンタクト層の膜厚50nmに対し、ボトムセルi層の膜厚を2μmに設定した本例の太陽電池の発電効率初期値は12.0%だった。

[0105] 比較例3:

トップセルi層、ボトムセルi層を表1に示す膜厚で形成した以外は前記比較例1と同様の方法に従って、タンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を1.5μmに設定した本例の太陽電池の発電効率初期値は10.8%に低下した。これは、発電電流が大幅に低下したためであり、比較例で用いた基板ではボトムセル膜厚が2μmなければ所望の電流が得られないということが分かった。

[0106] 実施例1:

本発明の前記実施形態に従って、タンデム型太陽電池を作製した。透明電極付き基板として、不連続な小山部とミクロの多数の凸部を有する層状のSnO_2を積層したダブルテクスチャ構造の基板(山部の高さ500nm、山部の密度は10μm角に30個)を適用した。本例のトップセルi層、ボトムセルi層の膜厚は、表1に示す通りとし、中間コンタクト層は形成しなかった。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を2μmに設定した本例の太陽電池の発電効率初期値は13.3%に向上できた。これは、ボトムセルの電流を大幅に増大できた効果である。

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本発明においては、ダブルテクスチャ構造の透明電極により、山部による大きな凹凸(マクロな凹凸)と、これよりも小さな凹凸(ミクロな凹凸)とすることにより、大きな凹凸である山部により長波長の光を散乱し、小さな凹凸表面より短波長の光を散乱することができる。このため、透明電極全体として広い波長領域の光において高い光散乱性を達成することができる。また山部による大きな凹凸があるため、太陽電池層の裏面電極にまで大きな凹凸形状が発生する。これにより、裏面電極からの反射光が太陽電池層内で有効に散乱するので、ボトムセルの電流を大幅に増大させることができる。

特に本発明においては、透明電極の山部の高さと密度を制御して太陽電池層の膜厚を最適化したので、長波長の光の散乱を最適化して、結晶質シリコン系半導体からなる光電変換層の発電効率が向上している。

[0107] 実施例2:

トップセルi層、ボトムセルi層を表1に示す膜厚で形成した以外は前記実施例1と同様の方法に従って、実施例2(1)のタンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を1.5μmに設定した本例の太陽電池の発電効率初期値は12.8%であり、比較例1に対し効率向上とボトムセル膜厚の25%薄膜化を同時に達成できた。本実施形態による透明電極付き基板の適用により、実施例1に記載したものと同様な効果によりボトムセルを薄膜化しても高い発電電流が得られ、ボトムセルを薄膜化できたためにVocとFFを向上できたためである。また、ボトムセルi層を薄膜化により、ボトムセルi層が厚かったためにこの製膜時間によって律速されていた光電変換装置の製造時間を大幅に短縮することができる。これにより、高速製膜との相乗効果で光電変換装置の生産性を向上させることができる。

さらに、電池性能のボトムセルi層膜厚依存性を調べるために、前記実施例2(1)のボトムセルi層の膜厚を変えて実施例2(2)～実施例2(5)のタンデム型太陽電池を作製した。各実施例におけるボトムセルi層の膜厚を表1に示す。また、各実施例の太陽電池の電池性能を表2に示す。

実施例2において、ボトムセルi層の膜厚が1.2μm以上2.4μm以下の範囲で、

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比較例1のボトムセルi層膜厚が2μmの場合と同等以上の効率が得られた。ボトムセルi層の膜厚のさらに好ましい範囲は1．5μm以上2μm以下である。

低下するのを抑制でき)VocとFFを向上できたためである。

[0108] 実施例3:

トップセルi層、中間コンタクト層、ボトムセルi層を表1に示す膜厚で形成した以外は前記実施例2(1)と同様の方法に従って、タンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表2に示す。トップセルi層の膜厚250nmとZnO中間コンタクト層の膜厚50nmに対し、ボトムセルi層の膜厚を1．5μmに設定した本例の太陽電池の発電効率初期値は12．8%だった。効率向上とボトムセル薄膜化を同時に達成できた。

[0109] 実施例4:

透明電極付き基板の山部の高さを表1に示す値に変えた以外は実施例2(1)と同様の方法に従って、実施例4(1)～実施例4(5)のタンデム型太陽電池を作製し、山部の高さと電池性能の関係を調べた。

得られた太陽電池の電池性能を表2に示す。山部の高さは0．4μm以上0．7μm以下が適正であった。山部の高さが0．4μm以上で高い発電電流が得られ、0．7μmを超えるとVocとFFが著しく低下するためである。

[0110] 実施例5:

透明電極付き基板の山部の密度を表1に示す値に変えた以外は実施例2(1)と同様の方法に従って、実施例5(1)～実施例5(6)のタンデム型太陽電池を作製し、山部の密度と電池性能の関係を調べた。

得られた太陽電池の電池性能を表2に示す。山部の密度が10μm角内に15個以上50個以下のとき、比較例1のi層膜厚2μmの場合と同等以上の効率が得られる。さらに好ましい範囲は10μm角内に20個以上45個以下である。密度が低すぎるとJsc(電流密度)が低下し、高すぎるとJscは飽和しVocとFFが低下して、効率が低下する。

[0111] [表1]

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		透明電極付き基板の山部	トップセルi層膜厚	中間層	ボトムセルi層膜厚	ボトムセルm層製膜後ラマン比
比較例1		—	300nm	なし	2μm	6.5
比較例2		—	250nm	50nm	2μm	6.5
比較例3		—	300nm	なし	1.5μm	5.8
実施例1		高さ0.5μm,密度30	300nm	なし	2μm	6.5
実施例2	(1)	高さ0.5μm,密度30	300nm	なし	1.5μm	5.8
	(2)		↑	↑	1μm	6.0
	(3)		↑	↑	1.2μm	5.4
	(4)		↑	↑	1.7μm	6.2
	(5)		↑	↑	2.4μm	6.8
実施例3		高さ0.5μm,密度30	250nm	50nm	1.5μm	5.8
実施例4	(1)	高さ0.4μm,密度30	300nm	なし	1.5μm	5.8
	(2)	高さ0.5μm,密度30	↑	↑	↑	5.8
	(3)	高さ0.6μm,密度30	↑	↑	↑	5.8
	(4)	高さ0.7μm,密度30	↑	↑	↑	5.8
	(5)	高さ0.9μm,密度30	↑	↑	↑	5.8
実施例5	(1)	高さ0.5μm,密度10	300nm	なし	1.5μm	5.8
	(2)	高さ0.5μm,密度15	↑	↑	↑	5.8
	(3)	高さ0.5μm,密度20	↑	↑	↑	5.8
	(4)	高さ0.5μm,密度30	↑	↑	↑	5.8
	(5)	高さ0.5μm,密度45	↑	↑	↑	5.8
	(6)	高さ0.5μm,密度50	↑	↑	↑	5.8

[0112] [表2]

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		電池性能			
		Isc (a-Si/c-Si)	Voc	FF	Eff
比較例1		1 (1/1)	1	1	1
比較例2		1 (1/1)	1	1	1
比較例3		0.89(1/0.89)	1	1	0.89
実施例1		1.15(1/1.15)	0.99	0.97	1.11
実施例2	(1)	1.06(1/1.06)	1.00	1.01	1.07
	(2)	0.80(1/0.80)	1.02	1.04	0.86
	(3)	0.96(1/0.96)	1.01	1.02	0.99
	(4)	1.03(1/1.03)	0.99	1.01	1.03
	(5)	1.13(1/1.13)	0.97	0.92	1.02
実施例3		1.06(1/1.06)	1.00	1.01	1.07
実施例4	(1)	1.00(1/1.00)	1.01	1.01	1.02
	(2)	1.06(1/1.06)	1.00	1.01	1.07
	(3)	1.08(1/1.08)	0.99	0.99	1.06
	(4)	1.10(1/1.10)	0.97	0.96	1.03
	(5)	1.10(1/1.10)	0.92	0.88	0.90
実施例5	(1)	0.93(0.9/0.9)	1.00	0.99	0.92
	(2)	0.99(1/0.99)	1.00	1.00	0.99
	(3)	1.04(1/1.04)	1.00	1.01	1.05
	(4)	1.06(1/1.06)	1.00	1.01	1.07
	(5)	1.06(1/1.06)	0.98	0.98	1.02
	(6)	1.05(1/1.05)	0.97	0.96	0.98

[0113] 第2実施形態

以下に、本発明の第2実施形態について、説明する。

本実施形態において、透明電極つき基板は、大型の凹凸と小型の凹凸が混在する

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ことが望ましく、小型の凹凸(ミクロな凹凸)と大型の凹凸(マクロな凹凸)により、ピッチが0．1μmから1．2μm、高さが0．1μmから1．0μmの凹凸が混在している。ピッチ0．8μm以上の大きな凹凸により800nm以上の長波長の光を拡散、閉じ込めでき、ピッチ0．3μm以下の小さな凹凸により500nm以下の短波長の光も有効に散乱、利用できる。すなわち、大きな凹凸により長波長の光を散乱し、小さな凹凸表面より短波長の光を散乱することができるため、全体として高い光散乱性を達成することができる。また分光ヘイズ率が550nm以上800nm以下の波長で20%以上である。

[0114] 本実施形態においても、透明電極つき基板は、第1実施形態と同様であり、透明電極つき基板は、大型の凹凸(マクロな凹凸)の山部112の平均の高さHa(平坦部上のミクロの凸部の頂部からの高さの平均値)が、0．4μm以上0．7μm以下であり、0．5μm以上0．6μm以下であることがより好ましい。山部の密度は、基板111面の10μm角あたり15以上50以下となり、この平均ピッチPaは、1．0μm以上3μm以下に相当する。一方、小型の凹凸(ミクロな凹凸)のミクロの多数の凸部の底面径が0.1μm以上0.3μm以下であり、高さ／底面径の比が0.7以上1.2以下である。

[0115] 前記透明電極付き基板におけるこのような表面性状は、例えば、前記第1実施形態で説明した表面形状の解析を行うことにより確認することができる。

[0116] また、このような形状及び構成を有する透明電極付き基板は、基板全体において、550nm以上800nm以下の波長における分光ヘイズ率が20%以上、好ましくは30%以上であることが好ましい。

ここで、「分光ヘイズ率」の定義は、上記第1実施形態において説明したとおりである。

[0117] 以下に、上述した本実施形態の透明電極付き基板の形状及び構成ならびに特性を満たす基板(透明基板)及び酸化物は、それぞれ前記第1実施形態で説明した基板および第1酸化物と同様であるので、これらの詳しい説明は省略する。

[0118] 本実施形態の透明電極付き基板は、大型の凹凸と小型の凹凸が混在することが望ましく、ピッチが0.1μmから1.2μm、高さが0.1μmから1．0μmの凹凸が混在している。ピッチ0.8μm以上の大きな凹凸により800nm以上の長波長の光を拡散、閉じ込めでき、ピッチ0.3μm以下の小さな凹凸により500nm以下の短波長の光も有効

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に散乱、利用できる。また、膜全体のシート抵抗が8Ω／□以上20Ω／□以下であることが好ましく、8Ω／□以上12Ω／□以下であることがより好ましく、550nmにおける透過率（透明性）は、浸液法で測定した場合、80%以上90%以下であることが好ましく、85%以上90%以下であることがより好ましい。

[0119] また、本実施形態の透明電極付き基板を、光電変換装置の透明電極に用いると、基板を経て入射された光は、透明電極により屈折、散乱されて光電変換部に入射し、光電変換部中を長い距離にわたって通過する。その結果、多くの光が光電変換部にて吸収され、光電変換効率が向上する効果を奏するものとなる。特に、太陽電池に用いた場合には、開放電圧及び曲線因子を低下させずに短絡電流を高く維持することが可能となるため、光電変換効率が向上するものとなる。

[0120] 本実施形態の光電変換装置の製造方法により製造される光電変換装置の構成および太陽電池パネルの製造方法は、後述の異相遮断層または異相防止層を設けたこと以外は前記第1実施形態と同様であるので、第1実施形態で用いた図1および図4ないし図7を参照する。前記第1実施形態と共通の部材については同一の参照符号を用いることとし、詳細な説明は省略する。

[0121] 本実施形態の光電変換装置においては、非晶質シリコン系半導体を主として有する光電変換層からなる第1セル層（トップ層）91の透明電極層側表面から裏面電極層側表面に貫通する異相を遮断または防止するために、後述の光電変換装置の製造方法に係る実施形態に示した方法により、第1セル層（トップ層）91中に異相遮断層（図示略）が設けられるか、もしくは、基板1と第1セル層（トップ層）91の間に異相防止層（図示略）が設けられる。

第1セル層（トップ層）91及び結晶質シリコン系半導体を主として有する光電変換層からなる第2セル層（ボトム層）92の間には、透明導電膜からなる中間コンタクト層93を設けても良い（但し、本発明の光電変換装置は、中間コンタクト層93を設けたものに限定されない）。

[0122] 本実施形態の太陽電池パネルの製造方法においては、まず、前記第1実施形態の図4の（a）および（b）と同様の方法を行い、透明電極基板が形成される。

[0123] 次に、製膜した透明電極層2の表面に対してイオン処理を行い、本実施形態の異

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相防止層を形成することができる。イオン処理は、例えば真空中でのアルゴンイオン照射によるイオンエッチングとすることができる。イオン処理に用いられる装置としては、フィラメントタイプのイオン源を使用したイオンミリング装置が挙げられる。この装置を用いてイオン処理を行う場合は、例えば容器内を10^{-4}Pa台に真空排気し、アルゴンガスを供給して5×10^{-3}Paの条件で、Arイオンを発生させ、加速電圧1kVでイオン照射してイオン処理を行うことができる。イオンは透明電極付き基板の透明電極層2表面に垂直に照射することが好ましい。照射時間は例えば180sec程度とすることができる。

[0124] 次に、前記第1実施形態の図4の(e)と同様の方法により透明電極膜のレーザーエッチングを行い、次いで異相遮断層または異相防止層を設けたこと以外は図4の(d)と同様の方法を行い、光電変換層3を形成する。

光電変換層3の第1セル層(トップ層)91として、非晶質シリコン薄膜からなるp層膜／i層膜／n層膜を順次形成する。太陽光の入射する側からp層, i層、n層がこの順で積層される。

なお、第1セル層91を製膜する前に、透明電極付き基板を真空容器で10^{-1}Pa以下の圧力とし、ヒータで100℃以上の温度に予備加熱(ベーキング)することが、異相の発生を防ぐために特に好ましい。

[0125] 本実施形態において、第1セル層91のp層は、SiH_4, H_2, CH_4, B_2H_6ガスをRFプラズマで反応生成させた、非晶質のBドープSiC膜であり、膜厚は4nm以上16nm以下とすることが好ましい。

[0126] また本実施形態において、第1セル層91のi層は、標準構成としては非晶質Si膜であり、SiH_4とH_2をRFプラズマで反応生成される。膜厚は100nm以上400nm以下とすることが好ましい。標準の製膜条件として、SiH_4とH_2を1:5の比率で供給して圧力を600Paに制御し、60MHzの高周波0．15W／cm^3で放電して、非晶質のi層を製膜することができる。この標準の製膜条件における製膜速度は、例えば1．1nm／sとすることができる。

[0127] 本実施形態の異相遮断層として、第1セル層91のi層中に、標準製膜条件よりも低パワーで製膜された層(例えば、i層製膜の初期に製膜される初期層、あるいはi層製

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膜の後期に製膜される後期層）を設けてもよい。このような層を製膜する場合は、高周波出力を例えば0．02W／cm^2の低パワーにして、低速で製膜すればよい。製膜速度は例えば0．2nm／s程度である。初期層及び後期層は、例えば60s（膜厚12nm相当）～120s（膜厚24nm相当）で製膜される。初期層または後期層を設けたi層は、プラズマ放電中にパワーを変更することにより、連続膜として形成される。

[0128] また本実施形態において、第1セル層91（トップ層）のn層は、標準構成としては結晶質（結晶成分を含む）のSi膜であり，SiH_4，H_2，PH_3ガスをRFプラズマで反応生成される。このn層単膜のラマン比は2以上であり、膜厚は10nm以上80nm以下とすることが好ましい。標準の製膜条件として、SiH_4とH_2とPH_3を1：80：0．02の比率で供給して圧力を100Paに制御し、基板と電極の間の間隔を20mmとし、60MHzの高周波0．3W／cm^2で放電して、微結晶（結晶とアモルファスが混在する膜質）のn層を製膜することができる。製膜速度は0．2nm／sとすることができる。製膜速度は例えば0．2nm／s程度とすることができる。

[0129] 本実施形態の異相遮断層として非晶質（結晶成分は存在しない）のn層を形成してもよい。この場合は、前記結晶質のn層の前に非晶質のn層が製膜される。この非晶質n層は、SiH_4とH_2とPH_3を1：1：0．05の比率で供給して圧力を20Paに制御し、基板と電極の間の間隔を20mmとし、60MHzの高周波を0．04W／cm^2で放電して製膜される。製膜速度は例えば0．2nm／s程度とすることができる。非晶質Si－n層と微結晶Si－n層を積層するときは、一旦放電を停止して流量／圧力を変更し、安定後再度放電させて行われる。例えば、非晶質Si製膜条件で15nm程度製膜し、さらに標準の結晶質製膜条件で25nm程度製膜すればよい。

[0130] 本実施形態の異相遮断層として、結晶質（結晶成分を含む）のn層を標準製膜条件より高圧で製膜してもよい。この場合は、例えば、SiH_4とH_2とPH_3を1：80：0．02の比率で供給して、圧力を200Paに制御し、基板と電極の間の間隔を標準条件の1／2である10mmに狭くして、60MHzの高周波を出力0．1W／cm^2で放電して、微結晶Si（結晶とアモルファスが混在する膜質）のn層を製膜することができる。

[0131] 本実施形態において，前記p層膜とi層膜の間には界面特性の向上のためにバッファー層（図示略）を設けてもよい。バッファー層として、バンドギャップが中間の物質を

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挿入することにより、p層(SIC膜)とi層(Si膜)の界面でのバンド不整合を抑制することができる。

本実施形態において、p層の製膜ガス(SiH_4、H_2、CH_4、B_2H_6)に対し、i層ではSiH_4及びH_2しか用いないため、ドーパント(B_2H_6)濃度及びバンド調整のためのCH_4濃度を調整する。具体的には、p層製膜室において、B_2H_6ガスの供給を停止し、B_2H_6の供給は壁面吸着量のみとし、CH_4ガスの供給量をp層に対し1/10～1/3に調整することで0.02～0.1μmの膜厚のバッファー層を形成した。これにより、p層及びi層と原子拡散が進行した結果、膜厚方向の炭素含有率及びバンドエネルギー構造は滑らかに変化する状態となり、p層とi層との界面特性が向上されることとなる。

[0132] 次に、第1セル層(トップ層)91の上に、前記第1実施形態と同様の方法、製膜条件により、微結晶シリコン薄膜からなる微結晶p層膜／微結晶i層膜／微結晶n層膜を順次製膜し、前記第1実施形態と同様の第2セル層(ボトム層)92を形成する。

[0133] 前記第1実施形態と同様に、第1セル層(トップ層)91と第2セル層(ボトム層)92の間に電流整合性を取るために半反射膜となることを目的に、中間コンタクト層93として、膜厚0nm以上90nm以下、より好ましくは5nm以上50nm以下のZnO系膜(例えばGZO(Gaドープ ZnO)膜)をスパッタリング装置により製膜して設けても良い。この中間コンタクト層93は、ZnO単膜での光吸収率がλ＝450nm以上1000nm以下の範囲で1%未満であることが好ましい。

[0134] 第2セル層92を形成した後、第1実施形態における図4の(e)から図7の(b)と同様の方法により太陽電池パネル50が完成する。次いで第1実施形態における図7の(c)および(d)と同様の方法により、発電検査および所定の性能試験ならびに外観検査をはじめ所定の性能検査を行う。

[0135] 上記実施形態では太陽電池として、トップセルとして非晶質シリコン系光電変換層を有し、ボトムセルとして結晶質(微結晶)シリコン系光電変換層を有するタンデム型太陽電池を用いたものについて説明したが、本発明は、この例に限定されるものではない。

例えば、光電変換層として非晶質シリコン系光電変換層のみを有するシングル型太陽電池や、前記トップセルと前記ボトムセルに加えてさらに1層もしくは2層以上の

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別の光電変換層を設けた多接合型太陽電池のような他の種類の薄膜太陽電池にも同様に適用可能である。

[0136] 〔実施例、参考例及び比較例〕

参考例1：

透明電極付き基板として、微細な凹凸のみのものを用いた。微細な凹凸の凸部の高さは0．1μm以上0．2μm以下、ピッチは0．1μm以上0．3μm以下、凸部の高さと底面径の比は0．7～1．0，波長550nmの分光ヘイズ率は20%，800nmの分光ヘイズ率は3%であった。透明電極付き基板が異なる以外は，本発明の前記実施形態における標準の製膜条件に従って、タンデム型太陽電池を作製した。

[0137] 透明電極付き基板上に形成した各層において，トップセルp層は膜厚8nm、トップセルn層は膜厚40nm、ボトムセルp層は膜厚30nm、ボトムセルn層は膜厚30nm、裏面電極のZnO層は膜厚80nm、裏面電極のAg層は膜厚300nmで，各参考例、比較例及び実施例において共通とした。本例のトップセルi層、トップセルn層の膜厚及び製膜条件は，表3に示す通りとし、中間コンタクト層は形成しなかった。

[0138] なお、表3に記載した各参考例、比較例及び実施例の「製膜条件」とは、以下の通りである。

トップセルi層の標準製膜条件：SiH_4とH_2を1：5の比率で供給して、圧力を600Paに制御し，60MHzの高周波を出力0．15W／cm^2で放電して、非晶質i層を製膜した。製膜速度は1．1nm／sとした。

[0139] トップセルi層の初期層または後期層の低速製膜条件：標準条件と高周波出力のみを変更し，0．02W／cm^2とした。製膜速度は0．2nm／sとした。標準製膜条件による膜との積層は、プラズマ放電中にパワーを変更することにより、連続膜とした。

[0140] トップセルn層の標準製膜条件：SiH_4とH_2とPH_3を1：80：0．02の比率で供給して，圧力を100Paに制御し、基板と電極の間の間隔を7mmとし、60MHzの高周波を出力0．3W／cm^2で放電して，微結晶（結晶と非晶質が混在する膜質）のn層を製膜した。製膜速度は0．2nm／sとした。

[0141] トップセルn層の非晶質Si製膜条件：SiH_4とH_2とPH_3を1：1：0．05の比率で供給して、圧力を20Paに制御し、基板と電極の間の間隔を7mmとし、60MHzの高周波

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を出力0．04W／cm^{3}で放電して、非晶質Si(結晶成分は存在しない)のn層を製膜した。製膜速度は0．2nm／sとした。非晶質Si－n層と微結晶Si－n層を積層するときは、一旦放電を停止して流量／圧力を変更し、安定後再度放電させた。

[0142] トップセルn層の高圧製膜条件：SiH_4とH_2とPH_3を1:80:0．02の比率で供給して、圧力を200Paに制御し、基板と電極の間の間隔を標準条件の1／2である10mmに狭くして、60MHzの高周波を出力0．3W／cm^{3}で放電して、微結晶Si(結晶と非晶質が混在する膜質)のn層を製膜した。

[0143] 参考例1で得られた太陽電池の電池性能を表4に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を2μmに設定した本例の太陽電池の発電効率(初期値)は12%だった。

なお、表4において、電池性能評価項目であるIsc、Voc、FF、Effは、それぞれ短絡電流、開放電圧、形状因子、発電効率(初期値)を表す。また、表4に示す参考例、比較例及び実施例において、電池性能評価結果は、参考例1を1とした相対値で記載する。本結果は、劣化前の初期値を記載したが、劣化率は本試験の範囲内では同等と考えられ、相対値で表すなら劣化後も同等である。

[0144] 参考例2：

トップセルi層、ボトムセルi層を表3に示す膜厚で形成した以外は前記参考例1と同様の方法に従って、タンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表4に示す。トップセルi層の膜厚300nmに対し、ボトムセルi層の膜厚を1．5μmに設定した本例の太陽電池の発電効率は10．8%に低下した。これは、発電電流が大幅に低下したためであり、参考例で用いた基板ではボトムセル膜厚が2μmなければ所望の電流が得られないということが分かった。

[0145] 比較例4：

本発明の前記実施形態における標準の製膜条件に従って、タンデム型太陽電池を作製した。透明電極付き基板として、実施例6と同じく大小の凹凸が混在する基板を適用した。本例のトップセルi層、トップセルn層の膜厚及び製膜条件は、表3に示す通りとし、中間コンタクト層は形成しなかった。すなわち、トップセルi層は製膜速度1．

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1nm／sで300nmの膜厚に、トップセルn層は結晶と非晶質が混在する微結晶となる条件で40nmの膜厚に製膜した。ボトムセルi層の膜厚は1．5μmとした。

[0146] 得られた太陽電池の電池性能を表4に示す。表4に示したように、本例の太陽電池は、電流は増大したものの、開放電圧と形状因子が低下して、発電効率初期値は参考例1のボトムセルi層膜厚が2μmの場合より低下していた。

[0147] 比較例4の太陽電池において開放電圧と形状因子が低下した原因を調査検討した。図10に大小の凹凸が混在する透明電極付き基板を用いて作製したタンデム型太陽電池の断面の透過型電子顕微鏡写真を示す。この電子顕微鏡写真において、透明電極の谷の部分（点線で囲んだ部分）でトップセルを上下に貫通する線が見える。これは、下地の隣接する面に製膜・成長する膜成長相間の不連続な境界が線状に見えるのもで、異相と呼んでおり、キャリア再結合中心が集中すると考えられ、電流リーク箇所に相当する。この異相が生じた場合に開放電圧と形状因子が低下していた。従って、本発明者らは、この異相を抑制すること，または完全に抑制はできなくても透明電極から中間コンタクト層又はボトムセルに至るまでトップセルを貫通する異相を遮断できれば、開放電圧低下，形状因子低下を抑制できると考えた。

[0148] 実施例6～実施例9：

トップセルi層、トップセルn層の膜厚及び製膜条件を表3に示す通りとした以外は前記比較例4と同様の方法に従って、実施例6～実施例9のタンデム型太陽電池を作製した。

得られた太陽電池の電池性能を表4に示す。

[0149] 実施例6においては、トップセルの非晶質Si－i層を製膜初期（p層との界面）のみ低パワーで製膜することにより、開放電圧低下，形状因子低下を抑制し、太陽電池性能を向上できた。これは、非晶質Si－i層の初期層によってトップセルを貫通する異相が遮断され、電流リークを抑制することができたためと考えられる。ボトムセルが膜厚1．5μmという薄膜で発電効率初期値13.0%という高効率が得られたことは、生産性と効率向上の両方で非常に大きな成果である。

[0150] 実施例7においては、トップセルの非晶質Si－i層を製膜後期（n層との界面）のみ低パワーで製膜することにより、開放電圧低下、形状因子低下を抑制し、太陽電池

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性能を向上できた。これは、非晶質Si－i層の後期層によってトップセルを貫通する異相が遮断され、電流リークを抑制することができたためと考えられる。この実施例7でも、ボトムセルが膜厚1．5μmという薄膜で発電効率初期値13.0%という高効率が得られたことは、生産性と効率向上の両方で非常に大きな成果である。

[0151] 実施例8においては、トップセルn層の製膜後期のみを標準製膜条件により製膜して結晶質とし、製膜初期の層を非晶質にすることで、開放電圧低下、形状因子低下を抑制し、太陽電池性能を向上できた。これは、トップセルn層において非晶質とした初期層がi層との界面で異相を埋めるため、トップセルを貫通する異相が遮断され、電流リークを抑制することができたためと推察される。ボトムセル膜厚1.5μmの薄膜で発電効率初期値13.2%が得られたのは、実施例6、実施例7と同様の異相遮断効果と、更にn層による界面改善効果が得られたためである。

[0152] 実施例9においては、トップセルn層を200Paの高圧で製膜して微結晶膜を形成することにより、開放電圧低下、形状因子低下を抑制し、太陽電池性能を向上できた。なお、実施例9において、トップセルn層の製膜の際の圧力を400Paとした場合も同様の効果が得られた。これは、高圧で製膜することによりトップセルn層がi層との界面の谷の部分に付きやすくなり、これによってトップセルを貫通する異相が遮断され、電流リークを抑制することができたためと考えられる。

[0153] [表3]

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	トップセルi層の製膜条件と膜厚	トップセルn層の製膜条件と膜厚
参考例1	標準製膜条件で300nm	標準製膜条件で2μm
参考例2	標準製膜条件で300nm	標準製膜条件で1.5μm
比較例4	標準製膜条件で300nm	標準製膜条件(結晶質)で40nm
実施例6	初期層：低速製膜条件で24nm(120s)；続けて標準製膜条件で残り276nm	標準製膜条件(結晶質)で40nm
実施例7	標準製膜条件で276nm；さらに後期層として低速製膜条件で24nm(120s)	標準製膜条件(結晶質)で40nm
実施例8	標準製膜条件で300nm	非晶質Si製膜条件で15nm；さらに標準製膜条件で25nm
実施例9	標準製膜条件で300nm	高圧製膜条件(結晶質)で40nm

[0154] 実施例10:

透明電極付き基板の透明電極表面に対してイオン処理を行った以外は、前記比較例4と同様の方法に従って、実施例10のタンデム型太陽電池を作製した。

イオン処理は、真空中でのアルゴンイオン照射によるイオンエッチングであり、装置としては、フィラメントタイプのイオン源を使用したイオンミリング装置を用いた。容器内を10^{-4}Pa台に真空排気し、アルゴンガスを供給して5×10^{-3}Paの条件で、Arイオンを発生させ、加速電圧1kVでイオン照射してイオン処理を行った。イオンは透明電極付き基板の透明電極表面に垂直に照射し、照射時間は180secとした。図8は、イオン処理前における透明電極付き基板の透明電極表面の電子顕微鏡写真(倍率5万倍)であり、図9は、イオン処理後における透明電極付き基板の透明電極表面の電子顕微鏡写真(倍率5万倍)である。

[0155] 得られた太陽電池の電池性能を表4に示す。なお、表4において、電池性能評価項目であるIsc、Voc、FF、Effは、それぞれ短絡電流、開放電圧、形状因子、発電効率を表す。Iscの(a－Si／c－Si)は、分光感度から求めたa－Si(非晶質)トップセルのIsc及びc－Si(結晶系)ボトムセルのIscである。

実施例10においては、前記イオン処理により、開放電圧低下、形状因子低下を抑

制し、太陽電池性能を向上できた。これはイオン処理によって基板の凹形状が円滑になり、トップセルにおける異相の形成が抑制されたため、電流リークを抑制することができたためと考えられる。

実施例1～10においては、ボトムセルi層製膜条件は固定であり、ボトムセルn層製膜後のラマン比は表1に示すとおり、5.0～7.0の間にあった。

[0156] 実施例11；

ボトムセルi層のH_2/SiH_4希釈率比を表5に示すように変えた以外は、実施例1と同様の方法に従って実施例11(1)～実施例11(6)のタンデム型太陽電池を作製し、ボトムセルのn層製膜後のラマン比と太陽電池特性の関係を調べた。その結果を図12に示す。なお、表5、及び図12において、H_2希釈率比、及び電池性能結果は、比較例1を1とした場合の相対値である。本結果は、劣化前の初期値を記載したが、劣化率は本試験の範囲内では同等と考えられ、相対値で表すなら劣化後も同等である。

表5及び図12からわかるように、n層製膜後のラマン比でみて3.0以上8.0以下のとき、比較例1よりも太陽電池性能が向上している。これは、ラマン比が3.0より低下するとVocが向上する一方で、Iscが著しく低下していることから、非晶質成分が多すぎて抵抗損失が生じたと推定される。ラマン比が8.0より増大すると、VocとFFが大きく低下していることより電流リークによる電圧損失が生じたと考えられ、結晶粒界の電流リークが想定される。第2セル層において、適度な非晶質相が存在することにより、結晶質シリコンの粒界に存在する欠陥を不活性にし、これにより、Iscの低下を抑制することに寄与しているものと考えられる。

また、図12において、H_2希釈率比0．9でEffの上昇が緩和し、H_2希釈率比1．1でEffが低下している。H_2希釈率比0．9以上1．1以下でのEff値は、実施例11(3)～実施例11(5)に示すように、比較例1に対し1.1倍以上の性能を得ることができた。したがって、ラマン比は、H_2希釈率比と電池性能との相関関係からみて、実験的に5.0以上7.5以下が最適値となる。

[0157] [表4]

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	電池性能			
	Isc (a-Si/c-Si)	Voc	FF	Eff
参考例1	1 (1/1)	1	1	1
参考例2	0.89(1/0.89)	1	1	0.89
比較例4	1.10(1/1.10)	0.95	0.92	0.97
実施例6	1.10(1/1.10)	0.99	0.99	1.08
実施例7	1.10(1/1.10)	0.99	0.99	1.08
実施例8	1.10(1/1.10)	1.00	1.00	1.10
実施例9	1.10(1/1.10)	0.99	0.98	1.07
実施例10	1.03(1/1.03)	1.01	1.01	1.05

[0158] [表5]

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No	H2希釈率比	ラマン比	電池性能				
			(ターゲット) Isc	(c-Si) Isc	Voc	FF	Eff
実施例11(1)	0.8	2	0.98	0.98	1.03	0.95	0.96
実施例11(2)	0.8	3	1.03	1.03	1.01	1.00	1.04
実施例11(3)	0.9	5	1.11	1.11	1.00	0.99	1.10
実施例11(4)	1.0	6.5	1.15	1.15	0.99	0.97	1.11
実施例11(5)	1.1	7.5	1.17	1.17	0.98	0.96	1.10
実施例11(6)	1.2	10	1.15	1.15	0.94	0.89	0.96
比較例1	1.0	6.5	1.00	1.00	1.00	1.00	1.00(12%)

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[0159] 以上、実施例6から実施例11によれば、分光ヘイズ率を高めた透明電極付き基板を適用しても開放電圧と形状因子の低下を抑制でき、薄いボトムセルで、高効率と高生産性を兼ね備えたタンデム太陽電池を作製可能となった。

なお、トップセル(非晶質Si層)全体を低パワーで製膜すると製膜速度が著しく低下するため、生産性が悪化する。しかし、上記実施例6、実施例7のように初期あるいは後期の20%程度の膜厚を低速で作製するだけであれば、生産性の悪化を極力抑えられて、高い生産効率で太陽電池を製造できる。また、実施例9のようにn層の製膜条件を改善した場合は、生産性の悪化はまったくなく、高い生産効率で太陽電池を製造できる。

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請求の範囲

[1] 透明絶縁性の基板上に透明電極層を設けてなる透明電極付き基板と、該透明電極付き基板の透明電極層側に順次形成された、結晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも有してなる光電変換装置であって、

前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上であり、

前記結晶質シリコン系半導体を主として有する光電変換層の膜厚が1.2μm以上2μm以下、かつラマン比が3.0以上8.0以下である光電変換装置。

[2] 前記透明電極付き基板と前記結晶質シリコン系半導体を主として有する光電変換層との間に、非晶質シリコン系半導体を主として有する光電変換層を有する請求項1に記載の光電変換装置。

[3] 前記非晶質シリコン系半導体を主として有する光電変換層と前記結晶質シリコン系半導体を主として有する光電変換層との間に中間コンタクト層を有する請求項2に記載の光電変換装置。

[4] 前記透明電極付き基板の透明電極層表面が、複数の山部と複数の平坦部とで構成され、該山部及び該平坦部の表面がミクロの多数の凸部を連続して有してなり、

前記山部の前記基板面垂直方向における高さが0.4μm以上0.7μm以下であり、

基板面10μm角における前記山部の数が15以上50以下であり、

前記ミクロの多数の凸部の底面径が0.1μm以上0.3μm以下であり、高さ／底面径の比が0.7以上1.2以下である請求項1から請求項3のいずれか1項に記載の光電変換装置。

[5] 透明絶縁性の基板上に透明電極層を形成して透明電極付き基板を作製し、

該透明電極付き基板の透明電極層側に非晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも順次形成する光電変換装置の製造方法であって、

前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘ

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イズ率が550nm以上800nm以下の波長で20%以上であり、

前記非晶質シリコン系半導体を主として有する光電変換層中に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相を遮断する異相遮断層を形成する光電変換装置の製造方法。

[6] 前記非晶質シリコン系半導体を主として有する光電変換層の形成においてp層、i層、n層を順次形成し、

前記i層の形成において該i層の他の部分より低速で製膜することにより前記異相遮断層を形成する、請求項5に記載の光電変換装置の製造方法。

[7] 前記非晶質シリコン系半導体を主として有する光電変換層の形成においてp層、i層、n層を順次形成し、

前記n層の形成において少なくともその一部に非晶質の層を形成することにより前記異相遮断層を形成する、請求項5に記載の光電変換装置の製造方法。

[8] 前記非晶質シリコン系半導体を主として有する光電変換層の形成においてp層、i層、n層を順次形成し、

前記n層の形成において少なくともその一部を200Pa以上の圧力下で製膜することにより前記異相遮断層を形成する、請求項5に記載の光電変換装置の製造方法。

[9] 透明絶縁性の基板上に透明電極層を形成して透明電極付き基板を作製し、

該透明電極付き基板の透明電極層側に非晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも順次形成する光電変換装置の製造方法であって、

前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上であり、

前記透明電極層の形成と前記光電変換層形成の間に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相の形成を防止する異相防止層を形成する光電変換装置の製造方法。

[10] 前記透明電極層の凸部を円滑化して前記異相防止層を形成する、請求項9に記載の光電変換装置の製造方法。

[11] 前記透明電極層表面にイオン処理を施して前記異相防止層を形成する、請求項9

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または請求項10に記載の光電変換装置の製造方法。

[12] 前記非晶質シリコン系半導体を主として有する光電変換層と前記裏面電極の間に、結晶質シリコン系半導体を主として有する光電変換層を形成する請求項5から請求項11のいずれか1項に記載の光電変換装置の製造方法。

[13] 透明絶縁性の基板上に透明電極層を設けてなる透明電極付き基板と、該透明電極付き基板の透明電極層側に順次形成された、非晶質シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも有し、

前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上800nm以下の波長で20%以上である光電変換装置であって、

前記非晶質シリコン系半導体を主として有する光電変換層中に、該光電変換層の透明電極層側表面から裏面電極層側表面に貫通する異相を遮断する異相遮断層を設けた光電変換装置。

[14] 前記非晶質シリコン系半導体を主として有する光電変換層において、p層、i層、n層が順次形成され、

前記非晶質シリコン系半導体を主として有する光電変換層のn層が非晶質シリコン系半導体を主として有する層と、結晶質シリコン系半導体を主として有する層で形成される請求項2又は13に記載の光電変換装置。

[15] 前記非晶質シリコン系半導体を主として有する光電変換層のp層とi層との間にバッファー層を設けた請求項2, 13又は14に記載の光電変換装置。

[16] 前記非晶質シリコン系半導体を主として有する光電変換層と前記裏面電極層との間に結晶質シリコン系半導体を主として有する光電変換層を有する請求項13に記載の光電変換装置。

[17] 前記結晶質シリコン系半導体を主として有する光電変換層の膜厚が1.2μm以上2μm以下、かつラマン比が3.0以上8.0以下である請求項16に記載の光電変換装置。

[18] 前記非晶質シリコン系半導体を主として有する光電変換層と前記裏面電極の間に、結晶質シリコン系半導体、結晶質もしくは非晶質シリコンゲルマニウム系半導体を

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主として有する光電変換層を有する請求項13に記載の光電変換装置。

[19] 前記非晶質シリコン系半導体を主として有する光電変換層と前記裏面電極の間に、結晶質もしくは非晶質シリコン系半導体、結晶質もしくは非晶質シリコンゲルマニウム系半導体を主として有する光電変換層を複数有する請求項13に記載の光電変換装置。

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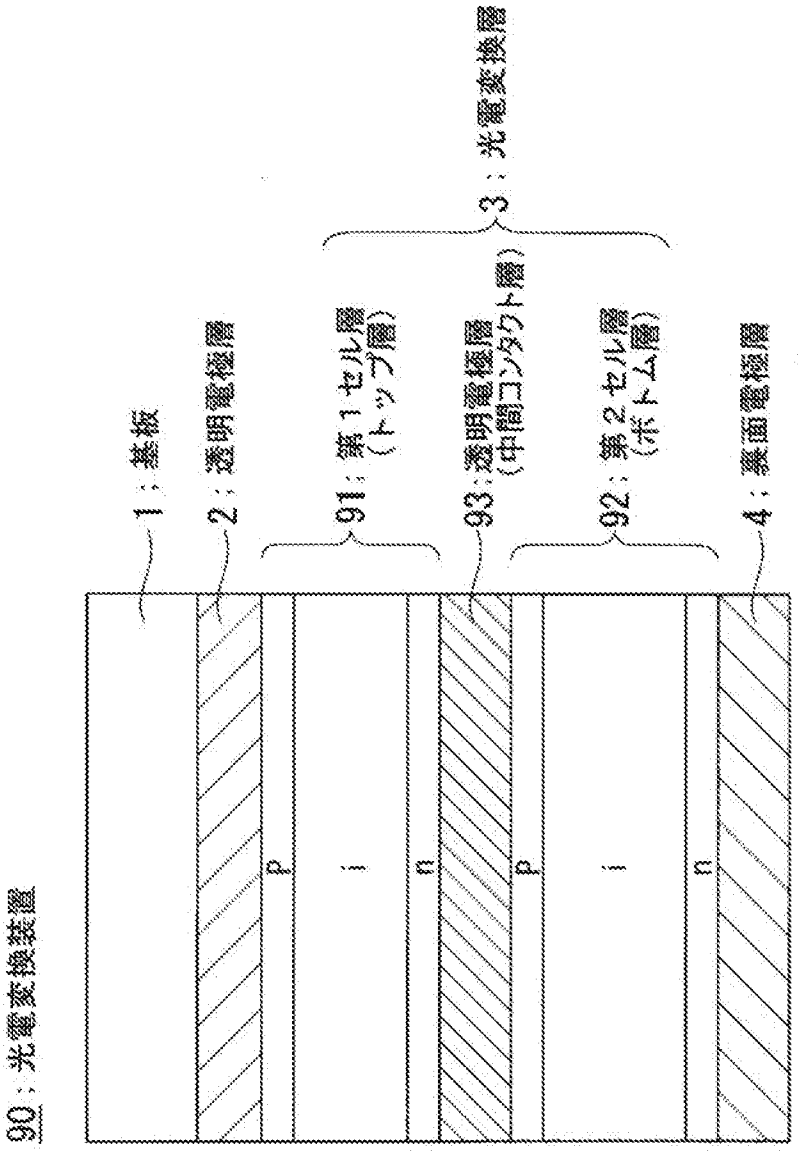
[図1]



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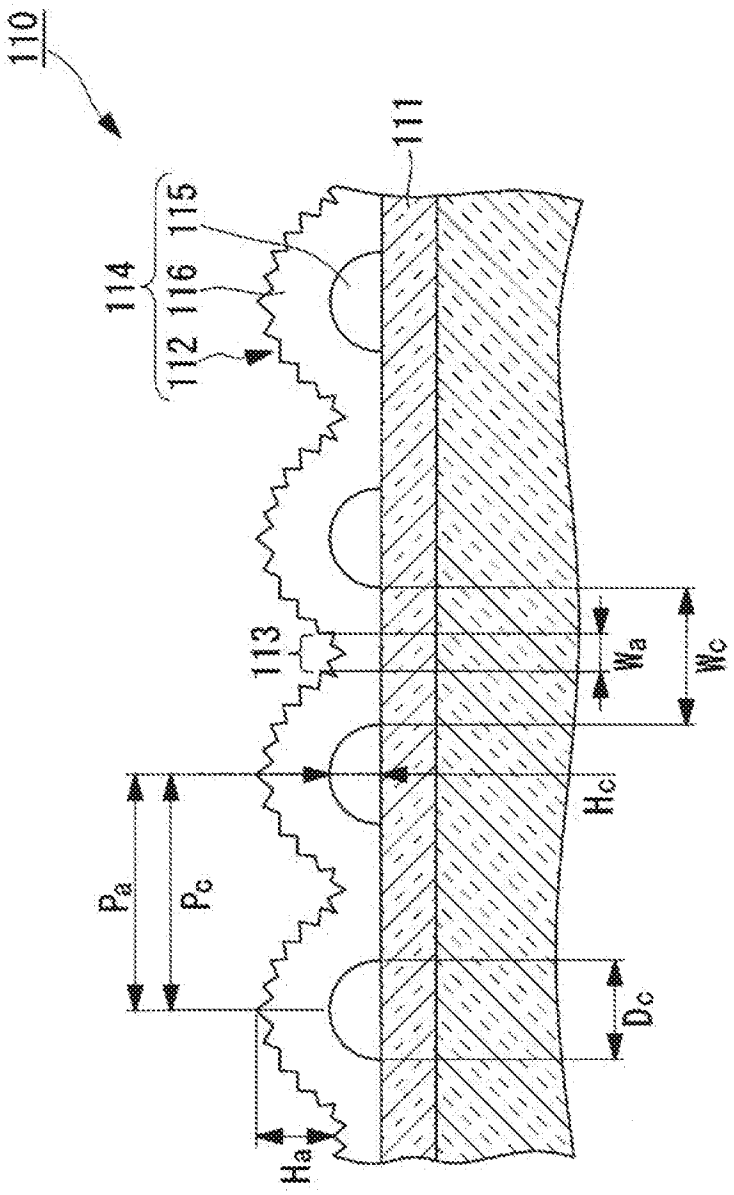
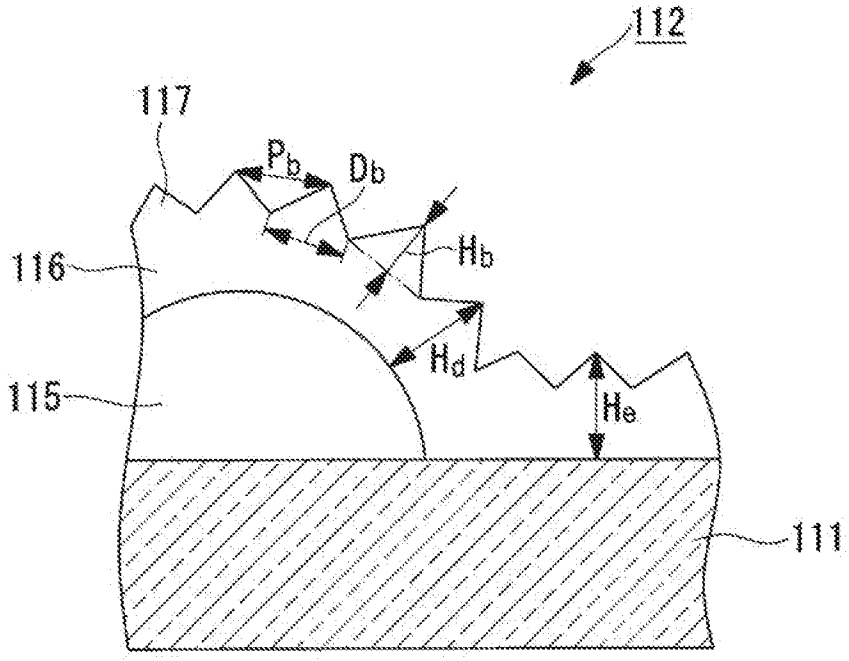
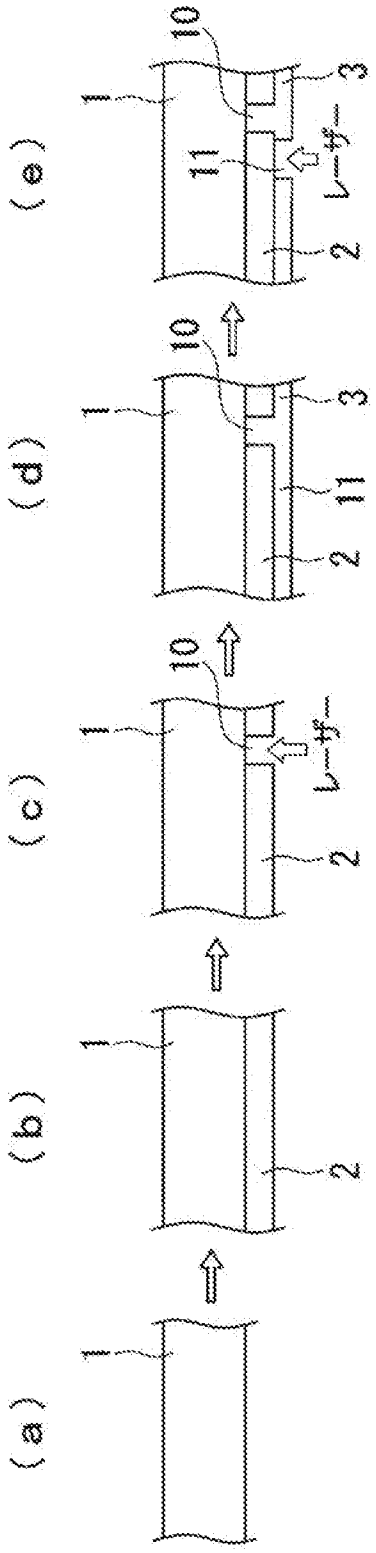
[図2]



[図3]



[図4]



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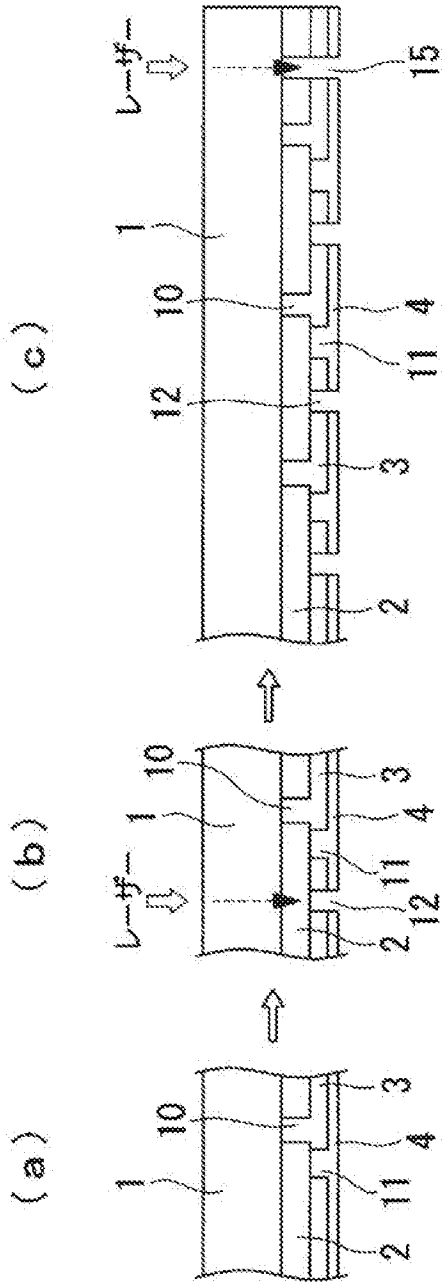
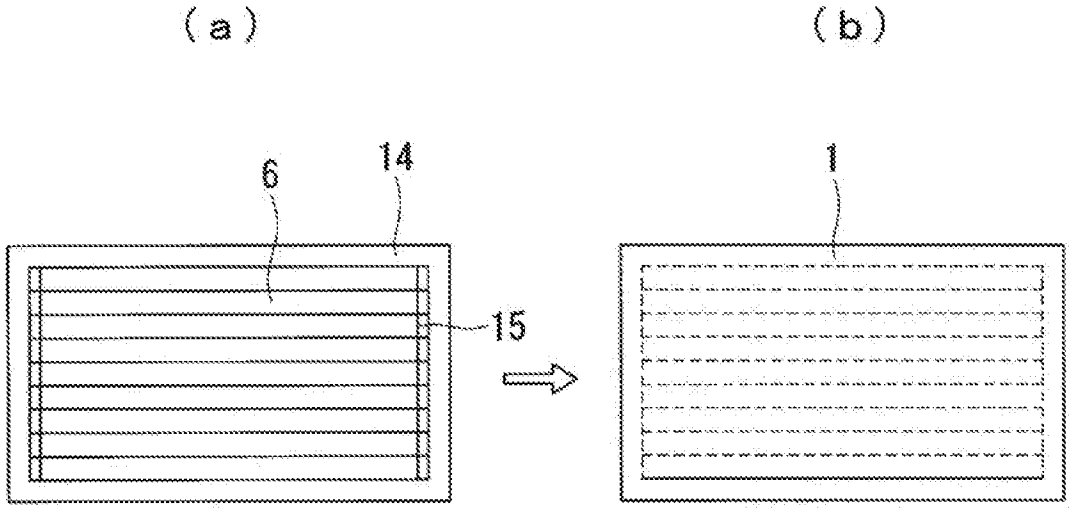
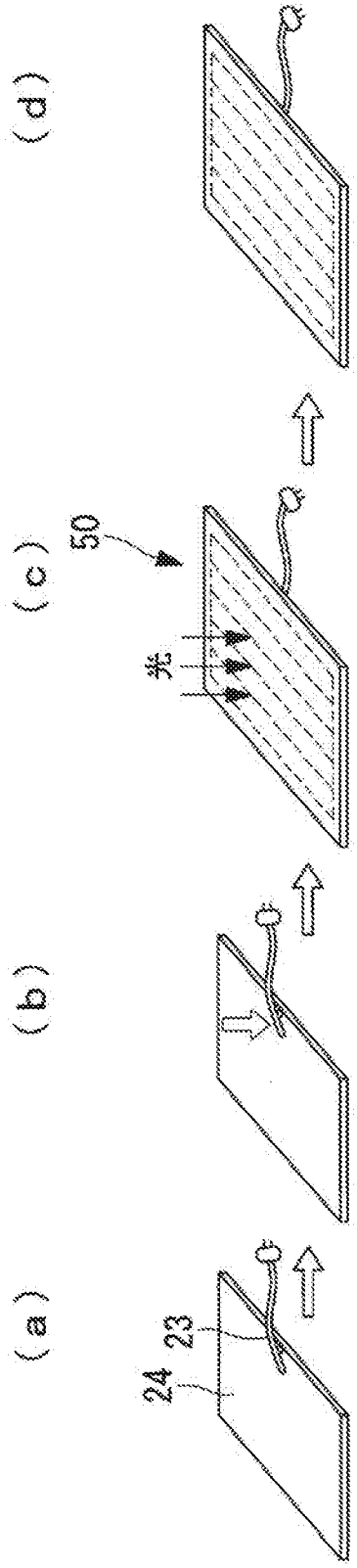
[図6]



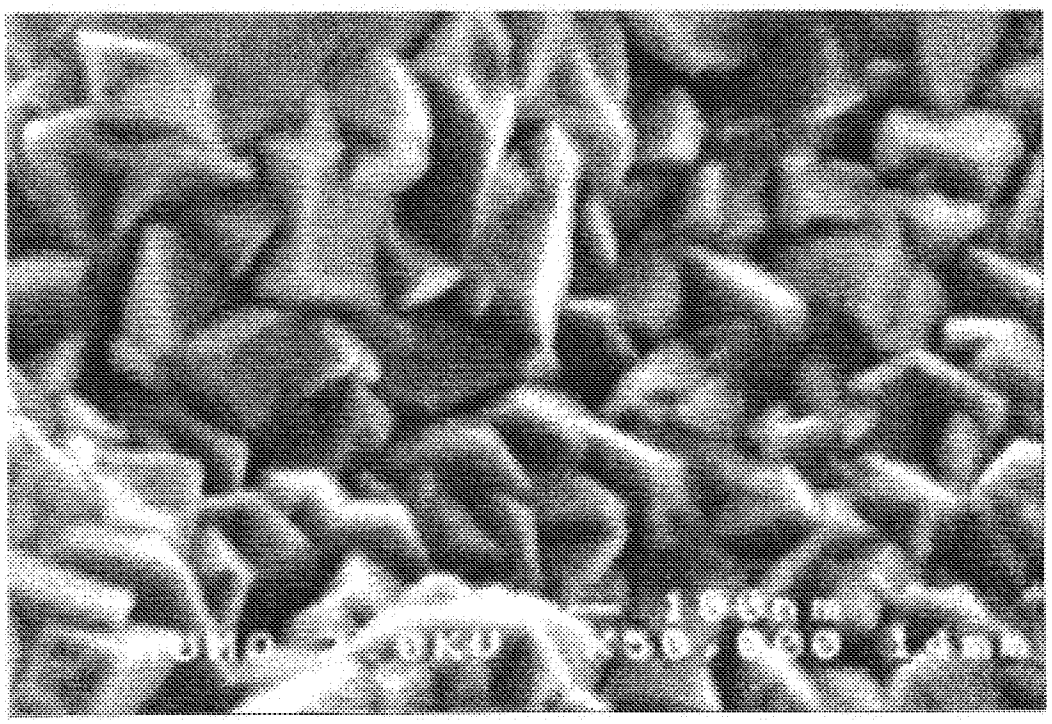
[図6]



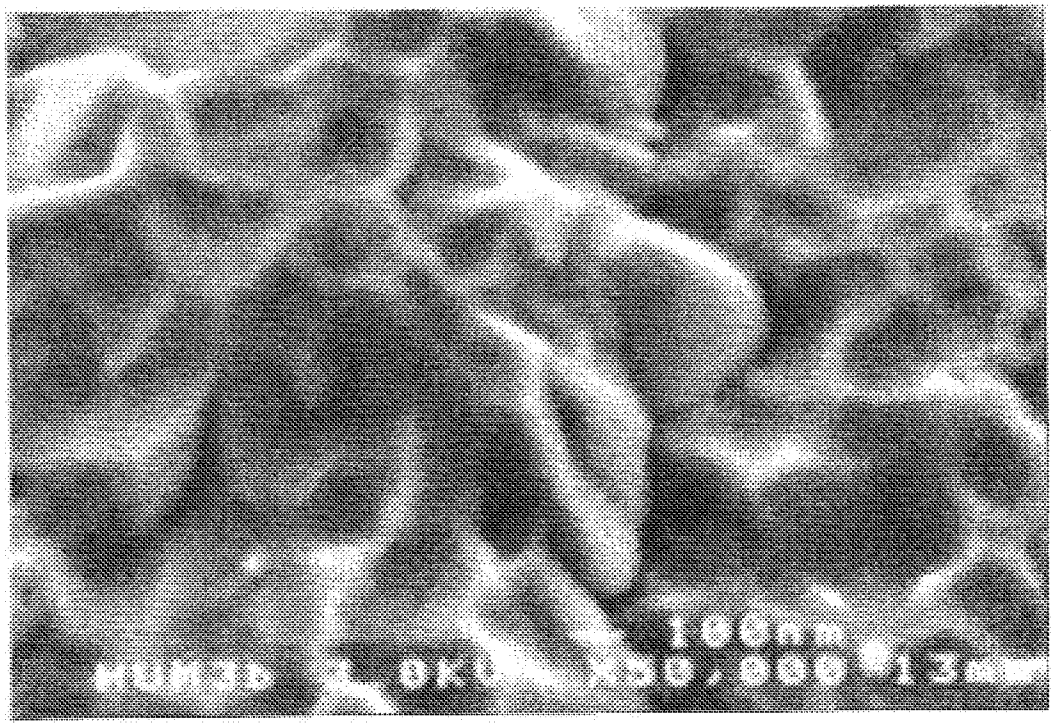
[図7]



[図8]



[図9]



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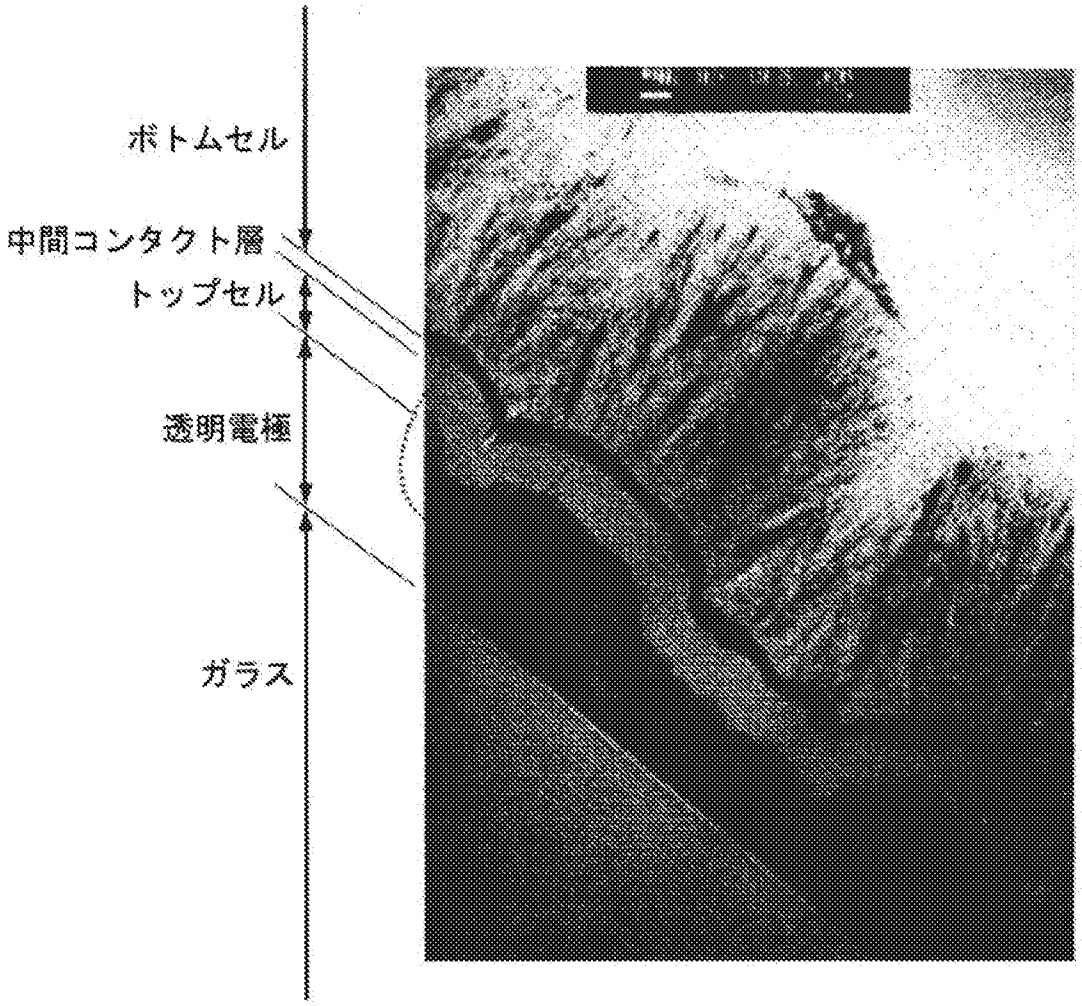
[図10]



[図11]

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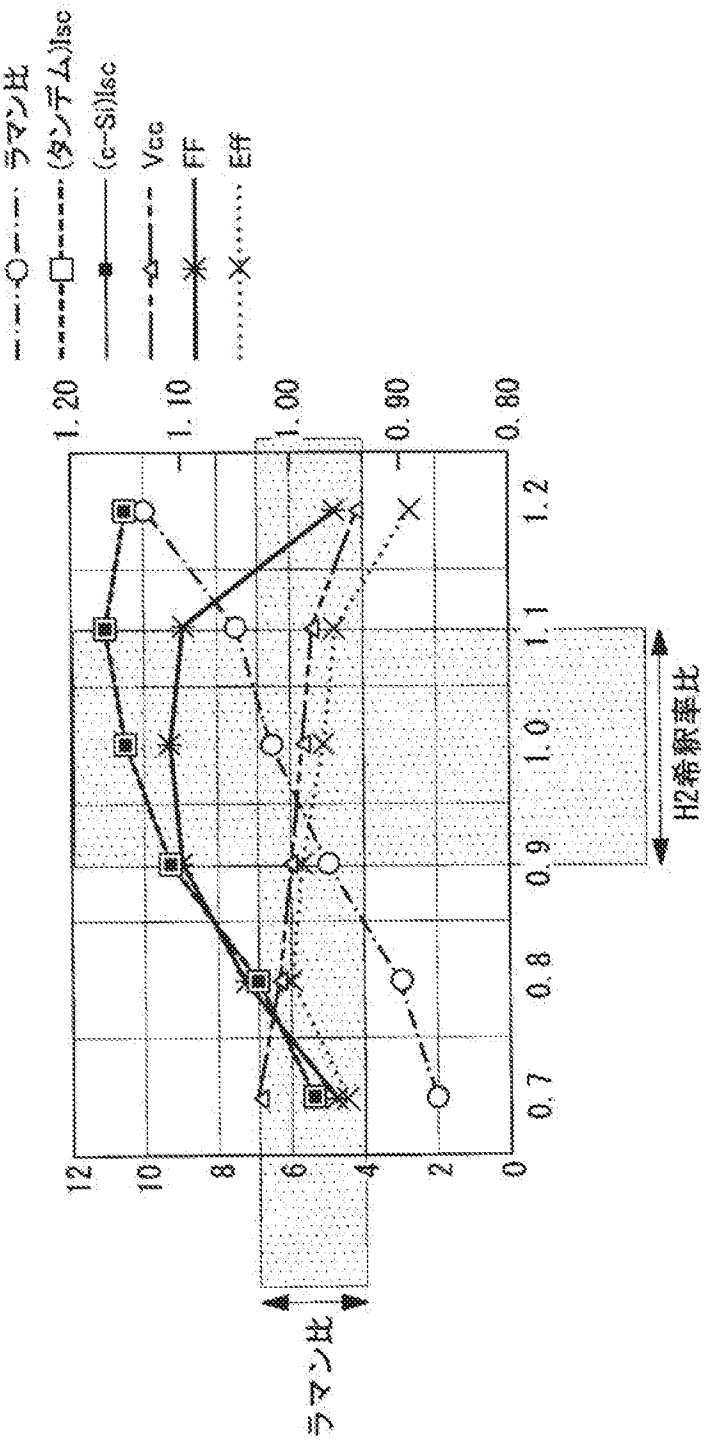
[図12]


ラマン比
(タンデムJ)Isc
(c-Si)Isc
Voc
FF
Eff
1.20
1.10
1.00
0.90
0.80
1.2
1.1
1.0
0.9
0.8
0.7
H2希釈率比
12
10
8
6
4
2
0
ラマン比

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2007/065386

A. CLASSIFICATION OF SUBJECT MATTER
H01L31/04(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L31/04

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2007
Kokai Jitsuyo Shinan Koho 1971-2007 Toroku Jitsuyo Shinan Koho 1994-2007

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2005-347490 A (Asahi Glass Co., Ltd.), 15 December, 2005 (15.12.05), Full text; all drawings (Family: none)	1-4,14,15
Y	JP 2002-26348 A (Mitsubishi Heavy Industries, Ltd.), 25 January, 2002 (25.01.02), Par. No. [0036] (Family: none)	1-4,14,15
Y	JP 2006-216921 A (Mitsubishi Heavy Industries, Ltd.), 17 August, 2006 (17.08.06), Par. No. [0044]; Fig. 5 (Family: none)	1-4,14,15

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 October, 2007 (30.10.07)	13 November, 2007 (13.11.07)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (April 2007)

SAMSUNG EX. 1002 - 1408/2862

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2007/065386

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2007-5345 A (Mitsubishi Heavy Industries, Ltd.), 11 January, 2007 (11.01.07), Par. No. [0041]; Fig. 15 (Family: none)	1-4,14,15

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2007/065386

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
A matter common to the inventions in claims 1-19 is "a photoelectric converter comprising a substrate with a transparent electrode where a transparent electrode layer is provided on a transparent insulating substrate, and at least a photoelectric conversion layer principally comprising a silicon based semiconductor and a backside electrode layer that are formed sequentially on the transparent electrode layer side of the substrate with a transparent electrode, wherein the substrate with a transparent electrode has a surface shape where large and small protrusions and recesses coexist and spectral haze rate is 20% or above at the wavelength of 550-800 nm.
(Continued to extra sheet.)

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.: 1-4, 14, 15

Remark on Protest

The

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

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Continuation of Box No.III of continuation of first sheet(2)

However, our search has found the above "photoelectric converter" is disclosed in Japanese Laid-open No. 2005-347490, and therefore it is not clearly novel. Consequently the common matter is not a special technical feature within the meaning of PCT Rule 13.2, second sentence, because the above "photoelectric converter" makes no contribution over the prior art.

Therefore, there is no matter common to all the inventions in claims 1-19 as a special technical feature, and there exists no other common matter to be considered to be a special technical feature within the meaning of PCT Rule 13.2, second sentence, therefore no technical relationship within the meaning of PCT Rule 13 can be found among those different inventions.

Accordingly, the inventions in claims 1-19 do not fulfill the requirement of unity of invention.

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国際調査報告

国際出願番号 PCT／JP2007／066386

A. 発明の属する分野の分類（国際特許分類（IPC））

Int.Cl. H01L31/04(2006.01)i

B. 調査を行った分野

調査を行った最小限資料（国際特許分類（IPC））

Int.Cl. H01L31/04

最小限資料以外の資料で調査を行った分野に含まれるもの

日本国実用新案公報	1922－1996年
日本国公開実用新案公報	1971－2007年
日本国実用新案登録公報	1996－2007年
日本国登録実用新案公報	1994－2007年

国際調査で使用した電子データベース（データベースの名称、調査に使用した用語）

C. 関連すると認められる文献

引用文献のカテゴリー＊	引用文献名 及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
Y	JP 2006-347490 A(旭硝子株式会社), 2005.12.15, 全文, 全図 (ファミリーなし)	1-4, 14, 15
Y	JP 2002-26348 A(三菱重工業株式会社), 2002.01.25, [0036] (ファミリーなし)	1-4, 14, 15
Y	JP 2006-216921 A(三菱重工業株式会社), 2006.08.17, [0044], 図5 (ファミリーなし)	1-4, 14, 15

☑ C欄の続きにも文献が列挙されている。　　☐ パテントファミリーに関する別紙を参照。

＊ 引用文献のカテゴリー
「A」特に関連のある文献ではなく、一般的技術水準を示すもの
「E」国際出願日前の出願または特許であるが、国際出願日以後に公表されたもの
「L」優先権主張に疑義を提起する文献又は他の文献の発行日若しくは他の特別な理由を確立するために引用する文献（理由を付す）
「O」口頭による開示、使用、展示等に言及する文献
「P」国際出願日前で、かつ優先権の主張の基礎となる出願の日の後に公表された文献
「T」国際出願日又は優先日後に公表された文献であって出願と矛盾するものではなく、発明の原理又は理論の理解のために引用するもの
「X」特に関連のある文献であって、当該文献のみで発明の新規性又は進歩性がないと考えられるもの
「Y」特に関連のある文献であって、当該文献と他の1以上の文献との、当業者にとって自明である組合せによって進歩性がないと考えられるもの
「&」同一パテントファミリー文献

国際調査を完了した日	国際調査報告の発送日
30.10.2007	13.11.2007

国際調査機関の名称及びあて先	特許庁審査官（権限のある職員）	2K	9010
日本国特許庁（ISA／JP） 郵便番号100－8915 東京都千代田区霞が関三丁目4番3号	吉野 三寛		
	電話番号 03－3581－1101 内線 3255		

様式PCT／ISA／210（第2ページ）（2007年4月）

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C（続き）．　関連すると認められる文献

引用文献のカテゴリー＊	引用文献名　及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
Y	JP 2007-6345 A(三菱重工業株式会社), 2007.01.11, [0041], 図 15 (ファミリーなし)	1-4, 14, 15

SAMSUNG EX. 1002 - 1413/2862

国際調査報告

国際出願番号 PCT／JP2007／065386

第II欄 請求の範囲の一部の調査ができないときの意見（第1ページの2の続き）

法第8条第3項（PCT17条(2)(a)）の規定により、この国際調査報告は次の理由により請求の範囲の一部について作成しなかった。

1. ☐ 請求の範囲＿＿＿＿＿＿＿＿は、この国際調査機関が調査をすることを要しない対象に係るものである。つまり、

2. ☐ 請求の範囲＿＿＿＿＿＿＿＿は、有意義な国際調査をすることができる程度まで所定の要件を満たしていない国際出願の部分に係るものである。つまり、

3. ☐ 請求の範囲＿＿＿＿＿＿＿＿は、従属請求の範囲であってPCT規則6.4(a)の第2文及び第3文の規定に従って記載されていない。

第III欄 発明の単一性が欠如しているときの意見（第1ページの3の続き）

次に述べるようにこの国際出願に二以上の発明があるとこの国際調査機関は認めた。

請求の範囲1－19に係る発明の共通の事項は、「透明絶縁性の基板上に透明電極層を設けてなる透明電極付き基板と、該透明電極付き基板の透明電極層側に順次形成された、シリコン系半導体を主として有する光電変換層ならびに裏面電極層とを少なくとも有してなる光電変換装置であって、前記透明電極付き基板は、表面が大小の凹凸が混在した形状であり、かつ分光ヘイズ率が550nm以上600nm以下の波長で20%以上である光電変換装置」である。

しかしながら、調査の結果、上記「光電変換装置」は、特開2005－347490号公報に開示されており、新規でないことが明らかとなり、結果として、上記「光電変換装置」は先行技術の域を出ないから、PCT規則13．2の第2文の意味において、この共通事項は特別な技術的特徴ではない。

それ故、特別な技術的特徴として請求の範囲1－19に係る発明全てに共通の事項はなく、PCT規則13．2の第2文の意味において特別な技術的特徴と考えられる他の共通の事項も存在しないので、それらの相違する発明の間にPCT規則13の意味における技術的な関連を見いだすことはできない。

よって、請求項1－19に係る発明は、発明の単一性の要件を満たしていない。

1. ☐ 出願人が必要な追加調査手数料をすべて期間内に納付したので、この国際調査報告は、すべての調査可能な請求の範囲について作成した。

2. ☐ 追加調査手数料を要求するまでもなく、すべての調査可能な請求の範囲について調査することができたので、追加調査手数料の納付を求めなかった。

3. ☐ 出願人が必要な追加調査手数料を一部のみしか期間内に納付しなかったので、この国際調査報告は、手数料の納付のあった次の請求の範囲のみについて作成した。

4. ☑ 出願人が必要な追加調査手数料を期間内に納付しなかったので、この国際調査報告は、請求の範囲の最初に記載されている発明に係る次の請求の範囲について作成した。

請求項1－4，14，15

追加調査手数料の異議の申立てに関する注意

☐ 追加調査手数料及び、該当する場合には、異議申立手数料の納付と共に、出願人から異議申立てがあった。

☐ 追加調査手数料の納付と共に出願人から異議申立てがあったが、異議申立手数料が納付命令書に示した期間内に支払われなかった。

☐ 追加調査手数料の納付はあったが、異議申立てはなかった。

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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
13 August 2009 (13.08.2009)

PCT

(10) International Publication Number
WO 2009/100023 A2

(51) International Patent Classification:
H01L 31/042 (2006.01)

(21) International Application Number:
PCT/US2009/032871

(22) International Filing Date:
2 February 2009 (02.02.2009)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/025,499 1 February 2008 (01.02.2008) US
61/053,080 14 May 2008 (14.05.2008) US

(71) Applicant *(for all designated States except US)*: **PRESIDENT & FELLOWS OF HARVARD COLLEGE** [US/US]; 17 Quincy Street, Cambridge, MA 02138 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **MAZUR, Eric** [NL/US]; 57 Lowell Road, Concord, MA 01742 (US). **WINKLER, Mark** [US/US]; 558 Mather Mail Center, Cambridge, MA 02138 (US). **TULL, Brian, R.** [US/US]; 1470 Boulevard, West Hartford, CT 06119 (US).

(74) Agents: **MOLLAAGHABABA, Reza** et al.; Nutter Mclennen & Fish Llp, World Trade Center West, 155 Seaport Boulevard, Boston, MA 02210-2604 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

WO 2009/100023 A2

(54) **Title**: A MULTIJUNCTION PHOTOVOLTAIC DEVICE

(57) **Abstract**: Photovoltaic devices (e.g., solar cells) are disclosed that include at least three radiation absorbing layers, each capable of absorbing radiation over a different wavelength range of the solar radiation spectrum. Any two of these three wavelength ranges can be partially overlapping, or alternatively they can be distinct. The layers are disposed relative to one another so as to form two junctions, each of which includes a depletion region. In some cases, the radiation absorbing layers can collectively absorb radiation over a wavelength range that spans at least about 60%, or 70%, or 80%, and preferably 90% of the solar radiation wavelength spectrum. By way of example, in some embodiments, one layer can exhibit significant absorption of solar radiation (e.g., it can absorb at least one radiation wavelength at an absorptance greater than about 90%) at wavelengths less than about 0.7 microns while another layer can exhibit significant absorption of the solar radiation at wavelengths in a range of about 0.7 microns to about 1 micron. The third layer can in turn exhibit a significant absorption of solar radiation at wavelengths greater than about 1 micron.

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A MULTIJUNCTION PHOTOVOLTAIC DEVICE

Related Application

The present application claims priority to provisional application entitled "All Silicon Multijunction Photovoltaic (Solar Cell)" filed on February 1, 2008 and having a serial number 61/025,499 as well as provisional application entitled "A Multijunction Photovoltaic Device" filed on May 14, 2008 and having a serial number 61/053,080. Both of these provisional applications are herein incorporated by reference.

Background

The present invention relates generally to photovoltaic devices and methods for their fabrication.

Photovoltaic devices produce electric power via conversion of the planet's most abundant and renewable energy input: sunlight. Crystalline silicon solar cells are among the most mature and efficient photovoltaic technologies. Additionally, silicon is the second most abundant element in the earth's crust. Although silicon would seem as the premier candidate for renewable and environmentally friendly solar energy conversion, high manufacturing costs and a recent shortage of device grade silicon have prevented such cells from economically competing with the combustion of fossil fuels as a source of electricity on a large scale.

Hence, there is a need for enhanced photovoltaic devices as well as improved fabrication techniques, particularly as they relate to enhanced silicon photovoltaic cells.

Summary

Photovoltaic devices (e.g., solar cells) are disclosed that include at least three radiation absorbing layers, each capable of absorbing radiation over a different wavelength range of the solar radiation spectrum. Any two of these three wavelength ranges can be partially overlapping, or alternatively they can be distinct from each other. The layers are disposed relative to one another so as to form two junctions, each of which includes a depletion region. In some cases, the radiation absorbing layers can collectively absorb radiation over a wavelength range that spans at least about 60%, or about 70%, or about 80%, and preferably at least about 90% of the solar radiation

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wavelength spectrum. By way of example, in some embodiments, one layer can exhibit significant absorption of solar radiation (e.g., it can absorb at least one radiation wavelength at an absorptance greater than about 90%) at wavelengths less than about 0.7 microns while another layer can exhibit significant absorption of the solar radiation at wavelengths in a range of about 0.7 microns to about 1 micron. The third layer can in turn exhibit a significant absorption of solar radiation at wavelengths greater than about 1 micron.

In a related aspect, the photovoltaic device is configured such that at least a portion of a surface of one of the layers can be exposed to the solar radiation. In many embodiments, the layer that is capable of absorbing high energy photons (shorter wavelengths) is the first layer that receives the radiation. A portion of the radiation is absorbed by that layer and the remaining radiation passes through the other two layers, each of which in turn absorbs a portion of the radiation corresponding to its wavelength absorption range. The absorption of the solar radiation can generate electron-hole pairs. At least some of such electron-hole pairs can be separated under the influence of the electric fields present in the depletion regions associated with the junctions between the layers so as to generate a voltage across the device.

In some embodiments, the radiation absorbing layers can collectively absorb at least about 60%, or at least about 70%, or at least about 80%, or at least about 90%, of solar radiation incident on a portion of at least one of the layers that is adapted for exposure to solar radiation.

Two electrically conductive electrodes, one of which is electrically coupled to the upper layer and the other to the lower layer, can be employed to apply the voltage generated across the device, in response to exposure to the solar radiation, to an external load. By way of example, in some embodiments, the photovoltaic device includes a radiation transparent substrate (e.g., a substrate that allows the passage of at least about 50% of incident solar radiation) on which the radiation absorbing layers are disposed. Although the term substrate is used it should be appreciated that, in a typical embodiment, the substrate will be the uppermost element of the device, upon which the solar radiation impinges. A radiation transparent electrically conductive layer (e.g., a layer formed of indium tin oxide or zinc oxide) disposed between the electrically conductive transparent layer and the upper layer, which is in electrical contact with at

least a portion of the upper layer, forms one of the electrodes. The other electrode can be formed by a metallic layer disposed over at least a portion of the lower layer so as to form an electrical contact therewith.

As noted above, at least a portion of the electron-hole pairs generated in response to the exposure of the radiation absorbing layers to solar radiation can drift in opposite directions under the influence of the electric fields in the depletion regions to generate a voltage across the electrodes, which can be applied to an external load.

In a related aspect, the various layers of the above photovoltaic device can be formed of silicon doped with a suitable dopant. By way of example, in some cases, the upper layer includes a p-doped layer of amorphous silicon (e.g., a layer having a thickness in a range of about 10 nanometers (nm) to about 500 nm) while the intermediate layer includes an n-doped layer of crystalline or polycrystalline silicon (e.g. a layer having a thickness in a range of about 5 μm (microns) to about 50 μm). The lower layer can include a thin layer of highly doped silicon that includes a high concentration of an n-type dopant (e.g., an atomic concentration of at least about 0.1%, e.g., in a range of about 0.1% to about 2%) that can absorb radiation wavelengths greater than about 1 micron (or 1.1 microns corresponding to the band gap of crystalline silicon) with a high absorptance (e.g., greater than about 50%, and preferably greater than about 90%) to generate electron-hole pairs.

In another aspect, the invention provides a photovoltaic device (e.g., a solar cell), which comprises a first semiconductor layer capable of absorbing radiation at wavelengths greater than about 1 micron with an absorptance greater than about 60% for at least one of those wavelengths, and a second semiconductor layer capable of absorbing radiation at one or more wavelengths in a range of about 0.7 microns to about 1 micron, where the second layer forms a junction with the first layer. The photovoltaic device can further include a third semiconductor layer that is capable of absorbing radiation at wavelengths less than about 0.7 microns, e.g., in a range of about 0.25 microns to about 0.7 microns, where the third layer forms a junction with said second layer. Each junction can comprise a depletion region in which an electric field is present.

In another aspect, a method of fabricating a photovoltaic device is disclosed that includes forming a radiation transparent conductive layer, which can function as an electrode, over a surface of a radiation transparent substrate. A layer of amorphous silicon doped with a p-type dopant can then be formed, e.g., via plasma enhanced chemical vapor deposition, over the transparent conductive layer. A layer of crystalline or polycrystalline silicon can then be formed over the amorphous layer, e.g., via low pressure chemical vapor deposition. A plurality of short laser pulses (e.g., pulses having temporal durations in a range of about 100 femtoseconds to about 500 femtoseconds) can be applied to an exposed surface of the crystalline or polycrystalline layer (that is a surface opposed to the one that is in contact with the amorphous layer) while exposing the surface to a fluid (e.g., a liquid or gas) having an electron-donating constituent to form a thin highly doped surface layer (e.g., one having a thickness in a range of about 10 nm to about 1000 nm) that functions as another radiation absorbing layer of the cell. Subsequently, a metallic layer can be deposited over the disordered layer (e.g., by evaporating a metal onto a top surface of the disordered layer) so as to generate another electrode. The highly doped layer, which can in some cases be a crystalline or polycrystalline layer, can also be formed to have these high doping levels using other techniques that yield similar optical properties. These techniques include irradiating with a plurality of short laser pulses having longer durations, e.g., as long as 1 picosecond, or even as long as 1 nanosecond, to about 100 nanoseconds. Other techniques to implant large quantities of dopants can also be used.

Further understanding of the invention can be obtained by reference to the following detailed description in conjunction with the associated drawings, which are discussed briefly below.

Brief Description of Drawings

FIGURE 1 schematically depicts a photovoltaic cell in accordance with one embodiment of the invention,

FIGURE 2 shows the spectral irradiance of solar radiation as a function of wavelength at the earth above the atmosphere (solid line) relative to radiation from a black body at a temperature of about 5900 K (dashed line),

FIGURE 3A schematically depicts an exemplary implementation of the photovoltaic cell of FIGURE 1,

FIGURE 3B schematically depicts the photovoltaic cell of FIGURE 3A attached to a load,

FIGURE 4 depicts absorption of radiation by three layers of a hypothetical solar cell according to an embodiment of the invention over different wavelength ranges of the solar spectrum,

FIGURE 5 depicts schematically absorption of photons in various layers of a solar cell according to an embodiment of the invention,

FIGURE 6A schematically depicts absorption of photons in a conventional homojunction solar cell,

FIGURE 6B schematically depicts the thermalization energy loss of an electron of an electron-hole pair generated in a conventional homojunction solar cell,

FIGURE 6C schematically depicts that absorption of a photon in conventional homojunction solar cell can yield work corresponding to the energy associated with the band gap,

FIGURE 7 schematically depicts depletion regions associated with junctions between various layers of a solar cell according to an embodiment of the invention,

FIGURE 8A shows surface structures generated in a silicon substrate via exposure of the substrate to femtosecond laser pulses in presence of SF_6,

FIGURE 8B is a cross-sectional TEM image of one of the spikes shown in FIGURE 8A,

FIGURE 9 shows radiation absorptance as a function of wavelength exhibited by a laser-processed silicon substrate relative to that exhibited by unstructured silicon,

FIGURE 10 shows rectification exhibited by a junction formed between a surface layer formed in silicon substrate by application of short laser pulses in presence of SF_6 and the underlying silicon substrate, and

FIGURE 11 shows I-V curve of a prototype solar cell.

Detailed Description

The present invention generally provides a multi-junction photovoltaic device (e.g., a solar cell) that can include, e.g., a first, a second and a third radiation absorbing layer, each capable of absorbing radiation over a different wavelength range within the solar wavelength spectrum. The first and the second layer can have, respectively, p-type and n-type doping (or *vice versa*) and can contact one another, e.g., along a surface, to form a junction characterized by a depletion region. In some cases, the third layer can have the same type of doping as that of the second layer (e.g., both the second layer and the third layer can have an n-type doping) but at a different (e.g., higher) concentration level (e.g., at least about 1% atomic), or it can have a different type of doping, such that a junction it forms with the intermediate layer would also include a depletion region. The term "depletion region," also commonly known as "depletion layer" or "depletion zone," is known in the art and can be formed across a junction between two semiconductors (e.g., a p-n junction) having different concentrations of electrons or holes via diffusion of carriers from the semiconductor having a higher concentration to the other until an electric field generated across the junction impedes the diffusion, thus leading to the formation of a region that is substantially lacking in mobile charge carriers and supports an electric field.

FIGURE 1 schematically depicts a multijunction photovoltaic device 10, e.g., a solar cell, that includes three radiation absorbing layers (regions) 12, 14, and 16 that are disposed relative to one another to form two junctions A and B. For ease of description, the layers 12, 14, and 16 are herein referred to in some cases, respectively, as the upper (first), intermediate (second) and lower (third) layers. Each layer is formed of a

material, e.g., a semiconductor, in which electron-hole pairs can be generated in response to the absorption of optical radiation having suitable wavelengths. The layers are disposed on a support substrate 18, which can be formed of a suitable radiation transparent material such as glass. In many embodiments, the substrate 18 can allow the passage of at least about 50% of the sun's radiation, and preferably at least about 80% and more preferably at least about 90% of the incident sun's radiation. A radiation transparent electrically conducting layer 20, which functions as one of two electrodes for coupling a voltage generated across the cell in response to solar radiation to an external load, separates the radiation absorbing layer 12 from the support substrate 18 and forms electrical contact with that absorbing layer.

A metallic layer 22 disposed over the lower layer 16 provides another electrode that in combination with the electrode 16 can be utilized to apply a voltage generated across the device to an external load (not shown). As discussed in more detail below, upon exposure of the layers 12, 14 and 16 to solar radiation, electron-hole pairs can be generated in those layers. At least a portion of these electron-hole pairs can be separated under the influence of the electric fields associated with the junctions A and B to drift in opposite directions toward the electrode 20 or 22. In this manner, a voltage can be generated across the device.

By way of example, in some implementations of the multijunction solar cell 10, each of the radiation absorbing layers 12, 14 and 16 can show a significant absorption, e.g., an absorption greater than about 60% (e.g., in a range of about 60% to about 100%), for radiation in a different wavelength band of the solar radiation spectrum. In some cases, such wavelength bands can have overlapping portions and can collectively cover the wavelengths of the sun's radiation not only in the visible wavelength range but also in the infrared range. For example, the layers can be collectively capable of absorbing all radiation wavelengths over a span of the sun's radiation spectrum extending from about 250 nm to about 2500 nm.

The sun's radiation spectrum exhibits wavelengths that span a range of about 0.25 microns to about 2.5 microns, with significant decrease in intensity for wavelengths beyond this range. Accordingly, the term "solar wavelength spectrum," as used herein can refer to a wavelength range extending from about 0.25 microns to about 2.5 microns.

The solar spectrum can be approximated by that of a black body radiating at a temperature of about 5900 K. The spectral irradiance, M, emitted by a black body in the units of $Wm^{-2}\mu m$ is given by:

$$M = \frac{2\pi hc^2}{\lambda^5} \frac{1}{\exp[\frac{hc}{kT\lambda}]-1} \qquad \text{Eq. (1)}$$

where h is Planck's constant, c is the speed of light, k is the Boltzmann constant, T is the temperature of the black body in units of Kelvin (K) and λ is the wavelength in units of microns (μm).

By way of example, FIGURE 2 shows a solar radiation spectrum indicating solar radiation irradiance as a function of the radiation wavelength. In some implementations, the layers 12 can exhibit a high absorption of the solar radiation with wavelengths less than about 0.7 microns while the region 14 can exhibit a high absorption of the solar radiation with wavelengths in a range of about 0.7 microns to about 1 micron. The layer 16 can in turn show a high absorption of the solar radiation with wavelengths greater than about 1 micron, e.g., in a range of about 1 micron to about 2.5 microns. The term "high absorption" refers to an absorption of radiation with an absorptance greater than about 60%, or greater than about 70%, or preferably greater than about 80%, and more preferably greater than about 90% (e.g., near unity).

FIGURE 3A shows a multijunction solar cell 24 that corresponds to an exemplary implementation of the aforementioned solar cell 10 in which each of the layers 10, 12 and 14 is formed primarily of silicon (that is, it is formed of silicon in which some dopants are incorporated). More specifically, the solar cell 24 includes a radiation transparent support substrate 26 that extends from an external surface 26a that is adapted for exposure to solar radiation to an internal surface 26b on which a layer of a transparent conductor 28 is disposed. In this embodiment, the substrate 26 is formed of glass, though in other embodiments it can be formed of other materials such as transparent dielectrics (e.g. quartz) or plastics or polymers. The radiation transparent conductor layer 28 can be formed, for example, of indium tin oxide (ITO) or zinc oxide (ZnO).

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The exemplary multijunction solar cell 24 further includes a radiation-absorbing layer 30 formed of p-doped amorphous silicon (αSi) that is disposed over the transparent conductor layer 28. The layer 30 can exhibit a thickness in a range of about 1 nm to about 1000 nanometers, and preferably in a range of about 10 nm to about 100 nanometers (e.g., about 50 nm). The doping level of the layer 30 can be, e.g., in a range of about 10^{14} cm^{-3} to about 10^{19} cm^{-3}, and preferably in a range of about 10^{16} cm^{-3} to about 10^{17} cm^{-3}. The layer 30 can be doped with a variety of p-type dopants, such as boron or aluminum or gallium.

Another radiation absorbing layer 32 is disposed over the layer 30 to form a junction J1 therewith, where the junction includes a depletion region. More specifically, in some embodiments the layer 32 can be formed of crystalline silicon (c-Si) or polycrystalline silicon (p-Si) that is appropriately doped. In this exemplary implementation, the layer 32 comprises polycrystalline silicon that is doped with an n-type dopant. The doping concentration of the layer 32 can be, for example, in a range of about 10^{12} cm^{-3} to about 10^{18} cm^{-3}, and preferably in a range of about 10^{14} cm^{-3} to about 10^{16} cm^{-3}. Further, the thickness of the layer 32 can be in a range of about 1 micrometer to about 500 micrometers, and preferably in a range of about 5 micrometers to about 50 micrometers (e.g., about 10 microns). The contact junction J1 formed between the layers 30 and 32 includes a depletion region. As discussed in more detail below, an electric field in the depletion region can facilitate the separation of the electron-hole pairs generated in that region or in vicinity thereof by incident solar photons. In some implementations, the layer 32 can be a thin layer having a thickness, e.g., in a range of about 1 micrometer to about 10 micrometers. In some cases, such a thin layer (e.g., a thickness in a range of about 1 mircon to about 10 microns) can exhibit an absorptance of about 25% or less in response to exposure to radiation wavelengths in a range of about 0.7 microns to about 1 micron.

In this embodiment, a thin highly-doped disordered layer 34 forms another junction J2 with the crystalline or polycrystalline layer 32 (in some other embodiments the heavily doped layer 34 can be crystalline exhibiting in some cases a highly ordered structure). Similar to the junction J1, the junction J2 can also include a depletion region that can facilitate the separation of electron-hole pairs generated by solar photons. As discussed in detail below, in some cases, the layer 34 can be fabricated by applying a

plurality of short laser pulses to the top surface of the underlying layer 32 while exposing the surface to an electron-donating compound (e.g., SF_6). The layer 34 can have a thickness in a range of about 10 nm to about 1000 nm, and preferably in a range of about 50 nm to about 200 nm. In many implementations, the layer 34 includes a high level of n-doping (e.g., at an atomic concentration of at least about 1%) so as to exhibit a higher n-type doping concentration level than that of the underlying layer 32.

As discussed in more detail below, in this embodiment, the highly-doped silicon layer 34 can absorb radiation with wavelengths greater than about 1 micron (e.g., greater than about 1.1 microns) with an absorptance significantly greater than that exhibited by crystalline silicon at those wavelengths. While crystalline silicon exhibits a precipitous drop in radiation absorption for wavelengths greater than that corresponding to its bandgap (e.g., greater than about 1.1 microns), the highly-doped silicon layer can exhibit in some cases near unity absorptance (e.g., an absorptance greater than about 90%) for those radiation wavelengths.

The absorption characteristics of the three layers 30, 32 and 34 in the exemplary multijunction solar cell 24 can allow the cell to absorb the incident solar photon flux over a wide wavelength range. By way of illustration, FIGURE 4 shows a plot indicating the absorption of solar photons by different layers 30, 32, and 34 of a hypothetical implementation of the solar cell 24, illustrating the number of photons absorbed by each of those layers (it should be understood that this figure is presented only for illustrative purposes and is not intended to necessarily indicate the optimal radiation absorption characteristics of a multijunction solar cell in accordance with the teachings of the invention). The plot shows the photon flux (number of photons per unit area) at a given energy in the AM1.5 solar spectrum. The area under the curve represents the number of photons in a given energy range. The amorphous silicon layer can absorb photons with energies greater than about 1.7 eV, while the polycrystalline or crystalline silicon layer can absorb photons with energies greater than about 1.1 eV. The highly-doped disordered layer (in some cases the highly-doped layer is not disordered) can in turn absorb photons with energies greater than about 0.5 eV. In some cases, the highly-doped layer can absorb photons with energies greater than about 0.25 eV.

Referring again to FIGURE 3A, a thin metallic layer 36 is disposed over the thin layer 34. The metallic layer 36 together with the aforementioned radiation transparent conductive layer 28 allow extracting a voltage from the solar cell 24 to be applied to an external load 38, as shown schematically in FIGURE 3B, and discussed in more detail below.

In use, upon exposure of the multijunction solar cell 24 to solar radiation, incident solar photons pass through the glass substrate 26 and the transparent conductor to be incident on the amorphous silicon layer 30. A portion of these photons are absorbed by the amorphous silicon layer so as to generate electron-hole pairs. The photons absorbed by the amorphous layer 30 are typically high energy photons, e.g., photons having energies greater than an energy corresponding to the band gap of amorphous silicon (e.g., 1.7 eV).

The remaining photons, or at least a large portion of them, enter the polycrystalline (or crystalline) layer 32. These photons have typically lower energy as many of the higher energy photons were previously absorbed by the amorphous layer 30. For example, many of these photons can have energies in a range of about 1.1 eV to about 1.7 eV. The absorption of these photons can also lead to the generation of electron-hole pairs. Finally, those photons that were not absorbed by the layers 30 and 32 reach the highly-doped layer 34 and are absorbed by that layer (at least a portion of those photons are absorbed by the layer 34) to generate additional electron-hole pairs. The energies of many of these photons lie in a range less than about 1.1 eV. In many implementations, the layer 34 exhibits micron-sized surface undulations that can help in trapping photons. In addition, the metallic layer 36 can reflect photons not absorbed by the radiation absorbing layers back to those layers.

Hence, the multijunction solar cell 24 absorbs photons over substantially the entire range of the solar radiation spectrum. Such absorption of photons corresponding to different wavelength ranges of the solar spectrum is schematically shown in a graph in FIGURE 5 for a hypothetical multijunction solar cell according to the teachings of the invention. The graph schematically indicates each material with its associated band gap (for example, in the solar cell shown in FIGURE 5, Material 1 corresponds to amorphous silicon, Material 2 corresponds to crystalline or polycrystalline silicon and Material 3 corresponds to a highly-doped disordered layer). The graph shows that the

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band gap of the three material progressively decreases such that the photons having higher energies are absorbed primarily in Material 1 to generate electron-hole pairs while lower energy photons are absorbed in the Materials 2 and 3 (in cases where a surface of Material 1 is exposed to solar radiation, high energy photons, which can be absorbed near the surface, can suffer less thermalization loss). Many device details, such as the bending of the bands at the junctions, are not shown in this figure.

By way of contrast, FIGURES 6A-6C schematically show the absorption of solar photons in a hypothetical homojunction photovoltaic cell (e.g., a solar cell). FIGURE 6A shows that only those photons having energies that are at least equal to that of the band gap can be absorbed. All absorbed photons yield about ε_{gap} of work, as shown schematically in FIGURE 6C. But many low energy photons are not absorbed. Further, some energy from high energy photons are lost to lattice thermalization (e.g., FIGURE 6B schematically shows energy (ε_{th}) lost by an electron of an electron-hole pair generated by a high energy photon to the lattice). By way of example, in a near ideal silicon homojunction material, photons representing more than about 20% of the solar energy are not absorbed and about 30% of the energy of the absorbed photons is lost to heat.

Referring again to FIGURE 3A, the junctions J1 and J2 include depletion regions. These depletion regions are shown schematically in FIGURE 7 as regions DP1 and DP2. The electron-hole pairs generated in each of the two depletion regions or in vicinity thereof are separated by the electric field present in the depletion regions to drift towards the upper or the lower conductors 36 and 28. Some of such electrons and holes are lost to electron-hole recombination events, while others are lost to non-radiative recombination at traps, and still others may be lost to Auger recombination. Those that reach the respective upper and lower metal electrodes can provide a voltage across the cell that can be applied to an external load, such as the light bulb shown in FIGURE 3B.

In some embodiments, the highly-doped layer exhibits not only a high doping concentration level but also good charge carrier mobility so as to minimize electron-hole recombination events and scattering. By way of example, the electron mobility in the highly doped layer 34 can be greater than about 500 $cm^2/V \cdot s$, e.g., in a range of about 100 $cm^2/V \cdot s$ to about 1000 $cm^2/V \cdot s$. As discussed in more detail below, in some cases the fabrication of the highly-doped layer can include a high-temperature annealing

protocol to ensure high electron mobility in that layer.

A variety of techniques can be employed to fabricate the multijunction solar cell 24. By way of example, in one such fabrication method, the transparent conductive electrode can be formed on a surface of glass substrate, e.g., by radio frequency sputtering from an indium tin oxide (ITO) target. Subsequently, the amorphous silicon layer can be grown on the exposed surface of the transparent metal electrode, in a manner known in the art, for example by decomposition of silane gas (SiH_4) in plasma enhanced chemical vapor deposition. Similarly, the crystalline or polycrystalline layer is grown on the amorphous layer. By way of example, thin films of amorphous and microcrystalline silicon can be produced by plasma-enhanced chemical vapor deposition using a mixture of silane (SiH_4) and hydrogen gases. The films can include a substantial amount of hydrogen (e.g., 5-20 at. %). Amorphous silicon films can be fabricated by utilizing pure silane while crystalline grains can be fabricated via high dilution in hydrogen. The degree of crystallinity can be varied by varying the concentration of silane, e.g., in a range of about 4.5% to about 8%. For example, in some cases, at a concentration of about 4.5%, the film can exhibit a high degree of crystallinity with an average grain size of, e.g., about 25 microns. Amorphous and microcrystalline silicon can be doped with a suitable n-type and p-type dopant, such as phosphorous or boron, during the deposition process. Polycrystalline films are also commonly grown via low-pressure chemical vapor deposition, via thermal decomposition of silane gas in a tube furnace.

The highly-doped layer 34 can then be generated by applying short radiation pulses to the exposed surface of the crystalline or polycrystalline layer 32 while the surface is exposed to an electron-donating compound (e.g., sulfur hexafluoride gas), as discussed in more detail below. It can also be generated via other techniques for implanting impurities beyond the solid solubility limit. Finally, the metallic electrode can be formed over the disordered layer 34, e.g., by evaporating a metal over that layer.

As discussed above, in this exemplary embodiment, the layer 34 is in the form of a disordered layer formed primarily of silicon in which a large quantity of an electron-donating dopant, e.g., sulfur, is incorporated. As noted in more detail below, such a layer can be formed by irradiating a silicon surface with short radiation pulses (e.g., pulses having temporal durations in a range of about 10 femtoseconds (fs) to about a few

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hundred nanoseconds) while exposing to the surface to an electron-donating constituent (e.g., SF_6). Such processing of silicon can generate the disordered layer 34 with a thickness, e.g., in a range of 10 nanometers to about 1000 nanometers, which exhibits not only significant absorption in the visible radiation wavelengths but also at wavelengths that are larger than that corresponding to the band gap of silicon (e.g., at wavelengths greater than about 1.1 microns).

By way of example, in some embodiments, the layer 34 can be fabricated by applying radiation pulses having temporal durations in a range of about 10 fs to about 500 fs (though longer pulse widths can also be utilized) and having wavelengths in a range of about 400 nm to about 800 nm to a surface of a crystalline silicon substrate; longer and shorter wavelengths can be used, for example from about 200 nm to wavelengths of several microns, e.g., 5 microns. The fluence (energy per unit area) of the pulses at the substrate surface can be, e.g., in a range of about 1 kJ/cm^2 to about 40 kJ/cm^2. In some cases, the substrate is moved relative to the radiation beam (or *vice versa*) such that different areas of the surface are irradiated with the pulses. The rate of movement of the substrate can be selected such that each irradiated area is exposed to a plurality of pulses, e.g., in a range of about a few tens to a few thousands (e.g., 500 pulses).

In some embodiments, the irradiation of the surface with the pulses is performed while the surface is exposed to a dopant chosen, e.g., from heavy chalcogens (e.g., sulfur, selenium, and tellurium). Without being limited to any particular theory, the train of the pulses can cause ultrafast melting of the substrate's lattice so as to yield a resolidification front that moves very fast, and can trap foreign atoms (e.g., sulfur) in its vicinity with a surface layer of the substrate at concentration levels that substantially exceed the respective solid solubility limit. These foreign atoms can be introduced in a variety of ways. For example, the substrate surface can be irradiated with the short (e.g., femtosecond) pulses while the surface is exposed to sulfur hexafluoride gas (e.g., the irradiation can be done in the presence of 500 torr sulfur hexafluoride gas). As another example, when doping the substrate with selenium or tellurium, a film of selenium or tellurium (e.g., a 100-nm film) can be thermally evaporated onto the substrate surface and then the coated surface can be irradiated with the short laser pulses.

The resulting substrate surface can exhibit micron-scale or sub-micron scale morphologies depending on the conditions utilized. By way of example, FIGURE 8A quasi-ordered array of microspikes that are about 1 – 15 microns tall and spaced by about 1 – 5 microns that were generated in a surface layer of a silicon substrate by exposing the surface to 100-fs laser pulses having a central wavelength of 800 nm and a fluence of about 8 kJ/m^2. Each area of the surface was exposed to about 600 pulses. A cross-sectional transmission electron microscopy (TEM) image of one of the spikes shown in FIGURE 8B reveals a doped, 300-nm thick polycrystalline disordered surface layer. In particular, the X-ray diffraction pattern shown in the inset of FIGURE 8B indicates that the disordered layer is in fact polycrystalline. Further, Rutherford backscattering data (not shown) indicates that the polycrystalline layer exhibits about 1% atomic doping, and diffraction studies reveal an average grain size of about 30 nm.

Further details regarding various ways of generating a doped surface layer by exposing a substrate surface to short laser pulses can be found U.S. Published Patent Application No. 2003/0029495 entitled "Systems and Methods for Light Absorption and Field Emission Using Microstructured Silicon," U.S. Published Patent Application No. 2006/0079062 entitled "Femtosecond Laser-Induced Formation of Submicrometer Spikes On a Semiconductor Substrate," U.S. Patent No. 7,057,256 entitled "Silicon-based Visible and Near-infrared Optoelectronic Devices," pending U.S. Patent Application No. 12/038209 entitled "Laser-Induced Structuring of Substrate Surfaces," each of which is herein incorporated by reference in its entirety. The present application also incorporates by reference a thesis entitled "Femtosecond Laser Ablation of Silicon: Nanoparticles, Doping and Photovoltaics," which was presented to Harvard University by Brian Tull in 2007.

The morphology of the disordered surface layer, e.g., characterized by a disordered array of microspikes, can be distinct from doping of the layer. For example, adjusting laser parameters (e.g., fluence) as well as the distribution of laser pulses over the surface can be employed to enhance or reduce the sizes of the surface features while still providing a requisite degree of doping (e.g., 1% atomic concentration). In some cases, the spikes or similar surface features generated by laser processing of the substrate can be used to amplify absorption of solar radiation incident on the surface due to multiple reflections. In other cases, it may advantageous to fabricate a highly doped

disordered surface layer that exhibits a substantially smooth top surface. By way of example, an international (PCT) application entitled "Engineering Flat Surfaces on Material Doped Via Femtosecond Laser Irradiation", which is concurrently filed herewith and is herein incorporated by reference in its entirety, describes a method of processing a substrate by irradiating at least a portion of the substrate surface with a plurality of short radiation pulses while exposing the surface to a dopant. The pulses are selected to have a fluence at the substrate surface that is greater than a melting fluence threshold and less than an ablation fluence threshold. In this manner, a quantity of the dopant can be incorporated into the substrate while ensuring that the roughness of the substrate's surface is significantly less than the wavelength of the applied radiation pulses.

Although the above description relates to generating a highly doped layer in crystalline silicon, the methods discussed above can be employed to generate such doping layers in amorphous silicon (e.g., in thin films of amorphous silicon) or other semiconductors by exposing them to short laser pulses in the presence of a dopant.

The radiation absorbing layer 34 generated by the above methods can exhibit a substantially uniform absorption of electromagnetic radiation incident thereon from ultraviolet to the near-infrared (e.g., in a range of about 250 nm to about 2500 nm). As such, it can be particularly useful in absorbing the solar radiation at wavelengths greater than about 1.1 microns, where crystalline silicon shows very low absorption. By way of illustration, FIGURE 9 shows the radiation absorptance as a function of wavelength for a highly doped surface layer formed in silicon via application of 100-fs pulses at a central wavelength of about 800 nm and a fluence of about 8 kJ/m^2 (each area was exposed to about 500 pulses), indicating a near-unity absorptance over a wide range of wavelengths. In contrast, as shown in the figure, the absorptance exhibited by a crystalline silicon substrate drops precipitously for wavelengths greater than about 1.1 microns.

Moreover, the highly-doped layer can form a diode junction with the underlying substrate that can be characterized by a depletion region. That is, in many cases, the dopant atoms are not only optically active but they can also act as electron donors. In some embodiments, subsequent to irradiation of substrate with laser pulses in the presence of a dopant, the substrate (and consequently the generated highly doped surface

layer) is annealed at an elevated temperature (e.g., at 900 K for about 30 minutes) to facilitate the formation of a diode junction between the doped surface layer and the underlying substrate. Such an annealing step is further discussed in Published U.S. Patent Application No. 2008/0044943 entitled "Manufacture of Silicon-based Devices Having Disordered Sulfur-doped Surface Layers," which is incorporated herein by reference in its entirety.

By way of illustration, FIGURE 10 shows that a junction between a surface layer formed in a silicon substrate by application of 100-fs pulses (800 nm central wavelength at a fluence of 8 kJ/m^2) and the underlying substrate demonstrates rectification. Additionally, regardless of the original substrate doping, room-temperature Hall measurements performed on a number of silicon substrates in which such highly doped surface layers are generated demonstrate a negative charge carrier concentration in a range of about 10^{19} to about 10^{20} cm^{-3} in that layer.

A multijunction photovoltaic cell according to the teachings of the invention can provide a number of advantages relative to conventional multijunction photovoltaic cells. For example, a multijunction photovoltaic cell of the invention can utilize a significant portion of the solar wavelength spectrum for generating electron-hole pairs. In addition, it can be fabricated by utilizing abundant raw materials and known techniques. In contrast, conventional cells typically include a combination of exotic materials that are expensive, both to acquire as raw materials as well as to incorporate into a device.

The following example is provided for illustrative purposes to generally indicate the feasibility of utilizing a highly-doped disordered layer, such as the aforementioned layer 34, as a radiation absorbing layer in a multijunction solar cell.

Example

A homojunction prototype solar cell was fabricated by generating a highly doped disordered layer as a top surface layer of a p-type silicon substrate (resistivity ρ = 800 Ohm-cm) by applying a plurality of 100-fs laser pulses having a central wavelength of 800-nm to a surface of the silicon substrate at a fluence of about 4 kJ/m^2 while exposing the surface to SF_6. Cr/Au electrical contacts were deposited, one on each opposed side of the substrate, to allow measuring a voltage generated across the cell in response to

exposure to solar radiation.

FIGURE 11 shows a current versus voltage (I-V) curve measured for the prototype homojunction cell. The open circuit voltage (V_{oc}) refers to a voltage developed across a solar cell, which is not connected to an external load, as a result of the electron-hole pairs generated in response solar radiation. The open circuit voltage can be measured, e.g., by determining a voltage needed to be applied to an illuminated solar cell to prevent flow of a current. The short circuit current (I_{sc}) refers to a current that flows through an external source having a vanishing resistance that is coupled across an illuminated cell. By way of example, the V_{oc} and I_{sc} can be determined by sweeping a voltage applied across

A power delivered by a solar cell to an external load connected across the cell having a given resistance can be determined by multiplying the current through the load by the voltage across the load. A variable used to characterize the quality of a solar cell is known as the fill factor (FF), which can be defined as follows:

$$FF = \frac{I_{\max} V_{\max}}{I_{SC} V_{OC}} \qquad \text{Eq. (2)}$$

where I_{max} and V_{max} correspond to current and voltage associated with a maximum power delivered by the cell, and V_{oc} and I_{sc} represent the open circuit voltage and short circuit current, respectively.

The efficiency of a solar cell, η(%), for converting solar power into electrical energy can be defined as:

$$\eta = \frac{I_{\max} V_{\max}}{T_1 A} \times 100\% \quad \text{Eq. (3)}$$

where T_1 represents the intensity of the light incident on the a surface of the cell exposed to the solar radiation, A represents the area exposed to the solar radiation, and I_{max} and V_{max} correspond to current and voltage associated with a maximum power delivered by the cell.

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The efficiency of the aforementioned prototype cell under irradiation of an $AM_{1.5}$ solar spectrum was measured to be about 2.2% with an open circuit voltage of about 0.42 V, a short circuit current of 14.4 mA/cm^2, and a fill factor of about 0.36.

Those having ordinary skill in the art will appreciate that various changes can be made to the above embodiments without departing from the scope of the invention.

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Claims:

1. A photovoltaic device, comprising

a first layer ,

a second layer forming a junction characterized by a depletion region with said first layer, and

a third layer forming a junction characterized by a depletion region with said intermediate layer,

each of said layers being adapted to absorb radiation over a different wavelength range of the solar spectrum so as to generate electron-hole pairs,

wherein at least one of said layers is capable of absorbing radiation at wavelengths greater than about 1 micron with an absorptance greater than about 60%.

2. The photovoltaic device of claim 1, wherein said wavelength ranges corresponding to absorption by the layers collectively span a wavelength range extending from 250 nm to about 2500 nm.

3. The photovoltaic device of claim 1, wherein said at least one layer exhibits an absorptance greater than about 70% for wavelengths greater than about 1 micron.

4. The photovoltaic device of claim 1, wherein said at least one layer exhibits an absorptance greater than about 80% for wavelengths greater than about 1 micron.

5. The photovoltaic device of claim 1, wherein said at least one layer exhibits an absorptance greater than about 90% for wavelengths greater than about 1 micron.

6. The photovoltaic device of claim 1, wherein one of said layers comprises amorphous silicon.

7. The photovoltaic device of claim 1, wherein one of said layers comprises any of crystalline or polycrystalline silicon.

8. The photovoltaic device of claim 1, wherein one of said layers comprises a silicon layer doped with a dopant at an atomic concentration greater than about 1%.

9. A photovoltaic device, comprising

a first radiation absorbing layer formed of silicon doped with a dopant so as to absorb electromagnetic radiation at one or more wavelengths greater than about 1 micrometers with an absorptance greater than about 70%,

a second radiation absorbing layer formed of any of doped crystalline or polycrystalline silicon disposed over said first layer, said second layer forming a junction with said first layer characterized by a depletion region, and

a third radiation absorbing layer formed of doped amorphous silicon disposed on said second layer so as to form a junction therewith characterized by a depletion region.

10. The photovoltaic device of claim 9, wherein said first layer comprises a layer containing said dopant with an atomic concentration greater than about 1%.

11. The photovoltaic device of claim 10, wherein said first layer has a thickness in a range of about 10 nm to about 1000 nm.

12 The photovoltaic device of claim 9, wherein at least a portion of one of said layers is configured for exposure to an external source of radiation.

13. The photovoltaic device of claim 9, further comprising a pair of electrodes each of which is in electrical coupling with one of said regions so as to facilitate generation of an electrical signal in response to exposure of said at least a portion of one of said regions to radiation from said source.

14. The photovoltaic device of claim 13, wherein said electrical signal comprises any of a voltage or a current.

15. The photovoltaic device of claim 9, wherein said first layers includes an n-type dopant.

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16. The photovoltaic device of claim 9, wherein said first layer exhibits an electron mobility greater than about 100 $cm^2/V \cdot s$.

17. A photovoltaic device, comprising

a first semiconductor layer capable of absorbing radiation at wavelengths greater than about 1.1 microns, said layer exhibiting an absorptance greater than about 25% for at least one of said wavelengths,

a second semiconductor layer capable of absorbing radiation at wavelengths in a range of about 0.7 microns to about 1.1 microns, said second layer forming a junction with said first layer,

a third semiconductor layer capable of absorbing radiation at wavelengths in a range of about 0.25 microns to about 0.7 microns, said third layer forming a junction with said second layer,

wherein said of said junctions comprises a depletion region.

18. The photovoltaic device of claim 17, wherein said first layer exhibits an absorptance in a range of about 0.25 to about 1.0 at radiation wavelengths in a range of about 1 micron to about 2 microns.

19. The photovoltaic device of claim 17, wherein said second layer exhibits an absorptance in a range of about 0.5 to about 1.0 at radiation wavelengths in said range of about 0.7 microns to about 1 micron.

20. The photovoltaic device of claim 17, wherein said third layer exhibits an absorptance in a range of about 0.5 to about 1 at radiation wavelengths in said range of about 0.25 microns to about 0.7 microns.

21. The photovoltaic device of claim 17, wherein each of said layers is formed primarily of silicon.

22. A photovoltaic device, comprising

an upper layer capable of generating electron-hole pairs in response to exposure to radiation having one or more wavelengths within a first wavelength range,

an intermediate layer forming a junction characterized by a depletion region with said upper layer, said intermediate layer being capable of generating electron-hole pairs in response to radiation having one or more wavelengths within a second wavelength range,

a lower layer forming a junction characterized by a depletion region with said intermediate layer, said lower layer being capable of generating electron-hole pairs in response to radiation having one or more wavelengths within a this wavelength range,

said wavelength ranges spanning different portions of the solar wavelength spectrum,

wherein at least a portion of one of said layers is configured for exposure to solar radiation, and wherein said layers are adapted to collectively absorb at least about 70% of solar radiation energy incident on said portion configured for exposure to solar radiation

23. The photovoltaic device of claim 22, wherein said layers are adapted to collectively absorb at least about 80% of solar radiation energy incident on said portion configured for exposure to solar radiation.

24. The photovoltaic device of claim 22, wherein said layers are adapted to collectively absorb at least about 90% of solar radiation energy incident on said portion configured for exposure to solar radiation.

25. A method of fabricating a photovoltaic device, comprising

forming a radiation transparent electrically conductive layer over a surface of a radiation transparent substrate,

disposing a first semiconductor radiation absorbing layer over said electrically conductive layer,

disposing a second semiconductor radiation absorbing layer over said first layer so as to form a junction with said first layer characterized by a depletion region,

applying a plurality of short radiation pulses to an uncovered surface of said second layer while said surface portion is exposed to a compound having an electron donating constituent in order to convert a portion of said second layer into a third radiation absorbing layer forming a junction characterized by a depletion region with said second layer, and

depositing an electrically conductive layer over said third layer.

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FIG. 1

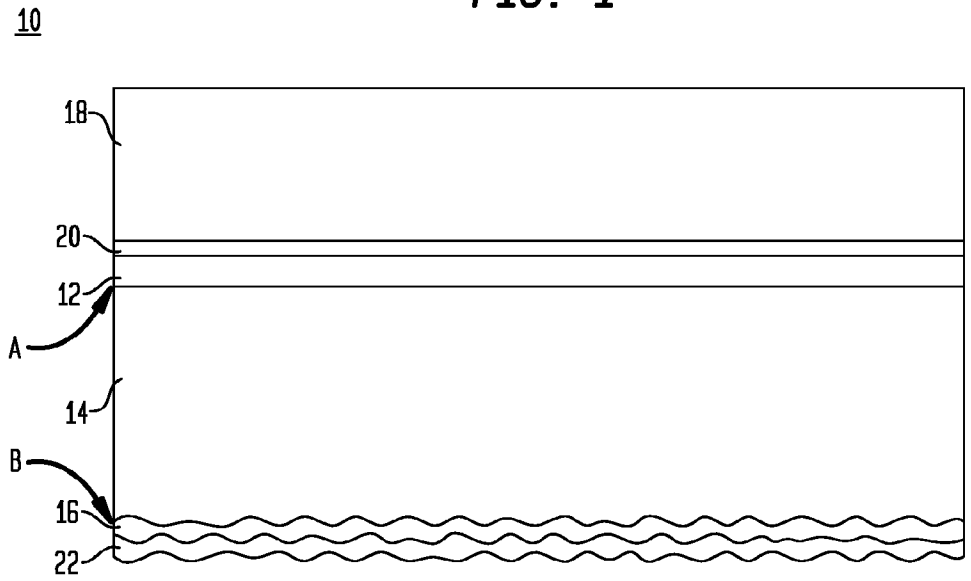

FIG. 2

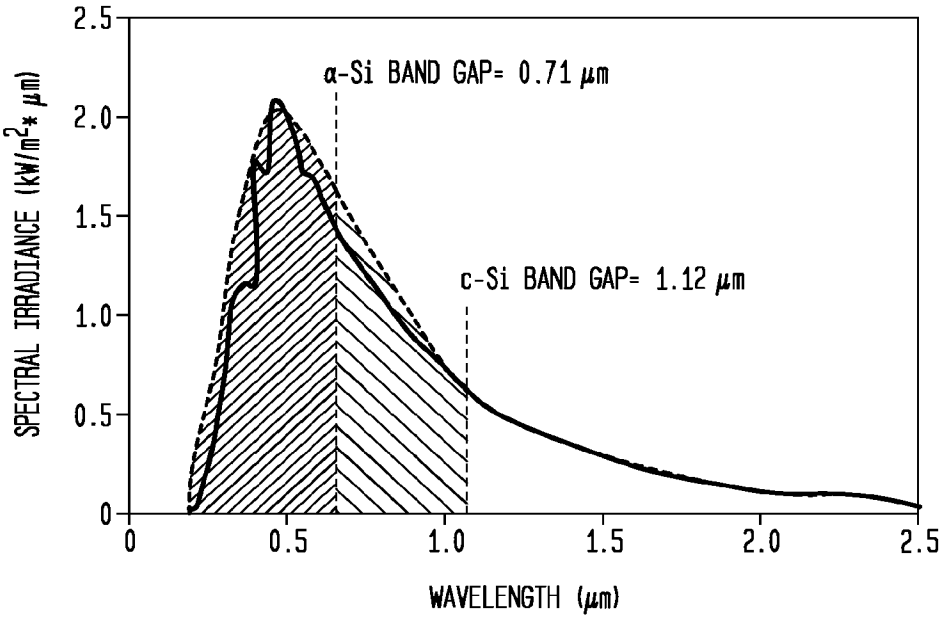

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FIG. 3A

FIG. 3B

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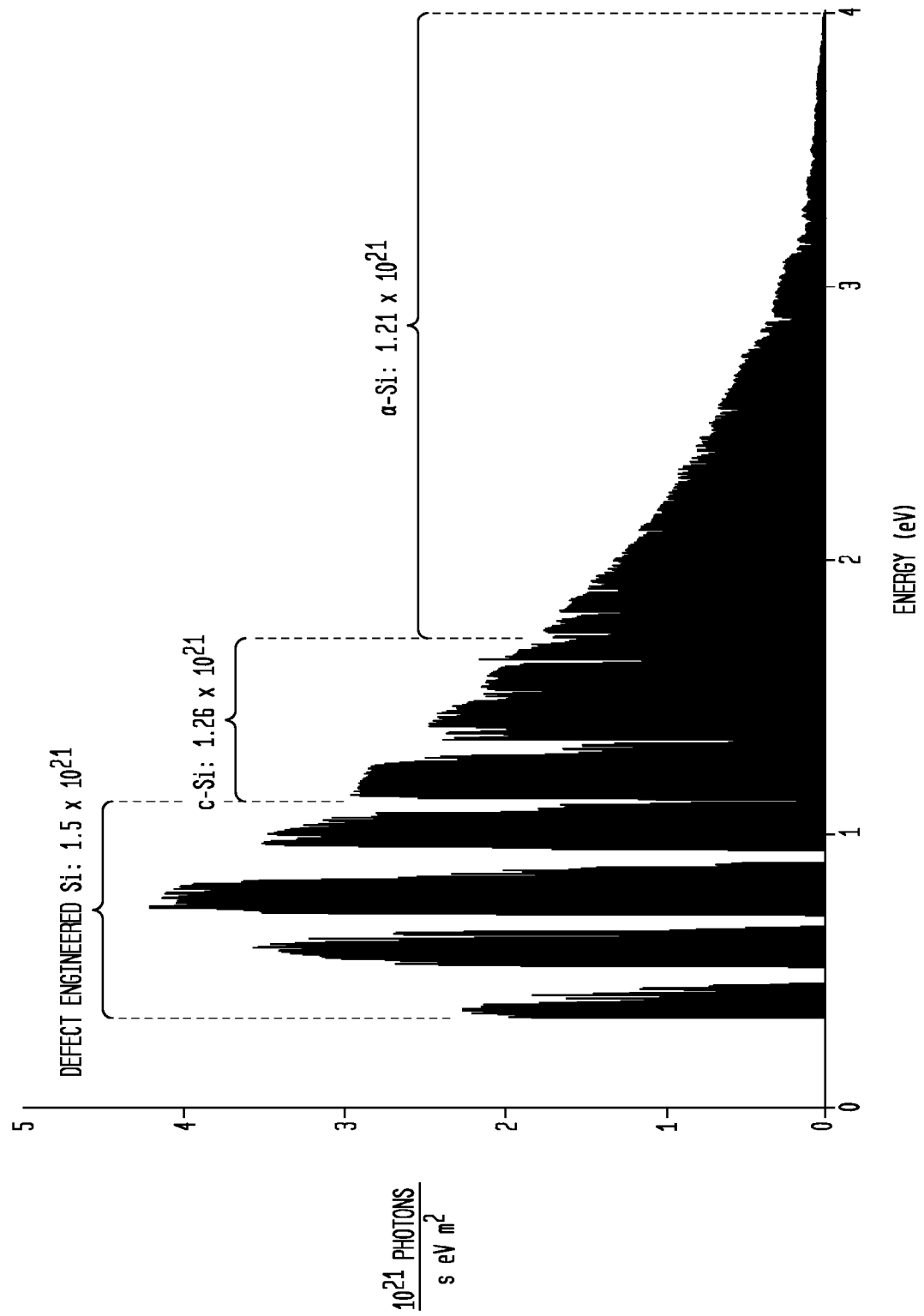
FIG. 4



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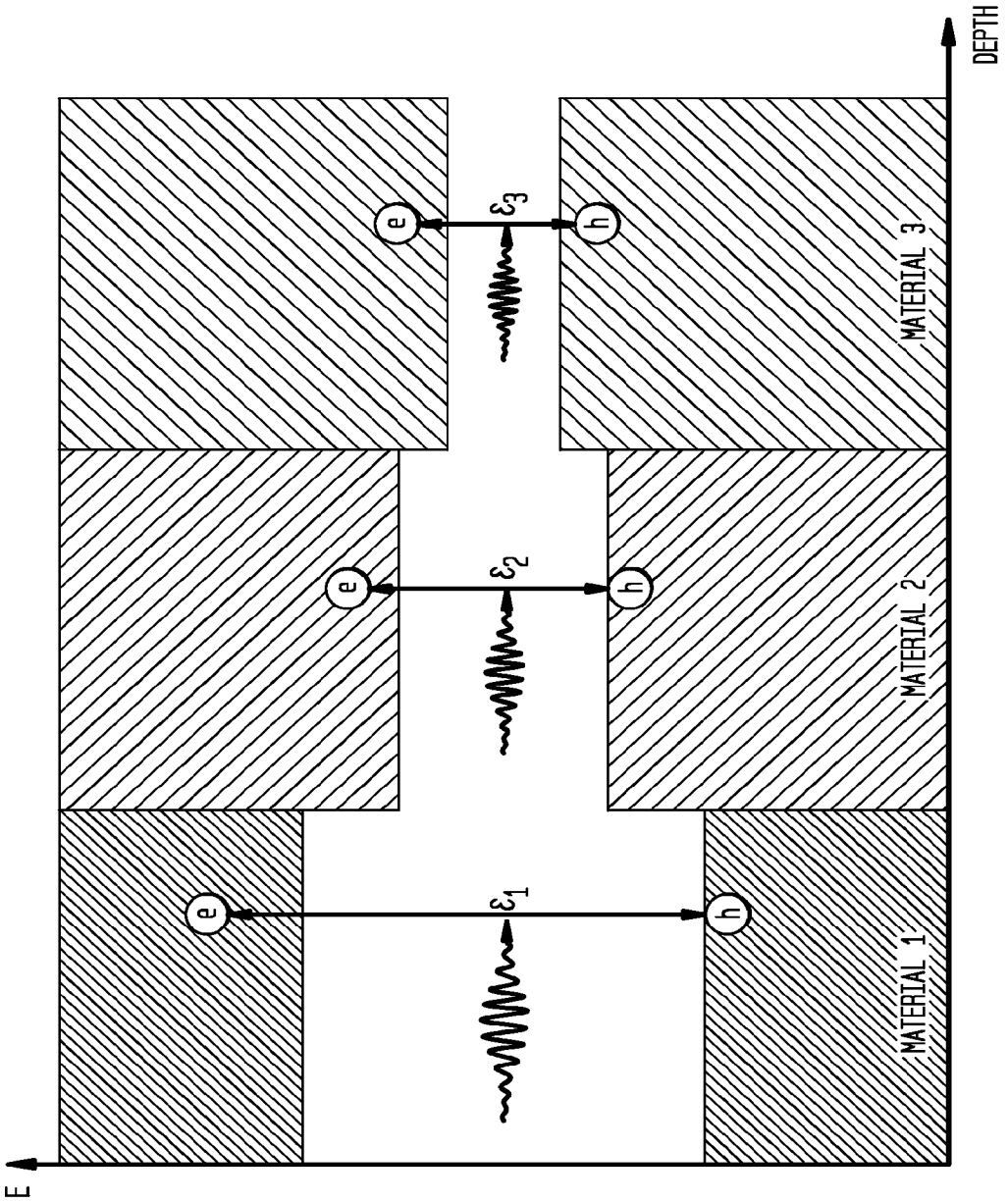

FIG. 5

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FIG. 6A

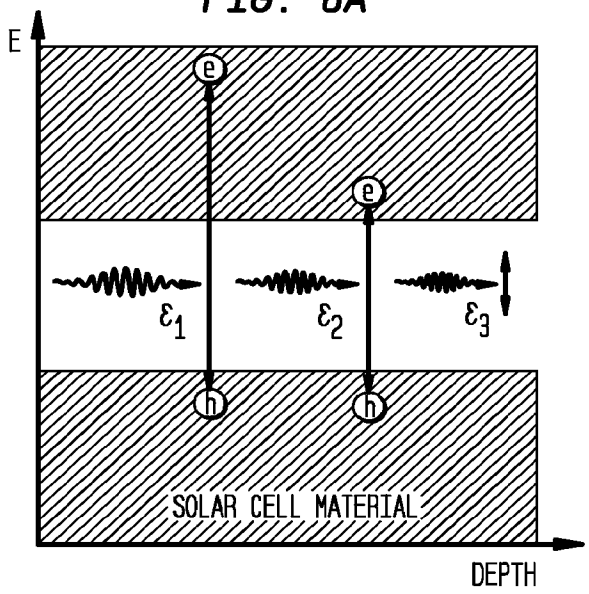

FIG. 6B

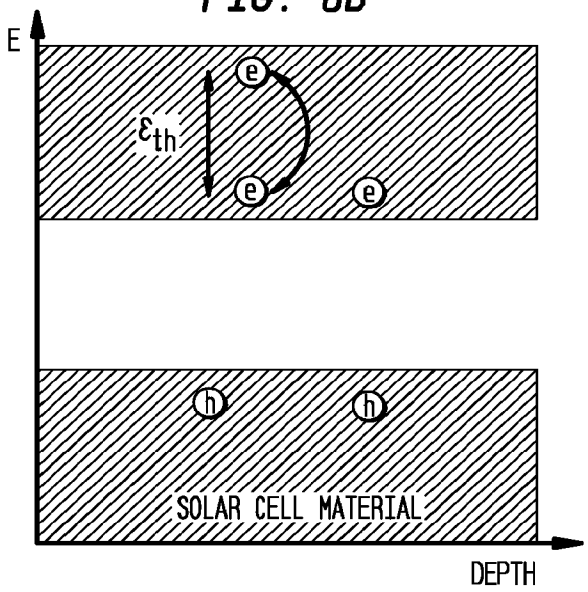

FIG. 6C

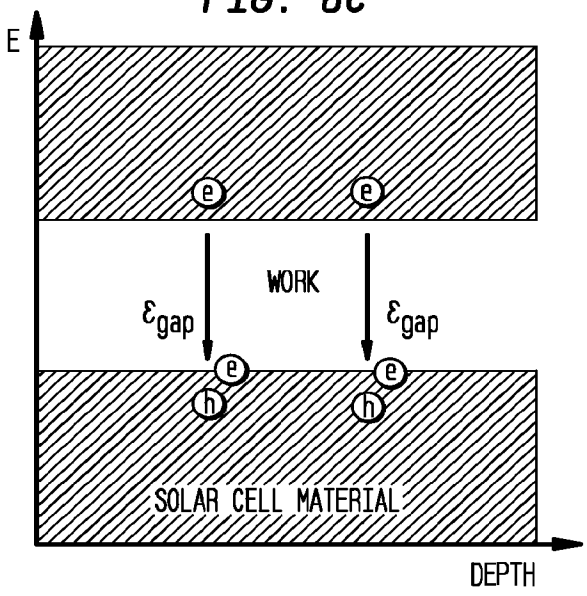

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FIG. 7

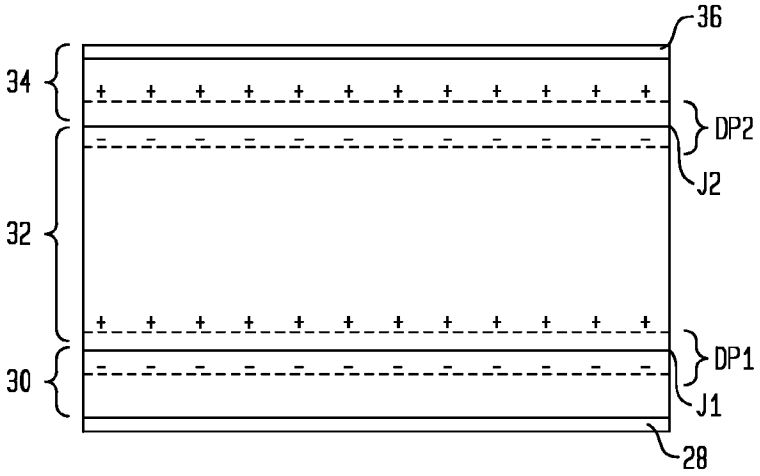

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FIG. 8A

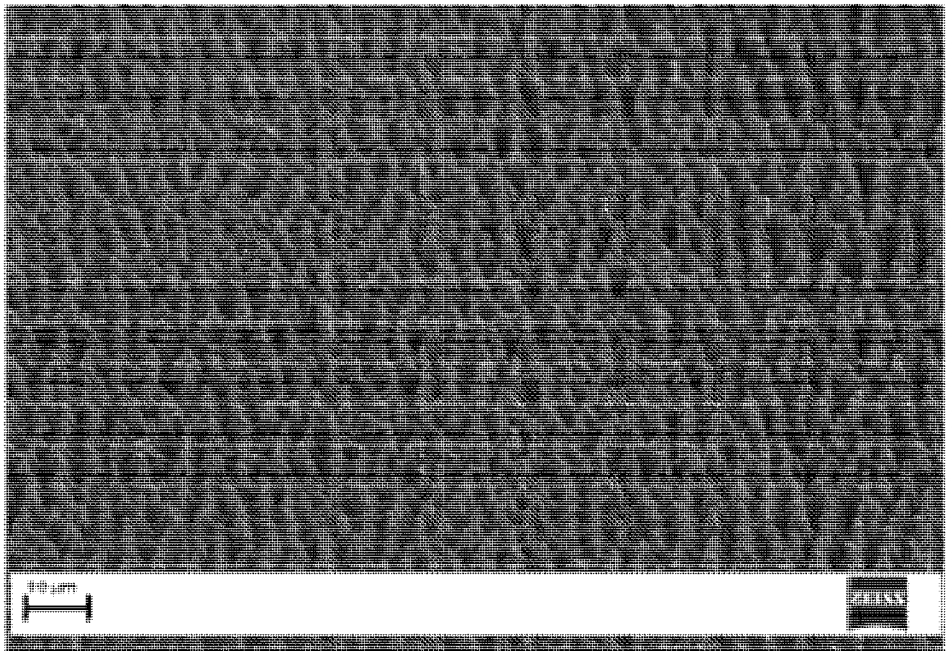

FIG. 8B

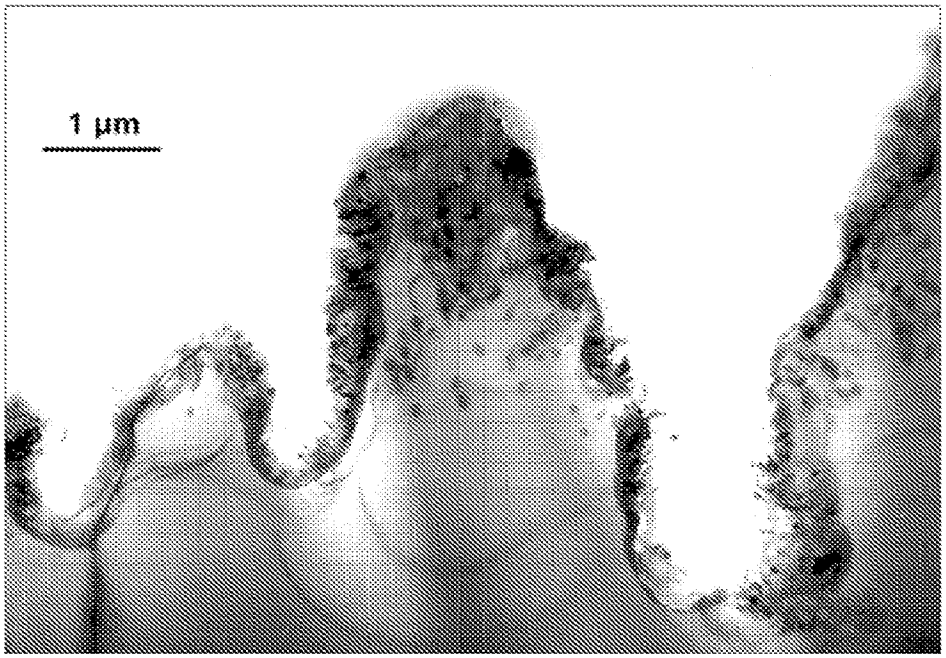

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FIG. 9

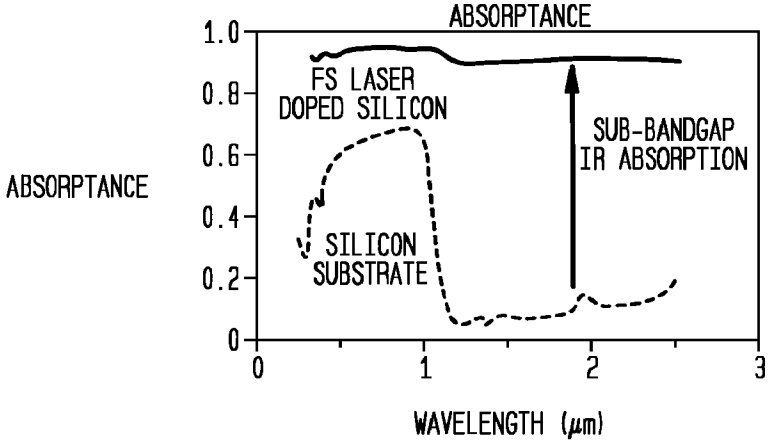


FIG. 10

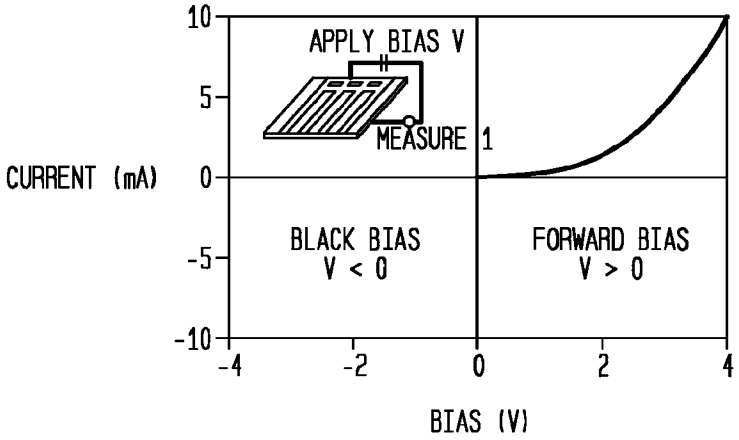
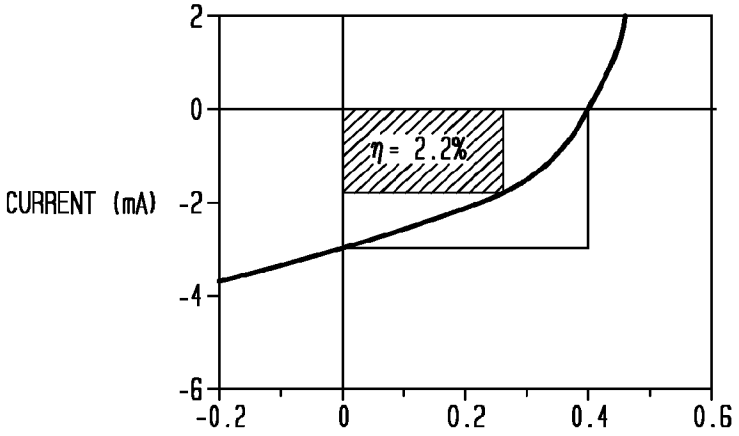


FIG. 11



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(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

(19) Weltorganisation für geistiges Eigentum
Internationales Büro

(43) Internationales Veröffentlichungsdatum
10. Dezember 2009 (10.12.2009)

PCT

(10) Internationale Veröffentlichungsnummer
WO 2009/147085 A1

(51) Internationale Patentklassifikation:
G01J 1/42 (2006.01) *G01J 5/20* (2006.01)
H01L 27/146 (2006.01)

(21) Internationales Aktenzeichen: PCT/EP2009/056603

(22) Internationales Anmeldedatum:
29. Mai 2009 (29.05.2009)

(25) Einreichungssprache: Deutsch

(26) Veröffentlichungssprache: Deutsch

(30) Angaben zur Priorität:
10 2008 002 270.5 6. Juni 2008 (06.06.2008) DE

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[Fortsetzung auf der nächsten Seite]

(54) **Title**: MULTISPECTRAL SENSOR

(54) **Bezeichnung**: MULTISPEKTRALER SENSOR

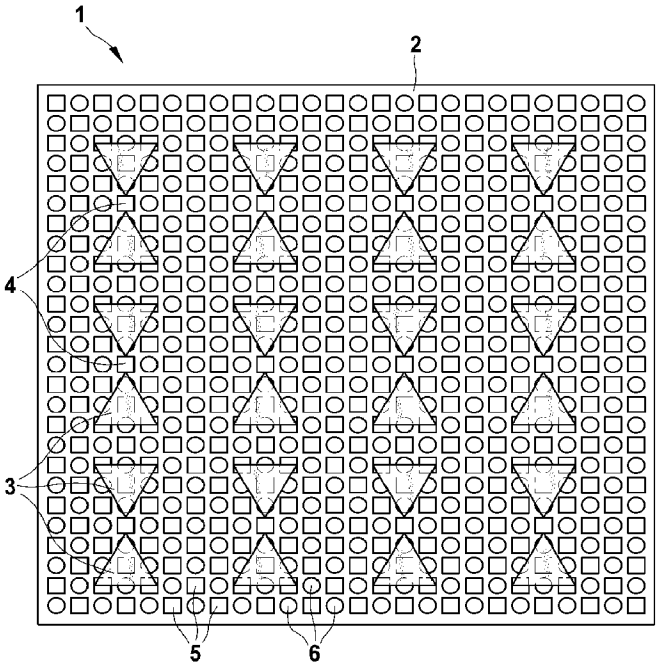

Fig. 1

(57) **Abstract**: The present invention relates to a multispectral sensor (1) comprising a complementary metal oxide semiconductor substrate (2) with a switching circuit, at least one antenna (3) - receiving means (4) combination device for detecting teraherz radiation, at least one other bolometer (5) for detecting mid-ranged infrared radiation and at least one diode (6) for detecting radiation in the visible to near infrared range, a multispectral imaging and/or spectroscopy system, method for detecting and/or examining life forms, objects and materials using such a system, as well as the use of such a sensor (1) and system.

(57) **Zusammenfassung**: Die vorliegende Erfindung betrifft einen multispektralen Sensor (1), der ein komplementäres Metall-Oxid-Halbleiter-Substrat (2) mit Schaltkreis, mindestens eine Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtung zur Detektion von Terahertzstrahlung, mindestens ein weiteres Bolometer (5) zur Detektion von mittlerer Infrarotstrahlung, und mindestens eine Diode (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs umfasst, ein multispektrales Bildgebungs- und/oder Spektroskopie-System, Verfahren zur Detektion und/oder Untersuchung von Lebewesen, Gegenständen und Materialien mit einem derartigen System sowie die Verwendung eines derartigen Sensors (1) und Systems.

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(84) **Bestimmungsstaaten** *(soweit nicht anders angegeben, für jede verfügbare regionale Schutzrechtsart)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), eurasisches (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), europäisches (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Veröffentlicht:

— *mit internationalem Recherchenbericht (Artikel 21 Absatz 3)*

— *vor Ablauf der für Änderungen der Ansprüche geltenden Frist; Veröffentlichung wird wiederholt, falls Änderungen eingehen (Regel 48 Absatz 2 Buchstabe h)*

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Titel

Multispektraler Sensor

Beschreibung

Die vorliegende Erfindung betrifft einen multispektralen Sensor zur Detektion von Terahertzstrahlung, Infrarotstrahlung und Strahlung des sichtbaren bis nahen Infrarot-Bereichs, ein multispektrales Bildgebungs- und/oder Spektroskopie-System, ein Verfahren zur Detektion und/oder Untersuchung von Lebewesen, Gegenständen und Materialien mit einem derartigen System sowie die Verwendung eines derartigen Sensors und Systems.

Stand der Technik

Das elektromagnetische Spektrum kann im Bereich des Terahertz-Frequenzbandes Informationen über die komplexe chemische Zusammensetzung von Stoffen, sowie über die dielektrischen Eigenschaften von Gegenständen geben. Für diese Anwendung werden derzeit recht komplexe Systeme verwendet, die beispielsweise gepulste Laserquellen enthalten. Ein wesentlicher Schwachpunkt der angebotenen Terahertz-Systeme besteht neben der Komplexität darin, dass eine Messung allein im Terahertz-Frequenzband wenig aussagekräftig ist und häufig durch parallele Messungen im sichtbaren oder infraroten Frequenzband ergänzt werden muss. Dies erfolgt herkömmlicherweise durch die parallele Verwendung mehrerer Detektoren oder Detektierungssysteme, die eine komplexe gegenseitige optische Ausrichtung erfordern, was hohe Kosten des Gesamtsystems zur Folge hat.

Offenbarung der Erfindung

Vorteile der Erfindung

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Der erfindungsgemäße multispektrale Sensor umfassend

- ein komplementäres Metall-Oxid-Halbleiter-Substrat mit Schaltkreis, und
- mindestens eine Antenne-Empfängermittel-Kombinationsvorrichtung zur Detektion von Terahertzstrahlung, und
- mindestens eine Vorrichtung zur Detektion von mittlerer Infrarotstrahlung, und
- mindestens eine Diode zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs

hat zum einen den Vorteil, dass alle Bauelemente des Sensors bei Raumtemperatur betrieben werden können. Daher bedarf ein erfindungsgemäßer Sensor **1** keiner Kühlung, insbesondere keiner kryoskopischen Kühlung. Zum anderen hat der erfindungsgemäße Sensor **1** den Vorteil, dass darauf verschiedenen Funktionen auf einem einzigen Bauteil vereint werden, wodurch vorteilhafterweise ein einziger Sensor zur Bewältigung komplexer Detektierungsanwendungen genügt. Darüber hinaus entfällt vorteilhafterweise das aufwendige Einstellen verschiedener Sensoren und es wird nur eine einzige breitbandige, vorzugsweise reflektive, Optik benötigt. Der erfindungsgemäße Sensor ermöglicht weiterhin vorteilhafterweise eine parallele, im Idealfall Echtzeit-Detektion von elektromagnetischer Strahlung im sichtbaren-nah-infraroten, mittel-infraroten und Terahertz-Bereich. Ferner können die erfindungsgemäßen Sensoren langfristig betrachtet zu niedrigen Produktionsstückkosten hergestellt werden, was auch eine Anwendung in Massenprodukten ermöglicht.

Zeichnungen

Weitere Vorteile und vorteilhafte Ausgestaltungen des erfindungsgemäßen Gegenstandes werden durch die Zeichnungen veranschaulicht und in der nachfolgenden Beschreibung erläutert. Dabei ist zu beachten, dass die Figuren nur beschreibenden Charakter haben und nicht dazu gedacht sind, die Erfindung in irgendeiner Form einzuschränken.

Fig. 1 zeigt eine Draufsicht auf eine Ausführungsform eines erfindungsgemäßen multispektralen Sensors.

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Figur 1 zeigt, dass der erfindungsgemäße Sensor **1** ein komplementäres Metall-Oxid-Halbleiter-Substrat **2** mit einem nicht dargestellten Schaltkreis umfasst. Derartige Substrate werden üblicherweise auch als CMOS-Substrat („complementary metal oxide semiconductor") bezeichnet. Erfindungsgemäß sind auf dem CMOS-Substrat **2** mindestens eine Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zur Detektion von Terahertzstrahlung, mindestens eine Vorrichtung **5** zur Detektion von mittlerer Infrarotstrahlung und mindestens eine Diode **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs angeordnet.

Im Rahmen der vorliegenden Erfindung wird unter dem Begriff „Terahertzstrahlung" elektromagnetische Strahlung in einem Bereich von etwa ≥ 15 µm bis etwa ≤ 1000 µm, und unter dem Begriff „mittlerer Infrarotstrahlung" elektromagnetische Strahlung in einem Bereich von etwa ≥ 1 µm bis etwa < 15 µm, und unter dem Begriff „Strahlung des sichtbaren bis nahen Infrarot-Bereichs" elektromagnetische Strahlung in einem Bereich von etwa $\geq 0{,}380$ µm bis etwa < 1 µm, verstanden.

Das Detektierungsintervall des erfindungsgemäßen Sensors **1** kann im Terahertz-Bereich sowohl $> 0{,}3$ Terahertz bis ≤ 20 Terahertz als auch beispielsweise $\geq 0{,}3$ Terahertz oder $\geq 0{,}5$ Terahertz oder ≥ 1 Terahertz bis ≤ 3 Terahertz oder ≤ 5 Terahertz oder ≤ 10 Terahertz, sein. Entsprechend kann das Detektierungsintervall des erfindungsgemäßen Sensors **1** im Terahertz-Bereich sowohl ≥ 15 µm bis < 1000 µm als auch beispielsweise ≥ 30 µm oder ≥ 60 µm oder ≥ 100 µm bis ≤ 300 µm oder ≤ 600 µm oder < 1000 µm, sein.

Ebenso kann das Detektierungsintervall des erfindungsgemäßen Sensors **1** im mittleren Infrarot-Bereich sowohl > 20 Terahertz bis ≤ 300 Terahertz als auch $\geq 21{,}4$ Terahertz bis $\leq 37{,}5$ Terahertz oder ≥ 60 Terahertz oder ≤ 100 Terahertz, sein. Entsprechend kann das Detektierungsintervall des erfindungsgemäßen Sensors **1** im mittleren Infrarot-Bereich sowohl ≥ 1 µm bis etwa < 15 µm als auch beispielsweise ≥ 3 µm bis ≤ 5 µm oder ≥ 8 µm bis ≤ 14 µm, sein.

Analog kann das Detektierungsintervall des erfindungsgemäßen Sensors **1** im sichtbaren bis nah-infraroten Bereich > 300 Terahertz bis ≤ 790 Terahertz sein.

Im Rahmen der vorliegenden Erfindung muss eine Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zur Detektion von Terahertzstrahlung beziehungsweise eine Vorrichtung **5** zur Detektion von mittlerer Infrarotstrahlung beziehungsweise eine Diode **6** zur

Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs folglich nicht den kompletten jeweiligen Strahlungsbereich detektieren.

Im Rahmen einer bevorzugten Ausführungsform der vorliegenden Erfindung weist der erfindungsgemäße Sensor **1** mindestens zwei unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern auf.

Eine Unterteilung des Terahertz-Bereichs in mindestens zwei, insbesondere schmalbandige, Unterbänder, hat den Vorteil, dass sich schmalbandige Antennen **3** besser an das Empfangsmittel **4** anpassen, insbesondere koppeln, lassen, wodurch bei geeigneter Anordnung die Empfindlichkeit („Performance") des Gesamtsystems verbessert werden kann.

Der erfindungsgemäße Sensor **1** weist daher vorzugsweise mindestens zwei unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen auf, die derart ausgebildet sind, dass der Terahertz-Bereich in mindestens zwei, insbesondere schmalbandige, Unterbänder aufgeteilt wird, welche den Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zugeordnet sind.

Darüber hinaus kann der erfindungsgemäße Sensor **1** mindestens zwei unterschiedliche Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern aufweisen.

Ferner kann der erfindungsgemäße Sensor **1** auch mindestens zwei unterschiedliche Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern aufweisen.

Wie Figur 1 zeigt, weist ein erfindungsgemäßer Sensor **1** vorzugsweise eine Vielzahl, beispielsweise gleicher und/oder unterschiedlicher (nicht dargestellt), Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs auf.

Als Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtung haben sich im Rahmen der vorliegenden Erfindung Antenne-Bolometer-Kombinationsvorrichtungen und/oder Antenne-

Diode-Kombinationsvorrichtungen, insbesondere Antenne-Bolometer-, Antenne-Schottky-Diode- und/oder Antenne-MIM-Diode-Kombinationsvorrichtungen, als besonders vorteilhaft erwiesen, da derartige Kombinationsvorrichtungen keine Kühlung, insbesondere keine kryoskopische Kühlung benötigen. Dabei wird im Sinn der vorliegenden Erfindung unter einer MIM-Diode eine Metall-Isolator-Metall-Diode („metal insulator metal diode") verstanden. Die Variation dieser unterschiedlichen **3**-Empfängermittel-**4**-Kombinationsvorrichtungen bietet eine Möglichkeit unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

Im Rahmen der vorliegenden Erfindung weist eine Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtung mindestens eine an das Empfängermittel **4**, insbesondere kapazitiv, gekoppelte Antennen **3** auf. Die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtung kann jedoch auch mindestens zwei Antennen **3** aufweisen, welche an das Empfängermittel **4**, insbesondere kapazitiv, gekoppelt sind. Die Zahl der Antennen bietet eine weitere Möglichkeit unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

Beim Einsatz eines Bolometers als Empfängermittel **4** dient die Antenne **3** dazu Terahertzstrahlung zu absorbieren, welche in dem mit der Antenne **3**, insbesondere kapazitiv, gekoppelten Bolometer in Wärme umgewandelt wird, wobei eine resultierende Widerstandsänderung des Bolometers gemessen wird. Bei dem Bolometer kann es sich dabei um ein Mikrobolometer handeln. Das Bolometer **4** kann im Rahmen der vorliegenden Erfindung ein in etwa $\geq 25\ \mu m^2$ bis $\leq 4900\ \mu m^2$, insbesondere $\geq 625\ \mu m^2$ bis $\leq 2500\ \mu m^2$, großes schichtförmiges Substrat aufweisen, welches mittels zwei elektrisch leitenden Stützen beabstandet zu dem CMOS-Substrat **2** angeordnet ist. Dabei kann das schichtförmige Substrat sowohl polygon, insbesondere rechteckig und/oder viereckig, als auch im Wesentlichen unrund, insbesondere ellipsoid oder kreisförmig, ausgestaltet sein. Das schichtförmige Substrat kann dabei amorphes Silizium oder Vanadiumoxid umfassen. Das schichtförmige Substrat kann beispielsweise parallel zu dem CMOS-Substrat **2** angeordnet sein. Die Bolometerausgestaltung bietet eine weitere Möglichkeit unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

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Beim Einsatz einer Diode **4**, insbesondere einer Schottky- oder MIM-Diode, als Empfängermittel **4** wird das von der Antenne **3** empfangene Terahertzsignal gleichgerichtet beziehungsweise bei einer heterodynen Empfangslösung mit einem weiteren Terahertzsignal in ein Zwischenfrequenzsignal gemischt. Die Diodenausgestaltung bietet eine weitere Möglichkeit unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

Im Rahmen der vorliegenden Erfindung können mehrere, insbesondere alle, Antennen **3**, wie in Figur 1 gezeigt, in einer Ebene angeordnet sein. Ebenso können im Rahmen der vorliegenden Erfindung mehrere, insbesondere alle, Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung beziehungsweise mehrere, insbesondere alle, Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs jeweils in einer Ebene angeordnet sein. Wie in Figur **1** gezeigt, können die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs dabei in einer gemeinsamen Ebene angeordnet sein.

Im Rahmen einer Ausführungsform der vorliegenden Erfindung ist mindestens eine Antenne **3** beziehungsweise sind die Antennen **3** der Antennenebene bezüglich mindestens einer Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und/oder mindestens einer Diode **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs, insbesondere bezüglich der Ebene der Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und/oder der Ebene der Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs, strahlungsseitig angeordnet.

Durch unterschiedliche Antennendesigns können Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen Absorptionseigenschaften hinsichtlich Frequenz und Polarisation im Terahertzband realisiert werden. Unterschiedliche Antennendesigns bieten eine weitere, insbesondere bevorzugte, Möglichkeit unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

Dabei kann eine Antenne **3** sowohl wie in Figur 1 gezeigt flächig als auch nicht-flächig ausgestaltet sein. Beispielsweise kann eine Antenne **3** im Rahmen der vorliegenden Erfindung

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polygon, insbesondere dreieckig, rechteckig und/oder viereckig, im Wesentlichen unrund, insbesondere ellipsoid oder kreisförmig, oder spiralförmig ausgestaltet sein.

Im Rahmen einer Ausführungsform der vorliegenden Erfindung weist der erfindungsgemäße Sensor **1** mindestens zwei Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichem Antennendesign auf. Beispielsweise können mehrere Antennendesigns, insbesondere selektiv, auf einem Sensor **1** kombiniert werden, welche mehrere, beispielsweise beabstandete, Frequenzbänder im Terahertz-Bereich zur Folge haben, welche auf spezielle zu detektierende Frequenzbereiche, beispielsweise für Sprengstoffe charakteristische Frequenzbereiche, abgestimmt sind und dadurch dem erfindungsgemäßen Sensor **1** vorteilhafterweise eine Spektroskopie- und/oder Frequenzselektions-Funktion verleihen.

Im Rahmen einer bevorzugten Ausführungsform der vorliegenden Erfindung weist der erfindungsgemäße Sensor **1** daher mindestens zwei unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen auf, die, insbesondere durch unterschiedliche Antennendesigns, auf spezielle/bevorzugt zu detektierende Frequenzbereiche im Terahertz-Bereich abgestimmt sind.

Im Rahmen einer bevorzugten Ausführungsform der vorliegenden Erfindung umfasst eine Antenne **3** eine, insbesondere dünne, Metallschicht und/oder Halbleiterschicht und/oder eine Schicht aus einem oder mehreren elektrisch leitenden Polymeren und/oder eine auf Kohlenstoffnanoröhren („carbon nanotubes“) basierende Schicht. Insbesondere kann eine Antenne **3** dabei aus einer, insbesondere dünnen, Metallschicht oder Halbleiterschicht oder Schicht aus einem oder mehreren elektrisch leitenden Polymeren oder auf Kohlenstoffnanoröhren („carbon nanotubes“) basierenden Schicht ausgebildet sein. Beispielsweise kann die Metallschicht aus Gold ausgebildet sein. Die Halbleiterschicht kann aus einem Halbleiter mit einer breiten Bandlücke („wide band gap semiconductor“), beispielsweise Indium-Zinn-Oxyd, Zinkoxid, Alluminiumnitrid, Galliumnitrid, und/oder Siliciumcarbid, insbesondere dotiertes Indium-Zinn-Oxyd, Zinkoxid, Alluminiumnitrid, Galliumnitrid, und/oder Siliciumcarbid, ausgebildet sein.

Im Rahmen einer besonders bevorzugten Ausführungsform der vorliegenden Erfindung ist die Metallschicht und/oder Halbleiterschicht durchlässig für Strahlung des sichtbaren bis nahen Infrarot-Bereichs und/oder des mittleren Infrarot-Bereichs. Dies hat den Vorteil, dass unterhalb der Antenne/n **3** einer Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtung eine oder mehrere Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und/oder eine oder

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mehrere Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs angeordnet sein können. Dabei dient der Begriff „unterhalb" nicht dazu die Ausrichtung bezüglich der Gravitationsrichtung, sondern bezüglich der erwarteten Strahlungsrichtung zu definieren, wobei „unterhalb einer Antenne" als auf der strahlungsabgewandten Seite einer Antenne **3** zu verstehen ist.

Im Rahmen der in Figur 1 gezeigten Ausführungsform sind unterhalb den Antennen **3** beziehungsweise zwischen den Antennen **3** und dem komplementären Metall-Oxid-Halbleiter-Substrat **2** zahlreiche Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs angeordnet. Dabei besteht zwischen den Antennen **3** und den Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung beziehungsweise den Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs keine galvanisch leitende Verbindung. Dabei bedeutet „keine galvanisch leitende Verbindung", dass keine „direkte" Leitung über eine, beispielsweise metallische, Leitung vorliegt, wobei eine kapazitive und/oder induktive „indirekte" Leitung nicht ausgeschlossen ist. Eine galvanisch leitende Verbindung zwischen den Antennen **3** und den Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung beziehungsweise den Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs kann beispielsweise dadurch vermieden werden, dass die Antennen **3** auf einem oder mehreren, nicht dargestellten, Träger/n, beispielsweise einer Trägerschicht, insbesondere aus einem oder mehreren nicht galvanisch leitenden Polymeren, aus einem galvanisch nicht-leitenden Material angeordnet sind.

Als Vorrichtung **5** zur Detektion von mittlerer Infrarotstrahlung können im Rahmen der vorliegenden Erfindung Bolometer und/oder MIM-Dioden eingesetzt werden. Der Einsatz von Bolometern und MIM-Dioden bietet daher eine Möglichkeit unterschiedliche Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen. Beim Einsatz von Bolometern **5** als Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung sind die Bolometer **5** vorzugsweise, wie in Figur 1 gezeigt, freistehend ausgebildet und angeordnet.

Als Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung eignet sich beispielsweise ein Bolometer, welches ein in etwa $\geq 25\ \mu m^2$ bis $\leq 4900\ \mu m^2$, insbesondere $\geq 625\ \mu m^2$ bis $\leq 2500\ \mu m^2$, großes schichtförmiges Substrat aufweist. Das schichtförmige Substrat kann dabei insbesondere mittels zwei galvanisch leitenden Stützen beabstandet zu dem CMOS-Substrat **2** angeordnet sein. Dabei kann das schichtförmige Substrat sowohl polygon, insbesondere

rechteckig und/oder viereckig, als auch im Wesentlichen unrund, insbesondere ellipsoid oder kreisförmig, ausgestaltet sein. Das schichtförmige Substrat kann dabei amorphes Silizium oder Vanadiumoxid umfassen. Das schichtförmige Substrat ist vorzugsweise parallel zu dem CMOS-Substrat **2** angeordnet. Durch den Abstand zwischen dem schichtförmigen Substrat und dem CMOS-Substrat **2** kann dabei vorteilhafterweise der Wellenlängenbereich der zu detektierenden Strahlung eingestellt werden. Für eine optimale Detektion entspricht der Abstand vorzugsweise einem Viertel der Wellenlänge der zu detektierenden Strahlung. Eine Änderung des Abstands zwischen dem schichtförmigen Substrat und dem CMOS-Substrat **2** bietet daher eine weitere Möglichkeit unterschiedliche Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

Als Dioden eignen sich beispielsweise Dioden, insbesondere Fotodioden, die in CMOS-bildgebenden Detektoren verwendet werden.

Wie Figur 1 veranschaulicht kann der erfindungsgemäße Sensor **1**, insbesondere ein Teil des erfindungsgemäßen Sensors **1**, beispielsweise das CMOS-Substrat **2**, die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtung/en, die Vorrichtung/en **5** zur Detektion von mittlerer Infrarotstrahlung und die Diode/n **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs des Sensors **1**, vorteilhafterweise monolithisch ausgestaltet sein. Dabei bedeutet der Begriff „monolithisch“, dass die Einheiten **2, 3, 4, 5, 6** des Sensors **1** eine, insbesondere untrennbare, Einheit bilden. Insbesondere kann es sich bei dem erfindungsgemäßen Sensor um einen monolithisch integrierten Chip handeln.

Der in Figur 1 nicht dargestellte Schaltkreis, die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs sind im Rahmen der vorliegenden Erfindung vorzugsweise derart ausgebildet und angeordnet, dass die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs, insbesondere unabhängig voneinander, beschaltet und/oder ausgelesen werden können. Zum Auswerten der ausgelesenen Messergebnisse weist der erfindungsgemäße Sensor **1** vorzugsweise eine Auswertelektronik auf. Darüber hinaus weist der Sensor vorzugsweise eine multispektrale Optik, beispielsweise eine reflektive Optik auf der Basis von Spiegeln, auf. Eine derartige multispektrale Optik ist zweckmäßigerweise bezüglich der auf dem CMOS-Substrat **2** angeordneten Bauelemente **3, 4, 5, 6** strahlungsseitig angeordnet.

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Die Auswertelektronik und multispektrale Optik kann, muss jedoch nicht, in den monolithischen Teil des Sensors **1** integriert sein.

Figur 1 zeigt, dass die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs rasterförmig angeordnet sein können. Dementsprechend können die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs auch als „Pixel" bezeichnet werden. Im Rahmen einer Ausführungsform der vorliegenden Erfindung sind die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs als Pixel eines Rasters von mindestens 20 mal 20, beispielsweise von mindestens 50 mal 50, insbesondere von mindestens 100 mal 100, Pixeln auf dem Sensor **1** angeordnet. Die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs können dabei in einem symmetrischen Muster auf dem Sensor **1** angeordnet sein. Vorzugsweise sind die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs dabei, wie in Figur 1 gezeigt, gleichmäßig auf dem Sensor **1** verteilt angeordnet. Insbesondere können dabei die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs alternierend angeordnet sein. Die Zahl an Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen kann im Rahmen der vorliegenden Erfindung geringer als die der Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und der Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs sein. Die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen können dann beispielsweise, wie in Figur 1 gezeigt, in regelmäßigen Abständen anstelle von einer Vorrichtung **5** zur Detektion von mittlerer Infrarotstrahlung oder Diode **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs in der ansonsten alternierenden Anordnung von Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs angeordnet werden.

Das Verhältnis von Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zu Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung kann im Rahmen der vorliegenden Erfindung in einem Bereich von $\geq$ 1:100 bis $\leq$ 100:1, beispielsweise von $\geq$ 1:50

bis ≤ 50:1, insbesondere von ≥ 1:30 bis ≤ 30:1, und/oder das Verhältnis von Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zu Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs in einem Bereich von ≥ 1:100 bis ≤ 100:**1**, beispielsweise von ≥ 1:50 bis ≤ 50:**1**, insbesondere von ≥ 1:30 bis ≤ 30:**1**, und/oder das Verhältnis von Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung zu Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs in einem Bereich von ≥ **1**:50 bis ≤ 50:**1**, beispielsweise von ≥ 1:10 bis ≤ 10:1, insbesondere von ≥ 1:3 bis ≤ 3:1, liegen. Beispielsweise kann das Verhältnis von Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zu Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung ≥ 1:5, beispielsweise ≥ 1:10, insbesondere ≥ 1:20 , und/oder das Verhältnis von Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zu Dioden **6** ≥ 1:5, beispielsweise ≥ 1:10, insbesondere von ≥ **1**:20, und/oder das Verhältnis von Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung zu Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs etwa **1**:**1**, sein.

Ferner betrifft die vorliegende Erfindung ein multispektrales Bildgebungs- und/oder Spektroskopie-System, welches einen erfindungsgemäßen Sensor **1**, welcher als Detektor dient, und eine Terahertzstrahlungsquelle aufweist. Dabei können der Sensor **1** und die Terahertzstrahlungsquelle bezüglich des zu untersuchenden Objektes sowohl derart angeordnet sein, dass der Sensor **1** die nach dem Durchstrahlen des Objektes verbleibende Strahlung detektiert als auch dass der Sensor **1** die von dem Objekt reflektierte und/oder gestreute Strahlung detektiert. Folglich können die Terahertzstrahlungsquelle, der Sensor **1** und das Objekt sowohl entlang einer Achse angeordnet sein, wobei das Objekt zwischen der Terahertzstrahlungsquelle und dem Sensor angeordnet ist, als auch nicht entlang einer Achse zueinander angeordnet sein.

Das erfindungsgemäße System ermöglicht vorteilhafterweise eine Echtzeit-Spektroskopie im Terahertz-Bereich sowie eine bildgebende Detektierung im Terahertz-Bereich sowie im Infrarot- und sichtbaren und nah-infraroten Bereich.

Darüber hinaus betrifft die vorliegende Erfindung ein Verfahren zur Detektion und/oder Untersuchung von Lebewesen, insbesondere Menschen und Tieren, Gegenständen und Materialien, mit einem erfindungsgemäßen System. Insbesondere kann dieses Verfahren auf Frequenzbereichsspektroskopie basieren. Vorzugsweise strahlt die Terahertzquelle in dem erfindungsgemäßen Verfahren ein schmales Terahertzband, beispielsweise mit einer Breite von

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etwa ≥ 20 Gigahertz bis etwa ≤ 200 Gigahertz, insbesondere von etwa ≥ 60 Gigahertz bis etwa ≤ 100 Gigahertz, aus, welches innerhalb eines breiten Frequenzbereichs, beispielsweise in einem Bereich von etwa ≥ 0,3 Terahertz bis etwa ≤ 20 Terahertz, beispielsweise von ≥ 0,3 Terahertz oder von ≥ 0,5 Terahertz oder von ≥ 1 Terahertz bis ≤ 3 Terahertz oder bis ≤ 5 Terahertz oder bis ≤ 10 Terahertz, verändert wird, wobei die transmittierte, reflektierte und/oder gestreute Strahlung durch den erfindungsgemäßen Sensor **1** detektiert, insbesondere gemessen wird. Das Messergebnis des erfindungsgemäßen Sensors **1** kann dabei durch ein Ausgabegerät, beispielsweise ein Display, einen Bildschirm oder einen Drucker, ausgegeben werden.

Weiterhin betrifft die vorliegende Erfindung die Verwendung eines erfindungsgemäßen Sensors **1**, eines erfindungsgemäßen Systems und/oder eines erfindungsgemäßen Verfahrens im Überwachungs/Sicherheitstechnik-, Transport-, Produktions-, Life-Science- und/oder Gesundheitsbereich. Insbesondere betrifft die vorliegende Erfindung die Verwendung eines erfindungsgemäßen Sensors **1**, eines erfindungsgemäßen Systems und/oder eines erfindungsgemäßen Verfahrens zur Detektion und/oder Untersuchung von Lebewesen, insbesondere Menschen und Tieren, Gegenständen und Materialien, insbesondere Sprengstoffen, beispielsweise bei Sicherheitskontrollen an Grenzen, in Transitgebäuden, wie Flughäfen und Bahnhöfen, in Transportmitteln, wie Bahnen, Bussen, Flugzeugen und/oder Schiffen, und/oder bei Großveranstaltungen, zur Einbruchssicherung von Gebäuden, Räumen und Fortbewegungsmitteln, zu medizinischen Zwecken und/oder zur zerstörungsfreien Überprüfung eines Werkstücks („non-destructive testing"), insbesondere von Werkstücken aus Kunststoff.

Ansprüche

1. Multispektraler Sensor (1), umfassend

   - ein komplementäres Metall-Oxid-Halbleiter-Substrat (2) mit Schaltkreis, und
   - mindestens eine Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtung zur Detektion von Terahertzstrahlung, und
   - mindestens eine Vorrichtung (5) zur Detektion von mittlerer Infrarotstrahlung, und
   - mindestens eine Diode (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs.

2. Sensor (1) nach Anspruch 1, dadurch gekennzeichnet, dass

   - die Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtung eine Antenne-Bolometer-Kombinationsvorrichtung oder eine Antenne-Diode-Kombinationsvorrichtung, insbesondere eine Antenne-Bolometer-, Antenne-Schottky-Diode- oder eine Antenne-Metall-Isolator-Metall-Diode-Kombinationsvorrichtung, und/oder
   - die Vorrichtung (5) zur Detektion von mittlerer Infrarotstrahlung ein Bolometer oder eine Metall-Isolator-Metal-Diode,

   ist.

3. Sensor (1) nach Anspruch 1 oder 2, dadurch gekennzeichnet, dass der Sensor (1)

   - mindestens zwei unterschiedliche Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern; und/oder
   - mindestens zwei unterschiedliche Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern, und/oder,

- mindestens zwei unterschiedliche Diode (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern,

aufweist.

4. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass der Sensor (1) mindestens zwei unterschiedliche Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen aufweist, die derart ausgebildet sind, dass der Terahertz-Bereich in mindestens zwei Unterbänder aufgeteilt wird, welche den Antenne-3-Empfängermittel-4-Kombinationsvorrichtungen zugeordnet sind.

5. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass der Sensor (1) mindestens zwei Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen mit unterschiedlichem Antennendesign aufweist.

6. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass der Sensor (1) mindestens zwei unterschiedliche Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen auf, die auf bevorzugt zu detektierende Frequenzbereiche im Terahertz-Bereiche abgestimmt sind.

7. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass der Sensor (1) eine Vielzahl von Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen, Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung und Dioden (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs aufweist, wobei die Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen, Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung und Dioden (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs rasterförmig angeordnet sind.

8. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen, Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung und Dioden (6) zur Detektion von Strahlung des

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sichtbaren bis nahen Infrarot-Bereichs als Pixel eines Rasters von mindestens 20 mal 20, beispielsweise von mindestens 50 mal 50, insbesondere von mindestens 100 mal 100, Pixeln auf dem Sensor (1) angeordnet sind.

9. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen, Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung und Dioden (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs in einem symmetrischen Muster auf dem Sensor (1) angeordnet sind.

10. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die Antenne/n (3) eine Metallschicht und/oder eine Halbleiterschicht und/oder eine Schicht aus einem oder mehreren elektrisch leitenden Polymeren und/oder eine auf Kohlenstoffnanoröhren basierende Schicht umfassen, welche durchlässig für Strahlung des sichtbaren bis nahen Infrarot-Bereichs und/oder Infrarotstrahlung ist.

11. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass unterhalb der Antenne/n (3) einer Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen eine oder mehrere Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung und/oder eine oder mehrere Dioden (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs angeordnet sind.

12. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die Antenne/n (3) auf einem oder mehreren Träger/n aus einem galvanisch nicht-leitenden Material angeordnet sind.

13. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass der Sensor (1) eine multispektrale Optik, insbesondere eine reflektive Optik, und/oder eine Auswertelektronik aufweist.

14. Multispektrales Bildgebungs- und/oder Spektroskopie-System, umfassend einen Sensor nach einem der vorhergehenden Ansprüche und eine Terahertzstrahlungsquelle.

15. Verfahren zur Detektion und/oder Untersuchung von Lebewesen, insbesondere Menschen und Tieren, Gegenständen und Materialien, mit einem System nach Anspruch 14, in dem die Terahertzquelle ein schmales Terahertzband ausstrahlt, welches innerhalb eines breiten Frequenzbereichs verändert wird, wobei die transmittierte, reflektierte und/oder gestreute Strahlung durch den erfindungsgemäßen Sensor (1) detektiert wird.

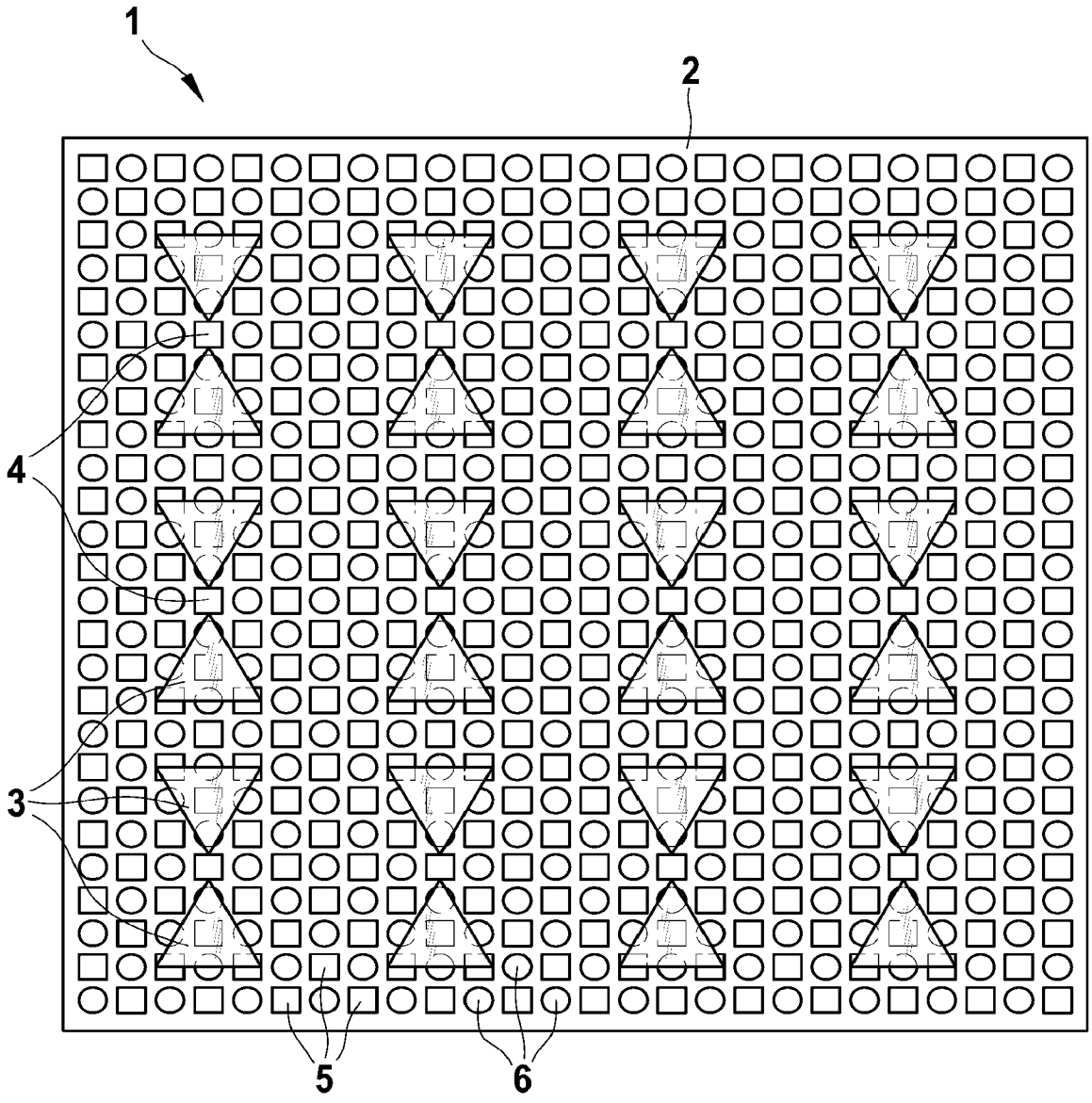

Fig. 1

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
25 March 2010 (25.03.2010)

PCT

(10) International Publication Number
WO 2010/033127 A1

(51) International Patent Classification:
H01L 27/146 (2006.01)

(21) International Application Number:
PCT/US2008/077209

(22) International Filing Date:
22 September 2008 (22.09.2008)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: RESPONSE-ENHANCED MONOLITHIC-HYBRID PIXEL

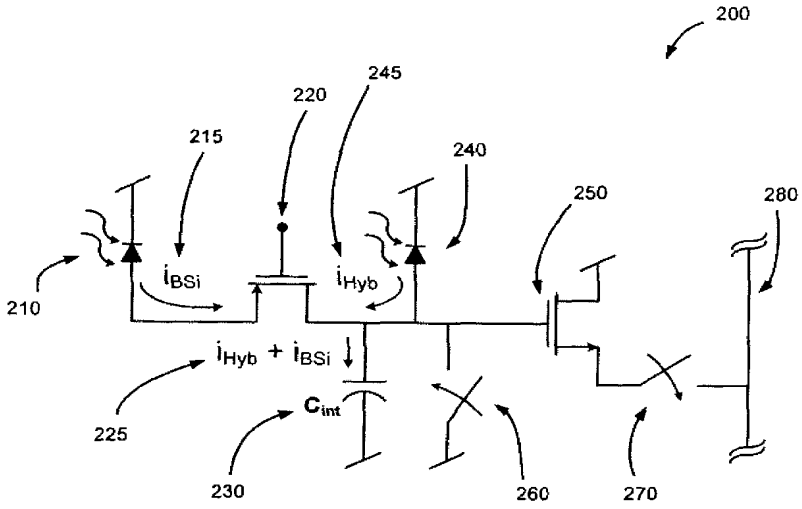

Fig. 2

(57) **Abstract**: A light-sensing pixel is described that includes more than one detector element, each of which is sensitive to a range of wavelengths of the electromagnetic spectrum. The detectors are arranged in a readout circuit that can be constructed on a monolithic semiconductor product such that one or more of the detectors can be switched on or off to include or exclude an output contribution from said detectors and enhance the response of the pixel. Also, the detectors can included a laser-treated semiconductor sensor for efficient sensing of radiation in one or more regions of the spectrum. Arrays and imaging products using such pixels are disclosed.

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RESPONSE-ENHANCED MONOLITHIC-HYBRID PIXEL

I. TECHNICAL FIELD

[0001] The present disclosure relates to the detection of electromagnetic radiation, and more particularly, to methods and articles for detecting such radiation using monolithic or hybrid semiconductor-based designs that have improved response to incident radiation.

II. RELATED APPLICATIONS

[0002] N/A

III. GOVERNMENT FUNDING

[0003] N/A

IV. BACKGROUND

[0004] Pixels, or "picture elements," are the basic light- or color-detection and display elements that form a digital image. Typical digital video and imaging systems use a collection of detector pixels to capture a two-dimensional image field at a capture end (such as a camera) and another corresponding collection of display pixels to display the corresponding two-dimensional image at a display end (such as a monitor). In digital imaging systems, an array of light-sensitive pixels, each including a light sensor or detector, respond to an intensity of incident light at each pixel location, providing an electrical output representative of the incident light. The output of an imager can be referred to as an image.

[0005] Motion or video cameras repeat the process described above, but permit a time-sequence to be captured, for example at regular intervals, so that the captured images can be replayed to recreate a dynamic scene or sequence.

[0006] Most film and digital pixel imagers include wavelength-specific sensors or detectors. The chemical composition of the film or the design of the digital pixels and associated filters determines the range of wavelengths of light to which the film or pixels respond. Practically, a detector or imager has a frequency response that is optimized to provide images of light in the range of wavelengths the imager is designed for. The most common examples are sensitive to visible light (e.g., red, green, blue, and combinations thereof). Visible light corresponds to

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the range of wavelengths of electromagnetic radiation to which our eyes are sensitive, and is generally in the range of 400 to 750 nanometers (nm).

[0007] Special film and digital pixel imagers are designed for low-light operation to provide night vision capability for military, security, or other special applications in which an illumination source is not available to cause a visible light image. Low-light or night vision imagers rely on detecting and imaging frequencies below (wavelengths longer than) the visible (red) wavelengths, and are sometimes called infra-red (IR) detectors. IR detection is more suited for picking up heat emissions from objects such as a person's body or a vehicle. IR radiation itself can be roughly divided into sub-spectra including the near-infra-red (NIR) having wavelengths between about 750 to 1100 nm, short-wave-infra-red (SWIR) having wavelengths between about 1100 and 2500 nm, medium-wave-infra-red (MWIR) having wavelengths between about 2500 and 8000 nm, and long-wave-infra-red (LWIR) having wavelengths between about 8000 and 12000 nm. These ranges are defined somewhat arbitrarily, and are given merely for simplifying the following discussion, and those skilled in the art will appreciate the generality of the discussion as it relates to the bands of wavelengths of the electromagnetic spectrum.

[0008] Present visible light imaging cameras have used silicon devices made with CID, CCD, or CMOS APS architectures. The low cost and efficient collection of photons from 400-750nm wavelengths has enabled silicon devices. Extending the use of silicon imagers into the near infrared (NIR) band requires a greater volume of material to detect these wavelengths because of silicon's relatively low absorption coefficient in this wavelength range. This increases the size of the detectors and causes increased leakage current and requires expensive manufacturing processes or higher voltages to operate. The use of thick silicon substrates also limits the ability to integrate other devices.

[0009] Present low-light or night vision IR imagers are usually less sensitive than would be desired, lack color definition, and have limited frequency response. Also, low-light imagers can be more costly, noisy, and require greater circuit resources than visible light imagers to achieve useful gains in low-signal conditions. Furthermore, IR sensors are larger than would be desired for compact portable applications because most IR sensitive materials must be cooled significantly to achieve good performance. Most sensors that can detect long-

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wavelength portions of the electromagnetic spectrum remain poor at detecting visible light, especially in the short-wavelength portions of the spectrum, for example blue and violet light.

[0010] One presently-available solution is a stacked detector, as described for example in U.S. Pat. No. 6,111,300 to Cao, et al. However, this detector fails to adequately capture radiation in a range suitable for some applications with sufficient sensitivity. In addition, present systems do not generally provide for efficient cost and space-efficient readout circuitry for use with stacked detector elements. Also, such systems lack the flexibility in their design to selectively optimize the detectors for a variety of uses under corresponding conditions.

[0011] In summary, present imaging sensors and pixels do not sufficiently capture the full range of wavelengths useful for developing good images across long and short wavelength portions of the spectrum, and improved detector designs and readout circuit integration is needed for such detectors.

V. SUMMARY

[0012] From the discussion given above it can be appreciated that better detectors capable of operating in a variety of wavelength ranges are desirable. The following discussion provides such improved detection methods and apparatus, including methods and apparatus for detecting light in the IR ranges as well as shorter visible ranges, including in the blue range. Greater bandwidth detectors allow imaging in a variety of lighting conditions, for example in day and night. Embodiments hereof provide silicon-based imagers and detector elements capable of imaging across a range of electromagnetic wavelengths, including in various portions of the IR spectrum and in a wide range of lighting conditions. Additionally, the present embodiments provide compact, thin designs that offer increased sensitivity and resolution at a lower cost than presently available systems. Embodiments hereof provide improved manufacturing and process handling capability for producing the detectors and for implementing readout circuits associated therewith.

[0013] A specific embodiment hereof is directed to a light-sensing pixel for detecting at least a portion of the electromagnetic spectrum, including a first detector element having a laser-treated detector portion for detecting a first range of wavelengths of the electromagnetic spectrum; a second detector element for

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detecting a second range of wavelengths of the electromagnetic spectrum; a collection point for accumulating a first electrical output of said first detector element as well as a second electrical output of said second detector; a bias point for applying a biasing voltage to said first detector element and capable of affecting the first electrical output of said first detector element; and an output point for providing an electrical output of said light-sensing pixel.

[0014] Another embodiment hereof is directed to a light-sensitive array comprising a plurality of pixels as described above, wherein said plurality of pixels each provides an electrical output that can be addressably sensed and contributes to a collective output of said array.

[0015] Yet another embodiment is directed to an imaging apparatus comprising an array of pixels as described above such that an image corresponding to said collective output of said array or pixels can be captured or displayed.

[0016] Other embodiments and uses for the methods and systems given herein can be developed by those skilled in the art upon comprehending the present disclosure.

VI. Brief Description of the Drawings

[0017] For a fuller understanding of the nature and advantages of the present invention, reference is be made to the following detailed description of preferred embodiments and in connection with the accompanying drawings, in which:

[0018] Fig. 1 illustrates an exemplary light-sensing pixel including a black silicon detector element;

[0019] Fig. 2 illustrates an exemplary light-sensing pixel including both a black silicon detector element and another detector element which can be hybridized onto the pixel for enhanced response; and

[0020] Fig. 3 illustrates an exemplary cross-sectional view of a response-enhanced pixel.

VII. Detailed Description

[0021] The present disclosure describes systems and articles of manufacture for providing light sensors, pixels, detectors, or imagers and methods for making and using the same. These methods and apparatus are useful in many applications, including applications benefiting from imaging in a variety of light

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conditions. In some embodiments the detectors and techniques provided herein can be adapted to small, inexpensive, low-power, portable applications such as hand-carried, helmet-mounted and similar applications.

[0022] Some or all embodiments hereof include a sensor or detector sensitive to certain electromagnetic wavelengths and formed into a device on a semiconductor substrate. In some embodiments, the detector includes a portion comprising a semiconductor material, for example silicon, which is irradiated by a short pulse laser to create modified micro-structured surface morphology. The laser processing can be the same or similar to that described in U.S. Patent No. 7,057,256 to Carey et al., which is hereby incorporated by reference. The laser-processed semiconductor is made to have advantageous light-absorbing properties. In some cases this type of material has been called "black silicon" due to its visually darkened appearance after the laser processing and because of its enhanced absorption of light and IR radiation compared to other forms of silicon.

[0023] Generally, the wavelength of the irradiating laser pulse for making black silicon, its fluence, and pulsewidth can affect the morphology of the microstructured surface. In some embodiments, the laser fluence may be between about 1.5 kJ/m^2 and 12 kJ/m^2, but can vary depending on the substrate composition. The choice of the fluence of laser pulses irradiating a silicon wafer to generate a microstructured layer therein can also affect the gettering performance (capacity and/or specificity) of a microstructured substrate. In general, in various embodiments of the invention, the laser pulse fluence is selected to be greater than about 3 kJ/m^2. More preferably, the fluence may be chosen to be in a range of about 3 kJ/m^2 to about 10 kJ/m^2, or a range of about 3 kJ/m^2 to about 8 kJ/m^2.

[0024] Additionally, the laser pulse length can affect the morphology and absorption properties of the treated silicon. Irradiation of a substrate according to the invention can be with femtosecond laser pulses or picosecond or nanosecond pulses. Other factors that can affect microstructures morphology include laser polarization and laser propagation direction relative to the irradiated silicon surface.

[0025] In some embodiments, the laser microstructuring of a substrate is performed in the presence of a mixture of two or more substances where needed to accomplish the present purposes. For example, silicon samples treated in the

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presence of a mixture of SF_6 and Cl_2 exhibit an increase in the microstructure density at higher partial pressure of SF_6.

[0026] We now turn to a description of an exemplary apparatus for detecting electromagnetic radiation or light in at least a range of wavelengths of the electromagnetic spectrum.

[0027] **Fig. 1** illustrates an exemplary pixel 100 comprising a photonic detector 110 of the laser-treated type described above (sometimes referred to as 'black silicon' detector) which can be integrated into a same substrate as the readout circuitry for the pixel. Radiation in certain wavelength ranges incident on pixel 100 is detected by detector 110 and creates a corresponding current i_{BSi} 115, which represents an electrical output, to flow from the detector. A direct injection detector bias 120 is applied to hold a relatively constant voltage across the detector 110.

[0028] Integration capacitance C_{int}, 150 which may be physical or parasitic and represents a collection point, integrates the charge collected by flow of current i_{BSi} 125 through the capacitor 150 over some time. Note that in this embodiment, currents 125 and 115 are equivalent and integrate on C_{int}, 150. A resultant output voltage is provided at the input of signal buffer 160, which represents an output point. Contact post 130 in this exemplary embodiment is not used but may be exposed at the surface of pixel 100, and can be used as will be described below to couple to a hybridized detector element to enhance the response of a pixel. Signal buffer 160 is addressed by column 190 and row enable switch 180 for non-destructive reading of pixel 100. It should be appreciated that a source follower buffer, row switch, and column line are merely examples of a generally-realizable output port, which here includes circuit elements 160, 190, and 180 only by way of example. A reset switch 170 shorts out capacitor 150 thus resetting the collection process. During normal operation detector 110 is reverse biased by the bias voltage applied to terminal 120 as mentioned above.

[0029] In some applications, the pixel 100 and its laser-treated detector 110 allow for detection and sensitivity to long wavelength radiation including in ranges beyond the visible range of the electromagnetic spectrum, such as the near infra-red or the infra-red ranges.

[0030] **Fig. 2** illustrates an exemplary response-enhanced pixel 200 having both a first laser-treated detector element 210 similar to those described above, but

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also includes another light sensitive detector element 240. Second detector 240 may be sensitive to a range of the electromagnetic spectrum that is different from the range of wavelengths that first detector 210 is sensitive to. For example, second detector 240 may be sensitive to shorter wavelengths than first detector 210. More specifically, second detector 240 may be sensitive to wavelengths nearer the blue light or ultraviolet (short) wavelengths of the visible spectrum. As will be described below, this can allow for an overall pixel 200 that has sensitivity to a broad range of wavelengths ranging across those detected by first detector 210 (e.g. longer wavelengths) to those detected by second detector 240 (e.g. shorter wavelengths).

[0031] In this embodiment, a first current or electrical output i_{BSi} 215 from first detector 210 as well as a second current or electrical output i_{Hyb} 245 from second detector 240 are summed and cause an integrated collected charge on collection point or capacitor C_{int} 230 to develop an output voltage at output point or signal buffer 250.

[0032] The pixel 200 can be addressed and read on column 280 and row enable 270 and can contribute to an array of pixels 200 in an imaging product as discussed earlier. Again, a reset switch 260 can be provided to zero out or reset or short out integration capacitor C_{int} 230. As discussed earlier, an generic output port can be used in the present context, of which the present embodiment includes circuit elements 250, 270, and 280 only by way of example.

[0033] In manufacturing such enhanced response detector pixels 200, the second detector element 240 may be hybridized over a monolithic pixel array using the previously-unused post 130 of Fig. 1. The second detector 240 can be selected and constructed such that it provides a great enough output resistance to the circuit of Fig. 2 so that a change in voltage on capacitor C_{int} 230 not to substantially affect the generated photocurrent i_{Hyb} 245 of second detector 240.

[0034] The combination of the detected light and corresponding outputs of detectors 210 and 240 can be used to form enhanced response pixels and enhanced response imaging products having a plurality of pixels such as the exemplary pixel of Fig. 2. Such imaging products can couple a grid of pixels 200 in a two-dimensional format to form sensors such as cameras and scanners that are responsive to a wide range of electromagnetic wavelengths. The output voltage at

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non-destructive signal buffer 250 will thus correspond to, and in some cases be a function of, the photon flux detected at each detector element, 210, 240.

[0035] It should be appreciated that the present disclosure can apply to more than just two detector elements, but rather, three or more detectors could be used, each sensitive to a range of wavelengths in a pixel structure.

[0036] In some embodiments, the structure of the present monolithic-hybrid pixels and the low reverse bias voltages required to bias the black silicon detectors allows selective shutting off of the black silicon detectors in situ. That is, the detectors 110 and 210 of Figs. 1 and 2 may be secured by proper application of bias voltage at terminals 120 and 220, respectively. In the example of the pixel 200 of Fig. 2, this can be used to provide unique and useful integration qualities to pixel 200, and can provide useful discrimination in color detection by pixel 200. The non-destructive read buffer 250 allows varying integration times without destroying or losing the collected charge on integration capacitor C_{int} 230.

[0037] In some embodiments the present pixels provide multi-color sensing, multi-integration sensors that enhance the overall response and usefulness of an associated sensing array or imaging product.

[0038] Fig. 3 illustrates a representative cross-sectional view of an exemplary response-enhanced pixel 300 similar to that described earlier with respect to Fig. 2.

[0039] Another feature of the present embodiments that facilitates its use in practical applications is that the present laser treated silicon is compatible with most standard CMOS readout circuit substrates, and can leverage known silicon MEMS and amorphous silicon MEMS technologies such as silicon MEMS cantilever technology.

[0040] The present invention should not be considered limited to the particular embodiments described above, but rather should be understood to cover all aspects of the invention as fairly set out in the attached claims. Various modifications, equivalent processes, as well as numerous structures to which the present invention may be applicable, will be readily apparent to those skilled in the art to which the present invention is directed upon review of the present disclosure. The claims are intended to cover such modifications.

[0041] We claim:

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VIII. CLAIMS

1. A light-sensing pixel for detecting at least a portion of the electromagnetic spectrum, comprising:

a first detector element having a laser-treated detector portion for detecting a first range of wavelengths of the electromagnetic spectrum;

a second detector element for detecting a second range of wavelengths of the electromagnetic spectrum;

a collection point for accumulating a first electrical output of said first detector element as well as a second electrical output of said second detector;

a bias point for applying a biasing voltage to said first detector element and capable of affecting the first electrical output of said first detector element; and

an output point for providing an electrical output of said light-sensing pixel.

2. The pixel of claim 1, said first detector element comprising a black silicon detector portion that is sensitive to electromagnetic wavelengths in an infra-red range of the electromagnetic spectrum.

3. The pixel of claim 2, said second detector element comprising a semiconducting photodetector element that is sensitive to electromagnetic wavelengths in a visible range of the electromagnetic spectrum.

4. The pixel of claim 1, further comprising readout circuitry including addressing switch points for addressing said pixel.

5. The pixel of claim 4, said readout circuitry constructed and arranged along with said first detector element in a monolithic semiconductor structure.

6. The pixel of claim 5, said second detector element constructed and arranged in a hybrid arrangement to be coupled to said monolithic semiconductor structure.

7. The pixel of claim 1, further comprising a post for coupling said second detector element to said readout circuitry and said collection point.

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8. The pixel of claim 1, said collection point comprising a capacitor which collects an electrical charge from said first and second detector elements.

9. The pixel of claim 1, said bias point constructed and arranged to receive a bias voltage and coupled to said first detector element to control the first electrical output of said first detector element.

10. The pixel of claim 9, said bias point providing a reverse bias voltage constructed and arranged to substantially shut off said first electrical output of said first detector element.

11. The pixel of claim 1, further comprising a reset switch coupled to said collection point.

12. The pixel of claim 1, said first and second electrical outputs comprising respective first and second electrical currents, and said bias point comprising a bias voltage terminal electrically coupled to said first and second detector elements and coupled to said collection point so as to control said first and second electrical currents.

13. A light-sensitive array comprising a plurality of pixels as claimed in claim 1, wherein said plurality of pixels each provides an electrical output that can be addressably sensed and contributes to a collective output of said array.

14. An imaging apparatus comprising an array of pixels as claimed in claim 13 such that an image corresponding to said collective output of said array or pixels can be captured or displayed.

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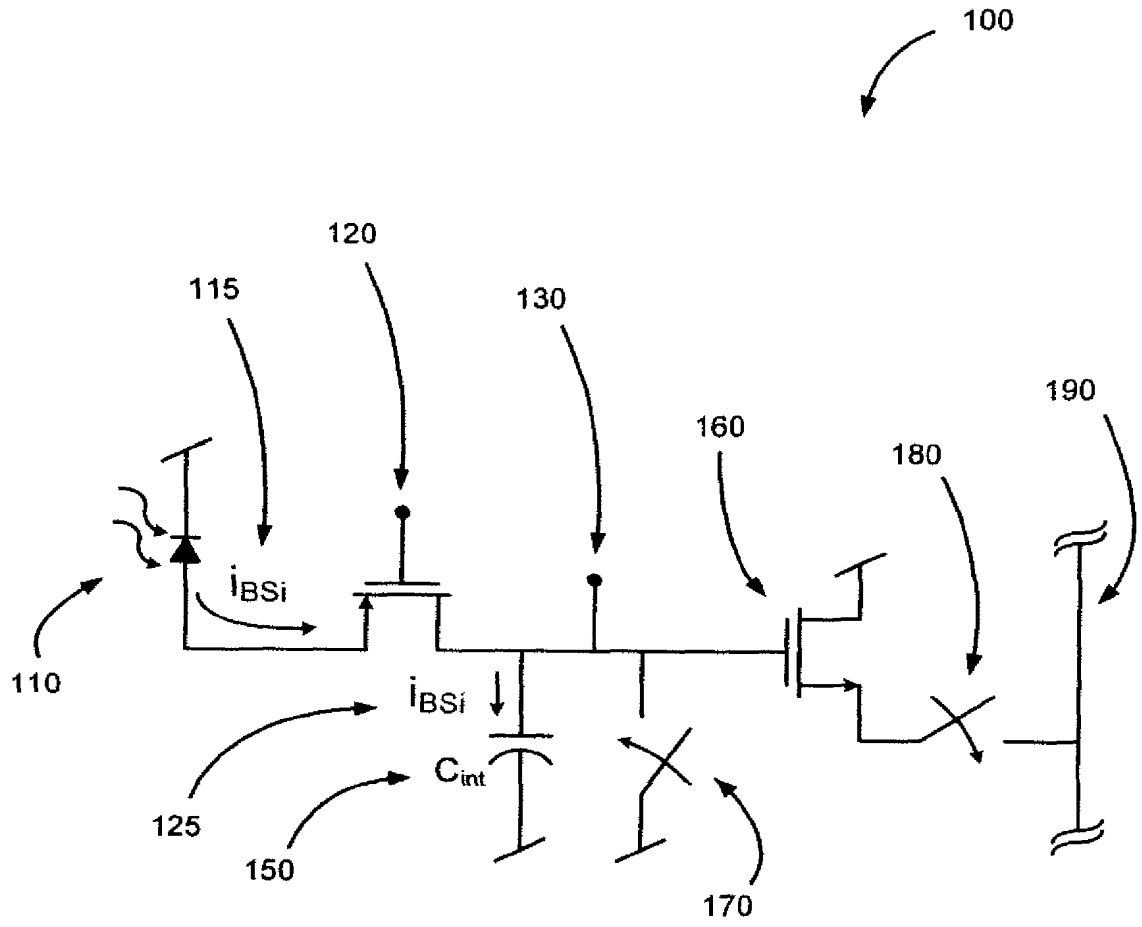

Fig. 1

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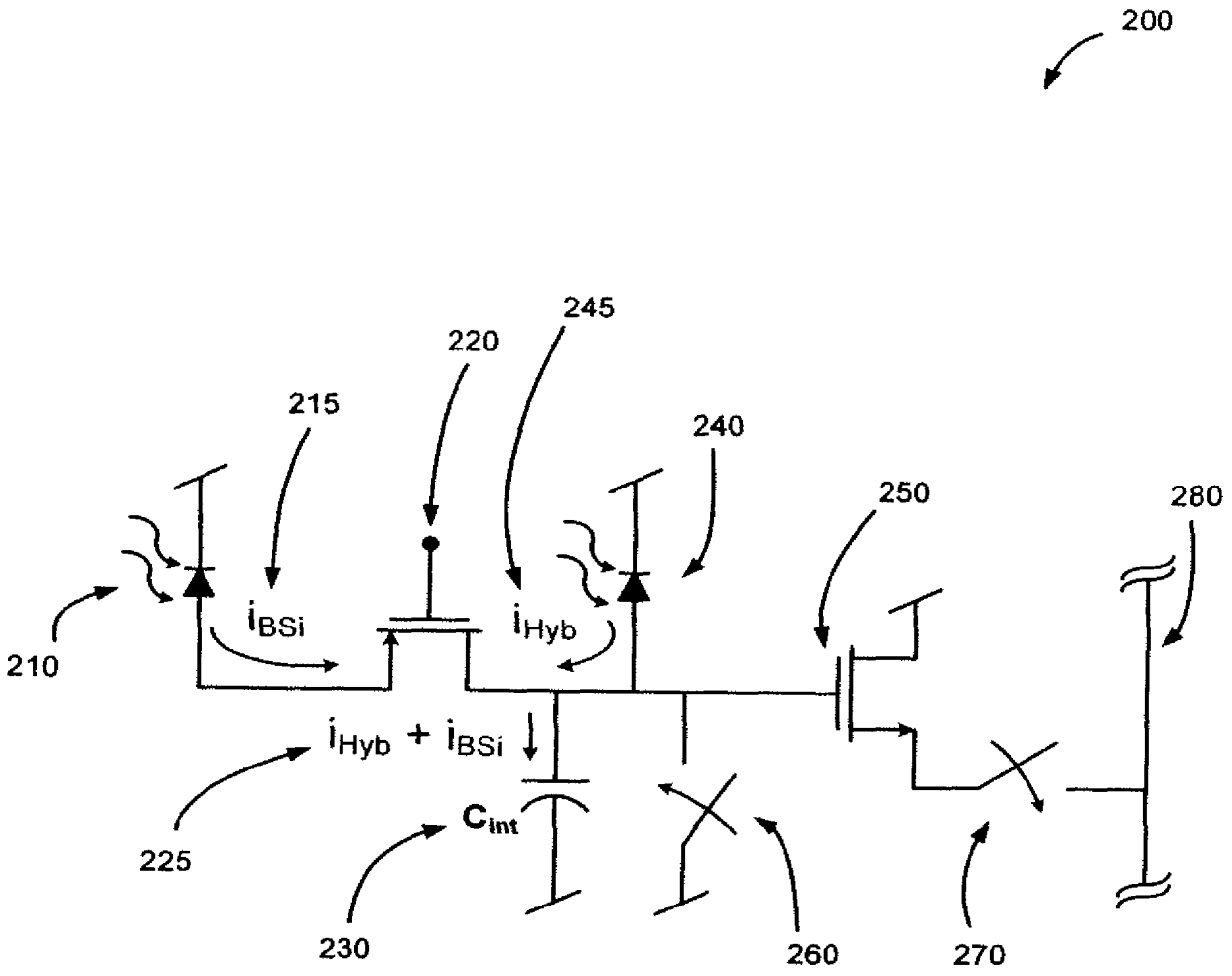

Fig. 2

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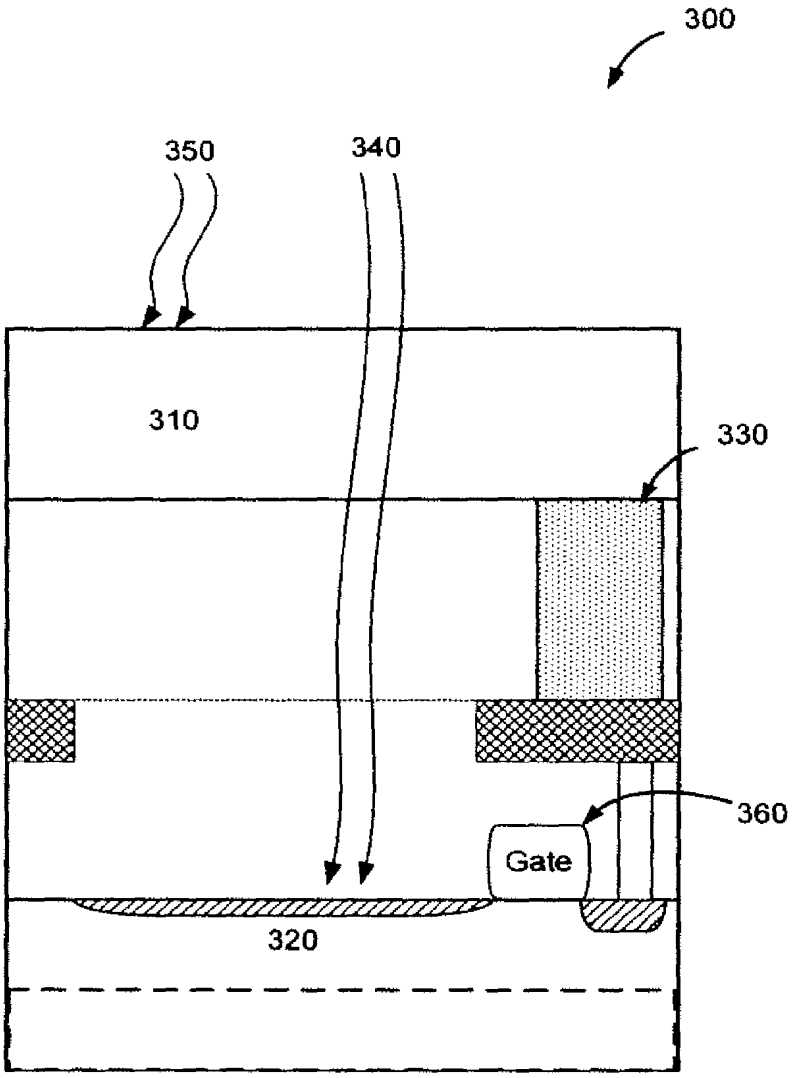

Fig. 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/077209

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/146

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 751 005 A (WYLES RICHARD H [US] ET AL) 12 May 1998 (1998-05-12) cited in the application column 3, lines 50-55; figures 1,2 column 5, lines 34-36 column 7, lines 9-15	1-5,7-14
Y	US 2003/029495 A1 (MAZUR ERIC [US] ET AL MAZUR ERIC [US] ET AL) 13 February 2003 (2003-02-13) cited in the application paragraphs [0030], [0031], [0036], [0042], [0043]; figure 1	1-5,7-14
Y	US 2007/051876 A1 (SUMI HIROFUMI [JP] ET AL) 8 March 2007 (2007-03-08)	1-5
A	figures 21,22	6-14

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 April 2009	16/04/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Fax: (+31–70) 340–3016	Zakharian, Andre

Form PCT/ISA/210 (second sheet) (April 2005)

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/077209

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 523 570 A (HAIRSTON ALLEN W [US]) 4 June 1996 (1996-06-04) column 2, lines 17-19; figure 1	6

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

SAMSUNG EX. 1002 - 1482/2862

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2008/077209

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5751005 A	12-05-1998	DE 69723808 D1	04-09-2003
		DE 69723808 T2	15-04-2004
		EP 0849802 A2	24-06-1998
		IL 122556 A	11-01-2001
		JP 3187760 B2	11-07-2001
		JP 10281869 A	23-10-1998
US 2003029495 A1	13-02-2003	US 2008258604 A1	23-10-2008
		US 2005127401 A1	16-06-2005
US 2007051876 A1	08-03-2007	JP 2006238093 A	07-09-2006
US 5523570 A	04-06-1996	NONE	

SAMSUNG EX. 1002 - 1483/2862

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
13 January 2011 (13.01.2011)

PCT

(10) International Publication Number
WO 2011/003871 A1

(51) International Patent Classification:
H01L 31/105 (2006.01) *G02B 6/42* (2006.01)
H01L 31/18 (2006.01) *G02F 1/01* (2006.01)
H01L 35/30 (2006.01) *G02F 1/025* (2006.01)
H01L 23/38 (2006.01)

(21) International Application Number:
PCT/EP2010/059571

(22) International Filing Date:
5 July 2010 (05.07.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/498,463 7 July 2009 (07.07.2009) US

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(74) Agent: **ROBERTS, Scott**; IBM United Kingdom Limited, Intellectual Property Law, Hursley Park, Winchester Hampshire SO21 2JN (GB).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: A TEMPERATURE CONTROL DEVICE FOR OPTOELECTRONIC DEVICES

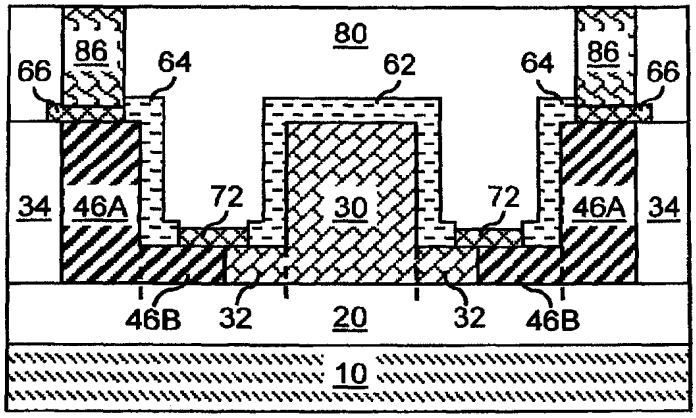

FIG. 9B

(57) Abstract: Current may be passed through an n-doped semiconductor region, a recessed metal semiconductor alloy portion, and a p-doped semiconductor region so that the diffusion of majority charge carriers in the doped semiconductor regions transfers heat from or into the semiconductor waveguide through Peltier-Seebeck effect. Further, a temperature control device may be configured to include a metal semiconductor alloy region located in proximity to an optoelectronic device, a first semiconductor region having a p-type doping, and a second semiconductor region having an n-type doping. The temperature of the optoelectronic device may thus be controlled to stabilize the performance of the optoelectronic device.

WO 2011/003871 A1

SAMSUNG EX. 1002 - 1484/2862

Published:

— *with international search report (Art. 21(3))*

A TEMPERATURE CONTROL DEVICE FOR OPTOELECTRONIC DEVICES

BACKGROUND

The present invention relates to a semiconductor structure, and particularly to a temperature control device for an optoelectronic device and a germanium photodetector for silicon waveguide, and methods of manufacturing the same, and methods of operating the same.

A semiconductor waveguide may be employed in microphotonic devices to enable high efficiency long range transmission of light over distances in the micrometer range or in the millimeter range. The semiconductor waveguide typically employs a single crystalline semiconductor material to minimize signal loss due to absorption of light. The semiconductor material in the semiconductor waveguide has a relative high refractive index. For example, silicon and germanium have a refractive index of about 3.45 and about 4.0, respectively. A dielectric material having a lower refractive constant surrounds the semiconductor waveguide so that a total reflection condition is satisfied at the interface between the semiconductor waveguide and the dielectric material for light impinging on the interface at a glancing angle. The semiconductor wave guide may thus be employed to transmit light having a wavelength greater than the wavelength corresponding to the band gap of the semiconductor material. Typically, infrared lights are employed in the semiconductor waveguide.

Many microphotonic devices manipulate the light in the semiconductor waveguide in some way. For example, the light in the semiconductor waveguide may be absorbed, reflected, or induced to change the phase. Many of the prior art methods that accomplish such optical manipulation employ exotic materials or special processing steps that are not typically employed in standard complementary metal-oxide-semiconductor (CMOS) processing steps, thereby increasing the manufacturing cost and processing complexity.

In view of the above, there exists a need to provide a structure that manipulates the light in a semiconductor waveguide with standard CMOS processing steps, and methods of manufacturing the same. Particularly, there exists a need to provide a structure that

modulates the phase of the light in the semiconductor waveguide with standard CMOS processing steps, and methods of manufacturing the same.

Further, performance of many optoelectronic devices is temperature sensitive. For example, performance of a semiconductor laser device is significantly affected by temperature variation. In a semiconductor chip integrating conventional semiconductor devices and optoelectronic devices, the performance of optoelectronic devices may be affected significantly due to the heat generated by conventional semiconductor devices and transferred to the optoelectronic devices. Thus, it is necessary to stabilize the temperature of the optoelectronic devices to provide stable operation of the optoelectronic devices within the semiconductor chip.

While placing optoelectronic devices at a location far away from the conventional semiconductor devices the thermal effect on the performance of the optoelectronic devices, such a design lowers the areal density of the conventional semiconductor devices or the optoelectronic devices. Thus, an integrated semiconductor chip including conventional semiconductor devices and optoelectronic devices at high density without adverse impact on the performance of the optoelectronic devices due to the thermal effects on the optoelectronic devices is desired.

BRIEF SUMMARY

The present invention provides a semiconductor waveguide having an integrated thermoelectric temperature control device to enable phase shifting of the light in the semiconductor waveguide and an optoelectronic device having an integrated thermoelectric temperature control device to control the temperature of the optoelectronic device.

In one embodiment of the present invention, a semiconductor waveguide is formed integrally with non-recessed semiconductor regions that are adjoined to the semiconductor waveguide through a recessed semiconductor portion having a lesser thickness than the semiconductor waveguide. One of the non-recessed semiconductor portions and an adjoining region of the recessed semiconductor portion are doped with p-type dopants to form a p-doped

semiconductor region, and another of the non-recessed semiconductor portions and an adjoining region of the recesses semiconductor portion are doped with n-type dopants to form an n-doped semiconductor region. After forming a dielectric spacer that covers sidewalls of the p-doped semiconductor region and the n-doped semiconductor region, the recessed semiconductor portion is metallized to form a recessed metal semiconductor alloy portion. Current is passed through the n-doped semiconductor region, the recessed metal semiconductor alloy portion, and the p-doped semiconductor region. The diffusion of majority charge carriers in the doped semiconductor regions transfers heat from or into the semiconductor waveguide through Peltier-Seebeck effect. The temperature change in the semiconductor waveguide alters refractive index of the semiconductor waveguide, which may be employed to modulate the phase of the light passing through the semiconductor waveguide.

According to an aspect of the present invention, a semiconductor structure is provided, which comprises: a semiconductor waveguide having a first thickness and located on a top surface of an insulator layer; a recessed semiconductor region of integral construction with the semiconductor waveguide, having a second thickness that is less than the first thickness, located on the insulator layer, and including a substantially undoped recessed semiconductor region; a p-doped semiconductor region laterally abutting the substantially undoped recessed semiconductor region; an n-doped semiconductor region laterally abutting the substantially undoped recessed semiconductor region and not abutting the p-doped semiconductor region; and a recessed metal semiconductor alloy portion abutting the recessed semiconductor region, the p-doped semiconductor region, and the n-doped semiconductor region.

According to another aspect of the present invention, a method of forming a semiconductor structure is provided, which comprises: forming shallow trench isolation structures laterally abutting a top semiconductor portion and vertically abutting a buried insulator layer in a top semiconductor layer of a semiconductor-on-insulator (SOI) substrate; forming a semiconductor waveguide by patterning the top semiconductor portion; forming a p-doped semiconductor region in the top semiconductor portion; forming an n-doped semiconductor region not abutting the p-doped semiconductor region in the top semiconductor region; and

forming a recessed metal semiconductor alloy portion directly on a recessed region of the top semiconductor portion, wherein the recessed metal semiconductor alloy portion is formed directly on the p-doped semiconductor region and the n-doped semiconductor region.

According to yet another aspect of the present invention, a method of operating a semiconductor device is provided, which comprises: providing a semiconductor structure including: a semiconductor waveguide located on a top surface of an insulator layer; a p-doped semiconductor region thermally connected to the silicon waveguide; an n-doped semiconductor region thermally connected to the silicon waveguide and not abutting the p-doped semiconductor region; and a recessed metal semiconductor alloy portion abutting the p-doped semiconductor region and the n-doped semiconductor region; and passing current through the n-doped semiconductor region, the recessed metal semiconductor alloy portion, and the p-doped semiconductor region.

In another embodiment of the present invention, an optoelectronic device is formed on a semiconductor substrate in proximity to a temperature control device. A semiconductor waveguide that is optically coupled to the optoelectronic device may be formed to enable transmission of optical signal through the semiconductor waveguide. The temperature control device is configured to include a metal semiconductor alloy region located in proximity to the optoelectronic device, a first semiconductor region having a p-type doping, and a second semiconductor region having an n-type doping. The metal semiconductor alloy region is thermally coupled with the optoelectronic device. Electrical current may be caused to flow through the first semiconductor region, the metal semiconductor alloy region, and the second semiconductor region to allow cooling of the metal semiconductor alloy region and the optoelectronic device through heat transfer. Conversely, the current may be caused to flow in the opposite direction to allow heating of the metal semiconductor alloy region and the optoelectronic device through heat transfer. The temperature of the optoelectronic device may thus be controlled to stabilize the performance of the optoelectronic device.

According to an aspect of the present invention, a semiconductor structure including a temperature control device and an optoelectronic device is provided. The temperature control device includes: a first metal semiconductor alloy region located on a substrate; a p-

doped semiconductor portion abutting the first metal semiconductor alloy region and located on the substrate; an n-doped semiconductor portion abutting the first metal semiconductor alloy region located on the substrate; wherein the temperature control device is configured to pass current from the p-doped semiconductor portion, through the first metal semiconductor alloy region, and to the n-doped semiconductor portion or from the n-doped semiconductor portion, through the first metal semiconductor alloy region, and to the p-doped semiconductor portion. The optoelectronic device includes a device that comprises a semiconductor material, configured to manipulate electromagnetic radiation, and is thermally coupled to the temperature control device.

According to another aspect of the present invention, a method of forming a semiconductor structure including a temperature control device and an optoelectronic device is provided. The method includes: patterning a top semiconductor layer of a semiconductor-on-insulator substrate to form a p-doped semiconductor portion and an n-doped semiconductor portion; forming a first metal semiconductor alloy region directly on the p-doped semiconductor portion and the n-doped semiconductor portion, wherein the p-doped semiconductor portion and an n-doped semiconductor portion and the first metal semiconductor alloy region constitute a portion of a temperature control device; forming a current conduction path configured to pass current from the p-doped semiconductor portion, through the first metal semiconductor alloy region, and to the n-doped semiconductor portion or from the n-doped semiconductor portion, through the first metal semiconductor alloy region, and to the p-doped semiconductor portion; and forming an optoelectronic device comprising a semiconductor material, configured to manipulate electromagnetic radiation, and is thermally coupled to the temperature control device.

According to yet another aspect of the present invention, a method of operating a semiconductor structure comprising a temperature control device and an optoelectronic device is provided. The method includes: providing a temperature control device including a first metal semiconductor alloy region located on a substrate, a p-doped semiconductor portion abutting the first metal semiconductor alloy region and located on the substrate, and an n-doped semiconductor portion abutting the first metal semiconductor alloy region located on the substrate; providing an optoelectronic device including a device that

comprises a semiconductor material, configured to manipulate electromagnetic radiation, and is thermally coupled to the temperature control device; and passing electrical current from the p-doped semiconductor portion, through the first metal semiconductor alloy region, and to the n-doped semiconductor portion or from the n-doped semiconductor portion, through the first metal semiconductor alloy region, and to the p-doped semiconductor portion, wherein heat is transferred in the direction of flow of majority charge carriers in the p-doped semiconductor portion and the n-doped semiconductor portion.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Embodiments of the present invention will now be described, by way of example only, with reference to the accompanying drawings in which:

FIGS. 1A – 1C are various views of a first exemplary semiconductor structure corresponding to the step after formation of a shallow trench isolation structures 34;

FIGS. 2A – 2C are various views of the first exemplary semiconductor structure corresponding to the step after formation of a pair of recessed line trenches 31;

FIGS. 3A – 3C are various views of the first exemplary semiconductor structure corresponding to the step after removal of a first photoresist (37A, 37B, 37C);

FIGS. 4A – 4C are various views of the first exemplary semiconductor structure corresponding to the step after formation of p-doped semiconductor regions (46A, 46B);

FIGS. 5A – 5C are various views of the first exemplary semiconductor structure corresponding to the step after formation of n-doped semiconductor regions (48A, 48B);

FIGS. 6A – 6C are various views of the first exemplary semiconductor structure corresponding to the step after removal of a third photoresist 47;

FIGS. 7A – 7C are various views of the first exemplary semiconductor structure corresponding to the step after formation of a dielectric material layer 60L;

FIGS. 8A – 8C are various views of the first exemplary semiconductor structure corresponding to the step after formation of a dielectric material portion 62 and dielectric spacers 64;

FIGS. 9A – 9C are various views of the first exemplary semiconductor structure corresponding to the step after formation of various metal semiconductor alloy portions, a middle-of-line (MOL) dielectric layer 80, and various conductive contact vias;

FIGS. 10, 11, and 12A, 12B, 13A, 13B, 14A, 14B, 15A, 15B, 16A, and 16B are various views of a second exemplary semiconductor structure corresponding to a second embodiment of the present invention. FIGS. 10 and 11 are vertical cross-sectional views. Each of FIG. 12A, 13A, 13A, 14A, 15A, and 16A is a vertical cross-sectional view along a vertical plane labeled Z – Z' in figures with the numeric label and the suffix "B." FIGS. 11B, 12B, 13B, and 14B are top-down views. FIG. 15B is a top-down view of selected elements to demonstrate lateral geometrical relationship between the selected elements;

FIG. 17 is a vertical cross-sectional view of a third exemplary semiconductor structure;

FIG. 18 is a vertical cross-sectional view of a fourth exemplary semiconductor structure;

FIG. 19 is a vertical cross-sectional view of a fifth exemplary semiconductor structure;

FIGS. 20 and 21 are sequential vertical cross-sectional views of a sixth exemplary semiconductor structure; and

FIG. 22 is a top-down view of selected elements to demonstrate lateral geometrical relationship between the selected elements of a seventh exemplary semiconductor structure according to a seventh embodiment of the present invention.

For all of the figures herein, the following conventions apply. Figures with the same numeric label correspond to the same stage of manufacturing for an exemplary semiconductor structure. Within FIGS. 1A – 9C, figures with the suffix "A" are top-down views, and figures with the suffix "B" or "C" are horizontal cross-sectional views along the plane B – B' or the plane C – C', respectively, in the figure with the same numeric label and the suffix "A."

DETAILED DESCRIPTION

As stated above, the present invention relates to a temperature control device for an optoelectronic device and a germanium photodetector for silicon waveguide, and methods of manufacturing the same, and methods of operating the same, which are now described in detail with accompanying figures. Throughout the drawings, the same reference numerals or letters are used to designate like or equivalent elements. Detailed descriptions of known functions and constructions unnecessarily obscuring the subject matter of the present invention have been omitted for clarity. The drawings are not necessarily drawn to scale.

Referring to FIGS. 1A – 1F, an exemplary semiconductor structure according to the present invention comprises a semiconductor substrate, which is a semiconductor-on-insulator (SOI) substrate. The semiconductor substrate includes an insulator layer 20 and a top semiconductor layer located above the insulator layer 20. The semiconductor substrate may further include a handle substrate 10, which is attached to the bottom surface of the insulator layer 20. The handle substrate 10 may comprise a semiconductor material, an insulator material, a conductive material, or a combination thereof. The insulator layer 20 and the handle substrate 10, if present, provide structural support to the top semiconductor layer which may comprise a contiguous semiconductor material layer that covers the entirety of the insulator layer 20.

The contiguous semiconductor material layer comprises a semiconductor material. Exemplary semiconductor materials that may be employed for the contiguous semiconductor material layer include, but are not limited to, silicon, germanium, silicon-germanium alloy, silicon carbon alloy, silicon-germanium-carbon alloy, gallium arsenide, indium arsenide, indium phosphide, III-V compound semiconductor materials, II-VI compound

semiconductor materials, organic semiconductor materials, and other compound semiconductor materials. Preferably, the entirety of the contiguous semiconductor material layer comprises a single crystalline semiconductor material having an epitaxial alignment among the semiconductor atoms. For example, the semiconductor material of the contiguous semiconductor material layer may comprise single crystalline silicon or single crystalline germanium. The thickness of the contiguous semiconductor material layer, which is herein referred to as a first thickness *t1*, may be from about 50 nm to about 1,000 nm, and typically from about 200 nm to about 500 nm, although lesser and greater thicknesses can also be employed.

Preferably, the contiguous semiconductor material layer comprises a substantially undoped semiconductor material so that the amount of impurities, including dopant atoms, in the contiguous semiconductor material layer is minimized. By minimizing the amount of impurities in the contiguous material layer, a semiconductor waveguide to be subsequently formed from a portion of the contiguous material layer provides low absorption rate of the signal. The atomic concentration of impurities, including dopants, in the contiguous semiconductor material layer is less than about $1.0 \times 10^{16}/cm^3$, and preferably less than about $1.0 \times 10^{15}/cm^3$, and more preferably less than about $1.0 \times 10^{14}/cm^3$. In case the contiguous semiconductor material layer comprises silicon, the resistivity of the material of the contiguous semiconductor material layer is greater than about 1 Ohm-cm, and preferably greater than about 10 Ohm-cm, and more preferably greater than about 100 Ohm-cm.

Trenches extending to the top surface of the insulator layer 20 are formed within the contiguous semiconductor material layer by a combination of lithographic means and an etch. Specifically, a photoresist (not shown) is applied over the top surface of the contiguous semiconductor material layer and lithographically patterned. The pattern in the photoresist is transferred into the contiguous semiconductor material layer by the etch, which is typically an anisotropic etch. After removal of the photoresist, the trenches are filled with a dielectric material such as a dielectric oxide, a dielectric nitride, a dielectric nitride, or a combination thereof. For example, silicon oxide and/or silicon nitride may be deposited into the trenches. The dielectric material above the top surface of the contiguous semiconductor material layer is removed, for example, by chemical mechanical planarization. The remaining portions of

the dielectric material filling the trenches constitute shallow trench isolation (STI) structures 34. Pad dielectric layers (not shown) may be employed to facilitate the planarization process.

The remaining portion of the contiguous semiconductor material layer constitutes a top semiconductor portion, which includes a primary top semiconductor portion 30P, first laterally protruding top semiconductor portions 30A, and second laterally protruding top semiconductor portions 30B. The primary top semiconductor portion 30P, the first laterally protruding top semiconductor portions 30A, and the second laterally protruding top semiconductor portions 30B comprise the same semiconductor material, have the same thickness, i.e., the first thickness *t1*, and are epitaxially aligned among one another. The sidewalls of the top semiconductor portion (30P, 30A, 30B) are laterally abutted by the shallow trench isolation structures 34. The first laterally protruding top semiconductor portions 30A and the second laterally protruding top semiconductor portions 30B laterally protrude out of the sidewalls of the primary top semiconductor portion 30P into the shallow trench isolation structures 34. Thus, each of the first laterally protruding top semiconductor portions 30A and the second laterally protruding top semiconductor portions 30B may comprise multiple sidewalls that laterally abut the shallow trench isolation structures 34. The shallow trench isolation structures 34 and the top semiconductor portion (30P, 30A, 30B) have substantially the same thickness, i.e., the first thickness *t1*.

At least one pair of a first laterally protruding top semiconductor portions 30A and a second laterally protruding top semiconductor portions 30B may be formed on one side of the primary top semiconductor portion 30P, and at least another pair of a first laterally protruding top semiconductor portions 30A and a second laterally protruding top semiconductor portions 30B may be formed on an opposite side of the primary top semiconductor portion 30P. The width of the semiconductor portion *SPW* may be from about 400 nm to about 3,000 nm, and preferably from about 600 nm to about 1,500 nm, although lesser and greater widths can also be employed. The length of the semiconductor portion *SPL* is the length of a semiconductor waveguide that is intended to be manufactured, and may be from about 10 μm to about 3 cm, and typically from about 30 μm to about 1 cm, although lesser and greater lengths can also be employed. Further, configurations for a

semiconductor waveguide having a curvature or a taper can also be employed, in which the shape of the top semiconductor portion (30P, 30A, 30B) are adjusted with a curvature, a taper, and/or other suitable geometric adjustments.

Referring to FIGS. 2A – 2C, a first photoresist is applied over the top surfaces of the top semiconductor portion (30P, 30A, 30B) and the shallow trench isolation structures 34 and lithographically patterned. The pattern in the first photoresist includes a pair of line troughs separated by a central photoresist portion 37A, which is a remaining portion of the first photoresist after lithographic patterning. The central photoresist portion 37A has a constant width, which is herein referred to as a waveguide width *ww*. The waveguide width *ww* may be from about 200 nm to about 1,500 nm, and preferably from about 300 nm to about 750 nm, although lesser and greater widths can also be employed. The remaining portions of the first photoresist include a first-side photoresist portion 37B and a second-side photoresist portion 37C, which are separated from the central photoresist portion 37A by the pair of line troughs. Each of the line troughs may have a substantially constant width, which is herein referred to as a line trough width *ltw*. The two line troughs may have the same line trough width *ltw*, or may have different line trough widths *ltw*. The sum of the two line trough widths *ltw* and the waveguide width *ww* may be less than, equal to, or greater than the width of the semiconductor portion *SPW*. While the present invention is described for the case in which the sum of the two line trough widths *ltw* and the waveguide width *ww* is less than the width of the semiconductor portion *SPW*, embodiments in which the sum of the two line trough widths *ltw* and the waveguide width *ww* is equal to, or greater than, the width of the semiconductor portion *SPW* are explicitly contemplated herein.

The pattern in the patterned portions of the first photoresist, i.e., the set of the central photoresist portion 37A, the first-side photoresist portion 37B, and the second-side photoresist portion 37C is transferred into the primary top semiconductor portion 30P, for example, by an anisotropic etch such as a reactive ion etch (RIE). The exposed portions of the primary top semiconductor portion 30P are vertically recessed by a recess depth *rd*, which is less than the first thickness *t1*. A pair of recessed line trenches 31 is formed directly underneath the two line troughs between the central photoresist portion 37A and each of the first-side and second-side photoresist portions (37B, 37C).

The recessed portions of the primary top semiconductor portion 30P are herein referred to as recessed semiconductor regions 30R. The recessed semiconductor regions have a second thickness *t2*, which is equal to the difference between the first thickness *t1* and the recess depth *rd*. The second thickness *t2* may be from about 10 nm to about 200 nm, and typically from about 30 nm to about 100 nm, although lesser and greater thicknesses can also be employed. The remaining sub-portion of the primary top semiconductor portion 30P underneath the central photoresist portion 37A is herein referred to a semiconductor waveguide 30. The semiconductor waveguide 30 has the first thickness *t1* and the waveguide width *ww*. The semiconductor waveguide 30 may be employed to transmit light along the direction of the length of the semiconductor portion *SPL* (See FIG. 1A). The sub-portions of the top semiconductor portion 30P directly underneath the pair of line trenches 31 are the recessed semiconductor regions 30R, which are of integral construction with the semiconductor waveguide 30.

The first-side photoresist portion 37B and the second-side photoresist portion 37C cover the upper surfaces of the first laterally protruding top semiconductor portions 30A and the second laterally protruding top semiconductor portions 30B. Thus, the first-side photoresist portion 37B and the second-side photoresist portion 37C are not recessed by the anisotropic etch, and have the first thickness *t1*. Each of the first laterally protruding top semiconductor portions 30A and the second laterally protruding top semiconductor portions 30B is a sup-portion of the top semiconductor portion (30P, 30A, 30b) having the first thickness *t1*. Sidewalls of the first laterally protruding top semiconductor portions 30A and the second laterally protruding top semiconductor portions 30B are exposed to the pair of recessed line trenches 31.

The semiconductor waveguide 30, the recessed semiconductor regions 30R, the first-side photoresist portions 37B, and the second-side photoresist portions 37C are of integral and unitary construction, i.e., in a single contiguous structure without any interface therebetween. In case the entirety of the top semiconductor portion (30P, 30A, 30B) is single crystalline prior to the formation of the semiconductor waveguide 30, the semiconductor waveguide 30, the recessed semiconductor regions 30R, the first-side photoresist portions 37B, and the second-side photoresist portions 37C are single crystalline

and epitaxially aligned among one another. In case the semiconductor substrate is an SOI substrate, the semiconductor waveguide 30, the semiconductor waveguide 30, the recessed semiconductor regions 30R, the first-side photoresist portion 37B, the second-side photoresist portion 37C, and the shallow trench isolation structures 34 are formed in a top semiconductor layer of the SOI substrate.

Referring to FIGS. 3A – 3C, the first photoresist is removed selective to the semiconductor material of the semiconductor waveguide 30, the recessed semiconductor regions 30R, the first-side photoresist portion 37B, the second-side photoresist portion 37C. Preferably, the removal of the first photoresist is selective to the dielectric material of the shallow trench isolation structures 34. While the present invention is described for the case in which edges of the recessed line trenches 31 is coincident with the sidewalls of the shallow trench isolation structures 34 that laterally abut the primary top semiconductor portion 30P (See FIG. 1A), embodiments in which the edges of the recessed line trenches 31 is offset from the sidewalls of the shallow trench isolation structures 34 inward or outward are explicitly contemplated herein.

Referring to FIGS. 4A – 4C, a second photoresist 45 is applied over the first exemplary semiconductor structure and lithographically patterned to form openings. The first laterally protruding top semiconductor portions 30A are exposed within the openings. Further, portions of the recessed semiconductor regions 30R that adjoin the first laterally protruding top semiconductor portions 30A are also exposed within the opening in the second photoresist 45. The second photoresist 45 covers the entirety of the semiconductor waveguide 30 and the second laterally protruding top semiconductor portions 30B. Further, the second photoresist 45 covers portions of the recessed semiconductor regions 30R that laterally abut the semiconductor waveguide 30.

P-type dopants are implanted into the first laterally protruding top semiconductor portions 30A and the exposed portions of the recessed semiconductor regions 30R. P-type dopants may be boron, gallium, indium, or a combination thereof. Preferably, the dose and the energy of the p-type dopants are selected to provide a heavy doping in the implanted regions. For example, the atomic concentration of p-type dopants in the implanted regions may be

from about 1.0 x 10^{19}/cm^3 to about 1.0 x 10^{21}/cm^3, and typically from about 5.0 x 10^{19}/cm^3 to about 5.0 x 10^{20}/cm^3, although lesser and greater dopant concentrations can also be employed.

The first laterally protruding top semiconductor portions 30A as implanted with the p-type dopants are herein referred to as p-doped non-recessed semiconductor regions 46A, which has a third thickness *t3*. Typically, the third thickness *t3* is the same as the first thickness *t1*. The portions of the recessed semiconductor regions 30R that are implanted with the p-type dopants are herein referred to as p-doped recessed semiconductor regions 46B. A contiguous pair of a p-doped non-recessed semiconductor region 46A and a p-doped recessed semiconductor region 46B collectively constitutes a p-doped semiconductor region (46A, 46B). The portions of the recessed semiconductor regions 30R that are not implanted with the p-type dopants are herein referred to as substantially undoped recessed semiconductor regions 32, which has the same composition as the semiconductor waveguide 30, i.e., has a total concentration of impurities, including dopants, less than about 1.0 x 10^{16}/cm^3.

Within each p-doped semiconductor region (46A, 46B), a p-doped non-recessed semiconductor region 46A laterally abuts a p-doped recessed semiconductor region 46B. Further, each p-doped recessed semiconductor region 46B laterally abuts a substantially undoped recessed semiconductor region 32. The second photoresist 45 is subsequently removed.

Referring to FIGS. 5A – 5C, a third photoresist 47 is applied over the first exemplary semiconductor structure and lithographically patterned to form openings. The second laterally protruding top semiconductor portions 30B are exposed within the openings. Further, portions of the substantially undoped recessed semiconductor regions 32 that adjoin the second laterally protruding top semiconductor portions 30B are also exposed within the opening in the third photoresist 47. The third photoresist 47 covers the entirety of the semiconductor waveguide 30 and the p-doped semiconductor region (46A, 46B). Further, the third photoresist 47 covers portions of the substantially undoped recessed semiconductor regions 32 that laterally abut the semiconductor waveguide 30.

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N-type dopants are implanted into the second laterally protruding top semiconductor portions 30B and the exposed portions of the substantially undoped recessed semiconductor regions 32. N-type dopants may be phosphorus, arsenic, antimony, or a combination thereof. Preferably, the dose and the energy of the n-type dopants are selected to provide a heavy doping in the implanted regions. For example, the atomic concentration of n-type dopants in the implanted regions may be from about $1.0 \times 10^{19}/cm^3$ to about $1.0 \times 10^{21}/cm^3$, and typically from about $5.0 \times 10^{19}/cm^3$ to about $5.0 \times 10^{20}/cm^3$, although lesser and greater dopant concentrations can also be employed.

The second laterally protruding top semiconductor portions 30B as implanted with the n-type dopants are herein referred to as n-doped non-recessed semiconductor regions 48A, which has the third thickness *t3*. The portions of the substantially undoped recessed semiconductor regions 32 that are implanted with the n-type dopants are herein referred to as n-doped recessed semiconductor regions 48B. A contiguous pair of an n-doped non-recessed semiconductor region 48A and an n-doped recessed semiconductor region 48B collectively constitutes an n-doped semiconductor region (48A, 48B). The substantially undoped recessed semiconductor regions 32 is reduced as portions of the substantially undoped recessed semiconductor regions 32 are converted into the n-doped recessed semiconductor regions 48B.

Within each n-doped semiconductor region (48A, 48B), an n-doped non-recessed semiconductor region 48A laterally abuts an n-doped recessed semiconductor region 48B. Further, each n-doped recessed semiconductor region 48B laterally abuts a substantially undoped recessed semiconductor region 32. The third photoresist 47 is subsequently removed.

Referring to FIGS. 6A – 6C, the first exemplary semiconductor structure after removal of the third photoresist 47 is shown. The substantially undoped recessed semiconductor regions 32, the p-doped recessed semiconductor regions 46B, and the n-doped recessed semiconductor regions 48B collectively constitute the recessed semiconductor regions (32, 46B, 48B). The recessed semiconductor regions (32, 46B, 48B) underlie the pair of recessed line trenches 31. The p-doped non-recessed semiconductor regions 48A, the n-doped non-

recessed semiconductor regions 48A, and the semiconductor waveguide 30 are not recessed. Each of the p-doped non-recessed semiconductor regions 48A and the n-doped non-recessed semiconductor regions 48A has a sidewall that is exposed to one of the recessed line trenches 31. The semiconductor waveguide 30 has two substantially parallel and substantially vertical sidewalls separated by the waveguide width *ww*. Each sidewall of the semiconductor waveguide 30 is exposed to one of the two recessed line trenches 31.

Referring to FIGS. 7A – 7C, a dielectric layer 60L is formed directly on the exposed surfaces of the first exemplary semiconductor structure including the top surface and the sidewall surfaces of the semiconductor waveguide 30, the top surfaces of the recessed semiconductor regions (32, 46B, 48B), the top surfaces and the sidewalls of the p-doped non-recessed semiconductor region 46A and the n-doped non-recessed semiconductor region 48A, and the top surfaces of the shallow trench isolation structures 34. The dielectric layer 60L comprises a dielectric material such as a dielectric oxide, a dielectric nitride, a dielectric oxynitride, or a combination thereof. For example, the dielectric layer 60L may comprise silicon nitride or silicon oxide. The dielectric material for the dielectric layer 60L has a lower refractive index than the semiconductor material of the semiconductor waveguide 30.

The dielectric layer 60L may be conformal or non-conformal. The thickness of the dielectric layer 60L, as measured on the top surface of the semiconductor waveguide 30, may be from about 4 nm to about 100 nm, and typically from about 10 nm to about 50 nm, although lesser and greater thicknesses can also be employed. The dielectric layer 60L may be formed by low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), rapid thermal chemical vapor deposition (RTCVD), atomic layer deposition (ALD), etc.

Referring to FIGS. 8A – 8C, the dielectric layer 60L is lithographically patterned into at least three portions. The lithographic patterning may be effected by applying a photoresist (not shown) to the top surface of the dielectric layer 60L and lithographically patterning the photoresist, followed by a pattern transfer into the dielectric layer by an etch. The etch may be an anisotropic etch or an isotropic etch.

Remaining portions of the dielectric layer 60L after the lithographic patterning include a dielectric material portion 62 which covers the entirety of the top surface and sidewalls of the semiconductor waveguide 30. The remaining portions of the dielectric layer 60L further includes dielectric spacers 64, each of which is located directly on at least one of a sidewall of a p-doped non-recessed semiconductor region 46A and a sidewall of an n-doped non-recessed semiconductor region 48A. In one embodiment, a dielectric spacer 64 may be formed contiguously and directly on a sidewall of a p-doped non-recessed semiconductor region 46A, a sidewall of an n-doped non-recessed semiconductor region 48A, and a sidewall of one of the shallow trench isolation structures 34 that is located between the p-doped non-recessed semiconductor region 46A and the sidewall of an n-doped non-recessed semiconductor region 48A. Horizontal surfaces of the p-doped non-recessed semiconductor regions 46A, the n-doped non-recessed semiconductor regions 48A, the p-doped recessed semiconductor regions 46B, and the n-doped recessed semiconductor regions 48B are exposed. All sidewalls of the p-doped non-recessed semiconductor regions 46A and the n-doped non-recessed semiconductor regions 48A are covered by the dielectric spacers 64.

On each side of the semiconductor waveguide 30, a contiguous set of exposed semiconductor surfaces is formed, which includes a top surface of a p-doped recessed semiconductor regions 46B, a top surface of an n-doped recessed semiconductor regions 48B, and a top surface of a portion of a substantially undoped recessed semiconductor regions 32 located therebetween.

Referring to FIGS. 9A – 9C, various metal semiconductor alloy portions are formed on the exposed semiconductor surfaces of the first exemplary semiconductor structure. Specifically, recessed metal semiconductor alloy portions 72 are formed directly on the exposed surfaces of the recessed semiconductor regions (32, 46B, 48B). First metal semiconductor alloy portions 66 are formed directly on the top surfaces of the p-doped non-recessed semiconductor regions 46A. Second metal semiconductor alloy portions 68 are formed directly on the top surfaces of the n-doped non-recessed semiconductor regions 46B.

The various metal semiconductor alloy portions (72, 66, 68) may be formed by methods known in the art such as deposition of a blanket metal layer, anneal at an elevated

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temperature to induce formation of metal semiconductor alloy materials, and removal of unreacted portions of the blanket metal layer. In case the semiconductor material of the recessed semiconductor regions (32, 46B, 48B) and the doped non-recessed semiconductor regions (46A, 48A) comprise silicon, the various metal semiconductor alloy portions (72, 66, 68) comprise a metal silicide. In case the semiconductor material of the recessed semiconductor regions (32, 46B, 48B) and the doped non-recessed semiconductor regions (46A, 48A) comprise germanium, the various metal semiconductor alloy portions (72, 66, 68) comprise a metal germanide. The recessed metal semiconductor alloy portions 72, the first metal semiconductor alloy portions 66, and the second metal semiconductor alloy portions 68 comprise the same metal semiconductor alloy material.

A middle-of-line (MOL) dielectric material layer 80 is formed on the first exemplary semiconductor structure. The pair of line troughs 31 is filled with the MOL dielectric layer 80. The dielectric materials that may be used for the MOL dielectric layer 80 include, but are not limited to, a silicate glass, an organosilicate glass (OSG) material, a SiCOH-based low-k material formed by chemical vapor deposition, a spin-on glass (SOG), or a spin-on low-k dielectric material such as SiLK™, etc. The silicate glass includes an undoped silicate glass (USG), borosilicate glass (BSG), phosphosilicate glass (PSG), fluorosilicate glass (FSG), borophosphosilicate glass (BPSG), etc. The dielectric material may be a low dielectric constant (low-k) material having a dielectric constant less than 3.0. The dielectric material may non-porous or porous.

A conductive contact via is formed directly on each of the first metal semiconductor alloy portions 66 and the second metal semiconductor alloy portions 68. Specifically, a first conductive contact via 86 is formed directly on each of the first metal semiconductor alloy portion 66, and a second conductive contact via 88 is formed directly on each of the second metal semiconductor alloy portion 68. The first and second metal semiconductor alloy portions (66, 68) comprise a conductive material such as doped polysilicon, a doped silicon-containing semiconductor material, W, Cu, Al, TaN, TiN, Ta, Ti, or a combination thereof.

Heat may be transferred between the semiconductor waveguide 30 and the set of the first metal semiconductor alloy portions 66 and the second metal semiconductor alloy portions 68

by passing current. Specifically, a voltage bias may be applied across a resistively connected pair of a first conducive contact via 86 and a second conductive contact via 88.

In one embodiment, the second conductive contact via 88 is held at a positive voltage relative to the first conductive contact via 86. In this case, electrical current flows from the second conductive contact via 88, then through a second metal semiconductor alloy portion 68, then through an n-doped non-recessed semiconductor region 48A, then through an n-doped recessed semiconductor region 48B, then through a recessed metal semiconductor alloy portion 72, then through a p-doped recessed semiconductor region 46B, then through a p-doped non-recessed semiconductor region 46A, then through a first metal semiconductor alloy portion 66, and into the first conductive contact via 86. In metallic materials or metal semiconductor alloy portions in the current path, electrons move in the opposite direction of the current flow to conduct electricity.

In semiconductor material portions, majority charge carriers provide electrical conduction. Specifically, holes having positive charges travel in the p-doped recessed semiconductor region 46B and the p-doped non-recessed semiconductor region 46A along the direction from the recessed metal semiconductor alloy portion 72 toward the first metal semiconductor alloy portion 66. Electrons having negative charges travel in the n-doped recessed semiconductor region 48B and the n-doped non-recessed semiconductor region 48A along the direction from the recessed metal semiconductor alloy portion 72 toward the second metal semiconductor alloy portion 68. Thus, the majority charge carriers travel away from the recessed metal semiconductor alloy portion 72 in the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B).

The mechanism of Peltier-Seebeck effect is in operation in the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B). According to Peltier-Seebeck effect, heat transfer accompanies diffusion of charge carriers in a semiconductor material and vice versa. In this case, the majority charge carriers diffuse away from the interface with the recessed metal semiconductor alloy portion 72 toward the interface with the first or second metal semiconductor alloy portion (66 or 68) in each of the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B).

Therefore, there is a net heat transfer from the recessed metal semiconductor alloy portion 72 to the first and second metal semiconductor alloy portions (66, 68). The heat that is transferred to the first and second metal semiconductor alloy portions (66, 68) may further be transferred to a heat sink through the first and second conductive contact vias (86, 88) and other metal interconnect structures (not shown) attached thereto.

Since the semiconductor waveguide 30, the recessed semiconductor regions (32, 46B, 48B), the p-doped semiconductor region (46A, 46B), and the n-doped semiconductor region (48A, 48B) are of integral construction without any interface therebetween, the entirety of the semiconductor waveguide 30, the recessed semiconductor regions (32, 46B, 48B), the p-doped semiconductor region (46A, 46B), and the n-doped semiconductor region (48A, 48B) is thermally connected among one another. Continual transfer of heat from the recessed metal semiconductor alloy portions 72, through the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B), and into the first and second metal semiconductor alloy portions (66, 68) cools the semiconductor waveguide 30.

Cooling of the semiconductor waveguide 30 affects the refractive index of the semiconductor material of the semiconductor waveguide. For example, single crystalline silicon has a wavelength-dependent refractive index, which is from about 3.42 to about 3. 56 between the wavelength range from about 1 micron to about 6 microns. The temperature dependency of the refractive index of silicon is about 1.6×10^{-4} per degree Celsius. Germanium has similar temperature dependency as silicon.

Temperature change in the semiconductor waveguide 30 may be advantageously employed to change the phase of light passing through the semiconductor waveguide. For example, light having a wavelength of about 3.42 micron in vacuum has a wavelength of about 1.00 micron in a semiconductor waveguide 30 that consists essentially of silicon. 1 degree change in the temperature of the semiconductor waveguide 30 induces a phase change of about $2\pi \times 1.6 \times 10^{-4}$ radian per 1 micron. The light changes phase by π radian after traveling about 3.125 mm. By employing a beam splitter connected to two semiconductor waveguides 30 and modulating the phase of the light in one of the semiconductor waveguides 30, constructive interference or destructive interference may be induced between

the two beams as the phase of one beam is modulated through cooling. Thus, by modulating the refractive index of a semiconductor waveguide 30 through the temperature change in the semiconductor waveguide 30 caused by heat transfer out of the semiconductor waveguide 30, the phase of the light passing through the semiconductor waveguide 30 may be modulated.

In another embodiment, the second conductive contact via 88 is held at a negative voltage relative to the first conductive contact via 86. In this case, electrical current flows from the first conductive contact via 86, then through a first metal semiconductor alloy portion 66, then through a p-doped non-recessed semiconductor region 46A, then through a p-doped recessed semiconductor region 46B, then through a recessed metal semiconductor alloy portion 72, then through an n-doped recessed semiconductor region 48B, then through an n-doped non-recessed semiconductor region 48A, then through a second metal semiconductor alloy portion 68, and into the second conductive contact via 88. In other words, the electrical current flows in the opposite direction of the current flow in the previous embodiment.

In this case, holes in the p-doped semiconductor region (46A, 46B) along the direction from the first metal semiconductor alloy portion 66 to the recessed metal semiconductor alloy portion 72. Electrons travel in the n-doped semiconductor region (48A, 48B) along the direction from the second metal semiconductor alloy portion 68 toward the recessed metal semiconductor alloy portion 72. Thus, the majority charge carriers travel toward the recessed metal semiconductor alloy portion 72 in the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B).

The mechanism of Peltier-Seebeck effect is also in operation in the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B). However, the majority charge carriers diffuse away from the interface with the first or second metal semiconductor alloy portion (66 or 68) toward the interface with the recessed metal semiconductor alloy portion 72 in each of the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B). Therefore, there is a net heat transfer from

the first and second metal semiconductor alloy portions (66, 68) to the recessed metal semiconductor alloy portion 72.

Since the entirety of the semiconductor waveguide 30, the recessed semiconductor regions (32, 46B, 48B), the p-doped semiconductor region (46A, 46B), and the n-doped semiconductor region (48A, 48B) is thermally connected among one another, heat transferred into the recessed metal semiconductor alloy portion 72 is transferred into the semiconductor waveguide 30. Thus, the semiconductor waveguide is heated as the current flows through the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B). The mechanism for the heat accumulation in the semiconductor waveguide 30 is not Joule heating, but a heat transfer through Peltier-Seebeck effect.

Heating of the semiconductor waveguide 30 affects the refractive index of the semiconductor material of the semiconductor waveguide in the same manner as the cooling of the semiconductor waveguide 30 except for the reversal of the polarity of the change in the refractive index. In a similar manner as in the previous embodiment, temperature change in the semiconductor waveguide 30 may be advantageously employed to change the phase of light passing through the semiconductor waveguide. By modulating the refractive index of a semiconductor waveguide 30 through the temperature change in the semiconductor waveguide 30 caused by heat transfer into the semiconductor waveguide 30, the phase of the light passing through the semiconductor waveguide 30 may be modulated.

Referring to FIG. 10, a second exemplary semiconductor structure according to a second embodiment of the present invention comprises a semiconductor substrate 108, which is a semiconductor-on-insulator (SOI) substrate. The SOI substrate includes a handle substrate 10, an insulator layer 20 abutting a top surface of the handle substrate 10, and a top semiconductor layer 129 located above the insulator layer 20. The insulator layer 20 and the handle substrate 10 provide structural support to the top semiconductor layer 129 which may comprise a contiguous semiconductor material layer that covers the entirety of the insulator layer 20. The top semiconductor layer 129 comprises a semiconductor material, which may be any of the material that may be employed for the contiguous semiconductor material layer of the first embodiment.

Preferably, the top semiconductor layer 129 comprises a substantially undoped semiconductor material so that the amount of impurities, including dopant atoms, in the top semiconductor layer 129 is minimized. By minimizing the amount of impurities in the contiguous material layer, a semiconductor waveguide having a low absorption rate of the signal may be subsequently formed from a portion of the top semiconductor layer. The atomic concentration of impurities, including dopants, in the top semiconductor layer 129 is less than about $1.0 \times 10^{16}/cm^3$, and preferably less than about $1.0 \times 10^{15}/cm^3$, and more preferably less than about $1.0 \times 10^{14}/cm^3$. In case the top semiconductor layer 129 comprises silicon, the resistivity of the material of the top semiconductor layer 129 is greater than about 1 Ohm-cm, and preferably greater than about 10 Ohm-cm, and more preferably greater than about 100 Ohm-cm.

The buried insulator layer 20 comprises a dielectric material such as a dielectric oxide, a dielectric nitride, or a dielectric oxynitride. For example, the buried insulator layer 20 may comprise silicon oxide. The buried insulator layer 20 may comprise a dielectric material having a dielectric constant greater than 3.0.

The handle substrate 10 may comprise a semiconductor material, an insulator material, a conductive material, or a combination thereof. In case the handle substrate 10 comprises a semiconductor material, the material for the handle substrate 10 may comprise any of the semiconductor material that may be employed for the top semiconductor layer 129 as described above.

Referring to FIG. 11, a hard mask layer 125 may be deposited on a top surface of the top semiconductor layer 129 and lithographically patterned to mask a portion of the top semiconductor layer 129, while exposing other portions of the top semiconductor layer 129. The hard mask layer 125 comprises a dielectric material such as silicon oxide, silicon nitride, or silicon oxynitride. The exposed portions of the top semiconductor layer 129 are recessed. An epitaxial semiconductor layer 127 may be deposited on the recessed surface of the top semiconductor layer 129. The epitaxial semiconductor layer may comprise a different semiconductor material than the top semiconductor layer 129. The material of the epitaxial

semiconductor layer 127 is single crystalline, and is epitaxially aligned to semiconductor material of the top semiconductor layer 127. For example, the top semiconductor layer 129 may comprise single crystalline silicon, and the epitaxial semiconductor layer 127 may comprise a silicon germanium alloy.

The hard mask layer 125 is subsequently removed. The top surface of the top semiconductor portions of the top semiconductor layer 129 may be planarized, for example, by chemical mechanical planarization.

Referring to FIGS. 12A and 12B, portions of the top semiconductor layer 129 are appropriately doped and patterned to form at least one p-doped semiconductor portion (131, 132) and at least one n-doped semiconductor portion (133, 134). Each of the at least one p-doped semiconductor region (131, 132) may comprise a lower p-doped semiconductor region 131 and an upper p-doped semiconductor region 132. Each of the at least one n-doped semiconductor region (133, 134) may comprise a lower n-doped semiconductor region 133 and an upper n-doped semiconductor region 134. In addition, a semiconductor waveguide 136 may be formed by a patterning another portion of the top semiconductor layer 129 without implanting additional dopant atoms. In this case, the semiconductor waveguide may comprise a substantially intrinsic semiconductor material having the same composition as the at least one p-doped semiconductor portion (131, 132) and the at least one n-doped semiconductor portion (133, 134) except for dopant species and dopant concentration. The substantially intrinsic semiconductor material may have a resistivity greater than 1 Ohm-cm as the material of the top semiconductor layer 129 described above. In one case, the semiconductor waveguide 136 may consist essentially of silicon, and the at least one lower p-doped semiconductor region 131 may consist essentially of p-doped silicon, and the at least one n-doped semiconductor region 133 may consist essentially of n-doped silicon.

The at least one upper p-doped semiconductor portion 132 may be formed by implanting p-type dopants into at least one portion of the epitaxial semiconductor layer 127 through at least one opening in a first implantation mask layer (not shown), which may be a first patterned photoresist layer. The at least one lower p-doped semiconductor portion 131 may

be formed by implanting p-type dopants into at least one portion of the top semiconductor layer 129 through the at least one opening in the first implantation mask layer. The at least one upper n-doped semiconductor portion 134 may be formed by implanting n-type dopants into at least one portion of the epitaxial semiconductor layer 127 through at least one opening in a second implantation mask layer (not shown), which may be a second patterned photoresist layer. The at least one lower n-doped semiconductor portion 133 may be formed by implanting n-type dopants into at least one portion of the top semiconductor layer 129 through the at least one opening in the second implantation mask layer.

After implantation of the p-type dopants and the n-type dopants, the top semiconductor layer 129 is lithographically patterned. The remaining portions of the epitaxial semiconductor layer 127 and the top semiconductor layer 129 after lithographic patterning include the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and optionally, the semiconductor waveguide 136. Thus, the heights of the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and the semiconductor waveguide 136 are substantially the same at this step.

Each of the at least one p-doped semiconductor portion (131, 132) may laterally abut the at least one n-doped semiconductor portion (133, 134). Alternately, a substantially undoped semiconductor material portion (not shown) having the same composition as the semiconductor waveguide 136 may be formed between one of the at least one p-doped semiconductor portion (131, 132) and the at least one n-doped semiconductor portion (133, 134).

Referring to FIGS. 13A and 13B, metal semiconductor alloy regions are formed on the sub-portions of the at least one upper p-doped semiconductor portion 132 and the at least one upper n-doped semiconductor portion 134. Specifically, a first metal semiconductor alloy region 140 is formed on each laterally abutting pair of a first sub-portion of the at least one p-doped semiconductor portion (131, 132) and a first sub-portion of the at least one n-doped semiconductor portion (133, 134). Each first metal semiconductor alloy region 140 is contiguous.

A second metal semiconductor alloy region 142 is formed on a second sub-portion of each of the at least one upper p-doped semiconductor portion 132. The second sub-portion of each of the at least one upper p-doped semiconductor portion 132 is located on an opposite end of the first sub-portion of that p-doped semiconductor portion 134. In each of the at least one p-doped semiconductor portion (131, 132), a middle sub-portion of the p-doped semiconductor portion (131, 132) that does not underlie a metal semiconductor alloy region separates, and laterally abuts, a first sub-portion of the p-doped semiconductor portion (131, 132) and a second sub-portion of the p-doped semiconductor portion (131, 132). Each of the at least one p-doped semiconductor portion (131, 132) includes a first sub-portion located directly underneath a portion of a first metal semiconductor alloy region 140, a second sub-portion located directly underneath a second metal semiconductor alloy region 142, and a middle sub-portion that laterally separates the first sub-portion and the second sub-portion of that p-doped semiconductor portion (131, 132).

A third metal semiconductor alloy region 144 is formed on a second sub-portion of each of the at least one upper n-doped semiconductor portion 134. The second sub-portion of each of the at least one upper n-doped semiconductor portion 134 is located on an opposite end of the first sub-portion of that n-doped semiconductor portion (133, 134). In each of the at least one n-doped semiconductor portion (133, 134), a middle sub-portion of the n-doped semiconductor portion (133, 134) that does not underlie a metal semiconductor alloy region separates, and laterally abuts, a first sub-portion of the n-doped semiconductor portion (133, 134) and a second sub-portion of the n-doped semiconductor portion (133, 134). Each of the at least one n-doped semiconductor portion (133, 134) includes a first sub-portion located directly underneath a portion of a first metal semiconductor alloy region 140, a second sub-portion located directly underneath a third metal semiconductor alloy region 144, and a middle sub-portion that laterally separates the first sub-portion and the second sub-portion of that p-doped semiconductor portion (131, 132).

The metal semiconductor alloy regions (140, 142, 144) may be formed by depositing an insulator layer (not shown), patterning openings in the insulator layer in areas in which the metal semiconductor alloy regions (140, 142, 144) are to be formed, depositing a metal

layer, reacting the material of the metal layer with the underlying semiconductor material, and removing unreacted portions of the metal layer. The insulator layer may, or may not, be subsequently removed. The metal layer comprises a metal that reacts with the underlying semiconductor material of the at least one p-doped semiconductor portion (131, 132) and the at least one n-doped semiconductor portion (133, 134). Non-limiting examples of the metal that may be employed as the material of the metal layer include Co, Ta, Ti, W, Ni, Pt, Os, and Ir. In case the underlying semiconductor material comprises silicon, the metal semiconductor alloy regions (140, 142, 144) may comprise a metal silicide. The thickness of the metal semiconductor alloy regions (140, 142, 144) may be from 10 nm to 100 nm, although lesser and greater thicknesses can also be employed.

Referring to FIGS. 14A and 14B, a photoresist 147 is applied over the top surface of the second exemplary semiconductor structure. An opening is formed in the photoresist 147 by lithographic patterning. The at least one first metal semiconductor alloy region 140 is exposed within the opening in the photoresist 147. A portion of the semiconductor waveguide 136 may be exposed within the opening in the photoresist 147. Not necessarily but preferably, edges of the photoresist 147 may overlie the middle sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) and the middle sub-portion(s) of the at least one n-doped semiconductor portion (133, 134).

Portions of the top surface of the buried insulator layer 20 are exposed within the opening in the photoresist 147. The exposed portions of the buried insulator layer 20 are removed from underneath the opening in the photoresist 147 by an etch, which may be an isotropic etch or an anisotropic etch. The photoresist 147 protects covered portions of the buried insulator layer 20 from the etch. The etch is selective to the metal semiconductor alloy portions (140, 142, 144), the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and the semiconductor waveguide 136. A trench is formed within the buried insulator layer 20 underneath the opening in the photoresist 147. A top surface of the handle substrate 10 may be exposed underneath the trench in the buried insulator layer 20.

The trench may undercut the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and a portion of the semiconductor waveguide 136. Preferably, the undercut of the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and a portion of the semiconductor waveguide 136 is controlled to prevent a complete dissociation from the top surface of the buried insulator layer 20 and to insure that each of the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and a portion of the semiconductor waveguide 136 remains attached to the buried insulator layer 20. Preferably, the edge of the trench in the buried insulator layer 20 is directly adjoined to the middle sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) and the middle sub-portion(s) of the at least one n-doped semiconductor portion (133, 134). Each of the first sub-portion of the at least one p-doped semiconductor portion (131, 132) and each of the first sub-portion of the at least one n-doped semiconductor portion (133, 134) may laterally protrude from the edges of the trench within the buried insulator layer 20, and overhang above the trench in the buried insulator layer 20. The remaining portions of the buried insulator layer 20 constitute at least one dielectric material portion that vertically abuts the bottom surfaces of the second sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) and the second sub-portion(s) of the at leas one n-doped semiconductor portion (133, 134).

Referring to FIGS. 15A and 15B, the trench in the buried insulator layer 20 is filled with a dielectric material. Preferably, the dielectric material filling the trench in the buried insulator layer 20 comprises a different material than the dielectric material of the buried insulator layer 20. Preferably, the dielectric material filling the trench comprises a low dielectric constant (low-k) material having a dielectric constant less than 3.0. In this case, the dielectric material filling the trench constitutes a low dielectric constant (low-k) dielectric material portion 150. The low-k dielectric material portion 150 laterally abuts the buried insulator layer 20 and vertically abuts the bottom surfaces of the first sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) and the first sub-portion(s) of the at leas one n-doped semiconductor portion (133, 134). The interface between the buried insulator layer 20 and the low-k dielectric material portion 150 may be located underneath

the middle sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) and the middle sub-portion(s) of the at least one n-doped semiconductor portion (133, 134).

The dielectric material portion of the buried insulator layer 20 comprises a dielectric material having a second edge underlying the middle sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) located between one of the at least one first metal semiconductor region 140 and one of the at least one second metal semiconductor region 142 and having a third edge underlying a middle sub-portion(s) of the at least one n-doped semiconductor portion (133, 134) located between one of the at least one first metal semiconductor region 140 and the at least one third metal semiconductor region 144. Further, the low-k dielectric material portion 150 comprises a dielectric material having a second edge underlying the middle sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) located between one of the at least one first metal semiconductor region 140 and one of the at least one second metal semiconductor region 142 and having a third edge underlying a middle sub-portion(s) of the at least one n-doped semiconductor portion (133, 134) located between one of the at least one first metal semiconductor region 140 and the at least one third metal semiconductor region 144.

Exemplary low-k dielectric materials that may be employed for the low-k dielectric material portion 150 include, but are not limited to, fluorinated or non-fluorinated organic polymer based low k materials such as Dow Chemical's SiLK™ dielectric, Honeywell's Flare™, polyimides, benzocyclobutene, polybenzoxazoles, aromatic thermoset polymers based on polyphenylene ethers, chemical vapor deposited polymers such as poly(p-xylylene), and organosilicate glasses (OSG's) that may be deposited by chemical vapor deposition. Organosilicate glasses contain a matrix of a hydrogenated oxidized silicon carbon material (SiCOH) comprising atoms of Si, C, O and H in a covalently bonded tri-dimensional network, and may be referred to as SiCOH dielectric materials. The low-k dielectric materials may be porous or non-porous. Typically, the low-k dielectric material of the low-k dielectric material portion 150 has less thermal conductivity than the dielectric material of the buried insulator layer 20. The low-k dielectric material portion 150 as deposited may cover the entirety of the second exemplary semiconductor structure. Preferably, the top surface of the low-k dielectric material portion 150 is planar, which may be effected by

depositing a self-planarizing low-k dielectric material or by planarizing a non-self-planarizing low-k dielectric material layer by chemical mechanical planarization, a recess etch, or a combination thereof.

An optoelectronic device 160 is formed on the top surface of the low-k dielectric material portion 150. The optoelectronic device may be any device that manipulates an optical signal, i.e., electromagnetic radiation. The optical signal may be in the ultraviolet range, in the visible spectrum, in the infrared range, or in a microwave range. The optoelectronic device 160 may include a plurality of devices that manipulate at least one optical signal and may, or may not, be interconnected amongst one another. The optoelectronic device 160 may, or may not, be optically coupled to the semiconductor waveguide 136. In case the optoelectronic device 160 is optically coupled to the semiconductor waveguide 136, the optoelectronic device 160 may manipulate the optical signal that are fed into, or received from, the semiconductor waveguide 136. The optoelectronic device 160 may include at least one of a laser, optical amplifier, an optical sensor, a waveguide, a quantum well, or any other device that may manipulate an optical signal. The optoelectronic device 160 may comprise any semiconductor material that may be employed for the top semiconductor layer 129 as described above. Particularly, the optoelectronic device 160 may comprise a III-V compound semiconductor material such as GaAs, $In_xGa_{1-x}As$, $Al_xIn_yGa_{1-x-y}As$, InP, $In_xGa_{1-x}As_yP_{1-y}$, etc. The range of x, y, and 1-x-y are between 0 and 1. The optoelectronic device 160 may comprise a doped semiconductor material or an undoped semiconductor material.

Optionally, the region of the low-k dielectric material portion 150 that is not covered by the optoelectronic device 160 may be etched by an etch that is selective to the optoelectronic device, the second and third metal semiconductor alloy regions (142, 144), the at least one p-doped semiconductor portion (131, 132), and the at least one n-doped semiconductor portion (133, 134).

Referring to FIGS. 16A and 16B, an interconnect-level dielectric material layer 80 is formed over the optoelectronic device 160 and the exposed portions of the buried insulator layer 20, the at least one second metal semiconductor alloy region 142, the at least one third metal semiconductor alloy region 144, the at least one p-doped semiconductor portion (131, 132), and the at least one n-doped semiconductor portion (133, 134). FIG. 16A is a vertical cross-

sectional view along the vertical plane Z – Z' in FIG. 16B, and FIG. 16B is a top-down view of selected elements including the at least one p-doped semiconductor portion (131, 132), the at least one first metal semiconductor alloy region 140, the at least one second metal semiconductor alloy region 142, the at least one third metal semiconductor alloy region 144, and the semiconductor waveguide 136. The location of the optoelectronic device 160 is shown in a broken line. The interconnect-level dielectric material layer 80 comprises a dielectric material, which may comprise any of the dielectric material that may be employed for the buried insulator layer or the low-k dielectric material portion 150. Additionally or alternately, the interconnect-level dielectric material layer 80 may comprise a doped silicate glass such as phosphosilicate glass (PSG), borosilicate glass (BSG), borophosphosilicate glass (BPSG), fluorosilicate glass (FSG), etc. The interconnect-level dielectric material layer 80 may further include other dielectric materials as well.

A first set of via holes may be formed in the interconnect-level dielectric material layer 80 above the optoelectronic device 160 and filled with a compound semiconductor material to form at least one compound semiconductor via 85. Each of the at least one compound semiconductor via vertically abuts the optoelectronic device 160 and provides conduction of electrical current or transmission of light to or from the optoelectronic device 160.

A second set of via holes is formed in the interconnect-level dielectric material layer 80 above each of the at least one second metal semiconductor alloy region 142 and the at least one third metal semiconductor alloy region 144. At least one first metal contact via 90 abutting each of the at least one second metal semiconductor alloy region 142 and at least one second metal contact via 92 abutting each of the at least one third metal semiconductor alloy region 144 are formed within the second set of via holes by filling the second set of via holes with a conductive metal and removing excess metal from above the top surface of the interconnect-level dielectric material layer 80. The at least one first metal contact via 90 and the at least one second metal contact via 92 comprises a metallic material such as W, Ta, Ti, WN, TaN, TiN, Cu, and Al. Other metallic materials may also be employed instead of, or in addition to, the metallic material described above.

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Each adjoined set of a first metal contact via 90, a second metal semiconductor alloy region 142, a p-doped semiconductor portion (131, 132), a first metal semiconductor alloy region 140, an n-doped semiconductor portion (133, 134), a third metal semiconductor alloy region 144, and a second metal contact via 92 constitutes a temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92). Each temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) is configured to provide a path for conduction of electrical current.

The path for conduction of electrical current may be from a second metal contact via 92, then through a third metal semiconductor alloy region 144, then through an n-doped semiconductor portion (133, 134), then through a first metal semiconductor alloy region 140, then through a p-doped semiconductor portion (131, 132), then through a second metal semiconductor alloy region 142, and then to a first metal contact via 90. This direction of current flow is herein referred to as a forward current direction. Alternately, the path for conduction of electrical current may be from a first metal contact via 90, then through a second metal semiconductor alloy region 142, then through a p-doped semiconductor portion (131, 132), then through a first metal semiconductor alloy region 140, then through an n-doped semiconductor portion (133, 134), then through a third metal semiconductor alloy region 144, and then to a second metal contact via 92. This direction of current flow is herein referred to as a reverse current direction.

Each temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) is thermally coupled to the optoelectronic device 160, which comprises a semiconductor material and is configured to manipulate electromagnetic radiation, i.e., an optical signal.

As electrical current flows through each of the at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92), heat is transferred in the direction of the flow of the majority charge carrier. This is because the mechanism of Peltier-Seebeck effect is in operation in the at least one p-doped semiconductor portion (131, 132) and the at least one n-doped semiconductor portion (133, 134). According to Peltier-Seebeck effect, heat transfer accompanies diffusion of charge carriers in a semiconductor material and vice versa.

If the electrical current flows in the forward current direction, the majority charge carriers diffuse away from the interface with one of the at least one first metal semiconductor alloy region 140 and toward the interface with one of the at least one second metal semiconductor alloy region 142 and the at least one third metal semiconductor alloy region 144 within the p-doped semiconductor portion (131, 132) and the n-doped semiconductor region 134 of each temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92). The majority charge carriers are holes in the at least one p-doped semiconductor portion (131, 132), and are electrons in the at least one n-doped semiconductor region 134. The heat is further transferred to the at least one first metal contact via 90 and the at least one second metal contact via 92. Because of the thermal coupling between the at least one first metal semiconductor alloy region 140 and the optoelectronic device 160, the heat is also transferred from the optoelectronic device 160 to the at least one first metal semiconductor alloy region 140 as the at least one first metal semiconductor alloy region 140 is cooled. Therefore, there is a net heat transfer from the optoelectronic device 160 to the at least one first metal contact via 90 and the at least one second metal contact via 92. The heat that is transferred to the at least one first metal contact via 90 and the at least one second metal contact via 92 may further be transferred to a heat sink (not shown) through metallic interconnect structures embedded in the interconnect-level dielectric material layer 80.

If the electrical current flows in the reverse current direction, the majority charge carriers diffuse toward the interface with one of the at least one first metal semiconductor alloy region 140 and away from the interface with one of the at least one second metal semiconductor alloy region 142 and the at least one third metal semiconductor alloy region 144 within the p-doped semiconductor portion (131, 132) and the n-doped semiconductor region 134 of each temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92). The transferred heat accumulates at the at least one second metal semiconductor alloy region 142 and the at least one third metal semiconductor alloy region 144. Because of the thermal coupling between the at least one first metal semiconductor alloy region 140 and the optoelectronic device 160, the heat is further transferred from the at least one first metal semiconductor alloy region 140 to the optoelectronic device 160 as the at least one first metal semiconductor alloy region 140 is heated by heat transfer. Therefore, there is a net heat transfer from the at least one first metal contact via 90 and the at least one second metal

contact via 92 to the optoelectronic device 160. The heat may be transferred from a heat sink (not shown) to the at least one first metal contact via 90 and the at least one second metal contact via 92 through metallic interconnect structures embedded in the interconnect-level dielectric material layer 80, then subsequently transferred to the optoelectronic device 160.

Therefore, by reversing the direction of flow of the electrical current, the direction of heat transfer may be reversed. Further, by adjusting the magnitude of the electrical current, the amount of heat transfer may be regulated. Typically, the material of the low-k dielectric material portion 150 has a lower thermal conductivity than the material of the buried insulator layer 20, thereby increasing the thermal isolation of the at least one first metal semiconductor alloy portion 140 and the optoelectronic device 160 from the handle substrate 10.

The first semiconductor device may be operated with a feedback mechanism for performance of the optoelectronic device 160. For example, the performance of the optoelectronic device 160 may be monitored during operation. Based on the monitored performance level of the optoelectronic device, a direction of the electrical current or magnitude of the electrical current may be manipulated to heat or cool the optoelectronic device, thereby reducing deviation in the performance of the optoelectronic device 160 from a target performance level.

Referring to FIG. 17, a third exemplary semiconductor structure according to a third embodiment of the present invention is derived from the second exemplary semiconductor structure by forming a substantially intrinsic lower semiconductor portion 30 and a substantially intrinsic upper semiconductor portion 138 in each temperature control device. A vertically abutting pair of a substantially intrinsic lower semiconductor portion 30 and a substantially intrinsic upper semiconductor portion 138 is herein referred to as a substantially intrinsic semiconductor portion (30, 138). Thus, each of the at least one temperature control device may include the substantially intrinsic semiconductor portion 30.

The substantially intrinsic semiconductor portion (30, 138) is formed between a p-doped semiconductor portion (131, 132) and an n-doped semiconductor portion (133, 134) of the at

least one temperature control device (90, 142, 131, 132, 140, 30, 138, 133, 134, 144, 92). The substantially intrinsic semiconductor portion (30, 138) may have the same composition as the semiconductor waveguide 136. The substantially intrinsic semiconductor portion (30, 138) vertically abuts the first metal semiconductor alloy region 140 of the at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92). In one case, the p-doped semiconductor portion (131, 132) and the n-doped semiconductor portion (133, 134) may be not abut each other, and are laterally separated by the substantially intrinsic semiconductor portion (30, 138). In another case, the p-doped semiconductor portion (131, 132) and the n-doped semiconductor portion (133, 134) may abut each other and the substantially intrinsic semiconductor portion (30, 138).

A low-k dielectric material portion 150, an optoelectronic device 160, an interconnect-level dielectric material layer 80, at least one compound semiconductor via 85, at least one first metal contact via 90, and at least one second metal contact via 92 may be formed in the same manner as in the second embodiment. Within the collective volume of the at least one substantially intrinsic semiconductor portion (30, 138) and the at least one first metal semiconductor alloy region 140, the current flows primarily through the at least one first metal semiconductor alloy region 140. Therefore, the addition of the at least one substantially intrinsic semiconductor portion (30, 138) does not change the current path in a substantial manner relative to the current path in the second embodiment. The at least one temperature control device (90, 142, 131, 132, 140, 30, 138, 133, 134, 144, 92) may be operated in the same manner as in the second embodiment to control the temperature of the optoelectronic device 160 and to regulate the performance of the optoelectronic device 160.

Referring to FIG. 18, a fourth exemplary semiconductor structure according to a fourth embodiment of the present invention is shown. The fourth exemplary semiconductor structure is derived from the second exemplary semiconductor structure of FIGS. 13A and 4B by omitting the steps corresponding to FIGS. 14A and 5B in the processing sequence. Specifically, application of a photoresist 147, patterning of the photoresist 147, and transfer of the pattern in the photoresist 147 into an exposed portion of the buried insulator layer 20 are omitted in the third embodiment.

Instead of patterning the buried insulator layer 20, a lower portion of an interconnect-level dielectric material layer 80 is formed over the at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) and the semiconductor waveguide 136. The top surface of the lower portion of the interconnect-level dielectric material layer 80 is planarized by employing a self-planarizing material for the lower portion of the interconnect-level dielectric material layer 80 and/or by performing a planarization processing step such as chemical mechanical planarization or a recess etch. An optoelectronic device 160 is formed over the top surface of the lower portion of the interconnect-level dielectric material layer 80. The optoelectronic device 160 may be the same as in the second embodiment, and may overlie the at least one first metal semiconductor alloy region 140 and a portion of the semiconductor waveguide 136. An upper portion of the interconnect-level dielectric material layer 80 is formed over the optoelectronic device 160. The lower portion and the upper portion of the interconnect-level dielectric material layer 80 may comprise the same material as in the second embodiment. At least one compound semiconductor via 85, at least one first metal contact via 90, and at least one second metal contact via 92 may be formed in the same manner as in the second embodiment. The at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) may be operated in the same manner as in the second embodiment to control the temperature of the optoelectronic device 160 and to regulate the performance of the optoelectronic device 160.

Referring to FIG. 19, a fifth exemplary semiconductor structure according to a fifth embodiment of the present invention is derived from the second exemplary semiconductor structure by omitting formation of at least one compound semiconductor via 85.

Referring to FIG. 20, a sixth exemplary semiconductor structure according to a sixth embodiment of the present invention is derived from the second exemplary semiconductor structure at a step corresponding to FIGS. 14A and 5B by removing the photoresist 147 and employing a non-conformal deposition process to form a low-k dielectric material portion 150. The material of the low-k dielectric material portion 150 may be the same as in the second embodiment. The non-conformal property of the deposition process employed to form the low-k dielectric material portion 150 deposits a low-k dielectric material over

narrow portions of the of the semiconductor structures above the top surface of the buried insulator layer 20, i.e., between the at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) and the semiconductor waveguide 136. Thus a cavity 152 is formed within the low-k dielectric material portion 150.

Referring to FIG. 21, processing steps corresponding to FIGS. 15A – 7B of the second embodiment are performed on the sixth exemplary semiconductor structure. The cavity 152 may be under vacuum after processing, or may be filled with air or a gas. The cavity 152 has a dielectric constant that is substantially equal to 1.0. The cavity 152 has a lower thermal conductivity than the material of the buried insulator layer 20, thereby increasing the thermal isolation of the at least one first metal semiconductor alloy portion 140 and the optoelectronic device 160 from the handle substrate 10. The at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) may be operated in the same manner as in the second embodiment to control the temperature of the optoelectronic device 160 and to regulate the performance of the optoelectronic device 160.

Referring to FIG. 22, a seventh exemplary semiconductor structure according to a seventh embodiment of the present invention is shown. FIG. 111 is a top-down view of selected elements including p-doped semiconductor portions (131, 132), n-doped semiconductor portions (133, 134), first metal semiconductor alloy regions 140, second metal semiconductor alloy regions 142, third metal semiconductor alloy regions 144, first metal contact vias 90, second metal contact vias 92, and a semiconductor waveguide 136. The location of the optoelectronic device 160 is shown in a broken line. A vertical cross-sectional view along the plane Z – Z' is the same as FIG. 15A.

Each of the first metal semiconductor alloy regions 140 is located within a first annulus. Each of the p-doped semiconductor portions (131, 132) and n-doped semiconductor portions (133, 134) is located within a second annulus which encloses and abuts the first annulus. Each of the second metal semiconductor alloy regions 142 and the third metal semiconductor alloy regions 144 is located within a third annulus which encloses and abuts the second annulus. The p-doped semiconductor portions (131, 132), the n-doped semiconductor portions (133, 134), the first metal semiconductor alloy regions 140, the second metal

semiconductor alloy regions 142, and the third metal semiconductor alloy regions 144 constitute two temperature control devices (90, 142, 131, 132, 140, 133, 134, 144, 92) between which a semiconductor waveguide 136 is located. An optoelectronic device 160 overlies portions of the two temperature control devices (90, 142, 131, 132, 140, 133, 134, 144, 92) and the semiconductor waveguide 136 as in the second embodiment. The two temperature control devices (90, 142, 131, 132, 140, 133, 134, 144, 92) may be operated in the same manner as in the second embodiment to control the temperature of the optoelectronic device 160 and to regulate the performance of the optoelectronic device 160.

In general, topological variations may be performed to the at least one temperature control devices (90, 142, 131, 132, 140, 133, 134, 144, 92 and optionally 30 and 138) to any of the exemplary semiconductor structures described above. Further, additional temperature control devices having a similar structure may be added to any of the exemplary semiconductor structures described above.

While the invention has been described in terms of specific embodiments, it is evident in view of the foregoing description that numerous alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, the invention is intended to encompass all such alternatives, modifications and variations which fall within the scope and spirit of the invention and the following claims.

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CLAIMS

1. A semiconductor structure comprising:

a semiconductor waveguide having a first thickness and located on a top surface of an insulator layer;

a recessed semiconductor region of integral construction with said semiconductor waveguide, having a second thickness that is less than said first thickness, located on said insulator layer, and including a substantially undoped recessed semiconductor region;

a p-doped semiconductor region laterally abutting said substantially undoped recessed semiconductor region;

an n-doped semiconductor region laterally abutting said substantially undoped recessed semiconductor region and not abutting said p-doped semiconductor region; and

a recessed metal semiconductor alloy portion abutting said recessed semiconductor region, said p-doped semiconductor region, and said n-doped semiconductor region.

2. The semiconductor structure of Claim 1, wherein said semiconductor waveguide, said recessed semiconductor portion, said p-doped semiconductor portion, and said n-doped semiconductor portion comprise a same semiconductor material.

3. The semiconductor structure of Claim 1 or Claim 2, wherein said semiconductor waveguide, said recessed semiconductor portion, said p-doped semiconductor portion, and said n-doped semiconductor portion are single crystalline and are epitaxially aligned among one another.

4. The semiconductor structure of any preceding Claims, wherein said semiconductor waveguide comprises substantially undoped silicon or substantially undoped germanium.

5. The semiconductor structure of any preceding Claims, wherein said recessed semiconductor region includes a p-doped recessed semiconductor region which is a portion of said p-doped semiconductor region and an n-doped recessed semiconductor region which is a portion of said n-doped semiconductor region.

6. The semiconductor structure of any preceding Claims, further comprising:

another recessed semiconductor region of integral construction with said semiconductor waveguide, having said second thickness, located on said insulator layer, and including another substantially undoped recessed semiconductor region;

another p-doped semiconductor region laterally abutting said other substantially undoped recessed semiconductor region;

another n-doped semiconductor region laterally abutting said other substantially undoped recessed semiconductor region and not abutting said other p-doped semiconductor region; and

another recessed metal semiconductor alloy portion abutting said other recessed semiconductor region, said other p-doped semiconductor region, and said other n-doped semiconductor region, wherein said other recessed semiconductor region, said other p-doped semiconductor region, said other n-doped semiconductor region, and said other recessed metal semiconductor alloy portion are located on an opposite side of said recessed semiconductor region, said p-doped semiconductor region, said n-doped semiconductor region, and said recessed metal semiconductor alloy portion about said semiconductor waveguide.

7. A method of forming a semiconductor structure comprising:

forming shallow trench isolation structures laterally abutting a top semiconductor portion and vertically abutting a buried insulator layer in a top semiconductor layer of a semiconductor-on-insulator (SOI) substrate;

forming a semiconductor waveguide by patterning said top semiconductor portion;

forming a p-doped semiconductor region in said top semiconductor portion;

forming an n-doped semiconductor region not abutting said p-doped semiconductor region in said top semiconductor region; and

forming a recessed metal semiconductor alloy portion directly on a recessed region of said top semiconductor portion, wherein said recessed metal semiconductor alloy portion is formed directly on said p-doped semiconductor region and said n-doped semiconductor region.

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8. The method of Claim 7, further comprising forming a pair of recessed line trenches in said top semiconductor portion, wherein a remaining sub-portion of said top semiconductor portion having a first thickness and located between said pair of recessed line trenches constitutes said semiconductor waveguide, wherein sub-portions of said top semiconductor portion directly underneath said pair of line trenches constitute recessed semiconductor regions of integral construction with said semiconductor waveguide having a second thickness that is less than said first thickness, and wherein sidewalls of two sup-portions of said top semiconductor portion having said first thickness are exposed to said pair of recessed line trenches.

9. The method of Claim 8, further comprising:

implanting p-type dopants into an area including one of said two sup-portions of said top semiconductor portion and a portion of one of said recessed semiconductor regions to form said p-doped semiconductor region; and

implanting n-type dopants into an area including the other of said two sup-portions of said top semiconductor portion and another portion of said one of said recessed semiconductor regions to form said n-doped semiconductor region.

10. The method of Claim 9, further comprising:

forming a dielectric layer on said semiconductor waveguide, said recessed semiconductor regions, said p-doped semiconductor region, and said n-doped semiconductor region; and

lithographically patterning said dielectric layer to form a dielectric material portion abutting a top surface and sidewalls of said semiconductor waveguide and a dielectric spacer that abuts a sidewall of said p-doped semiconductor region and a sidewall of said n-doped semiconductor region.

11. A semiconductor structure comprising a temperature control device and an optoelectronic device,

wherein said temperature control device includes:

a first metal semiconductor alloy region located on a substrate;

a p-doped semiconductor portion abutting said first metal semiconductor alloy region and located on said substrate;

an n-doped semiconductor portion abutting said first metal semiconductor alloy region located on said substrate; wherein said temperature control device is configured to pass current from said p-doped semiconductor portion, through said first metal semiconductor alloy region, and to said n-doped semiconductor portion or from said n-doped semiconductor portion, through said first metal semiconductor alloy region, and to said p-doped semiconductor portion, and

wherein said optoelectronic device includes a device that comprises a semiconductor material, configured to manipulate electromagnetic radiation, and is thermally coupled to said temperature control device.

12. The semiconductor structure of Claim 11, wherein said optoelectronic device includes at least one of a laser, optical amplifier, an optical sensor, a waveguide, and a quantum well.

13. The semiconductor structure of Claim 11 or Claim 12, wherein said optoelectronic device includes a III-V compound semiconductor material.

14. The semiconductor structure of any of Claims 11 to 13, further comprising a dielectric material portion comprising a dielectric material and vertically abutting a bottom surface of said p-doped semiconductor portion and a bottom surface of said n-doped semiconductor portion.

15. The semiconductor structure of any of Claims 11 to 14, wherein said p-doped semiconductor portion laterally abuts said n-doped semiconductor portion.

16. The semiconductor structure of any of Claims 11 to 15, further comprising a substantially intrinsic semiconductor portion laterally abutting said p-doped semiconductor portion and said n-doped semiconductor portion and vertically abutting said first metal semiconductor alloy region, wherein said substantially intrinsic semiconductor portion has a resistivity greater than 1 Ohm-cm.

17. The semiconductor structure of any of Claims 11 to 16, wherein said temperature control device further comprises:

a second metal semiconductor alloy region vertically abutting said p-doped semiconductor portion;

a third metal semiconductor alloy region vertically abutting said n-doped semiconductor portion;

a first metal contact via abutting said second metal semiconductor alloy region; and

a second metal contact via abutting said third metal semiconductor alloy region.

18. A method of forming a semiconductor structure comprising a temperature control device and an optoelectronic device, said method including:

patterning a top semiconductor layer of a semiconductor-on-insulator substrate to form a p-doped semiconductor portion and an n-doped semiconductor portion;

forming a first metal semiconductor alloy region directly on said p-doped semiconductor portion and said n-doped semiconductor portion, wherein said p-doped semiconductor portion and an n-doped semiconductor portion and said first metal semiconductor alloy region constitute a portion of a temperature control device;

forming a current conduction path configured to pass current from said p-doped semiconductor portion, through said first metal semiconductor alloy region, and to said n-doped semiconductor portion or from said n-doped semiconductor portion, through said first metal semiconductor alloy region, and to said p-doped semiconductor portion; and

forming an optoelectronic device comprising a semiconductor material, configured to manipulate electromagnetic radiation, and is thermally coupled to said temperature control device.

19. The method of Claim 18, further comprising:

removing a portion of a buried insulator layer underneath a sub-portion of said p-doped semiconductor portion and a sub-portion of said n-doped semiconductor portion to form a trench in said buried insulator layer; and

filling said trench with a low dielectric constant (low-k) material having a dielectric constant less than 3.0, wherein said optoelectronic device is formed over said low-k material.

20. The method of Claim 18 or Claim 19, further comprising forming a cavity laterally abutting a remaining portion of said buried insulator layer by removing said low-k material selective to said remaining portion of said buried insulator layer.

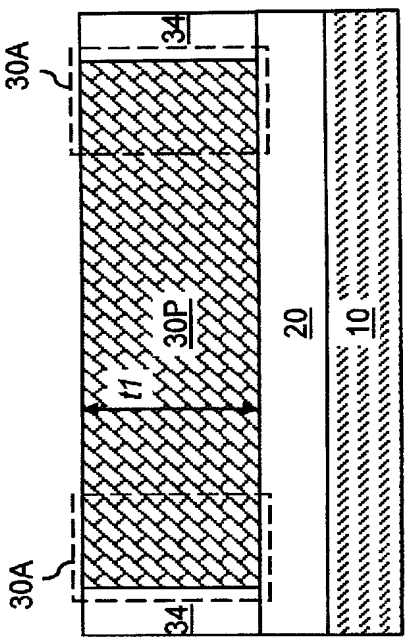

FIG. 1B

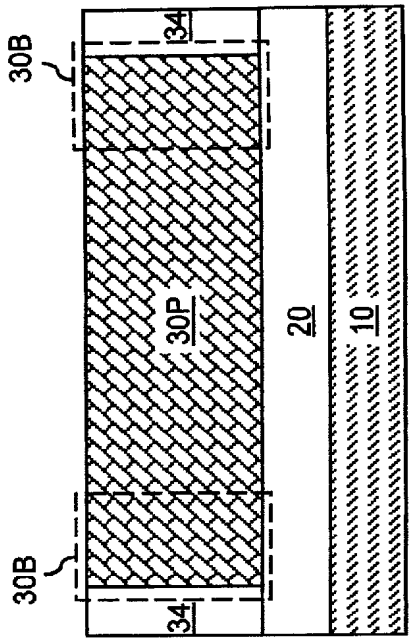

FIG. 1C

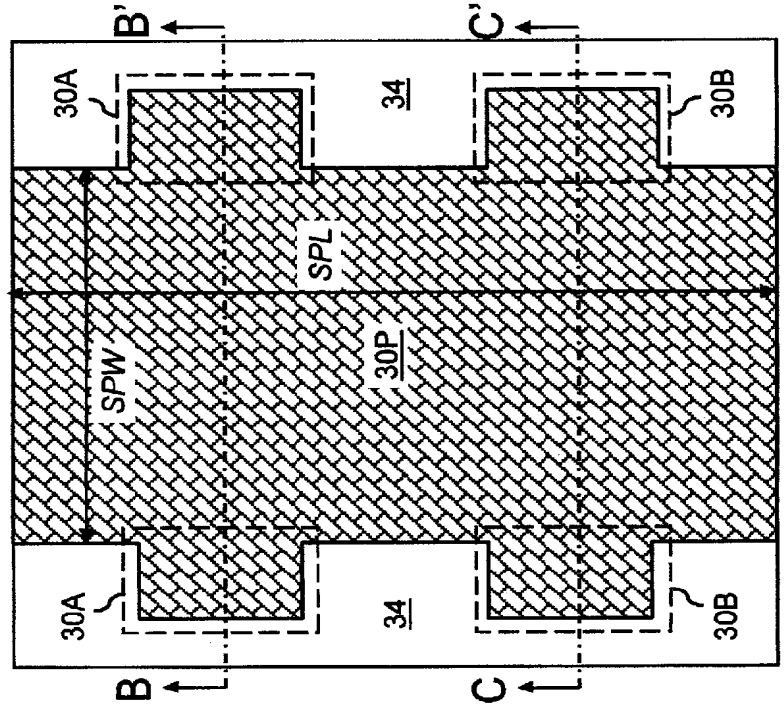

FIG. 1A

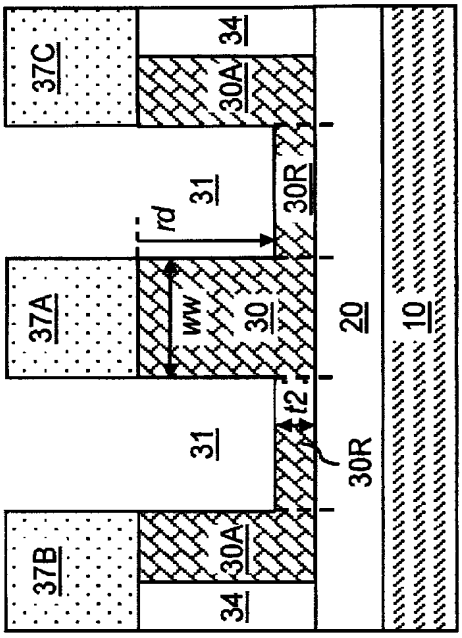

FIG. 2B

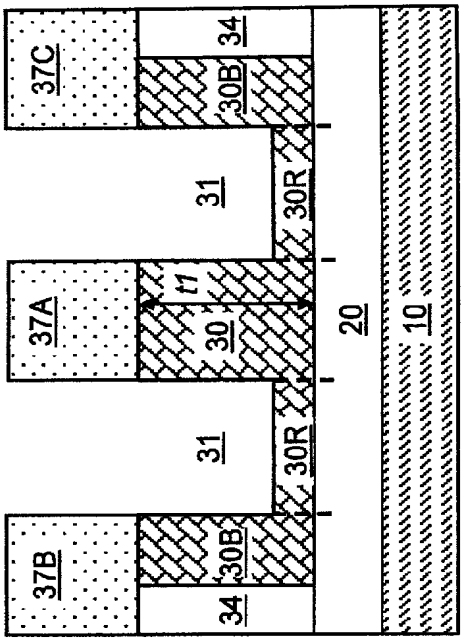

FIG. 2C

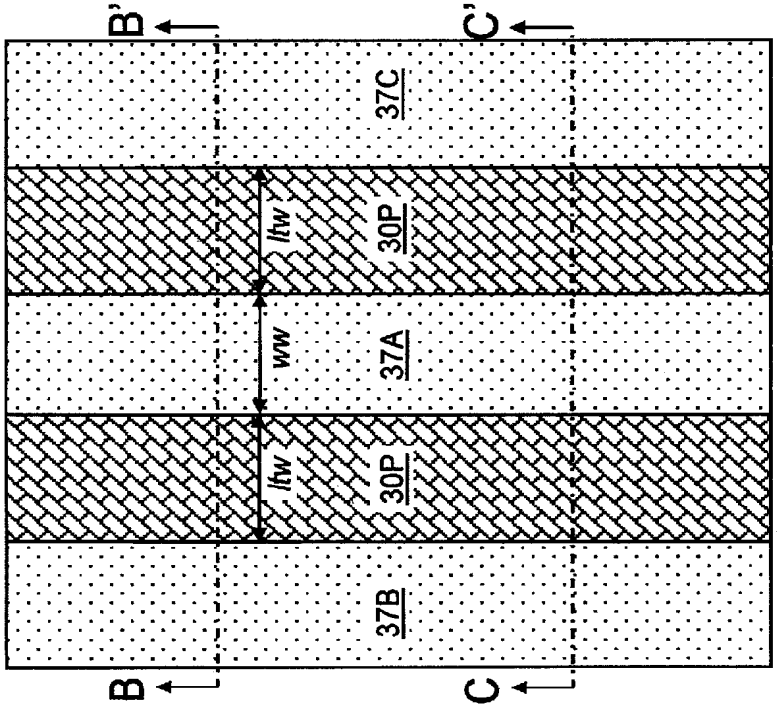

FIG. 2A

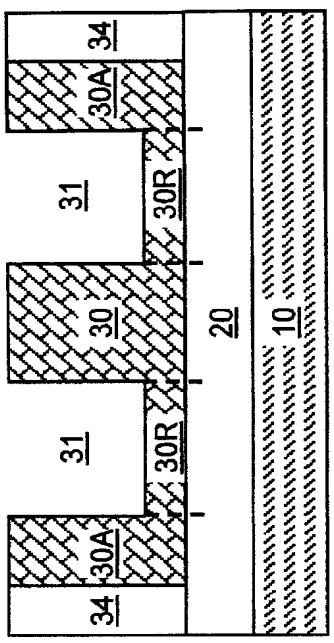

FIG. 3B

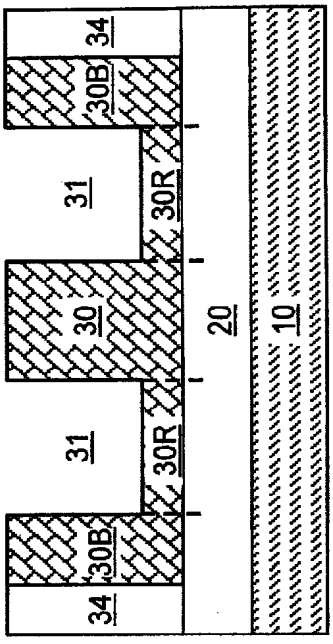

FIG. 3C

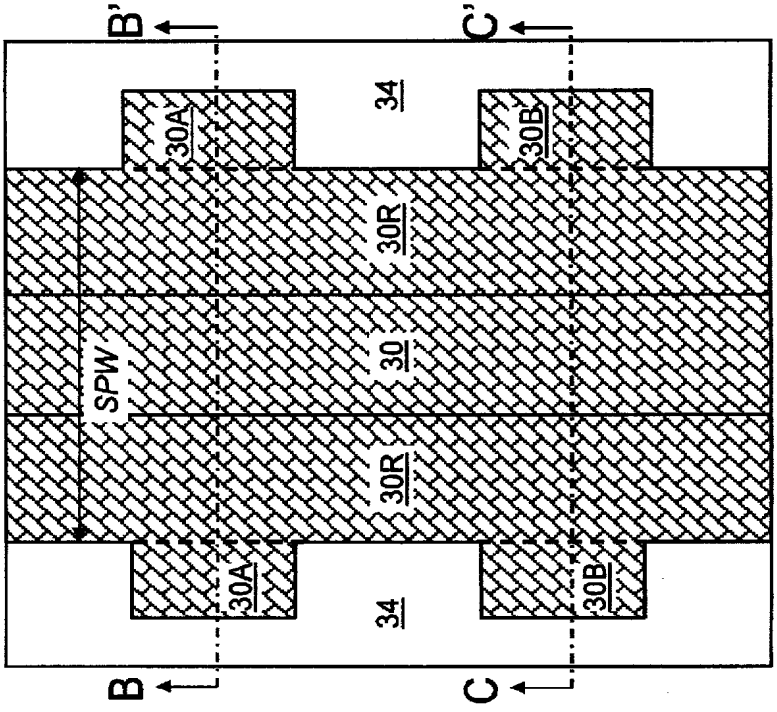

FIG. 3A

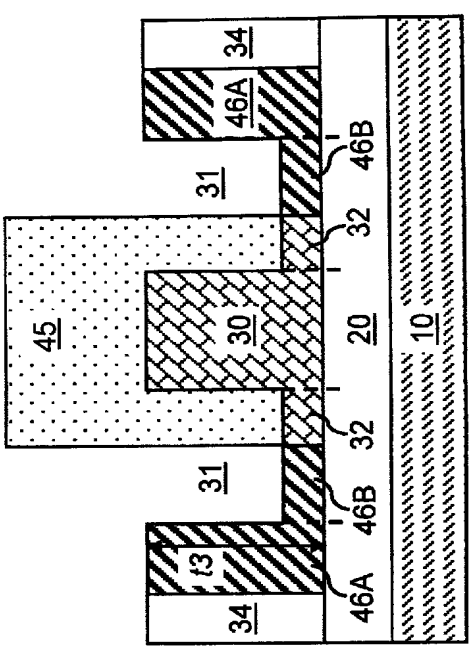

FIG. 4B

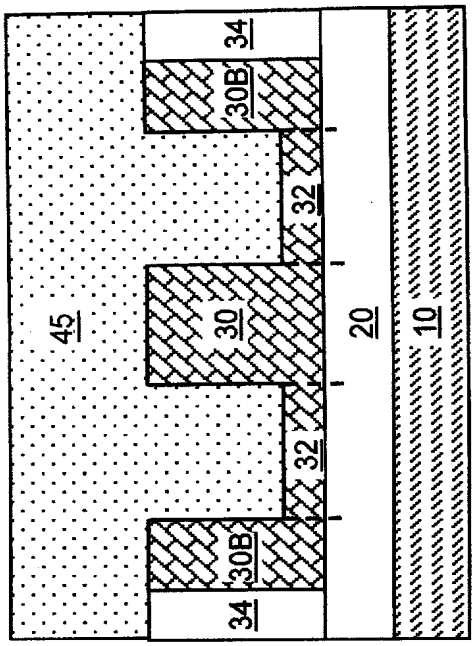

FIG. 4C

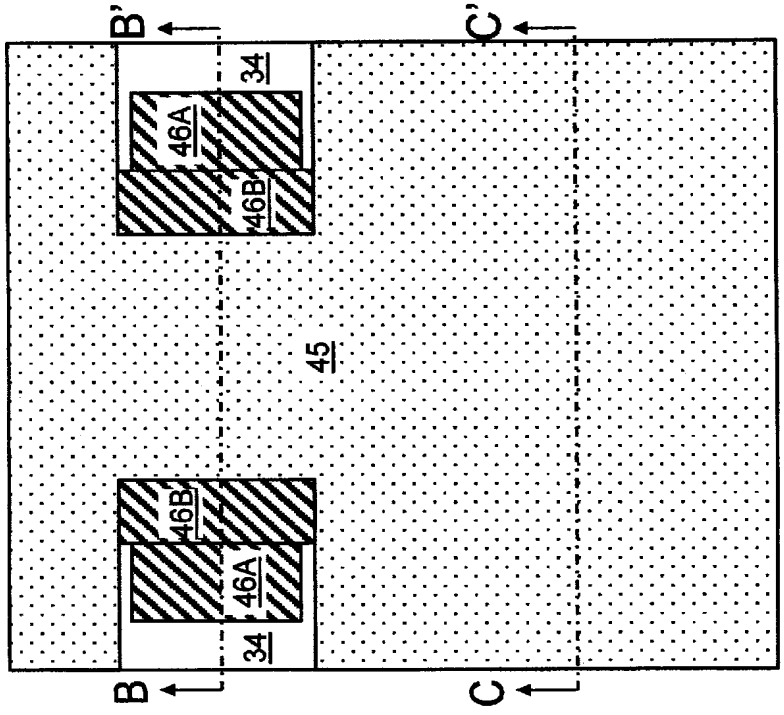

FIG. 4A

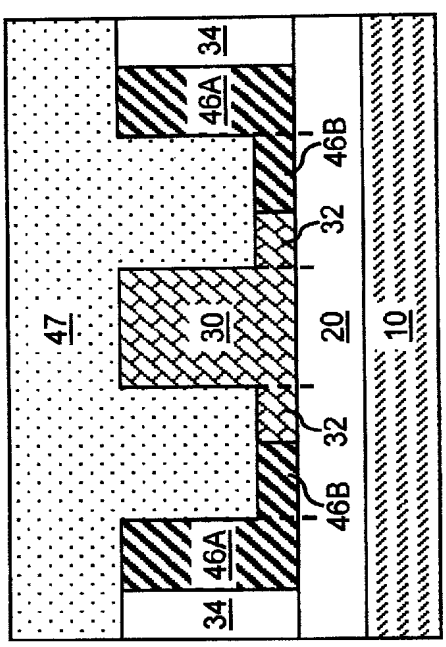

FIG. 5B

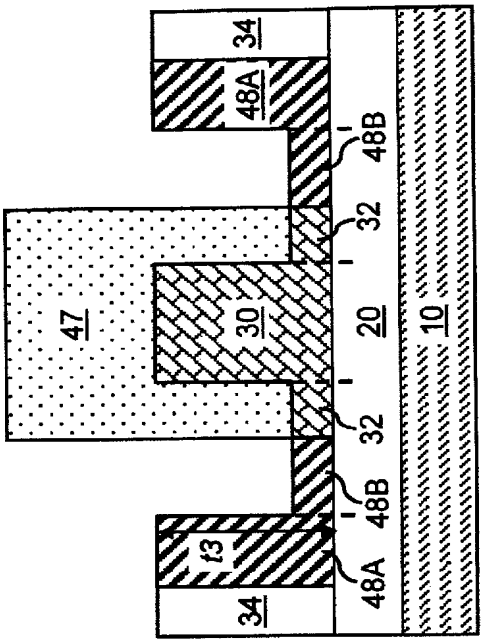

FIG. 5C

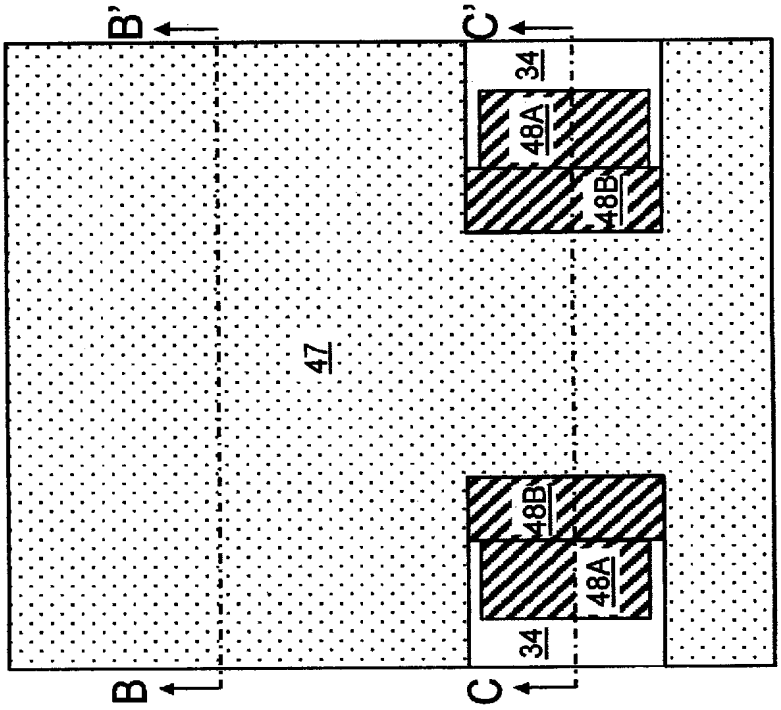

FIG. 5A

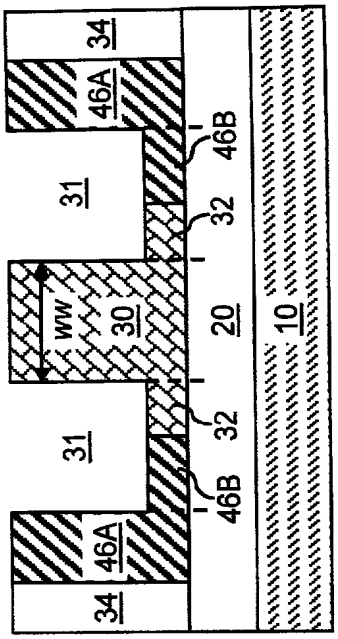

FIG. 6B

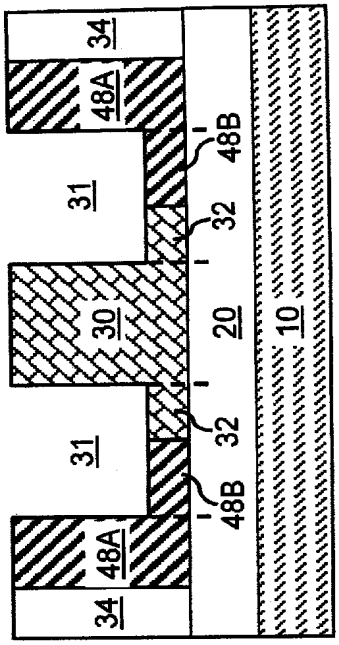

FIG. 6C

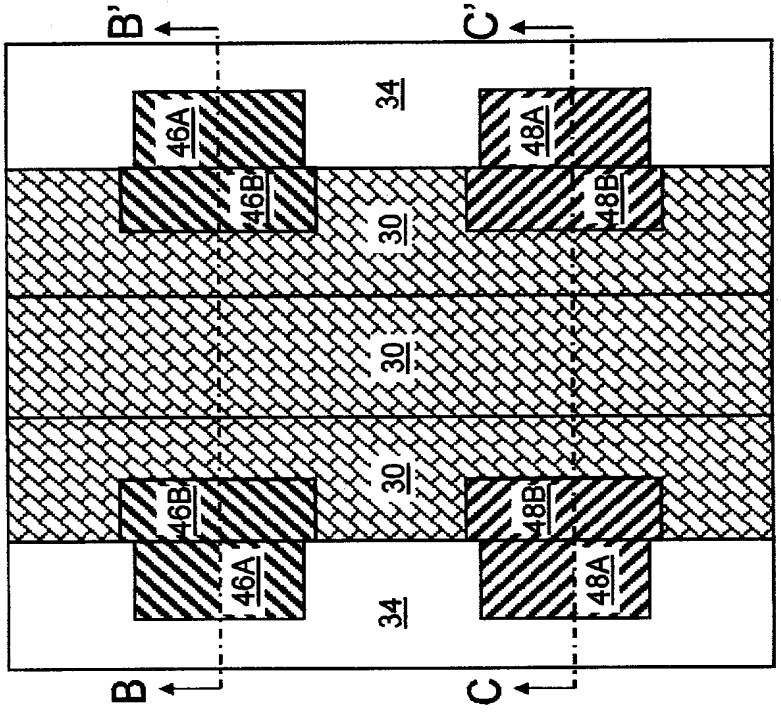

FIG. 6A

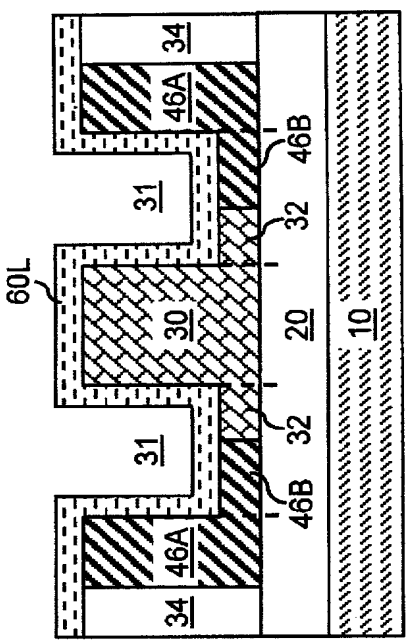

FIG. 7B

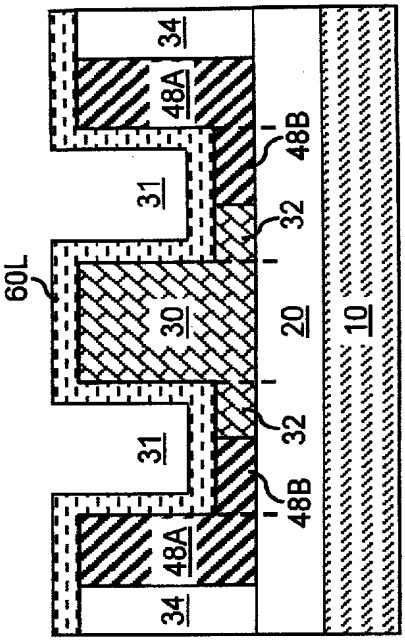

FIG. 7C

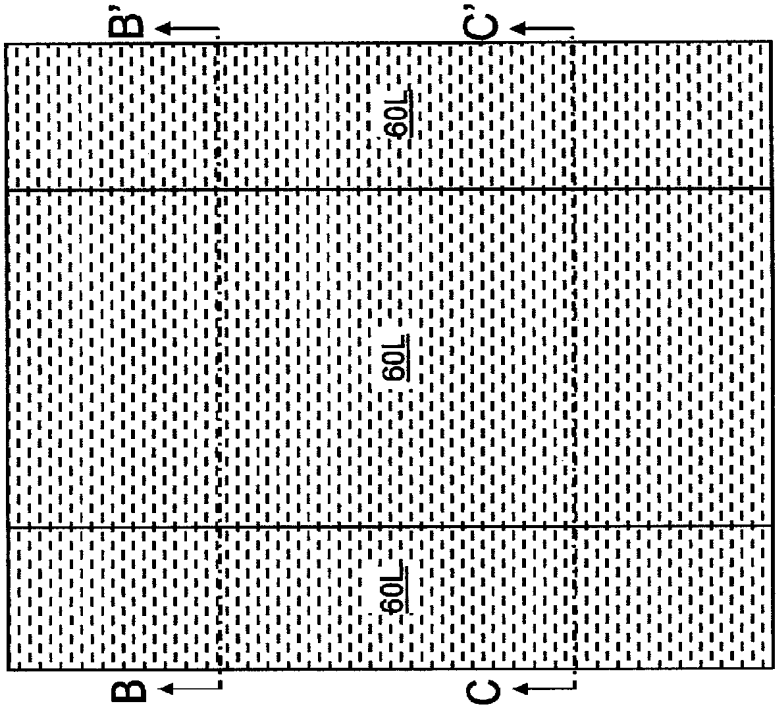

FIG. 7A

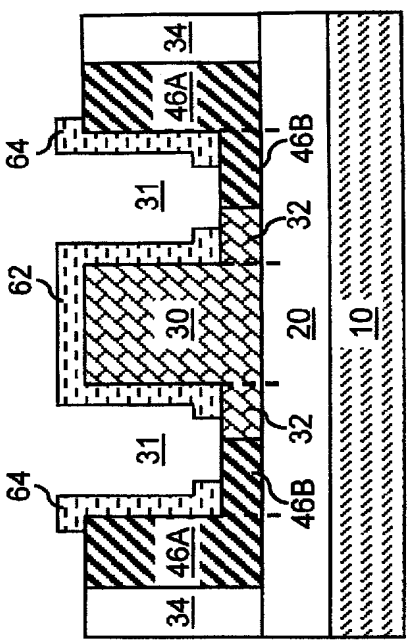

FIG. 8B

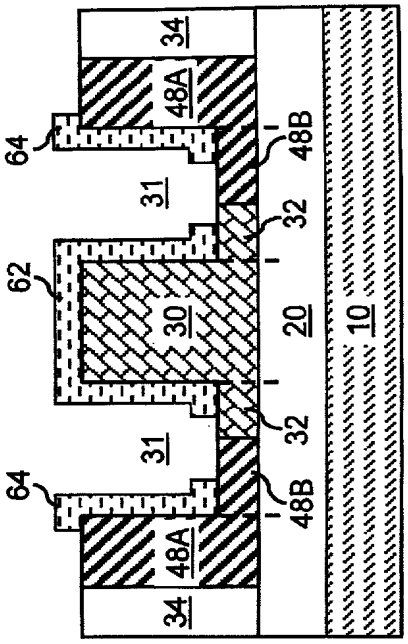

FIG. 8C

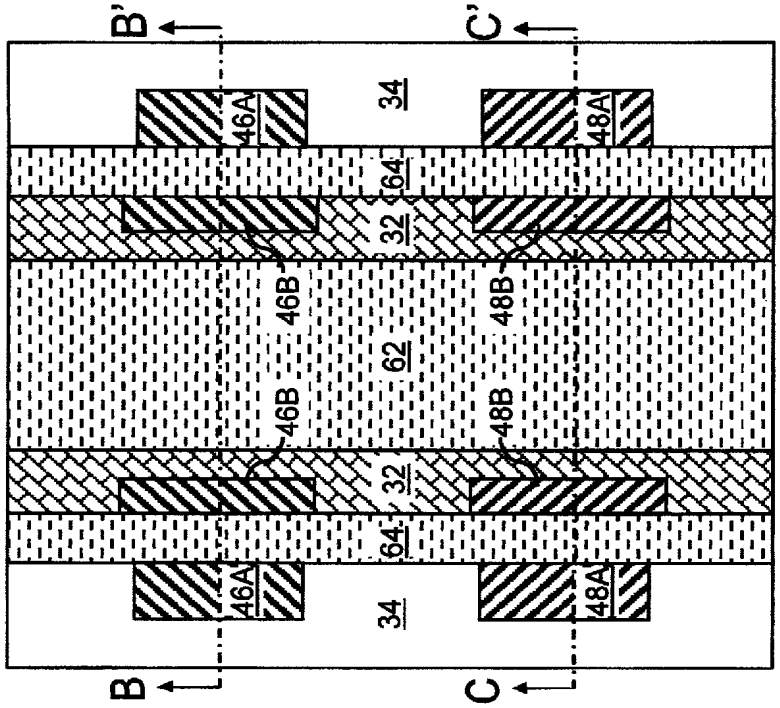

FIG. 8A

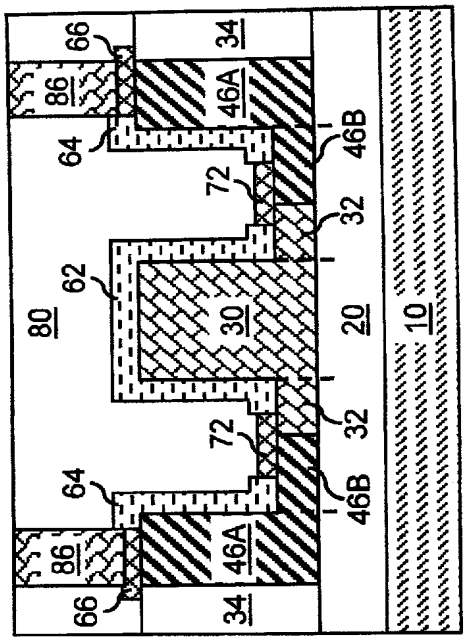

FIG. 9B

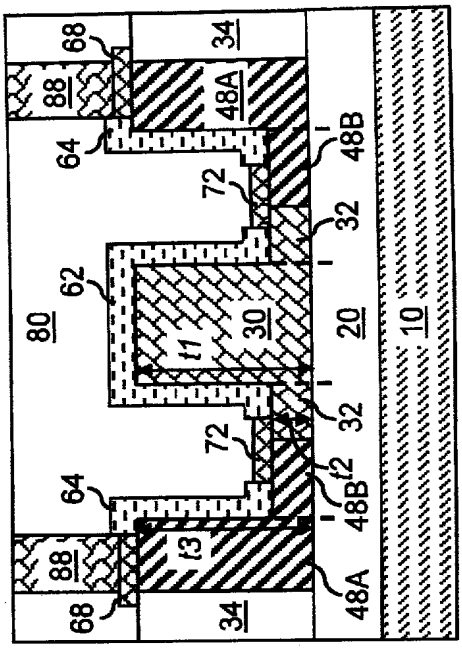

FIG. 9C

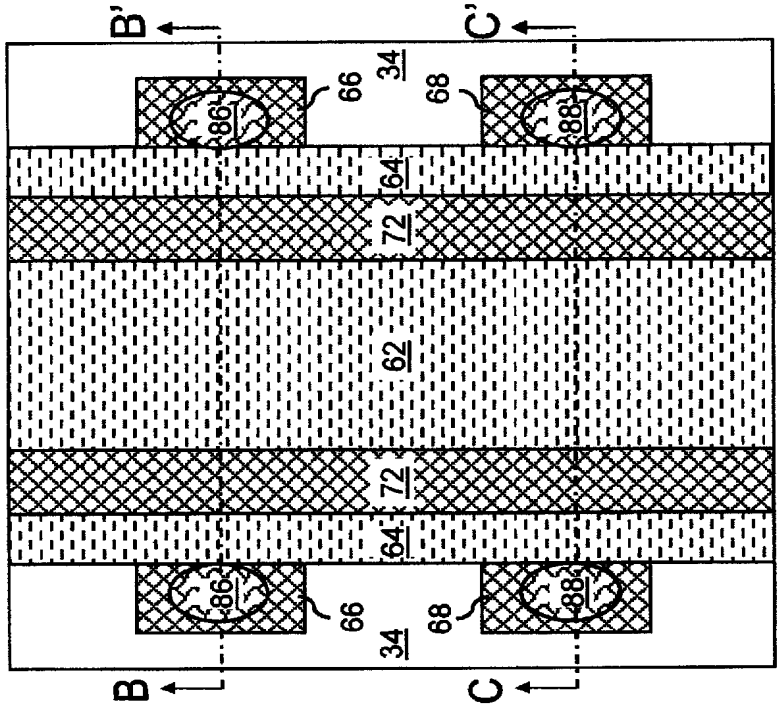

FIG. 9A

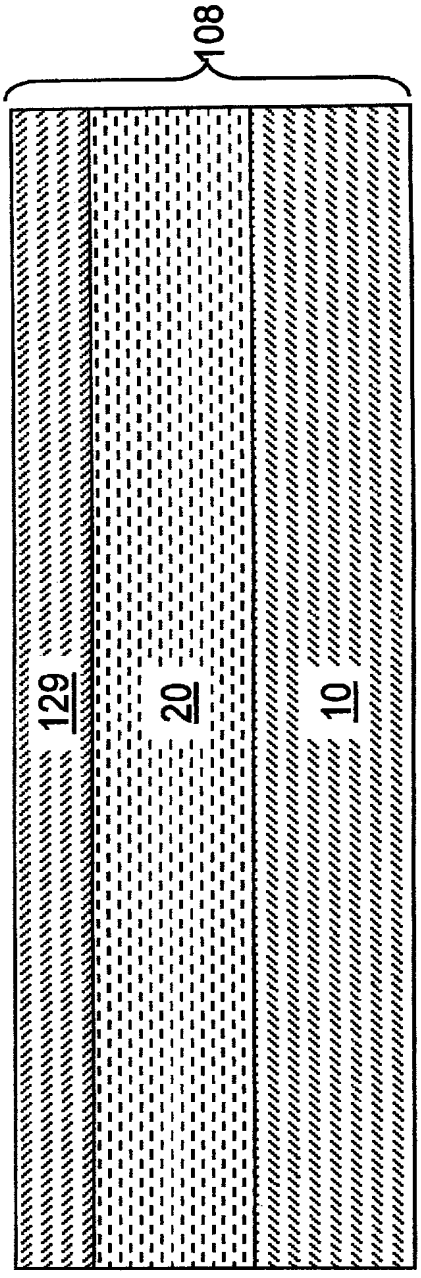

FIG. 10

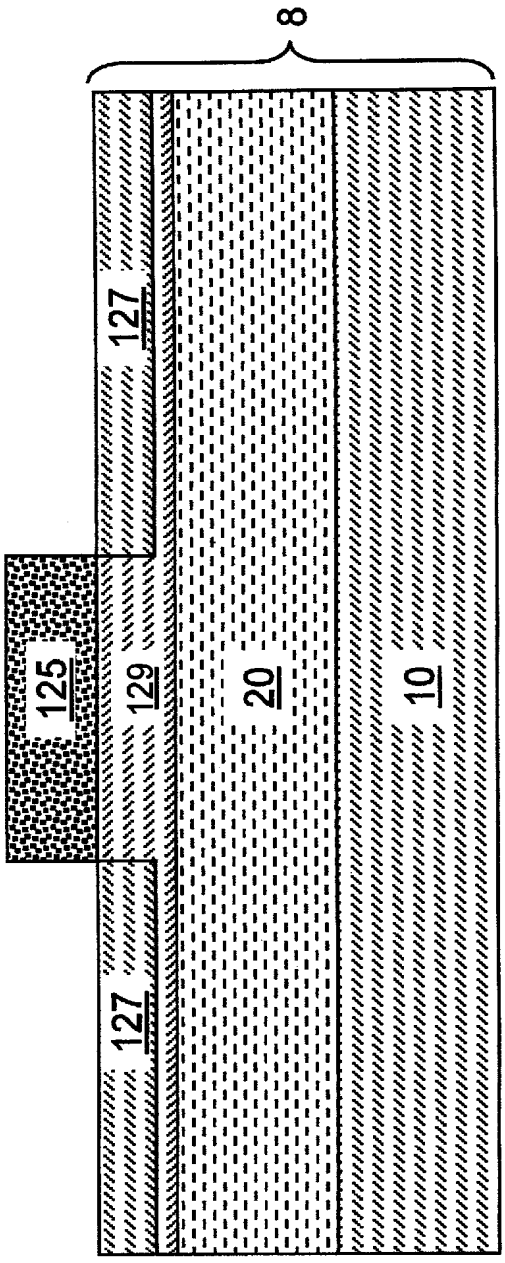

FIG. 11

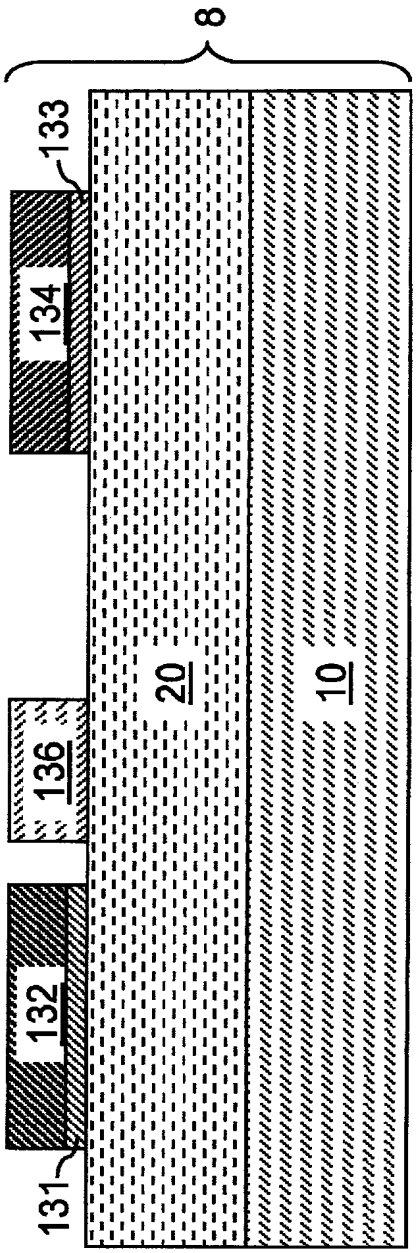

FIG. 12A

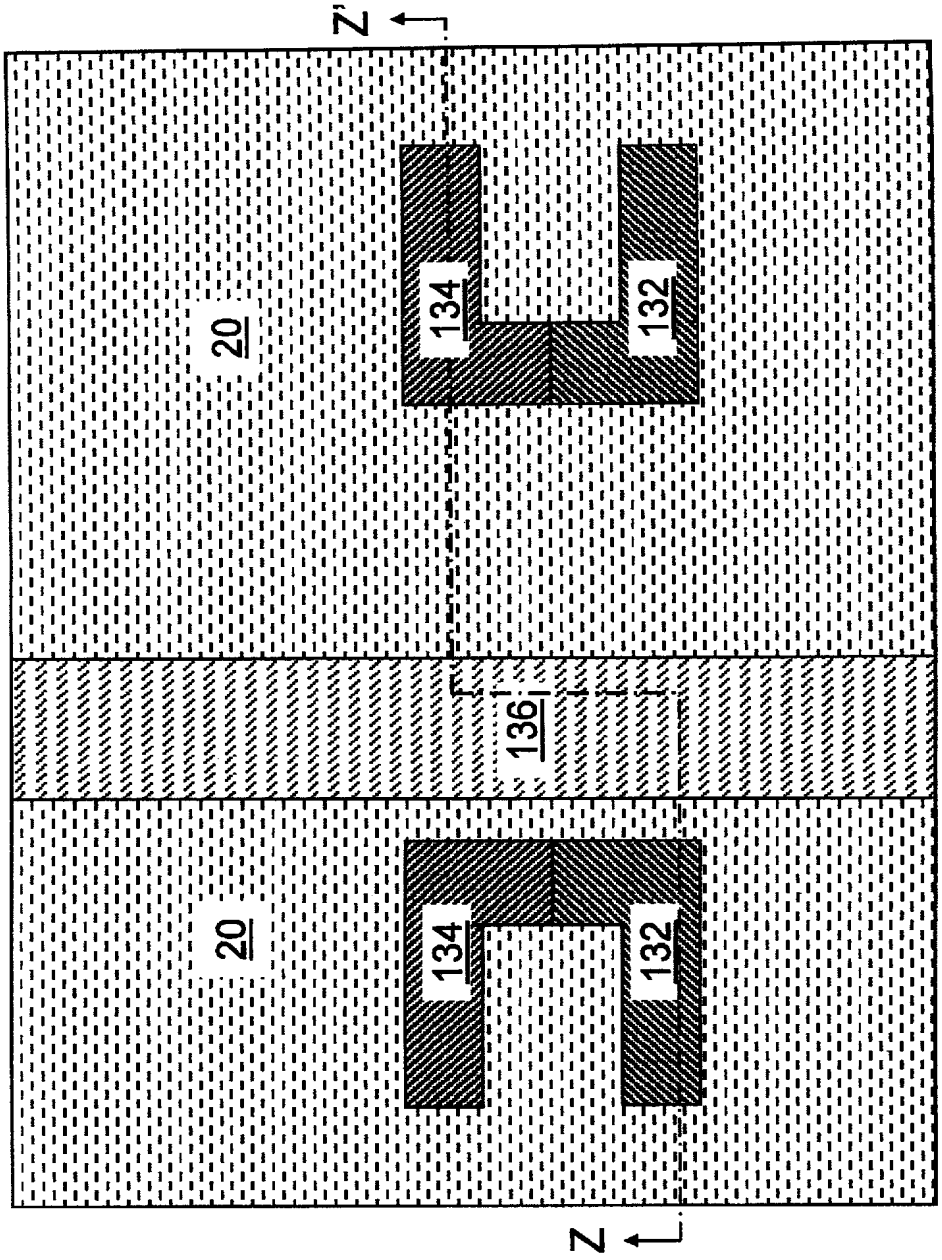

FIG. 12B

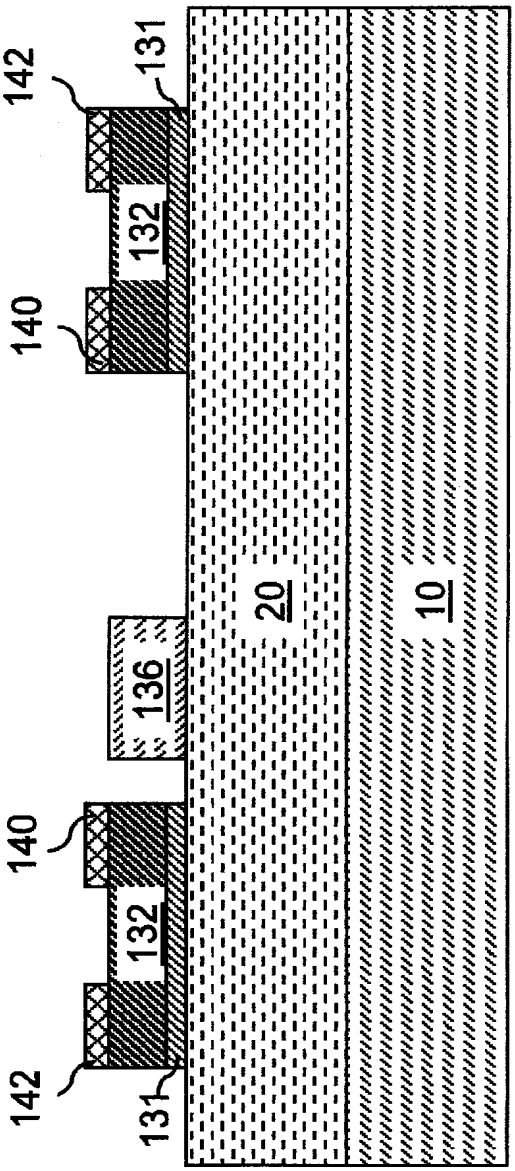

FIG. 13A

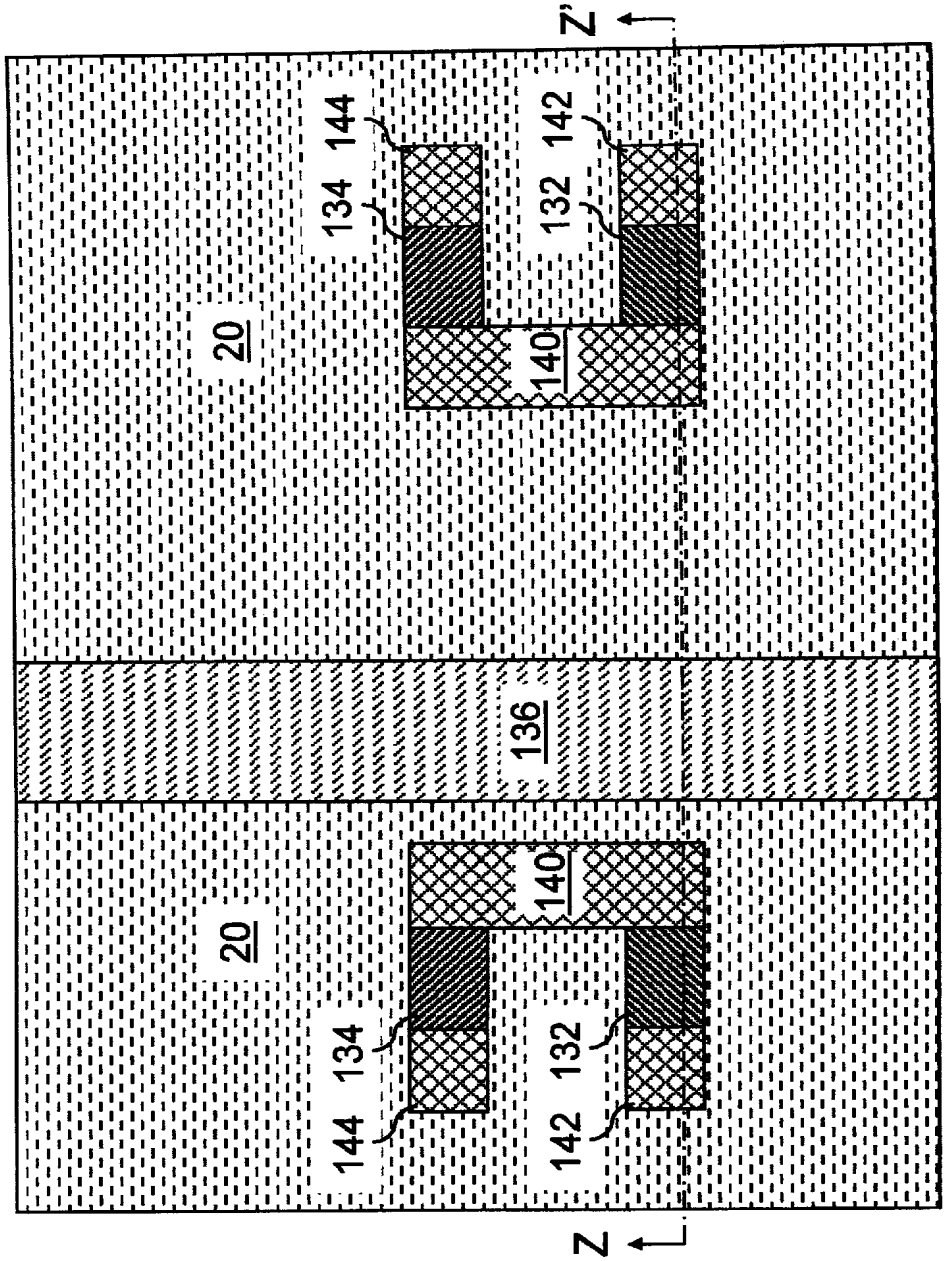

FIG. 13B

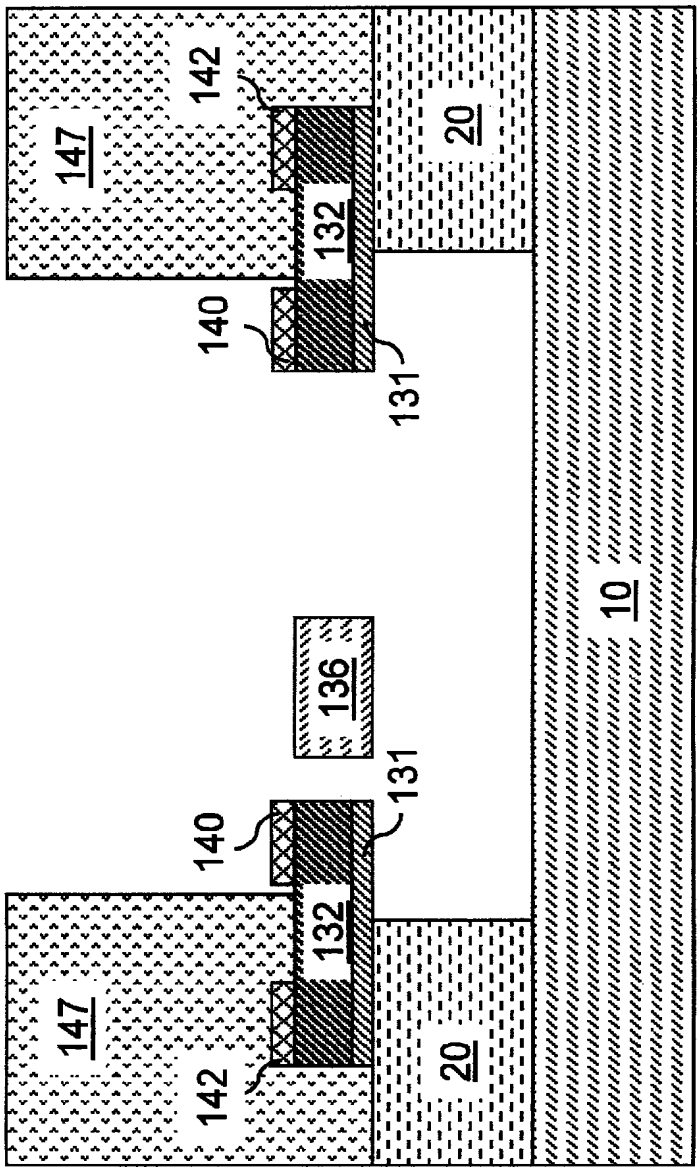

FIG. 14A

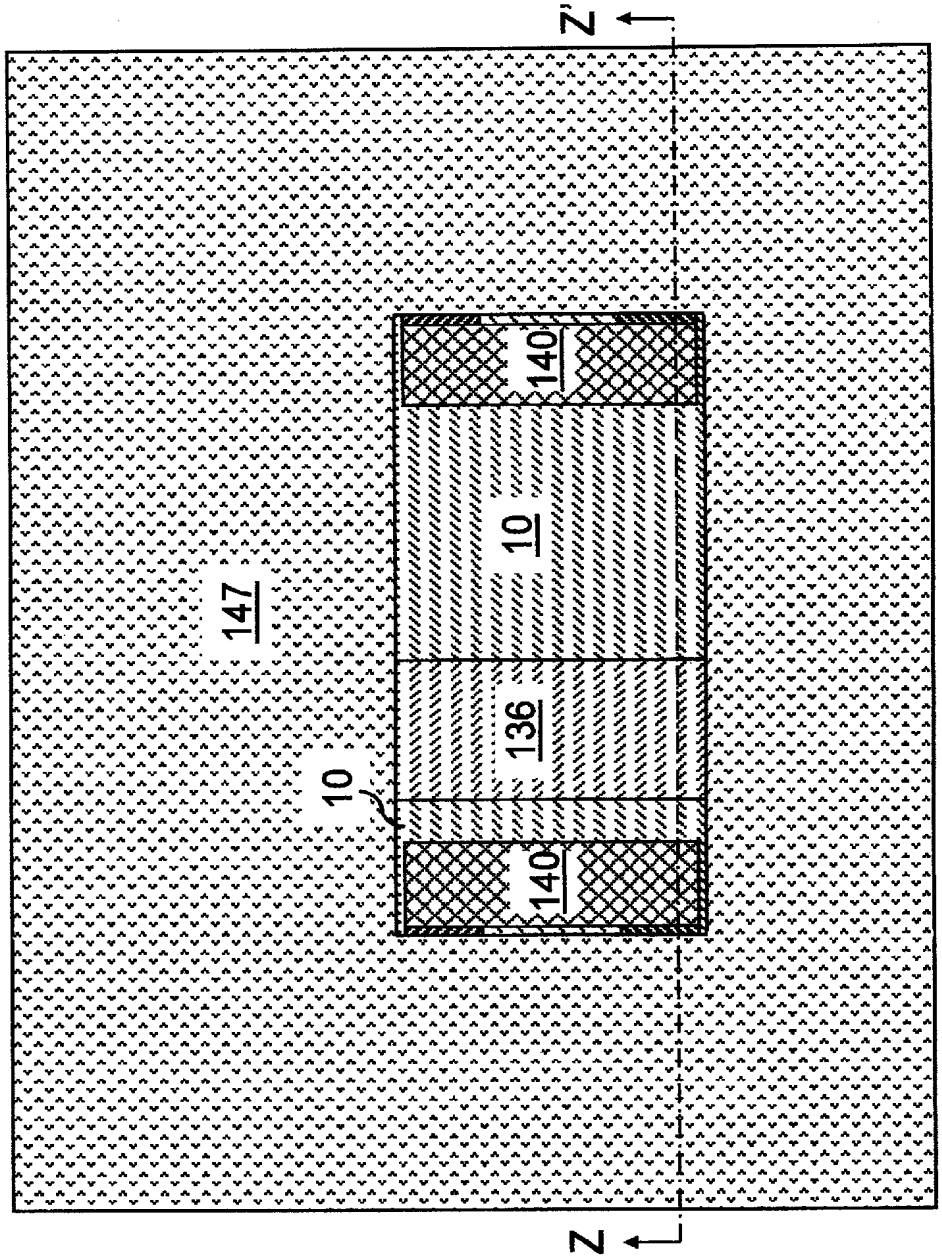

FIG. 14B

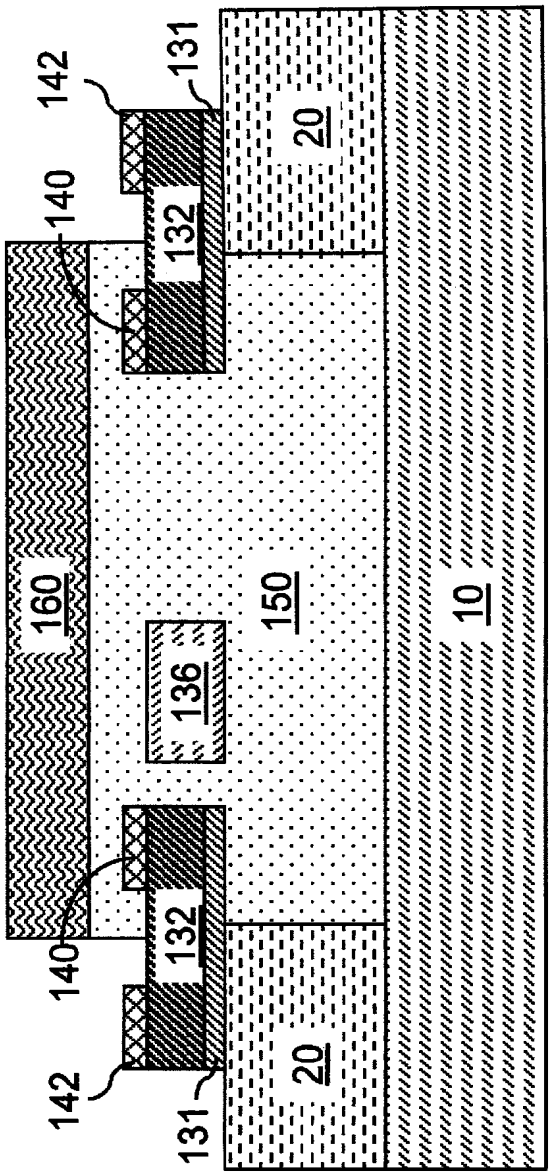

FIG. 15A

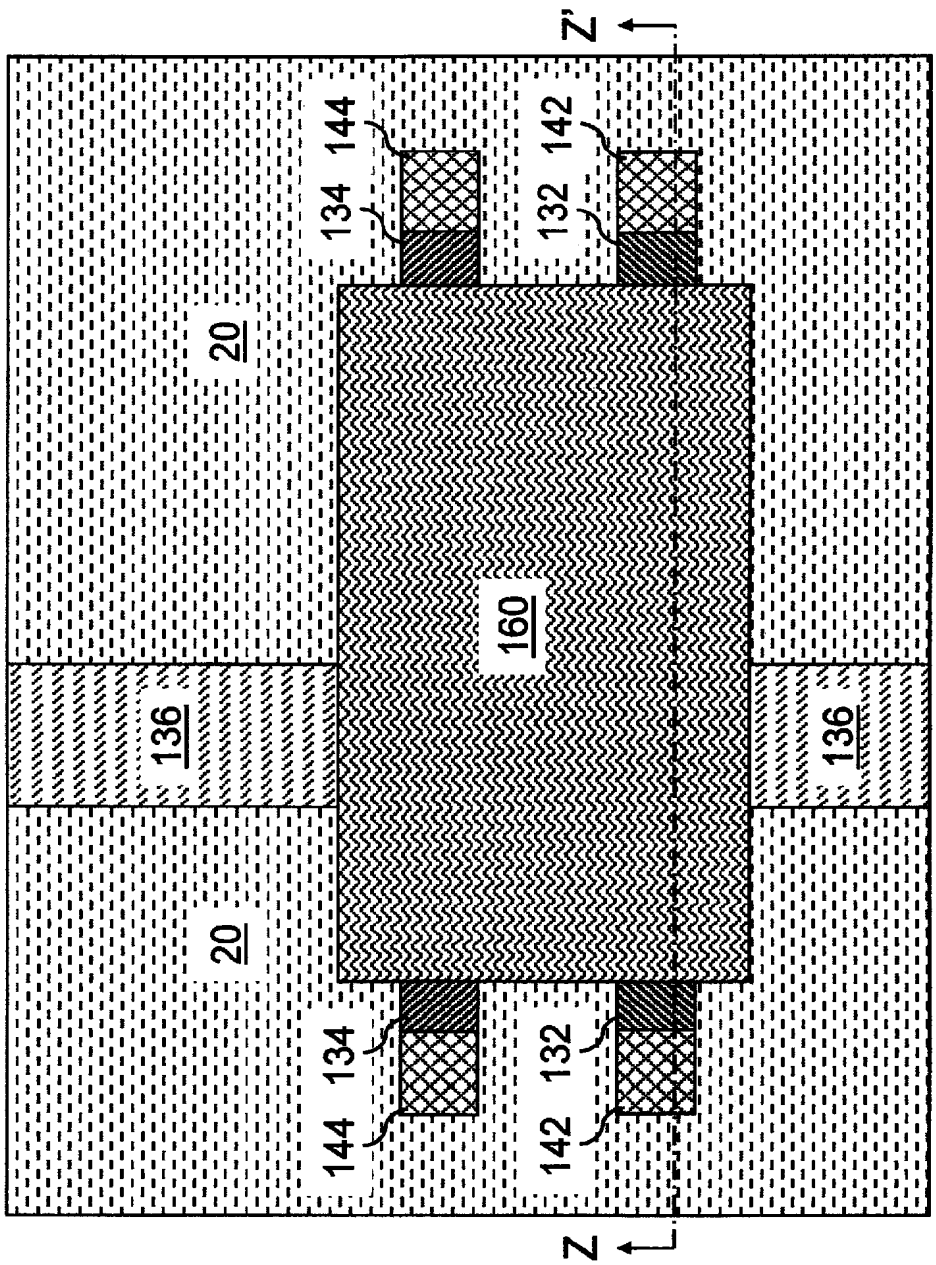

FIG. 15B

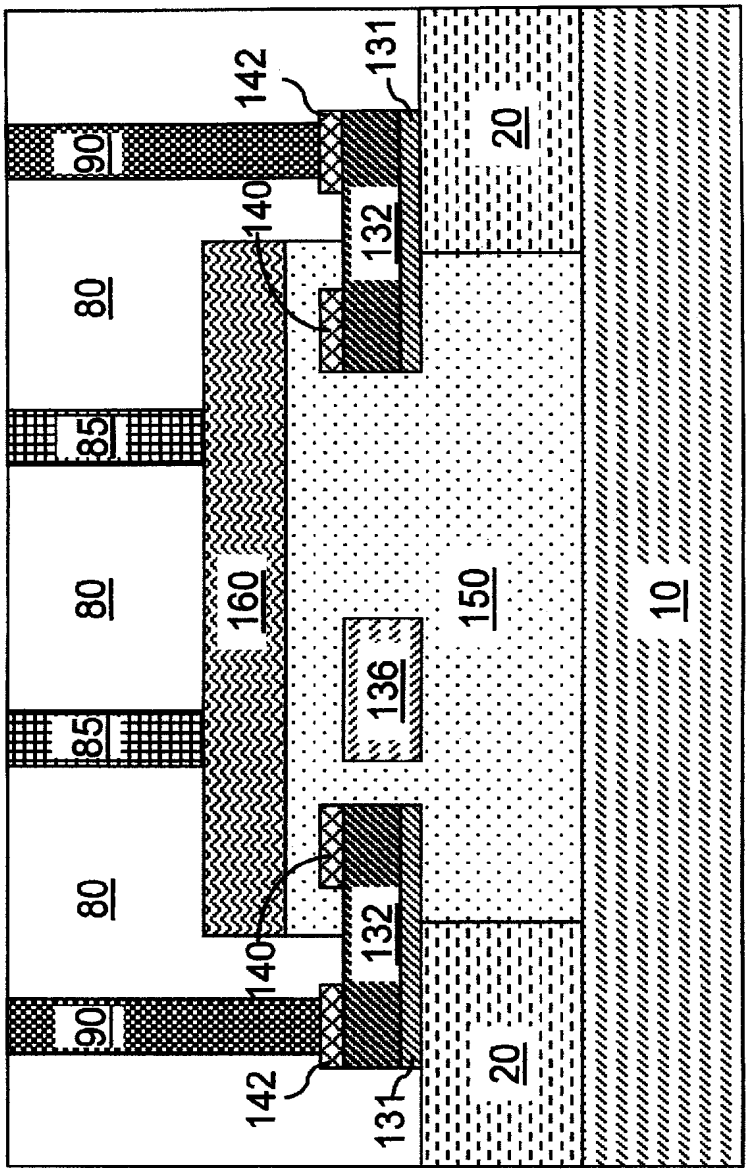
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FIG. 16A

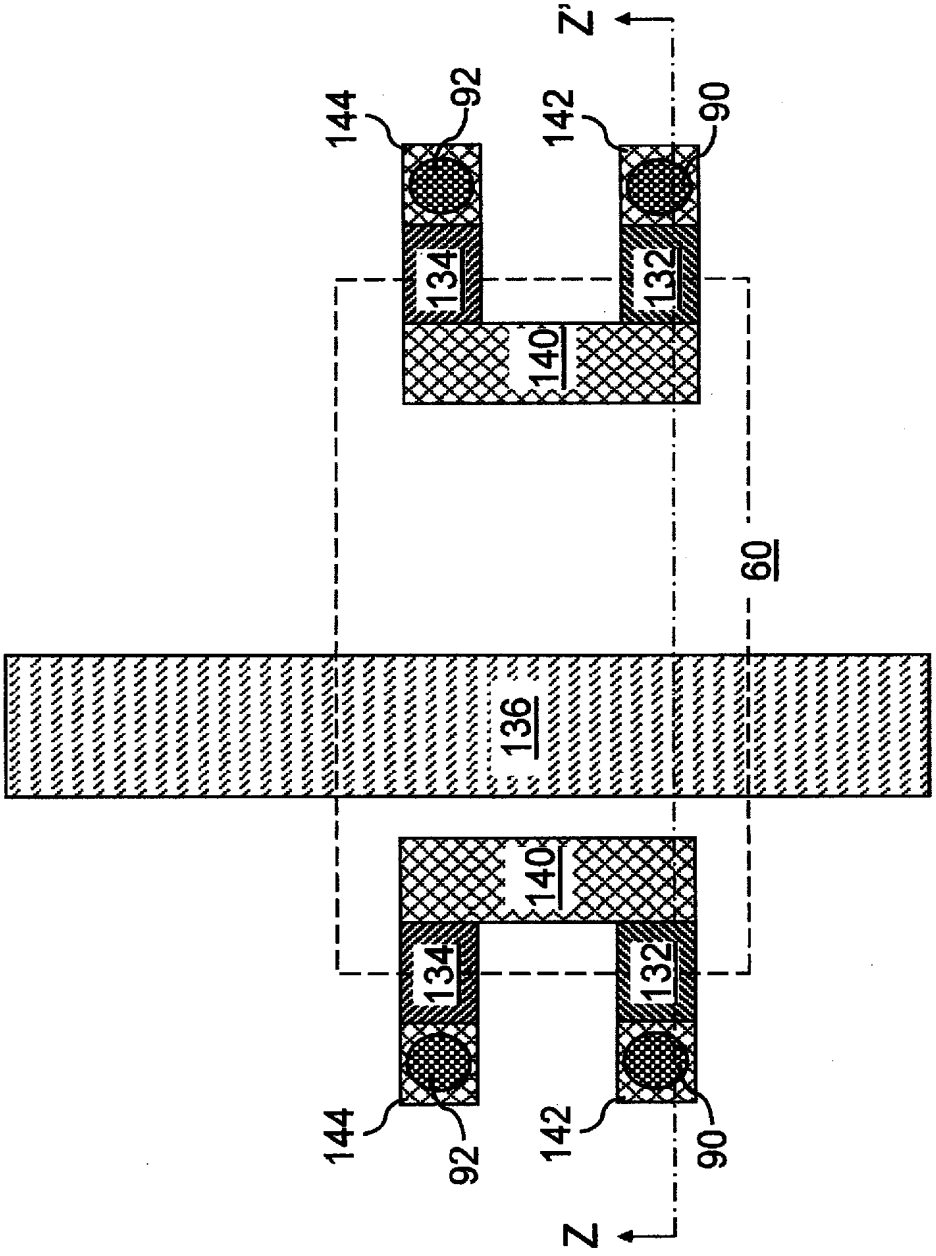

FIG. 16B

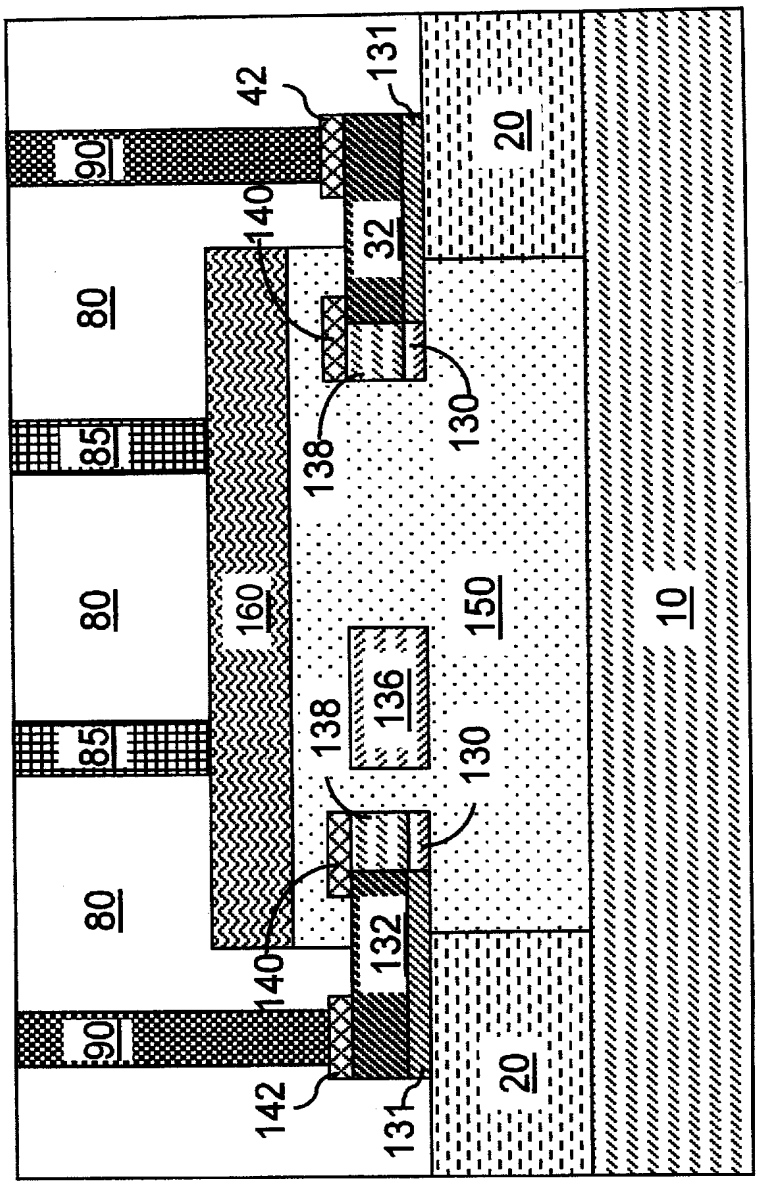
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FIG. 17

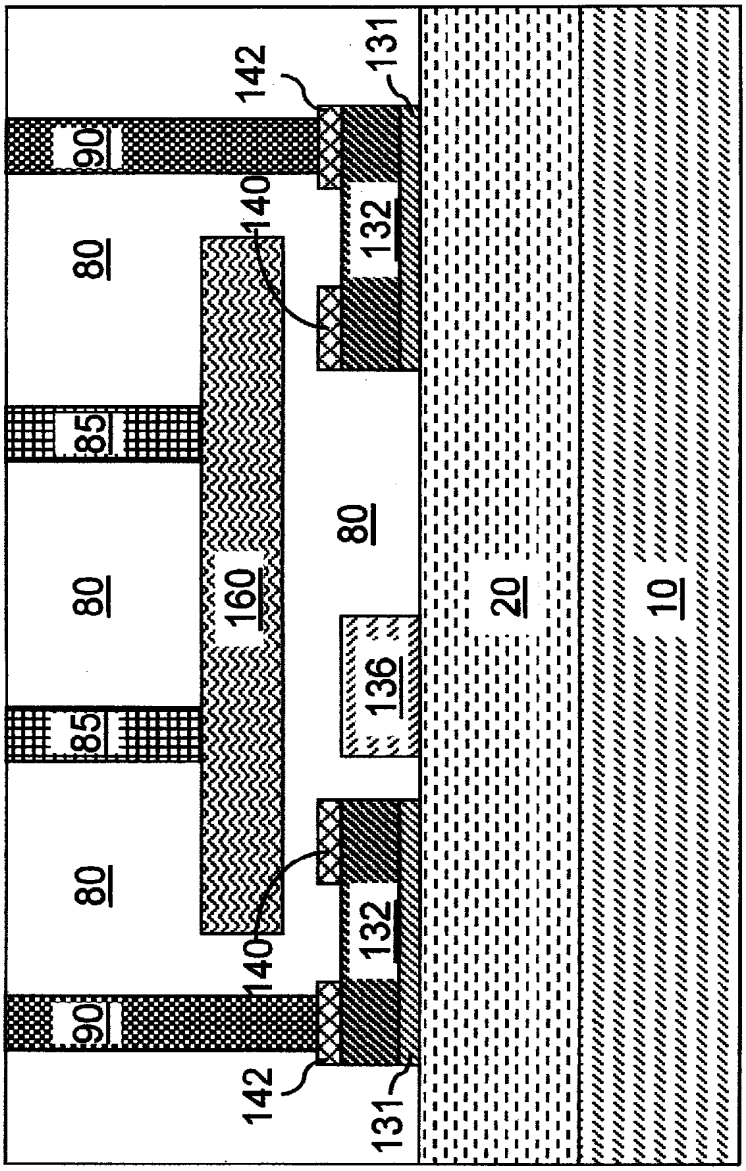
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FIG. 18

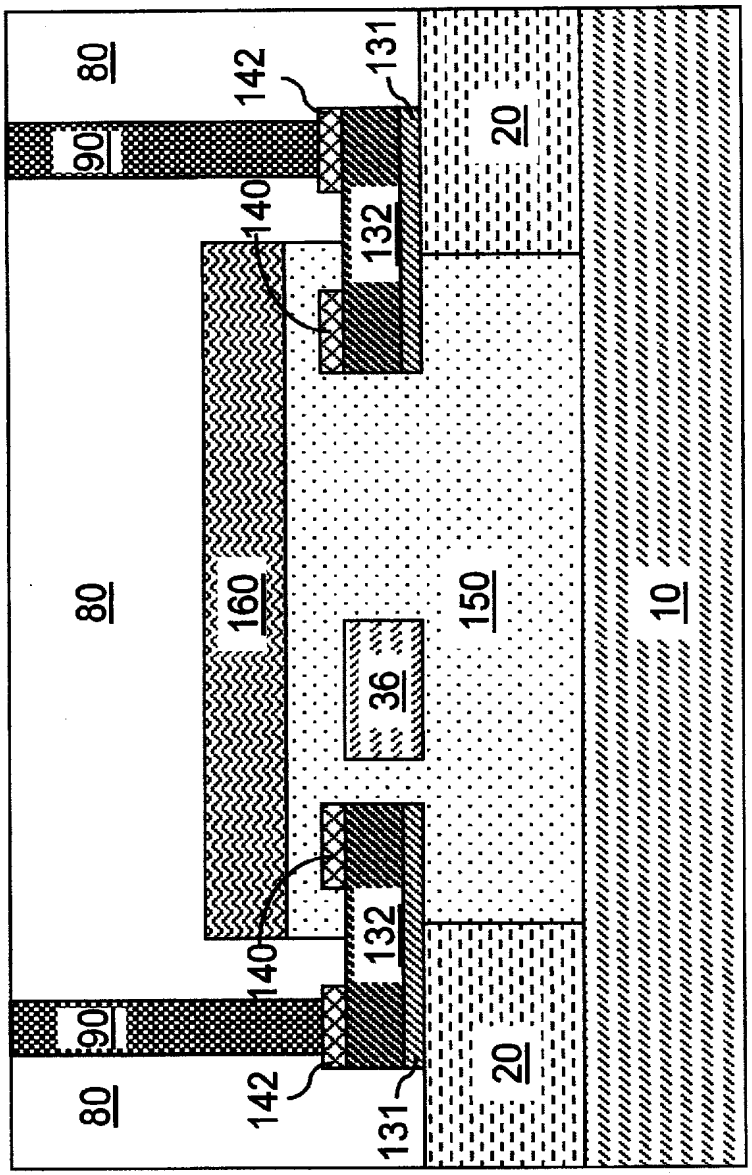

FIG. 19

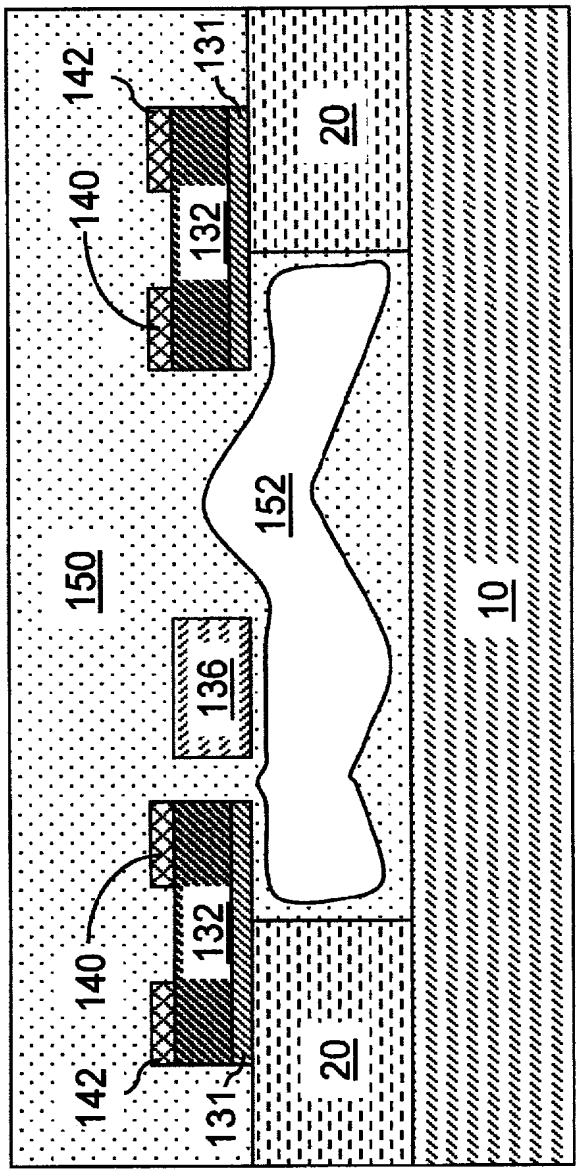

FIG. 20

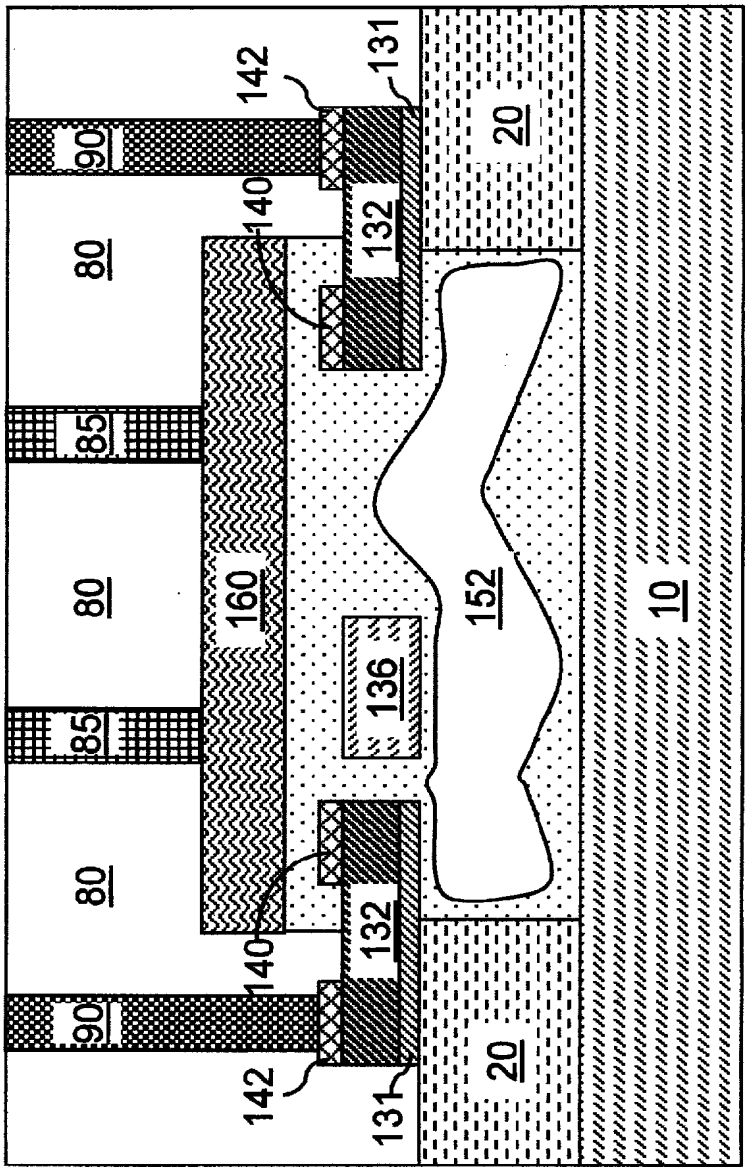
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FIG. 21

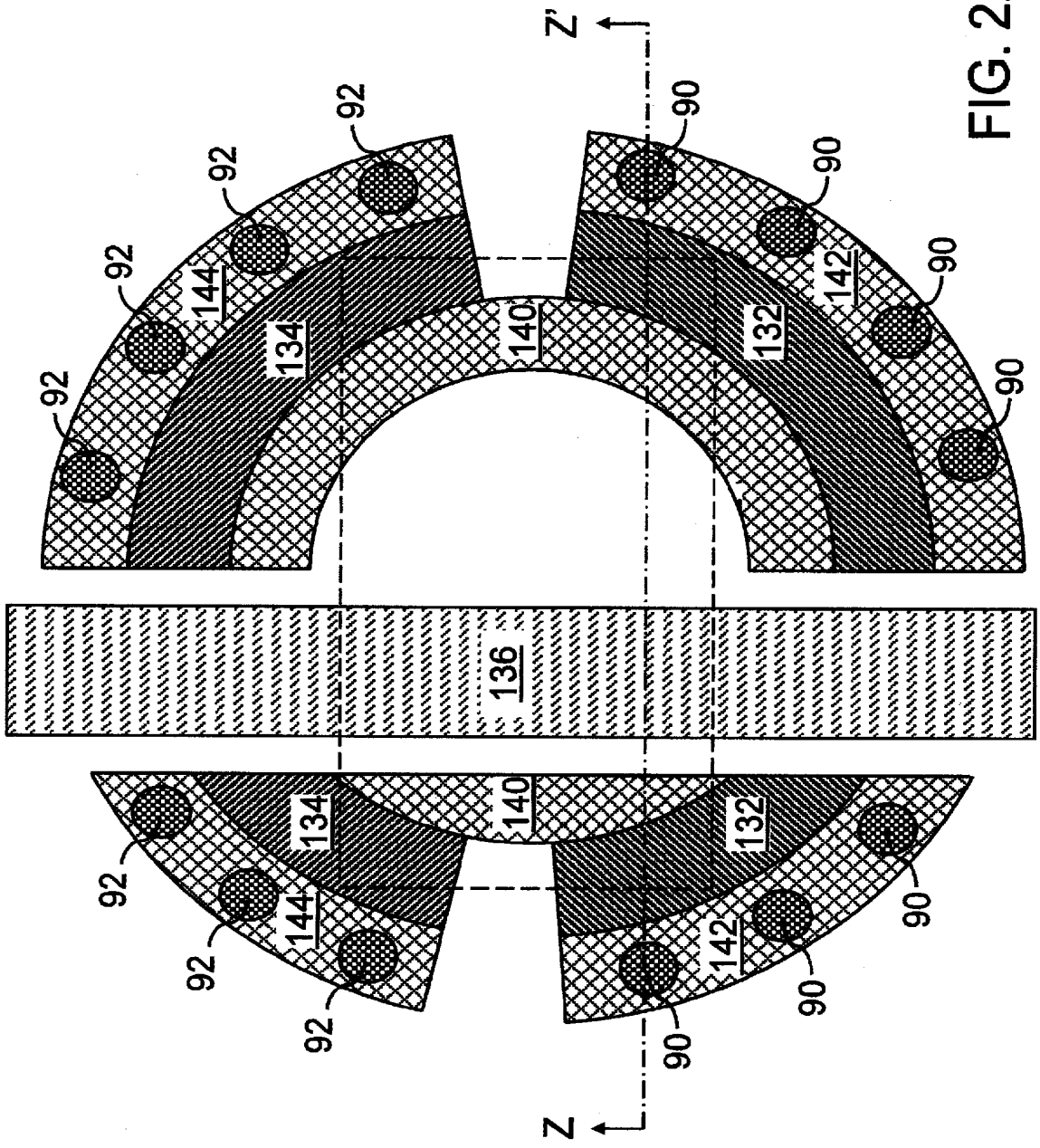

FIG. 22

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2010/059571

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L31/105 H01L31/18 H01L35/30 H01L23/38 G02B6/42
G02F1/01 G02F1/025
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L G02B G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 970 611 B1 (VAN DER VLIET FREDERIK MARCEL [US] ET AL) 29 November 2005 (2005-11-29) column 3, line 18 - column 11, line 64; figures 1A-8F	1-20
X	GB 2 332 284 A (BOOKHAM TECHNOLOGY LTD [GB]) 16 June 1999 (1999-06-16) page 9, line 11 - page 11, line 25; figures 1-4	1-20
A	US 7 340 709 B1 (MASINI GIANLORENZO [US] ET AL) 4 March 2008 (2008-03-04) column 4, line 4 - column 8, line 34; figures 1-8b	1-20

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 October 2010	21/10/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Albrecht, Claus

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2010/059571

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005/207704 A1 (KEYSER THOMAS [US] ET AL) 22 September 2005 (2005-09-22) paragraph [0033] - paragraph [0050]; figures 1-8	1-20

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

SAMSUNG EX. 1002 - 1558/2862

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2010/059571

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6970611 B1	29-11-2005	NONE	
GB 2332284 A	16-06-1999	AU 745594 B2	21-03-2002
		AU 3718599 A	23-11-1999
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		WO 9957600 A1	11-11-1999
		JP 2002513952 T	14-05-2002
		US 6278822 B1	21-08-2001
US 7340709 B1	04-03-2008	NONE	
US 2005207704 A1	22-09-2005	NONE	

SAMSUNG EX. 1002 - 1559/2862

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
24 March 2011 (24.03.2011)

PCT

(10) International Publication Number
WO 2011/035188 A2

(51) International Patent Classification:
H01L 27/146 (2006.01) *H01L 27/148* (2006.01)

(21) International Application Number:
PCT/US2010/049375

(22) International Filing Date:
17 September 2010 (17.09.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/243,434 17 September 2009 (17.09.2009) US
61/311,004 5 March 2010 (05.03.2010) US
61/311,107 5 March 2010 (05.03.2010) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

(54) **Title**: PHOTOSENSITIVE IMAGING DEVICES AND ASSOCIATED METHODS

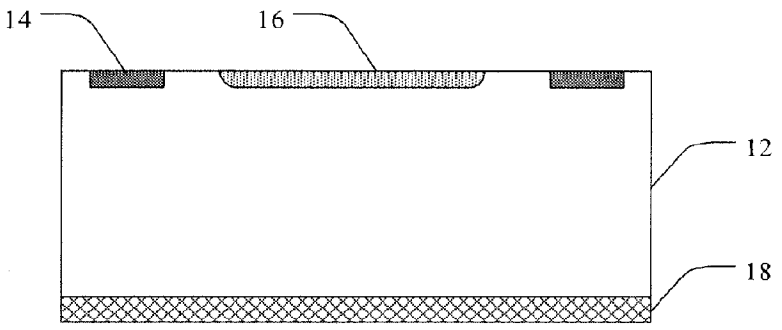

FIG. 1

(57) **Abstract**: Photosensitive devices and associated methods are provided. In one aspect, for example, a photosensitive imager device can include a semiconductor substrate having multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. In one aspect, the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation. In another aspect, interacting with electromagnetic radiation further includes increasing the semiconductor substrate's effective absorption wavelength as compared to a semiconductor substrate lacking a textured region.

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PHOTOSENSITIVE IMAGING DEVICES AND ASSOCIATED METHODS

PRIORITY DATA

This application claims the benefit of U.S. Provisional Patent Application Serial No. 61/243,434, filed on September 17, 2009, U.S. Provisional Patent Application Serial No. 61/311,004 filed on March 5, 2010, and U.S. Provisional Patent Application Serial No. 61/311,107, filed on March 5, 2010, each of which is incorporated herein by reference.

BACKGROUND

The interaction of light with semiconductor materials has been a significant innovation. Silicon imaging devices are used in various technologies, such as digital cameras, optical mice, video cameras, cell phones, and the like. Charge-coupled devices (CCDs) were widely used in digital imaging, and were later improved upon by complementary metal-oxide-semiconductor (CMOS) imagers having increased performance. CMOS sensors are typically manufactured from silicon and can covert visible incident light into a photocurrent and ultimately into a digital image. Silicon-based technologies for detecting infrared incident electromagnetic radiation have been problematic, however, because silicon is an indirect bandgap semiconductor having a bandgap of about 1.1eV. Thus the absorption of electromagnetic radiation having wavelengths of greater than about 1100 nm is, therefore, very low in silicon.

SUMMARY

The present disclosure provides photosensitive devices and associated methods. In one aspect, for example, a photosensitive imager device can include a semiconductor substrate having multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. In one aspect, the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation. In another aspect, interacting with electromagnetic radiation further includes increasing the semiconductor substrate's effective absorption length as compared to a semiconductor substrate lacking a textured region. In one specific aspect, the transfer

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element is selected from the group consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.

The textured region can be positioned in a variety of locations relative to the doped regions. In one aspect, for example, the textured region is positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions. In one specific aspect, the textured region has a surface morphology operable to direct electromagnetic radiation into or out of the semiconductor substrate. The surface morphology of the textured region relative to the semiconductor substrate can include a variety of configurations, including, without limitation, sloping, pyramidal, inverted pyramidal, spherical, parabolic, asymmetric, symmetric, and the like, including combinations thereof.

In another aspect, the textured region can be positioned on a surface of the semiconductor substrate that is adjacent the multiple doped regions. In a more specific aspect, an additional textured region can be positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions. In this manner, textured regions can thus be positioned adjacent to multiple doped regions and opposite the multiple doped regions.

Various aspects of the textured region can vary depending on the desired configuration of the device. In one aspect, however, the textured region includes surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof. Numerous surface feature morphologies are contemplated, nonlimiting examples of which include cones, pillars, pyramids, micolenses, quantum dots, inverted features, and combinations thereof. Additionally, the textured region can be formed by a variety of processes. Nonlimiting examples of such texturing processes can include lazing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, and combinations thereof.

Additional layers and/or structures can be included in various devices according to aspects present disclosure. In one aspect, for example, a reflective layer can be coupled to the semiconductor substrate and positioned to maintain the electromagnetic radiation in the semiconductor substrate. In another aspect, a lens can be optically coupled to the semiconductor substrate and positioned to focus incident electromagnetic radiation into the semiconductor substrate.

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In another aspect of the present disclosure, a method of making a photosensitive imager device is provided. Such a method can include forming a textured region on a semiconductor substrate having multiple doped regions forming a least one junction, wherein the textured region is formed in a position to interact with electromagnetic radiation and coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction.

In one aspect, the photosensitive imager device can be tuned to be selected to filter out specific electromagnetic radiation wavelengths. In one specific aspect, tuning includes forming surface features to have dimensions that selectively diffuse or selectively absorb a desired wavelength of electromagnetic radiation. In another aspect, tuning is accomplished through a factor selected from the group consisting of placement of the textured region, material type and/or thickness of the textured region, dopant type of the textured region, doping profile of the texture region, dopant profile of the semiconductor substrate, material type and/or thickness of the semiconductor substrate, and combinations thereof.

In another aspect of the present disclosure, a photosensitive imager device is provided. Such a device can include a semiconductor substrate having multiple doped regions forming a least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and at least 4 transistors coupled to the semiconductor substrate and with at least one of the transistors electrically coupled to the at least one junction.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic view of a photosensitive device in accordance with one aspect of the present disclosure;

FIG. 2 is a schematic view of a photosensitive device in accordance with another aspect of the present disclosure;

FIG. 3 is a schematic view of a photosensitive device in accordance with yet another aspect of the present disclosure;

FIG. 4 is a schematic view of a photosensitive device in accordance with a further aspect of the present disclosure;

FIG. 5 is a schematic view of a photosensitive device in accordance with yet a further aspect of the present disclosure;

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FIG. 6 is a schematic view of a photosensitive device in accordance with another aspect of the present disclosure;

FIG. 7 is a schematic view of a photosensitive pixel device in accordance with yet another aspect of the present disclosure;

FIG. 8 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

FIG. 9 is a schematic view of a photosensitive pixel device in accordance with yet a further aspect of the present disclosure;

FIG. 10 is a schematic view of a photosensitive pixel device in accordance with another aspect of the present disclosure;

FIG. 11 is a schematic view of a photosensitive pixel device in accordance with yet another aspect of the present disclosure;

FIG. 12 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

FIG. 13 is a schematic view of a photosensitive pixel device in accordance with another aspect of the present disclosure;

FIG. 14 is a schematic view of a photosensitive imager device in accordance with yet another aspect of the present disclosure;

FIG. 15 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

FIG. 16 is a schematic view of a photosensitive pixel device in accordance with another aspect of the present disclosure; and

FIG. 17 is a depiction of a method of making a photosensitive imager device in accordance with yet another aspect of the present disclosure.

DETAILED DESCRIPTION

Before the present disclosure is described herein, it is to be understood that this disclosure is not limited to the particular structures, process steps, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting.

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Definitions

The following terminology will be used in accordance with the definitions set forth below.

It should be noted that, as used in this specification and the appended claims, the singular forms "a," and, "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a dopant" includes one or more of such dopants and reference to "the layer" includes reference to one or more of such layers.

As used herein, the term "low oxygen content" refers to any material having an interstitial oxygen content that is less than or equal to about 60 ppm atomic.

As used herein, the terms "disordered surface" and "textured surface" can be used interchangeably, and refer to a surface having a topology with nano- to micron-sized surface variations formed by the irradiation of laser pulses. While the characteristics of such a surface can be variable depending on the materials and techniques employed, in one aspect such a surface can be several hundred nanometers thick and made up of nanocrystallites (e.g. from about 10 to about 50 nanometers) and nanopores. In another aspect, such a surface can include micron-sized structures (e.g. about 2 μm to about 60 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 500 μm.

As used herein, the term "fluence" refers to the amount of energy from a single pulse of laser radiation that passes through a unit area. In other words, "fluence" can be described as the energy density of one laser pulse.

As used herein, the terms "surface modifying" and "surface modification" refer to the altering of a surface of a semiconductor material using laser radiation. In one specific aspect, surface modification can include processes using primarily laser radiation or laser radiation in combination with a dopant, whereby the laser radiation facilitates the incorporation of the dopant into a surface of the semiconductor material. Accordingly, in one aspect surface modification includes doping of a semiconductor material.

As used herein, the term "target region" refers to an area of a semiconductor material that is intended to be doped or surface modified using laser radiation. The target region of a semiconductor material can vary as the surface modifying process progresses. For example, after a first target region is doped or surface modified, a second target region may be selected on the same semiconductor material.

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As used herein, the term "detection" refers to the sensing, absorption, and/or collection of electromagnetic radiation.

As used herein, the term "substantially" refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is "substantially" enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use of "substantially" is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is "substantially free of" particles would either completely lack particles, or so nearly completely lack particles that the effect would be the same as if it completely lacked particles. In other words, a composition that is "substantially free of" an ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

As used herein, the term "about" is used to provide flexibility to a numerical range endpoint by providing that a given value may be "a little above" or "a little below" the endpoint.

As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of "about 1 to about 5" should be interpreted to include

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not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

The Disclosure

Electromagnetic radiation can be present across a broad wavelength range, including visible range wavelengths (approximately 350nm to 800nm) and non-visible wavelengths (longer than about 800nm or shorter than 350 nm). The infrared spectrum is often described as including a near infrared portion of the spectrum including wavelengths of approximately 800 to 1300 nm, a short wave infrared portion of the spectrum including wavelengths of approximately 1300 nm to 3 micrometers, and a mid to long wave infrared (or thermal infrared) portion of the spectrum including wavelengths greater than about 3 micrometers up to about 30 micrometers. These are generally and collectively referred to herein as "infrared" portions of the electromagnetic spectrum unless otherwise noted.

Traditional silicon photodetecting imagers have limited light absorption/detection properties. For example, infrared light is mostly transparent to such silicon based detectors. While other materials (e.g. InGaAs) can be used to detect infrared electromagnetic radiation having wavelengths greater than about 1000 nm, silicon is still commonly used because it is relatively cheap to manufacture and can be used to detect wavelengths in the visible spectrum (i.e. visible light, 350 nm – 800 nm). Traditional silicon materials require substantial absorption depths to detect photons having wavelengths longer than approximately 700 nm. While visible light can be absorbed at relatively shallow depths in silicon, absorption of longer wavelengths (e.g. 900 nm) in silicon of a standard wafer depth (e.g. approximately 750 μm) is poor if at all. The devices of the present disclosure increase the absorption of semiconductor materials by decreasing the effective absorption length to longer wavelengths as compared to traditional materials. For example, the absorption depth of silicon can be reduced such that these longer wavelengths can be absorbed at depths of less than or equal to about 850 μm. In other words, by decreasing the

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effective absorption length these devices are able to absorb longer wavelengths (e.g. >1000 nm for silicon) within a thin semiconductor material. In addition to increasing the effective absorption length, the response rate or response speed can also be increased using thinner semiconductor materials.

The present disclosure additionally provides broadband photosensitive diodes, pixels, and imagers capable of detecting visible as well as infrared electromagnetic radiation, including associated methods of making such devices. A photosensitive diode can include a semiconductor substrate having multiple doped regions forming at least one junction, and at least one textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation. In one aspect the multiple doped regions can include at least one cathode region and at least one anode region. In some aspects, doped regions can include an n-type dopant and/or a p-type dopant as is discussed below, thereby creating a p-n junction. In other aspects, a photosensitive device can include an i-type region to form a p-i-n junction.

A photosensitive pixel can include a semiconductor substrate having multiple doped regions forming at least one junction, at least one textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. A photosensitive imager can include multiple photosensitive pixels. Additionally, an electrical transfer element can include a variety of devices, including without limitation, transistors, sensing nodes, transfer gates, transfer electrodes, and the like.

Photosensitive or photodetecting imagers include photodiodes or pixels that are capable of absorbing electromagnetic radiation within a given wavelength range. Such imagers can be passive pixel sensors (PPS), active pixel sensors (APS), digital pixel sensor imagers (DPS), or the like, with one difference being the image sensor read out architecture. For example, a semiconducting photosensitive imager can be a three or four transistor active pixel sensor (3T APS or 4T APS). Various additional components are also contemplated, and would necessarily vary depending on the particular configuration and intended results. As and example, a 4T configuration can additionally include, among other things, a transfer gate, a reset, a source follower, and row select transistors. Additionally, devices having greater than 4 transistors are also within the present scope.

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Photosensitive imagers can be front side illumination (FSI) or back side illumination (BSI) devices, and there are advantages and disadvantages to both architecture types. In a typical FSI imager, incident light enters the semiconductor device by first passing by transistors and metal circuitry. The light, however, can scatter off of the transistors and circuitry prior to entering the light sensing portion of the imager, thus causing optical loss and noise. A lens can be disposed on the topside of a FSI pixel to direct and focus the incident light to the light sensing active region of the device, thus partially avoiding the circuitry. In one aspect the lens can be a ulens. BSI imagers, one the other hand, are configured to have the depletion region of the junction extending to the opposite side of the device. In one aspect, for example, incident light enters the device via the light sensing portion and is mostly absorbed prior to reaching the circuitry. BSI designs allow for smaller pixel architecture and a high fill factor for the imager. As mentioned, the present disclosure can be adapted for either configuration. It should also be understood that devices according to aspects of the present disclosure can be incorporated into complimentary metal-oxide-semiconductor (CMOS) imager architectures or charge-coupled device (CCD) imager architectures.

In one aspect, as is shown in FIG. 1, a photosensitive diode 10 can include a semiconductor substrate 12 having multiple doped regions 14, 16 forming at least one junction, and at least one textured region 18 coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation. The different doped regions can have the same doping profile or different doping profiles, depending on the device. Such an architecture is a FSI design where light enters the semiconductor substrate from the direction of the multiple doped regions. While the device shown in FIG. 1 contains three doped regions, it should be noted that aspects containing one or more doped regions are considered to be within the present scope. Additionally, the semiconductor substrate can be doped, and thus can be considered to be a doped region in some aspects. It should also be noted that the photosensitive diode can be configured with a BSI architecture, and thus electromagnetic radiation would enter the semiconductor substrate from the direction of the textured region.

The various devices according to aspects of the present disclosure can exhibit increased quantum efficiency over traditional photosensitive devices. Any increase in the quantum efficiency makes a large difference in the signal to noise ratio. More complex structures can provide not only increased quantum efficiency but also good

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uniformity from pixel to pixel. In addition, devices of the present disclosure exhibit increased responsivity as compared to traditional photosensitive devices. For example, in one aspect the responsivity can be greater than or equal to 0.8A/W for wavelengths greater than 1000 nm for semiconductor substrate that is less than 100 μm thick.

Photosensitive imagers can be maintained under constant conditions (fixed voltage or current) to provide enhanced linearity and uniformity. Connections between the imager and the underlying device layers can be achieved using vias fabricated from a refractory metal, such as tungsten or tantalum. Placing storage elements under the imager may provide various photonic benefits. For example, the entire pixel array may be dedicated to signal processing. This may enable higher performance by permitting access to low level pixel signals. Furthermore, massively parallel operations can be performed by pixel processors. For example, analog to digital conversion, noise reduction (ie., true correlated double sampling), power conditioning, nearest neighbor pixel processing, compression, fusion, and color multiplexing operations can be performed.

A variety of semiconductor materials are contemplated for use with the devices and methods according to aspects of the present disclosure. Non-limiting examples of such semiconductor materials can include group IV materials, compounds and alloys comprised of materials from groups II and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can include silicon carbide (SiC) and silicon germanium (SiGe). In one specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum gallium arsenide, and combinations thereof.

Exemplary combinations of group II-VI materials can include cadmium selenide (CdSe), cadmium sulfide (CdS), cadmium telluride (CdTe), zinc oxide (ZnO), zinc selenide (ZnSe), zinc sulfide (ZnS), zinc telluride (ZnTe), cadmium zinc

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telluride (CdZnTe, CZT), mercury cadmium telluride (HgCdTe), mercury zinc telluride (HgZnTe), mercury zinc selenide (HgZnSe), and combinations thereof.

Exemplary combinations of group III-V materials can include aluminum antimonide (AlSb), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum phosphide (AlP), boron nitride (BN), boron phosphide (BP), boron arsenide (BAs), gallium antimonide (GaSb), gallium arsenide (GaAs), gallium nitride (GaN), gallium phosphide (GaP), indium antimonide (InSb), indium arsenide (InAs), indium nitride (InN), indium phosphide (InP), aluminum gallium arsenide (AlGaAs, $Al_xGa_{1-x}As$), indium gallium arsenide (InGaAs, $In_xGa_{1-x}As$), indium gallium phosphide (InGaP), aluminum indium arsenide (AlInAs), aluminum indium antimonide (AlInSb), gallium arsenide nitride (GaAsN), gallium arsenide phosphide (GaAsP), aluminum gallium nitride (AlGaN), aluminum gallium phosphide (AlGaP), indium gallium nitride (InGaN), indium arsenide antimonide (InAsSb), indium gallium antimonide (InGaSb), aluminum gallium indium phosphide (AlGaInP), aluminum gallium arsenide phosphide (AlGaAsP), indium gallium arsenide phosphide (InGaAsP), aluminum indium arsenide phosphide (AlInAsP), aluminum gallium arsenide nitride (AlGaAsN), indium gallium arsenide nitride (InGaAsN), indium aluminum arsenide nitride (InAlAsN), gallium arsenide antimonide nitride (GaAsSbN), gallium indium nitride arsenide antimonide (GaInNAsSb), gallium indium arsenide antimonide phosphide (GaInAsSbP), and combinations thereof.

The semiconductor material can be of any thickness that allows electromagnetic radiation detection and conversion functionality, and thus any such thickness of semiconductor material is considered to be within the present scope. In some aspects the laser processed region of the semiconductor increases the efficiency of the device such that the semiconductor material can be thinner than has previously been possible. Decreasing the thickness of the semiconductor reduces the amount of semiconductor material required to make such a device. In one aspect, for example, the semiconductor material has a thickness of from about 500 nm to about 50 μm. In another aspect, the semiconductor material has a thickness of less than or equal to about 500 μm. In yet another aspect, the semiconductor material has a thickness of from about 1 μm to about 10 μm. In a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 750 μm. In yet a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 100 μm.

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Additionally, various types of semiconductor material are contemplated, and any such material that can be incorporated into an electromagnetic radiation detection device is considered to be within the present scope. In one aspect, for example, the semiconductor material is monocrystalline. In another aspect, the semiconductor material is multicrystalline. In yet another aspect, the semiconductor material is microcrystalline. It is also contemplated that the semiconductor material can be amorphous. Specific nonlimiting examples include amorphous silicon or amorphous selenium.

The semiconductor materials of the present disclosure can also be made using a variety of manufacturing processes. In some cases the manufacturing procedures can affect the efficiency of the device, and may be taken into account in achieving a desired result. Exemplary manufacturing processes can include Czochralski (Cz) processes, magnetic Czochralski (mCz) processes, Float Zone (FZ) processes, epitaxial growth or deposition processes, and the like. Whether or not low oxygen content is desired in the device can also affect the choice of a manufacturing process for the semiconductor material. Various processes produce semiconductor materials containing varying amounts of oxygen, and as such, some applications having more stringent tolerances with respect to oxygen levels may benefit more from specific manufacturing procedures as compared to others. For example, during CZ crystal growth oxygen from the containment vessel, usually a quartz crucible, can become incorporated into the crystal as it is pulled. Additionally, other sources of oxygen contamination are also possible with the CZ process. Such contamination may be reduced, however, through the use of non oxygen-containing crucible materials, as well as the development of other crystal growth methods that do not utilize a crucible. One such process is the FZ process.

Materials grown with the CZ method can also be made to have lowered oxygen concentration through enhancements to the crystal growth process, such as growing the crystal in the presence of a magnetic field (i.e. the mCz process). Also, gettering techniques can be employed to reduce the impact of oxygen or other impurities on the finished device. These gettering techniques can include thermal cycles to liberate or nucleate impurities, or selective ion implantation of species to serve as gettering sites for the impurities. For example, oxygen concentrated in the semiconductor can be removed by the performing a furnace cycle to form a denuded zone. During heating with an inert gas, oxygen near the surface of the semiconductor

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diffuses out of the material. During the furnace cycle but after the denuding step, nucleating and growing steps may be performed. Nucleating sites for precipitates are formed during the nucleating step, and the precipitates are grown from the nucleating sites during a growing step. The precipitates are formed from interstitial oxygen within the bulk of the semiconductor material and beneath the denuded zone. The precipitation of oxygen in the bulk of the semiconductor material can be desired because such precipitates can act as gettering sites. Such precipitate formation can also be performed to "lock up" interstitial oxygen into the precipitates and reduce the likelihood that such oxygen can migrates from the bulk of the semiconductor material into the denuded zone.

In those aspects where low oxygen content of the device is desired, further processing of the semiconductor material can be performed so as to minimize the introduction of oxygen. Oxygen can exist in different states or at different sites (for example, interstitially or substitutionally) within a semiconductor such as silicon, dependent upon the thermal processing the semiconductor has received. If the semiconductor is subjected to temperatures higher than, for example, about 1000° C, oxygen can form aggregates or clusters that serve as defect sites in the crystal lattice. These sites may result in trap states and a reduction in carrier lifetime within the semiconductor material and device can occur. At lower temperatures (for example, around 400° C to 700° C), oxygen can behave as electrically active thermal donors. Thus, oxygen can have a negative impact on carrier lifetime and on carrier mobility. In a device fabricated to have photoconductive gain, the presence of oxygen causing reduced carrier lifetime may result in reduced levels of photoconductive gain.

It may be beneficial, therefore, to produce semiconductor devices such that a low oxygen content is obtained or maintained. This can be accomplished in a variety of ways, including using semiconductor materials having low levels of oxygen contained therein to begin with, processing these materials in a manner that minimizes the uptake of oxygen into the semiconductor lattice, and utilizing techniques that eliminate or reduce oxygen that may be present in the semiconductor. Such processes and techniques can include, for example, annealing the semiconductor material and any laser treated region to lower temperatures as compared to previous annealing procedures. Annealing processes are discussed more fully below.

Additionally, texture processing of the semiconductor material and/or any annealing process can be performed in a substantially oxygen-depleted environment

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in order to minimize the introduction of oxygen into the semiconductor. An oxygen-depleted or substantially oxygen-depleted environment can include a variety of environments. In one aspect, for example, the oxygen-depleted environment can be an environment whereby oxygen from the air or other sources has been replaced with a gas or other fluid containing little to no oxygen. In another aspect, processing can occur in a vacuum environment, and thus contain little to no oxygen. Additionally, oxygen-containing materials or materials that introduce oxygen into the semiconductor, such as, for example, quartz crucibles, can be avoided. As a practical matter, the term "oxygen-depleted environment" can be used to describe an environment with low levels of oxygen, provided a semiconductor material can be processed therein within the desired tolerances. Thus, environments having low oxygen, or little to no oxygen, are environments in which a semiconductor can be processed as a low-oxygen content semiconductor while maintaining oxygen levels within the tolerances of the present disclosure. In one aspect, an oxygen-depleted environment can be an oxygen-free environment. Further details regarding low-oxygen content semiconductor materials can be found in US Patent Application No. 12/771848, filed on April 30, 2010, which is incorporated herein by reference.

The semiconductor material can have varying levels of interstitial oxygen depending on the desired efficiency of the device. In some aspects, oxygen content may be of no concern, and thus any level of oxygen within the lattice is acceptable. In other aspects, a low oxygen content is desired. In one aspect a semiconductor material can have an oxygen content that is less than or equal to about 50 ppm atomic. In another aspect, a semiconductor material can have an oxygen content that is less than or equal to about 30 ppm atomic. In yet another aspect, the semiconductor material can have an oxygen content less than or equal to about 10 ppm atomic. In another aspect the semiconductor can have an oxygen content less than about 5 ppm atomic. In yet another aspect the semiconductor can have an oxygen content less than about 1 ppm atomic.

As has been described, the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device. The textured region can include surface features to increase the effective absorption length of the photosensitive pixel. The surface features can be cones, pyramids, pillars, protrusions, microlenses, quantum dots, inverted features and the like. Factors such

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as manipulating the feature sizes, dimensions, material type, dopant profiles, texture location, etc. can allow the diffusing region to be tunable for a specific wavelength. In one aspect, tuning the device can allow specific wavelengths or ranges of wavelengths to be absorbed. In another aspect, tuning the device can allow specific wavelengths or ranges of wavelengths to be reduced or eliminated via filtering.

Tuning can also be accomplished through the location of the texture region within the device, modifying the dopant profile(s) of regions within the device, dopant selection, and the like. Additionally, material composition near the textured region can create a wavelength specific photosensing pixel device. It should be noted that a wavelength specific photosensing pixel can differ from one pixel to the next, and can be incorporated into an imaging array. For example a 4 x 4 array can include a blue pixel, a green pixel, a red pixel, and infrared light absorbing pixel, or a blue pixel, two green pixels, and a red pixel.

Textured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared). Such internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor substrate. This increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.

The textured region can be formed by various techniques, including lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, additional material deposition, and the like. For example, pillar features can be incorporated into pixels by thinning or removing material from the backside of a FSI semiconductor substrate by using deep trench isolation and etching techniques. In one aspect material can be removed to a thickness of about 20 μm. Anisotropic etching can be used to produce a sloping backside pyramid structure, spherical, structure parabolic structure , a lens structure with reflectors, and the like. Such features on the backside of pillars will also serve to diffuse and reflect electromagnetic radiation.

In one aspect, the texturing process can be performed during the manufacture of the photosensitive device. In another aspect, the texturing process can be performed on a photosensitive device that has previously been made. For example, a CMOS, CCD, or other photosensitive element can be textured following manufacture. In this case, material layers may be removed from the photosensitive element to

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expose the semiconductor substrate or bulk material upon which a textured region may be formed.

One effective method of producing a textured region is through laser processing. Such laser processing allows discrete locations of the semiconductor substrate to be textured. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope. Laser treatment or processing can allow, among other things, enhanced absorption properties and thus increased electromagnetic radiation focusing and detection. The laser treated region can be associated with the surface nearest the impinging electromagnetic radiation, or the laser treated surface can be associated with a surface opposite in relation to impinging electromagnetic radiation, thereby allowing the radiation to pass through the semiconductor material before it hits the laser treated region.

In one aspect, for example, a target region of the semiconductor material can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Patents 7,057,256, 7,354,792 and 7,442,629, which are incorporated herein by reference in their entireties. Briefly, a surface of a semiconductor material is irradiated with laser radiation to form a textured or surface modified region. Such laser processing can occur with or without a dopant material. In those aspects whereby a dopant is used, the laser can be directed through a dopant carrier and onto the semiconductor surface. In this way, dopant from the dopant carrier is introduced into the target region of the semiconductor material. Such a region incorporated into a semiconductor material can have various benefits in accordance with aspects of the present disclosure. For example, the target region typically has a textured surface that increases the surface area of the laser treated region and increases the probability of radiation absorption via the mechanisms described herein. In one aspect, such a target region is a substantially textured surface including micron-sized and/or nano-sized surface features that have been generated by the laser texturing. In another aspect, irradiating the surface of semiconductor material includes exposing the laser radiation to a dopant such that irradiation incorporates the dopant into the semiconductor. Various dopant materials are known in the art, and are discussed in more detail herein.

Thus the surface of the semiconductor material is chemically and/or structurally altered by the laser treatment, which may, in some aspects, result in the

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formation of surface features appearing as microstructures or patterned areas on the surface and, if a dopant is used, the incorporation of such dopants into the semiconductor material. In some aspects, the features or microstructures can be on the order of 50 nm to 20 μm in size and can assist in the absorption of electromagnetic radiation. In other words, the textured surface can increase the probability of incident radiation being absorbed by the semiconductor material.

The type of laser radiation used to surface modify a semiconductor material can vary depending on the material and the intended modification. Any laser radiation known in the art can be used with the devices and methods of the present disclosure. There are a number of laser characteristics, however, that can affect the surface modification process and/or the resulting product including, but not limited to the wavelength of the laser radiation, pulse width, pulse fluence, pulse frequency, polarization, laser propagation direction relative to the semiconductor material, etc. In one aspect, a laser can be configured to provide pulsatile lasing of a semiconductor material. A short-pulsed laser is one capable of producing femtosecond, picosecond and/or nanosecond pulse durations. Laser pulses can have a central wavelength in a range of about from about 10 nm to about 8 μm, and more specifically from about 200 nm to about 1200 nm. The pulse width of the laser radiation can be in a range of from about tens of femtoseconds to about hundreds of nanoseconds. In one aspect, laser pulse widths can be in the range of from about 50 femtoseconds to about 50 picoseconds. In another aspect, laser pulse widths can be in the range of from about 50 picoseconds to 100 nanoseconds. In another aspect, laser pulse widths are in the range of from about 50 to 500 femtoseconds.

The number of laser pulses irradiating a target region can be in a range of from about 1 to about 2000. In one aspect, the number of laser pulses irradiating a semiconductor target region can be from about 2 to about 1000. Further, the repetition rate or frequency of the pulses can be selected to be in a range of from about 10 Hz to about 10 μHz, or in a range of from about 1 kHz to about 1 MHz, or in a range from about 10 Hz to about 1 kHz. Moreover, the fluence of each laser pulse can be in a range of from about 1 kJ/m^2 to about 20 kJ/m^2, or in a range of from about 3 kJ/m^2 to about 8 kJ/m^2.

A variety of dopant materials are contemplated, and any such material that can be used in the laser treatment process to surface modify a semiconductor material according to aspects of the present disclosure is considered to be within the present

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scope. It should be noted that the particular dopant utilized can vary depending on the semiconductor material being laser treated, as well as the intended use of the resulting semiconductor material. For example, the selection of potential dopants may differ depending on whether or not tuning of the photosensitive device is desired.

A dopant can be either electron donating or hole donating. In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof. It should be noted that the scope of dopant materials should include, not only the dopant materials themselves, but also materials in forms that deliver such dopants (i.e. dopant carriers). For example, S dopant materials includes not only S, but also any material capable being used to dope S into the target region, such as, for example, H_2S, SF_6, SO_2, and the like, including combinations thereof. In one specific aspect, the dopant can be S. Sulfur can be present at an ion dosage level of between about 5×10^{14} and about 1×10^{16} ions/cm^2. Non-limiting examples of fluorine-containing compounds can include ClF_3, PF_5, F_2 SF_6, BF_3, GeF_4, WF_6, SiF_4, HF, CF_4, CHF_3, CH_2F_2, CH_3F, C_2F_6, C_2HF_5, C_3F_8, C_4F_8, NF_3, and the like, including combinations thereof. Non-limiting examples of boron-containing compounds can include $B(CH_3)_3$, BF_3, BCl_3, BN, $C_2B_{10}H_{12}$, borosilica, B_2H_6, and the like, including combinations thereof. Non-limiting examples of phosphorous-containing compounds can include PF_5, PH_3, and the like, including combinations thereof. Non-limiting examples of chlorine-containing compounds can include Cl_2, SiH_2Cl_2, HCl, $SiCl_4$, and the like, including combinations thereof. Dopants can also include arsenic-containing compounds such as AsH_3 and the like, as well as antimony-containing compounds. Additionally, dopant materials can include mixtures or combinations across dopant groups, i.e. a sulfur-containing compound mixed with a chlorine-containing compound. In one aspect, the dopant material can have a density that is greater than air. In one specific aspect, the dopant material can include Se, H_2S, SF_6, or mixtures thereof. In yet another specific aspect, the dopant can be SF_6 and can have a predetermined concentration range of about 5.0×10^{-8} mol/cm^3 to about 5.0×10^{-4} mol/cm^3. SF_6 gas is a good carrier for the incorporation of sulfur into the semiconductor material via a laser process without significant adverse effects on the semiconductor material. Additionally, it is noted that dopants can also be liquid solutions of n-type or p-type dopant materials dissolved in a solution such as water, alcohol, or an acid or basic solution. Dopants can also be solid materials applied as a powder or as a suspension dried onto the wafer.

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The semiconductor substrate can be annealed for a variety of reasons, including dopant activation, semiconductor material damage repair, and the like. In those aspects including a laser textured region, the semiconductor material can be annealed prior to laser treatment, following laser treatment, during laser treatment, or both prior to and following laser treatment. Annealing can enhance the semiconductive properties of the device, including increasing the photoresponse properties of the semiconductor materials. Additionally, annealing can reduce damage done by the lasing process. Although any known anneal can be beneficial and would be considered to be within the present scope, annealing at lower temperatures can be particularly useful. Such a "low temperature" anneal can greatly enhance the photoconductive gain and external quantum efficiency of devices utilizing such materials. In one aspect, for example, the semiconductor material can be annealed to a temperature of from about 300° C to about 1100 C°. In another aspect, the semiconductor material can be annealed to a temperature of from about 500° C to about 900° C. In yet another aspect, the semiconductor material can be annealed to a temperature of from about 700° C to about 800° C. In a further aspect, the semiconductor material can be annealed to a temperature that is less than or equal to about 850° C.

The duration of the annealing procedure can vary according to the specific type of anneal being performed, as well as according to the materials being used. For example, rapid annealing processes can be used, and as such, the duration of the anneal may be shorter as compared to other techniques. Various rapid thermal anneal techniques are known, all of which should be considered to be within the present scope. In one aspect, the semiconductor material can be annealed by a rapid annealing process for a duration of greater than or equal to about 1 μs. In another aspect, the duration of the rapid annealing process can be from about 1 μs to about 1 ms. As another example, a baking or furnace anneal process can be used having durations that may be longer compared to a rapid anneal. In one aspect, for example, the semiconductor material can be annealed by a baking anneal process for a duration of greater than or equal to about 1 ms to several hours. As has been described, if low oxygen content semiconductor materials are used it may be beneficial to anneal such materials in a substantially oxygen-depleted environment.

As has been described, annealing can help reduce defects inherent to the semiconductor substrate and otherwise reduce electron/hole recombination. In other

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words, the annealing can help create electron states that effectively reduce the undesirable recombination processes. Annealing the semiconductor material may also improve the responsivity or photoconductive gain of the device. Photoconductive devices can have dopants, impurities, or defects that can introduce energy levels that can trap carriers. Trapping carriers and reducing recombination of photocarriers can lead to an increase in photoconductive gain of the device. The relationship of photoconductive gain and trapping time can be represented by Equation (I):

$$\text{Gain} = \tau_L/\tau_t \qquad \text{(I)}$$

where "τ_L" is the lifetime of an excess carrier and "τ_t" is the transit time of the carriers across the device. It is understood that the lifetime of an excess carrier can be increased by trapping a carrier species and reducing the recombination rate. An increase in gain can be achieved by trapping centers in the semiconductor that have millisecond trapping times at room temperature and short transit times in thinned lightly doped wafers. These trapping locations can decrease the recombination of carriers and therefore improve or increase the photoconductive gain of the device by allowing more electrons to traverse the different regions without being recombined.

Turning to FIG. 2, a reflecting layer 20 can be coupled to the semiconductor substrate 12. The reflecting layer can be coupled to any side or portion of the semiconductor substrate in order to reflect electromagnetic radiation back into the device. Accordingly, in one aspect the reflecting layer can be located on the semiconductor substrate opposite the incoming electromagnetic radiation. Thus, as is shown in FIG. 2, electromagnetic radiation passing though the semiconductor substrate and the textured region 16 can be reflected back into the semiconductor substrate. Additionally, a passivation layer 22 can be coupled to the semiconductor substrate. The passivation layer is shown coupled to the side of the semiconductor substrate facing the incoming electromagnetic radiation, however a passivation layer can be located anywhere on the device and still be within the present scope.

As has been described, location of the textured region can be used to provide enhancement and/or filtering of the incoming electromagnetic radiation. For example, a textured region located at the point of entry of the electromagnetic radiation into the photosensitive device tends to bend the electromagnetic radiation, particularly the blue wavelengths. Accordingly, one level of tuning can be accomplished by locating

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the textured region on the surface adjacent the incident electromagnetic radiation to purposely effectuate the filtering of blue wavelengths. Additionally, absorption of particular wavelengths of electromagnetic radiation occurs at different depths in the semiconductor layer and/or textured region. By increasing the absorption to green wavelengths, for example, the electrical signal as a result of green wavelengths can be increased in a diode or pixel. Certain traditional 4 pixel imagers have one red, one blue, and two green pixels, with the greater number of green pixels to account for increased sensitivity of the human eye to green colors. Thus in one aspect, a 4 pixel imager can have one blue, one red, and one green pixel having an increased green wavelength absorption. The fourth pixel can be used for an IR or other wavelength selective pixel depending on the desired application of the imager.

FIG. 3 shows a photosensitive device having textured regions 30 located on the sides of the semiconductor substrate 12. Such a configuration allows electromagnetic radiation normally exiting through the sides of the device to be further defused and absorbed within semiconductor substrate. The textured region(s) can be located on one or more sides to facilitate the enhanced absorption.

FIG. 4 shows a photosensitive device having a textured region 40 having a nonparallel surface with respect to the semiconductor substrate 12. Thus the overall configuration of the textured region can be designed to further enhance absorption and/or selectively tune the device. As has been described, the nonparallel surface can have a variety of configurations, such as, without limitation, nonparallel slope, a pyramid, an inverted pyramid, a concave shape, a convex shape, and the like. In some cases the configuration of the textured region can function to direct or focus electromagnetic radiation into the semiconductor substrate, and in other cases the configuration of the textured region can function to direct or focus electromagnetic radiation away from the semiconductor substrate.

As is shown in FIG. 5, a lens 50 can be coupled to the semiconductor substrate 12 on a side facing incoming electromagnetic radiation. Thus the lens can focus the electromagnetic radiation into the semiconductor substrate. In those aspects having circuitry or other structures disposed on the incoming electromagnetic radiation surface, the lens can further focus light around such structures, thereby reducing optical scattering and noise.

As is shown in FIG. 6, a textured region 60 is located on the semiconductor substrate 12 adjacent to the multiple doped regions 14, 16. The textured region can be

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associated with at least one of the doped regions as is shown, or the textured region can be distinct from the doped regions (not shown). Electromagnetic radiation can enter the photosensitive device at the side adjacent the doped regions, or alternatively at the side opposite the doped regions.

FIGs. 7-11 show various steps in the manufacture of a photosensitive pixel according to aspects of the present disclosure. FIG. 7 shows a cross-section of a front side illumination (FSI) photosensitive pixel device. The photosensitive pixel device can include a semiconductor substrate 72, and can be referred to as bulk semiconductor material. The semiconductor substrate includes at least one doped region 74 that can be doped with an electron donating or hole donating species to cause the region to become more positive or negative in polarity as compared to the semiconductor substrate. In one aspect, for example, the doped region can be p doped. In another aspect the doped region can be n doped. A highly doped region 76 can be formed on or near the doped region to create a pinned diode. In one example, the semiconductor substrate can be negative in polarity, and the doped region and the highly doped region can be doped with p+ and n- dopants respectively. In some aspects, variations of n(--), n(-), n(+), n(++), p(--), p(-), p(+), or p(++) type doping of the regions can be used. It should be noted that in one aspect the highly doped region can be the textured region. In other words, textured surface features can be formed on or in the highly doped region.

The device of FIG. 7 can further include various metal regions 78, at least one via 80, a passivation layer 82, trench isolation 84, and an electrical transfer element 86. Trench isolation elements can maintain pixel to pixel uniformity by reducing optical and electrical crosstalk. The trench isolation can be shallow (FIG. 7) or deep (FIG. 12) trench isolation. The trench isolation can include various materials, including, without limitation, dielectric materials, reflective materials, conductive materials, light diffusing features, and the like. These trench isolation regions can be configured to reflect incident light until it is absorbed, thereby increase the effective absorption length of the device.

As is shown in FIG. 8, a carrier substrate or carrier wafer 88 can be coupled to the photosensing pixel. In one aspect, the carrier substrate can be disposed on the passivation layer 82, although the carrier substrate can be disposed on any surface of the device. In one aspect, for example, the carrier substrate can be disposed on the semiconductor substrate (not shown). The carrier substrate can be coupled to the

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photosensing pixel by various techniques, and any such coupling mechanism is within the present scope. In one aspect, for example, the coupling can occur by way of a bonding layer or adhesive layer disposed on the device, for example, on the passivation layer. The support substrate can provide support to the semiconductor device both during and after manufacture, depending on whether or not the support is removed. The carrier substrate can be made of a semiconductor material that is the same or similar to the bulk semiconductor material, or it can be made of a different material.

As is shown in FIG. 9, a textured region 90 is coupled to the semiconductor substrate 72 opposite the doped regions 74,76. Thus light entering from the direction of the doped regions passes through the semiconductor substrate prior to contacting the textured region. The textured region can be disposed across an entire surface of the semiconductor substrate, as is shown in FIG. 9, or it can be disposed on one or more discrete regions (not shown).

As is shown in FIG. 10, an additional carrier support substrate 100 can be coupled to the device on an opposing side from the carrier support substrate 88. The additional carrier support substrate can be utilized for a variety of purposes, including providing additional support to the device, facilitating the removal of the first carrier support substrate, and the like. A reflective layer 102 can be disposed between the textured region 90 and the carrier support substrate. Thus the reflective layer can reflect electromagnetic radiation that passes through the textured region back toward the semiconductor substrate 72, thus reducing optical loss and backscattering. Thus, in some aspects a reflective layer can increase the quantum efficiency of the device. The reflective layer material can be any reflective material that can be incorporated into such a device. Nonlimiting examples can include materials such as silver, aluminum, and the like.

As is shown in FIG. 11, the carrier support substrate can be removed to expose the passivation layer 82 or any other material layer that was previously covered by the carrier support substrate. The additional carrier substrate 100 can be maintained in the device, removed from the device, or thinned to reduce the thickness of the substrate depending on the intended use of the device. The removal of material from the device, including the carrier support substrate and the additional carrier substrate, can be accomplished by a variety of methods including, without limitation, etching, chemical mechanical polishing, ion implanting (i.e. smart cut), and the like.

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Various types of trench isolation are contemplated, and any such isolation is considered to be within the present scope. As has been described, trench isolation can be shallow (FIG. 7, 84) or deep (FIG. 12, 120) trench isolation. The trench isolation can also include depths between shallow and deep, depending on the device design. Trench isolation can include dielectric materials, reflective materials, conductive materials, and combinations thereof, including textured regions and other light diffusing features. Thus the trench isolation layer can be configured to reflect incident electromagnetic radiation, in some cases until it is absorbed, thereby increasing the effective absorption length of the device. Additionally, in some aspects pillar features can be incorporated into pixels by thinning or removing material from the semiconductor substrate using deep trench isolation and etching techniques. As is shown in FIG. 13, the textured region 130 can have a nonparallel surface with respect to the semiconductor substrate 72 as has been described. This nonparallel morphology, when included with the deep trench isolation 120, can effectively focus electromagnetic radiation into the semiconductor substrate from multiple sides.

It is also contemplated, that a non-bulk material can be formed or disposed near a doped region in the device. The addition of the non-bulk material can allow for electromagnetic radiation diffusing features to be formed on or in the non-bulk material. A metal layer defining an aperture can also be included in one aspect of the present disclosure. The metal layer can be formed near the doped regions and can have a light entering region that defines an aperture. This light entering region can also include an antireflecting material.

Fig. 14 shows a photosensitive imager comprising two photosensitive pixels 140. Each photosensitive pixel includes a boundary region 142 that can include metal circuitry and a textured region 144. Each photosensitive pixel can include at least one transistor 146 or other electrical transfer element. Additional read out and circuitry elements 148 can be utilized and shared by both photosensitive pixels.

Turning to FIG. 15, a backside illuminated (BSI) photosensitive pixel according to one aspect present disclosure is provided. A lens 150 and an anti-reflective coating 152 are disposed on the backside of the pixel following thinning and trench isolation. A color filter 154 can be optically coupled to the lens to allow specific wavelengths filtering of the electromagnetic radiation. A textured region 156 can be coupled to the semiconductor substrate 72 opposite the lens in order to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes

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through to the front side of the pixel. Thus the electromagnetic radiation can be focused within the semiconductor substrate to the combined action of the textured region and the trench isolation 120

Fig. 16 shows a front side illuminated (FSI) imager according to another aspect of the present disclosure. A lens 160 and an antireflecting passivation layer on 62 are coupled to the front side of the pixel. A textured region 90 and a reflecting layer 102 are coupled to the semiconductor substrate 72 opposite the lens to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes through the semiconductor substrate. An aperture 164 formed in a metal or other reflective material layer 166 can increase the effectiveness of the optical cavity. Thus the lens focuses electromagnetic radiation through the aperture.

In other aspects of the present disclosure, various methods of making photosensitive diodes, pixels, and imagers, are contemplated. In one aspect, as is shown in FIG. 17, a method of making a photosensitive imager device can include forming a textured region on a semiconductor substrate having multiple doped regions forming a least one junction, wherein the textured region is formed in a position to interact with electromagnetic radiation 170. The method also includes coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction 172. In one aspect, multiple pixels can be associated together to form an imager. A passivation layer can also be disposed on the photosensitive imager device to protect and/or reduce the dark current of the device.

In another aspect of the present disclosure, a method for making a photosensitive diode is provided. Such a method can include forming at least one cathode and at least one anode on a surface of a semiconductor substrate, coupling a textured region to the semiconductor substrate, and coupling a support substrate to the semiconductor substrate. The textured region can be located adjacent to the anode and cathode, opposite the anode and cathode, or both adjacent and opposite the anode and cathode. An electrical transfer on the can be electrically coupled to at least one of the anode and cathode to form a photosensitive pixel. In another aspect, the semiconductor substrate can be thinned to improve the response rate and/or speed of the device. A passivation layer can also be disposed on the photosensitive diode to protect and/or reduce the dark current of the device. An additional support substrate can be attached to the device to provide additional support. In one aspect, the

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additional support substrate can be located on the opposite side of the photosensitive diode from the support substrate. The support substrate can subsequently be removed to allow for further processing.

Of course, it is to be understood that the above-described arrangements are only illustrative of the application of the principles of the present disclosure. Numerous modifications and alternative arrangements may be devised by those skilled in the art without departing from the spirit and scope of the present disclosure and the appended claims are intended to cover such modifications and arrangements. Thus, while the present disclosure has been described above with particularity and detail in connection with what is presently deemed to be the most practical embodiments of the disclosure, it will be apparent to those of ordinary skill in the art that numerous modifications, including, but not limited to, variations in size, materials, shape, form, function and manner of operation, assembly and use may be made without departing from the principles and concepts set forth herein.

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CLAIMS

What is claimed is:

1. A photosensitive imager device, comprising:

a semiconductor substrate having multiple doped regions forming a least one junction;

a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation; and

an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction.

2. The device of claim 1, wherein the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation.

3. The device of claim 1, wherein interacting with electromagnetic radiation further includes increasing the semiconductor substrate's effective absorption length as compared to a semiconductor substrate lacking a textured region.

4. The device of claim 1, wherein the transfer element is selected from the group consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.

5. The device of claim 1, further comprising a reflective layer coupled to the semiconductor substrate and positioned to maintain the electromagnetic radiation in the semiconductor substrate.

6. The device of claim 1, wherein the textured region is positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions.

7. The device of claim 6, wherein the textured region has a surface morphology operable to direct electromagnetic radiation into or out of the semiconductor substrate.

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8. The device of claim 7, wherein the surface morphology of the textured region relative to the semiconductor substrate is a member selected from the group consisting of sloping, pyramidal, inverted pyramidal, spherical, parabolic, asymmetric, symmetric, and combinations thereof.

9. The device of claim 1, wherein the textured region is positioned on a surface of the semiconductor substrate that is adjacent the multiple doped regions.

10. The device of claim 9, further comprising an additional textured region positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions.

11. The device of claim 1, wherein the textured region is coupled directly to at least one of the multiple doped regions.

12. The device of claim 1, wherein the textured region includes surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof.

13. The device of claim 12, wherein surface features include a member selected from the group consisting of cones, pillars, pyramids, micolenses, quantum dots, inverted features, and combinations thereof.

14. The device of claim 1, wherein the textured region has been formed by a process selected from the group consisting of lazing, chemical etching, nanoimprinting, material deposition, and combinations thereof.

15. The device of claim 1, further comprising a lens optically coupled to the semiconductor substrate and positioned to focus incident electromagnetic radiation into the semiconductor substrate.

16. A photosensitive imager array, comprising at least two photosensitive imager devices of claim 1.

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17. The array of claim 16, further comprising at least one trench isolation positioned between the at least two photosensitive imager device.

18. A method of making a photosensitive imager device, comprising:

forming a textured region on a semiconductor substrate, wherein the semiconductor substrate has multiple doped regions forming a least one junction, and wherein the textured region is formed in a position to interact with electromagnetic radiation; and

coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction .

19. The method of claim 18, wherein forming the textured region is by a process selected from the group consisting of lazing, chemical etching, nanoimprinting, material deposition, and combinations thereof.

20. The method of claim 18, wherein forming the textured region includes irradiating a target region with laser radiation to form surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof.

21. The method of claim 20, wherein irradiating the target region includes exposing the laser radiation to a dopant such that the irradiation incorporates the dopant into the textured region.

22. The method of claim 20, wherein the irradiation is performed using a pulsed laser including a member selected from the group consisting of a femtosecond laser, a picosecond laser, a nanosecond laser, and combinations thereof.

23. The method of claim 18, further comprising tuning an electrical response of the photosensitive imager device.

24. The method of claim 23, wherein tuning includes forming surface features to have dimensions that selectively diffuse or selectively absorb a desired wavelength of electromagnetic radiation.

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25. The method of claim 23, wherein tuning is accomplished through a factor selected from the group consisting of placement of the textured region, material type of the textured region, thickness of the textured region, dopant type of the textured region, doping profile of the texture region, doping profile of the semiconductor substrate, thickness of the substrate, and combinations thereof.

26. The method of claim 18, wherein the transfer element is selected from the group consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.

27. The method of claim 18, further comprising annealing the semiconductor substrate to a temperature of from about 300° C to about 1100° C.

28. A photosensitive imager device, comprising:

a semiconductor substrate having multiple doped regions forming a least one junction;

a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation; and

at least 4 transistors coupled to the semiconductor substrate and with at least one of the transistors electrically coupled to the at least one junction.

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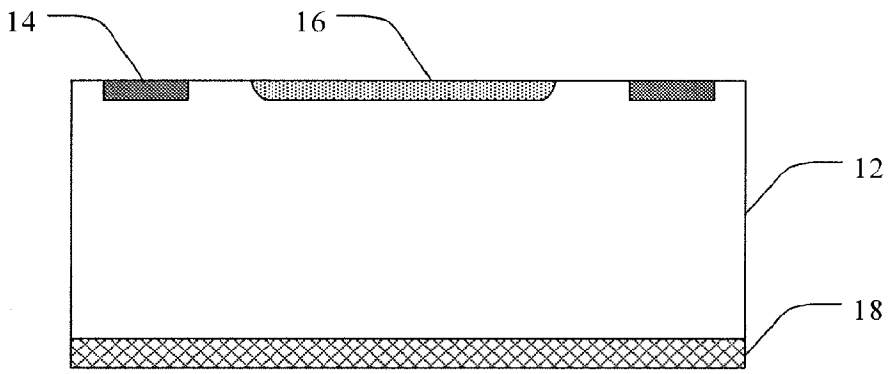

FIG. 1

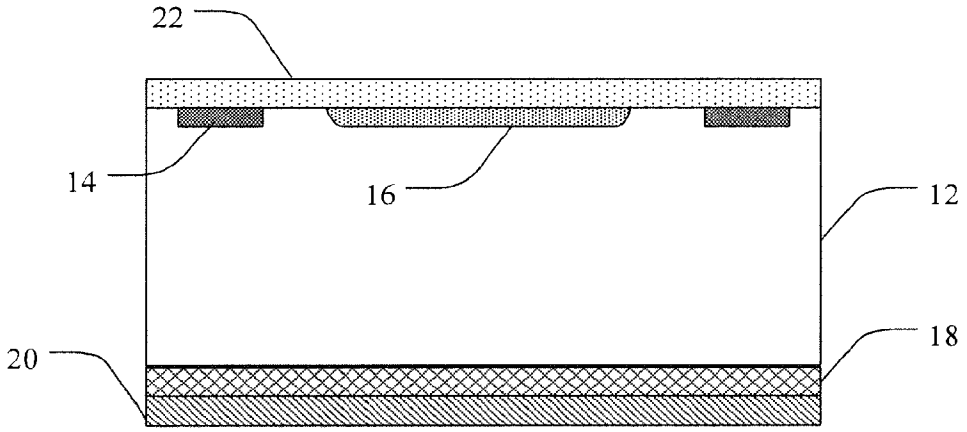

FIG. 2

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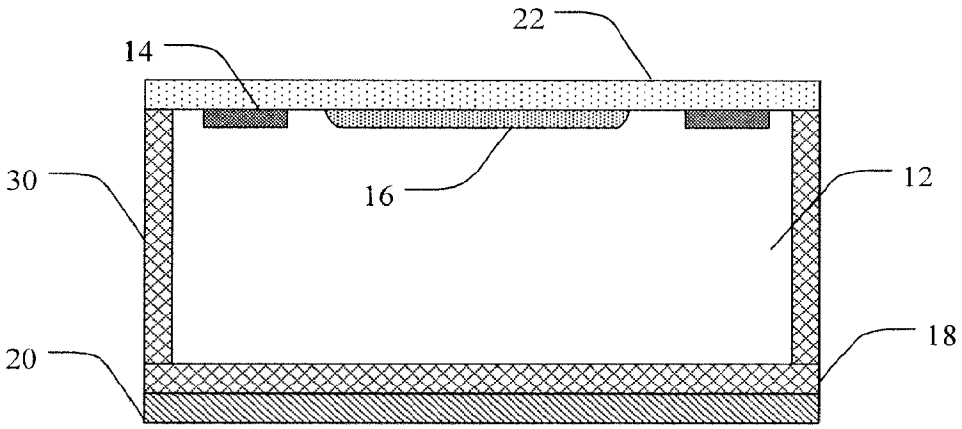

FIG. 3

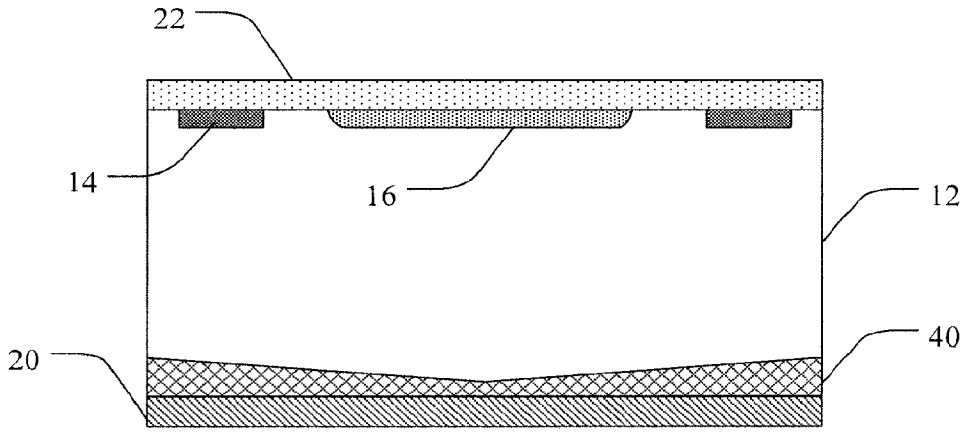

FIG. 4

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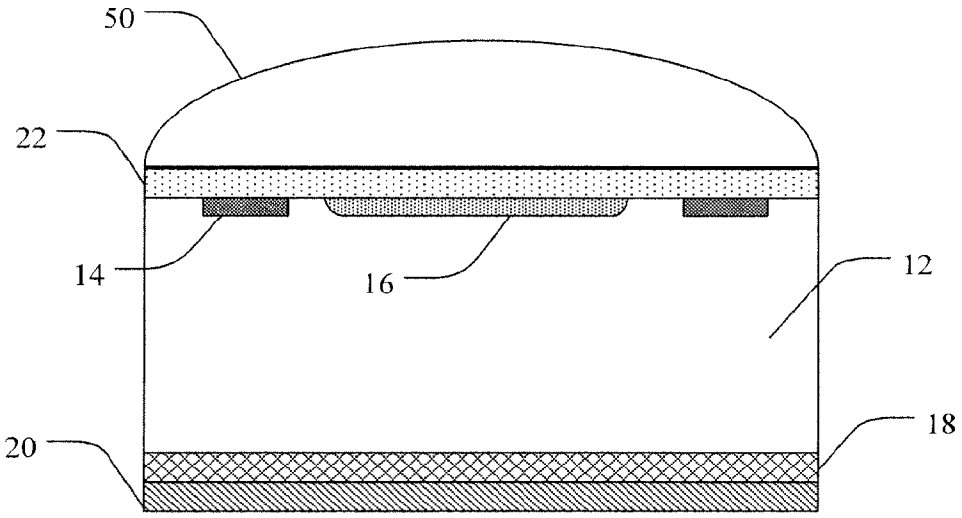

FIG. 5

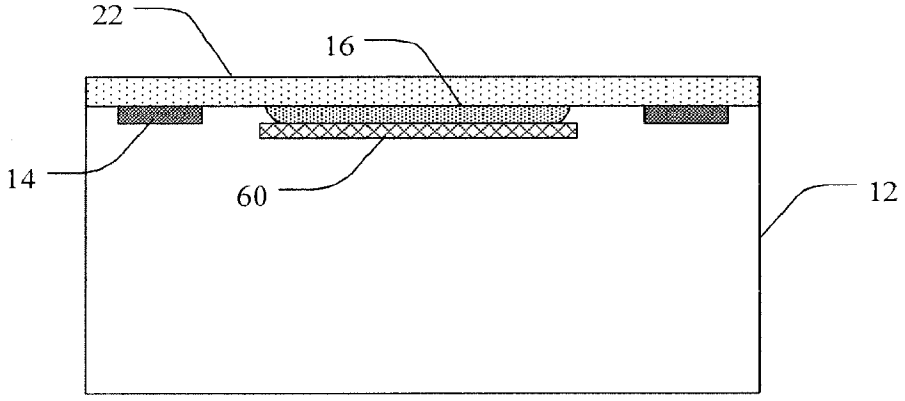

FIG. 6

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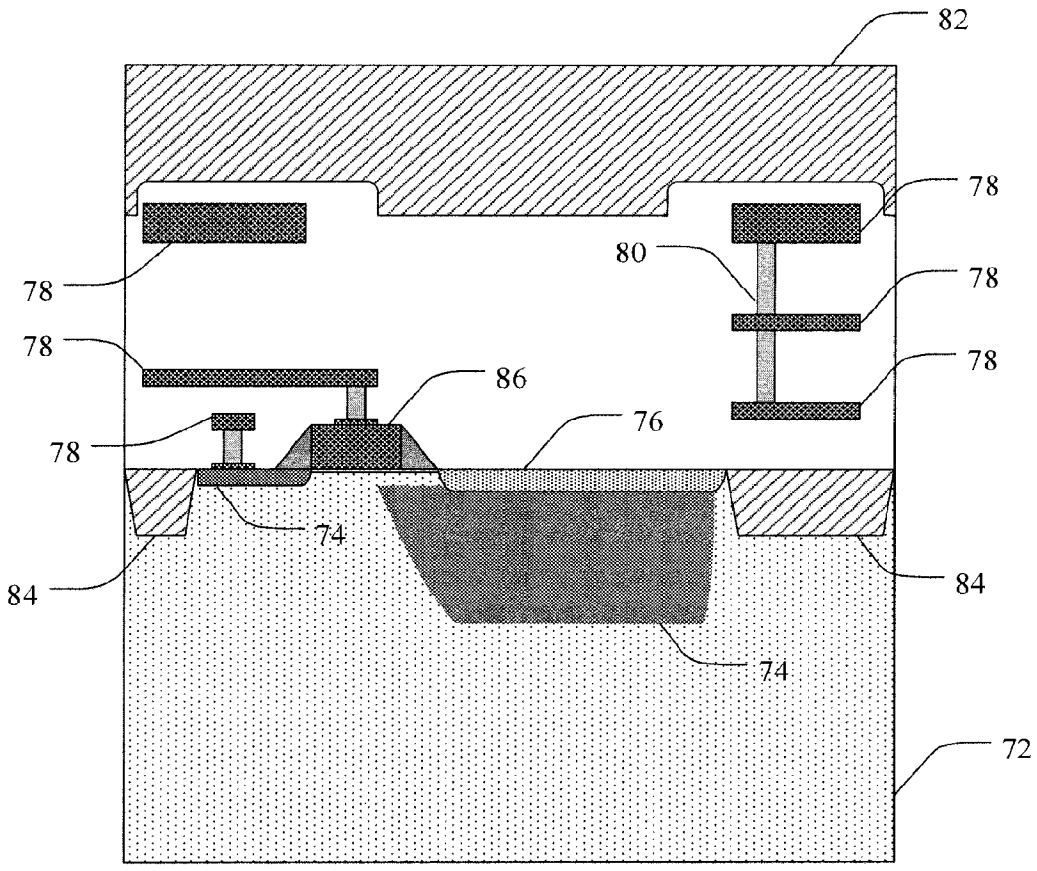

FIG. 7

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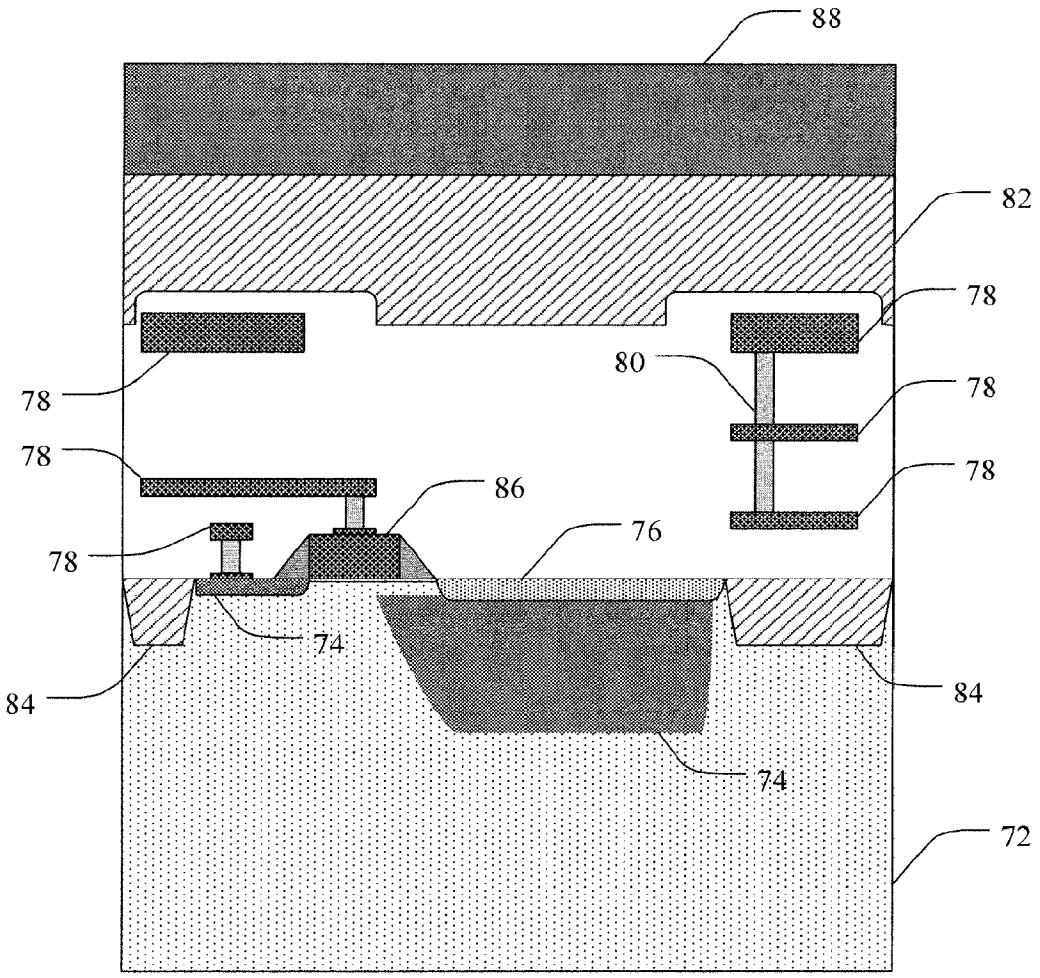

FIG. 8

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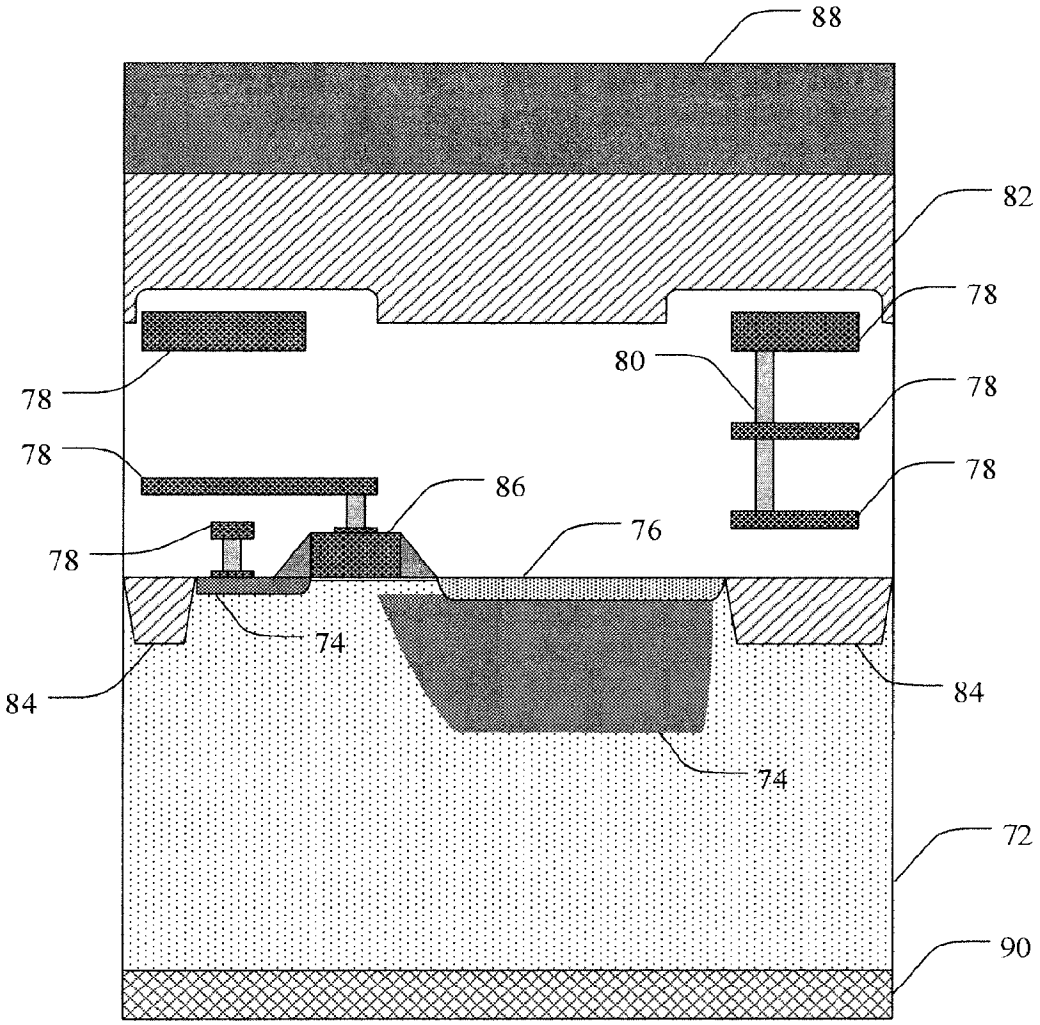

FIG. 9

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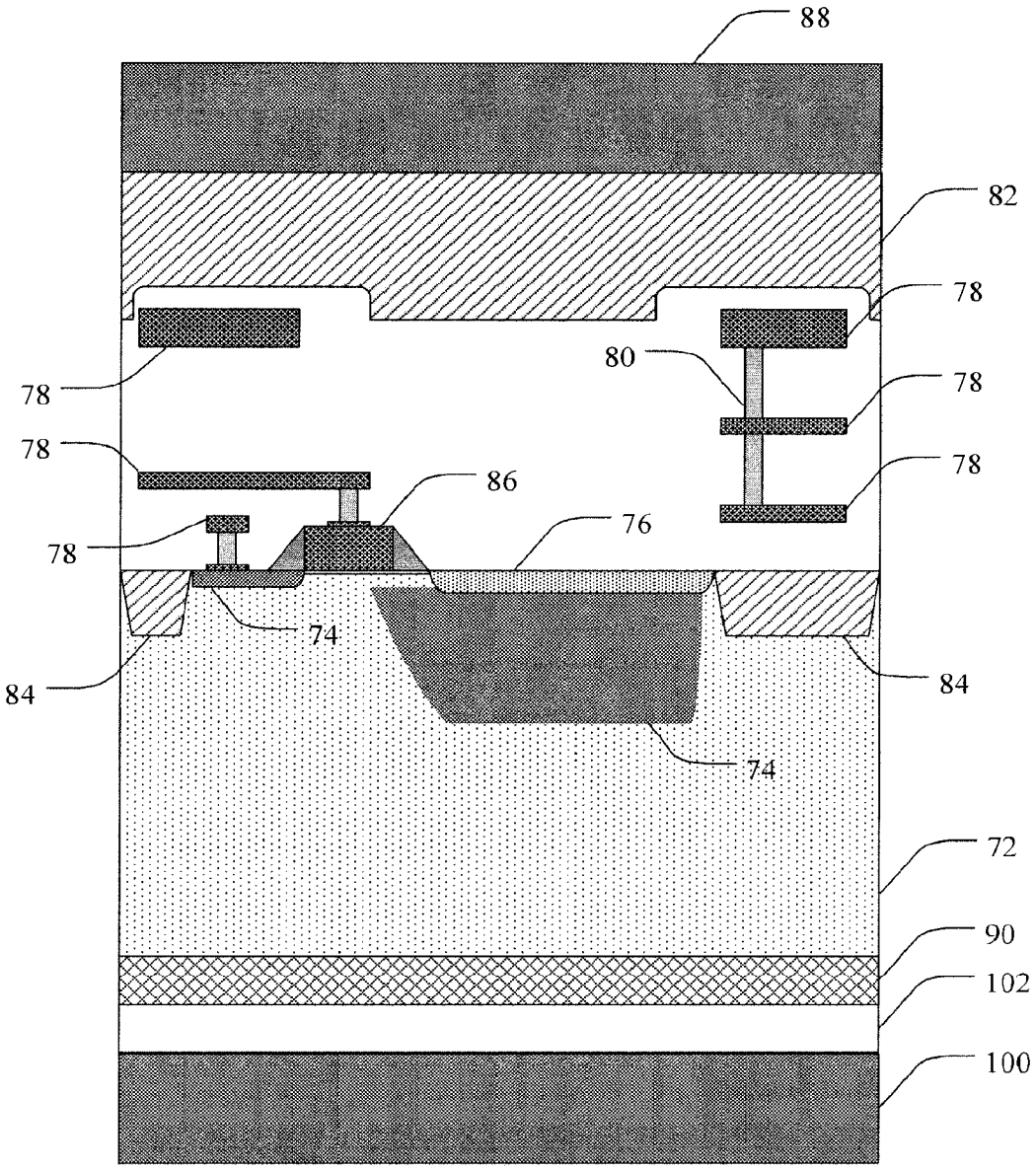

FIG. 10

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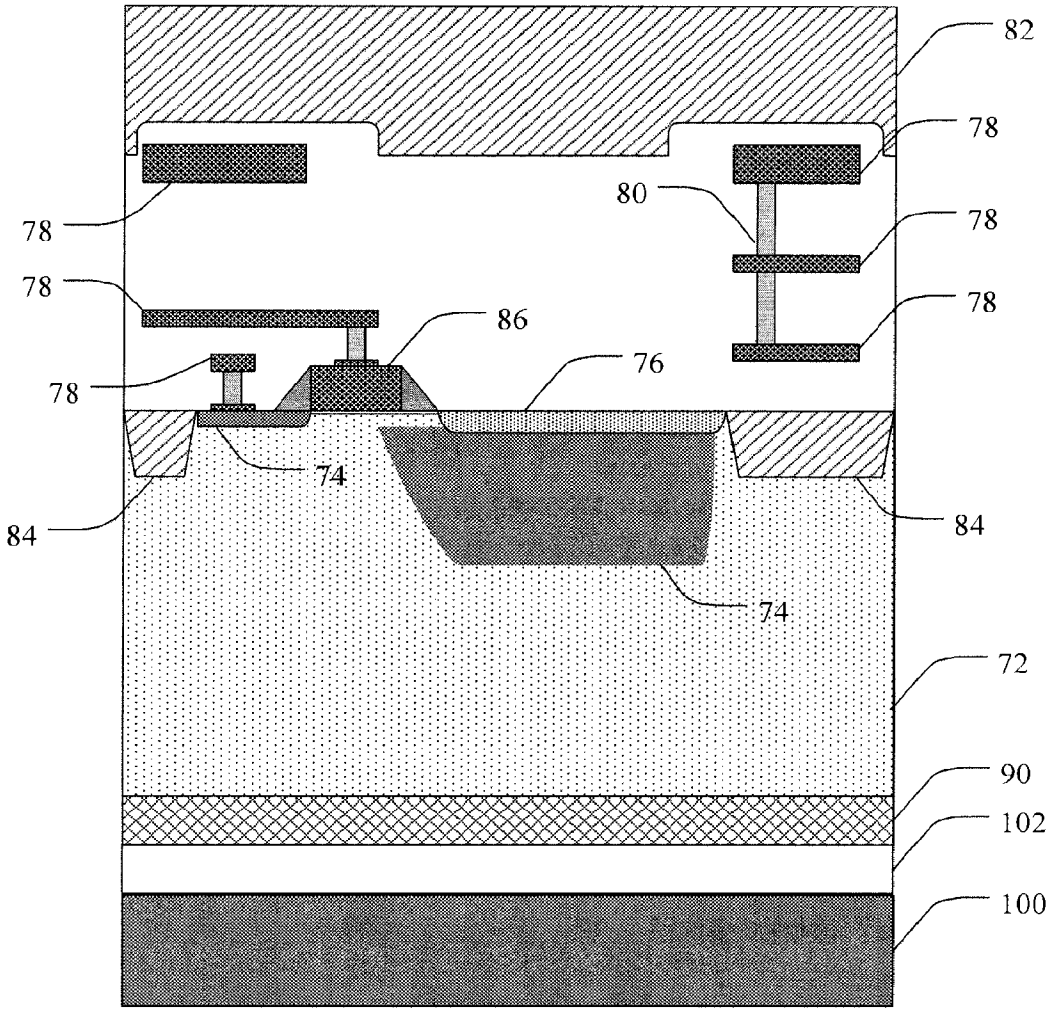

FIG. 11

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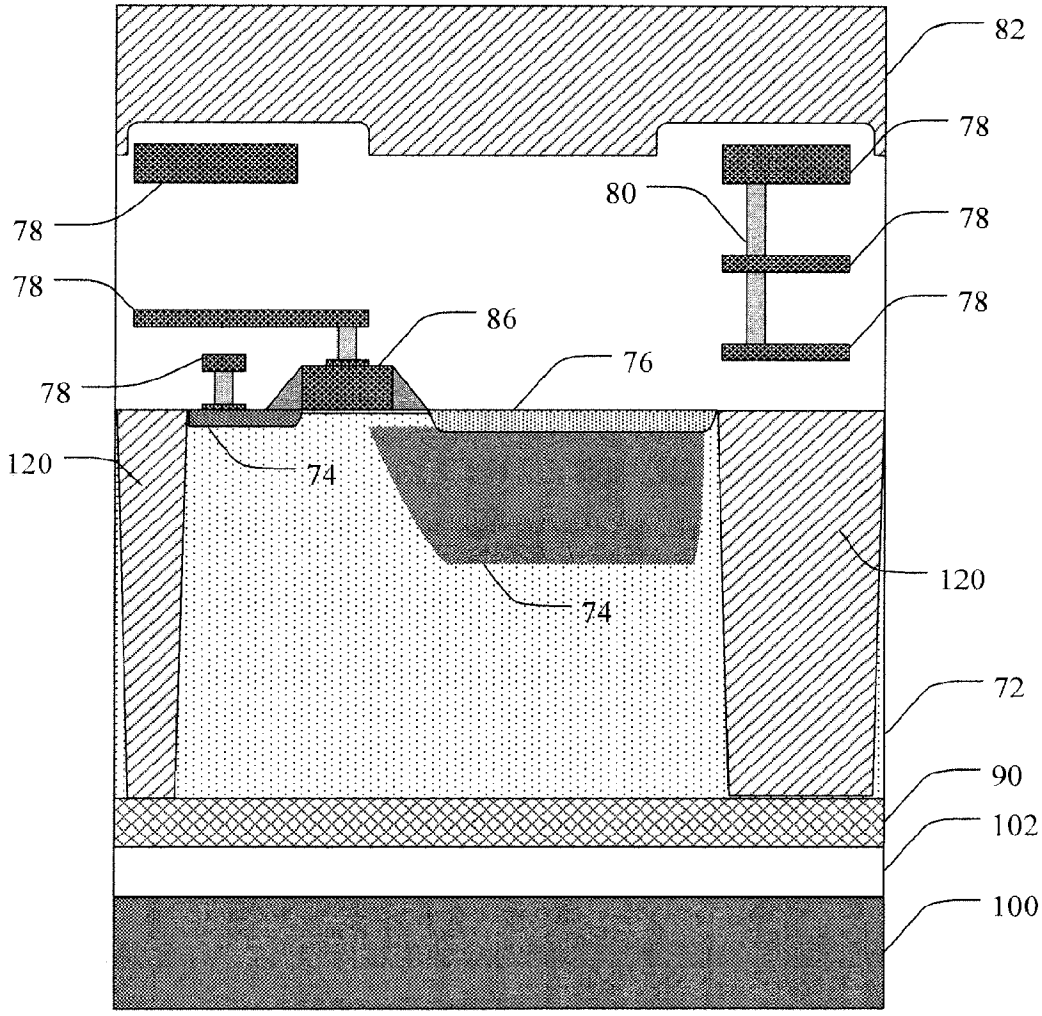

FIG. 12

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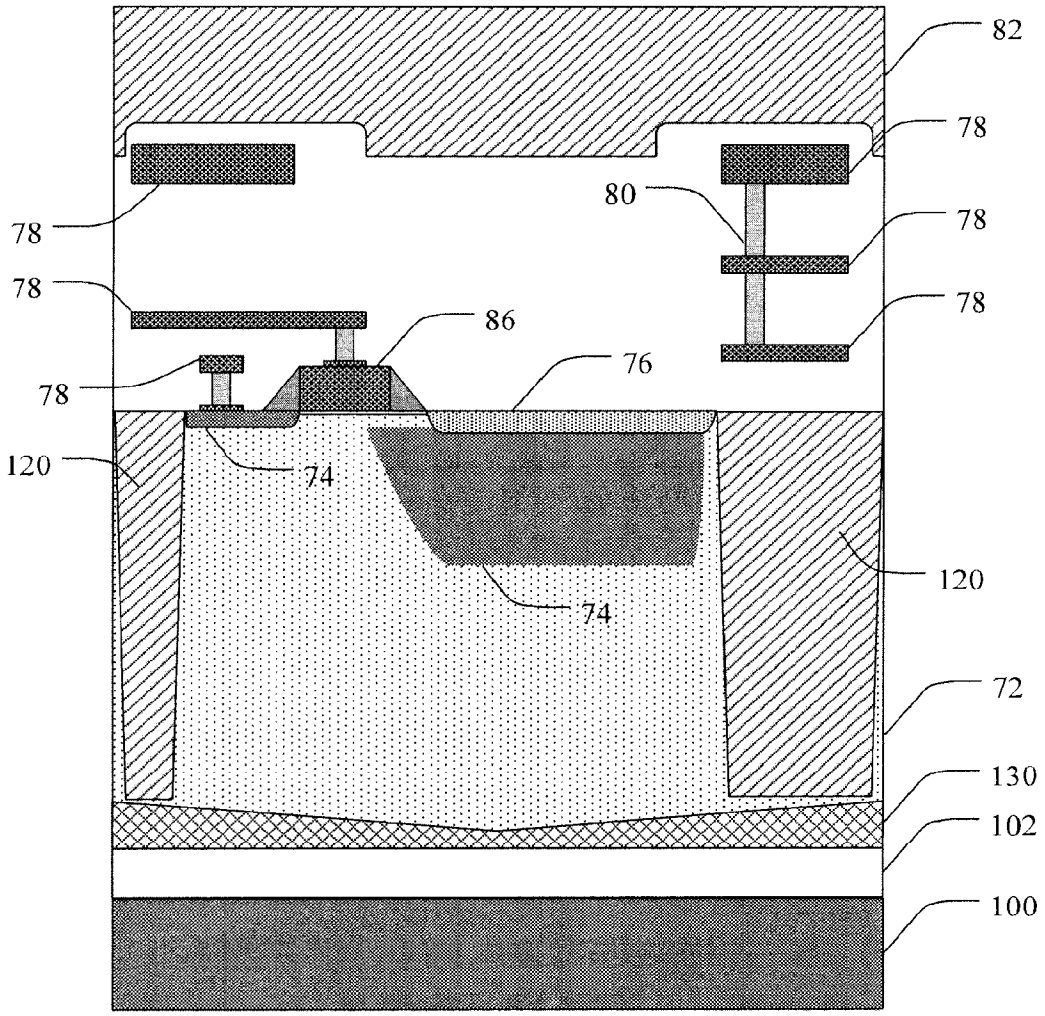

FIG. 13

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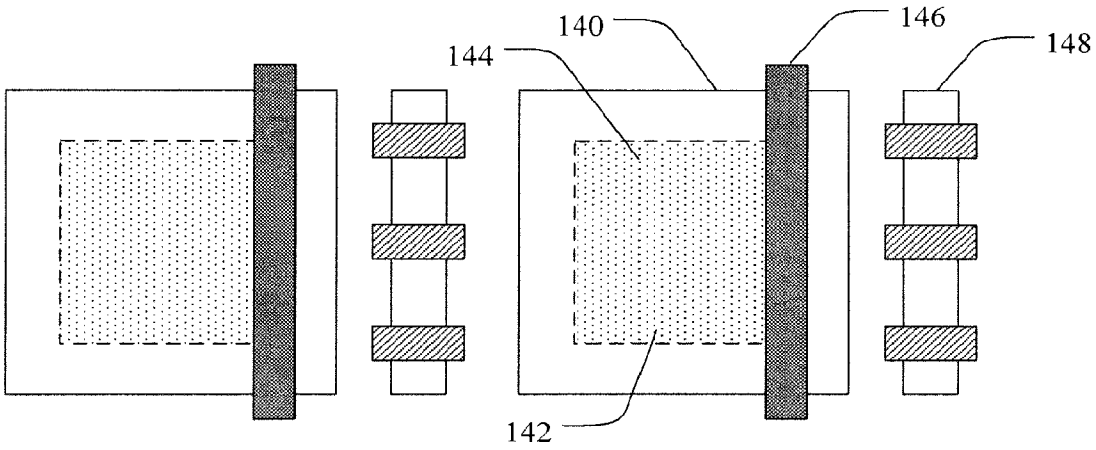

FIG. 14

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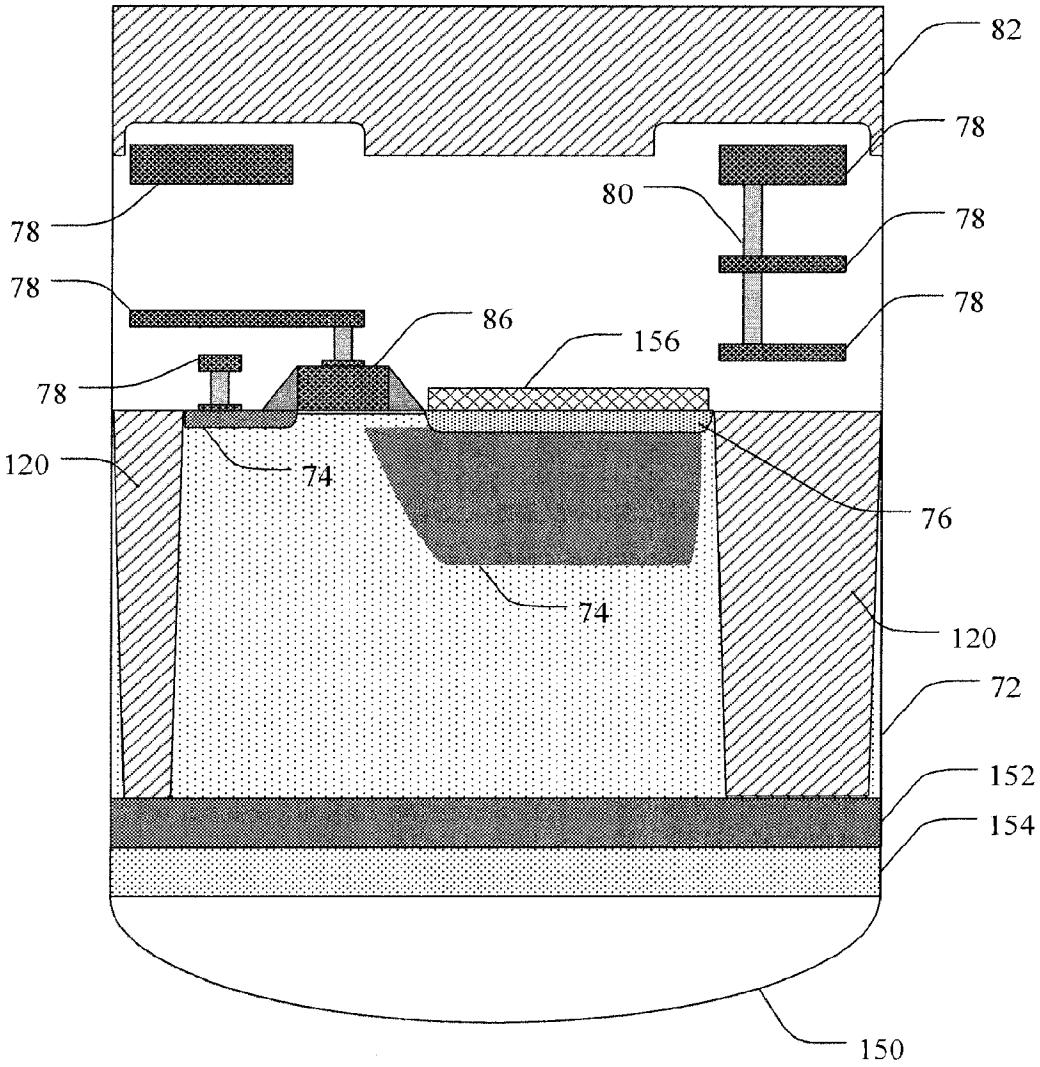

FIG. 15

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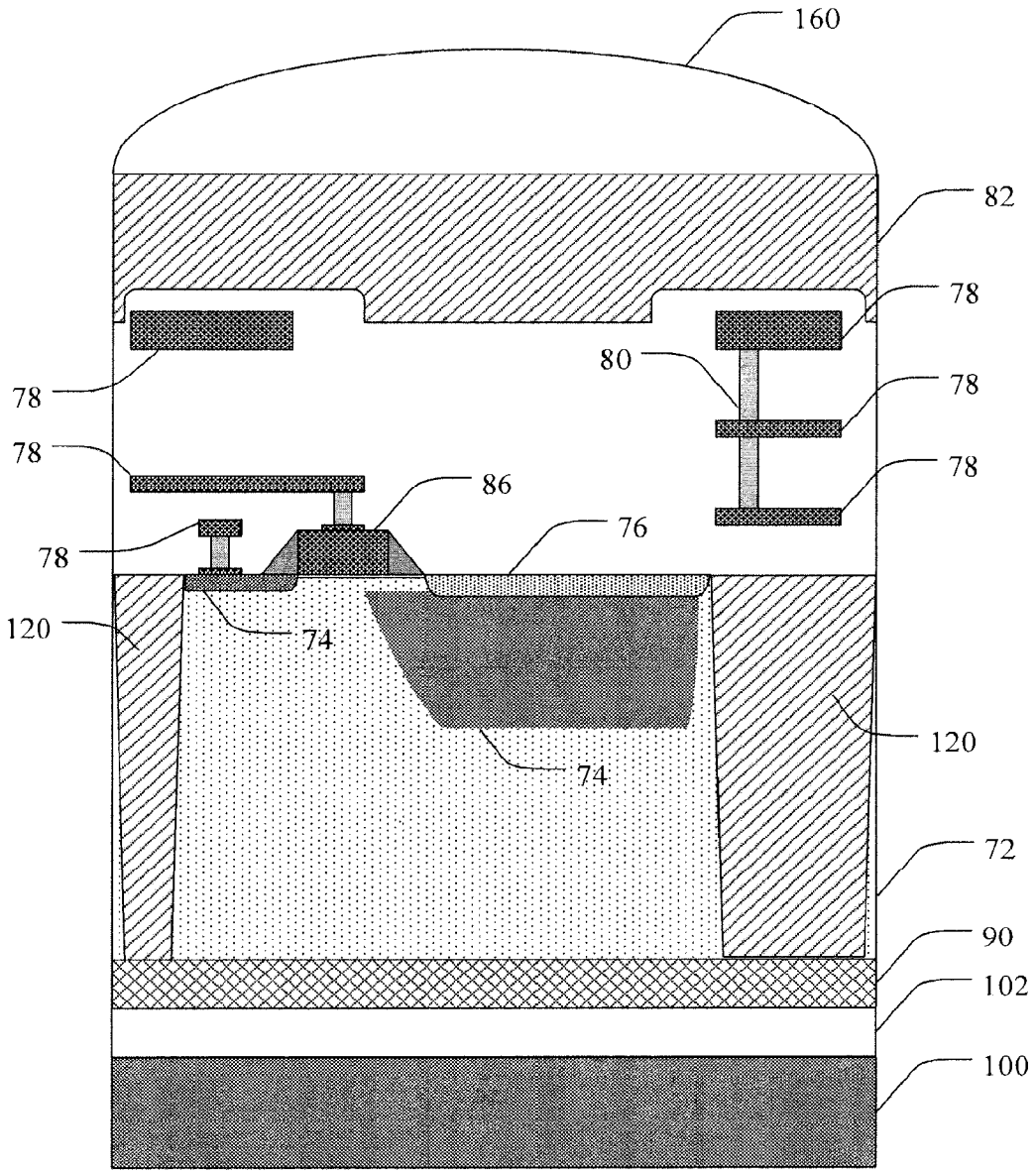

FIG. 16

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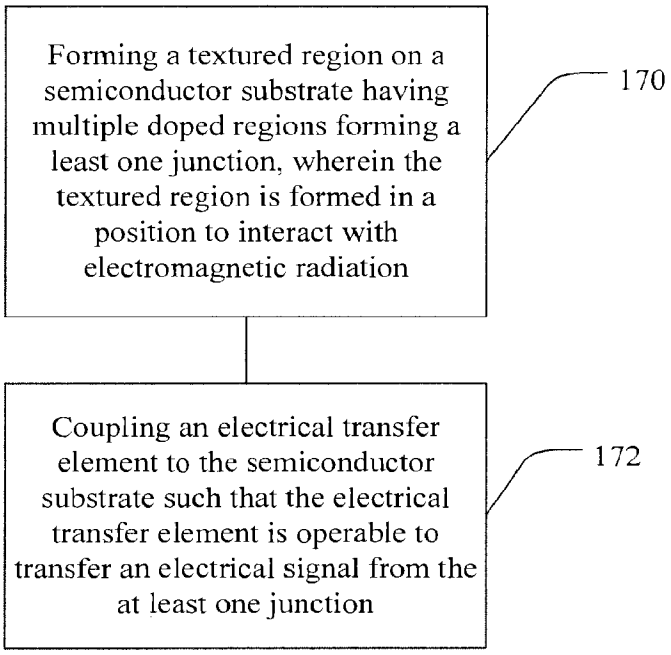

FIG. 17

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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 September 2011 (29.09.2011)

PCT

(10) International Publication Number
WO 2011/119618 A2

(51) International Patent Classification:
H01L 31/101 (2006.01) *H01L 31/0236* (2006.01)

(21) International Application Number:
PCT/US2011/029447

(22) International Filing Date:
22 March 2011 (22.03.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/317,147 24 March 2010 (24.03.2010) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

(54) Title: DEVICES HAVING ENHANCED ELECTROMAGNETIC RADIATION DETECTION AND ASSOCIATED METHODS

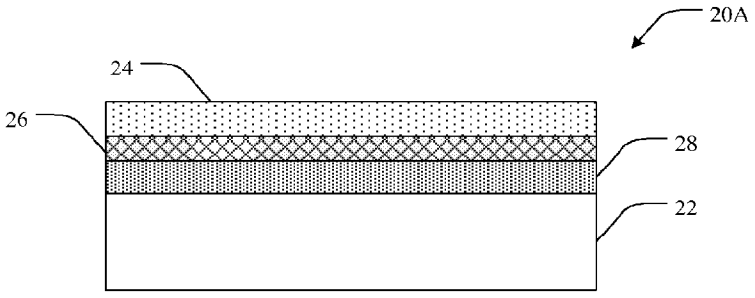

FIG. 2A

(57) Abstract: Photosensitive semiconductor devices and associated methods are provided. In one aspect, a semiconductor device can include a semiconductor substrate and a semiconductor layer coupled to the semiconductor substrate, where the semiconductor layer has a device surface opposite the semiconductor substrate. The device also includes at least one textured region coupled between the semiconductor substrate and the semiconductor layer. In another aspect, the device further includes at least one dielectric layer coupled between the semiconductor substrate and the semiconductor layer.

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DEVICES HAVING ENHANCED ELECTROMAGNETIC RADIATION DETECTION AND ASSOCIATED METHODS

PRIORITY DATA

This application claims the benefit of U.S. Provisional Patent Application Serial No. 61/317,147, filed on March 24, 2010, which is incorporated herein by reference.

BACKGROUND

Semiconductor on Insulator (SOI) wafer technology is an outgrowth of MicroElectroMechanical Systems (MEMS) technologies. An SOI wafer is a stacked wafer substrate where a device wafer (typically silicon) is bonded to a dielectric layer that is bonded to a support wafer, otherwise known as a handle wafer. A typical process flow for the fabrication of SOI wafers can be as follows: two wafers are polished and coated with an oxide or other dielectric material. The wafers are mounted polished side face to face and bonded under high temperature and pressure. Then one of the two wafers is ground down using mechanical grinding and chemical mechanical polishing to a specific thickness. In this way it is possible to generate semiconductor wafers that are electrically isolated from the underlying substrate.

SUMMARY

The present disclosure provides semiconductor structures and devices that can exhibit various enhanced properties, such as, for example, enhanced light detection properties. In one aspect, a semiconductor device is provided. Such a device can include a semiconductor substrate and a semiconductor layer coupled to the semiconductor substrate, where the semiconductor layer has a device surface opposite the semiconductor substrate. The device also includes at least one textured region coupled between the semiconductor substrate and the semiconductor layer. In another aspect, the device further includes at least one dielectric layer coupled between the semiconductor substrate and the semiconductor layer. In one aspect, the semiconductor layer is an epitaxially grown semiconductor layer. In another aspect, the semiconductor layer is a silicon layer. In a further aspect, a secondary semiconductor layer is disposed between the textured region and the semiconductor layer.

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Various positional configurations for the layers according to aspects of the present disclosure are contemplated, and any such configuration is considered to be within the present scope. In one specific aspect, for example, the dielectric layer is coupled between the semiconductor substrate and the textured region, and the textured region is disposed between the dielectric layer and the semiconductor layer. In one specific aspect, a reflective region is disposed between the semiconductor substrate and the textured region. In another specific aspect, the textured region is coupled directly to the semiconductor layer. In yet another specific aspect, a secondary semiconductor layer is disposed between the textured region and the semiconductor layer. In a further specific aspect, at least one cavity region disposed between the textured region and the dielectric layer. As another aspect of positional arrangement, the textured region is disposed between the semiconductor substrate and the dielectric layer, and the dielectric layer is disposed between the textured region and the semiconductor layer.

In one aspect of the present disclosure, a polysilicon layer is directly coupled to the dielectric layer. In another aspect, the polysilicon layer is disposed between multiple dielectric layers. In some aspects, the polysilicon layer can be doped.

In one aspect of the present disclosure, at least one photodiode optically active region is disposed on the device surface. In another aspect, the photodiode optically active region comprises a doped region. In yet another aspect, the device forms at least one photodetector. In a further aspect, the at least one photodetector is a plurality of photodetectors arranged in an array. In yet a further aspect, the textured region is arranged in a discontinuous pattern that corresponds spatially to the array of photodetectors. In another aspect, the device includes a plurality of isolation features in at least the semiconductor layer to isolate each photodetector in the array of photodetectors, where the isolation features isolate each photodetector electrically, optically, or both electrically and optically. In yet another aspect, the device includes at least one optical lens associated with the at least one photodetector. In a further aspect, the device includes at least one color filter associated with the at least one photodetector.

In one aspect of the present disclosure, the textured region is doped with a dopant to form an electrical back surface field. In another aspect, the electrical back surface field has been doped by a technique such as, without limitation, laser doping, ion implanting, diffusion doping, in situ doping, and the like, including combinations

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thereof. In yet another aspect, the textured region has a higher dopant concentration than the semiconductor layer. In a further aspect, the dopant has the same polarity as the semiconductor layer. Non-limiting examples of such dopants can include boron, indium, gallium, arsenic, antimony, phosphorus, and the like, including combinations thereof. Additionally, in other aspects a back surface field can be created by doping the semiconductor layer outside of the textured region. In one aspect, for example, the semiconductor layer is doped with a dopant to form an electrical back surface field, where the electrical back surface field is distinct from the textured region.

The present disclosure additionally provides methods of making semiconductor devices. In one aspect, one such method includes texturing at least a portion of a surface of a semiconductor layer to form a textured region, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate. In one aspect, the semiconductor layer is an epitaxially grown semiconductor layer. In another aspect, texturing at least a portion of a surface of a semiconductor layer to form a textured region further includes forming the epitaxially grown semiconductor layer on a growth substrate and texturing at least a portion of a surface of the epitaxially grown semiconductor layer to form a textured region. In yet another aspect, the method includes removing the growth substrate to expose the epitaxially grown semiconductor layer. In an alternative aspect, the method can include forming an epitaxially grown semiconductor layer on the semiconductor layer on an opposite side from the textured region.

In another aspect, wafer bonding includes depositing a polysilicon layer on the first dielectric layer and then bonding the polysilicon layer between the first dielectric layer and the second dielectric layer. In yet another aspect, at least a portion of the polysilicon layer can be doped. It is also contemplated that the present scope can include multiple dielectric and/or semiconductor material layers disposed between the semiconductor substrate and semiconductor layer.

In a further aspect, texturing at least a portion of a surface of the semiconductor layer to form the textured region further includes forming an opening in the semiconductor substrate, the second dielectric layer, and the first dielectric layer to expose a portion of the semiconductor layer and texturing at least a portion of the exposed portion of the semiconductor layer to form the textured region.

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In another aspect, the present disclosure provides a method of protecting a textured region from contamination during manufacture of a semiconductor device. Such a method includes texturing at least a portion of a surface of a semiconductor layer to form a textured region, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the dielectric layer, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate, wherein the textured region is protected from contamination during further manufacturing processes by the semiconductor layer and the semiconductor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

For a further understanding of the nature and advantage of the present disclosure, reference is being made to the following detailed description of embodiments and in connection with the accompanying drawings, in which:

FIG. 1 is a cross-sectional view of a semiconductor structure in accordance with an embodiment of the present disclosure;

FIG. 2A is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 2B is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 2C is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 2D is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 3 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 4 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 5 is a cross-sectional view of a semiconductor photodiode in accordance with another embodiment of the present disclosure;

FIG. 6 is a cross-sectional view of a semiconductor photodetecting imager in accordance with another embodiment of the present disclosure;

FIG. 7 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

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FIG. 8 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 9 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 10 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 11A is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 11B is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 11C is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 12A is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 12B is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 12C is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 13A is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 13B is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 13C is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

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FIG. 13D is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure; and

FIG. 14 is a depiction of a method of making a semiconductor device in accordance with yet another aspect of the present disclosure.

DETAILED DESCRIPTION

Before the present disclosure is described herein, it is to be understood that this disclosure is not limited to the particular structures, process steps, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting.

Definitions

The following terminology will be used in accordance with the definitions set forth below.

It should be noted that, as used in this specification and the appended claims, the singular forms "a," and, "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a dopant" includes one or more of such dopants and reference to "the layer" includes reference to one or more of such layers.

As used herein, the terms "disordered surface" and "textured surface" can be used interchangeably, and refer to a surface having a topology with nano- to micron-sized surface variations. Although any texturing technique is considered to be within the present scope, in one aspect the texturing is formed by the irradiation of laser pulses. Furthermore, while the characteristics of a textured surface can be variable depending on the materials and techniques employed, in one aspect such a surface can be several hundred nanometers thick and made up of nanocrystallites (e.g. from about 10 to about 50 nanometers), nanopores, and the like. In another aspect, such a surface can include micron-sized structures (e.g. about 2 μm to about 60 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 500 μm.

As used herein, the terms "surface modifying," "surface modification," and "texturing" can be used interchangeably, and refer to the altering of a surface of a

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semiconductor material using a texturing technique. In one specific aspect, surface modification can include processes using primarily laser radiation or laser radiation in combination with a dopant, whereby the laser radiation facilitates the incorporation of the dopant into a surface of the semiconductor material. Accordingly, in one aspect surface modification includes doping the material.

As used herein, the term "fluence" refers to the amount of energy from a single pulse of laser radiation that passes through a unit area. In other words, "fluence" can be described as the energy density of one laser pulse.

As used herein, the term "target region" refers to an area of a semiconductor material that is intended to be doped or surface modified using laser radiation. The target region of a semiconductor material can vary as the surface modifying process progresses. For example, after a first target region is doped or surface modified, a second target region may be selected on the same semiconductor material.

As used herein, the term "absorptance" refers to the fraction of incident electromagnetic radiation absorbed by a material or device.

As used herein, the term "substantially" refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is "substantially" enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use of "substantially" is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is "substantially free of" particles would either completely lack particles, or so nearly completely lack particles that the effect would be the same as if it completely lacked particles. In other words, a composition that is "substantially free of" an ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

As used herein, the term "about" is used to provide flexibility to a numerical range endpoint by providing that a given value may be "a little above" or "a little below" the endpoint.

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As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of "about 1 to about 5" should be interpreted to include not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

The Disclosure

The present disclosure provides semiconductor devices and associated methods that can exhibit various enhanced properties, such as, for example, enhanced light detection properties. Additionally, the present disclosure provides an integrated approach for the fabrication and application of textured semiconductor materials resulting in enhancement of image sensors and photodetectors. Specific types of semiconductor texturing can enhance the spectral bandwidth, absorption, and quantum efficiency of a semiconductor material. Performance can also be enhanced through various architecture configurations. Such configurations can also significantly improve the process integration of a particular device architecture with traditional process flows such as, for example, traditional CMOS process flows.

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A device design having a textured region located on, for example, the back surface of a photodetector, provides significant performance benefits. The textured region can have surface features that can lead to higher recombination of photocarriers for short wavelengths (e.g. in the blue green part of the spectrum) due to the very shallow penetration of those wavelengths into the detecting volume of the device. By physically locating the textured on the back surface of the device, a pristine surface is provided for the collection of short wavelengths on the top surface (i.e. the light incident surface), and the longer wavelengths that penetrate deep into or through the detecting region of the semiconductor material are collected by or with the help of the textured region opposite the light incident surface. It should be noted that, in addition to backside illuminated, front side illuminated architectures are also contemplated to be within the present scope. In addition, enhanced performance and ease of manufacture can also be accomplished by locating a textured region within a semiconductor stack or wafer. In some aspects, the textured layer can be located within the semiconductor stack early in the manufacturing process prior to the deposition of structures or circuitry that may be negatively affected by a texturing process. Additionally, such a semiconductor stack can be sent to an outside fabrication process for further manufacturing without exposing technological details regarding the textured region embedded between the semiconductor layers or any interaction between the textured region and the semiconductor layers.

In one aspect, as is shown in FIG. 1, a semiconductor device 10 is provided. While various semiconductor functions are contemplated, in one aspect the semiconductor device can exhibit enhanced electromagnetic radiation detection. Such a device can include a semiconductor substrate 12 and a semiconductor layer 14 coupled to the semiconductor substrate. The semiconductor layer has a device surface 15 opposite the semiconductor substrate. The device also includes at least one textured region 16 located or coupled between the semiconductor substrate and the semiconductor layer. As such, the textured region is enclosed between the semiconductor substrate and the semiconductor layer. Subsequent processing of the semiconductor device such as, for example, the formation of structures on the device surface, does not affect this buried textured region. In one aspect, the textured region can be formed on the semiconductor substrate. In another aspect, the textured region can be formed on the semiconductor layer. Additionally, for FIG. 1 and subsequent figures, the textured region can be a single textured region as is shown, or the textured

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region can be multiple discrete textured regions. Also, the textured region can cover only a portion of the surface area between the semiconductor substrate and the semiconductor layer as is shown, or the textured region can cover the entire surface area there between.

In another aspect, as is shown in FIG. 2A, a semiconductor device 20A is provided. Such a device can include a semiconductor substrate 22 and a semiconductor layer 24 coupled to the semiconductor substrate. The device also includes at least one textured region 26 located or coupled between the semiconductor substrate and the semiconductor layer, and at least one dielectric layer 28 coupled between the semiconductor substrate and the semiconductor layer. While various utilities are contemplated for the dielectric layer, in one aspect such a layer can be used to wafer bond the semiconductor layer to the semiconductor substrate. In one aspect, the dielectric layer can be formed on the semiconductor substrate. In another aspect, the dielectric layer can be formed on the textured region. Also, in some aspects the textured region can be formed on the dielectric layer. Additionally, in one aspect the semiconductor layer can be an epitaxially grown semiconductor layer. Thus in some aspects, the textured region can be formed on the epitaxially grown semiconductor layer.

It should be noted that, for all aspects, the present scope can also include multiple dielectric layers and/or multiple semiconductor material layers disposed between the semiconductor substrate and semiconductor layer. Additionally, the semiconductor layer itself can be multiple semiconductor layers and the semiconductor substrate can include multiple layers. It should also be noted that the semiconductor substrate refers to a substrate for a semiconductor, and can be comprised of semiconductor materials and/or non-semiconductor materials.

FIG. 2B shows a semiconductor device 20B having a secondary semiconductor layer 27 located between the textured region and the semiconductor layer. A semiconductor layer 24 is formed on the secondary semiconductor layer. In one aspect the semiconductor layer is an epitaxially grown semiconductor layer. Thus in some aspects, the textured region can be formed on the secondary semiconductor layer or on the dielectric layer 28. It should be noted that all reference numbers in FIGs. 2B-D that have been reused from FIG. 2A denote the same or similar materials and/or structures whether or not further description is provided.

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FIG. 2C shows a semiconductor device 20C whereby the dielectric layer 28 coupled between the semiconductor layer and the textured region. In this case, the dielectric layer can be formed on the semiconductor layer 24, the textured region 28, or on both the semiconductor layer and the textured region. In one aspect, the textured region can be formed on the semiconductor substrate 22. In another aspect, the textured region can be formed on the dielectric layer.

Additionally, in some aspects, as is shown in FIG. 2D for semiconductor device 20D, the dielectric layer can be a plurality of dielectric layers 28. In the case of wafer bonding, for example, a first dielectric layer can be associated with the textured layer and a second dielectric layer can be associated with the semiconductor substrate. The first dielectric layer and the second dielectric layer are heated and pressed together, with or without the aid of further pressure, temperature, or plasma surface activation, to cause the dielectric layers to bond to one another, thus forming a single wafer-bonded structure. It should be noted, however, that wafer-bonding can be accomplished without one or more dielectric layers, and as such the present scope should also include wafer-bonding that lacks such dielectric materials. Additionally, in some aspects, the textured region can be located in between the plurality of dielectric layers (not shown).

A variety of semiconductor materials are contemplated for use with the devices and methods according to aspects of the present disclosure. Such materials can be utilized as the semiconductor layer and/or the semiconductor substrate, as well as for the secondary semiconductor layer and the epitaxially grown semiconductor layer. Non-limiting examples of such semiconductor materials can include group IV materials, compounds and alloys comprised of materials from groups II and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can include silicon carbide (SiC) and silicon germanium (SiGe). In one specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum gallium arsenide, and combinations thereof.

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Exemplary combinations of group II-VI materials can include cadmium selenide (CdSe), cadmium sulfide (CdS), cadmium telluride (CdTe), zinc oxide (ZnO), zinc selenide (ZnSe), zinc sulfide (ZnS), zinc telluride (ZnTe), cadmium zinc telluride (CdZnTe, CZT), mercury cadmium telluride (HgCdTe), mercury zinc telluride (HgZnTe), mercury zinc selenide (HgZnSe), and combinations thereof.

Exemplary combinations of group III-V materials can include aluminum antimonide (AlSb), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum phosphide (AlP), boron nitride (BN), boron phosphide (BP), boron arsenide (BAs), gallium antimonide (GaSb), gallium arsenide (GaAs), gallium nitride (GaN), gallium phosphide (GaP), indium antimonide (InSb), indium arsenide (InAs), indium nitride (InN), indium phosphide (InP), aluminum gallium arsenide (AlGaAs, $Al_xGa_{1-x}As$), indium gallium arsenide (InGaAs, $In_xGa_{1-x}As$), indium gallium phosphide (InGaP), aluminum indium arsenide (AlInAs), aluminum indium antimonide (AlInSb), gallium arsenide nitride (GaAsN), gallium arsenide phosphide (GaAsP), aluminum gallium nitride (AlGaN), aluminum gallium phosphide (AlGaP), indium gallium nitride (InGaN), indium arsenide antimonide (InAsSb), indium gallium antimonide (InGaSb), aluminum gallium indium phosphide (AlGaInP), aluminum gallium arsenide phosphide (AlGaAsP), indium gallium arsenide phosphide (InGaAsP), aluminum indium arsenide phosphide (AlInAsP), aluminum gallium arsenide nitride (AlGaAsN), indium gallium arsenide nitride (InGaAsN), indium aluminum arsenide nitride (InAlAsN), gallium arsenide antimonide nitride (GaAsSbN), gallium indium nitride arsenide antimonide (GaInNAsSb), gallium indium arsenide antimonide phosphide (GaInAsSbP), and combinations thereof.

The semiconductor material can be of any thickness that allows the desired property or functionality of the semiconductor device, and thus any such thickness of semiconductor material is considered to be within the present scope. The textured region can increase the efficiency of the device such that, in some aspects, the semiconductor material can be thinner than has previously been possible. Decreasing the thickness reduces the amount of semiconductor material used to make such a device. In one aspect, for example, a semiconductor material such as the semiconductor layer has a thickness of from about 500 nm to about 50 μm. In another aspect, the semiconductor material has a thickness of less than or equal to about 500 μm. In yet another aspect, the semiconductor material has a thickness of from about 1 μm to about 10 μm. In a further aspect, the semiconductor material can have a

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thickness of from about 5 μm to about 750 μm. In yet a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 100 μm.

Additionally, various configurations of semiconductor materials are contemplated, and any such material configuration that can be incorporated into a semiconductor device is considered to be within the present scope. In one aspect, for example, the semiconductor material can include monocrystalline materials. In another aspect, the semiconductor material can include multicrystalline materials. In yet another aspect, the semiconductor material can include microcrystalline materials. It is also contemplated that the semiconductor material can include amorphous materials.

As has been described, the semiconductor substrate can be of any size, shape, and material capable of supporting the semiconductor layer and associated components during manufacture and/or use. The semiconductor substrate can be made from various materials, including the semiconductor materials described above, as well as non-semiconductor materials. Non-limiting examples of such materials can include metals, polymeric materials, ceramics, glass, and the like. In some aspects, the semiconductor substrate and the semiconductor layer have the same or substantially the same thermal expansion properties.

Furthermore, the semiconductor material according to aspects of the present disclosure can comprise multiple layers. In some aspects, layers can vary in majority carrier polarity (i.e. donor or acceptor impurities). The donor or acceptor impurities are typically determined by the type of dopant/impurities introduced into the device either through a growth process, deposition process, epitaxial process, implant process, lasing process or other known process to those skilled in the art. In some aspects such semiconductor materials can include an n-type layer, an intrinsic (i-type) layer, and a p-type layer, thus forming a p-i-n semiconductor material stack that creates a junction and/or depletion region. A semiconductor material devoid of an i-type layer is also contemplated in accordance with the present disclosure. In other aspects the semiconductor material may include multiple junctions. Additionally, in some aspects, variations of n(--), n(-), n(+), n(++), p(--), p(-), p(+), or p(++) type semiconductor layers can be used. The minus and positive signs are indicators of the relative magnitude of the doping of the semiconductor material.

As has been described, the textured region is buried between the semiconductor substrate and the semiconductor layer in various architectural

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arrangements. The textured can be of various thicknesses, depending on the desired use of the material. In one aspect, for example, the textured region has a thickness of from about 500 nm to about 100 μm. In another aspect, the textured region has a thickness of from about 500 nm to about 15 μm. In yet another aspect, the textured region has a thickness of from about 500 nm to about 2 μm. In a further aspect, the textured region has a thickness of from about 500 nm to about 1 μm. In another aspect, the textured region has a thickness of from about 200 nm to about 2 μm.

The textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and/or to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device. The textured region can include surface features to further increase the effective absorption length of the device. Non-limiting examples of shapes and configurations of surface features include cones, pillars, pyramids, microlenses, quantum dots, inverted features, gratings, protrusions, sphere-like structures, and the like, including combinations thereof. Additionally, surface features can be micron-sized, nano-sized, or a combination thereof. For example, cones, pyramids, protrusions, and the like can have an average height within this range. In one aspect, the average height would be from the base of the feature to the distal tip of the feature. In another aspect, the average height would be from the surface plane upon which the feature was created to the distal tips of the feature. In one specific aspect, a feature (e.g. a cone) can have a height of from about 50 nm to about 2 μm. As another example, quantum dots, microlenses, and the like can have an average diameter within the micron-sized and/or nano-sized range.

In addition to or instead of surface features, the textured region can include a textured layer. In one aspect, for example, the textured region can include a substantially conformal textured layer. Such a textured layer can have an average thickness of from about 1 nm to about 20 μm. In those aspects where the textured region includes surface features, the conformal textured layer can have a varying thickness relative to the location on the surface features upon which is deposited. In the case of cones, for example, the conformal textured layer can become thinner toward the tips of the cones. Such a conformal layer can include various materials, including, without limitation, SiO_2, Si_3N_4, amorphous silicon, polysilicon, a metal or metals, and the like, including combinations thereof. The conformal textured layer can also be one or more layers of the same or different materials, and can be formed during the creation of surface features or in a separate process.

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Textured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared). Such internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor layer. This increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.

The materials used for making the textured region can vary depending on the design and the desired characteristics of the device. As such, any material that can be utilized in the construction of a textured region is considered to be within the present scope. In one aspect, for example, the texture region can be a textured portion of a specific material, such as a portion of the semiconductor layer or the semiconductor substrate. If the texture layer is to be associated with the semiconductor layer, for example, a surface facing the semiconductor substrate can be textured prior to an attachment process such as wafer bonding. In another aspect, the textured region can be formed from a material that is deposited onto the semiconductor layer or semiconductor substrate, or the textured layer itself can be deposited. Such materials can include a semiconductor material, a dielectric material, or the like, including combinations thereof. In one specific example, the deposited material can include a silicon material. In another specific example, the deposited material can be polysilicon. In yet another aspect, the deposited material can be a dielectric material.

The texturing process can texture the entire substrate to be processed or only a portion of the substrate. In one aspect, for example, a substrate such as the semiconductor layer can be textured and patterned by an appropriate technique over an entire surface to form the texture region. In another aspect, a substrate such as the semiconductor layer can be textured and patterned across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch or a laser process to define a specific structure or pattern.

In addition to surface features, the textured region can have a surface morphology that is designed to focus or otherwise direct electromagnetic radiation. For example, in one aspect the textured region has a surface morphology operable to direct electromagnetic radiation into the semiconductor layer. Non-limiting examples of various surface morphologies include sloping, pyramidal, inverted pyramidal, spherical, square, rectangular, parabolic, asymmetric, symmetric, and the like, including combinations thereof.

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The textured region, including surface features as well as surface morphologies, can be formed by various techniques, including plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, selective epitaxial growth, and the like.

One effective method of producing a textured region is through laser processing. Such laser processing allows discrete target areas of a substrate to be textured, as well as entire surfaces. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope. Laser treatment or processing can allow, among other things, enhanced absorption properties and thus increased electromagnetic radiation focusing and detection.

In one aspect, for example, a target region of the substrate to be textured can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Patents 7,057,256, 7,354,792 and 7,442,629, which are incorporated herein by reference in their entireties. Briefly, a surface of a substrate material is irradiated with laser radiation to form a textured or surface modified region. Such laser processing can occur with or without a dopant material. In those aspects whereby a dopant is used, the laser can passed through a dopant carrier and onto the substrate surface. In this way, dopant from the dopant carrier is introduced into the target region of the substrate material. Such a region incorporated into a substrate material can have various benefits in accordance with aspects of the present disclosure. For example, the textured region typically has a textured surface that increases the surface area and increases the probability of radiation absorption. In one aspect, such a textured region is a substantially textured surface including micron-sized and/or nano-sized surface features that have been generated by the laser texturing. In another aspect, irradiating the surface of a substrate material includes exposing the laser radiation to a dopant such that irradiation incorporates the dopant into the substrate. Various dopant materials are known in the art, and are discussed in more detail herein.

Thus the surface of the substrate at the target region is thus chemically and/or structurally altered by the laser treatment, which may, in some aspects, result in the formation of surface features appearing as structures or patterned areas on the surface and, if a dopant is used, the incorporation of such dopants into the substrate material.

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In some aspects, the features or structures can be on the order of 50 nm to 20 μm in size and can assist in the absorption of electromagnetic radiation. In other words, the textured surface can increase the probability of incident radiation being absorbed.

The type of laser radiation used to surface modify a material can vary depending on the material and the intended modification. Any laser radiation known in the art can be used with the devices and methods of the present disclosure. There are a number of laser characteristics, however, that can affect the surface modification process and/or the resulting product including, but not limited to, the wavelength of the laser radiation, pulse width, pulse fluence, pulse frequency, polarization, laser propagation direction relative to the semiconductor material, etc. In one aspect, a laser can be configured to provide pulsatile lasing of a material. A short-pulsed laser is one capable of producing femtosecond, picosecond, and/or nanosecond pulse durations. Laser pulses can have a central wavelength in a range of about from about 10 nm to about 8 μm, and more specifically from about 200 nm to about 1200 nm. The pulse width of the laser radiation can be in a range of from about tens of femtoseconds to about hundreds of nanoseconds. In one aspect, laser pulse widths can be in the range of from about 50 femtoseconds to about 50 picoseconds. In another aspect, laser pulse widths can be in the range of from about 50 picoseconds to 100 nanoseconds. In another aspect, laser pulse widths are in the range of from about 50 to 500 femtoseconds.

The number of laser pulses irradiating a target region can be in a range of from about 1 to about 2000. In one aspect, the number of laser pulses irradiating a target region can be from about 2 to about 1000. Further, the repetition rate or frequency of the pulses can be selected to be in a range of from about 10 Hz to about 10 μHz, or in a range of from about 1 kHz to about 1 MHz, or in a range from about 10 Hz to about 1 kHz. Moreover, the fluence of each laser pulse can be in a range of from about 1 kJ/m^2 to about 20 kJ/m^2, or in a range of from about 3 kJ/m^2 to about 8 kJ/m^2.

A variety of dopant materials are contemplated for both the formation of doped regions in the semiconductor layer and for doping of the textured region, and any dopant that can be used in such processes to modify a material is considered to be within the present scope. It should be noted that the particular dopant utilized can vary depending on the material being doped, as well as the intended use of the resulting material.

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A dopant can be either a charge donating or a charge accepting dopant species. More specifically, an electron donating or a hole donating species can cause a region to become more positive or negative in polarity as compared to the substrate upon which the rests. In one aspect, for example, the doped region can be p-doped. In another aspect the doped region can be n-doped.

In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof. It should be noted that the scope of dopant materials should include, not only the dopant materials themselves, but also materials in forms that deliver such dopants (i.e. dopant carriers). For example, S dopant materials includes not only S, but also any material capable being used to dope S into the target region, such as, for example, H_2S, SF_6, SO_2, and the like, including combinations thereof. In one specific aspect, the dopant can be S. Sulfur can be present at an ion dosage level of from about 5×10^{14} to about 3×10^{20} ions/cm^2. Non-limiting examples of fluorine-containing compounds can include ClF_3, PF_5, F_2 SF_6, BF_3, GeF_4, WF_6, SiF_4, HF, CF_4, CHF_3, CH_2F_2, CH_3F, C_2F_6, C_2HF_5, C_3F_8, C_4F_8, NF_3, and the like, including combinations thereof. Non-limiting examples of boron-containing compounds can include $B(CH_3)_3$, BF_3, BCl_3, BN, $C_2B_{10}H_{12}$, borosilica, B_2H_6, and the like, including combinations thereof. Non-limiting examples of phosphorous-containing compounds can include PF_5, PH_3, $POCl_3$, P_2O_5, and the like, including combinations thereof. Non-limiting examples of chlorine-containing compounds can include Cl_2, SiH_2Cl_2, HCl, $SiCl_4$, and the like, including combinations thereof. Dopants can also include arsenic-containing compounds such as AsH_3 and the like, as well as antimony-containing compounds. Additionally, dopant materials can include mixtures or combinations across dopant groups, i.e. a sulfur-containing compound mixed with a chlorine-containing compound. In one aspect, the dopant material can have a density that is greater than air. In one specific aspect, the dopant material can include Se, H_2S, SF_6, or mixtures thereof. In yet another specific aspect, the dopant can be SF_6 and can have a predetermined concentration range of about 5.0×10^{-8} mol/cm^3 to about 5.0×10^{-4} mol/cm^3. As one non-limiting example, SF_6 gas is a good carrier for the incorporation of sulfur into a substrate via a laser process without significant adverse effects on the material. Additionally, it is noted that dopants can also be liquid solutions of n-type or p-type dopant materials dissolved in a solution such as water, alcohol, or an acid or basic

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solution. Dopants can also be solid materials applied as a powder or as a suspension dried onto the wafer.

In one aspect, the textured region can be doped with a dopant to form an electrical back surface field (EBSF). The EBSF impedes the movement of minority carriers from reaching the textured region, thus keeping such carriers away from potential recombination sites near the interface. Similarly, dark current generation can also be minimized by pinning the interface generation states at certain band energy states through band structure optimization so that the dark carrier generation mechanism is suppressed. Band structure optimization can be achieved by using a variety of methods. It should be noted that any method that forms an electrical field near or within the textured region can be used. Non-limiting examples of such methods can include shifting the Fermi level energy, bending the minority carrier band, inserting a material with a different bandgap, and the like, including combinations thereof.

In one aspect, for example, the band structure optimization can be realized by modifying the interface doping concentration. For example, for a p-type laser textured region, a more heavily p-doped layer that partially overlaps with the laser modified interface can be used. The conduction band thus bends toward the higher energy direction when reaching towards the more p-doped layer, and hence the laser modified interface. One specific aspect is a heavily doped p++ layer that partially overlaps with the laser modified interface layer in a p-epi substrate where both the p++ layer and the modified interface layer sit between the bottom of an epitaxial device layer and the top of a carrier wafer.

As such, in one aspect, the EBSF has been doped by a technique such as, without limitation, laser doping, ion implanting, diffusion doping, in situ doping, and the like, including combinations thereof. In another aspect, the textured region or the EBSF has a higher dopant concentration than the semiconductor layer. In yet another aspect, the dopant has the same polarity as the semiconductor layer. Various dopants for use in generating an EBSF are contemplated. Non-limiting examples include boron, indium, gallium, arsenic, antimony, phosphorus, and the like, including combinations thereof. It should also be noted that an EBSF can be produced in the semiconductor layer, the dielectric layer, or the semiconductor substrate. In one aspect, for example, semiconductor layer or the semiconductor substrate is doped with

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a dopant to form an electrical back surface field, where the EBSF is distinct from the textured region.

In another aspect, the band structure optimization can be realized by forming a heterojunction along a modified semiconductor interface. For example, a layer of amorphous silicon can be deposited on the textured region interface, thus forming a heterojunction that bends the minority carrier band towards the desired energy direction.

The dielectric layer can be made from a variety of materials, and such materials can vary depending on the device design and desired characteristics. One use for such a layer involves the coupling of the semiconductor layer to the semiconductor substrate. In some cases, wafer bonding can be used as a coupling technique. The dielectric layer can thus facilitate the attachment of these materials together, as has been described. The dielectric layer can be associated with the semiconductor layer, the semiconductor substrate, or both the semiconductor layer and the semiconductor substrate prior to bonding. In those aspects having a dielectric layer associated with both materials, the dielectric layers can be bonded directly together, or in some cases, bonded together with an intervening textured region. Additionally, in some aspects a textured region can be formed on one or more dielectric layers. In some aspects, a dielectric layer can be bonded to a semiconductor material such as, for example, polysilicon. In other aspects, the semiconductor layer and the semiconductor substrate can be bonded together without an intervening dielectric layer.

Non-limiting examples of dielectric layer materials can include oxides, nitrides, oxynitrides, and the like, including combinations thereof. In one specific aspect, the dielectric layer includes an oxide. In another aspect, the dielectric layer includes a buried oxide. Additionally, the dielectric layer can be of various thicknesses. In one aspect, for example, the dielectric layer has a thickness of from about 100 nm to about 4 microns. In another aspect, the dielectric layer has a thickness of from about 500 nm to about 2 microns. In yet another aspect, the dielectric layer has a thickness of from about 500 nm to about 1000 microns.

The devices according to aspects of the present disclosure can additionally include one or more reflecting regions. In one aspect, as is shown in FIG. 3, a photosensitive semiconductor device 30 can include a semiconductor substrate 32 and a semiconductor layer 34 coupled to the semiconductor substrate. The device also

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includes at least one textured region 36 located or coupled between the semiconductor substrate and the semiconductor layer, and at least one dielectric layer 38 coupled between the semiconductor substrate and the semiconductor layer. A reflecting region 39 is coupled to the semiconductor substrate, and positioned to interact with electromagnetic radiation. The reflecting region can be separated from the textured region by a dielectric layer as is shown, or the reflecting region can be associated directly with the textured region without an intervening dielectric layer. The reflecting region can be deposited over the entire interface between the semiconductor substrate and the next adjacent layer, or only over a portion of the interface. In some aspects, the reflecting region can be deposited over a larger area of the device compared to the textured region. The reflecting region can be positioned to reflect electromagnetic radiation that has passed through the texture region back through the textured region toward the semiconductor layer. In other words, as electromagnetic radiation passes through the semiconductor layer, a portion that is not absorbed contacts the textured region. Of that portion that contacts the textured region, a smaller portion may pass though the textured region to strike the reflecting region and be reflected back through the textured region toward the semiconductor layer.

A variety of reflective materials can be utilized in constructing the reflecting region, and any such material capable of incorporation into a photosensitive device is considered to be within the present scope. Non-limiting examples of such materials include a Bragg reflector, a metal reflector, a metal reflector over a dielectric material, a transparent conductive oxide such as zinc oxide, indium oxide, or tin oxide, and the like, including combinations thereof. Non-limiting examples of metal reflector materials can include silver, aluminum, gold, platinum, reflective metal nitrides, reflective metal oxides, and the like, including combinations thereof. In one aspect, a dielectric material can be coupled to the reflecting region along the side facing the textured region. In one specific aspect, the dielectric material can include an oxide layer and the reflecting region can include a metal layer. The surface of the metal layer on an oxide acts as a mirror-like reflector for the incident electromagnetic radiation from the backside.

Additionally, the textured surface of a metal on a roughened oxide can act as a diffusive scattering site for the incident electromagnetic radiation and also as a mirror-like reflector. Other aspects can utilize porous materials for the texturing. Porous polysilicon, for example, can be oxidized or oxide deposited and a reflective region

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such as a metal reflector can be associated therewith to provide a scattering and reflecting surface. In another aspect, aluminum can be subjected to anodic oxidation to provide porous aluminum oxide, a high dielectric constant insulator. This insulator can be coated with aluminum or other metals to provide a scattering and reflecting surface.

In one specific aspect, a reflective region can include a transparent conductive oxide, an oxide, and a metal layer. The transparent oxide can be textured and a metal reflector deposited thereupon. The textured surface of the metal on a roughened transparent conductive oxide can act as a diffusive scattering site for the incident electromagnetic radiation.

In another specific aspect, a Bragg reflector can be utilized as a reflective region. A Bragg reflector is a structure formed from multiple layers of alternating materials with varying refractive indexes, or by a periodic variation of some characteristic (e.g. height) of a dielectric waveguide, resulting in periodic variation in the effective refractive index in the guide. Each layer boundary causes a partial reflection of an optical wave. For waves whose wavelength is close to four times the optical thickness of the layers, the many reflections combine with constructive interference, and the layers act as a high-quality reflector. Thus the coherent super-positioning of reflected and transmitted light from multiple interfaces in the structure interfere so as to provide the desired reflective, transmissive, and absorptive behavior. In one aspect, the Bragg reflector layers can be alternating layers of silicon dioxide and silicon. Because of the high refractive index difference between silicon and silicon dioxide, and the thickness of these layers, this structure can be fairly low loss even in regions where bulk silicon absorbs appreciably. Additionally, because of the large refractive index difference, the optical thickness of the entire layer set can be thinner, resulting in a broader-band behavior and fewer fabrications steps.

Additional scattering can be provided by positioning a textured forward scattering layer on the side of the device that receives incident electromagnetic radiation. These forward scattering layers can be, without limitation, textured oxides or polysilicon without a reflector.

In another aspect, as is shown in FIG. 4, a photosensitive semiconductor device 40 can also include a polysilicon layer 42 disposes between multiple dielectric layers 38. It should be noted that all reference numbers in FIG. 4 that have been reused from previous figures denote the same or similar materials and/or structures

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whether or not further description is provided. The addition of the polysilicon layer can provide various improvements in manufacturing in some cases. For example, a rough surface of a textured region can be challenging to wafer bond. By depositing a thin dielectric layer followed by a thick polysilicon layer it can be possible to create a surface that can be polished. Thus, the polysilicon layer can be planarized and polished until smooth, and the resulting surface can be wafer bonded to the dielectric layer on the opposing material, e.g. the semiconductor substrate if the polysilicon is deposited on the semiconductor layer structure. It is also contemplated that such a process can be performed with only one dielectric layer or even without any dielectric layers being present. In another aspect, the polysilicon layer can be doped with a dopant. In yet another aspect, the polysilicon layer can be a monosilicon layer. In one specific aspect, the polysilicon layer is a monosilicon layer and the semiconductor layer is an epitaxial layer that has been etched from the backside to form the textured region.

In another aspect, as is shown in FIG. 5, a photodiode 50 having enhanced light detection performance is provided. The photodiode includes contacts 52 and a photodiode junction 54 formed on the semiconductor layer 34. In another aspect, as is shown in FIG. 6, a CMOS image sensor having improved light detection performance is provided. The CMOS image sensor includes photodiode junctions 64 and circuitry 62 formed on the semiconductor layer 34. It should be noted that all reference numbers in FIGs. 5 and 6 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided. In this way, the textured region 36 can be introduced into fabrication process at the start of the flow, at a lower cost and lower technical risk approach. Because the textured region is buried within the semiconductor materials at an early stage in the flow, the textured region can be protected from contamination during the further fabrication of the device. Additionally, potentially proprietary details such as the specific architecture of the texture region can be protected from view during the later stages of fabrication. This method could further include a step of removing the semiconductor substrate. It is understood that once the semiconductor device is formed the semiconductor substrate may no longer be necessary in some cases. In this way the semiconductor device can be mounted on various substrates as necessary for specific applications.

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In one aspect, isolation features can be utilized in order to isolate various portions of the device from one another. For example, in one aspect a semiconductor device can include a plurality of isolation features in at least the semiconductor layer that function to isolate each photodetector in an array of photodetectors from one another. The isolation features isolate each photodetector electrically, optically, or both electrically and optically. Isolation features can thus maintain uniformity across an array by reducing optical and electrical crosstalk between the photodetectors. FIG. 7 shows a semiconductor device 70 having an array of photodetectors 72. It should be noted that all reference numbers in FIG. 7 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided. The photodetectors are separated by a plurality of isolation features, in this case extending through the semiconductor layer 34 and the textured region 36. In one aspect, the isolation features extend through the semiconductor layer but not through the textured region. In another aspect, the isolation features extend beyond the textured region and into the dielectric layer or even into the semiconductor substrate. In some aspects, other structures such as polysilicon layers and reflective regions can contain isolation features. Accordingly, the isolation features can be deep or shallow, depending on the desired configuration of the device.

Isolation features can be made from various materials, including, without limitation, dielectric materials, reflective materials, conductive materials, light diffusing features, voids, and the like, including combinations thereof. Conductive materials used to fill the isolation feature etches or voids can be passivated in order to maintain electrical isolation. In other aspects, conductive materials can be utilized as vias. The isolation can be fabricated at the substrate level prior to fabrication of circuitry, the detector device, or the imaging array. In one aspect, voids can be created and either left as voids or filled with such materials to form the isolation features. For example, a layer surface can be photolithographically patterned and vertically etched to a desired depth (e.g. from the device surface of the semiconductor layer to the dielectric layer). Dielectric material can then be deposited conformally on surfaces within the etch until filled with the dielectric or other material. Any dielectric material remaining on the device surface of the semiconductor layer can be removed by chemical etching and/or mechanical polishing. As has been described, the isolation feature does not need to fully bisect the semiconductor structure, but

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rather only a portion can be isolated; this is known as shallow trench isolation as opposed to deep trench isolation.

Additionally, isolation features regions can be configured to reflect incident electromagnetic radiation until it is absorbed, thereby increase the effective absorption length of the device. In other aspects, the sides of isolation features can be doped. In some aspects, a doped isolation feature can form an electrical surface field, similar to an electrical back surface field as has been described. The isolation features can be formed before or after bonding of the semiconductor substrate to the semiconductor layer. Furthermore, the isolation features can be formed from either side of the semiconductor layer or from either side of the semiconductor substrate, depending on the depth and extent of the features.

In some aspects, the textured region can be arranged in a discontinuous pattern. As is shown in FIG. 8, for example, a semiconductor device 80 can have a discontinuous textured region 82. It should be noted that all reference numbers in FIG. 8 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided. Such a discontinuous pattern may correspond to structures elsewhere in the device, such as the spatial pattern of an array of photodetectors on the device surface (not shown).

In other aspects, one or more cavities can be disposed in the semiconductor device and associated with the textured region or regions. As is shown in FIG. 9, for example, a semiconductor device 90 can include a cavity region 92 associated with the textured region 36. The cavity region can enhance the functionality of the textured region, and can be particularly effective when optically coupled to a reflective region, whether the reflective region is on the near side or the far side of the dielectric layer 38. FIG. 10 shows a semiconductor device 100 having a plurality of cavity regions 102 arranged in a discontinuous pattern to correspond with the discontinuous pattern of the textured region 82. The cavity regions shown in FIGs. 9 and 10 can be formed prior to wafer bonding or following wafer bonding. If a cavity region is formed following wafer bonding, etching through the semiconductor substrate 32 may be required, following which the etch cavity can be partially filled. Additionally, a cavity region can be formed before or after formation of the textured region. In those aspects whereby a cavity region is formed after formation of the textured region, the intervening material would be etched until reaching the textured region. In those aspects whereby a cavity region is formed prior to formation of the

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textured region, an etch can be formed into the semiconductor layer 34 and the textured region can be formed thereon through the etch cavity. The formation of the textured region in this manner can be accomplished prior to wafer bonding or following wafer bonding by etching through the semiconductor substrate. It should be noted that all reference numbers in FIGs. 9 and 10 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided.

The present disclosure additionally provides various methods. In one aspect, as is shown in FIG. 14, for example, a method of making a semiconductor device can include texturing at least a portion of a surface of a semiconductor layer to form a textured region 142, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer 144, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate 146. In another aspect, the textured region is protected from contamination during further manufacturing processes by the semiconductor layer and the semiconductor substrate.

In another aspect, a method of making a semiconductor device can include laser texturing at least a portion of a surface of a semiconductor layer to form a textured region, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate.

In yet another aspect, a method of making a semiconductor device can include wet etch texturing at least a portion of a surface of a semiconductor layer to form a textured region, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate.

In one specific aspect, FIGs. 11A-C show one method of manufacturing a semiconductor device. As is shown in FIG. 11A, a semiconductor material 114 can be textured to create a textured region 112, and a dielectric layer 115 can be deposited over the textured region. In one aspect, the textured region can be formed by laser processing the semiconductor material. In another aspect, the textured region can be formed by wet etching the semiconductor material. The dielectric layer can then be

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polished until smooth with a process such as CMP processing. The resulting structure can then be wafer bonded to a semiconductor substrate 116, as is shown rotated 180° in FIG. 11B, with the polished surface of the dielectric layer being bonded to the semiconductor substrate. The dielectric layer can be bonded directly to the semiconductor substrate, or to a second dielectric layer formed on the semiconductor substrate (not shown). After wafer bonding, the semiconductor material can be polished to a specified thickness. In another aspect, an epitaxially grown semiconductor layer 118 can be grown on the polished surface of the semiconductor material to generate a low defect device region as shown in FIG. 11C.

In another aspect, FIGs. 12A-C show another method of manufacturing a semiconductor device. As is shown in FIG. 12A, a semiconductor material 124 can be textured to create a textured region 122, and a dielectric layer 125 can be deposited over the textured region. In one aspect, the semiconductor material can be an epitaxially grown semiconductor material. The dielectric layer can then be polished and a polysilicon layer 126 can be deposited thereupon, as is shown in FIG. 12B. In an alternative aspect, the polysilicon layer can be formed directly on the textured region without an intervening dielectric layer (not shown). The polysilicon layer can then be polished and wafer bonded to a semiconductor substrate 126, as is shown rotated 180° in FIG. 12C. The polysilicon layer can be bonded directly to the semiconductor substrate, or to a second dielectric layer 129 formed on the semiconductor substrate. After wafer bonding, the semiconductor material can be polished to a specified thickness.

In another aspect, FIGs. 13A-D show another method of manufacturing a semiconductor device. As is shown in FIG. 13A, a semiconductor layer 134 can be epitaxially grown on a temporary semiconductor support 139. The epitaxially grown semiconductor layer is textured to create a textured region 132, and a dielectric layer 135 is deposited over the textured region as is shown in FIG. 13B. Following polishing, the dielectric layer is wafer bonded to a semiconductor substrate 136, as is shown rotated 180° in FIG. 13C. The dielectric layer can be bonded directly to the semiconductor substrate, or to a second dielectric layer formed on the semiconductor substrate (not shown). The temporary semiconductor support can then be removed from the epitaxially grown semiconductor layer. This can be accomplished by any known process, such as wafer splitting, CMP processing, etc. The exposed epitaxial semiconductor layer can be further polished and thinned to produce a desired surface

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for further device deposition. In this manner semiconductor materials used to grow the epitaxial layer can be removed, leaving a higher quality surface with fewer crystal defects and dislocations.

Of course, it is to be understood that the above-described arrangements are only illustrative of the application of the principles of the present disclosure. Numerous modifications and alternative arrangements may be devised by those skilled in the art without departing from the spirit and scope of the present disclosure and the appended claims are intended to cover such modifications and arrangements. Thus, while the present disclosure has been described above with particularity and detail in connection with what is presently deemed to be the most practical embodiments of the disclosure, it will be apparent to those of ordinary skill in the art that numerous modifications, including, but not limited to, variations in size, materials, shape, form, function and manner of operation, assembly and use may be made without departing from the principles and concepts set forth herein.

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CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a semiconductor substrate;

a semiconductor layer coupled to the semiconductor substrate, the semiconductor layer having a device surface opposite the semiconductor substrate; and

at least one textured region coupled between the semiconductor substrate and the semiconductor layer.

2. The device of claim 1, further comprising at least one dielectric layer coupled between the semiconductor substrate and the semiconductor layer.

3. The device of claim 2, wherein the semiconductor layer is an epitaxially grown semiconductor layer.

4. The device of claim 2, wherein the semiconductor layer is a silicon layer.

5. The device of claim 2, further comprising a secondary semiconductor layer disposed between the textured region and the semiconductor layer.

6. The device of claim 2, wherein the dielectric layer is coupled between the semiconductor substrate and the textured region, and wherein the textured region is disposed between the dielectric layer and the semiconductor layer.

7. The device of claim 6, further comprising a reflective region disposed between the semiconductor substrate and the textured region.

8. The device of claim 6, wherein the textured region is coupled directly to the semiconductor layer.

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9. The device of claim 6, further comprising a secondary semiconductor layer disposed between the textured region and the semiconductor layer.

10. The device of claim 6, further comprising at least one cavity region disposed between the textured region and the dielectric layer.

11. The device of claim 2, further comprising a polysilicon layer directly coupled to the dielectric layer.

12. The device of claim 11, wherein the polysilicon layer is disposed between multiple dielectric layers.

13. The device of claim 2, wherein the textured region is disposed between the semiconductor substrate and the dielectric layer, and wherein the dielectric layer is disposed between the textured region and the semiconductor layer.

14. The device of claim 2, wherein the textured region is doped with a dopant to form an electrical back surface field.

15. The device of claim 14, wherein the electrical back surface field has been doped by a technique selected from the group consisting of laser doping, ion implanting, diffusion doping, in situ doping, and combinations thereof.

16. The device of claim 15, wherein the textured region has a higher dopant concentration than the semiconductor layer.

17. The device of claim 15, wherein the dopant has the same polarity as the semiconductor layer.

18. The device of claim 15, wherein the dopant is a member selected from the group consisting of boron, indium, gallium, arsenic, antimony, phosphorus, and combinations thereof.

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19. The device of claim 2, wherein the semiconductor layer is doped with a dopant to form an electrical back surface field, and wherein the electrical back surface field is distinct from the textured region.

20. The device of claim 2, further comprising at least one photodiode optically active region disposed on the device surface.

21. The device of claim 2, wherein the photodiode optically active region comprises a doped region.

22. The device of claim 2, wherein the device forms at least one photodetector.

23. The device of claim 22, wherein the at least one photodetector is a plurality of photodetectors arranged in an array.

24. The device of claim 23, wherein the textured region is arranged in a discontinuous pattern that corresponds spatially to the array of photodetectors.

25. The device of claim 23, further comprising a plurality of isolation features in at least the semiconductor layer to isolate each photodetector in the array of photodetectors, wherein the isolation features isolate each photodetector electrically, optically, or both electrically and optically.

26. The device of claim 23, further comprising at least one optical lens associated with the at least one photodetector.

27. The device of claim 23, further comprising at least one color filter associated with the at least one photodetector.

28. A method of making a semiconductor device, comprising:

texturing at least a portion of a surface of a semiconductor layer to form a textured region;

depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric

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layer; and

wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate.

29. The method of claim 28, wherein the semiconductor layer is an epitaxially grown semiconductor layer.

30. The method of claim 29, wherein texturing at least a portion of a surface of a semiconductor layer to form a textured region further includes:

forming the epitaxially grown semiconductor layer on a growth substrate; and

texturing at least a portion of a surface of the epitaxially grown semiconductor layer to form a textured region.

31. The method of claim 30, further comprising removing the growth substrate to expose the epitaxially grown semiconductor layer.

32. The method of claim 28, further comprising forming an epitaxially grown semiconductor layer on the semiconductor layer on an opposite side from the textured region.

33. The method of claim 28, wherein wafer bonding further includes:

depositing a polysilicon layer on the first dielectric layer; and

bonding the polysilicon layer between the first dielectric layer and the second dielectric layer.

34. The method of claim 33, further comprising doping at least a portion of the polysilicon layer.

35. The method of claim 28, wherein texturing at least a portion of a surface of the semiconductor layer to form the textured region further includes:

forming an opening in the semiconductor substrate, the second dielectric layer, and the first dielectric layer to expose a portion of the semiconductor layer; and

texturing at least a portion of the exposed portion of the semiconductor layer to form the textured region.

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36. The method of claim 28, wherein texturing includes a technique selected from the group consisting of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.

37. The method of claim 28, wherein texturing includes lasing.

38. A method of protecting a textured region from contamination during manufacture of a semiconductor device, comprising:

texturing at least a portion of a surface of a semiconductor layer to form a textured region;

depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the dielectric layer; and

wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate, wherein the textured region is protected from contamination during further manufacturing processes by the semiconductor layer and the semiconductor substrate.

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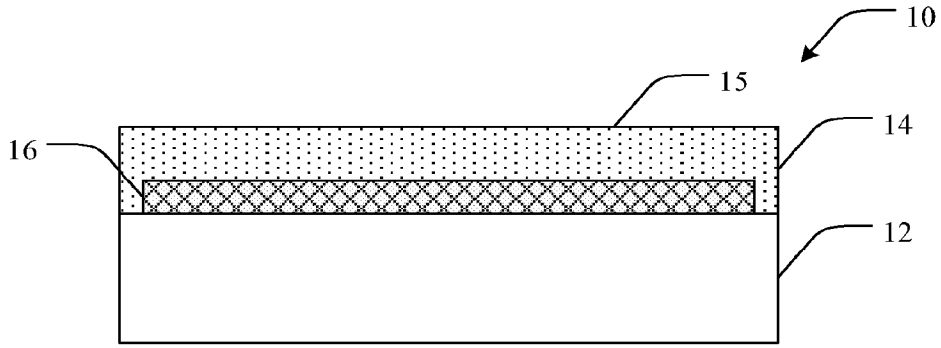

FIG. 1

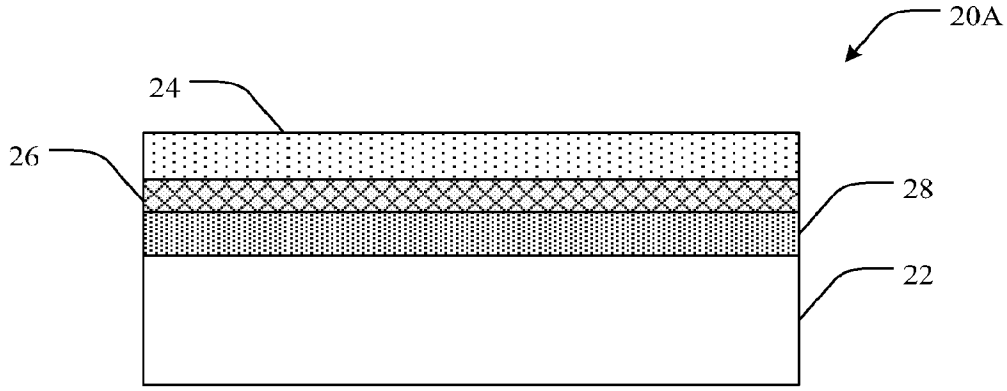

FIG. 2A

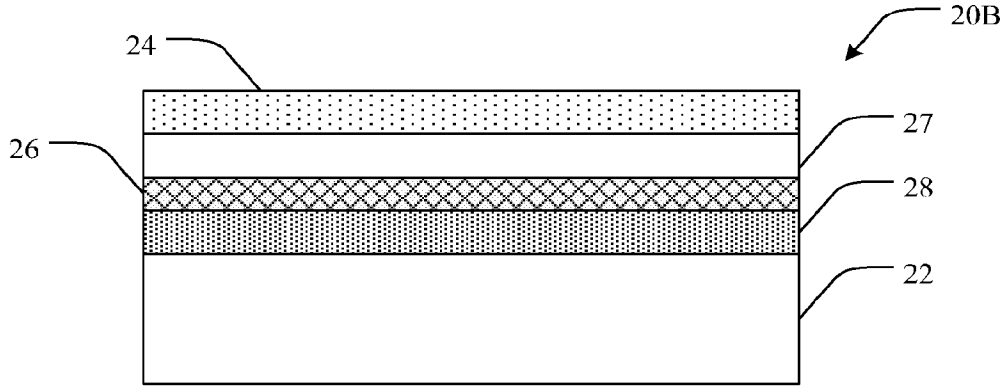

FIG. 2B

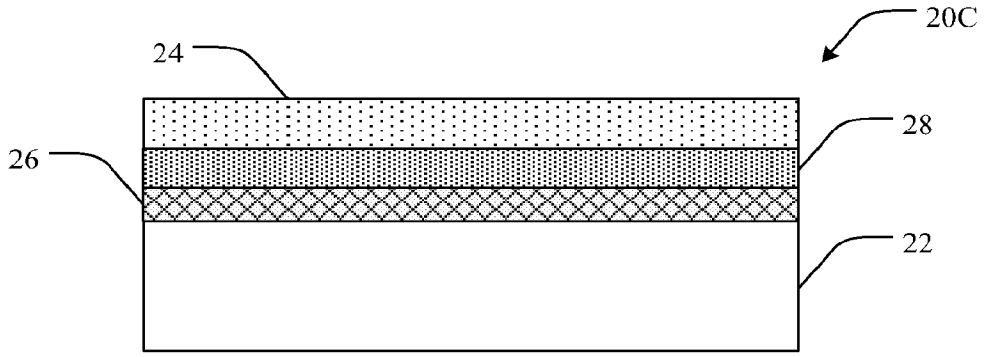

FIG. 2C

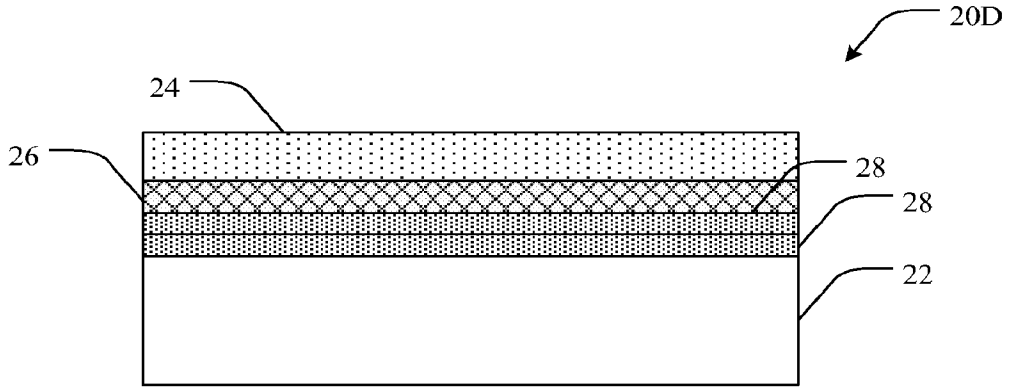

FIG. 2D

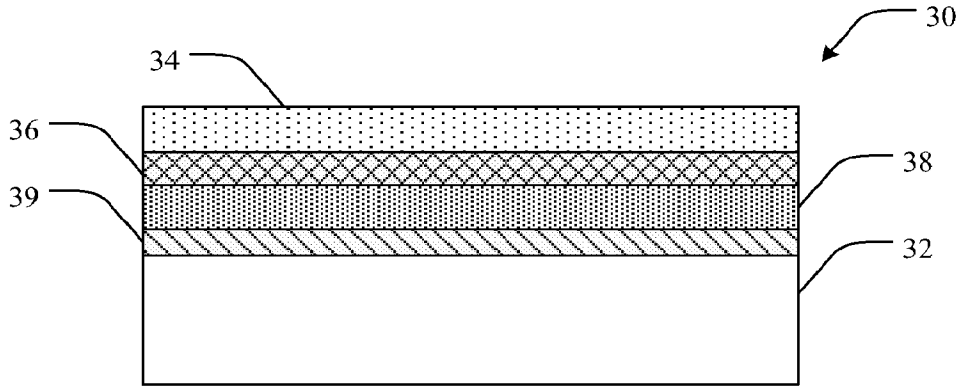

FIG. 3

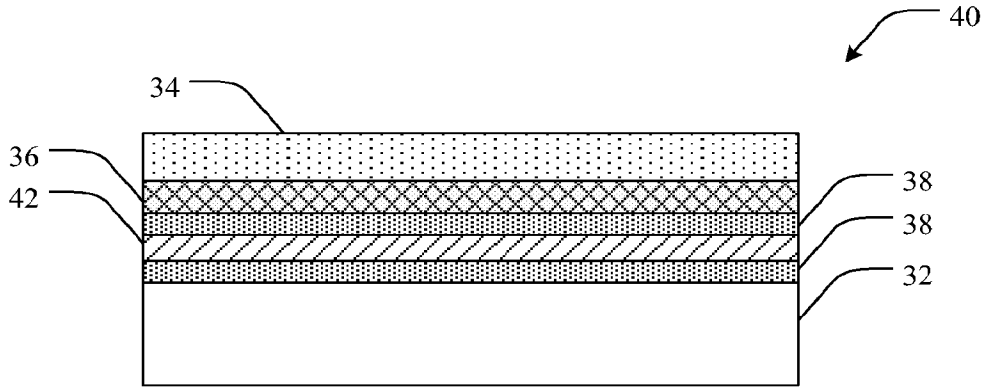

FIG. 4

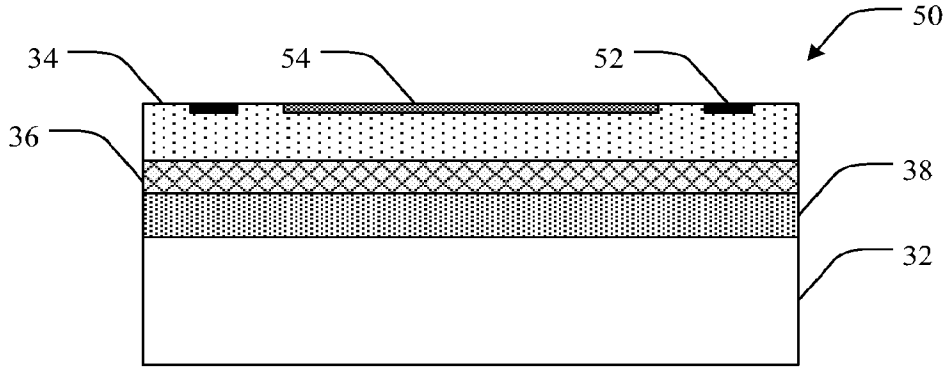

FIG. 5

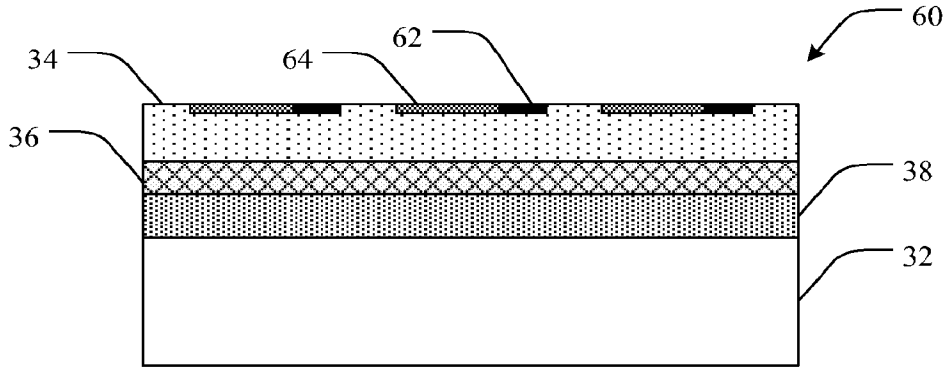

FIG. 6

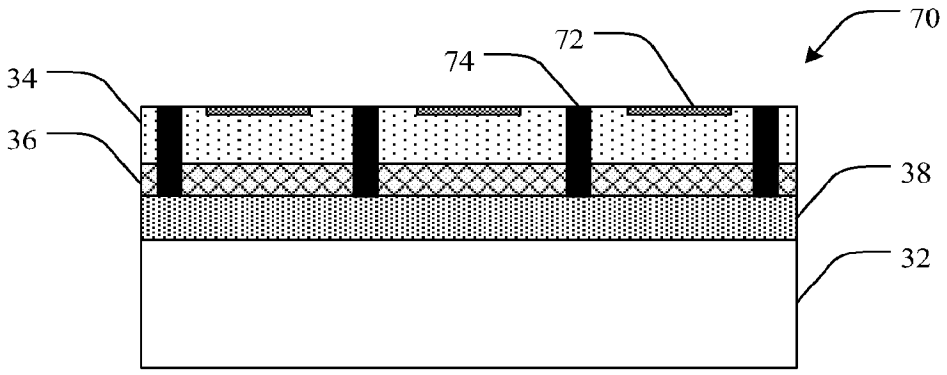

FIG. 7

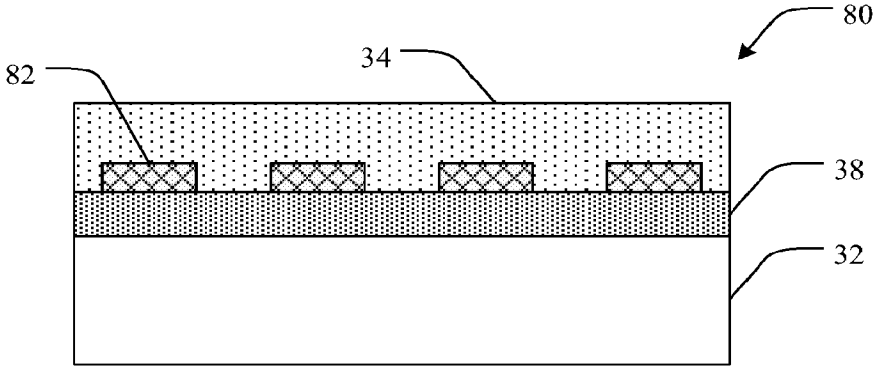

FIG. 8

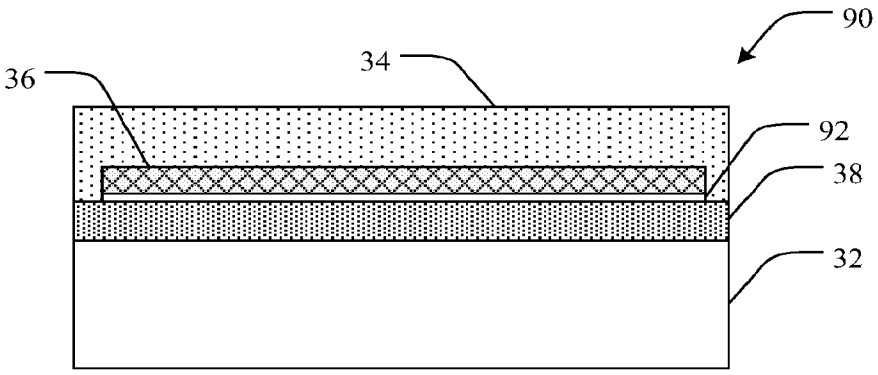

FIG. 9

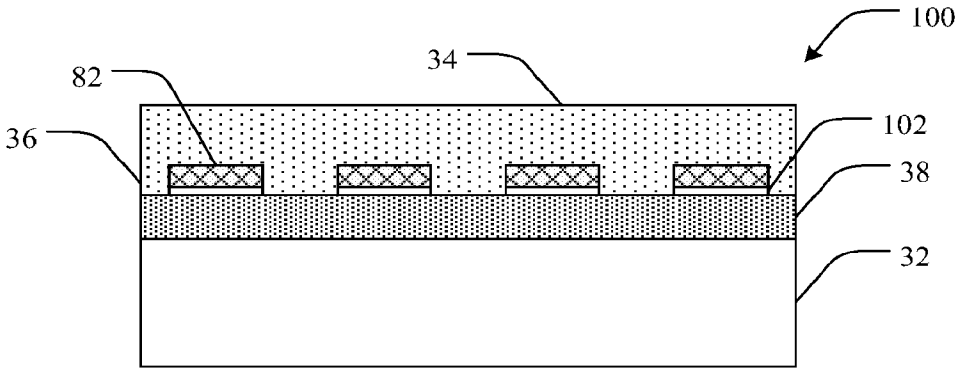

FIG. 10

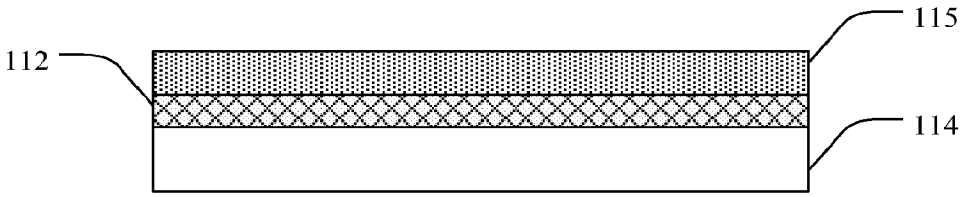

FIG. 11A

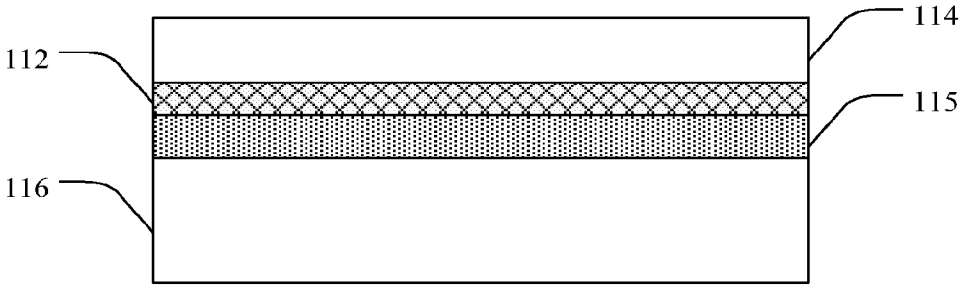

FIG. 11B

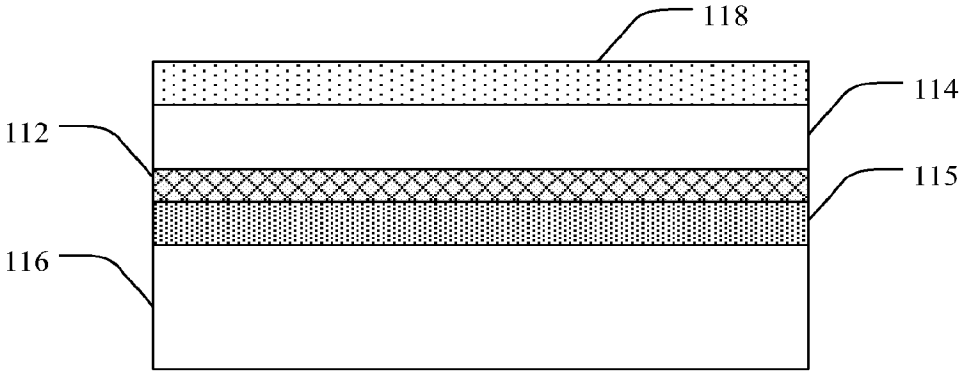

FIG. 11C

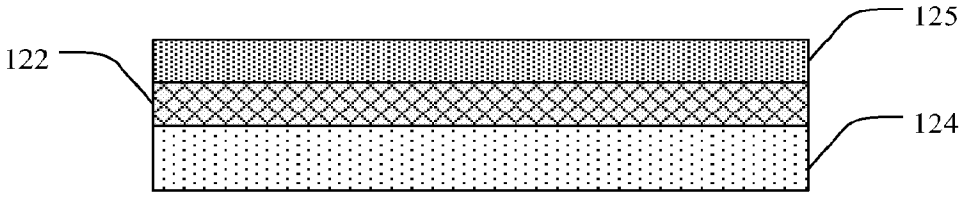

FIG. 12A

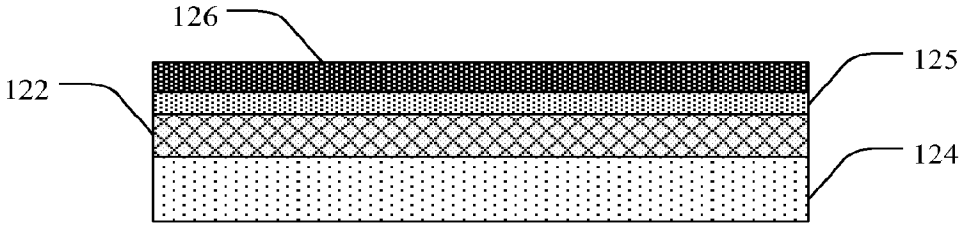

FIG. 12B

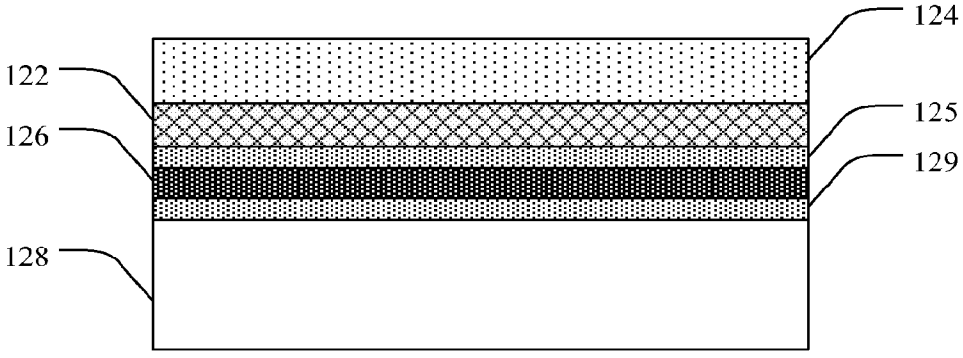

FIG. 12C

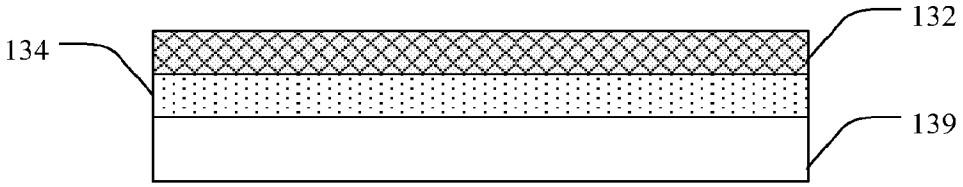

FIG. 13A

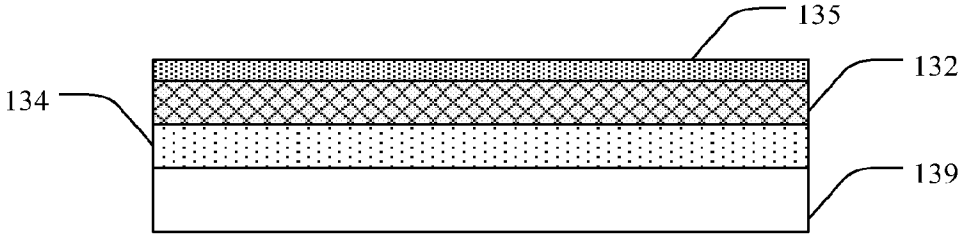

FIG. 13B

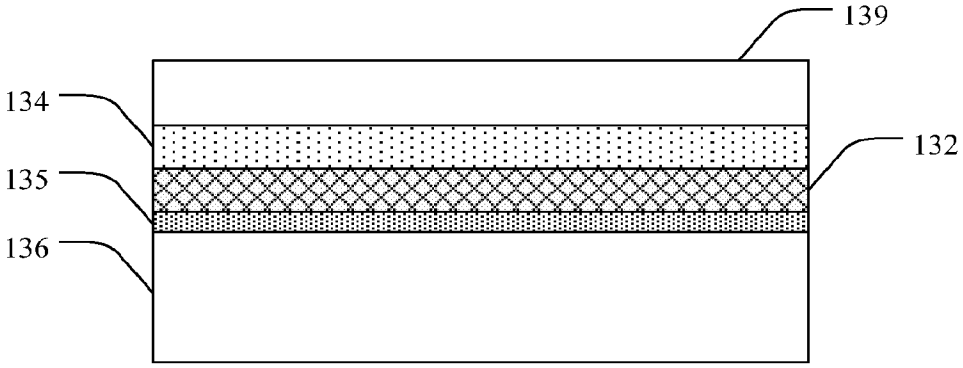

FIG. 13C

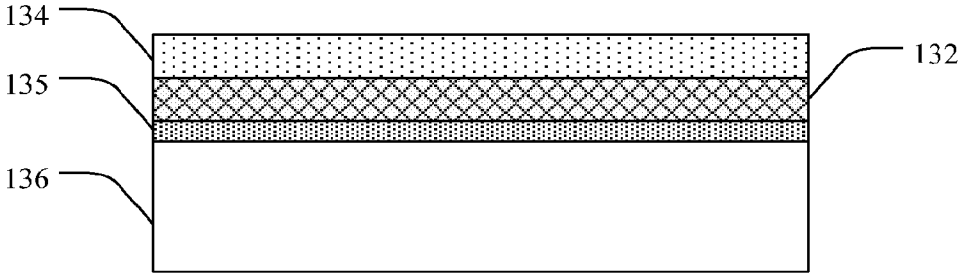

FIG. 13D

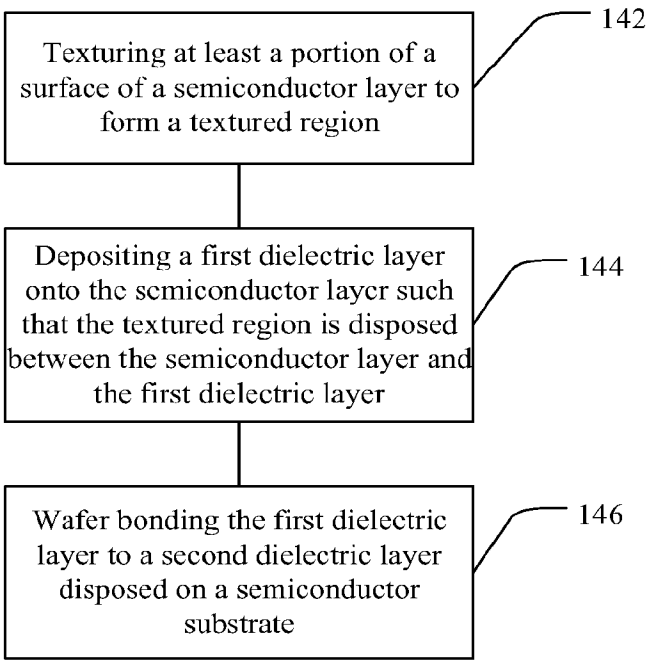
Texturing at least a portion of a surface of a semiconductor layer to form a textured region
142
Depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer
144
Wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate
146

FIG. 14

Electronic Acknowledgement Receipt

EFS ID:	26426350
Application Number:	15216244
International Application Number:	
Confirmation Number:	5052
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	136549
Filer:	Reza Mollaaghababa/Jillian Stockel
Filer Authorized By:	Reza Mollaaghababa
Attorney Docket Number:	143705.05221
Receipt Date:	22-JUL-2016
Filing Date:	
Time Stamp:	11:19:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Foreign Reference	JPH06275641.pdf	296929 d60269e8faca202867f9294c16eb025e3799e501	no	6

Warnings:

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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	26426659
Application Number:	15216244
International Application Number:	
Confirmation Number:	5052
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	136549
Filer:	Reza Mollaaghababa/Jlllian stockel
Filer Authorized By:	Reza Mollaaghababa
Attorney Docket Number:	143705.05221
Receipt Date:	22-JUL-2016
Filing Date:	
Time Stamp:	11:34:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	Arndt_1975.pdf	5226628 0d0185ac7fc60ac7348695ec7d6a14dd79478a48	no	4

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8	Foreign Reference	Borghesi_1995.pdf	21304314 9eacafa33b7b3f077cb834f0944ef1e23c8d3e0f	no	76
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9	Foreign Reference	Born_1999.pdf	490424 4c34933101608eab317d17662c7610be44b57870	no	10
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18	Non Patent Literature	Carey_2004_HarvardThesis.pdf	1509556 0f0dc525c09bdca5e36ec430a972810b77f852c1	no	162
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19	Non Patent Literature	Chang_2010.pdf	1233972 7c22e525b9c9e150f213c52f1fa4c84809a8954e	no	7
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38	Foreign Reference	Forbes_2010_BacksideNanoscale.pdf	5539706 5a8e9e26f6d2b38c34c06e59158295cc57a37983	no	4
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39	Foreign Reference	Forbes_2012_TexturingReflectivity.pdf	696945 2d051a6b663f518d45f890b52fb322c1059522d6	no	14
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51	Foreign Reference	HighPerformanceTech2004.pdf	7188181 db7e23468df8f71bc0e63250adfd2aa993c2947e	no	48
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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	26426957
Application Number:	15216244
International Application Number:	
Confirmation Number:	5052
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	136549
Filer:	Reza Mollaaghababa/Jillian Stockel
Filer Authorized By:	Reza Mollaaghababa
Attorney Docket Number:	143705.05221
Receipt Date:	22-JUL-2016
Filing Date:	
Time Stamp:	11:49:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	Joy_2007.pdf	6317763 1e7fa577eb7813813dd20ac793a934719d123ac8	no	4

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3	Non Patent Literature	Kim_2006.pdf	309524 b2f5e92604cd3d7ab9c86a71dbc6915f93339126	no	3
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35	Non Patent Literature	Pain_2009.pdf	797555 99c2b23f735387b1206552f23ea2a51e0b82fbea	no	23
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36	Non Patent Literature	Payne_2010.pdf	1457070 6a2c938f8676532cb21c25fea10cd0ea1223d44d	no	5
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37	Non Patent Literature	Pedraza_1999_AppliedPhysicsLtrs.pdf	725054 b8cee7b67b96749802bfbd3afe33793138fa9b5f	no	8
Warnings:					
Information:					
38	Non Patent Literature	Pedraza_2003_AppliedPhysicsA.pdf	725054 b8cee7b67b96749802bfbd3afe33793138fa9b5f	no	8
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39	Non Patent Literature	Rashkeev_2001.pdf	4725777 741a9b26114e89792107925fcc74aca6470de0f3	no	3
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40	Non Patent Literature	Russell_1989.pdf	485495 24ab2d32fc8e7a506a601c31ec6829490aaa0269	no	6
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41	Non Patent Literature	Russell_2003_SSCPacific.pdf	974057 7338b26469e9a0345bc218fb1b717f0fba724259	no	6
Warnings:					
Information:					
42	Non Patent Literature	Sai_2008.pdf	6207622 4c70bde62df23f4549aa8315679a2fda361a184d	no	3
Warnings:					
Information:					
43	Non Patent Literature	Sanchez_1996_Whiskerlike.pdf	5134904 2d2c9ece091fb35e9609e605f7e56d8ddcd35406	no	3
Warnings:					
Information:					

44	Non Patent Literature	Sanchez_1998_DynamicsOfThe.pdf	4810445 896cc8a084a80dff6bfa6931b30e3a7dcf81f182	no	4
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Information:					
45	Non Patent Literature	Sarnet_2008.pdf	2704794 8657bc415f08f3b20ac5dc9c4c60630485b471c9	no	15
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Information:					
46	Non Patent Literature	Senoussaoui_2003.pdf	1261403 b3960f68513cda8cf304626a23894b38ca854b63	no	5
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Information:					
47	Non Patent Literature	Serpenguzel2004.pdf	275277 68003afce7ba9e340e3533e45ed944882a39ed99	no	9
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48	Non Patent Literature	Shen_2007.pdf	347566 f2406eacdb44ce08e3940ef97ddfb93724789a50	no	3
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49	Non Patent Literature	SolarEnergyResearchInstitute_1984.pdf	12512054 78cfed4b5537043952fdf10b9f981d6592c30d29	no	10
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50	Non Patent Literature	Solhusvik_2009.pdf	5934788 9e030d00bc3754335b1b09d8a366bc18a55d13ec	no	3
Warnings:					
Information:					

51	Non Patent Literature	Stone_2001.pdf	10391786 fd946586593fa5ad2ce1300a6f24de893a5dcb10	no	6
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52	Non Patent Literature	Szlufcik1991.pdf	799386 c5d0c30e5063740935704a9deeff9ab29008c41a	no	3
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Information:					
53	Non Patent Literature	Tabbal_2007.pdf	527746 a0b82bd850fbee796872187b5fda4e60f8f986c1	no	6
Warnings:					
Information:					
54	Non Patent Literature	Takayanagi_2007.pdf	1294056 ed844f4cb85c12e1b0fdca0022967f85234f0ca2	no	4
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55	Non Patent Literature	Tower_2003.pdf	2310811 eba3d772edb3a8407054a5100b887df095969f51	no	7
Warnings:					
Information:					
56	Non Patent Literature	Tull_2007.pdf	8153883 037c360c382fc2b9bf47362776b2da2b1d7a52aa	no	174
Warnings:					
Information:					
57	Non Patent Literature	Uehara_2004.pdf	480240 e4bc10071ad2c99e3f1f89dd6465a3101df930c9	no	6
Warnings:					
Information:					

58	Non Patent Literature	Wilson_1984.pdf	2049764 94f5694e894ac0ad75200a7faa4ddb5a0885132b	no	5
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59	Non Patent Literature	Winderbaum_1997.pdf	8729122 9319f5b306628ebc2e8589da04e30f5336174832	no	10
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Information:					
60	Non Patent Literature	Wu_1999_APSCentennialMeeting.pdf	5020631 58fc0cf21a7da2ea09d0d8f84f73889a92d4710b	no	36
Warnings:					
Information:					
			Total Files Size (in bytes):	228943175	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	26427090
Application Number:	15216244
International Application Number:	
Confirmation Number:	5052
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	136549
Filer:	Reza Mollaaghababa/Jillian Stockel
Filer Authorized By:	Reza Mollaaghababa
Attorney Docket Number:	143705.05221
Receipt Date:	22-JUL-2016
Filing Date:	
Time Stamp:	11:55:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	Wu_2000_Thesis.pdf	5410273 6fd36a6c384a92d1ae9e5cfe85571a725a43d659	no	138

Warnings:

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Information:					
2	Non Patent Literature	Wu_2001_AppliedPhysicsLetterVol78.pdf	361848 e8f4a9215584d7f12d792e893bb335c965930908	no	3
Warnings:					
Information:					
3	Non Patent Literature	Wu_2002_AppliedPhysicsLetterVol81.pdf	291419 b60e60b201a7b431540d1bce3bdd3a8b749d8946	no	3
Warnings:					
Information:					
4	Non Patent Literature	Wu_BlackSilicon_1999.pdf	4227673 2bb6a45c93823c3b50a73852894adf51c931267a	no	40
Warnings:					
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5	Non Patent Literature	Xu_1993.pdf	12016946 54790907dc94a867bbae847d9f2822435f6c4bc0	no	9
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6	Non Patent Literature	Yablonovitch_1982.pdf	1273767 a8def6fed8fe5508e6ec06b9cc9362c738a746ce	no	6
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7	Non Patent Literature	Younkin_2003_JournalOfAppliedPhysicsVol93.pdf	325011 838dec3f7c57b9f19cd4066c297850246bb9a856	no	4
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Information:					
8	Non Patent Literature	Younkin_2001_Thesis.pdf	5144732 1f0e3703a2b18be1ab76bd3dd7c21651f222721c	no	136
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Information:					

9	Non Patent Literature	Yamamoto_2010.pdf	421949 effa345fb9f171099ecb37b26501e0d038296e7d	no	4
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11	Non Patent Literature	Yasutomi_2009.pdf	238518 7dd16cbccbd8fdba5a76a7d409d7f6ffa0b71bd6	no	4
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Information:					
12	Information Disclosure Statement (IDS) Form (SB08)	Yuan_2009_AppliedPhysicsLetters.pdf	414073 38ba48c35faa2e90282720908d4cca24d895ea69	no	3
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Information:					
This is not an USPTO supplied IDS fillable form					
13	Non Patent Literature	Zaidi_2000.pdf	1086636 0ac5f6c1490b85075cc6d3e4a1e0a361d04fa132	no	4
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14	Non Patent Literature	Zhang_1996.pdf	814553 27f139c127e7023b37d9b18e8605ef9769f1d680	no	10
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Information:					
15	Non Patent Literature	Zhu_2004.pdf	669226 c1232928e940617b23d88819971bf6e7f56d4fe8	no	7
Warnings:					
Information:					
			Total Files Size (in bytes):	34436043	

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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/216,244

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	26 minus 20 =	* 6			OR	x 80 =	480
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2080

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/216,244	07/21/2016	2852	2080	143705.05221	26	2

CONFIRMATION NO. 5052

FILING RECEIPT

136549
Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

OC000000084850118

Date Mailed: 08/05/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Martin U. Pralle, Wayland, MA;
Jeffrey McKee, Tualatin, OR;
Jason Sickler, Arlington, MA;

Applicant(s)

SiOnyx, LLC., Beverly, MA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 14/747,875 06/23/2015
which is a CON of 13/841,120 03/15/2013 PAT 9064764
which claims benefit of 61/614,275 03/22/2012

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

SAMSUNG EX. 1002 - 1678/2862

If Required, Foreign Filing License Granted: 08/03/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/216,244**

Projected Publication Date: 11/10/2016

Non-Publication Request: No

Early Publication Request: No
Title

Pixel Isolation Elements, Devices and Associated Methods

Preliminary Class

396

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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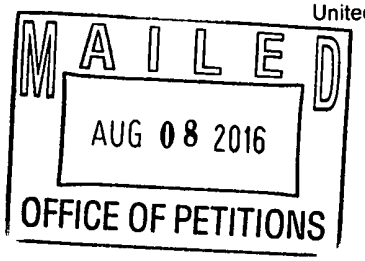

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston MA 02110-2736

Doc Code: TRACK1.GRANT

Decision Granting Request for Prioritized Examination (Track I or After RCE)	Application No.: 15/216,244

1. THE REQUEST FILED July 21, 2016 IS **GRANTED.**

The above-identified application has met the requirements for prioritized examination
- A. ☒ for an original nonprovisional application (Track I).
- B. ☐ for an application undergoing continued examination (RCE).

2. **The above-identified application will undergo prioritized examination.** The application will be accorded special status throughout its entire course of prosecution until one of the following occurs:

- A. filing a **petition for extension of time** to extend the time period for filing a reply;
- B. filing an **amendment to amend the application to contain more than four independent claims, more than thirty total claims**, or a multiple dependent claim;
- C. filing a **request for continued examination**;
- D. filing a notice of appeal;
- E. filing a request for suspension of action;
- F. mailing of a notice of allowance;
- G. mailing of a final Office action;
- H. completion of examination as defined in 37 CFR 41.102; or
- I. abandonment of the application.

Telephone inquiries with regard to this decision should be directed to Brian W. Brown at 571-272-5338.

/Brian W. Brown/
[*Signature*]

Petitions Examiner, Office of Petitions
(Title)

SAMSUNG EX. 1002 - 1681/2862

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/216,244	07/21/2016	Martin U. Pralle	143705.05221	5052

136549 7590 09/13/2016

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
09/13/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketingbn@pepperlaw.com
davisdr@pepperlaw.com

SAMSUNG EX. 1002 - 1682/2862

Office Action Summary	Application No. 15/216,244	Applicant(s) PRALLE ET AL.	
	Examiner LONG PHAM	Art Unit 2814	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *34-59* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) *34-59* are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Election/Restrictions

This application contains claims directed to the following patentably distinct species: embodiment or species 1 of fig. 1, embodiment or species 2 of fig. 2, embodiment or species 3 of fig. 3, embodiment or species 4 of fig. 4, embodiment or species 5 of fig. 5, embodiment or species 6 of fig. 6, embodiment or species 7 of fig. 7. The species are independent or distinct because **the patentability or unpatentability of one species does not necessarily imply the patentability or unpatentability of another species**. In addition, these species are not obvious variants of each other based on the current record.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species, or a single grouping of patentably indistinct species, for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no independent claim appears to be generic to other independent claims.

There is a search and/or examination burden for the patentably distinct species as set forth above because at least the following

reason(s) apply: **The searches of the patentably distinct species are not co-extensive**.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected species or grouping of patentably indistinct species**, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species or grouping of patentably indistinct species.

Should applicant traverse on the ground that the species, or groupings of patentably indistinct species from which election is

required, are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing them to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.A telephone call was made to -- on -- to request an oral election to the above restriction requirement, but did not result in an election being made.

The examiner has required restriction between product or apparatus claims and process claims. Where applicant elects claims directed to the product/apparatus, and all product/apparatus claims are subsequently found allowable, withdrawn process claims that include all the limitations of the allowable product/apparatus claims should be considered for rejoinder. All claims directed to a nonelected process invention must include all the limitations of an allowable product/apparatus claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product/apparatus claims and the rejoined process claims

will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product/apparatus are found allowable, an otherwise proper restriction requirement between product/apparatus claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product/apparatus claim will not be rejoined. See MPEP § 821.04. Additionally, in order for rejoinder to occur, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product/apparatus claims. **Failure to do so may result in no rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LONG PHAM whose telephone number is (571)272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached

on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

/LONG PHAM/
Primary Examiner, Art Unit 2814

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15216244	PRALLE ET AL.
	Examiner	Art Unit
	LONG PHAM	2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/07/2016								
	34	÷								
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/216,244	07/21/2016	Martin U. Pralle	143705.05221

CONFIRMATION NO. 5052

136549
Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

PUBLICATION NOTICE

OC000000087132890

Title: Pixel Isolation Elements, Devices and Associated Methods

Publication No.US-2016-0329366-A1
Publication Date:11/10/2016

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

SAMSUNG EX. 1002 - 1690/2862

Docket No.: 143705.05221

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Martin U. Pralle Application No.: 15/216,244 Filed: July 21, 2016 For: PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS	Confirmation No.: 5052 Art Unit: 2814 Examiner: Pham, Long

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Certificate of Mailing

I hereby certify that this correspondence is being electronically filed via EFS-Web to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

November 11, 2016 — Dated

Electronic Signature: /Andrew W. Schultz/
Andrew Schultz, Reg. No. 66,869

RESPONSE TO RESTRICTION REQUIREMENT

Dear Sir:

This paper is filed in response to the Restriction Requirement dated September 13, 2016.

Amendments to the Claims begin on page 2.

Remarks begin on page 6.

AMENDMENTS TO THE CLAIMS

1-33. (Canceled)

34. (Previously Presented) A light trapping device, comprising:

at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending at least partially around the pixel periphery;

a backside light trapping material substantially covering the backside surface; and

a peripheral light trapping material substantially covering the peripheral sidewall,

wherein the peripheral light trapping material creates a surface field at the peripheral sidewall.

35. (Previously Presented) The device of claim 34, wherein the backside light trapping material reflects the light incident thereon back into the pixel.

36. (Previously Presented) The device of claim 34, wherein the peripheral light trapping material reflects light incident thereon into the pixel.

37. (Previously Presented) The device of claim 34, wherein the peripheral sidewall extends completely around the pixel periphery.

38. (Previously Presented) The device of claim 34, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

39. (Previously Presented) The device of claim 34, wherein the peripheral sidewall extends through the pixel substantially from the light incident surface to the backside surface.

40. (Previously Presented) The device of claim 34, wherein at least one of the backside light trapping material and the peripheral light trapping material comprises a metal layer.

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41. (Previously Presented) The device of claim 34, wherein said peripheral light trapping material comprises an oxide.

42. (Previously Presented) The device of claim 34, wherein said peripheral light trapping material provides a passivating negative charge.

43. (Previously Presented) The device of claim 34, wherein said peripheral light trapping material exhibits a surface recombination velocity as low as 10 cm/s.

44. (Previously Presented) The device of claim 34, wherein the peripheral sidewall material has an index of refraction of less than about 2.1.

45. (Previously Presented) The device of claim 34, wherein the peripheral light trapping material comprises any of aluminum oxide and hafnium oxide.

46. (Previously Presented) The device of claim 34, wherein said pixel comprises a textured region.

47. (Previously Presented) The device of claim 46, wherein said textured region is coupled to the light incident surface.

48. (Previously Presented) The device of claim 47, wherein said textured region is located on said light incident surface.

49. (Previously Presented) The device of claim 47, wherein said textured region comprises a textured film layer.

50. (Previously Presented) The device of claim 49, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.

51. (Previously Presented) An array of light trapping pixel devices of claim 34.

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52. (Previously Presented) A light trapping device, comprising:

at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending at least partially around the pixel periphery;

a backside light trapping material at least partially covering the backside surface;

a peripheral light trapping material substantially covering the peripheral sidewall; and

a textured region positioned to interact with light incident thereon so as to increase quantum efficiency of the device.

53. (Previously Presented) The device of claim 52, wherein said backside light trapping material substantially covers the backside surface.

54. (Previously Presented) The device of claim 52, wherein said textured region is located on the light incident surface.

55. (Previously Presented) The device of claim 52, wherein said textured region is a textured film layer coupled to the light incident surface.

56. (Previously Presented) The device of claim 55, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.

57. (Previously Presented) The device of claim 52, wherein said textured region reflects at least a portion of light internally incident thereon into the pixel.

58. (Previously Presented) The device of claim 52, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

59. (Previously Presented) The device of claim 34, wherein the peripheral sidewall extends through the pixel substantially from the light incident surface to the backside surface.

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60. (New) The device of claim 52, wherein the textured region is formed by one of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.

61. (New) The device of claim 52, wherein the textured region is formed by lasing.

62. (New) The device of claim 52, further comprising at least one doped region disposed on at least one of the light incident surface and the backside surface.

63. (New) The device of claim 46, wherein the textured region is formed by one of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.

64. (New) The device of claim 46, wherein the textured region is formed by lasing.

65. (New) The device of claim 34, further comprising at least one doped region disposed on at least one of the light incident surface and the backside surface.

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REMARKS

The outstanding Action subjects pending claims 34-59 to a Restriction Requirement. Specifically, the outstanding Action requires election of one of the following species: Species 1 (Figure 1); Species 2 (Figure 2); Species 3 (Figure 3); Species 4 (Figure 4); Species 5 (Figure 5); Species 6 (Figure 6); and Species 7 (Figure 7).

Applicant elects, with traverse, Species 4 for continued prosecution. Claims 34-59 are believed to read on the elected species and are thus subject to examination. Applicant's election should not be construed as Applicant's acceptance of the species grouping as alleged in the Restriction Requirement. To the extent that Species 1-7 include characteristics that are not mutually exclusive, Applicant believes that the requirement for the election of species is improper. Further, reconsideration and withdrawal of the requirement for a species election is requested insofar as the limited number of indicated species demonstrate that it would not be unduly burdensome for the Office to conduct a search covering the claims directed to all of the identified species.

New Claims

As shown above, Applicant submits herewith new claims 60-65. Support for these claims can be found throughout the published application, for example, at paragraphs [0011], [0039], and [0068]. Applicant believes that new claims 60-65 read on the elected species and are thus subject to examination.

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Conclusion

The Director is authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 500436, under Docket No. 143705.05221.

Respectfully submitted,

Dated: November 11, 2016

Electronic Signature: /Andrew W. Schultz/

Andrew W. Schultz, Reg. No. 66,869
Attorney for Applicant
Pepper Hamilton LLP
125 High Street
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Boston, MA 02210
Tel: (617) 204-5176
Fax: (617) 204-5150

SAMSUNG EX. 1002 - 1697/2862

Electronic Patent Application Fee Transmittal

Application Number:	15216244
Filing Date:	21-Jul-2016
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Filer:	Andrew W. Schultz
Attorney Docket Number:	143705.05221

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	6	80	480
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**480**

Electronic Acknowledgement Receipt

EFS ID:	27473729
Application Number:	15216244
International Application Number:	
Confirmation Number:	5052
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	136549
Filer:	Andrew W. Schultz
Filer Authorized By:	
Attorney Docket Number:	143705.05221
Receipt Date:	11-NOV-2016
Filing Date:	21-JUL-2016
Time Stamp:	11:45:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$480
RAM confirmation Number	111416INTEFSW11465900
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Warnings:					
Information:					
2	Foreign Reference	JP2003242125.pdf	12132549 484fee5dcca5e19f65e696ccdbf2dbd26f0b3dd3	no	25
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Information:					
3	Non Patent Literature	Bernhard_1967.pdf	1944267 624a981547fed2da979d572a4a6af24a8f610a74	no	7
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Information:					
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Information:					
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Warnings:					
Information:					
6	Non Patent Literature	Koh_2000.pdf	554663 a71c512b3b509d821356eb91d7cebdb2e7c1eec1	no	5
Warnings:					
Information:					

7	Non Patent Literature	Jansen_1995.pdf	769230 8bb71dd982d4be9f37371d8cc8e499de9091b007	no	6
Warnings:					
Information:					
8	Non Patent Literature	Zhong_2016.pdf	836181 7d538cd6d16fbdaac27992141c46adfe61f85f69	no	11
Warnings:					
Information:					
9	Foreign Reference	JPH062444444.pdf	942522 ffbfc75eb3fcfa536afcd9024b4fcf2b3d744385	no	16
Warnings:					
Information:					
10	Transmittal Letter	IDSTransmittal.pdf	93177 5374b293545cbf790c5732ec9b8d8ac261d1950b	no	2
Warnings:					
Information:					
11	Information Disclosure Statement (IDS) Form (SB08)	SB08.pdf	1036865 7bb6a35b0ee8e5cdcef1236d23bb40ec3cdfcf71	no	6
Warnings:					
Information:					
12		15216244_ResponseRR.pdf	150591 e6ca04e1748fdd97ae4112e8ad008ec239ae538b	yes	7

Multipart Description/PDF files in .zip description

Document Description	Start	End
Response to Election / Restriction Filed	1	1
Claims	2	5
Applicant Arguments/Remarks Made in an Amendment	6	7

Warnings:

Information:					
13	Fee Worksheet (SB06)	fee-info.pdf	30584 423e8558a92d08788a7a8b965cafa25c442295f5	no	2
Warnings:					
Information:					
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
G06K 9/00, H04K 1/00, H04L 9/00, G07D 7/00

A1

(11) International Publication Number: **WO 00/31679**

(43) International Publication Date: 2 June 2000 (02.06.00)

(21) International Application Number: PCT/US99/26559

(22) International Filing Date: 10 November 1999 (10.11.99)

(30) Priority Data:

09/199,369	25 November 1998 (25.11.98)	US
09/310,302	12 May 1999 (12.05.99)	US

(71) Applicant: IRISCAN, INC. [US/US]; Suite E, 9 East Stow Road, Marlton, NJ 08053–3159 (US).

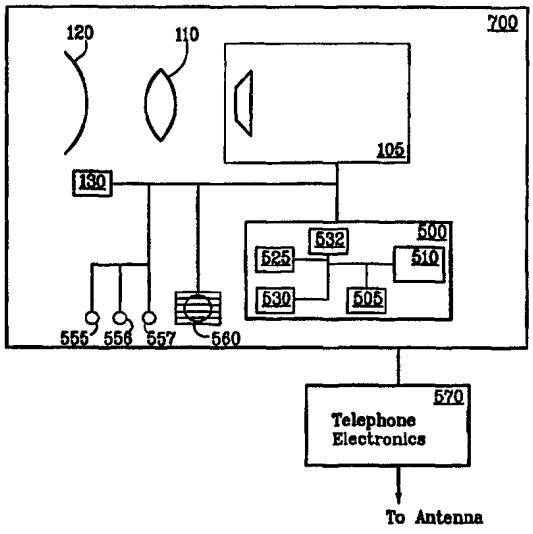
(72) Inventors: MUSGRAVE, Clyde; 3620 Fairfield Place, Frisco, TX 75035 (US). CAMBIER, James, L.; 10 Holly Drive, Medford, NJ 08055 (US).

(74) Agents: DONOHUE, John, P., Jr. et al.; Woodcock Washburn Kurtz Mackiewicz & Norris LLP, 46th floor, One Liberty Place, Philadelphia, PA 19103 (US).

(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: IRIS IMAGING TELEPHONE SECURITY MODULE AND METHOD



(57) Abstract

A compact handheld imaging apparatus (700) which can be used to capture high–quality iris images for identification of a person. The handheld iris imager is non–invasive and non–contacting and comprises a camera (105), a cold mirror (120), a lens (110), and an illuminator (130). The imager has sensors and indicators (555, 556, 557, 560) which assist a user in aligning and focusing the device. The imager also automatically captures the image when proper positioning is achieved. A template of the image is then compared to a database of previously stored templates of images to identify the person. The imager is integrated into a telecommunications device as a security module. The telecommunications device cannot be unlocked and used unless a user has been identified and authorized by the imager.

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IRIS IMAGING TELEPHONE SECURITY MODULE AND METHOD

RELATED APPLICATION DATA

The present application is a continuation-in-part application of U.S. Patent Application Serial Number 09/199,369, having a filing date of November 25, 1998.

FIELD OF THE INVENTION

The present invention relates in general to identification of physical characteristics of a human being or other animal. More particularly, the present invention relates to iris recognition.

BACKGROUND OF THE INVENTION

Various technologies are used for uniquely identifying a person in accordance with an examination of particular attributes of either the person's interior or exterior eye. One of these technologies involves the visual examination of the particular attributes of the exterior of the iris of at least one of the person's eyes. The iris of the human eye has random patterns of striations, ciliary processes, crypts, rings, furrows and other features which had been shown capable of generating highly unique biometric templates for personal identification. In this regard, reference is made to U.S. Patent No. 4,641,349, "Iris Recognition System", issued to Flom et al., and U.S. Patent No. 5,291,560, "Biometric Personal Identification System Based on Iris Analysis", issued to Daugman. As made clear

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by these patents, the visible texture of a person's iris can be used to distinguish one person from another with great accuracy. Thus, iris recognition can be used for such purposes as controlling access to a secure facility or a bank automatic teller machine, for example. An iris recognition system involves the use of an imager to video image the iris of each person attempting access, and image processing means for comparing this iris video image with a reference iris image on file in a database.

Iris identification systems have been developed that are capable of collecting images of the iris and processing them to produce biometric templates. These templates may be used to identify individual irises with extremely low error rates, on the order of 1 in 10^{78}. The systems capture the iris images using stationary optical platforms that are often large, complex, and expensive. The systems are difficult to use with minimal cooperation of the subject being identified. As a result their usefulness in many applications is limited.

The cellular telephone industry each year loses an estimated $650 million to cellular fraud, principally due to cloning of cellular telephones. Cloning involves re-programming a phone's electronic serial number and telephone number to those stolen from a legitimate subscriber. To counteract cloning, some service providers have utilized personal authentication techniques such as personal identification numbers (PIN) or voice verification to verify that the authorized subscriber is using the phone. This is unreliable because PIN number can be stolen or forgotten, and voice verification messages may be recorded.

Although the art of human recognition systems is well developed, there remain some problems inherent in this technology, particularly the lack of an iris imager and security module suitable for integration into a cellular telephone, and the lack of a method for using biometric information for enabling access to the cellular network. Therefore, a need exists for a recognition system that overcomes the drawbacks of the prior art.

SUMMARY OF THE INVENTION

The present invention is directed to a telecommunications device comprising a telephone security module comprising: iris acquisition means having a front surface for obtaining an image of an iris of an eye; a lens having a image plane disposed in front of the

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front surface of the iris acquisition means; a mirror disposed on a side of the lens opposite the iris acquisition means; an illuminator disposed along a side of the mirror; a memory for storing an iris image obtained by the iris acquisition means; a processor for extracting a template from the stored iris image; and a communications interface for transmitting the template to a central station.

According to one aspect of the invention, the iris acquisition means comprises a camera, and the mirror is a cold mirror. The camera is sensitive to light having a wavelength in a range between about 400 nm and about 1100 nm. The mirror reflects light having a wavelength in a range between about 400 nm and about 700 nm and passes light having a wavelength greater than about 700 nm.

According to another aspect of the present invention, the illuminator emits light having a wavelength in a range between about 680 nm and about 900 nm towards the iris of the eye being imaged, and the eye is out of contact with the iris imaging apparatus.

According to another aspect of the present invention, the module further comprises at least a visible indicator or an audible indicator to indicate when the image of the iris has been obtained. According to another aspect of the present invention, the module further comprises a focus assessment processor coupled to the visible indicator and/or the audible indicator.

According to another aspect of the present invention, the processor unlocks a telecommunications device responsive to a signal received from the central station.

In a further embodiment within the scope of the present invention, a method of unlocking a telecommunications device responsive to the identification of a person comprises the steps of: (a) storing image information of the iris of at least one person's eye; (b) illuminating an eye of an unidentified person having an iris; (c) obtaining an image of the iris of the unidentified person; (d) determining if the image is an image of sufficient quality for a step (f) of extracting; (e) repeating steps (b) through (d) until the image of sufficient quality is obtained; (f) extracting an iris template if the image is of sufficient quality; (g) comparing the template of the obtained image with the stored image information to identify the unidentified person; and (h) unlocking the telecommunications device responsive to a result of the step of comparing. The stored image information used for

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identification can be a code or template extracted from the image, and the comparison can be performed at a central database maintained by a telephone service provider.

According to one aspect of the present invention, the method further comprises the step of activating an indicator if the image is of insufficient quality. The indicator is an audible indicator.

According to another aspect of the present invention, the method further comprises the step of activating an indicator if the image is of sufficient quality. The indicator is a visible indicator.

According to another aspect of the present invention, the method further comprises the step of activating an indicator responsive to the step of comparing. The indicator is a visible indicator.

In accordance with a further aspect of the present invention, the step of determining if the image is an image of sufficient quality comprises the step of focus assessment processing the image.

According to another aspect of the present invention, the telecommunications device is unlocked if the step of comparing identifies the person.

In a further embodiment within the scope of the present invention, a telecommunications device comprises a telephone security module comprises: iris acquisition means having a front surface for obtaining an image of an iris of an eye; a lens having a image plane disposed in front of the front surface of the iris acquisition means; a mirror disposed on a side of the lens opposite the iris acquisition means; an illuminator disposed along a side of the mirror; a first memory for storing at least one template of at least one image of an iris of at least one person's eye; a second memory for storing an iris image obtained by the iris acquisition means; a processor for extracting a template from the stored iris image; and a comparator for comparing the template from stored iris image with the at least one template to identify the person.

In another embodiment within the scope of the present invention, a telecommunications device having telephone electronics comprises a telephone security module. The telecommunications device is unlocked if an iris template of an iris image identifies the person having the iris.

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BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other aspects of the present invention will become apparent from the following detailed description of the invention when considered in conjunction with the accompanying drawings. For the purpose of illustrating the invention, there is shown in the drawings an embodiment that is presently preferred, it being understood, however, that the invention is not limited to the specific methods and instrumentalities disclosed. In the drawings:

Fig. 1 is a schematic diagram of an exemplary iris imager in accordance with the present invention;

Fig. 2A is a schematic diagram of the imager of Fig. 1 shown in greater detail;

Fig. 2B is a schematic diagram of another exemplary imager in accordance with the present invention;

Fig. 3 is a simplified flowchart of a method of operation in accordance with the present invention;

Fig. 4 is a schematic diagram of an exemplary iris image recognition system in accordance with the present invention;

Fig. 5 is a schematic diagram of an exemplary iris imager having visual and aural indicators in accordance with the present invention;

Fig. 6 is a more detailed flow chart of a method of operation in accordance with the present invention;

Fig. 7 is a schematic diagram of an exemplary iris image recognition system having a focus assessment processor in accordance with the present invention;

Fig. 8 is a schematic diagram of an exemplary iris imager incorporated into a telephone in accordance with the present invention;

Fig. 9A is an isometric view of an exemplary telecommunications iris imager and telephone in accordance with the present invention;

Figs. 9B, 9C, and 9D show rear, side, and front elevational views of another exemplary device in which the imager of the present invention can be incorporated;

Fig. 10 is a flow diagram of an exemplary method of operation of a telecommunications iris imager in accordance with the present invention; and

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Fig. 11 is a diagram of a phone and communications server in communication with each other in accordance with the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS AND BEST MODE

The present invention is directed to a compact, handheld imaging apparatus and method which can be used to capture high-quality iris images. Preferably, the imager has sensors and indicators which assist the human operator in aligning and focusing the device. The imager also automatically captures the image when proper positioning is achieved. Because it is small and compact, it is practical for integration into a cellular telephone where it is used to authenticate telephone subscribers and eliminate cellular telephone fraud. Throughout the following detailed description similar reference numbers refer to similar elements in the figures of the drawings.

Fig. 1 illustrates a preferred embodiment of the handheld imager 100 in accordance with the present invention. The exemplary handheld, non-invasive, non-contacting iris imager comprises iris acquisition means 105, an imaging lens 110, a mirror 120, an optional diopter correction lens 125, and an illuminator 130. The imager 100 is preferably powered by a standard DC supply provided by a cellular telephone.

The iris acquisition means 105 is preferably a conventional solid state video camera, such as a charged coupled device (CCD) or complementary metal oxide semiconductor (CMOS) device. A preferred camera is a 1/3 inch format, monochrome CCD board camera, such as Computar Model EM200. Preferably, the video camera 105 is sensitive to light of wavelengths in the range of about 400 nanometers to about 1100 nanometers, and is positioned so that its front surface coincides with the image plane of the lens 110 in front of it. In the preferred embodiment, the object plane of the lens is approximately 89 mm in front of the lens 110. More preferably, the lens 110 is an optical lens with approximately 14.2 mm focal length.

The mirror 120, preferably a concave cold mirror having a radius of curvature preferably about 276 mm, is disposed on the side of the lens 110 opposite the video camera 105 and creates a magnified virtual image of the iris behind the mirror 120. In the preferred embodiment, the mirror 120 reflects visible light with wavelengths in the

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range of about 400 to about 700 nanometers, and passes light having longer wavelengths, such as those in the range of about 700 to about 900 nanometers.

The illuminator 130 is positioned just outside the edge of the cold mirror 120 and is used to illuminate the iris of the subject being identified. The preferred illuminator 130 emits light having wavelengths of about 680 to about 900 nanometers. Preferably, the illuminator 130 is a miniature quartz halogen or krypton gas bulb operating at approximately 1 watt.

The imager acquires images of an iris with sufficient clarity, focus, and size for use with conventional image processing and comparison routines, preferably in less than about 3 seconds. A preferred image processing and comparison routine is described in U.S. Patent No. 5,291,560, "Biometric Personal Identification System Based on Iris Analysis", issued to Daugman, and commonly assigned with the present invention to IriScan Inc., and incorporated herein by reference. However, any processing and comparison technique can be used with the image that is acquired at the imager, such as the image pixel correlation technique described in U.S. Patent No. 5,572,596, "Automated, Non-Invasive Iris Recognition System and Method", issued to Wildes et al. and the techniques described in U.S. Patent No. 4,641,349, "Iris Recognition System", issued to Flom et al., both of which are incorporated herein by reference.

Fig. 2A shows the apparatus of Fig. 1 in greater detail. The lens 110 gives a high resolution image of the eye 150 of the user, who is positioned in front of the lens 110, so that extreme proximity between the eye 150 and the imager 100 is not required (i.e., no contact is needed between the subject and the imager 100).

The handheld iris imager comprises a solid-state image capture device and an optical system which forms an image 109 of the iris on the image capture device at the image plane of the video camera 105 and at the same time produces a virtual image 115 of the iris which the user can use to position and focus the iris image. As a result, the user can, using the same eye being imaged, see a reflected image of the iris which can be used to position the handheld imager 100 so that a good iris image (i.e., an image that can be processed and compared to those stored in a database) can be obtained.

Fig. 2A also shows an optional dioptric correction lens 125 positioned between the eye 150 and the cold mirror 120. The dioptric correction lens 125 is an

adjustable optical element which corrects for the close-range focusing ability of the individual eye, which varies from subject to subject. When the lens 125 is properly adjusted, the magnified, reflected virtual image 115 of the subject's eye appears in sharp focus to the subject at the same eye-to-mirror distance at which the subject's eye is sharply focused on the front surface of the camera. This simplifies use of the imager, because the subject simply positions the image so that the virtual image 115 of the iris appears sharply focused.

A preferred embodiment of the dioptric correction mechanism has no correction lens 125 and instead has a mechanical means (not shown) for adjusting the position of the cold mirror 120 relative to the camera lens 110. This allows the user to vary the object distance of the cold mirror 120, thus changing the eye-to-lens distance at which the virtual image 115 of the iris is sharply focused.

The ability to set the dioptric correction mechanism to accommodate a particular user has a great utility if the imager is used by only one person most of the time. Once the correction is set, the user can easily position the device to obtain a sharply focused reflected image. This automatically produces a sharply focused image from the camera and substantially immediate acceptance of the image by the focus assessment processor described below. Image capture time is thereby reduced and overall convenience and utility is enhanced.

An eye 150 is positioned in front of the imager 100 (e.g., about 3.5 inches in front), as shown in Fig. 2A, and the illuminator 130 is turned on. This, in turn, illuminates the eye 150 and the iris therein. Preferably, the light having wavelengths of about 400 to about 700 nanometers is reflected by the cold mirror 120, thereby forming a magnified virtual image 115 behind the mirror 120 which the user can see through the eye being imaged. The radius of curvature of the mirror is selected so that the magnified image 115 of the eye substantially fills the user's entire field of view. Hence, when the imager 100 is positioned so that the entire eye 150 is visible, it is virtually assured that the eye 150 will be substantially centered in the object plane 140 of the camera 105. Under these conditions, the light having wavelengths of about 700 to about 900 nanometers is passed by the mirror 120 and forms an approximately centered image 109 of the eye 150 at the

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image plane 107 of the camera 105. The image is then captured and processed, as described below.

Although a cold mirror (one which reflects shorter wavelengths and passes longer wavelengths) is described herein, it is understood that a hot mirror (one which reflects longer wavelengths and passes shorter wavelengths) could also be used in accordance with the present invention. Such a configuration is shown in an imager 101 in Fig. 2B. The eye 150 is illuminated by an illuminator 131 emitting light having wavelengths in the range of about 680 to 900 nanometers. This light is reflected by the eye 150 and the light having wavelengths in the range of about 700 to 900 nanometers is reflected by the hot mirror 121 to be focused by the lens 111 onto the front surface of the camera 106. Light reflected from the eye 150 having shorter (visible) wavelengths in the range of about 400 to 700 nanometers passes through the hot mirror 121 and strikes a concave broadband mirror 122 which reflects light having wavelength from about 400 to 900 nanometers. This light forms a virtual image 115 of the eye 150 behind the concave mirror 122 that the user can see and use to align and focus the device, as described below.

The imager 100 of Figs. 1 and 2A, as well as the imager of Fig. 2B, is used in a system to identify the iris image that has been captured. As shown in Fig. 3, the eye is illuminated at step 160, and an acceptable or suitable image of the iris is obtained at step 165. The image is processed to extract an iris template or code at step 170, the template or code is encrypted (optional) and transmitted to the cellular provider (such as a central station; e.g., a Mobile Telephone Switching Office) at step 175, and the template or code is decrypted (if necessary) and compared to pre-existing templates or codes of authorized subscribers stored in a memory or database for identification and authorization of the user at step 180. If the user is authorized, the cellular provider enables the call placement at step 185. The cellular provider can either enable the call at the central station or send a signal to the telephone processor directing it to unlock the telephone.

Fig. 4 is a schematic diagram of an exemplary iris image recognition system in accordance with the present invention. The imager 100 is coupled to a microprocessor 210 that performs the processing and encryption. The microprocessor 210 resides in a cellular telephone 200.

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The microprocessor 210 is coupled to the imager 100 via conventional cables and/or printed circuit boards (PCBs) that are incorporated into the telephone 200. Other conventional means for coupling the imager 100 and the microprocessor 210 can be employed. The microprocessor 210 controls the imager 100 and runs software held in read only memory (ROM) 205. The processor 210 is connected via a bus 207 to the ROM 205, a random access memory (RAM) 232, another memory such as an erasable programmable ROM (EPROM) 230, and an input/output (I/O) controller 225. The RAM 232 is large enough to hold at least one captured image of an iris. The I/O controller 225 is connected to the appropriate circuitry and drivers (not shown) for issuing commands to control the imager 100.

The imager 100 preferably uses a digital camera and transmits digital images directly to the processing unit 210. "On/off" data is transmitted from the imager 100 to the processor 210 to initiate the image acquisition function. A digital image could be provided if a digital camera is used.

The image processing consists of a number of image processing steps (such as those described in U.S. Patent No. 5,291,560 and U.S. Patent No. 5,572,596, which are herein incorporated by reference) which lead to extraction of a unique and highly specific digital biometric template that can be used to identify the individual based on intensity patterns within the iris. The biometric template is transmitted to the cellular provider where it is compared against other templates stored in a memory or database. The database stores selected data representing images of the iris of a plurality of subjects. A match of the biometric template with a template stored in the database identifies the subject whose iris is being imaged.

Although an image of the eye is reflected back to the subject in mirror 120, this may not provide the desired feedback to the user to enable the user to properly position the imager so that a suitable iris image is obtained. For example, a user may be a novice in using and positioning the imager 100 with respect to the eye 150, or the user may be attempting to image the eye of another subject with the imager. Thus, preferably, the imager 100 comprises a passive feedback mechanism to guide the user in positioning the eye 150 to an optimum location to allow acquisition of a suitable image.

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The passive feedback mechanism is an indicator or combination of indicators that provides, on a near real-time basis, an indication to the user that an adequate iris image has or has not been obtained. Fig. 5 is a schematic diagram of an exemplary iris image recognition system that includes position indicators in accordance with the present invention. Preferably, the indicator is visible and/or audible, such as, for example, an indicator lamp 305 (e.g., a light emitting diode (LED)) that lights when an acceptable image has been captured (i.e., "image acquired"), and a aural indicator via a speaker 310, such as a beep or other tone, that sounds periodically until an acceptable image has been captured (i.e., "imaging in progress").

Additional indicators 306, 307 can be also be used, either alone or in combination, for such indications as "subject identified - accept" and "subject not identified - reject". These indications would be activated pursuant to the results of the processing and comparison performed at the database server at the cellular provider, as described above with respect to Fig. 3. Alternatively, other display devices, such as liquid crystal displays used for other purposes within the telephone, could be used as indicators.

The imager 100 also preferably has an on/off switch (not shown), such as a pushbutton, for powering up the imager and initiating the image acquisition process. Power for the imager 100 is preferably supplied by a battery. The imager 100 receives and acts on instructions from the processor 210 to perform functions such as lighting or turning off the indicator lamp(s) 305, providing the audible signals via the speaker 310, and lighting the 'accept' and 'reject' indicators.

Fig. 6 is a more detailed flow chart of a method of operation in accordance with the present invention. The eye is illuminated at step 350 and an image of the iris is obtained at step 355. At step 360, it is determined if the image is suitable for use with the image processing and comparison routines. If the image is suitable, the image is passed to the processor for further processing, at step 370, and transmission to the cellular provider. A comparison of the template to the templates stored in a database at the cellular provider is performed at step 373. If the comparison provides a positive match, then authorization is granted at step 376 for the user to use the phone. If the comparison does not provide a positive match, then authorization is not granted for the user to use the phone.

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If the image is not suitable at step 360, then at step 380, the indicator(s) is activated (e.g., a beep sound is issued), and processing continues at step 355 (i.e., another image is obtained).

Because the eye's own focusing system automatically adjusts to bring the virtual image 115 into sharp focus to the user, it cannot be relied upon to always accurately focus the eye image on the camera 105. For this purpose, a focus assessment system is used in one embodiment, as shown in Fig. 7. Digital video image information from the imaging device 100 is stored in a frame buffer memory 410, such as a RAM similar to RAM 232 described above with respect to Fig. 4, and capable of storing one complete frame of digitized video information. A focus assessment processor 420 accesses the digitized image information and applies certain measurement algorithms which are disclosed in a co-pending application entitled "Video-Rate Focus Assessment", Serial No. 60/109,960 (Attorney Docket No. ICAN-0067), and incorporated herein by reference. The output of the focus assessment is used to control an indicator, such as the audible indicator 310. As long as the focus assessment processor 420 determines that the captured image is not acceptable for further processing and comparison, the audible indicator 310 is directed to emit periodic sounds to alert the user. Images are repeatedly acquired and assessed until an acceptable one is received. After an acceptable iris image has been received, the audible indicator 310 is turned off and the final image is retained for further processing and comparison, for example, by the microprocessor 210, as described above.

Any known technique for image focusing can be used with the imager of the present invention, such as those described in U.S. Patent 4,876,608, entitled "Focus and Signal to Noise Measurement Routines in Input Scanners", issued to Eaton, U.S. Patent 5,151,583, entitled "Focus Adjustment Device Having Restricting Means for Restricting a Selecting Action According to the Degree of Nearness of a Distance Measurement", issued to Tokunaga et al., and U.S. Patent 5,404,163, entitled "In-Focus Detection Method and Method and Apparatus Using the Same for Non Contact Displacement Measurement", issued to Kubo. The preferred system and method for focus assessment is described below.

A focus score is computed for each video frame (i.e., each captured image). If the focus score exceeds a predetermined value, then it is determined that the image is focused enough for further processing and comparison. If the focus score does not exceed

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the predetermined value, then it is determined that the image is not focused enough for further processing, and an indicator (such as indicator 310, described with respect to Fig. 5) is activated and a further image is captured. Alternatively, a sequence of image frames can be obtained that cycle through a range of focus distances strobed at the video frame-rate, and the focus score computed for each frame can enable the selection of the best focused frame within the sequence of frames. For example, by obtaining image frames at each of several different lens settings and then fitting a spline curve to their respective focus scores one can predict the lens position that would deliver substantially the sharpest focus, by setting the derivative of the parameterized spline curve to zero and then solving the equation for position.

Specific implementation features of the preferred focus assessment system and method which enable its real-time operation, include (1) the computation of quantities in the 2D Fourier domain, without needing to compute an actual 2D Fourier Transform of an image (this avoids the need for approximately 2.25 million floating-point operations required for an FFT (Fast Fourier Transform) on a 500 x 500 pixel image, as the computational complexity of an FFT on n x n data is $O(n^2 \log_2 n)$); (2) only 6,400 integer multiplications (squarings) are performed, which in turn can be eliminated altogether by using small look-up tables; (3) no floating-point operations are required; (4) computation of focus scores is based upon simple algebraic combinations of pixel values within local closed neighborhoods, repeated across regions of the image; and (5) these operations not only allow the algorithm to execute in real-time, but it also enables a straightforward implementation in simple, low-cost, hardware devices that could be embedded within a digital camera or frame grabber.

Preferably, the focus assessment processor 420 is fast enough to determine a focus score for each frame in a video image stream in less than the time it takes to acquire a new frame (e.g., approximately 25 ms). The frame-by-frame focus scores can be used to control a moving lens element for rapid and accurate focus control, or alternatively, to select which of several frames in a video stream is the one in best focus. The rapid selection of well-focused video frames for further processing, such as image analysis and pattern recognition, is important in real-time computer vision because it prevents wasting processing time on poorly-focused images.

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The preferred focus assessment processor measures the focus quality of video images at standard rates of 25 (PAL) or 30 (NTSC) frames per second.

It is contemplated that the focus assessment processor 420 can be implemented in a general purpose personal computer (PC) or by a dedicated, low cost processor which is small enough to be incorporated into the camera electronics.

The processing of a video frame results in the return of an integer value (on a scale between 0 and 100) reflecting the quality of focus; the larger the value of the integer, the better the focus. A value of 0 indicates a completely defocused image whereas the value of 100 indicates maximum focus quality. A predetermined threshold is used to determine whether an image is sufficiently focused or whether another image needs to be retrieved. For example, values greater than about 40 can indicate sufficient quality of focus to warrant further image processing, while values less than about 40 cause a new image frame to be grabbed, and optional feedback provided to the focusing mechanism, if one exists, or to the subject controlling the camera position (via the indicator 310, for example).

Optical defocus is a phenomenon of the 2D Fourier domain. An image represented as a 2D function of the real plane, $I(x,y)$, has a 2D Fourier Transform $F(\mu,v)$ defined as shown in equation 1.

$$F(\mu,v)=\frac{1}{(2\pi)^{2xy}}\int\int I(x,y)e^{i(\mu x+vy)}dxdy \qquad (1)$$

In the image domain, defocus is preferably represented as convolution by the 2D point-spread function of the defocused optics. This in turn may be modeled as a Gaussian whose space constant is proportional to the degree of defocus. Thus, for perfectly focused optics, the optical point-spread function shrinks almost to a delta function, and convolution with a delta function causes no change to the image. Progressively defocused optics equates to convolving with a wider and wider point-spread function, which averages together whole neighborhoods of pixels by such a weighting function, thereby producing an increasingly blurred image.

If the convolving optical point-spread function causing defocus is modeled as a Gaussian whose width represents the degree of defocus, then defocus is equivalent to multiplying the 2D Fourier Transform of a perfectly focused image with the 2D Fourier

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Transform of the "defocusing" (convolving) Gaussian. This latter quantity is itself just another 2D Gaussian but in the Fourier domain, and its space constant (σ) there is the reciprocal of that of the image-domain convolving Gaussian that represented the optical point-spread function. The preferred focus assessment processor uses (1) the duality of convolution and multiplication in the two domains; (2) the fact that a Gaussian has a Fourier Transform which is itself a Gaussian, but with the reciprocal width because of (3) the Similarity Theorem. Thus, the 2D Fourier Transform $D_\sigma(\mu,v)$ of an image defocused to degree σ is related to $F(\mu,v)$, the 2D Fourier Transform of the corresponding in-focus image, as given by equation 2.

$$D_\sigma(\mu,v) = e^{-\left(\frac{\mu^2+v^2}{\sigma^2}\right)} F(\mu,v) \qquad (2)$$

From the above equation, the effect of defocus is to attenuate primarily the highest frequencies in the image, and that lower frequency components are virtually unaffected by defocus since the exponential term approaches unity as the frequencies (μ,v) become small. For simplicity, the present description has assumed isotropic optics and isotropic blur, and the optical point-spread function has been described as a Gaussian. However, the analysis can readily be generalized to non-Gaussian and to anisotropic optical point-spread functions.

Thus, an effective way to estimate the quality of focus of an image is to measure its total amount of energy in the 2D Fourier domain at high spatial frequencies, since these are the most attenuated by defocus. One may also perform a kind of "contrast normalization" to make such a spectrally-based focus measure independent of image content, by comparing the ratio of energy in the highest frequency bands to that in slightly lower frequency bands. Such spectrally-based energy measurements are facilitated by exploiting Lord Rayleigh's theorem for conserved total power in the two domains, shown in equation 3.

$$\int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty} |I(x,y)|^2 \, dxdy = \int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty} |F(\mu,v)|^2 d\mu dv \qquad (3)$$

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Thus, high-pass filtering or band-pass filtering an image at a ring of high spatial frequency (using only convolution in the 2D image domain) and measuring the residual energy, is equivalent to making the corresponding energy measurement in the high frequency bands of the 2D Fourier domain. The appropriate measurements in the 2D Fourier domain to assess focus can be performed without computing a time-consuming 2D Fourier Transform. Indeed, the measurements can be performed without even a single floating-point operation, and even without any multiplications if appropriate convolution kernels and look-up tables are used.

A real-time procedure for focus assessment based on these theoretical principles is used in the focus assessment processor 420. It executes much faster than the video frame-rate, and so real-time focus assessments can be made on a frame-by-frame basis. These can be used either to control the position of a focusing lens element, or alternatively as a type of autofocus system in which frames are grabbed at a variety of focal depths in order to select only the best one for processing, or to prevent time being wasted on processing image frames which are assessed to be in poor focus.

The 2D spectral measurements described above can be implemented by convolving an image with the following convolution kernel, in which pixel values within a predetermined region, such as, for example, an (8 x 8) neighborhood, are added together with the weights indicated in each of the cells:

-1	-1	-1	-1	-1	-1	-1	-1
-1	-1	-1	-1	-1	-1	-1	-1
-1	-1	+3	+3	+3	+3	-1	-1
-1	-1	+3	+3	+3	+3	-1	-1
-1	-1	+3	+3	+3	+3	-1	-1
-1	-1	+3	+3	+3	+3	-1	-1
-1	-1	-1	-1	-1	-1	-1	-1
-1	-1	-1	-1	-1	-1	-1	-1

It should be noted that no pixel-by-pixel multiplications are needed in order to impose these weights. Rather, the pixels in the central region are added together, such as the (4 x 4)

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square, that sum is tripled, and then all pixel values in the outer two pairs of rows and columns are subtracted from the tripled sum. The result is squared and added to an accumulator, thus implementing the left-hand side of equation (3) above for this local region of the image. The complete (8 x 8) convolution kernel is then moved to a new position in the image, along a sampling grid that selects every 4th row and every 4th column, and the operation is repeated. Thus, to assess the quality of focus within the central (320 x 320) region of an image, this set of 64 pixel summations followed by a squaring operation is repeated a total of $(320/4)^2=6,400$ times.

In the 2D Fourier domain, the spectral consequences of this operation can be appreciated by examining the 2D Fourier Transform of the convolution kernel above. The kernel is equivalent to the superposition of two centered square box functions, one of size (8 x 8) and amplitude -1, and the other of size (4 x 4) and amplitude +4 (for the central region in which they overlap, the two therefore sum to +3). The 2D Fourier Transform of each of these square functions is a 2D "sinc" function, whose size parameters differ by a factor of two in each of the dimensions and whose amplitudes are equal but opposite, because the two component boxes have equal but opposite volumes. Thus, the overall kernel has a 2D Fourier Transform $K(\mu,v)$ which is the difference of two differently-sized 2D sinc functions, as given by equation 4.

$$K(\mu,v)=\frac{\sin(\mu)\sin(v)}{\pi^2\mu v}-\frac{\sin(2\mu)\sin(2v)}{4\pi^2\mu v} \qquad (4)$$

This is a high-pass (or ultimately a band-pass) filter, selecting only a high range of spatial frequencies in all orientations. Towards its center, corresponding to very low spatial frequencies, its value approaches zero (as can also be inferred from the fact that the sum of all pixel weights in the convolution kernel shown above is zero). Thus, low frequencies play little or no role in computing a focus score, and only relatively high frequencies contribute significantly to the computation of a focus score. Equation (3) shows that summing the squares of all the local convolution sums across the image is equivalent to summing the total amount of high frequency energy in the 2D Fourier Transform of the image. The action of the convolution kernel is to impose the above power spectral weighting function so that primarily high frequency energy is measured.

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Finally, the summated 2D spectral energy is passed through a compressive nonlinearity of the form $f(x)=100\ x^2/(x^2+c^2)$ in order to generate a normalized focus score in the range of 0 to 100 for any image.

The focus assessment technique is applied immediately after each image frame is digitized and stored in the frame buffer memory 410 in order to assess whether the focus quality is sufficient to warrant any further processing. If the calculated focus quality value of the captured image is greater than or equal to a predetermined value, the image is passed to applicable programs for further processing, for example for extraction of a biometric template. The focus assessment technique can be used to compare the relative focus of an entire series of images in order to select the one most in-focus (i.e. having the highest focus assessment score), as well as to measure a single image.

The focus assessment technique can be used to provide a feedback indication to a system user who controls the position of the imager relative to the object being imaged. This can be accomplished by activating an indicator which would continue, while successive images are captured and their focus assessed, until the focus assessment score exceeds a predetermined value. At this point, the indicator is deactivated and the last image captured is transferred to the image processor 210 where it is processed to extract the biometric template.

The application of the focus assessment technique in combination with the feedback indicator helps resolve the man-machine interface problems associated with the use of digital imaging devices on the eye. Individuals using the system are provided positive, objective indicators and feedback as to the quality of image focus. The focus assessment processor can also be used in any situation where it is required to determine the quality of focus of video images at industry standard frame rates (NTSC and PAL).

Thus, the image is obtained at the imager and transmitted to an analog to digital converter 405. The digitized video information is then stored in a frame buffer memory 410. The focus assessment processor 420 isolates the central 320 x 320 region of the image. 8 x 8 pixel blocks (each pixel is in only one block) are then processed by first summing pixels in the central 4 x 4 region, tripling that sum, and then subtracting from this value all the pixel values in the outer two pairs of rows and columns. This result is then squared. This process is performed on each 8 x 8 block, and the results are summed. After

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the entire image has been processed, the summed result is compressed nonlinearly to generate a focus score between 0 and 100. This score is then compared to a predetermined number for determining if the indicator 310 should be activated.

The focus assessment is preferably performed by the microprocessor 210, or it can be a separate processor element within the telephone.

It is contemplated that in addition to the focus assessment processor, an auto-focus lens system could be used in the present invention. The results of the focus assessment control the lens system, thereby automatically adjusting focus to produce an optimal image. This would place less of a premium on the accuracy with which the user positions the eye, and would be helpful if the user could not see or hear the indicators described above.

The iris imager of the present invention can be used as a security module for electronic devices such as a telephone. Fig. 8 is a schematic diagram of an exemplary iris imager incorporated into a telephone in accordance with the present invention. The imager 700 comprises the camera 105, lens 110, mirror 120, and illuminator 130, as described above with respect to Fig. 1. The imager 700 also comprises visible indicators 555, 556, 557, which are similar to indicators 305, 306, 307, respectively, described above with respect to Fig. 5. An audible indicator 560, similar to indicator 310, is also disposed within the imager 700. The imager 700 further comprises electronics and circuitry 500 for processing and comparing the obtained image. The electronics and circuitry 500 comprises a microprocessor 510 (similar to microprocessor 210) that controls the imager 700 along with an I/O controller 525 and runs software held in a ROM 505. The processor 510 is connected to the ROM 505, a RAM 532 that is capable of storing at least one captured image or an iris, another memory 530, such as an EPROM, for storing a plurality of biometric templates or iris images that are to be compared with the captured iris image. The electronics and circuitry 500 is also connected to the camera 105, the illuminator 130, and the indicators 555, 556, 557, 560 for controlling these elements of the imager 700. The processor can also comprise a focus assessment processor, similar to the focus assessment processor 420.

It should be noted that in the embodiment of Fig. 8, the database memory 530 of templates is stored within the imager 700 and not at a central station (as described,

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for example, with respect to Fig. 4), as is the processor 510 used in the comparison. In the embodiment of Fig. 8, the comparison of the captured image template with the stored templates takes place locally within the telephone, and the biometric template is not sent to the central station for comparison or authentication. Instead, preferably, a code is inserted into the call set-up protocol and transmitted to the central station server, as described below.

The imager 700 is coupled to telephone electronics 570 for transmitting encrypted or unencrypted data to another telephone or system via an antenna. The telephone electronics 570 is essentially a telephone and is preferably a conventional cell phone having telephone electronics and is connected to a transmission antenna. Preferably, a conventional voltage regulator (not shown) provides the appropriate operating voltage to the imager 700 from the power supply (e.g., a battery) of the phone.

Preferably, the imager 700 of the present invention is incorporated into a handset of a telephone 575, as shown in Fig. 9A. The present invention can be incorporated into a conventional digital cell phone, as shown in Fig. 9A, such as those manufactured by Qualcomm or Nokia, or a conventional wired phone. U.S. Patent No. 5,448,622, "Cellular Telephone With Plural Telephone Numbers", issued to Huttunen, and U.S. Patent No. 5,790,957, "Speech Recall In Cellular Telephone", issued to Heidari, describe cellular telephones and telephone electronics and circuitry, and both of which are incorporated herein by reference.

Figs. 9B, 9C, and 9D show rear, side, and front elevational views of another exemplary device 800, also referred to as an IRISPHONE™, in which the imager of the present invention can be incorporated. A keypad 810 is used to enter phone numbers, etc., which are displayed on a display 815, such as an LCD, and a power supply 820 is preferably a re-chargeable battery. A transmission antenna 830 is also provided. An illuminator 840, similar to the illuminator 130, and a mirror 850, similar to the mirror 120 are provided on the front of the device 800. Also provided on the front of the device 800 is a microphone 860 and a speaker 865, for use in communications and as an indicator, similar to the indicator 310, described above. A switch or button 805 is used as an activator to begin iris image capture. The imager and phone circuitry 870 is encased within the device 800.

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Fig. 10 is a flow diagram of an exemplary method of operation of a telecommunications iris imager in accordance with the present invention. A user desiring to make a telephone call first unlocks the telephone by having his iris identified by the imager residing within the phone. The eye, and thus the iris, are illuminated at step 605. An image is obtained of the iris at step 610. At step 615, it is determined if the image is suitable for further processing and comparison, as described above. If the image is not suitable, the appropriate indicators are activated at step 620, and processing returns to step 610 with the capture of another iris image.

If the captured image is suitable for further processing, the image is processed at step 630 (an indicator can be activated to alert the user that a suitable image has been captured) to extract an iris template. The extracted template is compared to the stored images residing in a database, for example, in a memory 530, at step 635. If the iris template is invalid (i.e., if there is no match between the captured image and the stored images), at step 640, the phone remains off (locked), and the imaging routine exits. Optionally, indicators can also be activated. In this manner, the telephone remains locked, and cannot be used because it is determined that the user is unauthorized.

If the iris template is valid at step 635 (i.e., there is a match between the captured image and the stored images, and thus the identity of the user has been confirmed by the imager), the phone is turned on (unlocked), an indicator can be activated, and a user code is transmitted to the service provider (e.g., the central station server 900, as shown in Fig. 11) at step 650. The user code, also referred to as an IRISCODE™, comprising a 512 byte code for example, is generated and is inserted into the call set-up protocol and transmitted to the server 900.

At step 660, the server authenticates the IRISCODE™ against stored or pre-enrolled codes that are stored in a database 910 at the server site. If the code is invalid, then the user is not authorized to place a call, an indicator is activated at the phone, and the routine exits at step 670. If the code is valid, then the user can use the phone to place a call at step 680. The phone can be returned to its locked, secure state either upon being powered down or upon completion of the phone call.

Thus, in accordance with the present invention, the server can bill against the user's identity (responsive to the IRISCODE™) and not the phone number. Thus,

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different users can use the same phone, and be separately billed, according to the identities that are stored at the server. This provides an additional level of security and user validation.

It should be noted that any call set-up protocol can be used with the present invention, including GSM, TAC, and AMPS. For example, in the Group Speciale Mobile (GSM) cellphone architecture, an "Intel Architecture" microprocessor and "Intel SmartVoltage" flash memory are preferred components. The basis of this technology is a microprocessor, such as the Intel 386 microprocessor. The preferred memory is a non-volatile, re-writeable, low voltage flash memory that enables computer-like functions. In the case of a Nokia cellphone, for example, a 4-Mbit flash memory storage device stores the GSM protocol. Intel's 16-Mbit flash devices can store such things as phone numbers, fax numbers, calendar information, as well as a Graphical User's Interface (GUI) operating system. Similarly, each IRISCODE™ (e.g., 512 bytes) of the users can be stored in these flash memory devices. Preferably, about 40 pairs of IRISCODEs (one IRISCODE™ for the left eye and one IRISCODE™ for the right eye for each user) can be stored in the 4-Mbit devices and about 160 pairs of IRISCODEs can be stored in the 16-Mbit devices.

The operating system performs such functions as: (1) retrieve the live IRISCODE™ from the IRISPHONE™ image, (2) compare the "live" IRISCODE™ against the IRISCODE™ database stored in the memory (e.g., flash memory), and (3) transfer, upon positive identification, the authentication into the GSM protocol for transport to the wireless GSM server. This is done in a manner similar to the manner in which the Electronic Serial Number (ESN) is authenticated.

The Wireless Application Protocol (WAP), along with the Wireless Application Environment (WAE), have been developed to extend Internet content and advanced services to the cellphone industry. A wireless IRISPHONE™ captures an IRISCODE™ using the WAE user agent that sends the code to the cellphone memory for local authentication. An encoded request for authentication and identity is then sent to the origin server. An encoded positive identification or negative identification is returned, and either allows the user to make calls via identity-based billing or disallows all calls. For example, the call reject function would be used to reject the identity of an individual if the

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live IRISCODE™ did not match any stored value. The WAP Mark-up Language (WML) allows for user defined fields such as IRISCODEs.

The Electronic Business Card Format of WAP/WAE is compatible with a 512 byte IRISCODE™. The IRISCODE™ can be stored on a card instead of in flash memory.

Although illustrated and described herein with reference to certain specific embodiments, it will be understood by those skilled in the art that the invention is not limited to the embodiments specifically disclosed herein. Those skilled in the art also will appreciate that many other variations of the specific embodiments described herein are intended to be within the scope of the invention as defined by the following claims.

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What is claimed is:

1. A telecommunications device having telephone electronics for transmitting and receiving data, comprising:

a telephone security module comprising:

iris acquisition means having a front surface for obtaining an image of an iris of an eye;

a lens having an image plane disposed in front of said front surface of said iris acquisition means;

a mirror disposed on a side of said lens opposite said iris acquisition means;

an illuminator disposed along a side of said mirror;

a first memory for storing at least one template of at least one image of an iris of at least one person's eye;

a second memory for storing an iris image obtained by said iris acquisition means;

a processor for extracting a template from said stored iris image; and

a comparator for comparing said template from stored iris image with said at least one template to identify the person;

an input device for receiving user input;

a display for displaying said user input;

a power supply;

an antenna;

a microphone;

a speaker; and

an activator to begin iris image acquisition.

2. The telecommunications device according to claim 1, wherein said input device is a keypad.

3. The telecommunications device according to claim 1, wherein said power

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supply is a re-chargeable battery.

4. The telecommunications device according to claim 1, wherein said activator is one of switch and a pushbutton.

5. The telecommunications device according to claim 1, wherein said iris acquisition means comprises a camera, and said mirror is a cold mirror.

6. The telecommunications device according to claim 5, wherein said camera is sensitive to light having a wavelength in a range between about 400 nm and about 1100 nm.

7. The telecommunications device according to claim 5, wherein said mirror reflects light having a wavelength in a range between about 400 nm and about 700 nm and passes light having a wavelength greater than about 700 nm.

8. The telecommunications device according to claim 1, wherein said illuminator emits light having a wavelength in a range between about 680 nm and about 900 nm towards the iris of the eye being imaged, the eye being out of contact with the iris imaging apparatus.

9. The telecommunications device according to claim 1, further comprising at least one of a visible indicator and an audible indicator to indicate when the image of the iris has been obtained.

10. The telecommunications device according to claim 9, further comprising a focus assessment processor coupled to said at least one of a visible indicator and an audible indicator.

11. The telecommunications device according to claim 1, wherein said processor unlocks the telecommunications device responsive to the results of said comparison.

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12. A telecommunications device having telephone electronics for transmitting and receiving data, comprising:

a telephone security module comprising:

iris acquisition means having a front surface for obtaining an image of an iris of an eye;

a lens having an image plane disposed in front of said front surface of said iris acquisition means;

a mirror disposed on a side of said lens opposite said iris acquisition means;

an illuminator disposed along a side of said mirror;

a memory for storing an iris image obtained by said iris acquisition means;

a processor for extracting a template from said stored iris image; and

a communications interface for transmitting said template to a central station;

an input device for receiving user input;

a display for displaying said user input;

a power supply;

an antenna;

a microphone;

a speaker; and

an activator to begin iris image acquisition,

wherein said processor unlocks the telecommunications device responsive to a signal received from said central station.

13. A method of unlocking a telecommunications device responsive to the identification of a person, comprising the steps of:

(a) storing image information of the iris of at least one person's eye;

(b) illuminating an eye of an unidentified person having an iris;

(c) obtaining an image of said iris of said unidentified person;

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(d) determining if said image is an image of sufficient quality for a step (f) of extracting;

(e) repeating steps (b) through (d) until said image of sufficient quality is obtained;

(f) extracting an iris template if said image is of sufficient quality;

(g) comparing said iris template of said obtained image with said stored image information to identify said unidentified person; and

(h) unlocking the telecommunications device responsive to a result of said step of comparing.

14. The method according to claim 13, further comprising the step of activating an indicator if said image is of insufficient quality.

15. The method according to claim 14, wherein said indicator is an audible indicator.

16. The method according to claim 13, further comprising the step of activating an indicator responsive to said step of comparing.

17. The method according to claim 16, wherein said indicator is a visible indicator.

18. The method according to claim 13, wherein said step of determining if said image is an image of sufficient quality comprises the step of focus assessment processing said image.

19. The method according to claim 13, wherein said telecommunications device is unlocked if said step of comparing identifies said person.

20. The method according to claim 13, wherein said step of unlocking the

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telephone comprises the steps of unlocking the telecommunications device if said iris template substantially matches said stored image information and generating a user code,

wherein the telecommunications device remains locked if said iris template does not substantially match said stored image information.

21. The method according to claim 20, further comprising the step of activating an indicator if said iris template substantially matches said stored image information.

22. The method according to claim 20, further comprising the step of transmitting said user code to a service provider via a set-up protocol.

23. The method according to claim 22, wherein said set-up protocol is one of GSM, TAC, and AMPS.

24. The method according to claim 22, further comprising the steps of:

authenticating said user code at said service provider;

if said user code is authentic, authorizing a telephone call to be placed, otherwise, preventing a telephone call from being placed.

25. The method according to claim 24, wherein the step of authenticating comprises comparing said user code to a plurality of predetermined codes.

26. The method according to claim 25, wherein said predetermined codes are stored in a server database.

27. The method according to claim 24, further comprising the step of activating an indicator responsive to said step of authenticating.

28. The method according to claim 24, wherein if said user code is authentic, further comprising the steps of placing a telephone call and billing against an identity of said person.

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29. A telephone security module comprising:

iris acquisition means having a front surface for obtaining an image of an iris of an eye;

a lens having a image plane disposed in front of said front surface of said iris acquisition means;

a mirror disposed on a side of said lens opposite said iris acquisition means;

an illuminator disposed along a side of said mirror;

a memory for storing an iris image obtained by said iris acquisition means;

a processor for extracting a template from said stored iris image; and

a communications interface for transmitting said template to a central station.

30. The telephone security module according to claim 29, wherein said iris acquisition means comprises a camera, and said mirror is a cold mirror.

31. The telephone security module according to claim 30, wherein said camera is sensitive to light having a wavelength in a range between about 400 nm and about 1100 nm.

32. The telephone security module according to claim 30, wherein said mirror reflects light having a wavelength in a range between about 400 nm and about 700 nm and passes light having a wavelength greater than about 700 nm.

33. The telephone security module according to claim 29, wherein said illuminator emits light having a wavelength in a range between about 680 nm and about 900 nm towards the iris of the eye being imaged, the eye being out of contact with the iris imaging apparatus.

34. The telephone security module according to claim 29, further comprising at least one of a visible indicator and an audible indicator to indicate when the image of the iris has been obtained.

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35. The telephone security module according to claim 34, further comprising a focus assessment processor coupled to said at least one of a visible indicator and an audible indicator.

36. The telephone security module according to claim 29, wherein said processor unlocks a telephone responsive a signal received from said central station.

37. A method of unlocking a telephone responsive to the identification of a person, comprising the steps of:

(a) storing image information of the iris of at least one person's eye;

(b) illuminating an eye of an unidentified person having an iris;

(c) obtaining an image of said iris of said unidentified person;

(d) determining if said image is an image of sufficient quality for a step (f) of comparing;

(e) repeating steps (b) through (d) until said image of sufficient quality is obtained;

(f) comparing a template of said obtained image with said stored image information to identify said unidentified person; and

(g) unlocking the telephone responsive to a result of said step of comparing.

38. The method according to claim 37, further comprising the step of activating an indicator if said image is of insufficient quality.

39. The method according to claim 38, wherein said indicator is an audible indicator.

40. The method according to claim 37, further comprising the step of activating an indicator if said image is of sufficient quality.

41. The method according to claim 40, wherein said indicator is a visible indicator.

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42. The method according to claim 37, further comprising the step of activating an indicator responsive to said step of comparing.

43. The method according to claim 42, wherein said indicator is a visible indicator.

44. The method according to claim 37, wherein said step of determining if said image is an image of sufficient quality comprises the step of focus assessment processing said image.

45. The method according to claim 37, wherein said telephone is unlocked if said step of comparing identifies said person.

46. A system of identification of a person for unlocking a telephone, comprising:

the telephone security module of claim 29;

a second memory for storing at least one template of at least one image of an iris of at least one person's eye; and

a second processor for comparing said template of said stored iris image with said at least one stored template of said second memory to identify the person, and for unlocking the telephone responsive to the result of said comparison.

47. The system according to claim 46, wherein said second memory and said second processor are housed in a central station remote from the telephone security module.

48. The system according to claim 46, wherein said second processor unlocks the telephone when said template of said stored iris image substantially matches said at least one stored template of said second memory.

49. A telephone security module comprising:

iris acquisition means having a front surface for obtaining an image of an iris of an eye;

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a lens having a image plane disposed in front of said front surface of said iris acquisition means;

a mirror disposed on a side of said lens opposite said iris acquisition means;

an illuminator disposed along a side of said mirror;

a first memory for storing at least one template of at least one image of an iris of at least one person's eye;

a second memory for storing an iris image obtained by said iris acquisition means;

a processor for extracting a template from said stored iris image; and

a comparator for comparing said template from stored iris image with said at least one template to identify the person.

50. The telephone security module according to claim 49, wherein said iris acquisition means comprises a camera, and said mirror is a cold mirror.

51. The telephone security module according to claim 50, wherein said camera is sensitive to light having a wavelength in a range between about 400 nm and about 1100 nm.

52. The telephone security module according to claim 50, wherein said mirror reflects light having a wavelength in a range between about 400 nm and about 700 nm and passes light having a wavelength greater than about 700 nm.

53. The telephone security module according to claim 49, wherein said illuminator emits light having a wavelength in a range between about 680 nm and about 900 nm towards the iris of the eye being imaged, the eye being out of contact with the iris imaging apparatus.

54. The telephone security module according to claim 49, further comprising at least one of a visible indicator and an audible indicator to indicate when the image of the iris has been obtained.

55. The telephone security module according to claim 54, further comprising a focus assessment processor coupled to said at least one of a visible indicator and an audible indicator.

56. The telephone security module according to claim 49, wherein said processor unlocks a telephone responsive to the results of said comparison.

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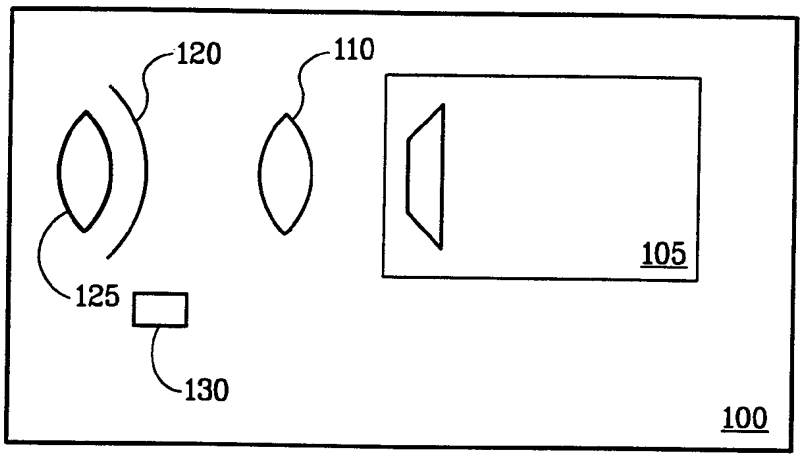

FIG. 1

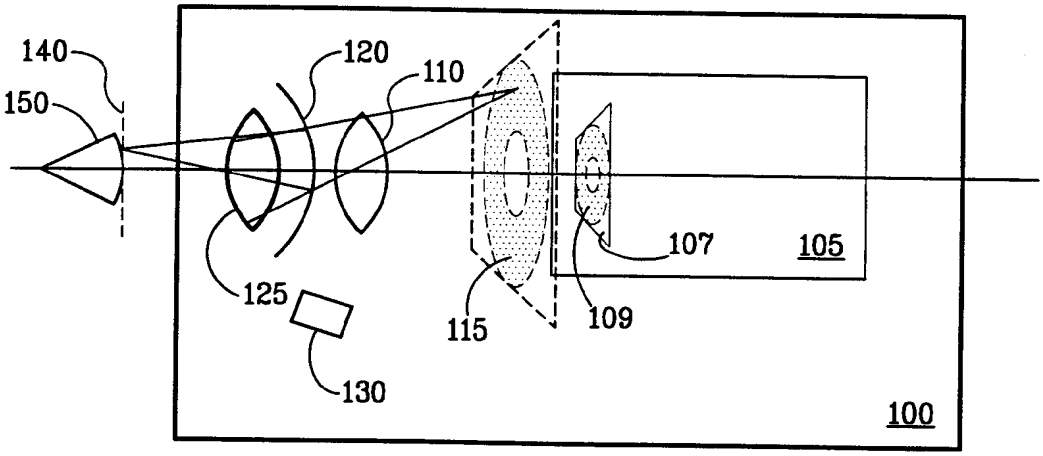

FIG. 2A

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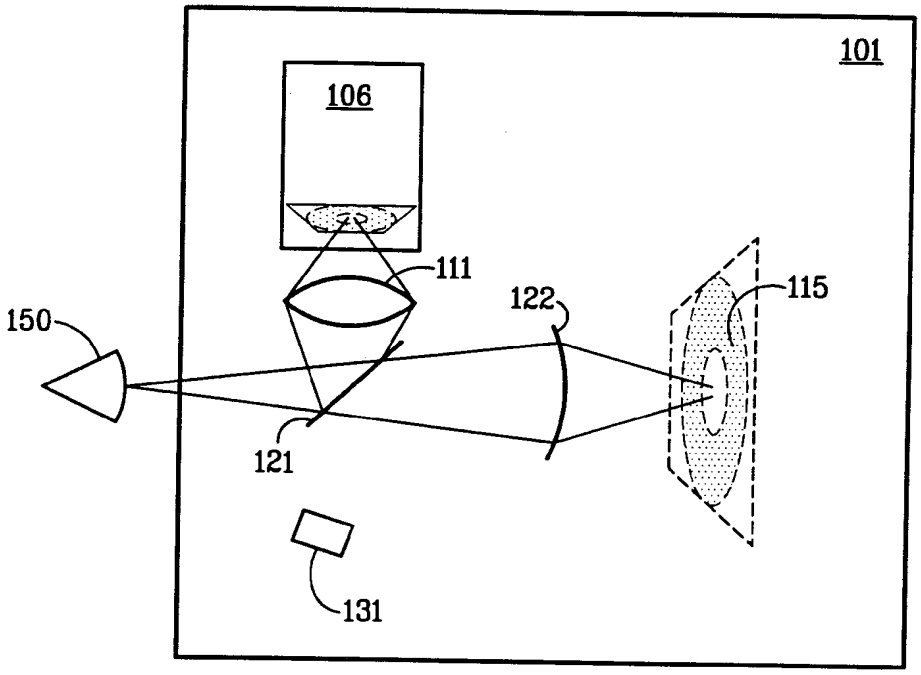

FIG. 2B

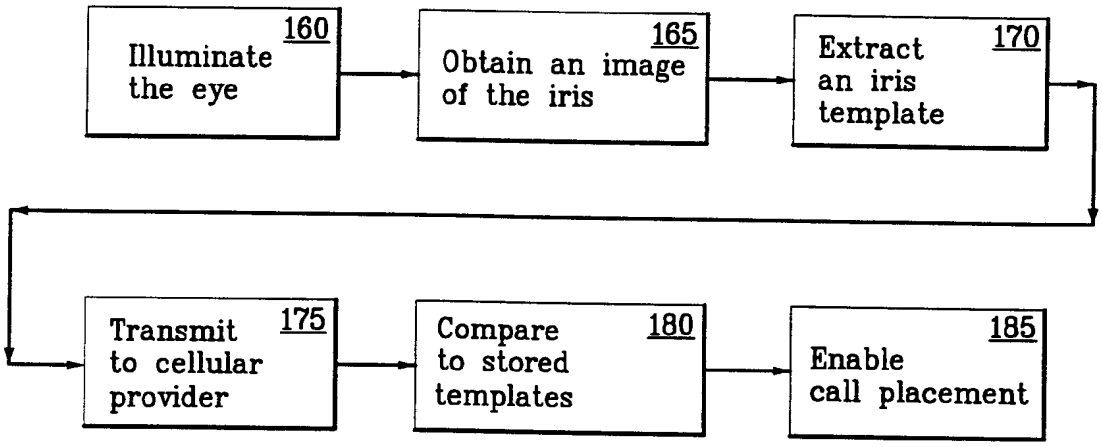

FIG. 3

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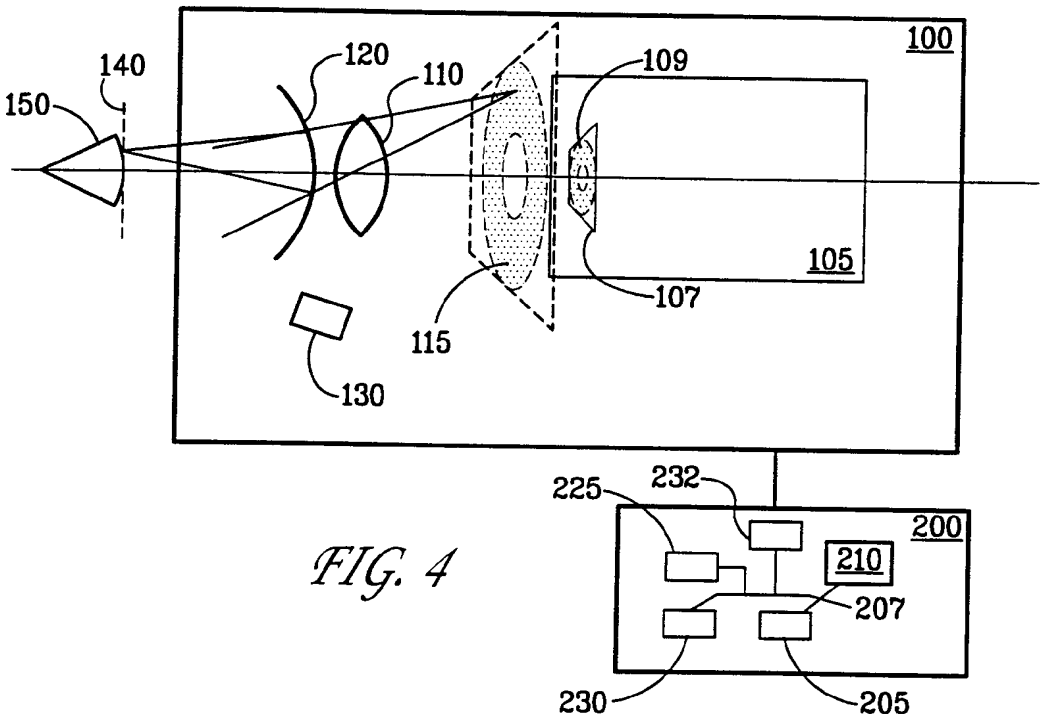

FIG. 4

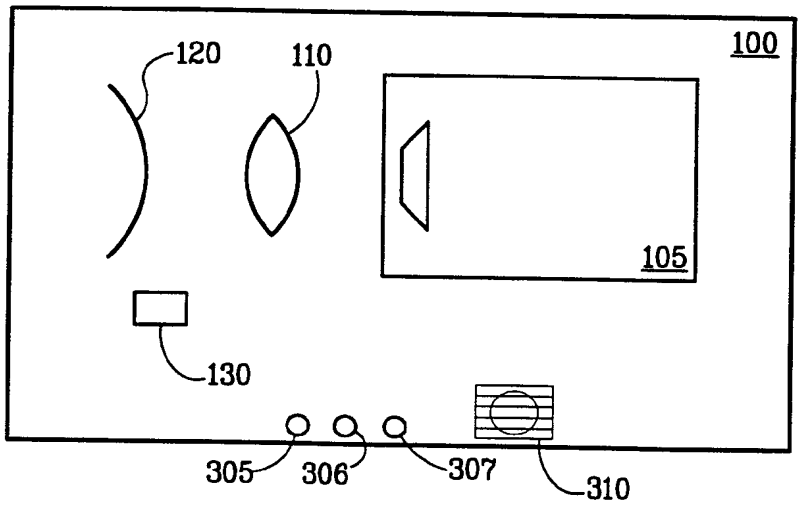

FIG. 5

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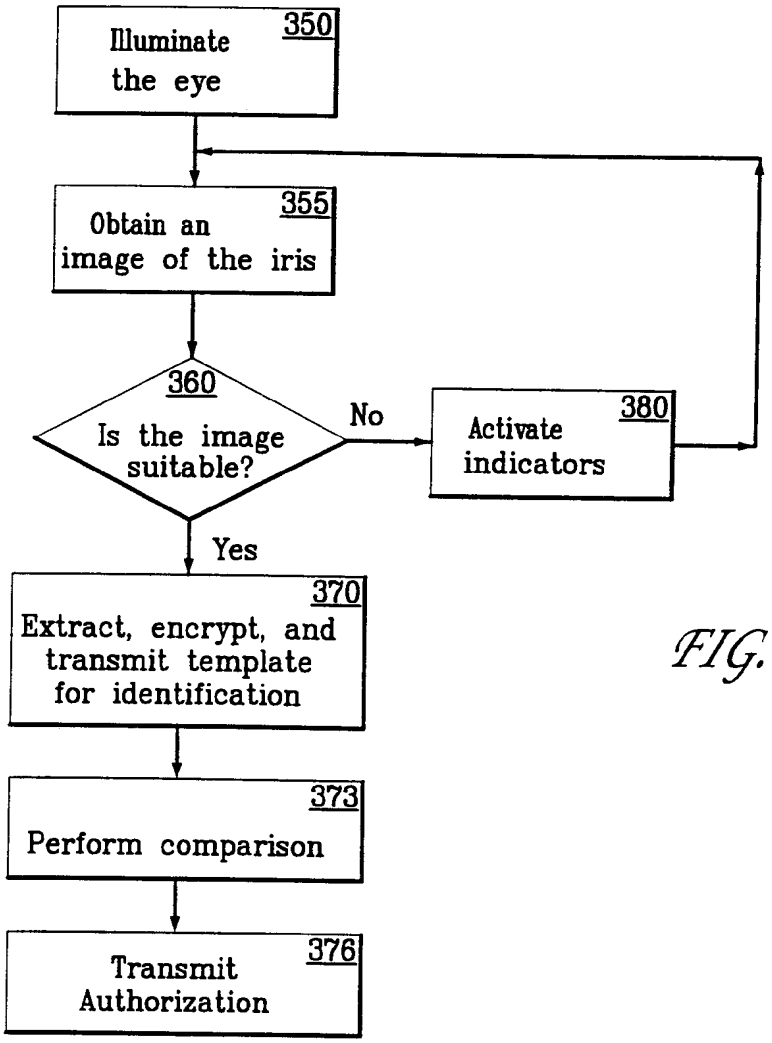

FIG. 6

FIG. 7

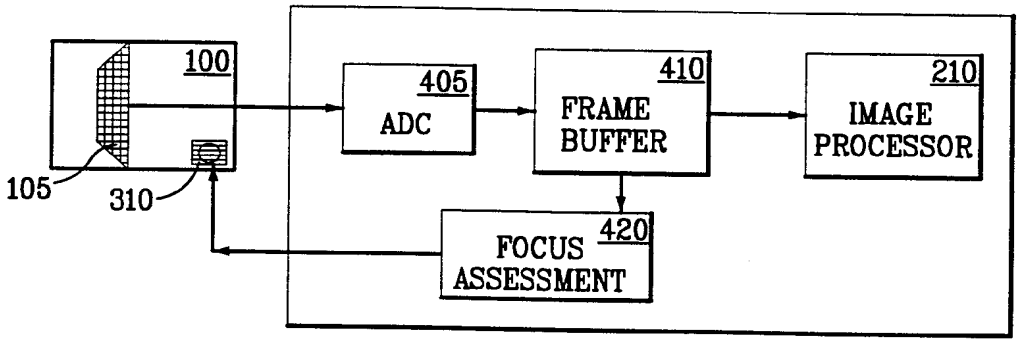

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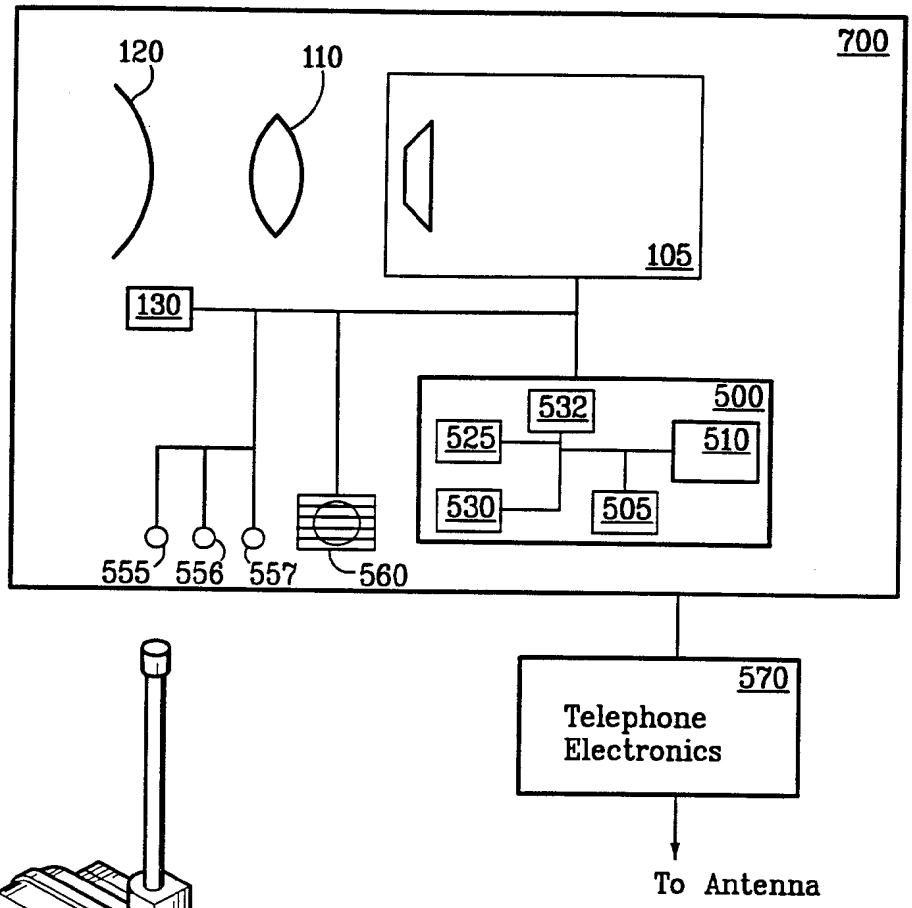
FIG. 8



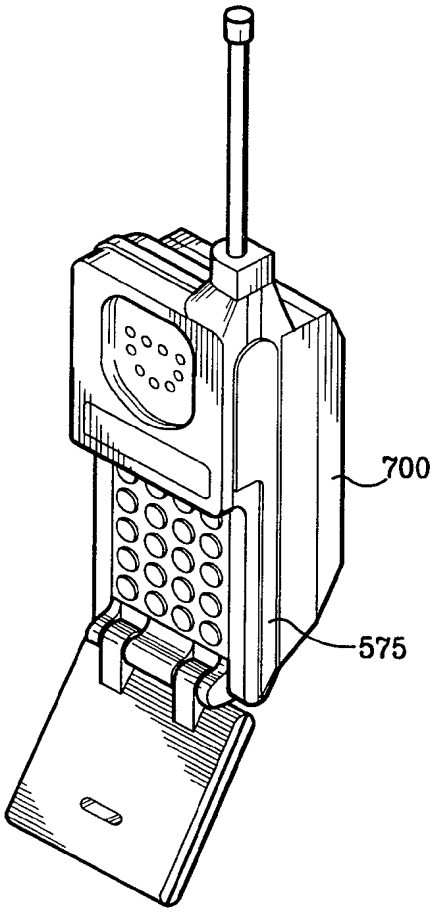


FIG. 9A

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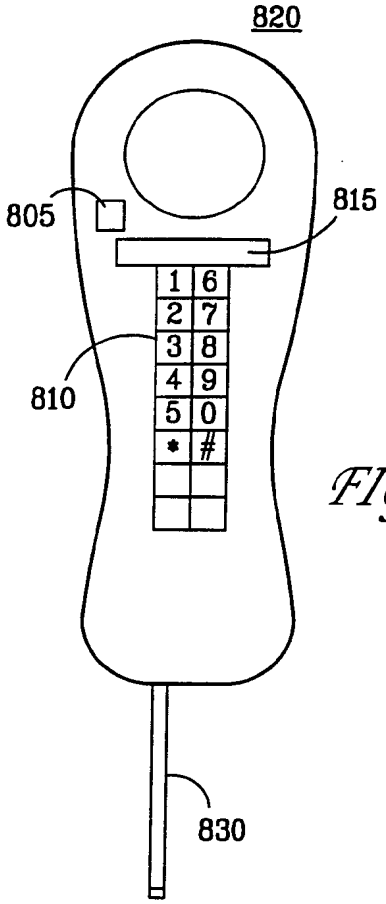

FIG. 9B

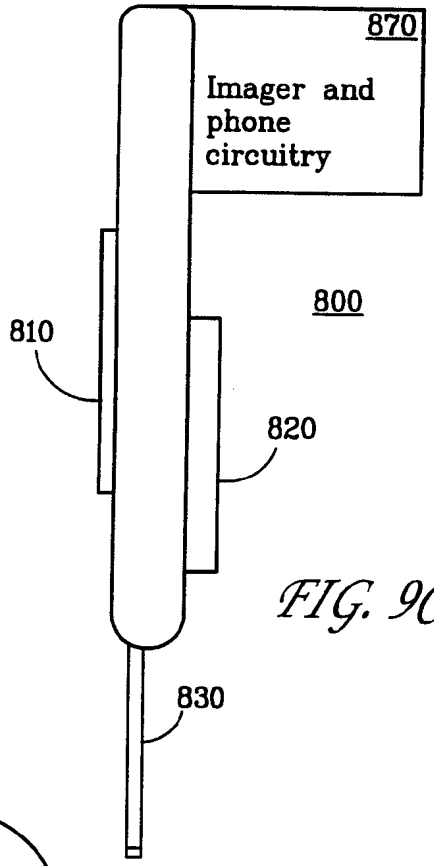

FIG. 9C

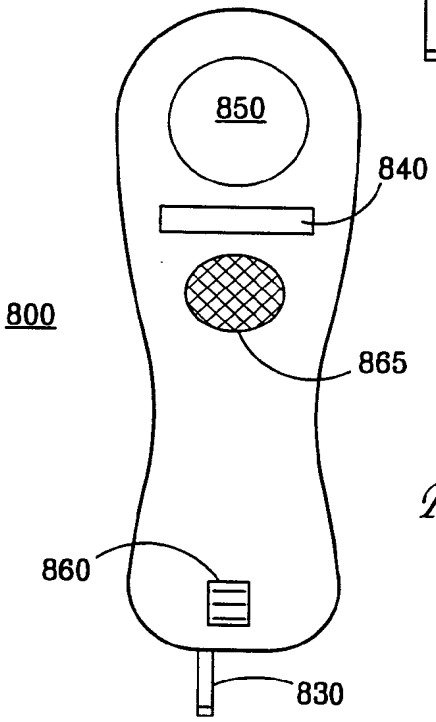

FIG. 9D

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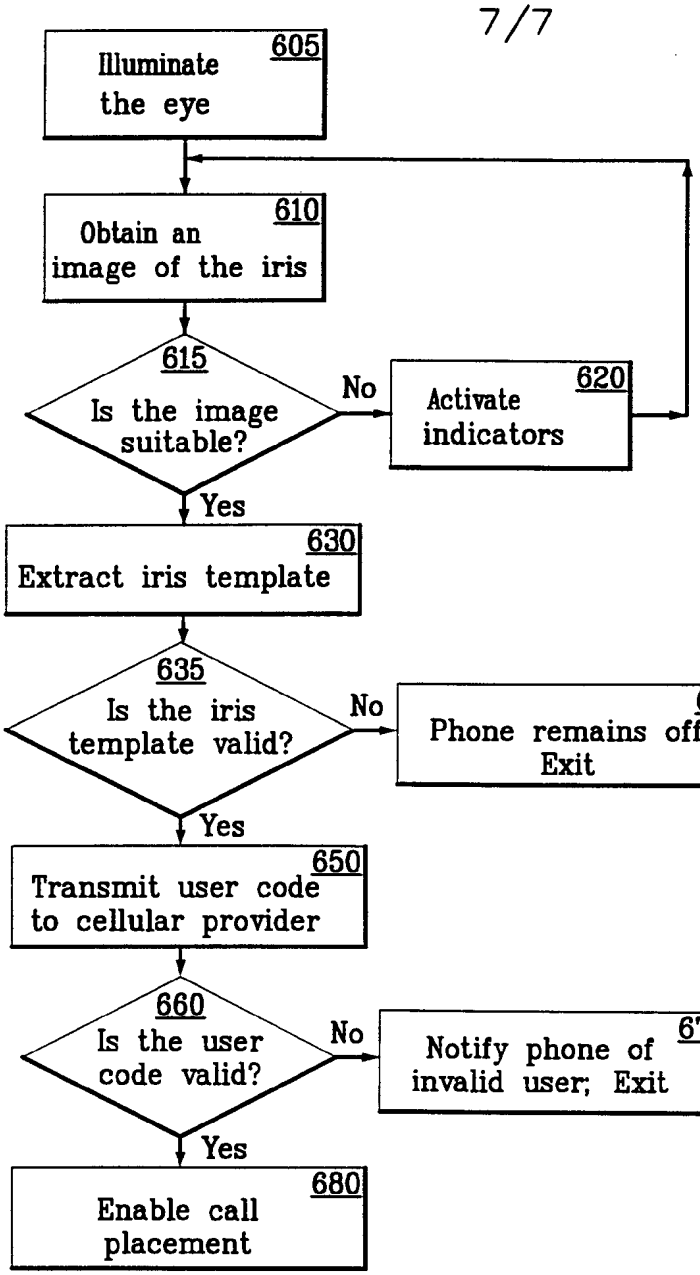

FIG. 10

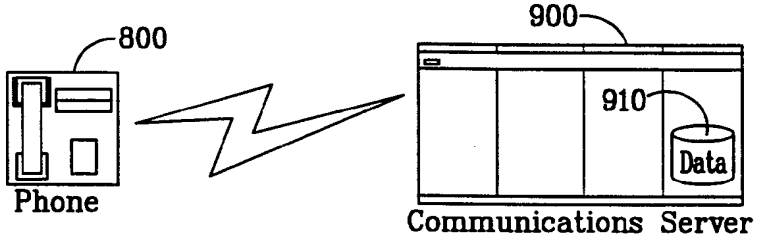

FIG. 11

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/26559

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G06K 9/00; H04K 1/00; H04L 9/00; G07D 7/00
US CL : 382/117; 380/25; 340/825.34
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 382/116, 117; 380/23, 24, 25; 340/825.34

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

IEEE ONLINE, EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,629,981 A (NERLIKAR) 13 May 1997, col. 6, line 56 - col. 7 , line 32; col. 17 ,line 56 - col. 18, line 67.	1-56
Y	US 5,359,669 A (SHANLEY et al.) 25 October 1994, col. 2, line 7 - col. 4, line 60	1-56
A	US 5,581,630 A (BONNEAU, Jr.) 03 December 1996, col. 3, line 27 - col. 4, line 53.	1-56

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 15 JANUARY 2000	Date of mailing of the international search report 02 February 2000 (02.02.00)
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer SHAWN B. CAGE James R. Matthews Telephone No. (703) 305-0572

Form PCT/ISA/210 (second sheet)(July 1992)★

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Espacenet

Bibliographic data: JP2003242125 (A) — 2003-08-29

PORTABLE INFORMATION TERMINAL, AUTHENTICATION AUXILIARY TERMINAL AND INDIVIDUAL AUTHENTICATION METHOD

Inventor(s): KUROSAWA TAKAHIRO; SAKAUCHI YUICHI ± (KUROSAWA TAKAHIRO, ; SAKAUCHI YUICHI)

Applicant(s): CANON KK ± (CANON INC)

Classification: **- international:** ***G06F15/00; G06F15/02; G06F21/31; G06F21/32; H04L9/32; H04M1/00; H04M1/274; H04M1/725; H04W12/08; H04W84/10;*** (IPC1-7): G06F15/00; G06F15/02; H04L9/32; H04M1/00; H04M1/274; H04M1/725; H04Q7/38

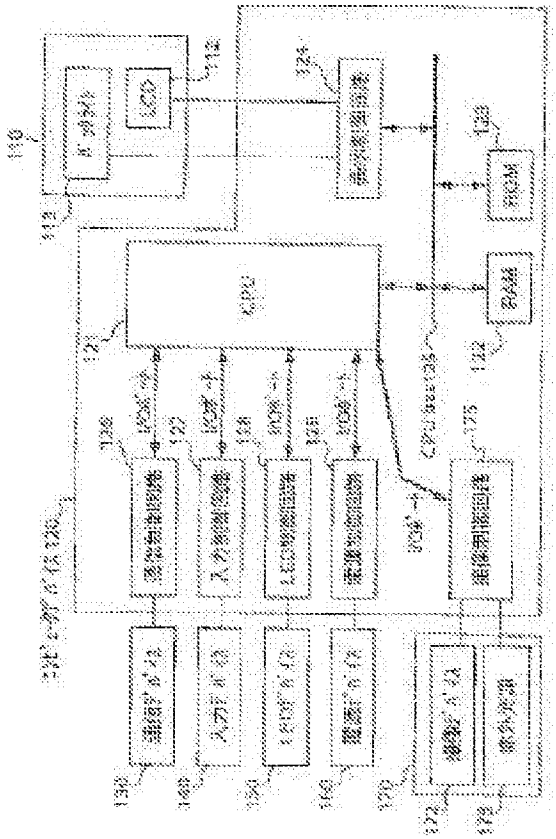
- cooperative:

Application number: JP20020040451 20020218 Global Dossier

Priority number(s): JP20020040451 20020218

Abstract of JP2003242125 (A)

PROBLEM TO BE SOLVED: To realize a safe and easy individual authentication by use of a portable information terminal. ;SOLUTION: An image displayed on the LCD 112 of the portable information terminal is enlarged through a free-form surface prism and displayed on the window part of a casing. A cursor displayed on the window part is controlled according to the instruction from an input device 140. When the start of individual authentication processing is instructed by the input device 140, a CPU 121 radiates infrared ray to the eyeballs of a user from an infrared ray source 172 to make an imaging device 172 acquire iris information. The acquired iris information is compared with the individual authentication information stored in a ROM 123, thereby, the CPU 121 executes the individual authentication. ;COPYRIGHT: (C)2003,JPO



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(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開2003－242125
（Ｐ2003－242125Ａ）
(43)公開日　平成15年８月29日(2003.8.29)

(51)Int.Cl.⁷	識別記号	ＦＩ	テーマコード（参考）
Ｇ０６Ｆ　15/02	３１５	Ｃ０６Ｆ　15/02	３１５Ａ　５Ｂ０１９
	３１０		３１０Ｄ　５Ｂ０８５
			３１０Ｚ　５Ｊ１０４
	３１５		３１５Ｒ　５Ｋ０２７
	３６０		３６０Ｚ　５Ｋ０３６

審査請求　未請求　請求項の数24　ＯＬ　（全 23 頁）　最終頁に続く

(21)出願番号　特願2002－40451(Ｐ2002－40451)

(22)出願日　平成14年２月18日(2002.2.18)

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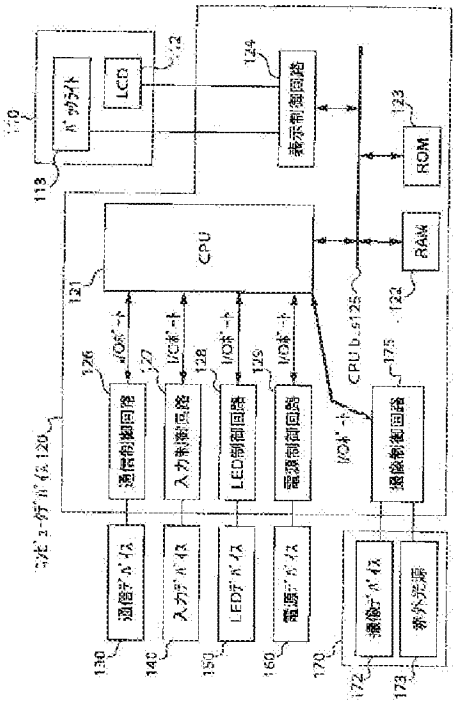
(74)代理人　100076428
弁理士　大塚　康徳　（外３名）

最終頁に続く

(54)【発明の名称】　携帯情報端末、認証補助端末及び個人認証方法

(57)【要約】
【課題】　携帯情報端末を用いて安全かつ簡単に個人認証を実現する。
【解決手段】　携帯情報端末のＬＣＤ１１２に表示された画像は、自由局面プリズムを通して拡大され、筐体の窓部に表示される。窓部に表示されるカーソルを入力デバイス１４０からの指示に応じて制御される。入力デバイス１４０により個人認証処理の起動を指示されると、ＣＰＵ１２１は、赤外光源１７３からユーザの眼球に赤外光を照射させ、撮像デバイス１７２で虹彩情報を取得させる。取得された虹彩情報と、ＲＯＭ１２３に記憶される個人認証情報とを比較することでＣＰＵ１２１は個人認証を実行する。



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【特許請求の範囲】
【請求項１】　手で把持可能な筐体と、
前記筐体に設けられた窓部と、
前記窓部の内側に設けられた拡大光学部と、
前記拡大光学部を経由して前記窓部に画像情報を表示する表示部と、
前記表示部により表示されるカーソルの動きを制御するための指示情報を入力する入力部と、
を備えたことを特徴とする携帯情報端末。
【請求項２】　前記拡大光学部は、自由曲面プリズムを含むことを特徴とする請求項１に記載の携帯情報端末。
【請求項３】　前記窓部の面積は、前記携帯情報端末のユーザが前記窓部に接眼している際に、第三者が実質的に前記窓部を覗くことのできない程度の面積であることを特徴とする請求項１又は請求項２に記載の携帯情報端末。
【請求項４】　前記表示部及び前記入力部を制御する制御部をさらに備え、前記制御部は、前記表示部にキーボード画像を表示させるよう制御し、さらに、前記入力部からクリック信号が入力されたときのカーソル位置に対応するキーを入力情報とすることを特徴とする請求項１乃至請求項３のいずれか１項に記載の携帯情報端末。
【請求項５】　生体情報を入力するための生体情報入力部をさらに備え、
前記制御部は、入力された生体情報に基づいて認証処理を実行することを特徴とする請求項１乃至請求項４のいずれか１項に記載の携帯情報端末。
【請求項６】　少なくとも一つの暗号アルゴリズムを実装した暗号化部と、
他の機器と情報を交換するための通信部と、
をさらに備え、
前記制御部は、前記入力された生体情報に基づいて前記暗号化部により前記情報を暗号化させ、暗号化された情報を前記通信部により送信させることを特徴とする請求項５に記載の携帯情報端末。
【請求項７】　前記通信部は、小電力の無線通信手段であることを特徴とする請求項６に記載の携帯情報端末。
【請求項８】　前記無線通信手段は、Ｂｌｕｅｔｏｏｔｈ仕様に準拠しているか又は、該Ｂｌｕｅｔｏｏｔｈ仕様よりも微弱な送信出力を使用して通信することを特徴とする請求項７に記載の携帯情報端末。
【請求項９】　前記生体情報入力部は、ユーザの眼の虹彩パターン、網膜パターン、指紋又は声紋に関する情報を入力することを特徴とする請求項５乃至請求項８のいずれか１項に記載の携帯情報端末。
【請求項１０】　前記暗号化部は、ＳＳＬ（Ｓｅｃｕｒｅ Ｓｏｃｋｅｔ Ｌａｙｅｒ）に対応した暗号アルゴリズムを備え、
前記通信部は、前記ＳＳＬの通信手順に則して、通信相手と暗号化された情報を通信することを特徴とする請求項６乃至請求項９のいずれか１項に記載の携帯情報端末。
【請求項１１】　前記通信部は、個人認証処理を実行する情報処理装置に対し、前記個人認証処理に必要な個人認証情報を送信することを特徴とする請求項６乃至請求項１０のいずれか１項に記載の携帯情報端末。
【請求項１２】　前記情報処理装置は、前記通信部と通信する通信手段を備えた銀行端末又はネットワーク上のサーバであることを特徴とする請求項１１に記載の携帯情報端末。
【請求項１３】　前記暗号化部は、前記入力された生体情報を鍵情報として利用することを特徴とする請求項６乃至請求項１２のいずれか１項に記載の携帯情報端末。
【請求項１４】　前記暗号化部により使用される複数の鍵情報を記憶する記憶部をさらに備え、
前記制御部は、前記入力された生体情報に基づいて、前記記憶部に記憶される複数の鍵情報の中から少なくとも１つの鍵情報を選択し、選択された鍵情報を前記暗号化部に使用させることを特徴とする請求項１３に記載の携帯情報端末。
【請求項１５】　前記暗号化部は、公開鍵暗号方式を用いた電子署名によって署名情報を生成することを特徴とする請求項６乃至請求項１４のいずれか１項に記載の携帯情報端末。
【請求項１６】　画像を表示するための表示部と、該表示部に表示された画像を光学的に拡大する拡大光学部と、前記表示部に表示される画像に応じた制御指示を入力する入力部とを備えた携帯情報端末を使用する個人認証方法であって、
前記制御指示が認証処理の開始要求であるか否かを判定するステップと、
前記制御指示が認証処理の開始要求であると判定されると、前記携帯情報端末のユーザに係る生体情報を入力するステップと、
前記生体情報及び予め登録された個人認証情報に基づいて前記ユーザが正当なユーザであるか否かを判定するステップと、
前記ユーザが正当なユーザである場合に所定の情報を出力するステップと、
を備えることを特徴とする個人認証方法。
【請求項１７】　前記所定の情報は、通信回線を介して他の機器に送信され、該機器において検証されるパスワード関連情報であることを特徴とする請求項１６に記載の個人認証方法。
【請求項１８】　前記パスワード関連情報は、アカウント情報及びパスワード情報を含んでいることを特徴とする請求項１７に記載の個人認証方法。
【請求項１９】　使用に際しパスワード関連情報を要求する情報処理装置に対して、通信回線を介して該パスワード関連情報を送信する認証補助端末であって、

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前記パスワード関連情報を記憶する第１の記憶手段と、
前記パスワード関連情報の送信を許可するための許可情報を記憶する第２の記憶手段と、
前記認証補助端末の使用者から生体情報を入力する生体情報入力手段と、
前記生体情報と前記許可情報とに基づいて、前記パスワード関連情報の送信が許可されているか否かを判定する判定手段と、
前記送信が許可されていると判定されると、前記パスワード関連情報を送信する送信手段と、
を備えることを特徴とする認証補助端末。
【請求項２０】　前記情報処理装置は、前記パスワード関連情報を受信する受信手段と、前記パスワード関連情報に基づいて個人認証を実行する認証手段とを備えた銀行端末又はネットワーク上のサーバであることを特徴とする請求項１９に記載の認証補助端末。
【請求項２１】　前記生体情報入力手段は、使用者の眼の虹彩パターン、網膜パターン、指紋又は声紋に関する情報を入力することを特徴とする請求項１９又は請求項２０に記載の認証補助端末。
【請求項２２】　使用に際しパスワード関連情報を要求する情報処理装置に対して、通信回線を介して該パスワード関連情報を送信する認証補助方法であって、
前記パスワード関連情報と、前記パスワード関連情報の送信を許可するための許可情報とを記憶するステップと、
前記情報処理装置の使用を希望する者から生体情報を入力するステップと、
前記生体情報と前記許可情報とに基づいて、前記パスワード関連情報の送信が許可されているか否かを判定するステップと、
前記送信が許可されていると判定されると、前記パスワード関連情報を送信するステップと、
を備えることを特徴とする認証補助方法。
【請求項２３】　請求項１乃至請求項１５及び請求項１９乃至請求項２１のいずれか１項に記載された前記手段のすべてをコンピュータに機能させるためのプログラムコードを備えたコンピュータプログラム。
【請求項２４】　請求項１６又は請求項２２のいずれか１項に記載された前記ステップのそれぞれをコンピュータに実行させるためのプログラムコードを備えたコンピュータプログラム。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、携帯情報端末に係り、とりわけ、個人認証機能を備える携帯情報端末、その携帯情報端末に適用される個人認証方法、及び、その個人認証機能をコンピュータに実行させるプログラムに関する。
【０００２】
【従来の技術】従来、手のひらサイズの大きさで、個人の知的活動を支援するための情報機器として、携帯情報端末（ＰＤＡ：Ｐｅｒｓｏｎａｌ Ｄｉｇｉｔａｌ Ａｓｓｉｓｔａｎｔ）が開発されている。この携帯情報端末は液晶表示装置を搭載し、スケジュール帳機能、メモ帳機能及び電話帳機能などを備えている。
【０００３】
【発明が解決しようとする課題】情報通信技術の浸透した情報化社会においても、実社会と同様に、プライバシーに対する懸念が高まっている。例えば、従来の携帯情報端末は、少なくとも２０ｃｍ以上ユーザの目から離して使用されることが多いため、液晶表示装置に個人情報が表示されれば、ユーザだけでなく、第三者からも覗き見される危険性があった。
【０００４】そこで、本願発明の目的は、第三者からの覗き見を抑制する携帯情報端末を提供することである。
【０００５】また、認証情報など重要な個人情報などをキーボードから入力する際には、入力された情報がアスタリスクなどでマスクされたとしても、キー入力操作を覗き見ることで第三者に知れ渡る危険性があった。
【０００６】そこで、本願発明の他の目的は、キー入力操作を見ただけでは、入力された情報を第三者が実質的に認識できないような入力部を備えた携帯情報端末を提供する。
【０００７】ところで、銀行端末などでは、依然として、キーボードにより暗証番号を入力させるように構成されている。従って、キー入力操作を覗き見られれば第三者に暗証番号を知られる危険性があった。
【０００８】そこで、本願発明のさらに他の目的は、銀行端末などの情報処理装置から暗証番号などを要求された場合に、内部に記憶された暗証番号を送信する携帯情報端末を提供することを目的とする。
【０００９】
【課題を解決するための手段】上記課題を解決すべく、本願発明は、手で把持可能な筐体と、前記筐体に設けられた窓部と、前記窓部の内側に設けられた拡大光学部と、前記拡大光学部を経由して前記窓部に画像情報を表示する表示部と、前記表示部により表示されるカーソルの動きを制御するための入力部と、を備えたことを特徴とする携帯情報端末を提供する。
【００１０】すなわち、筐体内に設けられた液晶表示装置の表示内容を自由曲面プリズムなどの拡大光学系を用いて拡大し、拡大された表示内容を窓部から覗き込むような構成としたことで、表示内容を第三者が覗きにくくなるのである。
【００１１】なお、筐体のサイズが手で把持可能なサイズであることから、自ずと窓部のサイズも小さいものとなり、第三者からは窓部を覗き難くなる。より具体的な例をあげると、前記窓部の面積は、前記携帯情報端末のユーザが前記窓部に接眼している際に、第三者が実質的

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に前記窓部を覗くことのできない程度の面積であればよいであろう。より覗かれにくくするためには、両手で把持可能なサイズよりも、片手で把持可能なサイズが好ましいかもしれない。

【００１２】他の上記課題を解決すべく、本願発明は、前記表示部及び前記入力部を制御する制御部をさらに備え、前記制御部は、前記表示部にキーボード画像を表示させるよう制御し、さらに、前記入力部からクリック信号が入力されたときのカーソル位置に対応するキーを入力情報とすることを特徴とする。

【００１３】すなわち、物理キーボードに代えてソフトウェアキーボードを備えることで、物理キーの数を減らし、キー入力操作を見ただけでは、どのような情報が入力されているかを第三者に知られにくくしている。

【００１４】また、生体情報を入力するための生体情報入力部をさらに備え、前記制御部は、入力された生体情報に基づいて認証処理を実行するようにしてもよい。すなわち、キー操作に代えて、生体情報を入力することにより認証処理を実行することで、認証時における認証情報の盗難を防止できよう。また、キー入力に比べ、ユーザに要求される入力工程が削減されるため、安全かつ容易に認証処理を実行できよう。

【００１５】さらに他の上記課題を解決すべく、本願発明は、少なくとも一つの暗号アルゴリズムを実装した暗号化部と、他の機器と情報を交換するための通信部と、をさらに備え、前記制御部は、前記入力された生体情報に基づいて前記暗号化部により前記情報を暗号化させ、暗号化された情報を前記通信部により送信させるようにしてもよい。

【００１６】このように携帯情報端末を構成することで、外部の機器と通信をより安全に実行することがかのうとなろう。

【００１７】また、前記通信部は、個人認証処理を実行する情報処理装置に対し、前記個人認証処理に必要な個人認証情報を送信するようにしてもよい。例えば、前記情報処理装置は、前記通信部と通信する通信手段を備えた銀行端末又はネットワーク上のサーバであれば、暗証番号のキー入力を簡略化でき、より安全に、より簡単に暗証番号を銀行端末等に入力することが可能となろう。

【００１８】また、前記暗号化部は、前記入力された生体情報を鍵情報として利用してもよい。

【００１９】また、前記暗号化部により使用される複数の鍵情報を記憶する記憶部をさらに備え、前記制御部は、前記入力された生体情報に基づいて、前記記憶部に記憶される複数の鍵情報の中から少なくとも１つの鍵情報を選択し、選択された鍵情報を前記暗号化部に使用させるようにしてもよい。

【００２０】また、上記課題を解決すべく、本願発明は、使用に際しパスワード関連情報を要求する情報処理装置に対して、通信回線を介して該パスワード関連情報を送信する認証補助端末であって、前記パスワード関連情報を記憶する第１の記憶手段と、前記パスワード関連情報の送信を許可するための許可情報を記憶する第２の記憶手段と、前記認証補助端末の使用者から生体情報を入力する生体情報入力手段と、前記生体情報と前記許可情報とに基づいて、前記パスワード関連情報の送信が許可されているか否かを判定する判定手段と、前記送信が許可されていると判定されると、前記パスワード関連情報を送信する送信手段と、を備えることを特徴とする認証補助端末を提供する。

【００２１】ここで、前記情報処理装置は、前記パスワード関連情報を受信する受信手段と、前記パスワード関連情報に基づいて個人認証を実行する認証手段とを備えた銀行端末又はネットワーク上のサーバであってもよい。

【００２２】また、前記生体情報入力手段は、使用者の眼の虹彩パターン、網膜パターン、指紋又は声紋に関する情報を入力するようにしてもよい。

【００２３】また、上記課題を解決すべく、本願発明は、使用に際しパスワード関連情報を要求する情報処理装置に対して、通信回線を介して該パスワード関連情報を送信する認証補助方法であって、前記パスワード関連情報と、前記パスワード関連情報の送信を許可するための許可情報とを記憶するステップと、前記情報処理装置の使用を希望する者から生体情報を入力するステップと、前記生体情報と前記許可情報とに基づいて、前記パスワード関連情報の送信が許可されているか否かを判定するステップと、前記送信が許可されていると判定されると、前記パスワード関連情報を送信するステップと、を備えることを特徴とする認証補助方法を提供する。

【００２４】

【発明の実施の形態】以下に本願発明の一実施形態を示す。もちろん以下の実施形態は、いわゆる当業者による本願発明の実施を容易にするため提供されるものであり、特許請求の範囲によって確定される本願発明の技術的範囲に含まれるほんの一部の実施形態にすぎない。従って、本願明細書に直接的に記載されていない実施形態であっても、技術思想が共通する限り本願発明の技術的範囲に包含されることは当業者に自明である。

【００２５】なお、便宜上複数の実施形態を記載するが、これらは個別に発明として成立するだけでなく、もちろん、複数の実施形態を適宜組み合わせることでも発明が成立することは、当業者であれば容易に理解できよう。

【００２６】（第１の実施形態）第１の実施形態では、とりわけ、携帯情報端末に使用される表示装置を改良することにより、第三者から表示内容を覗きにくくしたものである。ここでは、当該携帯情報端末の利用例として、携帯電話端末と接続し、携帯電話網を経由してインターネット上のＷＷＷ（Ｗｏｒｌｄ Ｗｉｄｅ Ｗｅｂ）

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サーバ（以下、「Ｗｅｂサーバ」という）に接続し、Ｗｅｂサーバにより提供されるページ情報を携帯情報端末に表示させる動作例について説明する。さらに、本実施形態によれば、表示されたページ情報内にテキスト入力ボックスが含まれ、かつ、そのテキスト入力ボックスをユーザが選択した際には、ソフトウェアキーボード機能が起動され、適切なテキスト入力が可能となる例についても説明する。

【００２７】図１は、本実施形態に係る携帯情報端末の概観図である。（Ａ）は該携帯情報端末の斜視図、（Ｂ）は正面図、（Ｃ）は該携帯情報端末を手で握った様子を示す図である。

【００２８】携帯情報端末の正面には、図１（Ｂ）に示す窓１があり、この窓１は、後述の自由曲面プリズムの接眼側に位置する。ユーザは、本携帯情報端末を手で把持し、眼をこの窓１に近づけて覗き込むことにより、後述の小型液晶ディスプレイの画面を拡大して見ることができる。本携帯情報端末は、電源として電池を用い、また無線通信機能を有するので、ユーザは本携帯情報端末を携帯して、必要な情報を見ることができるようになっている。

【００２９】また図１に示すように、正面から見て左上に操作ボタン２が装着されており、ユーザは操作ボタン２を操作して所望の情報を得るようにする。この操作ボタンには、例えば、わずかの指の動きを検出可能な感圧素子などを用いた入力デバイスにより実現される。この入力デバイスは、ノートブック・コンピュータなどにおいて使用されているポインティングデバイス（マウス）に相当するもので、二次元平面上でのポインティングとボタンクリックとを実現する。

【００３０】図２は、携帯情報端末の断面図である。図中１１２は、情報を表示するための小型液晶ディスプレイ、１１３は小型液晶ディスプレイ１１２に透過光を供給するバックライト、１１１は小型液晶ディスプレイ１１２の画面を拡大するための自由曲面プリズムである。これらの小型液晶ディスプレイ１１２、バックライト１１３、および自由曲面プリズム１１１により拡大系表示デバイス１１０が構成される。３は携帯情報端末の筐体、４は小型液晶ディスプレイ１１２に駆動信号を送るメイン基板である。

【００３１】図３は、自由曲面プリズム１１１における光路を示す図である。自由曲面プリズム１１１には、３つの光学的作用面１１１ａ～１１１ｃが存在する。観察者から最も遠い作用面１１１ｃの近傍には、小型液晶ディスプレイ１１２とバックライト１１３とが配置され、それらは観察者に適切な表示を与える位置に調整される。それぞれの作用面は、バックライト１１３から出た光が小型液晶ディスプレイ１１２を透過し、作用面１１１ｃ、１１１ａ、１１１ｂを経由して観察者に到達するよう設計されている。自由曲面プリズム１１１を利用することにより、画像出力を拡大表示するための拡大光学系をコンパクトサイズで実現できる。本実施形態では、小型液晶ディスプレイ１１２として透過型の液晶表示素子を使用しているが、これに代えて、反射型の液晶表示素子を使用してもよい。その場合、自由曲面プリズムの形状やバックライトの位置を適切に調整することになろう。

【００３２】図４は、携帯情報端末に実装される電気回路を示すブロック図である。携帯情報端末は、小型液晶ディスプレイ（ＬＣＤ）１１２やバックライト１１３等を含む拡大系表示デバイス１１０と、ＳｏＣ（Ｓｙｓｔｅｍ ｏｎ ａ Ｃｈｉｐ）技術によって集積された小型コンピュータデバイス１２０と、Ｂｌｕｅｔｏｏｔｈ準拠の消費電力が小さい通信デバイス１３０と、感圧素子やタクトスイッチを組み合わせることによりポインティングとボタンクリックとを実現した入力デバイス１４０と、点灯や点滅によって複数の表示状態を実現可能なＬＥＤデバイス１５０と、リチウムイオン二次電池などからなる電源デバイス１６０とを備え、これらを手の中に収まるほどの小型サイズの携帯情報端末内に実装している。なお、図１の操作ボタン２が入力デバイス１４０の操作部となる。

【００３３】そして、この携帯情報端末は、通信デバイス１３０を経由してネットワークから得られた情報をコンピュータデバイス１２０で処理し、拡大系表示デバイス１１０を介してユーザに提供するように動作する。

【００３４】コンピュータデバイス１２０の内部は、後述するプログラムによる各種の処理を実行するＣＰＵ１２１と、プログラムを格納したり処理の中間結果を保持したりするためのメモリとなるＲＡＭ１２２と、プログラムやデータなどのソフトウェアを記憶しているＲＯＭ１２３と、プログラムの実行結果を反映するよう小型液晶ディスプレイ１１２およびバックライト１１３を制御する表示制御回路１２４と、ＣＰＵ１２１やＲＡＭ１２２などのデータ通信路となるバス１２５と、通信デバイス１３０を制御する通信制御回路１２６と、入力デバイス１４０を制御する入力制御回路１２７と、ＬＥＤデバイス１５０を制御するＬＥＤ制御回路１２８と、省電力制御などのために電源デバイス１６０を制御する電源制御回路１２９とから構成される。この中で、ＲＡＭ１２２、ＲＯＭ１２３、表示制御回路１２４は、バス１２５を介してＣＰＵ１２１と接続される。通信制御回路１２６、入力制御回路１２７、ＬＥＤ制御回路１２８、ならびに電源制御回路１２９は、Ｉ／Ｏポートを介してＣＰＵ１２１と接続される。そして、これらの回路はＳｏＣ技術によって一つの半導体チップ上に小型実装されている。ワンチップ化が最も効率がよいと思われるが、複数チップにわけて実装してもよいことは当業者に明らかであろう。なお、本構成のＲＯＭ１２３には、マスクＲＯＭのような書き換えが不可能な記憶装置と、フラッシュ

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ROMのような繰り返し書き換え可能な記憶装置とが含まれる。

【００３５】図5は、携帯情報端末とネットワークとの接続形態を示す図である。インターネットなどのネットワーク３５０上には、複数のＷｅｂサーバ４００が存在する。本実施形態における携帯情報端末１００は、Ｂｌｕｅｔｏｏｔｈ網１５０を介して携帯電話端末２００に接続し、携帯電話端末２００は携帯電話回線網２５０を介してＷｅｂサーバ４００に接続する。

【００３６】携帯電話端末２００は、携帯電話回線網２５０への接続機能の他に、Ｂｌｕｅｔｏｏｔｈ通信機能を備える。携帯電話回線網２５０は、実際には、複数の無線基地局や交換機設備から構成されるが、説明を簡潔にするため携帯電話回線網２５０の詳細な説明は省略する。携帯電話回線網２５０からネットワーク３５０への乗り入れには、ルーター３００が介在する。ルーター３００は、多くの場合、ＩＳＰ（Ｉｎｔｅｒｎｅｔ Ｓｅｒｖｉｃｅ Ｐｒｏｖｉｄｅｒ）によって運営されており、携帯電話回線網２５０からネットワーク３５０への架け橋の役割を果たす。

【００３７】なお、本実施形態における携帯情報端末１００の構成を、携帯電話端末２００内に実装してもよい。逆に、携帯情報端末１００に、携帯電話端末２００の携帯電話機能を実装してもよい。

【００３８】携帯情報端末１００から発行されたＷｅｂページ情報のリクエストは、対応のＷｅｂサーバ４００へ送られ、これが受け入れられるとＷｅｂサーバ４００から携帯情報端末１００へＷｅｂページ情報が返送される。さらに、携帯情報端末１００では、受け取ったＷｅｂページ情報をブラウザプログラムにより解析して表示する。

【００３９】なお、携帯情報端末１００から携帯電話端末２００へのＢｌｕｅｔｏｏｔｈ通信では、ダイアルアップ・ネットワーキング・プロファイル（Ｄｉａｌ－ｕｐＮｅｔｗｏｒｋｉｎｇ ｐｒｏｆｉｌｅ）ならびにシリアル・ポート・プロファイル（ｓｅｒｉａｌ ｐｏｒｔ ｐｒｏｆｉｌｅ）に則った通信が行われる。

【００４０】また、ネットワーク上には、複数のＷｅｂブラウザ５００が接続され、同様に、Ｗｅｂサーバ４００に接続し、そこに保持されているページ情報を表示する。なお、Ｗｅｂサーバ４００ならびにＷｅｂブラウザ５００は、広く普及しているＷｅｂ技術を実装したサーバならびにブラウザであり、Ｗｅｂサーバ４００に保持されるページ情報は、ＨＴＭＬなどで記述され、ＵＲＬとして記述されたリンク情報が含まれる。そのリンク情報は、Ｗｅｂブラウザ５００などから別のページ情報へアクセスすることを容易にしている。この別のページ情報は、同じＷｅｂサーバ上に保持されていることもあるし、異なるＷｅｂサーバ上に保持されていることもある。

【００４１】また、携帯電話端末２００は、データ通信機能の他に、広く普及している通常の通話機能を備えているが、本実施形態では、データ通信機能とＢｌｕｅｔｏｏｔｈ通信機能とを使って、携帯情報端末１００からＷｅｂサーバ４００への接続を中継する機能のみに限定して説明する。すなわち、Ｂｌｕｅｔｏｏｔｈ通信によって携帯電話端末２００と携帯情報端末１００との接続が確立されている状態において、携帯情報端末１００内に実装されているダイアルアップ機能により、ＩＳＰの電話番号をダイアルすることを携帯電話端末２００に要求する。これに従い、携帯電話端末２００は、携帯電話回線網において携帯電話端末２００とＩＳＰとのリンクを確立する。そしてさらに、携帯情報端末１００内に実装されている通信スタックにより、携帯情報端末１００とＩＳＰが運営するルーター３００との間に仮想的な通信路を確立する。このようにして携帯電話端末２００は、携帯情報端末１００からＷｅｂサーバ４００への接続を中継する役割を果たす。なお、図5に示すネットワークとは、企業あるいは組織内で運用されるイントラネットである場合もあり、また、広く世界をつないでいるインターネットである場合もある。

【００４２】図6は、Ｗｅｂブラウザ５００がＷｅｂサーバ４００にＷｅｂページ情報を要求する際に使用される最も一般的な通信プロトコルであるＨＴＴＰ（ＨｙｐｅｒＴｅｘｔ Ｔｒａｎｓｆｅｒ Ｐｒｏｔｏｃｏｌ）による通信シーケンスの一例を示す図である。もちろん、ＷＡＰなど他のプロトコルが使用されてもよい。ＨＴＴＰの手順では、はじめに、Ｗｅｂブラウザ５００がＷｅｂサーバ４００との接続を確立し（ＨＴＴＰｃｏｎｎｅｃｔ）、続いて、Ｗｅｂブラウザ５００からＨＴＴＰｒｅｑｕｅｓｔ形式のデータ要求がＷｅｂサーバ４００へと発行される。そして、その要求を受け取ったＷｅｂサーバ４００が要求内容を解析し、ＨＴＴＰｒｅｓｐｏｎｓｅ形式の応答を送り返す。そして、最後に、通信を閉じて（ＨＴＴＰｃｌｏｓｅ）、１つのＨＴＴＰセッションが終了する。

【００４３】ＨＴＴＰｒｅｓｐｏｎｓｅ形式の内容について以下に説明する。ＨＴＴＰｒｅｓｐｏｎｓｅ形式の１行目は、ステイタスラインと定義されている（ＲＦＣ２６１６”ＨＴＴＰ１．１版”）。ここには、ＨＴＴＰバージョンとステイタスコードと理由文とが、空白文字で区切られて並ぶ。特に、２つ目の項目であるステイタスコードは３つの数字から構成され、ＨＴＴＰｒｅｓｐｏｎｓｅ形式の内容を分類するために使われる。

【００４４】図7は、携帯情報端末１００の動作の手順を示すフローチャートである。この動作処理を記述したプログラムは、図4に示すＲＯＭ１２３に記憶され、必要に応じてＣＰＵ１２１によって実行される。この実行に伴い、必要に応じて入力制御回路１２７や表示制御回路１２４あるいは通信制御回路１２６などが起動され

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る。

【００４５】まず、プログラムの開始時点のステップＳ１００１で、設定情報を読み取る。この設定情報に基づき、以降の処理内容が決定される。この設定情報の内容は、ＲＯＭ１２３に保存されている。典型的な設定情報は、ＲＯＭ１２３にプログラムなどと一緒に固定的に保存されているが、一部の設定情報に関しては、ユーザによって設定、変更され、ＲＯＭ１２３の別領域に保存されている。

【００４６】次に、ステップＳ１００２で、ＣＰＵ１２１は、ユーザからの指示を待つ。ここでの待ち受け対象は、典型的には、入力デバイス１４０からの入力信号であるが、通信デバイス１３０からの通信データの到着である場合もある。

【００４７】そして、ステップＳ１００３で、ＣＰＵ１２１は、ユーザからの指示を入力制御回路１２７から受け取る。

【００４８】ステップＳ１００４において、ＣＰＵ１２１は、受け取った指示がプログラムの終了を指示するものであるか否か判定する。終了を指示するものである場合には、ＣＰＵ１２１は、本プログラムを終了する。一方、終了を指示していない場合には、ステップＳ１００５に進む。

【００４９】ステップＳ１００５では、指示内容に応じた処理を実行し、その後、次の指示を待つために、ステップＳ１００２に戻る。なお、ステップＳ１００５において実行される処理のプログラムも、同様にＲＯＭ１２３に記憶され、ＣＰＵ１２１で実行される。

【００５０】図８は、携帯情報端末１００において実行されるＷｅｂアクセス処理の手順を示すフローチャートである。この処理を記述したプログラムは、ユーザからの指示に応じて図７のステップＳ１００５から呼び出されるものであり、Ｗｅｂアクセス機能、すなわちＷｅｂサーバからＷｅｂページ情報を取得し表示する機能を実現する。

【００５１】ユーザからの指示とは、例えば、表示画面上のポインティングカーソルがアンカー位置（リンク情報表示位置）にあるときにユーザによって入力デバイス１４０からクリック信号が入力された場合や、取得すべきＷｅｂページ情報のＵＲＬデータが直接入力された場合などを意味する。

【００５２】まず、ステップＳ２０００で、ＣＰＵ１２１は、拡大系表示デバイス１１０を低消費電力モードに切り替えるよう表示制御回路１２４に命令する。表示制御回路１２４は、例えば、バックライト１１３と小型液晶ディスプレイ１１２への給電を止める。

【００５３】次に、ステップＳ２００１で、ＣＰＵ１２１は、指示されたＵＲＬを取得する。このＵＲＬの指示は、ユーザが直接入力した場合やアンカーを選択した場合などがある。後者の場合には、クリックの位置情報から、ユーザが選択したアンカーを特定し、そこに含まれるリンク情報を取得する。

【００５４】続いて、ステップＳ２００２で、ＣＰＵ１２１は、取得したＵＲＬを解析する。この解析に応じて、ＣＰＵ１２１は、接続すべきＷｅｂサーバやプロトコルなどを決定する。

【００５５】続いて、ステップＳ２００３で、ＣＰＵ１２１は、指示されたＵＲＬが、携帯情報端末１００の自機内に存在するデータに対応するＵＲＬであるか否かを判定する。判定の結果、自機内に存在するならば、ステップＳ２００６に進み、一方、自機内に存在しないならば、ステップＳ２００４に進む。なお、この判定は、ＵＲＬの指示が直接自機内のデータを参照している場合や、外部のデータを参照しているが履歴ファイルや保存ファイルなどにそのデータがキャッシュされている場合をも考慮して判断する。

【００５６】ステップＳ２００４で、ＣＰＵ１２１は、指示されたページ情報が自機内に存在しないので、必要なＷｅｂページ情報を取得するため、指示されたＷｅｂサーバに、ＵＲＬによって指示されたプロトコルで接続する。ここで、典型的にはＨＴＴＰプロトコルが使用されるが、ＦＴＰ（Ｆｉｌｅ Ｔｒａｎｓｆｅｒ Ｐｒｏｔｏｃｏｌ）プロトコルなどが指定される場合もある。なお、プロトコルの指定が省略された時には、ＨＴＴＰプロトコルが使用される。

【００５７】そして、ステップＳ２００５において、ＣＰＵ１２１は、接続先のＷｅｂサーバから、ＵＲＬによって指示されたＷｅｂページ情報を取得し、ステップＳ２００７に進む。具体的には、ＵＲＬで指示されたデータをＷｅｂサーバにリクエストし、その後、Ｗｅｂサーバからのレスポンスを待ち、所望のＷｅｂページ情報を取得する。

【００５８】一方、ステップＳ２００６では、指示されたページ情報が自機内に存在するので、必要なＷｅｂページ情報を自機内から取得し、ステップＳ２００７に進む。

【００５９】次のステップＳ２００７では、ＣＰＵ１２１は、取得したＷｅｂページ情報を解析する。具体的には、ＨＴＭＬ形式などで記述された内容を読み取り、そこに埋め込まれた画像やその他のマルチメディア情報あるいはアンカー（リンク情報）などを検出した上で、ページ情報の論理構造を決定する。

【００６０】続いて、ステップＳ２００８で、ＣＰＵ１２１は、拡大系表示デバイス１１０を通常モードに切り替えるべく表示制御回路１２４を制御する。すなわち、表示制御回路１２４は、バックライト１１３および小型液晶ディスプレイ１１２への給電を止めていた場合には、給電を再開する。

【００６１】そして、ステップＳ２００９で、解析したＷｅｂページ情報を小型液晶ディスプレイ１１２に表示

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させる。具体的には、埋め込まれた種々の情報や解析結果の論理構造に基づいて、取得したＷｅｂページ情報を適切な配置にレイアウトする。そして、そのレイアウト結果を小型液晶ディスプレイ１１２の画面に反映する。

【００６２】そして、ステップＳ２０１０で、ユーザにＷｅｂページ情報へのアクセス完了を通知する。ここでは、通信相手となる携帯電話端末２００の着メロ機能を使ってユーザに通知する。具体的には、携帯情報端末１００が、Ｂｌｕｅｔｏｏｔｈ通信のシリアル・ポート・プロファイル仕様を用いて、携帯電話端末２００に直接接続し、予め取り決めておいた着メロ機能インタフェースに則して、適切なメロディデータを受け取り、そのメロディの演奏実行を指示する。典型的には、ＨＴＴＰｒｅｓｐｏｎｓｅ形式のステイタスコードごとにステイタスを識別可能なメロディの演奏を指定する。

【００６３】その後、ＣＰＵ１２１は、ユーザからの次の指示を待つため、本処理を終了し、図７のステップＳ１００２に戻る。

【００６４】図９は、図８に示すＷｅｂアクセス処理によって小型液晶ディスプレイ１１２に表示されたＷｅｂページ情報の一例を示す図である。ここでは、ＵＲＬデータ「ｈｔｔｐ：／／ｗｗｗ．ｘｙｚｎｅｗｓ．ｃｏｍ／ｊｐ／」が直接入力された結果表示されたＷｅｂページ情報を示す。このＷｅｂページ情報は、ＣＰＵ１２１及び表示制御回路１２４によって、表示信号に変換され、小型液晶ディスプレイ１１２に伝えられる。小型液晶ディスプレイ１１２は、表示信号に基づいて画像を表示する。バックライト１１３は、表示された画像に対し光を照射する。最後に、表示画像は、自由曲面プリズム１１１の光学的拡大作用を介することによって、観察者位置に結像される。

【００６５】なお、本実施形態における携帯電話端末２００の着メロ（着信メロディ）機能インタフェースは、携帯電話端末２００に備わるＢｌｕｅｔｏｏｔｈ通信デバイスを介して、携帯情報端末１００から適切なメロディデータを受け取り、そのメロディデータを、携帯電話端末２００に内蔵の音源装置に受け渡すものである。この際の携帯情報端末１００と携帯電話端末２００との間のデータ通信は、Ｂｌｕｅｔｏｏｔｈ通信におけるシリアル・ポート・プロファイル仕様に則り行なわれる。

【００６６】図１０は、携帯情報端末１００において実行される設定処理の手順を示すフローチャートである。この処理を記述したプログラムは、ユーザからの指示に応じて図７のステップＳ１００５から呼び出されるものであり、携帯情報端末１００の各種設定項目にユーザの指定する値を設定する機能を実現する。ユーザからの指定とは、具体的には例えば、表示画面上のメニュー項目から設定機能を選択して、この機能により指定を行う場合や、ユーザによる直接入力の場合などである。

【００６７】まず、ステップＳ３００１において、ＣＰＵ１２１は、携帯情報端末１００の現在の設定値を小型液晶ディスプレイ１１２に表示し、設定セッションを開始する。図１１は、小型液晶ディスプレイ１１２に表示された設定値の一例を示す図である。

【００６８】続いて、ステップＳ３００２において、ＣＰＵ１２１は、入力デバイス１４０からの設定画面に対するユーザ入力を待ち受ける。

【００６９】ステップＳ３００３において、ＣＰＵ１２１は、入力デバイス１４０からのユーザ入力を判定する。ここで、ユーザ入力が設定終了命令であるならば、ステップＳ３００４に進む。設定終了命令とは、「ｓｕｂｍｉｔ」と「ｃａｎｃｅｌ」とのいずれかである。一方、設定終了命令でないならば、ステップＳ３００７に進む。

【００７０】ステップＳ３００４で、さらに、ＣＰＵ１２１は、設定終了命令が、「ｓｕｂｍｉｔ」であるか「ｃａｎｃｅｌ」であるかを判定する。前者である場合には、ステップＳ３００５に進み、設定セッション中の設定内容の保持データを携帯情報端末１００に反映した後に、処理を終了する。ここで、設定内容を携帯情報端末１００に反映する処理には、設定内容をＲＯＭ１２３へ保存することも含まれる。

【００７１】一方、「ｃａｎｃｅｌ」が指示された場合には、ステップＳ３００６に進み、設定セッションの内容を破棄し、処理を終了する。

【００７２】ステップＳ３００３で設定終了命令以外であると判定されたならば、ステップＳ３００７に進み、ＣＰＵ１２１は、ユーザ入力によって受け取った設定内容を設定セッション内の保持データならびに画面上に反映させる。そして、次のユーザ入力を待ち受けるために、ステップＳ３００２に戻る。

【００７３】ところで、認証情報など重要な個人情報はできる限り安全に入力されなければならない。そこで、本実施形態では上記の構成に加え、ソフトウェアキーボードを実現する。

【００７４】図１２は、携帯情報端末１００において実行されるソフトウェアキーボード処理の手順を示すフローチャートである。この処理を記述したプログラムは、ユーザからの指示に応じて図７のステップＳ１００５から呼び出されるものであり、画面上に表示されたソフトウェアキーボードと入力デバイス１４０とを用いてテキスト入力を行うことができるテキスト入力機能を実現する。

【００７５】ユーザからの指示とは、例えば、表示画面上のポインティングカーソルがテキスト入力ボックス（ＨＴＭＬ記述のＴＥＸＴ型のＩＮＰＵＴタグを持つ要素など）位置にあるときに、ユーザによって入力デバイス１４０からクリック信号が入力された場合や、取得すべきＷｅｂページ情報のＵＲＬデータが直接入力される場合、あるいは、設定画面中でテキスト入力エリアが選

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択された場合などである。

【0076】まず、ステップS4001で、CPU121は、現在の環境や状況を表すコンテクスト情報を取得する。CPU121は、HTMLなどで記述されたページに記載されたテキスト入力要素（テキスト入力ボックス）でクリックが行われたことを入力制御回路127からの信号に基づいて検出すると、ソフトウェアキーボードを起動する。コンテクスト情報は、ページ情報上のテキスト入力要素の表示位置情報や、URLなどのページ識別情報や、ページ内の要素に割り当てられたHTML記述などのタグ情報などから構成される。なお、このコンテクスト情報に既にテキストデータが保持されている場合、例えば、テキスト入力ボックスがすでに値を保持している場合は、CPU121は、それをテキスト入力セッションのテキスト変数にコピーし、テキスト変数を初期化する。テキスト入力ボックスに何も含まれない場合には、CPU121は、テキスト変数を空文字列で初期化する。

【0077】次に、ステップS4002で、CPU121は、小型液晶ディスプレイ112にキーボード相似の仮想的なキーボード（以下「ソフトウェアキーボード」と呼ぶ）を表示させ、テキスト入力セッションを開始する。このソフトウェアキーボードには、通常のキーボードに含まれる文字入力用のキーに加えて、事前に登録された複数の語句（フレーズ）を入力するためのキーが含まれてもよい。事前登録された語句とは、頻繁に入力対象となることが予想される語句であり、事前に登録しておいて、それらの語句の入力時に、対応のキーを操作するだけで入力完了するためのものである。事前登録語句は、例えば、ユーザの名前、住所、電話番号、ログインアカウント、メールアドレスなどである。なお、事前登録語句にはセキュリティレベルの属性も登録され、セキュリティレベルの高い語句（例えば、預金口座番号、パスワードなど）は、後述のように、正当なユーザ以外が入力に使用することはできないようにしてもよい。事前登録語句の例を図13に示す。また、図14は、この事前登録語句の入力キーを含んだソフトウェアキーボードが小型液晶ディスプレイ112に表示される例を示している。

【0078】次に、ステップS4003で、CPU121は、入力デバイス140から、ソフトウェアキーボード上のいずれかのキーの選択指定（ポインティング）を入力し、入力された情報に基づいてユーザからの指示を受け取る。

【0079】続いて、ステップS4004で、CPU121は、受け取った指示が、ソフトウェアキーボードを使用したテキスト入力の終了を指示する命令であるか否かを判定する。入力終了命令であるならば、ステップS4005に進み、入力終了命令でないならば、ステップS4008に進む。ここで入力終了命令とは、図14に示す画面上のキー「ｓｕｂｍｉｔ」またはキー「ｃａｎｃｅｌ」がポインティングされることによって指示される命令である。

【0080】ステップS4005では、さらに、CPU121は、入力終了命令が、「ｓｕｂｍｉｔ」であるか、または「ｃａｎｃｅｌ」であるかを判定する。前者である場合には、ステップS4006に進み、テキスト入力セッション中のテキスト変数のテキストデータ値を、ソフトウェアキーボードを起動したコンテクストに反映し、本処理を終了する。ここで、テキストデータ値をコンテクストに反映する処理には、現在表示中のページ情報の適切な部分にテキストデータを表示することも含まれる。

【0081】一方、入力終了命令が「ｃａｎｃｅｌ」である場合には、ステップS4007に進み、テキスト入力セッションの内容を破棄し、処理を終了する。

【0082】ステップS4004で、受け取った指示が入力終了命令以外であると判定されたならば、ステップS4008に進み、指示内容に応じてテキスト入力セッションのテキスト変数を操作するよう処理する。この処理は、典型的には、テキスト変数への文字列の追加であるが、テキスト変数での編集位置の変更や文字の削除などの編集操作である場合もある。文字列の追加では、ソフトウェアキーボードを操作して所望の文字を選択して入力を行うが、また事前登録語句に対応するキーを操作して事前登録語句を簡単に入力することもできる。

【0083】ただし、このステップS4008の処理において、ステップS4003で受け取った指示内容が事前登録語句のテキスト変数への追加操作であり、かつ、その登録語句のセキュリティレベル（機密度合い）が所定の値（例えば4）よりも高い場合には、CPU121は、後述する認証手順（図15）を要求し、追加操作を実行すべきか否かを判定する。そして、認証された場合だけ、当該登録語句の入力を行う。なお、セキュリティレベルが所定の値よりも高い登録語句には、図14に示すように、鍵イメージのアイコンがキーとして予め設定されていて、セキュリティレベルの高い登録語句として他と区別されている。そして、次の指示を受け取るためステップS4003に戻る。

【0084】なお、ソフトウェアキーボード上のキーをポインティングするにあたっては、通常のポインティングカーソル（マウスカーソル相当）を表示せず、注目されているキーのみを点滅表示することでポインティングされているキーを表してもよい。そして、ユーザが入力デバイス140を操作して、ポインティングされるべきキーの移動を行った際には、その操作移動量に合せて、ポインティングされるべきキーをスキップ移動するようにしてもよい。このように制御プログラムを構成すれば、ポインティングカーソルによる点の選択ではなく、キー（またはボタン）を単位とした選択をも可能となろ

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う。これによって、ユーザは、ソフトウェアキーボード上のいずれかのキーを簡単にポインティングすることができる。

【００８５】ところで、暗証番号等の個人情報もソフトウエアキーにより一発入力できれば、ユーザの使い勝手は向上する。しかしながら、誰でも自由に個人情報を一発入力できたのでは、携帯情報端末が盗難された場合に悪用される恐れがある。そこで、本実施形態では、図１４に示すように銀行の口座番号、暗証番号などを一発入力する際には、事前に認証処理を設けて、安全性を確保したものである。

【００８６】図１５は、携帯情報端末１００において実行される認証手順の一例を示すフローチャートである。この処理を記述したプログラムは、図１２のステップＳ４００３で受け取った指示内容が事前登録語句のテキスト変数への追加操作であり、かつ、その登録語句のセキュリティレベルが所定の値よりも高い場合（すなわち、図１４に示されるように、ソフトウェアキーボード上の当該登録語句に鍵イメージのアイコンがキーとして予め設定されている場合など）に、図１２のステップＳ４００８から呼び出されるものであり、事前登録語句の入力に先立つ認証機能を実現する。

【００８７】まず、ステップＳ５００１では、ＣＰＵ１２１は、図１４に示すソフトウェアキーボードと類似のソフトウェアキーボードを小型液晶ディスプレイ１１２に表示させ、認証セッションを開始する。ここで表示されるソフトウェアキーボードは、例えば図１６に示すように、事前登録語句の入力キーを除いたものとなる。なおこの時、ＣＰＵ１２１は、認証セッションに保持する認証コード変数を空にして初期化する。

【００８８】次に、ステップＳ５００２で、ＣＰＵ１２１は、そのソフトウェアキーボード上のいずれかのキーをポインティングすることで表されたユーザからの指示を入力デバイス１４０から受け取る。

【００８９】続いて、ステップＳ５００３で、ＣＰＵ１２１は、受け取った指示が、ソフトウェアキーボードを使用した認証コードの入力の終了命令であるか否かを判定する。入力終了命令であるならば、ステップＳ５００４に進み、入力終了命令でないならば、ステップＳ５００７に進む。ここで入力終了命令とは、図１６に示す画面上のキー「ｓｕｂｍｉｔ」またはキー「ｃａｎｃｅｌ」がポインティングされることによって指示される命令である。

【００９０】ステップＳ５００４で、ＣＰＵ１２１は、入力終了命令が「ｓｕｂｍｉｔ」であるかまたは「ｃａｎｃｅｌ」であるかを判定する。前者である場合には、ステップＳ５００５に進み、認証セッション中の認証コード変数の値を事前登録された認証用パスワードと比較し、その比較結果を認証結果として出力して、本処理を終了する。認証用パスワードは、例えば、ＲＯＭ１２３に記憶して置き、ＣＰＵ１２１によって読み出される。また、認証用パスワードの長さは、入力効率の観点から、事前登録語句の長さよりも短い方が望ましいかもしれない。また、認証用パスワードは、複数の事前登録語句キーに対して共通に設定されることで、認証パスワードの亡失を防止してもよい。さて、入力終了命令が「ｃａｎｃｅｌ」である場合には、ステップＳ５００６に進み、認証セッションの内容を破棄し、「認証できず」という認証結果を出力して、処理を終了する。

【００９１】ステップＳ５００３で、ＣＰＵ１２１は、受け取った指示が認証コードの入力終了命令以外であると判定すると、ステップＳ５００７に進み、指示内容に応じて認証セッションの認証コード変数を操作するよう処理する。このステップＳ５００７の処理は、典型的には、認証コード変数への文字の追加であるが、文字の削除などの編集操作である場合もある。認証コード変数への文字の追加では、ソフトウェアキーボードを用いてユーザのパスワードが入力される。そして、次の指示を受け取るためステップＳ５００２に戻る。

【００９２】以上述べたように、手の中に入る程度に小型化された本実施形態の携帯情報端末では、携帯電話端末２００と組み合わせて利用することで、携帯電話回線網２５０を経由してインターネット３５０上のＷｅｂサーバ４００にアクセスし、なおかつ、得られたＷｅｂページ情報を大画面表示し、操作することが可能になる。

【００９３】特に、Ｗｅｂページ情報に含まれるテキスト入力ボックスへのテキスト入力（ＴＥＸＴ型のＩＮＰＵＴタグを持つ要素などの選択やＵＲＬの直接入力など）では、ソフトウェアキーボード機能を使用することで、実際のキーボードを備えることが難しい小型機器でのテキスト入力を可能にしている。

【００９４】さらに、このソフトウェアキーボード機能では、通常のポインティングデバイスによる画面上での点の選択ではなく、ソフトウェアキーボード上に表されるキー（またはボタン）を単位としたスキップ移動によって、キー（またはボタン）を単位として高速かつ正確なテキスト入力が可能となる。

【００９５】また、本実施形態のソフトウェアキーボード機能では、通常のキーに加えて、頻度の高い入力が予想される語句を事前に登録しておき、こうした語句に対応するキーを選択するだけで、そうした語句を入力することのできるインタフェースを備えており、入力が頻繁に行われる特定の複数の語句に関しては、一層簡便なテキスト入力を可能にしている。

【００９６】加えて、上記の事前登録語句の事前登録においてセキュリティレベルを併せて登録しておき、セキュリティレベルの高い事前登録語句が選択指定された場合には、ユーザの本人認証を実行し、認証された場合だけ、当該語句の入力を行えるようにする。これにより、他人によって事前登録語句を無闇に入力に使用されてし

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まうことを防止でき、高い安全性が確保できる。併せて、入力頻度の高い語句を対応キー１つの選択で入力できるという効率の良さも兼ね備え、高い安全性と効率の良さという相反する特徴の両立を実現している。

【００９７】なお、本実施形態では、ソフトウェアキーボード機能を起動した際のコンテクスト情報を用いて、テキスト入力セッションのテキスト変数の値を初期化しているが、それ以外にも、コンテクスト情報を利用することが考えられる。例えば、コンテクスト情報に含まれるテキスト入力ボックスの表示位置情報を用いて、ソフトウェアキーボードの表示位置を制御し、テキスト入力ボックスがソフトウェアキーボードによって隠されないように表示するように制御することもできる。逆に、テキスト入力ボックスを覆い隠すようにソフトウェアキーボードを表示することもできる。

【００９８】また、コンテクスト情報に含まれるＵＲＬなどのページ識別情報やタグ情報などを用いて、これらと事前登録語句との関連性を算出し、関連性が高い値が算出された語句を、図１４に示す小型液晶ディスプレイ１１２の画面（事前登録語句の入力キーを含んだソフトウェアキーボードが表示される画面）に優先的に表示し、選択が効率的にできるようにしてもよい。さらに、上記の算出された関連性が一定の値よりも大きくなっている場合には、ソフトウェアキーボードの表示に先立って、関連性の高い語句を並べ、ユーザに直接選択させるダイアログ画面を表示するようにしてもよい。

【００９９】また、本実施形態では、事前登録された語句に対応する各キーを、図１４に示すように、ソフトウェアキーボードの下部に表示しているが、これに代わって、ソフトウェアキーボードだけを示す画面と、事前登録語句に対応する各キーを示す画面とを用意し、それぞれの画面を所定のボタンの操作によって切り替えるようにしてもよい。その際、その所定のボタンは、ソフトウェアキーボードの一部に表示されるソフトウェアのボタンであってもよいし、また同等の機能を割り当てられた携帯情報端末１００のハードウェアのスイッチであってもよい。

【０１００】また、本実施形態では、本人認証を必要とするセキュリティレベルの高い登録語句に対して、それらの登録語句の対応キーとして鍵イメージのアイコンを利用して他の登録語句と区別しているが、必ずしも、表示画面上に区別のためのアイコンを表示する必要はない。また、セキュリティレベルに応じて登録語句を２つに区分するのでは、セキュリティレベルに応じて登録語句を３つ以上に区分し、各区分毎の登録語句に対して異なったセキュリティ管理を行うようにしてもよい。

【０１０１】また、本実施形態では、図１４に示される事前登録語句に対応するキーに、図１３に示される「表示」欄の文字列が表示されるようになっている。これに代わって、対応キーに、適切なアイコン画像を表示するようにしてもよい。

【０１０２】また、本実施形態では、自由曲面プリズム１１１を用いた小型の携帯情報端末に本発明を適用しているので、ソフトウェアキーボードはユーザにしか見えず、他人に覗き見られることはないが、通常のＣＲＴや液晶画面を用いた装置に本発明を適用する場合には、セキュリティレベルの高い語句を表示するに際しては、他人への漏洩を回避するような表示方法を工夫する必要がある。具体的には、該当語句部分の表示に半透明色を使用したり、該当語句部分を塗りつぶしたりするような表示が考えられる。あるいは、パーソナルコンピュータにおいてパスワード入力を行う際に行われる表示と同様に、該当語句部分の文字を　”＊”（アスタリスク）に置き換えて表示するようにしてもよい。

【０１０３】（第２の実施形態）第１の実施形態では、事前登録された語句の中でセキュリティレベルの高い語句が、入力すべき語句として選択指定された場合に、認証セッションを生成して、ソフトウェアキーボードを用いてユーザのパスワードを入力させ、認証を行うものであった。しかし、この方法では、せっかく語句を事前登録しておくことで当該語句の入力の煩わしさを低減することができるが、パスワードの入力といった煩わしさが残ってしまう。

【０１０４】そこで第２の実施形態では、生体情報（バイオメトリクス）を利用した認証セッションを導入することで、パスワードを入力するという操作を簡略化し、これによって、一層効率的で安全な語句入力を実現することを目的としている。特に、本実施形態では、虹彩（アイリス）情報を用いた認証セッションを採用するものである。

【０１０５】なお、眼球の虹彩や指紋などに代表されるバイオメトリクスは、本人認証のキー情報として利用可能である。例えば、米国センサ社（Ｓｅｎｓａｒ，Ｉｎｃ．）では、虹彩情報に基づく高精度の本人認証技術を提供している。この技術では、標準的なビデオカメラを用いて、眼球の虹彩を１メートルほどの距離から撮影し、これを基に虹彩の画像情報を抽出／コード化して２５６バイトにまでデータ圧縮し、本人認証用コードとしている。また、日本電気株式会社では、指紋認証モジュールを開発するとともに、そのモジュールをＰＣＭＣＩＡインタフェースのＰＣカードに実装して販売している。

【０１０６】さて、第２の実施形態の構成は、基本的に第１の実施形態の構成を基礎としている。そのため、共通する技術事項についての説明は省略し、記載の明瞭性を心がけることとする。第２の実施形態は、第１の実施形態に比べ、新たな撮像光学系を含むとともに、電気回路の一部とソフトウェアキーボード処理に係る認証手順について差異がある。

【０１０７】図１７は、第２の実施形態における撮像光

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学系の構成を示す図である。ここで、第1の実施形態における構成と同一部分には同一の参照符号を付してその説明を省略する。第2の実施形態では、自由曲面プリズム111の周辺に、認証に利用される生体情報を入力するための生体情報入力手段が配置される。例えば、生体情報として虹彩情報を入力する場合は、結像光学系171、撮像デバイス172、赤外光源173を含む撮像光学系が配置される。

【0108】赤外光源173は、虹彩画像を得るために観察者の目に対し赤外線を照明するための光源である。光源としては、例えば、観察者にとって視覚感度の低い赤外光を発光する発光ダイオードなどを用いればよい。結像光学系171は、観察者の虹彩で反射した赤外光を撮像デバイス172に集めるための光学系である。なお、結像光学系171は、自由曲面プリズム111の光学的作用面111aの作用をキャンセル（相殺）するように設計されることが望ましい。撮像デバイス172は、虹彩画像データを取得するためのイメージセンサーであり、CMOSセンサーデバイスなどで構成される。

【0109】図18は、第2の実施形態における携帯情報端末に実装される電気回路を示すブロック図である。ここで、第1の実施形態における構成と同一部分には同一の参照符号を付してその説明を省略する。第2の実施形態では、図4に示す第1の実施形態における電気回路に対して、撮像デバイス172、赤外光源173、ならびにそれらを制御するための撮像制御回路175が新たに追加されている。撮像制御回路175は、入力制御回路127などと同様に、I／Oポートによって CPU121に接続され、CPU121からの制御信号に従って、赤外光源173のオン／オフや、撮像デバイス172から取り込んだ画像データの転送を行う。

【0110】図19は、携帯情報端末100において実行される認証手順の一例を示すフローチャートである。この認証処理を記述したプログラムは、第1の実施形態と同様に、図12のステップS4008から呼び出されるものであり、事前登録語句の入力に先立つ認証機能を実現する。具体的には、図12のステップS4003で受け取られた指示の内容が事前登録語句をテキスト変数に追加するための指示であって、その登録語句のセキュリティレベルが所定の値よりも高い場合（換言すれば、ソフトウェアキーボードにおいて、当該登録語句に、鍵イメージのアイコンがキーとして予め設定されている場合）に、当該認証処理プログラムが呼び出される。

【0111】まず、ステップS6001では、CPU121は、赤外光源173ならびに撮像デバイス172に給電し、撮像準備を開始するよう撮像制御回路175に指示する。

【0112】次に、ステップS6002で、CPU121は、赤外光源173が安定するのを待って、撮像デバイス172で取り込まれた画像データをRAM122に転送するよう撮像制御回路175に指示する。RAM122には、認証用画像変数を格納する所定の記憶領域が予め設けられ、該画像データはこの所定の記憶領域に格納される。

【0113】ステップS6003で、CPU121は、赤外光源173ならびに撮像デバイス172への給電を中止するよう撮像制御回路175に指示する。

【0114】そして、ステップS6004で、CPU121は、RAM122に格納された認証用画像変数を分析し、虹彩に相当する部分画像を抽出してコード化する。こうして得られた認証用虹彩コード変数をRAM122の別の所定記憶領域に保持する。この際のコード化には、例えば、センサ社が提供する本人認証技術が利用される。

【0115】ステップS6005で、CPU121は、RAM122から認証用虹彩コード変数の値を読み出すとともに、ROM123から事前登録されている本人認証用虹彩コードを読み出し、両者を比較し、その比較結果を認証結果として出力し、本処理を終了する。

【0116】以上のように、第2の実施形態では、本人認証にバイオメトリクス情報、特に虹彩パターンを用いることで、認証のためにパスワードを入力する煩わしさを低減している。

【0117】なお、本実施形態では、虹彩画像を得るために赤外光源を使って眼球を照明しているが、これに代わって、可視光源を利用するようにしてもよい。可視光源を利用した場合には、虹彩のパターン情報の他に、虹彩の色情報などを認証に利用することができる。

【0118】また、本実施形態では、バイオメトリクス情報として虹彩情報を用いているが、同様の仕組みで網膜情報を利用してもよい。また、これに代わって、指紋情報や声紋情報を用いて認証を行うようにしてもよい。この場合は、生体情報入力手段として、指紋情報入力センサや声紋情報入力センサが用いられることになろう。

【0119】また、本実施形態では、携帯情報端末100に内蔵された認証手段を用いて本人認証を行うようにしているが、これに代えて、携帯情報端末100が外部認証機器と通信して本人認証を行うようにしてもよい。この場合の外部認証機器としては、セキュアICカード端末や、UIM（User Identity Module）を内蔵した携帯電話端末200などが考えられる。また、この場合の通信形態は、USBなどの有線接続であってもよいし、Bluetoothなどの無線通信であってもよい。

【0120】さらに、本人認証手段は、本実施形態のように単一の手法によって行うのではなく、これまで説明したバイオメトリクス利用の他、外部認証機器の利用、ソフトウェアキーボードを使ったパスワード認証などを組み合わせて利用するようにしてもよい。さらに、事前登録された語句のセキュリティレベルに応じて、これら

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を使い分けるようにしてもよい。さらに、本実施形態では、バイオメトリクスに基づく本人認証を安全なソフトウェアキーボードの実現に利用しているが、本実施形態の構成を、直接、インターネット上での課金サービスや個人情報サービスあるいはインターネットバンキングサービスなどの認証に応用してもよい。例えば、サーバに、事前登録された生体情報を用意しておき、そのサーバに対し、生体情報入力手段により入力された生体情報を送信し、サーバにおいて両者を比較して認証してもよい。あるいは、サーバからの認証要求に基づいて、生体情報による認証を携帯情報端末１００で実行し、その実行結果として認証成功又は認証失敗を示すデータをサーバに返信してもよい。後者の場合は、生体情報をサーバに転送する必要がないため、生体情報をネットワーク上で盗まれる危険性を低減できよう。

【０１２１】（第３の実施形態）第３の実施形態は、上述の形態情報端末１００を、銀行のＡＴＭ端末のような個人認証を必要とする装置と通信することで、個人認証装置（ＰｅｒｓｏｎａｌＴｒｕｓｔｅｄ Ｄｅｖｉｃｅ）として機能させようとするものである。携帯情報端末１００のハードウェア構成は第２の実施形態とほぼ同様の構成を用いてもよいが、ソフトウェア構成については、携帯情報端末１００を個人認証装置として機能させるためのソフトウェアが追加されることになる。

【０１２２】一般的なＡＴＭ端末では、現金を引き出す際にキャッシュカードと暗証番号を使って認証していた。本実施形態では、このような認証方式に代えて、携帯情報端末１００を個人認証装置として利用し、本人確認を行う例について説明する。説明の都合上、図１３に合せて、ユーザは、「Ａ銀行」に口座を有し、その口座番号は「１２１－２２０８６５」であるものとする。また、その口座パスワード情報に関しては、通常の４桁の数字よりもデータ量の大きいデータが設定されているものとする。例えば、本実施形態では、２５６バイトの口座パスワード情報が設定されるものとして説明する。

【０１２３】本実施形態では、虹彩情報を用いた本人確認を行うことによって、この個人認証装置に記憶した個人の秘密情報をより安全に持ち運べる特徴がある。

【０１２４】図２０は、本実施形態における装置間の接続状況を説明する接続図である。携帯情報端末１００は、Ｂｌｕｅｔｏｏｔｈ網１５０を経由して、ＡＴＭ端末８００と通信を行う。そして、ＡＴＭ端末８００は、銀行専用回線網８５０を介して銀行ホスト機９００と接続し、従来同様に入出金などの取引トランザクションを処理する。また、銀行ホスト９００は、他銀行ホスト９１０、９２０と銀行間接続網９５０と相互接続しており、銀行間をまたがる振込処理などを実行する。

【０１２５】図２１は、本実施形態の大まかな動作を説明するためのフローチャートである。以下において通信手続きは、Ｂｌｕｅｔｏｏｔｈに準拠して実行されるものとする。ステップｔ１０において、本実施形態の携帯情報端末１００を持ったユーザがＡＴＭ端末８００に接近する。ステップｔ１１において、ＡＴＭ端末８００が、接近した携帯情報端末１００を検出し、顧客確認セッションを開始する。この際、チャレンジ情報を生成し、携帯情報端末１００に送信する。ステップｔ１２）携帯情報端末１００が、虹彩情報を用いた本人確認を行った上で、口座番号や口座パスワード情報およびチャレンジ情報などからレスポンス情報を生成し、ＡＴＭ端末８００に送信する。ステップｔ１３において、ＡＴＭ端末８００は、送付された内容（口座番号やレスポンス情報）の正当性を判断する。そして、正当な顧客であることが確認されると、顧客確認セッションからコマンド受付セッションに移行し、その旨を携帯情報端末１００に送信する。ステップｔ１４において、携帯情報端末１００は、ユーザの指示に応じて、適切なコマンドメッセージを生成し、ＡＴＭ端末８００に送信する。ステップｔ１５において、ＡＴＭ端末８００は、受け取ったコマンドを実行し、そのその実行結果を携帯情報端末１００に送信する。そして、コマンド受付セッションを終了する。ステップｔ１６において、携帯情報端末１００は、実行結果を受け取ると、それを表示し、ＡＴＭ端末８００とのセッションを終了する。

【０１２６】図２２は、本実施形態に係るＡＴＭ端末８００のブロック図である。ＣＰＵ８２１は、ＡＴＭ端末８００の制御部の中核をなす演算装置である。ＲＡＭ８２２は、各種の変数を記憶したり、制御プログラムのワークエリアとして機能したりする。ＲＯＭ８２３は、ＢＩＯＳなど最も基礎的な制御プログラムを格納しており、ＥＥＰＲＯＭなどで構成することができる。ＢｌｕｅｔｏｏｔｈＩＦ８３０は、携帯情報端末１００とＢｌｕｅｔｏｏｔｈ網１５０を介して通信するための通信インタフェースである。専用回線網ＩＦ８４０は、銀行専用回線網８５０を介して銀行ホスト９００と通信するための通信インタフェースである。ＨＤＤ８５０は、ＯＳやアプリケーションプログラムなどを記憶したハードディスクドライブである。ＨＤＤ制御回路８５１は、ＨＤＤドライブ８５０を制御するための制御回路である。ディスプレイ８１２は、ユーザにメニュー画面や取引内容を表示するための表示装置である。ディスプレイ制御回路８２４は、ディスプレイ８１２の表示処理を制御するための制御回路である。紙幣機構８６０は、紙幣の払い出し及び紙幣の預け入れなどを行うための機械的な機構である。紙幣機構制御回路８６１は、紙幣機構８６０を駆動し制御するための制御回路である。

【０１２７】図２３は、本実施形態におけるＡＴＭ端末８００が携帯情報端末１００の接近を検出した際の、ＡＴＭ端末８００のソフトウェアの処理手順を説明するフローチャートである。この処理を記述したプログラムは、携帯情報端末１００が接近したことをＢｌｕｅｔｏ

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ｏｔｈＩＦ８３０により検出されると、ＡＴＭ端末８００の主プログラムから呼び出され、携帯情報端末１００を介した銀行取引を実現するものである。いずれのプログラムもＨＤＤ８５０に格納されているものとする。

【０１２８】ステップＳ７００１で、ＣＰＵ８２１は、接近した携帯情報端末１００と安全な通信を行うため、ＢｌｕｅｔｏｏｔｈＩＦ８３０を介して顧客確認セッションを開始する。ここでは、携帯情報端末１００とＳＳＬ相当のネゴシエーションを行うことで、以降の通信内容を暗号化するものとする。さらに、ＣＰＵ８２１は、乱数列からなるチャレンジ情報を生成し、顧客確認セッション開始メッセージに埋め込む。そして、この顧客確認セッション開始メッセージを携帯情報端末１００に送信するようＢｌｕｅｔｏｏｔｈＩＦ８３０に指示する。ＢｌｕｅｔｏｏｔｈＩＦ８３０は、この指示に応じて、当該メッセージを携帯情報端末１００にＢｌｕｅｔｏｏｔｈ網８５０を介して送信する。

【０１２９】ステップＳ７００２で、ＣＰＵ８２１は、携帯情報端末１００からの通信を待ち合わせ、ＢｌｕｅｔｏｏｔｈＩＦ８３０を介してデータを受信する。

【０１３０】ステップＳ７００３で、ＣＰＵ８２１は、受信されたデータから、口座番号、レスポンス情報を取り出す。ステップＳ７００４で、ＣＰＵ８２１は、取り出された口座番号及びレスポンス情報の正当性を判断する。ここで、正当と判断された場合には、ステップＳ７００５に進み、正当でないと判断された場合には、ステップＳ７００９に進む。なお、正当性の確認には、口座番号について、チャレンジ情報とレスポンス情報とを使って、ＣＨＡＰ（Challenge Handshake Authentication Protocol：3ウエイ・ハンドシェークによる認証手続きと、ハッシュ関数で計算した認証データを使う利用者認証プロトコル）相当の認証を行えばよいであろう。すなわち、口座番号に対応する口座パスワード情報及びチャレンジ情報を専用線回線網ＩＦ８４０を介して、銀行ホスト機９００から取り寄せ、これらの情報を一方向性のハッシュ関数に入力し、その出力をレスポンス情報と比較する。これによりＣＰＵ８２１は、正当性を確認する。

【０１３１】ステップＳ７００５では、通信内容から正当な顧客であることが確認されているので、ＣＰＵ８２１は、顧客確認セッションからコマンド受付セッションに移行する。そして、ＣＰＵ８２１は、確認された口座の属性情報から取引可能なコマンドをリストアップし、コマンド受付メッセージを携帯情報端末１００に送信する。なお、属性情報とコマンドの対応関係は予めＨＤＤ８５０に格納されているものとする。ステップＳ７００６では、ＣＰＵ８２１は、再び携帯情報端末１００からの通信を待ち合わせ、ＢｌｕｅｔｏｏｔｈＩＦ８３０にデータを受信させる。

【０１３２】ステップＳ７００７で、ＣＰＵ８２１は、受信されたデータからコマンド情報を抽出し、抽出されたコマンドを実行する。例えば、コマンドが振込み処理の場合には、銀行ホスト機９００に、その旨の指示を専用回線網ＩＦ８４０から送信する。例えば、コマンドが預金の引き出し処理の場合には、銀行ホスト機９００に残高確認の上、指定額を紙幣機構制御回路８６１に用意するよう指示し、紙幣機構制御回路８６１は、紙幣機構８６０に指定額相当の紙幣を紙幣機構８６０に出金させる。

【０１３３】最後に、ステップＳ７００８で、ＣＰＵ８２１は、ＢｌｕｅｔｏｏｔｈＩＦ８３０を介して携帯情報端末１００にその実行結果を送信し、コマンド受付セッションを終了する。

【０１３４】ステップＳ７００９では、携帯情報端末１００からの通信内容が正当でないと判断された場合の処理を行う。典型的には、ＢｌｕｅｔｏｏｔｈＩＦ８３０を介して銀行の顧客サービス窓口への連絡先を通知し、顧客確認セッションを終了する。

【０１３５】なお、ＡＴＭ端末８００における、口座番号や口座パスワード情報による顧客確認には、実際には、銀行ホスト機９００との交信が必要になるが、本実施形態の説明では、携帯情報端末１００とのやり取りに必要な部分を詳細に説明した。例えば、ステップＳ７００４の正当性確認は、ＡＴＭ端末８００内では処理せずに、受け取った情報を銀行ホスト機９００に転送し、銀行ホスト機で正当性を判定し、その判定結果のみをＡＴＭ端末８００に通知することにより、より安全性を高めてもよい。

【０１３６】また、ＡＴＭ端末８００は、セッションの途中で携帯情報端末１００との通信が失われるなどの例外処理時には、実際、そのセッションを破棄して、次の携帯情報端末１００の検出を行うが、本実施形態では、そのような例外的な状況については説明を省略する。

【０１３７】図２４は、本実施形態における携帯情報端末１００が、ＡＴＭ端末８００との間で銀行取引を行う場合の、携帯情報端末１００のソフトウェアの処理手順を説明するフローチャートである。この処理を記述したプログラムは、ユーザからの指示に応じて図７のステップＳ１００５から呼び出されるものであり、携帯情報端末１００を介した銀行取引を実現する。

【０１３８】まず、ステップＳ８００１では、ＣＰＵ１２１は、ＡＴＭ端末８００に、携帯情報端末１００の接近を知らせるメッセージを送信すべく、通信制御回路１２６に指示する。通信制御回路１２６は、当該指示に従って、通信デバイス１３０から当該メッセージをＡＴＭ端末８００に送信する。ＣＰＵ１２１は、さらに、安全な通信を行うためＳＳＬ相当のネゴシエーションを実行し、以降の通信内容を暗号化する。

【０１３９】次に、ステップＳ８００２では、通信デバイス１３０は、ＡＴＭ端末８００からチャレンジ情報を

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含む顧客確認セッション開始メッセージを受信する。受信されたメッセージは、通信制御回路１２６を介してＣＰＵ１２１に転送される。ＣＰＵ１２１は、このメッセージからチャレンジ情報を抽出する。

【０１４０】ステップＳ８００３では、この開始メッセージに応じて、ＣＰＵ１２１は、虹彩情報を用いた本人確認を行う。虹彩情報を用いた本人確認の手順は、第2の実施形態で説明した通りである。本実施形態では、図２５に示す画面を表示ＬＣＤ１１２に表示させ、虹彩情報を用いた本人確認をユーザに促す。ここで、本人であることが確認された場合には、ステップＳ８００４に進み、確認されなかった場合には、本人確認ができなかった旨をＬＣＤ１１２に表示させた後、ステップＳ８０１０に進む。

【０１４１】ステップＳ８００４では、本人であることが確認されているので、ＣＰＵ１２１は、顧客確認のための手順を進める。ここでは、ＣＰＵ１２１は、ＲＯＭ１２３内に安全に保持されているユーザの口座番号、口座パスワード情報を読み出し、レスポンス情報を生成する。具体的には、ステップＳ７００４の一方向性のハッシュ関数と同一のハッシュ関数を用いて、口座パスワード情報とチャレンジ情報を加工し、レスポンス情報を求める。

【０１４２】ステップＳ８００５では、ＣＰＵ１２１は、通信デバイス１３０からユーザの口座番号及びレスポンス情報をＡＴＭ端末８００に送信させる。

【０１４３】ステップＳ８００６では、ＡＴＭ端末８００からの通信を待ち合わせ、通信デバイス１３０がデータを受信する。

【０１４４】ステップＳ８００７では、受け取ったデータが、コマンド受付メッセージであるか否かを判定する。ここで、受け取ったデータが、コマンド受付メッセージであるならば、ステップＳ８００８に進み、そうでなかった場合には、受け取ったメッセージをＬＣＤ１１２に表示させた後、ステップＳ８０１１に進む。

【０１４５】ステップＳ８００８で、ＣＰＵ１２１は、受け取ったコマンド受付メッセージの内容に則して、預金引き出しや振込みなどの取引可能なコマンドをコマンド受付画面にＬＣＤ１１２表示させ、ユーザの指示を待つ。コマンドの種類によっては、サブメニュを表示し、コマンドに必要なパラメータを入力又は選択する。図２６は、コマンド受付画面の一例を示す図である。

【０１４６】ステップＳ８００９では、ＣＰＵ１２１は、ユーザが指示するコマンドおよびパラメータから適切なコマンドメッセージを生成し、当該コマンドメッセージを通信デバイス１１２からＡＴＭ端末８００に送信する。

【０１４７】最後に、ステップＳ８０１０で、通信デバイス１１２はコマンドの実行結果をＡＴＭ端末８００から受信する。ＣＰＵ１２１は、実行結果を受け取ると、それをＬＣＤ１１２に表示させ、ＡＴＭ端末８００とのセッションを終了する。図２７は、実行結果の表示例を示す図である。

【０１４８】ステップＳ８０１１で、ＣＰＵ１２１は、セッション中の中間データなどセッション関連データをクリアした上で処理を終了する。

【０１４９】ここでは、一つの銀行との取引について説明しているが、複数の銀行と取引があるユーザの場合には、ＲＯＭ１２３に、各銀行の口座パスワード情報を記憶させておき、必要な際に虹彩情報などで本人認証を実行してもよい。これによって、各銀行ごとに口座パスワード情報が異なり、そのすべてをユーザが覚えておくことが難しいような状況でも、必要な銀行取引を簡便に行う事が可能となろう。なお、セッション中に一定期間入力がない場合に、安全のため、セッションを中止するようにしてもよい。

【０１５０】以上、本実施形態では、本提案の虹彩情報を用いた本人確認によって、携帯情報端末１００に記憶した個人の秘密情報を安全に持ち運ぶことができる。また、取引過程を本提案の携帯情報端末１００に表示することによって他者から覗き見される危険性を低減できる。これによって、より安全て簡便な認証手段を提供できる。

【０１５１】また、本実施形態では、虹彩情報を用いた本人確認を行うことで、携帯情報端末１００内に安全に保持している口座パスワード情報を利用する例について説明してきた。しかしながら、このようにパスワードのような鍵情報を携帯情報端末１００内に秘匿する代わりに、虹彩情報を直接鍵情報として利用してもよい。また、本実施形態では、携帯情報端末１００とＡＴＭ端末８００とは、Ｂｌｕｅｔｏｏｔｈ仕様に準拠した通信を行うことを前提として説明しているが、個人認証機能を安全に提供するという観点からは、Ｂｌｕｅｔｏｏｔｈ仕様よりも微弱な電波出力の通信を行い、電波の有効到達範囲を限定する事で、ワイヤレス通信における信号傍受の懸念を低減してもよい。

【０１５２】さらに、本実施形態では、本提案の携帯情報端末１００を応用した個人認証装置を銀行取引に適用する例について説明しているが、実社会において認証を必要とする他のシステムに、この個人認証装置を適用してもよい。例えば、電子政府や電子自治体などが提供するサービスにおける本人確認の一環として利用することも可能である。あるいは、第１の実施形態又は第２の実施形態において説明された図５のような接続環境下で、インターネット上のサービスを受ける場合にも、本実施形態を応用できる。典型的には、インターネット上での課金サービス、個人情報サービス及びインターネットバンキングサービスなどのように個人認証を必要とするネットワーク上のサーバプログラムを通信相手として、携帯情報端末１００を協調動作するようにしてもよい。

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【0153】（第4の実施形態）第3の実施形態は、携帯情報端末100に保持される口座パスワード情報の確認方法としてCHAP相当の方法を用いる例であった。第4の実施形態は、携帯情報端末100を個人認証装置として利用する点では第3の実施形態と同じであるが、携帯情報端末100に保持される口座パスワード情報の確認に電子署名を用いる点に特徴がある。より具体的には、RSA公開鍵暗号方式を用いる電子署名によって口座パスワード情報を確認する。すなわち、携帯情報端末100に保持する秘密鍵と対になる公開鍵を事前に銀行ホスト機900に登録しておく。ATM端末800により生成されたチャレンジ情報に、携帯情報端末100が秘密鍵を用いて署名する。銀行ホスト機900は、その秘密鍵と対になっている公開鍵を用いて署名情報の正当性を判断する。具体的には、第3の実施形態において説明した次の二つのステップを以下のように変更することで実施できる。

【0154】変更ポイントの一つ目は、ステップS7004である。これを以下に説明するステップS7104に置き換える。ステップS7104で、CPUS21は、取り出された口座番号及びレスポンス情報の正当性を判断する。ここで、正当と判断された場合には、ステップS7005に進み、正当でないと判断された場合には、ステップS7009に進む。なお、正当性の確認には、口座番号について、チャレンジ情報及びレスポンス情報を専用回線網IFから840から銀行ホスト機900に送信し、銀行ホスト機900に正当性を判断させる。銀行ホスト機900は、レスポンス情報から署名情報を取り出し、取り出された署名情報と、口座番号について事前に登録してあるRSA公開鍵暗号方式の公開鍵とを署名確認関数に代入し、署名情報の正当性を判断する。

【0155】変更ポイントの二つ目は、ステップS8004である。これを以下に説明するステップS8104に置き換える。ステップS8104では、本人であることが確認されているので、顧客確認のための手順を進める。ここでは、携帯情報端末100のROM123内に安全に保持しているユーザの口座番号及び口座パスワード情報を読み出し、CPU121がレスポンス情報を生成する。本実施形態における口座パスワード情報は、RSA公開鍵暗号方式の秘密鍵である。この秘密鍵と対になる公開鍵は、事前に銀行ホスト機900に安全に登録されている。レスポンス情報の具体的な生成方法は、ステップS7104の署名確認関数と対になる署名関数に、秘密鍵とチャレンジ情報とを適用して署名を行い、その署名情報をレスポンス情報とする。

【0156】以上の二点の変更によって、電子署名を用いて口座パスワード情報の確認を行うことが可能となり、一層安全な認証手段を簡便に提供する事を実現している。

【0157】さらに、銀行ホスト機900が、CA（Certification Authority）として保証する公開鍵証明書を、事前に携帯情報端末100に発行し、携帯情報端末100が署名情報と公開鍵証明書とをレスポンス情報に添付し、ATM端末800に送信することで、銀行ホスト機900に代わってATM端末800が署名情報の正当性確認を実行してもよい。

【0158】（他の実施形態）なお、前述した各実施形態の機能を実現するソフトウェアのプログラムコードを記憶した記憶媒体を、システムあるいは装置に供給し、そのシステムあるいは装置のコンピュータ（またはCPUやMPU）が記憶媒体に格納されたプログラムコードを読み出して実行することによっても、本発明が達成されることは言うまでもない。

【0159】この場合、記憶媒体から読み出されたプログラムコード自体が、前述の各実施形態の機能を実現することになり、そのプログラムコードを記憶した記憶媒体が本発明を構成することになる。

【0160】プログラムコードを供給するための記憶媒体として、例えば、フロッピィディスク、ハードディスク、光ディスク、光磁気ディスク、CD−ROM、CD−R、磁気テープ、不揮発性のメモリカード、ROM、あるいは、通信可能なネットワークに接続されたサーバコンピュータなどを用いることができる。

【0161】また、コンピュータが読み出したプログラムコードを実行することにより、前述した各実施形態の機能が実現されるだけでなく、そのプログラムコードの指示に基づき、コンピュータ上で稼働しているOSなどが実際の処理の一部または全部を行い、その処理によって前述した各実施形態の機能が実現される場合も、本発明に含まれることは言うまでもない。

【0162】さらに、記憶媒体から読み出されたプログラムコードが、コンピュータに挿入された機能拡張ボードやコンピュータに接続された機能拡張ユニットに備わるメモリに書き込まれた後、そのプログラムコードの指示に基づき、その機能拡張ボードや機能拡張ユニットに備わるCPUなどが実際の処理の一部または全部を行い、その処理によって前述した各実施形態の機能が実現される場合も、本発明に含まれることは言うまでもない。

【0163】

【発明の効果】以上詳述したように、本願発明によれば、キー入力操作を見ただけでは、入力された情報を第三者が実質的に認識できないような入力部を備えた携帯情報端末が提供される。

【0164】また、本願発明の他の観点によれば、銀行端末などの情報処理装置から暗証番号などを要求された場合に、内部に記憶された暗証番号を送信する携帯情報端末が提供される。

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【０１６５】また、本願発明の携帯情報端末によれば、小型でありながら、安全かつ簡単に個人認証を実現することが可能となる。

【図面の簡単な説明】

【図１】実施形態に係る携帯情報端末の外観図である。

【図２】携帯情報端末の内部構成を示す断面図である。

【図３】自由曲面プリズムの光路を示す図である。

【図４】携帯情報端末に実装される電気回路を示すブロック図である。

【図５】携帯情報端末とネットワークとの接続形態を示す図である。

【図６】ＨＴＴＰによる通信シーケンスの一例を示す図である。

【図７】携帯情報端末の動作の手順を示すフローチャートである。

【図８】携帯情報端末において実行されるＷｅｂアクセス処理の手順を示すフローチャートである。

【図９】図８に示すＷｅｂアクセス処理によって小型液晶ディスプレイに表示されたＷｅｂページ情報の一例を示す図である。

【図１０】携帯情報端末において実行される設定処理の手順を示すフローチャートである。

【図１１】小型液晶ディスプレイに表示された設定値の一例を示す図である。

【図１２】携帯情報端末において実行されるソフトウェアキーボード処理の手順を示すフローチャートである。

【図１３】事前登録された語句の例を示す図である。

【図１４】事前登録語句の入力キーを含んだソフトウェアキーボードが小型液晶ディスプレイに表示された画面の一例を示す図である。

【図１５】携帯情報端末において実行される認証手順を示すフローチャートである。

【図１６】事前登録語句の入力キーを除いたソフトウェアキーボードを示す図である。

【図１７】第２の実施形態における撮像光学系の構成を示す図である。

【図１８】携帯情報端末に実装される電気回路を示すブロック図である。

【図１９】携帯情報端末において実行される認証手順を示すフローチャートである。

【図２０】第３の実施形態における装置間の接続状況を説明する接続図である。

【図２１】ＡＴＭ端末と携帯情報端末間の信号シーケンスの一例を示す図である。

【図２２】ＡＴＭ端末８００の一構成例を示したブロック図である。

【図２３】ＡＴＭ端末８００の動作を説明するフローチャートである。

【図２４】携帯情報端末１００の銀行取引手順を説明するフローチャートである。

【図２５】携帯情報端末１００が本人確認をユーザに促す際の画面例を示す図である。

【図２６】携帯情報端末１００のコマンド受付の画面例を示す図である。

【図２７】携帯情報端末１００のコマンド実行結果表示の例を示す図である。

【符号の説明】

１００　携帯情報端末
１１０　拡大系表示デバイス（画面表示部）
１１１　自由曲面プリズム
１１２　小型液晶ディスプレイ
１１３　バックライト
１２０　小型コンピュータデバイス
１２１　ＣＰＵ（第１の表示手段、格納手段、第２の表示手段、表示入力手段）
１２２　ＲＡＭ（記憶部、表示入力手段）
１２３　ＲＯＭ
１２４　表示制御回路（第１の表示手段、第２の表示手段、表示入力手段）
１２５　バス
１２６　通信制御回路
１２７　入力制御回路
１２８　ＬＥＤ制御回路
１２９　電源制御回路
１３０　通信デバイス
１４０　入力デバイス（操作手段）
１５０　ＬＥＤデバイス
１６０　電源デバイス
１７１　結像光学系
１７２　撮像デバイス
１７３　赤外光源
１７５　撮像制御回路

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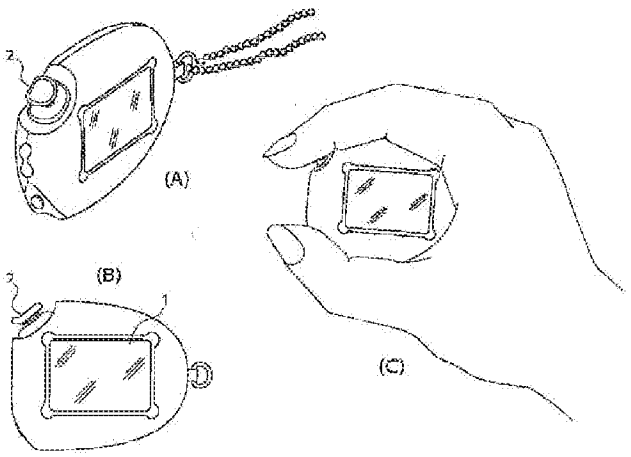
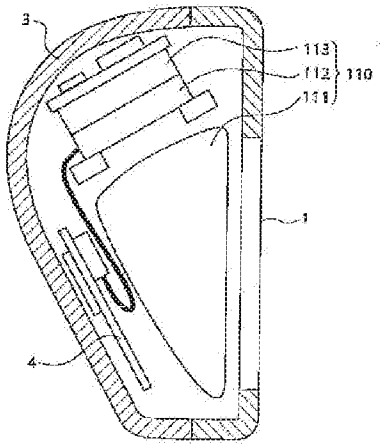
【図1】



【図2】



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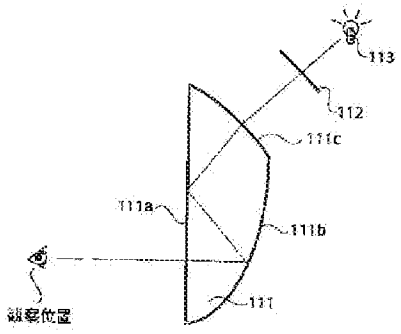

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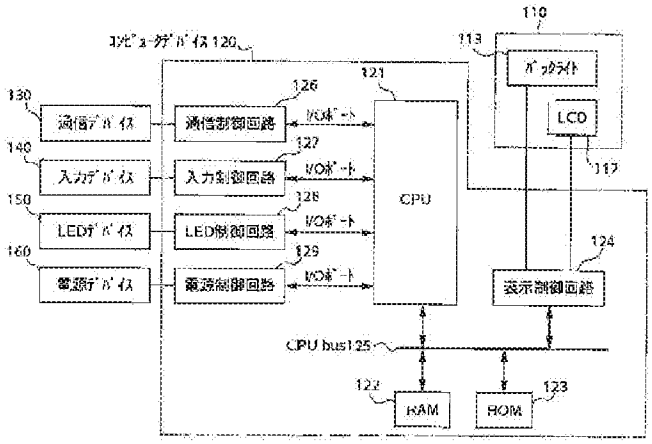

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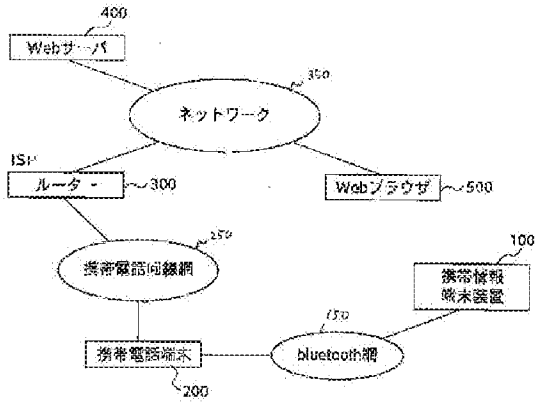

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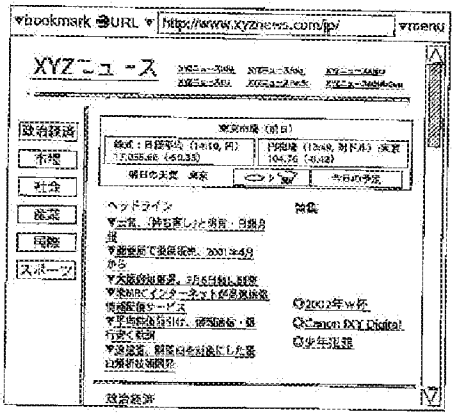

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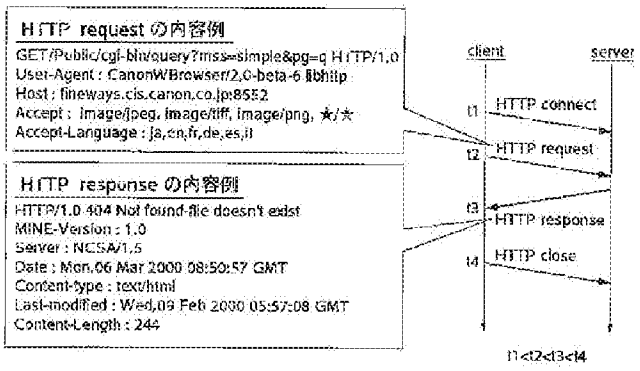

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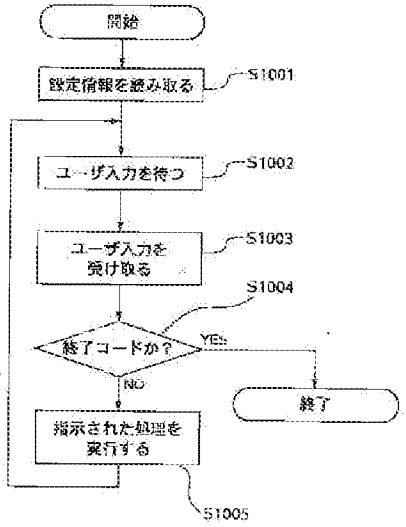

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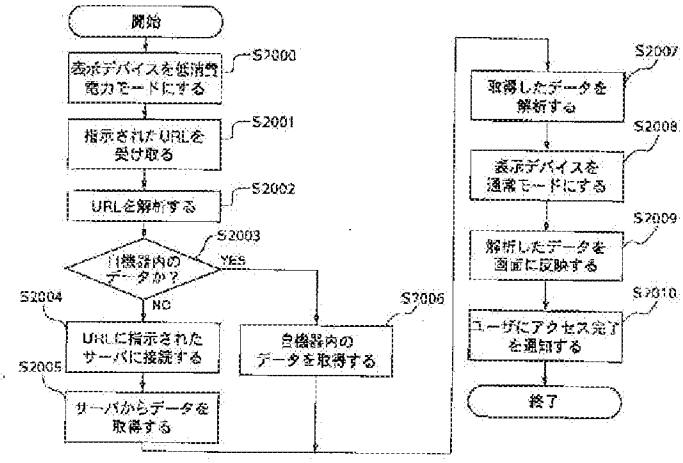

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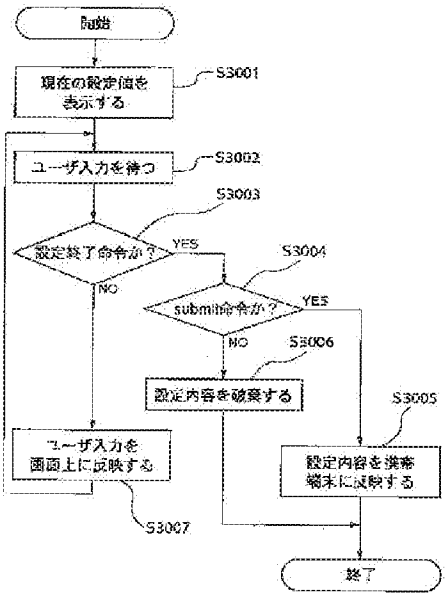

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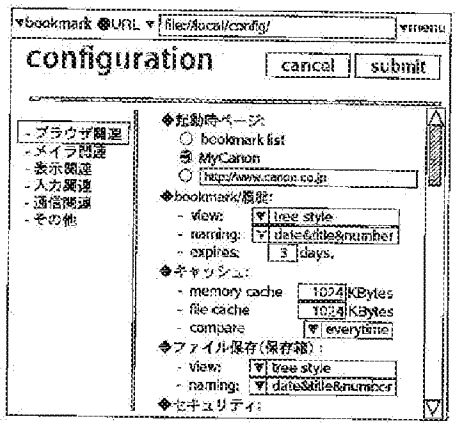

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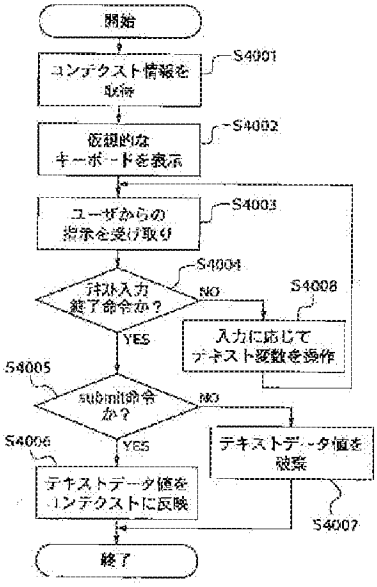

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[事前登録情報]

表示	内容	属性	セキュリティレベル
XYZニュース	http://www.xyz.com/japan	(URL)	1
会社名称	キヤノン株式会社	(名称)	1
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会社電話	(044)733-6111	(電話番号)	2
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氏名(ひらがな)	くろさわXXXX	(個人名)	4
氏名(カタカナ)	クロサワXXXX	(個人名)	4
氏名(roma)	KUROSAWA XXXX	(個人名)	4
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自宅FAX	(042)344-1243	(電話番号)	4
自宅電話	(042)344-2482	(電話番号)	4
ｱｶｳﾝﾄID (ISP1)	kjgs1223	(ID記号)	4
passwd(ISP1)	verserps	(パスワード)	4
mail(ISP1)	kjg61223@isp1.ne.jp	(ID記号)	3
口座番号(A銀行)	121-320865	(ID記号)	5
暗証番号(A銀行)	3971	(パスワード)	5
口座番号(B銀行)	03721-0110786	(ID記号)	5
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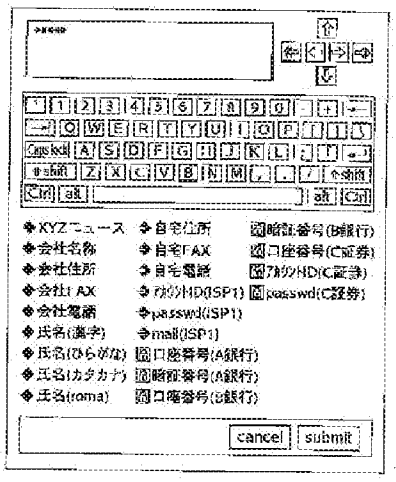

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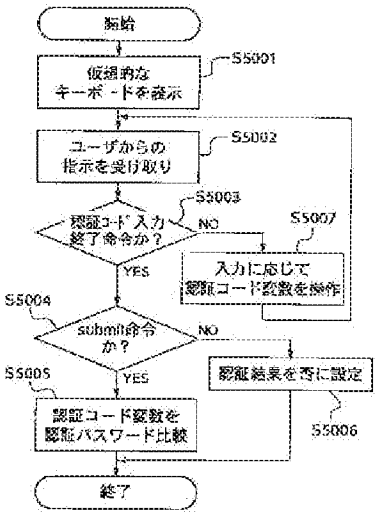

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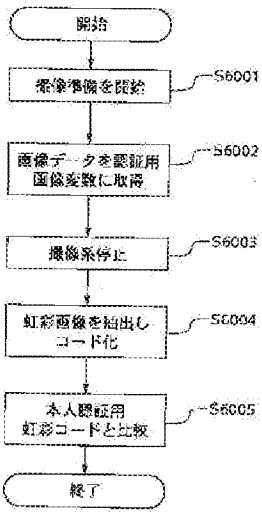

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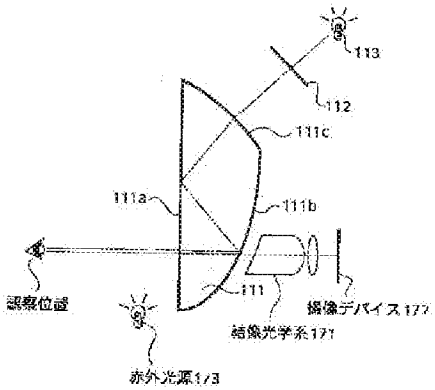

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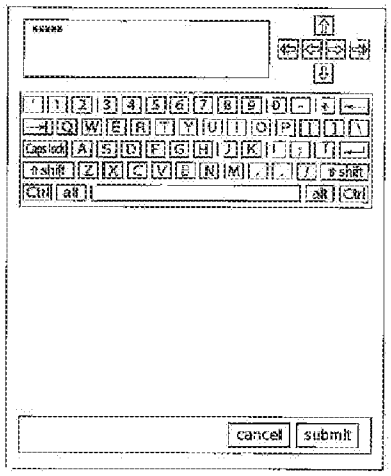

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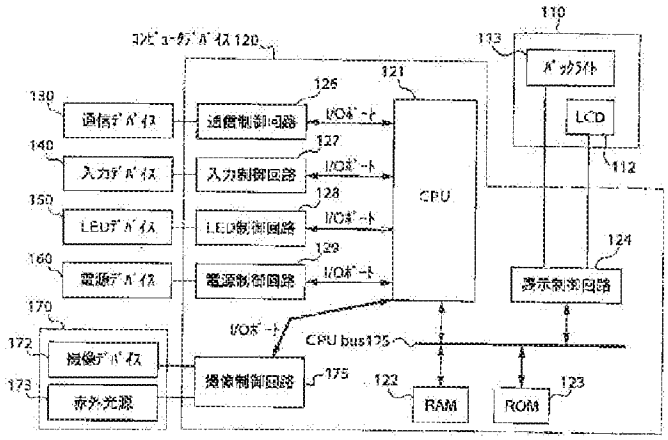

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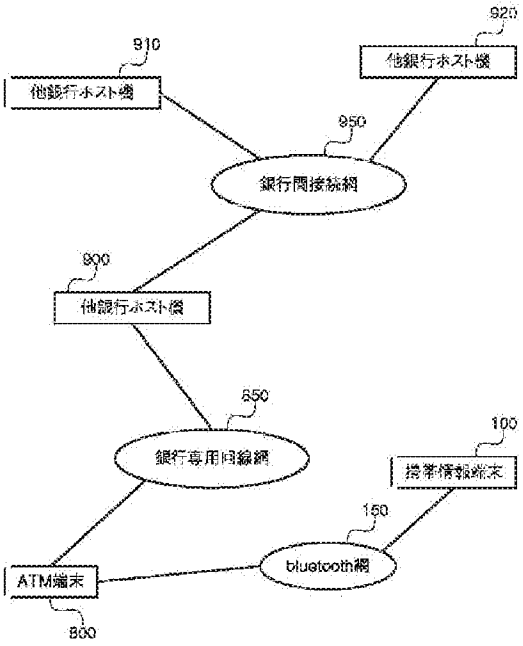

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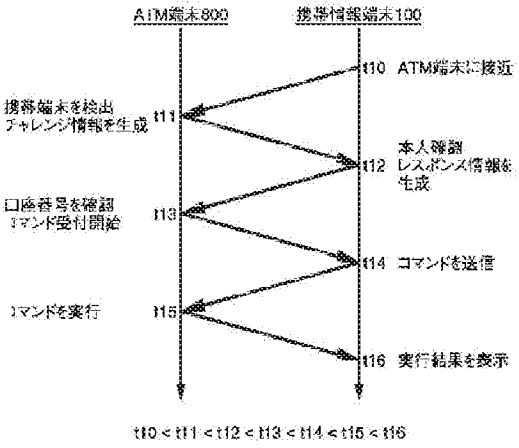

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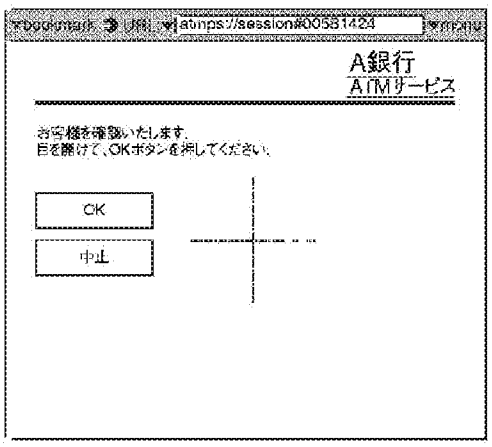

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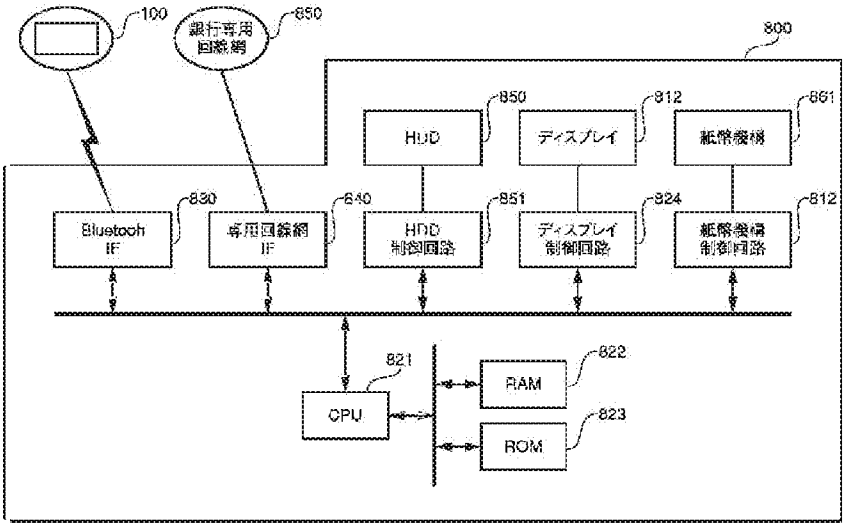

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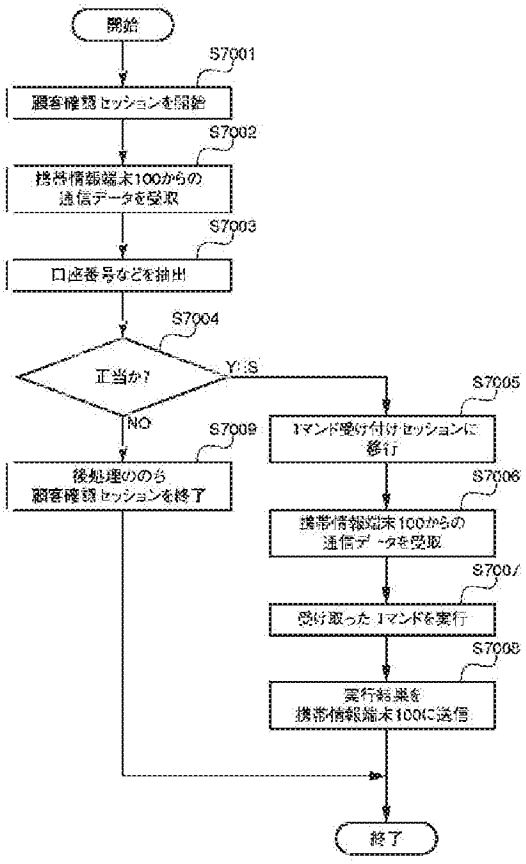

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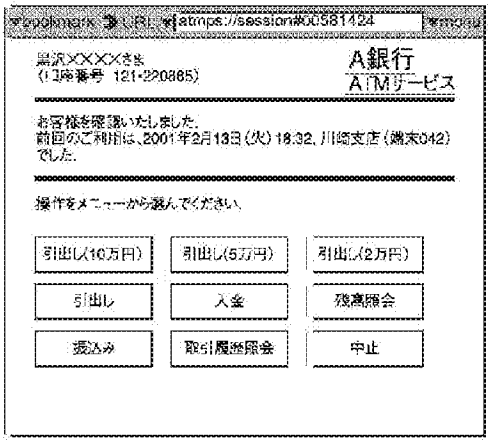

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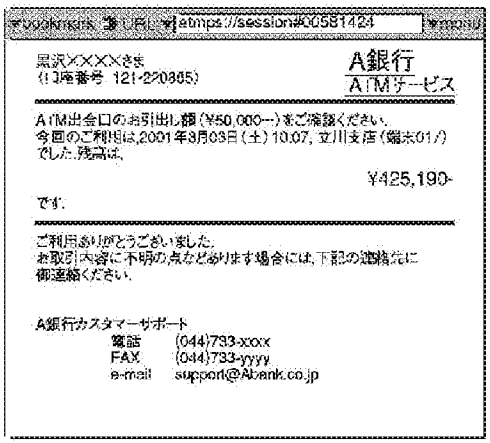

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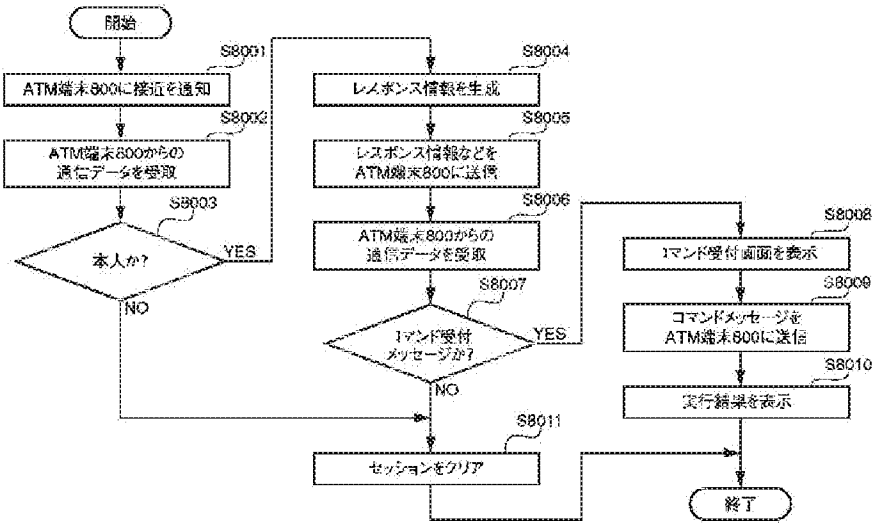

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(51)Int.Cl.[7]		識別記号	FI			(参考)
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					330F	
H04L	9/32		H04M	1/00	U	
H04M	1/00			1/274		
	1/274			1/725		
	1/725		H04B	7/26	109H	
H04Q	7/38		H04L	9/00	673D	

Fターム(参考) 5B019 BA10 DA06 DA08 DA10 EA10
GA10 HD20 HG30
5B085 AE03 AE25 BE01
5J104 AA07 AA16 EA03 KA01 KA02
KA16
5K027 AA11 BB09 FF01 FF22 HH23
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5K067 AA30 BB04 BB21 DD17 EE02
EE16 EE35 HH24 HH36

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DESCRIPTION JPH06244444

[0001]

The present invention relates to a light sensor, light such as the light-receiving device and the light excitation laser, such as a photoelectric conversion device - an optical confinement structure to be used in the light conversion device, and the like, and the light-receiving element using the same.

[0002]

2. Description of the Related Art light incident on the substrate, light using the same - light conversion, light - when performing the electrical conversion, and the like, effectively capture the light in the substrate, without missing the light to the outside of the substrate, by confining in the substrate, it is possible to increase the efficiency of each conversion as described above. To do this, the confinement of the light incident to the reflectance reduction and the substrate of the light at the substrate surface is important.

[0003]

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Conventionally, reduction of the reflectance of the incident light on the substrate surface, were performed using surface irregularities in the size of the anti-reflection film and a few tens of .mu.m. Also, Es IDC 89 Digest 270 pp (1989) (SID 89 DIGEST p270 (1989)) and as described in Japanese Patent Application No. 3-54371, reflection by the surface fine irregular with fine SiO2, MgF2 tablets it has been carried out using the anti-film.

[0004]

Method of using the conventional antireflection film |Problems to be solved by the invention is leak across the wavelength of the incident light is extensive, it is lowered sufficiently reflectance when the incident angle of light changes greatly there is a problem that can not be. Further, the method using several tens μm in size of the surface irregularities, since the light path is bent largely refracted when entering the substrate, as it is difficult to perform optical confinement on use the irregularities formed on the back surface there was a problem. In the case of using the antireflection film of fine surface irregularities with fine SiO2 grains or the like, because it does not consider the refractive index and the surface fine irregular shape of the substrate, it is difficult to very low reflectivity there is a problem that there is.

[0005]

The purpose of the present invention is to reduce the surface reflection is to provide a light receiving element using a light confinement structure and the same which can effectively perform the optical confinement.

[0006]

To achieve the above object SUMMARY OF THE INVENTION The optical confinement structure of the present invention, provided on the substrate and the substrate surface, made from a transition layer having an uneven light repeating width of the unevenness confinement configured to less main wavelength of light for performing.

[0007]

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The refractive index of the transition layer, the direction from the side of the substrate opposite to the substrate side, it is preferable to vary so as to approach the refractive index of the substrate. Such refractive index from the substrate outside, by continuously changing the direction of the substrate, a much lower reflectivity compared with the antireflection film by interference thin film formed by several layers, obtained over a wide range of wavelengths it can be.

[0008]

Further, the transition layer has a portion of the first material having arranged unevenness on the substrate side, the opposite of the irregularities corresponding thereto, the second material disposed on the side of the substrate opposite partial and more configuration, it is preferable that the refractive index of the first material as close to the same or refractive index of the substrate than the refractive index of the second material and the refractive index of the substrate. Portion of the first material include those formed using the substrate itself, for example, may be obtained by forming irregularities on the substrate surface, it may be those with a thing other materials on the substrate surface. Portion of the second material may be air, it may be a structure buried between the unevenness of the substrate surface in those of other materials.

[0009]

The shape of this unevenness, it is preferable that the area occupied on the plane portion of the second material is configured to decrease toward the substrate from the surface of the transition layer. Repeating the width of the unevenness, when the main light to perform optical confinement is visible light and preferably 1 μ m or less.

[0010]

Further, the light confinement structure of the present invention can be provided with a second concavo-convex pattern with a greater repetition width than the wavelength of the primary light to perform optical confinement on the back surface of the substrate. Furthermore, it is possible to provide a light reflecting layer on the back surface of the substrate.

[0011]

SAMSUNG EX. 1002 - 1774/2862

Further the light-receiving element of the present invention, using the above-described optical confinement structure, when the substrate and the first conductivity type, provided with a second conductivity type region of a first conductivity type opposite to the conductivity type substrate, desirably further It provided a first conductive type region of high concentration substrate, constituted by providing an electrode to be connected to these.

[0012]

A description will be given of the operation of the present invention by using the [action] Figure 1-6. FIG 1 (a), (b) is a partial perspective view and a sectional view of the vicinity of the substrate surface. If the light 4 from the external medium 1 to the substrate 3 is incident, repeatedly width 7 of the unevenness of the substrate surface is smaller than the wavelength of light, optical, the continuous refractive index of the transition layer 2 toward the surface of the substrate It acts as if it were changed to. That is, when the ratio between the second medium 5 of the first medium 6 as shown in FIG changes gradually toward the substrate, the refractive index with the refractive index with the second medium 5 of the first medium 6 , the refractive index of the film equivalent to the transition layer 2 that changes linearly are formed.

[0013]

State of a change in the transition layer of the refractive index is determined by mixed how the first medium and the second medium. The film consists of two kinds of media that the effective refractive index is represented by the average value of the respective medium. Figure 2 (a), (b), (c), (d), (e), (f), the first medium 6 respectively, rectangular, triangular groove, pyramid, hemisphere, sphere, reverse when having a shape such as pyramids, a refractive index of the second medium 5 1.0, and the refractive index of the first medium 6 to 3.5, the effective refractive index, such as shown in FIG. 3 It will have.

[0014]

Further, the refractive index 1.0 of the external medium 1 the shape of a pyramid and the sphere, the refractive index of the second medium 5 1.0, the refractive index of the first medium 6 3.5, the refractive index of the substrate 3 the calculated value of the reflectivity of the case of the 3.5

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shown in Figure 4. FIG. 4 (a), it shows the reflectance when the (b) is a pyramid shape, FIG. 4 (c), (d) a spherical linear scale and logarithmic scale, respectively the reflectance when the. Shows a slightly higher reflectance in the transition layer film thickness is 40nm in the pyramid shape, it shows the very low reflectance with a thick film thickness than this. The spherical, are also turned reflectance greater than 10% on average in any of the thickness, shows a slightly higher reflectivity compared to pyramidal shape.

[0015]

Figure 5 shows the relationship between the amount of light absorbed and the transition layer thickness on the pyramid shape. The refractive index 1.0 of the external medium 1, the refractive index of the first medium 6 3.5, the refractive index of the second medium 5 and the refractive index of the substrate 3 3.5 is 1.0, 1.5 If the results of calculation for. In either case, the thickness of the transition layer absorbs almost 100% in the large thickness than this amount of light absorbed is increased by several hundred nm before and after.

[0016]

Figure 6 shows the relationship between the amount of light absorbed and transition thickness of each shape. The refractive index 1.0 of the external medium 1, calculated for the case where the refractive index of the second medium 5 1.0, the refractive index of the first medium 6 3.5, the refractive index of the substrate 3 and 3.5 It shows the results. The light absorption amount in the film thickness tallest pyramid shape, until inverted pyramid indicates a respectively high absorption. However, not too light absorption amount is larger by increasing the thickness of the transition layer having a thickness in the rectangle and a spherical shape. As a result, the shape of the first medium, those with a shape like are upward in Figure 3 shows that the light absorption amount is large. In addition, in particular from that show a good result pyramid shape with a convex curve on the bottom of the upper right in Figure 3, the shape of the first medium 6 of this transition layer pyramid shape, pyramid, cone and convex downward as a shape obtained by rotating a line segment, larger shape than the proportion of decrease in the rate of decrease of the area of the substrate direction of the second medium 5 at the transition layer 2 near the surface in the transition layer 2 back surface near It was found to be preferable.

[0017]

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Specific substrate shape is described with reference to FIG. As shown in FIG. 7 (a), providing the transition layer 2 having a width 7 repeatedly on a substrate made of small irregularities. Accordingly, the refractive index of the transition layer 2 changes continuously from the refractive index of the outside air to the refractive index of the substrate 3 towards the bottom. Light 4 incident on the substrate 3 by the transition layer is incident on the substrate with almost no reflection at the substrate surface. Further, since the repeating width 7 is smaller than the wavelength of incident light, the incident light travels straight up to the back surface of the substrate at an angle that is incident without being reflected obliquely at the slope formed by the unevenness of the substrate surface.

[0018]

This substrate, periodic, such as in FIG. 7 (b), by forming an uneven 8 with large repeat width than the wavelength of the incident light, the light reflected by the back surface advances in the substrate at an angle, the substrate surface to reach. When the incident angle at this time is greater than the critical angle, the light goes again in the substrate is totally reflected. In this manner, the light once incident confined efficiently substrate 3. Further, by forming an irregular unevenness 9 with large repeat width than the wavelength of the incident light on the back surface as shown in FIG. 7 (c), the light is scattered and reflected by the back surface, reach the majority of the light is the substrate surface to have a critical angle of incidence larger than the angle when it is, is reflected back into the substrate, light incident is confined efficiently substrate 3. In these configurations, by forming a reflecting mirror on the back side, it is possible to reflect light more reliably backside.

[0019]

EXAMPLES An embodiment of the present invention will be described with reference to <Embodiment 1> FIG. In the present embodiment, on the surface of (100) plane silicon substrate 3, forming the transition layer, regular width, to form a pyramid 11 size. This pyramid, masks the backside, only the surface can be easily formed by processing with an alkaline etching solution. Further, the heated aqueous solution mainly containing Anmoniya or hydrazine is used as an etchant, machining the following micro pyramids. 11 1 .mu.m can be easily formed by performing.

[0020]

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The average size of the pyramids 11 of the thus obtained surface of the silicon substrate 3, as measured by SEM (scanning electron microscope) was about 0.3 .mu.m. The surface reflectance of the silicon substrate was measured, surface reflectance was significantly reduced in the wavelength range of 0.4~1.1 μm. Moreover, when provided with a coating by a thin oxide film on the silicon substrate 3 surface, the change in refractive index in the transition layer 2 becomes steep, further surface reflectance is lowered.

[0021]

Another embodiment of the present invention will be described with reference to <Embodiment 2> FIG. Cross section on the silicon substrate 3 was mainly triangular in this embodiment, to form a fine concavo-convex pattern 11 'of irregular size. Fine irregularities 11 'were formed by depositing films using CVD (chemical vapor deposition) method. The material of the film, was used a highly transparent and relatively refractive index of ITO, etc. ZnO2 material. The size of the fine irregularities 11 'deposition rate and temperature, could be about 0.5 μm on average by the gas pressure and the like. In addition, with a filler also serves as a surface protection (not shown) filled between the fine irregularities 11 '. This filler was formed a relatively small material having a refractive index such as SiO2 by a spin coating method or CVD method, or the like. Was significantly reduced in the wavelength range of the surface reflectance of the silicon substrate is also 0.4~1.1 μm.

[0022]

A further embodiment of the present invention will be described with reference to <Embodiment 3> FIG. In the present embodiment, the width repetition on the rear surface of the silicon substrate 3 as described in Example 2 was formed V-grooves 13 of 2 .mu.m. Accordingly, light incident from the surface is reflected by the back surface, is totally reflected again reach the surface, it is confined in the silicon substrate. V-groove 13 could be easily formed by using an etching mask using a normal photoresist. In this case, it may be a printing resist instead of the photoresist. Further, the back surface shape may be a shape such as an inverted pyramid or semi-circle as well V-groove only, the repetition width may be a larger size than the wavelength of the incident light. Further, to form a back reflecting mirror 14 in order to increase the reflectivity of the back.

[0023]

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A further embodiment of the present invention will be described with reference to <Embodiment 4> FIG. In the present embodiment, to form a pyramidal irregularities 15 on the back surface of the silicon substrate 3. A transparent glass as the material of the unevenness 15, adhered to the silicon substrate 3. As a result, it was able to easily form a light trapping structure without processing the silicon substrate 3. Further, as in Example 3, it was formed rear reflection mirror (not shown).

[0024]

An example of a light receiving element of the present invention will be described with reference to <Embodiment 5> FIG. In the same manner as in Example 3, on the p-type silicon substrate 21, cross section is mainly triangular, the minute irregularities 11 'irregular size, width repetition on the rear surface was formed a V-groove of 2 .mu.m (embodiment back reflector shown in example 3 is not formed). Next, provided a high-concentration p-type layer 19, heavily doped n-type layer 20 is formed by thermal diffusion method, the front and back surfaces in Passhibeshiyon oxide film of p-type silicon substrate 21 18 (oxide film on the surface is not shown) , and drilled holes in the oxide film 18 at a predetermined position, the electrodes 16 and 17 are formed by a vacuum deposition method to form a light-receiving element. The light-receiving element was improved photoelectric conversion efficiency than a conventional light-receiving element without the transition layer consisting of fine irregularities 11 '.

[0025]

Incidentally, the minute unevenness of shape other than the above, namely, the triangular groove, spheres, hemispheres, inverted pyramid, with a p-type silicon substrate with a transition layer having a rectangular, has formed the same way the light-receiving element, both of the conventional It was improved photoelectric conversion efficiency than the light receiving element.

[0026]

It was used silicon as the substrate in the above example, in addition to the silicon, Gariumuhiso. in FILL UP phosphorus-free, CuInS, single crystals of CdS, etc., polycrystalline, single atom of

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amorphous, and semiconductor multi-component, etc., glass , such as those of an insulating plastic or the like, what it may be of a material of course. Further, surface irregularities, the structure of the back surface irregularities may be any combination of the structures described above, the cross-sectional shape of the concave-convex is also the shape and described in FIG. 2, or regular, irregular no analogous thereto it is needless to say may be in the form.

[0027]

By using the structure of the present invention, an optical sensor, a light such as the light-receiving device and the light excitation laser, such as a powered conversion device - when it is necessary to confine to enable the light in the optical conversion devices and the like, effectively light confinement was able to perform. Further, the light receiving element of the present invention using such an optical confinement structure, could improve the photoelectric conversion efficiency.

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(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平6－244444

(43)公開日　平成６年(1994)９月２日

(51)Int.Cl.[5]	識別記号	庁内整理番号	Ｆ Ｉ	技術表示箇所
Ｈ０１Ｌ　31/04				
Ｇ０２Ｂ　5/00	Ｚ	9224－2Ｋ		
Ｈ０１Ｌ　31/10				
		7376－4Ｍ	Ｈ０１Ｌ　31/ 04	Ｆ
		8422－4Ｍ	31/ 10	Ｚ

審査請求　未請求　請求項の数10　ＯＬ　（全　７　頁）

(21)出願番号　特願平5－29092

(22)出願日　平成５年(1993)２月18日

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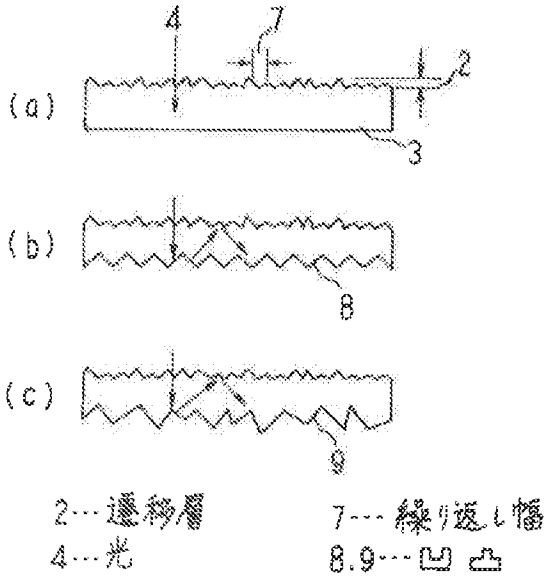
(54)【発明の名称】　光閉込め構造及びそれを用いた受光素子

(57)【要約】
【目的】表面反射を低減し、光閉じ込めを有効に行なうことができる光閉込め構造を提供すること。
【構成】基板３の表面に、凹凸を有する遷移層２を設け、この凹凸の繰り返し幅７を光閉じ込めを行なう主な光４の波長以下とする。基板３の裏面に凹凸８、９を設けることが好ましい。遷移層２の屈折率は、基板側と逆の側から基板側に向かって、基板の屈折率に近づくように変化させる。

図７



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【特許請求の範囲】
【請求項１】基板及び該基板表面に設けられた、凹凸を有する遷移層からなり、該凹凸の繰り返し幅は、光閉じ込めを行なう主な光の波長以下であることを特徴とする光閉込め構造。
【請求項２】請求項１記載の光閉込め構造において、上記遷移層の屈折率は、基板側と逆の側から基板側に向かって、基板の屈折率に近づくように変化することを特徴とする光閉込め構造。
【請求項３】請求項１記載の光閉込め構造において、上記遷移層は、基板側に配置された凹凸を有する第１の材質の部分と、これに対応する逆向きの凹凸を有し、基板と逆の側に配置された第２の材質の部分とよりなり、該第１の材質の屈折率は、基板の屈折率と同じか又は該第２の材質の屈折率よりも基板の屈折率に近いことを特徴とする光閉込め構造。
【請求項４】請求項３記載の光閉込め構造において、上記凹凸の形状を、上記第２の材質の部分の平面上に占める面積が上記遷移層の表面から基板の方向に向かって減少するように構成することを特徴とする光閉込め構造。
【請求項５】請求項４記載の光閉込め構造において、上記凹凸の形状を、上記第２の材質の部分の平面上に占める面積の上記遷移層の表面から基板の方向に向かって減少する割合が遷移層の裏面付近より表面付近で大きいように構成することを特徴とする光閉込め構造。
【請求項６】請求項１記載の光閉込め構造において、上記凹凸は、その断面形状が実質的に三角であることを特徴とする光閉込め構造。
【請求項７】請求項１から６のいずれか一に記載の光閉込め構造において、上記光閉じ込めを行なう主な光は、可視光であり、上記凹凸の繰り返し幅は、１μｍ以下であることを特徴とする光閉込め構造。
【請求項８】請求項１から７のいずれか一に記載の光閉込め構造において、上記基板は、その裏面に光閉じ込めを行なう主な光の波長より大きな繰返し幅を持つ第２の凹凸を有することを特徴とする光閉込め構造。
【請求項９】請求項１から８のいずれか一に記載の光閉込め構造において、上記基板は、その裏面に光反射層を有することを特徴とする光閉込め構造。
【請求項１０】請求項１から７のいずれか一に記載の光閉込め構造を用いた受光素子であって、上記基板は第１導電型であり、上記基板に設けられた第２導電型領域及びこれと接続する電極を有することを特徴とする受光素子。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、光センサー、光電変換装置等の受光装置や光励起レーザー等の光－光変換装置等に用いる光閉込め構造及びそれを用いた受光素子に関する。

【０００２】
【従来の技術】光を基板に入射し、これを用いて光－光変換、光－電気変換等を行なう場合、基板内に光を効率的に取り込み、この光を基板外に逃すことなく、基板内に閉じ込めることにより、上記の各変換の効率を高くすることができる。これを行なうためには、基板表面での光の反射率の低減及び基板内に入射した光の閉じ込めが重要である。
【０００３】従来、基板表面での入射光の反射率の低減は、反射防止膜や数十μｍの大きさの表面凹凸等を用いて行なわれていた。また、エス　アイ　ディー　８９　ダイジェスト　２７０頁（１９８９）（ＳＩＤ　８９　ＤＩＧＥＳＴ　ｐ２７０（１９８９））や特願平３－５４３７１に述べられているように、微細なＳｉＯ₂、ＭｇＦ₂粒を用いた表面微細凹凸による反射防止膜を用いることが行なわれていた。
【０００４】
【発明が解決しようとする課題】上記従来の反射防止膜を用いる方法は、入射光の波長が広範囲に及んだり、光の入射角が大きく変化する場合には充分に反射率を下げることが出来ないという問題があった。また、数十μｍの大きさの表面凹凸を用いる方法は、光が基板に入射したときに屈折で光路が大きく曲げられるため、裏面に形成された凹凸を用て光閉じ込めを行なうことは難しいという問題があった。また、微細なＳｉＯ₂粒等を用いた表面微細凹凸による反射防止膜を用いた場合は、基板の屈折率や表面微細凹凸形状について考慮していないため、反射率を非常に低くすることは困難であるという問題があった。
【０００５】本発明の目的は、表面反射を低減し、光閉じ込めを有効に行なうことができる光閉込め構造及びそれを用いた受光素子を提供することにある。
【０００６】
【課題を解決するための手段】上記目的を達成するために、本発明の光閉込め構造は、基板及び基板表面に設けられた、凹凸を有する遷移層からなり、この凹凸の繰り返し幅を光閉じ込めを行なう主な光の波長以下とするように構成する。
【０００７】この遷移層の屈折率は、基板側と逆の側から基板側に向かって、基板の屈折率に近づくように変化することが好ましい。このように屈折率が基板外部から、基板方向に連続的に変化することにより、数層で形成された干渉膜による反射防止膜に比べはるかに低い反射率を、波長の広い範囲に渡って得ることが出来る。
【０００８】また、この遷移層は、基板側に配置された凹凸を有する第１の材質の部分と、これに対応する逆向きの凹凸を有し、基板と逆の側に配置された第２の材質の部分とより構成し、第１の材質の屈折率を基板の屈折率と同じか又は第２の材質の屈折率よりも基板の屈折率に近くすることが好ましい。第１の材質の部分は、基板

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そのものを用いて形成されたもの、例えば、基板表面に凹凸を形成したものでもよく、基板表面に他の材質のものを付けたものでもよい。第２の材質の部分は、空気であってもよく、他の材質のもので基板表面の凹凸の間を埋めた構造であってもよい。

【０００９】この凹凸の形状は、第２の材質の部分の平面上に占める面積が遷移層の表面から基板の方向に向かって減少するように構成することが好ましい。凹凸の繰り返し幅は、光閉じ込めを行なう主な光が可視光であるとき、１μｍ以下とすることが好ましい。

【００１０】また、本発明の光閉込め構造は、基板の裏面に光閉じ込めを行なう主な光の波長より大きな繰返し幅を持つ第２の凹凸を設けることが出来る。さらに、基板の裏面に光反射層を設けることが出来る。

【００１１】さらに本発明の受光素子は、上記の光閉込め構造を用い、基板を第１導電型とするとき、第１導電型と逆の導電型の第２導電型領域を基板に設け、望ましくはさらに高濃度の第１導電型領域を基板に設け、これらと接続する電極を設けて構成される。

【００１２】

【作用】図１～６を用いて本発明の作用を説明する。図１（ａ）、（ｂ）は、基板表面近傍の部分斜視図及びその断面図である。基板３に外部媒質１から光４が入射する場合、基板表面の凹凸の繰り返し幅７が光の波長より小さいと、光学的には、遷移層２の屈折率が表面から基板に向って連続的に変化した場合と同様に作用する。つまり、図のように第２の媒質５と第１の媒質６の割合が基板に向って次第に変化する場合に、第２の媒質５の持つ屈折率から第１の媒質６の持つ屈折率に、屈折率が面積的に変化する膜と等価な遷移層２が形成される。

【００１３】屈折率の遷移層内での変化の様子は、第１の媒質と第２の媒質の混ざり方で決定される。２種類の媒質で構成される膜ではその実効的な屈折率は各々の媒質の平均値で表される。図２（ａ）、（ｂ）、（ｃ）、（ｄ）、（ｅ）、（ｆ）に示すように、それぞれ第１の媒質６が、矩形、三角溝、ピラミッド、半球、球、逆ピラミット等の形状を持つ場合には、第２の媒質５の屈折率を１．０、第１の媒質６の屈折率を３．５とすると、図３に示す様な実効的な屈折率を持つことになる。

【００１４】また、ピラミッドと球の形状について外部媒質１の屈折率１．０、第２の媒質５の屈折率を１．０、第１の媒質６の屈折率を３．５、基板３の屈折率を３．５とした場合の反射率の計算値を図４に示す。図４（ａ）、（ｂ）はピラミット形状のときの反射率を、図４（ｃ）、（ｄ）は球形状のときの反射率をそれぞれリニアースケールとログスケールで示したものである。ピラミッド形状では遷移層膜厚が４０ｎｍではやや高い反射率を示すが、これより厚い膜厚では非常に低い反射率を示している。球形では、いずれの膜厚においても平均で１０％を越える反射率になっており、ピラミッド形状に比べると若干高い反射率を示している。

【００１５】図５に、ピラミッド形状での吸収光量と遷移層膜厚との関係を示す。外部媒質１の屈折率１．０、第１の媒質６の屈折率を３．５、基板３の屈折率を３．５とし第２の媒質５の屈折率が１．０、１．５の場合について計算した結果を示す。いずれの場合も、遷移層の膜厚が数百ｎｍ前後で吸収光量が大きくなりこれより厚い膜厚ではほぼ１００％吸収する。

【００１６】図６に、各形状での吸収光量と遷移膜厚との関係を示す。外部媒質１の屈折率１．０、第２の媒質５の屈折率を１．０、第１の媒質６の屈折率を３．５、基板３の屈折率を３．５とした場合について計算した結果を示す。各膜厚での光吸収量はピラミッド形状で一番高く、逆ピラミッドまではそれぞれ高い吸収量を示している。しかし、矩形と球形では遷移層膜厚を厚くしてもあまり光吸収量は大きくならない。この結果は、第１の媒質の形状が、図３で右上がりである様な形状をしているものが光吸収量が大きい事を示している。また、特に図３で右上がりで下に凸の曲線を持つピラミッド形状がよい結果を示す事から、本遷移層の第１の媒質６の形状はピラミッド形状、多角錐、円錐や下に凸の部分を回転して得られる形状の様に、遷移層２表面付近での第２の媒質５の基板方向への面積の減少の割合が遷移層２裏面付近でのその減少の割合より大きい形状が好ましいことが分かった。

【００１７】具体的な基板形状を、図７を用いて説明する。図７（ａ）に示すように、基板上に繰り返し幅７が小さい凹凸から成る遷移層２を設ける。これにより、遷移層２の屈折率は上から下に向って外気の屈折率から基板３の屈折率まで連続的に変化する。この遷移層により基板３に入射する光４は、基板表面でほとんど反射することなく基板内へ入射する。また、繰り返し幅７が入射光の波長より小さいため、入射した光は基板表面の凹凸により形成される斜面で斜めに反射されることなく入射した角度で基板裏面まで直進する。

【００１８】この基板に、図７（ｂ）のような周期的で、入射光の波長より大きい繰り返し幅を持つ凹凸８を形成することにより、裏面で反射された光が斜めに基板内を進み、基板表面へ達する。このときの入射角度が臨界角より大きい場合、光は全反射されて再び基板内を進む。このようにして、一度入射した光は基板３に効率よく閉じ込められる。また、図７（ｃ）のように裏面に入射光の波長より大きい繰り返し幅を持つ不規則な凹凸９を形成することにより、裏面で光が散乱反射され、大部分の光が基板表面に達したときに臨界角より大きい入射角を持つため、基板内へ再び反射されて、入射した光が基板３に効率よく閉じ込められる。これらの構成では、裏面に反射鏡を形成することで、より確実に裏面で光を反射することができる。

【００１９】

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【実施例】〈実施例１〉図８を用いて本発明の一実施例を説明する。本実施例では、表面が（１００）面シリコン基板３の上に、遷移層を構成する、規則的な幅、大きさのピラミッド１１を形成した。このピラミッドは、裏面をマスクして、表面だけをアルカリ性のエッチング液で加工することにより容易に形成することができる。また、アンモニヤやヒドラジンを主成分とする加熱した水溶液をエッチング液として用いて、加工を行なうことにより１μｍ以下の微小なピラミッド１１を容易に形成することが出来る。

【００２０】このようにして得られたシリコン基板３の表面のピラミッド１１の平均のサイズは、ＳＢＭ（走査型電子顕微鏡）による測定では約０．３μｍであった。このシリコン基板の表面反射率を測定したところ、０．４～１．１μｍの波長範囲で表面反射率が著しく低下した。また、シリコン基板３表面に薄い酸化膜による皮膜を設けたところ、遷移層２内の屈折率の変化が急峻になり、さらに表面反射率が低下した。

【００２１】〈実施例２〉図９を用いて本発明の他の実施例を説明する。本実施例ではシリコン基板３の上に断面が主に三角形をした、不規則な大きさの微小凹凸１１’を形成した。微小凹凸１１’はＣＶＤ（化学気相成長）法を用いた堆積膜により形成した。膜の材質は、ＩＴＯ、ＺｎＯ₂等の透明で比較的屈折率の高い材料を用いた。微小凹凸１１’のサイズは堆積速度や温度、ガス圧等により平均で約０．５μｍにすることが出来た。また、表面保護を兼ねて充填材（図示せず）で微小凹凸１１’の凹を埋めた。この充填材にはＳｉＯ₂等の屈折率の比較的小さい材料をスピン塗布法やＣＶＤ法等で形成した。このシリコン基板の表面反射率も０．４～１．１μｍの波長範囲で著しく低下した。

【００２２】〈実施例３〉図１０を用いて本発明のさらに他の実施例を説明する。本実施例では、実施例２で述べたシリコン基板３の裏面に繰り返し幅が２μｍのＶ溝１３を形成した。これにより、表面から入射した光は、裏面で反射され、再び表面に達すると全反射され、シリコン基板内に閉じ込められる。Ｖ溝１３は通常のホトレジストを用いたエッチングマスクを用いて容易に形成することが出来た。この場合、ホトレジストでなく印刷レジストでもよい。また、裏面形状はＶ溝のみならず逆ピラミッドや半円等の形状でもよく、その繰り返し幅が入射光の波長より大きいサイズであればよい。また、裏面での反射率を高めるために裏面反射鏡１４を形成した。

【００２３】〈実施例４〉図１１を用いて本発明のさらに他の実施例を説明する。本実施例では、シリコン基板３の裏面にピラミット状の凹凸１５を形成した。この凹凸１５の材質には透明なガラスを用い、シリコン基板３に接着した。これにより、シリコン基板３を加工することなく容易に光トラップ構造を形成する事が出来た。また、実施例３と同じように、裏面反射鏡（図示せず）を

形成した。

【００２４】〈実施例５〉図１２を用いて本発明の受光素子の一実施例を説明する。実施例３と同様に、ｐ型シリコン基板２１の上に、断面が主に三角形をした、不規則な大きさの微小凹凸１１’を、裏面に繰り返し幅が２μｍのＶ溝を形成した（実施例３に示した裏面反射鏡は形成しない）。次に、高濃度ｐ型層１９、高濃度ｎ型層２０を熱拡散法で形成し、ｐ型シリコン基板２１の表面及び裏面にパッシベーション酸化膜１８（表面の酸化膜は図示せず）を設け、所定の位置の酸化膜１８に穴開けして、電極１６、１７を真空蒸着法により形成し、受光素子を形成した。この受光素子は、微小凹凸１１’からなる遷移層を設けない従来の受光素子よりも光電変換効率が向上した。

【００２５】なお、上記以外の形状の微小凹凸、すなわち、三角錐、球、半球、逆ピラミッド、粉形を有する遷移層を持つｐ型シリコン基板を用いて、同様に受光素子を形成したが、いずれも従来の受光素子よりも光電変換効率が向上した。

【００２６】以上の実施例で基板としてシリコンを用いたが、シリコンの他に、ガリウムヒソ、インジュウムリン、ＣｕＩｎＳ、ＣｄＳ等の単結晶、多結晶、非晶質の単原子、多元系等の半導体や、ガラス、プラスチック等の絶縁性のもの等、どのような材質のものであってもよいことは言うまでもない。また、表面凹凸、裏面凹凸の構造は上記で説明した構造のいずれかの組み合わせであってもよく、凹凸の断面形状も、図２で説明した形状や、それに類似した規則的、不規則ないかなる形状であってもよいことは言うまでもない。

【００２７】

【発明の効果】本発明の構造を用いることにより、光センサー、受電変換装置等の受光装置や光励起レーザー等の光ー光変換装置等において光を有効に閉じ込める必要がある場合に、有効に光閉じ込めを行なうことが出来た。また、このような光閉込め構造を用いた本発明の受光素子は、光電変換効率を向上させることが出来た。

【図面の簡単な説明】

【図１】本発明の原理を説明する概念図。

【図２】本発明の原理を説明する概念図。

【図３】本発明の効果を説明する計算結果の一例を示す図。

【図４】本発明の効果を説明する計算結果の一例を示す図。

【図５】本発明の効果を説明する計算結果の一例を示す図。

【図６】本発明の効果を説明する計算結果の一例を示す図。

【図７】本発明の原理を説明する概念図。

【図８】本発明の光閉込め構造の一実施例の断面模式図。

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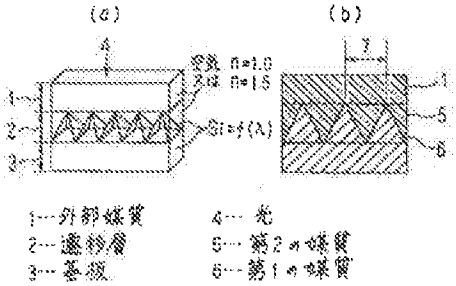
【図９】本発明の光閉込め構造の他の実施例の断面模式図及び斜視図。
【図１０】本発明の光閉込め構造の一実施例の斜視図。
【図１１】本発明の光閉込め構造の一実施例の斜視図。
【図１２】本発明の受光素子の一実施例の斜視図。
【符号の説明】
１…外部媒質
２…遷移層
３…基板
４…光
５…第２の媒質
６…第１の媒質
７…繰り返し幅
８、９、１５…凹凸
１１…ピラミッド
１１’…微小凹凸
１３…Ｖ溝
１４…裏面反射膜
１６、１７…電極
１８…酸化膜
１９…高濃度ｐ型層
２０…高濃度ｎ型層
２１…ｐ型シリコン基板

【図１】

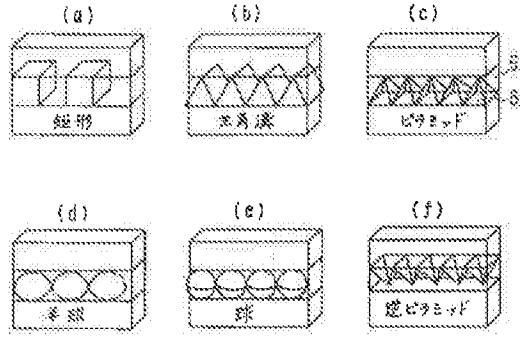
図１



1…外部媒質　　4…光
2…遷移層　　5…第２の媒質
3…基板　　6…第１の媒質

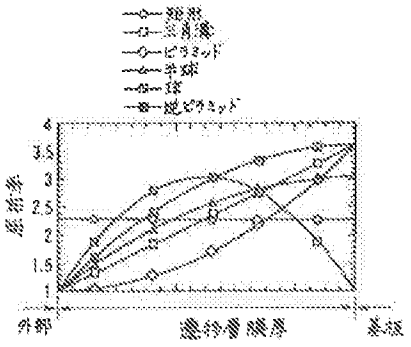
【図２】

図２



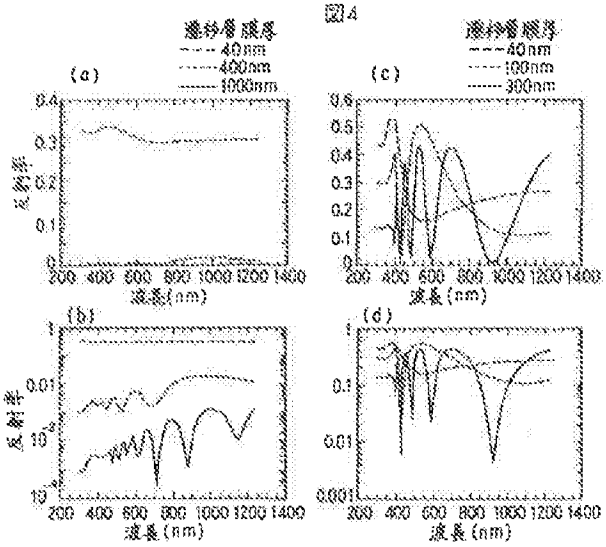
【図３】

図３



【図４】

図４



【図８】

図８

3…基板
11…ピラミッド

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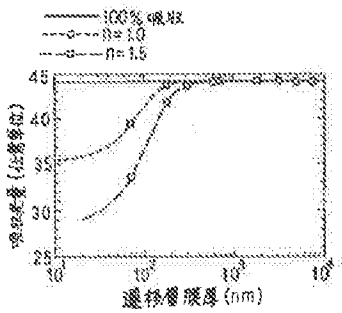
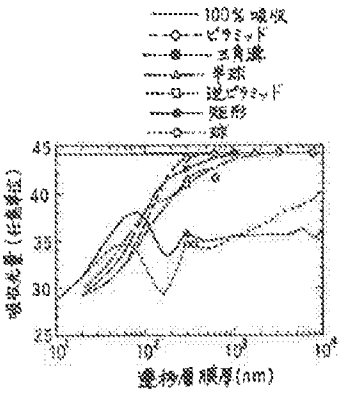
【図5】

図5



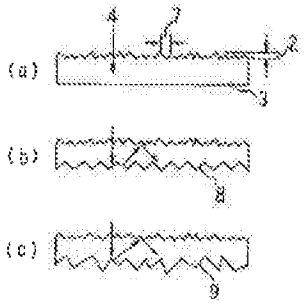
【図6】

図6



【図7】

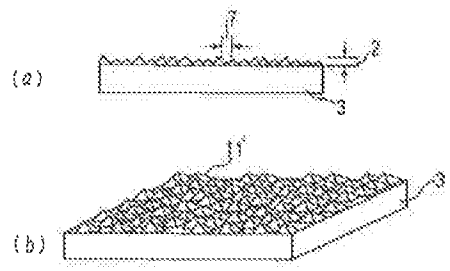
図7



2…遷移層　　7…繰り返し幅
4…光　　8,9…凹凸

【図9】

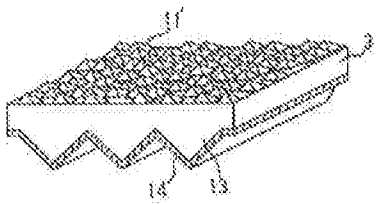
図9



11'…微小凹凸

【図10】

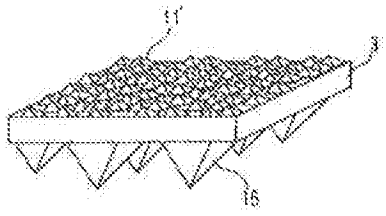
図10



11'…微小凹凸
13…V溝
14…裏面反射鏡

【図11】

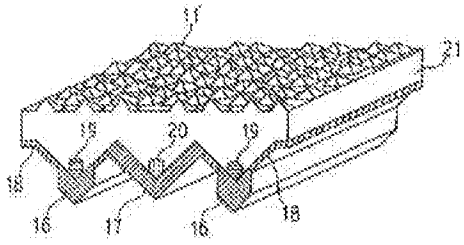
図11



11'…微小凹凸
15…凹凸

【図12】

図12



11'…微小凹凸　　19…高濃度p型層
16,17…電極　　20…高濃度n型層
18…酸化膜　　21…p型シリコン基板

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フロントページの続き

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Martin U. Pralle	Confirmation No.: 5052
Application No.: 15/216,244	Art Unit: 2814
Filed: July 21, 2016	Examiner: Pham, Long
For: PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS	

VIA EFS-WEB
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November 11, 2016 (Dated)
Electronic Signature: /Andrew W. Schultz/
Andrew W. Schultz, Reg. No. 66,869

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Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached substitute for PTO/SB/1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed before the mailing date of a first Office Action on the merits as far as is known to the undersigned (37 CFR 1.97(b)(3)).

In accordance with 37 CFR 1.98(a)(2)(ii), Applicant has not submitted copies of U.S. patents and U.S. patent applications.

In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in § 1.56 (b).

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 50-0436, under Order No. 143705.05221.

Respectfully submitted,

Dated: November 11, 2016

Electronic Signature: /Andrew W. Schultz/

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Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Attorney Docket Number	143705.05221

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First Named Inventor	Martin U. Pralle
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Examiner Name	Long Pham
Attorney Docket Number	143705.05221

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	2	20030228883		2003-12-11	Kusakari et al.	
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	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	Long Pham
	Attorney Docket Number	143705.05221

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	13	20140198240		2014-07-17	Rhoads	
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	5	EP1818855	EP		2007-08-15	Smart Wireless Corp.		

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First Named Inventor	Martin U. Pralle
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Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Attorney Docket Number	143705.05221

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That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Andrew W. Schultz/	Date (YYYY-MM-DD)	2016-11-11
Name/Print	Andrew W. Schultz	Registration Number	66869

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

SAMSUNG EX. 1002 - 1795/2862

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/216,244	Filing Date 07/21/2016	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **11/11/2016**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 32	Minus	** 26	= 6	X $80 =	480
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	**480**

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
BRENDA HARRISON

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

SAMSUNG EX. 1002 - 1796/2862

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/216,244	07/21/2016	Martin U. Pralle	143705.05221	5052

136549 7590 02/13/2017

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
02/13/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketingbn@pepperlaw.com
davisdr@pepperlaw.com

SAMSUNG EX. 1002 - 1797/2862

Office Action Summary	Application No. 15/216,244	Applicant(s) PRALLE ET AL.	
	Examiner LONG PHAM	Art Unit 2814	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/11/16*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *34-65* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *34-61,63 and 64* is/are rejected.

8)☒ Claim(s) *62 and 65* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *1/11/16, 7/22/16*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 34-59 and 60-65 in the reply filed on 11/11/16 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim(s) 34-40 and 51 is/are rejected under pre-AIA 35 U.S.C. 102(e) as being anticipated by Velichko (US pub 20130200251).

With respect to claim 34, Velichko teaches a light trapping device, comprising (see figs. 1-23 and associated text):

at least one light sensitive pixel 34 having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending at least partially around the pixel periphery;

a backside light trapping material 42 substantially covering the backside surface; and

a peripheral light trapping material 36 substantially covering the peripheral sidewall,

wherein the peripheral light trapping material inherently creates a surface field at the peripheral sidewall.

With respect to claim 35, Velichko teaches the backside light trapping material reflects the light incident thereon back into the pixel.

With respect to claim 36, Velichko teaches the peripheral light trapping material reflects light incident thereon into the pixel.

With respect to claim 37, Velichko teaches the peripheral sidewall extends completely around the pixel periphery.

With respect to claim 38, Velichko teaches the peripheral sidewall extends from the light incident surface to the backside surface.

With respect to claim 39, Velichko teaches the peripheral sidewall extends through the pixel substantially from the light incident surface to the backside surface.

With respect to claim 40, Velichko teaches at least one of the backside light trapping material and the peripheral light trapping material comprises a metal layer.

With respect to claim 51, Velichko teaches an array of light trapping pixel devices.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 41, 43, and 44 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Velichko (US pub 20130200251) as applied to claims 34-40 and 51 above, and further in view of Yanagisawa (JP 403183037) (a reference cited by the applicant).

With respect to claims 41, 43, and 44, Velichko teaches the peripheral light trapping material but fails to teach the peripheral light trapping material is made of silicon oxide or having a refractive index of less than about 2.1 or having a surface recombination velocity as low as 10 cm/s.

Yanagisawa teaches using a material of silicon oxide or having a refractive index of less than about 2.1 or having a surface recombination velocity as low as 10 cm/s to control reflectivity. See English abstract.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Yanagisawa into the device of Velichko to achieve the above benefit.

Claims 46-50 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Velichko (US pub 20130200251) as applied to claims 34-40 and 51 above, and further in view of Bour et al. (US pat 8470619).

With respect to claims 46-50, Velichko fails to a textured film layer is located on the incident light surface.

Bour et al. teach using a textured layer of metal or Al to enhance or control reflection of incident light. See col. 3, lines 40-50.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Bour et al. into the device of Velichko to achieve light efficiency. See col. 3, lines 40-50.

Claims 42 and 45 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Velichko (US pub 20130200251) as applied to claims 34-40 and 51 above, and further in view of Gray et al. (US pat 8906670).

With respect to claims 42 and 45, Velichko teaches the peripheral light trapping material but fails to teach the peripheral light trapping material is made of aluminum oxide or having passivating negative charge.

Gray et al. teach using a material of aluminum oxide or having passivating negative charge to control reflectivity. See col. 2, lines 1-15.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Gray et al. into the device of Velichko to achieve the above benefit. See col. 2, lines 1-15.

Claims 52, 54, 55, 56, and 57, 53, 58, 59, 60-61, and 63-64 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Velichko (US pub 20130200251) in combination with Bour et al. (US pat 8470619).

With respect to claims 52, 54, 55, 56, and 57, Velichko teaches a light trapping device, comprising (see figs. 1-23 and associated text):

at least one light sensitive pixel 34 having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending at least partially around the pixel periphery;

a backside light trapping material 42 at least partially covering the backside surface; and

a peripheral light trapping material 36 substantially covering the peripheral sidewall.

With respect to claims 52, 54, 55, 56, and 57, Velichko fails to teach a textured film layer is located on the incident light surface to increase quantum efficiency of the device.

Bour et al. teach using a textured layer of metal or Al to enhance or control reflection of incident light. See col. 3, lines 40-50.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Bour et al. into the device of Velichko to achieve light efficiency. See col. 3, lines 40-50.

With respect to claim 53, Velichko teaches said backside light trapping material substantially covers the backside surface.

With respect to claim 58, Velichko teaches the peripheral sidewall extends from the light incident surface to the backside surface.

With respect to claim 59, Velichko teaches the peripheral sidewall extends through the pixel substantially from the light incident surface to the backside surface.

With respect to claims 60, 61, 63, and 64, how the textured region is formed has not been given patentable weight because the claimed invention is directed to a device.

Allowable Subject Matter

Claims 62 and 65 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LONG PHAM whose telephone number is (571)272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To

schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

/LONG PHAM/
Primary Examiner, Art Unit 2814

Notice of References Cited	Application/Control No. 15/216,244	Applicant(s)/Patent Under Reexamination PRALLE ET AL.	
	Examiner LONG PHAM	Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2013/0200251 A1	08-2013	Velichko; Sergey	H01L31/02327	250/208.1
*	B	US-8,470,619 B2	06-2013	Bour; David P.	H01L21/268	257/98
*	C	US-8,906,670 B2	12-2014	Gray; Jeremy	G01N21/6452	422/407
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Substitute for Form 1449/PTO				Complete if Known	
				Application No.:	15/216,244
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date:	July 21, 2016
				First Named Inventor:	Martin U. Pralle
				Group Art Unit:	TBA
(use as many sheets as necessary)				Examiner Name:	TBA
Sheet	1	of	20	Attorney Docket No.:	143705.05221

U. S. PATENT DOCUMENTS

Examiner's Initials	Cite No.	U.S. Patent Document Number Kind Code (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
	A1	3487223	St. John	12/30/1969		
	A2	3922571	Smith	11/25/1975		
	A3	3973994	Redfield	8/10/1976		
	A4	3994012	Warner, Jr.	11/23/1976		
	A5	4017887	Davies et al.	4/12/1977		
	A6	4149174	Shannon	4/10/1979		
	A7	4176365	Kroger	11/27/1979		
	A8	4201450	Trapani	5/6/1980		
	A9	4242149	King et al.	12/30/1980		
	A10	4253882	Dalal	3/3/1981		
	A11	4277793	Webb	7/7/1981		
	A12	4322571	Stanbery	3/30/1982		
	A13	4419533	Czubatyj et al.	12/6/1983		
	A14	4452826	Shields et al.	6/5/1984		
	A15	4493942	Sheng et al.	1/15/1985		
	A16	4514582	Tiedje et al.	4/30/1985		
	A17	4536608	Sheng et al.	8/20/1985		
	A18	4568960	Petroff et al.	2/4/1986		
	A19	4593303	Dyck et al.	6/3/1986		
	A20	4593313	Nagasaki	6/3/1986		
	A21	4617593	Dudley	10/14/1986		
	A22	4630082	Sakai	12/16/1986		
	A23	4648936	Ashby et al.	3/10/1987		
	A24	4663188	Kane	5/5/1987		
	A25	4672206	Suzuki	6/9/1987		
	A26	4673770	Mandelkorn	6/16/1987		
	A27	4679068	Lillquist et al.	7/7/1987		
	A28	4751571	Lillquist	6/14/1988		
	A29	4775425	Guha et al.	10/4/1988		
	A30	4777490	Sharma et al.	10/11/1988		
	A31	4829013	Yamazaki	5/9/1989		
	A32	4883962	Elliot	11/28/1989		
	A33	4887255	Handa et al.	12/12/1989		
	A34	4894526	Bethea et al.	1/16/1990		
	A35	4910568	Taki, et al.	3/20/1990		
	A36	4910588	Kinoshita, et al.	3/20/1990		
	A37	4964134	Westbrook et al.	10/16/1990		
Examiner Signature		/LONG PHAM/		Date Considered	02/07/2017	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /LP/

SAMSUNG EX. 1002 - 1808/2862

Substitute for Form 1449/PTO				Complete if Known	
				Application No.:	15/216,244
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date:	July 21, 2016
				First Named Inventor:	Martin U. Pralle
				Group Art Unit:	TBA
(use as many sheets as necessary)				Examiner Name:	TBA
Sheet	2	of	20	Attorney Docket No.:	143705.05221

	A38	4965784	Land et al.	10/23/1990		
	A39	4968372	Maass	11/6/1990		
	A40	4999308	Nishiura et al.	3/12/1991		
	A41	5021100	Ishihara et al.	6/4/1991		
	A42	5021854	Huth	6/4/1991		
	A43	5080725	Green et al.	1/14/1992		
	A44	5081049	Green et al.	1/14/1992		
	A45	5100478	Kawabata	3/31/1992		
	A46	5114876	Weiner	5/19/1992		
	A47	5127964	Hamakawa et la.	7/7/1992		
	A48	5164324	Russell et al.	11/17/1992		
	A49	5208822	Haus et al	5/4/1993		
	A50	5223043	Olson et al.	6/29/1993		
	A51	5234790	Lang, et al.	8/10/1993		
	A52	5244817	Hawkins et al.	9/14/1993		
	A53	5296045	Banerjee et al.	3/22/1994		
	A54	5309275	Nishimura et al.	5/3/1994		
	A55	5322988	Russell et al.	6/21/1994		
	A56	5346850	Kaschmitter et al.	9/13/1994		
	A57	5370747	Noguchi et al.	12/6/1994		
	A58	5373182	Norton	12/13/1994		
	A59	5381431	Zayhowski	1/10/1995		
	A60	5383217	Uemura	1/17/1995		
	A61	5390201	Tomono et al.	2/14/1995		
	A62	5413100	Barthelemy et al.	5/9/1995		
	A63	5449626	Hezel	9/12/1995		
	A64	5454347	Shibata et al.	10/3/1995		
	A65	5502329	Pezzani	3/26/1996		
	A66	5523570	Hairston	6/4/1996		
	A67	5559361	Pezzani	9/24/1996		
	A68	5569615	Yamazaki et al.	10/29/1996		
	A69	5578858	Mueller et al.	11/26/1996		
	A70	5580615	Itoh et al.	12/3/1996		
	A71	5589008	Kepper	12/31/1996		
	A72	5589704	Levine	12/31/1996		
	A73	5597621	Hummel et al.	1/18/1997		
	A74	5627081	Tsuo et al.	5/6/1997		
	A75	5640013	Ishikawa, et al.	6/17/1997		
	A76	5641362	Meier	6/24/1997		
	A77	5705413	Harkin et al.	1/6/1998		
	A78	5705828	Noguchi et al.	1/6/1998		
	A79	5708486	Miyawaki et al.	1/13/1998		
	A80	5710442	Watanabe et al.	1/20/1998		
	A81	5714404	Mititsky et al.	2/3/1998		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date:	July 21, 2016
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	A82	5731213	Ono	3/24/1998		
	A83	5751005	Wyles et al.	5/12/1998		
	A84	5758644	Diab et el.	6/2/1998		
	A85	5766127	Pologe et al.	6/16/1998		
	A86	5766964	Rohatgi et al.	6/16/1998		
	A87	5773820	Osajda, et al.	6/30/1998		
	A88	5779631	Chance	7/14/1998		
	A89	5781392	Clark	7/14/1998		
	A90	5792280	Ruby et al	8/11/1998		
	A91	5808350	Jack et al	9/15/1998		
	A92	5859446	Nagasu et al.	1/12/1999		
	A93	5861639	Bernier	1/19/1999		
	A94	5923071	Saito	7/13/1999		
	A95	5935320	Graf et al.	8/10/1999		
	A96	5942789	Morikawa	8/24/1999		
	A97	5943584	Shim et al	8/24/1999		
	A98	5963790	Matsuno et al	10/5/1999		
	A99	5977603	Ishikawa	11/2/1999		
	A100	6071796	Voutsas	6/6/2000		
	A101	6072117	Matsuyama et al.	6/6/2000		
	A102	6080988	Ishizuya et al.	6/27/2000		
	A103	6097031	Cole	8/1/2000		
	A104	6106689	Matsuyama	8/22/2000		
	A105	6107618	Fossum et al.	8/22/2000		
	A106	6111300	Cao et al.	8/29/2000		
	A107	6147297	Wettling et al.	11/14/2000		
	A108	6160833	Floyd et al.	12/12/2000		
	A109	6168965	Malinovich, et al.	1/2/2001		
	A110	6194722	Fiorini et al.	2/27/2001		
	A111	6229192	Gu	5/8/2001		
	A112	6252256	Ugge et al.	6/26/2001		
	A113	6290713	Russell	9/18/2001		
	A114	6291302	Yu	9/18/2001		
	A115	6313901	Cacharelis	11/6/2001		
	A116	6320296	Fujii et al.	11/20/2001		
	A117	6331445	Janz et al	12/18/2001		
	A118	6372591	Mineji et al.	4/16/2002		
	A119	6372611	Horikawa	4/16/2002		
	A120	6379979	Connolly	4/30/2002		
	A121	6420706	Lurie, et al.	7/16/2002		
	A122	6429036	Nixon, et al.	8/6/2002		
	A123	6429037	Wenham et al.	8/6/2002		
	A124	6465860	Shigenaka, et al.	10/15/2002		
	A125	6475839	Zhang, et al.	11/5/2002		

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	A126	6483116	Kozlowski et al.	11/19/2002		
	A127	6483929	Marakami et al.	11/19/2002		
	A128	6486522	Bishay et al.	11/26/2002		
	A129	6493567	Krivitski et al.	12/10/2002		
	A130	6498336	Tian et al.	12/24/2002		
	A131	6500690	Yamagishi et al.	12/31/2002		
	A132	6504178	Carlson et al.	1/7/2003		
	A133	6580053	Voutsas	6/17/2003		
	A134	6583936	Kaminsky et al.	6/24/2003		
	A135	6597025	Lauter et al	7/22/2003		
	A136	6607927	Ramappa et al.	8/19/2003		
	A137	6624049	Yamazaki	9/23/2003		
	A138	6639253	Duane et al.	10/28/2003		
	A139	6667528	Cohen et al.	12/23/2003		
	A140	6677655	Fitzgerald	1/13/2004		
	A141	6677656	Francois	1/13/2004		
	A142	6683326	Iguchi, et al.	1/27/2004		
	A143	6689209	Falster et el.	2/10/2004		
	A144	6753585	Kindt	6/22/2004		
	A145	6759262	Theil et al.	7/6/2004		
	A146	6790701	Shigenaka, et al.	9/14/2004		
	A147	6800541	Okumura	10/5/2004		
	A148	6801799	Mendelson	10/5/2004		
	A149	6803555	Parrish et al.	10/12/2004		
	A150	6815685	Wany	11/9/2004		
	A151	6818535	Lu et al.	11/16/2004		
	A152	6822313	Matsushita	11/23/2004		
	A153	6825057	Heyers, et al.	11/30/2004		
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	A155	6864190	Han et al.	3/8/2005		
	A156	6867806	Lee et al.	3/15/2005		
	A157	6900839	Kozlowski et al.	5/31/2005		
	A158	6911375	Guarini et al.	6/28/2005		
	A159	6919587	Ballon et al.	7/19/2005		
	A160	6923625	Sparks	8/2/2005		
	A161	6927432	Holm, et al.	8/9/2005		
	A162	6984816	Holm, et al.	1/10/2006		
	A163	7008854	Forbes	3/7/2006		
	A164	7041525	Clevenger et al.	5/9/2006		
	A165	7057256	Carey, III et al.	6/6/2006		
	A166	7075079	Wood	7/11/2006		
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	A168	7109517	Zaidi	9/19/2006		
	A169	7126212	Enquist et al.	10/24/2006		

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	A171	7202102	Yao	4/10/2007		
	A172	7211501	Liu et al	5/1/2007		
	A173	7235812	Chu, et al.	6/26/2007		
	A174	7247527	Shimomura et al.	7/24/2007		
	A175	7247812	Tsao	7/24/2007		
	A176	7256102	Nakata, et al.	8/14/2007		
	A177	7271445	Forbes	9/18/2007		
	A178	7271835	Iizuka et al.	9/18/2007		
	A179	7285482	Ochi	10/23/2007		
	A180	7314832	Kountz et al.	1/1/2008		
	A181	7354792	Carey, III et al.	4/8/2008		
	A182	7358498	Geng et al.	4/15/2008		
	A183	7375378	Manivannan et al.	5/20/2008		
	A184	7390689	Mazur et al.	6/24/2008		
	A185	7432148	Li et al.	10/7/2008		
	A186	7442629	Mazur et al.	10/28/2008		
	A187	7446359	Lee, et al.	11/4/2008		
	A188	7446807	Hong	11/7/2008		
	A189	7456452	Wells et al.	11/25/2008		
	A190	7482532	Yi et al.	1/27/2009		
	A191	7498650	Lauxtermann	3/3/2009		
	A192	7504325	Koezuka et al.	3/17/2009		
	A193	7504702	Mazur et al.	3/17/2009		
	A194	7511750	Murakami	3/31/2009		
	A195	7521737	Augusto	4/21/2009		
	A196	7528463	Forbes	5/5/2009		
	A197	7542085	Altice, Jr. et al.	6/2/2009		
	A198	7547616	Fogel et al.	6/16/2009		
	A199	7551059	Farrier	6/23/2009		
	A200	7560750	Niira et al.	7/14/2009		
	A201	7564631	Li, et al.	7/21/2009		
	A202	7582515	Choi et al.	9/1/2009		
	A203	7592593	Kauffman, et al.	9/22/2009		
	A204	7595213	Kwon et al.	9/29/2009		
	A205	7605397	Kindem et al.	10/20/2009		
	A206	7615808	Pain, et al.	11/10/2009		
	A207	7618839	Rhodes	11/17/2009		
	A208	7619269	Ohkawa	11/17/2009		
	A209	7629582	Hoffman, et al.	12/8/2009		
	A210	7648851	Fu, et al.	1/19/2010		
	A211	7649156	Lee	1/19/2010		
	A212	7705879	Kerr et al.	4/27/2010		
	A213	7731665	Lee et al	6/8/2010		

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	A214	7741666	Nozaki, et al.	6/22/2010		
	A215	7745901	McCaffrey et al	6/29/2010		
	A216	7763913	Fan et al	7/27/2010		
	A217	7772028	Adkisson et al	8/10/2010		
	A218	7781856	Mazur et al.	8/24/2010		
	A219	7800192	Venezia, et al.	9/21/2010		
	A220	7816220	Mazur et al.	10/19/2010		
	A221	7828983	Weber et al	11/9/2010		
	A222	7847253	Carey et al.	12/7/2010		
	A223	7847326	Park, et al.	12/7/2010		
	A224	7855406	Yamaguchi et al	12/21/2010		
	A225	7875498	Elbanhawy, et al.	1/25/2011		
	A226	7880168	Lenchenkov	2/1/2011		
	A227	7884439	Mazur et al.	2/8/2011		
	A228	7884446	Mazur et al.	2/8/2011		
	A229	7910964	Kawahito et al.	3/22/2011		
	A230	7923801	Tian et al.	4/12/2011		
	A231	7968834	Veeder	6/28/2011		
	A232	8008205	Fukushima et al.	8/30/2011		
	A233	8013411	Cole	9/6/2011		
	A234	8030726	Sumi	10/4/2011		
	A235	8035343	Seman Jr.	10/11/2011		
	A236	8058615	McCaffrey	11/15/2011		
	A237	8080467	Carey et al.	12/20/2011		
	A238	8088219	Knerer et al.	1/3/2012		
	A239	8093559	Rajavel	1/10/2012		
	A240	8164126	Moon, et al.	4/24/2012		
	A241	8207051	Sickler et al.	6/26/2012		
	A242	8247259	Grolier et al.	8/21/2012		
	A243	8259293	Andreou et al.	9/4/2012		
	A244	8288702	Veeder	10/16/2012		
	A245	8476681	Haddad et al.	7/2/2013		
	A246	8564087	Yamamura et al.	10/22/2013		
	A247	8603902	Mazer et al.	12/10/2013		
	A248	8629485	Yamamura et al.	1/14/2014		
	A249	8680591	Haddad et al.	3/25/2014		
	A250	8742528	Yamamura et al.	6/3/2014		
	A251	8884226	Miyazaki, et al.	11/11/2014		
	A252	8916945	Sakamoto et al	12/23/2014		
	A253	8994135	Yamamura et al.	6/31/2015		
	A254	9190551	Yamamura et al.	11/17/2015		
	A255	RE43169	Parker	2/7/2012		
	A256	20010017344	Aebi	8/30/2001		
	A257	20010022768	Takahashi	9/20/2001		

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	A258	20010044175	Barret et al.	11/22/2001		
	A259	20020020893	Lhorte	2/21/2002		
	A260	20020024618	Imai	2/28/2002		
	A261	20020056845	Iguchi et al.	5/16/2002		
	A262	20020060322	Tanabe et al.	5/23/2002		
	A263	20020079290	Holdermann	6/27/2002		
	A264	20020117699	Roy	8/29/2002		
	A265	20020148964	Dausch et al.	10/17/2002		
	A266	20020182769	Campbell	12/5/2002		
	A267	20030029495	Mazur et al.	2/13/2003		
	A268	20030030083	Lee et al.	2/13/2003		
	A269	20030045092	Shin	3/6/2003		
	A270	20030057357	Uppal et al.	3/27/2003		
	A271	20030111106	Nagano et al.	6/19/2003		
	A272	20030210332	Frame	11/13/2003		
	A273	20030213515	Sano et al.	11/20/2003		
	A274	20040014307	Shin et al.	1/22/2004		
	A275	20040016886	Ringermacher et al.	1/29/2004		
	A276	20040041168	Hembree et al.	3/4/2004		
	A277	20040046224	Rossel et al.	3/11/2004		
	A278	20040077117	Ding et al.	4/22/2004		
	A279	20040080638	Lee	4/29/2004		
	A280	20040130020	Kuwabara et al.	7/22/2004		
	A281	20040161868	Hong	8/19/2004		
	A282	20040222187	Lin	11/11/2004		
	A283	20040252931	Belleville et al.	12/16/2004		
	A284	20050051822	Manning	3/10/2005		
	A285	20050062041	Terakawa et al.	3/24/2005		
	A286	20050101100	Kretchmer et al.	5/12/2005		
	A287	20050101160	Garg et al.	5/12/2005		
	A288	20050127401	Mazur et al.	6/16/2005		
	A289	20050134698	Schroeder et al.	6/23/2005		
	A290	20050150542	Madan	7/14/2005		
	A291	20050158969	Binnis et al.	7/21/2005		
	A292	20050211996	Krishna, et al.	9/29/2005		
	A293	20050227390	Shtein et al.	10/13/2005		
	A294	20060006482	Rieve, et al.	1/12/2006		
	A295	20060011954	Ueda et al.	1/19/2006		
	A296	20060011955	Baggenstoss	1/19/2006		
	A297	20060060848	Chang et al.	3/23/2006		
	A298	20060071254	Rhodes	4/6/2006		
	A299	20060079062	Mazur et al.	4/13/2006		
	A300	20060097172	Park	5/11/2006		
	A301	20060231914	Carey et al.	10/19/2006		

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	A302	20090097290	Chandrasekaran	4/16/2009		
	A303	20060118781	Rhodes	6/8/2006		
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	A305	20060132633	Nam, et al.	6/22/2006		
	A306	20060138396	Lin, et al.	6/29/2006		
	A307	20060145148	Hirai, et al.	7/6/2006		
	A308	20060145176	Lee	7/6/2006		
	A309	20060160343	Chong et al.	7/20/2006		
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	A314	20060210122	Cleveland	9/21/2006		
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	A318	20060238632	Shah	10/26/2006		
	A319	20060244090	Roy, et al.	11/2/2006		
	A320	20060255340	Manivannan et al.	11/16/2006		
	A321	20060257140	Seger	11/16/2006		
	A322	20070035849	Li et al.	2/15/2007		
	A323	20070035879	Hall,et al.	2/15/2007		
	A324	20070051876	Sumi et al.	3/8/2007		
	A325	20070052050	Dierickx	3/8/2007		
	A326	20070076481	Tennant	4/5/2007		
	A327	20070115554	Breitung et al	5/24/2007		
	A328	20070123005	Hiura et al.	5/31/2007		
	A329	20070138590	Wells, et al.	6/21/2007		
	A330	20070145505	Kim et al.	6/28/2007		
	A331	20070178672	Tanaka, et al.	8/2/2007		
	A332	20070187670	Hsu et al.	8/16/2007		
	A333	20070194356	Moon, et al.	8/23/2007		
	A334	20070194401	Nagai, et al.	8/23/2007		
	A335	20070195056	Lloyd	8/23/2007		
	A336	20070200940	Gruhlke et al.	8/30/2007		
	A337	20070201859	Sarrat	8/30/2007		
	A338	20070235827	Altice	10/11/2007		
	A339	20070247414	Roberts	10/25/2007		
	A340	20070262366	Baek et al.	11/15/2007		
	A341	20070290283	Park et al.	12/20/2007		
	A342	20070296060	Tanabe et al.	12/27/2007		
	A343	20080002863	Northcott	1/3/2008		
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Substitute for Form 1449/PTO				Complete if Known	
				Application No.:	15/216,244
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date:	July 21, 2016
				First Named Inventor:	Martin U. Pralle
				Group Art Unit:	TBA
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☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/07/2016	02/06/2017							
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SAMSUNG EX. 1002 - 1828/2862

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
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Attorney Docket Number	143705.05221

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	10	20100200658		2010-08-12	Olmstead et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	Long Pham
	Attorney Docket Number	143705.05221

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	JPH06244444	JP		1994-09-02	Hatachi Ltd.		
	2	WO200031679	WO		2000-06-02	Iriscan Inc.		
	3	JP2003242125	JP		2003-08-29	Cannon KK		
	4	JP2006255430	JP		2006-09-28	Fujitsu Ltd.		
	5	EP1818855	EP		2007-08-15	Smart Wireless Corp.		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Attorney Docket Number	143705.05221

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Bernhard, C.G., "Structural and Functional Adaptation in a Visual System" Endevor Vol. 26, May 1967. pp. 79-84.	
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EXAMINER SIGNATURE

Examiner Signature	/LONG PHAM/	Date Considered	02/07/2017

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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SAMSUNG EX. 1002 - 1832/2862

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Attorney Docket Number	143705.05221

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Andrew W. Schultz/	Date (YYYY-MM-DD)	2016-11-11
Name/Print	Andrew W. Schultz	Registration Number	66869

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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SAMSUNG EX. 1002 - 1834/2862

Attorney Docket No.: 143705.05221

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Martin U. Pralle Application No.: 15/216,244 Filed: July 21, 2016 For: PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS	Confirmation No.: 5052 Art Unit: 2814 Examiner: Pham, Long

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

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May 12, 2017 (Dated) Electronic Signature: /Reza Mollaaghababa/ (Reza Mollaaghababa, Reg. No. 43,810)

RESPONSE TO NON-FINAL OFFICE ACTION

Dear Sir:

This paper is filed in response to the non-final Office Action dated February 13, 2017.

Amendments to the Claims begin on page 2.

Remarks begin on page 6.

AMENDMENTS TO THE CLAIMS

1-33. (Canceled)

34. (Currently Amended) A light trapping device, comprising:

at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending at least partially around the pixel periphery;

a backside light trapping material substantially covering the backside surface; ~~and~~

a peripheral light trapping material substantially covering the peripheral sidewall[[,]]; and

at least one doped region disposed on at least one of the light incident surface and the backside surface,

wherein the peripheral light trapping material creates a surface field at the peripheral sidewall.

35. (Previously Presented) The device of claim 34, wherein the backside light trapping material reflects the light incident thereon back into the pixel.

36. (Previously Presented) The device of claim 34, wherein the peripheral light trapping material reflects light incident thereon into the pixel.

37. (Previously Presented) The device of claim 34, wherein the peripheral sidewall extends completely around the pixel periphery.

38. (Previously Presented) The device of claim 34, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

39. (Previously Presented) The device of claim 34, wherein the peripheral sidewall extends through the pixel substantially from the light incident surface to the backside surface.

40. (Previously Presented) The device of claim 34, wherein at least one of the backside light trapping material and the peripheral light trapping material comprises a metal layer.

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41. (Previously Presented) The device of claim 34, wherein said peripheral light trapping material comprises an oxide.

42. (Previously Presented) The device of claim 34, wherein said peripheral light trapping material provides a passivating negative charge.

43. (Previously Presented) The device of claim 34, wherein said peripheral light trapping material exhibits a surface recombination velocity as low as 10 cm/s.

44. (Previously Presented) The device of claim 34, wherein the peripheral sidewall material has an index of refraction of less than about 2.1.

45. (Previously Presented) The device of claim 34, wherein the peripheral light trapping material comprises any of aluminum oxide and hafnium oxide.

46. (Previously Presented) The device of claim 34, wherein said pixel comprises a textured region.

47. (Previously Presented) The device of claim 46, wherein said textured region is coupled to the light incident surface.

48. (Previously Presented) The device of claim 47, wherein said textured region is located on said light incident surface.

49. (Previously Presented) The device of claim 47, wherein said textured region comprises a textured film layer.

50. (Previously Presented) The device of claim 49, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.

51. (Previously Presented) An array of light trapping pixel devices of claim 34.

SAMSUNG EX. 1002 - 1837/2862

52. (Currently Amended) A light trapping device, comprising:

at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending at least partially around the pixel periphery;

a backside light trapping material at least partially covering the backside surface;

a peripheral light trapping material substantially covering the peripheral sidewall; ~~and~~

at least one doped region disposed on at least one of the light incident surface and the backside surface; and

a textured region positioned to interact with light incident thereon so as to increase quantum efficiency of the device.

53. (Previously Presented) The device of claim 52, wherein said backside light trapping material substantially covers the backside surface.

54. (Previously Presented) The device of claim 52, wherein said textured region is located on the light incident surface.

55. (Previously Presented) The device of claim 52, wherein said textured region is a textured film layer coupled to the light incident surface.

56. (Previously Presented) The device of claim 55, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.

57. (Previously Presented) The device of claim 52, wherein said textured region reflects at least a portion of light internally incident thereon into the pixel.

58. (Previously Presented) The device of claim 52, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

59. (Previously Presented) The device of claim 34, wherein the peripheral sidewall extends through the pixel substantially from the light incident surface to the backside surface.

SAMSUNG EX. 1002 - 1838/2862

60. (Previously Presented) The device of claim 52, wherein the textured region is formed by one of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.

61. (Currently Amended) The device of claim 52, wherein the textured region is formed by ~~lasing~~ laser radiation.

62. (Canceled)

63. (Previously Presented) The device of claim 46, wherein the textured region is formed by one of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.

64. (Currently Amended) The device of claim 46, wherein the textured region is formed by ~~lasing~~ laser radiation.

65. (Canceled)

66. (New) The device of claim 46, wherein said textured region is coupled to said backside surface.

SAMSUNG EX. 1002 - 1839/2862

REMARKS

Allowable Claims

The Office Action indicates that claims 62 and 65 are allowable if rewritten in independent form to include all of the limitations of the base claims on which they depend.

Claim 62 depends on independent claim 52 and claim 65 depends on independent claim 34. Applicants amend independent claims 34 and 52 to incorporate the limitations of allowable claims 65 and 62, respectively. Thus, amended claims 34 and 52 as well as the remainder of the pending claims, which depend on these claims, are believed to be in condition for allowance.

Rejections Pursuant to 35 U.S.C. §102

Claims 34-40 and 51 are rejected as being anticipated by Velichko.

In view of the above amendments, the rejection of these claims is moot and will not be discussed.

Rejections Pursuant to 35 U.S.C. §103

Claims 41, 43, and 44 are rejected as being unpatentable over Velichko in view of Yanagisawa.

In view of the above amendments, the rejection of these claims is moot and will not be discussed.

New Claim

New Independent claim 66 depends on claim 46, which in turn depends on claim 34, and further recites that said textured region is coupled to said backside surface. Support for the new claim 66 can be found in paragraph [0039] of the published U.S. patent application.

New claim 66 is patentable at least because of its dependence on allowable claim 34.

CONCLUSION

In view of the above amendments and remarks, Applicants respectfully request reconsideration and allowance of the application. Applicants invite the Examiner to call the undersigned if there are any outstanding issues.

SAMSUNG EX. 1002 - 1840/2862

Dated: May 12, 2017

Electronic Signature: /Reza Mollaaghababa/

Reza Mollaaghababa, Reg. No. 43,810
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Pepper Hamilton LLP
125 High Street
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Boston, MA 02210
Tel: (617) 204-5168
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SAMSUNG EX. 1002 - 1841/2862

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Martin U. Pralle	Confirmation No.: 5052
Application No.: 15/216,244	Art Unit: 2814
Filed: July 21, 2016	Examiner: Pham, Long
For: PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS	

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Commissioner for Patents
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May 12, 2017 (Dated) — Electronic Signature: /Reza Mollaaghababa/ Reza Mollaaghababa, Reg. No. 43,810

INFORMATION DISCLOSURE STATEMENT (IDS) TRANSMITTAL LETTER

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed more than three months after the U.S. filing date, OR more than three months after the date of entry of the national stage of a PCT application, AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Office Action or Notice of Allowance (37 CFR 1.97(c)). This IDS is accompanied with the fee set forth in 37 C.F.R. 1.17(p).

In accordance with 37 CFR 1.98(a)(2)(ii), Applicant has not submitted copies of U.S. patents and U.S. patent applications.

In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information

as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in § 1.56 (b).

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 50-0436, under Order No. 143705.05221.

Respectfully submitted,

Dated: May 12, 2017

Electronic Signature: /Reza Mollaaghababa/

Reza Mollaaghababa, Reg. No. 43,810
Attorney for Applicant
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SAMSUNG EX. 1002 - 1843/2862

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(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Attorney Docket Number	143705.05221

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4886958		1989-12-12	Merryman	
	2	5351446		1994-10-04	Langsdorf	
	3	5641969		1997-06-24	Cooke et al.	
	4	5727096		1998-03-10	Ghirardi et al.	
	5	6327022		2001-12-04	Nishi	
	6	6331885		2001-12-18	Nishi	
	7	6340281		2002-01-22	Haraguchi	
	8	7800684		2010-09-21	Tatani	

SAMSUNG EX. 1002 - 1844/2862

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	Long Pham
	Attorney Docket Number	143705.05221

	9	7897942		2011-03-01	Bereket	
	10	9184204		2015-11-10	Hu	
	11	9369641		2016-06-14	Hu	

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	1	20010044266		2001-11-22	Katsuoka	
	2	20050088634		2005-04-28	Kosugi	
	3	20090093100		2005-05-06	Chen	
	4	20080173620		2008-07-24	Grek	
	5	20090027640		2009-01-29	Shibazaki	
	6	20090114630		2009-05-07	Hawryluk	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	Long Pham
	Attorney Docket Number	143705.05221

	7	20090308457		2009-12-17	Smith et al.	
	8	20100140768		2010-06-10	Zafiropoulo	
	9	20130135439		2013-05-30	Kakuko et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	19838439	DE		2000-04-27	Fraunhofer-Ges Forschung		
	2	2509107	EP		2012-10-10	Boly Media Comm.		
	3	2010278472	JP		2010-12-09	Sony, Corp.		
	4	100825808	KR		2008-04-29	Samsung Electronics Co. Ltd.		
	5	20090077274	KR		2009-07-15	LG Electronics Inc.		
	6	2009147085	WO		2009-12-10	Thiel et al.		

SAMSUNG EX. 1002 - 1846/2862

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	Long Pham
	Attorney Docket Number	143705.05221

	7	2011003871	WO		2011-01-13	International Business Machines Corporation		
	8	2011035188	WO		2011-03-24	Sionyx, Inc.		
	9	2011119618	WO		2011-03-22	Sionyx, Inc.		
	10	2012174752	WO		2012-12-27	Boly Media Comm.		
	11	2014110484	WO		2014-07-17	Digimarc Corp.		

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	1	Carey, P.G. et al., "In-situ Doping of Silicon Using Gas Immersion Laser Doping (GILD) Process," Appl. Surf. Sci. 43, 325-332 (1989).	
	2	Gibbons, J., "Ion Implantation in Semiconductors-Part II; Damage Production and Annealing", proceedings of the IEEE Vol. 60, No. 9 pp. 1062-1096. Jun. 1972.	
	3	Ziou et al., "Depth from defocus using the hermite transform", IMAGE PROCESSING, 1998. ICIP 98. Intl. Conference on Chicago, IL. October 1998 pp. 958 - 962.	

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SAMSUNG EX. 1002 - 1847/2862

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	Long Pham
	Attorney Docket Number	143705.05221

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SAMSUNG EX. 1002 - 1848/2862

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Attorney Docket Number	143705.05221

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See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

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SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Reza Mollaaghababa/	Date (YYYY-MM-DD)	2017-05-12
Name/Print	Reza Mollaaghababa	Registration Number	43810

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Espacenet

Bibliographic data: DE19838439 (C1) — 2000-04-27

Vertically integrated thin film photodiode, for photodetector used e.g. in optical data storage and transmission, is produced by thinning and reflective coating of a photodiode substrate bonded to a temporary substrate

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Classification: **- international:** ***H01L31/0216; H01L31/0232; H01L31/0236;*** (IPC1-7): H01L31/0232; H01L31/0236; H01L31/102
- cooperative: **H01L31/02161**; **H01L31/0232**; **H01L31/0236**; Y02E10/50

Application number: DE1998138439 19980824

Priority number (s): DE1998138439 19980824

Abstract of DE19838439 (C1)

Thin film photodiode production comprises thinning and reflective coating of a photodiode substrate (1) bonded to a temporary substrate prior to bonding to a third substrate. A thin film photodiode is produced by bonding the photodiode side of a first substrate (1) to a second substrate, thinning the first substrate to a few microns thickness, applying a reflective layer or layer sequence onto the first substrate, bonding the reflective side of the first substrate onto a third substrate and removing the second substrate.

(19) BUNDESREPUBLIK DEUTSCHLAND

DEUTSCHES PATENT- UND MARKENAMT

(12) **Patentschrift**

(10) **DE 198 38 439 C 1**

(51) Int. Cl.[7]:
H 01 L 31/102
H 01 L 31/0232
H 01 L 31/0236

(21) Aktenzeichen: 198 38 439.4-33
(22) Anmeldetag: 24. 8. 1998
(43) Offenlegungstag: –
(45) Veröffentlichungstag der Patenterteilung: 27. 4. 2000

Innerhalb von 3 Monaten nach Veröffentlichung der Erteilung kann Einspruch erhoben werden

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(56) Für die Beurteilung der Patentfähigkeit in Betracht gezogene Druckschriften:

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(54) Dünnfilmphotodiode und Verfahren zur Herstellung

(57) Die Erfindung betrifft Dünnfilmphotodioden und ein Verfahren zur Herstellung.
Bei dem Verfahren wird ein erstes Substrat, das auf einer ersten Seite eine Photodiode aufweist, bereitgestellt. Das erste Substrat wird mit einem zweiten Substrat verbunden, wobei die erste Seite zum zweiten Substrat gerichtet ist. Das erste Substrat wird dann von einer zweiten, der ersten gegenüberliegenden Seite, bis auf eine Dicke von wenigen Mikrometern gedünnt. Anschließend wird eine die zu detektierende Strahlung reflektierende Schicht oder Schichtfolge auf die zweite Seite des ersten Substrates aufgebracht. Schließlich werden das erste Substrat auf ein drittes Substrat aufgebracht und das zweite Substrat entfernt.
Durch die erfindungsgemäße reflektierende Schicht an der Unterseite der Photodiode wird die Strahlung umgelenkt und durchdringt erneut die optisch aktive Schicht der Photodiode, so daß der Wirkungsgrad von Dünnfilmphotodioden stark erhöht wird.

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Beschreibung

Die Erfindung betrifft ein Verfahren zur Herstellung einer Dünnfilmphotodiode mit hohem Wirkungsgrad.

Es gibt derzeit viele technische Systeme, bei denen optische Signale erfaßt und zur Weiterverarbeitung in elektrische Signale umgewandelt werden müssen. Beispiele hierfür sind die Anwendungsfelder (magneto-)optische Datenspeicherung, wie bei CD-, DVD- oder MO-Laufwerken, die optische Datenübertragung über Glasfasernetzwerke, sowie die Bereiche Bildverarbeitung, Mustererkennung und optische Spektroskopie. Zur Detektion der elektromagnetischen Strahlung werden bei diesen Systemen in der Regel Halbleiter-Photodioden als Photodetektoren verwendet, die je nach Anforderung als Einzeldiode, Diodenzeile oder Diodenarray angeordnet werden. Im Bereich der Bildverarbeitung kommen hierbei insbesondere zeilenweise oder flächig angeordnete Detektoren zum Einsatz.

Als Grundmaterial zur Herstellung von Photodioden wird ein Halbleitersubstrat, beispielsweise aus Silizium, Germanium, III-V- oder IV-VI-Verbindungen, verwendet. Beispiele für III-V-Halbleiter sind GaAs, GaP, InP, InAs, InSb, GaInAs oder InGaAsP, für IV-VI-Halbleiter PbSe, PbTe.

Die einfallende elektromagnetische Strahlung wird im Halbleitersubstrat absorbiert und erzeugt Ladungsträger, die schließlich einen Photostrom hervorrufen. Die Größe des Stromflusses hängt von der Beleuchtungsstärke der zu erfassenden Strahlung ab. Der detektierbare Wellenlängenbereich wird durch das verwendete Halbleiter-Grundmaterial bestimmt. Dieser liegt im Fall von Silizium bei ca. 200 nm bis 1100 nm, während er bei Germanium ca. 200 nm bis 1700 nm umfaßt.

Zwischen den beiden Elektroden der Photodiode wird eine Raumladungszone erzeugt, in deren elektrischem Feld die Trennung der generierten Ladungsträger erfolgt. Um einen hohen Wirkungsgrad der Photodiode zu erhalten, muß gewährleistet werden, daß ein möglichst großer Teil der Strahlung in die Diode eingekoppelt und weitgehend innerhalb der Raumladungszone absorbiert wird. Außerhalb der Raumladungszone erzeugte Ladungsträger rekombinieren überwiegend und tragen nicht zum Photostrom bei. Die Rekombinationsrate wird durch Störungen des Kristallgitters und Defekte, die auch durch Verunreinigungen hervorgerufen werden können, erhöht und ist insbesondere im Bereich der Oberfläche sehr hoch.

Die Strahlungseinkopplung in die Photodiode wird durch die Brechungsindizes des Halbleitermaterials, der Deckschicht über der Photodiode und der Umgebung bestimmt. Bei monochromatischer Strahlung treten außerdem Interferenzeffekte durch Reflexionen an Grenzflächen auf, die die Transmission beeinflussen. Durch geeignete Wahl der Deckschichten über der Photodiode können eine optische Vergütung realisiert und die Strahlungseinkopplung für eine Wellenlänge oder einen Wellenlängenbereich optimiert werden.

Die Intensität der einfallenden Strahlung nimmt gemäß dem Absorptionsgesetz exponentiell mit zunehmender Eindringtiefe ab. Die Absorption und damit die Eindringtiefe werden durch den Absorptionskoeffizienten bestimmt, der hauptsächlich vom Halbleitermaterial und dessen Dotierung, sowie von der Wellenlänge der Strahlung abhängt. Die Absorption steigt in der Regel mit sinkender Wellenlänge und zunehmender Dotierung an. Ebenso bewirken Kristallstörungen, wie sie in polykristallinem oder amorphem Material in starkem Maß vorliegen, ein Ansteigen der Strahlungsabsorption.

Die Weite der Raumladungszone hängt bei gegebener elektrischer Spannung im Wesentlichen von der Dotierung des Halbleiters ab und nimmt mit sinkendem Dotierungsniveau zu. Häufig werden daher sog. pin-Photodioden verwendet, die eine intrinsische Halbleiterschicht enthalten, die sehr niedrig dotiert ist. Damit können Raumladungszonen mit einer Ausdehnung von mehreren Mikrometern erzeugt werden.

Lag in der Vergangenheit der Schwerpunkt der Entwicklung bei der Fertigung von Einzelphotodioden, so macht die zunehmende Nachfrage nach Gesamtsystemlösungen die Herstellung von integrierten Systemen erforderlich, bei denen Detektoren mit der dazugehörenden Auswerteelektronik, die Verstärkungs-, Logik- oder Speicherelemente enthalten kann, integriert werden.

Neben der monolithischen Integration, bei der Detektoren und Elektronik nebeneinander auf einem Substrat erzeugt werden, gewinnt mittlerweile die vertikale Integration (siehe z. B. Y. Akasaka, Proc IEEE 74 (1986) 1703) bzw. die Herstellung von Dünnfilmelementen für Anwendungen, die mit dem Begriff "Smart Label" umschrieben werden, eine immer größere Bedeutung. Hierbei spielen auch die Kosten eine Rolle, da die monolithische Integration zum einen die Entwicklung von speziellen Fertigungsprozessen erfordert und insgesamt höhere Fertigungskosten verursacht. Zum anderen sind Photodioden im Vergleich zur Auswerteelektronik verhältnismäßig einfache Elemente, die in der Regel eine große Fläche beanspruchen. Bei der Integration fallen damit für die Photodioden wesentlich höhere Flächenkosten an, als bei der Fertigung im Rahmen eines einfachen Photodiodenprozesses. Für die genannten Anwendungsgebiete ist es erforderlich, Photodioden in dünnen Halbleiterfilmen mit Dicken von wenigen Mikrometern herzustellen.

Eine Problematik bei der vertikalen Integration ist die Herstellung von elektrischen Verbindungen zwischen den einzelnen Ebenen. Es sind jedoch Verfahren zur Herstellung von dreidimensionalen Schaltungsanordnungen bekannt, mit denen nach dem Aufbringen der Ebene elektrische Verbindungen hergestellt werden können (siehe z. B. US-A-5563084). Voraussetzung dafür ist jedoch in der Regel, daß die einzelnen Ebenen möglichst dünn sind, typischerweise wenige Mikrometer. Die Dicke wird dabei überwiegend durch die Verdrahtungsebenen (Mehrlagenmetallisierung) bestimmt, das Siliziumsubstrat wird in der Regel bis auf Restdicken von bis zu 0,5 µm gedünnt.

Andererseits beträgt die Eindringtiefe der Strahlung in Silizium bei einer Wellenlänge von 800 nm ca. 10 µm, während sie bei einer Wellenlänge von 500 nm, was einer Strahlung im blaugrünen Spektralbereich entspricht, nur noch ca. 1 µm groß ist. Dies bedeutet, daß in Dünnfilmphotodioden, besonders bei längerwelliger Strahlung, nur noch ein geringer Teil der einfallenden Strahlung absorbiert und in elektrische Signale umgesetzt wird.

Der Erfindung liegt daher die Aufgabe zugrunde, ein Verfahren zur Herstellung von Dünnfilmphotodioden anzugeben, die gerade bei längerwelliger Strahlung noch einen hohen Wirkungsgrad aufweisen.

Die Aufgabe wird mit dem Verfahren nach Anspruch 1 gelöst. Vorteilhafte Ausgestaltungen des Verfahrens sind Gegenstand der Unteransprüche.

Bei dem erfindungsgemäßen Verfahren werden zunächst ein oder mehrere Photodioden auf bekannte Weise vorzugsweise in einem Standard-Halbleitersubstrat hergestellt, wobei in der Regel ein reiner Photodiodenprozeß verwendet wird. Anschließend wird ein Trägersubstrat mit der Vorderseite des Halbleitersubstrats verbunden, die die Photodioden aufweist. Hierbei ist keine Justage erforderlich. Es genügt vielmehr eine grobe Ausrichtung der beiden Substrate. Nun wird das Halbleitersubstrat von der Rückseite her auf die geforderte Restdicke des Halbleiterbereiches von einigen Mikrometern gedünnt. Anschließend wird die Rückseite mit ei-

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ner oder mehreren Schichten versehen, die die zu detektierende Strahlung reflektieren, vorzugsweise mit einem Reflexionsgrad von mindestens 50%. Diese Schichten können Metalle (z. B. Al, Cu, Mo, Ta, Ti, W), Metallverbindungen (z. B. AlSi, AlSiCu, $MoSi_2$, $TaSi_2$, $TiSi_2$, PtSi, WSi_2) oder dielektrische Schichten wie Oxid oder Nitrid sein, die eine Totalreflexion der zu detektierenden Strahlung an der Grenzfläche zwischen dem Halbleiterbereich und diesen Schichten bewirken.

Vorzugsweise wird vor dem Aufbringen der reflektierenden Schichten die Oberfläche des Halbleiter-Substrates aufgerauht oder angeätzt (z. B. mit KOH), um eine diffuse Reflexion oder eine Änderung des Reflexionswinkels an dieser Fläche zu erzielen.

Wird die Photodiode so ausgelegt, daß sich die Raumladungszone über die gesamte Schichtdicke erstreckt, so tragen die in der gesamten Schichtdicke (optisch aktive Schicht) generierten Ladungsträger zum Photostrom bei. Infolge der Absorption nimmt die Strahlungsintensität exponentiell mit zunehmender Tiefe ab. Bei einer geringen Absorption würde jedoch ein Großteil der Strahlung die optisch aktive Schicht der Photodiode durchdringen und nicht zum Photostrom beitragen. Durch die erfindungsgemäße reflektierende Schicht an der Unterseite der Photodiode wird die Strahlung umgelenkt, durchdringt erneut die optisch aktive Schicht der Photodiode und erzeugt wiederum Ladungsträger. Bei senkrechtem Einfall des Lichtes wird damit mindestens eine Verdoppelung der optisch wirksamen Tiefe erreicht. Durch die oben genannte Behandlung bzw. Strukturierung der Rückseite wird zusätzlich eine Richtungsänderung der Strahlung erreicht, so daß sich die Weglänge nochmals vergrößert. Darüber hinaus tritt auch an der Oberfläche der Photodiode beim Übergang vom optisch dichteren Halbleitermaterial in die Deckschichten, die in der Regel aus Oxid, Nitrid oder organischen Schichten, wie Polyimid, bestehen, eine Totalreflexion auf, so daß insgesamt der Wirkungsgrad von Dünnfilmphotodioden stark erhöht wird. Die erfindungsgemäße Rückseitenverspiegelung muß zur Erhöhung des Wirkungsgrades natürlich nicht unbedingt strukturiert werden.

Nach dem Aufbringen der reflektierenden Schicht bzw. Schichten wird die Photodiode auf ein weiteres Substrat aufgebracht. Nach dem Entfernen des Trägersubstrates werden schließlich die elektrischen Verbindungen hergestellt.

Die Rückseitenverspiegelung gewährleistet außerdem, daß die einfallende Strahlung nicht in darunterliegende Schichten einer vertikalen Integrierten Schaltung eindringt und die Eigenschaften der Schaltung beeinflußt. Eindringende Strahlung würde Ladungsträger erzeugen, die innerhalb einer Schaltung elektrische Ströme hervorrufen, die z. B. als unerwünschte Leckströme die Funktion des Bausteins stören können.

In einer vorteilhaften Ausführungsform wird die Rückseitenverspiegelung mit elektrisch leitenden Schichten realisiert und dient dadurch gleichzeitig als elektromagnetische Abschirmung, so daß ein Übersprechen zwischen den Ebenen verhindert wird.

Durch das erfindungsgemäße Verfahren können Dünnfilm-Photodetektoren geringer Dicke mit hohem Quantenwirkungsgrad hergestellt werden, die sich gut für eine vertikale Integration eignen.

Im folgenden wird die Erfindung anhand der Figuren und eines Ausführungsbeispiels näher erläutert. Hierbei zeigen

Fig. 1 ein Ausgangssubstrat mit einer auf übliche Weise hergestellten Photodiode;

Fig. 2 das gedünnte Ausgangssubstrat mit dem verbundenen Trägersubstrat auf der Vorderseite;

Fig. 3 das Trägersubstrat mit dem gedünnten Ausgangssubstrat nach Herstellung der Rückseitenverspiegelung;

Fig. 3a das Trägersubstrat mit dem gedünnten Ausgangssubstrat mit einer Rückseitenstreuschicht nach Herstellung der Rückseitenverspiegelung;

Fig. 3b das Trägersubstrat mit dem gedünnten Ausgangssubstrat mit lateralen Reflektoren nach Herstellung der Rückseitenverspiegelung; und

Fig. 4 ein Bauelementsubstrat mit vertikal integrierten Dünnfilm-Photodioden gemäß der vorliegenden Erfindung.

Das folgende Ausführungsbeispiel beschreibt die Herstellung einer Dünnfilm-Photodiode.

In einem Ausgangssubstrat **1**, beispielsweise aus monokristallinem Silizium, wird eine Photodiode **8** gemäß einem Standardverfahren der Halbleitertechnologie hergestellt. Solche Standardverfahren sind z. B. aus D. Widmann et al., Technologie hochintegrierter Schaltungen, Springer-Verlag, Berlin 1996, bekannt.

Die Diode besteht aus einem pn-Übergang von der hochdotierten Elektrode **3** zum Substrat **1**. Die Elektrode **3** ist dabei von entgegengesetzter Polarität wie das Substrat, d. h. bei einem n-leitenden Substrat p-dotiert. Das dotierte Gebiet **3** wird durch Ionenimplantation oder Diffusion erzeugt, wobei anschließend eine Temperung zum Eintreiben und/oder Aktivieren der Dotierstoffe folgen kann. Die Isolationsschicht **2**, die in der Regel aus Oxid besteht, kann dabei als Maskierung dienen. Alternativ ist selbstverständlich auch die Verwendung von Photolack zur Maskierung möglich.

Vor der Realisierung der elektrischen Anschlüsse wird eine Isolationsschicht **4** aufgebracht oder erzeugt, die aus undotiertem oder dotiertem Oxid, wie FSG, PSG, BSG oder BPSG, aus Nitrid oder einem Schichtsystem der genannten Materialien bestehen kann. Neben der Isolation gewährleistet diese Schicht auch einen Schutz der Photodiode. Anschließend wird die Metallisierung **5** hergestellt und eine Passivierungsschicht **6**, die beispielsweise aus Oxid und Nitrid besteht, abgeschieden. Das Ergebnis ist in **Fig. 1** dargestellt.

Als Verdrahtung kann auch eine Mehrlagenmetallisierung zum Einsatz kommen. Die Deckschichten über der Photodiode können zur Optimierung der Strahlungseinkopplung in die Photodiode auch teilweise oder vollständig entfernt, bzw. modifiziert werden.

Für eine vertikale Integration muß das Substrat **1** auf eine Restdicke von wenigen Mikrometern, vorzugsweise auf ≤ 5 µm, gedünnt werden. Dazu wird ein Trägersubstrat **10**, das eventuell mit einer Abdeckschicht **11**, aus beispielsweise Oxid, versehen ist, auf das erste Substrat **1** aufgebracht, wie in **Fig. 2** gezeigt. Als Trägersubstrat sind neben mono- oder polykristallinen Siliziumsubstraten auch andere Materialien verwendbar, die zu Halbleiterprozessen kompatibel sind, wie z. B. Quarz- oder Glassubstrate. Um eine gute Verbindung zu erreichen, wird dabei vorzugsweise die Oberfläche des Substrates **1** vorher planarisiert.

Die Planarisierung kann mit verschiedenen Verfahren durchgeführt werden. Dabei wird zuerst eine Isolationsschicht **7**, wie z. B. Spin-on-Glas oder ein CVD-Oxid aufgebracht. Die maximal mögliche Temperatur wird durch das zulässige Temperaturbudget, in der Regel durch die bei der Metallisierung verwendeten Materialien vorgegeben und liegt typischerweise im Bereich von 400°C. Anschließend wird die Oberfläche eingeebnet, was durch Rückätzen, mechanisches und/oder chemomechanisches Schleifen erfolgt. Nun wird auf die Oberfläche des Substrates **1** oder des Trägersubstrates **10** ganzflächig eine Haftschicht **12** aus einem organischen Material, wie Polyimid oder Photolack, aufgebracht. Diese Haftschicht **12** mit einer Dicke von typischerweise 1–2 µm bewirkt außerdem eine Planarisierung der Oberfläche. Auf die Haftschicht **12** wird schließlich das Trä-

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gersubstrat **10** aufgeklebt. Das Trägersubstrat **10** wird als Handlingsubstrat für die weiteren Prozeßschritte verwendet und schützt die Oberfläche des Substrates **1** bei der weiteren Bearbeitung.

Danach wird das Substrat **1**, das die Photodioden enthält, durch Ätzen und/oder Schleifen von der Rückseite her gedünnt, bis die Dicke des Substrates **1** nur noch wenige Mikrometer beträgt.

Dieser Dünnungsprozeß kann dadurch vereinfacht werden, daß als Ausgangsmaterial für das Substrat **1** SOI-Material verwendet wird, welches eine vergrabene Oxidschicht enthält. Dies hat den Vorteil, daß der Dünnungsprozeß so ausgelegt werden kann, daß diese vergrabene Oxidschicht als Ätzstopp dient. Aufgrund der großen Selektivität der Ätzprozesse wird damit eine hohe Homogenität der Dicke des gedünnten Substrates **1** erreicht. Die Enddicke des Substrates **1** wird dabei durch die Dicke der Substratschicht oberhalb des vergrabenen Oxides, das danach entfernt werden kann, bestimmt.

Eine weitere Alternative stellt die Verwendung einer hochdotierten Schicht als Ätzbarriere dar. In diesem Fall wäre die vergrabene Oxidschicht beim SOI-Material im Substrat **1** durch ein hochdotiertes Gebiet ersetzt. Durch den Einsatz von Ätzverfahren, deren Ätzraten stark dotierungsabhängig sind, wird schließlich erreicht, daß die Dünnung des Substrates **1** selbständig an dieser hochdotierten Schicht stoppt.

Nun wird die Rückseite des Substrates **1** gemäß **Fig. 3** mit einer Schicht oder einem Schichtsystem **13** versehen, das die zu detektierende Strahlung reflektiert. Diese Schichten können dabei Metalle (z. B. Al, Cu, Mo, Ta, Ti, W), Metallverbindungen (z. B. AlSi, AlSiCu, $MoSi_2$, $TaSi_2$, $TiSi_2$, PtSi, WSi_2) oder dielektrische Schichten wie Oxid oder Nitrid sein, die eine Totalreflexion der zu detektierenden Strahlung an der Grenzfläche zwischen den Schichten und dem Substrat bewirken. Durch elektrisch leitende Schichten kann außerdem ein Rückseitenkontakt zur Verfügung gestellt werden.

Vorzugsweise wird vor dem Aufbringen der reflektierenden Schichten die Oberfläche des Halbleiter-Substrates aufgerauht oder angeätzt, um eine diffuse Reflexion oder eine Änderung des Reflexionswinkels zu erzielen. Dieses Aufrauhen kann mechanisch und/oder chemisch erfolgen. Bei einer chemischen Behandlung kommen dabei Defektätzen oder Ätzen, deren Ätzrate von der Kristallorientierung abhängt, wie die KOH-Ätze, zur Anwendung. Alternativ oder zusätzlich können auch mit Hilfe einer Rückseitenlithographie, die hierzu keine Justierung erfordert, in Verbindung mit auf die Kristallorientierung sensitiven Ätzverfahren Schrägen bzw. Gräben **14** erzeugt werden. Durch diese Schrägen **14** werden mit der Rückseitenverspiegelung **13** die Richtung des reflektierten Lichtes geändert und damit Vielfachreflexionen im Substrat **1** hervorgerufen (vgl. **Fig. 3a**). Durch diese Maßnahme werden die optisch wirksame Substratdicke vervielfacht und der Wirkungsgrad der Photodiode stark erhöht. Für den Fall, daß die Schrägen **14** den später folgenden Verbindungsprozeß der vertikalen Integration stören, kann die Rückseite nach dem Erzeugen der Rückseitenverspiegelung **13** mit einem der bereits erwähnten Verfahren planarisiert werden.

Durch die Reflexionen kann jedoch auch eine Störung von benachbarten Elementen verursacht werden. Um dies zu verhindern, können zusätzlich Reflektoren **15** im Substrat **1** erzeugt werden, die das gedünnte Substrat **1** vorzugsweise durchdringen und damit einige Mikrometer tief sind (vgl. **Fig. 3b**). Die Reflektoren **15** können aus dielektrischen Schichten wie Oxid oder Nitrid bestehen. Weiterhin sind Schichtsysteme aus den genannten dielektrischen Schichten, polykristallinem Halbleitermaterial, Metallen oder Metallverbindungen möglich. Bei elektrisch leitfähigen Schichten ist dabei in der Regel eine seitliche Isolation zum Substrat **1** erforderlich, die durch dielektrische Schichten sichergestellt wird.

Ein Bauelementsubstrat **20**, welches elektronische Bauelemente **21** enthalten kann, wird als Grundsubstrat für die vertikale Integration verwendet. Nach Planarisierung der Oberfläche des Substrates **20** mit einem der bereits erwähnten Verfahren wird eine Haftschicht **22** aus z. B. Polyimid oder Photolack auf das Substrat **20** oder auf die Rückseite des Substrates **1** aufgebracht. Anschließend wird das Substrat **1**, welches die Photodioden enthält, justiert mit dem Bauelementsubstrat verbunden. Danach werden das Trägersubstrat **10**, die Abdeckschicht **11** und die Haftschicht **12** entfernt. Das resultierende System ist in **Fig. 4** dargestellt.

Das Trägersubstrat **10** und die Abdeckschicht **11** können durch Abätzen oder Abschleifen, die Haftschicht **12** mit einem Sauerstoffplasma oder einem Lösungsmittel abgetragen werden. Die Abdeckschicht **11** kann dabei als Stoppschicht für das Entfernen des Trägersubstrates **10** dienen.

Die Schichten **4**, **6** und **7** stellen gleichzeitig die Deckschichten über der Photodiode dar. Im Zuge einer Optimierung der Strahlungseinkopplung in die Photodiode kann bei Bedarf eine Modifikation dieser Schichten über den Photodioden durchgeführt werden. Dies kann durch ein lokales Dünnen, Entfernen und/oder Abschneiden erfolgen.

Die elektrische Verbindung zwischen den Photodioden und den Bauelementen **21** kann beim Aufbringen des Substrates **1** oder nach Entfernung des Trägersubstrates **10** mit einem bekannten Verfahren hergestellt werden.

Patentansprüche

1. Verfahren zur Herstellung von Dünnfilmphotodioden, mit folgenden Schritten:
   - Bereitstellen eines ersten Substrates (**1**) mit einer Photodiode auf einer ersten Seite;
   - Verbinden des ersten Substrates mit einem zweiten Substrat (**10**), wobei die erste Seite zum zweiten Substrat gerichtet ist;
   - Dünnen des ersten Substrates von einer zweiten, der ersten gegenüberliegenden Seite bis auf eine Dicke von wenigen Mikrometern;
   - Aufbringen einer die zu detektierende Strahlung reflektierende Schicht oder Schichtfolge (**13**) auf die zweite Seite des ersten Substrates;
   - Aufbringen des ersten Substrates auf ein drittes Substrat (**20**), wobei die reflektierende Schicht oder Schichtfolge zum dritten Substrat gerichtet ist; und
   - Entfernen des zweiten Substrates.

2. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß als erstes Substrat (**1**) ein Substrat aus Halbleitermaterial bereitgestellt wird, in dem die Photodiode aus unterschiedlich dotierten Bereichen gebildet ist.

3. Verfahren nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die reflektierende Schicht oder Schichtfolge (**13**) auf der dem ersten Substrat (**1**) zugewandten Seite strukturiert wird.

4. Verfahren nach Anspruch 3, dadurch gekennzeichnet, daß die Strukturierung durch Aufrauhen oder Anätzen der zweiten Seite des ersten Substrates (**1**) vor dem Aufbringen der reflektierenden Schicht oder Schichtfolge (**13**) erfolgt.

5. Verfahren nach Anspruch 3, dadurch gekennzeichnet, daß die Strukturierung durch Ätzen von Gräben (**14**) auf der zweiten Seite des ersten Substrates (**1**) vor

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dem Aufbringen der reflektierenden Schicht oder Schichtfolge (**13**) erfolgt.

6. Verfahren nach einem der Ansprüche 1 bis 5, dadurch gekennzeichnet, daß für die reflektierende Schicht oder Schichtfolge (**13**) elektrisch leitendes Material verwendet wird.

7. Verfahren nach einem der Ansprüche 1 bis 6, dadurch gekennzeichnet, daß das Dünnen des ersten Substrates (**1**) bis auf eine Dicke von maximal 5 Mikrometer erfolgt.

8. Verfahren nach einem der Ansprüche 1 bis 7, dadurch gekennzeichnet, daß als drittes Substrat (**20**) ein Substrat mit elektronischen Bauelementen (**21**) und/oder Metallisierungsebenen eingesetzt wird.

9. Verfahren nach einem der Ansprüche 1 bis 8, dadurch gekennzeichnet, daß auf dem ersten Substrat (**1**) mehrere Photodioden gebildet sind, wobei zwischen den Photodioden Gräben erzeugt und mit einem Material (**15**) zur Reflexion der zu detektierenden Strahlung gefüllt werden.

Hierzu 2 Seite(n) Zeichnungen

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- Leerseite -

Nummer: DE 198 38 439 C1
Int. Cl.[7]: H 01 L 31/102
Veröffentlichungstag: 27. April 2000

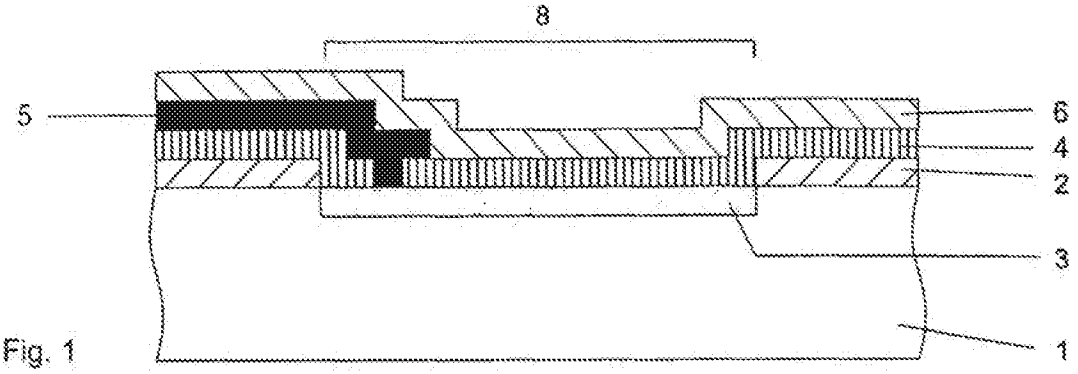

Fig. 1

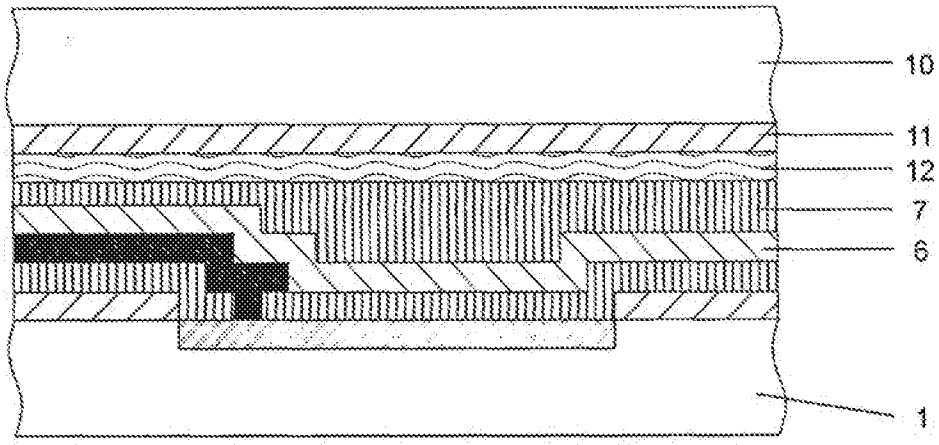

Fig. 2

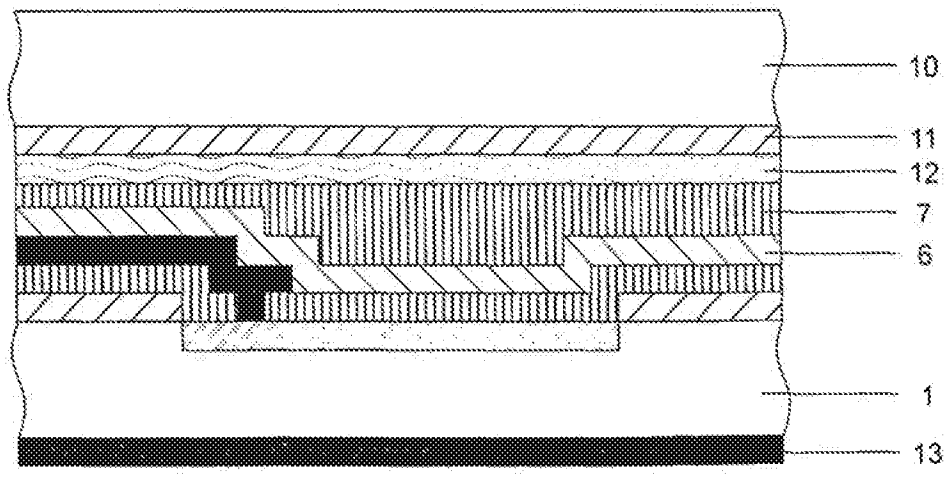

Fig. 3

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Nummer: DE 198 38 439 C1
Int. Cl.[7]: H 01 L 31/102
Veröffentlichungstag: 27. April 2000

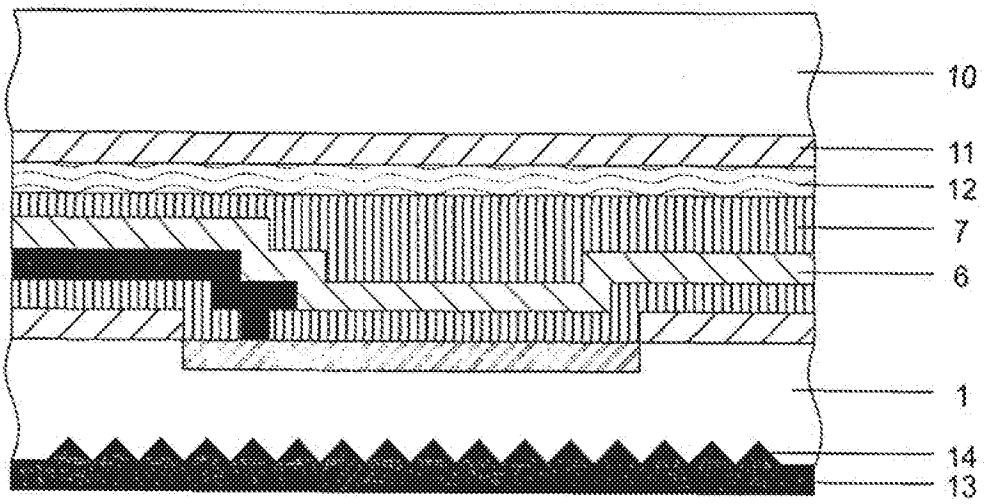

Fig. 3a

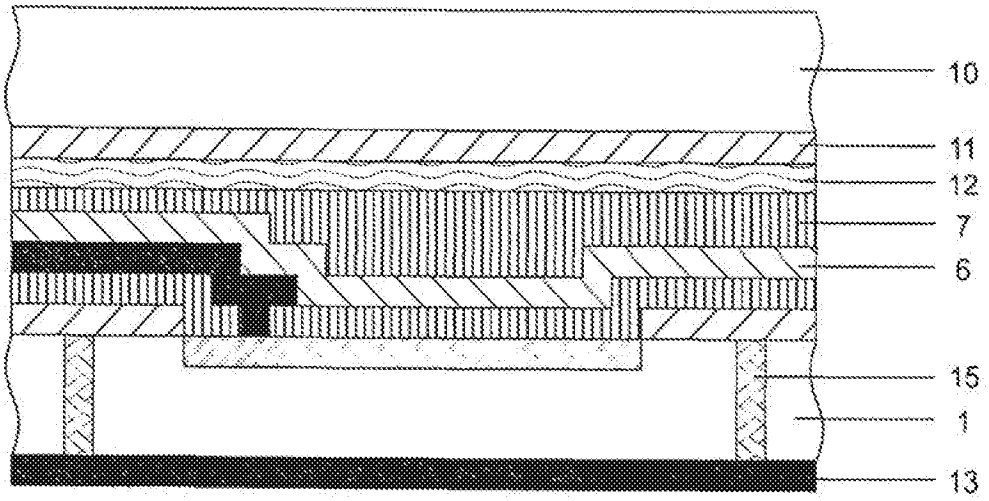

Fig. 3b

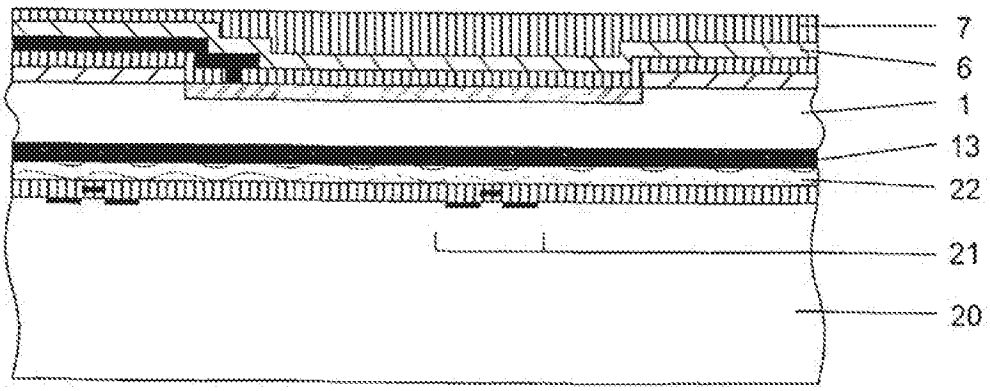

Fig. 4

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(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 2 509 107 A1

(12) EUROPEAN PATENT APPLICATION
published in accordance with Art. 153(4) EPC

(43) Date of publication:
10.10.2012 Bulletin 2012/41

(21) Application number: **10852350.7**

(22) Date of filing: **01.06.2010**

(51) Int Cl.:
H01L 27/146 *(2006.01)*

(86) International application number:
PCT/CN2010/073440

(87) International publication number:
WO 2011/150551 (08.12.2011 Gazette 2011/49)

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO SE SI SK SM TR

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(54) **MULTISPECTRAL PHOTOSENSITIVE DEVICE**

(57) A multi-spectrum photosensitive device comprises two, three, or four composite sensing pixels arranged in layers up and down in a base layer of P-type or N-type silicon by means of single-sided processing or double-sided processing, each composite sensing pixels can sense respectively spectrum orthogonal or complementary to each other in visible light or visible and infrared light. The basic sensing pixels on different layers of the composite sensing pixels can be designed to sense different colors or spectrums, so that a multi-spectrum photosensitive chip can be achieved by repeatedly arranging the macro units consisting of more than one composite sensing pixel. The present disclosure also includes a new multi-layer sensing pixel, and examples of which used in a single-sided double-layer, or a double-sided double-layer, or a double-sided three-layer, or a double-sided four-layer, or a single-sided mixed double-layer, or a double-sided mixed with double-layer or a multi-layer multi-spectrum sensing device. A multi-spectrum photosensitive device according to the present disclosure has the advantage of better color sensing performance, integration of color sensing and infrared sensing, and a simple processing technique.

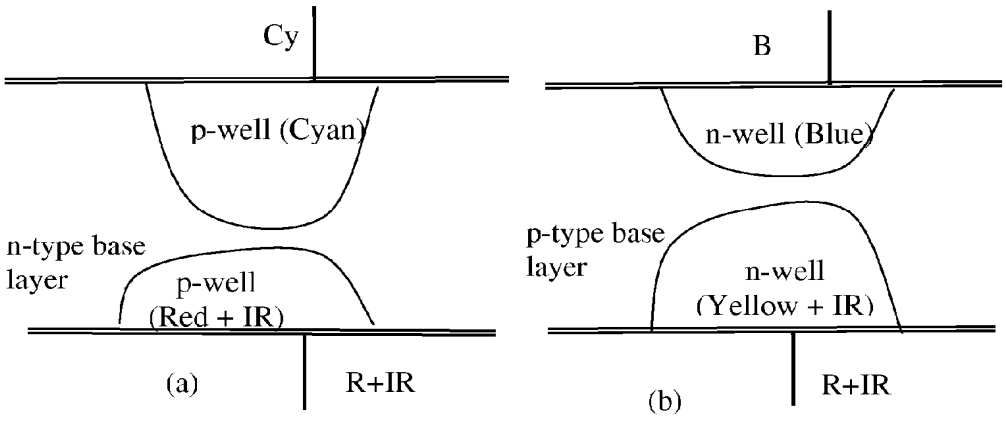

Fig 4

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Description

TECHNICAL FIELD

[0001] The present disclosure relates to a multi-spectrum photosensitive device, in particular, to physical implementation and manufacture thereof. More particularly, the present invention relates to a sensing device for panchromatic images which is achievable by CCD or CMOS semiconductor for simultaneously sensing several spectra (such as visible light and infrared). Herein, the panchromatic spectrum (or color) comprises the entire spectra of interest. For normal sensing devices (e.g., those for visible light), the panchromatic refers to the entire spectra of visible light that contains red, green, blue and white. For sensing devices used for a combination of infrared and visible light, the panchromatic refers to spectra of the visible light and infrared. The present disclosure applies to multi-spectrum sensing device for sensing infrared, monochrome and color images.

BACKGROUND ART

[0002] The present disclosure is a continuation of earlier applications titled "Multi-spectrum Photosensitive Device and Manufacturing Methods Thereof" (PCT/CN2007/071262) and "Multi-spectrum Photosensitive Device and Manufacturing Method Thereof" (Chinese Application No. 200810217270.2) owned by the present inventor, and aims to provide more specific and preferred semiconductor physical implementations.

[0003] The previous sensing devices focus on sensing either color visible light or infrared light, few of them sense both of color visible light and infrared light. Although there are other inventions or applications, such as using indium antimony semiconductor technology ("Silicon infrared focal plane arrays", M. Kimata, in Handbook of Infrared Detection Technologies, edited by M. Henini and M. Razeghi, pp.352-392, Elsevier Science Ltd., 2002), to simultaneously realize photosensitivity of visible light and infrared light, they do not sense color of light. The existing method of simultaneously obtaining the color and infrared light is to physically superpose a color sensing device with an infrared sensing device (such as "Backside-hybrid Photo detector for trans-chip detection of NIR light", by T. Tokudaetal., in IEEE Workshop on Charge-coupled Devices & Advanced Image Sensors, Elmau, Germany, May 2003, and "A CMOS image sensor with eye-safe detection function using backside carrier injection", T. Tokudaetal., J. Inst. Image Information & Television Eng., 60(3):366-372, March 2006).

[0004] There are three main reasons for failure of the existing sensing device in integrating the color sensing device with infrared sensing device. The first reason is that the existing color sensing device needs to use color filter film (including red / green / blue, or cyan /yellow / magenta / green) to get the color. However, these filter films also have a strong filtering characteristic on the infrared light. In addition, in order to make color vivid, an infrared filter is added to the lens specifically to reduce the possible fogging phenomenon caused by infrared light on color image. Foveon Company's X3 three-layer sensing technology achieves the selection of color according to the depth. Though this method does not use the filter film, the manufacture of the three-layer sensing technology has been very difficult and industrialization is not very successful. If an infrared layer is further added below the three layers, it will be more complicated and there is almost no practical value. The second reason is that silicon that is widely used in semiconductors absorbs the infrared with wavelength only below 1100 nm. Therefore, many infrared sensing devices utilize other semiconductor materials, such as germanium, silicon-germanium mixed crystals, HgCdTe, InSb and the like. These materials are not suitable for sensing visible light. The third reason is due to lack of practicable technology for manufacturing double-layer or multi-layer sensing device.

[0005] Therefore, some problems, such as how to achieve better photosensitivity and integrate the color sensing device with infrared sensing device, needs to be further invented and improved.

SUMMARY

TECHNICAL PROBLEM

[0006] Based on the above description, the present disclosure provides a multi-spectrum sensing device, which not only achieves color photosensitivity better, but also provides an implementation for integrating a color sensing device with an infrared sensing device.

TECHNICAL SOLUTION

[0007] The technical solution according to the present invention includes:

[0008] A multi-spectrum photosensitive device, comprising a base layer, wherein a plurality of composite sensing pixel macro units is repeatedly arranged in accordance with a preset pattern on the base layer, the composite sensing pixel macro unit comprises at least one composite sensing pixel comprising at least two basic sensing pixels, the basic sensing pixels are arranged in layers along a direction of light irradiation, each layer having one basic sensing pixel, and the basic sensing pixels are distributed at the top side, or bottom side, or top side and bottom side of the base layer in a manner of each side with at most two layers.

[0009] In an example of the multi-spectrum photosensitive device, the composite sensing pixel includes two basic sensing pixels, which are arranged in two layers at the top side or bottom side of the base layer to form a single-side double-layer composite sensing pixel, or are disposed respectively at the top side and bottom side of the base layer to form a double-sided double-layer com-

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posite sensing pixel.

[0010] In the multi-spectrum photosensitive device, the composite sensing pixel in the base layer may be a single-sided double-layer composite sensing pixel, so that the multi-spectrum sensing device constitutes a single-sided double-layer sensing device.

[0011] The single-sided double-layer composite sensing pixel may be formed by a composite N-P-N junction which is formed by doping P-type impurity on a base layer of N-type silicon to make a P-doped layer, then doping N-type impurity on P-doped layer.

[0012] The single-sided double-layer composite sensing pixel could be formed by a composite P-N-P junction, which is formed by doping N-type impurity on a base layer of P-type silicon to make an N-doped layer, then doping P-type impurity on the N-doped layer.

[0013] In the multi-spectrum photosensitive device, the composite sensing pixel in the base layer may be a double-sided double-layer composite sensing pixel, so that the multi-spectrum sensing device constitutes a double-sided double-layer sensing device.

[0014] The double-sided double-layer composite sensing pixel may be formed by a composite P-N-P junction which is formed by doping P-type impurity on both top side and bottom side of a base layer of N-type silicon.

[0015] The double-sided double-layer composite sensing pixel may be formed by a composite N-P-N junction which is obtained by doping N-type impurity on both top side and bottom side of a base layer of P-type silicon.

[0016] In an example of the multi-spectrum photosensitive device, the composite sensing pixel includes three or four basic sensing pixels, two of which are disposed in two layers at top side or bottom side of the base layer, and the remain basic sensing pixel(s) are disposed in one or two layers at bottom side or top side of the base layer, so as to form a double-sided multi-layer composite sensing pixel.

[0017] In the multi-spectrum photosensitive device, a composite sensing pixel in the base layer may be a double-sided multi-layer composite sensing pixel, so that the multi-spectrum sensing device constitutes a double-sided multi-layer sensing device.

[0018] The double-sided multi-layer composite sensing pixel may be formed by a composite junction of P-N-P, or N-P-N-P, or P-N-P-N, or N-P-N-P-N, wherein the composite junction is made by doping P-type impurity on both top side and bottom side of a base layer of N-type silicon to make a P-doped layer, and then doping N-type impurity on the P-doped layer.

[0019] The double-sided multi-layer composite sensing pixel may be formed by a composite junction of N-P-N, N-P-N-P, P-N-P-N or P-N-P-N-P, wherein the composite junction is made by doping N-type impurity on both top side and bottom side of a base layer of P-type silicon to make an N-doped layer, and then doping P-type impurity on the N-doped layer.

[0020] In the multi-spectrum photosensitive device, the basic sensing pixels in the composite sensing pixel respectively senses one of two spectrum bands of visible light or visible and infrared light orthogonal to each other, the combination of spectra sensed by all the composite sensing pixels in the composite sensing pixels macro units contains spectral information indispensable for color reconstruction within the color space of RGB or CMYK.

[0021] In the multi-spectrum photosensitive device, the spectrum sensed by the basic sensing pixels of the composite sensing pixels closest to the light source includes blank color, blue, green, cyan, white, and white plus infrared.

[0022] In the multi-spectrum photosensitive device, the spectrum sensed by basic sensing pixels of the composite sensing pixels farthest away from the light source includes blank color, green, red, yellow, white, red plus infrared, yellow plus infrared, and white plus infrared.

[0023] In the multi-spectrum photosensitive device, the bottom surface of the basic sensing pixel sensing infrared light in the bottom layer of the composite sensing pixel units is grown with silicon germanium crystal layer or germanium crystal layer for absorbing infrared light better.

[0024] In the multi-spectrum photosensitive device, the bottom of the basic sensing pixels for sensing infrared light is coated with a mirror reflection film.

[0025] In the multi-spectrum photosensitive device, the composite sensing pixel is sampled in an active manner to form an active pixel.

[0026] In the multi-spectrum photosensitive device, the composite sensing pixel is sampled in a passive manner to form a passive pixel.

[0027] In the multi-spectrum photosensitive device, the basic sensing pixel in the composite sensing pixels is a photo diode or a photo gate.

[0028] In the multi-spectrum photosensitive device, sensing mode of the multi-spectrum sensing device comprises front side sensing, back side sensing, or double-direction sensing mode, the double-direction sensing mode includes direction-selected-by-time-sharing mode, direction-selected-by-area-division mode, or direction-selected-by-pixel mode.

[0029] In the multi-spectrum photosensitive device, the preset pattern includes repeated ordering, rectangular pattern, or honeycomb pattern adopted by the composite pixels.

BENEFICIAL EFFECT

[0030] The beneficial technical effects of the present disclosure are designed to:

[0031] 1. A better color sensing performance is provided and a color sensing device is integrated with an infrared sensing device. In the present disclosure, at least two sensing pixel layers are provided in a direction of the light source irradiation in the form of composite sensing pixel containing at least two basic sensing pixels, the basic sensing pixels senses each spectral band of the

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spectrum at various layers, so that it is implemented that at least two spectral bands can be sensed at the same pixel position of one surface of the base layer but at different depths, so as to provide a better flexibility and a more pixel disposition on pattern arrangement of composite sensing pixel macro unit of the surface thereon, so that the sensibility, resolution and dynamic scope of the sensing device are greatly enhanced. On the other hand, when two sensing pixel layers are disposed as one sensing visible light and the other sensing infrared light, the integration of visible light device and infrared light device is realizable easily to sense color light and infrared light simultaneously.

[0032] 2. The processing technique implementing products is simple. By adopting existing CCD or CMOS sensing chip processing techniques and equipment, the present disclosure could easily manufacture a single-sided double-layer multi-spectrum sensing device, double-sided double-layer multi-spectrum sensing device and double-sided multi-spectrum sensing device for front side sensing, back side sensing or double-direction sensing. For the Foveon company's three-layer sensing device mentioned above, in order to carry out color sensing, it is necessary to dispose three layers at the same position to respectively sense three RGB colors so as to carry out color reconstruction. However, such method is difficult in processing three layers, and obviously makes wiring between transistors difficult, since connectors for different layers need to be separated from each other. Based on that, it is almost impossible for adding one more layer to the three RGB layers to perform infrared sensing. While the present disclosure carries out color reconstruction with pixel arranged in a pattern on the surface, so that it is unnecessary to dispose three layers in the direction of depth to implement color reconstruction, hence better color sensing performance is realized in the manner of dispose only two layers of basic sensing pixels on the same one surface. Since only two sensing pixel layers at most are disposed on the same surface, the difficulty of three-dimensional processing techniques is distinctly decreased, and wiring is relatively easy. Especially when a double-sided double-layer method is utilized, i.e. two basic sensing pixels in the composite sensing pixels are respectively disposed on two opposite sides, not only the single side double-layer method has better color sensing performance, but also each side processing is simplified as planar processing, that is, one sensing pixel layer is plane-processed on one side, then the base layer is turned over and the other sensing pixel layer is again plane-processed, so that the processing technique of double-sided double-layer sensing device is similar to that of current single-sided single-layer sensing device.

[0033] 3. Because the sensing device of the present disclosure carries out color reconstruction by combining depth spectrum filter and plane pattern arrangement, on one hand, it is unnecessary to adopt a color film, which greatly enhances production yield. On the other hand, redundant color information may be obtained so that many bad spots and dead spots could be compensated by background processing and the use of redundant color information. Accordingly, the fault occurrence ratio of the sensing device is decreased overall.

[0034] A plurality of the double-layer and multi-layer multi-spectrum sensing device suitable for sensing visible and infrared light according to embodiments of the present disclosure will be discussed, which are exemplary only for demonstrating the present disclosure, and are not intended to limit the protection scope of the present disclosure.

[0035] For those skilled in the art, the above and other purposes as well as advantages of the present disclosure will be apparent from the detailed description and illustration of preferred embodiments with reference to the drawings as shown below.

[0036] For the sake of simplicity, the following descriptions of drawings are mainly based on photo diode. However, almost all the examples may also use photo gate instead.

DESCRIPTIONS OF THE DRAWINGS

[0037] Figure 1 is a schematic diagram of traditional single-layer photo diode.

[0038] Figure 2 is a schematic diagram of a three-layer composite photo diode invented by Foveon Company, in which the diode at top layer senses blue, the diode at middle layer senses green, and the diode at bottom layer senses red. This manner makes full use of the relationship between light penetration depth and wavelength. From this figure we can imagine the difficulties of such kind of sensing device on pixel reading, for example, for the pixels of three distinct colors, the reading circuit will occupy a large space and the wiring will be difficult.

[0039] Figures 3 (a) and Figures 3 (b) are schematic diagrams of double-layer multi-spectrum sensing devices according to the present disclosure respectively. Figure 3(a) is suitable for illustrating a single-sided double-layer sensing device, and Figure 3(b) is suitable for illustrating a double-sided double-layer sensing device. The depths of T_1, T_2, T_3, and T_4 are determined in accordance with the relationship curve between incident depth and wavelength of light in the base material (silicon) (Gerald C. Holst and Terrance S. Lomheim, "CMOS/CCD Sensors and Camera Systems", JCD Publishing, pp. 125-125, ISBN 9780819467300, 2007). For example, if the photo diode at top layer is intended to sense blue (or cyan), T_1 should be chosen as about 1.5um (or about 4.5um); and if the bottom layer is intended to obtain red, T_2 and T_4 should be at least 8um, and T_3 should be at least 4.5um. If the photo diode at bottom layer is intended to obtain blue yellow, T_2 and T_4 should be at least 8um, and T_3 should be at least 1.5um. The photo diode at top layer and the bottom layer form a composite diode pair (composite sensing pixels). When the light is irradiated from the top, the photo diode at top layer is closer to the light source. When the light is irradiated from the bottom,

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the photo diode at bottom layer is closer to the light source.

[0040] Figure 4 (a) and Figure 4 (b) show a composite photo diode pair (composite sensing pixels) for sensing both the visible light and the infrared light simultaneously. In order to receive infrared light, the thickness of silicon substrate (T2 and T4 in Figure 3) can be thicker.

[0041] Figure 5 (a) and Figure 5 (b) are the situation of the composite photo diode pair in a single-layer sensing device being irradiated from the back side, in which the photo diode in Figure 5 (a) only senses visible light, and the photo diode in Figure 5 (b) senses both visible light and infrared light. In order to make the two composite photo diodes have a basically same thickness, germanium or silicon germanium crystal (SiGe), which can absorb infrared light better, can be grown at the back of the photo diode sensing the infrared light.

[0042] Figure 6 (a) and Figure 6 (b) are the situation of composite photo diode pair in a double-sided double-layer sensing device being irradiated from the front side, in which the photo diode in Figure 6 (a) only senses visible light, and the photo diode in Figure 6 (b) senses both visible light and infrared light. Similarly, in order to make the two composite photo diodes have a basically same thickness, germanium or silicon germanium crystal (SiGe), which can absorb infrared light better, can be grown at the back of the photo diode sensing the infrared light.

[0043] Figure 7 shows the situation of a composite photo diode in Figure 3 (a) with reading means. Due to the difficulty of wiring and sharing reading circuit, the single-sided double-layer sensing device is more suitably implemented with passive pixel (without FD and amplifying circuit).

[0044] Figure 8 shows the situation of composite photo diode in Figure 3 (b) with reading means. In contrast, when disposing reading circuit, the double-sided double-layer sensing device is easier and more flexible than the single-layer sensing device. Therefore, the double-sided double-layer sensing device can be achieved by either passive pixel, or active pixel. Furthermore, if it is achieved by active pixel, each pixel can be read with using only an average of 1.5 gates (utilizing 3T reading circuit), or 1.75 gates (utilizing 4T reading circuit).

[0045] Figure 9 shows a currently good reading circuit for a 4T active sensing pixel shared by 4-point, wherein one pixel utilizes 1.75 gates on average. We use it to explain that the double-layer or multi-layer sensing device according to the present disclosure could utilize the current standard reading and sampling circuit.

[0046] Figure 10 shows an example of a double-sided three-layer sensing device obtained by simply and directly applying a single-sided double-layer sensing device to bidirectional sensing, wherein the front side in Figure 10 (a) has one layer and the back side therein has two layers, while the front side in Figure 10 (b) has two layers and the back side therein has one layer. Such a sensing device with also three layers is easier and has more variations than Foveon Company's X3 three-layer sensing device. Take note to the difference between Figure 10 and Figure 2. The sensing pixels sensing three colors in Figure 2 are crowded on one side, while in Figure 10, there are only two pixels on one side and another pixel on the other side.

[0047] Figure 11 shows a double-sided four-layer sensing device generated by combining a single-sided double-layer sensing device and double-sided sensing mode. By using such a sensing device, four colors of blue, green, red and infrared may be sensed by one pixel. Although there are more colors and more layers, the manufacturing of the sensing device is much easier than that of Foveon Company's X3 three-layer sensing device.

[0048] Figure 12 shows examples of a double-sided multi-layer sensing device with mixing three layers and four layers.

[0049] Figure 13 shows examples of a double-sided multi-layer sensing device with mixing two layers and four layers.

[0050] Figure 14 shows examples of a double-sided multi-layer sensing device with mixing two layers and three layers.

[0051] Figure 15 and Figure 16 show examples of single-sided or double-sided double-layer sensing device with mixing two layers and one layer.

[0052] We see a degenerative case of a multi-layer composite sensing pixel in Figures 12-16: if one of the N-layer composite sensing pixels is a blank pixel, N-layer composite sensing pixels are degenerated to (N-1)-layer composite sensing pixels. Some double-layer sensing pixels degenerated to a single layer are shown in Figures 15 and 16. If two of the N-layer composite sensing pixels are blank pixels, N-layer composite sensing pixels are degenerated to (N-2)-layer composite sensing pixels, and so forth.

[0053] When the number of layers in the composite pixel is inconsistent, some of the layers may be treated as containing blank pixels (sensing blank color). Therefore, a mixed multi-layer sensing device is a specific case of a multi-layer sensing device, i.e. some of the composite pixels contain blank pixels.

[0054] These examples sufficiently demonstrate the capacity of a single-side double-layer sensing device and a double-sided double-layer or multi-layer sensing device. A series of new colorful sensing device with high performance is generated by combining the technologies of the two devices. It is specifically noted that, in a sensing device with more than three layers, the spectrum sensed by a photo diode positioned in each layer must be orthogonal to each other (that is, there is no common or overlapped portion, theoretically).

[0055] Figure 17 (a) and Figure 17 (b) shows a top view of a double-sided double-layer sensing device with rectangular pattern and honeycomb pattern, wherein FD is a reading capacitor shared by the upper layer and the lower layer. Of course, if needed, the upper layer and the lower layer could utilize a reading capacitor, respectively,

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even if using a group of reading capacitors, respectively.

[0056] Figure 18 (a) shows a top view of a double-sided double-layer multi-spectrum (sensing color plus infrared) sensing device with rectangular pattern, wherein FD is a reading capacitor shared by the upper layer and the lower layer. Figure 18 (b) shows a top view of a double-sided double-layer multi-spectrum (sensing color plus infrared) sensing device with rectangular pattern, wherein FD is a reading capacitor sharing the upper layer and the lower layer. Such kind of macro-pixel unit consisted of two composite pixels could also utilize active sensing pixels with 4-point sharing reading circuit as shown in Figure 9. Different from the single-side single-layer sensing device, the device in Figure 18 (a) adopts four sensing diodes sharing a reading circuit disposed on two sides.

[0057] Figure 19 shows a cross sectional view of 8-point or 4-point sharing reading circuit of a double-sided double-layer multi-spectrum (color plus infrared) sensing device (omitting 3T or 4T reading circuit). Here is an extreme case of FD which connects the upper layer and the lower layer. For a double-sided double-layer multi-spectrum (color plus infrared) sensing device, even if a 4-point sharing reading circuit also has two choices: one is that the 4 points are on the same surface, the other is that the 4 points are on different surfaces. In this diagram, we use another method to improve the absorbing efficiency of infrared light, i.e., mirror reflection materials (such as aluminum, silver or other reflection materials well matched with germanium or silicon) are coated at the back of the germanium layer and the silicon-germanium layer.

[0058] Figure 20 shows a cross section view of an 8-point or 4-point sharing reading circuit of the double-sided double-layer multi-spectrum (color plus infrared) sensing device (omitting 3T or 4T reading circuit). Here is a simpler case of FD not connecting upper layer and lower layer. When FD is not connecting the upper layer and lower layer, the top side or the bottom side of the double-sided double-layer multi-spectrum sensing device is the same as that of the single-sided single-layer sensing device.

[0059] Figure 21 shows a simple situation of producing the double-sided double-layer sensing device. When the base layer is opaque, the upper layer and lower layer can be achieved by a simple method of repeating the processing of the single-sided single-layer sensing device twice. The devices on both sides of the device can also be completely independent. This is a most simple method to achieve a double-direction sensing device.

[0060] Figure 22 (a) and Figure 22 (b) show a situation of a single-sided double-layer sensing devices being used for front side sensing and back side sensing, respectively. It is noted that, in the double-layer photo diode pairs, the photo diode closer to the light source will obtain color with shorter wavelength.

[0061] Figure 23 (a) and Figure 23 (b) show a situation of a double-sided double-layer sensing devices being used for front side sensing and back side sensing, respectively. It is noted that, when the direction of light source is changed, the color sensed by the double-layer photo diode pairs will changed, too. Generally, for two-way symmetrical double-sided double-layer sensing devices (referring to Chinese Application No. 200810217270.2, titled "Multi-spectrum sensing device and manufacturing method thereof"), when the direction of light source changes is changed, cyan and yellow will be exchanged, and blue and red will be exchanged, while green remains the same.

[0062] Figure 24 (a) and Figure 24 (b) show a situation of the front side and back side of a double-sided double-layer sensing device, in which macro pixel comprises three composite photo diodes (composite sensing pixels). When the macro pixel comprises three pixels, the three pixels are usually arranged in honeycomb pattern.

[0063] Figure 25, Figure 26, and Figure 27 are other possible implementations of a double-sided double-layer sensing device. These figures fully show the features of flexibility and diversity of a double-sided double-layer device. After a reasonable change, the discussions with respect to composite diodes in figures 3-16 are also applicable to the situation of figures 22-27. The small numbers of figures are just used to illustrate the principle, rather than limiting the essence and scope of the present disclosure.

[0064] Figure 28 is a principle schematic diagram of a photo gate. In the above illustration, if photo diode used as a basic sensing pixel is replaced by a photo gate, many completely similar implementations and conclusions can be obtained.

DETAILED DESCRIPTION

[0065] In order to facilitate describing the disclosure and explaining differences between the invention and existing technology, the following definition of the terms are provided: double-layer sensing device, multi-layer sensing device, double-sided sensing device, double-direction sensing device. The double-layer sensing device means that sensing pixels thereof are physically divided into two layers, each of which contains sensing pixels for sensing specific spectrum. The multi-layer sensing device refers to a sensing device with more than two layers, such as Foveon Company's X3 sensing device. The double-sided sensing device refers to a sensing device with two sensing surfaces, each of which can sense light from at least one direction. The bidirectional sensing device means that the sensing device can sense light from two directions (which usually form an angle of 180 degrees), i.e., both the front side and the back side of the sensing device can sense light.

[0066] A sensing device can simultaneously have one, two, or all of the following three characteristics: double-layer or multi-layer, double-sided, and double-direction. This disclosure mainly relates to a single-sided double-layer sensing device (as shown in Figure 22(a) and Figure 22(b)), a double-sided double-layer sensing device

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(as shown in Figure 23(a) and Figure 23(b)), and a double-sided multi-layer sensing device (as shown in Figures 10-14). Irrespective of a single-sided double-layer sensing device or a double-sided double-layer sensing device or a multi-layer sensing device, all of them can be used in front side sensing (as shown in Figure 22(a)), back side sensing (as shown in Figure 22(b)), or double-direction sensing (as shown in Figure 21 or Figure 23). However, designs of the sensing devices are different under different irradiation.

[0067] A multi-spectrum photosensitive device according to an embodiment of the present disclosure comprises a base layer, wherein a plural of composite sensing pixel macro units is repeatedly arranged in accordance with a preset pattern on the base layer, the composite sensing pixel macro unit comprises at least one composite sensing pixel consisting of at least two basic sensing pixels, the basic sensing pixels are arranged in layers along a direction of light irradiation, each layer having one basic sensing pixel, and the basic sensing pixels are distributed at the top side, or bottom side, or top side and bottom side of the base layer in a manner of single side with at most two layers. It is noted that, herein the terms "top side" and "bottom side" are just used to express the relative position of two sides of the base layers, rather than limiting the absolute physical location of the surfaces of the base layer. In the following description, to convey a similar definition, the positions with respect to the position of light source are also used to describe the terms "the obverse" (the front side) and "the reverse" (the back side) of the base layer.

[0068] Herein three terms are given: composite sensing pixel macro unit, composite sensing pixel, and basic sensing pixel. The basic sensing pixel is a sensing pixel on a layer and can not be divided. The composite sensing pixel is a combination of at least two basic sensing pixels. The basic sensing pixels in the composite sensing pixel are arranged in layers along a direction of light irradiation, and each layer is provided with one basic sensing pixel (the layer herein is called a sensing-pixel layer). As described in the aforementioned description of drawings, the basic sensing pixel can be a photo diode or a photo gate. When the basic sensing pixel is a photo diode, the composite sensing pixel is in a form of a composite sensing diode pair. Of course, it is noted that, each sensing-pixel layer in a composite sensing pixel is arranged along a direction of light irradiation (which is usually the normal direction of the sensing surface of the base layer), rather than limiting to just be arranged on a side of the base layer. Between the two opposite sides of the base layer irradiated by a light source, if taking the side closer to the light source as front side of the base layer and taking the side far away from the light source as back side of the base layer, each sensing-pixel layer in a composite sensing pixel can be arranged on front side of the base layer, or on back side of the base layer, or on both front side and back side of the base layer, but there are at most two layers of sensing pixels on each side. The relationship between the arrangement and quantity of the sensing-pixel layers can be summarized that, for a direction of a light source, the arrangement of the sensing-pixel layer may be [2,0], [0,2] (i.e., single-sided double-layer), or [1,1] (i.e., double-sided double-layer), or [1,2],[2,1] (i.e., double-sided multi-layer), wherein the first number in an array is the number of sensing-pixel layers arranged on front side of the base layer in the composite sensing pixel, and the second number is the number of the sensing-pixel layer arranged on back side of the base layer in the composite sensing pixel. The composite sensing pixel macro unit, also known as a macro-pixel, is a collection of the minimum number of composite sensing pixels, from which color reconstruction can be performed. A composite sensing pixel macro unit is repeatedly arranged in accordance with a preset pattern (such as square or honeycomb pattern, or repeated ordering), so that the color can be reconstructed throughout the image plane. For the double-layer multi-spectrum sensing device, the composite sensing pixel macro unit usually comprises at least two composite pixels. However, for a two-sided multi-layer multi-spectrum sensing device, the composite sensing pixel macro unit may be one composite pixel.

[0069] Since a composite pixel may be in various types, and a plurality of composite sensing pixels arranged on the base layer may be of different types, the sensing device according to the present disclosure may have a variety of flexible forms. For a composite sensing pixel, according to the number and distribution of the basic sensing pixel therein, the composite sensing pixel may be a single-sided double-layer composite sensing pixel, a double-sided double-layer composite sensing pixel, and a double-sided multi-layer composite sensing pixel. As mentioned above, in a single-sided double-layer composite sensing pixel or a double-sided double-layer composite sensing pixel, there are two basic sensing pixels, but the distribution therein are different. The basic sensing pixels in a single-sided double-layer composite sensing pixel are arranged in layers on one side of the base layer, while the basic sensing pixels of a double-sided double-layer composite sensing pixel are arranged on two sides of the base layer. For a double-sided multi-layer composite sensing pixel, there are three or four basic sensing pixels. Since at most two sensing-pixel layers are arranged on one side of the base layer, the basic sensing pixels therein must be arranged on two sides of the base layer, at least one side is provided with two basic sensing pixels arranged in layers. It is noted that, in a special case, the composite sensing pixel may comprise a blank pixel, in other words, the pixel is used for sensing blank color. In that case, if a basic sensing pixel in a single-sided double-layer composite sensing pixel is a blank pixel, the single-sided double-layer composite sensing pixel is equivalent to a single-sided single-layer composite sensing pixel from the perspective of sensing effectiveness.

[0070] Due to the various types, the arrangement of

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pixels in a composite sensing pixel is quite flexible. For example, if a single-sided double-layer composite sensing pixel is arranged at a certain position on the base layer, a double-sided double-layer composite sensing pixel may be arranged at a position adjacent to the said certain position, and the double-sided multi-layer composite sensing pixels may be arranged at another position adjacent to the said certain position. In short, different types of composite sensing pixels can be arranged at different positions on the base layer. In particular, according to this feature, when all the composite sensing pixels on the base layer in a sensing device are of the identical type, the sensing device is defined according to the type of the composite sensing pixels. For example, when all the composite sensing pixels of the base layer are the single-sided double-layer composite sensing pixels, the corresponding sensing device is regarded as a single-sided double-layer sensing device, and the sensing devices adopting the other two afore-mentioned composite sensing pixels are regarded as a double-sided double-layer sensing device or a double-sided multi-layer sensing device, respectively. It is noted that, as mentioned above, the composite sensing pixel may contain a blank pixel, thus the composite sensing pixel at a position of the base layer may be degenerated. For example, in a single-sided double-layer sensing device, if a composite sensing pixel comprises one blank pixel, the single-sided double-layer sensing pixel is actually degenerated as a single-sided single-layer sensing pixel, so that from the viewpoint of the details, a composite sensing pixel of a single-sided double-layer sensing device is not entirely a single-sided double-layer sensing pixel, but in a whole, this sensing device is still classified as a single-sided double-layer sensing device. Particularly, this sensing device can also be referred to as a mixed single-sided double-layer sensing device. Correspondingly, there exist also a mixed double-sided double-layer sensing device and a mixed double-sided multi-layer sensing device.

[0071] The basic sensing pixels of a composite sensing pixel are generally arranged to sense different spectral bands of visible light or visible and infrared light. For example, one of two spectral bands of visible light or visible and infrared light orthogonal to each other can be sensed respectively by two basic sensing pixel of the composite sensing pixel. Different spectral bands may be sensed respectively by the basic sensing pixels of the composite sensing pixel and composite sensing pixels of the composite sensing pixel macro unit, thus the combination of all spectra sensed by all composite sensing pixels of a composite sensing pixel macro unit contains the spectrum indispensable for color reconstruction within the color space of RGB or CMYK.

[0072] The spectra sensed by the basic sensing pixels closest to the light source in a composite sensing pixel includes blank color, blue, green, cyan, white, and white plus infrared. The spectra sensed by the basic sensing pixels farthest away from the light source in the composite sensing pixels includes blank color, green, red, yellow, white, red plus infrared, yellow plus infrared, and white plus infrared.

[0073] Hereto the arrangement of the sensing pixel according to the present disclosure has been described. Hereinafter, the processing implementation of a multi-spectrum sensing device according to the present disclosure will be described.

According to different materials of the base layer, an approach for achieving a single-sided double-layer multi-spectrum sensing device comprises:

[0074] Providing a base layer of N-type silicon crystal (see Figure 5 (a)), i.e. N-Substrate, at a location of a pixel on a side of the N-type base layer, P-type impurity is doped into the base layer at a certain depth from the surface of the location into the interior of the base layer according to the requirement of color depth, so as to form a P-doped layer. The P-doped layer is a sensing layer of a composite sensing pixel, that is, it forms a basic sensing pixel of the composite sensing pixel. Then, an N-type impurity is doped into the P-doped layer at another depth, which forms an N-doped layer within the P-doped layer, that is, it forms another basic sensing pixel in the composite sensing pixel. In the case, this single-sided double-layer composite sensing pixel is formed by a composite P-N-P junction.

[0075] Another approach is to provide a base layer of P-type silicon crystal (see Figure 5 (b)), i.e., P-substrate, at a location of a pixel on a side of the P-type base layer, N-type impurity is doped into the base layer at a certain depth from the surface of the location into the interior of the base layer according to the requirement of color depth, so as to form a N-doped layer. The N-doped layer is a sensing layer of a composite sensing pixel, that is, it forms a basic sensing pixel of the composite sensing pixel. Then, a P-type impurity is doped into the N-doped layer at another depth, which forms a P-doped layer within the N-doped layer, that is, it forms another basic sensing pixel in the composite sensing pixel. In this case, this single-sided double-layer composite sensing pixel is formed by a composite N-P-N junction.

[0076] The production of a composite sensing pixel is described above. For the production of other composite sensing pixels on the sensing side of the base layer, the processing thereof is the same. But the depths doped by impurities are different at different locations of pixels according to the wavelength of color spectrum desired to be sensed by the corresponding pixel.

[0077] An implementation of a double-sided double-layer multi-spectrum sensing device comprises:

[0078] providing a base layer of N-type silicon crystal (see Figure 4 (a)), i.e., N-substrate, classifying the pixels on the front side of the base layer according to the desired color, and doping P impurity with a certain depth according to the requirement of color depth for each type of pixel. Similarly, the pixels on the back side will also be classified according to the desired color, and P impurity with a certain depth is doped according to the require-

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ment of color depth for each type of pixel. The depth of the P impurity doped is determined according to the wavelength of spectrum desired to be sensed.

[0079] Another more advantageous approach is to provide a P-type base layer of silicon crystal (see Figure 4 (b)), i.e., P-substrate, classify the pixels on the front side according to the desired color, and dope N impurity with a certain depth according to the requirement of color depth for each type of pixel. Similarly, the pixels on the back side will also be classified according to the desired color, and N impurity with a certain depth is doped according to the requirement of color depth for each type of pixel. The depth of the N impurity doped is determined according to the wavelength of spectrum desired to be sensed. Since the mobility of N-type is better than that of P-type, the double-sided double-layer composite sensing pixel formed by this N-P-N composite junction is superior to the double-sided double-layer composite sensing pixel formed by the afore-described P-N-P composite junction.

[0080] An implementation of a double-sided multi-layer multi-spectrum sensing device comprises:

[0081] providing a base layer of N-type or P-type silicon crystal (Figure 9-14), making the front side of the base layer as one or two sensing pixel layers in the manner of single-sided double-layer or single-sided, and making the back side as one or two sensing pixel layers in the manner of single-sided double-layer or single-sided. According to the differences between the arrangement of the front side and the back side, a composite junction of a double-sided multi-layer composite sensing pixel comprising N-P-N, P-N-P, N-P-N-P, P-N-P-N, N-P-N-P-N, P-N-P-N-P and the like is formed.

[0082] After obtaining the composite sensing pixel, if it is needed to read the optical signal, a reading circuit and other control circuits are needed. The arrangement of the reading circuit and other control circuits is designed in accordance with passive pixel or active pixel. If it is designed with active pixel, in addition to the photo diode in Figure 3 (a), there will be a reading circuit shown in Figure 7, and many standard timing and control circuits (not shown in figures).

[0083] For the sensing pixel layer used to sense infrared light, germanium or silicon germanium crystal layer may grow on the bottom side of the corresponding position of the sensing pixel layer, that is the bottom side of the sensing pixel layer used to sensing the infrared light, in order to improve the absorption efficiency of the infrared spectrum. In addition, after growing the germanium or silicon germanium crystal layer, a mirror reflection film formed by aluminum, silver or other materials is plated on the bottom of the basic sensing pixel, in order to reflect the unabsorbed infrared photons, which are re-absorbed by infrared sensing pixel layer. The reflected intensity is determined according to the thickness and the absorption rate of the infrared sensing pixel layer, so as to avoid unnecessary interference with other pixels.

[0084] If the multi-spectrum sensing device is used for double-direction sensing, and the direction-selected-by-pixel pattern and the direction-selected-by-area-division pattern described in the patent application titled "Multi-spectrum sensing devices and manufacturing methods thereof" (China Application No. 200810217270.2, i.e., PCT/CN2010/073441) are used, a shading film is coated on some types of pixels or pixel areas of the front side, and on the other types of pixels or pixel areas of the back side.

[0085] In the above-mentioned implementation, we can completely use photo gate to replace photo diode, resulting in obtaining a single-sided double-layer sensing device, a double-sided double-layer sensing device, and a double-sided multi-layer sensing device, which are based on the photo gate.

[0086] Since the single-sided double-layer sensing device, the double-sided double-layer sensing device, and the double-sided multi-layer sensing device according to the present disclosure provide redundant color information, for the application to which the cost and size are critical (such as mobile phone), some composite pixels may contain blank pixel, resulting in a mixed single-sided double-layer sensing device, a mixed double-sided double-layer sensing device, and a mixed double-sided multi-layer sensing device.

[0087] The present disclosure can be produced by both CCD technology and CMOS technology. Since the production of the disclosure may be ultra-high sensitivity, the basic pixel can be read by means of passive pixel, or by means of active pixel. These features make the present disclosure integrated fully with the existing mature semiconductor chip production technology, therefore, the methods or production according to the present disclosure can be widely used. The disclosure dramatically improves the performance and functionality of sensing chip, at the same time, due to the increased product yields, the cost can be reduced or at least not increased.

[0088] By means of arranging optimally the basic sensing pixel in the composite sensing pixel on two depths, and forming various types of the sensing devices, such as single-sided double-layer, double-sided double-layer, and double-sided multi-layer, the present disclosure greatly extends the types of sensing chips, and physically realizes overlap and integration of the infrared sensing and the color sensing on a single chip for the first time.

[0089] In accordance with production methods provided by the present disclosure and natural and minor modifications thereof (such as, adding a filter film), a double-layer or multi-layer composite sensing pixel, which can sense spectrum orthogonal to each other within the space of visible light or visible plus infrared light, such as (blank color, white), (blue, yellow), (blue, green), (green, red), (blue, red), (blue, red + infrared), (blue, yellow + IR), (blank color, white + IR), (white + IR), (blue / green / red / green / yellow / white, infrared) and the like, can be achieved in the form of single-sided double-layer, double-sided double-layer, or double-sided multi-layer.

[0090] By using the aforementioned sensing methods

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such as double-sided, double-direction, double-layer and multi-layer methods, according to the present disclosure, a single sensing device can be used in a double-direction system, for greatly reducing system cost, lowering the size, reducing system complexity, and making it possible for some applications to receive multi-spectrum or multi-direction (or multi-spectrum signals from two directions) in the same system. For example, a capsule-style camera currently used for checking the patient's gastrointestinal system has a camera mounted on just one side thereof. In order to obtain the image of a certain location in the gastrointestinal system, multiple uses may be required, which cause great pain to the patient and the big expenses. For this purpose, it is desired to improve the capture range of a single shot. And if it is necessary to mount a camera on the other side of the capsule-style camera, by using the existing technology, two systems must be mounted in a very small space, which is quite difficult. However, by using the present invention, it just needs to add a lens on the other side, and still only one sensing chip is utilized, leading to smaller space demand and lower economic cost than those of two sets of sensing systems. In addition, the present disclosure can be used to monitor both front and back direction in a monitoring camera. For many 3G mobile phones with both front camera and back camera, the front camera and back camera can be replaced by a bidirectional camera according to the present disclosure, and switching between front sense and back scene can be achieved by electronic or mechanical switches. For some surveillance system of top class hotels, if it is required to monitor scenes at both ends of the corridor, by using the present disclosure, it just needs one monitoring system to complete the necessary monitoring rather than two monitoring systems for monitoring in both directions.

[0091] According to the integration method provided by the present disclosure, color and infrared can be sensed simultaneously in the same device (using CMOS or CCD semiconductor), and color image and infrared image are overlaid in the same space position. This new type of sensing device greatly extends the dynamic range of sensing device, so as to meet the high performance of automotive, security and other fields. Moreover, it will also be used for a small-size color sensing device such as the camera of mobile phones, to significantly improve image quality.

[0092] Although the present disclosure is disclosed through the above-mentioned preferred embodiments, such disclosure should not be considered limitations to the disclosure. For those skilled in the image sensing devices (such as semiconductor image sensor chips), from the disclosure, it is possible to anticipate many variations and extensions of the present disclosure, without departing from the spirit and concept of the invention.

Claims

1. A multi-spectrum photosensitive device, comprising a base layer, wherein a plurality of composite sensing pixel macro units is repeatedly arranged in accordance with a preset pattern on the base layer, the composite sensing pixel macro unit comprises at least one composite sensing pixel comprising at least two basic sensing pixels, the basic sensing pixels in a same composite sensing pixel are arranged in layers along a direction of light irradiation, each layer having one basic sensing pixel, and the basic sensing pixels are distributed at the top side, or bottom side, or top side and bottom side of the base layer, and each side comprises at most two layers.

2. The multi-spectrum photosensitive device according to claim 1, wherein the composite sensing pixel includes two basic sensing pixels which are arranged in two layers at the top side or bottom side of the base layer to form a single-sided double-layer composite sensing pixel, or are disposed respectively at the top side and bottom side of the base layer to form a double-sided double-layer composite sensing pixel.

3. The multi-spectrum photosensitive device according to claim 2, wherein the composite sensing pixel in the base layer is a single-sided double-layer composite sensing pixel, so that the multi-spectrum sensing device constitutes a single-sided double-layer sensing device.

4. The multi-spectrum photosensitive device according to claim 2 or 3, wherein the single-sided double-layer composite sensing pixel is formed by a composite N-P-N junction which is formed by doping P-type impurity on a base layer of an N-type silicon to make a P-doped layer, then doping N-type impurity on P-doped layer.

5. The multi-spectrum photosensitive device according to claim 2 or 3, wherein the single-sided double-layer composite sensing pixel is formed by a composite P-N-P junction which is formed by doping N-type impurity on a base layer of P-type silicon to make an N-doped layer, then doping P-type impurity on the N-doped layer.

6. The multi-spectrum photosensitive device according to claim 2, wherein the composite sensing pixel in the base layer is a double-sided double-layer composite sensing pixel, so that the multi-spectrum sensing device constitutes a double-sided double-layer sensing device.

7. The multi-spectrum photosensitive device according to claim 2 or 6, wherein the double-sided double-

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layer composite sensing pixel is formed by a composite P-N-P junction which is formed by doping P-type impurity on both top side and bottom side of a base layer of N-type silicon.

8. The multi-spectrum photosensitive device according to claim 2 or 6, wherein the double-sided double-layer composite sensing pixel is formed by a composite N-P-N junction which is obtained by doping N-type impurity on both top side and bottom side of a base layer of P-type silicon.

9. The multi-spectrum photosensitive device according to claim 1, wherein the composite sensing pixel includes three or four basic sensing pixels, two of which are disposed in two layers at top side or bottom side of the base layer, and the remain basic sensing pixel(s) are disposed in one or two layers at bottom side or top side of the base layer, so as to form a double-sided multi-layer composite sensing pixel.

10. The multi-spectrum photosensitive device according to claim 9, wherein the composite sensing pixel in the base layer is a double-sided multi-layer composite sensing pixel, so that the multi-spectrum sensing device constitutes a double-sided multi-layer sensing device.

11. The multi-spectrum photosensitive device according to claim 9 or 10, wherein the double-sided multi-layer composite sensing pixel is formed by a composite junction of P-N-P, or N-P-N-P, or P-N-P-N, or N-P-N-P-N, wherein the composite junction is made by doping P-type impurity on both top side and bottom side of a base layer of N-type silicon to make a P-doped layer, then doping N-type impurity on the P-doped layer.

12. The multi-spectrum photosensitive device according to claim 9 or 10, wherein the double-sided multi-layer composite sensing pixel is formed by a composite junction of N-P-N, or N-P-N-P, or P-N-P-N, or P-N-P-N-P, wherein the composite junction is made by doping N-type impurity on both top side and bottom side of a base layer of P-type silicon to make an N-doped layer, then doping P-type impurity on the N-doped layer.

13. The multi-spectrum photosensitive device according to claim 1, wherein the spectral bands sensed by the basic sensing pixels in a same composite sensing pixels respectively are orthogonal to each other, the spectral bands contains spectra of visible light or visible and infrared light, the combination of spectra sensed by all the composite sensing pixels in the composite sensing pixels macro units contains spectral information indispensable for color reconstruction within the color space of RGB or CMYK.

14. The multi-spectrum photosensitive device according to any one of claims 1-13, wherein the spectrum sensed by the basic sensing pixels of the composite sensing pixels closest to the light source includes blank color, blue, green, cyan, white, and white plus infrared.

15. The multi-spectrum photosensitive device according to any one of claims 1-14, wherein the spectrum sensed by the basic sensing pixels of the composite sensing pixels farthest away from the light source includes blank color, green, red, yellow, white, red plus infrared, yellow plus infrared, and white plus infrared.

16. The multi-spectrum photosensitive device according to any one of claims 1-15, wherein the bottom surface of the basic sensing pixel sensing infrared light in the bottom layer of the composite sensing pixel units grows with silicon germanium crystal layer or germanium crystal layer for absorbing infrared light better.

17. The multi-spectrum photosensitive device according to any one of claims 1-16, wherein the bottom of the basic sensing pixels for sensing infrared light is coated with a mirror reflection film.

18. The multi-spectrum photosensitive device according to any one of claims 1-17, wherein the composite sensing pixel is sampled in an active manner to form an active pixel.

19. The multi-spectrum photosensitive device according to any one of claims 1-17, wherein the composite sensing pixel is sampled in a passive manner to form a passive pixel.

20. The multi-spectrum photosensitive device according to any one of claims 1-19, wherein the basic sensing pixel in the composite sensing pixels is a photo diode or a photo gate.

21. The multi-spectrum photosensitive device according to any one of claims 1-20, wherein the sensing mode of the multi-spectrum sensing device comprises front side sensing, back side sensing, or double-direction sensing mode, wherein the double-direction sensing mode includes direction-selected-by-time-sharing mode, direction-selected-by-area-division mode, or direction-selected-by-pixel mode.

22. The multi-spectrum photosensitive device according to any one of claims 1-21, wherein the preset pattern includes repeated ordering, rectangular pattern, or honeycomb pattern adopted by the composite pixels.

SAMSUNG EX. 1002 - 1870/2862

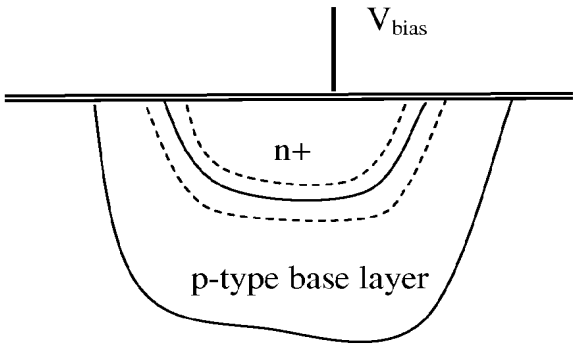

Fig 1

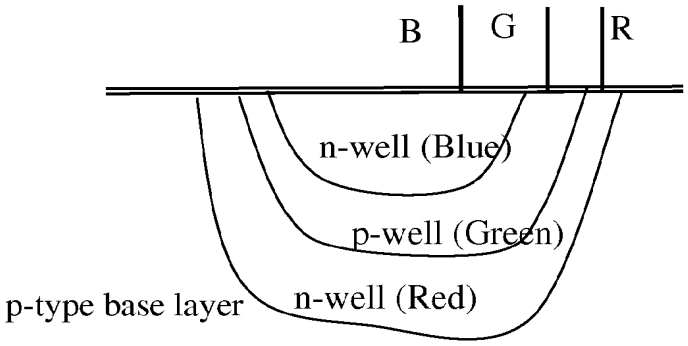

Fig 2

SAMSUNG EX. 1002 - 1871/2862

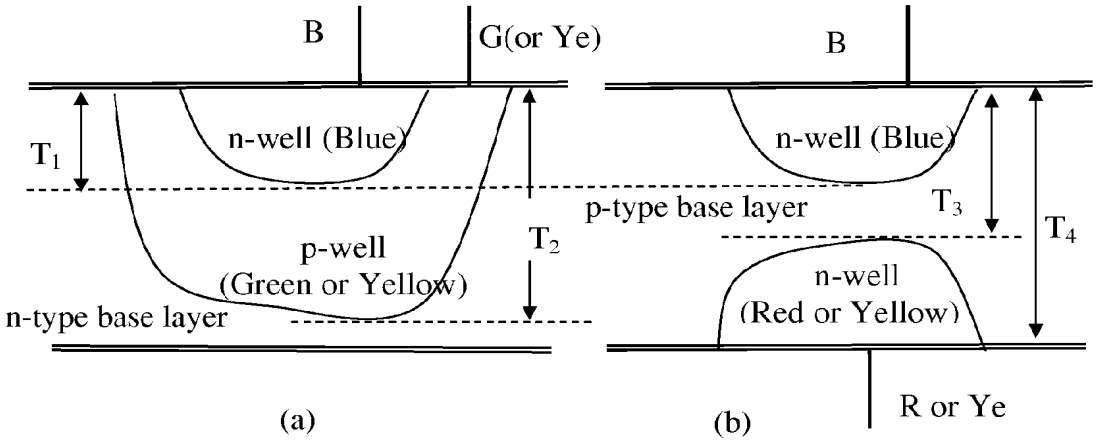

Fig 3

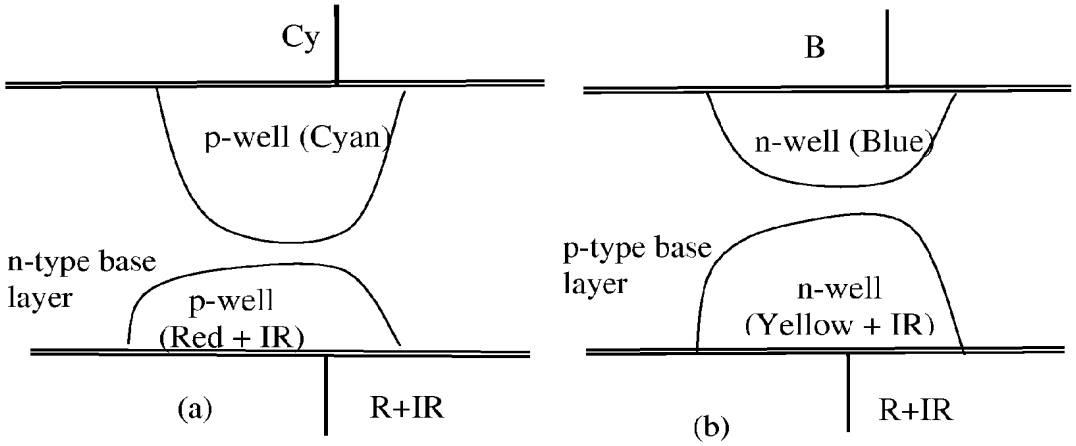

Fig 4

SAMSUNG EX. 1002 - 1872/2862

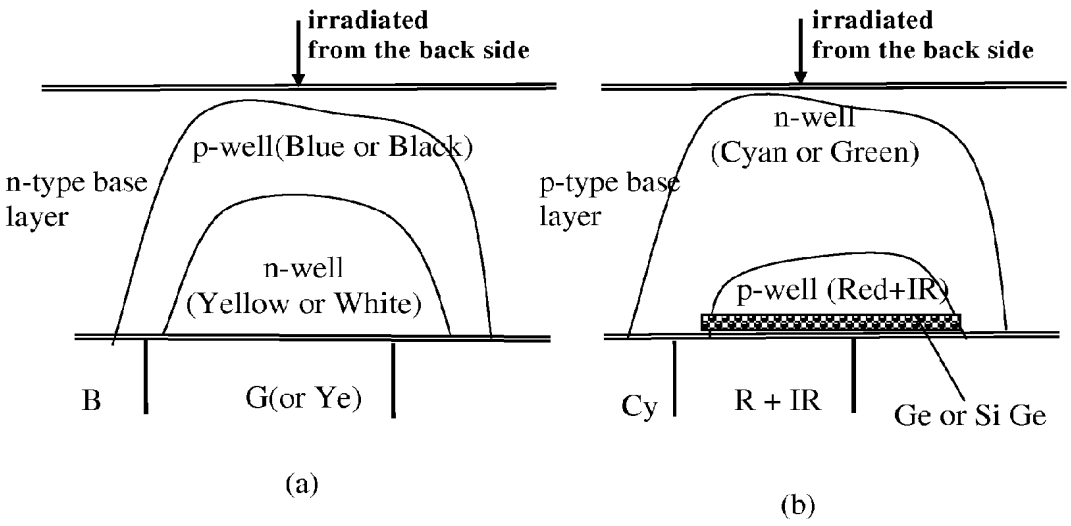

Fig 5

SAMSUNG EX. 1002 - 1873/2862

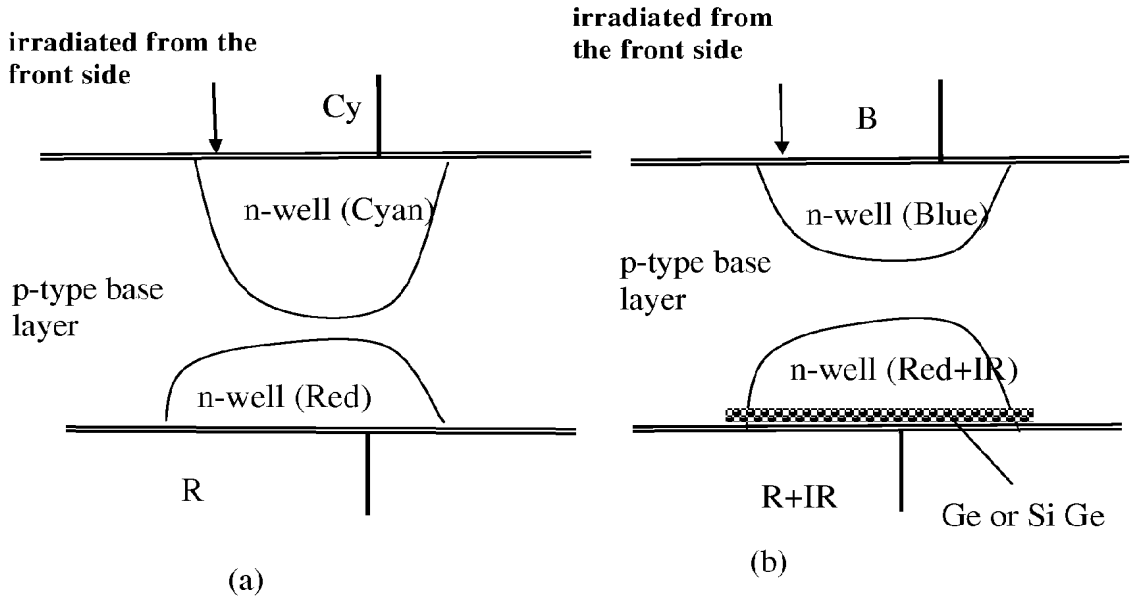

Fig 6

SAMSUNG EX. 1002 - 1874/2862

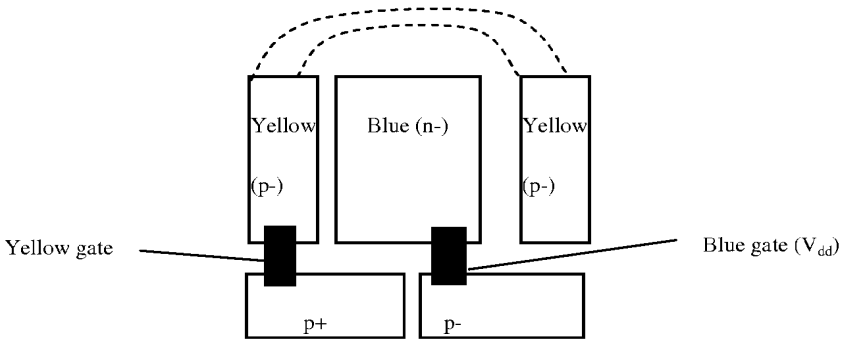

Fig 7

SAMSUNG EX. 1002 - 1875/2862

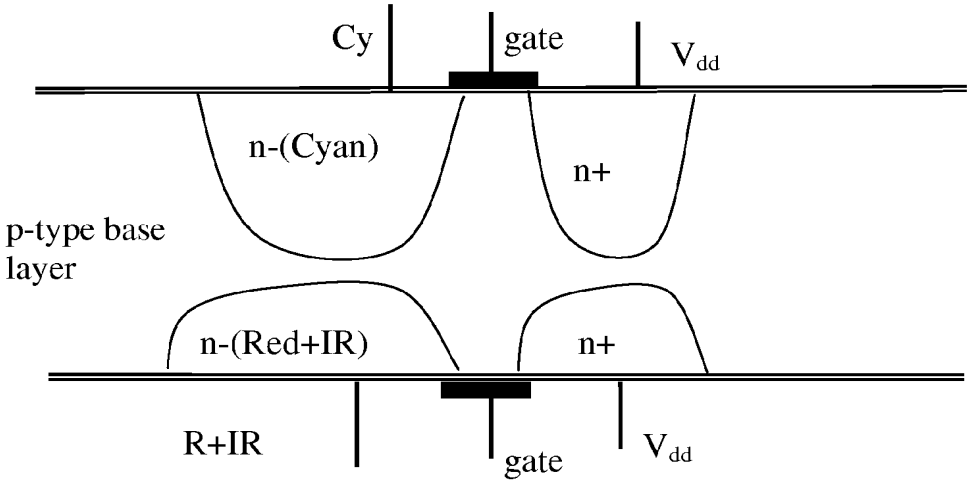

Fig 8

SAMSUNG EX. 1002 - 1876/2862

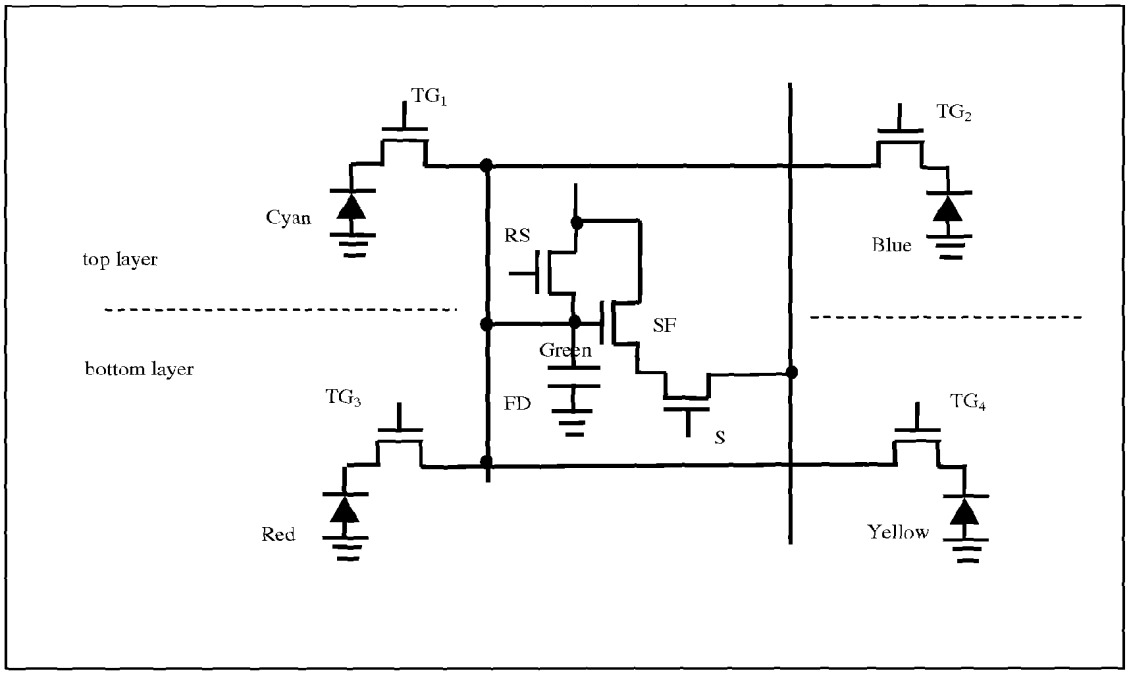

Fig 9

SAMSUNG EX. 1002 - 1877/2862

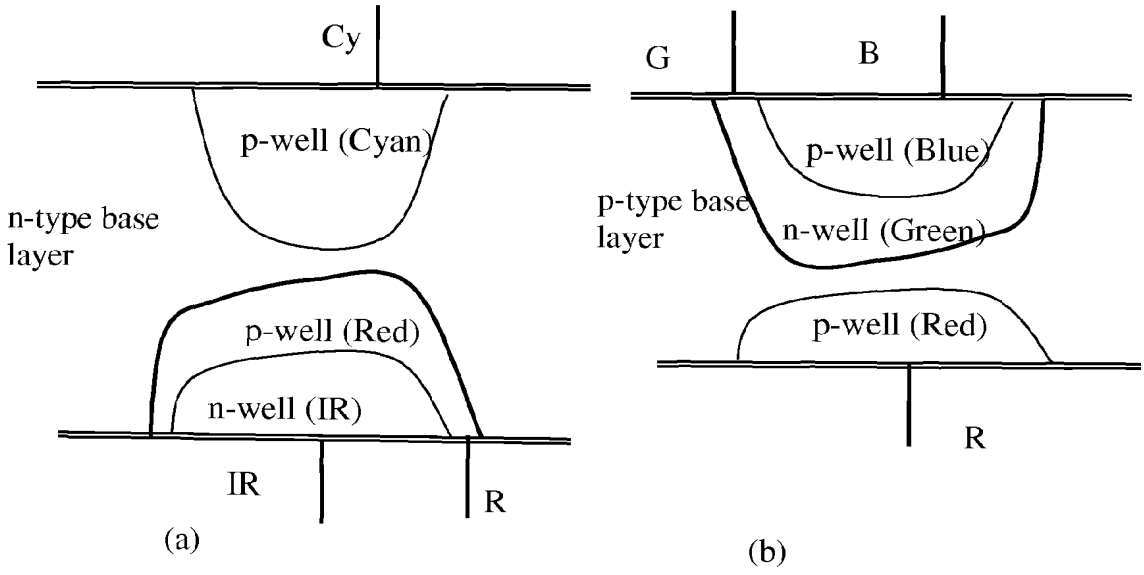

Fig 10

SAMSUNG EX. 1002 - 1878/2862

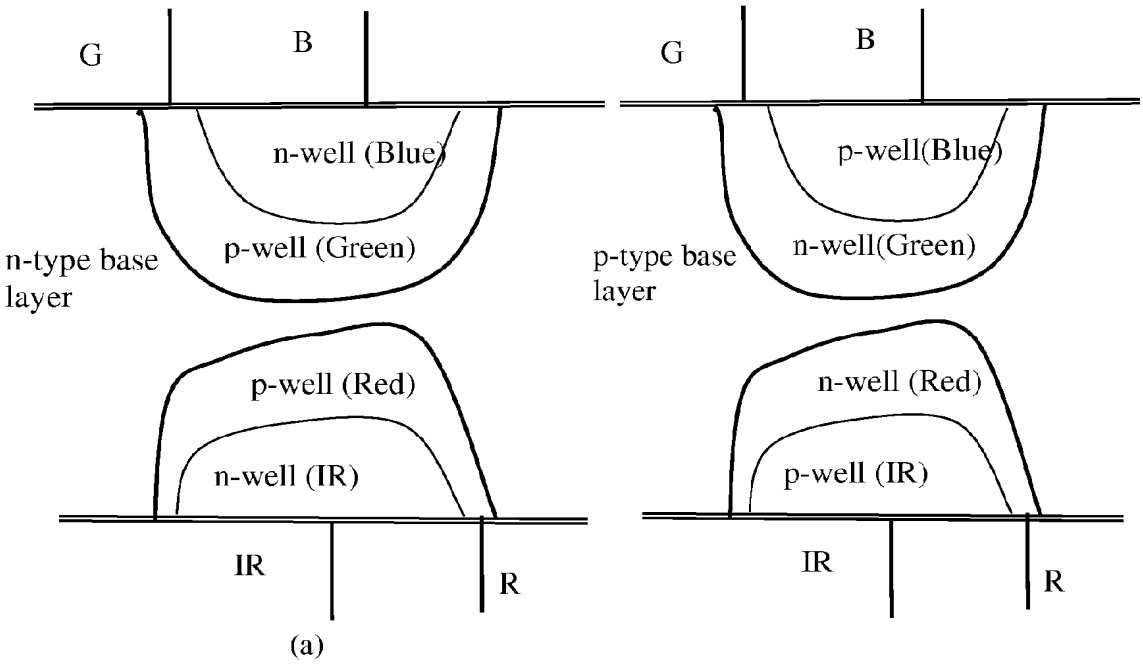

Fig 11

SAMSUNG EX. 1002 - 1879/2862

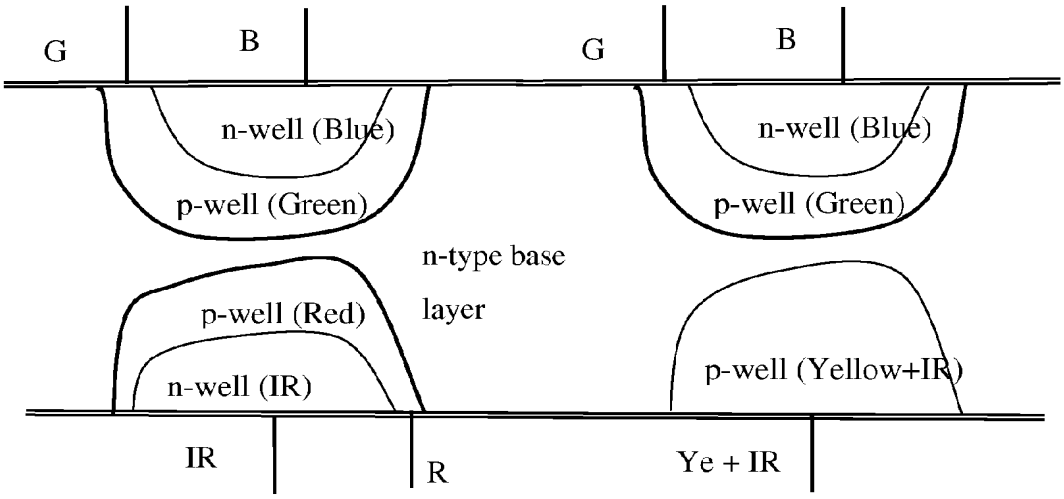

Fig 12

SAMSUNG EX. 1002 - 1880/2862

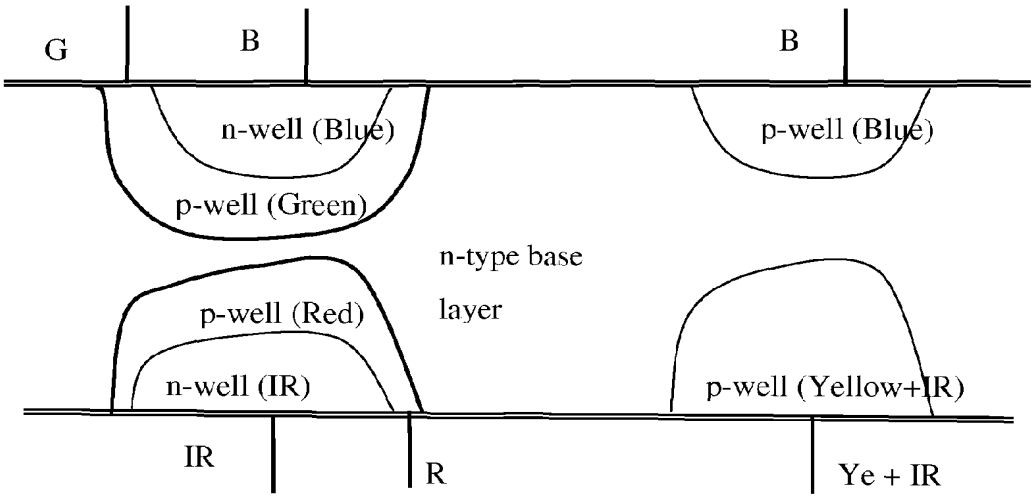

Fig 13

SAMSUNG EX. 1002 - 1881/2862

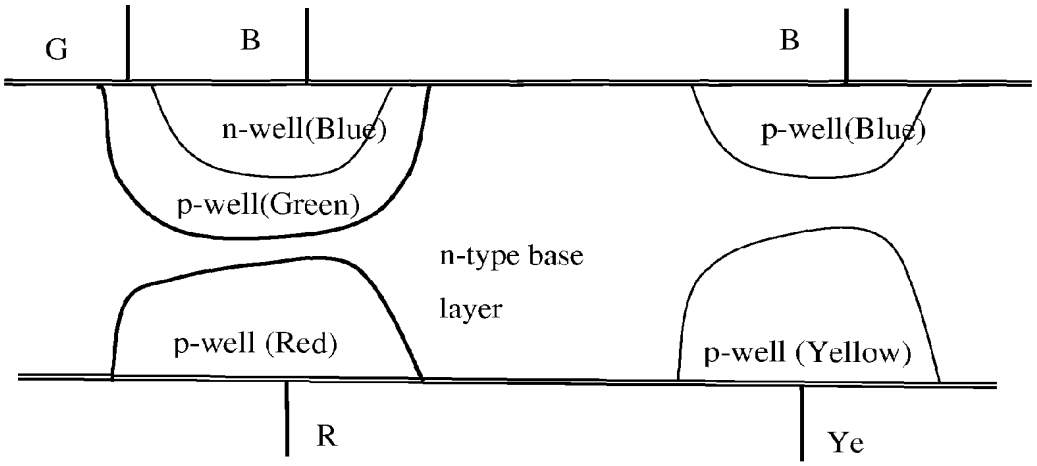

Fig 14

SAMSUNG EX. 1002 - 1882/2862

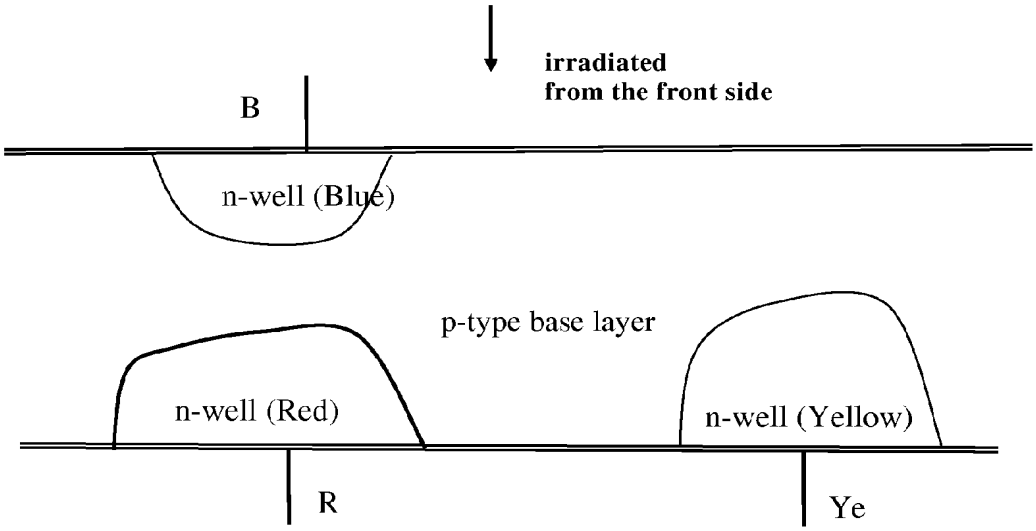

Fig 15

SAMSUNG EX. 1002 - 1883/2862

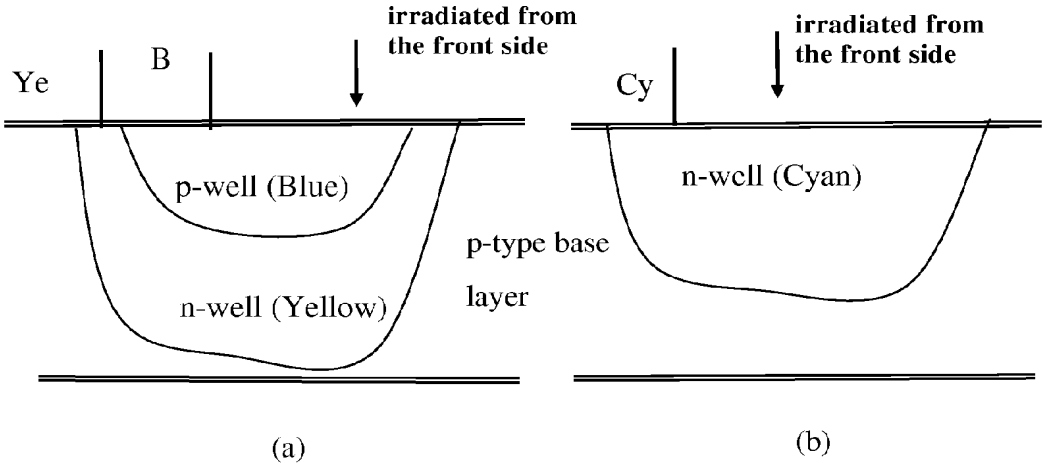

Fig 16

SAMSUNG EX. 1002 - 1884/2862

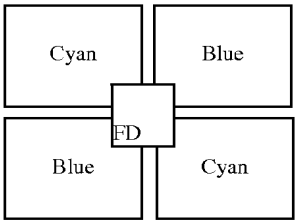

Fig17(a)

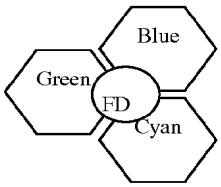

Fig17(b)

SAMSUNG EX. 1002 - 1885/2862

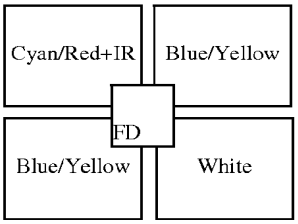

Fig 18(a)

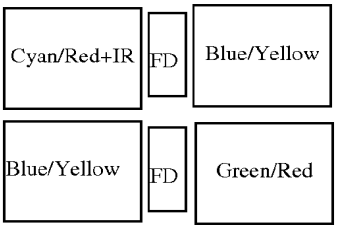

Fig18(b)

SAMSUNG EX. 1002 - 1886/2862

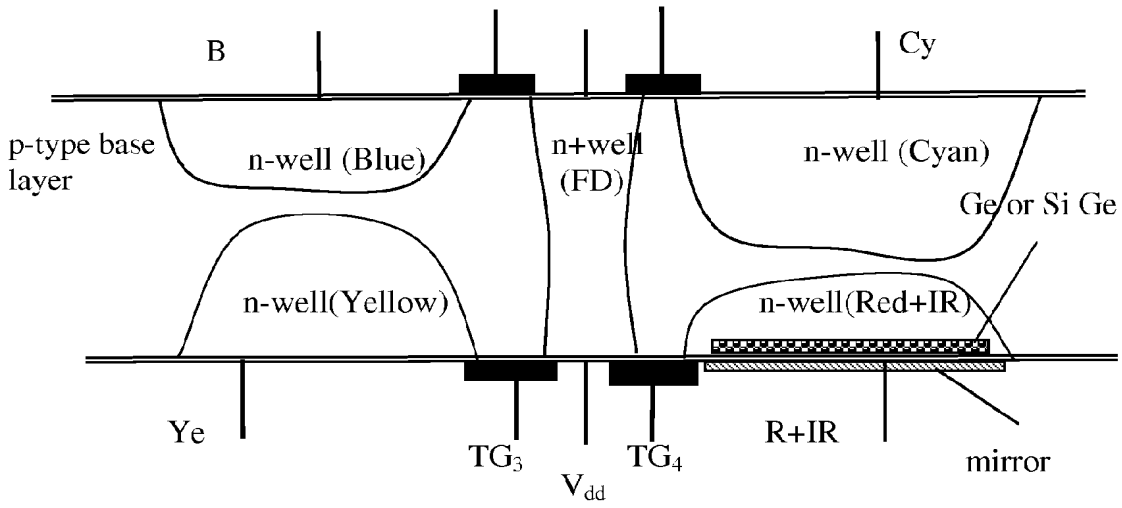

Fig 19

SAMSUNG EX. 1002 - 1887/2862

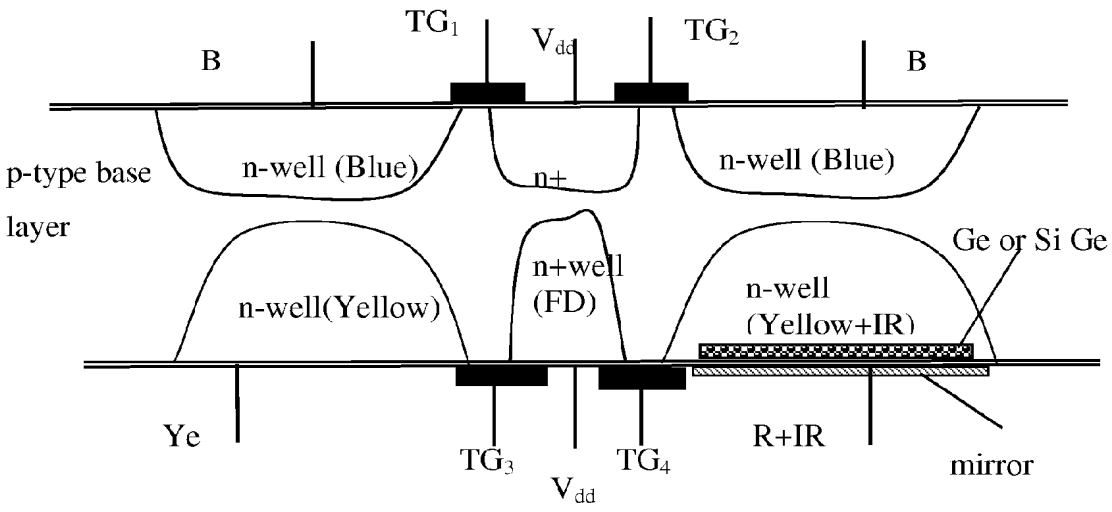

Fig 20

SAMSUNG EX. 1002 - 1888/2862

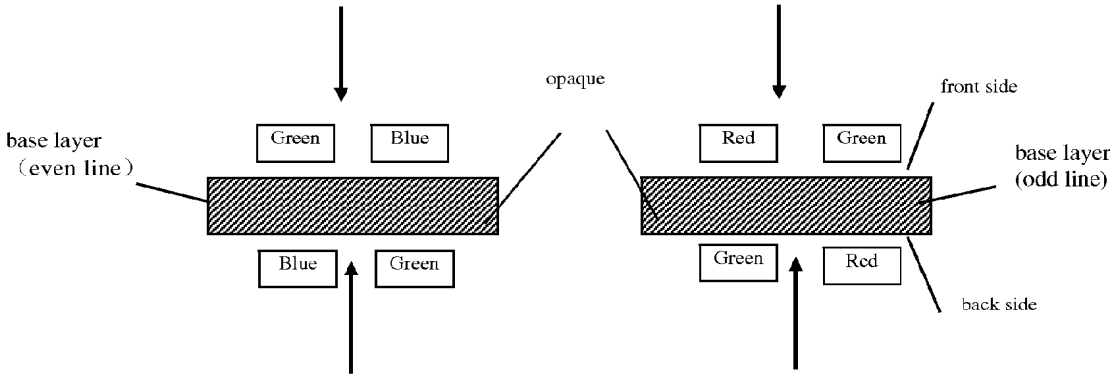

Fig 21

SAMSUNG EX. 1002 - 1889/2862

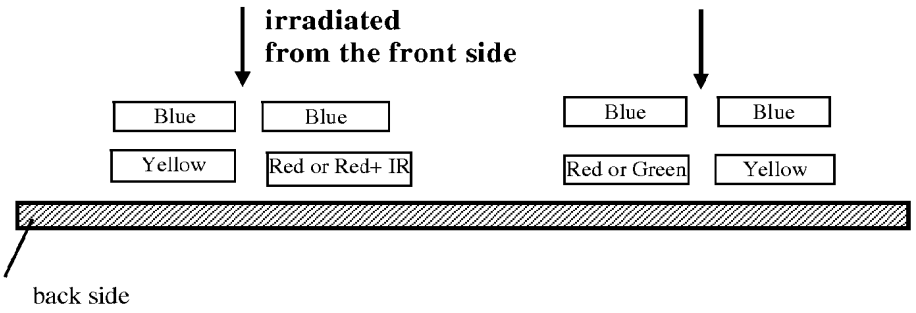

Fig 22(a)

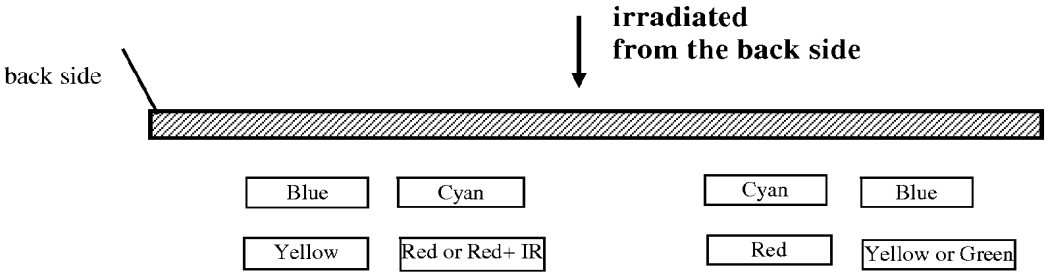

Fig 22(b)

SAMSUNG EX. 1002 - 1890/2862

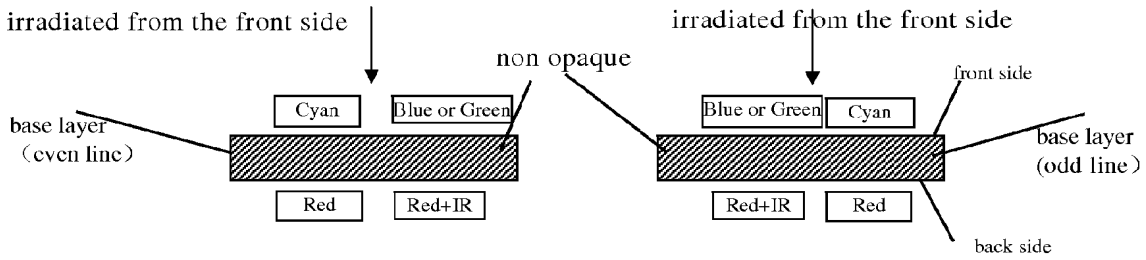

Fig23 (a)

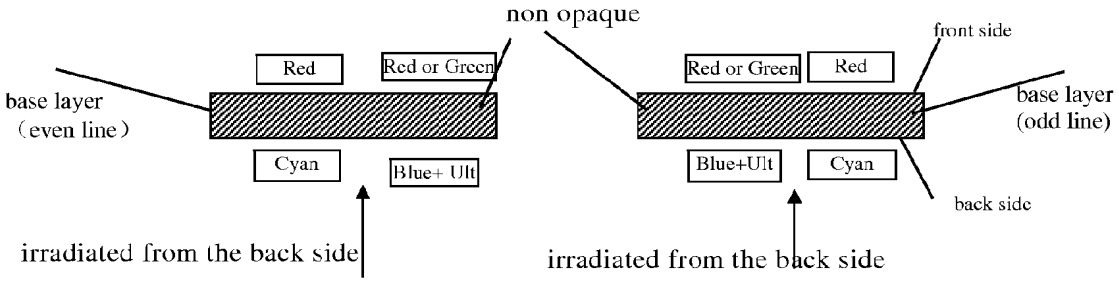

Fig23 (b)

SAMSUNG EX. 1002 - 1891/2862

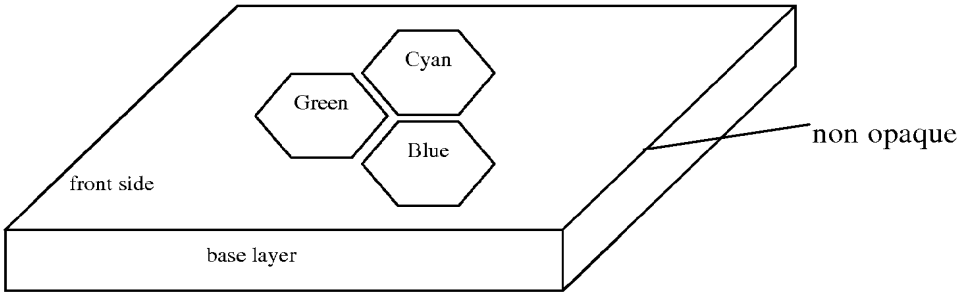

Fig24（a）

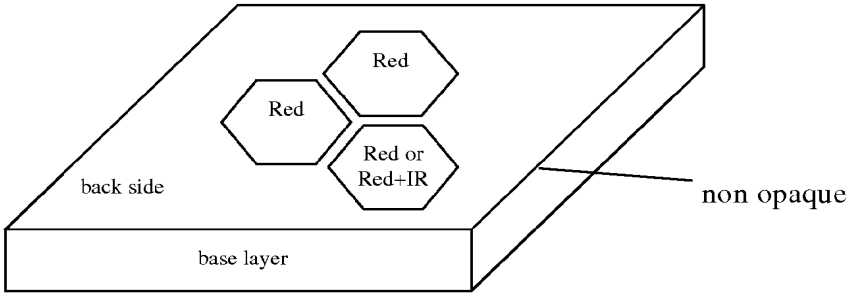

Fig24（b）

SAMSUNG EX. 1002 - 1892/2862

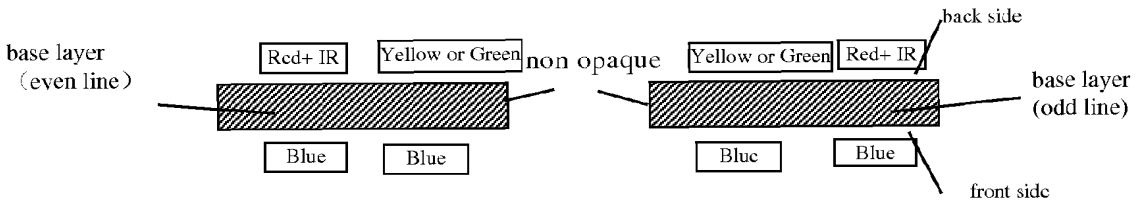

Fig 25

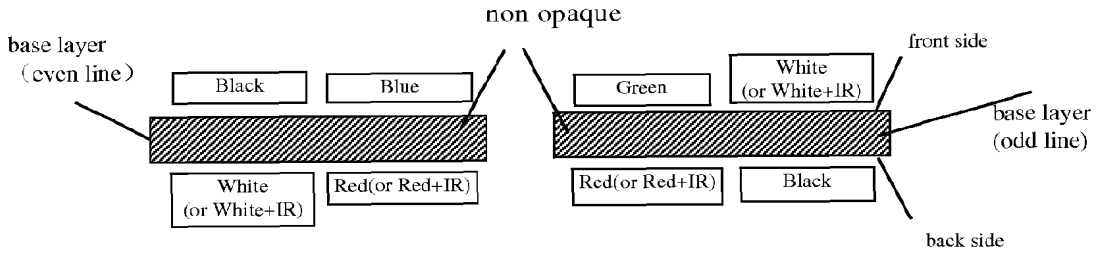

Fig 26

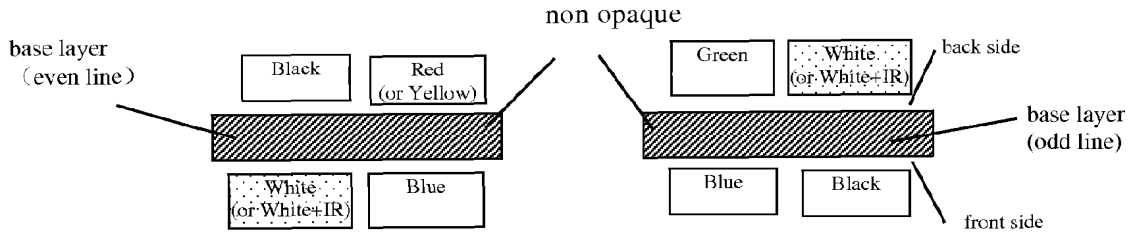

Fig 27

SAMSUNG EX. 1002 - 1893/2862

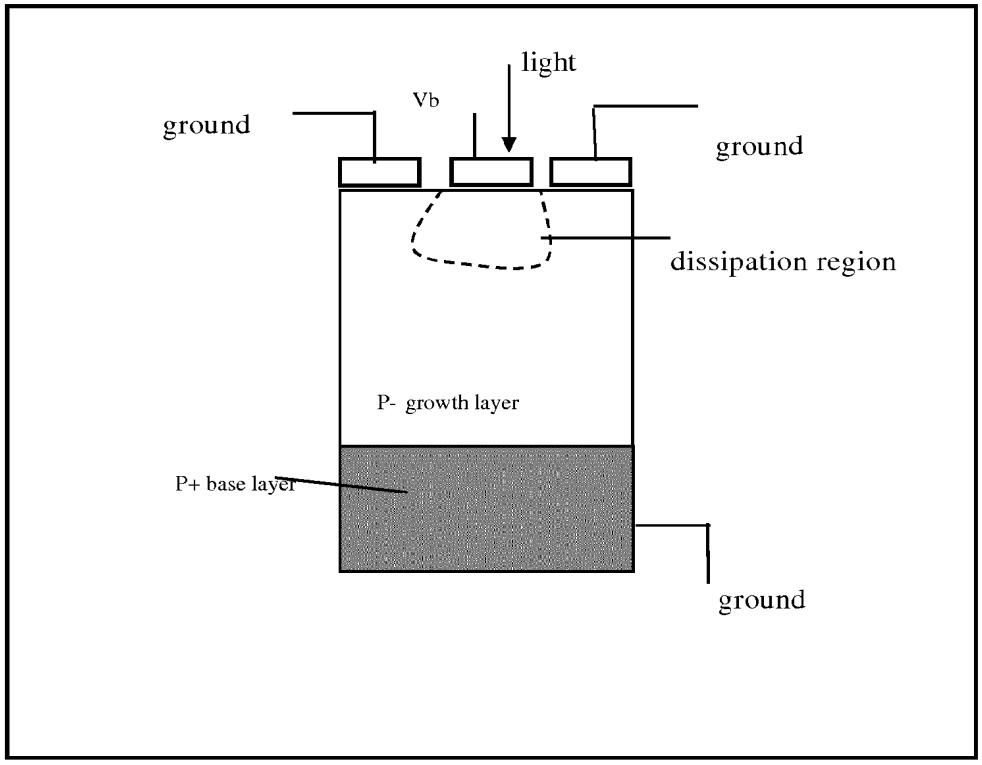

Fig 28

SAMSUNG EX. 1002 - 1894/2862

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2010/073440

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/146 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L 27/-, H01L 21/-, H01L 29/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI, WPI, EPODOC: composite pixel photosensi+ muli-colo?r multispec+ back backside rear photodiode photo-diode stack+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US2010/0109060A1 (OMNIVISION TECHNOLOGIES INC.) 06 May 2010 (06.05.2010) page 2, par. 16 to page 3, par. 29, figures 1-3	1-3, 9-10, 18-22
E	CN101807590A (BOLY MEDIA COMMUNICATIONS (SHENZHEN) CO., LTD.) 18 Aug. 2010 (18.08.2010) claims 1-22	1-22
A	CN101640213A (DONGBUHAITEK CO., LTD.) 03 Feb. 2010 (03.02.2010) The whole document	1-22
A	CN101345248A (BOLY MEDIA COMMUNICATIONS (SHENZHEN) CO., LTD.) 14 Jan. 2009 (14.01.2009) the whole document	1-22

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 Feb. 2011 (21.02.2011)	**24 Mar. 2011 (24.03.2011)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer YANG, Yong Telephone No. (86-10) 62411777

Form PCT/ISA /210 (second sheet) (July 2009)

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2010/073440

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN101577287A (SAMSUNG ELECTRONICS CO., LTD.) 11 Nov. 2009 (11.11.2009) the whole document	1-22
A	US2007/0218578A1 (SHARP LABORATORIES OF AMERICA, INC.) 20 Sep. 2007 (20.09.2007) the whole document	1-22
A	Dietmar Knipp et al. Vertically Integrated Amorphous Silicon Color Sensor Arrays, IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 53, No. 7, Jul. 2006, pages 1551-1557	1-22

Form PCT/ISA /210 (continuation of second sheet) (July 2009)

SAMSUNG EX. 1002 - 1896/2862

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2010/073440

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
US2010/0109060A1	06.05.2010	NONE	
CN101807590A	18.08.2010	NONE	
CN101640213A	03.02.2010	US2010026863A1	04.02.2010
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US2007/0218578A1	20.09.2007	US7419844B2	02.09.2008

Form PCT/ISA /210 (patent family annex) (July 2009)

SAMSUNG EX. 1002 - 1897/2862

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- CN 2007071262 W **[0002]**
- CN 200810217270 **[0002] [0061] [0084]**
- CN 2010073441 W **[0084]**

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- Silicon infrared focal plane arrays. **M. KIMATA.** Handbook of Infrared Detection Technologies. Elsevier Science Ltd, 2002, 352-392 **[0003]**
- **T. TOKUDAETAL.** Backside-hybrid Photo detector for trans-chip detection of NIR light. *IEEE Workshop on Charge-coupled Devices & Advanced Image Sensors, Elmau, Germany,* May 2003 **[0003]**
- **T. TOKUDAETAL.** A CMOS image sensor with eye-safe detection function using backside carrier injection. *J. Inst. Image Information & Television Eng.,* March 2006, vol. 60 (3), 366-372 **[0003]**
- **GERALD C. HOLST ; TERRANCE S. LOMHEIM.** CMOS/CCD Sensors and Camera Systems. JCD Publishing, 2007, 125-125 **[0039]**

SAMSUNG EX. 1002 - 1898/2862

Europäisches Patentamt
European Patent Office
Office européen des brevets

Espacenet

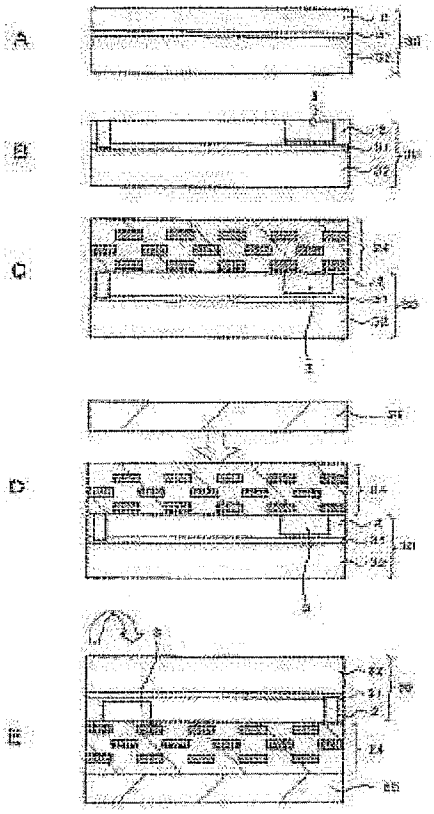
Bibliographic data: JP2010278472 (A) — 2010-12-09

METHOD OF MANUFACTURING SOLID-STATE IMAGING DEVICE

No documents available for this priority number.

Inventor(s):	MARUYAMA YASUSHI ± (MARUYAMA YASUSHI)
Applicant(s):	SONY CORP ± (SONY CORP)
Classification:	**- international:** ***H01L27/146*** **- cooperative:**
Application number:	JP20100191888 20100830
Priority number(s):	JP20100191888 20100830
Also published as:	JP5218502 (B2)

Abstract of JP2010278472 (A)



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PROBLEM TO BE SOLVED: To provide a solid-state imaging device which is more superior in reliability, a method of manufacturing the same, and a camera. ; SOLUTION: The solid-state imaging device has a semiconductor layer 10 in which a plurality of pixels made of a photoelectric-conversion section 11 and a pixel transistor are formed, and is formed with a multilayer interconnection layer 14 in one surface side of the semiconductor layer 10, wherein light from another surface side of the semiconductor layer 10 enters. In the device, a pad 5 is formed in the another surface side of the semiconductor layer 10, and an aperture which reaches a conductive layer in the multilayer interconnection layer 14 is formed at the pad 5. Further, the device has an insulating film 17 which is extended and formed over the another surface side of the semiconductor layer 10 to a sidewall in the aperture, is directly attached to the semiconductor layer 10 in the aperture, and insulates and covers the semiconductor layer 10; and another insulating film which is different from the insulating film 17 directly attached to the semiconductor layer 10, and extended and formed over the another surface side of the semiconductor layer 10 to the sidewall in the aperture. ; COPYRIGHT: (C)2011,JPO&INPIT

Last updated: 23.09.2013 Worldwide Database 5.8.11.4; 92p

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(19)日本国特許庁(JP)　(12)公開特許公報(A)　(11)特許出願公開番号
特開2010-278472
(P2010-278472A)
(43)公開日　平成22年12月9日(2010.12.9)

(51)Int.Cl.		F I		テーマコード（参考）
H01L 27/146	(2006.01)	H01L 27/14	A	4M118

審査請求 有　請求項の数 2　OL　（全 11 頁）

(21)出願番号　特願2010-191888 (P2010-191888)
(22)出願日　平成22年8月30日 (2010.8.30)
(62)分割の表示　特願2004-279780 (P2004-279780)の分割
原出願日　平成16年9月27日 (2004.9.27)

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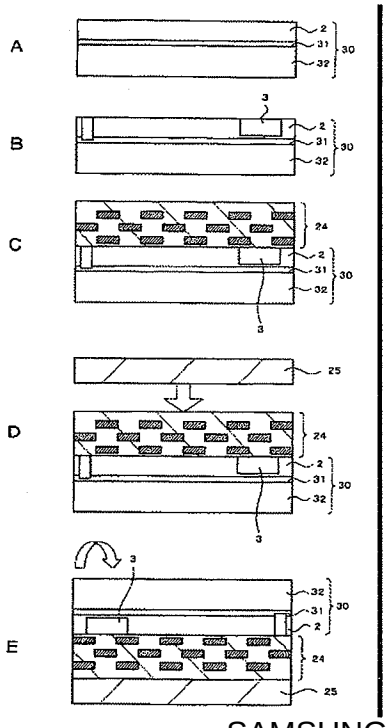
Fターム(参考)　4M118 AA05 AB01 BA14 CA04 CA18 CA32 EA01 EA14 EA18 FA06 FA26 FA33 GA02 GC07 GD03 GD04 GD07

(54)【発明の名称】固体撮像装置の製造方法

(57)【要約】
【課題】より信頼性に優れた固体撮像装置とその製造方法、及びカメラを提供する。
【解決手段】光電変換部１１と画素トランジスタからなる複数の画素が形成された半導体層１０を有し、半導体層１０の一方の面側に多層配線層１４が形成され、半導体層１０の他方の面側から光が入射される固体撮像装置であって、半導体層１０の他方の面側にパッド部５が形成され、パッド部５に多層配線層１４中の導電層に達する開口が形成され、半導体層１０の他方の面上から開口内の側壁に延長して形成された絶縁膜であって、開口内において半導体層１０に直付けされ、半導体層１０を絶縁被覆する絶縁膜１７と、半導体層１０に直付けされた絶縁膜１７とは異なる他の絶縁膜であって、半導体層１０の他方の面上から開口内の側壁に延長して形成された他の絶縁膜とを備える。
【選択図】図３



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【特許請求の範囲】
【請求項1】
半導体基板に光電変換部を形成する工程と、
前記半導体基板の光照射面側に、前記光照射面側からイオン注入することによってアキュムレーション層を形成する工程と、
前記半導体基板の光照射面とは反対側の面にイオン注入することによってアキュムレーション層を形成する工程と、
前記半導体基板の裏面側に第１の支持基板を、熱処理を行いながら貼り合わせる工程と、
前記半導体基板の光照射面側とは反対側を研磨し、前記半導体基板を所用の厚さに形成する工程と、
前記半導体基板の光照射面とは反対側の面に配線層を形成する工程と、
前記配線層上部に第２の支持基板を、熱処理を行いながら貼り合わせる工程と、
前記第１の支持基板を前記半導体基板の光照射面側から除去する工程と、
を有し、
前記半導体基板の両面のアキュムレーション層は、その不純物濃度が$1\times10^{17}cm^{-3}$～$1\times10^{19}cm^{-3}$となるように形成し、
前記半導体基板の光照射面側のアキュムレーション層は、前記第１の支持基板を貼り合わせる工程における熱処理により活性化して形成する
固体作撮像装置の製造方法。
【請求項2】
前記半導体基板の裏面側のアキュムレーション層は、光電変換部との接合深さが０．４μｍ以下となるように形成する
請求項１に記載の固体撮像装置の製造方法。

【発明の詳細な説明】
【技術分野】
【0001】
本発明は、基板裏面側から光を入射させるようにした裏面照射型固体撮像素子の製造方法に関する。
【背景技術】
【0002】
固体撮像素子として、ＣＭＯＳ型固体撮像素子及びＣＣＤ型固体撮像素子が知られている。例えばＣＭＯＳ型固体撮像素子は、フォトダイオードと複数のＭＯＳトランジスタとにより１画素を形成し、複数の画素を所要のパターンに配列して構成される。このフォトダイオードは、受光量に応じた信号電荷を生成し蓄積する光電変換素子であり、複数のＭＯＳトランジスタはフォトダイオードからの信号電荷の読み出し動作を行うための素子である。
【0003】
図８に、イメージセンサに適用した従来の裏面から光照射するＣＭＯＳ型固体撮像素子の例を示す。図８は、画素の要部を示している。単位画素ではフォトダイオード５３と、フォトダイオード５３からの信号電荷を読み出すＭＯＳトランジスタ５４と、それ以外のＭＯＳトランジスタ５５の構成部分を表している。この裏面照射型のＣＭＯＳ固体撮像素子５１は、第１導電型、例えばｎ型のシリコン半導体基板６１に各画素を区画するための画素分離領域６２を形成し、各区画された画素領域にフォトダイオード５３と複数のＭＯＳトランジスタ、すなわち読み出しトランジスタ５４、それ以外のＭＯＳトランジスタ５５が形成されて単位画素６０が構成される。そして、この画素６０が多数個、２次元マトリックス状に配列される。
【0004】
画素分離領域６２は、基板表面から基板裏面にわたって比較的に低不純物濃度の第２導

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電型であるｐ型半導体領域により形成される。フォトダイオード５３は、ｐ型の画素分離領域６２と各ＭＯＳトランジスタ５４、５５が形成される比較的に深いｐ型半導体ウェル領域６３とにより囲まれたｎ型半導体基板６１で形成される。すなわちフォトダイオード５３は、ｎ－半導体領域６１Ａとその表面側の高不純物濃度のｎ＋半導体領域（ｎ＋領域）６１Ｂとにより形成される。このｎ＋領域６１Ｂは、フォトダイオード３内で光電変換により生成された電子・正孔のうち信号となる電荷、この例では電子を蓄積するための電荷蓄積領域となる。さらに、このｎ＋半導体領域６１Ｂの表面にｐ＋半導体領域６４が形成される。

【0005】

各ＭＯＳトランジスタ５４、５５は、次のようにして構成される。ｐ型半導体ウェル領域６３の表面には、フォトダイオード５３に隣接するように、高不純物濃度のｎ型ソース・ドレイン領域（ｎ＋領域）５７、５８、５９がイオン注入により形成される。

読み出しトランジスタ５４は、ｎ型ソース・ドレイン領域５７と、フォトダイオード５３の表面側のソース・ドレイン領域を兼ねるｎ＋領域６１Ｂと、両領域５７及び６１Ｂ間のｐ－チャネル領域６５上にゲート絶縁膜を介して形成したゲート電極とにより構成される。また、読み出しトランジスタ５４以外のトランジスタ５５は、対をなすｎ型ソース・ドレイン領域５８及び５９と、両領域５８及び５９間のｐ型半導体ウェル領域６３上にゲート絶縁膜を介して形成したゲート電極６７とにより形成される。

また、ｎ型半導体基板６１の光照射面となる裏面には、暗電流の発生を抑制するための高不純物濃度のｐ型半導体領域よりなるｐ＋アキュムレーション層６８が形成される。

【0006】

この裏面照射型固体撮像素子５１は、半導体基板６１の裏面側から光をフォトダイオード５３に入射し、フォトダイオード５３において光電変換して受光量に応じた信号電荷をｎ＋領域６１Ｂに蓄積するようにしている。そして、各ＭＯＳトランジスタ５４、５５の読み出し動作によってｎ＋領域６１Ｂの信号電荷が読み出される。

【0007】

特許文献１には、上述した裏面照射型固体撮像素子が開示されている（特許文献１、図４参照）。

【図面の簡単な説明】

【0013】

【図1】本発明に係る裏面照射型固体撮像素子の一実施の形態を示す構成図である。

【図2】本発明に係る裏面照射型固体撮像素子の要部を示す断面図である。

【図3】Ａ～Ｅ 本発明に係る裏面照射型固体撮像素子の製造方法の一実施の形態を示す断面図である（その１）。

【図4】Ａ～Ｂ 本発明に係る裏面照射型固体撮像素子の製造方法の一実施の形態を示す断面図である（その２）。

【図5】Ａ～Ｆ 本発明に係る裏面照射型固体撮像素子の製造方法の他の実施の形態を示す断面図である（その１）。

【図6】Ａ～Ｄ 本発明に係る裏面照射型固体撮像素子の製造方法の他の実施の形態を示す断面図である（その２）。

【図7】本発明に係る裏面照射型固体撮像素子を用いる電子機器モジュールの構成図である。

【図8】従来の裏面照射型固体撮像素子を示す構成図である。

【符号の説明】

【0042】

１・・裏面照射型固体撮像素子、２・・半導体基板、３・・フォトダイオード、８・・ゲート電極、１３・・画素分離領域、１２，１５・・ｐ＋アキュムレーション層、１６・・ｐ型半導体ウェル領域、１７・・絶縁保護膜、２０・・単位画素、２１・・オンチップレンズ、２２・・オンチップカラーフィルタ、２４・・配線領域、２４ａ・・配線層、２５、３５・・支持基板、２６・・層間絶縁膜、３０・・ＳＯＩ基板、２８，３１，３６・

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・シリコン酸化膜、３２・・ｎ型半導体基板、５１・・裏面照射型固体撮像素子、５３・・フォトダイオード、５４・・読み出しトランジスタ、５５・・ＭＯＳトランジスタ、５７、５８、５９・・ドレイン領域（ｎ＋領域）、６０、単位画素、６１・・ｎ型のシリコン半導体基板、６１Ａ・・ｎ半導体領域（領域）、６１Ｂ・・ｎ＋半導体領域（ｎ＋領域）、６２・・画素分離領域、６４・・ｐ＋アキュムレーション層（電荷蓄積層）、６５・・ｐ－チャネル領域、６７・・ゲート電極、６８・・ｐ＋アキュムレーション層

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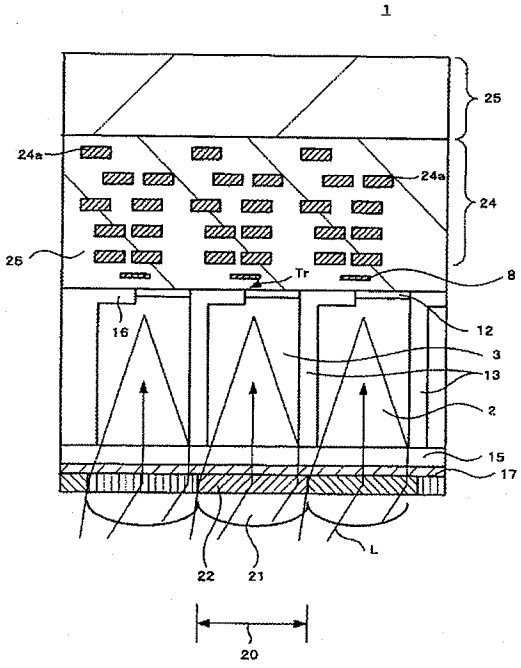
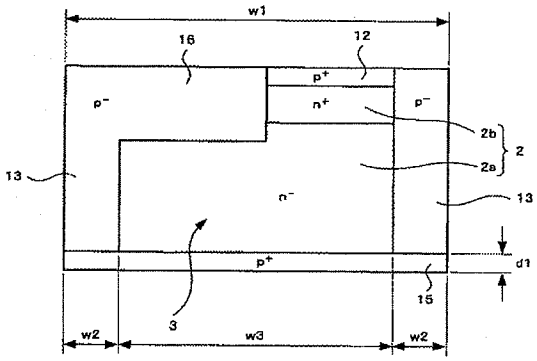
【図1】



【図2】



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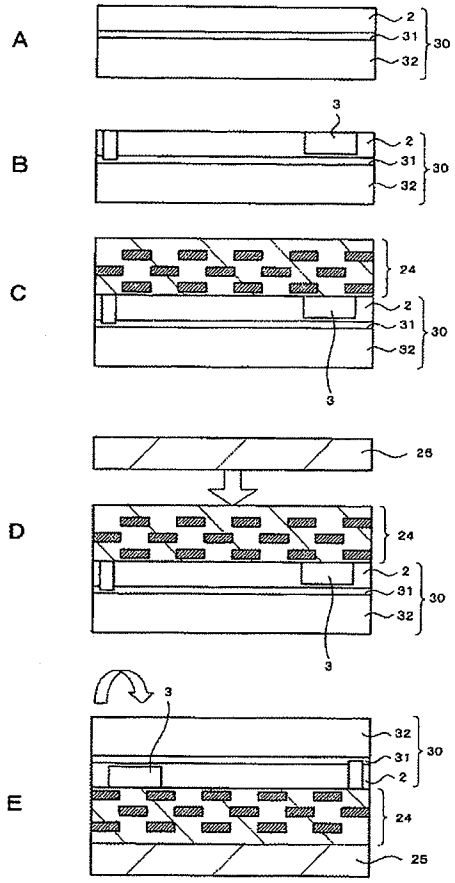
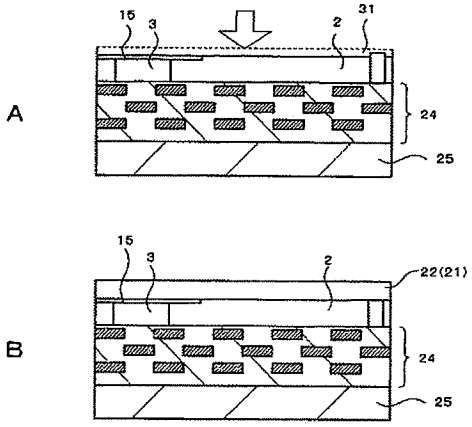
【図3】


A
2
31
32
30
B
3
2
31
32
30
C
24
2
31
32
30
3
26
D
24
2
31
32
30
3
E
3
32
31
30
2
24
25

【図4】



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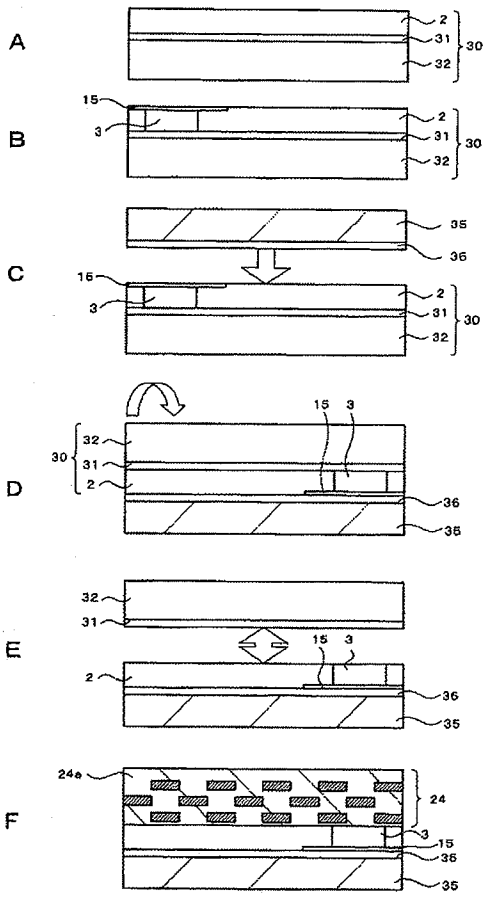
【図5】



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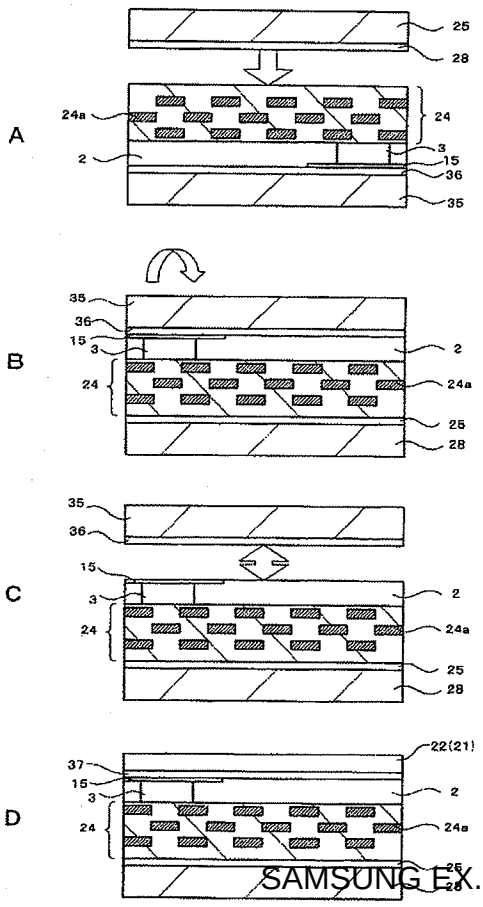
【図6】



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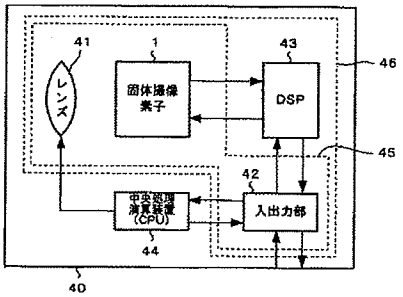
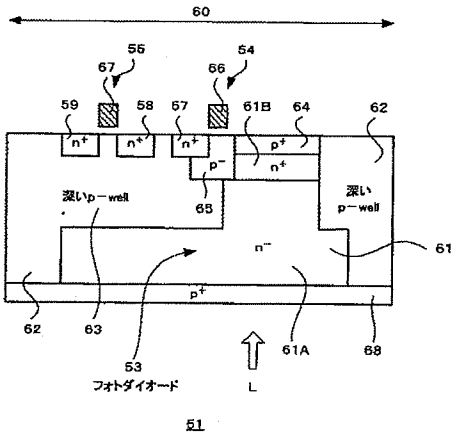
【図7】


41
1
43
46
レンズ
固体撮像素子
DSP
45
42
中央処理演算装置(CPU)
入出力部
44
40

【図8】


60
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67
54
66
59
58
57
61B
64
62
n+
n+
n+
p+
p−
n+
深いp−well
65
深い
p−well
61
n−
p+
62
63
53
フォトダイオード
L
61A
68
51

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(19) 대한민국특허청(KR)
(12) 등록특허공보(B1)

(45) 공고일자 2008년04월29일
(11) 등록번호 10-0825808
(24) 등록일자 2008년04월22일

(51) Int. Cl.
H01L 27/146 (2006.01)
(21) 출원번호 10-2007-0019134
(22) 출원일자 2007년02월26일
심사청구일자 2007년02월26일
(56) 선행기술조사문헌
KR1020020058459 A

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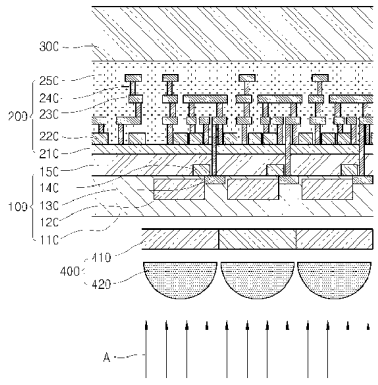
전체 청구항 수 : 총 20 항 심사관 : 안철흥

(54) 후면 조명 구조의 이미지 센서 및 그 이미지 센서 제조방법

(57) 요 약

본 발명은 광감도를 극대화하고 픽셀 당 수광 면적, 즉 포화도를 극대화할 수 있는 후면 조명 구조의 이미지 센서 및 그 이미지 센서 제조방법을 제공한다. 그 이미지 센서는 제1 웨이퍼 상에 형성된 포토 다이오드 및 트랜스퍼 게이트 트랜지스터(transfer gate transistor)를 포함하는 포토 다이오드부; 상기 포토 다이오드부 상부로 접합된 제2 웨이퍼 상에 형성된 신호처리 및 제어 트랜지스터 및 배선 라인을 포함하는 배선 라인부; 상기 배선 라인부 상부에 접합된 지지대 기판; 및 상기 제1 웨이퍼 하부에 형성된 필터부;를 포함한다. 또한, 그 이미지 센서 제조방법은 제1 웨이퍼 상에 포토 다이오드 및 트랜스퍼 게이트 트랜지스터를 포함한 포토 다이오드부를 형성하는 단계; 제2 웨이퍼를 상기 포토 다이오드부 상부로 접합하고 상기 제2 웨이퍼 상에 신호처리 및 제어 트랜지스터 및 배선 라인을 포함하는 배선 라인부를 형성하는 단계; 상기 배선 라인부 상부로 지지대 기판을 접합하는 단계; 및 상기 제1 웨이퍼 하부로 필터부를 형성하는 단계;를 포함한다.

대표도 - 도2



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특허청구의 범위

청구항 1

제1 웨이퍼 상에 형성된 포토 다이오드 및 트랜스퍼 게이트 트랜지스터(transfer gate transistor)를 포함하는 포토 다이오드부;

상기 포토 다이오드부 상부로 접합된 제2 웨이퍼 상에 형성된 신호처리 및 제어 트랜지스터 및 배선 라인을 포함하는 배선 라인부;

상기 배선 라인부 상부에 접합된 지지대 기판; 및

상기 제1 웨이퍼 하부에 형성된 필터부;를 포함하는 후면 조명(backside illumination) 구조의 이미지 센서.

청구항 2

제1 항에 있어서,

상기 제2 웨이퍼는 수소 이온주입(implantation) 공정이 수행된 웨이퍼이고,

상기 배선 라인부는 상기 포토 다이오드부 상부에 접합되는 상기 제2 웨이퍼가 스마트 컷(smart-cut)을 통해 제거되고 남은 부분에 상기 신호처리 및 제어 트랜지스터 및 배선 라인이 형성되어 이루어진 것을 특징으로 하는 후면 조명 구조의 이미지 센서.

청구항 3

제2 항에 있어서,

상기 제2 웨이퍼는 밀착 및 열처리를 통해 상기 포토 다이오드부 상부에 접합되는 것을 특징으로 하는 후면 조명 구조의 이미지 센서.

청구항 4

제1 항에 있어서,

상기 포토 다이오드부는 상기 포토 다이오드 주변 상부로 형성된 플로팅 디퓨전(floating difusion) 영역, 및 상기 포토 다이오드 및 트랜스퍼 게이트 트랜지스터가 형성된 상기 제1 웨이퍼 전면으로 형성된 절연층을 포함하는 것을 특징으로 하는 후면 조명 구조의 이미지 센서.

청구항 5

제1 항에 있어서,

상기 신호처리 및 제어 트랜지스터는 소스 팔로어 트랜지스터(source follower transistor), 선택 트랜지스터(selection transistor), 및 리셋 트랜지스터(reset transistor)를 포함하는 것을 특징으로 하는 후면 조명 구조의 이미지 센서.

청구항 6

제1 항에 있어서,

상기 이미지 센서는 상기 포토 다이오드부가 1개의 포토 다이오드 당 1개의 트랜지스터(1Tr/pixel)를 갖는 구조를 갖는 것을 특징으로 하는 후면 조명 구조의 이미지 센서.

청구항 7

제1 항에 있어서,

상기 제1 웨이퍼는 10 ㎛ 이하의 두께를 가지되, 상기 포토 다이오드 및 트랜스퍼 게이트 트랜지스터를 합한 두께 이상을 갖는 것을 특징으로 하는 후면 조명 구조의 이미지 센서.

청구항 8

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제1 항에 있어서,

상기 필터부는 빛을 파장에 따라 투과시키는 필터 어레이(filter array) 및 상기 필터 어레이로 빛을 집광하기 위한 마이크로 렌즈(micro-lens)를 포함하고,

상기 이미지 센서는 상기 필터부를 통해 상기 포토 다이오드로 바로 빛이 입사되는 구조를 갖는 것을 특징으로 하는 후면 조명 구조의 이미지 센서.

청구항 9

제8 항에 있어서,

상기 이미지 센서는 빛이 입사되는 상기 포토 다이오드 하부와 반대방향인 상기 포토 다이오드 상부로 상기 배선 라인부가 배치되어 빛에 대한 광감도(sensitivity)가 극대화된 것을 특징으로 하는 후면 조명 구조의 이미지 센서.

청구항 10

제1 웨이퍼 상에 포토 다이오드 및 트랜스퍼 게이트 트랜지스터를 포함한 포토 다이오드부를 형성하는 단계;

제2 웨이퍼를 상기 포토 다이오드부 상부로 접합하고 상기 제2 웨이퍼 상에 신호처리 및 제어 트랜지스터 및 배선 라인을 포함하는 배선 라인부를 형성하는 단계;

상기 배선 라인부 상부로 지지대 기판을 접합하는 단계; 및

상기 제1 웨이퍼 하부로 필터부를 형성하는 단계;를 포함하는 후면 조명 구조의 이미지 센서 제조방법.

청구항 11

제10 항에 있어서,

상기 포토 다이오드부 형성 단계는,

상기 제1 웨이퍼 상에 포토 다이오드를 형성하는 단계;

상기 포토 다이오드 주변 상부로 플로팅 디퓨젼 영역을 형성하는 단계;

상기 포토 다이오드 상부에 상기 트랜스퍼 게이트 트랜지스터 형성하는 단계; 및

상기 제1 웨이퍼 전면으로 절연층을 형성하는 단계;를 포함하는 것을 특징으로 하는 후면 조명 구조의 이미지 센서 제조방법.

청구항 12

제10 항에 있어서,

상기 제2 웨이퍼는 수소 이온주입 공정이 수행된 웨이퍼이고,

상기 제2 웨이퍼의 접합 및 배선 라인부를 형성하는 단계는,

상기 수소 이온이 주입된 상기 제2 웨이퍼의 상면을 상기 제1 기판과 접합하는 단계;

상기 제2 웨이퍼를 스마트 컷을 통해 절단하는 단계;

절단되어 남은 상기 제2 웨이퍼 상에 신호처리 및 제어 트랜지스터를 형성하는 단계; 및

상기 신호처리 및 제어 트랜지스터 상부로 BEOL(Back End Of Line) 공정을 수행하는 단계;를 포함하는 것을 특징으로 하는 후면 조명 구조의 이미지 센서 제조방법.

청구항 13

제12 항에 있어서,

상기 신호처리 및 제어 트랜지스터는 소스 팔로어 트랜지스터, 선택 트랜지스터, 및 리셋 트랜지스터를 포함하는 것을 특징으로 하는 후면 조명 구조의 이미지 센서 제조방법.

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청구항 14

제10 항에 있어서,

상기 이미지 센서 제조방법은,

상기 제1 웨이퍼 하부로 필터부를 형성하는 단계 전에

상기 제1 웨이퍼의 하면을 얇게 연마하는 단계를 포함하는 것을 특징으로 하는 후면 조명 구조의 이미지 센서 제조방법.

청구항 15

제14 항에 있어서,

상기 제1 웨이퍼는 상기 연마에 의해 10 ㎛ 이하의 두께를 가지되, 상기 포토 다이오드 및 트랜스퍼 게이트 트랜지스터를 합한 두께 이상을 갖는 것을 특징으로 하는 후면 조명 구조의 이미지 센서 제조방법.

청구항 16

제10 항에 있어서,

상기 필터부를 형성하는 단계는,

상기 제1 웨이퍼 하부로 빛을 파장에 따라 투과시키는 필터 어레이를 형성하는 단계; 및

상기 필터 어레이 하부로 빛을 집광하기 위한 마이크로 렌즈를 형성하는 단계:를 포함하는 것을 특징으로 하는 후면 조명 구조의 이미지 센서 제조방법.

청구항 17

제10 항에 있어서,

상기 이미지 센서는,

상기 포토 다이오드부가 1개의 포토 다이오드 당 1개의 트랜지스터(1Tr/pixel)를 갖는 구조를 갖는 것을 특징으로 하는 후면 조명 구조의 이미지 센서 제조방법.

청구항 18

제1 웨이퍼에 포토 다이오드 및 트랜스퍼 게이트 트랜지스터를 포함한 포토 다이오드부를 형성하는 단계;

제2 웨이퍼를 상기 포토 다이오드부 상부로 접합하고 스마트 컷을 통해 상기 제2 웨이퍼를 절단하는 단계;

절단되어 남은 상기 제2 웨이퍼에 신호처리 및 제어 트랜지스터 및 배선 라인을 포함하는 배선 라인부를 형성하는 단계;

상기 배선 라인부 상부로 지지대 기판을 접합하는 단계;

상기 제1 웨이퍼의 하면을 얇게 연마하는 단계; 및

상기 포토 다이오드부 하부로 필터부를 형성하는 단계;를 포함하는 후면 조명 구조의 이미지 센서 제조방법.

청구항 19

제18 항에 있어서,

상기 배선 라인부를 형성하는 단계는,

상기 남은 상기 제2 웨이퍼 상에 신호처리 및 제어 트랜지스터를 형성하는 단계; 및

상기 신호처리 및 제어 트랜지스터 상부로 BEOL(Back End Of Line) 공정을 수행하는 단계;를 포함하는 것을 특징으로 하는 후면 조명 구조의 이미지 센서 제조방법.

청구항 20

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제18 항에 있어서,

상기 신호처리 및 제어 트랜지스터는 소스 팔로어 트랜지스터, 선택 트랜지스터, 및 리셋 트랜지스터를 포함하고,

상기 이미지 센서는,

상기 포토 다이오드부가 1개의 포토 다이오드 당 1개의 트랜지스터(1Tr/pixel)를 갖는 구조를 갖는 것을 특징으로 하는 후면 조명 구조의 이미지 센서 제조방법.

명 세 서

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

<15> 본 발명은 이미지 센서 및 그 제조 방법에 관한 것으로, 특히 3차원 집적 방식을 이용한 이미지 센서 및 그 제조 방법에 관한 것이다.

<16> 이미지 센서는 광학 영상(optical image)을 전기 신호로 변환시키는 반도체 소자로서, 크게 전하결합소자(Charge Coupled Device: CCD)와 CMOS(Complementary Metal-Oxide-Silicon) 이미지 센서가 있다.

<17> 이 중에서 CCD는 개개의 MOS(Metal-Oxide-Silicon) 캐패시터가 서로 매우 근접한 위치에 있으면서 전하 캐리어가 캐패시터에 저장되고 이송되는 방식을 채용한 소자이다. 한편, CMOS(Complementary MOS) 이미지 센서는 제어회로(control circuit) 및 신호처리회로(signal processing circuit)를 주변회로로 사용하는 CMOS 기술을 이용하며, 화소 수만큼 MOS 트랜지스터를 만들고 이것을 이용하여 차례차례 출력을 검출하는 스위칭 방식을 채용한 소자이다.

<18> CMOS 이미지 센서는 CCD에 비해 구동방식이 간편하며, 신호처리회로를 한 칩에 집적할 수 있기 때문에 SOC(System On Chip)의 구현이 가능하여 모듈의 소형화에 유리하다. 그에 따라, 현재 모바일 폰(mobile phone), PC(Personal Computer)용 카메라 및 전자기기 등에서 광범위하게 사용되고 있다.

<19> 도 1은 종래의 3차원 집적(3D integration) 방식의 CMOS 이미지 센서를 개략적으로 보여주는 단면도이다.

<20> 도 1을 참조하면, 이미지 센서는 기판에 형성된 포토 다이오드(10, Photo Diode:PD)를 포함하는 수광부, 배선 라인층(20), 컬러 필터 어레이(30, Color Filter Array: CFA), 및 마이크로 렌즈(40, micro-lens)를 포함한다. 한편, 배선 라인층(20)은 도시한 바와 같이 컬러 필터 어레이(30)와 포토 다이오드(10) 사이에 존재하고 투명한 절연막 사이로 형성된 다층의 여러 배선 라인들(M1 ~ M4)로 구성된다.

<21> 이와 같은 종래의 이미지 센서는 제조 공정 특히 BEOL(Back End Of Line) 즉, 메탈라인 공정은 반도체 소자의 제조 공정과 유사하다. 이때, PMD(Pre-Metal Dielectric)와 IMD(Inter-Metal Dielectric) 및 보호막(passivation layer) 등을 형성하기 위하여 서로 상이한 절연 물질이 사용되어야 하며, 이로 인해 각 물질층 간 계면(Interface)에서 빛의 난반사 현상이 발생하여 광감도(sensitivity)를 떨어뜨린다. 또한, 상이한 절연막으로 인해 서로 다른 굴절률을 가지기 때문에 빛의 굴절에 의해 광감도가 떨어지기도 한다. 이와 함께, 종래의 CMOS 이미지 센서를 형성함에 있어서는, 포토 다이오드 형성 후에 메탈 배선 라인들(M1 ~ M4) 및 복수의 절연막 형성 및 평탄화 공정을 실시하여야 하므로 이에 따른 불량도 야기된다.

<22> 한편, 종래의 이미지 센서의 경우, 포토 다이오드 주위로 신호처리 및 제어를 위한 다수의 트랜지스터가 배치되어 픽셀 당 빛을 수광하는 면적이 작다. 즉, 픽셀 당 수광영역의 포화도(saturation)가 낮다. 그에 따라, 노이즈가 증가할 수 있고, 또한 노이즈에 따른 이미지 손실의 위험성이 증가되어 화질이 열화되는 문제 등이 발생하고 있다.

발명이 이루고자 하는 기술적 과제

<23> 따라서, 본 발명이 이루고자 하는 기술적 과제는 종래의 이미지 센서의 문제를 해결하여 광감도를 극대화하고 픽셀 당 수광 면적, 즉 포화도를 극대화할 수 있는 후면 조명 구조의 이미지 센서 및 그 이미지 센서 제조방법

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을 제공하는 데에 있다.

발명의 구성 및 작용

<24> 상기 기술적 과제를 달성하기 위하여, 본 발명은 제1 웨이퍼 상에 형성된 포토 다이오드 및 트랜스퍼 게이트 트랜지스터(transfer gate transistor)를 포함하는 포토 다이오드부; 상기 포토 다이오드부 상부로 접합된 제2 웨이퍼 상에 형성된 신호처리 및 제어 트랜지스터 및 배선 라인을 포함하는 배선 라인부; 상기 배선 라인부 상부에 형성된 지지대 기판; 및 상기 제1 웨이퍼 하부에 형성된 필터부;를 포함하는 후면 조명(backside illumination) 구조의 이미지 센서를 제공한다.

<25> 본 발명에 있어서, 상기 제2 웨이퍼는 수소 이온주입(implantation) 공정이 수행된 웨이퍼이고, 상기 배선 라인부는 상기 제2 웨이퍼가 상기 포토 다이오드부 상부에 접합되고 스마트 컷(smart-cut)을 통해 소정 부분이 제거되어 남은 부분에 상기 신호처리 및 제어 트랜지스터 및 배선 라인이 형성되어 이루어질 수 있다. 또한, 상기 제2 웨이퍼는 적층 및 열처리를 통해 상기 포토 다이오드부 상부에 접합될 수 있다.

<26> 한편, 상기 포토 다이오드부는 상기 포토 다이오드 주변 상부로 형성된 플로팅 디퓨전(floating difusion) 영역, 및 상기 포토 다이오드 및 트랜스퍼 게이트 트랜지스터가 형성된 상기 제1 웨이퍼 전면으로 형성된 절연층을 포함할 수 있다. 또한, 상기 신호처리 및 제어 트랜지스터는 소스 팔로어 트랜지스터(source follower transistor), 선택 트랜지스터(selection transistor), 및 리셋 트랜지스터(reset transistor)를 포함할 수 있다.

<27> 본 발명에 있어서, 상기 이미지 센서는 포화도(saturation)를 최대로 하기 위하여, 상기 포토 다이오드부는 1개의 포토 다이오드 당 1개의 트랜지스터(1Tr/pixel)를 갖는 구조를 가진다. 또한, 상기 필터부가 빛을 파장에 따라 투과시키는 필터 어레이(filter array) 및 상기 필터 어레이로 빛을 집광하기 위한 마이크로 렌즈(micro-lens)를 포함하여, 상기 이미지 센서는 상기 필터부를 통해 상기 포토 다이오드로 바로 빛이 입사되는 구조를 갖는다. 이러한 본 발명의 이미지 센서는 빛이 입사되는 상기 포토 다이오드 하부와 반대방향인 상기 포토 다이오드 상부로 상기 배선 라인부가 배치되어 빛에 대한 광감도(sensitivity)가 극대화될 수 있다.

<28> 본 발명은 또한 상기 기술적 과제를 달성하기 위하여, 제1 웨이퍼 상에 포토 다이오드 및 트랜스퍼 게이트 트랜지스터를 포함한 포토 다이오드부를 형성하는 단계; 제2 웨이퍼를 상기 포토 다이오드부 상부로 접합하고 상기 제2 웨이퍼 상에 신호처리 및 제어 트랜지스터 및 배선 라인을 포함하는 배선 라인부를 형성하는 단계; 상기 배선 라인부 상부로 지지대 기판을 접합하는 단계; 및 상기 제1 웨이퍼 하부로 필터부를 형성하는 단계;를 포함하는 후면 조명 구조의 이미지 센서 제조방법을 제공한다.

<29> 본 발명에 있어서, 상기 포토 다이오드부 형성 단계는, 상기 제1 웨이퍼 상에 포토 다이오드를 형성하는 단계; 상기 포토 다이오드 주변 상부로 플로팅 디퓨젼 영역을 형성하는 단계; 상기 포토 다이오드 상부에 상기 트랜스퍼 게이트 트랜지스터 형성하는 단계; 및 상기 제1 웨이퍼 전면으로 절연층을 형성하는 단계;를 포함할 수 있다.

<30> 또한, 상기 제2 웨이퍼는 수소 이온주입 공정이 수행된 웨이퍼이고, 상기 제2 웨이퍼의 접합 및 배선 라인부를 형성하는 단계는, 상기 수소 이온이 주입된 상기 제2 웨이퍼의 상면을 상기 제1 기판과 접합하여 열처리하는 단계; 상기 제2 웨이퍼의 소정 부분을 스마트-컷을 통해 제거하는 단계; 상기 남은 상기 제2 웨이퍼 상에 신호처리 및 제어 트랜지스터를 형성하는 단계; 및 상기 신호처리 및 제어 트랜지스터 상부로 BEOL(Back End Of Line) 공정을 수행하는 단계;를 포함할 수 있다. 여기서, 상기 신호처리 및 제어 트랜지스터는 전술한 바와 같이 소스 팔로어 트랜지스터, 선택 트랜지스터, 및 리셋 트랜지스터를 포함할 수 있다.

<31> 한편, 상기 이미지 센서 제조방법은, 상기 제1 웨이퍼 하부로 필터부를 형성하는 단계 전에 상기 제1 웨이퍼의 하면을 얇게 연마하는 단계를 포함할 수 있는데, 예컨대 상기 제1 웨이퍼는 상기 연마에 의해 10 ㎛ 이하의 두께를 가질 수 있다. 또한, 상기 필터부를 형성하는 단계는 상기 제1 웨이퍼 하부로 빛을 파장에 따라 투과시키는 필터 어레이를 형성하는 단계; 및 상기 필터 어레이 하부로 빛을 집광하기 위한 마이크로 렌즈를 형성하는 단계;를 포함할 수 있다.

<32> 본 발명에 따른 후면 조명 구조의 이미지 센서 및 그 제조 방법은 메탈 배선 라인이 포토 다이오드 전면으로 배치되고 필터부가 후면으로 배치됨으로써, 종래 메탈 배선 라인층의 존재에 인해 발생하던 광감도 저하 문제를 효과적으로 배제시킬 수 있다. 또한, 포토 다이오드부에 하나의 포토 다이오드 당 1개의 트랜지스터만을 포함하는 구조로 형성됨으로써, 수광영역의 포화도를 극대화시킬 수 있다. 더 나아가 제2 웨이퍼를 접합한 후에 트랜

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지스터 및 배선 라인들이 형성됨으로써, 트랜지스터 및 배선들 간의 수직 컨택 또는 비아를 용이하게 형성할 수 있는 장점도 있다.

<33> 도 2는 본 발명의 일 실시예에 따른 후면 조명 구조의 이미지 센서를 개략적으로 보여주는 단면도이다.

<34> 도 2를 참조하면, 본 발명의 이미지 센서는 제1 웨이퍼(110) 상에 형성된 포토 다이오드부(100), 포토 다이오드부(100) 상부의 제2 웨이퍼(210) 상에 형성된 배선 라인부(200), 배선 라인부(200) 상부의 지지대 기판(300) 및 제1 웨이퍼(110) 하부에 형성된 필터부(400)를 포함한다.

<35> 포토 다이오드부(100)는 제1 웨이퍼에 형성된 포토 다이오드(120, PD), 포토 다이오드(120) 주변 상부로 형성된 플로팅 디퓨전(Floating Diffusion: FD) 영역(130)과 포토 다이오드(120) 상부로 신호 전달을 위한 트랜스퍼 게이트(Transfer Gate: TG) 트랜지스터(140)를 포함한다. 한편, 이러한 포토 다이오드(120), 플로팅 디퓨전 영역(130) 및 트랜스퍼 게이트 트랜지스터(140)가 형성된 제1 웨이퍼(110) 상부 전면으로 제1 절연층(150)이 형성되어 있다.

<36> 본 실시예에 따른 이미지 센서의 포토 다이오드부(100)는 포토 다이오드(120) 하나 당 1개의 트랜지스터, 즉 트랜스퍼 게이트 트랜지스터(140)만을 포함하므로, 종래의 이미지 센서에 비해 획기적으로 포화도(saturation)를 증가시킬 수 있다. 여기서 포화도는 단위 픽셀 면적에 대한 수광영역의 면적을 나타내는 것으로 필 펙터(fill factor)라고도 한다. 종래의 이미지 센서는 포토 다이오드가 형성된 수광영역 주위로 다수의 신호 처리 및 제어를 위한 트랜지스터들이 형성되어 낮은 포화도를 가지고 있었다. 그러나 본 실시예의 이미지 센서는 단지 트랜스퍼 게이트 트랜지스터 하나만 형성되기 때문에 포화도가 극대화될 수 있다.

<37> 배선 라인부(200)는 포토 다이오드부(100) 상부로 형성되는데, 제2 웨이퍼(210) 상에 형성된 신호처리 및 제어 트랜지스터(220), 다층의 배선 라인(230) 및 트랜지스터와 배선 라인 또는 배선 라인들 간을 전기적으로 연결하는 수직 컨택 또는 비아(240)를 포함한다. 한편, 전술한 바와 같이 제2 웨이퍼(210) 상부로는 제2 절연층(250)이 형성되며, 이러한 제2 절연층(250)은 전술한 바와 같이 상이한 절연 물질이 사용된 다수의 절연막들로 구성될 수 있다.

<38> 여기서, 신호처리 및 제어 트랜지스터(220)는 트랜스퍼 게이트 트랜지스터(140)를 제외한 소오스 팔로어(source follower) 트랜지스터, 선택(selection) 트랜지스터, 리셋(reset) 트랜지스터 등이 될 수 있다. 트랜스퍼 게이트 트랜지스터(140)를 비롯한 이러한 신호처리 및 제어 트랜지스터(220)는 수직 컨택 또는 비아(240)를 통해 배선 라인(230)과 연결되게 된다.

<39> 도 2 부분에서 좀더 상세히 설명하겠지만, 본 실시예에 따른 수직 컨택 또는 비아(240)는 포토 다이오드부(100) 상부로 제2 웨이퍼가 접합된 후에 배선 라인(230) 공정과 함께 형성되기 때문에 얼라인을 맞추기 쉽고 그에 따라 수직 컨택 또는 비아(240)가 대우 작은 선폭을 가지고 형성될 수 있다.

<40> 배선 라인부(200) 상부로는 지지대 기판(300)이 접합 되는데, 지지대 기판(300)은 전체 이미지 센서를 지지하는 기능을 한다.

<41> 제1 웨이퍼(110) 하부로 형성되는 필터부(400)는 빛을 파장에 따라 투과시키는 레드(red), 그린(green), 블루(blue)와 같은 컬러 필터 어레이(410) 및 필터 어레이(410) 하부로 빛을 집광하기 위한 마이크로 렌즈(420)를 포함한다.

<42> 본 실시예의 이미지 센서는 포토 다이오드가 형성된 제1 웨이퍼(110) 하부로 필터부가 형성되어 빛(A)이 웨이퍼(110)의 하부로 입사되는 후면 조명(backside illumination) 구조를 갖는다. 그에 따라, 종래 전면 조명 구조에서 빛이 배선 라인층을 거치면서 발생 되었던 문제, 즉 난반사나 굴절률 차이 등에 의해 발생하던 광감도 저하 문제를 획기적으로 해결할 수 있다. 한편, 제1 웨이퍼의 배면을 연마하여 제1 웨이퍼를 수 ㎛ 이하로 얇게 함으로써, 빛의 입사 거리를 짧게 할 수 있고 그에 따라 더욱 광감도를 향상시킬 수 있는 장점을 갖는다.

<43> 도 3a ~ 3i는 본 발명의 다른 실시예에 따른 후면 조명 구조의 이미지 센서 제조방법을 보여주는 단면도들이다.

<44> 도 3a를 참조하면, 먼저 제1 웨이퍼(110a) 상에 포토 다이오드(120), 플로팅 디퓨전 영역(130) 및 트랜스퍼 게이트 트랜지스터(140)를 형성하고, 제1 웨이퍼(100a) 상부 전면으로 제1 절연층(150)을 형성하여 포토 다이오드부(100)를 완성하게 된다.

<45> 도 3b를 참조하면, 제1 웨이퍼와 다른 제2 웨이퍼(210a)를 준비하고 제2 웨이퍼(210a)에 수소 이온주입(B, hydrogen implantation) 공정을 수행한다. 이러한 수소 이온주입 공정은 차후에 스마트 컷(smart cut)을 통해

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제2 웨이퍼의 소정 부분을 절단하여 제거하기 위해 수행된다. 여기서 점선부분(212)으로 수소 이온이 주입되고 차후에 점선부분(212)으로 웨이퍼가 절단된다.

<46> 도 3c를 참조하면, 수소 이온주입 공정이 수행된 제2 웨이퍼(210a)를 포토 다이오드부(100) 상부로 접합하고 열처리를 수행한다. 즉, 제2 웨이퍼(210a)를 포토 다이오드부(100)로 밀착 적층하고 적절한 온도로 열처리를 행하는데, 이러한 열처리를 통해서 제2 웨이퍼의 소정부분, 즉 점선부분(212) 상부를 분리하여 제거하게 된다. 이러한 방법을 스마트 컷(smart cut)이라고 한다. 이러한 스마트 컷을 위한 열처리는 예컨대 300 ~ 600 ℃ 정도로 행할 수 있다.

<47> 도 3d를 참조하면, 포토 다이오드부(100) 상부로 소정 부분이 제거된 제2 웨이퍼(210)가 적층되어 있음을 볼 수 있는데, 제2 웨이퍼의 접합을 견고하게 하기 위하여 다소 고온의 열처리를 더 행할 수도 있다.

<48> 도 3e를 참조하면, 접합된 제2 웨이퍼(210) 상부로 신호처리 및 제어를 위한 다수의 트랜지스터(220)를 형성한다. 예컨대, 신호처리 및 제어 트랜지스터(220)는 트랜스퍼 게이트 트랜지스터를 제외한 소스 팔로어 트랜지스터, 선택 트랜지스터 및 리셋 트랜지스터 등이 될 수 있다. 한편, 이러한 신호처리 및 제어 트랜지스터(220) 상부로는 제1 배선 라인(232) 등이 형성될 수 있는데, 이러한 제1 배선 라인(232) 형성 전에 수직 컨택 또는 비아(240)를 형성하여 신호처리 및 제어 트랜지스터(220)와 트랜스퍼 게이트 트랜지스터(140)를 제1 배선 라인(232)으로 전기적으로 연결 되도록 한다.

<49> 도 3f를 참조하면, 제1 배선 라인(232) 상부로 제2 및 제3 배선 라인(234, 236) 등의 다층의 배선 라인들이 더 형성될 수 있고, 이러한 제2 및 제3 배선 라인(234, 236)들도 수직 컨택 또는 비아(240)를 통해 전기적으로 연결됨은 물론이다. 여기서, 배선 라인(230)으로 3개의 배선 라인들을 예로 들어 설명하였지만 그 미만의 배선 라인층 또는 더 많은 배선 라인층으로 배선 라인(230)이 형성될 수 있음은 물론이다.

<50> 이와 같은, 배선 라인(230) 공정, 즉 BEOL(Back End of Line) 공정이 완료하여 배선 라인부(200)를 완성한다. 여기서, 제2 절연층(250)이 하나로 층으로 표현되고 있지만, 전술한 바와 같이 전체 배선 라인(230)이 다층의 배선 라인들로 형성되므로 배선 라인들 사이 사이의 층간 절연막들이 다른 재질의 절연재료로 형성될 수 있음은 물론이다.

<51> 도 3g를 참조하면, BEOL 공정이 완료된 배선 라인부(200) 상부로 제3 웨이퍼, 즉 지지대 기판(300)을 접합하게 되는데, 이러한 지지대 기판(300)은 전체 이미지 센서에 대한 지지대 역할을 하게 된다. 접합은 앞서 제2 웨이퍼의 접합과 마찬가지로 밀착시켜 다소 고온의 열처리 등을 통해서 이루어진다. 물론 지지대 기판은 전체적으로 이용되므로 스마트 컷과 같은 공정은 진행되지 않는다.

<52> 도 3h를 참조하면, 포토 다이오드부(100)가 형성된 제1 웨이퍼(110a)의 하면을 연마한다. 이러한 연마를 통해 제1 웨이퍼의 두께를 수 ㎛, 예컨대 10 ㎛ 이하의 정도로 만들 수 있다. 그에 따라, 차후 제1 웨이퍼(110) 하부로 형성되는 필터부를 통해 입사되는 빛의 경로를 최소화하여 포토 다이오드(120)의 감광도를 극대화할 수 있다.

<53> 도 3i를 참조하면, 제1 웨이퍼(110) 하면으로 필터부(400)를 형성한다. 즉, 컬러 필터 어레이(410) 및 마이크로 렌즈(420)를 형성한다.

<54> 본 실시예의 이미지 센서 제조방법은 빛이 입사하는 필터부(400)와 반대 방향으로 배선 라인부(200)를 형성함으로써, 종래 빛이 배선 라인층을 거치면서 난반사나 절연막들 사이의 굴절율 차이에 기인한 광감도 저하문제를 효과적으로 배제시킬 수 있다. 또한, 제2 웨이퍼를 포토 다이오드부(100)로 접합한 후에 배선 라인부(200)가 형성되기 때문에, 트랜스퍼 게이트 트랜지스터, 신호처리 및 제어 트랜지스터와 배선 라인들 간의 수직 컨택 또는 홀을 작은 선폭을 가지고 용이하게 형성할 수 있다.

<55> 한편, 본 실시예의 이미지 센서 제조방법은 포토 다이오드부가 포토 다이오드 하나당 1개의 트랜지스터, 즉 트랜스퍼 게이트 트랜지스터만을 포함하도록 형성하므로 수광영역의 포화도를 극대화시킬 수 있는 장점을 가진다.

<56> 지금까지, 본 발명을 도면에 도시된 실시예를 참고로 설명하였으나 이는 예시적인 것에 불과하며, 본 기술 분야의 통상의 지식을 가진 자라면 이로부터 다양한 변형 및 균등한 타 실시예가 가능하다는 점을 이해할 것이다. 따라서 본 발명의 진정한 기술적 보호 범위는 첨부된 특허청구범위의 기술적 사상에 의해 정해져야 할 것이다.

발명의 효과

<57> 이상에서 상세히 설명한 바와 같이 본 발명에 따른 후면 조명 구조의 이미지 센서 및 그 제조 방법은 메탈 배선

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라인이 포토 다이오드 전면으로 배치되고 필터부가 후면으로 배치됨으로써, 종래 메탈 배선 라인층의 존재에 인해 발생하던 광감도 저하 문제를 효과적으로 배제시킬 수 있다.

<58> 또한, 포토 다이오드부에 하나의 포토 다이오드 당 1개의 트랜지스터만을 포함하는 구조로 형성됨으로써, 수광 영역의 포화도를 극대화시킬 수 있다.

<59> 더 나아가 제2 웨이퍼를 접합한 후에 트랜지스터 및 배선 라인들이 형성됨으로써, 트랜지스터 및 배선들 간의 수직 컨택 또는 비아를 용이하게 형성할 수 있는 장점을 갖는다.

도면의 간단한 설명

<1> 도 1은 종래의 3차원 집적(3D-integration) 방식의 CMOS 이미지 센서를 개략적으로 보여주는 단면도이다.

<2> 도 2는 본 발명의 일 실시예에 따른 후면 조명 구조의 이미지 센서를 개략적으로 보여주는 단면도이다.

<3> 도 3a ~ 3i는 본 발명의 다른 실시예에 따른 후면 조명 구조의 이미지 센서 제조방법을 보여주는 단면도들이다.

<4> <도면에 주요부분에 대한 설명>

<5> 100: 포토 다이오드부 110,110a:제1 웨이퍼

<6> 120: 포토 다이오드 130: 플로팅 디퓨전 영역

<7> 140: 트랜스퍼 게이트 트랜지스터 150: 제1 절연층

<8> 200: 배선 라인부 210,210a: 제2 웨이퍼

<9> 220: 신호처리 및 제어 트랜지스터 230: 배선 라인

<10> 232: 제1 배선 라인 234: 제2 배선 라인

<11> 236: 제3 배선 라인 240: 수직 컨택 또는 비아

<12> 250: 제2 절연층 300: 지지대 기판

<13> 400: 필터부 410: 필터 어레이

<14> 420: 마이크로 렌즈

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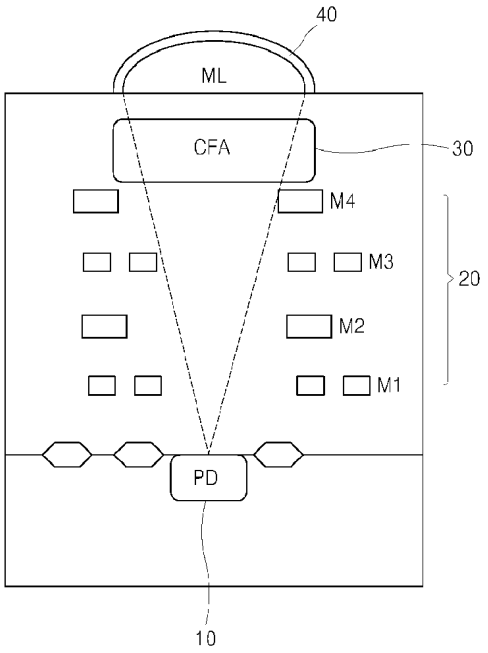
도면

도면1



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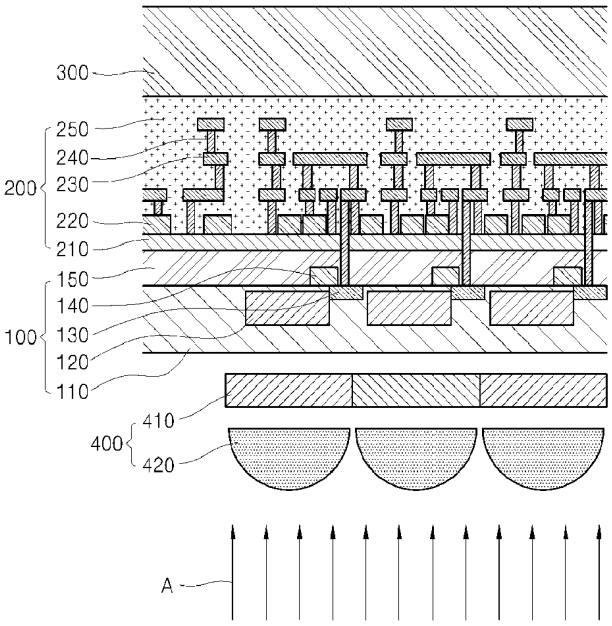

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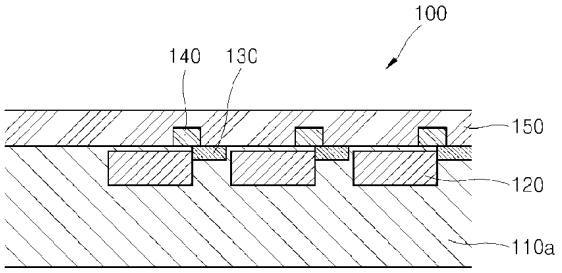
도면3a



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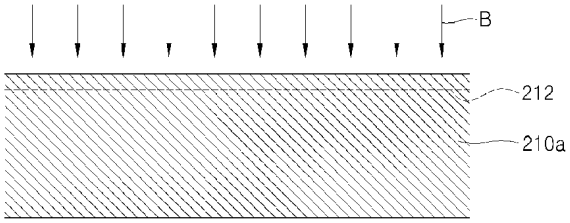

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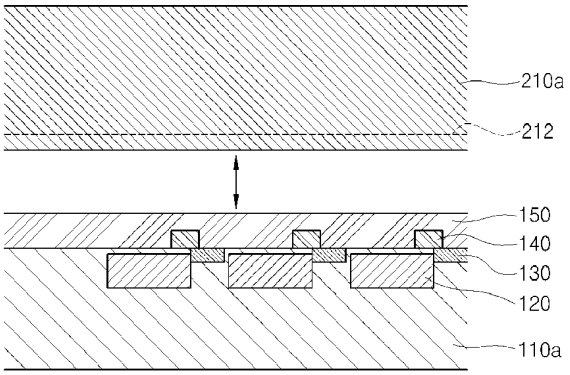
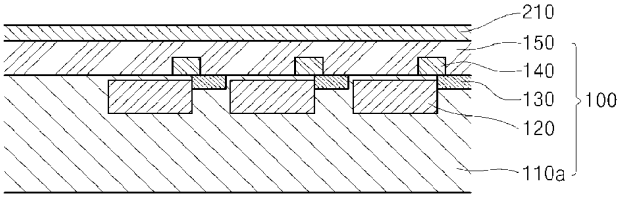


도면3d



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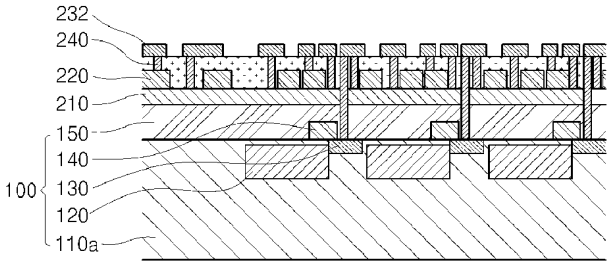
도면3e



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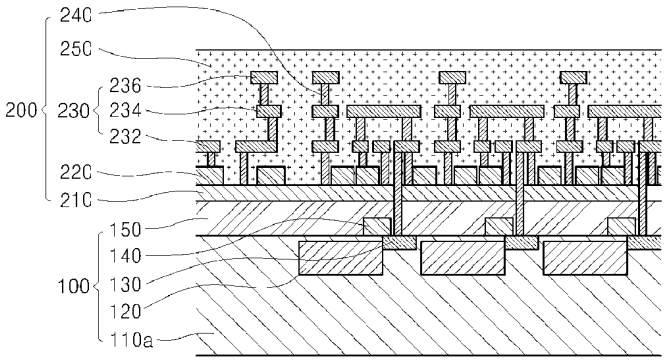

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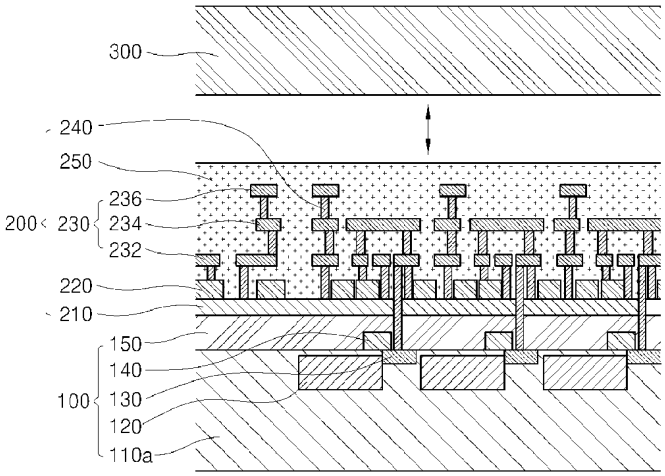

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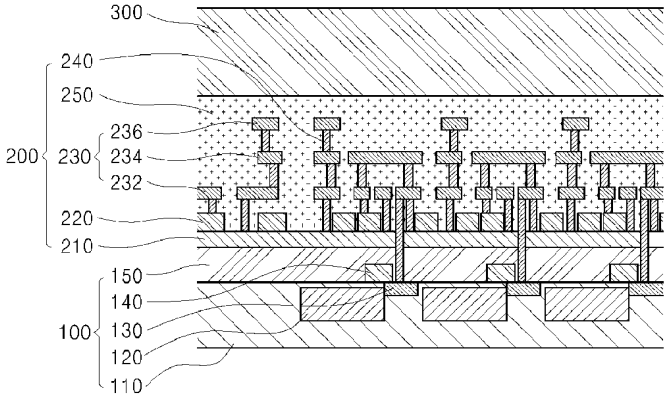

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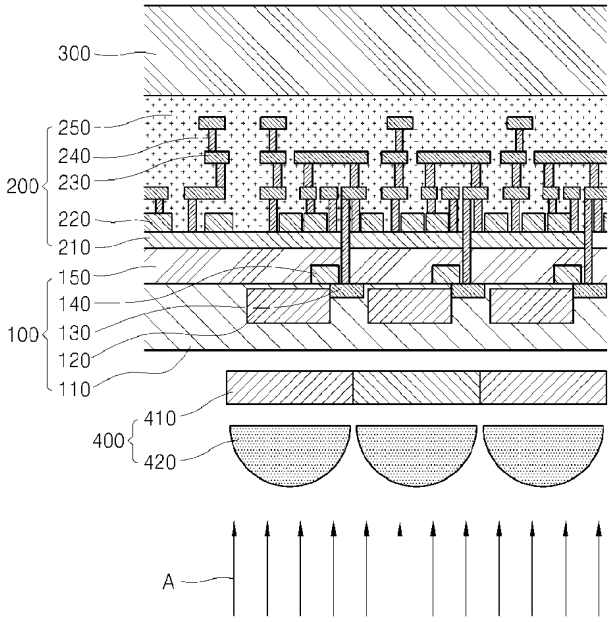

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Examined Patent Publication(B1)

Bibliographic Data

Int.Cl.	H01L 31/04 | H01L 31/0236 | H01L 31/18
Published Date	20140422
Registration No.	1013877150000
Registration Date	20140415
Application No.	1020080003122
Application Date	20080110
Unexamined Publication No.	1020090077274
Unexamined Publication Date	20090715
Requested Date of Examination	20121129
Agent.	PARK, Byung Chang
Inventor	CHOI, Chul Chae | KIM, Hye Won | YOON, Phil Won | KIM, Jin Sung
Applicant	LG Electronics Inc.
Rightholder	LG Electronics Inc.

발명의 명칭

나노 텍스쳐링 구조를 갖는 반도체 웨이퍼 기판을 포함하는벌크형 태양전지의 제조방법

Title of Invention

The bulk type method for manufacturing solar cell including the semiconductor wafer substrate having the nano texturing structure.

요약

본 발명에 따르면, 벌크형 태양전지에 포함되는 실리콘 웨이퍼 기판 상에 나노 텍스쳐링(texturing) 구조를 형성하는 방법에 있어서, 금속 나노 입자를 촉매로 하는 에칭법을 이용하여 상기 나노 텍스쳐링 구조를 형성함으로써 우수한 특성을 갖는 반사 방지막을 손쉽게 얻을 수 있는 벌크형 태양전지의 제조방법이 제공된다. 본 발명에 따르면, 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서, 상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되, 상기 나노 텍스쳐링 구조 형성 단계는 금속을 촉매로 하는 에칭법에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법이 제공된다.

나노 텍스쳐링, 나노 금속, 촉매, 에칭, 태양전지

Abstract

According to the present invention, provided is the bulk type method for manufacturing solar cell which easily can obtain the reflection barrier layer which has the excellent characteristic by forming the nano texturing structure as to the method for forming the nano texturing structure on the silicon wafer substrate included in the bulk type solar cell using the etching method the metal nanoparticle to the catalyst. According to the present invention, provided is the bulk type method for manufacturing solar cell which includes the step of forming the nano texturing structure of having the pattern of the nano-size on the silicon wafer substrate surface as to the bulk type method for manufacturing solar cell including the silicon wafer substrate and in which the nano texturing structure formation step is performed with the etching method the metal to the catalyst.

The nano texturing, the nano metal, the catalyst, the etching, the solar cell

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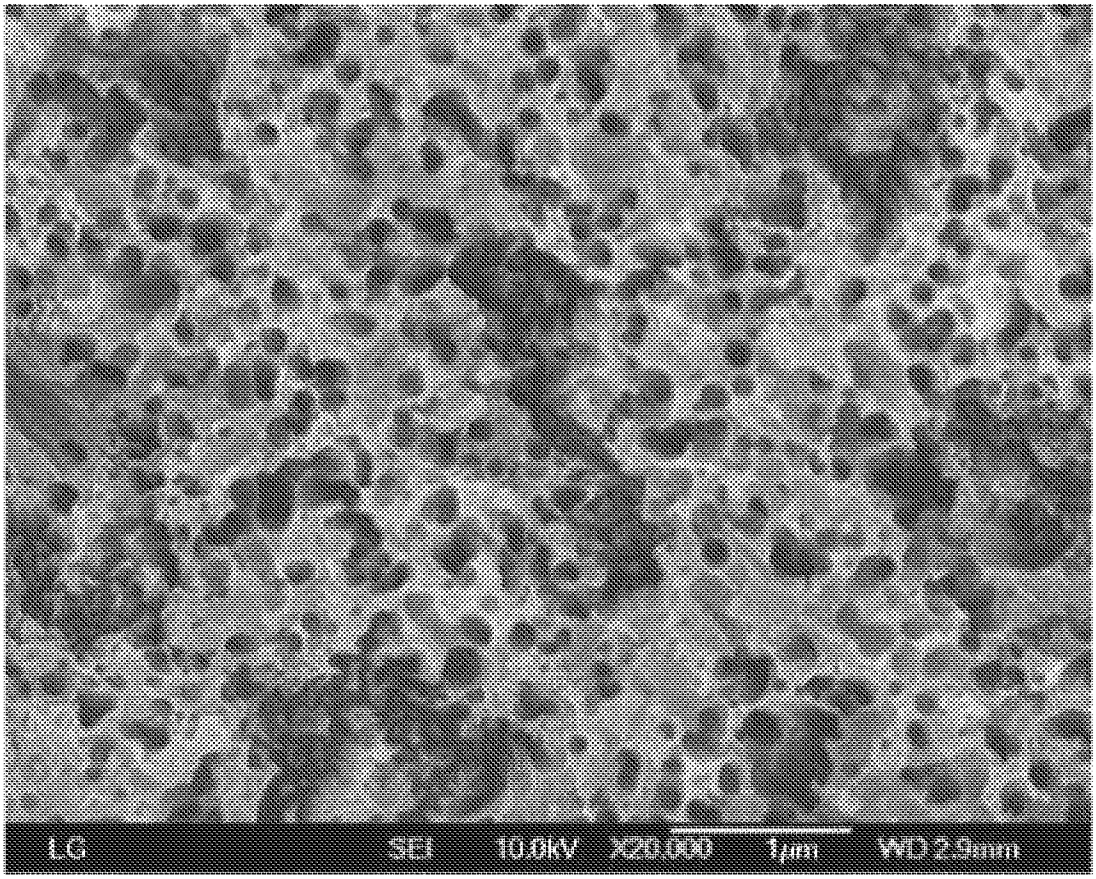
대표도면(Representative drawing)



청구의 범위

청구 **1**항:

실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서, 상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되, 상기 나노 텍스쳐링 구조 형성 단계는 금속을 촉매로 하는 에칭법에 의해 수행되고, 상기 나노 텍스쳐링 구조 형성 단계는, 나노 금속 입자들이 혼합되어 있는 용액을 상기 실리콘 웨이퍼 기판 상에 분산시키는 단계;열처리에 의하여 상기 용액을 건조시켜 상기 나노 금속입자들이 사이로 상기 실리콘 웨이퍼 기판이 노출되도록 상기 나노 금속 입자들을 남기는 단계; 에칭액을 사용하여 상기 나노 금속 입자들 사이에 노출된 상기 실리콘 웨이퍼 기판을 에칭하는 단계; 및상기 나노 금속 입자들을 제거하는 단계를 포함하는 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구 **2**항:

삭제

청구 **2**항:

Scope of Claims

Claim 1:

The bulk type method for manufacturing solar cell comprising the silicon wafer substrate, wherein the bulk type method for manufacturing solar cell is characterized by comprising the step: step: step: of etching the silicon wafer substrate exposed using the etchant between nano metal particles and the step of removing nano metal particles that nano metal particles leave nano metal particles the silicon wafer substrate is exposed by the interval it dries the solution with the thermal process that the nano texturing structure formation step disperses the solution in which nano metal particles are mixed on the silicon wafer substrate the nano texturing structure formation step is performed with the etching method the metal to the catalyst it includes the step of forming the nano texturing structure of having the pattern of the nano-size on the silicon wafer substrate surface.

Claim 2:

Deletion.

Claim 2:

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삭제

Deletion.

청구 **3**항:

Claim 3:

제1항에 있어서, 상기 나노 금속 입자들의 입경은 20nm 내지 200nm인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 1, the bulk type method for manufacturing solar cell in which the particle diameter of nano metal particles is 20nm to 200nm.

청구 **4**항:

Claim 4:

제1항에 있어서, 상기 나노 금속 입자들은 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 중 적어도 하나인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 1, the bulk type method for manufacturing solar cell in which nano metal particles are at least one among the gold (Au), silver (Ag), copper (Cu), pailadium (Pd), tin (Sn).

청구 **5**항:

Claim 5:

제1항에 있어서, 상기 에칭액은 플루오르화 수소(HF)와 과산화수소수(H2O2)의 혼합용액인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 1, the bulk type method for manufacturing solar cell in which the etchant is the mixture of the hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/SB)) and hydrogen fluoride (HF).

청구 **6**항:

Claim 6:

제5항에 있어서, 상기 플루오르화 수소(HF)와 과산화수소수(H2O2)의 혼합비는 10:1인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 5, the bulk type method for manufacturing solar cell in which the mixing ratio of the hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/SB)) and hydrogen fluoride (HF) is 10:1.

청구 **7**항:

Claim 7:

제1항에 있어서, 상기 용액에서 상기 나노 금속 입자들의 농도는 1000ppm 내지 100000ppm 인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 1, the bulk type method for manufacturing solar cell in which the concentration of nano metal particles is 1000ppm to 100000ppm in the solution.

청구 **8**항:

Claim 8:

제1항에 있어서, 상기 나노 금속 입자들이 혼합되어 있는 용액을 분산시키는 단계는, 스프레이법(spraying), 스핀코팅법(spin coating), 디핑법(dipping) 중 어느 하나에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 1, the bulk type method for manufacturing solar cell performed by any one of step, of dispersing the solution in which nano metal particles are mixed is the spraying, the spin coating method, and the dipping method.

청구 **9**항:

Claim 9:

제1항, 그리고 제3항 내지 제8항 중 어느 하나의 제조방법으로 제조된 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 포함하는 벌크형 태양전지.

The bulk type solar cell including the nano texturing structure of having the pattern of the nano-size on the silicon wafer substrate surface manufactured with one manufacturing method among the claims 1 and 3 through 8.

기술분야

Technical Field

본 발명은 벌크형 태양전지의 제조방법에 관한 것이다. 보다 상세하게는 벌크형 태양전지에 포함되는 실리콘 웨이퍼 기판 상에 나노 텍스쳐링(texturing) 구조를 형성하는 방법에 있어서, 금속 나노 입자를 촉매로 하는 에칭법을 이용하여 상기 나노 텍스쳐링 구조를 형성함으로써 우수한 특성을 갖는 반사방지막을 손쉽게 얻을 수 있는 벌크형 태양전지의 제조방법에 관한 것이다.

The present invention relates to the bulk type method for manufacturing solar cell. More specifically, it is about the bulk type method for manufacturing solar cell which easily can obtain the reflection barrier layer which has the excellent characteristic by forming the nano texturing structure as to the method for forming the nano texturing structure on the silicon wafer substrate included in the bulk type solar cell using the etching method the metal nanoparticle to the catalyst.

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배경기술

태양전지는 포토다이오드의 일종으로 태양광을 직접 전력으로 전환시키는 목적에 이용되고 있어, 대체 에너지원으로서 지상에서는 물론이고 우주개발을 위해서도 그 이용이 점차 확대되어가고 있어 전력용 전자소자로서 매우 중요하다. 그 구조도 p-n 접합형, 쇼트키 배리어형 및 이종(異種)반도체의 접합으로 이루어지는 것 등이 있으며, 소재로서는 실리콘#183#갈륨비소 등의 결정체, 기타 각종 반도체가 광범위하게 이용되고 있다. 특히 근래에 와서는 다결정(多結晶) 실리콘이나 비정질(非晶質) 실리콘을 이용한 태양전지의 개발과 실용화가 크게 각광을 받고 있다.

그러나 높은 광전변환효율과 품질특성 때문에 단결정의 실리콘 웨이퍼를 기반으로하는 벌크형 태양전지가 상용화되고 있는 실정이다.

일반적으로 실리콘 결정계(crystalline) 태양전지는 실리콘 웨이퍼를 출발 원료로 한다. 실리콘 웨이퍼는 고순도로 정제된 실리콘을 고온으로 가열하여 결정으로 성장된 잉곳을 만들고 이를 절단 및 연마를 통해 대형의 결정판 형태의 웨이퍼 기판을 만든다. 결정은 원자가 규칙적으로 배열된 물질을 의미한다.

종래의 태양전지를 제조하기 위한 웨이퍼의 처리 방법 중 가장 중요한 처리는 기판 표면의 텍스처링(texturing), 즉 조직화이다. 이러한 텍스처링의 목적은 빛을 받는 태양전지의 전면부에서의 반사율을 감소시키고, 태양전지 내에서 빛의 통과 길이를 길게 함으로써 태양전지 내부로 빛이 흡수되도록 하여 효율을 향상시키고자 하는 것이다. 한편, 기판 상에 광학 박막을 형성시켜 반사방지막으로서의 기능을 하게 할 수도 있다.

텍스처링된 종래의 태양전지용 웨이퍼 기판의 표면을 확대한 단면도는 도 1a에 도시하였다. 텍스처링한 후의 표면은 피라미드 구조를 가지므로 옆면에서 관찰할 때 정삼각형의 형상을 가진다.

종래 기술에 의하면, 경면 연마처리(Polishing)된 웨이퍼 표면은 입사되는 태양 빛의 30% 내지 50% 정도를 반사시키고, 표면을 피라미드 형태로 조직화(texturing)시키면 입사되는 태양광의 10% 내지 20% 정도를 반사하게 되어 반사율이 현저하게 줄어든다. 또한, 조직화시킨 표면에 반사방지막(anti-reflection, AR)을 증착시키면 반사율을 약 5% 내지 10%까지 감소시킬 수 있는 것으로 알려져 있다.

그러나, 상기 반사율은 태양광의 주요 흡수 파장대역인 500nm 내지 1000nm 에서관찰된 평균값으로서, 태양광 파장범위의 낮은 파장영역인 300nm 내지 400nm에서는 비교적 높은 반사도를 가지며, 반사방지막의 증착 이후라야만 비로소 상대적으

Background Art

The solar cell is used to the purpose of converting the sunlight into the direct electricity as a kind of the photo diode and it is in ground and the usage is gradually expanded as the alternation energy source for the space development and the purpose is important as the electric power electric component. It has to be made of the structure is the p-n heterogeneous, and the junction of the inhomogeneous semiconductor and schottky barrier type and crystal, the other all kinds of semiconductor including silicone · the GaAs etc. are extensively used as the material. Particularly, recently, development and put to practical use of the solar cell coming and uses the poly-crystal silicon or the amorphous silicon are in the spotlight.

But the high photoelectric conversion efficiency and the bulk type solar cell which therefore has the silicon wafer of the monocrystal as the base with quality characteristic are commercialized.

Generally, the silicon crystal (crystalline) solar cell the silicon wafer to the starting raw material. The silicone refined to the high purity is heated with the high temperature and the silicon wafer makes the ingot grown up to the Decision and this the wafer substrate of the definitive edition form of the large size is made through the cut and grinding. The material in which the atom as to the Decision, is regularly arranged is meant.

Most, the important processing is the texturing of the substrate surface, in other words, the organizing among the processing method of the wafer for manufacturing the conventional solar cell. The reflectivity at the front surface of the solar cell in which the object of such texturing receives light is decreased and Light is absorbed in the solar cell into the solar cell inside by drawing the passing length of light and to improve the efficiency. In the meantime, the optical thin film is formed on the substrate and it functions as the reflection barrier layer.

The cross-sectional view enlarging the surface of the wafer substrate for the textured conventional solar cell showed in the drawing 1a. When observing in side since the surface of the texturing has the pyramid structure it has the shape of the regular triangle.

According to the prior art, 30% of the sunlight in which the wafer surface which becomes with the mirror-polishing processing (Polishing) is incoming to about 50% is reflected and 10% of the sunlight which is incoming if it orders the surface through the pyramid shape with the organizing (texturing) to about 20% is reflected and reflectivity remarkably decreases. Moreover, it is known that reflectivity can be reduced to about 5% to 10% if the reflection barrier layer (anti-reflection, AR) is evaporated in the surface structured.

But reflectivity includes the relatively high reflectivity in 300nm which is 500nm which is the major absorption wavelength band of the sunlight to the average value which becomes with 1000nm west observation and is t

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로 더 낮은 반사도를 갖게 되는 문제점을 가지고 있다. 따라서, 모든 태양광의 파장영역에서 균일하게 낮은 반사율을 갖는 기판 표면을 형성하고자 하는 연구가 진행되었고, 그 결과 나노 구조를 갖는 나노 텍스쳐링 구조가 형성된 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지가 개발되었다.

he low wavelength area of the sunlight wavelength range. To 400nm, and the problem of having the reflectivity which is relatively lower as the deposition after of the reflection barrier layer at last. Therefore, in the wavelength area of all sunlights, the research to form the substrate surface having the low reflectivity proceeded and the bulk type solar cell including the silicon wafer substrate in which the nano texturing structure consequently of having the nanostructure was formed was developed.

이러한 나노 텍스쳐링 구조를 갖는 종래 태양전지용 실리콘 웨이퍼 기판의 표면을 확대한 이미지는 도 1과 같다. 도 1을 참조하면 조직화된 웨이퍼 기판 상에는 피라미드 형태의 나노 구조가 형성되어 있음을 알 수 있다.

The image enlarging the surface of the conventional solar battery use silicone wafer substrate having such nano texturing structure is same as those of fig. 1. Referring to Figure 1, it can know that the nanostructure of the pyramid shape is formed on the wafer substrate which becomes systemized.

이러한 나노 텍스쳐링 구조로 형성되는 반사방지막은 넓은 파장영역 및 넓은 입사각 범위에서 반사 방지막으로서의 기능을 수행한다. 종래에는 이러한 나노 텍스쳐링 구조를 형성하기 위해 진공 중에서 염소(Cl) 기체 또는 플루오르화 황(SF6)을 이용하여 반응성 이온 에칭(RIE; Reactive Ion Etching)을 수행하거나, 실리콘 웨이퍼 기판 표면에 금속을 매우 얇게 증착한 후 습식에칭을 수행하였다.

The function as the reflection barrier layer is performed in the wavelength area in which the reflection barrier layer formed into such nano texturing structure is broad and the wide incidence angular range. Conventionally, in order to form the nano texturing structure of being like that the reactive ion etch (RIE: Reactive Ion Etching) was performed among the vacuum using the chlorine (Cl) gas or the sulfonicfluoride (SF(SB)6(/SB)) or it was very thin the metal the wet etching was performed in the silicon wafer substrate surface after doing the deposition.

그러나, 상기 방법 중 반응성 이온 에칭법을 이용하는 방법은 복잡하고 값비싼 장비를 필요로 하는 진공 공정이 필수적이라는 문제가 있다. 한편, 습식 에칭을 이용하는 방법은 금속과 에칭액과의 촉매반응으로 실리콘을 에칭하여 나노 텍스쳐링 구조를 형성하는 방식으로 반응성 이온 에칭(RIE)을 이용하는 방식보다 공정상 간단하다는 장점이 있다. 그러나, 이 방법 또는 진공 장비를 사용하여야 하는 문제가 있다.

But it has the problem the vacuum process which need the expensive equipment in which the method for using the reactive ion etching method among the method is complicated and is essential. In the meantime, the wet etching is used. And a method has the advantage that is simple than the mode which uses with eutectic phase the metal, and the mode etching the silicone to the catalyst reaction with the etchant and forms the nano texturing structure the reactive ion etch (RIE). But there is a problem that it does using this method or the vacuum equipment.

따라서, 진공 장비 등을 사용하지 않기 위하여 실리콘에 전기도금 방식을 이용하여 금속을 얇게 도금한 후 이를 에칭하여 위와 같은 방법으로 나노 텍스쳐링 구조를 형성시키기도 한다.

Therefore, in order not to use the vacuum equipment etc., it thins this the metal is etched using the electro plating after doing plating and the nano texturing structure is formed into the method as in the above in the silicone.

한편, 실리콘 웨이퍼 기판 표면에 나노 텍스쳐링 구조를 형성시키는 또 다른 방법으로는 황 가스 분위기에서 실리콘 웨이퍼 기판 표면에 엑시머 레이저를 조사함으로써 나노 텍스쳐링 구조를 형성하는 방법이 있다.

In the meantime, in another method for forming the nano texturing structure in the silicon wafer substrate surface the sulfur gas atmosphere, it has the method for forming the nano texturing structure by irradiating the excimer laser in the silicon wafer substrate surface.

또한, 나노 텍스쳐링 구조가 아닌 복수 개의 홀로 이루어지는 다공성 구조를 실리콘 웨이퍼 기판에 형성시킴으로써 반사방지막을 형성하기도 한다. 그러나, 이 방법은 기판 표면에 다공성 구조를 형성시키기 위해 전기분해장치 등 복잡한 장치를 이용한 공정을 필요로 한다는 문제가 있다.

Moreover, by forming the porous structure of being alone made of being not nano texturing structure of multiple in the silicon wafer substrate the reflection barrier layer is formed. But this method has the problem that the process of using the apparatus complicated with the electrolysis device etc. in order to form the porous structure in the substrate surface, is required.

따라서, 간단한 공정만으로도 우수한 특성을 가지는 텍스쳐링 구조를 형성시킬 수 있는 기술에 대한 개발이 필요하다.

Therefore, the development about the technology forming the texturing structure of having the excellent

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characteristic into the simple process is.

발명의 내용

Summary of Invention

해결하고자 하는 과제

Problem to be solved

본 발명은 상술한 바와 같은 종래 기술의 문제점을 해결하기 위한 것으로, 진공공정 등의 필요없이 간소화된 공정만으로 실리콘 웨이퍼 기판 표면에 우수한 반사방지 특성을 갖는 나노 텍스쳐링 구조를 형성시킬 수 있는 벌크형 태양전지의 제조방법을 제공하는 데에 그 목적이 있다.

It has the purpose to provides the bulk type method for manufacturing solar cell forming the nano texturing structure of having the excellent anti-reflection property on the silicon wafer substrate surface into the process of becoming streamlined without the need including the vacuum process etc. the invention solves the problem of the prior art as described above.

과제해결 수단

Means to solve the problem

상술한 목적을 달성하기 위한 본 발명의 일 실시형태에 따르면, 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서, 상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되, 상기 나노 텍스쳐링 구조 형성 단계는 금속을 촉매로 하는 에칭법에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법이 제공된다.

The step of forming the nano texturing structure of having the pattern of the nano-size on the silicon wafer substrate surface is included as to the bulk type method for manufacturing solar cell including the silicon wafer substrate for achieving the above-described purpose. The bulk type method for manufacturing solar cell performed by the etching method in which the nano texturing structure formation step the metal to the catalyst is provided.

상기 나노 텍스쳐링 구조 형성 단계는, 나노 금속 입자가 혼합되어 있는 용액을 상기 실리콘 웨이퍼 기판 상에 분산시키는 단계, 에칭액을 사용하여 상기 나노 금속 입자가 분산된 실리콘 웨이퍼 기판을 에칭하는 단계, 및 상기 나노 금속 입자를 제거하는 단계를 포함할 수 있다.

The nano texturing structure formation step comprises the step of dispersing the solution, and the step of etching the silicon wafer substrate and the step of removing the nano metal particle. As to the step of, the nano metal particle is mixed on the silicon wafer substrate. As to the step of, the nano metal particle is dispersed using the etchant.

상기 나노 금속 입자의 입경은 20nm 내지 200nm로 하는 것이 바람직하다.

It is the be desirable that the particle diameter of the nano metal particle is done by 20nm to 200nm.

상기 나노 금속 입자는 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 중 적어도 하나로 하는 것이 바람직하다.

It is the be desirable that the nano metal particle is done by at least one among the gold (Au), silver (Ag), copper (Cu), palladium (Pd), tin (Sn).

상기 에칭액은 플루오르화 수소(HF)와 과산화수소수(H2O2)의 혼합용액인 것이 바람직하다.

The etchant is the be desirable the mixture of the hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/SB)) and hydrogen fluoride (HF).

상기 플루오르화 수소(HF)와 과산화수소수(H2O2)의 혼합비는 10:1로 하는 것이 바람직하다.

It is the be desirable that the mixing ratio of the hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/SB)) and hydrogen fluoride (HF) is done by 10:1.

상기 용액에서 상기 나노 금속 입자의 농도는 1000ppm 내지 100000ppm 으로 하는 것이 바람직하다.

In the solution, it is the be desirable that the concentration of the nano metal particle is done by 1000ppm to 100000ppm.

상기 나노 금속 입자가 혼합되어 있는 용액을 분산시키는 단계는, 스프레이법(spraying), 스핀코팅법(spin coating), 디핑법(dipping) 중 어느 하나에 의해 수행될 수 있다.

It can be performed by any one of step, of dispersing the solution in which the nano metal particle is mixed is the spraying, the spin coating method, and the dipping method.

상기 목적을 달성하기 위한 본 발명의 벌크형 태양전지는 상기의 제조방법으로 제조되고 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 포함할 수 있다.

The nano texturing structure of the bulk type solar cell of the invention for achieving the purpose being made of the manufacturing method described in the above and having the pattern of the nano-size on the silicon

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wafer substrate surface is include might.

발명의 효과

Effects of the Invention

본 발명에 따르면, 진공공정 등의 복잡한 공정의 필요없이 간소화된 공정만으로 실리콘 웨이퍼 기판 표면에 우수한 반사방지 특성을 갖는 나노 텍스쳐링 구조를 형성시킬 수 있다.

According to the invention, the nano texturing structure of having the anti-reflection property of being excellent on the silicon wafer substrate surface can be formed into the process of becoming streamlined without the need of the process of being complicated including the vacuum process etc.

상세설명

Detailed Description

이하, 첨부되는 도면을 참조하여 본 발명의 실시형태들을 상세하게 설명하도록 한다.

Hereinafter, specifically the attached embodiments of the invention is illustrated.

도 2는 본 발명의 일 실시형태에 따른 태양전지용 실리콘 웨이퍼 기판의 표면을 전자현미경으로 관찰한 이미지이다.

Figure 2 is an image observing the surface of the solar battery use silicone wafer substrate to the electron microscope according to one embodiment of the invention.

도 2를 참조하면, 본 발명의 실리콘 웨이퍼 기판의 표면은 나노 패턴으로 이루어지는 나노 텍스쳐링 구조를 갖는다.

Referring to Figure 2, the surface of the silicon wafer substrate of the invention has the nano texturing structure of being made of the nano pattern.

상기 나노 텍스쳐링 구조는 나노크기의 패턴으로 이루어져 있다. 즉, 실리콘 웨이퍼 기판 상부에 나노 크기의 패턴들이 조직화되어 있는 구조이다. 나노 텍스쳐링 구조에 의하면 반사방지막(anti-reflection; AR)을 사용하는 것과 다른 특징을 얻을 수 있다. 즉, 반사방지막을 사용하면 특정 파장 대역에서만 반사방지의 효과를 얻을 수 있는 반면 나노 텍스쳐링 구조에 의하면 넓은 파장영역에서 균일하게 반사방지의 효과를 얻을 수 있다.

The nano texturing structure comprises the pattern of the nano-size. That is, the structure where the patterns of the nano-size become systematic in the silicon wafer substrate upside. According to the nano texturing structure, the other characteristic can be obtained the reflection barrier layer (anti-reflection: AR) is used. That is, if the reflection barrier layer is used the effect of the anti-reflection can be obtained from the certain wavelength band on the other hands the effect of the anti-reflection can be uniformly obtained according to the nano texturing structure from the wide wavelength area.

나노 패턴의 크기는 태양전지의 반사방지막으로서의 기능을 최대한 달성할 수 있는 범위 내에서 선택될 수 있다. 즉, 패턴의 크기가 너무 크면 반사율이 저하될 수 있고, 반대로 패턴의 크기가 너무 작으면 반사가 방지되어 태양전지로 흡수되는 광량이 미미해지기 때문에, 그 크기를 적절하게 선택하여야 한다.

The size of the nano pattern can be selected in the range that to the utmost can achieve the function as the anti-reflection layer for a solar cell. That is, reflectivity can be degraded if the size of the pattern is so big and the light quantity which the reflection is prevented if the size of the pattern is so small on the contrary and is absorbed into the solar cell is sight. Therefore the size has to be appropriately selected.

이하, 본 발명의 태양전지용 실리콘 웨이퍼 기판의 나노 텍스쳐링 구조를 형성하는 방법에 대해 설명하기로 한다. 도 3a 내지 도 3f는 본 발명의 일 실시형태에 따른 나노 텍스쳐링 구조를 갖는 실리콘 웨이퍼 기판을 포함하는 태양전지를 제조하는 과정을 설명하는 공정도이다.

Hereinafter, it decides to explain the method for forming the nano texturing structure of the solar battery use silicone wafer substrate of the invention. Figures 3a through 3f are the process map for illustrating the process of manufacturing the solar cell including the silicon wafer substrate having the nano texturing structure according to one embodiment of the invention.

먼저, 도 3a에 도시되는 바와 같은 실리콘 웨이퍼 기판(110) 표면에 잔류하는 네이티브 옥사이드(native oxide; 120)를 제거한다. 실리콘 웨이퍼 기판(110)의 표면에는 실리콘 웨이퍼 기판(110)의 제조 과정에서 형성되거나, 대기 중의 노출 등에 따라 형성되는 네이티브 옥사이드(120)가 잔류하게 되는데 나노 텍스쳐링 구조를 형성하기 전에 이러한 이물질을 제거해

In advance, the native oxide (native oxide: 120) remaining in the silicon wafer substrate (110) surface as illustrated in Figure 3a is removed. In the surface of the silicon wafer substrate (110), it is formed at the manufacturing process of the silicon wafer substrate (110) or before the native oxide (120) formed according to

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주어야 한다. 실리콘 웨이퍼 기판(110)을 플루오르화 수소(HF) 혼합용액에 담금으로써 일어나는 화학 반응에 의해 상기와 같은 네이티브 옥사이드(120)가 제거될 수 있다.

the exposure among the atmosphere etc. remaining behind but forming the nano texturing structure such foreign substance is removed. The above-mentioned native oxide (120) can be the silicon wafer substrate (110) removed in the hydrogen fluoride (HF) mixture as the dipping with the chemical reaction occurring.

그 후, 도 3b에 도시되는 바와 같이, 네이티브 옥사이드(120)가 제거된 실리콘 웨이퍼 기판(110) 상에 나노 금속 입자(135)가 분산되어 있는 수용액(130)을 도포하고 건조시킨다. 후에 나노 금속 입자(135)가 형성되어 있지 않은 부분의 실리콘 웨이퍼 기판(110)이 에칭됨으로써 나노 텍스쳐링 구조가 형성된다. 상기 수용액(130)에는 나노 금속 입자(135)가 약 1000 ppm 내지 100000ppm 의 농도로 고르게 분산되어 있을 수 있다. 한편, 나노 금속 입자(135)의 입경은 형성하고자 하는 나노 텍스쳐링 구조의 패턴의 형태에 따라 적절하게 선택될 수 있다. 나노 금속 입자(135)의 입경이 너무 크면 나노 텍스쳐링 구조에 포함되는 패턴 간의 거리가 지나치게 멀어지게 되고, 입경이 너무 작으면 패턴이 너무 조밀하게 형성될 수 있으므로, 적절한 범위 내에서 선택될 수 있다. 일례로서 나노 금속 입자(135)의 입경을 20nm 내지 200nm 의 범위 내에서 선택할 수 있다. 한편, 나노 금속 입자의 구성 물질은 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 등으로 할 수 있다. 일례로서, 약 100nm의 입경을 갖는 은(Ag)을 나노 금속 입자(135)로 선택할 수 있다.

Thereafter, as shown in Figure 3b, the aqueous solution (130) in which the nano metal particle (135) is dispersed is coated with on the silicon wafer substrate (110) from which the native oxide (120) is removed and it dries. After, the nano texturing structure is formed since the silicon wafer substrate (110) of the part in which the nano metal particle (135) is not formed is etched. In the aqueous solution (130), the nano metal particle (135) is evenly dispersed into the concentration of about 1000ppm to 100000ppm. In the meantime, according to the form which the particle diameter of the nano metal particle (135) forms of the pattern of the nano texturing structure, it can be appropriately selected. If the particle diameter of the nano metal particle (135) is so large, the distance included in the nano texturing structure between the pattern becomes overly distant and the pattern can be so tightly formed if the grain size is so small. Therefore it can be selected in the proper range. As an example, the particle diameter of the nano metal particle (135) can be chosen in the range of 20nm to 200nm. In the meantime, the configuration element of the nano metal particle can be done by the gold (Au), the silver (Ag), the copper (Cu), the palladium (Pd), the tin (Sn) etc. As an example, the silver (Ag) having the particle diameter of about 100nm can be selected as the nano metal particle (135).

한편, 나노 금속 입자(135)가 혼합되어 있는 수용액(130)을 실리콘 웨이퍼 기판(110) 상에 도포하는 데에는 스프레이법(spraying), 스핀코팅법(spin coating), 디핑법(dipping) 등이 이용될 수 있다. 스프레이법은 수용액(130)을 실리콘 웨이퍼 기판(110) 상에 고르게 분사하는 방식이고, 스핀코팅법은 실리콘 웨이퍼 기판(110) 상에 수용액(130)을 떨어뜨린 후 이를 회전시켜 수용액(130)이 원심력에 의해 실리콘 웨이퍼 기판(110) 상에 코팅될 수 있도록 하는 방식이며, 디핑법은 실리콘 웨이퍼 기판(110)을 수용액(130)에 담가 코팅을 하는 방식이다. 이러한 방식으로 나노 금속 입자(135)가 분산되어 있는 수용액(130)이 실리콘 웨이퍼 기판(110) 상에 도포되면, 열처리 등을 통하여 이를 건조시켜 실리콘 웨이퍼 기판(110) 상에 나노 금속 입자(135)만이 남을 수 있도록 한다.

In the meantime, the spraying, the spin coating method, the dipping method etc. can be used to coat with the aqueous solution (130) in which the nano metal particle (135) is mixed on the silicon wafer substrate (110). It is the mode in which the spraying evenly sprays the aqueous solution (130) on the silicon wafer substrate (110) and it is the mode in which it rotates this after the spin coating method drops down the aqueous solution (130) on the silicon wafer substrate (110) and the aqueous solution (130) is coated with the centrifugal force on the silicon wafer substrate (110) and it is the mode in which the dipping method dips the silicon wafer substrate (110) in the aqueous solution (130) and coated. In this way, if the aqueous solution (130) in which the nano metal particle (135) is dispersed is coated on the silicon wafer substrate (110) this is dried through the thermal process etc. and it remains on the silicon wafer substrate (110) only the nano metal particle (135).

다음으로, 실리콘 웨이퍼 기판(110)을 에칭액에 담궈 에칭(etching)한다. 상기 에칭액으로는 플루오르화 수소(HF)와 과산화수소수(H2O2)가 혼합되어 있는 용액을 사용할 수 있다. 본래는 플루오르화 수소(HF)와 과산화수소수(H2O2)가 혼합

Next, the silicon wafer substrate (110) is dipped in the etchant and it does with the etching (etching). The solution in which the hydrogen fluoride (HF) and hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/SB)) are mixed can

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되어 있는 용액만으로는 실리콘 웨이퍼 기판(110)을 에칭시킬 수 없으나, 기판(110) 상에 분산되어 있는 나노 금속 입자(135)가 촉매로 작용하여 나노 금속 입자(135)들 사이의 공간에 노출되어 있는 실리콘 웨이퍼 기판(110)이 에칭될 수 있는 것이다. 플루오르화 수소(HF)와 과산화수소수(H2O2)의 혼합비는 10:1 정도로 하는 것이 바람직하다. 도 3c는 이러한 방법에 의해 에칭된 실리콘 웨이퍼 기판(110)의 단면 구조를 나타낸다. 나노 금속 입자(135)들 사이의 공간에 노출된 실리콘 웨이퍼 기판(110)이 에칭됨으로써 나노 패턴으로 형성되는 나노 텍스쳐링 구조가 형성되게 되는 것이다.

be used as the etchant. The inherent cannot etch the silicon wafer substrate (110) to the solution in which t he hydrogen fluoride (HF) and hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/SB)) are mixed. But the nano met al particle (135) dispersed on the substrate (110) acts on the catalyst and the exposed silicon wafer substrat e (110) can be etched on space between nano metal p article (135). It is the be desirable that the mixing ratio of the hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/S B)) and hydrogen fluoride (HF) is done by about 10:1. Figure 3c shows the section structure of the silicon wa fer substrate (110) etched with such method. Since th e silicon wafer substrate (110) exposed to space betw een nano metal particle (135) is etched the nano textu ring structure of being formed with the nano pattern is formed.

에칭이 완료되면 순수(pure water)를 이용하여 실리콘 웨이퍼 기판(110)을 세척한 후에 금속 에칭을 수행하여 나노 금속 입자(135)를 제거한다. 도 3d는 에칭에 의해 나노 금속 입자(135)가 제거된 실리콘 웨이퍼 기판(110)의 모습을 나타낸다. 이렇게 함으로써 표면에 나노 텍스쳐링 구조가 형성된 실리콘 웨이퍼 기판(110)이 얻어질 수 있다.

When the etching is completed, after the silicon wafer substrate (110) is washed using the pure water the me tal etching is performed and the nano metal particle (1 35) is removed. Figure 3d shows the display of the silic on wafer substrate (110) in which the nano metal parti cle (135) is removed using the etching. By doing this, t he silicon wafer substrate (110) in which the nano text uring structure is formed in the surface can be obtaine d.

그 후, 도 3e에 도시되는 바와 같이, 상기 나노 텍스쳐링 구조가 형성된 제1전도성(예를 들면, p형)을 갖는 실리콘 웨이퍼 기판(110)에 제2전도성(예를 들면, n형)을 갖는 물질을 확산시켜 p-n 접합을 형성하고, 표면에 패시베이션 층(passivation; 150)을 형성한다. 패시베이션 층(150)은 실리콘 웨이퍼 기판(110)을 부동태화시켜 표면 결함을 최소화하기 위한 것이다. 패시베이션 층(150)은 실리콘 웨이퍼 기판(110)의 표면을 산화시킴으로써 형성될 수 있다. 즉, 상기 산화 반응에 의해 안정한 물질인 실리콘 산화물(SiOx)이 실리콘 웨이퍼 기판(110) 표면에 형성됨으로써 패시베이션 층(150)이 형성될 수 있다. 한편, 실리콘 질화물(SiNx) 등의 물질을 상기 실리콘 웨이퍼 기판(110) 표면에 증착함으로써 패시베이션 층(150)을 형성시킬 수도 있다.

Thereafter, as shown in Figure 3e, material having the second conductivity (for example, the n-type) are diffu sed over the silicon wafer substrate (110) having the fi rst conductivity (for example, the p-type) in which the nano texturing structure is formed and the p-n junction is formed and the passivation layer (passivation: 150) i s formed on the surface. The passivation layer (150) m akes something passive the silicon wafer substrate (11 0) and the surface defect is to be minimized. The passi vation layer (150) can be formed by oxidizing the surfa ce of the silicon wafer substrate (110). That is, since t he silicon oxide (SiO(SB)x(/SB)) which is material which are stable with the oxidation reaction is formed in the s ilicon wafer substrate (110) surface the passivation lay er (150) can be formed. In the meantime, the passivati on layer (150) can be formed by depositing the materia l including the silicon nitride (SiN(SB)x(/SB)) etc. on th e silicon wafer substrate (110) surface.

다음으로, 도 3f에 도시되는 바와 같이, 상기 패시베이션 층(150)이 형성된 실리콘 웨이퍼 기판(110) 상에 전극(170)을 형성시킴으로써 태양전지가 완성된다. 전극(170)은 통상의 인쇄법(printing) 등에 의해 형성될 수 있다.

Next, as shown in Figure 3f, by forming the electrode (170) on the silicon wafer substrate (110) in which the passivation layer (150) is formed the solar cell is compl eted. The electrode (170) is formed by the normal print ing method etc.

이러한 방법에 의하면, 진공공정 또는 전기분해공정 등을 사용하지 않고도 실리콘 웨이퍼 기판에 나노 텍스쳐링 구조를 형성할 수 있으며, 이에 따라 나노 텍스쳐링 구조 형성에 필요한 작업 공수를 간소화할 수 있고, 제조 원가가 절감될 수 있다.

According to such method, the nano texturing structure can be formed on the silicon wafer substrate even though the vacuum process or the electrolysis pr ocess etc. are not used and accordingly the necessary man-hour can be streamlined in the nano texturing text uring and the manufacturing cost can be cut down.

또한, 값비싼 장비 또는 복잡한 공정 없이도 나노 텍스쳐링 구조와 같은 우수한 특성의 반사방지막을 얻을 수 있다.

Moreover, expensive the reflection barrier layer of the excellent characteristic like the nano texturing structur e can be obtained without the complex process.

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면책안내

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SAMSUNG EX. 1002 - 1935/2862

공개특허 10-2009-0077274

(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(11) 공개번호 10-2009-0077274
(43) 공개일자 2009년07월15일

(51) 국제특허분류(Int. Cl.)
H01L 31/052 (2006.01)
(21) 출원번호 10-2008-0003122
(22) 출원일자 2008년01월10일
심사청구일자 없음

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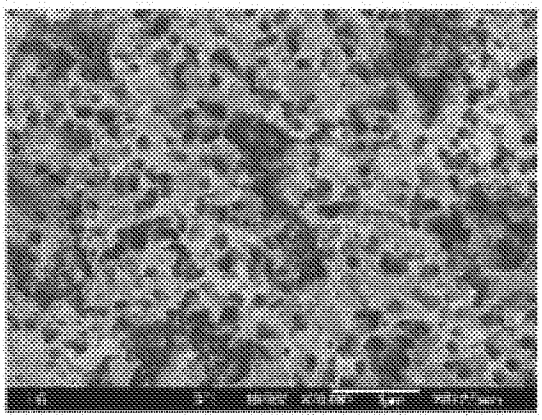
전체 청구항 수 : 총 9 항

(54) 발명의 명칭 **나노 텍스쳐링 구조를 갖는 반도체 웨이퍼 기판을 포함하는벌크형 태양전지의 제조방법**

(57) 요 약

본 발명에 따르면, 벌크형 태양전지에 포함되는 실리콘 웨이퍼 기판 상에 나노 텍스쳐링(texturing) 구조를 형성하는 방법에 있어서, 금속 나노 입자를 촉매로 하는 에칭법을 이용하여 상기 나노 텍스쳐링 구조를 형성함으로써 우수한 특성을 갖는 반사방지막을 손쉽게 얻을 수 있는 벌크형 태양전지의 제조방법이 제공된다. 본 발명에 따르면, 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서, 상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되, 상기 나노 텍스쳐링 구조 형성 단계는 금속을 촉매로 하는 에칭법에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법이 제공된다.

대 표 도 - 도2



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특허청구의 범위

청구항 1

실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서,

상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되,

상기 나노 텍스쳐링 구조 형성 단계는 금속을 촉매로 하는 에칭법에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 2

제1항에 있어서,

상기 나노 텍스쳐링 구조 형성 단계는,

나노 금속 입자가 혼합되어 있는 용액을 상기 실리콘 웨이퍼 기판 상에 분산시키는 단계;

에칭액을 사용하여 상기 나노 금속 입자가 분산된 실리콘 웨이퍼 기판을 에칭하는 단계; 및

상기 나노 금속 입자를 제거하는 단계를 포함하는 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 3

제2항에 있어서,

상기 나노 금속 입자의 입경은 20㎚ 내지 200㎚인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 4

제2항에 있어서,

상기 나노 금속 입자는 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 중 적어도 하나인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 5

제2항에 있어서,

상기 에칭액은 플루오르화 수소(HF)와 과산화수소수(H_2O_2)의 혼합용액인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 6

제5항에 있어서,

상기 플루오르화 수소(HF)와 과산화수소수(H_2O_2)의 혼합비는 10:1인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 7

제2항에 있어서,

상기 용액에서 상기 나노 금속 입자의 농도는 1000ppm 내지 100000ppm 인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 8

제2항에 있어서,

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상기 나노 금속 입자가 혼합되어 있는 용액을 분산시키는 단계는, 스프레이법(spraying), 스핀코팅법(spin coating), 디핑법(dipping) 중 어느 하나에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 9

제1항 내지 제8항 중 어느 하나의 제조방법으로 제조된 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 포함하는 벌크형 태양전지.

발 명 의

발명의 상세한 설명

기 술 분 야

[0001] 본 발명은 벌크형 태양전지의 제조방법에 관한 것이다. 보다 상세하게는 벌크형 태양전지에 포함되는 실리콘 웨이퍼 기판 상에 나노 텍스쳐링(texturing) 구조를 형성하는 방법에 있어서, 금속 나노 입자를 촉매로 하는 에칭법을 이용하여 상기 나노 텍스쳐링 구조를 형성함으로써 우수한 특성을 갖는 반사방지막을 손쉽게 얻을 수 있는 벌크형 태양전지의 제조방법에 관한 것이다.

배 경 기 술

[0002] 태양전지는 포토다이오드의 일종으로 태양광을 직접 전력으로 전환시키는 목적에 이용되고 있어, 대체 에너지원으로서 지상에서는 물론이고 우주개발을 위해서도 그 이용이 점차 확대되어가고 있어 전력용 전자소자로서 매우 중요하다. 그 구조도 p-n 접합형, 쇼트키 배리어형 및 이종(異種)반도체의 접합으로 이루어지는 것 등이 있으며, 소재로서는 실리콘 갈륨비소 등의 결정체, 기타 각종 반도체가 광범위하게 이용되고 있다. 특히 근래에 와서는 다결정(多結晶) 실리콘이나 비정질(非晶質) 실리콘을 이용한 태양전지의 개발과 실용화가 크게 각광을 받고 있다.

[0003] 그러나 높은 광전변환효율과 품질특성 때문에 단결정의 실리콘 웨이퍼를 기반으로하는 벌크형 태양전지가 상용화되고 있는 실정이다.

[0004] 일반적으로 실리콘 결정계(crystalline) 태양전지는 실리콘 웨이퍼를 출발 원료로 한다. 실리콘 웨이퍼는 고순도로 정제된 실리콘을 고온으로 가열하여 결정으로 성장된 잉곳을 만들고 이를 절단 및 연마를 통해 대형의 결정판 형태의 웨이퍼 기판을 만든다. 결정은 원자가 규칙적으로 배열된 물질을 의미한다.

[0005] 종래의 태양전지를 제조하기 위한 웨이퍼의 처리 방법 중 가장 중요한 처리는 기판 표면의 텍스쳐링(texturing), 즉 조직화이다. 이러한 텍스쳐링의 목적은 빛을 받는 태양전지의 전면부에서의 반사율을 감소시키고, 태양전지 내에서 빛의 통과 길이를 길게 함으로써 태양전지 내부로 빛이 흡수되도록 하여 효율을 향상시키고자 하는 것이다. 한편, 기판 상에 광학 박막을 형성시켜 반사방지막으로서의 기능을 하게 할 수도 있다.

[0006] 텍스쳐링된 종래의 태양전지용 웨이퍼 기판의 표면을 확대한 단면도는 도 1a에 도시하였다. 텍스쳐링한 후의 표면은 피라미드 구조를 가지므로 옆면에서 관찰할 때 정삼각형의 형상을 가진다.

[0007] 종래 기술에 의하면, 경면 연마처리(Polishing)된 웨이퍼 표면은 입사되는 태양 빛의 30% 내지 50% 정도를 반사시키고, 표면을 피라미드 형태로 조직화(texturing)시키면 입사되는 태양광의 10% 내지 20% 정도를 반사하게 되어 반사율이 현저하게 줄어든다. 또한, 조직화시킨 표면에 반사방지막(anti-reflection, AR)을 증착시키면 반사율을 약 5% 내지 10%까지 감소시킬 수 있는 것으로 알려져 있다.

[0008] 그러나, 상기 반사율은 태양광의 주요 흡수 파장대역인 500㎚ 내지 1000㎚ 에서관찰된 평균값으로서, 태양광 파장범위의 낮은 파장영역인 300㎚ 내지 400㎚에서는 비교적 높은 반사도를 가지며, 반사방지막의 증착 이후라야만 비로소 상대적으로 더 낮은 반사도를 갖게 되는 문제점을 가지고 있다. 따라서, 모든 태양광의 파장영역에서 균일하게 낮은 반사율을 갖는 기판 표면을 형성하고자 하는 연구가 진행되었고, 그 결과 나노 구조를 갖는 나노 텍스쳐링 구조가 형성된 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지가 개발되었다.

[0009] 이러한 나노 텍스쳐링 구조를 갖는 종래 태양전지용 실리콘 웨이퍼 기판의 표면을 확대한 이미지는 도 1과 같다. 도 1을 참조하면 조직화된 웨이퍼 기판 상에는 피라미드 형태의 나노 구조가 형성되어 있음을 알 수

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있다.

[0010] 이러한 나노 텍스쳐링 구조로 형성되는 반사방지막은 넓은 파장영역 및 넓은 입사각 범위에서 반사 방지막으로서의 기능을 수행한다. 종래에는 이러한 나노 텍스쳐링 구조를 형성하기 위해 진공 중에서 염소(Cl) 기체 또는 플루오르화 황(SF_6)을 이용하여 반응성 이온 에칭(RIE: Reactive Ion Etching)을 수행하거나, 실리콘 웨이퍼 기판 표면에 금속을 매우 얇게 증착 한 후 습식에칭을 수행하였다.

[0011] 그러나, 상기 방법 중 반응성 이온 에칭법을 이용하는 방법은 복잡하고 값비싼 장비를 필요로 하는 진공 공정이 필수적이라는 문제가 있다. 한편, 습식 에칭을 이용하는 방법은 금속과 에칭액과의 촉매반응으로 실리콘을 에칭하여 나노 텍스쳐링 구조를 형성하는 방식으로 반응성 이온 에칭(RIE)을 이용하는 방식보다 공정상 간단하다는 장점이 있다. 그러나, 이 방법 또는 진공 장비를 사용하여야 하는 문제가 있다.

[0012] 따라서, 진공 장비 등을 사용하지 않기 위하여 실리콘에 전기 도금 방식을 이용하여 금속을 얇게 도금한 후 이를 에칭하여 위와 같은 방법으로 나노 텍스쳐링 구조를 형성시키기도 한다.

[0013] 한편, 실리콘 웨이퍼 기판 표면에 나노 텍스쳐링 구조를 형성시키는 또 다른 방법으로는 할 가스 분위기에서 실리콘 웨이퍼 기판 표면에 엑시머 레이저를 조사함으로써 나노 텍스쳐링 구조를 형성하는 방법이 있다.

[0014] 또한, 나노 텍스쳐링 구조가 아닌 복수 개의 홈로 이루어지는 다공성 구조을 실리콘 웨이퍼 기판에 형성시킴으로써 반사방지막을 형성하기도 한다. 그러나, 이 방법은 기판 표면에 다공성 구조를 형성시키기 위해 전기분해 장치 등 복잡한 장치를 이용한 공정을 필요로 한다는 문제가 있다.

[0015] 따라서, 간단한 공정만으로도 우수한 특성을 가지는 텍스쳐링 구조를 형성시킬 수 있는 기술에 대한 개발이 필요하다.

발명의 내용

해결 하고자하는 과제

[0016] 본 발명은 상술한 바와 같은 종래 기술의 문제점을 해결하기 위한 것으로, 진공공정 등의 필요없이 간소화된 공정만으로 실리콘 웨이퍼 기판 표면에 우수한 반사방지 특성을 갖는 나노 텍스쳐링 구조를 형성시킬 수 있는 벌크형 태양전지의 제조방법을 제공하는 데에 그 목적이 있다.

과제 해결수단

[0017] 상술한 목적을 달성하기 위한 본 발명의 일 실시형태에 따르면, 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서, 상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되, 상기 나노 텍스쳐링 구조 형성 단계는 금속을 촉매로 하는 에칭법에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법이 제공된다.

[0018] 상기 나노 텍스쳐링 구조 형성 단계는, 나노 금속 입자가 혼합되어 있는 용액을 상기 실리콘 웨이퍼 기판 상에 분산시키는 단계, 에칭액을 사용하여 상기 나노 금속 입자가 분산된 실리콘 웨이퍼 기판을 에칭하는 단계, 및 상기 나노 금속 입자를 제거하는 단계를 포함할 수 있다.

[0019] 상기 나노 금속 입자의 입경은 20nm 내지 200nm로 하는 것이 바람직하다.

[0020] 상기 나노 금속 입자는 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 중 적어도 하나로 하는 것이 바람직하다.

[0021] 상기 에칭액은 플루오르화 수소(HF)와 과산화수소수(H_2O_2)의 혼합용액인 것이 바람직하다.

[0022] 상기 플루오르화 수소(HF)와 과산화수소수(H_2O_2)의 혼합비는 10:1로 하는 것이 바람직하다.

[0023] 상기 용액에서 상기 나노 금속 입자의 농도는 1000ppm 내지 100000ppm 으로 하는 것이 바람직하다.

[0024] 상기 나노 금속 입자가 혼합되어 있는 용액을 분산시키는 단계는, 스프레이법(spraying), 스핀코팅법(spin

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coating), 디핑법(dipping) 중 어느 하나에 의해 수행될 수 있다.

[0025] 상기 목적을 달성하기 위한 본 발명의 벌크형 태양전지는 상기의 제조방법으로 제조되고 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 포함할 수 있다.

효 과

[0026] 본 발명에 따르면, 진공공정 등의 복잡한 공정의 필요없이 간소화된 공정만으로 실리콘 웨이퍼 기판 표면에 우수한 반사방지 특성을 갖는 나노 텍스쳐링 구조를 형성시킬 수 있다.

발명의 실시를 위한 구체적인 내용

[0027] 이하, 첨부되는 도면을 참조하여 본 발명의 실시형태들을 상세하게 설명하도록 한다.

[0028] 도 2는 본 발명의 일 실시형태에 따른 태양전지용 실리콘 웨이퍼 기판의 표면을 전자현미경으로 관찰한 이미지이다.

[0029] 도 3을 참조하면, 본 발명의 실리콘 웨이퍼 기판의 표면은 나노 패턴으로 이루어지는 나노 텍스쳐링 구조를 갖는다.

[0030] 상기 나노 텍스쳐링 구조는 나노크기의 패턴으로 이루어져 있다. 즉, 실리콘 웨이퍼 기판 상부에 나노 크기의 패턴들이 조직화되어 있는 구조이다. 나노 텍스쳐링 구조에 의하면 반사방지막(anti-reflection: AR)을 사용하는 것과 다른 특징을 얻을 수 있다. 즉, 반사방지막을 사용하면 특정 파장 대역에서만 반사방지의 효과를 얻을 수 있는 반면 나노 텍스쳐링 구조에 의하면 넓은 파장영역에서 균일하게 반사방지의 효과를 얻을 수 있다.

[0031] 나노 패턴의 크기는 태양전지의 반사방지막으로서의 기능을 최대한 달성할 수 있는 범위 내에서 선택될 수 있다. 즉, 패턴의 크기가 너무 크면 반사율이 저하될 수 있고, 반대로 패턴의 크기가 너무 작으면 반사가 방지되어 태양전지로 흡수되는 광량이 미미해지기 때문에, 그 크기를 적절하게 선택하여야 한다.

[0032] 이하, 본 발명의 태양전지용 실리콘 웨이퍼 기판의 나노 텍스쳐링 구조를 형성하는 방법에 대해 설명하기로 한다. 도 3a 내지 도 3f는 본 발명의 일 실시형태에 따른 나노 텍스쳐링 구조를 갖는 실리콘 웨이퍼 기판을 포함하는 태양전지를 제조하는 과정을 설명하는 공정도이다.

[0033] 먼저, 도 3a에 도시되는 바와 같은 실리콘 웨이퍼 기판(110) 표면에 잔류하는 네이티브 옥사이드(native oxide: 130)를 제거한다. 실리콘 웨이퍼 기판(110)의 표면에는 실리콘 웨이퍼 기판(110)의 제조 과정에서 형성되거나, 대기 중의 노출 등에 따라 형성되는 네이티브 옥사이드(120)가 잔류하게 되는데 나노 텍스쳐링 구조를 형성하기 전에 이러한 이물질을 제거해주어야 한다. 실리콘 웨이퍼 기판(110)을 플루오르화 수소(HF) 혼합용액에 담금으로써 일어나는 화학 반응에 의해 상기와 같은 네이티브 옥사이드(120)가 제거될 수 있다.

[0034] 그 후, 도 3b에 도시되는 바와 같이, 네이티브 옥사이드(120)가 제거된 실리콘 웨이퍼 기판(110) 상에 나노 금속 입자(135)가 분산되어 있는 수용액(130)을 도포하고 건조시킨다. 후에 나노 금속 입자(135)가 형성되어 있지 않은 부분의 실리콘 웨이퍼 기판(110)이 에칭됨으로써 나노 텍스쳐링 구조가 형성된다. 상기 수용액(130)에는 나노 금속 입자(135)가 약 1000ppm 내지 100000ppm 의 농도로 고르게 분산되어 있을 수 있다. 한편, 나노 금속 입자(135)의 입경은 형성하고자 하는 나노 텍스쳐링 구조의 패턴의 형태에 따라 적절하게 선택될 수 있다. 나노 금속 입자(135)의 입경이 너무 크면 나노 텍스쳐링 구조에 포함되는 패턴 간의 거리가 지나치게 멀어지게 되고, 입경이 너무 작으면 패턴이 너무 조밀하게 형성될 수 있으므로, 적절한 범위 내에서 선택될 수 있다. 일례로서 나노 금속 입자(135)의 입경을 20nm 내지 200nm 의 범위 내에서 선택할 수 있다. 한편, 나노 금속 입자의 구성 물질은 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 등으로 할 수 있다. 일례로서, 약 100nm의 입경을 갖는 은(Ag)을 나노 금속 입자(135)로 선택할 수 있다.

[0035] 한편, 나노 금속 입자(135)가 혼합되어 있는 수용액(130)을 실리콘 웨이퍼 기판(110) 상에 도포하는 데에는 스프레이법(spraying), 스핀코팅법(spin coating), 디핑법(dipping) 등이 이용될 수 있다. 스프레이법은 수용액(130)을 실리콘 웨이퍼 기판(110) 상에 고르게 분사하는 방식이고, 스핀코팅법은 실리콘 웨이퍼 기판(110) 상에 수용액(130)을 떨어뜨린 후 이를 회전시켜 수용액(130)이 원심력에 의해 실리콘 웨이퍼 기판(110) 상에 코팅될 수 있도록 하는 방식이며, 디핑법은 실리콘 웨이퍼 기판(110)을 수용액(130)에 담가 코팅을 하는 방식이다. 이

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러한 방식으로 나노 금속 입자(135)가 분산되어 있는 수용액(130)이 실리콘 웨이퍼 기판(110) 상에 도포되면, 열처리 등을 통하여 이를 건조시켜 실리콘 웨이퍼 기판(110) 상에 나노 금속 입자(135)만이 남을 수 있도록 한다.

[0036] 다음으로, 실리콘 웨이퍼 기판(110)을 에칭액에 담궈 에칭(etching)한다. 상기 에칭액으로는 플루오르화 수소(HF)와 과산화수소수(H_2O_2)가 혼합되어 있는 용액을 사용할 수 있다. 본래는 플루오르화 수소(HF)와 과산화수소수(H_2O_2)가 혼합되어 있는 용액만으로는 실리콘 웨이퍼 기판(110)을 에칭시킬 수 없으나, 기판(110) 상에 분산되어 있는 나노 금속 입자(135)가 촉매로 작용하여 나노 금속 입자(135)들 사이의 공간에 노출되어 있는 실리콘 웨이퍼 기판(110)이 에칭될 수 있는 것이다. 플루오르화 수소(HF)와 과산화수소수(H_2O_2)의 혼합비는 10:1 정도로 하는 것이 바람직하다. 도 3c는 이러한 방법에 의해 에칭된 실리콘 웨이퍼 기판(110)의 단면 구조를 나타낸다. 나노 금속 입자(135)들 사이의 공간에 노출된 실리콘 웨이퍼 기판(110)이 에칭됨으로써 나노 패턴으로 형성되는 나노 텍스쳐링 구조가 형성되게 되는 것이다.

[0037] 에칭이 완료되면 순수(pure water)를 이용하여 실리콘 웨이퍼 기판(110)을 세척한 후에 금속 에칭을 수행하여 나노 금속 입자(135)를 제거한다. 도 3d는 에칭에 의해 나노 금속 입자(135)가 제거된 실리콘 웨이퍼 기판(110)의 모습을 나타낸다. 이렇게 함으로써 표면에 나노 텍스쳐링 구조가 형성된 실리콘 웨이퍼 기판(110)이 얻어질 수 있다.

[0038] 그 후, 도 3e에 도시되는 바와 같이, 상기 나노 텍스쳐링 구조가 형성된 제1전도성(예를 들면, p형)을 갖는 실리콘 웨이퍼 기판(110)에 제2전도성(예를 들면, n형)을 갖는 물질을 확산시켜 p-n 접합을 형성하고, 표면에 패시베이션 층(passivation; 150)을 형성한다. 패시베이션 층(150)은 실리콘 웨이퍼 기판(110)을 부동태화시켜 표면 결함을 최소화하기 위한 것이다. 패시베이션 층(150)은 실리콘 웨이퍼 기판(110)의 표면을 산화시킴으로써 형성될 수 있다. 즉, 상기 산화 반응에 의해 안정한 물질인 실리콘 산화물(SiO_2)이 실리콘 웨이퍼 기판(110) 표면에 형성됨으로써 패시베이션 층(150)이 형성될 수 있다. 한편, 실리콘 질화물(SiN_x) 등의 물질을 상기 실리콘 웨이퍼 기판(110) 표면에 증착함으로써 패시베이션 층(150)을 형성시킬 수도 있다.

[0039] 다음으로, 도 3f에 도시되는 바와 같이, 상기 패시베이션 층(150)이 형성된 실리콘 웨이퍼 기판(110) 상에 전극(170)을 형성시킴으로써 태양전지가 완성된다. 전극(170)은 통상의 인쇄법(printing) 등에 의해 형성될 수 있다.

[0040] 이러한 방법에 의하면, 진공공정 또는 전기분해공정 등을 사용하지 않고도 실리콘 웨이퍼 기판에 나노 텍스쳐링 구조를 형성할 수 있으며, 이에 따라 나노 텍스쳐링 구조 형성에 필요한 작업 공수를 간소화할 수 있고, 제조 원가가 절감될 수 있다.

[0041] 또한, 값비싼 장비 또는 복잡한 공정 없이도 나노 텍스쳐링 구조와 같은 우수한 특성의 반사방지막을 얻을 수 있다.

도면의 간단한 설명

[0042] 도 1은 종래 태양전지용 실리콘 웨이퍼 기판 표면에 형성된 나노 텍스쳐링 구조를 전자현미경으로 관찰한 이미지이다.

[0043] 도 2는 본 발명의 일 실시형태에 따른 태양전지용 실리콘 웨이퍼 기판의 표면을 전자현미경으로 관찰한 이미지이다.

[0044] 도 3a 내지 도 3f는 본 발명의 일 실시형태에 따른 태양전지용 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조과정을 설명하는 공정도이다.

[0045] <도면의 주요부분에 대한 부호의 설명>

[0046] 110: 기판 120: 네이티브 옥사이드

[0047] 130: 나노 금속 입자가 혼합된 수용액 135: 금속 나노 입자

[0048] 150: 패시베이션 층 170: 전극

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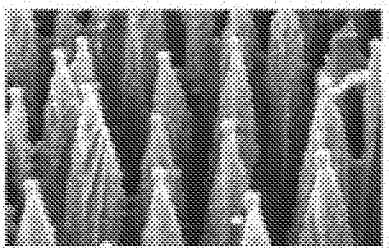
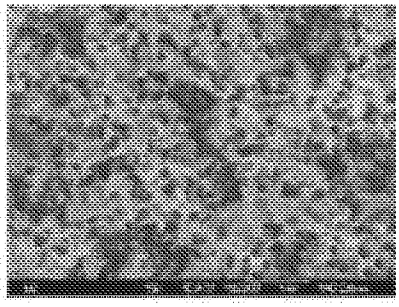
도면

도면1



도면2



도면3a

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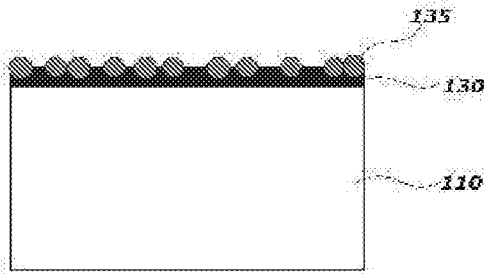
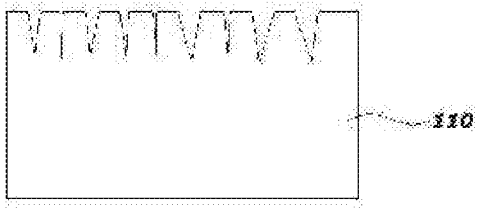
도면3b

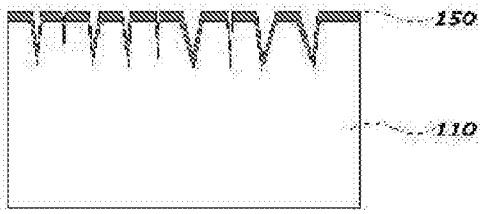


도면3c

도면3d



도면3e



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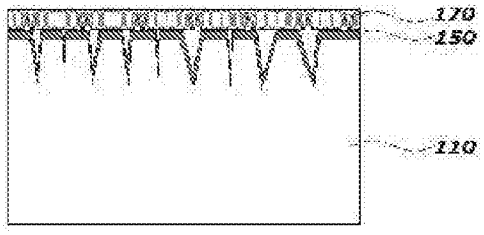
도면3f



SAMSUNG EX. 1002 - 1945/2862

(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

(19) Weltorganisation für geistiges Eigentum
Internationales Büro

(43) Internationales Veröffentlichungsdatum
10. Dezember 2009 (10.12.2009)

PCT

(10) Internationale Veröffentlichungsnummer
WO 2009/147085 A1

(51) Internationale Patentklassifikation:
G01J 1/42 (2006.01) *G01J 5/20* (2006.01)
H01L 27/146 (2006.01)

(21) Internationales Aktenzeichen: PCT/EP2009/056603

(22) Internationales Anmeldedatum:
29. Mai 2009 (29.05.2009)

(25) Einreichungssprache: Deutsch

(26) Veröffentlichungssprache: Deutsch

(30) Angaben zur Priorität:
10 2008 002 270.5 6. Juni 2008 (06.06.2008) DE

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[Fortsetzung auf der nächsten Seite]

(54) **Title**: MULTISPECTRAL SENSOR

(54) **Bezeichnung**: MULTISPEKTRALER SENSOR

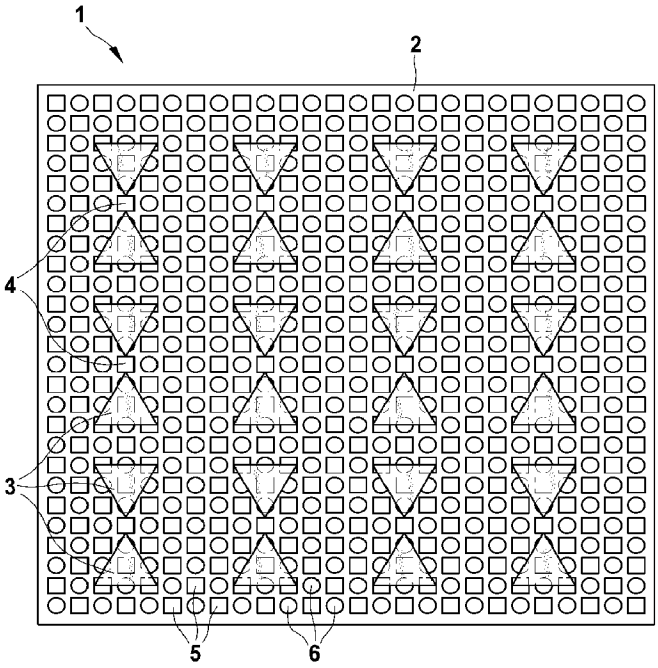

Fig. 1

(57) **Abstract**: The present invention relates to a multispectral sensor (1) comprising a complementary metal oxide semiconductor substrate (2) with a switching circuit, at least one antenna (3) - receiving means (4) combination device for detecting teraherz radiation, at least one other bolometer (5) for detecting mid-ranged infrared radiation and at least one diode (6) for detecting radiation in the visible to near infrared range, a multispectral imaging and/or spectroscopy system, method for detecting and/or examining life forms, objects and materials using such a system, as well as the use of such a sensor (1) and system.

(57) **Zusammenfassung**: Die vorliegende Erfindung betrifft einen multispektralen Sensor (1), der ein komplementäres Metall-Oxid-Halbleiter-Substrat (2) mit Schaltkreis, mindestens eine Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtung zur Detektion von Terahertzstrahlung, mindestens ein weiteres Bolometer (5) zur Detektion von mittlerer Infrarotstrahlung, und mindestens eine Diode (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs umfasst, ein multispektrales Bildgebungs- und/oder Spektroskopie-System, Verfahren zur Detektion und/oder Untersuchung von Lebewesen, Gegenständen und Materialien mit einem derartigen System sowie die Verwendung eines derartigen Sensors (1) und Systems.

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(84) **Bestimmungsstaaten** *(soweit nicht anders angegeben, für jede verfügbare regionale Schutzrechtsart)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), eurasisches (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), europäisches (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Veröffentlicht:

— *mit internationalem Recherchenbericht (Artikel 21 Absatz 3)*

— *vor Ablauf der für Änderungen der Ansprüche geltenden Frist; Veröffentlichung wird wiederholt, falls Änderungen eingehen (Regel 48 Absatz 2 Buchstabe h)*

SAMSUNG EX. 1002 - 1947/2862

Titel

Multispektraler Sensor

Beschreibung

Die vorliegende Erfindung betrifft einen multispektralen Sensor zur Detektion von Terahertzstrahlung, Infrarotstrahlung und Strahlung des sichtbaren bis nahen Infrarot-Bereichs, ein multispektrales Bildgebungs- und/oder Spektroskopie-System, ein Verfahren zur Detektion und/oder Untersuchung von Lebewesen, Gegenständen und Materialien mit einem derartigen System sowie die Verwendung eines derartigen Sensors und Systems.

Stand der Technik

Das elektromagnetische Spektrum kann im Bereich des Terahertz-Frequenzbandes Informationen über die komplexe chemische Zusammensetzung von Stoffen, sowie über die dielektrischen Eigenschaften von Gegenständen geben. Für diese Anwendung werden derzeit recht komplexe Systeme verwendet, die beispielsweise gepulste Laserquellen enthalten. Ein wesentlicher Schwachpunkt der angebotenen Terahertz-Systeme besteht neben der Komplexität darin, dass eine Messung allein im Terahertz-Frequenzband wenig aussagekräftig ist und häufig durch parallele Messungen im sichtbaren oder infraroten Frequenzband ergänzt werden muss. Dies erfolgt herkömmlicherweise durch die parallele Verwendung mehrerer Detektoren oder Detektierungssysteme, die eine komplexe gegenseitige optische Ausrichtung erfordern, was hohe Kosten des Gesamtsystems zur Folge hat.

Offenbarung der Erfindung

Vorteile der Erfindung

SAMSUNG EX. 1002 - 1948/2862

Der erfindungsgemäße multispektrale Sensor umfassend

- ein komplementäres Metall-Oxid-Halbleiter-Substrat mit Schaltkreis, und
- mindestens eine Antenne-Empfängermittel-Kombinationsvorrichtung zur Detektion von Terahertzstrahlung, und
- mindestens eine Vorrichtung zur Detektion von mittlerer Infrarotstrahlung, und
- mindestens eine Diode zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs

hat zum einen den Vorteil, dass alle Bauelemente des Sensors bei Raumtemperatur betrieben werden können. Daher bedarf ein erfindungsgemäßer Sensor **1** keiner Kühlung, insbesondere keiner kryoskopischen Kühlung. Zum anderen hat der erfindungsgemäße Sensor **1** den Vorteil, dass darauf verschiedenen Funktionen auf einem einzigen Bauteil vereint werden, wodurch vorteilhafterweise ein einziger Sensor zur Bewältigung komplexer Detektierungsanwendungen genügt. Darüber hinaus entfällt vorteilhafterweise das aufwendige Einstellen verschiedener Sensoren und es wird nur eine einzige breitbandige, vorzugsweise reflektive, Optik benötigt. Der erfindungsgemäße Sensor ermöglicht weiterhin vorteilhafterweise eine parallele, im Idealfall Echtzeit-Detektion von elektromagnetischer Strahlung im sichtbaren-nah-infraroten, mittel-infraroten und Terahertz-Bereich. Ferner können die erfindungsgemäßen Sensoren langfristig betrachtet zu niedrigen Produktionsstückkosten hergestellt werden, was auch eine Anwendung in Massenprodukten ermöglicht.

Zeichnungen

Weitere Vorteile und vorteilhafte Ausgestaltungen des erfindungsgemäßen Gegenstandes werden durch die Zeichnungen veranschaulicht und in der nachfolgenden Beschreibung erläutert. Dabei ist zu beachten, dass die Figuren nur beschreibenden Charakter haben und nicht dazu gedacht sind, die Erfindung in irgendeiner Form einzuschränken.

Fig. 1 zeigt eine Draufsicht auf eine Ausführungsform eines erfindungsgemäßen multispektralen Sensors.

SAMSUNG EX. 1002 - 1949/2862

Figur 1 zeigt, dass der erfindungsgemäße Sensor **1** ein komplementäres Metall-Oxid-Halbleiter-Substrat **2** mit einem nicht dargestellten Schaltkreis umfasst. Derartige Substrate werden üblicherweise auch als CMOS-Substrat („complementary metal oxide semiconductor") bezeichnet. Erfindungsgemäß sind auf dem CMOS-Substrat **2** mindestens eine Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zur Detektion von Terahertzstrahlung, mindestens eine Vorrichtung **5** zur Detektion von mittlerer Infrarotstrahlung und mindestens eine Diode **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs angeordnet.

Im Rahmen der vorliegenden Erfindung wird unter dem Begriff „Terahertzstrahlung" elektromagnetische Strahlung in einem Bereich von etwa ≥ 15 µm bis etwa ≤ 1000 µm, und unter dem Begriff „mittlerer Infrarotstrahlung" elektromagnetische Strahlung in einem Bereich von etwa ≥ 1 µm bis etwa < 15 µm, und unter dem Begriff „Strahlung des sichtbaren bis nahen Infrarot-Bereichs" elektromagnetische Strahlung in einem Bereich von etwa $\geq 0{,}380$ µm bis etwa < 1 µm, verstanden.

Das Detektierungsintervall des erfindungsgemäßen Sensors **1** kann im Terahertz-Bereich sowohl $> 0{,}3$ Terahertz bis ≤ 20 Terahertz als auch beispielsweise $\geq 0{,}3$ Terahertz oder $\geq 0{,}5$ Terahertz oder ≥ 1 Terahertz bis ≤ 3 Terahertz oder ≤ 5 Terahertz oder ≤ 10 Terahertz, sein. Entsprechend kann das Detektierungsintervall des erfindungsgemäßen Sensors **1** im Terahertz-Bereich sowohl ≥ 15 µm bis < 1000 µm als auch beispielsweise ≥ 30 µm oder ≥ 60 µm oder ≥ 100 µm bis ≤ 300 µm oder ≤ 600 µm oder < 1000 µm, sein.

Ebenso kann das Detektierungsintervall des erfindungsgemäßen Sensors **1** im mittleren Infrarot-Bereich sowohl > 20 Terahertz bis ≤ 300 Terahertz als auch $\geq 21{,}4$ Terahertz bis $\leq 37{,}5$ Terahertz oder ≥ 60 Terahertz oder ≤ 100 Terahertz, sein. Entsprechend kann das Detektierungsintervall des erfindungsgemäßen Sensors **1** im mittleren Infrarot-Bereich sowohl ≥ 1 µm bis etwa < 15 µm als auch beispielsweise ≥ 3 µm bis ≤ 5 µm oder ≥ 8 µm bis ≤ 14 µm, sein.

Analog kann das Detektierungsintervall des erfindungsgemäßen Sensors **1** im sichtbaren bis nah-infraroten Bereich > 300 Terahertz bis ≤ 790 Terahertz sein.

Im Rahmen der vorliegenden Erfindung muss eine Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zur Detektion von Terahertzstrahlung beziehungsweise eine Vorrichtung **5** zur Detektion von mittlerer Infrarotstrahlung beziehungsweise eine Diode **6** zur

Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs folglich nicht den kompletten jeweiligen Strahlungsbereich detektieren.

Im Rahmen einer bevorzugten Ausführungsform der vorliegenden Erfindung weist der erfindungsgemäße Sensor **1** mindestens zwei unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern auf.

Eine Unterteilung des Terahertz-Bereichs in mindestens zwei, insbesondere schmalbandige, Unterbänder, hat den Vorteil, dass sich schmalbandige Antennen **3** besser an das Empfangsmittel **4** anpassen, insbesondere koppeln, lassen, wodurch bei geeigneter Anordnung die Empfindlichkeit („Performance“) des Gesamtsystems verbessert werden kann.

Der erfindungsgemäße Sensor **1** weist daher vorzugsweise mindestens zwei unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen auf, die derart ausgebildet sind, dass der Terahertz-Bereich in mindestens zwei, insbesondere schmalbandige, Unterbänder aufgeteilt wird, welche den Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zugeordnet sind.

Darüber hinaus kann der erfindungsgemäße Sensor **1** mindestens zwei unterschiedliche Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern aufweisen.

Ferner kann der erfindungsgemäße Sensor **1** auch mindestens zwei unterschiedliche Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern aufweisen.

Wie Figur 1 zeigt, weist ein erfindungsgemäßer Sensor **1** vorzugsweise eine Vielzahl, beispielsweise gleicher und/oder unterschiedlicher (nicht dargestellt), Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs auf.

Als Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtung haben sich im Rahmen der vorliegenden Erfindung Antenne-Bolometer-Kombinationsvorrichtungen und/oder Antenne-

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Diode-Kombinationsvorrichtungen, insbesondere Antenne-Bolometer-, Antenne-Schottky-Diode- und/oder Antenne-MIM-Diode-Kombinationsvorrichtungen, als besonders vorteilhaft erwiesen, da derartige Kombinationsvorrichtungen keine Kühlung, insbesondere keine kryoskopische Kühlung benötigen. Dabei wird im Sinn der vorliegenden Erfindung unter einer MIM-Diode eine Metall-Isolator-Metall-Diode („metal insulator metal diode") verstanden. Die Variation dieser unterschiedlichen **3**-Empfängermittel-**4**-Kombinationsvorrichtungen bietet eine Möglichkeit unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

Im Rahmen der vorliegenden Erfindung weist eine Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtung mindestens eine an das Empfängermittel **4**, insbesondere kapazitiv, gekoppelte Antennen **3** auf. Die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtung kann jedoch auch mindestens zwei Antennen **3** aufweisen, welche an das Empfängermittel **4**, insbesondere kapazitiv, gekoppelt sind. Die Zahl der Antennen bietet eine weitere Möglichkeit unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

Beim Einsatz eines Bolometers als Empfängermittel **4** dient die Antenne **3** dazu Terahertzstrahlung zu absorbieren, welche in dem mit der Antenne **3**, insbesondere kapazitiv, gekoppelten Bolometer in Wärme umgewandelt wird, wobei eine resultierende Widerstandsänderung des Bolometers gemessen wird. Bei dem Bolometer kann es sich dabei um ein Mikrobolometer handeln. Das Bolometer **4** kann im Rahmen der vorliegenden Erfindung ein in etwa $\geq 25\ \mu m^2$ bis $\leq 4900\ \mu m^2$, insbesondere $\geq 625\ \mu m^2$ bis $\leq 2500\ \mu m^2$, großes schichtförmiges Substrat aufweisen, welches mittels zwei elektrisch leitenden Stützen beabstandet zu dem CMOS-Substrat **2** angeordnet ist. Dabei kann das schichtförmige Substrat sowohl polygon, insbesondere rechteckig und/oder viereckig, als auch im Wesentlichen unrund, insbesondere ellipsoid oder kreisförmig, ausgestaltet sein. Das schichtförmige Substrat kann dabei amorphes Silizium oder Vanadiumoxid umfassen. Das schichtförmige Substrat kann beispielsweise parallel zu dem CMOS-Substrat **2** angeordnet sein. Die Bolometerausgestaltung bietet eine weitere Möglichkeit unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

Beim Einsatz einer Diode **4**, insbesondere einer Schottky- oder MIM-Diode, als Empfängermittel **4** wird das von der Antenne **3** empfangene Terahertzsignal gleichgerichtet beziehungsweise bei einer heterodynen Empfangslösung mit einem weiteren Terahertzsignal in ein Zwischenfrequenzsignal gemischt. Die Diodenausgestaltung bietet eine weitere Möglichkeit unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

Im Rahmen der vorliegenden Erfindung können mehrere, insbesondere alle, Antennen **3**, wie in Figur 1 gezeigt, in einer Ebene angeordnet sein. Ebenso können im Rahmen der vorliegenden Erfindung mehrere, insbesondere alle, Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung beziehungsweise mehrere, insbesondere alle, Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs jeweils in einer Ebene angeordnet sein. Wie in Figur **1** gezeigt, können die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs dabei in einer gemeinsamen Ebene angeordnet sein.

Im Rahmen einer Ausführungsform der vorliegenden Erfindung ist mindestens eine Antenne **3** beziehungsweise sind die Antennen **3** der Antennenebene bezüglich mindestens einer Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und/oder mindestens einer Diode **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs, insbesondere bezüglich der Ebene der Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und/oder der Ebene der Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs, strahlungsseitig angeordnet.

Durch unterschiedliche Antennendesigns können Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen Absorptionseigenschaften hinsichtlich Frequenz und Polarisation im Terahertzband realisiert werden. Unterschiedliche Antennendesigns bieten eine weitere, insbesondere bevorzugte, Möglichkeit unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

Dabei kann eine Antenne **3** sowohl wie in Figur 1 gezeigt flächig als auch nicht-flächig ausgestaltet sein. Beispielsweise kann eine Antenne **3** im Rahmen der vorliegenden Erfindung

polygon, insbesondere dreieckig, rechteckig und/oder viereckig, im Wesentlichen unrund, insbesondere ellipsoid oder kreisförmig, oder spiralförmig ausgestaltet sein.

Im Rahmen einer Ausführungsform der vorliegenden Erfindung weist der erfindungsgemäße Sensor **1** mindestens zwei Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichem Antennendesign auf. Beispielsweise können mehrere Antennendesigns, insbesondere selektiv, auf einem Sensor **1** kombiniert werden, welche mehrere, beispielsweise beabstandete, Frequenzbänder im Terahertz-Bereich zur Folge haben, welche auf spezielle zu detektierende Frequenzbereiche, beispielsweise für Sprengstoffe charakteristische Frequenzbereiche, abgestimmt sind und dadurch dem erfindungsgemäßen Sensor **1** vorteilhafterweise eine Spektroskopie- und/oder Frequenzselektions-Funktion verleihen.

Im Rahmen einer bevorzugten Ausführungsform der vorliegenden Erfindung weist der erfindungsgemäße Sensor **1** daher mindestens zwei unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen auf, die, insbesondere durch unterschiedliche Antennendesigns, auf spezielle/bevorzugt zu detektierende Frequenzbereiche im Terahertz-Bereich abgestimmt sind.

Im Rahmen einer bevorzugten Ausführungsform der vorliegenden Erfindung umfasst eine Antenne **3** eine, insbesondere dünne, Metallschicht und/oder Halbleiterschicht und/oder eine Schicht aus einem oder mehreren elektrisch leitenden Polymeren und/oder eine auf Kohlenstoffnanoröhren („carbon nanotubes“) basierende Schicht. Insbesondere kann eine Antenne **3** dabei aus einer, insbesondere dünnen, Metallschicht oder Halbleiterschicht oder Schicht aus einem oder mehreren elektrisch leitenden Polymeren oder auf Kohlenstoffnanoröhren („carbon nanotubes“) basierenden Schicht ausgebildet sein. Beispielsweise kann die Metallschicht aus Gold ausgebildet sein. Die Halbleiterschicht kann aus einem Halbleiter mit einer breiten Bandlücke („wide band gap semiconductor“), beispielsweise Indium-Zinn-Oxyd, Zinkoxid, Alluminiumnitrid, Galliumnitrid, und/oder Siliciumcarbid, insbesondere dotiertes Indium-Zinn-Oxyd, Zinkoxid, Alluminiumnitrid, Galliumnitrid, und/oder Siliciumcarbid, ausgebildet sein.

Im Rahmen einer besonders bevorzugten Ausführungsform der vorliegenden Erfindung ist die Metallschicht und/oder Halbleiterschicht durchlässig für Strahlung des sichtbaren bis nahen Infrarot-Bereichs und/oder des mittleren Infrarot-Bereichs. Dies hat den Vorteil, dass unterhalb der Antenne/n **3** einer Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtung eine oder mehrere Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und/oder eine oder

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mehrere Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs angeordnet sein können. Dabei dient der Begriff „unterhalb" nicht dazu die Ausrichtung bezüglich der Gravitationsrichtung, sondern bezüglich der erwarteten Strahlungsrichtung zu definieren, wobei „unterhalb einer Antenne" als auf der strahlungsabgewandten Seite einer Antenne **3** zu verstehen ist.

Im Rahmen der in Figur 1 gezeigten Ausführungsform sind unterhalb den Antennen **3** beziehungsweise zwischen den Antennen **3** und dem komplementären Metall-Oxid-Halbleiter-Substrat **2** zahlreiche Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs angeordnet. Dabei besteht zwischen den Antennen **3** und den Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung beziehungsweise den Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs keine galvanisch leitende Verbindung. Dabei bedeutet „keine galvanisch leitende Verbindung", dass keine „direkte" Leitung über eine, beispielsweise metallische, Leitung vorliegt, wobei eine kapazitive und/oder induktive „indirekte" Leitung nicht ausgeschlossen ist. Eine galvanisch leitende Verbindung zwischen den Antennen **3** und den Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung beziehungsweise den Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs kann beispielsweise dadurch vermieden werden, dass die Antennen **3** auf einem oder mehreren, nicht dargestellten, Träger/n, beispielsweise einer Trägerschicht, insbesondere aus einem oder mehreren nicht galvanisch leitenden Polymeren, aus einem galvanisch nicht-leitenden Material angeordnet sind.

Als Vorrichtung **5** zur Detektion von mittlerer Infrarotstrahlung können im Rahmen der vorliegenden Erfindung Bolometer und/oder MIM-Dioden eingesetzt werden. Der Einsatz von Bolometern und MIM-Dioden bietet daher eine Möglichkeit unterschiedliche Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen. Beim Einsatz von Bolometern **5** als Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung sind die Bolometer **5** vorzugsweise, wie in Figur 1 gezeigt, freistehend ausgebildet und angeordnet.

Als Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung eignet sich beispielsweise ein Bolometer, welches ein in etwa $\geq 25\ \mu m^2$ bis $\leq 4900\ \mu m^2$, insbesondere $\geq 625\ \mu m^2$ bis $\leq 2500\ \mu m^2$, großes schichtförmiges Substrat aufweist. Das schichtförmige Substrat kann dabei insbesondere mittels zwei galvanisch leitenden Stützen beabstandet zu dem CMOS-Substrat **2** angeordnet sein. Dabei kann das schichtförmige Substrat sowohl polygon, insbesondere

rechteckig und/oder viereckig, als auch im Wesentlichen unrund, insbesondere ellipsoid oder kreisförmig, ausgestaltet sein. Das schichtförmige Substrat kann dabei amorphes Silizium oder Vanadiumoxid umfassen. Das schichtförmige Substrat ist vorzugsweise parallel zu dem CMOS-Substrat **2** angeordnet. Durch den Abstand zwischen dem schichtförmigen Substrat und dem CMOS-Substrat **2** kann dabei vorteilhafterweise der Wellenlängenbereich der zu detektierenden Strahlung eingestellt werden. Für eine optimale Detektion entspricht der Abstand vorzugsweise einem Viertel der Wellenlänge der zu detektierenden Strahlung. Eine Änderung des Abstands zwischen dem schichtförmigen Substrat und dem CMOS-Substrat **2** bietet daher eine weitere Möglichkeit unterschiedliche Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

Als Dioden eignen sich beispielsweise Dioden, insbesondere Fotodioden, die in CMOS-bildgebenden Detektoren verwendet werden.

Wie Figur 1 veranschaulicht kann der erfindungsgemäße Sensor **1**, insbesondere ein Teil des erfindungsgemäßen Sensors **1**, beispielsweise das CMOS-Substrat **2**, die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtung/en, die Vorrichtung/en **5** zur Detektion von mittlerer Infrarotstrahlung und die Diode/n **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs des Sensors **1**, vorteilhafterweise monolithisch ausgestaltet sein. Dabei bedeutet der Begriff „monolithisch“, dass die Einheiten **2, 3, 4, 5, 6** des Sensors **1** eine, insbesondere untrennbare, Einheit bilden. Insbesondere kann es sich bei dem erfindungsgemäßen Sensor um einen monolithisch integrierten Chip handeln.

Der in Figur 1 nicht dargestellte Schaltkreis, die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs sind im Rahmen der vorliegenden Erfindung vorzugsweise derart ausgebildet und angeordnet, dass die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs, insbesondere unabhängig voneinander, beschaltet und/oder ausgelesen werden können. Zum Auswerten der ausgelesenen Messergebnisse weist der erfindungsgemäße Sensor **1** vorzugsweise eine Auswertelektronik auf. Darüber hinaus weist der Sensor vorzugsweise eine multispektrale Optik, beispielsweise eine reflektive Optik auf der Basis von Spiegeln, auf. Eine derartige multispektrale Optik ist zweckmäßigerweise bezüglich der auf dem CMOS-Substrat **2** angeordneten Bauelemente **3, 4, 5, 6** strahlungsseitig angeordnet.

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Die Auswertelektronik und multispektrale Optik kann, muss jedoch nicht, in den monolithischen Teil des Sensors **1** integriert sein.

Figur 1 zeigt, dass die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs rasterförmig angeordnet sein können. Dementsprechend können die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs auch als „Pixel" bezeichnet werden. Im Rahmen einer Ausführungsform der vorliegenden Erfindung sind die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs als Pixel eines Rasters von mindestens 20 mal 20, beispielsweise von mindestens 50 mal 50, insbesondere von mindestens 100 mal 100, Pixeln auf dem Sensor **1** angeordnet. Die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs können dabei in einem symmetrischen Muster auf dem Sensor **1** angeordnet sein. Vorzugsweise sind die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs dabei, wie in Figur 1 gezeigt, gleichmäßig auf dem Sensor **1** verteilt angeordnet. Insbesondere können dabei die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs alternierend angeordnet sein. Die Zahl an Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen kann im Rahmen der vorliegenden Erfindung geringer als die der Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und der Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs sein. Die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen können dann beispielsweise, wie in Figur 1 gezeigt, in regelmäßigen Abständen anstelle von einer Vorrichtung **5** zur Detektion von mittlerer Infrarotstrahlung oder Diode **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs in der ansonsten alternierenden Anordnung von Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs angeordnet werden.

Das Verhältnis von Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zu Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung kann im Rahmen der vorliegenden Erfindung in einem Bereich von $\geq$ 1:100 bis $\leq$ 100:1, beispielsweise von $\geq$ 1:50

bis ≤ 50:1, insbesondere von ≥ 1:30 bis ≤ 30:1, und/oder das Verhältnis von Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zu Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs in einem Bereich von ≥ 1:100 bis ≤ 100:**1**, beispielsweise von ≥ 1:50 bis ≤ 50:**1**, insbesondere von ≥ 1:30 bis ≤ 30:**1**, und/oder das Verhältnis von Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung zu Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs in einem Bereich von ≥ **1**:50 bis ≤ 50:**1**, beispielsweise von ≥ 1:10 bis ≤ 10:1, insbesondere von ≥ 1:3 bis ≤ 3:1, liegen. Beispielsweise kann das Verhältnis von Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zu Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung ≥ 1:5, beispielsweise ≥ 1:10, insbesondere ≥ 1:20 , und/oder das Verhältnis von Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zu Dioden **6** ≥ 1:5, beispielsweise ≥ 1:10, insbesondere von ≥ **1**:20, und/oder das Verhältnis von Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung zu Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs etwa **1**:**1**, sein.

Ferner betrifft die vorliegende Erfindung ein multispektrales Bildgebungs- und/oder Spektroskopie-System, welches einen erfindungsgemäßen Sensor **1**, welcher als Detektor dient, und eine Terahertzstrahlungsquelle aufweist. Dabei können der Sensor **1** und die Terahertzstrahlungsquelle bezüglich des zu untersuchenden Objektes sowohl derart angeordnet sein, dass der Sensor **1** die nach dem Durchstrahlen des Objektes verbleibende Strahlung detektiert als auch dass der Sensor **1** die von dem Objekt reflektierte und/oder gestreute Strahlung detektiert. Folglich können die Terahertzstrahlungsquelle, der Sensor **1** und das Objekt sowohl entlang einer Achse angeordnet sein, wobei das Objekt zwischen der Terahertzstrahlungsquelle und dem Sensor angeordnet ist, als auch nicht entlang einer Achse zueinander angeordnet sein.

Das erfindungsgemäße System ermöglicht vorteilhafterweise eine Echtzeit-Spektroskopie im Terahertz-Bereich sowie eine bildgebende Detektierung im Terahertz-Bereich sowie im Infrarot- und sichtbaren und nah-infraroten Bereich.

Darüber hinaus betrifft die vorliegende Erfindung ein Verfahren zur Detektion und/oder Untersuchung von Lebewesen, insbesondere Menschen und Tieren, Gegenständen und Materialien, mit einem erfindungsgemäßen System. Insbesondere kann dieses Verfahren auf Frequenzbereichsspektroskopie basieren. Vorzugsweise strahlt die Terahertzquelle in dem erfindungsgemäßen Verfahren ein schmales Terahertzband, beispielsweise mit einer Breite von

etwa ≥ 20 Gigahertz bis etwa ≤ 200 Gigahertz, insbesondere von etwa ≥ 60 Gigahertz bis etwa ≤ 100 Gigahertz, aus, welches innerhalb eines breiten Frequenzbereichs, beispielsweise in einem Bereich von etwa ≥ 0,3 Terahertz bis etwa ≤ 20 Terahertz, beispielsweise von ≥ 0,3 Terahertz oder von ≥ 0,5 Terahertz oder von ≥ 1 Terahertz bis ≤ 3 Terahertz oder bis ≤ 5 Terahertz oder bis ≤ 10 Terahertz, verändert wird, wobei die transmittierte, reflektierte und/oder gestreute Strahlung durch den erfindungsgemäßen Sensor **1** detektiert, insbesondere gemessen wird. Das Messergebnis des erfindungsgemäßen Sensors **1** kann dabei durch ein Ausgabegerät, beispielsweise ein Display, einen Bildschirm oder einen Drucker, ausgegeben werden.

Weiterhin betrifft die vorliegende Erfindung die Verwendung eines erfindungsgemäßen Sensors **1**, eines erfindungsgemäßen Systems und/oder eines erfindungsgemäßen Verfahrens im Überwachungs/Sicherheitstechnik-, Transport-, Produktions-, Life-Science- und/oder Gesundheitsbereich. Insbesondere betrifft die vorliegende Erfindung die Verwendung eines erfindungsgemäßen Sensors **1**, eines erfindungsgemäßen Systems und/oder eines erfindungsgemäßen Verfahrens zur Detektion und/oder Untersuchung von Lebewesen, insbesondere Menschen und Tieren, Gegenständen und Materialien, insbesondere Sprengstoffen, beispielsweise bei Sicherheitskontrollen an Grenzen, in Transitgebäuden, wie Flughäfen und Bahnhöfen, in Transportmitteln, wie Bahnen, Bussen, Flugzeugen und/oder Schiffen, und/oder bei Großveranstaltungen, zur Einbruchssicherung von Gebäuden, Räumen und Fortbewegungsmitteln, zu medizinischen Zwecken und/oder zur zerstörungsfreien Überprüfung eines Werkstücks („non-destructive testing"), insbesondere von Werkstücken aus Kunststoff.

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Ansprüche

1. Multispektraler Sensor (1), umfassend

   - ein komplementäres Metall-Oxid-Halbleiter-Substrat (2) mit Schaltkreis, und
   - mindestens eine Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtung zur Detektion von Terahertzstrahlung, und
   - mindestens eine Vorrichtung (5) zur Detektion von mittlerer Infrarotstrahlung, und
   - mindestens eine Diode (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs.

2. Sensor (1) nach Anspruch 1, dadurch gekennzeichnet, dass

   - die Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtung eine Antenne-Bolometer-Kombinationsvorrichtung oder eine Antenne-Diode-Kombinationsvorrichtung, insbesondere eine Antenne-Bolometer-, Antenne-Schottky-Diode- oder eine Antenne-Metall-Isolator-Metall-Diode-Kombinationsvorrichtung, und/oder
   - die Vorrichtung (5) zur Detektion von mittlerer Infrarotstrahlung ein Bolometer oder eine Metall-Isolator-Metal-Diode,

   ist.

3. Sensor (1) nach Anspruch 1 oder 2, dadurch gekennzeichnet, dass der Sensor (1)

   - mindestens zwei unterschiedliche Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern; und/oder
   - mindestens zwei unterschiedliche Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern, und/oder,

- mindestens zwei unterschiedliche Diode (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern,

aufweist.

4. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass der Sensor (1) mindestens zwei unterschiedliche Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen aufweist, die derart ausgebildet sind, dass der Terahertz-Bereich in mindestens zwei Unterbänder aufgeteilt wird, welche den Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zugeordnet sind.

5. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass der Sensor (1) mindestens zwei Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen mit unterschiedlichem Antennendesign aufweist.

6. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass der Sensor (1) mindestens zwei unterschiedliche Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen auf, die auf bevorzugt zu detektierende Frequenzbereiche im Terahertz-Bereiche abgestimmt sind.

7. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass der Sensor (1) eine Vielzahl von Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen, Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung und Dioden (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs aufweist, wobei die Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen, Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung und Dioden (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs rasterförmig angeordnet sind.

8. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen, Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung und Dioden (6) zur Detektion von Strahlung des

sichtbaren bis nahen Infrarot-Bereichs als Pixel eines Rasters von mindestens 20 mal 20, beispielsweise von mindestens 50 mal 50, insbesondere von mindestens 100 mal 100, Pixeln auf dem Sensor (1) angeordnet sind.

9. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen, Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung und Dioden (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs in einem symmetrischen Muster auf dem Sensor (1) angeordnet sind.

10. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die Antenne/n (3) eine Metallschicht und/oder eine Halbleiterschicht und/oder eine Schicht aus einem oder mehreren elektrisch leitenden Polymeren und/oder eine auf Kohlenstoffnanoröhren basierende Schicht umfassen, welche durchlässig für Strahlung des sichtbaren bis nahen Infrarot-Bereichs und/oder Infrarotstrahlung ist.

11. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass unterhalb der Antenne/n (3) einer Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen eine oder mehrere Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung und/oder eine oder mehrere Dioden (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs angeordnet sind.

12. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die Antenne/n (3) auf einem oder mehreren Träger/n aus einem galvanisch nicht-leitenden Material angeordnet sind.

13. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass der Sensor (1) eine multispektrale Optik, insbesondere eine reflektive Optik, und/oder eine Auswertelektronik aufweist.

14. Multispektrales Bildgebungs- und/oder Spektroskopie-System, umfassend einen Sensor nach einem der vorhergehenden Ansprüche und eine Terahertzstrahlungsquelle.

15. Verfahren zur Detektion und/oder Untersuchung von Lebewesen, insbesondere Menschen und Tieren, Gegenständen und Materialien, mit einem System nach Anspruch 14, in dem die Terahertzquelle ein schmales Terahertzband ausstrahlt, welches innerhalb eines breiten Frequenzbereichs verändert wird, wobei die transmittierte, reflektierte und/oder gestreute Strahlung durch den erfindungsgemäßen Sensor (1) detektiert wird.

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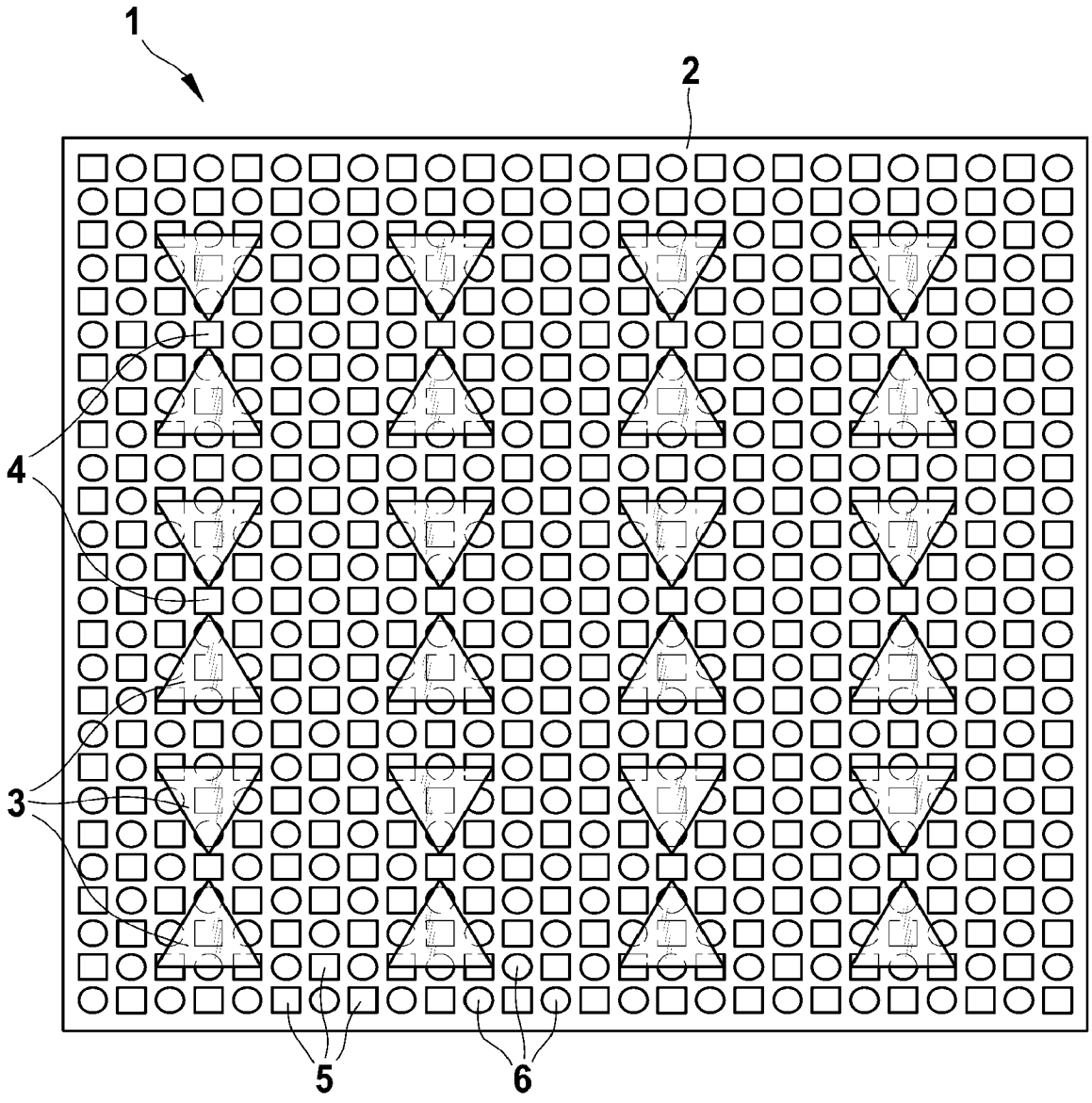

Fig. 1

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
13 January 2011 (13.01.2011)

PCT

(10) International Publication Number
WO 2011/003871 A1

(51) International Patent Classification:
H01L 31/105 (2006.01) *G02B 6/42* (2006.01)
H01L 31/18 (2006.01) *G02F 1/01* (2006.01)
H01L 35/30 (2006.01) *G02F 1/025* (2006.01)
H01L 23/38 (2006.01)

(21) International Application Number:
PCT/EP2010/059571

(22) International Filing Date:
5 July 2010 (05.07.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/498,463 7 July 2009 (07.07.2009) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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(54) Title: A TEMPERATURE CONTROL DEVICE FOR OPTOELECTRONIC DEVICES

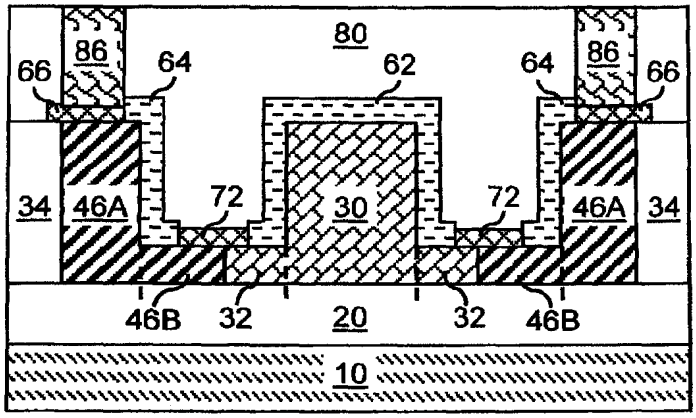

FIG. 9B

(57) Abstract: Current may be passed through an n-doped semiconductor region, a recessed metal semiconductor alloy portion, and a p-doped semiconductor region so that the diffusion of majority charge carriers in the doped semiconductor regions transfers heat from or into the semiconductor waveguide through Peltier-Seebeck effect. Further, a temperature control device may be configured to include a metal semiconductor alloy region located in proximity to an optoelectronic device, a first semiconductor region having a p-type doping, and a second semiconductor region having an n-type doping. The temperature of the optoelectronic device may thus be controlled to stabilize the performance of the optoelectronic device.

WO 2011/003871 A1

SAMSUNG EX. 1002 - 1965/2862

Published:

— *with international search report (Art. 21(3))*

SAMSUNG EX. 1002 - 1966/2862

A TEMPERATURE CONTROL DEVICE FOR OPTOELECTRONIC DEVICES

BACKGROUND

The present invention relates to a semiconductor structure, and particularly to a temperature control device for an optoelectronic device and a germanium photodetector for silicon waveguide, and methods of manufacturing the same, and methods of operating the same.

A semiconductor waveguide may be employed in microphotonic devices to enable high efficiency long range transmission of light over distances in the micrometer range or in the millimeter range. The semiconductor waveguide typically employs a single crystalline semiconductor material to minimize signal loss due to absorption of light. The semiconductor material in the semiconductor waveguide has a relative high refractive index. For example, silicon and germanium have a refractive index of about 3.45 and about 4.0, respectively. A dielectric material having a lower refractive constant surrounds the semiconductor waveguide so that a total reflection condition is satisfied at the interface between the semiconductor waveguide and the dielectric material for light impinging on the interface at a glancing angle. The semiconductor wave guide may thus be employed to transmit light having a wavelength greater than the wavelength corresponding to the band gap of the semiconductor material. Typically, infrared lights are employed in the semiconductor waveguide.

Many microphotonic devices manipulate the light in the semiconductor waveguide in some way. For example, the light in the semiconductor waveguide may be absorbed, reflected, or induced to change the phase. Many of the prior art methods that accomplish such optical manipulation employ exotic materials or special processing steps that are not typically employed in standard complementary metal-oxide-semiconductor (CMOS) processing steps, thereby increasing the manufacturing cost and processing complexity.

In view of the above, there exists a need to provide a structure that manipulates the light in a semiconductor waveguide with standard CMOS processing steps, and methods of manufacturing the same. Particularly, there exists a need to provide a structure that

modulates the phase of the light in the semiconductor waveguide with standard CMOS processing steps, and methods of manufacturing the same.

Further, performance of many optoelectronic devices is temperature sensitive. For example, performance of a semiconductor laser device is significantly affected by temperature variation. In a semiconductor chip integrating conventional semiconductor devices and optoelectronic devices, the performance of optoelectronic devices may be affected significantly due to the heat generated by conventional semiconductor devices and transferred to the optoelectronic devices. Thus, it is necessary to stabilize the temperature of the optoelectronic devices to provide stable operation of the optoelectronic devices within the semiconductor chip.

While placing optoelectronic devices at a location far away from the conventional semiconductor devices the thermal effect on the performance of the optoelectronic devices, such a design lowers the areal density of the conventional semiconductor devices or the optoelectronic devices. Thus, an integrated semiconductor chip including conventional semiconductor devices and optoelectronic devices at high density without adverse impact on the performance of the optoelectronic devices due to the thermal effects on the optoelectronic devices is desired.

BRIEF SUMMARY

The present invention provides a semiconductor waveguide having an integrated thermoelectric temperature control device to enable phase shifting of the light in the semiconductor waveguide and an optoelectronic device having an integrated thermoelectric temperature control device to control the temperature of the optoelectronic device.

In one embodiment of the present invention, a semiconductor waveguide is formed integrally with non-recessed semiconductor regions that are adjoined to the semiconductor waveguide through a recessed semiconductor portion having a lesser thickness than the semiconductor waveguide. One of the non-recessed semiconductor portions and an adjoining region of the recessed semiconductor portion are doped with p-type dopants to form a p-doped

semiconductor region, and another of the non-recessed semiconductor portions and an adjoining region of the recesses semiconductor portion are doped with n-type dopants to form an n-doped semiconductor region. After forming a dielectric spacer that covers sidewalls of the p-doped semiconductor region and the n-doped semiconductor region, the recessed semiconductor portion is metallized to form a recessed metal semiconductor alloy portion. Current is passed through the n-doped semiconductor region, the recessed metal semiconductor alloy portion, and the p-doped semiconductor region. The diffusion of majority charge carriers in the doped semiconductor regions transfers heat from or into the semiconductor waveguide through Peltier-Seebeck effect. The temperature change in the semiconductor waveguide alters refractive index of the semiconductor waveguide, which may be employed to modulate the phase of the light passing through the semiconductor waveguide.

According to an aspect of the present invention, a semiconductor structure is provided, which comprises: a semiconductor waveguide having a first thickness and located on a top surface of an insulator layer; a recessed semiconductor region of integral construction with the semiconductor waveguide, having a second thickness that is less than the first thickness, located on the insulator layer, and including a substantially undoped recessed semiconductor region; a p-doped semiconductor region laterally abutting the substantially undoped recessed semiconductor region; an n-doped semiconductor region laterally abutting the substantially undoped recessed semiconductor region and not abutting the p-doped semiconductor region; and a recessed metal semiconductor alloy portion abutting the recessed semiconductor region, the p-doped semiconductor region, and the n-doped semiconductor region.

According to another aspect of the present invention, a method of forming a semiconductor structure is provided, which comprises: forming shallow trench isolation structures laterally abutting a top semiconductor portion and vertically abutting a buried insulator layer in a top semiconductor layer of a semiconductor-on-insulator (SOI) substrate; forming a semiconductor waveguide by patterning the top semiconductor portion; forming a p-doped semiconductor region in the top semiconductor portion; forming an n-doped semiconductor region not abutting the p-doped semiconductor region in the top semiconductor region; and

forming a recessed metal semiconductor alloy portion directly on a recessed region of the top semiconductor portion, wherein the recessed metal semiconductor alloy portion is formed directly on the p-doped semiconductor region and the n-doped semiconductor region.

According to yet another aspect of the present invention, a method of operating a semiconductor device is provided, which comprises: providing a semiconductor structure including: a semiconductor waveguide located on a top surface of an insulator layer; a p-doped semiconductor region thermally connected to the silicon waveguide; an n-doped semiconductor region thermally connected to the silicon waveguide and not abutting the p-doped semiconductor region; and a recessed metal semiconductor alloy portion abutting the p-doped semiconductor region and the n-doped semiconductor region; and passing current through the n-doped semiconductor region, the recessed metal semiconductor alloy portion, and the p-doped semiconductor region.

In another embodiment of the present invention, an optoelectronic device is formed on a semiconductor substrate in proximity to a temperature control device. A semiconductor waveguide that is optically coupled to the optoelectronic device may be formed to enable transmission of optical signal through the semiconductor waveguide. The temperature control device is configured to include a metal semiconductor alloy region located in proximity to the optoelectronic device, a first semiconductor region having a p-type doping, and a second semiconductor region having an n-type doping. The metal semiconductor alloy region is thermally coupled with the optoelectronic device. Electrical current may be caused to flow through the first semiconductor region, the metal semiconductor alloy region, and the second semiconductor region to allow cooling of the metal semiconductor alloy region and the optoelectronic device through heat transfer. Conversely, the current may be caused to flow in the opposite direction to allow heating of the metal semiconductor alloy region and the optoelectronic device through heat transfer. The temperature of the optoelectronic device may thus be controlled to stabilize the performance of the optoelectronic device.

According to an aspect of the present invention, a semiconductor structure including a temperature control device and an optoelectronic device is provided. The temperature control device includes: a first metal semiconductor alloy region located on a substrate; a p-

doped semiconductor portion abutting the first metal semiconductor alloy region and located on the substrate; an n-doped semiconductor portion abutting the first metal semiconductor alloy region located on the substrate; wherein the temperature control device is configured to pass current from the p-doped semiconductor portion, through the first metal semiconductor alloy region, and to the n-doped semiconductor portion or from the n-doped semiconductor portion, through the first metal semiconductor alloy region, and to the p-doped semiconductor portion. The optoelectronic device includes a device that comprises a semiconductor material, configured to manipulate electromagnetic radiation, and is thermally coupled to the temperature control device.

According to another aspect of the present invention, a method of forming a semiconductor structure including a temperature control device and an optoelectronic device is provided. The method includes: patterning a top semiconductor layer of a semiconductor-on-insulator substrate to form a p-doped semiconductor portion and an n-doped semiconductor portion; forming a first metal semiconductor alloy region directly on the p-doped semiconductor portion and the n-doped semiconductor portion, wherein the p-doped semiconductor portion and an n-doped semiconductor portion and the first metal semiconductor alloy region constitute a portion of a temperature control device; forming a current conduction path configured to pass current from the p-doped semiconductor portion, through the first metal semiconductor alloy region, and to the n-doped semiconductor portion or from the n-doped semiconductor portion, through the first metal semiconductor alloy region, and to the p-doped semiconductor portion; and forming an optoelectronic device comprising a semiconductor material, configured to manipulate electromagnetic radiation, and is thermally coupled to the temperature control device.

According to yet another aspect of the present invention, a method of operating a semiconductor structure comprising a temperature control device and an optoelectronic device is provided. The method includes: providing a temperature control device including a first metal semiconductor alloy region located on a substrate, a p-doped semiconductor portion abutting the first metal semiconductor alloy region and located on the substrate, and an n-doped semiconductor portion abutting the first metal semiconductor alloy region located on the substrate; providing an optoelectronic device including a device that

comprises a semiconductor material, configured to manipulate electromagnetic radiation, and is thermally coupled to the temperature control device; and passing electrical current from the p-doped semiconductor portion, through the first metal semiconductor alloy region, and to the n-doped semiconductor portion or from the n-doped semiconductor portion, through the first metal semiconductor alloy region, and to the p-doped semiconductor portion, wherein heat is transferred in the direction of flow of majority charge carriers in the p-doped semiconductor portion and the n-doped semiconductor portion.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Embodiments of the present invention will now be described, by way of example only, with reference to the accompanying drawings in which:

FIGS. 1A – 1C are various views of a first exemplary semiconductor structure corresponding to the step after formation of a shallow trench isolation structures 34;

FIGS. 2A – 2C are various views of the first exemplary semiconductor structure corresponding to the step after formation of a pair of recessed line trenches 31;

FIGS. 3A – 3C are various views of the first exemplary semiconductor structure corresponding to the step after removal of a first photoresist (37A, 37B, 37C);

FIGS. 4A – 4C are various views of the first exemplary semiconductor structure corresponding to the step after formation of p-doped semiconductor regions (46A, 46B);

FIGS. 5A – 5C are various views of the first exemplary semiconductor structure corresponding to the step after formation of n-doped semiconductor regions (48A, 48B);

FIGS. 6A – 6C are various views of the first exemplary semiconductor structure corresponding to the step after removal of a third photoresist 47;

FIGS. 7A – 7C are various views of the first exemplary semiconductor structure corresponding to the step after formation of a dielectric material layer 60L;

FIGS. 8A – 8C are various views of the first exemplary semiconductor structure corresponding to the step after formation of a dielectric material portion 62 and dielectric spacers 64;

FIGS. 9A – 9C are various views of the first exemplary semiconductor structure corresponding to the step after formation of various metal semiconductor alloy portions, a middle-of-line (MOL) dielectric layer 80, and various conductive contact vias;

FIGS. 10, 11, and 12A, 12B, 13A, 13B, 14A, 14B, 15A, 15B, 16A, and 16B are various views of a second exemplary semiconductor structure corresponding to a second embodiment of the present invention. FIGS. 10 and 11 are vertical cross-sectional views. Each of FIG. 12A, 13A, 13A, 14A, 15A, and 16A is a vertical cross-sectional view along a vertical plane labeled Z – Z' in figures with the numeric label and the suffix "B." FIGS. 11B, 12B, 13B, and 14B are top-down views. FIG. 15B is a top-down view of selected elements to demonstrate lateral geometrical relationship between the selected elements;

FIG. 17 is a vertical cross-sectional view of a third exemplary semiconductor structure;

FIG. 18 is a vertical cross-sectional view of a fourth exemplary semiconductor structure;

FIG. 19 is a vertical cross-sectional view of a fifth exemplary semiconductor structure;

FIGS. 20 and 21 are sequential vertical cross-sectional views of a sixth exemplary semiconductor structure; and

FIG. 22 is a top-down view of selected elements to demonstrate lateral geometrical relationship between the selected elements of a seventh exemplary semiconductor structure according to a seventh embodiment of the present invention.

For all of the figures herein, the following conventions apply. Figures with the same numeric label correspond to the same stage of manufacturing for an exemplary semiconductor structure. Within FIGS. 1A – 9C, figures with the suffix "A" are top-down views, and figures with the suffix "B" or "C" are horizontal cross-sectional views along the plane B – B' or the plane C – C', respectively, in the figure with the same numeric label and the suffix "A."

DETAILED DESCRIPTION

As stated above, the present invention relates to a temperature control device for an optoelectronic device and a germanium photodetector for silicon waveguide, and methods of manufacturing the same, and methods of operating the same, which are now described in detail with accompanying figures. Throughout the drawings, the same reference numerals or letters are used to designate like or equivalent elements. Detailed descriptions of known functions and constructions unnecessarily obscuring the subject matter of the present invention have been omitted for clarity. The drawings are not necessarily drawn to scale.

Referring to FIGS. 1A – 1F, an exemplary semiconductor structure according to the present invention comprises a semiconductor substrate, which is a semiconductor-on-insulator (SOI) substrate. The semiconductor substrate includes an insulator layer 20 and a top semiconductor layer located above the insulator layer 20. The semiconductor substrate may further include a handle substrate 10, which is attached to the bottom surface of the insulator layer 20. The handle substrate 10 may comprise a semiconductor material, an insulator material, a conductive material, or a combination thereof. The insulator layer 20 and the handle substrate 10, if present, provide structural support to the top semiconductor layer which may comprise a contiguous semiconductor material layer that covers the entirety of the insulator layer 20.

The contiguous semiconductor material layer comprises a semiconductor material. Exemplary semiconductor materials that may be employed for the contiguous semiconductor material layer include, but are not limited to, silicon, germanium, silicon-germanium alloy, silicon carbon alloy, silicon-germanium-carbon alloy, gallium arsenide, indium arsenide, indium phosphide, III-V compound semiconductor materials, II-VI compound

semiconductor materials, organic semiconductor materials, and other compound semiconductor materials. Preferably, the entirety of the contiguous semiconductor material layer comprises a single crystalline semiconductor material having an epitaxial alignment among the semiconductor atoms. For example, the semiconductor material of the contiguous semiconductor material layer may comprise single crystalline silicon or single crystalline germanium. The thickness of the contiguous semiconductor material layer, which is herein referred to as a first thickness *t1*, may be from about 50 nm to about 1,000 nm, and typically from about 200 nm to about 500 nm, although lesser and greater thicknesses can also be employed.

Preferably, the contiguous semiconductor material layer comprises a substantially undoped semiconductor material so that the amount of impurities, including dopant atoms, in the contiguous semiconductor material layer is minimized. By minimizing the amount of impurities in the contiguous material layer, a semiconductor waveguide to be subsequently formed from a portion of the contiguous material layer provides low absorption rate of the signal. The atomic concentration of impurities, including dopants, in the contiguous semiconductor material layer is less than about $1.0 \times 10^{16}/cm^3$, and preferably less than about $1.0 \times 10^{15}/cm^3$, and more preferably less than about $1.0 \times 10^{14}/cm^3$. In case the contiguous semiconductor material layer comprises silicon, the resistivity of the material of the contiguous semiconductor material layer is greater than about 1 Ohm-cm, and preferably greater than about 10 Ohm-cm, and more preferably greater than about 100 Ohm-cm.

Trenches extending to the top surface of the insulator layer 20 are formed within the contiguous semiconductor material layer by a combination of lithographic means and an etch. Specifically, a photoresist (not shown) is applied over the top surface of the contiguous semiconductor material layer and lithographically patterned. The pattern in the photoresist is transferred into the contiguous semiconductor material layer by the etch, which is typically an anisotropic etch. After removal of the photoresist, the trenches are filled with a dielectric material such as a dielectric oxide, a dielectric nitride, a dielectric nitride, or a combination thereof. For example, silicon oxide and/or silicon nitride may be deposited into the trenches. The dielectric material above the top surface of the contiguous semiconductor material layer is removed, for example, by chemical mechanical planarization. The remaining portions of

the dielectric material filling the trenches constitute shallow trench isolation (STI) structures 34. Pad dielectric layers (not shown) may be employed to facilitate the planarization process.

The remaining portion of the contiguous semiconductor material layer constitutes a top semiconductor portion, which includes a primary top semiconductor portion 30P, first laterally protruding top semiconductor portions 30A, and second laterally protruding top semiconductor portions 30B. The primary top semiconductor portion 30P, the first laterally protruding top semiconductor portions 30A, and the second laterally protruding top semiconductor portions 30B comprise the same semiconductor material, have the same thickness, i.e., the first thickness *t1*, and are epitaxially aligned among one another. The sidewalls of the top semiconductor portion (30P, 30A, 30B) are laterally abutted by the shallow trench isolation structures 34. The first laterally protruding top semiconductor portions 30A and the second laterally protruding top semiconductor portions 30B laterally protrude out of the sidewalls of the primary top semiconductor portion 30P into the shallow trench isolation structures 34. Thus, each of the first laterally protruding top semiconductor portions 30A and the second laterally protruding top semiconductor portions 30B may comprise multiple sidewalls that laterally abut the shallow trench isolation structures 34. The shallow trench isolation structures 34 and the top semiconductor portion (30P, 30A, 30B) have substantially the same thickness, i.e., the first thickness *t1*.

At least one pair of a first laterally protruding top semiconductor portions 30A and a second laterally protruding top semiconductor portions 30B may be formed on one side of the primary top semiconductor portion 30P, and at least another pair of a first laterally protruding top semiconductor portions 30A and a second laterally protruding top semiconductor portions 30B may be formed on an opposite side of the primary top semiconductor portion 30P. The width of the semiconductor portion *SPW* may be from about 400 nm to about 3,000 nm, and preferably from about 600 nm to about 1,500 nm, although lesser and greater widths can also be employed. The length of the semiconductor portion *SPL* is the length of a semiconductor waveguide that is intended to be manufactured, and may be from about 10 μm to about 3 cm, and typically from about 30 μm to about 1 cm, although lesser and greater lengths can also be employed. Further, configurations for a

semiconductor waveguide having a curvature or a taper can also be employed, in which the shape of the top semiconductor portion (30P, 30A, 30B) are adjusted with a curvature, a taper, and/or other suitable geometric adjustments.

Referring to FIGS. 2A – 2C, a first photoresist is applied over the top surfaces of the top semiconductor portion (30P, 30A, 30B) and the shallow trench isolation structures 34 and lithographically patterned. The pattern in the first photoresist includes a pair of line troughs separated by a central photoresist portion 37A, which is a remaining portion of the first photoresist after lithographic patterning. The central photoresist portion 37A has a constant width, which is herein referred to as a waveguide width *ww*. The waveguide width *ww* may be from about 200 nm to about 1,500 nm, and preferably from about 300 nm to about 750 nm, although lesser and greater widths can also be employed. The remaining portions of the first photoresist include a first-side photoresist portion 37B and a second-side photoresist portion 37C, which are separated from the central photoresist portion 37A by the pair of line troughs. Each of the line troughs may have a substantially constant width, which is herein referred to as a line trough width *ltw*. The two line troughs may have the same line trough width *ltw*, or may have different line trough widths *ltw*. The sum of the two line trough widths *ltw* and the waveguide width *ww* may be less than, equal to, or greater than the width of the semiconductor portion *SPW*. While the present invention is described for the case in which the sum of the two line trough widths *ltw* and the waveguide width *ww* is less than the width of the semiconductor portion *SPW*, embodiments in which the sum of the two line trough widths *ltw* and the waveguide width *ww* is equal to, or greater than, the width of the semiconductor portion *SPW* are explicitly contemplated herein.

The pattern in the patterned portions of the first photoresist, i.e., the set of the central photoresist portion 37A, the first-side photoresist portion 37B, and the second-side photoresist portion 37C is transferred into the primary top semiconductor portion 30P, for example, by an anisotropic etch such as a reactive ion etch (RIE). The exposed portions of the primary top semiconductor portion 30P are vertically recessed by a recess depth *rd*, which is less than the first thickness *t1*. A pair of recessed line trenches 31 is formed directly underneath the two line troughs between the central photoresist portion 37A and each of the first-side and second-side photoresist portions (37B, 37C).

The recessed portions of the primary top semiconductor portion 30P are herein referred to as recessed semiconductor regions 30R. The recessed semiconductor regions have a second thickness *t2*, which is equal to the difference between the first thickness *t1* and the recess depth *rd*. The second thickness *t2* may be from about 10 nm to about 200 nm, and typically from about 30 nm to about 100 nm, although lesser and greater thicknesses can also be employed. The remaining sub-portion of the primary top semiconductor portion 30P underneath the central photoresist portion 37A is herein referred to a semiconductor waveguide 30. The semiconductor waveguide 30 has the first thickness *t1* and the waveguide width *ww*. The semiconductor waveguide 30 may be employed to transmit light along the direction of the length of the semiconductor portion *SPL* (See FIG. 1A). The sub-portions of the top semiconductor portion 30P directly underneath the pair of line trenches 31 are the recessed semiconductor regions 30R, which are of integral construction with the semiconductor waveguide 30.

The first-side photoresist portion 37B and the second-side photoresist portion 37C cover the upper surfaces of the first laterally protruding top semiconductor portions 30A and the second laterally protruding top semiconductor portions 30B. Thus, the first-side photoresist portion 37B and the second-side photoresist portion 37C are not recessed by the anisotropic etch, and have the first thickness *t1*. Each of the first laterally protruding top semiconductor portions 30A and the second laterally protruding top semiconductor portions 30B is a sup-portion of the top semiconductor portion (30P, 30A, 30b) having the first thickness *t1*. Sidewalls of the first laterally protruding top semiconductor portions 30A and the second laterally protruding top semiconductor portions 30B are exposed to the pair of recessed line trenches 31.

The semiconductor waveguide 30, the recessed semiconductor regions 30R, the first-side photoresist portions 37B, and the second-side photoresist portions 37C are of integral and unitary construction, i.e., in a single contiguous structure without any interface therebetween. In case the entirety of the top semiconductor portion (30P, 30A, 30B) is single crystalline prior to the formation of the semiconductor waveguide 30, the semiconductor waveguide 30, the recessed semiconductor regions 30R, the first-side photoresist portions 37B, and the second-side photoresist portions 37C are single crystalline

and epitaxially aligned among one another. In case the semiconductor substrate is an SOI substrate, the semiconductor waveguide 30, the semiconductor waveguide 30, the recessed semiconductor regions 30R, the first-side photoresist portion 37B, the second-side photoresist portion 37C, and the shallow trench isolation structures 34 are formed in a top semiconductor layer of the SOI substrate.

Referring to FIGS. 3A – 3C, the first photoresist is removed selective to the semiconductor material of the semiconductor waveguide 30, the recessed semiconductor regions 30R, the first-side photoresist portion 37B, the second-side photoresist portion 37C. Preferably, the removal of the first photoresist is selective to the dielectric material of the shallow trench isolation structures 34. While the present invention is described for the case in which edges of the recessed line trenches 31 is coincident with the sidewalls of the shallow trench isolation structures 34 that laterally abut the primary top semiconductor portion 30P (See FIG. 1A), embodiments in which the edges of the recessed line trenches 31 is offset from the sidewalls of the shallow trench isolation structures 34 inward or outward are explicitly contemplated herein.

Referring to FIGS. 4A – 4C, a second photoresist 45 is applied over the first exemplary semiconductor structure and lithographically patterned to form openings. The first laterally protruding top semiconductor portions 30A are exposed within the openings. Further, portions of the recessed semiconductor regions 30R that adjoin the first laterally protruding top semiconductor portions 30A are also exposed within the opening in the second photoresist 45. The second photoresist 45 covers the entirety of the semiconductor waveguide 30 and the second laterally protruding top semiconductor portions 30B. Further, the second photoresist 45 covers portions of the recessed semiconductor regions 30R that laterally abut the semiconductor waveguide 30.

P-type dopants are implanted into the first laterally protruding top semiconductor portions 30A and the exposed portions of the recessed semiconductor regions 30R. P-type dopants may be boron, gallium, indium, or a combination thereof. Preferably, the dose and the energy of the p-type dopants are selected to provide a heavy doping in the implanted regions. For example, the atomic concentration of p-type dopants in the implanted regions may be

from about 1.0 x 10^{19}/cm^3 to about 1.0 x 10^{21}/cm^3, and typically from about 5.0 x 10^{19}/cm^3 to about 5.0 x 10^{20}/cm^3, although lesser and greater dopant concentrations can also be employed.

The first laterally protruding top semiconductor portions 30A as implanted with the p-type dopants are herein referred to as p-doped non-recessed semiconductor regions 46A, which has a third thickness *t3*. Typically, the third thickness *t3* is the same as the first thickness *t1*. The portions of the recessed semiconductor regions 30R that are implanted with the p-type dopants are herein referred to as p-doped recessed semiconductor regions 46B. A contiguous pair of a p-doped non-recessed semiconductor region 46A and a p-doped recessed semiconductor region 46B collectively constitutes a p-doped semiconductor region (46A, 46B). The portions of the recessed semiconductor regions 30R that are not implanted with the p-type dopants are herein referred to as substantially undoped recessed semiconductor regions 32, which has the same composition as the semiconductor waveguide 30, i.e., has a total concentration of impurities, including dopants, less than about 1.0 x 10^{16}/cm^3.

Within each p-doped semiconductor region (46A, 46B), a p-doped non-recessed semiconductor region 46A laterally abuts a p-doped recessed semiconductor region 46B. Further, each p-doped recessed semiconductor region 46B laterally abuts a substantially undoped recessed semiconductor region 32. The second photoresist 45 is subsequently removed.

Referring to FIGS. 5A – 5C, a third photoresist 47 is applied over the first exemplary semiconductor structure and lithographically patterned to form openings. The second laterally protruding top semiconductor portions 30B are exposed within the openings. Further, portions of the substantially undoped recessed semiconductor regions 32 that adjoin the second laterally protruding top semiconductor portions 30B are also exposed within the opening in the third photoresist 47. The third photoresist 47 covers the entirety of the semiconductor waveguide 30 and the p-doped semiconductor region (46A, 46B). Further, the third photoresist 47 covers portions of the substantially undoped recessed semiconductor regions 32 that laterally abut the semiconductor waveguide 30.

N-type dopants are implanted into the second laterally protruding top semiconductor portions 30B and the exposed portions of the substantially undoped recessed semiconductor regions 32. N-type dopants may be phosphorus, arsenic, antimony, or a combination thereof. Preferably, the dose and the energy of the n-type dopants are selected to provide a heavy doping in the implanted regions. For example, the atomic concentration of n-type dopants in the implanted regions may be from about $1.0 \times 10^{19}/cm^3$ to about $1.0 \times 10^{21}/cm^3$, and typically from about $5.0 \times 10^{19}/cm^3$ to about $5.0 \times 10^{20}/cm^3$, although lesser and greater dopant concentrations can also be employed.

The second laterally protruding top semiconductor portions 30B as implanted with the n-type dopants are herein referred to as n-doped non-recessed semiconductor regions 48A, which has the third thickness *t3*. The portions of the substantially undoped recessed semiconductor regions 32 that are implanted with the n-type dopants are herein referred to as n-doped recessed semiconductor regions 48B. A contiguous pair of an n-doped non-recessed semiconductor region 48A and an n-doped recessed semiconductor region 48B collectively constitutes an n-doped semiconductor region (48A, 48B). The substantially undoped recessed semiconductor regions 32 is reduced as portions of the substantially undoped recessed semiconductor regions 32 are converted into the n-doped recessed semiconductor regions 48B.

Within each n-doped semiconductor region (48A, 48B), an n-doped non-recessed semiconductor region 48A laterally abuts an n-doped recessed semiconductor region 48B. Further, each n-doped recessed semiconductor region 48B laterally abuts a substantially undoped recessed semiconductor region 32. The third photoresist 47 is subsequently removed.

Referring to FIGS. 6A – 6C, the first exemplary semiconductor structure after removal of the third photoresist 47 is shown. The substantially undoped recessed semiconductor regions 32, the p-doped recessed semiconductor regions 46B, and the n-doped recessed semiconductor regions 48B collectively constitute the recessed semiconductor regions (32, 46B, 48B). The recessed semiconductor regions (32, 46B, 48B) underlie the pair of recessed line trenches 31. The p-doped non-recessed semiconductor regions 48A, the n-doped non-

recessed semiconductor regions 48A, and the semiconductor waveguide 30 are not recessed. Each of the p-doped non-recessed semiconductor regions 48A and the n-doped non-recessed semiconductor regions 48A has a sidewall that is exposed to one of the recessed line trenches 31. The semiconductor waveguide 30 has two substantially parallel and substantially vertical sidewalls separated by the waveguide width *ww*. Each sidewall of the semiconductor waveguide 30 is exposed to one of the two recessed line trenches 31.

Referring to FIGS. 7A – 7C, a dielectric layer 60L is formed directly on the exposed surfaces of the first exemplary semiconductor structure including the top surface and the sidewall surfaces of the semiconductor waveguide 30, the top surfaces of the recessed semiconductor regions (32, 46B, 48B), the top surfaces and the sidewalls of the p-doped non-recessed semiconductor region 46A and the n-doped non-recessed semiconductor region 48A, and the top surfaces of the shallow trench isolation structures 34. The dielectric layer 60L comprises a dielectric material such as a dielectric oxide, a dielectric nitride, a dielectric oxynitride, or a combination thereof. For example, the dielectric layer 60L may comprise silicon nitride or silicon oxide. The dielectric material for the dielectric layer 60L has a lower refractive index than the semiconductor material of the semiconductor waveguide 30.

The dielectric layer 60L may be conformal or non-conformal. The thickness of the dielectric layer 60L, as measured on the top surface of the semiconductor waveguide 30, may be from about 4 nm to about 100 nm, and typically from about 10 nm to about 50 nm, although lesser and greater thicknesses can also be employed. The dielectric layer 60L may be formed by low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), rapid thermal chemical vapor deposition (RTCVD), atomic layer deposition (ALD), etc.

Referring to FIGS. 8A – 8C, the dielectric layer 60L is lithographically patterned into at least three portions. The lithographic patterning may be effected by applying a photoresist (not shown) to the top surface of the dielectric layer 60L and lithographically patterning the photoresist, followed by a pattern transfer into the dielectric layer by an etch. The etch may be an anisotropic etch or an isotropic etch.

Remaining portions of the dielectric layer 60L after the lithographic patterning include a dielectric material portion 62 which covers the entirety of the top surface and sidewalls of the semiconductor waveguide 30. The remaining portions of the dielectric layer 60L further includes dielectric spacers 64, each of which is located directly on at least one of a sidewall of a p-doped non-recessed semiconductor region 46A and a sidewall of an n-doped non-recessed semiconductor region 48A. In one embodiment, a dielectric spacer 64 may be formed contiguously and directly on a sidewall of a p-doped non-recessed semiconductor region 46A, a sidewall of an n-doped non-recessed semiconductor region 48A, and a sidewall of one of the shallow trench isolation structures 34 that is located between the p-doped non-recessed semiconductor region 46A and the sidewall of an n-doped non-recessed semiconductor region 48A. Horizontal surfaces of the p-doped non-recessed semiconductor regions 46A, the n-doped non-recessed semiconductor regions 48A, the p-doped recessed semiconductor regions 46B, and the n-doped recessed semiconductor regions 48B are exposed. All sidewalls of the p-doped non-recessed semiconductor regions 46A and the n-doped non-recessed semiconductor regions 48A are covered by the dielectric spacers 64.

On each side of the semiconductor waveguide 30, a contiguous set of exposed semiconductor surfaces is formed, which includes a top surface of a p-doped recessed semiconductor regions 46B, a top surface of an n-doped recessed semiconductor regions 48B, and a top surface of a portion of a substantially undoped recessed semiconductor regions 32 located therebetween.

Referring to FIGS. 9A – 9C, various metal semiconductor alloy portions are formed on the exposed semiconductor surfaces of the first exemplary semiconductor structure. Specifically, recessed metal semiconductor alloy portions 72 are formed directly on the exposed surfaces of the recessed semiconductor regions (32, 46B, 48B). First metal semiconductor alloy portions 66 are formed directly on the top surfaces of the p-doped non-recessed semiconductor regions 46A. Second metal semiconductor alloy portions 68 are formed directly on the top surfaces of the n-doped non-recessed semiconductor regions 46B.

The various metal semiconductor alloy portions (72, 66, 68) may be formed by methods known in the art such as deposition of a blanket metal layer, anneal at an elevated

temperature to induce formation of metal semiconductor alloy materials, and removal of unreacted portions of the blanket metal layer. In case the semiconductor material of the recessed semiconductor regions (32, 46B, 48B) and the doped non-recessed semiconductor regions (46A, 48A) comprise silicon, the various metal semiconductor alloy portions (72, 66, 68) comprise a metal silicide. In case the semiconductor material of the recessed semiconductor regions (32, 46B, 48B) and the doped non-recessed semiconductor regions (46A, 48A) comprise germanium, the various metal semiconductor alloy portions (72, 66, 68) comprise a metal germanide. The recessed metal semiconductor alloy portions 72, the first metal semiconductor alloy portions 66, and the second metal semiconductor alloy portions 68 comprise the same metal semiconductor alloy material.

A middle-of-line (MOL) dielectric material layer 80 is formed on the first exemplary semiconductor structure. The pair of line troughs 31 is filled with the MOL dielectric layer 80. The dielectric materials that may be used for the MOL dielectric layer 80 include, but are not limited to, a silicate glass, an organosilicate glass (OSG) material, a SiCOH-based low-k material formed by chemical vapor deposition, a spin-on glass (SOG), or a spin-on low-k dielectric material such as SiLK™, etc. The silicate glass includes an undoped silicate glass (USG), borosilicate glass (BSG), phosphosilicate glass (PSG), fluorosilicate glass (FSG), borophosphosilicate glass (BPSG), etc. The dielectric material may be a low dielectric constant (low-k) material having a dielectric constant less than 3.0. The dielectric material may non-porous or porous.

A conductive contact via is formed directly on each of the first metal semiconductor alloy portions 66 and the second metal semiconductor alloy portions 68. Specifically, a first conductive contact via 86 is formed directly on each of the first metal semiconductor alloy portion 66, and a second conductive contact via 88 is formed directly on each of the second metal semiconductor alloy portion 68. The first and second metal semiconductor alloy portions (66, 68) comprise a conductive material such as doped polysilicon, a doped silicon-containing semiconductor material, W, Cu, Al, TaN, TiN, Ta, Ti, or a combination thereof.

Heat may be transferred between the semiconductor waveguide 30 and the set of the first metal semiconductor alloy portions 66 and the second metal semiconductor alloy portions 68

by passing current. Specifically, a voltage bias may be applied across a resistively connected pair of a first conducive contact via 86 and a second conductive contact via 88.

In one embodiment, the second conductive contact via 88 is held at a positive voltage relative to the first conductive contact via 86. In this case, electrical current flows from the second conductive contact via 88, then through a second metal semiconductor alloy portion 68, then through an n-doped non-recessed semiconductor region 48A, then through an n-doped recessed semiconductor region 48B, then through a recessed metal semiconductor alloy portion 72, then through a p-doped recessed semiconductor region 46B, then through a p-doped non-recessed semiconductor region 46A, then through a first metal semiconductor alloy portion 66, and into the first conductive contact via 86. In metallic materials or metal semiconductor alloy portions in the current path, electrons move in the opposite direction of the current flow to conduct electricity.

In semiconductor material portions, majority charge carriers provide electrical conduction. Specifically, holes having positive charges travel in the p-doped recessed semiconductor region 46B and the p-doped non-recessed semiconductor region 46A along the direction from the recessed metal semiconductor alloy portion 72 toward the first metal semiconductor alloy portion 66. Electrons having negative charges travel in the n-doped recessed semiconductor region 48B and the n-doped non-recessed semiconductor region 48A along the direction from the recessed metal semiconductor alloy portion 72 toward the second metal semiconductor alloy portion 68. Thus, the majority charge carriers travel away from the recessed metal semiconductor alloy portion 72 in the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B).

The mechanism of Peltier-Seebeck effect is in operation in the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B). According to Peltier-Seebeck effect, heat transfer accompanies diffusion of charge carriers in a semiconductor material and vice versa. In this case, the majority charge carriers diffuse away from the interface with the recessed metal semiconductor alloy portion 72 toward the interface with the first or second metal semiconductor alloy portion (66 or 68) in each of the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B).

Therefore, there is a net heat transfer from the recessed metal semiconductor alloy portion 72 to the first and second metal semiconductor alloy portions (66, 68). The heat that is transferred to the first and second metal semiconductor alloy portions (66, 68) may further be transferred to a heat sink through the first and second conductive contact vias (86, 88) and other metal interconnect structures (not shown) attached thereto.

Since the semiconductor waveguide 30, the recessed semiconductor regions (32, 46B, 48B), the p-doped semiconductor region (46A, 46B), and the n-doped semiconductor region (48A, 48B) are of integral construction without any interface therebetween, the entirety of the semiconductor waveguide 30, the recessed semiconductor regions (32, 46B, 48B), the p-doped semiconductor region (46A, 46B), and the n-doped semiconductor region (48A, 48B) is thermally connected among one another. Continual transfer of heat from the recessed metal semiconductor alloy portions 72, through the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B), and into the first and second metal semiconductor alloy portions (66, 68) cools the semiconductor waveguide 30.

Cooling of the semiconductor waveguide 30 affects the refractive index of the semiconductor material of the semiconductor waveguide. For example, single crystalline silicon has a wavelength-dependent refractive index, which is from about 3.42 to about 3. 56 between the wavelength range from about 1 micron to about 6 microns. The temperature dependency of the refractive index of silicon is about 1.6×10^{-4} per degree Celsius. Germanium has similar temperature dependency as silicon.

Temperature change in the semiconductor waveguide 30 may be advantageously employed to change the phase of light passing through the semiconductor waveguide. For example, light having a wavelength of about 3.42 micron in vacuum has a wavelength of about 1.00 micron in a semiconductor waveguide 30 that consists essentially of silicon. 1 degree change in the temperature of the semiconductor waveguide 30 induces a phase change of about $2\pi \times 1.6 \times 10^{-4}$ radian per 1 micron. The light changes phase by π radian after traveling about 3.125 mm. By employing a beam splitter connected to two semiconductor waveguides 30 and modulating the phase of the light in one of the semiconductor waveguides 30, constructive interference or destructive interference may be induced between

the two beams as the phase of one beam is modulated through cooling. Thus, by modulating the refractive index of a semiconductor waveguide 30 through the temperature change in the semiconductor waveguide 30 caused by heat transfer out of the semiconductor waveguide 30, the phase of the light passing through the semiconductor waveguide 30 may be modulated.

In another embodiment, the second conductive contact via 88 is held at a negative voltage relative to the first conductive contact via 86. In this case, electrical current flows from the first conductive contact via 86, then through a first metal semiconductor alloy portion 66, then through a p-doped non-recessed semiconductor region 46A, then through a p-doped recessed semiconductor region 46B, then through a recessed metal semiconductor alloy portion 72, then through an n-doped recessed semiconductor region 48B, then through an n-doped non-recessed semiconductor region 48A, then through a second metal semiconductor alloy portion 68, and into the second conductive contact via 88. In other words, the electrical current flows in the opposite direction of the current flow in the previous embodiment.

In this case, holes in the p-doped semiconductor region (46A, 46B) along the direction from the first metal semiconductor alloy portion 66 to the recessed metal semiconductor alloy portion 72. Electrons travel in the n-doped semiconductor region (48A, 48B) along the direction from the second metal semiconductor alloy portion 68 toward the recessed metal semiconductor alloy portion 72. Thus, the majority charge carriers travel toward the recessed metal semiconductor alloy portion 72 in the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B).

The mechanism of Peltier-Seebeck effect is also in operation in the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B). However, the majority charge carriers diffuse away from the interface with the first or second metal semiconductor alloy portion (66 or 68) toward the interface with the recessed metal semiconductor alloy portion 72 in each of the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B). Therefore, there is a net heat transfer from

the first and second metal semiconductor alloy portions (66, 68) to the recessed metal semiconductor alloy portion 72.

Since the entirety of the semiconductor waveguide 30, the recessed semiconductor regions (32, 46B, 48B), the p-doped semiconductor region (46A, 46B), and the n-doped semiconductor region (48A, 48B) is thermally connected among one another, heat transferred into the recessed metal semiconductor alloy portion 72 is transferred into the semiconductor waveguide 30. Thus, the semiconductor waveguide is heated as the current flows through the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B). The mechanism for the heat accumulation in the semiconductor waveguide 30 is not Joule heating, but a heat transfer through Peltier-Seebeck effect.

Heating of the semiconductor waveguide 30 affects the refractive index of the semiconductor material of the semiconductor waveguide in the same manner as the cooling of the semiconductor waveguide 30 except for the reversal of the polarity of the change in the refractive index. In a similar manner as in the previous embodiment, temperature change in the semiconductor waveguide 30 may be advantageously employed to change the phase of light passing through the semiconductor waveguide. By modulating the refractive index of a semiconductor waveguide 30 through the temperature change in the semiconductor waveguide 30 caused by heat transfer into the semiconductor waveguide 30, the phase of the light passing through the semiconductor waveguide 30 may be modulated.

Referring to FIG. 10, a second exemplary semiconductor structure according to a second embodiment of the present invention comprises a semiconductor substrate 108, which is a semiconductor-on-insulator (SOI) substrate. The SOI substrate includes a handle substrate 10, an insulator layer 20 abutting a top surface of the handle substrate 10, and a top semiconductor layer 129 located above the insulator layer 20. The insulator layer 20 and the handle substrate 10 provide structural support to the top semiconductor layer 129 which may comprise a contiguous semiconductor material layer that covers the entirety of the insulator layer 20. The top semiconductor layer 129 comprises a semiconductor material, which may be any of the material that may be employed for the contiguous semiconductor material layer of the first embodiment.

Preferably, the top semiconductor layer 129 comprises a substantially undoped semiconductor material so that the amount of impurities, including dopant atoms, in the top semiconductor layer 129 is minimized. By minimizing the amount of impurities in the contiguous material layer, a semiconductor waveguide having a low absorption rate of the signal may be subsequently formed from a portion of the top semiconductor layer. The atomic concentration of impurities, including dopants, in the top semiconductor layer 129 is less than about $1.0 \times 10^{16}/cm^3$, and preferably less than about $1.0 \times 10^{15}/cm^3$, and more preferably less than about $1.0 \times 10^{14}/cm^3$. In case the top semiconductor layer 129 comprises silicon, the resistivity of the material of the top semiconductor layer 129 is greater than about 1 Ohm-cm, and preferably greater than about 10 Ohm-cm, and more preferably greater than about 100 Ohm-cm.

The buried insulator layer 20 comprises a dielectric material such as a dielectric oxide, a dielectric nitride, or a dielectric oxynitride. For example, the buried insulator layer 20 may comprise silicon oxide. The buried insulator layer 20 may comprise a dielectric material having a dielectric constant greater than 3.0.

The handle substrate 10 may comprise a semiconductor material, an insulator material, a conductive material, or a combination thereof. In case the handle substrate 10 comprises a semiconductor material, the material for the handle substrate 10 may comprise any of the semiconductor material that may be employed for the top semiconductor layer 129 as described above.

Referring to FIG. 11, a hard mask layer 125 may be deposited on a top surface of the top semiconductor layer 129 and lithographically patterned to mask a portion of the top semiconductor layer 129, while exposing other portions of the top semiconductor layer 129. The hard mask layer 125 comprises a dielectric material such as silicon oxide, silicon nitride, or silicon oxynitride. The exposed portions of the top semiconductor layer 129 are recessed. An epitaxial semiconductor layer 127 may be deposited on the recessed surface of the top semiconductor layer 129. The epitaxial semiconductor layer may comprise a different semiconductor material than the top semiconductor layer 129. The material of the epitaxial

semiconductor layer 127 is single crystalline, and is epitaxially aligned to semiconductor material of the top semiconductor layer 127. For example, the top semiconductor layer 129 may comprise single crystalline silicon, and the epitaxial semiconductor layer 127 may comprise a silicon germanium alloy.

The hard mask layer 125 is subsequently removed. The top surface of the top semiconductor portions of the top semiconductor layer 129 may be planarized, for example, by chemical mechanical planarization.

Referring to FIGS. 12A and 12B, portions of the top semiconductor layer 129 are appropriately doped and patterned to form at least one p-doped semiconductor portion (131, 132) and at least one n-doped semiconductor portion (133, 134). Each of the at least one p-doped semiconductor region (131, 132) may comprise a lower p-doped semiconductor region 131 and an upper p-doped semiconductor region 132. Each of the at least one n-doped semiconductor region (133, 134) may comprise a lower n-doped semiconductor region 133 and an upper n-doped semiconductor region 134. In addition, a semiconductor waveguide 136 may be formed by a patterning another portion of the top semiconductor layer 129 without implanting additional dopant atoms. In this case, the semiconductor waveguide may comprise a substantially intrinsic semiconductor material having the same composition as the at least one p-doped semiconductor portion (131, 132) and the at least one n-doped semiconductor portion (133, 134) except for dopant species and dopant concentration. The substantially intrinsic semiconductor material may have a resistivity greater than 1 Ohm-cm as the material of the top semiconductor layer 129 described above. In one case, the semiconductor waveguide 136 may consist essentially of silicon, and the at least one lower p-doped semiconductor region 131 may consist essentially of p-doped silicon, and the at least one n-doped semiconductor region 133 may consist essentially of n-doped silicon.

The at least one upper p-doped semiconductor portion 132 may be formed by implanting p-type dopants into at least one portion of the epitaxial semiconductor layer 127 through at least one opening in a first implantation mask layer (not shown), which may be a first patterned photoresist layer. The at least one lower p-doped semiconductor portion 131 may

be formed by implanting p-type dopants into at least one portion of the top semiconductor layer 129 through the at least one opening in the first implantation mask layer. The at least one upper n-doped semiconductor portion 134 may be formed by implanting n-type dopants into at least one portion of the epitaxial semiconductor layer 127 through at least one opening in a second implantation mask layer (not shown), which may be a second patterned photoresist layer. The at least one lower n-doped semiconductor portion 133 may be formed by implanting n-type dopants into at least one portion of the top semiconductor layer 129 through the at least one opening in the second implantation mask layer.

After implantation of the p-type dopants and the n-type dopants, the top semiconductor layer 129 is lithographically patterned. The remaining portions of the epitaxial semiconductor layer 127 and the top semiconductor layer 129 after lithographic patterning include the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and optionally, the semiconductor waveguide 136. Thus, the heights of the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and the semiconductor waveguide 136 are substantially the same at this step.

Each of the at least one p-doped semiconductor portion (131, 132) may laterally abut the at least one n-doped semiconductor portion (133, 134). Alternately, a substantially undoped semiconductor material portion (not shown) having the same composition as the semiconductor waveguide 136 may be formed between one of the at least one p-doped semiconductor portion (131, 132) and the at least one n-doped semiconductor portion (133, 134).

Referring to FIGS. 13A and 13B, metal semiconductor alloy regions are formed on the sub-portions of the at least one upper p-doped semiconductor portion 132 and the at least one upper n-doped semiconductor portion 134. Specifically, a first metal semiconductor alloy region 140 is formed on each laterally abutting pair of a first sub-portion of the at least one p-doped semiconductor portion (131, 132) and a first sub-portion of the at least one n-doped semiconductor portion (133, 134). Each first metal semiconductor alloy region 140 is contiguous.

A second metal semiconductor alloy region 142 is formed on a second sub-portion of each of the at least one upper p-doped semiconductor portion 132. The second sub-portion of each of the at least one upper p-doped semiconductor portion 132 is located on an opposite end of the first sub-portion of that p-doped semiconductor portion 134. In each of the at least one p-doped semiconductor portion (131, 132), a middle sub-portion of the p-doped semiconductor portion (131, 132) that does not underlie a metal semiconductor alloy region separates, and laterally abuts, a first sub-portion of the p-doped semiconductor portion (131, 132) and a second sub-portion of the p-doped semiconductor portion (131, 132). Each of the at least one p-doped semiconductor portion (131, 132) includes a first sub-portion located directly underneath a portion of a first metal semiconductor alloy region 140, a second sub-portion located directly underneath a second metal semiconductor alloy region 142, and a middle sub-portion that laterally separates the first sub-portion and the second sub-portion of that p-doped semiconductor portion (131, 132).

A third metal semiconductor alloy region 144 is formed on a second sub-portion of each of the at least one upper n-doped semiconductor portion 134. The second sub-portion of each of the at least one upper n-doped semiconductor portion 134 is located on an opposite end of the first sub-portion of that n-doped semiconductor portion (133, 134). In each of the at least one n-doped semiconductor portion (133, 134), a middle sub-portion of the n-doped semiconductor portion (133, 134) that does not underlie a metal semiconductor alloy region separates, and laterally abuts, a first sub-portion of the n-doped semiconductor portion (133, 134) and a second sub-portion of the n-doped semiconductor portion (133, 134). Each of the at least one n-doped semiconductor portion (133, 134) includes a first sub-portion located directly underneath a portion of a first metal semiconductor alloy region 140, a second sub-portion located directly underneath a third metal semiconductor alloy region 144, and a middle sub-portion that laterally separates the first sub-portion and the second sub-portion of that p-doped semiconductor portion (131, 132).

The metal semiconductor alloy regions (140, 142, 144) may be formed by depositing an insulator layer (not shown), patterning openings in the insulator layer in areas in which the metal semiconductor alloy regions (140, 142, 144) are to be formed, depositing a metal

layer, reacting the material of the metal layer with the underlying semiconductor material, and removing unreacted portions of the metal layer. The insulator layer may, or may not, be subsequently removed. The metal layer comprises a metal that reacts with the underlying semiconductor material of the at least one p-doped semiconductor portion (131, 132) and the at least one n-doped semiconductor portion (133, 134). Non-limiting examples of the metal that may be employed as the material of the metal layer include Co, Ta, Ti, W, Ni, Pt, Os, and Ir. In case the underlying semiconductor material comprises silicon, the metal semiconductor alloy regions (140, 142, 144) may comprise a metal silicide. The thickness of the metal semiconductor alloy regions (140, 142, 144) may be from 10 nm to 100 nm, although lesser and greater thicknesses can also be employed.

Referring to FIGS. 14A and 14B, a photoresist 147 is applied over the top surface of the second exemplary semiconductor structure. An opening is formed in the photoresist 147 by lithographic patterning. The at least one first metal semiconductor alloy region 140 is exposed within the opening in the photoresist 147. A portion of the semiconductor waveguide 136 may be exposed within the opening in the photoresist 147. Not necessarily but preferably, edges of the photoresist 147 may overlie the middle sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) and the middle sub-portion(s) of the at least one n-doped semiconductor portion (133, 134).

Portions of the top surface of the buried insulator layer 20 are exposed within the opening in the photoresist 147. The exposed portions of the buried insulator layer 20 are removed from underneath the opening in the photoresist 147 by an etch, which may be an isotropic etch or an anisotropic etch. The photoresist 147 protects covered portions of the buried insulator layer 20 from the etch. The etch is selective to the metal semiconductor alloy portions (140, 142, 144), the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and the semiconductor waveguide 136. A trench is formed within the buried insulator layer 20 underneath the opening in the photoresist 147. A top surface of the handle substrate 10 may be exposed underneath the trench in the buried insulator layer 20.

The trench may undercut the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and a portion of the semiconductor waveguide 136. Preferably, the undercut of the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and a portion of the semiconductor waveguide 136 is controlled to prevent a complete dissociation from the top surface of the buried insulator layer 20 and to insure that each of the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and a portion of the semiconductor waveguide 136 remains attached to the buried insulator layer 20. Preferably, the edge of the trench in the buried insulator layer 20 is directly adjoined to the middle sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) and the middle sub-portion(s) of the at least one n-doped semiconductor portion (133, 134). Each of the first sub-portion of the at least one p-doped semiconductor portion (131, 132) and each of the first sub-portion of the at least one n-doped semiconductor portion (133, 134) may laterally protrude from the edges of the trench within the buried insulator layer 20, and overhang above the trench in the buried insulator layer 20. The remaining portions of the buried insulator layer 20 constitute at least one dielectric material portion that vertically abuts the bottom surfaces of the second sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) and the second sub-portion(s) of the at leas one n-doped semiconductor portion (133, 134).

Referring to FIGS. 15A and 15B, the trench in the buried insulator layer 20 is filled with a dielectric material. Preferably, the dielectric material filling the trench in the buried insulator layer 20 comprises a different material than the dielectric material of the buried insulator layer 20. Preferably, the dielectric material filling the trench comprises a low dielectric constant (low-k) material having a dielectric constant less than 3.0. In this case, the dielectric material filling the trench constitutes a low dielectric constant (low-k) dielectric material portion 150. The low-k dielectric material portion 150 laterally abuts the buried insulator layer 20 and vertically abuts the bottom surfaces of the first sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) and the first sub-portion(s) of the at leas one n-doped semiconductor portion (133, 134). The interface between the buried insulator layer 20 and the low-k dielectric material portion 150 may be located underneath

the middle sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) and the middle sub-portion(s) of the at least one n-doped semiconductor portion (133, 134).

The dielectric material portion of the buried insulator layer 20 comprises a dielectric material having a second edge underlying the middle sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) located between one of the at least one first metal semiconductor region 140 and one of the at least one second metal semiconductor region 142 and having a third edge underlying a middle sub-portion(s) of the at least one n-doped semiconductor portion (133, 134) located between one of the at least one first metal semiconductor region 140 and the at least one third metal semiconductor region 144. Further, the low-k dielectric material portion 150 comprises a dielectric material having a second edge underlying the middle sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) located between one of the at least one first metal semiconductor region 140 and one of the at least one second metal semiconductor region 142 and having a third edge underlying a middle sub-portion(s) of the at least one n-doped semiconductor portion (133, 134) located between one of the at least one first metal semiconductor region 140 and the at least one third metal semiconductor region 144.

Exemplary low-k dielectric materials that may be employed for the low-k dielectric material portion 150 include, but are not limited to, fluorinated or non-fluorinated organic polymer based low k materials such as Dow Chemical's SiLK™ dielectric, Honeywell's Flare™, polyimides, benzocyclobutene, polybenzoxazoles, aromatic thermoset polymers based on polyphenylene ethers, chemical vapor deposited polymers such as poly(p-xylylene), and organosilicate glasses (OSG's) that may be deposited by chemical vapor deposition. Organosilicate glasses contain a matrix of a hydrogenated oxidized silicon carbon material (SiCOH) comprising atoms of Si, C, O and H in a covalently bonded tri-dimensional network, and may be referred to as SiCOH dielectric materials. The low-k dielectric materials may be porous or non-porous. Typically, the low-k dielectric material of the low-k dielectric material portion 150 has less thermal conductivity than the dielectric material of the buried insulator layer 20. The low-k dielectric material portion 150 as deposited may cover the entirety of the second exemplary semiconductor structure. Preferably, the top surface of the low-k dielectric material portion 150 is planar, which may be effected by

depositing a self-planarizing low-k dielectric material or by planarizing a non-self-planarizing low-k dielectric material layer by chemical mechanical planarization, a recess etch, or a combination thereof.

An optoelectronic device 160 is formed on the top surface of the low-k dielectric material portion 150. The optoelectronic device may be any device that manipulates an optical signal, i.e., electromagnetic radiation. The optical signal may be in the ultraviolet range, in the visible spectrum, in the infrared range, or in a microwave range. The optoelectronic device 160 may include a plurality of devices that manipulate at least one optical signal and may, or may not, be interconnected amongst one another. The optoelectronic device 160 may, or may not, be optically coupled to the semiconductor waveguide 136. In case the optoelectronic device 160 is optically coupled to the semiconductor waveguide 136, the optoelectronic device 160 may manipulate the optical signal that are fed into, or received from, the semiconductor waveguide 136. The optoelectronic device 160 may include at least one of a laser, optical amplifier, an optical sensor, a waveguide, a quantum well, or any other device that may manipulate an optical signal. The optoelectronic device 160 may comprise any semiconductor material that may be employed for the top semiconductor layer 129 as described above. Particularly, the optoelectronic device 160 may comprise a III-V compound semiconductor material such as GaAs, $In_xGa_{1-x}As$, $Al_xIn_yGa_{1-x-y}As$, InP, $In_xGa_{1-x}As_yP_{1-y}$, etc. The range of x, y, and 1-x-y are between 0 and 1. The optoelectronic device 160 may comprise a doped semiconductor material or an undoped semiconductor material.

Optionally, the region of the low-k dielectric material portion 150 that is not covered by the optoelectronic device 160 may be etched by an etch that is selective to the optoelectronic device, the second and third metal semiconductor alloy regions (142, 144), the at least one p-doped semiconductor portion (131, 132), and the at least one n-doped semiconductor portion (133, 134).

Referring to FIGS. 16A and 16B, an interconnect-level dielectric material layer 80 is formed over the optoelectronic device 160 and the exposed portions of the buried insulator layer 20, the at least one second metal semiconductor alloy region 142, the at least one third metal semiconductor alloy region 144, the at least one p-doped semiconductor portion (131, 132), and the at least one n-doped semiconductor portion (133, 134). FIG. 16A is a vertical cross-

sectional view along the vertical plane Z – Z' in FIG. 16B, and FIG. 16B is a top-down view of selected elements including the at least one p-doped semiconductor portion (131, 132), the at least one first metal semiconductor alloy region 140, the at least one second metal semiconductor alloy region 142, the at least one third metal semiconductor alloy region 144, and the semiconductor waveguide 136. The location of the optoelectronic device 160 is shown in a broken line. The interconnect-level dielectric material layer 80 comprises a dielectric material, which may comprise any of the dielectric material that may be employed for the buried insulator layer or the low-k dielectric material portion 150. Additionally or alternately, the interconnect-level dielectric material layer 80 may comprise a doped silicate glass such as phosphosilicate glass (PSG), borosilicate glass (BSG), borophosphosilicate glass (BPSG), fluorosilicate glass (FSG), etc. The interconnect-level dielectric material layer 80 may further include other dielectric materials as well.

A first set of via holes may be formed in the interconnect-level dielectric material layer 80 above the optoelectronic device 160 and filled with a compound semiconductor material to form at least one compound semiconductor via 85. Each of the at least one compound semiconductor via vertically abuts the optoelectronic device 160 and provides conduction of electrical current or transmission of light to or from the optoelectronic device 160.

A second set of via holes is formed in the interconnect-level dielectric material layer 80 above each of the at least one second metal semiconductor alloy region 142 and the at least one third metal semiconductor alloy region 144. At least one first metal contact via 90 abutting each of the at least one second metal semiconductor alloy region 142 and at least one second metal contact via 92 abutting each of the at least one third metal semiconductor alloy region 144 are formed within the second set of via holes by filling the second set of via holes with a conductive metal and removing excess metal from above the top surface of the interconnect-level dielectric material layer 80. The at least one first metal contact via 90 and the at least one second metal contact via 92 comprises a metallic material such as W, Ta, Ti, WN, TaN, TiN, Cu, and Al. Other metallic materials may also be employed instead of, or in addition to, the metallic material described above.

Each adjoined set of a first metal contact via 90, a second metal semiconductor alloy region 142, a p-doped semiconductor portion (131, 132), a first metal semiconductor alloy region 140, an n-doped semiconductor portion (133, 134), a third metal semiconductor alloy region 144, and a second metal contact via 92 constitutes a temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92). Each temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) is configured to provide a path for conduction of electrical current.

The path for conduction of electrical current may be from a second metal contact via 92, then through a third metal semiconductor alloy region 144, then through an n-doped semiconductor portion (133, 134), then through a first metal semiconductor alloy region 140, then through a p-doped semiconductor portion (131, 132), then through a second metal semiconductor alloy region 142, and then to a first metal contact via 90. This direction of current flow is herein referred to as a forward current direction. Alternately, the path for conduction of electrical current may be from a first metal contact via 90, then through a second metal semiconductor alloy region 142, then through a p-doped semiconductor portion (131, 132), then through a first metal semiconductor alloy region 140, then through an n-doped semiconductor portion (133, 134), then through a third metal semiconductor alloy region 144, and then to a second metal contact via 92. This direction of current flow is herein referred to as a reverse current direction.

Each temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) is thermally coupled to the optoelectronic device 160, which comprises a semiconductor material and is configured to manipulate electromagnetic radiation, i.e., an optical signal.

As electrical current flows through each of the at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92), heat is transferred in the direction of the flow of the majority charge carrier. This is because the mechanism of Peltier-Seebeck effect is in operation in the at least one p-doped semiconductor portion (131, 132) and the at least one n-doped semiconductor portion (133, 134). According to Peltier-Seebeck effect, heat transfer accompanies diffusion of charge carriers in a semiconductor material and vice versa.

If the electrical current flows in the forward current direction, the majority charge carriers diffuse away from the interface with one of the at least one first metal semiconductor alloy region 140 and toward the interface with one of the at least one second metal semiconductor alloy region 142 and the at least one third metal semiconductor alloy region 144 within the p-doped semiconductor portion (131, 132) and the n-doped semiconductor region 134 of each temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92). The majority charge carriers are holes in the at least one p-doped semiconductor portion (131, 132), and are electrons in the at least one n-doped semiconductor region 134. The heat is further transferred to the at least one first metal contact via 90 and the at least one second metal contact via 92. Because of the thermal coupling between the at least one first metal semiconductor alloy region 140 and the optoelectronic device 160, the heat is also transferred from the optoelectronic device 160 to the at least one first metal semiconductor alloy region 140 as the at least one first metal semiconductor alloy region 140 is cooled. Therefore, there is a net heat transfer from the optoelectronic device 160 to the at least one first metal contact via 90 and the at least one second metal contact via 92. The heat that is transferred to the at least one first metal contact via 90 and the at least one second metal contact via 92 may further be transferred to a heat sink (not shown) through metallic interconnect structures embedded in the interconnect-level dielectric material layer 80.

If the electrical current flows in the reverse current direction, the majority charge carriers diffuse toward the interface with one of the at least one first metal semiconductor alloy region 140 and away from the interface with one of the at least one second metal semiconductor alloy region 142 and the at least one third metal semiconductor alloy region 144 within the p-doped semiconductor portion (131, 132) and the n-doped semiconductor region 134 of each temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92). The transferred heat accumulates at the at least one second metal semiconductor alloy region 142 and the at least one third metal semiconductor alloy region 144. Because of the thermal coupling between the at least one first metal semiconductor alloy region 140 and the optoelectronic device 160, the heat is further transferred from the at least one first metal semiconductor alloy region 140 to the optoelectronic device 160 as the at least one first metal semiconductor alloy region 140 is heated by heat transfer. Therefore, there is a net heat transfer from the at least one first metal contact via 90 and the at least one second metal

contact via 92 to the optoelectronic device 160. The heat may be transferred from a heat sink (not shown) to the at least one first metal contact via 90 and the at least one second metal contact via 92 through metallic interconnect structures embedded in the interconnect-level dielectric material layer 80, then subsequently transferred to the optoelectronic device 160.

Therefore, by reversing the direction of flow of the electrical current, the direction of heat transfer may be reversed. Further, by adjusting the magnitude of the electrical current, the amount of heat transfer may be regulated. Typically, the material of the low-k dielectric material portion 150 has a lower thermal conductivity than the material of the buried insulator layer 20, thereby increasing the thermal isolation of the at least one first metal semiconductor alloy portion 140 and the optoelectronic device 160 from the handle substrate 10.

The first semiconductor device may be operated with a feedback mechanism for performance of the optoelectronic device 160. For example, the performance of the optoelectronic device 160 may be monitored during operation. Based on the monitored performance level of the optoelectronic device, a direction of the electrical current or magnitude of the electrical current may be manipulated to heat or cool the optoelectronic device, thereby reducing deviation in the performance of the optoelectronic device 160 from a target performance level.

Referring to FIG. 17, a third exemplary semiconductor structure according to a third embodiment of the present invention is derived from the second exemplary semiconductor structure by forming a substantially intrinsic lower semiconductor portion 30 and a substantially intrinsic upper semiconductor portion 138 in each temperature control device. A vertically abutting pair of a substantially intrinsic lower semiconductor portion 30 and a substantially intrinsic upper semiconductor portion 138 is herein referred to as a substantially intrinsic semiconductor portion (30, 138). Thus, each of the at least one temperature control device may include the substantially intrinsic semiconductor portion 30.

The substantially intrinsic semiconductor portion (30, 138) is formed between a p-doped semiconductor portion (131, 132) and an n-doped semiconductor portion (133, 134) of the at

least one temperature control device (90, 142, 131, 132, 140, 30, 138, 133, 134, 144, 92). The substantially intrinsic semiconductor portion (30, 138) may have the same composition as the semiconductor waveguide 136. The substantially intrinsic semiconductor portion (30, 138) vertically abuts the first metal semiconductor alloy region 140 of the at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92). In one case, the p-doped semiconductor portion (131, 132) and the n-doped semiconductor portion (133, 134) may be not abut each other, and are laterally separated by the substantially intrinsic semiconductor portion (30, 138). In another case, the p-doped semiconductor portion (131, 132) and the n-doped semiconductor portion (133, 134) may abut each other and the substantially intrinsic semiconductor portion (30, 138).

A low-k dielectric material portion 150, an optoelectronic device 160, an interconnect-level dielectric material layer 80, at least one compound semiconductor via 85, at least one first metal contact via 90, and at least one second metal contact via 92 may be formed in the same manner as in the second embodiment. Within the collective volume of the at least one substantially intrinsic semiconductor portion (30, 138) and the at least one first metal semiconductor alloy region 140, the current flows primarily through the at least one first metal semiconductor alloy region 140. Therefore, the addition of the at least one substantially intrinsic semiconductor portion (30, 138) does not change the current path in a substantial manner relative to the current path in the second embodiment. The at least one temperature control device (90, 142, 131, 132, 140, 30, 138, 133, 134, 144, 92) may be operated in the same manner as in the second embodiment to control the temperature of the optoelectronic device 160 and to regulate the performance of the optoelectronic device 160.

Referring to FIG. 18, a fourth exemplary semiconductor structure according to a fourth embodiment of the present invention is shown. The fourth exemplary semiconductor structure is derived from the second exemplary semiconductor structure of FIGS. 13A and 4B by omitting the steps corresponding to FIGS. 14A and 5B in the processing sequence. Specifically, application of a photoresist 147, patterning of the photoresist 147, and transfer of the pattern in the photoresist 147 into an exposed portion of the buried insulator layer 20 are omitted in the third embodiment.

Instead of patterning the buried insulator layer 20, a lower portion of an interconnect-level dielectric material layer 80 is formed over the at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) and the semiconductor waveguide 136. The top surface of the lower portion of the interconnect-level dielectric material layer 80 is planarized by employing a self-planarizing material for the lower portion of the interconnect-level dielectric material layer 80 and/or by performing a planarization processing step such as chemical mechanical planarization or a recess etch. An optoelectronic device 160 is formed over the top surface of the lower portion of the interconnect-level dielectric material layer 80. The optoelectronic device 160 may be the same as in the second embodiment, and may overlie the at least one first metal semiconductor alloy region 140 and a portion of the semiconductor waveguide 136. An upper portion of the interconnect-level dielectric material layer 80 is formed over the optoelectronic device 160. The lower portion and the upper portion of the interconnect-level dielectric material layer 80 may comprise the same material as in the second embodiment. At least one compound semiconductor via 85, at least one first metal contact via 90, and at least one second metal contact via 92 may be formed in the same manner as in the second embodiment. The at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) may be operated in the same manner as in the second embodiment to control the temperature of the optoelectronic device 160 and to regulate the performance of the optoelectronic device 160.

Referring to FIG. 19, a fifth exemplary semiconductor structure according to a fifth embodiment of the present invention is derived from the second exemplary semiconductor structure by omitting formation of at least one compound semiconductor via 85.

Referring to FIG. 20, a sixth exemplary semiconductor structure according to a sixth embodiment of the present invention is derived from the second exemplary semiconductor structure at a step corresponding to FIGS. 14A and 5B by removing the photoresist 147 and employing a non-conformal deposition process to form a low-k dielectric material portion 150. The material of the low-k dielectric material portion 150 may be the same as in the second embodiment. The non-conformal property of the deposition process employed to form the low-k dielectric material portion 150 deposits a low-k dielectric material over

narrow portions of the of the semiconductor structures above the top surface of the buried insulator layer 20, i.e., between the at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) and the semiconductor waveguide 136. Thus a cavity 152 is formed within the low-k dielectric material portion 150.

Referring to FIG. 21, processing steps corresponding to FIGS. 15A – 7B of the second embodiment are performed on the sixth exemplary semiconductor structure. The cavity 152 may be under vacuum after processing, or may be filled with air or a gas. The cavity 152 has a dielectric constant that is substantially equal to 1.0. The cavity 152 has a lower thermal conductivity than the material of the buried insulator layer 20, thereby increasing the thermal isolation of the at least one first metal semiconductor alloy portion 140 and the optoelectronic device 160 from the handle substrate 10. The at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) may be operated in the same manner as in the second embodiment to control the temperature of the optoelectronic device 160 and to regulate the performance of the optoelectronic device 160.

Referring to FIG. 22, a seventh exemplary semiconductor structure according to a seventh embodiment of the present invention is shown. FIG. 111 is a top-down view of selected elements including p-doped semiconductor portions (131, 132), n-doped semiconductor portions (133, 134), first metal semiconductor alloy regions 140, second metal semiconductor alloy regions 142, third metal semiconductor alloy regions 144, first metal contact vias 90, second metal contact vias 92, and a semiconductor waveguide 136. The location of the optoelectronic device 160 is shown in a broken line. A vertical cross-sectional view along the plane Z – Z' is the same as FIG. 15A.

Each of the first metal semiconductor alloy regions 140 is located within a first annulus. Each of the p-doped semiconductor portions (131, 132) and n-doped semiconductor portions (133, 134) is located within a second annulus which encloses and abuts the first annulus. Each of the second metal semiconductor alloy regions 142 and the third metal semiconductor alloy regions 144 is located within a third annulus which encloses and abuts the second annulus. The p-doped semiconductor portions (131, 132), the n-doped semiconductor portions (133, 134), the first metal semiconductor alloy regions 140, the second metal

semiconductor alloy regions 142, and the third metal semiconductor alloy regions 144 constitute two temperature control devices (90, 142, 131, 132, 140, 133, 134, 144, 92) between which a semiconductor waveguide 136 is located. An optoelectronic device 160 overlies portions of the two temperature control devices (90, 142, 131, 132, 140, 133, 134, 144, 92) and the semiconductor waveguide 136 as in the second embodiment. The two temperature control devices (90, 142, 131, 132, 140, 133, 134, 144, 92) may be operated in the same manner as in the second embodiment to control the temperature of the optoelectronic device 160 and to regulate the performance of the optoelectronic device 160.

In general, topological variations may be performed to the at least one temperature control devices (90, 142, 131, 132, 140, 133, 134, 144, 92 and optionally 30 and 138) to any of the exemplary semiconductor structures described above. Further, additional temperature control devices having a similar structure may be added to any of the exemplary semiconductor structures described above.

While the invention has been described in terms of specific embodiments, it is evident in view of the foregoing description that numerous alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, the invention is intended to encompass all such alternatives, modifications and variations which fall within the scope and spirit of the invention and the following claims.

CLAIMS

1. A semiconductor structure comprising:

a semiconductor waveguide having a first thickness and located on a top surface of an insulator layer;

a recessed semiconductor region of integral construction with said semiconductor waveguide, having a second thickness that is less than said first thickness, located on said insulator layer, and including a substantially undoped recessed semiconductor region;

a p-doped semiconductor region laterally abutting said substantially undoped recessed semiconductor region;

an n-doped semiconductor region laterally abutting said substantially undoped recessed semiconductor region and not abutting said p-doped semiconductor region; and

a recessed metal semiconductor alloy portion abutting said recessed semiconductor region, said p-doped semiconductor region, and said n-doped semiconductor region.

2. The semiconductor structure of Claim 1, wherein said semiconductor waveguide, said recessed semiconductor portion, said p-doped semiconductor portion, and said n-doped semiconductor portion comprise a same semiconductor material.

3. The semiconductor structure of Claim 1 or Claim 2, wherein said semiconductor waveguide, said recessed semiconductor portion, said p-doped semiconductor portion, and said n-doped semiconductor portion are single crystalline and are epitaxially aligned among one another.

4. The semiconductor structure of any preceding Claims, wherein said semiconductor waveguide comprises substantially undoped silicon or substantially undoped germanium.

5. The semiconductor structure of any preceding Claims, wherein said recessed semiconductor region includes a p-doped recessed semiconductor region which is a portion of said p-doped semiconductor region and an n-doped recessed semiconductor region which is a portion of said n-doped semiconductor region.

6. The semiconductor structure of any preceding Claims, further comprising:

another recessed semiconductor region of integral construction with said semiconductor waveguide, having said second thickness, located on said insulator layer, and including another substantially undoped recessed semiconductor region;

another p-doped semiconductor region laterally abutting said other substantially undoped recessed semiconductor region;

another n-doped semiconductor region laterally abutting said other substantially undoped recessed semiconductor region and not abutting said other p-doped semiconductor region; and

another recessed metal semiconductor alloy portion abutting said other recessed semiconductor region, said other p-doped semiconductor region, and said other n-doped semiconductor region, wherein said other recessed semiconductor region, said other p-doped semiconductor region, said other n-doped semiconductor region, and said other recessed metal semiconductor alloy portion are located on an opposite side of said recessed semiconductor region, said p-doped semiconductor region, said n-doped semiconductor region, and said recessed metal semiconductor alloy portion about said semiconductor waveguide.

7. A method of forming a semiconductor structure comprising:

forming shallow trench isolation structures laterally abutting a top semiconductor portion and vertically abutting a buried insulator layer in a top semiconductor layer of a semiconductor-on-insulator (SOI) substrate;

forming a semiconductor waveguide by patterning said top semiconductor portion;

forming a p-doped semiconductor region in said top semiconductor portion;

forming an n-doped semiconductor region not abutting said p-doped semiconductor region in said top semiconductor region; and

forming a recessed metal semiconductor alloy portion directly on a recessed region of said top semiconductor portion, wherein said recessed metal semiconductor alloy portion is formed directly on said p-doped semiconductor region and said n-doped semiconductor region.

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8. The method of Claim 7, further comprising forming a pair of recessed line trenches in said top semiconductor portion, wherein a remaining sub-portion of said top semiconductor portion having a first thickness and located between said pair of recessed line trenches constitutes said semiconductor waveguide, wherein sub-portions of said top semiconductor portion directly underneath said pair of line trenches constitute recessed semiconductor regions of integral construction with said semiconductor waveguide having a second thickness that is less than said first thickness, and wherein sidewalls of two sup-portions of said top semiconductor portion having said first thickness are exposed to said pair of recessed line trenches.

9. The method of Claim 8, further comprising:

implanting p-type dopants into an area including one of said two sup-portions of said top semiconductor portion and a portion of one of said recessed semiconductor regions to form said p-doped semiconductor region; and

implanting n-type dopants into an area including the other of said two sup-portions of said top semiconductor portion and another portion of said one of said recessed semiconductor regions to form said n-doped semiconductor region.

10. The method of Claim 9, further comprising:

forming a dielectric layer on said semiconductor waveguide, said recessed semiconductor regions, said p-doped semiconductor region, and said n-doped semiconductor region; and

lithographically patterning said dielectric layer to form a dielectric material portion abutting a top surface and sidewalls of said semiconductor waveguide and a dielectric spacer that abuts a sidewall of said p-doped semiconductor region and a sidewall of said n-doped semiconductor region.

11. A semiconductor structure comprising a temperature control device and an optoelectronic device,

wherein said temperature control device includes:

a first metal semiconductor alloy region located on a substrate;

a p-doped semiconductor portion abutting said first metal semiconductor alloy region and located on said substrate;

an n-doped semiconductor portion abutting said first metal semiconductor alloy region located on said substrate; wherein said temperature control device is configured to pass current from said p-doped semiconductor portion, through said first metal semiconductor alloy region, and to said n-doped semiconductor portion or from said n-doped semiconductor portion, through said first metal semiconductor alloy region, and to said p-doped semiconductor portion, and

wherein said optoelectronic device includes a device that comprises a semiconductor material, configured to manipulate electromagnetic radiation, and is thermally coupled to said temperature control device.

12. The semiconductor structure of Claim 11, wherein said optoelectronic device includes at least one of a laser, optical amplifier, an optical sensor, a waveguide, and a quantum well.

13. The semiconductor structure of Claim 11 or Claim 12, wherein said optoelectronic device includes a III-V compound semiconductor material.

14. The semiconductor structure of any of Claims 11 to 13, further comprising a dielectric material portion comprising a dielectric material and vertically abutting a bottom surface of said p-doped semiconductor portion and a bottom surface of said n-doped semiconductor portion.

15. The semiconductor structure of any of Claims 11 to 14, wherein said p-doped semiconductor portion laterally abuts said n-doped semiconductor portion.

16. The semiconductor structure of any of Claims 11 to 15, further comprising a substantially intrinsic semiconductor portion laterally abutting said p-doped semiconductor portion and said n-doped semiconductor portion and vertically abutting said first metal semiconductor alloy region, wherein said substantially intrinsic semiconductor portion has a resistivity greater than 1 Ohm-cm.

17. The semiconductor structure of any of Claims 11 to 16, wherein said temperature control device further comprises:

a second metal semiconductor alloy region vertically abutting said p-doped semiconductor portion;

a third metal semiconductor alloy region vertically abutting said n-doped semiconductor portion;

a first metal contact via abutting said second metal semiconductor alloy region; and

a second metal contact via abutting said third metal semiconductor alloy region.

18. A method of forming a semiconductor structure comprising a temperature control device and an optoelectronic device, said method including:

patterning a top semiconductor layer of a semiconductor-on-insulator substrate to form a p-doped semiconductor portion and an n-doped semiconductor portion;

forming a first metal semiconductor alloy region directly on said p-doped semiconductor portion and said n-doped semiconductor portion, wherein said p-doped semiconductor portion and an n-doped semiconductor portion and said first metal semiconductor alloy region constitute a portion of a temperature control device;

forming a current conduction path configured to pass current from said p-doped semiconductor portion, through said first metal semiconductor alloy region, and to said n-doped semiconductor portion or from said n-doped semiconductor portion, through said first metal semiconductor alloy region, and to said p-doped semiconductor portion; and

forming an optoelectronic device comprising a semiconductor material, configured to manipulate electromagnetic radiation, and is thermally coupled to said temperature control device.

19. The method of Claim 18, further comprising:

removing a portion of a buried insulator layer underneath a sub-portion of said p-doped semiconductor portion and a sub-portion of said n-doped semiconductor portion to form a trench in said buried insulator layer; and

filling said trench with a low dielectric constant (low-k) material having a dielectric constant less than 3.0, wherein said optoelectronic device is formed over said low-k material.

20. The method of Claim 18 or Claim 19, further comprising forming a cavity laterally abutting a remaining portion of said buried insulator layer by removing said low-k material selective to said remaining portion of said buried insulator layer.

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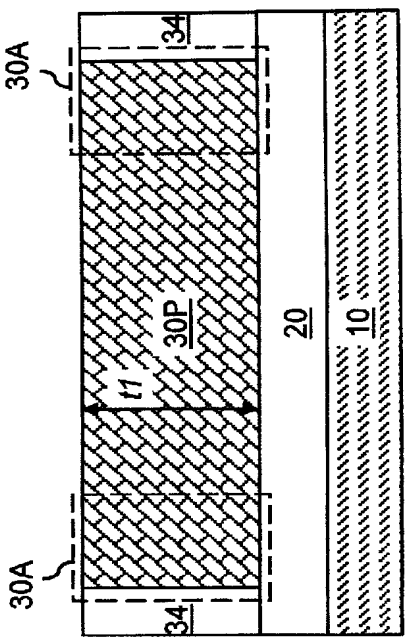

FIG. 1B

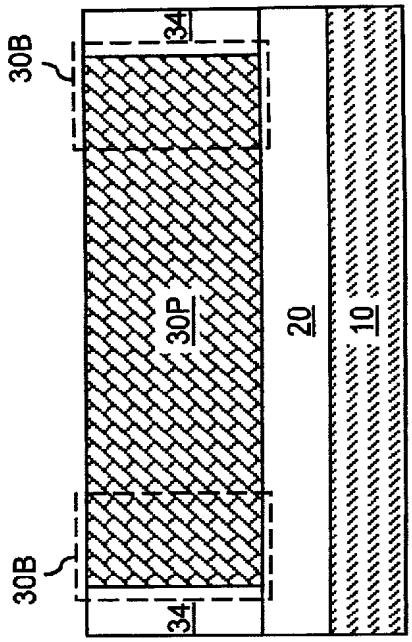

FIG. 1C

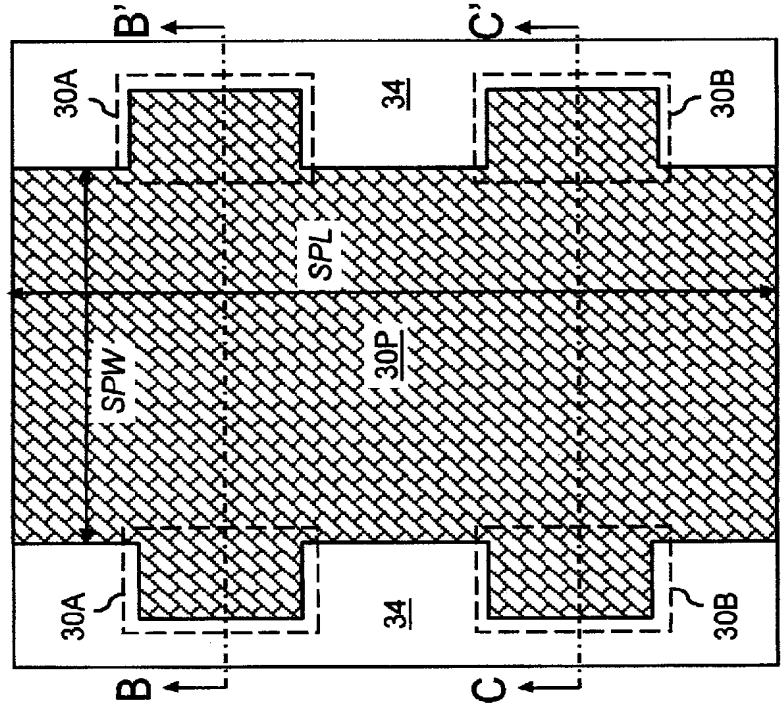

FIG. 1A

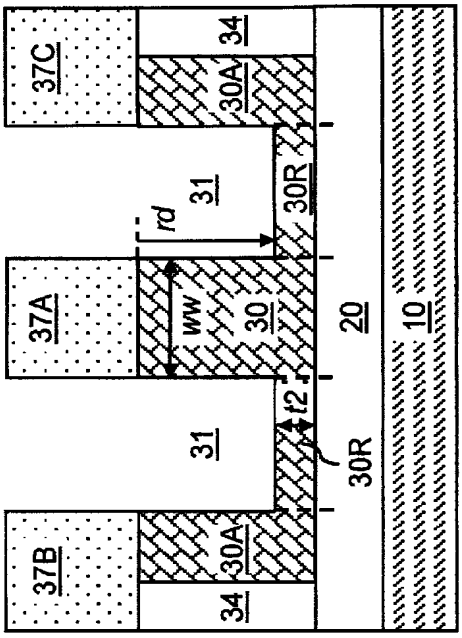

FIG. 2B

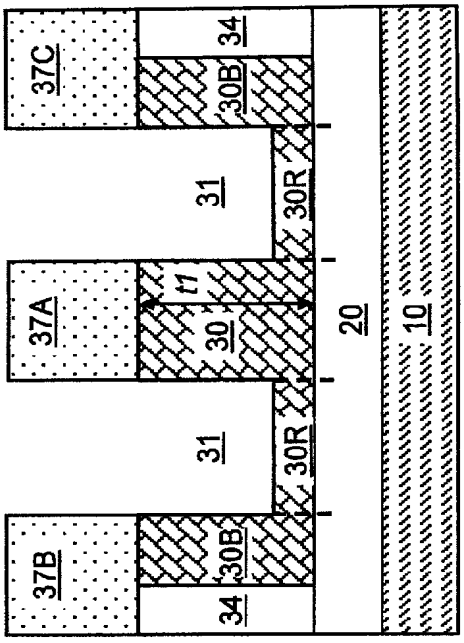

FIG. 2C

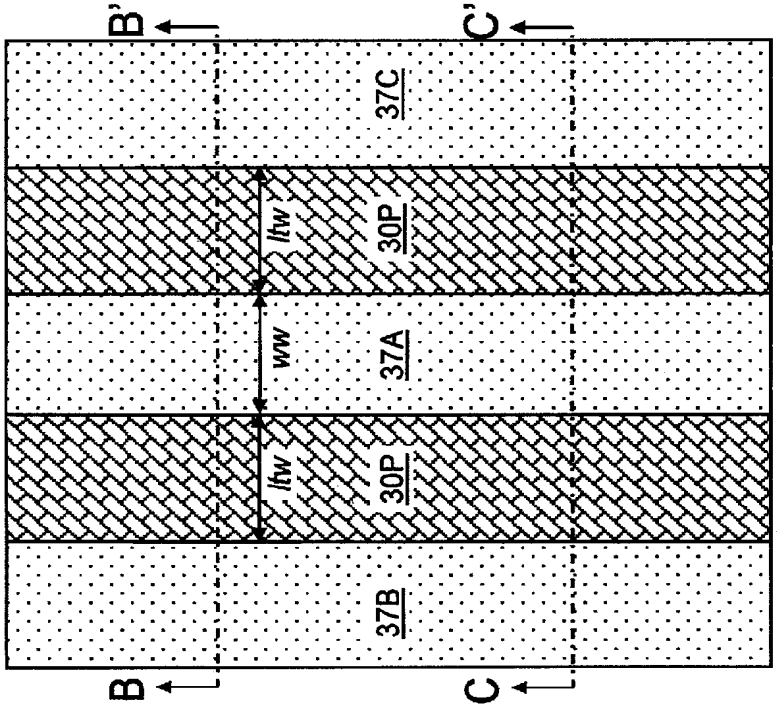

FIG. 2A

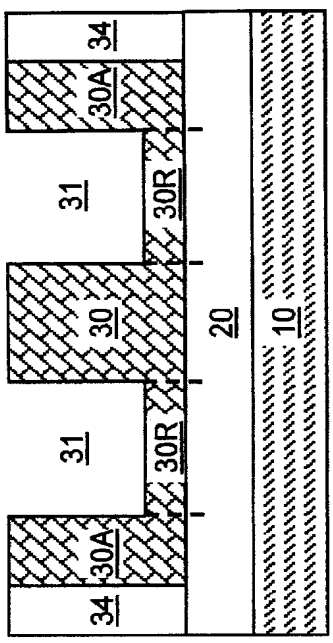

FIG. 3B

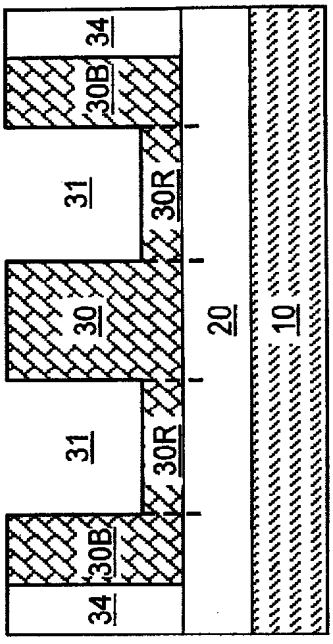

FIG. 3C

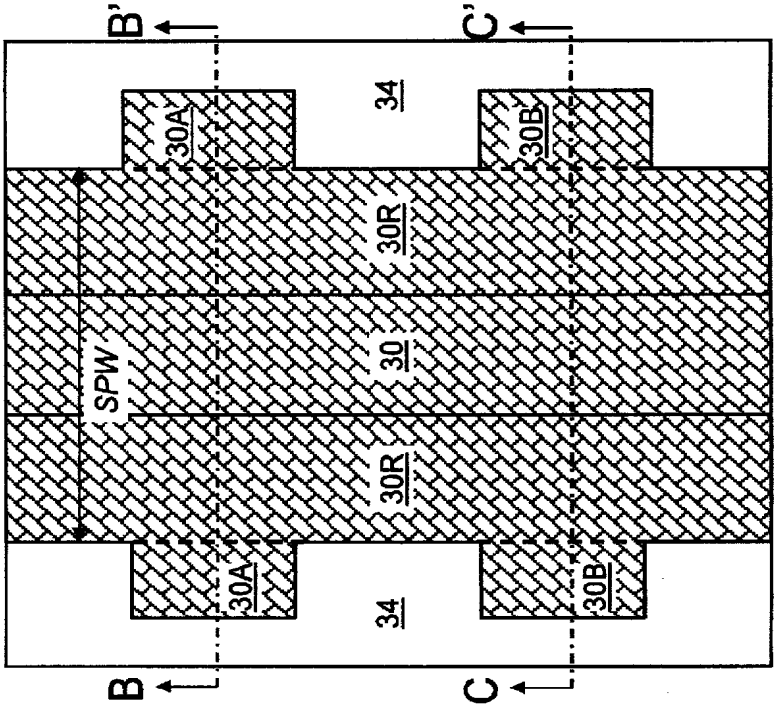

FIG. 3A

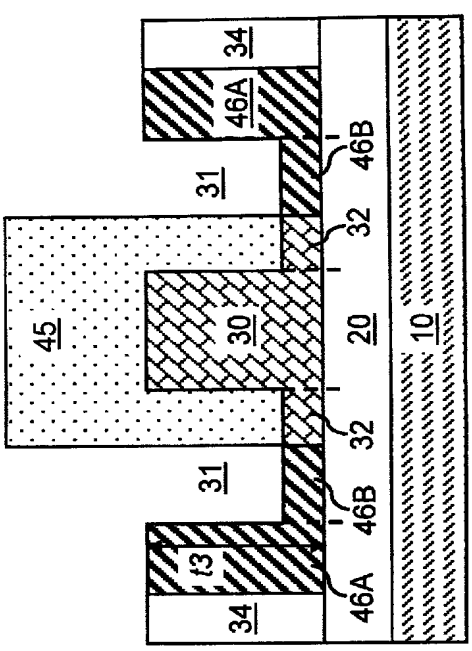

FIG. 4B

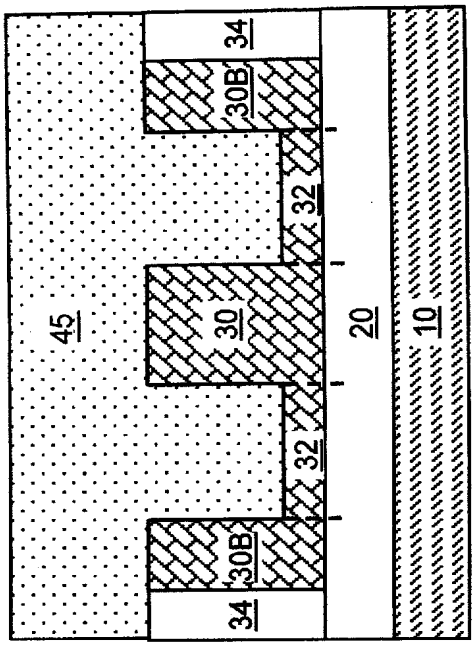

FIG. 4C

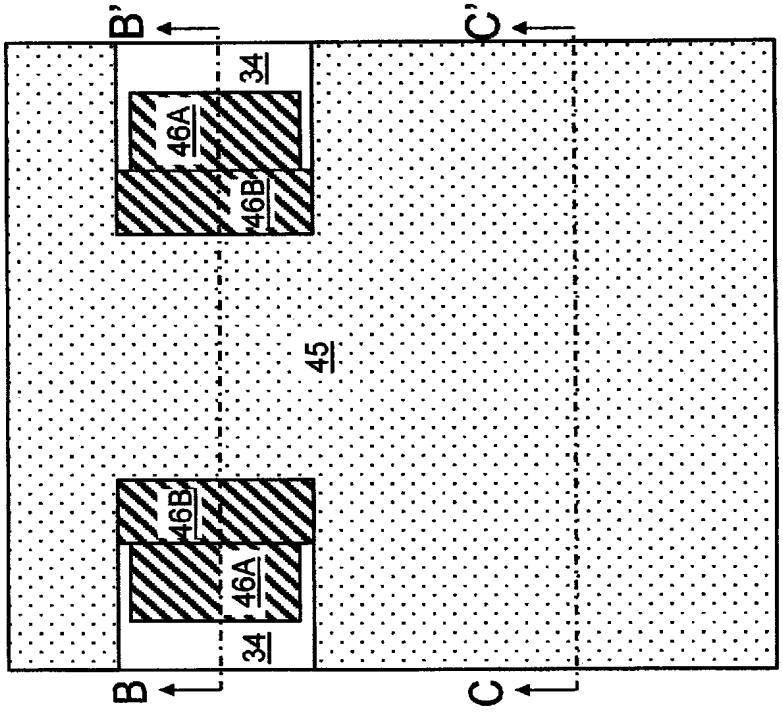

FIG. 4A

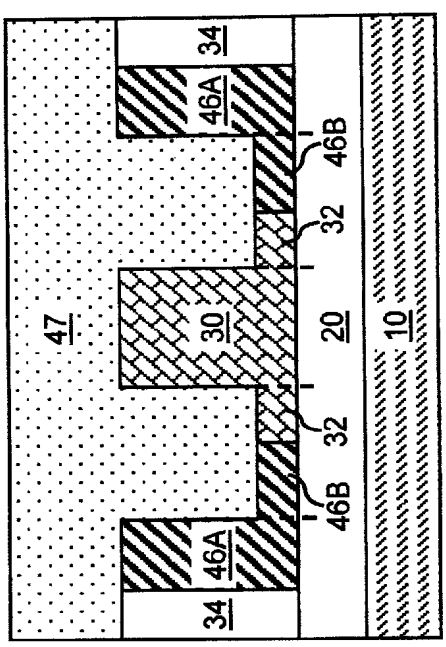

FIG. 5B

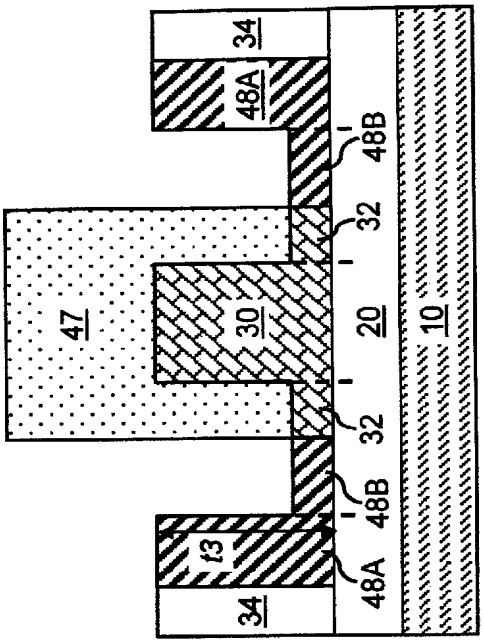

FIG. 5C

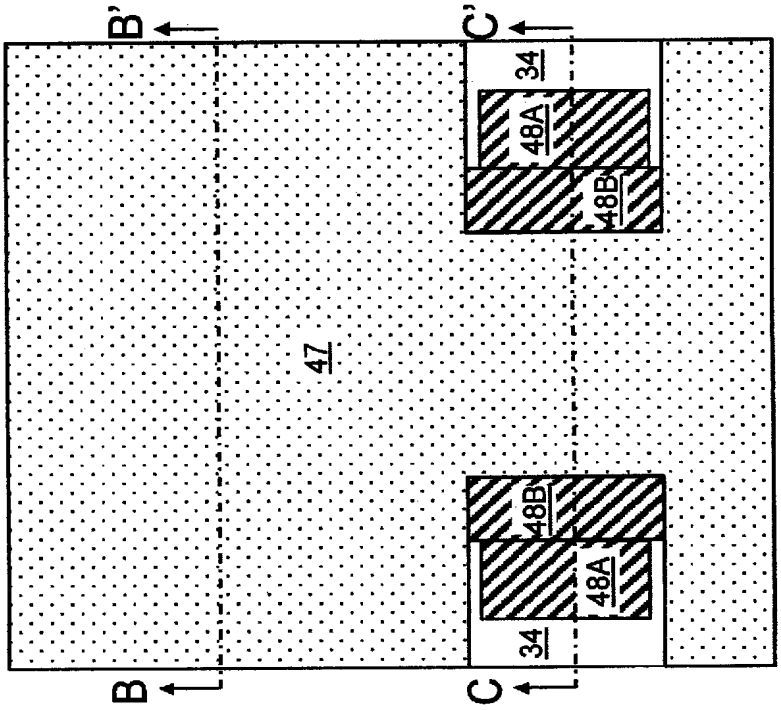

FIG. 5A

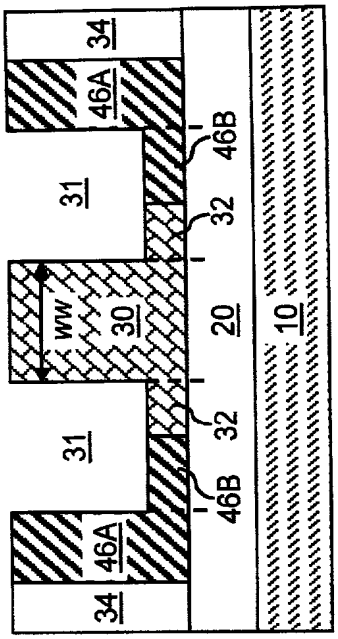

FIG. 6B

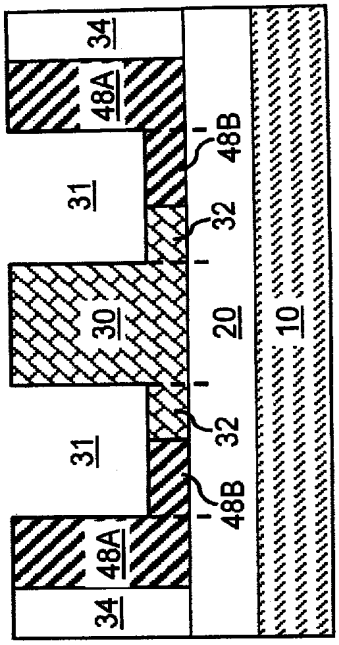

FIG. 6C

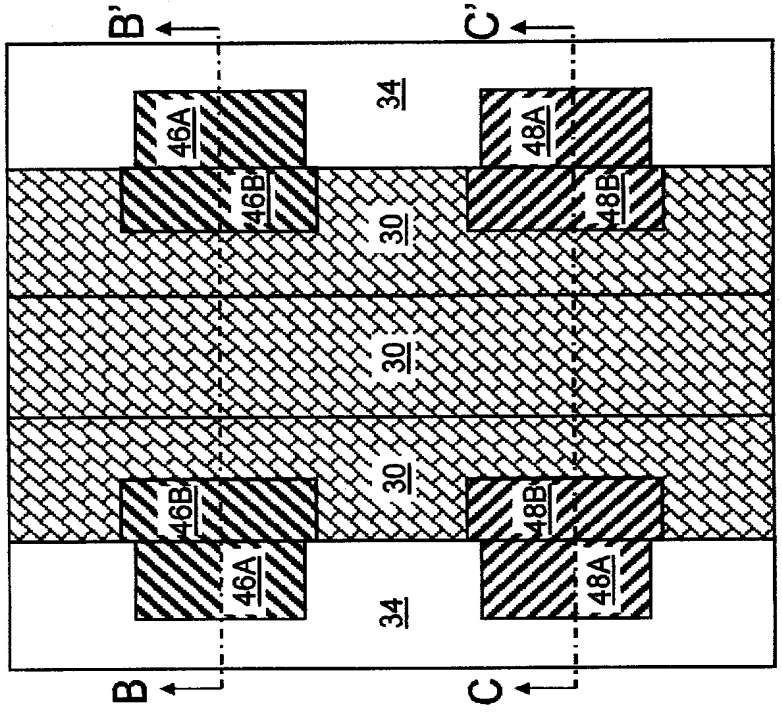

FIG. 6A

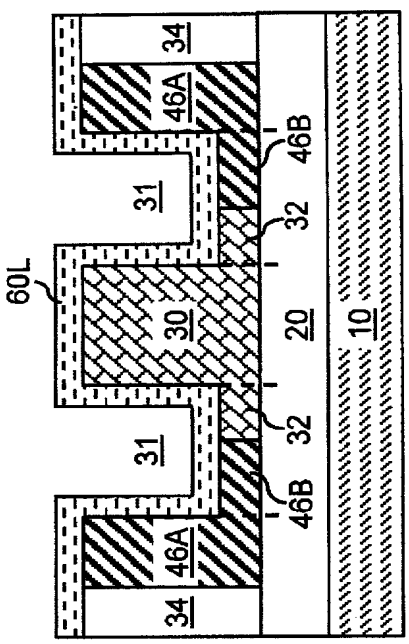

FIG. 7B

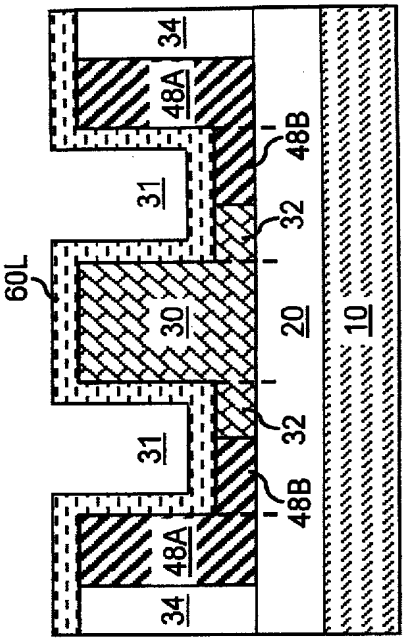

FIG. 7C

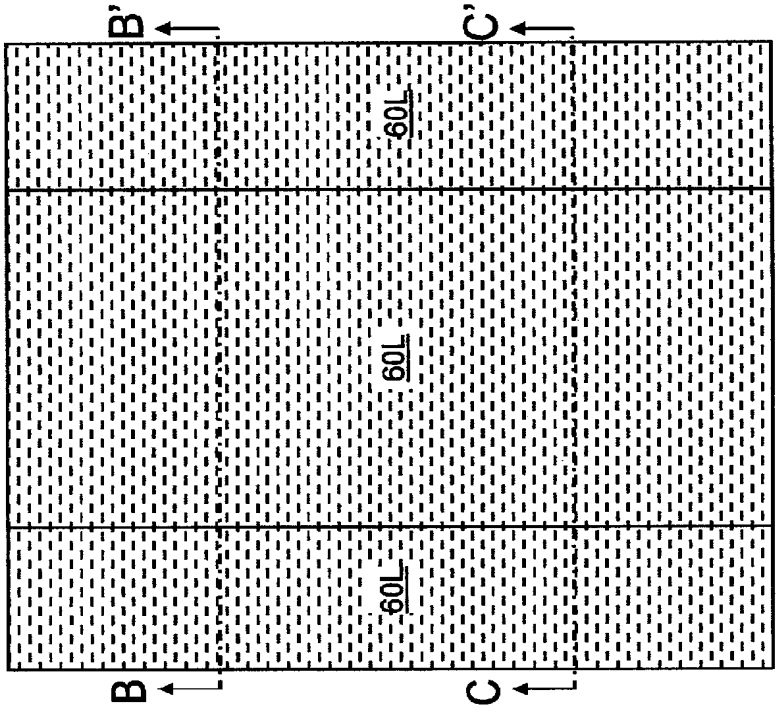

FIG. 7A

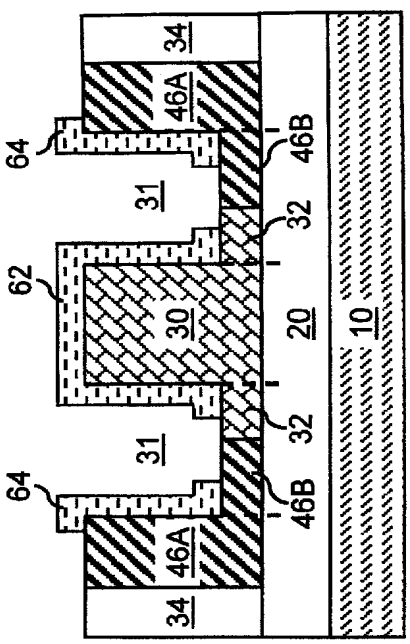

FIG. 8B

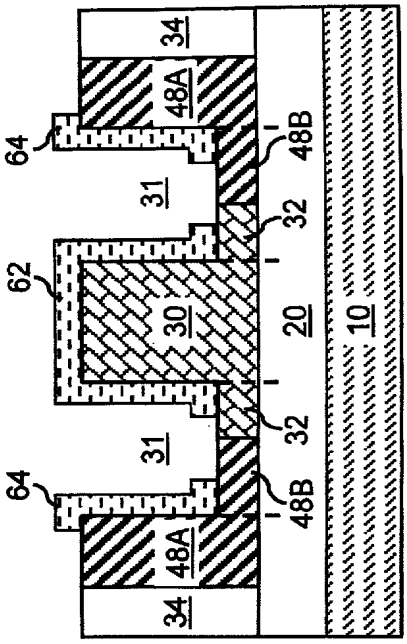

FIG. 8C

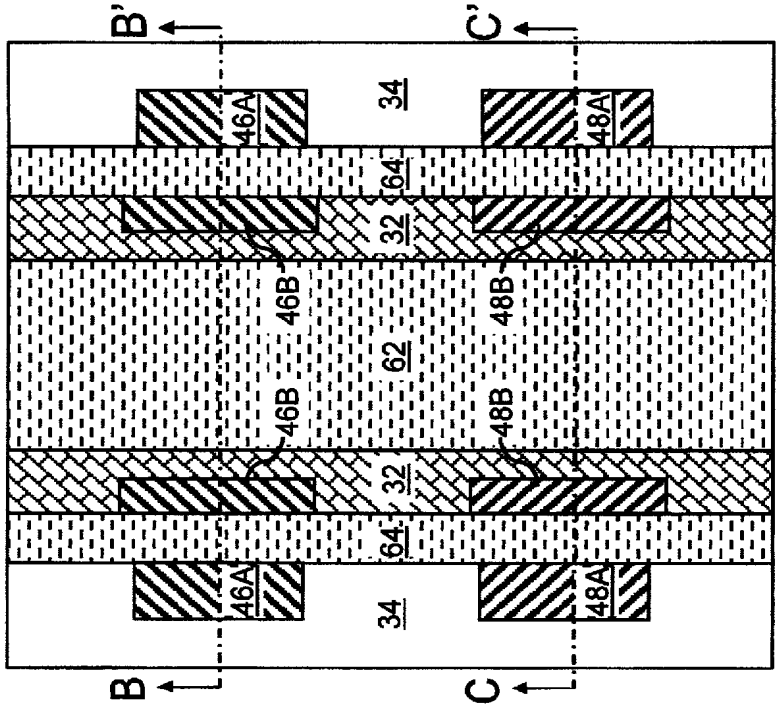

FIG. 8A

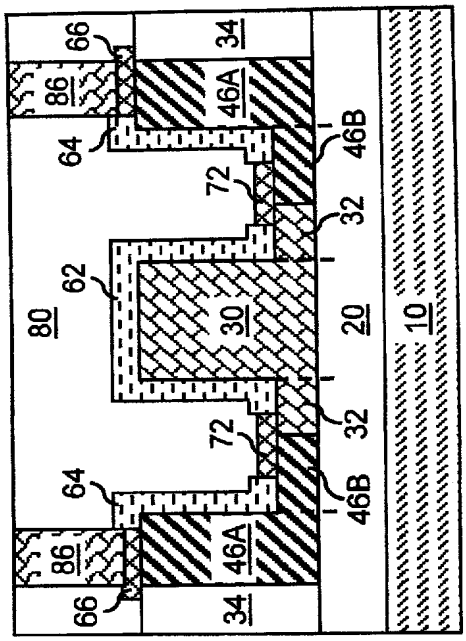

FIG. 9B

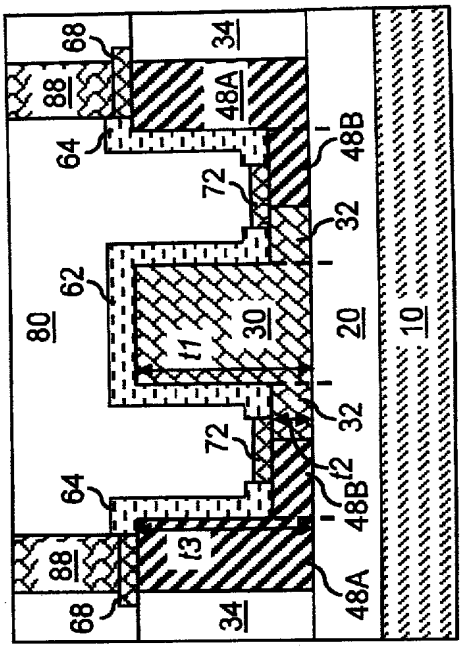

FIG. 9C

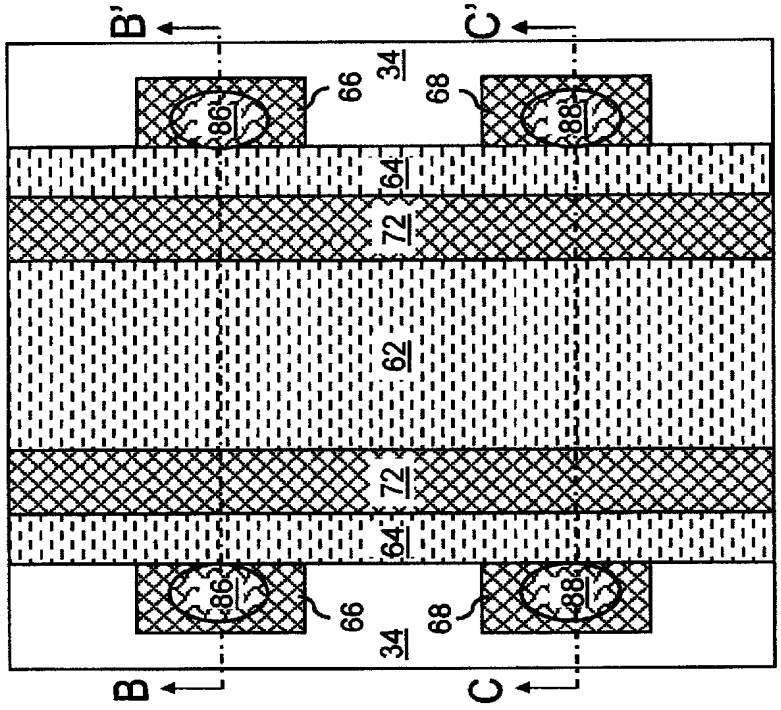

FIG. 9A

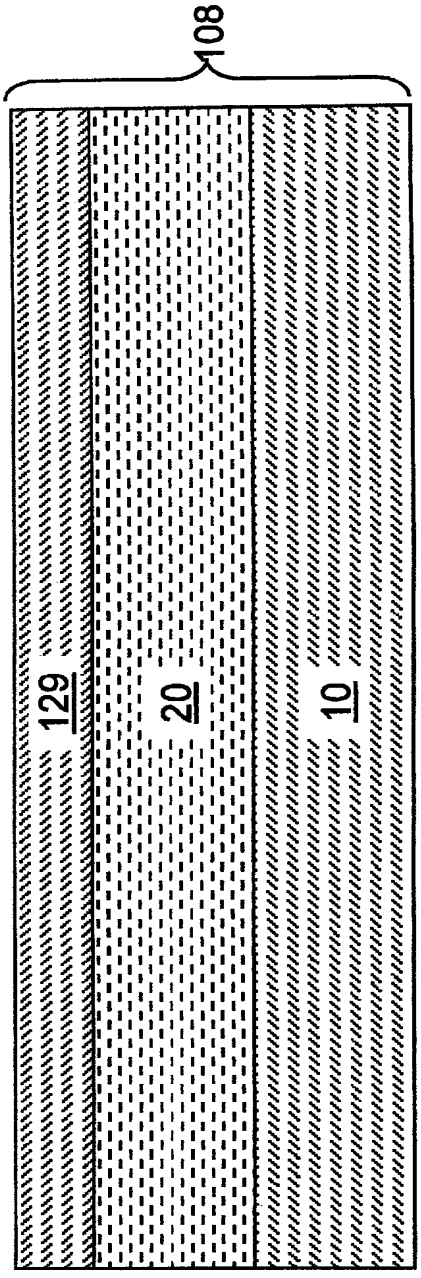

FIG. 10

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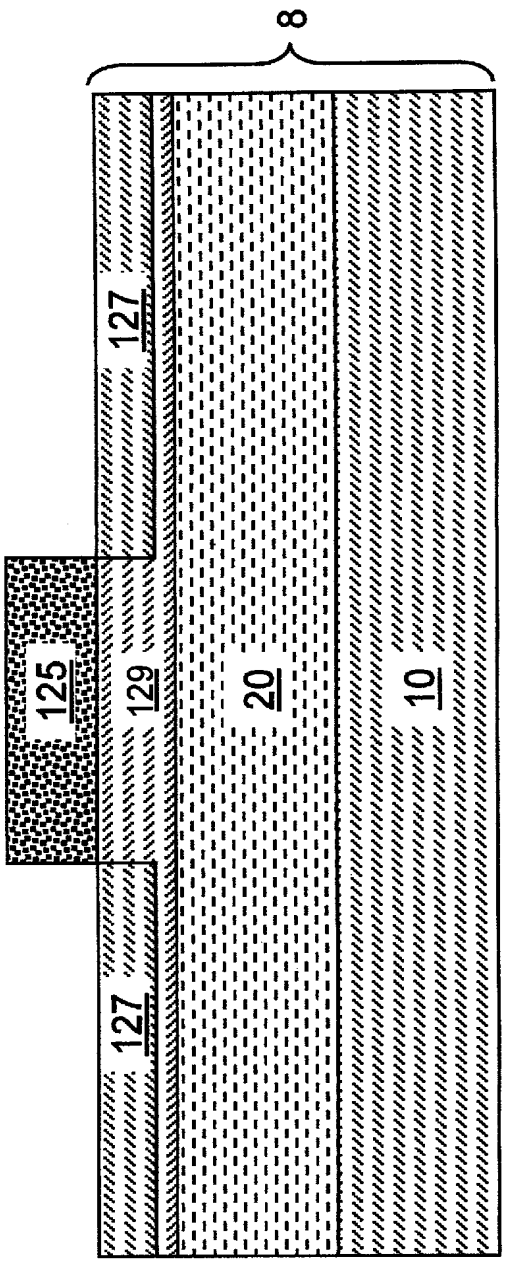

FIG. 11

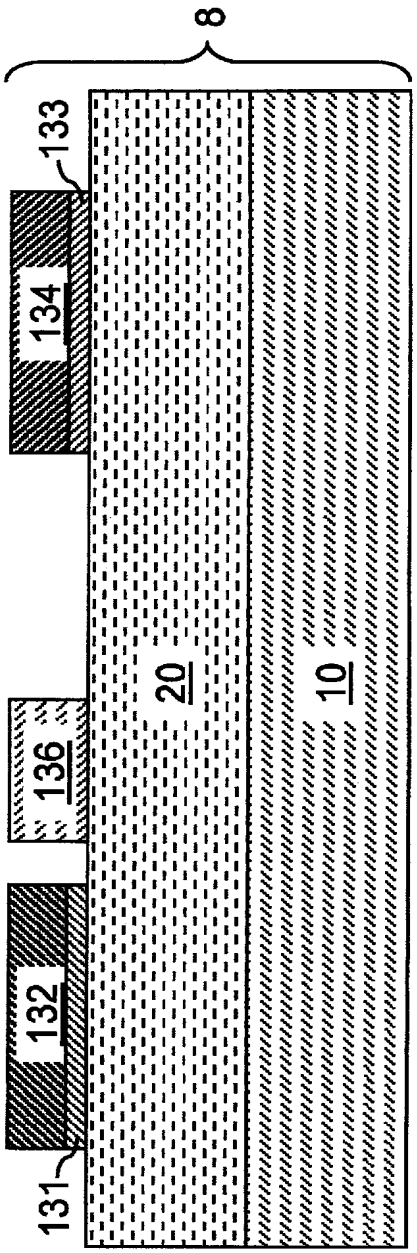

FIG. 12A

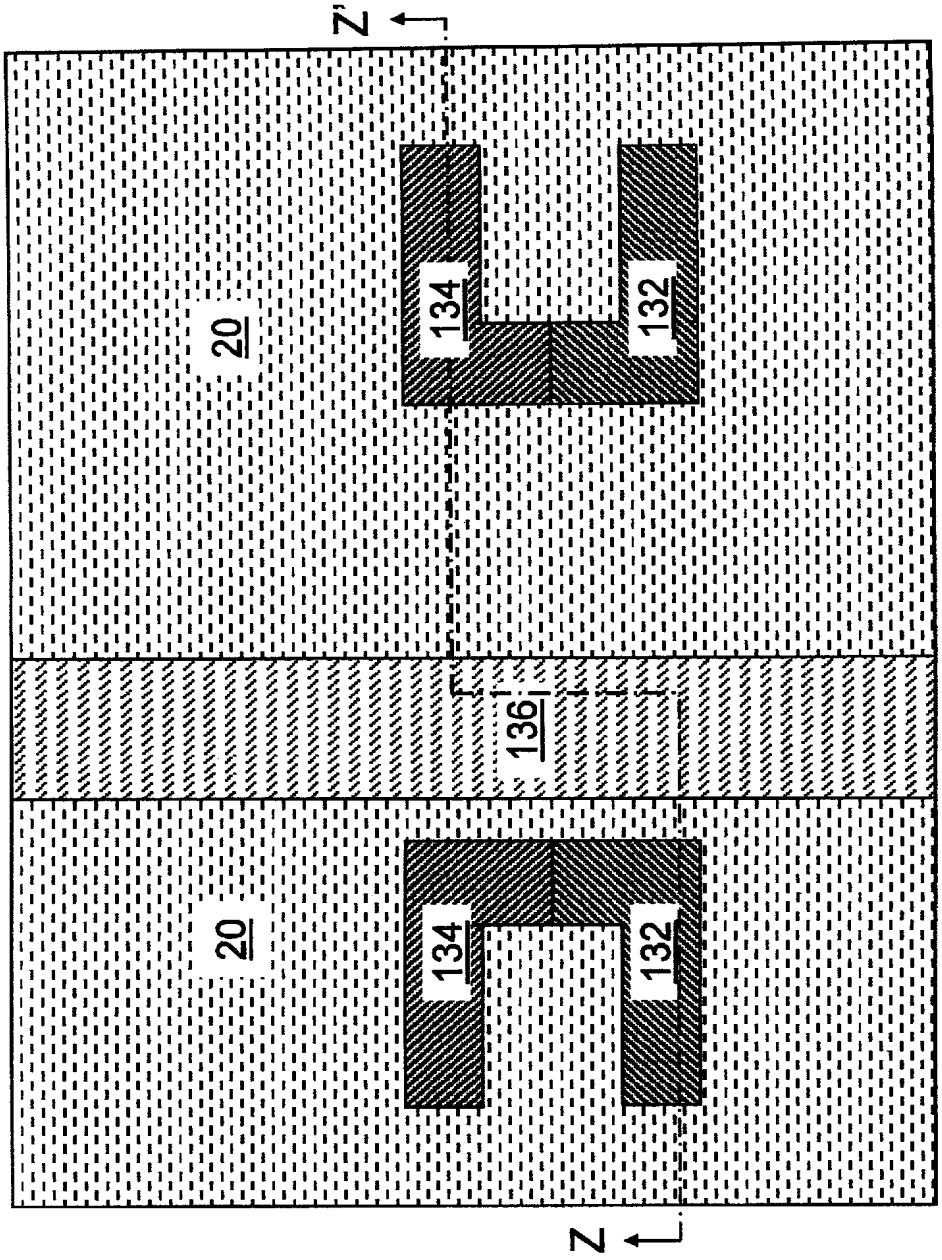

FIG. 12B

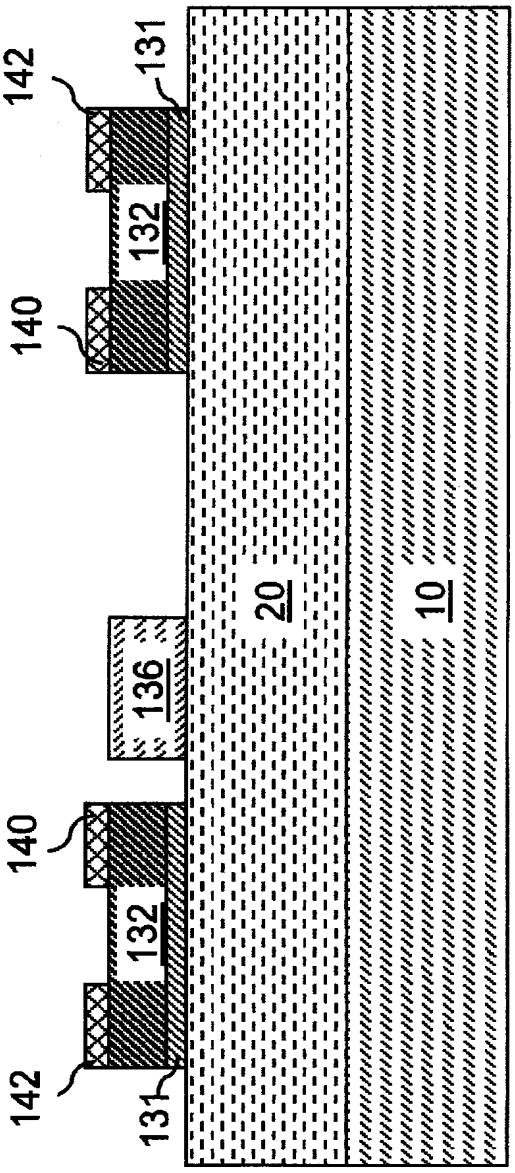

FIG. 13A

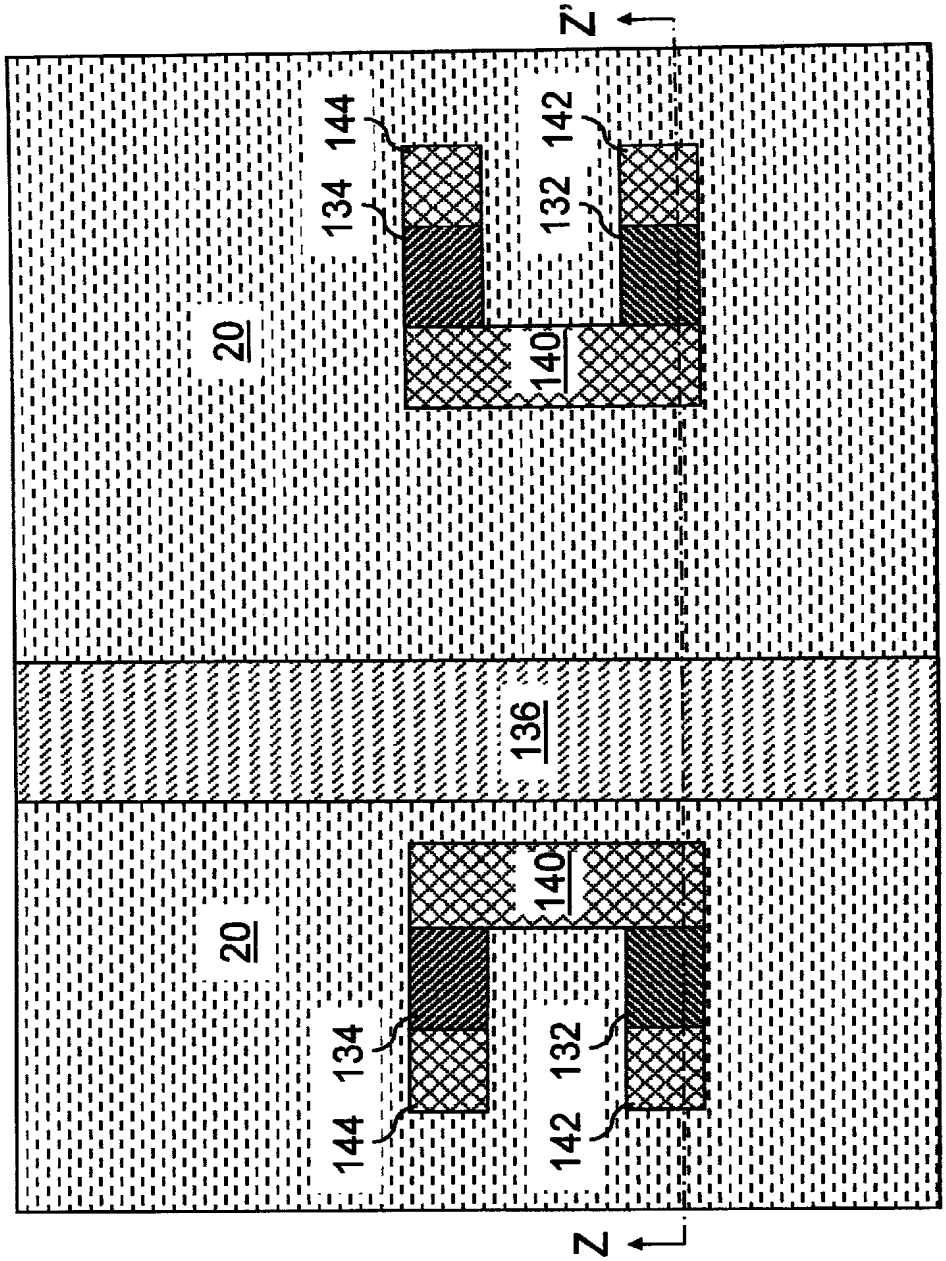

FIG. 13B

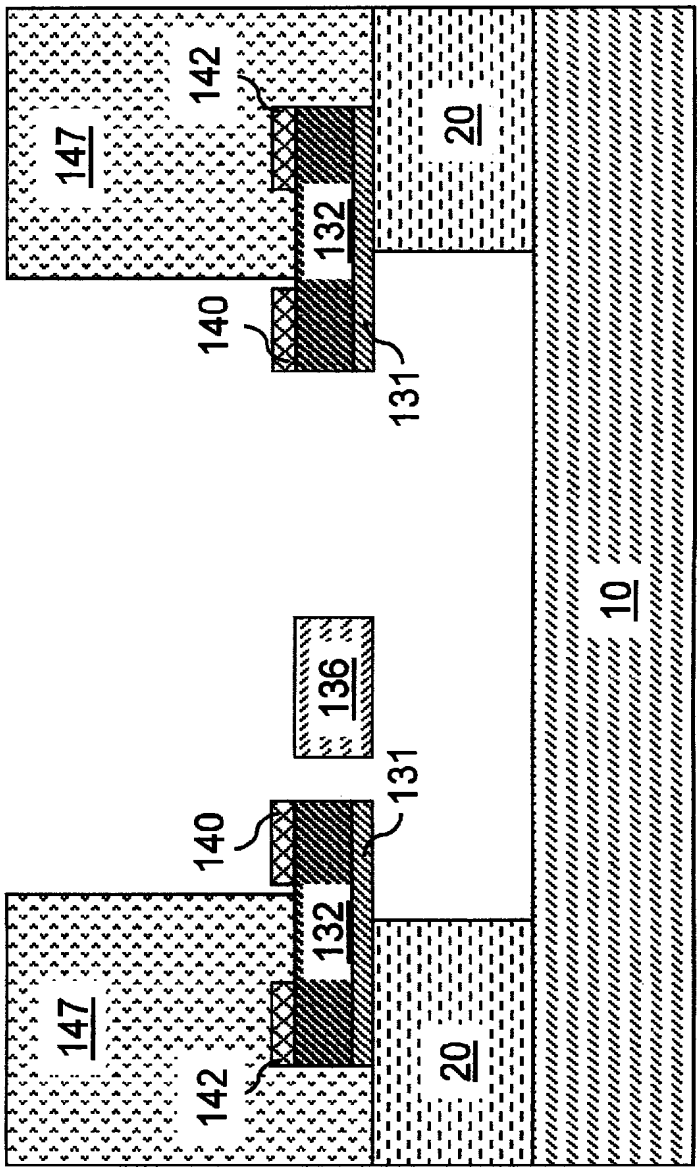

FIG. 14A

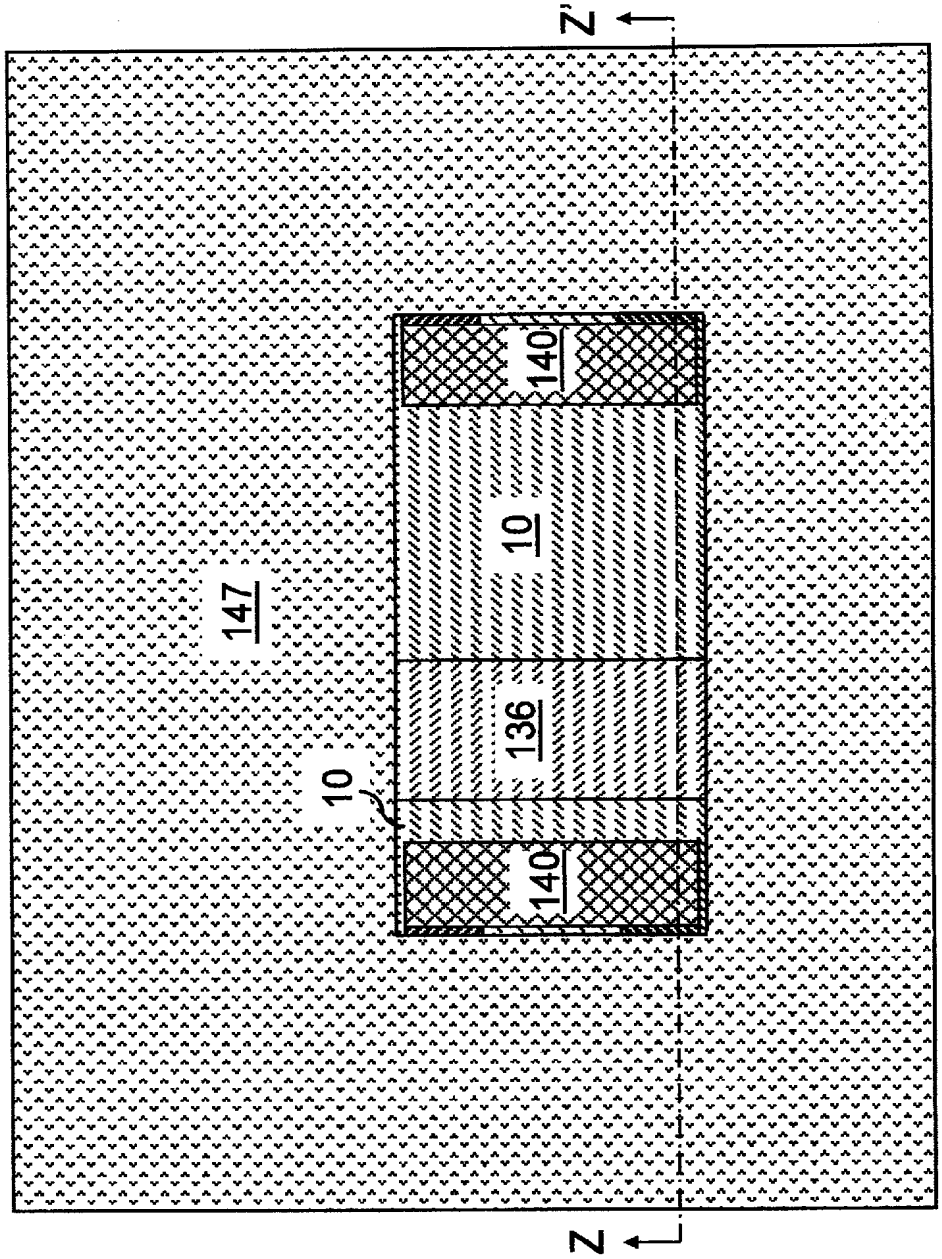

FIG. 14B

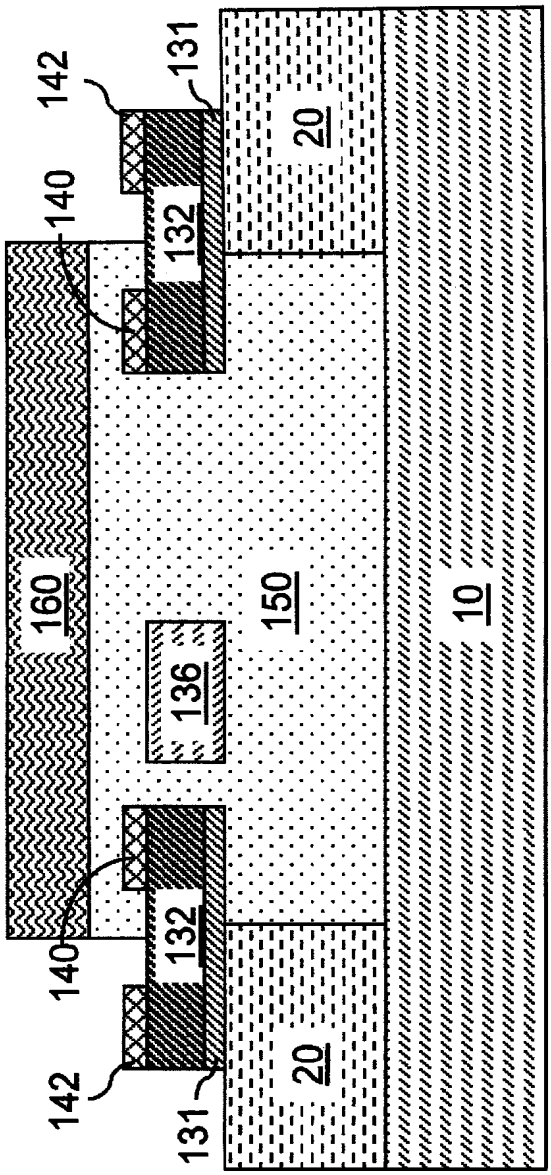

FIG. 15A

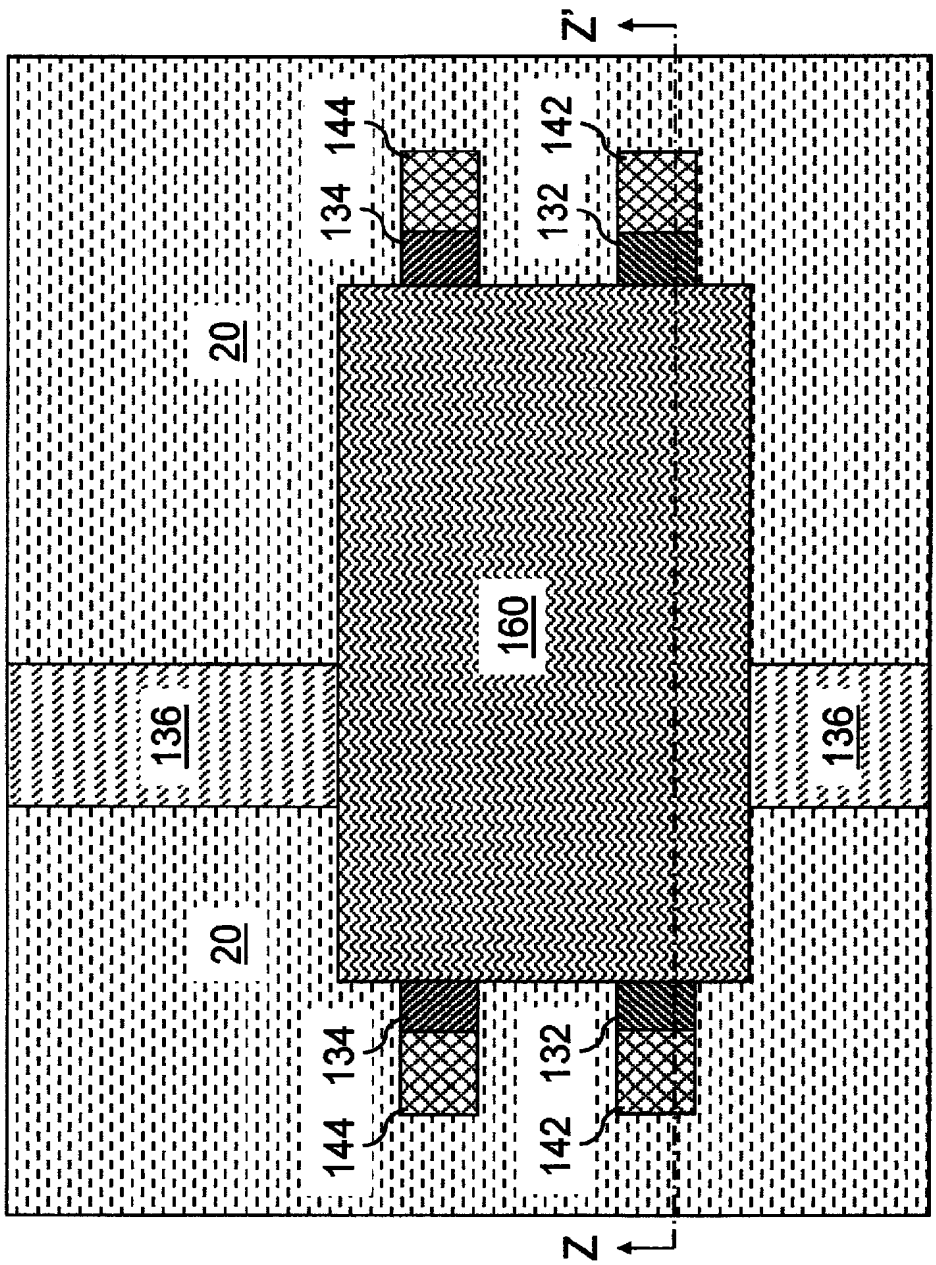

FIG. 15B

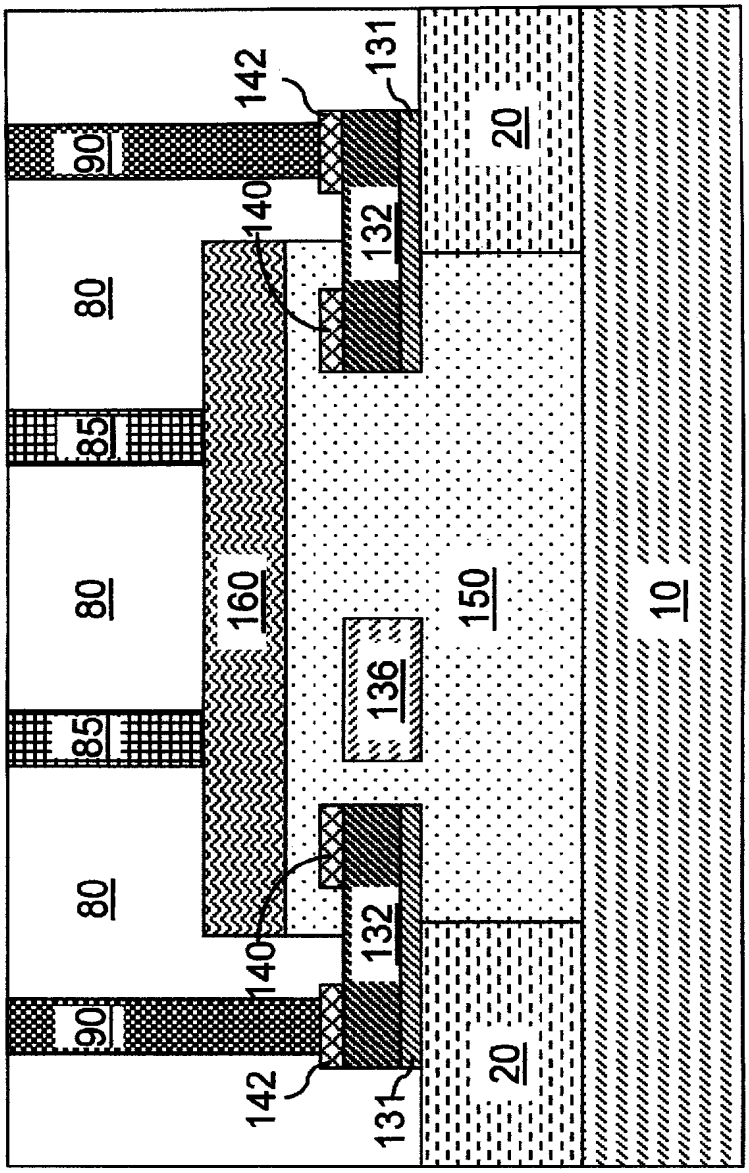
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FIG. 16A

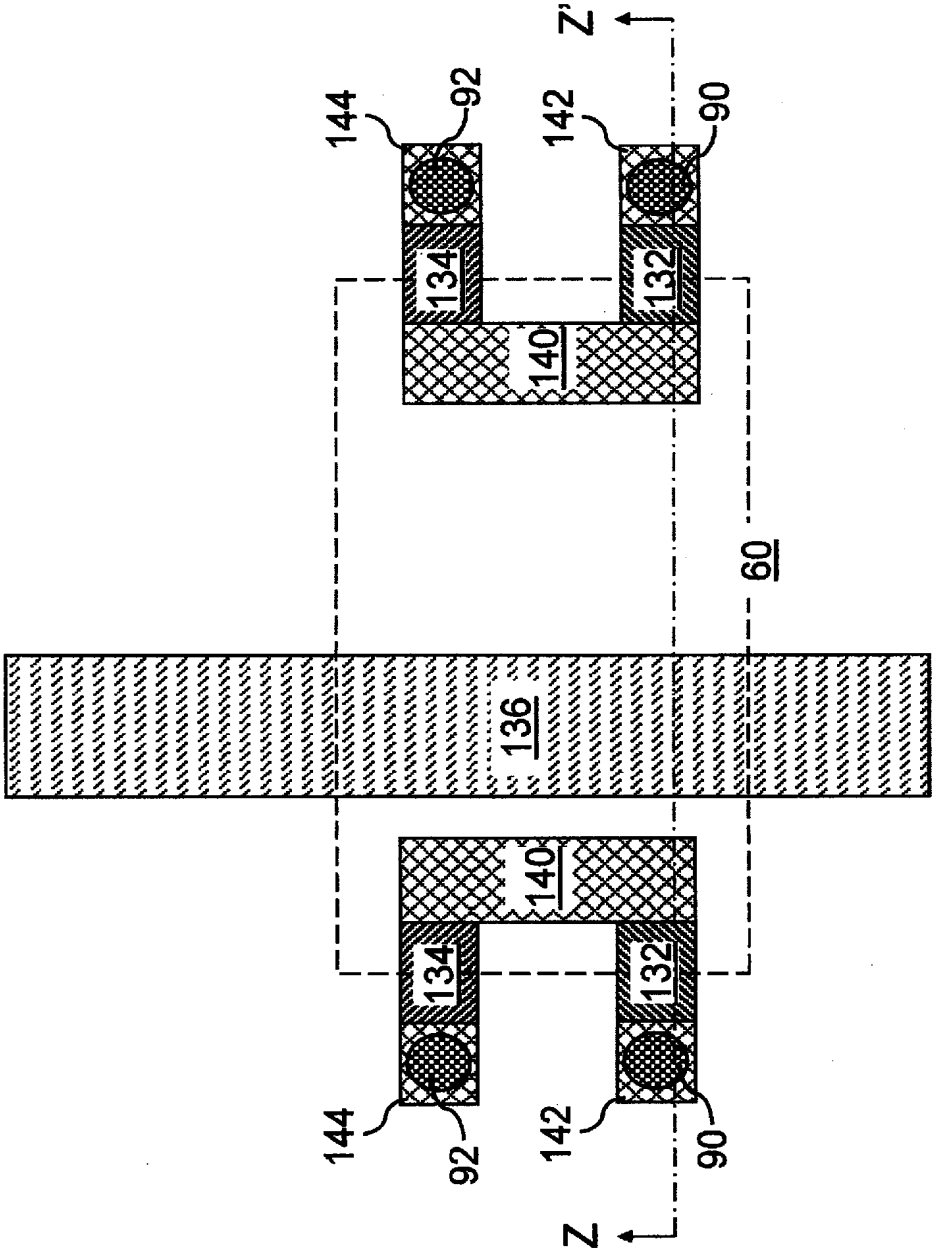

FIG. 16B

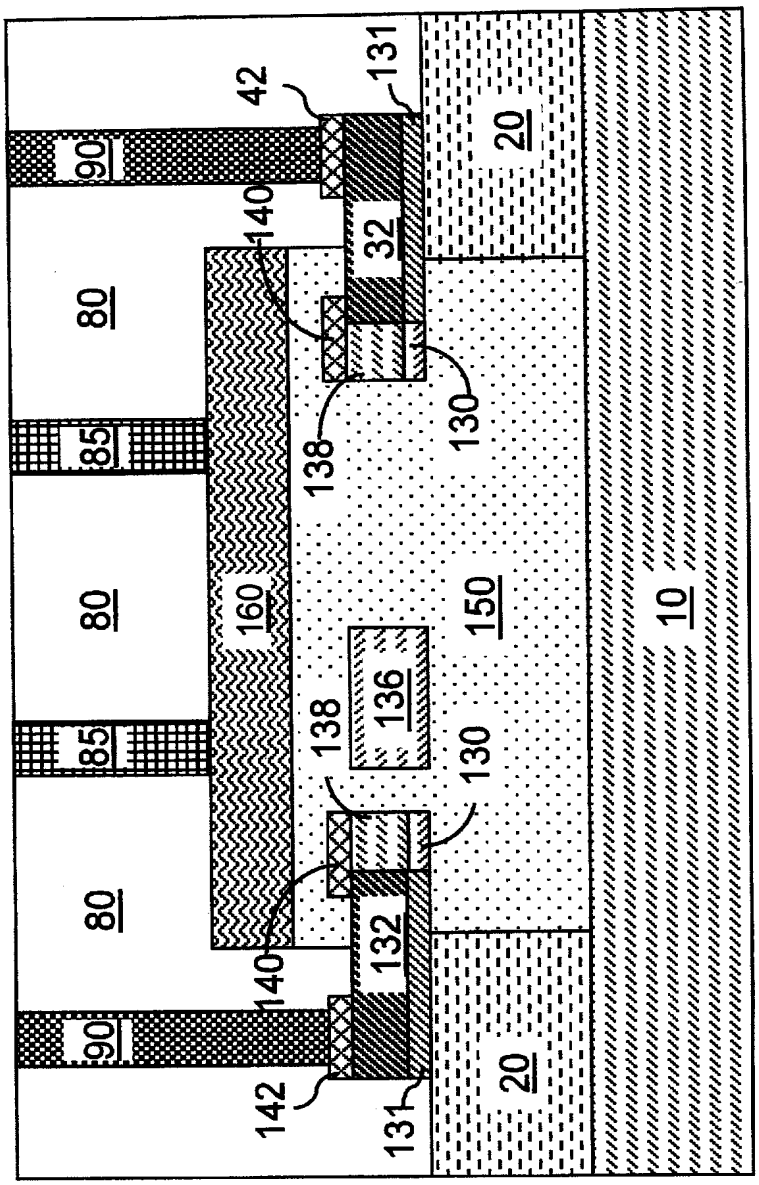
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FIG. 17

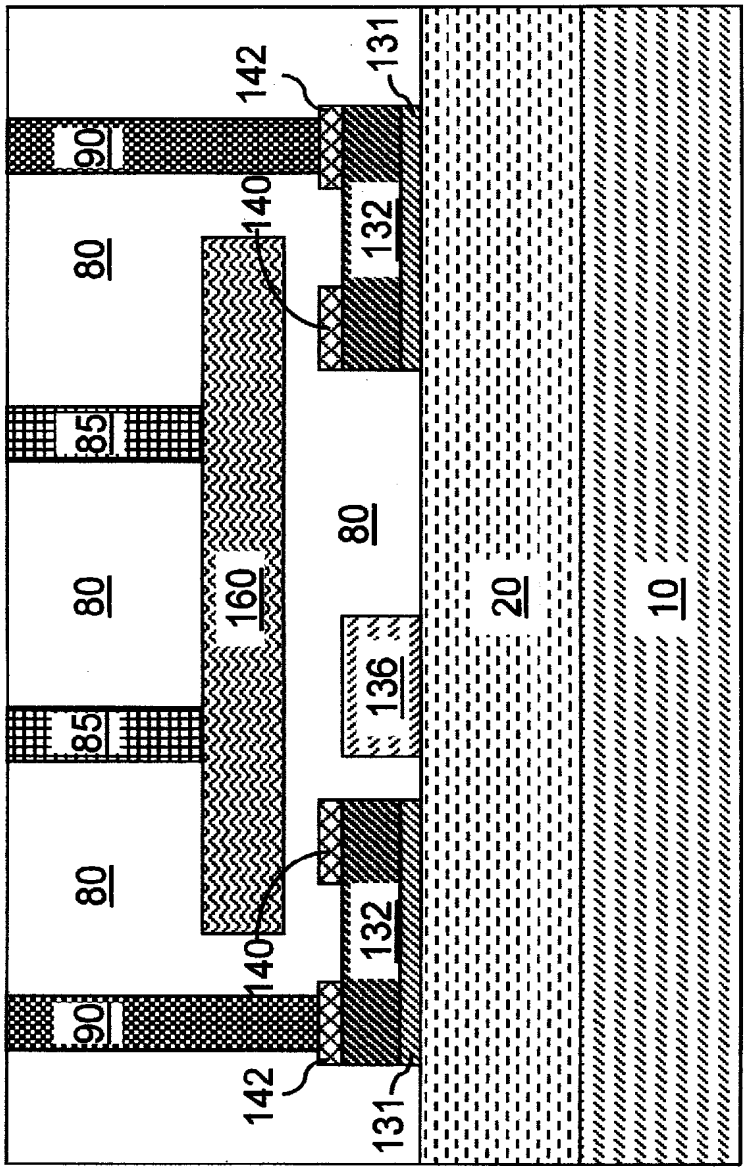
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FIG. 18

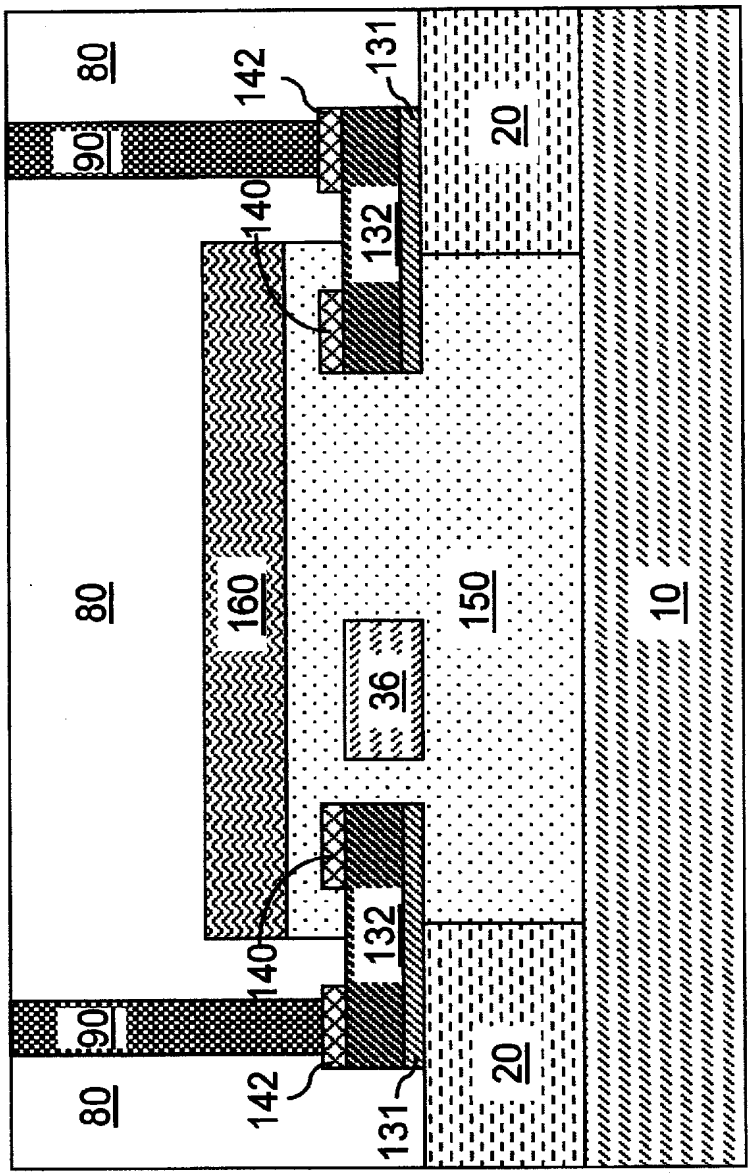

FIG. 19

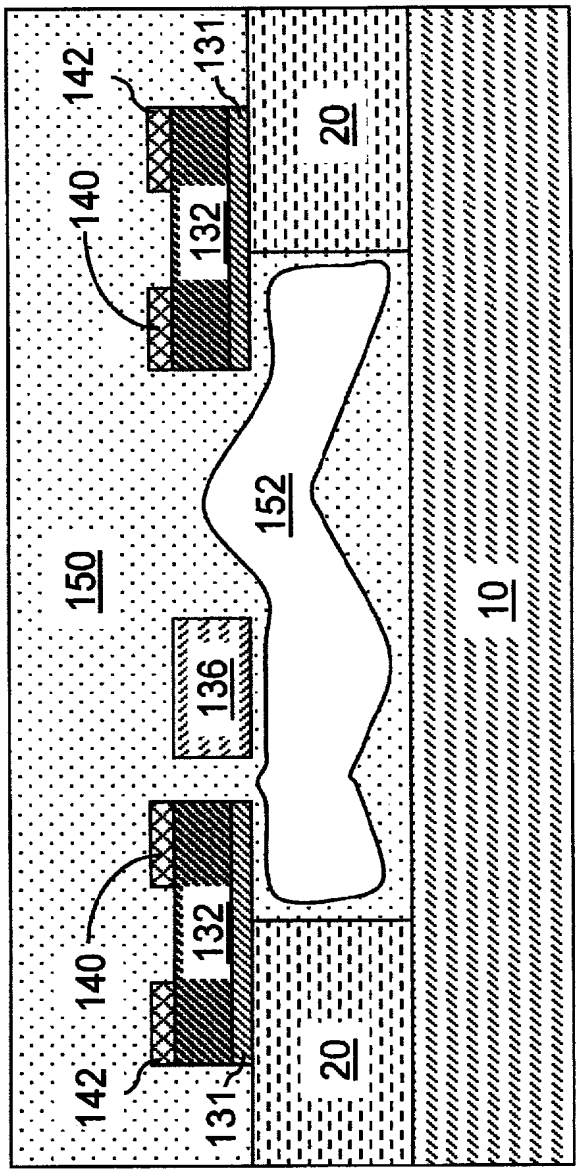

FIG. 20

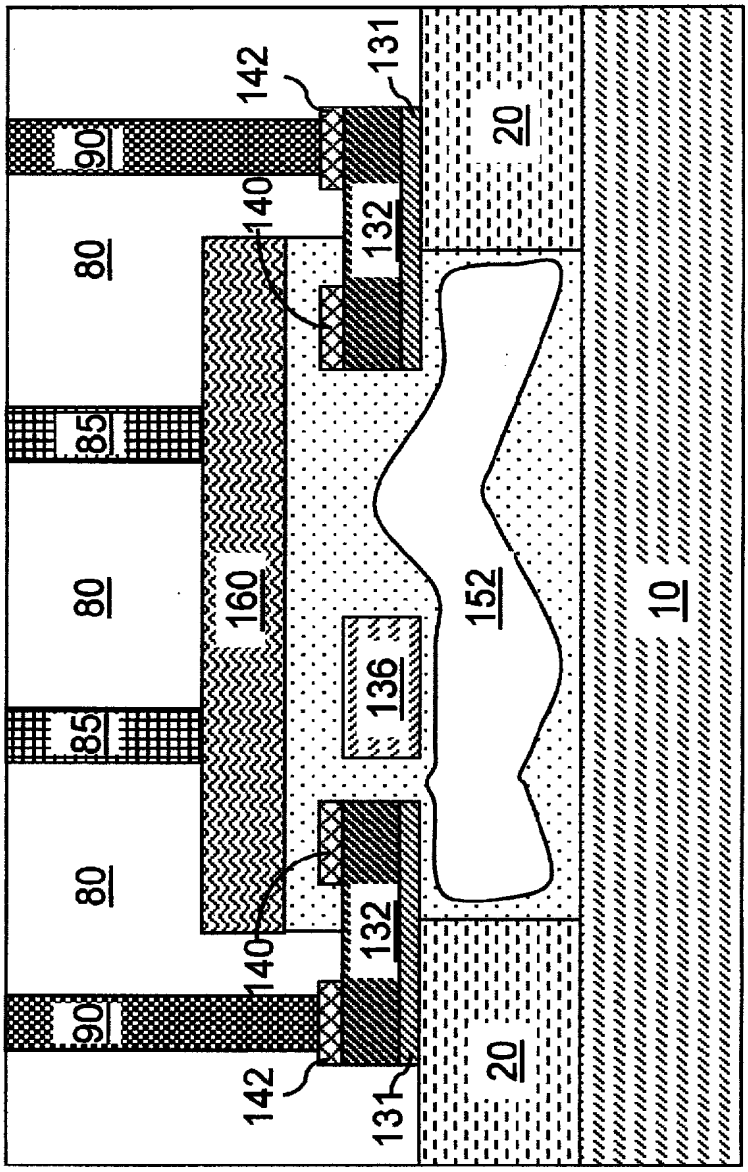
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FIG. 21

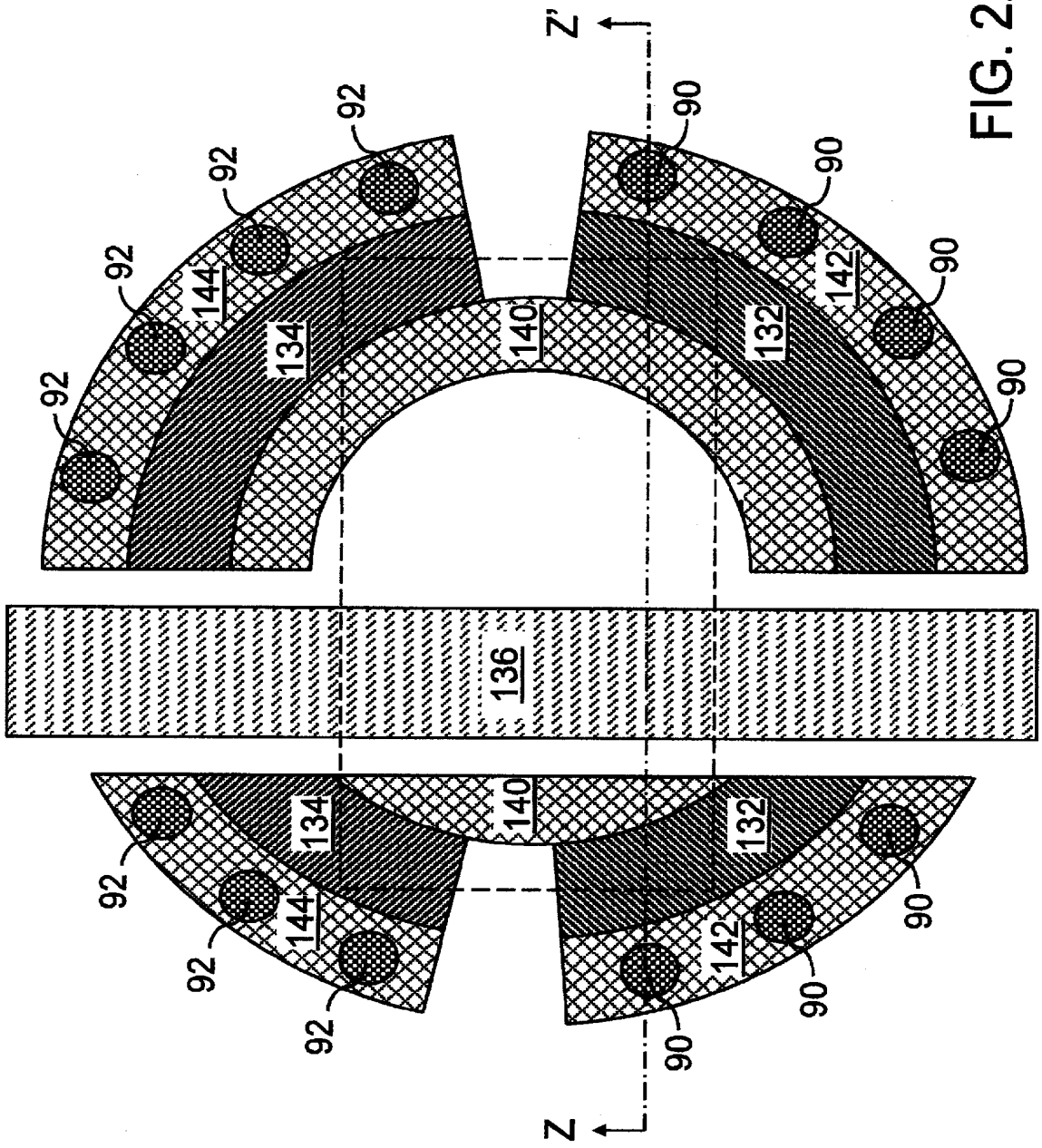

FIG. 22

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2010/059571

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L31/105 H01L31/18 H01L35/30 H01L23/38 G02B6/42
G02F1/01 G02F1/025
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L G02B G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 970 611 B1 (VAN DER VLIET FREDERIK MARCEL [US] ET AL) 29 November 2005 (2005-11-29) column 3, line 18 - column 11, line 64; figures 1A-8F	1-20
X	GB 2 332 284 A (BOOKHAM TECHNOLOGY LTD [GB]) 16 June 1999 (1999-06-16) page 9, line 11 - page 11, line 25; figures 1-4	1-20
A	US 7 340 709 B1 (MASINI GIANLORENZO [US] ET AL) 4 March 2008 (2008-03-04) column 4, line 4 - column 8, line 34; figures 1-8b	1-20

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 October 2010	21/10/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Albrecht, Claus

Form PCT/ISA/210 (second sheet) (April 2005)

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2010/059571

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005/207704 A1 (KEYSER THOMAS [US] ET AL) 22 September 2005 (2005-09-22) paragraph [0033] - paragraph [0050]; figures 1-8	1-20

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2010/059571

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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
24 March 2011 (24.03.2011)

PCT

(10) International Publication Number
WO 2011/035188 A2

(51) International Patent Classification:
H01L 27/146 (2006.01) *H01L 27/148* (2006.01)

(21) International Application Number:
PCT/US2010/049375

(22) International Filing Date:
17 September 2010 (17.09.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/243,434 17 September 2009 (17.09.2009) US
61/311,004 5 March 2010 (05.03.2010) US
61/311,107 5 March 2010 (05.03.2010) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

(54) Title: PHOTOSENSITIVE IMAGING DEVICES AND ASSOCIATED METHODS

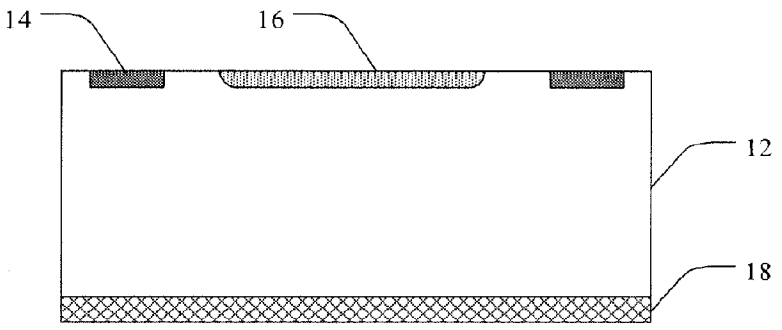

FIG. 1

(57) Abstract: Photosensitive devices and associated methods are provided. In one aspect, for example, a photosensitive imager device can include a semiconductor substrate having multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. In one aspect, the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation. In another aspect, interacting with electromagnetic radiation further includes increasing the semiconductor substrate's effective absorption wavelength as compared to a semiconductor substrate lacking a textured region.

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PHOTOSENSITIVE IMAGING DEVICES AND ASSOCIATED METHODS

PRIORITY DATA

This application claims the benefit of U.S. Provisional Patent Application Serial No. 61/243,434, filed on September 17, 2009, U.S. Provisional Patent Application Serial No. 61/311,004 filed on March 5, 2010, and U.S. Provisional Patent Application Serial No. 61/311,107, filed on March 5, 2010, each of which is incorporated herein by reference.

BACKGROUND

The interaction of light with semiconductor materials has been a significant innovation. Silicon imaging devices are used in various technologies, such as digital cameras, optical mice, video cameras, cell phones, and the like. Charge-coupled devices (CCDs) were widely used in digital imaging, and were later improved upon by complementary metal-oxide-semiconductor (CMOS) imagers having increased performance. CMOS sensors are typically manufactured from silicon and can covert visible incident light into a photocurrent and ultimately into a digital image. Silicon-based technologies for detecting infrared incident electromagnetic radiation have been problematic, however, because silicon is an indirect bandgap semiconductor having a bandgap of about 1.1eV. Thus the absorption of electromagnetic radiation having wavelengths of greater than about 1100 nm is, therefore, very low in silicon.

SUMMARY

The present disclosure provides photosensitive devices and associated methods. In one aspect, for example, a photosensitive imager device can include a semiconductor substrate having multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. In one aspect, the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation. In another aspect, interacting with electromagnetic radiation further includes increasing the semiconductor substrate's effective absorption length as compared to a semiconductor substrate lacking a textured region. In one specific aspect, the transfer

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element is selected from the group consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.

The textured region can be positioned in a variety of locations relative to the doped regions. In one aspect, for example, the textured region is positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions. In one specific aspect, the textured region has a surface morphology operable to direct electromagnetic radiation into or out of the semiconductor substrate. The surface morphology of the textured region relative to the semiconductor substrate can include a variety of configurations, including, without limitation, sloping, pyramidal, inverted pyramidal, spherical, parabolic, asymmetric, symmetric, and the like, including combinations thereof.

In another aspect, the textured region can be positioned on a surface of the semiconductor substrate that is adjacent the multiple doped regions. In a more specific aspect, an additional textured region can be positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions. In this manner, textured regions can thus be positioned adjacent to multiple doped regions and opposite the multiple doped regions.

Various aspects of the textured region can vary depending on the desired configuration of the device. In one aspect, however, the textured region includes surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof. Numerous surface feature morphologies are contemplated, nonlimiting examples of which include cones, pillars, pyramids, micolenses, quantum dots, inverted features, and combinations thereof. Additionally, the textured region can be formed by a variety of processes. Nonlimiting examples of such texturing processes can include lazing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, and combinations thereof.

Additional layers and/or structures can be included in various devices according to aspects present disclosure. In one aspect, for example, a reflective layer can be coupled to the semiconductor substrate and positioned to maintain the electromagnetic radiation in the semiconductor substrate. In another aspect, a lens can be optically coupled to the semiconductor substrate and positioned to focus incident electromagnetic radiation into the semiconductor substrate.

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In another aspect of the present disclosure, a method of making a photosensitive imager device is provided. Such a method can include forming a textured region on a semiconductor substrate having multiple doped regions forming a least one junction, wherein the textured region is formed in a position to interact with electromagnetic radiation and coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction.

In one aspect, the photosensitive imager device can be tuned to be selected to filter out specific electromagnetic radiation wavelengths. In one specific aspect, tuning includes forming surface features to have dimensions that selectively diffuse or selectively absorb a desired wavelength of electromagnetic radiation. In another aspect, tuning is accomplished through a factor selected from the group consisting of placement of the textured region, material type and/or thickness of the textured region, dopant type of the textured region, doping profile of the texture region, dopant profile of the semiconductor substrate, material type and/or thickness of the semiconductor substrate, and combinations thereof.

In another aspect of the present disclosure, a photosensitive imager device is provided. Such a device can include a semiconductor substrate having multiple doped regions forming a least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and at least 4 transistors coupled to the semiconductor substrate and with at least one of the transistors electrically coupled to the at least one junction.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic view of a photosensitive device in accordance with one aspect of the present disclosure;

FIG. 2 is a schematic view of a photosensitive device in accordance with another aspect of the present disclosure;

FIG. 3 is a schematic view of a photosensitive device in accordance with yet another aspect of the present disclosure;

FIG. 4 is a schematic view of a photosensitive device in accordance with a further aspect of the present disclosure;

FIG. 5 is a schematic view of a photosensitive device in accordance with yet a further aspect of the present disclosure;

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FIG. 6 is a schematic view of a photosensitive device in accordance with another aspect of the present disclosure;

FIG. 7 is a schematic view of a photosensitive pixel device in accordance with yet another aspect of the present disclosure;

FIG. 8 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

FIG. 9 is a schematic view of a photosensitive pixel device in accordance with yet a further aspect of the present disclosure;

FIG. 10 is a schematic view of a photosensitive pixel device in accordance with another aspect of the present disclosure;

FIG. 11 is a schematic view of a photosensitive pixel device in accordance with yet another aspect of the present disclosure;

FIG. 12 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

FIG. 13 is a schematic view of a photosensitive pixel device in accordance with another aspect of the present disclosure;

FIG. 14 is a schematic view of a photosensitive imager device in accordance with yet another aspect of the present disclosure;

FIG. 15 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

FIG. 16 is a schematic view of a photosensitive pixel device in accordance with another aspect of the present disclosure; and

FIG. 17 is a depiction of a method of making a photosensitive imager device in accordance with yet another aspect of the present disclosure.

DETAILED DESCRIPTION

Before the present disclosure is described herein, it is to be understood that this disclosure is not limited to the particular structures, process steps, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting.

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Definitions

The following terminology will be used in accordance with the definitions set forth below.

It should be noted that, as used in this specification and the appended claims, the singular forms "a," and, "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a dopant" includes one or more of such dopants and reference to "the layer" includes reference to one or more of such layers.

As used herein, the term "low oxygen content" refers to any material having an interstitial oxygen content that is less than or equal to about 60 ppm atomic.

As used herein, the terms "disordered surface" and "textured surface" can be used interchangeably, and refer to a surface having a topology with nano- to micron-sized surface variations formed by the irradiation of laser pulses. While the characteristics of such a surface can be variable depending on the materials and techniques employed, in one aspect such a surface can be several hundred nanometers thick and made up of nanocrystallites (e.g. from about 10 to about 50 nanometers) and nanopores. In another aspect, such a surface can include micron-sized structures (e.g. about 2 μm to about 60 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 500 μm.

As used herein, the term "fluence" refers to the amount of energy from a single pulse of laser radiation that passes through a unit area. In other words, "fluence" can be described as the energy density of one laser pulse.

As used herein, the terms "surface modifying" and "surface modification" refer to the altering of a surface of a semiconductor material using laser radiation. In one specific aspect, surface modification can include processes using primarily laser radiation or laser radiation in combination with a dopant, whereby the laser radiation facilitates the incorporation of the dopant into a surface of the semiconductor material. Accordingly, in one aspect surface modification includes doping of a semiconductor material.

As used herein, the term "target region" refers to an area of a semiconductor material that is intended to be doped or surface modified using laser radiation. The target region of a semiconductor material can vary as the surface modifying process progresses. For example, after a first target region is doped or surface modified, a second target region may be selected on the same semiconductor material.

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As used herein, the term "detection" refers to the sensing, absorption, and/or collection of electromagnetic radiation.

As used herein, the term "substantially" refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is "substantially" enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use of "substantially" is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is "substantially free of" particles would either completely lack particles, or so nearly completely lack particles that the effect would be the same as if it completely lacked particles. In other words, a composition that is "substantially free of" an ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

As used herein, the term "about" is used to provide flexibility to a numerical range endpoint by providing that a given value may be "a little above" or "a little below" the endpoint.

As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of "about 1 to about 5" should be interpreted to include

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not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

The Disclosure

Electromagnetic radiation can be present across a broad wavelength range, including visible range wavelengths (approximately 350nm to 800nm) and non-visible wavelengths (longer than about 800nm or shorter than 350 nm). The infrared spectrum is often described as including a near infrared portion of the spectrum including wavelengths of approximately 800 to 1300 nm, a short wave infrared portion of the spectrum including wavelengths of approximately 1300 nm to 3 micrometers, and a mid to long wave infrared (or thermal infrared) portion of the spectrum including wavelengths greater than about 3 micrometers up to about 30 micrometers. These are generally and collectively referred to herein as "infrared" portions of the electromagnetic spectrum unless otherwise noted.

Traditional silicon photodetecting imagers have limited light absorption/detection properties. For example, infrared light is mostly transparent to such silicon based detectors. While other materials (e.g. InGaAs) can be used to detect infrared electromagnetic radiation having wavelengths greater than about 1000 nm, silicon is still commonly used because it is relatively cheap to manufacture and can be used to detect wavelengths in the visible spectrum (i.e. visible light, 350 nm – 800 nm). Traditional silicon materials require substantial absorption depths to detect photons having wavelengths longer than approximately 700 nm. While visible light can be absorbed at relatively shallow depths in silicon, absorption of longer wavelengths (e.g. 900 nm) in silicon of a standard wafer depth (e.g. approximately 750 μm) is poor if at all. The devices of the present disclosure increase the absorption of semiconductor materials by decreasing the effective absorption length to longer wavelengths as compared to traditional materials. For example, the absorption depth of silicon can be reduced such that these longer wavelengths can be absorbed at depths of less than or equal to about 850 μm. In other words, by decreasing the

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effective absorption length these devices are able to absorb longer wavelengths (e.g. >1000 nm for silicon) within a thin semiconductor material. In addition to increasing the effective absorption length, the response rate or response speed can also be increased using thinner semiconductor materials.

The present disclosure additionally provides broadband photosensitive diodes, pixels, and imagers capable of detecting visible as well as infrared electromagnetic radiation, including associated methods of making such devices. A photosensitive diode can include a semiconductor substrate having multiple doped regions forming at least one junction, and at least one textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation. In one aspect the multiple doped regions can include at least one cathode region and at least one anode region. In some aspects, doped regions can include an n-type dopant and/or a p-type dopant as is discussed below, thereby creating a p-n junction. In other aspects, a photosensitive device can include an i-type region to form a p-i-n junction.

A photosensitive pixel can include a semiconductor substrate having multiple doped regions forming at least one junction, at least one textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. A photosensitive imager can include multiple photosensitive pixels. Additionally, an electrical transfer element can include a variety of devices, including without limitation, transistors, sensing nodes, transfer gates, transfer electrodes, and the like.

Photosensitive or photodetecting imagers include photodiodes or pixels that are capable of absorbing electromagnetic radiation within a given wavelength range. Such imagers can be passive pixel sensors (PPS), active pixel sensors (APS), digital pixel sensor imagers (DPS), or the like, with one difference being the image sensor read out architecture. For example, a semiconducting photosensitive imager can be a three or four transistor active pixel sensor (3T APS or 4T APS). Various additional components are also contemplated, and would necessarily vary depending on the particular configuration and intended results. As and example, a 4T configuration can additionally include, among other things, a transfer gate, a reset, a source follower, and row select transistors. Additionally, devices having greater than 4 transistors are also within the present scope.

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Photosensitive imagers can be front side illumination (FSI) or back side illumination (BSI) devices, and there are advantages and disadvantages to both architecture types. In a typical FSI imager, incident light enters the semiconductor device by first passing by transistors and metal circuitry. The light, however, can scatter off of the transistors and circuitry prior to entering the light sensing portion of the imager, thus causing optical loss and noise. A lens can be disposed on the topside of a FSI pixel to direct and focus the incident light to the light sensing active region of the device, thus partially avoiding the circuitry. In one aspect the lens can be a ulens. BSI imagers, one the other hand, are configured to have the depletion region of the junction extending to the opposite side of the device. In one aspect, for example, incident light enters the device via the light sensing portion and is mostly absorbed prior to reaching the circuitry. BSI designs allow for smaller pixel architecture and a high fill factor for the imager. As mentioned, the present disclosure can be adapted for either configuration. It should also be understood that devices according to aspects of the present disclosure can be incorporated into complimentary metal-oxide-semiconductor (CMOS) imager architectures or charge-coupled device (CCD) imager architectures.

In one aspect, as is shown in FIG. 1, a photosensitive diode 10 can include a semiconductor substrate 12 having multiple doped regions 14, 16 forming at least one junction, and at least one textured region 18 coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation. The different doped regions can have the same doping profile or different doping profiles, depending on the device. Such an architecture is a FSI design where light enters the semiconductor substrate from the direction of the multiple doped regions. While the device shown in FIG. 1 contains three doped regions, it should be noted that aspects containing one or more doped regions are considered to be within the present scope. Additionally, the semiconductor substrate can be doped, and thus can be considered to be a doped region in some aspects. It should also be noted that the photosensitive diode can be configured with a BSI architecture, and thus electromagnetic radiation would enter the semiconductor substrate from the direction of the textured region.

The various devices according to aspects of the present disclosure can exhibit increased quantum efficiency over traditional photosensitive devices. Any increase in the quantum efficiency makes a large difference in the signal to noise ratio. More complex structures can provide not only increased quantum efficiency but also good

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uniformity from pixel to pixel. In addition, devices of the present disclosure exhibit increased responsivity as compared to traditional photosensitive devices. For example, in one aspect the responsivity can be greater than or equal to 0.8A/W for wavelengths greater than 1000 nm for semiconductor substrate that is less than 100 μm thick.

Photosensitive imagers can be maintained under constant conditions (fixed voltage or current) to provide enhanced linearity and uniformity. Connections between the imager and the underlying device layers can be achieved using vias fabricated from a refractory metal, such as tungsten or tantalum. Placing storage elements under the imager may provide various photonic benefits. For example, the entire pixel array may be dedicated to signal processing. This may enable higher performance by permitting access to low level pixel signals. Furthermore, massively parallel operations can be performed by pixel processors. For example, analog to digital conversion, noise reduction (ie., true correlated double sampling), power conditioning, nearest neighbor pixel processing, compression, fusion, and color multiplexing operations can be performed.

A variety of semiconductor materials are contemplated for use with the devices and methods according to aspects of the present disclosure. Non-limiting examples of such semiconductor materials can include group IV materials, compounds and alloys comprised of materials from groups II and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can include silicon carbide (SiC) and silicon germanium (SiGe). In one specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum gallium arsenide, and combinations thereof.

Exemplary combinations of group II-VI materials can include cadmium selenide (CdSe), cadmium sulfide (CdS), cadmium telluride (CdTe), zinc oxide (ZnO), zinc selenide (ZnSe), zinc sulfide (ZnS), zinc telluride (ZnTe), cadmium zinc

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telluride (CdZnTe, CZT), mercury cadmium telluride (HgCdTe), mercury zinc telluride (HgZnTe), mercury zinc selenide (HgZnSe), and combinations thereof.

Exemplary combinations of group III-V materials can include aluminum antimonide (AlSb), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum phosphide (AlP), boron nitride (BN), boron phosphide (BP), boron arsenide (BAs), gallium antimonide (GaSb), gallium arsenide (GaAs), gallium nitride (GaN), gallium phosphide (GaP), indium antimonide (InSb), indium arsenide (InAs), indium nitride (InN), indium phosphide (InP), aluminum gallium arsenide (AlGaAs, $Al_xGa_{1-x}As$), indium gallium arsenide (InGaAs, $In_xGa_{1-x}As$), indium gallium phosphide (InGaP), aluminum indium arsenide (AlInAs), aluminum indium antimonide (AlInSb), gallium arsenide nitride (GaAsN), gallium arsenide phosphide (GaAsP), aluminum gallium nitride (AlGaN), aluminum gallium phosphide (AlGaP), indium gallium nitride (InGaN), indium arsenide antimonide (InAsSb), indium gallium antimonide (InGaSb), aluminum gallium indium phosphide (AlGaInP), aluminum gallium arsenide phosphide (AlGaAsP), indium gallium arsenide phosphide (InGaAsP), aluminum indium arsenide phosphide (AlInAsP), aluminum gallium arsenide nitride (AlGaAsN), indium gallium arsenide nitride (InGaAsN), indium aluminum arsenide nitride (InAlAsN), gallium arsenide antimonide nitride (GaAsSbN), gallium indium nitride arsenide antimonide (GaInNAsSb), gallium indium arsenide antimonide phosphide (GaInAsSbP), and combinations thereof.

The semiconductor material can be of any thickness that allows electromagnetic radiation detection and conversion functionality, and thus any such thickness of semiconductor material is considered to be within the present scope. In some aspects the laser processed region of the semiconductor increases the efficiency of the device such that the semiconductor material can be thinner than has previously been possible. Decreasing the thickness of the semiconductor reduces the amount of semiconductor material required to make such a device. In one aspect, for example, the semiconductor material has a thickness of from about 500 nm to about 50 μm. In another aspect, the semiconductor material has a thickness of less than or equal to about 500 μm. In yet another aspect, the semiconductor material has a thickness of from about 1 μm to about 10 μm. In a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 750 μm. In yet a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 100 μm.

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Additionally, various types of semiconductor material are contemplated, and any such material that can be incorporated into an electromagnetic radiation detection device is considered to be within the present scope. In one aspect, for example, the semiconductor material is monocrystalline. In another aspect, the semiconductor material is multicrystalline. In yet another aspect, the semiconductor material is microcrystalline. It is also contemplated that the semiconductor material can be amorphous. Specific nonlimiting examples include amorphous silicon or amorphous selenium.

The semiconductor materials of the present disclosure can also be made using a variety of manufacturing processes. In some cases the manufacturing procedures can affect the efficiency of the device, and may be taken into account in achieving a desired result. Exemplary manufacturing processes can include Czochralski (Cz) processes, magnetic Czochralski (mCz) processes, Float Zone (FZ) processes, epitaxial growth or deposition processes, and the like. Whether or not low oxygen content is desired in the device can also affect the choice of a manufacturing process for the semiconductor material. Various processes produce semiconductor materials containing varying amounts of oxygen, and as such, some applications having more stringent tolerances with respect to oxygen levels may benefit more from specific manufacturing procedures as compared to others. For example, during CZ crystal growth oxygen from the containment vessel, usually a quartz crucible, can become incorporated into the crystal as it is pulled. Additionally, other sources of oxygen contamination are also possible with the CZ process. Such contamination may be reduced, however, through the use of non oxygen-containing crucible materials, as well as the development of other crystal growth methods that do not utilize a crucible. One such process is the FZ process.

Materials grown with the CZ method can also be made to have lowered oxygen concentration through enhancements to the crystal growth process, such as growing the crystal in the presence of a magnetic field (i.e. the mCz process). Also, gettering techniques can be employed to reduce the impact of oxygen or other impurities on the finished device. These gettering techniques can include thermal cycles to liberate or nucleate impurities, or selective ion implantation of species to serve as gettering sites for the impurities. For example, oxygen concentrated in the semiconductor can be removed by the performing a furnace cycle to form a denuded zone. During heating with an inert gas, oxygen near the surface of the semiconductor

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diffuses out of the material. During the furnace cycle but after the denuding step, nucleating and growing steps may be performed. Nucleating sites for precipitates are formed during the nucleating step, and the precipitates are grown from the nucleating sites during a growing step. The precipitates are formed from interstitial oxygen within the bulk of the semiconductor material and beneath the denuded zone. The precipitation of oxygen in the bulk of the semiconductor material can be desired because such precipitates can act as gettering sites. Such precipitate formation can also be performed to "lock up" interstitial oxygen into the precipitates and reduce the likelihood that such oxygen can migrates from the bulk of the semiconductor material into the denuded zone.

In those aspects where low oxygen content of the device is desired, further processing of the semiconductor material can be performed so as to minimize the introduction of oxygen. Oxygen can exist in different states or at different sites (for example, interstitially or substitutionally) within a semiconductor such as silicon, dependent upon the thermal processing the semiconductor has received. If the semiconductor is subjected to temperatures higher than, for example, about 1000° C, oxygen can form aggregates or clusters that serve as defect sites in the crystal lattice. These sites may result in trap states and a reduction in carrier lifetime within the semiconductor material and device can occur. At lower temperatures (for example, around 400° C to 700° C), oxygen can behave as electrically active thermal donors. Thus, oxygen can have a negative impact on carrier lifetime and on carrier mobility. In a device fabricated to have photoconductive gain, the presence of oxygen causing reduced carrier lifetime may result in reduced levels of photoconductive gain.

It may be beneficial, therefore, to produce semiconductor devices such that a low oxygen content is obtained or maintained. This can be accomplished in a variety of ways, including using semiconductor materials having low levels of oxygen contained therein to begin with, processing these materials in a manner that minimizes the uptake of oxygen into the semiconductor lattice, and utilizing techniques that eliminate or reduce oxygen that may be present in the semiconductor. Such processes and techniques can include, for example, annealing the semiconductor material and any laser treated region to lower temperatures as compared to previous annealing procedures. Annealing processes are discussed more fully below.

Additionally, texture processing of the semiconductor material and/or any annealing process can be performed in a substantially oxygen-depleted environment

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in order to minimize the introduction of oxygen into the semiconductor. An oxygen-depleted or substantially oxygen-depleted environment can include a variety of environments. In one aspect, for example, the oxygen-depleted environment can be an environment whereby oxygen from the air or other sources has been replaced with a gas or other fluid containing little to no oxygen. In another aspect, processing can occur in a vacuum environment, and thus contain little to no oxygen. Additionally, oxygen-containing materials or materials that introduce oxygen into the semiconductor, such as, for example, quartz crucibles, can be avoided. As a practical matter, the term "oxygen-depleted environment" can be used to describe an environment with low levels of oxygen, provided a semiconductor material can be processed therein within the desired tolerances. Thus, environments having low oxygen, or little to no oxygen, are environments in which a semiconductor can be processed as a low-oxygen content semiconductor while maintaining oxygen levels within the tolerances of the present disclosure. In one aspect, an oxygen-depleted environment can be an oxygen-free environment. Further details regarding low-oxygen content semiconductor materials can be found in US Patent Application No. 12/771848, filed on April 30, 2010, which is incorporated herein by reference.

The semiconductor material can have varying levels of interstitial oxygen depending on the desired efficiency of the device. In some aspects, oxygen content may be of no concern, and thus any level of oxygen within the lattice is acceptable. In other aspects, a low oxygen content is desired. In one aspect a semiconductor material can have an oxygen content that is less than or equal to about 50 ppm atomic. In another aspect, a semiconductor material can have an oxygen content that is less than or equal to about 30 ppm atomic. In yet another aspect, the semiconductor material can have an oxygen content less than or equal to about 10 ppm atomic. In another aspect the semiconductor can have an oxygen content less than about 5 ppm atomic. In yet another aspect the semiconductor can have an oxygen content less than about 1 ppm atomic.

As has been described, the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device. The textured region can include surface features to increase the effective absorption length of the photosensitive pixel. The surface features can be cones, pyramids, pillars, protrusions, microlenses, quantum dots, inverted features and the like. Factors such

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as manipulating the feature sizes, dimensions, material type, dopant profiles, texture location, etc. can allow the diffusing region to be tunable for a specific wavelength. In one aspect, tuning the device can allow specific wavelengths or ranges of wavelengths to be absorbed. In another aspect, tuning the device can allow specific wavelengths or ranges of wavelengths to be reduced or eliminated via filtering.

Tuning can also be accomplished through the location of the texture region within the device, modifying the dopant profile(s) of regions within the device, dopant selection, and the like. Additionally, material composition near the textured region can create a wavelength specific photosensing pixel device. It should be noted that a wavelength specific photosensing pixel can differ from one pixel to the next, and can be incorporated into an imaging array. For example a 4 x 4 array can include a blue pixel, a green pixel, a red pixel, and infrared light absorbing pixel, or a blue pixel, two green pixels, and a red pixel.

Textured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared). Such internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor substrate. This increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.

The textured region can be formed by various techniques, including lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, additional material deposition, and the like. For example, pillar features can be incorporated into pixels by thinning or removing material from the backside of a FSI semiconductor substrate by using deep trench isolation and etching techniques. In one aspect material can be removed to a thickness of about 20 μm. Anisotropic etching can be used to produce a sloping backside pyramid structure, spherical, structure parabolic structure , a lens structure with reflectors, and the like. Such features on the backside of pillars will also serve to diffuse and reflect electromagnetic radiation.

In one aspect, the texturing process can be performed during the manufacture of the photosensitive device. In another aspect, the texturing process can be performed on a photosensitive device that has previously been made. For example, a CMOS, CCD, or other photosensitive element can be textured following manufacture. In this case, material layers may be removed from the photosensitive element to

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expose the semiconductor substrate or bulk material upon which a textured region may be formed.

One effective method of producing a textured region is through laser processing. Such laser processing allows discrete locations of the semiconductor substrate to be textured. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope. Laser treatment or processing can allow, among other things, enhanced absorption properties and thus increased electromagnetic radiation focusing and detection. The laser treated region can be associated with the surface nearest the impinging electromagnetic radiation, or the laser treated surface can be associated with a surface opposite in relation to impinging electromagnetic radiation, thereby allowing the radiation to pass through the semiconductor material before it hits the laser treated region.

In one aspect, for example, a target region of the semiconductor material can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Patents 7,057,256, 7,354,792 and 7,442,629, which are incorporated herein by reference in their entireties. Briefly, a surface of a semiconductor material is irradiated with laser radiation to form a textured or surface modified region. Such laser processing can occur with or without a dopant material. In those aspects whereby a dopant is used, the laser can be directed through a dopant carrier and onto the semiconductor surface. In this way, dopant from the dopant carrier is introduced into the target region of the semiconductor material. Such a region incorporated into a semiconductor material can have various benefits in accordance with aspects of the present disclosure. For example, the target region typically has a textured surface that increases the surface area of the laser treated region and increases the probability of radiation absorption via the mechanisms described herein. In one aspect, such a target region is a substantially textured surface including micron-sized and/or nano-sized surface features that have been generated by the laser texturing. In another aspect, irradiating the surface of semiconductor material includes exposing the laser radiation to a dopant such that irradiation incorporates the dopant into the semiconductor. Various dopant materials are known in the art, and are discussed in more detail herein.

Thus the surface of the semiconductor material is chemically and/or structurally altered by the laser treatment, which may, in some aspects, result in the

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formation of surface features appearing as microstructures or patterned areas on the surface and, if a dopant is used, the incorporation of such dopants into the semiconductor material. In some aspects, the features or microstructures can be on the order of 50 nm to 20 μm in size and can assist in the absorption of electromagnetic radiation. In other words, the textured surface can increase the probability of incident radiation being absorbed by the semiconductor material.

The type of laser radiation used to surface modify a semiconductor material can vary depending on the material and the intended modification. Any laser radiation known in the art can be used with the devices and methods of the present disclosure. There are a number of laser characteristics, however, that can affect the surface modification process and/or the resulting product including, but not limited to the wavelength of the laser radiation, pulse width, pulse fluence, pulse frequency, polarization, laser propagation direction relative to the semiconductor material, etc. In one aspect, a laser can be configured to provide pulsatile lasing of a semiconductor material. A short-pulsed laser is one capable of producing femtosecond, picosecond and/or nanosecond pulse durations. Laser pulses can have a central wavelength in a range of about from about 10 nm to about 8 μm, and more specifically from about 200 nm to about 1200 nm. The pulse width of the laser radiation can be in a range of from about tens of femtoseconds to about hundreds of nanoseconds. In one aspect, laser pulse widths can be in the range of from about 50 femtoseconds to about 50 picoseconds. In another aspect, laser pulse widths can be in the range of from about 50 picoseconds to 100 nanoseconds. In another aspect, laser pulse widths are in the range of from about 50 to 500 femtoseconds.

The number of laser pulses irradiating a target region can be in a range of from about 1 to about 2000. In one aspect, the number of laser pulses irradiating a semiconductor target region can be from about 2 to about 1000. Further, the repetition rate or frequency of the pulses can be selected to be in a range of from about 10 Hz to about 10 μHz, or in a range of from about 1 kHz to about 1 MHz, or in a range from about 10 Hz to about 1 kHz. Moreover, the fluence of each laser pulse can be in a range of from about 1 kJ/m^2 to about 20 kJ/m^2, or in a range of from about 3 kJ/m^2 to about 8 kJ/m^2.

A variety of dopant materials are contemplated, and any such material that can be used in the laser treatment process to surface modify a semiconductor material according to aspects of the present disclosure is considered to be within the present

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scope. It should be noted that the particular dopant utilized can vary depending on the semiconductor material being laser treated, as well as the intended use of the resulting semiconductor material. For example, the selection of potential dopants may differ depending on whether or not tuning of the photosensitive device is desired.

A dopant can be either electron donating or hole donating. In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof. It should be noted that the scope of dopant materials should include, not only the dopant materials themselves, but also materials in forms that deliver such dopants (i.e. dopant carriers). For example, S dopant materials includes not only S, but also any material capable being used to dope S into the target region, such as, for example, H_2S, SF_6, SO_2, and the like, including combinations thereof. In one specific aspect, the dopant can be S. Sulfur can be present at an ion dosage level of between about 5×10^{14} and about 1×10^{16} ions/cm^2. Non-limiting examples of fluorine-containing compounds can include ClF_3, PF_5, F_2 SF_6, BF_3, GeF_4, WF_6, SiF_4, HF, CF_4, CHF_3, CH_2F_2, CH_3F, C_2F_6, C_2HF_5, C_3F_8, C_4F_8, NF_3, and the like, including combinations thereof. Non-limiting examples of boron-containing compounds can include $B(CH_3)_3$, BF_3, BCl_3, BN, $C_2B_{10}H_{12}$, borosilica, B_2H_6, and the like, including combinations thereof. Non-limiting examples of phosphorous-containing compounds can include PF_5, PH_3, and the like, including combinations thereof. Non-limiting examples of chlorine-containing compounds can include Cl_2, SiH_2Cl_2, HCl, $SiCl_4$, and the like, including combinations thereof. Dopants can also include arsenic-containing compounds such as AsH_3 and the like, as well as antimony-containing compounds. Additionally, dopant materials can include mixtures or combinations across dopant groups, i.e. a sulfur-containing compound mixed with a chlorine-containing compound. In one aspect, the dopant material can have a density that is greater than air. In one specific aspect, the dopant material can include Se, H_2S, SF_6, or mixtures thereof. In yet another specific aspect, the dopant can be SF_6 and can have a predetermined concentration range of about 5.0×10^{-8} mol/cm^3 to about 5.0×10^{-4} mol/cm^3. SF_6 gas is a good carrier for the incorporation of sulfur into the semiconductor material via a laser process without significant adverse effects on the semiconductor material. Additionally, it is noted that dopants can also be liquid solutions of n-type or p-type dopant materials dissolved in a solution such as water, alcohol, or an acid or basic solution. Dopants can also be solid materials applied as a powder or as a suspension dried onto the wafer.

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The semiconductor substrate can be annealed for a variety of reasons, including dopant activation, semiconductor material damage repair, and the like. In those aspects including a laser textured region, the semiconductor material can be annealed prior to laser treatment, following laser treatment, during laser treatment, or both prior to and following laser treatment. Annealing can enhance the semiconductive properties of the device, including increasing the photoresponse properties of the semiconductor materials. Additionally, annealing can reduce damage done by the lasing process. Although any known anneal can be beneficial and would be considered to be within the present scope, annealing at lower temperatures can be particularly useful. Such a "low temperature" anneal can greatly enhance the photoconductive gain and external quantum efficiency of devices utilizing such materials. In one aspect, for example, the semiconductor material can be annealed to a temperature of from about 300° C to about 1100 C°. In another aspect, the semiconductor material can be annealed to a temperature of from about 500° C to about 900° C. In yet another aspect, the semiconductor material can be annealed to a temperature of from about 700° C to about 800° C. In a further aspect, the semiconductor material can be annealed to a temperature that is less than or equal to about 850° C.

The duration of the annealing procedure can vary according to the specific type of anneal being performed, as well as according to the materials being used. For example, rapid annealing processes can be used, and as such, the duration of the anneal may be shorter as compared to other techniques. Various rapid thermal anneal techniques are known, all of which should be considered to be within the present scope. In one aspect, the semiconductor material can be annealed by a rapid annealing process for a duration of greater than or equal to about 1 μs. In another aspect, the duration of the rapid annealing process can be from about 1 μs to about 1 ms. As another example, a baking or furnace anneal process can be used having durations that may be longer compared to a rapid anneal. In one aspect, for example, the semiconductor material can be annealed by a baking anneal process for a duration of greater than or equal to about 1 ms to several hours. As has been described, if low oxygen content semiconductor materials are used it may be beneficial to anneal such materials in a substantially oxygen-depleted environment.

As has been described, annealing can help reduce defects inherent to the semiconductor substrate and otherwise reduce electron/hole recombination. In other

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words, the annealing can help create electron states that effectively reduce the undesirable recombination processes. Annealing the semiconductor material may also improve the responsivity or photoconductive gain of the device. Photoconductive devices can have dopants, impurities, or defects that can introduce energy levels that can trap carriers. Trapping carriers and reducing recombination of photocarriers can lead to an increase in photoconductive gain of the device. The relationship of photoconductive gain and trapping time can be represented by Equation (I):

$$\text{Gain} = \tau_L/\tau_t \qquad \text{(I)}$$

where "τ_L" is the lifetime of an excess carrier and "τ_t" is the transit time of the carriers across the device. It is understood that the lifetime of an excess carrier can be increased by trapping a carrier species and reducing the recombination rate. An increase in gain can be achieved by trapping centers in the semiconductor that have millisecond trapping times at room temperature and short transit times in thinned lightly doped wafers. These trapping locations can decrease the recombination of carriers and therefore improve or increase the photoconductive gain of the device by allowing more electrons to traverse the different regions without being recombined.

Turning to FIG. 2, a reflecting layer 20 can be coupled to the semiconductor substrate 12. The reflecting layer can be coupled to any side or portion of the semiconductor substrate in order to reflect electromagnetic radiation back into the device. Accordingly, in one aspect the reflecting layer can be located on the semiconductor substrate opposite the incoming electromagnetic radiation. Thus, as is shown in FIG. 2, electromagnetic radiation passing though the semiconductor substrate and the textured region 16 can be reflected back into the semiconductor substrate. Additionally, a passivation layer 22 can be coupled to the semiconductor substrate. The passivation layer is shown coupled to the side of the semiconductor substrate facing the incoming electromagnetic radiation, however a passivation layer can be located anywhere on the device and still be within the present scope.

As has been described, location of the textured region can be used to provide enhancement and/or filtering of the incoming electromagnetic radiation. For example, a textured region located at the point of entry of the electromagnetic radiation into the photosensitive device tends to bend the electromagnetic radiation, particularly the blue wavelengths. Accordingly, one level of tuning can be accomplished by locating

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the textured region on the surface adjacent the incident electromagnetic radiation to purposely effectuate the filtering of blue wavelengths. Additionally, absorption of particular wavelengths of electromagnetic radiation occurs at different depths in the semiconductor layer and/or textured region. By increasing the absorption to green wavelengths, for example, the electrical signal as a result of green wavelengths can be increased in a diode or pixel. Certain traditional 4 pixel imagers have one red, one blue, and two green pixels, with the greater number of green pixels to account for increased sensitivity of the human eye to green colors. Thus in one aspect, a 4 pixel imager can have one blue, one red, and one green pixel having an increased green wavelength absorption. The fourth pixel can be used for an IR or other wavelength selective pixel depending on the desired application of the imager.

FIG. 3 shows a photosensitive device having textured regions 30 located on the sides of the semiconductor substrate 12. Such a configuration allows electromagnetic radiation normally exiting through the sides of the device to be further defused and absorbed within semiconductor substrate. The textured region(s) can be located on one or more sides to facilitate the enhanced absorption.

FIG. 4 shows a photosensitive device having a textured region 40 having a nonparallel surface with respect to the semiconductor substrate 12. Thus the overall configuration of the textured region can be designed to further enhance absorption and/or selectively tune the device. As has been described, the nonparallel surface can have a variety of configurations, such as, without limitation, nonparallel slope, a pyramid, an inverted pyramid, a concave shape, a convex shape, and the like. In some cases the configuration of the textured region can function to direct or focus electromagnetic radiation into the semiconductor substrate, and in other cases the configuration of the textured region can function to direct or focus electromagnetic radiation away from the semiconductor substrate.

As is shown in FIG. 5, a lens 50 can be coupled to the semiconductor substrate 12 on a side facing incoming electromagnetic radiation. Thus the lens can focus the electromagnetic radiation into the semiconductor substrate. In those aspects having circuitry or other structures disposed on the incoming electromagnetic radiation surface, the lens can further focus light around such structures, thereby reducing optical scattering and noise.

As is shown in FIG. 6, a textured region 60 is located on the semiconductor substrate 12 adjacent to the multiple doped regions 14, 16. The textured region can be

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associated with at least one of the doped regions as is shown, or the textured region can be distinct from the doped regions (not shown). Electromagnetic radiation can enter the photosensitive device at the side adjacent the doped regions, or alternatively at the side opposite the doped regions.

FIGs. 7-11 show various steps in the manufacture of a photosensitive pixel according to aspects of the present disclosure. FIG. 7 shows a cross-section of a front side illumination (FSI) photosensitive pixel device. The photosensitive pixel device can include a semiconductor substrate 72, and can be referred to as bulk semiconductor material. The semiconductor substrate includes at least one doped region 74 that can be doped with an electron donating or hole donating species to cause the region to become more positive or negative in polarity as compared to the semiconductor substrate. In one aspect, for example, the doped region can be p doped. In another aspect the doped region can be n doped. A highly doped region 76 can be formed on or near the doped region to create a pinned diode. In one example, the semiconductor substrate can be negative in polarity, and the doped region and the highly doped region can be doped with p+ and n- dopants respectively. In some aspects, variations of n(--), n(-), n(+), n(++), p(--), p(-), p(+), or p(++) type doping of the regions can be used. It should be noted that in one aspect the highly doped region can be the textured region. In other words, textured surface features can be formed on or in the highly doped region.

The device of FIG. 7 can further include various metal regions 78, at least one via 80, a passivation layer 82, trench isolation 84, and an electrical transfer element 86. Trench isolation elements can maintain pixel to pixel uniformity by reducing optical and electrical crosstalk. The trench isolation can be shallow (FIG. 7) or deep (FIG. 12) trench isolation. The trench isolation can include various materials, including, without limitation, dielectric materials, reflective materials, conductive materials, light diffusing features, and the like. These trench isolation regions can be configured to reflect incident light until it is absorbed, thereby increase the effective absorption length of the device.

As is shown in FIG. 8, a carrier substrate or carrier wafer 88 can be coupled to the photosensing pixel. In one aspect, the carrier substrate can be disposed on the passivation layer 82, although the carrier substrate can be disposed on any surface of the device. In one aspect, for example, the carrier substrate can be disposed on the semiconductor substrate (not shown). The carrier substrate can be coupled to the

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photosensing pixel by various techniques, and any such coupling mechanism is within the present scope. In one aspect, for example, the coupling can occur by way of a bonding layer or adhesive layer disposed on the device, for example, on the passivation layer. The support substrate can provide support to the semiconductor device both during and after manufacture, depending on whether or not the support is removed. The carrier substrate can be made of a semiconductor material that is the same or similar to the bulk semiconductor material, or it can be made of a different material.

As is shown in FIG. 9, a textured region 90 is coupled to the semiconductor substrate 72 opposite the doped regions 74,76. Thus light entering from the direction of the doped regions passes through the semiconductor substrate prior to contacting the textured region. The textured region can be disposed across an entire surface of the semiconductor substrate, as is shown in FIG. 9, or it can be disposed on one or more discrete regions (not shown).

As is shown in FIG. 10, an additional carrier support substrate 100 can be coupled to the device on an opposing side from the carrier support substrate 88. The additional carrier support substrate can be utilized for a variety of purposes, including providing additional support to the device, facilitating the removal of the first carrier support substrate, and the like. A reflective layer 102 can be disposed between the textured region 90 and the carrier support substrate. Thus the reflective layer can reflect electromagnetic radiation that passes through the textured region back toward the semiconductor substrate 72, thus reducing optical loss and backscattering. Thus, in some aspects a reflective layer can increase the quantum efficiency of the device. The reflective layer material can be any reflective material that can be incorporated into such a device. Nonlimiting examples can include materials such as silver, aluminum, and the like.

As is shown in FIG. 11, the carrier support substrate can be removed to expose the passivation layer 82 or any other material layer that was previously covered by the carrier support substrate. The additional carrier substrate 100 can be maintained in the device, removed from the device, or thinned to reduce the thickness of the substrate depending on the intended use of the device. The removal of material from the device, including the carrier support substrate and the additional carrier substrate, can be accomplished by a variety of methods including, without limitation, etching, chemical mechanical polishing, ion implanting (i.e. smart cut), and the like.

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Various types of trench isolation are contemplated, and any such isolation is considered to be within the present scope. As has been described, trench isolation can be shallow (FIG. 7, 84) or deep (FIG. 12, 120) trench isolation. The trench isolation can also include depths between shallow and deep, depending on the device design. Trench isolation can include dielectric materials, reflective materials, conductive materials, and combinations thereof, including textured regions and other light diffusing features. Thus the trench isolation layer can be configured to reflect incident electromagnetic radiation, in some cases until it is absorbed, thereby increasing the effective absorption length of the device. Additionally, in some aspects pillar features can be incorporated into pixels by thinning or removing material from the semiconductor substrate using deep trench isolation and etching techniques. As is shown in FIG. 13, the textured region 130 can have a nonparallel surface with respect to the semiconductor substrate 72 as has been described. This nonparallel morphology, when included with the deep trench isolation 120, can effectively focus electromagnetic radiation into the semiconductor substrate from multiple sides.

It is also contemplated, that a non-bulk material can be formed or disposed near a doped region in the device. The addition of the non-bulk material can allow for electromagnetic radiation diffusing features to be formed on or in the non-bulk material. A metal layer defining an aperture can also be included in one aspect of the present disclosure. The metal layer can be formed near the doped regions and can have a light entering region that defines an aperture. This light entering region can also include an antireflecting material.

Fig. 14 shows a photosensitive imager comprising two photosensitive pixels 140. Each photosensitive pixel includes a boundary region 142 that can include metal circuitry and a textured region 144. Each photosensitive pixel can include at least one transistor 146 or other electrical transfer element. Additional read out and circuitry elements 148 can be utilized and shared by both photosensitive pixels.

Turning to FIG. 15, a backside illuminated (BSI) photosensitive pixel according to one aspect present disclosure is provided. A lens 150 and an anti-reflective coating 152 are disposed on the backside of the pixel following thinning and trench isolation. A color filter 154 can be optically coupled to the lens to allow specific wavelengths filtering of the electromagnetic radiation. A textured region 156 can be coupled to the semiconductor substrate 72 opposite the lens in order to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes

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through to the front side of the pixel. Thus the electromagnetic radiation can be focused within the semiconductor substrate to the combined action of the textured region and the trench isolation 120

Fig. 16 shows a front side illuminated (FSI) imager according to another aspect of the present disclosure. A lens 160 and an antireflecting passivation layer on 62 are coupled to the front side of the pixel. A textured region 90 and a reflecting layer 102 are coupled to the semiconductor substrate 72 opposite the lens to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes through the semiconductor substrate. An aperture 164 formed in a metal or other reflective material layer 166 can increase the effectiveness of the optical cavity. Thus the lens focuses electromagnetic radiation through the aperture.

In other aspects of the present disclosure, various methods of making photosensitive diodes, pixels, and imagers, are contemplated. In one aspect, as is shown in FIG. 17, a method of making a photosensitive imager device can include forming a textured region on a semiconductor substrate having multiple doped regions forming a least one junction, wherein the textured region is formed in a position to interact with electromagnetic radiation 170. The method also includes coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction 172. In one aspect, multiple pixels can be associated together to form an imager. A passivation layer can also be disposed on the photosensitive imager device to protect and/or reduce the dark current of the device.

In another aspect of the present disclosure, a method for making a photosensitive diode is provided. Such a method can include forming at least one cathode and at least one anode on a surface of a semiconductor substrate, coupling a textured region to the semiconductor substrate, and coupling a support substrate to the semiconductor substrate. The textured region can be located adjacent to the anode and cathode, opposite the anode and cathode, or both adjacent and opposite the anode and cathode. An electrical transfer on the can be electrically coupled to at least one of the anode and cathode to form a photosensitive pixel. In another aspect, the semiconductor substrate can be thinned to improve the response rate and/or speed of the device. A passivation layer can also be disposed on the photosensitive diode to protect and/or reduce the dark current of the device. An additional support substrate can be attached to the device to provide additional support. In one aspect, the

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additional support substrate can be located on the opposite side of the photosensitive diode from the support substrate. The support substrate can subsequently be removed to allow for further processing.

Of course, it is to be understood that the above-described arrangements are only illustrative of the application of the principles of the present disclosure. Numerous modifications and alternative arrangements may be devised by those skilled in the art without departing from the spirit and scope of the present disclosure and the appended claims are intended to cover such modifications and arrangements. Thus, while the present disclosure has been described above with particularity and detail in connection with what is presently deemed to be the most practical embodiments of the disclosure, it will be apparent to those of ordinary skill in the art that numerous modifications, including, but not limited to, variations in size, materials, shape, form, function and manner of operation, assembly and use may be made without departing from the principles and concepts set forth herein.

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CLAIMS

What is claimed is:

1. A photosensitive imager device, comprising:

a semiconductor substrate having multiple doped regions forming a least one junction;

a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation; and

an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction.

2. The device of claim 1, wherein the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation.

3. The device of claim 1, wherein interacting with electromagnetic radiation further includes increasing the semiconductor substrate's effective absorption length as compared to a semiconductor substrate lacking a textured region.

4. The device of claim 1, wherein the transfer element is selected from the group consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.

5. The device of claim 1, further comprising a reflective layer coupled to the semiconductor substrate and positioned to maintain the electromagnetic radiation in the semiconductor substrate.

6. The device of claim 1, wherein the textured region is positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions.

7. The device of claim 6, wherein the textured region has a surface morphology operable to direct electromagnetic radiation into or out of the semiconductor substrate.

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8. The device of claim 7, wherein the surface morphology of the textured region relative to the semiconductor substrate is a member selected from the group consisting of sloping, pyramidal, inverted pyramidal, spherical, parabolic, asymmetric, symmetric, and combinations thereof.

9. The device of claim 1, wherein the textured region is positioned on a surface of the semiconductor substrate that is adjacent the multiple doped regions.

10. The device of claim 9, further comprising an additional textured region positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions.

11. The device of claim 1, wherein the textured region is coupled directly to at least one of the multiple doped regions.

12. The device of claim 1, wherein the textured region includes surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof.

13. The device of claim 12, wherein surface features include a member selected from the group consisting of cones, pillars, pyramids, micolenses, quantum dots, inverted features, and combinations thereof.

14. The device of claim 1, wherein the textured region has been formed by a process selected from the group consisting of lazing, chemical etching, nanoimprinting, material deposition, and combinations thereof.

15. The device of claim 1, further comprising a lens optically coupled to the semiconductor substrate and positioned to focus incident electromagnetic radiation into the semiconductor substrate.

16. A photosensitive imager array, comprising at least two photosensitive imager devices of claim 1.

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17. The array of claim 16, further comprising at least one trench isolation positioned between the at least two photosensitive imager device.

18. A method of making a photosensitive imager device, comprising:

forming a textured region on a semiconductor substrate, wherein the semiconductor substrate has multiple doped regions forming a least one junction, and wherein the textured region is formed in a position to interact with electromagnetic radiation; and

coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction .

19. The method of claim 18, wherein forming the textured region is by a process selected from the group consisting of lazing, chemical etching, nanoimprinting, material deposition, and combinations thereof.

20. The method of claim 18, wherein forming the textured region includes irradiating a target region with laser radiation to form surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof.

21. The method of claim 20, wherein irradiating the target region includes exposing the laser radiation to a dopant such that the irradiation incorporates the dopant into the textured region.

22. The method of claim 20, wherein the irradiation is performed using a pulsed laser including a member selected from the group consisting of a femtosecond laser, a picosecond laser, a nanosecond laser, and combinations thereof.

23. The method of claim 18, further comprising tuning an electrical response of the photosensitive imager device.

24. The method of claim 23, wherein tuning includes forming surface features to have dimensions that selectively diffuse or selectively absorb a desired wavelength of electromagnetic radiation.

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25. The method of claim 23, wherein tuning is accomplished through a factor selected from the group consisting of placement of the textured region, material type of the textured region, thickness of the textured region, dopant type of the textured region, doping profile of the texture region, doping profile of the semiconductor substrate, thickness of the substrate, and combinations thereof.

26. The method of claim 18, wherein the transfer element is selected from the group consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.

27. The method of claim 18, further comprising annealing the semiconductor substrate to a temperature of from about 300° C to about 1100° C.

28. A photosensitive imager device, comprising:

a semiconductor substrate having multiple doped regions forming a least one junction;

a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation; and

at least 4 transistors coupled to the semiconductor substrate and with at least one of the transistors electrically coupled to the at least one junction.

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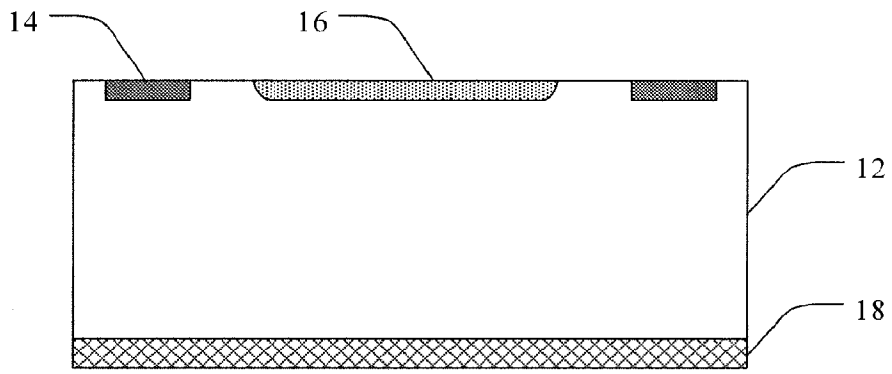

FIG. 1

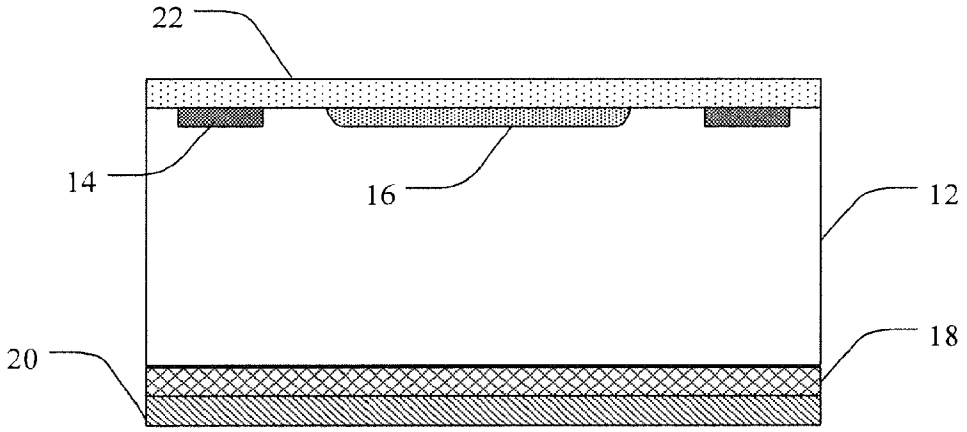

FIG. 2

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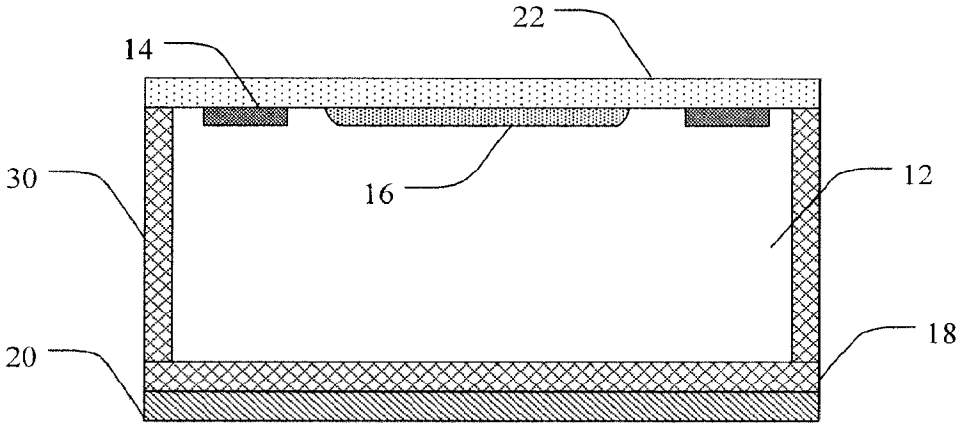

FIG. 3

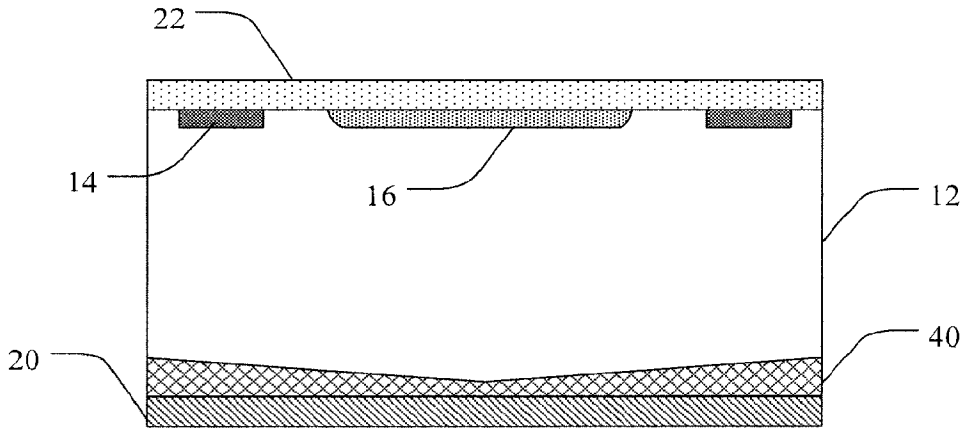

FIG. 4

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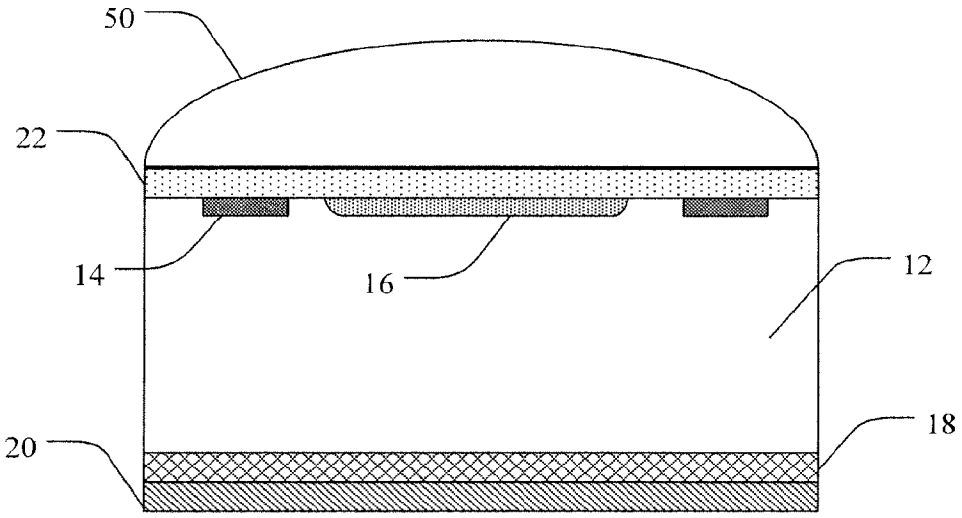

FIG. 5

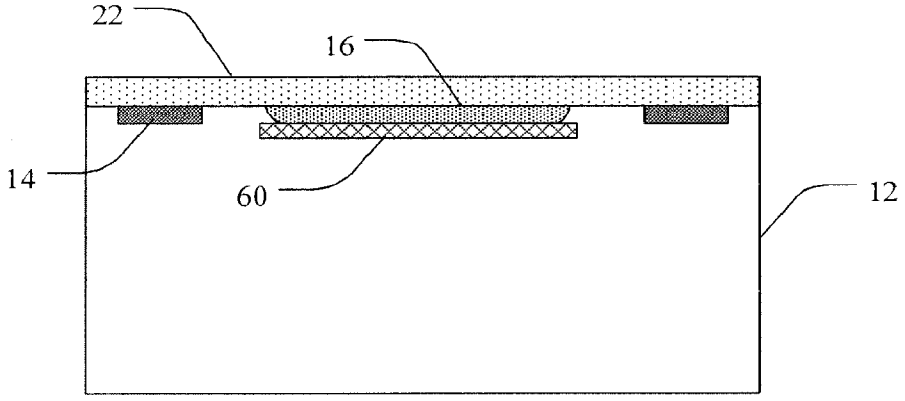

FIG. 6

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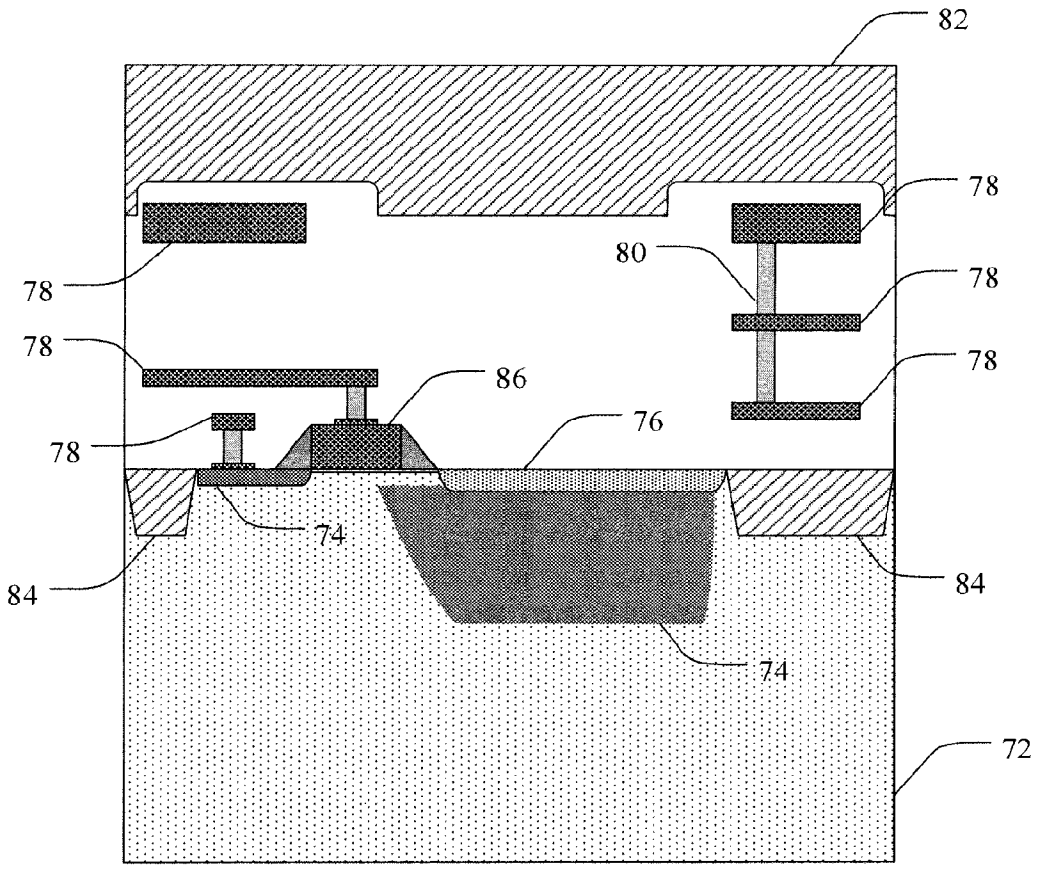

FIG. 7

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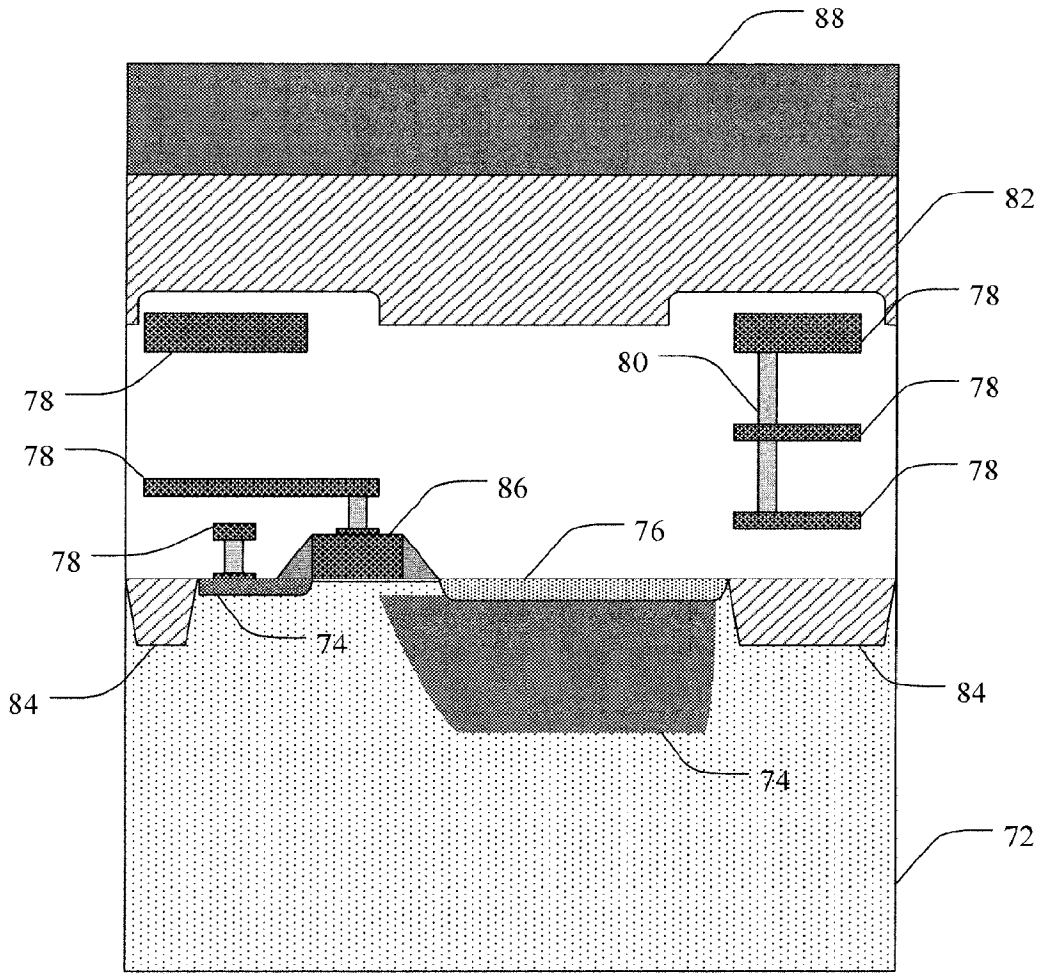

FIG. 8

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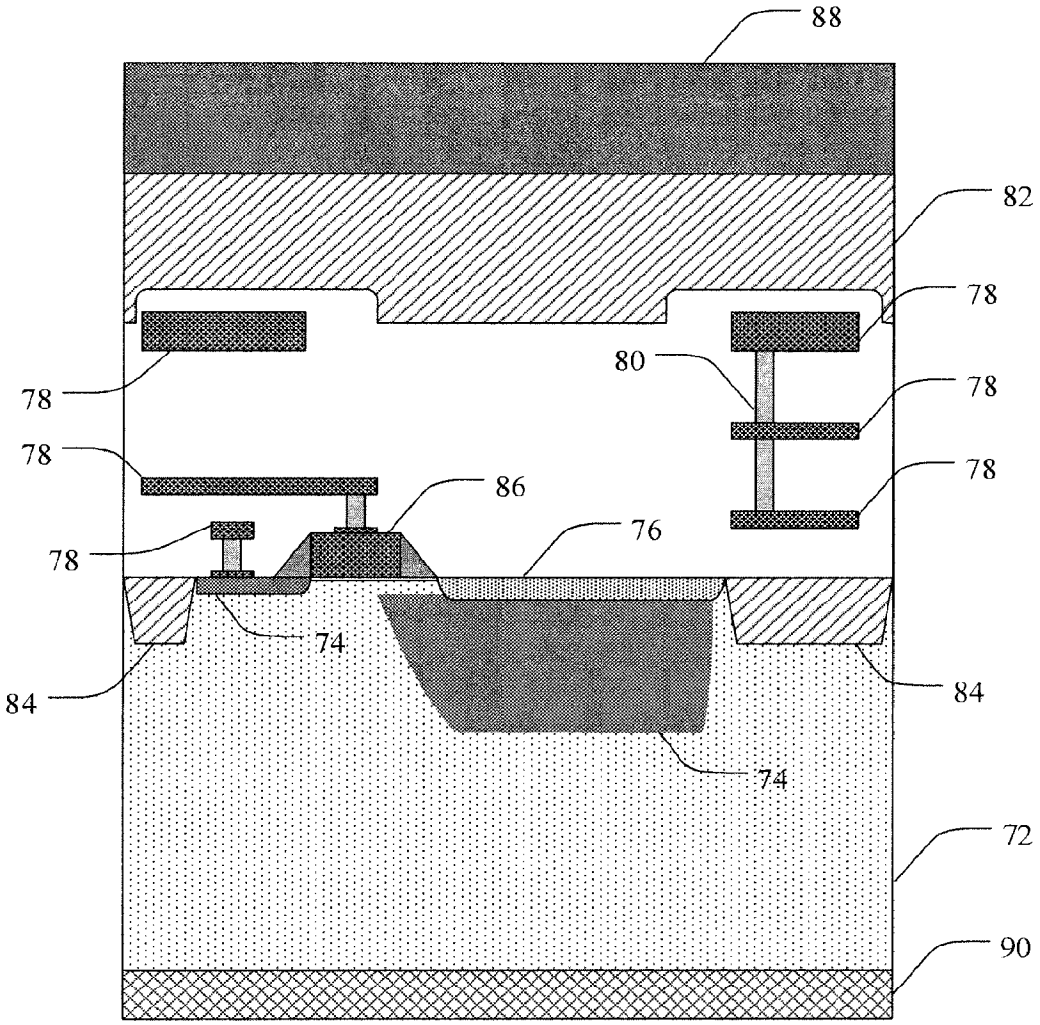

FIG. 9

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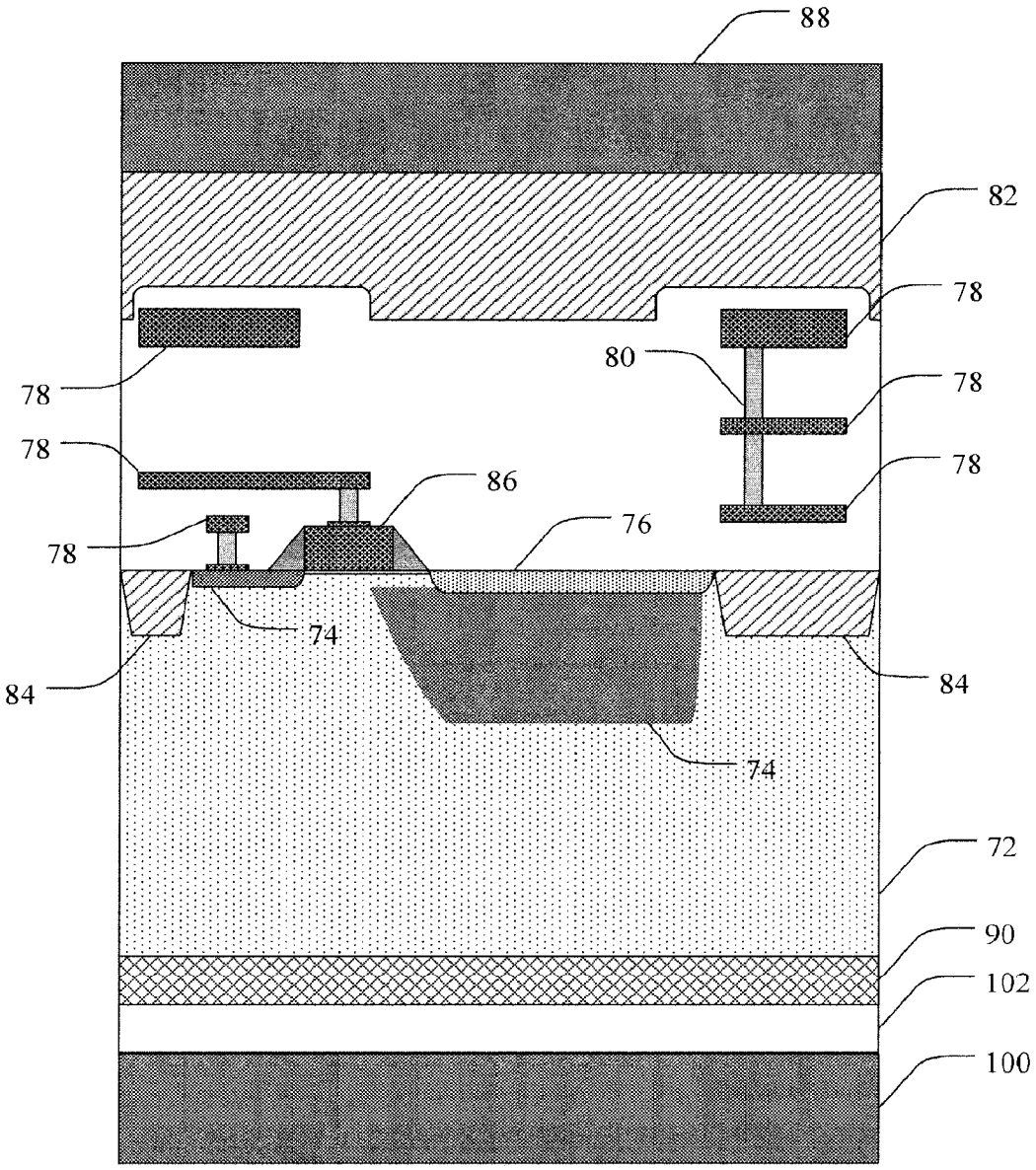

FIG. 10

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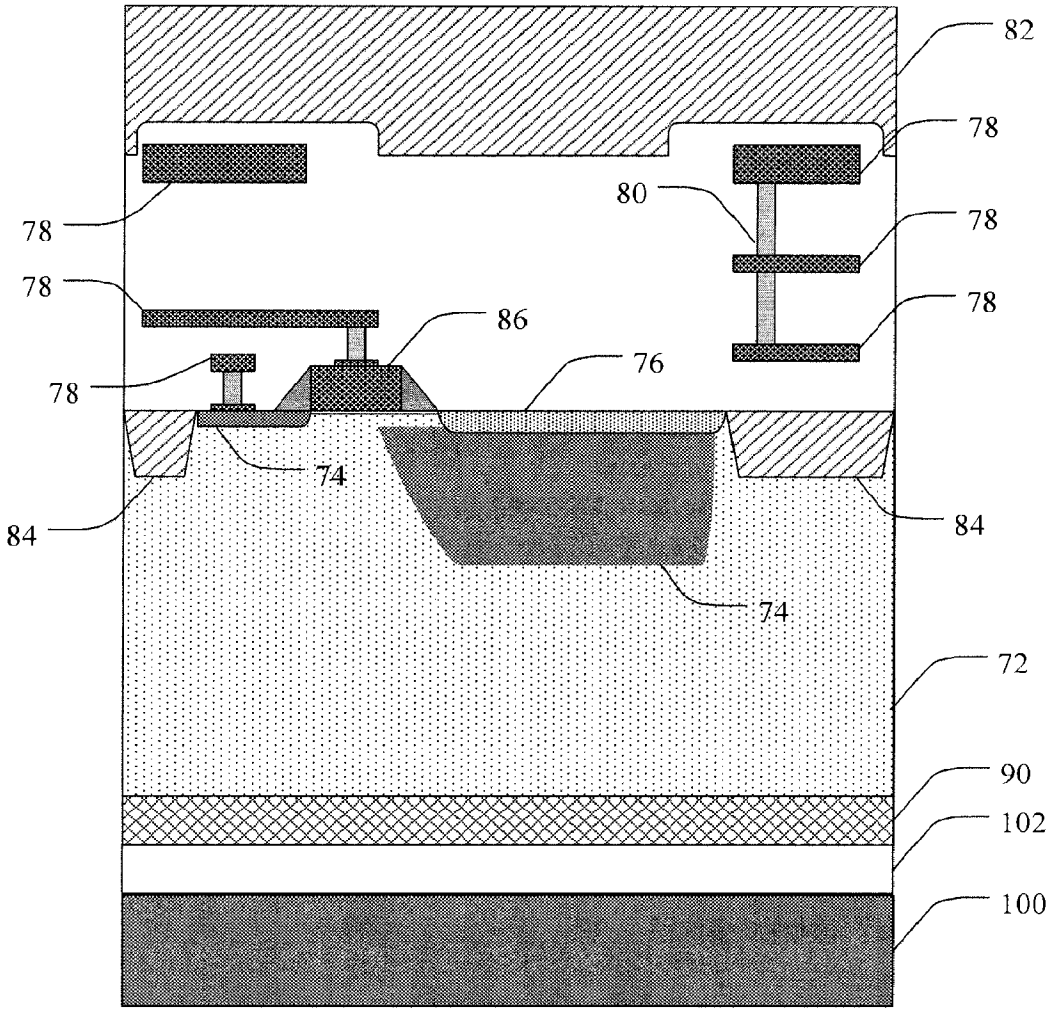

FIG. 11

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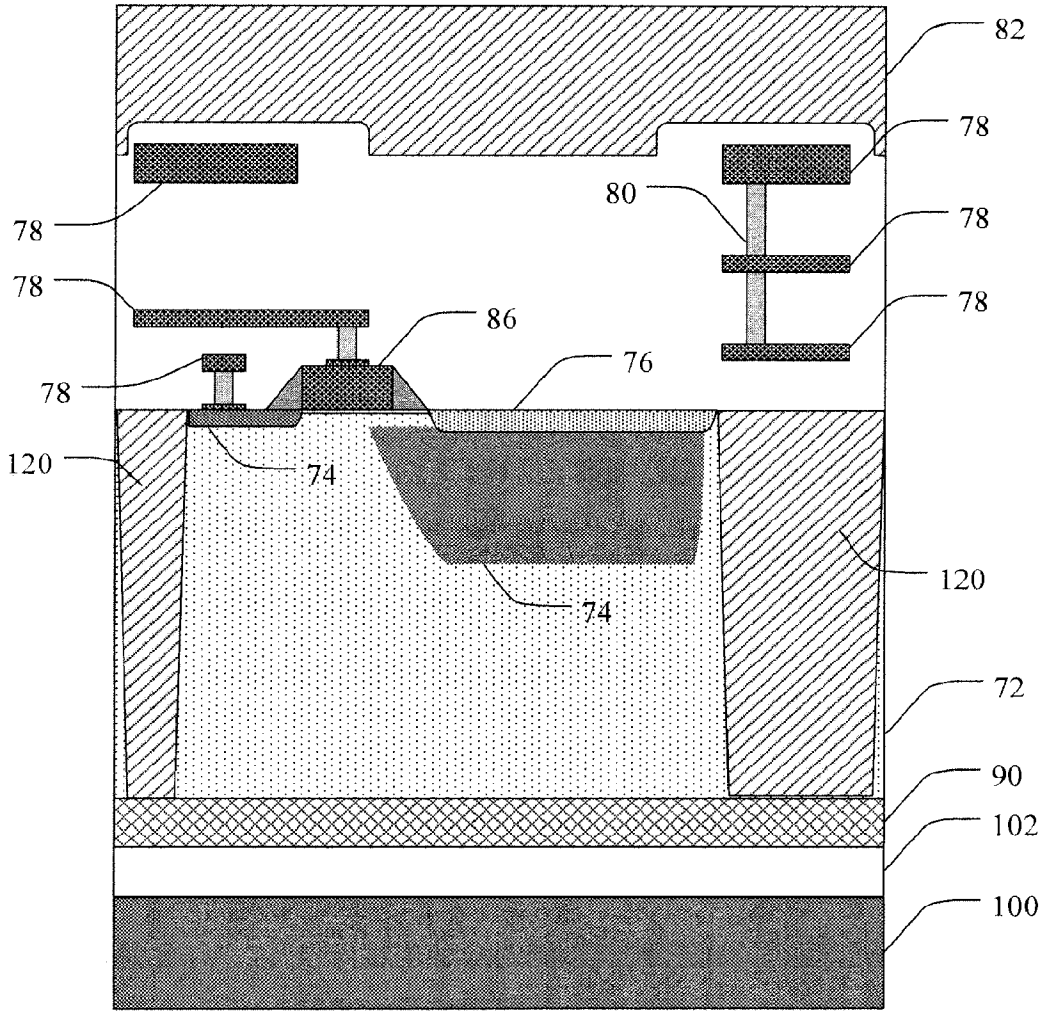

FIG. 12

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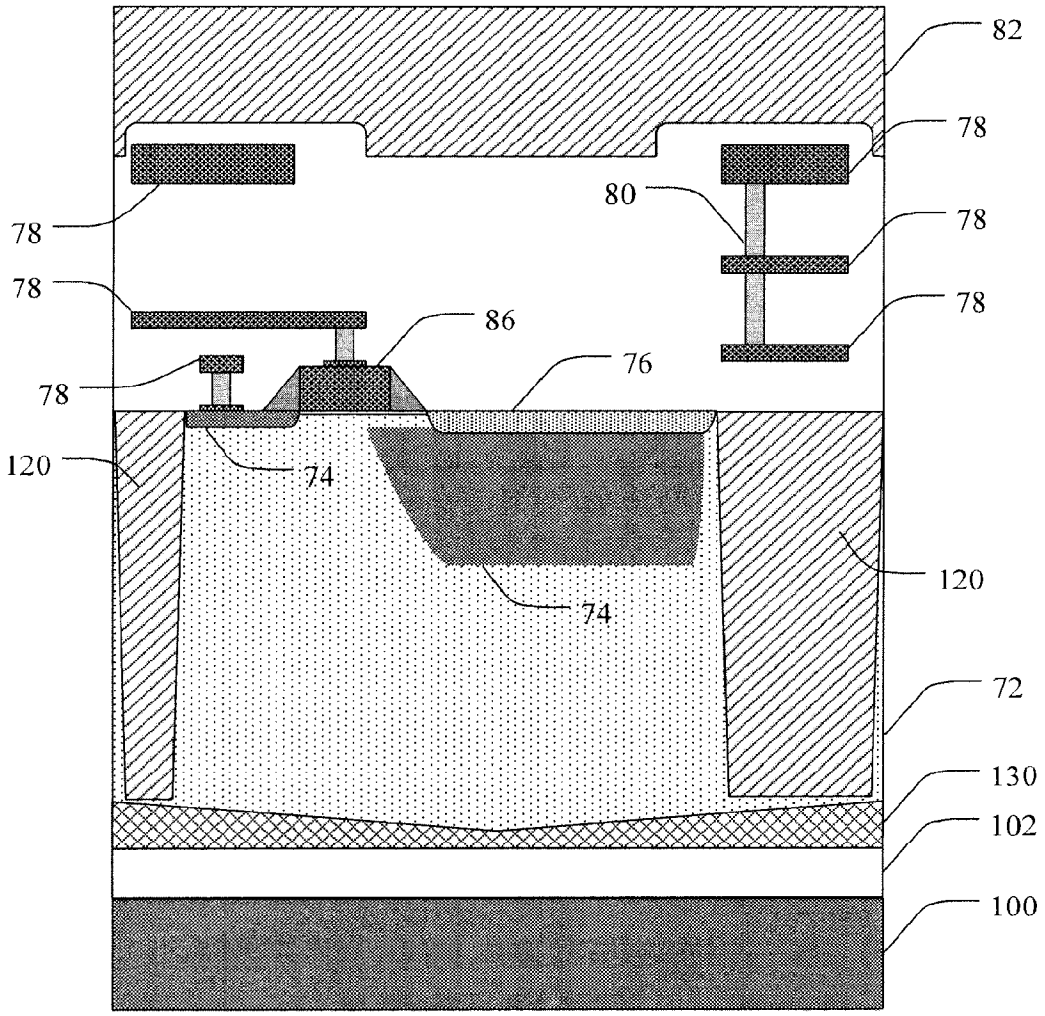

FIG. 13

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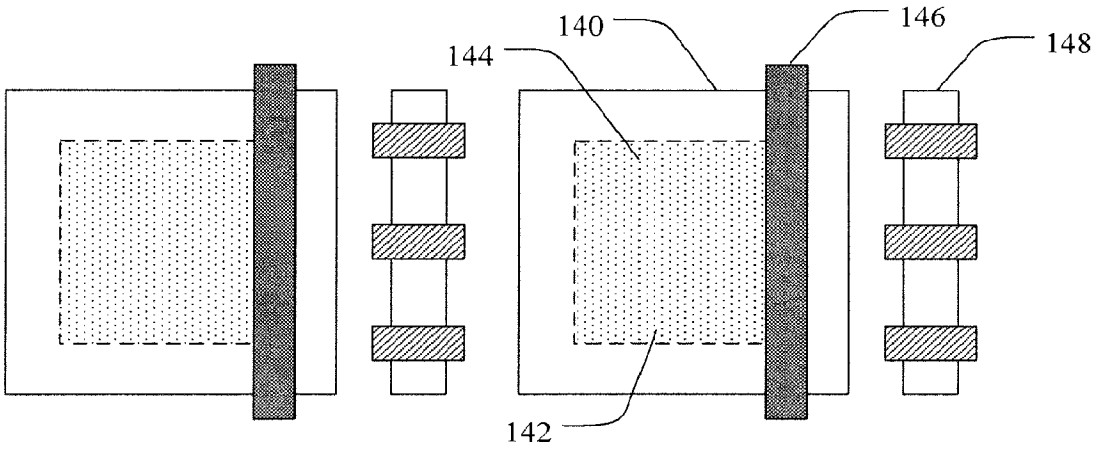

FIG. 14

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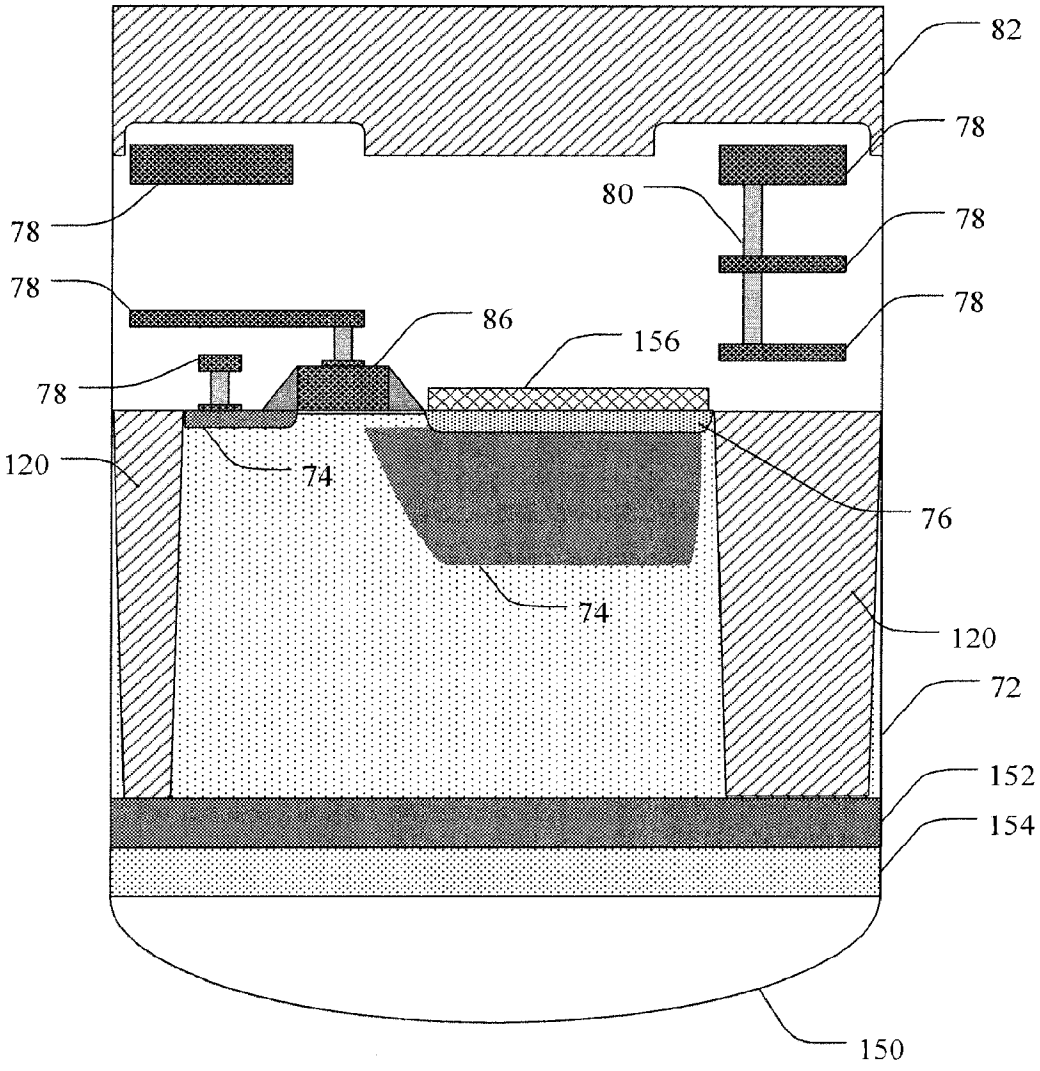

FIG. 15

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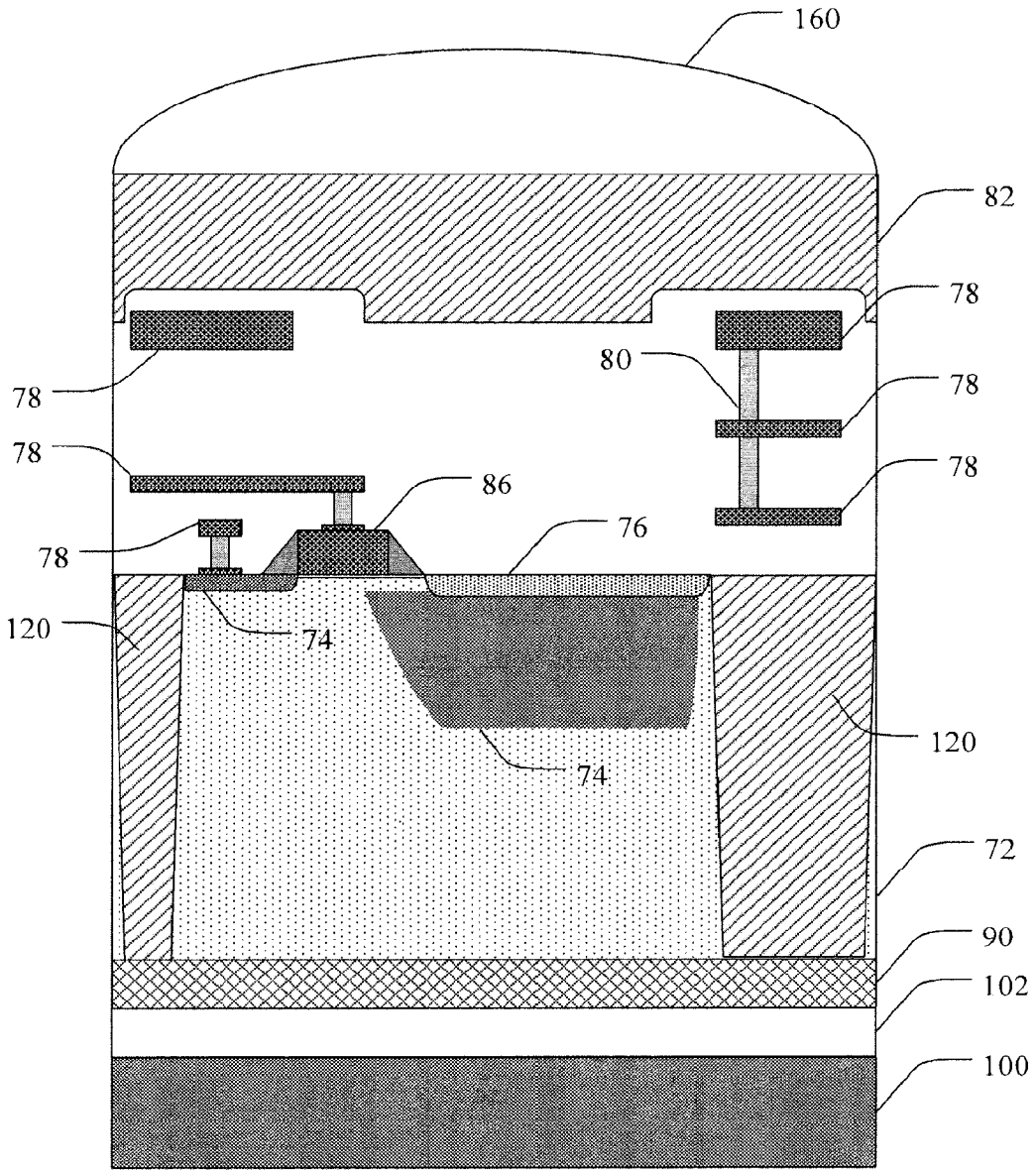

FIG. 16

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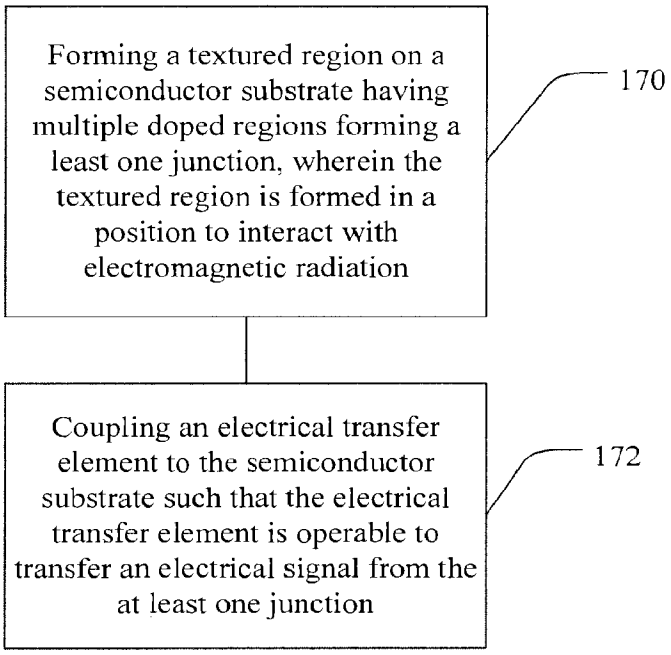

FIG. 17

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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 September 2011 (29.09.2011)

PCT

(10) International Publication Number
WO 2011/119618 A2

(51) International Patent Classification:
H01L 31/101 (2006.01) *H01L 31/0236* (2006.01)

(21) International Application Number:
PCT/US2011/029447

(22) International Filing Date:
22 March 2011 (22.03.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/317,147 24 March 2010 (24.03.2010) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

(54) **Title**: DEVICES HAVING ENHANCED ELECTROMAGNETIC RADIATION DETECTION AND ASSOCIATED METHODS

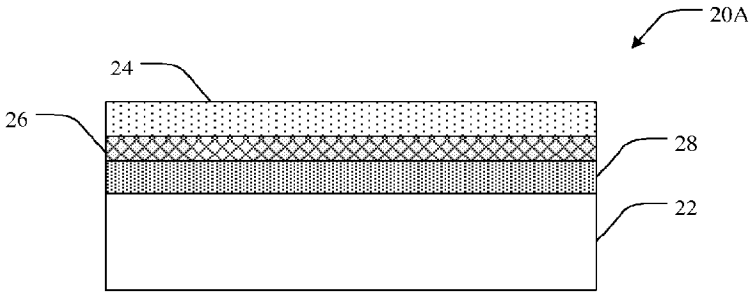

FIG. 2A

(57) **Abstract**: Photosensitive semiconductor devices and associated methods are provided. In one aspect, a semiconductor device can include a semiconductor substrate and a semiconductor layer coupled to the semiconductor substrate, where the semiconductor layer has a device surface opposite the semiconductor substrate. The device also includes at least one textured region coupled between the semiconductor substrate and the semiconductor layer. In another aspect, the device further includes at least one dielectric layer coupled between the semiconductor substrate and the semiconductor layer.

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DEVICES HAVING ENHANCED ELECTROMAGNETIC RADIATION DETECTION AND ASSOCIATED METHODS

PRIORITY DATA

This application claims the benefit of U.S. Provisional Patent Application Serial No. 61/317,147, filed on March 24, 2010, which is incorporated herein by reference.

BACKGROUND

Semiconductor on Insulator (SOI) wafer technology is an outgrowth of MicroElectroMechanical Systems (MEMS) technologies. An SOI wafer is a stacked wafer substrate where a device wafer (typically silicon) is bonded to a dielectric layer that is bonded to a support wafer, otherwise known as a handle wafer. A typical process flow for the fabrication of SOI wafers can be as follows: two wafers are polished and coated with an oxide or other dielectric material. The wafers are mounted polished side face to face and bonded under high temperature and pressure. Then one of the two wafers is ground down using mechanical grinding and chemical mechanical polishing to a specific thickness. In this way it is possible to generate semiconductor wafers that are electrically isolated from the underlying substrate.

SUMMARY

The present disclosure provides semiconductor structures and devices that can exhibit various enhanced properties, such as, for example, enhanced light detection properties. In one aspect, a semiconductor device is provided. Such a device can include a semiconductor substrate and a semiconductor layer coupled to the semiconductor substrate, where the semiconductor layer has a device surface opposite the semiconductor substrate. The device also includes at least one textured region coupled between the semiconductor substrate and the semiconductor layer. In another aspect, the device further includes at least one dielectric layer coupled between the semiconductor substrate and the semiconductor layer. In one aspect, the semiconductor layer is an epitaxially grown semiconductor layer. In another aspect, the semiconductor layer is a silicon layer. In a further aspect, a secondary semiconductor layer is disposed between the textured region and the semiconductor layer.

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Various positional configurations for the layers according to aspects of the present disclosure are contemplated, and any such configuration is considered to be within the present scope. In one specific aspect, for example, the dielectric layer is coupled between the semiconductor substrate and the textured region, and the textured region is disposed between the dielectric layer and the semiconductor layer. In one specific aspect, a reflective region is disposed between the semiconductor substrate and the textured region. In another specific aspect, the textured region is coupled directly to the semiconductor layer. In yet another specific aspect, a secondary semiconductor layer is disposed between the textured region and the semiconductor layer. In a further specific aspect, at least one cavity region disposed between the textured region and the dielectric layer. As another aspect of positional arrangement, the textured region is disposed between the semiconductor substrate and the dielectric layer, and the dielectric layer is disposed between the textured region and the semiconductor layer.

In one aspect of the present disclosure, a polysilicon layer is directly coupled to the dielectric layer. In another aspect, the polysilicon layer is disposed between multiple dielectric layers. In some aspects, the polysilicon layer can be doped.

In one aspect of the present disclosure, at least one photodiode optically active region is disposed on the device surface. In another aspect, the photodiode optically active region comprises a doped region. In yet another aspect, the device forms at least one photodetector. In a further aspect, the at least one photodetector is a plurality of photodetectors arranged in an array. In yet a further aspect, the textured region is arranged in a discontinuous pattern that corresponds spatially to the array of photodetectors. In another aspect, the device includes a plurality of isolation features in at least the semiconductor layer to isolate each photodetector in the array of photodetectors, where the isolation features isolate each photodetector electrically, optically, or both electrically and optically. In yet another aspect, the device includes at least one optical lens associated with the at least one photodetector. In a further aspect, the device includes at least one color filter associated with the at least one photodetector.

In one aspect of the present disclosure, the textured region is doped with a dopant to form an electrical back surface field. In another aspect, the electrical back surface field has been doped by a technique such as, without limitation, laser doping, ion implanting, diffusion doping, in situ doping, and the like, including combinations

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thereof. In yet another aspect, the textured region has a higher dopant concentration than the semiconductor layer. In a further aspect, the dopant has the same polarity as the semiconductor layer. Non-limiting examples of such dopants can include boron, indium, gallium, arsenic, antimony, phosphorus, and the like, including combinations thereof. Additionally, in other aspects a back surface field can be created by doping the semiconductor layer outside of the textured region. In one aspect, for example, the semiconductor layer is doped with a dopant to form an electrical back surface field, where the electrical back surface field is distinct from the textured region.

The present disclosure additionally provides methods of making semiconductor devices. In one aspect, one such method includes texturing at least a portion of a surface of a semiconductor layer to form a textured region, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate. In one aspect, the semiconductor layer is an epitaxially grown semiconductor layer. In another aspect, texturing at least a portion of a surface of a semiconductor layer to form a textured region further includes forming the epitaxially grown semiconductor layer on a growth substrate and texturing at least a portion of a surface of the epitaxially grown semiconductor layer to form a textured region. In yet another aspect, the method includes removing the growth substrate to expose the epitaxially grown semiconductor layer. In an alternative aspect, the method can include forming an epitaxially grown semiconductor layer on the semiconductor layer on an opposite side from the textured region.

In another aspect, wafer bonding includes depositing a polysilicon layer on the first dielectric layer and then bonding the polysilicon layer between the first dielectric layer and the second dielectric layer. In yet another aspect, at least a portion of the polysilicon layer can be doped. It is also contemplated that the present scope can include multiple dielectric and/or semiconductor material layers disposed between the semiconductor substrate and semiconductor layer.

In a further aspect, texturing at least a portion of a surface of the semiconductor layer to form the textured region further includes forming an opening in the semiconductor substrate, the second dielectric layer, and the first dielectric layer to expose a portion of the semiconductor layer and texturing at least a portion of the exposed portion of the semiconductor layer to form the textured region.

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In another aspect, the present disclosure provides a method of protecting a textured region from contamination during manufacture of a semiconductor device. Such a method includes texturing at least a portion of a surface of a semiconductor layer to form a textured region, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the dielectric layer, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate, wherein the textured region is protected from contamination during further manufacturing processes by the semiconductor layer and the semiconductor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

For a further understanding of the nature and advantage of the present disclosure, reference is being made to the following detailed description of embodiments and in connection with the accompanying drawings, in which:

FIG. 1 is a cross-sectional view of a semiconductor structure in accordance with an embodiment of the present disclosure;

FIG. 2A is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 2B is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 2C is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 2D is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 3 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 4 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 5 is a cross-sectional view of a semiconductor photodiode in accordance with another embodiment of the present disclosure;

FIG. 6 is a cross-sectional view of a semiconductor photodetecting imager in accordance with another embodiment of the present disclosure;

FIG. 7 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

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FIG. 8 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 9 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 10 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 11A is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 11B is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 11C is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 12A is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 12B is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 12C is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 13A is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 13B is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 13C is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

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FIG. 13D is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure; and

FIG. 14 is a depiction of a method of making a semiconductor device in accordance with yet another aspect of the present disclosure.

DETAILED DESCRIPTION

Before the present disclosure is described herein, it is to be understood that this disclosure is not limited to the particular structures, process steps, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting.

Definitions

The following terminology will be used in accordance with the definitions set forth below.

It should be noted that, as used in this specification and the appended claims, the singular forms "a," and, "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a dopant" includes one or more of such dopants and reference to "the layer" includes reference to one or more of such layers.

As used herein, the terms "disordered surface" and "textured surface" can be used interchangeably, and refer to a surface having a topology with nano- to micron-sized surface variations. Although any texturing technique is considered to be within the present scope, in one aspect the texturing is formed by the irradiation of laser pulses. Furthermore, while the characteristics of a textured surface can be variable depending on the materials and techniques employed, in one aspect such a surface can be several hundred nanometers thick and made up of nanocrystallites (e.g. from about 10 to about 50 nanometers), nanopores, and the like. In another aspect, such a surface can include micron-sized structures (e.g. about 2 μm to about 60 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 500 μm.

As used herein, the terms "surface modifying," "surface modification," and "texturing" can be used interchangeably, and refer to the altering of a surface of a

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semiconductor material using a texturing technique. In one specific aspect, surface modification can include processes using primarily laser radiation or laser radiation in combination with a dopant, whereby the laser radiation facilitates the incorporation of the dopant into a surface of the semiconductor material. Accordingly, in one aspect surface modification includes doping the material.

As used herein, the term "fluence" refers to the amount of energy from a single pulse of laser radiation that passes through a unit area. In other words, "fluence" can be described as the energy density of one laser pulse.

As used herein, the term "target region" refers to an area of a semiconductor material that is intended to be doped or surface modified using laser radiation. The target region of a semiconductor material can vary as the surface modifying process progresses. For example, after a first target region is doped or surface modified, a second target region may be selected on the same semiconductor material.

As used herein, the term "absorptance" refers to the fraction of incident electromagnetic radiation absorbed by a material or device.

As used herein, the term "substantially" refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is "substantially" enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use of "substantially" is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is "substantially free of" particles would either completely lack particles, or so nearly completely lack particles that the effect would be the same as if it completely lacked particles. In other words, a composition that is "substantially free of" an ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

As used herein, the term "about" is used to provide flexibility to a numerical range endpoint by providing that a given value may be "a little above" or "a little below" the endpoint.

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As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of "about 1 to about 5" should be interpreted to include not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

The Disclosure

The present disclosure provides semiconductor devices and associated methods that can exhibit various enhanced properties, such as, for example, enhanced light detection properties. Additionally, the present disclosure provides an integrated approach for the fabrication and application of textured semiconductor materials resulting in enhancement of image sensors and photodetectors. Specific types of semiconductor texturing can enhance the spectral bandwidth, absorption, and quantum efficiency of a semiconductor material. Performance can also be enhanced through various architecture configurations. Such configurations can also significantly improve the process integration of a particular device architecture with traditional process flows such as, for example, traditional CMOS process flows.

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A device design having a textured region located on, for example, the back surface of a photodetector, provides significant performance benefits. The textured region can have surface features that can lead to higher recombination of photocarriers for short wavelengths (e.g. in the blue green part of the spectrum) due to the very shallow penetration of those wavelengths into the detecting volume of the device. By physically locating the textured on the back surface of the device, a pristine surface is provided for the collection of short wavelengths on the top surface (i.e. the light incident surface), and the longer wavelengths that penetrate deep into or through the detecting region of the semiconductor material are collected by or with the help of the textured region opposite the light incident surface. It should be noted that, in addition to backside illuminated, front side illuminated architectures are also contemplated to be within the present scope. In addition, enhanced performance and ease of manufacture can also be accomplished by locating a textured region within a semiconductor stack or wafer. In some aspects, the textured layer can be located within the semiconductor stack early in the manufacturing process prior to the deposition of structures or circuitry that may be negatively affected by a texturing process. Additionally, such a semiconductor stack can be sent to an outside fabrication process for further manufacturing without exposing technological details regarding the textured region embedded between the semiconductor layers or any interaction between the textured region and the semiconductor layers.

In one aspect, as is shown in FIG. 1, a semiconductor device 10 is provided. While various semiconductor functions are contemplated, in one aspect the semiconductor device can exhibit enhanced electromagnetic radiation detection. Such a device can include a semiconductor substrate 12 and a semiconductor layer 14 coupled to the semiconductor substrate. The semiconductor layer has a device surface 15 opposite the semiconductor substrate. The device also includes at least one textured region 16 located or coupled between the semiconductor substrate and the semiconductor layer. As such, the textured region is enclosed between the semiconductor substrate and the semiconductor layer. Subsequent processing of the semiconductor device such as, for example, the formation of structures on the device surface, does not affect this buried textured region. In one aspect, the textured region can be formed on the semiconductor substrate. In another aspect, the textured region can be formed on the semiconductor layer. Additionally, for FIG. 1 and subsequent figures, the textured region can be a single textured region as is shown, or the textured

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region can be multiple discrete textured regions. Also, the textured region can cover only a portion of the surface area between the semiconductor substrate and the semiconductor layer as is shown, or the textured region can cover the entire surface area there between.

In another aspect, as is shown in FIG. 2A, a semiconductor device 20A is provided. Such a device can include a semiconductor substrate 22 and a semiconductor layer 24 coupled to the semiconductor substrate. The device also includes at least one textured region 26 located or coupled between the semiconductor substrate and the semiconductor layer, and at least one dielectric layer 28 coupled between the semiconductor substrate and the semiconductor layer. While various utilities are contemplated for the dielectric layer, in one aspect such a layer can be used to wafer bond the semiconductor layer to the semiconductor substrate. In one aspect, the dielectric layer can be formed on the semiconductor substrate. In another aspect, the dielectric layer can be formed on the textured region. Also, in some aspects the textured region can be formed on the dielectric layer. Additionally, in one aspect the semiconductor layer can be an epitaxially grown semiconductor layer. Thus in some aspects, the textured region can be formed on the epitaxially grown semiconductor layer.

It should be noted that, for all aspects, the present scope can also include multiple dielectric layers and/or multiple semiconductor material layers disposed between the semiconductor substrate and semiconductor layer. Additionally, the semiconductor layer itself can be multiple semiconductor layers and the semiconductor substrate can include multiple layers. It should also be noted that the semiconductor substrate refers to a substrate for a semiconductor, and can be comprised of semiconductor materials and/or non-semiconductor materials.

FIG. 2B shows a semiconductor device 20B having a secondary semiconductor layer 27 located between the textured region and the semiconductor layer. A semiconductor layer 24 is formed on the secondary semiconductor layer. In one aspect the semiconductor layer is an epitaxially grown semiconductor layer. Thus in some aspects, the textured region can be formed on the secondary semiconductor layer or on the dielectric layer 28. It should be noted that all reference numbers in FIGs. 2B-D that have been reused from FIG. 2A denote the same or similar materials and/or structures whether or not further description is provided.

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FIG. 2C shows a semiconductor device 20C whereby the dielectric layer 28 coupled between the semiconductor layer and the textured region. In this case, the dielectric layer can be formed on the semiconductor layer 24, the textured region 28, or on both the semiconductor layer and the textured region. In one aspect, the textured region can be formed on the semiconductor substrate 22. In another aspect, the textured region can be formed on the dielectric layer.

Additionally, in some aspects, as is shown in FIG. 2D for semiconductor device 20D, the dielectric layer can be a plurality of dielectric layers 28. In the case of wafer bonding, for example, a first dielectric layer can be associated with the textured layer and a second dielectric layer can be associated with the semiconductor substrate. The first dielectric layer and the second dielectric layer are heated and pressed together, with or without the aid of further pressure, temperature, or plasma surface activation, to cause the dielectric layers to bond to one another, thus forming a single wafer-bonded structure. It should be noted, however, that wafer-bonding can be accomplished without one or more dielectric layers, and as such the present scope should also include wafer-bonding that lacks such dielectric materials. Additionally, in some aspects, the textured region can be located in between the plurality of dielectric layers (not shown).

A variety of semiconductor materials are contemplated for use with the devices and methods according to aspects of the present disclosure. Such materials can be utilized as the semiconductor layer and/or the semiconductor substrate, as well as for the secondary semiconductor layer and the epitaxially grown semiconductor layer. Non-limiting examples of such semiconductor materials can include group IV materials, compounds and alloys comprised of materials from groups II and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can include silicon carbide (SiC) and silicon germanium (SiGe). In one specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum gallium arsenide, and combinations thereof.

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Exemplary combinations of group II-VI materials can include cadmium selenide (CdSe), cadmium sulfide (CdS), cadmium telluride (CdTe), zinc oxide (ZnO), zinc selenide (ZnSe), zinc sulfide (ZnS), zinc telluride (ZnTe), cadmium zinc telluride (CdZnTe, CZT), mercury cadmium telluride (HgCdTe), mercury zinc telluride (HgZnTe), mercury zinc selenide (HgZnSe), and combinations thereof.

Exemplary combinations of group III-V materials can include aluminum antimonide (AlSb), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum phosphide (AlP), boron nitride (BN), boron phosphide (BP), boron arsenide (BAs), gallium antimonide (GaSb), gallium arsenide (GaAs), gallium nitride (GaN), gallium phosphide (GaP), indium antimonide (InSb), indium arsenide (InAs), indium nitride (InN), indium phosphide (InP), aluminum gallium arsenide (AlGaAs, $Al_xGa_{1-x}As$), indium gallium arsenide (InGaAs, $In_xGa_{1-x}As$), indium gallium phosphide (InGaP), aluminum indium arsenide (AlInAs), aluminum indium antimonide (AlInSb), gallium arsenide nitride (GaAsN), gallium arsenide phosphide (GaAsP), aluminum gallium nitride (AlGaN), aluminum gallium phosphide (AlGaP), indium gallium nitride (InGaN), indium arsenide antimonide (InAsSb), indium gallium antimonide (InGaSb), aluminum gallium indium phosphide (AlGaInP), aluminum gallium arsenide phosphide (AlGaAsP), indium gallium arsenide phosphide (InGaAsP), aluminum indium arsenide phosphide (AlInAsP), aluminum gallium arsenide nitride (AlGaAsN), indium gallium arsenide nitride (InGaAsN), indium aluminum arsenide nitride (InAlAsN), gallium arsenide antimonide nitride (GaAsSbN), gallium indium nitride arsenide antimonide (GaInNAsSb), gallium indium arsenide antimonide phosphide (GaInAsSbP), and combinations thereof.

The semiconductor material can be of any thickness that allows the desired property or functionality of the semiconductor device, and thus any such thickness of semiconductor material is considered to be within the present scope. The textured region can increase the efficiency of the device such that, in some aspects, the semiconductor material can be thinner than has previously been possible. Decreasing the thickness reduces the amount of semiconductor material used to make such a device. In one aspect, for example, a semiconductor material such as the semiconductor layer has a thickness of from about 500 nm to about 50 μm. In another aspect, the semiconductor material has a thickness of less than or equal to about 500 μm. In yet another aspect, the semiconductor material has a thickness of from about 1 μm to about 10 μm. In a further aspect, the semiconductor material can have a

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thickness of from about 5 μm to about 750 μm. In yet a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 100 μm.

Additionally, various configurations of semiconductor materials are contemplated, and any such material configuration that can be incorporated into a semiconductor device is considered to be within the present scope. In one aspect, for example, the semiconductor material can include monocrystalline materials. In another aspect, the semiconductor material can include multicrystalline materials. In yet another aspect, the semiconductor material can include microcrystalline materials. It is also contemplated that the semiconductor material can include amorphous materials.

As has been described, the semiconductor substrate can be of any size, shape, and material capable of supporting the semiconductor layer and associated components during manufacture and/or use. The semiconductor substrate can be made from various materials, including the semiconductor materials described above, as well as non-semiconductor materials. Non-limiting examples of such materials can include metals, polymeric materials, ceramics, glass, and the like. In some aspects, the semiconductor substrate and the semiconductor layer have the same or substantially the same thermal expansion properties.

Furthermore, the semiconductor material according to aspects of the present disclosure can comprise multiple layers. In some aspects, layers can vary in majority carrier polarity (i.e. donor or acceptor impurities). The donor or acceptor impurities are typically determined by the type of dopant/impurities introduced into the device either through a growth process, deposition process, epitaxial process, implant process, lasing process or other known process to those skilled in the art. In some aspects such semiconductor materials can include an n-type layer, an intrinsic (i-type) layer, and a p-type layer, thus forming a p-i-n semiconductor material stack that creates a junction and/or depletion region. A semiconductor material devoid of an i-type layer is also contemplated in accordance with the present disclosure. In other aspects the semiconductor material may include multiple junctions. Additionally, in some aspects, variations of n(--), n(-), n(+), n(++), p(--), p(-), p(+), or p(++) type semiconductor layers can be used. The minus and positive signs are indicators of the relative magnitude of the doping of the semiconductor material.

As has been described, the textured region is buried between the semiconductor substrate and the semiconductor layer in various architectural

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arrangements. The textured can be of various thicknesses, depending on the desired use of the material. In one aspect, for example, the textured region has a thickness of from about 500 nm to about 100 μm. In another aspect, the textured region has a thickness of from about 500 nm to about 15 μm. In yet another aspect, the textured region has a thickness of from about 500 nm to about 2 μm. In a further aspect, the textured region has a thickness of from about 500 nm to about 1 μm. In another aspect, the textured region has a thickness of from about 200 nm to about 2 μm.

The textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and/or to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device. The textured region can include surface features to further increase the effective absorption length of the device. Non-limiting examples of shapes and configurations of surface features include cones, pillars, pyramids, microlenses, quantum dots, inverted features, gratings, protrusions, sphere-like structures, and the like, including combinations thereof. Additionally, surface features can be micron-sized, nano-sized, or a combination thereof. For example, cones, pyramids, protrusions, and the like can have an average height within this range. In one aspect, the average height would be from the base of the feature to the distal tip of the feature. In another aspect, the average height would be from the surface plane upon which the feature was created to the distal tips of the feature. In one specific aspect, a feature (e.g. a cone) can have a height of from about 50 nm to about 2 μm. As another example, quantum dots, microlenses, and the like can have an average diameter within the micron-sized and/or nano-sized range.

In addition to or instead of surface features, the textured region can include a textured layer. In one aspect, for example, the textured region can include a substantially conformal textured layer. Such a textured layer can have an average thickness of from about 1 nm to about 20 μm. In those aspects where the textured region includes surface features, the conformal textured layer can have a varying thickness relative to the location on the surface features upon which is deposited. In the case of cones, for example, the conformal textured layer can become thinner toward the tips of the cones. Such a conformal layer can include various materials, including, without limitation, SiO_2, Si_3N_4, amorphous silicon, polysilicon, a metal or metals, and the like, including combinations thereof. The conformal textured layer can also be one or more layers of the same or different materials, and can be formed during the creation of surface features or in a separate process.

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Textured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared). Such internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor layer. This increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.

The materials used for making the textured region can vary depending on the design and the desired characteristics of the device. As such, any material that can be utilized in the construction of a textured region is considered to be within the present scope. In one aspect, for example, the texture region can be a textured portion of a specific material, such as a portion of the semiconductor layer or the semiconductor substrate. If the texture layer is to be associated with the semiconductor layer, for example, a surface facing the semiconductor substrate can be textured prior to an attachment process such as wafer bonding. In another aspect, the textured region can be formed from a material that is deposited onto the semiconductor layer or semiconductor substrate, or the textured layer itself can be deposited. Such materials can include a semiconductor material, a dielectric material, or the like, including combinations thereof. In one specific example, the deposited material can include a silicon material. In another specific example, the deposited material can be polysilicon. In yet another aspect, the deposited material can be a dielectric material.

The texturing process can texture the entire substrate to be processed or only a portion of the substrate. In one aspect, for example, a substrate such as the semiconductor layer can be textured and patterned by an appropriate technique over an entire surface to form the texture region. In another aspect, a substrate such as the semiconductor layer can be textured and patterned across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch or a laser process to define a specific structure or pattern.

In addition to surface features, the textured region can have a surface morphology that is designed to focus or otherwise direct electromagnetic radiation. For example, in one aspect the textured region has a surface morphology operable to direct electromagnetic radiation into the semiconductor layer. Non-limiting examples of various surface morphologies include sloping, pyramidal, inverted pyramidal, spherical, square, rectangular, parabolic, asymmetric, symmetric, and the like, including combinations thereof.

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The textured region, including surface features as well as surface morphologies, can be formed by various techniques, including plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, selective epitaxial growth, and the like.

One effective method of producing a textured region is through laser processing. Such laser processing allows discrete target areas of a substrate to be textured, as well as entire surfaces. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope. Laser treatment or processing can allow, among other things, enhanced absorption properties and thus increased electromagnetic radiation focusing and detection.

In one aspect, for example, a target region of the substrate to be textured can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Patents 7,057,256, 7,354,792 and 7,442,629, which are incorporated herein by reference in their entireties. Briefly, a surface of a substrate material is irradiated with laser radiation to form a textured or surface modified region. Such laser processing can occur with or without a dopant material. In those aspects whereby a dopant is used, the laser can passed through a dopant carrier and onto the substrate surface. In this way, dopant from the dopant carrier is introduced into the target region of the substrate material. Such a region incorporated into a substrate material can have various benefits in accordance with aspects of the present disclosure. For example, the textured region typically has a textured surface that increases the surface area and increases the probability of radiation absorption. In one aspect, such a textured region is a substantially textured surface including micron-sized and/or nano-sized surface features that have been generated by the laser texturing. In another aspect, irradiating the surface of a substrate material includes exposing the laser radiation to a dopant such that irradiation incorporates the dopant into the substrate. Various dopant materials are known in the art, and are discussed in more detail herein.

Thus the surface of the substrate at the target region is thus chemically and/or structurally altered by the laser treatment, which may, in some aspects, result in the formation of surface features appearing as structures or patterned areas on the surface and, if a dopant is used, the incorporation of such dopants into the substrate material.

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In some aspects, the features or structures can be on the order of 50 nm to 20 μm in size and can assist in the absorption of electromagnetic radiation. In other words, the textured surface can increase the probability of incident radiation being absorbed.

The type of laser radiation used to surface modify a material can vary depending on the material and the intended modification. Any laser radiation known in the art can be used with the devices and methods of the present disclosure. There are a number of laser characteristics, however, that can affect the surface modification process and/or the resulting product including, but not limited to, the wavelength of the laser radiation, pulse width, pulse fluence, pulse frequency, polarization, laser propagation direction relative to the semiconductor material, etc. In one aspect, a laser can be configured to provide pulsatile lasing of a material. A short-pulsed laser is one capable of producing femtosecond, picosecond, and/or nanosecond pulse durations. Laser pulses can have a central wavelength in a range of about from about 10 nm to about 8 μm, and more specifically from about 200 nm to about 1200 nm. The pulse width of the laser radiation can be in a range of from about tens of femtoseconds to about hundreds of nanoseconds. In one aspect, laser pulse widths can be in the range of from about 50 femtoseconds to about 50 picoseconds. In another aspect, laser pulse widths can be in the range of from about 50 picoseconds to 100 nanoseconds. In another aspect, laser pulse widths are in the range of from about 50 to 500 femtoseconds.

The number of laser pulses irradiating a target region can be in a range of from about 1 to about 2000. In one aspect, the number of laser pulses irradiating a target region can be from about 2 to about 1000. Further, the repetition rate or frequency of the pulses can be selected to be in a range of from about 10 Hz to about 10 μHz, or in a range of from about 1 kHz to about 1 MHz, or in a range from about 10 Hz to about 1 kHz. Moreover, the fluence of each laser pulse can be in a range of from about 1 kJ/m^2 to about 20 kJ/m^2, or in a range of from about 3 kJ/m^2 to about 8 kJ/m^2.

A variety of dopant materials are contemplated for both the formation of doped regions in the semiconductor layer and for doping of the textured region, and any dopant that can be used in such processes to modify a material is considered to be within the present scope. It should be noted that the particular dopant utilized can vary depending on the material being doped, as well as the intended use of the resulting material.

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A dopant can be either a charge donating or a charge accepting dopant species. More specifically, an electron donating or a hole donating species can cause a region to become more positive or negative in polarity as compared to the substrate upon which the rests. In one aspect, for example, the doped region can be p-doped. In another aspect the doped region can be n-doped.

In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof. It should be noted that the scope of dopant materials should include, not only the dopant materials themselves, but also materials in forms that deliver such dopants (i.e. dopant carriers). For example, S dopant materials includes not only S, but also any material capable being used to dope S into the target region, such as, for example, H_2S, SF_6, SO_2, and the like, including combinations thereof. In one specific aspect, the dopant can be S. Sulfur can be present at an ion dosage level of from about 5×10^{14} to about 3×10^{20} ions/cm^2. Non-limiting examples of fluorine-containing compounds can include ClF_3, PF_5, F_2 SF_6, BF_3, GeF_4, WF_6, SiF_4, HF, CF_4, CHF_3, CH_2F_2, CH_3F, C_2F_6, C_2HF_5, C_3F_8, C_4F_8, NF_3, and the like, including combinations thereof. Non-limiting examples of boron-containing compounds can include $B(CH_3)_3$, BF_3, BCl_3, BN, $C_2B_{10}H_{12}$, borosilica, B_2H_6, and the like, including combinations thereof. Non-limiting examples of phosphorous-containing compounds can include PF_5, PH_3, $POCl_3$, P_2O_5, and the like, including combinations thereof. Non-limiting examples of chlorine-containing compounds can include Cl_2, SiH_2Cl_2, HCl, $SiCl_4$, and the like, including combinations thereof. Dopants can also include arsenic-containing compounds such as AsH_3 and the like, as well as antimony-containing compounds. Additionally, dopant materials can include mixtures or combinations across dopant groups, i.e. a sulfur-containing compound mixed with a chlorine-containing compound. In one aspect, the dopant material can have a density that is greater than air. In one specific aspect, the dopant material can include Se, H_2S, SF_6, or mixtures thereof. In yet another specific aspect, the dopant can be SF_6 and can have a predetermined concentration range of about 5.0×10^{-8} mol/cm^3 to about 5.0×10^{-4} mol/cm^3. As one non-limiting example, SF_6 gas is a good carrier for the incorporation of sulfur into a substrate via a laser process without significant adverse effects on the material. Additionally, it is noted that dopants can also be liquid solutions of n-type or p-type dopant materials dissolved in a solution such as water, alcohol, or an acid or basic

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solution. Dopants can also be solid materials applied as a powder or as a suspension dried onto the wafer.

In one aspect, the textured region can be doped with a dopant to form an electrical back surface field (EBSF). The EBSF impedes the movement of minority carriers from reaching the textured region, thus keeping such carriers away from potential recombination sites near the interface. Similarly, dark current generation can also be minimized by pinning the interface generation states at certain band energy states through band structure optimization so that the dark carrier generation mechanism is suppressed. Band structure optimization can be achieved by using a variety of methods. It should be noted that any method that forms an electrical field near or within the textured region can be used. Non-limiting examples of such methods can include shifting the Fermi level energy, bending the minority carrier band, inserting a material with a different bandgap, and the like, including combinations thereof.

In one aspect, for example, the band structure optimization can be realized by modifying the interface doping concentration. For example, for a p-type laser textured region, a more heavily p-doped layer that partially overlaps with the laser modified interface can be used. The conduction band thus bends toward the higher energy direction when reaching towards the more p-doped layer, and hence the laser modified interface. One specific aspect is a heavily doped p++ layer that partially overlaps with the laser modified interface layer in a p-epi substrate where both the p++ layer and the modified interface layer sit between the bottom of an epitaxial device layer and the top of a carrier wafer.

As such, in one aspect, the EBSF has been doped by a technique such as, without limitation, laser doping, ion implanting, diffusion doping, in situ doping, and the like, including combinations thereof. In another aspect, the textured region or the EBSF has a higher dopant concentration than the semiconductor layer. In yet another aspect, the dopant has the same polarity as the semiconductor layer. Various dopants for use in generating an EBSF are contemplated. Non-limiting examples include boron, indium, gallium, arsenic, antimony, phosphorus, and the like, including combinations thereof. It should also be noted that an EBSF can be produced in the semiconductor layer, the dielectric layer, or the semiconductor substrate. In one aspect, for example, semiconductor layer or the semiconductor substrate is doped with

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a dopant to form an electrical back surface field, where the EBSF is distinct from the textured region.

In another aspect, the band structure optimization can be realized by forming a heterojunction along a modified semiconductor interface. For example, a layer of amorphous silicon can be deposited on the textured region interface, thus forming a heterojunction that bends the minority carrier band towards the desired energy direction.

The dielectric layer can be made from a variety of materials, and such materials can vary depending on the device design and desired characteristics. One use for such a layer involves the coupling of the semiconductor layer to the semiconductor substrate. In some cases, wafer bonding can be used as a coupling technique. The dielectric layer can thus facilitate the attachment of these materials together, as has been described. The dielectric layer can be associated with the semiconductor layer, the semiconductor substrate, or both the semiconductor layer and the semiconductor substrate prior to bonding. In those aspects having a dielectric layer associated with both materials, the dielectric layers can be bonded directly together, or in some cases, bonded together with an intervening textured region. Additionally, in some aspects a textured region can be formed on one or more dielectric layers. In some aspects, a dielectric layer can be bonded to a semiconductor material such as, for example, polysilicon. In other aspects, the semiconductor layer and the semiconductor substrate can be bonded together without an intervening dielectric layer.

Non-limiting examples of dielectric layer materials can include oxides, nitrides, oxynitrides, and the like, including combinations thereof. In one specific aspect, the dielectric layer includes an oxide. In another aspect, the dielectric layer includes a buried oxide. Additionally, the dielectric layer can be of various thicknesses. In one aspect, for example, the dielectric layer has a thickness of from about 100 nm to about 4 microns. In another aspect, the dielectric layer has a thickness of from about 500 nm to about 2 microns. In yet another aspect, the dielectric layer has a thickness of from about 500 nm to about 1000 microns.

The devices according to aspects of the present disclosure can additionally include one or more reflecting regions. In one aspect, as is shown in FIG. 3, a photosensitive semiconductor device 30 can include a semiconductor substrate 32 and a semiconductor layer 34 coupled to the semiconductor substrate. The device also

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includes at least one textured region 36 located or coupled between the semiconductor substrate and the semiconductor layer, and at least one dielectric layer 38 coupled between the semiconductor substrate and the semiconductor layer. A reflecting region 39 is coupled to the semiconductor substrate, and positioned to interact with electromagnetic radiation. The reflecting region can be separated from the textured region by a dielectric layer as is shown, or the reflecting region can be associated directly with the textured region without an intervening dielectric layer. The reflecting region can be deposited over the entire interface between the semiconductor substrate and the next adjacent layer, or only over a portion of the interface. In some aspects, the reflecting region can be deposited over a larger area of the device compared to the textured region. The reflecting region can be positioned to reflect electromagnetic radiation that has passed through the texture region back through the textured region toward the semiconductor layer. In other words, as electromagnetic radiation passes through the semiconductor layer, a portion that is not absorbed contacts the textured region. Of that portion that contacts the textured region, a smaller portion may pass though the textured region to strike the reflecting region and be reflected back through the textured region toward the semiconductor layer.

A variety of reflective materials can be utilized in constructing the reflecting region, and any such material capable of incorporation into a photosensitive device is considered to be within the present scope. Non-limiting examples of such materials include a Bragg reflector, a metal reflector, a metal reflector over a dielectric material, a transparent conductive oxide such as zinc oxide, indium oxide, or tin oxide, and the like, including combinations thereof. Non-limiting examples of metal reflector materials can include silver, aluminum, gold, platinum, reflective metal nitrides, reflective metal oxides, and the like, including combinations thereof. In one aspect, a dielectric material can be coupled to the reflecting region along the side facing the textured region. In one specific aspect, the dielectric material can include an oxide layer and the reflecting region can include a metal layer. The surface of the metal layer on an oxide acts as a mirror-like reflector for the incident electromagnetic radiation from the backside.

Additionally, the textured surface of a metal on a roughened oxide can act as a diffusive scattering site for the incident electromagnetic radiation and also as a mirror-like reflector. Other aspects can utilize porous materials for the texturing. Porous polysilicon, for example, can be oxidized or oxide deposited and a reflective region

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such as a metal reflector can be associated therewith to provide a scattering and reflecting surface. In another aspect, aluminum can be subjected to anodic oxidation to provide porous aluminum oxide, a high dielectric constant insulator. This insulator can be coated with aluminum or other metals to provide a scattering and reflecting surface.

In one specific aspect, a reflective region can include a transparent conductive oxide, an oxide, and a metal layer. The transparent oxide can be textured and a metal reflector deposited thereupon. The textured surface of the metal on a roughened transparent conductive oxide can act as a diffusive scattering site for the incident electromagnetic radiation.

In another specific aspect, a Bragg reflector can be utilized as a reflective region. A Bragg reflector is a structure formed from multiple layers of alternating materials with varying refractive indexes, or by a periodic variation of some characteristic (e.g. height) of a dielectric waveguide, resulting in periodic variation in the effective refractive index in the guide. Each layer boundary causes a partial reflection of an optical wave. For waves whose wavelength is close to four times the optical thickness of the layers, the many reflections combine with constructive interference, and the layers act as a high-quality reflector. Thus the coherent superpositioning of reflected and transmitted light from multiple interfaces in the structure interfere so as to provide the desired reflective, transmissive, and absorptive behavior. In one aspect, the Bragg reflector layers can be alternating layers of silicon dioxide and silicon. Because of the high refractive index difference between silicon and silicon dioxide, and the thickness of these layers, this structure can be fairly low loss even in regions where bulk silicon absorbs appreciably. Additionally, because of the large refractive index difference, the optical thickness of the entire layer set can be thinner, resulting in a broader-band behavior and fewer fabrications steps.

Additional scattering can be provided by positioning a textured forward scattering layer on the side of the device that receives incident electromagnetic radiation. These forward scattering layers can be, without limitation, textured oxides or polysilicon without a reflector.

In another aspect, as is shown in FIG. 4, a photosensitive semiconductor device 40 can also include a polysilicon layer 42 disposes between multiple dielectric layers 38. It should be noted that all reference numbers in FIG. 4 that have been reused from previous figures denote the same or similar materials and/or structures

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whether or not further description is provided. The addition of the polysilicon layer can provide various improvements in manufacturing in some cases. For example, a rough surface of a textured region can be challenging to wafer bond. By depositing a thin dielectric layer followed by a thick polysilicon layer it can be possible to create a surface that can be polished. Thus, the polysilicon layer can be planarized and polished until smooth, and the resulting surface can be wafer bonded to the dielectric layer on the opposing material, e.g. the semiconductor substrate if the polysilicon is deposited on the semiconductor layer structure. It is also contemplated that such a process can be performed with only one dielectric layer or even without any dielectric layers being present. In another aspect, the polysilicon layer can be doped with a dopant. In yet another aspect, the polysilicon layer can be a monosilicon layer. In one specific aspect, the polysilicon layer is a monosilicon layer and the semiconductor layer is an epitaxial layer that has been etched from the backside to form the textured region.

In another aspect, as is shown in FIG. 5, a photodiode 50 having enhanced light detection performance is provided. The photodiode includes contacts 52 and a photodiode junction 54 formed on the semiconductor layer 34. In another aspect, as is shown in FIG. 6, a CMOS image sensor having improved light detection performance is provided. The CMOS image sensor includes photodiode junctions 64 and circuitry 62 formed on the semiconductor layer 34. It should be noted that all reference numbers in FIGs. 5 and 6 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided. In this way, the textured region 36 can be introduced into fabrication process at the start of the flow, at a lower cost and lower technical risk approach. Because the textured region is buried within the semiconductor materials at an early stage in the flow, the textured region can be protected from contamination during the further fabrication of the device. Additionally, potentially proprietary details such as the specific architecture of the texture region can be protected from view during the later stages of fabrication. This method could further include a step of removing the semiconductor substrate. It is understood that once the semiconductor device is formed the semiconductor substrate may no longer be necessary in some cases. In this way the semiconductor device can be mounted on various substrates as necessary for specific applications.

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In one aspect, isolation features can be utilized in order to isolate various portions of the device from one another. For example, in one aspect a semiconductor device can include a plurality of isolation features in at least the semiconductor layer that function to isolate each photodetector in an array of photodetectors from one another. The isolation features isolate each photodetector electrically, optically, or both electrically and optically. Isolation features can thus maintain uniformity across an array by reducing optical and electrical crosstalk between the photodetectors. FIG. 7 shows a semiconductor device 70 having an array of photodetectors 72. It should be noted that all reference numbers in FIG. 7 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided. The photodetectors are separated by a plurality of isolation features, in this case extending through the semiconductor layer 34 and the textured region 36. In one aspect, the isolation features extend through the semiconductor layer but not through the textured region. In another aspect, the isolation features extend beyond the textured region and into the dielectric layer or even into the semiconductor substrate. In some aspects, other structures such as polysilicon layers and reflective regions can contain isolation features. Accordingly, the isolation features can be deep or shallow, depending on the desired configuration of the device.

Isolation features can be made from various materials, including, without limitation, dielectric materials, reflective materials, conductive materials, light diffusing features, voids, and the like, including combinations thereof. Conductive materials used to fill the isolation feature etches or voids can be passivated in order to maintain electrical isolation. In other aspects, conductive materials can be utilized as vias. The isolation can be fabricated at the substrate level prior to fabrication of circuitry, the detector device, or the imaging array. In one aspect, voids can be created and either left as voids or filled with such materials to form the isolation features. For example, a layer surface can be photolithographically patterned and vertically etched to a desired depth (e.g. from the device surface of the semiconductor layer to the dielectric layer). Dielectric material can then be deposited conformally on surfaces within the etch until filled with the dielectric or other material. Any dielectric material remaining on the device surface of the semiconductor layer can be removed by chemical etching and/or mechanical polishing. As has been described, the isolation feature does not need to fully bisect the semiconductor structure, but

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rather only a portion can be isolated; this is known as shallow trench isolation as opposed to deep trench isolation.

Additionally, isolation features regions can be configured to reflect incident electromagnetic radiation until it is absorbed, thereby increase the effective absorption length of the device. In other aspects, the sides of isolation features can be doped. In some aspects, a doped isolation feature can form an electrical surface field, similar to an electrical back surface field as has been described. The isolation features can be formed before or after bonding of the semiconductor substrate to the semiconductor layer. Furthermore, the isolation features can be formed from either side of the semiconductor layer or from either side of the semiconductor substrate, depending on the depth and extent of the features.

In some aspects, the textured region can be arranged in a discontinuous pattern. As is shown in FIG. 8, for example, a semiconductor device 80 can have a discontinuous textured region 82. It should be noted that all reference numbers in FIG. 8 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided. Such a discontinuous pattern may correspond to structures elsewhere in the device, such as the spatial pattern of an array of photodetectors on the device surface (not shown).

In other aspects, one or more cavities can be disposed in the semiconductor device and associated with the textured region or regions. As is shown in FIG. 9, for example, a semiconductor device 90 can include a cavity region 92 associated with the textured region 36. The cavity region can enhance the functionality of the textured region, and can be particularly effective when optically coupled to a reflective region, whether the reflective region is on the near side or the far side of the dielectric layer 38. FIG. 10 shows a semiconductor device 100 having a plurality of cavity regions 102 arranged in a discontinuous pattern to correspond with the discontinuous pattern of the textured region 82. The cavity regions shown in FIGs. 9 and 10 can be formed prior to wafer bonding or following wafer bonding. If a cavity region is formed following wafer bonding, etching through the semiconductor substrate 32 may be required, following which the etch cavity can be partially filled. Additionally, a cavity region can be formed before or after formation of the textured region. In those aspects whereby a cavity region is formed after formation of the textured region, the intervening material would be etched until reaching the textured region. In those aspects whereby a cavity region is formed prior to formation of the

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textured region, an etch can be formed into the semiconductor layer 34 and the textured region can be formed thereon through the etch cavity. The formation of the textured region in this manner can be accomplished prior to wafer bonding or following wafer bonding by etching through the semiconductor substrate. It should be noted that all reference numbers in FIGs. 9 and 10 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided.

The present disclosure additionally provides various methods. In one aspect, as is shown in FIG. 14, for example, a method of making a semiconductor device can include texturing at least a portion of a surface of a semiconductor layer to form a textured region 142, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer 144, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate 146. In another aspect, the textured region is protected from contamination during further manufacturing processes by the semiconductor layer and the semiconductor substrate.

In another aspect, a method of making a semiconductor device can include laser texturing at least a portion of a surface of a semiconductor layer to form a textured region, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate.

In yet another aspect, a method of making a semiconductor device can include wet etch texturing at least a portion of a surface of a semiconductor layer to form a textured region, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate.

In one specific aspect, FIGs. 11A-C show one method of manufacturing a semiconductor device. As is shown in FIG. 11A, a semiconductor material 114 can be textured to create a textured region 112, and a dielectric layer 115 can be deposited over the textured region. In one aspect, the textured region can be formed by laser processing the semiconductor material. In another aspect, the textured region can be formed by wet etching the semiconductor material. The dielectric layer can then be

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polished until smooth with a process such as CMP processing. The resulting structure can then be wafer bonded to a semiconductor substrate 116, as is shown rotated 180° in FIG. 11B, with the polished surface of the dielectric layer being bonded to the semiconductor substrate. The dielectric layer can be bonded directly to the semiconductor substrate, or to a second dielectric layer formed on the semiconductor substrate (not shown). After wafer bonding, the semiconductor material can be polished to a specified thickness. In another aspect, an epitaxially grown semiconductor layer 118 can be grown on the polished surface of the semiconductor material to generate a low defect device region as shown in FIG. 11C.

In another aspect, FIGs. 12A-C show another method of manufacturing a semiconductor device. As is shown in FIG. 12A, a semiconductor material 124 can be textured to create a textured region 122, and a dielectric layer 125 can be deposited over the textured region. In one aspect, the semiconductor material can be an epitaxially grown semiconductor material. The dielectric layer can then be polished and a polysilicon layer 126 can be deposited thereupon, as is shown in FIG. 12B. In an alternative aspect, the polysilicon layer can be formed directly on the textured region without an intervening dielectric layer (not shown). The polysilicon layer can then be polished and wafer bonded to a semiconductor substrate 126, as is shown rotated 180° in FIG. 12C. The polysilicon layer can be bonded directly to the semiconductor substrate, or to a second dielectric layer 129 formed on the semiconductor substrate. After wafer bonding, the semiconductor material can be polished to a specified thickness.

In another aspect, FIGs. 13A-D show another method of manufacturing a semiconductor device. As is shown in FIG. 13A, a semiconductor layer 134 can be epitaxially grown on a temporary semiconductor support 139. The epitaxially grown semiconductor layer is textured to create a textured region 132, and a dielectric layer 135 is deposited over the textured region as is shown in FIG. 13B. Following polishing, the dielectric layer is wafer bonded to a semiconductor substrate 136, as is shown rotated 180° in FIG. 13C. The dielectric layer can be bonded directly to the semiconductor substrate, or to a second dielectric layer formed on the semiconductor substrate (not shown). The temporary semiconductor support can then be removed from the epitaxially grown semiconductor layer. This can be accomplished by any known process, such as wafer splitting, CMP processing, etc. The exposed epitaxial semiconductor layer can be further polished and thinned to produce a desired surface

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for further device deposition. In this manner semiconductor materials used to grow the epitaxial layer can be removed, leaving a higher quality surface with fewer crystal defects and dislocations.

Of course, it is to be understood that the above-described arrangements are only illustrative of the application of the principles of the present disclosure. Numerous modifications and alternative arrangements may be devised by those skilled in the art without departing from the spirit and scope of the present disclosure and the appended claims are intended to cover such modifications and arrangements. Thus, while the present disclosure has been described above with particularity and detail in connection with what is presently deemed to be the most practical embodiments of the disclosure, it will be apparent to those of ordinary skill in the art that numerous modifications, including, but not limited to, variations in size, materials, shape, form, function and manner of operation, assembly and use may be made without departing from the principles and concepts set forth herein.

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CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a semiconductor substrate;

a semiconductor layer coupled to the semiconductor substrate, the semiconductor layer having a device surface opposite the semiconductor substrate; and

at least one textured region coupled between the semiconductor substrate and the semiconductor layer.

2. The device of claim 1, further comprising at least one dielectric layer coupled between the semiconductor substrate and the semiconductor layer.

3. The device of claim 2, wherein the semiconductor layer is an epitaxially grown semiconductor layer.

4. The device of claim 2, wherein the semiconductor layer is a silicon layer.

5. The device of claim 2, further comprising a secondary semiconductor layer disposed between the textured region and the semiconductor layer.

6. The device of claim 2, wherein the dielectric layer is coupled between the semiconductor substrate and the textured region, and wherein the textured region is disposed between the dielectric layer and the semiconductor layer.

7. The device of claim 6, further comprising a reflective region disposed between the semiconductor substrate and the textured region.

8. The device of claim 6, wherein the textured region is coupled directly to the semiconductor layer.

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9. The device of claim 6, further comprising a secondary semiconductor layer disposed between the textured region and the semiconductor layer.

10. The device of claim 6, further comprising at least one cavity region disposed between the textured region and the dielectric layer.

11. The device of claim 2, further comprising a polysilicon layer directly coupled to the dielectric layer.

12. The device of claim 11, wherein the polysilicon layer is disposed between multiple dielectric layers.

13. The device of claim 2, wherein the textured region is disposed between the semiconductor substrate and the dielectric layer, and wherein the dielectric layer is disposed between the textured region and the semiconductor layer.

14. The device of claim 2, wherein the textured region is doped with a dopant to form an electrical back surface field.

15. The device of claim 14, wherein the electrical back surface field has been doped by a technique selected from the group consisting of laser doping, ion implanting, diffusion doping, in situ doping, and combinations thereof.

16. The device of claim 15, wherein the textured region has a higher dopant concentration than the semiconductor layer.

17. The device of claim 15, wherein the dopant has the same polarity as the semiconductor layer.

18. The device of claim 15, wherein the dopant is a member selected from the group consisting of boron, indium, gallium, arsenic, antimony, phosphorus, and combinations thereof.

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19. The device of claim 2, wherein the semiconductor layer is doped with a dopant to form an electrical back surface field, and wherein the electrical back surface field is distinct from the textured region.

20. The device of claim 2, further comprising at least one photodiode optically active region disposed on the device surface.

21. The device of claim 2, wherein the photodiode optically active region comprises a doped region.

22. The device of claim 2, wherein the device forms at least one photodetector.

23. The device of claim 22, wherein the at least one photodetector is a plurality of photodetectors arranged in an array.

24. The device of claim 23, wherein the textured region is arranged in a discontinuous pattern that corresponds spatially to the array of photodetectors.

25. The device of claim 23, further comprising a plurality of isolation features in at least the semiconductor layer to isolate each photodetector in the array of photodetectors, wherein the isolation features isolate each photodetector electrically, optically, or both electrically and optically.

26. The device of claim 23, further comprising at least one optical lens associated with the at least one photodetector.

27. The device of claim 23, further comprising at least one color filter associated with the at least one photodetector.

28. A method of making a semiconductor device, comprising:

texturing at least a portion of a surface of a semiconductor layer to form a textured region;

depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric

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layer; and

wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate.

29. The method of claim 28, wherein the semiconductor layer is an epitaxially grown semiconductor layer.

30. The method of claim 29, wherein texturing at least a portion of a surface of a semiconductor layer to form a textured region further includes:

forming the epitaxially grown semiconductor layer on a growth substrate; and

texturing at least a portion of a surface of the epitaxially grown semiconductor layer to form a textured region.

31. The method of claim 30, further comprising removing the growth substrate to expose the epitaxially grown semiconductor layer.

32. The method of claim 28, further comprising forming an epitaxially grown semiconductor layer on the semiconductor layer on an opposite side from the textured region.

33. The method of claim 28, wherein wafer bonding further includes:

depositing a polysilicon layer on the first dielectric layer; and

bonding the polysilicon layer between the first dielectric layer and the second dielectric layer.

34. The method of claim 33, further comprising doping at least a portion of the polysilicon layer.

35. The method of claim 28, wherein texturing at least a portion of a surface of the semiconductor layer to form the textured region further includes:

forming an opening in the semiconductor substrate, the second dielectric layer, and the first dielectric layer to expose a portion of the semiconductor layer; and

texturing at least a portion of the exposed portion of the semiconductor layer to form the textured region.

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36. The method of claim 28, wherein texturing includes a technique selected from the group consisting of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.

37. The method of claim 28, wherein texturing includes lasing.

38. A method of protecting a textured region from contamination during manufacture of a semiconductor device, comprising:

texturing at least a portion of a surface of a semiconductor layer to form a textured region;

depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the dielectric layer; and

wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate, wherein the textured region is protected from contamination during further manufacturing processes by the semiconductor layer and the semiconductor substrate.

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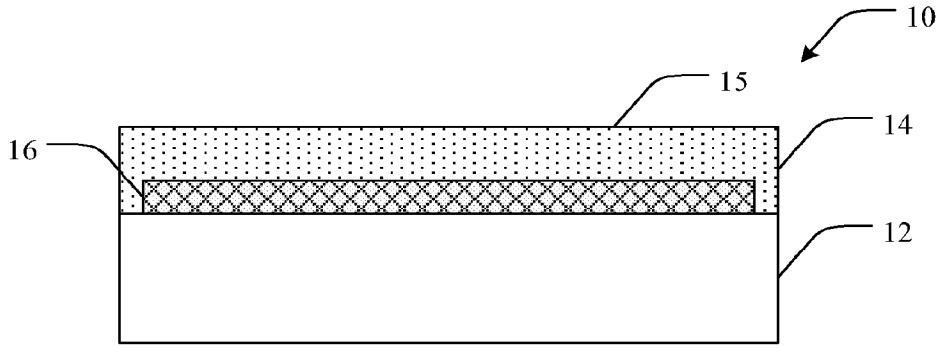

FIG. 1

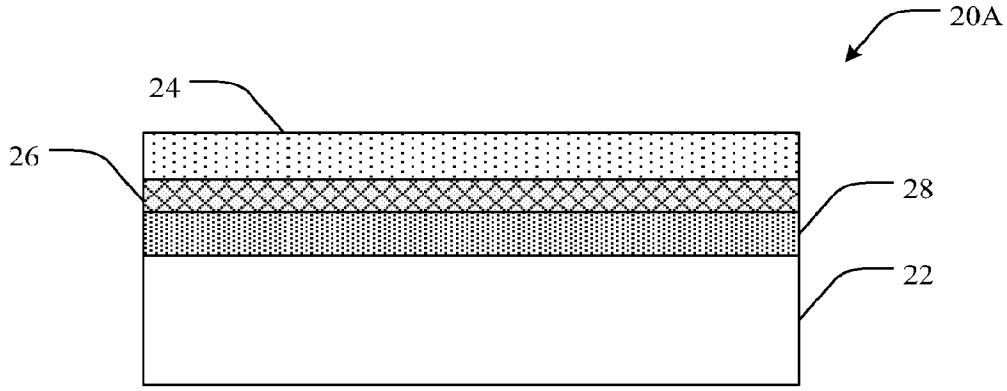

FIG. 2A

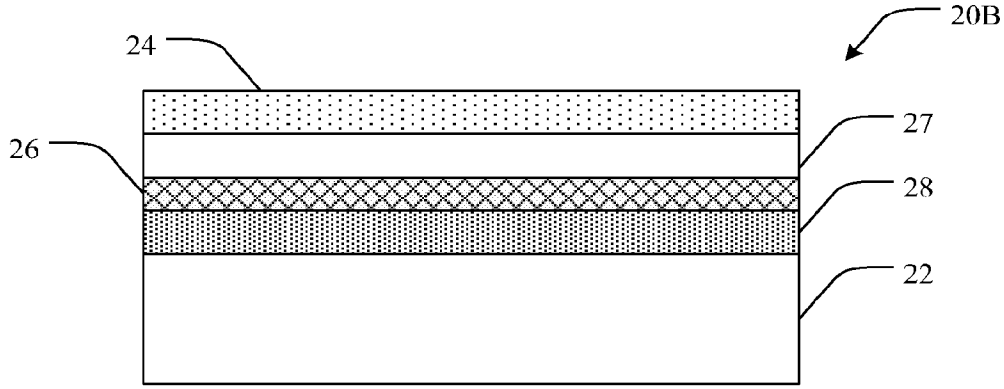

FIG. 2B

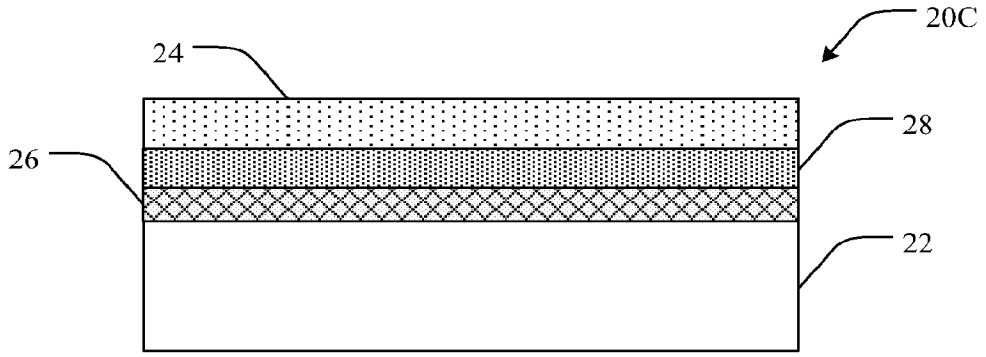

FIG. 2C

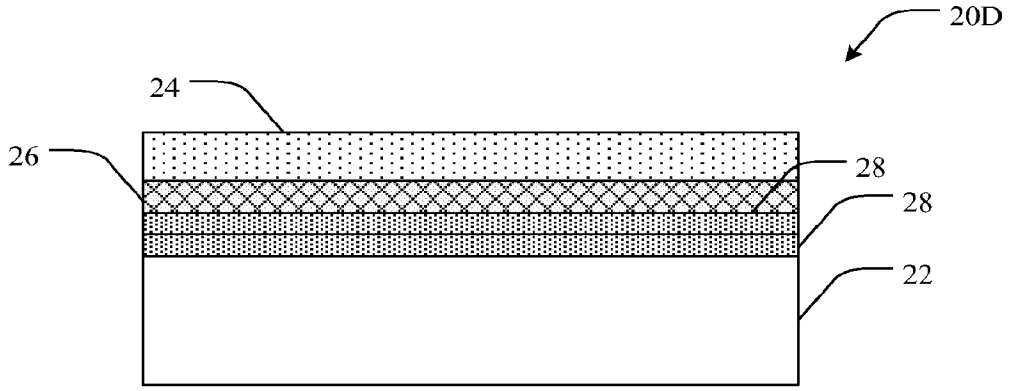

FIG. 2D

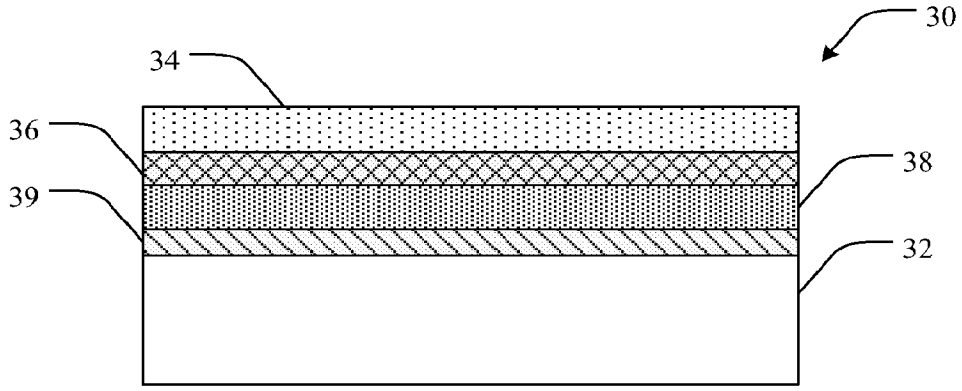

FIG. 3

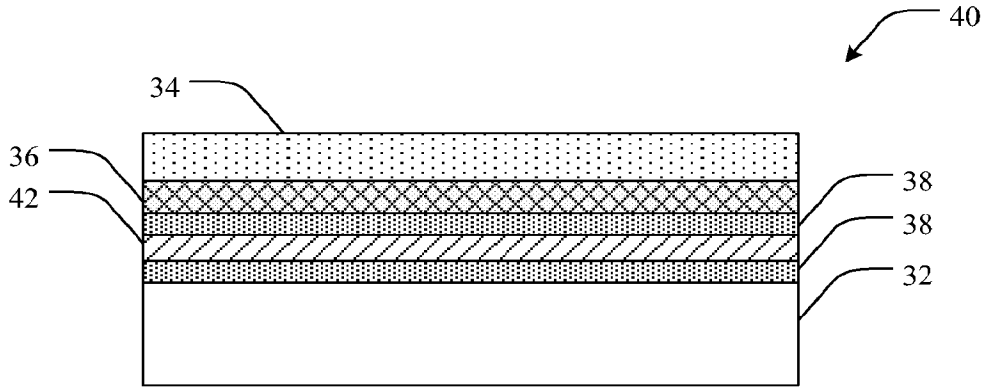

FIG. 4

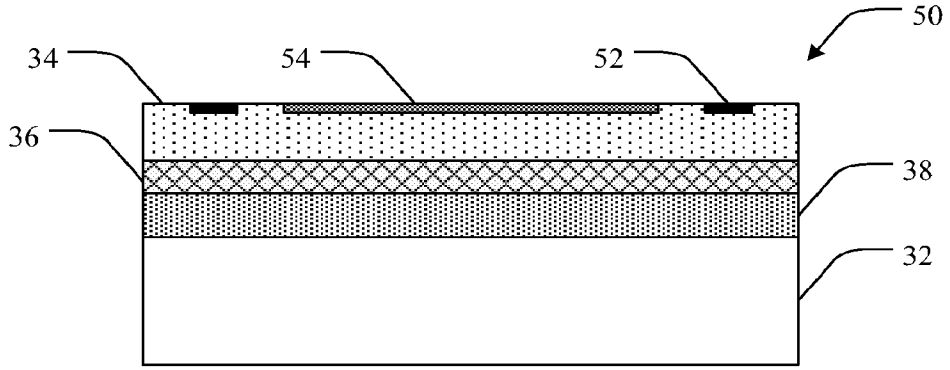

FIG. 5

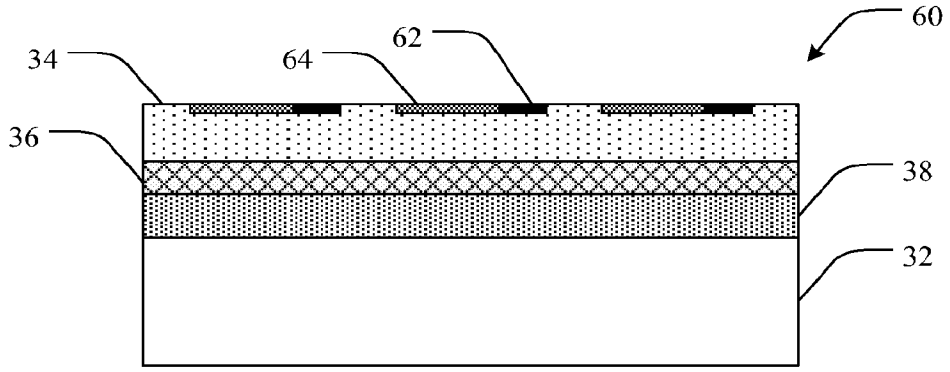

FIG. 6

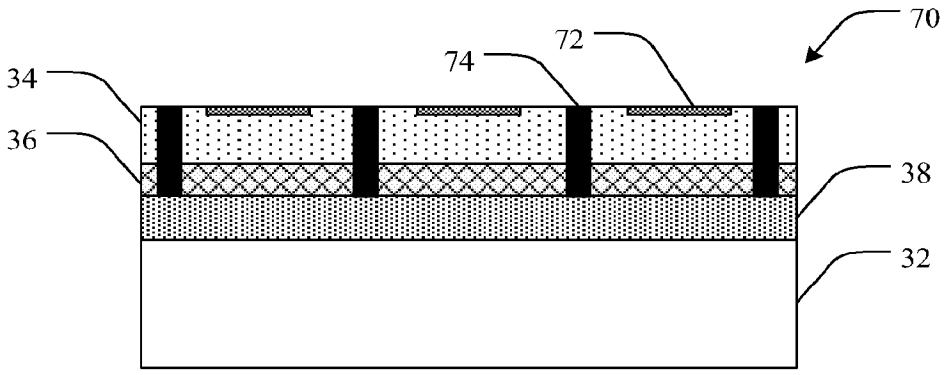

FIG. 7

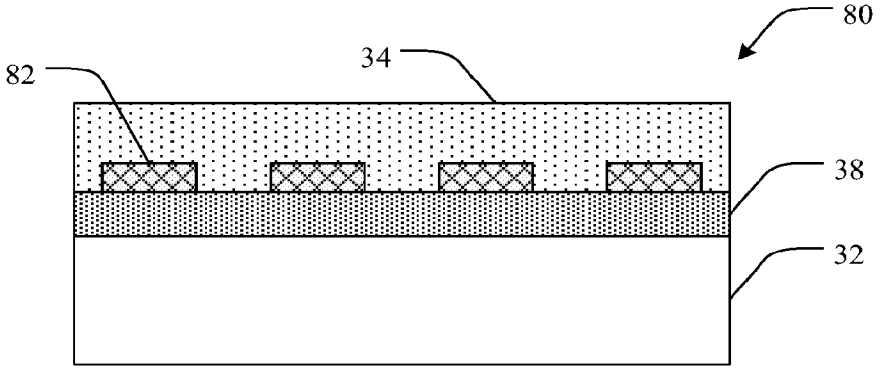

FIG. 8

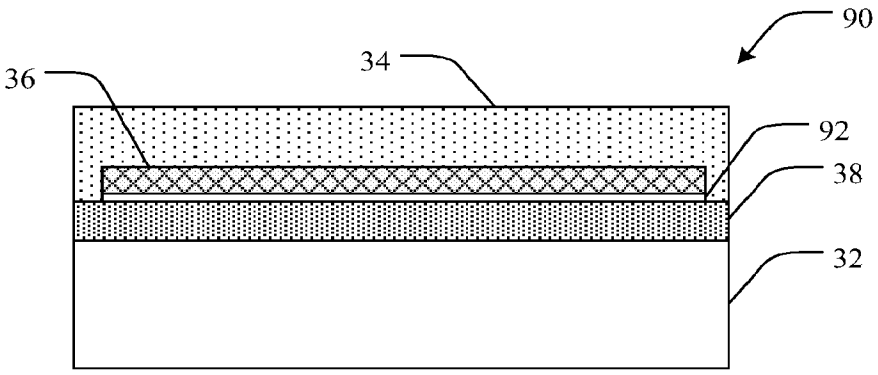

FIG. 9

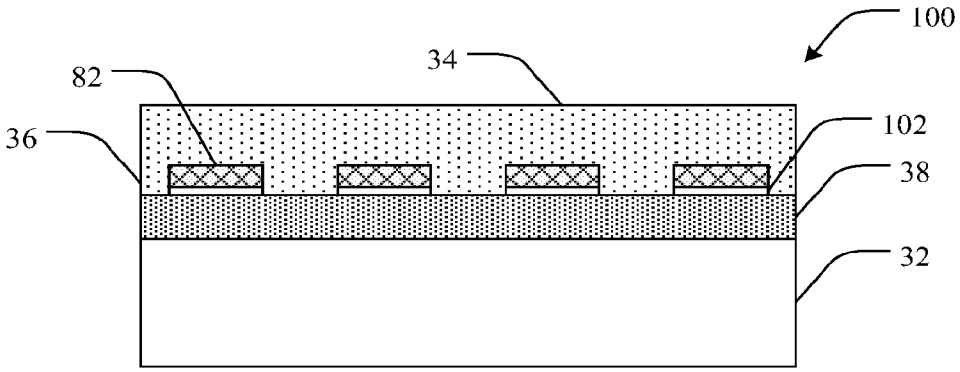

FIG. 10

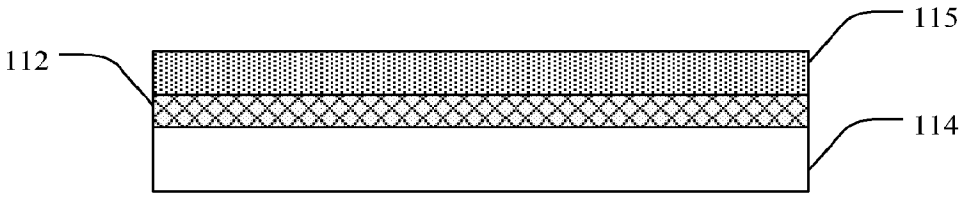

FIG. 11A

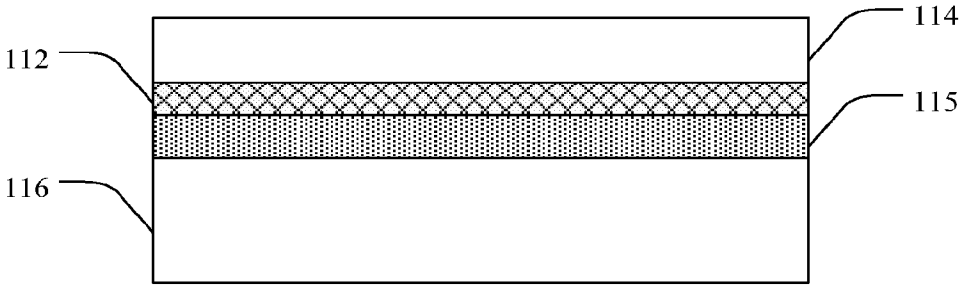

FIG. 11B

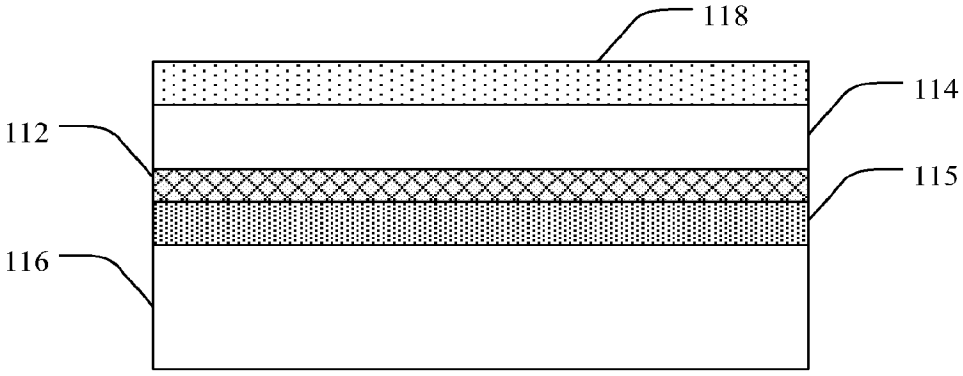

FIG. 11C

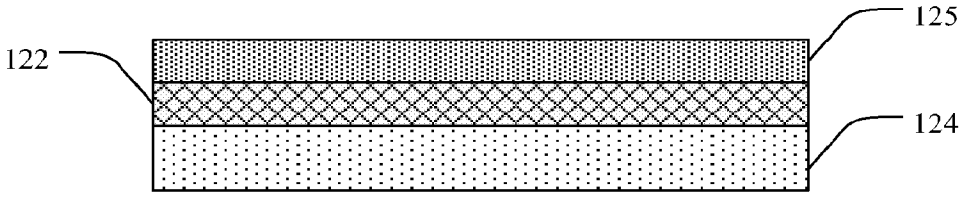

FIG. 12A

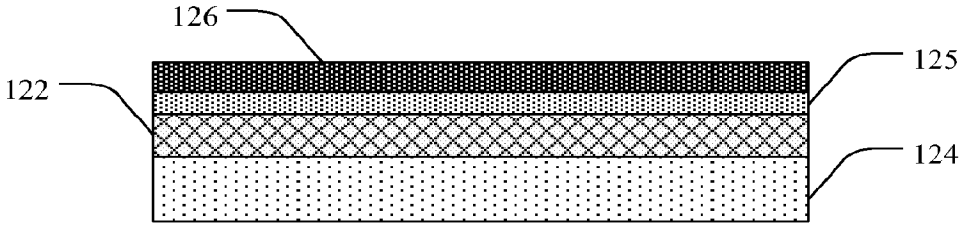

FIG. 12B

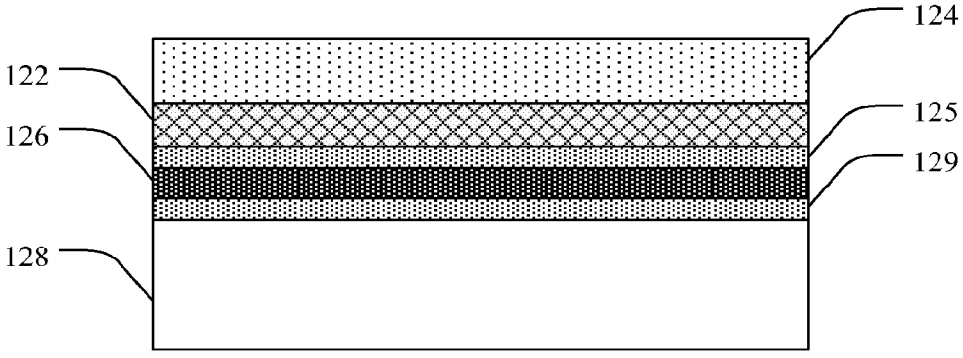

FIG. 12C

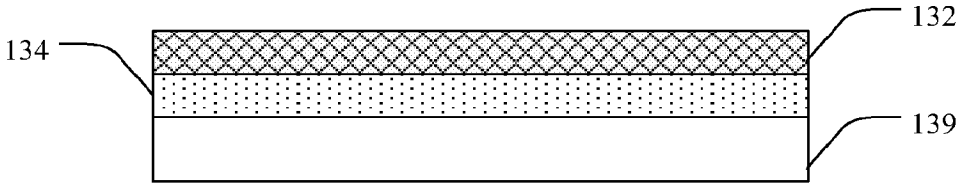

FIG. 13A

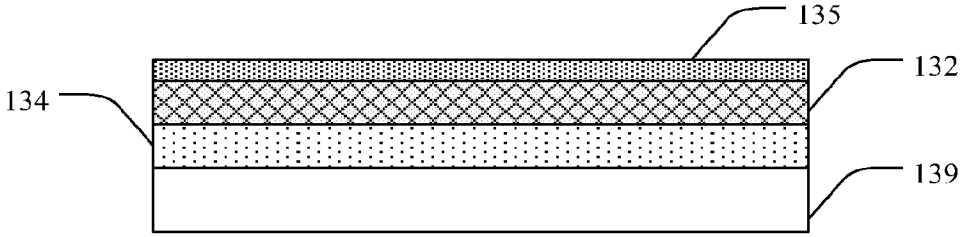

FIG. 13B

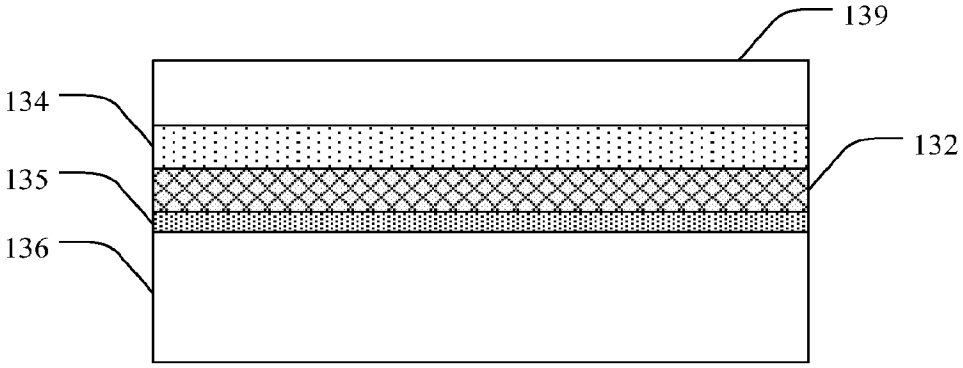

FIG. 13C

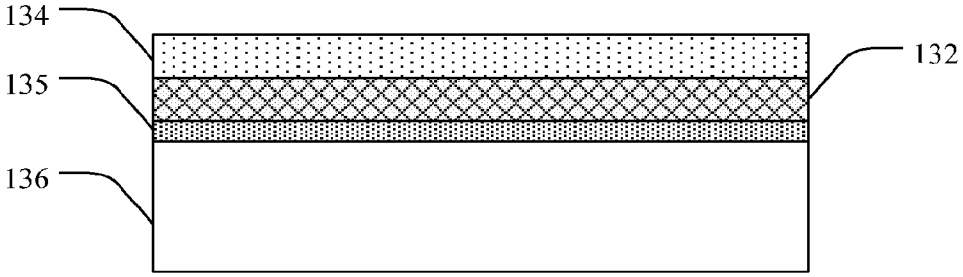

FIG. 13D

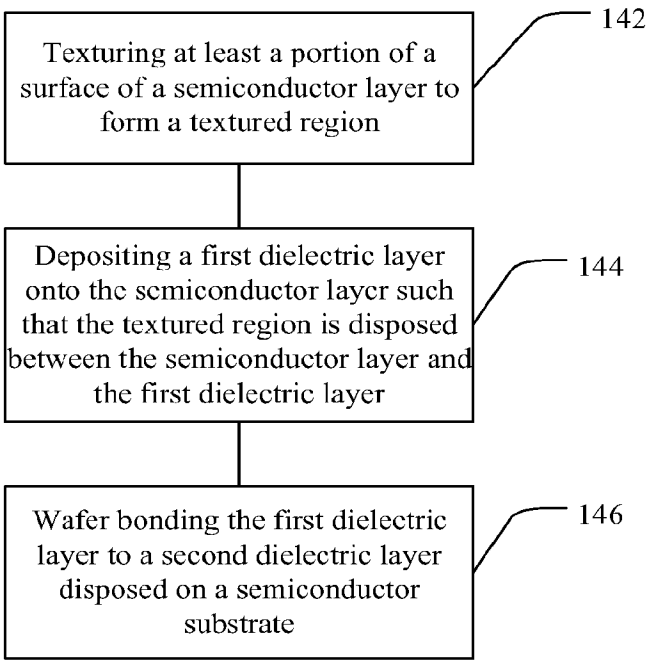
Texturing at least a portion of a surface of a semiconductor layer to form a textured region
142
Depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer
144
Wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate
146

FIG. 14

(12) 按照专利合作条约所公布的国际申请

(19) 世界知识产权组织
国 际 局

(43) 国际公布日
2012 年 12 月 27 日 (27.12.2012)

WIPO | PCT

(10) 国际公布号
WO 2012/174752 A1

(51) 国际专利分类号:
H01L 27/146 (2006.01) *H04N 5/335* (2011.01)

(21) 国际申请号: PCT/CN2011/076338

(22) 国际申请日: 2011 年 6 月 24 日 (24.06.2011)

(25) 申请语言: 中文

(26) 公布语言: 中文

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(84) 指定国 (除另有指明，要求每一种可提供的地区保护): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), 欧亚 (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), 欧洲 (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)。

本国际公布:

— 包括国际检索报告(条约第 21 条(3))。

(54) **Title**: MULTI SCENE DEPTH PHOTO SENSITIVE DEVICE, SYSTEM THEREOF, SCENE DEPTH EXPANDING METHOD, AND OPTICAL IMAGING SYSTEM

(54) **发明名称** : 多景深感光器件、系统、景深扩展方法及光学成像系统

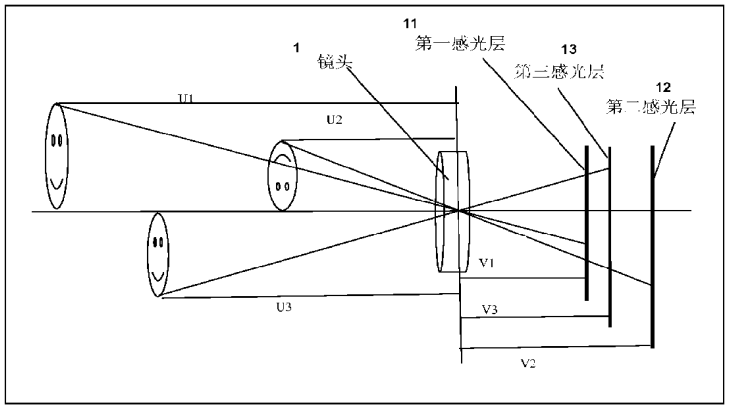

图 13 / FIG. 13

1 LENS
11 THE FIRST PHOTOSENSITIVE LAYER
12 THE SECOND PHOTOSENSITIVE LAYER
13 THE THIRD PHOTOSENSITIVE LAYER

(57) **Abstract**: A multi scene depth photo sensitive device, system thereof, scene depth expanding method and an optical imaging system are provide. The multi scene depth photo sensitive device comprises at least two photo sensitive pixel layers which can sense a light source, and the at least two photo sensitive pixel layers are disposed at a predetermined distance so that the different optical signals from the lens disposed at a a certain distance from the photo sensitive device can be focused on the different photo sensitive pixel layers. It is possible to realize focus automatically while avoiding utilizing electrodynamic element and mechanical element.

(57) **摘要**: 提供一种多景深感光器件、系统、景深扩展方法及光学成像系统。多景深感光器件包括至少两个可感应到光源的感光象素层，至少两个感光象素层之间按预定的距离间隔设置，使来自距离感光器件特定距离的镜头的不同光信号被聚焦到不同的感光象素层。可以避免使用电动机构和机械部件而实现自动对焦。

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说 明 书

多景深感光器件、系统、景深扩展方法及光学成像系统

技术领域

本发明涉及感光领域，具体的说，涉及一种多景深感光器件、利用该多景深感光器件的感光系统、景深扩展方法以及一种光学成像系统与方法。

背景技术

本发明是本发明人稍早一点的《多光谱感光器件及其制作方法》（PCT/CN2007/071262），《多光谱感光器件及其制作方法》（中国申请号：200810217270.2），《多光谱感光器件》（中国申请号：200910105372.X），《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2），《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7）的延续，旨在提供更为具体而且优选的多光谱感光器件在芯片及系统级别的实现。

感光系统，是一种通过光学镜头进行景物的捕捉、收集，并由感光器件，例如CMOS感光芯片进行景物的记录的系统。感光系统工作时，调节镜头，使距离镜头一定距离的景物清晰成像的过程，叫做对焦，该景物所在的点，称为对焦点，因为“清晰”具有相对性，所以对焦点前（靠近镜头）、后一定距离内的景物的成像都可以是清晰的，这个前后范围的总和称为景深。通常前景深小于后景深，即精确对焦后，对焦点前只有很短一段距离内的景物能清晰成像，而对焦点后很长一段距离内的景物都是清晰的。

获得宽景深清晰成像的系统是人们长期以来的研究目标之一。研究表明，景深的大小与镜头焦距有关，焦距长的镜头景深小，焦距短的镜头景深大。可见，镜头焦距调整是获得宽景深清晰成像的手段之一；另外，根据几何光学的基本成像公式（$\frac{1}{f}=\frac{1}{u}+\frac{1}{v}$，其中，f为镜头焦距，u为物距，即被摄物到镜头的距离，v为象距，即镜头到感光器件的距离），可见，象距的动态调整也是获得宽景深清晰成像的手段之一。

因此，现有感光系统中的自动对焦方式，都采用上述两种手段之一。例如，镜头由一组镜片构成，通过调整镜片之间的距离，从而可以调整镜头焦距或（镜头与感光器件的）象距（而实现光学变焦或对焦）；或者通过驱

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动例如 CMOS 感光器件位移，从而改变象距（而实现光学对焦）。然而，显然的，这两种方式的对焦，都需要电动机构和复杂、精密的机械部件来进行镜片或感光器件的位移驱动。这样，不仅显著增加了尺寸，也显著增加了成本和功耗。在很多的应用里，如手机照相和医用照相里，这些都是明显的不利因素。

一些不采用运动机构的宽景深系统因此被提出，试图在某些应用里取代自动对焦的需求。这种系统在手机照相的应用里，被称之为 EDoF (Extended Depth of Focus)，例如，DXO 公司提出的一种 EDoF 系统，通过特别的镜头设计，让感光器件中的红色感光象素聚焦在无穷远处，兰色感光象素聚焦在尽可能的近距(例如 50cm) 。而绿色感光象素聚焦在某个中间的位置。这样，无论物体处于哪个位置，总有一个颜色的图像是清楚或相对比较清楚的。之后，通过数学的手段，以比较清楚的颜色为主体，不够清楚的颜色为辅助信息，就能在比较宽的范围，还原和计算出较清楚的图像。

然而，采用单层感光器件，当红色感光象素聚焦在无穷远时，兰色感光象素的聚焦距离一般很难做得比 50cm 更小。此外，对于采用贝叶图案的感光器件，红色象素和兰色象素都只占感光象素的 1/4。因此，当需要以红色或兰色作为清晰度计算的主体时，图像的分辨率已经减少到以绿色为主体时的分辨率的一半以下。可见，这种方案有一定的局限性。

因此，仍然有必要对现有感光器件或系统进行改进。

发明内容

本发明所要解决的技术问题是，提供一种多景深感光器件、利用该多景深感光器件的感光系统、景深扩展方法以及一种光学成像系统与方法，其以物理的手段实现了自动对焦或多距离成像，避免使用电动机构和复杂、精密的机械部件，具有良好的景深扩展性能。

为解决上述技术问题，本发明采用了以下技术方案:

一种多景深感光器件，包括至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自距所述感光器件特定距离的镜头的不同光信号被聚焦到不同的所述感光象素层。

在本发明的一种实施例中，所述感光象素层包括化学镀膜感光象素层和半导体感光象素层中的至少一者。

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在本发明的一种实施例中，所述化学镀膜感光象素层包括量子点感光象素。

在本发明的一种实施例中，所述半导体感光象素层包括 CMOS 光敏二极管、CMOS 感光门、CCD 光敏二极管、CCD 感光门、和具有双向电荷转移功能的 CMOS 和 CCD 感光二极管和感光门。

在本发明的一种实施例中，所述不同光信号，包括不同距离的光信号，或者不同波长的光信号。

在本发明的一种实施例中，波长更短的光信号被聚焦到离镜头更近的感光象素层。

在本发明的一种实施例中，所述感光象素层为两层，紫色光、兰色光、绿色光、或青色光被聚焦到离镜头较近的感光象素层，绿色光、红色光、黄色光、可见光、或红外光被聚焦到离镜头较远的感光象素层。

在本发明的一种实施例中，所述感光象素层为三层，紫外光、兰色光、或青色光被聚焦到离镜头最近的感光象素层；兰色光、绿色光、红色光、或黄色光被聚焦到位于中间的感光象素层；红色光、黄色光、可见光、或红外光被聚焦到离镜头最远的感光象素层。

在本发明的一种实施例中，更远距离的光信号被聚焦到离镜头更近的感光象素层。

在本发明的一种实施例中，所述感光象素层为两层，无穷远处的光信号被聚焦到离镜头较近的感光象素层，感兴趣最短距离的光信号被聚焦到离镜头较远的感光象素层。

在本发明的一种实施例中，无穷远处的紫色光、兰色光、绿色光、或青色光被聚焦到离镜头较近的感光象素层，感兴趣最短距离的绿色光、红色光、黄色光、可见光、或红外光被聚焦到离镜头较远的感光象素层。

在本发明的一种实施例中，所述感光象素层为三层，无穷远处的光信号被聚焦到离镜头最近的感光象素层，感兴趣最短距离的光信号被聚焦到离镜头最远的感光象素层，无穷远处与感兴趣最短距离之间的一个中间距离的光信号被聚焦到位于中间的感光象素层。

在本发明的一种实施例中，所述感光象素层为三层，无穷远处的紫外光、兰色光、或青色光被聚焦到离镜头最近的感光象素层，感兴趣最短距离的红色光、黄色光、可见光、或红外光被聚焦到离镜头最远的感光象素层，无穷远处与感兴趣最短距离之间的一个中间距离的兰色光、绿色光、红色光、或黄色光被聚焦到位于中间的感光象素层。

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在本发明的一种实施例中，所述感兴趣最短距离包括 2mm，5mm，7mm，1cm，2cm，3cm，5cm，7cm，10cm，20cm，30cm，40cm，50cm，60cm，70cm，80cm，100cm，或 150cm。

在本发明的一种实施例中，至少两个所述感光象素层之间设置有透光层。

在本发明的一种实施例中，所述感光象素层中的感光象素为正面感光象素、背面感光象素、或双向感光象素。

在本发明的一种实施例中，当感光象素为双向感光象素时，其感光选向方式为隔离选向、分时选向、分区选向、或象素选向。

在本发明的一种实施例中，所述感光象素层中的感光象素分别感应包含紫外线、可见光、近红外、和远红外中的一个互补谱段或子谱段；或者所述化学镀膜感光象素和半导体感光象素分别感应包含紫外线、可见光、近红外、和远红外中的一个正交谱段或子谱段。

在本发明的一种实施例中，所述互补谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近红外光谱+远红外光谱，黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱；

所述正交谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近红外光谱+远红外光谱，黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱。

在本发明的一种实施例中，每一感光象素层中的色彩排列包括同一排列、水平排列、垂直排列、对角排列、广义贝叶排列、YUV422 排列、横向 YUV422 排列、蜂窝排列、均布排列。

在本发明的一种实施例中，至少一个所述感光象素层中的部分或全部感光象素的正面、背面或双面设置有滤光膜，所述滤光膜的选频特性包括红外截止滤波、兰色带通、绿色带通、红色带通、青色带通、黄色带通、品红色带通、或可见光带通。

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在本发明的一种实施例中，所述感光象素层中的相邻两层各自设有读取电路；或者所述感光象素层的相邻两层共用读取电路。

在本发明的一种实施例中，所述读取电路为主动象素读取电路、被动象素读取电路、或主动象素与被动象素混合读取电路。

在本发明的一种实施例中，所述主动象素包括 3T、4T、5T 或 6T 主动象素。

在本发明的一种实施例中，所述读取电路的共用方式包括单层或上下层 4 点共享方式、单层或上下层 6 点共享方式、单层或上下层 8 点共享方式、或单层或上下层任意点共享方式。

在本发明的一种实施例中，所述读取电路包括用于对每一感光象素层的象素阵列中的紧邻的同行异列、异行同列、或异行异列的象素间进行两两合并采样，获得第一合并象素的采样数据的第一合并单元；以及用于对第一合并单元得到的第一合并象素的采样数据进行合并采样以获得第二合并象素的采样数据的第二合并单元。

在本发明的一种实施例中，所述读取电路还包括第三合并单元，用于对第二合并单元得到的第二合并象素的采样数据进行合并采样以获得第三合并象素的采样数据。

在本发明的一种实施例中，所述第一合并单元或第二合并单元的象素合并方式为相同或不同色彩象素间的电荷相加方式或信号平均方式，其中不同色彩象素间的象素合并方式遵照色彩空间变换的方式，以满足色彩重建的要求。

在本发明的一种实施例中，所述色彩空间变换包括 RGB 到 CyYeMgX 空间的变换、RGB 到 YUV 空间的变换、或 CyYeMgX 到 YUV 空间的变换，其中 X 为 R(红)、G(绿)、B(兰)中的任一种。

在本发明的一种实施例中，所述电荷相加方式通过象素直接并联或将电荷同时转移到读取电容（FD）中完成。

在本发明的一种实施例中，所述第一合并单元或第二合并单元的基于色彩的合并采样方式包括同色合并方式、异色合并方式、混杂合并方式、或选择性抛弃多余色彩合并方式，且第一合并单元和第二合并单元采用的合并采样方式不同时为同色合并方式。

在本发明的一种实施例中，所述第一合并单元或第二合并单元的基于位置的合并采样方式包括以下几种方式中的至少一种：直接输出到总线的信号自动平均方式、跳行或跳列方式、和逐个采样方式。

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在本发明的一种实施例中，所述第三合并单元的合并采样方式包括：色彩空间变换方式和后端数字图像缩放方式中的至少一种。

在本发明的一种实施例中，包括具有跨层读取功能的全局电子快门，所述全局电子快门包含多个可同时转移并读取一层或多层感光象素层的电荷或电压值的不感光的转移和读取象素。

在本发明的一种实施例中，所述多个不感光的转移和读取象素位于不感光象素转移和读取层；或者位于所述感光象素层。

在本发明的一种实施例中，每一感光象素层，设置有一个紧邻的不感光象素转移和读取层。

在本发明的一种实施例中，所述不感光的转移和读取象素由半导体电路制成。

本发明也提供了一种景深扩展方法，包括：

在感光器件中设置至少两个可感应到光源的感光象素层，并将至少两个所述感光象素层按预设距离间隔布置，使得来自距所述感光器件特定距离的镜头的不同光信号被聚焦到不同的所述感光象素层。

在本发明的一种实施例中，通过来自不同感光象素层的具有不同清晰度的图像而获取一幅清晰图像。

本发明还提供了一种光学成像方法，包括：

设置镜头和包括至少两个可感应到光源的感光象素层的感光器件；将所述感光器件放置在距所述镜头特定距离，且至少两个所述感光象素层之间按预设距离间隔布置，使得来自镜头的不同光信号被聚焦到不同的所述感光象素层。

本发明还提供了一种光学成像系统，包括镜头和多景深感光器件，所述多景深感光器件布置在距所述镜头特定距离，包括至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自所述镜头的不同光信号被聚焦到不同的所述感光象素层。

在本发明的一种实施例中，所述不同光信号，包括不同距离的光信号，或者不同波长的光信号。

在本发明的一种实施例中，波长更短的光信号被聚焦到离镜头更近的感光象素层。

在本发明的一种实施例中，更远距离的光信号被聚焦到离镜头更近的感光象素层。

本发明还提供了一种感光系统，包括上述的感光器件。

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在本发明的一种实施例中，所述感光系统包括数码相机，照相手机，摄像机，视频或照相监控系统，图像识别系统，医学图像系统，军用、消防或井下图像系统，自动跟踪系统，立体影像系统，机器视觉系统，汽车视觉或辅助驾驶系统，电子游戏系统，网络摄像头，红外和夜视系统，多光谱成像系统，和电脑摄像头中的一种。

现有的感光系统，不仅自动对焦系统需要电动机构和复杂、精密的机械部件，而且对于 6mm 直径以上的镜头而言，为了实现在 10cm 至无穷远的宽距自动对焦，镜头的行程必须在 0.2mm 以上，也就是说，无穷远处清晰成像的象距与 10cm 处清晰成像的象距差，至少是 0.2mm，即 200um。众所周知，硅或其它半导体材料都是不透明的。光进入硅后，大约在 12um 处，就已经被吸收得所剩无几了。因此即使使用自动对焦系统，现有的感光系统也很难获得较宽的景深范围。

本发明的多景深感光器件、利用该多景深感光器件的感光系统、景深扩展方法，以及光学成像系统及方法，通过设置至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自距感光器件特定距离的镜头的不同光信号被聚焦到不同的感光象素层，从而不同感光象素层可以得到不同景深的图像。从产品角度，感光器件可以制作成感光芯片独立存在，但从应用角度，例如光学成像，感光器件通常需要与镜头配合使用。镜头，依其大小、材料、曲面设计等具有不同的聚焦特性，例如以普通的手机镜头为例，其景深范围通常是无穷远到 2m，超出该景深范围，则需要采用自动对焦技术，例如通过调整感光器件到镜头的距离，也即调整象距到某一合适数据，才能获得例如 50cm-30cm 的清晰景象。而在本发明中，如果选定的应用镜头是手机镜头，则可以按下例在感光器件中设置两个感光象素层（称第一感光象素层和第二感光象素层），当与该选定的手机镜头配合时，感光器件被放置在距该镜头特定距离，此时，第一感光象素层到镜头的距离为第一象距，第二感光象素层到镜头的距离为第二象距（第一象距小于第二象距），此时，距镜头的特定距离以及两个感光象素层之间的预设距离，使得从无穷远到 2m 的景深范围的景物将可在第一感光象素层清晰成像，从 50cm-30cm 的景深范围的景物将可在第二感光象素层清晰成像。由此，实现了两个景深或景深扩展。需要注意的是，上述说明例中，感光象素层的数量和景深范围均仅为示例性数据，可以理解，通过对感光象素层的数量和相互间的预设距离调整，可以形成连

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续、交叠、互补、或正交的景深范围，多个感光象素层各自的景深范围叠加将使感光器件具有相当宽的景深范围，从而无需自动对焦即可获得宽景深范围内的清晰图像，避免使用电动机构和复杂、精密的机械部件，显著的节约了空间和成本。另一方面，在本发明中，通常至少可以从一个感光象素层获得较为完整的图像信息，从而图像具有相当高的清晰度，且无需繁琐的数学计算。

本发明将通过实施例描述这种新型的、威力巨大的混合多光谱感光象素组、感光器件和系统。这些优选实现方式，仅仅是作为举例来说明本发明的优点和实现方法而已，而不是为了限制这些发明的保护范围。

对于相关业界的有识之士而言，本发明的上述及其它目的和优点，在阅读过下面的优选的带有多个插图解释的实现案例的细节描述之后，将是十分明显的。

附图说明

图 1 是一个光谱分布的示意图。可见光一般是指 390nm 到 760nm 波长的光。一般由棱镜的分光效应而从可见光分出来看到的兰光波长在 440－490nm，绿光波长在 520－570nm，红光波长在 630－740nm，而在感光器件的设计中，一般把 390－500nm 划为兰色区，500-610nm 划为绿色区，610-760nm 划为红色区，但这种红、绿、兰的谱段的划分并不是绝对的。图中的红、绿、兰、青（兰绿复合）、和黄（绿红复合）的波形，是原色感光象素或补色（复合色）感光象素所需求的理想的波长响应曲线。如果作为基色的原色感光象素或补色（复合色）感光象素不具备类似的波长响应曲线，则很难重建人类所能看到绝大部分色彩。

图 2 是感光象素的 3T 读取电路。

图 3 是感光象素的 4T 读取电路。

图 4 是本人在《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2）和《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7）提出的四点共享读取电路。

图 5 是本人在《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2）和《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7）提出的两层六点共享读取电路。

图 6 是本人在《一种多光谱感光器件及其采样方法》（中国申请号：

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200910105948.2）和《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7）提出的两层八点共享读取电路。

图 7 是本人在《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7）提出的任意 N 点共享读取电路。

图 8 是本人在《多光谱感光器件及其制作方法》（中国申请号：200810217270.2）和《多光谱感光器件》（中国申请号：200910105372.X）中提出的，上下层感光象素在感兴趣的光谱上互补或正交的双层感光器件的示意图。这种感光器件通过采用精心选择的彩色图案和排列，可以得到非常多优秀的双层感光器件。这些感光器件可以用于正面感光，背面感光，和双向感光。这些方法和原理，同样也可适用于本发明的多光谱感光器件。

图 9 是本人在《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2）中提出的一种在不同色彩象素间实现电荷合并的子采样方法。这种方法同样适用于本发明的多光谱感光器件。

图 10 是本人在《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2）中提出的采用色彩空间变换来实现的一种象素合并和子采样方法。这种方法同样适用于本发明的多光谱感光器件。

图 11 是本发明提出的一种用于景深扩展的两层感光器件的结构示意图，其中透光层的厚度，由所希望的两个感光平面的象距差（V2-V1）来决定。

图 12 是本发明提出的一种用于景深扩展的三层感光器件的结构示意图，其中透光层的厚度，由所希望的两个感光平面的象距差（V2-V1 或 V3-V2）来决定。

图 13 是第一种利用多层感光器件实现景深扩展的原理示意图。在这个示意图里，位于不同距离的物体，将清晰地聚焦在多层感光器件的不同感光象素层。因此，位于这三个距离之间的任一物体，都将清楚或者比较清楚地聚焦在一个，或者两个感光象素层，从而达到景深扩展的效果。图中，U1，U2，U3 是物距（即物体到镜头的距离），V1，V2，V3 是象距（即感光象素层到镜头的距离）。

图 14 是第二种同时利用特殊的镜头设计方法和多层感光器件来实现更好的景深扩展效果的原理示意图。对一般光学系统而言，波长更短的光，焦距更短。因此，对镜头进行特别的设计，可以让波长更短的光，聚焦在离镜头更近的感光象素层，或者说，离光源更近的感光象素层；而将波长更长

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的光，聚焦在离镜头更远的感光层，或者说，离光源更远的感光象素层；而将波长中等的光，聚焦在中间的感光层。这样，这种成像系统同时结合多光谱和多象距的特点，就能极大地扩展景深。这种系统，对于微距照相，有着无比的优势。

图 15 是实现图 11 所示的多景深感光器件的感光象素级别的原理示意图。通过调整透光层的厚度，可以调整两个感光象素层之间的距离，从而让两个感光象素层的感光象素，分别对应不同的景深。该例中，上下两个感光象素层均采用半导体感光象素层。

图 16（a）、（b）、（c）、（d）是实现图 11 所示的多景深感光器件的另一种感光象素级别的原理示意图。同样，通过调整透光层的厚度，可以调整两个感光象素层之间的距离，从而让两个感光象素层的感光象素，分别对应不同的景深。该例中，上层的感光象素层采用化学镀膜感光象素层，而下层的感光象素层采用半导体感光象素层，显然二者可以互换而不影响其实现多景深的效果。

图 15 和图 16 都只描绘了感光象素的情况，其它读取电路和辅助电路，因为可以与现有的相同，都被省略。

图 17（a）、（b）、（c）、（d）是实现图 11 所示的多景深感光器件的另一种感光象素级别的原理示意图。同样，通过调整透光层的厚度，可以调整上层的一个感光象素层与下层的另两个感光象素层之间的距离，从而让不同感光象素层的感光象素，分别对应不同的景深。在该例中，上层的一个感光象素层采用化学镀膜感光象素层，下层的另两个感光象素层采用半导体感光象素层，注意到，图 17（a）、（b）中的两个半导体感光象素层布置在一个半导体基层的两面，图 17（c）、（d）中的两个半导体感光象素层布置在一个半导体基层的一面。照射方向可以是该半导体基层的正面或是背面。另需注意的是，由于半导体的透光性限制，半导体基层厚度一般较薄，通常不满足景深扩展所需的感光象素层间隔距离的需求。因此，两个半导体感光象素层更多的用来实现多光谱的需求。

图 18（a）、（b）是实现图 11 所示的多景深感光器件的另一种感光象素级别的原理示意图。同样，通过调整透光层的厚度，可以调整上层的一个感光象素层与下层的另两个感光象素层之间的距离，从而让不同感光象素层的感光象素，分别对应不同的景深。在该例中，上层的一个感光象素层采用化学镀膜感光象素层，下层的另两个感光象素层分别采用半导体感

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光象素层和化学镀膜感光象素层。中间的半导体感光象素层（的两面）可以含有读取三个感光象素层所必需的读取象素和采样电路。

图 19（a）、（b）是实现图 12 所示的多景深感光器件的一种感光象素级别的原理示意图。注意到，在该例中，从上到下依次布置化学镀膜感光象素层、第一透光层、第一半导体感光象素层、第二透光层、第二半导体感光象素层。第一半导体感光象素层和第二半导体感光象素层分别实现在不同的两个半导体基层上，化学镀膜感光象素层与第一半导体感光象素层之间的距离通过调整第一透光层的厚度实现，第一半导体感光象素层与第二半导体感光象素层之间的距离通过调整第二透光层的厚度实现。读取和采样电路可以在位于中间的第一半导体感光象素层实现，也可以分布在两个半导体感光象素层。

对于具有两层半导体感光象素层的实施例，例如图 8 和图 15 等，如果将其中一个感光象素层中的感光象素去掉，做成专门用于读取电路和信号处理的层，则可以得到如图 20-23 所示的本发明提出的带有(具有跨层读取功能的)全局电子快门的感光器件。图 20-23 仅是展示了该带有(具有跨层读取功能的)全局电子快门的感光器件的感光象素层和不感光的转移和读取象素层，显然，结合前述，当保留定焦在不同景深的多个感光象素层时，则可以得到带有(具有跨层读取功能的)全局电子快门的多景深感光器件。

图 20 是本发明提出的两行共用一行转移象素（读取电容）的示意图。这实际上是《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7)中隔行扫描方式的一种新的实现。在这里，转移象素和感光象素不在同一层，因而可以获得更好的感光面积的使用效率，但同时增加了一倍的快门速度。重要的是，这种方式可以用于以化学感光材料(如量子感光膜)为感光象素层的感光器件。

图 21 是利用半导体的不良透光性能，将半导体基层厚度增加到一定厚度，使得下层的象素感不到光。然后，利用金属穿孔或是表面走线，外部连接的方式，将上层的感光象素信号，通过二极管或读取放大开关电路引到不感光象素层的读取象素上，在那里进行采样读取，从而将一个两层的感光器件退化成一个(具有跨层读取功能的)全局电子快门的单层感光器件。这个器件在结构上是双层的，但在效果上却是单层的。当这种方式用于图 17(a)所示的多层感光器件时，就能得到(具有跨层读取功能的)全局

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电子快门的多景深感光器件。

图 22 是本发明提出的以传统的(CMOS 和 CCD)半导体电路为基础的带有（具有跨层读取功能的）全局电子快门的多光谱两层感光器件的示意图。同样地，感光象素信号到不感光读取象素上的转移，由二极管或放大开关电路来控制的。

图 23 是本发明提出的另一种以化学感光材料(如量子感光膜)为基础的带有（具有跨层读取功能的）全局电子快门的多光谱两层感光器件的示意图，其中感光象素层采用化学感光材料(如量子感光膜)，而读取电路和信号处理层则是 CMOS 半导体层。注意到在该图示例中，每一个感光象素都对应有一个不感光的电荷转移象素，用于实现全局电子快门。这也是多层感光器件的为简单实现全局电子快门而特意进行的一种退化。

图 24 是本人在《一种感光器件及其读取方法、读取电路》(中国申请号：200910106477.7)提出的一种同时采用主动象素和被动象素来读取感光象素信号的读取电路。采用这种方法的好处是，能够极大地扩大感光器件的动态范围，并且成倍地节省图像预览时的功耗。这种混合读取电路在高灵敏度的多层多光谱感光器件和带有全局电子快门的多光谱感光器件里尤其有用。

图 25 是《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2）中用来描述该发明中提出的象素合并和子采样方法的采样控制电路示意图。本发明也将用到这种新型的象素合并和子采样方法。

具体实施方式

下面通过具体实施方式结合附图对本发明作进一步详细说明。

本发明将提出的多景深感光器件，其主要用途是景深扩展，即手机行业里目前所称的 EDoF(即 Extended Depth of Focus)。景深扩展尤其在照相手机中有着非常广泛的应用，然而，目前的景深扩展主要使用光学和数学手段，通常是利用光学变焦或自动对焦的方式实现景深调整，这要求电动机构和复杂、精密的机械部件的配合，因而将显著增加空间和成本。

本发明实施例所提出的多景深感光器件，结合多层感光器件的实现，包括至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自距感光器件特定距离的镜头的不同光信号被聚焦到不同的感光象素层，从而不同感光象素层构成了具有不同象距的

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感光平面，可以定焦不同的景深，由此扩展了感光器件的景深范围，相当于从多点光学对焦这一物理手段上实现了自动对焦，相应可以去除电动机构和复杂、精密的机械部件的配合，显著地节省了空间和成本。

所述感光象素层，包括化学镀膜感光象素层和半导体感光象素层中的至少一者。即上述至少两个感光象素层，可以全部是化学镀膜感光象素层，或者全部是半导体感光象素层，或者部分是化学镀膜感光象素层，部分是半导体感光象素层。其中，化学镀膜感光象素层包括量子点感光象素。半导体感光象素层包括 CMOS 光敏二极管、CMOS 感光门、CCD 光敏二极管、CCD 感光门、和具有双向电荷转移功能的 CMOS 和 CCD 感光二极管和感光门。

上述的感光象素层，分别用来感应不同的光信号。本发明中，关注的光信号特性主要包括光信号的频谱特性，即光的波长，以及光信号的距离特性，即光信号到镜头的距离。因此，光信号的不同，是指两个光信号之间，上述两个特性中至少有一者不同，即两个光信号之间，可能是波长不同，或者距离不同，或者波长和距离都不同。当然，由于自然界常见复色光，例如白光，因此如果需要得到不同波长的光，一般需要配合镜头设计，利用例如棱镜的分光效应，镜头材料或曲面设计对不同波长的光的不同折射率从而使不同波长的光分离并聚焦在不同的感光象素层上。

在聚焦不同波长的光信号的时候，一般地，波长更短的光信号被聚焦到离镜头更近的感光象素层。例如，感光象素层为两层，则聚焦在离镜头较近的感光象素层的光信号是紫色、兰色光、青色、或绿色光，聚焦在离镜头较远的感光象素层的光信号是绿色光、红色光、黄色光、可见光(白色光)、或红外光。又如，感光象素层为三层，则聚焦在离镜头最近的感光象素层的光信号是紫外光、兰色光、或青色光；聚焦在位于中间的感光象素层的光信号是绿色光、兰色光、黄色光、红色光、或可见光(白色光)；聚焦在离光源最远的感光象素层的光信号是红色光、黄色光、可见光、或红外光。

在聚焦不同距离的光信号的时候，一般地，更远距离的光信号被聚焦到离镜头更近的感光象素层。例如，感光象素层为两层，聚焦在离光源较近的感光象素层的是无穷远处的光信号，聚焦在离光源较远的感光象素层的是感兴趣最短距离的光信号。结合聚焦不同波长的光，还可以进一步设置为：无穷远处的紫外光、兰色光、青色光、或绿色光被聚焦到离光源较近的感光象素层；感兴趣最短距离的绿色光、红色光、黄色光、可见光(白

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色光)、或红外光被聚焦到离光源较远的感光象素层。

又如，感光象素层为三层，聚焦在离光源最近的感光象素层的是无穷远处的光信号，聚焦在离光源最远的感光象素层的是感兴趣最短距离的光信号，聚焦在位于中间的感光象素层的是无穷远处与感兴趣最短距离的一个中间距离的光信号。结合聚焦不同波长的光，还可以进一步设置为：无穷远处的紫外光、兰色光、青色光、或绿色光被聚焦到离光源最近的感光象素层；无穷远处与感兴趣最短距离的一个中间距离的绿色光、兰色光、黄色光、红色光、或可见光(白色光)被聚焦到位于中间的感光象素层；感兴趣最短距离的红色光、黄色光、可见光、或红外光被聚焦到离光源最远的感光象素层。

实施方式中，感兴趣最短距离包括 2mm，5mm，7mm，1cm，2cm，3cm，5cm，7cm，10cm，20cm，30cm，40cm，50cm，60cm，70cm，80cm，100cm，150cm。所谓感兴趣最短距离，是指用户关注的景物到镜头的最近距离。例如，感兴趣最短距离是 2mm，是指用户关注的景物到镜头的最近距离是 2mm，当景物到镜头的距离小于 2mm，则不再关注。

图 13 显示了距离与聚焦平面的关系。在该图中，位于不同距离的物体，将清晰地聚焦在多层感光器件的不同感光象素层。因此，位于这三个距离之间的任一物体，都将清楚或者比较清楚地聚焦在一个，或者两个感光象素层，从而从同一个感光器件，能够同时得到它们的清晰图像。

图 14 显示了波长与聚焦平面的关系，对一般光学系统而言，波长更短的光，焦距更短。因此，通过对镜头进行设计，可以让波长更短的光，聚焦在离镜头更近的感光象素层；波长更长的光，聚焦在离镜头更远的感光象素层；波长中等的光，聚焦在中间的感光象素层。这样，处于不同距离的物体，总有一个颜色，在一个感光层中是清楚的。于是，这种成像系统同时结合了多光谱和多象距的特点，每个感光层有自己的景深范围，并且对于不同波长的光，景深距离和范围不同，可以将各个感光层的景深范围进行整合，能够极大地扩展景深，对于微距照相，有着无比的优势。

由于可以从不同感光象素层得到具有不同清晰度的多个图像，因而这些图像之间可以相互参照，通过图像的整合、选用和舍弃，以及插值、增强、或反卷积等数学处理，而获得清晰的图像。

实施方式还包括在上述多景深感光器件中，实现一种具有跨层读取功能的全局电子快门，包括多个不感光的转移和读取象素，所述不感光的转移和

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读取象素的每一个能够用来转移和读取处在其它层的至少一个感光象素的电荷或电压值。从而多个不感光的转移和读取象素可同时转移并读取一层或多层感光象素层的电荷或电压值。多个不感光的转移和读取象素可以与感光象素位于同一象素层，显然，这意味着该象素层的感光灵敏度的下降。多个不感光的转移和读取象素也可以与感光象素位于不同的象素层，即形成独立的感光象素层和独立的不感光的转移和读取象素层，显然，这意味该具有跨层读取功能的全局电子快门只能在两层或多层感光器件中实现。

可以为每一个感光象素层设置一个紧邻的对应的不感光象素转移和读取层，所述不感光象素转移和读取层可同时转移对应的感光象素层的所有象素的电荷或电压值；或者可同时转移对应的感光象素层的奇数行或偶数行象素的电荷或电压值。图 20 显示了两行共用一行读取电容的设计，以实现逐行扫描的功能。不感光的转移和读取象素层，可以半导体电路做成。

图 21 显示了一种两层感光器件的退化实现，以获得单层的带有全局电子快门的单层感光器件。这种方法利用了半导体材料的不良透光性，将两半导体基层加厚，使得底层感不到光，而只能用于做象素读取。将这个方法用于图 17(a)所示的三层感光器件时，就能得到带全局电子快门的两层多景深感光器件。

图 22 和图 23 显示了一种具有跨层读取功能的全局电子快门的象素级别的实现。

文中出现的远近，上下等位置关系，均是指以光源为基准的相对位置。例如，上层感光象素层和下层感光象素层的描述，是指感光象素层水平放置，光源从上方垂直照射向感光象素层而言。显而易见，本文中的上下关系实际上具有更加广泛的含义，即，例如感光面垂直放置，光源从左侧或右侧，或者从前侧或后侧垂直照射向感光面，则所谓的上下关系，则等同于前后关系或者左右关系。不失一般性，本领域技术人员可以理解，其中的上方、下方等描述，可以用左侧、右侧、前侧、后侧等描述进行等同的替代。不同种类的感光象素层，如化学镀膜感光象素层或半导体感光象素层，其上下关系并无限制，何者处于上方，何者处于下方是可以根据需要任意设置的。下文所述的基层顶面和底面，同样表达类似含义，即以水平放置，光源从上方垂直照射向基层而言，此时，位于上方的基层表面称为顶面，位于下方的基层表面称为底面。可以理解，当基层垂直放置，光源从左侧或右侧，或者从前侧或后侧垂直照射向基层时，可等同替代为前侧

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面和后侧面，左侧面和右侧面的表述。

此外，也需特别注意术语“可感应到光源”和“感光”之间的差异，感光象素层的“感光”，指的是该象素具有感光能力，“可感应到光源”，指的是感光象素是否能够感应到光源的结果，即感光象素的感光能力是否得到发挥，例如，由于半导体的透光性限制，当在一个半导体基层的顶面和底面各布置一个半导体感光象素层时，如果该半导体基层厚度超出半导体的透光性限制，则光源向该半导体基层照射时，只有顶面的半导体感光象素层能够感应到光源，而底面的半导体感光象素层受半导体基层厚度限制而无法感应到光源，则称顶面的半导体感光象素层为可感应到光源的感光象素层，即感光象素的感光能力得以发挥；称底面的半导体感光象素层为不可感应到光源的感光象素层，即感光象素的感光能力未能发挥。注意到在后文中，利用不可感应到光源的感光象素层，可以形成不感光的转移和读取象素层。

当化学镀膜感光象素或半导体感光象素为双向感光象素时，则涉及到感光选向问题，即尽管能够双向感光，但不能接受同一时刻两个方向的光照，需要在一个时刻选择一个方向的光源照射，感光选向方式可以为隔离选向、分时选向、分区选向、或象素选向等等，也就是说，可以通过例如遮光膜遮挡等方式来实现分时刻、分区域、分象素的感光选向。双向照射的情况, 例如图 8 所示。

感光象素层，大致相当于垂直于光源照射方向的感光平面，在这样的感光平面中，布置有多个感光象素（通常形成为多行多列的象素阵列），对于多个感光象素层中的每一感光象素层，其可能是平面混合型，也就是既布置有化学镀膜感光象素，也布置有半导体感光象素。另外的情形是，同一感光象素层中仅布置一种感光象素，如此，将形成化学镀膜感光象素层，或者半导体感光象素层。

在实施方式中，感光器件的同一位置（即由一层感光象素层的该象素位置上穿透而来的光照射到另一感光象素层上的位置）但不同层的感光象素，分别感应包含紫外线、可见光、近红外、和远红外中的一个互补谱段或子谱段；或者分别感应包含紫外线、可见光、近红外、和远红外中的一个正交谱段或子谱段。其中，互补谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近

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红外光谱+远红外光谱，黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱；

正交谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近红外光谱+远红外光谱，黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱。

实施方式包括让感光器件中至少一层感应两个不同的光谱(即射频)谱段。对于每一感光象素层而言，其象素阵列的色彩排列包括同一排列(象素阵列中的象素色彩相同)、水平排列(象素阵列中的同一行象素色彩相同)、垂直排列(象素阵列中的同一列象素色彩相同)、对角排列(象素阵列中的同一对角线的象素色彩相同)、广义贝叶排列(象素阵列中的一条对角线上的象素色彩相同，另外一条对角线上的象素色彩不同)、YUV422 排列、横向 YUV422 排列、蜂窝排列、均布排列(四个象素均匀交错等距排列)等。

需要注意的是，本文中的术语“布置”，包含了各种在例如半导体基层或透光层上形成化学镀膜感光象素层或半导体感光象素层的制作工艺。例如，半导体基层为一个 N 型硅晶体基板，在该基板一面上的一个象素位置，根据色彩的深度需求，由该象素位置表面向基板内部做一定深度的 P 杂质置入，形成一个 P 掺杂层，该 P 掺杂层即形成为一个半导体象素，如果在该 P 掺杂层做另一定深度的 N 杂质置入，形成在 P 掺杂层中的 N 掺杂层，该 N 掺杂层即形成为另一半导体感光象素(与前一 P 掺杂层的半导体感光象素在不同感光象素层，但象素位置相对应)，可以按照《多光谱感光器件及其制作方法》(PCT/CN2007/071262)提供的方法，在 390nm 附近，500nm 附近，610nm 附近，和 760nm 附近设置分层线，使得任一分层线上下的对应点象素感应互补或正交的光谱。图 1 给出了一个分层线的设置的例子，即通过不同深度的杂质掺入，形成不同的色彩。在基板的该面进行化学镀膜溶液的涂抹加工，可以形成化学镀膜感光象素层，由于制作或者加工工艺的多样性，在本文中均以“布置”进行表述。

上述的两层半导体感光象素在不同深度上的布置，实现了在基板一个

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表面上的同一象素位置可以感应到至少两个谱段，从而提供了在该表面上的象素图案排列上的更好的灵活性以及更多的象素布置，能够大幅提高感光器件的灵敏度,解析度,和动态范围。

对于上述在半导体基板某一面的不同深度的掺杂加工，其同一位置最多布置两层感光象素，这是由于在同一位置布置 3 层，加工上难度极大，同时在布线上，由于各层间的引线需要相互隔离，3 层引线显然造成了布线上的困难。而在本发明中，采用同一面上最多布置两层上述的半导体感光象素层，并可结合平面上的象素图案排列完成彩色重建，因而可以实现更好的彩色感光性能。由于同一面上最多以深度掺杂方式布置两个半导体感光象素层，因而明显降低了立体加工工艺的难度，且在布线上，也相对简单。

对于基板，可以采用单面或者双面加工工艺，从而形成单面感光器件或者双面感光器件。双面感光器件，对于上述的深度掺杂加工，如果采用两个半导体感光象素层一者布置在基板的顶面，另一者布置在基板底面的双面布置方式，则对于每一面而言，其都简化为平面加工工艺，可以在一面上完成一个感光象素层的平面加工后，将基板进行翻转而在另一面同样以平面加工工艺完成另一感光象素层的加工，使得加工工艺近似于现有的单面单层感光器件的加工工艺，相对于上述的同一面的两层掺杂的立体加工而言，更为简单。另一方面，沿光照方向，在基板的某一位置，可以布置多层感光象素。

半导体感光象素层通常制作在半导体基层上，为了实现景深扩展，在实际制作中，通常采用增设透光层（例如透明玻璃层）来调整不同感光象素层之间的距离，例如，在一半导体基层上制作一层或多层半导体感光象素层，而后在该半导体基层上放置一透光层，而后，在该透光层上涂抹加工出一层化学镀膜感光象素层。通过透光层的不同厚度设置，相当于预设化学镀膜感光象素层和半导体感光象素层之间的间隔距离，进而实现景深扩展。

在很多的应用里，在化学镀膜感光象素层或半导体感光象素层的正面，背面，或双面并不涂任何滤光膜。但在另外一些应用里，如对于色彩还原要求特别高的专业相机或摄像机，实施方式包括使用滤光膜的方式。滤光膜设置在化学镀膜感光象素层或半导体感光象素层中的全部或部分感光象素的正面，背面，或双面。滤光膜的选频特性包括红外截止滤波、兰

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色带通、绿色带通、红色带通、青色带通、黄色带通、品红色带通、或可见光带通。滤光膜的使用是通过牺牲少数象素的灵敏度，来去除不想要的光谱的影响，减少上下左右象素之间的干涉（crosstalk），或者获得正交性更好的三原色或是更纯正的补色信号。

实施方式包括让所述多景深感光器件的多层感光象素层的相邻两层各自使用自己的读取电路。

实施方式包括让所述多景深感光器件的多层感光象素层的相邻两层共用置于其中一层的读取电路。

实施方式包括让所述多景深感光器件的读取电路位于半导体感光象素层，或独立的读取电路层。

所述多景深感光器件的读取电路的实施方式包括采用《一种多光谱感光器件及其采样方法》（中国申请号：200910105948.2）和《一种感光器件及其读取方法、读取电路》（中国申请号：200910106477.7）中的象素读取和子采样方法。

实施方式包括在所述多景深感光器件的信号读取电路里采用主动象素读取电路、被动象素读取电路、或主动象素与被动象素混合读取电路。

所述主动象素包括 3T、4T、5T、或 6T 主动象素。3T 和 4T 的主动象素结构分别如图 2 和图 3 所示。

所述读取电路的共享方式包括无共享方式、单层或上下层 4 点共享方式、单层或上下层 6 点共享方式、单层或上下层 8 点共享方式、或单层或上下层任意点共享方式。4 点共享方式，6 点共享方式，8 点共享方式，和任意点共享方式，分别如图 4，图 5，图 6，和图 7 所示。

实施方式中，多景深感光器件的所述读取电路包括用于对每一感光象素层的象素阵列中的紧邻的同行异列、异行同列、或异行异列的象素间进行两两合并采样，获得第一合并象素的采样数据的第一合并单元；以及用于对第一合并单元得到的第一合并象素的采样数据进行合并采样以获得第二合并象素的采样数据的第二合并单元。

实施方式还包括：读取电路还包括第三合并单元，用于对第二合并单元得到的第二合并象素的采样数据进行合并采样以获得第三合并象素的采样数据。

在本发明的一种实施例中，所述的感光器件，所述第一合并单元或第二合并单元的象素合并方式为相同或不同色彩象素间的电荷相加方式或信号平均方式，其中不同色彩象素间的象素合并方式遵照色彩空间变换的方

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式，以满足色彩重建的要求。

上述的第一合并象素和第二合并象素来自于将子采样至少分为两个过程的处理，即第一合并采样过程和第二合并采样过程。第一合并采样过程和第二合并采样过程，通常发生在象素的行（合并）采样和列（合并）采样之间，主要对模拟信号进行，除电荷相加部分通常只在第一合并采样过程中做以外，其次序和内容通常是可以交换的。此外，也可以包括第三合并采样过程，第三合并采样过程发生在模数转换之后，主要对数字信号进行。

对于第一合并采样过程，是取象素阵列中两个紧邻的象素来进行合并。一方面，完成了紧邻象素的合并，将合并后的象素称为第一合并象素，需要理解的是，第一合并象素只是为本发明描述之便，利用该概念来指代进行第一合并过程后的象素，而不代表物理上，在象素阵列中存在一个“第一合并象素”;将两个紧邻象素合并采样后的数据称为第一合并象素的采样数据。紧邻，系指两个象素之间从水平，垂直，或对角方向上来看紧挨着，中间没有其它象素。紧邻的情况包含同行异列，异行同列，或异行异列。一般而言，在这种合并中，信号将至少是两个象素的信号平均，而噪声则会降低$\sqrt{N}$，因此，合并后，至少可以将信噪比提高$\sqrt{N}$倍，且这种合并可以在相同或不同色彩的象素之间进行。另一方面，由于两个合并的色彩可以不同，即色彩相加或平均，从色彩的三原色原理可知，两种原色的相加是另一种原色的补色，就是说，两个不同原色的象素合并，产生另一种原色的补色，从原色空间，变换到了补色空间，仅仅是发生了色彩空间变换，仍然可以通过不同的补色而完成彩色重建。也即通过这种方式，既能实现不同色彩的象素合并以提高信噪比，同时又能够进行彩色重建。整个子采样过程也因此得到优化，更加适应大数据量的象素阵列的高速需求。色彩空间变换的一个基本要求是，变换后的色彩的组合，能够（通过插值等手段）重建所需要的 RGB（或 YUV，或 CYMK）色彩。

需要了解，由于通常象素阵列包含多个象素，第一合并采样只是将两个象素进行合并，显然，合并形成的第一合并象素也具有多个。对于不同的第一合并象素，其采用的色彩合并方式可以相同，也可以不同。当第一合并全部在相同的色彩间进行时，我们将之称为同色合并方式；当第一合并全部在不同的色彩间进行时，我们将之称为异色合并方式；当第一合并部分在相同色彩间进行、部分在不同色彩间进行，我们将之称为混杂合并

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方式；当对象素阵列中的一些多余的色彩进行抛弃（当然，抛弃是选择性的，例如，不能因此而影响到彩色重建），这样的色彩合并方式称为选择性抛弃多余彩色方式。

显然的，第二合并过程是对多个第一合并象素的操作，同样的，可以将色彩相同的第一合并象素进行合并；也可以将色彩不同的第一合并象素进行合并（当然，这种情况下可能导致三原色的全部相加而无法重建出彩色）。

上述的同色合并、异色合并、混杂合并等方式，是将合并采样做基于色彩的分类，另外，从合并采样的位置选取的角度，第一合并过程和第二合并过程的合并采样方式包括：直接输出到总线的信号自动平均方式、跳行或跳列方式，逐个采样方式，以及这些方式的两种或三种的同时使用。除电荷相加部分通常只能在第一合并采样过程中做以外，第一合并过程和第二合并过程，除了次序的不同外，其方式都是相同和可以交换的。

所谓直接输出到总线的信号自动平均方式，就是，将需要合并的信号(色彩相同或是不同)，同时输出到数据采集总线上去，通过（电压）信号的自动平衡，来获得需要合并信号的平均值。所谓跳行或跳列方式就是跳过一些行或列，从而通过减少数据量的方式来实现（合并）采样。所谓逐个采样方式，实际上就是不做任何合并，依此读取原来的象素或第一合并象素。这三个方式有一些是可以同时使用的，例如，跳行或跳列方式可与直接输出到总线的信号自动平均方式或逐个采样方式同时使用。

第三合并采样过程的子采样方式包括色彩空间变换方式、后端数字图像缩放方式、以及这两个方式的串行使用。第一和第二合并过程主要是在模拟信号上进行，而第三子采样过程主要是在数字信号上进行，即模数转换之后进行。通过将处于不同空间位置的三个或四个色彩象素，当作同一个点上的值而转换到另一个色彩空间，就又可实现水平和（或）垂直方向上的数据减少，从而达到子采样的效果。而数字图像缩放方式，是最为直观常用的子采样方式。

在合并采样时可以实现电荷相加。目前的合并采样几乎都是只做到了电压或电流信号的平均，这种方式在合并 N 点时，最多只能将信噪比提高 $\sqrt{N}$ 倍。这是因为现有的合并采样都是 N 个相同色彩的象素共用一根输出线的方式进行合并采样，在这根输出线上，各个象素的电压或电流信号必然要进行（自动的）平均，因此，其信噪比的提高只是在于噪声合并后降

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低了$\sqrt{N}$，从而使信噪比提高最多$\sqrt{N}$倍。而采用本发明的电荷相加方式，例如通过读取电容存储电荷，实现电荷的累加，从而信号可以进行叠加而使得信噪比可以提高至少 N 倍， 比信号平均的方法高至少$\sqrt{N}$倍。也就是说，将 N 个信号以电荷相加的方法合并，理论上最高可以达到N^2个信号相平均的效果或更好(如下面所述)，这是效果非常显著的提高信噪比的手段。

紧邻象素相加，还带来另外一个显著的效果，就是，象素之间的相互干扰(cross-talking)效果被减弱。这是由于本来相互干扰的色彩，现在是合法的一体，也就是说，原来属于噪声的一部分信号，现在成了有效的信号部分，因此，N 个信号电荷相加带来信噪比的改进，可以接近理论上的上限，即 N$\sqrt{N}$倍，从而，相当于N^3个信号相平均的效果。

在全图采样（即对一个图像的按最高分辨率进行采样）时，可以采用逐行扫描、隔行或跨行读取的方式，不需要提高时钟速度和采用帧缓存器，将大阵列图像的全图读取帧率在拍单张照时翻倍。如果增加 AD 转换器和行缓存，那么，全图读取帧率还可以提高更多。这个方法对于省去机械快门有非常重要的价值。

请注意本发明的逐行扫描、隔行或跨行读取的方式，与传统电视系统里的场扫描方式（interleaved scanning）是不同的。传统的场扫描方式，是隔行扫描，隔行读取，因此，奇数场和偶数场（无论是感光还是读取）在时间上差了一场，即半帧。而本发明的逐行扫描、隔行或跨行读取的方式，象素在感光时间顺序上却是与逐行扫描、逐行读取方式是完全一样的，只是行的读取次序做了变化。细节描述请见《一种多光谱感光器件及其采样方法》(中国申请号: 200910105948.2)和《一种感光器件及其读取方法、读取电路》(中国申请号: 200910106477.7) 。

在本发明的一种实施例中，所述的感光器件，所述色彩空间变换包括 RGB 到 CyYeMgX 空间的变换、RGB 到 YUV 空间的变换、或 CyYeMgX 到 YUV 空间的变换，其中 X 为 R(红)、G(绿)、B(兰)中的任一种。图 10 显示了一种利用色彩空间变换来实现子采样的一种方式。

实施方式中包括，上述电荷相加方式通过象素直接并联或将电荷同时转移到读取电容（FD）中完成。

如上所述，多景深感光器件中，第一合并单元或第二合并单元的基于色彩的合并采样方式包括同色合并方式、异色合并方式、混杂合并方式、或选择性抛弃多余色彩合并方式，且第一合并单元和第二合并单元采用的

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合并采样方式不同时为同色合并方式，也即两个合并单元中至少有一个合并单元不采用同色合并方式。

如上所述，第一合并单元或第二合并单元的基于位置的合并采样方式包括以下几种方式中的至少一种：直接输出到总线的信号自动平均方式、跳行或跳列方式、和逐个采样方式。亦即这几种基于位置的合并采样方式可以单独使用，也可以组合使用。

如上所述，在上述感光器件中，可以用色彩空间变换方式和后端数字图像缩放方式中的至少一种来实现所述第三合并采样单元的合并采样方式。

图 9 显示了一种异色象素电荷合并的方式。

实现上述子采样功能的是如图 25 所示的行地址解码控制器和列地址解码控制器。行地址解码控制器将输出两类信号，行选信号 Row[i]（每行一条线）和行控制矢量信号 RS[i]（每行一条或多条线），其中 i 为行的标号。类似地，列地址解码控制器将输出两类信号，列选信号 Col[j]（每列一条线）和列控制矢量信号 T[j]（每列一条或多条线），其中 j 为列的标号。

行选信号 Row[i]是用来做行的选择，而列选信号 Col[j]是用来做列的选择。这是两组相对标准的信号。行控制矢量信号 RS[i]是对现有 CMOS 行控制信号的扩展（每行一条线扩展到每行多条线），而列控制矢量信号 T[j]，有的 CMOS 感光器件根本没有，即使有，也是一列只有一个。

RS[i]和 T[j]用来控制感光象素的复位，清零，感光时间控制，电荷转移，象素合并，和象素读取。由于行列的对称性，RS[i]和 T[j]有很多种具体的实现方式。这些信号的具体实现方式并不受限。

如上所述，多光谱感光器件的全图采样方式包括逐行扫描、逐行读取方式或逐行扫描、隔行或跨行读取方式。

实施方式还包括制作一种感光系统，包括上述的多景深感光器件。

所述感光系统用于获取正面，背面，或双向的图像。

所述感光系统包括数码相机，照相手机，摄像机，视频或照相监控系统，图像识别系统，医学图像系统，军用、消防、和井下图像系统，自动跟踪系统，立体影像系统，机器视觉系统，汽车视觉或辅助驾驶系统，电子游戏系统，网络摄像头，红外和夜视系统，多光谱成像系统，和电脑摄像头。

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实施方式还包括实现一种景深扩展方法，包括步骤：在感光器件中设置至少两个可感应到光源的感光象素层，并将至少两个所述感光象素层按预设距离间隔布置，使得来自距所述感光器件特定距离的镜头的不同光信号，被聚焦到不同的感光象素层。

景深扩展方法中，通过来自不同感光象素层的具有不同清晰度的图像而获取一幅清晰图像。

实施方式中还包括一种成像方法，或者说所述感光器件在成像中的应用，是设置镜头和包括至少两个可感应到光源的感光象素层的感光器件；将所述感光器件放置在距所述镜头特定距离，且至少两个所述感光象素层之间按预设距离间隔布置，使得来自镜头的不同光信号被聚焦到不同的所述感光象素层。

参见图 11-14，实施方式中还包括了一种光学成像系统，包括镜头和多景深感光器件，所述多景深感光器件布置在距所述镜头特定距离，包括至少两个可感应到光源的感光象素层；至少所述感光象素层之间按预设距离间隔布置，来自距所述感光器件特定距离的镜头的不同光信号，被聚焦到不同的感光象素层。

如图 13，可以是不同距离上的所有感兴趣波长的光，分别聚焦在每一感光象素层；或者如图 14，可以是相同距离上的不同波长的光，分别聚焦在每一感光象素层；也可以是不同距离上的不同波长的光，分别聚焦在每一感光象素层。

实施方式包括各个感光象素层聚焦的光，其波长按各个感光象素层距所述光学镜头从近到远逐渐增长。或者在各个感光象素层中，更远距离的光信号，被聚焦在离镜头更近的感光象素层。

例如，当包括两个可感应到光源的感光象素层，两个感光象素层分别位于镜头的第一象距和第二象距，可以通过光学镜头设计，将紫外光、兰色光、绿色光、青色光、或白色光聚焦在离镜头最近的感光象素层；相应的，将兰色光、绿色光、红色光、黄色光、或红外光聚焦在离镜头最远的感光象素层。

又如，当包括三个可感应到光源的感光象素层，三个感光象素层分别位于镜头的第一象距、第二象距、第三象距，可以通过光学镜头设计，将紫外光、兰色光、绿色光、或青色光聚焦在离镜头最近的感光象素层；相应的，将红色光、黄色光、可见光、或红外光聚焦在离镜头最远的感光象素层；相应的，将绿色光、黄色光、可见光、或红色光聚焦在中间的感光象素

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层。

又如，当包括四个可感应到光源的感光象素层，四个感光象素层分别位于镜头的第一象距、第二象距、第三象距、第四象距，可以通过光学镜头设计，将紫外光、兰色光、绿色光、或青色光聚焦在离镜头最近的感光象素层；相应的，将红色光、黄色光、白色光、或红外光聚焦在离镜头最远的感光象素层；相应的，将兰色光、绿色光、或青色光聚焦在离镜头第二近的感光象素层；相应的，将绿色光、红色光、白色光、或黄色光聚焦在离镜头第三近的感光象素层。

又如，当包括两个可感应到光源的感光象素层，两个感光象素层分别位于镜头的第一象距、第二象距，可以通过光学镜头设计，将紫外光或可见光聚焦在离镜头最近的感光象素层；将可见光或红外光聚焦在离镜头最远的感光象素层。

又如，当包括三个可感应到光源的感光象素层，三个感光象素层分别位于镜头的第一象距、第二象距、第三象距，可以通过光学镜头设计，将紫外光或白色光聚焦在离镜头最近的感光象素层；将白色光或红外光聚焦在离镜头最远的感光象素层；将白色光聚焦在中间的感光象素层。

又如，当包括四个可感应到光源的感光象素层，四个感光象素层分别位于镜头的第一象距、第二象距、第三象距、第四象距，可以通过光学镜头设计，将紫外光或白色光聚焦在离镜头最近的感光象素层；将白色光或红外光聚焦在离镜头最远的感光象素层；将白色光聚焦在离镜头第二近的感光象素层；将白色光聚焦在离镜头第三近的感光象素层。

需要注意的是，在上述例子中，对于包括所有感兴趣波长的光，例如白色光，如果说明白色光被聚焦到不同感光象素层，则其一般来源于不同距离，即例如离镜头最近的感光象素层聚焦的是无穷远处的白色光，离镜头最远的感光象素层聚焦的是感兴趣最短距离的白色光。即当两个感光象素层聚焦的光信号的频谱特性相同，则其必须具有不同的距离特性。

本发明的多景深感光器件，兼具多光谱的优异特性，可同时获得众多的彩色信号和其它光谱信号，例如在一种四层感光器件中，可沿光路按距光源从近到远布置一个感应紫外光的第一化学镀膜感光象素层、一个感应兰光，绿光，或青光的第一半导体感光象素层，一个感应红光，黄光，或绿光的第二半导体感光象素层，一个感应红外光的第二化学镀膜感光象素层。其中，第一半导体感光象素层和第二半导体感光象素层分别实现在两个半导体基层上，两个半导体基层之间设置一个具有预设厚度的透光层，

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第一化学镀膜感光象素层布置在第一半导体感光象素层所在基层的顶面上方；第二化学镀膜感光象素层布置在第二半导体感光象素层所在基层的底面下方。由此，不仅实现了景深扩展，且可几乎最大程度的利用入射光能量，在得到彩色的同时，也得到全光谱的信息，充分发挥不同感光材料的特点。这样一种四层多光谱感光器件，制作难度并不太高。如果结合采用前文中本人之前发明的先进采样和以电荷合并和色彩变换为显著特征的子采样电路和方法，更能够大幅地降低感光器件和系统的复杂度，从而为各种应用提供巨大的方便和崇高的性能。

本发明的多景深感光器件，首先实现的第一种特殊用途是景深扩展，现有的 EDoF 主要是使用了光学和数学的手段实现景深扩展，一般需要借助例如镜头等进行自动对焦，相比之下，本发明是直接的通过器件内的不同感光象素层按预设距离间隔设置这样的物理手段实现景深扩展。其次实现的第二种特殊用途是实现全局电子快门，现有的全局电子快门 (Global Shutter) 主要是使用了读取电路的手段，相比之下，本发明利用不感光的转移和读取象素，可以在不用机械快门的情况下，实现高象素的高速拍照。当这两种实现(即景深扩展和全局电子快门)，在同一个感光器件上得以集成的时候，多层多光谱感光器件的巨大威力就得以充分的发挥。因此，本发明在很多指标和性能上，大幅超越现有的方法。

本发明的多景深感光器件，借助于调整不同感光象素层的距离，除了大幅提高灵敏度以外，还能大幅提高系统景深范围，从而让图像更清楚，系统反应速度更快，应用面更宽，乃至消除某些应用中的自动对焦需求。本发明的多景深感光器件在其涵盖的景深范围，能够快速地获取清晰的图像，而不需要经过一个调焦的过程。景深扩展除了能够降低自动对焦的难度和成本外，甚至在某些应用中如手机照相，微距照相，或远距照相，能够彻底消除自动对焦的需求。景深扩展还能让同一张照片里处于不同距离的物体同时清楚，这在一些特殊应用中也是极有用的，而这是自动对焦所不能做到的，因为现有的自动对焦系统，只能让某个距离内的物体清楚成像，而不能让非常宽的一个范围内的物体都清楚。因此，本发明的景深扩展实现，在具有自动对焦能力的系统里，也仍然具备有很大的价值

由于本发明的多景深感光器件的高灵敏度，其感光速度也可大幅提高，从而为在很多应用中取下机械快门提供了可能。由此，在本发明的多景深感光器件中，还提出一种具有跨层读取功能的全局电子快门的实现，以期

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取代某些应用中可能需要的机械快门。全局电子快门作用是在一瞬间，将感光象素里的电荷或电压值拷贝到不感光的读取象素里去，以便读取电路从容的读出。

结合景深扩展全局电子快门的实现，将二者集成在一个感光器件上时，一个不需要自动对焦和机械快门的高性能、高速度、高象素感光系统，就可以芯片的方式来实现，大大地降低系统的尺寸、复杂度、功耗和成本，为很多新的应用提供了可能。

这种带有全局电子快门的或多景深的感光器件，可为感光系统省去机械快门或者省去自动对焦系统（或者降低对自动对焦系统的要求），并在不加快感光器件时钟的情况下，实现高速的电子快门或清晰成像。

在极大地简化了感光系统的机械复杂度的要求的同时，本发明采用两层或多层的布局，结合先进的两层或多层互补或正交色彩图案排列的方法，能够最大化的利用入射光子的能量，不用或只用少许的彩色滤光膜，从而达到或接近到达光电转换效率的理论上限，并在完整地重建彩色的同时，获得其它光谱的图像，包括紫外线图像，近红外图像，和远红外图像。

当感光象素层与读取电路分层后，读取电路层的读取电路和处理计算可以做得非常精细和复杂，为单芯片感光系统的制作，提供了巨大的便利。

这种多景深感光器件可同时获得众多的彩色信号和其它光谱信号，采用本人之前发明的先进的采样和以电荷合并和色彩变换为显著特征的子采样电路和方法，能够大幅地降低感光器件和系统的复杂度，从而为各种应用提供巨大的方便和崇高的性能。

这种多景深感光器件，可用于正面感光，背面感光，或双向感光。通过精细布置各层感光器件的象素感应光谱段和各层色彩图案的合理布局，可以产生各种优选的多光谱感光器件，如高灵敏度彩色感光器件，高灵敏度彩色和红外感光器件，无杂色（杂色由插值引起的）的高灵敏度彩色或多光谱感光器件等等。

采用主动象素和被动象素读取相结合的手段，可以获得超低功耗感光器件，超高动态范围感光器件。

以上内容是结合具体的实施方式对本发明所作的进一步详细说明，不能认定本发明的具体实施只局限于这些说明。对于本发明所属技术领域的普通技术人员来说，在不脱离本发明构思的前提下，还可以做出若干简单推演或替换，都应当视为属于本发明的保护范围。

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权 利 要 求 书

1. 一种多景深感光器件，其特征在于，包括至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自距所述感光器件特定距离的镜头的不同光信号被聚焦到不同的所述感光象素层。

2. 如权利要求 1 所述的感光器件，其特征在于，所述感光象素层包括化学镀膜感光象素层和半导体感光象素层中的至少一者。

3. 如权利要求 2 所述的感光器件，其特征在于，所述化学镀膜感光象素层包括量子点感光象素。

4. 如权利要求 2 所述的感光器件，其特征在于，所述半导体感光象素层包括 CMOS 光敏二极管、CMOS 感光门、CCD 光敏二极管、CCD 感光门、和具有双向电荷转移功能的 CMOS 和 CCD 感光二极管和感光门。

5. 如权利要求 1-4 任一所述的感光器件，其特征在于，所述不同光信号，包括不同距离的光信号，或者不同波长的光信号。

6. 如权利要求 5 所述的感光器件，其特征在于，波长更短的光信号被聚焦到离镜头更近的感光象素层。

7. 如权利要求 6 所述的感光器件，其特征在于，所述感光象素层为两层，紫色光、兰色光、绿色光、或青色光被聚焦到离镜头较近的感光象素层，绿色光、红色光、黄色光、可见光、或红外光被聚焦到离镜头较远的感光象素层。

8. 如权利要求 6 所述的感光器件，其特征在于，所述感光象素层为三层，紫外光、兰色光、或青色光被聚焦到离镜头最近的感光象素层；兰色光、绿色光、红色光、或黄色光被聚焦到位于中间的感光象素层；红色光、黄色光、可见光、或红外光被聚焦到离镜头最远的感光象素层。

9. 如权利要求 5 所述的感光器件，其特征在于，更远距离的光信号被聚焦到离镜头更近的感光象素层。

10. 如权利要求 9 所述的感光器件，其特征在于，所述感光象素层为两层，无穷远处的光信号被聚焦到离镜头较近的感光象素层，感兴趣最短距离的光信号被聚焦到离镜头较远的感光象素层。

11. 如权利要求 10 所述的感光器件，其特征在于，无穷远处的紫色光、

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兰色光、绿色光、或青色光被聚焦到离镜头较近的感光象素层，感兴趣最短距离的绿色光、红色光、黄色光、可见光、或红外光被聚焦到离镜头较远的感光象素层。

12. 如权利要求 9 所述的感光器件，其特征在于，所述感光象素层为三层，无穷远处的光信号被聚焦到离镜头最近的感光象素层，感兴趣最短距离的光信号被聚焦到离镜头最远的感光象素层，无穷远处与感兴趣最短距离之间的一个中间距离的光信号被聚焦到位于中间的感光象素层。

13. 如权利要求 12 所述的感光器件，其特征在于，所述感光象素层为三层，无穷远处的紫外光、兰色光、或青色光被聚焦到离镜头最近的感光象素层，感兴趣最短距离的红色光、黄色光、可见光、或红外光被聚焦到离镜头最远的感光象素层，无穷远处与感兴趣最短距离之间的一个中间距离的兰色光、绿色光、红色光、或黄色光被聚焦到位于中间的感光象素层。

14. 如权利要求 10-13 任一所述的感光器件，其特征在于，所述感兴趣最短距离包括 2mm, 5mm, 7mm, 1cm, 2cm, 3cm, 5cm, 7cm, 10cm, 20cm, 30cm, 40cm, 50cm, 60cm, 70cm, 80cm, 100cm, 或 150cm。

15. 如权利要求 1-14 任一所述的感光器件，其特征在于，至少两个所述感光象素层之间设置有透光层。

16. 如权利要求 1-15 任一所述的感光器件，其特征在于，所述感光象素层中的感光象素为正面感光象素、背面感光象素、或双向感光象素。

17. 如权利要求 16 所述的感光器件，其特征在于，当感光象素为双向感光象素时，其感光选向方式为隔离选向、分时选向、分区选向、或象素选向。

18. 如权利要求 1-17 任一所述的感光器件，其特征在于，所述感光象素层中的感光象素分别感应包含紫外线、可见光、近红外、和远红外中的一个互补谱段或子谱段；或者所述化学镀膜感光象素和半导体感光象素分别感应包含紫外线、可见光、近红外、和远红外中的一个正交谱段或子谱段。

19. 如权利要求 18 所述的感光器件，其特征在于，所述互补谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近红外光谱+远红外光谱，

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黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱；

所述正交谱段或子谱段包含紫外光谱，兰色光谱，绿色光谱，红色光谱，近红外光谱，远红外光谱，青色光谱，黄色光谱，白色光谱，近红外光谱+远红外光谱，红色光谱+近红外光谱，红光谱+近红外光谱+远红外光谱，黄色光谱+近红外光谱，黄色光谱+近红外光谱+远红外光谱，可见光谱+近红外光谱+远红外光谱，紫外光谱+可见光谱，紫外光谱+可见光谱+近红外光谱，紫外光谱+可见光谱+近红外光谱+远红外光谱。

20. 如权利要求 1-19 任一所述的感光器件，其特征在于，每一感光象素层中的色彩排列包括同一排列、水平排列、垂直排列、对角排列、广义贝叶排列、YUV422 排列、横向 YUV422 排列、蜂窝排列、均布排列。

21. 如权利要求 1-20 任一所述的感光器件，其特征在于，至少一个所述感光象素层中的部分或全部感光象素的正面、背面或双面设置有滤光膜，所述滤光膜的选频特性包括红外截止滤波、兰色带通、绿色带通、红色带通、青色带通、黄色带通、品红色带通、或可见光带通。

22. 如权利要求 1-21 任一所述的感光器件，其特征在于，所述感光象素层中的相邻两层各自设有读取电路；或者所述感光象素层的相邻两层共用读取电路。

23. 如权利要求 22 所述的感光器件，其特征在于，所述读取电路为主动象素读取电路、被动象素读取电路、或主动象素与被动象素混合读取电路。

24. 如权利要求 23 所述的感光器件，其特征在于，所述主动象素包括 3T、4T、5T 或 6T 主动象素。

25. 如权利要求 22 所述的感光器件，其特征在于，所述读取电路的共用方式包括单层或上下层 4 点共享方式、单层或上下层 6 点共享方式、单层或上下层 8 点共享方式、或单层或上下层任意点共享方式。

26. 如权利要求 22-25 所述的感光器件，其特征在于，所述读取电路包括用于对每一感光象素层的象素阵列中的紧邻的同行异列、异行同

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列、或异行异列的象素间进行两两合并采样，获得第一合并象素的采样数据的第一合并单元；以及用于对第一合并单元得到的第一合并象素的采样数据进行合并采样以获得第二合并象素的采样数据的第二合并单元。

27. 如权利要求 26 所述的感光器件，其特征在于，所述读取电路还包括第三合并单元，用于对第二合并单元得到的第二合并象素的采样数据进行合并采样以获得第三合并象素的采样数据。

28. 如权利要求 26 或 27 所述的感光器件，其特征在于，所述第一合并单元或第二合并单元的象素合并方式为相同或不同色彩象素间的电荷相加方式或信号平均方式，其中不同色彩象素间的象素合并方式遵照色彩空间变换的方式，以满足色彩重建的要求。

29. 如权利要求 28 所述的感光器件，其特征在于，所述色彩空间变换包括 RGB 到 CyYeMgX 空间的变换、RGB 到 YUV 空间的变换、或 CyYeMgX 到 YUV 空间的变换，其中 X 为 R(红)、G(绿)、B(兰)中的任一种。

30. 如权利要求 29 所述的感光器件，其特征在于，所述电荷相加方式通过象素直接并联或将电荷同时转移到读取电容（FD）中完成。

31. 如权利要求 26-30 所述的感光器件，其特征在于，所述第一合并单元或第二合并单元的基于色彩的合并采样方式包括同色合并方式、异色合并方式、混杂合并方式、或选择性抛弃多余色彩合并方式，且第一合并单元和第二合并单元采用的合并采样方式不同时为同色合并方式。

32. 如权利要求 26-31 所述的感光器件，其特征在于，所述第一合并单元或第二合并单元的基于位置的合并采样方式包括以下几种方式中的至少一种：直接输出到总线的信号自动平均方式、跳行或跳列方式、和逐个采样方式。

33. 如权利要求 27-32 所述的感光器件，其特征在于，所述第三合并单元的合并采样方式包括：色彩空间变换方式和后端数字图像缩放方式中的至少一种。

34. 如权利要求 1-33 所述的感光器件，其特征在于，包括具有跨层读取功能的全局电子快门，所述全局电子快门包含多个可同时转移并读取一层或多层感光象素层的电荷或电压值的不感光的转移和读取象素。

35. 如权利要求 34 所述的感光器件，其特征在于，所述多个不感光的转

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移和读取象素位于不感光象素转移和读取层；或者位于所述感光象素层。

36. 如权利要求 35 所述的感光器件，其特征在于，每一感光象素层，设置有一个紧邻的不感光象素转移和读取层。

37. 如权利要求 34-36 任一所述的感光器件，所述不感光转移和读取象素由半导体电路制成。

38. 一种景深扩展方法，其特征在于，包括:
在感光器件中设置至少两个可感应到光源的感光象素层，并将至少两个所述感光象素层按预设距离间隔布置，使得来自距所述感光器件特定距离的镜头的不同光信号被聚焦到不同的所述感光象素层。

39. 如权利要求 38 所述的景深扩展方法，其特征在于，通过来自不同感光象素层的具有不同清晰度的图像而获取一幅清晰图像。

40. 一种光学成像方法，其特征在于，包括:
设置镜头和包括至少两个可感应到光源的感光象素层的感光器件;
将所述感光器件放置在距所述镜头特定距离，且至少两个所述感光象素层之间按预设距离间隔布置，使得来自镜头的不同光信号被聚焦到不同的所述感光象素层。

41. 一种光学成像系统，其特征在于，包括镜头和多景深感光器件，所述多景深感光器件布置在距所述镜头特定距离，包括至少两个可感应到光源的感光象素层，至少两个所述感光象素层之间按预设距离间隔布置，使得来自所述镜头的不同光信号被聚焦到不同的所述感光象素层。

42. 如权利要求 41 所述的光学成像系统，其特征在于，所述不同光信号，包括不同距离的光信号，或者不同波长的光信号。

43. 如权利要求 42 所述的光学成像系统，其特征在于，波长更短的光信号被聚焦到离镜头更近的感光象素层。

44. 如权利要求 42 所述的光学成像系统，其特征在于，更远距离的光信号被聚焦到离镜头更近的感光象素层。

45. 一种感光系统，其特征在于，包括如权利要求 1-35 任一所述的感光器件。

46. 如权利要求 45 所述的感光系统，其特征在于，所述感光系统包括数码相机，照相手机，摄像机，视频或照相监控系统，图像识别系统，医学图像系统，军用、消防或井下图像系统，自动跟踪系统，立体

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影像系统，机器视觉系统，汽车视觉或辅助驾驶系统，电子游戏系统，网络摄像头，红外和夜视系统，多光谱成像系统，和电脑摄像头中的一种。

SAMSUNG EX. 1002 - 2162/2862

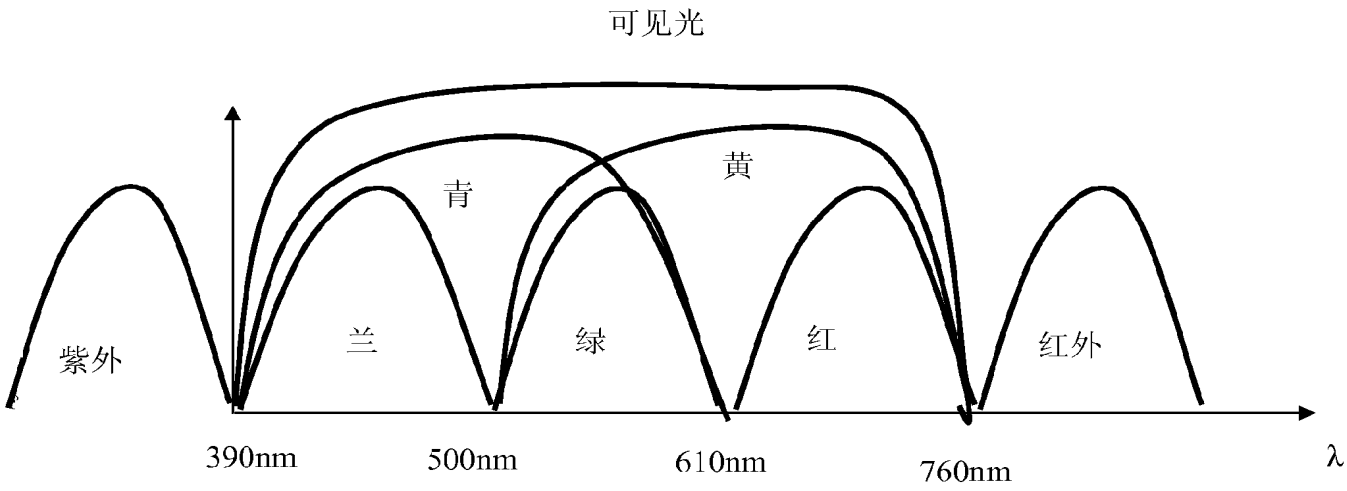
可见光
紫外
兰
青
绿
黄
红
红外
390nm
500nm
610nm
760nm
λ

图 1

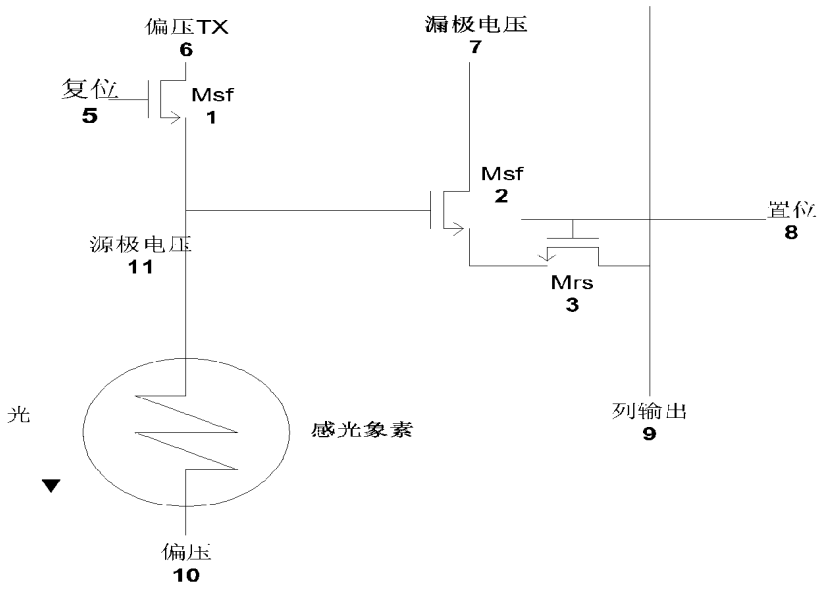
偏压TX
6
复位
5
Msf
1
漏极电压
7
Msf
2
置位
8
源极电压
11
Mrs
3
光
感光象素
列输出
9
偏压
10

图 2

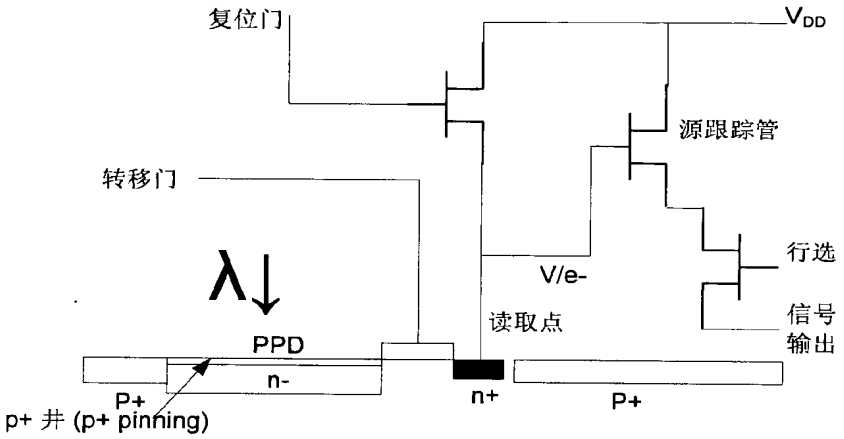

图 3

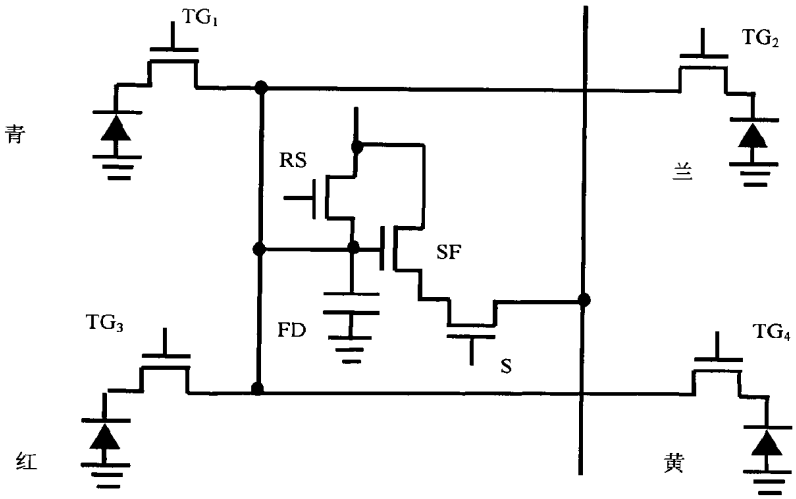

图 4

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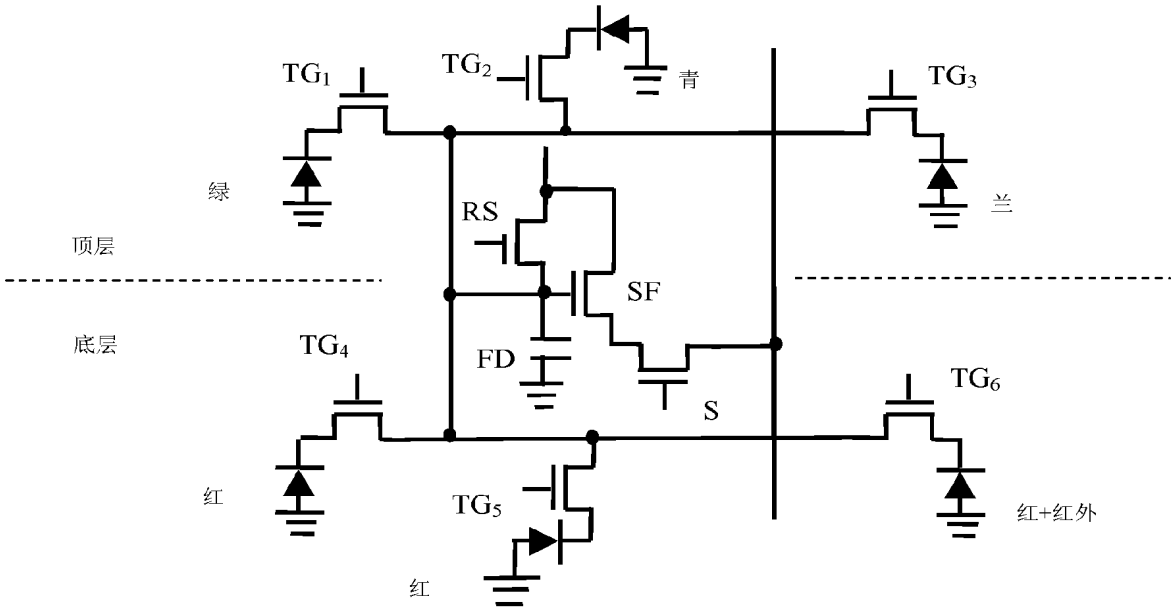

图 5

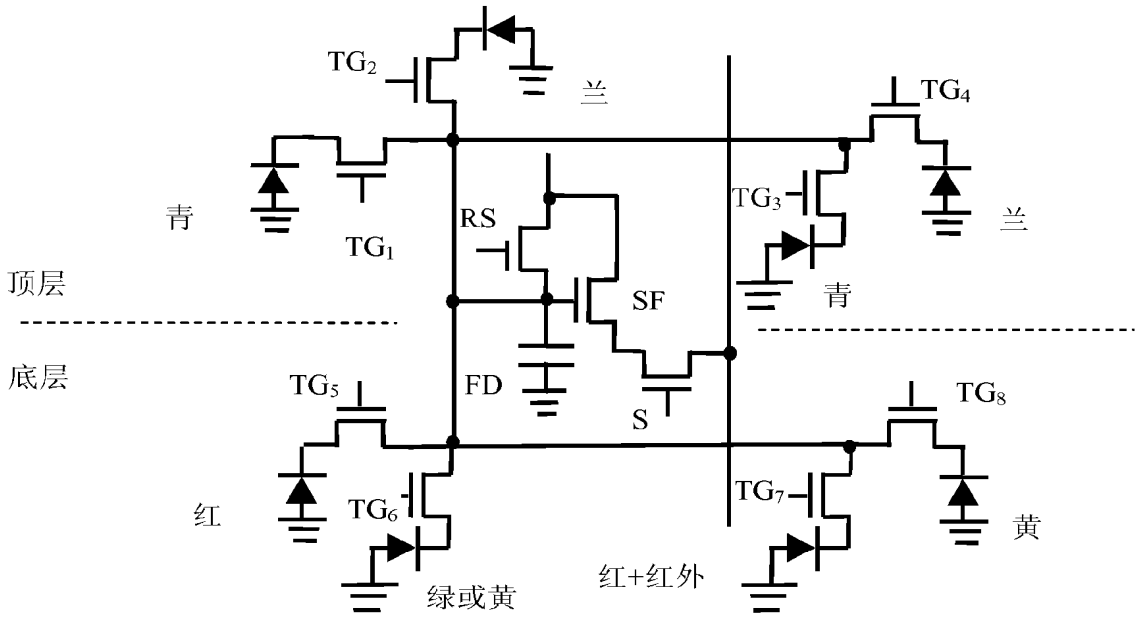

图 6

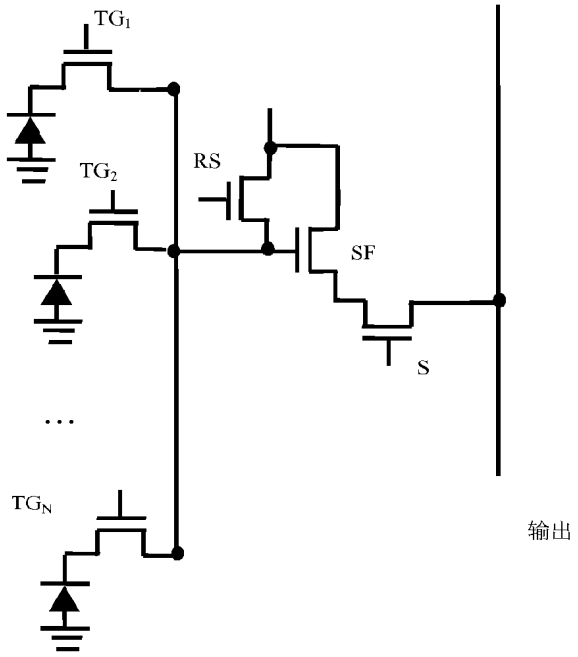
TG1
TG2
RS
SF
S
...
TGN
输出

图 7

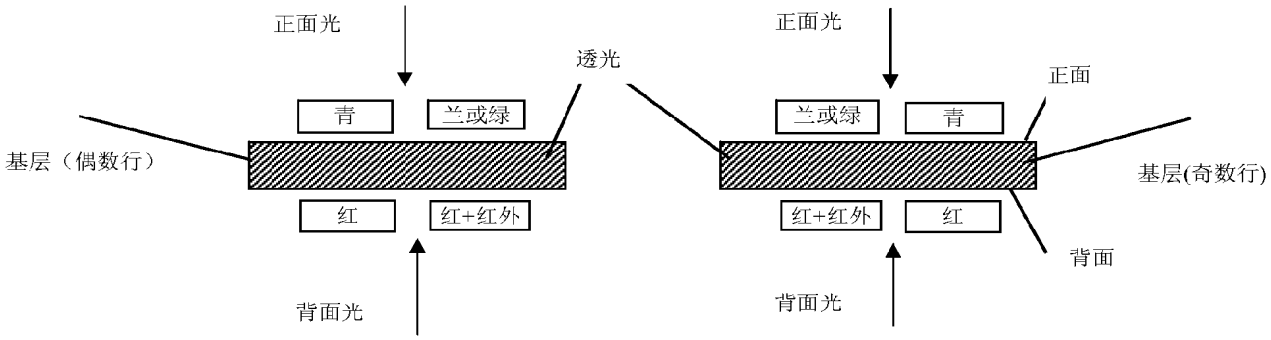
正面光
透光
青
兰或绿
基层（偶数行）
红
红+红外
背面光
正面光
正面
兰或绿
青
基层(奇数行)
红+红外
红
背面
背面光

图 8

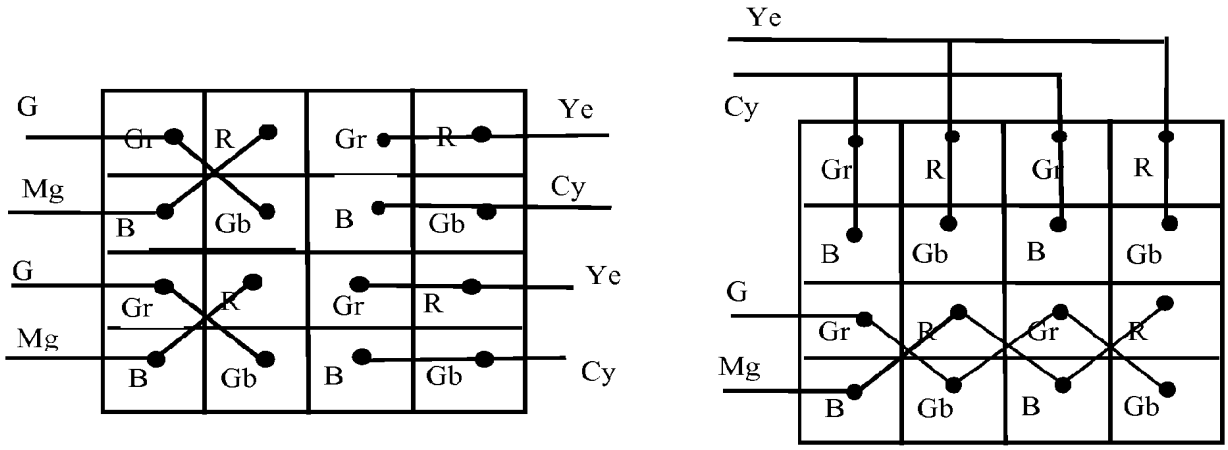

图 9

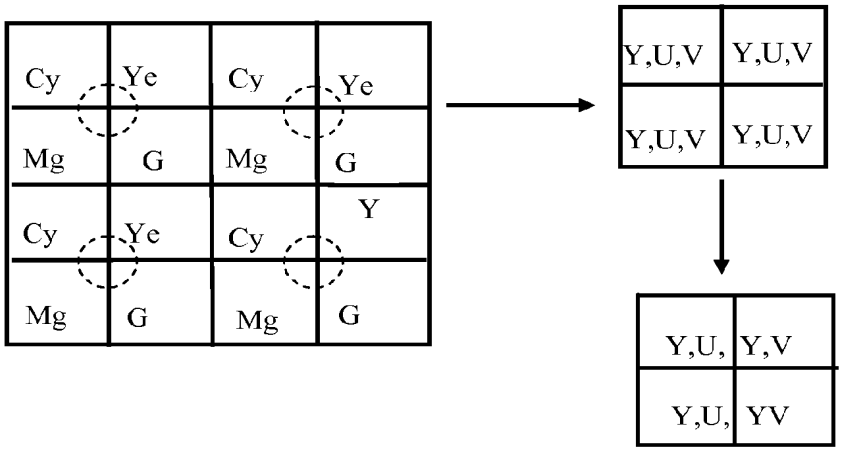

图 10

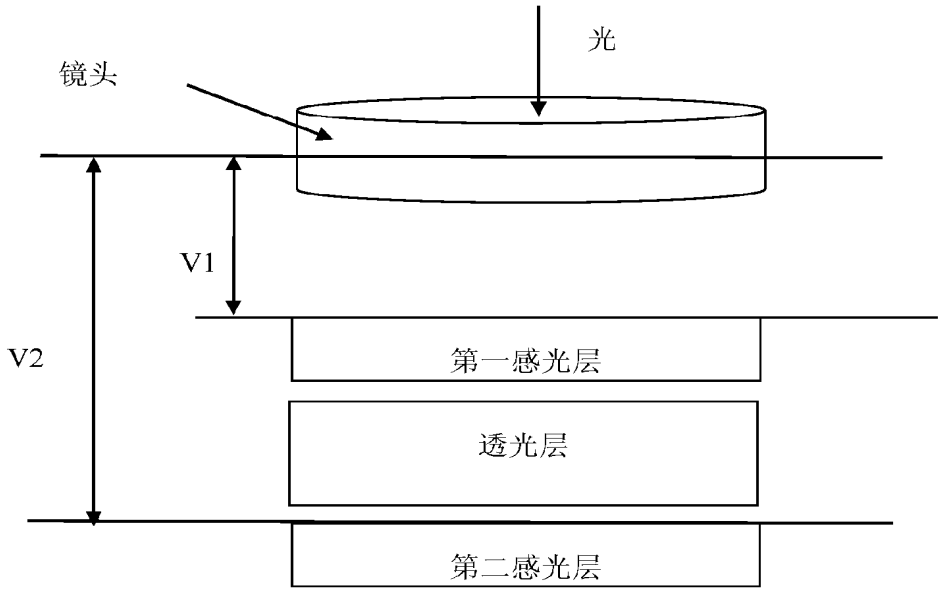

图 11

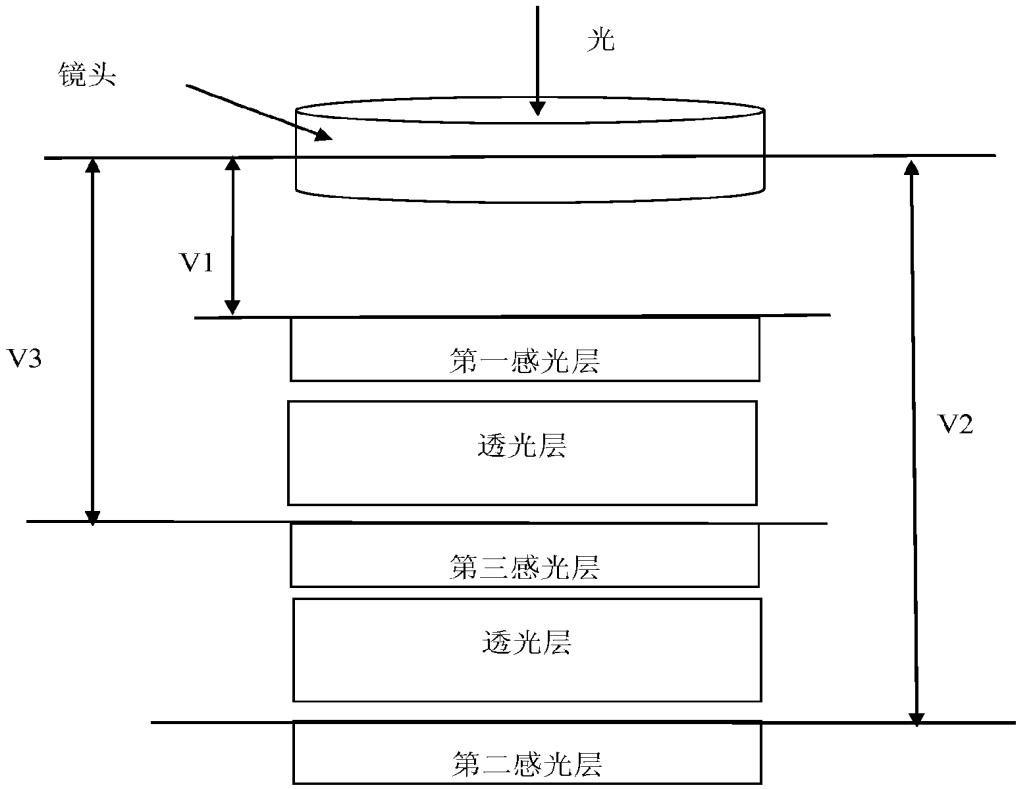

图 12

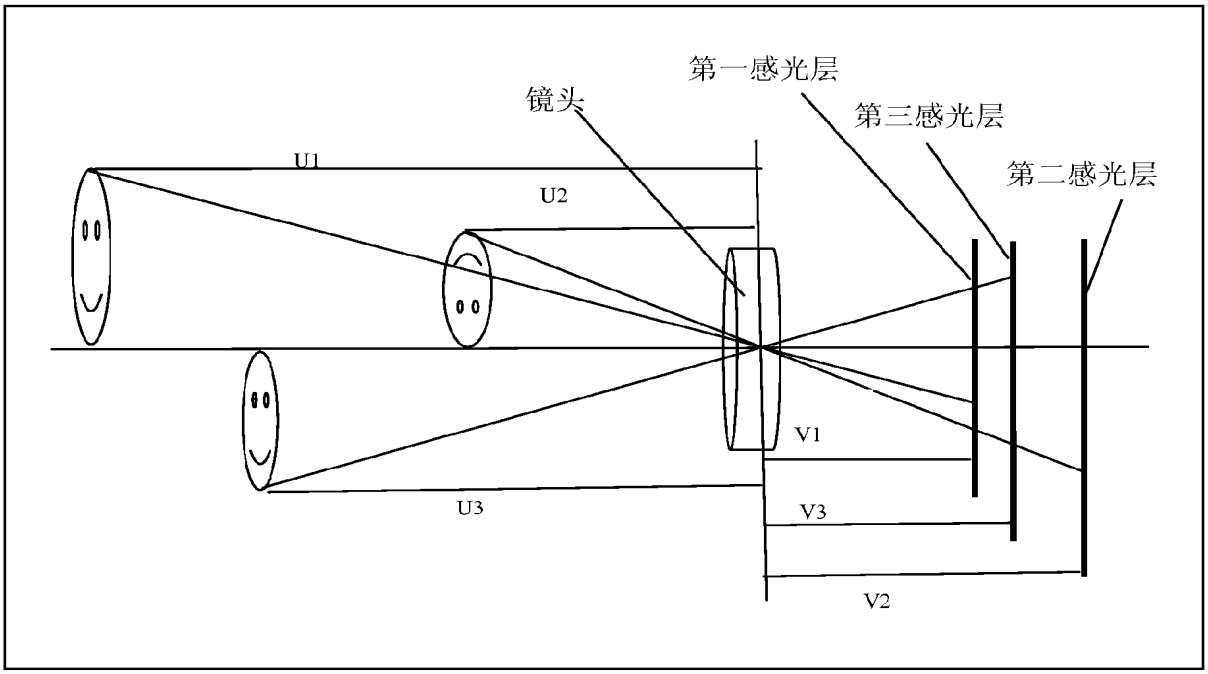

图 13

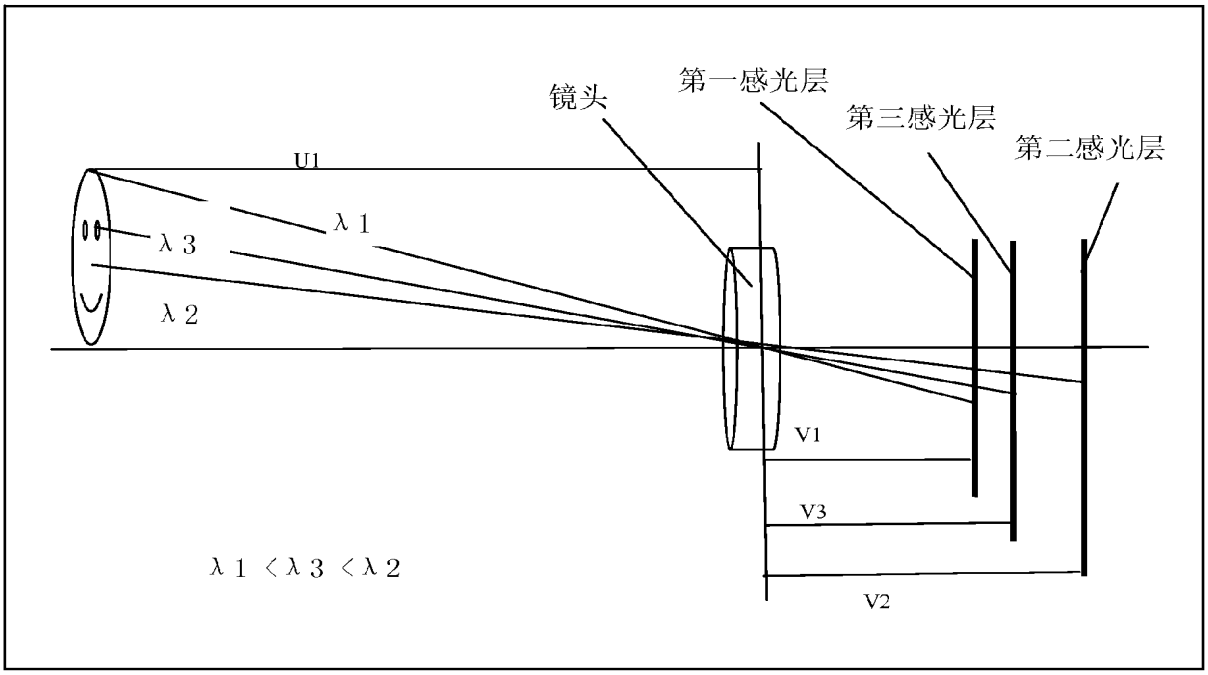

图 14

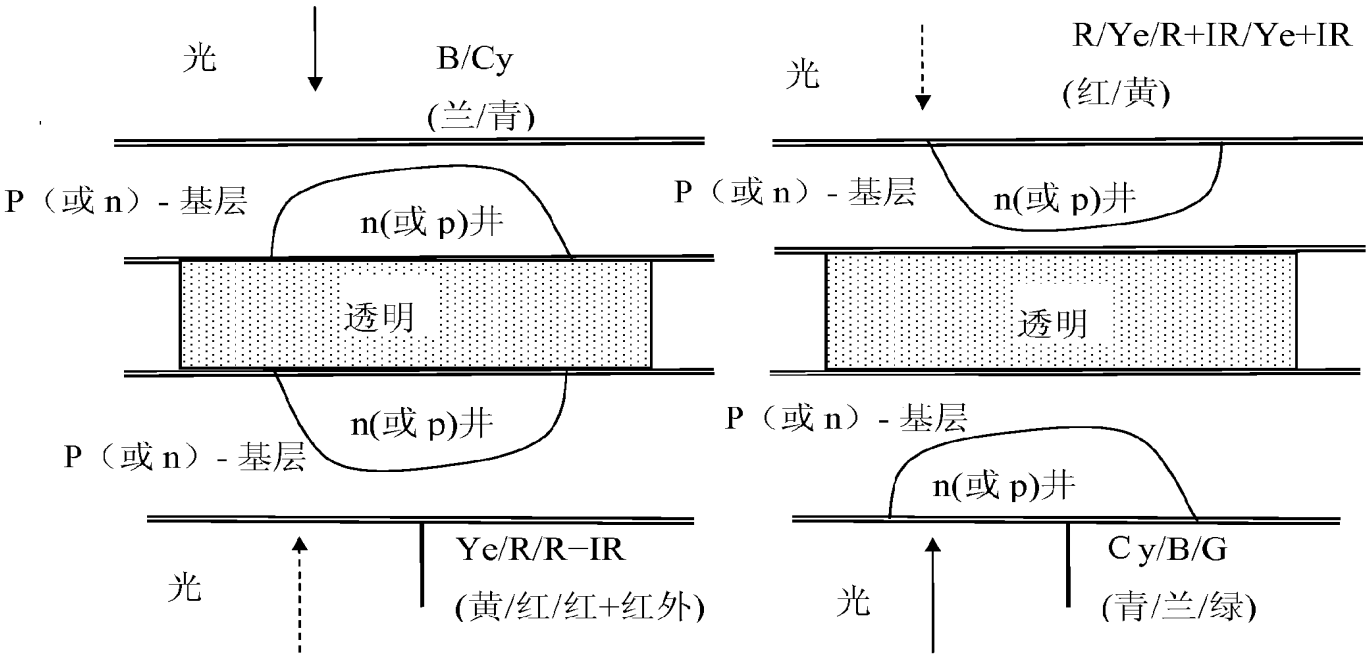
光
B/Cy
(兰/青)
P（或 n）- 基层
n(或 p)井
透明
n(或 p)井
P（或 n）- 基层
光
Ye/R/R−IR
(黄/红/红+红外)
光
R/Ye/R+IR/Ye+IR
(红/黄)
P（或 n）- 基层
n(或 p)井
透明
P（或 n）- 基层
n(或 p)井
光
C y/B/G
(青/兰/绿)

图 15

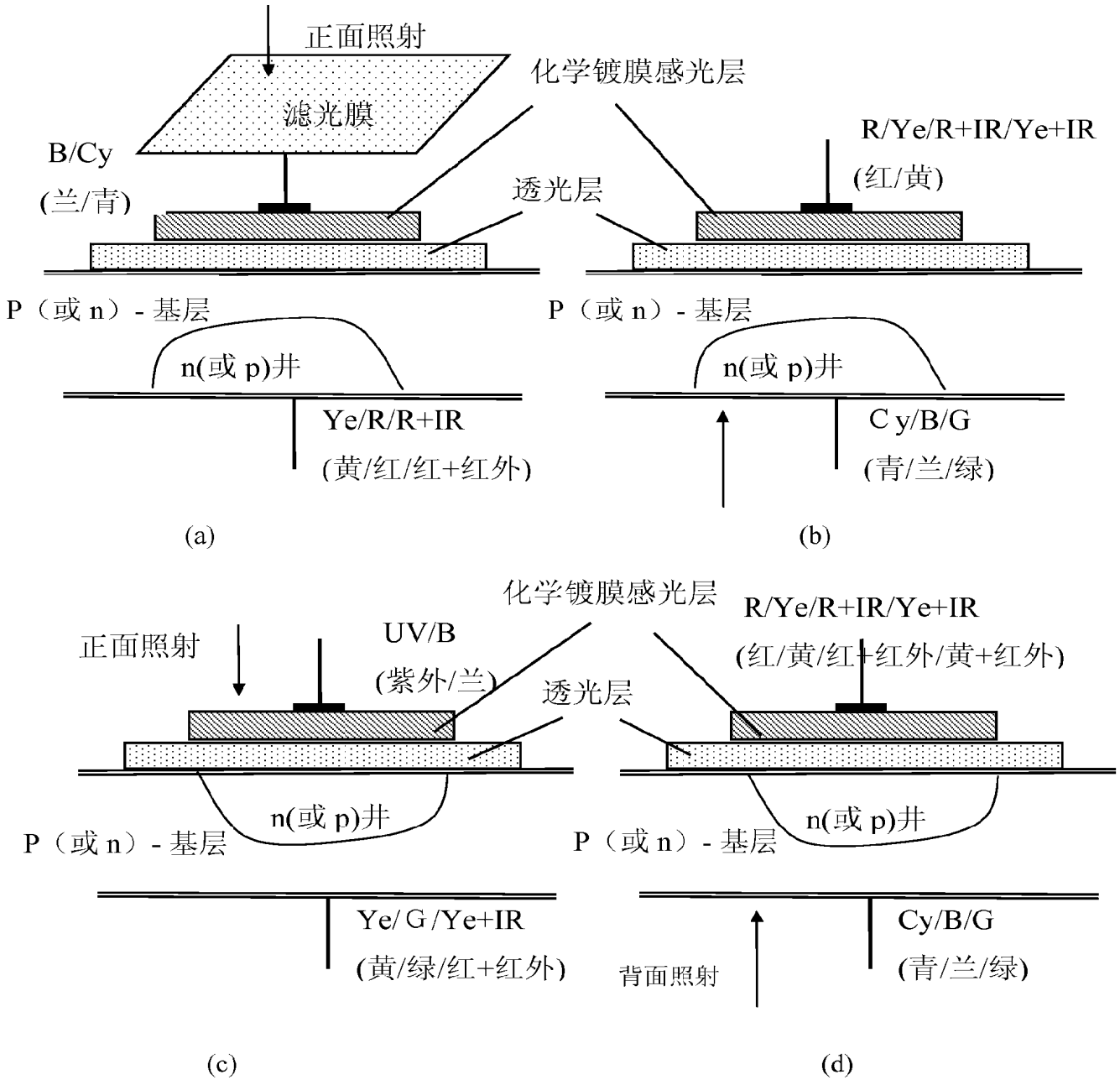
正面照射
化学镀膜感光层
滤光膜
B/Cy
(兰/青)
透光层
R/Ye/R+IR/Ye+IR
(红/黄)
P（或 n）- 基层
n(或 p)井
Ye/R/R+IR
(黄/红/红+红外)
(a)
P（或 n）- 基层
n(或 p)井
C y/B/G
(青/兰/绿)
(b)
化学镀膜感光层
R/Ye/R+IR/Ye+IR
(红/黄/红+红外/黄+红外)
正面照射
UV/B
(紫外/兰)
透光层
n(或 p)井
P（或 n）- 基层
Ye/ G /Ye+IR
(黄/绿/红+红外)
(c)
n(或 p)井
P（或 n）- 基层
Cy/B/G
(青/兰/绿)
背面照射
(d)

图 16

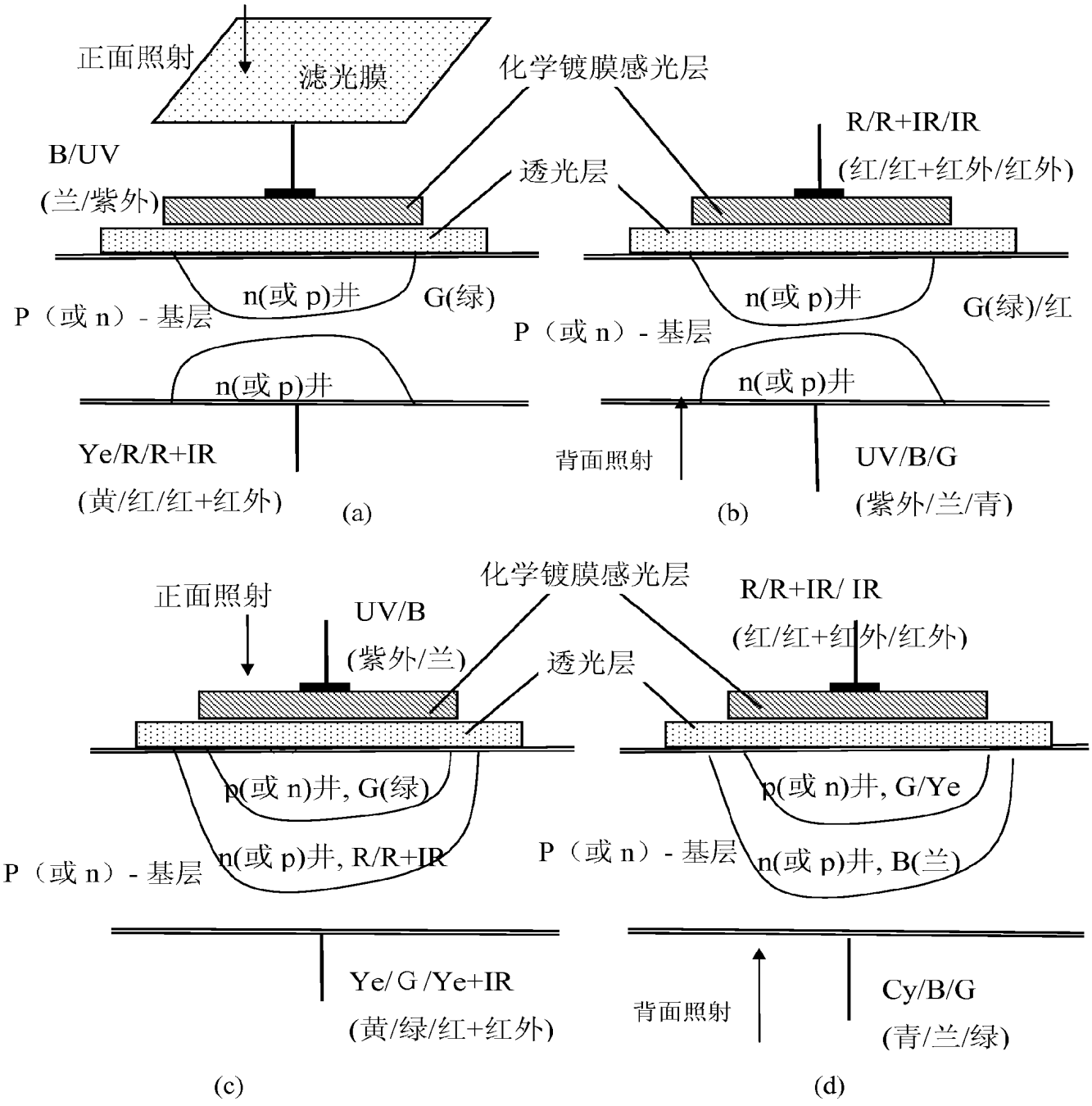
正面照射
滤光膜
化学镀膜感光层
B/UV
(兰/紫外)
透光层
n(或 p)井
G(绿)
P（或 n）- 基层
n(或 p)井
Ye/R/R+IR
(黄/红/红+红外)
(a)
R/R+IR/IR
(红/红+红外/红外)
n(或 p)井
G(绿)/红
P（或 n）- 基层
n(或 p)井
背面照射
UV/B/G
(紫外/兰/青)
(b)
正面照射
UV/B
(紫外/兰)
化学镀膜感光层
透光层
R/R+IR/ IR
(红/红+红外/红外)
p(或 n)井, G(绿)
n(或 p)井, R/R+IR
P（或 n）- 基层
Ye/ G /Ye+IR
(黄/绿/红+红外)
(c)
p(或 n)井, G/Ye
P（或 n）- 基层
n(或 p)井, B(兰)
背面照射
Cy/B/G
(青/兰/绿)
(d)

图 17

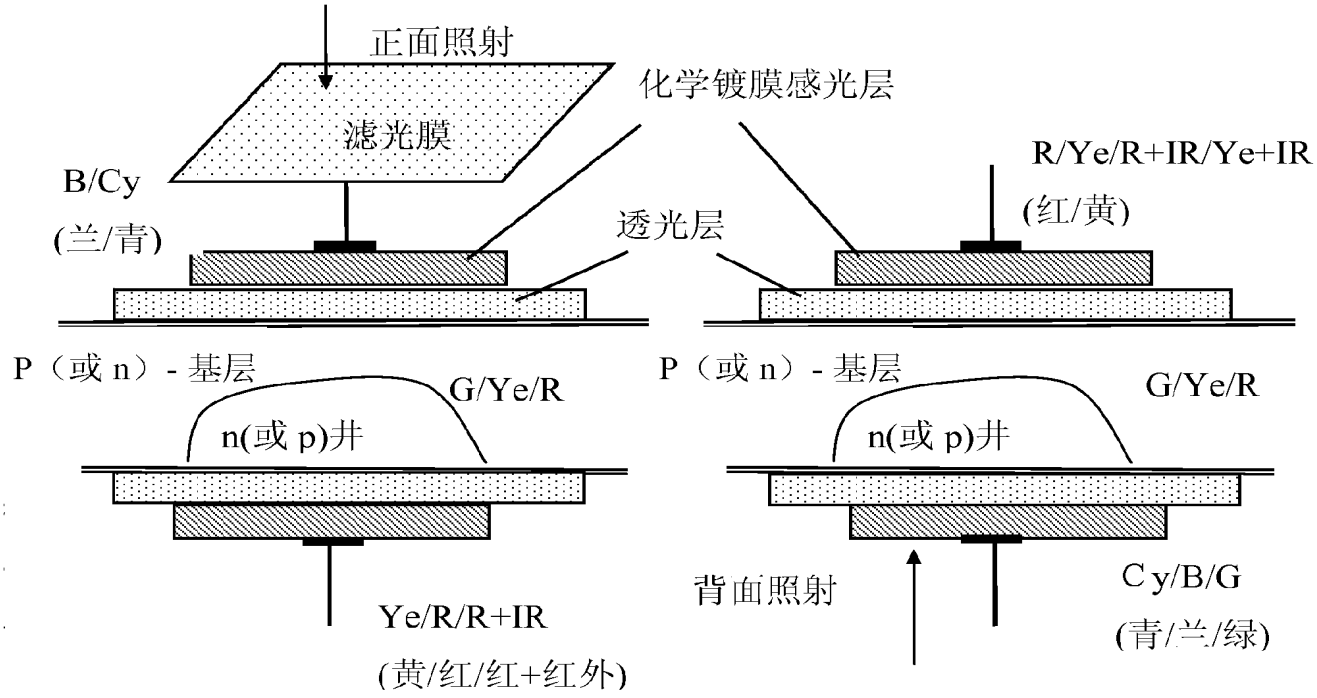
正面照射
滤光膜
化学镀膜感光层
B/Cy
(兰/青)
透光层
R/Ye/R+IR/Ye+IR
(红/黄)
P（或 n）- 基层
G/Ye/R
n(或 p)井
Ye/R/R+IR
(黄/红/红+红外)
P（或 n）- 基层
G/Ye/R
n(或 p)井
背面照射
Cy/B/G
(青/兰/绿)
(a)
(b)

图 18

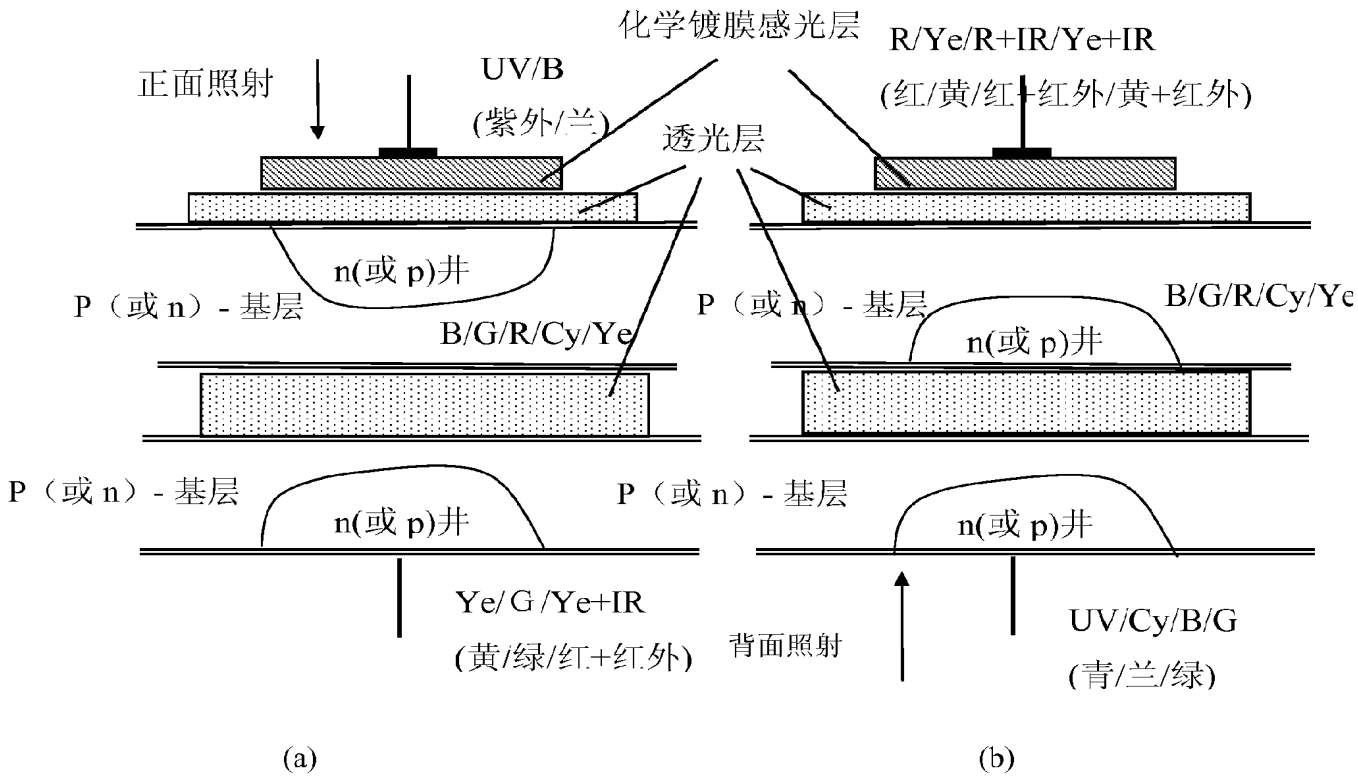
化学镀膜感光层
正面照射
UV/B
(紫外/兰)
透光层
R/Ye/R+IR/Ye+IR
(红/黄/红+红外/黄+红外)
n(或 p)井
P（或 n）- 基层
B/G/R/Cy/Ye
P（或 n）- 基层
n(或 p)井
B/G/R/Cy/Ye
P（或 n）- 基层
n(或 p)井
Ye/G/Ye+IR
(黄/绿/红+红外)
P（或 n）- 基层
n(或 p)井
背面照射
UV/Cy/B/G
(青/兰/绿)
(a)
(b)

图 19

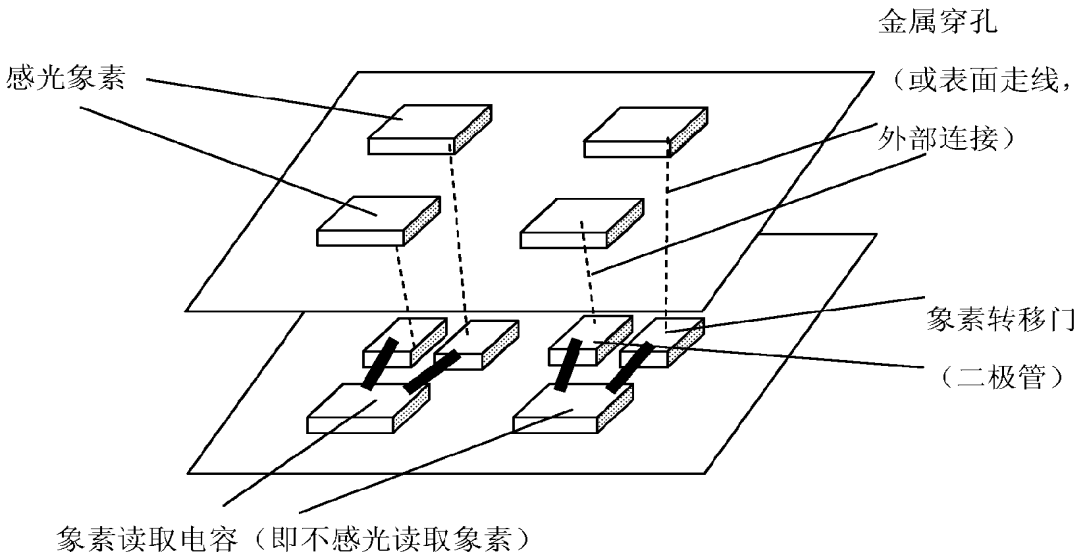

图 20

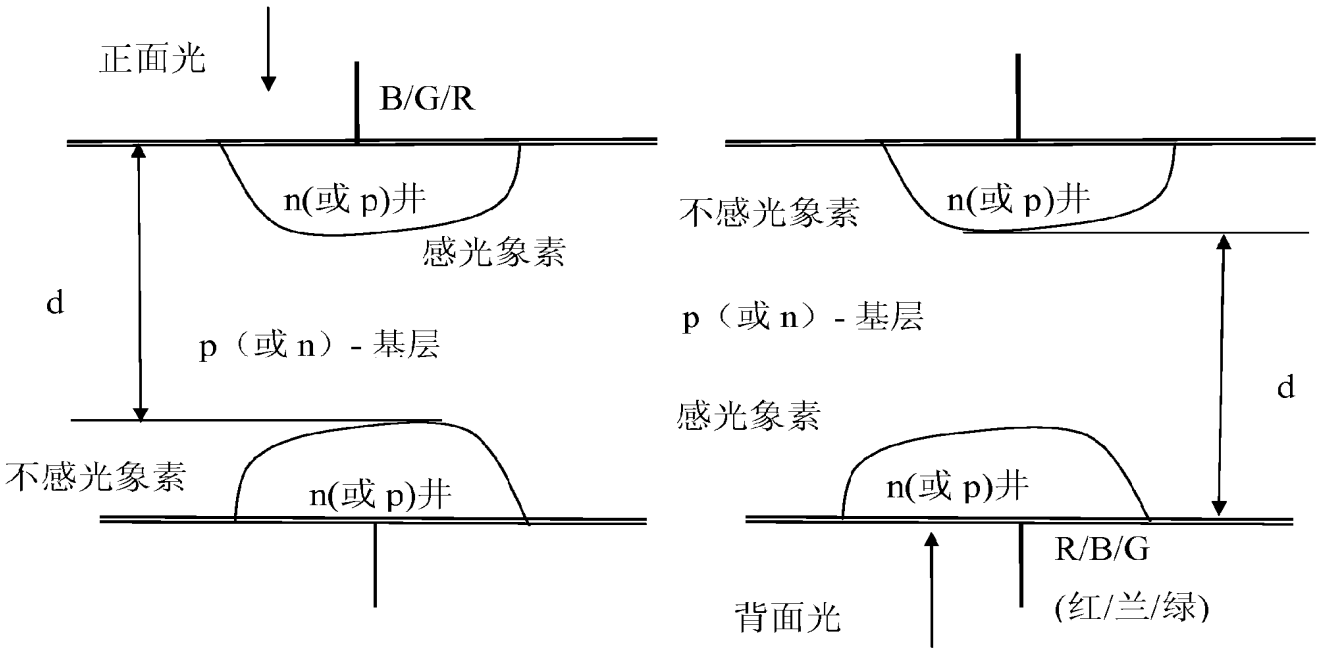
正面光
B/G/R
n(或 p)井
感光象素
d
p（或 n）- 基层
不感光象素
n(或 p)井
不感光象素
n(或 p)井
p（或 n）- 基层
感光象素
d
n(或 p)井
R/B/G
(红/兰/绿)
背面光

图 21

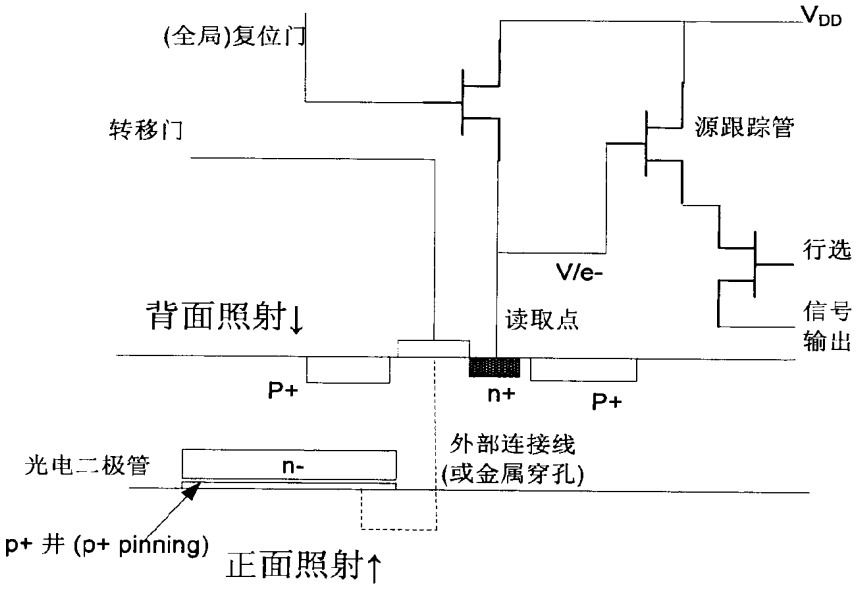

图 22

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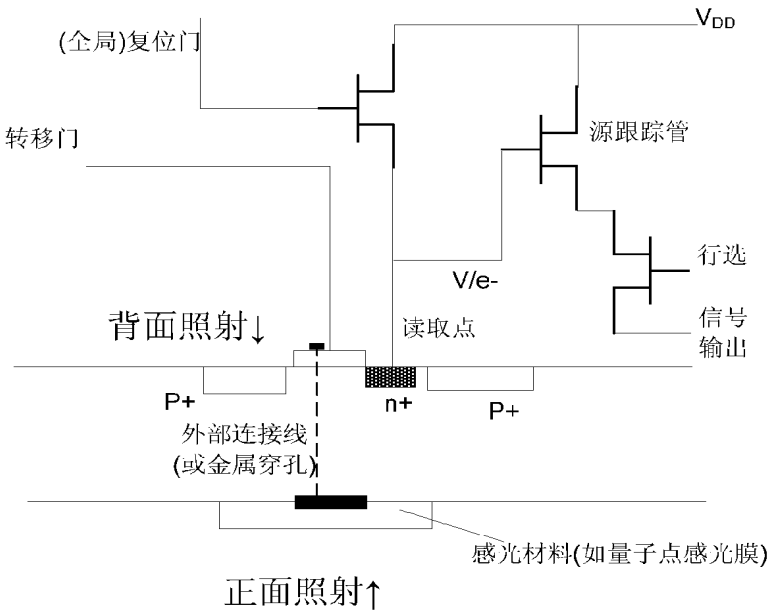
(全局)复位门
V_{DD}
转移门
源跟踪管
行选
V/e-
背面照射↓
读取点
信号
输出
P+
n+
P+
外部连接线
(或金属穿孔)
感光材料(如量子点感光膜)
正面照射↑

图 23

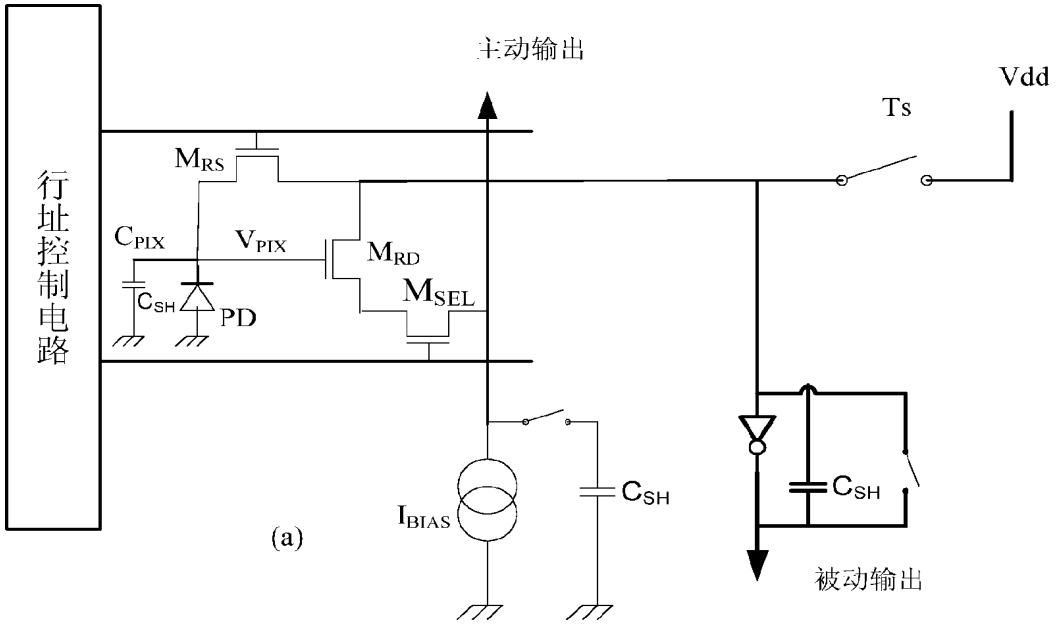
行址控制电路
主动输出
Vdd
Ts
M_{RS}
C_{PIX}
V_{PIX}
M_{RD}
M_{SEL}
C_{SH}
PD
I_{BIAS}
C_{SH}
C_{SH}
被动输出
(a)

图 24

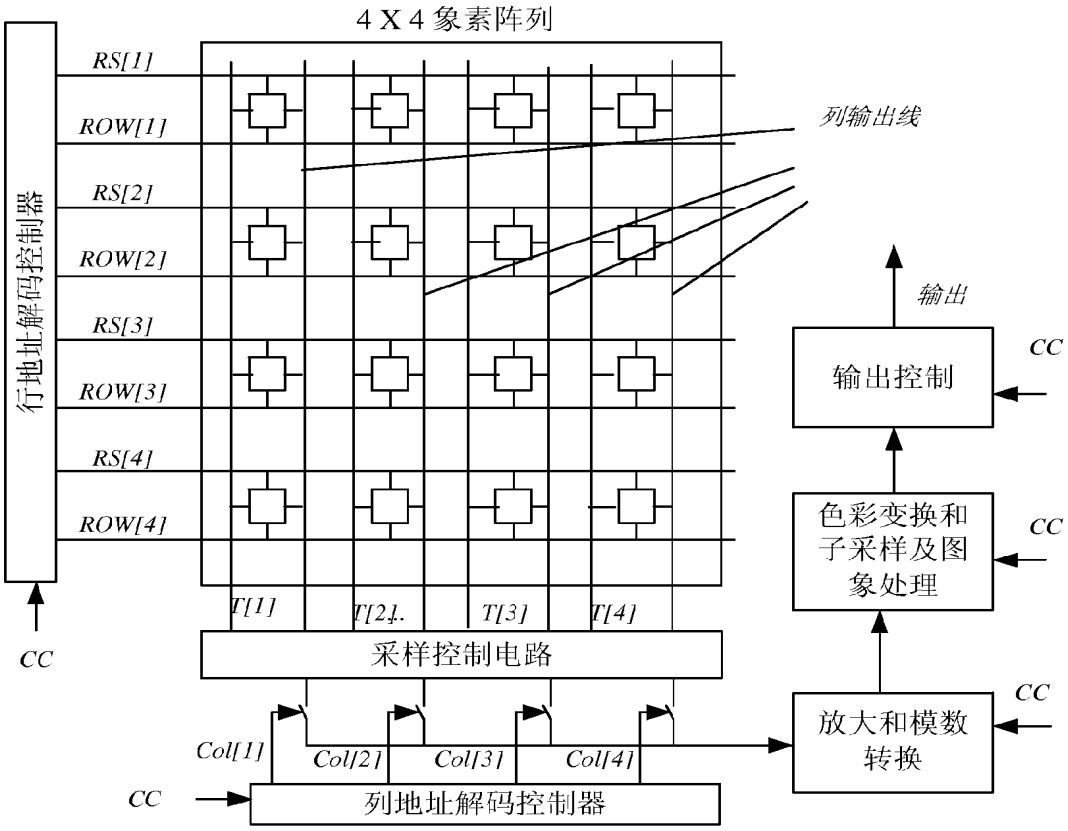

图 25

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/076338

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS,CNKI,WPI,EPODOC: photo sensitive pixel lens signal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN101345248B (BOLI MALJIE COMMUNICATION SHENZHEN CO LTD et al) 14 Jul.2010 (14.07.2010) embodiment of the description figs. 5-16	1,4-14,18-21,38-46
Y		2-3,15-17,22-37
Y	CN101740587A (BOLI MALJIE COMMUNICATION SHENZHEN CO LTD) 16 Jun.2010 (16.06.2010) figs. 9-14	15-17
Y	CN101807590A (BOLI MALJIE COMMUNICATION SHENZHEN CO LTD) 18 Aug.2010 (18.08.2010) [0043]-[0057] of the description, figs. 7-17	15-17,22-25

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 Mar.2012 (21.03.2012)	**29 Mar. 2012 (29.03.2012)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer ZHONG, Yi Telephone No. (86-10)62411594

Form PCT/ISA /210 (second sheet) (July 2009)

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/076338

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	CN101834974A (BOLI MALJIE COMMUNICATION SHENZHEN CO LTD) 15 Sep.2010 (15.09.2010) claims, [0076]-[0091] of the description, figs. 1-26	25-37
Y	WO2008131313A2 (TIAN et al) 30 Oct.2008 (30.10.2008) The whole document	2-3, 25-37
X	US2006266921A1 (KANG et al) 30 Nov.2006 (30.11.2006) Figs.7-10	1,38,40,41,45
X	JP2005526458A (MICRON TECHNOLOGY INC) 2 Sep.2005 (02.09.2005) Fig. 3	1,38,40,41,45
E	CN102244083A (BORIS MULTI-MEDIA HOLDINGS INC) 16 Nov.2011 (16.11.2011) The whole document	1-5,20-33
E	CN102263114A (BORIS MULTI-MEDIA HOLDINGS INC) 30 Nov.2011 (30.11.2011) The whole document	1-46

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/076338

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN101345248B	14.07.2010	CN101345248A	14.01.2009
		WO2009006776A1	15.01.2009
		EP2172973A1	07.04.2010
		US2010141771A1	10.06.2010
		KR20100057599A	31.05.2010
		CA2705315A1	15.01.2009
		INMUMNP201000137E	16.07.2010
		JP2010532869A	14.10.2010
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/076338

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
		KR20060122136A	30.11.2006
		KR100665177B1	09.01.2007
		US7348539B2	25.03.2008
		TW200642077A	01.12.2006
		CN100481479C	22.04.2009
		TW306308B1	11.02.2009
		JP4418443B2	17.02.2010
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		CN100375539C	12.03.2008

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/076338

A. CLASSIFICATION OF SUBJECT MATTER

H01L27/146（2006.01）i
H04N5/335（2011.01）i

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国际检索报告

国际申请号
PCT/CN2011/076338

A. 主题的分类

见附加页

按照国际专利分类(IPC)或者同时按照国家分类和 IPC 两种分类

B. 检索领域

检索的最低限度文献(标明分类系统和分类号)

IPC： H01L

包含在检索领域中的除最低限度文献以外的检索文献

在国际检索时查阅的电子数据库(数据库的名称，和使用的检索词（如使用）)

CNABS，CNKI，WPI，EPODOC：感光 象素 镀膜 纳米 颗粒 pixel photo sensitive lens signal

C. 相关文件

类 型*	引用文件，必要时，指明相关段落	相关的权利要求
X	CN101345248B（博立码杰通讯（深圳）有限公司等）14.7 月 2010（14.07.2010）说明书实施例，附图 5-16	1，4-14，18-21，38-46
Y		2-3，15-17，22-37
Y	CN101740587A（博立码杰通讯（深圳）有限公司）16.6 月 2010（16.06.2010）附图 9-14	15-17
Y	CN101807590A（博立码杰通讯（深圳）有限公司）18.8 月 2010（18.08.2010）说明书第[0043]-[0057]，附图 7-17	15-17，22-25
Y	CN101834974A（博立码杰通讯（深圳）有限公司）15.9 月 2010（15.09.2010）权利要求书，说明书第[0076]-[0091]，附图 1-26	25-37

☒ 其余文件在 C 栏的续页中列出。 ☒ 见同族专利附件。

* 引用文件的具体类型：

"A" 认为不特别相关的表示了现有技术一般状态的文件

"E" 在国际申请日的当天或之后公布的在先申请或专利

"L" 可能对优先权要求构成怀疑的文件，或为确定另一篇引用文件的公布日而引用的或者因其他特殊理由而引用的文件（如具体说明的）

"O" 涉及口头公开、使用、展览或其他方式公开的文件

"P" 公布日先于国际申请日但迟于所要求的优先权日的文件

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"&" 同族专利的文件

国际检索实际完成的日期	国际检索报告邮寄日期
21.3 月 2012（21.03.2012）	**29.3 月 2012 (29.03.2012)**
ISA/CN 的名称和邮寄地址： 中华人民共和国国家知识产权局 中国北京市海淀区蓟门桥西土城路 6 号 100088 传真号： (86-10)62019451	受权官员 钟翊 电话号码：(86-10) **62411594**

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C(续). 相关文件

类　型	引用文件，必要时，指明相关段落	相关的权利要求
Y	WO2008131313A2（TIAN 等）30.10 月 2008（30.10.2008） 全文	2-3, 25-37
X	US2006266921A1（KANG 等）30.11 月 2006（30.11.2006） 图 7-10	1，38，40，41，45
X	JP2005526458A（微米技术有限公司）02.9 月 2005（02.09.2005） 附图 3	1，38，40，41，45
E	CN102244083A（博立多媒体控股有限公司）16.11 月 2011（16.11.2011） 全文	1-5，20-33
E	CN102263114A（博立多媒体控股有限公司）30.11 月 2011（30.11.2011） 全文	1-46

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国际检索报告

关于同族专利的信息

国际申请号
PCT/CN2011/076338

检索报告中引用的专利文件	公布日期	同族专利	公布日期
CN101345248B	14.07.2010	CN101345248A	14.01.2009
		WO2009006776A1	15.01.2009
		EP2172973A1	07.04.2010
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		CA2705315A1	15.01.2009
		INMUMNP201000137E	16.07.2010
		JP2010532869A	14.10.2010
CN101740587A	16.06.2010	无	
CN101807590A	18.08.2010	无	
CN101837974A	22.09.2010	无	
CN102244083A	16.11.2011	无	
CN102263114A	30.11.2011	无	
WO2008131313A2	30.10.2008	WO2008131313A3	11.12.2008
		US2009152664A1	18.06.2009
		EP2143141A2	13.01.2010
		US2010187404A1	29.07.2010
		US2010187408A1	29.07.2010
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		CN102017147A	13.04.2011
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		US2011303897A1	15.12.2011
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		TW200642077A	01.12.2006
		CN100481479C	22.04.2009
		TW306308B1	11.02.2009
		JP4418443B2	17.02.2010
JP2005526458A	02.09.2005	CN100375539C	12.03.2008

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国际检索报告
关于同族专利的信息

国际申请号
PCT/CN2011/076338

检索报告中引用的专利文件	公布日期	同族专利	公布日期
		US2003211405A1	13.11.2003
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		AU2003269305A1	02.12.2003
		US6783900B2	31.08.2004
		EP1506679A1	16.02.2005
		KR20050003456A	10.01.2005
		CN1669332A	14.09.2005
		EP1506679B1	27.12.2006
		KR100621086B1	14.09.2006
		DE60310706E	08.02.2007
		DE60310706T2	11.10.2007

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国际申请号
PCT/CN2011/076338

A. 主题的分类

H01L27/146（2006.01）i

H04N5/335（2011.01）i

SAMSUNG EX. 1002 - 2193/2862

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
17 July 2014 (17.07.2014)

WIPO | PCT

(10) International Publication Number
WO 2014/110484 A2

(51) International Patent Classification:
H01L 27/146 (2006.01)

(21) International Application Number:
PCT/US2014/011236

(22) International Filing Date:
13 January 2014 (13.01.2014)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/751,787 11 January 2013 (11.01.2013) US
61/759,996 1 February 2013 (01.02.2013) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

WO 2014/110484 A2

(54) **Title**: NEXT GENERATION IMAGING METHODS AND SYSTEMS

(57) **Abstract**: Novel imaging arrangements are detailed. One comprises an optical array sensor with plural photo-electron generating regions dispersed at two or more layers in the structure. Two of these photo-electron generating regions are vertically separated by at least 10 microns - making the sensor useful for sensing objects at focal distances ranging from less than ten inches, out to infinity. The photosites may be spectrally selective. One such arrangement includes a top CMOS sensor array that passes 25% or more of the visible incident light into the structure. A second CMOS sensor array can be provided at a bottom of the structure, for receiving light that was not transduced to photo-electrons elsewhere in the sensor. Another arrangement involves movement of a camera sensor, in a repetitive tracking/pop-back motion, to reduce motion blur in individual frames of a video sequence. A great number of other arrangements are also detailed.

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NEXT GENERATION IMAGING METHODS AND SYSTEMS

Related Application Data

In the US, this application claims priority to copending provisional applications 61/751,787, filed January 11, 2013, and 61/759,996, filed February 1, 2013

Field of Technology

The present technology relates to camera systems.

Background and Introduction

Foveon, Inc. (now Sigma Corporation) produces image sensors comprising an array of photosites, each of which includes three vertically-stacked photodiodes. Each of the three photosites responds to different wavelengths of light (i.e., each has a different spectral sensitivity curve). The Foveon technology is detailed, e.g., in patents 6,727,521, 6,731,397, 6,841,816, 6,958,862, 6,998,660, and 7,339,216.

Lytro, Pelican Imaging and others produce light field cameras that capture 4D light field information about a scene, through use of microlenses. Such "plenoptic imaging" systems are detailed, e.g., in patent publications 20070252074, 20080131019, 20080266655, 20100026852, 20100265385, 20110069189, 20110080487, and 20110122308.

Various companies have developed transparent semiconductors, transistors and electrodes useful in CMOS image sensors. Exemplary technology is detailed in Samsung's patent applications 20110156114 and 20090101948. Familiar transparent electrode materials include tin-doped indium oxide, zinc oxide, and carbon nanotube films. Additional information is provided in Ginsley, et al, Handbook of Transparent Conductors, Springer, 534 pp., 2011.

The artisan is presumed to be familiar with technologies involved in fabrication of semiconductor image sensors, including the foregoing.

In accordance with one aspect of the present technology, photosensors are again stacked. However, the stacking is considerably thicker than the prior art, making possible

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camera sensors that provide multi-focal length imaging, e.g., between six inches and infinity.

Fig. 1 introduces certain concepts used in the technology. Plural layers P1 – P8 are stacked in an integrated structure, behind a lens system. Each layer comprises one or more photodetectors. The distance of each layer behind the lens corresponds to a different object distance, in accordance with the focal length of the lens. (I.e., the reciprocal of the object-lens distance, plus the reciprocal of the photodetector-lens distance, equals the reciprocal of the lens focal length.)

An image sensor can comprise a 2D array of such stacks, as illustrated schematically in Fig. 2.

The foregoing and many other features and advantages of the present technology will be apparent from the following detailed description, which proceeds with reference to the accompanying drawings.

Brief Description of the Drawings

Fig. 1 shows a stack comprising plural photodetectors.

Fig. 2 shows an array comprising a 2D array of the stacks of Fig. 1.

Fig. 3 shows a basic implementation using two stacked image sensors.

Fig. 3A shows an image sharpness curve for the implementation of Fig. 3.

Fig. 4 is similar to Fig. 3, but shows four stacked image sensors.

Figs. 5-8 show other variants employing stacked image sensors.

Fig. 9 shows a sparse color filter array.

Fig. 10 illustrates how photosites in different layers of a stack can be at different positions in the layers.

Fig. 11A show how the various photosites in the Fig. 10 arrangement may spatially relate, when viewed down through the stack.

Figs. 11B and 11C are similar to Fig. 11A, but illustrate other spatial relations.

Figs. 12A and 12B show different tree structures, by which photosites can be arranged relative to charge-conducting electrodes.

Fig. 13 is a diagram illustrating movement of a smartphone sensor as a function of time.

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Fig. 14 is a schematic illustration of part of a smartphone camera system according employing certain aspects of the present technology.

Figs. 15A and 15B illustrate 2D motion of a smartphone sensor as a function of time.

Figs. 16 and 17 outline the evolution of imaging systems, culminating with "Era 5" – the subject of the present technology.

Detailed Description

Fig. 3 shows a first particular embodiment, including first and second stacked image sensors, and a lens system. The first sensor is at an image plane corresponding to an object at an infinite distance from the lens system; the second sensor is at an image plane corresponding to an object at a distance of six inches. The two sensors have the same pixel dimensions (e.g., 1936 x 2592 pixels).

The first sensor is fabricated to pass at least some of the light incident on its top surface through its structure, and on towards the second image sensor. Such transmissivity can be achieved by appropriate design and fabrication of the charge transfer conductors and associated readout circuitry, so that some light passing through the photodetection region is not blocked by such structures. For example, the structures may be sized and placed so that gaps between them allow for the passage of some light. Some of the circuitry may be positioned to the periphery of the sensor – where light passage is not an issue. Still further, some of the conductors/circuitry can be fabricated using optically-transparent materials.

In the illustrated embodiment, the top sensor absorbs 25% of the incident light, and passes 75%. But this number is not critical. Even if it passed a tenth of this amount or less (e.g., 5%), advantageous results associated with the Fig. 3 arrangement would still be realized.

Light passing through the first sensor enters an optically transmissive medium. The thickness of the medium depends on the range of focal distances to be accommodated. An exemplary thickness for this medium is 100 microns, but depending on particular application requirements this thickness may be as small as 10 microns, or as large as many hundreds of microns.

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The medium can comprise various materials. Air is attractive for certain optical properties. However, interfaces between air and other optical materials are sometimes disfavored. Another suitable medium is glass. Another is a semiconductor. Still another is a fluid. Combinations can, of course, be used.

Light exiting this medium is incident on the second image sensor. This second sensor can be conventional in structure.

When a subject is at an infinite distance from the lens, the lens presents a focused image on the top sensor. Very high resolution sampling of this image is achieved by the top sensor (in accordance with the sensor's physical resolution).

Part of that focused light energy on the top sensor from the infinite-distance object passes through the first sensor, and through the intervening medium, and falls on the second sensor. There the image is no longer focused. The strong edges and contrasts that are associated with a focused image are lost. A very low contrast, highly blurred image results.

For an object at six inches distance from the lens, the situation is reversed. The lens casts a focused image on the bottom sensor (albeit with some of the light absorbed by its passage through the top sensor), yielding high resolution image data from the bottom sensor. At the top sensor, in contrast, the image is out of focus – with low contrast.

Not shown in Fig. 3 is an ancillary system that collects data output from the two image sensors, and makes them available for post-processing. In one mode, this post-processing can comprise simply adding output signals from corresponding pixels in the first and second sensors, yielding a frame of output image data having the same dimensions as the image data from the first and second sensors. (The output signals from the first sensor may be scaled by a factor of three to compensate for the fact that the bottom sensor receives three times the light absorbed by the top sensor.)

If the post-processing operation adds the images from the first and second sensors, an image sharpness curve like that shown in Fig. 3A results. At an object distance of six inches, maximally-sharp imagery is output by the second sensor. The first sensor, however, outputs a maximally-blurred image in this situation – contributing a low contrast noise signal.

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At distances greater than six inches, the image output by the second sensor becomes increasingly blurred – reducing the net sharpness of the combined output signal.

As the object distance approaches infinity, the sharpness of the image output by the first sensor increases – until its maximum value at infinity. Again, a low contrast noise signal is contributed by the other (second) sensor, which outputs maximally-blurred imagery for an object distance of infinity.

The just-discussed principles can be extended to any number of stacked photosensor arrays. Fig. 4 shows an arrangement employing three arrays. Again, the top and bottom sensors are positioned to capture focused images from objects at distances of infinity and six inches, respectively. However, the Fig. 4 arrangement includes a third sensor array positioned to capture focused imagery from objects at a distance of two feet.

The design of this third photosensor array can be similar to that of the top array, e.g., transmissive of part of the incident light (e.g., 75%). In this arrangement, approximately 50% of the incoming light is absorbed before being passed to the CMOS sensor at the bottom of the stack.

This arrangement produces a curve akin to Fig. 3A, but with three humps rather than two.

It will be noted that the third photodetector array in Fig. 4 is closer to the top sensor than the bottom sensor. Yet the top two sensors collect imagery from the largest range of focal distances, i.e., two feet to infinity. This is a consequence of the lens equation.

Figs. 5-8 illustrate still other stacking variants. Fig. 5 shows four sensor arrays. Like Fig. 4, the spacing of the arrays within the stack is non-uniform.

Fig. 6 shows a stack of five sensor arrays – this time with uniform spacing through the stack.

In some arrangements, such as Fig. 7, the sensors can be spaced in a random fashion.

Fig. 8 illustrates that in all such stacked-sensor embodiments, precise alignment of the sensors is not required. Any mis-alignment between sensors can be detected after fabrication (e.g., by analysis of test imagery), and compensated-for in post-processing.

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Nothing has yet been said about color. The human eye is much more sensitive to luminance (brightness) than color. Accordingly, color typically needn't be resolved as finely as luminance for most purpose. (For example, an image sensor with a million photosensor cells may produce only 250,000 samples of red information, and a like number of samples of blue, using a Bayer color filter.)

In the embodiments of Figs. 3 – 8, the bottom photosensor in the stack can employ a Bayer color filter for sampling red, green and blue at different photosites. The upper sensors can include a regular or random distribution of color filters as well, which may be sparse (i.e., some photosites have no filter).

Fig. 9 shows one form of sparse, regular color filter array, which may be tiled across the top image sensor in Fig. 3, or across the top and intermediate image sensors in Fig. 4. (In the latter case, the color filters on the sensors may be spatially staggered relative to each other.) In the depicted color filter array – as with the conventional Bayer pattern – green is sampled twice as frequently as red and blue. A variety of other such patterns, including some that are denser and some that are sparser, are straight-forward to implement.

In a variant embodiment, the component stacked photosensors can produce color information through use of Foveon-like technology. However, if a conventional Foveon sensor is used top the stack, then no light would penetrate to lower layers. One approach is to fabricate a sparse array of Foveon sensor pixels – interspersed with clear pixels. This enables passage of some of the incident light through the clear pixels to lower layers.

Second Class of Embodiments

The arrangements detailed above involve, conceptually – if not necessarily physically, a mechanical configuration of parts. In more sophisticated embodiments, a stacked photosensor structure is achieved in integrated fashion, using familiar semiconductor fabrication techniques (deposition, masking, lithography, doping, etc.).

Returning briefly to Fig. 1, imagine that each of the layers P1 – P8 is a volume of a semiconductor material, into which one or more photosensitive regions has been formed. Such an arrangement is shown in the exploded view of Fig. 10, in which the

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photosensitive regions (sometimes terms photosites) are shown by ovals. Physically, these ovals are three-dimensional in character – akin to M&M candies in configuration – encompassing a junction between a P-doped region and an N-doped region, and a depletion zone through which photo-electrons can be routed for collection (e.g., to charge-accumulating capacitors – not shown).

(In a different arrangement, the depicted ovals are physically realized by component structures that extend a greater distance in the vertical direction than in the horizontal.)

This second class of embodiment permits the size and placement of the photo-electron generating and collecting structures to be tailored as desired, e.g., to optimize quantum efficiency, achieve particular sampling objectives, etc.

For example, within the various layers along the Z-axis, the photosites can be spatially staggered (i.e., in the X-Y plane) to limit vertical occlusion of one by the other.

Fig. 11A shows one pattern of photosites – looking down through the stack along the Z-axis. (Only five photosites are shown, for clarity of illustration.) The photosites are symmetrically spaced within the X-Y boundaries of the stacked column. If each photosite absorbs 100% of the photons propagating vertically down through the stack that encounters the site, the depicted Fig. 11A arrangement would absorb 68% of the total electrons. That is, 68% of the X-Y area is occupied by photosites.

Other arrangements can, of course, be employed. Fig. 11B shows that the photosites in the different layers can be placed in random fashion in X-Y. Although this leads to lower quantum efficiencies, the stochastic sampling thereby effected has other desirable properties.

The photosite regions needn't be circular in aspect. Fig. 11C shows how hexagonal photosites can be employed – yielding still greater photon capture and efficiency.

In a particular arrangement, the Fig. 10 stack is 10 microns on a side, and the photosites have diameters of 1.75 microns. The total stack depth depends on the desired focal range; a stack depth of 100 microns is exemplary. (This roughly corresponds to a common smartphone configuration, which uses an f2.0 lens, spaced 3.85mm from the sensor array, and provides a focus range of six inches to infinity.)

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Continuing with the M&M analogy, the photosites may be of different colors. More accurately, they may have different spectral responses. A simple starting point is to provide each photosite with either a corresponding red, green or blue filter, so that it responds to photons only of the associated wavelength.

While that's a simple conceptualization of the idea, placement of color filters within an integrated circuit complicates its fabrication. Another approach to making different photosites responsive to different spectra is by the phenomenon popularized by Foveon – doping the semiconductor so that photons of different energies are more likely to penetrate to (and be detected in) different depths of the photosensor structure. Different doping can be used in different of the Fig. 2 stacks, so that across a given X-Y plane of the structure, different regions are attuned to different light frequencies. (That is, at a depth of 56 microns, not all photosites are maximally responsive to the same wavelength of light.)

Still another approach to making different photosites respond to different spectra is through use of dichroic mirrors or filters. Put simply, a frequency-selective mirror (thin film-based) can be fabricated under a photosite. If a quantum of light passes the photosite without dislodging a photo-electron, it next encounters the thin film structure. The dimensions of this structure are chosen to induce a reflection of certain wavelengths of light. Such light is reflected back towards the photosite it just passed (i.e., vertically, up through the stack) – giving this quantum of light a second chance to kick a photo-electron out of the semiconductor material in that photosite.

Yet another approach to realizing photosites having different spectral selectivities is through use of quantum dot material. Work at MIT's Tisdale Lab, at Delft University, and Invisage, has demonstrated use of quantum dot and film materials in image sensors. Related work is detailed, e.g., in Prins et al, Fast and Efficient Photodetection in Nanoscale Quantum-Dot Junctions, Nano Letters, Vol. 12, No. 11, October, 2012, pp. 5740-5743; Konstantatos et al, Solution-Processed Quantum Dot Photodetectors, Proc. IEEE, Vol. 97, No. 10, pp. 1666-1683, October, 2009; and in patent publications 7,476,904, 20070132052, 20110101205, 20110226934, 20100187404, and 20130032782.

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A particular implementation employs quantum dot material to transduce photons in the visible region into a short burst (e.g., nanosecond-scale burst) of electron/exciton energy, which is then measured and correlated to wavelength of the existing photon.

In one illustrative embodiment, such quantum dot transducers (with a scale of 2 – 20 nm) are distributed in a sensing volume 100 microns in thickness. Each quantum dot effectively serves as a photon-transduction pulser, with the pulse size (strength) correlating to incoming photon wavelength (i.e., color). Depending on implementation, there may be thousands of such dots per square micron through the device. The pulses may be quantized (desirably near the sites) to 6- or 8-bits of resolution.

While imaging science has long been fixated on tri-color systems (red/green/blue, and cyan/magenta/yellow), such arrangements optically pale in comparison to the capabilities of the human vision system. Better is to employ a richer spectral vocabulary. Thus, the spectral responses of the photosites employed in the present technology desirably are of more than three types (although in certain embodiments, single-, two- or three-spectral responses can be used). Four is on the low side. Different spectral responses numbering eight or more are be preferred.

In this regard, reference is made to published patent application 20130308045. It details, e.g., how multiple different (sometimes complex) spectra can be used to illuminate an object, so as to permit the object's spectrometry to be assessed more accurately than is possible with conventional R/G/B technology. In like fashion, use of multiple different spectral sensitivities by different photosites in the present technology similarly enables color imaging that exceeds the limitations of traditional tri-color systems.

Five years from now, smartphones desirably will include both the technology detailed in the just-cited application, and the sensor technology detailed herein.

Returning to and stretching the M&M analogy a bit, the electrons collected by the various photosites need to be routed for collection – typically by charge-storage capacitors (which may be formed at the bottom of the sensor array – beneath the last photosensitive regions). This routing can be effected by conductive electrodes (vias) that pass – typically vertically – through the integrated structure. In some implementations, these conductive electrodes are bundled – forming trunk-like structures. In such case, the

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M&M photosites may be regarded as leaves on branches (horizontal electrodes) that extend from this vertical trunk.

Transparent electrode materials can be used to limit absorption of light within the bulk of the structure. Nanowires can be employed for the vertical vias in the photosensor array. (See, e.g., Fan et al, Electrical and Photoconductive Properties of Vertical ZnO Nanowires in High Density Arrays, Applied Physics Letters, Vol. 89, No. 21, 2006; and patent publications 20070155025 and 20110315988.)

Figs. 12A and 12B illustrate the concept of such a tree. The trunk (comprising plural conductive vias) is represented by the darker vertical line. Photosites are coupled to the component electrodes of the trunk, for routing of their photo-electrons to charge-storing capacitors. Fig. 12A shows a regularly-arranged configuration. Fig. 12B shows one with more randomness.

These figures, of course, show only two dimensions. It will be recognized that additional photosites can exist in the third dimension, and can be similarly coupled to the tree trunk.

Note, too, that the number of photosites in each layer of the tree can be different. The photosites within any X-Y layer needn't be regularly and uniformly distributed. Some regions of a layer may be locally dense with photosites, while others can be relatively sparse. As with other design choices, application constraints will commonly dictate such details in any particular embodiment.

Although not shown in Fig. 10, a conventional image sensor (e.g., CMOS or Foveon) may be formed – or affixed – at the bottom of the integrated photosensor stack, to collect any remaining photons not transduced by the photosites throughout the volume.

Returning to Fig. 1, the illustrated light rays captured from nearby "Object 2," and focused by the lens down into zone P7, first pass through all of zones P1 – P6. The artisan will recognize that such light can kick-out photo-electrons in any of these zones P1-P6, on its way to P7.

Moreover, while the light rays converge in zone P7, they may pass through even that zone, and end up kicking-out photo-electrons in zone P8.

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Thus, all of the component zones may output electron charge due to light from Object 2. However, the electron count produced by zone P7 will exceed that from any of the other zones, due to the increase in the electric field near the focal zone.

Further Information on Blur and Sampling

Additional technical insight into the present technology may be gained by examining the important difference between what is popularly called "blur" on the one hand, and what may be called Explicit Angular Sampling, or just angular sampling.

One might say that blur is a physical phenomenon that has rather strict "depth of field" implications – primarily driven by the classic f-number of a lens being used, while angular sampling happens to be a core design principle of most embodiments of this technology, and helps explain why classic depth of field challenges can be overcome.

It is exceedingly well known in signal sampling theory and practice that the discrete sampling of a signal (one dimensional, two, or even three) needs only be slightly finer that the local undulatory properties of a signal (expressed deliberately in lay terminology to make the point). More colloquially, if it wiggles, sample it at three to five points per wiggle, and you should be fine. More technically, whereas Nyquist suggests that taking only two discrete samples per cycle of the highest frequency of a signal may suffice, engineering practice suggests a slight "oversampling" of a signal is desired for good measure, as it were.

Keeping the underlying issues still high-level (intuitive and even slightly pedestrian if the reader is a trained optical engineer), let us look at a simple scenario: a 4 millimeter focal length smart phone camera with an f2 aperture, or 2 millimeter aperture. We can further assume that the best focus "spot size" for a focused point is 2 microns. Simple ray-theory depth of field arguments tell us that for every 4 microns a sensor travels away from the "best focus" plane, the spot size will grow by 2 microns. Thus by 10 microns or so out of focus, the "spot size" of a point has grown to 5 microns. Optical engineers may rightly cringe at this over-simplification of "depth of field," but please tolerate the desire here to just point out that "blur" can happen very easily in modern smart phone cameras even with 10 to 20 micron out-of-focus conditions. 10 to 20 microns matter.

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So continuing on with the pan-audience ray-trace storyline, once a typical f2 lens and planar-sensor is say 40 microns "out of focus," the "blur circle" as it is often called has grown to be 20 microns, 10 times worse than the pristine 2 micron tight-focus capability of the lens. Wiggle-wise, wiggles with ten times less detail need only have ten times sparser sampling, hence any pixels at 2 microns are ludicrously oversampling these "blurred" signals at this out-of-focus plane. In a nutshell, the conventional planar approach to image sampling inherits this rather stark depth-of-field phenomena and the culturally-ingrained idea of focus and blur (lack thereof).

Enter the third dimension of a sensor and the simple notion of sprinkling photosites at various depths inside a sensor, rather than simply in one plane (or three thinly packed planes for color sampling a la RGB and Foveon). In short, distribute 2 micron-ish photosites at various depths of a sensor from the front surface all the way to the furthest optically active surface, typically over a 100 micron thickness at least for a smart phone camera (4mm, f2 or f2.8). As noted, give these 3D splayed photosites various spectral selection properties while you're at it, no need to rigidly adhere to RGB models only (though adhering to these models is acceptable as well).

Nature's Teachings: Light Detection is a 3D Quantum Affair, not a 2D Sampling

Nature has provided us the examples of the faunal retina and the floral chlorophyll for study of light to energy transduction in general. Let's roll with that.

The closest engineering approach perhaps would be to view pixels not as photosites per se, but as micro-waveguides very much borrowing on rod/cone principles and chlorophyll-molecular-chain principles for more efficient photo-electron production. The 10 micron by 10 micron vertical cell cavity arrangement (Fig. 10) with "trees" of active photosites are near the same physical scale as single-mode optical fiber, and thus lend themselves very well to electromagnetic field modeling in the extreme details of semi-conductor and/or "nanotech material deposition" engineering of both the vertical structures as well as the individually active photo-electron generation sites.

Another well-known prior art which is general 2-dimensional in its primary application, but can be adapted easily to three dimensions, is the "dichroic filter." As noted, controlled layering of differing substances with differing optical densities,

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especially at the 1-2 micron scales of the optical photosites, can be an extra widget in the design toolbox as the spectral selection properties of these photosites is determined.

Moveable Sensors

In accordance with a further aspect of the present technology, a sensor in a smartphone or other such video camera system is disposed on a moveable mount, permitting motion of the sensor relative to the rest of the optical assembly (e.g., the lens).

Moveable lenses, sensors, and camera mounts have previously been employed for mechanical image stabilization, and such teachings can be employed in embodiments of the present technology. But the aim of the present technology is somewhat different.

For example, prior art mechanical image stabilization, as used in video cameras and film motion picture cameras, has largely sought to keep static features of a scene at consistent locations, frame to frame – despite unintended movement of the camera (e.g., caused by hand jitter).

When a video camera is moved in a deliberate fashion, e.g., in a panning motion, then arrangements like that marketed under the Steadicam brand are sometimes used to stabilize the camera mount (i.e., the lens and sensor together). This type of stabilization tends to isolate the camera from the operator's undesired, high frequency, movements. More uniform motions, however, such as panning, are not counter-acted by such arrangements.

Contemporary versions of Steadicam-like arrangements employ MEMS-based rate gyrosensors mounted to a gimbaled camera rig, to measure the angular rate of the camera's rotation. Signals from these gyrosensors are used to drive DC servomoters, coupled to the camera's rotational axes, to effect compensatory motions.

The present technology again contemplates panning, or other deliberate movements of the camera. But instead of mitigating motions that are ancillary to the desired movement (as with the above Steadicam-like arrangements), the present technology acts in concert with the desired movement, to reduce frame motion blur caused by such desired movement.

Consider the case of a pan (i.e., a rotation of a video camera around a vertical axis), in which the video camera captures a frame of imagery every thirtieth of a second.

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(The exposure interval of each frame may be 30 milliseconds, and 3.33 milliseconds may elapse between frame exposures.)

If the camera is panned at a rate of six degrees per second, then each successive frame depicts a view through the lens that is advanced, relative to the prior frame, by an increment of 0.2 degrees. This horizontal change in the viewed scene causes an apparent movement of fixed image features across the sensor, also in a horizontal direction. If the camera lens has a field of view of 30 degrees, and projects the imaged scene onto a sensor having 480 columns of pixels, then each degree of view corresponds to 16 columns. From one frame to the next, the 0.2 degree change in camera orientation corresponds to a horizontal shift of about 3 columns of pixels.

In accordance with one embodiment of the present technology, a MEMS or piezo-electric actuator linearly shifts the camera sensor a horizontal distance of 3 pixel columns during the exposure of each of the frames – to counteract the panning-induced movement of the image on the sensor during that exposure period. At the end of the exposure period, the actuator quickly re-traces its travel in an opposite direction, to prepare for exposure of the next frame. This process repeats for each frame, so that the sensor alternately tracks the movement of the panning image, and then pops back to its original position. This operation may be termed a "track-pop" cycle.

Fig. 13 shows the movement of the camera sensor in a horizontal dimension as a function of time. The illustrative sensor has a horizontal dimension of 4.8 millimeters, so that each pixel row is 0.01 millimeters across (i.e., 10 microns). During the course of a single exposure interval, the sensor is moved three pixel rows, or 30 microns. In the brief inter-frame interval, the actuator pops quickly back to its original position.

Fig. 14 (not to scale) schematically shows a section view through part of a smartphone. A lens is positioned above an image sensor. The exterior surface of the lens terminates at a threaded opening into which an accessory lens (e.g., for additional light capture, or for microscopy) can be installed. The lens may include an auto-focus actuator (not shown) that mechanically moves the lens towards or away from the sensor. (If an image sensor of the sort described earlier is employed, then such mechanical focus arrangement is not needed.)

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The sensor is mounted for movement by a MEMS actuator 132, which can translate the sensor towards or away from the actuator. The actuator may provide a range of motion of 50 microns, on each side of the sensor's nominal position (i.e., aligned with the lens.)

It will be recognized that the foregoing description is necessarily simplified, for expository convenience. In actual practice, for example, the sensor may be translated in two directions, e.g. in "x" and "y." Two actuators can be used for this function, or a single, 2D actuator, can be employed. (An example of the latter, using comb electrodes that are controllably excited to move optical elements in two dimensions, is detailed in patent 6,914,710.)

Horizontal panning was assumed in the foregoing example. More generally, the nature of camera movement (e.g., angular panning, linear translation, etc.), and associated movement parameters, are desirably sensed by one or more 3D accelerometers and gyroscopes. Camera movement data can also be discerned from image sensor data, e.g., by tracking movement of scene features in the camera's field of view. Signals output from one or more such sensors are provided to the device processor, which computes the direction, magnitude, and timing of sensor movements that are needed to counteract motion of the image across the sensor during a frame exposure. Corresponding control signals are then sent to the sensor actuator(s).

More particularly, movement of the camera and/or movement of dominant subject matter in a scene both give rise to gross lateral shifts of the light fields falling on a sensor. The dynamic X-Y re-positioning of the sensor attempts to track, as best as possible, the global average of this shift. Desirably, these shifts are sensed, and used to generate appropriate control signals.

One approach is to utilize the now quite ubiquitous MEMS gyroscopes and accelerometers in order to determine the general movement characteristics of a camera on a frame-by-frame timescale. If one infers that a scene is largely not changing, the drive signals applied to the MEMS actuators can simply be an inversion of these measured movements of the camera. A second approach, which can be utilized separately or in combination with the first approach, is to use acquired pixel data from the sensor itself to measure and infer "residual tracking motion," for lack of a better term. In other words, it

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is a known prior art to determine the direction and extent of "motion blur" in a given image, providing for a measured value which after two such frames of such motion blur, can be used to assist in forming the drive signals for the MEMS track-pop actuation signals.

While the foregoing technology is described with reference to linear translation of the image sensor, in other embodiments different sensor movements can additionally, or alternatively, be employed. For example, the plane of the sensor may be tipped and/or tilted, so that its surface normal is non-parallel to the axis of the lens. Similarly, the sensor may be twisted (rotated) along its surface normal axis.

It will be recognized that the physical movement of the sensor needn't precisely counteract the movement of the image projected onto the sensor. Any similarity between such motions is an improvement over none. Likewise, while the exemplary embodiment included a 3.33 millisecond interval between exposures, during which interval the sensor popped back to its original position, this is not essential. The pop-back of the sensor to its original position can occur during the exposure. Due to the brevity of such movement, and the relatively small distance traveled, the consequent impairment of image quality may be acceptable in certain applications.

Additional Details re Light-Field Tracking MEMS

Companies such as Digital Optics Corporation and Tessera Technologies, Inc., among others, currently commercially supply MEMS-based Auto-Focus (AF) devices which provide the Z-axis displacement mechanism between a lens and a 2D sensor. As noted, aspects of the present technology posit use of such MEMS devices to also mechanically actuate motions in both the X and the Y direction: sensor plane relative to the plane of the lens. That is, the sensor would controllably shift at near 1-micron-level resolution relative to the parallel planes of the lens and sensor.

Current MEMs AF device specifications are nicely close to the specifications useful required for track-pop imaging cycles. In particular, full range actuation distances approaching 100 microns or even more are desirable, as will be discussed. Likewise, half-range movements in the single digit millisecond range and preferably even better are

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desirable, though as will be seen, a track-pop cycle program can be adapted to the specifications of whatever a given physical MEMS device can provide.

One aspect of track-pop cycling is to extend the prior art MEMS actuation from one axis to three. One way to do this is to do what many laboratory optical scientists do with much larger actuation stages than MEMS, and that is to simply bolt on a single actuation stage onto a second one but at an orthogonal manner, where the actuation of one stage moves the entire second stage along one given axis, then the second "riding" stage can then move a third body in some orthogonal direction, where that third body become yet a third MEMS actuation stage oriented "push axis" along the remaining orthogonal direction in 3-space (orthogonal to both of the first two stages). This long winded description mirrors the klunkiness and costliness of this approach, but it is important to note that this solution will unequivocally work.

A preferred approach to building 3-axes MEMS devices is to drive toward "close" to the same packaging form factor and dimensions of the current class of AF MEMS devices. The micron-level comb and spring structures currently laid out on nicely planar structures for 1-D AF have to "break the plane" at least in a higher level of assembly, if not at the raw manufacturing level. (In other words, individual one-axis MEMS actuation likely will still be manufactured as a 1-D actuation-axis structure, but it will need to be more finely sliced up, twisted and then re-assembled orthogonally with its identical or nearly identical siblings (other uni-axis actuators). One approach to doing this is to start with a current Z-axis (focus axis) version of a MEMS actuator, and then "float" this stage on two separate rail tracks, the first rail track attaching the top MEMS (the AF stage) to an X-axis stage which is itself pushed and pulled along the rail axis, then below this stage there is a 90 degree rotated rail (from the first rail) which attaches the X stage to the Y stage, with the Y-stage then having a push-pull MEMS structure activating the two stages along the second rail. In this approach, the elegant thin form factor of current AF MEMS devices can be "thickened" outside of the critical optical aperture area and still allow for the seating of a lens in relatively close proximity to a sensor (typically only a few millimeters between the back of a lens surface and the front of a sensor surface).

Once a 3-axis arrangement is in place, whether a klunky version or an elegant and thin one, the operation of shifting a sensor in close "tracking" to a light field projected

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onto that sensor can take place. The specifications of range of motion and response time then become parameters for determining the detailed timing of track and pop imaging. In general, the maximum speed of a MEMS actuation, projected through the focal length of a lens and then onto a scene being imaged, represents the very fastest motion that a scene can move in front of a camera and still be "tracked" by the MEMS motion. Likewise, when a given "tracking" has reached its full motion extent on the MEMS device, a command to end an exposure can take place, then kicking off the "pop" cycle which pops the MEMS actuation back to the other side of its full range. (If a particular MEMS axis represents the "long motion axis" of the current movement of the camera, the other axis will have a "pop" generally not quite as long as its full range).

In such arrangement, individual exposures of "tracked frames" last as long as the full range stroke of the long-motion axis MEMS device. For intuitive grounding of the basic lens and motion parameters, one can imagine a lens with 3.75mm focal length and a MEMS device with 100 microns full range motion. This gives a projected shift of just about 1.5 degrees, which, if one were to be panning (rotating) a camera operating at 30 frames per second, indicates that objects can move up to 45 degrees per second before they start to have residual blur beyond what the tracking can handle. Those practiced in these arts understand this situation is radically more nuanced than this simple example but the "order of magnitude" of how MEMS' full ranges, response times, focal lengths, etc. all play together is important to intuitively outline. Let us not forget as well that the "pop" phase usually posits turning off the exposing activities of the main sensor as the MEMS actuator(s) pop the sensor back to a new tracking starting point, and thus this "pop" time can represent a significant loss of information gathering if MEMS devices are not manufactured with an eye towards fast (ideally faster than one millisecond) full range popping capabilities. Much slower times can easily be made operational, the cost is simply dead time for light gathering.

Figs. 15A and 15B further illustrate the foregoing. Two plots are shown: Fig. 15A shows MEMS actuator displacement of the sensor in the "x" direction, and Fig. 15B is a similar illustration but in the "y" direction. The two actuator waveforms are synchronized, so that the track and pop phases coincide. The "x" actuator travels +/- 30 microns around a nominal position (i.e., from 0 – 60 microns, centered at 30 microns).

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The "y" actuator is operated to move the sensor a smaller displacement, +/- 10 microns around its nominal position. It will be recognized that a single control signal (a timing waveform) can be scaled and offset to generate both the "x" and "y" control signals.

In the illustrated arrangement, the "track" interval (i.e., the frame exposure interval) is 5 milliseconds, and the "pop" interval is 2 milliseconds. Pop intervals that are less than 50% of the track intervals are typically utilized, with more preferable values for the pop interval being less than 20%, 10%, or even less than 5% or 2% of the track interval.

Motion-Stasis-Motion

In accordance with a further aspect of the present technology, an operational mode of the camera is controlled in accordance with a camera gesture. In a particular embodiment, a user signals interest in a scene when a phone is swept along a path to a point where it is briefly held, after which the phone is swept back in a contrary direction. The position at which it is briefly held indicates the user's interest in the scene viewed by the camera from that position.

Data from the phone sensors (accelerometers, gyroscopes, and feature tracking by the camera) are processed to classify the phone as either being in a "motion" phase, or a "stasis" phase. Each phase is characterized by motion parameter thresholds. For example, the "motion" phase may be characterized by any movement at a rate greater than one centimeter per second. (Such velocity can be derived by integrating data from the accelerometer sensor.) Stasis may be characterized by movement at a rate less than 0.5 centimeter per second.

To sense the just-described gesture, the device processor starts by looking for an initial motion phase. When that phase concludes, a time window (e.g., two seconds) starts within which the processor looks for a stasis phase. If stasis is not sensed within that interval (e.g., if the device moves at between 0.5 and 1 cm/second for more than 2 seconds), then the classifier resets – again looking for an initial motion phase.

If a stasis phase is sensed, it must persist for a threshold interval, which may be bounded both by minimum and maximum values. For example, the minimum value may be a value greater than 0.1, 0.2, or 0.5 seconds. The maximum value may be a value less

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than 1, 2 or 5 seconds. If the device is held in a stasis phase for the required threshold interval, then the process next looks for a retracting motion.

A retracting motion is a second "motion" phase, but one in which the motion is in a direction contrary to the initial motion phase. This can be defined mathematically in various ways, but the concept is familiar: if the user takes the phone from a rest position, sweeps it to a stasis position, and then returns it to (or near) the initial rest position, then that latter motion is a retraction motion.

One algorithmic definition begins by defining a first axis, which is that of a first vector between the device's position at the start of the initial motion phase, and its position at the stasis phase. (The actual path might be curved, but the start and end points define a straight line.) A retraction motion is tested by attributes of a second vector: namely, that between the device's position at the stasis phase, and its position at the end of the second motion phase. If this second vector has a component – when projected onto the first axis – that is larger than its projection onto any axis orthogonal to the first axis, and is in a direction opposite to that of the first vector, then the second motion phase is a retraction motion.

Put another way, if the first motion defines a first direction, then the second motion should have a principle component that is oriented in a direction opposite to that first direction, if the second motion is to be classified as a retraction motion.

Image frames may be captured throughout these phases, at a video capture rate (e.g., 30 frames per second). Or, video capture may commence only after device velocity falls below a threshold, e.g., 1 cm/second (such as at the end of the initial motion phase), and may terminate when the device velocity again rises above that threshold (such as at the beginning of the retraction motion phase).

Data from plural such image frames are combined in known fashion to synthesize one or more enhanced images, e.g., increasing the resolution, or extending the field of view, as contrasted with any single captured image frame. Desirably, two or more such composite images are created (e.g., from different virtual viewpoints), and are presented to the user on the device display. The user can flip or scroll between the composite images, using known image review UI paradigms, and select one or more for long term storage (e.g., in the Photo Library or Camera Roll data structures of the Apple iPhone).

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Ideally, the frames of video imagery from which the images presented to the user are composited, are gathered using a sensor of the type earlier described, providing 3D information. In such arrangement, there is no focal plane – outside of which subjects are out of focus. Instead, everything in the composite image is in focus.

Review

A far-from-complete list of some of the inventive arrangements provided by this technology includes the following:

An apparatus having an optical array sensor for use with a lens, where the sensor comprises a structure having a vertical thickness of at least 10 microns, with plural photo-electron generating regions (photosites) dispersed at two or more layers within that thickness (corresponding to differing lens focal planes). Two of these layers are vertically separated by at least 10 microns.

In other embodiments, two of these layers are vertically separated by at least 50 microns. A particular such sensor is useful for sensing objects at distances from the lens ranging from less than ten inches, out to infinity.

In some such arrangements, the photosites are spectrally selective, and there are at least two different types of spectral selection. Commonly there may be four or more. Desirably, the photosites are transmissive to light for non-spectrally-selected wavelengths of light.

In one particular sensor, the structure has a thickness of more than 50 microns, comprises three or more different layers of photosites. These three layers correspond to objects imaged at respective distances of (a) less than 10 inches, (b) between ten inches and three feet, and (c) greater than three feet.

The above-noted sensor may be provided with a first CMOS sensor array atop said structure, which serves as an entry surface onto which light entering the structure is first incident. This CMOS sensor array may pass 25% or more of the visible incident light into said structure.

Similarly, the above-noted sensor may be provided with a second CMOS sensor array at a bottom of the structure, for receiving light that was not transduced to photo-electrons elsewhere in the sensor.

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In some arrangements, both of the just-referenced CMOS sensors are provided, thereby sandwiching the structure. In such a configuration, a first fraction of incoming light is transduced to electrons by the first CMOS sensor atop the structure, another fraction of incoming light is transduced to electrons by the photosites in the structure, and a further fraction of the incoming light is transduced to electrons by the second CMOS sensor behind the structure.

In another particular sensor, there are at least four differing depth layers for the photo-electron generating regions in the structure. Each of these regions comprises plural photosites, and an X-Y arrangement of the photosites in one of said layers is staggered relative to an X-Y arrangement of the photosites in a successive layer.

The just-described sensor may have a density of photosites such that 25% or less of incident light reaches a CMOS sensor array at the back of the structure.

The above-noted sensors may include photosites arranged such that a line normal to the thickness passes through a first photosite in one layer and a second, different photosite in a different layer. These first and second photosites are desirably differently spectrally selective.

The above-noted sensors can include a first gated conduction path that couples a first photosite to a first transfer capacitor, and a second gated conduction path that couples a second photosite to a second transfer capacitor, where the first and second transfer capacitors are optically shielded from incident light.

Such a sensor can further include control circuitry for alternately gating the conduction paths on and off plural times per second, to produce raw video signal charge streams to the transfer capacitors.

Smartphones equipped with the above-described sensors, and a lens, are also contemplated.

The technology also includes an apparatus having a stack of plural photodetectors P_1 - P_N and a lens. The lens introduces light onto a first exterior surface of the stack, for passage through the stack towards a second exterior surface of the stack. The stack positions different of the photodetectors at different distances from the lens, so that they provide dominant responses to light captured from objects at different distances from the

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lens in accordance with the photodetectors' distances from the lens. A distance between photodetectors P_1 - P_N in the stack is at least 20 microns.

Another such sensor includes four or more light-detecting volumes P_1, P_2, P_3 - P_N arranged so that light detected in volume P_2 has first passed through volume P_1, light detected in volume P_3 has first passed through volumes P_1 and P_2, etc.. A distance between volumes P_1 - P_N is at least 20 microns, permitting the sensor to provide object distance information when used with a lens that directs light from an object onto the sensor.

In the just-detailed sensor, the light-detecting volumes can be arranged in a stack along a stack axis. A first of the volumes has a first photosensitive region, and a second of said volumes has a second photosensitive region. A line between centers of these first and second photosensitive regions is not parallel to said stack axis.

Put another way, if the light-detecting volumes are arranged in a stack along a Z axis in an X, Y, Z Cartesian coordinate system, each of the light-detecting volumes each has an extent in X-Y space. In such view, a first of the volumes has a photosensitive region at a first X-Y location, and others of the volumes have respective photosensitive regions at other X-Y locations that are different than the first X-Y location. In such an arrangement, a light ray traveling through the sensor parallel to the Z axis encounters different of said photosensitive regions, depending on the ray's location in X-Y space.

Another arrangement employs a video camera system (e.g., in a smartphone) that includes a lens coupled to a body, and an image sensor (lying in an image plane). A uniform motion of this system (i.e., a deliberate motion, as contrasted with an unintended motion – such as hand jitter, which may also be present) is sensed while capturing video imagery. This capturing of video imagery comprises capturing a still image frame N times a second. The uniform motion of the system results in a uniform movement of image features across the image plane. During this video capture, a uniform physical tracking movement of the image sensor, within the camera body, is repeatedly performed. This tracking movement of the image sensor is in a direction that tracks the uniform movement of image features across the image plane. Each such tracking movement is followed by a uniform popping movement, which returns the image sensor back to an

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original position that it occupied at the beginning of said uniform tracking movement. These tracking and popping movements are repeated N times a second.

In some embodiments, each of the uniform tracking movement has a first time duration, and each of said uniform popping movements has a second time duration, where the second time duration is less than 20% of the first time duration.

The tracking and popping movements of the image sensor can be performed by repetitively and synchronously operating a pair of orthogonally-oriented MEMS actuators.

Other Comments

It will be recognized that references to transparent materials simply refer to a material that does not block 100% of the light energy of interest. A material that intercepts 99% of the light, and passes 1%, is still regarded as transparent. (If only 0.001% of the light passes, it is no longer regarded as transparent. Between .001% and 1% is a range that may or may not be regarded as transparent – depending on the particular application being served.)

While the embodiments of Fig. 3, etc., contemplated that the component image sensors are of the same resolutions, this is not required. In other arrangements the sensors can be of differing resolutions.

The detailed embodiment employs CMOS semiconductor image sensor technology. However, the principles of the detailed arrangement can be applied to any other type of image sensor arrangement, whether presently known (e.g., CCD or organic photosensors) or later developed.

The number of different layers of photosites employed in a particular embodiment is application dependent. Although eight layers are illustrated in Fig. 1, a lesser number (e.g., 3 or 6, etc.) or a greater number (e.g., 9 or 20 or 32, etc.) can be used. If each of the layers is 12 microns in thickness, a stack of eight yields a total stack depth of about 100 microns. A thicker or thinner stack may be desired, depending on the focal length of the lens, and the range of distances from which object images are to be captured. (The stack may be made thicker by increasing the number of photodetectors, or by increasing their component thicknesses.)

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The thicknesses of the photosites can be non-uniform, e.g., in acknowledgement that the photon flux deeper in the structure is diminished by photon absorption in higher layers. Alternatively, or additionally, the gains of the corresponding output amplifiers can be non-uniform – with those driven by photosites deeper in the structure having higher gains than those associated with photosites closer to the lens. Still further, the doping of semiconductor structures in deeper photosensors can be different than the doping of corresponding semiconductor structures in higher photosensors.

While a single lens L is shown in Figs. 1 and 3 for clarity of illustration, it will be recognized that plural lenses can be used, e.g., a compound lens, or a lens for each pixel, or a lens per group of neighboring pixels, or lenticular lenses, etc. Combinations can also be used, e.g., a single object lens, in conjunction with a plurality of microlenses, as is known in certain light field architectures.

The details of the photodetectors, and their respective charge accumulation, latching, switching and reset circuitry are not detailed, as same are within the skills of the artisan in photosensor design.

Applicant's published applications 20110212717, 20110161076, 20120284012, and 20130223673, detail methods and arrangements that are useful in combination with the present technology. Publication 20110212717, for example, teaches that post-processing of sensor data is desirably performed by processing circuitry on the same substrate as the sensing elements. In the present case, such processing circuitry can take the raw signals from the various sensors/photosites, and process them to produce data streams optimized for their intended use (e.g., one data stream optimized for rendering to a user on a screen, another optimized for recognizing text from close focal distances, etc.).

It will be recognized that multiple features are taught by this specification, and different particular embodiments have been detailed that combine different of these features. However, it will be recognized that the features can be combined in myriad arrangements, too numerous to catalog. This disclosure should be regarded as teaching all combinations of the disclosed features.

To provide a comprehensive disclosure without unduly lengthening this specification, applicant incorporates by reference the documents identified herein, as well

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as the documents they respectively reference. All such documents are incorporated in their entireties, as if fully set forth herein. The artisan is presumed to be familiar with the teachings from such references.

5

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Claims:

1. Apparatus comprising an optical array sensor for use with a lens, the sensor comprising a structure having a vertical thickness of at least 10 microns, with plural photo-electron generating regions dispersed at two or more layers within that thickness, said layers corresponding to differing lens focal planes, two of said plural photo-electron generating regions being vertically separated by at least 10 microns.

2. The apparatus of claim 1 wherein said structure includes first and second planar arrays of photodetectors, said first and second planar arrays being vertically separated by at least 50 microns, wherein the sensor is useful for sensing objects at distances from the lens ranging from less than ten inches, out to infinity.

3. The apparatus of claim 1 wherein the photo-electron generating regions are spectrally selective and there are at least two different types of spectral selection.

4. The apparatus of claim 3 wherein the photo-electron generating regions are spectrally selective and there are at least four different types of spectral selection.

5. The apparatus of claim 3 wherein the photo-electron generating regions are transmissive to light for non-spectrally-selected wavelengths of light.

6. The apparatus of claim 1 wherein said structure has a vertical thickness of more than 50 microns, and the sensor comprises three or more photo-electron generating regions at said differing layers, the three regions corresponding to objects imaged at respective distances of (a) less than 10 inches, (b) between ten inches and three feet, and (c) greater than three feet.

7. The apparatus of claim 1 that further includes a first CMOS sensor array atop said structure, serving as an entry surface onto which light entering the structure is

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first incident, said first CMOS sensor array passing at least 25% of visible incident light into said structure.

8. The apparatus of claim 7 that further includes a second CMOS sensor array at a bottom of said structure, said first and second CMOS sensor arrays thereby sandwiching the structure, wherein a first fraction of incoming light is transduced to electrons by the first CMOS sensor atop the structure, and a second fraction of the incoming light is transduced to electrons by the second CMOS sensor behind the structure.

9. The apparatus of claim 8 in which a third fraction of the incoming light is transduced to electrons by photo-electron generating regions in the structure between the first and second CMOS sensor arrays.

10. The apparatus of claim 1 that further includes a CMOS sensor array at a bottom of said structure, for receiving light that was not transduced to electrons elsewhere in the sensor.

11. The apparatus of claim 10 wherein there are at least four differing depth layers for the photo-electron generating regions in the structure, each of the photo-electron generating regions comprising plural photosites, wherein an X-Y arrangement of the photosites in one of said layers is staggered relative to an X-Y arrangement of the photosites in a successive layer, and wherein a density of the photosites is such that 25% or less of incident light reaches the CMOS sensor array at the bottom of said structure.

12. The apparatus of claim 1 wherein there are at least four differing depth layers for the photo-electron generating regions in the structure, each of the photo-electron generating regions comprising plural photosites, wherein an X-Y arrangement of the photosites in one of said layers is staggered relative to an X-Y arrangement of the photosites in a successive layer.

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13. The apparatus of claim 1 in which each of the photo-electron generating regions comprises plural photosites, and a line along a vertical axis passes through a first photosite in one layer and a second, different photosite in a different layer, said first and second photosites being differently spectrally selective, the sensor further including a first gated conduction path coupling the first photosite to a first transfer capacitor, and a second gated conduction path coupling the second photosite to a second transfer capacitor, the first and second transfer capacitors being optically shielded from incident light.

14. The apparatus of claim 13 that further includes control circuitry for alternately gating said conduction paths on and off plural times per second, to produce raw video signal charge streams to said transfer capacitors.

15. The apparatus of claim 12 comprising a smartphone equipped with said sensor and a lens.

16. An apparatus including a vertical stack of plural photodetectors P_1 - P_N and a lens, the lens introducing light onto a first exterior surface of the stack, for passage through the stack towards a second exterior surface of the stack, the stack positioning different of the photodetectors at different distances from the lens, the different photodetectors providing dominant responses to light captured from objects at different distances from the lens in accordance with the photodetectors' distances from the lens, a vertical distance between photodetectors P_1 - P_N in said stack being at least 20 microns.

17. A sensor comprising four or more light-detecting volumes P_1, P_2, P_3 - P_N arranged so that light detected in volume P_2 has first passed through volume P_1, light detected in volume P_3 has first passed through volumes P_1 and P_2, etc., wherein a distance between volumes P_1 - P_N is at least 20 microns, permitting the sensor to provide object distance information when used with a lens that directs light from an object onto the sensor.

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18. The sensor of claim 17 in which:

said light-detecting volumes are arranged in a stack along a stack axis;

a first of said volumes has a first photosensitive region therein, and a second of said volumes has a second photosensitive region therein; and

a line between centers of said first and second photosensitive regions is not parallel to said stack axis.

19. The sensor of claim 17 in which:

said light-detecting volumes are arranged in a stack along a Z axis in an X, Y, Z Cartesian coordinate system, said light-detecting volumes each having an extent in X-Y space;

a first of said volumes has a photosensitive region at a first X-Y location; and

others of said volumes have respective photosensitive regions at other X-Y locations that are different than the first X-Y location;

wherein a light ray traveling through the sensor parallel to the Z axis encounters different of said photosensitive regions, depending on the ray's location in X-Y space.

20. A method employing a video camera system, said system including a lens coupled to a body, and an image sensor, the image sensor lying in an image plane, the method comprising the acts:

sensing a uniform motion of the video camera system while capturing video imagery, said capturing of video imagery comprising the capturing of a still image frame N times a second, said uniform motion of the video camera system resulting in a uniform movement of image features across the image plane, said uniform motion being deliberate rather than unintended;

repeatedly performing a uniform physical tracking movement of the image sensor, within the body, in a direction that tracks said uniform movement of image features across the image plane, followed by a uniform popping movement that returns the image sensor back to an original position it occupied at a beginning of said uniform tracking movement;

wherein said tracking and popping movements are repeated N times a second.

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21. The method of claim 20 in which each of said uniform tracking movements is of a first time duration, and each of said uniform popping movements is of a second time duration, where the second time duration is less than 20% of the first time duration.

22. The method of claim 20 in which said tracking and popping movements of the image sensor are performed by repetitively and synchronously operating a pair of orthogonally-oriented MEMS actuators.

23. A method comprising:

sensing a first movement of a camera-equipped device, the first movement defining in a first direction;

following the sensed first movement, sensing a pause in movement of the device; and

following the sensed pause, sensing a second movement of the device, the second movement defining in a second direction;

wherein said second direction has a principle component that is oriented in a direction opposite to said first direction;

the method further including:

capturing frames of imagery at least during in an interval between the first and second movements of the device;

processing a first data set, comprising plural of said captured image frames, to yield a first composite data set;

processing a second, different, data set, comprising plural of said captured image frames, to yield a second composite data set; and

storing the first and second composite data sets for user review and selection.

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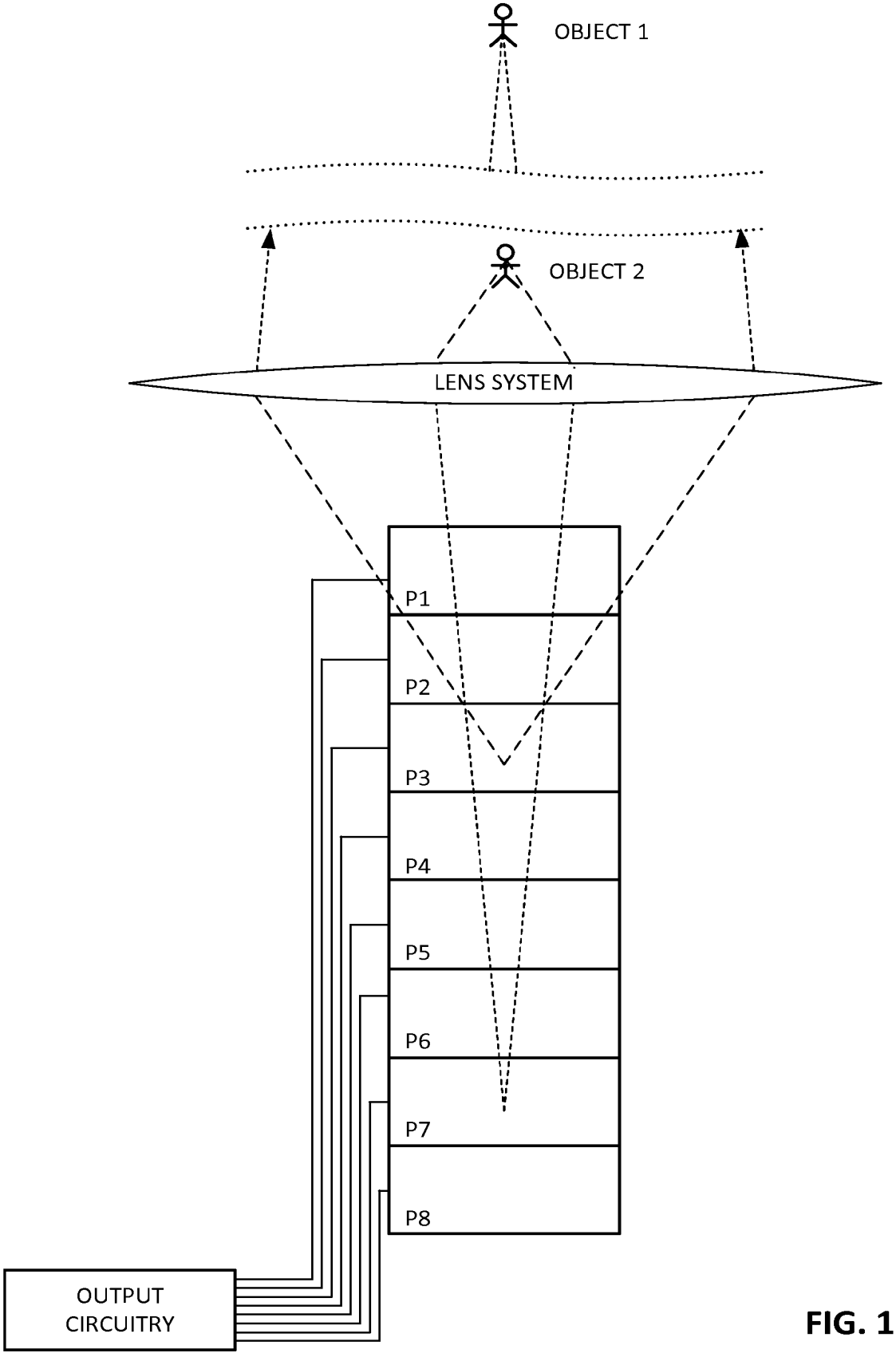
OBJECT 1
OBJECT 2
LENS SYSTEM
P1
P2
P3
P4
P5
P6
P7
P8
OUTPUT CIRCUITRY

FIG. 1

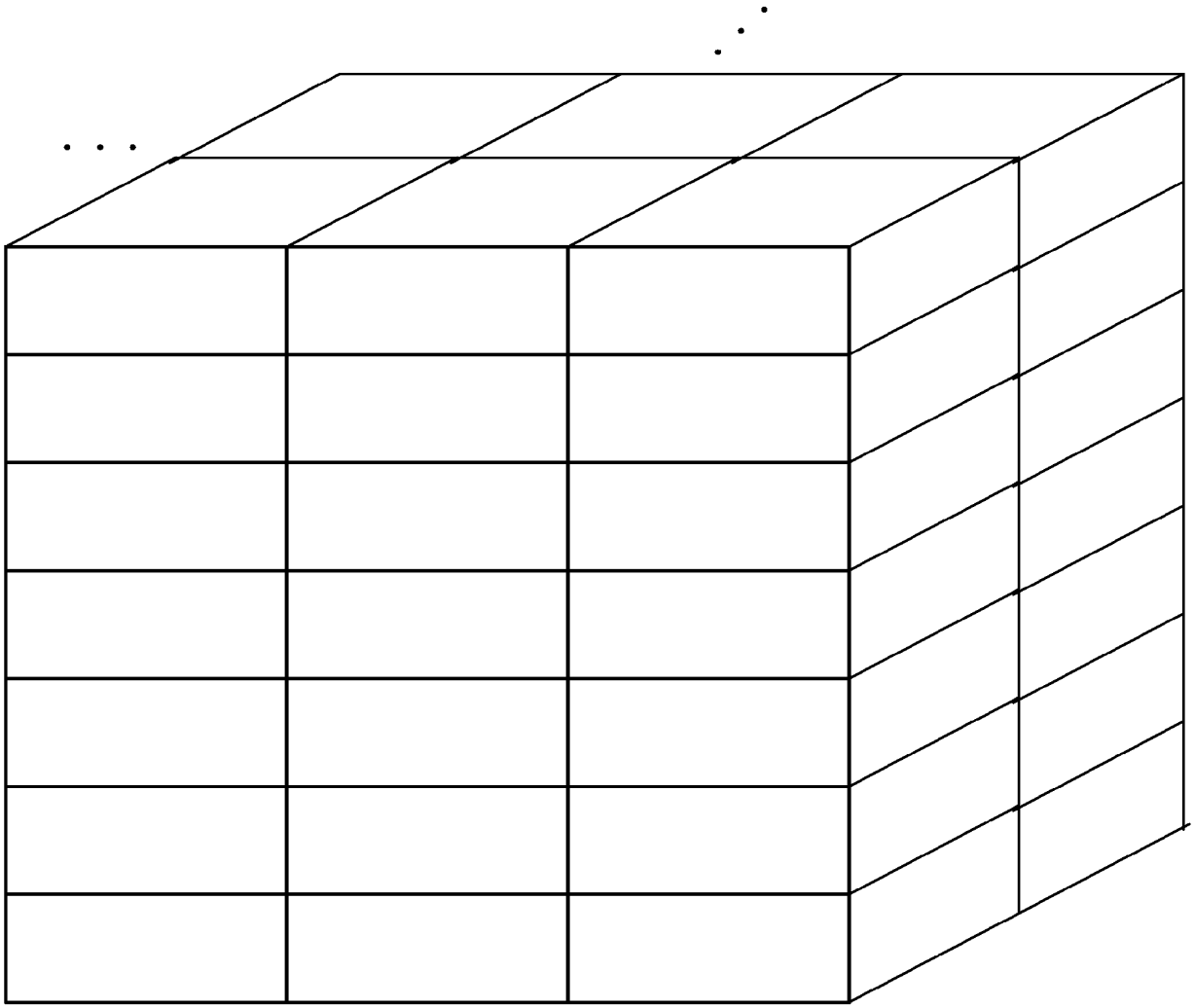

FIG. 2

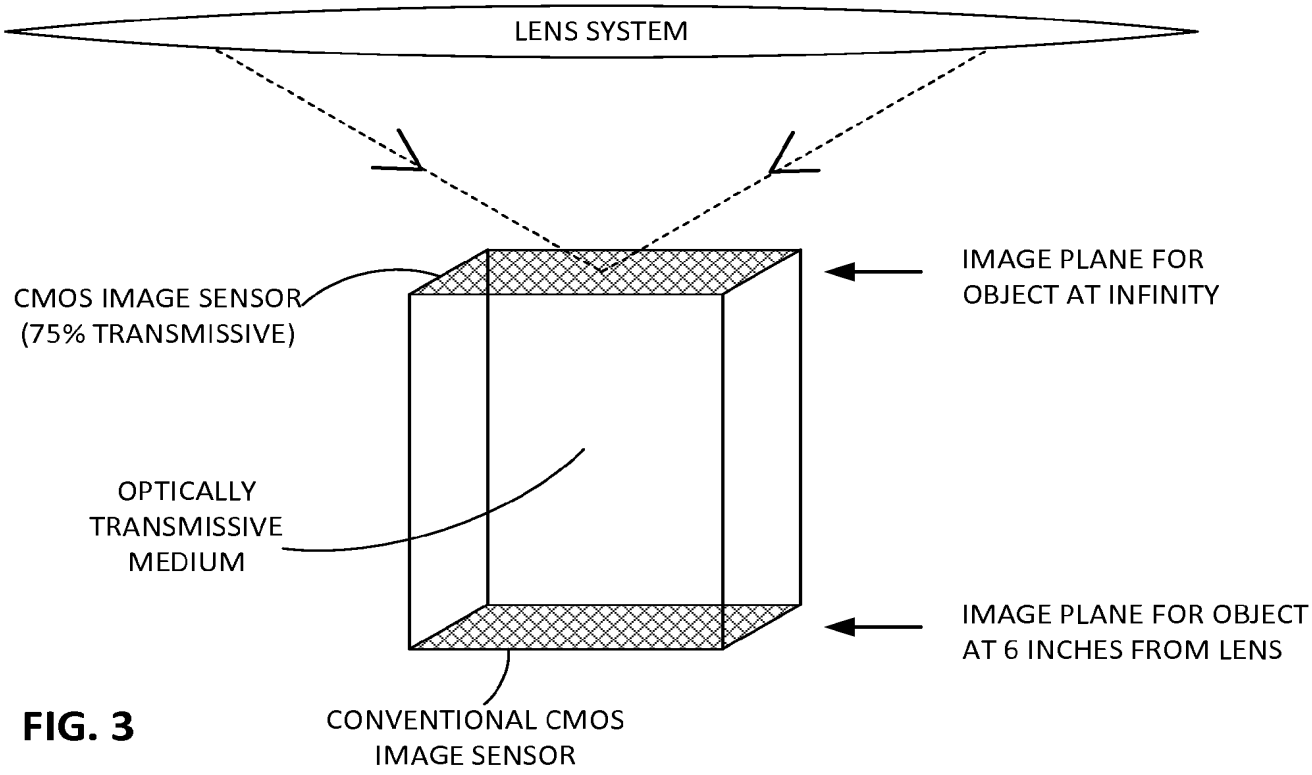
LENS SYSTEM
CMOS IMAGE SENSOR
(75% TRANSMISSIVE)
IMAGE PLANE FOR
OBJECT AT INFINITY
OPTICALLY
TRANSMISSIVE
MEDIUM
IMAGE PLANE FOR OBJECT
AT 6 INCHES FROM LENS
CONVENTIONAL CMOS
IMAGE SENSOR

FIG. 3

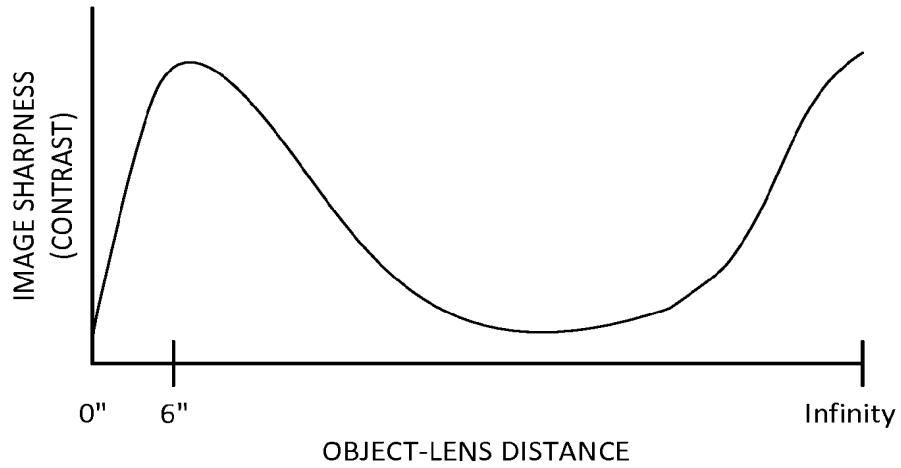
IMAGE SHARPNESS
(CONTRAST)
0"
6"
Infinity
OBJECT-LENS DISTANCE

FIG. 3A

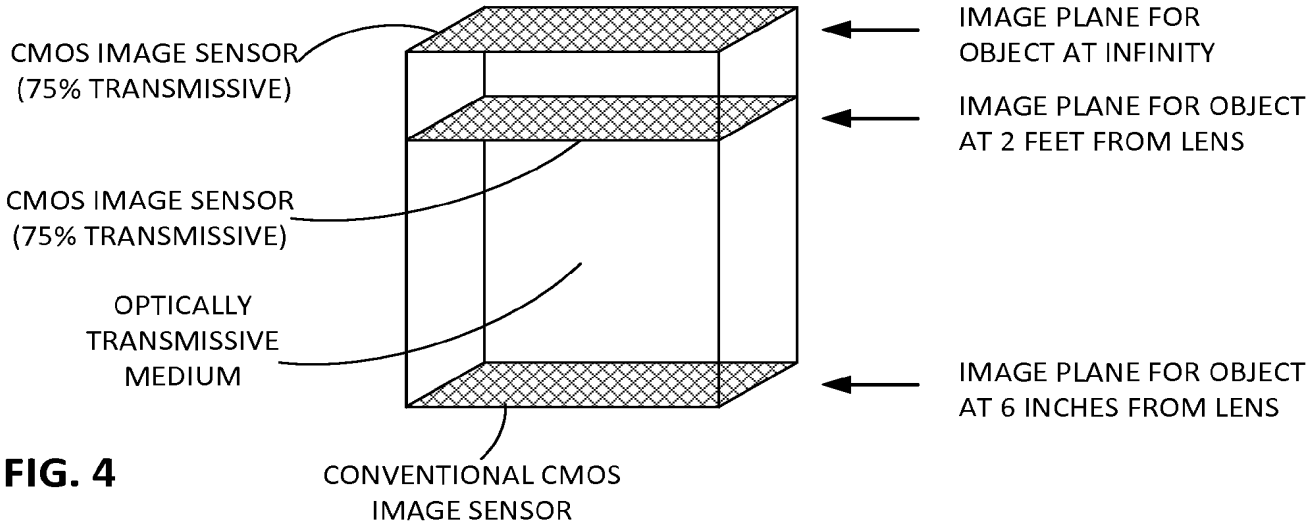

FIG. 4

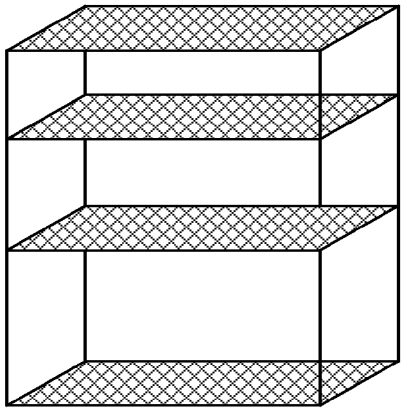

FIG. 5

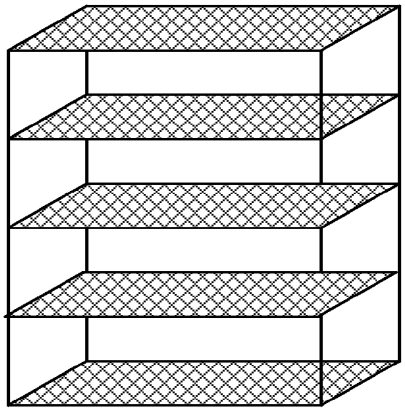

FIG. 6

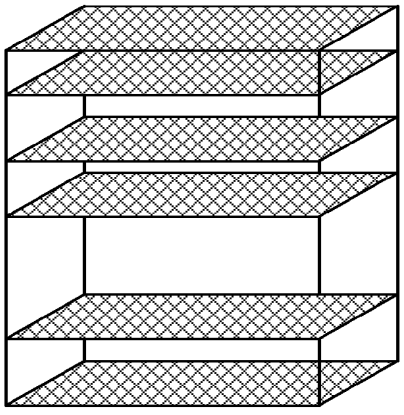

FIG. 7

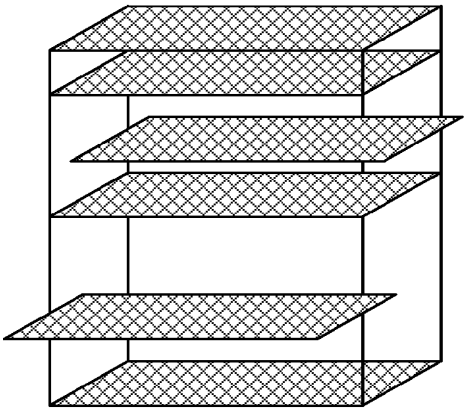

FIG. 8

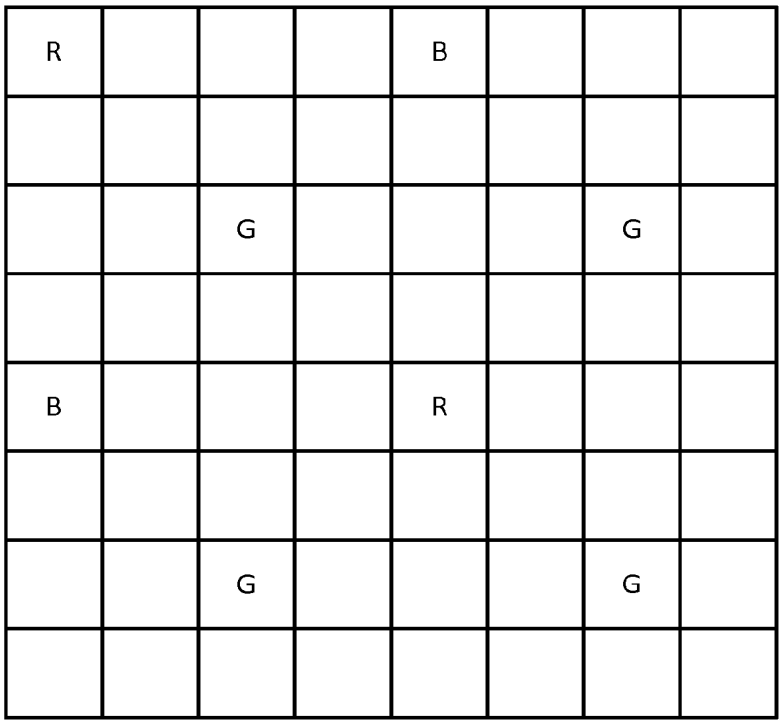

FIG. 9

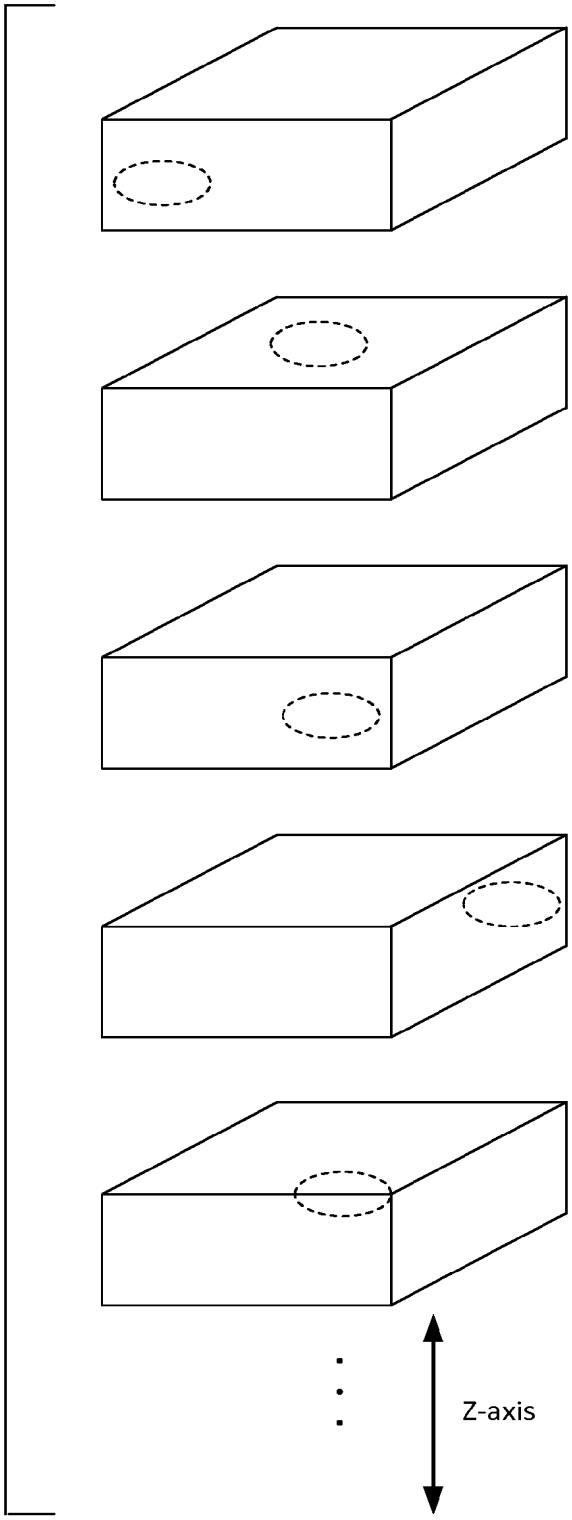

FIG. 10

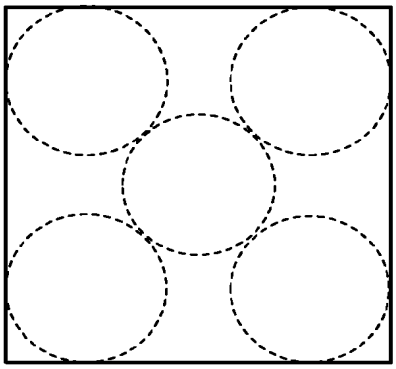

FIG. 11A

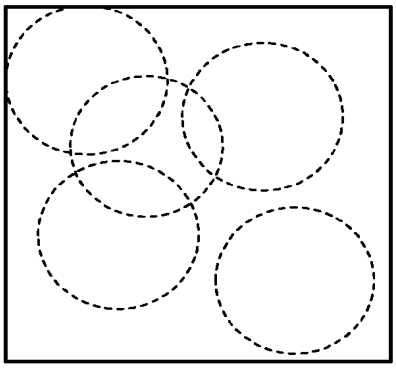

FIG. 11B

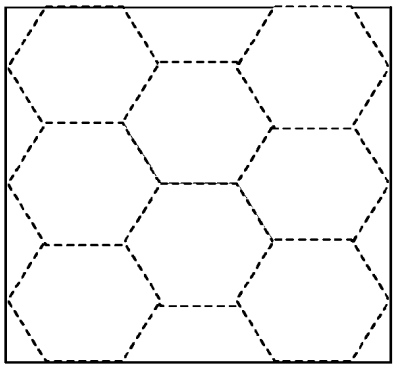

FIG. 11C

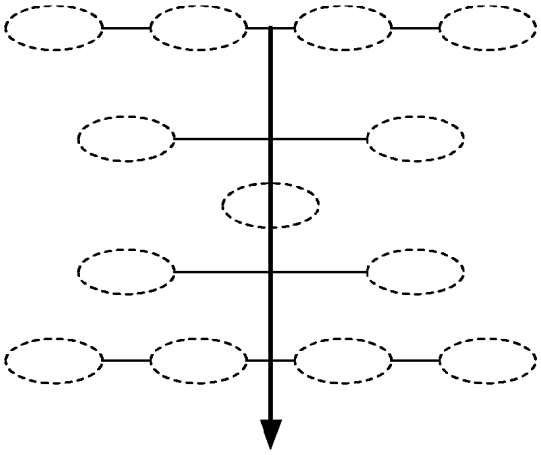

FIG. 12A

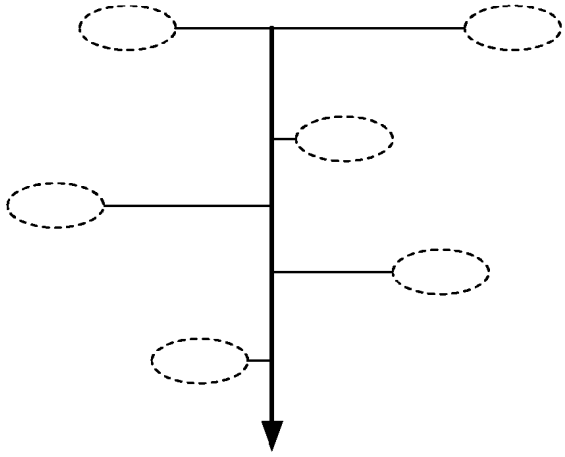

FIG. 12B

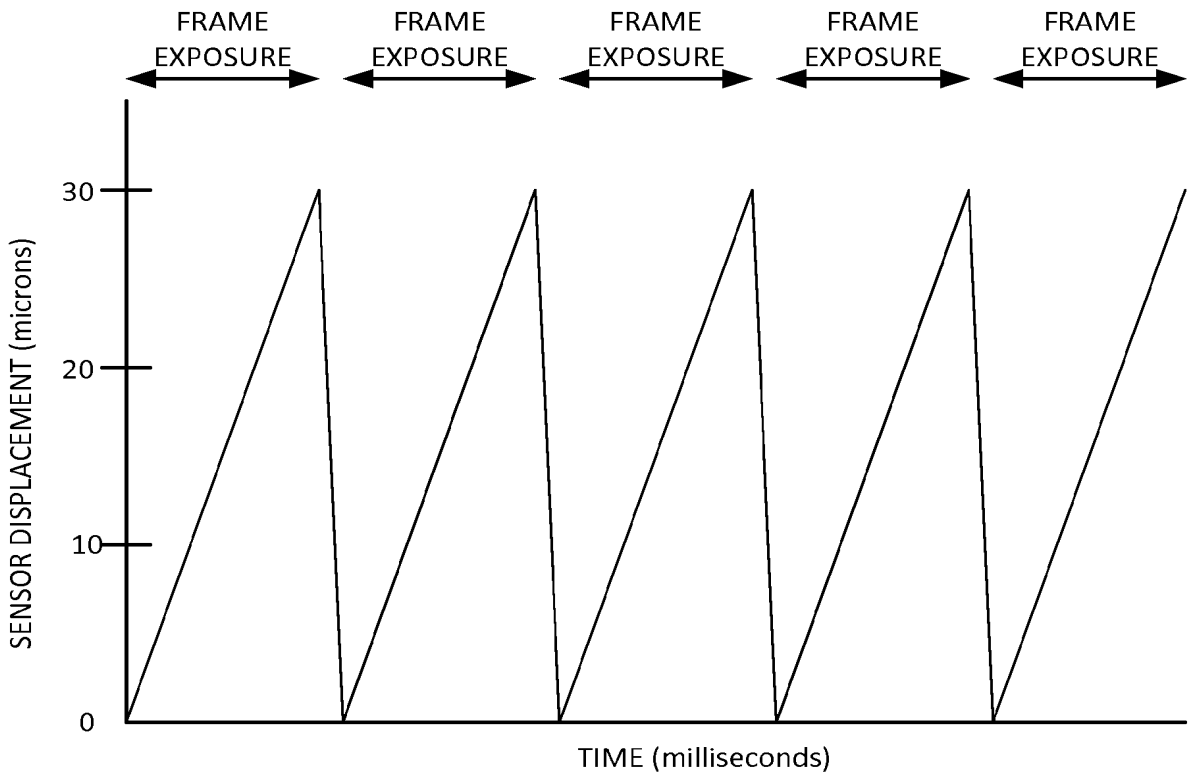
FRAME EXPOSURE
FRAME EXPOSURE
FRAME EXPOSURE
FRAME EXPOSURE
FRAME EXPOSURE
30
20
10
0
SENSOR DISPLACEMENT (microns)
TIME (milliseconds)

FIG. 13

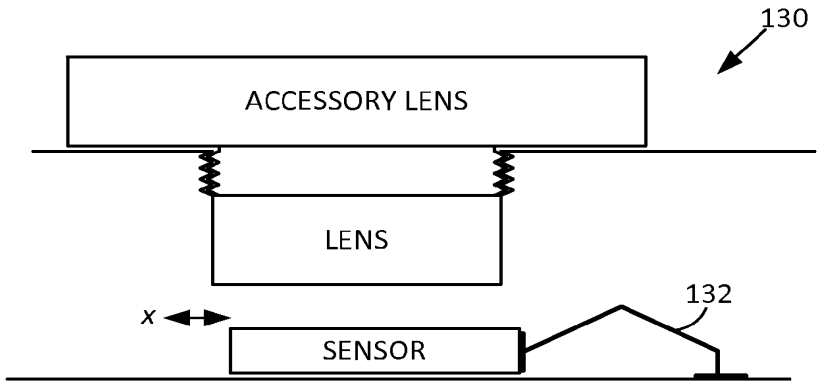
130
ACCESSORY LENS
LENS
132
x
SENSOR

FIG. 14

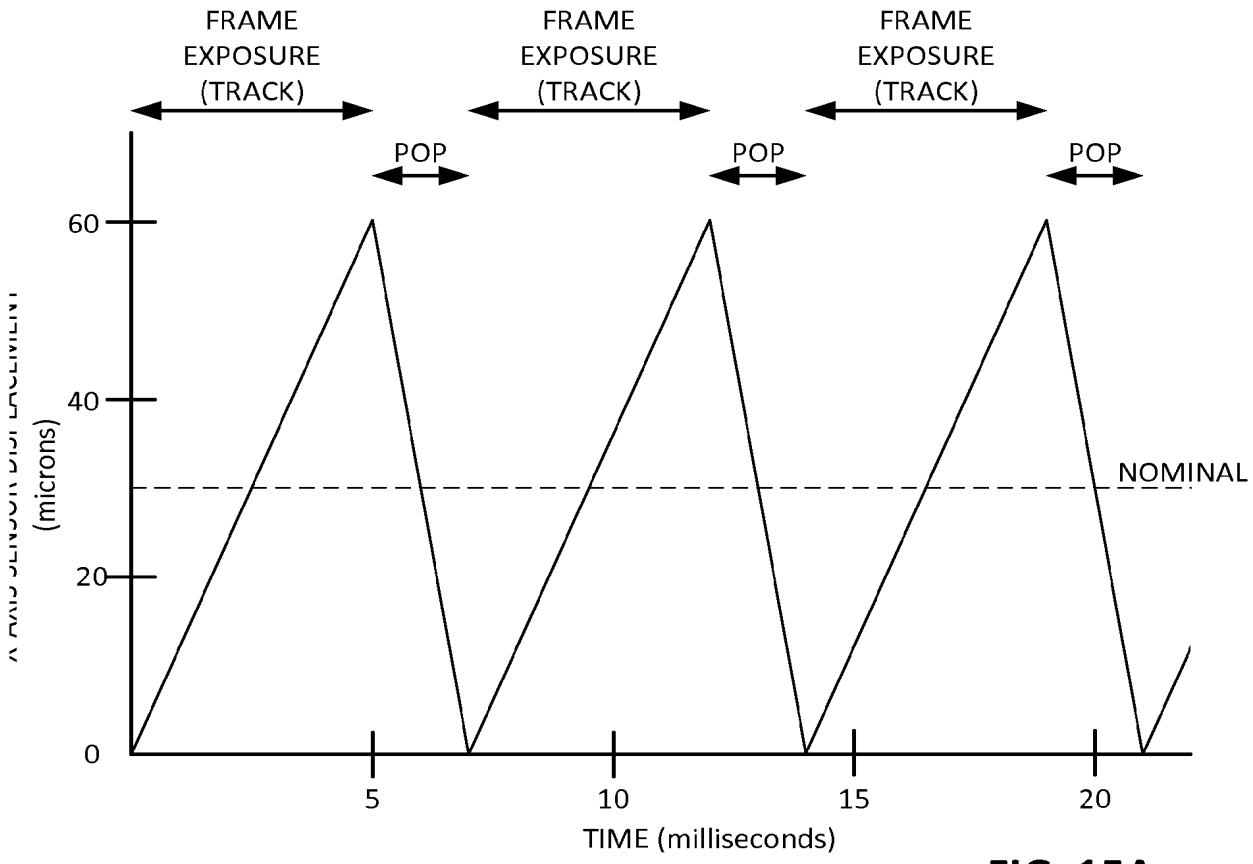

FIG. 15A

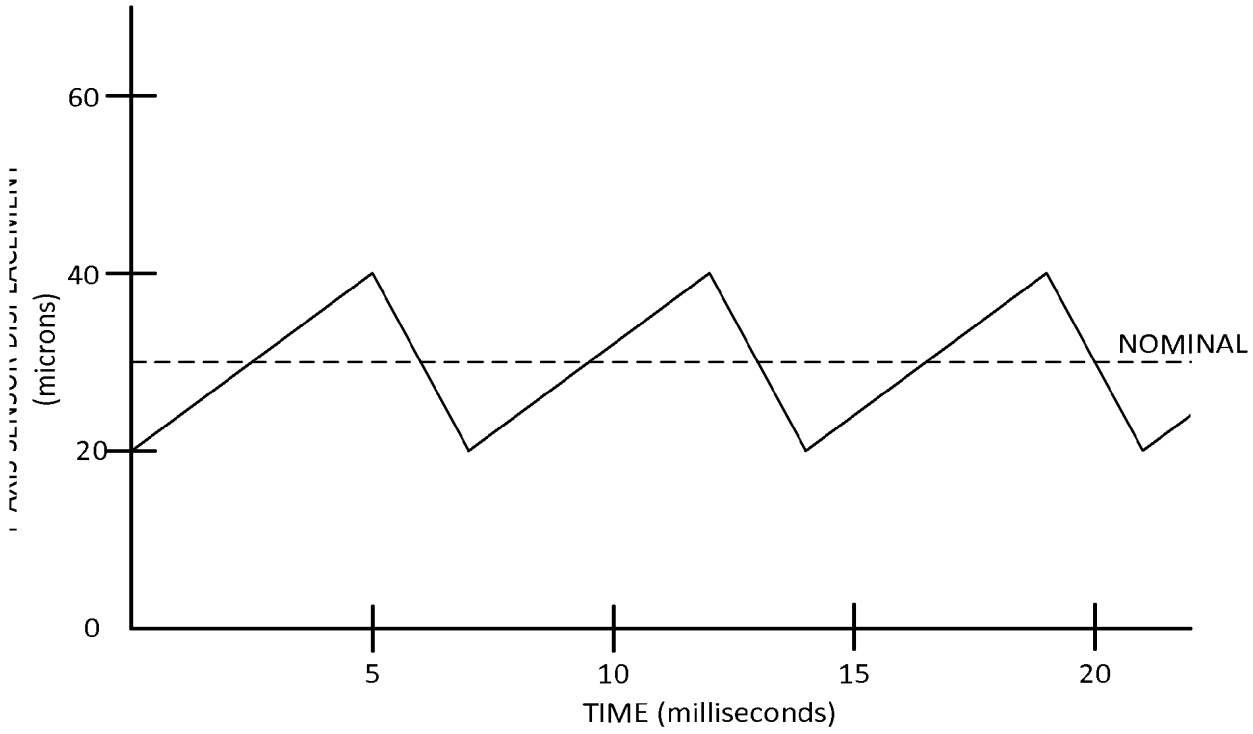

FIG. 15B

Sensor/Camera Evolution

- Era 1: Analog Sensor, 1970 - 1990
  - A/D everything else off-chip
- Era 2: Digital CCD's & CMOS, 1990's early 2000's
  - Digital data, often compressed, exits chip
- Era 3: System on Chip Sensors, mid 2000's – present
  - Getting processing gates onto the sensor, still & video merging
- Era 4: Wafer-Level-Cameras late 2000's – present
  - Personal devices

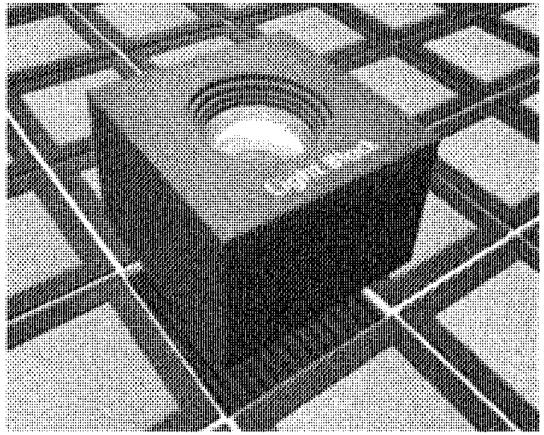

FIG. 16

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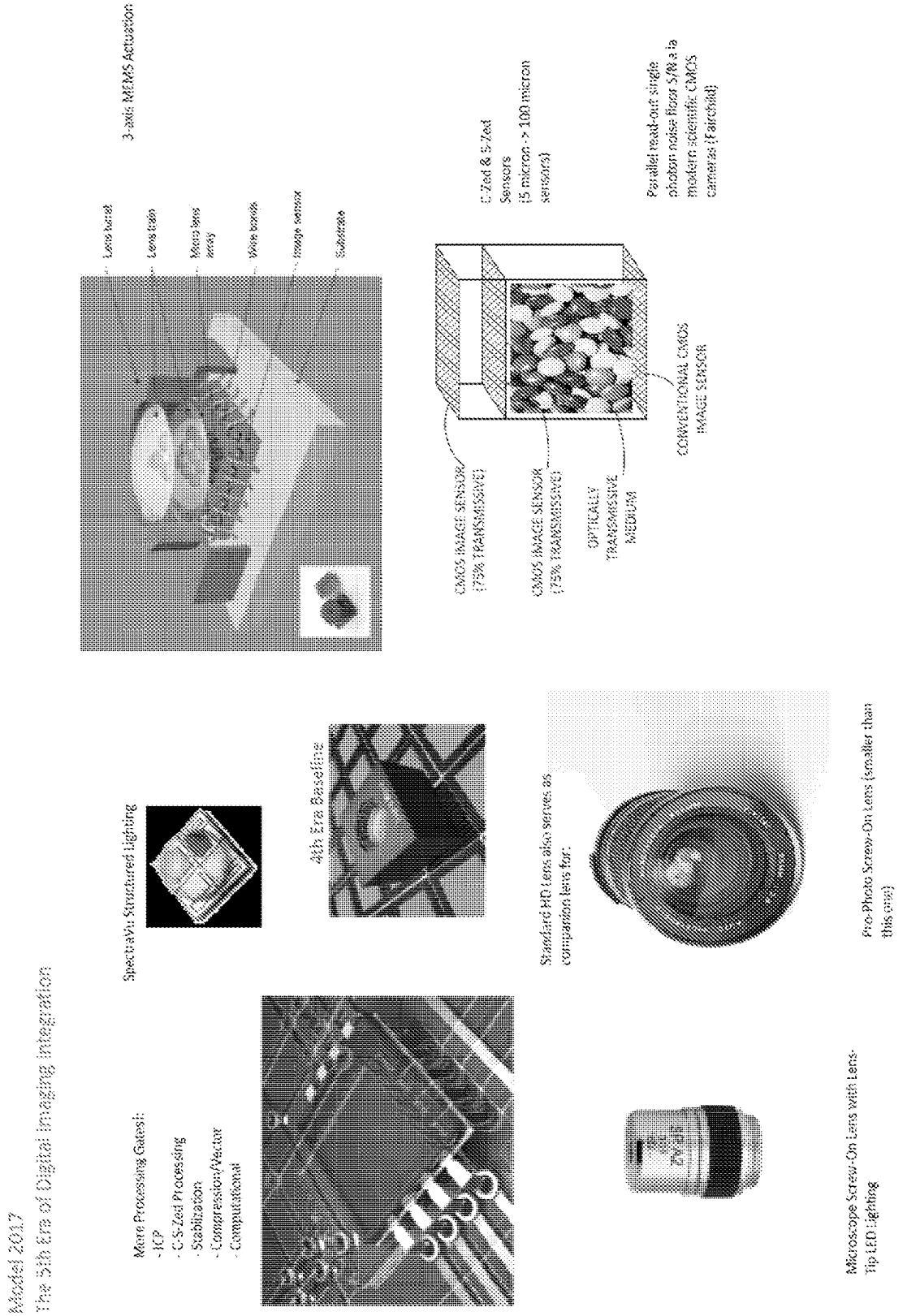

FIG. 17

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Electronic Patent Application Fee Transmittal

Application Number:	15216244
Filing Date:	21-Jul-2016
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Filer:	Reza Mollaaghababa/Jillian Stockel
Attorney Docket Number:	143705.05221

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	29194732
Application Number:	15216244
International Application Number:	
Confirmation Number:	5052
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	136549
Filer:	Reza Mollaaghababa/Jillian Stockel
Filer Authorized By:	Reza Mollaaghababa
Attorney Docket Number:	143705.05221
Receipt Date:	12-MAY-2017
Filing Date:	21-JUL-2016
Time Stamp:	14:03:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$180
RAM confirmation Number	051517INTEFSW14081200
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		5221_Response.pdf	130283 97a53444dda7018754753e6fcbdbfb42b514eb88	yes	7
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	5	
	Applicant Arguments/Remarks Made in an Amendment		6	7	
Warnings:					
Information:					
2	Transmittal Letter	5221_IDSTransmittal.pdf	93416 0d341bca69335fd4745269465a913a1194b1f69d	no	2
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	5221_SB08.pdf	1036648 15f28d1caf3f4de9ed59b96456bbcd05fed81a06	no	7
Warnings:					
Information:					
4	Foreign Reference	DE19838439.pdf	1680083 1bbd6553cd61e869de070de2645cd4308d79229f	no	9
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Information:					
5	Foreign Reference	EP2509107A1.pdf	1361527 7ce82ba536ff3d53d0413875489e5475a614a1d7	no	39

Warnings:					
Information:					
6	Foreign Reference	JP2010278472.pdf	412252 b8d1fc94e5f63cc03f3e7a3c274d82c0b5cb6e4c	no	14
Warnings:					
Information:					
7	Foreign Reference	KR100825808B1.pdf	646102 06d2e3325f454fa224d492eebbe50e6c5da62c9e	no	13
Warnings:					
Information:					
8	Foreign Reference	KR2009077274.pdf	1463669 60ca30c6321a2ce0f15a3d172394ee35f9732bd5	no	20
Warnings:					
Information:					
9	Foreign Reference	WO2009147085.pdf	914681 92df957ec313f823b1604eac4f222d69568e3a0d	no	19
Warnings:					
Information:					
10	Foreign Reference	WO2011003871.pdf	1095011 e6a1904f2a4623e78352c87e598aed2d50cb1df7	no	76
Warnings:					
Information:					
11	Foreign Reference	WO2011035188.pdf	822105 5a30ad842648e5bc3c9e9c6261ff272dce79856a	no	45
Warnings:					
Information:					
12	Foreign Reference	WO2011119618.pdf	2079786 263ea5074666524e598adfd3d2dbac345798edf4	no	43
Warnings:					
Information:					

13	Foreign Reference	WO2012174752A1.pdf	2917593 b5a400d6ee9594d956b1729384d5bc03eddf04cb	no	65
Warnings:					
Information:					
14	Foreign Reference	WO2014110484A2.pdf	1923614 12d98c93286052c4468e9da9b313f3132e547967	no	43
Warnings:					
Information:					
15	Non Patent Literature	CareyPG_1989.pdf	1535156 47a5cb16160430c66c5062052f010c4741441583	no	8
Warnings:					
Information:					
16	Non Patent Literature	Gibbons_1972.pdf	14804775 5e1c22a1c76a9da7b1e0ba78313bc891d2854de6	no	45
Warnings:					
Information:					
17	Non Patent Literature	Ziou_1998.pdf	489927 acd9f526b1469df3b2003edab8cd4aa450a9de36	no	5
Warnings:					
Information:					
18	Fee Worksheet (SB06)	fee-info.pdf	30348 ff32a841cccc2805afab34a3a5ddfbf333dfe892	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	33436976	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
15/216,244	07/21/2016	

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **05/12/2017**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 31	Minus	** 32	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
GAIL WOOTEN

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

SAMSUNG EX. 1002 - 2244/2862

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/216,244	07/21/2016	Martin U. Pralle	143705.05221	5052

136549 7590 06/19/2017

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
06/19/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketingbn@pepperlaw.com
davisdr@pepperlaw.com

SAMSUNG EX. 1002 - 2245/2862

Office Action Summary	Application No. 15/216,244	Applicant(s) PRALLE ET AL.	
	Examiner LONG PHAM	Art Unit 2814	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/12/17*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *34-61,63,64 and 66* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *34-61,63,64 and 66* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *5/12/17*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

In light of the new ground of rejections, the indication of allowability of claims 62 and 65 has been withdrawn.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claim(s) 34-39, 46-49 and 51 and 63-64 and 66 is/are rejected under pre-AIA 35 U.S.C. 102(a) as being anticipated by Haddad et al. WO 2011035188 (a reference cited by the applicant).

With respect to claim 34, Haddad et al. teach a light trapping device, comprising (see figs. 1-17, particularly fig. 3 and associated text):

at least one light sensitive pixel having a light incident surface (top), a backside surface (bottom) opposite the light incident surface, and a peripheral sidewall extending at least partially around the pixel periphery;

a **backside light trapping material** 20 substantially covering the backside surface;

a **peripheral light trapping material** 30 substantially covering the peripheral sidewall; and

at least **one doped region** 14,16 disposed on at least one of the light incident surface and the backside surface,

wherein the peripheral light trapping material inherently creates a surface field at the peripheral sidewall.

With respect to claim 35, Haddad et al. teach the backside light trapping material reflects the light incident thereon back into the pixel.

With respect to claim 36, Haddad et al. teach the peripheral light trapping material reflects light incident thereon into the pixel.

With respect to claim 37, Haddad et al. teach the peripheral sidewall extends completely around the pixel periphery.

With respect to claim 38, Haddad et al. teach the peripheral sidewall extends from the light incident surface to the backside surface.

With respect to claim 39, Haddad et al. teach wherein the peripheral sidewall extends through the pixel substantially from the light incident surface to the backside surface.

With respect to claim 46, Haddad et al. teach said pixel comprises **a textured region** 60, 18, 40.

With respect to claim 47, Haddad et al. teach said textured region is coupled to the light incident surface.

With respect to claim 48, Haddad et al. teach said textured region is located on said light incident surface.

With respect to claim 49, Haddad et al. teach said textured region comprises a textured film layer.

With respect to claim 51, Haddad et al. teach an array of light trapping pixel device.

With respect to claims 63 and 64, how the textured region is formed has not given patentable weight since claimed invention is directed to a device.

With respect to claim 66, Haddad et al. teach said textured region is coupled to said backside surface.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 41, 43, 44, are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Haddad et al. WO 2011035188 as applied to claims

34-39, 46-49 and 51 and 63-64 and 66 above, and further in view of Yanagisawa (JP 403183037) (a reference cited by the applicant).

With respect to claims 41, 43, and 44, Haddad et al. teach the peripheral light trapping material but fails to teach the peripheral light trapping material is made of silicon oxide or having a refractive index of less than about 2.1 or having a surface recombination velocity as low as 10 cm/s.

Yanagisawa teaches using a material of silicon oxide or having a refractive index of less than about 2.1 or having a surface recombination velocity as low as 10 cm/s to control reflectivity. See English abstract.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Yanagisawa into the device of Haddad et al. to achieve the above benefit.

Claims 42 and 45 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Haddad et al. WO 2011035188 as applied to claims 34-34-39, 46-49 and 51 and 63-64 and 66 above, and further in view of Gray et al. (US pat 8906670) (reference previously cited).

With respect to claims 42 and 45, Haddad et al. teach the peripheral light trapping material but fails to teach the peripheral light trapping material is made of aluminum oxide or having passivating negative charge.

Gray et al. teach using a material of aluminum oxide or having passivating negative charge to control reflectivity. See col. 2, lines 1-15.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Gray et al. into the device of Haddad et al. to achieve the above benefit. See col. 2, lines 1-15.

Claims 40 and 50 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Haddad et al. WO 2011035188 as applied to claims 34-39, 46-49 and 51 and 63-64 and 66 above, and further in view of Bour et al. (US pat 8470619) (reference previously cited).

With respect to claims 40 and 50, Haddad et al. fail to teach the trapping or reflecting layer and textured or reflecting layer comprise of a metal layer.

Bour et al. teach using a textured or reflecting layer of metal or Al to enhance or control reflection of incident light. See col. 3, lines 40-50.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Bour et al. into the device of Haddad et al. to achieve light efficiency. See col. 3, lines 40-50.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claim(s) 52-55, 57-61 is/are rejected under pre-AIA 35 U.S.C. 102(a) as being anticipated by Haddad et al. WO 2011035188 (a reference cited by the applicant).

With respect to claim 52, Haddad et al. teach a light trapping device, comprising (see figs. 1-17, particularly fig.1-6 and associated text):

at least one light sensitive pixel having a light incident surface (top), a backside surface (bottom) opposite the light incident surface, and a peripheral sidewall extending at least partially around the pixel periphery;

a **backside light trapping material** 20 at least partially covering the backside surface;

a **peripheral light trapping material** 30 substantially covering the peripheral sidewall; and

at least one doped region 14,16 disposed on at least one of the light incident surface and the backside surface; and

a **textured region** 60 positioned to interact with light incident thereon so as to increase quantum efficiency of the device.

With respect to claim 53, Haddad et al. teach said backside light trapping material substantially covers the backside surface.

With respect to claim 54, Haddad et al. teach said textured region is located on the light incident surface.

With respect to claim 55, Haddad et al. teach said textured region is a textured film layer coupled to the light incident surface.

With respect to claim 57, Haddad et al. teach said textured region reflects at least a portion of light internally incident thereon into the pixel.

With respect to claim 58, Haddad et al. teach the peripheral sidewall extends from the light incident surface to the backside surface.

With respect to claim 59, Haddad et al. teach the peripheral sidewall extends through the pixel substantially from the light incident surface to the backside surface.

With respect to claims 60 and 61, how the textured region is formed has not given patentable weight since claimed invention is directed to a device.

Claim 56 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Haddad et al. WO 2011035188 as applied to claims 52-55 and 57-61 above, and further in view of Bour et al. (US pat 8470619) (reference previously cited).

With respect to claim 56, Haddad et al. fail to teach the trapping or reflecting layer and textured or reflecting layer comprise of a metal layer.

Bour et al. teach using a textured or reflecting layer of metal or Al to enhance or control reflection of incident light. See col. 3, lines 40-50.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Bour et al. into the device of Haddad et al. to achieve light efficiency. See col. 3, lines 40-50.

Response to Arguments

Applicant's arguments with respect to claims 34-61, 63-64, and 66 have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LONG PHAM whose telephone number is (571)272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

/LONG PHAM/
Primary Examiner, Art Unit 2814

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Attorney Docket Number	143705.05221

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4886958		1989-12-12	Merryman	
	2	5351446		1994-10-04	Langsdorf	
	3	5641969		1997-06-24	Cooke et al.	
	4	5727096		1998-03-10	Ghirardi et al.	
	5	6327022		2001-12-04	Nishi	
	6	6331885		2001-12-18	Nishi	
	7	6340281		2002-01-22	Haraguchi	
	8	7800684		2010-09-21	Tatani	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.P./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	Long Pham
	Attorney Docket Number	143705.05221

	9	7897942		2011-03-01	Bereket	
	10	9184204		2015-11-10	Hu	
	11	9369641		2016-06-14	Hu	

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U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20010044266		2001-11-22	Katsuoka	
	2	20050088634		2005-04-28	Kosugi	
	3	20090093100		2005-05-06	Chen	
	4	20080173620		2008-07-24	Grek	
	5	20090027640		2009-01-29	Shibazaki	
	6	20090114630		2009-05-07	Hawryluk	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.P./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Attorney Docket Number	143705.05221

	7	20090308457		2009-12-17	Smith et al.	
	8	20100140768		2010-06-10	Zafiropoulo	
	9	20130135439		2013-05-30	Kakuko et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	19838439	DE		2000-04-27	Fraunhofer-Ges Forschung		
	2	2509107	EP		2012-10-10	Boly Media Comm.		
	3	2010278472	JP		2010-12-09	Sony, Corp.		
	4	100825808	KR		2008-04-29	Samsung Electronics Co. Ltd.		
	5	20090077274	KR		2009-07-15	LG Electronics Inc.		
	6	2009147085	WO		2009-12-10	Thiel et al.		

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.P./

SAMSUNG EX. 1002 - 2258/2862

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	Long Pham
	Attorney Docket Number	143705.05221

	7	2011003871	WO		2011-01-13	International Business Machines Corporation		
	8	2011035188	WO		2011-03-24	Sionyx, Inc.		
	9	2011119618	WO		2011-03-22	Sionyx, Inc.		
	10	2012174752	WO		2012-12-27	Boly Media Comm.		
	11	2014110484	WO		2014-07-17	Digimarc Corp.		

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Carey, P.G. et al., "In-situ Doping of Silicon Using Gas Immersion Laser Doping (GILD) Process," Appl. Surf. Sci. 43, 325-332 (1989).	
	2	Gibbons, J., "Ion Implantation in Semiconductors-Part II; Damage Production and Annealing", proceedings of the IEEE Vol. 60, No. 9 pp. 1062-1096. Jun. 1972.	
	3	Ziou et al., "Depth from defocus using the hermite transform", IMAGE PROCESSING, 1998. ICIP 98. Intl. Conference on Chicago, IL. October 1998 pp. 958 - 962.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Attorney Docket Number	143705.05221

EXAMINER SIGNATURE			
Examiner Signature	/LONG PHAM/	Date Considered	06/10/2017

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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SAMSUNG EX. 1002 - 2260/2862

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Attorney Docket Number	143705.05221

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Reza Mollaaghababa/	Date (YYYY-MM-DD)	2017-05-12
Name/Print	Reza Mollaaghababa	Registration Number	43810

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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SAMSUNG EX. 1002 - 2261/2862

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The information provided by you in this form will be subject to the following routine uses:

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

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SAMSUNG EX. 1002 - 2262/2862

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S2	84	US-3035052-$.DID. OR US-20030029495-$.DID. OR US-20040222187-$.DID. OR US-20050127401-$.DID. OR US-20050227390-$.DID. OR US-20060011955-$.DID. OR US-20060079062-$.DID. OR US-20060118781-$.DID. OR US-20060180885-$.DID. OR US-20060231914-$.DID. OR US-20070145505-$.DID. OR US-20080026550-$.DID. OR US-20080036022-$.DID. OR US-20080044943-$.DID. OR US-20080076240-$.DID. OR US-20080099804-$.DID. OR US-20080178932-$.DID. OR US-20080258604-$.DID. OR US-20090065051-$.DID. OR US-20090142879-$.DID. OR US-20090160983-$.DID. OR US-20090194671-$.DID. OR US-20090200586-$.DID. OR US-20090213883-$.DID. OR US-3487223-$.DID. OR US-4277793-$.DID. OR US-4419533-$.DID. OR US-4493942-$.DID. OR US-4514582-$.DID. OR US-4536608-$.DID. OR US-4663188-$.DID. OR US-4829013-$.DID. OR US-5080725-$.DID. OR US-5081049-$.DID. OR US-5100478-$.DID. OR US-5114876-$.DID. OR US-5164324-$.DID. OR US-5322988-$.DID. OR US-5346850-$.DID. OR US-5597621-$.DID. OR US-5714404-$.DID. OR US-5731213-$.DID. OR US-5792280-$.DID. OR US-6147297-$.DID. OR US-6498336-$.DID. OR US-6580053-$.DID. OR US-6583936-$.DID. OR US-6667528-$.DID. OR US-6759262-$.DID. OR US-6800541-$.DID. OR US-7057256-$.DID. OR US-7091411-$.DID. OR US-7109517-$.DID. OR US-7247527-$.DID. OR US-7314832-$.DID. OR US-7354792-$.DID. OR US-7390689-$.DID. OR US-7442629-$.DID. OR US-7456452-$.DID. OR US-7482532-$.DID. OR US-7498650-$.DID. OR US-7504325-$.DID. OR US-7504702-$.DID. OR US-7511750-$.DID. OR US-7745901-$.DID. OR US-7781856-$.DID. OR US-7816220-$.DID. OR US-7847253-$.DID. OR US-7884439-$.DID. OR US-7884446-$.DID. OR US-8030726-$.DID. OR US-8058615-$.DID. OR US-8207051-$.DID.	US-PGPUB; USPAT; USOCR; JPO; IBM_TDB	OR	ON	2014/06/25 14:14

SAMSUNG EX. 1002 - 2263/2862

		OR US-8476681-$.DID. OR US-3666484-$.DID. OR US-2030766-$.DID. OR JP-07173484-$.DID. OR JP-071734840721-$.DID. OR JP-2008187003-$.DID. OR JP-2011091128-$.DID. OR JP-2152226-$.DID. OR JP-63116421-$.DID. OR JP-9298308-$.DID. OR KR-20010061058-$.DID. OR KR-20100118864-$.DID. OR WO-2006086014-$.DID. OR WO-2009100023-$.DID. OR WO-2011035188-$.DID. OR WO-2011119618-$.DID.				
S3	7768	(light adj2 (trapping or trapped))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 14:16
S4	11	S2 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 14:16
S5	2251	(reflector or Bragg) and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:40
S6	14	(reflector or Bragg) and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:41
S7	888	(reflector or Bragg) near3 backside	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:55
S8	51623	(reflector or Bragg) near3 (side or sidewall or edge or wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:55
S9	112640	pixel near5 (side or sidewall or edge or wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:56

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S10	143	S7 same S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:56
S11	2	S9 same4 S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:56
S12	3	S9 and S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:57
S13	1	S12 not S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:57
S14	179	S7 same4 S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:58
S15	145	S14 and (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:59
S16	129	S14 same10 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:59
S17	128	S14 same8 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:59
S18	1204	(reflector or Bragg) near5 backside	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2014/06/25 16:09

SAMSUNG EX. 1002 - 2265/2862

			DERWENT; IBM_TDB			
S19	71202	(reflector or Bragg) near5 (side or sidewall or edge or wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S20	280	S18 same4 S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S21	195	S20 same4 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S22	7	S18 same2 S9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:10
S23	7	S22 same4 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:10
S24	217	S18 same S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:13
S25	0	(light adj2 sensitive adj2 pixel) same4 S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:14
S26	0	(light adj2 sensitive adj2 pixel) and S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:14
S27	14	pixel same4 S24	US-PGPUB; USPAT; USOCR;	OR	ON	2014/06/25 16:14

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			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S28	7	S27 and index	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:18
S29	26925	(high adj2 index) near3 (layer or film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:48
S30	27823	(low adj2 index) near3 (layer or film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:48
S31	12802	S29 near10 S30	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:48
S32	1170	(reflector or Bragg) same S31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:49
S33	611	(reflector or Bragg) near10 S31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:49
S34	4200	S30 near5 ("between")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:49
S35	1972	S34 near10 S29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:50
S36	81	(reflector or Bragg) near10 S35	US-PGPUB;	OR	ON	2014/06/26

SAMSUNG EX. 1002 - 2267/2862

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			12:50
S37	188	S29 near5 (polysilicon or polycrystalline or poly or (amorphous adj2 silicon) or germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:53
S38	2500	S30 near5 (oxide or nitride or oxynitride or oxynitrides)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:53
S39	14	S37 near20 S38	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:53
S40	0	(reflector or Bragg) same S39	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:54
S41	0	S39 near20 ("between")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:54
S42	51	backside near6 (textured near2 (layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:12
S43	10	S42 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:25

SAMSUNG EX. 1002 - 2268/2862

		H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.)				
S44	5	S39 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:25
S45	2	S36 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:25
S46	1	("20140138785").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:26
S47	3930	(257/432).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:54
S48	218	(257/228).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:54
S50	1	("9373732").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/07/13 15:10
S51	1	("9373732").PN.	US-PGPUB;	OR	OFF	2016/07/15

SAMSUNG EX. 1002 - 2269/2862

			USPAT; USOCR			10:13
S52	395	reflective near3 (aluminum adj oxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/15 13:07
S53	35214	(rough or textured) near2 (layer or film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:24
S54	44833	light adj2 incident adj2 surface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:24
S55	38	S53 same S54	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:25
S56	10	S55 same efficiency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:25
S57	0	S55 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:29
S58	0	S55 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:30
S59	3	S55 same (metal or polysilicon or amorphous)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:30
S60	1864	S53 same efficiency	US-PGPUB; USPAT; USOCR;	OR	ON	2017/02/06 01:32

SAMSUNG EX. 1002 - 2270/2862

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S61	42	S60 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:32
S62	351	S60 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN" or metal or polysilicon or amorphous)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:32
S63	85	S62 same4 incident	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:33
S64	228102	(reflective near2 (material or layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:11
S65	530599	("AlO" or (aluminum adj oxide)) or ("HfO" or (hafnium adj oxide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:12
S66	403	S64 near3 S65	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:12
S67	2	S66 near4 (benefit or beneficial or advantages or advantageous or advantegeously)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:13
S68	2	S66 near10 (benefit or beneficial or advantages or advantageous or advantegeously)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:13
S69	31128	(anti or non) near2 S64	US-PGPUB;	OR	ON	2017/02/06

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			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:20
S70	121	S65 near4 S69	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:20
S71	2	S70 same (benefit or beneficial or advantages or advantageous or advantegeously)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:20
S72	2	(dope or doping or implanting or implant or implants implantation or dopes) near2 (light adj incident adj surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:04
S73	6	(dope or doping or implanting or implant or implants implantation or dopes) near2 (light adj2 incident adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:05
S74	13	(dope or doping or implanting or implant or implants implantation or dopes) near4 (light adj2 incident adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:05
S75	167141	(doped or implanted) adj2 (region or section or portion or part)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:13
S76	1	S75 near4 (light adj2 incident adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:13
S77	26	S75 near10 (light adj2 incident adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2017/02/06 12:15

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			IBM_TDB			
S78	25	S77 not S76	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:15
S79	1	("9064764").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/02/06 12:20
S80	44833	(light adj2 incident adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 17:49
S81	167141	(doped or implanted) adj2 (region or section or portion or part)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 17:49
S82	9	S80 near6 S81	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 17:49
S83	364064	(light adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 17:50
S84	54	S83 near4 S81	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 17:50
S85	53	S84 not S82	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 17:50
S86	21	("20030214595" | "20030228883" | "20050093100" | "20060086956" | "20060128087" | "20070189583" | "20070237504" | "20080158398" | "20080192133" | "20080284884" | "20100200658" | "20110194100" | "20110292380" | "20140198240" | "5101260" | "5600130" | "5626687" |	US-PGPUB; USPAT	OR	ON	2017/02/07 07:43

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		"5635089" | "6082858" | "6204506" | "6907135").PN.				
S87	21	("20030214595" | "20030228883" | "20050093100" | "20060086956" | "20060128087" | "20070189583" | "20070237504" | "20080158398" | "20080192133" | "20080284884" | "20100200658" | "20110194100" | "20110292380" | "20140198240" | "5101260" | "5600130" | "5626687" | "5635089" | "6082858" | "6204506" | "6907135").PN.	US-PGPUB; USPAT	OR	ON	2017/02/07 07:44
S88	20	("20010044266" | "20050088634" | "20080173620" | "20090027640" | "20090093100" | "20090114630" | "20090308457" | "20100140768" | "20130135439" | "4886958" | "5351446" | "5641969" | "5727096" | "6327022" | "6331885" | "6340281" | "7800684" | "7897942" | "9184204" | "9369641").PN.	US-PGPUB; USPAT	OR	ON	2017/06/01 13:32

6/ 10/ 2017 5:12:02 PM
C:\ Users\ lpham\ Documents\ EAST\ Workspaces\ 15-216,244.wsp

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15216244	PRALLE ET AL.
	Examiner	**Art Unit**
	LONG PHAM	2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/07/2016	02/06/2017	06/10/2017						
	34	÷	✓	✓						
	35	÷	✓	✓						
	36	÷	✓	✓						
	37	÷	✓	✓						
	38	÷	✓	✓						
	39	÷	✓	✓						
	40	÷	✓	✓						
	41	÷	✓	✓						
	42	÷	✓	✓						
	43	÷	✓	✓						
	44	÷	✓	✓						
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	46	÷	✓	✓						
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	48	÷	✓	✓						
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	59	÷	✓	✓						
	60		✓	✓						
	61		✓	✓						
	62		O	-						
	63		✓	✓						
	64		✓	✓						
	65		O	-						
	66			✓						

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PTO/AIA/80 (07-12)
Approved for use through 11/30/2014. OMB 0651-0035
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I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

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OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☑ The address associated with Customer Number: 136549

OR

☐	Firm or Individual Name			
	Address			
	City		State	Zip
	Country			
	Telephone		Email	

Assignee Name and Address: SiOnyx, LLC
100 Cummings Center, Suit 243F
Beverly, MA 01915

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	12/18/15
Name	Stephen Saylor	Telephone	508.521.4305
Title	CEO, SiOnyx LLC		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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Electronic Acknowledgement Receipt

EFS ID:	29590814
Application Number:	15216244
International Application Number:	
Confirmation Number:	5052
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	136549
Filer:	Reza Mollaaghababa/Jillian Stockel
Filer Authorized By:	Reza Mollaaghababa
Attorney Docket Number:	143705.05221
Receipt Date:	23-JUN-2017
Filing Date:	21-JUL-2016
Time Stamp:	13:26:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	SIOnyx_POA.pdf	135241 3e9144ffe18fe0c3a5f4a21cbd2f422b21d9b7ac	no	2

Warnings:

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Information:	
Total Files Size (in bytes):	135241

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

Courtesy Reminder for
Application Serial No: 15/216,244

Attorney Docket No: 143705.05221
Customer Number: 136549
Date of Electronic Notification: 06/19/2017

This is a courtesy reminder that new correspondence is available for this application. If you have not done so already, please review the correspondence. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:
docketingbn@pepperlaw.com
davisdr@pepperlaw.com

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/216,244	07/21/2016	Martin U. Pralle	143705.05221

CONFIRMATION NO. 5052

POA ACCEPTANCE LETTER

136549
Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

OC000000092381365

Date Mailed: 06/28/2017

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 06/23/2017.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/sphouminh/

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Martin U. Pralle Application No.: 15/216,244 Filed: July 21, 2016 For: PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS	Confirmation No.: 5052 Art Unit: 2814 Examiner: Pham, Long

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Certificate of Mailing

I hereby certify that this correspondence is being electronically filed via EFS-Web to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

November 13, 2017 (Dated) — Electronic Signature: /Reza Mollaaghababa/ (Reza Mollaaghababa, Reg. No. 43,810)

RESPONSE TO NON-FINAL OFFICE ACTION

Dear Sir:

This paper is filed in response to the non-final Office Action dated June 19, 2017.

Amendments to the Claims begin on page 2.

Remarks begin on page 7.

AMENDMENTS TO THE CLAIMS

1-33. (Canceled)

34. (Currently Amended) An imager ~~A light trapping~~ device, comprising:

at least ~~one~~ two adjacent light sensitive ~~pixel~~ pixels each having a light incident surface, and a backside surface opposite the light incident surface~~, and a peripheral sidewall extending at least partially around the pixel periphery~~;

~~a backside light trapping material substantially covering the backside surface;~~

~~a peripheral light trapping material~~ a peripheral isolation element at least partially separating said two adjacent light sensitive pixels ~~substantially covering the peripheral sidewall~~;

each of said pixels having at least one doped region disposed on at least one of the light incident surface and the backside surface,

wherein the peripheral isolation element comprises at least two materials having different indices of refraction ~~light trapping material creates a surface field at the peripheral sidewall~~.

35. (Currently Amended) The device of claim 34, wherein said peripheral isolation element comprises a first, a second and a third layer, wherein said third layer is disposed between said first and second layers, and wherein each of said first and second layer exhibits an index of refraction less than an index of refraction of said third layer ~~the backside light trapping material reflects the light incident thereon back into the pixel~~.

36. (Currently Amended) The device of claim 34, wherein the index of refraction of at least one of said first and second layer is at least 0.2 lower relative the refractive index of the third layer ~~peripheral light trapping material reflects light incident thereon into the pixel~~.

37. (Currently Amended) The device of claim 34, wherein at least of one of said at least two materials comprises silicon dioxide ~~the peripheral sidewall extends completely around the pixel periphery~~.

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38. (Currently Amended) The device of claim 35 ~~34~~, wherein at least one of said first and second layers comprises silicon dioxide ~~the peripheral sidewall extends from the light incident surface to the backside surface~~.

39. (Currently Amended) The device of claim 34, wherein the ~~peripheral sidewall~~ isolation element extends ~~through the pixel~~ substantially from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels.

40. (Currently Amended) The device of claim 35 ~~34~~, wherein at least one of the first and second layer comprises Al_2O_3 ~~backside light trapping material and the peripheral light trapping material comprises a metal layer~~.

41. (Currently Amended) The device of claim 34, wherein said ~~peripheral light trapping material~~ peripheral isolation element comprises an oxide.

42. (Currently Amended) The device of claim 34, wherein said ~~peripheral light trapping material~~ isolation element provides a passivating negative charge.

43. (Currently Amended) The device of claim 34, wherein said ~~peripheral light trapping material~~ isolation element exhibits a surface recombination velocity as low as 10 cm/s.

44. (Currently Amended) The device of claim 34, wherein the ~~peripheral sidewall material~~ isolation element comprises at least one material having ~~has~~ an index of refraction of less than about 2.1.

45. (Currently Amended) The device of claim 34, wherein the ~~peripheral light trapping material~~ isolation element comprises any of aluminum oxide and hafnium oxide.

46. (Currently Amended) The device of claim 34, wherein at least one of said two adjacent light sensitive ~~pixel~~ pixels comprises a textured region.

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47. (Previously Presented) The device of claim 46, wherein said textured region is coupled to the light incident surface.

48. (Currently Amended) The device of claim 47, wherein said light incident surface comprises said textured region ~~is located on said light incident surface~~.

49. (Previously Presented) The device of claim 47, wherein said textured region comprises a textured film layer.

50. (Previously Presented) The device of claim 49, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.

51. (Currently Amended) The device of claim 46, wherein said backside surface comprises said textured region ~~An array of light trapping pixel devices of claim 34~~.

52. (Currently Amended) An imager ~~A light trapping~~ device, comprising:

at least two adjacent ~~one~~ light sensitive ~~pixel~~ pixels each having a light incident surface, and a backside surface opposite the light incident surface~~, and a peripheral sidewall extending at least partially around the pixel periphery~~;

~~a backside light trapping material at least partially covering the backside surface;~~

a peripheral isolation element separating said at least two adjacent light sensitive pixels so as to reduce optical crosstalk therebetween, said isolation element comprising at least two materials having different indices of refraction ~~a peripheral light trapping material substantially covering the peripheral sidewall~~; ~~and~~

at least one doped region disposed on at least one of the light incident surface and the backside surface~~; and~~

~~a textured region positioned to interact with light incident thereon so as to increase quantum efficiency of the device~~.

53. (Currently Amended) The device of claim 52, wherein said peripheral isolation element comprises a first, a second and a third layer, wherein said third layer is disposed between said

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first and second layers, and wherein each of said first and second layers exhibits an index of refraction less than an index of refraction of said third layer ~~said backside light trapping material substantially covers the backside surface~~.

54. (Currently Amended) The device of claim 52, wherein at least one of said light incident surface and said backside surface of at least one of said two adjacent light sensitive pixels comprises a textured region ~~is located on the light incident surface~~.

55. (Currently Amended) The device of claim 54 ~~52~~, wherein said textured region is a textured film layer ~~coupled to the light incident surface~~.

56. (Previously Presented) The device of claim 55, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.

57. (Currently Amended) The device of claim 54 ~~52~~, wherein said textured region reflects at least a portion of light internally incident thereon into the pixel.

58. (Currently Amended) The device of claim 52, wherein the isolation element ~~peripheral sidewall~~ extends from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels.

59. (Currently Amended) The device of claim 52 ~~34~~, wherein said at least two materials comprises silicon dioxide and aluminum oxide ~~the peripheral sidewall extends through the pixel substantially from the light incident surface to the backside surface~~.

60. (Currently Amended) The device of claim 54 ~~52~~, wherein said at least two pixels are formed monolithically in a common semiconductor substrate ~~the textured region is formed by one of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof~~.

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61. (Currently Amended) The device of claim 54 ~~52~~, wherein the textured region is formed by laser radiation.

62. (Canceled)

63. (Previously Presented) The device of claim 46, wherein the textured region is formed by one of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.

64. (Previously Presented) The device of claim 46, wherein the textured region is formed by laser radiation.

65. (Canceled)

66. (Canceled)

67. (New) The device of claim 46, wherein said textured region is coupled to the backside surface.

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REMARKS

Applicant amends claims 34-46, 48, 51-55, and 57-61, cancel claim 66 without prejudice, and add new claim 67 as indicated above. Support for the amendments can be found, e.g., at paragraphs [0039], [0043], [0044], [0045], [0047], and [0052], as well as FIG. 2 of Applicant's published U.S. application. No new matter is added.

Rejections Pursuant to 35 U.S.C. §102

1. *Claims 34-39, 46-49, 51, 63, and 64 are rejected as being anticipated by PCT Pub. No. WO 2011035188 ("Haddad")*

Claim 34, as amended, recites an imager device, which comprises at least two adjacent light sensitive pixels each having a light incident surface, a backside surface opposite the light incident surface, and a peripheral isolation element at least partially separating said two adjacent light sensitive pixels. Each of the pixels has at least one doped region disposed on at least one of the light incident surface and the backside surface, wherein the peripheral isolation element comprises at least two materials having different indices of refraction.

Haddad is generally directed to a photosensitive imager device that can include a semiconductor substrate having multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the junction. Abstract.

Haddad does not, however, disclose an isolation element disposed between two adjacent light sensitive pixels, where the isolation element comprises at least two materials having different indices of refraction, as recited in amended claim 1. In particular, Haddad does not disclose that its peripheral light trapping material (e.g., element 30 depicted in FIG. 30) includes at least two materials having different indices of refraction.

Thus, Haddad does not anticipate independent claim 34. Further, claims 35-39, 46, 51, 63, and 64 depend on claim 34 and hence are patentable over Haddad at least for the reasons provided in connection with claim 34.

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II. Claims 52-55 and 57-61 are rejected as being anticipated by Haddad

Independent claim 52 recites an imager device, which comprises at least two adjacent light sensitive pixels each having a light incident surface, and a backside surface opposite the light incident surface. The imager device further includes a peripheral isolation element separating said at least two adjacent light sensitive pixels so as to reduce optical crosstalk therebetween, said isolation element comprising at least two materials having different indices of refraction. The imager device further includes at least one doped region disposed on at least one of the light incident surface and the backside surface.

The reasoning provided above in connection with claim 34 applies equally to establish that independent claim 52 is also patentable over the cited art. In particular, Haddad does not disclose an isolation element comprising at least two materials having different indices of refraction.

Further, claims 53-55 and 57-61 depend directly or indirectly on claim 52 and hence are also patentable over the cited art at least for the reasons provided above in connection with claim 52.

Rejections Pursuant to 35 U.S.C. §103

I. Claims 41, 43, and 44 are rejected as being unpatentable over Haddad and further in view of JP H03183037 (Yanagisawa)[1]

Yanagisawa is directed to an optical storage medium. Page 1. Yanagisawa discloses that conventionally aluminum or gold is used as the material of the reflective film. *Id.* Yanagisawa explains that such conventional reflective films can experience corrosion when exposed to high temperature and high humidity. *Id.* Yanagisawa indicates that it is an object of its purported invention to provide an optical storage medium that is weather resistant, and particularly to an optical storage medium that has excellent corrosion resistance and adhesiveness. *Id.*

[1] Applicant notes that the Office Action identifies this reference as JP 403183037. Applicant notes that the publication number is JP H03183037, as indicated on the IDS filed on February 13, 2017 (reference B14). Additionally, Applicant notes that it has relied on a machine translation of this reference provided by EPO's Espace (and which is appended hereto as Exhibit 1) for understanding Yanagisawa's disclosure and refers to this machine translation in the following discussion.

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Specifically, Yanagisawa discloses forming combined layers of high-refractive index layers of adequate film thicknesses on a transparent substrate, thereby obtaining high reflectivity. Abstract. For example, Yanagisawa discloses a combination of high-refractive index layers consisting of silicon, germanium and low-refractive index layers consisting of silicon oxide, magnesium fluoride on a transparent substrate. *Id.*

As an initial matter, Yanagisawa is non-analogous art relative to the claimed invention. In particular, Yanagisawa is not in the field of the claimed invention. Nor is Yanagisawa reasonably pertinent to the problems faced by the present inventor. As such, it is non-analogous art relative to the claimed invention. *See In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004) (holding that two separate tests define the scope of analogous art: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of inventor's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the inventor is involved).

While the claimed invention is directed to an imager device, Yanagisawa is directed to an optical storage medium. Further, the teachings of Yanagisawa regarding an optical storage medium are not pertinent to the problem faced by the present inventors. In particular, the present inventors explain that imagers can be incorporated into a variety of devices, including digital cameras, camcorders, computer, cell phones, etc. *See*, published application at para. [0002]. The present inventors further explain that "[d]ue to the ever decreasing size (foot print) of these devices, image sensors have correspondingly seen a decrease in size." *Id.* However, "pixel size reduction can lead to a significant sacrifice in image quality." *Id.* In particular, "[a]s pixel sizes continue to decrease, image signal to noise tends to decrease while electrical and optical cross-talk between adjacent sensor pixels tends to increase." *Id.* The teachings of Yanagisawa regarding an optical storage medium is not pertinent to solving the problem of cross-talk between pixels in an imager device.

Moreover, even if one were to combine Haddad with Yanagisawa one still would not arrive at the subject matter of claims 41, 43, and 44. Each of these claims depends on claim 34 and hence incorporates the limitations of claim 34. As discussed above, Haddad does not disclose a peripheral isolation element that comprises at least two materials with different indices

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of refraction. And Yanagisawa does not cure this gap in the teachings of Haddad. In particular, Yanagisawa does not disclose, or even suggest, using its reflective layers as an isolation element in an imager device.

Thus, claims 41, 43 and 44 are patentable over the cited art.

II. Claims 42 and 45 are rejected as being unpatentable over Haddad further in view of U.S. Patent No. 8,906,670 ("Gray")

Claims 42 and 45 depend on claim 34 and hence incorporate the features of claim 34. As discussed above, Haddad does not disclose the subject matter of claim 34. Gray does not cure the gap in the teachings of Haddad with regard to the subject matter of claim 34. Rather, Gray is simply directed to optical confinement structures such as zero-mode waveguides. (7:11-13).

New Claims

New claim 67 depends, via intervening claim 46, on claim 34 and further recites that the textured region recited in claim 46 is coupled to the backside surface. This claim is patentable over the cited art at least for the reasons provided above in connection with claim 34.

Conclusion

In view of the above amendments and remarks, Applicant respectfully requests reconsideration and allowance of the application. Applicant invites the Examiner to call the undersigned if there are any outstanding issues.

The Director is authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 50-0436, under Docket No. 143705.05601.

Dated: November 13, 2017

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Exhibit 1

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DESCRIPTION JPH03183037

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to an optical storage used for audio equipment or information equipment. Conventionally, a compact disc (hereinafter abbreviated as CD), which is one of optical storage bodies,), Aluminum or gold is used as the material of the reflective film. However, in recent years, CD-ROMs on which computer data are recorded on CDs have become widespread, and more highly-preserved at high temperature and high humidity is desired more than ever before. Problems to be Solved by the Invention In the conventional optical memory using a gold or aluminum reflective film, under such harsh environments, corrosion occurs when the deposited reflective film is aluminum, and in the case of gold, There is a problem that it is peeled from the body and the error rate used as an indicator of signal reading increases and it can not be adapted to the above-mentioned needs. Also, the reflective film materials other than the aluminum yarn were in a state of being unusable due to insufficient reflectance. SUMMARY OF THE INVENTION The present invention has been made to solve the conventional problems as described above, and it is an object of the present invention to provide an optical storage medium having a weather resistance, particularly excellent corrosion resistance and adhesiveness, . Means for Solving the Problems The present invention is a method for manufacturing a magnetic recording medium including a transparent substrate and a combination layer or a low refractive index layer which is formed in order of a high refractive index layer and a low refractive index layer, And a high refractive index layer in that order on a recording bit forming surface of the transparent substrate; and a high refractive index layer coated on the recording bit forming surface of the transparent substrate, Layer and a

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low refractive index layer in this order, and a reflective layer which is coated on the combination layer. The high refractive index layer used in this presentation is mainly silicon, germanium, boron, zinc sulfide,! ! Titanium dioxide, magnesium oxide, indium oxide, antimony oxide, antimony sulfide, tellurium, cadmium telluride, lead telluride and the like can be used. Further, the low refractive index layer used in the present invention is silicon oxide. Magnesium fluoride, aluminum oxide, cerium bromide, magnesium oxide, calcium bromide. Sodium bromide, lithium bromide, carbon (amorphous or diamond), and the like can be used. The reflective layer used in the present invention may be a reflective layer made of chromium, molybdenum, tungsten, vanadium, niobium, tantalum, titanium, zirconium, hafnium, manganese, rhenium, ruthenium, iron, osmium, cobalt, rhodium, iridium, nickel, palladium, platinum, Metals such as cadmium, tin, lead, thallium, antimony, bismuth, indium, gallium and the like or alloys thereof or metal nitrides such as titanium nitride, zirconium nitride, hafnium nitride and the like can be used.

Also anti - gold or silver alone!) Since it is not desirable in terms of adhesion and copper and aluminum in view of corrosiveness in terms of adhesion, it is preferable to use it as an alloy with a metal used as the reflective layer It is desirable to use it. The transparent substrate used in the present invention is an acrylic resin. Polycarbonate resin, polyolefin resin, epoxy resin, fluororesin, glass, sol-gel glass and the like can be used. In the optical memory of the present invention, a high refractive index layer and a low refractive index layer are alternately formed on a transparent substrate on which recording bits are formed by injection molding or tight adhesion transfer from a stamper by sputtering, ion blending, cluster An ion beam method, a plasma CVD method, an evaporation method, or the like, and then, if necessary, a reflective film is formed on the combination layer in the same manner as described above. For the transparent substrate, for example, a silicic acid polymer is spin-coated on a glass substrate, a stamper is brought into close contact with the spin coating, and bits are transferred to form a transparent substrate with bits. Also, resin may be injected into the mold of the stamper and removed from the mold to form a transparent substrate with bits. The optical memory of the present invention produced in this way has both high reflectance and high weather resistance (high adhesion and high corrosion resistance), and is far superior to the conventional gold or aluminum reflection film coated directly on a transparent substrate It has reliability concerning long-term data preservation. In the optical memory of the present invention, a combination layer comprising a high refractive index layer and a low refractive index layer is formed on a transparent substrate. By this combination layer, reflected light from each layer causes multiple interference. At this time, when the film thickness of each layer is selected to an appropriate value, the phases coincide and the reflectance can be increased to nearly 100%. Therefore, it is unnecessary to directly form a reflection film made of A ° C, ALJ, or the like directly on the transparent substrate as in the related art, and an optical memory with high reliability is provided. Even with only the combined layer of the high refractive index layer and the low refractive index layer, the reflectance can be made close to 100%, but a combination of multiple layers is required. Therefore, if a reflective layer is provided on the combination layer of the low refractive index

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layer and the high refractive index layer, high reflectance can be obtained with a small number of combination layers. In addition, as the difference in refractive index between the high refractive index layer and the low refractive index layer is large, the film thickness of the two layers can be reduced, and the shape (depth, width, length) of the bit is unlikely to be impaired. DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS Embodiments of the present invention will be described in detail below with reference to the drawings. 1 (a) is a partial cross-sectional view thereof, and FIG. 1 (b) is an enlarged cross-sectional view of a portion A in (a) of FIG. 1, showing an embodiment of the optical memory of the present invention. is there.

Here, two samples coated with the material, the structure, or the film thickness of the transparent substrate 1, the high refractive index layer 2, and the low refractive index layer 3 are not shown in Table 1 and 2, respectively, were prepared. 2 (a) is a partial cross-sectional view thereof, FIG. 2 (b) is an enlarged view of a part B in (a) of FIG. 2, FIG. 2 shows another embodiment of the optical storage 1 of the present invention, FIG. Here, the transparent substrate 1, the low refractive index layer 3, and the high refractive index layer 2 are the materials shown in (1) and (IV) of Table 1, respectively. Two samples coated with 4 M and film thickness were made. FIG. 3 is a partial cross-sectional view showing another embodiment of the optical memory 1 of the present invention. The three samples coated with the material, the structure and the film thickness shown in V, VI, VN of Table 1 by the transparent substrate 1, the high refractive index layer 2, the low refractive index layer 3 and the reflection layer 4 Was prepared. Table 1 also shows the foul rate of each sample obtained. (Hereinafter referred to as "margins") Next, a weather resistance test at a temperature of 70 ° C. and a relative humidity of 95% was conducted for 6 months on a comparative sample in which aluminum and gold were formed as reflective films on a transparent substrate made of these samples and a polycarbonate resin , And the number of errors as an indicator of the quality of the signal was measured. After six months of weathering test, the number of errors of the sample of the present invention was not deteriorated at all, but the comparative sample using the aluminum reflective film was corroded and the comparative sample using the gold reflective film was erroneous Deteriorated as the measurement became impossible. As described in detail above, the optical memory of the present invention has excellent adhesion to a transparent substrate, has corrosion resistance and high reflectance, uses a reflective film of aluminum yarn The reliability can be improved much more than the optical memory body which has been subjected to the light irradiation.

[0002]

Brief Description of the Drawings

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[0003]

FIGS. 1 to 3 are partial cross-sectional views of one embodiment of the optical storage of the present invention, respectively. 1 transparent substrate 2 high refractive index layer 3 low refractive index layer 4 reflective layer

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Martin U. Pralle Application No.: 15/216,244 Filed: July 21, 2016 For: PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS	Confirmation No.: 5052 Art Unit: 2814 Examiner: Pham, Long

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November 13, 2017 (Dated) — Electronic Signature: /Reza Mollaaghababa/ (Reza Mollaaghababa, Reg. No. 43,810)

INFORMATION DISCLOSURE STATEMENT (IDS) TRANSMITTAL LETTER

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed more than three months after the U.S. filing date, OR more than three months after the date of entry of the national stage of a PCT application, AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Office Action or Notice of Allowance (37 CFR 1.97(c)). This IDS is accompanied with the fee set forth in 37 C.F.R. 1.17(p).

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It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 50-0436, under Order No. 143705.05221.

Respectfully submitted,

Dated: November 13, 2017

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
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(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Attorney Docket Number	143705.05221

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	1	5236863		1993-08-17	Iranmesh	
	2	5410168		1995-04-25	Hisa	
	3	8076746		2011-12-13	McCarten et al.	
	4	9419159		2016-08-16	Sakamoto et al.	
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	1	20040256561		2004-12-23	Beuhler et al.	

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	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	Long Pham
	Attorney Docket Number	143705.05221

	2	20070063219		2007-03-22	Sa'ar et al.	
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	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	Long Pham
	Attorney Docket Number	143705.05221

	13	20120274744		2012-11-01	Wan	
	14	20140352779		2014-14-04	Smirnov et al.	
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	1	Campbell, Stephen A., "The Science and Engineering of Microeletronic Fabrication, 2nd Ed.", Oxford University Press, 2001, pp. 406-411.	
	2	Ohring, Milton." The Materials of Science of Thin Films"; pp.176-179; Academic Press, 1992.	

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	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	Long Pham
	Attorney Docket Number	143705.05221

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SAMSUNG EX. 1002 - 2303/2862

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Attorney Docket Number	143705.05221

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Reza Mollaaghababa/	Date (YYYY-MM-DD)	2017-11-13
Name/Print	Reza Mollaaghababa	Registration Number	43810

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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