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Growth of Ⅲ-nitride light-emitting devices on textured substrates

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Abstract of TW200627675 (A)

A III-nitride light emitting device is grown on a textured substrate, in order to reduce the amount of total internal reflection at the interface between the substrate and the III-nitride layers. In some embodiments, the device includes a first growth region substantially free of voids, and a second growth region that improves the material quality such that high quality layers can be grown over the first and second regions.

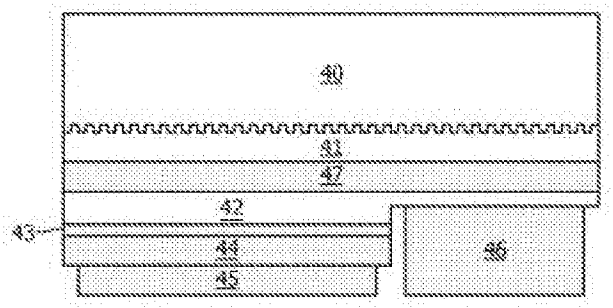


FIG. 1

發明專利說明書

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一、發明名稱：（中文/英文）

紋理基底上III族氮化物發光裝置之成長

GROWTH OF III-NITRIDE LIGHT-EMITTING DEVICES ON TEXTURED SUBSTRATES

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1. 美國 U.S.A.

2. 美國 U.S.A.

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四、聲明事項：

☐ 主張專利法第二十二條第二項☐第一款或☐第二款規定之事實，其事實發生日期為：　年　月　日。

☑ 申請前已向下列國家（地區）申請專利：

【格式請依：受理國家（地區）、申請日、申請案號　順序註記】

☑ 有主張專利法第二十七條第一項國際優先權：

1. 美國；2004年09月23日；10/950,000

2.

☐ 無主張專利法第二十七條第一項國際優先權：

1.

2.

☐ 主張專利法第二十九條第一項國內優先權：

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☐ 主張專利法第三十條生物材料：

☐ 須寄存生物材料者：

國內生物材料　【格式請依：寄存機構、日期、號碼　順序註記】

國外生物材料　【格式請依：寄存國家、機構、日期、號碼　順序註記】

☐ 不須寄存生物材料者：

所屬技術領域中具有通常知識者易於獲得時，不須寄存。

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九、發明說明：

【發明所屬之技術領域】

本發明係關於III族氮化物發光裝置之成長。

【先前技術】

半導體發光二級體(LED)係目前可獲得之最有效光源之一。目前所關注的用於製造能跨越可見光譜操作之高亮度LED的材料系統包括：III-V族化合物半導體，特定言之為鎵、鋁、銦及氮之二元、三元及四元合金，亦稱為III族氮化物材料。該等裝置通常具有一夾於p-摻雜區域與n-摻雜區域之間的發光或活性區域。該活性區域可為一單一發光層或藉由障壁層隔開之多個量子井層。III族氮化物裝置通常係藉由金屬有機化學汽相沈積(MOCVD)、分子束磊晶法(MBE)或其他磊晶技術而於藍寶石、碳化矽或III族氮化物基底上磊晶成長。成長於一傳導性基底上之裝置通常具有形成於基底相對側面上的觸點。或者，該裝置在成長於傳導性較差之基底上時，可經蝕刻以曝露基底同側之n-類型部分及p-類型區域部分兩者，或出於光學或電學原因而如此。然後，該等觸點係形成於曝露區域上。若該等觸點係反射性且光自該裝置之相對於觸點的一側經提取，該裝置稱為覆晶。由於藍寶石的高溫穩定性且相對容易生產，因而III族氮化物LED結構通常成長於藍寶石基底上。

由於半導體層與基底之間的界面上之折射率存在很大差異，因而藍寶石基底之使用可導致提取效率不良。當光入射至兩種材料之界面上時，折射率之差異決定於該界面上

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多少光經反射，且多少光透射穿過該界面。折射率差異愈大，反射的光愈多。藍寶石之折射率(1.8)係低於藍寶石上所成長之III族氮化物裝置層(2.4)之折射率。因此，當III族氮化物裝置層上所產生之光到達半導體層與藍寶石基底之間的界面上時，該光之大部分係經反射。反射光在經提取前係經波導且形成大量穿過該裝置的通道(pass)。歸因於III族氮化物裝置層的任一層內觸點處的光學損失、自由載體吸收及帶間吸收，該等大量通道致使光顯著衰減。

【發明內容】

根據本發明之實施例，一III族氮化物發光裝置係成長於一紋理基底上，以降低該基底與該III族氮化物層之間的界面處的全內反射量。在某些實施例中，該裝置包括一大體上無空隙之第一成長區域，及一第二成長區域；該第二成長區域係用於改良材料品質，使得高品質層可成長於該第一及第二區域之上方。

【實施方式】

藍寶石或其他合適基底與III族氮化物裝置層之間的界面處之全內反射可藉由紋理化或圖案化該基底而降低。如本文所用，"紋理化"意指基底表面歸因於表面任意粗糙化或歸因於表面上形成具重複特徵部分之圖案而不平滑。為節省語言，下述許多實例意指圖案化之基底表面。應理解，相同的原則可應用於具有任意粗糙化之基底表面的裝置。一圖案化基底一般具有隨圖案變化而變化之厚度。如本文所用，一圖案化基底上之"特徵部分(feature)"意指基底上

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比最小基底厚度較厚之圖案部分。舉例而言，若基底上之圖案包括由基底較薄之三角區域介於基底較厚之三角區域中，如圖3A所示，該"特徵部分"係較厚之三角區域。

高品質III族氮化物裝置層很難成長於圖案化基底上。一種將高品質III族氮化物層成長於圖案化基底或圖案化緩衝層上的技術係磊晶橫向過度成長，如(例如)Zheleva等人之題為"Methods of Fabricating Gallium Nitride Semiconductor Layers By Lateral Growth From Sidewalls Into Trenches, and Gallium Nitride Semiconductor Structures Fabricated Thereby"的美國專利第6,265,289號中所描述。磊晶橫向過度成長技術使III族氮化物層自基底上所形成之圖案化區域，或者成長基底上方所形成的III族氮化物緩衝層上之圖案化區域橫向成長。圖案化區域通常係經蝕刻之凸台，其中橫向成長主要源於凸台頂部，或圖案化區域通常為由遮罩層蝕刻之窗，其中成長主要源於窗內部。當磊晶橫向過度成長可導致產生高品質材料時，一主要缺點在於橫向成長條件通常導致橫向成長材料下方之渠溝中的空隙填充有空氣。由於空氣具有比III族氮化物材料及藍寶石兩者之折射率更低的折射率，該等空隙可導致全內反射，潛在地減少自該裝置所提取的光的數量。此外，用於促進磊晶橫向過度成長之圖案，凸台或藉由遮罩層蝕刻之窗，通常無法經優化以改良自該裝置之光提取。

當III族氮化物層在有利於填充圖案化基底上之特徵部分的條件下成長時，歸因於源自圖案化基底不同特徵部分上

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的晶粒碰撞，所得III族氮化物晶體層粗糙，具有小結晶粒度且/或具有高缺陷密度。半導體發光裝置之層的表面粗糙、小結晶粒及所存在之缺陷可使裝置內部發光效率降級，潛在地破壞藉由圖案化基底所產生之任何益處。缺陷一般亦均勻分佈且集中於圖案化特徵部分邊緣附近或自相鄰特徵部分碰撞處之成長，其可引起諸如發光二級體之大面積裝置的漏電問題。

根據本發明之實施例，於一紋理化或圖案化基底上之III族氮化物晶體的成長發生於多個階段。在第一階段中，成長條件有利於形成一符合基底之無空隙且具有平坦平滑表面之層。在第二階段中，自該第一階段中所產生之缺陷被中斷，且材料品質得以改良。然後，額外的層在有利於形成具一定品質之材料的成長條件下得以成長，該材料之品質係適合於半導體發光裝置中之電活性層及光活性層。基底上之圖案係經選擇以便於無空隙地填充圖案並改良光提取。儘管下述實例描述兩個成長階段，但在某些實施例中，可在第一及第二成長階段之後，繼之以類似於下文所述第一或第二成長階段之額外成長階段，以得到所需材料品質。

圖1說明一根據本發明之實施例的裝置。一第一成長區域41成長於一紋理化或圖案化基底40的上方。合適之基底包括(例如)藍寶石及SiC。一第二成長區域47成長於第一成長區域41之上方。然後，包括有一n-類型區域42、一活性區域43及一p-類型區域44之裝置層成長於該第二成長區域

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47上方。p-類型區域44及活性區域43之一部分係經蝕刻掉以曝露出n-類型區域42之一部分。一n-觸點46形成於n-類型區域42之曝露部分上，且一p-觸點45形成於p-類型區域44之剩餘部分上。觸點45及46通常為反射性的。該裝置安裝於一子基板上或觸點朝下之其他結構，使得光可自裝置通過基底40而提取。

圖2說明一形成圖1所示裝置之方法。在步驟20中，提供一紋理化或圖案化基底40。儘管基底40上之紋理係任意的，但該紋理通常為一重複性圖案。圖3A說明一合適圖案之實例。在圖3A所示之圖案中，三角狀凸起區域1係藉由三角狀凹陷區域2而分隔。圖3A所示之柵格對應於一微米。該圖案可藉由(例如)習知掩模及蝕刻步驟而形成，諸如濕式或乾式蝕刻或離子研磨。圖3B說明一合適基底之一部分的橫截面圖，諸如圖3A所示之基底。該圖案之特徵部分通常具有約5微米之長度1且可具有介於約1微米至約10微米之間的長度。該等特徵部分通常具有至少1微米之間距2。該等特徵部分通常具有約0.4微米之高度3且可具有介於約0.1微米至約1微米之間的高度。

在步驟22中，第一成長區域41在有利於填充成長基底上的圖案中之特徵部分的條件下成長，以形成一平滑層。第一成長區域41通常包括一填充成長基底上之圖案的粗糙成長區域(例如，三維成長之晶粒於橫截面上具有峰部及谷部)，繼之以一平滑成長區域(例如，二維成長)。舉例而言，第一成長區域41可包括一厚度介於0.1至1微米之間且

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具有50至175 nm之RMS粗糙度的粗糙成長區域。粗糙成長區域之一般厚度為約0.7微米，RMS粗糙度為約100 nm。該粗糙成長區域繼之以一RMS粗糙度小於20 nm之平滑區域。平滑區域之一般RMS粗糙度為約5 nm。第一成長區域41可於相對高壓、高溫及高的H_2：NH_3比率之條件下形成，以形成一平滑的無空隙層。第一成長區域41可具有一例如介於約10^9 cm^{-2}與10^{10} cm^{-2}之間的高缺陷密度。在某些實施例中，第二成長區域或後續層之成長消除第一成長區域成長期間所存在之缺陷，使得第一成長區域41不會具有較裝置中其他區域大體較高之缺陷密度。第一成長區域41之最小厚度為基底40上圖案特徵部分之高度或約為0.5微米，無論哪個更大。第一成長區域41通常具有約1.5微米的厚度。包括有一粗糙成長區域繼之以一平滑成長區域之合適的第一成長區域之實例包括具有或不具有可選晶粒聚結層之缺陷減少層(defect reduction layer)及具有或不具有可選晶粒聚結層之晶核層，如美國專利第6,630,692號所揭示，該案以引用方式併入本文中，且如下文所述。

在第一成長區域41後，藉由一減少或消除第一成長區域41中之缺陷或至少部分地防止第一成長區域41中之缺陷擴散至裝置區域42、43及44的第二成長區域47而使得材料品質得以改良。第二成長區域47具有一小於第一成長區域41之缺陷密度。類似於第一成長區域41，第二成長區域47可包括一用於改良裝置中材料品質之粗糙成長區域，繼之以一用於提供適合於裝置中後續層成長之表面的平滑成長區

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域。舉例而言，類似於第一成長區域41，第二成長區域可包括一厚度介於0.1與1微米之間且RMS粗糙度介於50與175 nm之間的粗糙成長區域。粗糙成長區域之一般厚度約為0.7微米，RMS粗糙度約為100 nm。粗糙成長區域繼之以一RMS粗糙度小於20 nm之平滑成長區域。平滑區域之一般RMS粗糙度約為5 nm。適用於改良材料品質之第二成長區域47的實例包括Si摻雜層、具有或不具有可選晶粒聚結層之缺陷減少層，及具有或不具有可選晶粒聚結層之晶核層，如美國專利第6,630,692號中所描述。

在第二成長區域47後，n-類型區域42、活性區域43及p-類型區域44成長。一凸台係經蝕刻且形成觸點45及46。

本文所述實施例中之半導體層係藉由MOCVD以三甲基鎵(TMG)或三乙基鎵(TEG)作為鎵源，三甲基鋁(TMAl)作為鋁源、三甲基銦(TMIn)作為銦源、氨(NH_3)作為氮源、矽烷(SiH_4)作為矽源且以氫氣(H_2)或氮氣(N_2)作為載氣之習知單向流MOCVD反應器中成長。亦可使用其他MOCVD反應器、其他源及載氣，及諸如分子束磊晶法(MBE)或氫化物氣相磊晶法(HVPE)之其他成長方法。

在某些實施例中，一或多個低溫GaN晶核層成長於基底40上以覆蓋基底40上之圖案。低溫晶核層(例如)成長至厚度約為20 nm至約50 nm，通常為約25 nm，且其係於約為500℃至約600℃，通常約為550℃之溫度下成長。儘管在此實施例中，低溫晶核層係GaN，但在其他實施例中可使用其他III族氮化物材料。該等晶核層如M. Iwaya等人之日本

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應用物理雜誌(Japanese Journal of Applied Physics) 37,316 (1998)中所描述，其全文以引用方式併入本文中。

在某些實施例中，第一成長區域41包括一缺陷減少層。該缺陷減少層以一般三維粗糙成長而填充基底40上之圖案。缺陷減少層於約900℃至約1175℃，通常約1125℃之溫度條件下在基底40上成長。在缺陷減少層成長期間，NH_3/TMG與NH_3/H_2之分壓比率(更一般而言，V/III與V/H_2，其中V及III代表自元素週期表之V族及III族之元素)係低於彼等維持平滑成長表面形態所要求者之分壓比率，如裝置層42、43及44。在GaN缺陷減少層成長期間之該等分壓比率的範圍及典型值如下文表1之列(a)所列。缺陷減少層在該等條件下成長為厚度約為0.1 μm至約15 μm，通常為約0.5至1 μm。而後停止TMG流，且缺陷減少層可曝露於連續的氫氣及氨氣流中持續約1秒至約1000秒，通常約為一分鐘。H_2及NH_3環境蝕刻缺陷減少層20之表面。該等成長及蝕刻條件有助於形成一包括通常具有約0.1 μm至約1 μm之直徑的個別獨立GaN晶粒或島狀物之粗糙表面。

在粗糙缺陷減少層成長後，III族氮化物材料聚結入平滑層中係所要的。在某些實施例中，缺陷減少層於粗糙成長後展現自然的晶粒聚結狀態。在某些實施例中，可選GaN晶粒聚結層可於約950℃至約1200℃，通常約1160℃之溫度條件下成長於缺陷減少層上。成長溫度及NH_3/TMG與NH_3/H_2分壓比率係經選擇以促進快速橫向(平行於基底表

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面)成長且導致GaN晶粒之晶粒聚結及一平滑磊晶成長表面之形成。在GaN晶粒聚結層成長期間，該等分壓比率之範圍及典型值係如下表1之列(b)中所列。晶粒聚結層具有(例如)約0.5 μm至約20 μm，通常約0.5至1.5 μm之厚度。晶粒聚結層可經矽摻雜至例如約10^{18} cm^{-3}之濃度。

一可選高溫(標準)GaN層可成長於晶粒聚結層上(若存在)，或者成長於缺陷減少層上。標準GaN層於約950℃至約1200℃，通常約1125℃之溫度下成長。標準GaN層成長期間，NH_3/TMG與NH_3/H_2分壓比率之範圍及典型值係如下表1之列(c)所列。該等成長條件係經選擇以促進平滑成長表面形態及高成長速率。標準GaN層具有(例如)約0.1 μm至約10 μm，通常約2 μm之厚度。標準GaN層可不摻雜或經矽之n-類型摻雜至(例如)約10^{18} cm^{-3}或更高之濃度。

缺陷減少層、可選晶粒聚結層及可選高溫GaN層之次序可可多次重複以進一步減少裝置層42、43及44中之缺陷密度。

表1-成長分壓比率

	NH_3/TMG		NH_3/H_2	
層	典型值	範圍	典型值	範圍
a)缺陷減少層	510	200-1500	0.13	0.1-0.3
b)晶粒聚結層	2200	1000-4000*	0.3	≥0.2，通常0.2-0.9
c)標準層	1680	800-4000*	0.5	≥0.35，通常0.35-0.85

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*歸因於緩慢成長速率之實際限制。

在某些實施例中，第二成長區域47包括一類似於上述參考第一成長區域41所描述之缺陷減少層的缺陷減少層。第二成長區域47之缺陷減少層改良材料品質，且可使用或不使用一可選晶粒聚結層及一可選標準III族氮化物層。在第二成長區域47之缺陷減少層成長期間，以及可選晶粒聚結層與可選標準GaN層之成長期間，NH_3/TMG與NH_3/H_2分壓比率之範圍及典型值係如上表1之列(a)-(c)中所列。

在某些實施例中，第二成長區域47包括一Si摻雜層以改良材料品質。該Si摻雜層可為一於約950℃至約1200℃，通常約1160℃之溫度下成長於第一區域41上之高溫GaN層。在該Si摻雜之GaN層成長期間，NH_3/TMG與NH_3/H_2分壓比率之範圍及典型值可與上表1中列(b)及(c)中所列之彼等用於標準GaN層或晶粒聚結層之範圍及典型值大體上相同。該等成長條件係經選擇以促進平滑成長表面形態。Si摻雜層可經矽之n-類型摻雜至例如約10^{18} cm^{-3}或更高之濃度。

Si摻雜層之形成係如下所述：首先一GaN層成長至厚度為(例如)約0.1 μm至約10 μm，通常約1 μm。而後，停止TMG流且將GaN層曝露於SiH_4或Si_2H_6以將約0.1個單層至約3個單層，通常為約一個單層的矽沈積至該層之表面。所沈積之矽可與層28中之氮反應形成覆蓋該層之部分表面的微遮罩(micro mask)(島狀物)。當III族氮化物隨後在該表面上重新開始成長時，III族氮化物材料於該表面之未覆

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蓋部分上成核，垂直地成長，且而後在該遮罩上方橫向成長以形成一低缺陷密度層。在某些實施例中，成長條件及所輸送之矽的量未產生微遮罩，但足以導致類似於第一區域41之缺陷減少層的粗糙成長。

一可選晶粒聚結層可在大體類似於彼等上述條件的條件下成長於Si摻雜之遮罩的上方。一包括Si摻雜GaN層及可選晶粒聚結層之次序可在第一成長區域41上方重複多次以進一步降低裝置區域42、43及44中之缺陷密度。

儘管在上述實例中，第二成長區域47之層係由GaN形成，然而，在其他實施例中，該等層可由其他III族氮化物材料形成，諸如，InGaN、AlGaN、AlInGaN、AlInGaNAs、AlInGaNP或其組合。類似於上述實例之缺陷減少結構在S. Tanaka等人之日本應用物理雜誌(Japanese Journal of Applied Physics) 39, L831 (2000)中得以描述，其全文以引用方式併入本文中。諸如上述實施例中所使用之微遮罩技術在此技術中可稱為"矽摻雜"或抗界面活性劑方法。

在某些實施例中，第二成長區域47包括一用於改良材料品質之晶核層。一適用於第二成長區域47之晶核層係如上文參考第一成長區域41所述。

圖4係一較大接合裝置之平面圖(意即，面積大於或等於一平方毫米)。圖5係圖4所示裝置沿軸70方向之橫截面圖。圖4及圖5說明可用於如圖1-3與附文中所示及所述任何磊晶結構之觸點的排列。磊晶結構59包括圖1之區域

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41、47、42、43及44。磊晶結構59之活性區域係藉由形成有n-觸點46之三個渠溝而分隔成四個區域。各區域係藉由形成於p-觸點45上之四個p-子基板連接件54而連接至一子基板。n-觸點46環繞該等四個活性區域。n-觸點46藉由六個n-子基板連接件53而連接至一子基板。n-及p-觸點可藉由一絕緣層52而電隔絕。

圖6係一封裝發光裝置之分解圖。一散熱片100置於一嵌入模製導線框架106內。該嵌入模製導線框架106係(例如)一經填充之塑料材料成型於提供一電學路徑之金屬框架的周圍。散熱片100可包括一可選反射碗102。發光裝置晶粒104，其可為任何上述裝置，係直接安裝或經由一熱傳導子基板103間接安裝至散熱片100上。可添加一可為光學透鏡之保護蓋108。

儘管已詳細描述本發明，但彼等熟習此項技術者應瞭解，對於本發明而言可進行不脫離本文所述之發明概念之精神的修改。因此，本發明之範疇不應限定於所說明及描述之特定實施例。

【圖式簡單說明】

圖1說明一根據本發明之實施例的III族氮化物發光裝置。

圖2說明一形成圖1之裝置的方法。

圖3A說明一形成於圖1之基底40的表面上之圖案的實例。

圖3B為基底40之一部分的橫截面圖。

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圖4及圖5為圖1所示觸點排列之平面圖及橫截面圖。

圖6為一封裝發光裝置之分解圖。

【主要元件符號說明】

1	三角狀凸起區域
2	三角狀凹陷區域
40	紋理化或圖案化基底
41	第一成長區域
42	n-類型區域
43	活性區域
44	p-類型區域
45	p-觸點
46	n-觸點
47	第二成長區域
52	絕緣層
53	n-子基板連接件
54	p-子基板連接件
59	磊晶結構
70	軸
100	散熱片
102	可選反射碗
103	熱傳導子基板
104	發光裝置晶粒
106	嵌入模製導線框架
108	保護蓋

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五、中文發明摘要：

本發明係揭示一種III族氮化物發光裝置，其係成長於一紋理基底上，以降低該基底與該III族氮化物層之間的界面處之全內反射的量。在某些實施例中，該裝置包括一大體上無空隙之第一成長區域，及一第二成長區域，該第二成長區域用於改良材料品質，使得高品質層可成長於該第一與第二區域的上方。

六、英文發明摘要：

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P4.13-540

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19.08.2005

ABSTRACT:

A III-nitride light emitting device is grown on a textured substrate, in order to reduce the amount of total internal reflection at the interface between the substrate and the III-nitride layers. In some embodiments, the device includes a first growth region substantially free of voids, and a second growth region that improves the material quality such that high quality layers can be grown over the first and second regions.

Fig. 1

案號：(0486)	國外相應案：☑見申請書 ☐其他：		
中說份數：(	☐改中文 Title	☐細則§17 但書	字數：
☑原文說明書檔名：p:\Foreign Spec\ -filing			存檔人：
譯者：	審稿者：	代表圖：	化學式：

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十、申請專利範圍：

1. 一種結構，其包括：

一紋理基底；

一置於該基底之該紋理表面上的第一III族氮化物區域，該第一III族氮化物區域大體上無空隙；

一置於該第一III族氮化物區域上之第二III族氮化物區域，該第二III族氮化物區域具有一小於該第一III族氮化物區域之平均缺陷密度的平均缺陷密度；及

一置於一n-類型區域與一p-類型區域之間的發光區域，該發光區域覆蓋於該第二III族氮化物區域上。

2. 如請求項1之結構，其中該第一III族氮化物區域具有一大於$10^9 cm^{-2}$之缺陷密度。

3. 如請求項1之結構，其中該第一III族氮化物區域具有一介於0.5微米與10微米之間的厚度。

4. 如請求項1之結構，其中該第一III族氮化物區域包含：

一厚度介於0.1微米與15微米之間的缺陷減少層；及

一厚度介於0.4微米與20微米之間的晶粒聚結層；

其中，該晶粒聚結層之一表面比該缺陷減少層之一表面更平滑。

5. 如請求項4之結構，其中：

該缺陷減少層具有一介於0.5微米與1微米之間的厚度；及

該晶粒聚結層具有一介於0.5微米與1.5微米之間的厚度。

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6. 如請求項1之結構，其中該第二III族氮化物區域包含一矽摻雜區域。

7. 如請求項6之結構，其中該矽摻雜區域包含：

一厚度介於0.1微米與1微米之間的GaN層；及

一厚度介於0.1個單層與3個單層之間的矽層。

8. 如請求項1之結構，其中該第二III族氮化物區域包含：

一厚度介於0.1微米與15微米之間的缺陷減少層；及

一厚度介於0.4微米與20微米之間的晶粒聚結層；

其中，該晶粒聚結層之一表面比該缺陷減少層之一表面更平滑。

9. 如請求項8之結構，其中：

該缺陷減少層具有一介於0.5微米與1微米之間的厚度；及

該晶粒聚結層具有一介於0.5微米與1.5微米之間的厚度。

10. 如請求項1之結構，其進一步包含：

一電連接至該n-類型區域之n-觸點；及

一電連接至該p-類型區域之p-觸點。

11. 如請求項10之結構，其進一步包含：

電連接至該等n-及p-觸點之導線；及

一置於該發光區域上方之保護蓋。

12. 如請求項1之結構，其中：

該基底上之該紋理包含一重複特徵部分之圖案；

該等特徵部分具有一至少為1微米之長度；及

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該等特徵部分具有一介於0.1微米與1微米之間的高度。

13. 如請求項12之結構，其中該圖案具有一包含一峰部及一谷部之橫截面。

14. 如請求項12之結構，其中該等特徵部分具有至少1微米之間隔。

15. 一種結構，其包含：

一紋理基底；

一置於該基底之該紋理表面上的第一III族氮化物區域，該第一III族氮化物區域大體上無空隙，該第一III族氮化物區域包含一與該基底相鄰之第一部分及一第二部分；其中該第二部分之RMS粗糙度小於該第一部分之RMS粗糙度；

一置於該第一III族氮化物區域上之第二III族氮化物區域，該第二III族氮化物區域包含一與該第一III族氮化物區域相鄰之第一部分及一第二部分；其中該第二部分之RMS粗糙度小於該第一部分之RMS粗糙度；及

一置於一n-類型區域與一p-類型區域之間的發光區域，該發光區域覆蓋於該第二III族氮化物區域上。

16. 如請求項15之結構，其中：

該第一區域之該第一部分具有一介於50 nm與175 nm之間的RMS粗糙度；及

該第一區域之該第二部分具有一小於20 nm之RMS粗糙度。

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17. 如請求項15之結構，其中：

該第二區域之該第一部分具有一介於50 nm與175 nm之間的RMS粗糙度；及

該第二區域之該第二部分具有一小於20 nm之粗糙度。

18. 如請求項15之結構，其中該第二III族氮化物區域之該第一部分包含一矽摻雜區域。

19. 如請求項18之結構，其中該矽摻雜區域包含：

一厚度介於0.1微米與1微米之間的GaN層；及

一厚度介於0.1個單層與3個單層之間的矽層。

20. 如請求項15之結構，其中：

該第一區域之該第一部分包含一厚度介於0.1微米與15微米之間的缺陷減少層；及

該第一區域之該第二部分包含一厚度介於0.4微米與20微米之間的晶粒聚結層；

其中，該晶粒聚結層之一表面比該缺陷減少層之一表面更平滑。

21. 如請求項20之結構，其中：

該缺陷減少層具有一介於0.5微米與1微米之間的厚度；及

該晶粒聚結層具有一介於0.5微米與1.5微米之間的厚度。

22. 如請求項15之結構，其進一步包含：

一電連接至該n-類型區域之n-觸點；

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一電連接至該p-類型區域之p-觸點。

23. 如請求項22之結構，其進一步包含：

電連接至該等n-及p-觸點之導線；及

一置於該發光區域上方之保護蓋。

24. 如請求項15之結構，其中：

該基底上之該紋理包含一重複特徵部分之圖案；

該等特徵部分具有一至少1微米之長度；及

該等特徵部分具有一介於0.1微米與1微米之間的高度。

25. 一種製造一半導體發光裝置之方法，該方法包含：

提供一紋理成長基底；

將一第一III族氮化物區域成長於該成長基底上方，其中適於成長該第一III族氮化物區域之成長條件係經選擇以填充該紋理成長基底上之特徵部分，使得該第一III族氮化物區域大體上無空隙；及

將一第二III族氮化物區域成長於該第一III族氮化物區域上方，該第二III族氮化物區域包含一與該第一III族氮化物區域相鄰之第一部分及一第二部分；

其中，該第一區域之該第二部分成長期間的一V族來源之分壓係大於該第一區域之該第一部分成長期間的V族來源之分壓。

26. 如請求項25之方法，其中該第二區域之該第二部分成長期間之一V族來源之分壓係大於該第二區域之該第一部分成長期間的V族來源之分壓。

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27. 如請求項25之方法，其中成長該第二III族氮化物區域之該第一部分包含：

成長一第一GaN層；及

將該第一GaN層之表面曝露於一Si源。

28. 如請求項27之方法，其中將該第一GaN層之一表面曝露於一Si源包含將0.1至3個單層Si沈積至該第一GaN層之該表面上。

29. 一種製造一半導體發光裝置之方法，該方法包含：

提供一紋理成長基底；

將一第一III族氮化物區域成長於該成長基底上方，其中適於成長該第一III族氮化物區域之成長條件係經選擇以填充該紋理成長基底上之特徵部分，使得該第一III族氮化物區域大體上無空隙；及

將一第二III族氮化物區域成長於該第一III族氮化物區域上方，該第二III族氮化物區域包含一與該第一III族氮化物區域相鄰之第一部分及一第二部分；

其中，該第一區域之該第二部分成長期間之一成長溫度係高於該第一區域之該第一部分成長期間之成長溫度。

30. 如請求項29之方法，其中該第二區域之該第二部分成長期間之一成長溫度係高於該第二區域之該第一部分成長期間之成長溫度。

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十一、圖式：

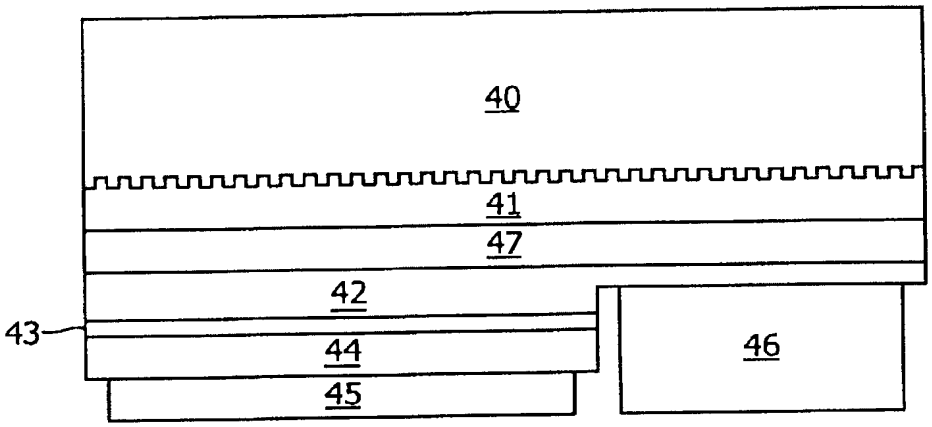


圖 1

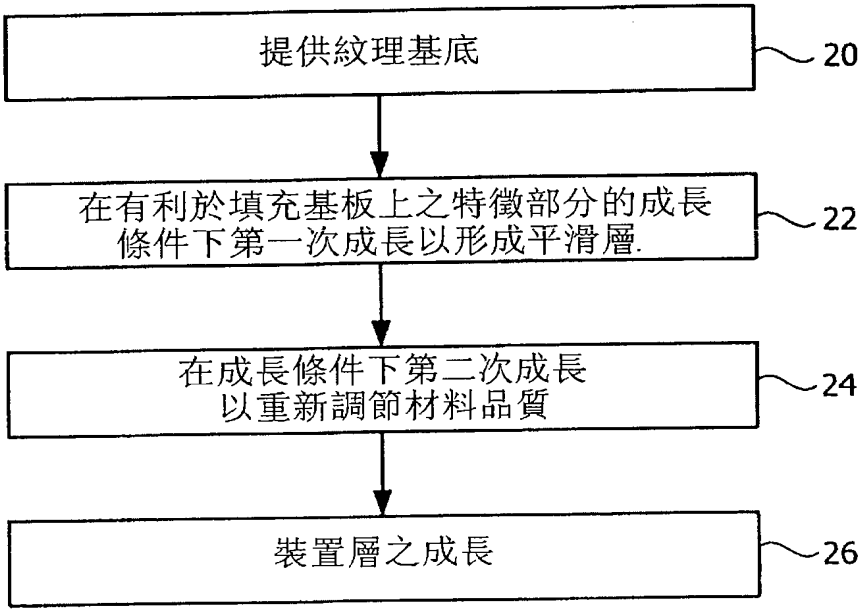


圖 2

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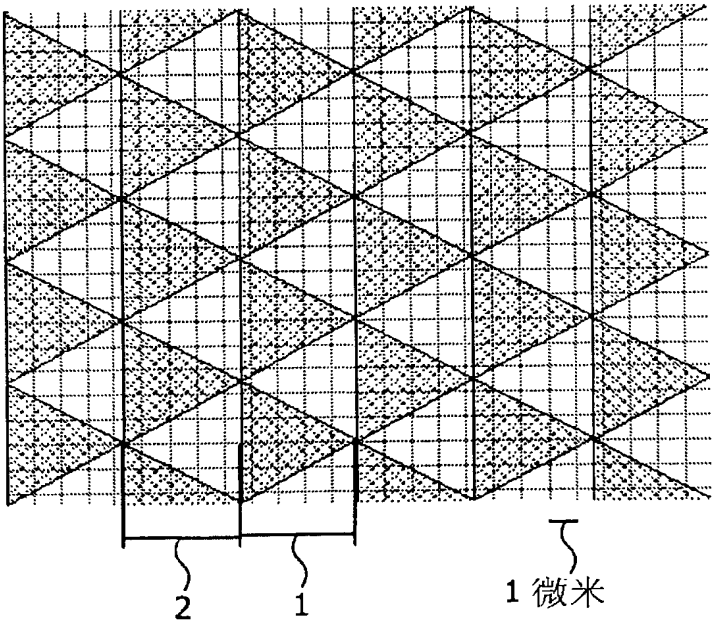


圖 3A

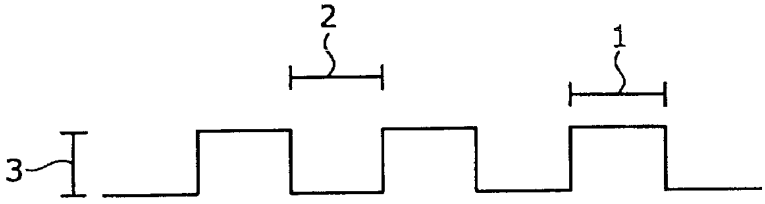


圖 3B

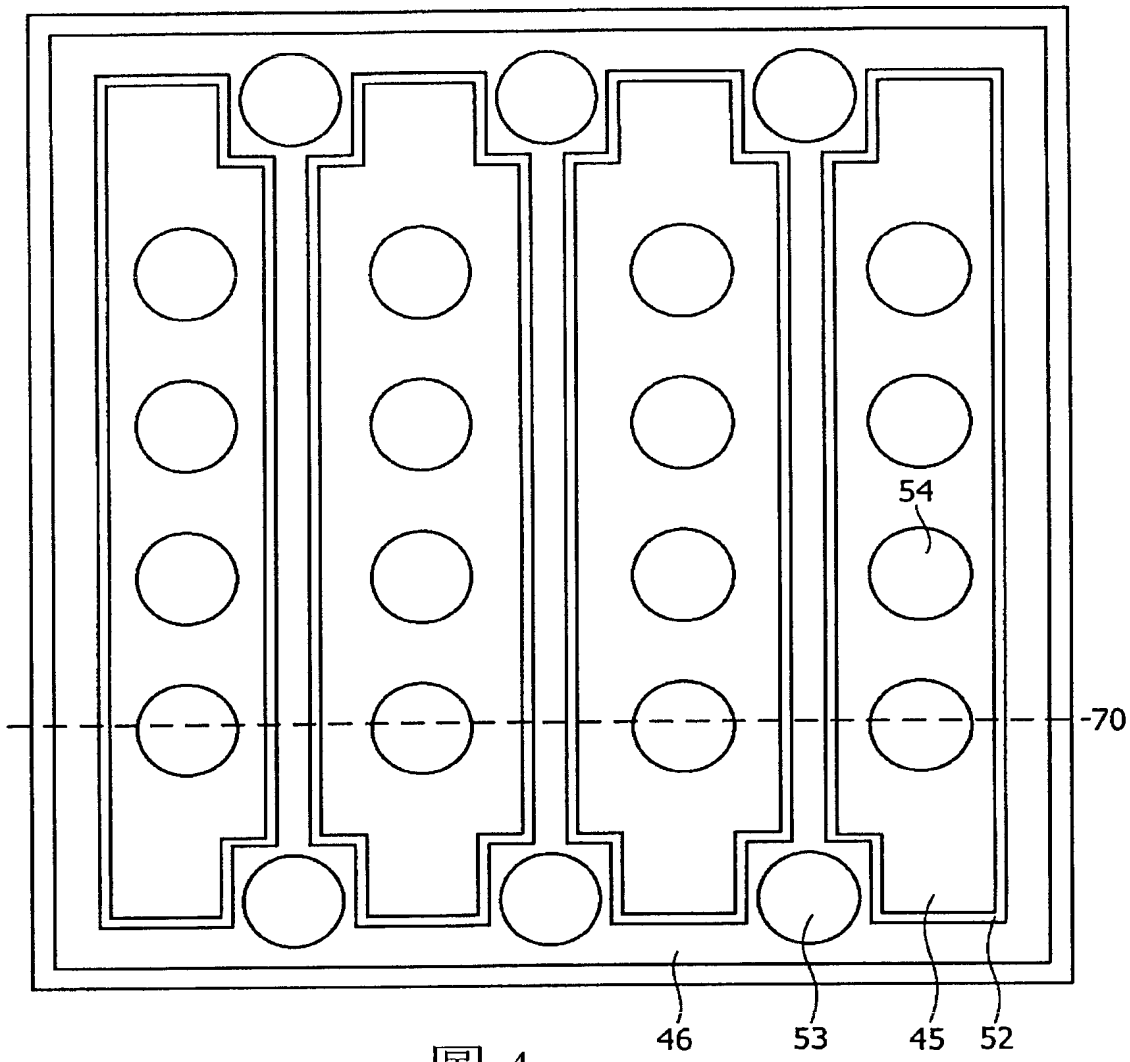


圖 4

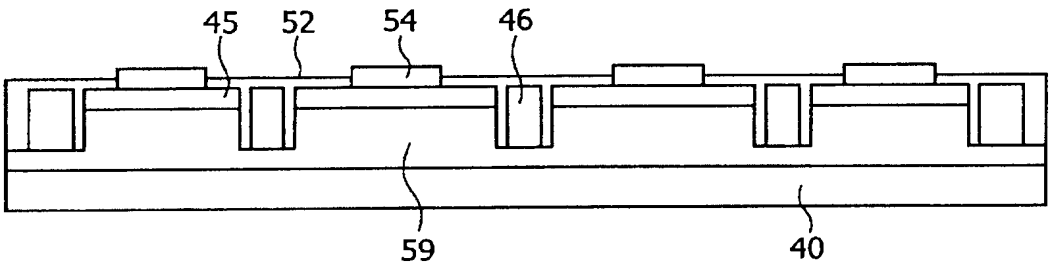


圖 5

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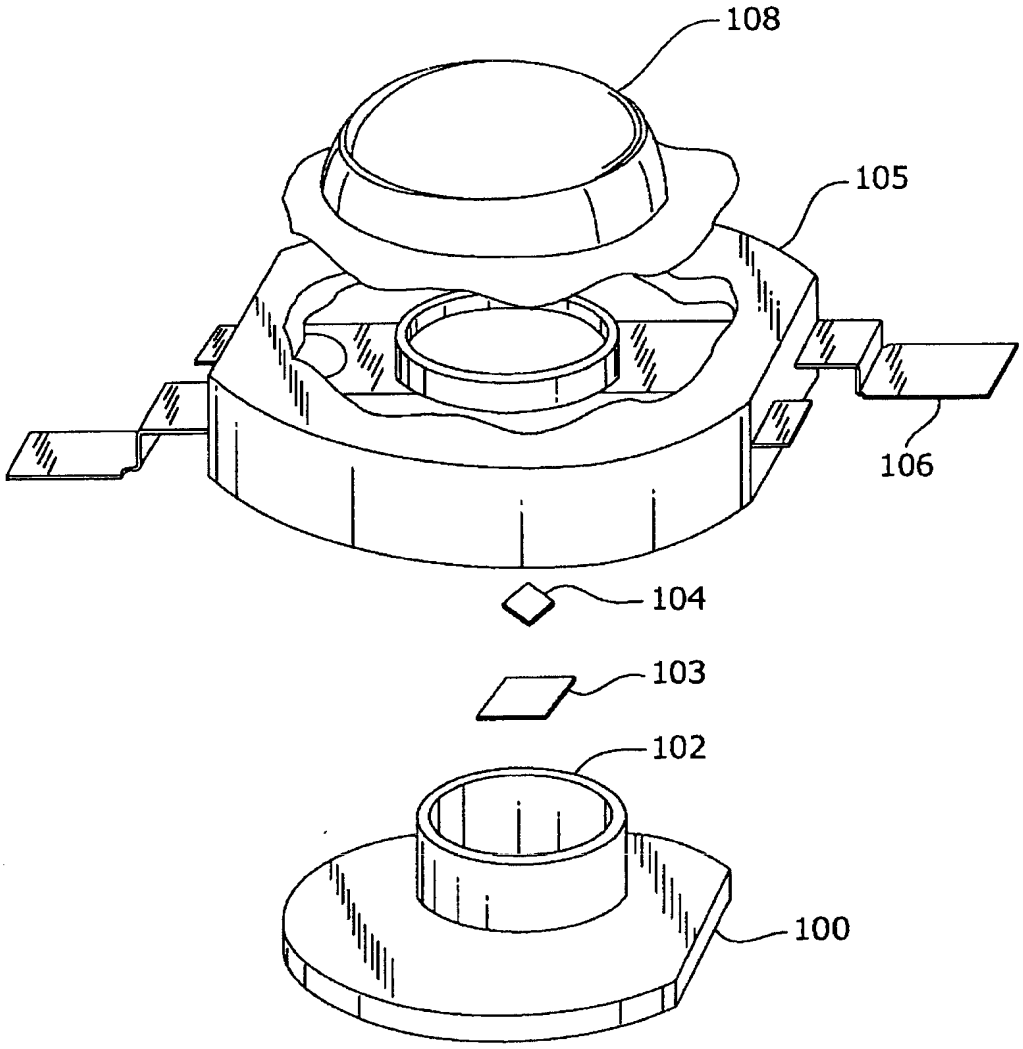


圖 6

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七、指定代表圖：

(一)本案指定代表圖為：第（ 1 ）圖。

(二)本代表圖之元件符號簡單說明：

40	紋理化或圖案化基底
41	第一成長區域
42	n-類型區域
43	活性區域
44	p-類型區域
45	p-觸點
46	n-觸點
47	第二成長區域

八、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

(無)

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Espacenet

Bibliographic data: TW200818529 (A) — 2008-04-16

Thin-film diode structure using a sacrificial doped dielectric layer

Inventor(s): WIDENBORG PER INGEMAR [SE]; ABERLE ARMIN GERHARD [DE] ± (WIDENBORG, PER INGEMAR, ; ABERLE, ARMIN GERHARD)

Applicant(s): NEWSOUTH INNOVATIONS PTY LTD [AU] ± (NEWSOUTH INNOVATIONS PTY LTD)

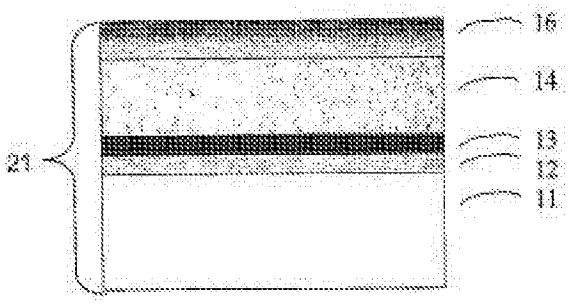
Classification: - international:***H01L31/042***
- cooperative: **H01L29/66113**; **H01L29/868**; **H01L31/0392**; **H01L31/077**; **H01L31/1872**; H01L21/02532; H01L21/02672; H01L21/268; Y02E10/50; Y02P70/521

Application number: TW20070131647 20070827

Priority number (s): AU20060904759 20060831

Also published as: WO2008025057 (A1)

Abstract of TW200818529 (A)



A method of fabricating a thin-film crystalline semiconductor 3-layer diode structure on a foreign supporting substrate or superstrate, and a thin-film crystalline semiconductor 3-layer diode structure on a foreign supporting substrate or superstrate are disclosed. A sacrificial dielectric overlayer (15) containing n or p-type dopant atoms is deposited on an exposed amorphous lightly doped or undoped semiconductor layer of a 2-layer semiconductor structure (13, 14) formed on the substrate or superstrate (11). The amorphous lightly doped or undoped semiconductor layer (13, 14) is crystalised. A heavily doped semiconductor layer is formed by diffusing the n or p-type atoms from the sacrificial dielectric overlayer into a portion of the crystallized lightly doped or

undoped semiconductor layer, whereby the 3-layer diode structure (21) is formed. The sacrificial dielectric overlayer (15) is removed from the 3-layer diode structure.

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200818529

發明專利說明書

（本說明書格式、順序及粗體字，請勿任意更動，※記號部分請勿填寫）

※ 申請案號： 96131647

※ 申請日期： 96.8.27 ※IPC 分類： H01L 31/042(2006.01)

一、發明名稱：（中文/英文）

使用一犧牲摻雜介電層之薄膜二極體結構

THIN-FILM DIODE STRUCTURE USING A SACRIFICIAL DOPED DIELECTRIC LAYER

二、申請人：（共 1 人）

姓名或名稱：（中文/英文）

新南革新股份有限公司 / NEWSOUTH INNOVATIONS PTY LTD

代表人：（中文/英文）

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國 籍：（中文/英文）

澳洲 / AUSTRALIA

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姓 名：（中文/英文）

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2. 艾伯里 阿銘 G. / ABERLE, ARMIN GERHARD

國 籍：（中文/英文）

1. 瑞典 / SWEDEN
2. 德國 / GERMANY

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四、聲明事項：

☐ 主張專利法第二十二條第二項☐第一款或☐第二款規定之事實，其事實發生日期為：。

☑ 申請前已向下列國家（地區）申請專利：

【格式請依：受理國家（地區）、申請日、申請案號　順序註記】

☑ 有主張專利法第二十七條第一項國際優先權：

1. 澳洲、　2006/08/31、　2006904759

☐ 無主張專利法第二十七條第一項國際優先權：

☐ 主張專利法第二十九條第一項國內優先權：

【格式請依：申請日、申請案號　順序註記】

☐ 主張專利法第三十條生物材料：

☐ 須寄存生物材料者：

國內生物材料　【格式請依：寄存機構、日期、號碼　順序註記】

國外生物材料　【格式請依：寄存國家、機構、日期、號碼　順序註記】

☐ 不須寄存生物材料者：

所屬技術領域中具有通常知識者易於獲得時，不須寄存。

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九、發明說明：

【發明所屬之技術領域】

發明領域

本發明廣泛有關於一製造一薄膜晶性半導體3層二極體結構於一外異支撐基材或覆材上之方法，且有關一薄膜晶性半導體3層二極體結構。

【先前技術】

發明背景

諸如玻璃等外異支撐材料上之薄膜晶性半導體裝置結構在譬如薄膜太陽能電池及平板顯示器等電子業中變得日益重要。太陽能電池的案例中，由於其相較於傳統、以矽晶圓為基礎的模組只需要一比例部分的半導體材料之事實，薄膜有潛力鉅幅降低太陽能模組的製造成本。尚且，薄膜太陽能電池具有可以在一大面積支撐材料(-1 m^2)上予以製造之優點，使得製程流線化且進一步降低加工成本。

一晶性半導體二極體通常為結構$n^+\pi p^+$或$p^+\pi n^+$的一3層裝置，其中上標"+"代表重度摻雜而π為p(對於輕度p-型摻雜)、n(對於輕度n-型摻雜)或i(對於本徵性，亦即未摻雜材料)。兩表面層的重度摻雜係容許形成低電阻歐姆接觸部且亦有利於降低二極體中之載體重組率(carrier recombination rate)。

由於透明度及低成本，玻璃是電子件中一種特別重要的支撐外異材料，而能夠具有譬如以液晶為基礎的平板顯示器及覆材組態中的薄膜太陽能模組(亦即，日光經由玻璃

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片進入太陽能電池)。然而，由於玻璃的有限穩定度，使裝置品質晶性半導體材料形成於玻璃上係構成一種可觀的挑戰。

至今發展出的低溫多晶矽太陽能電池之最成功方法之一係為松山等人的“部份摻雜方法”[一固相結晶化方法所製備之高品質多晶矽薄膜]，非晶性固體期刊，Vol. 198-200，pp.940-944 (1966)，其中一2層堆積體的非晶矽材料(1至20微米範圍中的厚度)藉由固相結晶化(SPC)以約600℃在數小時期間產生結晶化。若2層非晶性堆積體由一薄、重度n-型(磷) 摻雜層及一遠為較厚、未摻雜或輕度摻雜層所構成，可藉由SPC獲得優良品質的晶矽材料。此方法所產生的優良材料品質之理由係在於整體堆積體的方向性結晶化，開始係為n^+摻雜層(“長晶”層)且隨後進展經過結構的其餘部分(“結晶化層”)。松山等人已經顯示，一重度磷摻雜非晶矽層係遠比輕度摻雜(未摻雜)矽層更為快速地結晶，且因此作為一n*n(或n*i)結構中之優良長晶層。為了以SPC製的n*n結構實現一二極體結構，松山等人以低溫將一重度p+摻雜氫化非晶矽層沉積在結構上，提供一由晶性及非晶性矽所構成之異質接合二極體。標準測試條件下的測量係顯露出，此等低溫製造的異質接合二極體展現出金屬基材上高於9%良好的太陽能電池效率，具有約10微米之吸收器區(“基底”)中的少數載體擴散長度。

雖然松山等人獲得的效率對於一外異基材上的一薄膜晶矽太陽能電池係為合理，缺點係在於形成重度p^+摻雜氫

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化非晶矽需要一分離的半導體沉積步驟(其中因此n或i-型矽層的表面需以小心且可能昂貴的方式來清潔)並由於非晶矽的低側向電導無法藉由簡單放下一金屬格柵而不需要額外沉積具有低薄片電阻(<1000 Ω/平方)的透明傳導性氧化物(TCO)來實現p^+非晶矽層之接觸，故顯著地增添裝置的製造成本。

巴梭爾(Basore)[玻璃模組上的晶矽之簡化加工及改良的效率，第19屆歐洲光伏太陽能會議的會議紀錄，巴黎，2004六月，pp. 455-458(WIP,慕尼黑,2004)]已經建議另一種用於在一外異基材上實現一薄膜晶矽二極體結構之方法。一n^+pp^+堆積體的非晶矽沉積在一玻璃基材上且隨後整體3層堆積體藉由SPC以約600℃在數個小時期間產生結晶化。並且，n^+層之用途係作為長晶層且因此提供整體非晶性堆積體的方向性結晶化。此途徑的利益係為一較流線化、且因此很可能更合乎成本效益之製程。然而，由於表面處出現重度p-摻雜(硼)層，長晶不只開始於埋設n^+層中且亦在p^+層中。因此，整體堆積體的結晶化係從兩側發生，導致相較於三洋方法(Sanyo method)之顯著降低的顆粒尺寸及顯著較大的瑕疵密度。

因此需要提供企圖解決至少一上述缺點之一用於實現一薄膜晶矽二極體結構之方法。

【發明內容】

發明概要

根據本發明的第一態樣，提供一用於製造一薄膜晶性

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半導體3層二極體結構於一外異支撐基材或覆材上之方法，該方法包含將一含有n或p-型摻雜物原子的一犧牲介電覆層沉積在基材或覆材上所形成的一2層半導體結構之一經曝露的非晶性輕度摻雜或未摻雜半導體層上；將非晶性輕度摻雜或未摻雜半導體層結晶化；藉由將來自犧牲介電覆層的n或p-型原子擴散至結晶化輕度摻雜或未摻雜半導體層的一部分內來形成一重度摻雜半導體層，其中因此形成3層二極體結構；及從3層二極體結構移除犧牲介電覆層。

2層半導體結構可包含非晶性輕度摻雜或未摻雜半導體層及一非晶性重度摻雜經埋設半導體層，且用於將非晶性輕度摻雜或未摻雜半導體層結晶化之步驟包含經由固相結晶化將重度摻雜經埋設半導體層結晶化。

可以約500至650℃範圍中的溫度在約6至48小時的期間進行固相結晶化。

該方法可進一步包含藉由形成一晶性半導體籽晶層於基材或覆材上、製備一氫終止式籽晶層表面於晶性半導體籽晶層上、及將輕度摻雜或未摻雜非晶性層沉積在籽晶層表面上來形成2層半導體結構，且用於將非晶性輕度摻雜或未摻雜半導體層結晶化之步驟係包含固相磊晶。

晶性半導體籽晶層可以相較於重度摻雜半導體層呈相反類型的一極性被重度摻雜。

晶性半導體籽晶層可能未經摻雜或以與重度摻雜半導體層相同的極性被摻雜，且形成2層半導體結構係包含將一非晶性半導體膜沉積在籽晶層表面上以使與晶性半導體籽

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晶層相鄰之非晶性半導體膜的一第一部分以相較於重度摻雜半導體層呈相反類型的一極性被重度摻雜，且使非晶性半導體膜的一第二部分身為非晶性輕度摻雜或未摻雜半導體層，且形成重度摻雜半導體層之步驟進一步包含使來自非晶性半導體膜的第一部分之摻雜物原子擴散至晶性半導體籽晶層內以形成3層半導體結構之一重度摻雜經埋設半導體層。

可以約500至650℃範圍中的溫度在約6至48小時期間進行固相磊晶。

籽晶層可以選自由下列各物所組成的群組之一方法製造：鋁引發式結晶化，金屬引發式結晶化，固相結晶化或雷射引發式結晶化。

該方法可包含形成一介電障壁層於基材或覆材上，及形成3層二極體結構於介電障壁層上。

介電障壁層可包含選自由下列各物所組成的群組之一材料：氮化矽，氧化矽，碳化矽及其一合金或一組合。

3層二極體結構可包含選自由下列各物所組成的群組之一材料：矽，鍺，或矽及鍺的一合金。

犧牲介電覆層可選自由下列各物所組成的群組：氮化矽，氧化矽，碳化矽及其一合金或一組合。

犧牲介電覆層可利用選自由下列各物所組成的群組之一方法作沉積：PECVD，濺鍍及蒸鍍。

可以約1秒至15分鐘範圍中的期間利用約800至1050℃範圍中的一溫度所進行之快速熱退火來擴散來自犧牲介電

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覆層的n或p-型原子藉以形成重度摻雜半導體層。

該方法可進一步包含以約350至650℃範圍中的一溫度在移除犧牲介電覆層之後使3層二極體結構曝露於原子性氫。

犧牲介電覆層可在形成輕度摻雜或未摻雜非晶性半導體結構的最後步驟之後作原位沉積而不破壞真空。

輕度摻雜或未摻雜半導體層的摻雜可低於約$10^{18}cm^{-3}$，且重度摻雜經埋設半導體層的摻雜大於約$10^{18}cm^{-3}$。

一其上可支撐3層半導體結構之表面係可被紋理化以輔助光困陷在3層半導體結構中。

根據本發明的第二態樣，提供利用如第一態樣中所界定的一方法形成於一外異支撐基材或覆材上之一薄膜晶性半導體3層二極體結構。

圖式簡單說明

一般熟習該技術者瞭解將連同圖式僅藉由範例從下文描述容易地得知且更加瞭解本發明的實施例，其中:

第1至5圖為顯示利用固相結晶化(SPC)之裝置的製造之示意橫剖視圖；

第6至10圖為顯示利用固相磊晶(SPE)之裝置的製造之示意橫剖視圖。

【實施方式】

較佳實施例之詳細說明

一所描述方法係使用一非晶性$n^+\pi$(或$p^+\pi$) 2層結構上之

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一犧牲摻雜介電覆層，其具有以約600℃藉由SPC之非晶性2層堆積體的一後續結晶化。利用約800至1050℃範圍中的高溫之一分離的快速熱退火(RTA)期間從經摻雜覆層至下方晶矽層內之摻雜物擴散藉以產生$n^+\pi p^+$(或$p^+\pi n^+$)薄膜晶性二極體結構的第三、重度摻雜層。RTA之後係為約500至620℃範圍中利用原子性氫之一瑕疵鈍化處理，其中因此在氫化處理之前以一氫氟酸沾浸來移除經摻雜覆層(經摻雜氧化矽)。第三層中之摻雜物的一大比例部分在氫化處理之後係為電子主動性。

另一所描述方法中，單層的π-型(亦即，輕度摻雜或未摻雜)非晶矽係沉積至一玻璃片上的一氫終止式重度摻雜晶矽籽晶層上，接著係為犧牲摻雜介電覆層之沉積。由於出現晶性籽晶層(其提供長晶表面)，在此例中經由固相磊晶(SPC)發生非晶矽層的結晶化。對於非晶矽層的SPE之詳細描述請參照威登柏格(Widenborg)等人的[藉由固相磊晶之玻璃上的AIC多晶矽籽晶層之磊晶加厚，結晶生長期刊，Vol.276，pp.19-28 (2005)]，其內容合併於本文中以供參考。再度利用約800至1050℃範圍中的高溫之一快速熱退火(RTA)期間從犧牲摻雜覆層至下方晶矽層內之摻雜物擴散藉以生成所需要的第三、重度摻雜層。在約500至620℃範圍中以原子性氫的一處理之前以一氫氟酸沾浸來移除犧牲摻雜覆層(經摻雜氧化矽)。第三層中之摻雜物的一大比例部分在氫化處理之後係為電子主動性。

現在將參照第1至5圖來描述利用SPC之裝置的製造。

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一薄介電障壁層12沉積在一外異支撐材料11上，如第1圖所示。應注意外異支撐材料11可被適當地紋理化以輔助光困陷在經光製3層半導體結構中。為求清楚起見，第1至5圖中已經省略紋理。介電障壁層12包含一介電材料諸如氮化矽，氧化矽，碳化矽或者這些材料的一合金或一組合。譬如，在玻璃覆材的案例中，可利用矽烷、氨及氮的一氣體混合物藉由電漿增強化學氣相沉積(PECVD)方法來沉積一具有約70 nm厚度之SiN膜。接著，非晶性半導體材料之一2層堆積體(13，14)沉積在薄介電層12上，其中第一層13被重度摻雜而第二層14被輕度摻雜或為本徵性，如第2圖所示。層13及14可包含非晶性半導體材料諸如矽，鍺或矽及鍺的一合金。譬如，可以約375至425℃範圍中的一沉積溫度利用矽烷及經摻雜氫的一氣體混合物藉由PECVD方法來沉積非晶矽，其中第一層13在約$1x10^{18}$至$1x10^{21}cm^{-3}$磷原子範圍中被重度摻雜，其具有約$1x10^{20}cm^{-3}$的較佳磷濃度及約50 nm的較佳厚度。第二層14可在約$1x10^{15}$至$1x10^{18}cm^{-3}$範圍中藉由硼被輕度p-型摻雜，其具有約$5x10^{16}$的較佳硼濃度及約1500 nm的較佳厚度。

一薄摻雜介電層15隨後沉積在非晶性半導體層14上，如第3圖所示。介電層15可包含一介電材料，諸如氮化矽，氧化矽，碳化矽或者這些材料的一合金或一組合。介電層15可利用諸如電漿增強式化學氣相沉積(PECVD)、濺鍍或蒸鍍等沉積技術作沉積。一範例中，具有約70 nm厚度之介電層15係包含一含有痕量的碳之經硼摻雜(p-型)氧化矽，其

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在300至350℃基材溫度、一標準平行板組態中經由射頻(13.56 MHz) PECVD (RF PECVD)作沉積。一範例所使用之氣體混合物係由下列所組成(括弧中的氣流): 矽烷(約1 sccm)，氫(約2 sccm)中的0.5%三甲硼，一氧化二氮(約150 sccm)，及氮(約150 sccm)。沉積壓力約為150毫托耳(mTorr)且功率密度約為0.025 W/cm^2。所產生的沉積速率約為10 nm/min。一範例中，介電層15在非晶性半導體沉積步驟(相較第2圖)之後作原位沉積而不破壞一真空沉積室中的真空。

裝置20隨後受到一熱退火，其中非晶性半導體層13及14經由SPC產生結晶化且其中經曝露薄介電層15中的摻雜原子未顯著地擴散至半導體層13及14內。一範例中，在約500至650℃範圍中的溫度以約6至48小時期間進行結晶化。所描述範例中，此熱退火步驟在一氮清除式大氣壓爐具中進行。

接著係使裝置20受到處於高溫的一快速熱退火(RTA)處理，其中因此使經曝露薄介電層15中的摻雜原子顯著地擴散至晶性半導體層14內且因此生成一位於層15與14之間的第三摻雜層16，如第4圖所示。一範例中，RTA在約800至1050℃的一溫度範圍中進行位於約1秒至15分鐘範圍中之一段期間。

隨後，薄摻雜介電層15被移除且裝置21受到一原子性氫處理，如第5圖所示。一範例中，在約350至650℃範圍中的一溫度進行對於原子性氫的曝露。

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已經藉由PECVD(電漿增強式化學氣相沉積)製造利用參照上文第1至5圖所述的方法製成之數個1.5微米厚矽太陽能電池裝置，其中利用一硼矽酸玻璃片11，一氮化矽層12，一重度磷摻雜非晶性Si:H層13，一輕度硼摻雜非晶性Si:H層14，及一原位沉積於基底層14上之重度硼摻雜矽(碳)氧化物層15。非晶矽層13及14隨後以約600℃在約15小時期間產生結晶化。裝置隨後在約900℃以5分鐘受到一RTA處理，在該期間藉由摻雜物擴散生成第三、重度摻雜層16。隨後藉由在氫氟酸中蝕刻來移除犧牲硼摻雜矽(碳)氧化物層15，接著是約610℃玻璃溫度歷時約15分鐘時程之一氫化製程。

所產生的p^+層(層16)被硼重度摻雜，如同低達1000歐姆/平方之所測得的薄片電阻及用於決定摻雜極性之熱探針測量所確認。製成的p-n接面太陽能電池之電性特徵化係顯示，用於形成重度摻雜背表面層(背表面場(BSF)層)之所描述的犧牲摻雜介電覆層方法相較於習知生長的BSF層之裝置而言具有較優品質。具有所描述經擴散BSF層之太陽能電池及一其中唯一差異在於一習知生長的BSF層之均等裝置之開路電壓差係為一顯著的40至50 mV，其中對於所描述經擴散BSF層具有一較高電壓。具有經由犧牲摻雜介電覆層方法所形成的所描述BSF層之太陽能電池係具有高於500 mV之一1-太陽開路電壓(1-sun open circuit voltage)且胞元受到寄生理想性因數n=2重組之可忽略的影響，潛在能夠具有極高的充填因數(且因此具有高的太陽能轉換效率)。一具有一

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經擴散BSF層之金屬化太陽能電池係獲得超過70%的一充填因數，其為對於玻璃上的多晶矽太陽能電池之優良數值。

現在將參照第6至10圖來描述利用SPE之裝置的製造。

一薄介電障壁層112沉積在一外異支撐材料111上且一薄、大顆粒狀重度摻雜($>10^{18}cm^{-3}$)晶性半導體層117形成於層112上，如第6圖所示。應注意外異支撐材料112可被適當地紋理化以輔助光困陷於經光製3層半導體結構中。為求清楚起見，第6至10圖中已經省略紋理。熟習該技術者將瞭解，一薄(<<1微米)晶性半導體層形成於一外異基材上係遠比使用既有沉積技術之一厚(>1微米)晶性層的形成更為容易。確切言之，可利用諸如鋁引發式結晶化、金屬引發式結晶化、固相結晶化、或雷射引發式結晶化等技術來製造晶性半導體層或籽晶層117。介電障壁層112包含一介電材料諸如氮化矽，氧化矽，碳化矽或這些材料的一合金或一組合。譬如，可使用矽烷、氨及氮的一氣體混合物藉由PECVD方法來沉積具有70 nm±10 nm厚度的一SiN膜。接著，生成一潔淨及氫終止式籽晶層表面，接著係為沉積一輕度摻雜非晶性半導體層118，如第7圖所示。一潔淨的氫終止式矽表面譬如由下列步驟實現: (i)矽表面浸於過氧化氫及硫酸之一新鮮1:1混合物中10分鐘；在去離子水中沖洗表面；(iii)晶矽層117的表面浸入一5%氫氟酸溶液中直到表面為斥水性為止，接著在去離子水中作一沖洗。具有潔淨的氫終止式矽表面及其支撐層111及112之晶矽層117在清潔步驟完成的約60分鐘內被裝載至真空機中。層118可包含

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非晶性半導體材料諸如矽，鍺或矽與鍺的一合金。譬如，非晶矽可以約375至425℃範圍的沉積溫度利用矽烷及經摻雜氫的一氣體混合物藉由PECVD方法作沉積，其中層118以位於約$1x10^{15}$至$1x10^{18}cm^{-3}$範圍中被硼輕度p-型摻雜，其具有約$5x10^{16}$的較佳硼濃度及約1500 nm的較佳厚度。

一薄摻雜介電層119隨後沉積在非晶性半導體層118上，如第8圖所示。介電層119可包含一介電材料，諸如氮化矽，氧化矽，碳化矽或這些材料的一合金或一組合。介電層119可利用諸如PECVD、濺鍍或蒸鍍等沉積技術作沉積。一範例中，約有70 nm厚度之介電層119係包含一含有痕量的碳之硼摻雜(p-型)氧化矽，其在約300至350℃的至少一基材溫度以一標準平行板組態經由射頻(13.56 MHz) PECVD(RF PECVD)作沉積。吾人實驗中所使用的氣體混合物係由下列組成: 矽烷(約1 sccm)，氫(約2 sccm)中的0.5%三甲硼，一氧化二氮(約150 sccm)，及氮(約150 sccm)。沉積壓力約為150毫托耳(mTorr)且RF功率密度約為0.025 W/cm^2，導致約10 nm/min的沉積速率。一範例中，介電層119在非晶性半導體沉積步驟(相較第7圖)之後作原位沉積而不破壞一真空沉積室中的真空。

裝置121隨後受到一熱退火，其中非晶性半導體層118經由SPE產生結晶化且其中經曝露薄介電層119中的摻雜原子未顯著地擴散至半導體層118內。一範例中，在約500至650℃範圍中的溫度以約6至48小時期間進行結晶化。

接著使裝置121受到處於高溫的一快速熱退火(RTA)處

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理，其中因此使薄介電層119中的摻雜原子顯著地擴散至晶性半導體層118內且生成一位於層119與118之間的第三、重度摻雜層120，如第9圖所示。一範例中，RTA在約800至1050℃的一溫度範圍中進行約1秒至15分鐘範圍中之一段期間。

隨後，薄摻雜介電層119被移除且裝置122受到一原子性氫處理，如第10圖所示。一範例中，在約350至650℃範圍中的一溫度進行對於原子性氫的曝露。

利用上述參照第6至10圖描述的方法所製造之玻璃上的太陽能電池亦已被製作並相較於用以形成背表面場(BSF)層的習知途徑亦已展現優異之開路電壓。

在上文參照第6至10圖所描述實施例之修改中，不採用一重度摻雜(>$10^{18}cm^{-3}$)晶性半導體籽晶層，形成一本徵性(亦即未摻雜)籽晶層、或一具有低摻雜位準及/或不良摻雜極性之籽晶層。非晶性半導體層118可在經修改實施例中沉積為一2摻雜位準結構，而與籽晶層相鄰之層118的一薄區(厚度約50 nm±20nm)含有對於籽晶層貢獻之過多的摻雜原子(5x10^{19}至1x$10^{21}cm^{-3}$範圍的濃度之n或p-型)。RTA步驟期間，層118中來自相鄰區之過多摻雜物擴散至籽晶層117內且形成籽晶層中所想要的摻雜位準及極性，而與如上述的重度摻雜BSF層120之形成呈現同時。與籽晶層相鄰之層118中的過多摻雜係具有與BSF層120相反之摻雜極性。

所描述的方法經由SPC或SPE提供晶性半導體材料的一3層堆積體($n^+\pi p^+$或$p^+\pi n^+$)之製造，其中只從一側發生整體堆積體的結晶化。這相較於從兩側之整體3層堆積體的結晶

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化而言可提供經改良的顆粒尺寸及較低的瑕疵密度。並且，晶性層中沿著譬如顆粒邊界等較佳區域之來自經摻雜介電質之增強的摻雜物擴散係可在製成的二極體中提供降低的重組率(recombination rate)。

由於非晶矽比起晶矽對於污染曝露而言顯著地更為敏感，所描述方法的一額外利益在於沉積在非晶性半導體上之摻雜介電層亦作為結晶化及樣本處置期間對抗大氣汙染之一保護性擴散障壁。

尚且，摻雜介電層防止來自RTA室的污染物在RTA製程期間擴散至晶性半導體內，其由於RTA製程期間所使用的很高溫度故通常身為重大污染來源。

所描述方法係能夠以一流線化製程來實現玻璃上的$n^+\pi p^+$(或$p^+\pi n^+$)均質接合晶性薄膜二極體結構同時維持高材料品質。這提供顯著潛力來實現更合乎成本效益且仍有效率的薄膜太陽能電池及模組。

熟習該技術者將瞭解，可如特定實施例所顯示對於本發明作出許多變異及/或修改而不脫離如廣泛描述之本發明的精神或範圍。因此該等實施例在各方面被視為示範性而非限制性。

【圖式簡單說明】

第1至5圖為顯示利用固相結晶化(SPC)之裝置的製造之示意橫剖視圖；

第6至10圖為顯示利用固相磊晶(SPE)之裝置的製造之示意橫剖視圖。

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【主要元件符號說明】

11,111…外異支撐材料

12…薄介電障壁層

13…第一層

14…第二層

15,119…薄摻雜介電層

16…第三摻雜層

20…裝置

21,121…裝置

112…薄介電障壁層

117…薄、大顆粒狀重度摻雜晶性半導體層

118…輕度摻雜非晶性半導體層

120…第三、重度摻雜層

122…裝置

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五、中文發明摘要：

本發明揭露一製造一薄膜晶性半導體3層二極體結構於一外異支撐基材或覆材上之方法、及一位於一外異支撐基材或覆材上之薄膜晶性半導體3層二極體結構。一含有n或p-型摻雜物原子之犧牲介電覆層係沉積在基材或覆材上所形成之一2層半導體結構的一經曝露非晶性輕度摻雜或未摻雜半導體層上。非晶性輕度摻雜或未摻雜半導體層係被結晶化。藉由將n或p-型原子從犧牲介電覆層擴散至經結晶輕度摻雜或未摻雜半導體層的一部分內來形成一重度摻雜半導體層，其中因此形成3層二極體結構。犧牲介電覆層自3層二極體結構被移除。

六、英文發明摘要：

A method of fabricating a thin-film crystalline semiconductor 3-layer diode structure on a foreign supporting substrate or superstrate, and a thin-film crystalline semiconductor 3-layer diode structure on a foreign supporting substrate or superstrate are disclosed. A sacrificial dielectric overlayer (15) containing n or p-type dopant atoms is deposited on an exposed amorphous lightly doped or undoped semiconductor layer of a 2-layer semiconductor structure (13, 14) formed on the substrate or superstrate (11). The amorphous lightly doped or undoped semiconductor layer (13, 14) is crystalised. A heavily doped semiconductor layer is formed by diffusing the n or p-type atoms from the sacrificial dielectric overlayer into a portion of the crystallised lightly doped or undoped semiconductor layer, whereby the 3-layer diode structure (21) is formed. The sacrificial dielectric overlayer (15) is removed from the 3-layer diode structure.

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十、申請專利範圍：

1. 一種用於製造一薄膜晶性半導體3層二極體結構於一外異支撐基材或覆材上之方法，該方法包含：將一包含n或p-型摻雜物原子的犧牲介電覆層沉積在該基材或覆材上所形成之一2層半導體結構的一經曝露非晶性輕度摻雜或未摻雜半導體層上；將該非晶性輕度摻雜或未摻雜半導體層結晶化；藉由將來自該犧牲介電覆層的n或p-型原子擴散至該結晶化輕度摻雜或未摻雜半導體層的一部分內來形成一重度摻雜半導體層，其中因此形成3層二極體結構；及從該3層二極體結構移除該犧牲介電覆層。
2. 如申請專利範圍第1項之方法，其中該2層半導體結構包含該非晶性輕度摻雜或未摻雜半導體層及一非晶性重度摻雜經埋設半導體層，且用於將該非晶性輕度摻雜或未摻雜半導體層結晶化之步驟係包含經由固相結晶化將該重度摻雜經埋設半導體層結晶化。
3. 如申請專利範圍第2項之方法，其中以約500至650℃範圍中的溫度在約6至48小時期間進行該固相結晶化。
4. 如申請專利範圍第1項之方法，進一步包含藉由形成一晶性半導體籽晶層於該基材或覆材上、製備一氫終止式籽晶層表面於該晶性半導體籽晶層上、及將該輕度摻雜或未摻雜非晶性層沉積在該籽晶層表面上來形成該2層半導體結構，且用於將該非晶性輕度摻雜或未摻雜半導體層結晶化之步驟係包含固相磊晶。

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5. 如申請專利範圍第4項之方法，其中該晶性半導體籽晶層係以相較於該重度摻雜半導體層呈相反類型的一極性被重度摻雜。

6. 如申請專利範圍第4項之方法，其中該晶性半導體籽晶層係未經摻雜或以與該重度摻雜半導體層相同的一極性被摻雜，且形成該2層半導體結構係包含將一非晶性半導體膜沉積在該籽晶層表面上以使與該晶性半導體籽晶層相鄰之該非晶性半導體膜的一第一部分以相較於該重度摻雜半導體層呈相反類型的一極性被重度摻雜，且使該非晶性半導體膜的一第二部分身為該非晶性輕度摻雜或未摻雜半導體層，且形成該重度摻雜半導體層之步驟進一步包含使來自該非晶性半導體膜的第一部分之摻雜物原子擴散至該晶性半導體籽晶層內以形成該3層半導體結構之一重度摻雜經埋設半導體層。

7. 如申請專利範圍第4至6項中任一項之方法，其中以約500至650℃範圍中的溫度在約6至48小時期間進行該固相磊晶。

8. 如申請專利範圍第4至7項中任一項之方法，其中該籽晶層係以選自由下列各物所組成的群組之一方法製造：鋁引發式結晶化，金屬引發式結晶化，固相結晶化或雷射引發式結晶化。

9. 如前述申請專利範圍任一項之方法，包含形成一介電障壁層於該基材或覆材上，及形成該3層二極體結構於該介電障壁層上。

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10. 如申請專利範圍第9項之方法，其中該介電障壁層包含選自由下列各物所組成的群組之一材料：氮化矽，氧化矽，碳化矽及其一合金或一組合。

11. 如前述申請專利範圍任一項之方法，其中該3層二極體結構包含選自由下列各物所組成的群組之一材料：矽，鍺，或矽及鍺的一合金。

12. 如前述申請專利範圍任一項之方法，其中該犧牲介電覆層選自由下列各物所組成的群組：氮化矽，氧化矽，碳化矽及其一合金或一組合。

13. 如前述申請專利範圍任一項之方法，其中該犧牲介電覆層利用選自由下列各物所組成的群組之一方法作沉積：PECVD，濺鍍及蒸鍍。

14. 如前述申請專利範圍任一項之方法，其中以約1秒至15分鐘範圍中的期間利用約800至1050℃範圍中的一溫度所進行之快速熱退火來擴散來自該犧牲介電覆層的n或p-型原子藉以形成該重度摻雜半導體層。

15. 如前述申請專利範圍任一項之方法，進一步包含以約350至650℃範圍中的一溫度在移除該犧牲介電覆層之後使該3層二極體結構曝露於原子性氫。

16. 如前述申請專利範圍任一項之方法，其中該犧牲介電覆層在形成該輕度摻雜或未摻雜非晶性半導體結構的最後步驟之後作原位沉積而不破壞真空。

17. 如前述申請專利範圍任一項之方法，其中該輕度摻雜或未摻雜半導體層的摻雜係低於約$10^{18}cm^{-3}$，且該重度摻

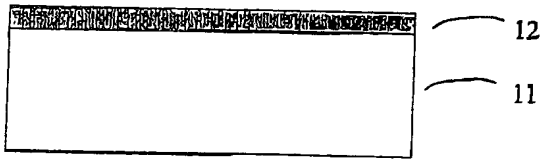
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雜經埋設半導體層的摻雜大於約$10^{18}cm^{-3}$。

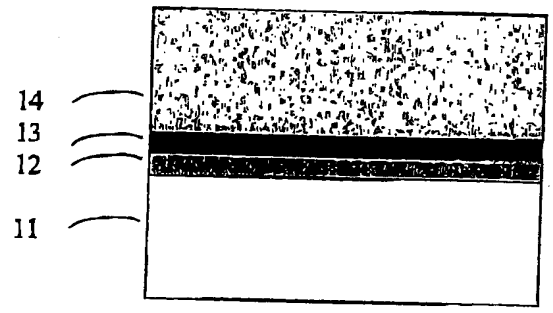
18. 如前述申請專利範圍任一項之方法，其中一其上支撐該3層半導體結構之表面係被紋理化以輔助光困陷在該3層半導體結構中。

19. 一種薄膜晶性半導體3層二極體結構，其利用根據申請專利範圍第1至18項中任一項之方法形成於一外異支撐基材或覆材上。

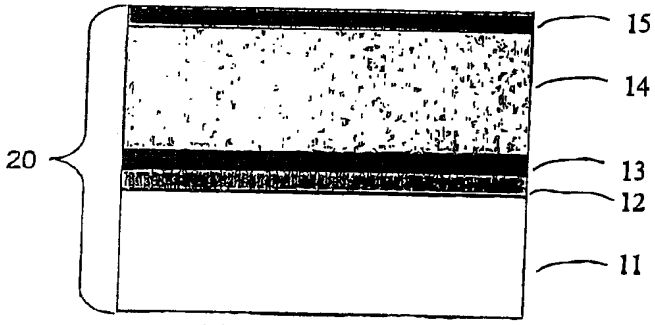
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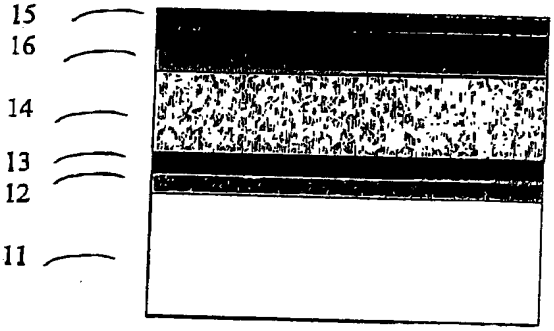
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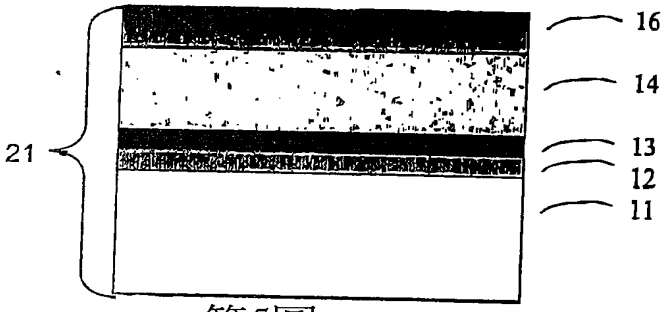
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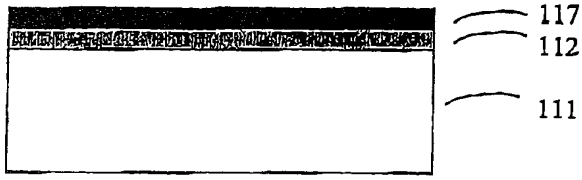
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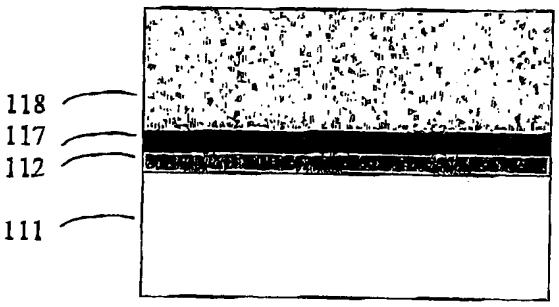
第4圖



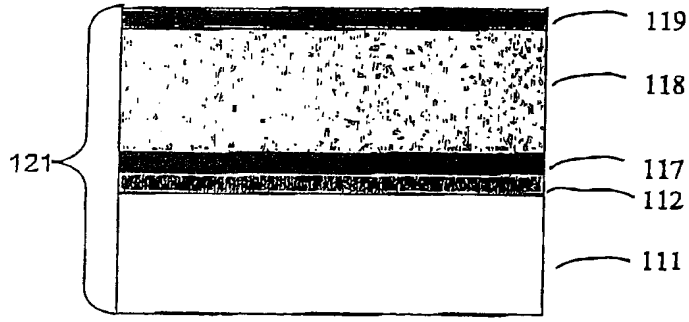
第5圖



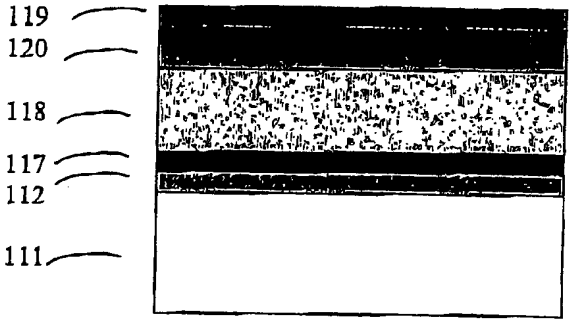
第6圖



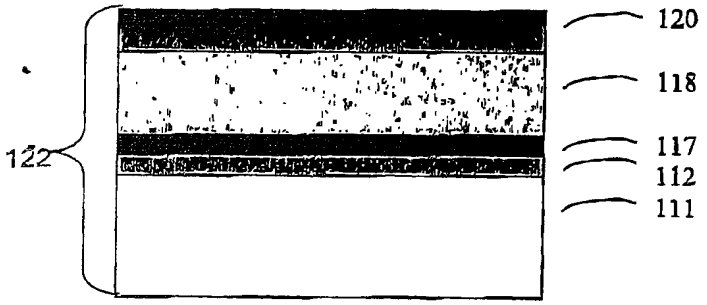
第7圖



第8圖



第9圖



第10圖

七、指定代表圖：

(一)本案指定代表圖為：第（ 5 ）圖。

(二)本代表圖之元件符號簡單說明：

11…外異支撐材料
12…薄介電障壁層
13…一層
14…第二層
16…第三摻雜層
21…裝置

八、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

SAMSUNG EX. 1002 - 2362/2862

Electronic Patent Application Fee Transmittal

Application Number:	15216244
Filing Date:	21-Jul-2016
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Filer:	Reza Mollaaghababa
Attorney Docket Number:	143705.05221

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 2 months with $0 paid	1252	1	600	600
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**780**

Electronic Acknowledgement Receipt

EFS ID:	30934601
Application Number:	15216244
International Application Number:	
Confirmation Number:	5052
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	136549
Filer:	Reza Mollaaghababa
Filer Authorized By:	
Attorney Docket Number:	143705.05221
Receipt Date:	13-NOV-2017
Filing Date:	21-JUL-2016
Time Stamp:	17:27:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$780
RAM confirmation Number	111417INTEFSW17280500
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Response.pdf	276706 7a98fc04d04d06784af11039b8138c725dbf551f	yes	16
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	6	
	Applicant Arguments/Remarks Made in an Amendment		7	16	
Warnings:					
Information:					
2	Transmittal Letter	IDS_filed_13Nov2017.pdf	75739 f32cb58c794eabc5a0399cdd746672e4a301073b	no	2
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	SB08.pdf	1036060 26ffe0e7711df47f4435c53db5c3a2a8ea6512f3	no	6
Warnings:					
Information:					
4	Foreign Reference	TW200627675.pdf	2216562 208dd9813e9baed8124c8d9cce5f719b74867157	no	30
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Information:					
5	Foreign Reference	TW200818529.pdf	2198415 ff6438f89efacc49cc528aa6d617efb4933ed873	no	27

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6	Non Patent Literature	Ohring_1992.pdf	1967436 9c6394aa4e664a406b717c36e5623f3f6df0434a	no	4
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Information:					
7	Non Patent Literature	Campbell_2001.pdf	1578476 594485326236798ed7002e1d0554577118 51a68d	no	5
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Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	32232 53e6f9f69d007f2219cf7575d04a0dfec48f6d45	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	9381626		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/216,244	Filing Date 07/21/2016	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **11/13/2017**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 31	Minus	** 32	= 0	X $0 =	0
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $0 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
BURNELL L. ROSS

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/216,244	07/21/2016	Martin U. Pralle	143705.05221	5052

136549 7590 02/22/2018

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
02/22/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketingbn@pepperlaw.com
davisdr@pepperlaw.com

SAMSUNG EX. 1002 - 2369/2862

Office Action Summary	Application No. 15/216,244	Applicant(s) PRALLE ET AL.	
	Examiner LONG PHAM	Art Unit 2814	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/13/2017*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *34-61,63,64 and 67* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *34, 36-37, 39-61, 63, 64, and 67* is/are rejected.

8)☒ Claim(s) *35,38 and 53* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *11/13/2017*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

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The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 34, 36, 39-51 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Haddad et al. WO 2011035188 (a reference cited by the applicant) in combination with Ooka (JP407074240) and Bour et al. (US pat 8470619) (reference previously cited).

With respect to claim 34, Haddad et al. teach an imager, comprising (see figs. 1-17, particularly fig. 3 and associated text):

at least two adjacent light sensitive pixels having a light incident surface (top), and a backside surface (bottom) opposite the light incident surface;

a peripheral isolation element 30 at least partially separating said two adjacent light sensitive pixels;

each of said pixels having at least one doped region 14,16 disposed on at least one of the light incident surface and the backside surface.

Haddad et al. fail to teach the peripheral isolation element comprises at least two materials having different indices of refraction.

Ooka teaches an imager in which an isolation element comprises at least two materials having different indices of refraction. See English abstract.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Ooka into the device of Haddad et al. to achieve improved reflection efficiency and reabsorbing optical energy. See English abstract.

With respect to claim 36, Haddad et al. fail to teach the range for the relative values of the refractive index.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the range for the relative values of the refractive index through routine experimentation and optimization to obtain optimal or desired device performance because there is no evidence indicating that the range for the relative values of the refractive index is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claim 37, Haddad et al. fail to teach the isolation element comprises of silicon dioxide.

However, the use of silicon dioxide as isolation element is well-known in semiconductor art.

With respect to claim 39, Haddad et al. teach the isolation element extends substantially from the light incident surface to the backside surface of at least one of said two djacent light sensitive pixels.

With respect to claim 40, Haddad et al. fail to teach the isolation element comprises of Al_2O_3.

However, the use of Al_2O_3as isolation element is well-known in semiconductor art.

With respect to claim 41, Haddad et al. fail to teach the isolation element comprises of oxide.

However, the use of oxide as isolation element is well-known in semiconductor art.

With respect to claim 42, if Haddad et al. uses Al_2O_3 as isolation element the isolation element would inherently have a passivating negative charge.

With respect to claim 43, if Haddad et al. uses oxide as isolation element the isolation element would inherently have a surface recombination velocity as low as 10 cm/s

With respect to claim 44, if Haddad et al. uses oxide as isolation element the isolation element would inherently have an index of refraction of less than 2.1.

With respect to claim 45, Haddad et al. fail to teach the isolation element comprises of al oxide and hf oxide.

However, the use of al oxide and hf oxide as isolation element is well-known in semiconductor art.

With respect to claim 46, Haddad et al. teach at least one of said adjacent light sensitive pixels comprises a textured region 60, 18, 40.

With respect to claim 47, Haddad et al. teach said textured region is coupled to the light incident surface.

With respect to claim 48, Haddad et al. teach said light incident surface comprises said textured region.

With respect to claim 49, Haddad et al. teach said textured region comprises a textured film layer.

With respect to claim 51, Haddad et al. teach said backside surface comprises of said textured region.

With respect to claims 50, Haddad et al. fail to teach the trapping or reflecting layer and textured or reflecting layer comprise of a metal layer.

Bour et al. teach using a textured or reflecting layer of metal or Al to enhance or control reflection of incident light. See col. 3, lines 40-50.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Bour et al. into the device of Haddad et al. to achieve light efficiency. See col. 3, lines 40-50.

With respect to claims 63 and 64, how the textured region is formed has not given patentable weight since claimed invention is directed to a device.

With respect to claim 66, Haddad et al. teach said textured region is coupled to said backside surface.

Claims 52, 54-61 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Haddad et al. WO 2011035188 (a reference cited by the applicant) in combination with Ooka (JP407074240) and Bour et al. (US pat 8470619) (reference previously cited).

With respect to claim 52, Haddad et al. teach an imager, comprising (see figs. 1-17, particularly fig. 3 and associated text):

at least two adjacent light sensitive pixels each having a light incident surface, and a backside surface opposite the light incident surface;

a peripheral isolation element separating said at least two adjacent light sensitive pixels so as to reduce optical crosstalk therebetween,;

at least one doped region disposed on at least one of the light incident surface and the backside surface .

Haddad et al. fail to teach the peripheral isolation element comprises at least two materials having different indices of refraction.

Ooka teaches an imager in which an isolation element comprises at least two materials having different indices of refraction. See English abstract.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Ooka into the device of Haddad et al. to achieve improved reflection efficiency and reabsorbing optical energy. See English abstract.

With respect to claim 54, Haddad et al. teach at least one of said light incident surface and said backside surface of at least one of said two adjacent light sensitive pixels comprises a textured region.

With respect to claim 55, Haddad et al. teach said textured region is a textured film layer.

With respect to claim 56, Haddad et al. fail to teach the trapping or reflecting layer and textured or reflecting layer comprise of a metal layer.

Bour et al. teach using a textured or reflecting layer of metal or Al to enhance or control reflection of incident light. See col. 3, lines 40-50.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Bour et al. into the device of Haddad et al. to achieve light efficiency. See col. 3, lines 40-50.

With respect to claim 57, Haddad et al. teach said textured region reflects at least a portion of light internally incident thereon into the pixel.

With respect to claim 58, Haddad et al. teach the isolation element extends from the light incident surface to the backside surface of at least onf of said two adjacent light sensitive pixels.

With respect to claim 59, Haddad et al. fail to teach the isolation element comprises of al oxide and hf oxide.

However, the use of al oxide and hf oxide as isolation element is well-known in semiconductor art.

With respect to claim 60, Haddad et al. teach said at least two pixels are formed monolithically in a common semiconductor substrate.

With respect to claim 61, how the textured region is formed has not given patentable weight since claimed invention is directed to a device.

Allowable Subject Matter

Claims 35, 38, and 53 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed 11/13/2017 have been fully considered but they are not persuasive. See above rejection.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LONG PHAM whose telephone

number is (571)272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

/LONG PHAM/
Primary Examiner, Art Unit 2814

Notice of References Cited	Application/Control No. 15/216,244	Applicant(s)/Patent Under Reexamination PRALLE ET AL.	
	Examiner LONG PHAM	Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
	A	US-				
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N	JP407074240	03-1995	JAPAN	OOKA	
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号

特開平7－74240

(43)公開日　平成７年(1995)３月17日

(51)Int.Cl.[6]	識別記号	庁内整理番号	ＦＩ		技術表示箇所
Ｈ０１Ｌ 21/762					
27/12	Ｆ				
31/10					
		9169－4M	Ｈ０１Ｌ 21/ 76	Ｄ	
			31/ 10	Ａ	

審査請求　有　請求項の数２　ＦＤ　（全　３　頁）

(21)出願番号　特願平5－168606

(22)出願日　平成５年(1993)６月15日

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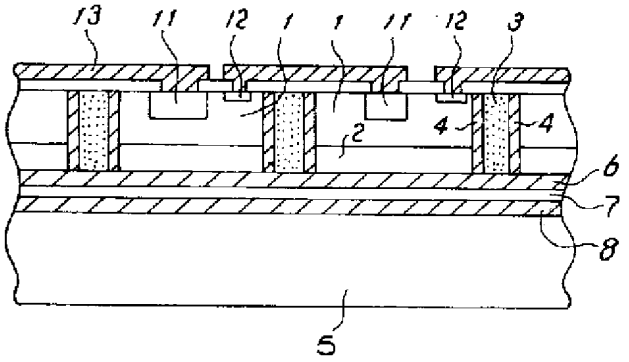
(74)代理人　弁理士　煤孫　耕郎

(54)【発明の名称】　半導体装置

(57)【要約】

【目的】　ＳＯＩ基板を用いたフォトダイオードを形成する場合、光電流を効率良く得るために、絶縁膜の光反射効率を向上させて、光エネルギーの吸収量を高める。

【構成】　ＳＯＩ基板を用いてフォトダイオードを形成し、光エネルギーの吸収効率を高めるために、入射した光を高効率で反射し、再吸収させる。そのために入射光を反射する半導体装置底面の絶縁分離膜を異なる屈折率を持った材質を組み合わせて複合化することで、反射率を高める。



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【特許請求の範囲】
【請求項１】　単結晶シリコン基板と、前記単結晶シリコン基板の一表面上に設けられた複合絶縁膜と、前記複合絶縁膜上に設けられた単結晶シリコン層と、側面を接して設けられた絶縁膜と、前記絶縁膜間を充填する多結晶シリコン層とを有することを特徴とする半導体装置。
【請求項２】　複合絶縁膜が異なる材質の２種類以上の絶縁膜で構成されることを特徴とする請求項１に記載の半導体装置。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明はＳＯＩ基板を用いた半導体装置に関し、特にフォトダイオードに関する。
【０００２】
【従来の技術】従来のフォトダイオード半導体装置は、図２に示すように、多結晶シリコン２１を支持体として、ダイオード素子１つ１つを絶縁分離する酸化膜２２で単結晶シリコン層１を取り囲んだ誘電体分離構造を有している。これはダイオード素子を直列に直接し、高い起電力を得るため、ダイオード素子領域１つ１つを分離する必要があるためである。この従来の誘電体分離構造は、４００μｍ程度の厚い多結晶シリコンを有しているため、コストが高くなる、基板の反りが大きくなるなどの問題があった。
【０００３】これらの問題を解決するために、図３に示すような特開平３－１８００７０号や特開平３－１３６３４６号などによるＳＯＩ基板を用いたものが、提案されている。ここでフォトダイオード素子１つ１つの光電流を高めるために、光結合するキャリアの総量を多くする必要があり、各フォトダイオード素子領域のシリコン層厚さ１を厚くすることで対応している。図２に示す誘電体分離基板では、シリコン層１の厚さを厚くすることは容易であるが、図３に示すＳＯＩ基板はシリコン層１の厚さを厚くすると絶縁分離領域３及び４の形成が困難になるため、シリコン層１厚さを薄くしても、起電力を高めることができるように、特開昭６３－１３２４６０号に示されるように、シリコン層１と絶縁膜３１との界面に高不純物濃度層２を設けていた。
【０００４】
【発明が解決しようとする課題】この従来のＳＯＩ基板では、シリコン層が薄いため、絶縁膜を光が透過しやすく、起電効率を高めるために高不純物濃度層を形成しても、あまり起電効率が上らないという問題があった。
【０００５】
【課題を解決するための手段】本発明は、単結晶シリコン基板と、前記単結晶シリコン基板の一表面上に設けられた複合絶縁膜と、前記複合絶縁膜上に設けられた単結晶シリコン層と、側面を接して設けられた絶縁膜と、前記絶縁膜間を充填する多結晶シリコン層とを有する半導体装置である。

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【０００６】
【作用】本発明においては、ＳＯＩ基板を用いた半導体装置は、フォトダイオードを形成するシリコン層と、各ダイオードを分離する絶縁領域と、光反射効率を高める複合絶縁膜と、シリコン層底部に設けられた高濃度不純物層と、支持基板となるシリコン基板とを備えており、シリコン層の表面上から光を受け、シリコン層（シリコン単結晶領域）を透過してＰ－Ｎ接合境界付近で吸収された光エネルギーは光電流となり、残りの光エネルギーは透過して複合絶縁膜に到達する。複合絶縁膜は、光エネルギーを高効率で反射し、再びＰ－Ｎ接合に達して、光電流に変換されるという作用をするものである。
【０００７】
【実施例】次に本発明の実施例について、図面を参照して説明する。図１は、本発明の一実施例の半導体装置の断面図である。支持体となる単結晶基板５上に絶縁酸化膜６及び８と窒化膜７で形成された複合絶縁膜上に、フォトダイオードを形成するシリコン単結晶領域１及び高濃度不純物層２が形成されており、各光フォトダイオード素子は、絶縁酸化膜４と、多結晶シリコン層３とで絶縁されている。シリコン単結晶領域１上には、アーノード１１、カソード１２を有するフォトダイオードが形成され、アルミ電極１３で各フォトダイオードは直列に接続されている。シリコン単結晶領域１の表面上から光を受け、シリコン層を透過してＰ－Ｎ接合境界付近で吸収された光エネルギーは、光電流となり、残りの光エネルギーは透過して複合絶縁膜に到達する。複合絶縁膜は、光エネルギーを高効率で反射し、再びＰ－Ｎ接合に達して、光電流に変換される。
【０００８】複合絶縁膜は、光エネルギーを効率的に反射するために、絶縁酸化膜６～８の材質、厚さを入射光の波長合わせ変更を行う。例えば、第１の実施例においては絶縁酸化膜６及び８の膜厚を１．０μｍ、絶縁膜７は、シリコン窒化膜０．１μｍを用い、第２の実施例では、絶縁酸化膜６及び８は２．０μｍを用い、絶縁膜７を多結晶シリコン膜０．１μｍを用いるなどである。第２の実施例は第１の実施例と構造は同じでものである。
【０００９】
【発明の効果】以上説明したように、本発明は、絶縁分離膜を異なった屈折率を持った材質のものを組み合わせて複合化し構成することにより、入射光の反射効率を高めて光エネルギーを再吸収させ、エネルギー変換効率を向上させることができる。
【図面の簡単な説明】
【図１】本発明の一実施例の断面図
【図２】従来の誘電体分離基板の半導体装置の断面図
【図３】従来のＳＯＩ基板の半導体装置の断面図
【符号の説明】
１　単結晶シリコン層
２　高濃度不純物層

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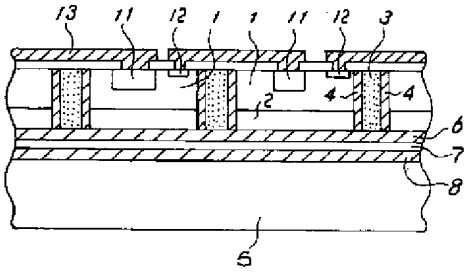
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３　多結晶シリコン層
４　絶縁酸化膜
５　単結晶シリコン基板
６　絶縁酸化膜
７　絶縁膜
８　絶縁酸化膜

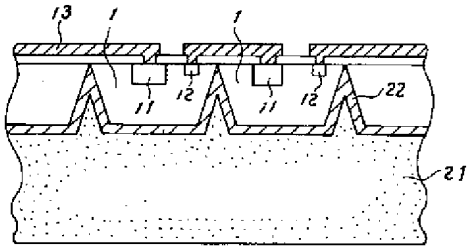
４

１１　アノード
１２　カソード
１３　アルミ電極
２１　多結晶シリコン層
２２　絶縁酸化膜
３１　絶縁酸化膜

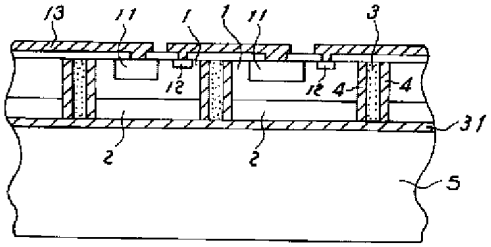
【図１】



【図２】



【図３】



SAMSUNG EX. 1002 - 2383/2862

PAT-NO: JP407074240A

DOCUMENT-IDENTIFIER: JP 07074240 A

TITLE: SEMICONDUCTOR DEVICE

PUBN-DATE: March 17, 1995

INVENTOR-INFORMATION:

NAME	COUNTRY
OOKA, TSUKASA	

ASSIGNEE-INFORMATION:

NAME	COUNTRY
NEC CORP	N/A

APPL-NO: JP05168606

APPL-DATE: June 15, 1993

INT-CL (IPC): H01L021/762 , H01L027/12 , H01L031/10

ABSTRACT:

PURPOSE: To enhance energy conversion efficiency by composing a dielectric isolation film of a combination materials having different refractive index thereby enhancing the reflection efficiency of incident light and reabsorbing the optical energy.

CONSTITUTION: A silicon single crystal region 1 for forming a photodiode and a heavily doped impurity layer 2 are formed on a composite insulation film of oxide 6 and nitride 7 deposited on a single crystal substrate 5. Each photodiode element is isolated by an oxide 4 and polysilicon layer 3 and photodiodes, each having an anode 11 and a cathode 12, are formed on the silicon single crystal region 1 and connected in series through an Al electrode 13. A light impinging on the surface of the silicon single crystal region 1 passes through the silicon layer and reaches the composite insulation film with the energy thereof being absorbed in the vicinity of the P-N junction. The optical energy is reflected on the composite insulation film with high efficiency reaches again at the P-N junction where the optical energy is converted into an optoelectric current.

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Attorney Docket Number	143705.05221

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5236863		1993-08-17	Iranmesh	
	2	5410168		1995-04-25	Hisa	
	3	8076746		2011-12-13	McCarten et al.	
	4	9419159		2016-08-16	Sakamoto et al.	
	5	9673250		2017-06-06		

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20040256561		2004-12-23	Beuhler et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	Long Pham
	Attorney Docket Number	143705.05221

	2	20070063219		2007-03-22	Sa'ar et al.	
	3	20070103580		2007-05-10	Noto	
	4	20070125951		2007-06-07	Snider et al.	
	5	20080142686		2008-06-19	Konno et al.	
	6	20090009596		2009-01-08	Kerr et al.	
	7	20090174026		2009-07-09	Carey et al.	
	8	20090242019		2009-10-01	Ramamoorthy et al.	
	9	20100102366		2010-04-29	Lee et al.	
	10	20110003424		2011-01-06	De Ceuster et al.	
	11	20110019050		2011-01-27	Yamashita	
	12	20120080733		2012-04-05	Doan et al.	

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	Application Number	15216244
	Filing Date	2016-07-21
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	Art Unit	2814
	Examiner Name	Long Pham
	Attorney Docket Number	143705.05221

	13	20120274744		2012-11-01	Wan	
	14	20140352779		2014-14-04	Smirnov et al.	
	15	20150076468		2015-03-19	Yamaguchi et al.	

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	200627675	TW		2006-08-01	Lumileds Lighting US LLC		
	2	200818529	TW		2008-04-16	Newsouth Innovations		

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Campbell, Stephen A., "The Science and Engineering of Microeletronic Fabrication, 2nd Ed.", Oxford University Press, 2001, pp. 406-411.	
	2	Ohring, Milton." The Materials of Science of Thin Films"; pp.176-179; Academic Press, 1992.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Attorney Docket Number	143705.05221

EXAMINER SIGNATURE

Examiner Signature	/LONG PHAM/	Date Considered	02/15/2018

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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SAMSUNG EX. 1002 - 2389/2862

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Attorney Docket Number	143705.05221

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Reza Mollaaghababa/	Date (YYYY-MM-DD)	2017-11-13
Name/Print	Reza Mollaaghababa	Registration Number	43810

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15216244	PRALLE ET AL.
	Examiner	**Art Unit**
	LONG PHAM	2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/07/2016	02/06/2017	06/10/2017	02/15/2018					
	34	÷	✓	✓	✓					
	35	÷	✓	✓	O					
	36	÷	✓	✓	✓					
	37	÷	✓	✓	✓					
	38	÷	✓	✓	O					
	39	÷	✓	✓	✓					
	40	÷	✓	✓	✓					
	41	÷	✓	✓	✓					
	42	÷	✓	✓	✓					
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	62		O	-						
	63		✓	✓	✓					
	64		✓	✓	✓					
	65		O	-						
	66			✓	-					
	67				✓					

SAMSUNG EX. 1002 - 2392/2862

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	20	("20040256561" | "20070063219" | "20070103580" | "20070125951" | "20080142686" | "20090009596" | "20090174026" | "20090242019" | "20100102366" | "20110003424" | "20110019050" | "20120080733" | "20120274744" | "20140352779" | "20150076468" | "5236863" | "5410168" | "8076746" | "9419159" | "9673250").PN.	US-PGPUB; USPAT	OR	ON	2018/02/15 10:41
L2	24107	(layer or film) near3 (different near2 (refractive or refraction or refracting))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:45
L3	18	2 near4 isolation	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:45
L4	5	3 same4 (pixel or pixels)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:45
L5	13	3 not 4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:47
L6	22683	bragg adj2 (reflective or reflector)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:51
L7	58	6 near4 isolation	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2018/02/15 10:52

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			IBM_TDB			
L8	6	7 same4 (pixel or pixels)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:52
L9	52	7 not 8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:55
L10	29452	(isolation or isolating or insulation or insulating) near2 (multi-layer or multiple)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:57
L11	19	10 near10 (different near2 (refractive or refraction or refracting))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:58
L12	48	10 near3 (silicon adj2 dioxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 13:05
L13	1	12 same4 (pixel or pixels)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 13:05
L14	19531	(isolation or isolating or insulation or insulating) near2 (silicon adj2 dioxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 13:08
L15	53	14 near4 (benefit or advantage or beneficial or advantageous)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 13:08
L16	4006	(isolation or isolating or insulation or insulating) near2 ("Al.sub.2O.sub.3")	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2018/02/15 13:10

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			EPO; JPO; DERWENT; IBM_TDB			
L17	450872	aluminum adj oxide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 13:11
L18	57928	hafnium adj oxide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 13:11
L19	2014	(isolation or isolating or insulation or insulating) near6 17 near6 18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 13:11
S2	84	US-3035052-$.DID. OR US-20030029495-$.DID. OR US-20040222187-$.DID. OR US-20050127401-$.DID. OR US-20050227390-$.DID. OR US-20060011955-$.DID. OR US-20060079062-$.DID. OR US-20060118781-$.DID. OR US-20060180885-$.DID. OR US-20060231914-$.DID. OR US-20070145505-$.DID. OR US-20080026550-$.DID. OR US-20080036022-$.DID. OR US-20080044943-$.DID. OR US-20080076240-$.DID. OR US-20080099804-$.DID. OR US-20080178932-$.DID. OR US-20080258604-$.DID. OR US-20090065051-$.DID. OR US-20090142879-$.DID. OR US-20090160983-$.DID. OR US-20090194671-$.DID. OR US-20090200586-$.DID. OR US-20090213883-$.DID. OR US-3487223-$.DID. OR US-4277793-$.DID. OR US-4419533-$.DID. OR US-4493942-$.DID. OR US-4514582-$.DID. OR US-4536608-$.DID. OR US-4663188-$.DID. OR US-4829013-$.DID. OR US-5080725-$.DID. OR US-5081049-$.DID. OR US-5100478-$.DID. OR US-5114876-$.DID. OR US-5164324-$.DID. OR US-5322988-$.DID. OR US-5346850-$.DID. OR US-5597621-$.DID. OR US-5714404-$.DID. OR US-5731213-$.DID. OR US-5792280-$.DID. OR US-6147297-$.DID. OR US-6498336-$.DID. OR US-6580053-$.DID. OR US-6583936-$.DID. OR US-6667528-$.DID. OR US-6759262-$.DID. OR US-6800541-	US-PGPUB; USPAT; USOCR; JPO; IBM_TDB	OR	ON	2014/06/25 14:14

SAMSUNG EX. 1002 - 2395/2862

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S3	7768	(light adj2 (trapping or trapped))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 14:16
S4	11	S2 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 14:16
S5	2251	(reflector or Bragg) and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:40
S6	14	(reflector or Bragg) and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:41
S7	888	(reflector or Bragg) near3 backside	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:55
S8	51623	(reflector or Bragg) near3 (side or	US-PGPUB;	OR	ON	2014/06/25

SAMSUNG EX. 1002 - 2396/2862

		sidewall or edge or wall)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			15:55
S9	112640	pixel near5 (side or sidewall or edge or wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:56
S10	143	S7 same S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:56
S11	2	S9 same4 S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:56
S12	3	S9 and S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:57
S13	1	S12 not S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:57
S14	179	S7 same4 S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:58
S15	145	S14 and (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:59
S16	129	S14 same10 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2014/06/25 15:59

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			IBM_TDB			
S17	128	S14 same8 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:59
S18	1204	(reflector or Bragg) near5 backside	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S19	71202	(reflector or Bragg) near5 (side or sidewall or edge or wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S20	280	S18 same4 S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S21	195	S20 same4 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S22	7	S18 same2 S9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:10
S23	7	S22 same4 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:10
S24	217	S18 same S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:13
S25	0	(light adj2 sensitive adj2 pixel) same4 S24	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2014/06/25 16:14

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			EPO; JPO; DERWENT; IBM_TDB			
S26	0	(light adj2 sensitive adj2 pixel) and S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:14
S27	14	pixel same4 S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:14
S28	7	S27 and index	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:18
S29	26925	(high adj2 index) near3 (layer or film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:48
S30	27823	(low adj2 index) near3 (layer or film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:48
S31	12802	S29 near10 S30	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:48
S32	1170	(reflector or Bragg) same S31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:49
S33	611	(reflector or Bragg) near10 S31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:49
S34	4200	S30 near5 ("between")	US-PGPUB; USPAT;	OR	ON	2014/06/26 12:49

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			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S35	1972	S34 near10 S29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:50
S36	81	(reflector or Bragg) near10 S35	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:50
S37	188	S29 near5 (polysilicon or polycrystalline or poly or (amorphous adj2 silicon) or germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:53
S38	2500	S30 near5 (oxide or nitride or oxynitride or oxynitrides)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:53
S39	14	S37 near20 S38	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:53
S40	0	(reflector or Bragg) same S39	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:54
S41	0	S39 near20 ("between")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:54
S42	51	backside near6 (textured near2 (layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:12

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S43	10	S42 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:25
S44	5	S39 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:25
S45	2	S36 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:25

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S46	1	("20140138785").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:26
S47	3930	(257/432).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:54
S48	218	(257/228).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:54
S50	1	("9373732").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/07/13 15:10
S51	1	("9373732").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/07/15 10:13
S52	395	reflective near3 (aluminum adj oxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/15 13:07
S53	35214	(rough or textured) near2 (layer or film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:24
S54	44833	light adj2 incident adj2 surface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:24
S55	38	S53 same S54	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:25
S56	10	S55 same efficiency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:25
S57	0	S55 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:29
S58	0	S55 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN")	US-PGPUB; USPAT; USOCR;	OR	ON	2017/02/06 01:30

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			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S59	3	S55 same (metal or polysilicon or amorphous)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:30
S60	1864	S53 same efficiency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:32
S61	42	S60 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:32
S62	351	S60 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN" or metal or polysilicon or amorphous)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:32
S63	85	S62 same4 incident	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:33
S64	228102	(reflective near2 (material or layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:11
S65	530599	("AlO" or (aluminum adj oxide)) or ("HfO" or (hafnium adj oxide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:12
S66	403	S64 near3 S65	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:12
S67	2	S66 near4 (benefit or beneficial or	US-PGPUB;	OR	ON	2017/02/06

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		advantages or advantageous or advantegeously)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:13
S68	2	S66 near10 (benefit or beneficial or advantages or advantageous or advantegeously)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:13
S69	31128	(anti or non) near2 S64	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:20
S70	121	S65 near4 S69	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:20
S71	2	S70 same (benefit or beneficial or advantages or advantageous or advantegeously)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:20
S72	2	(dope or doping or implanting or implant or implants implantation or dopes) near2 (light adj incident adj surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:04
S73	6	(dope or doping or implanting or implant or implants implantation or dopes) near2 (light adj2 incident adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:05
S74	13	(dope or doping or implanting or implant or implants implantation or dopes) near4 (light adj2 incident adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:05
S75	167141	(doped or implanted) adj2 (region or section or portion or part)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2017/02/06 12:13

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			IBM_TDB			
S76	1	S75 near4 (light adj2 incident adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:13
S77	26	S75 near10 (light adj2 incident adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:15
S78	25	S77 not S76	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:15
S79	1	("9064764").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/02/06 12:20
S80	44833	(light adj2 incident adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 17:49
S81	167141	(doped or implanted) adj2 (region or section or portion or part)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 17:49
S82	9	S80 near6 S81	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 17:49
S83	364064	(light adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 17:50
S84	54	S83 near4 S81	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 17:50

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S85	53	S84 not S82	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 17:50
S86	21	("20030214595" | "20030228883" | "20050093100" | "20060086956" | "20060128087" | "20070189583" | "20070237504" | "20080158398" | "20080192133" | "20080284884" | "20100200658" | "20110194100" | "20110292380" | "20140198240" | "5101260" | "5600130" | "5626687" | "5635089" | "6082858" | "6204506" | "6907135").PN.	US-PGPUB; USPAT	OR	ON	2017/02/07 07:43
S87	21	("20030214595" | "20030228883" | "20050093100" | "20060086956" | "20060128087" | "20070189583" | "20070237504" | "20080158398" | "20080192133" | "20080284884" | "20100200658" | "20110194100" | "20110292380" | "20140198240" | "5101260" | "5600130" | "5626687" | "5635089" | "6082858" | "6204506" | "6907135").PN.	US-PGPUB; USPAT	OR	ON	2017/02/07 07:44
S88	20	("20010044266" | "20050088634" | "20080173620" | "20090027640" | "20090093100" | "20090114630" | "20090308457" | "20100140768" | "20130135439" | "4886958" | "5351446" | "5641969" | "5727096" | "6327022" | "6331885" | "6340281" | "7800684" | "7897942" | "9184204" | "9369641").PN.	US-PGPUB; USPAT	OR	ON	2017/06/01 13:32

2/ 15/ 2018 2:07:49 PM
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PTO/SB/30EFS (02-18)
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	15/216,244	Filing Date	2016-07-21	Docket Number (if applicable)	143705.05221	Art Unit	2814
First Named Inventor	Martin U. Pralle			Examiner Name	Pham, Long		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 500436

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

Applicant Signature

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
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Signature of Registered U.S. Patent Practitioner			
Signature	/Reza Mollaaghababa/	Date (YYYY-MM-DD)	2018-08-01
Name	Reza Mollaaghababa	Registration Number	43810

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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REMARKS

Applicants amend claims 34, 36, 38, 42-45, 52, 57, 58 and add new claims 68-121 as indicated above. Support for the amendments and the new claims can be found, e.g., at paragraphs [0013], [0014], [0036], [0037], [0039], [0041], [0046], [0053], [0054], [0058], [0060], [0064] of the U.S. published application.

Allowable Subject Matter

Claims 35, 38, and 53 are deemed allowable if rewritten in independent form including all limitations of the base claim and any intervening claims.

The original claim 35 depends on independent claim 34. As indicated above, claim 34 is amended to incorporate the features of claim 35, and claim 35 is canceled. Claim 34 is further amended to recite that the at least two adjacent light sensitive pixels are *image sensor* pixels in order to further clarify that claim 34 is directed to an *imager* device.

Accordingly, claim 34 is believed to be in condition for allowance. Further, claim 38 depends on claim 34 and hence is also in condition for allowance at least because of its dependence on claim 34.

The original claim 53 depends on independent claim 52. Claim 52 is amended to incorporate the features of claim 53. In addition, similar to claim 34, claim 52 is amended to emphasize that the two adjacent light sensitive pixels are *image sensor* pixels.

Thus, claim 52 is believed to be in condition for allowance.

Rejections Pursuant to 35 U.S.C. §103

I. Claims 34, 36, and 39-51 are rejected as being unpatentable over Haddad et al. (WO 2011035188) in combination with Ooka (JP407074240) and Bour et al. (U.S. Patent No. 8,470,619).

As discussed above, claim 34 is amended to incorporate the features of allowable claim 35. Thus, claim 34 is believed to be in condition for allowance. Claims 36 and 39-51 depend, either directly or indirectly, on claim 34 and hence are also in condition for allowance and their rejection over the combination of Haddad, Ooka and Bour is moot.

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II. Claims 52, 54-61 are rejected as being unpatentable over Haddad in combination with Ooka and Bour.

As discussed above, claim 52 is amended to incorporate the features of allowable claim 53. Thus, claim 52 and claims 54-61, which depend directly or indirectly, on claim 52 are in condition for allowance and their rejections over the combination of Haddad, Ooka and Bour is moot.

New Claims

New claims 68, 69, 70, 71, 76-82, 90-95, 102-107, 114-115, and 118-119 depend, either directly or indirectly, on claim 34 and hence are in condition for allowance at least for the reasons provided above in connection with claim 34. And new claims 72-75, 83-88, 96-101, 108-113, 116-117, and 120-121 depend, either directly or indirectly, on independent claim 52 and hence are in condition for allowance at least for the reasons provided above in connection with claim 52.

CONCLUSION

In view of the above amendments and remarks, Applicants respectfully request allowance of the application. The Examiner is invited to call the undersigned if there are any questions.

The Director is authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 50-0436, under Docket No. 143705.05221.

Dated: August 1, 2018

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AMENDMENTS TO THE CLAIMS

1-33. (Canceled)

34. (Currently Amended) An imager device, comprising:

at least two adjacent light sensitive image sensor pixels each having a light incident surface, and a backside surface opposite the light incident surface;

a peripheral isolation element at least partially separating said two adjacent light sensitive pixels;

each of said pixels having at least one doped region disposed on at least one of the light incident surface and the backside surface,

wherein the peripheral isolation element comprises at least two materials having different indices of refraction,

wherein said peripheral isolation element comprises a first, a second and a third layer, wherein said third layer is disposed between said first and second layers, and wherein each of said first and second layer exhibits an index of refraction less than an index of refraction of said third layer.

35. (Canceled)

36. (Currently Amended) The device of claim 34, wherein the index of refraction of at least one of said first and second layer is at least 0.2 lower relative to the refractive index of the third layer.

37. (Previously Presented) The device of claim 34, wherein at least of one of said at least two materials comprises silicon dioxide.

38. (Currently Amended) The device of claim 34 ~~35~~, wherein at least one of said first and second layers comprises silicon dioxide.

39. (Previously Presented) The device of claim 34, wherein the isolation element extends substantially from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels.

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40. (Previously Presented) The device of claim 34, wherein at least one of the first and second layer comprises Al_2O_3.

41. (Previously Presented) The device of claim 34, wherein said peripheral isolation element comprises an oxide.

42. (Currently Amended) The device of claim 34, wherein said peripheral isolation element provides a passivating negative charge.

43. (Currently Amended) The device of claim 34, wherein said peripheral isolation element exhibits a surface recombination velocity as low as 10 cm/s.

44. (Currently Amended) The device of claim 34, wherein the peripheral isolation element comprises at least one material having an index of refraction of less than about 2.1.

45. (Currently Amended) The device of claim 34, wherein the peripheral isolation element comprises any of aluminum oxide and hafnium oxide.

46. (Previously Presented) The device of claim 34, wherein at least one of said two adjacent light sensitive pixels comprises a textured region.

47. (Previously Presented) The device of claim 46, wherein said textured region is coupled to the light incident surface.

48. (Previously Presented) The device of claim 47, wherein said light incident surface comprises said textured region.

49. (Previously Presented) The device of claim 47, wherein said textured region comprises a textured film layer.

50. (Previously Presented) The device of claim 49, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.

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51. (Previously Presented) The device of claim 46, wherein said backside surface comprises said textured region.

52. (Currently Amended) An imager device, comprising:

at least two adjacent light sensitive image sensor pixels each having a light incident surface, and a backside surface opposite the light incident surface;

a peripheral isolation element separating said at least two adjacent light sensitive pixels so as to reduce optical crosstalk therebetween, said isolation element comprising at least two materials having different indices of refraction,

at least one doped region disposed on at least one of the light incident surface and the backside surface,

wherein said peripheral isolation element comprises a first, a second and a third layer, wherein said third layer is disposed between said first and second layers, and wherein each of said first and second layers exhibits an index of refraction less than an index of refraction of said third layer.

53. (Canceled)

54. (Previously Presented) The device of claim 52, wherein at least one of said light incident surface and said backside surface of at least one of said two adjacent light sensitive pixels comprises a textured region.

55. (Previously Presented) The device of claim 54, wherein said textured region is a textured film layer.

56. (Previously Presented) The device of claim 55, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.

57. (Currently Amended) The device of claim 54, wherein said textured region reflects at least a portion of light internally incident thereon into the at least one pixel.

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58. (Currently Amended) The device of claim 52, wherein the peripheral isolation element extends from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels.

59. (Previously Presented) The device of claim 52, wherein said at least two materials comprises silicon dioxide and aluminum oxide.

60. (Previously Presented) The device of claim 54, wherein said at least two pixels are formed monolithically in a common semiconductor substrate.

61. (Previously Presented) The device of claim 54, wherein the textured region is formed by laser radiation.

62. (Canceled)

63. (Previously Presented) The device of claim 46, wherein the textured region is formed by one of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.

64. (Previously Presented) The device of claim 46, wherein the textured region is formed by laser radiation.

65. (Canceled)

66. (Canceled)

67. (Previously Presented) The device of claim 46, wherein said textured region is coupled to the backside surface.

68. (New) The device of claim 34, wherein said peripheral isolation element comprises tantalum oxide.

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69. (New) The device of claim 68, wherein said tantalum oxide comprises tantalum aluminum oxynitride.

70. (New) The device of claim 34, wherein said peripheral isolation element comprises lanthanum oxide.

71. (New) The device of claim 70, wherein said lanthanum oxide comprises lanthanum aluminum oxide.

72. (New) The device of claim 52, wherein said peripheral isolation element comprises tantalum oxide.

73. (New) The device of claim 72, wherein said tantalum oxide comprises tantalum aluminum oxynitride.

74. (New) The device of claim 52, wherein said peripheral isolation element comprises lanthanum oxide.

75. (New) The device of claim 74, wherein said lanthanum oxide comprises lanthanum aluminum oxide.

76. (New) The device of claim 34, wherein each of said at least two adjacent light sensitive image sensor pixels comprises a semiconductor portion providing said light incident surface and said backside surface, wherein said peripheral isolation element isolates the semiconductor portions of said at least two adjacent light sensitive image sensor pixels.

77. (New) The device of claim 76, wherein said peripheral isolation element optically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.

78. (New) The device of claim 76, wherein said peripheral isolation element electrically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.

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79. (New) The device of claim 76, wherein an index of refraction of the semiconductor portion of each of said at least two adjacent image sensor pixels is different from indices of refraction of said layers of the peripheral isolation element such that light incident from each of said semiconductor portions on said peripheral isolation element is reflected, thereby providing optical isolation between the pixels.

80. (New) The device of claim 34, wherein said at least two adjacent light sensitive image sensor pixels are formed monolithically on a common semiconductor substrate and are isolated from one another by said peripheral isolation element.

81. (New) The device of claim 34, wherein said peripheral isolation element is a trench isolation element.

82. (New) The device of claim 34, wherein said peripheral isolation element has a width in a range from about 100 nm to about 50 microns.

83. (New) The device of claim 52, wherein each of said at least two adjacent light sensitive image sensor pixels comprises a semiconductor portion providing said light incident surface and said backside surface, wherein said peripheral isolation element isolates the semiconductor portions of said at least two adjacent light sensitive image sensor pixels.

84. (New) The device of claim 83, wherein said peripheral isolation element optically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.

85. (New) The device of claim 84, wherein said peripheral isolation element electrically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.

86. (New) The device of claim 85, wherein an index of refraction of the semiconductor portion of each of said at least two adjacent image sensor pixels is different from indices of refraction of said layers of the peripheral isolation element such that light incident from each of

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said semiconductor portions on said peripheral isolation element is reflected, thereby providing optical isolation between the pixels.

87. (New) The device of claim 52, wherein said at least two adjacent light sensitive image sensor pixels are formed monolithically on a common semiconductor substrate and are isolated from one another by said peripheral isolation element.

88. (New) The device of claim 52, wherein said peripheral isolation element is a trench isolation element.

89. (New) The device of claim 52, wherein said peripheral isolation element has a width in a range from about 100 nm to about 50 microns.

90. (New) The imager device of claim 76 , wherein at least one of the first layer and the second layer of said peripheral isolation element and said semiconductor portion of each of said at least two adjacent pixels comprise different materials.

91. (New) The imager device of claim 34, wherein the first layer and the second layer of said peripheral isolation element comprise different materials .

92. (New) The imager device of claim 34, wherein the peripheral isolation element comprises at least three materials.

93. (New) The imager device of claim 34, wherein the peripheral isolation element comprises more than three layers.

94. (New) The imager device of claim 34, wherein the peripheral isolation element comprises a light trapping material filling a trench.

95. (New) The imager device of claim 94, wherein the trench is one of a shallow trench and a deep trench.

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96. (New) The imager device of claim 83, wherein at least one of the first layer and the second layer of the peripheral isolation element and said semiconductor portion of each of said at least two adjacent pixels comprise different materials.

97. (New) The imager device of claim 52, wherein the first layer and the second layer of said peripheral isolation element comprise different materials.

98. (New) The imager device of claim 52, wherein the peripheral isolation element comprises at least three materials.

99. (New) The imager device of claim 52, wherein the peripheral isolation element comprises more than three layers.

100. (New) The imager device of claim 52, wherein the peripheral isolation element comprises a light trapping material filling a trench.

101. (New) The imager device of claim 100, wherein the trench is one of a shallow trench and a deep trench.

102. (New) The imager device of claim 34, wherein said peripheral isolation element comprises a trench isolation element formed by filling a trench with said first, said second, and said third layers.

103. (New) The imager device of claim 102, wherein said trench isolation element has a depth in a range of about 100 nm to about 50 microns.

104. (New) The imager device of claim 103, wherein said trench isolation element has a width in a range of about 100 nm to about 10 microns.

105. (New) The imager device of claim 34, wherein said peripheral isolation element is configured to reflect at least a portion of light incident thereon from any of said two adjacent light sensitive pixels back to that pixel.

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106. (New) The imager device of claim 105, wherein the peripheral isolation element is further configured to optically isolate said two adjacent light sensitive pixels.

107. (New) The imager device of claim 106, wherein the peripheral isolation element is further configured to electrically isolate said two adjacent light sensitive pixels.

108. (New) The imager device of claim 52, wherein said peripheral isolation element comprises a trench isolation element formed by filling a trench with said first, said second, and said third layers.

109. (New) The imager device of claim 108, wherein said trench isolation element has a depth in a range of about 100 nm to about 50 microns.

110. (New) The imager device of claim 109, wherein said trench isolation element has a width in a range of about 100 nm to about 10 microns.

111. (New) The imager device of claim 52, wherein said peripheral isolation element is configured to reflect at least a portion of light incident thereon from any of said two adjacent light sensitive pixels back to that pixel.

112. (New) The imager device of claim 111, wherein the peripheral isolation element is further configured to optically isolate said two adjacent light sensitive pixels.

113. (New) The imager device of claim 112, wherein the peripheral isolation element is further configured to electrically isolate said two adjacent light sensitive pixels.

114. (New) The imager device of claim 34, wherein the peripheral isolation element comprises a textured region.

115. (New) The imager device of claim 34, wherein the peripheral isolation element further comprises a first textured region between the first layer and one of said adjacent pixels and a second textured region between the second layer and the other one of said adjacent pixels.

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116. (New) The imager device of claim 52, wherein the peripheral isolation element comprises a textured region.

117. (New) The imager device of claim 52, wherein the peripheral isolation element further comprises a first textured region between the first layer and one of said adjacent pixels and a second textured region between the second layer and the other one of said adjacent pixels.

118. (New) The imager device of claim 34, wherein the peripheral isolation element comprises five layers.

119. (New) The imager device of claim 118, wherein the five layers include the first layer, the second layer, the third layer, a fourth layer disposed between the first layer and one of said adjacent pixels and a fifth layer disposed between the second layer and the other one of said adjacent pixels.

120. (New) The imager device of claim 52, wherein the peripheral isolation element comprises five layers.

121. (New) The imager device of claim 120, wherein the five layers include the first layer, the second layer, the third layer, a fourth layer disposed between the first layer and one of said adjacent pixels and a fifth layer disposed between the second layer and the other one of said adjacent pixels.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Martin U. Pralle Application No.: 15/216,244 Filed: July 21, 2016 For: PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS	Confirmation No.: 5052 Art Unit: 2814 Examiner: Pham, Long

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Certificate of Mailing

I hereby certify that this correspondence is being electronically filed via EFS-Web to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

August 1, 2018 (Dated) — Electronic Signature: /Reza Mollaaghababa/ (Reza Mollaaghababa, Reg. No. 43,810)

RESPONSE TO FINAL OFFICE ACTION

Dear Sir:

This paper is filed in response to the final Office Action dated February 22, 2018.

Amendments to the Claims begin on page 2.

Remarks begin on page 12.

Electronic Patent Application Fee Transmittal

Application Number:	15216244
Filing Date:	21-Jul-2016
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Filer:	Reza Mollaaghababa/Irene Gommerstadt
Attorney Docket Number:	143705.05221

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 3 months with $0 paid	1253	1	1400	1400
Miscellaneous:				
RCE- 1ST REQUEST	1801	1	1300	1300
		Total in USD ($)		**2700**

Electronic Acknowledgement Receipt

EFS ID:	33335460
Application Number:	15216244
International Application Number:	
Confirmation Number:	5052
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	136549
Filer:	Reza Mollaaghababa/Irene Gommerstadt
Filer Authorized By:	Reza Mollaaghababa
Attorney Docket Number:	143705.05221
Receipt Date:	01-AUG-2018
Filing Date:	21-JUL-2016
Time Stamp:	11:11:49
Application Type:	Utility under 35 USC 111(a)

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Payment was successfully received in RAM	$2700
RAM confirmation Number	080118INTEFSW11135200
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	1_143705_05221_IDS_Transmittal.pdf	104174 3c997ef4588e6843b8c261406b95dcde44a772fa	no	2
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	2_143705_05221_IDS_sb08_wRCE.pdf	2134296 505a02d3ea29400670b02320f3cc7f34f74be915	no	11
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Information:					
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3	Foreign Reference	1_CN101241923A_US20081912 96A1.pdf	767032 6ea5522a3466bcbb3e8f28c4911ff5e10a3eba20	no	11
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5	Foreign Reference	3_CN101740597A_US2010128161.pdf	772339 0b5431189b97a50f178ace3c4dad26bc57894ce2	no	10
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6	Foreign Reference	4_CN101978498A_US2009200625.pdf	602808 7b6358fa9358d718ecd55ad0fcfe7c187a170ae5	no	10
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7	Foreign Reference	5_CN102270646_w_Trans.pdf	9287155 dfb8aa37a1752ff9aa3fcfdcf81f6fa5bdb1ae16	no	29
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11	Foreign Reference	9_JP2012169530A_w_Trans.pdf	24050452 8f6c80f913843acca27f9c236ae0b2a8982e6ef5	no	94
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12	Foreign Reference	10_JP2012191005A_US2012228473.pdf	473261 6fa90bd1fa2c31252461677281c3e3e0d2467f8f	no	10
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13	Foreign Reference	11_KR20060020400A_w_Trans.pdf	4118885 0a5085d231a16921cc0b6cdf6840cd4742a0036d	no	18
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14	Foreign Reference	12_KR20080014301A_w_Trans.pdf	4757084 739ad4d9907277b71cd834b34113fe916318fce4	no	17
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21	Non Patent Literature	2_Choubey_et_al.pdf	3037275 3261bfcf84afd37a6554d9f9a11cd5877452b00a	no	7
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34	Non Patent Literature	15_Park_2454.pdf	1354989 303da6b3848a23e4419a59d429dcb682cc7d0b77	no	6
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35	Non Patent Literature	16_Yaung_8.pdf	340363 268c30957d82d66a02348acd4c79c864ac269d50	no	4
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36	Non Patent Literature	17_electroiq_com_insights_from_leading_edge_2016.pdf	1013528 796d1c9fcc425e935a0efe08fd875d3fbb6e7cdd	no	6
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38	Non Patent Literature	19_Itonaga_8.pdf	443939 d90dc7ba1e4d8bda0f33ce7a9c6a0bc9165522c1	no	4
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39	Non Patent Literature	20_Minoglou_129.pdf	232674 e78b82857ae0a13d4a35ddf3e7e24da9f7e07e5d	no	3
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Warnings:					
Information:					
41	Request for Continued Examination (RCE)	RCE.pdf	1349985 bc270df465bb993c712724f1f177fdc56a81926b	no	3
Warnings:					
Information:					

42		Response.pdf	182780 40e42d804e62454b3ae5133da5e0b0a833a3ebb4	yes	13

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Applicant Arguments/Remarks Made in an Amendment	12	13
Claims	2	11
Amendment Submitted/Entered with Filing of CPA/RCE	1	1

Warnings:

Information:

43	Fee Worksheet (SB06)	fee-info.pdf	32418 cba98f60d38b5bf6564436ed1c22bbe73836bb54	no	2

Warnings:

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Total Files Size (in bytes):	137742316

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: SiOnyx, LLC. Application No.: 15/216,244 Filed: July 21, 2016 For: Pixel Isolation Elements, Devices and Associated Methods	Confirmation No.: 5052 Art Unit: 2814 Examiner: PHAM, LONG

VIA EFS-WEB
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Certificate of Mailing
I hereby certify that this correspondence is being electronically filed via EFS-Web to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

July 31, 2018 (Dated) — Electronic Signature: /Reza Mollaaghababa/
Reza Mollaaghababa, Reg. No. 43,810

INFORMATION DISCLOSURE STATEMENT (IDS) TRANSMITTAL LETTER

Dear Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached substitute for PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed concurrent with the filing of a request for continued examination (37 CFR 1.97(b)(4)). A certification statement pursuant to 37 C.F.R. 1.97(e) is not submitted herewith.

In accordance with 37 CFR 1.98(a)(2)(ii), Applicant has not submitted copies of U.S. patents and U.S. patent applications. Applicant submits herewith copies of foreign patents and non-patent literature in accordance with 37 CFR 1.98(a)(2) and (d) that were not previously

provided in U.S. App. No. 14/747,875 (filed June 23, 2015) and 13/841,120 (filed March 15, 2013), to which the instant application claims priority as a continuation.

In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in § 1.56 (b).

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 50-0436, under Order No. 143705.05221.

Respectfully submitted,

Dated: July 31, 2018

/Reza Mollaaghababa/
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SAMSUNG EX. 1002 - 2434/2862

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	PHAM, LONG
Attorney Docket Number	143705.05221

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4546945		1985-10-15	Nessfield	
	2	5583704		1996-12-10	Fujii	
	3	5802091		1998-08-01	Chakrabarti et al	
	4	6131511		2000-10-17	Wachi et al	
	5	6131512		2000-10-17	Verlinden et al	
	6	6479093		2002-11-12	Lauffer et al	
	7	6690968		2004-02-10	Mejia	
	8	7315014		2008-01-01	Lee et al	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	PHAM, LONG
	Attorney Docket Number	143705.05221

	9	7728274		2010-06-01	Pilla et al	
	10	8268403		2007-04-30	Akiyama et al	
	11	8445950		2013-05-21	Iida et al	
	12	8445985		2013-05-21	Hiyama et al	
	13	8530264		2013-09-10	De Munck et al	
	14	8604405		2013-12-10	Liu et al	
	15	8729678		2014-05-20	Shim et al	
	16	8928784		2015-01-06	Watanabe et al	
	17	9064762		2015-06-23	Yamaguchi	
	18	9478572		2016-10-25	Miyanami	
	19	9659984		2017-05-23	Ohkubo et al	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	PHAM, LONG
Attorney Docket Number	143705.05221

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U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050184291		2005-08-25	Cole et al	
	2	20050184353		2005-08-25	Mouli	
	3	20080303932		2008-12-11	Wang et al	
	4	20080191296		2008-08-14	Wang et al.	
	5	20090090988		2009-04-09	OHGISHI	
	6	20090096049		2009-04-16	Oshiyama et al	
	7	20090278967		2009-11-12	Toumiya	
	8	20090200625		2009-08-13	Venezia et al.	
	9	20100108864		2010-05-06	OHTA et al	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	PHAM, LONG
	Attorney Docket Number	143705.05221

	10	20100128161		2010-05-27	Yamaguchi	
	11	20100201834		2010-08-12	Maruyama et al.	
	12	20110241148		2011-10-06	Hiyama et al	
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	14	20120025199		2012-02-02	Chen et al	
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	16	20120153128		2012-06-21	Roy et al	
	17	20120188431		2012-07-26	Takimoto	
	18	20120217602		2012-08-30	Enomoto	
	19	20120049306		2012-03-01	Ohba et al.	
	20	20120228473		2012-09-13	Yoshitsugu	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	PHAM, LONG
	Attorney Docket Number	143705.05221

	21	20130020468		2013-01-24	Mitsuhashi et al	
	22	20130207212		2013-08-15	Mao et al	
	23	20140374868		2014-12-25	LEE et al	
	24	20140054662		2014-02-27	Yanagita et al	
	25	20170244920		2017-08-24	Ohkubo et al	
	26	20120147241	A1	2012-06-14	YAMAGUCHI TETSUJI	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
1	1	101241923	CN		2008-08-13	TAIWAN SEMICONDUCTOR MFG	See corresponding US2008191296	☐
2	2	101465361	CN		2009-06-24	TAIWAN SEMICONDUCTOR MFG		☒
3	3	101740597	CN		2010-06-16	SONY CORP	See corresponding US2010128161	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	PHAM, LONG
	Attorney Docket Number	143705.05221

4	4	101978498	CN		2011-02-16	OMNIVISION TECH INC	See corresponding US2009200625	☐
5	5	102270646	CN		2011-12-07	NA		☒
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7	7	2011003860	JP		2011-01-06	SONY CORP	See corresponding US2010201834	☐
8	8	2012054321	JP		2012-03-15	SONY CORP	See corresponding US2012049306	☐
9	9	2012169530	JP		2012-09-06	SONY CORP		☒
10	10	2012191005	JP		2012-10-04	SONY CORP	See corresponding US2012228473	☐
11	11	20060020400	KR		2006-03-06	MAGNACHIP SEMICONDUCTOR LTD		☒
12	12	20080014301	KR		2008-02-14	SAMSUNG ELECTRONICS CO LTD		☒
13	13	20080097709	KR		2008-11-06	DONGBU ELECTRONICS CO LTD		☒
14	14	20110079323	KR		2011-07-07	DONGBU HITEK CO LTD		☒

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	PHAM, LONG
	Attorney Docket Number	143705.05221

15	15	20170070266	KR		2017-06-21	SONY CORP	See corresponding US2014054662	☐
16	16	2012117931	WO		2012-09-07	SONY CORPORATION	See corresponding US2014054662	☐
	17	2007258684	JP		2007-10-04	SONY CORP	See corresponding US20120147241	☐

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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Byung Jun Park et al, Jpn. J. Appl. Phys. 46 2454, 2007, 5 pages.	☐
	2	Choubey et al., On Evolution of CMOS Image Sensors, Proceedings of the 8th International Conference on Sensing Technology, Sep. 2-4, 2014, Liverpool, UK, pages.	☐
	3	Fontaine, Ray, A Survey of Enabling Technologies in Successful Consumer Digital Imaging Products (Part 3: Pixel Isolation Structures), http://www.techinsights.com,July 24, 2017, 13 pages.	☐
	4	IMEC, 3D INTEGRATED IMAGE SENSORS FOR SMART IMAGING SYSTEMS, PIET DE MOOR, 2010, 32 pages.	☐
	5	KOREAN INTELLECTUAL PROPERTY OFFICE (KIPO), CMOS Image Sensor, KIPO, 2004, 29 pages.	☐
	6	MUNCK, Generic building blocks for 3D integration and their application on hybrid CMOS image sensors, KATHOLIEKE UNIVERSITEIT LEUVEN, Kapeldreef 75 — B-3001 Heverlee, September 2008, 328 pages.	☐

SAMSUNG EX. 1002 - 2441/2862

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	PHAM, LONG
	Attorney Docket Number	143705.05221

	7	Rao, et al., Monolithic and Fully-Hybrid Backside Illuminated CMOS Imagers for Smart Sensing, IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, 4 pages.	☐
	8	STMicroelctronics, BSI – technical challenges, IISW-2009, Bergen. 25th June 2009, 37 pages.	☐
	9	https://blogs.yahoo.co.jp/miyabiman_now/25628945.html	☐
	10	Agranov, et al., Pixel continues to shrink….Small Pixels for Novel CMOS Image Sensors, 4 pages.	☐
	11	Fontaine, A Review of the 1.4 µm Pixel Generation, Technology Analysis Group Chipworks Inc., 2011, 4 pages.	☐
	12	Lee et al., SNR Performance Comparison of 1.4um Pixel : FSI, Light-guide, and BSI, 2011, 3 pages.	☐
	13	Tournier, et al., Pixel-to-Pixel isolation by Deep Trench technology, STMicroelectronics, 850, rue Jean Monnet – F-38926 Crolles Cedex – France, 2011, 4 pages.	☐
	14	Tournier, et al., Pixel-to-Pixel isolation by Deep Trench technology: Application to CMOS Image Sensor, https://www.researchgate.net/publication/268300742, 2011, 5 pages.	☐
	15	B.J. Park et al., "Deep Trench Isolation for Crosstalk Suppression in Active Pixel Sensors with 1.7µm Pixel Pitch", in Japanese Journal of Applied Physics, Vol. 46, No. 4B, pp. 2454-5457, 2007	☐
	16	D. N. Yaung et al., "High performance 300mm backside illumination technology for continuous pixel shrinkage," 2011 International Electron Devices Meeting, Washington, DC, 2011, pp. 8.2.1-8.2.4.	☐
	17	http://electroiq.com/insights-from-leading-edge/2016/09/iftle-303-sony-introduces-ziptronix-dbi-technology-in-samsung-galaxy-s7, "Omnivision was the first to sample BSI in 2007 but costs were too high and adoption was thus very low", (2016)	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	PHAM, LONG
	Attorney Docket Number	143705.05221

	18	http://joseph-tang.blogspot.com/2017/, Oshiyama et al. , Near-infrared Sensitivity Enhancement of a Back-illuminated Complementary Metal Oxide Semiconductor Image Sensor with a Pyramid Surface for Diffraction Structure,(2017)	☐
	19	K. Itonaga et al., "Extremely-low-noise CMOS Image Sensor with high saturation capacity," 2011 International Electron Devices Meeting, Washington, DC, 2011, pp. 8.1.1-8.1.4.	☐
	20	K. Minoglou et al., "Reduction of Electrical Crosstalk in Hybrid Backside Illuminated CMOS Imagers using Deep Trench Isolation," 2008 International Interconnect Technology Conference, Burlingame, CA, USA, 2008, pp. 129-131.	☐
	21	Y. Kitamura et al., "Suppression of crosstalk by using backside deep trench isolation for 1.12μm backside illuminated CMOS image sensor," 2012 International Electron Devices Meeting, San Francisco, CA, 2012, pp. 24.2.1-24.2.4.	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

SAMSUNG EX. 1002 - 2443/2862

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	PHAM, LONG
Attorney Docket Number	143705.05221

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Reza Mollaaghababa, Reg. No. 43810/	Date (YYYY-MM-DD)	2018-07-31
Name/Print	Reza Mollaaghababa	Registration Number	43810

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

SAMSUNG EX. 1002 - 2444/2862

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

SAMSUNG EX. 1002 - 2445/2862

Espacenet

Bibliographic data: CN101241923 (A) — 2008-08-13

Image sensor semiconductor device

Inventor(s): SHINE CHUNG [CN] ± (CHUNG SHINE, ; WANG WEN-DE, ; YAUNG DUN-NIAN, ; HSU TZU-HSUAN)

Applicant(s): TAIWAN SEMICONDUCTOR MFG [CN] ± (TAIWAN SEMICONDUCTOR MFG, ; TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD)

Classification: - international: ***H01L27/146***
- cooperative: **H01L27/14625**; **H01L27/14632**; **H01L27/14687**

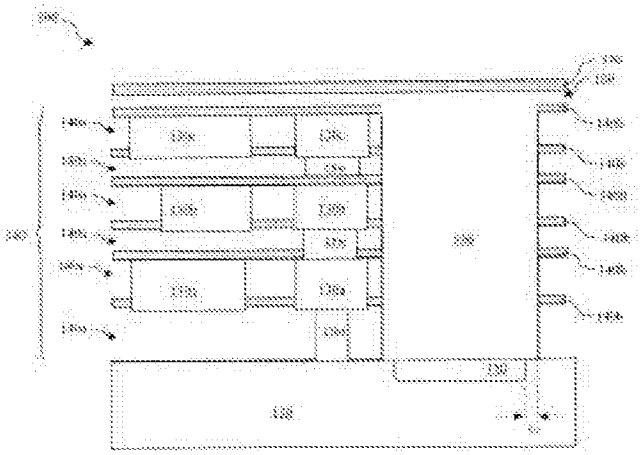
Application number: CN20071127069 20070628

Priority number(s): US20070672681 20070208

Also published as: CN101241923 (B) JP2008198971 (A) US2008191296 (A1) US7803647 (B2)

Abstract of CN101241923 (B)

The present disclosure provides an image sensor semiconductor device. The semiconductor device includes a sensor element disposed in a semiconductor substrate; an inter-level dielectric (ILD) disposed on the semiconductor substrate; and a trench disposed in the ILD, overlying and enclosing the sensor element, and filled with a first dielectric material.



[19] 中华人民共和国国家知识产权局

[51] Int. Cl.
H01L 27/146 (2006.01)

[12] 发明专利申请公布说明书

[21] 申请号 200710127069.0

[43] 公开日 2008 年 8 月 13 日

[11] 公开号 CN 101241923A

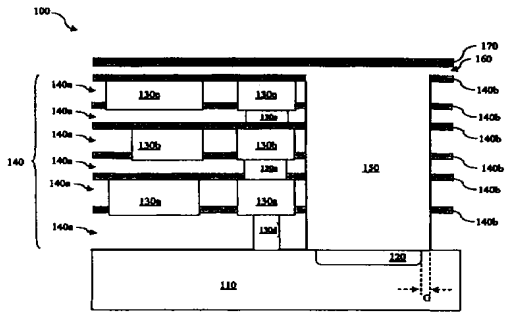
[22] 申请日 2007.6.28
[21] 申请号 200710127069.0
[30] 优先权
[32] 2007. 2. 8 [33] US [31] 11/672,681
[71] 申请人 台湾积体电路制造股份有限公司
地址 中国台湾新竹科学工业园区
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[54] 发明名称

图像传感器半导体器件

[57] 摘要

本发明公开了一种图像传感器半导体器件。此半导体器件包括传感组件，置于半导体基板内；层间介电材料(ILD)，置于半导体基板上；以及沟槽，置于 ILD 内，覆盖并包围传感组件，且填充有第一介电材料。



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1. 一种图像传感器半导体器件，包括:

传感组件，置于半导体基板内;

层间介电材料，置于该半导体基板上；以及

沟槽，置于该层间介电材料内，该沟槽覆盖并包围该传感组件且填充有第一介电材料。

2. 如权利要求 1 所述的器件，其特征在于，该沟槽更内衬第二介电材料。

3. 如权利要求 2 所述的器件，其特征在于，该第一介电材料包括折射率高于该第二介电材料的介电材料。

4. 如权利要求 2 所述的器件，其特征在于，该第二介电材料包括一含氮材料。

5. 如权利要求 2 所述的器件，其特征在于，该第二材料的厚度范围约在 50～500 埃之间。

6. 如权利要求 1 所述的器件，其特征在于，该第一介电材料包括介电材料可被从待成像物体朝向该传感组件的可见光所穿透，其中该可见光的波长范围在约 300～800 nm 之间。

7. 如权利要求 1 所述的器件，其特征在于，该第一介电材料包括折射率高于该层间介电材料的介电材料。

8. 如权利要求 1 所述的器件，其特征在于，该第一介电材料包括氧化硅。

9. 如权利要求 1 所述的器件，其特征在于，该第一介电材料包括多膜结构。

10. 如权利要求 1 所述的器件，其特征在于，该层间介电材料包括掺杂氟化物的硅化玻璃或掺杂碳的氧化硅。

11. 如权利要求 1 所述的器件，其特征在于，该传感组件包括互补式金属氧化物半导体图像传感器、电荷耦合器件传感器或有源图象素传感器。

12. 如权利要求 1 所述的器件，其特征在于，通过俯视，该传感组件位于该沟槽内，具有至少 0.1 微米的偏距。

13. 如权利要求 1 所述的器件，其特征在于，还包括置于该层间介电材料内的多个金属特征，每一金属特征的临界尺寸实质地小于约 0.25 微米。

14. 如权利要求 1 所述的器件，其特征在于，该传感组件的尺寸范围在约 0.5～5 微米之间。

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图像传感器半导体器件

技术领域

本发明涉及一种图像传感器半导体器件，具体地涉及改进高等互补式金属氧化物半导体（CMOS）成像器中多介电层结构的光传播。

背景技术

图像传感器是含若干形成在半导体基板上的传感组件或图象素的集成电路器件。传感组件用来感应投向半导体基板的大量暴露光。由于集成电路类型的多，随着半导体技术的发展而有改进图像传感器的需要。半导体技术的常规发展是在一或多导电层中采用铜。例如，高等半导体技术中互连金属使用铜，它可于金属层间介电层（inter-metal dielectric layers）之间增加各种蚀刻终止层与阻挡层，以防止铜迁移到附近的氧化硅介电材料中。氮化硅已广泛用作阻挡层和终止层。然而，氮化硅与氧化硅之间的折射率差异将引起光干涉，从而导致改变或降低图像传感器的性能。

发明内容

因此，本本发明提供一种图像传感器半导体器件。该器件包含置于半导体基板内的传感组件；置于半导体基板上的层间介电材料（ILD）以及置于ILD内的沟槽，该沟槽覆盖并包围住传感组件并填充有第一介电材料。

在一些实施例中，沟槽进一步与内衬第二介电材料。第一介电材料可包含折射率高于第二介电材料的介电材料。第二介电材料可包含含氮材料。第二材料的厚度范围可在约50~500埃之间。

在一些实施例中，第一介电材料包含可使从成像物体朝传感组件方向的可见光透射的介电材料。可见光的波长范围在约300~800nm之间。第一介电材料可包含折射率高于ILD的介电材料。

在一些实施例中，第一介电材料包含氧化硅。第一介电材料可包含多膜结构。第一介电材料可与传感组件接触。ILD可包含掺杂氟化物的硅酸盐玻璃（FSG）。ILD可包含掺杂碳的氧化硅。

在一些实施例中，传感组件包含互补式金属氧化物半导体（CMOS）图像传感器。传感组件可包含电荷耦合器件传感器。传感组件可包含有源图象

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素传感器。传感组件可包含无源图象素传感器。通过俯视，传感器组件可在沟槽内，并具有至少约 0.1 微米的偏距（offset）。该器件可进一步地包含置于 ILD 内的若干金属特征，每一金属特征的临界尺寸实质地小于约 0.25 微米。传感组件的尺寸范围可在约 0.5 微米至 5 微米之间。

本本发明还提供制造半导体器件的方法。该方法包含在半导体基板内形成传感组件；在半导体基板上形成层间介电材料（ILD），及多层互连（MLI）置于该 ILD；在 ILD 内形成开口，其中，该开口包围该传感组件；用介电材料填充该开口；以及对该开口内的介电材料实施抛光工艺。

在一些实施例中，本方法进一步包含在开口填充之前，在开口内形成衬垫。填充开口可包括使用折射率高于该衬垫的介电材料。在另一实施例中，填充开口包括使用折射率高于该 ILD 的介电材料。

在另一实施例中，图像传感器半导体器件包含：置于半导体基板内的传感组件；置于该半导体基板上的层间介电材料（ILD）；以及置于 ILD 内的沟槽，覆盖并接触传感组件，且用第一介电材料填充。

在一些实施例中，第一介电材料包含一种材料，其可为成像光所透射并作为成像光的波导。第一介电材料可包含具有高折射率的材料，被具有低折射率的材料所包围，用来对成像光全反射。第一介电材料可包含玻璃。

附图说明

本发明所揭示的各种态样可通过以下详细描述并结合附图而获得最佳的理解。值得强调的是，附图的尺寸及比例未必按照此技艺中的标准实务来绘制。事实上，为清楚讨论，不同特征的尺寸可任意地增加或减小。

图 1 是依照本发明所揭示的态样，例示一实施例的半导体器件的剖面图；

图 2 是依照本发明所揭示的态样，例示制造图 1 所示半导体器件的实施例的方法流程图；

图 3 是依照本发明所揭示的态样，例示图 1 所示的实施例的半导体器件的俯视图；

图 4 是依照本发明所揭示的态样，例示所构建的另一实施例的半导体器件剖面图。

具体实施方式

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将要理解的是，本揭示提供许多不同的实现方式或实例，它们将获利自本发明。下列将描述各组件及装配的具体实例，以简化本揭示。当然，它们仅为实例性而不意图是限制性。此外，本发明所揭示可在不同实例中重复使用各标号和/或字母。这种重复使用仅是为了简洁或清楚的目的，其本身不代表被讨论的实例和/或构造之间的关系。而且本说明中，第一特征形成于随后的第二特征上或之上，可包含第一与第二特征以直接接触方式而形成的实例，也可包含附加特征介入第一及第二特征而形成的实例，这样一来，第一与第二特征可不直接接触。

参考图 1 与图 2，以下将分别叙述具有图像传感组件的半导体器件 100 及其制造方法 200。图 1 是半导体器件 100 的实施例的剖面图，图 2 是一实施例的方法 200 的流程图。

方法 200 开始于步骤 210，提供半导体基板 110，在其内形成图像传感器 120。基板 110 包含晶体结构的硅。基板 110 可替代地或额外地包含其它基本的半导体如锗或金刚石。基板 110 也可包含化合半导体如碳化硅、砷化镓、砷化铟或磷化铟。基板 110 可包含各种 p 型掺杂区和/或 n 型掺杂区，经构建及耦合形成各种器件及功能特征。在各种步骤及工艺中，所有掺杂特征可通过使用如离子注入或扩散的工艺来实现。基板 110 可包含其它特征如浅沟槽隔离（STI）、外延层、绝缘层上半导体（SOI）结构或其各种组合。

图像传感组件 120 设置于半导体基板 110 内。传感组件 120 包含光感区，光感区可以是具有 N 型和/或 P 型掺杂的掺杂区域，其系通过如扩散或离子注入的方法，形成于半导体基板 110 内。光感区的掺杂浓度范围可在约 1014~1021 原子/cm3 之间。光感区可有一表面面积，其范围为相关联的传感组件的面积的约 10%～80%之间，其可加以运作以接收光（或来自待成像物体的其它形式的辐射能）。传感组件 120 的实例包含光电二极管、互补式金属氧化物半导体（CMOS）图像传感器、电荷耦合器件（CCD）传感器、有源传感器、无源传感器和/或散布于或形成于基板 110 内的其它类型器件。同样地，传感组件 120 可包含传统和/或未来开发的图像传感器件。

在此仅为示范目的提供传感组件 120。半导体器件 100 可包含设置于数组或其它合适结构内的若干传感组件。若干传感组件可设计成不同的传感类型。例如，一组传感组件可以是 CMOS 图像传感器，而其它组传感组件可以是无源传感器。而且，传感组件 120 可包含彩色图像传感器和/或单色图像

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传感器。

接着进行方法200的步骤220，在半导体基板110上形成多层互连(MLI)130和层间介电材料（ILD）140。MLI 130耦合于传感组件120及形成于半导体基板110内的其它电单元。图1例示具有三金属层的MLI结构。MLI 130包含不同金属特征如金属一130a、金属二130b、及金属三130c。MLI 130还包含接触特征130d，接触特征130d构建在金属一130a与半导体基板之间，并与两者耦合。MLI 130还包含通孔130e，每个通孔130e构建在相邻金属层间，并相互耦合。例如，通孔130e可设置在金属一130a与金属二130b之间，以及设置在金属二130b与金属三130c之间。金属特征130a、130b、130c、130d及130e中每一金属特征的临界尺寸实质地小于0.25微米。MLI 130包含铜。MLI 130可替代地或共同地包含其它导电材料如铜合金、钛、氮化钛、钽、氮化钽、钨、多晶硅、硅化金属或它们的各种组合。硅化金属可包含硅化镍、硅化钴、硅化钨、硅化钽、硅化钛、硅化铂、硅化铒、硅化钯或其各种组合。

多层互连可通过技术如CVD、溅射、电镀、其它合适工艺或其各种组合而形成。例如，PVD可用来形成铜种子层，然而电镀工艺用来沉积更多的铜以作为互连。图1所示的三金属层仅为简要示范起见。在不同的实施例中，MLI 130可包含少于或多于三金属层。MLI 130设计布置成没有阻挡传感组件120与成像光。

ILD 140设置在半导体基板110上，与MLI 130电绝缘。ILD 140可包含前金属介电层（PMD）和多种金属间介电层140a及多种蚀刻终止/阻挡层140b（或简化起见称为阻挡层）介入于邻接的IMD 140a之间。PMD与IMD层140a中每一层的厚度范围在约0.1微米~1微米之间。在一实例中，PMD的厚度范围在约3500～7000埃之间。通孔一与通孔二之间的IMD层的厚度范围在约1000～4000埃之间。金属一与金属二之间的IMD层的厚度范围在约1000~5000埃之间。位在较高金属层的IMD 140a可更厚。IMD与PMD 140a可包含二氧化硅如：未掺杂的硅玻璃（USG）、氮化硅、氮氧化硅、聚酰亚胺、旋涂式玻璃（SOG）、掺杂氟化物的硅酸玻璃（FSG）、掺杂碳的氧化硅如SiCOH、黑钻石（Black Diamond®）（美国加州Santa Clara的Applied Materials (应用材料)，）、干凝胶（Xerogel）、气凝胶（Aerogel）、无定形氟化碳、聚对二甲苯基（Parylene）、BCB（二苯并环丁烯）、SiLK（陶氏化学，

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中部，密歇根州）和/或其它合适材料。阻挡层 140b 在镶嵌工艺中可提供蚀刻终止功能、及阻挡功能以消除湿气扩散至 MLI130 以及铜迁移至 ILD140。阻挡层 140b 可包含氮化硅、氮氧化硅、碳化硅或其它适当的材料。ILD140（包含 140a 和 140b）可通过如旋涂、CVD、溅射、或其它合适工艺等技术来形成。例如，等离子体增强（PE）CVD 可用来将硅烷（SiH4）或四乙氧基硅烷(TEOS)形成氧化硅。在另一实施例中，可使用高密度等离子体(HDP)CVD。

MLI 130 与 ILD 140 可以称作镶嵌工艺如双镶嵌工艺或单镶嵌制成的集成工艺来形成。在一实例中，每一金属层、通孔及接触孔可通过下列描述的工艺流程而形成。蚀刻终止和/或阻挡层首先形成在半导体器件 100 上。蚀刻阻挡层可包含氮化硅或氮氧化硅。介电材料沉积在蚀刻终止层上形成介电层，并可进一步利用如化学机械平坦化(CMP)工艺或回蚀刻工艺而平坦化。CMP 终止层可形成在介电层上。然后根据预设计电路图案利用光光刻工艺蚀刻介电层形成沟槽（如贯通 130a 的 130e）。利用如溅射方法，在沟槽内沉积用于阻挡和/或粘结的衬垫层。接着在衬垫化后的沟槽内利用溅射工艺填充铜形成铜种子层，及利用电镀工艺形成铜填充。然后可除去介电层上形成的铜，并用 CMP 或回蚀刻工艺平坦化半导体器件 100。可替代的是，可利用现有技术的各种实施例中已知的双镶嵌工艺来形成 MLI 130 与 ILD 140。在一些实施例中，在步骤 220，可与 MLI 130 一起形成虚拟金属特征(dummy metal features)。例如，虚拟金属特征可形成在传感单元 120 之上的区域内，用于调节图案密度以及提高 CMP 性能。在下一步骤中，在沟槽形成期间，可除去虚拟金属特征。

方法 200 进行到步骤 230，在 ILD 140 内形成沟槽（开口）150。定义并布置出沟槽 150，从而暴露出传感单元 120。沟槽 150 具有延伸至传感组件 120 表面的深度。在另一实施例中，沟槽 150 不延伸至传感组件 120 表面，并且一部分 ILD 140 仍介于沟槽 150 与传感组件 120 之间（图未示）。通过俯视，沟槽 150 的水平尺寸实质地包围传感组件 120。例如，另外地如图 3 所示的传感组件 120 和沟槽 150 的俯视图，沟槽 150 之外围线将传感组件 120 包围在内。传感组件 120 与沟槽 150 的每一尺寸用 A 和 B 标出。传感组件 120 的尺寸范围在约 0.5 微米~5 微米之间。沟槽 150 的尺寸 B 可具有相似的范围，但具有一偏距，从而实质地包围传感组件。沟槽 150 设置成沟槽之外

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围线与传感组件 120 的各边具有一间隙，用 'G' 表示。间隙 G 可约 0.1 微米或更大。可用工艺流包含光刻图案化以及蚀刻来形成沟槽 150。例如，在 ILD 140 上施加光刻胶层，并利用光刻工艺将其图案化以形成开口。接着，蚀刻 ILD 130 并贯穿图案化光刻胶的开口，暴露出传感组件 120，生成沟槽 150。蚀刻工艺可利用干蚀刻技术，并使用碳氟基蚀刻剂以及氧气。在各种实施例中，碳氟基蚀刻剂可包含 CF_4、CHF_3、C_2F_6、C_3F_8、C_4F_8 或其各种组合。干蚀刻工艺的工艺温度可在约 100~150 度之间。可替代的是，蚀刻工艺可利用以氢氟酸（HF）为主的蚀刻剂的湿蚀刻技术。监控蚀刻工艺，以免过度蚀刻至半导体基板 110 与形成于内的传感组件 120。在另一实施例中，在形成 MLI 130 与 ILD 140 之前，在半导体基板 110 上可形成蚀刻终止层。因此，蚀刻工艺将停止在蚀刻终止层上。沟槽内的蚀刻终止层可用其它的蚀刻工艺除去，以便暴露出下面的传感组件 120。在另一实施例中，在 ILD 140 内形成沟槽 150 中，使用掩模层。例如施加一掩模层至 ILD 140。在掩模层上施加光刻胶层，并利用光刻工艺将其图案化形成开口。接着，蚀刻掩模层，将开口从光刻胶层转移到掩模层。用湿剥除或其后的等离子体灰化以除去光刻胶层。然后，蚀刻 ILD 140 贯过掩模层开口，从而在半导体基板 110 上形成沟槽 150 并暴露出传感组件 120。

方法 200 进行到步骤 240，填充沟槽 150。沟槽 150 实质地用可一种从成像物体朝传感组件方向的光可穿透的介电材料来填充。该光可以是可见光，波长范围在约 300～800nm 之间。

此外，在一实施例中，沟槽 150 内填充的介电材料的折射率高于周围的材料。填充的介电材料在显微透镜与传感组件之间形成波导，以达到对来自待成像物体的成像光的全反射。其它要求，例如显微透镜的焦距或显微透镜与传感组件间的距离可得到缓和，而不牺牲成像效率和品质。在一实施例中，沟槽 150 内填充的介电材料的折射率高于 ILD 140。

沟槽 150 内的填充材料包含以各种技术沉积的氧化硅，如未掺杂的硅石玻璃（USG）、用等离子体增强 CVD 从硅烷（SiH_4）所形成的氧化硅、用等离子体增强 CVD 从四乙氧基硅烷（TEOS）形成的氧化硅、高密度等离子体（HDP）CVD、旋涂式玻璃或其各种组合。沟槽 150 内的填充材料可替代地包含掺杂氧化物如氟化硅玻璃、掺杂碳的硅酸盐（SiCOH）或其它合适的材料如其它透明玻璃。沟槽 150 内的填充材料可以是一多膜结构。

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方法 200 进行至步骤 250，对沟槽 150 内以及 ILD 140 之上的填充材料实施平坦化工艺，从而平坦化半导体器件 100 并除去多余的填充材料。平坦化工艺可包含回蚀刻、CMP 或其各种组合。

方法 200 进行到步骤 260，在 ILD 140 及 MLI 130 上形成一钝化层，以实质地覆盖半导体器件并密封器件以避免受潮及其它污染。在一实例中，钝化层可包含置于 ILD 140 和填充的沟槽 150 上的氧化硅层 160、及氧化硅层 160 上的氮化硅层 170，用于增强钝化和粘结。

半导体器件 100 及其制造方法 200 可具有不同的变化形式。图 4 显示另一实施例的半导体器件 100 的剖面图。沟槽 150 进一步包含衬垫层 150a。衬垫层 150a 实质地形成在沟槽 150 的侧壁上，并可另外地形成在沟槽 150 的底部上。衬垫层 150a 可包含含氮材料，如氮化硅、氮氧化硅或其它合适的材料。在步骤 230 形成沟槽 150 之后并在步骤 240 填充沟槽 150 之前，衬垫层 150a 可用 CVD 工艺或其它适当的方法形成。衬垫层 150a 的厚度范围在约 50~500 埃之间，可具有多膜结构。衬垫层 150a 提供密封效果，以消除来自 MLI 130 的湿气和污染，及/或提供折射功能，以控制朝向传感组件的成像光，从而具有更高的成像效率并降低与其它功能单元如半导体器件中的其它传感组件间的干扰。在另一实施例中，衬垫化后的沟槽内的填充的介电材料的折射率高于衬垫层 150a。在另一实施例中，衬垫层 150a 的折射率高于 ILD 层 140。在另一实施例中，衬垫层 150a 的折射率高于 IMD 层 140a。利用填充的介电材料和衬垫层可实现全折射。为此目的，填充的介电材料和衬垫层可使用各种材料，该各种材料可包含不同材料、或者具有制造技术、不同工艺参数、不同类型掺杂和/或不同掺杂浓度的同一材料。例如，上面提及的 CVD 方法可通过动态控制工艺温度以形成衬垫层和填充的介电材料，而达成从衬垫层到填充的介电层的折射率变化。在另一实例中。填充的介电材料可包含用 CVD 方法形成的硼掺杂的硅酸盐。在另一实施例中，衬垫层或 ILD 可使用低 k 材料。

前面已概述了几个实施例的特征，从而本领域技术人员可更好地理解其后的详细描述。本领域技术人员应当理解，他们可容易地利用本揭示作为基础，来设计或修正其它工艺和结构，以实现在此介绍的实施例的目的和/或优点。本领域的技术人员也意识到，这种等同构建并没有脱离本发明的精神和范围，而且他们可作各种变化、替代、改变而不脱离本发明的精神和范围。

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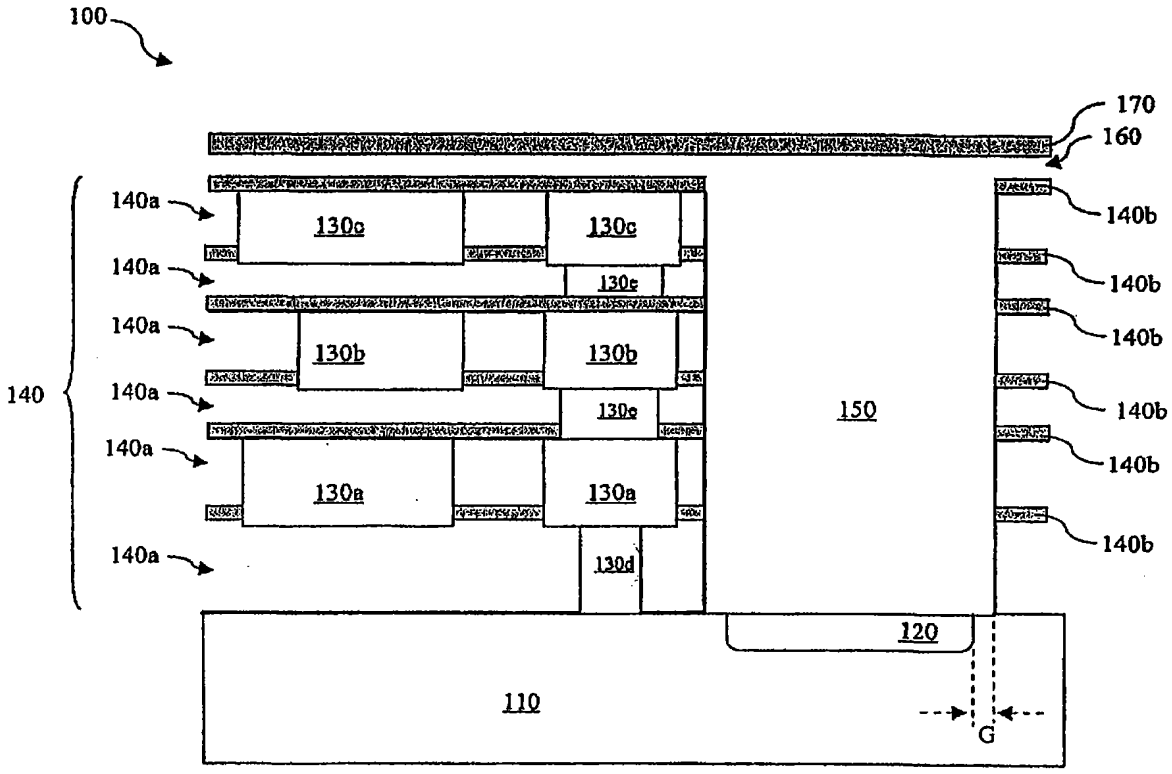


图 1

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Espacenet

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Isolation structure of image sensor element

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Abstract of CN101465361 (A)

The invention provides an image sensor element, which comprises a substrate with a pixel region and a peripheral region. A first isolation structure is formed in the pixel region of the substrate. The first isolation structure comprises a ditch with a first depth. A second isolation structure is formed in the peripheral region of the substrate. The second isolation structure comprises a ditch with a second depth. The first depth is greater than the second depth.

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DESCRIPTION CN101465361

The present invention provides an image sensor element that includes a substrate having a pixel area and a peripheral area. The first isolation structure is formed in a pixel area of the substrate. The first isolation structure includes a trench having a first depth. The second isolation structure is formed in a peripheral region of the substrate. The second isolation structure includes a trench having a second depth. The first depth is greater than the second depth.

Image sensor element isolation structure

Technical field

The present disclosure relates generally to image sensors and, more specifically, to image sensors including integrated circuits such as complementary metal-oxide semiconductor (CMOS) image sensors and charge coupled devices (CCDs). Image Sensor.

Background technique

In semiconductor technology, an image sensor is used to sense the amount of exposure projected onto the semiconductor substrate. CMOS sensors and CCD sensors are widely used in many applications such as digital cameras. These image sensors use a matrix of pixels containing light sensing elements to collect light energy and convert the image to digital data. However, when the pixel size is reduced, the sensitivity of the pixel will be reduced. In addition, the crosstalk between pixels will increase. Mutual interference can detract from spatial resolution, reduce overall sensitivity, provide poor color isolation, and can introduce additional noise into the

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image, especially after the color correction process. Processes and thin color filters containing these thin layers of material (e.g., thin dielectric and metal layers) can be used to improve optical interference. However, these conventional methods of improving electrical mutual interference (e.g., providing a sensor with a thin epitaxial layer) are provided for other problems such as Electrostatic discharge (ESD) failure. Problems with other conventional image sensors include long-wavelength light sensitivity and image defects, such as from a Blooming effect (a particular area of the output image is displayed brighter than the original image).

Therefore, there is a need for improved image sensors.

Summary of the Invention

The present disclosure provides disclosures related to semiconductor devices, and more particularly to an isolation structure of an image sensor. The proposed novel structure can reduce electrical mutual interference and other optical defects between pixels.

The present invention provides an image sensor having a substrate including a pixel area and a peripheral area, a first isolation structure formed in a pixel area of the substrate, and a second isolation formed in a peripheral area of the substrate structure. The first isolation structure includes a first trench having a first depth, the second isolation structure includes a second trench having a second depth, and wherein the first depth is greater than the second depth.

In other words, the present invention provides an image sensor element including a substrate having a pixel area and a peripheral area. The isolation structure is formed in the pixel area of the substrate. The isolation structure includes a trench. Another isolation structure is formed in the peripheral region of the substrate. The isolation structure also includes trenches. The trench formed in the pixel area has a greater depth than the trench formed in the peripheral area.

In another aspect, the present invention provides another image sensor element including a substrate having a pixel area and a peripheral area. A plurality of pixels are formed in the substrate of the pixel region. Ditches are formed between two pixels. The trench has a first depth. The second trench is formed in the peripheral region of the substrate. The depth of the second trench is less than the first depth.

In yet another aspect, the present invention provides a method of forming an image sensor. A substrate including a pixel area and a peripheral area is provided. A first isolation trench is formed in a pixel region of the substrate,

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and forming the first isolation trench includes etching the substrate to a first depth. A second isolation trench is formed in the peripheral region of the substrate. Forming the second isolation trench includes etching the substrate to a second depth, the second depth being less than the first depth.

Description of the drawings

The various aspects disclosed herein are best understood from the foregoing detailed description and by reading the accompanying drawings. It should be emphasized that many features are not drawn to scale according to industry standard practice. In fact, the size of each feature may be arbitrarily increased or decreased for clarity of discussion.

FIG. 1 is a top view of an image sensor including a pixel area and a peripheral area; FIG.

FIG. 2 is a sectional view of a conventional image sensor including a matrix of pixels and a peripheral area; FIG.

3 is a cross-sectional view of an image sensor including a pixel matrix and a peripheral area of an embodiment;

FIG. 4 is a flowchart showing an embodiment of a method of manufacturing the image sensor of FIG. 3; FIG.

Figures 5a to 5g are sectional views of the embodiment of the method of Figure 4;

6 is a flow chart of another alternative embodiment of the method of manufacturing an image sensor of FIG. 3;

Figures 7a to 7e are cross-sectional views of the method embodiment of Figure 5; and

FIG. 8 is a cross-sectional view of an alternate embodiment of an image sensor including a matrix of pixels and a peripheral region.

detailed description

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The present disclosure relates generally to semiconductor elements, particularly image sensors. It should be understood, however, that specific embodiments are provided as examples to teach broader concepts of the invention and that those skilled in the art can readily apply the teachings of this disclosure to other methods or elements. In addition, it should be understood that the methods and apparatus discussed in this disclosure encompass some conventional structures and/or processes. Since these structures and processes are well known in the field, they will only be discussed in general detail. Moreover, for convenience and example, reference numerals are repeated throughout the drawings, and the repetitions do not indicate any desirable features or combination of steps throughout the drawings. Also, forming the first feature past the second feature, over the second feature, or coupled to the second feature may include in the subsequent description such embodiments in which the first and second features are formed in direct contact; or may be included in Between the first and second features are inserted embodiments that form additional features, such that the first and second features may not be in direct contact. Furthermore, forming features on the surface of the substrate or substrate may include forming features (eg, implant regions, trenches) over the substrate surface, adjacent to the substrate surface, directly on the substrate surface, and/or extending below the substrate surface. Examples.

Referring to FIG. 1, the image sensing element 100 provides a pixel area 110 and a peripheral area 120. The pixel area 110 includes a matrix of pixels 110a. In an embodiment, the image sensing element 100 may be a complementary metal oxide semiconductor (CMOS) image sensor (CIS) or an active pixel sensor. In alternative embodiments, the image sensor 100 may be a charge coupled device (CCD) sensor. The image sensing element 100 may be a front-side light sensor or a back-side light sensor. In the structure of the back side light emitting sensor, the sensed light is incident on the back side of the substrate and the pixels are formed on the front side of the substrate. Pixel 110a includes at least one optical detector (e.g., photodiode) to record light intensity or intensity. In an embodiment, pixel 110a includes a pin photodiode. Each pixel 110a also includes at least one transistor. The pixel 110a includes a reset transistor, a source follower transistor, a selector transistor, and/or a transfer transistor. The reset transistor may perform reset of the pixel 110a. The source follower transistor may allow the voltage to be combined with the observed pixel 110a without removing the accumulated charge. The selector transistor may be a row selector transistor and allow reading of a single row of pixels 110a when the selector transistor is on. The transfer transistor can move the accumulated charge in the photodetector of the pixel 110a to another element, thus outputting data from the pixel. Transfer transistors may allow associated subsampling. In an embodiment, the pass transistor may be combined (assigned) to a single photodiode, and the source follower, reset and selector transistors may be combined (shared) with multiple photodiodes. In the second embodiment, the transfer transistor may be coupled to a photodiode, and the source follower and reset transistor may be coupled to a plurality of photodiodes. In one embodiment, each pixel 110 includes four transistors. The image sensor element is a 4T CMOS image sensor commonly used in the field. The 4T CMOS image sensor may include a pass transistor, a reset transistor, a source follower transistor, and a selector transistor. In one embodiment, the transistors included in pixel region 110 include a metal oxide semiconductor field effect transistor (MOSFET) having a gate that includes a silicide layer. The silicide layer may include silicides such as nickel silicides, cobalt silicides, tungsten silicides, germanium silicides, titanium silicides, platinum silicides, germanium silicides, palladium silicides, and/or combinations thereof.

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In the peripheral region 120, additional circuitry and inputs/outputs are provided adjacent to the pixel region 110 to provide an operating environment for the pixel 110a and/or to support external communication with the pixel 110a. The peripheral area 120 may also be a logic area as it may include logic circuitry coupled to the pixel 110a. The peripheral area 120 may include low power logic circuitry. The low power logic circuit may include low power, high speed, high performance logic circuits. The peripheral circuit 120 may include, for example, a pixel driving circuit, a circuit for obtaining a signal charge, an A/D converter, a processing circuit for forming an image output signal, an electrical connector to which other elements may be connected, and/or commonly used in the field. Other components. In an embodiment, the peripheral region 120 includes MOSFET elements having source, drain, and gate electrodes, each of which includes a silicide layer. The silicide layer may include silicides such as nickel silicide, cobalt silicide, tungsten silicide, germanium silicide, titanium silicide, platinum silicide, germanium silicide, palladium silicide, and/or combinations thereof.

Referring now to FIG. 2, a cross-sectional view of a conventional image sensor 200 is shown. The image sensor 200 includes a pixel area 210 and a peripheral area 220. The color filter 230 is disposed above the pixel area 210 . The color filter 230 has a plurality of filters including a blue filter 230a, a green filter 230b, a red filter 230c, and a blue filter 230d. The sensor 200 includes a substrate 250 having a sub-layer 250a and an epitaxial layer 250b. A plurality of trenches including trenches 260a, 260b, 260c, and 270 are formed on the substrate 250. The trenches 260a, 260b, and 260c are formed in the pixel area 210. The trench 270 is formed in the peripheral area 220 . The trench 270 is substantially similar to the trenches 260a, 260b, and 260c. For example, the trench 270 and the trenches 260a, 260b, and 260c have substantially the same depth D1. In general, D1 is between 0.3 and 0.6 μ m.

Ditches in the pixel area (including 260a, 260b, and 260c) are used to separate pixels from the second pixel. For example, the trench 260b is used to separate a pixel formed in the substrate 250 (region P2) under the red filter 230c and a substrate 250 formed under the green filter 230b (region P1) pixels. The trench 270 can be used to separate one or more components in the peripheral area. The element 200 has the disadvantage that the trenches 260a, 260b, and/or 260c may not properly separate one pixel region from another. Depths of the trenches 260a, 260b, and/or 260c may not be sufficient to prevent light-generating carriers from the first pixel region (e.g., the region P1) from moving to the second pixel region (e.g., the region P2). This will cause electrical interference with each other and degrade the performance of the sensor 200. Therefore, there is a need for an improved isolation structure.

Referring to FIG. 3, an image sensor element 300 of an embodiment of the present invention is shown. The image sensor 300 includes a substrate 310 having a sub-layer 310a and an epitaxial layer 310b, and a color filter 320 above the substrate 310. The image sensor element 300 may be substantially the same as the image sensor element 100 of FIG. 1 described above. The image sensor element 300 includes a pixel area 302 and a peripheral area 304. A plurality of pixels (not shown) may be formed in the pixel area 302 of the substrate 310. For example, a first

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pixel may be formed in region P3, and a second pixel may be formed in region P4. The pixel includes a photodetector and one or more transistors. One or more pixels of the image sensor element 300 may be substantially similar to the pixels 110a of Figure 1 previously described. The peripheral region 304 may be substantially similar to the peripheral region 120 shown in Figure 1 previously described.

The color filter 320 includes blue filters 320a and 320d, a green filter 320b, and a red filter 320c, although color filters of other embodiments are also possible. In an alternate embodiment, the image sensing element 300 is a backside light emitting sensor. In an embodiment, the color filter 320 is disposed adjacent to the back surface of the substrate 310, and filters light incident on the back side of the substrate 310. One or more micro-lenses (not shown) may be formed adjacent to the color filter 320 with respect to the substrate 310 .

The substrate 310 may be a crystalline silicon. In alternative embodiments, the substrate 310 may include other base semiconductors (e.g., germanium), or may include compound semiconductors (e.g., silicon carbide, gallium arsenide, indium arsenide, and indium phosphide). In one embodiment, the substrate 310 is a P-type substrate (P conductive) (eg, a substrate doped with a P-type dopant (eg, boron or aluminum) with conventional diffusion or ion implantation). In other embodiments, the substrate 310 may include a P+ substrate, an N+ substrate, and/or other conductive types known in the art. The substrate 310 may include a silicon-on-insulator (SOI) substrate. The epitaxial layer 310b allows different doping profiles than other portions of the substrate 310 (including the sub-layer 310a). The epitaxial layer 310b can be grown on the substrate 310 using conventional methods. In one embodiment, the epitaxial layer 310b is a p-epitaxial layer. In one embodiment, the sub-layer 310a is a p+ layer. Possible embodiments include the epitaxial layer 310b is an N-epitaxial layer and the sub-layer 310a is an N+ sub-layer, the epitaxial layer 310b is an N-epitaxial layer and the sub-layer 310a is a P+ sub-layer, and/or Other commonly used conductive types in the field. The thickness T of the epitaxial layer 310b may be between about 2 μ m and 10 μ m. In another embodiment, the thickness T of the epitaxial layer may be approximately 4 μ m.

In one embodiment, the epitaxial layer 310b is a p-type conductivity type, and a photodiode included in a pixel (not shown) formed in the substrate 310 includes an N-type photogeneration region (eg, formed in a P-type region). An epitaxial N-type well photodetector. The N-type light generating region may be formed by doping the substrate with N-type dopants (e.g., phosphorous, arsenic, and/or other N-type dopants commonly used in the described art). The doping may be accomplished using conventional processes known in the art (e.g., lithographic patterning followed by ion implantation or diffusion). In other embodiments, the photodiode includes a pin photodiode. The pin layer may be doped with a p-type dopant. The p-type dopant may include boron, aluminum, and/or other P-type conductivity type dopants commonly used in the art.

An isolation structure including isolation trenches 340 is formed in the peripheral region 304 of the image sensor 300 . The isolation trench 340 may include a shallow trench isolation (STI) structure. The isolation trench 340

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can assist in isolating one or more components formed on the peripheral region 304. The depth D2 of the isolation trench 340 is less than about 0.6 μm. In an embodiment, the depth D2 of the isolation trench 340 is about 0.3 μm to 0.6 μm. A deeper depth D2 (eg, greater than 0.6 μm) may provide a high sheet resistance (Rs) of the N-type well junction located in the peripheral region 304 . A higher Rs detracts from the pick-up function. The isolation trench 340 may include silicon oxide. In one embodiment, the isolation trench 340 may contain air in addition to or in place of silicon oxide. Other embodiments in which the trenches 340 contain other insulating materials are also possible. The isolation trench 340 may be formed by conventional methods commonly used in the art. For example, hole etching is performed in the peripheral region 304 of the substrate 310 using conventional processes such as reactive ion etching (RIE) of a pattern formed according to a conventional photolithography process. The hole can then be filled. For example, in one embodiment, the trenches are filled with silicon oxide. In one embodiment, the process includes high-density plasma chemical vapor deposition (HDPCVD) of silicon oxide to fill holes and then a chemical mechanical polish (CMP) process The oxide is planarized. In alternative embodiments, the process includes Sub-Atmospheric Chemical Vapor Deposition (SACVD) of silicon oxide followed by a chemical mechanical polishing process to planarize the oxide. The method of forming the isolation trench 340 will be discussed later in more detail.

A plurality of isolation structures including isolation trenches 330a, 330b, and 330c are formed in the pixel area 302 of the substrate 310. The isolation trenches 330a, 330b, and 330c may include shallow trench isolation (STI) structures. The isolation trenches 330a, 330b, and/or 330c at least partially isolate the pixels from the second pixels of the pixel area 302. For example, the isolation trench 330b provides blocking barriers from the pixel area P3 to the pixel area P4. The depth D3 of the isolation trenches 330a, 330b and/or 330c is greater than about 0.6 μm. In an embodiment, the isolation trenches 330a, 330b, and/or 330c may have a depth D3 of between about 0.6 μm and 2 μm. In an embodiment, the isolation trenches 330a, 330b and/or 330c may have a depth D3 of between about 0.6 μm and 1 μm. In an embodiment, the isolation trenches 330a, 330b, and/or 330c may have a depth D3 of about 1 μm to 2 μm.

The isolation trenches 330a, 330b, and/or 330c may include (eg, completely fill in or partially fill in) the insulation material. The insulating material (such as silicon oxide) can isolate minority carriers from the pixels to the second pixel. In alternative embodiments, the isolation trenches 330a, 330b, and/or 330c may be filled with an oxide, a substantially optically opaque material, and/or a low-refractive index material, which will be described in detail later with reference to FIG. The isolation trenches 330a, 330b, and/or 330c may be formed using conventional techniques commonly used in the field. For example, hole etching is performed in the pixel region 302 of the substrate 310 using conventional processes such as reactive ion etching (RIE) performed after the pattern formed by a conventional photolithography process. The hole can then be filled. For example, in one embodiment, the trenches are filled with silicon oxide. In one embodiment, the process includes high density plasma chemical vapor deposition of silicon oxide to fill holes, followed by a chemical mechanical polishing process to flatten the oxide. In an alternate embodiment, the process includes sub-atmospheric chemical vapor deposition of silicon oxide followed by a chemical mechanical polishing process to planarize the oxide. The method of forming the isolation trenches 330a, 330b, and 330c will be discussed in more detail later.

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FIG. 4 shows a method 400 of forming an image sensor including an isolation structure. FIGS. 5 a, 5 b, 5 c, 5 d, 5 e, and 5 f show continuous changes of the substrate 500, which correspond to the steps of FIG. 4. The method 400 may be used to fabricate an image sensor element substantially similar to the image sensor 300 described in FIG.

Method 400 begins at step 402 by providing a substrate including a pixel area and a peripheral area. The substrate also includes an epitaxial layer. The substrate provided may be substantially similar to substrate 310 of FIG. 3 previously described. In the example of Fig. 5a, a substrate 500 is provided. Substrate 500 includes a sub-layer 502 and an epitaxial layer 504 . In one embodiment, the sub-layer 502 is a P+ layer and the epi-layer 504 is a P-layer. The substrate 500 further includes a pixel area 500a and a peripheral area 500b. The pixel area 500a may be substantially similar to the pixel area 110 and/or the pixel area 302 shown in FIGS. 1 and 3, respectively. The peripheral region 500b may be substantially similar to the peripheral region 120 and/or the peripheral region 304 shown in FIGS. 1 and 3, respectively.

The method 400 then proceeds to step 404 where a plurality of isolation structures are formed in the pixel area of the substrate. The isolation structure includes isolation trenches. The trenches are formed to a depth greater than about 0.6 μ m. The trenches may be formed using processes commonly used in the art (e.g., lithographic patterning with RIE etching) to form holes (ditches) in the patterned regions. In the example of FIG. 5b, the trench 510 is etched in the substrate 500, and more precisely in the epitaxial layer 504 of the substrate 500. The trench 510 is etched to a depth D4. D4 may be between about 0.6 μ m and 2 μ m.

The method 400 proceeds to step 406 where a layer of insulating material is formed on the substrate. The layer may be made of a deposition material using chemical vapor deposition, Plasma Enhanced Chemical Vapor Deposition (PECVD), Atmospheric Pressure Chemical Vapor Deposition (APCVD), Low Pressure Chemical Vapor Deposition, High Density Plasma Chemical Vapor Deposition, Atomic Layer Chemical Vapor Deposition, Sub-atmospheric Chemical Vapor Deposition (SACVD), and/or other processes commonly used in such fields. In an embodiment, the isolating material is silicon oxide. In an embodiment, the oxide is deposited by HDP CVD or SACVD. The layer may be partially or completely filled with the trenches of the pixel area as previously described with respect to step 404. In the example of FIG. 5c, a conformal insulating layer 520 is deposited on the substrate 500. The insulating layer 520 fills the trench 510, which is now designated isolation trench 510a. The method then proceeds to step 408 where the insulating layer is planarized. In an embodiment, the layer is planarized using a chemical mechanical polishing process. The example of FIG. 5d shows a flattened layer of insulating material 520, so that the insulating material fills completely in the isolation trench 510a and provides a substantial plane of the substrate 500.

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The method 400 proceeds to step 410 where at least one isolation structure is formed in a peripheral region of the substrate. The isolation structure includes isolation trenches. The depth of the trench etch is less than the depth of the trench formed in the pixel region as described in step 404. The etch depth of the trenches may be less than about 0.6 μm. The trenches may be etched using processes commonly used in the art, such as photolithographic patterning followed by RIE etching to form holes (ditches) in accordance with patterned regions. In the example of FIG. 5e, the trench 530 is etched in the peripheral region 500b of the substrate 500, and more precisely in the epitaxial layer 504 of the substrate 500. The trench 530 is etched to a depth D5. D5 is smaller than D4 shown in FIG. 5b. In one embodiment, D5 is less than about 0.6 μm. The method 400 proceeds to step 412 where a conformable layer of insulating material is deposited on the substrate. The layer can be completely or partially filled into the trench of the peripheral area as described in step 410 . The insulating material layer may be Physical Vapor Deposition (PVD) (sputtering), chemical vapor deposition, plasma enhanced chemical vapor deposition, atmospheric pressure chemical vapor deposition, low pressure chemical vapor deposition, high density plasma chemistry Deposition is performed by vapor deposition (HDPCVD), atomic layer chemical vapor deposition, sub-atmospheric pressure chemical vapor deposition (SACVD), and/or other processes commonly used in the art. In an embodiment, the insulating material is silicon oxide. In another embodiment, the oxide is deposited by HDP CVD or SACVD. In the example of FIG. 5f, a conformal topography layer 540 of insulating material is deposited on the substrate 500 and includes filling the trenches 530. The method 400 proceeds to step 414 where the insulating layer is planarized. In one embodiment, the insulating layer is planarized using an electrochemical mechanical polishing process. The example of FIG. 5g shows a planarized layer of insulating material 540, so the insulating material fills in the trench 530 and provides a substantially planar surface of the substrate 500. In an embodiment, the insulating layer 540 includes silicon oxide.

Referring to FIG. 6, a method 600 of manufacturing an image sensor element is shown; FIGS. 7a, 7b, 7c, 7d, and 7e show continuous changes of the substrate 700, which correspond to the steps of FIG. The method 600 may be used to fabricate image sensor elements substantially similar to the image sensor 300 described in FIG.

Method 600 begins in step 602 with providing a substrate including a pixel area and a peripheral area. The substrate also includes an epitaxial layer. The substrate provided may be substantially similar to substrate 310 of FIG. 3 previously described. In the example of FIG. 7a, a substrate 700 is provided. Substrate 700 includes a sub-layer 702 and an epitaxial layer 704 . In an embodiment, the sub-layer 702 is a P+ layer, and the epitaxial layer 704 may be a P-layer. The substrate 700 further includes a pixel area 700a and a peripheral area 700b. The pixel area 700a may be substantially similar to the pixel area 110 and/or the pixel area 302 shown in FIGS. 1 and 3, respectively. The peripheral area 700b may be substantially similar to the peripheral area 120 and/or the peripheral area 304 shown in FIGS. 1 and 3, respectively.

Method 600 then proceeds to step 604 where a plurality of isolation structures are formed in the pixel area of the substrate. The isolation structure includes isolation trenches. The trench may be formed at a depth of the substrate greater than 0.6 μm. The trenches may be formed using processes commonly used in the art, such as

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etching in accordance with the patterned RIE after photolithographic patterning to form holes (ditches). In the example of FIG. 7b, the trench 710 is etched in the substrate 700, and more precisely in the epitaxial layer 704 of the substrate 700. The trench 710 is etched to a depth D6. D6 is greater than 0.6 μm. In one embodiment, D6 is between about 0.6 μm and 2 μm.

The method 600 proceeds to step 606 where at least one isolation structure is formed in a peripheral region of the substrate. The isolation structure includes isolation trenches. The formation depth of the trench may be less than 0.6 μm. The depth of the trench etch is less than the depth of the trench formed in the pixel region in step 604 . The trenches can be formed by processes commonly used in the field, such as photolithographic patterning and RIE etching according to the patterned regions to form holes (ditches). In the example of FIG. 7c, the trench 720 is etched in the peripheral region 700b of the substrate 700. The depth of the trench 720 is D7. D7 is smaller than D6 shown in Fig. 7b. In an embodiment, D7 may be less than 0.6 μm.

The method 600 proceeds to step 608 where a layer of insulating material is formed on the substrate. The layers may be formed by conventional deposition processes such as chemical vapor deposition, plasma enhanced chemical vapor deposition, atmospheric pressure chemical vapor deposition, low pressure chemical vapor deposition, high density plasma chemical vapor deposition (HDPCVD), atomic layer chemical vapor deposition, Pressure Vapor Chemical Vapor Deposition (SACVD) and/or other processes commonly used in the field. In an embodiment, a silicon oxide layer may be formed on the substrate using, for example, HDPCVD or SACVD deposition. The insulating material layer completely or partially fills the trenches formed in steps 606 and 604, respectively, in the peripheral area and the pixel area. In the example of FIG. 7d, a conformal topography layer 730 comprising an insulating material is deposited over the substrate 700 and includes filling the trenches 710 and 720, which are currently designated as isolation trenches 710a and 720a. In an embodiment, the layer 730 includes silicon oxide. The method 600 proceeds to step 610 where the insulating layer is planarized. In an embodiment, the insulating layer is planarized using a chemical mechanical polishing process. The example of FIG. 7e shows a planarized layer of insulating material 730, so the trenches 710a and 720b are filled in and provide a substantially planar surface of the substrate 700.

Referring to FIG. 8, an image sensor 800 is shown. The image sensor 800 includes a substrate 802 having a sub-layer 804 and an epitaxial layer 806, and a color filter 808 above the substrate 802. The image sensor 800 has a pixel area 802a and a peripheral area 802b. The image sensor element 800 may be substantially similar to the image sensor element 300 and/or image sensor 100 shown previously in FIGS. 3 and 1 respectively. Moreover, for example, the substrate 802 may be substantially similar to the substrate 310 shown in FIG. 3; the peripheral region 802b may be substantially similar to the peripheral region 102 shown in FIGS. 1 and 3 respectively. And/or peripheral area 304. The color filter 808 may be substantially similar to the color filter 320 shown in Figure 3 previously described. A plurality of pixels (not shown) may be formed in the pixel area 802a of the substrate 800. The one or more pixels formed on the substrate 802 may be substantially similar to the pixels 110a of Figure 1 previously described.

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An isolation structure including isolation trenches 816 is formed in the peripheral area 802b of the image sensor 800. The isolation trenches 816 may be substantially similar to the isolation trenches 340 shown in Figure 3 previously described. A plurality of isolation structures including isolation trenches 810, 812, and 814 may be formed in the pixel area 802a of the image sensor 800. The isolation trenches 810, 812, and/or 814 may include STI structures. The isolation trenches 810, 812, and/or 814 provide enhanced isolation between the pixels of the pixel area 802a and the second pixels. The depth of the isolation trenches 810, 812 and/or 814 is greater than the isolation trench 816. In one embodiment, the isolation trenches 810, 812, and/or 814 include a depth greater than 0.6 μ m, and the isolation trenches 816 include a depth less than 0.6 μ m.

The isolation trenches 810, 812 and/or 814 may be filled with one or more materials. The isolation trench 810 includes a first layer 810a and a second layer 810b. The isolation trench 812 includes a first layer 812a and a second layer 812b, and the isolation trench includes a first layer 814a and a second layer 814b. The first layers 810a, 812a, and/or 814a of the isolation trench may include a layer of insulating material. The insulating material (e.g. silicon oxide) can assist in isolating the minority carriers from the pixel to the second pixel. In an embodiment, the second layer 810b, 812b and/or 814b of the isolation trenches comprise a substantially optically opaque material. In an embodiment, the opacity of the substantially optically opaque material is greater than about 50%. In the example of the substantially optically opaque material, tungsten and/or other opaque materials including other metal films may be included. The use of a substantially optically opaque material may increase the sensitivity of the image sensor 800 to long wavelength light. In alternative embodiments, the second layers 810b, 812b, and/or 814b comprise a low refractive index material (RI), such as air. In an embodiment, the low RI material includes an RI value of less than about 5 . In an embodiment, the second layers 810b, 812b, and/or 814b may include air gaps in the first layers 810a, 812a, and 814a that have an insulating material. Adding a low RI material allows for increased incident light reflection. The above embodiments are only for illustration and not limitation. Other structures and material combinations are possible.

Therefore, an image sensor element is provided. The element includes a substrate having a pixel area and a peripheral area. Isolation structures are formed in the pixel area of the substrate. The isolation structure includes a trench. Another isolation structure is formed in the peripheral region of the substrate. The isolation structure also includes a trench. The trenches formed in the pixel area have a greater depth than the trenches formed in the peripheral area.

In addition, another image sensor element is provided that includes a substrate having a pixel area and a peripheral area. A plurality of pixels are formed in the substrate of the pixel region. Ditches are formed between two pixels. The trench has a first depth. The second trench is formed in the peripheral region of the substrate. The depth of the second trench is less than the first depth.

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A method of forming an image sensor is also provided. A substrate including a pixel area and a peripheral area is provided. A first isolation trench is formed in a pixel region of the substrate, and forming the first isolation trench includes etching the substrate to a first depth. A second isolation trench is formed in the peripheral region of the substrate. Forming the second isolation trench includes etching the substrate to a second depth, the second depth being less than the first depth.

Although the present invention has been described in detail with respect to some embodiments thereof, it will be apparent to those skilled in the art that various modifications may be made without departing from the novel teachings and advantages of the present disclosure based on the teachings and disclosure of the present invention.

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CLAIMS CN101465361

1.
An image sensor element characterized by comprising:

a substrate including a pixel area and a peripheral area;

a first isolation structure formed in a pixel region of the substrate, wherein the first isolation structure includes a first trench having a first depth; and

A second isolation structure formed in a peripheral region of the substrate, wherein the second isolation structure includes a second trench having a second depth, and wherein the first depth is greater than the second depth.

2.
The element of claim 1 wherein the first isolation structure comprises silicon oxide.

3.
The element of claim 1 wherein the first isolation structure comprises a material selected from the group consisting of insulating materials, substantially optically opaque materials, low refractive index materials, and combinations thereof.

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4.
The element of claim 1 wherein the first depth is greater than about 0.6 μ m.

5.
The element according to claim 1, wherein the substrate comprises an epitaxial layer having a first conductivity type and a substrate layer having a second conductivity type.

6.
The element according to claim 5, wherein said substrate is selected from the group consisting of a substrate of a first conductivity type including p-type and a second conductivity type of p+ type, a first conductivity type including n-type, and n+. The substrate of the second conductivity type includes a group consisting of an n-type first conductivity type and a p+ type second conductivity type substrate.

7.
An image sensor element characterized by comprising:

a substrate including a pixel area and a peripheral area;

a first pixel and a second pixel formed in a pixel region of the substrate;

a first trench isolation structure formed in a pixel region of the substrate and between the first pixel and the second pixel, wherein the first trench isolation structure has a first depth; and

A second trench isolation structure is formed in the peripheral region, the second trench isolation structure has a second depth, and the second depth is less than the first depth.

8.
The element of claim 7, wherein the substrate comprises an epitaxial layer having a first conductivity type, and wherein the first pixel comprises a photodiode having a second conductivity type.

9.
The element of claim 7 wherein the first depth is between about 0.6 μ m and 1 μ m.

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10.

The element of claim 7 wherein the second depth is about 0.6 μ m or less.

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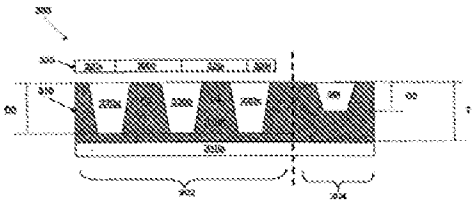
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[54] 发明名称

图像传感器元件的隔离结构

[57] 摘要

本发明提供一种图像传感器元件，其包含具有像素区域和外围区域的衬底。 第一隔离结构形成于所述衬底的像素区域中。 所述第一隔离结构包含具有第一深度的沟渠。 第二隔离结构形成于所述衬底的外围区域中。 所述第二隔离结构包含具有第二深度的沟渠。 所述第一深度大于所述第二深度。



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1. 一种图像传感器元件，其特征在于包含：

包含像素区域和外围区域的衬底；

形成于所述衬底的像素区域中的第一隔离结构，其中所述第一隔离结构包含具有第一深度的第一沟渠；以及

形成于所述衬底的外围区域中的第二隔离结构，其中所述第二隔离结构包含具有第二深度的第二沟渠，且其中所述第一深度大于所述第二深度。

2. 根据权利要求 1 所述的元件，其特征在于所述第一隔离结构包含氧化硅。

3. 根据权利要求 1 所述的元件，其特征在于所述第一隔离结构包含的材料选自由绝缘材料、实质光学不透明材料、低折射率材料和其组合组成的群组。

4. 根据权利要求 1 所述的元件，其特征在于所述第一深度大于约 0.6 μm。

5. 根据权利要求 1 所述的元件，其特征在于所述衬底包含具第一导电型的外延层和具第二导电型的衬底层。

6. 根据权利要求 5 所述的元件，其特征在于所述衬底选自由包含 p-型的第一导电型和 p+型的第二导电型的衬底、包含 n-型的第一导电型和 n+型的第二导电型的衬底以及包含 n-型的第一导电型和 p+型的第二导电型的衬底组成的群组。

7. 一种图像传感器元件，其特征在于包含：

包含像素区域和外围区域的衬底；

形成于所述衬底的像素区域中的第一像素和第二像素；

第一沟渠隔离结构，其形成于所述衬底的像素区域中，且位于所述第一像素和第二像素之间，其中所述第一沟渠隔离结构具有第一深度；以及

第二沟渠隔离结构，其形成于所述外围区域中，所述第二沟渠隔离结构具有第二深度，所述第二深度小于所述第一深度。

8. 根据权利要求 7 所述的元件，其特征在于所述衬底包含具有第一导电型的外延层，且其中所述第一像素包含具有第二导电型的光电二极管。

9. 根据权利要求 7 所述的元件，其特征在于所述第一深度介于约 0.6 μm 与 1 μm 之间。

10. 根据权利要求 7 所述的元件，其特征在于所述第二深度为约 0.6 μm 或更小。

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图像传感器元件的隔离结构

技术领域

本揭示内容大体上涉及图像传感器，且明确地说，涉及包含集成电路的图像传感器，例如互补金属氧化物半导体（Complementary metal-oxide semiconductor；CMOS）图像传感器和电荷耦合元件（Charge coupled device；CCD）图像传感器。

背景技术

在半导体技术中，图像传感器用来感测投射于所述半导体衬底的曝光量。CMOS 传感器和 CCD 传感器均广泛使用于许多应用，如数码相机。这些图像传感器使用包含光线感测元件的像素矩阵以收集光能量并将图像转换成数字数据。然而，当像素尺寸缩小后，像素的敏感度将减低。另外，像素间的相互干扰（Crosstalk）将增加。相互干扰可减损空间分辨率、减低整体敏感度、提供不良颜色隔离，且可在图像中引入额外的噪声，特别是在色彩校正程序之后。包含这些需要较薄材料层（例如薄介电和金属层）的工艺和薄彩色滤光片可用来改善光学相互干扰。然而，这些传统改善电气相互干扰的方法（例如提供具有薄外延层的传感器）被提供用于例如静电放电（Electrostatic discharge；ESD）失败的其它问题。其它传统图像传感器的问题包含长波长光敏感度和图像缺陷，例如从兴盛效应（Blooming effect）（输出图像的特定区域显示较原始图像为亮）。

因此，需要经改进的图像传感器。

发明内容

本发明提供涉及半导体元件的揭示内容，特别是涉及图像传感器的隔离结构。所提出的新颖结构可以减低像素间的电气相互干扰和其它光学缺陷。

本发明提供一种图像传感器，其具有包含像素区域和外围区域的衬底、形成于所述衬底的像素区域中的第一隔离结构、形成于所述衬底的外围区域中的第二隔离结构。其中所述第一隔离结构包含具有第一深度的第一沟渠，所述第二隔离结构包含具有第二深度的第二沟渠，且其中所述第一深度大于所述第二深度。

换句话说，本发明提供一种图像传感器元件，所述元件包含具有像素区域和外围区域的衬底。隔离结构形成于衬底的像素区域中。所述隔离结构包含沟渠。另一隔离结构形成于所述衬底的外围区域中。所述隔离结构也包含沟渠。形成于像素区域中的沟渠与

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形成于外围区域中的沟渠相比具有较大深度。

另一方面，本发明提供另一种图像传感器元件，所述元件包含具有像素区域和外围区域的衬底。多个像素形成于所述像素区域的衬底中。在两个像素之间形成沟渠。所述沟渠具有第一深度。第二沟渠形成于所述衬底的外围区域中。所述第二沟渠的深度小于第一深度。

又一方面，本发明提供一种形成图像传感器的方法。提供包含像素区域和外围区域的衬底。第一隔离沟渠形成于所述衬底的像素区域中，形成所述第一隔离沟渠包含将所述衬底蚀刻到第一深度。第二隔离沟渠形成于所述衬底的外围区域中。形成所述第二隔离沟渠包含将所述衬底蚀刻到第二深度，所述第二深度小于所述第一深度。

附图说明

本发明所揭示的各方面最佳地由上述详细说明且通过读取附图加以了解。需强调的是，根据工业的标准实践，许多特征并未依照比例绘制。事实上，为了论述的明确，可任意增加或减少各项特征的尺寸。

图 1 是包含像素区域和外围区域的图像传感器的俯视图；

图 2 是包含像素矩阵和外围区域的常规图像传感器的剖视图；

图 3 是实施例的包含像素矩阵和外围区域的图像传感器的剖视图；

图 4 是展示制造图 3 的图像传感器的方法的实施例的流程图；

图 5a 到 5g 是图 4 方法实施例的剖视图；

图 6 是图 3 制造图像传感器方法的另一替代实施例的流程图；

图 7a 到 7e 是图 5 方法实施例的剖视图；以及

图 8 是包含像素矩阵和外围区域的图像传感器的替代实施例的剖视图。

具体实施方式

本揭示内容大体上涉及半导体元件，特别是图像传感器。然而，应了解，提供特定实施例作为范例以教示较广的发明观念，而所属领域的一般技术人员可轻易将本揭示内容的教示应用于其它方法或元件。另外，应了解，本揭示内容中所论述的方法和装置包含一些传统的结构和/或工艺。既然这些结构和工艺在所述领域中是众所周知的，那么将仅以一般详细程度对其进行论述。再者，为了方便和举例，在整个图式中重复参考标号，且所述重复在整个图式中并非指示任何需要的特征或步骤组合。而且，越过第二特征、在第二特征上方或耦合于第二特征形成第一特征在后续叙述中可包含这样的实施例，其中所述第一和第二特征直接接触形成；或可包含在第一与第二特征之间插入形成额外特

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征的实施例，如此所述第一和第二特征或许并非直接接触。再者，在衬底或衬底表面形成特征可包含在衬底表面上方、邻近于衬底表面、直接于衬底表面及/或延伸于衬底表面下方形成特征（例如植入区、沟渠）的实施例。

参看图 1，图像感测元件 100 提供像素区域 110 和外围区域 120。所述像素区域 110 包含像素 110a 的矩阵。在一实施例中，所述图像感测元件 100 可为互补金属氧化物半导体（CMOS）图像传感器（CIS）或主动像素传感器。在替代实施例中，所述图像传感器 100 可为电荷耦合元件（CCD）传感器。所述图像感测元件 100 可为前侧发光传感器或背侧发光传感器。在背侧发光传感器的结构中，被感测的光线入射到衬底背侧，而在衬底前侧形成像素。像素 110a 包含至少一光学检测器（例如光电二极管）以记录光线亮度或强度。在一实施例中，像素 110a 包含接脚光电二极管。各个像素 110a 还包含至少一个晶体管。所述像素 110a 包含复位（reset）晶体管、源极跟随器（source follower）晶体管、选择器（selector）晶体管和/或传输（transfer）晶体管。所述复位晶体管可执行对所述像素 110a 的复位。所述源极跟随器晶体管可允许电压与被观测像素 110a 结合而不移除累积电荷。所述选择器晶体管可以是行选择器晶体管，且当选择器晶体管开启时允许读取单行像素 110a。传输晶体管可将像素 110a 的光检测器中的累积电荷移动到另一元件，因此从像素输出数据。传输晶体管可允许关联的二次采样。在一实施例中，传输晶体管可结合（分派）于单一光电二极管，而源极跟随器、复位和选择器晶体管可结合于（共用于）多个光电二极管。在第二实施例中，传输晶体管可结合于光电二极管，而源极跟随器和复位晶体管可结合于多个光电二极管。在一实施例中，各像素 110 包含 4 个晶体管。所述图像传感器元件是所述领域中常用的 4T CMOS 图像传感器。所述 4T CMOS 图像传感器可包含传输晶体管、复位晶体管、源极跟随器晶体管和选择器晶体管。在一实施例中，包含于像素区域 110 中的晶体管包含金属氧化物半导体场效晶体管（MOSFET），其具有包含硅化物层的栅极。所述硅化物层可包含硅化物，例如镍硅化物、钴硅化物、钨硅化物、钽硅化物、钛硅化物、铂硅化物、铒硅化物、钯硅化物和/或其组合。

在外围区域 120 中，在邻近所述像素区域 110 处提供增加的电路和输入/输出，以提供像素 110a 的操作环境且/或支持与像素 110a 的外在沟通。所述外围区域 120 也可为逻辑区域，如同其可包含结合于像素 110a 的逻辑电路。所述外围区域 120 可包含低功率逻辑电路。所述低功率逻辑电路可包含低功率、高速、高效能逻辑电路。所述外围电路 120 可包含例如依序驱动像素、得到信号电荷的电路、A/D 转换器、形成图像输出信号的处理电路、可连接其它元件的电连接器和/或所述领域中常用的其它构件。在一实施例中，

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所述外围区域 120 包含具有源极、漏极和栅极电极的 MOSFET 元件，其均包含硅化物层。所述硅化物层可包含硅化物，例如镍硅化物、钴硅化物、钨硅化物、钽硅化物、钛硅化物、铂硅化物、铒硅化物、钯硅化物和/或其组合。

现参看图 2，其展示传统的图像传感器 200 的剖视图。所述图像传感器 200 包含像素区域 210 和外围区域 220。彩色滤光片 230 置于所述像素区域 210 上方。所述彩色滤光片 230 具有多个滤光片，包含蓝色滤光片 230a、绿色滤光片 230b、红色滤光片 230c 和蓝色滤光片 230d。所述传感器 200 包含具有次层 250a 和外延层 250b 的衬底 250。包含沟渠 260a、260b、260c 和 270 的多个沟渠形成于衬底 250 上。所述沟渠 260a、260b 和 260c 形成于像素区域 210 中。所述沟渠 270 形成于所述外围区域 220 中。所述沟渠 270 实质上类似于所述沟渠 260a、260b 和 260c。例如，所述沟渠 270 与沟渠 260a、260b 和 260c 具有实质上相同的深度 D1。一般来说，D1 介于 0.3 到 0.6 μm。

像素区域中的沟渠（包含 260a、260b 和 260c）用于分隔像素与第二像素。举例来说，沟渠 260b 用于分隔形成于所述红光滤光片 230c 下方的衬底 250 中（区域 P2）的像素与形成于所述绿光滤光片 230b 下方的衬底 250 中（区域 P1）的像素。所述沟渠 270 可用于分隔外围区域中的一个或一个以上构件。所述元件 200 具有沟渠 260a、260b 和/或 260c 可能无法适当分隔一个像素区域与另一个像素区域的缺点。所述沟渠 260a、260b 和/或 260c 的深度可能不足以防止来自第一像素区域（例如区域 P1）的光产生载子移动到第二像素区域（例如区域 P2）。这将导致电气相互干扰且减损所述传感器 200 的效能。因此，需要一种经改善的隔离结构。

参看图 3，其展示本发明实施例的图像传感器元件 300。所述图像传感器 300 包含具有次层 310a 和外延层 310b 的衬底 310，以及位于所述衬底 310 上方的彩色滤光片 320。所述图像传感器元件 300 可实质上与前述图 1 的图像传感器元件 100 相同。所述图像传感器元件 300 包含像素区域 302 和外围区域 304。多个像素（未图示）可形成于所述衬底 310 的像素区域 302 中。举例来说，第一像素可形成于区域 P3 中，且第二像素可形成于区域 P4 中。所述像素包含光检测器和一个或一个以上晶体管。所述图像传感器元件 300 的一个或一个以上像素可实质上类似于前述图 1 的像素 110a。所述外围区域 304 可实质上类似于前述图 1 所示的外围区域 120。

所述彩色滤光片 320 包含蓝光滤光片 320a 和 320d、绿光滤光片 320b 和红光滤光片 320c，虽然其它实施例的彩色滤光片也是可能的。在替代实施例中，所述图像感测元件 300 是背侧发光传感器。在一实施例中，所述彩色滤光片 320 设于邻近所述衬底 310 的

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背面处，且过滤入射于所述衬底 310 背侧的光线。可形成邻近所述彩色滤光片 320、相对于所述衬底 310 的一个或一个以上微透镜（未图示）。

所述衬底 310 可以是具结晶结构的硅。在替代实施例中，所述衬底 310 可包含其它基础半导体（如锗（germanium）），或可包含化合物半导体（如硅碳化物、镓砷化物、铟砷化物和铟磷化物）。在一实施例中，所述衬底 310 是 P 型衬底（P 导电型）（例如以传统的扩散或离子植入掺杂 P 型掺杂物（如硼或铝）的衬底）。在其它实施例中，所述衬底 310 可包含 P+衬底、N+衬底和/或其它所述领域已知的导电型。所述衬底 310 可包含绝缘层上硅（SOI）衬底。所述外延层 310b 与衬底 310 的其它部分（包含次层 310a）相比允许不同的掺杂形貌。所述外延层 310b 可使用传统方法来成长于所述衬底 310 上。在一实施例中，所述外延层 310b 为 p-外延层。在一实施例中，所述次层 310a 为 p+层。可能的实施例包含所述外延层 310b 为 N-外延层且所述次层 310a 为 N+次层，所述外延层 310b 为 N-外延层且所述次层 310a 为 P+次层，和/或其它所述领域中常用的导电型。外延层 310b 的厚度 T 可介于大约 2 μm 与 10 μm 之间。在另一实施例中，外延层的厚度 T 可大约为 4 μm。

在一实施例中，所述外延层 310b 为 p 型导电型，且形成在衬底 310 中的像素（未图示）中所包含的光电二极管包含具有 N 型光产生区域（例如形成于 P 型外延层的 N 型阱）的光检测器。所述 N 型光产生区域可利用将 N 型掺杂物（如磷、砷和/或其它所述领域常用的 N 型掺杂物）掺杂于所述衬底来形成。所述掺杂可利用所述领域已知的传统工艺（如光刻图案化接着离子植入或扩散）来实现。在其它实施例中，所述光电二极管包含接脚光电二极管。所述接脚层可掺杂 p 型掺杂物。所述 p 型掺杂物可包含硼、铝和/或其它所述领域常用的 P 型导电型掺杂物。

包含隔离沟渠 340 的隔离结构形成于所述图像传感器 300 的外围区域 304 中。所述隔离沟渠 340 可包含浅沟渠隔离（STI）结构。所述隔离沟渠 340 可协助隔离一个或一个以上形成于所述外围区域 304 上的构件。所述隔离沟渠 340 的深度 D2 小于大约 0.6 μm。在一实施例中，所述隔离沟渠 340 的深度 D2 介于大约 0.3 μm 到 0.6 μm。较深的深度 D2（例如大于 0.6μm）可提供位于所述外围区域 304 的 N 型阱接合的高片电阻（Rs）。较高的 Rs 可减损拾取（Pick-up）功能。所述隔离沟渠 340 可包含氧化硅。在一实施例中，除氧化硅以外或替代氧化硅，隔离沟渠 340 可包含空气。所述沟渠 340 包含其它隔离材料的其它实施例也是可行的。所述隔离沟渠 340 可由所述领域中常用的传统方法形成。例如，利用传统的工艺（如根据传统光刻工艺形成的图案的反应式离子蚀刻（RIE））在衬

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底 310 的外围区域 304 中进行孔洞蚀刻。所述孔洞可接着被填满。例如在一实施例中，所述沟渠被填入氧化硅。在一实施例中，所述工艺包含氧化硅的高密度等离子体化学气相沉积（High Density Plasma Chemical Vapor Deposition；HDPCVD）以填入孔洞，并接着进行化学机械抛光（Chemical Mechanical Polish；CMP）工艺以平坦化所述氧化物。在替代实施例中，所述工艺包含氧化硅的次大气化学气相沉积（Sub-Atmospheric Chemical Vapor Deposition；SACVD），并接着进行化学机械抛光工艺以平坦化所述氧化物。形成所述隔离沟渠 340 的方法将随后进行更详细论述。

包含隔离沟渠 330a、330b 和 330c 的多个隔离结构形成于衬底 310 的像素区域 302 中。所述隔离沟渠 330a、330b 和 330c 可包含浅沟渠隔离（STI）结构。所述隔离沟渠 330a、330b 和/或 330c 至少部分将像素与所述像素区域 302 的第二像素隔离。例如，所述隔离沟渠 330b 提供阻隔少数载子从像素区域 P3 到达像素区域 P4。所述隔离沟渠 330a、330b 和/或 330c 的深度 D3 大于大约 0.6μm。在一实施例中，所述隔离沟渠 330a、330b 和/或 330c 可具有介于大约 0.6μm 到 2μm 的深度 D3。在一实施例中，所述隔离沟渠 330a、330b 和/或 330c 可具有介于大约 0.6 μm 到 1 μm 的深度 D3。在一实施例中，所述隔离沟渠 330a、330b 和/或 330c 可具有介于大约 1 μm 到 2μm 的深度 D3。

所述隔离沟渠 330a、330b 和/或 330c 可包含（例如完全填满或部分填入）绝缘材料。所述绝缘材料（如氧化硅）可隔离少数载子从像素到达第二像素。在替代实施例中，所述隔离沟渠 330a、330b 和/或 330c 可填入氧化物、实质光学不透明材料和/或低折射率材料，其将参看图 7 在随后详细叙述。所述隔离沟渠 330a、330b 和/或 330c 可利用所述领域常用的传统技术形成。例如，利用传统的工艺（如执行于传统光刻工艺形成的图案后的反应式离子蚀刻（RIE））在衬底 310 的像素区域 302 中进行孔洞蚀刻。所述孔洞可接着被填满。例如在一实施例中，所述沟渠被填入氧化硅。在一实施例中，所述工艺包含氧化硅的高密度等离子体化学气相沉积以填入孔洞，并接着进行化学机械抛光工艺以平坦化所述氧化物。在替代实施例中，所述工艺包含氧化硅的次大气化学气相沉积，并接着进行化学机械抛光工艺以平坦化所述氧化物。形成所述隔离沟渠 330a、330b 和 330c 的方法将随后进行更详细论述。

图 4 展示形成包含隔离结构的图像传感器的方法 400。图 5a、5b、5c、5d、5e 和 5f 展示衬底 500 的持续改变，其对应于图 4 的步骤。所述方法 400 可用于制造实质上类似于图 3 所述的图像传感器 300 的图像传感器元件。

方法 400 起始于步骤 402，提供包含像素区域和外围区域的衬底。所述衬底还包含

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外延层。所提供的衬底可实质上类似于前述图 3 的衬底 310。在图 5a 的例子中，提供衬底 500。衬底 500 包含次层 502 和外延层 504。在一实施例中，所述次层 502 为 P+层，而外延层 504 可为 P-层。所述衬底 500 进一步包含像素区域 500a 和外围区域 500b。所述像素区域 500a 可实质上类似于图 1 和 3 分别所示的像素区域 110 和/或像素区域 302。所述外围区域 500b 可实质上类似于图 1 和图 3 分别所示的外围区域 120 和/或外围区域 304。

方法 400 接着进行步骤 404，其中在衬底的像素区域中形成多个隔离结构。所述隔离结构包含隔离沟渠。所述沟渠形成的深度大于大约 0.6 μm。所述沟渠可利用所述领域常用的工艺形成（如光刻图案化伴随 RIE 蚀刻）以在图案化区域中形成孔洞（沟渠）。在图 5b 的例子中，沟渠 510 蚀刻于衬底 500 中，而更精确地说是在衬底 500 的外延层 504 中。所述沟渠 510 被蚀刻到深度 D4。D4 可介于大约 0.6 μm 到 2 μm。

方法 400 进行步骤 406，其中在所述衬底上形成绝缘材料层。所述层可由沉积材料制成，其使用化学气相沉积、等离子体增强化学气相沉积（Plasma Enhanced Chemical Vapor Deposition；PECVD）、大气压化学气相沉积（Atmospheric Pressure Chemical Vapor Deposition；APCVD）、低压（Low Pressure）化学气相沉积、高密度等离子体化学气相沉积、原子层（Atomic Layer）化学气相沉积、次气压化学气相沉积（Sub-atmospheric Chemical Vapor Deposition；SACVD）和/或其它所述领域常用的工艺。在一实施例中，所述隔离材料是氧化硅。在一实施例中，所述氧化物由 HDPCVD 或 SACVD 沉积。所述层可部分或完全填入如先前关于步骤 404 所述的像素区域的沟渠。在图 5c 的例子中，顺应形貌的绝缘层 520 沉积于所述衬底 500 上。所述绝缘层 520 填入所述沟渠 510，其现在被指定为隔离沟渠 510a。所述方法接着进行步骤 408，其中将所述绝缘层进行平坦化。在一实施例中，所述层利用化学机械抛光工艺进行平坦化。图 5d 的例子展示平坦化后的绝缘材料层 520，因此所述绝缘材料完全填入所述隔离沟渠 510a 中，且提供衬底 500 的实质平面。

方法 400 进行步骤 410，其中在所述衬底的外围区域中形成至少一隔离结构。所述隔离结构包含隔离沟渠。沟渠蚀刻的深度小于步骤 404 所述形成于像素区域的沟渠的深度。所述沟渠的蚀刻深度可小于大约 0.6 μm。所述沟渠可利用所述领域常用的工艺来蚀刻形成，如光刻图案化后伴随 RIE 蚀刻以根据图案化区域形成孔洞（沟渠）。在图 5e 的例子中，沟渠 530 蚀刻于衬底 500 的外围区域 500b 中，而更精确地说是在衬底 500 的外延层 504 中。所述沟渠 530 被蚀刻到深度 D5。D5 小于图 5b 所示的 D4。在一实施例中，

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D5 小于大约 0.6 μm。所述方法 400 进行到步骤 412，其中在所述衬底上沉积顺应形貌的绝缘材料层。所述层如步骤 410 所述可完全或部分填入所述外围区域的沟渠。所述绝缘材料层可由物理气相沉积（Physical Vapor Deposition：PVD）（溅镀（Sputtering））、化学气相沉积、等离子体增强化学气相沉积、大气压化学气相沉积、低压化学气相沉积、高密度等离子体化学气相沉积（HDPCVD）、原子层化学气相沉积、次气压化学气相沉积（SACVD）和/或其它所述领域常用的工艺进行沉积。在一实施例中，所述绝缘材料是氧化硅。在另一实施例中，所述氧化物由 HDPCVD 或 SACVD 沉积。在图 5f 的例子中，绝缘材料的顺应形貌层 540 沉积在所述衬底 500 上，并包含填入所述沟渠 530。所述方法 400 进行到步骤 414，其中将所述绝缘层进行平坦化。在一实施例中，所述绝缘层利用化学机械抛光工艺进行平坦化。图 5g 的例子展示平坦化后的绝缘材料层 540，因此所述绝缘材料填入所述沟渠 530 中，且提供衬底 500 的实质平面。在一实施例中，所述绝缘层 540 包含氧化硅。

参看图 6，其展示制造图像传感器元件的方法 600；图 7a、7b、7c、7d 和 7e 展示衬底 700 的持续改变，其对应于图 6 的步骤。所述方法 600 可用于制造实质上类似于图 3 所述的图像传感器 300 的图像传感器元件。

方法 600 起始于步骤 602，提供包含像素区域和外围区域的衬底。所述衬底还包含外延层。所提供的衬底可实质上类似于前述图 3 的衬底 310。在图 7a 的例子中，提供衬底 700。衬底 700 包含次层 702 和外延层 704。在一实施例中，所述次层 702 为 P+层，而外延层 704 可为 P-层。所述衬底 700 进一步包含像素区域 700a 和外围区域 700b。所述像素区域 700a 可实质上类似于图 1 和 3 分别所示的像素区域 110 和/或像素区域 302。所述外围区域 700b 可实质上类似于图 1 和图 3 分别所示的外围区域 120 和/或外围区域 304。

方法 600 接着进行步骤 604，其中在衬底的像素区域中形成多个隔离结构。所述隔离结构包含隔离沟渠。所述沟渠可形成于所述衬底的深度大于 0.6 μm。所述沟渠可利用所述领域常用的工艺形成，如在光刻图案化后根据所述图案化 RIE 进行蚀刻，以形成孔洞（沟渠）。在图 7b 的例子中，沟渠 710 蚀刻于衬底 700 中，而更精确地说是在衬底 700 的外延层 704 中。所述沟渠 710 被蚀刻到深度 D6。D6 大于 0.6 μm。在一实施例中，D6 介于大约 0.6 μm 到 2 μm。

方法 600 进行步骤 606，其中在所述衬底的外围区域中形成至少一隔离结构。所述隔离结构包含隔离沟渠。所述沟渠的形成深度可小于 0.6 μm。所述沟渠蚀刻的深度小于

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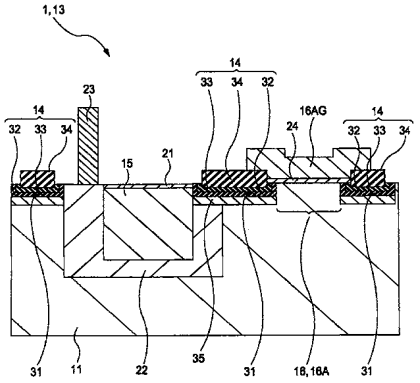
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(54)发明名称

固态成像装置、固态成像装置的制造方法和成像设备

(57)摘要

本发明涉及固态成像装置、固态成像装置的制造方法和成像设备。该固态成像装置在半导体基板上包括具有多个像素的像素部分，所述像素部分设置有：光电转换部分，对入射光进行光电转换以获得信号电荷；和像素晶体管部分，将从光电转换部分读取的信号电荷转换成电压，其中布置在像素部分中的元件隔离区域包括埋入布置在半导体基板中的沟槽中的绝缘膜，并且该绝缘膜包括具有负电荷的绝缘膜。



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1. 一种固态成像装置，其在半导体基板上包括具有多个像素的像素部分，所述像素部分设置有：

光电转换部分，对入射光进行光电转换以获得信号电荷；和

像素晶体管部分，将从光电转换部分读取的信号电荷转换成电压，

其中，布置在所述像素部分中的元件隔离区域包括埋入布置在所述半导体基板中的沟槽中的绝缘膜，并且

所述绝缘膜包括具有负电荷的绝缘膜。

2. 根据权利要求 1 的固态成像装置，

其中，所述元件隔离区域至少将所述像素彼此隔离。

3. 根据权利要求 1 的固态成像装置，

其中，所述具有负电荷的绝缘膜是包含从包括以下元素的组中选择的至少一种元素的绝缘膜：铪、锆、铝、钽、钛、钇和镧系元素。

4. 根据权利要求 1 的固态成像装置，

其中，P 型杂质区域布置在所述元件隔离区域下方的半导体基板中。

5. 根据权利要求 4 的固态成像装置，

其中，所述 P 型杂质区域的电势是固定的。

6. 一种固态成像装置的制造方法，该方法按顺序包括如下步骤：

在半导体基板的像素区域中形成用于进行元件隔离的第一沟槽，并且在周边电路区域中形成用于进行元件隔离的第二沟槽；

在第一沟槽和第二沟槽的内表面上形成具有负电荷的绝缘膜，其中氧化硅膜位于第一沟槽和第二沟槽的内表面与具有负电荷的绝缘膜之间；

去除布置在周边电路区域中并具有负电荷的绝缘膜；

使得第二沟槽深于第一沟槽；以及

将埋入式绝缘膜埋入第一沟槽和第二沟槽中，以在第一沟槽中形成第一元件隔离区域并且在第二沟槽中形成第二元件隔离区域。

7. 根据权利要求 6 的固态成像装置的制造方法，

其中，在去除具有负电荷的绝缘膜之后并且在将埋入式绝缘膜埋入第一沟槽和第二沟槽中之前，在第一沟槽底部的半导体基板中形成 P 型杂质区域。

8. 一种固态成像装置的制造方法，该方法按顺序包括如下步骤：

在半导体基板的像素区域中形成用于进行元件隔离的第一沟槽，并且在周边电路区域中形成用于进行元件隔离的第二沟槽；

在对第一沟槽加掩模的同时使得第二沟槽深于第一沟槽；

在第一沟槽和第二沟槽的内表面上形成具有负电荷的绝缘膜，其中氧化硅膜位于第一沟槽和第二沟槽的内表面与具有负电荷的绝缘膜之间；

去除布置在周边电路区域中并具有负电荷的绝缘膜；以及

将埋入式绝缘膜埋入第一沟槽和第二沟槽中，以在第一沟槽中形成第一元件隔离区域并且在第二沟槽中形成第二元件隔离区域。

9. 根据权利要求 8 的固态成像装置的制造方法，

其中，在去除具有负电荷的绝缘膜之后并在将埋入式绝缘膜埋入第一沟槽和第二沟槽

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中之前，在第一沟槽底部的半导体基板中形成 P 型杂质区域。

10. 一种固态成像装置的制造方法，该方法按顺序包括如下步骤：

在包括半导体基板的基板的周边电路区域中形成用于进行元件隔离的第一沟槽；

将第一埋入式绝缘膜埋入到第一沟槽中以形成第一元件隔离区域；

在基板上形成覆盖第一元件隔离区域的绝缘膜；

在设置有所述绝缘膜的半导体基板的像素区域中形成用于进行元件隔离的第二沟槽；

在第二沟槽的内表面上形成具有负电荷的绝缘膜，其中氧化硅膜位于第二沟槽的内表面与具有负电荷的绝缘膜之间；以及

将第二埋入式绝缘膜埋入第二沟槽中以形成第二元件隔离区域。

11. 根据权利要求 10 的固态成像装置的制造方法，

其中，在形成第二沟槽之后并且在将第二埋入式绝缘膜埋入第二沟槽中之前，在第二沟槽底部的半导体基板中形成 P 型杂质区域。

12. 一种固态成像装置的制造方法，该方法按顺序包括如下步骤：

在半导体基板的像素区域中形成用于进行元件隔离的第一沟槽，并且在周边电路区域中形成用于进行元件隔离的第二沟槽；

在对第一沟槽加掩模的同时使得第二沟槽深于第一沟槽；

在第一沟槽和第二沟槽的内表面上形成具有负电荷的绝缘膜，其中氧化硅膜位于第一沟槽和第二沟槽的内表面与具有负电荷的绝缘膜之间；以及

将埋入式绝缘膜埋入第一沟槽和第二沟槽中，以在第一沟槽中形成第一元件隔离区域并在第二沟槽中形成第二元件隔离区域。

13. 根据权利要求 12 的固态成像装置的制造方法，

其中，在去除具有负电荷的绝缘膜之后并且在埋入埋入式绝缘膜之前，在第一沟槽底部的半导体基板中形成 P 型杂质区域。

14. 一种成像设备，包括：

图像聚焦光学部分，对入射光进行会聚；

成像部分，包括固态成像装置，用于接收由图像聚焦光学部分会聚的光并对其进行光电转换；以及

信号处理部分，对进行了光电转换的信号进行处理，

其中，所述固态成像装置在半导体基板上包括像素部分，所述像素部分设置有：

光电转换部分，对入射光进行光电转换以获得信号电荷；和

像素晶体管部分，将从光电转换部分读取的信号电荷转换成电压，

布置在所述像素部分中的元件隔离区域包括埋入布置在所述半导体基板中的沟槽中的绝缘膜，并且

所述绝缘膜包括具有负电荷的绝缘膜。

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固态成像装置、固态成像装置的制造方法和成像设备

技术领域

[0001] 本发明涉及固态成像装置、该固态成像装置的制造方法以及成像设备。

背景技术

[0002] 近年来，通常，在细小半导体集成电路中使用浅沟槽隔离 (STI) 进行元件隔离。然而，由于通过在半导体基板中深挖沟槽来提供 STI，所以在埋入沟槽中的用于进行元件隔离的绝缘膜与半导体基板之间的界面处出现晶体缺陷或界面态 (interface state)，从而变成噪声源。因此，关于 CMOS 图像传感器，在采用 STI 作为并行于周边电路的像素部分的元件隔离方法的情况下，以如下方式出现特性劣化：在被挖掘的半导体基板与埋入式绝缘膜之间的界面处产生噪声。因此，提出下面这种方法作为减小由于噪声导致的固态成像元件的劣化的技术，在该方法中减小像素区域的元件隔离区域中的半导体基板的挖掘量，从而抑制从元件隔离端产生噪声（例如，参照日本未审专利申请公报 No. 2006-24786 和日本未审专利申请公报 No. 2006-93319）。

[0003] 然而，即使在应用上述的减小像素部分的元件隔离的挖掘量的元件隔离方法的情况下，如图 13 和图 14 所示，也需要通过引入 P 型杂质在像素部分 111 的元件隔离区域 112 下形成空穴累积层 113。上述的图 13 示出了像素部分的平面布局，图 14 是示出沿图 13 所示的线 XIV-XIV 剖开的、像素部分的截面的截面图。

[0004] 结果，由于像素变得更加细小，空穴累积层 113 的杂质的扩散的影响变得明显，并且由于 P 型杂质的扩散影响，减小了复位晶体管 114R、放大晶体管 114A、选择晶体管 114S 的有效沟道宽度。如果如上所述减小了有效沟道宽度，则尤其放大晶体管 114A 的 1/f 噪声的劣化是成问题的。

[0005] 另外，由于使像素变得更加细小，所以难以增加沟道宽度。

[0006] 因此，难以确保降噪与细小像素之间的兼容性。

[0007] 此外，提出了一种方法，其中为了抑制在 STI 结构的元件隔离区域中产生噪声，在 STI 中埋入用于施加电压的导体以使得用于进行元件隔离的绝缘膜与半导体基板之间的界面进入空穴累积状态（例如，参照日本未审专利申请公报 No. 2006-120804）。

[0008] 在将用于施加电压的导体埋入上述 STI 中的方法中，需要在元件隔离区域中埋入用于施加负电压的导体。此时，需要将该导体埋入元件隔离区域中，尤其是像素区域的选择晶体管和放大晶体管附近的元件隔离区域中，以避免与用作晶体管的栅电极的多晶硅电导通。然而，难以在避开栅电极的多晶硅的同时在细小像素的像素区域的整个元件隔离区域埋入该导体。因此，对于抑制 1/f 噪声的劣化以及减小像素的晶体管的沟道的效果的目的，难以通过埋入导体来获得劣化抑制效果。

发明内容

[0009] 本发明的发明人认识到，由于像素变得更加细小而难以增大沟道宽度，并且如果减小了有效沟通宽度，则像素晶体管部分尤其是放大晶体管的 1/f 噪声劣化，因此很难获

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得降噪与细小像素之间的兼容性。

[0010] 期望噪声减小与细小像素可以互相兼容。

[0011] 提供了一种根据本发明的实施例的固态成像装置，其在半导体基板上包括具有多个像素的像素部分，所述像素部分包括：光电转换部分，对入射光进行光电转换以获得信号电荷；以及像素晶体管部分，将从上述光电转换部分读取的信号电荷转换成电压，其中，布置在上述像素部分中的元件隔离区域包括埋入布置在上述半导体基板中的沟槽中的绝缘膜，并且上述绝缘膜包括具有负电荷的绝缘膜。

[0012] 在根据本发明的实施例的固态成像装置中，布置在像素部分中的元件隔离区域包括具有负电荷的绝缘膜。因此，在紧邻元件隔离区域位于下方的半导体基板中产生由具有负电荷的绝缘膜中的负电荷生成的空穴累积层。通过该空穴累积层抑制了由元件隔离区域与半导体基板之间的界面处的缺陷导致的噪声产生。另外，由于通过负电荷形成空穴累积层，所以可以省去现有技术中的在紧邻元件隔离区域位于下方的半导体基板中形成的 P 型杂质区域。作为另一选择，在形成 P 型杂质区域的情况下，可以减小它的浓度。因此，抑制了由于 P 型杂质区域的 P 型杂质的扩散导致的像素晶体管部分中的晶体管的有效沟道宽度的减小，由此可以确保足够的有效沟道宽度。因此，减小了像素晶体管部分中的晶体管的 1/f 噪声。换言之，抑制了由于 P 型杂质区域导致的 P 型杂质的扩散并且相应减小了像素尺寸，同时确保了有效沟道宽度并且减小了 1/f 噪声。

[0013] 本发明提供了一种根据本发明的实施例的固态成像装置的制造方法（第一制造方法），该方法按顺序包括如下步骤：在半导体基板的像素区域中形成用于进行元件隔离的第一沟槽，并且在周边电路区域中形成用于进行元件隔离的第二沟槽；在上述第一沟槽和上述第二沟槽的内表面上形成具有负电荷的绝缘膜，其中氧化硅膜位于第一沟槽和第二沟槽的内表面与具有负电荷的绝缘膜之间；去除布置在上述周边电路区域中并具有负电荷的上述绝缘膜；使得上述第二沟槽深于第一沟槽；以及将埋入式绝缘膜埋入上述第一沟槽和上述第二沟槽中，以在上述第一沟槽中形成第一元件隔离区域并且在上述第二沟槽中形成第二元件隔离区域。

[0014] 本发明提供了一种根据本发明的实施例的固态成像装置的制造方法（第二制造方法），该方法按顺序包括如下步骤：在半导体基板的像素区域中形成用于进行元件隔离的第一沟槽，并且在周边电路区域中形成用于进行元件隔离的第二沟槽；使得上述第二沟槽深于上述第一沟槽，同时对上述第一沟槽加掩模；在上述第一沟槽和上述第二沟槽的内表面上形成具有负电荷的绝缘膜，其中氧化硅膜位于第一沟槽和第二沟槽的内表面与具有负电荷的绝缘膜之间；去除布置在上述周边电路区域中并具有负电荷的上述绝缘膜；以及将埋入式绝缘膜埋入上述第一沟槽和上述第二沟槽中，以在上述第一沟槽中形成第一元件隔离区域并且在上述第二沟槽中形成第二元件隔离区域。

[0015] 本发明提供了一种根据本发明的实施例的固态成像装置的制造方法（第三制造方法），该方法按顺序包括如下步骤：在包括半导体基板的基板的周边电路区域中形成用于进行元件隔离的第一沟槽；将第一埋入式绝缘膜埋入到上述第一沟槽中以形成第一元件隔离区域；在上述基板上形成覆盖上述第一元件隔离区域的绝缘膜；在设置有上述绝缘膜的上述半导体基板的像素区域中形成用于进行元件隔离的第二沟槽；在上述第二沟槽的内表面上形成具有负电荷的绝缘膜，其中氧化硅膜位于第二沟槽的内表面与具有负电荷的绝

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缘膜之间；以及将第二埋入式绝缘膜埋入上述第二沟槽中以形成第二元件隔离区域。

[0016] 本发明提供了一种根据本发明的实施例的固态成像装置的制造方法（第四制造方法），该方法按顺序包括如下步骤：在半导体基板的像素区域中形成用于进行元件隔离的第一沟槽，并且在周边电路区域中形成用于进行元件隔离的第二沟槽；使得上述第二沟槽深于上述第一沟槽，同时对山数第一沟槽加掩模；在上述第一沟槽和上述第二沟槽的内表面上形成具有负电荷的绝缘膜，其中氧化硅膜位于第一沟槽和第二沟槽的内表面与具有负电荷的绝缘膜之间；以及将埋入式绝缘膜埋入上述第一沟槽和上述第二沟槽中，以在上述第一沟槽中形成第一元件隔离区域并在上述第二沟槽中形成第二元件隔离区域。

[0017] 在根据本发明的实施例的固态成像装置的各制造方法中，在布置在像素部分中的元件隔离区域中形成具有负电荷的绝缘膜。因此，在紧邻元件隔离区域位于下方的半导体基板中产生由具有负电荷的绝缘膜中的负电荷生成的空穴累积层。通过该空穴累积层抑制了由元件隔离区域与半导体基板之间的界面处的缺陷导致的噪声产生。另外，由于通过负电荷形成空穴累积层，所以可以省去现有技术中的在紧邻元件隔离区域位于下方的半导体基板中形成的 P 型杂质区域。作为另一选择，在形成 P 型杂质区域的情况下，可以减小它的浓度。因此，抑制了由于 P 型杂质区域的 P 型杂质的扩散导致的像素晶体管部分中的晶体管的有效沟道宽度的减小，由此可以确保足够的有效沟道宽度。因此，减小了像素晶体管部分中的晶体管的 1/f 噪声。换言之，抑制了由于 P 型杂质区域导致的 P 型杂质的扩散并且相应减小了像素尺寸，同时确保了有效沟道宽度并且减小了 1/f 噪声。

[0018] 本发明提供了一种根据本发明的实施例的成像设备，包括：图像聚焦光学部分，对入射光进行会聚；成像部分，包括固态成像装置，用于接收由上述图像聚焦光学部分会聚的光并对其进行光电转换；以及信号处理部分，对进行了光电转换的信号进行处理，其中，上述固态成像装置在半导体基板上包括像素部分。所述像素部分设置有：光电转换部分，对入射光进行光电转换以获得信号电荷；和像素晶体管部分，将从上述光电转换部分读取的信号电荷转换成电压。布置在上述像素部分中的元件隔离区域包括埋入布置在上述半导体基板中的沟槽中的绝缘膜，并且上述绝缘膜包括具有负电荷的绝缘膜。

[0019] 在根据本发明的实施例的成像设备中，采用根据本发明的实施例的固态成像装置。因此，抑制了固态成像装置的像素晶体管部分中的晶体管的有效沟道宽度的减小，由此减小了像素晶体管部分中的晶体管的 1/f 噪声。

[0020] 关于根据本发明的实施例的固态成像装置，抑制了由于 P 型杂质区域导致的 P 型杂质的扩散并且可以相应减小了像素尺寸，同时确保有效沟道宽度并且减小了 1/f 噪声。因此，噪声抑制与细小像素可以相互兼容。因此，存在提高成像的图像质量的优点。

[0021] 关于根据本发明的实施例的固态成像装置的各制造方法，抑制了由于 P 型杂质区域导致的 P 型杂质的扩散并且可以相应减小了像素尺寸，同时确保有效沟道宽度并且减小了 1/f 噪声。因此，噪声抑制与细小像素可以相互兼容。因此，存在提高成像的图像质量的优点。

[0022] 关于根据本发明的实施例的成像设备，由于采用了根据本发明的实施例的降噪与细小像素可以兼得的固态成像装置，所以存在由于更高图像质量和更高灵敏度而提高了成像的图像质量的优点。

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附图说明

[0023] 图 1 是示出根据本发明的第一实施例的固态成像装置的示例的示意性结构截面图；

[0024] 图 2A 和图 2B 分别是示出根据本发明的第一实施例的固态成像装置的示例的平面布局图和电路图；

[0025] 图 3A 到图 3E 是示出根据本发明的第二实施例的固态成像装置的制造方法的第一示例的生产步骤的截面图；

[0026] 图 4A 到图 4E 是示出根据本发明的第二实施例的固态成像装置的制造方法的第一示例的生产步骤的截面图；

[0027] 图 5A 到图 5E 是示出根据本发明的第三实施例的固态成像装置的制造方法的第二示例的生产步骤的截面图；

[0028] 图 6A 到图 6F 是示出根据本发明的第三实施例的固态成像装置的制造方法的第二示例的生产步骤的截面图；

[0029] 图 7A 到图 7E 是示出根据本发明的第四实施例的固态成像装置的制造方法的第三示例的生产步骤的截面图；

[0030] 图 8A 到图 8D 是示出根据本发明的第四实施例的固态成像装置的制造方法的第三示例的生产步骤的截面图；

[0031] 图 9A 到图 9C 是示出根据本发明的第四实施例的固态成像装置的制造方法的第三示例的生产步骤的截面图；

[0032] 图 10A 到图 10E 是示出根据本发明的第五实施例的固态成像装置的制造方法的第四示例的生产步骤的截面图；

[0033] 图 11A 到图 11D 是示出根据本发明的第五实施例的固态成像装置的制造方法的第四示例的生产步骤的截面图；

[0034] 图 12 是示出根据本发明的第六实施例的成像设备的示例的框图；

[0035] 图 13 是现有技术中的固态成像装置的示例的示意性结构截面图；以及

[0036] 图 14 是示出现有技术中的固态成像装置的示例的平面布局图。

具体实施方式

[0037] 将在下面描述执行本发明的优选实施例（下文中称作实施例）。

[0038] 第一实施例

[0039] 固态成像装置的结构的一个示例

[0040] 将参照图 1 所示的示意性结构截面图、图 2A 所示的平面布局图以及图 2B 所示的电路图来描述根据本发明的第一实施例的固态成像装置的结构的一个示例。图 1 是示意性示出了沿图 2A 所示的线 I-I 剖开的截面的图。

[0041] 如图 2A 和 2B 所示，根据本发明的实施例的固态成像装置 1 包括像素部分 12 以及位于像素部分 12 的周边的周边电路部分（附图中没有示出），在像素部分 12 中在半导体基板 11 上布置有多个像素 13（在附图中示出了一个典型像素）。另外，上述的像素部分 12 包括用于隔离各个像素 13 的元件隔离区域 14。此外，上述的像素部分 12 和周边电路部分被除上述的元件隔离区域 14 以外的元件隔离区域（附图中没有示出）隔离。

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[0042] 上述像素 13 包括光电转换部分 15 和像素晶体管部分 16。

[0043] 上述光电转换部分 15 对入射光进行光电转换以获得信号电荷，并且例如由光电二极管形成光电转换部分 15。

[0044] 上述像素晶体管部分 16 将从上述光电转换部分 15 读取的信号电荷转换成电压。例如，从上述光电转换部分 15 一侧依次布置有转移晶体管（可以称作读取晶体管）16T、复位晶体管 16R、放大晶体管 16A 和选择晶体管 16S。在这点上，上述转移晶体管 16T 和上述复位晶体管 16R 共有的扩散层构成了浮动扩散区 FD。浮动扩散区 FD 连接到放大晶体管 16A 的栅电极 16AG（图 2A 中没有示出）。

[0045] 此外，上述周边电路部分包括像素垂直扫描电路、水平扫描电路、驱动电路、定时产生电路等。

[0046] 将在下文中参照图 1 详细描述上述像素 13。在图 1 中，放大晶体管 16A 被显示为像素晶体管部分 16 的代表。

[0047] 如图 1 所示，被元件隔离区域 14 隔离的光电转换部分 15 和像素晶体管部分 16（放大晶体管 16A 以及附图中没有示出的复位晶体管、选择晶体管等）布置在半导体基板 11 上。

[0048] P 型扩散层 21 布置在上述光电转换部分 15 的表面上以抑制噪声。

[0049] 另外，P 型扩散层 22 布置在上述光电转换部分 15 的周围以将光电转换部分 15 与周围隔离。电极部分 23 布置在 P 型扩散层 22 上以将 P 型扩散层 22 的电势固定在恒定值。

[0050] 关于上述的放大晶体管 16A，栅电极 16AG 布置在半导体基板 11 上，栅极绝缘膜 24 位于半导体基板 11 与栅电极 16AG 之间，并且源极 - 漏极区域（附图中没有示出）布置在该栅电极 16AG 的两侧（沟道长度方向：与图垂直的方向）。尽管附图中没有示出，但是复位晶体管、选择晶体管和转移晶体管具有相似的结构。然而，关于转移晶体管，源极 - 漏极区域之一还用作光电转换部分的 N 型区域，而另一个区域用作浮动扩散区 FD（参照图 2A）。

[0051] 上述的元件隔离区域 14 布置在沟槽 31 上，用以对布置在半导体基板 11 中的沟槽 31 进行填充。也就是说，氧化硅膜 32 布置在上述沟槽 31 的内表面上，具有负电荷的绝缘膜 33 布置在氧化硅膜 32 的表面上。另外，埋入式绝缘膜 34 布置在沟槽 31 中，其中上述的氧化硅膜 32 和具有负电荷的绝缘膜 33 布置在绝缘膜 34 与沟槽 31 之间，从而使得绝缘膜 34 具有高于半导体基板 11 的表面的高度。

[0052] 例如由氧化铪 (HfO_2) 膜、氧化锆 (ZrO_2) 膜、氧化铝 (Al_2O_3) 膜、氧化钽 (Ta_2O_5) 膜、氧化钛 (TiO_2) 膜或者氧化钇 (Y_2O_3) 膜形成上述的具有负电荷的绝缘膜 33。

[0053] 对于上述的具有负电荷的绝缘膜 33，可以使用通过化学气相沉积法、喷溅法、原子层沉积 (ALD) 法等形成的膜。然而，具有与基板的良好界面并且通过原子层沉积方法形成的膜是有利的。

[0054] 另外，由于在形成膜的同时可以形成用于减小界面态的大约 1nm 的氧化硅 (SiO_2) 层，所以利用原子层沉积法是有利的。在这种情况下，可以省去上述的氧化硅膜 32 的形成。

[0055] 除了上述的材料以外的材料的示例包括：镧系元素氧化物，例如氧化镧 (La_2O_3)、氧化铈 (CeO_2)、氧化镨 (Pr_2O_3)、氧化钕 (Nd_2O_3)、氧化钷 (Pm_2O_3)、氧化钐 (Sm_2O_3)、氧化铕 (Eu_2O_3)、氧化钆 (Gd_2O_3)、氧化铽 (Tb_2O_3)、氧化镝 (Dy_2O_3)、氧化钬 (Ho_2O_3)、氧化铒 (Er_2O_3)、氧化铥 (Tm_2O_3)、氧化镱 (Yb_2O_3) 和氧化镥 (Lu_2O_3)。此外，还可以由氮化铪膜、氮化铝膜、氮氧化

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铪膜或氮氧化铝膜形成上述的具有负电荷的绝缘膜 33。

[0056] 关于上述的具有负电荷的绝缘膜 33，在损害绝缘性的范围内，可以对该绝缘膜 33 加入硅 (Si) 或氮 (N)。在不损害膜的绝缘性的范围内，适当地确定硅或氮的浓度。在如上所述加入硅 (Si) 或氮 (N) 的情况下，可以增强膜的耐热性并且提高在处理期间防止离子注入的能力。

[0057] 在上述沟槽 31 的底部，P 型杂质区域 35 布置在上述半导体基板 11 中。通过对半导体基板 11 掺入 P 型杂质（例如，硼或二氟化硼）形成该 P 型杂质区域 35。该 P 型杂质区域 35 的杂质浓度可以低于现有技术的布置在元件隔离区域下的半导体基板中的 P 型杂质区域的杂质浓度。

[0058] 在这点上，在通过上述的具有负电荷的绝缘膜 33 的负电荷向上述元件隔离区域 14 下的半导体基板 11 充分引入空穴的情况下，不需要形成上述的 P 型杂质区域 35。

[0059] 此外，上述的 P 型杂质区域 35 连接到上述的 P 型杂质区域 22。因此，通过上述的 P 型杂质区域 22 固定了上述的 P 型杂质区域 35 的电势。

[0060] 在上述的固态成像装置 1 中，像素部分 12 的元件隔离区域 14 包括具有负电荷的绝缘膜 33。因此，在紧邻元件隔离区域 14 位于下方的半导体基板 11 中产生由于具有负电荷的绝缘膜 33 中的负电荷而生成的空穴累积层。通过空穴累积层抑制由于元件隔离区域 14 与半导体基板 11 之间的界面处的缺陷而导致的噪声生成。

[0061] 另外，由于通过负电荷形成空穴累积层，所以可以省去现有技术中在紧邻元件隔离区域位于下方的半导体基板中形成的 P 型杂质区域。

[0062] 作为另一选择，在形成 P 型杂质区域 35 的情况下，可以减小它的浓度。也就是说，在形成上述的 P 型杂质区域 35 的情况下，除了由于上述的具有负电荷的绝缘膜 33 的负电荷而生成的空穴累积层以外，还增强了空穴累积效果。

[0063] 因此，即使当 P 型杂质区域 35 的浓度减小时，仍通过上述的具有负电荷的绝缘膜 33 的负电荷引发与之对应的空穴，由此获得了与现有技术中的固态成像装置的空穴浓度基本相等的空穴浓度，在现有技术中布置 P 型杂质区域而没有上述的具有负电荷的绝缘膜 33。结果，与现有技术中的布置在固态成像装置的元件隔离区域下的 P 型杂质区域相比，可以减小上述的 P 型杂质区域 35 的浓度。

[0064] 如上所述，与以前相比可以减小 P 型杂质区域 35 的杂质浓度，或者可以省去 P 型杂质区域 35。因此，减小了 P 型杂质向晶体管的沟道区域的扩散。因此，可以使晶体管的有效沟道宽度大于现有技术中的固态成像装置的有效沟道宽度。

[0065] 也就是说，尽管随着晶体管变得更加细小由于 P 型杂质的扩散导致沟道减小的效果变得明显，但是仍能够抑制该效果。具体地讲，由于抑制了放大晶体管 16A 的有效沟道宽度的减小，所以减小了 1/f 噪声。另外，由于抑制了沟道减小的效果，所以实现了如下效果：抑制了晶体管的阈值电压的增加以及减小了阈值电压的变化。

[0066] 换言之，抑制了由于 P 型杂质区域 35 导致的 P 型杂质的扩散并且相应地减小了像素尺寸，同时确保了像素晶体管部分 16 的晶体管的有效沟道宽度并且减小了 1/f 噪声。

[0067] 因此，噪声抑制和细小像素可以变得相互兼容。

[0068] 此外，由于降噪而提高了成像的图像质量。此外，细小像素可以增加像素的数目。成像的图像质量由此变成更高水平的清晰度。存在如上所述的优点。

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[0069] 如果上述的 P 型杂质区域 35 的 P 型杂质扩散到光电转换部分 15 侧，则可能会出现不利影响，例如，饱和电荷量下降或者残像劣化）。然而，在上述的固态成像装置 1 中，由于可以省去上述的 P 型杂质区域 35 或者可以减小上述的 P 型杂质区域 35 的浓度，所以可以抑制饱和电荷量下降以及残像劣化。

[0070] 在固态成像装置的某结构中，通过元件隔离区域完全隔离形成有光电转换部分和转移晶体管的区域与形成有复位晶体管、放大晶体管和选择晶体管的像素晶体管部分。具有这种结构的固态成像装置可以具有与根据本发明的实施例的固态成像装置 1 的结构相同的结构，在根据本发明的实施例的固态成像装置 1 中具有负电荷的绝缘膜被应用于元件隔离区域。

[0071] 第二实施例

[0072] 固态成像装置的制造方法的第一示例

[0073] 将参照图 3A 到图 4E 所示的生产步骤的截面图，描述根据本发明的第二实施例的固态成像装置的制造方法的第一示例。

[0074] 如图 3A 所示，在半导体基板 11 上依次形成氧化硅膜 71 和氮化硅膜 72。例如，将硅基板用于上述的半导体基板 11。

[0075] 然后，如图 3B 所示，在上述的氮化硅膜 72 上形成用于形成元件隔离沟槽的抗蚀剂掩模（附图中没有示出）。将获得的掩模用作蚀刻掩模，并且对上述的氮化硅膜 72、上述的氧化硅膜 71 和上述的半导体基板 11 进行蚀刻。也就是说，在半导体基板 11 的像素区域 17 中形成用于进行元件隔离的第一沟槽 51，在周边电路区域 18 中形成用于进行元件隔离的第二沟槽 52。

[0076] 基于在像素部分中形成的元件隔离区域的绝缘膜的膜厚度，确定对于上述的第一沟槽 51 和第二沟槽 52 的、半导体基板 11 的挖掘深度。上述的挖掘深度被指定为例如 150nm 以下，并且优选是大约 50nm。

[0077] 然后，去除上述的抗蚀剂掩模。

[0078] 接下来，如图 3C 所示，在上述的第一沟槽 51 的内表面上形成氧化硅膜 53，在上述的第二沟槽 52 的内表面上形成氧化硅膜 54。例如通过热氧化方法对暴露在上述的第一沟槽 51 和第二沟槽 52 的内部的上述的半导体基板 11 进行氧化，形成上述的氧化硅膜 53 和 54。

[0079] 因此，通过氧化硅膜 53 和 54，减小了上述的第一沟槽 51 和第二沟槽 52 与上述的半导体基板 11 的界面处存在的缺陷。

[0080] 然而，由于上述的氧化硅膜 53 和 54 的膜厚度增加，减小了之后埋入并且具有负电荷的膜向半导体基板 11 引入空穴的效果。

[0081] 因此，上述的氧化硅膜 53 和 54 的膜厚度优选为 5nm 以下。

[0082] 然后，如图 3D 所示，在上述的第一沟槽 51 和上述的第二沟槽 52 的内表面上形成具有负电荷的绝缘膜 55，其中上述的氧化硅膜 53 和 54 位于在它们之间。在上述的氮化硅膜 72 上也形成该具有负电荷的绝缘膜 55。

[0083] 例如，通过氧化铪（HfO_2）膜、氧化锆（ZrO_2）膜、氧化铝（Al_2O_3）膜、氧化钽（Ta_2O_5）膜、氧化钛（TiO_2）膜或者氧化钇（Y_2O_3）膜形成上述的具有负电荷的绝缘膜 55。

[0084] 膜形成方法的示例包括化学气相沉积法、喷溅法和原子层沉积（ALD）法。为了提

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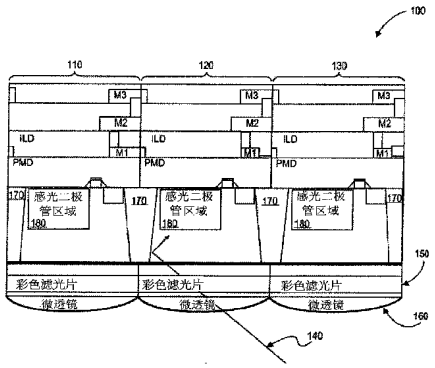
权利要求书 2 页 说明书 5 页 附图 7 页

(54)发明名称

具有深光反射沟槽的背照式图像传感器

(57)摘要

本发明提供一种像素阵列，其是使用基板形成的，该基板具有前侧及用于接收入射光的背侧。各个像素通常包含金属化层、感光区域及沟槽，这种金属化层被包含在该基板的前侧中，该感光区域是形成于该基板的后侧中，该沟槽围绕该基板的后侧中的感光区域而形成。该沟槽造成入射光被导引远离该沟槽并朝向该感光区域。



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1. 一种图像传感器，包括：

利用具有前侧及背侧的基板形成的像素阵列，其中该背侧是用于接收入射光，每个像素包含：

该基板的前侧中所包括的金属化层；及

形成至所述金属化层的背侧的感光区域；及

围绕该基板的背侧中的感光区域形成的沟槽，该沟槽造成该入射光被导引远离该沟槽并朝向该感光区域。

2. 如权利要求 1 所述的装置，其中该沟槽是由气体填充的或被排空以产生真空或部分真空。

3. 如权利要求 1 所述的装置，其中该沟槽的一部分位于一区域中，该区域至少部分地处于相邻像素的周边。

4. 如权利要求 1 所述的装置，其中该沟槽是在使该基板的背侧薄化之后形成的。

5. 如权利要求 4 所述的装置，其中利用化学或机械平坦化 (CMP) 处理使该基板薄化。

6. 如权利要求 4 所述的装置，其中在使用浅沟槽隔离 (STI) 区域作为蚀刻终止层的情况下利用化学蚀刻处理使该基板薄化。

7. 如权利要求 1 所述的装置，其中该基板的背侧所接收的入射光响应于在该沟槽与该基板之间的介面处的全内反射而从该沟槽反射。

8. 如权利要求 1 所述的装置，其中填充该沟槽的材料具有比该基板的折射率小的折射率。

9. 如权利要求 1 所述的装置，其中该沟槽具有在该沟槽与该感光区域的介面处的反射性金属。

10. 如权利要求 1 所述的装置，其中该沟槽是使用非保形沉积介电膜加以密封的。

11. 如权利要求 1 所述的装置，其中该沟槽是通过在围绕着该感光区域的周边区域的一部分中的浅沟槽隔离 (STI) 区域的背侧蚀刻而形成的。

12. 如权利要求 1 所述的装置，其中该基板的背侧被图案化并被蚀刻以露出浅沟槽隔离 (STI) 区域。

13. 如权利要求 1 的装置，其中该沟槽是通过蚀刻该浅沟槽隔离 (STI) 区域并通过用二氧化硅来填充被蚀刻的 STI 区域而形成的。

14. 如权利要求 1 所述的装置，其中该沟槽是通过蚀刻该浅沟槽隔离 (STI) 区域使得一硅层残留于该 STI 区域中而形成的。

15. 一种方法，包括：

形成与沟槽相邻的感光区域，该感光区域形成为至少通过在其中形成有该沟槽的水平；

移除基板的背侧的一部分使得该沟槽的表面被暴露；

移除被暴露的沟槽的一部分；及

用具有与该基板不同的折射率的材料来填充由基板背侧被移除的部分及被暴露的沟槽的被移除的部分先前所占据的区域。

16. 如权利要求 15 所述的方法，其进一步包括施加非保形层以涂布该基板的背侧。

17. 如权利要求 15 所述的方法，其进一步包括将反射层施加至通过移除被暴露的沟槽

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的一部分而露出的表面。

18. 一种方法，包括：

形成与沟槽相邻的感光区域，其中该感光区域及该沟槽是使用基板的顶侧形成的；

蚀刻该基板的背侧的一部分，使得该沟槽的表面被暴露；及

用具有不同折射率的材料来填充由基板背侧被移除的部分先前所占据的区域。

19. 如权利要求 15 所述的方法，其中该沟槽被蚀刻以留下一硅层。

20. 如权利要求 19 所述的方法，其进一步包括离子注入背侧硅。

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具有深光反射沟槽的背照式图像传感器

[0001] 本发明主张 2008 年 2 月 8 号申请的美国专利临时申请案第 61/027,393 号题为「具有深光反射沟槽的背照式图像传感器」的权利，其以引用方式并入本文中。

技术领域

[0002] 本发明一般涉及成像电路，尤其涉及但不限于图像传感器。

背景技术

[0003] 集成电路已被研发以减小用于实施电路系统的元件的尺寸。举例来说，集成电路利用越来越小的设计特征，其能减少用于实施该电路系统的面积，使得现在多种设计特征正好在可见光的波长以下。随着图像传感器及作为感测阵列的一部分的单独的像素的尺寸不断缩小，重要的是更有效地捕获照射该感测阵列的入射光。因此，更有效地捕获入射光有助于维持或改善由尺寸不断缩小的感测阵列所捕获的电子图像的品质。

发明内容

[0004] 本文描述一种图像感测深光反射沟槽的实施例。在如下描述中提到多个具体细节以提供这种实施例的一透彻的理解。然而，本领域技术人员将了解此处描述的技术可被实践而不具有一个或更多个这种具体细节，或具有其他方法、元件、材料等。在其他情况下，熟知的结构、材料或操作未被详细显示或描述以避免混淆某些方面。

[0005] 贯穿此说明书，对「一个实施例」或「一实施例」的引用意为一种结合该实施例而描述的特定特征、结构、或特性被包含于本发明的至少一个实施例中。因此，在此说明的多个地方，用语「在一个实施例中」或「在一实施例中」的出现不必都涉及该相同的实施例。此外，在一个或更多个实施例中，这种特定的特征、结构或特性可以任何适当的方式组合。使用于此的术语「或」通常意为包含一种包含功能的意思，例如「及 / 或」。

[0006] 总体而言，集成电路包括用于多种应用的电路。这种应用使用多种装置，例如逻辑装置、成像器（包含 CMOS 及 CCD 成像器）及存储器（例如 DRAM 以及基于 NOR 及 NAND 的闪存存储器装置）。这些装置通常利用晶体管以发挥多种功能，包含信号的切换及放大。

[0007] 晶体管通常是通过执行于一硅基板上的光刻处理而形成于集成电路中。这种处理包含诸如将一光刻胶层施加至该基板、使用光（包含深紫外波长）将该光刻胶层曝光成一图案、通过蚀刻移除该光刻胶的曝光部分（或非曝光部分，仰赖于所使用的正光刻胶或负光刻胶）及例如通过沉积或注入附加材料而修改曝光结构的步骤以形成多种用于电子元件（包含晶体管）的结构。

[0008] 术语「基板」包含使用基于硅、锗化硅、锗、砷化镓及类似物的半导体形成的基板。术语基板亦可涉及已被执行于该基板上以在该基板中形成区域及 / 或结的先前处理步骤。术语基板亦可包含多种技术，例如掺杂及未掺杂半导体、硅的外延层及形成于该基板上的其他半导体结构。

[0009] 化学机械平坦化 (CMP) 可经执行以提供适于形成附加结构的被修改基板的表面。

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这种附加结构可通过执行诸如上述列出的处理步骤而被添加至该基板。

[0010] 由于作为一感测阵列的一部分的单独的像素中的这种图像传感器的尺寸日益变小，多种设计尝试更有效地捕获照射该感测阵列的入射光。举例来说，像素的光感测元件（例如光电二极管）的面积通常是通过在各个像素上（或之下）配置一微透镜而被最大化，使得该入射光被更好地聚焦于该光感测元件上。光通过该微透镜的聚焦尝试捕获通常入射于该像素被该感光元件占据的区域之外的光（并因此消失及 / 或「泄露」至其他非目的像素）。

[0011] 另一种可使用的方法是自该 CMOS 图像传感器（例如之下）的「背侧」收集光。使用该图像传感器的背侧允许光子被收集于一区域中，该区域相对而言未被许多通常用于形成典型的图像传感器的介电及金属层阻挡。一种背照式 (BSI) 图像传感器可通过使该图像传感器的硅基板变薄而制成，其可降低入射光在遇到该图像传感器的感测区域之前所穿越的硅的量。

[0012] 然而，在使该图像传感器的基板变薄时，将遭遇在该像素的灵敏度及（与相邻像素的）串扰之间做出权衡。举例来说，当较少地薄化时（其导致较厚的剩余硅基板），用于将光转换为电子 - 空穴对的光电二极管的较大的（体积）区域可被提供。当这种电子 - 空穴对被形成（在被提供的该较大区域中）相对远离该光电二极管空乏区时，被形成的这种电子 - 空穴对更易于被相邻的光电二极管捕获。由相邻光电二极管对形成的这种电子 - 空穴对的捕获是一种被称为电串扰的效应（其可导致彩色图像传感器中的彩色噪声）。因此，电串扰的机率随着该硅基板的厚度而增加，而灵敏度随着较薄的硅基板的使用而减小。

[0013] 光学串扰亦影响捕获入射光的效率。前照式 (FSI) 装置通常包含金属化层，入射光横穿穿过这种金属化层。FSI 装置可利用适当放置在这种金属化层中的金属结构以将光引导至该光电二极管，进而阻挡杂光进入错误的光电二极管而产生光学串扰。与之相反的是，背照式 (BSI) 装置通常不将入射光穿过这种金属化层，且因此不朝感光区域引导光。因此光学串扰是 BSI 装置中的一个更大的问题（与例如 FSI 装置相比）。

[0014] 根据本发明，BSI 像素阵列是利用一基板形成，该基板具有一前侧及一用于接收入射光的背侧。各个像素通常包含被包含于该基板的该前侧上的金属化层、一形成于该基板的该背侧（或该前侧）中的感光区域。一沟槽促使该入射光被导引远离该沟槽并朝向该感光区域。

[0015] 各个 BSI 像素具有深沟槽，其由一种在相邻的像素之间的低折射率的材料（例如 SiO_2，或其中该材料可为「空的」，如由一种常压气体填充或被抽空以产生一真空或部分真空）填充。这种深沟槽提高像素的灵敏度同时减少像素之间的串扰。像素之间的电子串扰被减少是因为相对而言在像素收集区域的较低处形成的电子 - 空穴对通常不会（或不能）迁移至相邻的像素。大体减少（或消除）的电子 - 空穴对的迁移允许一更厚的硅收集区域被使用，其导致灵敏度被提高。光学串扰被减少是因为该基板（例如硅）及这种深沟槽之间的折射率差异导致具有例如大于例如 16.6 度的入射角的光的全内反射（其中空气填充的深沟槽被提供于相邻的像素之间）。

附图说明

[0016] 图 1 为在 CMOS 图像传感器中背照式 (BSI) 像素的范例传感器阵列的一截面图；

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[0017] 图 2 为根据本发明的一实施例该 CMOS 图像传感器的一范例背照式 (BSI) 像素的一截面图；

[0018] 图 3 包含图 3A 到图 3E，显示一种形成一深光反射沟槽的范例方法；

[0019] 图 4 包含图 4A 到图 4E，显示另一种形成一深光反射沟槽的方法；

[0020] 图 5 显示一种具有一薄衬里氧化物的深光反射沟槽；

[0021] 图 6 显示一种具有一氧化物填充剂的深光反射沟槽；及

[0022] 图 7 显示一种不自前表面延伸至后表面的深光反射沟槽。

具体实施方式

[0023] 为达说明的目的，图 1 显示根据本发明的一实施例在 CMOS 图像传感器中的背照式 (BSI) 像素的范例传感器阵列的截面。阵列 100 包含像素 110、120 及 130。结构 100 通常含有至少数千个像素且通常含有不止一百万个像素。为了显示的清晰性，三个像素被显示。

[0024] 该像素阵列 100 通常是以二维阵列被配置使得可响应于被各个像素捕获的入射光 (140) 而形成一电子图像。各个像素可具有滤光片 150（包含彩色滤光片）使得该电子图像可被用以捕获彩色图像或提高该像素对例如某个波长的光的敏感性。各个像素亦可具有与各个像素关联的微透镜 160，使得该入射光被更直接地引导至该像素中。

[0025] 举例来说，入射光 140 横穿像素 120 的微透镜 160。该入射光是由该微透镜 160 更直接地折射至该像素 120 的基板中。然而，该入射光通过该微透镜 160 的方向改变（在此实例中）不足以防止该入射光 140 遇到位于像素 110 及 120 之间的沟槽 170。根据本发明，该沟槽 170 的一先前的氧化物被移除及 / 或替换，使得在该沟槽 170 与该像素 120 的基板之间的介面的相对折射率被增大而使得入射光 140 朝该像素 120 的一感光部位 180 反射。因此图 1 被用于例如显示该光可由该深沟槽弯曲至该像素或光电二极管中。

[0026] 图 2 显示根据本发明的一实施例一 CMOS 图像传感器的一范例背照式 (BSI) 像素的一截面图。结构 200 包含一基板 202，其上形成有一感光的感光二极管区域 204。一浮动漏极 206 通常形成为具有一种导电类型（例如 N 型，与感光二极管区域 204 的导电类型相比，N 型具有更高的 N 型材料浓度）。

[0027] 绝缘结构 208 形成于该基板 202 内以促进将这些像素彼此绝缘。绝缘结构 208 通常可利用诸如深沟槽隔离 (DTI) 或硅局部氧化 (LOCOS) 的方法而形成。一绝缘结构 208 可利用一 DTI 方法通过在该基板 202 内蚀刻一沟槽及在该沟槽内沉积一介电材料（例如二氧化硅）而形成。这种沟槽可自该基板 202 的前侧或背侧蚀刻。经沉积的介电材料可利用 CMP 而平坦化。一栅极结构 210 被形成于该基板 202 之上以控制自该感光二极管区域 204 流向该浮动漏极 206 的电流。

[0028] 在一图像传感器中一种典型的单独像素 200 可包含多个层的堆迭体，这些层包含金属层、平坦化层及类似物。如图所示，该像素 200 包含一前金属介电材料 212。该介电材料 212 可为任何绝缘体，例如氧化物。对于一些实施例来说，该介电材料可为氧化硅。通孔 214 可通过蚀刻及沉积一合适的金属或导电材料而形成于该介电材料 212 内。

[0029] 具有若干 M1 导体的第一金属层可形成于该介电材料 212 中（或上）。对于一些实施例来说，该第一金属层可被蚀刻为这种 M1 金属导体的形状。该介电材料 216 可被沉积及 / 或成长以填充这种 M1 导体之间的空隙。该介电材料 212 可使这种 M1 导体与下方结构绝

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缘。这种 M1 导体可为铜、铝、铜铝混合物或其他适于传输一信号的材料（例如钨）。

[0030] 如图所示，该像素 200 包含第二金属层，该第二金属层具有配置于一中间层介电材料 216 中（或上）的若干 M2 导体。对于一些实施例来说，该第二金属层可被蚀刻成这种 M2 导体的形状。该介电材料 218 可被沉积及 / 或成长以填充这种 M2 导体之间的空隙。该介电材料 216 可使这种 M1 金属导体与这种 M2 金属导体绝缘。通孔 214 可被使用以电连接在该阵列的不同层上的结构。

[0031] 该像素 200 进一步包含第三金属层，该第三金属层具有配置于一中间层介电材料 218 中（或上）的若干 M3 导体。对于一些实施例来说，该第二金属层可经蚀刻为这种 M3 导体的形状。一介电材料 220 可被沉积及 / 或成长以填充这种 M3 导体之间的空隙。该介电材料 218 可使这种 M2 金属导体与这种 M3 金属导体绝缘。该介电材料 220 可被成长及 / 或沉积以使 M3 金属导体绝缘及 / 或使该阵列的顶面平坦化。

[0032] 图 3 显示一种形成一深光反射沟槽的范例方法。深光反射沟槽可形成于一用于浅沟槽隔离的区域中。浅沟槽隔离是经形成以电隔离相邻的像素及周边电路装置。该浅沟槽隔离通常为一种在硅基板内蚀刻且之后由二氧化硅填充的沟槽。典型的沟槽深度为大约 300 纳米到 400 纳米（依据用于形成该沟槽的技术），或可小于 400 纳米。

[0033] 图 3A 显示一包含大约一到三微米深的深沟槽光反射结构 310（深沟槽结构 310）的范例截面。这种深沟槽结构 310 通常亦由氧化物填充。在这种深沟槽结构 310 形成后，可应用一前侧制造方法。在图 3B 中在该前侧制造处理完成后，背侧薄化处理被完成，以开始一背照式 (BSI) 制造处理。在一常规 BSI 处理中，基板 320 的背侧通常通过 CMP 及 / 或不涉及蚀刻终止层的使用的化学蚀刻而被薄化。根据本发明，深沟槽结构 310 可被用作一 CMP 蚀刻终止层，其可改善对背侧薄化的厚度控制。

[0034] 在该基板 320 已被薄化后，这种深沟槽结构 310 的下表面被暴露，如图 3B 所显示。在图 3C 中，在这种深沟槽中被暴露的二氧化硅是利用一种对硅具选择性的蚀刻方法移除（例如湿式或干式蚀刻方法）。此时，深光反射沟槽形成于空的沟槽 330 中，产生一较大的折射率差异（例如硅到空气）。或者，这种空沟槽 330 可用一种金属涂布（及 / 或填充）以制成一更加完美的反射器。图 3D 显示一种在该阵列的下表面上沉积非保形涂层 340。一非保形介电膜被沉积，其密封住这种沟槽（其可为空的、被涂布或被填充的）。SiO_2 亦可被留于这种沟槽中。

[0035] 图 3E 显示了额外的背侧处理，诸如硅背侧保护（例如注入）或溢料式浇口（未显示）或防反射涂层 350。此外，滤光片 360 被配置于由该非保形涂层 340 所界定的层之上。这种滤光片可与感光元件对齐使得一滤光片 360 与该像素的该基板及该二极管感测区域对齐。一微透镜 370 可被配置于该彩色滤光片 360 之上以促进将光线折射至该像素中。

[0036] 图 4 显示形成一深光反射沟槽的一种替代性方法。图 4A 显示一种相似于图 3A 的像素结构的像素结构（其中隔离由 STI 实现，而非深沟槽）。在被薄化至一理想厚度后，利用光刻胶 440 使基板 420 的背侧光刻图案化。基板 420 的背侧可利用图 4B 所显示的标准方法而图案化。在图 4C 中，（基板 420 的）硅及 (STI 结构 410 的）氧化物被蚀刻，如图 4C 所示。因此，该蚀刻形成深光反射沟槽 430。在图 4D 中，该光刻胶被移除。在图 4E 中一反射涂层 450 被保形施加至这种深光反射沟槽 430 的表面，并填充沟槽 430，如图 4E 所示。可继续附加处理以添加诸如一防反射层、一彩色滤光片及一微透镜的结构。在多种实施例中

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该沟槽可自不同的边侧蚀刻。举例来说，该深沟槽可自背侧蚀刻并与该前侧 STI 对齐。该背侧蚀刻亦可在该深沟槽不与该前侧 STI 对齐且连接至该前侧 STI 的情况下被完成。在另一替代实施例中，该前侧 STI 可被消除，及所有隔离自背侧执行。

[0037] 图 5 显示一种具有一薄衬里氧化物的深光反射沟槽。该标准浅沟槽隔离可形成于像素阵列及周边电路中。在浅沟槽蚀刻之后，该周边电路可由光刻胶掩盖，且该像素阵列沟槽经更深地蚀刻至一微米到三微米（以形成一如图 5 所显示的深光反射沟槽 510）。一薄衬里氧化物 520 利用一高温在深光反射沟槽 510 内成长以使该深光反射沟槽 510 的硅侧壁钝化。周边的浅沟槽可用一种典型的沟槽填充技术（使用，例如，氧化物 540）填充。由于该沟槽的相对较高的长宽比，该深沟槽在该 STI 被填充时并不必被完全填充。因此气隙 530 可被自然地形成于该沟槽的内部。因此，在硅薄化之后不需要氧化物蚀刻。不执行该氧化物蚀刻的优点在于保持该衬里氧化物以更好地使表面钝化及降低处理复杂度。在硅薄化之后可通过等离子体浸入离子注入而完成进一步钝化。

[0038] 图 6 显示一种具有一氧化物填充剂的深光反射沟槽。该像素 600 的背侧可经图案化，深沟槽结构 610 可被蚀刻。一种沟槽填充技术（适于填充具有高长宽比的沟槽，例如「高且薄的」沟槽）可被用以用氧化物填充这种沟槽以形成一具有一氧化物填充剂的深光反射沟槽。在多种范例方法中，原始氧化物 620 可能是存在的。由于硅及二氧化硅之间的折射率差异相对较大，用于全内反射的最终临界角仍足以应付多种传感器应用。

[0039] 图 7 显示一种不自前表面延伸至后表面的深光反射沟槽。在硅 730 被薄化至一理想厚度后，该后表面可注入 P 型注入物 740 以进行钝化。一形成于像素阵列及周边电路中的深沟槽隔离可经蚀刻使得一相对较薄的硅层 720（例如几分的一微米）残留于该深沟槽 710 的底部及该后表面之间。残留于该沟槽之下的薄硅层 720 亦可被使用以电连接像素基板及阵列晶体管。

[0040] 本发明的例示的实施例的以上描述，包含描述于摘要中的内容，并非意图其详尽或将本发明限制为所揭示的任何精确形式。虽然本发明的这种具体实施例及实例以说明的目的描述于此，但本领域技术人员将发现多种修改可在本发明的范围内。

[0041] 鉴于如上的详细描述，可对被本发明做出这些修改。使用于如下权利要求中的术语不应被理解为将本发明限制为在本说明书中揭示的特定实施例。本发明的范围将完全由如下的这种权利要求确定，其应根据已确立的权利要求解读原理而被理解。

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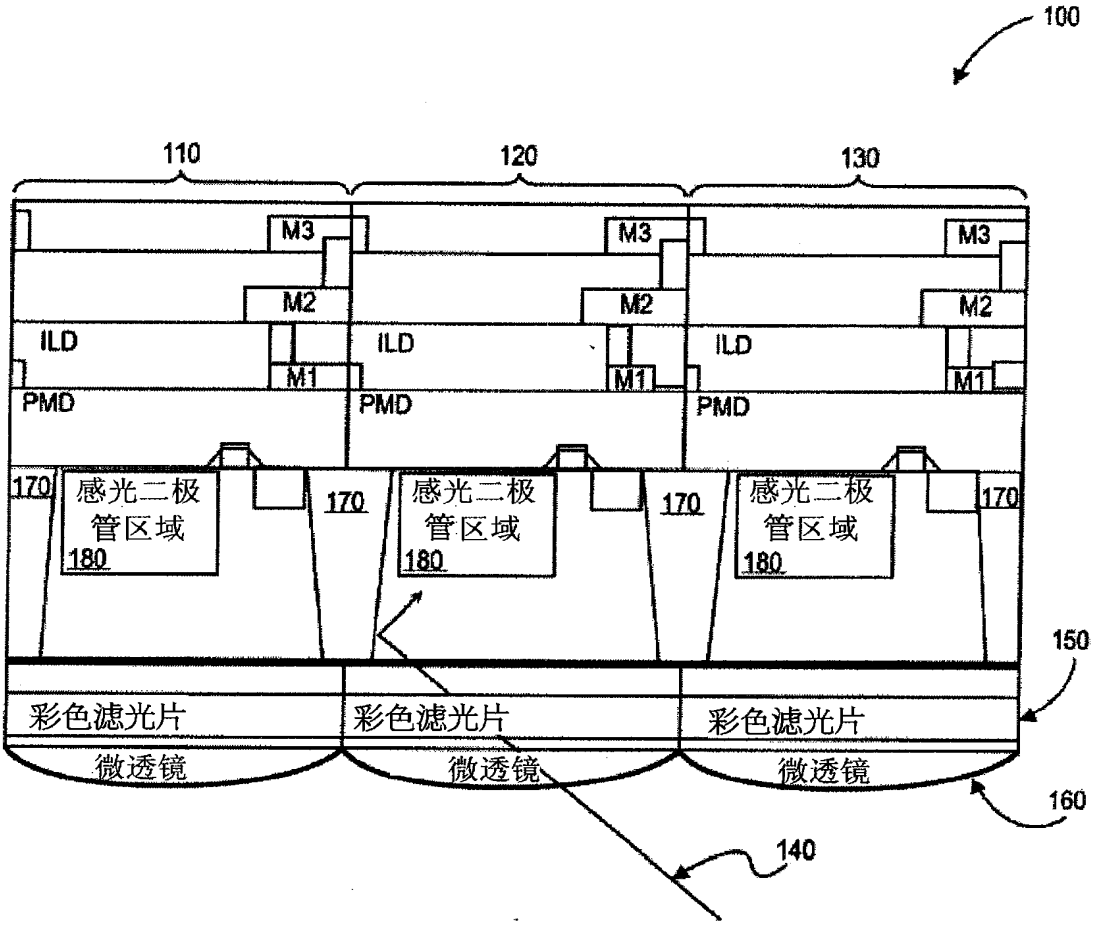


图 1

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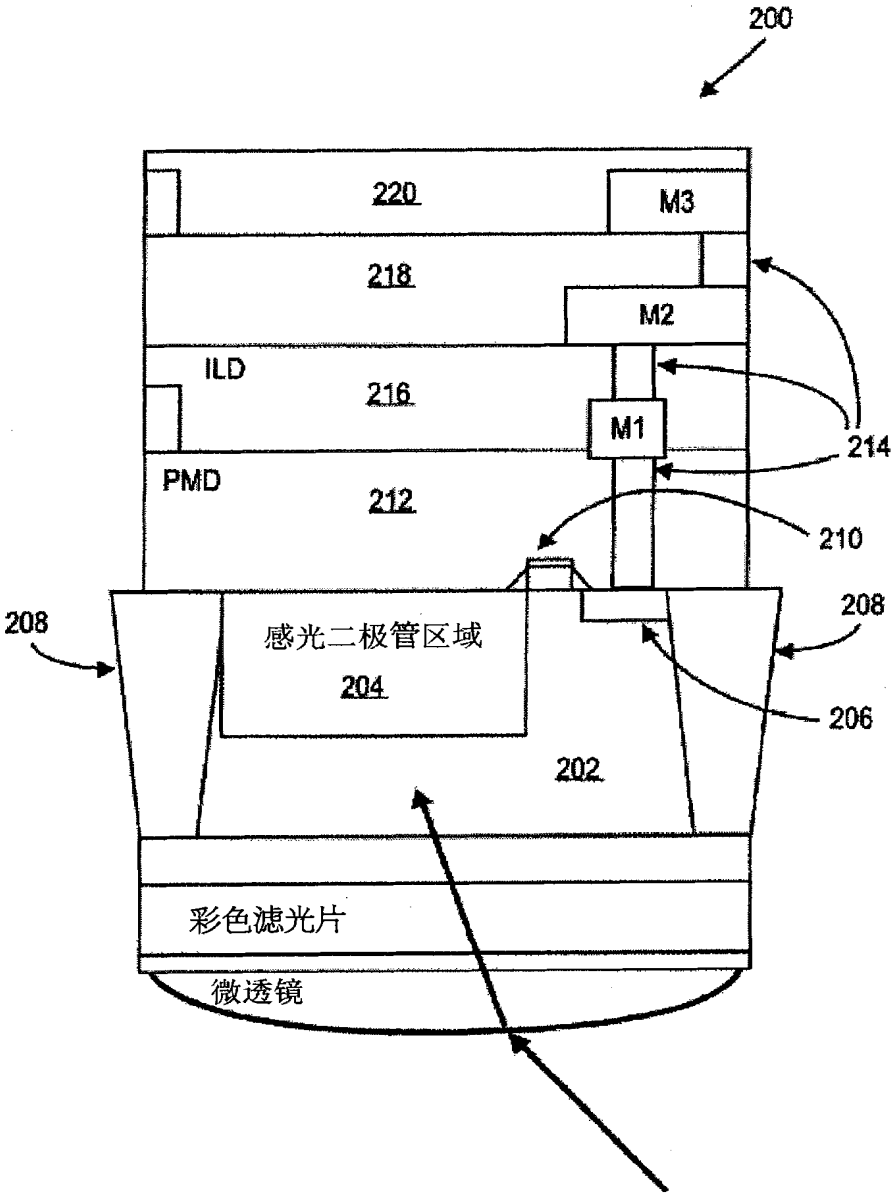


图 2

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Espacenet

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Applicant(s):

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DESCRIPTION CN102270646

The invention provides a back-illuminated CMOS image sensor comprising: a semiconductor substrate having a first surface and a second surface opposite thereto; the semiconductor substrate including at least one pixel cell region; an isolation structure located Between adjacent pixel cell regions; wherein the isolation structure is a deep trench isolation structure, and the deep trench isolation structure penetrates the first surface and the second surface of the semiconductor substrate. The present invention reduces crosstalk of electrical signals between adjacent pixel cell regions, improves display fade of CMOS image sensors, and improves imaging quality.

Backlighting CMOS image sensor

Technical field

The present invention relates to an image sensor, and more particularly to a backlit CMOS image sensor.

Background technique

The image sensor is an important part of the digital camera. According to the different components, the image sensor is divided into a Charge Coupled Device (CCD) image sensor and a Complementary Metal-Oxide Semiconductor (CMOS) image sensor. Among them, CMOS image sensors are highly integrated, easily compatible with standard CMOS fabrication processes, and have low power consumption. With the improvement of CMOS fabrication processes, CMOS image sensors have become the mainstream of current image sensors.

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An existing CMOS image sensor is disclosed in Chinese Patent Application No. 200710148796.5. Existing CMOS image sensors include a semiconductor substrate, which typically includes a plurality of pixel cell regions arranged in a matrix with shallow trench isolation structures (STIs) between adjacent pixel cell regions. Please refer to FIG. 1. FIG. 1 is a schematic structural diagram of a conventional CMOS image sensor. The CMOS image sensor includes a semiconductor substrate 100. The semiconductor substrate 100 includes a plurality of pixel unit regions 103. In the figure, there are 2 pixel unit regions. 103 is described as an example; there is a shallow trench isolation structure 106 between adjacent pixel cell regions 103 . The pixel unit area 103 is used to form a pixel. The pixel unit area 103 generally includes a photodiode area 104 and a transistor area 105. The photodiode area 104 is used to form a photodiode, and the photodiode is used for photoelectric conversion. The transistor region 105 is used to form a transistor for amplifying and outputting an electrical signal converted by a photodiode. The shallow trench isolation structure 106 is used for isolation of adjacent pixels. The semiconductor substrate 100 includes a first surface 101 and a second surface 102 opposite thereto. Light enters the pixel unit area 103 from the second surface 102. Those skilled in the art refer to the CMOS image sensor as a Backside illuminated CMOS image sensor.

In practice, it has been found that the above-mentioned back-illuminated CMOS image sensor has a problem of display fading, which affects the imaging quality.

Therefore, there is a need for a back-illuminated CMOS image sensor that can improve the display fading problem and improve the image quality of the CMOS image sensor.

Summary of the Invention

The problem solved by the present invention is to provide a back-illuminated CMOS image sensor capable of improving the display fading problem and improving the image quality of the CMOS image sensor.

To solve the above problem, the present invention provides a backlit CMOS image sensor including:

a semiconductor substrate, the semiconductor substrate having a first surface and a second surface opposite thereto;

The semiconductor substrate includes at least one pixel unit area;

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The isolation structure is located between adjacent pixel unit regions;

Wherein, the isolation structure is a deep trench isolation structure, and the deep trench isolation structure penetrates the first surface and the second surface of the semiconductor substrate.

Optionally, the width of the deep trench isolation structure is less than or equal to 0.25 micrometers.

Optionally, the depth of the deep trench isolation structure ranges from 1.5 to 4 microns.

Optionally, the filler in the deep trench isolation structure is a dielectric.

Optionally, the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate.

Optionally, the semiconductor substrate is sequentially formed with a filter and a microlens, and the filter and the microlens are located on the second surface of the semiconductor substrate.

The invention also provides a method for manufacturing a backlit CMOS image sensor, comprising:

A semiconductor substrate is provided, the semiconductor substrate having a first surface and a third surface opposite thereto, the semiconductor substrate including at least one pixel cell region;

A deep trench isolation structure is formed in the semiconductor substrate along the first surface, the deep trench isolation structure has a bottom along a depth direction of the trench, the trench depth direction is perpendicular to the first surface and the third The surface, the deep trench isolation structure is located between adjacent pixel cell regions;

The bottom of the deep trench isolation structure is used as a stop layer, the semiconductor substrate is thinned along the third surface of the semiconductor substrate, stops at the second surface, and the second surface exposes the deep trench The bottom of the isolation structure.

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Optionally, the thinning method includes a chemical mechanical polishing method.

Optionally, forming the deep trench isolation structure in the semiconductor substrate along the first surface includes the following steps:

Forming a hard mask layer having a first opening between adjacent pixel cell regions of the first surface;

Etching the semiconductor substrate along the first opening to form a second opening in the semiconductor substrate;

Filling the second opening with a dielectric

The hard mask layer is removed to form a deep trench isolation structure.

Optionally, the depth of the deep trench isolation structure ranges from 1.5 to 4 microns.

Optionally, the width of the deep trench isolation structure is less than or equal to 0.25 micrometers.

Optionally, the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate.

Optionally, the method further includes: forming a filter and a micro lens sequentially along the second surface with the pixel unit area, and the method for manufacturing the filter and the micro lens comprises a photolithography step, and The deep trench isolation structure serves as a photolithographically aligned mark.

Compared with the prior art, the present invention has the following advantages:

By providing a deep trench isolation structure penetrating the first surface and the second surface of the

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semiconductor substrate between adjacent pixel cell regions, isolation between adjacent pixels is performed, thereby preventing the photocarriers in the pixel cell region from diffusing to The adjacent pixel unit area reduces the crosstalk caused by electrical signals to the adjacent pixel unit area, improves the display fade of the CMOS image sensor, and improves the imaging quality.

Further, the filler in the deep trench isolation structure is a dielectric, and the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate, and the light totally reflects at the interface between the deep trench isolation structure and the semiconductor substrate. The light is prevented from entering the adjacent pixel unit area through the deep trench isolation structure, the crosstalk to the optical signal of the adjacent pixel unit area is reduced, the display fading of the CMOS image sensor is further improved, and the imaging quality is improved; The dielectric material of the trench isolation structure is silicon oxide and has a different color from the silicon of the semiconductor substrate. In the process of forming a filter and a microlens by a photolithography process, the deep trench isolation structure can be used as an alignment mark for lithography. No special alignment layer is required, saving process steps and reducing production costs.

Description of the drawings

FIG. 1 is a schematic structural diagram of a prior art CMOS image sensor.

FIG. 2 is a schematic structural diagram of a CMOS image sensor according to an embodiment of the present invention.

FIG. 3 is a schematic diagram illustrating the principle of total reflection formed at the interface between the deep trench isolation structure and the semiconductor substrate.

FIG. 4 is a schematic flowchart of a method for manufacturing a CMOS image sensor according to an embodiment of the present invention.

FIG. 5 to FIG. 9 are schematic cross-sectional views of a method for fabricating a CMOS image sensor according to the present invention.

detailed description

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The existing Backside illuminated CMOS image sensor has a problem of display fading. The inventor's research found that the cause of fading is crosstalk of neighboring pixels. One of the reasons for the crosstalk is that the existing shallow trench isolation structure cannot effectively isolate the photocarrier diffusion between adjacent pixel units. Since the incident light of the CMOS image sensor using the backlight illuminates the pixel cell region of the semiconductor substrate through the microlens and the filter, in the prior art, in order to increase the effective photosensitive area of the photodiode in the pixel unit region, the depth of the photodiode is usually higher. Large, its depth can reach more than 10000 Angstroms, while the depth of the existing shallow trench isolation structure is usually 2000 to 5000 Angstroms. In the photoelectric conversion, the photo-generated carriers generated by photoelectric conversion of the photodiode may be diffused, and the existing shallow trench isolation structure cannot effectively isolate the photo-generated carriers so that the photo-generated carriers may go to adjacent pixels. Crosstalk of electrical signals is caused to adjacent pixels, causing the display of the CMOS image sensor to fade.

The back-illuminated CMOS image sensor provided by the present invention solves the crosstalk of electrical signals and improves the display fading problem of CMOS image sensors. The back-illuminated CMOS image sensors include:

a semiconductor substrate, the semiconductor substrate having a first surface and a second surface opposite thereto;

The semiconductor substrate includes at least one pixel unit area;

The isolation structure is located between adjacent pixel unit regions;

Wherein, the isolation structure is a deep trench isolation structure, and the deep trench isolation structure penetrates the first surface and the second surface of the semiconductor substrate.

The technical solutions of the present invention will be described in detail below in conjunction with specific embodiments. Please refer to FIG. 2 . FIG. 2 is a schematic structural diagram of a CMOS image sensor according to an embodiment of the present invention.

The CMOS image sensor includes a semiconductor substrate 200, and the material of the semiconductor substrate 200 may be silicon, SOI, gallium nitride, or gallium arsenide. The semiconductor substrate 200 has a

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first surface 201 and a second surface 202 opposite thereto. In the present embodiment, the semiconductor substrate 200 is a silicon substrate having a P-type conductivity type.

As shown in FIG. 2, the semiconductor substrate 200 includes at least one pixel unit area 203. For convenience of description, the two pixel unit area 203 will be described as an example. There is a deep trench isolation structure 206 between adjacent pixel cell regions 203. The deep trench isolation structure 206 penetrates the first surface 201 and the second surface 202 of the semiconductor substrate 200 . The pixel unit region 203 of the semiconductor substrate 200 is formed with a filter 209 and a microlens 210. In this embodiment, the refractive index of the micro lens 210 ranges from 1.2 to 4, and its material may be silicon nitride SiNX, zirconium oxide ZrO2, hafnium oxide HfO2, titanium oxide TiO2, aluminum oxide Al3O2, zinc oxide ZnO2, etc. The range of the refractive index of the filter 209 is 1.4 to 2. The material of the filter 209 may be a photoresist material. The filter 209 and the microlenses 210 are formed by a photolithography process, and the deep trench isolation structure 206 can be used as an alignment mark for photolithography during a photolithography process that forms the filter.

Still referring to FIG. 2, the pixel cell area 203 is used to form a pixel. The pixel cell region 203 includes a photodiode region 204 and a transistor region 205. The photodiode region 204 is used to form a photodiode, which is used for photoelectric conversion, and converts light signals incident from the second surface 202 into corresponding electrical signals to generate photogenerated carriers. The transistor region 205 is used to form a transistor for amplifying and outputting the electrical signal converted by the photodiode. According to actual conditions, the transistor region 205 includes three or more transistors. The transistors have a shallow trench isolation structure and are used to isolate the transistors in the pixels. The depth of the shallow trench isolation structure ranges from 2000 to 5000 Angstroms.

In this embodiment, the deep trench isolation structure 206 penetrates the first surface 201 and the second surface 202 of the semiconductor substrate 200 . As an embodiment, the thickness of the semiconductor substrate 200 is in the range of 1.5 to 4 microns. The thickness of the deep trench isolation structure 206 should be the same as the depth of the semiconductor substrate 200, that is, 1.5 to 4 microns. As a preferred embodiment, the thickness of the semiconductor substrate 200 is 2 33 μ m, so that the photodiodes in the pixel unit region 203 can better absorb incident light, and accordingly, the deep trench isolation structure 206 is The depth is preferably in the range of 2 to 3 microns. Since the deep trench isolation structure 206 penetrates the first surface 201 and the second surface 202 of the semiconductor substrate 200, the deep trench isolation structure 206 can effectively prevent the photo-generated light generated by the photodiode of the pixel during photoelectric conversion. The flow diffuses to adjacent pixels, reduces the crosstalk of electrical signals to adjacent pixels, improves the pixel fading of the CMOS image sensor, and improves the imaging quality of the CMOS image sensor.

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The width of the deep trench isolation structure 206 is less than or equal to the width of the prior art shallow trench isolation structure to save chip area. As an embodiment, the width of the deep trench isolation structure 206 is 0.25 μm or less.

The filler in the deep trench isolation structure 206 is a dielectric whose refractive index is less than 0.8 times the refractive index of the semiconductor substrate. In this way, when the incident light enters the pixel unit area 203, total reflection is formed at the interface between the deep trench isolation structure 203 and the semiconductor substrate 200, so that incident light is prevented from entering the adjacent pixel unit area 203 through the deep trench isolation structure 206, and adjacent pixel units are The area 203 causes crosstalk of the optical signal, further improving the display fading problem of the CMOS image sensor. In order to facilitate the description of the principle that the light forms a total reflection at the interface between the deep trench isolation structure and the semiconductor substrate, the partial region 300 of the CMOS image sensor in Fig. 2 is enlarged and illustrated. The partial region 300 includes a pixel unit region 203, a corresponding filter 209, a microlens 210, and a deep trench isolation structure 206 on both sides of the pixel unit region 203. Please refer to FIG. 3. FIG. 3 is a schematic diagram illustrating the principle of total reflection formed at the interface between the deep trench isolation structure and the semiconductor substrate.

As shown in FIG. 3, the light A enters the pixel unit area 203 from the air through the micro lens 210, the filter 209, and the second surface 202 of the semiconductor substrate 200. Ideally, the light A is the photodiode of the pixel unit area 203. Absorption, however, may allow light to enter the interface of the deep trench isolation structure 206 and the semiconductor substrate 200 because the light A may have a certain tilt angle. Due to the difference in refractive index between the materials of the air, the microlens 210, the filter 209, and the semiconductor substrate 200, the light A reaches the interface between the deep trench isolation structure 206 and the semiconductor substrate 200 to refract light a plurality of times. Specifically, the normal line between the micro lens 210 and the air interface is O1, the angle between the light line A in the air and the normal line O1 is a1, and after the refraction, the angle between the light line A and the normal line O1 in the micro lens 210 is refracted. A2; The light A is transmitted to the interface between the microlens 210 and the filter 209 in the micro lens 210, the normal of the interface between the micro lens 210 and the filter 209 is O2, and the light A is in the micro lens 210. The included angle of the normal line O2 is a3. After refraction, the angle between the light A in the filter 209 and the normal line O2 is aa4; the light A is transmitted to the filter 209 and the semiconductor liner in the filter 209. The interface of the bottom 200, the normal of the interface between the filter 209 and the semiconductor substrate 200 is O3, and the angle between the light A and the normal O3 in the filter 209 is a5, and after being refracted, The angle a6 between the light A and the normal O3 in the semiconductor substrate 200; within the semiconductor substrate 200, the light A is transmitted to the interface between the semiconductor substrate 200 and the deep trench isolation structure 206. The normal to the interface between the 200 and the deep trench isolation structure 206 is O4, and the angle between the light A and the normal O4 in the semiconductor substrate 200 is β . In this embodiment, the interface between the deep trench isolation structure 206 and the semiconductor substrate 200 is perpendicular to the interface between the filter 209 and the semiconductor substrate 200. Therefore, the normal line O4 is perpendicular to the normal line O3, and thus, the

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angle β and the angle a6. Mutual corner.

Since in practice, the thickness of the micro lens 210 and the thickness of the filter 209 are optimally set by those skilled in the art, it is possible to make the angle a6 the same as the angle a1. The maximum value of the angle a1 is called the chief ray angle (CRA), and the angle of the principal ray tilt angle is in the range of 0 to 35° . Therefore, the angle a6 has an inclination angle ranging from 0 to 35° , and the angle β of the angle β of the angle a6 ranges from 55 to 90° , that is, the incident angle of the light ray and the normal O4 ranges from 55 to 90° . Therefore, assuming that the total reflection critical angle is α , if the light is to be totally reflected at the interface between the semiconductor substrate 200 and the deep trench isolation structure 206, α should be smaller than 55° to ensure the incident angle range between the light and the normal O4. At 55 to 90° , any incident angle is larger than α , and total reflection can be formed when the incident angle of the light and the normal O4 is 55 to 90° . Assuming that the total reflection critical angle is 55° , the refractive index of the semiconductor substrate 200 is x, and the refractive index of the dielectric filled in the deep trench isolation structure 206 is y, then according to the total reflection calculation formula: sin55° /sin90° =y/ x

y=sin55° *x=0.8*x

According to the above analysis, when the total reflection critical angle is 55° , the refractive index of the dielectric filled in the corresponding deep trench isolation structure 206 is 0.8 times the refractive index of the semiconductor substrate 200 .

Since the critical angle α of total reflection depends on the refractive index of the semiconductor substrate 200 and the refractive index of the filled dielectric in the deep trench isolation structure 206. Specifically, in the case where the refractive index of the semiconductor substrate 200 is constant, the smaller the refractive index of the dielectric filled in the deep trench isolation structure 206 is, the smaller the total angle a of the total reflection is. From the foregoing analysis, it can be seen that when the critical angle of total reflection is 55° , the refractive index of the dielectric in the corresponding deep trench isolation result 206 is 0.8 times the refractive index of the semiconductor substrate 200 . To make the total reflection critical angle less than 55° , the refractive index of the dielectric filled in the deep trench isolation structure 206 should be less than 0.8 times the refractive index of the semiconductor substrate 200 to ensure the light A in the deep trench isolation structure 206 and the semiconductor liner The total reflection occurs at the interface of the bottom 200. Therefore, the light A is left in the pixel unit area 203, so as to prevent crosstalk caused by the light A through the deep trench isolation structure 206 to the adjacent pixel unit area, and further improve the display fading phenomenon of the existing CMOS image sensor.

As an embodiment, when the material of the semiconductor substrate 200 is silicon, the filler of the deep trench

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isolation structure 206 may be silicon oxide, and the silicon oxide may have a refractive index less than or equal to 0.8 of the refractive index of silicon. Times. In this embodiment, the refractive index of silicon is 3.46, and the refractive index of silicon oxide is 1.46. In this way, the incident light can form a full reflection at the interface between the deep trench isolation structure 206 and the semiconductor substrate 200. Alternatively, the dielectric filled in the deep trench isolation structure 206 may be of other materials, provided that the refractive index of the dielectric filled in the deep trench isolation structure 206 is less than or equal to 0.8 times the refractive index of the silicon substrate. When the material of the semiconductor substrate 200 is other semiconductor material, the material of the dielectric filled in the deep trench isolation structure 206 may also be other materials, but the dielectric filled in the deep trench isolation structure 206 should have a lower refractive index than the semiconductor substrate. 200 is 0.8 times the refractive index to ensure that total reflection is formed at the interface between the deep trench isolation structure 206 and the semiconductor substrate 200 .

It should be noted that the above analysis is consistent with the width of the deep trench isolation structure 206 along the perpendicular to the first surface 201 and the second surface 202, so that the interface between the deep trench isolation structure 206 and the semiconductor substrate 200 is perpendicular to the first surface 201. The second surface 202 is described as an example. In practice, the width of the deep trench isolation structure 206 in the direction perpendicular to the first surface 201 to the second surface 202 may not be uniform due to the limitation of the manufacturing process, resulting in the interface between the deep trench isolation structure 206 and the semiconductor substrate 200 The first surface 201 and the second surface 202 have a certain inclination angle, but the inclination angle has little influence on the total reflection of the incident light rays at the interface and can be ignored. Therefore, in the case where the refractive index of the filling dielectric in the deep trench isolation structure 206 is less than 0.8 times the refractive index of the semiconductor substrate 200, incident light can be totally reflected at the interface.

The invention also provides a method for manufacturing a CMOS image sensor. Please refer to FIG. 4. FIG. 4 is a schematic flowchart of a method for manufacturing a CMOS image sensor according to an embodiment of the present invention. The method includes:

Step S1, providing a semiconductor substrate, the semiconductor substrate having a first surface and a third surface opposite thereto, the semiconductor substrate including at least one pixel unit area;

In step S2, a deep trench isolation structure is formed along the first surface in the semiconductor substrate, the deep trench isolation structure has a bottom along the trench depth direction, and the trench depth direction is perpendicular to the first surface. And the third surface, the deep trench isolation structure is located between adjacent pixel cell regions;

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Step S3, using the bottom of the deep trench isolation structure as a stop layer, thinning the semiconductor substrate along the third surface of the semiconductor substrate, stopping at the second surface, and exposing the second surface to the second surface. The bottom of the deep trench isolation structure. The technical scheme of the present invention will be described in detail with reference to the following embodiments. Please refer to FIG. 5 to FIG. 9. FIG. 5 to FIG. 9 are schematic cross-sectional views of a method for fabricating a CMOS image sensor according to the present invention.

First, referring to FIG. 5, a semiconductor substrate 200 is provided. The semiconductor substrate 200 has a first surface 201 and a third surface 211 opposite thereto. The semiconductor substrate 200 includes at least one pixel unit area 203. For convenience of description, the two pixel unit areas 203 of this embodiment are taken as an example for illustration. The pixel unit area 203 is for subsequent formation of pixels.

Then, a hard mask layer 207 having a first opening is formed between the adjacent pixel unit regions 203 of the first surface 201, and a material of the hard mask layer 207 may be oxide, silicon nitride, or the like. Then, the semiconductor substrate 200 is etched along the first opening, and a second opening 208 is formed in the semiconductor substrate 200. The second opening 208 is located between adjacent pixel unit regions 203. The second opening 208 has a 211 opening direction perpendicular to the first surface 201 and the third surface.

Next, referring to FIG. 6, a dielectric is filled in the second opening 208. The refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate 200. As an example, when the material of the semiconductor substrate 200 is silicon, the material of the dielectric is selected from silicon oxide. In this embodiment, the refractive index of silicon is 3.46, and the refractive index of silicon oxide is 1.46. Alternatively, when the material of the semiconductor substrate 200 is silicon, the material of the dielectric may be other dielectric (e.g., silicon nitride, silicon oxynitride, or the like) having a refractive index less than 0.8 times that of silicon. In other embodiments, the material of the semiconductor substrate 200 may be other semiconductor materials such as germanium, gallium arsenide, etc., and the material of the dielectric material has a refractive index less than 0.8 times the refractive index of the semiconductor substrate 200 . It can also be silicon nitride or silicon oxynitride. If the material of the dielectric is silicon oxide, the filling method may be high density plasma chemical vapor deposition (HDPCVD) and spin glass (SOG).

Then, referring to FIG. 7 , the dielectrics above the first surface 201 of the hard mask layer 207 and the second opening 208 are removed to form a deep trench isolation structure 206 with a deep trench isolation structure 206 along the trench depth direction. The bottom portion of the bottom portion of the deep trench isolation structure 206 is substantially perpendicular to the first surface 201 and the third surface 211. The deep trench isolation structure 206 has a depth ranging from 1.5 to 4 microns and a width of less than or equal to 0.25 microns. As one embodiment, the method of removing the dielectrics located above the first surface 201 of the hard mask layer 207 and the second opening 208 is a chemical mechanical polishing method.

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8, with the bottom of the deep trench isolation structure 206 as a stop layer, the semiconductor substrate 200 is thinned along the third surface 211 of the semiconductor substrate 200 to stop at the second surface 202. The second surface 202 exposes the bottom of the deep trench isolation structure 206 . The deep trench isolation structure 206 penetrates the first surface 201 of the semiconductor substrate 200 and the second surface 202 opposite thereto. As an embodiment, the thinning method includes a chemical mechanical polishing method. Since the material of the semiconductor substrate 200 is silicon, the dielectric filled in the deep trench isolation structure 206 is silicon oxide. The chemical mechanical polishing step has different polishing rates for silicon and silicon oxide. Therefore, the deep trench isolation structure 206 is The bottom can serve as a grinding stop.

9, a filter 209 and a micro lens 210 are sequentially formed in the pixel unit area 202, and a process of forming the filter 209 and the micro lens 210 includes a photolithography process. Deep trench isolation structure 206 is a photolithographically aligned mark. Since the deep trench isolation structure 206 is filled with an oxide and the material of the semiconductor substrate 200 is silicon, the color of the deep trench isolation structure 206 is different from the color of the semiconductor substrate 200 , and the deep trench isolation structure is exposed during exposure. The 206 can be used as a mark for photolithography alignment. Compared with the prior art special technology for making a photolithography alignment layer, a special photolithography alignment layer is not required, and the process steps are reduced. The material of the filter 209 is the same as the prior art. As an example, the material of the filter 209 is a photoresist material; the material of the micro lens 210 is the same as the prior art, and as an embodiment, the micro lens The material of 210 can be silicon nitride SiNX, zirconium oxide ZrO2, hafnium oxide HfO2, titanium oxide TiO2, aluminum oxide Al3O2, zinc oxide ZnO2, and the like.

In general, after the formation of the deep trench isolation structure 206 and the thinning process of the semiconductor substrate 200, pixels are generally formed in the pixel unit area 203. As a person skilled in the art, it will not be described here in detail.

In summary, the present invention provides a backlit CMOS image sensor having a deep trench isolation structure between pixel cell regions of the backlit CMOS image sensor. The deep trench isolation structure penetrates the semiconductor substrate. The first surface and the second surface are opposite to each other, so as to effectively isolate adjacent pixels, avoid the crosstalk of the electrical signals of adjacent pixels, improve the display fading problem of the CMOS image sensor, and improve the imaging quality. Further, the deep trench isolation structure is internally filled with a dielectric, the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate, and the light forms a total reflection at the interface between the deep trench isolation structure and the semiconductor substrate, avoiding Light enters adjacent pixels, causing crosstalk of optical signals to adjacent pixels, which further improves the display fading problem of CMOS image sensors and improves the imaging quality. At the same time, during the photolithography process of forming the filters and microlenses, the deep trench isolation structure can serve as a mark for photolithographic alignment,

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reducing the number of process steps.

Although the present invention has been disclosed as the preferred embodiments, it is not intended to limit the present invention. Any person skilled in the art can make possible changes and modifications without departing from the spirit and scope of the present invention. Therefore, the present invention The scope of protection shall be subject to the scope defined by the claims of the present invention.

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CLAIMS CN102270646

1.

A backlit CMOS image sensor includes:

一种背面照光的CMOS图像传感器，包括：

a semiconductor substrate, the semiconductor substrate having a first surface and a second surface opposite thereto;

半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面；

The semiconductor substrate includes at least one pixel unit area;

所述半导体衬底包括至少一个像素单元区域；

The isolation structure is located between adjacent pixel unit regions;

隔离结构，位于相邻像素单元区域之间；

The method is characterized in that the isolation structure is a deep trench isolation structure, and the deep trench isolation structure penetrates

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其特征在于，所述隔离结构为深沟槽隔离结构、所述深沟槽隔离结构贯穿

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The first surface and the second surface of the semiconductor substrate.

所述半导体衬底的第一表面和第二表面。

2.

The backlight-powered CMOS image sensor according to claim 1, wherein the width of the deep trench isolation structure is 0.25 μ m or less.

如权利要求1所述的背面照光的CMOS图像传感器，其特征在于，所述深沟槽隔离结构的宽度小于等于0.25微米。

3.

The backlight powered CMOS image sensor of claim 1, wherein the deep trench isolation structure has a depth in the range of 1.5 to 4 microns.

如权利要求1所述的背面照光的CMOS图像传感器，其特征在于，所述深沟槽隔离结构的深度范围为1.5～4微米。

4.

The backlight powered CMOS image sensor according to claim 1, wherein the filler in the deep trench isolation structure is a dielectric.

如权利要求1所述的背面照光的CMOS图像传感器，其特征在于，所述深沟槽隔离结构内填充物为电介质。

5.

The backlit CMOS image sensor according to claim 4, wherein the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate.

如权利要求4所述的背面照光的CMOS图像传感器，其特征在于，所述电介质的折射率小于所述半导体衬底的折射率的0.8倍。

6.

The backlight-source CMOS image sensor according to claim 1, wherein the semiconductor substrate is formed with a filter and a microlens in this order, and the filter and the microlens are located on the semiconductor

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substrate. Two surfaces.

如权利要求1所述的背面照光的CMOS图像传感器，其特征在于，所述半 导体衬底的依次形成有滤光片和微透镜，所述滤光片和微透镜位于所述半 导体衬底的第二表面。

7.

A method for fabricating a backside illuminated CMOS image sensor, comprising: providing a semiconductor substrate, the semiconductor substrate having a first surface and a third surface opposite thereto, the semiconductor substrate including at least one pixel Unit area

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一种背面照光的CMOS图像传感器的制作方法，其特征在于，包括：提供半导体衬底，所述半导体衬底具有第一表面和与之相对的第三表面，所述半导体衬底包括至少一个像素单元区域；

A deep trench isolation structure is formed in the semiconductor substrate along the first surface, the deep trench isolation structure has a bottom along a depth direction of the trench, the trench depth direction is perpendicular to the first surface and the third The surface, the deep trench isolation structure is located between adjacent pixel cell regions;

沿所述第一表面在所述半导体衬底内形成深沟槽隔离结构，所述深沟槽隔 离结构具有沿槽深方向的底部，所述槽深方向垂直于所述第一表面和第三 表面，所述深沟槽隔离结构位于相邻的像素单元区域之间；

The bottom of the deep trench isolation structure is used as a stop layer, the semiconductor substrate is thinned along the third surface of the semiconductor substrate, stops at the second surface, and the second surface exposes the deep trench The bottom of the isolation structure.

以所述深沟槽隔离结构的底部为停止层，沿所述半导体衬底第三表面对所 述半导体衬底进行减薄，停止在第二表面，所述第二表面露出所述深沟槽 隔离结构的底部。

8.

The method of fabricating a backlit CMOS image sensor according to claim 7, wherein the thinning method includes a chemical mechanical polishing method.

如权利要求7所述的背面照光的CMOS图像传感器的制作方法，其特征在 于，所述减薄方法包括化学机械研磨的方法。

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9.

The method of fabricating a backlit CMOS image sensor according to claim 7, wherein forming the deep trench isolation structure in the semiconductor substrate along the first surface comprises the following steps:

如权利要求7所述的背面照光的CMOS图像传感器的制作方法，其特征在于，所述沿所述第一表面在所述半导体衬底内形成深沟槽隔离结构包括步骤：

a hard mask layer having a first opening is formed between adjacent pixel cell regions of the first surface; the semiconductor substrate is etched along the first opening, and a second opening is formed in the semiconductor substrate;

在第一表面的相邻像素单元区域之间形成具有第一开口的硬掩膜层；沿所述第一开口对半导体衬底进行刻蚀，在所述半导体衬底内形成第二开口；

Filling the second opening with a dielectric

在所述第二开口内填充电介质，

The hard mask layer is removed to form a deep trench isolation structure.

去除所述硬掩膜层，形成深沟槽隔离结构。

10.

The method of fabricating a backlit CMOS image sensor according to claim 9, wherein the deep trench isolation structure has a depth in the range of 1.5 to 4 microns.

如权利要求9所述的背面照光的CMOS图像传感器的制作方法，其特征在于，所述深沟槽隔离结构的深度范围为1.5～4微米。

11.

The method of fabricating a backlit CMOS image sensor according to claim 9, wherein the width of the deep trench isolation structure is less than or equal to 0.25 micrometers.

如权利要求9所述的背面照光的CMOS图像传感器的制作方法，其特征在于，所述深沟槽隔离结构的宽度小于等于0.25微米。

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12.

The method of fabricating a back light CMOS image sensor according to claim 9, wherein the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate.

如权利要求9所述的背面照光的CMOS图像传感器的制作方法，其特征在于，所述电介质的折射率小于所述半导体衬底的折射率的0.8倍。

13.

The method for fabricating a backlit CMOS image sensor according to claim 7, further comprising: forming a filter and a microlens sequentially along the second surface with the pixel unit area, the filter and The fabrication method of the microlens includes a photolithography step in which the deep trench isolation structure is used as a mark for photolithography alignment.

如权利要求7所述的背面照光的CMOS图像传感器的制作方法，其特征在于，还包括：在与像素单元区域沿所述第二表面依次形成滤光片和微透镜，所述滤光片和微透镜的制作方法包括光刻步骤，所述光刻步骤中以所述深沟槽隔离结构作为光刻对准的标记。

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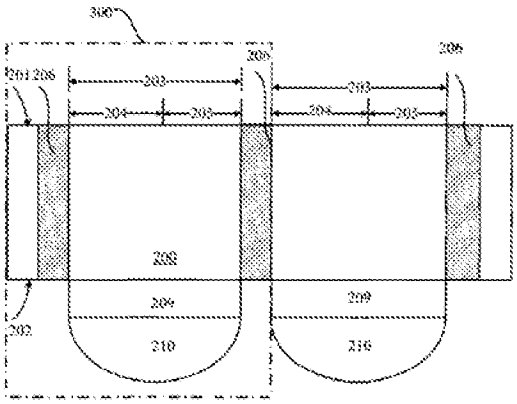
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(54)发明名称

背面照光的CMOS图像传感器

(57)摘要

本发明提供背面照光的CMOS图像传感器，包括：半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面；所述半导体衬底包括至少一个像素单元区域；隔离结构，位于相邻像素单元区域之间；其中，所述隔离结构为深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬底的第一表面和第二表面。本发明减少了相邻像素单元区域之间的电信号的串扰，改善了CMOS图像传感器的显示颜色，提高了成像质量。



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1. 一种背面照光的 CMOS 图像传感器，包括：

半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面；

所述半导体衬底包括至少一个像素单元区域；

隔离结构，位于相邻像素单元区域之间；

其特征在于，所述隔离结构为深沟槽隔离结构，所述深沟槽隔离结构贯穿

所述半导体衬底的第一表面和第二表面。

2. 如权利要求 1 所述的背面照光的 CMOS 图像传感器，其特征在于，所述深沟槽隔离结构的宽度小于等于 0.25 微米。

3. 如权利要求 1 所述的背面照光的 CMOS 图像传感器，其特征在于，所述深沟槽隔离结构的深度范围为 1.5 ～ 4 微米。

4. 如权利要求 1 所述的背面照光的 CMOS 图像传感器，其特征在于，所述深沟槽隔离结构内填充物为电介质。

5. 如权利要求 4 所述的背面照光的 CMOS 图像传感器，其特征在于，所述电介质的折射率小于所述半导体衬底的折射率的 0.8 倍。

6. 如权利要求 1 所述的背面照光的 CMOS 图像传感器，其特征在于，所述半导体衬底的依次形成有滤光片和微透镜，所述滤光片和微透镜位于所述半导体衬底的第二表面。

7. 一种背面照光的 CMOS 图像传感器的制作方法，其特征在于，包括：提供半导体衬底，所述半导体衬底具有第一表面和与之相对的第三表面，所述半导体衬底包括至少一个像素单元区域；

沿所述第一表面在所述半导体衬底内形成深沟槽隔离结构，所述深沟槽隔离结构具有沿槽深方向的底部，所述槽深方向垂直于所述第一表面和第三表面，所述深沟槽隔离结构位于相邻的像素单元区域之间；

以所述深沟槽隔离结构的底部为停止层，沿所述半导体衬底第三表面对所述半导体衬底进行减薄，停止在第二表面，所述第二表面露出所述深沟槽隔离结构的底部。

8. 如权利要求 7 所述的背面照光的 CMOS 图像传感器的制作方法，其特征在于，所述减薄方法包括化学机械研磨的方法。

9. 如权利要求 7 所述的背面照光的 CMOS 图像传感器的制作方法，其特征在于，所述沿所述第一表面在所述半导体衬底内形成深沟槽隔离结构包括步骤：

在第一表面的相邻像素单元区域之间形成具有第一开口的硬掩膜层；沿所述第一开口对半导体衬底进行刻蚀，在所述半导体衬底内形成第二开口；

在所述第二开口内填充电介质，

去除所述硬掩膜层，形成深沟槽隔离结构。

10. 如权利要求 9 所述的背面照光的 CMOS 图像传感器的制作方法，其特征在于，所述深沟槽隔离结构的深度范围为 1.5 ～ 4 微米。

11. 如权利要求 9 所述的背面照光的 CMOS 图像传感器的制作方法，其特征在于，所述深沟槽隔离结构的宽度小于等于 0.25 微米。

12. 如权利要求 9 所述的背面照光的 CMOS 图像传感器的制作方法，其特征在于，所述电介质的折射率小于所述半导体衬底的折射率的 0.8 倍。

13. 如权利要求 7 所述的背面照光的 CMOS 图像传感器的制作方法，其特征在于，还包

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括：在与像素单元区域沿所述第二表面依次形成滤光片和微透镜，所述滤光片和微透镜的制作方法包括光刻步骤，所述光刻步骤中以所述深沟槽隔离结构作为光刻对准的标记。

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背面照光的 CMOS 图像传感器

技术领域

[0001] 本发明涉及图像传感器，特别涉及背面照光的 CMOS 图像传感器。

背景技术

[0002] 图像传感器是组成数字摄像头的重要组成部分，根据元件不同分为电荷耦合 (CCD, Charge Coupled Device) 图像传感器和金属氧化物半导体 (CMOS, Complementary Metal-Oxide Semiconductor) 图像传感器。其中，由于 CMOS 图像传感器集成度高，容易与标准的 CMOS 制作工艺兼容，并且功耗低，随着 CMOS 制作工艺的改进，CMOS 图像传感器成为目前图像传感器的主流技术。

[0003] 在申请号为 200710148796.5 的中国专利申请中公开了一种现有的 CMOS 图像传感器。现有的 CMOS 图像传感器包括半导体衬底，所述半导体衬底通常包括若干呈矩阵排布的像素单元区域，相邻的像素单元区域之间具有浅沟槽隔离结构 (STI)。请参考图 1，图 1 是现有的 CMOS 图像传感器结构示意图，所述 CMOS 图像传感器包括：半导体衬底 100，所述半导体衬底 100 包括若干像素单元区域 103，图中以 2 个像素单元区域 103 为例进行说明；相邻像素单元区域 103 之间具有浅沟槽隔离结构 106。其中所述像素单元区域 103 用于形成像素，通常所述像素单元区域 103 包括光电二极管区域 104 和晶体管区域 105，所述光电二极管区域 104 用于形成光电二极管，所述光电二极管用于光电转换；所述晶体管区域 105 用于形成晶体管，所述晶体管用于将光电二极管转换的电信号放大后输出。所述浅沟槽隔离结构 106 用于相邻像素的隔离。所述半导体衬底 100 包括第一表面 101 和与之相对的第二表面 102。光线从第二表面 102 进入像素单元区域 103 内。本领域技术人员将所述 CMOS 图像传感器称为背面照光的 (Backside illuminated)CMOS 图像传感器。

[0004] 在实际中发现，上述背面照光的 CMOS 图像传感器具有显示褪色的问题，影响了成像质量。

[0005] 因此，需要一种背面照光的 CMOS 图像传感器，能够改善显示褪色的问题，提高 CMOS 图像传感器的成像质量。

发明内容

[0006] 本发明解决的问题是提供了一种背面照光的 CMOS 图像传感器，能够改善显示褪色的问题，提高 CMOS 图像传感器的成像质量。

[0007] 为解决上述问题，本发明提供一种背面照光的 CMOS 图像传感器，包括：

[0008] 半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面；

[0009] 所述半导体衬底包括至少一个像素单元区域；

[0010] 隔离结构，位于相邻像素单元区域之间；

[0011] 其中，所述隔离结构为深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬底的第一表面和第二表面。

[0012] 可选的，所述深沟槽隔离结构的宽度小于等于 0.25 微米。

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[0013] 可选的，所述深沟槽隔离结构的深度范围为 1.5 ～ 4 微米。

[0014] 可选的，所述深沟槽隔离结构内填充物为电介质。

[0015] 可选的，所述电介质的折射率小于所述半导体衬底的折射率的 0.8 倍。

[0016] 可选的，所述半导体衬底的依次形成有滤光片和微透镜，所述滤光片和微透镜位于所述半导体衬底的第二表面。

[0017] 本发明还提供一种背面照光的 CMOS 图像传感器的制作方法，包括：

[0018] 提供半导体衬底，所述半导体衬底具有第一表面和与之相对的第三表面，所述半导体衬底包括至少一个像素单元区域；

[0019] 沿所述第一表面在所述半导体衬底内形成深沟槽隔离结构，所述深沟槽隔离结构具有沿槽深方向的底部，所述槽深方向垂直于所述第一表面和第三表面，所述深沟槽隔离结构位于相邻的像素单元区域之间；

[0020] 以所述深沟槽隔离结构的底部为停止层，沿所述半导体衬底第三表面对所述半导体衬底进行减薄，停止在第二表面，所述第二表面露出所述深沟槽隔离结构的底部。

[0021] 可选的，所述减薄方法包括化学机械研磨的方法。

[0022] 可选的，所述沿所述第一表面在所述半导体衬底内形成深沟槽隔离结构包括步骤：

[0023] 在第一表面的相邻像素单元区域之间形成具有第一开口的硬掩膜层；

[0024] 沿所述第一开口对半导体衬底进行刻蚀，在所述半导体衬底内形成第二开口；

[0025] 在所述第二开口内填充电介质，

[0026] 去除所述硬掩膜层，形成深沟槽隔离结构。

[0027] 可选的，所述深沟槽隔离结构的深度范围为 1.5 ～ 4 微米。

[0028] 可选的，所述深沟槽隔离结构的宽度小于等于 0.25 微米。

[0029] 可选的，所述电介质的折射率小于所述半导体衬底的折射率的 0.8 倍。

[0030] 可选的，还包括：在与像素单元区域沿所述第二表面依次形成滤光片和微透镜，所述滤光片和微透镜的制作方法包括光刻步骤，所述光刻步骤中以所述深沟槽隔离结构作为光刻对准的标记。

[0031] 与现有技术相比，本发明具有以下优点：

[0032] 通过在相邻像素单元区域之间设置贯穿半导体衬底的第一表面和第二表面的深沟槽隔离结构，进行相邻像素间的隔离，避免了像素单元区域内的光生载流子扩散至相邻像素单元区域，减少对相邻像素单元区域造成电信号的串扰，改善了 CMOS 图像传感器的显示褪色，提高了成像质量。

[0033] 进一步地，所述深沟槽隔离结构内的填充物为电介质，所述电介质的折射率小于半导体衬底折射率的 0.8 倍，光线在深沟槽隔离结构和半导体衬底的界面形成全反射，避免光线经深沟槽隔离结构进入相邻的像素单元区域，减小了对相邻像素单元区域的光信号的串扰，进一步改善了 CMOS 图像传感器的显示褪色，提高了成像质量；所述深沟槽隔离结构填充电介质为氧化硅，与半导体衬底的硅具有不同的颜色，在进行光刻工艺形成滤光片和微透镜的过程中，深沟槽隔离结构可以作为光刻的对准标记，无需专门的对准层，节省了工艺步骤，降低了生产成本。

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附图说明

[0034] 图 1 是现有技术 CMOS 图像传感器结构示意图。

[0035] 图 2 是本发明的一个实施例的 CMOS 图像传感器结构示意图。

[0036] 图 3 是光线在深沟槽隔离结构与半导体衬底界面形成全反射原理示意图。

[0037] 图 4 是本发明的一个实施例的 CMOS 图像传感器的制作方法流程示意图。

[0038] 图 5 ～图 9 是本发明 CMOS 图像传感器制作方法剖面结构示意图。

具体实施方式

[0039] 现有的背面照光的 (Backside illuminated)CMOS 图像传感器存在显示褪色的问题。经发明人研究发现，褪色的原因是相邻像素的串扰 (crosstalk)。所述串扰的原因之一是现有的浅沟槽隔离结构无法有效隔离相邻的像素单元之间光生载流子扩散。由于采用背面照光的 CMOS 图像传感器的入射光线经过微透镜和滤光片进入半导体衬底的像素单元区域，现有技术为了提高像素单元区域内的光电二极管的有效感光面积，通常光电二极管的深度较大，其深度可达 10000 埃以上，而现有的浅沟槽隔离结构的深度范围通常为 2000 ～ 5000 埃。在进行光电转换时，所述光电二极管光电转换所产生的光生载流子可能扩散，而现有的浅沟槽隔离结构无法有效隔离光生载流子，从而光生载流子可能至相邻像素，对相邻像素造成电信号的串扰，从而导致 CMOS 图像传感器的显示褪色。

[0040] 本发明提供的背面照光的 CMOS 图像传感器解决了电信号的串扰，改善了 CMOS 图像传感器的显示褪色问题，所述背面照光的 CMOS 图像传感器包括：

[0041] 半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面；

[0042] 所述半导体衬底包括至少一个像素单元区域；

[0043] 隔离结构，位于相邻像素单元区域之间；

[0044] 其中，所述隔离结构为深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬底的第一表面和第二表面。

[0045] 下面将结合具体的实施例对本发明的技术方案进行详细的说明。请参考图 2，图 2 是本发明一个实施例的 CMOS 图像传感器结构示意图。

[0046] 所述 CMOS 图像传感器包括半导体衬底 200，所述半导体衬底 200 的材料可以是硅、SOI、氮化镓或者砷化镓。所述半导体衬底 200 具有第一表面 201 和与之相对的第二表面 202。本实施例中，所述半导体衬底 200 为具有 P 型导电类型的硅衬底。

[0047] 如图 2，所述半导体衬底 200 包括至少一个像素单元区域 203，为了便于说明，以 2 个像素单元区域 203 为例进行说明。相邻的像素单元区域 203 之间具有深沟槽隔离结构 206。所述深沟槽隔离结构 206 贯穿所述半导体衬底 200 的第一表面 201 和第二表面 202。半导体衬底 200 的像素单元区域 203 形成有滤光片 209 和微透镜 210。本实施例中，所述微透镜 210 的折射率范围为 1.2 ～ 4，其材质可以为氮化硅 SiN_x、氧化锆 ZrO_2、氧化铪 HfO_2、氧化钛 TiO_2、氧化铝 Al_2O_3、氧化锌 ZnO_2 等，所述滤光片 209 的折射率范围为 1.4 ～ 2，其材质可以为光阻材料。所述滤光片 209 和微透镜 210 通过光刻工艺形成，在形成滤光片的光刻工艺过程中，深沟槽隔离结构 206 可以作为光刻的对准标记使用。

[0048] 仍参考图 2，所述像素单元区域 203 用于形成像素。所述像素单元区域 203 包括光电二极管区域 204 和晶体管区域 205。所述光电二极管区域 204 用于形成光电二极管，所述

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光电二极管用于进行光电转换，将从第二表面 202 入射的光信号转换为相应的电信号，产生光生载流子。所述晶体管区域 205 用于形成晶体管，所述晶体管用于将所述光电二极管转换的电信号放大、输出。根据实际情况，所述晶体管区域 205 内包括 3 个或 3 个以上晶体管，所述晶体管之间具有浅沟槽隔离结构，用于像素内的晶体管之间相互隔离。所述浅沟槽隔离结构的深度范围为 2000 ～ 5000 埃。

[0049] 本实施例中，所述深沟槽隔离结构 206 贯穿所述半导体衬底 200 的第一表面 201 和第二表面 202。作为一个实施例，所述半导体衬底 200 的厚度范围为 1.5 ～ 4 微米，所述深沟槽隔离结构 206 的厚度应与所述半导体衬底 200 的深度相同，即为 1.5 ～ 4 微米。作为优选的实施例，所述半导体衬底 200 的厚度为 2 ～ 3 微米，以使得像素单元区域 203 内的光电二极管能更好的吸收入射光线，相应地，所述深沟槽隔离结构 206 的深度范围优选为 2 ～ 3 微米。由于所述深沟槽隔离结构 206 贯穿所述半导体衬底 200 的第一表面 201 和第二表面 202，因此，深沟槽隔离结构 206 可以有效阻止像素的光电二极管在光电转换时产生的光生载流子扩散至相邻像素，减少对相邻像素的电信号的串扰，改善 CMOS 图像传感器的像素褪色，提高了 CMOS 图像传感器的成像质量。

[0050] 所述深沟槽隔离结构 206 的宽度小于或等于现有技术的浅沟槽隔离结构的宽度，以节约芯片面积。作为一个实施例，所述深沟槽隔离结构 206 的宽度范围为小于等于 0.25 微米。

[0051] 所述深沟槽隔离结构 206 内填充物为电介质，所述电介质的折射率小所述半导体衬底的折射率的 0.8 倍。这样入射光线进入像素单元区域 203 时在深沟槽隔离结构 203 与半导体衬底 200 的界面形成全反射，避免入射光线经过深沟槽隔离结构 206 进入相邻像素单元区域 203，对相邻像素单元区域 203 造成光信号的串扰，进一步改善 CMOS 图像传感器的显示褪色的问题。为了便于说明光线在深沟槽隔离结构和半导体衬底的界面形成全反射的原理，对图 2 中 CMOS 图像传感器的部分区域 300 进行放大说明。所述部分区域 300 包括像素单元区域 203、与之对应的滤光片 209、微透镜 210、以及像素单元区域 203 两侧的深沟槽隔离结构 206。请参考图 3，图 3 是光线在深沟槽隔离结构与半导体衬底界面形成全反射原理示意图。

[0052] 如图 3 所示，光线 A 自空气经过微透镜 210、滤光片 209、半导体衬底 200 的第二表面 202 进入像素单元区域 203，理想的状况是，光线 A 被像素单元区域 203 的光电二极管吸收，但是，由于光线 A 可能具有一定倾斜角因此光线可能会入射深沟槽隔离结构 206 与半导体衬底 200 的界面。由于通常空气、微透镜 210、滤光片 209、半导体衬底 200 的材质不同而折射率不同，光线 A 到达深沟槽隔离结构 206 与半导体衬底 200 的界面发生多次光的折射。具体地，在微透镜 210 和空气界面的法线为 01，在空气中光线 A 与所述法线 01 的夹角为 a1，经过折射，在微透镜 210 内光线 A 与法线 01 的夹角为 a2；光线 A 在微透镜 210 内传输至微透镜 210 和滤光片 209 的界面，所述微透镜 210 和滤光片 209 的界面的法线为 02，在微透镜 210 内光线 A 与所述法线 02 的夹角为 a3，经过折射，在滤光片 209 内光线 A 与所述法线 02 的夹角为 aa4；光线 A 在滤光片 209 内传输至滤光片 209 与半导体衬底 200 的界面，所述滤光片 209 与半导体衬底 200 的界面的法线为 03，在滤光片 209 内所述光线 A 与所述法线 03 的夹角为 a5，经过折射，在半导体衬底 200 内光线 A 与法线 03 的夹角 a6；在半导体衬底 200 内，所述光线 A 传输至半导体衬底 200 与所述深沟槽隔离结构 206 的界面，所述半导体

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衬底 200 与所述深沟槽隔离结构 206 的界面的法线为 O4，在半导体衬底 200 内光线 A 与法线 O4 的夹角为 β。本实施例中，深沟槽隔离结构 206 与半导体衬底 200 的界面垂直于滤光片 209 与半导体衬底 200 的界面，因此，法线 O4 与法线 O3 垂直，从而，角度 β 与角度 a6 互为余角。

[0053] 由于在实际中，本领域技术人员对微透镜 210 的厚度、滤光片 209 的厚度进行优化设置，可以使得使得角度 a6 与角度 a1 相同。角度 a1 的最大值称为主光线倾斜角 (chief ray angle，CRA)，而主光线倾斜角的角度范围为 0 ～ 35°。因此，角度 a6 倾斜角度范围为 0 ～ 35°，角度 a6 的余角 β 的角度范围为 55 ～ 90°，即光线与法线 O4 的入射角范围为 55 ～ 90°。因此，假设全反射临界角为 α，若要光线在半导体衬底 200 与深沟槽隔离结构 206 的界面形成全反射，α 应小于为 55°，以保证在光线与法线 O4 的入射角范围为 55 ～ 90° 时，任一入射角均大于 α，从而光线与法线 O4 的入射角为 55 ～ 90° 时可以形成全反射。假设全反射临界角为 55°，半导体衬底 200 的折射率为 x，深沟槽隔离结构 206 内填充的电介质的折射率为 y，则根据全反射计算公式：sin55° /sin90° = y/x

[0054] y = sin55° *x = 0.8*x

[0055] 由上述分析可知，当全反射临界角为 55° 时，对应的深沟槽隔离结构 206 内填充的电介质的折射率为半导体衬底 200 的折射率的 0.8 倍。

[0056] 由于全反射的临界角 α 取决于半导体衬底 200 的折射率和深沟槽隔离结构 206 内填充电介质的折射率关系。具体地，在半导体衬底 200 的折射率一定的情况下，深沟槽隔离结构 206 内填充的电介质的折射率越小，全反射的临界角 α 越小。由前面的分析可知，在全反射的临界角为 55° 时对应的深沟槽隔离结果 206 内的电介质的折射率为半导体衬底 200 折射率的 0.8 倍。若要使得全反射临界角小于 55°，深沟槽隔离结构 206 内填充的电介质的折射率应小于半导体衬底 200 折射率的 0.8 倍，以保证光线 A 在深沟槽隔离结构 206 和半导体衬底 200 的界面发生全反射。从而，光线 A 留在像素单元区域 203 内，避免光线 A 经过深沟槽隔离结构 206 对相邻像素单元区域造成串扰，进一步改善现有的 CMOS 图像传感器的显示褪色现象。

[0057] 作为一个实施例，所述半导体衬底 200 的材质为硅时，所述深沟槽隔离结构 206 的填充物可以为氧化硅，并且所述氧化硅的折射率可以小于等于硅的折射率的 0.8 倍。本实施例中，硅的折射率为 3.46，氧化硅的折射率为 1.46，这样入射光线在深沟槽隔离结构 206 和半导体衬底 200 的界面可以形成全反射。可替代地，在深沟槽隔离结构 206 内填充的电介质的折射率小于等于硅衬底的折射率的 0.8 倍前提下，深沟槽隔离结构 206 内填充的电介质可以为其他材质。当半导体衬底 200 的材质为其他半导体材料时，深沟槽隔离结构 206 内填充的电介质的材质还可以为其他材质，但是深沟槽隔离结构 206 内填充的电介质的折射率应小于半导体衬底 200 折射率的 0.8 倍，以保证在深沟槽隔离结构 206 和半导体衬底 200 的界面形成全反射。

[0058] 需要说明的是，上述分析以深沟槽隔离结构 206 沿垂直于第一表面 201 和第二表面 202 的宽度一致，从而深沟槽隔离结构 206 与半导体衬底 200 的界面为垂直于第一表面 201 和第二表面 202 为例进行说明。在实际中，由于制造工艺的限制，深沟槽隔离结构 206 沿垂直于第一表面 201 至第二表面 202 方向的宽度可能不均匀，导致深沟槽隔离结构 206 与半导体衬底 200 的界面与第一表面 201 和第二表面 202 之间具有一定的倾斜角度，但是

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所述倾斜角度对入射光线在所述界面形成全反射的影响较小，可以忽略不计。因此，在深沟槽隔离结构 206 内填充电介质的折射率小于半导体衬底 200 折射率的 0.8 倍的情况下，入射光线在所述界面可以形成全反射。

[0059] 本发明还提供一种 CMOS 图像传感器的制作方法。请参考图 4，图 4 是本发明一个实施例的 CMOS 图像传感器的制作方法流程示意图。所述方法包括：

[0060] 步骤 S1，提供半导体衬底，所述半导体衬底具有第一表面和与之相对的第三表面，所述半导体衬底包括至少一个像素单元区域；

[0061] 步骤 S2，沿所述第一表面在所述半导体衬底内形成深沟槽隔离结构，所述深沟槽隔离结构具有沿槽深方向的底部，所述槽深方向垂直于所述第一表面和第三表面，所述深沟槽隔离结构位于相邻的像素单元区域之间；

[0062] 步骤 S3，以所述深沟槽隔离结构的底部为停止层，沿所述半导体衬底第三表面对所述半导体衬底进行减薄，停止在第二表面，所述第二表面露出所述深沟槽隔离结构的底部。下面结合实施例对本发明的技术方案进行详细说明。请参考图 5～图 9，图 5～图 9 是本发明的 CMOS 图像传感器制作方法剖面结构示意图。

[0063] 首先，请参考图 5，提供半导体衬底 200，所述半导体衬底 200 具有第一表面 201 和与之相对的第三表面 211。所述半导体衬底 200 包括至少一个像素单元区域 203，为了便于说明，本实施例 2 个像素单元区域 203 为例进行说明。所述像素单元区域 203 用于后续形成像素。

[0064] 然后，在第一表面 201 的相邻的像素单元区域 203 之间形成具有第一开口的硬掩膜层 207，所述硬掩膜层 207 的材质可以为氧化物、氮化硅等。然后，沿所述第一开口对半导体衬底 200 进行刻蚀，在所述半导体衬底 200 内形成第二开口 208，所述第二开口 208 位于相邻像素单元区域 203 之间。所述第二开口 208 具有垂直于第一表面 201 和第三表面的 211 开口方向。

[0065] 接着，参考图 6，在所述第二开口 208 内填充电介质。所述电介质的折射率小于半导体衬底 200 的折射率的 0.8 倍。作为一个实施例，当所述半导体衬底 200 的材质为硅时，所述电介质的材质选自氧化硅。本实施例中，硅的折射率为 3.46，氧化硅的折射率为 1.46。可替代的，当所述半导体衬底 200 的材质为硅时，所述电介质的材质可以为折射率小于硅的折射率的 0.8 倍的其他电介质（例如是氮化硅或氮氧化硅等）。在其他的实施例中，所述半导体衬底 200 的材质可以为锗、砷化镓等其他半导体材料，在折射率小于半导体衬底 200 的折射率的 0.8 倍的前提下，所述电介质的材质也可以为氮化硅或氮氧化硅。若所述电介质的材质为氧化硅，其填充方法可以为高密度等离子体化学气相沉积法 (HDPCVD) 和自旋玻璃法 (SOG)。

[0066] 然后，参考图 7，去除所述硬掩膜层 207 和第二开口 208 的位于第一表面 201 上方的电介质，形成深沟槽隔离结构 206，所述深沟槽隔离结构 206 具有沿槽深方向的底部，所述槽深方向与第二开口 208 的开口方向一致，即所述深沟槽隔离结构 206 的槽深方向垂直于所述第一表面 201 和第三表面 211。所述深沟槽隔离结构 206 的深度范围为 1.5～4 微米，其宽度小于等于 0.25 微米。作为一个实施例，所述去除所述硬掩膜层 207 和第二开口 208 的位于第一表面 201 上方的电介质的方法为化学机械研磨的方法。

[0067] 然后，参考图 8，以所述深沟槽隔离结构 206 的底部为停止层，沿所述半导体衬底

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200 第三表面 211 对半导体衬底 200 进行减薄，停止在第二表面 202，所述第二表面 202 露出所述深沟槽隔离结构 206 的底部。所述深沟槽隔离结构 206 贯穿所述半导体衬底 200 的第一表面 201 和与之相对的第二表面 202。作为一个实施例，所述减薄方法包括化学机械研磨方法。由于半导体衬底 200 的材质为硅，深沟槽隔离结构 206 内填充的电介质为氧化硅，所述化学机械研磨步骤对硅和氧化硅具有不同的研磨速率，因此，深沟槽隔离结构 206 的底部可以作为研磨的停止层。

[0068] 接着，参考图 9，在所述像素单元区域 202 依次形成滤光片 209 和微透镜 210，所述滤光片 209 和微透镜 210 的形成过程包括光刻工艺，所述光刻工艺以所述深沟槽隔离结构 206 为光刻对准的标记。由于深沟槽隔离结构 206 内填充氧化物，而半导体衬底 200 的材质为硅，所述深沟槽隔离结构 206 的颜色与半导体衬底 200 的颜色不同，在曝光时，深沟槽隔离结构 206 可以作为光刻对准的标记，与现有技术专门制作光刻对准层的技术相比，不需要专门的光刻对准层，减少工艺步骤。所述滤光片 209 的材质与现有技术相同，作为一个实施例，滤光片 209 的材质为光阻材料；所述微透镜 210 的材质与现有技术相同，作为一个实施例，微透镜 210 的材质为可以为氮化硅 SiN_x、氧化锆 ZrO_2、氧化铪 HfO_2、氧化钛 TiO_2、氧化铝 Al_2O_3、氧化锌 ZnO_2 等。

[0069] 通常，在深沟槽隔离结构 206 形成之后和对半导体衬底 200 进行减薄工艺之前，通常要在像素单元区域 203 内形成像素。作为本领域技术人员的公知技术，在此不做详细说明。

[0070] 综上，本发明提供了一种背面照光的 CMOS 图像传感器，所述背面照光的 CMOS 图像传感器的像素单元区域之间具有深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬底的第一表面和与之相对的第二表面，从而有效隔离相邻像素，避免了相邻像素电信号的串扰，改善了 CMOS 图像传感器的显示褪色问题，提高了成像质量。进一步地，所述深沟槽隔离结构内部填充电介质，所述电介质的折射率小于半导体衬底的折射率的 0.8 倍，光线在深沟槽隔离结构和半导体衬底的界面上形成全反射，避免光线进入相邻像素，对相邻像素造成光信号的串扰，更加改善了 CMOS 图像传感器的显示褪色问题，提高了成像质量。同时，在形成滤光片和微透镜的光刻工艺时，所述深沟槽隔离结构可以作为光刻对准的标记，减少了工艺步骤。

[0071] 本发明虽然以较佳实施例公开如上，但其并不是用来限定本发明，任何本领域技术人员在不脱离本发明的精神和范围内，都可以做出可能的变动和修改，因此本发明的保护范围应当以本发明权利要求所界定的范围为准。

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Espacenet

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CMOS image sensor with back illumination

Inventor(s): JIEGUANG HUO ± (HUO JIEGUANG)

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Classification: **- international:** ***H01L27/146***
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Priority number(s): CN20102222129U 20100601

Abstract of CN201725796 (U)

The utility model provides a CMOS image sensor with back illumination. The image sensor comprises: a semiconductor substrate that is provided with a first surface and a second surface opposite to the first surface and comprises at least one pixel unit area, and an isolation structure between adjacent pixel unit areas, wherein the isolation structure is deep trench isolation structure that penetrates through the first surface and the second surface of the semiconductor substrate. The CMOS image sensor reduces the crosstalk of electric signals between adjacent pixel unit areas, improves the display fading of CMOS image sensors and enhances imaging quality.

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DESCRIPTION CN201725796

The utility model provides a back-illuminated CMOS image sensor, comprising: a semiconductor substrate, the semiconductor substrate having a first surface and a second surface opposite thereto; the semiconductor substrate comprising at least one pixel unit area; an isolation structure, Located between adjacent pixel cell regions; wherein the isolation structure is a deep trench isolation structure that penetrates the first surface and the second surface of the semiconductor substrate. The utility model reduces the crosstalk of electrical signals between adjacent pixel unit regions, improves the display fading of the CMOS image sensor, and improves the imaging quality.

Backlighting CMOS image sensor

Technical field

The utility model relates to an image sensor, in particular to a CMOS image sensor with backlighting.

Background technique

The image sensor is an important part of the digital camera. According to the different components, the image sensor is divided into a Charge Coupled Device (CCD) image sensor and a Metal Oxide Semiconductor (CMOS) image sensor. Among them, due to the high integration of CMOS image sensors, it is easy to be compatible with standard CMOS fabrication processes, and the power consumption is low. With the improvement of CMOS fabrication processes, CMOS image sensors have become the mainstream technology of current image sensors.

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An existing CMOS image sensor is disclosed in Chinese Patent Application No. 200710148796.5. Existing CMOS image sensors include a semiconductor substrate, which typically includes a plurality of pixel cell regions arranged in a matrix with shallow trench isolation structures (STIs) between adjacent pixel cell regions. Please refer to FIG. 1. FIG. 1 is a schematic structural diagram of a conventional CMOS image sensor. The CMOS image sensor includes a semiconductor substrate 100. The semiconductor substrate 100 includes several pixel unit regions 103. In the figure, there are two pixel unit regions. 103 is described as an example; there is a shallow trench isolation structure 106 between adjacent pixel cell regions 103 . The pixel unit area 103 is used to form a pixel. The pixel unit area 103 generally includes a photodiode area 104 and a transistor area 105. The photodiode area 104 is used to form a photodiode, and the photodiode is used for photoelectric conversion. The transistor region 105 is used to form a transistor for amplifying and outputting an electrical signal converted by a photodiode. The shallow trench isolation structure 106 is used for isolation of adjacent pixels. The semiconductor substrate 100 includes a first surface 101 and a second surface 102 opposite thereto. Light enters the pixel unit area 103 from the second surface 102 . Those skilled in the art refer to the CMOS image sensor as a Backside illuminated CMOS image sensor.

In practice, it has been found that the above-mentioned back-illuminated CMOS image sensor has a problem of fading, which affects the image quality.

Therefore, there is a need for a back-illuminated CMOS image sensor that can improve the display fading problem and improve the image quality of the CMOS image sensor.

Utility model content

The utility model solves the problem that the invention provides a backlight CMOS image sensor, which can improve the display fading problem and improve the imaging quality of the CMOS image sensor.

To solve the above problems, the present invention provides a backlit CMOS image sensor including:

a semiconductor substrate, the semiconductor substrate having a first surface and a second surface opposite thereto;

The semiconductor substrate includes at least one pixel unit area;

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The isolation structure is located between adjacent pixel unit regions;

Wherein, the isolation structure is a deep trench isolation structure, and the deep trench isolation structure penetrates the first surface and the second surface of the semiconductor substrate.

Optionally, the width of the deep trench isolation structure is less than or equal to 0.25 micrometers.

Optionally, the depth of the deep trench isolation structure ranges from 1.5 to 4 microns.

Optionally, the filler in the deep trench isolation structure is a dielectric.

Optionally, the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate.

Optionally, the semiconductor substrate is sequentially formed with a filter and a microlens, and the filter and the microlens are located on the second surface of the semiconductor substrate.

Compared with the prior art, the utility model has the following advantages:

By providing a deep trench isolation structure penetrating the first surface and the second surface of the semiconductor substrate between adjacent pixel cell regions, isolation between adjacent pixels is performed, thereby preventing the photocarriers in the pixel cell region from diffusing to The adjacent pixel unit area reduces the crosstalk caused by electrical signals to the adjacent pixel unit area, improves the display fade of the CMOS image sensor, and improves the imaging quality.

Further, the filler in the deep trench isolation structure is a dielectric, and the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate, and the light totally reflects at the interface between the deep trench isolation structure and the semiconductor substrate. The light is prevented from entering the adjacent pixel unit area through the deep trench isolation structure, the crosstalk to the optical signal of the adjacent pixel unit area is reduced, the display fading of the CMOS image sensor is further improved, and

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the imaging quality is improved; The dielectric material of the trench isolation structure is silicon oxide, which has a different color from the silicon of the semiconductor substrate. In the process of forming a filter and a microlens by a photolithography process, the deep trench isolation structure can be used as an alignment mark for lithography. No special alignment layer is required, saving process steps and reducing production costs.

Description of the drawings

FIG. 1 is a schematic structural diagram of a prior art CMOS image sensor.

FIG. 2 is a schematic structural diagram of a CMOS image sensor according to an embodiment of the present invention.

FIG. 3 is a schematic diagram illustrating the principle of total reflection formed at the interface between the deep trench isolation structure and the semiconductor substrate.

detailed description

Existing Backside illuminated CMOS image sensors have problems with display fading. The inventor's research found that the cause of fading is crosstalk of neighboring pixels. One of the reasons for the crosstalk is that the existing shallow trench isolation structure cannot effectively isolate the photocarrier diffusion between adjacent pixel units. Since the incident light of the CMOS image sensor using the backlight illuminates the pixel cell region of the semiconductor substrate through the microlens and the filter, in the prior art, in order to increase the effective photosensitive area of the photodiode in the pixel unit region, the depth of the photodiode is usually higher. Large, its depth can reach more than 10000 angstroms, while the depth of the existing shallow trench isolation structure is usually 2000-5000 angstroms. In the photoelectric conversion, the photo-generated carriers generated by photoelectric conversion of the photodiode may be diffused, and the existing shallow trench isolation structure cannot effectively isolate the photo-generated carriers so that the photo-generated carriers may go to adjacent pixels. Crosstalk of electrical signals is caused to adjacent pixels, causing the display of the CMOS image sensor to fade.

The back-illuminated CMOS image sensor provided by the present invention solves the crosstalk of electrical signals and improves the display fading problem of the CMOS image sensor. The back-illuminated CMOS image sensor includes:

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a semiconductor substrate, the semiconductor substrate having a first surface and a second surface opposite thereto;

The semiconductor substrate includes at least one pixel unit area;

The isolation structure is located between adjacent pixel unit regions;

Wherein, the isolation structure is a deep trench isolation structure, and the deep trench isolation structure penetrates the first surface and the second surface of the semiconductor substrate.

The technical solutions of the present invention will be described in detail below in conjunction with specific embodiments. Please refer to FIG. 2 . FIG. 2 is a schematic structural diagram of a CMOS image sensor according to an embodiment of the present invention.

The CMOS image sensor includes a semiconductor substrate 200 whose material may be silicon, SOI, gallium nitride, or gallium arsenide. The semiconductor substrate 200 has a first surface 201 and a second surface 202 opposite thereto. In the present embodiment, the semiconductor substrate 200 is a silicon substrate having a P-type conductivity type.

As shown in FIG. 2, the semiconductor substrate 200 includes at least one pixel unit area 203. For convenience of description, the two pixel unit area 203 will be described as an example. There is a deep trench isolation structure 206 between adjacent pixel cell regions 203 . The deep trench isolation structure 206 penetrates the first surface 201 and the second surface 202 of the semiconductor substrate 200 . The pixel unit region 203 of the semiconductor substrate 200 is formed with a filter 209 and micro lenses 210 . In this embodiment, the refractive index of the micro lens 210 is in the range of 1.2 to 4, and its material may be silicon nitride SiNX, zirconium oxide ZrO2, hafnium oxide HfO2, titanium oxide TiO2, aluminum oxide Al3O2, zinc oxide ZnO2, etc. The range of the refractive index of the filter 209 is 1.4 to 2. The material of the filter 209 may be a photoresist material. The filter 209 and the micro lens 210 are formed through a photolithography process. During the photolithography process for forming the filter, the deep trench isolation structure 206 can be used as an alignment mark for photolithography.

Still referring to FIG. 2, the pixel cell area 203 is used to form a pixel. The pixel cell region 203 includes a photodiode region 204 and a transistor region 205 . The photodiode region 204 is used to form a photodiode,

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which is used for photoelectric conversion and converts an optical signal incident from the second surface 202 into a corresponding electrical signal to generate photogenerated carriers. The transistor region 205 is used to form a transistor for amplifying and outputting the electrical signal converted by the photodiode. According to actual conditions, the transistor region 205 includes three or more transistors, and the transistors have a shallow trench isolation structure therebetween, and the transistors in the pixel are isolated from each other. The depth of the shallow trench isolation structure ranges from 2000 to 5000 Angstroms.

In this embodiment, the deep trench isolation structure 206 penetrates the first surface 201 and the second surface 202 of the semiconductor substrate 200 . As an embodiment, the thickness of the semiconductor substrate 200 ranges from 1.5 to 4 microns. The thickness of the deep trench isolation structure 206 should be the same as the depth of the semiconductor substrate 200, that is, 1.5 to 4 microns. As a preferred embodiment, the thickness of the semiconductor substrate 200 is 2 33 μ m so that the photodiodes in the pixel unit region 203 can better absorb incident light, and accordingly, the deep trench isolation structure 206 is The depth is preferably in the range of 2 to 3 microns. Since the deep trench isolation structure 206 penetrates the first surface 201 and the second surface 202 of the semiconductor substrate 200, the deep trench isolation structure 206 can effectively prevent the photo-generated light generated by the photodiode of the pixel during photoelectric conversion. The flow diffuses to adjacent pixels, reduces the crosstalk of electrical signals to adjacent pixels, improves the pixel fading of the CMOS image sensor, and improves the imaging quality of the CMOS image sensor.

The width of the deep trench isolation structure 206 is less than or equal to the width of the prior art shallow trench isolation structure to save chip area. As an embodiment, the width of the deep trench isolation structure 206 is 0.25 micrometers or less.

The filler in the deep trench isolation structure 206 is a dielectric whose refractive index is less than 0.8 times the refractive index of the semiconductor substrate. In this way, when the incident light enters the pixel unit area 203, total reflection is formed at the interface between the deep trench isolation structure 203 and the semiconductor substrate 200, so that incident light is prevented from entering the adjacent pixel unit area 203 through the deep trench isolation structure 206, and adjacent pixel units are The area 203 causes crosstalk of the optical signal, further improving the display fading problem of the CMOS image sensor. In order to facilitate the description of the principle that the light forms a total reflection at the interface between the deep trench isolation structure and the semiconductor substrate, a partial region 300 of the CMOS image sensor in FIG. 2 is enlarged and illustrated. The partial region 300 includes a pixel unit region 203, a corresponding filter 209, a microlens 210, and a deep trench isolation structure 206 on both sides of the pixel unit region 203. Please refer to FIG. 3 , which is a schematic diagram illustrating the principle of total reflection of light at the interface between the deep trench isolation structure and the semiconductor substrate.

As shown in FIG. 3, the light A enters the pixel unit area 203 from the air through the micro lens 210, the filter

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209, and the second surface 202 of the semiconductor substrate 200. Ideally, the light A is the photodiode of the pixel unit area 203. Absorption, however, may allow light to enter the interface of the deep trench isolation structure 206 and the semiconductor substrate 200 because the light A may have a certain tilt angle. Due to the difference in refractive index between the air, the micro lens 210, the filter 209, and the semiconductor substrate 200, the light rays A reach the interface between the deep trench isolation structure 206 and the semiconductor substrate 200 to refract light a plurality of times. Specifically, the normal line between the micro lens 210 and the air interface is O1, the angle between the light line A in the air and the normal line O1 is a1, and after the refraction, the angle between the light line A and the normal line O1 in the micro lens 210 is refracted. For a2, the light A is transmitted to the interface between the microlens 210 and the filter 209 in the micro lens 210. The normal of the interface between the micro lens 210 and the filter 209 is O2. The light A and the light in the micro lens 210 are The included angle of the normal line O2 is a3. After refraction, the angle between the light A in the filter 209 and the normal line O2 is aa4; the light A is transmitted to the filter 209 and the semiconductor liner in the filter 209. The interface of the bottom 200, the normal of the interface between the filter 209 and the semiconductor substrate 200 is O3, and the angle between the light A and the normal O3 in the filter 209 is a5, and after being refracted, The angle a6 between the light A and the normal O3 in the semiconductor substrate 200; within the semiconductor substrate 200, the light A is transmitted to the interface between the semiconductor substrate 200 and the deep trench isolation structure 206. The normal to the interface between the 200 and the deep trench isolation structure 206 is O4, and the angle between the light A and the normal O4 in the semiconductor substrate 200 is β. In this embodiment, the interface between the deep trench isolation structure 206 and the semiconductor substrate 200 is perpendicular to the interface between the filter 209 and the semiconductor substrate 200. Therefore, the normal line O4 is perpendicular to the normal line O3, and thus, the angle β and the angle a6. Mutual corner.

Since in practice, the thickness of the micro lens 210 and the thickness of the filter 209 are optimally set by those skilled in the art, it is possible to make the angle a6 the same as the angle a1. The maximum value of the angle a1 is called the chief ray angle (CRA), and the angle of the chief ray inclination angle ranges from 0 to 35°. Therefore, the angle α 6 of the angle of inclination is in the range of 0-35°, and the angle β of the angle β of the angle a6 is in the range of 55-90°, that is, the range of the incident angle of the light ray and the normal O4 is 55-90°. Therefore, assuming that the total reflection critical angle is α, if the light is to be totally reflected at the interface between the semiconductor substrate 200 and the deep trench isolation structure 206, α should be smaller than 55° to ensure the incident angle range between the light and the normal O4. At 55 to 90°, any incident angle is larger than α, and total reflection can be formed when the incident angle of the light and the normal O4 is 55 to 90°. Assuming that the total reflection critical angle is 55°, the refractive index of the semiconductor substrate 200 is x, and the refractive index of the dielectric filled in the deep trench isolation structure 206 is y, then according to the total reflection calculation formula: $\sin 55^\circ / \sin 90^\circ = y/x$

$y = \sin 55^\circ * x = 0.8 * x$

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According to the above analysis, when the total reflection critical angle is 55° , the refractive index of the dielectric filled in the corresponding deep trench isolation structure 206 is 0.8 times the refractive index of the semiconductor substrate 200 .

Since the critical angle α of the total reflection depends on the refractive index of the semiconductor substrate 200 and the refractive index of the filled dielectric in the deep trench isolation structure 206 . Specifically, in the case where the refractive index of the semiconductor substrate 200 is constant, the smaller the refractive index of the dielectric filled in the deep trench isolation structure 206 is, the smaller the critical angle α of the total reflection is. From the foregoing analysis, it can be seen that when the critical angle of total reflection is 55° , the refractive index of the dielectric in the corresponding deep trench isolation result 206 is 0.8 times the refractive index of the semiconductor substrate 200 . To make the total reflection critical angle less than 55° , the refractive index of the dielectric filled in the deep trench isolation structure 206 should be less than 0.8 times the refractive index of the semiconductor substrate 200 to ensure the light A in the deep trench isolation structure 206 and the semiconductor liner The total reflection occurs at the interface of the bottom 200. Therefore, the light A stays in the pixel unit area 203 , so as to prevent crosstalk caused by the light A through the deep trench isolation structure 206 to the adjacent pixel unit area, and further improve the display fading phenomenon of the existing CMOS image sensor.

As an embodiment, when the material of the semiconductor substrate 200 is silicon, the filler of the deep trench isolation structure 206 may be silicon oxide, and the silicon oxide may have a refractive index less than or equal to 0.8 of the refractive index of silicon. Times. In this embodiment, the refractive index of silicon is 3.46, and the refractive index of silicon oxide is 1.46, so that the incident light can form total reflection at the interface between the deep trench isolation structure 206 and the semiconductor substrate 200. Alternatively, under the condition that the refractive index of the dielectric filled in the deep trench isolation structure 206 is less than or equal to 0.8 times the refractive index of the silicon substrate, the dielectric filled in the deep trench isolation structure 206 may be other materials. When the material of the semiconductor substrate 200 is other semiconductor material, the material of the dielectric filled in the deep trench isolation structure 206 may also be other materials, but the dielectric filled in the deep trench isolation structure 206 should have a smaller refractive index than the semiconductor substrate. 200 is 0.8 times the refractive index to ensure that total reflection is formed at the interface between the deep trench isolation structure 206 and the semiconductor substrate 200 .

To sum up, the present invention provides a back-illuminated CMOS image sensor having a deep trench isolation structure between pixel cell regions of the back-illuminated CMOS image sensor. The deep trench isolation structure penetrates the semiconductor liner. The first surface of the bottom and the second surface opposite thereto effectively isolate the adjacent pixels, avoid crosstalk of electrical signals of adjacent pixels, improve the display fading problem of the CMOS image sensor, and improve the imaging quality. Further, the deep trench isolation structure is internally filled with a dielectric, the refractive index of the dielectric is less than 0.8 times the refractive index of the semiconductor substrate, and the light forms a total reflection at the interface

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between the deep trench isolation structure and the semiconductor substrate, avoiding Light enters adjacent pixels, causing crosstalk of optical signals to adjacent pixels, which further improves the display fading problem of CMOS image sensors and improves the imaging quality. At the same time, in the photolithography process for forming the filter and the microlens, the deep trench isolation structure can serve as a mark for photolithography alignment, reducing the number of process steps.

Although the utility model is disclosed as the preferred embodiment as above, it is not intended to limit the utility model. Any person skilled in the art can make possible changes and modifications without departing from the spirit and scope of the utility model. Therefore, the protection scope of the present invention should be based on the scope defined by the claims of the present invention.

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CLAIMS CN201725796

1.
A backside illuminated CMOS image sensor, comprising: a semiconductor substrate having a first surface and a second surface opposite thereto; the semiconductor substrate including at least one pixel cell region; an isolation structure at a phase The adjacent pixel unit region is characterized in that the isolation structure is a deep trench isolation structure, and the deep trench isolation structure penetrates the first surface and the second surface of the semiconductor substrate.

2.
The backlight-powered CMOS image sensor according to claim 1, wherein the width of the deep trench isolation structure is less than or equal to 0.25 micrometers.

3.
The backlit CMOS image sensor according to claim 1, wherein the deep trench isolation structure has a depth in the range of 1.5 to 4 microns.

4.
The backlit CMOS image sensor according to claim 1, wherein the filler in the deep trench isolation structure is a dielectric.

5.
The backlit CMOS image sensor according to claim 4, wherein the refractive index of the dielectric is less than 0.8

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times the refractive index of the semiconductor substrate.

6.

The backlight-source CMOS image sensor according to claim 1, wherein the semiconductor substrate is formed with a filter and a microlens in this order, and the filter and the microlens are located on the semiconductor substrate. Two surfaces.

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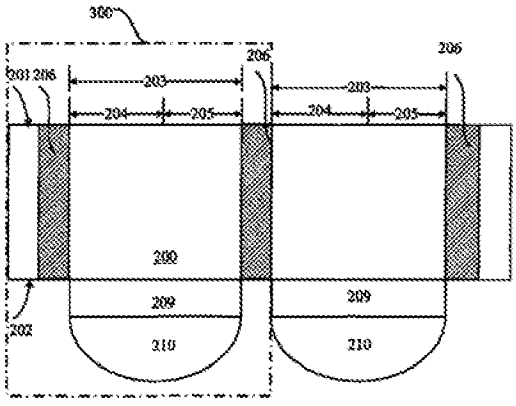
权利要求书 1 页 说明书 5 页 附图 2 页

(54)实用新型名称

背面照光的 CMOS 图像传感器

(57)摘要

本实用新型提供背面照光的 CMOS 图像传感器，包括：半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面；所述半导体衬底包括至少一个像素单元区域；隔离结构，位于相邻像素单元区域之间；其中，所述隔离结构为深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬底的第一表面和第二表面。本实用新型减少了相邻像素单元区域之间的电信号的串扰，改善了 CMOS 图像传感器的显示颜色，提高了成像质量。



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1. 一种背面照光的 CMOS 图像传感器，包括：

半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面；

所述半导体衬底包括至少一个像素单元区域；

隔离结构，位于相邻像素单元区域之间；

其特征在于，所述隔离结构为深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬底的第一表面和第二表面。

2. 如权利要求 1 所述的背面照光的 CMOS 图像传感器，其特征在于，所述深沟槽隔离结构的宽度小于等于 0.25 微米。

3. 如权利要求 1 所述的背面照光的 CMOS 图像传感器，其特征在于，所述深沟槽隔离结构的深度范围为 1.5 ～ 4 微米。

4. 如权利要求 1 所述的背面照光的 CMOS 图像传感器，其特征在于，所述深沟槽隔离结构内填充物为电介质。

5. 如权利要求 4 所述的背面照光的 CMOS 图像传感器，其特征在于，所述电介质的折射率小于所述半导体衬底的折射率的 0.8 倍。

6. 如权利要求 1 所述的背面照光的 CMOS 图像传感器，其特征在于，所述半导体衬底的依次形成有滤光片和微透镜，所述滤光片和微透镜位于所述半导体衬底的第二表面。

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背面照光的 CMOS 图像传感器

技术领域

[0001] 本实用新型涉及图像传感器，特别涉及背面照光的 CMOS 图像传感器。

背景技术

[0002] 图像传感器是组成数字摄像头的重要组成部分，根据元件不同分为电荷耦合 (CCD, Charge Coupled Device) 图像传感器和金属氧化物半导体 (CMOS, Complementary Metal-Oxide Semiconductor) 图像传感器。其中，由于 CMOS 图像传感器集成度高，容易与标准的 CMOS 制作工艺兼容，并且功耗低，随着 CMOS 制作工艺的改进，CMOS 图像传感器成为目前图像传感器的主流技术。

[0003] 在申请号为 200710148796.5 的中国专利申请中公开了一种现有的 CMOS 图像传感器。现有的 CMOS 图像传感器包括半导体衬底，所述半导体衬底通常包括若干呈矩阵排布的像素单元区域，相邻的像素单元区域之间具有浅沟槽隔离结构 (STI)。请参考图 1，图 1 是现有的 CMOS 图像传感器结构示意图，所述 CMOS 图像传感器包括：半导体衬底 100，所述半导体衬底 100 包括若干像素单元区域 103，图中以 2 个像素单元区域 103 为例进行说明；相邻像素单元区域 103 之间具有浅沟槽隔离结构 106。其中所述像素单元区域 103 用于形成像素，通常所述像素单元区域 103 包括光电二极管区域 104 和晶体管区域 105，所述光电二极管区域 104 用于形成光电二极管，所述光电二极管用于光电转换；所述晶体管区域 105 用于形成晶体管，所述晶体管用于将光电二极管转换的电信号放大后输出。所述浅沟槽隔离结构 106 用于相邻像素的隔离。所述半导体衬底 100 包括第一表面 101 和与之相对的第二表面 102。光线从第二表面 102 进入像素单元区域 103 内。本领域技术人员将所述 CMOS 图像传感器称为背面照光的 (Backside illuminated)CMOS 图像传感器。

[0004] 在实际中发现，上述背面照光的 CMOS 图像传感器具有显示褪色的问题，影响了成像质量。

[0005] 因此，需要一种背面照光的 CMOS 图像传感器，能够改善显示褪色的问题，提高 CMOS 图像传感器的成像质量。

实用新型内容

[0006] 本实用新型解决的问题是提供了一种背面照光的 CMOS 图像传感器，能够改善显示褪色的问题，提高 CMOS 图像传感器的成像质量。

[0007] 为解决上述问题，本实用新型提供一种背面照光的 CMOS 图像传感器，包括：

[0008] 半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面；

[0009] 所述半导体衬底包括至少一个像素单元区域；

[0010] 隔离结构，位于相邻像素单元区域之间；

[0011] 其中，所述隔离结构为深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬底的第一表面和第二表面。

[0012] 可选的，所述深沟槽隔离结构的宽度小于等于 0.25 微米。

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[0013] 可选的，所述深沟槽隔离结构的深度范围为 1.5 ～ 4 微米。

[0014] 可选的，所述深沟槽隔离结构内填充物为电介质。

[0015] 可选的，所述电介质的折射率小于所述半导体衬底的折射率的 0.8 倍。

[0016] 可选的，所述半导体衬底的依次形成有滤光片和微透镜，所述滤光片和微透镜位于所述半导体衬底的第二表面。

[0017] 与现有技术相比，本实用新型具有以下优点：

[0018] 通过在相邻像素单元区域之间设置贯穿半导体衬底的第一表面和第二表面的深沟槽隔离结构，进行相邻像素间的隔离，避免了像素单元区域内的光生载流子扩散至相邻像素单元区域，减少对相邻像素单元区域造成电信号的串扰，改善了 CMOS 图像传感器的显示褪色，提高了成像质量。

[0019] 进一步地，所述深沟槽隔离结构内的填充物为电介质，所述电介质的折射率小于半导体衬底折射率的 0.8 倍，光线在深沟槽隔离结构和半导体衬底的界面形成全反射，避免光线经深沟槽隔离结构进入相邻的像素单元区域，减小了对相邻像素单元区域的光信号的串扰，进一步改善了 CMOS 图像传感器的显示褪色，提高了成像质量；所述深沟槽隔离结构填充电介质为氧化硅，与半导体衬底的硅具有不同的颜色，在进行光刻工艺形成滤光片和微透镜的过程中，深沟槽隔离结构可以作为光刻的对准标记，无需专门的对准层，节省了工艺步骤，降低了生产成本。

附图说明

[0020] 图 1 是现有技术 CMOS 图像传感器结构示意图。

[0021] 图 2 是本实用新型的一个实施例的 CMOS 图像传感器结构示意图。

[0022] 图 3 是光线在深沟槽隔离结构与半导体衬底界面形成全反射原理示意图。

具体实施方式

[0023] 现有的背面照光的 (Backside illuminated)CMOS 图像传感器存在显示褪色的问题。经发明人研究发现，褪色的原因是相邻像素的串扰 (crosstalk)。所述串扰的原因之一是现有的浅沟槽隔离结构无法有效隔离相邻的像素单元之间光生载流子扩散。由于采用背面照光的 CMOS 图像传感器的入射光线经过微透镜和滤光片进入半导体衬底的像素单元区域，现有技术为了提高像素单元区域内的光电二极管的有效感光面积，通常光电二极管的深度较大，其深度可达 10000 埃以上，而现有的浅沟槽隔离结构的深度范围通常为 2000 ～ 5000 埃。在进行光电转换时，所述光电二极管光电转换所产生的光生载流子可能扩散，而现有的浅沟槽隔离结构无法有效隔离光生载流子，从而光生载流子可能至相邻像素，对相邻像素造成电信号的串扰，从而导致 CMOS 图像传感器的显示褪色。

[0024] 本实用新型提供的背面照光的 CMOS 图像传感器解决了电信号的串扰，改善了 CMOS 图像传感器的显示褪色问题，所述背面照光的 CMOS 图像传感器包括：

[0025] 半导体衬底，所述半导体衬底具有第一表面和与之相对的第二表面；

[0026] 所述半导体衬底包括至少一个像素单元区域；

[0027] 隔离结构，位于相邻像素单元区域之间；

[0028] 其中，所述隔离结构为深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬

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底的第一表面和第二表面。

[0029] 下面将结合具体的实施例对本实用新型的技术方案进行详细的说明。请参考图2，图 2 是本实用新型一个实施例的 CMOS 图像传感器结构示意图。

[0030] 所述CMOS图像传感器包括半导体衬底200，所述半导体衬底200的材料可以是硅、SOI、氮化镓或者砷化镓。所述半导体衬底 200 具有第一表面 201 和与之相对的第二表面 202。本实施例中，所述半导体衬底 200 为具有 P 型导电类型的硅衬底。

[0031] 如图 2，所述半导体衬底 200 包括至少一个像素单元区域 203，为了便于说明，以 2 个像素单元区域 203 为例进行说明。相邻的像素单元区域 203 之间具有深沟槽隔离结构 206。所述深沟槽隔离结构 206 贯穿所述半导体衬底 200 的第一表面 201 和第二表面 202。半导体衬底 200 的像素单元区域 203 形成有滤光片 209 和微透镜 210。本实施例中，所述微透镜 210 的折射率范围为 1.2 ～ 4，其材质可以为氮化硅 SiN_x、氧化锆 ZrO_2、氧化铪 HfO_2、氧化钛 TiO_2、氧化铝 Al_2O_3、氧化锌 ZnO_2 等，所述滤光片 209 的折射率范围为 1.4 ～ 2，其材质可以为光阻材料。所述滤光片 209 和微透镜 210 通过光刻工艺形成，在形成滤光片的光刻工艺过程中，深沟槽隔离结构 206 可以作为光刻的对准标记使用。

[0032] 仍参考图 2，所述像素单元区域 203 用于形成像素。所述像素单元区域 203 包括光电二极管区域 204 和晶体管区域 205。所述光电二极管区域 204 用于形成光电二极管，所述光电二极管用于进行光电转换，将从第二表面 202 入射的光信号转换为相应的电信号，产生光生载流子。所述晶体管区域 205 用于形成晶体管，所述晶体管用于将所述光电二极管转换的电信号放大、输出。根据实际情况，所述晶体管区域 205 内包括 3 个或 3 个以上晶体管，所述晶体管之间具有浅沟槽隔离结构，用于像素内的晶体管之间相互隔离。所述浅沟槽隔离结构的深度范围为 2000 ～ 5000 埃。

[0033] 本实施例中，所述深沟槽隔离结构 206 贯穿所述半导体衬底 200 的第一表面 201 和第二表面 202。作为一个实施例，所述半导体衬底 200 的厚度范围为 1.5 ～ 4 微米，所述深沟槽隔离结构 206 的厚度应与所述半导体衬底 200 的深度相同，即为 1.5 ～ 4 微米。作为优选的实施例，所述半导体衬底 200 的厚度为 2 ～ 3 微米，以使得像素单元区域 203 内的光电二极管能更好的吸收入射光线，相应地，所述深沟槽隔离结构 206 的深度范围优选为 2 ～ 3 微米。由于所述深沟槽隔离结构 206 贯穿所述半导体衬底 200 的第一表面 201 和第二表面 202，因此，深沟槽隔离结构 206 可以有效阻止像素的光电二极管在光电转换时产生的光生载流子扩散至相邻像素，减少对相邻像素的电信号的串扰，改善 CMOS 图像传感器的像素褪色，提高了 CMOS 图像传感器的成像质量。

[0034] 所述深沟槽隔离结构 206 的宽度小于或等于现有技术的浅沟槽隔离结构的宽度，以节约芯片面积。作为一个实施例，所述深沟槽隔离结构 206 的宽度范围为小于等于 0.25 微米。

[0035] 所述深沟槽隔离结构 206 内填充物为电介质，所述电介质的折射率小所述半导体衬底的折射率的 0.8 倍。这样入射光线进入像素单元区域 203 时在深沟槽隔离结构 203 与半导体衬底 200 的界面形成全反射，避免入射光线经过深沟槽隔离结构 206 进入相邻像素单元区域 203，对相邻像素单元区域 203 造成光信号的串扰，进一步改善 CMOS 图像传感器的显示褪色的问题。为了便于说明光线在深沟槽隔离结构和半导体衬底的界面形成全反射的原理，对图 2 中 CMOS 图像传感器的部分区域 300 进行放大说明。所述部分区域 300 包括像

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素单元区域 203、与之对应的滤光片 209、微透镜 210、以及像素单元区域 203 两侧的深沟槽隔离结构 206。请参考图 3，图 3 是光线在深沟槽隔离结构与半导体衬底界面形成全反射原理示意图。

[0036] 如图 3 所示，光线 A 自空气经过微透镜 210、滤光片 209、半导体衬底 200 的第二表面 202 进入像素单元区域 203，理想的状况是，光线 A 被像素单元区域 203 的光电二极管吸收，但是，由于光线 A 可能具有一定倾斜角因此光线可能会入射深沟槽隔离结构 206 与半导体衬底 200 的界面。由于通常空气、微透镜 210、滤光片 209、半导体衬底 200 的材质不同而折射率不同，光线 A 到达深沟槽隔离结构 206 与半导体衬底 200 的界面发生多次光的折射。具体地，在微透镜 210 和空气界面的法线为 01，在空气中光线 A 与所述法线 01 的夹角为 a1，经过折射，在微透镜 210 内光线 A 与法线 01 的夹角为 a2；光线 A 在微透镜 210 内传输至微透镜 210 和滤光片 209 的界面，所述微透镜 210 和滤光片 209 的界面的法线为 02，在微透镜 210 内光线 A 与所述法线 02 的夹角为 a3，经过折射，在滤光片 209 内光线 A 与所述法线 02 的夹角为 aa4；光线 A 在滤光片 209 内传输至滤光片 209 与半导体衬底 200 的界面，所述滤光片 209 与半导体衬底 200 的界面的法线为 03，在滤光片 209 内所述光线 A 与所述法线 03 的夹角为 a5，经过折射，在半导体衬底 200 内光线 A 与法线 03 的夹角 a6；在半导体衬底 200 内，所述光线 A 传输至半导体衬底 200 与所述深沟槽隔离结构 206 的界面，所述半导体衬底 200 与所述深沟槽隔离结构 206 的界面的法线为 04，在半导体衬底 200 内光线 A 与法线 04 的夹角为 β。本实施例中，深沟槽隔离结构 206 与半导体衬底 200 的界面垂直于滤光片 209 与半导体衬底 200 的界面，因此，法线 04 与法线 03 垂直，从而，角度 β 与角度 a6 互为余角。

[0037] 由于在实际中，本领域技术人员对微透镜 210 的厚度、滤光片 209 的厚度进行优化设置，可以使得使得角度 a6 与角度 a1 相同。角度 a1 的最大值称为主光线倾斜角 (chief ray angle，CRA)，而主光线倾斜角的角度范围为 0 ～ 35°。因此，角度 a6 倾斜角度范围为 0 ～ 35°，角度 a6 的余角 β 的角度范围为 55 ～ 90°，即光线与法线 04 的入射角范围为 55 ～ 90°。因此，假设全反射临界角为 α，若要光线在半导体衬底 200 与深沟槽隔离结构 206 的界面形成全反射，α 应小于为 55°，以保证在光线与法线 04 的入射角范围为 55 ～ 90° 时，任一入射角均大于 α，从而光线与法线 04 的入射角为 55 ～ 90° 时可以形成全反射。假设全反射临界角为 55°，半导体衬底 200 的折射率为 x，深沟槽隔离结构 206 内填充的电介质的折射率为 y，则根据全反射计算公式：sin55° /sin90° = y/x

[0038] y = sin55° *x = 0.8*x

[0039] 由上述分析可知，当全反射临界角为 55° 时，对应的深沟槽隔离结构 206 内填充的电介质的折射率为半导体衬底 200 的折射率的 0.8 倍。

[0040] 由于全反射的临界角 α 取决于半导体衬底 200 的折射率和深沟槽隔离结构 206 内填充电介质的折射率关系。具体地，在半导体衬底 200 的折射率一定的情况下，深沟槽隔离结构 206 内填充的电介质的折射率越小，全反射的临界角 α 越小。由前面的分析可知，在全反射的临界角为 55° 时对应的深沟槽隔离结果 206 内的电介质的折射率为半导体衬底 200 折射率的 0.8 倍。若要使得全反射临界角小于 55°，深沟槽隔离结构 206 内填充的电介质的折射率应小于半导体衬底 200 折射率的 0.8 倍，以保证光线 A 在深沟槽隔离结构 206 和半导体衬底 200 的界面发生全反射。从而，光线 A 留在像素单元区域 203 内，避免光

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线 A 经过深沟槽隔离结构 206 对相邻像素单元区域造成串扰，进一步改善现有的 CMOS 图像传感器的显示褪色现象。

[0041] 作为一个实施例，所述半导体衬底 200 的材质为硅时，所述深沟槽隔离结构 206 的填充物可以为氧化硅，并且所述氧化硅的折射率可以小于等于硅的折射率的 0.8 倍。本实施例中，硅的折射率为 3.46，氧化硅的折射率为 1.46，这样入射光线在深沟槽隔离结构 206 和半导体衬底 200 的界面可以形成全反射。可替代地，在深沟槽隔离结构 206 内填充的电介质的折射率小于等于硅衬底的折射率的 0.8 倍前提下，深沟槽隔离结构 206 内填充的电介质可以为其他材质。当半导体衬底 200 的材质为其他半导体材料时，深沟槽隔离结构 206 内填充的电介质的材质还可以为其他材质，但是深沟槽隔离结构 206 内填充的电介质的折射率应小于半导体衬底 200 折射率的 0.8 倍，以保证在深沟槽隔离结构 206 和半导体衬底 200 的界面形成全反射。

[0042] 综上，本实用新型提供了一种背面照光的 CMOS 图像传感器，所述背面照光的 CMOS 图像传感器的像素单元区域之间具有深沟槽隔离结构，所述深沟槽隔离结构贯穿所述半导体衬底的第一表面和与之相对的第二表面，从而有效隔离相邻像素，避免了相邻像素电信号的串扰，改善了 CMOS 图像传感器的显示褪色问题，提高了成像质量。进一步地，所述深沟槽隔离结构内部填充电介质，所述电介质的折射率小于半导体衬底的折射率的 0.8 倍，光线在深沟槽隔离结构和半导体衬底的界面上形成全反射，避免光线进入相邻像素，对相邻像素造成光信号的串扰，更加改善了 CMOS 图像传感器的显示褪色问题，提高了成像质量。同时，在形成滤光片和微透镜的光刻工艺时，所述深沟槽隔离结构可以作为光刻对准的标记，减少了工艺步骤。

[0043] 本实用新型虽然以较佳实施例公开如上，但其并不是用来限定本实用新型，任何本领域技术人员在不脱离本实用新型的精神和范围内，都可以做出可能的变动和修改，因此本实用新型的保护范围应当以本实用新型权利要求所界定的范围为准。

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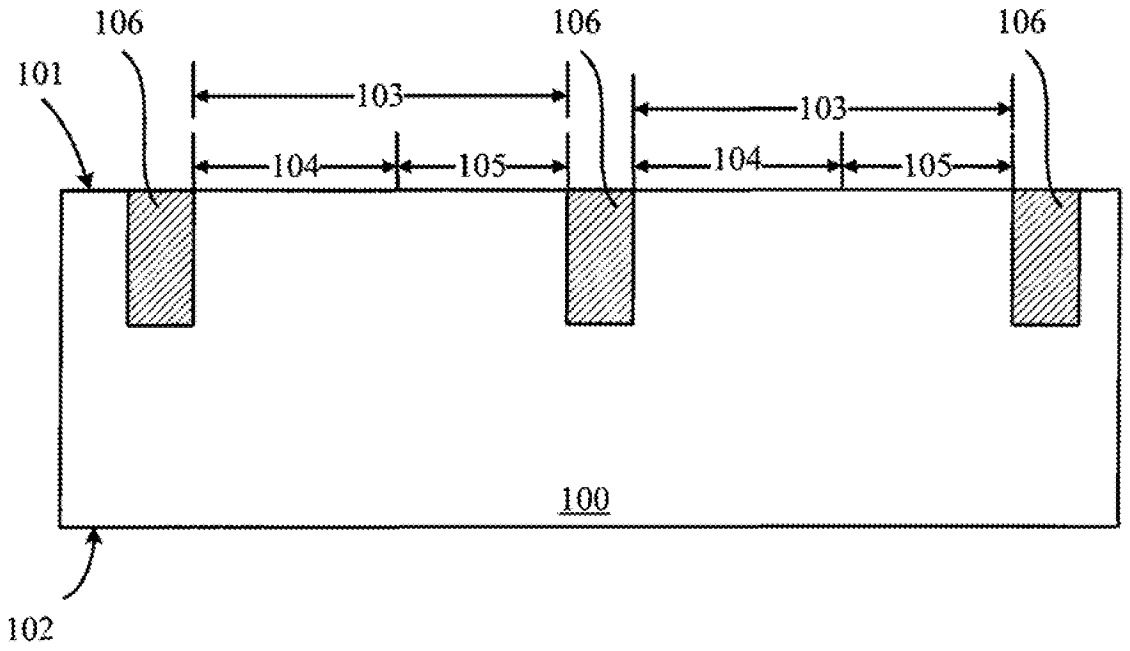


图 1

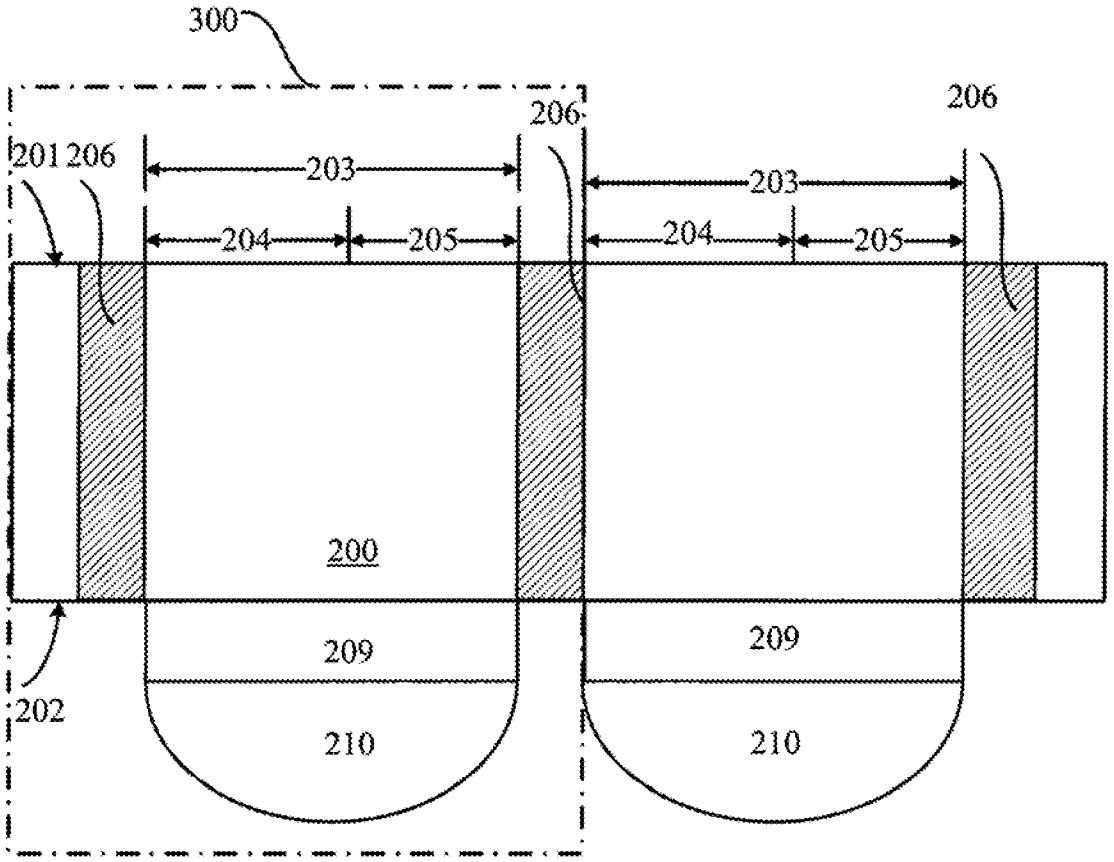


图 2

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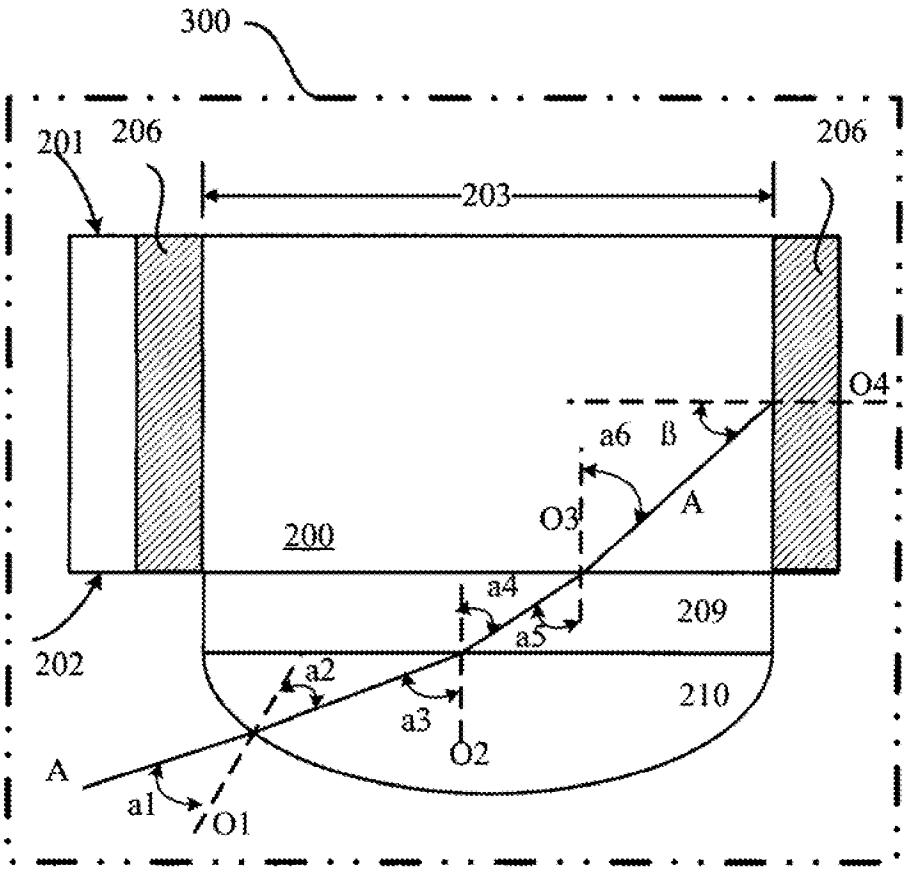


图 3

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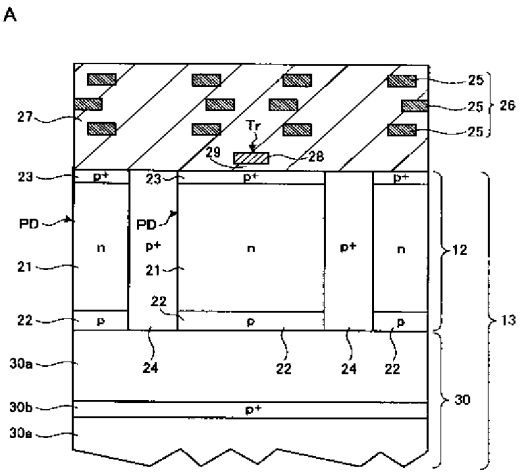
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(54)【発明の名称】固体撮像装置とその製造方法、及び電子機器

(57)【要約】
【課題】集光特性の向上が図られ、フレアやスミア等の光学的雑音が抑制された裏面照射型の固体撮像装置、及びその製造方法を提供する。また、その固体撮像装置を用いた電子機器を提供する。
【解決手段】基板１３に形成された複数の画素２を有する固体撮像装置１において、各画素２は、基板１３に埋め込まれた遮光部１７によって分離されている。この遮光部１７は、隣接する受光部ＰＤ間に形成され、基板１３の裏面側から所望の深さに形成されたトレンチ部１９、及びトレンチ部１９内に埋め込まれた遮光膜２０で構成されている。これにより、斜めに入射した光が受光部ＰＤに入射するのを防ぐことができる。
【選択図】図３



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【特許請求の範囲】
【請求項１】
複数の受光部が形成された基板であって、前記基板の裏面側が光照射面とされる基板と、
前記基板の表面側に形成された配線層と、
隣接する受光部間に形成され、前記基板の裏面側から所望の深さに形成されたトレンチ部、及び前記トレンチ部内に埋め込まれた遮光膜で構成された遮光部と、
を有する固体撮像装置。
【請求項２】
前記隣接する受光部間には、所定の不純物領域から構成され、隣接する受光部間を電気的に分離する為の素子分離領域が形成されており、
前記遮光部は、前記素子分離領域内に形成されている
請求項１記載の固体撮像装置。
【請求項３】
前記遮光部は、前記基板を貫通して形成されている
請求項２記載の固体撮像装置。
【請求項４】
前記トレンチ部とトレンチ部に埋め込まれた遮光膜との間には、高誘電率材料膜が形成されている
請求項３記載の固体撮像装置。
【請求項５】
前記遮光膜は、アルミニウム又はタングステンで構成されている
請求項４記載の固体撮像装置。
【請求項６】
前記高誘電率材料膜は、酸化ハフニウム、五酸化タンタル、又は二酸化ジルコニウムで構成されている
請求項４記載の固体撮像装置。
【請求項７】
基板の表面領域に複数の受光部及び所望の不純物領域を形成し、裏面領域にエッチングストッパー層を形成する工程、
前記基板の表面側に、層間絶縁膜を介して形成された複数層の配線からなる配線層を形成する工程、
前記基板を前記基板の裏面側から前記エッチングストッパー層までエッチングする工程、
前記基板を貫通して、前記基板の裏面側から所望の深さに達するトレンチ部を形成する工程、
前記基板に形成されたトレンチ部に埋め込み膜を形成し、前記埋め込み膜をストッパーとして、前記基板を薄肉化する工程、
前記埋め込み膜を除去して後、前記トレンチ部に、遮光膜を埋め込む工程、
有する固体撮像装置の製造方法。
【請求項８】
前記基板の裏面領域は、ノンドープのシリコン層により構成され、前記エッチングストッパー層は、ｐ型の高濃度不純物層によって構成されている
請求項７記載の固体撮像装置の製造方法。
【請求項９】
前記トレンチ部は前記基板を貫通するように形成する
請求項８記載の固体撮像装置の製造方法。
【請求項１０】
前記トレンチ部とトレンチ部に埋め込まれた遮光膜との間には、高誘電率材料膜が形成されている

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請求項９記載の固体撮像装置の製造方法。
【請求項１１】
前記遮光膜は、アルミニウム又はタングステンで構成されている
請求項９記載の固体撮像装置の製造方法。
【請求項１２】
前記高誘電率材料膜は、酸化ハフニウム、五酸化タンタル、又は二酸化ジルコニウムで構成されている
請求項９記載の固体撮像装置の製造方法。
【請求項１３】
光学レンズと、
複数の受光部が形成された基板であって、前記基板の裏面側が光照射面とされる基板と、前記基板の表面側に形成された配線層と、隣接する受光部間に形成され、前記基板の裏面側から所望の深さに形成されたトレンチ部、及び前記トレンチ部内に埋め込まれた遮光膜で構成された遮光部と、から構成され、前記光学レンズに集光された光が入射される固体撮像装置と
前記固体撮像装置から出力される出力信号を処理する信号処理回路と、
を含む電子機器。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明は、裏面照射型の固体撮像装置とその製造方法、及び電子機器に関する。
【背景技術】
【０００２】
固体撮像装置は、ＣＣＤ（Charge Coupled Device）型固体撮像装置と、ＣＭＯＳ（Complementary Metal Oxide Semiconductor）型固体撮像装置とに大別される。
これらの固体撮像装置では、画素毎にフォトダイオードからなる受光部が形成されており、受光部では、受光部に入射した光による光電変換により信号電荷が生成される。ＣＣＤ型の固体撮像装置では、受光部において生成された信号電荷はＣＣＤ構造を有する電荷転送部内を転送され、出力部において画素信号に変換されて出力される。一方、ＣＭＯＳ型の固体撮像装置では、受光部において生成された信号電荷は画素毎に増幅され、増幅された信号が画素信号として信号線により出力される。
【０００３】
このような固体撮像装置では、斜めの入射光や受光部上部において乱反射した入射光により半導体基板内で偽信号が生成され、スミアやフレア等の光学的雑音が発生するという問題がある。
【０００４】
下記特許文献１には、ＣＣＤ型の固体撮像装置において、電荷転送部上部に形成される遮光膜を受光部と読み出しゲート部との界面に形成された溝部に埋め込まれるように形成することで、スミアの発生を抑制する構成が記載されている。特許文献１においては、ＬＯＣＯＳ酸化膜を用いて形成した溝部に遮光膜を形成する構成とされているため、遮光膜を基板深くに形成することは困難であり、スミアの原因とされる斜め光の入射を完全に阻止することはできない。また、遮光膜を埋め込む深さに比例し、画素面積が縮小するので、遮光膜を深く埋め込むことは本質的に困難である。
【０００５】
ところで、近年、基板上の配線層が形成される側とは反対側から光を照射する、裏面照射型の固体撮像装置が提案されている（下記特許文献２参照）。裏面照射型の固体撮像装置では、光照射側に配線層や回路素子等が構成されないため、基板に形成された受光部の開口率を高くできる他、入射光が配線層等に反射されることなく受光部に入射されるので、感度の向上が図られる。
【０００６】

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このような裏面照射型の固体撮像装置においても、斜め光による光学的雑音が懸念されるため、光照射側となる基板の裏面側の受光部間に遮光膜を形成することが好ましい。この場合、光照射側となる基板の裏面側に遮光膜を有する層を１層形成することが考えられるが、遮光膜の高さに比例して基板とオンチップレンズ面との間の距離が長くなるため、集光特性の悪化が起こりうる。集光特性が悪化した場合には、他の画素のカラーフィルタを透過した斜めの光が、その画素とは異なる画素の受光部に入射し、混色や感度低下という問題も発生する。

【先行技術文献】

【特許文献】

【０００７】

【特許文献１】特開２００４－１４０１５２号公報

【特許文献２】特開２００４－７１９３１号公報

【発明の概要】

【発明が解決しようとする課題】

【０００８】

上述の点に鑑み、本発明は、集光特性の向上が図られ、フレアやスミア等の光学的雑音が抑制された裏面照射型の固体撮像装置、及びその製造方法を提供する。また、その固体撮像装置を用いた電子機器を提供する。

【課題を解決するための手段】

【０００９】

上記課題を解決し、本発明の目的を達成するため、本発明の固体撮像装置は、基板と、配線層と、遮光部とを有する構成とされている。基板には、複数の受光部が形成されており、基板の裏面側が光照射面とされている。また、配線層は、基板の表面側に形成されている。また、遮光部は、隣接する受光部間に形成され、基板の裏面側から所望の深さに形成されたトレンチ部、及びトレンチ部内に埋め込まれた遮光膜で構成されている。

【００１０】

本発明の固体撮像装置では、基板に形成された複数の受光部間が、基板の裏面側から所望の深さに形成されたトレンチ部を遮光膜によって埋め込むことによって形成された遮光部により分離されている。このため、光照射面とされる基板の裏面側から斜めの光が入射した場合、遮光部によって、斜めの入射光が遮られる。これにより、基板に形成された受光部への斜めの光の入射が抑制される。

【００１１】

また、本発明の固体撮像装置の製造方法は、まず、裏面領域にエッチングストッパー層を形成した基板の表面領域に複数の受光部及び所望の不純物領域を形成し、次に、基板の表面側に層間絶縁膜を介して形成された複数層の配線からなる配線層を形成する。次に、基板の裏面側から基板を薄肉化する。薄肉化は、基板のエッチングストッパー層までエッチングする。次に、基板を貫通して、基板の裏面側から所望の深さに達するトレンチ部を形成する。次に、基板に形成されたトレンチ部に埋め込み膜を形成し、埋め込み膜をストッパーとして、基板を薄肉化する。次に、埋め込み膜を除去して後、トレンチ部に、遮光膜を埋め込む。

【００１２】

本発明の固体撮像装置の製造方法では、光学レンズと、上述した固体撮像装置と、信号処理回路とを有して構成されている。

【発明の効果】

【００１３】

本発明によれば、フレア特性やスミア特性が向上され、また、混色やブルーミングを抑制された固体撮像装置を得ることができる。また、その固体撮像装置を用いることにより、画質の向上が図られた電子機器が得られる。

【図面の簡単な説明】

【００１４】

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【図１】本発明の第１の実施形態に係るＣＭＯＳ型の固体撮像装置の全体を示す概略構成図である。
【図２】第１の実施形態に係る固体撮像装置の画素部における断面構成図である。
【図３】Ａ　第１の実施形態に係る固体撮像装置の製造工程図である。
【図４】Ｂ　第１の実施形態に係る固体撮像装置の製造工程図である。
【図５】Ｃ　第１の実施形態に係る固体撮像装置の製造工程図である。
【図６】Ｄ　第１の実施形態に係る固体撮像装置の製造工程図である。
【図７】Ｅ　第１の実施形態に係る固体撮像装置の製造工程図である。
【図８】Ｆ　第１の実施形態に係る固体撮像装置の製造工程図である。
【図９】Ｇ　第１の実施形態に係る固体撮像装置の製造工程図である。
【図１０】Ｈ　第１の実施形態に係る固体撮像装置の製造工程図である。
【図１１】Ｉ，Ｊ　第１の実施形態に係る固体撮像装置の製造工程図である。
【図１２】Ｋ，Ｌ　第１の実施形態に係る固体撮像装置の製造工程図である。
【図１３】本発明の第２の実施形態に係る固体撮像装置の画素部における断面構成図である。
【図１４】本発明の第３の実施形態に係る電子機器の概略構成図である。
【発明を実施するための形態】
【００１５】
以下に、本発明の実施形態に係る固体撮像装置とその製造方法、及び電子機器の一例を、図１～図１４を参照しながら説明する。本発明の実施形態は以下の順で説明する。なお、本発明は以下の例に限定されるものではない。
１．第１の実施形態：固体撮像装置
　１．１　固体撮像装置全体の構成
　１．２　要部の構成
　１．３　固体撮像装置の製造方法
２．第２の実施形態：固体撮像装置
３．第３の実施形態：電子機器
【００１６】
〈１．第１の実施形態：固体撮像装置〉
［１－１　固体撮像装置全体の構成］
図１は、本発明の第１の実施形態に係るＣＭＯＳ型の固体撮像装置の全体を示す概略構成図である。
本実施形態例の固体撮像装置１は、シリコンからなる基板１１上に配列された複数の画素２から構成される画素部３と、垂直駆動回路４と、カラム信号処理回路５と、水平駆動回路６と、出力回路７と、制御回路８等を有して構成される。
【００１７】
画素２は、フォトダイオードからなる受光部と、複数の画素トランジスタとから構成され、基板１１上に、２次元アレイ状に規則的に複数配列される。画素２を構成する画素トランジスタは、転送トランジスタ、リセットトランジスタ、選択トランジスタ、アンプトランジスタで構成される４つのＭＯＳトランジスタであってもよく、また、選択トランジスタを除いた３つのトランジスタであってもよい。
【００１８】
画素部３は、２次元アレイ状に規則的に複数配列された画素２から構成される。画素部３は、実際に光を受光し光電変換によって生成された信号電荷を増幅してカラム信号処理回路５に読み出す有効画素領域と、黒レベルの基準になる光学的黒を出力するための黒基準画素領域（図示せず）とから構成されている。黒基準画素領域は、通常は、有効画素領域の外周部に形成されるものである。
【００１９】
制御回路８は、垂直同期信号、水平同期信号及びマスタクロックに基づいて、垂直駆動回路４、カラム信号処理回路５、及び水平駆動回路６等の動作の基準となるクロック信号

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や制御信号などを生成する。そして、制御回路８で生成されたクロック信号や制御信号などは、垂直駆動回路４、カラム信号処理回路５及び水平駆動回路６等に入力される。

【００２０】

垂直駆動回路４は、例えばシフトレジスタによって構成され、画素部３の各画素２を行単位で順次垂直方向に選択走査する。そして、各画素２のフォトダイオードにおいて受光量に応じて生成した信号電荷に基づく画素信号を、垂直信号線を通してカラム信号処理回路５に供給する。

【００２１】

カラム信号処理回路５は、例えば、画素２の列毎に配置されており、１行分の画素２から出力される信号を画素列毎に黒基準画素領域（図示しないが、有効画素領域の周囲に形成される）からの信号によって、ノイズ除去や信号増幅等の信号処理を行う。カラム信号処理回路５の出力段には、水平選択スイッチ（図示せず）が水平信号線１０とのあいだに設けられている。

【００２２】

水平駆動回路６は、例えばシフトレジスタによって構成され、水平走査パルスを順次出力することによって、カラム信号処理回路５の各々を順番に選択し、カラム信号処理回路５の各々から画素信号を水平信号線１０に出力させる。

【００２３】

出力回路７は、カラム信号処理回路５の各々から水平信号線１０を通して、順次に供給される信号に対し信号処理を行い出力する。

【００２４】

［１－２　要部の構成］

図２に、本実施形態例の固体撮像装置１の画素部３における断面構成図を示す。本実施形態例の固体撮像装置１は、裏面照射型のＣＭＯＳ型固体撮像装置を例としたものである。

【００２５】

図２に示すように、本実施形態例の固体撮像装置１は、基板１３と、基板１３の表面側に形成された配線層２６、及び支持基板１４と、基板１３の裏面側に形成されたカラーフィルタ層１５、及びオンチップレンズ１６とから構成されている。

【００２６】

基板１３は、シリコンからなる半導体基板で構成され、例えば第１導電型（本実施形態例ではｎ型とする）の半導体基板により構成されている。基板１３は、３μｍ～５μｍの厚みを有し、基板１３の画素形成領域１２には受光部ＰＤと、画素回路部を構成する複数の画素トランジスタＴｒとから構成される画素２が、複数個、二次元マトリクス状に形成されている。また、図２では図示を省略するが、基板１３に形成された画素２の周辺領域には、周辺回路部が構成されている。

【００２７】

受光部ＰＤは、画素形成領域１２に形成される暗電流抑制領域２２，２３と、その暗電流抑制領域２２，２３の間の領域に形成される電荷蓄積領域２１により構成されている。暗電流抑制領域２３は基板１３（画素形成領域１２）の表面側に形成され、第２導電型（本実施形態例ではｐ型）の高濃度不純物領域により構成されている。また、暗電流抑制領域２２は基板１３（画素形成領域１２）の裏面側に形成され、ｐ型の不純物領域により構成されている。電荷蓄積領域２１は、ｎ型の不純物領域により構成されている。この受光部ＰＤでは、主に暗電流抑制領域２２，２３を構成するｐ型の不純物領域と、電荷蓄積領域２１を構成するｎ型の不純物領域との間に形成されるｐｎ接合によりフォトダイオードが構成されている。

受光部ＰＤでは、入射した光の光量に応じた信号電荷が生成され、蓄積される。また、基板の界面で発生する暗電流の原因となる電子は暗電流抑制領域２２，２３の多数キャリアである正孔に吸収されることにより、暗電流が抑制される。

【００２８】

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画素トランジスタＴｒは、基板１３の表面側に形成された図示しないソース・ドレイン領域と、基板１３の表面上にゲート絶縁膜２９を介して形成されたゲート電極２８とから構成されている。画素トランジスタＴｒは、前述したように、転送トランジスタ、リセットトランジスタ、増幅トランジスタを含む３つの画素トランジスタＴｒを有する構成でもよく、また、選択トランジスタを含む４つの画素トランジスタＴｒを有する構成であってもよい。ソース・ドレイン領域は、図示を省略するが、基板１３表面側に形成されたｎ型の高濃度不純物領域により形成され、本実施形態例の画素トランジスタＴｒはｎチャネルＭＯＳトランジスタとして機能する。

【００２９】

また、隣接する画素２と画素２との間には、基板１３の表面から裏面に架けてｐ型の高濃度不純物領域からなる素子分離領域２４が形成されており、この素子分離領域２４により各画素２は電気的に分離されている。さらに、素子分離領域２４には、基板１３の裏面側から所望の深さに形成された遮光部１７が形成されている。遮光部１７は、平面でみると、各画素２を囲むように例えば格子状に形成されるものである。この遮光部１７は、基板１３の裏面側に形成された所望の深さのトレンチ部１９と、トレンチ部１９の側壁及び底面に形成された高誘電率材料膜１８と、高誘電率材料膜１８を介してトレンチ部１９に埋め込まれた遮光膜２０とから構成されている。このとき、トレンチ部１９に埋め込まれた遮光膜２０の最表面は、基板１３の裏面と面一に構成されている。高誘電率材料膜１８の材料としては、例えば、酸化ハフニウム（HfO_2）、五酸化タンタル（Ta_2O_5）、二酸化ジルコニウム（ZrO_2）を用いることができる。また、遮光膜２０の材料としては、例えば、タングステン（Ｗ）、アルミニウム（Ａｌ）を用いることができる。

【００３０】

配線層２６は、基板１３の表面側に形成されており、層間絶縁膜２７を介して複数層（本実施形態例では３層）に積層された配線２５を有して構成されている。配線層２６に形成される配線２５を介して、画素２を構成する画素トランジスタＴｒが駆動される。

【００３１】

支持基板１４は、配線層２６の基板１３に面する側とは反対側の面に形成されている。この支持基板１４は、製造段階で基板１３の強度を確保するために構成されているものであり、例えばシリコン基板により構成されている。

【００３２】

カラーフィルタ層１５は、基板１３の裏面側に形成されており、画素毎に例えば、Ｒ（赤色）、Ｇ（緑色）、Ｂ（青色）のカラーフィルタ層が形成されている。カラーフィルタ層１５では、所望の波長の光が透過され、透過した光が基板１３内の受光部ＰＤに入射する。

【００３３】

オンチップレンズ１６は、カラーフィルタ層１５の基板１３に面する側とは反対側の面に形成されている。オンチップレンズ１６では照射された光が集光され、集光された光はカラーフィルタ層１５を介して各受光部ＰＤに効率良く入射する。

【００３４】

以上の構成を有する固体撮像装置１では、基板１３の裏面側から光が照射され、オンチップレンズ１６及びカラーフィルタ層１５を透過した光が受光部ＰＤにて光電変換することにより、信号電荷が生成される。そして受光部ＰＤにて生成された信号電荷は、基板１３の表面側に形成された画素トランジスタＴｒを介して、配線層２６の所望の配線２５で形成された垂直信号線により画素信号として出力される。

【００３５】

本実施形態例の固体撮像装置１では、素子分離領域２４により、隣接する画素２と画素２との間では素子分離領域２４のポテンシャルによって形成された障壁により電子の移動がなされない。すなわち、基板１３内に形成される不純物領域の濃度勾配により画素間の電気的分離がなされる。

さらに、素子分離領域２４に埋め込まれて形成された遮光部１７により、光入射面側に

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おいて斜めに入射してくる光が隣接する画素２に入射することを防ぐ。すなわち、遮光部１７によって画素間の光学的分離がなされる。

【００３６】

また、素子分離領域２４にトレンチ部１９を形成する場合、トレンチ部１９の側壁及び底面に物理的ダメージやイオン照射による不純物活性化によりトレンチ部１９の周辺部でピニングはずれが発生する可能性がある。この問題点に対し、本実施形態例では、トレンチ部１９の側壁及び底面に固定電荷を多く持つ高誘電率材料膜１８を形成することによりピニング外れが防止される。

【００３７】

本実施形態例の固体撮像装置１によれば、隣接する画素間には、素子分離領域２４に埋め込まれた遮光部１７が構成されているので、受光面に入射してくる斜め光が受光部ＰＤに入射するのを防ぐことができる。これにより、オンチップレンズで集光しきれずに隣接する画素２に向って入射する光が遮光され、隣接する画素間で起こる光学的な混色が低減される。また、受光面とオンチップレンズ１６との間で発生する回折光や反射光のうち、隣接する画素２に向って入射する角度の大きい光が遮光されるので、フレアの発生が低減される。

【００３８】

さらに、本実施形態例の固体撮像装置１によれば、遮光部１７は、素子分離領域２４に埋め込まれた構成とされているので、基板１３裏面の受光面が平坦になり、基板１３の裏面側に形成されるカラーフィルタ層１５及びオンチップレンズ１６が受光面に近づく。これにより、光が入射するオンチップレンズ１６の表面と、基板１３の受光面との距離が近づくため集光特性が向上し、混色の低減が図られる。

【００３９】

［１－３　製造方法］

図３～図１２に、本実施形態例の固体撮像装置１の製造工程図を示し、本実施形態例の固体撮像装置１の製造方法を説明する。

【００４０】

まず、図３Ａに示すように、基板１３に受光部ＰＤ、画素トランジスタＴｒから構成される複数の画素２を形成し、基板１３の表面側に、層間絶縁膜２７を介して形成された複数層の配線２５からなる配線層２６を形成する。これらの画素２及び配線層２６は、通常の固体撮像装置１と同様の方法で形成することができる。

【００４１】

本実施形態例では、例えば、３μｍ～５μｍの厚さのｎ型の表面領域となる画素形成領域１２を有し、画素形成領域１２の下に裏面領域３０を有する基板１３準備する。そして、この基板１３の表面側から所望の不純物を所望の濃度でイオン注入することにより、画素形成領域１２に、受光部ＰＤ、素子分離領域２４、及び図示しないソース・ドレイン領域を形成する。そして、基板１３の表面には、例えばシリコン酸化膜からなるゲート絶縁膜２９を形成したのち、ゲート絶縁膜２９上部の所望の領域に、例えばポリシリコンからなるゲート電極２８を形成する。ゲート電極２８の形成工程は、画素形成領域１２内の受光部ＰＤやソース・ドレイン領域等の形成工程の前に行ってもよく、その場合は、受光部ＰＤやソース・ドレイン領域を、ゲート電極２８をマスクとしてセルフアラインで形成することができる。その他、ゲート電極２８の側面に、例えばシリコン酸化膜やシリコン窒化膜等で構成されるサイドウォールを形成してもよい。

また、配線層２６は、ゲート電極２８形成後、例えばシリコン酸化膜からなる層間絶縁膜２７の形成と、アルミニウムや銅等で構成される配線２５の形成を所望の回数繰り返して行うことにより形成することができる。このとき、図示しないが各配線間を接続するコンタクト部の形成も行われる。

裏面領域３０は、画素形成領域１２側から順に、ノンドープのシリコン層３０ａ、ｐ型の高濃度不純物層からなるエッチングストッパー層３０ｂ、ノンドープのシリコン層３０ａが積層された構造とされている。このエッチングストッパー層３０ｂは、ノンドープの

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シリコン層３０ａの所望の領域にボロンを高濃度にイオン注入することによって形成することができる。その他、ノンドープのシリコン層３０ａをエピタキシャル成長法によって形成し、その形成過程で、所望の領域にｐ型の高濃度不純物層を形成する方法を用いてもよい。本実施形態例の裏面領域３０は、基板１３に接する側のシリコン層３０ａが、約２μｍ～５μｍ、エッチングストッパー層３０ｂが約１μｍ、エッチングストッパー層３０ｂ上に形成されるシリコン層３０ａが、約１μｍとなるように構成されている。

【００４２】

次に、図４Ｂに示すように、配線層２６上部に、有機系接着剤またはプラズマ照射による物理的接着により支持基板１４を張り合わせる。

【００４３】

そして、図５Ｃに示すように、支持基板１４を張り合わせた後素子を反転し、物理的研磨法により裏面領域３０の上面を研磨する。このとき、エッチングストッパー層３０ｂに到達しない程度に研磨を行う。

【００４４】

次に、弗硝酸を用いてウェットエッチングすることにより、裏面領域３０のシリコン層３０ａをエッチングする。そうすると、図６Ｄに示すようにノンドープのシリコン層３０ａとｐ型高濃度不純物層からなるエッチングストッパー層３０ｂのドーピング種の違いにより、エッチングがエッチングストッパー層３０ｂでストップする。すなわち、裏面領域３０の上面側に形成されたシリコン層３０ａのみがエッチング除去される。

【００４５】

次に、図７Ｅに示すように、裏面領域３０の上部にフォトレジスト層３１を形成し、素子分離領域２４の遮光部１７を形成する領域に開口部３１ａが形成されるように露光、現像する。この場合、前工程において、裏面領域３０はエッチングストッパー層３０ｂまでエッチング除去されているため表面が平坦とされている。このため、フォトレジスト層３１も表面が平坦となるように形成されるためフォトレジスト層３１の露光、現像が精度良く行われ、所望の開口部３１ａをより正確にパターン形成することができる。

【００４６】

次に、所望の形状にパターニングされたフォトレジスト層３１をマスクとしてドライエッチングをすることにより、図８Ｆに示すように、裏面領域３０を貫通して画素形成領域１２の裏面側から所望の深さに達するトレンチ部１９を形成する。トレンチ部１９の深さは、前述したように、基板１３の裏面側から入射する斜め光を受光面側で遮光できる程度の深さに形成されればよく、本実施形態例では、基板１３の裏面から例えば５００ｎｍ～１０００ｎｍの深さまでトレンチ部１９を形成する。

【００４７】

次に、図９Ｃに示すように、トレンチ部１９を埋め込むようにシリコン酸化膜（SiO_2）又はシリコン窒化膜（ＳｉＮ）からなる埋め込み膜３２を、例えばＣＶＤ法を用いて成膜する。

【００４８】

次に、図１０Ｈに示すように、ウェットエッチングにより所定の時間エッチングすることにより、埋め込み膜３２をエッチバックする。このとき、埋め込み膜３２の表面が、基板１３裏面から５０～６０ｎｍ程度突出した状態でエッチバックを終了する。

【００４９】

次に、埋め込み膜３２をストッパーとして用い、ＣＭＰ法により裏面領域３０を研磨し、裏面領域３０を薄肉化する。これにより図１１Ｉに示すように、裏面領域３０が除去される。

【００５０】

次に、図１１Ｊに示すように、トレンチ部１９に埋め込まれた埋め込み膜３２をウェットエッチングにより除去すると共に、前工程のＣＭＰ法による研磨工程、及びトレンチ部１９形成工程において発生したダメージ層を除去する。埋め込み膜３２を除去する薬液は、埋め込み膜３２がSiO_2の場合沸酸を用い、ＳｉＮの場合は燐酸を用いると良い。ダ

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メージ層除去は、例えばアンモニア水のようなアルカリ性薬液を用いるのが好ましい。

【００５１】

次に、図１２Ｋに示すように、トレンチ部１９の側壁及び底面を含む基板１３裏面に、ＣＶＤ法又はスパッタ法を用いて、高誘電率材料膜１８を成膜する。続いて、高誘電率材料膜１８が成膜されたトレンチ部１９を含む全面に、ＣＶＤ法を用いて遮光膜２０を成膜し、トレンチ部１９内部に遮光膜２０を埋め込む。

【００５２】

次に、図１２Ｌに示すように、例えば塩酸、硫酸等の酸系薬液によりウェットエッチングすることにより、遮光膜２０の高さを調整する。このとき、遮光膜２０表面と基板１３の裏面が面一となるように遮光膜２０の高さを調整する。

【００５３】

その後、基板１３の裏面側に、通常の方法を用いてカラーフィルタ層１５、及びオンチップレンズ１６を形成して図２に示す本実施形態例の固体撮像装置１が完成する。

【００５４】

以上のように、本実施形態例の固体撮像装置１はバルク基板によって形成することができる。通常の裏面照射型の固体撮像装置ではＳＯＩ（Silicon On Insulator）基板が用いられていたが、本実施形態例ではＳＯＩ基板よりもコストの低いバルク基板によって形成することができるため、高価なＳＯＩ基板を用いる必要がなくコストの低減が図られる。

【００５５】

また、本実施形態例の固体撮像装置１では、ノンドープのシリコン層３０ａに、ｐ型の高濃度不純物層からなるエッチングストッパー層３０ｂが形成された裏面領域３０有する基板１３を用いる例とした。しかしながら、これに限定されることなく、その他、種々のエッチングストッパー層を有する基板を用いることができる。例えばエッチングストッパー層３０ｂとしてＳｉＣやＳｉＧｅ層を用いても良い。

【００５６】

また、本実施形態例の固体撮像装置１の製造方法では、トレンチ部１９に図９Ｈの工程でストッパーとして用いられる埋め込み膜３２を形成することができ、図１０Ｉの工程の裏面領域３０の薄膜化が容易になる。そして、裏面領域３０の薄膜化が容易になるため、裏面領域３０に形成されるｐ型高濃度不純物層を、基板１３に形成された受光部ＰＤからある程度離れた距離に形成することができる。このため、エッチングストッパー層３０ｂであるｐ型高濃度不純物層の拡散工程における熱による画素形成領域１２の受光部ＰＤのキャリアプロファイルの変調を抑制することができる。

【００５７】

また、本実施形態例の固体撮像装置１の製造方法では、基板１３に形成される素子分離領域２４は、基板１３の表面側からｐ型の不純物をイオン注入することによって形成される。このため、表面側から深い位置の画素形成領域１２（この場合、基板１３の裏面側）では、急峻なポテンシャルプロファイルが形成されにくい。そうすると、基板１３の裏面側では、生成された信号電荷が素子分離領域２４を通過して、隣接する画素２に漏れ込む可能性があり、混色やブルーミングの原因となる。本実施形態例では、基板１３の裏面側の素子分離領域２４には、遮光部１７が埋め込まれて形成されている。このため、素子分離領域２４の特に素子分離機能が弱い領域において、隣接する画素に漏れ込む信号電荷を物理的に遮ることができ、基板１３内の信号電荷の移動による混色やブルーミングが抑制される。

【００５８】

〈２．第２の実施形態：固体撮像装置〉

次に、本発明の第２の実施形態に係る固体撮像装置について説明する。本実施形態例の固体撮像装置は、第１の実施形態の固体撮像装置と同様に裏面照射型の固体撮像装置であり、全体の構成は、図１と同様であるから、重複説明を省略する。

【００５９】

図１３は、本実施形態例における固体撮像装置４０の要部の概略断面構成図である。図

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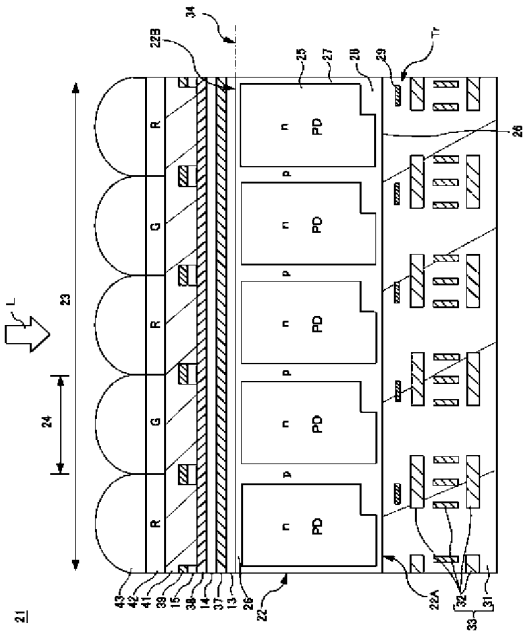
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最終頁に続く

(54)【発明の名称】固体撮像素子及びその製造方法、並びに固体撮像装置及び撮像装置

(57)【要約】
【課題】界面ダメージを回避し、信頼性や密着性を劣化させることなく暗電流の発生を抑制する。
【解決手段】受光部を有する半導体基板２２と、半導体基板表面に形成された酸化膜１３と、同酸化膜の上層にＴｉの密着層１５を介して形成された遮光膜１９とを備える。更に、酸化膜１３と密着層１５との間に、同酸化膜よりも酸化エンタルピーが小さな材料であるTa_2O_5からなる金属酸化膜１４が配置されている。
【選択図】図２



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【特許請求の範囲】
【請求項１】
入射光を光電変換する受光部を有する半導体基板と、
該半導体基板の表面に形成された酸化物層と、
該酸化物層よりも上層に密着層を介して形成された遮光層と、
前記酸化物層と前記密着層との間に配置され、前記酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成された酸素供給層とを備える
固体撮像素子。
【請求項２】
前記酸素供給層は、光透過性材料から構成されると共に、前記半導体基板の受光部が形成された領域に対応する領域の略全面に形成された
請求項１に記載の固体撮像素子。
【請求項３】
前記酸素供給層は、前記遮光層が形成された領域に対応する領域にのみ形成された
請求項１に記載の固体撮像素子。
【請求項４】
前記密着層および遮光層を構成する材料の酸化エンタルピーは、前記酸化物層を構成する材料の酸化エンタルピーよりも大きい
請求項１、請求項２または請求項３に記載の固体撮像素子。
【請求項５】
前記密着層および遮光層は、アルミニウム、チタン、アルミニウム合金若しくは窒化チタンのうち少なくとも１つの材料を含んで構成されている
請求項１、請求項２、請求項３または請求項４に記載の固体撮像素子。
【請求項６】
前記酸素供給層は、酸化タンタル（Ta_2O_5）、酸化ニオブ（Nb_2O_5）、酸化バナジウム（V_2O_3）、酸化クロム（Cr_2O_3）、酸化タングステン（WO_2）若しくは酸化モリブデン（MoO_2）を用いて構成されている
請求項１、請求項２、請求項３、請求項４または請求項５に記載の固体撮像素子。
【請求項７】
前記固体撮像素子は、
入射光を電気信号に変換する受光部を有する複数の画素部と、該画素部が形成された半導体基板の一面側に配線層を備え、該配線層が形成されている面とは反対側より入射される光を前記受光部で受光する裏面照射型固体撮像素子である
請求項１、請求項２、請求項３、請求項４、請求項５または請求項６に記載の固体撮像素子。
【請求項８】
入射光を光電変換する受光部を有する半導体基板と、
該半導体基板の表面に形成された酸化物層と、
該酸化物層よりも上層に密着層を介して形成された配線層と、
前記酸化物層と前記密着層との間に配置され、前記酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成された酸素供給層とを備える
固体撮像素子。
【請求項９】
前記酸素供給層は、光透過性材料から構成されると共に、前記半導体基板の受光部が形成された領域に対応する領域の略全面に形成された
請求項８に記載の固体撮像素子。
【請求項１０】
前記酸素供給層は、前記配線層が形成された領域に対応する領域にのみ形成された
請求項８に記載の固体撮像素子。
【請求項１１】

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前記密着層および遮光層を構成する材料の酸化エンタルピーは、前記酸化物層を構成する材料の酸化エンタルピーよりも大きい
請求項８、請求項９または請求項１０に記載の固体撮像素子。
【請求項１２】
前記密着層および遮光層は、アルミニウム、チタン、アルミニウム合金若しくは窒化チタンのうち少なくとも１つの材料を含んで構成されている
請求項８、請求項９、請求項１０または請求項１１に記載の固体撮像素子。
【請求項１３】
前記酸素供給層は、酸化タンタル（Ta_2O_5）、酸化ニオブ（Nb_2O_5）、酸化バナジウム（V_2O_3）、酸化クロム（Cr_2O_3）、酸化タングステン（WO_2）若しくは酸化モリブデン（MoO_2）を用いて構成されている
請求項８、請求項９、請求項１０、請求項１１または請求項１２に記載の固体撮像素子。
【請求項１４】
入射光を光電変換する受光部を有すると共に、その表面に酸化物層が形成された半導体基板の上層に、前記酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成される酸素供給層を形成する工程と、
該酸素供給層よりも上層に密着層を介して遮光層を形成する工程とを備える
固体撮像素子の製造方法。
【請求項１５】
入射光を光電変換する受光部を有すると共に、その表面に酸化物層が形成された半導体基板の上層に、前記酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成される酸素供給層を形成する工程と、
該酸素供給層よりも上層に密着層を介して配線層を形成する工程とを備える
固体撮像素子の製造方法。
【請求項１６】
入射光を光電変換する受光部を含む半導体基板と、該半導体基板の表面に形成された酸化物層と、該酸化物層よりも上層に密着層を介して形成された遮光層と、前記酸化物層と前記密着層との間に配置され、前記酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成された酸素供給層を有する固体撮像素子と、
前記受光部に入射光を集光する光学系とを備える
固体撮像装置。
【請求項１７】
入射光を光電変換する受光部を含む半導体基板と、該半導体基板の表面に形成された酸化物層と、該酸化物層よりも上層に密着層を介して形成された配線層と、前記酸化物層と前記密着層との間に配置され、前記酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成された酸素供給層を有する固体撮像素子と、
前記受光部に入射光を集光する光学系とを備える
固体撮像装置。
【請求項１８】
入射光を光電変換する受光部を含む半導体基板と、該半導体基板の表面に形成された酸化物層と、該酸化物層よりも上層に密着層を介して形成された遮光層と、前記酸化物層と前記密着層との間に配置され、前記酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成された酸素供給層を有する固体撮像素子と、
前記受光部に入射光を集光する光学系と、
前記受光部で光電変換された信号電荷を処理する信号処理部とを備える
撮像装置。
【請求項１９】
入射光を光電変換する受光部を含む半導体基板と、該半導体基板の表面に形成された酸化物層と、該酸化物層よりも上層に密着層を介して形成された配線層と、前記酸化物層と

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前記密着層との間に配置され、前記酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成された酸素供給層を有する固体撮像素子と、
前記受光部に入射光を集光する光学系と、
前記受光部で光電変換された信号電荷を処理する信号処理部とを備える
撮像装置。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明は固体撮像素子及びその製造方法、並びに固体撮像装置及び撮像装置に関する。詳しくは、暗電流の発生を抑制することが可能な固体撮像素子及びその製造方法、並びにこうした固体撮像素子を用いた固体撮像装置及び撮像装置に係るものである。
【背景技術】
【０００２】
従来、ビデオカメラやデジタルスチルカメラなどにおいて、ＣＣＤ（Ｃｈａｒｇｅ Ｃｏｕｐｌｅｄ Ｄｅｖｉｃｅ）やＣＭＯＳイメージセンサで構成された固体撮像装置が広く使用されている。なお、ＣＭＯＳ型固体撮像装置には、図２０に示す表面照射型と、図２１に示す裏面照射型が知られている。
【０００３】
表面照射型固体撮像装置１１１は、図２０の模式的構成図で示す様に、半導体基板１１２に光電変換部となるフォトダイオードＰＤと複数の画素トランジスタからなる単位画素１１６が複数形成された画素領域１１３を有して構成されている。画素トランジスタは、図示しないが、図２０ではゲート電極１１４を示して、模式的に画素トランジスタの存在を示している。
【０００４】
各フォトダイオードＰＤは不純物拡散層による素子分離領域１１５で分離されており、半導体基板１１２の画素トランジスタが形成された表面側に層間絶縁膜１１７を介して複数の配線１１８を配置した多層配線層１１９が形成されている。配線１１８は、フォトダイオードＰＤの位置に対応する部分を除いて形成されている。
【０００５】
多層配線層１１９上には、平坦化膜１２０を介して順次オンチップカラーフィルタ１２１及びオンチップマイクロレンズ１２２が形成されている。オンチップカラーフィルタ１２１は、例えば赤（Ｒ）、緑（Ｇ）、青（Ｂ）の各色フィルタを配列して構成されている。
【０００６】
表面照射型の固体撮像装置１１１では、多層配線層１１９が形成された基板表面を受光面１２３として、光Ｌがこの基板表面側から入射することとなる。
【０００７】
一方、裏面照射型固体撮像装置１３１は、図２１の模式的構成図に示す様に、半導体基板１１２に光電変換部となるフォトダイオードＰＤと複数の画素トランジスタからなる単位画素１１６が複数形成された画素領域１１３を有して構成されている。画素トランジスタは、図示しないが、基板表面側に形成され、図２１ではゲート電極１１４を示して、模式的に画素トランジスタの存在を示している。
【０００８】
各フォトダイオードＰＤは不純物拡散層による素子分離領域１１５で分離されており、半導体基板１１２の画素トランジスタが形成された表面側に層間絶縁膜１１７を介して複数の配線１１８を形成した多層配線層１１９が形成されている。裏面照射型では、配線１１８はフォトダイオードＰＤの位置に関係なく形成することができる。
【０００９】
また、半導体基板１１２のフォトダイオードＰＤが臨む裏面上に、順次絶縁層１２８、オンチップカラーフィルタ１２１及びオンチップマイクロレンズ１２２が形成されている

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【００１０】

裏面照射型の固体撮像装置１３１では、多層配線層及び画素トランジスタが形成された基板表面とは反対側の基板裏面を受光面１３２として、光Ｌがこの基板裏面側から入射することとなる。なお、光Ｌは多層配線層１１９の制約を受けることなく、フォトダイオードＰＤに入射されることとなるので、フォトダイオードＰＤの開口を広く取ることができ、高感度化が実現することとなる。

【００１１】

ところで、上記した様な固体撮像装置は感度の向上と並んでノイズ低減を図ることが極めて重要な課題である。特に、入射光が無い状態で、光電変換を行う受光部が設けられた半導体基板と上層膜との界面における界面準位が発生源となる暗電流は、固体撮像装置として低減されるべきノイズである。

【００１２】

ここで、暗電流とは受光部に光が入射していない状態でもフォトダイオードＰＤおよびその周辺から電子の生成が起こる現象であり、暗電流が多く発生すると、固体撮像素子の撮像性能の基準となる黒レベルが悪化して充分な階調の分解能を得ることができず、撮像時の感度が低下してしまう。

【００１３】

また、界面準位とは、半導体基板内部の結晶欠陥や不純物、酸化膜界面との結合欠陥に起因した電子の存在し得るエネルギー状態であり、界面準位が増えると暗電流の発生が助長されることとなる。

【００１４】

なお、界面準位の一因として、光電変換を行う受光部が設けられた半導体基板の表面と、これを被覆する酸化膜との界面から酸素原子（Ｏ）が奪われることで生じる界面層のダメージが挙げられる。

【００１５】

以下、この点について図面を用いて説明を行う。

図２２は裏面照射型固体撮像装置の構造を示した模式図であり、受光部（図示せず）が設けられた半導体基板（Ｓｉ基板）２０１と、半導体基板表面に形成された酸化膜（ＳｉＯ）２０２を有する。また、酸化膜２０２の上層には反射防止膜（ＳｉＯＮ）２０３が設けられ、その上層には絶縁膜（SiO_2）２０４が設けられ、絶縁膜２０４の更に上層には密着層（Ｔｉ）２０５を介して遮光膜（Ｗ）２０６が設けられている。

【００１６】

ここで、遮光膜（Ｗ）２０６と絶縁膜（SiO_2）２０４との密着性の向上を図るために密着層（Ｔｉ）２０５を形成しているのであるが、Ｔｉは酸素（Ｏ）との結合力が強い。そして、こうしたＴｉによる還元作用によって酸化膜２０２と半導体基板２０１の界面から酸素原子（Ｏ）が奪われることとなり、上述の通り、酸化膜２０２と反動体基板２０１間の界面においてダメージが生じることとなり、結果として暗電流の発生を助長してしまうこととなる。

【００１７】

ところで、暗電流を低減するための技術の１つとして、界面準位の原因となる結合欠陥を水素雰囲気で熱処理することで（Ｓｉｎｔｅｒｉｎｇ）、欠陥に伴うＳｉの未結合手を水素終端させる方法がある。

【００１８】

しかし、遮光膜で覆われている領域については水素シンター処理の効果が得られにくいこともあって、こうした技術だけでは界面準位の発生を充分に低減することができていなかった。

【００１９】

そのため、例えば特許文献１では、各画素の光電変換素子の上部に水素を供給するための水素供給膜を配すると共に、水素供給膜と遮光部材との間に水素の拡散を抑制するため

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の拡散防止膜を形成する技術が提案されている。

【００２０】

また、例えば特許文献２では、反射防止膜がチタンを含まない材料によって形成されると共に、配線用及びコンタクトプラグ用のバリア層及び密着層がチタンを含まない材料によって形成される技術が提案されている。

【００２１】

なお、特許文献１に記載の技術によって、光電変換素子の表面やゲート絶縁膜等への水素供給が充分に行われることとなり、界面準位をターミネートすることができるために、暗電流を低減することが可能となる。

【００２２】

また、特許文献２に記載の技術によって、チタンの影響による暗電流ノイズの増加を除去することが可能となる。

【先行技術文献】

【特許文献】

【００２３】

【特許文献１】特開２０１０－１６１２８号公報
【特許文献２】特開２００３－２２９５５６号公報

【発明の概要】

【発明が解決しようとする課題】

【００２４】

しかしながら、水素供給膜を成膜した場合には、上記した半導体基板と酸化膜の界面における酸素欠陥に起因する界面ダメージを回避することは困難である。

【００２５】

また、密着層やバリアメタルにチタンを用いずに配線層や遮光層を形成した場合には、配線の信頼性や密着性が劣化するといった影響が懸念される。

【００２６】

本発明は以上の点に鑑みて創案されたものであって、界面ダメージを回避すると共に、信頼性や密着性を劣化させることなく暗電流を抑制することができる固体撮像素子及びその製造方法、並びに固体撮像装置及び撮像装置を提供することを目的とする。

【課題を解決するための手段】

【００２７】

上記の目的を達成するために、本発明に係る固体撮像素子は、入射光を光電変換する受光部を有する半導体基板と、該半導体基板の表面に形成された酸化物層と、該酸化物層よりも上層に密着層を介して形成された遮光層と、前記酸化物層と前記密着層との間に配置され、前記酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成された酸素供給層とを備える。

【００２８】

ここで、酸化物層と密着層との間に配置され、酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成された酸素供給層によって、酸化物層と半導体基板の界面層（界面酸化物）が保護されてダメージを受けることが無くなり、界面準位の形成による暗電流の発生を抑制することができる。

【００２９】

即ち、チタンやアルミニウム等の酸素との結合力が強い材料が存在したとしても、こうした材料は半導体基板界面の酸化物層から酸素原子を奪うよりも、酸素供給層から酸素を奪う方が化学反応上、エネルギー的に安定しているために、上述の様に酸化物層と半導体基板の界面層（界面酸化物）は保護され、暗電流の発生を抑制することができるのである。

【００３０】

また、半導体基板の受光部が形成された領域に対応する領域の略全面に酸素供給層が形成された場合には、より一層充分に酸化物層と半導体基板の界面層（界面酸化物）を保護

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することができ、暗電流発生の抑制について高い効果を期待することができる。なお、有効画素領域の上層に酸素供給層を形成する場合には、受光部に入射光を到達させる必要があることから、酸素供給層は光透過性に優れた材料から構成される必要がある。

【００３１】

更に、遮光層が形成された領域に対応する領域にのみ酸素供給層が形成された場合には、有効画素領域の上層構造は通常の固体撮像素子（酸素供給層が形成されていない固体撮像素子）と同じ構造となる。そのため、酸素供給層を構成する材料の透過率や屈折率はどの様なものであっても良く、材料選択や成膜条件の自由度が高く、インテグレーション上の制約が少ないため、よりプロセスウィンドウの広い条件で安定した製造プロセスを構築することが可能である。

【００３２】

なお、酸素供給層の一例としては、酸化タンタル（Ta_2O_5）、酸化ニオブ（Nb_2O_5）、酸化バナジウム（V_2O_3）、酸化クロム（Cr_2O_3）、酸化タングステン（WO_2）若しくは酸化モリブデン（MoO_2）を用いて構成する場合が挙げられる。

【００３３】

また、本発明の固体撮像素子は、入射光を光電変換する受光部を有する半導体基板と、該半導体基板の表面に形成された酸化物層と、該酸化物層よりも上層に密着層を介して形成された配線層と、前記酸化物層と前記密着層との間に配置され、前記酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成された酸素供給層とを備える。

【００３４】

ここで、酸化物層と密着層との間に配置され、酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成された酸素供給層によって、半導体基板と酸化物層の界面層（界面酸化物）が保護されてダメージを受けることが無くなり、界面準位の形成による暗電流の発生を抑制することができる。

【００３５】

即ち、チタンやアルミニウム等の酸素との結合力が強い材料が存在したとしても、こうした材料は半導体基板界面の酸化物層から酸素原子を奪うよりも、酸素供給層から酸素を奪う方が化学反応上、エネルギー的に安定しているために、上述の様に酸化物層と半導体基板の界面層（界面酸化物）は保護され、暗電流の発生を抑制することができるのである。

【００３６】

また、半導体基板の受光部が形成された領域に対応する領域の略全面に酸素供給層が形成された場合には、より一層充分に酸化物層（界面酸化物）を保護することができ、暗電流発生の抑制について高い効果を期待することができる。なお、有効画素領域の上層に酸素供給層を形成する場合には、受光部に入射光を到達させる必要があることから、酸素供給層は光透過性に優れた材料から構成される必要がある。

【００３７】

更に、配線層が形成された領域に対応する領域にのみ酸素供給層が形成された場合には、有効画素領域の上層構造は通常の固体撮像素子（酸素供給層が形成されていない固体撮像素子）と同じ構造となる。そのため、酸素供給層を構成する材料の透過率や屈折率はどの様なものであっても良く、材料選択や成膜条件の自由度が高く、インテグレーション上の制約が少ないため、よりプロセスウィンドウの広い条件で安定した製造プロセスを構築することが可能である。

【００３８】

また、上記の目的を達成するために、本発明に係る固体撮像素子の製造方法は、入射光を光電変換する受光部を有すると共に、その表面に酸化物層が形成された半導体基板の上層に、前記酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成される酸素供給層を形成する工程と、該酸素供給層よりも上層に密着層を介して遮光層を形成する工程とを備える。

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【００３９】
ここで、入射光を光電変換する受光部を有すると共に、その表面に酸化物層が形成された半導体基板の上層に、酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成される酸素供給層を形成し、続いて、酸素供給層よりも上層に密着層を介して遮光層を形成することによって、結果として、酸化物層と密着層との間に酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成された酸素供給層を形成することとなる。そのため、酸化物層と半導体基板の界面層（界面酸化物）が保護されてダメージを受けることが無くなり、界面準位の形成による暗電流の発生を抑制することができる。
【００４０】
また、本発明に係る固体撮像素子の製造方法は、入射光を光電変換する受光部を有すると共に、その表面に酸化物層が形成された半導体基板の上層に、前記酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成される酸素供給層を形成する工程と、該酸素供給層よりも上層に密着層を介して配線層を形成する工程とを備える。
【００４１】
ここで、入射光を光電変換する受光部を有すると共に、その表面に酸化物層が形成された半導体基板の上層に、酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成される酸素供給層を形成し、続いて、酸素供給層よりも上層に密着層を介して配線層を形成することによって、結果として、酸化物層と密着層との間に酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成された酸素供給層を形成することとなる。そのため、酸化物層と半導体基板の界面層（界面酸化物）が保護されてダメージを受けることが無くなり、界面準位の形成による暗電流の発生を抑制することができる。
【００４２】
また、上記の目的を達成するために、本発明に係る固体撮像装置は、入射光を光電変換する受光部を含む半導体基板と、該半導体基板の表面に形成された酸化物層と、該酸化物層よりも上層に密着層を介して形成された遮光層と、前記酸化物層と前記密着層との間に配置され、前記酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成された酸素供給層を有する固体撮像素子と、前記受光部に入射光を集光する光学系とを備える。
【００４３】
更に、本発明に係る固体撮像装置は、入射光を光電変換する受光部を含む半導体基板と、該半導体基板の表面に形成された酸化物層と、該酸化物層よりも上層に密着層を介して形成された配線層と、前記酸化物層と前記密着層との間に配置され、前記酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成された酸素供給層を有する固体撮像素子と、前記受光部に入射光を集光する光学系とを備える。
【００４４】
また、上記の目的を達成するために、本発明に係る撮像装置は、入射光を光電変換する受光部を含む半導体基板と、該半導体基板の表面に形成された酸化物層と、該酸化物層よりも上層に密着層を介して形成された遮光層と、前記酸化物層と前記密着層との間に配置され、前記酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成された酸素供給層を有する固体撮像素子と、前記受光部に入射光を集光する光学系と、前記受光部で光電変換された信号電荷を処理する信号処理部とを備える。
【００４５】
更に、本発明に係る撮像装置は、入射光を光電変換する受光部を含む半導体基板と、該半導体基板の表面に形成された酸化物層と、該酸化物層よりも上層に密着層を介して形成された配線層と、前記酸化物層と前記密着層との間に配置され、前記酸化物層を構成する材料の酸化エンタルピーよりも小さな酸化エンタルピーを示す材料から構成された酸素供給層を有する固体撮像素子と、前記受光部に入射光を集光する光学系と、前記受光部で光

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電変換された信号電荷を処理する信号処理部とを備える。
【発明の効果】
【００４６】
本発明の固体撮像素子及びその製造方法で得られる固体撮像素子、並びに固体撮像装置及び撮像装置では、界面ダメージを回避し、信頼性や密着性を劣化させることなく暗電流の発生を抑制することができる。
【図面の簡単な説明】
【００４７】
【図１】本発明の各実施の形態に適用されるＣＭＯＳ型固体撮像装置の一例の概略構成図である。
【図２】本発明に係る固体撮像装置の第１の実施の形態を説明するための模式図である。
【図３（ａ）】第１の実施の形態の変形例を説明するための模式図（１）である。
【図３（ｂ）】第１の実施の形態の変形例を説明するための模式図（２）である。
【図４】第１の実施の形態の固体撮像装置の製造方法を説明するための模式図（１）である。
【図５】第１の実施の形態の固体撮像装置の製造方法を説明するための模式図（２）である。
【図６】本発明に係る固体撮像装置の第２の実施の形態を説明するための模式図である。
【図７】第２の実施の形態の固体撮像装置の製造方法を説明するための模式図（１）である。
【図８】第２の実施の形態の固体撮像装置の製造方法を説明するための模式図（２）である。
【図９】本発明に係る固体撮像装置の第３の実施の形態を説明するための模式図である。
【図１０（ａ）】第３の実施の形態の変形例を説明するための模式図（１）である。
【図１０（ｂ）】第３の実施の形態の変形例を説明するための模式図（２）である。
【図１０（ｃ）】第３の実施の形態の変形例を説明するための模式図（３）である。
【図１１】第３の実施の形態の固体撮像装置の製造方法を説明するための模式図（１）である。
【図１２】第３の実施の形態の固体撮像装置の製造方法を説明するための模式図（２）である。
【図１３】本発明に係る固体撮像装置の第４の実施の形態を説明するための模式図である。
【図１４】第４の実施の形態の固体撮像装置の製造方法を説明するための模式図（１）である。
【図１５】第４の実施の形態の固体撮像装置の製造方法を説明するための模式図（２）である。
【図１６】本発明を適用した撮像装置の一例であるカメラ７７を説明するための模式図である。
【図１７】第１の実施の形態の変形例を説明するための模式図である。
【図１８】有機光電変換膜と有機カラーフィルタ層の平面的配置（コーディング）の一例を説明するための模式図である。
【図１９】単位画素の回路構成の一例を説明するための模式図である。
【図２０】従来のＣＭＯＳ型固体撮像装置（表面照射型）を説明するための模式図である。
【図２１】従来のＣＭＯＳ型固体撮像装置（裏面照射型）を説明するための模式図である。
【図２２】従来の裏面照射型固体撮像装置の構造を説明するための模式図である。
【発明を実施するための形態】
【００４８】
以下、本発明を実施するための形態（以下、「実施の形態」と称する）について説明す

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る。なお、説明は以下の順序で行う。
１．ＣＭＯＳ型固体撮像装置の概略構成例
２．第１の実施の形態（裏面照射型固体撮像装置の場合（１））
３．第２の実施の形態（裏面照射型固体撮像装置の場合（２））
４．第３の実施の形態（表面照射型固体撮像装置の場合（１））
５．第４の実施の形態（表面照射型固体撮像装置の場合（２））
６．第５の実施の形態（撮像装置の場合）
７．変形例
【００４９】
＜１．ＣＭＯＳ型固体撮像装置の概略構成例＞
図１に、本発明の各実施の形態に適用されるＣＭＯＳ型固体撮像装置の一例の概略構成を示す。ここで示す固体撮像装置１は、図１に示す様に、半導体基板１１（例えばシリコン基板）に複数の光電変換素子を含む画素２が規則的に２次元的に配列された画素領域（いわゆる撮像領域）３と、周辺回路部とを有して構成されている。
【００５０】
画素２は、光電変換素子となる例えばフォトダイオードと、複数の画素トランジスタ（いわゆるＭＯＳトランジスタ）を有している。複数の画素トランジスタは、例えば転送トランジスタ、リセットトランジスタ及び増幅トランジスタの３つのトランジスタで構成することができる。その他、選択トランジスタを追加して４つのトランジスタで構成することもできる。
【００５１】
図１９は画素２の単位画素の回路構成の一例を説明するための模式図である。
単位画素は、光電変換素子として例えばフォトダイオード５１を有し、この１個のフォトダイオード５１に対して、転送トランジスタ５２、増幅トランジスタ５３、アドレストランジスタ５４、リセットトランジスタ５５の４つのトランジスタを能動素子として有する。
【００５２】
フォトダイオード５１は、入射光をその光量に応じた量の電荷（ここでは電子）に光電変換する。転送トランジスタ５２は、フォトダイオード５１とフローティングディフュージョンＦＤとの間に接続されている。そして、駆動配線５６を通じて転送トランジスタのゲート（転送ゲート）に駆動信号が与えられることで、フォトダイオード５１で光電変換された電子をフローティングディフュージョンＦＤに転送する。
【００５３】
フローティングディフュージョンＦＤには、増幅トランジスタ５３のゲートが接続されている。増幅トランジスタ５３は、アドレストランジスタ５４を介して垂直信号線５７に接続され、画素部外の定電流源Ｉとソースフォロアを構成している。駆動配線５８を通してアドレス信号がアドレストランジスタ５４のゲートに与えられ、アドレストランジスタ５４がオンすると、増幅トランジスタ５３はフローティングディフュージョンＦＤの電位を増幅してその電位に応じた電圧を垂直信号線５７に出力する。垂直信号線５７を通じて、各画素から出力された電圧はＳ／Ｈ・ＣＤＳ回路に出力される。
【００５４】
リセットトランジスタ５５は、電源ＶｄｄとフローティングディフュージョンＦＤとの間に接続されている。駆動配線５９を通してリセットトランジスタ５５のゲートにリセット信号が与えられることで、フローティングディフュージョンＦＤの電位を電源電位Ｖｄｄにリセットする。
【００５５】
これらの動作は、転送トランジスタ５２、アドレストランジスタ５４及びリセットトランジスタ５５の各ゲートが行単位で接続されていることから、１行分の各画素について同時に行われることとなる。
【００５６】

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SOLID STATE IMAGE SENSOR, MANUFACTURING METHOD THEREFOR, AND ELECTRONIC APPARATUS

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Abstract of JP2012169530 (A)

PROBLEM TO BE SOLVED: To enhance the image quality of a captured image.SOLUTION: A first light shielding part 313A is provided in a trench TR formed in a pixel separation part 301 of a semiconductor substrate 101. A second light shielding part 313B is provided on the upper surface of the first light shielding part 313A. The second light shielding part 313B is formed so that the center of the second light shielding part 313B is shifted more to the peripheral side of a pixel region PA than the center of the pixel separation part 301, on the periphery of the center of the pixel region PA. In other words, "pupil correction" is performed for at least the second light shielding part.

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DESCRIPTION JP2012169530

PROBLEM TO BE SOLVED: To improve image quality of captured images. A first light shielding portion 313 A is provided inside a trench TR formed in a pixel separation portion 301 of a semiconductor substrate 101. At the same time, the second light shielding portion 313B is provided on the upper surface side of the first light shielding portion 313A. Here, in order to shift the center of the second light shielding portion 313 </ b> B more toward the periphery of the pixel region PA than the center of the pixel separating portion 301 around the center of the pixel region PA, the second light shielding portion 313B are formed. That is, "pupil correction" is performed for at least the second light shielding portion. (FIG.

Solid-state imaging device, manufacturing method thereof, electronic device

[0001]
The present technology relates to a solid-state imaging device, a manufacturing method thereof, and an electronic apparatus.

[0002]

Electronic devices such as digital video cameras and digital still cameras include solid state imaging devices.

For example, a CMOS (Complementary Metal Oxide Semiconductor) type image sensor and a CCD (Charge Coupled Device) type image sensor are included as a solid-state imaging device.

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[0003]

In the solid-state imaging device, a plurality of pixels are arranged in a pixel region of a substrate. In each pixel, a photoelectric conversion unit is provided. The photoelectric conversion unit is, for example, a photodiode, and receives incident light on a light receiving surface and photoelectrically converts it to generate a signal charge.

[0004]

Among solid-state image pickup devices, a CCD image sensor has a vertical transfer portion provided between a plurality of pixel rows arranged in a vertical direction in a pixel region. In the vertical transfer section, a plurality of transfer electrodes are provided so as to face the vertical transfer channel region with a gate insulating film interposed therebetween, and the signal charges read from the photoelectric conversion section by the charge readout section are transferred in the vertical direction As shown in FIG.

[0005]

On the other hand, in the CMOS image sensor, in addition to the photoelectric conversion portion, pixels are formed so as to include pixel transistors. The pixel transistor is configured to read the signal charge generated by the photoelectric conversion unit and output it as an electric signal to the signal line.

[0006]

Generally, in a solid-state imaging device, a substrate is provided on the surface side where a multilayer wiring layer in which a plurality of wirings are laminated is provided, and light incident from the surface side of the substrate is received by the photoelectric conversion portion on the light receiving surface .

[0007]

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In the case of "surface illumination type", a multilayer wiring layer is interposed between the microlens and the light receiving surface, and the distance between the light collecting surface and the light receiving surface is long.

Therefore, when light is incident at an inclination with respect to the light receiving surface, the light included in the multilayer wiring layer may be blocked and may not reach the light receiving surface in some cases. Therefore, it may be difficult to improve the sensitivity.

[0008]
For this reason, a "backside illumination type" in which the photoelectric conversion unit receives light incident from the back side opposite to the surface on which the multilayer wiring layer is provided on the substrate has been proposed.

[0009]

In the solid-state imaging device, incident light incident on one pixel may not be incident on the photodiode of the one pixel but may be incident on the photodiode of another adjacent pixel.

Therefore, due to such an optical phenomenon, noise is included in the signal, and the image quality of the captured image may be deteriorated in some cases. For example, in the case of capturing a color image, when incident light is incident obliquely with respect to the light receiving surface, it is not incident on the light receiving surface right under the incident light but another light receiving originally receiving colored light of another color May enter the surface. For this reason, so-called "color mixing" occurs, which causes color misregistration in the captured color image, which may degrade image quality. In order to suppress the occurrence of such a problem, a light shielding film is provided between a plurality of pixels (see, for example, Patent Documents 1 and 2).

[0010]

Further, at the central portion of the pixel region in which a plurality of pixels are arranged, the angle of the principal ray incident through the external optical system is substantially perpendicular to the light receiving surface, whereas the pixel In the peripheral portion of the region, the angle of the incident principal ray is inclined. For this reason, the central portion of

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the captured image becomes a bright image and the peripheral portion becomes a dark image in some cases. In other words, a so-called shading phenomenon may occur, which may degrade image quality. In order to solve such a problem, it is called "pupil correction" to correct the arrangement of on-chip lenses and the like. Specifically, it has been practiced to provide an on-chip lens so that the position of the on-chip lens disposed around the pixel region shifts toward the center of the pixel region with respect to the light receiving surface. For example, each part is arranged so that the pitch of the on-chip lens becomes narrower than the pitch of the plurality of photoelectric conversion parts arranged in the pixel region (see, for example, Patent Document 3).

[0011]

Further, in the solid-state imaging device, in order to suppress the occurrence of dark current due to the interface state of the semiconductor substrate provided with the photoelectric conversion portion to improve the image quality, the photoelectric conversion portion is formed by HAD (Hole Accumulation Diode) structure has been proposed. In the HAD structure, the generation of dark current is suppressed by forming a positive charge accumulation (hole) accumulation region on the light receiving surface of the n-type charge accumulation region. In order to form the positive charge accumulation region at the interface portion of the photoelectric conversion portion, it has been proposed to provide "a film having a negative fixed charge" as a pinning layer to suppress the generation of dark current. For example, a high dielectric film such as a hafnium oxide film (HfO 2 film) is used as "a film having negative fixed charges" (see, for example, Patent Document 4).

[0012]

In order to suppress the generation of dark current, it has been proposed to provide a control gate on the front side of the "back side irradiation type" and apply a negative voltage to the control gate (for example, refer to Japanese Patent Application Laid-Open reference). In addition, in order to suppress the generation of dark current, it has been proposed to apply a negative voltage to a metal light-shielding film having a light-receiving surface portion for receiving light having an opening (see, for example, Patent Document 6)

[0013]

As described above, in the solid-state imaging device, various techniques have been proposed to improve the image quality of the captured image.

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[0014]
Japanese Unexamined Patent Publication No. 2010-109295 Patent Document 2: Japanese Patent Application Laid-Open No. 2010-186818 Patent Document 3: Japanese Patent No. 3551437 Patent Document 4: Japanese Unexamined Patent Application Publication No. 2008-306154 Patent Document 2: Japanese Unexamined Patent Application Publication No. 2007-258684 Patent Document 3: Japanese Unexamined Patent Publication No. Hei 5-275673

[0015]
In the solid-state imaging device, further improvement of the image quality etc. of the captured image is desired.

[0016]
Accordingly, the present technology provides a solid-state imaging device, a manufacturing method thereof, and an electronic device, which can improve the image quality of a captured image and the like.

[0017]
In the solid-state imaging device and the electronic device of the present technology, a plurality of the solid-state imaging device and the electronic device are provided inside the semiconductor substrate, corresponding to each of a plurality of pixels arranged in the pixel region of the semiconductor substrate with a space therebetween. And a pixel separating portion provided inside the semiconductor substrate so as to be interposed between the plurality of pixels in the pixel region, wherein the pixel separating portion is formed on the semiconductor substrate A first light shielding portion provided inside a trench formed on the incident surface side of the first light shielding portion on the incident surface side of the semiconductor substrate and provided on the incident surface side of the first light shielding portion And the second light shielding portion is formed so that the center of the second light shielding portion in the periphery from the center of the pixel region is larger than the center of the pixel separating portion in the pixel Shift a lot to the side of the area It is sea urchin formation.

[0018]
A manufacturing method of a solid-state image pickup device according to the present technology is a method of manufacturing a solid-state image pickup device including a photoelectric conversion portion that receives incident light on a light receiving surface, so as to correspond to each of a plurality of pixels arranged in a pixel region of a semiconductor

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substrate with a space therebetween A pixel separating portion forming step of providing a pixel separating portion inside the semiconductor substrate so as to be interposed between the plurality of pixels in the pixel region, wherein the pixel separation In the portion forming step, a first light shielding portion is provided in a trench formed in the pixel separation portion of the semiconductor substrate on the incident surface side, and a first light shielding portion is formed on the surface of the semiconductor substrate on the incident surface side, At least the second light shielding portion is provided on the incident surface side of the one light shielding portion, and in the step of forming the second light shielding portion, the center of the second light shielding portion is located closer to the periphery than the center of the pixel region, The center of Against it, to shift more toward the periphery of the pixel region, forming the second light-shielding portion.

[0019]

In the present technology, the first light shielding portion is provided inside the trench formed in the pixel separation portion of the semiconductor substrate, and the second light shielding portion is provided on the incident surface side of the first light shielding portion.

Here, the second light shielding portion is formed so that the center of the second light shielding portion shifts more toward the periphery of the pixel region than the center of the pixel separation portion in the periphery of the center of the pixel region.

That is, "pupil correction" is performed at least for the second light shielding portion.

[0020]

According to the present technology, it is possible to provide a solid-state imaging device, a manufacturing method thereof, and an electronic device capable of improving the image quality or the like of a captured image.

[0021]

FIG. 1 is a configuration diagram showing a configuration of a camera in the first embodiment.

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FIG. 2 is a diagram showing the overall configuration of the solid-state imaging device according to the first embodiment.

FIG. 3 is a diagram showing a main part of the solid-state imaging device according to the first embodiment.

FIG. 4 is a diagram showing a main part of the solid-state imaging device according to the first embodiment.

FIG. 5 is a diagram showing a main part of the solid-state imaging device according to the first embodiment.

FIG. 6 is a diagram showing a main part of the solid-state imaging device according to the first embodiment. FIG. 7 is a diagram showing a main part of the solid-state imaging device according to the first embodiment. FIG. 8 is a timing chart showing a control signal to be transmitted to the pixel transistor Tr of the pixel P when imaging is performed in the first embodiment. FIG. 9 is a diagram showing a method of manufacturing the solid-state imaging device according to the first embodiment. FIG. 10 is a diagram showing a method of manufacturing the solid-state imaging device in the first embodiment. FIG. 11 is a diagram showing a method for manufacturing the solid-state imaging device in the first embodiment. FIG. 12 is a view showing a manufacturing method of the solid-state imaging device in the first embodiment. FIG. 13 is a diagram showing a manufacturing method of the solid-state imaging device in the first embodiment. FIG. 14 is a cross-sectional view showing how the incident light enters the solid-state imaging device in the first embodiment. FIG. 15 is a diagram showing a main part of the solid-state imaging device according to the second embodiment. FIG. 16 is a cross-sectional view showing how incident light enters the solid-state imaging device in the second embodiment. FIG. 17 is a diagram showing a main part of the solid-state imaging device according to the third embodiment. FIG. 18 is a cross-sectional view showing how incident light enters the solid-state imaging device in the third embodiment. FIG. 19 is a diagram showing a main part of the solid-state imaging device according to the fourth embodiment. FIG. 20 is a diagram showing a main part of the solid-state imaging device according to the fourth embodiment. FIG. 21 is a diagram showing a main part of the solid-state imaging device in the fifth embodiment. FIG. 22 is a diagram showing a main part of the solid-state imaging device in the sixth embodiment. FIG. 23 is a diagram showing a main part of the solid-state imaging device according to the seventh embodiment. FIG. 24 is a diagram showing a main part of the solid-state imaging device according to the eighth embodiment. FIG. 25 is a diagram showing a main part of the solid-state imaging device according to the ninth embodiment.

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[0022]
Embodiments will be described with reference to the drawings.

[0023]

The description is given in the following order.

1. Embodiment 1 (Case of "pupil correction" on the upper part of the light shielding film of the pixel separating section) 2. Second Embodiment (Case of "Pupil Correction" on the Top of Light Shielding Film of Pixel Separation Unit) 3. Third Embodiment (Case of "Pupil Correction" on the Top of Light Shielding Film of Pixel Separation Unit) Embodiment 4 (a case where a diffusion layer is provided in a pixel separation portion) 5. Fifth Embodiment (Case of "Pupil Correction" on the Top and Bottom of Light Shielding Film of Pixel Separation Unit) Embodiment 6 (Case of "pupil correction" on the upper part and the lower part of the light shielding film of the pixel separation part) Embodiment 7 (Case of "pupil correction" on the upper part and the lower part of the light shielding film of the pixel separation part) 8. Eighth Embodiment (Penetration of Shading Film of Pixel Separation Unit) 9. Embodiment 9 (Case where the light shielding film of the pixel separating portion is penetrated) Other

[0024]

< 1. First Embodiment (A) Device Configuration (A-1) Configuration of Main Part of Camera FIG. 1 is a configuration diagram showing a configuration of a camera in a first embodiment.

[0025]
As shown in FIG. 1, the camera 40 includes a solid-state imaging device 1, an optical system 42, a control unit 43, and a signal processing unit 44.

[0026]

In the camera 40, the solid-state imaging device 1 receives incident light H incident as a subject

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image via the optical system 42 on the imaging plane PS and photoelectrically converts it to generate signal charges.

Here, the solid-state imaging device 1 is driven based on a control signal output from the control unit 43, reads the generated signal charge, and outputs an electric signal.

[0027]
The optical system 42 includes optical members such as an imaging lens and a diaphragm and is arranged so as to condense the incident light H onto the imaging surface PS of the solid-state imaging device 1.

[0028]
The control unit 43 outputs various control signals to the solid-state imaging device 1 and the signal processing unit 44, and controls and drives the solid-state imaging device 1 and the signal processing unit 44.

[0029]
The signal processing unit 44 is configured to generate a digital image of the subject image by performing signal processing with the electric signal output from the solid-state imaging device 1 as raw data.

[0030]

In the present embodiment, as shown in FIG. 1, a light beam H 1 emitted from the optical system 42 is incident as incident light H at an angle perpendicular to the imaging plane PS at the center portion of the imaging plane PS.

On the other hand, in the peripheral portion of the imaging plane PS, the principal ray H 2 is incident as incident light H at an angle tilted with respect to the direction perpendicular to the imaging plane PS.

Here, the principal ray H 2 of the incident light is inclined from the center of the imaging plane PS toward the periphery.

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This is because the exit pupil distance formed by the diaphragm forming the optical system 42, which will be described later, is finite.

[0031]

(A-2) Main Configuration of Solid-State Imaging Device The overall configuration of the solid-state imaging device 1 will be described.

[0032]

FIG. 2 is a diagram showing the overall configuration of the solid-state imaging device according to the first embodiment.

[0033]

The solid-state imaging device 1 of this embodiment is a CMOS type image sensor, and includes a semiconductor substrate 101, as shown in FIG. 2.

In the semiconductor substrate 101, for example, a single crystal silicon substrate is thinned, and a pixel region PA and a peripheral region SA are provided on the surface.

[0034]

As shown in FIG. 2, the pixel region PA has a rectangular shape, and a plurality of pixels P are arranged at equal intervals in the horizontal direction x and the vertical direction y, respectively.

That is, the pixels P are arranged in a matrix.

[0035]

In the pixel region PA, the pixel P is configured to receive incident light and generate signal

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charges. Then, the generated signal charge is read out by a pixel transistor (not shown) and outputted as an electric signal. The detailed configuration of the pixel P will be described later.

[0036]

As shown in FIG. 2, the peripheral area SA is located around the pixel area PA. In the peripheral area SA, a peripheral circuit is provided.

[0037]
Specifically, as shown in FIG. 2, the vertical drive circuit 13, the column circuit 14, the horizontal drive circuit 15, the external output circuit 17, the timing generator (TG) 18, and the shutter drive circuit 19, And is provided as a peripheral circuit.

[0038]
As shown in FIG. 2, the vertical drive circuit 13 is provided in the side portion of the pixel area PA in the peripheral area SA, and is configured to select and drive the pixels P of the pixel area PA in units of rows There.

[0039]

As shown in FIG. 2, the column circuit 14 is provided in the lower end portion of the pixel area PA in the peripheral area SA, and performs signal processing on a signal output from the pixel P on a column basis.

Here, the column circuit 14 includes a CDS (Correlated Double Sampling) circuit (not shown) and performs signal processing for removing fixed pattern noise.

[0040]

As shown in FIG. 2, the horizontal drive circuit 15 is electrically connected to the column circuit 14.

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The horizontal drive circuit 15 includes, for example, a shift register, and sequentially outputs signals held for each column of pixels P in the column circuit 14 to the external output circuit 17.

[0041]

As shown in FIG. 2, the external output circuit 17 is electrically connected to the column circuit 14, performs signal processing on the signal output from the column circuit 14, and outputs it to the outside. The external output circuit 17 includes an AGC (Automatic Gain Control) circuit 17 a and an ADC circuit 17 b. In the external output circuit 17, after the AGC circuit 17 a applies a gain to the signal, the ADC circuit 17 b converts the analog signal to the digital signal and outputs it to the outside.

[0042]

As shown in FIG. 2, the timing generator 18 is electrically connected to the vertical drive circuit 13, the column circuit 14, the horizontal drive circuit 15, the external output circuit 17, and the shutter drive circuit 19, respectively. The timing generator 18 generates various timing signals and outputs the timing signals to the vertical drive circuit 13, the column circuit 14, the horizontal drive circuit 15, the external output circuit 17, and the shutter drive circuit 19, thereby controlling the drive of each part.

[0043]
The shutter drive circuit 19 is configured to select the pixels P in units of rows and adjust the exposure time in the pixels P.

[0044]
(A-3) Detailed Configuration of Solid-State Imaging Device Detailed contents of the solid-state imaging device according to the present embodiment will be described.

[0045]
3 to 7 are diagrams showing the main parts of the solid-state imaging device in the first embodiment.

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[0046]

FIG. 3 is a cross-sectional view of the pixel P.

In FIG. 3, one pixel arranged in the central portion of the pixel area PA shown in FIG. 2 and showing the X 1 -X 2 portion.

[0047]

FIG. 4 is a top view of the pixel P, showing four pixels P arranged in the central portion of the pixel area PA shown in FIG. 2.

In FIG. 4, for the sake of convenience of explanation, there are portions showing each member by using a line other than a solid line such as a broken line.

[0048]

FIG. 5 is a cross-sectional view of the pixel separation unit 301.

FIG. 6 is a top view of the pixel separation unit 301. In FIGS. 5 and 6, (a) shows the pixel separation section 301 between the pixels P arranged in the central portion of the pixel area PA shown in FIG. 2, and shows the X 1 C - X 2 C section. On the other hand, (b) shows a pixel separation section 301 between pixels P arranged in the peripheral part of the pixel region PA shown in FIG. 2, and shows the X 1 S - X 2 S part. That is, in FIGS. 5 and 6, the pixel separation section 301 provided between a pair of pixels P aligned in the horizontal direction x is shown. Although not shown, the pixel separating unit 301 provided between the pair of pixels P arranged in the vertical direction y is also provided in a form similar to that of FIG. 5 and FIG. 6.

[0049]

Further, FIG. 7 shows the circuit configuration of the pixel P.

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[0050]

As shown in FIG. 3, in the solid-state imaging device 1, a photodiode 21 is provided inside a semiconductor substrate 101.

Here, it is provided on the semiconductor substrate 101 of thinned single crystal silicon.

[0051]
On the back surface (upper surface in FIG. 3) of the semiconductor substrate 101, members such as a color filter CF and a microlens ML are provided.

[0052]

On the other hand, the pixel transistor Tr shown in FIG. 7 is provided on the front surface (the lower surface in FIG. 3) of the semiconductor substrate 101 although not shown in FIG. 3.

As shown in FIG. 3, a wiring layer 111 is provided so as to cover the pixel transistor Tr, and on the surface of the wiring layer 111 opposite to the semiconductor substrate 101 side, a support substrate SS Are provided.

[0053]
That is, the solid-state imaging device 1 of the present embodiment is a "back-illuminated CMOS image sensor", in which the incident light H incident from the back side (upper surface) side is received by the photodiode 21 and a color image is generated by imaging As shown in FIG.

[0054]
Details of each part will be sequentially explained.

[0055]

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(A) Photodiode 21 In the solid-state imaging device 1, a plurality of photodiodes 21 are arranged in the pixel area PA so as to correspond to the plurality of pixels P shown in FIG. 2.

That is, on the imaging plane (xy plane), they are provided side by side in the horizontal direction x and the vertical direction y orthogonal to the horizontal direction x.

[0056]
A plurality of photodiodes 21 are provided in the semiconductor substrate 101 with a space therebetween so that the incident light H is received by the light receiving surface JS and photoelectrically converted so as to generate and accumulate signal charges.

[0057]

Here, as shown in FIG. 3, the photodiode 21 receives incident light H incident from the rear surface (upper surface in FIG. 3) of the semiconductor substrate 101.

As shown in FIG. 3, a flattening film HT, a color filter CF, and a microlens ML are provided above the photodiode 21. The incident light H that has entered through each part sequentially is received by the light receiving surface JS And photoelectric conversion is performed.

[0058]
As shown in FIG. 3, the photodiode 21 is provided in the semiconductor substrate 101.

[0059]

For example, in the photodiode 21, the n-type semiconductor region 101 n is formed as a charge accumulation region that accumulates charges (here, electrons).

In the photodiode 21, the n-type semiconductor region 101 n is provided inside the p-type semiconductor regions 101 pa, 101 pc of the semiconductor substrate 101.

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Here, a p-type semiconductor region 101 pc is provided on the back surface (upper surface) side of the semiconductor substrate 101 in the n-type semiconductor region 101 n. In the n-type semiconductor region 101 n, on the surface (lower surface) side of the semiconductor substrate 101, a p-type semiconductor region 101 pc having a higher impurity concentration than the back surface (upper surface) side is provided. That is, the photodiode 21 has the HAD structure, and the p-type semiconductor regions 101 pa and 101 pc are formed so as to suppress generation of dark current at each interface between the upper surface side and the lower surface side of the n-type semiconductor region 101 n Has been done.

[0060]

As shown in FIG. 3, a pixel separation section 301 for electrically separating a plurality of pixels P is provided, and the photodiode 21 is provided in the region of the pixel P partitioned by the pixel separation section 301 Has been done. For example, as shown in FIG. 4, the pixel separating unit 301 is formed in a grid pattern so as to be interposed between a plurality of pixels P, and the photodiode 21 is formed by arranging the pixels P And is formed in the region.

[0061]

As shown in FIG. 7, the anode of each photodiode 21 is grounded, the accumulated signal charge (here, electrons) is read out by the pixel transistor Tr and is transferred as an electric signal to the vertical signal line 27 And is configured to be outputted.

[0062]

(B) Color Filter CF In the solid-state imaging device 1, as shown in FIG. 3, the color filter CF is provided on the back side (upper surface in FIG. 3) side of the semiconductor substrate 101.

[0063]

Here, as shown in FIG. 3, the planarizing film HT is formed of a light transmitting material so as to cover the back surface (upper surface) of the semiconductor substrate 101, and the semiconductor substrate 101 A color filter CF is formed on the back surface (upper surface) of the color filter CF.

[0064]

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As shown in FIG. 4, the color filter CF includes a red filter layer CFR, a green filter layer CFG, and a blue filter layer CFB.

Each of the red filter layer CFR, the green filter layer CFG, and the blue filter layer CFB is disposed adjacent to each other, and one of them is provided corresponding to each of the plurality of pixels P.

[0065]

Here, as shown in FIG. 4, the red filter layer CFR, the green filter layer CFG, and the blue filter layer CFB are arranged so as to be aligned in a Bayer array.

That is, the plurality of green filter layers CFG are arranged side by side in the diagonal direction so as to form a checkered pattern.

The red filter layer CFR and the blue filter layer CFB are arranged in the diagonal direction in the plurality of green filter layers CFG.

[0066]

In the color filter CF, the red filter layer CFR has high light transmittance in a wavelength band corresponding to red (for example, 625 to 740 nm). In other words, the red filter layer CFR is formed so that the incident light H passes through the light receiving surface JS as red light.

[0067]

In the color filter CF, the green filter layer CFG has high light transmittance in a wavelength band corresponding to green (for example, 500 to 565 nm). In other words, the green filter layer CFG is formed so that the light transmittance of light in a wavelength range shorter than that of the red filter layer CFR is high, and the incident light H passes through the light receiving surface JS as green light.

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[0068]

In the color filter CF, the blue filter layer CFB has high light transmittance in a wavelength band corresponding to blue (for example, 450 to 485 nm). In other words, the blue filter layer CFB is formed so that the light transmittance of light having a wavelength range shorter than that of the green filter layer CFG is high, and the incident light passes through the light receiving surface JS as blue light.

[0069]

In this way, the color filter CF has a plurality of types of filter layers CFR, CFG, CFB with high transmittance for light in different wavelength ranges corresponding to each of the plurality of pixels P and are disposed adjacent to each other .

[0070]

(C) Microlens ML In the solid-state imaging device 1, as shown in FIG. 3, the microlens ML is provided on the upper surface of the color filter CF on the side of the back surface (upper surface in FIG. 3) of the semiconductor substrate 101 .

[0071]

A plurality of microlenses ML are arranged so as to correspond to each pixel P.

The microlens ML is a convex lens that protrudes in a convex shape on the back surface side of the semiconductor substrate 101 and is configured to collect incident light H to the photodiode 21 of each pixel P.

For example, the microlens ML is formed using an organic material such as a resin.

[0072]

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(D) Pixel Separation Unit 301 In the solid-state imaging device 1, the pixel separation unit 301 is formed so as to partition a plurality of pixels P as shown in FIGS. 3 and 4. The pixel separation unit 301 electrically separates the respective pixels P from each other. That is, inside the semiconductor substrate 301, the photodiodes 21 of each pixel P are electrically isolated.

[0073]
As shown in FIG. 3, in the pixel separating section 301, p type semiconductor regions 101 pa, 101 pc are provided between the n type semiconductor regions 101 n constituting the charge accumulation region of the photodiode 21.

[0074]
As shown in FIG. 3, in the pixel separating section 301, in the portion of the semiconductor substrate 101 on the rear surface (upper surface) where the incident light H is incident and located on the side of the photodiode 21, the trench TR Are provided.

[0075]
As shown in FIG. 3, the pixel separation portion 301 includes an insulating layer 311 and a light shielding layer 313, and these portions are provided inside the above-described trench TR.

[0076]

As shown in FIG. 4, the pixel separating unit 301 has a lattice shape in plan view, and is interposed between a plurality of pixels P.

A trench TR is formed in the pixel separating portion 301 so that the planar shape is a lattice shape.

A photodiode 21 is formed in the rectangular region partitioned by the grid-like pixel separation portion 301.

[0077]

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Specifically, as shown in FIG. 4, the pixel separating unit 301 divides the pixel P so that it extends in a straight line in a vertical direction y orthogonal to the horizontal direction x between a pair of pixels P arranged in the horizontal direction x For example.

Along with this, the pixel separation section 301 is provided so as to extend linearly in the horizontal direction x between a pair of pixels P aligned in the vertical direction y.

[0078]

As shown in FIG. 4, similarly to the pixel separation section 301, the trench TR extends in the vertical direction y between a pair of pixels P aligned in the horizontal direction x and a pair of Is provided so as to extend in the horizontal direction x between the pixels P. The insulating layer 311 and the light shielding layer 313 are provided so as to extend in the vertical direction y and the horizontal direction x between the respective pixels P like the pixel separation portion 301 and the trench TR.

[0079]

As shown in FIGS. 5 and 6, the pixel separating unit 301 separates a portion located in the center of the pixel area PA (see FIG. 2) (in the case of (a)) and a portion located in the periphery of the pixel area PA (In the case of b), some are formed in different modes.

[0080]

As shown in FIGS. 5 and 6, in the pixel separating section 301, the trench TR is formed such that the center portion (in the case of (a)) of the pixel area PA (see FIG. 2) and the peripheral portion ((b) of the pixel area PA) In the case of FIG.

[0081]

Specifically, as shown in FIG. 5, the trench TR has a tapered cross section of a plane (xz plane) along the horizontal direction x and the depth direction z, and the trench TR is formed on the back surface (upper surface) Side is formed to be wider than the width TH 1 on the surface (lower surface) side.

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In addition, as shown in FIG. 5, the trench TR is formed such that this cross section is symmetrical with respect to the axis along the depth direction z.

[0082]
As shown in FIG. 6, the trench TR is formed so that its side surface extends in the vertical direction y.

[0083]

In the present embodiment, as shown in FIGS. 5 and 6 (a), in the central portion of the pixel region PA (see FIG. 2), the trench TR is located between the pair of pixels P in the central axis in the horizontal direction x Coincides with the center axis 301CX in the horizontal direction x of the pixel separation section 301. [

2B), the central axis in the horizontal direction x between the pair of pixels P in the peripheral portion of the pixel area PA (see FIG. 2) is located in the horizontal direction x of the pixel separation unit 301 And is formed so as to coincide with the center axis 301CX in the center axis 301CX.

[0084]

As shown in FIGS. 5 and 6, the insulating layer 311 is provided so as to cover the inner surface of the trench TR formed on the back surface (upper surface) side of the semiconductor substrate 101.

The insulating layer 311 is similarly formed in the central portion (in the case of (a)) of the pixel region PA (see FIG. 2) and in the peripheral portion (in the case of (b)) of the pixel region PA.

[0085]

As shown in FIGS. 5 and 6, a light shielding layer 313 is provided so as to bury the inside of the trench TR covered with the insulating layer 311. A part of the light shielding layer 313 is formed

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in a different manner in the center part (in the case of (a)) of the pixel region PA (see FIG. 2) and in the peripheral part (in the case of (b)) of the pixel region PA There.

[0086]
5 and 6 show the pixel separation section 301 provided between a pair of pixels P aligned in the horizontal direction x, the pixel separation section 301 provided between a pair of pixels P arranged in the vertical direction y Are also formed in the same manner as above.

[0087]
The details of each part constituting the pixel separation section 301 will be described.

[0088]
(D-1) Insulating Layer 311 The insulating layer 311 is provided in the pixel separating portion 301, as shown in FIG. 3.

[0089]
Here, the insulating layer 311 is formed inside the trench TR so as to cover the side surface and the bottom surface.

[0090]
3, in addition to the pixel separating section 301, the insulating layer 311 is formed so as to cover the light receiving surface JS on which the incident light H is incident on the back surface (upper surface) of the semiconductor substrate 101 There.

[0091]
In the present embodiment, the insulating layer 311 includes a first insulating film 311 A and a second insulating film 311 B, as shown in FIG. 3.

[0092]

As shown in FIG. 3, the first insulating film 311 </ b> A is formed inside the trench TR and covers the side surface and the bottom surface in the pixel separation portion 301.

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As shown in FIG. 3, the first insulating film 311 </ b> A is formed so as to cover the light receiving surface JS on which the incident light H is incident on the back surface (upper surface) of the semiconductor substrate 101.

[0093]

As shown in FIG. 3, the second insulating film 311 B is formed so as to cover the side surface and the bottom surface of the trench TR inside the trench TR via the first insulating film 311 A in the pixel separation portion 301 as shown in FIG. 3 .

As shown in FIG. 3, the second insulating film 311 </ b> B is formed so as to cover the light receiving surface JS on the back surface (upper surface) of the semiconductor substrate 101 with the first insulating film 311 </ b> A interposed therebetween.

[0094]
As shown in FIGS. 5 and 6, the first insulating film 311 A and the second insulating film 311 B are formed so that the center portion (in the case of (a)) of the pixel region PA (see FIG. 2) and the peripheral portion (B)) are formed in the same manner.

[0095]
Each of the first insulating film 311 A and the second insulating film 311 B is formed using an insulating material such as SiO 2, SiN, a low-k material (SiOC, SiLK) or the like.

[0096]

Here, it is preferable that the refractive index of the first insulating film 311 </ b> A is formed using a material between the second insulating film 311 </ b> B and the semiconductor substrate 101.

That is, it is preferable that the first insulating film 311 </ b> A and the second insulating film 311 </ b> B are laminated so that the refractive index is sequentially lowered in the trench TR.

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By doing like this, it is possible to suitably prevent light traveling from the semiconductor substrate 101 side to the trench TR from being reflected at the interface.

[0097]

Although the case where the insulating layer 311 is formed of two films of the first insulating film 311 </ b> A and the second insulating film 311 </ b> B has been described, the insulating layer 311 is not limited thereto.

The insulating film 311 may be composed of three or more films.

In addition, the insulating layer 311 may be formed of a single material.

[0098]

(D-2) Light-shielding layer 313 As shown in FIGS. 3 and 4, the light-shielding layer 313 is provided in the pixel separation portion 301.

[0099]

In this embodiment, as shown in FIGS. 3 and 4, the light shielding layer 313 includes a first light shielding portion 313 A and a second light shielding portion 313 B, and the first light shielding portion 313 A and the second light shielding portion 313 B Are provided so as to be integrated with each other.

[0100]

As shown in FIG. 3, the first light shielding portion 313 A of the light shielding layer 313 is formed so as to bury the inside of the trench TR with the insulating layer 311 interposed therebetween.

The first light shielding portion 313 </ b> A is provided within the range of a portion where the trench TR is provided on the back surface (upper surface) of the semiconductor substrate 101.

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[0101]

Here, as shown in FIG. 3, the first light-shielding portion 313 A is formed so that a cross section of a plane (xz plane) along the horizontal direction x and the depth direction z is tapered.

That is, as shown in FIG. 5 (a), the first light shielding portion 313 A is formed so that the width HA 2 on the back surface (upper surface) side of the semiconductor substrate 101 is wider than the width HA 1 on the surface (lower surface) side There.

In addition, the first light shielding portion 313 </ b> A is formed so that this cross section is symmetrical with respect to the axis along the depth direction z.

[0102]

As shown in FIGS. 5 and 6, the first light shielding portion 313 A has a central portion (in the case of (a)) of the pixel region PA (see FIG. 2) and a peripheral portion (in the case of (b)) of the pixel region PA, In the same manner.

[0103]

Specifically, as shown in FIGS. 5 and 6 (a), in the center portion of the pixel area PA, the first light shielding portion 313 </ b> A is arranged in a horizontal direction x (x) between a pair of pixels P arranged in the horizontal direction x Is coincident with the central axis 301CX in the horizontal direction x of the pixel separating unit 301. In this case,

[0104]

As shown in FIGS. 5 and 6 (b), also in the peripheral portion of the pixel region PA, the first light shielding portion 313 </ b> A has the center axis in the horizontal direction x larger than the center in the horizontal direction x of the pixel separation portion 301 And is formed to coincide with the shaft 301CX.

[0105]

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As shown in FIG. 3, the second light shielding portion 313 </ b> B of the light shielding layer 313 is formed above the back surface (upper surface) of the semiconductor substrate 101 with the insulating layer 311 interposed therebetween.

The lower surface of the second light shielding portion 313 </ b> B is connected to the upper surface of the first light shielding portion 313 </ b> A.

In addition, the second light shielding portion 313 </ b> B is provided so as to protrude in a convex shape above the back surface (upper surface) of the semiconductor substrate 101 covered with the insulating layer 311.

The second light shielding portion 313 </ b> B is provided in the range of the portion where the trench TR is provided on the back surface (upper surface) of the semiconductor substrate 101.

[0106]

Here, as shown in FIG. 3, the second light-shielding portion 313 </ b> B is formed between the pair of pixels P arranged adjacent to each other in the horizontal direction x, the surface along the horizontal direction x and the depth direction z (the xz plane) Is formed so as to have a rectangular shape.

As shown in FIG. 5A, the second light shielding portion 313B is formed such that the width HB in the horizontal direction x is larger than the widths HB1, HB2 of the first light shielding portion 313A. In addition, the second light shielding portion 313 </ b> B is formed such that the cross section is symmetrical with respect to the axis along the depth direction z.

[0107]

As shown in FIG. 5 and FIG. 6, the second light shielding portion 313 B has a central portion (in the case of (a)) of the pixel region PA (see FIG. 2) and a peripheral portion (in the case of (b)) of the pixel region PA, And are formed at different positions from each other.

[0108]

Specifically, as shown in FIGS. 5 and 6 (a), at the central portion of the pixel region PA (see FIG.

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2), the second light shielding portion 313 </ b> B is formed such that the center of the cross section (xz plane) in the horizontal direction x The axis is formed so as to coincide with the central axis 301CX in the horizontal direction x of the pixel separating unit 301. As shown in FIG.

[0109]

On the other hand, as shown in FIGS. 5 and 6 (b), in the peripheral portion of the pixel region PA (see FIG. 2), the second light shielding portion 313 B is formed such that the center axis in the horizontal direction x of this cross section 313 BCX does not coincide with the center axis 301 CX in the horizontal direction x of the pixel separation unit 301.

Here, the center axis 313 BCX of the second light shielding portion 313 B is located closer to the periphery side (see FIG. 2) of the pixel region PA than the center axis 301 CX of the pixel separation portion 301.

And the second light shielding portion 313 </ b> B is formed so as to shift to the right side in FIG. 5). That is, the second light shielding portion 313 B is formed so that the center axis 313 BCX of the second light shielding portion 313 B and the center axis 301 CX of the pixel separation portion 301 are separated by a predetermined shift amount Dx in the horizontal direction x .

[0110]

As described above, the so-called "pupil correction" is not performed on the first light shielding portion 313 A of the light shielding layer 313, and "pupil correction" is performed on the second light shielding portion 313 B. That is, since the shift amount of the first light shielding portion 313A is zero, the second light shielding portion 313B is formed so that the shift amount Dx of the second light shielding portion 313B is larger than the shift amount of the first light shielding portion 313A ing.

[0111]

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In the present embodiment, the pixel region PA is divided into a central part and a peripheral part thereof, and the pixel region PA is provided with a second light shielding part 313 B as shown in FIGS. 5 and 6 (a) with respect to the central part , And the second light shielding portion 313 B is provided in the peripheral portion as shown in FIGS. 5 and 6 (b). Specifically, as shown in FIG. 5A, at the center of the pixel area PA, the pitch PBc of the second light shielding units 313 </ b> B arranged at equal intervals in the horizontal direction x is equal to the distance between the pixels arranged at equal intervals in the horizontal direction x Is formed to be the same as the pitch PG of the separation section 301. That is, as shown in FIG. 6 (a), the pitch PBc of the second light shielding portion 313 </ b> B extending in the vertical direction y in the horizontal direction x and the pitch PBc of the pixel separating portion 301 extending in the vertical direction y Are aligned in the horizontal direction x are the same as each other. On the other hand, in the peripheral area of the pixel area PA, as shown in FIG. 5 (b), the pitch PBs of the second light shielding units 313 </ b> B arranged at equal intervals in the horizontal direction x is equal to the number of pixels And is formed so as to be wider than the pitch PG of the separation portion 301. That is, as shown in FIG. 6B, the pitch PBc of the second light shielding portion 313 </ b> B extending in the vertical direction y in the horizontal direction x is extended in the vertical direction y of the pixel separation portion 301 Are wider than the pitch PG arranged in the horizontal direction x. Although not shown, the second light shielding portion 313 B is also provided in the vertical direction y as well.

[0112]

In addition to this, with respect to the second light shielding portion 313B, the shift amount Dx between the center axis 313BCX of the second light shielding portion 313B and the center axis 301CX of the pixel separation portion 301 May be increased. Specifically, with respect to each of the second light-shielding portions 313 </ b> B provided in each of the pixel separation portions 301 between the plurality of pixels P aligned in the horizontal direction x, the pitch in the horizontal direction x thereof is larger than the pitch of the pixel separation portion 301 As shown in FIG. The pitch in the vertical direction y of each of the second light shielding portions 313 B provided in each of the pixel separation portions 301 between a plurality of pixels P arranged in the vertical direction y is wider than the pitch of the pixel separation portion 301 As shown in FIG. That is, with respect to the pixel separating portion 301 and the second light shielding portion 313 provided between the pair of pixels P in the pixel region PA, the second light shielding portion 313 is arranged at a wider pitch than the pixel separating portion 301 at equal intervals As shown in FIG.

[0113]

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The light shielding layer 313 is formed using a light shielding material that shields light by reflecting light. For example, a light shielding layer 313 is formed using a metal material such as Ti, TiN, W, Al or the like.

[0114]

In the present embodiment, the first light-shielding portion 313 A and the second light-shielding portion 313 B are formed of the same material and formed so as to be integrated, but the present invention is not limited thereto. The first light shielding portion 313 A and the second light shielding portion 313 B may be formed of different materials. That is, the light shielding layer 313 may have a laminated structure.

[0115]

(E) Pixel Transistor Tr In the solid-state imaging device 1, a plurality of pixel transistors Tr are provided so as to correspond to the plurality of pixels P shown in FIG. 2.

[0116]

As shown in FIG. 7, the pixel transistor Tr includes a transfer transistor 22, an amplification transistor 23, a selection transistor 24, and a reset transistor 25, and is configured to read the signal charge from the photodiode 21 and output it as an electric signal There.

[0117]

Though not shown in FIG. 3, each of the transistors 22 to 25 constituting the pixel transistor Tr is provided on the surface on which the wiring layer 111 is provided in the semiconductor substrate 101.

For example, each of the transistors 22 to 25 is an N-channel MOS transistor, and each gate is formed using, for example, polysilicon.

Each of the transistors 22 to 25 is covered with a wiring layer 111.

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[0118]

In the pixel transistor Tr, as shown in FIG. 7, the transfer transistor 22 is configured to transfer the signal charge generated by the photodiode 21 to the floating diffusion FD. Specifically, as shown in FIG. 7, the transfer transistor 22 is provided between the cathode of the photodiode 21 and the floating diffusion FD. In the transfer transistor 22, the transfer line 26 is electrically connected to the gate. In the transfer transistor 22, based on the transfer signal TG transmitted from the transfer line 26 to the gate, the signal charge accumulated in the photodiode 21 is transferred to the floating diffusion FD.

[0119]

In the pixel transistor Tr, as shown in FIG. 7, the amplification transistor 23 is configured to amplify and output an electrical signal converted from charge to voltage in the floating diffusion FD. Specifically, as shown in FIG. 7, the gate of the amplifying transistor 23 is electrically connected to the floating diffusion FD. Further, the drain of the amplification transistor 23 is electrically connected to the power supply line Vdd, and the source thereof is electrically connected to the selection transistor 24. When the selection transistor 24 is selected to be in the ON state, the amplification transistor 23 is supplied with a constant current from the constant current source I and operates as a source follower. Therefore, in the amplification transistor 23, the selection signal is supplied to the selection transistor 24, whereby the electric signal converted from the charge to the voltage in the floating diffusion FD is amplified.

[0120]

In the pixel transistor Tr, as shown in FIG. 7, the selection transistor 24 is configured to output the electric signal output by the amplification transistor 23 to the vertical signal line 27 based on the selection signal. Specifically, as shown in FIG. 7, the selection transistor 24 has a gate connected to the address line 28 to which the selection signal is supplied. The selection transistor 24 is turned on when the selection signal is supplied, and outputs the output signal amplified by the amplification transistor 23 to the vertical signal line 27 as described above.

[0121]

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In the pixel transistor Tr, in the reset transistor 25, as shown in FIG. 7, the reset transistor 25 is configured to reset the gate potential of the amplification transistor 23. Specifically, as shown in FIG. 7, the gate of the reset transistor 25 is electrically connected to the reset line 29 to which the reset signal is supplied. In the reset transistor 25, the drain is electrically connected to the power supply line Vdd, and the source is electrically connected to the floating diffusion FD. The reset transistor 25 resets the gate potential of the amplification transistor 23 to the power supply voltage via the floating diffusion FD based on the reset signal transmitted from the reset line 29.

[0122]

FIG. 8 is a timing chart showing a control signal to be transmitted to the pixel transistor Tr of the pixel P when imaging is performed in the first embodiment.

[0123]

8A shows the selection signal SEL to be input to the gate of the selection transistor 24. In FIG.

(B) shows the reset signal RST input to the gate of the reset transistor 25. (C) shows the transfer signal TG input to the gate of the transfer transistor 22. (See FIG. 7).

[0124]

As shown in FIG. 8, when imaging is performed, the selection signal SEL is set to the high level at the first time point t 1, and the selection transistor 24 is turned on. Then, at the second time point t 2, the reset signal RST is set to the high level, and the reset transistor 25 is turned on. Thereby, the gate potential of the amplifying transistor 23 is reset (see FIG. 7).

[0125]

As shown in FIG. 8, at the third time point t 3, the reset signal RST is set to the low level, and the reset transistor 25 is turned off. Thereafter, a voltage corresponding to the reset level is read out to the column circuit 14 as an output signal (see FIGS. 2 and 7).

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[0126]

As shown in FIG. 8, at the fourth time point t 4, the transfer signal TG is set to the high level, and the transfer transistor 22 is turned on. As a result, the signal charge accumulated in the photodiode 21 is transferred to the floating diffusion FD (see FIG. 7).

[0127]

As shown in FIG. 8, at the fifth time point t 5, the transfer signal TG is set to the low level, and the transfer transistor 22 is turned off. Thereafter, a voltage of a signal level corresponding to the amount of the accumulated signal charge is read out to the column circuit 4 as an output signal (see FIGS. 2 and 7).

[0128]

In the column circuit 14, the signal of the reset level read out earlier and the signal of the signal level read out later are differentially processed to accumulate signals (see FIGS. 2 and 7).

[0129]

As a result, fixed pattern noise generated due to variations in Vth of each transistor provided for each pixel P is canceled.

[0130]

In the operation of driving the pixel P as described above, since the gates of the respective transistors 22, 24, and 25 are connected in units of rows composed of a plurality of pixels P arranged in the horizontal direction x, they are arranged in row units Are simultaneously performed on a plurality of pixels P.

[0131]

More specifically, it is sequentially selected in the vertical direction on a horizontal line (pixel row) basis by the selection signal supplied by the vertical drive circuit 13 described above.

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The transistors of each pixel P are controlled by various timing signals output from the timing generator 18.

As a result, the signal in each pixel is read out to the column circuit 14 for each column of pixels P through the vertical signal line 27 (see FIGS. 2 and 7).

[0132]
Then, the signals accumulated in the column circuit 14 are selected by the horizontal drive circuit 15 and sequentially output to the external output circuit 17 (see FIGS. 2 and 7).

[0133]
Then, the signal processing unit 44 carries out signal processing with the signal obtained by this imaging as raw data to generate a digital image (see FIG. 1).

[0134]
(F) About the Wiring Layer 111 In the solid-state imaging device 1, the wiring layer 111 includes, as shown in FIG. 3, a back surface (upper surface) on which the respective parts such as the color filter CF and the microlens ML are provided in the semiconductor substrate 101 Is provided on the opposite surface (lower surface).

[0135]

The wiring layer 111 includes a wiring 111 h and an insulating layer 111 z. In the insulating layer 111 z, a wiring 111 h is formed so as to be electrically connected to each element.

The wiring layer 111 is a so-called multilayer wiring layer, and is formed by alternately stacking an interlayer insulating film and a wiring 111 h constituting the insulating layer 111 z plural times.

Here, a plurality of wirings 111 h are stacked via an insulating layer 111 z so as to function as wirings such as the transfer line 26, the address line 28, the vertical signal line 27, the reset line

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29 and the like shown in FIG. 7 And is formed.

[0136]

In the wiring layer 111, a support substrate SS is provided on the surface opposite to the side on which the semiconductor substrate 101 is located.

For example, a substrate made of a silicon semiconductor having a thickness of several hundreds μm is provided as a support substrate SS.

[0137]
(B) Manufacturing Method A principal part of a manufacturing method for manufacturing the above-described solid-state imaging device 1 will be described.

[0138]
9 to 13 are diagrams showing a method for manufacturing a solid-state imaging device according to the first embodiment.

[0139]
Each figure shows a cross section similarly to FIG. 3.

[0140]
In the present embodiment, the steps (a) to (e) shown in each drawing are sequentially performed, and the solid-state imaging device 1 shown in FIG. 3 and the like is manufactured.

[0141]
Details of each process are sequentially shown.

[0142]
(A) Formation of Photodiodes 21 and the Like First, as shown in FIG. 9, photodiodes 21 and the like are formed.

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[0143]

Here, impurities are ion-implanted from the surface of the semiconductor substrate 101 made of a single crystal silicon semiconductor, so that each part such as the photodiode 21 is formed.

For example, after forming the p-type semiconductor region 101 pa over the entire surface of the semiconductor substrate 101, a p-type semiconductor region 101 pc having a higher impurity concentration than that is formed.

Then, an n-type semiconductor region 101 n is formed in a portion of the semiconductor substrate 101 where the photodiode 21 is to be formed.

[0144]

For example, each part is formed so as to have the following impurity concentration.

Impurity concentration of the p-type semiconductor region 101 pa: 5.0 × 10 <16> to 5.0 × 10 <17> cm <-3> Impurity concentration of the p-type semiconductor region 101 pc: 5.0 × 10 <17> to 5.0 × 10 < > cm <-3> Impurity concentration of n-type semiconductor region 101 n: 5.0 × 10 <15> to 5.0 × 10 <16> cm <-3>

[0145]

After forming the pixel transistor Tr (not shown in FIG. 7) on the surface of the semiconductor substrate 101, the wiring layer 111 is formed so as to cover the pixel transistor Tr.

Then, the supporting substrate SS is bonded to the surface of the wiring layer 111.

[0146]

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Thereafter, the semiconductor substrate 101 is thinned.

For example, it is preferable to perform thinning so as to satisfy the following conditions.

Thickness of semiconductor substrate 101 after thinning: 2 to 10 μ m Method: Chemical mechanical polishing (CMP) method (Otherwise, dry etching, wet etching is also acceptable.

Alternatively, a combination of CMP and dry etching or wet etching may be used.)

[0147]
Note that members such as the photodiode 21, the pixel transistor Tr, and the like are formed in the semiconductor layer of the SOI substrate (not shown), the wiring layer 111 and the supporting substrate SS are provided in the same manner as described above, and then thinning processing is performed Also good.

[0148]
(B) Formation of Trench TR Next, as shown in FIG. 10, a trench TR is formed.

[0149]
Here, in the semiconductor substrate 101, the trench TR is formed in the pixel separation portion 301 located between the plurality of pixels P.

[0150]

For example, after forming a mask (not shown) having a portion where a trench TR is to be formed on the back surface (upper surface) of the semiconductor substrate 101, the semiconductor substrate 101 is processed using the mask to form a trench TR .

For example, a dry etching process is performed on the semiconductor substrate 101 to form a trench TR.

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Then remove that mask.

[0151]

In the present embodiment, for example, it is preferable to form the trench TR so as to satisfy the following conditions.

· Width TH 1 on the lower surface side: 100 nm to 400 nm (When the width TH 1 is 100 nm or less, when burying the insulating film 311, probability of occurrence of defect may increase due to the self stress of the insulating film 311 itself. On the other hand, if the width TH 1 is too wide, the area of the formation region of the photodiode 21 decreases and the saturated electron amount decreases.) Width TH 2 on the upper surface side: 200 nm to 500 nm (The width TH 2 is determined by lithography resolution. The width YH 2 is a value in an exposure machine that uses, for example, KrF as a light source designation. Depth DT: 100 nm to 600 nm (Regions where color mixing tends to occur are distributed at positions where the depth DT from the light receiving surface JS is 100 nm to 500 nm, and this portion is divided by the trench TR to suppress color mixing it can.)

[0152]
(C) Formation of First Insulating Film 311 A Next, as shown in FIG. 11, the first insulating film 311 A is formed.

[0153]

Here, as shown in FIG. 11, the first insulating film 311 A is formed so as to cover the side surface and the bottom surface inside the trench TR in the pixel separation portion 301.

At the same time, the first insulating film 311 A is formed so as to cover the back surface (upper surface) of the semiconductor substrate 101.

[0154]

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For example, it is preferable to form the first insulating film 311 </ b> A under the following conditions. Material: HfO 2 (refractive index n = 2.1), TaO (refractive index n = 2.2), ZrO 2 (refractive index = 2.3), Al 2 O 3 (refractive index n = 2.1) Thickness: 40 nm To 60 nm Forming method: atomic layer deposition (ALD) method, sputtering method, metalorganic vapor phase CVD method (MOCVD method)

[0155]
(D) Formation of Second Insulating Film 311 B Next, as shown in FIG. 12, a second insulating film 311 B is formed.

[0156]

Here, as shown in FIG. 12, the second insulating film 311 B is formed so as to cover the side surface and the bottom surface of the trench TR via the first insulating film 311 A inside the trench TR.

At the same time, the second insulating film 311 B is formed so as to cover the back surface (upper surface) of the semiconductor substrate 101 with the first insulating film 311 A interposed therebetween.

[0157]

For the second insulating film 311 </ b> B, for example, it is preferable to form the second insulating film 311 </ b> B under the following conditions. Material: SiO 2 (refractive index n = 1.5), SiOC (refractive index n = 1.1) Thickness: 50 nm to 500 nm Method of formation: sputtering method, CVD method

[0158]
(E) Formation of light shielding layer 313 Next, as shown in FIG. 13, a light shielding layer 313 is formed.

[0159]

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Here, as shown in FIG. 13, the light shielding layer 313 is provided in the pixel separation portion 301.

[0160]
In the present embodiment, the light shielding layer 313 is provided so that the first light shielding portion 313 A and the second light shielding portion 313 B are integrated.

[0161]
Specifically, the first light shielding portion 313 A fills the inside of the trench TR with the insulating layer 311 interposed therebetween, and the second light shielding portion 313 B covers the back surface (upper surface) of the semiconductor substrate 101 via the insulating layer 311 , A light shielding layer 313 is formed.

[0162]

Regarding formation of the light shielding layer 313, first, a light shielding material that shields light is embedded in the trench TR with the insulating layer 311 interposed therebetween, thereby forming the first light shielding portion 313 A.

At the same time, a light shielding material for shielding light is formed so as to cover the back surface (upper surface) of the semiconductor substrate 101.

Then, the portion covering the back surface (upper surface) of the semiconductor substrate 101 is patterned to form the second light shielding portion 313B.

[0163]

For example, the light shielding layer 313 is formed under the following conditions.

Metal material such as Ti, Ti, W, Al and the like. The width HA 1 on the lower surface side of the first light-shielding portion 313 A: 0 nm to 50 nm (there is no limitation as to the width, depending on the shape of the trench TR and the film thickness of the insulating film 311 It is

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determined.

) Width HA 2 on the upper surface side of the first light shielding portion 313 A: 50 to 200 nm (there is no limitation on the width, and it is determined by the shape of the trench TR and the film thickness of the insulating film 311.) - Depth DA of the first light shielding portion 313 A: 100 nm to 300 nm (Improvement in optical characteristics is prominent because the first light shielding portion 313 A enters the wiring layer 111 side from the upper surface of the semiconductor substrate 101 by 50 nm or more . The width HB of the second light shielding portion 313B is 200 nm to 300 nm the thickness TB of the second light shielding portion 313B is 100 nm to 500 nm (optimized by the metal material used for the light shielding layer 313 and the film forming method). As an index, this thickness is set so that the light attenuation factor at 600 nm to 800 nm becomes -80 dB.)

[0164]
As shown in FIGS. 5 and 6, with respect to the second light shielding portion 313 B, the central portion (in the case of (a)) of the pixel region PA (see FIG. 2) and the peripheral portion ((b)) Are formed so as to be at different positions from each other.

[0165]

Here, in the peripheral portion of the pixel region PA, the center axis 313 BCX of the second light shielding portion 313 B is located closer to the peripheral side of the pixel region PA (see FIG. 2) than the central axis 301 CX of the pixel separation portion 301.

(Right side in FIG. 5 (b)), the second light shielding portion 313 B is formed. That is, the second light shielding portion 313 </ b> B is formed so that the center axis 313 </ b> BCX of the second light shielding portion 313 </ b> B and the central axis 301 </ b> CX of the pixel separation portion 301 are separated by a predetermined shift amount Dx in the horizontal direction x.

[0166]
As described above, the second light shielding portion 313B is formed by performing so-called "pupil correction".

[0167]

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For example, the shift amount Dx is determined by the size of the pixel P and the distance between the microlens ML and the light receiving surface JS.

Calculation of the shift amount Dx is performed, for example, using a ray tracing method or FDTD method.

[0168]
(F) Formation of Color Filter CF and Microlens ML Next, as shown in FIG. 3, the respective members of the color filter CF and microlens ML are formed.

[0169]
Here, the planarization film HT is formed on the back surface (upper surface) of the semiconductor substrate 101 provided with the light shielding layer 313.

[0170]
Thereafter, a color filter CF is formed.

[0171]

For example, a coating solution containing a dye such as a pigment or a dye and a photosensitive resin is coated by a coating method such as a spin coating method to form a coating film, and the coating film is patterned by lithography technique.

In this way, by forming the respective filter layers CFR, CFG, CFB, the color filter CF is provided.

[0172]
Thereafter, a microlens ML is provided on the upper surface of the color filter CF.

[0173]

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For example, after patterning the photosensitive resin film by photolithography technology, it is deformed into a lens shape by reflow processing, thereby forming the microlens ML.

In addition to this, after forming a lens-shaped resist pattern on the lens material film, the microlens ML may be formed by performing an etch back process using the resist pattern as a mask.

[0174]
By successively carrying out each step in this manner, a CMOS type image sensor of "back side irradiation type" is completed.

[0175]

(C) Summary As described above, in the present embodiment, the pixel separation unit 301 is provided inside the semiconductor substrate 101 so as to be interposed between the plurality of pixels P in the pixel area PA.

In the pixel separation portion 301, a first light shielding portion 313 A is provided inside a trench TR formed on the back surface (upper surface) side of the semiconductor substrate 101.

At the same time, a second light shielding portion 313 B is provided on the back surface (upper surface) of the semiconductor substrate 101.

Here, in the periphery of the center of the pixel region PA, the center of the second light shielding part 313 </ b> B of the second light shielding part 313 </ b> B shifts more toward the periphery of the pixel region PA than the center of the pixel separation part 301 As shown in FIG.

[0176]
That is, in the present embodiment, "pupil correction" is performed for the second light shielding portion 313B.

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[0177]
FIG. 14 is a cross-sectional view showing how the incident light enters the solid-state imaging device in the first embodiment.

[0178]

In FIG. 14, as with FIG. 5 (b), the peripheral portion of the pixel region PA (see FIGS. 1 and 2) is shown.

In FIG. 14, (a) shows a case where "pupil correction" is not performed on the second light shielding portion 313 B, unlike the present embodiment.

On the other hand, (b) is the case of the present embodiment, and shows the case where "pupil correction" is performed.

[0179]

As shown in FIG. 14, in the peripheral portion (see FIGS. 1 and 2) of the pixel area PA, no light beam is incident perpendicularly to the back surface of the semiconductor substrate 101, and the inclined light beam H 2 is incident. Here, the light ray H 2 is inclined so as to travel from the center of the pixel region PA to the periphery when heading toward the back surface of the semiconductor substrate 101.

[0180]

14 (a) and 14 (b), the light vector L1 of the light beam H2 incident on the inclined surface is reflected by the first light-shielding portion 313A of the light-shielding layer 313 after entering the insulating layer 311. As shown in FIG. Then, the reflected light vector L 1 is incident on the photodiode 21 and photoelectrically converted.

[0181]

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In addition, among the light beams H 2 incident at an inclination, the light vectors L 2 and L 3 are shielded by the second light shielding portion 313 B of the light shielding layer 313 as shown in FIGS. 14 (a) and 14 (b). Among them, the light vector L <b> 2 is reflected by the side surface of the second light shielding portion 313 </ b> B of the light shielding layer 313.

[0182]

At this time, as shown in FIG. 14 (a), when "pupil correction" is not performed for the second light shielding portion 313 B, the distance from the reflected portion to the back surface of the semiconductor substrate 101 is long , It attenuates before being photoelectrically converted.

[0183]

On the other hand, as shown in FIG. 14 (b), when "pupil correction" is performed on the second light shielding portion 313 B, the distance from the reflected portion to the back surface of the semiconductor substrate 101 is short Is not attenuated, enters the photodiode 21, and is photoelectrically converted.

In this manner, when "pupil correction" is performed, light can reach the photodiode 21 efficiently. Therefore, the image quality of the captured image can be improved.

[0184]

As shown in FIG. 14 (a), the light vector L 4 among the light beams H 2 incident on the inclined surface is such that when "pupil correction" is not performed on the second light shielding portion 313 B, the light shielding portion 313 B And is incident on the photodiode 21 of the adjacent pixel P. For this reason, "mixed color" or the like occurs, and the image quality of the captured image may be deteriorated in some cases.

[0185]

However, as shown in FIG. 14 (b), when "pupil correction" is performed on the second light

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shielding portion 313 B, the light vector L 4 is shielded by the second light shielding portion 313 B and the photodiode 21 . Therefore, in the present embodiment, it is possible to suppress the occurrence of "mixed color" and the like and to improve the image quality of the captured image.

[0186]
Therefore, in the present embodiment, the image quality of the captured image can be improved.

[0187]

In the present embodiment, the first insulating film 311 </ b> A constituting the insulating layer 311 is provided so as to cover the inner surface of the trench TR.

A second insulating film 311 </ b> B is provided so as to cover the inner surface of the trench TR with the first insulating film 311 </ b> A interposed therebetween. The first insulating film 311 </ b> A is formed using a material having a refractive index between the semiconductor substrate 101 and the second insulating film 311 </ b> B. Therefore, at the interface between the semiconductor substrate 101 and the trench TR, since the difference in refractive index is small, reflection of light at the interface can be suppressed. Therefore, in the ear embodiments, the effect of suppressing the surface reflectance can be more suitably exhibited.

[0188]

< 2 . Embodiment 2> (A) Device Configuration, etc. FIG. 15 is a diagram showing a main part of a solid-state imaging device in Embodiment 2. In FIG.

[0189]

FIG. 15 shows a pixel separation section 301 between pixels P arranged in the peripheral portion of the pixel area PA shown in FIG. 2 as in FIG. 5 and FIG. 6 (b), showing the X 1 S - X 2 S portion ing. FIG. 15A is a cross-sectional view of the pixel separation unit 301, and FIG. 15B is a top view of the pixel separation unit 301.

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[0190]

As shown in FIG. 15, in this embodiment, as can be seen from FIGS. 5 and 6 (b), the position of the second light shielding portion 313 B of the light shielding layer 313 in the peripheral portion of the pixel region PA is shifted Which is different from the first embodiment. Except for this point and related points, the present embodiment is similar to the first embodiment. For this reason, descriptions of overlapping parts are omitted as appropriate.

[0191]

As shown in FIG. 15, the first light shielding portion 313 A of the light shielding layer 313 is formed so as to bury the inside of the trench TR via the insulating layer 311 as in the case of the first embodiment.

[0192]

As shown in FIG. 15, the second light shielding portion 313 </ b> B of the light shielding layer 313 is formed above the back surface (upper surface) of the semiconductor substrate 101 with the insulating layer 311 interposed therebetween.

[0193]

2), the center axis 313BCX of the second light shielding portion 313B is located closer to the periphery side of the pixel area PA (see FIG. 2) than the center axis 301CX of the pixel separation portion 301. In addition, in the peripheral portion of the pixel area PA (see FIG.

And the second light shielding portion 313 </ b> B is formed so as to shift to the right side in FIG. 5).

That is, so-called "pupil correction" is performed for the second light shielding portion 313B.

[0194]

However, in the present embodiment, as shown in FIG. 15, the shift amount Dx between the central axis 313 BCX of the second light shielding portion 313 B and the central axis 301 CX of the pixel separation portion 301 is larger than that in the first embodiment The second light

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shielding portion 313 </ b> B is formed.

[0195]
Specifically, in the case of the first embodiment, the second light shielding portion 313B is formed so as to be positioned within the range of the portion where the upper surface of the trench TR is located on the back surface (upper surface) of the semiconductor substrate 101 (See Fig. 5, Fig. 6 (b) etc).

[0196]

On the other hand, in the present embodiment, as shown in FIGS. 15A and 15B, the second light shielding portion 313 </ b> B is formed such that the range of the portion where the upper surface of the trench TR is located on the back surface (upper surface) of the semiconductor substrate 101 , It is formed so as to be located in a portion other than the range.

That is, the second light shielding portion 313 </ b> B is formed such that a predetermined shift amount Gx is shifted from the range of the portion where the upper surface of the trench TR is located on the back surface (upper surface) of the semiconductor substrate 101.

[0197]
Thus, in the present embodiment, the light shielding layer 313 is formed so that the upper surface of the first light shielding portion 313 </ b> A does not cover with the second light shielding portion 313 </ b> B but includes a portion where the light is incident upon being exposed.

[0198]
(B) Summary As described above, in the present embodiment, in the second light shielding portion 313B, the center of the second light shielding portion 313B is located closer to the center of the pixel separation portion 301 than the center of the pixel area PA , And is formed so as to be shifted to the peripheral side of the pixel area PA more.

[0199]
That is, in the present embodiment, "pupil correction" is performed for the second light shielding portion 313B.

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[0200]
Therefore, in the present embodiment, as in the first embodiment, the image quality of the captured image can be improved.

[0201]
In particular, in the present embodiment, in order to make the shift amount Dx between the center axis 313 BCX of the second light shielding portion 313 </ b> B and the central axis 301 </ b> CX of the pixel separation portion 301 larger than that in the first embodiment, A light shielding portion 313B is formed (see FIG. 15).

[0202]

Therefore, in the present embodiment, the light can reach the photodiode 21 more efficiently than in the case of the first embodiment.

Further, occurrence of "mixed color" and the like can be more effectively suppressed.

[0203]
FIG. 16 is a cross-sectional view showing how incident light enters the solid-state imaging device in the second embodiment.

[0204]
FIG. 16 shows a peripheral portion (see FIGS. 1 and 2) of the pixel area PA similarly to FIG. 15 (a).

[0205]

As shown in FIG. 16, in the peripheral portion (see FIGS. 1 and 2) of the pixel region PA, no light beam is incident perpendicularly to the back surface of the semiconductor substrate 101, and the inclined light beam H 2 is incident.

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Here, the light ray H 2 is inclined so as to travel from the center of the pixel region PA to the periphery when heading toward the back surface of the semiconductor substrate 101.

[0206]

As shown in FIG. 16, the light vector L 1 out of the inclined incident light H 2 is reflected by the first light shielding portion 313 A of the light shielding layer 313 after entering the insulating layer 311.

Then, the reflected light vector L 1 is incident on the photodiode 21 and photoelectrically converted.

[0207]

The light vectors L2 and L3 among the light beams H2 which are incident in an inclined state are blocked by the second light shielding portion 313B of the light shielding layer 313, as shown in FIG.

Among them, the light vector L 3 is reflected by the side surface of the second light shielding portion 313 B of the light shielding layer 313.

Then, it enters the photodiode 21 and is photoelectrically converted.

Therefore, in the present embodiment, light can reach the photodiode 21 efficiently.

Therefore, the image quality of the captured image can be improved.

[0208]

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The light vector L4 among the light beams H2 incident in an inclined state is shielded by the second light shielding portion 313B and does not enter the photodiode 21 of the adjacent pixel P as shown in FIG.

In the present embodiment, "pupil correction" is performed so that the second light shielding portion 313 </ b> B shifts to the peripheral side of the pixel region PA than in the first embodiment. Therefore, in the present embodiment, it is possible to more effectively suppress the occurrence of "mixed color" and the like and to improve the image quality of the captured image.

[0209]

＜3． Embodiment 3 (A) Device Configuration and the Like FIG. 17 is a diagram showing a main part of a solid-state imaging device in Embodiment 3.

[0210]

FIG. 17 shows a pixel separating portion 301 between pixels P arranged in the peripheral portion of the pixel area PA shown in FIG. 2, similarly to FIG. 15, and shows the X 1 S - X 2 S portion. FIG. 17A is a cross-sectional view of the pixel separation unit 301, and FIG. 17B is a top view of the pixel separation unit 301.

[0211]

As shown in FIG. 17, in the present embodiment, the width HBS of the second light shielding portion 313 B of the light shielding layer 313 is different from that in the second embodiment as can be seen from comparison with FIG. 15. Except for this point and related points, the present embodiment is similar to the second embodiment. For this reason, descriptions of overlapping parts are omitted as appropriate.

[0212]

As shown in FIG. 17, the second light shielding portion 313 B of the light shielding layer 313 is formed above the back surface (upper surface) of the semiconductor substrate 101 via the

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insulating layer 311 as in the second embodiment There.

[0213]

2), the center axis 313BCX of the second light shielding portion 313B is located closer to the periphery side of the pixel area PA (see FIG. 2) than the center axis 301CX of the pixel separation portion 301. In addition, in the peripheral portion of the pixel area PA (see FIG.

And the second light shielding portion 313 </ b> B is formed so as to shift to the right side in FIG. 17). That is, so-called "pupil correction" is performed for the second light shielding portion 313B.

[0214]
Furthermore, in the present embodiment, the shift amount Dx between the center axis 313 BCX of the second light shielding portion 313 </ b> B and the central axis 301 </ b> CX of the pixel separation portion 301 is larger than that in the first embodiment The second light shielding portion 313 </ b> B is formed.

[0215]
However, in the present embodiment, unlike the second embodiment, the second light shielding portion 313 </ b> B is formed so as to be located within the range of the portion where the upper surface of the trench TR is located on the back surface (upper surface) of the semiconductor substrate 101 ing.

[0216]

Further, as shown in FIG. 17, the second light shielding portion 313B is formed such that the width HBS is narrower than the central portion in the peripheral portion of the pixel area PA.

The second light shielding portion 313 </ b> B is formed with a width HB similar to that in the first embodiment (see FIG. 5 (a)) in the center portion of the pixel region PA.

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[0217]
Thus, in the light-shielding layer 313 of the present embodiment, the upper surface of the first light-shielding portion 313 A is formed not to be covered with the second light-shielding portion 313 B but including the exposed portion as in the second embodiment .

[0218]
(B) Summary As described above, in the present embodiment, in the second light shielding portion 313B, the center of the second light shielding portion 313B is located closer to the center of the pixel separation portion 301 than the center of the pixel area PA , And is formed so as to be shifted to the peripheral side of the pixel area PA more.

[0219]
That is, in the present embodiment, "pupil correction" is performed for the second light shielding portion 313B.

[0220]
Therefore, in the present embodiment, as in the second embodiment, the image quality of the captured image can be improved.

[0221]

In the case of the second embodiment, as shown in FIG. 15A, in the peripheral portion of the pixel region PA, the second light shielding portion 313 B is located at a position other than the range of the portion where the upper surface of the trench TR is located are doing.

Therefore, in the second embodiment, the effective light-shielding width EH is a value obtained by adding the width HB of the second light-shielding portion 313 </ b> B and the width of the portion where the upper surface of the first light-shielding portion 313 </ b> A is exposed.

[0222]

On the other hand, in the present embodiment, as shown in FIG. 17, in the present embodiment, the second light shielding portion 313 </ b> B is formed such that a portion where the upper

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surface of the trench TR is located on the back surface (upper surface) of the semiconductor substrate 101 in the peripheral portion of the pixel region PA Of the outer circumference of the inner circumferential surface of the casing.

In the peripheral portion of the pixel region PA, the second light shielding portion 313B is formed so that the width HBS is narrower than the central portion.

Therefore, in the present embodiment, the effective light shielding width EH is a value obtained by adding the width HBS of the second light shielding portion 313 </ b> B and the width of the portion where the upper surface of the first light shielding portion 313 </ b> A is exposed.

[0223]

In this manner, in the peripheral portion of the pixel region PA, the width HBS of the second light shielding portion 313 </ b> B in the present embodiment is narrower than the width HB in the second embodiment.

Therefore, the effective light-shielding width EH is narrower in the case of this embodiment (see FIG. 17 (a)) than in the case of the second embodiment (see FIG. 15 (a)).

[0224]

In the case where the effective light shielding width EH is wide as in the case of the second embodiment, a decrease in sensitivity occurs.

Since this decrease in sensitivity occurs continuously in the pixel area PA, "shading" occurs in the captured image, which may cause deterioration in image quality. However, in the present embodiment, as described above, since the effective light-shielding width EH is narrower than that in the second embodiment, occurrence of "shading" can be suppressed and the image quality can be improved.

[0225]

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FIG. 18 is a cross-sectional view showing how incident light enters the solid-state imaging device in the third embodiment.

[0226]
FIG. 18 shows a peripheral portion (see FIGS. 1 and 2) of the pixel area PA similarly to FIG. 17 (a).

[0227]

As shown in FIG. 18, in the peripheral portion (see FIGS. 1 and 2) of the pixel region PA, when the width HBS of the second light shielding portion 313 B is narrow, the light L 5 due to the rounding advances to another pixel There are cases.

When the light reflected by the second light shielding portion 313 B enters into the second insulating film 311 B having a low refractive index, the wraparound occurs.

Then, since the first light-shielding portion 313 A and the second light-shielding portion 311 B surrounded by the first light-shielding portion 311 A function as an optical waveguide, there is a case where the light L 5 that has traveled around reaches other pixels P is there.

[0228]
For this reason, it is conceivable that the occurrence of "color mixture" increases due to this light L 5.

[0229]

However, in the present embodiment, since the first light shielding portion 313 </ b> A is provided in the trench TR, the first light shielding portion 313 </ b> A shields the light L <b> 5 and does not enter the other pixels P.

Therefore, in the present embodiment, the occurrence of "color mixing" can be effectively suppressed.

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[0230]

< 4 . Embodiment 4> (A) Apparatus Configuration, etc. FIG. 19 and FIG. 20 are diagrams showing essential parts of a solid-state imaging device in Embodiment 4. FIG.

[0231]

FIG. 19 is a cross-sectional view of the pixel separation section 301 similarly to FIG. 5. FIG. 20 is a top view of the pixel separating unit 301 similarly to FIG. 6. In FIGS. 19 and 20, (a) shows the pixel separation section 301 between the pixels P arranged in the central portion of the pixel area PA shown in FIG. 2, and shows the X 1 C - X 2 C section. On the other hand, (b) shows a pixel separation section 301 between pixels P arranged in the peripheral part of the pixel region PA shown in FIG. 2, and shows the X 1 S - X 2 S part.

[0232]

As shown in FIG. 19 and FIG. 20, in the present embodiment, as can be seen from comparison with FIGS. 5 and 6, a pixel separation diffusion layer 101 pb is further provided. Except for this point and related points, the present embodiment is similar to the first embodiment. For this reason, descriptions of overlapping parts are omitted as appropriate.

[0233]

As shown in FIGS. 19 and 20, the pixel separation diffusion layer 101 pb is provided in the pixel separation section 301.

[0234]

The pixel separation diffusion layer 101 pb is formed by diffusing an impurity of a conductivity type different from that of the n type semiconductor region 101 n that accumulates the signal charge in the photodiode 21.

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Specifically, the pixel separation diffusion layer 101 pb is formed by ion-implanting a p-type impurity into the semiconductor substrate 101, and the pixel separation diffusion layer 101 pb of the photodiodes 21 (see FIG. 3) provided in each of the plurality of pixels P And electrically separates them.

[0235]

For example, the pixel separation diffusion layer 101 pb is formed under the following conditions. Impurity concentration: 5 × 10 <16> to 5 × 10 <18> cm <-3>

[0236]

As shown in FIGS. 19 and 20, in the center portion and the peripheral portion of the pixel area PA (see FIG. 2), the central axis in the horizontal direction x of the pixel separation diffusion layer 101 pb is located in the horizontal direction x of the pixel separation unit 301 And is formed to coincide with the center axis 301CX. Although not shown, in the vertical direction y, the pixel separation diffusion layer 101 pb is also formed so that the central axis in the vertical direction y coincides with the central axis in the vertical direction y of the pixel separation section 301.

[0237]
As in the first embodiment, a trench TR is provided in the semiconductor substrate 101 provided with the pixel separation diffusion layer 101 pb, and the insulating layer 311 and the light shielding layer 313 are provided inside the trench TR .

[0238]
That is, as shown in FIGS. 19 and 20, the second light-shielding portion 313 B is formed so that the center portion (in the case of (a)) of the pixel region PA (see FIG. 2) and the peripheral portion And in the case of FIG.

[0239]
(B) Summary As described above, in the present embodiment, in the second light shielding portion 313B, the center of the second light shielding portion 313B is located closer to the center of the pixel separation portion 301 than the center of the pixel area PA , And is formed so as to

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be shifted to the peripheral side of the pixel area PA more.

[0240]
That is, in the present embodiment, "pupil correction" is performed for the second light shielding portion 313B.

[0241]
In addition, since the pixel separation diffusion layer 101 pb is provided, separation between the plurality of pixels P can be suitably expressed.

[0242]
Therefore, in the present embodiment, as in the first embodiment, the image quality of the captured image can be improved.

[0243]

In the present embodiment, the case where the trench TR is provided in the semiconductor substrate 101 similarly to the first embodiment, and the insulating layer 311 and the light shielding layer 313 are provided inside the trench TR has been described, but the present invention is not limited to this.

As in the second and third embodiments, the light shielding layer 313 and the like may be formed.

[0244]

< 5.

FIFTH EMBODIMENT (A) Device Configuration, etc. FIG. 21 is a diagram showing a main part of a solid-state imaging device according to a fifth embodiment.

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[0245]

FIG. 21 shows a pixel separation unit 301 between pixels P arranged in the peripheral portion of the pixel area PA shown in FIG. 2, similar to FIG. 19 and FIG. 20 (b), showing the X 1 S - X 2 S portion ing.

FIG. 21A is a cross-sectional view of the pixel separation unit 301, and FIG. 21B is a top view of the pixel separation unit 301.

[0246]

As shown in FIG. 21, in the present embodiment, as can be seen from FIG. 19 and FIG. 20 (b), in the peripheral portion of the pixel region PA, the trench TR, the insulating layer 311, the light shielding layer 313 1 The position of the light shielding portion 313 A is different from that of the fourth embodiment.

Except for this point and related points, the present embodiment is similar to the fourth embodiment.

For this reason, descriptions of overlapping parts are omitted as appropriate.

[0247]
As shown in FIG. 21, the pixel separation section 301 is provided with a pixel separation diffusion layer 101 pb as in the fourth embodiment.

[0248]

In the pixel separation section 301, as shown in FIG. 21, a trench TR is provided on the back surface (upper surface) side of the semiconductor substrate 101.

In the pixel separation portion 301, the insulating layer 311 and the light shielding layer 313 are

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provided inside the trench TR.

[0249]
Specifically, as shown in FIG. 21, in the trench TR, unlike in the fourth embodiment, in the peripheral portion of the pixel region PA (see FIG. 2), the center axis 313 ACX in the horizontal direction x is divided by the pixel separation portion 301 Does not coincide with the center axis 301CX in the horizontal direction x of

[0250]

Here, as shown in FIG. 21, the center axis 313 ACX of the trench TR is located closer to the peripheral side of the pixel region PA (see FIG. 2) than the center axis 301 CX of the pixel separation portion 301.

The right side in FIG. 21), the trench TR is formed.

That is, the trench TR is formed so that the center axis 313 ACX of the trench TR and the center axis 301 CX of the pixel separation portion 301 are separated by a predetermined shift amount Dx in the horizontal direction x.

[0251]
In the present embodiment, the trench TR is formed in a portion where the pixel separation diffusion layer 101 pb is formed.

[0252]
As shown in FIG. 21, an insulating layer 311 is provided in the same manner as in the fourth embodiment so as to cover the inner surface of the trench TR.

[0253]

Here, as shown in FIG. 21, since the trench TR is shifted in the peripheral portion of the pixel region PA, the insulating layer 311 is also provided in a shifted position similarly to this.

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That is, the center axis 313 ACX of the insulating layer 311 in the trench TR is located closer to the periphery side (see FIG. 2) of the pixel region PA than the center axis 301 CX of the pixel separation portion 301.

An insulating layer 311 is formed so as to shift to the right side in FIG. 21).

[0254]
Then, as shown in FIG. 21, a light shielding layer 313 is provided so as to bury the inside of the trench TR covered with the insulating film 311.

[0255]
Here, the first light-shielding portion 313 A of the light-shielding layer 313 is different from the central portion (see FIG. 19A) of the pixel region PA (see FIG. 2) and the peripheral portion And in the case of FIG. 21 (a)) are formed at different positions.

[0256]

Specifically, as shown in FIG. 21, in the peripheral portion of the pixel region PA (see FIG. 2), the first light shielding portion 313 A is arranged such that the center axis 313 ACX in the horizontal direction x is shifted in the horizontal direction x of the pixel separation portion 301 And does not coincide with the center axis 301CX.

The central axis 313 ACX of the first light shielding portion 313 A is located closer to the peripheral side of the pixel region PA (see FIG. 2) than the central axis 301 CX of the pixel separation portion 301.

And the first light shielding portion 313 </ b> A is formed so as to shift to the right side in FIG. 21). That is, the first light shielding portion 313 A is formed so that the center axis 313 ACX of the first light shielding portion 313 A and the center axis 301 CX of the pixel separation portion 301 are separated by a predetermined shift amount Dx in the horizontal direction x .

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[0257]

The second light shielding portion 313 </ b> B of the light shielding layer 313 is formed such that the center portion (see FIG. 19A) of the pixel area PA (see FIG. 2) and the peripheral portion And in the case of FIG. 21 (a)) are formed at different positions. Here, the center axis 313 BCX of the second light shielding portion 313 B is located closer to the periphery side (see FIG. 2) of the pixel region PA than the center axis 301 CX of the pixel separation portion 301. And the first light shielding portion 313 </ b> A is formed so as to shift to the right side in FIG. 21). That is, the second light shielding portion 313 B is formed so that the center axis 313 BCX of the second light shielding portion 313 B and the center axis 301 CX of the pixel separation portion 301 are separated by a predetermined shift amount Dx in the horizontal direction x .

[0258]

As described above, in the present embodiment, so-called "pupil correction" is performed for both of the first light shielding portion 313 A and the second light shielding portion 313 B constituting the trench TR, the insulating layer 311, and the light shielding layer 313 . Here, in each pixel separating section 301, the light shielding layer 313 is formed so that the central axis 313 ACX of the first light shielding section 313 A and the central axis 313 BCX of the second light shielding section 313 B coincide with each other.

[0259]

In the present embodiment, the pixel region PA is divided into a central part and a peripheral part thereof, and in the central part of the pixel region PA, as shown in FIGS. 19 and 20 (a), each part such as the light shielding layer 313 is provided ing. On the other hand, in the peripheral portion of the pixel region PA, as shown in FIGS. 21A and 21B, various portions such as the light shielding layer 313 are provided.

[0260]

Besides this, with respect to each portion such as the light-shielding layer 313, the shift amount Dx between the center axes 313 ACX, 313 BCX of the respective portions and the central axis 301 CX of the pixel separation portion 301 along the direction from the center of the pixel area PA toward the periphery May be increased.

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[0261]

Specifically, with respect to the trench TR, the first light shielding portion 313 A, and the second light shielding portion 313 B provided in each of the pixel separation portions 301 between the plurality of pixels P arranged in the horizontal direction x, the pitch in the horizontal direction x thereof Is formed so as to be wider than the pitch of the pixel separation section 301.

Further, with respect to the trench TR, the first light-shielding portion 313 A, and the second light-shielding portion 313 B provided in each pixel separation portion 301 between the plurality of pixels P arranged in the vertical direction y, the pitch in the vertical direction y of the pixel separation portion 301 as shown in FIG.

[0262]

That is, with respect to the pixel separation portion 301 and the trench TR provided between the pair of pixels P in the pixel region PA, the trenches TR are formed so as to be aligned with the pixel region PA at a wider pitch than the pixel separation portion 301 . Further, with respect to the pixel separating portion 301 and the first light shielding portion 313 A provided between the pair of pixels P in the pixel region PA, the first light shielding portion 313 A has a wider pitch than the pixel separating portion 301 with the pixel area PA As shown in FIG. Further, with respect to the pixel separating portion 301 and the second light shielding portion 313 </ b> B provided between the pair of pixels P in the pixel area PA, the second light shielding portion 313 </ b> B has a wider pitch than the pixel separating portion 301, Formed to line up with PA. Further, the trench TR, the first light shielding portion 313 A, and the second light shielding portion 313 B are formed to be arranged at the same pitch in the pixel region PA.

[0263]

(B) Summary As described above, in the present embodiment, in the second light shielding portion 313B, the center of the second light shielding portion 313B is located closer to the center of the pixel separation portion 301 than the center of the pixel area PA , And is formed so as to be shifted to the peripheral side of the pixel area PA more.

[0264]

Therefore, in the present embodiment, as in the case of the fourth embodiment, the image quality

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of the captured image can be improved.

[0265]
In addition, in the present embodiment, so-called "pupil correction" is also performed for the trench TR, the insulating layer 311, and the first light shielding portion 313 A configuring the light shielding layer 313.

[0266]

In the case where the width of the second light shielding portion 313 B is narrowed in the peripheral portion of the pixel region PA as in the third embodiment (see FIG. 17), processing of the second light shielding portion 313 B may not be easy in some cases.

However, in the present embodiment, since the structure of the trench TR, the insulating layer 311, and the light shielding layer 313 is the same in the entire pixel region PA and the width of the second light shielding portion 313 B is not narrow, it is preferable to perform processing it can.

[0267]

In addition, in this embodiment, the trench TR is formed in the portion where the pixel separation diffusion layer 101 pb is formed.

For this reason, "pupil correction" can be performed without changing the sensitivity or the number of saturated electrons.

[0268]

＜6.

Sixth Embodiment (A) Device Configuration and the Like FIG. 22 is a diagram showing a main

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part of a solid-state imaging device according to a sixth embodiment.

[0269]

22, similarly to FIG. 21, the pixel separating unit 301 between the pixels P arranged in the peripheral portion of the pixel area PA shown in FIG. 2 and showing the X 1 S - X 2 S portion. FIG. 22A is a cross-sectional view of the pixel separation unit 301, and FIG. 22B is a top view of the pixel separation unit 301.

[0270]

As shown in FIG. 22, in this embodiment, as can be seen from comparison with FIG. 21, the position of the second light shielding portion 313 B of the light shielding layer 313 in the peripheral portion of the pixel region PA is different from that in the fifth embodiment. Except for this point and related points, the present embodiment is similar to the fifth embodiment. For this reason, descriptions of overlapping parts are omitted as appropriate.

[0271]
As shown in FIG. 22, the first light shielding portion 313 A of the light shielding layer 313 is formed so as to fill the inside of the trench TR with the insulating layer 311 interposed therebetween in the same manner as in the case of Embodiment 5 (see FIG. 21) And is formed.

[0272]

Specifically, in the peripheral portion of the pixel region PA (see FIG. 2), the central axis 313 ACX of the first light shielding portion 313 A is located closer to the peripheral side of the pixel region PA (see FIG. 2 .

And the first light shielding portion 313 </ b> A is formed so as to shift to the right side in FIG. 21). That is, the first light shielding portion 313 A is formed so that the center axis 313 ACX of the first light shielding portion 313 A and the center axis 301 CX of the pixel separation portion 301 are separated by a predetermined shift amount Dx in the horizontal direction x .

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[0273]
Further, as shown in FIG. 22, the second light shielding portion 313 </ b> B is formed above the back surface (upper surface) of the semiconductor substrate 101 with the insulating layer 311 interposed therebetween.

[0274]

2), the center axis 313BCX of the second light shielding portion 313B is located closer to the periphery side of the pixel area PA (see FIG. 2) than the center axis 301CX of the pixel separation portion 301 .

And the second light shielding portion 313 </ b> B is formed so as to shift to the right side in FIG. 21). That is, the second light shielding portion 313B is formed so that the center axis 313BCX of the second light shielding portion 313B and the center axis 301CX of the pixel separation portion 301 are separated by a predetermined shift amount Dxb in the horizontal direction x .

[0275]

In the present embodiment, as shown in FIG. 22, a second light shielding portion 313 B is formed so that the shift amount Dxb is larger than in the case of the fifth embodiment (see FIG. 21). That is, as shown in FIG. 22, the second light shielding portion 313B is formed so that the shift amount Dxb of the second light shielding portion 313B is larger than the shift amount Dx of the first light shielding portion 313A.

[0276]
(B) Summary As described above, in the present embodiment, so-called "pupil correction" is performed on the first light shielding portion 313 A and the second light shielding portion 313 B configuring the trench TR, the insulating layer 311, and the light shielding layer 313 ing.

[0277]
Therefore, in the present embodiment, as in the case of the fifth embodiment, the image quality of the captured image can be improved.

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[0278]

In particular, in the present embodiment, in order to make the shift amount Dx between the center axis 313 BCX of the second light shielding portion 313 </ b> B and the central axis 301 </ b> CX of the pixel separation portion 301 larger than that in the fifth embodiment, A light shielding portion 313B is formed (see FIG. 22).

That is, the light-shielding layer 313 of the fifth embodiment is replaced by the light-shielding layer 313 of the second embodiment.

[0279]

Therefore, in this embodiment, as described in the second embodiment, the light can reach the photodiode 21 more efficiently than in the fifth embodiment.

Further, occurrence of "mixed color" and the like can be more effectively suppressed.

[0280]

In the present embodiment, the light-shielding layer 313 of Embodiment 5 is replaced with the light-shielding layer 313 of Embodiment 2, but the present invention is not limited to this. The light shielding layer 313 of the fifth embodiment may be replaced with the light shielding layer 313 of the third embodiment.

[0281]

＜7． Seventh Embodiment (A) Device Configuration and the Like FIG. 23 is a diagram showing a main part of a solid-state imaging device according to a seventh embodiment.

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[0282]

FIG. 23 shows the pixel separation section 301 between the pixels P arranged in the peripheral part of the pixel region PA shown in FIG. 2, similarly to FIG. 21, and shows the X 1 S - X 2 S part. FIG. 23 shows a cross section of the pixel separation section 301.

[0283]

As shown in FIG. 23, in the present embodiment, as can be seen from comparison with FIG. 21, in the peripheral portion of the pixel region PA, the positions of the trench TR, the insulating layer 311, and the light shielding layer 313 are the same as in Embodiment 5 and It is different. Except for this point and related points, the present embodiment is similar to the fifth embodiment. For this reason, descriptions of overlapping parts are omitted as appropriate.

[0284]
As shown in FIG. 23, the pixel separation portion 301 is provided with a pixel separation diffusion layer 101 pb as in the fifth embodiment.

[0285]

23, in the pixel separating section 301, as shown in FIG. 23, the center axis 313 ACX of the trench TR and the center axis 301 CX of the pixel separating section 301 are separated from each other by a predetermined shift amount Dx in the horizontal direction x , A trench TR is formed.

Further, the center axis 313 ACX of the insulating layer 311 in the trench TR is located closer to the peripheral side of the pixel region PA (see FIG. 2) than the central axis 301 CX of the pixel separation portion 301. An insulating layer 311 is formed so as to shift to the right side in FIG. 21). The center axes 313 ACX and 313 BCX of the first light shielding portion 313 A and the second light shielding portion 313 B and the center axis 301 CX of the pixel separation portion 301 are formed so as to be separated by a predetermined shift amount Dx in the horizontal direction x There.

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[0286]
As described above, in the present embodiment, "pupil correction" is performed similarly for each of the first light-shielding portion 313 A and the second light-shielding portion 313 B constituting the trench TR, the insulating layer 311, and the light-shielding layer 313 There.

[0287]
However, in the present embodiment, as shown in FIG. 23, each part is formed so that the shift amount Dx is larger than in the case of the fifth embodiment.

[0288]
In this case, as shown in FIG. 23, the trench TR is formed so as to be positioned on a portion where the pixel separation diffusion layer 101 pb is formed and a portion other than that portion on the back surface (upper surface) of the semiconductor substrate 101 .

[0289]

Further, in this embodiment, the trench TR is formed so as to be located inside the p-type semiconductor region 101 pa provided on the back side of the n-type semiconductor region 101 n in the semiconductor substrate 101.

For example, the p-type semiconductor region 101 pa is formed so that the depth from the back surface of the semiconductor substrate 101 is 300 to 500 nm, and the trench TR is formed to a depth shallower than this depth.

[0290]
(8) Summary As described above, in the present embodiment, so-called "pupil correction" is performed on the first light shielding portion 313 A and the second light shielding portion 313 B configuring the trench TR, the insulating layer 311, and the light shielding layer 313 ing.

[0291]
Therefore, in the present embodiment, as in the case of the fifth embodiment, the image quality of the captured image can be improved.

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[0292]

The depletion layer of the photodiode 21 does not extend deep within the p-type semiconductor region 101 pa.

Therefore, in the range where the p-type semiconductor region 101 pa exists, the photoelectric conversion and the number of saturated electrons do not change.

Therefore, in the present embodiment, the trench TR is also formed in a portion other than the portion where the pixel separation diffusion layer 101 pb is formed, but the sensitivity and the number of saturated electrons do not change.

[0293]

＜8.

Embodiment 8> (A) Apparatus Configuration, etc. FIG. 24 is a diagram showing a main part of a solid-state imaging device in Embodiment 8. In FIG.

[0294]

FIG. 24 shows a pixel separation section 301 between pixels P arranged in the peripheral part of the pixel region PA shown in FIG. 2, similarly to FIG. 21, and shows the X 1 S - X 2 S part.

FIG. 24 shows a cross section of the pixel separation section 301.

[0295]

As shown in FIG. 24, in the present embodiment, as can be seen from comparison with FIG. 21, the trench TR in the peripheral portion of the pixel region PA is different from that in the fifth

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embodiment. Except for this point and related points, the present embodiment is similar to the fifth embodiment. For this reason, descriptions of overlapping parts are omitted as appropriate.

[0296]
As shown in FIG. 24, the trench TR is formed so as to penetrate between the back surface (upper surface) and the front surface (lower surface) of the semiconductor substrate 101.

[0297]
As shown in FIG. 24, the insulating layer 311 is formed inside the trench TR so as to cover the side surface.

[0298]

As shown in FIG. 24, the first light shielding portion 313 A of the light shielding layer 313 is formed so as to bury the inside of the trench TR with the insulating layer 311 interposed therebetween.

Here, the first light shielding portion 313 </ b> A is formed so as to penetrate between the back surface (upper surface) and the front surface (lower surface) of the semiconductor substrate 101.

[0299]
The second light shielding portion 313 </ b> B is formed above the back surface (upper surface) of the semiconductor substrate 101 via the insulating layer 311.

[0300]
(B) Summary As described above, in the present embodiment, so-called "pupil correction" is performed on the first light shielding portion 313 A and the second light shielding portion 313 B configuring the trench TR, the insulating layer 311, and the light shielding layer 313 ing.

[0301]
Therefore, in the present embodiment, as in the case of the fifth embodiment, the image quality of the captured image can be improved.

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[0302]

In particular, in the present embodiment, the trench TR is formed so as to penetrate between the back surface (upper surface) and the front surface (lower surface) of the semiconductor substrate 101.

An insulating layer 311 and a light shielding layer 313 are formed inside the trench TR.

Like the trench TR, the first light shielding portion 313 A of the light shielding layer 313 is formed so as to penetrate between the back surface (upper surface) and the front surface (lower surface) of the semiconductor substrate 101.

[0303]

Therefore, in the present embodiment, it is possible to block light between the pixels P over the entire depth direction z of the semiconductor substrate 101.

Therefore, occurrence of "color mixing" or the like can be prevented more favorably.

[0304]

In the present embodiment, in the case of the fifth embodiment, the structure in which the trench TR penetrates is shown, but the configuration is not limited to this.

In another embodiment, the trench TR may be penetrated.

[0305]

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< 9 . Ninth Embodiment (A) Device Configuration and the Like FIG. 25 is a diagram showing a main part of a solid-state imaging device according to a ninth embodiment.

[0306]

FIG. 25 shows a pixel separation section 301 between pixels P arranged in the peripheral portion of the pixel area PA shown in FIG. 2, similarly to FIG. 24, showing the X 1 S - X 2 S portion. FIG. 25 shows a cross section of the pixel separation section 301.

[0307]

As shown in FIG. 25, in the present embodiment, as can be seen from comparison with FIG. 24, the first light shielding portion 313 A of the light shielding layer 313 is different from the case of the eighth embodiment in the peripheral portion of the pixel region PA. Except for this point and related points, the present embodiment is similar to the eighth embodiment. For this reason, descriptions of overlapping parts are omitted as appropriate.

[0308]
As shown in FIG. 25, the first light shielding portion 313 A of the light shielding layer 313 penetrates between the back surface (upper surface) and the front surface (lower surface) of the semiconductor substrate 101.

[0309]

At the same time, the first light shielding portion 313 A of the light shielding layer 313 is provided so as to be connected to the wiring 111 h constituting the wiring layer 111.

Here, the first light shielding portion 313 </ b> A is connected to the wiring 111 h provided in the portion closest to the semiconductor substrate 101 among the plurality of wirings 111 h provided so as to be stacked in the wiring layer 111. As described above, the first light shielding portion 313 A is made of a metal material and has conductivity, so it is electrically connected to the wiring 111 h.

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[0310]

For the first light shielding portion 313 A of the light shielding layer 313, a voltage may be applied via the wiring 111 h. In the present embodiment, it is preferable to apply, for example, a negative voltage of -1.0 to 3.0 V to the first light shielding portion 313 </ b> A at the time of performing the imaging operation. As a result, holes are accumulated in the vicinity of the interface, so generation of dark current can be suitably prevented (see JP-A-2007-258684).

[0311]

(B) Summary As described above, in the present embodiment, so-called "pupil correction" is performed on the first light shielding portion 313 A and the second light shielding portion 313 B configuring the trench TR, the insulating layer 311, and the light shielding layer 313 ing.

[0312]

Therefore, in the present embodiment, as in the case of the fifth embodiment, the image quality of the captured image can be improved.

[0313]

In the present embodiment, the first light shielding portion 313 </ b> A penetrates between the surface on the back (upper surface) side and the surface (lower surface) side in the semiconductor substrate 101, and the insulating layer 111 z And is connected to the wiring 111 h provided therein.

Then, by applying a voltage to the first light shielding portion 313 A via the wiring 111 h, generation of dark current is suppressed.

Therefore, the image quality of the captured image can be further improved.

[0314]

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<10. Other> The implementation of the present technology is not limited to the above-described embodiment, and various modifications can be adopted.

[0315]

In the above embodiment, the case where the present technology is applied to a camera has been described, but the present invention is not limited thereto. The present technology may be applied to other electronic devices including a solid-state imaging device such as a scanner or a copier.

[0316]

In the above embodiment, the case where four types of transfer transistors, amplification transistors, selection transistors, and reset transistors are provided as pixel transistors has been described, but the present invention is not limited thereto. For example, the present invention may be applied to a case where three types of transfer transistors, amplification transistors, and reset transistors are provided as pixel transistors.

[0317]

In the above embodiment, a case where one transfer transistor, one amplification transistor, one selection transistor, and one reset transistor is provided for one photodiode has been described, but the present invention is not limited thereto. For example, the present invention may be applied to a case where one amplification transistor, one selection transistor, and one reset transistor are provided for each of a plurality of photodiodes.

[0318]
In addition to the CMOS type image sensor, the present technology may be applied to a CCD type image sensor.

[0319]

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Further, in the manufacture of the solid-state imaging device, when forming the trench TR in the portion formed by the pixel separation portion 301, the trench may be formed simultaneously with other portions.

For example, when the surface of a pad electrode (not shown) formed similarly to the wiring 111 h in the wiring layer 111 is exposed, a trench may be formed above the surface thereof in the same step as above. By doing so, it is possible to further improve the manufacturing efficiency.

[0320]

In addition, the insulating layer 311 of the above embodiment may be formed by a so-called LOCOS (Local Oxidation of Silicon) process. In other words, the insulating layer 311 may be formed by locally oxidizing the surface of the semiconductor substrate 101.

[0321]
In addition, each of the above embodiments may be appropriately combined.

[0322]
That is, the present technology can also take the following configuration.

[0323]
(1) A plurality of photoelectric conversion units are provided in the semiconductor substrate, corresponding to each of a plurality of pixels arranged in a pixel area of the semiconductor substrate with a space therebetween, and the photoelectric conversion unit receives incident light on a light receiving surface, And a pixel separation portion provided in the semiconductor substrate so as to be interposed between the plurality of pixels in the pixel region, wherein the pixel separation portion is formed on the incident surface side of the semiconductor substrate A first light shielding portion provided inside the trench, a second light shielding portion provided on the incident surface side surface of the semiconductor substrate, the second light shielding portion provided on the incident surface side of the first light shielding portion, , The second light shielding portion is formed such that the center of the second light shielding portion is shifted more toward the periphery of the pixel region than the center of the pixel separating portion around the center of the pixel region It is formed to be a solid Image apparatus.

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[0324]
(2) The pixel separating portion may further include an insulating layer covering the inner surface of the trench, and the first light shielding portion is formed so as to bury the inside of the trench with the insulating layer interposed therebetween. The solid-state imaging device according to (1) above.

[0325]

(3) The semiconductor device according to (1), wherein the insulating layer includes a first insulating film covering an inner surface of the trench and a second insulating film covering an inner surface of the trench with the first insulating film interposed therebetween, The solid-state imaging device according to (2), wherein a refractive index of the first insulating film is formed using a material between the semiconductor substrate and the second insulating film.

(4) The semiconductor device according to any one of (1) to (3), wherein the trench is formed such that the width of the incident surface side of the semiconductor substrate is larger than the width of the surface opposite to the incident surface, State image pickup device.

[0326]
(5) The semiconductor device according to any one of (1) to (4), wherein the second light shielding portion is formed so as to be located within a range of a portion where the trench is located on a surface of the semiconductor substrate on the incident surface side Wherein the solid-state imaging device is a solid-state imaging device.

[0327]
(6) The solid-state imaging device according to (5), wherein the second light shielding portion is formed so that a width of a peripheral portion of the pixel region is narrower than a width of a central portion of the pixel region.

[0328]
(7) The liquid crystal display device according to any one of (1) to (6) above, wherein the pixel separating unit includes a pixel separating / diffusing layer in which an impurity of a conductivity type different from that of a semiconductor region accumulating a signal charge in the photoelectric converting portion is diffused Of the solid-state imaging device.

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[0329]
(8) The trench is formed so that the center of the trench is more shifted toward the periphery of the pixel region than the center of the pixel isolation portion in the periphery of the center of the pixel region , The solid-state imaging device according to any one of the above (1) to (7).

[0330]
(9) In the first light-shielding portion, the center of the first light-shielding portion is more shifted toward the periphery of the pixel region than the center of the pixel separating portion around the center of the pixel region And the second electrode is formed so as to be in contact with the first electrode.

[0331]
(10) Each of the first light-shielding portion and the second light-shielding portion is formed such that the central axis of the first light-shielding portion and the central axis of the second light-shielding portion coincide with each other, 9).

[0332]
(11) The pixel separating unit may include a pixel separating / diffusing layer in which an impurity of a conductivity type different from that of a semiconductor region accumulating a signal charge in the photoelectric converting portion is diffused, and the trench is formed in the pixel The solid-state imaging device according to the above (8), wherein the solid-state imaging device is formed in a portion where a separation diffusion layer is formed.

[0333]
(12) The semiconductor device according to any one of (1) to (12), wherein the trench is formed so as to penetrate between the surface on the incident surface side and the surface on the opposite side from the incident surface in the semiconductor substrate).

[0334]
(13) The semiconductor device according to (12), wherein the first light shielding portion is formed so as to penetrate between the surface on the incident surface side and the surface on the opposite side to the incident surface, Of the solid-state imaging device.

[0335]

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(14) a pixel transistor which is provided on a surface of the semiconductor substrate opposite to the incident surface and outputs the signal charge generated by the photoelectric conversion portion as an electric signal; and And a wiring layer provided so as to cover the pixel transistor on a surface on the opposite side of the solid-state imaging device, the solid-state imaging device having the solid-state imaging device according to any one of (1) to (13).

(15) The semiconductor light-emitting device according to (15), wherein the first light-shielding portion penetrates between the surface on the incident surface side and the surface on the opposite side from the incident surface, in the semiconductor substrate, (14), wherein the solid-state imaging device is connected to the wiring.

[0336]
(16) The liquid crystal display device according to (16), further comprising a color filter through which the incident light is transmitted to the light receiving surface, wherein the color filter includes a plurality of filter layers having high transmittance for light in different wavelength ranges, (1) to (15), wherein the plurality of pixels are arranged adjacent to each other.

[0337]
(17) Forming a plurality of photoelectric conversion portions provided inside the semiconductor substrate so as to correspond to each of a plurality of pixels aligned in the pixel region of the semiconductor substrate with photoelectric conversion portions for receiving incident light on the light receiving surface And a pixel separation portion forming step of providing a pixel separation portion in the semiconductor substrate so as to be interposed between the plurality of pixels in the pixel region, wherein in the pixel separation portion forming step, A first light shielding portion is provided inside the trench formed on the incident surface side in the pixel separation portion of the first light shielding portion on the incident surface side of the semiconductor substrate, Wherein in the step of forming the second light shielding portion, at least in the periphery of the center of the pixel region, the center of the second light shielding portion is located closer to the center of the pixel separating portion than the second light shielding portion, region To shift more toward the periphery, forming the second light-shielding portion, the manufacturing method of the solid-state imaging device.

[0338]
(18) A photoelectric conversion device comprising: a plurality of photoelectric conversion units provided in the semiconductor substrate, each photoelectric conversion unit receiving incident

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light on a light receiving surface, corresponding to each of a plurality of pixels aligned in a pixel area of a semiconductor substrate with a spacing therebetween; And a pixel separation portion provided in the semiconductor substrate so as to be interposed between the plurality of pixels in the pixel region, wherein the pixel separation portion is formed on the incident surface side of the semiconductor substrate A first light shielding portion provided inside the trench, a second light shielding portion provided on the incident surface side surface of the semiconductor substrate, the second light shielding portion provided on the incident surface side of the first light shielding portion, , The second light shielding portion is formed such that the center of the second light shielding portion is shifted more toward the periphery of the pixel region than the center of the pixel separating portion around the center of the pixel region It is formed so that electricity Equipment.

[0339]

In the above embodiment, the photodiode 21 is an example of a photoelectric conversion unit.

Further, in the above embodiment, the camera 40 is an example of an electronic device.

[0340]

17: External output circuit 17a: AGC circuit 17b: ADC circuit 18: Timing generator 19: Shutter driving circuit 1: Solid state imaging device 13: Vertical driving circuit 14: Column circuit 15: Horizontal driving circuit 17: External output circuit 17: 21: photodiode, 22: transfer transistor, 23: amplification transistor, 24: selection transistor, 25: reset transistor, 26: transfer line, 27: vertical signal line, 28: address line, 29: reset line, 40: A p-type semiconductor region; 101 pc: a p-type semiconductor region; 111: a wiring layer; 111 h: a wiring , 111 z: an insulating layer, 301: a pixel separation portion, 311: an insulating layer, 311 A: a first insulating film, 311 B: a CF: color filter, CFB: green filter layer, CFR: green filter layer, CFR: red filter layer, FD: floating diffusions , H: incident light, HM: hard mask, HT: flattening film, I: constant current source, JS: light receiving surface, ML: microlens, P: pixel, PA: pixel region, PS: imaging surface, SA: peripheral Region, SS: support substrate, SZ, insulating film, TR: trench, Tr: pixel transistor

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CLAIMS JP2012169530

1.
A plurality of photoelectric conversion units provided inside the semiconductor substrate corresponding to each of a plurality of pixels aligned in a pixel region of the semiconductor substrate with a space therebetween and receiving incident light on a light receiving surface; And a pixel separating portion which is provided in the semiconductor substrate so as to be interposed between the plurality of pixels in the semiconductor substrate, wherein the pixel separating portion is formed in a portion of a trench formed on the incident surface side of the semiconductor substrate At least a first light shielding portion provided in the interior and a second light shielding portion provided on the incident surface side surface of the semiconductor substrate and provided on the incident surface side of the first light shielding portion , The second light shielding portion is formed such that the center of the second light shielding portion is shifted more toward the periphery of the pixel region from the center of the pixel separation portion in the periphery than the center of the pixel region Solid state imaging device formed .

2.
2. The semiconductor device according to claim 1, wherein the pixel separating portion further includes an insulating layer covering an inner surface of the trench, and the first light shielding portion is formed so as to bury the inside of the trench via the insulating layer. Of the solid-state imaging device.

3.
Wherein the insulating layer includes a first insulating film covering an inner surface of the trench and a second insulating film covering an inner surface of the trench with the first

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insulating film interposed therebetween, The solid-state imaging device according to claim 2, wherein the film is formed using a material having a refractive index between the semiconductor substrate and the second insulating film.

4.

The solid-state imaging device according to claim 1, wherein the trench is formed such that a width of the semiconductor substrate on the incident surface side is larger than a width on a surface side opposite to the incident surface.

5.

2. The solid-state imaging device according to claim 1, wherein the second light shielding portion is formed so as to be located within a range of a portion where the trench is located on a surface of the semiconductor substrate on the incident surface side.

6.

6. The solid-state imaging device according to claim 5, wherein the second light-shielding portion is formed so that a width in a peripheral portion of the pixel region is narrower than a width in a central portion of the pixel region.

7.

2. The solid-state imaging device according to claim 1, wherein the pixel separation unit includes a pixel separation diffusion layer in which an impurity having a conductivity type different from that of a semiconductor region in which the signal charge is accumulated in the photoelectric conversion unit is diffused.

8.

The trench is formed such that the center of the trench is shifted more toward the periphery of the pixel region than the center of the pixel isolation portion in the periphery of the center of the pixel region Wherein the solid-state imaging device is a solid-state imaging device.

9.

The first light-shielding portion is formed such that the center of the first light-shielding portion is shifted more toward the periphery of the pixel region with respect to the center of the pixel separation portion in the periphery than the center of the pixel region State image pickup device according to claim 8.

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10.
Each of the first light-shielding portion and the second light-shielding portion is formed such that a central axis of the first light-shielding portion and a central axis of the second light-shielding portion coincide with each other. .

11.
Wherein the pixel separating unit includes a pixel separation diffusion layer in which an impurity of a conductivity type different from that of a semiconductor region in which the signal charge is accumulated in the photoelectric conversion unit is diffused and the trench is formed in the pixel separation diffusion layer Is formed in a portion where the first electrode and the second electrode are formed.

12.
The solid-state imaging device according to claim 1, wherein the trench penetrates between a surface on the incident surface side and a surface on the opposite side to the incident surface in the semiconductor substrate.

13.
The solid state image pickup device according to claim 12, wherein the first light shielding portion is formed so as to penetrate between a surface on the incident surface side and a surface on the opposite side from the incident surface in the semiconductor substrate .

14.
A pixel transistor which is provided on a surface of the semiconductor substrate opposite to the incident surface and outputs a signal charge generated by the photoelectric conversion portion as an electric signal; a pixel transistor provided on a side of the semiconductor substrate opposite to the incident surface And a wiring layer provided so as to cover the pixel transistor in a plane of the solid-state imaging device.

15.
The first light-shielding portion penetrates between the surface on the incident surface side and the surface on the opposite side to the incident surface in the semiconductor substrate, and the first light-shielding portion penetrates through the wiring provided in the insulating layer in the wiring layer 15. The solid-state imaging device according to claim 14, being connected.

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16.

Wherein the plurality of types of filter layers having high transmittance for light in different wavelength ranges are adjacent to each other corresponding to each of the plurality of pixels, And the second light receiving element is arranged in the second direction.

17.

A photoelectric conversion portion forming step in which a plurality of photoelectric conversion portions for receiving incident light on a light receiving surface are provided inside the semiconductor substrate so as to correspond to each of a plurality of pixels aligned in a pixel region of the semiconductor substrate, And a pixel separation portion forming step of providing a pixel separation portion in the semiconductor substrate so as to be interposed between the plurality of pixels in the pixel region, wherein in the pixel separation portion forming step, A first light shielding portion is provided inside the trench formed on the incident surface side in the separation portion and a second light shielding portion is formed on the incident surface side surface of the semiconductor substrate and on the incident surface side of the first light shielding portion, Wherein in the step of forming the second light shielding portion, the center of the second light shielding portion is located closer to the center of the pixel separation portion than the center of the pixel region in the vicinity of the pixel region of To to shift more to form the second light-shielding portion, the manufacturing method of the solid-state imaging device.

18.

A plurality of photoelectric conversion units provided inside the semiconductor substrate corresponding to each of a plurality of pixels aligned in a pixel region of the semiconductor substrate with a space therebetween and receiving incident light on a light receiving surface; And a pixel separating portion which is provided in the semiconductor substrate so as to be interposed between the plurality of pixels in the semiconductor substrate, wherein the pixel separating portion is formed in a portion of a trench formed on the incident surface side of the semiconductor substrate At least a first light shielding portion provided in the interior and a second light shielding portion provided on the incident surface side surface of the semiconductor substrate and provided on the incident surface side of the first light shielding portion , The second light shielding portion is formed such that the center of the second light shielding portion is shifted more toward the periphery of the pixel region from the center of the pixel separation portion in the periphery than the center of the pixel region The electronic equipment being formed.

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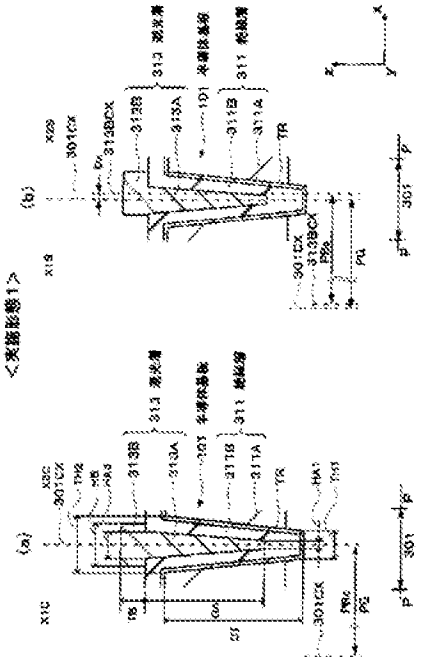
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(54)【発明の名称】固体撮像装置、および、その製造方法、電子機器

(57)【要約】
【課題】撮像画像の画像品質を向上させる。
【解決手段】半導体基板１０１の画素分離部３０１に形成されたトレンチＴＲの内部に第１遮光部３１３Ａを設ける。これと共に、その第１遮光部３１３Ａの上面側に第２遮光部３１３Ｂを設ける。ここでは、画素領域ＰＡの中心よりも周辺において、第２遮光部３１３Ｂの中心が、画素分離部３０１の中心に対して、画素領域ＰＡの周辺の側へ多くシフトするように、第２遮光部３１３Ｂを形成する。つまり、少なくとも第２遮光部について「瞳補正」を実施する。
【選択図】図５



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【特許請求の範囲】
【請求項１】
半導体基板の画素領域に間を隔てて並ぶ複数の画素のそれぞれに対応して、複数が前記半導体基板の内部に設けられており、入射光を受光面で受光する光電変換部と、
前記画素領域において前記複数の画素の間に介在するように前記半導体基板の内部に設けられている画素分離部と
を有し、
前記画素分離部は、
前記半導体基板の前記入射面側に形成されたトレンチの内部に設けられている第１遮光部と、
前記半導体基板の前記入射面側の面上であって、前記第１遮光部の前記入射面側に設けられている第２遮光部と
を少なくとも含み、
前記第２遮光部は、前記画素領域の中心よりも周辺において、当該第２遮光部の中心が、前記画素分離部の中心に対して、前記画素領域の周辺の側へ多くシフトするように形成されている、
固体撮像装置。
【請求項２】
前記画素分離部は、
前記トレンチの内部の面を被覆する絶縁層
を更に含み、
前記第１遮光部は、前記絶縁層を介して前記トレンチの内部を埋め込むように形成されている、
請求項１に記載の固体撮像装置。
【請求項３】
前記絶縁層は、
前記トレンチの内側の面を被覆する第１絶縁膜と、
前記第１絶縁膜を介在して前記トレンチの内側の面を被覆する第２絶縁膜と
を含み、
前記第１絶縁膜は、屈折率が前記半導体基板と前記第２絶縁膜との間の材料を用いて形成されている、
請求項２に記載の固体撮像装置。
【請求項４】
前記トレンチは、前記半導体基板において前記入射面側の幅が、前記入射面と反対側の面の側の幅よりも広くなるように形成されている、
請求項１に記載の固体撮像装置。
【請求項５】
前記第２遮光部は、前記半導体基板の前記入射面側の面において、前記トレンチが位置する部分の範囲内に位置するように形成されている、
請求項１に記載の固体撮像装置。
【請求項６】
前記第２遮光部は、前記画素領域の周辺部分における幅が、前記画素領域の中心部分における幅よりも狭くなるように形成されている、
請求項５に記載の固体撮像装置。
【請求項７】
前記画素分離部は、
前記光電変換部において信号電荷を蓄積する半導体領域とは異なる導電型の不純物が拡散された画素分離拡散層
を有する、
請求項１に記載の固体撮像装置。

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【請求項８】
前記トレンチは、前記画素領域の中心よりも周辺において、当該トレンチの中心が、前記画素分離部の中心に対して、前記画素領域の周辺の側へ多くシフトするように形成されている、
請求項１に記載の固体撮像装置。
【請求項９】
前記第１遮光部は、前記画素領域の中心よりも周辺において、当該第１遮光部の中心が、前記画素分離部の中心に対して、前記画素領域の周辺の側へ多くシフトするように形成されている、
請求項８に記載の固体撮像装置。
【請求項１０】
前記第１遮光部と前記第２遮光部とのそれぞれは、当該第１遮光部の中心軸と当該第２遮光部の中心軸とが互いに一致するように形成されている、
請求項９に記載の固体撮像装置。
【請求項１１】
前記画素分離部は、
前記光電変換部において信号電荷を蓄積する半導体領域とは異なる導電型の不純物が拡散された画素分離拡散層
を有し、
前記トレンチは、前記半導体基板において前記画素分離拡散層が形成された部分に形成されている、
請求項８に記載の固体撮像装置。
【請求項１２】
前記トレンチは、前記半導体基板において、前記入射面の側の面と、前記入射面とは反対側の面との間を貫通するように形成されている、
請求項１に記載の固体撮像装置。
【請求項１３】
前記第１遮光部は、前記半導体基板において、前記入射面の側の面と、前記入射面とは反対側の面との間を貫通するように形成されている、
請求項１２に記載の固体撮像装置。
【請求項１４】
前記半導体基板において前記入射面とは反対側の面に設けられており、前記光電変換部で生成された信号電荷を電気信号として出力する画素トランジスタと、
前記半導体基板において前記入射面とは反対側の面にて、前記画素トランジスタを被覆するように設けられている配線層と
を有する、
請求項１に記載の固体撮像装置。
【請求項１５】
前記第１遮光部は、前記半導体基板において、前記入射面の側の面と、前記入射面とは反対側の面との間を貫通し、前記配線層において絶縁層中に設けられた配線に接続されている、
請求項１４に記載の固体撮像装置。
【請求項１６】
前記入射光が前記受光面へ透過するカラーフィルタ
を含み、
前記カラーフィルタは、
互いに異なる波長範囲の光について透過率が高い複数種のフィルタ層が、前記複数の画素のそれぞれに対応して互いに隣接して配置されている、
請求項１に記載の固体撮像装置。
【請求項１７】

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入射光を受光面で受光する光電変換部を、半導体基板の画素領域に間を隔てて並ぶ複数の画素のそれぞれに対応するように、前記半導体基板の内部に複数設ける光電変換部形成工程と、

前記画素領域において前記複数の画素の間に介在するように前記半導体基板の内部に画素分離部を設ける画素分離部形成工程と

を有し、

前記画素分離部形成工程では、

前記半導体基板の前記画素分離部において前記入射面側に形成されたトレンチの内部に第１遮光部を設けると共に、前記半導体基板の前記入射面側の面上であって前記第１遮光部の前記入射面側に第２遮光部を少なくとも設け、

前記第２遮光部の形成工程では、前記画素領域の中心よりも周辺において、前記第２遮光部の中心が、前記画素分離部の中心に対して、前記画素領域の周辺の側へ多くシフトするように、前記第２遮光部を形成する、

固体撮像装置の製造方法。

【請求項１８】

半導体基板の画素領域に間を隔てて並ぶ複数の画素のそれぞれに対応して、複数が前記半導体基板の内部に設けられており、入射光を受光面で受光する光電変換部と、

前記画素領域において前記複数の画素の間に介在するように前記半導体基板の内部に設けられている画素分離部と

を有し、

前記画素分離部は、

前記半導体基板の前記入射面側に形成されたトレンチの内部に設けられている第１遮光部と、

前記半導体基板の前記入射面側の面上であって、前記第１遮光部の前記入射面側に設けられている第２遮光部と

を少なくとも含み、

前記第２遮光部は、前記画素領域の中心よりも周辺において、当該第２遮光部の中心が、前記画素分離部の中心に対して、前記画素領域の周辺の側へ多くシフトするように形成されている、

電子機器。

【発明の詳細な説明】

【技術分野】

【０００１】

本技術は、固体撮像装置、および、その製造方法、電子機器に関する。

【背景技術】

【０００２】

デジタルビデオカメラ、デジタルスチルカメラなどの電子機器は、固体撮像装置を含む。たとえば、固体撮像装置として、ＣＭＯＳ（Ｃｏｍｐｌｅｍｅｎｔａｒｙ Ｍｅｔａｌ Ｏｘｉｄｅ Ｓｅｍｉｃｏｎｄｕｃｔｏｒ）型イメージセンサ、ＣＣＤ（Ｃｈａｒｇｅ Ｃｏｕｐｌｅｄ Ｄｅｖｉｃｅ）型イメージセンサを含む。

【０００３】

固体撮像装置は、基板の画素領域に複数の画素が配列されている。各画素においては、光電変換部が設けられている。光電変換部は、たとえば、フォトダイオードであり、入射光を受光面で受光し光電変換することによって、信号電荷を生成する。

【０００４】

固体撮像装置のうち、ＣＣＤ型イメージセンサは、画素領域において、垂直方向に並ぶ複数の画素の列の間に、垂直転送部が設けられている。垂直転送部は、垂直転送チャネル領域にゲート絶縁膜を介して対面するように複数の転送電極が設けられており、電荷読出し部によって光電変換部から読み出された信号電荷を、垂直方向へ転送するように構成されている。

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【０００５】
これに対して、ＣＭＯＳ型イメージセンサは、光電変換部のほかに、画素トランジスタを含むように、画素が構成されている。画素トランジスタは、光電変換部で生成された信号電荷を読み出して，信号線へ電気信号として出力するように構成されている。
【０００６】
固体撮像装置では、一般に、基板において、複数の配線が積層された多層配線層が設けられた表面側に設けられており、その表面側から入射する光を、光電変換部が受光面で受光する。
【０００７】
「表面照射型」の場合には、マイクロレンズと受光面との間に、多層配線層が介在し集光面と受光面との間の距離が長い。このため、受光面に対して傾斜して光が入射したときには、その多層配線層に含まれる配線に、その光が遮られて、受光面に到達しない場合がある。よって、感度を向上させることが困難な場合がある。
【０００８】
このため、基板において多層配線層が設けられた表面とは反対側の裏面側から入射する光を、光電変換部が受光する「裏面照射型」が提案されている。
【０００９】
固体撮像装置においては、一の画素に入射した入射光が、その一の画素のフォトダイオードに入射せずに、隣接する他の画素のフォトダイオードに入射する場合がある。このため、このような光学的な現象に起因して信号にノイズが含まれることになり、撮像画像の画像品質が低下する場合がある。たとえば、カラー画像を撮像する場合において、入射光が受光面に対して傾斜して入射したときには、その直下の受光面に入射せずに、本来、他の色の着色光を受光する他の受光面へ入射する場合がある。このため、いわゆる「混色」が発生して、撮像したカラー画像において色調のズレが生じ、画像品質が低下する場合がある。このような不具合の発生を抑制するために、複数の画素の間に遮光膜を設けている（たとえば、特許文献１，２参照）。
【００１０】
また、複数の画素が配列された画素領域の中心部分においては、外付けの光学系を介して入射する主光線の角度が、受光面に対して、ほぼ垂直であるのに対して、その画素領域の周辺部分においては、入射する主光線の角度が傾斜している。このため，撮像画像の中心部分が明るい画像になり、周辺部分が暗い画像になる場合がある。つまり、いわゆるシェーディング現象が発生して、画像品質が低下する場合がある。このような不具合を改善するために、「瞳補正」と称して、オンチップレンズ等の配置を補正することが、実施されている。具体的には、画素領域の周辺において配置されるオンチップレンズの位置が、受光面に対して、画素領域の中心側へシフトするように、オンチップレンズを設けることが実施されている。たとえば、画素領域にて並ぶ複数の光電変換部のピッチよりも、オンチップレンズのピッチが狭くなるように、各部を配置している（たとえば、特許文献３などを参照）。
【００１１】
また，固体撮像装置では、光電変換部が設けられた半導体基板の界面準位に起因して暗電流が発生することを抑制して画像品質を向上させるために、光電変換部をＨＡＤ（Ｈｏｌｅ Ａｃｃｕｍｕｌａｔｉｏｎ Ｄｉｏｄｅ）構造にすることが提案されている。ＨＡＤ構造では、ｎ型の電荷蓄積領域の受光面上に正電荷蓄積（ホール）蓄積領域を形成することで、暗電流の発生を抑制している。そして，この正電荷蓄積領域を光電変換部の界面部分に形成するために、「負の固定電荷を有する膜」をピニング層として設けて、暗電流の発生を抑制することが提案されている。たとえば、酸化ハフニウム膜（HfO_2膜）のような高誘電体膜を、「負の固定電荷を有する膜」として用いている（たとえば，特許文献４などを参照）。
【００１２】
また、暗電流の発生を抑制するために、「裏面照射型」の表面側に、制御ゲートを設け

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、その制御ゲートに負電圧を印加することが提案されている（たとえば、特許文献５などを参照）。その他、暗電流の発生を抑制するために、光を受光する受光面部分が開口した金属遮光膜に負電圧を印加することが提案されている（たとえば、特許文献６などを参照）

【００１３】

このように、固体撮像装置においては、撮像画像の画像品質を向上させるために、種々の技術が提案されている。

【先行技術文献】

【特許文献】

【００１４】

【特許文献１】特開２０１０－１０９２９５号公報
【特許文献２】特開２０１０－１８６８１８号公報
【特許文献３】特許３５５１４３７号
【特許文献４】特開２００８－３０６１５４号公報
【特許文献５】特開２００７－２５８６８４号公報
【特許文献６】特開平５－２７５６７３号公報

【発明の概要】

【発明が解決しようとする課題】

【００１５】

固体撮像装置においては、さらに、撮像画像の画像品質などを向上させることが望まれている。

【００１６】

したがって、本技術は、撮像画像の画像品質などを向上可能な、固体撮像装置、および、その製造方法、電子機器を提供する。

【課題を解決するための手段】

【００１７】

本技術の固体撮像装置および電子機器は、半導体基板の画素領域に間を隔てて並ぶ複数の画素のそれぞれに対応して、複数が前記半導体基板の内部に設けられており、入射光を受光面で受光する光電変換部と、前記画素領域において前記複数の画素の間に介在するように前記半導体基板の内部に設けられている画素分離部とを有し、前記画素分離部は、前記半導体基板の前記入射面側に形成されたトレンチの内部に設けられている第１遮光部と、前記半導体基板の前記入射面側の面上であって、前記第１遮光部の前記入射面側に設けられている第２遮光部とを少なくとも含み、前記第２遮光部は、前記画素領域の中心よりも周辺において、当該第２遮光部の中心が、前記画素分離部の中心に対して、前記画素領域の周辺の側へ多くシフトするように形成されている。

【００１８】

本技術の固体撮像装置の製造方法は、入射光を受光面で受光する光電変換部を、半導体基板の画素領域に間を隔てて並ぶ複数の画素のそれぞれに対応するように、前記半導体基板の内部に複数設ける光電変換部形成工程と、前記画素領域において前記複数の画素の間に介在するように前記半導体基板の内部に画素分離部を設ける画素分離部形成工程とを有し、前記画素分離部形成工程では、前記半導体基板の前記画素分離部において前記入射面側に形成されたトレンチの内部に第１遮光部を設けると共に、前記半導体基板の前記入射面側の面上であって前記第１遮光部の前記入射面側に第２遮光部を少なくとも設け、前記第２遮光部の形成工程では、前記画素領域の中心よりも周辺において、前記第２遮光部の中心が、前記画素分離部の中心に対して、前記画素領域の周辺の側へ多くシフトするように、前記第２遮光部を形成する。

【００１９】

本技術においては、半導体基板の画素分離部に形成されたトレンチの内部に第１遮光部を設けると共に、その第１遮光部の入射面側に第２遮光部を設ける。ここでは、画素領域の中心よりも周辺において、第２遮光部の中心が、画素分離部の中心に対して、画素領域

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の周辺の側へ多くシフトするように、第２遮光部を形成する。つまり、すくなくとも第２遮光部について「瞳補正」を実施する。

【発明の効果】

【００２０】

本技術によれば、撮像画像の画像品質等を向上可能な、固体撮像装置、および、その製造方法、電子機器を提供することができる。

【図面の簡単な説明】

【００２１】

【図１】図１は、実施形態１において、カメラの構成を示す構成図である。

【図２】図２は、実施形態１において、固体撮像装置の全体構成を示す図である。

【図３】図３は、実施形態１において、固体撮像装置の要部を示す図である。

【図４】図４は、実施形態１において、固体撮像装置の要部を示す図である。

【図５】図５は、実施形態１において、固体撮像装置の要部を示す図である。

【図６】図６は、実施形態１において、固体撮像装置の要部を示す図である。

【図７】図７は、実施形態１において、固体撮像装置の要部を示す図である。

【図８】図８は、実施形態１において、撮像を実施する際に、画素Ｐの画素トランジスタＴｒへ送信する制御信号を示すタイミングチャートである。

【図９】図９は、実施形態１において、固体撮像装置の製造方法を示す図である。

【図１０】図１０は、実施形態１において、固体撮像装置の製造方法を示す図である。

【図１１】図１１は、実施形態１において、固体撮像装置の製造方法を示す図である。

【図１２】図１２は、実施形態１において、固体撮像装置の製造方法を示す図である。

【図１３】図１３は、実施形態１において、固体撮像装置の製造方法を示す図である。

【図１４】図１４は、実施形態１において、固体撮像装置に入射光が入射する様子を示す断面図である。

【図１５】図１５は、実施形態２において、固体撮像装置の要部を示す図である。

【図１６】図１６は、実施形態２において、固体撮像装置に入射光が入射する様子を示す断面図である。

【図１７】図１７は、実施形態３において、固体撮像装置の要部を示す図である。

【図１８】図１８は、実施形態３において、固体撮像装置に入射光が入射する様子を示す断面図である。

【図１９】図１９は、実施形態４において、固体撮像装置の要部を示す図である。

【図２０】図２０は、実施形態４において、固体撮像装置の要部を示す図である。

【図２１】図２１は、実施形態５において、固体撮像装置の要部を示す図である。

【図２２】図２２は、実施形態６において、固体撮像装置の要部を示す図である。

【図２３】図２３は、実施形態７において、固体撮像装置の要部を示す図である。

【図２４】図２４は、実施形態８において、固体撮像装置の要部を示す図である。

【図２５】図２５は、実施形態９において、固体撮像装置の要部を示す図である。

【発明を実施するための形態】

【００２２】

実施形態について、図面を参照して説明する。

【００２３】

なお、説明は、下記の順序で行う。

１．実施形態１（画素分離部の遮光膜の上部を「瞳補正」する場合）

２．実施形態２（画素分離部の遮光膜の上部を「瞳補正」する場合）

３．実施形態３（画素分離部の遮光膜の上部を「瞳補正」する場合）

４．実施形態４（画素分離部に拡散層を設ける場合）

５．実施形態５（画素分離部の遮光膜の上部および下部を「瞳補正」する場合）

６．実施形態６（画素分離部の遮光膜の上部および下部を「瞳補正」する場合）

７．実施形態７（画素分離部の遮光膜の上部および下部を「瞳補正」する場合）

８．実施形態８（画素分離部の遮光膜を貫通させる場合）

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９．実施形態９（画素分離部の遮光膜を貫通させる場合）
１０．その他
【００２４】
＜１．実施形態１＞
（Ａ）装置構成
（Ａ－１）カメラの要部構成
図１は、実施形態１において、カメラの構成を示す構成図である。
【００２５】
図１に示すように、カメラ４０は、固体撮像装置１と、光学系４２と、制御部４３と、信号処理部４４とを有する。
【００２６】
カメラ４０において、固体撮像装置１は、光学系４２を介して被写体像として入射する入射光Ｈを撮像面ＰＳで受光し光電変換して信号電荷を生成する。ここでは、固体撮像装置１は、制御部４３から出力される制御信号に基づいて駆動し、生成した信号電荷を読み出して、電気信号を出力する。
【００２７】
光学系４２は、結像レンズや絞りなどの光学部材を含み、入射光Ｈを、固体撮像装置１の撮像面ＰＳへ集光するように配置されている。
【００２８】
制御部４３は、各種の制御信号を固体撮像装置１と信号処理部４４とに出力し、固体撮像装置１と信号処理部４４とを制御して駆動させる。
【００２９】
信号処理部４４は、固体撮像装置１から出力された電気信号をローデータとして信号処理を実施することによって、被写体像についてデジタル画像を生成するように構成されている。
【００３０】
本実施形態では、図１に示すように、撮像面ＰＳの中心部分においては、光学系４２から出射される光線Ｈ１が、撮像面ＰＳに対して垂直な角度で、入射光Ｈとして入射する。一方で、撮像面ＰＳの周辺部分においては、主光線Ｈ２が、撮像面ＰＳに対して垂直な方向に対して傾斜した角度で、入射光Ｈとして入射する。ここでは、撮像面ＰＳの中心から周囲へ向かって入射光の主光線Ｈ２が傾斜する。これは、後述の光学系４２を構成する絞りによって形成される射出瞳距離が有限であることに起因する。
【００３１】
（Ａ－２）固体撮像装置の要部構成
固体撮像装置１の全体構成について説明する。
【００３２】
図２は、実施形態１において、固体撮像装置の全体構成を示す図である。
【００３３】
本実施形態の固体撮像装置１は、ＣＭＯＳ型イメージセンサであり、図２に示すように、半導体基板１０１を含む。半導体基板１０１においては、たとえば、単結晶シリコン基板が薄膜化されたものであり、画素領域ＰＡと、周辺領域ＳＡとが面に設けられている。
【００３４】
画素領域ＰＡは、図２に示すように、矩形形状であり、複数の画素Ｐが水平方向ｘと垂直方向ｙとのそれぞれに等間隔で配置されている。つまり、画素Ｐがマトリクス状に並んでいる。
【００３５】
画素領域ＰＡにおいて、画素Ｐは、入射光を受光して信号電荷を生成するように構成されている。そして、その生成した信号電荷が、画素トランジスタ（図示なし）によって読み出されて電気信号として出力される。画素Ｐの詳細な構成については、後述する。
【００３６】

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周辺領域ＳＡは、図２に示すように、画素領域ＰＡの周囲に位置している。そして、この周辺領域ＳＡにおいては、周辺回路が設けられている。

【００３７】

具体的には、図２に示すように、垂直駆動回路１３と、カラム回路１４と、水平駆動回路１５と、外部出力回路１７と、タイミングジェネレータ（ＴＧ）１８と、シャッター駆動回路１９とが、周辺回路として設けられている。

【００３８】

垂直駆動回路１３は、図２に示すように、周辺領域ＳＡにおいて、画素領域ＰＡの側部に設けられており、画素領域ＰＡの画素Ｐを行単位で選択して駆動させるように構成されている。

【００３９】

カラム回路１４は、図２に示すように、周辺領域ＳＡにおいて、画素領域ＰＡの下端部に設けられており、列単位で画素Ｐから出力される信号について信号処理を実施する。ここでは、カラム回路１４は、ＣＤＳ（Ｃｏｒｒｅｌａｔｅｄ Ｄｏｕｂｌｅ Ｓａｍｐｌｉｎｇ；相関二重サンプリング）回路（図示なし）を含み、固定パターンノイズを除去する信号処理を実施する。

【００４０】

水平駆動回路１５は、図２に示すように、カラム回路１４に電気的に接続されている。水平駆動回路１５は、たとえば、シフトレジスタを含み、カラム回路１４において画素Ｐの列ごとに保持されている信号を、順次、外部出力回路１７へ出力させる。

【００４１】

外部出力回路１７は、図２に示すように、カラム回路１４に電気的に接続されており、カラム回路１４から出力された信号について信号処理を実施後、外部へ出力する。外部出力回路１７は、ＡＧＣ（Ａｕｔｏｍａｔｉｃ Ｇａｉｎ Ｃｏｎｔｒｏｌ）回路１７ａとＡＤＣ回路１７ｂとを含む。外部出力回路１７においては、ＡＧＣ回路１７ａが信号にゲインをかけた後に、ＡＤＣ回路１７ｂがアナログ信号からデジタル信号へ変換して、外部へ出力する。

【００４２】

タイミングジェネレータ１８は、図２に示すように、垂直駆動回路１３、カラム回路１４、水平駆動回路１５，外部出力回路１７，シャッター駆動回路１９のそれぞれに電気的に接続されている。タイミングジェネレータ１８は、各種のタイミング信号を生成し、垂直駆動回路１３、カラム回路１４、水平駆動回路１５，外部出力回路１７，シャッター駆動回路１９に出力することで、各部について駆動制御を行う。

【００４３】

シャッター駆動回路１９は、画素Ｐを行単位で選択して、画素Ｐにおける露光時間を調整するように構成されている。

【００４４】

（Ａ－３）固体撮像装置の詳細構成

本実施形態にかかる固体撮像装置の詳細内容について説明する。

【００４５】

図３～図７は、実施形態１において、固体撮像装置の要部を示す図である。

【００４６】

図３は、画素Ｐの断面図である。図３では、図２に示す画素領域ＰＡの中心部分に配置された一の画素であって，Ｘ１－Ｘ２部分を示している。

【００４７】

図４は、画素Ｐの上面図であり、図２に示す画素領域ＰＡの中心部分に配置された４つの画素Ｐを示している。図４では、説明の都合で、破線などの実線以外の線を用いて、各部材を示している部分がある。

【００４８】

図５は、画素分離部３０１の断面図である。図６は、画素分離部３０１の上面図である

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。図５，図６において、（ａ）は、図２に示す画素領域ＰＡの中心部分に配置された画素Ｐの間の画素分離部３０１であって、ＸＩＣ－Ｘ２Ｃ部分を示している。これに対して、（ｂ）は、図２に示す画素領域ＰＡの周辺部分に配置された画素Ｐの間の画素分離部３０１であって、ＸＩＳ－Ｘ２Ｓ部分を示している。つまり、図５，図６では、水平方向ｘに並ぶ一対の画素Ｐの間に設けられた画素分離部３０１を示している。図示を省略しているが、垂直方向ｙに並ぶ一対の画素Ｐの間に設けられた画素分離部３０１についても、図５，図６と同様な形態で設けられている。

【００４９】

また、図７は、画素Ｐの回路構成を示している。

【００５０】

図３に示すように、固体撮像装置１は、半導体基板１０１の内部にフォトダイオード２１が設けられている。ここでは，薄膜化された単結晶シリコンの半導体基板１０１に設けられている。

【００５１】

半導体基板１０１の裏面（図３では上面）には、カラーフィルタＣＦ、マイクロレンズＭＬなどの部材が設けられている。

【００５２】

これに対して、半導体基板１０１の表面（図３では、下面）には、図３では図示していないが，図７に示す画素トランジスタＴｒが設けられている。そして、図３に示すように、その画素トランジスタＴｒを被覆するように配線層１１１が設けられており，配線層１１１において、半導体基板１０１の側に対して反対側の面には、支持基板ＳＳが設けられている。

【００５３】

つまり、本実施形態の固体撮像装置１は、「裏面照射型ＣＭＯＳイメージセンサ」であって、裏面（上面）側から入射する入射光Ｈを、フォトダイオード２１が受光し、カラー画像を撮像によって生成するように構成されている。

【００５４】

各部の詳細について順次説明する。

【００５５】

（ａ）フォトダイオード２１について

固体撮像装置１において、フォトダイオード２１は、図２に示した複数の画素Ｐに対応するように、複数が画素領域ＰＡに配置されている。つまり、撮像面（ｘｙ面）において、水平方向ｘと、この水平方向ｘに対して直交する垂直方向ｙとのそれぞれに並んで設けられている。

【００５６】

フォトダイオード２１は、入射光Ｈを受光面ＪＳで受光し光電変換することによって信号電荷を生成して蓄積するように、複数が半導体基板１０１の内部に間を隔てて設けられている。

【００５７】

ここでは、図３に示すように，半導体基板１０１の裏面（図３では上面）側から入射する入射光Ｈをフォトダイオード２１が受光する。フォトダイオード２１の上方には、図３に示すように、平坦化膜ＨＴ，カラーフィルタＣＦ，マイクロレンズＭＬが設けられており、各部を順次介して入射した入射光Ｈを、受光面ＪＳで受光して光電変換が行われる。

【００５８】

図３に示すように、フォトダイオード２１は、半導体基板１０１内に設けられている。

【００５９】

たとえば、フォトダイオード２１は、ｎ型半導体領域１０１ｎが，電荷（ここでは、電子）を蓄積する電荷蓄積領域として形成されている。フォトダイオード２１においては、ｎ型半導体領域１０１ｎは、半導体基板１０１のｐ型半導体領域１０１ｐａ，１０１ｐｃの内部に設けられている。ここでは、ｎ型半導体領域１０１ｎにおいて、半導体基板１０

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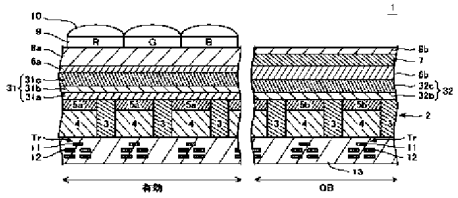
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(54)【発明の名称】固体撮像素子、固体撮像素子の製造方法および撮像装置

(57)【要約】
【課題】暗電流を抑制することができる固体撮像素子を提供する。
【解決手段】固体撮像素子は、光電変換が行われるフォトダイオードが形成された有効領域と、遮光膜により遮光された光学的黒領域とが形成された半導体基板と、前記有効領域上であって、負の固定電荷を有する層が少なくとも１層以上積層された第１の膜と、前記遮光領域上であって、負の固定電荷を有する層が少なくとも１層以上積層された第２の膜と、を備え、前記第１の膜が有する層の数が前記第２の膜が有する層の数と異なる。
【選択図】図１



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【特許請求の範囲】
【請求項１】
光電変換が行われるフォトダイオードが形成された有効領域、および遮光膜により遮光された光学的黒領域が形成された半導体基板と、
前記有効領域上であって、負の固定電荷を有する層が少なくとも１層以上積層された第１の膜と、
前記遮光領域上であって、負の固定電荷を有する層が少なくとも１層以上積層された第２の膜と、を備え、
前記第１の膜が有する層の数が前記第２の膜が有する層の数と異なる
固体撮像素子。
【請求項２】
前記第１の膜は、
前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、
前記第１層上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第２層と、
前記第２層上に、物理的気相成長を用いて形成された第３層と、を有し、
前記第２の膜は、
前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、
前記第１層上に、物理的気相成長を用いて形成された第２層と、を有する
請求項１に記載の固体撮像素子。
【請求項３】
前記第１の膜は、
前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、
前記第１層上に、物理的気相成長を用いて形成された第２層と、有し、
前記第２の膜は、
前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、
前記第１層上に、物理的気相成長を用いて形成された第２層と、
前記第２層上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第３層と、を有する
請求項１に記載の固体撮像素子。
【請求項４】
前記第１の膜は、
前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、
前記第１層上に、物理的気相成長を用いて形成された第２層と、
前記第２層上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第３層と、を有し、
前記第２の膜は、
前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層を有する
請求項１に記載の固体撮像素子。
【請求項５】
前記第１の膜および前記第２の膜を構成する層は、酸化ハフニウム膜、酸化アルミニウム膜、酸化ジルコニウム膜、酸化タンタル膜および酸化チタン膜のうちいずれかの１つの膜からなる
請求項１～４のいずれか１項に記載の固体撮像素子。

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【請求項６】
半導体基板に、光電変換が行われるフォトダイオードが形成された有効領域および遮光膜により遮光された光学的黒領域を形成する工程と、
前記有効領域上に負の固定電荷を有する層が少なくとも１層以上積層された第１の膜を形成する工程と、
前記遮光領域上に、負の固定電荷を有する層が少なくとも１層以上積層され、前記第１の膜が有する層の数とは異なる数の層を有する第２の膜を形成する工程と、を有する
固体撮像素子の製造方法。
【請求項７】
請求項１～５のいずれか１項に記載の固体撮像素子と、
前記固体撮像素子に被写体像を結像する光学系と、
前記固体撮像素子を駆動させる駆動パルスを生成する駆動部と、
前記固体撮像素子の出力画像信号を処理する信号処理回路と、を備える
撮像装置。
【発明の詳細な説明】
【技術分野】
【０００１】
本開示は、固体撮像素子、固体撮像素子の製造方法および撮像装置に関する。
【背景技術】
【０００２】
ＣＣＤ（Ｃｈａｒｇｅ Ｃｏｕｐｌｅｄ Ｄｅｖｉｃｅ）型やＣＭＯＳ（Ｃｏｍｐｌｅｍｅｎｔａｒｙ Ｍｅｔａｌ Ｏｘｉｄｅ Ｓｅｍｉｃｏｎｄｕｃｔｏｒ）型の固体撮像素子では、フォトダイオードにおける結晶欠陥や、半導体基板に形成された受光部とその上の絶縁層との界面における界面準位が、暗電流の原因となることが知られている。
【０００３】
そこで、暗電流の発生を抑制する技術として、半導体基板の全面、例えば、受光画素領域(以下、「有効領域」という)および光学的黒領域（以下、「ＯＢ領域」という）上に、負の固定電荷を持つ膜を形成する技術が提案されている。この技術では、半導体基板上に負の固定電荷を持つ膜を形成し、受光部と絶縁層との界面付近に正電荷（ホール）を蓄積することで、界面準位に起因する暗電流の発生を抑制している。
【先行技術文献】
【特許文献】
【０００４】
【特許文献１】特開２０１０－２３９１１６号公報
【発明の概要】
【発明が解決しようとする課題】
【０００５】
しかしながら、界面準位に起因する暗電流は、有効領域とＯＢ領域とでは、その案電流量が異なる。従って、上述した負の固定電荷を有する膜を半導体基板の全面に形成する場合には、全体的な暗電流量は低減するものの、有効領域とＯＢ領域との暗電流差が発生し、いわゆるＯＢ段差が発生することが問題となっている。
【０００６】
かかる問題に鑑みて、本発明は、有効領域における暗電流と光学的黒領域における暗電流との差を小さくすることができ、いわゆるＯＢ段差を改善することができる固体撮像素子、固体撮像素子の製造方法および撮像装置を提供するものである。
【課題を解決するための手段】
【０００７】
そこで、本開示の固体撮像素子は、光電変換が行われるフォトダイオードが形成された有効領域と、遮光膜により遮光された光学的黒領域とが形成された半導体基板と、前記有効領域上であって、負の固定電荷を有する層が少なくとも１層以上積層された第１の膜と

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、前記遮光領域上であって、負の固定電荷を有する層が少なくとも１層以上積層された第２の膜と、を備え、前記第１の膜が有する層の数が前記第２の膜が有する層の数と異なるものである。

【０００８】

また、本開示の固体撮像素子においては、前記第１の膜は、前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、前記第１層上に、前記原子層蒸着法または前記有機金属化学的気相成長法を用いて形成された第２層と、前記第２層上に、物理的気相成長を用いて形成された第３層と、を有し、前記第２の膜は、前記半導体基板上に、前記原子層蒸着法または前記有機金属化学的気相成長法を用いて形成された第１層と、前記第１層上に、前記物理的気相成長を用いて形成された第２層と、を有するものである。

【０００９】

また、本開示の固体撮像素子においては、前記第１の膜は、前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、前記第１層上に、物理的気相成長を用いて形成された第２層と、有し、前記第２の膜は、前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、前記第１層上に、物理的気相成長を用いて形成された第２層と、前記第２層上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第３層と、を有するものである。

【００１０】

また、本開示の固体撮像素子においては、前記第１の膜は、前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層と、前記第１層上に、物理的気相成長を用いて形成された第２層と、前記第２層上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第３層と、を有し、前記第２の膜は、前記半導体基板上に、原子層蒸着法または有機金属化学的気相成長法を用いて形成された第１層を有するものである。

【００１１】

また、本開示の固体撮像素子においては、前記第１の膜および前記第２の膜を構成する層は、酸化ハフニウム膜、酸化アルミニウム膜、酸化ジルコニウム膜、酸化タンタル膜および酸化チタン膜のうちいずれかの１つの膜からなるものである。

【００１２】

また、本開示の固体撮像素子の製造方法は、半導体基板に、光電変換が行われるフォトダイオードが形成された有効領域および遮光膜により遮光された光学的黒領域を形成する工程と、前記有効領域上に負の固定電荷を有する層が少なくとも１層以上積層された第１の膜を形成する工程と、前記遮光領域上に、負の固定電荷を有する層が少なくとも１層以上積層され、前記第１の膜が有する層の数とは異なる数の層を有する第２の膜を形成する工程と、を有するものである。

【００１３】

また、本開示の撮像装置は、前記固体撮像素子と、前記固体撮像素子に被写体像を結像する光学系と、前記固体撮像素子を駆動させる駆動パルスを生成する駆動部と、前記固体撮像素子の出力画像信号を処理する信号処理回路と、を備えるものである。

【発明の効果】

【００１４】

本開示によれば、有効領域における暗電流と光学的黒領域における暗電流との差を小さくすることができ、いわゆるＯＢ段差を改善することができる。

【図面の簡単な説明】

【００１５】

【図１】本開示の実施形態に係る固体撮像素子の断面構造を示す図である。

【図２】負の固定電荷を有する膜の膜厚と暗電流量との関係図である。

【図３】本開示の実施形態に係る固体撮像素子の製造方法を示す図である。

【図４】本開示の実施形態に係る固体撮像素子を備えた撮像装置の構成を示す図である。

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【図５】変形例１係る固体撮像素子の断面構造を示す図である。
【図６】変形例１係る固体撮像素子の製造方法を示す図である。
【図７】負の固定電荷を有する膜の膜厚と暗電流量との関係図である。
【図８】変形例２係る固体撮像素子の断面構造を示す図である。
【図９】変形例２係る固体撮像素子の製造方法を示す図である。
【図１０】負の固定電荷を有する膜の膜厚と暗電流量との関係図である。
【発明を実施するための形態】
【００１６】
本開示に係る固体撮像素子では、固体撮像素子の半導体基板におけるフォトダイオードが形成された有効領域上に、負の固定電荷を有する第１の膜（以下、「第１の膜」という）を形成し、遮光膜により遮光された光学的黒領域上に、第１の膜とは積層される層の数が異なる負の固定電荷を有する第２の膜（以下、「第２の膜」という）を形成する。
【００１７】
第１の膜は、例えば、半導体基板上に形成された第１層と、この第１層上に形成された第２層と、この第２層上に形成された第３層とにより構成される。
【００１８】
第１の膜を構成する第１層および第２層は、ＡＬＤ（Atomic Layer Deposition；原子層蒸着）法またはＭＯＣＶＤ（Metal Organic Chemical Vapor Deposition；有機金属化学的気相成長）法を用いて形成する。また、第１の膜を構成する第３層は、ＰＶＤ（Physical Vapor Deposition；物理的気相成長）法により形成する。
【００１９】
また、第２の膜は、例えば、半導体基板上に形成された第１層と、この第１層上に形成された第２層とにより構成される。第２の膜を構成する第１層は、ＡＬＤ法またはＭＯＣＶＤ法を用いて形成する。また、第２の膜を構成する第２層は、ＰＶＤ法により形成する。
【００２０】
第１の膜および第２の膜を構成する層の材料としては、例えば、酸化ハフニウム（HfO_2）、酸化アルミニウム（Al_2O_3）、酸化ジルコン（ZrO_2）、酸化タンタル（Ta_2O_5）および酸化チタン（TiO_2）等の酸化物が挙げられる。これらの酸化物の層は、絶縁ゲート型電界効果トランジスタのゲート絶縁膜等に用いられている実績があるため、形成方法が確立されており、容易に形成することができる。
【００２１】
また、これらの材料のうち、特に、屈折率の比較的高い、酸化ハフニウム（屈折率２．０５）、酸化タンタル（屈折率２．１６）、酸化チタン（屈折率２．２０）等を形成した場合には、反射防止効果をも得ることも可能になる。
【００２２】
上記以外の材料としては、例えば、希土類元素の酸化物が挙げられる。即ち、ランタン、プラセオジム、セリウム、ネオジム、プロメチウム、サマリウム、ユウロピウム、ガドリニウム、テルビウム、ジスプロシウム、ホルミウム、エルビウム、ツリウム、イッテルビウム、ルテチウム、イットリウムの各酸化物が挙げられる。
さらにまた、窒化ハフニウム、窒化アルミニウム、酸窒化ハフニウム、酸窒化アルミニウムを使用することも可能である。
【００２３】
負の固定電荷を有する第１層、第２層、第３層に、絶縁性を損なわない範囲で、層中にシリコン（Ｓｉ）や窒素（Ｎ）が添加されていてもよい。その場合、シリコンや窒素の濃度は、層の絶縁性が損なわれない範囲で適宜決定される。このように、シリコンや窒素が添加されることによって、各層の耐熱性やプロセスの中でのイオン注入の阻止能力を上げることが可能になる。
【００２４】
第１の膜を構成する第１層および第２層、および第２の膜を構成する第１層は、上述の

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とおり、ＡＬＤ法またはＭＯＣＶＤ法を用いて形成する。ＡＬＤ法により第１の膜を形成する場合には、例えば、基板温度が２００～５００℃、プリカーサの流量が１０～５００ｓｃｃｍ、プリカーサの照射時間が１～１５秒、O_3の流量が５～５０ｓｃｃｍの条件とする。また、ＭＯＣＶＤ法により第１の膜を形成する場合には、例えば、基板温度が２００～６００℃の条件とする。

【００２５】

なお、半導体基板がシリコン層であり、その上に第１の膜を構成する第１層や第２の膜を構成する第１層をＡＬＤ法により形成した場合には、同時に、シリコン層の表面に界面準位を低減する酸化シリコン膜を厚さ１ｎｍ程度形成することが可能になる。

【００２６】

第１の膜を構成する第２層は、上述のとおり、ＡＬＤ法またはＭＯＣＶＤ法を用いて形成する。ＡＬＤ法により、第１の膜を構成する第２層を形成する場合には、例えば、基板温度が２００～５００℃、プリカーサの流量が１０～５００ｓｃｃｍ、プリカーサの照射時間が１～１５秒、O_3の流量が５～５０ｓｃｃｍの条件とする。また、ＭＯＣＶＤ法により、第１の膜を構成する第２層を形成する場合には、例えば、基板温度が２００～６００℃の条件とする。

【００２７】

また、第１の膜を構成する第３層および第２の膜を構成する第２層は、上述のとおり、ＰＶＤ法を用いて形成する。ＰＶＤ法により、第１の膜を構成する第３層、および第２の膜を構成する第２層を形成する際には、例えば、圧力が０．０１～５０Ｐａ、パワーが５００～２０００Ｗ、Ａｒの流量が５～５０ｓｃｃｍ、O_2の流量が５～５０ｓｃｃｍの条件とする。

【００２８】

ＰＶＤ法により、第１の膜を構成する第３層、および第２の膜を構成する第２層を形成するので、ＡＬＤ法やＭＯＣＶＤ法と比較して形成速度が速くなり、比較的短い時間で、ある程度厚い膜を形成することが可能になる。

【００２９】

第１の膜を構成する第２層の膜厚、および第２の膜を構成する第１層の膜厚は、特に限定されないが、第１の膜を構成する第３層、および第２の膜を構成する第２層をＰＶＤ法により形成する際に半導体基板にダメージを与えることがないように、第１の膜を構成する第２層、および第２の膜を構成する第１層にはある程度以上の厚さが必要である。好ましくは、第１の膜の膜厚を１ｎｍ以上とする。

また、第１の膜を構成する第２層、および第２の膜を構成する第１層は、ＡＬＤ法またはＭＯＣＶＤ法によって形成するため、厚く形成するには時間がかかる。そのため、第１の膜を構成する第２層および第２の膜を構成する第１層の厚さは、５ｎｍ程度以下とすることが好ましい。

【００３０】

本開示に係る固体撮像素子では、有効領域上にて第１層上に第２層を形成し、さらに、第２層上に第３層を形成する第１の膜を備えているため、３つの層を合わせて、充分な負バイアス効果が得られる。また、ＯＢ領域上にて第１層上に第２層を形成する第２の膜を備えているため、２つの層を合わせて、充分な負バイアス効果が得られる。

【００３１】

特に、有効領域における第１の膜と、ＯＢ領域における第２の膜との膜構造を異なるようにしたため、有効領域における暗電流とＯＢ領域における暗電流の差を小さくして、いわゆるＯＢ段差を改善することができる。また、暗電流量の負の固定電荷を有する膜厚依存性により、各固体撮像素子の暗電流量に合わせて膜厚を調整することでＯＢ段差を調整することもできる。

【００３２】

また、有効領域における第１の膜とＯＢ領域における第２の膜の膜厚を個別に変更することができるため、第１の膜側から受光する場合では、受光画素部は負の固定電荷を有す

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る膜を反射防止膜としての最適膜厚を選択できる。

【００３３】

また、ＯＢ領域においては、光の入射を考慮する必要がないため反射防止膜的な効果から離れ暗電流改善のみで第２の膜の膜厚を調整することができる。

【００３４】

また、第１の膜を構成する第２層および第２の膜を構成する第１層をＡＬＤ法またはＭＯＣＶＤ法を用いて形成するので、第１の膜を構成する第２層および第２の膜を構成する第１層を形成する際に半導体基板にダメージを与えないようにすることができる。

【００３５】

上述したように、本開示によれば、第１の膜の膜厚と、第２の膜の膜厚とを個別に調整することができる。これにより、第１の膜の膜厚を、反射防止膜としての機能を発揮する最適な膜厚にすることができる。

【００３６】

さらに、光学的黒領域には光が入射しないため、第２の膜が反射防止膜としての機能を有する必要がないため、暗電流を改善するための最適な膜厚にすることができる。

【００３７】

以下に、本開示の実施形態に係る固体撮像素子について、図面を参照して説明する。各図において、同一の構成要素には同一の符号を付してある。なお、説明は以下の順序で行う。

１．固体撮像素子の構成
２．固体撮像素子の製造方法
３．撮像装置の構成等
４．その他の固体撮像素子の構成及び製造方法

【００３８】

〔１．固体撮像素子の構成〕

まず、本実施形態に係る固体撮像素子１の構成について、図１を参照して説明する。図１は、本実施形態に係る固体撮像素子の断面構造を示す図である。なお、本実施形態では、本発明を、いわゆる裏面照射型のＣＭＯＳ固体撮像素子（ＣＭＯＳイメージセンサ）に適用した例について説明する。

【００３９】

固体撮像素子１は、半導体基板２における有効領域２１およびＯＢ領域２２に、入射光を光電変換する受光部として、フォトダイオードとなる電荷蓄積領域４が、Ｎ型の不純物領域によって形成されている。この電荷蓄積領域４の表面には、正電荷蓄積領域５が形成されており、これら電荷蓄積領域４および正電荷蓄積領域５によって、ＨＡＤ（Hole-Accumulation Diode sensor）構造が構成されている。なお、それぞれの電荷蓄積領域４および正電荷蓄積領域５は、素子分離領域３により分離されている。

【００４０】

半導体基板２の表面側においては、半導体基板２の電荷蓄積領域４の下方に、ＭＯＳトランジスタＴｒのゲート電極１１が形成され、さらに下方に金属配線による配線層１２が形成されている。

【００４１】

ゲート電極１１および各層の配線層１２の間は、層間の絶縁層１３によって絶縁されている。なお、絶縁層１３は、図示しないが、下方に設けられる支持基板等によって支持されている。

【００４２】

電荷蓄積領域４を有するフォトダイオードによって、それぞれの画素が構成される。各画素には、図示のＭＯＳトランジスタ（この場合は、電荷蓄積領域４に蓄積した電荷を読み出し・転送する転送トランジスタ）Ｔｒを含む、１個以上のトランジスタを有して構成される。

【００４３】

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各画素の電荷蓄積領域４の間は、Ｐ型の素子分離領域３により分離されている。なお、図示しないが、電荷蓄積領域４のＭＯＳトランジスタＴｒのゲート電極１１側の界面に、ｐ＋半導体領域を形成して、絶縁層１３との界面における暗電流の発生を抑制することが好ましい。

【００４４】

半導体基板２の裏面側において、有効領域２１の上層には、負の固定電荷を有する第１の膜（以下、「第１の膜」という）３１が形成されている。この第１の膜３１は、半導体基板２上に形成された第１層３１ａと、この第１層３１ａ上に形成された第２層３１ｂと、この第２層３１ｂ上に形成された第３層３１ｃとが積層された構成を有する。

【００４５】

第１層３１ａは、例えば、酸化ハフニウム膜、酸化アルミニウム膜、酸化ジルコニウム膜、酸化タンタル膜および酸化チタン膜のうちいずれかの１つの膜を有し、ＡＬＤ法またはＭＯＣＶＤ法により形成される。

【００４６】

また、第２層３１ｂは、例えば、酸化ハフニウム膜、酸化アルミニウム膜、酸化ジルコニウム膜、酸化タンタル膜および酸化チタン膜のうちいずれかの１つの膜を有し、ＡＬＤ法またはＭＯＣＶＤ法により形成される。

第１層３１ａ、第２層３１ｂは、いずれもＡＬＤ法又はＭＯＣＶＤ法で形成されるため、第１層３１ａ、第２層３１ｂをあわせてＡＬＤ層とも称する。

【００４７】

また、第３層３１ｃは、例えば、酸化ハフニウム膜、酸化アルミニウム膜、酸化ジルコニウム膜、酸化タンタル膜および酸化チタン膜のうちいずれかの１つの膜を有し、ＰＶＤ法により形成される。従って、第３層３１ｃをＰＶＤ層とも称する。

【００４８】

このように、有効領域２１の上層に負の固定電荷を有する第１層３１ａ、第２層３１ｂ、第３層３１ｃが積層された第１の膜３１を形成している。第１の膜３１の中の負の固定電荷によって、電荷蓄積領域４の表面に電界が加わり、電荷蓄積領域４の表面に正電荷蓄積領域５が形成される。これにより、電荷蓄積領域４の表面にイオン注入をしなくても、正電荷蓄積領域５を形成することが可能になる。

【００４９】

第１の膜３１上には、例えば酸化シリコン（SiO_2）膜からなる絶縁膜６ａが形成されており、この絶縁膜６ａの上には、平坦化膜８ａが形成されている。また、平坦化膜８ａの上には、画素毎に、対応する色（赤Ｒ、緑Ｇ、青Ｂ）のカラーフィルタ９が形成されており、各カラーフィルタ９の上には、それぞれ、集光のためのオンチップレンズ１０が設けられている。

【００５０】

ＯＢ領域２２の上層には、負の固定電荷を有する第２の膜（以下、「第２の膜」という）３２が形成されている。この第２の膜３２は、半導体基板２上に形成された第１層３２ｂと、この第１層３２ｂ上に形成された第２層３２ｃとが積層された構成を有する。

【００５１】

第１層３２ｂは、例えば、酸化ハフニウム膜、酸化アルミニウム膜、酸化ジルコニウム膜、酸化タンタル膜および酸化チタン膜のうちいずれかの１つの膜を有し、ＡＬＤ法またはＭＯＣＶＤ法により形成される。従って、第１層３２ｂをＡＬＤ層とも称する。

【００５２】

第２層３２ｃは、例えば、酸化ハフニウム膜、酸化アルミニウム膜、酸化ジルコニウム膜、酸化タンタル膜および酸化チタン膜のうちいずれかの１つの膜を有し、ＰＶＤ法により形成される。従って、第２層３２ｃをＰＶＤ層とも称する。

【００５３】

このように、ＯＢ領域２２の上層に、負の固定電荷を有する第１層３２ｂ及び第２層３２ｃが積層された第２の膜３２を形成しているため、この第２の膜３２の中の負の固定電

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荷によって、電荷蓄積領域４の表面に電界が加わり、電荷蓄積領域４の表面に正電荷蓄積領域５が形成される。これにより、電荷蓄積領域４の表面にイオン注入をしなくても、正電荷蓄積領域５を形成することが可能になる。

【００５４】

第２の膜３２上には、例えば酸化シリコン膜からなる絶縁膜６ｂが形成されており、この絶縁膜６ｂの上には、ＯＢ領域２２を覆うように、遮光膜７が形成されている。この遮光膜７によって、フォトダイオードに光が入らない領域（図示しないオプティカルブラック領域）を作り、そのフォトダイオードの出力によって画像での黒レベルを決定することができる。

【００５５】

上述したように、第１の膜３１は３層の積層構造であり、第２の膜３２は２層の積層構造である。このように、固体撮像素子１は、第１の膜３１が有する層の数が第２の膜３２が有する層の数と異なる。本実施形態では、第１の膜３１が有する層の数は、第２の膜３２が有する層の数より多く、第１の膜３１の膜厚が第２の膜３２の膜厚より厚くなっている。ただし、第１の膜３１の膜厚と第２の膜３２の膜厚の差（段差）は数ｎｍ程度である。この程度の段差は、後述するように第１の膜３１及び第２の膜３２上に絶縁膜６や平坦化膜８を形成することで吸収することができるため、固体撮像素子１のカラーフィルタ９などを平らな膜上に形成することができる。

【００５６】

絶縁膜６ｂおよび遮光膜７を覆って、平坦化膜８ｂが形成されている。

【００５７】

本実施の形態の固体撮像素子１は、図１の上方から光が入射されると、フォトダイオードの電荷蓄積領域４において光を信号電荷に変換する光電変換が生じるため、入射光を受光検出することができる。そして、固体撮像素子１は、フォトダイオードが形成された半導体基板２から見て、下層にある配線層１２の側（表面側）とは反対側（裏面側）の上層から光を入射させる、いわゆる裏面照射型構造となっている。

【００５８】

特に、固体撮像素子１では、有効領域２１上に第１の膜３１を形成し、ＯＢ領域２２上に第２の膜３２を形成しているため、有効領域２１における暗電流の低減と、ＯＢ領域２２における暗電流の低減を個別に行うことができる。これにより、図７に示すように、有効領域２１とＯＢ領域２２における暗電流量差を低減することができ、いわゆるＯＢ段差の発生を抑制することができる。

【００５９】

本実施の形態の固体撮像素子１においては、特に、有効領域２１における第１の膜３１が、第１層３１ａと、その上の第２層３１ｂと、その上の第３層３１ｃとの３層の積層構造となっている。また、ＯＢ領域２２における第２の膜３２が、第１層３２ｂと、その上の第２層３２ｃとの２層の積層構造となっている。

【００６０】

第１の膜３１では、第１層３１ａおよび第２層３１ｂはＡＬＤ法またはＭＯＣＶＤ法により形成し、第３層３１ｃはＰＶＤ法により形成する。また、第２の膜３２では、第１層３２ｂはＡＬＤ法またはＭＯＣＶＤ法により形成し、第２層３２ｃはＰＶＤ法により形成する。

【００６１】

これら第１の膜３１を構成する第１層３１ａ、第２層３１ｂおよび第３層３１ｃの材料としては、例えば、酸化ハフニウム、酸化アルミニウム、酸化ジルコン、酸化タンタルおよび酸化チタンのうちいずれか一つの酸化物を使用することが可能である。また、上述した、窒化物や酸窒化物、希土類元素の酸化物等も、使用することが可能である。

【００６２】

また、第２の膜３２を構成する第１層３２ｂおよび第２層３２ｃの材料としては、例えば、酸化ハフニウム、酸化アルミニウム、酸化ジルコン、酸化タンタルおよび酸化チタン

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のうちいずれか１つの酸化物を使用することが可能である。また、上述した、窒化物や酸窒化物、希土類元素の酸化物等も、使用することが可能である。

【００６３】

半導体基板２の上層に、第１の膜３１および第２の膜３２を設けたことにより、界面付近に正電荷（ホール）が蓄積されるようにすることができる。なお、特に、第１の膜３１として、屈折率の比較的高い、酸化ハフニウム膜、酸化タンタル膜および酸化チタン等の酸化膜を形成した場合には、反射防止効果を得ることも可能になる。

【００６４】

図２に上述した負の固定電荷を有する膜３１，３２の膜厚に対する暗電流量の関係を示す。図２（ａ）は、ＡＬＤ層の厚さと暗電流量の関係を示す図であり、図２（ｂ）、（ｃ）は、ＰＶＤ層の厚さと暗電流量の関係を示す図である。図２（ｂ）、（ｃ）に示すように暗電流量は、ＰＶＤ層の膜厚には大きく依存せず、図２（ａ）に示すように、暗電流量は、ＡＬＤ層の厚さに依存する。

【００６５】

図２（ａ）に示すように、有効領域における暗電流量は、ＯＢ領域における暗電流量よりも大きい。また、第１の膜３１および第２の膜３２ともにＡＬＤ層の厚さを薄くすることで、暗電流量は減少する。これまでの固体撮像素子は、有効領域及びＯＢ領域のＡＬＤ層の厚さが等しくなるように半導体基板２上に膜が形成されていた。従って、有効領域とＯＢ領域の暗電流量の差（ＯＢ段差）は一定以上発生し、膜厚が大きくなるほどその差が大きくなっていた。

一方、本実施形態の固体撮像素子１は、暗電流量が大きい有効領域のＡＬＤ層の厚さを、ＯＢ領域のＡＬＤ層より厚くしている。そのため、有効領域における暗電流量と、ＯＢ領域における暗電流量との暗電流量差が減少する。

【００６６】

〔２．固体撮像素子の製造方法〕

次に、本実施の形態の固体撮像素子１の製造方法について説明する。図３は固体撮像素子１の製造方法を示す図である。なお、以下の説明は、有効領域２１の半導体基板２内に電荷蓄積領域４が形成されており、ＭＯＳトランジスタＴｒのゲート電極１１および配線層１２が形成されている状態から始めることとする。

【００６７】

まず、図３（ａ）に示すように、ＡＬＤ法またはＭＯＣＶＤ法により、半導体基板２の有効領域２１およびＯＢ領域２２上に、負の固定電荷を有する膜３３として酸化ハフニウム膜を形成する。なお、負の固定電荷を有する膜３３ａの材料としては、上述した酸化ハフニウム以外にも、例えば、酸化アルミニウム、酸化ジルコン、酸化タンタルおよび酸化チタンのうちいずれか１つの酸化物を用いることができる。

【００６８】

ＡＬＤ法で形成する場合の形成条件は、例えば、形成基板温度２００～５００℃、プリカーサ流量が１０～５００ｓｃｃｍ、照射時間１～１５秒、O_3流量１０～５００ｓｃｃｍ、とする。また、負の固定電荷を有する膜３３ａの膜厚は、好ましくは１ｎｍ以上である。

【００６９】

次に、図３（ｂ）に示すように、有効領域２１における負の固定電荷を有する膜３３ａ上にレジスト４０を形成した後、ウェットエッチングによりレジスト４０および露出している負の固定電荷を有する膜３３ａを除去する。これにより、図３（ｃ）に示すように、半導体基板２の有効領域２１上に、第１の膜３１を構成する第１層３１ａを形成する。

【００７０】

次に、図３（ｄ）に示すように、ＡＬＤ法またはＭＯＣＶＤ法により、第１層３１ａおよびＯＢ領域２２上に、負の固定電荷を有する膜３４として酸化ハフニウム膜を形成する。これにより、第１層３１ａ上に第２層３１ｂを形成し、ＯＢ領域２２上に第２の膜３２の第１層３２ｂを形成する。なお、負の固定電荷を有する膜３４の材料としては、上述し

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FABRICATING METHOD OF CMOS IMAGE SENSOR WITH REDUCED LOSS OF LIGHT

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DESCRIPTION KR20060020400

FIELD OF THE INVENTION [0001] The present invention relates to a CMOS image sensor,

FIG. 1A is a circuit diagram showing a unit pixel of a conventional CMOS image sensor,

1B shows a schematic structure of a conventional CMOS image sensor chip,

1C is a cross - sectional view illustrating a cross section of a pixel array portion and a logic region in a conventional CMOS image sensor,

FIGS. 2A to 2C are cross - sectional views illustrating a manufacturing process of a CMOS image sensor according to an exemplary embodiment of the present invention,

FIG. 2d is a plan view showing a state of a CMOS image sensor chip according to an embodiment of the present invention,

3 is a cross - sectional view showing a case where the technical idea of the present invention is applied to a unit pixel.

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Description of the Related Art [0002]

30 : Substrate 31: gate

32 : Spacer 33: Interlayer insulating film

34 : M1 contact 35: first metal wiring (M1)

36 : VIA 1 37, 39, 42: metal interlayer insulating film

38 : Second metal wiring (M2) 40: VIA 2

41 : Third metal wiring (M3) 43: VIA3

44 : Fourth metal wiring (M4) 45: mask

46 : Trench 47: oxide film

50 : Substrate 51: photodiode

52 : Gate 53: spacer

54 : Interlayer insulating film 55, 56: metal interlayer insulating film

57 : Oxide film

In particular, the present invention relates to a method of manufacturing a CMOS image sensor, in particular, an oxide film is buried in an edge region between a pixel array and

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a logic circuit to a depth of a second metal interconnection to receive light totally reflected by the oxide film back into the pixel array It is an invention that reduces the loss of light. Generally, an image sensor is a semiconductor device that converts an optical image into an electrical signal. Typical image sensor devices include a charge coupled device (CCD) and a CMOS image sensor. The charge - coupled device is a device in which individual MOS (Metal - Oxide - Silicon) capacitors are located in close proximity to each other and the charge carrier is stored and transferred to the capacitor. The Simos image sensor has a control circuit and a signal processing circuit (CMOS) technology that uses a signal processing circuit as a peripheral circuit to make MOS transistors as many as the number of pixels, and employs a switching system that sequentially detects the output using the MOS transistors. FIG. 1A is a circuit diagram showing a unit pixel composed of one photodiode PD and four MOS transistors in a conventional CMOS image sensor, which includes a photodiode 100 that receives light and generates photo charges, A transfer transistor 101 for transferring the photoelectrons collected in the photodiode 100 to the floating diffusion region 102; resetting the floating diffusion region 102 by setting the potential of the floating diffusion region to a desired value and discharging the charge; A drive transistor 104 having a gate to which a voltage of the floating diffusion region is applied to act as a source follower buffer amplifier and a switching transistor 104 serving as an addressing function And a select transistor 105 for performing the above operation. And a load transistor 106 is formed so that an output signal (Output Signal) can be read out of a unit pixel.

1B is a plan view showing an approximate view of a CMOS image sensor chip composed of a pixel array in which such a unit pixel is composed of several tens to millions of pixels, and a logic circuit portion and the like for processing image data. Referring to this, it can be seen that the logic circuit portion is arranged around the pixel array that receives the light. FIG. 1C is a cross - sectional view showing a cross section of a pixel array and a logic circuit portion together, and particularly, an interface between the pixel array and the logic circuit portion. FIG. First, in FIG. 1C, a pixel array region and a logic region are shown together. The pixel array region is a region where a light receiving portion composed of a photodiode or the like is formed. The logic region is a region where a general logic circuit for signal processing is mainly formed to be. That is, a gate electrode 12 having a spacer 13 is formed on a semiconductor substrate 11, and an interlayer insulating film 14 for insulation is formed on a substrate including a gate electrode. A metal contact 15 (M1 contact) for connecting the gate electrode 12 and the first metal interconnection 16 is formed on the gate electrode 12 through the interlayer insulating film 14. A first metal wiring 16 is patterned on the interlayer insulating film 14 and second to fourth metal wirings 18, 20 and 22 are stacked thereon. A metal wiring (Not shown) are provided for insulating the semiconductor substrate 1 from each other.

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Here, the metal interlayer insulating film typically has a structure in which an FSG film and a TEOS oxide film are stacked. 1C shows VIA 1 to VIA 3 for electrically connecting the respective metal wirings. Referring to FIG. 1C, it can be seen that in the conventional CMOS image sensor, the pixel array region is formed only up to the second metal interconnection (M2) 18, and the logic region is formed up to the fourth metal interconnection 22. In other words, in the pixel array region formed only up to the second metal wirings (M2) and (18), the oxide film series FGS film and the TEOS oxide film are formed in two layers to match the height of the fourth metal wiring in the logic region.

In the conventional image sensor having such a structure, the fourth metal wiring 22 of the logic region is formed of a shielding metal to surround the pixel array region, which is a boundary between the pixel array region and the logic region, And to reduce the loss of light incident on the edge of the region. However, according to the related art, the shielding metal using the fourth metal interconnection can not collect the incident light incident on the edge toward the pixel array, and has a disadvantage in that almost all of the incident light is lost due to the permittivity of the metal. SUMMARY OF THE INVENTION It is an object of the present invention to provide a method of manufacturing a CMOS image sensor in which light loss is reduced at an edge portion of a pixel array and a difference in light sensitivity between a center portion and an edge portion of the pixel array is reduced .

According to an aspect of the present invention, there is provided a method of manufacturing a CMOS image sensor having a pixel array region and a logic region, the method comprising: forming a second metal interconnection in the pixel array region and the logic region, Forming a fourth metal interconnection and forming an interlayer insulating film in the pixel array region; Etching the interlayer dielectric to form a trench of the second metal interconnection depth at an interface between the pixel array region and the logic region; And filling the trench with an oxide film having a refractive index lower than that of the interlayer insulating film. In the present invention, a film of an oxide film series is buried in the interface between the pixel array and the logic region to a depth of the second metal interconnection, and the incident light is totally reflected by the film of the oxide film series to be incident on the pixel array, The photosensitivity of the edge portion of the light emitting layer can be improved. DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings, so that those skilled in the art can easily carry out the technical idea of the present invention. FIGS. 2A to 2C are cross - sectional views illustrating a manufacturing process of a CMOS image sensor according to an

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embodiment of the present invention, and one embodiment of the present invention will be described with reference to FIG. First, the process up to the formation of the fourth metal interconnection 44 is the same as in the prior art. Referring to FIG. 1, an active layer and a field region defining a field region are formed on a semiconductor substrate having a pixel array region and a logic region. Such an element isolation film is not shown in FIG. 2A. Next, a photodiode is formed in the pixel array region. The photodiode is also not shown in FIG. 2A. Next, a gate electrode 31 having a spacer 32 is formed on a semiconductor substrate and a source / drain region (not shown) is formed. Next, an interlayer insulating film 33 is formed on the substrate 30 including the gate electrode 31, a certain portion of the interlayer insulating film 33 is removed, a conductive material is buried, and the gate electrode 31 and the first metal The metal contact 34 connecting the wiring 35 is formed.

Next, a first metal interlayer insulating film 37 is formed on the first metal interconnection 35, and then a first metal interconnection 37 is formed through the first metal interlayer insulating film 37 to connect the first metal interconnection and the second metal interconnection. Thereby forming a via (VIA 1) 36. Next, the second metal interconnection 38 is patterned on the first inter - metal - insulating film 37. Such a process proceeds in the same way in both the pixel array region and the logic region, but the subsequent process proceeds differently in the pixel array region and the logic region. That is, in the logic region, the process of sequentially stacking the third metal interconnection 41 and the fourth metal interconnection 44 proceeds. On the other hand, in the pixel array region, only the metal interlayer insulating films 39 and 42 are sequentially stacked, Wiring is not used. 2A, reference numerals 40 and 43 denote VIA 2 and VIA 3, respectively. After forming the fourth metal wirings 44 in this manner, the mask 45 is used to form the trench 46 at the interface between the pixel array region and the logic region. At this time, it is preferable that the depth of the trench is up to the second metal interconnection 38, and the depth of the trench is about 16000 in the 0.18 μ m class CMOS image sensor. Next, as shown in FIG. 2B, an oxide film 47 is deposited on the entire structure to fill the trench. Here, the oxide film 47 has a refractive index as low as about 1.41 and has a relatively lower refractive index than the metal interlayer insulating film on the pixel array side. Thus, in the embodiment of the present invention, the total light loss at the interface can be reduced through the total reflection using the oxide film 47. After the oxide film 47 is deposited, the etch - back process for the oxide film 47 is performed until the surface of the fourth metal interconnection 44 is exposed as shown in FIG. 2C. As a result, An oxide film remains in the form of a spacer, and the trench is buried with an oxide film. At this time, the thickness of the fourth metal interconnection is about 6500 ANGSTROM. Although not shown in FIG. 2C, conventional processes such as a passivation film, a color filter, and a microlens formation are performed to complete a CMOS image sensor.

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As a result, since an oxide film having a low refractive index is buried in the periphery of the pixel array, the light incident on the interface between the pixel array region and the logic region is totally reflected by the oxide film and re - enters the pixel array region. According to the present invention, it is possible to improve the photosensitivity at the edge portion of the pixel array and to reduce the difference in the photosensitivity between the center portion and the edge portion of the pixel array. FIG. 2D is a plan view showing a schematic view of a CMOS image sensor chip formed in accordance with an embodiment of the present invention. It can be seen that a low refractive index oxide film 47 is buried along the edge of the pixel array. 3 is a cross - sectional view showing a state in which the technical idea of the present invention is applied to a unit pixel. That is, FIG. 3 is a cross - sectional view showing one unit pixel as a center. Referring to FIG. First, formation of the second metal interconnection (M2) is the same as that of the first embodiment of the present invention. That is, the semiconductor substrate 50 is provided with a photodiode 51 for receiving light and converting it into an electric signal, and a gate electrode 52 having a spacer 53 is formed. An interlayer insulating film 54 is formed on the semiconductor substrate 50 including the gate electrode. On the interlayer insulating film, a first metal interconnection M 1 and a second metal interconnection M 2 laid out so as not to block the path of light incident on the photodiode, (M2) are formed. Reference numerals 54 and 55 denote metal interlayer insulating films. After the second metal interconnection line M2 is formed in this way, the upper part of the second metal interconnection line M2 is covered with the interlayer insulating film 56. Thereafter, the metal interlayer insulating film 56 is etched to form a trench, wherein the trench is formed at a position corresponding to the periphery of the photodiode. Next, when the trench is filled with the oxide film 57 having a low refractive index, the buried oxide film 57 functions to induce total reflection, thereby preventing loss of light incident on the photodiode. It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the invention. Will be apparent to those of ordinary skill in the art.

When the present invention is applied to a CMOS image sensor, it is possible not only to reduce the light loss occurring at the edge portion of the pixel array, but also to reduce the difference in sensitivity between the center portion and the edge portion of the pixel array.

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CLAIMS KR20060020400

1.
A method for manufacturing a CMOS image sensor having a pixel array region and a logic region, the method comprising the steps of forming a second metal interconnection in the pixel array region and the logic region, forming a fourth metal interconnection in the logic region, Forming an interlayer insulating film in the region; Etching the interlayer dielectric to form a trench of the second metal interconnection depth at an interface between the pixel array region and the logic region; And filling the trench with an oxide film having a refractive index lower than that of the interlayer insulating film.

2.
The method of claim 1, wherein the step of filling the trench with an oxide film having a refractive index lower than that of the interlayer insulating film includes: forming an interlayer insulating film including the trench and an oxide film having a refractive index lower than that of the interlayer insulating film ; And advancing the chivebeck process until the fourth metal interconnection is exposed. & Lt; Desc / Clms Page number 19 & gt;

3.
The method of claim 1, wherein the refractive index of the oxide film is 1.41 in the step of filling the trench with an oxide film having a refractive index lower than that of the interlayer insulating film.

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심사청구 : 없음

(54) 광 손실을 감소시킨 시모스 이미지센서의 제조방법

요약

본 발명은 시모스 이미지센서의 제조방법에 관한 것으로 특히, 픽셀어레이의 둘레부분에 상대적으로 저 굴절률을 갖는 산화막을 제 2 금속배선 깊이까지 매립함으로써 픽셀어레이의 엣지부분에서 발생하였던 광 손실을 절감한 발명이다. 이를 위한 본 발명은 픽셀 어레이 영역과 로직영역을 구비한 시모스 이미지센서의 제조방법에 있어서, 상기 픽셀 어레이 영역과 상기 로직 영역에 제 2 금속배선까지 형성한 후, 상기 로직 영역에는 제 4 금속배선까지 형성하며 상기 픽셀 어레이 영역에는 층간절연막을 형성하는 단계; 상기 층간절연막을 식각하여 상기 픽셀 어레이 영역과 상기 로직 영역 사이의 경계면에 상기 제 2 금속배선 깊이의 트렌치를 형성하는 단계; 및 상기 트렌치 내부를 상기 층간절연막 보다 굴절률이 낮은 산화막으로 매립하는 단계를 포함하여 이루어진다.

대표도

도 2c

색인어

시모스 이미지센서, 굴절률, 전반사, 픽셀 어레이, 광 손실

명세서

도면의 간단한 설명

도1a는 통상적인 시모스 이미지센서의 단위화소를 도시한 회로도,

도1b는 종래기술에 따른 시모스 이미지센서칩의 대략적인 구조를 도시한 도면,

도1c는 종래기술에 따른 시모스 이미지센서에서 픽셀 어레이 부분과 로직영역의 단면을 비교하여 도시한 단면도,

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도2a 내지 도2c는 본 발명의 일실시예에 따른 시모스 이미지센서의 제조공정을 도시한 공정단면도,

도2d는 본 발명의 일실시예에 따른 시모스 이미지센서 칩의 모습을 보인 평면도면,

도3은 본 발명의 기술적 사상을 단위화소에 적용한 경우를 도시한 단면도면.

도면의 주요부분에 대한 부호의 설명

30 : 기판 31 : 게이트

32 : 스페이서 33 : 층간절연막

34 : M1 콘택 35 : 제 1 금속배선(M1)

36 : VIA 1 37, 39, 42 : 금속층간절연막

38 : 제 2 금속배선(M2) 40 : VIA 2

41 : 제 3 금속배선(M3) 43 : VIA3

44 : 제 4 금속배선(M4) 45 : 마스크

46 : 트렌치 47 : 산화막

50 : 기판 51 : 포토다이오드

52 : 게이트 53 : 스페이서

54 : 층간절연막 55, 56 : 금속층간절연막

57 : 산화막

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 시모스 이미지센서의 제조방법에 관한 것으로 특히, 픽셀 어레이와 로직회로 사이의 엣지영역에 제 2 금속배선 깊이까지 산화막을 빙 둘러 매립함으로써, 상기 산화막에 의해 전반사된 빛을 픽셀 어레이로 다시 받아들여 빛의 손실을 감소시킨 발명이다.

일반적으로, 이미지센서는 광학 영상(optical image)을 전기적 신호로 변환시키는 반도체 장치로서, 대표적인 이미지센서 소자로는 전하결합소자(Charge Coupled Device: CCD)와 시모스 이미지센서를 들 수 있다.

그 중에서 전하결합소자는 개개의 MOS(Metal-Oxide-Silicon) 캐패시터가 서로 매우 근접한 위치에 있으면서 전하 캐리어가 캐패시터에 저장되고 이송되는 소자이며, 시모스 이미지센서는 제어회로(control circuit) 및 신호처리회로(signal processing circuit)를 주변회로로 사용하는 CMOS 기술을 이용하여 화소(pixel)수 만큼 MOS 트랜지스터를 만들고 이것을 이용하여 순차적으로 출력을 검출하는 스위칭 방식을 채용하는 소자이다.

도1a는 통상의 시모스 이미지센서에서 1개의 포토다이오드(PD)와 4개의 MOS 트랜지스터로 구성된 단위화소(Unit Pixel)를 도시한 회로도로서, 빛을 받아 광전하를 생성하는 포토다이오드(100)와, 포토다이오드(100)에서 모아진 광전하를 플로팅확산영역(102)으로 운송하기 위한 트랜스퍼 트랜지스터(101)와, 원하는 값으로 플로팅 확산영역의 전위를 세팅

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하고 전하를 배출하여 플로팅 확산영역(102)를 리셋시키기 위한 리셋 트랜지스터(103)와, 플로팅 확산영역의 전압이 게이트로 입가되어 소스 팔로워 버퍼 증폭기(Source Follower Buffer Amplifier) 역할을 하는 드라이브 트랜지스터(104)와, 스위칭(Switching) 역할로 어드레싱(Addressing) 역할을 수행하는 셀렉트 트랜지스터(105)로 구성된다. 단위 화소 밖에는 출력신호(Output Signal)를 읽을 수 있도록 로드(load) 트랜지스터(106)가 형성된 모습을 도시하고 있다.

도1b는 이러한 단위화소가 수십 내지 수백만개 구비된 픽셀 어레이를 비롯하여 화상 데이터를 처리하는 로직회로부 등으로 구성된 시모스 이미지센서 칩의 대략적인 모습을 도시한 평면도이다. 이를 참조하면 빛을 수광하는 픽셀 어레이의 주변으로 로직회로부가 배치되어 있음을 알 수 있다.

도1c는 픽셀어레이와 로직회로부의 단면을 함께 도시한 단면도면으로 특히, 픽셀 어레이와 로직회로부의 경계면을 중점적으로 도시한 도면으로, 도1c를 참조하여 종래기술의 문제점을 설명하면 다음과 같다.

먼저, 도1c에는 픽셀 어레이 영역과 로직 영역이 함께 도시되어 있는 바, 픽셀어레이 영역은 포토다이오드 등으로 구성된 수광부가 형성되어 있는 영역이며, 로직영역은 신호처리를 위한 일반적인 논리회로가 중점적으로 형성된 부분이다.

즉, 반도체 기판(11) 상에는 스페이서(13)를 구비한 게이트 전극(12)이 형성되어 있으며, 게이트 전극을 포함한 기판 상에는 절연을 위한 층간절연막(14)이 형성되어 있다. 그리고 게이트 전극(12) 상에는 층간절연막(14)을 관통하여 게이트 전극(12)과 제 1 금속배선(16)을 연결하는 금속콘택(15)(M1 contact)이 형성되어 있다.

또한, 층간절연막(14) 상에는 제 1 금속배선(16)이 패터닝되어 있으며, 그 위로는 제 2 내지 제 4 금속배선(18, 20, 22)이 적층되어 형성되며, 각 금속배선 사이에는 금속배선들을 절연하기 위한 금속층간절연막(도면부호는 부여하지 않음)이 각각 구비되어 있다. 여기서 금속층간절연막은 통상적으로 FSG 막과 TEOS 산화막이 적층된 구조를 갖고 있음을 알 수 있다. 또한, 도1c에는 각각의 금속배선을 전기적으로 연결하기 위한 VIA 1 내지 VIA 3 가 도시되어 있다.

도1c를 참조하면 종래의 시모스 이미지센서에서, 픽셀 어레이 영역은 제 2 금속배선(M2)(18)까지만 형성되어 있으며, 로직영역은 제 4 금속배선(22)까지 형성되어 있음을 알 수 있다.

즉, 제 2 금속배선(M2)(18)까지만 형성된 픽셀어레이 영역에서는 산화막 계열의 FGS 막과 TEOS 산화막이 2 겹씩 형성되어, 로직 영역의 제 4 금속배선과 높이를 맞추고 있다.

이와같은 구조의 종래 이미지센서에서는, 로직 영역의 제 4 금속배선(22)을 실딩 메탈(shielding metal)로 형성하여 픽셀 어레이 영역을 둘러싸고 있는데, 이는 픽셀 어레이영역과 로직영역간의 경계임을 나타내는 동시에 픽셀 어레이 영역의 가장자리로 입사하는 빛의 손실을 감소시키기 위한 목적도 있었다.

하지만, 종래기술에 따라 제 4 금속배선을 이용한 실딩 메탈은 엣지로 입사하는 입사광을 픽셀 어레이 쪽으로 모아주지 못하고, 금속의 특수한 유전율에 의해 거의 대부분을 손실하는 단점이 있었다.

발명이 이루고자 하는 기술적 과제

본 발명은 상기한 종래의 문제점을 해결하기 위한 것으로, 픽셀 어레이의 엣지부분에서 광손실을 감소시키며 나아가 픽셀 어레이의 중심부분과 엣지부분의 광감도 차이를 줄인 시모스 이미지센서 제조방법을 제공함을 목적으로 한다.

발명의 구성 및 작용

상기한 목적을 달성하기 위한 본 발명은, 픽셀 어레이 영역과 로직영역을 구비한 시모스 이미지센서의 제조방법에 있어서, 상기 픽셀 어레이 영역과 상기 로직 영역에 제 2 금속배선까지 형성한 후, 상기 로직 영역에는 제 4 금속배선까지 형성하며 상기 픽셀 어레이 영역에는 층간절연막을 형성하는 단계; 상기 층간절연막을 식각하여 상기 픽셀 어레이 영역과 상기 로직 영역 사이의 경계면에 상기 제 2 금속배선 깊이의 트렌치를 형성하는 단계; 및 상기 트렌치 내부를 상기 층간절연막 보다 굴절률이 낮은 산화막으로 매립하는 단계를 포함하여 이루어진다.

본 발명에서는 픽셀 어레이와 로직 영역의 경계면에 제 2 금속배선 깊이까지 산화막 계열의 막을 매립시켜, 입사된 빛이 산화막 계열의 막에 의해 전반사되어 픽셀 어레이 쪽으로 입사하도록 유도함으로써 빛의 손실을 막고 픽셀 어레이의 엣지부분의 광감도를 향상시킬 수 있었다.

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이하, 본 발명이 속하는 기술분야에서 통상의 지식을 가진 자가 본 발명의 기술적 사상을 용이하게 실시할 수 있을 정도로 상세히 설명하기 위하여, 본 발명의 가장 바람직한 실시예를 첨부된 도면을 참조하여 설명한다.

도2a 내지 도2c는 본 발명의 일실시예에 따른 시모스 이미지센서의 제조공정을 도시한 공정단면도로써 이를 이을 참조하여 본 발명의 일실시예를 설명한다.

우선, 제 4 금속배선(44)을 형성하기 까지의 공정은 종래기술과 동일하다.

이를 참조하면 먼저, 픽셀 어레이 영역과 로직영역을 갖는 반도체 기판 상에 활성영역과 필드영역을 정의하는 소자분리막을 형성한다. 이러한 소자분리막은 도2a에는 도시하지 않았다.

다음으로 픽셀 어레이 영역에 포토다이오드를 형성한다. 포토다이오드 역시 도2a에는 도시되어 있지 않다. 다음으로 반도체 기판 상부에 스페이서(32)을 구비한 게이트 전극(31)을 형성하고 소스/드레인 영역(미도시)을 형성한다.

다음으로, 게이트 전극(31)을 포함한 기판(30) 상부에 층간절연막(33)을 형성한 후, 층간절연막(33)을 일정부분 제거하고 전도물질을 매립하여 게이트 전극(31)과 제 1 금속배선(35)을 연결하는 금속콘택(34)을 형성한다.

이어서, 제 1 금속배선(35)의 상부에 제 1 금속층간절연막(37)을 형성한 후, 제 1 금속층간절연막(37)을 관통하여 제 1 금속배선과 제 2 금속배선을 연결하는 제 1 비아(VIA 1)(36)를 형성한다.

다음으로 제 1 금속층간절연막(37) 상에 제 2 금속배선(38)을 패터닝한다.

이와같은 공정은 픽셀어레이 영역과 로직영역에서 모두 동일하게 진행되나, 이후의 공정은 픽셀어레이 영역과 로직영역에서 달리 진행된다.

즉, 로직영역에서는 제 3 금속배선(41) 및 제 4 금속배선(44)이 차례로 적층되는 공정이 진행되는 반면에, 픽셀 어레이 영역에서는 금속층간절연막(39, 42)만이 차례로 적층되며 더이상의 금속배선은 사용되지 않는다.

도2a에서 미설명 부호 40, 43 은 각각 VIA 2 와 VIA 3 를 나타낸다.

이와같이 제 4 금속배선(44)까지 형성한 다음, 마스크(45)를 이용하여 픽셀어레이 영역과 로직영역 사이의 경계면에 트렌치(46)를 형성한다. 이때, 트렌치의 깊이는 제 2 금속배선(38)까지로 하며 0.18㎛ 급 시모스 이미지센서에서는 트렌지의 깊이가 16000Å 정도 되는 것이 바람직하다.

다음으로, 도2b에 도시된 바와같이 전체 구조상에 산화막(47)을 증착하여 트렌치를 매립한다.

여기서, 산화막(47)은 1.41 정도의 낮은 굴절률을 갖고 있으며, 픽셀 어레이쪽의 금속층간절연막 보다는 상대적으로 낮은 굴절률을 갖고 있다. 이와같이 본 발명의 일실시예에서는 상기의 산화막(47)을 이용한 전반사를 통해 경계면에서의 빛 손실을 줄일 수 있었다.

이와같이 산화막(47)을 증착한 다음에는 도2c에 도시된 바와같이 제 4 금속배선(44)의 표면이 드러날 때까지 산화막(47)에 대한 에치백 공정을 진행하게 되면, 제 4 금속배선의 측면에는 스페이서 형태로 산화막이 남게 되며, 트렌치는 산화막으로 매립된다. 이때, 제 4 금속배선의 두께는 6500Å 정도 된다.

이후에 도2c에는 도시되어 있지 않지만, 패시베이션막, 칼라필터, 마이크로렌즈 형성 등의 통상적인 공정을 진행하여 시모스 이미지센서를 완성한다.

결과적으로 픽셀어레이의 주변으로는 저 굴절률을 갖는 산화막이 매립되어 있으므로, 픽셀 어레이 영역과 로직영역사이의 경계면으로 입사하는 빛은 산화막에 의해 전반사되어 픽셀 어레이 영역으로 재입사하게 된다.

본 발명에서는 이러한 점을 이용하여 픽셀 어레이의 엣지부분에서의 광감도를 향상시켜 줄 수 있었으며 또한, 픽셀 어레이의 중앙부분과 엣지부분의 광감도 차이도 감소시킬 수 있었다.

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도2d는 본 발명의 일실시예에 따라 형성된 시모스 이미지센서 칩의 대략적인 모습을 도시한 평면도로써, 픽셀 어레이의 가장자리를 따라 저 굴절률의 산화막(47)이 매립되어 있음을 알 수 있다.

도3은 본 발명의 기술적 사상을 단위화소에 적용한 모습을 도시한 단면도이다. 즉, 도3은 하나의 단위화소를 중심으로 그 단면을 도시한 도면으로 이를 참조하여 설명한다.

먼저, 제 2 금속배선(M2)을 형성하기 까지는 본 발명의 제 1 실시예와 동일하다. 즉, 반도체 기판(50)에는 빛을 수광하여 전기신호로 변환하는 포토다이오드(51)가 형성되어 있으며, 또한 스페이서(53)을 구비한 게이트 전극(52)이 형성되어 있다.

또한, 게이트 전극을 포함한 반도체 기판(50) 상에는 층간절연막(54)이 형성되어 있으며, 층간절연막 상에는 포토다이오드로 입사하는 빛의 진로를 막지 않도록 레이아웃된 제 1 금속배선(M1) 및 제 2 금속배선(M2)이 형성되어 있다.

미설명 부호 54, 55 는 금속층간절연막이다.

이와같이 제 2 금속배선(M2)까지 형성한 후에는 그 상부를 금속층간절연막(56)으로 덮은 공정이 진행된다. 이후, 상기 금속층간절연막(56)을 식각하여 트렌치를 형성하되, 트렌치는 포토다이오드의 둘레에 대응하는 위치에 형성한다.

다음으로, 트렌치를 저 굴절률의 산화막(57)으로 매립하게 되면, 매립된 산화막(57)이 전반사를 유도하는 역할을 하여 포토다이오드로 입사하는 빛의 손실을 방지할 수 있게 된다.

이상에서 설명한 바와 같이 본 발명은 전술한 실시예 및 첨부된 도면에 의해 한정되는 것이 아니고, 본 발명의 기술적 사상을 벗어나지 않는 범위 내에서 여러 가지 치환, 변형 및 변경이 가능함이 본 발명이 속하는 기술분야에서 통상의 지식을 가진 자에게 있어 명백할 것이다.

발명의 효과

본 발명을 시모스 이미지센서에 적용하게 되면, 픽셀 어레이의 엣지부분에서 발생하였던 광 손실을 절감할 수 있을 뿐 아니라 나아가 픽셀 어레이의 중앙부분과 엣지부분과의 광 감도 차이를 줄일 수 있는 장점이 있다.

(57) 청구의 범위

청구항 1.

픽셀 어레이 영역과 로직영역을 구비한 시모스 이미지센서의 제조방법에 있어서,

상기 픽셀 어레이 영역과 상기 로직 영역에 제 2 금속배선까지 형성한 후, 상기 로직 영역에는 제 4 금속배선까지 형성하며 상기 픽셀 어레이 영역에는 층간절연막을 형성하는 단계;

상기 층간절연막을 식각하여 상기 픽셀 어레이 영역과 상기 로직 영역 사이의 경계면에 상기 제 2 금속배선 깊이의 트렌치를 형성하는 단계; 및

상기 트렌지 내부를 상기 층간절연막 보다 굴절률이 낮은 산화막으로 매립하는 단계

를 포함하여 이루어지는 시모스 이미지센서의 제조방법.

청구항 2.

제 1 항에 있어서,

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상기 트렌치 내부를 상기 층간절연막 보다 굴절률이 낮은 산화막으로 매립하는 단계는,

상기 트렌치를 포함하는 층간절연막과 상기 제 4 금속배선 상부에 상기 층간절연막 보다 굴절률이 낮은 산화막을 적층형성하는 단계; 및

상기 제 4 금속배선의 노출될 때 까지 에치백 공정을 진행하는 단계

을 포함하여 이루어지는 것을 특징으로 하는 시모스 이미지센서의 제조방법.

청구항 3.

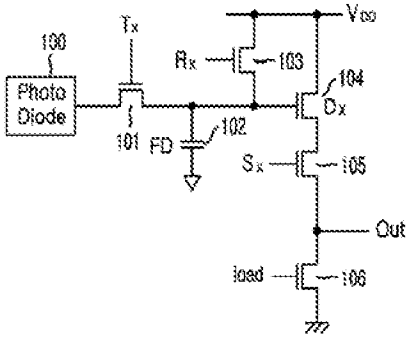
제 1 항에 있어서,

상기 트렌치 내부를 상기 층간절연막 보다 굴절률이 낮은 산화막으로 매립하는 단계에서,

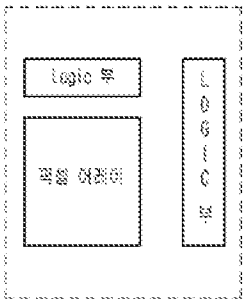
상기 산화막의 굴절률은 1.41 인 것을 특징으로 하는 시모스 이미지센서의 제조방법.

도면

도면1a

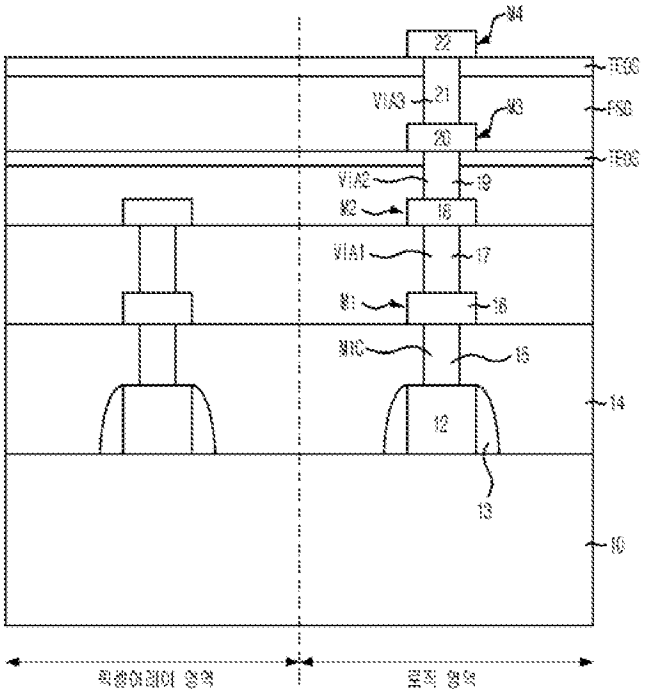


도면1b

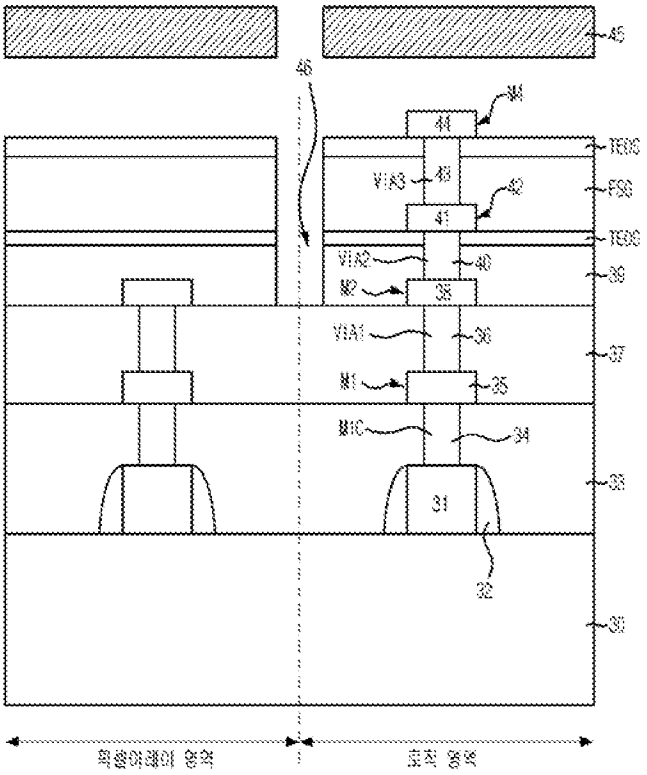


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도면1c

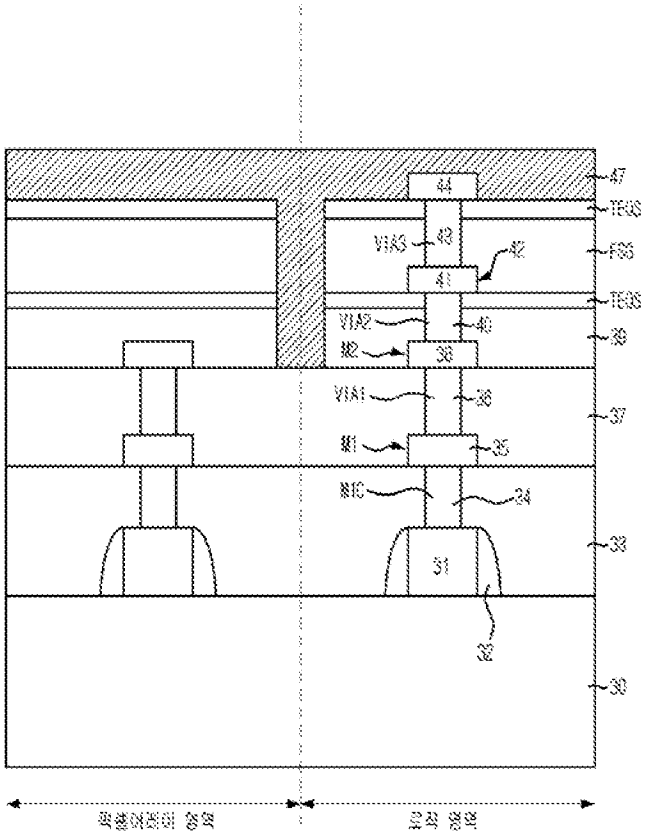


도면2a

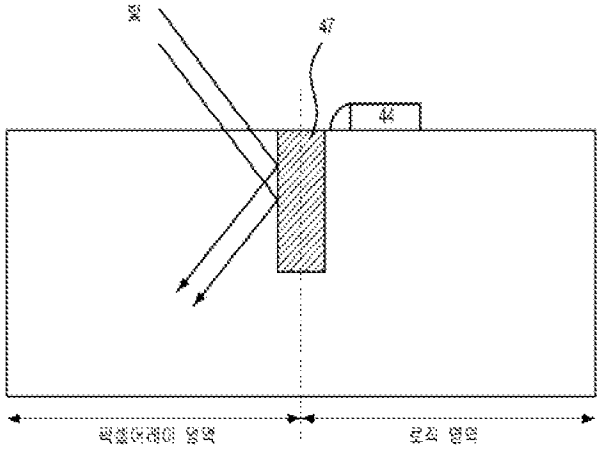


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도면2b

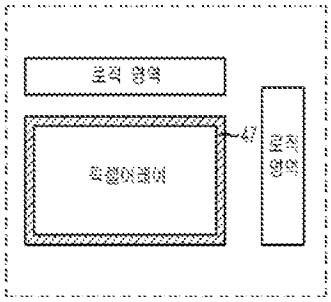


도면2c

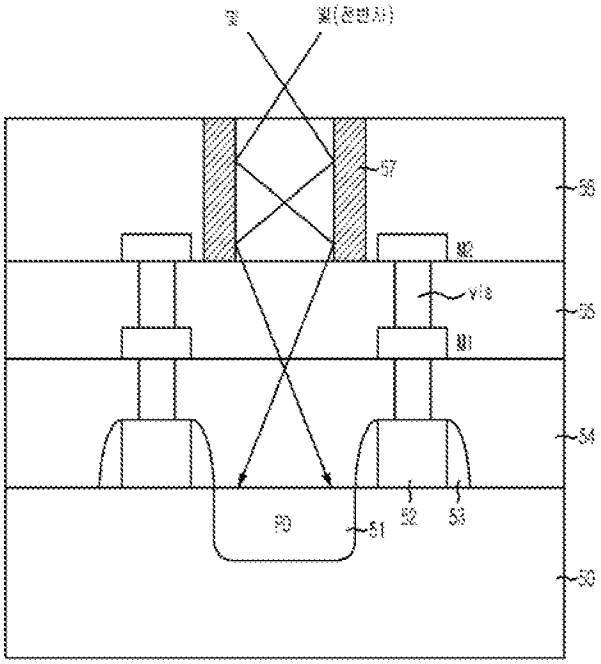


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도면2



도면3



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Espacenet

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BACK ILLUMINATED CMOS IMAGE SENSORS WITH DEEP TRENCH ISOLATION AND METHOD FOR PRODUCING THE SAME

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Classification: - international:***H01L27/146***
- cooperative: **H01L27/1461**; **H01L27/14629**; **H01L27/1463**; **H01L27/14685** more

Application number: KR20060075806 20060810 Global Dossier

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Abstract of KR20080014301 (A)

A back illuminated CMOS image sensor having a deep trench device isolating film and a method for producing the same are provided to prevent an electrical crosstalk and an optical crosstalk between pixels by isolating a photo diode of a pixel array using a device isolating film with a deep trench structure. A back illuminated CMOS image sensor comprises a device isolating film with a deep trench structure(13), a photo diode(11), a pixel circuit(20), and a lens(30). The device isolating film with the deep trench structure is formed by extending from a first side to a second side of a semiconductor substrate(10). The photo diode is defined by the device isolating film with the deep trench structure, and is formed by extending from a first side to a second side of the semiconductor substrate. The pixel circuit adjacent to the first side of the semiconductor substrate is formed. The lens adjacent to the second side of the semiconductor substrate is formed.

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DESCRIPTION KR20080014301

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a back - illuminated CMOS image sensor including a deep trench isolation film,

1 is a schematic cross - sectional view of a pixel array region of a conventional back - illuminated CMOS sensor.

2 is a schematic cross - sectional view of a pixel array region of a chip edge portion of a conventional back - illuminated CMOS sensor.

3 is a schematic cross - sectional view of a pixel array region of a back - illuminated CMOS image sensor according to an embodiment of the present invention.

FIG. 4 is a schematic flowchart for explaining a method of fabricating a back - illuminated CMOS image sensor according to the present invention in order.

Description of the Related Art

10: Semiconductor substrate 11: Photodiode

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13: Deep trench isolation film 20:

30: Lens part 31: Color filter

33: Micro lens 40: Support substrate

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a CMOS image device, and more particularly, to a back illuminated CMOS image sensor capable of preventing cross talk and a method of manufacturing the same. A typical image sensor is a semiconductor device that converts an optical image into an electrical signal. Such an image sensor can be classified into a CCD (charge coupled device) and a CMOS image sensor (CIS). Image sensors are based on a two - dimensional array of pixels. Each pixel includes a sensing element that can convert a portion of the optical image into an electrical signal. The electrical signals are used, for example, to reproduce the optical image on the display. A CMOS image sensor is a device having a photodiode for receiving an optical signal in a unit pixel and a MOS transistor for controlling the optical signal. The manufacturing process is very simple compared to a CCD, and a well - It has an advantage that it can be manufactured as one chip together with the signal processing element. As CMOS technology is developed in the direction of reduction of photolithography, the size of pixels and circuits of CMOS image sensors is also decreasing. As the size of a pixel decreases, a pixel array having a large number of pixels can be formed at a low cost. On the other hand, there is a problem in that the photosensitivity drops due to a small amount of incident light. In particular, in a front illuminated CMOS image sensor using an active pixel sensor (APS), a metal line associated with the active circuit reduces the fill factor of the pixel array. This is because, even if the line width of the metal line is reduced, the amount of light reaching the diffusion region is reduced due to the presence of the metal line, the photodiode diffusion region which is the light sensing unit is blocked, or the light reaches the photodiode diffusion region.

A back illuminated CMOS sensor is an image sensor in which a circuit is present on the front side of the substrate and a lens is present on the rear side of the substrate. Since the light does not pass through the circuit area but directly enters the impurity region of the photodiode through the lens, it is possible to solve the problem of reduction of the filling rate of the front - illuminated CMOS image sensor. 1 is a schematic cross - sectional view of a conventional back - illuminated CMOS sensor. The pixel circuit portion 1 of the CMOS sensor is formed in a laminated manner on one surface 7 of the

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substrate 2. | An impurity region 9 of a photodiode extending to the other surface 8 of the substrate 2 is formed on the pixel circuit portion 1 and a color filter 3 and a microlens 4 are formed thereon. The substrate 2 of the CMOS image sensor is very thin and is supported by the support substrate 6 contacting the pixel circuit portion 1. | A manufacturing method of such a conventional back - illuminated CMOS sensor is as follows. First, the impurity region 2 of the photodiode is formed at a depth of a certain depth from the front surface of the substrate by ion implantation, and the circuit pattern layers constituting the pixel circuit portion 1 are formed. A supporting substrate 6 is attached to the front surface of the substrate in contact with the pixel circuit portion 1 and the rear surface of the substrate is polished to expose the impurity region 2 of the photodiode from the rear surface of the substrate. A lens portion 5 including a color filter 3 and a microlens 4 is formed on the exposed photodiode 2. The region immediately below the color filter 3 in the region of the photodiode 2 corresponds to the farthest from the front surface of the substrate and the probability that the concentration of the ion implanted impurity is not uniform becomes high. In the back - illuminated CMOS sensor, the element isolation between the photodiodes 2 is performed by the doping profile. In the region under the color filter 3, the doping profile is not clear due to the irregularity of the impurity concentration, The electrical crosstalk may not be completely removed. 2, in the case of a pixel located at the edge of the chip, the microlens 3 and the color filter 4 are not aligned with the corresponding photodiode 2 and a photodiode (not shown) 2 by a predetermined amount.

Therefore, in the case of the pixels at the chip edge, the possibility of optical crosstalk is increased. An object of the present invention is to provide a back - illuminated CMOS image sensor capable of blocking electrical crosstalk between pixels and optical crosstalk. According to another aspect of the present invention, there is provided a method of fabricating a backside illumination type CMOS image sensor capable of blocking electrical crosstalk between pixels and optical crosstalk.

According to an aspect of the present invention, there is provided a back - illuminated CMOS image sensor including a semiconductor substrate having a first surface and a second surface, the device having a deep trench structure extending from the first surface toward the second surface, ; A photodiode defined by the deep trench isolation film and extended from the first surface to the second surface; A pixel circuit portion formed adjacent to the first surface of the semiconductor substrate; And a lens portion formed adjacent to the second surface of the semiconductor substrate. And a support substrate on the pixel circuit portion. It is preferable that the depth of the device isolation film of the deep trench structure is 3 to 10 mu m. The deep - trench structure may be formed of an insulating film having a refractive index lower than that of the

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semiconductor substrate such that light incident obliquely through the photodiode is totally reflected at the boundary of the isolation film, and may be a silicon oxide film. And a glass substrate between the second surface of the semiconductor substrate and the lens portion. The pixel circuit portion may include a transfer transistor, a reset transistor, a drive transistor, a selection transistor, and a wiring. The lens portion may include a color filter adjacent to the second surface of the semiconductor substrate and a microlens on the color filter. According to another aspect of the present invention, there is provided a method of manufacturing a back - illuminated CMOS image sensor, including: forming a deep - trench structure isolation layer from a first surface of a semiconductor substrate; Forming a photodiode region in the semiconductor substrate defined by the device isolation film by ion implantation from the first surface; Forming a pixel circuit portion on the first surface of the semiconductor substrate over the photodiode region; Polishing the second surface of the semiconductor substrate on which the pixel circuit portion is formed; And forming a lens portion on the second surface of the polished semiconductor substrate, the lens portion being aligned with the photodiode. Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings.

However, the present invention is not limited to the embodiments described herein but may be embodied in other forms. Rather, the embodiments disclosed herein are being provided so that this disclosure will be thorough and complete, and will fully convey the concept of the invention to those skilled in the art. In the drawings, the thicknesses of layers and regions are exaggerated for clarity. Like reference numerals designate like elements throughout the specification. 3 is a simplified cross - sectional view of a back - illuminated CMOS image sensor according to an embodiment of the present invention. 3 shows a pixel array portion including the photodiode 11, the pixel circuit portion 20, and the lens portion 30. In Fig. 3, the semiconductor substrate 10 on which the photodiode 11 is formed has a front side 13 directed downward and a back side 15 directed upward. In the back - illuminated CMOS image sensor, since the light is incident from the back surface 15 of the semiconductor substrate 10, the thickness of the substrate must be small enough to allow the incident light to reach the photodiode 11. The photodiode 11 in the semiconductor substrate 10 can be formed by the p - type impurity region in the n - type impurity or the n - type impurity region in the p - type impurity region. A pixel circuit portion 20 including transistors and wirings constituting a unit pixel together with a photodiode 11 is formed on the front surface 13 of the semiconductor substrate 10 under the photodiode 11. A passivation layer (not shown) and an adhesive layer (not shown) may be further formed between the pixel circuit portion 20 and the support substrate 40. The passivation layer A lens unit 30 including a color filter 31 and a microlens 33 is formed on the back surface of the semiconductor substrate 10 on the photodiode 11. A transparent substrate (not shown) such as glass may be further

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formed between the photodiode 11 and the lens unit 30. [In the present invention, adjacent photodiodes (11) are separated from each other by a deep trench isolation film (13).

The deep trench isolation film 13 may be formed by a depth of the photodiode 11 or may be formed to be slightly shallow. The deep trench isolation film 13 is formed just below the lens portion 30 so that the electrons or holes generated by the light in the photodiode 11 can not move vertically and move to the adjacent pixel region Electrical crosstalk can be prevented. Since the impurity region of the photodiode 11 is formed by deep ion implantation from the front surface of the semiconductor substrate 10 in the backside illumination type CMOS image sensor, the impurity region which is in contact with the back surface of the semiconductor substrate 10 under the lens portion 30 The doping profile is disturbed and electrical crosstalk can occur. The electrical crosstalk can be prevented by the deep trench isolation film 13 which is an insulating film. The incident light having a slope through the lens unit 30 is totally reflected at the boundary between the photodiode 11 and the isolation film 13 and can not pass through the photodiode 11 of the adjacent pixel. Therefore, optical crosstalk Can be prevented. In order to increase the light receiving efficiency of obliquely incident light, the pixels of the edge portion of the chip of the conventional CMOS image sensor are formed such that the lens portion 30 and the corresponding photodiode 11 in one pixel are overlapped obliquely There is a high possibility that optical crosstalk between adjacent pixels occurs. However, in the present invention, as shown in FIG. 4, the deep trench isolation film 13 between the photodiodes 11 is made of a material having a refractive index lower than that of the silicon of the photodiode 11 and is made obliquely incident on the deep trench isolation film 13 Optical crosstalk can be prevented by totally reflecting light. FIG. 5 is a schematic flowchart for explaining a method of manufacturing a back - illuminated CMOS image sensor according to the present invention in order. Referring to FIG. 5, a deep trench isolation layer is formed on a semiconductor substrate (S10). The deep trench isolation film is formed by etching a semiconductor substrate using a hard mask pattern such as a silicon nitride film as a mask to form a deep trench and then filling an insulating film such as a silicon oxide film.

The insulating film is formed by forming an insulating film to fill the deep trench, planarizing the insulating film, and removing the hard mask pattern. Next, a photodiode region is formed by ion implantation of impurities into the semiconductor substrate having the deep trench isolation film formed thereon (S20). The photodiode region can be formed by forming a p - type impurity region in the n - type impurity or an n - type impurity region in the p - type impurity region. After the photodiode region is formed on the semiconductor substrate, a pixel circuit portion including a transistor and a wiring

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that constitute a unit pixel such as a transfer transistor, a reset transistor, a driving transistor, and a selection transistor is formed on the substrate (S30). A supporting substrate is attached to the front surface of the semiconductor substrate on which the pixel circuit portion is formed (S40). A passivation layer for protecting the pixel circuit portion before attachment of the supporting substrate can be formed. After the supporting substrate is attached, the back surface of the semiconductor substrate is polished and chemically mechanically polished so that light can be incident from the back surface of the semiconductor substrate to the photodiode region, thereby reducing the thickness of the semiconductor substrate (S50). A lens portion including a color filter and a microlens is formed on the photodiode on the back surface of the semiconductor substrate (S60). At this time, a glass substrate may be further formed between the back surface of the semiconductor substrate and the lens portion. While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it is to be understood that the invention is not limited to the disclosed exemplary embodiments, It will be apparent to those skilled in the art that the present invention can be carried out without departing from the spirit and scope of the invention.

According to the present invention, the inter - pixel electrical crosstalk and the optical crosstalk can be blocked by isolating the photodiode of the pixel array into the deep - trench structure element isolation film in the back - illuminated CMOS image sensor.

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CLAIMS KR20080014301

1.
An element isolation layer of a deep trench structure formed in a semiconductor substrate having a first surface and a second surface and extended from the first surface to the second surface; A photodiode defined by the deep trench isolation film and extended from the first surface to the second surface; A pixel circuit portion formed adjacent to the first surface of the semiconductor substrate; And a lens portion formed adjacent to the second surface of the semiconductor substrate.

2.
The backside illumination type CMOS image sensor according to claim 1, further comprising a supporting substrate on the pixel circuit portion.

3.
The backside illumination type CMOS image sensor according to claim 1, wherein the depth of the device isolation film of the deep trench structure is 3 to 10 mu m.

4.
The backside illumination type CMOS image sensor according to claim 1, wherein the deep - trench structure element isolation film is formed of an insulating film having a refractive index lower than that of the semiconductor substrate so that light obliquely incident through the photodiode is totally reflected at a boundary of the isolation film.

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5.
The backside illumination type CMOS image sensor according to claim 4, wherein the device isolation film of the deep trench structure is a silicon oxide film.

6.
The back - illuminated CMOS image sensor according to claim 1, further comprising a glass substrate between the second surface of the semiconductor substrate and the lens portion.

7.
The backside illumination type CMOS image sensor according to claim 1, wherein the pixel circuit portion includes a transfer transistor, a reset transistor, a driving transistor, a selection transistor, and a wiring.

8.
The backside illumination type CMOS image sensor according to claim 1, wherein the lens portion includes a color filter adjacent to the second surface of the semiconductor substrate and a microlens on the color filter.

9.
Forming a device isolation film of a deep trench structure from the first surface of the semiconductor substrate; Forming a photodiode region in the semiconductor substrate defined by the device isolation film by ion implantation from the first surface; Forming a pixel circuit portion on the first surface of the semiconductor substrate over the photodiode region; Polishing the second surface of the semiconductor substrate on which the pixel circuit portion is formed; And forming a lens portion on the second surface of the polished semiconductor substrate in alignment with the photodiode.

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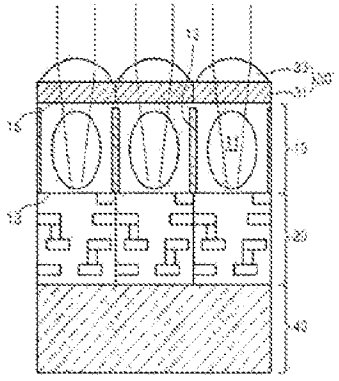
전체 청구항 수 : 총 9 항

(54) 딥트렌치 소자분리막을 포함하는 이면 조사형 CMOS이미지 센서 및 그 제조방법

(57) 요 약

딥트렌치 구조의 소자분리막을 구비한 이면 조사형 CMOS 이미지 센서 및 그 제조방법을 개시한다. 본 발명에 의한 CMOS 이미지 센서는 제1 면과 제2 면을 갖는 반도체 기판 내에서 상기 제1 면으로부터 상기 제2면을 향하여 확장되어 형성된 딥트렌치 구조의 소자분리막; 상기 딥트렌치 소자분리막에 의하여 한정되며 상기 제1 면으로부터 상기 제2면을 향하여 확장되어 형성된 포토다이오드; 상기 반도체 기판의 상기 제1 면에 인접하여 형성된 화소 회로부; 및 상기 반도체 기판의 상기 제2 면에 인접하여 형성된 랜즈부를 포함한다. 화소 어레이의 포토다이오드가 딥트렌치 구조의 소자분리막으로 격리됨으로써 화소간 전기적 크로스토크와 광학적 크로스토크를 방지할 수 있다.

대표도 - 도3



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특허청구의 범위

청구항 1

제1 면과 제2 면을 갖는 반도체 기판 내에서 상기 제1 면으로부터 상기 제2면을 향하여 확장되어 형성된 딥트렌치 구조의 소자분리막;

상기 딥트렌치 소자분리막에 의하여 한정되며 상기 제1 면으로부터 상기 제2면을 향하여 확장되어 형성된 포토다이오드;

상기 반도체 기판의 상기 제1 면에 인접하여 형성된 회소 회로부; 및

상기 반도체 기판의 상기 제2 면에 인접하여 형성된 렌즈부;를 포함하는 이면 조사형 CMOS 이미지 센서.

청구항 2

제1 항에 있어서, 상기 회소 회로부 위의 지지 기판을 더 포함하는 이면 조사형 CMOS 이미지 센서.

청구항 3

제1 항에 있어서, 상기 딥트렌치 구조의 소자분리막의 깊이는 3~10㎛인 이면 조사형 CMOS 이미지 센서.

청구항 4

제1 항에 있어서, 상기 딥트렌치 구조의 소자분리막은 상기 포토다이오드를 통과하여 경사입사된 빛이 상기 소자분리막의 경계에서 전반사되도록 상기 반도체 기판보다 굴절율이 낮은 절연막으로 형성된 이면 조사형 CMOS 이미지 센서.

청구항 5

제4 항에 있어서, 상기 딥트렌치 구조의 소자분리막은 실리콘 산화막인 이면 조사형 CMOS 이미지 센서.

청구항 6

제1 항에 있어서, 상기 반도체 기판의 상기 제2 면과 상기 렌즈부 사이에 글래스 기판을 더 포함하는 이면 조사형 CMOS 이미지 센서.

청구항 7

제1 항에 있어서, 상기 회소 회로부는 전달 트랜지스터, 리셋 트랜지스터, 구동 트랜지스터, 선택 트랜지스터 및 배선을 포함하는 이면 조사형 CMOS 이미지 센서.

청구항 8

제1 항에 있어서, 상기 렌즈부는 상기 반도체 기판의 상기 제2 면에 인접한 칼라필터와 상기 칼라필터 위의 마이크로 렌즈를 포함하는 이면 조사형 CMOS 이미지 센서.

청구항 9

반도체 기판의 제1 면으로부터 딥트렌치 구조의 소자분리막을 형성하는 단계;

상기 소자분리막에 의하여 한정되는 상기 반도체 기판 내에 상기 제1 면으로부터의 이온주입에 의하여 포토다이오드 영역을 형성하는 단계;

상기 포토다이오드 영역 위로 상기 반도체 기판의 상기 제1 면에 회소 회로부를 형성하는 단계;

상기 회소 회로부가 형성된 상기 반도체 기판의 상기 제2 면을 연마하는 단계;

연마된 상기 반도체 기판의 상기 제2 면에 상기 포토다이오드에 정렬하여 렌즈부를 형성하는 단계;를 포함하는 이면 조사형 CMOS 이미지 센서를 형성하는 방법.

명 세 서

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발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

<10> 본 발명은 CMOS 이미지소자에 관한 것으로 더욱 상세하게는 크로스토크(cross talk)를 방지할 수 있는 이면 조사형(back illuminated) CMOS 이미지 센서 및 그 제조방법에 관한 것이다.

<11> 일반적인 이미지 센서는 광학 영상(optical image)을 전기 신호로 변환시키는 반도체 소자를 의미한다. 이러한 이미지 센서는 CCD(Charge Coupled Device)와 CMOS 이미지 센서(CMOS image Sensor; CIS)로 구분될 수 있다. 이미지 센서들은 화소(pixel)의 2차원적인 배열에 관계하고 있다. 각 화소는 광학 영상의 일부를 전기적인 신호로 변환할 수 있는 감지 요소(sensing element)를 포함한다. 전기적인 신호들은 예를 들면, 디스플레이에 광학적 영상을 다시 생성하는데 사용된다.

<12> CMOS 이미지 센서는 단위 화소 내에 광신호를 수신하는 포토다이오드와 상기 광신호를 제어할 수 있는 모스트랜지스터를 구비하는 소자로, CCD에 비해 제조공정이 매우 단순하며 잘 확립된 CMOS 기술을 이용하여 다른 여러 신호처리 소자와 더불어 하나의 칩으로 제조할 수 있는 장점이 있다.

<13> CMOS 기술이 포토리소그래피의 축소의 방향으로 진계됨에 따라 CMOS 이미지 센서의 화소 및 회로의 크기도 감소하고 있다. 화소의 크기가 감소함에 따라 적은 비용으로 많은 수의 화소로 이루어진 화소 어레이를 만들 수 있는 장점이 있으나, 한편으로 적은 양의 광입사로 인하여 광감도가 떨어지는 문제점이 있다. 특히, 능동 화소(active pixel sensor: APS)를 사용하는 전면 조사형(front illuminated) CMOS 이미지 센서에서는 능동회로와 관련된 금속 라인이 화소 어레이의 채움율(fill factor)을 감소시킨다. 이것은 금속 라인의 선폭이 축소되어도 금속 라인의 존재로 인하여 광감지부인 포토다이오드 확산영역이 가려지거나 빛이 포토다이오드 확산영역에 도달하는 거리가 멀어짐으로써 확산영역에 도달하는 빛의 양이 감소되어 일어난다.

<14> 이면 조사형(back illuminated) CMOS 센서는 회로가 기판의 전면에 존재하고 렌즈가 기판의 이면에 존재하는 이미지 센서이다. 빛이 회로영역을 통과하지 않고 렌즈를 통하여 바로 포토다이오드의 불순물 영역으로 들어오므로 전면 조사형 CMOS 이미지 센서의 채움율 감소의 문제를 해결할 수 있다.

<15> 도 1은 종래의 이면 조사형 CMOS 센서의 개략적인 단면도이다. 기판(2)의 일면(7)에 접하여 CMOS 센서의 화소 회로부(1)가 적층 형성되어 있다. 화소 회로부(1) 위로 기판(2)의 다른 일면(8)까지 확장되는 포토다이오드의 불순물 영역(9)이 형성되어 있으며 그 위로 칼라필터(3)와 마이크로 렌즈(4)가 형성되어 있다. CMOS 이미지 센서의 기판(2)은 그 두께가 매우 얇아 화소 회로부(1)에 접한 지지기판(6)에 의하여 지지된다.

<16> 이러한 종래의 이면 조사형 CMOS 센서의 제조 방법은 다음과 같다. 먼저, 이온주입에 의하여 기판의 전면으로부터 일정 깊이의 깊이에 포토다이오드의 불순물 영역(2)을 형성한 후 화소 회로부(1)를 구성하는 회로 패턴층을 형성한다. 그리고 화소 회로부(1)에 접하여 기판의 전면에 지지기판(6)을 부착하고 기판의 후면을 연마하여 포토다이오드의 불순물 영역(2)을 기판의 일면으로부터 노출시킨다. 노출된 포토다이오드(2) 위로 칼라필터(3)와 마이크로 렌즈(4)를 포함하는 렌즈부(5)를 형성한다.

<17> 포토다이오드(2) 영역 중 칼라필터(3) 바로 아래 영역은 기판의 전면으로부터 가장 멀리 떨어진 곳에 해당되어 이온주입된 불순물의 농도가 균일하지 않을 확률이 높아진다. 이면 조사형 CMOS 센서에서는 포토다이오드(2) 간의 소자분리가 도핑 프로파일에 의하여 이루어지는데, 칼라필터(3) 아래 영역은 빛의 수광량이 많은 부분이면서도 불순물 농도의 불균일로 인하여 도핑 프로파일이 명확하지 않아 전기적인 크로스토크(electrical crosstalk)가 완벽하게 제거되지 못할 수 있다.

<18> 또한, 도 2에 도시한 바와 같이 칩의 에지에 있는 화소의 경우에는 마이크로 렌즈(3) 및 칼라필터(4)가 해당 포토다이오드(2)에 정렬되어 있지 않고 빛의 수광량을 높이기 위하여 포토다이오드(2)에 대하여 일정하게 이동(shift)하여 형성된다. 따라서 칩 에지의 화소의 경우에는 광학적 크로스토크(optical crosstalk)가 발생할 가능성이 높아진다.

발명이 이루고자 하는 기술적 과제

<19> 본 발명이 이루고자 하는 기술적 과제는 화소간 전기적 크로스토크와 광학적 크로스토크를 차단할 수 있는 이면

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조사형 CMOS 이미지 센서를 제공하는데 있다.

<20> 본 발명이 이루고자 하는 다른 기술적 과제는 화소간 전기적 크로스토크와 광학적 크로스토크를 차단할 수 있는 이면 조사형 CMOS 이미지 센서의 제조방법을 제공하는데 있다.

발명의 구성 및 작용

<21> 상기 목적을 달성하기 위한 본 발명에 따른 이면 조사형 CMOS 이미지 센서는 제1 면과 제2 면을 갖는 반도체 기판 내에서 상기 제1 면으로부터 상기 제2면을 향하여 확장되어 형성된 딥트렌치 구조의 소자분리막; 상기 딥트렌치 소자분리막에 의하여 한정되며 상기 제1 면으로부터 상기 제2면을 향하여 확장되어 형성된 포토다이오드; 상기 반도체 기판의 상기 제1 면에 인접하여 형성된 화소 회로부; 및 상기 반도체 기판의 상기 제2 면에 인접하여 형성된 랜즈부;를 포함한다.

<22> 상기 화소 회로부 위의 지지 기판을 더 포함할 수 있다.

<23> 상기 딥트렌치 구조의 소자분리막의 깊이는 3~10㎛인 것이 바람직하다.

<24> 상기 딥트렌치 구조의 소자분리막은 상기 포토다이오드를 통과하여 경사입사된 빛이 상기 소자분리막의 경계에서 전반사되도록 상기 반도체 기판보다 굴절율이 낮은 절연막으로 형성하는 것이 바람직하며, 실리콘 산화막일 수 있다.

<25> 상기 반도체 기판의 상기 제2 면과 상기 랜즈부 사이에 글래스 기판을 더 포함할 수 있다.

<26> 상기 화소 회로부는 전달 트랜지스터, 리셋 트랜지스터, 구동 트랜지스터, 선택 트랜지스터 및 배선을 포함할 수 있다.

<27> 상기 랜즈부는 상기 반도체 기판의 상기 제2 면에 인접한 칼라필터과 상기 칼라필터 위의 마이크로 랜즈를 포함할 수 있다.

<28> 상기 다른 목적을 달성하기 위한 본 발명에 따른 이면 조사형 CMOS 이미지 센서의 제조방법은 반도체 기판의 제1 면으로부터 딥트렌치 구조의 소자분리막을 형성하는 단계; 상기 소자분리막에 의하여 한정되는 상기 반도체 기판 내에 상기 제1 면으로부터의 이온주입에 의하여 포토다이오드 영역을 형성하는 단계; 상기 포토다이오드 영역 위로 상기 반도체 기판의 상기 제1 면에 화소 회로부를 형성하는 단계; 상기 화소 회로부가 형성된 상기 반도체 기판의 상기 제2 면을 연마하는 단계; 및 연마된 상기 반도체 기판의 상기 제2 면에 상기 포토다이오드에 정렬하여 랜즈부를 형성하는 단계;를 포함한다.

<29> 이하, 첨부된 도면을 참조하여 본 발명의 바람직한 실시예를 상세히 설명하기로 한다. 그러나, 본 발명은 여기서 설명되는 실시예들에 한정되지 않고 다른 형태로 구체화될 수도 있다. 오히려, 여기서 소개되는 실시예들은 개시된 내용이 철저하고 완전해질 수 있도록 그리고 당업자에게 본 발명의 사상이 충분히 전달될 수 있도록 하기 위해 제공되는 것이다. 도면들에 있어서, 층 및 영역들의 두께는 명확성을 기하여 위하여 과장된 것이다. 명세서 전체에 걸쳐서 동일한 참조번호들은 동일한 구성요소들을 나타낸다.

<30> 도 3은 본 발명의 일 실시예에 따른 이면 조사형 CMOS 이미지 센서의 일부를 단순화하여 보여주는 단면도이다. 도 3에는 포토다이오드(11), 화소 회로부(20) 및 랜즈부(30)를 포함하는 화소 어레이 부분이 도시되어 있다. 도 3에서 포토다이오드(11)가 형성되어 있는 반도체 기판(10)은 전면(front side, 13)이 아래를 향하고 있으며 이면(back side, 15)이 위를 향하고 있다. 이면 조사형 CMOS 이미지 센서에서는 빛이 반도체 기판(10)의 이면(15)으로부터 입사되므로 입사된 빛이 포토다이오드(11)에 도달할 수 있을 정도로 기판의 두께가 얇아야 한다.

<31> 반도체 기판(10) 내의 포토다이오드(11)는 n형 불순물 내의 p형 불순물 영역, 또는 p형 불순물 영역 내의 n형 불순물 영역에 의하여 형성될 수 있다. 포토다이오드(11) 아래의 반도체 기판(10)의 전면(13)에는 포토다이오드(11)와 함께 단위 화소를 구성하는 트랜지스터들과 배선들을 포함하는 화소 회로부(20)가 적층되어 형성되어 있다. 화소 회로부(20) 아래로 지지 기판(40)이 부착되어 있으며, 화소 회로부(20)와 지지 기판(40) 사이에는 패시베이션층(미도시)과 접착층(미도시)가 더 형성될 수 있다. 포토다이오드(11) 위의 반도체 기판(10)의 이면에는 칼라 필터(31) 및 마이크로 랜즈(33)를 포함하는 랜즈부(30)가 형성되어 있다. 포토다이오드(11)와 랜즈부(30) 사이에는 글래스와 같은 투명기판(미도시)이 더 형성될 수 있다.

<32> 본 발명에서는 인접하는 포토다이오드(11)가 딥트렌치 소자분리막(13)에 의하여 서로 분리된다. 딥트렌치 소자분리막(13)은 포토다이오드(11)의 깊이만큼 형성되거나 그보다 약간 얇게 형성될 수 있다. 딥트렌치 소자분리막(13)은 랜즈부(20)의 바로 아래까지 형성되어 있어서, 포토다이오드(11) 내에서 빛에 의해 생성된 전자 또는 전

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공이 수직으로 이동하기 못하고 인접 화소 영역으로 이동하여 발생하는 전기적 크로스토크(electrical crosstalk)를 방지할 수 있다. 이면 조사형 CMOS 이미지 센서에서는 포토다이오드(11)의 불순물 영역이 반도체 기판(10)의 전면으로부터 깊은 이온주입에 의하여 생성되므로 렌즈부(30) 아래의 반도체 기판(10)의 이면에 접하는 불순물 영역은 도핑 프로파일이 플트러져서 전기적 크로스토크가 발생할 수 있는데, 절연막인 딥트렌치 소자분리막(13)에 의하여 전기적 크로스토크가 방지될 수 있는 것이다.

<33> 또한 렌즈부(30)를 통해 경사를 갖고 입사된 빛은 포토다이오드(11)와 소자분리막(13)의 경계에서 전반사되어 인접 화소의 포토다이오드(11)로 통과하지 못하므로 광학적 크로스토크(optical crosstalk)를 방지할 수 있다. 종래의 CMOS 이미지 센서의 칩의 에지부의 화소는 비스듬히 들어오는 빛의 수광효율을 높이기 위하여 하나의 화소에서 렌즈부(30)와 이에 대응하는 포토다이오드(11)가 서로 수직으로 겹쳐지 않고 비스듬히 겹치도록 형성되어 인접 화소간 광학적 크로스토크가 발생할 가능성이 컸다. 그러나 본 발명에서는 도 4에 나타낸 바와 같이 포토다이오드(11) 사이의 딥트렌치 소자분리막(13)이 포토다이오드(11)의 실리콘보다 굴절율이 낮은 물질을 사용하여 딥트렌치 소자분리막(13)으로 비스듬히 들어오는 빛을 전반사함으로써 광학적 크로스토크를 방지할 수 있다.

<34> 도 5는 본 발명에 따른 이면 조사형 CMOS 이미지 센서의 제조방법을 순서대로 설명하기 위한 개략적인 순서도이다.

<35> 도 5를 참조하면, 먼저 반도체 기판에 딥트렌치 소자분리막을 형성한다(S10). 딥트렌치 소자분리막은 실리콘 질화막과 같은 하드마스크 패턴을 마스크로 하여 반도체 기판을 식각하여 딥트렌치를 형성한 후, 실리콘 산화막과 같은 절연막을 충전하여 형성한다. 절연막 매립은 딥트렌치를 매립하도록 절연막의 형성하고 평탄화한 후 하드마스크 패턴을 제거하여 이루어진다.

<36> 이어서 딥트렌치 소자분리막이 형성된 반도체 기판 내에 불순물의 이온주입에 의하여 포토다이오드 영역을 형성한다(S20). 포토다이오드 영역은 n형 불순물 내에 p형 불순물 영역을 형성하거나 p형 불순물 영역 내의 n형 불순물 영역을 형성함으로써 만들 수 있다.

<37> 반도체 기판에 포토다이오드 영역을 만든 후에 기판 위로 전달 트랜지스터, 리셋 트랜지스터, 구동 트랜지스터, 선택 트랜지스터와 같은 단위 화소를 구성하는 트랜지스터와 배선을 포함하는 화소 회로부를 형성한다(S30).

<38> 화소 회로부가 형성된 반도체 기판의 전면에 지지 기판을 부착한다(S40). 지지기판의 부착 전 화소 회로부를 보호하기 위한 패시베이션층을 형성할 수 있다.

<39> 지지기판을 부착한 후 반도체 기판의 이면으로부터 포토다이오드 영역으로 빛이 입사될 수 있을 정도로 반도체 기판의 이면을 갈고 화학적 기계적 연마를 수행하여 반도체 기판의 두께를 얇게 만든다(S50).

<40> 반도체 기판의 이면의 포토다이오드 위로 칼라필터 및 마이크로 렌즈를 포함하는 렌즈부를 형성한다(S60). 이때 반도체 기판의 이면과 렌즈부 사이에 글래스 기판을 더 형성되어 있을 수도 있다.

<41> 이상에서 본 발명의 실시예에 대하여 상세히 설명하였지만, 설명한 본 발명은 전술한 실시예 및 첨부된 도면에 의해 한정되는 것이 아니고, 본 발명의 기술적 사상을 벗어나지 않는 범위 내에서 여러 가지 치환, 변형 및 변경이 가능하다는 것이 본 발명이 속하는 기술분야에서 통상의 지식을 가진 자에게 있어 명백할 것이다.

발명의 효과

<42> 본 발명에 의하면 이면 조사형 CMOS 이미지 센서에서 화소 어레이의 포토다이오드를 딥트렌치 구조의 소자분리막으로 격리함으로써 화소간 전기적 크로스토크와 광학적 크로스토크를 차단할 수 있다.

도면의 간단한 설명

<1> 도 1은 종래의 이면 조사형 CMOS 센서의 화소 어레이 영역의 개략적인 단면도이다.

<2> 도 2은 종래의 이면 조사형 CMOS 센서의 칩 에지 부분의 화소 어레이 영역의 개략적인 단면도이다.

<3> 도 3은 본 발명의 일 실시예에 따른 이면 조사형 CMOS 이미지 센서의 화소 어레이 영역의 개략적인 단면도이다.

<4> 도 4는 본 발명에 따른 이면 조사형 CMOS 이미지 센서의 제조방법을 순서대로 설명하기 위한 개략적인 순서도이다.

<5> * 도면의 주요 부분에 대한 부호의 설명

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<6> 10: 반도체 기판 11: 포토다이오드

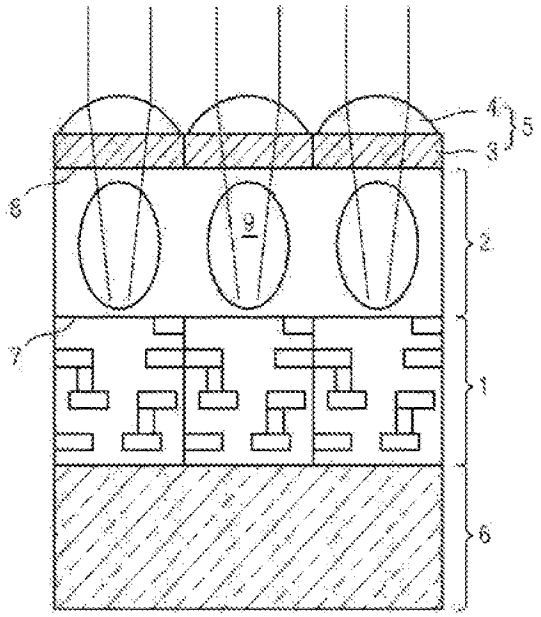
<7> 13: 빌트인 소자분리막 20: 화소 회로부

<8> 30: 렌즈부 31: 컬러필터

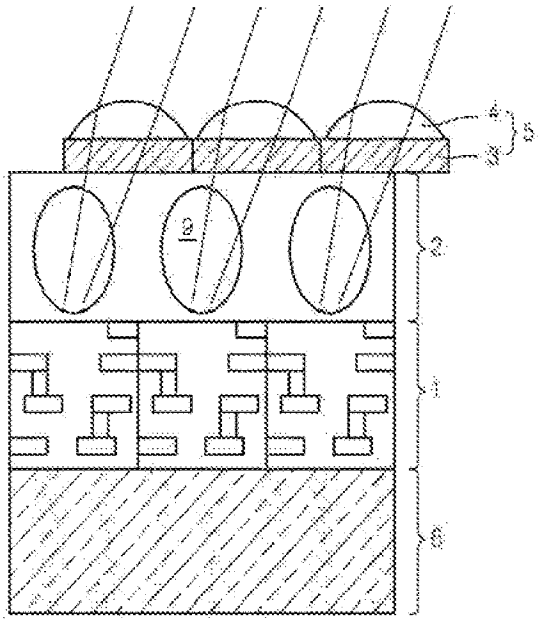
<9> 33: 마이크로 렌즈 40: 지지기판

도면

도면1

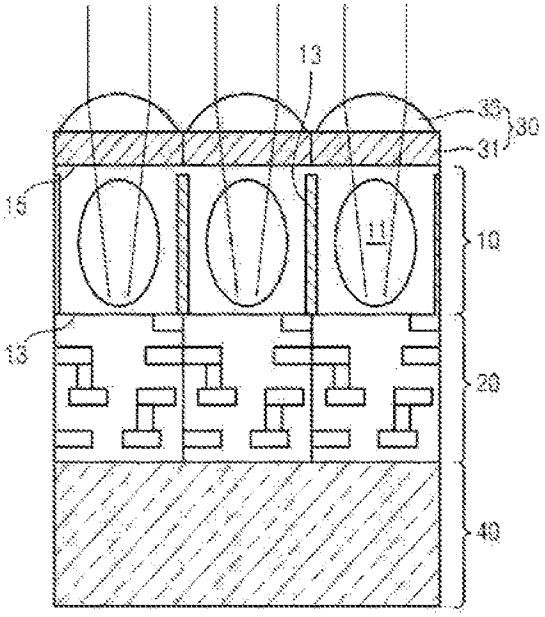


도면2

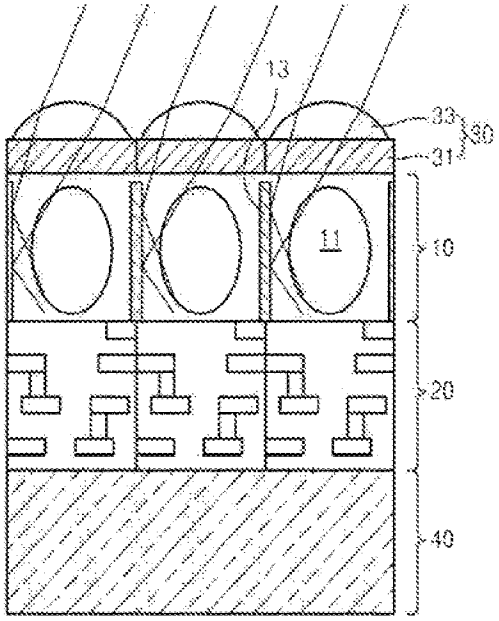


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도면3

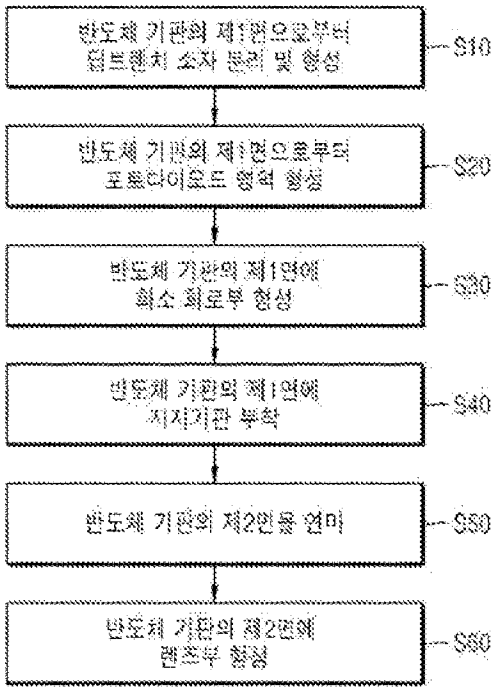


도면4



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도면5



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Espacenet

Bibliographic data: KR20080097709 (A) — 2008-11-06

IMAGE SENSOR AND METHOD FOR FABRICATING OF THE SAME

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Classification: - international:*H01L27/146*
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Priority number(s): KR20070042900 20070503

Abstract of KR20080097709 (A)

An image sensor and a method for fabricating the same are provided to improve the sensitivity of the image sensor by increasing the refractive index of the incident light. The image sensor includes the color filter array(30) formed on the array of pixel substrate(10); The first micro lens formed on the color filter array(50,51,52); the supplementary light-collecting portion(61) formed on the array of pixel of the substrate including first micro lens. The supplementary light-collecting portion is positioned in the gap region between the first micro lens. The trench having the form in which the floor side is pressed in the supplementary light-collecting portion is formed.

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DESCRIPTION KR20080097709

BACKGROUND OF THE INVENTION 1. Field of the Invention [0001] The present invention relates to an image sensor,

1 is a view showing a conventional image sensor.

2 to 6 are views showing a manufacturing process of the image sensor according to the first embodiment.

7 to 11 are views showing a manufacturing process of the image sensor according to the second embodiment.

In the present embodiment, an image sensor and a manufacturing method thereof are disclosed. An image sensor is a semiconductor device that converts an optical image into an electrical signal and is mainly composed of a charge coupled device (CCD) and a complementary metal oxide silicon (CMOS) image sensor Sensor (CIS). On the other hand, the CCD has a disadvantage in that the driving method is complicated, power consumption is high, and a multistage photo process is required, which complicates the manufacturing process. Recently, as a next generation image sensor for overcoming the disadvantages of the charge - Moss image sensors are attracting attention. The CMOS image sensor forms a photodiode and a MOS transistor in a unit pixel to sequentially detect an electrical signal of each unit pixel in a switching manner to realize an image. In manufacturing such various image sensors, focusing techniques for increasing the photo

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sensitivity of the image sensor have been developed, and a typical example of the focusing technique is forming a microlens. In the image sensor shown in FIG. 1, a micro lens is formed by patterning an organic photoresist for a microlens on a pixel array substrate 1 on which a unit pixel 2 including a photodiode (not shown) is formed and then performing a reflow process The convex microlenses 3 are formed to refract the path of the incident light to condense a larger amount of light into the photodiode region. The microlenses 3 are formed by a single patterning process and a gap D of about 0.1 to 0.2 μ m is generated between the microlenses 3 when the reflow process is performed. Particularly, the light entering between the gaps D of the microlenses 3 goes straight as they are, and is not condensed by the photodiodes, which causes a decrease in the photosensitivity of the image sensor. Also, there is a problem that light not condensed passes through the gap D of the microlenses 3 and is detected by unit pixels disposed on the pixel array substrate 1, thereby generating noise and crosstalk.

The present embodiment provides an image sensor capable of increasing light efficiency by primarily refracting light at an upper portion of a microlens and condensing light with a microlens, and a method of manufacturing the same. Embodiments of the present invention provide an image sensor capable of improving light sensitivity by reflecting light incident between gaps of microlenses, and a method of manufacturing the same.

The image sensor of the first embodiment comprises: a color filter array formed on a pixel array substrate; A first micro - lens formed on the color filter array; And an auxiliary light collecting portion formed on the color filter array including the first microlenses. The method of manufacturing an image sensor of the first embodiment further includes: forming a color filter array on a pixel array substrate; Forming a first microlens on the color filter array; And forming an auxiliary light collecting portion on the color filter array including the first microlenses. The image sensor of the second embodiment includes: a color filter array formed on a pixel array substrate; A planarization layer formed on the color filter array; And a microlens formed on the planarization layer, wherein a reflection film is formed on the planarization layer so as to be located in a gap region of the microlens. Forming a filter array; Forming a planarization layer including a reflective film on the color filter array; and forming a microlens on the planarization layer. Hereinafter, a method of manufacturing an image sensor according to an embodiment of the present invention will be described in detail with reference to the accompanying drawings. In the description of the embodiments, when it is described as being formed on & quot; on / over & quot; of each layer, the on / over may be directly and / indirectly formed. The thickness and size of each layer in the drawings are exaggerated, omitted, or schematically shown for convenience and clarity of explanation. Also, the size of each component does not entirely reflect the actual size.

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& Lt; First Embodiment & gt; Fig. 6 shows an image sensor according to the first embodiment. Referring to Fig. 6, the image sensor of the first embodiment includes a color filter array 30 formed on a pixel array substrate 10; First microlenses (50, 51, 52) formed on the color filter array (30); And an auxiliary condensing unit 61 formed on the pixel array substrate 10 including the first microlenses 50, 51, and 52.

The auxiliary condensing unit 61 includes a trench 62 having a concave bottom surface to be positioned between the first microlenses 50, that is, a gap region. And a second microlens 81 formed on the trench 62 of the auxiliary light collecting part 61. In particular, the second microlens 81 and the first microlenses 50, 51 and 52 may be formed of the same material. In addition, the auxiliary light - collecting portion 61 may be formed of an oxide film (SiO2). In addition, the upper surface of the first microlens 50 may be formed in a convex shape, and the lower surface of the second microlens 81 may be formed in a concave shape. As described above, since the auxiliary condensing portion formed of the oxide film is formed on the first microlens, the light incident from the object is refracted through the auxiliary condensing portion first and then incident on the first microlens. Therefore, The sensor performance of the image sensor can be improved. In addition, the bottom surface of the trench formed in the auxiliary light collecting portion is formed in a concave shape, and when the light incident from the object goes straight to the gap region of the first microlens, it passes through the trench region. Then, due to the concave shape of the bottom surface of the trench, the refractive index of the light is increased, thereby preventing the light from passing through the gap region of the first microlens, thereby improving the quality of the image sensor. In addition, by forming the second microlens in the trench of the auxiliary light collecting portion, when the light incident from the object goes straight to the gap region of the first microlens, the light passes through the second microlens. Then, the concave shape of the second microlens bottom surface causes the light to be bent outward and incident on the neighboring first microlens, so that the light collecting ratio of the image sensor is increased and the photosensitivity can be improved. Hereinafter, the manufacturing process of the image sensor according to the first embodiment will be described with reference to FIGS. 2 to 6. FIG. 2, a color filter array 30 is formed on a pixel array substrate 10 in a region corresponding to a unit pixel. The pixel array substrate 10 includes a unit pixel (not shown) formed of a photodiode (not shown) for sensing light incident through the color filter array 30 and transistors (not shown) for processing charges generated in the photodiode 11).

The pixel array substrate 10 may include a metal wiring layer 20 formed of a metal wiring (not shown) for transmitting a signal to the unit pixel 11 and an insulating film (not shown), and a passivation film (not shown) . Then, the color filter array 30 is

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formed on the pixel array substrate 10. The color filter array 30 forms a color filter layer (not shown) including a photosensitive material and a pigment or a photosensitive material and a dye on the pixel array substrate 10 through a spin coating process or the like. Then, the color filter layer is exposed by a pattern mask and developed to form a color filter array 30 on the pixel array substrate 10. The color filter array 30 has one color filter for each unit pixel to separate colors from incident light. For example, the first color filter of the color filter array 30 is red, the second color filter is green, and the third color filter is composed of three colors of blue , Adjacent color filters slightly overlap each other to form a step. A planarization layer 40 may be formed on the color filter array to compensate for the level difference of the color filter array 30. The first microlenses 50, 51, and 52 are formed on the color filter array 30 to condense light into the photodiode. The first micro lenses 50, 51, and 52 coat the photoresist for forming microlenses onto the color filter array 30 through a spin process or the like. After the photoresist film (not shown) is selectively exposed and developed, a photoresist pattern (not shown) is formed on each of the color filters. Thereafter, a reflow process is performed to form first dome - shaped first microlenses 50, 51, and 52 having a convex shape. At this time, a gap D1 may be generated between the adjacent first microlenses 51 and 52 in the first microlens 50. Referring to FIG. 3, in order to prevent light from being incident on the gap D1 between the first microlenses 50, 51, and 52, the first microlenses 50, 51, The auxiliary light collecting portion 61 is formed on the substrate 10.

The auxiliary light - collecting unit 61 is formed by depositing an oxide film (SiO 2) 60 on the pixel array substrate 10 including the first microlenses 50, 51, and 52. Since the refractive index of the first microlenses 50, 51 and 52 is about 1.7 and the refractive index of the oxide film 60 is about 1.4, the light incident through the air having the refractive index of about 1 passes through the oxide film 60 And the incident light is incident on the first microlenses 50, 51, and 52, so that the light collecting rate to the photodiode can be improved. Referring to FIG. 4, a photoresist film is coated on the oxide film 60 and patterned to form a mask pattern 71. The mask pattern 71 is formed on the oxide film 60 such that the upper surface of the auxiliary light collecting portion 61 at a portion corresponding to the gap D1 of the first microlenses 50, 51, . 5, when the auxiliary light - collecting portion 61 is etched using the mask pattern 71 as an etching mask, a trench having a width corresponding to the gap region of the first microlenses 50, 51, 62 are formed. For example, the trench 62 may be etched by a dry etching method, and the bottom surface of the trench 62 may be formed to have a concave shape by controlling the injection gas. When the bottom surface of the trench 62 of the auxiliary light collecting part 61 is formed in a concave shape and light is incident on the trench 62 of the auxiliary light collecting part 61 as described above, when the concave shape of the bottom surface of the trench 62 The incident light can be converged by the

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first microlenses 50, 51 and 52 without being incident on the region of the gap D1. 6, the mask pattern 71 is removed and a photoresist for microlens formation similar to that of the first microlens 50 is applied on the auxiliary light collecting portion 61 on which the trench 62 is formed, The surface of the light condensing portion 61 is exposed and planarized. A second microlens 81 is formed in the trench 62 of the auxiliary light collecting part 61. The bottom surface of the second microlens 81 is formed to have a concave shape with respect to the first microlens 50 according to the shape of the bottom surface of the trench 62.

Therefore, as shown in FIG. 6, since the second microlens 81 having a concave shape is formed on the upper side of the auxiliary light collecting part 61 at a position corresponding to the gap area, 1 light, the light is firstly refracted by the second microlens 81 to the outer region with respect to the straight - ahead direction, and the sub - The light is refracted by the light portion 61 and then incident on the adjacent first microlenses 51 and 52 of the first microlens 50 to increase the light efficiency of the photodiode. In addition, incident light is prevented from being incident on the gap region, so that crosstalk and noise can be prevented, and the photosensitivity can be improved. Further, an auxiliary light collecting part formed of an oxide film on the first microlens can prevent image defects that may occur from impact or particles in a subsequent package or bump process. & Lt; Second Embodiment & gt; Fig. 11 shows an image sensor according to the second embodiment. The image sensor of the second embodiment includes a color filter array 130 formed on a pixel array substrate 100; A planarization layer 141 formed on the color filter array 130; And a reflective layer 181 is formed on the planarization layer 140 so as to be positioned in a gap D2 between the microlenses 150, 151 and 152. The reflective layer 181 is formed on the planarization layer 140, In addition, the planarization layer 140 may be an oxide film (SiO 2), and the reflective layer 181 may be formed of a metal material. As described above, the reflection film is formed on the surface of the planarization layer exposed by the gap region of the microlens, and when the light entering from the object goes straight to the gap region of the microlens, it is reflected back to the outside by the reflection film. Therefore, it is possible to prevent the occurrence of crosstalk and noise by preventing light from entering the gap region of the microlens in advance, thereby improving the quality of the image sensor. Hereinafter, a manufacturing process of the image sensor according to the second embodiment will be described with reference to FIGS. 7 to 11. FIG.

Referring to FIG. 7, a color filter array 130 is formed on a pixel array substrate 100 in a region corresponding to the unit pixel 110. FIG. The pixel array substrate 100 includes a unit pixel (not shown) formed of a photodiode (not shown) for sensing light incident

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through the color filter array 130 and transistors (not shown) for processing charges generated in the photodiode 110). The pixel array substrate 100 may include a metal wiring layer 120 formed of a metal wiring (not shown) and a passivation film (not shown). The metal wiring layer 120 may transmit a signal to the unit pixel 110 . The color filter array 130 is formed on the pixel array substrate 100. The color filter array 130 forms a color filter layer (not shown) including a photosensitive material and a pigment or a photosensitive material and a dye on the pixel array substrate 100 through a spin coating process or the like. Then, the color filter layer is exposed by a pattern mask and developed to form a color filter on the pixel array substrate 100. The color filter array 130 has one color filter for each unit pixel 110 to separate colors from incident light. For example, the first color filter of the color filter array 130 is red, the second color filter is green, and the third color filter is composed of three colors of blue , Adjacent color filters slightly overlap each other to form a step. A planarization layer 140 is formed on the color filter array in order to compensate the step of the color filter array 30. For example, the planarization layer 140 may have an oxide film (SiO2) having a thickness of 6000 to 90000 angstroms. Referring to FIG. 8, a photoresist film is coated on the planarization layer 140 and patterned to form a mask pattern 170. The mask pattern 170 is formed to expose the upper surface of the planarization layer 61 corresponding to the gap D2 of the microlenses 150, 151 and 152 to be formed.

When the planarization layer 140 is etched using the mask pattern 170 as an etching mask, a trench 142 is formed. For example, the width of the trench 142 may be about 0.1 to 0.3 탆, and in order to protect the color filter array 130 formed under the planarization layer 141 when the trench 142 is formed, So that the planarization layer 141 is not completely etched. 9 and 10, a metal material is deposited on the planarization layer 141 on which the trench 142 is formed, and then a planarization process is performed to form a reflection film 181 in the trench 142. For example, the reflective layer 181 may be formed by depositing TiN, Al, W or the like by CVD or PVD to form a reflective layer 180, and then planarizing the surface of the planarized layer 140 by a CMP process A reflection film 181 may be formed in the trench 142. Referring to FIG. 11, microlenses 150, 151, and 152 are formed on the planarization layer 140 to condense light into a photodiode. The microlenses 150, 151, and 152 coat the photoresist for microlens formation on the planarization layer 140 through a spin process or the like. After the photoresist film (not shown) is selectively exposed and developed, a photoresist pattern (not shown) is formed on each of the color filters. Thereafter, a reflow process is performed to form dome - shaped microlenses 150, 151 and 152 having a convex shape. At this time, a gap D2 may be generated between the microlenses 150 and neighboring microlenses 151 and 152, and a gap D2 formed between the microlenses 150, 151, The reflective film 181 formed on the reflective film 140 is exposed. 11, a reflection film 181 is formed between the micro - lenses 150, 151

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and 152, so that light incident from an object is emitted from the micro - lens 150, The light that has not passed through the microlenses 150, 151, and 152 is reflected by the reflection layer 181, and is reflected by the reflection layer 181. Therefore, So that the photosensitivity of the photodiode can be improved.

The reflection film 181 can block the incidence of the light that is not condensed in the gap D2 of the microlens 150 so that noise and crosstalk of the photodiode disposed on the pixel array substrate 100 It is possible to improve the quality of the image sensor by preventing occurrence in advance. It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the invention. It will be clear to those who have.

As described above, according to the image sensor and the manufacturing method thereof according to the first embodiment, the refractive index of the incident light is increased to improve the light collection efficiency of the microlens, thereby improving the sensor sensitivity of the image sensor. According to the first embodiment, the auxiliary light collecting portion formed on the upper portion of the microlens can prevent image defects that may be generated from impact or particles in a subsequent package or bump process. According to the image sensor and the method of manufacturing the same according to the second embodiment, a reflection film is formed in the gap region of the microlens to reflect light incident on the gap region, thereby preventing crosstalk between pixels and noise from occurring. The reliability can be improved.

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CLAIMS KR20080097709

1.
A color filter array formed on the pixel array substrate; A first micro - lens formed on the color filter array; And an auxiliary collecting portion formed on the pixel array substrate including the first microlens.

2.
The image sensor according to claim 1, wherein a trench having a concave bottom surface is formed in the auxiliary condensing unit so as to be located in a gap region between the first microlenses.

3.
The image sensor according to claim 1 or 2, further comprising a second microlens formed on the trench of the auxiliary light collecting portion.

4.
The image sensor according to any one of claims 1 to 3, wherein the auxiliary condenser is formed of an oxide film (SiO2).

5.
Forming a color filter array on the pixel array substrate; Forming a first microlens on

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the color filter array; And forming an auxiliary light collecting portion on the color filter array including the first microlenses.

6.

The method according to claim 5, wherein the forming of the auxiliary light collecting part comprises: forming an oxide film on the color filter array including the first microlenses, The method comprising the steps of:

7.

7. The method of claim 6, further comprising forming a second microlens by depositing the same material as the first microlens on the trench.

8.

A color filter array formed on the pixel array substrate; A planarization layer formed on the color filter array; And a microlens formed on the planarization layer, wherein the planarization layer includes a reflective film formed in a gap region of the microlens.

9.

Forming a color filter array on the pixel array substrate; Forming a planarization layer including a reflective film on the color filter array; and forming a microlens on the planarization layer.

10.

10. The image sensor of claim 9, wherein the planarization layer is an oxide film and the reflective film is formed of a metal material.

11.

10. The method of claim 9, wherein forming the planarization layer further comprises: forming an oxide film on the color filter array; Forming a mask on the oxide film; Etching the oxide film by the mask to form a trench in a region where a gap of the microlens is to be formed; And filling the trench with a metal material to form a reflective film.

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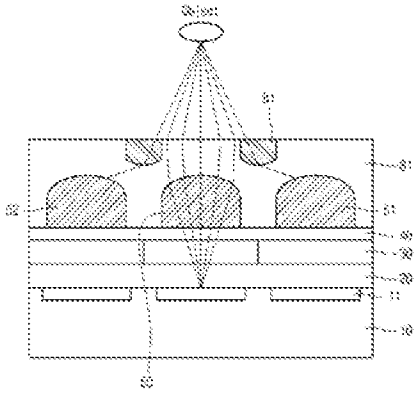
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(54) 이미지 센서 및 그의 제조방법

(57) 요 약

본 실시예의 이미지 센서는, 픽셀 어레이 기판 상에 형성된 컬러필터 어레이; 상기 컬러필터 어레이 상에 형성된 제1 마이크로렌즈; 및 상기 제1 마이크로렌즈를 포함하는 컬러필터 어레이 상에 형성된 보조 집광부를 포함한다.

대 표 도 - 도6



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특허청구의 범위

청구항 1

픽셀 어레이 기판 상에 형성된 컬러필터 어레이;

상기 컬러필터 어레이 상에 형성된 제1 마이크로렌즈; 및

상기 제1 마이크로렌즈를 포함하는 픽셀 어레이 기판 상에 형성된 보조 집광부를 포함하는 이미지 센서.

청구항 2

제1항에 있어서,

상기 제1 마이크로렌즈 사이의 갭 영역에 위치되도록 상기 보조 집광부에는 바닥면이 오목한 형태를 갖는 트렌치가 형성된 이미지 센서.

청구항 3

제1항 또는 제2항에 있어서,

상기 보조 집광부의 트렌치에 형성된 제2 마이크로렌즈를 포함하는 이미지 센서.

청구항 4

제1항 내지 제3항 중 어느 한 항에 있어서,

상기 보조 집광부는 산화막(SiO_2)으로 형성된 것을 특징으로 하는 이미지 센서.

청구항 5

픽셀 어레이 기판 상에 컬러필터 어레이를 형성하는 단계;

상기 컬러필터 어레이 상에 제1 마이크로렌즈를 형성하는 단계;

상기 제1 마이크로렌즈를 포함하는 상기 컬러필터 어레이 상부로 보조 집광부를 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 6

제5항에 있어서,

상기 보조 집광부를 형성하는 단계는,

상기 제1 마이크로렌즈를 포함하는 상기 컬러필터 어레이 상부로 산화막을 형성하는 단계;

상기 제1 마이크로렌즈 사이에 바닥면이 오목한 형태의 트렌치를 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 7

제6항에 있어서,

상기 트렌치에 제1 마이크로렌즈와 동일한 물질을 증착하여 제2 마이크로렌즈를 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 8

픽셀 어레이 기판 상에 형성된 컬러필터 어레이;

상기 컬러필터 어레이 상에 형성된 평탄화층;

상기 평탄화층 상에 형성된 마이크로렌즈를 포함하며,

상기 평탄화층에는 상기 마이크로렌즈의 갭 영역에 위치되도록 반사막이 형성된 것을 포함하는 이미지 센서.

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청구항 9

픽셀 어레이 기판 상에 컬러필터 어레이을 형성하는 단계;

상기 컬러필터 어레이 상에 반사막을 포함하는 평탄화층을 형성하는 단계;및

상기 평탄화층 상에 마이크로렌즈를 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 10

제9항에 있어서,

상기 평탄화층은 산화막이고 상기 반사막은 금속물질로 형성된 것을 포함하는 이미지 센서.

청구항 11

제9항에 있어서,

상기 평탄화층을 형성하는 단계는,

상기 컬러필터 어레이 상에 산화막을 형성하는 단계;

상기 산화막 상에 마스크를 형성하는 단계;

상기 마스크에 의해 산화막을 식각하여 마이크로렌즈의 갭이 형성될 영역에 트렌치를 형성하는 단계;

상기 트렌치에 금속물질을 매립하여 반사막을 형성하는 단계를 포함하는 이미지 센서의 제조방법.

명 세 서

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

<4> 본 실시예에서는 이미지 센서 및 그의 제조방법을 개시한다.

<5> 이미지 센서(Image sensor)는 광학적 영상(optical image)을 전기적 신호로 변환시키는 반도체 소자로써, 크게 전하결합소자(charge coupled device; CCD)와 씨모스(CMOS; Complementary Metal Oxide Silicon) 이미지 센서(Image Sensor)(CIS)로 구분된다.

<6> 한편, CCD는 구동 방식이 복잡하고, 전력 소비가 클 뿐만 아니라, 다단계의 포토 공정이 요구되므로 제조 공정이 복잡한 단점을 갖고 있으므로, 최근에는 상기 전하 결합 소자의 단점을 극복하기 위한 차세대 이미지 센서로서 씨모스 이미지 센서가 주목을 받고 있다.

<7> 씨모스 이미지센서는 단위 화소 내에 포토 다이오드와 모스 트랜지스터를 형성시킴으로써 스위칭 방식으로 각 단위 화소의 전기적 신호를 순차적으로 검출하여 영상을 구현한다.

<8> 이러한 다양한 이미지 센서를 제조함에 있어서, 이미지 센서의 광감도(photo sensitivity)를 증가시키기 위한 집광기술들이 개발되고 있으며, 상기 집광 기술의 대표적인 예가 마이크로렌즈를 형성하는 것이다.

<9> 도 1에 도시된 이미지 센서에서 마이크로렌즈는 포토다이오드(미도시)를 포함하는 단위화소(2)가 형성된 픽셀 어레이 기판(1) 상부에 마이크로렌즈용 유기물 포토레지스트를 패터닝한 후 리플로우 공정을 진행하여 볼록형 마이크로 렌즈(3)를 형성함으로써 입사광의 경로를 굴절시켜 보다 많은 양의 빛을 포토다이오드 영역으로 집광한다.

<10> 상기와 같은 마이크로렌즈(3)는 한편의 패터닝 공정에 의해 형성되어 리플로우 공정을 거치면 각 마이크로 렌즈(3) 사이에 약 0.1 내지 0.2㎛의 갭(gap)(D)이 발생된다.

<11> 특히, 상기 마이크로렌즈(3)의 갭(D) 사이로 입사되는 빛은 그대로 직진하게 되어 포토다이오드로 집광되지 않게 되므로 이미지 센서의 광감도를 저하시키는 원인이 된다.

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<12> 또한, 상기 마이크로렌즈(3)의 갭(D) 사이로 집광되지 않은 빛이 통과하여 픽셀 어레이 기판(1)에 배치된 단위 픽셀에 감지됨으로써 노이즈 및 크로스 토크가 발생되는 문제점이 있다.

발명이 이루고자 하는 기술적 과제

<13> 본 실시예는 마이크로렌즈의 상부에서 광을 일차적으로 굴절시켜 마이크로렌즈로 광을 집광시켜 광 효율을 증대시킬 수 있는 이미지 센서 및 그의 제조방법을 제공한다.

<14> 본 발명의 실시예는 마이크로렌즈의 갭 사이로 입사되는 광을 반사시켜 광감도를 향상시킬 수 있는 이미지 센서 및 그의 제조방법을 제공한다.

발명의 구성 및 작용

<15> 제1 실시예의 이미지 센서는, 픽셀 어레이 기판 상에 형성된 컬러필터 어레이; 상기 컬러필터 어레이 상에 형성된 제1 마이크로렌즈; 및 상기 제1 마이크로렌즈를 포함하는 컬러필터 어레이 상에 형성된 보조 집광부를 포함한다.

<16> 또한 제1 실시예의 이미지 센서의 제조방법은, 픽셀 어레이 기판 상에 컬러필터 어레이를 형성하는 단계; 상기 컬러필터 어레이 상에 제1 마이크로렌즈를 형성하는 단계; 상기 제1 마이크로렌즈를 포함하는 상기 컬러필터 어레이 상부로 보조 집광부를 형성하는 단계를 포함한다.

<17> 제2 실시예의 이미지 센서는, 픽셀 어레이 기판 상에 형성된 컬러필터 어레이; 상기 컬러필터 어레이 상에 형성된 평탄화층; 상기 평탄화층 상에 형성된 마이크로렌즈를 포함하며, 상기 평탄화층에는 상기 마이크로렌즈의 갭 영역에 위치되도록 반사막이 형성된 것을 포함한다

<18> 또한, 제2 실시예의 이미지 센서의 제조방법은, 픽셀 어레이 기판 상에 컬러필터 어레이를 형성하는 단계; 상기 컬러필터 어레이 상에 반사막을 포함하는 평탄화층을 형성하는 단계;및 상기 평탄화층 상에 마이크로렌즈를 형성하는 단계를 포함한다.

<19> 이하, 본 발명의 실시예에 따른 이미지 센서의 제조방법을 첨부한 도면을 참조하여 상세히 설명한다.

<20> 실시예의 설명에 있어서, 각 층의 "상/위(on/over)"에 형성되는 것으로 기재되는 경우에 있어, 상/위(on/over)는 직접(directly)과 또는 다른 층을 개재하여(indirectly) 형성되는 것을 모두 포함한다.

<21> 도면에서 각층의 두께나 크기는 설명의 편의 및 명확성을 위하여 과장되거나 생략되거나 또는 개략적으로 도시되었다. 또한 각 구성요소의 크기는 실제크기를 전적으로 반영하는 것은 아니다.

<22> <제1 실시예>

<23> 도 6은 제1 실시예에 따른 이미지 센서를 도시하고 있다.

<24> 도 6을 참조하여, 제1 실시예의 이미지 센서는 픽셀 어레이 기판(10) 상에 형성된 컬러필터 어레이(30); 상기 컬러필터 어레이(30) 상에 형성된 제1 마이크로렌즈(50,51,52); 및 상기 제1 마이크로렌즈(50,51,52)를 포함하는 픽셀 어레이 기판(10) 상에 형성된 보조 집광부(61)를 포함한다.

<25> 또한, 상기 제1 마이크로렌즈(50) 사이 즉, 갭 영역에 위치되도록 상기 보조 집광부(61)에는 바닥면이 오목한 형태로 형성된 트렌치(62)를 포함한다.

<26> 또한, 상기 보조 집광부(61)의 트렌치(62)에 형성된 제2 마이크로렌즈(81)를 포함한다. 특히, 상기 제2 마이크로렌즈(81)와 상기 제1 마이크로렌즈(50,51,52)는 동일한 물질로 형성될 수 있다.

<27> 또한, 상기 보조 집광부(61)는 산화막(SiO_2)으로 형성될 수 있다.

<28> 또한, 상기 제1 마이크로렌즈(50)의 상면은 볼록한 형태로 형성되고, 제2 마이크로렌즈(81)의 하부면은 오목한 형태로 형성될 수 있다.

<29> 상기와 같이 제1 마이크로렌즈의 상부에 산화막으로 형성된 보조 집광부가 형성되어 물체로부터 입사되는 빛은 상기 보조 집광부를 통해 1차로 굴절된 후 제1 마이크로렌즈로 입사되기 때문에 제1 마이크로렌즈의 집광율을 향상시켜 이미지 센서의 센서티비티를 향상시킬 수 있다.

<30> 또한, 상기 보조 집광부에 형성된 트렌치의 바닥면이 오목한 형태로 형성되어 물체로부터 입사되는 빛이 상기

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제1 마이크로렌즈의 갭 영역으로 직진할 경우 트렌치 영역으로 통과하게 된다. 그러면 상기 트렌치 바닥면의 오목한 형태에 의하여 빛은 굴절률이 높아지게 되어 제1 마이크로렌즈의 갭 영역을 통과하는 것을 방지하므로써 이미지센서의 품질을 향상시킬 수 있다.

<31> 또한, 상기 보조 집광부의 트렌치에 제2 마이크로렌즈를 형성함으로써, 물체로부터 입사되는 빛이 상기 제1 마이크로렌즈의 갭 영역으로 직진할 경우 상기 제2 마이크로렌즈를 통과하게 된다. 그러면 상기 제2 마이크로렌즈 바닥면의 오목한 형태에 의하여 빛은 바깥 쪽으로 꺾이게 되어 이웃하는 제1 마이크로렌즈로 입사되므로 이미지 센서의 집광율이 높아져 광감도를 향상시킬 수 있다.

<32> 이하, 도 2 내지 도 6을 참조하여 제1 실시예에 따른 이미지 센서의 제조공정을 설명한다.

<33> 도 2를 참조하여, 픽셀 어레이 기판(10) 상으로 단위화소에 대응하는 영역에 컬러필터 어레이(30)를 형성한다.

<34> 상기 픽셀 어레이 기판(10)은 컬러필터 어레이(30)를 통해 입사된 빛을 감지하는 포토다이오드(미도시) 및 상기 포토다이오드에서 발생된 신호를 처리하는 트랜지스터들(미도시)로 구성된 단위화소(11)를 포함한다.

<35> 또한 상기 픽셀 어레이 기판(10)은 단위화소(11)로 신호를 전달하는 금속배선(미도시) 및 절연막(미도시)으로 이루어지는 금속배선층(20) 및 패시베이션막(미도시)을 포함할 수 있다.

<36> 그리고, 상기 픽셀 어레이 기판(10) 상에 상기 컬러필터 어레이(30)를 형성한다.

<37> 상기 컬러필터 어레이(30)는 감광물질 및 안료 또는 감광물질 및 염료를 포함하는 컬러필터층(미도시)을 스핀 코팅 공정등을 통해 픽셀 어레이 기판(10) 상에 형성한다. 이어서, 상기 컬러필터층을 패턴 마스크에 의하여 노광한 후 현상하여 상기 픽셀 어레이 기판(10) 상에 컬러필터 어레이(30)를 형성한다.

<38> 상기 컬러필터 어레이(30)는 각각의 단위화소 마다 하나의 컬러필터가 형성되어 입사하는 빛으로부터 색을 분리해 낸다. 예를 들어, 상기 컬러필터 어레이(30)의 제1 컬러필터는 레드(Red)이고, 제2 컬러필터는 그린(Green)이며, 제3 컬러필터는 블루(Blue)의 3가지 색으로 이루어지며, 인접한 컬러필터들은 서로 약간씩 오버랩되어 단차가 형성된다.

<39> 상기 컬러필터 어레이(30)의 단차를 보완하기 위하여, 상기 컬러필터 어레이 상부로 평탄화층(40)이 형성될 수도 있다.

<40> 그리고, 상기 컬러필터 어레이(30) 상부로 포토다이오드로의 집광을 위한 제1 마이크로렌즈(50,51,52)를 형성한다.

<41> 상기 제1 마이크로렌즈(50,51,52)는 상기 컬러필터 어레이(30) 상부로 마이크로 렌즈 형성용 포토레지스트를 스핀 공정등을 통해 도포한다. 그리고, 상기 포토레지스트막(미도시)을 선택적으로 노광 및 현상한 후 각각의 컬러필터 상부에 포토레지스트 패턴(미도시)을 형성한다. 이후, 리플로우 공정을 실시하여 볼록한 형상을 갖는 돔 형태의 제1 마이크로렌즈(50,51,52)를 형성한다.

<42> 이때, 상기 제1 마이크로렌즈(50)는 이웃하는 제1 마이크로렌즈(51,52) 사이에 갭(gap)(D1)이 발생될 수 있다.

<43> 도 3을 참조하여, 상기 제1 마이크로렌즈들(50,51,52) 사이의 갭(D1)으로 빛이 입사되는 것을 방지하기 위하여 상기 제1 마이크로렌즈(50,51,52)가 형성된 픽셀 어레이 기판(10) 상으로 보조 집광부(61)를 형성한다.

<44> 상기 보조 집광부(61)는 상기 제1 마이크로렌즈(50,51,52)를 포함하는 상기 픽셀 어레이 기판(10) 상부로 산화막(SiO2)(60)을 증착하여 형성한다.

<45> 이는 상기 제1 마이크로렌즈(50,51,52)의 굴절률은 약 1.7 정도이고 상기 산화막(60)의 굴절률은 약 1.4 정도이기 때문에, 굴절률이 약 1인 공기를 통해 입사되는 광은 상기 산화막(60)를 통해 1차로 굴절되어 제1 마이크로렌즈(50,51,52)로 입사되기 때문에 포토다이오드로의 집광율을 향상시킬 수 있는 것이다.

<46> 도 4를 참조하여, 상기 산화막(60) 상부로 포토레지스트막을 도포하고 패터닝하여 마스크 패턴(71)을 형성한다. 상기 마스크 패턴(71)은 상기 제1 마이크로렌즈(50,51,52)의 갭(D1) 영역에 대응하는 부분의 상기 보조 집광부(61) 상면이 노출되도록 상기 산화막(60) 상에 형성된다.

<47> 도 5를 참조하여, 상기 마스크 패턴(71)을 식각마스크로 하여 상기 보조 집광부(61)를 식각하면 상기 제1 마이크로렌즈(50,51,52)의 갭 영역에 대응되는 너비를 갖는 트렌치(62)가 형성된다. 예를 들어, 상기 트렌치(62)는 건식식각방법에 의해 식각되고, 주입가스를 조절하여 상기 트렌치(62)의 바닥면이 오목한 형태를 가지도록 형성

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할 수 있다.

<48> 상기와 같이 보조 집광부(61)의 트렌치(62) 바닥면이 오목한 형태로 형성되어 상기 보조 집광부(61)의 트렌치(62)로 광이 입사되면 상기 트렌치(62)의 바닥면의 오목한 형태에 의해 입사광은 셀(D1) 영역으로 사입사 되지 않고 제1 마이크로렌즈(50,51,52)로 집광될 수 있게 된다.

<49> 도 6을 참조하여, 상기 마스크 패턴(71)을 제거하고 상기 트렌치(62)가 형성된 보조 집광부(61) 상부에 제1 마이크로렌즈(50)와 동일한 마이크로 렌즈 형성용 포토레지스트을 도포한 후 상기 보조 집광부(61)의 표면이 노출되도록 평탄화 시킨다.

<50> 그러면 상기 보조 집광부(61)의 트렌치(62) 내부에는 제2 마이크로렌즈(81)가 형성된다.

<51> 상기 제2 마이크로렌즈(81)의 바닥면은 상기 트렌치(62)의 바닥면 형태에 의하여 제1 마이크로렌즈(50)에 대하여 오목한 형태를 가지도록 형성된다.

<52> 따라서, 도 6에 도시된 바와 같이 상기 보조 집광부(61)의 상측에 상기 셀 영역에 대응되는 위치에 오목한 형태의 제2 마이크로 렌즈(81)가 형성되어 있으므로, 물체로부터 입사되는 광이 상기 제1 마이크로렌즈(50,51,52)의 셀(D1) 영역으로 입사될 경우 상기 광은 상기 제2 마이크로렌즈(81)에 의해 직진 방향에 대하여 바깥쪽 영역으로 1차 굴절되고 그 하부의 보조 집광부(61)에 의해 2차 굴절된 후 제1 마이크로렌즈(50)의 이웃하는 제1 마이크로렌즈(51,52)로 입사되어 포토다이오드로의 광 효율을 증가시킬 수 있다.

<53> 또한, 입사광이 셀 영역으로 입사되는 것이 방지되어 크로스 토크 및 노이즈 발생을 방지하여 광감도를 향상시킬 수 있다.

<54> 또한, 상기 제1 마이크로렌즈의 상부에 산화막으로 이루어진 보조 집광부에 의해 후속의 패키지 또는 범프 공정에서의 충격 또는 파티클 등으로부터 발생할 수 있는 이미지 결함을 방지할 수 있다.

<55> <제2 실시예>

<56> 도 11은 제2 실시예에 따른 이미지 센서를 도시하고 있다.

<57> 제2 실시예의 이미지 센서는 픽셀 어레이 기판(100) 상에 형성된 컬러필터 어레이(130); 상기 컬러필터 어레이(130) 상에 형성된 평탄화층(141); 상기 평탄화층(141) 상에 형성된 마이크로렌즈(150,151,152)를 포함하며, 상기 평탄화층(140)에는 상기 마이크로렌즈(150,151,152)의 셀(D2) 영역에 위치되도록 반사막(181)이 형성된 것을 포함한다.

<58> 또한, 상기 평탄화층(140)은 산화막(SiO_2)이고 상기 반사막(181)은 금속물질로 형성될 수 있다.

<59> 상기와 같이 마이크로렌즈의 셀 영역에 의해 노출되는 평탄화층의 표면에 반사막이 형성되어, 물체로부터 입사되는 빛이 상기 마이크로렌즈의 셀영역으로 직진할 경우 상기 반사막에 의해 외부로 다시 반사된다.

<60> 따라서, 상기 마이크로렌즈의 셀영역으로 빛이 입사되는 것을 사전에 차단하므로써 크로스토크 및 노이즈 발생을 방지하여 이미지 센서의 품질을 향상시킬 수 있다.

<61> 이하, 도 7 내지 도 11을 참조하여 제2 실시예에 따른 이미지 센서의 제조공정을 설명한다.

<62> 도 7을 참조하여, 픽셀 어레이 기판(100) 상으로 단위화소(110)에 대응하는 영역에 컬러필터 어레이(130)를 형성한다.

<63> 상기 픽셀 어레이 기판(100)은 컬러필터 어레이(130)를 통해 입사된 빛을 감지하는 포토다이오드(미도시) 및 상기 포토다이오드에서 발생된 전하를 처리하는 트랜지스터들(미도시)로 구성된 단위화소(110)를 포함한다.

<64> 또한 상기 픽셀 어레이 기판(100)은 단위화소(110)로 신호를 전달하는 금속배선(미도시) 및 절연막(미도시)으로 이루어지는 금속배선층(120) 및 패시베이션막(미도시)을 포함할 수 있다.

<65> 그리고, 상기 픽셀 어레이 기판(100) 상에 상기 컬러필터 어레이(130)를 형성한다.

<66> 상기 컬러필터 어레이(130)는 감광물질 및 안료 또는 감광물질 및 염료를 포함하는 컬러필터층(미도시)을 스핀 코팅 공정등을 통해 픽셀 어레이 기판(100) 상에 형성한다. 이어서, 상기 컬러필터층을 패턴 마스크에 의하여 노광한 후 현상하여 상기 픽셀 어레이 기판(100) 상에 컬러필터를 형성한다.

<67> 상기 컬러필터 어레이(130)는 각각의 단위화소(110) 마다 하나의 컬러필터가 형성되어 입사하는 빛으로부터 색

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을 분리해 낸다. 예를 들어, 상기 컬러필터 어레이(130)의 제1 컬러필터는 레드(Red)이고, 제2 컬러필터는 그린(Green)이며, 제3 컬러필터는 블루(Blue)의 3가지 색으로 이루어지며, 인접한 컬러필터들은 서로 약간씩 오버랩되어 단차가 형성된다.

<68> 상기 컬러필터 어레이(30)의 단차를 보완하기 위하여, 상기 컬러필터 어레이 상부로 평탄화층(140)을 형성한다. 예를 들어, 상기 평탄화층(140)은 산화막(SiO_2)을 6000~60000Å의 두께로 형성할 수 있다.

<69> 도 8을 참조하여 상기 평탄화층(140) 상부에 포토레지스트막을 도포하고 패터닝하여 마스크 패턴(170)을 형성한다. 상기 마스크 패턴(170)은 이후 형성되는 마이크로렌즈(150,151,152)의 갭(D2) 영역에 대응하는 상기 평탄화층(61) 상면이 노출되도록 형성된다.

<70> 상기 마스크 패턴(170)을 식각 마스크로 하여 상기 평탄화층(140)을 식각하면 트렌치(142)가 형성된다. 예를 들어, 상기 트렌치(142)의 너비는 약 0.1~0.3㎛ 정도로 형성하고, 상기 트렌치(142) 형성시 상기 평탄화층(141)의 하부에 형성된 상기 컬러필터 어레이(130)를 보호하기 위하여 상기 평탄화층(141)이 완전히 식각되지 않도록 한다.

<71> 도 9 및 도 10을 참조하여, 상기 트렌치(142)가 형성된 평탄화층(141)의 상부로 광속물질을 증착한 다음 평탄화 공정을 진행하여 상기 트렌치(142) 내부에 반사막(181)을 형성한다. 예를 들어, 상기 반사막(181)은 CVD 또는 PVD 방법에 의해 Ti, Al, W 등을 증착하여 반사막층(180)을 형성한 후, CMP 공정에 의해 상기 평탄화층(140)의 표면을 평탄화시켜서 상기 트렌치(142)의 내부에 반사막(181)을 형성할 수 있다.

<72> 도 11 을 참조하여 상기 평탄화층(140) 상부로 포토다이오드로의 집광을 위한 마이크로렌즈(150,151,152)를 형성한다.

<73> 상기 마이크로렌즈(150,151,152)는 상기 평탄화층(140) 상부로 마이크로 렌즈 형성용 포토레지스트를 스핀 공정 등을 통해 도포한다. 그리고, 상기 포토레지스트막(미도시)을 선택적으로 노광 및 현상한 후 각각의 컬러필터 상부에 및 포토레지스트 패턴(미도시)을 형성한다. 이후, 리플로우 공정을 실시하여 볼록한 형상을 갖는 돔 형태의 마이크로렌즈(150,151,152)를 형성한다.

<74> 이때, 상기 마이크로렌즈(150)는 이웃하는 마이크로렌즈(151,152)와의 사이에 갭(gap)(D2)이 발생될 수 있으며, 상기 마이크로렌즈(150,151,152) 사이에 형성된 갭(D2)에 의하여 상기 평탄화층(140)에 형성된 반사막(181)이 노출된 상태가 된다.

<75> 따라서, 도 11에 도시된 바와 같이 상기 마이크로렌즈(150,151,152)들의 갭(D2) 사이에는 반사막(181)이 형성되어 있으므로, 만일 물체로부터 입사되는 광이 상기 마이크로렌즈(150)를 벗어나 상기 마이크로렌즈(150)의 갭(D2) 사이로 전진하게 되면 상기 반사막(181)으로 도달하게 되고 상기 광은 반사막(181)에 의해 다시 외부로 다시 반사되게 되므로, 마이크로렌즈(150,151,152)를 경유하지 않은 광은 포토다이오드로 입사되지 않게 되어 포토다이오드의 광감도를 향상시킬 수 있다.

<76> 또한, 상기 마이크로렌즈(150)의 갭(D2) 사이로 집광되지 않은 빛이 입사되는 것을 반사막(181)에 의하여 차단시킬 수 있으므로, 픽셀 어레이 기판(100)에 배치된 포토 다이오드의 노이즈 및 크로스 토크의 사전에 발생을 차단하여 이미지 센서의 품질을 향상시킬 수 있다.

<77> 이상에서 설명한 본 실시예는 전술한 실시예 및 도면에 의해 한정되는 것이 아니고, 본 실시예의 기술적 사상을 벗어나지 않는 범위 내에서 여러가지 치환, 변형 및 변경할 수 있다는 것은 본 발명이 속하는 기술 분야에서 통상의 지식을 가진 자에게 있어 명백할 것이다.

발명의 효과

<78> 이상에서 설명한 바와 같이 제1 실시예에 따른 이미지 센서 및 그의 제조방법에 의하면 입사광의 굴절율을 높여서 마이크로렌즈의 집광율을 향상시키므로써 이미지센서의 센서티비티를 향상시킬 수 있는 효과가 있다.

<79> 또한, 제1 실시예에 의하면 마이크로렌즈의 상부에 형성된 보조집광부에 의해 후속의 패키지 또는 범프 공정에서의 충격 또는 파티클 등으로부터 발생할 수 있는 이미지 결함을 방지할 수 있는 효과가 있다.

<80> 제2 실시예에 따른 이미지 센서 및 그의 제조방법에 의하면, 마이크로렌즈의 갭 영역에 반사막이 형성되어 갭 영역으로 입사되는 빛을 반사시키므로써 픽셀 간의 크로스토크 및 노이즈 발생을 사전에 차단하여 이미지 센서의 신뢰성을 향상시킬 수 있다.

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도면의 간단한 설명

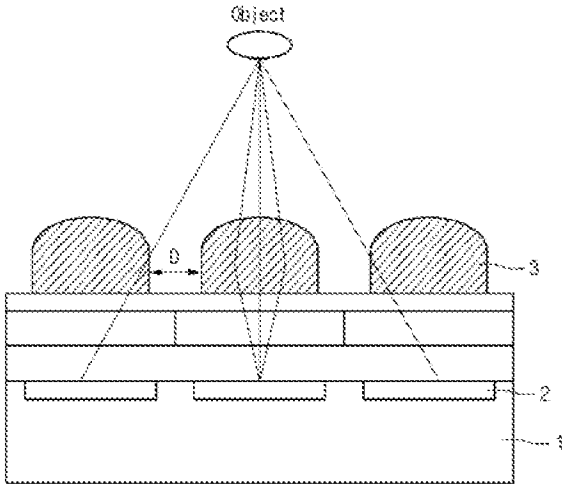
<1> 도 1 은 종래의 이미지 센서를 도시한 도면이다.

<2> 도 2 내지 도 6은 제1 실시예에 따른 이미지 센서의 제조 공정을 나타내는 도면이다.

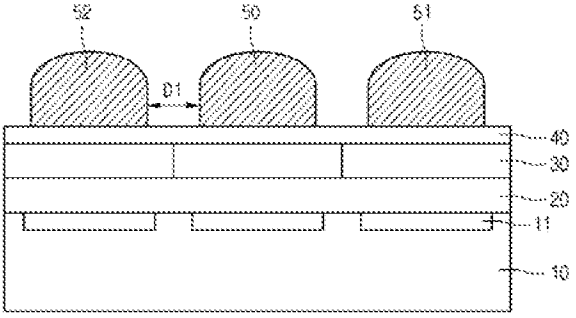
<3> 도 7 내지 도 11는 제2 실시예에 따른 이미지 센서의 제조 공정을 나타내는 도면이다.

도면

도면1

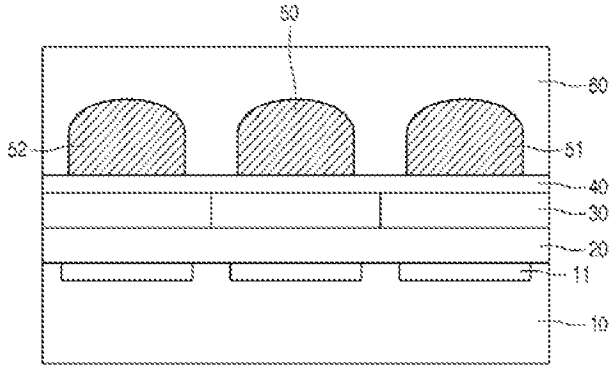


도면2

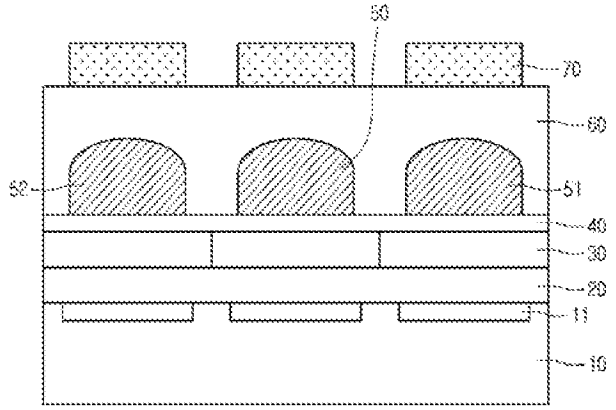


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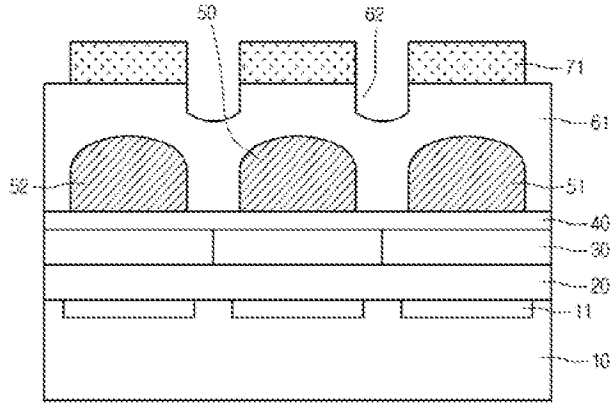
도면3



도면4

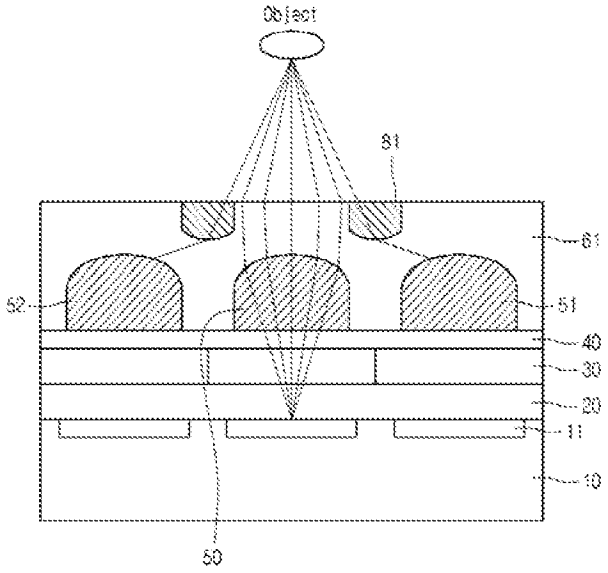


도면5

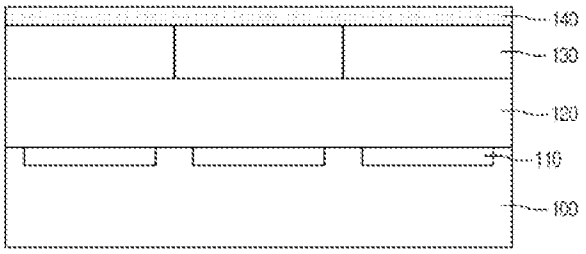


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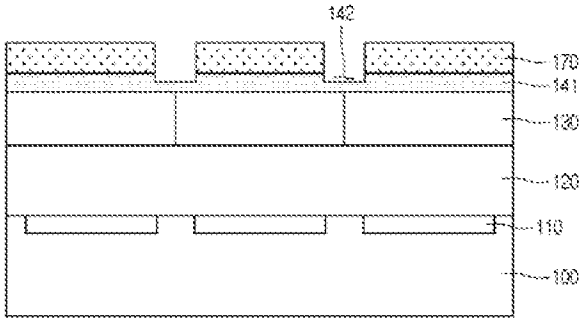
도면6



도면7



도면8



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Espacenet

Bibliographic data: KR20110079323 (A) — 2011-07-07

IMAGE SENSOR AND METHOD FOR MANUFACTURING THE SAME

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Classification: - **international:*H01L27/146***
- **cooperative:** **H01L27/14625**; **H01L27/1463**; **H01L27/14689**
more

Application number: KR20090136341 20091231 Global Dossier

Priority number(s): KR20090136341 20091231

Abstract of KR20110079323 (A)

PURPOSE: An image sensor and a manufacturing method thereof are provided to improve electric cross talk and an optical cross talk. CONSTITUTION: An image sensor includes the first element isolation film(120), a unit pixel, an interlayer insulating layer(150), a trench and the second element isolation film(170). The first element isolation film is formed in the front of a semiconductor substrate so that a pixel region is defined. The unit pixel includes a light sensing part and a readout circuit formed in a pixel region. The interlayer insulating layer includes a wiring formed on the front side of the semiconductor substrate. The trench is formed in a backside of the semiconductor substrate in correspondence to the element isolation film. The second element isolation film is formed in the trench.

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DESCRIPTION KR20110079323

[0001] IMAGE SENSOR AND METHOD FOR MANUFACTURING THE SAME [0002]

Embodiments relate to an image sensor and a method of manufacturing the same. An image sensor is a semiconductor device that converts an optical image into an electrical signal and is classified into a charge coupled device (CCD) image sensor and a CMOS image sensor (CIS) .

Generally, an image sensor forms a photodiode on a silicon substrate by ion implantation. As the size of the photodiode gradually decreases for the purpose of increasing the number of pixels without increasing the chip size, the image quality is reduced due to reduction of the area of the light receiving portion. In addition, since the stack height is not reduced as much as the area of the light receiving portion is reduced, the number of photons incident on the light receiving portion due to the diffraction phenomenon of light called an airy disk also tends to decrease. One of the alternatives to overcome this is to try to minimize the level difference of the light receiving part by receiving light through the wafer backside and to prevent the interference of light by metal routing Sensor) is performed. There is a problem in that the backside light receiving image sensor is not susceptible to optical crosstalk because there is no element isolation region on the back surface of the substrate.

Embodiments provide an image sensor capable of preventing crosstalk and a method of manufacturing the same. An image sensor according to an embodiment includes: a first isolation layer formed on a front surface side of a semiconductor substrate so that a

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pixel region is defined; A unit pixel including a light sensing part and a lead - out circuit formed in the pixel area; An interlayer insulating layer including a wiring formed on a front side of the semiconductor substrate; A trench formed on a back side of the semiconductor substrate opposite to a front surface of the semiconductor substrate and formed on a rear surface of the semiconductor substrate so as to correspond to the first element isolation film; And a second isolation layer formed in the trench. A method of manufacturing an image sensor according to an embodiment includes forming a first device isolation film on a front side of a semiconductor substrate so that a pixel region is defined; Forming a unit pixel including a light sensing part and a lead - out circuit in the pixel area; A step of forming an interlayer insulating layer including wiring on a front side of the semiconductor substrate; Forming a trench on the back side of the semiconductor substrate opposite to the front surface of the semiconductor substrate so as to correspond to the first device isolation film; And forming a second isolation film in the trench. The image sensor and the manufacturing method thereof according to the embodiment can simultaneously improve the electrical crosstalk and the optical crosstalk in the rear light receiving image sensor. That is, a first element isolation region may be formed on the front side of the semiconductor substrate, and a second element isolation region may be formed on the rear side of the semiconductor substrate. Particularly, since the electron generating region of the semiconductor substrate can be formed by the second element isolation region, the optical crosstalk can be fundamentally prevented. In addition, the second isolation regions are formed in a dual structure having different refractive indexes, and the light sensitivity of the unit pixel can be improved since the path of the incident light can be changed.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS Hereinafter, a rear light receiving image sensor according to an embodiment and a method of manufacturing the same will be described in detail with reference to the accompanying drawings. In the description of the embodiment, in the case of being described as being formed on & quot; on / under & quot; of each layer, it is to be understood that the top / bottom may be formed directly, All included. 7, 8 and 9 are sectional views of the image sensor according to the embodiment. An image sensor according to an embodiment includes: a first isolation layer 120 formed on a front side of a semiconductor substrate such that a pixel region is defined; A unit pixel including a light sensing unit 130 and a lead - out circuit 140 formed in the pixel region; An interlayer insulating layer 150 including wirings M1 and M2 formed on a front side of the semiconductor substrate 100; The semiconductor device according to the present invention includes a semiconductor substrate 100 and a semiconductor substrate 100. The semiconductor substrate 100 is formed on the back side of the semiconductor substrate 100 opposite to the front surface of the semiconductor substrate 100, (160); And a second isolation layer 170 formed on the trench 160. The color filter 200 or the microlens 210 may be disposed on

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the rear surface of the semiconductor substrate 100 corresponding to the unit pixel. The second isolation layer 170 may be formed of an insulating material or a metal material. The rear surface of the semiconductor substrate 100 can be separated by unit pixels by the second isolation layer 170. Thus, crosstalk can be prevented by adjusting the photocharge generating region in the semiconductor substrate 100. [8, the second isolation layer 170 includes a first insulation layer 180 formed on the surface of the trench 160 and a second insulation layer 180 formed on the first insulation layer 180 And a second insulating layer 190 formed on the second insulating layer 190. [For example, the first insulating layer 180 may have a first refractive index, and the second insulating layer 190 may have a second refractive index that is greater than the first refractive index.

For example, the refractive index of the first insulating layer 180 may be 1.0 to 1.46, and the refractive index of the second insulating layer 190 may be 1.68 to 3.0. Since the outer side and the inner side of the second isolation film 170 are formed to have different refractive indexes, light incident on a neighboring pixel with an inclination angle can be incident on the corresponding pixel by the second isolation film 170 have. Accordingly, it is possible to prevent the light sensing rate and the crosstalk of the light sensing unit corresponding to the unit pixel. Referring to FIG. 9, the second conductive type layer 300 may be formed on the rear surface of the semiconductor substrate 100. For example, a p + layer can be formed, but is not limited thereto. The second conductive type layer may neutralize the charge trap at the interface of the back side surface of the semiconductor substrate. At this time, the second isolation layer 170 may be formed on the second conductive type layer 300 and the rear surface of the semiconductor substrate 100. The second conductive type layer 300 and the second isolation layer 170 may be formed on the semiconductor substrate 100 to improve full well characteristics. The image sensor according to the embodiment can prevent electrical crosstalk by the first device isolation film formed on the front surface of the semiconductor substrate and effectively prevent optical crosstalk by the second device isolation film formed on the rear surface of the semiconductor substrate. Hereinafter, a method of manufacturing an image sensor according to an embodiment will be described with reference to FIGS. 1 to 9. FIG. First, as shown in FIG. 1, a first device isolation layer 120 is formed on a front side of a semiconductor substrate 100 to define a pixel region. The semiconductor substrate 100 may be a high concentration p - type substrate (p + +). The front side of the semiconductor substrate 100 may include a low concentration p - epi layer 110 by performing an epitaxial process. An ion implantation layer 105 may be formed on the entire surface of the semiconductor substrate 100.

That is, in the embodiment, the lower portion of the semiconductor substrate 100 can be

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easily removed by forming the ion - implanted layer 105 before the wiring process. The ion implantation layer 105 may be formed by implanting ions such as hydrogen (H) or helium (He), but is not limited thereto. The back surface of the semiconductor substrate 100 may be easily removed by using the ion implantation layer 105 instead of removing the back surface of the semiconductor substrate 100 by backgrinding, And can be stably removed. Thus, the production yield of the rear light receiving image sensor can be remarkably increased. The first isolation layer 120 may be formed on the front side of the epi layer 110 of the semiconductor substrate 100 by an STI process. Although not shown, an ion implantation region may be further formed to isolate the light sensing unit 130. This ion implantation region can be formed before or after the first isolation film 120 is formed. Next, a unit pixel including a light sensing part 130 and a lead - out circuit 140 is formed in a pixel region of the semiconductor substrate 100. The light sensing unit 130 may be a photodiode. The light sensing unit 130 may be formed on the semiconductor substrate 100 by a pn junction formed by an n - type ion implantation region and a p - type ion implantation region, but the present invention is not limited thereto. Surplus electrons and the like can be prevented by the p - type ion implantation region. In addition, embodiments can achieve a charge dumping effect by forming PNP junctions. A lead - out circuit 140 for signal processing is formed on the semiconductor substrate 100 on which the light sensing part 130 is formed. For example, the lead - out circuit 140 may include, but is not limited to, a transfer transistor, a reset transistor, a drive transistor, and a select transistor. Next, an interlayer insulating layer 150 and a wiring are formed on the front side of the semiconductor substrate 100. For example, the wiring may include a first metal M1 and a second metal M2.

On the other hand, a carrier wafer (not shown) can be bonded onto the interlayer insulating layer 150 including the wiring. The carrier wafer may be a means for handling the semiconductor substrate 100. Referring to FIG. 2, a part of the back side opposite to the front side of the semiconductor substrate 100 is removed. For example, the lower side of the ion implantation layer 105 of the semiconductor substrate 100 is removed. That is, the heat treatment is performed on the ion - implanted layer 105 to blob the hydrogen ions, and the hydrogen ions are cut with a blade or the like to remove the hydrogen ions, and the upper side of the semiconductor substrate 100 is left as a linar layer . Thereafter, the planarization process may be performed on the rear surface of the cut semiconductor substrate 100. Alternatively, the opposite side of the front side of the semiconductor substrate 100 may be removed by a back graining process. Accordingly, a p - layer (p ++) having a high concentration, which is the back side of the semiconductor substrate 100, can be exposed. Alternatively, the second conductive type layer (p +) 300 may be formed on the rear surface of the semiconductor substrate 100 as shown in FIG. The second conductive type layer 300 may neutralize the charge trap at the interface of the back surface of the semiconductor substrate 100. Next, a

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photoresist pattern 10 is formed on the rear surface of the semiconductor substrate 100. The photoresist pattern 10 may be patterned to correspond to the unit pixel. At this time, the opening 15 of the photoresist pattern 10 may selectively expose the rear surface of the semiconductor substrate 100 corresponding to the position of the first isolation layer 120. Referring to FIG. 3, a trench 160 is formed on the rear surface of the semiconductor substrate 100. The trench 160 may be formed on the backside of the semiconductor substrate 100 to correspond to the first isolation layer 120. The trench 160 may be formed through an etching process using the photoresist pattern as an etching mask.

The trench 160 may be formed by etching a p ++ region of a high concentration of the semiconductor substrate 100 and the p - type epitaxial layer 110 to a predetermined depth. Referring to FIG. 4, a second isolation layer 170 is formed in the trench 160. The rear surface of the semiconductor substrate 100 may be divided into unit pixels by the second isolation layer 170. The second isolation layer 170 may be formed by applying a metal or an insulating material to the trench 160. For example, the second isolation layer 170 may be formed of a metal such as tungsten, aluminum, or titanium. In particular, the second isolation layer 170 may be formed of a metal to prevent incident light from being incident on a photo - sensing portion of an adjacent pixel other than the corresponding pixel. For example, the second isolation layer 170 may be formed of the same oxide or nitride as the first trench 160. As shown in FIGS. 5 and 6, the second isolation layer 170 may have a different refractive index n in the trench 160. Referring to FIG. 5, a first insulating layer 180 is formed along the surface of the trench 160. The first insulating layer 180 may be formed of a material having a first refractive index. For example, the first refractive index may be 1.0 to 1.46. Referring to FIG. 6, a second insulating layer 190 is formed on the first insulating layer 180 so that the trench 160 is formed. The second insulating layer 190 may be formed of a material having a second refractive index greater than the first refractive index. For example, the second refractive index may be 1.68 to 3.0. For example, the first insulating layer 180 may be SiO 2 (n = 1.46) and the second insulating layer 190 may be SiN (n = 2.05), but the present invention is not limited thereto. The second isolation layer 170 may be formed by filling the outer surface of the trench 160 with a material having a small index of refraction and filling the inner portion of the trench with a material having a large index of refraction.

Since the second isolation layer 170 has a double layer structure having different refractive indexes, the incident light having a tilt angle is refracted by the second isolation layer 170 to the corresponding pixel, . That is, the second isolation film may be one in which the total reflection principle is applied. Accordingly, the incident light can be refracted by the second isolation layer 170 to the light sensing unit 130 of the

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corresponding pixel, and the light receiving rate of the unit pixel can be improved. Referring to FIG. 7, a color filter 200 is formed on the rear surface of the semiconductor substrate 100. The color filter 200 is formed for each unit pixel using a dyed photoresist, and can separate colors from incident light. For example, the color filter 200 may be a red, a green, and a blue color filter. Thereafter, a microlens 210 is formed on the color filter 200. The microlens 210 is formed in the shape of a convex lens, and can condense light into the photo - sensing unit of the corresponding unit pixel. A first isolation layer 120 is formed on a front side of the semiconductor substrate 100 and a second isolation layer 170 is formed on a back side of the semiconductor substrate 100, Crosstalk of the light incident on the rear surface of the substrate 100 can be prevented. Particularly, in the rear light receiving image sensor, since the incidence of light is made through the rear surface of the substrate and the red, green, and blue regions are formed from the substrate surface, the crosstalk against the blue signal located at the bottom of the light sensing portion is prevented Can be. Accordingly, the photosensitivity of the image sensor can be uniform. 8 is a cross - sectional view showing a color filter 200 and a microlens 210 formed on the rear surface of the semiconductor substrate 100 including the second isolation layer 170 having a double sidewall structure. 9 is a cross - sectional view illustrating a second device isolation layer 170 having a double sidewall structure selectively formed on the second conductive type layer 300 and the semiconductor substrate 100.

The light passing through the microlens 210 and the color filter 200 may be incident on the corresponding light sensing unit. At this time, light incident at an inclination angle is refracted by the second isolation layer 170 and may be incident on the light sensing unit 130 of the corresponding pixel. Thus, the light sensitivity of the image sensor can be improved. The present invention is not limited to the described embodiments and drawings, and various other embodiments are possible within the scope of the claims.

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CLAIMS KR20110079323

1.
A first device isolation layer formed on a front surface side of the semiconductor substrate so as to define a pixel region; A unit pixel including a light sensing part and a lead - out circuit formed in the pixel area; An interlayer insulating layer including a wiring formed on a front side of the semiconductor substrate; A trench formed on a back side of the semiconductor substrate opposite to a front surface of the semiconductor substrate and formed on a rear surface of the semiconductor substrate so as to correspond to the first element isolation film; And a second isolation layer formed in the trench.

2.
The image sensor according to claim 1, wherein the second isolation film is formed of an insulating material or a metal material.

3.
The semiconductor device according to claim 1, wherein the second isolation layer comprises: a first insulation layer formed on a surface of the trench and having a first refractive index; And a second insulating layer formed on the first layer so that the trench is taped, and having a second refractive index larger than the first refractive index.

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4.
The image sensor of claim 1, further comprising a second conductive type layer formed on a rear surface of the semiconductor substrate, wherein the second conductive type layer and the second conductive type layer are formed on a rear surface of the semiconductor substrate.

5.
The image sensor according to claim 1, comprising a color filter or a microlens formed on the rear surface of the semiconductor substrate corresponding to the unit pixel.

6.
Forming a first device isolation film on a front side of a semiconductor substrate so that a pixel region is defined; Forming a unit pixel including a light sensing part and a lead - out circuit in the pixel area; A step of forming an interlayer insulating layer including wiring on a front side of the semiconductor substrate; Forming a trench on the back side of the semiconductor substrate opposite to the front surface of the semiconductor substrate so as to correspond to the first device isolation film; And forming a second isolation film in the trench.

7.
7. The method of claim 6, wherein the second isolation layer is formed by applying an insulating material to the trench.

8.
7. The method of claim 6, wherein the second isolation layer is formed by applying a metal material to the trench.

9.
The method according to claim 6, wherein the forming of the second isolation layer comprises: forming a first insulation layer having a first refractive index on a surface of the trench; And forming a second insulating layer having a second refractive index larger than the first refractive index on the first insulating layer so that the trench is formed on the first insulating layer.

10.

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The method of claim 6, further comprising forming a second conductive type layer on a rear surface of the semiconductor substrate, and then forming the second element isolation film.

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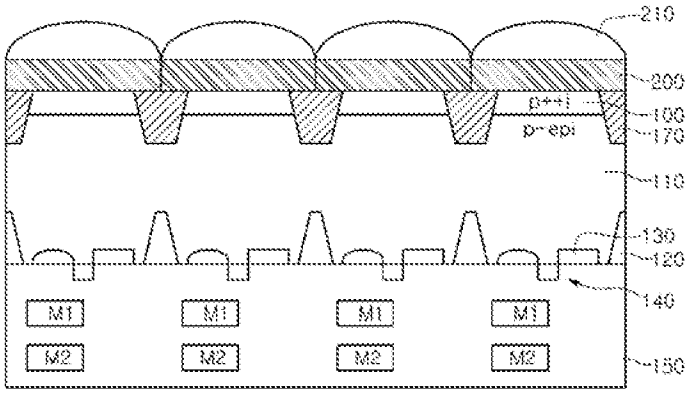
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(54) 이미지 센서 및 그 제조방법

(57) 요 약

실시예에 따른 이미지 센서는, 픽셀영역이 정의되도록 반도체 기판의 전면측에 형성된 제1 소자분리막; 상기 픽셀영역에 형성된 광감지부 및 리드아웃 서킷을 포함하는 단위픽셀; 상기 반도체 기판의 전면(front side) 상에 형성된 배선을 포함하는 층간절연층; 상기 반도체 기판의 전면과 반대되는 상기 반도체 기판의 후면(back side)에 형성되고, 상기 제1 소자분리막과 대응되도록 상기 반도체 기판의 후면에 형성된 트렌치; 및 상기 트렌치에 형성된 제2 소자분리막을 포함한다.

대 표 도 - 도7



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특허청구의 범위

청구항 1

픽셀영역이 정의되도록 반도체 기판의 전면측에 형성된 제1 소자분리막;

상기 픽셀영역에 형성된 광감지부 및 리드아웃 서킷을 포함하는 단위픽셀;

상기 반도체 기판의 전면(front side) 상에 배선을 포함하는 층간절연층;

상기 반도체 기판의 전면과 반대되는 상기 반도체 기판의 후면(back side)에 형성되고, 상기 제1 소자분리막과 대응되도록 상기 반도체 기판의 후면에 형성된 트렌치; 및

상기 트렌치에 형성된 제2 소자분리막을 포함하는 이미지 센서.

청구항 2

제1항에 있어서,

상기 제2 소자분리막은 절연물질 또는 금속 물질로 형성된 이미지 센서.

청구항 3

제1항에 있어서,

상기 제2 소자분리막은,

상기 트렌치의 표면에 형성되고 제1 굴절률을 가지는 제1 절연층; 및

상기 트렌치가 갭필되도록 상기 제1 층 상에 형성되고, 제1 굴절률보다 큰 제2 굴절률을 가지는 제2 절연층을 포함하는 이미지 센서.

청구항 4

제1항에 있어서,

상기 반도체 기판의 후면 상에 형성된 제2 도전형 층을 더 포함하고,

상기 제2 소자분리막은 상기 제2 도전형 층 및 상기 반도체 기판의 후면에 형성된 것을 포함하는 이미지 센서.

청구항 5

제1항에 있어서,

상기 단위픽셀에 대응하는 상기 반도체 기판의 후면 상에 형성된 컬러필터 또는 마이크로 렌즈를 포함하는 이미지 센서.

청구항 6

픽셀영역이 정의되도록 반도체 기판의 전면측에 제1 소자분리막을 형성하는 단계;

상기 픽셀영역에 광감지부 및 리드아웃 서킷을 포함하는 단위픽셀을 형성하는 단계;

상기 반도체 기판의 전면(front side) 상에 배선을 포함하는 층간절연층을 형성하는 단계;

상기 반도체 기판의 전면과 반대되는 상기 반도체 기판의 후면(back side)에 상기 제1 소자분리막과 대응되도록 트렌치를 형성하는 단계; 및

상기 트렌치에 제2 소자분리막을 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 7

제6항에 있어서,

상기 제2 소자분리막은 상기 트렌치에 절연물질을 갭필하여 형성되는 이미지 센서의 제조방법.

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청구항 8

제6항에 있어서,

상기 제2 소자분리막은 상기 트렌치의 유전물질을 갭필하여 형성되는 이미지 센서의 제조방법.

청구항 9

제6항에 있어서,

상기 제2 소자분리막을 형성하는 단계는,

상기 트렌치의 표면에 제1 유전물을 가지는 제1 절연층을 형성하는 단계; 및

상기 트렌치가 갭필되도록 상기 제1 절연층 상에 제1 유전물보다 큰 제2 유전물을 가지는 제2 절연층을 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 10

제6항에 있어서,

상기 반도체 기판의 후면 상에 제2 도전형 층을 형성한 다음, 상기 제2 소자분리막을 형성하는 단계를 포함하는 이미지 센서의 제조방법.

명 세 서

발명의 상세한 설명

기 술 분 야

[0001] 실시예는 이미지 센서 및 그 제조방법에 관한 것이다.

[0002] 이미지센서(Image sensor)는 광학적 영상(optical image)을 전기적 신호로 변환시키는 반도체소자로서, 전하결합소자(Charge Coupled Device: CCD) 이미지센서와 씨모스 이미지센서(CMOS Image Sensor: CIS)로 구분된다.

배 경 기 술

[0003] 일반적으로 이미지 센서는 실리콘 기판에 포토다이오드(Photodiode)를 이온주입 방식으로 형성시킨다. 칩 사이즈(Chip size) 증가 없이 픽셀(Pixel) 수 증가를 위한 목적으로 포토다이오드의 사이즈가 점점 감소함에 따라 수광부 면적 축소로 이미지 특성(Image Zuality)이 감소하는 경향을 보이고 있다.

[0004] 또한, 수광부 면적 축소만큼의 적층높이(Stack height)의 감소가 이루어지지 못하여 에어리 디스크(Airy disk)라 불리는 빛의 회절 현상으로 수광부에 입사되는 포톤(photon)의 수 역시 감소하는 경향을 보이고 있다.

[0005] 이를 극복하기 위한 대안 중 하나로 웨이퍼 백사이드(Wafer Back Side)를 통해 빛을 받아들여 수광부의 단차를 최소화하고, 메탈 라우팅(Metal routing)에 의한 빛의 간섭을 현상을 방지할 수 있는 시도(후면수광 이미지 센서)가 이루어지고 있다.

[0006] 이러한 후면수광 이미지 센서에서 기판(substrate)의 후면 상에 소자분리 영역이 존재하지 않아 광학적 크로스 토크(Cross talk)에 매우 취약한 문제가 있다.

발명의 내용

해결 하고자하는 과제

[0007] 실시예는 크로스 토크를 방지할 수 있는 이미지센서 및 그 제조방법을 제공한다.

과제 해결수단

[0008] 실시예에 따른 이미지 센서는, 픽셀영역이 정의되도록 반도체 기판의 전면측에 형성된 제1 소자분리막; 상기 픽셀영역에 형성된 광감지부 및 리드아웃 회로를 포함하는 단위픽셀; 상기 반도체 기판의 전면(front side) 상에 형성된 배선을 포함하는 층간절연층; 상기 반도체 기판의 전면과 반대되는 상기 반도체 기판의 후면(back sid

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e)에 형성되고, 상기 제1 소자분리막과 대응되도록 상기 반도체 기판의 후면에 형성된 트렌치; 및 상기 트렌치에 형성된 제2 소자분리막을 포함한다.

[0009] 실시예에 따른 이미지 센서의 제조방법은, 픽셀영역이 정의되도록 반도체 기판의 전면측에 제1 소자분리막을 형성하는 단계; 상기 픽셀영역에 광감지부 및 리드아웃 서킷을 포함하는 단위픽셀을 형성하는 단계; 상기 반도체 기판의 전면(front side) 상에 배선을 포함하는 층간절연층을 형성하는 단계; 상기 반도체 기판의 전면과 반대되는 상기 반도체 기판의 후면(back side)에 상기 제1 소자분리막과 대응되도록 트렌치를 형성하는 단계; 및 상기 트렌치에 제2 소자분리막을 형성하는 단계를 포함한다.

효 과

[0010] 실시예에 따른 이미지 센서 및 그 제조방법은, 후면수광 이미지 센서에서 전기적 크로스 토크 및 광학적 크로스 토크를 동시에 개선할 수 있다.

[0011] 즉, 반도체 기판의 전면측에 제1 소자분리 영역을 형성하고, 상기 반도체 기판의 후면측에 제2 소자분리 영역을 형성할 수 있다.

[0012] 특히, 상기 제2 소자분리 영역에 의하여 반도체 기판의 전자 생성 영역을 설정할 수 있으므로, 근본적으로 광학적 크로스 토크를 방지할 수 있다.

[0013] 또한, 상기 제2 소자분리 영역은 서로 다른 굴절률을 가지는 이중구조로 형성되고, 입사광의 경로를 바꿀수 있으므로 단위픽셀의 광 감도를 향상시킬 수 있다.

발명의 실시를 위한 구체적인 내용

[0014] 이하, 실시예에 따른 후면수광 이미지센서 및 그 제조방법을 첨부된 도면을 참조하여 상세히 설명한다.

[0015] 실시예의 설명에 있어서, 각 층의 "상/아래(on/under)"에 형성되는 것으로 기재되는 경우에 있어, 상/아래는 직접(directly)과 또는 다른 층을 개재하여(indirectly) 형성되는 것을 모두 포함한다.

[0016] 도 7, 도 8 및 도 9는 실시예에 따른 이미지 센서의 단면도이다.

[0017] 실시예에 따른 이미지 센서는, 픽셀영역이 정의되도록 반도체 기판의 전면측에 형성된 제1 소자분리막(120); 상기 픽셀영역에 형성된 광감지부(130) 및 리드아웃 서킷(140)을 포함하는 단위픽셀; 상기 반도체 기판(100)의 전면(front side) 상에 형성된 배선(M1,M2)을 포함하는 층간 절연층(150); 상기 반도체 기판(100)의 전면과 반대되는 상기 반도체 기판(100)의 후면(back side)측에 형성되고, 상기 제1 소자분리막(120)과 대응되도록 상기 반도체 기판(100)의 후면에 형성된 트렌치(160); 및 상기 트렌치(160)에 형성된 제2 소자분리막(170)을 포함한다.

[0018] 상기 단위픽셀에 대응하는 상기 반도체 기판(100)의 후면 상에 컬러필터(200) 또는 마이크로 렌즈(210)가 배치될 수 있다.

[0019] 상기 제2 소자분리막(170)은 절연물질 또는 금속 물질로 형성될 수 있다.

[0020] 상기 제2 소자분리막(170)에 의하여 반도체 기판(100)의 후면을 단위픽셀 별로 분리할 수 있다. 이에 따라, 상기 반도체 기판(100) 내의 광 전하 생성영역을 조절함으로써 크로스 토크를 방지할 수 있다.

[0021] 도 8을 참조하여, 상기 제2 소자분리막(170)은, 상기 트렌치(160)의 표면에 형성된 제1 절연층(180) 및 상기 트렌치(160)가 갭필되도록 상기 제1 절연층(180) 상에 형성된 제2 절연층(190)을 포함한다. 예를 들어, 상기 제1 절연층(180)은 제1 굴절률을 가지고, 상기 제2 절연층(190)은 제1 굴절률보다 큰 제2 굴절률을 가질 수 있다.

[0022] 예를 들어, 상기 제1 절연층(180)의 굴절률은 1.0~1.46일 수 있고, 제2 절연층(190)의 굴절률은 1.68~3.0일 수 있다.

[0023] 상기 제2 소자분리막(170)의 외측 및 내측이 서로 다른 굴절률을 가지도록 형성됨으로써, 경사각을 가지고 이웃하는 픽셀로 입사하는 광이 상기 제2 소자분리막(170)에 의하여 해당하는 픽셀로 입사될 수 있다. 이에 따라, 단위픽셀에 해당하는 광감지부의 광감지율 및 크로스 토크를 방지할 수 있다.

[0024] 도 9를 참조하여, 상기 반도체 기판(100)의 후면 상에 제2 도전형 층(300)이 형성될 수 있다.

[0025] 예를 들어, p+층을 형성할 수 있으나, 이에 한정되는 것은 아니다. 상기 제2 도전형 층은 상기 반도체 기판의 후면(back side) 표면의 인터페이스(interface)에서 전하 트랩(trap)을 중성화시킬 수 있다.

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[0026] 이때, 상기 제2 소자분리막(170)은 상기 제2 도전형 층(300) 및 상기 반도체 기판(100)의 후면에 형성될 수 있다.

[0027] 상기 제2 도전형 층(300) 및 상기 반도체 기판(100)에 제2 소자분리막(170)이 형성되어, 풀웰특성(Full well) 특성을 향상시킬 수 있다.

[0028] 실시예에 따른 이미지 센서는, 반도체 기판의 전면에 형성된 제1 소자분리막에 의하여 전기적 크로스 토크를 방지하고, 상기 반도체 기판의 후면에 형성된 제2 소자분리막에 의하여 광학적 크로스 토크를 효과적으로 방지할 수 있다.

[0029] 이하, 도 1 내지 도 9를 참조하여 실시예에 따른 이미지 센서의 제조방법을 설명한다.

[0030] 우선, 도 1에 도시된 바와 같이 반도체 기판(100)의 전면(Front Side)에 제1 소자분리막(120)을 형성하여 액셀 영역을 정의한다.

[0031] 상기 반도체 기판(100)은 고농도의 p형 기판(p++) 일 수 있다. 상기 반도체 기판(100)의 전면(Front Side)은 에피택셜(epitaxial) 공정을 실시하여 저농도의 p형 에피층(p-epi)(110)을 포함할 수 있다.

[0032] 상기 반도체 기판(100)의 전면에 이온주입층(105)를 형성할 수 있다. 즉, 실시예는 배선공정 전에 미리 이온주입층(105)을 형성함으로써 상기 반도체 기판(100)의 하부를 용이하게 제거할 수 있다. 이러한 이온주입층(105)은 수소(H) 또는 헬륨(He) 등의 이온을 주입하여 형성할 수 있으나, 이에 한정되지 않는다.

[0033] 상기 이온주입층(105)을 형성하는 경우, 백 그라인딩에 의해 상기 반도체 기판(100)의 후면을 제거하는 것이 아니라, 상기 이온주입층(105)을 이용하여 상기 반도체 기판(100)의 후면을 용이하고 안정적으로 제거할 수 있게 된다. 이에 따라, 후면수광 이미지 센서의 제조 수율을 현저히 상승시킬 수 있다.

[0034] 상기 제1 소자분리막(120)은 STI 공정에 의하여 상기 반도체 기판(100)의 에피층(110) 전면(front)측에 형성될 수 있다. 도시되지는 않았지만, 상기 광감지부(130)의 격리를 위해 이온주입영역을 더 형성할 수도 있다. 이러한 이온주입 영역은 제1 소자분리막(120)의 형성 전 또는 후에 형성할 수 있다.

[0035] 다음으로, 상기 반도체 기판(100)의 액셀영역에 광감지부(130) 및 리드아웃 서킷(140)을 포함하는 단위픽셀을 형성한다.

[0036] 상기 광감지부(130)는 포토다이오드일 수 있다.

[0037] 상기 광감지부(130)는 상기 반도체 기판(100)의 n형 이온주입영역 및 p형 이온주입영역의 의한 pn정션에 의하여 형성될 수 있으나, 이에 한정되는 것은 아니다.

[0038] 상기 p형 이온주입 영역에 의해 잉여전자 등을 방지할 수 있다. 또한, 실시예는 PNP 정션을 형성하여 전하덤핑(charge dumping) 효과를 얻을 수 있다.

[0039] 상기 광감지부(130)가 형성된 반도체 기판(100) 상에 신호처리를 위한 리드아웃 서킷(140)을 형성한다.

[0040] 예를 들어, 상기 리드아웃 서킷(140)은 트랜스퍼 트랜지스터, 리셋 트랜지스터, 드라이브 트랜지스터 및 셀렉트 트랜지스터를 포함할 수 있으나 이에 한정되는 것은 아니다.

[0041] 다음으로, 상기 반도체 기판(100)의 전면(Front Side) 상에 층간 절연층(150)과 배선을 형성한다. 예를 들어, 상기 배선은 제1 메탈(M1) 및 제2 메탈(M2) 등을 포함할 수 있다.

[0042] 한편, 상기 배선을 포함하는 층간 절연층(150) 상에 캐리어 웨이퍼(미도시)를 본딩할 수 있다. 이러한 캐리어 웨이퍼는 상기 반도체 기판(100)을 핸들링하기 위한 수단일 수 있다.

[0043] 도 2를 참조하여, 상기 반도체 기판(100) 전면(Front Side)의 반대인 후면(Back Side)의 일부를 제거한다.

[0044] 예를 들어, 상기 반도체 기판(100)의 이온주입층(105)을 기준으로 그 하측을 제거한다.

[0045] 즉, 상기 이온주입층(105)에 대한 열처리를 진행하여 수소이온을 기포화(bubble) 시킨 후 폴리싱 등으로 컷팅하여 제거하고, 상기 반도체 기판(100)의 상측이 타이너 레이어(Tiner layer)로 남아있게 된다. 이후, 컷팅된 상기 반도체 기판(100)의 후면에 대한 평탄화공정이 진행될 수도 있다.

[0046] 또는, 상기 반도체 기판(100)의 전면측(Front Side)의 반대측을 백그라인딩(back grinding) 공정으로 제거할 수도 있다.

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[0047] 이에 따라, 상기 반도체 기판(100)의 후면(Back Side)인 고농도의 p층(p++)이 노출될 수 있다.

[0048] 또는 도 9에 도시된 바와 같이 상기 반도체 기판(100)의 후면 상에 제2 도전형 층(p+)(300) 형성할 수도 있다.

[0049] 상기 제2 도전형 층(300)은 반도체 기판(100) 후면 표면의 인터페이스에서 전하 트랩을 중성화시킬 수 있다.

[0050] 다음으로, 상기 반도체 기판(100)의 후면 상에 포토레지스트 패턴(10)이 형성된다.

[0051] 상기 포토레지스트 패턴(10)은 상기 단위픽셀에 대응하도록 패터닝될 수 있다. 이때, 상기 포토레지스트 패턴(10)의 개구부(15)는 상기 제1 소자분리막(120)의 위치와 대응되는 상기 반도체 기판(100)의 후면을 선택적으로 노출시킬 수 있다.

[0052] 도 3을 참조하여, 상기 반도체 기판(100)의 후면에 트렌치(160)가 형성된다.

[0053] 상기 트렌치(160)는 상기 제1 소자분리막(120)에 대응하도록 상기 반도체 기판(100)의 후면측에 형성될 수 있다.

[0054] 상기 트렌치(160)는 상기 포토레지스트 패턴을 식각마스크로 사용하는 식각공정을 통해 형성될 수 있다.

[0055] 상기 트렌치(160)는 상기 반도체 기판(100)의 고농도 p++영역과 상기 p형 에피층(110)을 소정 깊이로 식각하여 형성할 수 있다.

[0056] 도 4를 참조하여, 상기 트렌치(160)에 제2 소자분리막(170)이 형성된다.

[0057] 상기 제2 소자분리막(170)에 의하여 상기 반도체 기판(100)의 후면은 단위픽셀 별로 분리될 수 있다.

[0058] 상기 제2 소자분리막(170)은 상기 트렌치(160)에 금속물질 또는 절연물질을 갭필하여 형성될 수 있다.

[0059] 예를 들어, 상기 제2 소자분리막(170)은 텅스텐, 알루미늄 및 타이타늄과 같은 금속으로 형성될 수 있다. 특히, 상기 제2 소자분리막(170)이 금속으로 형성되어 입사광은 해당 픽셀이 아닌 인접 픽셀의 광감지부로 입사하는 것을 차단할 수 있다.

[0060] 예를 들어, 상기 제2 소자분리막(170)은 상기 제1 트렌치(160)와 동일한 산화막 또는 질화막으로 형성될 수 있다.

[0061] 도 5 및 도 6에 도시된 바와 같이, 상기 제2 소자분리막(170)은 상기 트렌치(160)의 내부에 서로 다른 굴절률(n)을 가지도록 형성할 수도 있다.

[0062] 도 5를 참조하여, 상기 트렌치(160)의 표면을 따라 제1 절연층(180)이 형성된다.

[0063] 상기 제1 절연층(180)은 제1 굴절률을 가지는 물질로 형성될 수 있다. 예를 들어, 상기 제1 굴절률은 1.0~1.46일 수 있다.

[0064] 도 6을 참조하여, 상기 트렌치(160)가 갭필되도록 상기 제1 절연층(180) 상에 제2 절연층(190)이 형성된다.

[0065] 상기 제2 절연층(190)은 제1 굴절률 보다 큰 제2 굴절률을 가지는 물질로 형성될 수 있다. 예를 들어, 상기 제2 굴절률은 1.68~3.0일 수 있다.

[0066] 예를 들어, 상기 제1 절연층(180)은 SiO_2(n=1.46)이고 제2 절연층(190)은 SIN(n=2.05)일 수도 있으나, 이에 한정되는 것은 아니다.

[0067] 상기 트렌치(160)의 외측 표면에 작은 굴절률을 가지는 물질을 채우고, 상기 트렌치(160)의 내측에 큰 굴절률을 가지는 물질을 채움으로써 제2 소자분리막(170)을 형성할 수 있다.

[0068] 상기 제2 소자분리막(170)은 서로 다른 굴절률을 가지는 이중층 구조를 가지므로써, 경사각을 가지고 입사되는 빛은 상기 제2 소자분리막(170)에 의하여 해당픽셀로 굴절되고 광감지부(130)로 입사될 수 있다. 즉, 상기 제2 소자분리막은 전반사 법칙이 적용된 것일 수 있다.

[0069] 이에 따라, 상기 제2 소자분리막(170)에 의하여 입사광을 해당하는 픽셀의 광감지부(130)로 굴절시키고, 단위픽셀의 수광율을 향상시킬 수 있다.

[0070] 도 7을 참조하여, 상기 반도체 기판(100)의 후면 상에 컬러필터(200)가 형성된다.

[0071] 상기 컬러필터(200)는 염색된 포토레지스트를 사용하여 각각의 단위픽셀마다 하나씩 형성되고 입사하는 빛으로

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부터 색을 분리할 수 있다.

[0072] 예를 들어, 상기 컬러필터(200)는 레드(Red), 그린(Green) 및 블루(Blue) 컬러필터 일 수 있다.

[0073] 이후, 상기 컬러필터(200) 상에 마이크로 렌즈(210)가 형성된다.

[0074] 상기 마이크로 렌즈(210)는 볼록렌즈 형태로 형성되고, 해당하는 단위픽셀의 광감지부로 빛을 집광시킬 수 있다.

[0075] 상기 반도체 기판(100)의 전면(front side)측에는 제1 소자분리막(120)이 형성되고, 상기 반도체 기판(100)의 후면(back side)측에는 제2 소자분리막(170)이 형성되어, 상기 반도체 기판(100)의 후면으로 입사되는 광의 크로스 토크를 방지할 수 있다.

[0076] 특히, 후면수광 이미지 센서에서 빛의 입사가 기판의 후면을 통해 이루어지고, 기판 표면으로부터 레드, 그린 및 블루 영역이 형성되기 때문에 광감지부의 가장 아래쪽에 위치한 블루 신호에 대한 크로스 토크를 발생을 방지할 수 있다.

[0077] 이에 따라, 이미지 센서의 광감도가 균일할 수 있다.

[0078] 도 8은 이중측벽 구조를 가지는 제2 소자분리막(170)을 포함하는 상기 반도체 기판(100)의 후면 상에 컬러필터(200) 및 마이크로 렌즈(210)가 형성된 것을 나타내는 단면도이다.

[0079] 도 9는 상기 제2 도전형 층(300) 및 반도체 기판(100)에 선택적으로 이중측벽 구조의 제2 소자분리막(170)이 형성된 것을 나타내는 단면도이다.

[0080] 상기 마이크로 렌즈(210) 및 컬러필터(200)를 통과한 빛은 해당하는 광감지부로 입사될 수 있다. 이때, 경사각을 가지로 입사되는 빛은 상기 제2 소자분리막(170)에 의하여 굴절되고 해당하는 픽셀의 광감지부(130)로 입사될 수 있다. 이에 따라, 이미지 센서의 광 감도를 향상시킬 수 있다.

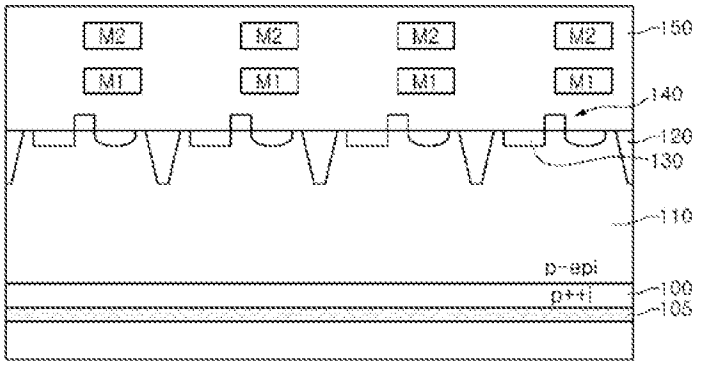
[0081] 본 발명은 기재된 실시예 및 도면에 의해 한정되는 것이 아니고, 청구항의 권리범위에 속하는 범위 안에서 다양한 다른 실시예가 가능하다.

도면의 간단한 설명

[0082] 도 1 내지 도 9는 실시예에 따른 이미지 센서의 제조공정을 나타내는 단면도이다.

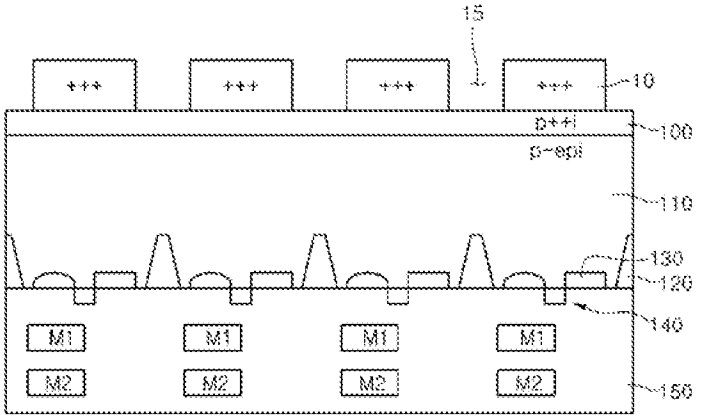
도면

도면1

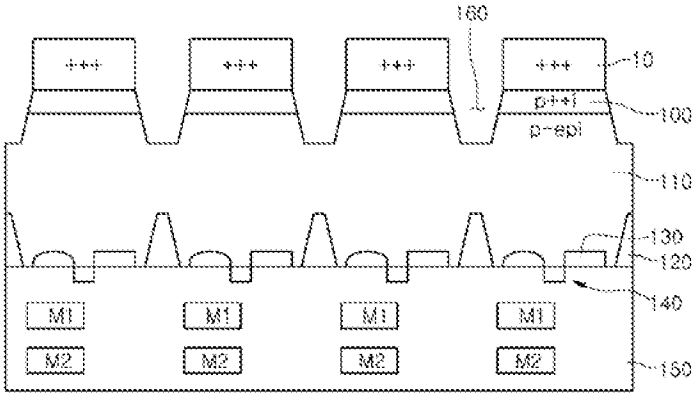


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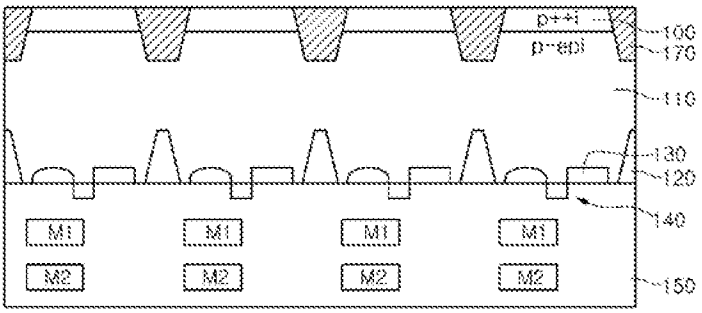
도면2



도면3

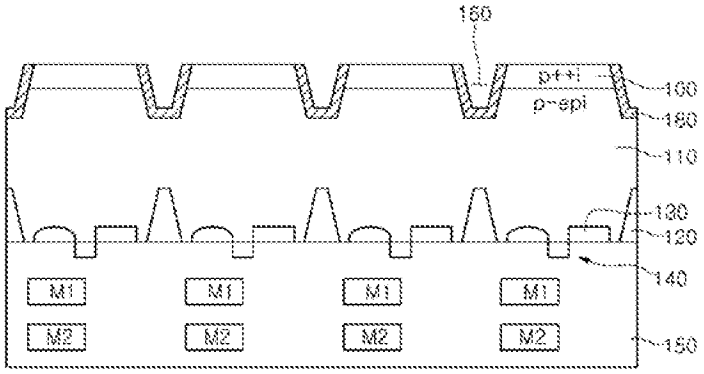


도면4

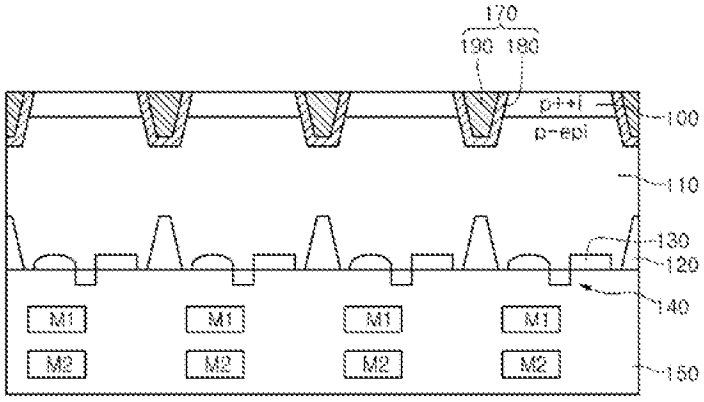


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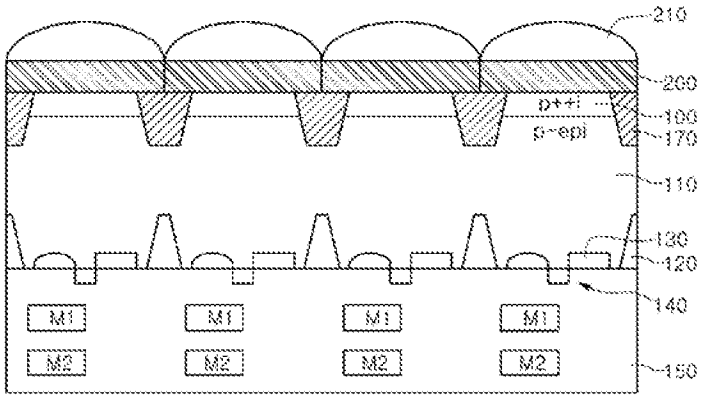
도면5



도면6

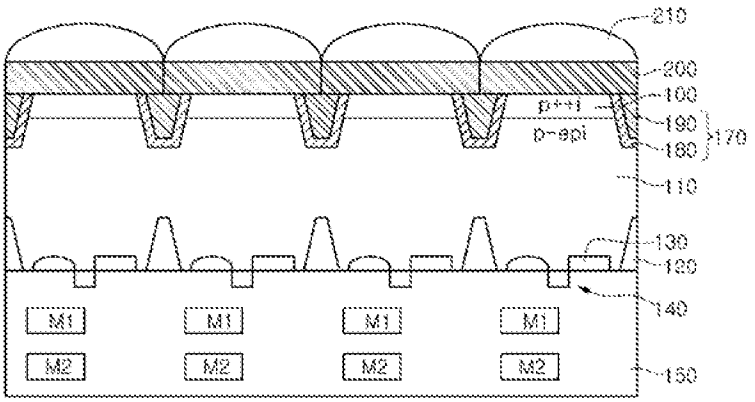


도면7

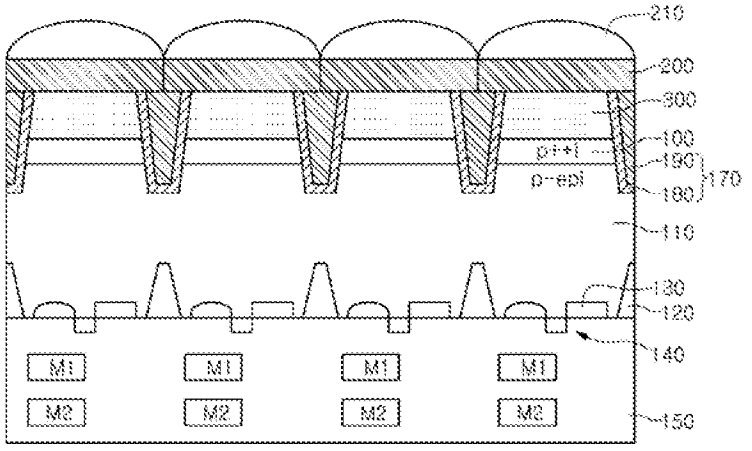


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도면2



도면3



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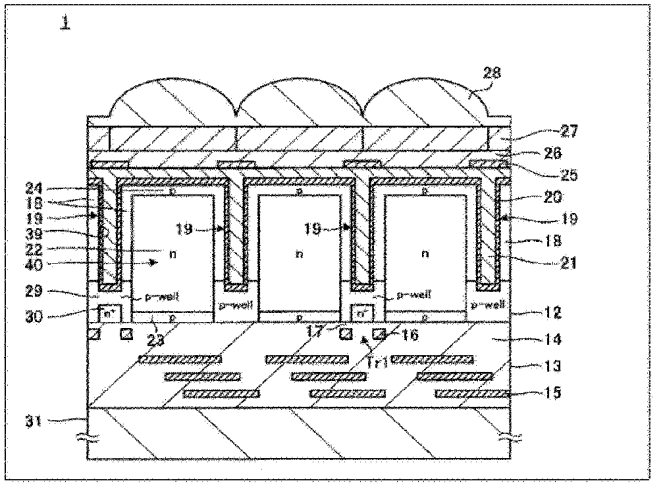
전체 청구항 수 : 총 22 항

(54) 발명의 명칭 **고체 촬상 장치, 고체 촬상 장치의 제조 방법 및 전자 기기**

(57) 요 약

본 기술은, 광학 혼색의 저감 등의 특성을 더욱 향상시킨 고체 촬상 장치를 제공할 수 있는 고체 촬상 장치, 고체 촬상 장치의 제조 방법 및 전자 기기에 관한 것이다. 또한, 그 고체 촬상 장치를 이용한 전자 기기를 제공한다. 기판(12)과, 기판(12)에 형성된 복수의 광전 변환부(40)를 구비한 고체 촬상 장치에서, 절연막(21)이 매입된 소자 분리부(19)를 형성한다. 소자 분리부(19)는, 기판(12)의 광입사측부터 깊이 방향으로 형성된 홈부(30) 내에서, 홈부(30)의 내벽면을 피복하도록 형성된 고정 전하를 갖는 절연막(20)으로 구성되어 있다.

대 표 도 - 도2



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명 세 서

청구범위

청구항 1

반도체 기판과,

상기 반도체 기판의 제1 광전 변환부와,

상기 반도체 기판의 제2 광전 변환부와,

상기 반도체 기판의 제3 광전 변환부와,

상기 제1 광전 변환부와 상기 제2 광전 변환부 사이에 배치된 제1 홈부와,

상기 제1 홈부는 상기 반도체 기판의 깊이 방향으로 연장되고, 고정 전하를 갖는 제1 절연막의 제1 부분을 포함하며,

상기 제2 광전 변환부와 상기 제3 광전 변환부 사이에 배치된 제2 홈부와,

상기 제2 홈부는 상기 반도체 기판의 깊이 방향으로 연장되고, 상기 제1 절연막의 제2 부분을 포함하며,

상기 제1 및 제2 광전 변환부 사이의 제1 절연막 상에 배치되는 제2 절연막과,

상기 제1 홈부의 깊이는 제2 홈부의 깊이보다 깊은 것을 특징으로 하는 고체 촬상 장치.

청구항 2

제1항에 있어서,

상기 제2 절연막은 실리콘 산화물, 실리콘 질화물 또는 실리콘 산 질화물을 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 3

제1항에 있어서,

상기 제1 절연막은, 하프늄(Hf), 알루미늄(Al), 지르코늄(Zr), 탄탈륨(Ta), 티타늄(Ti), 란타넘(La), 프라세오디뮴(Pr), 세륨(Ce), 네오디뮴(Nd), 프로메튬(Pm), 사마륨(Sm), 유로퓸(Eu), 가돌리늄(Gd), 터븀(Tb), 디스프로슘(Dy), 홀뮴(Ho), 툴륨(Tm), 이터븀(Yb), 루테튬(Lu) 또는 이트륨(Y) 중 적어도 어느 하나의 원소를 포함하는 산화물 또는 질화물인 것을 특징으로 하는 고체 촬상 장치.

청구항 4

제1항에 있어서,

상기 제1 절연막은 산화 하프늄을 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 5

제1항에 있어서,

상기 제2 절연막은 산화실리콘을 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 6

제1항에 있어서,

상기 반도체 기판은 광 입사 측인 제1면 및 상기 제1면의 반대측인 제2면을 포함하고, 배선층은 상기 제2면의 반도체 기판에 배치된 것을 특징으로 하는 고체 촬상 장치.

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청구항 7

제6항에 있어서,

상기 반도체 기판의 상기 제1면에 배치된 차광막을 더 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 8

제7항에 있어서,

상기 차광막상에 배치된 평탄화막을 더 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 9

제7항에 있어서,

상기 차광막의 상부에 배치된 컬러 필터를 더 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 10

제9항에 있어서,

상기 컬러 필터상에 배치된 온칩 렌즈를 더 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 11

제6항에 있어서,

상기 제1 홈부는 상기 반도체 기판의 상기 제2 면상에 형성된 p형 영역에 이르는 깊이로 형성되는 것을 특징으로 하는 고체 촬상 장치.

청구항 12

제1항에 있어서,

상기 제1 홈부는 상기 반도체 기판의 표면 측에 형성된 p형 영역에 이르는 깊이로 형성되는 것을 특징으로 하는 고체 촬상 장치.

청구항 13

제1항에 있어서,

플로팅 디퓨전부와,

상기 제1 광전 변환부는 상기 플로팅 디퓨전부에 연결되고, 상기 플로팅 디 퓨전부는 리셋 트랜지스터 및 증폭 트랜지스터에 연결되는 것을 특징으로 하는 고체 촬상 장치.

청구항 14

제13항에 있어서,

상기 플로팅 디퓨전부, 증폭 트랜지스터 및 리셋 트랜지스터는 상기 제1 광전 변환부 및 상기 제2 광전 변환부에 의해 공유되는 것을 특징으로 하는 고체 촬상 장치.

청구항 15

제13항에 있어서,

상기 증폭 트랜지스터에 연결된 선택 트랜지스터를 더 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 16

제15항에 있어서,

상기 선택 트랜지스터에 연결된 신호선을 더 포함하는 것을 특징으로 하는 고체 촬상 장치.

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청구항 17

제16항에 있어서,

제1 광전 변환부에 연결된 전송 트랜지스터와,

상기 제1 광전 변환부와 상기 플로팅 디퓨전부 사이에 배치된 전송 게이트 전극을 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 18

제17항에 있어서,

상기 전송 게이트 전극은 상기 제1 광전 변환부와 상기 플로팅 디퓨전부 사이에 대각선 방향으로 배치되는 것을 특징으로 하는 고체 촬상 장치.

청구항 19

제1항에 있어서,

상기 제2 광전 변환부를 둘러싸는 소자 분리부를 포함하고, 상기 소자 분리부는 상기 제1 절연막의 제1 부분 및 상기 제2 절연막을 더 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 20

제1항에 있어서,

상기 제1 홈부의 적어도 일부 상에 배치된 차광막을 더 포함하는 것을 특징으로 하는 고체 촬상 장치.

청구항 21

제1항에 있어서,

플로팅 디퓨전부와, 상기 제1 홈부는 상기 플로팅 디퓨전부 상에 배치되는 것을 특징으로 하는 고체 촬상 장치.

청구항 22

고체 촬상 장치는,

반도체 기판과,

상기 반도체 기판 내의 제1 광전 변환부와,

상기 반도체 기판 내의 제2 광전 변환부와,

상기 반도체 기판 내의 제3 광전 변환부와,

상기 제1 광전 변환부와 상기 제2 광전 변환부 사이에 배치된 제1 홈부와,

상기 제1 홈부는 상기 반도체 기판의 깊이 방향으로 연장되고, 고정 전하를 갖는 제1 절연막의 제1 부분을 포함하며,

상기 제2 광전 변환부와 상기 제3 광전 변환부 사이에 배치된 제2 홈부와,

상기 제2 홈부는 반도체 기판의 깊이 방향으로 연장되고, 상기 제1 절연막의 제2 부분을 포함하며,

상기 제1 및 제2 광전 변환부 사이의 제1 절연막 상에 배치되는 제2 절연막과,

상기 제1 홈부의 깊이는 상기 제2 홈부의 깊이보다 깊으며, 상기 고체 촬상 장치상에 화상을 형성하도록 구성된 광학 렌즈를 포함하는 것을 특징으로 하는 전자 기기.

발명의 설명

기 술 분 야

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[0001] 본 개시는, 이면(裏面) 조사형의 고체 촬상 장치와 그 제조 방법 및 전자 기기에 관한 것이다.

배 경 기 술

[0002] 근래, 기판상의 배선층이 형성되는 측과는 반대측부터 광을 조사하는, 이면 조사형의 고체 촬상 장치가 제안되어 있다(하기 특허 문헌 1 참조). 이면 조사형의 고체 촬상 장치에서는, 광조사측에 배선층이나 회로 소자 등이 형성되지 않기 때문에, 기판에 형성된 수광부의 개구률을 높게 할 수 있는 외에, 입사광이 배선층 등에서 반사되는 일 없이 수광부에 입사되기 때문에, 감도의 향상이 도모된다.

[0003] 특허 문헌 1의 고체 촬상 장치는, 광학 혼색(混色)을 저감하기 위해, 화소 경계에 차광막을 마련하고 있다.

선행기술문헌

특허문헌

[0004] (특허문헌 0001) 일본 특개2010-186818호 공보

발명의 내용

해결하려는 과제

[0005] 이와 같은 고체 촬상 장치에서, 광학 혼색의 저감 등의 한층 더 특성 향상이 요구되고 있다.

[0006] 본 개시는, 광학 혼색의 저감 등의 특성을 더욱 향상시킨 고체 촬상 장치를 제공한다. 또한, 그 고체 촬상 장치를 이용한 전자 기기를 제공한다.

과제의 해결 수단

[0007] 본 개시된 제1의 측면의 고체 촬상 장치는, 기판과, 기판에 형성된 복수의 광전 변환부를 구비한다. 또한, 기판의 광입사측부터 깊이 방향으로 형성된 홈부(溝部) 내에서, 홈부의 내벽면을 피복하도록 형성된 고정 전하를 갖는 절연막으로 구성되는 소자 분리부를 구비한다.

[0008] 본 개시된 제2의 측면의 고체 촬상 장치는, 기판과, 상기 기판에 형성된 복수의 광전 변환부를 구비한다. 또한, 기판의 광입사측부터 깊이 방향으로 형성된 홈부와, 홈부의 내벽면을 피복하도록 마련된 막을 구비하고, 중공(中空) 구조를 갖는 소자 분리부를 구비한다.

[0009] 본 개시된 제1의 측면의 고체 촬상 장치의 제조 방법은, 기판에, 광전 변환부를 갖는 복수의 화소를 형성하는 공정과, 기판의 이면측부터 깊이 방향에 걸쳐서 소망하는 깊이의 홈부를 형성하는 공정을 갖는다. 다음에, 홈부의 내벽면에 고정 전하를 갖는 절연막을 형성하고, 소자 분리부를 형성하는 공정을 갖는다.

[0010] 본 개시된 제2의 측면의 고체 촬상 장치의 제조 방법은, 기판에, 광전 변환부를 갖는 복수의 화소를 형성하는 공정과, 기판의 이면측부터 깊이 방향에 걸쳐서 소망하는 깊이의 홈부를 형성하는 공정을 갖는다. 다음에, 홈부의 내부에 중공부가 형성되도록 상기 홈부의 내벽면에 소망하는 막을 성막함으로써 소자 분리부를 형성하는 공정을 갖는다.

[0011] 본 개시된 전자 기기는, 광학 렌즈와, 광학 렌즈에 집광된 광이 입사되는 상술한 고체 촬상 장치와, 고체 촬상 장치로부터 출력되는 출력 신호를 처리하는 신호 처리 회로를 구비한다.

발명의 효과

[0012] 본 개시에 의하면, 고체 촬상 장치에서, 혼색 저감 등의 특성의 한층 더 향상이 도모된다. 또한, 그 고체 촬상 장치를 이용함에 의해, 화질의 향상이 도모된 전자 기기를 얻을 수 있다.

도면의 간단한 설명

[0013] 도 1은 본 개시된 제1의 실시 형태에 관한 고체 촬상 장치의 전체 구성을 도시하는 도면.

도 2는 본 개시된 제1의 실시 형태에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

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도 3은 본 개시된 제1의 실시 형태에 관한 고체 촬상 장치의 평면 레이아웃도.

도 4의 A 및 도 4의 B는, 본 개시된 제1의 실시 형태에 관한 고체 촬상 장치의 제조 방법을 도시하는 도면.

도 5의 C 및 도 5의 D는, 본 개시된 제1의 실시 형태에 관한 고체 촬상 장치의 제조 방법을 도시하는 도면.

도 6은 본 개시된 제1의 실시 형태에 관한 고체 촬상 장치와 종래의 고체 촬상 장치의 주요부의 포텐셜 분포도.

도 7은 제1의 실시 형태의 변형례 1에 관한 고체 촬상 장치의 평면 레이아웃도.

도 8은 제1의 실시 형태의 변형례 2에 관한 고체 촬상 장치의 평면 레이아웃도.

도 9는 본 개시된 제2의 실시 형태에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

도 10의 A 내지 도 10의 C는, 본 개시된 제2의 실시 형태에 관한 고체 촬상 장치의 제조 방법을 도시하는 도면.

도 11은 본 개시된 제3의 실시 형태에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

도 12는 본 개시된 제4의 실시 형태에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

도 13의 A 및 도 13의 B는, 본 개시된 제4의 실시 형태에 관한 고체 촬상 장치의 제조 방법을 도시하는 도면.

도 14의 C는, 본 개시된 제4의 실시 형태에 관한 고체 촬상 장치의 제조 방법을 도시하는 도면.

도 15는 본 개시된 제5의 실시 형태에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

도 16은 본 개시된 제6의 실시 형태에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

도 17은 본 개시된 제7의 실시 형태에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

도 18의 A 및 도 18의 B는, 본 개시된 제7의 실시 형태에 관한 고체 촬상 장치의 제조 방법을 도시하는 도면.

도 19는 본 개시된 제8의 실시 형태에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

도 20의 A 및 도 20의 B는, 본 개시된 제8의 실시 형태에 관한 고체 촬상 장치의 제조 방법을 도시하는 도면.

도 21은 변형례에 관한 고체 촬상 장치의 주요부의 단면 구성을 도시하는 도면.

도 22는 본 개시된 제9의 실시 형태에 관한 전자 기기의 개략 구성도.

발명을 실시하기 위한 구체적인 내용

[0014] 본 발명자들은, 특허 문헌 1의 고체 촬상 장치에서, 이하의 과제를 발견하였다.

[0015] 이면형의 고체 촬상 장치에서는, 포토 다이오드가 형성되는 반도체층이 표면 조사형의 고체 촬상 장치와 비교하여 얇게 형성된다. 이 때문에, 종래의 표면 조사형의 고체 촬상 장치에서는, 포토 다이오드에서 넘쳐진 신호 전하는 반도체층의 깊이 방향(종방향)으로 오버플로시키는 구성이 채택되어 있지만, 이면 조사형의 고체 촬상 장치에서는, 반도체층의 깊이 방향으로 오버플로시킬 수가 없다. 이 때문에, 이면 조사형의 고체 촬상 장치에서는, 포토 다이오드에서 넘쳐진 전자는, 플로팅 디퓨전에 흐르도록 구성되어 있다(이른바, 래터럴 오버플로).

[0016] 래터럴 오버플로 구조를 채용하는 경우, 포토 다이오드로부터 넘쳐진 전자가, 플로팅 디퓨전측으로 흐르는지, 인접하는 포토 다이오드측으로 흐르는지는, 기판 내의 포텐셜에 의해 정해진다. 따라서 전하 축적시에, 포토 다이오드와 플로팅 디퓨전과의 사이의 포텐셜을, 인접하는 포토 다이오드 사이의 포텐셜보다도 높게 설정함으로써, 넘쳐진 전자를 수시로 플로팅 디퓨전에 전송할 수 있다. 이 때문에, 넘쳐진 전자를 플로팅 디퓨전에 전송 가능한 구성으로 하는 경우, 포화 전하량(Qs)의 저하가 큰 과제로 된다. 한편, 포화 전하량을 크게 한 경우에는, 장시간 축적시에 백점(白点) 화소로부터 넘쳐진 신호 전하가 인접하는 화소에 누입(漏入)되어 감으로써 블루밍(blooming)이 발생하고, 해상도 열화, 화질 열화의 하나의 원인이 된다.

[0017] 또한, 화소 경계에 차광막을 마련하는 구조에서는, 비스듬한 광이 들어온 경우에 차광막의 아래에서 발생하는 혼색을 완전히 억제할 수가 없다.

[0018] 본 개시된 실시 형태에서는, 혼색 저감, 블루밍의 억제나 포화 특성의 향상이 가능한 고체 촬상 장치에 관해 설명한다.

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[0019] 이하에, 본 개시된 실시 형태에 관한 고체 촬상 장치와 그 제조 방법, 및 전자 기기의 한 예를, 도 1 내지 도 22를 참조하면서 설명한다. 본 개시된 실시 형태는 이하의 순서로 설명한다. 또한, 본 개시는 이하의 예로 한정되는 것이 아니다.

[0020] 1. 제1의 실시 형태 : 고체 촬상 장치(4화소로 하나의 플로팅 디퓨전부를 공유하는 예)

[0021] 1-1 고체 촬상 장치 전체의 구성

[0022] 1-2 주요부의 구성

[0023] 1-3 고체 촬상 장치의 제조 방법

[0024] 1-4 변형례 1

[0025] 1-5 변형례 2

[0026] 2. 제2의 실시 형태 : 고체 촬상 장치(소자 분리부 내에 차광막이 형성되는 예)

[0027] 3. 제3의 실시 형태 : 고체 촬상 장치(소자 분리부의 기판 이면측의 단부만이 p형 반도체 영역에 접하는 예)

[0028] 4. 제4의 실시 형태 : 고체 촬상 장치(소자 분리부가 기판을 관통하는 예)

[0029] 5. 제5의 실시 형태 : 고체 촬상 장치(소자 분리부 내에 형성된 차광층이 배선층에 접속되는 예)

[0030] 6. 제6의 실시 형태 : 고체 촬상 장치(소자 분리부에 2층의 고정 전하막을 형성하는 예)

[0031] 7. 제7의 실시 형태 : 고체 촬상 장치(소자 분리부가 중공 구조인 예)

[0032] 8. 제8의 실시 형태 : 고체 촬상 장치(소자 분리부가 중공 구조인 예)

[0033] 8-1 변형례

[0034] 9. 제9의 실시 형태 : 전자 기기

[0035] <1. 제1의 실시 형태 : 고체 촬상 장치>

[0036] [1-1 고체 촬상 장치 전체의 구성]

[0037] 도 1은, 본 개시된 제1의 실시 형태에 관한 CMOS형의 고체 촬상 장치의 전체를 도시하는 개략 구성도이다.

[0038] 본 실시 형태의 고체 촬상 장치(1)는, 실리콘으로 이루어지는 기판(11)상에 배열된 복수의 화소(2)를 갖는 화소 영역(3)과, 수직 구동 회로(4)와, 칼럼 신호 처리 회로(5)와, 수평 구동 회로(6)와, 출력 회로(7)와, 제어 회로(8) 등을 갖고서 구성된다.

[0039] 화소(2)는, 포토 다이오드로 이루어지는 광전 변환부와, 복수의 화소 트랜지스터로 구성되고, 기판(11)상에, 2차원 어레이형상으로 규칙적으로 복수 배열된다. 화소(2)를 구성하는 화소 트랜지스터는, 전송 트랜지스터, 리셋 트랜지스터, 선택 트랜지스터, 앰프 트랜지스터로 구성되는 4개의 MOS 트랜지스터라도 좋고, 또한, 선택 트랜지스터를 제외한 3개의 트랜지스터라도 좋다.

[0040] 화소 영역(3)은, 2차원 어레이형상으로 규칙적으로 배열된 복수의 화소(2)를 갖는다. 화소 영역(3)은, 실제로 광을 수광하고 광전 변환에 의해 생성된 신호 전하를 증폭하여 칼럼 신호 처리 회로(5)에 판독하는 유효 화소 영역과, 흑레벨의 기준이 되는 광학적 흑을 출력하기 위한 흑 기준 화소 영역(도시 생략)으로 구성되어 있다. 흑 기준 화소 영역은, 통상은, 유효 화소 영역의 외주부에 형성되는 것이다.

[0041] 제어 회로(8)는, 수직 동기 신호, 수평 동기 신호 및 마스터 클록에 의거하여, 수직 구동 회로(4), 칼럼 신호 처리 회로(5), 및 수평 구동 회로(6) 등의 동작의 기준이 되는 클록 신호나 제어 신호 등을 생성한다. 그리고, 제어 회로(8)에서 생성된 클록 신호나 제어 신호 등은, 수직 구동 회로(4), 칼럼 신호 처리 회로(5) 및 수평 구동 회로(6) 등에 입력된다.

[0042] 수직 구동 회로(4)는, 예를 들면 시프트 레지스터에 의해 구성되고, 화소 영역(3)의 각 화소(2)를 행 단위로 순차적으로 수직 방향으로 선택 주사한다. 그리고, 각 화소(2)의 포토 다이오드에서 수광량에 응하여 생성한 신호 전하에 의거한 화소 신호를, 수직 신호선을 통하여 칼럼 신호 처리 회로(5)에 공급한다.

[0043] 칼럼 신호 처리 회로(5)는, 예를 들면, 화소(2)의 열마다 배치되어 있고, 1행분의 화소(2)로부터 출력된 신호를 화소열마다 흑 기준 화소 영역(도시하지 않지만, 유효 화소 영역의 주위에 형성된다)으로부터의 신호에 의해,

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노이즈 제거나 신호 증폭 등의 신호 처리를 행한다. 칼럼 신호 처리 회로(5)의 출력단에는, 수평 선택 스위치(도시 생략)가 수평 신호선(10)과의 사이에 마련되어 있다.

[0044] 수평 구동 회로(6)는, 예를 들면 시프트 레지스터에 의해 구성되고, 수평 주사 펄스를 순차적으로 출력함에 의해, 칼럼 신호 처리 회로(5)의 각각을 순번대로 선택하고, 칼럼 신호 처리 회로(5)의 각각으로부터 화소 신호를 수평 신호선(10)에 출력시킨다.

[0045] 출력 회로(7)는, 칼럼 신호 처리 회로(5)의 각각으로부터 수평 신호선(10)을 통하여, 순차적으로 공급되는 신호에 대해 신호 처리를 행하여 출력한다.

[0046] [1-2 주요부의 구성]

[0047] 도 2에, 본 실시 형태의 고체 촬상 장치(1)의 화소 영역(3)에서의 단면 구성을 도시하고, 도 3에, 본 실시 형태의 고체 촬상 장치(1)의 화소 영역(3)의 평면 레이아웃을 도시한다. 본 실시 형태의 고체 촬상 장치(1)는, 이면 조사형의 CMOS형 고체 촬상 장치를 예로 한 것이고, 4개의 광전 변환부에 대해 소요되는 화소 트랜지스터를 공유시킨, 이른바 4화소 공유를 1단위로 한 예이다. 또한, 이하의 설명에서는, 제1 도전형을 p형으로 하고, 제2 도전형을 n형으로 하여 설명한다.

[0048] 도 2에 도시하는 바와 같이, 본 실시 형태의 고체 촬상 장치(1)는, 복수의 화소를 갖는 기판(12)과, 기판(12)의 표면측에 형성된 배선층(13)과, 지지 기판(31)을 구비한다. 또한, 기판(12)의 이면측에 차례로 형성된 고정 전하를 갖는 절연막(이하, 고정 전하막)(20)과, 절연막(21)과, 차광막(25)과, 평탄화막(26)과, 컬러 필터층(27)과, 온칩 렌즈(28)를 또한 구비한다.

[0049] 기판(12)은, 실리콘으로 이루어지는 반도체 기판으로 구성되고, 예를 들면 1㎛ 내지 6㎛의 두께를 갖고서 형성되어 있다. 기판(12)의 화소 영역(3)에는 포토 다이오드로 이루어지는 광전 변환부(40)와, 화소 회로부를 구성하는 복수의 화소 트랜지스터(Tr1 내지 Tr4)로 구성되는 화소가 복수개, 2차원 매트릭스형상으로 형성되어 있다. 그리고, 인접하는 광전 변환부(40) 사이는 소자 분리부(19)에 의해 전기적으로 분리되어 있다. 또한, 도 2에서는 도시를 생략하지만, 기판(12)에 형성된 화소 영역의 주변 영역에는, 주변 회로부가 구성되어 있다.

[0050] 광전 변환부(40)는, 기판(12)의 표면측 및 이면측에 형성되는 제1 도전형(이하 p형) 반도체 영역(23, 24)과, 그 사이에 형성되는 제2 도전형(이하 n형) 반도체 영역(22)으로 구성되어 있다. 광전 변환부(40)에서는, 그 p형 반도체 영역(23, 24)과 n형 반도체 영역(22)와의 사이의 pn 접합으로 주된 포토 다이오드가 구성되어 있다. 광전 변환부(40)에서는, 입사한 광의 광량에 응한 신호 전하가 생성되고, n형 반도체 영역(22)에 축적된다. 또한, 기판(12)의 계면에서 발생하는 암전류의 원인이 되는 전자는 기판(12)의 표면 및 이면에 형성된 p형 반도체 영역(23, 24)의 다수 캐리어인 정공에 흡수됨에 의해, 암전류가 억제된다.

[0051] 또한, 각 광전 변환부(40)는 p형 반도체 영역으로 구성된 화소 분리층(18)과, 그 화소 분리층(18) 내에 형성된 소자 분리부(19)에 의해 전기적으로 분리되어 있다.

[0052] 화소 트랜지스터는, 본 실시 형태에서는, 도 3에 도시하는 바와 같이, 전송 트랜지스터(Tr1), 리셋 트랜지스터(Tr2), 증폭 트랜지스터(Tr3), 선택 트랜지스터(Tr4)의 4개의 트랜지스터로 구성되어 있다.

[0053] 전송 트랜지스터(Tr1)는, 도 3에 도시하는 바와 같이, 2행2열로 형성된 4개의 광전 변환부(40)의 중심부에 형성된 플로팅 디퓨전부(30)와, 전송 게이트 전극(16)으로 구성되어 있다. 플로팅 디퓨전부(30)는, 도 2에 도시하는 바와 같이, 기판(12)의 표면측에 형성된 p-웰층(29)에, n형의 불순물이 고농도로 이온 주입됨으로써 형성된 n형 반도체 영역으로 구성된다. 또한, 전송 게이트 전극(16)은, 광전 변환부(40)와 플로팅 디퓨전부(30)와의 사이의 기판(12) 표면측에, 게이트 절연막(17)을 통하여 형성되어 있다.

[0054] 화소 트랜지스터 중, 리셋 트랜지스터(Tr2), 증폭 트랜지스터(Tr3), 선택 트랜지스터(Tr4)는 플로팅 디퓨전부(30)를 공유하는 4개의 광전 변환부(40)마다 형성되어 있다. 이들의 화소 트랜지스터는, 도 3에 도시하는 바와 같이 4개의 광전 변환부(40)로 구성되는 군의 일방의 측에 배치되어 있다.

[0055] 리셋 트랜지스터(Tr2)는, 대(對)의 소스·드레인 영역(35 및 36)과, 그 소스·드레인 영역(35, 36)의 사이에 형성된 리셋 게이트 전극(32)에 의해 구성된다. 증폭 트랜지스터(Tr3)는, 대의 소스·드레인 영역(36 및 37)과, 그 소스·드레인 영역(36, 37)의 사이에 형성된 증폭 게이트 전극(33)에 의해 구성된다. 선택 트랜지스터(Tr4)는, 대의 소스·드레인 영역(37 및 38)과, 그 소스·드레인 영역(37, 38)의 사이에 형성된 선택 게이트 전극(34)에 의해 구성된다.

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[0056] 리셋 트랜지스터(Tr2), 증폭 트랜지스터(Tr3), 선택 트랜지스터(Tr4)에 관해서는 단면 구성의 도시를 생략하지만, 이들의 화소 트랜지스터에 관해서도 전송 트랜지스터(Tr1)와 같은 구성으로 되어 있다. 즉, 소스·드레인 영역(35 내지 38)은, 플로팅 디퓨전부(30)와 마찬가지로 기판(12)의 표면의 p-웰층(29) 내에 형성된 n형의 고농도 불순물 영역으로 구성된다. 또한, 리셋 게이트 전극(32), 증폭 게이트 전극(33), 선택 게이트 전극(34)은, 기판(12)의 표면측에 게이트 절연막(17)을 통하여 형성되어 있다.

[0057] 소자 분리부(19)는, 기판(12)의 이면측부터 깊이 방향으로 형성된 홈부(39) 내에 차례로 매입하여 형성된 고정 전하막(20), 및 절연막(21)으로 구성되고, 기판(12)에 형성된 화소 분리층(18) 내에 새겨 넣어져서 형성되어 있다. 즉, 소자 분리부(19)는, 도면에 도시하는 바와 같이 화소를 둘러싸도록 격자형상으로 형성되어 있다. 또한, 인접하는 광전 변환부(40)와 광전 변환부(40)의 사이에 화소 트랜지스터가 형성되어 있는 경우에는, 플로팅 디퓨전부(30)나 소스·드레인 영역에 겹쳐지도록 배치되어 있다.

[0058] 또한, 소자 분리부(19)는, 화소 트랜지스터가 형성되는 p-웰층(29)에 달하는 깊이로 형성되고, 플로팅 디퓨전부(30)나 소스·드레인 영역에는 달하지 않는 깊이로 형성되어 있다. 플로팅 디퓨전부(30)나 소스·드레인 영역의 깊이가 1㎛ 미만이라고 하면, 소자 분리부(19)는, 기판(12) 표면부터 0.25 내지 5.0㎛ 정도의 깊이까지 형성할 수 있다. 본 실시 형태에서는, 화소 트랜지스터의 p-웰층(29)에 달하는 깊이로 형성되어 있지만, 소자 분리부(19)의 기판(12) 이면측의 단부가 p형의 반도체층에 접하도록 형성되면 좋고, 반드시 p-웰층(29)에 달하는 깊이가 아니라도 좋다. 본 실시 형태와 같이, p형 반도체층으로 이루어지는 화소 분리층(18) 내에 형성되는 경우에는, p-웰층(29)에 달하지 않는 구성으로도 절연 분리의 효과를 얻을 수 있다.

[0059] 또한, 홈부(39)에 형성되는 고정 전하막(20)은 홈부(39)의 내주면(內周面) 및 저면에 성막됨과 함께, 기판(12)의 이면 전면(全面)에 형성되어 있다. 또한, 이하의 설명에서는, 홈부(30)의 내주면 및 저면을 합쳐서, 「내벽면」으로 하여 설명한다. 고정 전하막(20)으로서는, 실리콘 등의 기판상에 퇴적함에 의해 고정 전하를 발생시켜서 피닝(pining)을 강화시키는 것이 가능한 재료를 사용하는 것이 바람직하고, 부(負)의 전하를 갖는 고굴절률 재료막 또는 고유전체막을 이용할 수 있다. 구체적인 재료로서는, 예를 들면, 하프늄(Hf), 알루미늄(Al), 지르코늄(Zr), 탄탈럼(Ta) 및 타이타늄(Ti) 중 적어도 하나의 원소를 포함하는 산화물 또는 질화물을 적용할 수 있다. 성막 방법으로서는, 예를 들면, 화학기상 성장법(이하, CVD(Chemical Vapor Deposition)법), 스퍼터링법, 원자층 증착법(이하, ALD(Atomic Layer Deposition)법) 등을 들 수 있다. ALD법을 이용하면, 성막중에 계면준위를 저감하는 SiO2막을 동시에 1㎚ 정도의 막두께로 형성할 수 있다. 또한, 상기 이외의 재료로서는, 란타넘(La), 프라세오디뮴(Pr), 세륨(Ce), 네오디뮴(Nd), 프로메튬(Pm), 사마륨(Sm), 유로퓸(Eu), 가돌리늄(Gd), 터븀(Tb), 디스프로슘(Dy), 홀뮴(Ho), 툴륨(Tm), 이터븀(Yb), 루테튬(Lu) 및 이트륨(Y) 중 적어도 하나의 원소를 포함하는 산화물 또는 질화물 등을 들 수 있다. 또한, 상기 고정 전하막은, 산질화하프늄막 또는 산질화알루미늄막으로 형성하는 것도 가능하다.

[0060] 상술한 고정 전하막(20)의 재료에는, 절연성을 손상시키지 않는 범위에서, 막 내에 실리콘(Si)이나 질소(N)가 첨가되어 있어도 좋다. 그 농도는, 막의 절연성이 손상되지 않는 범위에서 적절히 결정된다. 이와 같이, 실리콘(Si)이나 질소(N)가 첨가됨에 의해, 막의 내열성이나 프로세스 중에서 이온 주입의 저지 능력을 올리는 것이 가능해진다.

[0061] 본 실시 형태에서는, 홈부(39)의 내벽면 및 기판(12)의 이면에 부의 전하를 갖는 고정 전하막(20)이 형성되어 있기 때문에, 고정 전하막(20)에 접한 면에 반전층이 형성된다. 이에 의해, 실리콘 계면이 반전층에 의해 피닝되기 때문에, 암전류의 발생이 억제된다. 또한, 기판(12)에 홈부(39)를 형성하는 경우, 홈부(39)의 측벽 및 저면에 물리적 데미지가 발생하고, 홈부(39)의 주변부에서 피닝 어긋남이 발생할 가능성이 있다. 이 문제점에 대해, 본 실시 형태에서는, 홈부(39)의 측벽 및 저면에 고정 전하를 많이 갖는 고정 전하막(20)을 형성함에 의해 피닝 어긋남이 방지된다.

[0062] 절연막(21)은, 고정 전하막(20)이 형성된 홈부(39) 내에 매입됨과 함께, 기판(12)의 이면측 전면에 형성되어 있다. 절연막(21)의 재료로서는, 고정 전하막(20)과는 다른 굴절률을 갖는 재료로 형성하는 것이 바람직하고, 예를 들면, 산화실리콘, 질화실리콘, 산질화실리콘, 수지 등을 사용할 수 있다. 또한, 정(正)의 고정 전하를 갖지 않는, 또는 정의 고정 전하가 적다는 특징을 갖는 재료를 절연막(21)에 이용할 수 있다.

[0063] 그리고, 홈부(39)가 절연막(21)으로 매입됨에 의해, 각 화소를 구성하는 광전 변환부(40)가 절연막(21)을 통하여 분리된다. 이에 의해, 인접 화소에 신호 전하가 누입되기 어려워지기 때문에, 포화 전하량(Qs)을 초과한 신호 전하가 발생한 경우에 있어서, 넘쳐진 신호 전하가 인접하는 광전 변환부(40)에 누입되는 것을 저감할 수 있

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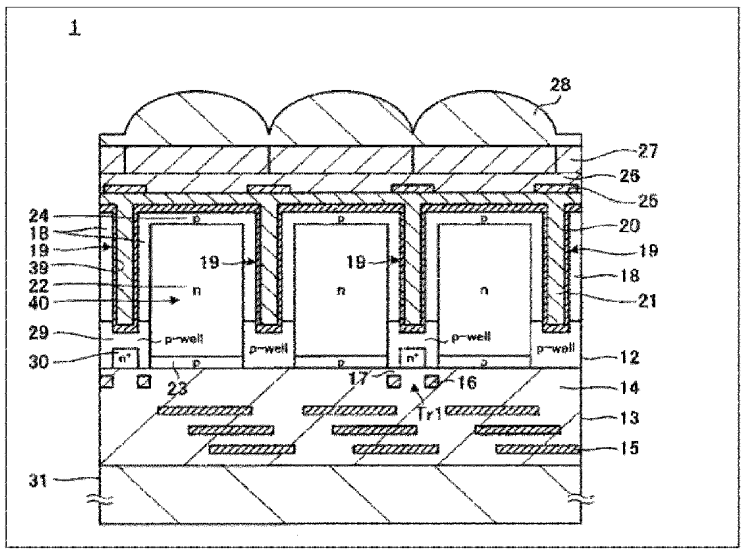
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[続葉有]

(54) **Title**: SOLID STATE IMAGING DEVICE AND FABRICATION METHOD THEREFOR, AND ELECTRONIC INSTRUMENT

(54) 発明の名称 : 固体撮像装置、固体撮像装置の製造方法及び電子機器

[図2]



(57) **Abstract**: The present invention relates to the provision of a solid state imaging device having improved characteristics such as reduced optical color mixing, a fabrication method for the same, and an electronic instrument. An electronic instrument using the solid state imaging device is also provided. A solid state imaging device provided with a substrate (12) and a plurality of photoelectric conversion units (40) formed in the substrate (12), wherein element isolation sections (19) having insulating layers (21) buried therein are formed. The element isolation sections (19) are constituted by insulating layers (20) that have a fixed electrical charge and that are formed so as to cover the surface of the inner walls of groove sections (30), the groove sections (30) being formed in the depth direction from the optical incidence side of the substrate (12).

(57) 要約: 本技術は、光学混色の低減等の特性をさらに向上させた固体撮像装置を提供することができる固体撮像装置、固体撮像装置の製造方法及び電子機器に関する。また、その固体撮像装置を用いた電子機器を提供する。基板１２と、基板１２に形成された複数の光電変換部４０とを備える固体撮像装置において、絶縁膜２１が埋め込まれた素子分離部１９を形成する。素子分離部１９は、基板１２の光入射側から深さ方向に形成された溝部３０内において、溝部３０の内壁面を被覆するように形成された固定電荷を有する絶縁膜２０で構成されている。

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明　細　書

発明の名称 ：

固体撮像装置、固体撮像装置の製造方法及び電子機器

技術分野

[0001] 本開示は、裏面照射型の固体撮像装置とその製造方法及び電子機器に関する。

背景技術

[0002] 近年、基板上の配線層が形成される側とは反対側から光を照射する、裏面照射型の固体撮像装置が提案されている（下記特許文献１参照）。裏面照射型の固体撮像装置では、光照射側に配線層や回路素子等が形成されないため、基板に形成された受光部の開口率を高くできる他、入射光が配線層等に反射されることなく受光部に入射されるので、感度の向上が図られる。

特許文献１の固体撮像装置は、光学混色を低減するために、画素境界に遮光膜を設けている。

先行技術文献

特許文献

[0003] 特許文献1：特開２０１０－１８６８１８号公報

発明の概要

発明が解決しようとする課題

[0004] このような固体撮像装置において、光学混色の低減等のさらなる特性向上が求められている。

[0005] 本開示は、光学混色の低減等の特性をさらに向上させた固体撮像装置を提供する。また、その固体撮像装置を用いた電子機器を提供する。

課題を解決するための手段

[0006] 本開示の第１の側面の固体撮像装置は、基板と、基板に形成された複数の光電変換部とを備える。また、基板の光入射側から深さ方向に形成された溝

部内において、溝部の内壁面を被覆するように形成された固定電荷を有する絶縁膜で構成された素子分離部を備える。

[0007] 本開示の第２の側面の固体撮像装置は、基板と、前記基板に形成された複数の光電変換部とを備える。また、基板の光入射側から深さ方向に形成された溝部と、溝部の内壁面を被覆するように設けられた膜を備え、中空構造を有する素子分離部を備える。

[0008] 本開示の第１の側面の固体撮像装置の製造方法は、基板に、光電変換部を有する複数の画素を形成する工程と、基板の裏面側から深さ方向にかけて所望の深さの溝部を形成する工程を有する。次に、溝部の内壁面に固定電荷を有する絶縁膜を形成し、素子分離部を形成する工程を有する。

[0009] 本開示の第２の側面の固体撮像装置の製造方法は、基板に、光電変換部を有する複数の画素を形成する工程と、基板の裏面側から深さ方向にかけて所望の深さの溝部を形成する工程を有する。次に、溝部の内部に中空部が形成されるように前記溝部の内壁面に所望の膜を成膜することで素子分離部を形成する工程を有する。

[0010] 本開示の電子機器は、光学レンズと、光学レンズに集光された光が入射される上述の固体撮像装置と、固体撮像装置から出力される出力信号を処理する信号処理回路とを備える。

発明の効果

[0011] 本開示によれば、固体撮像装置において、混色低減等の特性のさらなる向上が図られる。また、その固体撮像装置を用いることにより、画質の向上が図られた電子機器が得られる。

図面の簡単な説明

[0012] [図1]本開示の第１の実施形態に係る固体撮像装置の全体構成を示す図である。

[図2]本開示の第１の実施形態に係る固体撮像装置の要部の断面構成を示す図である。

[図3]本開示の第１の実施形態に係る固体撮像装置の平面レイアウトである。

[図4]図４のＡ及び図４のＢは、本開示の第１の実施形態に係る固体撮像装置の製造方法を示す図である。

[図5]図４のＣ及び図４のＤは、本開示の第１の実施形態に係る固体撮像装置の製造方法を示す図である。

[図6]本開示の第１の実施形態に係る固体撮像装置と従来の固体撮像装置の要部のポテンシャル分布図である。

[図7]第１の実施形態の変形例１に係る固体撮像装置の平面レイアウトである。

[図8]第１の実施形態の変形例２に係る固体撮像装置の平面レイアウトである。

[図9]本開示の第２の実施形態に係る固体撮像装置の要部の断面構成を示す図である。

[図10]図１０のＡ～図１０のＣは、本開示の第２の実施形態に係る固体撮像装置の製造方法を示す図である。

[図11]本開示の第３の実施形態に係る固体撮像装置の要部の断面構成を示す図である。

[図12]本開示の第４の実施形態に係る固体撮像装置の要部の断面構成を示す図である。

[図13]図１３のＡ及び図１３のＢは、本開示の第４の実施形態に係る固体撮像装置の製造方法を示す図である。

[図14]図１４のＣは、本開示の第４の実施形態に係る固体撮像装置の製造方法を示す図である。

[図15]本開示の第５の実施形態に係る固体撮像装置の要部の断面構成を示す図である。

[図16]本開示の第６の実施形態に係る固体撮像装置の要部の断面構成を示す図である。

[図17]本開示の第７の実施形態に係る固体撮像装置の要部の断面構成を示す図である。

[図18]図１８のＡ及び図１８のＢは、本開示の第７の実施形態に係る固体撮像装置の製造方法を示す図である。

[図19]本開示の第８の実施形態に係る固体撮像装置の要部の断面構成を示す図である。

[図20]図２０のＡ及び図２０のＢは、本開示の第８の実施形態に係る固体撮像装置の製造方法を示す図である。

[図21]変形例に係る固体撮像装置の要部の断面構成を示す図である。

[図22]本開示の第９の実施形態に係る電子機器の概略構成図である。

発明を実施するための形態

[0013] 本発明者らは、特許文献１の固体撮像装置において、以下の課題を発見した。

[0014] 裏面型の固体撮像装置では、フォトダイオードが形成される半導体層が表面照射型の固体撮像装置と比較して薄く形成される。このため、従来の表面照射型の固体撮像装置では、フォトダイオードで溢れた信号電荷は半導体層の深さ方向（縦方向）にオーバーフローさせる構成が採られていたが、裏面照射型の固体撮像装置では、半導体層の深さ方向にオーバーフローさせることができない。このため、裏面照射型の固体撮像装置では、フォトダイオードで溢れた電子は、フローティングディフュージョンへ流れるように構成されている（いわゆる、ラテラルオーバーフロー）。

[0015] ラテラルオーバーフロー構造を採用する場合、フォトダイオードから溢れた電子が、フローティングディフュージョン側に流れるか、隣接するフォトダイオード側に流れるかは、基板内のポテンシャルによって決まる。したがって、電荷蓄積時に、フォトダイオードとフローティングディフュージョンとの間のポテンシャルを、隣接するフォトダイオード間のポテンシャルよりも高く設定することで、溢れた電子を随時フローティングディフュージョンに転送することができる。このため、溢れた電子をフローティングディフュージョンに転送可能な構成とする場合、飽和電荷量（Ｑｓ）の低下が大きな課題となる。一方、飽和電荷量を大きくした場合には、長時間蓄積時に白点

画素から溢れた信号電荷が隣接する画素に漏れ込んでいくことでブルーミングが発生し、解像度劣化、画質劣化の一因となる。

また、画素境界に遮光膜を設ける構造では、斜めの光が入った場合に遮光膜の下で発生する混色を完全に抑制することができない。

本開示の実施形態では、混色低減、ブルーミングの抑制や飽和特性の向上が可能な固体撮像装置について説明する。

[0016] 以下に、本開示の実施形態に係る固体撮像装置とその製造方法、及び電子機器の一例を、図１～図２２を参照しながら説明する。本開示の実施形態は以下の順で説明する。なお、本開示は以下の例に限定されるものではない。

１．第１の実施形態：固体撮像装置（４画素で一つのフローティングディフュージョン部を共有する例）

１－１　固体撮像装置全体の構成

１－２　要部の構成

１－３　固体撮像装置の製造方法

１－４　変形例１

１－５　変形例２

２．第２の実施形態：固体撮像装置（素子分離部内に遮光膜が形成される例）

３．第３の実施形態：固体撮像装置（素子分離部の基板裏面側の端部のみがｐ型半導体領域に接する例）

４．第４の実施形態：固体撮像装置（素子分離部が基板を貫通する例）

５．第５の実施形態：固体撮像装置（素子分離部内に形成された遮光層が配線層に接続される例）

６．第６の実施形態：固体撮像装置（素子分離部に２層の固定電荷膜を形成する例）

７．第７の実施形態：固体撮像装置（素子分離部が中空構造である例）

８．第８の実施形態：固体撮像装置（素子分離部が中空構造である例）

８－１　変形例

９．第９の実施形態：電子機器

[0017] 〈１．第１の実施形態：固体撮像装置〉

［１－１　固体撮像装置全体の構成］

図１は、本開示の第１の実施形態に係るＣＭＯＳ型の固体撮像装置の全体を示す概略構成図である。

本実施形態の固体撮像装置１は、シリコンからなる基板１１上に配列された複数の画素２を有する画素領域３と、垂直駆動回路４と、カラム信号処理回路５と、水平駆動回路６と、出力回路７と、制御回路８等を有して構成される。

[0018] 画素２は、フォトダイオードからなる光電変換部と、複数の画素トランジスタとから構成され、基板１１上に、２次元アレイ状に規則的に複数配列される。画素２を構成する画素トランジスタは、転送トランジスタ、リセットトランジスタ、選択トランジスタ、アンプトランジスタで構成される４つのＭＯＳトランジスタであってもよく、また、選択トランジスタを除いた３つのトランジスタであってもよい。

[0019] 画素領域３は、２次元アレイ状に規則的に配列された複数の画素２を有する。画素領域３は、実際に光を受光し光電変換によって生成された信号電荷を増幅してカラム信号処理回路５に読み出す有効画素領域と、黒レベルの基準になる光学的黒を出力するための黒基準画素領域（図示せず）とから構成されている。黒基準画素領域は、通常は、有効画素領域の外周部に形成されるものである。

[0020] 制御回路８は、垂直同期信号、水平同期信号及びマスタクロックに基づいて、垂直駆動回路４、カラム信号処理回路５、及び水平駆動回路６等の動作の基準となるクロック信号や制御信号などを生成する。そして、制御回路８で生成されたクロック信号や制御信号などは、垂直駆動回路４、カラム信号処理回路５及び水平駆動回路６等に入力される。

[0021] 垂直駆動回路４は、例えばシフトレジスタによって構成され、画素領域３の各画素２を行単位で順次垂直方向に選択走査する。そして、各画素２のフ

ォトダイオードにおいて受光量に応じて生成した信号電荷に基づく画素信号を、垂直信号線を通してカラム信号処理回路５に供給する。

[0022] カラム信号処理回路５は、例えば、画素２の列毎に配置されており、１行分の画素２から出力される信号を画素列毎に黒基準画素領域（図示しないが、有効画素領域の周囲に形成される）からの信号によって、ノイズ除去や信号増幅等の信号処理を行う。カラム信号処理回路５の出力段には、水平選択スイッチ（図示せず）が水平信号線１０とのあいだに設けられている。

[0023] 水平駆動回路６は、例えばシフトレジスタによって構成され、水平走査パルスを順次出力することによって、カラム信号処理回路５の各々を順番に選択し、カラム信号処理回路５の各々から画素信号を水平信号線１０に出力させる。

[0024] 出力回路７は、カラム信号処理回路５の各々から水平信号線１０を通して、順次に供給される信号に対し信号処理を行い出力する。

[0025] ［１－２　要部の構成］

図２に、本実施形態の固体撮像装置１の画素領域３における断面構成を示し、図３に、本実施形態の固体撮像装置１の画素領域３の平面レイアウトを示す。本実施形態の固体撮像装置１は、裏面照射型のＣＭＯＳ型固体撮像装置を例としたものであり、４つの光電変換部に対して所要の画素トランジスタを共有させた、いわゆる４画素共有を１単位とした例である。また、以下の説明では、第１導電型をｐ型とし、第２導電型をｎ型として説明する。

[0026] 図２に示すように、本実施形態の固体撮像装置１は、複数の画素を有する基板１２と、基板１２の表面側に形成された配線層１３と、支持基板３１とを備える。また、基板１２の裏面側に順に形成された固定電荷を有する絶縁膜（以下、固定電荷膜）２０と、絶縁膜２１と、遮光膜２５と、平坦化膜２６と、カラーフィルタ層２７と、オンチップレンズ２８とをさらに備える。

[0027] 基板１２は、シリコンからなる半導体基板で構成され、例えば１μｍ～６μｍの厚みを有して形成されている。基板１２の画素領域３にはフォトダイオードからなる光電変換部４０と、画素回路部を構成する複数の画素トラン

ジスタ（Ｔｒ１～Ｔｒ４）とから構成される画素が複数個、二次元マトリクス状に形成されている。そして、隣接する光電変換部４０間は素子分離部１９により電気的に分離されている。また、図２では図示を省略するが、基板１２に形成された画素領域の周辺領域には、周辺回路部が構成されている。

[0028] 光電変換部４０は、基板１２の表面側及び裏面側に形成される第１導電型（以下ｐ型）半導体領域２３，２４と、その間に形成される第２導電型（以下ｎ型）半導体領域２２とで構成されている。光電変換部４０では、そのｐ型半導体領域２３，２４とｎ型半導体領域２２との間のｐｎ接合で主なフォトダイオードが構成されている。光電変換部４０では、入射した光の光量に応じた信号電荷が生成され、ｎ型半導体領域２２に蓄積される。また、基板１２の界面で発生する暗電流の原因となる電子は基板１２の表面及び裏面に形成されたｐ型半導体領域２３，２４の多数キャリアである正孔に吸収されることにより、暗電流が抑制される。

また、各光電変換部４０はｐ型半導体領域で構成された画素分離層１８と、その画素分離層１８内に形成された素子分離部１９によって電気的に分離されている。

[0029] 画素トランジスタは、本実施形態においては、図３に示すように、転送トランジスタＴｒ１、リセットトランジスタＴｒ２、増幅トランジスタＴｒ３、選択トランジスタＴｒ４の４つのトランジスタで構成されている。

[0030] 転送トランジスタＴｒ１は、図３に示すように、２行２列に形成された４つの光電変換部４０の中心部に形成されたフローティングディフュージョン部３０と、転送ゲート電極１６とで構成されている。フローティングディフュージョン部３０は、図２に示すように、基板１２の表面側に形成されたｐーウェル層２９に、ｎ型の不純物が高濃度にイオン注入されることで形成されたｎ型半導体領域で構成される。また、転送ゲート電極１６は、光電変換部４０とフローティングディフュージョン部３０との間の基板１２表面側に、ゲート絶縁膜１７を介して形成されている。

[0031] 画素トランジスタのうち、リセットトランジスタＴｒ２、増幅トランジス

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SOLID-STATE IMAGING APPARATUS, MANUFACTURING METHOD THEREFOR, AND CAMERA

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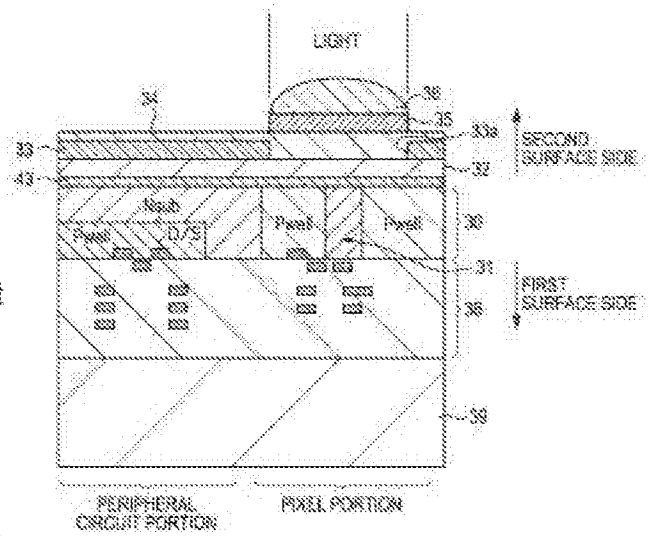
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Abstract of JP2007258684 (A)

PROBLEM TO BE SOLVED: To provide a solid-state imaging apparatus capable of suppressing at least dark current, a manufacturing method therefor, and a camera equipped with the solid-state imaging apparatus. SOLUTION: The solid-state imaging apparatus according to the present embodiment has a wiring layer on a first surface

side of a substrate 30 to receive light from a second surface side of the substrate 30. The solid-state imaging apparatus comprises: a light receiving unit 31 that is formed on the substrate 30 to include a charge-storage region 41; a transfer gate 51 that is disposed on the first surface of the substrate 30 to be adjacent to the light receiving unit 31 and transfers a signal charge stored in the light receiving unit 31; and a control gate 52 that is disposed on the first surface of the substrate 30 to overlie the light receiving unit 31 and controls the electric potential near the first surface of the light receiving unit 31. ;COPYRIGHT: (C)2008,JPO&INPIT



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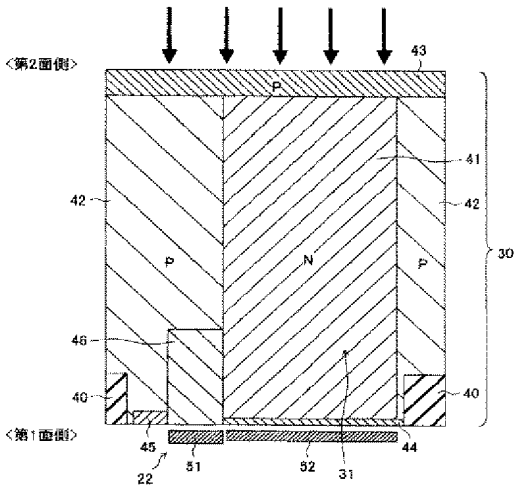
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(54)【発明の名称】固体撮像装置及びその製造方法、並びにカメラ

(57)【要約】
【課題】少なくとも暗電流の抑制を図ることができる固体撮像装置およびその製造方法、並びに当該固体撮像装置を備えたカメラを提供する。
【解決手段】本実施形態に係る固体撮像装置は、基板３０の第１面側に配線層を有し、基板３０の第２面側から光を受光する。当該固体撮像装置は、基板３０に形成され、電荷蓄積領域４１を含む受光部３１と、基板３０の第１面上であって受光部３１に隣接して配置され、受光部３１に蓄積された信号電荷を転送する転送ゲート５１と、基板３０の第１面上であって受光部３１に重なって配置され、受光部３１の第１面近傍のポテンシャルを制御する制御ゲート５２とを有する。
【選択図】図４



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【特許請求の範囲】
【請求項1】
基板の第１面側に配線層を有し、前記基板の第２面側から光を受光する固体撮像装置であって、
前記基板に形成され、第１導電型領域を含む受光部と、
前記基板の第１面上であって前記受光部に隣接して配置され、前記受光部に蓄積された信号電荷を転送する転送ゲートと、
前記基板の第１面上であって前記受光部に重なって配置され、前記受光部の第１面近傍のポテンシャルを制御する制御ゲートとを有する
ことを特徴とする固体撮像装置。
【請求項2】
前記受光部は、少なくとも前記第１面側または前記第２面側のいずれかには、第２導電型領域を有することを特徴とする請求項１記載の固体撮像装置。
【請求項3】
１つの受光部に対して複数の前記制御ゲートが配置されている
ことを特徴とする請求項１記載の固体撮像装置。
【請求項4】
基板の第１面側に配線層を有し、前記基板の第２面側から光を受光する固体撮像装置の製造方法であって、
基板に第１導電型領域を含む受光部を形成する工程と、
前記基板の第１面上であって前記受光部に隣接する部位に、転送ゲートを形成する工程と、
前記基板の第１面上であって前記受光部に重なる部位に、制御ゲートを形成する工程とを有する
ことを特徴とする固体撮像装置の製造方法。
【請求項5】
基板の第１面側に配線層を有し、前記基板の第２面側から光を受光する固体撮像装置と、
前記固体撮像装置の前記第２面側に入射光を導く光学系と、
前記固体撮像装置の出力信号を処理する信号処理回路と
を有し、
前記固体撮像装置は、
前記基板に形成され、第１導電型領域を含む受光部と、
前記基板の第１面上であって前記受光部に隣接して配置され、前記受光部に蓄積された信号電荷を転送する転送ゲートと、
前記基板の第１面上であって前記受光部に重なって配置され、前記受光部の第１面近傍のポテンシャルを制御する制御ゲートとを有する
ことを特徴とするカメラ。
【請求項6】
受光部の受光面上に透明導電膜を有し、
前記受光面と前記透明導電膜との間に存在する絶縁膜の膜厚が５０ｎｍ以下に設定されている
ことを特徴とする固体撮像装置。
【請求項7】
前記絶縁膜が、酸化シリコン膜または酸窒化シリコン膜である
ことを特徴とする請求項６記載の固体撮像装置。
【請求項8】
受光部の受光面上に透明導電膜を有し、
前記受光面と前記透明導電膜との間に存在する２種類以上の膜からなる積層膜のうち前

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記受光面に接する膜は酸化シリコン膜であり、前記酸化シリコン膜の膜厚が５０ｎｍ以下に設定されている
　ことを特徴とする固体撮像装置。
【請求項9】
　基板の第１面側に配線層が形成され、前記基板の第２面側を前記受光部の受光面として、裏面照射型に構成されている
　ことを特徴とする請求項７記載の固体撮像装置。
【請求項10】
　基板の第１面側に配線層が形成され、前記基板の第２面側を前記受光部の受光面として、裏面照射型に構成されている
　ことを特徴とする請求項８記載の固体撮像装置。
【請求項11】
　基板に形成された第１導電型領域を含む受光部の受光面上に膜厚５０ｎｍ以下の絶縁膜を形成する工程と、
　前記絶縁膜上に透明導電膜を形成する工程とを有する
　ことを特徴とする固体撮像装置の製造方法。
【請求項12】
　基板に形成された第１導電型領域を含む受光部の受光面上に、該受光面に接する膜厚５０ｎｍ以下の酸化シリコン膜を含んで２種類以上の積層絶縁膜を形成する工程と、
　前記積層絶縁膜上に透明導電膜を形成する工程とを有する
　ことを特徴とする固体撮像装置の製造方法。
【請求項13】
　固体撮像装置の受光部に入射光を導く光学系と、
　前記固体撮像装置の出力信号を処理する信号処理回路とを備え、
　前記固体撮像装置は、
　受光部の受光面上に透明導電膜を有し、
　前記受光面と前記透明導電膜との間に存在する絶縁膜の膜厚が５０ｎｍ以下に設定されている
　ことを特徴とするカメラ。
【請求項14】
　固体撮像装置の受光部に入射光を導く光学系と、
　前記固体撮像装置の出力信号を処理する信号処理回路とを備え、
　前記固体撮像装置は、
　受光部の受光面上に透明導電膜を有し、
　前記受光面と前記透明導電膜との間に存在する２種類以上の膜からなる積層膜のうち前記受光面に接する１種類の酸化シリコン膜の膜厚が５０ｎｍ以下に設定されている
　ことを特徴とするカメラ。
【請求項15】
　受光部の受光面上に負の固定電荷を有する膜が形成されている
　ことを特徴とする固体撮像装置。
【請求項16】
　前記負の固定電荷を有する膜は、一部が結晶化した絶縁膜である
　ことを特徴とする請求項１５記載の固体撮像装置。
【請求項17】
　前記少なくとも一部が結晶化した絶縁膜は、ハフニウム、ジルコニウム、アルミニウム、タンタル、チタン、イットリウム、ランタノイドから選ばれた元素の酸化物絶縁膜であり、膜中に少なくとも一部が結晶化した領域を有する
　ことを特徴とする請求項１６記載の固体撮像装置。
【請求項18】
　前記少なくとも一部が結晶化した絶縁膜の膜厚が３ｎｍ以上で１００ｎｍ以下である

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ことを特徴とする請求項１７記載の固体撮像装置。
【請求項19】
基板の第１面側に配線層が形成され、前記基板の第２面側を受光部の受光面として、裏面照射型に構成されている
ことを特徴とする請求項１６記載の固体撮像装置。
【請求項20】
固体撮像装置の受光部に入射光を導く光学系と、
前記固体撮像装置の出力信号を処理する信号処理回路とを備え、
前記固体撮像装置は、受光部の受光面上に負の固定電荷を有する膜が形成されている
【発明の詳細な説明】カメラ。
【技術分野】
【0001】
本発明は、固体撮像装置及びその製造方法、並びに当該固体撮像装置を備えるカメラに関する。
【背景技術】
【0002】
固体撮像装置、例えばＣＣＤイメージセンサやＣＭＯＳイメージセンサでは、受光部であるフォトダイオード中の結晶欠陥や、受光部とその上の絶縁膜との界面における界面準位が暗電流の発生源となることが知られている。そのうち、界面準位に起因した暗電流の発生を抑制する手法としては、埋め込み型フォトダイオード構造が有効である。この埋め込み型フォトダイオードは、ｎ型半導体領域を形成し、このｎ型半導体領域の表面すなわち絶縁膜との界面近傍に、暗電流抑制のための浅く不純物濃度の濃いｐ型半導体領域（正孔蓄積領域）を形成して構成される。その埋め込み型フォトダイオードの作製方法としては、ｐ型不純物となるＢやＢＦ2 をイオン注入し、アニールして、フォトダイオードを構成するｎ型半導体領域と絶縁膜との界面近傍にｐ型半導体領域を作製することが一般的である。
【0003】
ところが、従来のイオン注入法を用いて、埋め込み型フォトダイオードを形成する際には、不純物の活性化のために７００℃以上という高温の熱処理が必要不可欠である。このため、４００℃以下の低温プロセスではイオン注入によるｐ型半導体領域の形成は困難である。また、不純物の拡散を抑制するために、高温での長時間の活性化を避けたい場合も、イオン注入及びアニールを施すｐ型半導体領域の形成方法は好ましくない。
【0004】
一方、ＣＭＯＳイメージセンサでは、各画素が、フォトダイオードと読み出し、リセット、増幅などの各種のトランジスタを含んで形成される。フォトダイオードにより光電変換された信号は、当該トランジスタにより処理される。各画素の上部には多層の金属配線を含む配線層が形成される。配線層上には、フォトダイオードに入射する光の波長を規定するカラーフィルタや、フォトダイオードに光を集光するオンチップレンズが形成される。
【0005】
上記のＣＭＯＳイメージセンサでは、画素の上部の配線により光が遮られて、各画素の感度が低下する問題があった。また、これらの配線で反射された光が隣接画素に入射すると、混色等の原因となる。このため、フォトダイオードや各種のトランジスタを形成したシリコン基板の裏側を研磨することにより薄膜化し、基板裏面側から光を入射させて光電変換する裏面照射型の固体撮像装置が提案されている（特許文献１参照）。上述したように、暗電流を抑制するため、フォトダイオードの部位には浅く濃いｐ型半導体領域（正孔蓄積領域）が形成されているが、裏面照射型の固体撮像装置の場合、この正孔蓄積領域は、基板の表面側及び裏面側に形成される（特許文献１参照）。
【0006】
しかしながら、イオン注入による浅く濃いｐ型半導体領域の形成には限界がある。この

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ため、暗電流の抑制のためにｐ型半導体領域の不純物濃度をさらに上げようとすると、ｐ型半導体領域が深くなる。ｐ型半導体領域が深くなると、フォトダイオードのｐｎ接合が転送ゲートから離れるために、転送ゲートによる読出し能力が低下する虞れがある。

【0007】

【特許文献1】特開２００３－３１７８５号公報

【発明の開示】

【発明が解決しようとする課題】

【0008】

本発明は、上述の点に鑑み、その目的は、少なくとも界面準位に起因した暗電流の抑制を可能にした固体撮像装置およびその製造方法、並びにその固体撮像装置を備えたカメラを提供することにある。

【課題を解決するための手段】

【0009】

本発明に係る固体撮像装置は、基板の第１面側に配線層を有し、前記基板の第２面側から光を受光する固体撮像装置であって、前記基板に形成され、第１導電型領域を含む受光部と、前記基板の第１面上であって前記受光部に隣接して配置され、前記受光部に蓄積された信号電荷を転送する転送ゲートと、前記基板の第１面上であって前記受光部に重なって配置され、前記受光部の第１面近傍のポテンシャルを制御する制御ゲートとを有することを特徴とする。

【0010】

本発明に係る固体撮像装置の製造方法は、基板の第１面側に配線層を有し、前記基板の第２面側から光を受光する固体撮像装置の製造方法であって、基板に第１導電型領域を含む受光部を形成する工程と、前記基板の第１面上であって前記受光部に隣接する部位に、転送ゲートを形成する工程と、前記基板の第１面上であって前記受光部に重なる部位に、制御ゲートを形成する工程とを有することを特徴とする。

【0011】

本発明に係るカメラは、基板の第１面側に配線層を有し、前記基板の第２面側から光を受光する固体撮像装置と、前記固体撮像装置の前記第２面側に入射光を導く光学系と、前記固体撮像装置の出力信号を処理する信号処理回路とを有し、前記固体撮像装置は、前記基板に形成され、第１導電型領域を含む受光部と、前記基板の第１面上であって前記受光部に隣接して配置され、前記受光部に蓄積された信号電荷を転送する転送ゲートと、前記基板の第１面上であって前記受光部に重なって配置され、前記受光部の第１面近傍のポテンシャルを制御する制御ゲートとを有することを特徴とする。

【0012】

上記の本発明では、制御ゲートにより受光部の第１面近傍のポテンシャルを制御できることから、暗電流の発生が抑制される。また、受光部の第１導電型領域中であって、第１面近傍に信号電荷が蓄積されるため、転送ゲートによる信号電荷の読み出し能力が向上する。

【0013】

本発明に係る固体撮像装置は、受光部の受光面上に透明導電膜を有し、前記受光面と前記透明導電膜との間に存在する絶縁膜の膜厚が５０ｎｍ以下に設定されていることを特徴とする。

【0014】

本発明に係る固体撮像装置は、受光部の受光面上に透明導電膜を有し、前記受光面と前記透明導電膜との間に存在する２種類以上の膜からなる積層膜のうち前記受光面に接する膜は酸化シリコン膜であり、前記酸化シリコン膜の膜厚が５０ｎｍ以下に設定されていることを特徴とする。

【0015】

本発明に係る固体撮像装置の製造方法は、基板に形成された第１導電型領域を含む受光部の受光面上に膜厚５０ｎｍ以下の絶縁膜を形成する工程と、前記絶縁膜上に透明導電膜

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を形成する工程とを有することを特徴とする。
【0016】
本発明に係る固体撮像装置の製造方法は、基板に形成された第１導電型領域を含む受光部の受光面上に、該受光面に接する膜厚５０ｎｍ以下の酸化シリコン膜を含んで２種類以上の積層絶縁膜を形成する工程と、前記積層絶縁膜上に透明導電膜を形成する工程とを有することを特徴とする。
【0017】
本発明に係るカメラは、固体撮像装置の受光部に入射光を導く光学系と、前記固体撮像装置の出力信号を処理する信号処理回路とを備え、前記固体撮像装置は、受光部の受光面上に透明導電膜を有し、前記受光面と前記透明導電膜との間に存在する絶縁膜の膜厚が５０ｎｍ以下に設定されていることを特徴とする。
【0018】
本発明に係るカメラは、固体撮像装置の受光部に入射光を導く光学系と、前記固体撮像装置の出力信号を処理する信号処理回路とを備え、前記固体撮像装置は、受光部の受光面上に透明導電膜を有し、前記受光面と前記透明導電膜との間に存在する２種類以上の膜からなる積層膜のうち前記受光面に接する膜は酸化シリコン膜であり、前記酸化シリコン膜の膜厚が５０ｎｍ以下に設定されていることを特徴とする。
【0019】
上記の本発明では、透明導電膜により受光部の受光面のポテンシャルを制御できることから、暗電流に発生が抑制される。また、受光面と透明導電膜との間に存在する絶縁膜の膜厚、あるいは積層絶縁膜であれば、その受光面に接する酸化シリコン膜の膜厚、を５０ｎｍ以下に設定することにより、絶縁膜と透明導電膜とで反射防止膜が形成され、受光部への光吸収率が向上し、感度を向上することができる。
【0020】
本発明に係る固体撮像装置は、受光部の受光面上に負の固定電荷を有する膜が形成されていることを特徴とする。負の固定電荷を有する膜としては、好ましくは一部が結晶化した絶縁膜である。
【0021】
本発明に係るカメラは、固体撮像装置の受光部に入射光を導く光学系と、固体撮像装置の出力信号を処理する信号処理回路とを備え、前記固体撮像装置は、受光部の受光面上に負の固定電荷を有する膜が形成されていることを特徴とする。
【0022】
上記の本発明では、受光部の受光面上に負の固定電荷を有する膜が形成されているので、受光部の表面が正孔蓄積状態となり、界面準位に起因した暗電流の発生が抑制される。
【発明の効果】
【0023】
本発明によれば、少なくとも暗電流の抑制を図った固体撮像装置およびカメラを実現することができる。
【発明を実施するための最良の形態】
【0024】
以下に、本発明の実施の形態について、図面を参照して説明する。
【0025】
（第１実施の形態）
図１は、本実施形態に係る固体撮像装置の概略構成図である。
【0026】
固体撮像装置は、画素部１１と、周辺回路部とを有し、これらが同一の半導体基板上に搭載された構成となっている。本例では、周辺回路部として、垂直選択回路１２と、Ｓ／Ｈ（サンプル／ホールド）・ＣＤＳ（Correlated Double Sampling：相関二重サンプリング）回路１３と、水平選択回路１４と、タイミングジェネレータ（ＴＧ）１５と、ＡＧＣ（Automatic Gain Control）回路１６と、Ａ／Ｄ変換回路１７と、デジタルアンプ１８と

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を有する。

【0027】

画素部１１には、後述する単位画素が行列状に多数配置され、行単位でアドレス線等が、列単位で信号線等がそれぞれ設けている。

【0028】

垂直選択回路１２は、画素を行単位で順に選択し、各画素の信号を垂直信号線を通して画素列毎にＳ／Ｈ・ＣＤＳ回路１３に読み出す。Ｓ／Ｈ・ＣＤＳ回路１３は、各画素列から読み出された画素信号に対し、ＣＤＳ等の信号処理を行う。

【0029】

水平選択回路１４は、Ｓ／Ｈ・ＣＤＳ回路１３に保持されている画素信号を順に取り出し、ＡＧＣ回路１６に出力する。ＡＧＣ回路１６は、水平選択回路１４から入力した信号を適当なゲインで増幅し、Ａ／Ｄ変換回路１７に出力する。

【0030】

Ａ／Ｄ変換回路１７は、ＡＧＣ回路１６から入力したアナログ信号をデジタル信号に変換し、デジタルアンプ１８に出力する。デジタルアンプ１８は、Ａ／Ｄ変換回路１７から入力したデジタル信号を適当に増幅して、パッド（端子）より出力する。

【0031】

垂直選択回路１２、Ｓ／Ｈ・ＣＤＳ回路１３、水平選択回路１４、ＡＧＣ回路１６、Ａ／Ｄ変換回路１７およびデジタルアンプ１８の各動作は、タイミングジェネレータ１５から出力される各種のタイミング信号に基づいて行われる。

【0032】

図２は、画素部１１の単位画素の回路構成の一例を示す図である。

【0033】

単位画素は、光電変換素子として例えばフォトダイオード２１を有し、この１個のフォトダイオード２１に対して、転送トランジスタ２２、増幅トランジスタ２３、アドレストランジスタ２４、リセットトランジスタ２５の４つのトランジスタを能動素子として有する。

【0034】

フォトダイオード２１は、入射光をその光量に応じた量の電荷（ここでは電子）に光電変換する。転送トランジスタ２２は、フォトダイオード２１とフローティングディフュージョンＦＤとの間に接続され、駆動配線２６を通じてそのゲート（転送ゲート）に駆動信号が与えられることで、フォトダイオード２１で光電変換された電子をフローティングディフュージョンＦＤに転送する。

【0035】

フローティングディフュージョンＦＤには、増幅トランジスタ２３のゲートが接続されている。増幅トランジスタ２３は、アドレストランジスタ２４を介して垂直信号線２７に接続され、画素部外の定電流源Ｉとソースフォロアを構成している。そして、駆動配線２８を通してアドレス信号がアドレストランジスタ２４のゲートに与えられ、当該アドレストランジスタ２４がオンすると、増幅トランジスタ２３はフローティングディフュージョンＦＤの電位を増幅してその電位に応じた電圧を垂直信号線２７に出力する。垂直信号線２７を通じて、各画素から出力された電圧はＳ／Ｈ・ＣＤＳ回路１３に出力される。

【0036】

リセットトランジスタ２５は、電源ＶｄｄとフローティングディフュージョンＦＤとの間に接続され、駆動配線２９を通してそのゲートにリセット信号が与えられることで、フローティングディフュージョンＦＤの電位を電源Ｖｄｄの電位にリセットする。これらの動作は、転送トランジスタ２２、アドレストランジスタ２４およびリセットトランジスタ２５の各ゲートが行単位で接続されていることから、１行分の各画素について同時に行われる。

【0037】

図３は、固体撮像装置の画素部および周辺回路部における概略断面図である。本実施形

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態に係る固体撮像装置は、配線層３８が形成された第１面側とは反対側の第２面側から光を受光する。

【0038】

基板３０は、例えばｎ型のシリコン基板からなり、本発明の基板に相当する。基板３０には、単位画素を構成する複数の受光部３１が形成されている。受光部３１は、図２に示すフォトダイオード２１に相当する。受光部３１は、基板３０中のｐｎ接合により構成される。基板３０は、裏面から光を入射し得るように、シリコンウェハを薄膜化することにより形成される。基板３０の厚さは、固体撮像装置の種類にもよるが、可視光用の場合には２～６μｍであり、近赤外線用では６～１０μｍとなる。

【0039】

基板３０の第２面側（裏面側、光入射側）には、酸化シリコンからなる絶縁膜３２を介して、遮光膜３３が形成されている。遮光膜３３には、受光部３１の部位に開口部３３ａが形成されている。遮光膜３３上には、窒化シリコンからなる保護膜３４が形成されている。

【0040】

保護膜３４上には、所望の波長領域の光のみを通過させるカラーフィルタ３５が形成されている。また、カラーフィルタ３５上には、入射光を受光部３１へ集光させるマイクロレンズ３６が形成されている。

【0041】

基板３０の第１面側には、各種のトランジスタが形成される。図示はしないが、基板３０の画素部には、図２に示すトランジスタ２２～２５が形成される。また、図示はしないが、基板３０の周辺回路部にはｐウェルおよびｎウェルが形成されており、これらウェルにＣＭＯＳ回路が形成されている。

【0042】

基板３０の第１面（表面）上には、多層の金属配線を含む配線層３８が形成されている。配線層３８上には、図示しない接着層を介して支持基板３９が設けられている。支持基板３９は、基板３０の強度を補強するために設けられる。支持基板３９は、例えばシリコン基板からなる。

【0043】

図４は、基板３０の画素部の要部断面図である。

【0044】

受光部３１の部位には、基板３０にｎ型の電荷蓄積領域（第１導電型領域）４１が形成されている。電荷が蓄積する部位を第１面側に近づけるため、第１面側にいくに従って不純物濃度が高くなるように、電荷蓄積領域４１が形成されていることが好ましい。また、入射光を効率良く取り込むため、第２面側にいくに従って面積が大きくなるように、電荷蓄積領域４１を形成してもよい。

【0045】

基板３０中であって、電荷蓄積領域４１の周囲には、ｐ型ウェル４２が形成されている。基板３０の第２面側には、浅いｐ型の正孔蓄積領域（第２導電型領域）４３が画素部の全面に形成されている。基板３０の第１面側であって、受光部３１の部位には、浅いｐ型の正孔蓄積領域（第２導電型領域）４４が形成されている。電荷蓄積領域４１に対して第１面側および第２面側に正孔蓄積領域４３，４４が形成されていることにより、埋め込みフォトダイオードからなる受光部３１が構成される。

【0046】

基板３０の第１面側には、酸化シリコンからなる素子分離絶縁膜４０が形成されている。基板３０の第１面側には、ｎ型のフローティングディフュージョン（ＦＤ）４５が形成されている。フローティングディフュージョン４５と電荷蓄積領域４１との間には、ｐ型領域４６が形成されており、両者は電気的に分離されている。

【0047】

基板３０の第１面上には、図示しないゲート絶縁膜を介して、転送トランジスタ２２の

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転送ゲート５１が形成されている。転送ゲート５１は、受光部３１に隣接して配置されており、ｐ型領域４６上に形成されている。転送ゲート５１は、例えばポリシリコンからなる。

【0048】

基板３０の第１面上には、図示しないゲート絶縁膜を介して、制御ゲート５２が形成されている。制御ゲート５２は、受光部３１の全面に重なって配置されている。制御ゲート５２は、例えばポリシリコンからなる。加工性および抵抗の観点から、制御ゲート５２の膜厚は、転送ゲート５１と同程度とすることが好ましい。光は第２面側から入射するため、受光部３１の第１面側に制御ゲート５２が存在しても、光を遮ることはない。

【0049】

図示はしないが、画素内の転送トランジスタ２２以外のトランジスタ（図２の増幅トランジスタ２３、アドレストランジスタ２４、リセットトランジスタ２５）は、基板３０の第１面側におけるｐ型ウェル４２上に形成されている。

【0050】

次に、本実施形態に係る固体撮像装置の動作について、図４および図５を参照して説明する。図５は、固体撮像装置の動作におけるバイアス例を示す図である。

【0051】

電荷蓄積期間では、図中矢印に示す向きから入射した光は、基板３０の受光部（フォトダイオード）３１により光電変換されて、入射光量に応じた信号電荷が発生する。信号電荷は、電荷蓄積領域４１中をドリフトし、電荷蓄積領域４１中であって正孔蓄積領域４４付近に蓄積される。電荷蓄積期間においては、転送ゲート５１には負電圧が印加されており、転送トランジスタ２２はオフ状態となっている。また、制御ゲート５２には、負電圧が印加されている。このため、正孔が基板３０の界面（第１面）付近に蓄積され、暗電流が低減される。

【0052】

制御ゲート５２に印加する負電圧は、制御ゲート５２下の不純物濃度、ゲート酸化膜厚等によって異なる。例えば０．２５μｍ世代のプロセスで、１×１０１６／ｃｍ３のｐ型不純物濃度をもつ正孔蓄積領域４４を形成した場合には、－１Ｖ程度を印加すれば、暗電流の発生は十分抑制できる。

【0053】

読み出し時には、転送ゲート５１に正電圧が印加され、転送トランジスタ２２がオン状態となる。この結果、受光部３１に蓄積された信号電荷は、フローティングディフュージョン４５に転送される。正電圧は、例えば、電源電圧（３．３Ｖあるいは２．７Ｖ）と等しい。

【0054】

読み出し時において、基本的に制御ゲート５２には、蓄積時と同じ負電圧（例えば－１Ｖ）が印加される。ただし、読み出し時において、制御ゲート５２に、一時的に＋１Ｖ程度の正電圧を印加してもよい。この場合には、蓄積された信号電荷が第１面側に近づくため、転送ゲート５１による読み出し能力を向上させることができる。なお、読み出しに要する期間は、蓄積期間に比べて非常に短いため、制御ゲート５２に正電圧を印加することにより発生する暗電流は少ない。

【0055】

転送された信号電荷の量に従って、フローティングディフュージョン４５の電位が変化する。フローティングディフュージョン４５の電位は、増幅トランジスタ２３により増幅され、その電位に応じた電圧が垂直信号線２７に出力される（図２参照）。

【0056】

リセット時には、リセットトランジスタ２５のゲートに正電圧が印加されて、フローティングディフュージョン４５は電源Ｖｄｄの電圧にリセットされる。このとき、転送ゲート５１に負電圧が印加されており、転送トランジスタ２２はオフ状態となっている。また、制御ゲート５２には、負電圧が印加されている。

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【0057】
上記した信号電荷の蓄積動作、読み出し動作、リセット動作が繰り返し行われる。
【0058】
次に、上記の固体撮像装置の製造方法について説明する。本実施形態では、転送ゲート５１と制御ゲート５２を同時に形成する例について説明する。
【0059】
図６（ａ）に示すように、基板３０に、ＳＴＩ（Shallow Trench Isolation）技術により素子分離絶縁膜４０を形成した後、イオン注入法により、ｎ型の電荷蓄積領域４１、ｐ型ウェル４２、ｐ型の正孔蓄積領域４４、ｐ型領域４６を形成する。なお、各領域の形成順序に限定はない。
【0060】
次に、図６（ｂ）に示すように、熱酸化法により、基板３０上に、酸化シリコンからなるゲート絶縁膜６０を形成する。続いて、ゲート絶縁膜６０上に、ＣＶＤ法によりポリシリコンからなる電極層５０を形成する。ポリシリコンの膜厚は１００ｎｍ～３００ｎｍであり、ポリシリコンへの不純物の導入は成膜時に行う。
【0061】
次に、図７（ａ）に示すように、レジストマスクを用いて電極層５０をエッチングして、転送ゲート５１および制御ゲート５２を形成する。このとき、画素部の他のトランジスタ（図２参照）のゲートも同時に形成される。
【0062】
次に、図７（ｂ）に示すように、全面に酸化シリコンあるいは窒化シリコンを堆積させて、転送ゲート５１および制御ゲート５２間のギャップに絶縁膜６１を埋め込む。
【0063】
以上により、転送ゲート５１および制御ゲート５２が形成される。ゲート形成後のプロセスについて、図３を参照して説明する。基板３０の第１面側に、絶縁膜の形成および配線の形成を繰り返すことにより、配線層３８を形成する。その後、配線層３８上に支持基板３９を貼り付ける。
【0064】
続いて、基板３０の裏面（第２面側）をＣＭＰにより研磨して、基板３０を薄膜化する。続いて、イオン注入および活性化アニールを施し、基板３０の第２面にｐ型の正孔蓄積領域４３（図４参照）を形成する。なお前記活性化アニールは、配線層の形成後に行うため、配線の耐熱性を超えない必要がある。それを実現するためには、配線層まで熱の影響が届かないレーザーアニールを用いることが好適である。
【0065】
その後、基板３０上に、ＣＶＤ法により酸化シリコンからなる絶縁膜３２を形成し、絶縁膜３２上に遮光膜３３をパターン加工する。遮光膜３３上に、ＣＶＤ法により窒化シリコンからなる保護膜３４を形成し、カラーフィルタ３５およびマイクロレンズ３６を形成する。
【0066】
以上により、本実施形態に係る裏面照射型の固体撮像装置が製造される。
【0067】
転送ゲート５１と制御ゲート５２を単層で形成する他の例について、図８および図９を参照して説明する。図８，９では、基板構造を省略している。
【0068】
まず、先と同様にして、基板３０に、ＳＴＩ（Shallow Trench Isolation）技術により素子分離絶縁膜４０を形成した後、イオン注入法により、ｎ型の電荷蓄積領域４１、ｐ型ウェル４２、ｐ型の正孔蓄積領域４４、ｐ型領域４６を形成する（図６（ａ）参照）。なお、各領域の形成順序に限定はない。
【0069】
次に、図８（ａ）に示すように、基板３０上に熱酸化法により酸化シリコンからなるゲ

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ート絶縁膜６０を形成し、ゲート絶縁膜６０上にＣＶＤ法により、ポリシリコンからなる電極層５０を形成する。ポリシリコンの膜厚は１００ｎｍ～３００ｎｍであり、ポリシリコンへの不純物の導入は成膜時に行う。続いて、電極層５０上に、ＣＶＤ法により酸化シリコン膜６２ａおよび窒化シリコン膜６２ｂを堆積して、酸化シリコン膜６２ａおよび窒化シリコン膜６２ｂからなるハードマスク６２を形成する。

【0070】

次に、図８（ｂ）に示すように、リソグラフィ技術により形成したレジストマスクを用いて、ハードマスク６２をパターニングする。これにより、ハードマスク６２には幅Ｗ１の開口が形成される。幅Ｗ１の最小値は、リソグラフィの解像限界で決まる。

【0071】

次に、図８（ｃ）に示すように、ハードマスク６２の開口の側壁にサイドウォール絶縁膜６３を形成する。サイドウォール絶縁膜６３は、ハードマスク６２の開口内を含む全面に、ＣＶＤ法により酸化シリコン膜を堆積し、当該酸化シリコン膜をエッチバックすることにより形成される。サイドウォール絶縁膜６３により、リソグラフィの解像限界で決まる幅Ｗ１よりも狭い幅Ｗ２の開口部が得られる。

【0072】

次に、図９（ａ）に示すように、ハードマスク６２およびサイドウォール絶縁膜６３を用いて電極層５０をドライエッチングして、転送ゲート５１および制御ゲート５２を形成する。制御ゲート５２および制御ゲート５２のギャップは、幅Ｗ２にほぼ等しい。必要に応じて、転送ゲート５１と制御ゲート５２の間における基板３０にイオン注入を行う。

【0073】

次に、図９（ｂ）に示すように、転送ゲート５１および制御ゲート５２のギャップ部を含む全面に、ＣＶＤ法により酸化シリコン膜６４ａおよび窒化シリコン膜６４ｂを順に堆積して、埋め込み絶縁膜６４を形成する。

【0074】

次に、図９（ｃ）に示すように、ハードマスク６２上の埋め込み絶縁膜６４をエッチバックして、転送ゲート５１および制御ゲート５２のギャップ部のみに埋め込み絶縁膜６４を残す。

【0075】

以降の工程としては、先に記載した通りである。なお、本実施形態では、転送ゲート５１および制御ゲート５２を単層で形成する方法を例に説明したが、その形成方法に限定はない。例えば、制御ゲート５２を形成後、酸化により制御ゲート５２の表面に酸化シリコン膜を形成し、その後転送ゲート５１を形成してもよい。あるいは、転送ゲート５１を先に形成し、酸化により転送ゲート５１の側壁に酸化シリコン膜を形成した後に、制御ゲート５２を形成してもよい。転送ゲート５１を先に形成する場合には、転送ゲート５１をイオン注入マスクとして、正孔蓄積領域４４を形成してもよい。

【0076】

図１０は、上記の固体撮像装置が用いられるカメラの概略構成図である。

【0077】

カメラ１００は、上記した固体撮像装置１０１と、光学系１０２と、信号処理回路１０３とを有する。本発明のカメラは、固体撮像装置１０１、光学系１０２および信号処理回路１０３がモジュール化したカメラモジュールの形態を含む。

【0078】

光学系１０２は、被写体からの像光（入射光）を固体撮像装置１０１の撮像面上に結像させる。これにより、固体撮像装置１０１の受光部３１において、入射光は入射光量に応じた信号電荷に変換され、受光部３１において、一定期間当該信号電荷が蓄積される。

【0079】

信号処理回路１０３は、固体撮像装置１０１の出力信号に対して種々の信号処理を施して映像信号として出力する。

【0080】

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次に、上記の本実施形態に係る固体撮像装置およびその製造方法、並びにカメラの効果について説明する。

【0081】

本実施形態に係る固体撮像装置では、基板３０の第１面上に、受光部３１に重なって制御ゲート５２が配置されている。この制御ゲート５２に負電圧を印加することにより、基板３０の第１面付近に正孔が蓄積され、暗電流が低減される。

【0082】

この結果、正孔蓄積領域４４のｐ型不純物濃度を下げても暗電流を抑制できることから、受光部３１のｐｎ接合を第１面側に近づけることができるため、転送ゲート５１の読み出し能力を向上させることができる。読み出し可能な信号電荷量を増加させることができることから、ダイナミックレンジを向上させることができる。

【0083】

従来、暗電流を抑制するためには、正孔蓄積領域４４のｐ型不純物濃度を１×１０１８／ｃｍ３程度まで上げる必要があったが、本実施形態では、正孔蓄積領域４４のｐ型不純物濃度を１×１０１６／ｃｍ３程度まで下げることができる。なお、正孔蓄積領域４４の不純物濃度をさらに下げたい場合には、制御ゲート５２に印加すべき負電圧をより大きくすればよい。

【0084】

上記の本実施形態に係る固体撮像装置の製造方法によれば、転送ゲート５１および制御ゲート５２を備えた固体撮像装置を製造することができる。特に転送ゲート５１と制御ゲート５２を同時に形成する場合には、製造工程の増加を抑制しつつ、上記した固体撮像装置を製造することができる。

【0085】

上記の固体撮像装置を備えることにより、暗電流の抑制およびダイナミックレンジの拡大を図ったカメラを実現することができる。

【0086】

（第２実施の形態）

図１１は、第２実施形態に係る固体撮像装置における、基板３０の画素部の要部断面図である。なお、第１実施形態と同一の構成要素には、同じ符号を付してあり、その説明は省略する。

【0087】

基板３０の第１面上には、図示しないゲート絶縁膜を介して、２つの制御ゲート５２－１，５２－２が形成されている。転送ゲート５１側から第１制御ゲート５２－１、第２制御ゲート５２－２の順に配置されている。制御ゲート５２－１，５２－２は、受光部３１に重なって配置されている。制御ゲート５２－１，５２－２は、例えばポリシリコンからなる。加工性および抵抗の観点から、制御ゲート５２－１，５２－２の膜厚は、転送ゲート５１と同程度とすることが好ましい。光は第２面側から入射するため、受光部３１の第１面側に制御ゲート５２－１，５２－２が存在しても、光を遮ることはない。なお、受光部３１上に３つ以上の制御ゲートが配置されていてもよい。

【0088】

上記の固体撮像装置は、第１実施形態と同様にして作製される。例えば、第１実施形態と同様に、転送ゲート５１、制御ゲート５２－１，５２－２を同時に形成してもよい。あるいは、第１制御ゲート５２－１を形成後、酸化により第１制御ゲート５２－１の表面に酸化シリコン膜を形成し、その後、第１制御ゲート５２－１の両側に転送ゲート５１および第２制御ゲート５２－２を形成してもよい。

【0089】

次に、本実施形態に係る固体撮像装置の動作について、図１１および図１２を参照して説明する。図１２は、固体撮像装置の動作におけるバイアス例を示す図である。

【0090】

電荷蓄積期間では、図中矢印に示す向きから入射した光は、基板３０の受光部（フォト

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ダイオード）３１により光電変換されて、入射光量に応じた信号電荷が発生する。信号電荷は、電荷蓄積領域４１中をドリフトし、電荷蓄積領域４１中であって正孔蓄積領域４４付近に蓄積される。電荷蓄積期間においては、転送ゲート５１には負電圧が印加されており、転送トランジスタ２２はオフ状態となっている。また、第１制御ゲート５２－１および第２制御ゲート５２－２には、負電圧が印加されている。このため、正孔が基板３０の界面（第１面）付近に蓄積され、暗電流が低減される。

【0091】

第１制御ゲート５２－１および第２制御ゲート５２－２に印加する負電圧は、制御ゲート５２下の不純物濃度、ゲート酸化膜厚等によって異なる。例えば０．２５μｍ世代のプロセスで、１×１０１６／ｃｍ３のｐ型不純物濃度をもつ正孔蓄積領域４４を形成した場合には、－１Ｖ程度のバイアスがあれば、暗電流の発生は十分抑制できる。信号電荷は、電荷蓄積領域４１中であって正孔蓄積領域４４付近に蓄積される。

【0092】

読み出し時（読み出し１）には、まず、第１制御ゲート５２－１に正電圧（例えば、＋１Ｖ程度）が印加される。これにより、ＣＣＤと同様の原理で、電荷蓄積領域４１中の信号電荷は、第１制御ゲート５２－１下に集まる。

【0093】

次に、転送ゲート５１に正電圧が印加され、第１制御ゲート５２－１に負電圧が印加される（読み出し２参照）。これにより、転送トランジスタ２２がオン状態となり、第１制御ゲート５２－１下に集められた信号電荷は、フローティングディフュージョン４５に転送される。転送ゲート５１に印加する正電圧は、例えば、電源電圧（３．３Ｖあるいは２．７Ｖ）に等しい。このとき、第１制御ゲート５２－１に負電圧を印加することにより、基板３０に水平方向に電界がかかるため、信号電荷はフローティングディフュージョン４５に効率的に転送される。

【0094】

転送された信号電荷の量に従って、フローティングディフュージョン４５の電位が変化する。フローティングディフュージョン４５の電位は、増幅トランジスタ２３により増幅され、その電位に応じた電圧が垂直信号線２７に出力される（図２参照）。

【0095】

リセット時には、リセットトランジスタ２５のゲートに正電圧が印加されて、フローティングディフュージョン４５は電源Ｖｄｄの電圧にリセットされる。このとき、転送ゲート５１に負電圧が印加されており、転送トランジスタ２２はオフ状態となっている。また、制御ゲート５２－１，５２－２には、負電圧が印加されている。

【0096】

上記の信号電荷の蓄積動作、読み出し動作、リセット動作が繰り返し行われる。

【0097】

本実施形態では、受光部３１上に複数の制御ゲート５２－１，５２－２を設け、第１制御ゲート５２－１と転送ゲート５１を順次オン／オフしていくことにより、基板３０に水平方向に電界を生じさせて、電荷を効率的に転送することができる。

【0098】

従来、電荷を効率的に読み出す観点から、基板３０に水平方向に電界を生じさせる場合には、電荷蓄積領域４１の不純物濃度を水平方向に変化させる必要があった。この場合には、電荷蓄積領域４１の不純物濃度が薄い領域において、電位井戸が浅くなるため、蓄積電荷量が減少する。この結果、ダイナミックレンジの減少に繋がる。本実施形態の場合には、水平方向に濃度勾配を設ける必要がなくなるため、ダイナミックレンジの減少はない。本実施形態は、特に画素サイズが大きい固体撮像装置に有効である。

【0099】

上記の固体撮像装置の製造方法によれば、転送ゲート５１および制御ゲート５２－１，５２－２を備えた固体撮像装置を製造することができる。特に転送ゲート５１と制御ゲート５２－１，５２－２を同時に形成する場合には、製造工程の増加を抑制しつつ、上記し

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た固体撮像装置を製造することができる。

【0100】

上記の固体撮像装置を備えることにより、暗電流の抑制およびダイナミックレンジの拡大を図ったカメラを実現することができる。

【0101】

（第３実施形態）

図１３は、第３実施形態に係る固体撮像装置における、基板３０の画素部の要部断面図である。なお、第１実施形態と同一の構成要素には、同じ符号を付してあり、その説明は省略する。

【0102】

基板３０の第１面上には、図示しないゲート絶縁膜を介して、制御ゲート５２が形成されている。本実施形態では、制御ゲート５２は、受光部３１の一部のみを覆っている。制御ゲート５２下には正孔蓄積領域４４は設けられていない。この結果、転送ゲート５１側から制御ゲート５２のみが配置された領域と、正孔蓄積領域４４のみが配置された領域が形成されている。ただし、正孔蓄積領域４４は受光部３１の全面に形成されていてもよい。また、制御ゲート５２と正孔蓄積領域４４の配置を逆にしてもよい。

【0103】

上記の固体撮像装置は、第１実施形態と同様にして作製される。例えば、第１実施形態と同様に、転送ゲート５１および制御ゲート５２を同時に形成してもよい。あるいは、制御ゲート５２を形成後、酸化により制御ゲート５２の表面に酸化シリコン膜を形成し、その後転送ゲート５１を形成してもよい。あるいは、転送ゲート５１を先に形成し、酸化により転送ゲート５１の側壁に酸化シリコン膜を形成した後に、制御ゲート５２を形成してもよい。正孔蓄積領域４４は、転送ゲート５１および制御ゲート５２の前に形成してもよく、あるいは転送ゲート５１および制御ゲート５２をマスクとしたイオン注入により形成してもよい。

【0104】

次に、本実施形態に係る固体撮像装置の動作について、図１３を参照して説明する。固体撮像装置の動作におけるバイアス例は第１実施形態と同様である（図５参照）。

【0105】

電荷蓄積期間では、図中矢印に示す向きから入射した光は、基板３０の受光部（フォトダイオード）３１により光電変換されて、入射光量に応じた信号電荷が発生する。信号電荷は、電荷蓄積領域４１中をドリフトし、電荷蓄積領域４１の第１面側に蓄積される。電荷蓄積期間においては、転送ゲート５１には負電圧が印加されており、転送トランジスタ２２はオフ状態となっている。また、制御ゲート５２には、負電圧が印加されている。正孔蓄積領域４４および制御ゲート５２により、受光部３１の第１面付近に正孔が蓄積されるため、暗電流が低減される。

【0106】

読み出し時には、転送ゲート５１に正電圧が印加され、転送トランジスタ２２がオン状態となる。この結果、受光部３１に蓄積された信号電荷は、フローティングディフュージョン４５に転送される。転送ゲート５１に印加される正電圧は、例えば、電源電圧（３．３Ｖあるいは２．７Ｖ）に等しい。

【0107】

読み出し時において、制御ゲート５２には、基本的に蓄積時と同じ負電圧（例えば－１Ｖ）が印加される。ただし、読み出し時において、制御ゲート５２に、一時的に＋１Ｖ程度の正電圧を印加してもよい。この場合には、信号電荷が第１面側に近づくため、転送ゲート５１による読み出し能力を向上させることができる。なお、読み出しに要する期間は、蓄積期間に比べて非常に短いため、制御ゲート５２に正電圧を印加することにより発生する暗電流は少ない。

【0108】

転送された信号電荷の量に従って、フローティングディフュージョン４５の電位が変化

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する。フローティングディフュージョン４５の電位は、増幅トランジスタ２３により増幅され、その電位に応じた電圧が垂直信号線２７に出力される（図２参照）。

【0109】

リセット時には、リセットトランジスタ２５のゲートに正電圧が印加されて、フローティングディフュージョン４５は電源Ｖｄｄの電位にリセットされる。このとき、転送ゲート５１に負電圧が印加されており、転送トランジスタ２２はオフ状態となっている。また、制御ゲート５２には、負電圧が印加されている。

【0110】

上記した信号電荷の蓄積動作、読み出し動作、リセット動作が繰り返し行われる。

【0111】

上記の本実施形態に係る固体撮像装置によれば、受光部３１の一部にのみ重なるように制御ゲート５２を設けた場合であっても、第１実施形態と同様の効果、すなわち、暗電流の低減と読み出し能力の向上を図ることができる。また、制御ゲート５２を設けることにより、受光部３１の一部にのみ正孔蓄積領域４４を形成することができる。

【0112】

受光部３１の一部にのみ正孔蓄積領域４４を形成する場合には、転送ゲート５１，５２をマスクとしたイオン注入により、制御ゲート５２に対してセルフアラインで正孔蓄積領域４４を形成することができる。なお、受光部３１の全面に正孔蓄積領域４４を形成してもよい。

【0113】

上記の固体撮像装置を備えることにより、暗電流の抑制およびダイナミックレンジの拡大を図ったカメラを実現することができる。

【0114】

上述したように、第１乃至第３実施の形態によれば、暗電流の抑制と、信号電荷の読み出し能力向上を図った固体撮像装置およびカメラを実現することができる。

【0115】

（第４実施の形態）

図１４は、第４実施の形態に係る固体撮像装置における、画素部の要部断面図である。本実施の形態も裏面照射型の固体撮像装置であり、第１実施の形態と同一の構成要素には、同じ符号を付してあり、その説明は省略する。

【0116】

本実施の形態に係る固体撮像装置は、光電変換部となるフォトダイオードで構成された受光部３１の受光面上、すなわちフォトダイオードを構成する第１導電型領域（ｎ型の電荷蓄積領域）４１の受光面上に単層の絶縁膜７１を介して透明導電膜７４を形成し、この透明導電膜７４に負電圧を印加するように構成される。この透明導電膜７４は、受光部表面のポテンシャルを制御する制御ゲートとなる。透明導電膜７４上には絶縁膜の例えば酸化シリコン膜７５を介して平坦化膜７６が形成され、平坦化膜７６上にカラーフィルタ３５、その上にオンチップマイクロレンズ３６が形成される。透明導電膜７４には、酸化シリコン膜７５を貫通して配線（遮光膜を兼ねる）７７が接続され、この配線７７が撮像領域８１（画素部１１に相当）から周辺回路領域８２上に延長して形成される。

【0117】

そして、本実施の形態においては、透明導電膜７４を有する構造がフォトダイオードでの光の吸収率で優位性を得るために、透明導電膜７４下の絶縁膜７１、本例では酸化シリコン膜の膜厚ｄ１を５０ｎｍ以下に設定する。好ましくは、絶縁膜７１である酸化シリコン膜の膜厚ｄ１を５０ｎｍ以下にし、その酸化シリコン膜の膜厚ｄ１に応じて透明導電膜７４の膜厚ｄ２を最適化する。絶縁膜７１としては、酸化シリコン膜の他、酸窒化シリコン膜とすることもできる。

【0118】

透明導電膜７４としてインジウムと錫を含む酸化膜、すなわちＩＴＯ（酸化インジウム錫）膜を用いた場合には、透明導電膜（ＩＴＯ膜）７４の屈折率が２．０程度、絶縁膜（

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酸化シリコン膜）７１の屈折率が１．４５程度であり、透明導電膜（ＩＴＯ膜）７４と絶縁膜（酸化シリコン膜）７１で反射防止膜が構成される。透明導電膜７４としては、ＩＴＯ膜の他、亜鉛を含む酸化膜すなわち酸化亜鉛膜とすることもできる。

【0119】

絶縁膜７１の膜厚ｄ１としては、５０ｎｍ以下、１．０ｎｍ～５０ｎｍの範囲、好ましくは３０ｎｍ以下、より好ましくは１５ｎｍ～３０ｎｍとすることができる。絶縁膜７１の膜厚ｄ１は、薄ければ薄い程、酸化シリコン膜（膜厚ｄ１）とＩＴＯ膜（膜厚ｄ２）を最適化した際の透過率を向上させることが出来るため、固体撮像装置の感度が良くなる。５０ｎｍを超えると、反射成分が大きくなり、１．０ｎｍより薄いと絶縁性が得に難くなる。

【0120】

第４実施の形態によれば、フォトダイオードで構成された受光部３１の受光面上に単層の絶縁膜７１を介して透明導電膜７４を形成し、この透明導電膜７４に負電圧を印加することにより、フォトダイオード表面がホールアキュミレーション状態（正孔蓄積状態）になり、界面準位に起因した暗電流成分を抑制することができる。しかも、透明導電膜７４下の該透明導電膜７４より屈折率の低い絶縁膜７１の膜厚ｄ１を５０ｎｍ以下にすることにより、透明導電膜７４と絶縁膜７１により反射防止膜が形成され、透明導電膜７４を用いても感度低下を伴うことない。従って、本実施の形態の固体撮像装置では、低暗電流かつ高感度を実現できる。

【0121】

因みに、フォトダイオード表面に絶縁膜を介して透明導電膜を形成し、その透明導電膜に負電圧を印加することで、フォトダイオード表面をホールアキュミレーション状態にして、埋め込み型フォトダイオードと同様に界面の暗電流を抑制出来るが、不利な点も生じる。すなわち、透明導電膜を形成することにより、フォトダイオード上部に積層される層構造が増加し、上層膜の界面での反射光成分が増加、または透明導電膜例えばＩＴＯ膜における短波長成分の光吸収の増加が発生する。これらの光学的な損失のために暗電流の低下は可能であるが、それと同時に感度の点で不利になる可能性がある。

【0122】

これに対して、本実施の形態のように、透明導電膜７４下の酸化シリコン膜あるいは酸窒化シリコン膜などの単層絶縁膜７１の膜厚ｄ１を５０ｎｍ以下にし、その膜厚ｄ１に応じた透明導電膜７４の膜厚ｄ２を最適化することで、界面の暗電流の抑制と感度の向上を両立させることができる。

【0123】

次に、図１５～図１９を用いて具体的に透明導電膜７４下の絶縁膜７１、本例では酸化シリコン膜の膜厚が５０ｎｍ以下としたときに、フォトダイオードへの光吸収率で優位になることを実証する。

【0124】

絶縁膜（酸化シリコン膜）７１上に透明導電膜（ＩＴＯ膜）７４を形成した図１４のデバイス構造を考える。図１５に、透明導電膜（ＩＴＯ膜）７４の膜厚ｄ２、及び透明導電膜（ＩＴＯ膜）７４下の絶縁膜（酸化シリコン膜）７１の膜厚ｄ１をパラメータとして、フォトダイオードに吸収される光の吸収率をシミュレーションより求めたデータを示す。

【0125】

図１５では、フォトダイオードの深さを４μｍと仮定し、横軸を波長４５０ｎｍの光のフォトダイオードへの吸収率（＝青の吸収率を想定）をとり、縦軸に波長５５０ｎｍの光のフォトダイオードへの吸収率（＝緑の吸収率を想定）をとり、両者の吸収率をプロットしている。同図中の凡例のＯｘとは、透明導電膜（ＩＴＯ膜）７４下の絶縁膜である酸化シリコン膜厚を示し、各酸化シリコン膜厚に対して、図中で結ばれた曲線（細線）はＩＴＯ膜厚を１０ｎｍ刻みで０ｎｍ～１００ｎｍまで振っている。凡例の“ＩＴＯなし”の曲線は、ＩＴＯ膜下の酸化シリコン膜のみを膜厚０ｎｍ～２００ｎｍまで振り、ＩＴＯ膜を形成していない場合のデータを表している。

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【0126】
なお、透明導電膜（ＩＴＯ膜）上部の膜は固定しており、透明導電膜（ＩＴＯ膜）７４上部の絶縁膜（酸化シリコン膜）７５は１００ｎｍ厚、平坦化膜７６はシリコン（Ｓｉ）、酸素（Ｏ）、炭素（Ｃ）を成分とした平坦化膜を１μｍ厚として屈折率は１．５の材料を想定している。また、カラーフィルタ３５は屈折率１．６～１．７程度の材料を想定している。
【0127】
図１５に示すように、青光と緑光の吸収率を両立するためには、透明導電膜（ＩＴＯ膜）７４下の絶縁膜厚（酸化シリコン膜厚）ｄ１に対して、最適なＩＴＯ膜厚ｄ２が存在することが分かる。また、ＩＴＯ膜の最適膜厚を設定しても、青光及び緑光の吸収率の最大値は、ＩＴＯ膜下の酸化シリコン膜厚ｄ１により律速されていることが確認できる。フォトダイオードでの光の吸収率としては、実線枠内（青光及び緑光のフォトダイオードでの吸収率が共に約７３％以上得られる範囲）に入ることが望まれる。より好ましくは青光、緑光共に吸収率が８０％以上の範囲に入ることが望ましい。ＩＴＯ膜の無い酸化シリコン膜のみをベースとした構造に対して、ＩＴＯ膜を用いた構造は、フォトダイオードでの光の吸収率で優位性を持つためには、少なくともＩＴＯ膜下の酸化シリコン膜厚ｄ１が５０ｎｍ以下であることが必要である。なお、好ましくは、ＩＴＯ膜を用いた構造が、ＩＴＯ膜を用いない構造に対してフォトダイオードへの光の吸収率で優位性を持つためには３０ｎｍ以下である。
【0128】
図１６及び図１７に、ＩＴＯ膜下の酸化シリコン膜厚ｄ１とＩＴＯ膜厚ｄ２を変化させた際の、青光及び緑光のフォトダイオードでの吸収率を強度グラフで表したデータを示す。図１６は波長４５０ｎｍの青光におけるフォトダイオードへの光の吸収率、図１７は波長５５０ｎｍの緑光におけるフォトダイオードへの光の吸収率を示す。図１６、図１７から青光、緑光いずれも吸収率が向上するためには、ＩＴＯ膜下の酸化シリコン膜厚ｄ１を薄くした方が良好であることが分かる。図１６、図１７において、白い領域８４、８５が最適領域である。
【0129】
さらに、図１８にＩＴＯ膜下の酸化シリコン膜厚ｄ１＝２０ｎｍ、図１９にＩＴＯ膜下の酸化シリコン膜厚ｄ１＝１６０ｎｍの、それぞれ青光、緑光のフォトダイオードへの吸収率をそれぞれ示す。図１９の酸化シリコン膜厚ｄ１が１６０ｎｍの場合には、青光と緑光でピークとなるＩＴＯ膜厚ｄ２が異なってしまう、青光と緑光の吸収率が共存しない。一方、図１８に示すように酸化シリコン膜厚ｄ１が薄い場合には、ＩＴＯ膜厚ｄ２を最適化することで青光と緑光の吸収率を両立することができる。
【0130】
本発明では、上記第４実施の形態の固体撮像装置を備えることにより、暗電流の抑制と感度の向上を両立させたカメラを実現することができる。
【0131】
第４実施の形態では透明導電膜７４下に絶縁膜７１として単層の酸化シリコン膜あるいは酸窒化シリコン膜を形成した構成であるが、絶縁膜として２種類以上の積層絶縁膜を形成した構成とすることもできる。この場合の実施の形態を次に示す。
【0132】
（第５実施の形態）
図２０は、第５実施の形態に係る固体撮像装置における、画素部の要部断面図である。本実施の形態も裏面照射型の固体撮像装置であり、第１実施の形態と同一の構成要素には、同じ符号を付してあり、その説明は省略する。
【0133】
本実施の形態に係る固体撮像装置は、光電変換部となるフォトダイオードで構成された受光部の受光面、すなわちフォトダイオードを構成する第１導電型領域（ｎ型の電荷蓄積領域）４１の受光面上に２種類以上の絶縁膜による積層絶縁膜８３、本例では下層の絶縁

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膜７２、本例では酸化シリコン（ＳｉＯ2 ）膜と、上層の絶縁膜７３、本例では窒化シリコン（ＳｉＮ）膜の２層絶縁膜を介して透明導電膜７４を形成し、この透明導電膜７４に負電圧を印加するように構成される。透明導電膜７４は、受光部表面のポテンシャルを制御する制御ゲートとなる。下層の絶縁膜（酸化シリコン膜）７２は受光部の受光面に接するように下層に形成される。透明導電膜７４上には絶縁膜７５例えば酸化シリコン膜を介して平坦化膜７６が形成され、平坦化膜７６上にカラーフィルタ３５、その上にオンチップマイクロレンズ３６が形成される。透明導電膜７４には、絶縁膜（酸化シリコン膜）７５を貫通して配線（遮光膜を兼ねる）７７が接続され、この配線７７が撮像領域８１（画素部１１に相当）から周辺回路領域８２上に延長して形成される。

【0134】

ここで、２層の絶縁膜７２、７３のうち、上層の絶縁膜（窒化シリコン膜）７３は屈折率が２．０程度であり、透明導電膜７４の例えばＩＴＯ膜の屈折率が２．０程度であるので、両者は光学的にほぼ同等の光学特性を有する。このため、透明導電膜（ＩＴＯ膜）７４の膜厚ｄ２は実効的に屈折率が同程度の透明導電膜（ＩＴＯ膜）７４と上層の絶縁膜（窒化シリコン膜）７３の合計の膜厚となる。上層の絶縁膜７３として、窒化シリコン膜に代えて屈折率が２．０程度の酸化ハフニウム（ＨｆＯ2 ）膜を用いることもできる。

【0135】

そして、本実施の形態においては、第４実施の形態と同様に、透明導電膜７４下の絶縁膜（本例では酸化シリコン膜）７２の膜厚ｄ１を５０ｎｍ以下に設定する。好ましくは絶縁膜（酸化シリコン膜）７２の膜厚ｄ１を５０ｎｍ以下にし、その絶縁膜厚（酸化シリコン膜厚）ｄ１に応じて上記実効的な透明導電膜厚ｄ２を最適化する。絶縁膜７２としては、酸化シリコン膜に代えて酸窒化シリコン膜を用いることもできる。透明導電膜７４としては、ＩＴＯ膜の他、前述した酸化亜鉛膜を用いることもできる。

【0136】

絶縁膜（酸化シリコン膜）７２の膜厚ｄ１としては、上層絶縁膜７３が酸化ハフニウム（ＨｆＯ2 ）膜の場合には、０．５ｎｍ程度まで薄くすることが可能である。従って、膜厚ｄ１としては５０ｎｍ以下、０．５ｎｍ～５０ｎｍの範囲、好ましくは３０ｎｍ以下、１５ｎｍ～３０ｎｍとすることができる。

【0137】

本実施の形態の積層絶縁膜８３を有する構成を図１５に当てはめた場合、ＩＴＯ膜厚ｄ２は、実効的にＩＴＯ膜７４と窒化シリコン膜あるいは酸化ハフニウム膜の上層の絶縁膜７３との合計膜厚となる。すなわち、第５実施の形態においても、図１５に示すと同傾向のデータが得られる。

【0138】

第５実施の形態によれば、第４実施の形態と同様に、フォトダイオードで構成された受光部３１の受光面上に下層を絶縁膜７２である酸化シリコン膜とした積層絶縁膜８３を介して透明導電膜７４を形成し、この透明導電膜７４に負電圧を印加することにより、フォトダイオード表面がホールアキュミレーション状態（正孔蓄積状態）になり、界面準位に起因した暗電流成分を抑制することができる。しかも、透明導電膜７４下の酸化シリコン膜厚ｄ１を５０ｎｍ以下にすることにより、透明導電膜７４を用いても感度低下を伴うことなく、低暗電流かつ高感度を実現できる。

【0139】

本発明では、上記第５実施の形態の固体撮像装置を備えることにより、暗電流の抑制と感度の向上を両立させたカメラを実現することができる。

【0140】

図２１～図２２に、上述の第４実施の形態の固体撮像装置の製造方法の実施の形態を示す。同図は模式的断面図であり、撮像領域８１と周辺回路領域８２の部分を示している。

先ず、図２１Ａに示すように、撮像領域８１にフォトダイオードを含む画素と配線層が形成され、周辺回路領域８２に所要の周辺回路が形成された半導体基板３０の裏面上に、フォトダイオード及び周辺回路側の全面に所要の膜厚の単層の絶縁膜７１及び所要の膜厚

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の透明導電膜７４を積層する。絶縁膜（酸化シリコン膜）７１は、好ましくは薄い方がよい。

【0141】

本例では絶縁耐圧と吸収率を考慮して膜厚１５ｎｍの単層の絶縁膜（酸化シリコン膜）７１を形成する。この絶縁膜（酸化シリコン膜）７１上に膜厚５０ｎｍの透明導電膜７４であるＩＴＯ膜を積層する。絶縁膜７１の酸化シリコン膜は、ＳｉH4 、O2 を原料としたプラズマＣＶＤ法や、ＴＥＯＳを用いたプラズマＣＶＤ法などを用いて形成することができる。また、透明導電膜７４のＩＴＯ膜は、ＩＴＯターゲットを用いたスパッタ法を用いて成膜できる。この際、透明導電膜（ＩＴＯ膜）７４の膜厚ｄ２は下部の絶縁膜（酸化シリコン膜）７１の膜厚ｄ１に応じて最適化する必要がある。ここでは上記のように絶縁膜厚（酸化シリコン膜厚）ｄ１が１５ｎｍであるので、それに対応して透明導電膜（ＩＴＯ膜）７４は最適化した５０ｎｍとする。勿論酸化シリコン膜厚ｄ１が異なれば、それに応じてＩＴＯ膜厚ｄ２も変更される。

【0142】

次に、図２１Ｂに示すように、ＩＴＯ膜７４を選択的にエッチング除去して所望の領域、すなわち画素が形成される撮像領域８１のみに残す。

【0143】

次に、図２１Ｃに示すように、透明導電膜（ＩＴＯ膜）７４及び周辺回路８２側の全面に所要の膜厚の絶縁膜（酸化シリコン膜）７５を形成する。本例ではプラズマＣＶＤ法を用いて１５０ｎｍ程度の絶縁膜（酸化シリコン膜）７５を形成する。

【0144】

次に、図２１Ｄに示すように、透明導電膜（ＩＴＯ膜）７４へバイアス電圧を印加するための配線用のコンタクトホール８６を絶縁膜（酸化シリコン膜）７５に形成する。

【0145】

次に、図２２Ｅに示すように、このコンタクトホール８６を含む全面に遮光膜と配線を兼ねる金属膜７７ａを形成する。金属膜７７ａは積層構造とすることができ、積層構造として最上層をＡｌとしたＡｌ／ＴｉＮ／Ｔｉを用いることができる。

【0146】

次に、図２２Ｆに示すように、金属膜７７ａをパターニングして周辺回路８２側へ伸びる遮光膜を兼ねる配線７７を形成する。

【0147】

次に、図２２Ｇに示すように、全面に所要の膜厚の平坦化膜７６を形成する。本例ではシリコン（Ｓｉ）と酸素（Ｏ）と炭素（Ｃ）を主成分とする絶縁膜を１μｍ程度塗布し、アニールして平坦化膜７６を形成する。この平坦化膜７６上にカラーフィルタ３５を形成し、さらにその上に集光のためのオンチップマイクロレンズ３６を形成して、目的の第４実施の形態の固体撮像装置を得る。

【0148】

図２３～図２４に、上述の第５実施の形態の固体撮像装置の製造方法の実施の形態を示す。同図は模式的断面図であり、撮像領域８１と周辺回路領域８２の部分を示している。

先ず、図２３Ａに示すように、撮像領域８１にフォトダイオードを含む画素と配線層が形成され、周辺回路領域８２に所要の周辺回路が形成された半導体基板３０の裏面上に、フォトダイオード及び周辺回路側の全面にわたり、所要の膜厚の積層絶縁膜８３及び所要の膜厚の透明導電膜７４を積層する。

【0149】

本例では絶縁耐圧と吸収率を考慮して膜厚１５ｎｍ程度の下層の絶縁膜７２である酸化シリコン膜を形成し、その上に上層の絶縁膜７３である窒化シリコン膜を形成して積層絶縁膜８３とし、さらにその上に透明導電膜７４としてＩＴＯ膜を形成する。絶縁膜７２の酸化シリコン膜は、ＳｉH4 、O2 を原料としたプラズマＣＶＤ法や、ＴＥＯＳを用いたプラズマＣＶＤ法等を用いて形成することができる。上層の絶縁膜７３の窒化シリコン膜は、ＳｉH4 、ＮH3 またはＳｉH4 、N2 を原料としたプラズマＣＶＤ法で形成するこ

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とができる。透明導電膜７４のＩＴＯ膜は、ＩＴＯターゲットを用いたスパッタ法を用いて成膜できる。なお、絶縁膜（窒化シリコン膜）７３と透明導電膜（ＩＴＯ膜）７４の合計の膜厚ｄ２は、下層の絶縁膜（酸化シリコン膜）７２に対して最適化する必要がある。絶縁膜（酸化シリコン膜）７２は、好ましくは薄い方が良い。ここでは絶縁膜（酸化シリコン膜）７２の膜厚が１５ｎｍ程度であるので、それに対して最適化して上層の絶縁膜厚（窒化シリコン膜厚）７３の膜厚を３０ｎｍ程度、透明導電膜（ＩＴＯ膜）の膜厚を２０ｎｍ程度とする。勿論、絶縁膜（酸化シリコン膜）７２の膜厚ｄ１が異なれば、それに応じて絶縁膜（窒化シリコン膜）７３の膜厚、透明導電膜（ＩＴＯ膜）の膜厚も変更される。

【0150】

次に、図２３Ｂに示すように、透明導電膜(ＩＴＯ膜）７４を選択的にエッチング除去して所望の領域、すなわち画素が形成される撮像領域８１のみに残す。

【0151】

次に、図２３Ｃに示すように、透明導電膜(ＩＴＯ膜）７４及び周辺回路８２側の全面に所要の膜厚の絶縁膜(酸化シリコン膜）７５を形成する。本例ではプラズマＣＶＤ法を用いて１５０ｎｍ程度の絶縁膜(酸化シリコン膜）７５を形成する。

【0152】

次に、図２３Ｄに示すように、透明導電膜(ＩＴＯ膜）７４へバイアス電圧を印加するための配線用のコンタクトホール８６を絶縁膜(酸化シリコン膜）７５に形成する。

【0153】

次に、図２４Ｅに示すように、このコンタクトホール８６を含む全面に遮光膜と配線を兼ねる金属膜７７ａを形成する。金属膜７７ａは積層構造とすることができ、積層構造として最上層をＡｌとしたＡｌ／ＴｉＮ／Ｔｉを用いることができる。

【0154】

次に、図２４Ｆに示すように、金属膜７７ａをパターニングして周辺回路８２側へ伸びる遮光膜を兼ねる配線７７を形成する。

【0155】

次に、図２４Ｇに示すように、全面に所要の膜厚の平坦化膜７６を形成する。本例ではシリコン（Ｓｉ）と酸素（Ｏ）と炭素（Ｃ）を主成分とする絶縁膜を１μｍ程度塗布し、アニールして平坦化膜７６を形成する。この平坦化膜７６上にカラーフィルタ３５を形成し、さらにその上に集光のためのオンチップマイクロレンズ３６を形成して、目的の第５実施の形態の固体撮像装置を得る。

【0156】

本実施の形態の固体撮像装置の製造方法によれば、このようにして界面準位に起因した暗電流の抑制と高感度化を両立させた裏面照射型のＣＭＯＳ固体撮像装置を製造することができる。

【0157】

なお、第６実施の形態として、図示しないが、図１４及び図２０の固体撮像装置において、フォトダイオードを構成するｎ型半導体領域の受光面側の表面に暗電流抑制のためのｐ型半導体領域（正孔蓄積領域）を形成した構成とすることができる。このような埋め込み型フォトダイオードと組み合わせることにより、透明導電膜に印加する負電圧を低くすることができ、かつ界面のｐ型半導体領域の不純物濃度を低くして従来と同じ暗電流抑制効果を得ることができる。

【0158】

さらに、第４実施の形態、第５実施の形態または第６実施の形態と、第１実施の形態、第２実施の形態または第３実施の形態とを組み合わせた構成とすることもできる。

【0159】

上述の第４実施の形態、第５実施の形態及び第６実施の形態は、裏面照射型のＣＭＯＳイメージセンサで適用したが、表面照射型のＣＭＯＳイメージセンサに適用することも可能である。また、ＣＣＤイメージセンサに適用することも可能である。

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【0160】
上述したように、第４実施の形態以降の実施の形態によれば、暗電流の抑制と、感度向上の両立を図った固体撮像装置およびカメラを実現することができる。
【0161】
（第６実施の形態）
次に、本発明に係る固体撮像装置の第６実施の形態を説明する。
【0162】
図２５は、第６実施の形態に係る固体撮像装置における、画素部の要部の断面図である。本実施の形態も裏面照射型の固体撮像装置であり、第１実施の形態と同一の構成要素には、同じ符号を付して、その説明は省略する。
【0163】
本実施の形態に係る固体撮像装置は、光電変換部となるフォトダイオードで構成された受光部３１の受光面上（すなわち、基板の第２面側）上、すなわちフォトダイオードを構成する第１導電型領域（ｎ型の電荷蓄積領域）４１の受光面上に所要の膜厚ｄ３を有する、負の固定電荷を有する膜、例えば少なくとも一部が結晶化した絶縁膜９２が形成される。この少なくとも一部が結晶化した絶縁膜９２としては、ハフニウム、ジルコニウム、アルミニウム、タンタル、チタン、イットリウム、ランタノイド等の元素の酸化物絶縁膜であり、膜中に少なくとも一部が結晶化した領域を有するものである。
【0164】
この少なくとも一部が結晶化した絶縁膜９２の膜厚としては、３ｎｍ以上、１００ｎｍ以下とすることができる。膜厚が３ｎｍより薄いと、結晶化し難くい。膜厚の上限は実用上１００ｎｍ程度でよく、それより厚くする必要はない。透過率など光学的には、数１０ｎｍ程度の膜厚が最適である。
【0165】
上記結晶化した絶縁膜９２と受光部３１の受光面との界面には所要の薄い膜厚ｄ３の絶縁膜９３、本例では酸化シリコン膜が形成される。結晶化した絶縁膜９２の酸化ハフニウム膜は、所要の温度による結晶化アニールで、膜中に負の電荷が形成される。この結晶化した絶縁膜９２は、受光部３１の受光面のポテンシャルを制御するポテンシャル制御機能を有する。
【0166】
上記結晶化した絶縁膜９２上には所要の膜厚の絶縁膜９４、例えば酸化シリコン膜を介して平坦化膜９５が形成される。平坦化膜９５上にはカラーフィルタ３５、その上にオンチップマイクロレンズ３６が形成される。撮像領域８１（画素部１１に相当）に隣接する周辺回路領域８２の絶縁膜（酸化シリコン膜）９４上には遮光膜９７が形成される。
【0167】
結晶化した絶縁膜９２、例えば酸化ハフニウム膜の場合は前述したように屈折率が２．０程度であり、その上の絶縁膜(酸化シリコン膜）９４は屈折率が１．４５程度である。したがって、結晶化した絶縁膜（酸化ハフニウム膜）９２と絶縁膜(酸化シリコン膜）９４により反射防止膜が形成される。
【0168】
第６実施の形態に係る固体撮像装置によれば、受光部３１の受光面上に負の固定電荷を有する膜、例えば少なくとも一部が結晶化した絶縁膜９２を形成することにより、フォトダイオードの表面を正孔蓄積状態とさせることができる。これにより、界面準位に起因した暗電流成分を抑制することができる。また、従来のように正孔蓄積層を形成するためのイオン注入及びアニールを施すこともなく、もしくは低濃度のドーズ量であってもフォトダイオード表面を正孔蓄積状態にすることができ、界面準位に起因の暗電流を抑制することができる。さらに、負の固定電荷を有する膜、例えば結晶化した絶縁膜（例えば酸化ハフニウム膜）９２とその上の絶縁膜(酸化シリコン膜）９４により反射防止膜が形成され、低暗電流かつ高感度を実現できる。
【0169】

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本発明では、上記第６実施の形態の固体撮像装置を備えることにより、暗電流の抑制と感度の向上を両立させたまめ等を実現することができる。

【0170】

更に、詳細説明する。前述したフォトダイオード、すなわち第１導電型領域（ｎ型の電荷蓄積領域）の表面側に第２導電型領域（ｐ型の正孔蓄積領域）を有する、いわゆる埋込み型のフォトダイオード構造は、界面準位起因のキャリア生成に起因した暗電流を、界面近傍を正孔（ホール）蓄積状態にすることによって抑制している。ここで、イオン注入によって正孔蓄積状態に出来ない場合は、フォトダイオード中の不純物プロファイル（ドーパント・プロファイル）でなく、フォトダイオードの上層の膜の固定電荷によって表面近傍を正孔蓄積状態にすればよい。また、この受光部に接する膜は、より界面準位を低減できた方が暗電流の低減には好適である。そのために必要なことは、界面準位が少ない上に、膜中に負の固定電荷を有する膜を形成することである。

【0171】

上記したような界面準位が少ない上に、膜中に負の固定電荷を形成する材料としては、Atomic Layer Deposition法による酸化ハフニウムが好適である。

【0172】

近年、低消費電力向けＬＳＩでは、低リーク電流を達成するために数ｎｍレベルの酸化ハフニウムが検討されており、さらに、酸化ハフニウムは結晶化するとリーク電流が増加することが知られている。一般的には、ゲート絶縁膜用途の数ｎｍ程度の膜厚の酸化ハフニウム膜は、５００℃程度の温度で結晶化するといわれている。そのため、耐熱性を向上するために酸化ハフニウムにＳｉを添加し、結晶化温度を上昇させるなどの対策が用いられている。しかしながら、ゲート絶縁膜用途でなく、イメージセンサのフォトダイオード表面に酸化ハフニウム膜を形成する場合は、リーク電流という特性は問題にならない。

【0173】

また、低反射膜構造を実現するためには、図２６に示すように、酸化ハフニウム（HfO_2）膜として、５０ｎｍ程度の膜厚が好適である。図２６は、フォトダイオード上に下から酸化シリコン（SiO_2）膜、酸化ハフニウム（HfO_2）膜、酸化シリコン（SiO_2）膜及びカラーフィルタを順次積層形成した、フォトダイオード構造において、酸化ハフニウム膜の膜厚を１０ｎｍから１０ｎｍ刻みで１００ｎｍまで変化させたときに、膜厚の依存性を示している。縦軸に緑フォトダイオードへの光の吸収率（％）、横軸に青フォトダイオードへの光の吸収率（％）を採ったときの、膜厚が５０ｎｍ程度で、青フォトダイオードへの光の吸収率が９０％以上、緑フォトダイオードへの光の吸収率が８０％以上となっている。

【0174】

上記のように従来のＭＯＳ－ＬＳＩで用いられなかった厚い膜厚の酸ハフニウム膜を形成した最には、結晶化温度が低下し３００℃程度で結晶化が開始することが分かった。図２７は、３２０℃、１６時間の熱処理の有無による酸ハフニウム膜のＴＥＭ写真である。図２７Ａは熱酸化処理の無い場合のＴＥＭ写真であり、図２７Ｂは熱酸化処理後のＴＥＭ写真である。図２７では、シリコン基板２０１上に酸化シリコン膜２０２、酸ハフニウム膜２０３、保護膜となる酸化シリコン膜２０４がこの順に積層された構成である。図２７Ｂに示すように、熱処理後に酸ハフニウム膜２０３が全体にわたり結晶化していることが確認できる。図２７Ａの熱処理しない酸ハフニウム膜２０３は結晶化している領域は膜中の局所的な領域に限られる。

【0175】

また、図２８は、酸ハフニウム膜において、上記のような熱処理を伴う結晶化で膜中の固定電荷がどのような振る舞いをするかを示している。図２９は、酸化ハフニウム（HfO_2）膜１０ｎｍと酸化シリコン（SiO_2）膜の積層膜構造をゲート絶縁膜としたＭＯＳキャパシタのＣ－Ｖ特性である。同図では、ＭＯＳキャパシタを作製した後、熱処理温度を３２０℃に固定して、熱処理時間を変化したときの、フラットバンド電圧Ｖｆｂを測定した結果である。図２８から分かるように、熱処理時間の延長と共に、フラットバン

ド電圧Ｖｆｂがプラスにシフトして行く。つまり、酸ハフニウム膜中の負の電荷が増加していることが分かる。

【0176】

同様に、図２９に、熱処理時間を１時間に固定して、熱処理温度を変化したときの電圧Ｖｆｂの挙動を示す。この場合も、熱処理温度が高い方がフラットバンド電圧Ｖｆｂはプラスにシフト、つまり酸ハフニウム膜中の負の電荷が増加していることが示されている。

【0177】

このように、例えば５０ｎｍという厚い酸ハフニウム膜を用いるときは、低反射構造を実現することができる。同時に、結晶化温度を下げ、絶縁膜中の負電荷を増やすことができ、固体撮像装置において好適である。以上、酸化ハフニウム膜を１０ｎｍ以上の膜厚にして熱処理を施すことにより、４００℃以下の温度で酸化ハフニウムの結晶膜が形成され、また熱処理の増加、つまり結晶化が進行するに伴い酸化ハフニウム膜に負の電荷が形成されることを新たに見出された。これは、従来のＭＯＳ－ＬＳＩ用とゲート絶縁膜用途としては固定電荷が多い事、かつ結晶化することによるリーク電流の増加という避けるべき特性である。しかし、本実施の形態では、上記酸化ハフニウム膜は、固体撮像装置のフォトダイオード表面への正孔蓄積効果に対して非常に適している。これにより、４００℃以下の低温プロセスでフォトダイオード表面を正孔蓄積状態にすることを可能とし、暗電流抑制が実現できる。

【0178】

上例では、酸化ハフニウム膜について説明したが、その他、ジルコニウム、アルミニウム、タンタル、チタン、イットリウム、ランタノイド等の酸化物絶縁膜についても、膜中に負の固定電荷を形成することができる。受光面上にこれらの酸化物絶縁膜を形成することにより、フォトダイオードフォトダイオード表面を正孔蓄積状態にすることが可能になり、暗電流抑制が実現できる。

【0179】

図３０～図３２に、上述の第６実施の形態の固体撮像装置の製造方法の実施の形態を示す。同図は模式的断面図であり、撮像領域８１と周辺回路８２の部分を示している。

【0180】

先ず、図３０Ａに示す半導体基板３０の撮像領域８１に２次元アレイ状にフォトダイオードを含む複数の画素を形成し、周辺回路８１にＣＭＯＳトランジスタからなるロジック回路等を形成する。

【0181】

次に、図３０Ｂに示すように、撮像領域８１及び周辺回路８２の全面上にＡＬＤ法によって酸化ハフニウム膜９２を形成する。この酸化ハフニウム膜９２は屈折率が２．０程度であり、好適な膜厚を調整することで反射防止効果を得ることが可能になる。好ましくは膜厚が５０ｎｍ～６０ｎｍの酸化ハフニウム膜９２を形成する。また、前記ＡＬＤ法によって酸化ハフニウム膜９２を形成する際には、基板３０の表面つまりフォトダイオード表面と、酸化ハフニウム膜９２との界面に１ｎｍ程度の酸化シリコン膜９３が形成される。

【0182】

次に、図３０Ｃに示すように、酸化ハフニウム膜９２の結晶化アニールを行い、酸化ハフニウム膜中に負の固定電荷を形成する。

【0183】

次に、図３１Ｄに示すように、酸化ハフニウム膜９２上に酸化シリコン膜９４及び遮光膜９７を形成する。この酸化シリコン膜９４を形成することで、酸化ハフニウム膜９２と遮光膜９７とが直接接触せず、両者の接触に起因した酸化ハフニウム膜９２と遮光膜９７との反応を抑制することができる。同時に、遮光膜９７のエッチングの際に酸化ハフニウム膜９２の表面を直接エッチングに晒すことを防ぐことができる。また、遮光膜９７としては、遮光能力に優れたタングステン（Ｗ）を用いるのが好ましい。

【0184】

次に、図３１Ｅに示すように、遮光膜９７を撮像領域８１の一部及び周辺回路８２の全

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面を覆うように選択除去する。この加工された遮光膜９７によって、フォトダイオードに光が入らない領域を作り、フォトダイオードの出力によって画像での黒レベルを決定する。また、周辺回路８２には光が入ることによる特性変動を抑制する。

【0185】

次に、図３２Ｆに示すように、遮光膜９７による段差を低減する平坦化膜９５を形成する。この平坦化膜９５は塗布による絶縁膜で形成される。

【0186】

次に、図３２Ｇに示すように、平坦化膜９５上の撮像領域８１側において、カラーフィルタ３５を形成し、さらにその上に集光のためのオンチップマイクロレンズ３６を形成して、目的の第６実施の形態の固体撮像装置を得る。

【0187】

本発明は、上記の実施形態の説明に限定されない。

例えば、本実施形態で挙げた数値や材料は一例であり、これに限定されるものではない。

その他、本発明の要旨を逸脱しない範囲で、種々の変更が可能である。

【図面の簡単な説明】

【0188】

【図1】第１～第６実施形態に係る固体撮像装置の概略構成図である。

【図2】画素部の単位画素の回路図である。

【図3】固体撮像装置の概略断面図である。

【図4】第１実施形態に係る固体撮像装置における、基板の要部断面図である。

【図5】第１実施形態に係る固体撮像装置の動作におけるバイアス例を示す図である。

【図6】第１実施形態に係る固体撮像装置の製造の一例を示す工程断面図である。

【図7】第１実施形態に係る固体撮像装置の製造の一例を示す工程断面図である。

【図8】第１実施形態に係る固体撮像装置の製造の他の例を示す工程断面図である。

【図9】第１実施形態に係る固体撮像装置の製造の他の例を示す工程断面図である。

【図10】カメラの概略構成を示す図である。

【図11】第２実施形態に係る固体撮像装置における、基板の要部断面図である。

【図12】第２実施形態に係る固体撮像装置の動作におけるバイアス例を示す図である。

【図13】第３実施形態に係る固体撮像装置における、基板の要部断面図である。

【図14】第４実施の形態に係る固体撮像装置における、基板の要部断面図である。

【図15】第４実施の形態に係る固体撮像装置の説明に供する、フォトダイオードに吸収される青光と緑光の吸収率のシミュレーション図である。

【図16】第４実施の形態に係る固体撮像装置の説明に供する、波長４５０ｎｍにおけるフォトダイオードへの光の吸収率の強度グラフの図である。

【図17】第４実施の形態に係る固体撮像装置の説明に供する、波長５５０ｎｍにおけるフォトダイオードへの光の吸収率の強度グラフの図である。

【図18】第４実施の形態に係る固体撮像装置の説明に供する、酸化シリコン膜厚２０ｎｍを固定して透明導電膜（ＩＴＯ膜）の膜厚を変化したときの青光と緑光の吸収率を示すグラフである。

【図19】第４実施の形態に係る固体撮像装置の説明に供する、酸化シリコン膜厚１６０ｎｍを固定してＩＴＯ膜厚を変化したときの青光と緑光の吸収率を示すグラフである。

【図20】第５実施の形態に係る固体撮像装置における、基板の要部断面図である。

【図21】Ａ～Ｄ　第４実施の形態に係る固体撮像装置の製造方法の実施の形態を示す製造工程図（その１）である。

【図22】Ｅ～Ｇ　第４実施の形態に係る固体撮像装置の製造方法の実施の形態を示す製造工程図（その２）である。

【図23】Ａ～Ｄ　第５実施の形態に係る固体撮像装置の製造方法の実施の形態を示す製造工程図（その１）である。

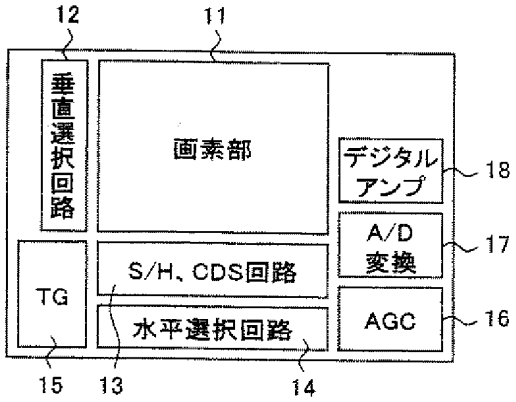
【図24】Ｅ～Ｇ　第５実施の形態に係る固体撮像装置の製造方法の実施の形態を示す製造

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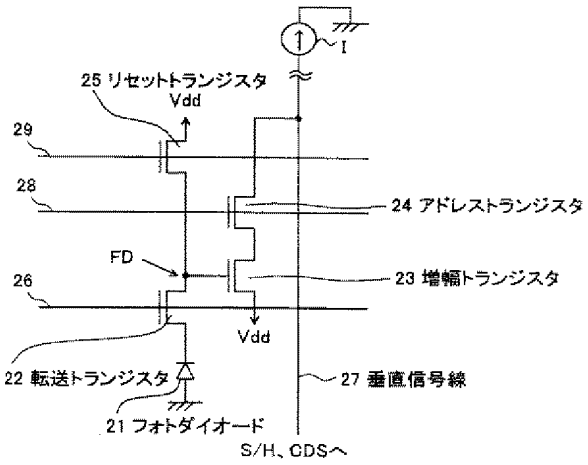
工程図（その２）である。
【図25】第６実施の形態に係る固体撮像装置における、基板の要部断面図である。
【図26】第６実施の形態に係る固体撮像装置の説明に供する、酸化ハフニウム膜を用いたときの青、緑のフォトダイオードへの光の吸収率を示す特性図である。
【図27】Ａ，Ｂ　熱処理の有無による酸化ハフニウムのＴＥＭ写真である。
【図28】酸化ハフニウム膜を用いたＭＯＳキャパシタのＶｆｂの熱処理時間依存性を示すグラフである。
【図29】酸化ハフニウム膜を用いたＭＯＳキャパシタのＶｆｂの熱処理温度依存性を示すグラフである。
【図30】Ａ～Ｃ　第６実施の形態に係る固体撮像装置の製造方法の実施の形態を示す製造工程図（その１）である。
【図31】Ｄ～Ｅ　第６実施の形態に係る固体撮像装置の製造方法の実施の形態を示す製造工程図（その２）である。
【図32】Ｆ～Ｇ　第６実施の形態に係る固体撮像装置の製造方法の実施の形態を示す製造工程図（その３）である。
【符号の説明】
【0189】
１１…画素部、１２…垂直選択回路、１３…Ｓ／Ｈ・ＣＤＳ回路、１４…水平選択回路、１５…タイミングジェネレータ、１６…ＡＧＣ回路、１７…Ａ／Ｄ変換回路、１８…デジタルアンプ、２１…フォトダイオード、２２…転送トランジスタ、２３…増幅トランジスタ、２４…アドレストランジスタ、２５…リセットトランジスタ、２６，２８，２９…駆動配線、２７…垂直信号線、３０…基板、３１…受光部、３２…絶縁膜、３３…遮光膜、３３ａ…開口部、３４…保護膜、３５…カラーフィルタ、３６…オンチップマイクロレンズ、３８…配線層、３９…支持基板、４０…素子分離絶縁膜、４１…電荷蓄積領域、４２…ｐ型ウェル、４３…正孔蓄積領域、４４…正孔蓄積領域、４５…フローティングディフュージョン、４６…ｐ型領域、５０…電極層、５１…転送ゲート、５２…制御ゲート、５２－１…第１制御ゲート、５２－２…第２制御ゲート、６０…ゲート絶縁膜、６１…絶縁膜、６２…ハードマスク、６２ａ…酸化シリコン膜、６２ｂ…窒化シリコン膜、６３…サイドウォール絶縁膜、６４…埋め込み絶縁膜、６４ａ…酸化シリコン膜、６４ｂ…窒化シリコン膜、７１・・絶縁膜（酸化シリコン膜または酸窒化シリコン膜）、７２・・絶縁膜（酸化シリコン膜または酸窒化シリコン膜）、７３・・絶縁膜（窒化シリコン膜または酸化ハフニウム膜）、７４・・透明導電膜、７５・・絶縁膜（酸化シリコン膜）、７６・・平坦化膜、７７・・配線、８１・・撮像領域、８２・・周辺回路領域、８３・・積層絶縁膜、９２・・負の固定電荷を有する膜である結晶化した絶縁膜、９３・・絶縁膜（酸化シリコン膜）、９４・・絶縁膜（酸化シリコン膜）、９５・・平坦化膜、９７・・遮光膜、１００…カメラ、１０１…固体撮像装置、１０２…光学系、１０３…信号処理回路

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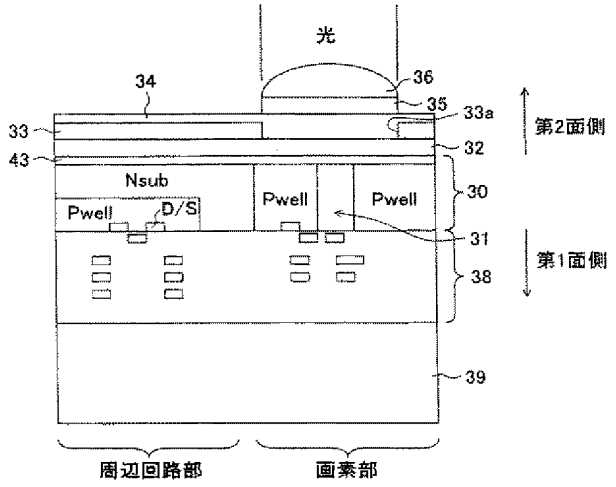
【図1】



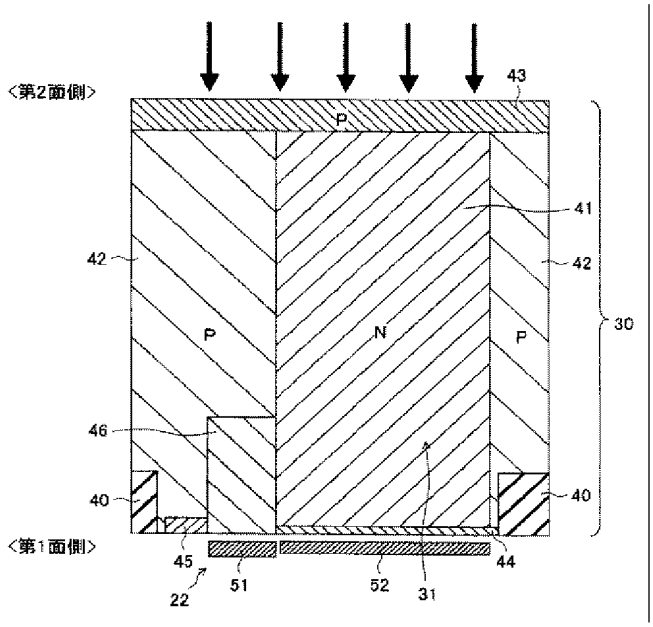
【図2】



【図3】



【図4】

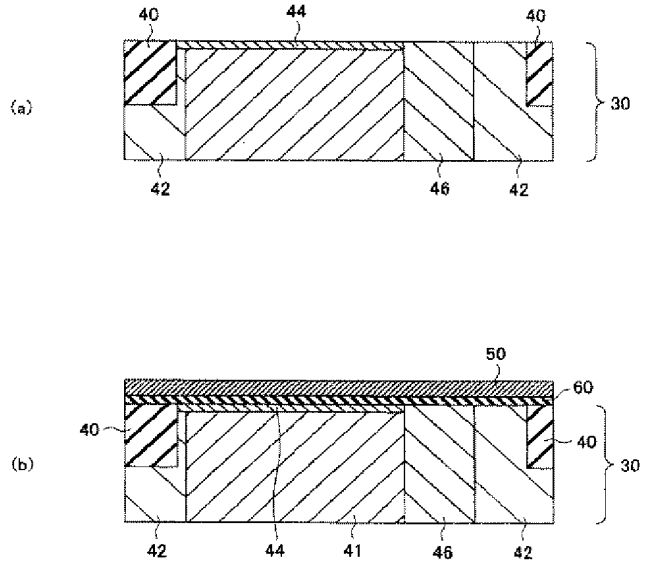


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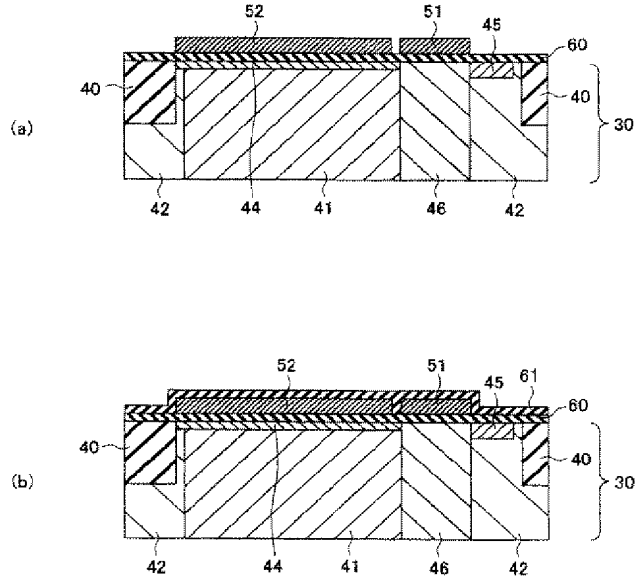
【図5】

	蓄積	読み出し	リセット
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転送ゲート	−	＋	−
リセットゲート	O	O	＋

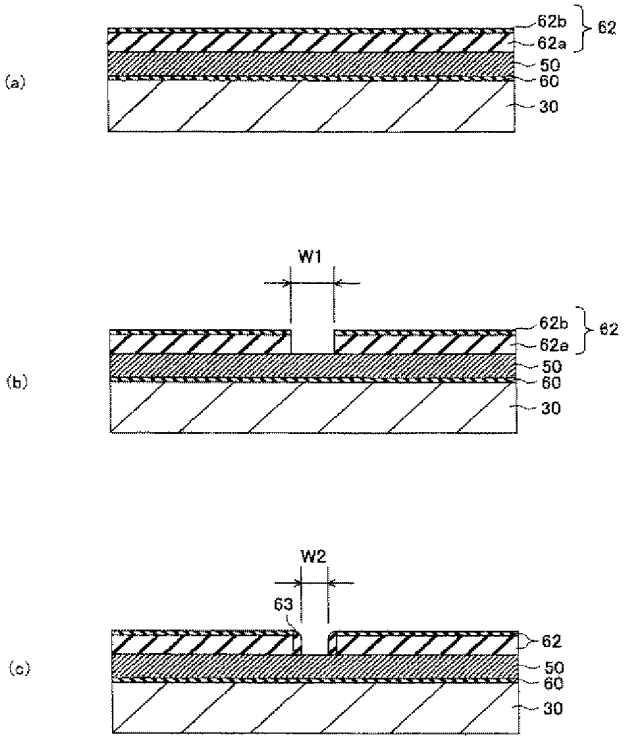
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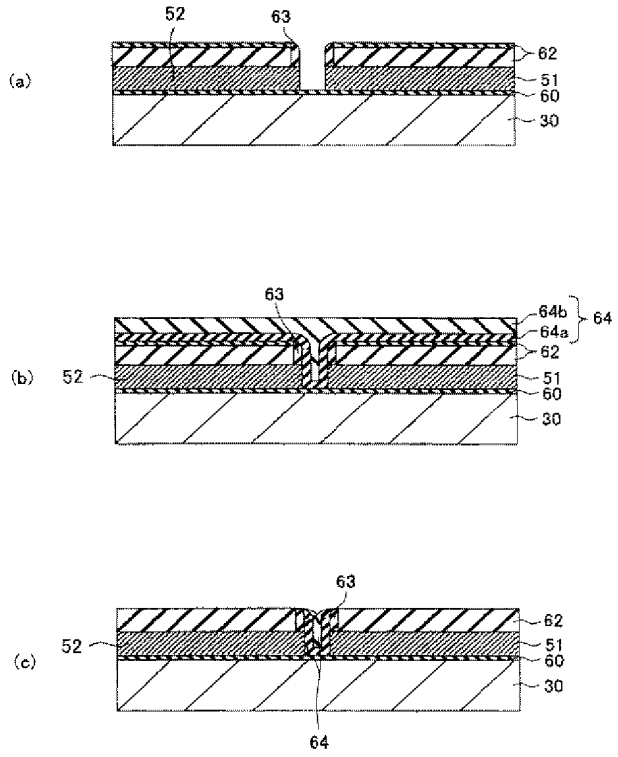
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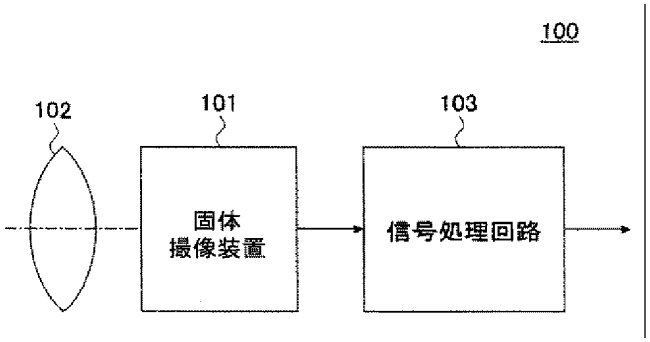
【図8】



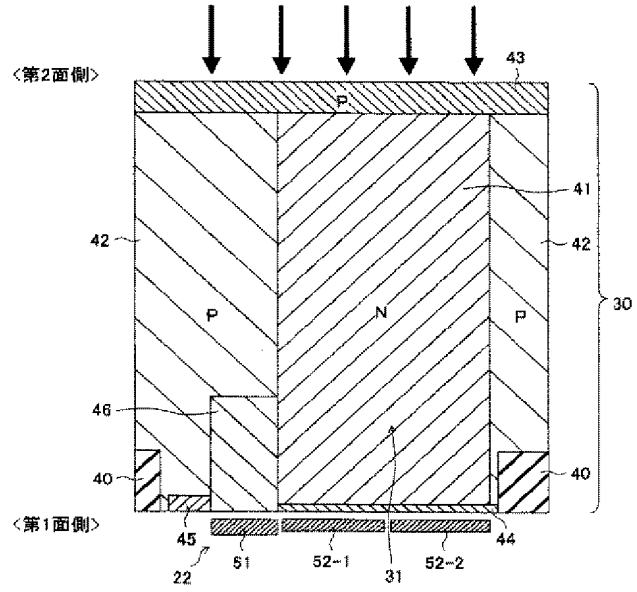
【図9】



【図10】



【図11】

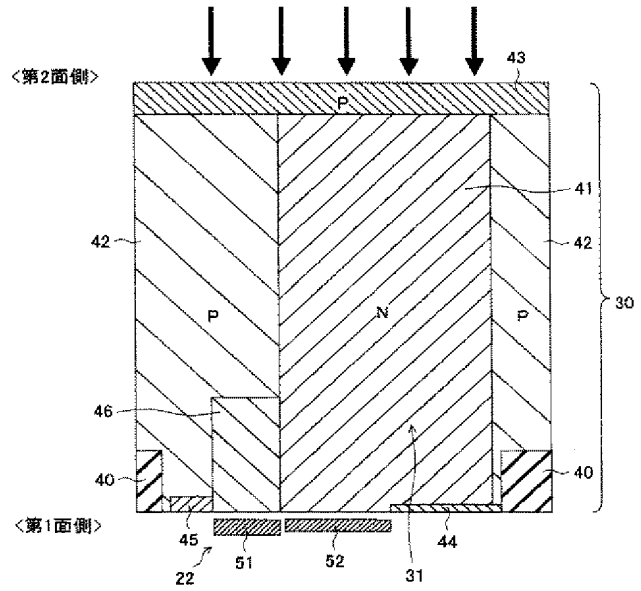


【図12】

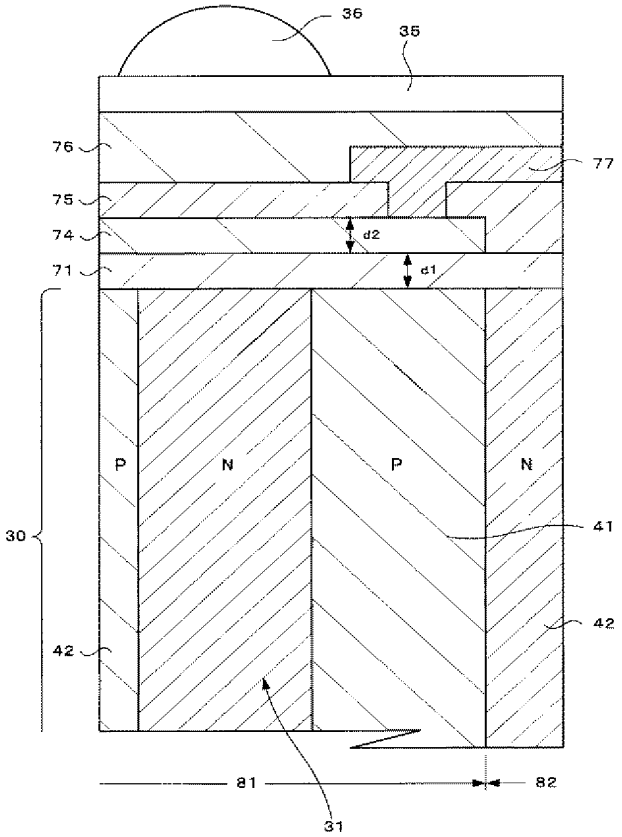
	蓄積	読み出し1	読み出し2	リセット
第2制御ゲート	−	−	−	−
第1制御ゲート	−	+	−	−
転送ゲート	−	−	+	−
リセットゲート	0	0	0	+

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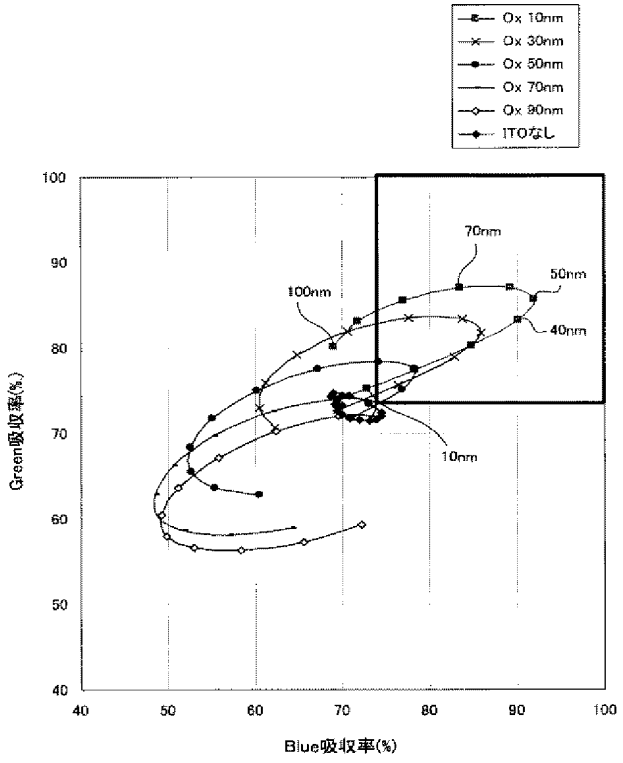
【図13】



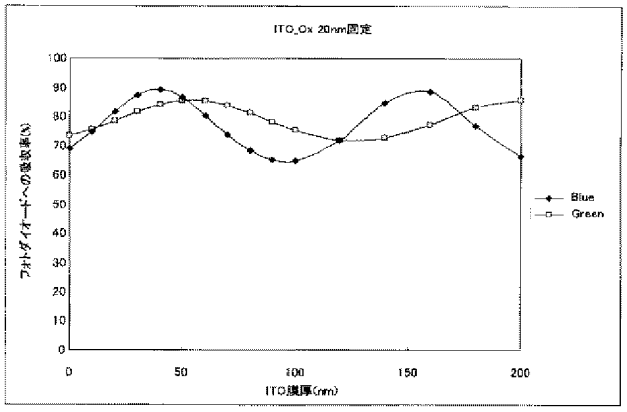
【図14】



【図15】

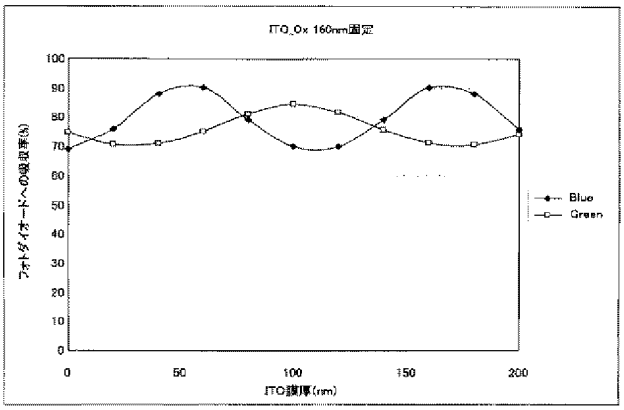


【図18】

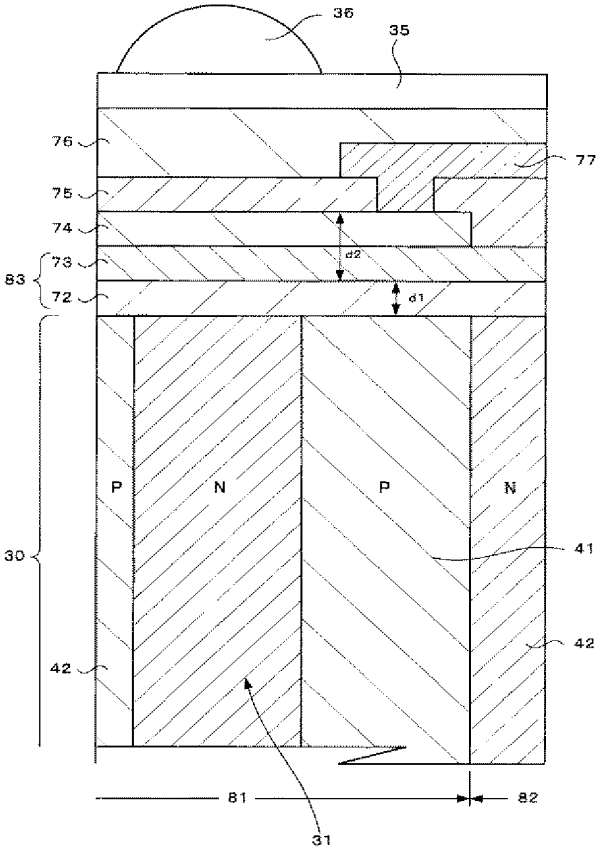


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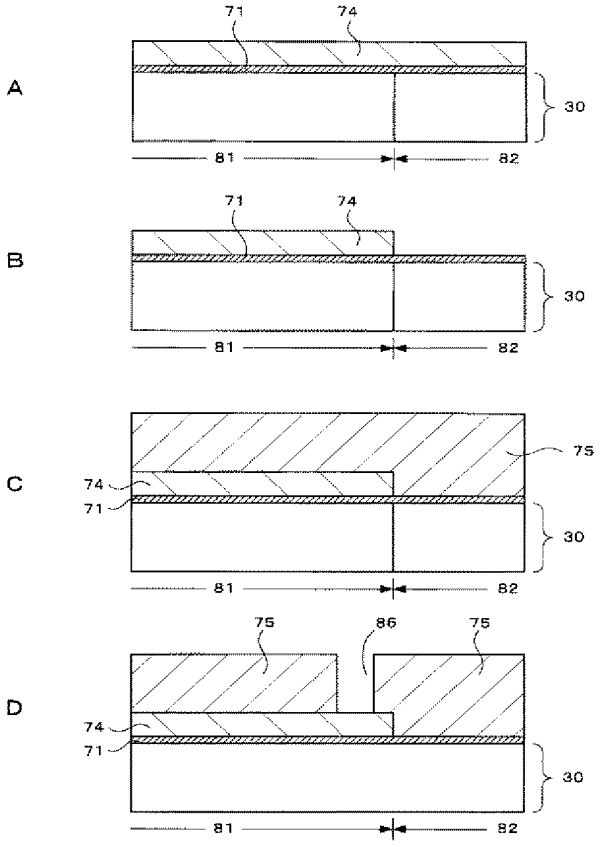
【図19】



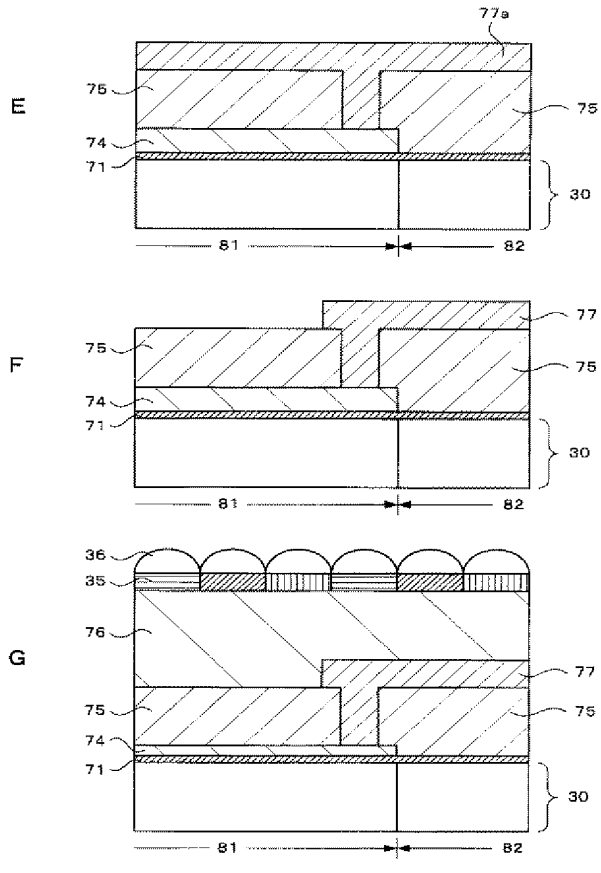
【図20】



【図21】

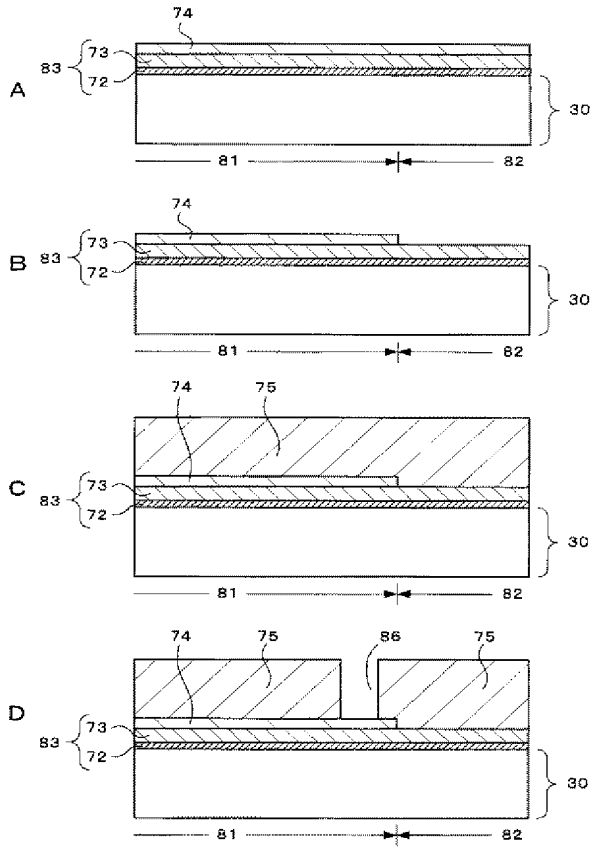


【図22】

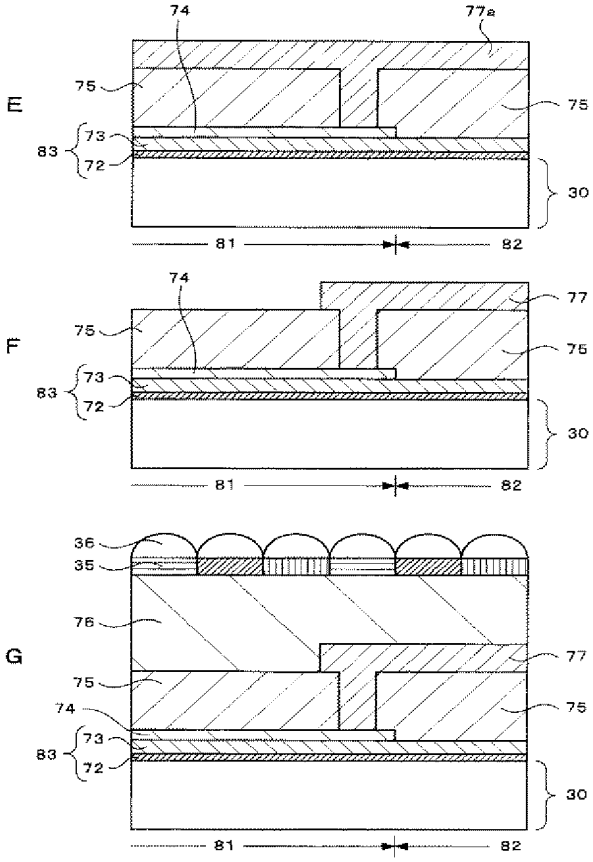


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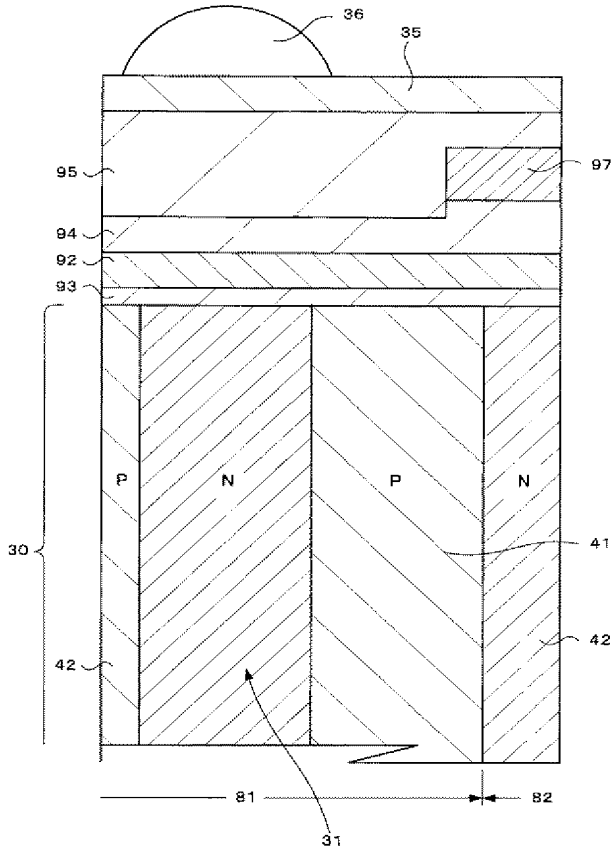
【図23】



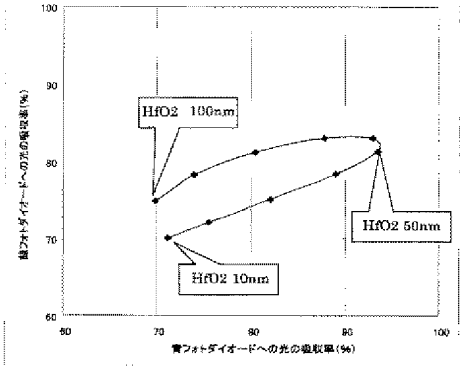
【図24】



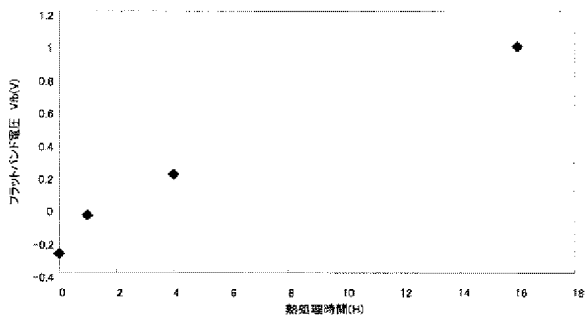
【図25】



【図26】

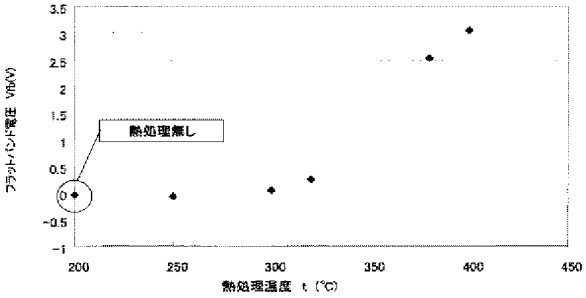


【図28】

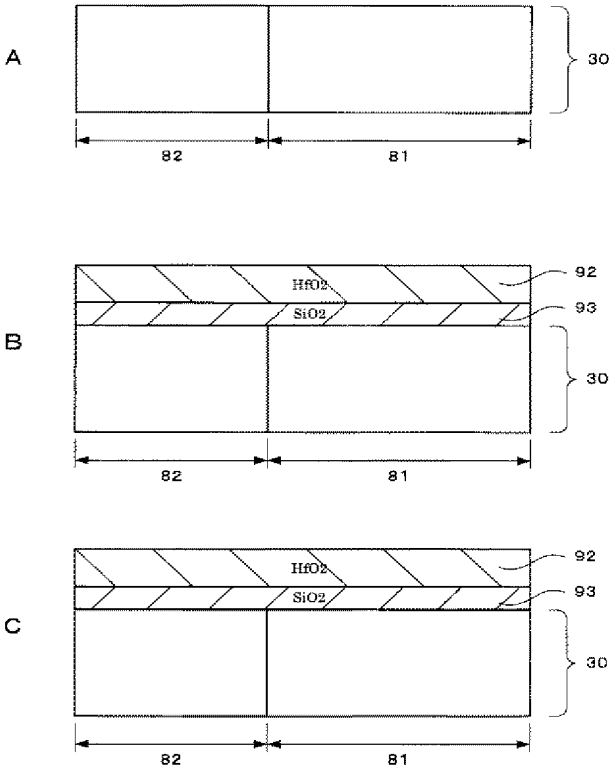


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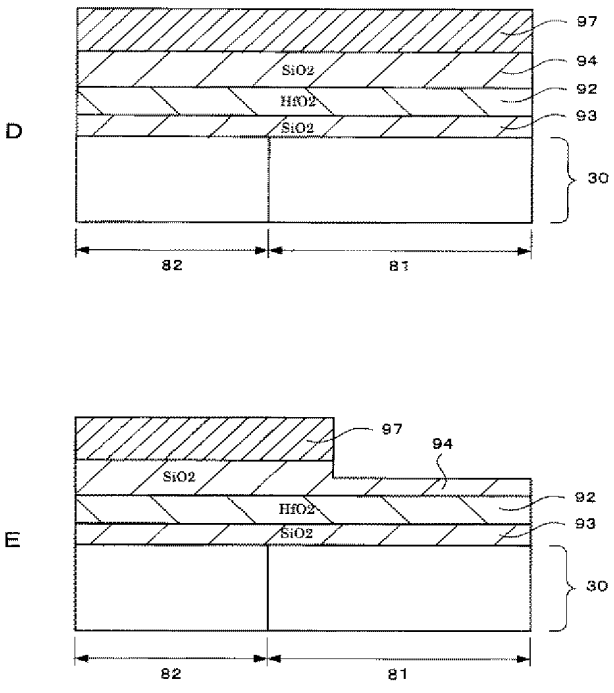
【図29】



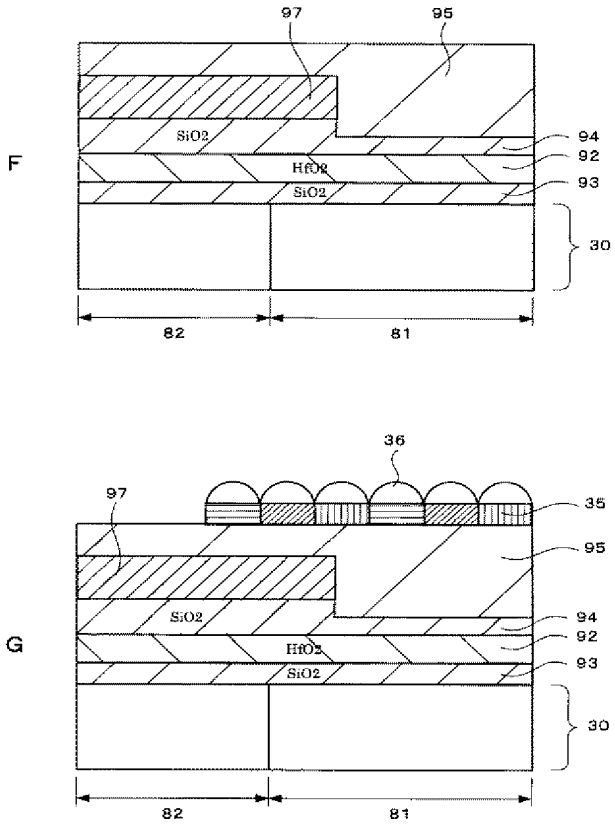
【図30】



【図31】

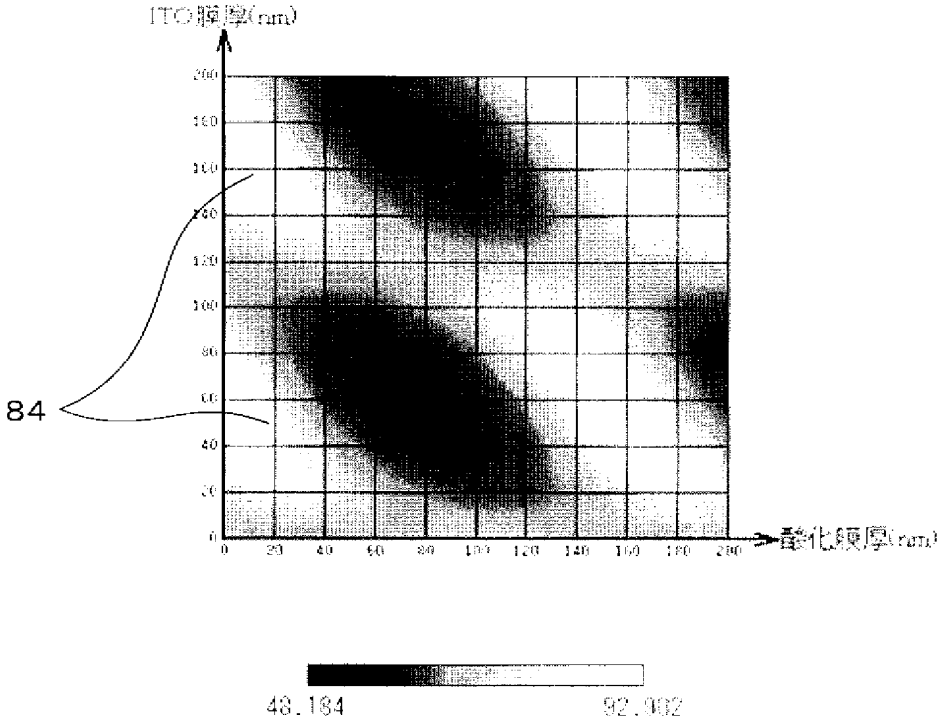


【図32】



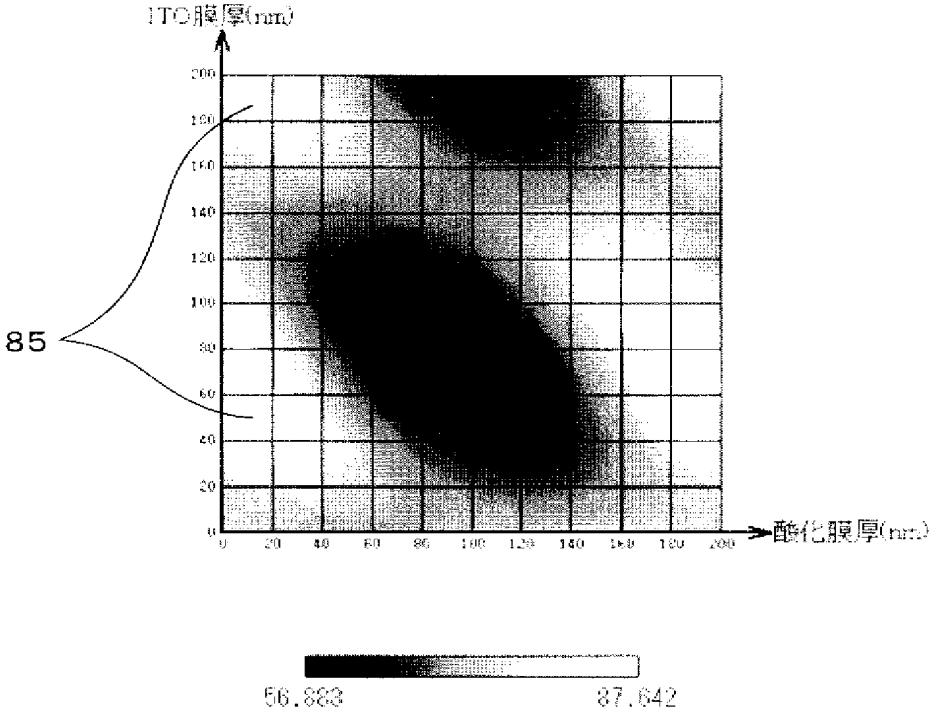
SAMSUNG EX. 1002 - 2805/2862

【図16】



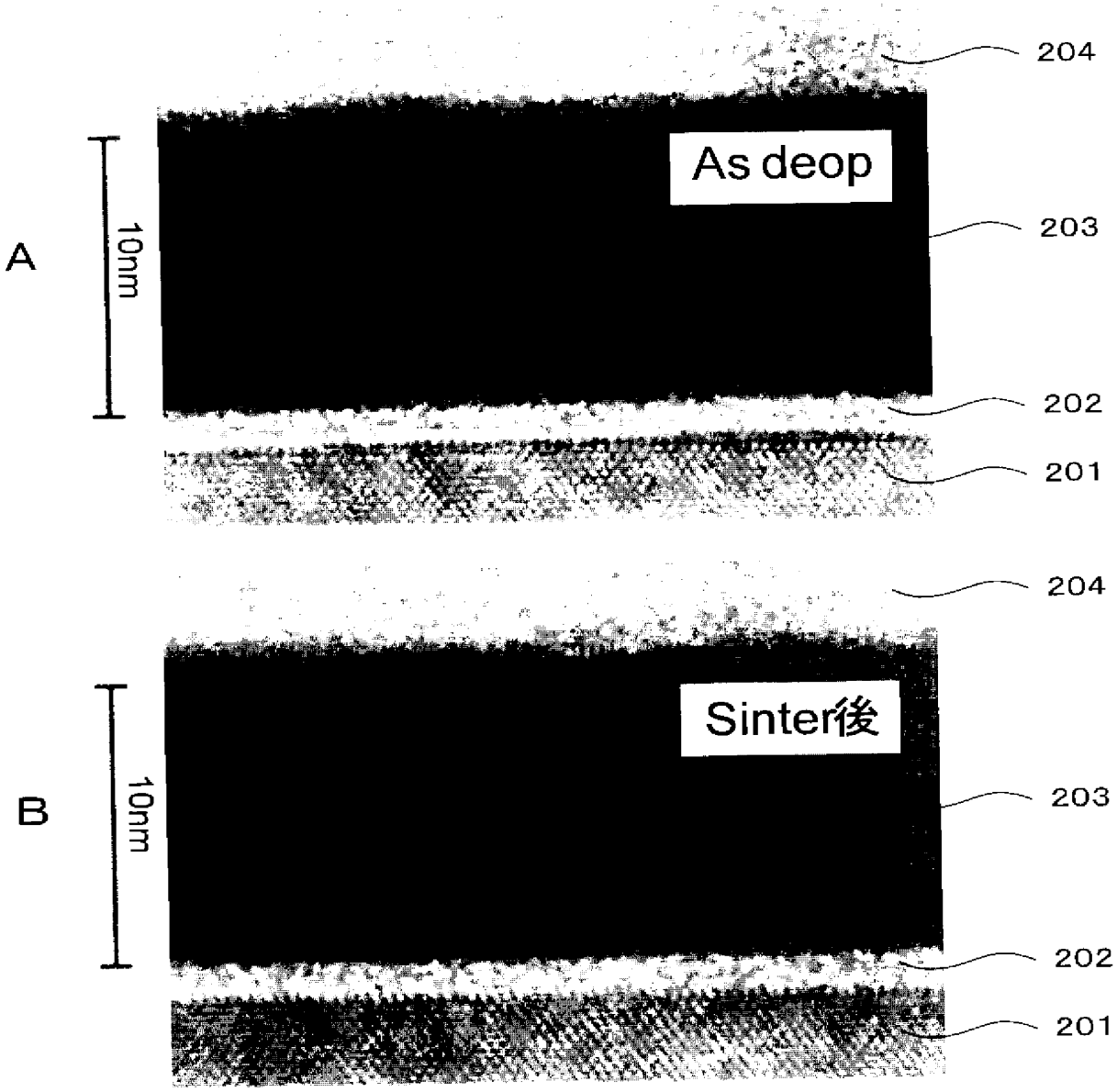
450nmにおけるフォトダイオードへの光の吸収率

【図17】



550nmにおけるフォトダイオードへの光の吸収率

【図27】



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東京都港区港南１丁目７番１号　ソニー株式会社内

Ｆターム(参考) 4M118 AA05 AB01 BA14 CA03 CA04 CA32 CB13 CB14 DB09 DD04
EA14 FA06 FA28 FA33 GA02 GB11 GB15 GB17 GC07 GD04
5C024 CX32 CY47 GX03 GX15 GY31

SAMSUNG EX. 1002 - 2808/2862

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

136549 7590 10/24/2018

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

EXAMINER
PHAM, LONG

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/24/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/216,244	07/21/2016	Martin U. Pralle	143705.05221	5052

TITLE OF INVENTION: Pixel Isolation Elements, Devices and Associated Methods

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	01/24/2019

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

SAMSUNG EX. 1002 - 2809/2862

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

136549 7590 10/24/2018
Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/216,244	07/21/2016	Martin U. Pralle	143705.05221	5052

TITLE OF INVENTION: Pixel Isolation Elements, Devices and Associated Methods

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	01/24/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAM, LONG	2814	257-432000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

SAMSUNG EX. 1002 - 2810/2862

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/216,244	07/21/2016	Martin U. Pralle	143705.05221	5052

136549 7590 10/24/2018

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/24/2018

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

SAMSUNG EX. 1002 - 2811/2862

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

SAMSUNG EX. 1002 - 2812/2862

Notice of Allowability	Application No. 15/216,244	Applicant(s) Pralle et al.	
	Examiner LONG PHAM	Art Unit 2814	AIA Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to AMENDMENT DATED 8/1/2018.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 34,36-52,54-61,63-64 and 67-121 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 8/1/2018.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/LONG PHAM/
Primary Examiner, Art Unit 2814

SAMSUNG EX. 1002 - 2813/2862

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/216,244	Pralle et al.
	Examiner	Art Unit
	LONG PHAM	2814

CPC - Searched*		
Symbol	Date	Examiner
SEE ISSUE CLASSIFICATION	09/25/2018	LP

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
UPDATED TEXT AND INTERFERENCE SEARCHES	09/25/2018	LP

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
H01L	27/1463	09/25/2018	LP

SAMSUNG EX. 1002 - 2814/2862

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/216,244	Pralle et al.
	Examiner	**Art Unit**
	LONG PHAM	2814

CPC						
Symbol					**Type**	**Version**
H01L	/	27	/	1463	F	2013-01-01
H01L	/	27	/	14627	I	2013-01-01
H01L	/	27	/	14629	I	2013-01-01
H01L	/	27	/	14685	I	2013-01-01
H01L	/	27	/	14625	I	2013-01-01
H01L	/	27	/	1462	I	2013-01-01
H01L	/	27	/	14607	I	2013-01-01
H01L	/	27	/	14645	I	2013-01-01
H01L	/	27	/	14689	I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	83	
/LONG PHAM/ Primary Examiner, Art Unit 2814	25 September 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4,6

U.S. Patent and Trademark Office — Part of Paper No.: 20180925

SAMSUNG EX. 1002 - 2815/2862

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/216,244	Pralle et al.
	Examiner	**Art Unit**
	LONG PHAM	2814

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H01L	/	27	/	146

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	83	
/LONG PHAM/ Primary Examiner, Art Unit 2814	25 September 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4,6

U.S. Patent and Trademark Office

Part of Paper No.: 20180925

SAMSUNG EX. 1002 - 2816/2862

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/216,244	Pralle et al.
	Examiner	**Art Unit**
	LONG PHAM	2814

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	34	12	46	23	58	34	72	45	83	56	94	67	105	78	116
2	36	13	47	24	59	35	73	46	84	57	95	68	106	79	117
3	37	14	48	25	60	36	74	47	85	58	96	69	107	80	118
4	38	15	49	26	61	37	75	48	86	59	97	70	108	81	119
5	39	16	50	27	63	38	76	49	87	60	98	71	109	82	120
6	40	17	51	28	64	39	77	50	88	61	99	72	110	83	121
7	41	18	52	29	67	40	78	51	89	62	100	73	111		
8	42	19	54	30	68	41	79	52	90	63	101	74	112		
9	43	20	55	31	69	42	80	53	91	64	102	75	113		
10	44	21	56	32	70	43	81	54	92	65	103	76	114		
11	45	22	57	33	71	44	82	55	93	66	104	77	115		

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	83	
/LONG PHAM/ Primary Examiner, Art Unit 2814	25 September 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4,6

U.S. Patent and Trademark Office

Part of Paper No.: 20180925

SAMSUNG EX. 1002 - 2817/2862

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/216,244	Pralle et al.
	Examiner	**Art Unit**
	LONG PHAM	2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/07/2016	02/06/2017	06/10/2017	02/15/2018	09/25/2018				
	34	÷	✓	✓	✓	=				
	35	÷	✓	✓	O	-				
	36	÷	✓	✓	✓	=				
	37	÷	✓	✓	✓	=				
	38	÷	✓	✓	O	=				
	39	÷	✓	✓	✓	=				
	40	÷	✓	✓	✓	=				
	41	÷	✓	✓	✓	=				
	42	÷	✓	✓	✓	=				
	43	÷	✓	✓	✓	=				
	44	÷	✓	✓	✓	=				
	45	÷	✓	✓	✓	=				
	46	÷	✓	✓	✓	=				
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	49	÷	✓	✓	✓	=				
	50	÷	✓	✓	✓	=				
	51	÷	✓	✓	✓	=				
	52	÷	✓	✓	✓	=				
	53	÷	✓	✓	✓	-				
	54	÷	✓	✓	✓	=				
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	61		✓	✓	✓	=				
	62		O	-		-				
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	64		✓	✓	✓	=				
	65		O	-		-				
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	67				✓	=				
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	73					=				
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	75					=				

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/216,244	Pralle et al.
	Examiner	**Art Unit**
	LONG PHAM	2814

CLAIM		DATE								
Final	Original	09/07/2016	02/06/2017	06/10/2017	02/15/2018	09/25/2018				
	76					=				
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	120					=				
	121					=				

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	45	("0969984" | "20050184291" | "20050184353" | "20080191296" | "20080303932" | "20090090988" | "20090096049" | "20090200625" | "20090278967" | "20100108864" | "20100128161" | "20100201834" | "20110241148" | "20110241152" | "20120025199" | "20120049306" | "20120147241" | "20120153127" | "20120153128" | "20120188431" | "20120217602" | "20120228473" | "20130020468" | "20130207212" | "20140054662" | "20140374868" | "20170244920" | "4546945" | "5583704" | "5802091" | "6131511" | "6131512" | "6479093" | "6690968" | "7315014" | "7728274" | "8268403" | "8445950" | "8445985" | "8530264" | "8604405" | "8729678" | "8928784" | "9064762" | "9478572").PN.	US-PGPUB; USPAT	OR	ON	2018/09/25 13:45
L2	1	("20160329366").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/25 13:57
L3	9556	H01L27/1463.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/25 14:06
L5	0	H01L27/14637.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/25 14:06
L6	17402	H01L27/14627.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/25 14:06
L7	4188	H01L27/14629.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/25 14:06

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L8	12683	H01L27/14685.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/25 14:06
L9	12130	H01L27/14625.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/25 14:06
L10	4452	H01L27/1462.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/25 14:06
L11	2461	H01L27/14607.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/25 14:06
L12	7967	H01L27/14645.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/25 14:07
L13	11554	H01L27/14689.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/25 14:07
S2	84	US-3035052-$.DID. OR US-20030029495-$.DID. OR US-20040222187-$.DID. OR US-20050127401-$.DID. OR US-20050227390-$.DID. OR US-20060011955-$.DID. OR US-20060079062-$.DID. OR US-20060118781-$.DID. OR US-20060180885-$.DID. OR US-20060231914-$.DID. OR US-20070145505-$.DID. OR US-20080026550-$.DID. OR US-20080036022-$.DID. OR US-20080044943-$.DID. OR US-20080076240-$.DID. OR US-20080099804-$.DID. OR US-20080178932-$.DID. OR US-20080258604-$.DID. OR US-20090065051-$.DID. OR US-20090142879-$.DID. OR US-	US-PGPUB; USPAT; USOCR; JPO; IBM_TDB	OR	ON	2014/06/25 14:14

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		20090160983-$.DID. OR US-20090194671-$.DID. OR US-20090200586-$.DID. OR US-20090213883-$.DID. OR US-3487223-$.DID. OR US-4277793-$.DID. OR US-4419533-$.DID. OR US-4493942-$.DID. OR US-4514582-$.DID. OR US-4536608-$.DID. OR US-4663188-$.DID. OR US-4829013-$.DID. OR US-5080725-$.DID. OR US-5081049-$.DID. OR US-5100478-$.DID. OR US-5114876-$.DID. OR US-5164324-$.DID. OR US-5322988-$.DID. OR US-5346850-$.DID. OR US-5597621-$.DID. OR US-5714404-$.DID. OR US-5731213-$.DID. OR US-5792280-$.DID. OR US-6147297-$.DID. OR US-6498336-$.DID. OR US-6580053-$.DID. OR US-6583936-$.DID. OR US-6667528-$.DID. OR US-6759262-$.DID. OR US-6800541-$.DID. OR US-7057256-$.DID. OR US-7091411-$.DID. OR US-7109517-$.DID. OR US-7247527-$.DID. OR US-7314832-$.DID. OR US-7354792-$.DID. OR US-7390689-$.DID. OR US-7442629-$.DID. OR US-7456452-$.DID. OR US-7482532-$.DID. OR US-7498650-$.DID. OR US-7504325-$.DID. OR US-7504702-$.DID. OR US-7511750-$.DID. OR US-7745901-$.DID. OR US-7781856-$.DID. OR US-7816220-$.DID. OR US-7847253-$.DID. OR US-7884439-$.DID. OR US-7884446-$.DID. OR US-8030726-$.DID. OR US-8058615-$.DID. OR US-8207051-$.DID. OR US-8476681-$.DID. OR US-3666484-$.DID. OR US-2030766-$.DID. OR JP-07173484-$.DID. OR JP-071734840721-$.DID. OR JP-2008187003-$.DID. OR JP-2011091128-$.DID. OR JP-2152226-$.DID. OR JP-63116421-$.DID. OR JP-9298308-$.DID. OR KR-20010061058-$.DID. OR KR-20100118864-$.DID. OR WO-2006086014-$.DID. OR WO-2009100023-$.DID. OR WO-2011035188-$.DID. OR WO-2011119618-$.DID.				
S3	7768	(light adj2 (trapping or trapped))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 14:16
S4	11	S2 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 14:16

S5	2251	(reflector or Bragg) and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:40
S6	14	(reflector or Bragg) and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:41
S7	888	(reflector or Bragg) near3 backside	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:55
S8	51623	(reflector or Bragg) near3 (side or sidewall or edge or wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:55
S9	112640	pixel near5 (side or sidewall or edge or wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:56
S10	143	S7 same S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:56
S11	2	S9 same4 S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:56
S12	3	S9 and S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:57
S13	1	S12 not S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2014/06/25 15:57

			DERWENT; IBM_TDB			
S14	179	S7 same4 S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:58
S15	145	S14 and (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:59
S16	129	S14 same10 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:59
S17	128	S14 same8 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:59
S18	1204	(reflector or Bragg) near5 backside	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S19	71202	(reflector or Bragg) near5 (side or sidewall or edge or wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S20	280	S18 same4 S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S21	195	S20 same4 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S22	7	S18 same2 S9	US-PGPUB; USPAT; USOCR;	OR	ON	2014/06/25 16:10

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S23	7	S22 same4 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:10
S24	217	S18 same S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:13
S25	0	(light adj2 sensitive adj2 pixel) same4 S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:14
S26	0	(light adj2 sensitive adj2 pixel) and S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:14
S27	14	pixel same4 S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:14
S28	7	S27 and index	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:18
S29	26925	(high adj2 index) near3 (layer or film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:48
S30	27823	(low adj2 index) near3 (layer or film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:48
S31	12802	S29 near10 S30	US-PGPUB;	OR	ON	2014/06/26

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			12:48
S32	1170	(reflector or Bragg) same S31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:49
S33	611	(reflector or Bragg) near10 S31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:49
S34	4200	S30 near5 ("between")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:49
S35	1972	S34 near10 S29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:50
S36	81	(reflector or Bragg) near10 S35	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:50
S37	188	S29 near5 (polysilicon or polycrystalline or poly or (amorphous adj2 silicon) or germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:53
S38	2500	S30 near5 (oxide or nitride or oxynitride or oxynitrides)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:53
S39	14	S37 near20 S38	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2014/06/26 12:53

			IBM_TDB			
S40	0	(reflector or Bragg) same S39	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:54
S41	0	S39 near20 ("between")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:54
S42	51	backside near6 (textured near2 (layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:12
S43	10	S42 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:25
S44	5	S39 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:25

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		H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.)				
S45	2	S36 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:25
S46	1	("20140138785").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:26
S47	3930	(257/432).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:54
S48	218	(257/228).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:54
S50	1	("9373732").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/07/13 15:10
S51	1	("9373732").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/07/15 10:13
S52	395	reflective near3 (aluminum adj oxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/15 13:07
S53	35214	(rough or textured) near2 (layer or film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:24
S54	44833	light adj2 incident adj2 surface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:24
S55	38	S53 same S54	US-PGPUB;	OR	ON	2017/02/06

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			01:25
S56	10	S55 same efficiency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:25
S57	0	S55 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:29
S58	0	S55 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:30
S59	3	S55 same (metal or polysilicon or amorphous)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:30
S60	1864	S53 same efficiency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:32
S61	42	S60 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:32
S62	351	S60 same ((silicon adj oxide) or "SiO" or (silicon adj nitride) or "SiN" or metal or polysilicon or amorphous)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 01:32
S63	85	S62 same4 incident	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2017/02/06 01:33

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			IBM_TDB			
S64	228102	(reflective near2 (material or layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:11
S65	530599	("AlO" or (aluminum adj oxide)) or ("HfO" or (hafnium adj oxide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:12
S66	403	S64 near3 S65	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:12
S67	2	S66 near4 (benefit or beneficial or advantages or advantageous or advantegeously)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:13
S68	2	S66 near10 (benefit or beneficial or advantages or advantageous or advantegeously)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:13
S69	31128	(anti or non) near2 S64	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:20
S70	121	S65 near4 S69	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:20
S71	2	S70 same (benefit or beneficial or advantages or advantageous or advantegeously)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 11:20
S72	2	(dope or doping or implanting or implant or implants implantation or dopes) near2 (light adj incident adj surface)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2017/02/06 12:04

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			EPO; JPO; DERWENT; IBM_TDB			
S73	6	(dope or doping or implanting or implant or implants implantation or dopes) near2 (light adj2 incident adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:05
S74	13	(dope or doping or implanting or implant or implants implantation or dopes) near4 (light adj2 incident adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:05
S75	167141	(doped or implanted) adj2 (region or section or portion or part)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:13
S76	1	S75 near4 (light adj2 incident adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:13
S77	26	S75 near10 (light adj2 incident adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:15
S78	25	S77 not S76	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 12:15
S79	1	("9064764").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/02/06 12:20
S80	44833	(light adj2 incident adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 17:49
S81	167141	(doped or implanted) adj2 (region or section or portion or part)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2017/02/06 17:49

			IBM_TDB			
S82	9	S80 near6 S81	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 17:49
S83	364064	(light adj2 surface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 17:50
S84	54	S83 near4 S81	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 17:50
S85	53	S84 not S82	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/02/06 17:50
S86	21	("20030214595" | "20030228883" | "20050093100" | "20060086956" | "20060128087" | "20070189583" | "20070237504" | "20080158398" | "20080192133" | "20080284884" | "20100200658" | "20110194100" | "20110292380" | "20140198240" | "5101260" | "5600130" | "5626687" | "5635089" | "6082858" | "6204506" | "6907135").PN.	US-PGPUB; USPAT	OR	ON	2017/02/07 07:43
S87	21	("20030214595" | "20030228883" | "20050093100" | "20060086956" | "20060128087" | "20070189583" | "20070237504" | "20080158398" | "20080192133" | "20080284884" | "20100200658" | "20110194100" | "20110292380" | "20140198240" | "5101260" | "5600130" | "5626687" | "5635089" | "6082858" | "6204506" | "6907135").PN.	US-PGPUB; USPAT	OR	ON	2017/02/07 07:44
S88	20	("20010044266" | "20050088634" | "20080173620" | "20090027640" | "20090093100" | "20090114630" | "20090308457" | "20100140768" | "20130135439" | "4886958" | "5351446" | "5641969" | "5727096" | "6327022" | "6331885" | "6340281" | "7800684" | "7897942" | "9184204" | "9369641").PN.	US-PGPUB; USPAT	OR	ON	2017/06/01 13:32
S89	20	("20040256561" | "20070063219" | "20070103580" | "20070125951" | "20080142686" | "20090009596" |	US-PGPUB; USPAT	OR	ON	2018/02/15 10:41

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		"20090174026" | "20090242019" | "20100102366" | "20110003424" | "20110019050" | "20120080733" | "20120274744" | "20140352779" | "20150076468" | "5236863" | "5410168" | "8076746" | "9419159" | "9673250").PN.				
S90	24107	(layer or film) near3 (different near2 (refractive or refraction or refracting))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:45
S91	18	S90 near4 isolation	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:45
S92	5	S91 same4 (pixel or pixels)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:45
S93	13	S91 not S92	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:47
S94	22683	bragg adj2 (reflective or reflector)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:51
S95	58	S94 near4 isolation	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:52
S96	6	S95 same4 (pixel or pixels)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:52
S97	52	S95 not S96	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2018/02/15 10:55

			DERWENT; IBM_TDB			
S98	29452	(isolation or isolating or insulation or insulating) near2 (multi-layer or multiple)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:57
S99	19	S98 near10 (different near2 (refractive or refraction or refracting))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 10:58
S100	48	S98 near3 (silicon adj2 dioxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 13:05
S101	1	S100 same4 (pixel or pixels)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 13:05
S102	19531	(isolation or isolating or insulation or insulating) near2 (silicon adj2 dioxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 13:08
S103	53	S102 near4 (benefit or advantage or beneficial or advantageous)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 13:08
S104	4006	(isolation or isolating or insulation or insulating) near2 ("Al.sub.2O.sub.3")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 13:10
S105	450872	aluminum adj oxide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 13:11
S106	57928	hafnium adj oxide	US-PGPUB; USPAT; USOCR;	OR	ON	2018/02/15 13:11

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S107	2014	(isolation or isolating or insulation or insulating) near6 S105 near6 S106	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/15 13:11

9/ 25/ 2018 2:07:39 PM
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SAMSUNG EX. 1002 - 2835/2862

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	PHAM, LONG
Attorney Docket Number	143705.05221

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4546945		1985-10-15	Nessfield	
	2	5583704		1996-12-10	Fujii	
	3	5802091		1998-08-01	Chakrabarti et al	
	4	6131511		2000-10-17	Wachi et al	
	5	6131512		2000-10-17	Verlinden et al	
	6	6479093		2002-11-12	Lauffer et al	
	7	6690968		2004-02-10	Mejia	
	8	7315014		2008-01-01	Lee et al	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.P./

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	9	7728274		2010-06-01	Pilla et al	
	10	8268403		2007-04-30	Akiyama et al	
	11	8445950		2013-05-21	Iida et al	
	12	8445985		2013-05-21	Hiyama et al	
	13	8530264		2013-09-10	De Munck et al	
	14	8604405		2013-12-10	Liu et al	
	15	8729678		2014-05-20	Shim et al	
	16	8928784		2015-01-06	Watanabe et al	
	17	9064762		2015-06-23	Yamaguchi	
	18	9478572		2016-10-25	Miyanami	
	19	9659984		2017-05-23	Ohkubo et al	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	2	20050184353		2005-08-25	Mouli	
	3	20080303932		2008-12-11	Wang et al	
	4	20080191296		2008-08-14	Wang et al.	
	5	20090090988		2009-04-09	OHGISHI	
	6	20090096049		2009-04-16	Oshiyama et al	
	7	20090278967		2009-11-12	Toumiya	
	8	20090200625		2009-08-13	Venezia et al.	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
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Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	PHAM, LONG
Attorney Docket Number	143705.05221

	10	20100128161		2010-05-27	Yamaguchi	
	11	20100201834		2010-08-12	Maruyama et al.	
	12	20110241148		2011-10-06	Hiyama et al	
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	14	20120025199		2012-02-02	Chen et al	
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	17	20120188431		2012-07-26	Takimoto	
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	19	20120049306		2012-03-01	Ohba et al.	
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	21	20130020468		2013-01-24	Mitsuhashi et al	
	22	20130207212		2013-08-15	Mao et al	
	23	20140374868		2014-12-25	LEE et al	
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	25	20170244920		2017-08-24	Ohkubo et al	
	26	20120147241	A1	2012-06-14	YAMAGUCHI TETSUJI	

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
1	1	101241923	CN		2008-08-13	TAIWAN SEMICONDUCTOR MFG	See corresponding US2008191296	☐
2	2	101465361	CN		2009-06-24	TAIWAN SEMICONDUCTOR MFG		☒
3	3	101740597	CN		2010-06-16	SONY CORP	See corresponding US2010128161	☐

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SAMSUNG EX. 1002 - 2840/2862

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First Named Inventor	Martin U. Pralle
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Examiner Name	PHAM, LONG
Attorney Docket Number	143705.05221

4	4	101978498	CN		2011-02-16	OMNIVISION TECH INC	See corresponding US2009200625	☐
5	5	102270646	CN		2011-12-07	NA		☒
6	6	201725796	CN		2011-01-26	GALAXYCORE INC		☒
7	7	2011003860	JP		2011-01-06	SONY CORP	See corresponding US2010201834	☐
8	8	2012054321	JP		2012-03-15	SONY CORP	See corresponding US2012049306	☐
9	9	2012169530	JP		2012-09-06	SONY CORP		☒
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11	11	20060020400	KR		2006-03-06	MAGNACHIP SEMICONDUCTOR LTD		☒
12	12	20080014301	KR		2008-02-14	SAMSUNG ELECTRONICS CO LTD		☒
13	13	20080097709	KR		2008-11-06	DONGBU ELECTRONICS CO LTD		☒
14	14	20110079323	KR		2011-07-07	DONGBU HITEK CO LTD		☒

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15	15	20170070266	KR		2017-06-21	SONY CORP	See corresponding US2014054662	☐
16	16	2012117931	WO		2012-09-07	SONY CORPORATION	See corresponding US2014054662	☐
	17	2007258684	JP		2007-10-04	SONY CORP	See corresponding US20120147241	☐

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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Byung Jun Park et al, Jpn. J. Appl. Phys. 46 2454, 2007, 5 pages.	☐
	2	Choubey et al., On Evolution of CMOS Image Sensors, Proceedings of the 8th International Conference on Sensing Technology, Sep. 2-4, 2014, Liverpool, UK, pages.	☐
	3	Fontaine, Ray, A Survey of Enabling Technologies in Successful Consumer Digital Imaging Products (Part 3: Pixel Isolation Structures), http://www.techinsights.com,July 24, 2017, 13 pages.	☐
	4	IMEC, 3D INTEGRATED IMAGE SENSORS FOR SMART IMAGING SYSTEMS, PIET DE MOOR, 2010, 32 pages.	☐
	5	KOREAN INTELLECTUAL PROPERTY OFFICE (KIPO), CMOS Image Sensor, KIPO, 2004, 29 pages.	☐
	6	MUNCK, Generic building blocks for 3D integration and their application on hybrid CMOS image sensors, KATHOLIEKE UNIVERSITEIT LEUVEN, Kapeldreef 75 — B-3001 Heverlee, September 2008, 328 pages.	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.P./

SAMSUNG EX. 1002 - 2842/2862

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Attorney Docket Number	143705.05221

	7	Rao, et al., Monolithic and Fully-Hybrid Backside Illuminated CMOS Imagers for Smart Sensing, IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, 4 pages.	☐
	8	STMicroelctronics, BSI – technical challenges, IISW-2009, Bergen. 25th June 2009, 37 pages.	☐
	9	https://blogs.yahoo.co.jp/miyabiman_now/25628945.html	☐
	10	Agranov, et al., Pixel continues to shrink….Small Pixels for Novel CMOS Image Sensors, 4 pages.	☐
	11	Fontaine, A Review of the 1.4 µm Pixel Generation, Technology Analysis Group Chipworks Inc., 2011, 4 pages.	☐
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	14	Tournier, et al., Pixel-to-Pixel isolation by Deep Trench technology: Application to CMOS Image Sensor, https://www.researchgate.net/publication/268300742, 2011, 5 pages.	☐
	15	B.J. Park et al., "Deep Trench Isolation for Crosstalk Suppression in Active Pixel Sensors with 1.7µm Pixel Pitch", in Japanese Journal of Applied Physics, Vol. 46, No. 4B, pp. 2454-5457, 2007	☐
	16	D. N. Yaung et al., "High performance 300mm backside illumination technology for continuous pixel shrinkage," 2011 International Electron Devices Meeting, Washington, DC, 2011, pp. 8.2.1-8.2.4.	☐
	17	http://electroiq.com/insights-from-leading-edge/2016/09/iftle-303-sony-introduces-ziptronix-dbi-technology-in-samsung-galaxy-s7, "Omnivision was the first to sample BSI in 2007 but costs were too high and adoption was thus very low", (2016)	☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Art Unit	2814
	Examiner Name	PHAM, LONG
	Attorney Docket Number	143705.05221

	18	http://joseph-tang.blogspot.com/2017/, Oshiyama et al. , Near-infrared Sensitivity Enhancement of a Back-illuminated Complementary Metal Oxide Semiconductor Image Sensor with a Pyramid Surface for Diffraction Structure,(2017)	☐
	19	K. Itonaga et al., "Extremely-low-noise CMOS Image Sensor with high saturation capacity," 2011 International Electron Devices Meeting, Washington, DC, 2011, pp. 8.1.1-8.1.4.	☐
	20	K. Minoglou et al., "Reduction of Electrical Crosstalk in Hybrid Backside Illuminated CMOS Imagers using Deep Trench Isolation," 2008 International Interconnect Technology Conference, Burlingame, CA, USA, 2008, pp. 129-131.	☐
	21	Y. Kitamura et al., "Suppression of crosstalk by using backside deep trench isolation for 1.12μm backside illuminated CMOS image sensor," 2012 International Electron Devices Meeting, San Francisco, CA, 2012, pp. 24.2.1-24.2.4.	☐

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EXAMINER SIGNATURE

Examiner Signature	/LONG PHAM/	Date Considered	09/25/2018

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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Art Unit	2814
Examiner Name	PHAM, LONG
Attorney Docket Number	143705.05221

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Reza Mollaaghababa, Reg. No. 43810/	Date (YYYY-MM-DD)	2018-07-31
Name/Print	Reza Mollaaghababa	Registration Number	43810

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.P./

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.E./

SAMSUNG EX. 1002 - 2846/2862

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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BIB DATA SHEET

CONFIRMATION NO. 5052

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/216,244	07/21/2016	257	2814	143705.05221

APPLICANTS

SiOnyx, LLC., Beverly, MA;

INVENTORS

Martin U. Pralle, Wayland, MA;
Jeffrey McKee, Tualatin, OR;
Jason Sickler, Arlington, MA;

**** CONTINUING DATA ***************************

This application is a CON of 14/747,875 06/23/2015 PAT 9905599
which is a CON of 13/841,120 03/15/2013 PAT 9064764
which claims benefit of 61/614,275 03/22/2012

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

08/03/2016

Foreign Priority claimed ❑ Yes ☑ No 35 USC 119(a-d) conditions met ❑ Yes ☑ No Verified and Acknowledged /LONG PHAM/ Examiner's Signature	❑ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		MA	4	26	2

ADDRESS

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736
UNITED STATES

TITLE

Pixel Isolation Elements, Devices and Associated Methods

FILING FEE RECEIVED		
2560	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other _____ ❑ Credit

SAMSUNG EX. 1002 - 2847/2862

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

136549 7590 10/24/2018
Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/216,244	07/21/2016	Martin U. Pralle	143705.05221	5052

TITLE OF INVENTION: Pixel Isolation Elements, Devices and Associated Methods

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	01/24/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAM, LONG	2814	257-432000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Thomas J. Engellenner
2 Reza Mollaaghababa
3 Pepper Hamilton LLP

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: SiOnyx, LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Beverly, MA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 500436

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Andrew W. Schultz/ Date January 22, 2019

Typed or printed name Andrew W. Schultz Registration No. 66869

SAMSUNG EX. 1002 - 2848/2862

Electronic Patent Application Fee Transmittal

Application Number:	15216244
Filing Date:	21-Jul-2016
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Filer:	Andrew W. Schultz/Irene Gommerstadt
Attorney Docket Number:	143705.05221

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1000**

Electronic Acknowledgement Receipt

EFS ID:	34916852
Application Number:	15216244
International Application Number:	
Confirmation Number:	5052
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	136549
Filer:	Andrew W. Schultz/Irene Gommerstadt
Filer Authorized By:	Andrew W. Schultz
Attorney Docket Number:	143705.05221
Receipt Date:	22-JAN-2019
Filing Date:	21-JUL-2016
Time Stamp:	11:39:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	012219INTEFSW11414000
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Issue_Fee.pdf	90126 5a0d93900d9a98b5d461aea7d1225b99f807b132	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30144 7b838dfda5629299099370965621 1d7787b875c0	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	120270		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Attorney Docket Number	143705.05221

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5236863		1993-08-17	Iranmesh	
	2	5410168		1995-04-25	Hisa	
	3	8076746		2011-12-13	McCarten et al.	
	4	9419159		2016-08-16	Sakamoto et al.	
Change(s) applied to document, /D.W./ 12/1/2018	5	9673250		2017-06-06	Haddad et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20040256561		2004-12-23	Beuhler et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH.

SAMSUNG EX. 1002 - 2853/2862

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15216244
	Filing Date	2016-07-21
	First Named Inventor	Martin U. Pralle
	Art Unit	2814
	Examiner Name	Long Pham
	Attorney Docket Number	143705.05221

	9	7897942		2011-03-01	Bereket	
	10	9184204		2015-11-10	Hu	
	11	9369641		2016-06-14	Hu	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20010044266		2001-11-22	Katsuoka	
	2	20050088634		2005-04-28	Kosugi	
Change(s) applied to document, /K.B./ 12/5/2018	3	20090093100		04/2009 ~~2005-05-06~~	Xia, et al. ~~Chen~~	
	4	20080173620		2008-07-24	Grek	
	5	20090027640		2009-01-29	Shibazaki	
	6	20090114630		2009-05-07	Hawryluk	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /K.B./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Change(s) applied to document, /K.B./ 12/5/2018

Application Number	15216244
Filing Date	2016-07-21
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	PHAM, LONG
Attorney Docket Number	143705.05221

	9	7728274		2010-06-01	Pilla et al	
	10	8268403		09/2012 ~~2007-04-30~~	Akiyama et al	
	11	8445950		2013-05-21	Iida et al	
	12	8445985		2013-05-21	Hiyama et al	
	13	8530264		2013-09-10	De Munck et al	
	14	8604405		2013-12-10	Liu et al	
	15	8729678		2014-05-20	Shim et al	
	16	8928784		2015-01-06	Watanabe et al	
	17	9064762		2015-06-23	Yamaguchi	
	18	9478572		2016-10-25	Miyanami	
	19	9659984		2017-05-23	Ohkubo et al	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /K.B./

SAMSUNG EX. 1002 - 2855/2862

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/216,244	03/05/2019	10224359	143705.05221	5052

136549 7590 02/13/2019

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Martin U. Pralle, Wayland, MA;
SiOnyx, LLC., Beverly, MA;
Jeffrey McKee, Tualatin, OR;
Jason Sickler, Arlington, MA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

SAMSUNG EX. 1002 - 2856/2862

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	15/216,244
Filing Date	21-Jul-2016
First Named Inventor	Martin U. PRALLE
Title	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
Art Unit	
Examiner Name	
Attorney Docket Number	143705.000333

SIGNATURE of Applicant or Patent Practitioner

Signature	/Gunnar G. Leinberg/	Date (Optional)	2022-09-01
Name	Gunnar G. Leinberg	Registration Number	35,584
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 11951

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

SiOnyx, LLC

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	
Name	Steven D. Saylor		
Title	President and CEO		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	46533426
Application Number:	15216244
International Application Number:	
Confirmation Number:	5052
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	136549
Filer:	Gunnar G. Leinberg/Mary Frances Heeks
Filer Authorized By:	Gunnar G. Leinberg
Attorney Docket Number:	143705.05221
Receipt Date:	01-SEP-2022
Filing Date:	21-JUL-2016
Time Stamp:	11:37:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	20220901_Corrected_POA_with_Transmittal_143705_000333.pdf	328413 ba00e26ae497a77188fac64ce06b19f33302a034	no	2

Warnings:

Information:	
Total Files Size (in bytes):	328413

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/216,244	07/21/2016	Martin U. Pralle	143705.05221

CONFIRMATION NO. 5052

POWER OF ATTORNEY NOTICE

136549
Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

OC000000136285881

Date Mailed: 09/16/2022

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/01/2022.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/hsarwari/

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/216,244	07/21/2016	Martin U. Pralle	143705.000333

CONFIRMATION NO. 5052

POA ACCEPTANCE LETTER

11951
Troutman Pepper Hamilton Sanders LLP (Rochester)
70 Linden Oaks
Suite 210
Rochester, NY 14625

OC000000136285898

Date Mailed: 09/16/2022

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/01/2022.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/hsarwari/

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