

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Samsung Electronics Co., Ltd.,
Petitioner,

v.

SiOnyx, LLC,
Patent Owner.

Case No. IPR2025-00163
Patent No. 10,224,359

**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO.
10,224,359 UNDER 35 U.S.C. §§ 311–319 AND 37 C.F.R. § 42.100 *et seq.***

Petition B, Based on Primary Reference of Hwang

Table of Contents

I.	Introduction.....	1
II.	Standing, Mandatory Notices, and Fee Authorization	1
A.	Grounds for Standing	1
B.	Real Parties-in-Interest.....	1
C.	Related Matters.....	1
D.	Counsel Information.....	1
E.	Service Information.....	2
F.	Payment of Fees Under 37 C.F.R. §42.103.....	2
III.	Summary of Challenge	3
IV.	Overview of the '359 Patent.....	5
V.	Level of Ordinary Skill.....	7
VI.	Claim Construction.....	7
VII.	Application of Prior Art to the Challenged Claims.....	8
A.	Ground 1: Claims 1-5, 7, 10, 18, 23, 25, 38-43, 45-50, 52-64, 67-70, 73-75, and 80-83 Are Anticipated or Rendered Obvious by Hwang	8
1.	Overview of Hwang.....	8
2.	Claim 1	9
a)	Element 1[pre]: “An imager device, comprising:”	9
b)	Element 1[a]: “at least two adjacent light sensitive image sensor pixels each having a light incident surface, and a backside surface opposite the light incident surface;”	9

- c) Element 1[b]: “a peripheral isolation element at least partially separating said two adjacent light sensitive pixels;” 12
- d) Element 1[c]: “each of said pixels having at least one doped region disposed on at least one of the light incident surface and the backside surface,” 13
- e) Element 1[d]: “wherein the peripheral isolation element comprises at least two materials having different indices of refraction,” 15
- f) Element 1[e]: “wherein said peripheral isolation element comprises a first, a second and a third layer,” 15
- g) Element 1[f]: “wherein said third layer is disposed between said first and second layers, and” 17
- h) Element 1[g]: “wherein each of said first and second layer exhibits an index of refraction less than an index of refraction of said third layer.” 17
- 3. Claim 2: “The device of claim 1, wherein the index of refraction of at least one of said first and second layer is at least 0.2 lower relative to the refractive index of the third layer.” ...17
- 4. Claim 3: “The device of claim 1, wherein at least of one of said at least two materials comprises silicon dioxide.” 18
- 5. Claim 4: “The device of claim 1, wherein at least one of said first and second layers comprises silicon dioxide.” 19
- 6. Claim 5: “The device of claim 1, wherein the isolation element extends substantially from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels.” 19
- 7. Claim 7: “The device of claim 1, wherein said peripheral isolation element comprises an oxide.” 22

8.	Claim 10: “The device of claim 1, wherein the peripheral isolation element comprises at least one material having an index of refraction of less than about 2.1.”	22
9.	Claim 18	23
a)	Element 18[pre]: “An imager device, comprising:”	23
b)	Element 18[a]: “at least two adjacent light sensitive image sensor pixels each having a light incident surface, and a backside surface opposite the light incident surface;”	23
c)	Element 18[b]: “a peripheral isolation element separating said at least two adjacent light sensitive pixels so as to reduce optical crosstalk therebetween,”	23
d)	Element 18[c]: “said isolation element comprising at least two materials having different indices of refraction,”	24
e)	Element 18[d]: “at least one doped region disposed on at least one of the light incident surface and the backside surface,”	24
f)	Element 18[e]: “wherein said peripheral isolation element comprises a first, a second and a third layer,”	24
g)	Element 18[f]: “wherein said third layer is disposed between said first and second layers, and”	24
h)	Element 18[g]: “wherein each of said first and second layers exhibits an index of refraction less than an index of refraction of said third layer.”	24
10.	Claim 23: “The device of claim 18, wherein the peripheral isolation element extends from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels.”	25

11. Claim 25: “The device of claim 19, wherein said at least two pixels are formed monolithically in a common semiconductor substrate.” 25
12. Claim 38: “The device of claim 1, wherein each of said at least two adjacent light sensitive image sensor pixels comprises a semiconductor portion providing said light incident surface and said backside surface, wherein said peripheral isolation element isolates the semiconductor portions of said at least two adjacent light sensitive image sensor pixels.” 26
13. Claim 39: “The device of claim 38, wherein said peripheral isolation element optically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.” 28
14. Claim 40: “The device of claim 38, wherein said peripheral isolation element electrically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.” 28
15. Claim 41: “The device of claim 38, wherein an index of refraction of the semiconductor portion of each of said at least two adjacent image sensor pixels is different from indices of refraction of said layers of the peripheral isolation element such that light incident from each of said semiconductor portions on said peripheral isolation element is reflected, thereby providing optical isolation between the pixels.” 29
16. Claim 42: “The device of claim 1, wherein said at least two adjacent light sensitive image sensor pixels are formed monolithically on a common semiconductor substrate and are isolated from one another by said peripheral isolation element.” 30
17. Claim 43: “The device of claim 1, wherein said peripheral isolation element is a trench isolation element.” 31
18. Claim 45: “The device of claim 18, wherein each of said at least two adjacent light sensitive image sensor pixels comprises a semiconductor portion providing said light incident surface and said backside surface, wherein said peripheral isolation

	element isolates the semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”	31
19.	Claim 46: “The device of claim 45, wherein said peripheral isolation element optically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”	31
20.	Claim 47: “The device of claim 46, wherein said peripheral isolation element electrically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”	32
21.	Claim 48: “The device of claim 47, wherein an index of refraction of the semiconductor portion of each of said at least two adjacent image sensor pixels is different from indices of refraction of said layers of the peripheral isolation element such that light incident from each of said semiconductor portions on said peripheral isolation element is reflected, thereby providing optical isolation between the pixels.”	32
22.	Claim 49: “The device of claim 18, wherein said at least two adjacent light sensitive image sensor pixels are formed monolithically on a common semiconductor substrate and are isolated from one another by said peripheral isolation element.”	32
23.	Claim 50: “The device of claim 18, wherein said peripheral isolation element is a trench isolation element.”	32
24.	Claim 52: “The imager device of claim 38, wherein at least one of the first layer and the second layer of said peripheral isolation element and said semiconductor portion of each of said at least two adjacent pixels comprise different materials.”	33
25.	Claim 53: “The imager device of claim 1, wherein the first layer and the second layer of said peripheral isolation element comprise different materials.”	33

26. Claim 54: “The imager device of claim 1, wherein the peripheral isolation element comprises at least three materials.” 37
27. Claim 55: “The imager device of claim 1, wherein the peripheral isolation element comprises more than three layers.” 38
28. Claim 56: “The imager device of claim 1, wherein the peripheral isolation element comprises a light trapping material filling a trench.” 39
29. Claim 57: “The imager device of claim 56, wherein the trench is one of a shallow trench and a deep trench.” 39
30. Claim 58: “The imager device of claim 45, wherein at least one of the first layer and the second layer of the peripheral isolation element and said semiconductor portion of each of said at least two adjacent pixels comprise different materials.” 40
31. Claim 59: “The imager device of claim 18, wherein the first layer and the second layer of said peripheral isolation element comprise different materials.” 40
32. Claim 60: “The imager device of claim 18, wherein the peripheral isolation element comprises at least three materials.” 40
33. Claim 61: “The imager device of claim 18, wherein the peripheral isolation element comprises more than three layers.” 40
34. Claim 62: “The imager device of claim 18, wherein the peripheral isolation element comprises a light trapping material filling a trench.” 40
35. Claim 63: “The imager device of claim 62, wherein the trench is one of a shallow trench and a deep trench.” 41
36. Claim 64: “The imager device of claim 1, wherein said peripheral isolation element comprises a trench isolation

	element formed by filling a trench with said first, said second, and said third layers.”	41
37.	Claim 67: “The imager device of claim 1, wherein said peripheral isolation element is configured to reflect at least a portion of light incident thereon from any of said two adjacent light sensitive pixels back to that pixel.”	42
38.	Claim 68: “The imager device of claim 67, wherein the peripheral isolation element is further configured to optically isolate said two adjacent light sensitive pixels.”	43
39.	Claim 69: “The imager device of claim 68, wherein the peripheral isolation element is further configured to electrically isolate said two adjacent light sensitive pixels.”	43
40.	Claim 70: “The imager device of claim 18, wherein said peripheral isolation element comprises a trench isolation element formed by filling a trench with said first, said second, and said third layers.”	43
41.	Claim 73: “The imager device of claim 18, wherein said peripheral isolation element is configured to reflect at least a portion of light incident thereon from any of said two adjacent light sensitive pixels back to that pixel.”	43
42.	Claim 74: “The imager device of claim 73, wherein the peripheral isolation element is further configured to optically isolate said two adjacent light sensitive pixels.”	44
43.	Claim 75: “The imager device of claim 74, wherein the peripheral isolation element is further configured to electrically isolate said two adjacent light sensitive pixels.”	44
44.	Claim 80: “The imager device of claim 1, wherein the peripheral isolation element comprises five layers.”	44
45.	Claim 81: “The imager device of claim 80, wherein the five layers include the first layer, the second layer, the third layer, a fourth layer disposed between the first layer and one of said adjacent pixels and a fifth layer disposed between the second layer and the other one of said adjacent pixels.”	44

46.	Claim 82: “The imager device of claim 18, wherein the peripheral isolation element comprises five layers.”	46
47.	Claim 83: “The imager device of claim 82, wherein the five layers include the first layer, the second layer, the third layer, a fourth layer disposed between the first layer and one of said adjacent pixels and a fifth layer disposed between the second laer and the other one of said adjacent pixels.”	46
B.	Ground 2: Claims 12-17, 19-22, 26-29, and 76-79 Are Obvious Based on Hwang and Haddad188	47
1.	Overview of Haddad188	47
2.	Motivation to Combine Hwang and Haddad188	48
3.	Claim 12: “The device of claim 1, wherein at least one of said two adjacent light sensitive pixels comprises a textured region.”	52
4.	Claim 13: “The device of claim 12, wherein said textured region is coupled to the light incident surface.”	53
5.	Claim 14: “The device of claim 13, wherein said light incident surface comprises said textured region.”	53
6.	Claim 15: “The device of claim 13, wherein said textured region comprises a textured film layer”	54
7.	Claim 16: “The device of claim 15, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”	54
8.	Claim 17: “The device of claim 12, wherein said backside surface comprises said textured region.”	56
9.	Claim 19: “The device of claim 18, wherein at least one of said light incident surface and said backside surface of at least one of said two adjacent light sensitive pixels comprises a textured region.”	57

10.	Claim 20: “The device of claim 19, wherein said textured region is a textured film layer.”	57
11.	Claim 21: “The device of claim 20, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”	57
12.	Claim 22: “The device of claim 19, wherein said textured region reflects at least a portion of light internally incident thereon into the at least one pixel.”	58
13.	Claim 26: “The device of claim 19, wherein the textured region is formed by laser radiation.”	58
14.	Claim 27: “The device of claim 12, wherein the textured region is formed by one of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.”	59
15.	Claim 28: “The device of claim 12, wherein the textured region is formed by laser radiation.”	59
16.	Claim 29: “The device of claim 12, wherein said textured region is coupled to the backside surface.”	60
17.	Claim 76: “The imager device of claim 1, wherein the peripheral isolation element comprises a textured region.”	60
18.	Claim 77: “The imager device of claim 1, wherein the peripheral isolation element further comprises a first textured region between the first layer and one of said adjacent pixels and a second textured region between the second layer and the other one of said adjacent pixels.”	60
19.	Claim 78: “The imager device of claim 18, wherein the peripheral isolation element comprises a textured region.”	62
20.	Claim 79: “The imager device of claim 18, wherein the peripheral isolation element further comprises a first textured region between the first layer and one of said adjacent pixels	

and a second textured region between the second layer and the other one of said adjacent pixels.” 62

C.	Ground 3: Claims 6, 8, 9, 11, 24, 30, 32, 34, and 36 Are Obvious Based on Hwang and Shinohara.....	62
1.	Overview of Shinohara	62
2.	Motivation to Combine Hwang and Shinohara	64
3.	Claim 6: “The device of claim 1, wherein at least one of the first and second layer comprises Al ₂ O ₃ .”.....	67
4.	Claim 8: “The device of claim 1, wherein said peripheral isolation element provides a passivating negative charge.”	68
5.	Claim 9: “The device of claim 1, wherein said peripheral isolation element exhibits a surface recombination velocity as low as 10 cm/s.”	68
6.	Claim 11: “The device of claim 1, wherein the peripheral isolation element comprises any of aluminum oxide and hafnium oxide.”	69
7.	Claim 24: “The device of claim 18, wherein said at least two materials comprises silicon dioxide and aluminum oxide.”	69
8.	Claim 30: “The device of claim 1, wherein said peripheral isolation element comprises tantalum oxide.”	70
9.	Claim 32: “The device of claim 1, wherein said peripheral isolation element comprises lanthanum oxide.”	70
10.	Claim 34: “The device of claim 18, wherein said peripheral isolation element comprises tantalum oxide.”	71
11.	Claim 36: “The device of claim 18, wherein said peripheral isolation element comprises lanthanum oxide.”	71
D.	Ground 4: Claims 44, 51, 65-66, and 71-72 Are Obvious Based on Hwang and Roy	71
1.	Overview of Roy	71

2.	Motivation to Combine Hwang and Roy	73
3.	Claim 44: “The device of claim 1, wherein said peripheral isolation element has a width in a range from about 100 nm to about 50 microns.”	75
4.	Claim 51: “The device of claim 18, wherein said peripheral isolation element has a width in a range from about 100 nm to about 50 microns.”	75
5.	Claim 65: “The imager device of claim 64, wherein said trench isolation element has a depth in a range of about 100 nm to about 50 microns.”	75
6.	Claim 66: “The imager device of claim 65, wherein said trench isolation element has a width in a range of about 100 nm to about 10 microns.”	76
7.	Claim 71: “The imager device of claim 70, wherein said trench isolation element has a depth in a range of about 100 nm to about 50 microns.”	76
8.	Claim 72: “The imager device of claim 71, wherein said trench isolation element has a width in a range of about 100 nm to about 10 microns.”	77
VIII.	Discretionary Denial Is Inappropriate	77
IX.	Conclusion	78

List of Exhibits

Exhibit	Description
1001	U.S. Patent No. 10,224,359 (the “’359 patent”)
1002	File History for U.S. Patent No. 10,224,359
1003	Declaration of Dr. Michael Lebby
1004	Curriculum Vitae of Dr. Michael Lebby
1005	U.S. Patent Application Publication No. 2011/0156186 (Iida)
1006	U.S. Patent No. 7,675,099 (Hwang)
1007	International Publication No. WO 2011/035188 (Haddad188)
1008	U.S. Patent Application Publication No. 2012/0033119 (Shinohara)
1009	U.S. Patent Application Publication No. 2009/0266973 (Roy)
1010	P. Saint-Cast et al., “Very low surface recombination velocity on p-type c-Si by high-rate plasma-deposited aluminum oxide,” <i>Appl. Phys. Lett.</i> , 95, 151502 (2009), pp. 1-3, Oct. 14, 2009 (Saint-Cast)
1011	Samsung’s Proposed Constructions, Inv. No. 337-TA-1403 (Aug. 27, 2024)
1012	SiOnyx’s Proposed Constructions, Inv. No. 337-TA-1403 (Aug. 27, 2024)
1013	Email from N. Subhedar re: Claim Construction M&C Follow-Up (Sept. 8, 2024)
1014	Joint Claim Construction Chart, Inv. No. 337-TA-1403 (Nov. 1, 2024)
1015	Simon M. Sze, <i>Physics of Semiconductor Devices</i> (2nd ed. 1981)
1016	Georg Haas & Calvin D. Salzberg, “Optical Properties of Silicon Monoxide in the Wavelength Region from 0.24 to 14.0 Microns,” <i>J. Opt. Soc. Am.</i> , vol. 44, no. 3, pp. 181-87, Mar. 1954 (Haas)
1017	F. López & E. Bernabéu, “Refractive Index of Vacuum-Evaporated SiO Thin Films: Dependence on Substrate Temperature,” <i>Thin Solid Films</i> , 191 (1990), pp. 13-19 (Lopez)
1018	CRC Handbook of Chemistry and Physics (67th ed. 1986)
1019	Quick Reference Manual for Silicon (1985)
1020	A.X. Wei et al., “Electrical and optical properties of tantalum oxide thin films prepared by reactive magnetron sputtering,” <i>J. Alloys Compd.</i> , 509 (2011), pp. 9758-63 (Wei)
1021	Tero Pilvi (2008). <i>Atomic Layer Deposition for optical applications: metal fluoride thin films and novel devices</i> [Academic Dissertation University of Helsinki] ISBN 978-952-92-4814-8, 978-952-10-5133-3, http://ethesis.helsinki.fi .

Petition for *Inter Partes* Review of U.S. Pat. No. 10,224,359

Exhibit	Description
1022	E. Yablonovitch et al., “Unusually Low Surface-Recombination Velocity on Silicon and Germanium Surfaces,” <i>Phys. Rev. Lett.</i> , vol. 57, no. 2, pp. 249-52, Jul. 14, 1986
1023	J. Woollam et al., “Overview of Variable Angle Spectroscopic Ellipsometer (VASE), Part I: Basic Theory and Typical Applications,” <i>Crit. Rev. Opt. Sci. Technol.</i> , vol. CR72 (1999), pp. 3-28

I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner”) petitions for *inter partes* review seeking cancellation of claims 1-30, 32, 34, 36, 38-83 (the “Challenged Claims”) of U.S. Patent No. 10,224,359 (Ex. 1001, the “’359 patent”).

II. STANDING, MANDATORY NOTICES, AND FEE AUTHORIZATION

A. Grounds for Standing

Pursuant to 37 C.F.R. §42.104(a), Petitioner certifies that the ’359 patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the ’359 patent on the grounds identified in this petition.

B. Real Parties-in-Interest

The real parties-in-interest are Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.

C. Related Matters

Petitioner identifies the following related matters.

- *Sensors with Pixels and Products Containing the Same*, Inv. No. 337-TA-1403 (ITC) (the “Related Case”)
- *SiOnyx, LLC v. Samsung Electronics, Co., Ltd.*, 2:24-cv-00291 (E.D. Tex.)

D. Counsel Information

Petitioner designates the following counsel:

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Pursuant to 37 C.F.R. § 42.10 (b), Petitioner filed a power of attorney with the above designation of counsel.

E. Service Information

Service information is provided in the designation of counsel above. Petitioner consents to service of all documents via electronic mail at the email addresses above and at Samsung-SiOnyx-IPR-Cov@cov.com.

F. Payment of Fees Under 37 C.F.R. §42.103

This petition is accompanied by the fees set forth in 37 C.F.R. §42.15(a). Please charge or credit Deposit Account No. 60-3160 with any shortage or overpayment of fees associated with this petition and any other fees incurred by Petitioner.

III. SUMMARY OF CHALLENGE

- **Ground 1:** Claims 1-5, 7, 10, 18, 23, 25, 38-43, 45-50, 52-64, 67-70, 73-75, and 80-83 are anticipated, or at a minimum obvious, based on Hwang.
- **Ground 2:** Claims 12-17, 19-22, 26-29, and 76-79 are obvious based on Hwang and Haddad188.
- **Ground 3:** Claims 6, 8, 9, 11, 24, 30, 32, 34, and 36 are obvious based on Hwang and Shinohara.
- **Ground 4:** Claims 44, 51, 65-66, and 71-72 are obvious based on Hwang and Roy.

The application for the '359 patent was filed on July 21, 2016 and claims priority to a provisional application filed on March 22, 2012. Each asserted reference is available as prior art under 35 U.S.C. §102,¹ as shown below:

Exhibit	Reference	Date(s)	Availability as Prior Art
1006	U.S. Patent No. 7,675,099 (Hwang)	March 9, 2010 (issued)	§ 102(a), (b), & (e)(2)
1007	International Publication No. WO 2011/035188 (Haddad188)	March 24, 2011 (published)	§ 102(a) & (e)(1)

¹ The application for the '359 patent was filed after March 16, 2013 but claims priority to a provisional application that was filed before March 16, 2013. Accordingly, pre-AIA conditions for patentability apply.

Exhibit	Reference	Date(s)	Availability as Prior Art
1008	U.S. Patent Application Publication No. 2012/0033119 (Shinohara)	February 9, 2012 (published)	§ 102(a) & (e)(1)
1009	U.S. Patent Application Publication No. 2009/0266973 (Roy)	October 29, 2009 (published)	§ 102(a), (b), & (e)(1)

None of the foregoing references were substantively considered by the Examiner during prosecution. Hwang, Shinohara, and Roy were not of record during prosecution. Although Haddad¹⁸⁸ was cited in an IDS during prosecution, the Examiner did not rely on it to reject any claims and thus did not meaningfully address it. Accordingly, the Board should not deny institution under §325(d) and *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020) (precedential).

In applying *Advanced Bionics*, the Board considers the “*Becton, Dickinson*” factors, *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017) (precedential as to §III.C.5, first paragraph). “[I]f the record of the Office’s previous consideration of the art is not well developed or silent, then a petitioner may show the Office erred by overlooking something persuasive.” *Advanced Bionics*, IPR2019-01469 at 10. “An example of a material error may include misapprehending or overlooking specific teachings of the relevant prior art

where those teachings impact patentability of the challenged claims.” *Id.* at 8, n.9.

Here, to the extent that the disclosures Haddad¹⁸⁸ were before the Office during prosecution, the Examiner materially erred by overlooking or not appreciating their relevance to the challenged claims, as described herein. *See STMicroelectronics, Inc. v. Trustees of Purdue Univ.*, IPR2022-00309, Paper 14 at 12-13 (P.T.A.B. July 6, 2022) (finding that petitioner demonstrated examiner erred by not appreciating that IDS reference disclosed features recited in the challenged claims).

IV. OVERVIEW OF THE '359 PATENT

The '359 patent relates to image sensor pixels and isolation elements for trapping light within such pixels. '359 patent, 6:16-20. According to the patent, reduced pixel size for image sensors tends to increase electrical and optical crosstalk between adjacent pixels, and image signal-to-noise tends to decrease. *Id.*, 1:26-28. The patent purportedly provides for semiconductor devices with, for example, “enhanced light detection properties.” '359 patent, 6:13-16.

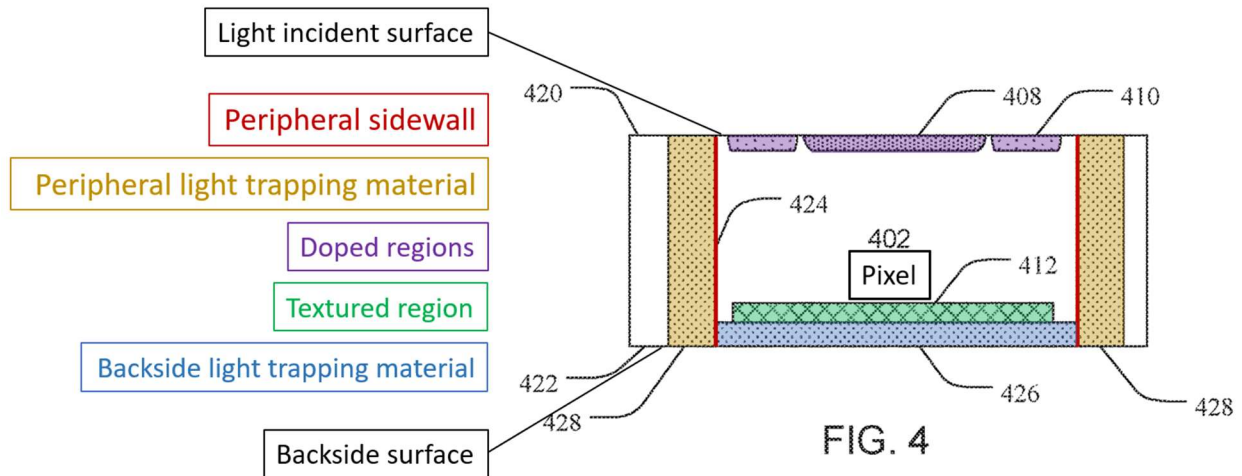
The patent broadly asserts that a “variety of reflective materials can be utilized in constructing [] isolation features in order to provide optical isolation, light trapping, and/or electrical isolation,” and that “any such material capable of incorporation into a photosensitive device” is within the patent’s scope. *Id.*, 7:64-8:1. Light that contacts the peripheral light trapping material or backside light

trapping material is “reflected back toward the pixel.” *Id.*, 1:51-54. Light is “effectively maintained inside the pixel until it is absorbed.” *Id.*, 12:31-32.

An isolation element can include at least two layers comprising material having a lower optical refractive index as compared to the material of a third layer disposed between those two layers. *Id.*, 8:36-40. In this case, the isolation element functions as a Bragg reflector. *Id.*, 8:35-36. The patent states that a large index of refraction “mismatch” can result in “total reflection at the trench side walls.” *Id.*, 9:26-28.

The pixel may also include a “textured region.” *Id.*, 6:45-47. “[A] textured region typically has a textured surface that increases the surface area and increases the probability of radiation absorption.” *Id.*, 15:27-30.

Figure 4 is a cross-sectional view of a light trapping pixel discussed in the patent. *Id.*, 3:40-42. Figure 4 (below) corresponds to the “Species 4” elected by the applicant during prosecution. Ex-1002 at 1696.



'359 patent, Fig. 4 (annotated); *see id.*, 11:13-34; *see also* Ex-1003, ¶¶41-48.

V. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art (“POSITA”) as of March 2012 would have had a Bachelor’s degree in engineering, physics, or a related or equivalent field, and two or more years of experience researching, developing, designing, and/or evaluating image sensors using photonics. Ex-1003, ¶50. A person with less or different education but more relevant practical experience, or vice versa, may also meet this standard. *Id.*

VI. CLAIM CONSTRUCTION

For purposes of this petition, Petitioner does not believe that any specialized constructions are necessary. However, in the Related Case, Petitioner and Patent Owner proposed competing constructions for certain '359 patent terms, which are addressed as relevant below. *See* Ex-1011-1014.

VII. APPLICATION OF PRIOR ART TO THE CHALLENGED CLAIMS

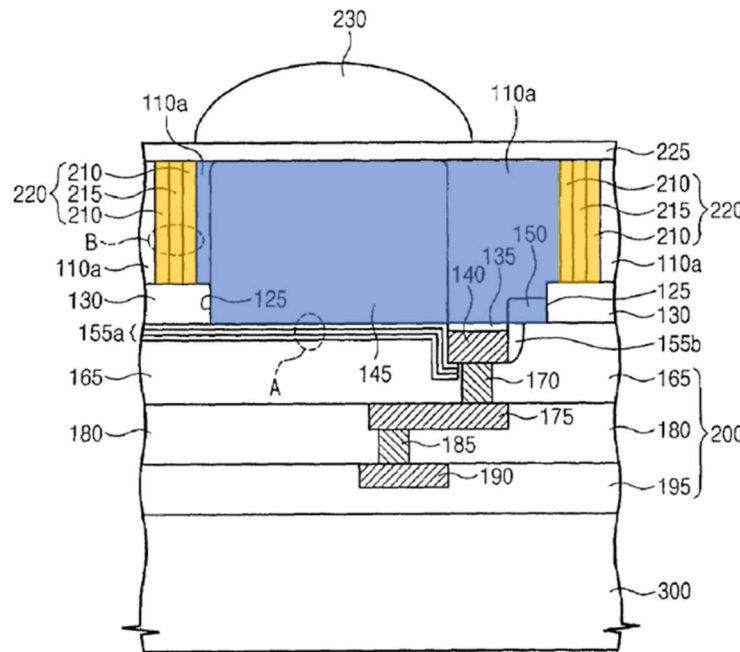
A. Ground 1: Claims 1-5, 7, 10, 18, 23, 25, 38-43, 45-50, 52-64, 67-70, 73-75, and 80-83 Are Anticipated or Rendered Obvious by Hwang

1. Overview of Hwang

Like the '359 patent, Hwang is directed to light-sensitive pixels in imaging devices. Hwang, Abstract. Furthermore, like the '359 patent, Hwang is concerned with improving image quality by increasing the percentage of incident light absorbed by the photodiode. *Id.*, 1:31-36.

An exemplary embodiment from Hwang is depicted below.

Fig. 2



Id., Fig. 2 (annotated).

Among other things, Figure 2 depicts a “sidewall multi-layered reflection layer 220” (shown in orange) “provided between the side walls of the pixel

semiconductor patterns 110a” (shown in blue). *Id.*, 6:7-9. “[T]he sidewall multi-layered reflection layer 220 includes layers with different respective refractive indexes.” *Id.*, 6:11-13. Hwang shows that the sidewall multi-layered reflection layer 220 is “disposed along the boundaries of all of the pixel semiconductor patterns 110a” to “enclose[] the side walls of the pixel semiconductor patterns 110a.” *Id.*, 6:15-21, 6:21-23. As shown in Figure 2, “[e]ach pixel semiconductor pattern 110a has a photodiode 145 disposed therein.”² *Id.*, 5:57-58. Ex-1003, ¶¶55-60

2. Claim 1

a) Element 1[pre]: “An imager device, comprising:”

Hwang teaches or suggests this preamble. Ex-1003, ¶¶61-62.

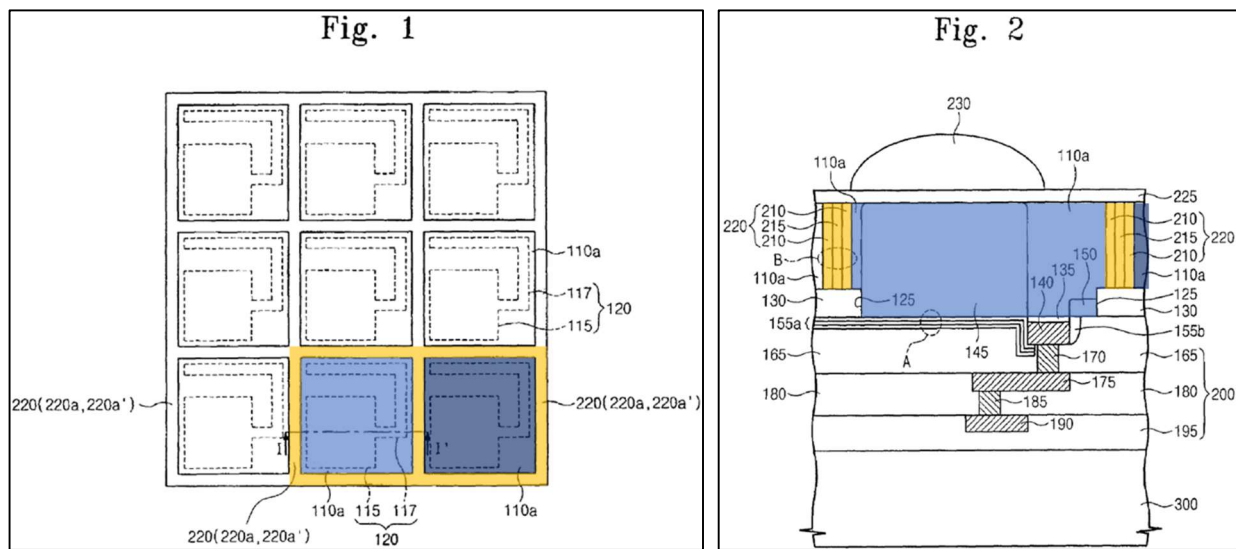
Hwang discloses an “image sensor that converts incident light to electrical signals.” *See, e.g.*, Hwang, 1:14-18.

b) Element 1[a]: “at least two adjacent light sensitive image sensor pixels each having a light incident surface, and a backside surface opposite the light incident surface;”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶63-66.

² While Hwang calls element 145 a “photodiode,” POSITAs would understand that photodiode, i.e., the structure that converts light into an electrical signal, encompasses more than just element 145, and would further include the surrounding pixel semiconductor patterns 110a. Ex-1003, ¶59 n.3.

Hwang's image sensor comprises *at least two adjacent light sensitive image sensor pixels*, as shown below (one in light blue, the other in dark blue). In describing the embodiment in Figure 2, Hwang discloses "a plurality of pixel semiconductor patterns 110a" that are "arranged two-dimensionally in rows and columns." Hwang, 5:52-54.³ "Each pixel semiconductor pattern 110a has a photodiode 145 disposed therein." *Id.*, 5:57-58.

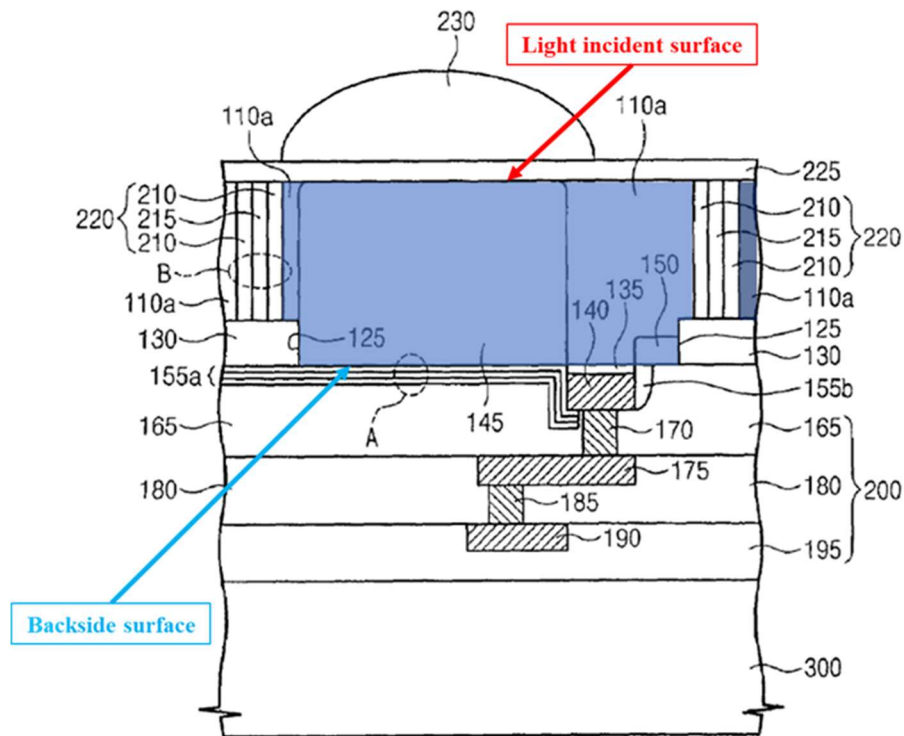


Hwang, Figs. 1-2 (annotated); Ex-1003, ¶64.

Each pixel (110a) further has a *light incident surface*, and a *backside surface opposite the light incident surface*, as illustrated below:

³ All emphases in quotes have been added, unless otherwise stated.

Fig. 2



Id., Fig. 2 (annotated). “The pixel semiconductor patterns 110a have first and second surfaces in parallel, i.e., that face one another,” where “the first surface ... is more proximate to the substrate 300 than is the second surface.” Hwang, 6:37–40. Hwang’s “second surface” constitutes a *light incident surface*, *see id.*, 8:17–22 (“[e]xternal light ... is incident on the second surface of the photodiode 145.”), and its “first surface” constitutes a *backside surface opposite the light incident surface*.

Ex-1003, ¶¶65-66.⁴

- c) **Element 1[b]: “a peripheral isolation element at least partially separating said two adjacent light sensitive pixels;”**

Hwang’s image sensor includes *a peripheral isolation element at least partially separating said two adjacent light sensitive pixels*. Ex-1003, ¶¶67-68.

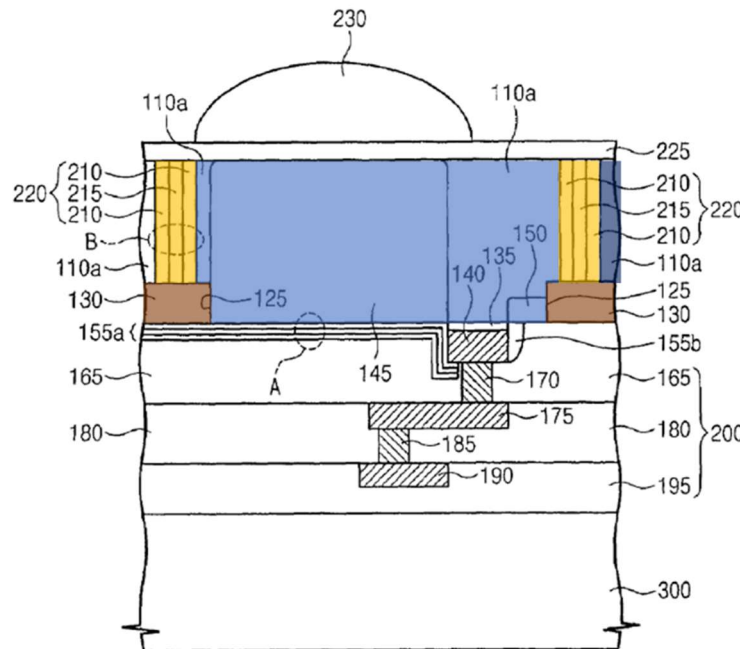
In describing the Figure 2 embodiment, Hwang discloses “[a] sidewall multi-layered reflection layer 220 [] provided between the side walls of the pixel semiconductor patterns 110a.” Hwang, 6:7-9. Hwang discloses that “layer 220 can be disposed along the boundaries of all of the pixel semiconductor patterns 110a, and all of the pixel semiconductor patterns 110a can thus be *separat[ed]* by the sidewall multi-layered reflection layer 220.” *Id.*, 6:19-23. Hwang also discloses that “layer 220 minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels.” *Id.*, 10:23-26. As a result, “interference of

⁴ Figures 2 and 6 use differently arranged sidewall multi-layered reflection layers but are otherwise the same. *See* Hwang, 11:57–60; Ex-1003, ¶66 n.5. Therefore, POSITAs would appreciate that Hwang’s disclosures for elements in Figure 6 (including layer 220a' comprising layers 212a' and 217a') are pertinent to corresponding elements in Figure 2 (including layer 220 comprising layers 210 and 215).

the image sensor can be minimized.” *Id.*, 10:26-27; *see also id.*, 10:19-40, 15:42-48.

Thus, element 220 is located on the *peripher[y]* of, and *at least partially separat[es]*, the adjacent light sensitive pixels.

Fig. 2



Id., Fig. 2 (annotated).

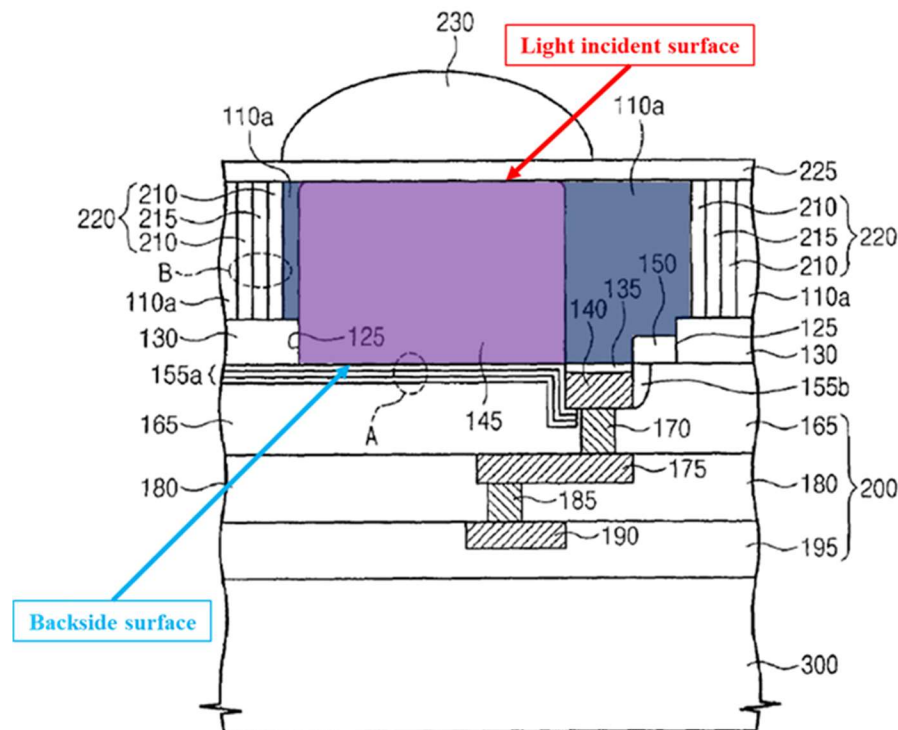
- d) **Element 1[c]: “each of said pixels having at least one doped region disposed on at least one of the light incident surface and the backside surface,”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶69-70.

As discussed regarding limitation 1[a], pixel semiconductor pattern 110a’s “second surface” corresponds to the *light incident surface* and its “first surface” corresponds to the *backside surface*. Hwang discloses that “[t]he pixel semiconductor patterns 110a are doped with a first conductive dopant” and that

“[t]he photodiodes 145 are regions doped with a second conductive dopant.” Hwang, 5:58-60. Hwang further explains that “[t]he photodiode 145 also has a first surface and a second surface that face each other,” that “the first surface of the photodiode 145 is coplanar with the first surface of the pixel substrate pattern 110a,” and that, “[a]s shown in FIG. 2, the second surface of the photodiode 145 can share a common surface with the second surface of the pixel substrate pattern 110a.” *Id.*, 6:61-67. Thus, doped region 110a (shown in dark blue below) and doped region 145 (shown in purple below) are *disposed on both of the light incident surface and the backside surface* (shown below). Ex-1003, ¶70.

Fig. 2



Hwang, Fig. 2 (annotated).

- e) **Element 1[d]: “wherein the peripheral isolation element comprises at least two materials having different indices of refraction,”**

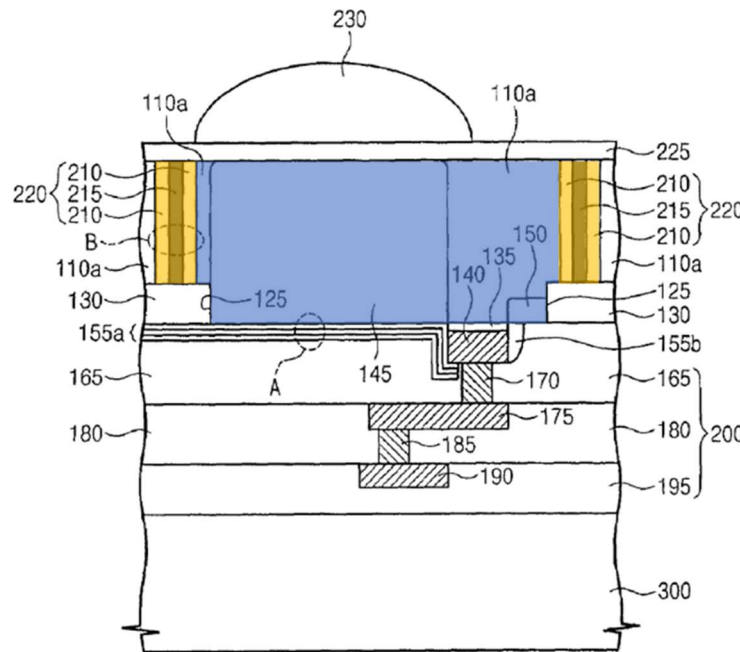
Hwang’s *peripheral isolation element* (element 220) *comprises at least two materials having different indices of refraction.* Ex-1003, ¶¶71-72.

Hwang discloses that layer 220 “includes a plurality of layers sequentially stacked at the side walls of the pixel semiconductor patterns 110a,” Hwang, 6:9-11: “a first sidewall reflection layer 210 and a second sidewall reflection layer 215.” *Id.*, 9:58-60. Hwang discloses that “[t]he refractive index of the first sidewall reflection layer 210 is different from the refractive index[] of ... the second sidewall reflection layer 215,” *id.*, 9:60-63; that “layer 210 can be a silicon oxide layer or a layer of air (with a refractive index of 1)” and that “layer 215 can be a silicon layer,” *id.*, 10:2-5; and that silicon oxide has “a refractive index of approximately 1.46” whereas silicon has “a refractive index of approximately 4,” *id.*, 9:28-30.

- f) **Element 1[e]: “wherein said peripheral isolation element comprises a first, a second and a third layer,”**

Hwang’s *peripheral isolation element* (element 220) *comprises a first, a second and a third layer* as shown below. Ex-1003, ¶¶73-74.

Fig. 2



Hwang, Fig. 2 (annotated).

Hwang discloses that layer 220 “includes a structure in which the first and second sidewall reflection layers 210 and 215 are stacked in an alternating manner a plurality of times on the side wall of the pixel semiconductor pattern 110a.” *Id.*, 10:6-10. Further, “the layers of the sidewall multi-layered reflection layer 220 contacting the pair of neighboring pixel semiconductor patterns 110a can be the first sidewall reflection layer 210” and “a second sidewall reflection layer 215 interposed between two first sidewall reflection layers 210.” *Id.*, 10:14-17, 10:48-50. Thus, Hwang’s peripheral isolation element comprises three layers: element 210 left of element 215 (*first layer*), element 210 right of element 215 (*second layer*), both

shown in orange above, and element 215 (*third layer*), shown in brown above. Ex-1003, ¶74.

g) Element 1[f]: “wherein said third layer is disposed between said first and second layers, and”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶75-76.

As shown in Figure 2 above, element 215 (*third layer*) is disposed between element 210 on its left (*first layer*) and element 210 on its right (*second layer*). *See also* Hwang, 10:14-17, 10:48-50 (“second sidewall reflection layer 215 interposed between two first sidewall reflection layers 210”).

h) Element 1[g]: “wherein each of said first and second layer exhibits an index of refraction less than an index of refraction of said third layer.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶77-78.

Hwang discloses that the refractive index of the first sidewall reflection layer 210 (*first and second layers*) “can be lower than the refractive index[] of” the second sidewall reflection layer 215 (*third layer*). Hwang, 9:63-66.

3. Claim 2: “The device of claim 1, wherein the index of refraction of at least one of said first and second layer is at least 0.2 lower relative to the refractive index of the third layer.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶79-80.

As discussed regarding limitation 1[e], Hwang discloses that the first sidewall reflection layer 210 (*first and second layers*) “can be a silicon oxide layer or a layer of air (with a refractive index of 1)” and that the second sidewall reflection layer 215

(*third layer*) “can be a silicon layer.” Hwang, 10:2-5. Hwang discloses that silicon oxide has “a refractive index of approximately 1.46” whereas silicon has “a refractive index of approximately 4.” *Id.*, 9:28-30. Thus, *the index of refraction of both of Hwang’s first layer and second layer (layers 210) is at least 0.2 lower* than that of Hwang’s *third layer* (layer 215).

4. Claim 3: “The device of claim 1, wherein at least of one of said at least two materials comprises silicon dioxide.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶81-83.

As discussed regarding limitations 1[d] and 1[e], Hwang discloses that “layer 210 can be a silicon oxide layer.” Hwang, 10:2-4; *see also id.*, 9:58-60, 10:48-55.

POSITAs would understand that, in disclosing layer 210 formed of silicon oxide, Hwang uses the term “silicon oxide” to mean “silicon dioxide” (SiO_2) as opposed to “silicon monoxide” (SiO). Ex-1003, ¶83. POSITAs would know that the refractive index of silicon dioxide is around 1.4-1.5, whereas the refractive index of silicon monoxide is at least around 1.8-2.2. *See, e.g.*, Ex-1015, Appendix I at 852 (refractive index of “ SiO_2 ” is “1.46”); Ex-1016, Abstract (refractive index of “silicon monoxide” (“ SiO ”) ranges from 2.15 to 1.95 in the 0.40 to 0.70 micron wavelength range); Ex-1017 at 17 & Fig. 2 (refractive index of “silicon monoxide” ranges from about 1.8-1.9 in the 1 to 5 micron wavelength range); Ex-1019 at 2-60 (refractive index of “ SiO_2 ” ranges from about 1.4-1.5 in the 0.40 to 0.70 micron wavelength range). Hwang specifies that its silicon oxide has “a refractive index of

approximately 1.46,” confirming that it is using silicon dioxide as opposed to silicon monoxide. Hwang, 9:28-29. Consistent with such an understanding, the ’359 patent itself uses the term “silicon oxide” to mean “silicon dioxide,” as it alternatively refers to the layers depicted in its Figure 2 as including “silicon dioxide” and “silicon oxide.” ’359 patent, 9:13-18 (“[T]he Bragg reflector can be constructed of a layer of polysilicon sandwiched between two layers of silicon dioxide.”); 10:20-22 (“Returning to FIG. 2, layers [of] the silicon oxide and polysilicon....”). *At least one of the materials* of Hwang’s sidewall multi-layered reflection layer 220 therefore *comprises silicon dioxide*.

5. Claim 4: “The device of claim 1, wherein at least one of said first and second layers comprises silicon dioxide.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶84-85.

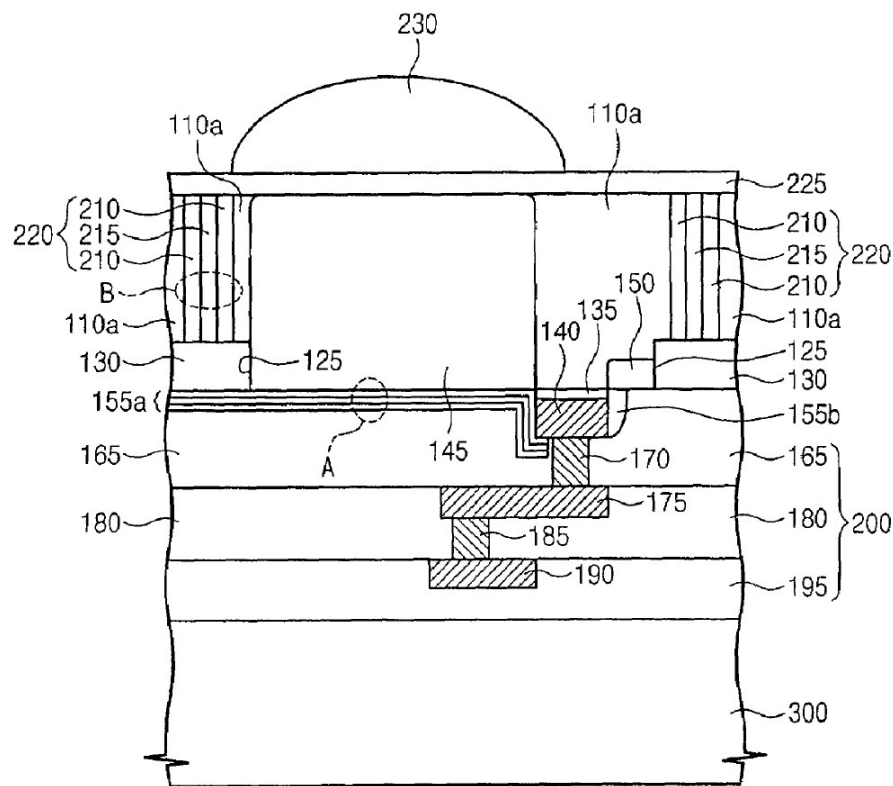
As discussed regarding limitation 1[d], Hwang discloses that the “first sidewall reflection layer 210” (*first and second layers*) “can be a silicon oxide layer,” Hwang, 10:2-4, 10:48-55. As discussed regarding claim 3, in describing layer 210, Hwang uses the term “silicon oxide” to mean “silicon dioxide.”

6. Claim 5: “The device of claim 1, wherein the isolation element extends substantially from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶86-90.

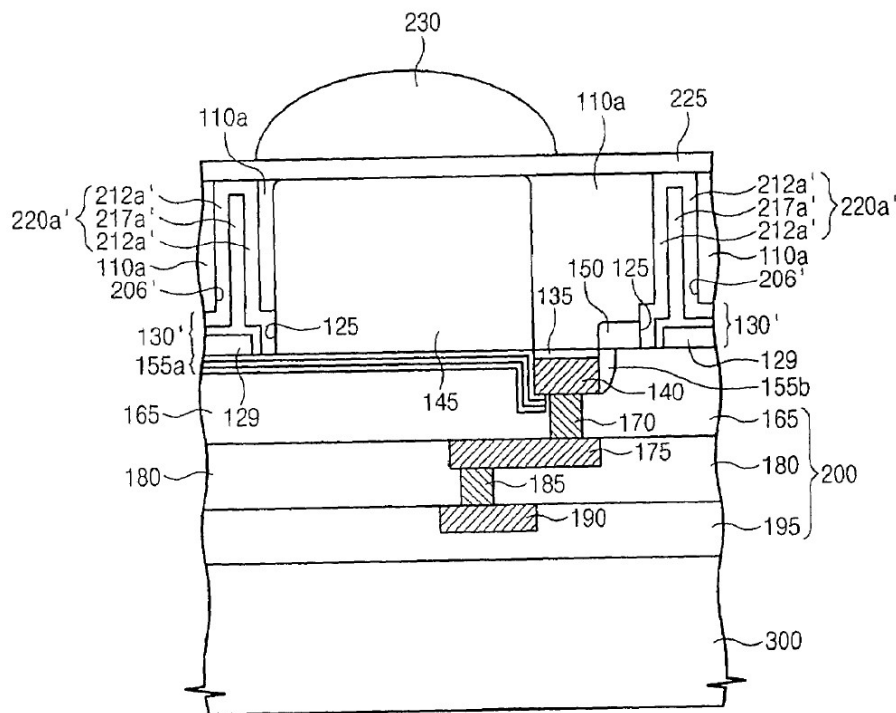
As discussed regarding limitation 1[b], Hwang discloses that “[a] sidewall multi-layered reflection layer 220 [*isolation element*] is provided between the side walls of the pixel semiconductor patterns 110a.” Hwang, 6:7-9; *see also id.*, 6:19-23. “As shown [in Figure 2], the sidewall multi-layered reflection layer 220 can contact the device isolation pattern 130.” *Id.*, 10:61-62. That is, it extends *substantially from the light incident surface* (the “second surface” of pixel 110a) to isolation pattern 130 adjacent to the *backside surface* (the “first surface”) of the pixels.

Fig. 2



To the extent there is any question whether the isolation element *extends substantially to the backside surface*, this element further would have been obvious. In Figure 6 below, Hwang discloses a modification of the Figure 2 embodiment in which a sidewall multi-layered reflection layer (element 220a' in Figure 6) extends fully *from the light incident surface to the backside surface*. Ex-1003, ¶88; Hwang, 11:66-12:2. “The first and second sidewall reflection layers 212a' and 217a' can be extended into trench 125.” Hwang, 12:25-26.

Fig. 6



POSITAs would have been motivated to modify Hwang’s layer 220 of Figure 2 to extend from the light incident surface to the backside surface, as suggested by

Figure 6, to increase “absorption efficiency of external light” and decrease “interference between neighboring pixels.” *See id.*, 10:28-40; Ex-1003, ¶89. POSITAs would have known that a gap in sidewall reflection between the light incident surface and the backside surface can allow electrons to escape under the sidewall trench into a neighboring pixel. *See, e.g.*, Roy, [0039]. POSITAs would consider the extension of Hwang’s layer 220 to be a known technique to improve a similar device in the same way and to be a simplification of manufacturing steps. *See, e.g., id.*, [0079].

Accordingly, it would have been obvious to POSITAs to modify Hwang’s layer 220 wherein it extends substantially from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels. Ex-1003, ¶90.

7. Claim 7: “The device of claim 1, wherein said peripheral isolation element comprises an oxide.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶91-92.

As discussed regarding limitation 1[d], Hwang discloses that “[t]he first sidewall reflection layer 210 can be a silicon oxide layer.” Hwang, 10:2-3, 10:48-55.

8. Claim 10: “The device of claim 1, wherein the peripheral isolation element comprises at least one material having an index of refraction of less than about 2.1.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶93-94.

As discussed regarding claim 2, Hwang discloses that “[t]he first sidewall reflection layer 210 can be a silicon oxide layer,” Hwang, 10:2-3, and that silicon oxide has “a refractive index of approximately 1.46,” *id.*, 9:28-29, which is *less than about 2.1*.

9. Claim 18

a) Element 18[pre]: “An imager device, comprising:”

Hwang teaches or suggests this preamble. Ex-1003, ¶¶95-96.

See discussion of 1[pre].

b) Element 18[a]: “at least two adjacent light sensitive image sensor pixels each having a light incident surface, and a backside surface opposite the light incident surface;”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶97-98.

See discussion of limitation 1[a].

c) Element 18[b]: “a peripheral isolation element separating said at least two adjacent light sensitive pixels so as to reduce optical crosstalk therebetween,”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶99-101.

As discussed regarding limitation 1[b], Hwang discloses *a peripheral isolation element*—sidewall multi-layered reflection layer 220—*separating at least two adjacent light sensitive pixels*. Hwang discloses that this layer 220 serves to *reduce optical crosstalk* between the *adjacent ... pixels*, as it “minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other

pixels.” *See* Hwang, 10:19-26. As a result, “interference of the image sensor can be minimized, and image distortion can be minimized.” *Id.*, 10:26-27; *see also id.*, 10:10-18, 28-40, 15:42-48.

- d) Element 18[c]: “said isolation element comprising at least two materials having different indices of refraction,”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶102-103.

See discussion of limitation 1[d].

- e) Element 18[d]: “at least one doped region disposed on at least one of the light incident surface and the backside surface,”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶104-105.

See discussion of limitation 1[c].

- f) Element 18[e]: “wherein said peripheral isolation element comprises a first, a second and a third layer,”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶106-107.

See discussion of limitation 1[e].

- g) Element 18[f]: “wherein said third layer is disposed between said first and second layers, and”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶108-109.

See discussion of limitation 1[f].

- h) Element 18[g]: “wherein each of said first and second layers exhibits an index of refraction less than an index of refraction of said third layer.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶110-111.

See discussion of limitation 1[g].

- 10. Claim 23: “The device of claim 18, wherein the peripheral isolation element extends from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶112-113.

See discussion of claim 5, explaining that it would have been obvious to modify the image sensor of Hwang Figure 2 so that the isolation element extends *fully from the light incident surface to the backside surface*.

- 11. Claim 25: “The device of claim 19, wherein said at least two pixels are formed monolithically in a common semiconductor substrate.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶114-116.

The '359 patent specifies: “As used herein, the term ‘monolithic’ refers to an electronic device in which electronic components are formed on the same substrate. For example, two monolithic pixel elements are pixel elements that are formed on the same semiconductor substrate.” '359 patent, 5:19-21.

Hwang discloses forming its plurality of pixel semiconductor patterns 110a (pixels) *in a common semiconductor substrate*—i.e., by selectively etching a single semiconductor layer 110. *See* Hwang, 3:60-63; *see also id.*, 4:5-7, 12:42-48, 13:29-35. Hwang discloses subsequently forming its photodiodes 145 in the same semiconductor layer. *See id.*, 3:29-30; *see also id.*, 1:63-64, 2:66, 5:52-55, 16:13.

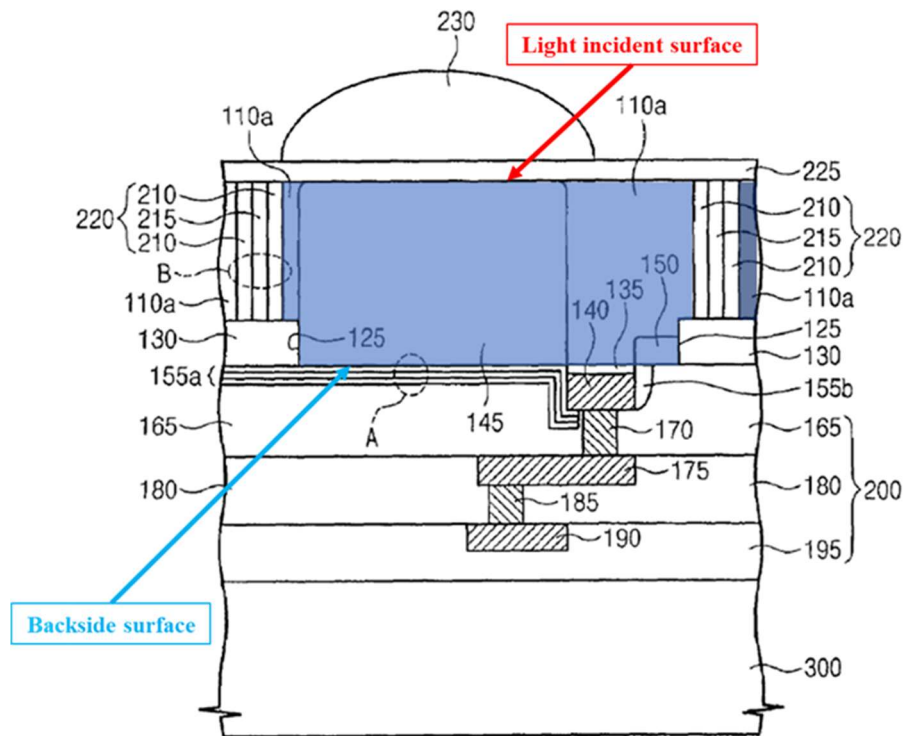
- 12. Claim 38: “The device of claim 1, wherein each of said at least two adjacent light sensitive image sensor pixels comprises a semiconductor portion providing said light incident surface and said backside surface, wherein said peripheral isolation element isolates the semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶117-120.

First, each of Hwang’s *light sensitive image sensor pixels* comprises a *semiconductor portion*: pixel semiconductor pattern 110a. Hwang discloses that “[t]he pixel semiconductor patterns 110a are formed as a semiconductor” and “can be formed of silicon.” Hwang, 5:52-55.

Second, as discussed regarding limitation 1[a], (i) the *light incident surface* is the pixel semiconductor pattern 110a’s “second surface” (shown below), and (ii) the *backside surface* is its “first surface” (shown below).

Fig. 2



Id., Fig. 2 (annotated); Ex-1003, ¶119.

Third, Hwang discloses that its sidewall multi-layered reflection layer 220 separates and optically *isolates* pixel semiconductor patterns 110a and “is interposed between a pair of neighboring pixel semiconductor patterns 110a” so that “the occurrence of interference between neighboring pixels can be minimized.” *Id.*, 10:10-18; *see also id.*, 6:21-23. Hwang discloses that layer 220 “minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels.” Hwang, 10:24-26. As a result, “interference of the image sensor can be minimized, and image distortion can be minimized.” *Id.*, 10:26-27; *see also id.*, 10:19-40, 15:42-48.

- 13. Claim 39: “The device of claim 38, wherein said peripheral isolation element optically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶121-122.

As discussed regarding claim 38, sidewall multi-layered reflection layer 220 *optically isolates* pixel semiconductor patterns 110a.

- 14. Claim 40: “The device of claim 38, wherein said peripheral isolation element electrically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶123-125.

Hwang discloses that its *peripheral isolation element* layer 220 *electrically isolates the semiconductor portions 110a of adjacent pixels*. As discussed regarding claim 5, POSITAs would have been motivated to modify Hwang’s sidewall multi-layered reflection layer 220 of Figure 2 to extend from the light incident surface to the backside surface, as suggested by Figure 6. *See* Hwang, 10:28-40. POSITAs would have known that a gap in sidewall reflection between the light incident surface and the backside surface can allow electrons to escape under the sidewall trench into a neighboring pixel. *See, e.g.,* Roy, [0039]; Shinohara, [0064] (because “adjacent pixels are physically isolated from each other ... the leakage of charge in the photodiode PD into an adjacent pixel can be substantially prevented”). POSITAs would consider the extension of Hwang’s layer 220 to be a known technique to

electrically isolate adjacent pixels to improve a similar device in the same way. Ex-1003, ¶124.

15. **Claim 41: “The device of claim 38, wherein an index of refraction of the semiconductor portion of each of said at least two adjacent image sensor pixels is different from indices of refraction of said layers of the peripheral isolation element such that light incident from each of said semiconductor portions on said peripheral isolation element is reflected, thereby providing optical isolation between the pixels.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶126-129.

As discussed above regarding claim 5, Hwang discloses a modification of the Figure 2 embodiment in which layer 220 extends from the light incident surface to the backside surface, as shown for example in Hwang Figure 6. Hwang, 11:66-12:2. In the Figure 6 approach, “[t]he second sidewall reflection layer 217a' is disposed within the groove 206 and on the first sidewall reflection layer 212a'.” *Id.*, 11:33-35. A POSITA would understand that layer 217a' is formed of polysilicon. *See also* Hwang, 14:58-4; Ex-1003, ¶127. Silicon dioxide has “a refractive index of approximately 1.46” whereas the silicon of semiconductor portion 110a has “a refractive index of approximately 4,” Hwang, 9:28-30. POSITAs would know that polysilicon has a refractive index different from the semiconductor portion 110a. Ex-1023, Fig. 19; Ex-1003, ¶127. In this case, the *index of refraction* of the image sensor pixels (silicon) is *different from indices of refraction* of all the *layers of the peripheral isolation element* (silicon dioxide and polysilicon).

As discussed regarding limitation 18[b], Hwang's peripheral isolation element optically isolates the adjacent light sensitive image sensor pixels. Hwang specifies that the peripheral isolation element achieves such isolation by reflecting light incident on it from the semiconductor portions of the adjacent pixels it separates. *See* Hwang, 10:19-40.

Accordingly, POSITAs would find it obvious to follow Hwang's teachings to construct an imager device wherein *an index of refraction of the semiconductor portion of each of at least two adjacent image sensor pixels* (approximately 4 for pixel semiconductor pattern 110a) *is different from indices of refraction of the layers of the peripheral isolation element* (approximately 1.46 for silicon dioxide and greater than 4 for polysilicon) *such that light incident from each of said semiconductor portions on said peripheral isolation element is reflected, thereby providing optical isolation between the pixels*. Ex-1003, ¶¶128-129.

- 16. Claim 42: “The device of claim 1, wherein said at least two adjacent light sensitive image sensor pixels are formed monolithically on a common semiconductor substrate and are isolated from one another by said peripheral isolation element.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶130-132.

As discussed regarding claim 25, Hwang discloses that its *adjacent light sensitive image sensor pixels are formed monolithically on a common semiconductor substrate*.

As discussed regarding limitation 1[b], Hwang discloses that its *adjacent light sensitive image sensor pixels are isolated from one another* by its sidewall multi-layered reflection layer 220.

17. Claim 43: “The device of claim 1, wherein said peripheral isolation element is a trench isolation element.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶133-134.

Hwang discloses that its sidewall multi-layered reflection layer 220 is formed by “etch[ing] a plurality of grooves 205” in “semiconductor layer 110” and then “fill[ing] the grooves with a predetermined material.” Hwang, 12:42-45, 12:50-51; *see id.*, 12:42-13:3. Accordingly, POSITAs would understand that Hwang’s *peripheral isolation element* layer 220 is a *trench* element—i.e., formed by etching and filing trenches.

18. Claim 45: “The device of claim 18, wherein each of said at least two adjacent light sensitive image sensor pixels comprises a semiconductor portion providing said light incident surface and said backside surface, wherein said peripheral isolation element isolates the semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶135-136.

See discussion of claim 38.

19. Claim 46: “The device of claim 45, wherein said peripheral isolation element optically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶137-138.

See discussion of claim 39.

- 20. Claim 47: “The device of claim 46, wherein said peripheral isolation element electrically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶139-140.

See discussion of claim 40.

- 21. Claim 48: “The device of claim 47, wherein an index of refraction of the semiconductor portion of each of said at least two adjacent image sensor pixels is different from indices of refraction of said layers of the peripheral isolation element such that light incident from each of said semiconductor portions on said peripheral isolation element is reflected, thereby providing optical isolation between the pixels.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶141-142.

See discussion of claim 41.

- 22. Claim 49: “The device of claim 18, wherein said at least two adjacent light sensitive image sensor pixels are formed monolithically on a common semiconductor substrate and are isolated from one another by said peripheral isolation element.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶143-144.

See discussion of claim 42.

- 23. Claim 50: “The device of claim 18, wherein said peripheral isolation element is a trench isolation element.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶145-146.

See discussion of claim 43.

- 24. Claim 52: “The imager device of claim 38, wherein at least one of the first layer and the second layer of said peripheral isolation element and said semiconductor portion of each of said at least two adjacent pixels comprise different materials.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶147-148.

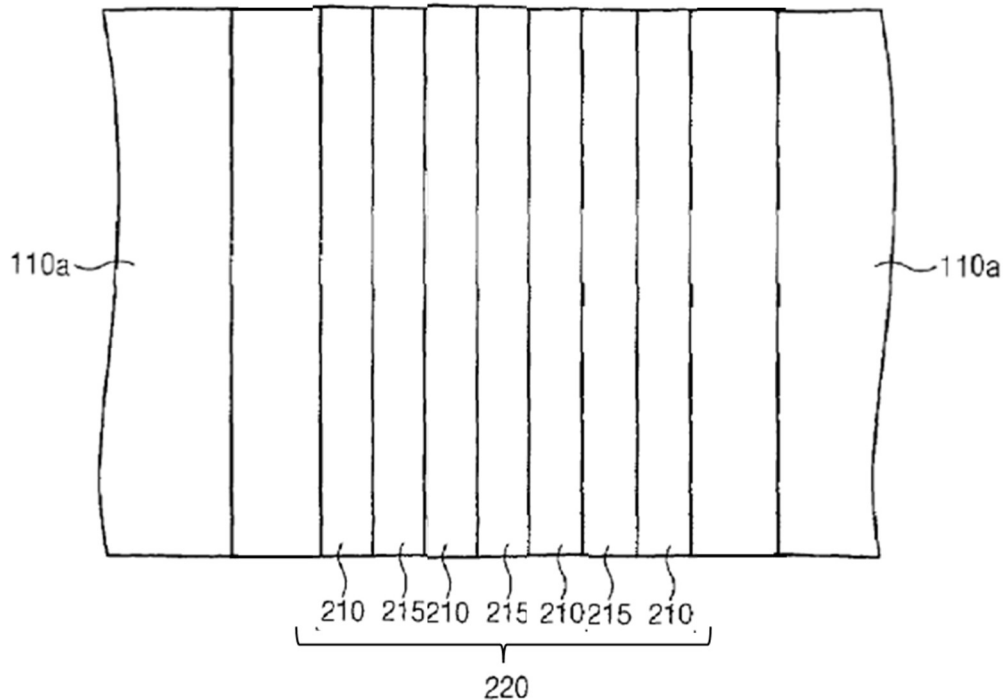
Hwang discloses that its first sidewall reflection layer 210 (*first and second layers*) “can be a silicon oxide layer,” Hwang, 10:2-4, and that “the pixel semiconductor patterns 110a can be formed of silicon,” *id.*, 5:52-55. Thus, *at least one of the first layer and second layer of Hwang’s peripheral isolation element (layer 220) and the semiconductor portion of each of the adjacent pixels (pixel semiconductor patterns 110a) comprise different materials.*

- 25. Claim 53: “The imager device of claim 1, wherein the first layer and the second layer of said peripheral isolation element comprise different materials.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶149-153.

Hwang discloses that layer 220 “includes a structure in which the first and second sidewall reflection layers 210 and 215 are stacked in an alternating manner a plurality of times.” Hwang, 10:6-10; *see also id.*, 2:16-19, 4:12-15, Fig. 4. Hwang further discloses that “[t]he number of layers of the sidewall multi-layered reflection layer 220 ... varies according to the number of the grooves 205.” *See id.*, 12:62-13:3. Accordingly, Hwang’s sidewall multi-layered reflection layer 220 can be

constructed of seven layers, beginning with layer 210 at the outside and alternating between material layers 210 and 215. Ex-1003, ¶150.



Hwang, Fig. 4 (modified).

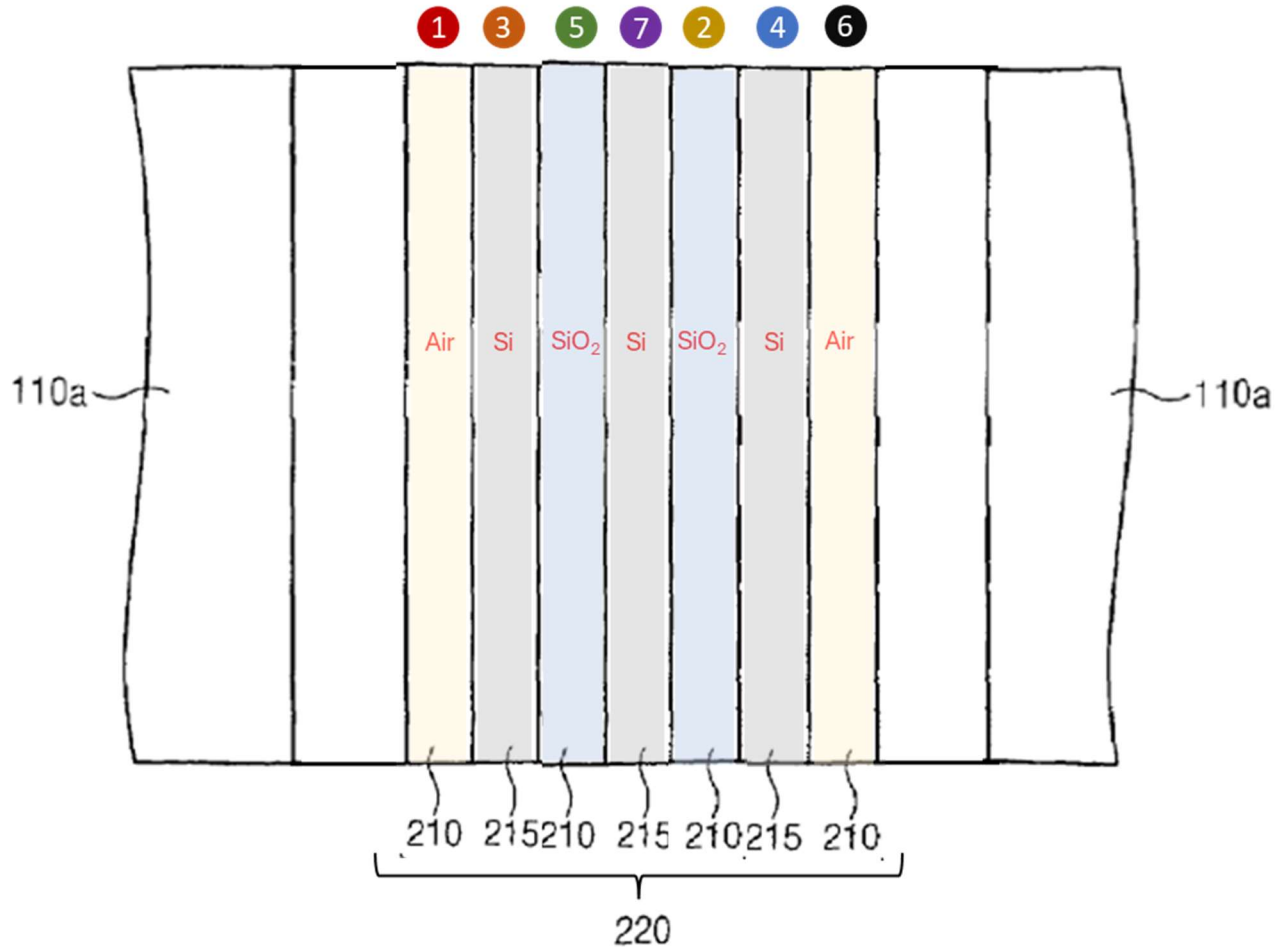
Hwang also teaches that “[t]he first sidewall reflection layer 210 can be a silicon oxide layer or a layer of air (with a refractive index of 1).” Hwang, 10:2-4. In constructing a seven-layer Hwang sidewall multi-layered reflection layer, POSITAs would find it obvious to apply Hwang’s teachings to use both silicon oxide and air as layers 210, such that the final construct would be 210 (air) - 215 (silicon) - 210 (silicon dioxide) - 215 (silicon) - 210 (silicon dioxide) - 215 (silicon) - 210 (air). Ex-1003, ¶151. The indices of refraction of such a construct would aid in the reflectivity of the sidewall multi-layered reflection layer, consistent with Hwang’s

teachings that “the sidewall multi-layered reflection layer 220 include layers with different respective refractive indexes,” *id.*, 6:11-13, to increase the light sensitivity, *id.*, 9:11-14. Also, POSITAs would know that placing an air layer at the outermost layer would result in lower surface recombination velocity. *See generally* Ex-1022. By using these known techniques, POSITAs would improve the base Figure 2 embodiment. Ex-1003, ¶151.

Numbering the layers of this sidewall multi-layered reflection layer as 210 (air; first) - 215 (silicon; third) - 210 (silicon dioxide; fifth) - 215 (silicon; seventh) - 210 (silicon dioxide; second) - 215 (silicon; fourth) - 210 (air; sixth) would still meet the limitations of claim 1. Layer numbering has no impact on limitations 1[a]-1[d]. Limitation 1[e] is met because the seven-layer sidewall multi-layered reflection layer comprises a first, second, and third layer. Limitation 1[f] is met because the

third layer is disposed between the first and second layers.⁵ Limitation 1[g] is met because the refractive indices of the first layer (air, $n=1$) and second layer (silicon dioxide, $n=1.46$) are both less than the refractive index of the third layer (silicon, $n\approx 4$).

⁵ In the Related Proceeding, Patent Owner proposed to construe *said third layer is disposed between said first and second layers* to mean “a third layer between the first and second layers, wherein the first and second layers can be different materials from one another,” while Petitioner proposed that the third layer is in contact with the first and second layers on opposing sides. Ex-1011; Ex-1012. For purposes of this petition, Petitioner adopts Patent Owner’s construction, which is met by Hwang’s seven-layer sidewall multi-layered reflection layer, as explained in the main text.



Hwang, Fig. 4 (annotated and modified); Ex-1003, ¶152.

The first layer (air) and the second layer (silicon dioxide) of Hwang’s seven-layer sidewall multi-layered reflection layer comprise different materials.

26. Claim 54: “The imager device of claim 1, wherein the peripheral isolation element comprises at least three materials.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶154-155.

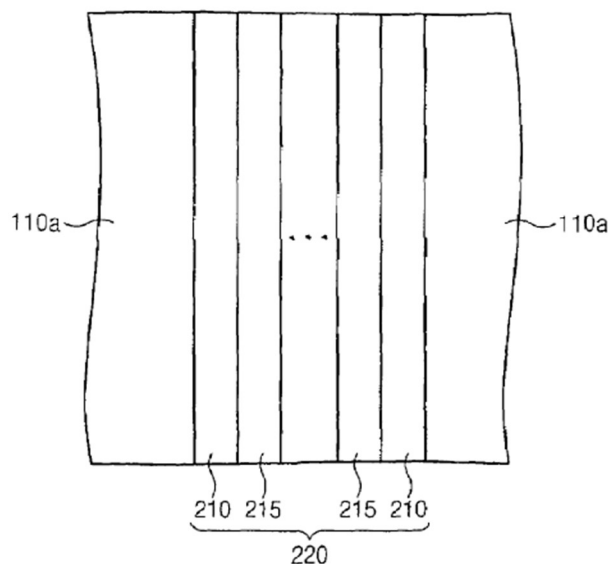
See discussion of claim 53 regarding a seven-layer construct according to the teachings of Hwang. In such a construct of Hwang’s sidewall multi-layered reflection layer, *at least three materials* are provided: air, silicon dioxide, and silicon.

27. Claim 55: “The imager device of claim 1, wherein the peripheral isolation element comprises more than three layers.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶156-157.

Hwang discloses that its *peripheral isolation element* layer 220 “includes a structure in which the first and second sidewall reflection layers 210 and 215 are stacked in an alternating manner a plurality of times on the side wall of the pixel semiconductor pattern 110a.” Hwang, 10:6-10; *see also id.*, 2:16-19, 4:12-15, 10:6-10, Fig. 4 (below). Hwang further discloses that “when three ... grooves 205 are formed to enclose one pixel semiconductor pattern 110a, the number of layers of the sidewall multi-layered reflection layer 220 is five.” *Id.*, 12:67-13:3.

Fig. 4



Id., Fig. 4; *id.*, 5:1-4, 9:35-40, 10:6-10, 12:67-13:3. Thus, Hwang discloses a

peripheral isolation element layer 220 that comprises more than three layers.

28. Claim 56: “The imager device of claim 1, wherein the peripheral isolation element comprises a light trapping material filling a trench.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶158-160.

Hwang discloses forming layer 220 by selectively etching grooves 205 surrounding pixel semiconductor patterns 110a and then filling those grooves with a predetermined material. Hwang, 12:42-61. Accordingly, each layer 210 of Hwang’s *peripheral isolation element layer 220 comprises a material filling a trench* (groove 205).

Hwang discloses that layer 220 reflects light incident on it from the photodiode 145 that it encloses back onto that same photodiode, minimizing incidence of such light “on other pixels.” *Id.*, 10:19-40; *see also id.*, 8:61-9:14. Thus, layer 220 traps light within the pixel it encloses. Ex-1003, ¶160.

29. Claim 57: “The imager device of claim 56, wherein the trench is one of a shallow trench and a deep trench.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶161-163.

As discussed regarding claim 56 and shown in Figure 13, Hwang discloses forming each groove 205 (*trench*) by selectively etching the semiconductor layer 110. Hwang, 12:42-45, Fig. 13. Accordingly, as discussed regarding claim 5, Hwang teaches *a deep trench* that extends substantially from the light incident surface to the backside surface.

- 30. Claim 58: “The imager device of claim 45, wherein at least one of the first layer and the second layer of the peripheral isolation element and said semiconductor portion of each of said at least two adjacent pixels comprise different materials.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶164-165.

See discussion of claim 52.

- 31. Claim 59: “The imager device of claim 18, wherein the first layer and the second layer of said peripheral isolation element comprise different materials.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶166-167.

See discussion of claim 53.

- 32. Claim 60: “The imager device of claim 18, wherein the peripheral isolation element comprises at least three materials.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶168-169.

See discussion of claim 54.

- 33. Claim 61: “The imager device of claim 18, wherein the peripheral isolation element comprises more than three layers.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶170-171.

See discussion of claim 55.

- 34. Claim 62: “The imager device of claim 18, wherein the peripheral isolation element comprises a light trapping material filling a trench.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶172-173.

See discussion of claim 56.

35. Claim 63: “The imager device of claim 62, wherein the trench is one of a shallow trench and a deep trench.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶174-175.

See discussion of claim 57.

36. Claim 64: “The imager device of claim 1, wherein said peripheral isolation element comprises a trench isolation element formed by filling a trench with said first, said second, and said third layers.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶176-177.

The recited element *a trench isolation element formed by filling a trench with said first, said second, and said third layers* is a product-by-process element. Accordingly, a determination of validity considers only the end-product and not the process of making it. *See Amgen Inc. v. F. Hoffman-La Roche Ltd.*, 580 F.3d 1340, 1369 (Fed. Cir. 2009). “As a result, a product-by-process claim can be anticipated by a prior art product that does not adhere to the claim’s process limitation.” *Id.* at 1370.

As discussed regarding claim 56, Hwang discloses a peripheral isolation element comprising a light trapping material filling a trench. Hwang, 10:14-17, 10:48-50. Layer 220 is trench-based isolation element because “[a] sidewall multi-layered reflection layer 220 is formed on the sidewall of the pixel semiconductor pattern 110a” by “selectively etch[ing] to form a plurality of grooves 205 surrounding the pixel semiconductor patterns 110a.” *Id.*, 12:51-53, 12:43-45. “[T]he

grooves 205 are filled with a predetermined material.” *Id.*, 12:50-51. The result, as depicted in Hwang Figure 2, is a *trench isolation element* with *first* (element 210), *second* (element 210), and *third* (element 215) layers filling a trench.⁶

37. Claim 67: “The imager device of claim 1, wherein said peripheral isolation element is configured to reflect at least a portion of light incident thereon from any of said two adjacent light sensitive pixels back to that pixel.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶178-179.

As discussed regarding claim 38, Hwang discloses that its sidewall multi-layered reflection layer 220 reflects light incident on it from the photodiode 145 that it encloses back onto that same photodiode, such that *at least a portion of light incident* on the pixel’s layer 220 is *reflect[ed] back to that pixel*. To achieve this result, Hwang discloses positioning layer 220 “between a pair of neighboring pixel semiconductor patterns 110a.” Hwang, 10:11-12. Hwang discloses that layer 220 “minimizes incidence of the light ... on the photodiode 145 within another pixel semiconductor pattern 110a. In other words,... layer 220 minimizes incidence of the

⁶ To the extent the Board finds that grooves 205 separated by layer 215 do not constitute a trench, it would have been obvious to POSITAs to try “an alternate embodiment of a method of forming an image sensor according to aspects of the present invention,” Hwang, 13:26-28, by which a single groove 206 is etched and filled to form three layers. *See id.*, 13:31-49, Fig. 15; Ex-1003, ¶177 n.7.

light incident on a photodiode 145 that it encloses being incident on other pixels.”

Id., 10:19-26.

- 38. Claim 68: “The imager device of claim 67, wherein the peripheral isolation element is further configured to optically isolate said two adjacent light sensitive pixels.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶180-181.

See discussion of claim 39.

- 39. Claim 69: “The imager device of claim 68, wherein the peripheral isolation element is further configured to electrically isolate said two adjacent light sensitive pixels.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶182-183.

See discussion of claim 40.

- 40. Claim 70: “The imager device of claim 18, wherein said peripheral isolation element comprises a trench isolation element formed by filling a trench with said first, said second, and said third layers.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶184-185.

See discussion of claim 64.

- 41. Claim 73: “The imager device of claim 18, wherein said peripheral isolation element is configured to reflect at least a portion of light incident thereon from any of said two adjacent light sensitive pixels back to that pixel.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶186-187.

See discussion of claim 67.

- 42. Claim 74: “The imager device of claim 73, wherein the peripheral isolation element is further configured to optically isolate said two adjacent light sensitive pixels.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶188-189.

See discussion of claim 39.

- 43. Claim 75: “The imager device of claim 74, wherein the peripheral isolation element is further configured to electrically isolate said two adjacent light sensitive pixels.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶190-191.

See discussion of claim 40.

- 44. Claim 80: “The imager device of claim 1, wherein the peripheral isolation element comprises five layers.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶192-193.

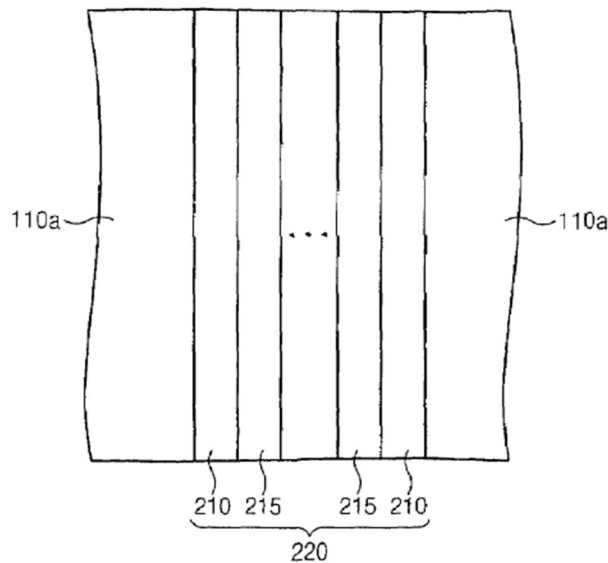
See discussion of claim 55.

- 45. Claim 81: “The imager device of claim 80, wherein the five layers include the first layer, the second layer, the third layer, a fourth layer disposed between the first layer and one of said adjacent pixels and a fifth layer disposed between the second layer and the other one of said adjacent pixels.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶194-196.

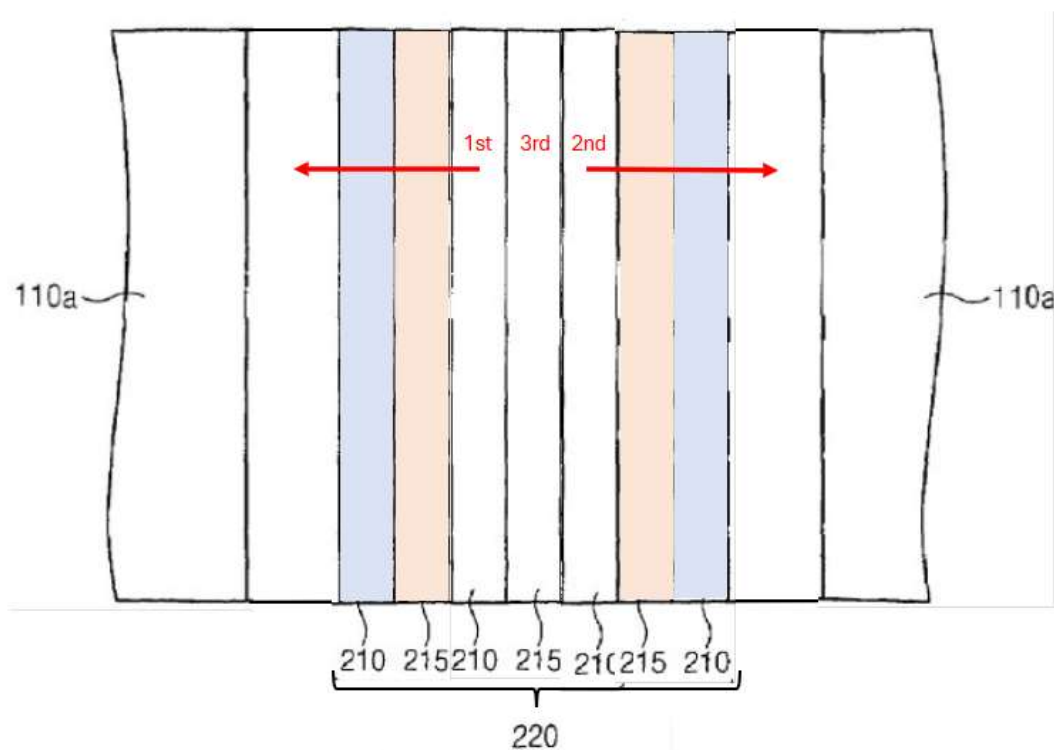
Hwang discloses that its sidewall multi-layered reflection layer 220 “includes a structure in which the first and second sidewall reflection layers 210 and 215 are stacked in an alternating manner a plurality of times.” Hwang, 10:6-10; *see also id.*, 2:16-19, 4:12-15, 5:1-4, 9:35-40, Fig. 4 (below).

Fig. 4



Id., Fig. 4.

As discussed regarding claim 53, in view of Hwang's teachings, it would have been obvious for POSITAs to form a seven-layered reflection layer 220, as shown below. Ex-1003, ¶196. Such a peripheral isolation element would satisfy claim 81 because it would comprise (i) the same three layers as discussed in claim limitation 1[e] (*first, second, and third layers*); (ii) a layer shown in orange below (*fourth layer, to the left of the first layer*) *disposed between the first layer and the adjacent pixel*; and (iii) a layer shown in orange below (*fifth layer, to the right of the second layer*) *disposed between the second layer and the adjacent pixel*.



Hwang, Fig. 4 (annotated and modified).

- 46. Claim 82: “The imager device of claim 18, wherein the peripheral isolation element comprises five layers.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶197-198.

See discussion of claim 55.

- 47. Claim 83: “The imager device of claim 82, wherein the five layers include the first layer, the second layer, the third layer, a fourth layer disposed between the first layer and one of said adjacent pixels and a fifth layer disposed between the second layer and the other one of said adjacent pixels.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶199-200.

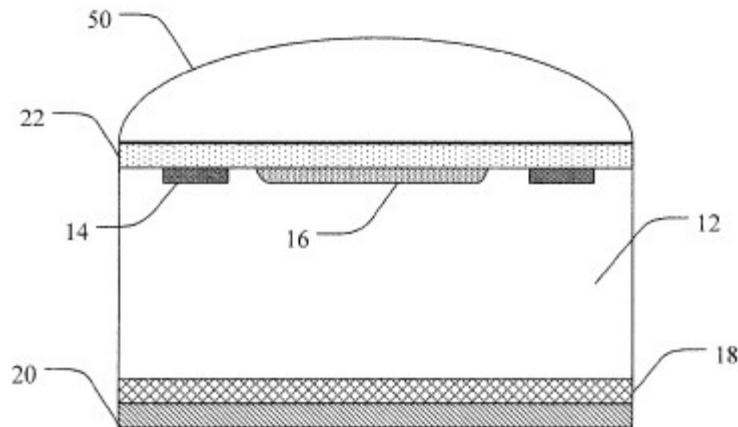
See discussion of claim 81.

B. Ground 2: Claims 12-17, 19-22, 26-29, and 76-79 Are Obvious Based on Hwang and Haddad188

1. Overview of Haddad188

Haddad188 is similarly directed to light-sensitive pixels in imaging devices with pixel separation structures. Haddad188, 1:24-30, 21:12-13. Haddad188 also discloses a “textured region at the point of entry of the electromagnetic radiation,” which “provide[s] enhancement and/or filtering of the incoming electromagnetic radiation.” *Id.*, 20:30-21:2; *see also id.*, 2:18-27.

An exemplary embodiment from Haddad188 is depicted below.



Id., Fig. 5.

Among other things, Figure 5 depicts a “textured region 18 coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation.”

Id., 9:18-21; Ex-1003, ¶¶201-205.

2. Motivation to Combine Hwang and Haddad188

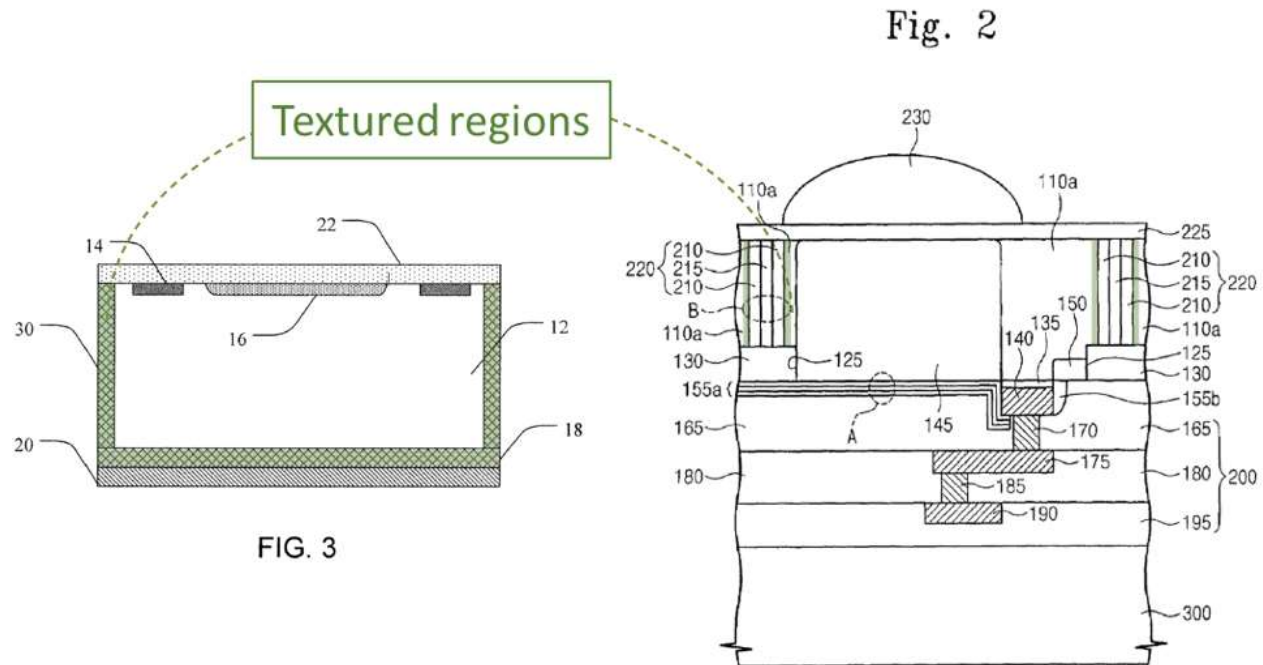
POSITAs would have been motivated to use Haddad188's textured regions with Hwang's semiconductor substrate faces and sidewall multi-layer reflective layers. Ex-1003, ¶206. Haddad188 teaches that a "textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device." Haddad188, 14:29-31. Haddad188 explains that "[t]extured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device." *Id.*, 15:14-16. As a result, quantum efficiency of the device increases, "leading to an improved signal to noise ratio." *Id.*, 15:18-19, 21:12-15, Fig. 3. Whether to use Haddad188's textured regions would have depended on the particular design needs regarding the cost of manufacture and the desired improvement in absorption and sensitivity. Ex-1003, ¶206.

Haddad188 discloses that "[o]ne effective method of producing a textured region is through laser processing." Haddad188, 16:3-4; 16:14-19 ("[A] surface of a semiconductor material is irradiated with laser radiation to form a textured or surface modified region."). POSITAs would know that laser provides excellent control of the surface profile and may be programmed to offer optical performance that exceeds

simple wet and dry etching of surfaces, especially when texturing is being implemented. Ex-1003, ¶207.

Using Haddad188's textured regions to further improve light absorption and sensitivity would have been a use of a known technique to improve similar devices in the same way. Both Hwang and Haddad188 are directed to photosensitive imager devices. Hwang, Abstract, 1:14-18, 5:47-51; Haddad188, 1:24-30, 8:15-22. Both contemplate using additional layers that improve absorption of external light by reflecting light incident on a pixel back toward the photodiode. *See* Hwang, 7:45-47, 8:59-9:14, 10:31-34 (“[T]he portion of the light reflected toward the sidewall multi-layered reflection layer 220 from the light reflected by the first and second boundary surfaces is incident again on the photodiode.”), 20:20-22 (“The reflecting layer can be coupled to any side or portion of the semiconductor substrate in order to reflect electromagnetic radiation back into the device.”). Haddad188's photosensitive devices also include at least one textured region positioned within the semiconductor substrate to interact with electromagnetic radiation to improve efficiency over traditional photosensitive devices. Haddad188, 9:18-21, 9:32-33. POSITAs would have been motivated to modify Hwang's sidewall multi-layered reflection layer 220 with Haddad188's textured region to increase the quantum efficiency of the device. Ex-1003, ¶208.

Applying Haddad188's processing to Hwang's sidewall multi-layered reflection layer 220 would have yielded a Hwang device such as the following:



POSITAs would have known to apply Haddad188's textured regions to Hwang's photosensitive device. Ex-1003, ¶¶209-210. For example, Hwang and Haddad188 both place trench isolation structures between adjacent pixels to reduce optical and electrical crosstalk. *See* Hwang, 6:15-17 (teaching sidewall multi-layered reflection layer 220), 10:23-26 (same); Haddad188, 22:21-29 (teaching trench isolation elements), 24:1-15 (same).

Given the similarities, POSITAs would have recognized that the combination would have required nothing more than applying Haddad188's teachings about textured regions and trench isolation structures to Hwang's teaching of trench structures to isolate image sensor pixels. Ex-1003, ¶211. Indeed, Haddad188 notes

that “[t]rench isolation can include dielectric materials, reflective materials, conductive materials, and combinations thereof, including textured regions and other light diffusing features ... to reflect incident electromagnetic radiation.” Haddad188, 24:5-8. Thus, applying Haddad188’s textured regions to Hwang’s pixel isolation structures would have amounted to nothing more than applying a known technique to improve a similar device in the same way, and it would have yielded predictable results.

POSITAs would have recognized that incorporating Haddad188’s textured regions into Hwang’s device would provide certain benefits. Ex-1003, ¶212. Haddad188 explains that a textured region can result in “increasing the semiconductor substrate’s effective absorption length as compared to a semiconductor substrate lacking a textured region.” *Id.*, 1:32-34; *see also id.* 22:27-29, 24:7-9. Additionally, Haddad188 explains that when textured regions are placed on the sides of the device, “electromagnetic radiation normally exiting through the sides of the device” can be “further defused [diffused]⁷ and absorbed within semiconductor substrate,” resulting in “enhanced absorption.” *Id.*, 21:12-16.

⁷ Haddad188 clarifies that the textured region is used “to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes through to the (continued...) ”

It would have been well within the abilities of POSITAs to use the textured regions described in Haddad188 for Hwang's device. POSITAs would have had a reasonable expectation of success. Ex-1003, ¶213.

3. Claim 12: “The device of claim 1, wherein at least one of said two adjacent light sensitive pixels comprises a textured region.”

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶214-217.

Hwang's imaging device as modified to use Haddad188's textured regions would satisfy this limitation. As shown above, the modification would entail using *a textured region* in each of Hwang's *light sensitive pixels*. See Haddad188, 9:18-21 (“In one aspect, as is shown in FIG. 1, a photosensitive diode 10 can include a semiconductor substrate 12 having multiple doped regions 14, 16 forming at least one junction, and at least one textured region 18 coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation.”); *see also id.*, Fig. 5, 14:29-31.

front side of the pixel” so that the radiation can be “focused within the semiconductor substrate.” Haddad188, 24:34-25:3.

4. Claim 13: “The device of claim 12, wherein said textured region is coupled to the light incident surface.”

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶218-222.

Hwang’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. The modification would entail a textured region that is *coupled to the light incident surface*, given that Haddad188 teaches “locating the textured region on the surface adjacent the incident electromagnetic radiation to purposely effectuate the filtering of blue wavelengths.” Haddad188, 20:32-21:2; *see also id.*, 8:9-10, 14:29-31. Haddad188 also discloses that “a textured region 60 is located on the semiconductor substrate 12 adjacent to the multiple doped regions 14, 16,” *id.*, 21:33-34, or “[a] textured region 156 can be coupled to the semiconductor 72 opposite the lens,” *id.*, 24:32-33.

5. Claim 14: “The device of claim 13, wherein said light incident surface comprises said textured region.”

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶223-226.

Hwang’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. The modification would entail the *light incident surface compris[ing] said textured region*, given that Haddad188 teaches that the “surface

features” of the textured region can be formed directly in a semiconductor material. Haddad188, 16:33-17:2, 14:29-31.

6. Claim 15: “The device of claim 13, wherein said textured region comprises a textured film layer”

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶227-230.

Hwang’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation using *a textured film layer*. Haddad188 discloses that “[t]he textured region can be formed by various techniques, including lasing, chemical etching..., nanoimprinting, additional material deposition, and the like.” Haddad188, 15:20-29. Haddad188 further explains that “material can be removed to a thickness of about 20 μm ,” *id.*, 15:25, which is in the ’359 patent’s suggested range of “1nm to 20 μm .” ’359 patent, 14:22-23. POSITAs would therefore understand that Haddad188’s textured region can be formed as a textured film layer through material deposition. Ex-1003, ¶228.

7. Claim 16: “The device of claim 15, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶231-236.

Hwang's imaging device as modified to use Haddad188's textured regions would satisfy this limitation. Haddad188 discloses a passivation layer 22 at the light incident surface. Haddad188, 20:26-29, Fig.2. Haddad188 also suggests locating a textured region at the point of entry of the electromagnetic radiation into the photosensitive device. *Id.*, 20:32-21:1. Taking these teachings together, a POSITA would have reason to make a textured film layer at the point of entry *compris[ing]* *silicon dioxide* given its passivating quality.

Haddad188 further discloses that “[a] variety of semiconductor materials are contemplated for use with [its] devices” and that the semiconductor material in which the textured region is formed “can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types.” Haddad188, 10:24-27.

POSITAs would seek a transparent material capable of texturing so as not to interfere with the reflective qualities of the layered pixel separation structure of Hwang. Ex-1003, ¶234. Reviewing the groups of materials disclosed in Haddad188 at 10-11, POSITAs would have recognized amorphous silicon and multicrystalline silicon, for example, as materials that may be readily textured and used in transparent applications, depending upon processing. As such, POSITAs would understand that

Haddad188 would rely on such materials for its textured regions, thereby making them obvious to try. Ex-1003, ¶234.

8. Claim 17: “The device of claim 12, wherein said backside surface comprises said textured region.”

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶237-240.

Hwang’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. The modification would entail the *backside surface compris[ing] a textured region*, given that Haddad188 discloses “a textured region 90 is coupled to the semiconductor substrate 72 opposite the doped regions 74,76.” Haddad188, 23:9-10. Moreover, Haddad188 teaches that its textured regions can not only be coupled to the semiconductor substrate but can also be produced within the substrate. *Id.*, 16:3-5 (“One effective method of producing a textured region is through laser processing. Such laser processing allows discrete locations of the semiconductor substrate to be textured.”); 16:15-17. Accordingly, POSITAs would have understood that the backside semiconductor substrate could have a textured region coupled thereto or have a textured region formed directly therein. Ex-1003, ¶238.

- 9. Claim 19: “The device of claim 18, wherein at least one of said light incident surface and said backside surface of at least one of said two adjacent light sensitive pixels comprises a textured region.”**

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶241-243.

As discussed regarding claims 13 and 14, Hwang in view of Haddad188 renders obvious the device of claims 1 and 18 wherein the *light incident surface comprises a textured region*.

As discussed regarding claim 17, Hwang in view of Haddad188 renders obvious the device of claims 1 and 18 wherein the *backside surface comprises a textured region*.

- 10. Claim 20: “The device of claim 19, wherein said textured region is a textured film layer.”**

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶244-245.

See discussion of claim 15.

- 11. Claim 21: “The device of claim 20, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”**

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶246-247.

See discussion of claim 16.

12. Claim 22: “The device of claim 19, wherein said textured region reflects at least a portion of light internally incident thereon into the at least one pixel.”

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶248-251.

Hwang’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. The modification would provide a *textured region* that *reflects at least a portion of light internally incident thereon into the at least one pixel*, given that Haddad188 discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31. Haddad188 further discloses that its textured regions achieve “internal reflection” of “incident electromagnetic radiation” to “allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device.” *Id.*, 15:14–18.

13. Claim 26: “The device of claim 19, wherein the textured region is formed by laser radiation.”

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶252-255.

Hwang’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. The modification would entail forming the *textured region* using *laser radiation*, given that Haddad188 discloses that “[o]ne effective

method of producing a textured region is through laser processing.” Haddad188, 16:3-4; 16:14-19 (“[A] surface of a semiconductor material is irradiated with laser radiation to form a textured or surface modified region.”). Ex-1003, ¶253.

14. Claim 27: “The device of claim 12, wherein the textured region is formed by one of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.”

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶256-259.

As discussed regarding claim 12, Hwang in view of Haddad188 renders obvious an imager device with a textured region. Modifying Hwang’s imaging device according to Haddad188’s processing would satisfy this limitation. Haddad188 discloses that “[a]dditionally, the textured region can be formed by a variety of processes. Nonlimiting examples of such texturing processes can include lazing, chemical etching..., nanoimprinting, material deposition, and combinations thereof.” Haddad188, 2:18-27; *see also id.*, 16:3-13.

15. Claim 28: “The device of claim 12, wherein the textured region is formed by laser radiation.”

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶260-261.

See discussion of claim 26.

16. Claim 29: “The device of claim 12, wherein said textured region is coupled to the backside surface.”

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶262-263.

See discussion of claim 17.

17. Claim 76: “The imager device of claim 1, wherein the peripheral isolation element comprises a textured region.”

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶264-267.

As discussed regarding limitation 1[b], Hwang discloses a *peripheral isolation element* layer 220 at least partially separating adjacent light sensitive pixels. Hwang’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. As discussed and shown above, the modification would entail locating *a textured region* along the *peripheral isolation element*, given that Haddad188 discloses that “FIG. 3 shows a photosensitive device having textured regions 30 located on the sides of the semiconductor substrate 12.” Haddad188, 21:12-13; *see also id.*, 22:21-29, 24:1-15, 14:29-31.

18. Claim 77: “The imager device of claim 1, wherein the peripheral isolation element further comprises a first textured region between the first layer and one of said adjacent pixels and a second textured region between the second layer and the other one of said adjacent pixels.”

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶268-274.

As discussed regarding limitation 1[b], Hwang discloses *peripheral isolation elements* separating *adjacent light sensitive pixels*. Hwang, 6:19-23. Haddad188 discloses that “[t]rench isolation can include dielectric materials, reflective materials, conductive materials, and combinations thereof, including textured regions and other light diffusing features.” Haddad188, 24:5-7; *see also id.*, 21:12-16; Ex-1003, ¶¶269-270.

As discussed regarding limitation 1[e], Hwang discloses a peripheral isolation element that comprises a *first, second, and third layer*. Specifically, Hwang discloses a “second sidewall reflection layer 215 interposed between two first sidewall reflection layers 210.” Hwang, 10:14-17, 10:48-50. Hwang further explains that “the refractive index of the first sidewall reflection layer 210 can be lower than the refractive indexes of the pixel semiconductor pattern 110a and the second sidewall reflection layer 215.” *Id.*, 9:63-66. Because the interfaces formed between these three layers of different refractive indices contributes to the quality of the isolation, it would be logical for POSITAs to put the *textured region* in between the outermost layers of the peripheral isolation element (*first and second layers*) and the *adjacent pixel*. *See supra* §VII.B.2; Ex-1003, ¶271.

Adding a textured region on either side of Hwang’s sidewall multi-layered reflection layer 220, following the teaching of Haddad188’s Figure 2, is consistent

with both references' objective of increasing absorption of electromagnetic radiation and improving isolation. Ex-1003, ¶272.

19. Claim 78: “The imager device of claim 18, wherein the peripheral isolation element comprises a textured region.”

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶275-276.

See discussion of claim 76.

20. Claim 79: “The imager device of claim 18, wherein the peripheral isolation element further comprises a first textured region between the first layer and one of said adjacent pixels and a second textured region between the second layer and the other one of said adjacent pixels.”

This limitation is obvious based on Hwang in view of Haddad188. Ex-1003, ¶¶277-278.

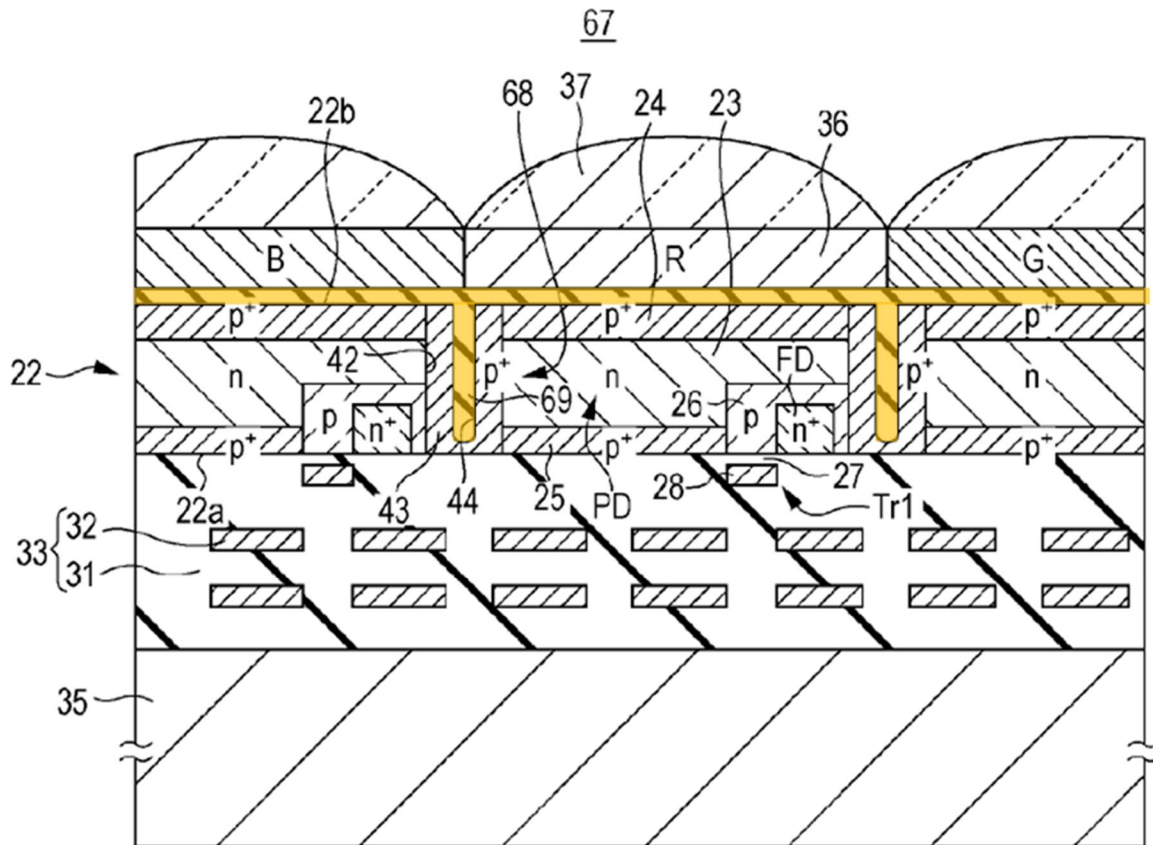
See discussion of claim 77.

C. Ground 3: Claims 6, 8, 9, 11, 24, 30, 32, 34, and 36 Are Obvious Based on Hwang and Shinohara

1. Overview of Shinohara

Shinohara is similarly directed to light-sensitive pixels in imaging devices with pixel separation structures. Shinohara, Abstract. Furthermore, Shinohara describes “an element isolation region for isolating pixels from each other.” *Id.*, [0006]. Shinohara also describes how “leakage of photoelectrically converted charge into an adjacent pixel can be prevented.” *Id.*, [0021]; Ex-1003, ¶¶279-281.

An exemplary embodiment from Shinohara is depicted below.



Id., Fig. 9A (annotated).

Shinohara's Figure 9A is a schematic structural view showing a section of a solid-state imaging device, including insulating film 69. *Id.*, [0032]. "As shown in FIG. 9A, the insulating film 69 can be formed over the entire surface containing the photodiode PD of the surface 22 a as well as in the void 44." *Id.*, [0090]. Shinohara teaches that using an insulating film having a negative fixed charge enhances the passivation characteristics of the element isolation region. *Id.*, [0095]. Accordingly, Shinohara discloses using "a film of hafnium dioxide (HfO_2), dialuminum trioxide (Al_2O_3), ditantalum pentaoxide (Ta_2O_5), dilanthanum trioxide (La_2O_3), or diyttrium trioxide (Y_2O_3)" as insulating film 69. *Id.*, [0091]. See Ex-1003, ¶¶282-283.

2. Motivation to Combine Hwang and Shinohara

It would have been obvious to combine Hwang and Shinohara. Ex-1003, ¶¶284-294.

POSITAs would have been motivated to select from Shinohara's insulating film materials for Hwang's sidewall multi-layered reflective layer. Shinohara notes a known method of using trench-style isolation regions to suppress leakage of charge into an adjacent pixel. Shinohara, [0011]-[0012], [0017]. Accordingly, Shinohara teaches manufacturing a solid-state imaging device by "forming a trench having a predetermined depth in a semiconductor substrate from a surface thereof; and filling a semiconductor layer in the trench by an epitaxial growth to form an element isolation region." *Id.*, [0017].

Hwang discloses that for layer 220, "the refractive index of the first sidewall reflection layer 210 can be lower than the refractive indexes of the pixel semiconductor pattern 110a and the second sidewall reflection layer 215." Hwang, 9:63-66. Hwang discloses a peripheral isolation element comprising at least two materials having different indices of refraction. *Id.*, 10:14-17, 10:45-50. Hwang explains that the refractive index of the first sidewall reflection layer 210 of silicon oxide ($n=1.46$) or air ($n=1$) can be lower than the refractive indexes of the pixel semiconductor pattern 110a and the second sidewall reflection layer 215 (both silicon, $n\approx 4$). *Id.*, 9:28-30, 9:63-66, 10:2-4. POSITAs would have known that the

interface state between Si and SiO₂ existing in the sidewalls of the trench separation structures generates large noises, and causes the S/N ratio to rapidly deteriorate. *See, e.g.,* Iida, [0007]. POSITAs would have been motivated to consider Shinohara to identify other potential materials, within Hwang's constraints, to provide passivation and further improve absorption and sensitivity. Ex-1003, ¶¶285-286.

For example, Shinohara teaches that an insulating film having a negative fixed charge can comprise materials such as "dialuminum trioxide (Al₂O₃)." Shinohara, [0091]. POSITAs would consider using Shinohara's Al₂O₃ for Hwang's first sidewall reflection layer 210 because aluminum oxide exhibits better passivation and lower surface velocity recombination than silicon dioxide. Ex-1010 at 1-3; *see also* '359 patent, 9:54-65. Forming Hwang's pixel isolation groove results in an exposed surface of the silicon substrate. "The sidewall multi-layered reflection layer 220 includes a material layer 210 [(silicon dioxide)] filling the grooves 205 and the residual portion 215 [(silicon)] of the semiconductor layer 110 disposed between the grooves 205." Hwang, 12:53-5; *see also id.*, 13:11-13 ("[A]fter the plurality of grooves 205 is formed, a silicon oxide layer that fills the plurality of grooves 205 can be formed."). However, dark current may be generated from the interface state between Si and SiO₂. Ex-1003, ¶287.

Surface recombination contributes to dark current, which reduces image quality. POSITAs would seek to minimize surface recombination velocity along the

side faces and the bottom face of the trench so that converted charge is retained longer in the silicon substrate for collection. Depositing Shinohara's Al_2O_3 in place of Hwang's first sidewall reflection layer 210 silicon dioxide would provide a surface velocity recombination of about 10 cm/s, Ex-1010 at 2-3, thus improving the image quality of Hwang's imager device. Ex-1003, ¶288.

Further, Shinohara teaches that an insulating film having a negative fixed charge can comprise materials such as "ditantalum pentaoxide (Ta_2O_5) [or] dilanthanum trioxide (La_2O_3)." Shinohara, [0091]. Ta_2O_5 and La_2O_3 are negative fixed charge films offering better passivation than Hwang's silicon dioxide, while also providing indices of refraction that maintain Hwang's teaching to "induc[e] constructive interference of light reflected by at least one boundary in the sidewall multi-layered reflection layer and a boundary between the sidewall multi-layered reflection layer and the pixel semiconductor pattern." Hwang, 2:25-29; Ex-1020 at 9758; Ex-1021 at 46; Ex-1003, ¶289.

Hwang and Shinohara are directed to the same field of endeavor: semiconductor image sensors. Hwang, 1:14-18, 5:47-57; Shinohara, [0051]. Furthermore, Hwang and Shinohara are specifically directed to placing trench isolation structures between adjacent pixels to reduce crosstalk. Hwang, 6:15-17, 10:23-26, 12:42-53; Shinohara, [0021], [0090]; Ex-1003, ¶290.

Further, building a Hwang imager device using the trench isolation structures and materials described in Shinohara (e.g., insulating film 69) would have been nothing more than a simple design choice. As Shinohara teaches, POSITAs understood that “it is important to suppress the occurrence of color mixture caused by leakage of charge (such as electron) photoelectrically converted in the vicinity of the rear surface side into an adjacent pixel.” Shinohara, [0008]; *see id.*, [0094]. POSITAs would have looked to Shinohara to identify a material for Hwang’s pixel separation structure to improve “the rate at which the external light is absorbed by the photodiode 145.” Hwang, 9:12-13. In view of these recognized needs and similarity in structure and function of the isolation trenches in Hwang and Shinohara, POSITAs would have been motivated to look to Shinohara’s alternative designs for trench isolation materials. Ex-1003, ¶¶291-294.

3. Claim 6: “The device of claim 1, wherein at least one of the first and second layer comprises Al_2O_3 .”

This limitation is obvious based on Hwang in view of Shinohara. Ex-1003, ¶¶295-297.

As explained above, it would have been obvious in light of Shinohara to use Al_2O_3 for Hwang’s layer 210 (*first and second layers*).

4. Claim 8: “The device of claim 1, wherein said peripheral isolation element provides a passivating negative charge.”

This limitation is obvious based on Hwang in view of Shinohara. Ex-1003, ¶¶298-300.

As explained above, it would have been obvious in light of Shinohara to use Al_2O_3 for Hwang’s layer 210 (*first and second layers*) and thereby provide a *passivating negative charge*. Shinohara’s insulating film provides a passivating negative charge. Accordingly, the generation of white spots and dark current can be suppressed. Shinohara, [0095] (“When the insulating film having a negative fixed charge is used as the insulating film 69, the hole pinning state by p-type semiconductor layer 43 of the element isolation region 68 can be enhanced.”); *see also id.*, [0021], [0103].

5. Claim 9: “The device of claim 1, wherein said peripheral isolation element exhibits a surface recombination velocity as low as 10 cm/s.”

This limitation is obvious based on Hwang in view of Shinohara. Ex-1003, ¶¶301-302.

As explained above, it would have been obvious in light of Shinohara to use Al_2O_3 for Hwang’s layer 210 (*first and second layers*). Further, POSITAs would seek to lower the surface recombination velocity at the wall of Hwang’s *peripheral isolation element* sidewall multi-layered reflection layer 220 to ensure that the accumulated charge can be collected before it recombines. To this end, POSITAs

would be aware that an aluminum oxide fixed charge layer 210 (*first and second layers*) would *exhibit a surface recombination velocity as low as 10 cm/s*. Ex-1010 at 2-3; *see also* '359 patent, 9:58-60 (“Low surface recombination velocities, as low as 10 cm/s can be obtained through various deposition processes of Al₂O₃ layers on the silicon substrate”); Ex-1003, ¶¶303-305.

6. Claim 11: “The device of claim 1, wherein the peripheral isolation element comprises any of aluminum oxide and hafnium oxide.”

This limitation is obvious based on Hwang in view of Shinohara. Ex-1003, ¶¶303-305.

As explained above, it would have been obvious in light of Shinohara to use Al₂O₃ for Hwang’s layer 210 (*first and second layers*).

7. Claim 24: “The device of claim 18, wherein said at least two materials comprises silicon dioxide and aluminum oxide.”

This limitation is obvious based on Hwang in view of Shinohara. Ex-1003, ¶¶306-308.

As discussed regarding claim 53, Hwang’s sidewall multi-layered reflection layer 220 can be constructed of seven layers, beginning with layer 210 and alternating between material layers 210 and 215. In a seven-layer construct of Hwang’s sidewall multi-layered reflection layer, the layers can therefore be 210 (silicon dioxide) - 215 (silicon) - 210 (silicon dioxide) - 215 (silicon) - 210 (silicon dioxide) - 215 (silicon) - 210 (silicon dioxide). Ex-1003, ¶307.

As explained above, it would have been obvious in light of Shinohara to use Al_2O_3 for Hwang's outermost layers 210. Specifically, to yield the benefits discussed, POSITAs would use aluminum dioxide as a replacement for the outermost sidewall reflection layers 210. The resulting sidewall multi-layered reflection layer structure would be 210 (aluminum oxide; $n=1.76$) - 215 (silicon; $n\approx 4$) - 210 (silicon dioxide; $n=1.46$) - 215 (silicon; $n\approx 4$) - 210 (silicon dioxide; $n=1.46$) - 215 (silicon; $n\approx 4$) - 210 (aluminum oxide; $n=1.76$). Accordingly, this modification would entail a sidewall multi-layered reflection layer 220 *compris[ing] silicon dioxide and aluminum oxide*.

8. Claim 30: “The device of claim 1, wherein said peripheral isolation element comprises tantalum oxide.”

This limitation is obvious based on Hwang in view of Shinohara. Ex-1003, ¶¶309-311.

As explained above, it would have been obvious in light of Shinohara to use Ta_2O_5 for Hwang's layer 210 (*first and second layers*). POSITAs would understand that ditantalum pentaoxide (Ta_2O_5) is *tantalum oxide* and would use these terms interchangeably. See Ex-1018 at B-136 (defining formula of “tantalum oxide” as “ Ta_2O_5 ”).

9. Claim 32: “The device of claim 1, wherein said peripheral isolation element comprises lanthanum oxide.”

This limitation is obvious based on Hwang in view of Shinohara. Ex-1003, ¶¶312-314.

As explained above, it would have been obvious in light of Shinohara to use La_2O_3 for Hwang's layer 210 (*first and second layers*). POSITAs would understand that dilanthanum trioxide (La_2O_3) is *lanthanum oxide* and would use these terms interchangeably. See Ex-1018 at B-98-99 (defining formula of "lanthanum oxide" as " La_2O_3 ").

10. Claim 34: "The device of claim 18, wherein said peripheral isolation element comprises tantalum oxide."

This limitation is obvious based on Hwang in view of Shinohara. Ex-1003, ¶¶315-316.

See discussion of claim 30.

11. Claim 36: "The device of claim 18, wherein said peripheral isolation element comprises lanthanum oxide."

This limitation is obvious based on Hwang in view of Shinohara. Ex-1003, ¶¶317-318.

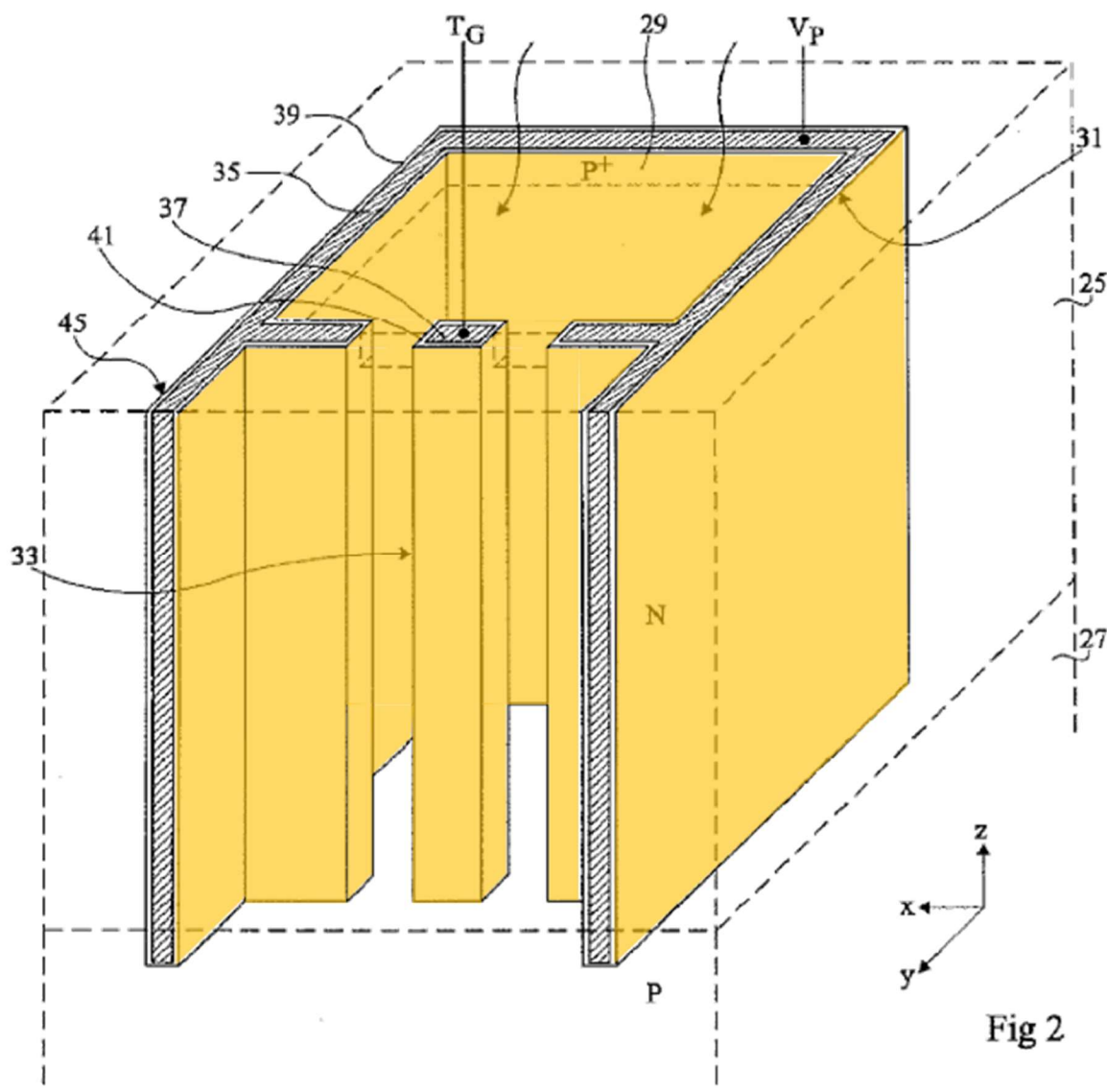
See discussion of claim 32.

D. Ground 4: Claims 44, 51, 65-66, and 71-72 Are Obvious Based on Hwang and Roy

1. Overview of Roy

Roy is similarly directed to light-sensitive pixels in imaging devices with pixel separation structures. Roy, Abstract. Also, like the '359 patent, Roy refers to a "photodiode [that] is delimited by an enclosure comprising a trench." *Id.*, [0050].

An exemplary embodiment from Roy is depicted below:



Id., Fig. 2 (annotated).

Roy's Figure 2 is a perspective view of a photodiode associated with a charge transfer system of an image sensor. *Id.*, [0029]. Among other things, Roy's Figure 2 depicts trenches 31 and 45 and column 33 that may have varying widths, and thin insulating films 39 and 41. *Id.*, [0050], [0057]. *See also* Ex-1003, ¶¶319-323.

2. Motivation to Combine Hwang and Roy

It would have been obvious to combine Hwang and Roy. More specifically, POSITAs would have been motivated to apply Roy's teachings regarding dimensions of pixel separation structures to Hwang's imaging device and would have had a reasonable expectation of success. Ex-1003, ¶324.

POSITAs were concerned with "decreas[ing] the size of image sensor pixels" to decrease volume constraints. Roy, [0007], [0011]. Indeed, Roy discloses a device in which "[h]eavily-doped P-type area 29 may have dimensions approximately equal to 1 x 1 μm ." Roy, [0057]. POSITAs would have recognized that smaller image sensors are particularly beneficial for mobile applications such as smartphones and other hand-held electronics. Ex-1003, ¶325.

Hwang recognizes that "the configuration of the image sensor" can "reduce [its] spectral sensitivity." Hwang, 1:36-38. To limit such problems, Hwang teaches forming sidewall multi-layered reflection layers disposed between the side walls of the pixel semiconductor patterns. *See id.*, 9:41-10:5, 10:17-18. Hwang provides some framework for the dimensions of its sidewalls, suggesting around 160nm and 200nm total for layers 210 and 215, depending on material. *See* Hwang, 10:48-60. Accordingly, POSITAs seeking to implement Hwang's imaging device would be motivated to look elsewhere for further guidance for the dimensions of the device's

sidewall multi-layered reflection layers. POSITAs would look to Roy for this purpose. Ex-1003, ¶326.

Roy notes that the pixel dimensions of prior art imaging devices were “not optimized,” Roy, [0009]; notes, like Hwang, the need to design such devices with “pixels of small dimensions and high storage capacities” with “insulation enabling limiting crosstalk,” *id.*, [0011], [0012-0015]; and teaches pixel separation structure dimensions that achieve such objectives, *id.*, [0057], [0045], [0053], [0069].

POSITAs would have had a reasonable expectation of success in combining Hwang and Roy. Both Hwang and Roy are directed to image sensor devices comprising light-sensitive pixels, including specifically the design of trench isolation structures placed between adjacent pixels to reduce crosstalk. *See, e.g.*, Hwang, 10:36-60; Roy, Abstract, [0057]. Given the similarities in structure, scale, and function of the image sensors and pixel separation structures taught by Hwang and Roy, building Hwang’s imaging device using the pixel isolation structure dimensions taught by Roy would have been a simple design choice for applying a known technique to yield a predictable result. Ex-1003, ¶¶327-329.

It would have been well within POSITAs’ abilities to use the dimensions taught by Roy in forming the pixel separation structures in Hwang’s device; indeed, it would have involved routine manufacturing steps that both Hwang and Roy disclose. *See, e.g.*, Hwang, 12:42-53; Roy, [0082]. Roy also teaches that its pixel

separation structure dimensions increase “manufacturing simplicity,” Roy, [0079], further motivating the POSITA to use them for Hwang’s device and further reinforcing the POSITA’s expectation of success. Ex-1003, ¶330.

3. Claim 44: “The device of claim 1, wherein said peripheral isolation element has a width in a range from about 100 nm to about 50 microns.”

This limitation is obvious based on Hwang in view of Roy. Ex-1003, ¶¶331-334.

As discussed regarding claim 1, Hwang discloses a *peripheral isolation element* comprising a “sidewall multi-layered reflection layer 220.” Roy discloses that its trench 31/45 and column 32 “may have a width of approximately 0.2 μ m and be separated, at the level of the interruption area of trench 31, by a distance approximately equal to 0.2 μ m,” i.e., 200 nm. Roy, [0057].

4. Claim 51: “The device of claim 18, wherein said peripheral isolation element has a width in a range from about 100 nm to about 50 microns.”

This limitation is obvious based on Hwang in view of Roy. Ex-1003, ¶¶335-336.

See discussion of claim 44.

5. Claim 65: “The imager device of claim 64, wherein said trench isolation element has a depth in a range of about 100 nm to about 50 microns.”

This limitation is obvious based on Hwang in view of Roy. Ex-1003, ¶¶337-340.

As discussed regarding claim 64, Hwang discloses a *trench isolation element*. Roy discloses that “[a]ccording to an embodiment, the trench and the column have depths ranging between 1 and 10 μm , the conductive material in the trench and in the column is polysilicon, and the material forming the insulated walls of the column and of the trench is selected from the group comprising silicon oxide, silicon nitride, silicon oxynitride, or is formed of a multiple-layer stack of these materials.” Roy [0020].

6. Claim 66: “The imager device of claim 65, wherein said trench isolation element has a width in a range of about 100 nm to about 10 microns.”

This limitation is obvious based on Hwang in view of Roy. Ex-1003, ¶¶341-344.

As discussed regarding claim 65, Hwang discloses a *trench isolation element*. Roy discloses that “[t]rench 31/45 and column 33 may have a width of approximately 0.2 μm and be separated, at the level of the interruption area of trench 31, by a distance approximately equal to 0.2 μm ,” i.e., 200 nm. Roy [0057].

7. Claim 71: “The imager device of claim 70, wherein said trench isolation element has a depth in a range of about 100 nm to about 50 microns.”

This limitation is obvious based on Hwang in view of Roy. Ex-1003, ¶¶345-346.

See discussion of claim 65.

8. **Claim 72: “The imager device of claim 71, wherein said trench isolation element has a width in a range of about 100 nm to about 10 microns.”**

This limitation is obvious based on Hwang in view of Roy. Ex-1003, ¶¶347-348.

See discussion of claim 66.

VIII. DISCRETIONARY DENIAL IS INAPPROPRIATE

The Board should not exercise its discretion to deny institution under 35 U.S.C. §314(a). No other petitions have been filed against the '359 patent and thus the *General Plastic* factors for serial petitions do not weigh against institution. The existence of a parallel ITC proceeding should not be a factor for consideration in determining whether the Board may exercise its discretion to deny institution. *See* Vidal, K., Memorandum—Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, USPTO (June 21, 2022) at 6-7, https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621.pdf. The parallel district court case has been stayed. Discretionary denial is further inappropriate because this petition presents compelling evidence of unpatentability. Accordingly, the *Fintiv* factors should not be applied to deny institution of this proceeding.

IX. CONCLUSION

Petitioner respectfully requests *inter partes* review and cancellation of the Challenged Claims of the '359 patent.

Date: November 29, 2024

Respectfully submitted,

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CERTIFICATION OF WORD COUNT

I certify that the foregoing complies with the type-volume limitation of 37 C.F.R. § 42.24 and contains 13,412 words based on the word count indicated by the word-processing system used to prepare the paper, and excluding those portions exempted by § 42.24(a).

Date: November 29, 2024

/Dave A. Garr /

Dave A. Garr (Reg. No. 74,932)

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6 and 42.105, I hereby certify that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,224,359 under U.S.C. §§ 311-319 and 37 C.F.R. § 42.100 *et seq.*, together with its supporting exhibits, Power of Attorney, and Explanation of Parallel Petitions was served by Federal Express for Saturday delivery, a means at least as fast and reliable as Priority Mail Express®, on the following correspondence address of record for patent owner:

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