

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Samsung Electronics Co., Ltd.,
Petitioner,

v.

SiOnyx, LLC,
Patent Owner.

Case No. IPR2025-00163
Patent No. 10,224,359

**DECLARATION OF DR. MICHAEL LEBBY IN SUPPORT OF PETITION
FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,224,359**

Petition B, Based on Primary Reference of Hwang

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I. INTRODUCTION

1. I, Michael Lebby, declare as follows.

2. I have been retained as a technical consultant on behalf of Samsung Electronics Co., Ltd. (“Samsung” or “Petitioner”), which I understand to be the petitioner in the present proceeding. I have been asked to consider whether the references listed as Exhibits 1006-1009 below disclose or render obvious the limitations recited in claims 1-30, 32, 34, 36, and 38-83 of U.S. Patent No. 10,224,359 (Ex-1001, “’359 patent”). I have also been asked to consider the state of the art and the “prior art,” i.e., references, available before the time of the alleged invention of the ’359 patent. My opinions are provided in this declaration.

3. I am being compensated at my standard consulting rate for my time. My compensation is in no way contingent on the results of these or any other proceedings relating to the ’359 patent.

II. BACKGROUND AND QUALIFICATIONS

4. A description of my professional background and qualifications is provided below. An additional account of my work experience and qualifications is included in my *curriculum vitae*, which is Ex-1004 (“CV”).

5. I am currently the CEO and CTO at GenusTechnik Inc., which provides consulting services in areas that include image sensors, photonics, optoelectronics, semiconductors as used in image sensors and other optical applications.

6. In addition, I am currently the Chairman, CEO, and Director of the Board of Directors for Lightwave Logic. As CEO, I successfully guided Lightwave Logic to up-list to NASDAQ in September 2021 organically (i.e., without the raising of financing), and I led the company to acceptance in the Russell 3000 index in 2022.

7. I have led and run optoelectronics start-ups, and I have commercialized optoelectronic and photonics technologies into volume manufacturing. I have also worked as a Corporate Venture Capitalist specializing in optical communications, photonics, sensing, electronics, and semiconductors, and I am currently a technical expert advising the European Commission regarding evaluation of numerous photonic technology proposals, including image sensor proposals. I am a Fellow Member of the National Academy of Inventors (NAI), the IEEE, and Optica (OSA), and I was voted Photonic Integrated Circuit (PIC) business leader of the year by the PIC International Conference in 2018.

8. In particular, my technical expertise has included the design of components for photonics technology that can source light as well as receive and detect light. These components include LEDs, ICs, lasers, photodetectors, diodes, image sensors, etc. In many of my industrial and commercial roles in the photonics industry I have used, designed, optimized, and improved photonic materials, components, and packages both through solutions of engineering problems as well as patents and publications.

9. Over the course of my career in photonics, optoelectronics, and optical technology in general, I have worked in nearly every aspect of the field, including optical assembly, laser diodes, photodetectors, image sensors, LEDs, integrated circuits (e.g. drivers, and other basic electronic digital and analog functions), as well as fiber optics. In particular, I have designed optoelectronic devices such as LEDs, laser diodes (VCSELs – vertical cavity surface emitting lasers), photodiodes, image sensors, and solar cells with a focus on efficient optical device design that maximizes device performance. For example, I have worked on improving light extraction efficiency in laser diodes as well as LEDs, where these devices are utilized in modules. I have also worked on arrays of detectors for sensing applications.

10. I started my career in 1977 at the Ministry of Defense (United Kingdom), in the Royal Electrical and Mechanical Engineers as a telecommunications apprentice. At the Ministry of Defence, I studied material and characterization issues relating to Gallium Arsenide (GaAs) and Indium Phosphide (InP) optoelectronic devices, as well as semiconductor device design, fabrication, and characterization, particularly with materials using III-V semiconductors. I also worked with silicon for integrated circuits, silicon photonics, and ceramic-based radio-frequency (RF) electronic packaging that included low-temperature co-fired ceramic. These devices and materials were utilized in photonic-based transceiver

packages and modules. I also worked on electronics, motors, sensors, and other technologies that combined photonics with electronics.

11. I attended the University of Bradford, where I obtained a Bachelor's of Engineering (Electrical Engineering), with honors, in 1984, an MBA in 1985 and a Ph.D. (Electrical Engineering) in 1987. My Ph.D. thesis related to the characterization and fabrication of both optoelectronic and electronic semiconductor devices that included the detection of light. In 2004, I was awarded a Doctor of Engineering (a Doctorate degree higher than a Ph.D.) from the University of Bradford for my "Technical Contributions to Optoelectronics." This was only the second time in the University of Bradford's history that a Doctor of Engineering was granted based on industry experience.

12. While attending the University of Bradford and for a few years thereafter, i.e., from 1985 to 1989, I worked as a researcher in the Photonics Research Department of AT&T Bell Labs ("Bell Labs"). At Bell Labs, I focused my research on novel device designs using III-V semiconductor material systems including FETs, bipolar transistors, LEDs, laser diodes, and photodetectors. My research at Bell Labs became the subject of my Ph.D. thesis.

13. After completing my Ph.D. at the University of Bradford and my work at Bell Labs, I became a Research and Development Manager ("R&D Manager") in the photonics division of Motorola's Corporate R&D Labs ("Motorola"). I worked

at Motorola from 1989 to 1998, where my responsibilities included research and development in optical interconnects, electrical and fiber optic connectors, optical/electrical engines, electronic ICs, displays, laser devices, LEDs, optical lenses, image sensors, and optical waveguides, as well as the packaging and reliability of mobile product prototypes. Some of the prototypes on which I worked included moving parts with motors (both standard as well as semiconductor MEMs based), and phased array optical beams that could direct and re-direct optical beams. While at Motorola, I was the inventor or co-inventor on over 150 utility patents, and I received a special award from the Chairman of Motorola in 1998 for exemplary patent accomplishments. At that time, I had the highest number of issued utility patents in the history of Motorola.

14. As an R&D Manager at Motorola, I initiated Motorola's work in optical interconnect technology (known at Motorola as "Optobus"TM) and associated optical connectors, electronics, and photonics components, and I was also involved in research and development on the IC chip designs that this parallel interconnect module utilized. In this project, transparent plastics were developed and molded onto standard metallic lead frames for both light-emitting devices (e.g., LEDs, VCSELs) and photodetectors, which collect light and convert it into an electronic signal. These transparent lead frame packages were developed in volume production at Motorola. I also worked on various techniques to improve both photonics-based detectors such

as photodetectors, image sensors, as well as photonics-based emitters such as lasers and LEDs, both as individual components as well as in arrays of multiple components.

15. In 1998, I left Motorola to join TE Connectivity (previously Tyco Electronics) as Director of Technology and Business Development. In that role, I helped develop technology strategy for optical communications, optoelectronic transceivers, and fiber optic connector and adapter products for the Global Optoelectronics Division. My work included designing and characterizing photodetectors, sensors, LEDs, laser-based photonic packages and modules for product manufacturing.

16. In 1999, I joined Intel Capital (“Intel”) as Director of Business Development and as a corporate investor. My work at Intel included sourcing, negotiating, and closing private placement equity deals in the optical networking, photonic component, interconnect, optical lens, image sensor, and semiconductor industries. My work at Intel also included investigating the investment of Intel Capital equity in photonic devices, optical beams, and other technologies to support the physical movement of optical signals. I also was one of the founders of Intel’s silicon photonics division, which worked to establish a fabrication facility in South San Jose to investigate silicon-based image sensors and the integration of silicon FET electronics with optoelectronics into the same silicon semiconductor wafer.

17. From 2005 to 2010, I served as the Executive Director, President, and CEO of the Optoelectronic Industry Development Association (OIDA) – a trade association that represented photonics manufacturers in the fields of photonic sensing fiber optics, display, defense, aerospace, LED lighting and automotive/motor vehicles. I was responsible for organizing technical conferences, workshops and forecasts using industry roadmaps, all of which featured a portfolio of photonics technology that included: optical sensors, free-space optics, optical interconnects, fiber optics, optical communications, automotive photonic technologies, wavelength division multiplexing, LEDs, displays and their associated packaging.

18. In 2010, I became the General Manager and CTO of Translucent, Inc., a start-up company that developed and manufactured silicon and rare earth oxide-based epitaxial semiconductor wafers.

19. I was employed by Glyndŵr University from 2013 to 2015 as a Professor of Optoelectronics, where I focused on the design, simulation, and testing of high-speed, low-power photonic integrated circuits, optoelectronic integrated circuits, laser diodes, optics, and solar cells for applications that included communications, automotive, displays, sensing, and energy.

20. From 2013 to 2015, I was also employed as the President and CEO of OneChip Photonics Corporation, where I additionally served as an elected

independent board member. In these roles, I focused on technical, business, and operational strategy for fiber optic communications based on InP photonic integrated circuits, as well as optoelectronic integrated circuits for fiber optic transceivers that incorporated electrical and optical multiplexing schemes using fiber optic connectors.

21. Over the course of my career, I have also led panels and given numerous keynote and invited presentations, speeches, and talks at workshops and conferences, including on photonic and optoelectronic materials, devices, components, packages as well as photonics technology in general.

22. Due to my passion for optics, I have been elected to the London Guild of Spectacle Makers. A more detailed description of my education, as well as my training and experience in the relevant technology, is included in my CV.

23. I hold over 340 combined issued USPTO patents and published USPTO patent applications that have been derived from over 230 issued U.S. utility patents, mostly in the field of optoelectronics, photonics, electronics, and semiconductors. I have been cited by the USPTO to be in the most prolific seventy-five inventors in the United States from 1988 to 1997.

24. I have authored approximately 65 publications and have achieved over 400 media events that include: technical articles, books, chapters, invited speaker events at conferences as well as interviews that included TV, video, radio, and social,

industrial, professional media in general. This includes technical, business-related, and financial conferences as a contributing, invited, and keynote speaker. Details can be found in my CV. Over the past decade, I have been a project reviewer and technical expert for the European Commission on numerous occasions.

25. I have also served as an expert witness on numerous patent matters, including 50 IPR proceedings and 5 PGR proceedings. I have also been deposed on more than 60 occasions, including in ITC and District court proceedings.

26. A complete listing of these patents, publications, articles, lectures, and other public media is included with my CV.

27. On the basis of my education and the experience described above, I believe I am qualified to give the opinions set out herein.

III. MATERIALS REVIEWED

28. I am not an attorney and offer no legal opinions. However, in my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art. See Section VI.B below for the level of ordinary skill in the art for this declaration.

29. In preparing this declaration, I reviewed the '359 patent, including the claims of the patent in view of the specification; the prosecution history of the '359 patent; and numerous publications and technical references from and preceding the

time of the alleged invention. More specifically, I have reviewed each of the following:

Exhibit	Description
1001	U.S. Patent No. 10,224,359 (the “’359 patent”)
1002	File History for U.S. Patent No. 10,224,359
1003	Declaration of Dr. Michael Lebby
1004	Curriculum Vitae of Dr. Michael Lebby
1005	U.S. Patent Application Publication No. 2011/0156186 (Iida)
1006	U.S. Patent No. 7,675,099 (Hwang)
1007	International Publication No. WO 2011/035188 (Haddad188)
1008	U.S. Patent Application Publication No. 2012/0033119 (Shinohara)
1009	U.S. Patent Application Publication No. 2009/0266973 (Roy)
1010	P. Saint-Cast et al., “Very low surface recombination velocity on p-type c-Si by high-rate plasma-deposited aluminum oxide,” <i>Appl. Phys. Lett.</i> , 95, 151502 (2009), pp. 1-3, Oct. 14, 2009 (Saint-Cast)
1011	Samsung’s Proposed Constructions, Inv. No. 337-TA-1403 (Aug. 27, 2024)
1012	SiOnyx’s Proposed Constructions, Inv. No. 337-TA-1403 (Aug. 27, 2024)
1013	Email from N. Subhedar re: Claim Construction M&C Follow-Up (Sept. 8, 2024)
1014	Joint Claim Construction Chart, Inv. No. 337-TA-1403 (Nov. 1, 2024)
1015	Simon M. Sze, <i>Physics of Semiconductor Devices</i> (2nd ed. 1981)
1016	Georg Haas & Calvin D. Salzberg, “Optical Properties of Silicon Monoxide in the Wavelength Region from 0.24 to 14.0 Microns,” <i>J. Opt. Soc. Am.</i> , vol. 44, no. 3, pp. 181-87, Mar. 1954 (Haas)
1017	F. López & E. Bernabéu, “Refractive Index of Vacuum-Evaporated SiO Thin Films: Dependence on Substrate Temperature,” <i>Thin Solid Films</i> , 191 (1990), pp. 13-19 (Lopez)
1018	CRC Handbook of Chemistry and Physics (67th ed. 1986)
1019	Quick Reference Manual for Silicon (1985)
1020	A.X. Wei et al., “Electrical and optical properties of tantalum oxide thin films prepared by reactive magnetron sputtering,” <i>J. Alloys Compd.</i> , 509 (2011), pp. 9758-63 (Wei)
1021	Tero Pilvi (2008). <i>Atomic Layer Deposition for optical applications: metal fluoride thin films and novel devices</i> [Academic Dissertation University of Helsinki] ISBN 978-952-92-4814-8, 978-952-10-5133-3, http://ethesis.helsinki.fi .

Exhibit	Description
1022	E. Yablonovitch et al., “Unusually Low Surface-Recombination Velocity on Silicon and Germanium Surfaces,” <i>Phys. Rev. Lett.</i> , vol. 57, no. 2, pp. 249-52, Jul. 14, 1986
1023	J. Woollam et al., “Overview of Variable Angle Spectroscopic Ellipsometer (VASE), Part I: Basic Theory and Typical Applications,” <i>Crit. Rev. Opt. Sci. Technol.</i> , vol. CR72 (1999), pp. 3-28

IV. RELEVANT LEGAL STANDARDS

30. I am not an attorney. For the purposes of this declaration, I have been informed about certain aspects of the law that are relevant to forming my opinions. I have applied the following understanding of the law.

31. I have been informed that a patent claim may be “anticipated” if each element of that claim is present either explicitly or inherently in a single prior art reference, and that the elements should be arranged in the reference as in the claim. Petitioner’s counsel has informed me that for a claimed limitation to be inherently present, the prior art need not expressly disclose the limitation, so long as the claimed limitation necessarily flows from a disclosure in the prior art.

32. I have been informed that a patent claim can be considered to have been obvious to a person of ordinary skill in the art at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a person of ordinary skill in the art at the time the application was filed.

33. I have been informed that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

34. I have been informed that a single reference can render a patent claim obvious if any differences between that reference and the claims would have been obvious to a person of ordinary skill in the art. Alternatively, the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to one having ordinary skill in the art. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider, among other factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, and when combined, would yield predictable results;
- whether a person of ordinary skill in the art could implement a predictable variation, and would see the benefit of doing so;

- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by those skilled in the art;
- whether a person of ordinary skill would have recognized a reason to combine known elements in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

35. I have been informed that one of ordinary skill in the art has ordinary creativity and is not an automaton. I have been informed that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

36. I understand that various objective or “real world” factors may be indicative of non-obviousness. I understand that such factors include:¹

- the commercial success of the claimed invention;

¹ I am not aware of any objective evidence of non-obviousness having been identified in connection with the '359 patent.

- the existence of a long-felt, unresolved need for a solution to the problem solved by the claimed invention;
- failed attempts to solve the problem solved by the claimed invention;
- copying of the claimed invention;
- unexpected results of the claimed invention;
- praise for the claimed invention by others in the relevant field; and
- willingness of others to accept a license under the patent because of the merits of the claimed invention.

V. TECHNOLOGY BACKGROUND

37. Since the early 2000s, digital cameras and camcorders have become increasingly popular, largely due to the development of advanced image sensors. These sensors play a critical role in converting visual information into electrical signals, which are then processed to create digital images or videos. At the heart of an image sensor lies an array of light-sensitive pixels, each of which is a photodiode capable of detecting light. The photodiode's function is to convert incoming light photons into electrons; the quantity of electrons collected at each pixel determines the pixel's brightness. By assembling this data across all pixels, the sensor constructs a coherent image or video corresponding to the captured scene.

38. In an ideal scenario, an image sensor would achieve perfect efficiency, converting every photon that strikes it into a collected electron. However, in practice,

some photons are lost during the conversion process. The efficiency of this conversion is quantified by a metric known as external quantum efficiency, or quantum efficiency for short. Quantum efficiency is defined as the percentage of photons incident on an image sensor that are converted into collected electrons. '359 patent, 4:31-34. Some incident photons may be lost because they are reflected off before reaching the semiconductor layer including a photodiode; others may be lost because they pass through the semiconductor layer without being absorbed. To mitigate such losses, it is common practice to include in an image sensor microstructures that let more light into the semiconductor layer including a photodiode, as well as microstructures that reflect and scatter light that leaves the semiconductor layer back into the semiconductor layer.

39. Photodiodes are typically fabricated by doping a semiconductor layer to create a junction, which is used for sensing light. A photodiode junction is then connected to a neighboring metallization layer, which carries the electrical signal to external circuits that integrate the signals from all pixels to form a complete image. In the design of image sensors, the side of the semiconductor layer where the photodiode junction and the metallization layer are located is referred to as the “front side,” while the opposite side is known as the “backside.” Image sensors can be designed to receive light from either the front side (front side illuminated, or FSI) or

the backside (backside illuminated, or BSI), each offering different advantages and trade-offs.

40. Front side illuminated sensors are easier and less costly to manufacture, but they suffer from greater light loss because the incident light must pass through the metallization layer before reaching the photodiode junction. This can reduce the sensor's overall efficiency and image quality, especially in low-light conditions. Conversely, backside illuminated sensors are more challenging and expensive to produce but offer superior performance because the incident light directly reaches the photodiode junction without passing through the metallization layer. This design reduces light loss and improves the sensor's quantum efficiency, leading to better image quality, particularly in demanding lighting environments.

VI. OVERVIEW OF U.S. PATENT NO. 10,224,359

A. Summary

41. The '359 patent relates to image sensor pixels and elements for trapping light within such pixels. '359 patent, 6:16-20. The patent states that a reduction in the size of pixels in an image sensor can sacrifice image quality. '359 patent, 1:24-26. According to the patent, reduced pixel size for image sensors tends to increase electrical and optical crosstalk between adjacent pixels, and image signal-to-noise tends to decrease. '359 patent, 1:26-28. The patent purportedly provides for

semiconductor devices with, for example, “enhanced light detection properties.”
'359 patent, 6:13-16.

42. The patent refers to “light trapping elements” that can “isolate neighboring pixels in an image sensor.” '359 patent, 6:18-20. The isolation elements can be configured “to optically and/or electrically isolate neighboring pixels from one another in addition to trapping light within the pixel.” '359 patent, 6:20-22. The patent also refers to isolation elements as “trench isolation features” or “sidewalls.” '359 patent, 7:42-43.

43. The patent broadly asserts that a “variety of reflective materials can be utilized in constructing the isolation features in order to provide optical isolation, light trapping, and/or electrical isolation,” and that “any such material capable of incorporation into a photosensitive device” is within the patent’s scope. '359 patent, 7:64-8:1. Examples of such materials include a Bragg reflector or a metal reflector, including for example “silver, aluminum, gold, platinum, reflective metal nitrides, reflective metal oxides, and the like.” '359 patent, 8:1-9. The isolation elements can be doped to affect properties of the material with respect to electrical isolation. '359 patent, 8:13-16.

44. According to the patent, a light sensitive pixel can have “a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least

substantially around the pixel periphery.” ’359 patent, 1:43-48. Furthermore, the pixel can include “a backside light trapping material substantially covering the backside surface and a peripheral light trapping material substantially covering the peripheral sidewall.” ’359 patent, 1:48-51. Light that contacts the peripheral light trapping material or backside light trapping material is “reflected back toward the pixel.” ’359 patent, 1:51-54. The patent states that “light entering the pixel that is not absorbed will interact with and be reflected internally” by backside or peripheral sidewall light trapping materials, for example. ’359 patent, 12:26-31. Light is “effectively maintained inside the pixel until it is absorbed.” ’359 patent, 12:31-32. There may also be an “array” of light trapping pixels. ’359 patent, 1:54-55.

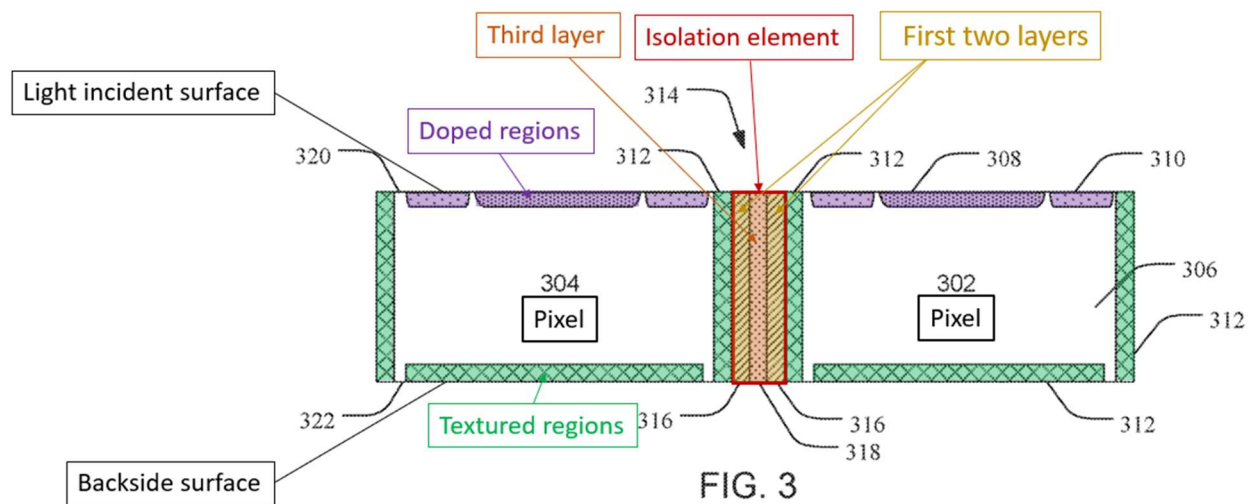
45. The isolation element can include at least two layers comprising material having a lower optical refractive index² as compared to the material of a third layer disposed or sandwiched between those two layers. ’359 patent, 8:36-40. In this case, the isolation element functions as a Bragg reflector. ’359 patent, 8:35-36. The patent states that a large index of refraction “mismatch” can result in “total reflection at the trench side walls.” ’359 patent, 9:26-28.

² Herein I use the term “refractive index” to refer to optical refractive index.

46. The pixel may also include a “textured region.” ’359 patent, 6:45-47.

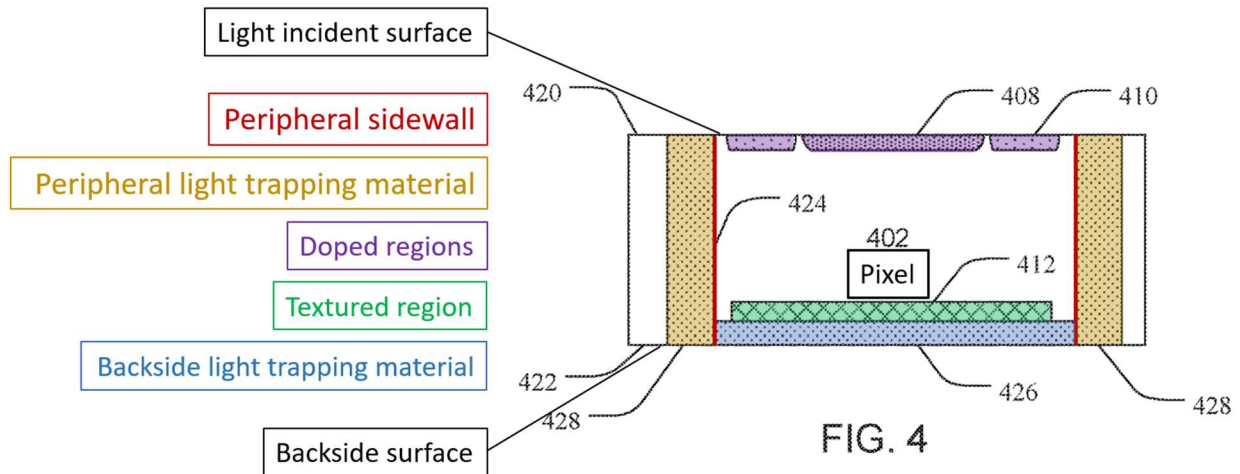
“[A] textured region typically has a textured surface that increases the surface area and increases the probability of radiation absorption.” ’359 patent, 15:27-30.

47. Figure 3 is a cross-sectional view of multiple image sensor pixels in accordance with an embodiment discussed in the patent. '359 patent, 3:37-39. Figure 3 is provided below.



'359 patent, Fig. 3 (annotated); *see* '359 patent, 10:63-11:12.

48. Figure 4 is a cross-sectional view of a light trapping pixel discussed in the patent. '359 patent, 3:40-42. Figure 4 corresponds to the “Species 4” elected by the applicant during prosecution. Ex-1002 at 1696. Figure 4 differs from Figure 3 in that it depicts one pixel (rather than two), and in that it depicts “backside light trapping material.” '359 patent, 11:22-24. Figure 4 is provided below.



'359 patent, Fig. 4 (annotated); *see* '359 patent, 11:13-34.

B. Level of Ordinary Skill in the Art

49. It is my understanding that factors defining the level of ordinary skill in the art include: (1) the types of problems encountered in the art; (2) the prior art solutions to those problems; (3) the rapidity with which innovations are made; (4) the sophistication of technology; and (5) the educational level of active workers in the field.

50. A person of ordinary skill in the art ("POSITA") as of March 2012 would have had a bachelor's degree in engineering, physics, or a related or equivalent field, and two or more years of experience researching, developing, designing, and/or evaluating image sensors using photonics. A person with less or different education but more relevant practical experience, or vice versa, may also meet this standard.

51. I met this definition of a POSITA as of March 2012. I applied this definition of a POSITA in forming my opinion in this declaration. I understand that SiOnyx, LLC (“SiOnyx” or “Patent Owner”) asserted the ’359 patent in a related case, *Sensors with Pixels and Products Containing the Same*, Inv. No. 337-TA-1403 (the “Related Case”). I understand that Patent Owner’s expert in the Related Case opined that “[t]he level of ordinary skill for the Asserted Patents should be defined as a person having at least a bachelor’s degree in electrical engineering, materials science, or physics, (or an equivalent technical degree), at least two years of experience in optoelectronics, and at least three years of work experience in semiconductor manufacturing. Further, a master’s degree or Ph.D. in a relevant field may substitute for some work experience or vice versa.” I met Patent Owner’s definition of a POSITA as of March 2012. My opinions remain the same under Patent Owner’s definition.

C. Claim Construction

52. I understand that in this proceeding, the claims should be construed in accordance with their ordinary and customary meaning in light of the specification, as understood by one of ordinary skill in the art. I have therefore applied those plain and ordinary meanings in my analysis.

53. I understand that, in the Related Case, Petitioner and Patent Owner have proposed competing constructions for certain terms of the ’359 patent. *See* Ex-1011; Ex-1012; Ex-1013; Ex-1014.

54. For purposes of my opinions, I was asked to apply the parties' proposed constructions where both parties' proposed constructions were available and consistent with the plain and ordinary meaning. Where the parties' constructions may have impacted my analysis, I address each as is relevant below.

VII. CLAIMS ANALYSIS

A. Ground 1: Claims 1-5, 7, 10, 18, 23, 25, 38-43, 45-50, 52-64, 67-70, 73-75, and 80-83 Are Anticipated or Rendered Obvious by Hwang

1. Overview of Hwang

55. I understand that Hwang is prior art because it issued on March 9, 2010, before the '359 patent's provisional application filing date of March 22, 2012.

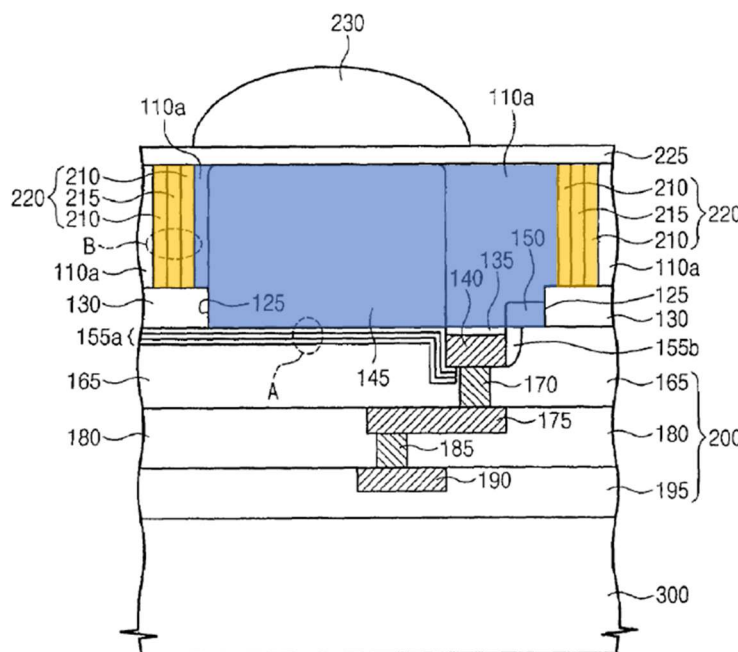
56. Hwang was not cited in any IDS and was not discussed during prosecution of the '359 patent.

57. Like the '359 patent, Hwang is directed to light-sensitive pixels in imaging devices. Hwang, Abstract ("Provided are an image sensor and a method of forming the image sensor. The image sensor has a base multi-layered reflection layer interposed between a photodiode and interlayer insulating layer. The photodiode has a first surface adjacent to the interlayer insulating layer and a second surface opposite the first surface. Here, external light is incident on the second surface of the photodiode. Also, the image sensor includes a sidewall multi-layer reflection layer that encloses the photodiode."). Furthermore, like the '359 patent, Hwang is concerned with improving image quality by increasing the percentage of incident

light absorbed by the photodiode. Hwang, 1:31-36. “The higher the percentage of incident light absorbed by the photodiode, the higher the spectral sensitivity.” Hwang, 1:31-34. Hwang further explains that longer wavelength light is less likely to be absorbed completely by the photodiode, thus reducing spectral sensitivity. Hwang, 1:41-48.

58. An exemplary embodiment from Hwang is depicted below.

Fig. 2



Hwang, Fig. 2 (annotated).

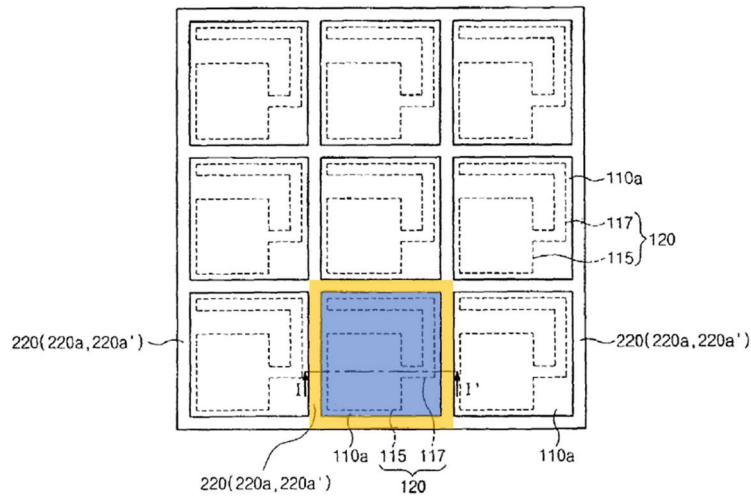
59. Figure 2 of Hwang shows a cross-sectional view of an image sensor. Hwang, 4:59-63, 5:47-51. Among other things, Figure 2 depicts a “sidewall multi-layered reflection layer 220” (shown in orange) “provided between the side walls of the pixel semiconductor patterns 110a” (shown in blue). Hwang, 6:7-9. And “the

sidewall multi-layered reflection layer 220 includes layers with different respective refractive indexes.” Hwang, 6:11-13. Hwang shows that the sidewall multi-layered reflection layer 220 is “disposed along the boundaries of all of the pixel semiconductor patterns 110a” to “enclose[] the side walls of the pixel semiconductor patterns 110a.” Hwang, 6:15-21. “[A]ll of the pixel semiconductor patterns 110a can thus be separated by the sidewall multi-layered reflection layer 220.” Hwang, 6:21-23. As shown in Figure 2, “[e]ach pixel semiconductor pattern 110a has a photodiode 145 disposed therein.”³ Hwang, 5:57-58.

60. As shown in the plan view of Figure 1 (below), a plurality of pixel semiconductor patterns 110a are arranged in rows and columns on the substrate to form an image sensor. Hwang, 5:47-54.

³ While Hwang calls element 145 a “photodiode,” POSITAs would understand that photodiode, i.e., the structure that converts light into an electrical signal, encompasses more than just element 145, and would further include the surrounding pixel semiconductor patterns 110a. The photodiode comprises a junction created between the differently doped semiconductor regions. *See, e.g.*, Hwang, 6:3-4 (“Therefore, the photodiodes 145 form a PN junction with the pixel semiconductor pattern 110a.”); *see generally id.*, 5:52-6:6.

Fig. 1



Hwang, Fig. 1 (annotated).

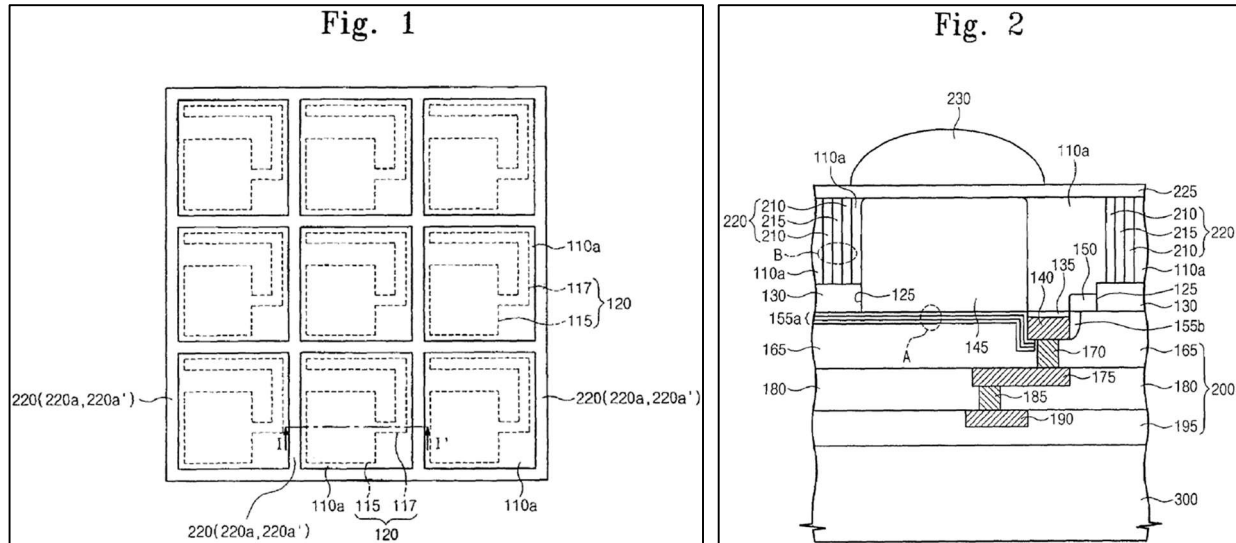
2. Claim 1

a) Element 1 ``` [pre]: “An imager device, comprising:” ```

61. Hwang teaches or suggests this preamble.

62. Hwang discloses an “image sensor that converts incident light to electrical signals.” *See, e.g.*, Hwang, 1:14-18. Figure 1 shows a plan view of an image sensor, and Figure 2 shows a cross-sectional view of such image sensor.

Hwang, 4:59-63, 5:47-51.



Hwang, Figs. 1-2.

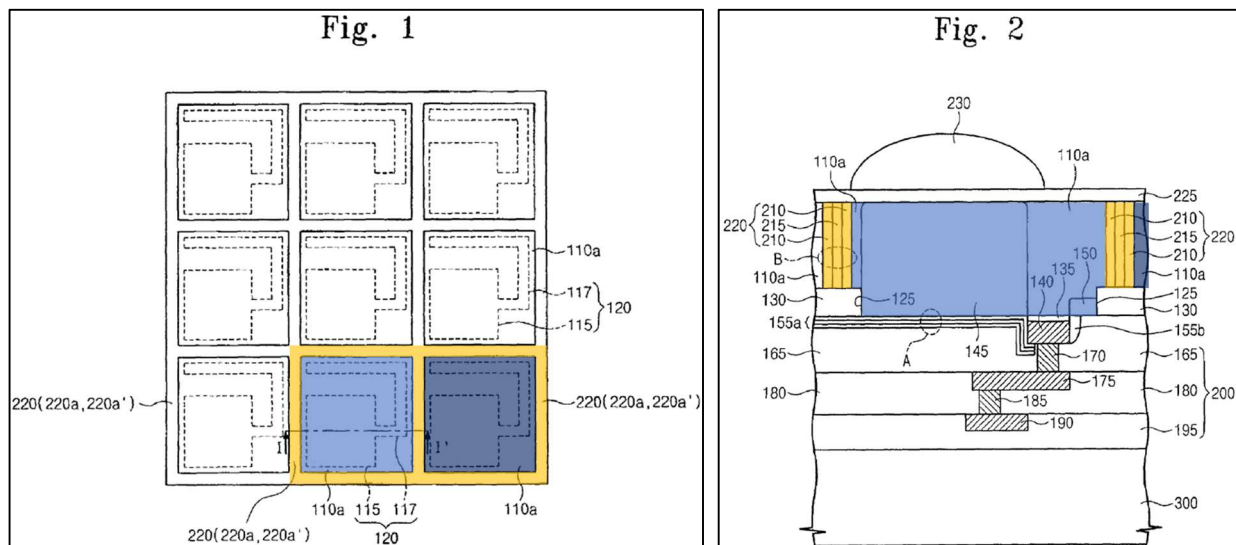
- b) **Element 1[a]: “at least two adjacent light sensitive image sensor pixels each having a light incident surface, and a backside surface opposite the light incident surface;”**

63. Hwang teaches or suggests this limitation.

64. Hwang’s image sensor comprises *at least two adjacent light sensitive image sensor pixels*, as shown in blue below (one pixel in light blue, the other in dark blue). In describing the embodiment shown in Figure 2, Hwang discloses “a plurality of pixel semiconductor patterns 110a” that are “arranged two-dimensionally in rows and columns.” Hwang, 5:52-54. Hwang discloses that “[e]ach pixel semiconductor pattern 110a has a photodiode 145 disposed therein.” Hwang, 5:57-58.⁴ As Hwang explains, “[a] photodiode is a representative type of light

⁴ All emphases in quotes have been added, unless otherwise stated.

receiver. When external light is incident on a depletion region in the photodiode, electron-hole pairs are generated, and the external light is converted to electrical signals.” Hwang, 1:23-29.

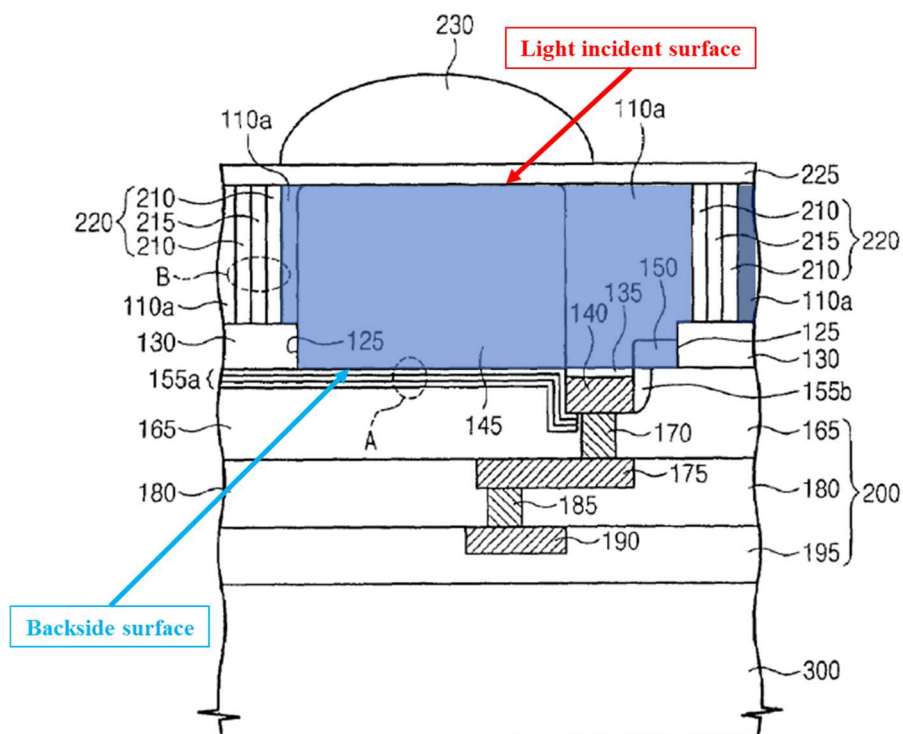


Hwang, Figs. 1-2 (annotated).

65. Hwang discloses that each light sensitive image sensor pixel has a light incident surface and a backside surface opposite the light incident surface. Hwang discloses that “[t]he pixel semiconductor patterns 110a have first and second surfaces in parallel, i.e., that face one another.” Hwang, 6:37-38. Hwang discloses that “[a] color filter 225 is disposed on the second surface of the pixel semiconductor pattern 110a, and a micro lens 230 that covers the photodiode 145 is disposed on the color filter 225. External light passes through the micro lens 230 and the color filter 225, and is incident on the second surface of the photodiode 145.” Hwang, 8:17-22. Thus, the “second surface” of the pixel semiconductor pattern 110a (shown below)

is a *light incident surface*. Hwang also discloses that “the first surface of a pixel semiconductor pattern 110a is more proximate to the substrate 300 than is the second surface.” Hwang, 6:38-40. “A device isolation pattern 130 that separates an active region 120 is disposed on the first surface of the pixel semiconductor pattern 110a.” Hwang, 6:40-43. “[T]he first surface of the photodiode 145 is coplanar with the first surface of the pixel substrate pattern 110a.” Hwang, 6:63-65. “The first surface of the floating doped region 150 shares the same surface with the first surface of the pixel semiconductor pattern 110a.” Hwang, 7:40-42. Thus, the “first surface” of the pixel semiconductor pattern 110a (shown below) is a *backside surface opposite the light incident surface*.

Fig. 2



Hwang, Fig. 2 (annotated).

66. “The pixel semiconductor patterns 110a have first and second surfaces in parallel, i.e., that face one another,” where “the first surface ... is more proximate to the substrate 300 than is the second surface.” Hwang, 6:37–40. Hwang’s “second surface” constitutes a *light incident surface*, see Hwang, 8:17–22 (“[e]xternal light ... is incident on the second surface of the photodiode 145.”), and its “first surface” constitutes a *backside surface opposite the light incident surface*.⁵

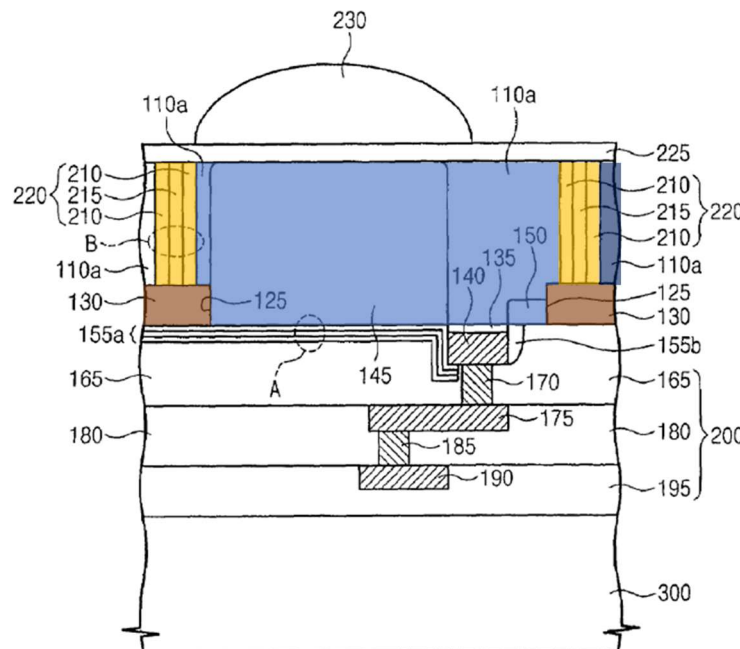
c) Element 1[b]: “a peripheral isolation element at least partially separating said two adjacent light sensitive pixels;”

67. Hwang teaches or suggests this limitation.

68. In describing the embodiment shown in Figure 2, Hwang discloses a *peripheral isolation element* comprising a “sidewall multi-layered reflection layer 220.” Hwang discloses that “[a] sidewall multi-layered reflection layer 220 is provided between the side walls of the pixel semiconductor patterns 110a.” Hwang,

⁵ Figures 2 and 6 use differently arranged sidewall multi-layered reflection layers but are otherwise the same. See Hwang, 11:57–60. Therefore, a POSITA would appreciate that Hwang’s disclosures for elements in Figure 6 (including layer 220a' comprising layers 212a' and 217a') are pertinent to corresponding elements in Figure 2 (including layer 220 comprising layers 210 and 215).

Fig. 2



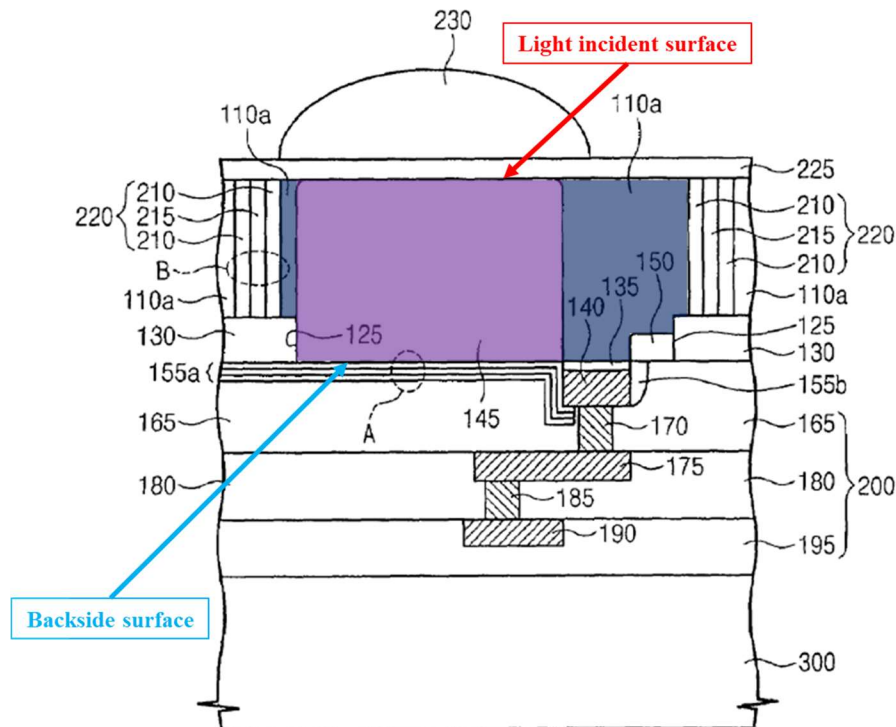
Hwang, Fig. 2 (annotated).

d) Element 1[c]: “each of said pixels having at least one doped region disposed on at least one of the light incident surface and the backside surface,”

69. Hwang teaches or suggests this limitation.

70. As discussed above regarding limitation 1[a], pixel semiconductor pattern 110a’s “second surface” corresponds to the *light incident surface* and its “first surface” corresponds to the *backside surface*. Hwang discloses that “[t]he pixel semiconductor patterns 110a are doped with a first conductive dopant” and that “[t]he photodiodes 145 are regions doped with a second conductive dopant.” Hwang, 5:58-60. Hwang further explains that “[t]he photodiode 145 also has a first surface and a second surface that face each other,” that “the first surface of the photodiode 145 is coplanar with the first surface of the pixel substrate pattern 110a,” and that, “[a]s shown in FIG. 2, the second surface of the photodiode 145 can share a common surface with the second surface of the pixel substrate pattern 110a.” Hwang, 6:61-67. Thus, doped region 110a (shown in dark blue below) and doped region 145 (shown in purple below) are *disposed on* both of the *light incident surface and the backside surface* (shown below).

Fig. 2



Hwang, Fig. 2 (annotated).

e) **Element 1[d]: “wherein the peripheral isolation element comprises at least two materials having different indices of refraction,”**

71. Hwang teaches or suggests this limitation.

72. Hwang discloses that layer 220 (*peripheral isolation element*) “includes a plurality of layers sequentially stacked at the side walls of the pixel semiconductor patterns 110a,” Hwang, 6:9-11: “a first sidewall reflection layer 210 and a second sidewall reflection layer 215.” Hwang, 9:58-60. Hwang discloses that “[t]he refractive index of the first sidewall reflection layer 210 is different from the refractive index[] of ... the second sidewall reflection layer 215,” Hwang, 9:60-63;

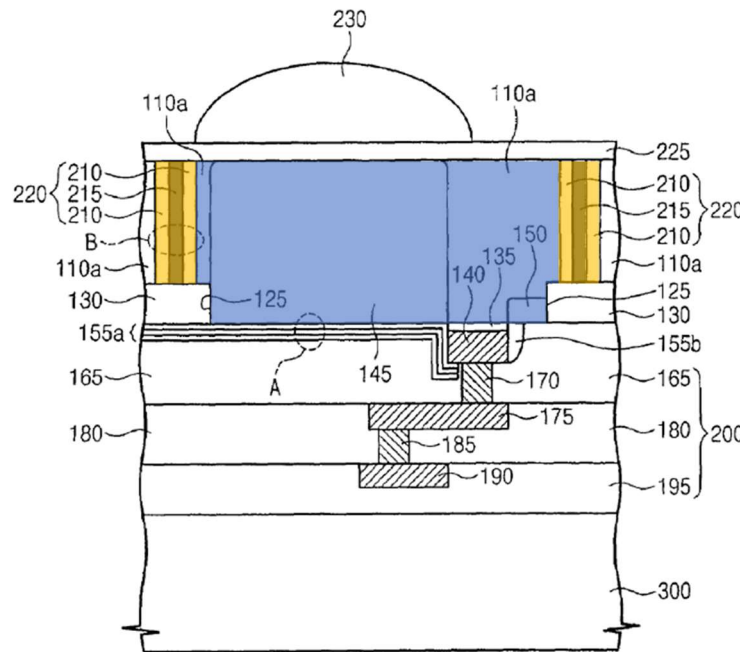
that “layer 210 can be a silicon oxide layer or a layer of air (with a refractive index of 1)” and that “layer 215 can be a silicon layer,” Hwang, 10:2-5; and that silicon oxide has “a refractive index of approximately 1.46” whereas silicon has “a refractive index of approximately 4,” Hwang, 9:28-30. Thus, layer 220 *comprises at least two materials having different indices of refraction.*

f) Element 1[e]: “wherein said peripheral isolation element comprises a first, a second and a third layer,”

73. Hwang teaches or suggests this limitation.

74. Hwang discloses that layer 220 (*peripheral isolation element*) “includes a structure in which the first and second sidewall reflection layers 210 and 215 are stacked in an alternating manner a plurality of times on the side wall of the pixel semiconductor pattern 110a.” Hwang, 10:6-10. Further, “the layers of the sidewall multi-layered reflection layer 220 contacting the pair of neighboring pixel semiconductor patterns 110a can be the first sidewall reflection layer 210” and “a second sidewall reflection layer 215 interposed between two first sidewall reflection layers 210.” Hwang, 10:14-17, 10:48-50. Thus, Hwang’s peripheral isolation element comprises three layers: element 210 left of element 215, shown in orange below (*first layer*), element 210 right of element 215, shown in orange below (*second layer*), and element 215, shown in brown below (*third layer*).

Fig. 2



Hwang, Fig. 2 (annotated).

g) Element 1[f]: “wherein said third layer is disposed between said first and second layers, and”

75. Hwang teaches or suggests this limitation.

76. As shown in Figure 2 above, element 215 (*third layer*) is disposed between element 210 on its left (*first layer*) and element 210 on its right (*second layer*). *See also* Hwang, 10:14-17, 10:48-50 (“second sidewall reflection layer 215 interposed between two first sidewall reflection layers 210”).

a) Element 1[g]: “wherein each of said first and second layer exhibits an index of refraction less than an index of refraction of said third layer.”

77. Hwang teaches or suggests this limitation.

78. Hwang discloses that the refractive index of the first sidewall reflection layer 210 (*first and second layers*) “can be lower than the refractive index[] of” the second sidewall reflection layer 215 (*third layer*). Hwang, 9:63-66.

3. Claim 2: “The device of claim 1, wherein the index of refraction of at least one of said first and second layer is at least 0.2 lower relative to the refractive index of the third layer.”

79. Hwang teaches or suggests this limitation.

80. As discussed above regarding limitation 1[e], Hwang discloses that the first sidewall reflection layer 210 (*first and second layers*) “can be a silicon oxide layer or a layer of air (with a refractive index of 1)” and that the second sidewall reflection layer 215 (*third layer*) “can be a silicon layer.” Hwang, 10:2-5. Hwang discloses that silicon oxide has “a refractive index of approximately 1.46” whereas silicon has “a refractive index of approximately 4.” Hwang, 9:28-30. Thus, *the index of refraction* of both of Hwang’s *first layer* and *second layer* (layers 210) is at least 0.2 lower than that of Hwang’s *third layer* (layer 215).

4. Claim 3: “The device of claim 1, wherein at least of one of said at least two materials comprises silicon dioxide.”

81. Hwang teaches or suggests this limitation.

82. As discussed above regarding limitations 1[d] and 1[e], Hwang discloses a “first sidewall reflection layer 210” corresponding to the *first layer* of the *peripheral isolation element*, Hwang, 9:58-60, and specifies that “layer 210 can be

a silicon oxide layer,” Hwang, 10:2-4; *see also* Hwang, 10:48-55 (“the first and second sidewall reflection layers 210 and 215 respectively formed of a silicon oxide layer and a silicon layer”).

83. A POSITA would understand that, in disclosing layer 210 formed of silicon oxide, Hwang uses the term “silicon oxide” to mean “silicon dioxide” (SiO_2) as opposed to “silicon monoxide” (SiO). A POSITA would know that the refractive index of silicon dioxide is around 1.4-1.5, whereas the refractive index of silicon monoxide is at least around 1.8-2.2. *See, e.g.*, Ex-1015, Appendix I at 852 (refractive index of “ SiO_2 ” is “1.46”); Ex-1016, Abstract (refractive index of “silicon monoxide” (“ SiO ”) ranges from 2.15 to 1.95 in the 0.40 to 0.70 micron wavelength range); Ex-1017 at 17 & Fig. 2 (refractive index of “silicon monoxide” ranges from about 1.8 to about 1.9 in the 1 to 5 micron wavelength range); Ex-1019 at 2-60 (refractive index of “ SiO_2 ” ranges from about 1.5 to 1.4 in the 0.40 to 0.70 micron wavelength range). Hwang specifies that its silicon oxide has “a refractive index of approximately 1.46,” confirming that it is using silicon dioxide as opposed to silicon monoxide. Hwang, 9:28-29. Consistent with this understanding, the ’359 patent itself uses the term “silicon oxide” to mean “silicon dioxide,” as it alternatively refers to the layers depicted in its Figure 2 as including “silicon dioxide” and “silicon oxide.” ’359 patent, 9:13-18 (“[A] Bragg reflector can be made as in FIG. 2, whereby a high refractive index material sandwiched between two low refractive index materials. In

one specific aspect, for example, the Bragg reflector can be constructed of a layer of polysilicon sandwiched between two layers of silicon dioxide."); '359 patent, 10:20-22 (“Returning to FIG. 2, layers [of] the silicon oxide and polysilicon...”). Thus, *at least one of the at least two materials* that comprise Hwang’s *peripheral isolation element* comprises *silicon dioxide*.

5. Claim 4: “The device of claim 1, wherein at least one of said first and second layers comprises silicon dioxide.”

84. Hwang teaches or suggests this limitation.

85. As discussed above regarding limitation 1[d], Hwang discloses that the “first sidewall reflection layer 210” (*first and second layers of the peripheral isolation element*) “can be a silicon oxide layer,” Hwang, 10:2-4, 10:48-55. As discussed above regarding claim 3, in describing layer 210, Hwang uses the term “silicon oxide” to mean “silicon dioxide” (SiO₂).

6. Claim 5: “The device of claim 1, wherein the isolation element extends substantially from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels.”

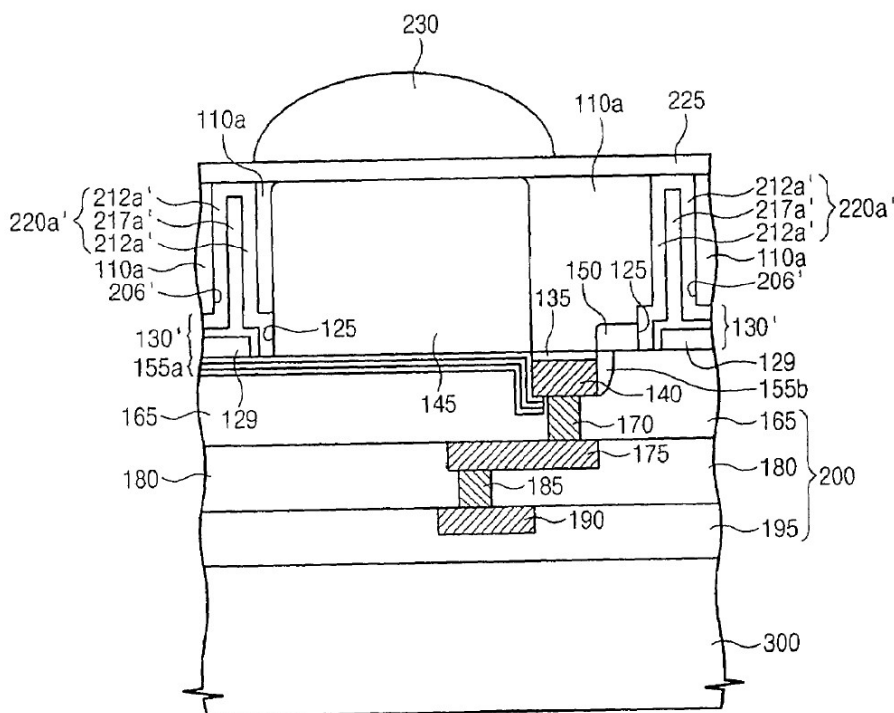
86. Hwang teaches or suggests this limitation.

87. As discussed above regarding limitation 1[b], Hwang discloses a peripheral isolation element comprising a “sidewall multi-layered reflection layer 220.” Hwang discloses that “[a] sidewall multi-layered reflection layer 220 [*isolation element*] is provided between the side walls of the pixel semiconductor patterns 110a.”

Hwang, 6:19-23. “As shown [in Figure 2], the sidewall multi-layered reflection layer 220 can contact the device isolation pattern 130.” Hwang, 10:61-62. That is, it extends *substantially from the light incident surface* (the “second surface” of pixel 110a) to isolation pattern 130 adjacent to the *backside surface* (the “first surface”) of the pixels.

88. To the extent there is any question whether the isolation element *extends substantially to the backside surface*, this element further would have been obvious. In Figure 6 below, Hwang discloses a modification of the Figure 2 embodiment in which a sidewall multi-layered reflection layer (element 220a' in Figure 6) extends fully *from the light incident surface to the backside surface*. “The sidewall multi-layered reflection layer 220a' includes a first sidewall reflection layer 212a' and a second sidewall reflection layer 217a' having different refractive indexes.” Hwang, 11:66-12:2. “The first and second sidewall reflection layers 212a' and 217a' can be extended into trench 125.” Hwang, 12:25-26.

Fig. 6



89. A POSITA would have been motivated to modify Hwang's sidewall multi-layered reflection layer 220 of Figure 2 to extend from the light incident surface to the backside surface, as suggested by Figure 6, to increase "absorption efficiency of external light" and decrease "interference between neighboring pixels." *See* Hwang, 10:28-40. A POSITA would have known that a gap in sidewall reflection between the light incident surface and the backside surface can allow electrons to escape under the sidewall trench into a neighboring pixel. *See, e.g.,* Roy, [0039] ("Usually, trench 11 has a depth ranging between 0.3 and 0.7 μm . Thereby, this trench limits the crosstalk without however completely canceling it since electron/hole pairs may be photogenerated down to a depth from 3 to 10 μm Electrons can thus pass under trench 11 from the N area of a photodiode to the N area of a neighboring photodiode."). A POSITA would consider the full extension of Hwang's sidewall multi-layered reflection layer 220 to be a known technique to improve a similar device in the same way. Additionally, a POSITA would have considered a trench extending from the light incident surface to the backside surface, instead of creating separate trenches 205 and 125, as in Figure 2, to be a simplification of manufacturing steps. *See, e.g.,* Roy, [0079].

90. Accordingly, it would have been obvious to a POSITA to modify Hwang's sidewall multi-layered reflection layer 220 *wherein it extends substantially from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels.*

7. Claim 7: “The device of claim 1, wherein said peripheral isolation element comprises an oxide.”

91. Hwang teaches or suggests this limitation.

92. As discussed above regarding limitation 1[d], Hwang discloses that “[t]he first sidewall reflection layer 210” (*first and second layers of the peripheral isolation element*) “can be a silicon oxide layer.” Hwang, 10:2-4; Hwang, 10:48-55.

8. Claim 10: “The device of claim 1, wherein the peripheral isolation element comprises at least one material having an index of refraction of less than about 2.1.”

93. Hwang teaches or suggests this limitation.

94. As discussed above regarding claim 2, Hwang discloses that “[t]he first sidewall reflection layer 210” (*first and second layers of the peripheral isolation element*) “can be a silicon oxide layer,” Hwang, 10:2-4, and that silicon oxide has “a refractive index of approximately 1.46,” Hwang, 9:28-29. Thus, Hwang’s *peripheral isolation element comprises at least one material having an index of refraction of less than about 2.1*.

9. Claim 18

a) Element 18[pre]: “An imager device, comprising:”

95. Hwang teaches or suggests this preamble.

96. See discussion of claim 1[pre].

- b) **Element 18[a]: “at least two adjacent light sensitive image sensor pixels each having a light incident surface, and a backside surface opposite the light incident surface;”**

97. Hwang teaches or suggests this limitation.

98. See discussion of limitation 1[a].

- c) **Element 18[b]: “a peripheral isolation element separating said at least two adjacent light sensitive pixels so as to reduce optical crosstalk therebetween,”**

99. Hwang teaches or suggests this limitation.

100. As discussed above regarding limitation 1[b], Hwang discloses a *peripheral isolation element*—sidewall multi-layered reflection layer 220—*separating at least two adjacent light sensitive pixels*.

101. Hwang discloses that layer 220 serves to reduce optical crosstalk between adjacent light sensitive pixels. Hwang discloses that layer 220 “is interposed between a pair of neighboring pixel semiconductor patterns 110a” so that “the occurrence of interference between neighboring pixels can be minimized.” Hwang, 10:10-18. Hwang discloses that this layer 220 serves to *reduce optical crosstalk* between the *adjacent ... pixels*, as it “minimizes incidence of the light (reflected by the base multi-layered reflection layer 155a at the first and second boundary surfaces) on the photodiode 145 within another pixel semiconductor pattern 110a. In other words, ... layer 220 minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels.” Hwang, 10:19-

26. As a result, “interference of the image sensor can be minimized, and image distortion can be minimized.” Hwang, 10:26-27; *see also* Hwang, 10:28-40, 15:42-48.

d) Element 18[c]: “said isolation element comprising at least two materials having different indices of refraction,”

102. Hwang teaches or suggests this limitation.

103. See discussion of limitation 1[d].

e) Element 18[d]: “at least one doped region disposed on at least one of the light incident surface and the backside surface,”

104. Hwang teaches or suggests this limitation.

105. See discussion of limitation 1[c].

f) Element 18[e]: “wherein said peripheral isolation element comprises a first, a second and a third layer,”

106. Hwang teaches or suggests this limitation.

107. See discussion of limitation 1[e].

g) Element 18[f]: “wherein said third layer is disposed between said first and second layers, and”

108. Hwang teaches or suggests this limitation.

109. See discussion of limitation 1[f].

h) Element 18[g]: “wherein each of said first and second layers exhibits an index of refraction less than an index of refraction of said third layer.”

110. Hwang teaches or suggests this limitation.

111. See discussion of limitation 1[g].

10. Claim 23: “The device of claim 18, wherein the peripheral isolation element extends from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels.”

112. Hwang teaches or suggests this limitation.

113. See discussion of claim 5, explaining that it would have been obvious to modify the image sensor of Hwang Figure 2 so that the isolation element extends fully *from the light incident surface to the backside surface*.

11. Claim 25: “The device of claim 19, wherein said at least two pixels are formed monolithically in a common semiconductor substrate.”

114. Hwang teaches or suggests this limitation.

115. The '359 patent specifies: “As used herein, the term ‘monolithic’ refers to an electronic device in which electronic components are formed on the same substrate. For example, two monolithic pixel elements are pixel elements that are formed on the same semiconductor substrate.” ’359 patent, 5:19-23.

116. Hwang discloses forming its plurality of pixel semiconductor patterns 110a (pixels) *in a common semiconductor substrate*—i.e., by selectively etching a single semiconductor layer 110. *See* Hwang, 3:60-63 (“forming a plurality of grooves for defining the pixel semiconductor pattern through selectively etching the semiconductor layer”); *see also* Hwang, 4:5-7, 12:42-48, 13:29-35. Hwang discloses subsequently forming its photodiodes 145 in the same semiconductor layer. *See*

Hwang, 3:29-30 (“forming a photodiode in a semiconductor layer included in a first substrate”); *see also* Hwang, 1:63-64, 2:66, 5:52-55, 16:13 (“a photodiode in the pixel semiconductor pattern”). Thus, Hwang teaches *form[ing] its pixels monolithically in a common semiconductor substrate*.

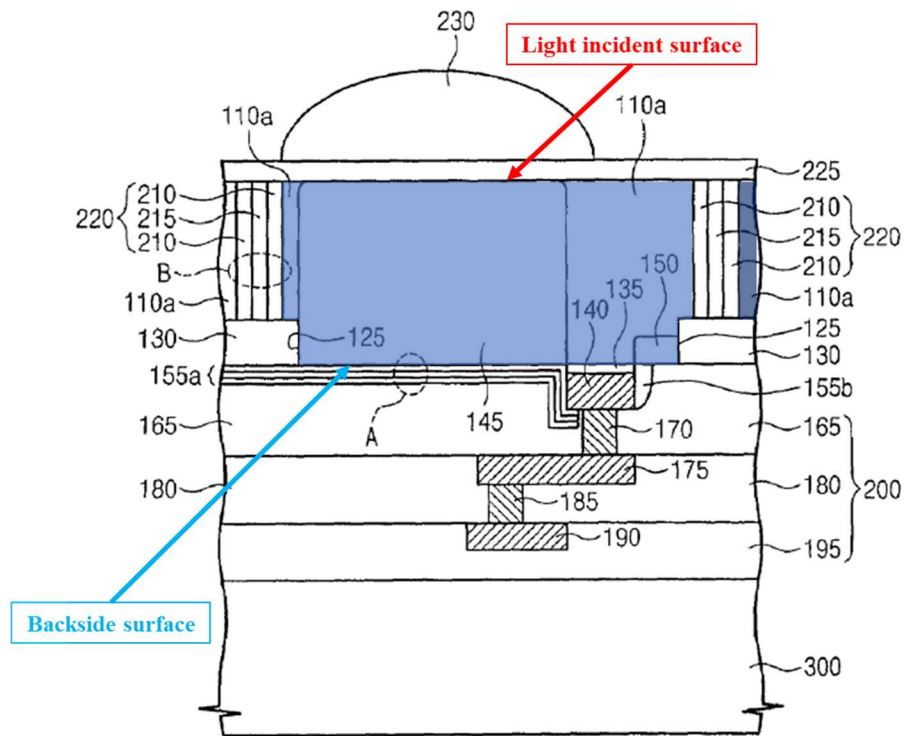
- 12. Claim 38: “The device of claim 1, wherein each of said at least two adjacent light sensitive image sensor pixels comprises a semiconductor portion providing said light incident surface and said backside surface, wherein said peripheral isolation element isolates the semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”**

117. Hwang teaches or suggests this limitation.

118. First, each of Hwang’s *light sensitive image sensor pixels* comprises a *semiconductor portion* providing the *light incident surface* and the *backside surface*: pixel semiconductor pattern 110a. Hwang discloses that “[t]he pixel semiconductor patterns 110a are formed as a semiconductor” and “can be formed of silicon.” Hwang, 5:52-55.

119. Second, as discussed above regarding limitation 1[a], (i) the *light incident surface* is the pixel semiconductor pattern 110a’s “second surface” (shown below), and (ii) the *backside surface* is its “first surface” (shown below).

Fig. 2



Hwang, Fig. 2 (annotated).

120. Third, Hwang discloses that its sidewall multi-layered reflection layer 220 (*peripheral isolation element*) separates and optically *isolates* pixel semiconductor patterns 110a. Hwang discloses that layer 220 “is interposed between a pair of neighboring pixel semiconductor patterns 110a” so that “the occurrence of interference between neighboring pixels can be minimized.” Hwang, 10:10-18; *see also* Hwang, 6:21-23 (“[A]ll of the pixel semiconductor patterns 110a can thus be separated by the sidewall multi-layered reflection layer 220.”). Hwang discloses that layer 220 “minimizes incidence of the light (reflected by the base multi-layered reflection layer 155a at the first and second boundary surfaces) on the photodiode

145 within another pixel semiconductor pattern 110a. In other words, ... layer 220 minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels.” Hwang, 10:19-26. As a result, “interference of the image sensor can be minimized, and image distortion can be minimized.” Hwang, 10:26-27; *see also* Hwang, 10:19-40, 15:42-48.

13. Claim 39: “The device of claim 38, wherein said peripheral isolation element optically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”

121. Hwang teaches or suggests this limitation.

122. As discussed above regarding claim 38, sidewall multi-layered reflection layer 220 (*peripheral isolation element*) *optically isolates* pixel semiconductor patterns 110a (*semiconductor portions* of adjacent pixels).

14. Claim 40: “The device of claim 38, wherein said peripheral isolation element electrically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”

123. Hwang teaches or suggests this limitation.

124. As discussed above regarding claim 5, a POSITA would have been motivated to modify Hwang’s sidewall multi-layered reflection layer 220 of Figure 2 (*peripheral isolation element*) to extend from the light incident surface to the backside surface, as suggested by Figure 6, to increase “absorption efficiency of external light” and decrease “interference between neighboring pixels.” *See* Hwang, 10:28-40. A

POSITA would have known that a gap in sidewall reflection between the light incident surface and the backside surface can allow electrons to escape under the sidewall trench into a neighboring pixel. *See, e.g.*, Roy, [0039] (“Usually, trench 11 has a depth ranging between 0.3 and 0.7 μm . Thereby, this trench limits the crosstalk without however completely canceling it since electron/hole pairs may be photogenerated down to a depth from 3 to 10 μm Electrons can thus pass under trench 11 from the N area of a photodiode to the N area of a neighboring photodiode.”); Shinohara, [0064] (because “adjacent pixels are physically isolated from each other ... the leakage of charge in the photodiode PD into an adjacent pixel can be substantially prevented”). A POSITA would consider the full extension of Hwang’s sidewall multi-layered reflection layer 220 to be a known technique to *electrically isolate adjacent pixels* to improve a similar device in the same way. Additionally, a POSITA would have considered a trench extending from the light incident surface to the backside surface, instead of creating separate trenches 205 and 125, as in Figure 2, to be a simplification of manufacturing steps. *See, e.g.*, Roy, [0079].

125. Accordingly, it would have been obvious for a POSITA to modify Hwang make an imager device *wherein said peripheral isolation element electrically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels*.

15. **Claim 41: “The device of claim 38, wherein an index of refraction of the semiconductor portion of each of said at least two adjacent image sensor pixels is different from indices of refraction of said layers of the peripheral isolation element such that light incident from each of said semiconductor portions on said peripheral isolation element is reflected, thereby providing optical isolation between the pixels.”**

126. Hwang teaches or suggests this limitation.

127. As discussed above regarding claim 5, Hwang discloses a modification of the Figure 2 embodiment in which the sidewall multi-layered reflection layer 220 extends from the light incident surface to the backside surface, as shown for example in Hwang Figure 6. “The sidewall multi-layered reflection layer 220a' includes a first sidewall reflection layer 212a' and a second sidewall reflection layer 217a' having different refractive indexes.” Hwang, 11:66-12:2. In the Figure 6 approach, “[t]he second sidewall reflection layer 217a' is disposed within the groove 206 and on the first sidewall reflection layer 212a'.” Hwang, 11:33-35. A POSITA would understand that layer 217a' is formed of polysilicon. *See also* Hwang, 14:58-4. Silicon dioxide has “a refractive index of approximately 1.46” whereas the silicon of semiconductor portion 110a has “a refractive index of approximately 4,” Hwang, 9:28-30. A POSITA would know that polysilicon has a refractive index different from the semiconductor portion 110a. *See* Ex-1023, Fig. 19 (noting an index of refraction greater than 4 the middle of the visible spectrum). In this case, the *index of refraction*

of the image sensor pixels (silicon) *is different from indices of refraction* of all the *layers of the peripheral isolation element* (silicon dioxide and polysilicon).

128. As discussed above regarding limitation 18[b], Hwang's peripheral isolation element optically isolates the adjacent light sensitive image sensor pixels. Hwang specifies that the peripheral isolation element achieves such isolation by reflecting light incident on it from the semiconductor portions of the adjacent pixels it separates. *See* Hwang, 10:19-40 (describing how light reflected from the surfaces of the adjacent pixel semiconductor patterns 110a is "also reflected" by the sidewall multi-layered reflection layer 220 back "on the photodiode 145," achieving optical isolation by minimizing "incidence of light reflected by the ... surfaces on neighboring pixels").

129. Accordingly, a POSITA would find it obvious to follow Hwang's teachings to construct an imager device wherein *an index of refraction of the semiconductor portion of each of at least two adjacent image sensor pixels* (approximately 4 for pixel semiconductor pattern 110a) *is different from indices of refraction of the layers of the peripheral isolation element* (approximately 1.46 for silicon dioxide and greater than 4 for polysilicon) *such that light incident from each of said semiconductor portions on said peripheral isolation element is reflected, thereby providing optical isolation between the pixels.*

- 16. Claim 42: “The device of claim 1, wherein said at least two adjacent light sensitive image sensor pixels are formed monolithically on a common semiconductor substrate and are isolated from one another by said peripheral isolation element.”**

130. Hwang teaches or suggests this limitation.

131. As discussed above regarding claim 25, Hwang discloses that its *adjacent light sensitive image sensor pixels are formed monolithically on a common semiconductor substrate*.

132. As discussed above regarding limitation 1[b], Hwang discloses that its *adjacent light sensitive image sensor pixels are isolated from one another* by its sidewall multi-layered reflection layer 220 (*peripheral isolation element*).

- 17. Claim 43: “The device of claim 1, wherein said peripheral isolation element is a trench isolation element.”**

133. Hwang teaches or suggests this limitation.

134. Hwang discloses that its sidewall multi-layered reflection layer 220 (*peripheral isolation element*) is formed by “etch[ing] a plurality of grooves 205” in “semiconductor layer 110” and then “fill[ing] the grooves with a predetermined material.” Hwang, 12:42-45, 12:50-51; *see* Hwang, 12:42-13:3. Accordingly, a POSITA would understand that Hwang’s *peripheral isolation element* layer 220 is a “trench” element—i.e., formed by etching and filing trenches.

18. Claim 45: “The device of claim 18, wherein each of said at least two adjacent light sensitive image sensor pixels comprises a semiconductor portion providing said light incident surface and said backside surface, wherein said peripheral isolation element isolates the semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”

135. Hwang teaches or suggests this limitation.

136. See discussion of claim 38.

19. Claim 46: “The device of claim 45, wherein said peripheral isolation element optically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”

137. Hwang teaches or suggests this limitation.

138. See discussion of claim 39.

20. Claim 47: “The device of claim 46, wherein said peripheral isolation element electrically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”

139. Hwang teaches or suggests this limitation.

140. See discussion of claim 40.

21. Claim 48: “The device of claim 47, wherein an index of refraction of the semiconductor portion of each of said at least two adjacent image sensor pixels is different from indices of refraction of said layers of the peripheral isolation element such that light incident from each of said semiconductor portions on said peripheral isolation element is reflected, thereby providing optical isolation between the pixels.”

141. Hwang teaches or suggests this limitation.

142. See discussion of claim 41.

22. Claim 49: “The device of claim 18, wherein said at least two adjacent light sensitive image sensor pixels are formed monolithically on a common semiconductor substrate and are isolated from one another by said peripheral isolation element.”

143. Hwang teaches or suggests this limitation.

144. See discussion of claim 42.

23. Claim 50: “The device of claim 18, wherein said peripheral isolation element is a trench isolation element.”

145. Hwang teaches or suggests this limitation.

146. See discussion of claim 43.

24. Claim 52: “The imager device of claim 38, wherein at least one of the first layer and the second layer of said peripheral isolation element and said semiconductor portion of each of said at least two adjacent pixels comprise different materials.”

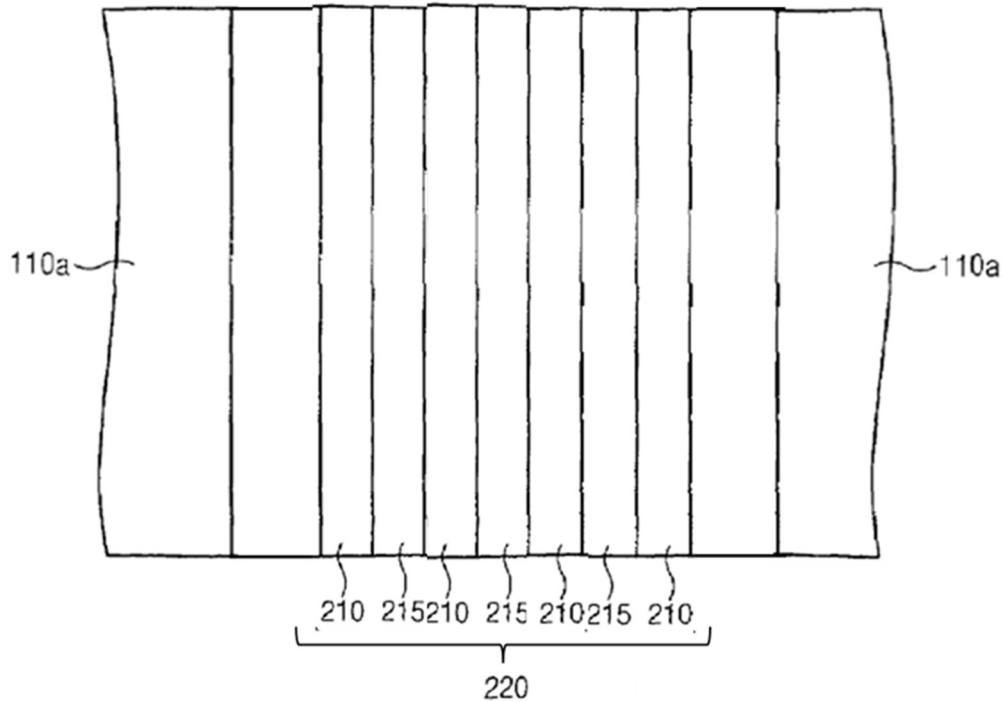
147. Hwang teaches or suggests this limitation.

148. Hwang discloses that its first sidewall reflection layer 210 (*first and second layers of the peripheral isolation element*) “can be a silicon oxide layer,” Hwang, 10:2-4, and that “the pixel semiconductor patterns 110a can be formed of silicon.” Hwang, 5:52-55. Thus, *at least one of the first layer and the second layer of Hwang’s peripheral isolation element (layer 220) and the semiconductor portion of each of the adjacent pixels (pixel semiconductor patterns 110a) comprise different materials.*

25. Claim 53: “The imager device of claim 1, wherein the first layer and the second layer of said peripheral isolation element comprise different materials.”

149. Hwang teaches or suggests this limitation.

150. Hwang discloses that its sidewall multi-layered reflection layer 220 (*peripheral isolation element*) “includes a structure in which the first and second sidewall reflection layers 210 and 215 are stacked in an alternating manner a plurality of times.” Hwang, 10:6-10; *see also* Hwang, 2:16-19, 4:12-15, 10:6-10, Fig. 4. Hwang further discloses that “[t]he number of layers of the sidewall multi-layered reflection layer 220 ... varies according to the number of the grooves 205. ... As shown [for example, in Figure 2], when two ... grooves 205 are formed, the sidewall multi-layered reflection layer 220 has three layers. Alternately, when three ... grooves 205 are formed to enclose one pixel semiconductor pattern 110a, the number of layers of the sidewall multi-layered reflection layer 220 is five.” Hwang, 12:62-13:3. Accordingly, Hwang’s sidewall multi-layered reflection layer 220 can be constructed of seven layers, beginning with layer 210 at the outside and alternating between material layers 210 and 215.



Hwang, Fig. 4 (modified).

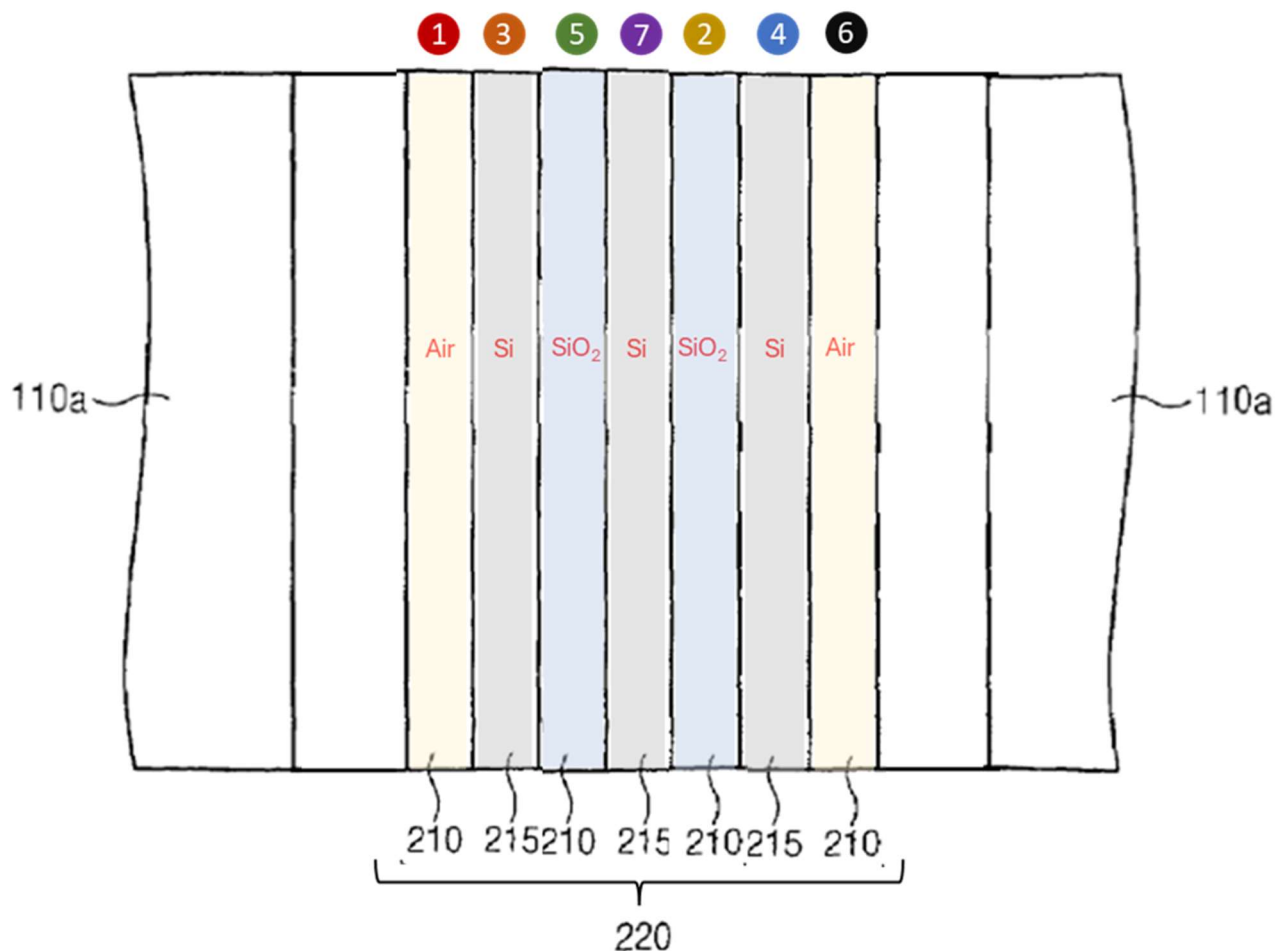
151. Hwang also teaches that “[t]he first sidewall reflection layer 210 can be a silicon oxide layer or a layer of air (with a refractive index of 1).” Hwang, 10:2-4. In constructing a seven-layer Hwang sidewall multi-layered reflection layer, a POSITA would find it obvious to apply Hwang’s teachings to use both silicon oxide and air as layers 210, such that the final construct would be 210 (air) - 215 (silicon) - 210 (silicon dioxide) - 215 (silicon) - 210 (silicon dioxide) - 215 (silicon) - 210 (air). The indices of refraction of such a construct would aid in the reflectivity of the sidewall multi-layered reflection layer, consistent with Hwang’s teachings that “the sidewall multi-layered reflection layer 220 include layers with different respective refractive indexes,” Hwang, 6:11-13, and that as a result of these differences, “the rate at which the external

light is absorbed by the photodiode 145 in increased to increase the light sensitivity of the image sensor,” Hwang, 9:11-14. Also, a POSITA would know that placing an air layer at the outermost layer would result in lower surface recombination velocity. *See generally* Ex-1022. By using the known techniques, a POSITA would improve the base Figure 2 embodiment.

152. Numbering the layers of this sidewall multi-layered reflection layer as 210 (air; first) - 215 (silicon; third) - 210 (silicon dioxide; fifth) - 215 (silicon; seventh) - 210 (silicon dioxide; second) - 215 (silicon; fourth) - 210 (air; sixth) would still meet all the limitations of claim 1. Layer numbering has no impact on limitations 1[a]-1[d]. Limitation 1[e] is met because the seven-layer sidewall multi-layered reflection layer comprises a first, second, and third layer. Limitation 1[f] is met because the third layer is disposed between the first and second layers.⁶ Limitation 1[g] is met because the

⁶ In the Related Proceeding, Patent Owner proposed to construe *said third layer is disposed between said first and second layers* to mean “a third layer between the first and second layers, wherein the first and second layers can be different materials from one another,” while Petitioner proposed that the third layer is in contact with the first and second layers on opposing sides. Ex-1011; Ex-1012. For purposes of this petition, Petitioner adopts Patent Owner’s construction, which is met by Hwang’s seven-layer sidewall multi-layered reflection layer, as explained in the main text.

refractive indices of the first layer (air, approximately 1) and second layer (silicon dioxide, approximately 1.46) are both less than the refractive index of the third layer (silicon, approximately 4).



Hwang, Fig. 4 (annotated and modified).

153. The *first layer* (air) and the *second layer* (silicon dioxide) of Hwang's seven-layer sidewall multi-layered reflection layer *comprise different materials*.

26. Claim 54: "The imager device of claim 1, wherein the peripheral isolation element comprises at least three materials."

154. Hwang teaches or suggests this limitation.

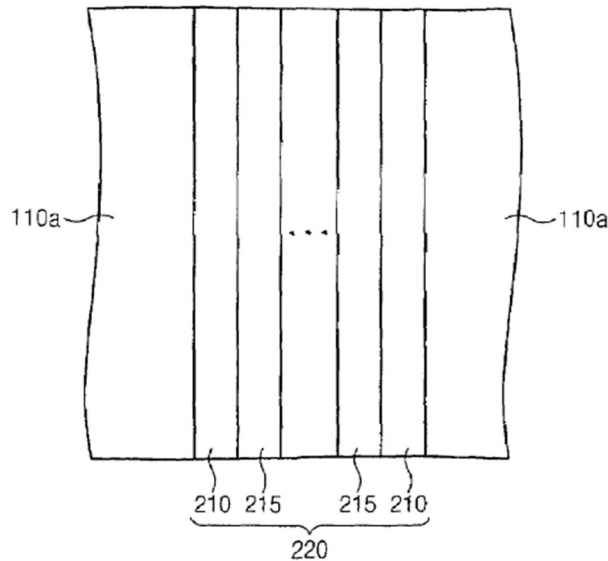
155. See discussion of claim 53 regarding a seven-layer construct according to the teachings of Hwang. In the seven-layer construct of Hwang's sidewall multi-layered reflection layer, the layers are 210 (air) - 215 (silicon) - 210 (silicon dioxide) - 215 (silicon) - 210 (silicon dioxide) - 215 (silicon) - 210 (air). In such a construct of Hwang's sidewall multi-layered reflection layer, *at least three materials* are provided.

27. Claim 55: “The imager device of claim 1, wherein the peripheral isolation element comprises more than three layers.”

156. Hwang teaches or suggests this limitation.

157. Hwang discloses that its sidewall multi-layered reflection layer 220 (*peripheral isolation element*) “includes a structure in which the first and second sidewall reflection layers 210 and 215 are stacked in an alternating manner a plurality of times on the side wall of the pixel semiconductor pattern 110a.” Hwang, 10:6-10; *see also* Hwang, 2:16-19, 4:12-15, 10:6-10; Hwang, Fig. 4 (below). Hwang further discloses that “[t]he number of layers of the sidewall multi-layered reflection layer 220 ... varies according to the number of the grooves 205. ... [W]hen three ... grooves 205 are formed to enclose one pixel semiconductor pattern 110a, the number of layers of the sidewall multi-layered reflection layer 220 is five.” Hwang, 12:62-13:3.

Fig. 4



Hwang, Fig. 4; Hwang, 5:1-4, 9:35-40, 10:6-10. Thus, Hwang discloses a *peripheral isolation element* layer 220 that *comprises more than three layers*.

28. Claim 56: “The imager device of claim 1, wherein the peripheral isolation element comprises a light trapping material filling a trench.”

158. Hwang teaches or suggests this limitation.

159. Hwang discloses forming its sidewall multi-layered reflection layer 220 (*peripheral isolation element*) by filling trenches with material. Hwang discloses forming layer 220 by selectively etching grooves 205 surrounding pixel semiconductor patterns 110a and then filling those grooves with a predetermined material. Hwang, 12:42-61. Accordingly, each layer 210 of Hwang’s multi-layered reflection layer 220 consists of material *filling a trench* (groove 205).

160. Hwang discloses that the material filling layer 210 traps light within each pixel. Hwang discloses that its multi-layered reflection layer 220 is interposed between adjacent pixels and that its layers contacting the pair of pixels “can be the first sidewall reflection layer 210.” Hwang, 10:10-17. Hwang discloses that layer 220 reflects light incident on it from the photodiode 145 that it encloses back onto that same photodiode, minimizing incidence of such light “on other pixels.” Hwang, 10:19-40; *see also* Hwang, 8:61-9:14 (external light incident on photodiode 145 is “reflected at a high rate” from the “base multi-layered reflection layer 155a”). Thus, layer 220 traps light within the pixel it encloses.

29. Claim 57: “The imager device of claim 56, wherein the trench is one of a shallow trench and a deep trench.”

161. Hwang teaches or suggests this limitation.

162. As discussed above regarding claim 56 and shown in Figure 13, Hwang discloses forming each groove 205 (*trench*) by selectively etching the semiconductor layer 110. Hwang, 12:42-45, Fig. 13.

163. The '359 patent states that, “[f]or simplicity, the figures in this disclosure show deep trench isolation but it should be understood that shallow trench isolation architectures can be utilized, and that deep trench isolation need not completely extend from one side to the other.” '359 patent, 7:56-60. Accordingly, as discussed above regarding claim 5, Hwang teaches *a deep trench* that extends substantially from the light incident surface to the backside surface.

- 30. Claim 58: “The imager device of claim 45, wherein at least one of the first layer and the second layer of the peripheral isolation element and said semiconductor portion of each of said at least two adjacent pixels comprise different materials.”**

164. Hwang teaches or suggests this limitation.

165. See discussion of claim 52.

- 31. Claim 59: “The imager device of claim 18, wherein the first layer and the second layer of said peripheral isolation element comprise different materials.”**

166. Hwang teaches or suggests this limitation.

167. See discussion of claim 53.

- 32. Claim 60: “The imager device of claim 18, wherein the peripheral isolation element comprises at least three materials.”**

168. Hwang teaches or suggests this limitation.

169. See discussion of claim 54.

- 33. Claim 61: “The imager device of claim 18, wherein the peripheral isolation element comprises more than three layers.”**

170. Hwang teaches or suggests this limitation.

171. See discussion of claim 55.

- 34. Claim 62: “The imager device of claim 18, wherein the peripheral isolation element comprises a light trapping material filling a trench.”**

172. Hwang teaches or suggests this limitation.

173. See discussion of claim 56.

35. Claim 63: “The imager device of claim 62, wherein the trench is one of a shallow trench and a deep trench.”

174. Hwang teaches or suggests this limitation.

175. See discussion of claim 57.

36. Claim 64: “The imager device of claim 1, wherein said peripheral isolation element comprises a trench isolation element formed by filling a trench with said first, said second, and said third layers.”

176. Hwang teaches or suggests this limitation.

177. As discussed above regarding claim 56, Hwang discloses a peripheral isolation element comprising a light trapping material filling a trench. “[T]he layers of the sidewall multi-layered reflection layer 220 contacting the pair of neighboring pixel semiconductor patterns 110a can be the first sidewall reflection layer 210” and “a second sidewall reflection layer 215 interposed between two first sidewall reflection layers 210.” Hwang, 10:14-17, 10:48-50. Sidewall multi-layered reflection layer 220 is trench-based isolation element because “[a] sidewall multi-layered reflection layer 220 is formed on the sidewall of the pixel semiconductor pattern 110a” by “selectively etch[ing] to form a plurality of grooves 205 surrounding the pixel semiconductor patterns 110a.” Hwang, 12:51-53, 12:43-45. “[T]he grooves 205 are filled with a predetermined material.” Hwang, 12:50-51. The result, as depicted in Hwang Figure

2, is a trench isolation element with *first* (element 210), *second* (element 210), and *third* (element 215) *layers* filling a trench.⁷

37. Claim 67: “The imager device of claim 1, wherein said peripheral isolation element is configured to reflect at least a portion of light incident thereon from any of said two adjacent light sensitive pixels back to that pixel.”

178. Hwang teaches or suggests this limitation.

179. As discussed above regarding claim 38, Hwang discloses that its sidewall multi-layered reflection layer 220 (*peripheral isolation element*) reflects light incident on it from the photodiode 145 that it encloses back onto that same photodiode, such that *at least a portion of light incident* on the pixel’s layer 220 is *reflect[ed] back to that pixel*. To achieve this result, Hwang discloses configuring layer 220 by alternately stacking “first and second sidewall reflection layers 210 and 215,” Hwang, 10:6-10, adjusting the thicknesses of layers 210 and 215, Hwang, 10:41-55, and positioning layer 220 “between a pair of neighboring pixel semiconductor patterns 110a,” Hwang, 10:11-12. Hwang discloses that layer 220

⁷ To the extent the Board finds that grooves 205 separated by layer 215 do not constitute a trench, it would have been obvious to a POSITA to try “an alternate embodiment of a method of forming an image sensor according to aspects of the present invention,” Hwang, 13:26-28, by which a single groove 206 is etched and filled to form three layers. *See* Hwang, 13:31-49, Fig. 15.

“minimizes incidence of the light (reflected by the base multi-layered reflection layer 155a at the first and second boundary surfaces) on the photodiode 145 within another pixel semiconductor pattern 110a. In other words, ... layer 220 minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels.”

Hwang, 10:19-26.

38. Claim 68: “The imager device of claim 67, wherein the peripheral isolation element is further configured to optically isolate said two adjacent light sensitive pixels.”

180. Hwang teaches or suggests this limitation.

181. See discussion of claim 39.

39. Claim 69: “The imager device of claim 68, wherein the peripheral isolation element is further configured to electrically isolate said two adjacent light sensitive pixels.”

182. Hwang teaches or suggests this limitation.

183. See discussion of claim 40.

40. Claim 70: “The imager device of claim 18, wherein said peripheral isolation element comprises a trench isolation element formed by filling a trench with said first, said second, and said third layers.”

184. Hwang teaches or suggests this limitation.

185. See discussion of claim 64.

41. Claim 73: “The imager device of claim 18, wherein said peripheral isolation element is configured to reflect at least a portion of light incident thereon from any of said two adjacent light sensitive pixels back to that pixel.”

186. Hwang teaches or suggests this limitation.

187. See discussion of claim 67.

42. Claim 74: “The imager device of claim 73, wherein the peripheral isolation element is further configured to optically isolate said two adjacent light sensitive pixels.”

188. Hwang teaches or suggests this limitation.

189. See discussion of claim 39.

43. Claim 75: “The imager device of claim 74, wherein the peripheral isolation element is further configured to electrically isolate said two adjacent light sensitive pixels.”

190. Hwang teaches or suggests this limitation.

191. See discussion of claim 40.

44. Claim 80: “The imager device of claim 1, wherein the peripheral isolation element comprises five layers.”

192. Hwang teaches or suggests this limitation.

193. See discussion of claim 55.

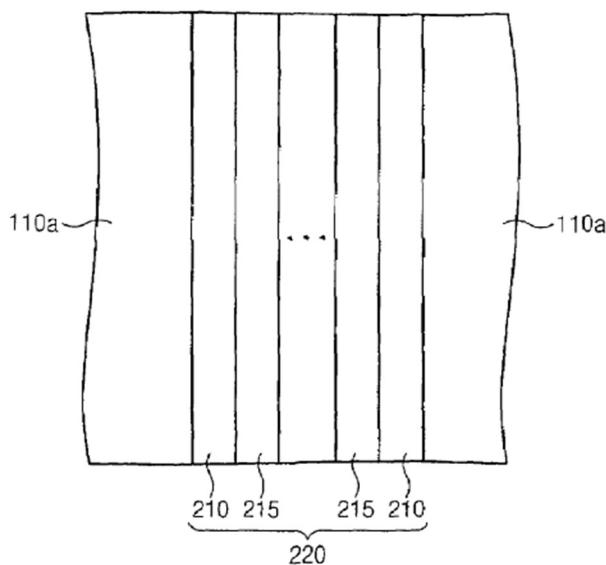
45. Claim 81: “The imager device of claim 80, wherein the five layers include the first layer, the second layer, the third layer, a fourth layer disposed between the first layer and one of said adjacent pixels and a fifth layer disposed between the second layer and the other one of said adjacent pixels.”

194. Hwang teaches or suggests this limitation.

195. Hwang discloses that its sidewall multi-layered reflection layer 220 (*peripheral isolation element*) “includes a structure in which the first and second sidewall reflection layers 210 and 215 are stacked in an alternating manner a plurality of times.” Hwang, 10:6-10; *see also* Hwang, 2:16-19, 4:12-15, 10:6-10;

Hwang, Fig. 4 (below). Hwang further discloses that “[t]he number of layers of the sidewall multi-layered reflection layer 220 ... varies according to the number of the grooves 205. ... As shown [for example, in Figure 2], when two ... grooves 205 are formed, the sidewall multi-layered reflection layer 220 has three layers. Alternately, when three ... grooves 205 are formed to enclose one pixel semiconductor pattern 110a, the number of layers of the sidewall multi-layered reflection layer 220 is five.”
Hwang, 12:62-13:3.

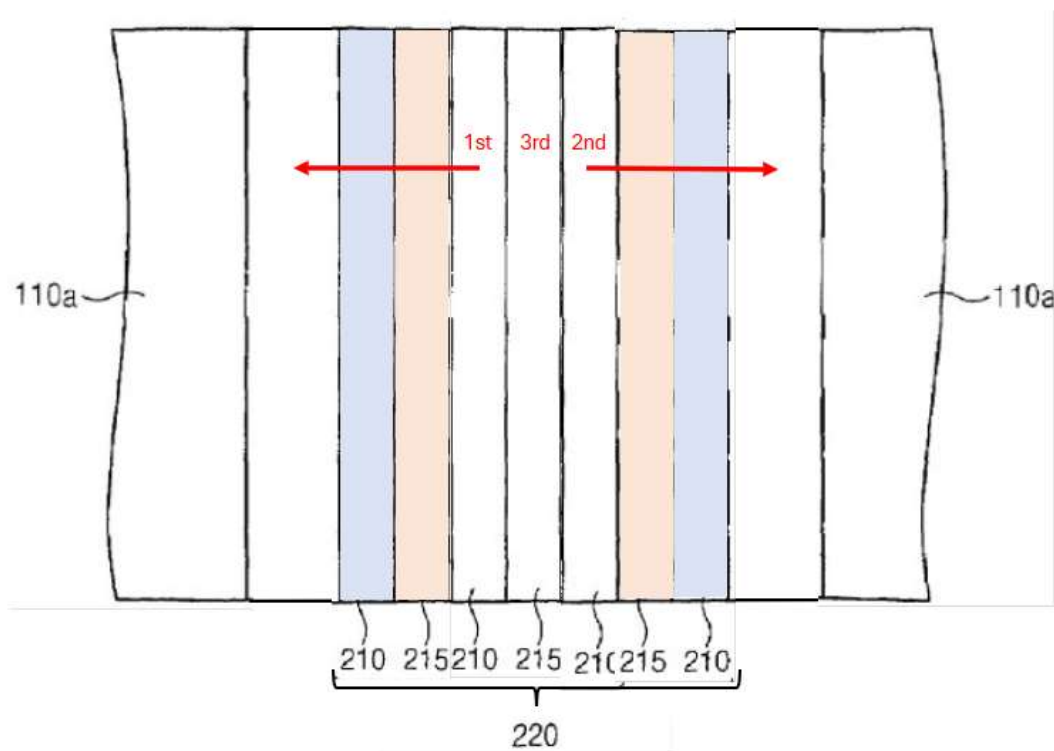
Fig. 4



Hwang, Fig. 4; Hwang, 5:1-4, 9:35-40, 10:6-10.

196. As discussed regarding claim 53, in view of Hwang’s teachings to form a sidewall multi-layered reflection layer 220 by alternately stacking first and second sidewall reflection layers 210 and 215 “a plurality of times,” it would have

been obvious for a POSITA to form a seven-layered reflection layer 220 using four grooves 205, as shown schematically below. Such a peripheral isolation element would satisfy claim 81 because, as shown below, it would comprise (i) the same three layers as discussed in claim limitation 1[e] (*first, second, and third layers*); (ii) a layer shown in orange below (*fourth layer, to the left of the first layer*) disposed between the *first layer* and the *adjacent pixel*; and (iii) a layer shown in orange below (*fifth layer, to the right of the second layer*) disposed between the *second layer* and the *adjacent pixel*.



Hwang, Fig. 4 (annotated and modified).

46. Claim 82: “The imager device of claim 18, wherein the peripheral isolation element comprises five layers.”

197. Hwang teaches or suggests this limitation.

198. See discussion of claim 55.

47. Claim 83: “The imager device of claim 82, wherein the five layers include the first layer, the second layer, the third layer, a fourth layer disposed between the first layer and one of said adjacent pixels and a fifth layer disposed between the second layer and the other one of said adjacent pixels.”

199. Hwang teaches or suggests this limitation.

200. See discussion of claim 81.

B. Ground 2: Claims 12-17, 19-22, 26-29, and 76-79 Are Obvious Based on Hwang and Haddad188

1. Overview of Haddad188

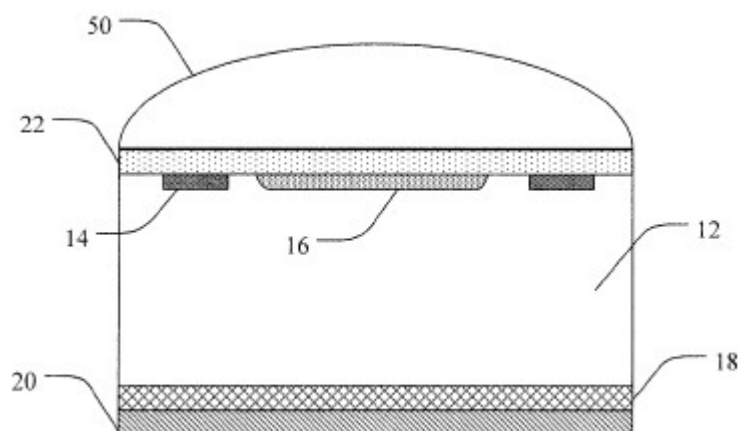
201. I understand that Haddad188 is prior art because it was published on March 24, 2011, before the '359 patent's provisional application filing date of March 22, 2012.

202. Haddad188 is cited on the face of the '359 patent (page 6, second column), among several hundred other references cited. Haddad188 was also cited in an IDS during prosecution of the '359 patent (again among many other references).

203. Like the '359 patent, Haddad188 is directed to light-sensitive pixels in imaging devices with pixel separation structures. Haddad188, 1:24-30 (“The present disclosure provides photosensitive devices and associated methods. In one aspect, for example, a photosensitive device can include a semiconductor substrate having

multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction.”); 21:12-13. Haddad188 also discloses a “textured region at the point of entry of the electromagnetic radiation,” which “provide[s] enhancement and/or filtering of the incoming electromagnetic radiation.” Haddad188, 20:30-21:2. Haddad188’s “textured region includes surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof,” and contemplates “numerous surface feature morphologies.” Haddad188, 2:18-27.

204. An exemplary embodiment from Haddad188 is depicted below.



Haddad188, Fig. 5.

205. Haddad188’s Figure 5 is a schematic view of a photosensitive device. Haddad188, 3:33-34. Among other things, it depicts a “textured region 18 coupled to

the semiconductor substrate and positioned to interact with electromagnetic radiation.”

Haddad188, 9:18-21.

2. Motivation to Combine Hwang and Haddad188

206. A POSITA would have been motivated to use Haddad188’s textured regions with Hwang’s semiconductor substrate faces and sidewall multi-layer reflective layers. Haddad188 teaches that a “textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31. Haddad188 explains that “[t]extured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device.... Such internal reflection causes the effective absorption length to be greater than the thickness of the substrate.” Haddad188, 15:14-18. As a result of increased absorption length, quantum efficiency of the device increases, “leading to an improved signal to noise ratio.” Haddad188, 15:18-19. For example, Haddad188 discloses a “photosensitive device having textured regions on the sides of the semiconductor substrate 12. Such a configuration allows electromagnetic radiation normally exiting through the sides of the device to be further diffused and absorbed within [the] semiconductor substrate.” Haddad188, 21:12-15, Fig. 3. “The textured region(s) can be located on one or more sides to facilitate the enhanced absorption.” Haddad188, 21:15-16. Whether to use

Haddad188's textured regions would have depended on the particular design needs regarding the cost of manufacture and the desired improvement in absorption and sensitivity.

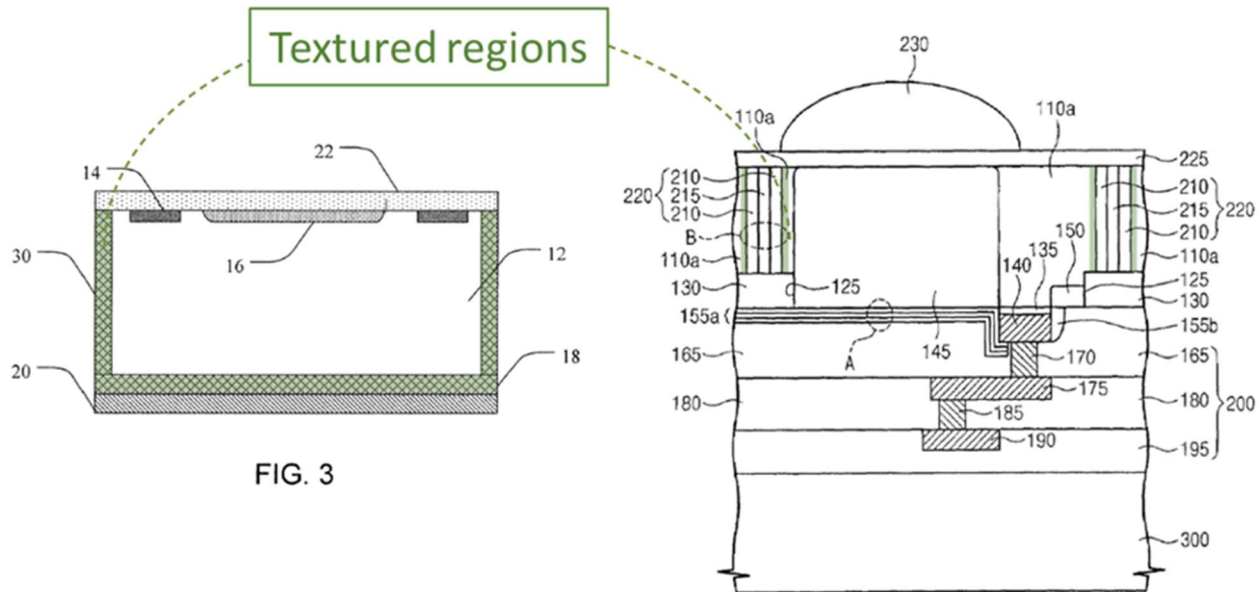
207. Haddad188 discloses that “[o]ne effective method of producing a textured region is through laser processing.” Haddad188, 16:3-4; 16:14-19 (“[A] surface of a semiconductor material is irradiated with laser radiation to form a textured or surface modified region.”). POSITAs would know that laser provides excellent control of the surface profile and may be programmed to offer optical performance that exceeds simple wet and dry etching of surfaces, especially when texturing is being implemented.

208. Using Haddad188's textured regions to further improve light absorption and sensitivity would have been a use of a known technique to improve similar devices in the same way. Both Hwang and Haddad188 are directed to photosensitive imager devices. Hwang, Abstract, 1:14-18, 5:47-51; Haddad188, 1:24-30, 8:15-22. Both Hwang and Haddad188 contemplate using additional layers that improve absorption of external light by reflecting light incident on a pixel back toward the photodiode. *See* Hwang, 7:45-47 (“A base multi-layered reflection layer 155a is interposed between the photodiode 145 and the interlayer insulating layer 200.”), 8:59-9:14 (“[E]xternal light incident on the second surface of the photodiode 145 is reflected by” surfaces of the “base multi-layered reflection layer 155a,” such that reflected light “is incident again

on the photodiode 145. As a result, the rate at which the external light is absorbed by the photodiode 145 is increased to increase the light sensitivity of the image sensor.”), 10:31-34 (“[T]he portion of the light reflected toward the sidewall multi-layered reflection layer 220 from the light reflected by the first and second boundary surfaces is incident again on the photodiode.”), Haddad188, 20:20-22 (“The reflecting layer can be coupled to any side or portion of the semiconductor substrate in order to reflect electromagnetic radiation back into the device.”). Haddad188’s photosensitive devices also include at least one textured region positioned within the semiconductor substrate to interact with electromagnetic radiation to improve efficiency over traditional photosensitive devices. Haddad188, 9:18-21, 9:32-33 (“The various devices according to aspects of the present disclosure can exhibit increased quantum efficiency over traditional photosensitive devices. Any increase in the quantum efficiency makes a large difference in the signal to noise ratio.”).

209. A POSITA would have been motivated to modify Hwang’s sidewall multi-layered reflection layer 220 with Haddad188’s textured region to increase the quantum efficiency of the device. Applying Haddad188’s processing to Hwang’s sidewall multi-layered reflection layer 220 would have yielded a Hwang device such as the following:

Fig. 2



210. A POSITA would have known to apply Haddad188's textured regions to Hwang's photosensitive device. For example, Hwang and Haddad188 both place trench isolation structures between adjacent pixels to reduce optical and electrical crosstalk. *See* Hwang, 6:15-17 ("sidewall multi-layered reflection layer 220 encloses the side walls of the pixel semiconductor patterns 110a"), 10:23-26 ("sidewall multi-layered reflection layer 220 minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels"); Haddad188, 22:21-29 ("Trench isolation elements can maintain pixel to pixel uniformity by reducing optical and electrical crosstalk."), 24:1-15 ("[T]he trench isolation layer can be configured to reflect incident electromagnetic radiation, in some cases until it is absorbed, thereby increasing the effective absorption length of the device.").

211. Given the similarities in structure and function of the image sensors described in Hwang and Haddad188, a POSITA would have recognized that the combination would have required nothing more than applying Haddad188's teachings about textured regions and trench isolation structures to Hwang's teaching of trench structures to isolate image sensor pixels. Indeed, Haddad188 notes that "[t]rench isolation can include dielectric materials, reflective materials, conductive materials, and combinations thereof, including textured regions and other light diffusing features ... to reflect incident electromagnetic radiation." Haddad188, 24:5-8. Thus, applying Haddad188's textured regions to Hwang's pixel isolation structures would have amounted to nothing more than applying a known technique to improve a similar device in the same way, and it would have yielded predictable results.

212. A POSITA would have recognized that incorporating Haddad188's textured regions into Hwang's device would provide certain benefits. Haddad188 explains that "the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation," and can result in "increasing the semiconductor substrate's effective absorption length as compared to a semiconductor substrate lacking a textured region." Haddad188, 1:30-34. Haddad188 also explains that the trench isolation elements can further increase "the effective absorption length of the device." Haddad188, 22:27-29, 24:7-9. Additionally, Haddad188 further explains that when textured regions are placed on the sides of the

device, “electromagnetic radiation normally exiting through the sides of the device” can be “further defused [diffused]⁸ and absorbed within semiconductor substrate,” resulting in “enhanced absorption,” Haddad188, 21:12-16, and that this benefit can be achieved when the textured region is included as part of the trench isolation elements. Haddad188, 24:5-9.

213. A POSITA would have had a reasonable expectation of success. It would have been well within the abilities of a POSITA to use the textured regions described in Haddad188 for Hwang’s device. It would have involved routine manufacturing steps with predictable results. In particular, the fabrication process techniques used would involve standard modules, standard techniques, and standard processes. The fabrication of trench layers, including those with silicon materials and dielectrics, would have been well-known to a POSITA, as would the characteristic properties of the materials, such as optical refractive index, etch rates, and crystal quality. Fabrication processing techniques, including photolithography, etching deposition, and metallization, existed well before the relevant period.

⁸ Haddad188 clarifies that the textured region is used “to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes through to the front side of the pixel” so that the radiation can be “focused within the semiconductor substrate.” Haddad188, 24:34-25:3.

3. Claim 12: “The device of claim 1, wherein at least one of said two adjacent light sensitive pixels comprises a textured region.”

214. This limitation is obvious based on Hwang in view of Haddad188.

215. Hwang’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. As shown above, the modification would entail using *a textured region* in each of Hwang’s *light sensitive pixels*. See Haddad188, 9:18-21 (“In one aspect, as is shown in FIG. 1, a photosensitive diode 10 can include a semiconductor substrate 12 having multiple doped regions 14, 16 forming at least one junction, and at least one textured region 18 coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation.”); *see also* Haddad188, Fig. 5. Haddad188 further discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31.

216. It would have been obvious to combine Hwang and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

217. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein at least one of the said two adjacent light sensitive pixels comprises a textured region*.

4. Claim 13: “The device of claim 12, wherein said textured region is coupled to the light incident surface.”

218. This limitation is obvious based on Hwang in view of Haddad188.

219. Hwang’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. The modification would entail a textured region that is *coupled to the light incident surface*, given that Haddad188 teaches “locating the textured region on the surface adjacent the incident electromagnetic radiation to purposely effectuate the filtering of blue wavelengths.” Haddad188, 20:32-21:2; *see also id.*, 8:9-10. Haddad188 further discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31. Haddad188 also discloses that “a textured region 60 is located on the semiconductor substrate 12 adjacent to the multiple doped regions 14, 16,” Haddad188, 21:33-34, or “[a] textured region 156 can be coupled to the semiconductor 72 opposite the lens,” Haddad188, 24:32-33.

220. Haddad188 further discloses “[a]s has been described, location of the textured region can be used to provide enhancement and/or filtering of the incoming electromagnetic radiation. For example, a textured region located at the point of entry of the electromagnetic radiation into the photosensitive device tends to bend the electromagnetic radiation, particularly the blue wavelengths. Accordingly, one level of tuning can be accomplished by locating the textured region on the surface

adjacent the incident electromagnetic radiation to purposely effectuate the filtering of blue wavelengths.” Haddad188, 20:30-21:2.

221. It would have been obvious to combine Hwang and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

222. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein said textured region is coupled to the light incident surface*.

5. Claim 14: “The device of claim 13, wherein said light incident surface comprises said textured region.”

223. This limitation is obvious based on Hwang in view of Haddad188.

224. Hwang’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. The modification would entail the *light incident surface compris[ing] said textured region*, given that Haddad188 teaches that the “surface features” of the textured region can be formed directly in a semiconductor material. Haddad188 discloses “[v]arious aspects of the textured region can vary depending on the desired configuration of the device. In one aspect, however, the textured region includes surface features.... Numerous surface feature morphologies are contemplated, nonlimiting examples of which include cones, pillars, pyramids, microlenses, quantum dots, inverted features, and combinations thereof.” Haddad188, 2:18-23. Haddad188 discloses that these surface features of the textured region can be formed directly in a semiconductor material. Haddad188, 16:33-17-2 (“[T]he surface of the semiconductor material is chemically and/or structurally altered by

the laser treatment, which may, in some aspects, result in the formation of surface features appearing as microstructures or patterned areas on the surface”). Haddad188 further discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31.

225. It would have been obvious to combine Hwang and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

226. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein said light incident surface comprises said textured region*.

6. Claim 15: “The device of claim 13, wherein said textured region comprises a textured film layer”

227. This limitation is obvious based on Hwang in view of Haddad188.

228. Hwang’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation using *a textured film layer*. Haddad188 discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31. Haddad188 further discloses that “[t]he textured region can be formed by various techniques, including lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, additional material deposition, and the like.” Haddad188, 15:20-29. Haddad188

further explains that “material can be removed to a thickness of about 20 μm ,” Haddad188, 15:25, which is in the ’359 patent’s suggested range of “1nm to 20 μm .” ’359 patent, 14:22-23. A POSITA would therefore understand that Haddad188’s textured region can be formed as a textured film layer through material deposition.

229. It would have been obvious to combine Hwang and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

230. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein said textured region comprises a textured film layer*.

7. Claim 16: “The device of claim 15, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”

231. This limitation is obvious based on Hwang in view of Haddad188.

232. Hwang’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. Haddad188 discloses “a passivation layer 22 ... is shown coupled to the side of the semiconductor substrate facing the incoming electromagnetic radiation, however a passivation layer can be located anywhere on the device and still be within the present scope.” Haddad188, 20:26-29, Fig.2. Further, “a textured region located at the point of entry of the electromagnetic radiation into the photosensitive device tends to bend the electromagnetic radiation, particularly the blue wavelengths. Accordingly, one level of tuning can be accomplished by locating the textured region on the surface adjacent the incident electromagnetic radiation.”

Haddad188, 20:32-21:1. Taking these teachings together, a POSITA would have reason to make a textured film layer at the point of entry *compris[ing]silicon dioxide* given its passivating quality.

233. Haddad188 further discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31. Haddad188 further discloses that “[a] variety of semiconductor materials are contemplated for use with [its] devices” and that the semiconductor material in which the textured region is formed “can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types.” Haddad188, 10:24-27. Accordingly, Haddad188 discloses that the *textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof*.

234. A POSITA would seek a transparent material capable of texturing so as not to interfere with the reflective qualities of the layered pixel separation structure of Hwang. Reviewing the groups of materials disclosed in Haddad188 at 10-11, a POSITA would have recognized amorphous silicon and multicrystalline silicon (also known as polysilicon), for example, as materials that may be readily textured and used in transparent applications, depending upon processing. As such, a POSITA would

understand that Haddad188 would rely on such transparent materials for its textured regions, thereby making them obvious to try.

235. It would have been obvious to combine Hwang and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

236. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein said textured region comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.*

8. Claim 17: “The device of claim 12, wherein said backside surface comprises said textured region.”

237. This limitation is obvious based on Hwang in view of Haddad188.

238. Hwang’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. The modification would entail the *backside surface compris[ing] a textured region*, given that “a textured region 90 is coupled to the semiconductor substrate 72 opposite the doped regions 74,76. Thus light entering from the direction of the doped regions passes through the semiconductor substrate prior to contacting the textured region. The textured region can be disposed across an entire surface of the semiconductor substrate, as is shown in FIG. 9, or it can be disposed on one or more discrete regions (not shown).” Haddad188, 23:9-14. Moreover, Haddad188 teaches that its textured regions can not only be coupled to the semiconductor substrate, but can also be produced within the substrate. Haddad188, 16:3-5 (“One effective method of producing a textured region is through laser

processing. Such laser processing allows discrete locations of the semiconductor substrate to be textured.”), 16:14-15 (“In one aspect, for example, a target region of the semiconductor material can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Patents 7,057,256, 7,354,792, and 7,442,629, which are incorporated herein by reference in their entireties.”). Accordingly, a POSITA would have understood that the backside semiconductor substrate could have a textured region coupled thereto or have a textured region formed directly therein.

239. It would have been obvious to combine Hwang and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

240. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein the backside surface comprises the textured region*.

9. Claim 19: “The device of claim 18, wherein at least one of said light incident surface and said backside surface of at least one of said two adjacent light sensitive pixels comprises a textured region.”

241. This limitation is obvious based on Hwang in view of Haddad188.

242. As discussed above regarding claims 13 and 14, Hwang in view of Haddad188 renders obvious the device of claims 1 and 18 wherein the *light incident surface comprises a textured region*.

243. As discussed above regarding claim 17, Hwang in view of Haddad188 renders obvious the device of claims 1 and 18 wherein the *backside surface comprises a textured region*.

10. Claim 20: “The device of claim 19, wherein said textured region is a textured film layer.”

244. This limitation is obvious based on Hwang in view of Haddad188.

245. See discussion of claim 15.

11. Claim 21: “The device of claim 20, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”

246. This limitation is obvious based on Hwang in view of Haddad188.

247. See discussion of claim 16.

12. Claim 22: “The device of claim 19, wherein said textured region reflects at least a portion of light internally incident thereon into the at least one pixel.”

248. This limitation is obvious based on Hwang in view of Haddad188.

249. Hwang’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. The modification would provide a *textured region that reflects at least a portion of light internally incident thereon into the at least one pixel*, given that Haddad188 discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31. Haddad188 discloses that “[a]s is shown in FIG. 13,

the textured region 130 can have a nonparallel [i.e., non-uniform] surface with respect to the semiconductor substrate 72 as has been described. This nonparallel morphology, when included with the deep trench isolation 120, *can effectively focus electromagnetic radiation into the semiconductor substrate from multiple sides.*” Haddad188, 24:11-15. Haddad188 further discloses that its textured regions achieve “internal reflection” of “incident electromagnetic radiation” to “allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device.” Haddad188, 15:14–18.

250. It would have been obvious to combine Hwang and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

251. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein the textured region reflects at least a portion of light internally incident thereon into the pixel.*

13. Claim 26: “The device of claim 19, wherein the textured region is formed by laser radiation.”

252. This limitation is obvious based on Hwang in view of Haddad188.

253. Hwang’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. The modification would entail forming the *textured region using laser radiation*, given that Haddad188 discloses that “[o]ne effective method of producing a textured region is through laser processing. Such laser processing allows discrete locations of the semiconductor substrate to be

textured. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope.” Haddad188, 16:3-7; 16:14-19 (“[A] surface of a semiconductor material is irradiated with laser radiation to form a textured or surface modified region.”). Haddad188 further discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31. A POSITA would know that laser provides excellent control of the surface profile and may be programmed to offer optical performance that exceeds simple wet and dry etching of surfaces, especially when texturing is being implemented. A POSITA would have been familiar with using laser radiation as a normal processing fabrication tool.

254. It would have been obvious to combine Hwang and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

255. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein the textured region is formed by laser radiation*.

14. Claim 27: “The device of claim 12, wherein the textured region is formed by one of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.”

256. This limitation is obvious based on Hwang in view of Haddad188.

257. As discussed above regarding claim 12, Hwang in view of Haddad188 renders obvious an imager device with a textured region. Modifying Hwang's imaging device according to Haddad188's processing would satisfy this limitation. Haddad188 discloses that "the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device." Haddad188, 14:29-31. Haddad188 further discloses that "[a]dditionally, the textured region can be formed by a variety of processes. Nonlimiting examples of such texturing processes can include lazing [i.e., lasing or laser processing⁹], chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, and combinations thereof." Haddad188, 2:18-27.

258. It would have been obvious to combine Hwang and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

259. Accordingly, it would have been obvious for a POSITA to make an imager device *wherein the textured region is formed by one of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.*

⁹ Haddad188 explains that "[o]ne effective method of producing a textured region is through laser processing" or "[l]aser treatment." Haddad188, 16:3-4.

15. Claim 28: “The device of claim 12, wherein the textured region is formed by laser radiation.”

260. This limitation is obvious based on Hwang in view of Haddad188.

261. See discussion of claim 26.

16. Claim 29: “The device of claim 12, wherein said textured region is coupled to the backside surface.”

262. This limitation is obvious based on Hwang in view of Haddad188.

263. See discussion of claim 17.

17. Claim 76: “The imager device of claim 1, wherein the peripheral isolation element comprises a textured region.”

264. This limitation is obvious based on Hwang in view of Haddad188.

265. As discussed above regarding limitation 1[b], Hwang discloses a *peripheral isolation element* layer 220 at least partially separating adjacent light sensitive pixels. Hwang’s imaging device as modified to use Haddad188’s textured regions would satisfy this limitation. As discussed and shown above, the modification would entail locating *a textured region* along the *peripheral isolation element*, given that Haddad188 discloses that “FIG. 3 shows a photosensitive device having textured regions 30 located on the sides of the semiconductor substrate 12. Such a configuration allows electromagnetic radiation normally exiting through the sides of the device to be further defused [diffused] and absorbed within semiconductor substrate. The textured region(s) can be located on one or more sides to facilitate the enhanced absorption.” Haddad188, 21:12-16; *see also* Haddad188, 22:21-29, 24:1-

15. Haddad188 also discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31. Furthermore, Haddad188 discloses that “trench isolation can include ... textured regions.” Haddad188, 24:5-6. Similarly, Hwang discloses that “device isolation pattern 130 can be in a shape that fills a trench 125 formed on the first surface of the pixel semiconductor pattern 110a.” Hwang, 6:43-45.

266. It would have been obvious to combine Hwang and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

267. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein the peripheral isolation element comprises a textured region*.

18. Claim 77: “The imager device of claim 1, wherein the peripheral isolation element further comprises a first textured region between the first layer and one of said adjacent pixels and a second textured region between the second layer and the other one of said adjacent pixels.”

268. This limitation is obvious based on Hwang in view of Haddad188.

269. As discussed above regarding limitation 1[b], Hwang discloses *peripheral isolation elements separating adjacent light sensitive pixels*. Hwang further explains that “the sidewall multi-layered reflection layer 220 can be disposed along the boundaries of all of the pixel semiconductor patterns 110a, and all of the pixel semiconductor patterns 110a can thus be separated by the sidewall multi-

layered reflection layer 220.” Hwang, 6:19-23. Haddad188 further discloses that “[t]rench isolation can include dielectric materials, reflective materials, conductive materials, and combinations thereof, including textured regions and other light diffusing features. Thus, the trench isolation layer can be configured to reflect incident electromagnetic radiation, in some cases until it is absorbed, thereby increasing the effective absorption length of the device.” Haddad188, 24:5-9. Haddad188 further discloses that “FIG. 3 shows a photosensitive device having textured regions 30 located on the sides of the semiconductor substrate 12. Such a configuration allows electromagnetic radiation normally exiting through the sides of the device to be further defused [diffused] and absorbed within semiconductor substrate. The textured region(s) can be located on one or more sides to facilitate the enhanced absorption.” Haddad188, 21:12-16.

270. Haddad188 further discloses providing a textured region between a pixel and reflective and passivation layers. Haddad188, 20:19-29 (“Thus, as is shown in FIG. 2, electromagnetic radiation passing through the semiconductor substrate and the textured region [18] can be reflected back [by reflecting layer 20] into the semiconductor substrate. Additionally, a passivation layer 22 can be coupled to the substrate. ... [A] passivation layer can be located anywhere on the device and still be within the present scope.”); Fig 2 (below).

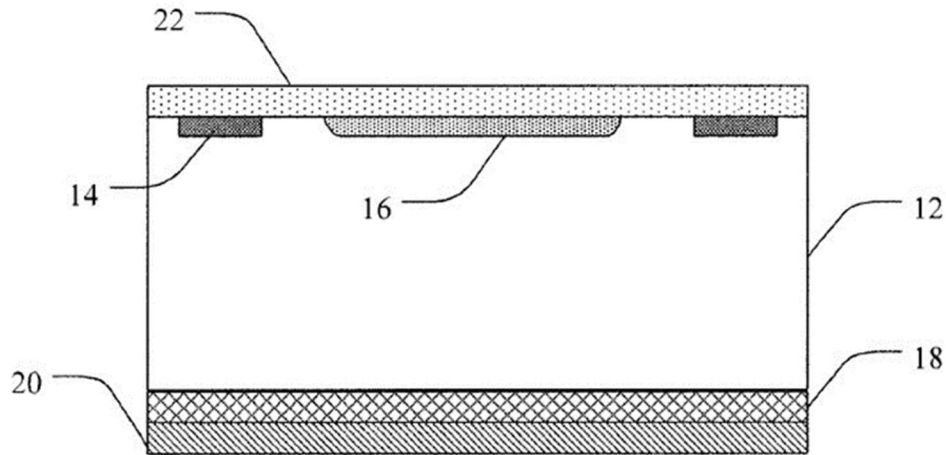


FIG. 2

271. As discussed above regarding limitation 1[e], Hwang discloses a peripheral isolation element that comprises a *first*, a *second*, and a *third layer*. Specifically, as shown in Figure 2, Hwang discloses a “second sidewall reflection layer 215 interposed between two first sidewall reflection layers 210.” Hwang, 10:14-17, 10:48-50. Hwang further explains that “the refractive index of the first sidewall reflection layer 210 can be lower than the refractive indexes of the pixel semiconductor pattern 110a and the second sidewall reflection layer 215.” Hwang, 9:63-66. Specifically, Hwang teaches that the first sidewall reflection layer 210 (*first* and *second layers*) and second sidewall reflection layer 215 (*third layer*) have different refractive indices. Because the interfaces formed between these three layers of different refractive indices is an important characteristic of the quality of the isolation, it would be logical for a POSITA to put the textured region in between the

outermost layers of the peripheral isolation element (*first and second layers*) and the adjacent pixel to improve isolation. *See supra* §VII.B.2. Haddad188 further discloses that “the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Haddad188, 14:29-31.

272. Adding a textured region on either side of Hwang’s sidewall multi-layered reflection layer 220, following the teaching of Haddad188’s Figure 2, is consistent with both references’ objective of increasing absorption of electromagnetic radiation and improving isolation.

273. It would have been obvious to combine Hwang and Haddad188, with a reasonable expectation of success, as discussed in Section VII.B.2 above.

274. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein the peripheral isolation element further comprises a first textured region between the first layer and one of said adjacent pixels and a second textured region between the second layer and the other one of said adjacent pixels.*

19. Claim 78: “The imager device of claim 18, wherein the peripheral isolation element comprises a textured region.”

275. This limitation is obvious based on Hwang in view of Haddad188.

276. See discussion of claim 76.

- 20. Claim 79: “The imager device of claim 18, wherein the peripheral isolation element further comprises a first textured region between the first layer and one of said adjacent pixels and a second textured region between the second layer and the other one of said adjacent pixels.”**

277. This limitation is obvious based on Hwang in view of Haddad188.

278. See discussion of claim 77.

C. Ground 3: Claims 6, 8, 9, 11, 24, 30, 32, 34, and 36 Are Obvious Based on Hwang and Shinohara

1. Overview of Shinohara

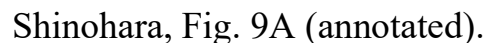
279. I understand that Shinohara is prior art because it was published on February 9, 2012, before the '359 patent's provisional application filing date of March 22, 2012.

280. Shinohara was not listed in any IDS and was not discussed during prosecution of the '359 patent.¹⁰

281. Like the '359 patent, Shinohara is directed to light-sensitive pixels in imaging devices with pixel separation structures. Shinohara, Abstract (“A solid state imaging device having a backside illuminated structure, includes: a pixel region in which pixels each having a plurality of pixel transistors are arranged in a two-dimensional matrix; an element isolation region isolating the pixels which is

¹⁰ The patent that issued from Shinohara (U.S. Patent No. 8,749,679) also was not discussed during prosecution.

282. An exemplary embodiment from Shinohara is depicted below.



94

of the surface 22 a as well as in the void 44.” *Id.*, [0090]. Shinohara teaches that using an insulating film having a negative fixed charge enhances the passivation characteristics of the element isolation region. *Id.*, [0095]. Accordingly, Shinohara discloses using “a film of hafnium dioxide (HfO_2), dialuminum trioxide (Al_2O_3), ditantalum pentaoxide (Ta_2O_5), dilanthanum trioxide (La_2O_3), or diyttrium trioxide (Y_2O_3)” as insulating film 69. *Id.*, [0091].

2. Motivation to Combine Hwang and Shinohara

284. It would have been obvious to combine Hwang and Shinohara.

285. A POSITA would have been motivated to select from Shinohara’s insulating film materials for Hwang’s sidewall multi-layered reflective layer. Shinohara notes a known method in which “an element isolation region which physically isolates pixels is formed by a trench method in a rear surface of a substrate so as to suppress leakage of charge into an adjacent pixel.” Shinohara, [0011]. This leakage of charge results in a decrease in sensitivity of the pixel. Shinohara, [0012]. Accordingly, Shinohara teaches manufacturing a solid-state imaging device by “forming a trench having a predetermined depth in a semiconductor substrate from a surface thereof; and filling a semiconductor layer in the trench by an epitaxial growth to form an element isolation region.” Shinohara, [0017].

286. Hwang discloses that for sidewall multi-layered reflective layer 220, “the refractive index of the first sidewall reflection layer 210 can be lower than the

refractive indexes of the pixel semiconductor pattern 110a and the second sidewall reflection layer 215.” Hwang, 9:63-66. Hwang discloses a peripheral isolation element comprising at least two materials having different indices of refraction. Hwang, 10:14-17, 10:45-50. Hwang explains that the refractive index of the first sidewall reflection layer 210 of silicon oxide ($n=1.46$) or air ($n=1$) can be lower than the refractive indexes of the pixel semiconductor pattern 110a and the second sidewall reflection layer 215 (both silicon, $n\approx 4$). Hwang, 9:28-30, 9:63-66, 10:2-4. POSITAs would have known that the interface state between Si and SiO₂ existing in the sidewalls of the trench separation structures generates large noises and causes the S/N ratio to rapidly deteriorate. *See, e.g.*, Iida, [0007]. A POSITA would have been motivated to consider Shinohara to identify other potential materials, within Hwang’s constraints, to further improve absorption and sensitivity.

287. For example, Shinohara teaches that an insulating film having a negative fixed charge can comprise materials such as “dialuminum trioxide (Al₂O₃).” Shinohara, [0091]. A POSITA would consider using Shinohara’s Al₂O₃ for Hwang’s first sidewall reflection layer 210 because aluminum oxide exhibits better passivation and lower surface velocity recombination than silicon dioxide. Ex-1010 at 1-3; *see also* ’359 patent, 9:54-65. Forming Hwang’s pixel isolation groove results in an exposed surface of the silicon substrate. “The sidewall multi-layered reflection layer 220 includes a material layer 210 [(silicon dioxide)] filling the grooves 205 and the residual

portion 215 [(silicon)] of the semiconductor layer 110 disposed between the grooves 205.” Hwang, 12:53-5; *see also* Hwang, 13:11-13 (“[A]fter the plurality of grooves 205 is formed, a silicon oxide layer that fills the plurality of grooves 205 can be formed.”). However, dark current may be generated from the interface state between Si and SiO₂.

288. Surface recombination contributes to dark current, which reduces image quality. A POSITA would seek to minimize surface recombination velocity along the side faces and the bottom face of the trench so that converted charge is retained longer in the silicon substrate for collection. Depositing Shinohara’s Al₂O₃ in place of Hwang’s first sidewall reflection layer 210 silicon dioxide would provide a surface velocity recombination of about 10 cm/s, Ex-1010 at 2-3, thus improving the image quality of Hwang’s imager device.

289. Further, Shinohara teaches that an insulating film having a negative fixed charge can comprise materials such as “ditantalum pentaoxide (Ta₂O₅) [or] dilanthanum trioxide (La₂O₃).” Shinohara, [0091]. Ta₂O₅ and La₂O₃ are negative fixed charge films offering better passivation than Hwang’s silicon dioxide, while also providing indices of refraction that maintain Hwang’s teaching to “induc[e] constructive interference of light reflected by at least one boundary in the sidewall multi-layered reflection layer and a boundary between the sidewall multi-layered

reflection layer and the pixel semiconductor pattern.” Hwang, 2:25-29; Ex-1020 at 9758; Ex-1021 at 46.

290. Hwang and Shinohara are directed to the same field of endeavor: semiconductor image sensors. Hwang, 1:14-18, 5:47-57; Shinohara, [0051]. Furthermore, Hwang and Shinohara are specifically directed to placing trench isolation structures between adjacent pixels to reduce crosstalk. Hwang, 6:15-17 (“sidewall multi-layered reflection layer 220 encloses the side walls of the pixel semiconductor patterns 110a”), 10:23-26 (“sidewall multi-layered reflection layer 220 minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels”), 12:42-53 (“[S]emiconductor layer 110 can selectively be etched to form a plurality of grooves 205 surrounding the pixel semiconductor patterns 110a. ... [T]he grooves 205 are filled with a predetermined material. Thus, a sidewall multi-layered reflection layer 220 is formed.”); Shinohara, [0021] (“[S]ince the semiconductor layer in the trench by an epitaxial growth functions as a pinning layer, the generation of white spots and dark current in the element isolation region can be suppressed. Since the isolation power of the element isolation region is enhanced, the leakage of photoelectrically converted charge into an adjacent pixel can be prevented.”), [0090] (“[A]n element isolation region 68 for isolating pixels is formed such that the p-type semiconductor layer 43 is provided in the trench 42 by an epitaxial growth, and an insulating film 69 is filled in the void 44 inside this p-type semiconductor layer 43.”).

291. Shinohara's method for manufacturing the filled trench is directed, in part, to overcome shortcomings of the existing prior art whereby it is "difficult to solve the causes of the generation of white spots and dark current by the trench formation. That is, there have been problems in that an inside wall of the trench may not be placed in a hole pinning state by a p-type impurity layer and the defects are not recovered by annealing or the like." Shinohara, [0011]. Shinohara's trench filling material is also intended to provide further prevention of electrical and optical crosstalk. Shinohara, [0094]. In addition to performance benefits, Shinohara's disclosed process purports to yield a more efficient manufacturing process. Shinohara, [0093], [0096] (referencing [0088]-[0089]). Like Shinohara, Hwang considers the fabrication and processing of a pixel separation structure. *See generally* Hwang, 13:20-15:32. Whether to use the materials identified in Shinohara for Hwang's sidewall multi-layered reflection layer 220 would have depended on the particular design needs and manufacturing considerations to achieve the desired improvements in electrical and optical crosstalk.

292. Building Hwang's imager device using the materials described in Shinohara would have been a simple design choice to improve similar devices in the same way, with no need for experimentation. Given the similarities in structure and function of the image sensors described in Hwang and Shinohara, a POSITA would have recognized that the combination would have required nothing more than applying Shinohara's teachings about trench isolation structures and their materials to Hwang's

device using trench structures to isolate image sensor pixels. This would amount to nothing more than applying a known technique to improve a similar device in the same way, and it would have yielded predictable results.

293. Further, building a Hwang imager device using the trench isolation structures and materials described in Shinohara would have been nothing more than a simple design choice. As Shinohara teaches, a POSITA understood that “it is important to suppress the occurrence of color mixture caused by leakage of charge (such as electron) photoelectrically converted in the vicinity of the rear surface side into an adjacent pixel.” Shinohara, [0008]. “[S]ince the filled insulated film 69 has a refractive index different from that of the p-type semiconductor layer 43, even if inclined incident light is incident thereon, the light is not photoelectrically converted in an adjacent pixel after passing through the element isolation region 68.” Shinohara, [0094]. POSITA would have looked to Shinohara to identify a material for Hwang’s pixel separation structure to improve “the rate at which the external light is absorbed by the photodiode 145.” Hwang, 9:12-13. In view of these recognized needs and similarity in structure and function of the isolation trenches in Hwang and Shinohara, a POSITA would have been motivated to look to Shinohara’s alternative designs for trench isolation materials.

294. A POSITA would have had a reasonable expectation of success. It would have been well within the abilities of a POSITA to use the materials described in Shinohara for Hwang’s device. It would have involved routine manufacturing steps

that Hwang had already used in its device with predictable results. In particular, the fabrication process techniques used would involve standard modules, standard techniques, and standard processes. The fabrication of trench layers, including those with silicon materials and dielectrics, would have been well-known to a POSITA, as would the characteristic properties of the materials, such as optical refractive index, etch rates, and crystal quality. Fabrication processing techniques, including photolithography, etching deposition, and metallization, existed well before the relevant period.

3. Claim 6: “The device of claim 1, wherein at least one of the first and second layer comprises Al_2O_3 .”

295. This limitation is obvious based on Hwang in view of Shinohara.

296. As explained above, it would have been obvious in light of Shinohara to use Al_2O_3 for Hwang’s layer 210 (*first and second layers*).

297. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein at least the first layer comprises Al_2O_3* .

4. Claim 8: “The device of claim 1, wherein said peripheral isolation element provides a passivating negative charge.”

298. This limitation is obvious based on Hwang in view of Shinohara.

299. As explained above, it would have been obvious in light of Shinohara to use Al_2O_3 for Hwang’s layer 210 (*first and second layers*) and thereby provide a *passivating negative charge*. Shinohara’s insulating film provides a passivating

negative charge. Accordingly, the generation of white spots and dark current can be suppressed. Shinohara, [0095] (“When the insulating film having a negative fixed charge is used as the insulating film 69, the hole pinning state by p-type semiconductor layer 43 of the element isolation region 68 can be enhanced.”); *see also id.*, [0021], [0103].

300. Accordingly, it would have been obvious to a POSITA to build an imager device *wherein said peripheral isolation element provides a passivating negative charge.*

5. Claim 9: “The device of claim 1, wherein said peripheral isolation element exhibits a surface recombination velocity as low as 10 cm/s.”

301. This limitation is obvious based on Hwang in view of Shinohara.

302. As explained above, it would have been obvious in light of Shinohara to use Al₂O₃ for Hwang’s layer 210 (*first and second layers*). Further, POSITAs would seek to lower the surface recombination velocity at the wall of Hwang’s *peripheral isolation element* sidewall multi-layered reflection layer 220 to ensure that the accumulated charge can be collected before it recombines. To this end, POSITAs would be aware that an aluminum oxide fixed charge layer 210 (*first and second layers*) would *exhibit a surface recombination velocity as low as 10 cm/s*. Ex-1010 at 2-3 *see also* ’359 patent, 9:58-60 (“Low surface recombination velocities, as low as 10

cm/s can be obtained through various deposition processes of Al_2O_3 layers on the silicon substrate”).

6. Claim 11: “The device of claim 1, wherein the peripheral isolation element comprises any of aluminum oxide and hafnium oxide.”

303. This limitation is obvious based on Hwang in view of Shinohara.

304. As explained above, it would have been obvious in light of Shinohara to use Al_2O_3 for Hwang’s layer 210 (*first and second layers*).

305. Accordingly, it would have been obvious to a POSITA to build an imager device *wherein said peripheral isolation element comprises any of aluminum oxide and hafnium oxide*.

7. Claim 24: “The device of claim 18, wherein said at least two materials comprises silicon dioxide and aluminum oxide.”

306. This limitation is obvious based on Hwang in view of Shinohara.

307. As discussed regarding claim 53, Hwang’s sidewall multi-layered reflection layer 220 can be constructed of seven layers, beginning with layer 210 and alternating between material layers 210 and 215. In a seven-layer construct of Hwang’s sidewall multi-layered reflection layer, the layers can therefore be 210 (silicon dioxide) - 215 (silicon) - 210 (silicon dioxide) - 215 (silicon) - 210 (silicon dioxide) - 215 (silicon) - 210 (silicon dioxide).

308. As explained above, it would have been obvious in light of Shinohara to use Al_2O_3 for Hwang’s outermost layers 210. Specifically, to yield the benefits

discussed, POSITAs would use aluminum dioxide as a replacement for the outermost sidewall reflection layers 210. The resulting sidewall multi-layered reflection layer structure would be 210 (aluminum oxide; $n=1.76$) - 215 (silicon; $n\approx 4$) - 210 (silicon dioxide; $n=1.46$) - 215 (silicon; $n\approx 4$) - 210 (silicon dioxide; $n=1.46$) - 215 (silicon; $n\approx 4$) - 210 (aluminum oxide; $n=1.76$). Accordingly, this modification would entail a sidewall multi-layered reflection layer 220 *compris[ing] silicon dioxide and aluminum oxide*.

8. Claim 30: “The device of claim 1, wherein said peripheral isolation element comprises tantalum oxide.”

309. This limitation is obvious based on Hwang in view of Shinohara.

310. As explained above, it would have been obvious in light of Shinohara to use Ta₂O₅ for Hwang’s layer 210 (*first and second layers*). POSITAs would understand that ditantalum pentaoxide (Ta₂O₅) is *tantalum oxide* and would use these terms interchangeably. See Ex-1018 at B-136 (defining formula of “tantalum oxide” as “Ta₂O₅”).

311. Accordingly, it would have been obvious for a POSITA to make an imager device *wherein said peripheral isolation element comprises tantalum oxide*.

9. Claim 32: “The device of claim 1, wherein said peripheral isolation element comprises lanthanum oxide.”

312. This limitation is obvious based on Hwang in view of Shinohara.

313. As explained above, it would have been obvious in light of Shinohara to use La_2O_3 for Hwang's layer 210 (*first and second layers*). POSITAs would understand that dilanthanum trioxide (La_2O_3) is *lanthanum oxide* and would use these terms interchangeably. See Ex-1018 at B-98-99 (defining formula of "lanthanum oxide" as " La_2O_3 ").

314. Accordingly, it would have been obvious for a POSITA to make an imager device *wherein said peripheral isolation element comprises lanthanum oxide*.

10. Claim 34: "The device of claim 18, wherein said peripheral isolation element comprises tantalum oxide."

315. This limitation is obvious based on Hwang in view of Shinohara.

316. See discussion of claim 30.

11. Claim 36: "The device of claim 18, wherein said peripheral isolation element comprises lanthanum oxide."

317. This limitation is obvious based on Hwang in view of Shinohara.

318. See discussion of claim 32.

D. Ground 4: Claims 44, 51, 65-66, and 71-72 Are Obvious Based on Hwang and Roy

1. Overview of Roy

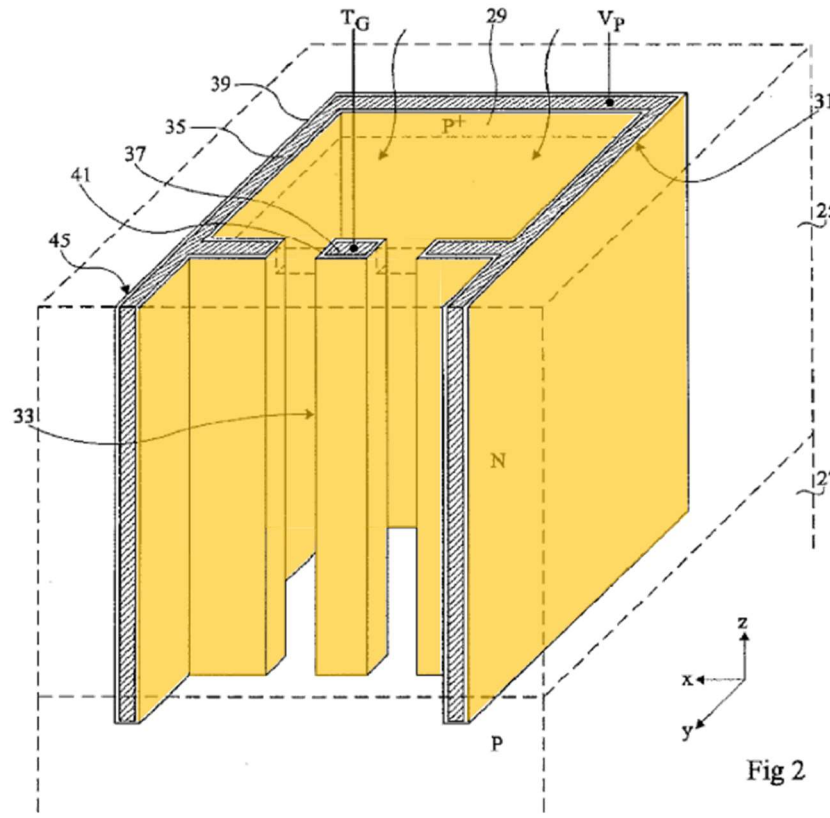
319. I understand that Roy is prior art because it was published on October 29, 2009, before the '359 patent's provisional application filing date of March 22, 2012.

320. Roy was not cited in any IDS and was not discussed during prosecution of the '359 patent.¹¹

321. Like the '359 patent, Roy is directed to light-sensitive pixels in imaging devices with pixel separation structures. Roy, Abstract (“An image sensor formed in a semiconductor stack of a lower region of a first conductivity type and of an upper region of a second conductivity type, including: a photodiode formed of a first portion of the stack. . .”). Also, like the '359 patent, Roy refers to a “photodiode [that] is delimited by an enclosure comprising a trench.” Roy, [0050].

322. An exemplary embodiment from Roy is depicted below:

¹¹ The patent that issued from Roy (U.S. Patent No. 8,193,479) also was not discussed during prosecution.



Roy, Fig. 2 (annotated).

323. Roy's Figure 2 is a perspective view of a photodiode associated with a charge transfer system of an image sensor. Roy, [0029]. Among other things, Roy's Figure 2 depicts trenches 31 and 45 and column 33 that may have varying widths, and thin insulating films 39 and 41. Roy, [0050], [0057].

2. Motivation to Combine Hwang and Roy

324. It would have been obvious to combine Hwang and Roy. More specifically, a POSITA would have been motivated to apply Roy's teachings regarding dimensions of pixel separation structures to Hwang's imaging device and would have had a reasonable expectation of success in doing so.

325. POSITAs were concerned with “decreas[ing] the size of image sensor pixels” to decrease volume constraints, Roy, [0007], and as products were becoming smaller, there was “a need for an image sensor comprising pixels of small dimensions,” Roy, [0011]. Indeed, Roy discloses a device in which “[h]eavily-doped P-type area 29 may have dimensions approximately equal to 1 x 1 μm .” Roy, [0057]. A POSITA would have recognized that smaller image sensors are particularly beneficial for mobile applications such as smartphones and other hand-held electronics because limited space must be shared between all components of the device (such as batteries, displays, antennas, and processing units, among others). Indeed, miniaturization has been a common goal and metric for consumer products for the past thirty to forty years.

326. With regard to performance of image sensor pixels, Hwang recognizes that “the configuration of the image sensor” can “reduce [its] spectral sensitivity.” Hwang, 1:36-38. “Spectral sensitivity is one of the crucial characteristics of an image sensor.” Hwang, 1:30-31. To limit such problems, Hwang teaches forming sidewall multi-layered reflection layers disposed between the side walls of the pixel semiconductor patterns. *See* Hwang, 9:41-10:5. With use of these reflection layers, “occurrence if interference between neighboring pixels can be minimized.” Hwang, 10:17-18.

327. Hwang provides some framework for the dimensions of its sidewalls, suggesting around 160nm and 200nm total for layers 210 and 215, depending on material. *See* Hwang, 10:48-60. Accordingly, a POSITA seeking to implement Hwang's imaging device would be motivated to look elsewhere for further guidance for the dimensions of the device's sidewall multi-layered reflection layers.

328. A POSITA would look to Roy for this purpose. Roy notes that the pixel dimensions of prior art imaging devices were "not optimized," Roy, [0009]; notes, like Hwang, the need to design such devices with "pixels of small dimensions and high storage capacities" with "insulation enabling limiting crosstalk," Roy, [0011], [0012-0015]; and teaches pixel separation structure dimensions that achieve such objectives, Roy, [0057] (teaching specific depth and width ranges), [0045] (teaching that invention achieves "an image sensor having reduced dimensions ... with a low crosstalk, with a low dark current, and enabling efficient transfer of the electrons"), [0053], [0069] (teaching that invention enables "photodiodes of very small dimensions having a significant electron accumulation capacity").

329. A POSITA would have had a reasonable expectation of success in combining Hwang and Roy in this manner. Both Hwang and Roy are directed to image sensor devices comprising light-sensitive pixels, including specifically the design of trench isolation structures placed between adjacent pixels to reduce crosstalk. *See, e.g.*, Hwang, 10:36-60; Roy, Abstract, [0057]. Given the similarities

in structure, scale, and function of the image sensors and pixel separation structures taught by Hwang and Roy, building Hwang's imaging device using the pixel isolation structure dimensions taught by Roy would have been a simple design choice for applying a known technique to yield a predictable result.

330. It would have been well within a POSITA's abilities to use the dimensions taught by Roy in forming the pixel separation structures in Hwang's device; indeed, it would have involved routine manufacturing steps that both Hwang and Roy disclose. *See, e.g.*, Hwang, 12:42-53 (“[S]emiconductor layer 110 can selectively be etched to form a plurality of grooves 205 surrounding the pixel semiconductor patterns 110a. ... [T]he grooves 205 are filled with a predetermined material. Thus, a sidewall multi-layered reflection layer 220 is formed.”); Roy, [0082] (“forming, in trench(es) 31/45 in and column(s) 33, thin insulating layers 39 and 41, followed by polysilicon 35 and 37”). Roy also teaches that its pixel separation structure dimensions increase “manufacturing simplicity,” Roy, [0079], further motivating the POSITA to use them for Hwang's device and further reinforcing the POSITA's expectation of success. In particular, the fabrication process techniques used would involve standard modules, standard techniques, and standard processes. The fabrication of trench layers, including those with silicon materials and dielectrics, would have been well-known to a POSITA, as would the characteristic properties of the materials, such as optical refractive index, etch rates, and crystal quality.

Fabrication processing techniques, including photolithography, etching deposition, and metallization, existed well before the relevant period.

3. Claim 44: “The device of claim 1, wherein said peripheral isolation element has a width in a range from about 100 nm to about 50 microns.”

331. This limitation is obvious based on Hwang in view of Roy.

332. As discussed above regarding claim 1, Hwang discloses a peripheral isolation element comprising a “sidewall multi-layered reflection layer 220.” Roy discloses that its trench 31/45 and column 32 “may have a width of approximately 0.2 μ m and be separated, at the level of the interruption area of trench 31, by a distance approximately equal to 0.2 μ m,” i.e., 200 nm. Roy, [0057].

333. It would have been obvious to combine Hwang and Roy, with a reasonable expectation of success, as discussed in Section VII.D.2 above.

334. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein the peripheral isolation element has a width in a range from about 100 nm to 50 microns.*

4. Claim 51: “The device of claim 18, wherein said peripheral isolation element has a width in a range from about 100 nm to about 50 microns.”

335. This limitation is obvious based on Hwang in view of Roy.

336. See discussion of claim 44.

5. Claim 65: “The imager device of claim 64, wherein said trench isolation element has a depth in a range of about 100 nm to about 50 microns.”

337. This limitation is obvious based on Hwang in view of Roy.

338. As discussed above regarding claim 64, Hwang discloses a trench isolation element. Roy discloses that “[a]ccording to an embodiment, the trench and the column have depths ranging between 1 and 10 μ m, the conductive material in the trench and in the column is polysilicon, and the material forming the insulated walls of the column and of the trench is selected from the group comprising silicon oxide, silicon nitride, silicon oxynitride, or is formed of a multiple-layer stack of these materials.” Roy [0020].

339. It would have been obvious to combine Hwang and Roy, with a reasonable expectation of success, as discussed in Section VII.D.2 above.

340. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein said trench isolation element has a depth in a range of about 100 nm to 50 microns*.

6. Claim 66: “The imager device of claim 65, wherein said trench isolation element has a width in a range of about 100 nm to about 10 microns.”

341. This limitation is obvious based on Hwang in view of Roy.

342. As discussed above regarding claim 65, Hwang discloses a trench isolation element. Roy discloses that “[t]rench 31/45 and column 33 may have a

width of approximately 0.2 μm and be separated, at the level of the interruption area of trench 31, by a distance approximately equal to 0.2 μm ,” i.e., 200 nm. Roy [0057].

343. It would have been obvious to combine Hwang and Roy, with a reasonable expectation of success, as discussed in Section VII.D.2 above.

344. Accordingly, it would have been obvious to a POSITA to make an imager device *wherein said trench isolation element has a width in a range of about 100 nm to 10 microns.*

7. Claim 71: “The imager device of claim 70, wherein said trench isolation element has a depth in a range of about 100 nm to about 50 microns.”

345. This limitation is obvious based on Hwang in view of Roy.

346. See discussion of claim 65.

8. Claim 72: “The imager device of claim 71, wherein said trench isolation element has a width in a range of about 100 nm to about 10 microns.”

347. This limitation is obvious based on Hwang in view of Roy.

348. See discussion of claim 66.

VIII. CONCLUSION

349. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false

Case No. IPR2024-00163

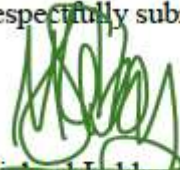
U.S. Patent No. 10,224,359

Declaration of Michael Lebby

statements and the like so made are punishable by fine or imprisonment, or both,
under Section 1001 of Title 18 of the United States Code.

Executed on November 29, 2024

Respectfully submitted,



Michael Lebby