UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.

Before The Honorable Bryan F. Moore
Administrative Law Judge

In the Matter of	
CERTAIN SENSORS WITH PIXELS AND PRODUCTS CONTAINING THE SAME	**Investigation No. 337-TA-1403**

WITNESS STATEMENT OF DR. DEAN NEIKIRK

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I. Introduction

Q1 Please state your name for the record.

A1 Dean Neikirk.

Q2 What is your role in this Investigation?

A2 I am an expert witness for Samsung Electronics, Co., Ltd.; Samsung Electronics America, Inc.; and Samsung Semiconductor, Inc. ("Samsung"). Specifically, Samsung has asked me to evaluate, and offer opinions on certain issues related to asserted claims in U.S. Patent Nos. 11,721,714 (the "'714 Patent"); 9,064,764 (the "'764 Patent"); 9,905,599 (the "'599 Patent"); and 10,224,359 (the "'359 Patent") (the "Light Trapping Patents"), including invalidity of certain claims of the Light Trapping Patents and whether certain Samsung or SiOnyx sensors and products containing those sensors practice certain claims of the Light Trapping Patents.

Q3 Please turn to JX-0011, JX-0013, JX-0014, and JX-0015. Do you recognize these documents?

A3 Yes. These are the '359, '714, '764, and '599 patents, respectively.

Q4 Are you being compensated for your work on this Investigation?

A4 I am being compensated at an hourly rate of $800. My compensation does not depend on the outcome of this Investigation.

Q5 Where are you currently employed?

A5 I am an Emeritus Professor in the Department of Electrical and Computer Engineering, at the Cockrell School of Engineering of The University of Texas at Austin, holding the Emeritus Cullen Trust for Higher Education Professorship in Engineering.

Q6 Please turn to RX-0544 (Neikirk C.V.). Do you recognize RX-0544?

A6 Yes. It is a copy of my curriculum vitae, which summarizes my education, professional background, and qualifications.

Q7 Please briefly describe your education, starting with where you attended college.

A7 I received a B.S. degree (1979) in physics from Oklahoma State University, and an M.S. degree (1981) and Ph.D. degree (1984) in applied physics from the California Institute of Technology.

Q8 Please summarize your academic research.

A8 My research over the last forty years has concentrated heavily in the areas of electromagnetics, microwave engineering, microelectronics, semiconductor devices, IC fabrication, and new sensors, including infrared and optical devices for use in multispectral

imaging systems. This research work has been funded by many agencies, focusing on the fabrication and modeling of semiconductor devices, electromagnetic devices and detectors, chemical sensors, temperature sensors, proximity sensors, and pressure sensors, as well as research on the high frequency properties of transmission lines, RF devices, and infrared to terahertz detectors for use in focal plane imaging arrays. My research related to the development of new chemical sensors (an "electronic taste" sensor) was selected for a commercialization venture between The University of Texas and two outside start-up companies.

For 37 years, I conducted research with students and research scientists in the Microelectromagnetics Research Group in the Microelectronics Research Center at The University of Texas at Austin. For over ten years, I also served as the Graduate Advisor of the Department of Electrical and Computer Engineering at the University of Texas at Austin, as well as serving for over five years as an Associate Chairman of the Electrical and Computer Engineering Department at The University of Texas at Austin. I also served as Associate Dean of Graduate Studies from 2014 to 2021.

Q9 Have you undertaken any other academic initiatives?

A9 In 1985, I established the Microelectronics Fabrication Teaching Laboratory at The University of Texas at Austin, which continues to this day to provide undergraduate and graduate students with hands-on experience in IC fabrication. I have taught many courses in integrated-circuit fabrication, microwave devices, IC packaging, electromagnetics, computer aided design methods for circuit simulation, sensors of all sorts, and micro-electromechanical systems.

In recognition of my research and classroom teaching accomplishments, I received the 1984-85 Engineering Foundation Faculty Award from the University of Texas at Austin Engineering Foundation Advisory Council, the 1985-90 General Motors Foundation Centennial Teaching Fellowship, the 1987 Award for Outstanding Engineering Teaching by an Assistant Professor, the 1990-1992 Temple Foundation Endowed Faculty Fellowship, the 1997 College of Engineering Award for Outstanding Teaching in the Department of Electrical and Computer Engineering, the 2003 Department of Electrical and Computer Engineering Gordon T. Lepley IV Endowed Memorial Teaching Award, and the 2007 Lockheed Martin Aeronautics Company Award for Excellence in Engineering Teaching.

Q10 What types of courses did you teach at the University of Texas?

A10 Over the years, I have taught a variety of electrical engineering courses. These include Integrated Circuit Fabrication, VLSI Fabrication Techniques, Ultra Large Scale Integrated Circuit Fabrication Techniques, Integrated Circuit Nanomanufacturing Techniques, Electromagnetics in Packaging, Simulation Methods in CAD/VLSI, Micro-Electromechanical Systems, Electromagnetic Engineering, and Microwave and Radio Frequency Engineering. I have also taught several continuing education courses in these fields.

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Q11 Have you been involved with any technical societies or journals?

A11 Yes. I am currently a Life Senior Member of the IEEE. From March 1991 to October 1994, I served as an Associate Editor for the IEEE publication called "IEEE Transactions on Education." I also served as a member of the Editorial Board on the IEEE Transactions on Microwave Theory and Techniques in the 1990-2000 timeframe.

I have also devoted a significant portion of my time at the University of Texas to contributing to various technical journals and other publications. My work has been included in 95 archival journal publications, 165 referenced conference proceedings, and 24 published abstracts. I have also contributed to book chapters and technical reports relating to various electrical engineering topics. My publications have addressed technologies such as chemical sensors, integrated circuits for antenna arrays, determining conductor loss in transmission lines, optical and electromagnetic devices for infrared detection, multilayer interconnection lines for high-speed digital integrated circuits, RF oscillator circuits, memory-switching double-barrier quantum-well diodes circuits, RF and infrared detection circuits, and other topics related to sensors and optical systems.

Q12 Are you a named inventor on any patents?

A12 Through my work on sensors, electronic systems and innovations in other related fields, I have been named an inventor on 17 U.S. patents. These are summarized in my curriculum vitae.

Q13 To what do your patents generally relate?

A13 Many of my patents are related to sensor arrays used for chemical testing, most using devices based on optical interactions. These include, for example, U.S. Patent 6,589,779: "General signaling protocol for chemical receptors in immobilized matrices," U.S. Patent 6,602,702: "Detection system based on an analyte reactive particle," U.S. Patent 7,316,899, 'Portable sensor array system," and U.S. Patent 8,105,849, "Integration of fluids and reagents into self-contained cartridges containing sensor elements." As another example, U.S. Patent No. 9,291,586, titled "Passive Wireless Self-Resonant Sensor," relates to a sensor for detecting materials, including a substrate, a passivation layer formed on the substrate, a high surface area material disposed on the passivation layer, and a self-resonant structure that includes a planar spiral inductor and a plurality of planar interdigitated capacitor electrodes disposed within the passivation layer.

Samsung offers Dr. Neikirk as an expert in the area of electrical engineering and physics including, but not limited to, optoelectronics and standard semiconductor manufacturing processes.

II. Summary of Opinions

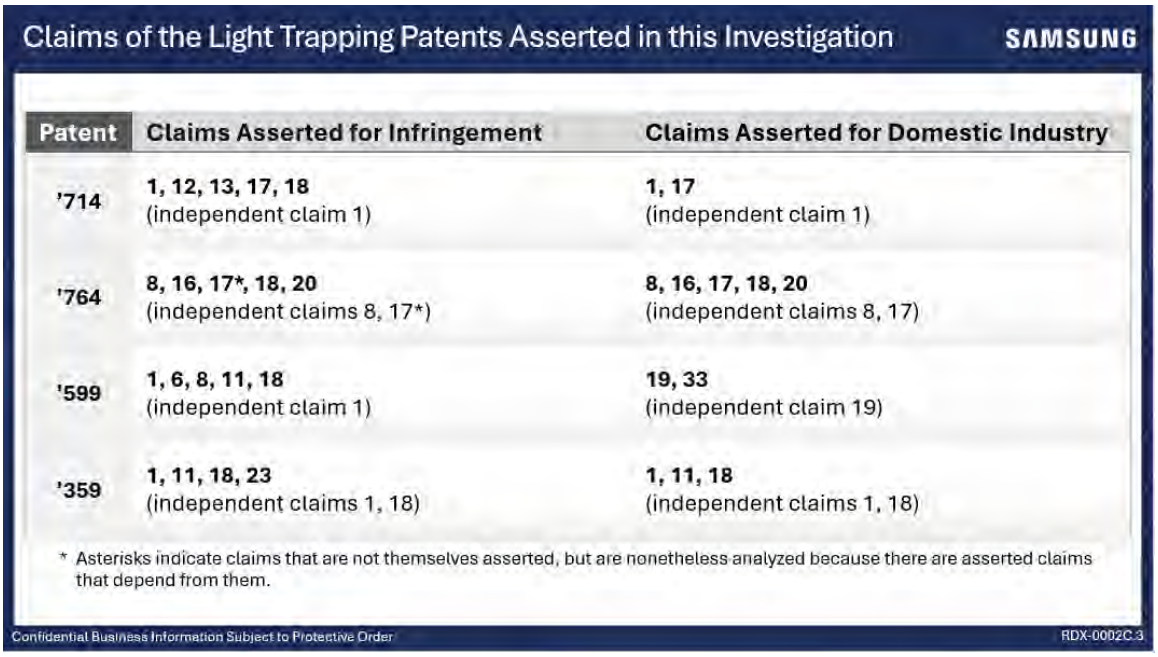
Q14 Please turn to RDX-0002C. Do you recognize RDX-0002C?

A14 Yes. RDX-0002C is a set of demonstratives to assist my testimony.

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Q15 Are you familiar with what claims of the Light Trapping Patents are asserted in this investigation?

A15 Yes. I understand that SiOnyx is asserting claims 1, 12-13, 17, and 18 of the '714 patent ("'714 patent Asserted Claims"); claims 8, 16-18, and 20 of the '764 patent ("'764 patent Asserted Claims); claims 1, 6, 8, 11, 18-19, and 33 of the '599 patent ("'599 patent Asserted Claims); and claims 1, 11, 18, and 23 of the '359 patent ("'359 patent Asserted Claims). I have prepared a demonstrative, RDX-0002C.3 to summarize this understanding.



Q16 Dr. Neikirk, what opinions are you offering on issues of anticipation and obviousness?

A16 In my opinion, all of the asserted claims of the Light Trapping Patents are invalid as either anticipated or obvious. I have prepared demonstratives, RDX-0002C.4-7, to summarize my opinions.

The '714 Patent Asserted Claims Are Invalid as Anticipated or Obvious

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References	Basis	Claim(s)
Hwang-based Grounds		
• Ground 1: **Hwang**	§§ 102, 103	**1**
• Ground 2: **Hwang in view of Kasuga**	§ 103	1, **12, 13**
• Ground 3: **Hwang in view of Konno**	§ 103	1, **12, 18**
Yamada-based Grounds		
• Ground 4: **Yamada**	§§ 102, 103	**1, 12, 17**
• Ground 5: **Yamada in view of Konno**	§ 103	1, 12, 17, **18**
Haddad188-based Grounds		
• Ground 6: **Haddad188 in view of Schubert**	§ 103	**1, 12, 17, 18**
Suzunaga-based grounds		
• Ground 7: **Suzunaga**	§§ 102, 103	**1, 12, 13, 18**

* Claims not in bold are addressed in the previous ground, e.g., Hwang teaches or suggests claim 1 for the reasons explained in Ground 1, and those reasons are equally applicable to Grounds 2 and 3.

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RDX-0002C.4

The '764 Patent Asserted Claims Are Invalid as Anticipated or Obvious

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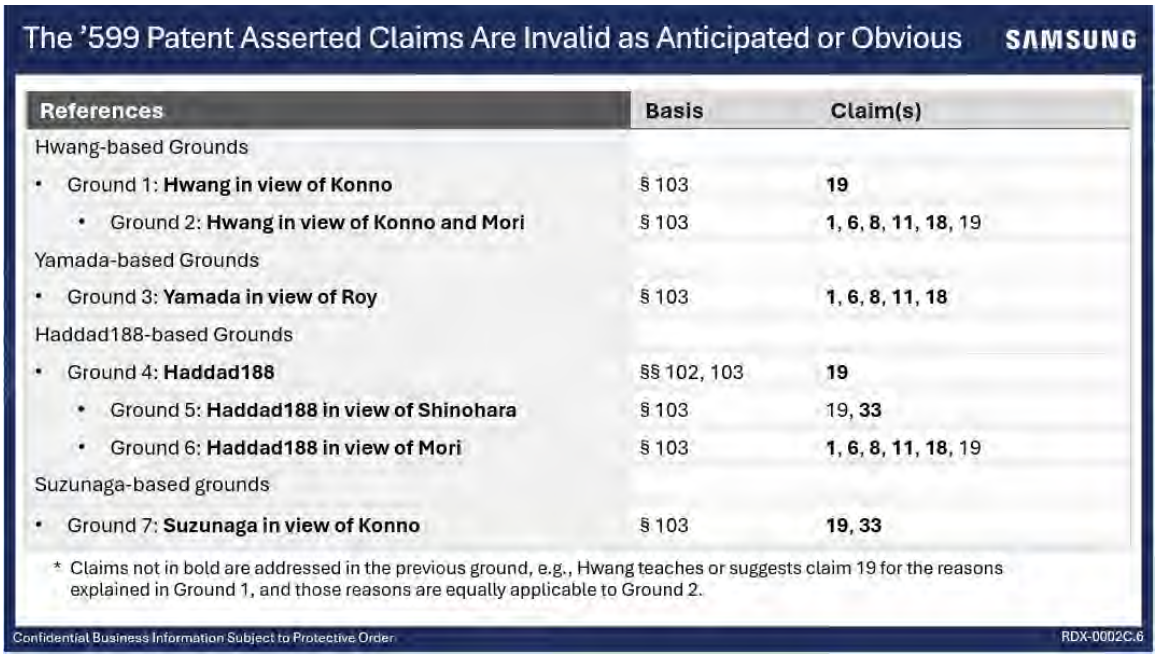
References	Basis	Claim(s)
Hwang-based Grounds		
• Ground 1: **Hwang**	§§ 102, 103	**8**
• Ground 2: **Hwang in view of Konno**	§ 103	8, **17, 18**
Yamada-based Grounds		
• Ground 3: **Yamada**	§§ 102, 103	**8, 16**
• Ground 4: **Yamada in view of Konno**	§ 103	8, 16, **17, 18, 20**
Haddad188-based Grounds		
• Ground 5: **Haddad188**	§§ 102, 103	**17, 18, 20**
• Ground 6: **Haddad188 in view of Schubert**	§ 103	**8, 16**, 17, 18, 20
Suzunaga-based grounds		
• Ground 7: **Suzunaga**	§§ 102, 103	**8, 17, 18**

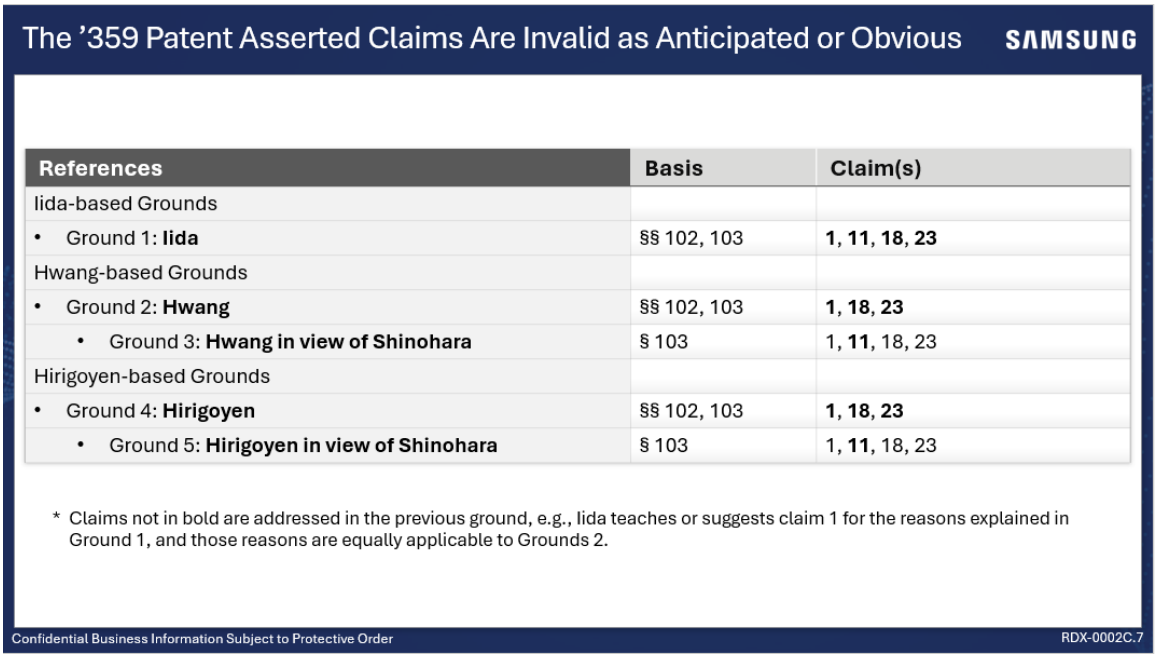
* Claims not in bold are addressed in the previous ground, e.g., Hwang teaches or suggests claim 8 for the reasons explained in Ground 1, and those reasons are equally applicable to Ground 2.

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RDX-0002C.5

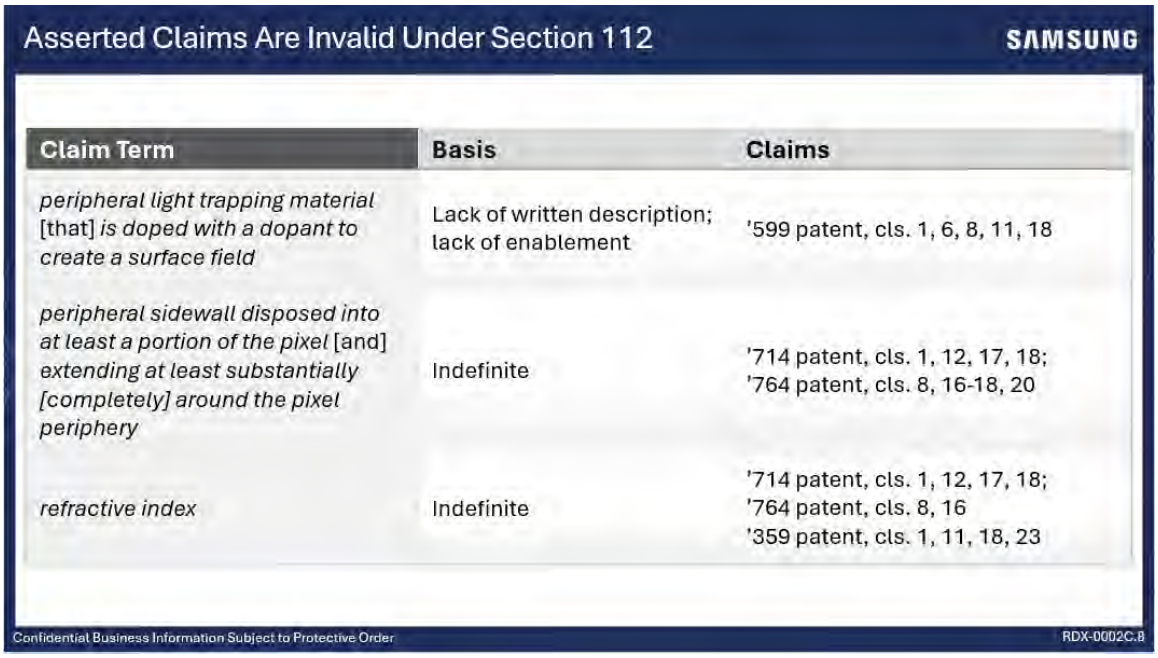
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Q17 Dr. Neikirk, what opinions are you offering regarding whether the Light Trapping Patents satisfy the requirements of Section 112?

A17 In my opinion, claims 1, 6, 8, 11, and 18 of the '599 patent are invalid for lack of written description and lack of enablement. Additionally, claims 1, 12, and 17-18 of the '714 patent; claims 8, 16-18, 20-21 and 23 of the '764 patent; and claims 1, 11, 18, and 23-24 are of the '359 patent are invalid as indefinite. I have prepared a demonstrative, RDX-0002C.8, to summarize my opinions.



III. Legal Standards

Q18 What is your understanding of the legal standard for a patent's priority date?

A18 I have been informed that a patent may claim priority to a related, earlier patent application. I understand that for patents to claim priority to a provisional application, the provisional application's written description must adequately support the claims of the patent. I have also been informed that the disclosure of the earlier-filed application must convey with reasonable clarity to persons of ordinary skill in the art ("POSITAs") that, as of the priority date sought, the applicant was in possession of the invention.

Q19 What is your understanding of the legal standard for construing patent claims?

A19 I have been informed that, in general, claim terms should be given their plain and ordinary meaning to POSITAs of the patent at the time of the invention.

I have been informed that the ALJ issued Order No. 36 Construing Certain Claim Terms in this Investigation with respect to the Light Trapping Patents. I applied the ALJ's claim constructions in my analysis.

Q20 What is your understanding of the legal standards for the burden of proof in invalidating a patent?

A20 I have been informed that each issued patent claim is presumed valid and that invalidity must be proven by clear and convincing evidence.

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Q21 What is your understanding of the legal standard for anticipation?

A21 I have been informed that a patent claim is anticipated if every claim limitation is disclosed in the same arrangement as in the claim, either expressly or inherently, in a single prior art reference. I understand that when a reference, such as a patent, "incorporates by reference" another document, the referenced document becomes effectively part of the reference.

Q22 What is your understanding of the legal standard for obviousness?

A22 I have been informed that a patent claim is obvious if the differences between the claimed invention and the prior art are such that the invention as a whole would have been obvious before the claimed invention's effective filing date to POSITAs. I understand that the factors to consider are: the prior art's scope and content; the differences between the prior art and claim; the level of ordinary skill in the art; and any evidence of secondary considerations of nonobviousness (if available).

I understand that a claim composed of several elements is not obvious merely because each of its elements was independently known in the prior art, and that obviousness should not be analyzed using the benefit of hindsight. Instead, it must be analyzed from the standpoint of what was known and understood by a POSITA at the time of the claimed invention.

I understand that claims can be obvious in view of a single prior art reference or that multiple references may be combined. To be obvious in view of a single prior art reference, there must be a reason to modify the reference to achieve the claimed invention. To be obvious in view of multiple references, a POSITA must have had a motivation to combine the references. References may also be combined with POSITAs' knowledge. I understand that the obviousness analysis may take into account the inferences and creative steps that POSITAs would employ.

Q23 What is your understanding of the legal standard to assess whether POSITAs would have been motivated to combine references?

A23 In determining whether a prior art reference could have been modified or combined with other prior art or other information known to POSITAs, I have been informed that the following principles may be considered:

> combining known elements according to known methods to yield predictable results;
>
> simple substitution of one known element for another to yield predictable results;
>
> use of known techniques to improve similar items or methods in the same way;
>
> applying known techniques to known references that are ready for improvement, to yield predictable results;

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any need or problem known in the filed and addressed by the reference can provide a reason for combining the elements in the manner claimed;

POSITAs often will be able to fit the teachings of multiple references together like a puzzle; and

the proper analysis of obviousness requires a determination of whether POSITAs would have a "reasonable expectation of success"—not "absolute predictability" of success—in achieving the claimed invention by combining prior art references.

I have been informed that a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually, as filtered through POSITA's knowledge.

I have been informed that when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. If POSITAs can implement a predictable variation and would see the benefit of doing so, that variation is likely to be obvious.

Q24 What is your understanding of the legal standard for secondary considerations of non-obviousness?

A24 I have been informed that "secondary considerations" refer to real-world considerations that may show that a claim would not have been obvious to a POSITA. I understand that such considerations may include: commercial success, copying, a long-standing problem or need, prior failures, commercial acquiescence of competitors, skepticism, and independent development, and unexpected results.

I understand that for evidence of secondary considerations to be accorded substantial weight, the patentee must establish a nexus between the evidence and the claimed invention. This ensures that any secondary considerations are due to qualities of the invention being patented rather than some extraneous factor.

Q25 What is your understanding of the legal standards for written description and enablement?

A25 I have been informed that a patent claim is invalid if the patent specification does not contain a written description of the claimed invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable POSITAs to make and use the same.

Q26 What is your understanding of the legal standard for written description?

A26 I have been informed that the purpose of the written description requirement is to ensure that the scope of the right to exclude, as set forth in the claims, does not exceed the scope of the inventor's disclosed contribution to the field. I understand that the standard is

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whether the specification reasonably conveys to POSITAs that the inventor possessed the claimed subject matter as of the patent's filing date.

I have been informed that the written description requirement does not demand any particular form of disclosure, or that the specification recite the claimed invention verbatim. But descriptions that merely render the invention obvious does not suffice.

Q27 What is your understanding of the legal standard for enablement?

A27 I have been informed that the specification must permit POSITAs to practice the full scope of the claimed invention without undue experimentation. I understand that the following factors may be considered to determine whether any experimentation would have been undue: the quantity of experimentation necessary; amount of direction or guidance presented; presence or absence of working examples; nature of the claimed invention; state of the prior art; relative skill of those in the art; predictability or unpredictability of the art; and breadth of the claims.

Q28 What is your understanding of the legal standard for indefiniteness?

A28 I have been informed that a patent claim is invalid as indefinite if it does not particularly point out and distinctly claim the subject matter which the applicant regards as his invention. I have further been informed that a patent suffers from indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, POSITAs about the invention's scope.

Q29 What is your understanding of the legal standard for noninfringement?

A29 I have been informed that a device infringes a patent claim if every element of the claim, as it has been properly construed, is present in the device, either literally or under the doctrine of equivalents. I understand, however, that SiOnyx is not relying on the doctrine of equivalents in this case. I understand that it is SiOnyx's burden to prove infringement by a preponderance of the evidence.

IV. Background

A. Technology Overview

Q30 What is the technology at issue in this Investigation?

A30 The technology at issue in this Investigation relates to image sensor pixels. Over the last two decades, the consumer market has increasingly moved to digital cameras and camcorders over traditional film devices. This is in part due to the development of advanced image sensors used to convert visual information into electrical signals, which are then processed to create digital images or videos.

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Q31 Can you provide a brief history of the developments in this field?

A31 The first image sensor technology to deliver performance practical and affordable enough to include in consumer products was the charge-coupled device sensor. Development of the CCD sensor dates to work done at Bell Labs in the late 1960s. Scientists Willard Boyle and George E. Smith used a series of MOS capacitors connected in series to pass a charge from one capacitor to the next. Boyle and Smith recognized as early as 1970 that this technology could be used in an imaging device.

Efforts to make a CCD image sensor device proceeded into the 1970s, including work done by Fairchild Semiconductor, RCA, and Kodak Research Labs. The first digital camera was created in 1975 by Steven Sasson at Eastman Kodak. It was made from parts of Kodak's Super 8 movie cameras and used a CCD sensor that shot in black and white. *See* RX-0308 (Goodrich). CCD sensors read out from the edge of the sensor, one pixel at a time, cascading the charge down from one pixel to the next each time a pixel is read. The speed at which this can be done is dictated by the current applied to the chip, which placed power demands on consumer digital cameras. Nevertheless, CCD sensors dominated the market into the 2000s.

Q32 What technology came after CCD sensors?

A32 In the 1990s, researchers turned to CMOS image sensors based initially on passive pixel architectures and later on active pixel architectures. In a passive pixel sensor, every passive pixel includes an access transistor and a photodiode. The pixels are arranged in a two-dimensional structure with an access enable wire shared through pixels in the same row and an output wire shared through the column. Each column end includes an amplifier. Passive pixel sensors have limitations such as slow readout and high noise. The addition of an amplifier to each pixel addressed these problems and resulted in the creation of the active pixel sensor. Because the CMOS process had become well-established as a stable process and was the baseline process for almost all logic and microprocessors, researchers began to build CMOS devices using passive and active pixel structures.

In 1993, Eric Fossum, from NASA's Jet Propulsion Laboratory, demonstrated a CMOS active pixel image sensor with intra-pixel charge transfer. This was further developed into an array of pixels that utilized pinned photodiodes and other circuitry. This led to commercialization of CMOS sensors that could achieve performance on par with, and later exceeding, CCD sensors. By the late 2010s, CMOS sensors had largely if not completely replaced CCD sensors in the commercial market.

Q33 At a basic level, how does a CMOS image sensor work?

A33 At the heart of a CMOS image sensor lies an array of light-sensitive pixels, each of which has a photodiode capable of detecting light. A photodiode converts incoming photons into electrons and holes (i.e., charge carriers). The quantity of charge carriers collected at each pixel determines its brightness. Photodiodes are typically fabricated by doping a semiconductor layer to create a junction, which is used for sensing light. The photodiode junction is then connected to a metallization layer that carries the electrical signal to

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external circuits. By assembling this data across all pixels, the sensor constructs an image or video corresponding to the captured scene.

An ideal image sensor would convert every incoming photon into a collected electron or hole. However, in practice, some photons and some electrons are lost during conversion. Some incident photons may be lost because they are reflected before reaching the photodiode, while others may be lost because they pass through the semiconductor layer without being absorbed. Even when photons generate charge carriers, some of those may not be collected by circuitry. Quantum efficiency is the measure of how close to ideal a given image sensor performs. Quantum efficiency is generally defined as ratio of electrons collected per photons incident on an optoelectronic device.

Q34 What is the general layout of an image sensor?

A34 In the design of image sensors, the side of the semiconductor layer where the photodiode junction and the metallization layer are located is generally referred to as the "front side," while the opposite side is known as the "backside." Image sensors can be designed to receive light from either the front side (front side illuminated, or FSI) or the backside (backside illuminated, or BSI).

FSI sensors are generally easier and less costly to manufacture, but they suffer from greater light loss because the incident light must pass through the metallization layer before reaching the photodiode junction, resulting in photon loss. This can reduce the sensor's overall efficiency and image quality, especially in low-light conditions. Conversely, BSI sensors are generally more challenging and expensive to produce but offer superior performance because the incident light directly reaches the photodiode junction without passing through the metallization layer. This design can reduce photon loss and hence improve quantum efficiency, leading to better image quality, particularly in demanding lighting environments.

Q35 Are there other designs that can reduce photon loss?

A35 To mitigate photon loss in an image sensor pixel, microstructures may be included in an image sensor to facilitate photons reaching a photodiode, as well as microstructures that reflect and scatter light within the active portion of the semiconductor layer. Pixel isolation elements, or sidewalls, and textured regions are two types of microstructures that may be used in image sensor pixels to minimize photon loss. These technologies and their implementation in image sensor pixels, as well as the general structure of CMOS image sensors were well known prior to the Light Trapping Patents and, indeed, before SiOnyx was formed.

Q36 What are pixel isolation elements?

A36 For example, pixel sidewalls are isolation structures that physically separate a pixel from its neighbor. Sidewalls can prevent photons from transmitting through one pixel into an adjacent pixel (i.e., optical isolation) and prevent charge in one pixel from migrating to an adjacent pixel (i.e., electrical isolation). Sidewalls are generally formed by creating one or more trenches in the semiconductor substrate and adding materials with various

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characteristics, depending on design goals and manufacturing considerations. Two common techniques for trench isolation are known as shallow trench isolation (STI) and deep trench isolation (DTI).

Q37 Did SiOnyx invent STI and DTI?

A37 No. Neither STI nor DTI were invented by SiOnyx. They have been known techniques since prior to 2012. *See* RX-0313 (Tournier). In fact, testimony from Drs. Vineis, Pralle, Palsule, and Carey, who I understand all to be current or former SiOnyx employees, support my opinion, as does testimony from SiOnyx's expert, Dr. Foty.

Q38 Please turn to JX-0037C (Vineis). Can you explain how Dr. Vineis's testimony supports your opinion?

A38 Yes. JX-0037C is the deposition transcript of Chris Vineis, who I understand is the Chief Technology Officer of SiOnyx. In his deposition, Dr. Vineis admitted that SiOnyx did not invent using trench isolation in an imaging device. JX-0037C, 129:17-130:20.

Q39 Please turn to JX-0038C (Pralle). Can you explain how Dr. Pralle's testimony supports your opinion?

A39 Yes. JX-0038C is the deposition transcript of Martin Pralle, who I understand is the General Manager of the Government Division of SiOnyx, which includes advanced research and development with the U.S. government, and a named inventor on the Light Trapping Patents. Dr. Pralle agreed that DTI was known in other devices prior to his work on the Light Trapping Patents. *See* JX-0038C, 242:15-243:3, 245:2-7.

Q40 Please turn to JX-0028C (Carey). Can you explain how Dr. Carey's testimony supports your opinion?

A40 Yes. JX-0028C is the deposition transcript of James Carey, who I understand was one of the founders of SiOnyx. Dr. Carey admitted in the deposition that trench isolation was already a known technique prior to SiOnyx's patents and that Dr. Carey did not understand the Light Trapping patents to be claiming to have invented STI or DTI. JX-0028C, 116:10-13, 127:17, 19.

Q41 Are you aware of others working on deep trench isolation before SiOnyx?

A41 Yes. Companies such as HTC marketed cameras with image sensors that included DTI as early as 2010.

Q42 Please turn to RX-0302 (TechInsights Blog). Do you recognize RX-0302?

A42 Yes. RX-0302 is a blog posting from TechInsights that discusses early DTI use in BSI image sensors. *See* RX-0302.1 ("The first DTI structures for back-illuminated CIS were found in 2010 in the HTC One UltraPixel camera chip fabricated by STMicroelectronics.").

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Q43 How do pixel sidewalls formed by trench isolation isolate pixels?

A43 Sidewalls as well as the backside surface of the pixel may be constructed of or have added to them reflective materials to not only physically but optically retain light within a pixel. Some materials are inherently reflective, such as certain metals, while others are reflective in combination with other materials. For example, a distributed Bragg reflector ("DBR") is a multilayer-stack of alternate high- and low- refractive index films that can function together to reflect photons. DBRs were known prior to 2012, as was the use of reflective materials on pixel sidewalls and surfaces, and were not invented by SiOnyx. *See, e.g.*, JX-0038C (Pralle), 237:6-239:20.

Q44 Were reflective pixel sidewalls known in the art before 2012?

A44 Yes. Reflective sidewalls in image sensors were known in the art prior to 2012. For example, Samsung was developing image sensors at this time that included multi-layered reflection layers in conjunction with deep trench isolation elements. U.S. Patent No. 7,675,099 to Hwang discloses aspects of these development efforts. I will discuss Hwang in more detail in connection with my specific invalidity opinions.

Q45 Are there other microstructures that mitigate photon loss in an image sensor pixel?

A45 Texturing silicon surfaces can diffuse, or scatter, light within a pixel, and were also known in the art prior to 2012, including based on the published work of SiOnyx's own founders.

Q46 Please turn to JX-0020C (Mazur). Do you recognize JX-0020C?

A46 JX-0020C is the deposition transcript of Eric Mazur, who I understand was involved in the founding of SiOnyx. According to the transcript, in 1996, Dr. Eric Mazur of Harvard University made the "serendipitous" discovery of a method of texturing silicon, which he referred to as "black silicon." *See* JX-0020C, 11:20-12:9. I understand from the transcript that Dr. Mazur described black silicon as silicon that has been heavily doped with a chalcogenide (such as sulfur) under the influence of ultra-short laser pulses. JX-0020C, 12:10-14. Dr. Mazur worked on black silicon for 7 years with Dr. Carey before the founding of SiOnyx. JX-0020C, 28:7-11.

Q47 Please turn to RX-0059C (Mazur-Hamamatsu). What is this document?

A47 RX-0059C is the deposition transcript of Eric Mazur from a previous litigation involving Hamamatsu. In the transcript, Dr. Mazur indicates that his initial black silicon process involved treating silicon with a femtosecond laser in a sulfur hexafluoride atmosphere. RX-0059C (Mazur-Hamamatsu), 44:13-45:16.

Q48 Please turn to JX-0017C (Sickler). Do you recognize JX-0017C?

A48 JX-0017C is the deposition transcript of Jason Sickler, who I understand was a former employee of SiOnyx.

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Q49 What, if anything, did Dr. Sickler say regarding the impact of the laser process on silicon?

A49 Dr. Sickler explains that the process resulted in changes in the texture, crystallinity, and structure of the target silicon. JX-0017C (Sickler), 17:9-16.

Q50 What, if anything, did Dr. Mazur say regarding the potential use of silicon treated in this manner?

A50 Dr. Mazur claims that the black silicon process increases absorptivity and extends photosensitivity further into the near-IR range. JX-0020C (Mazur), 13:3-15. Indeed, Dr. Mazur recognized that the only use for his black silicon process is to increase the sensitivity of sensors, including image sensors. JX-0020C (Mazur), 12:15-23.

Q51 Are there alternative techniques for texturing silicon?

A51 Yes. For example, an alternative technique for creating textured silicon using a reactive ion etching technique was known prior to Dr. Mazur's discovery and was also referred to by scientists as "black silicon." Dr. Carey admitted that reactive ion etching was known in the 1990s. JX-0028C (Carey), 19:2-4.

Q52 Was the black silicon process publicly disclosed?

A52 I understand that Dr. Mazur disclosed the black silicon process to administrators at Harvard University, but they initially declined to seek patent protection. *See* JX-0028C (Carey), 35:22-40:11; RX-0059C (Mazur-Hamamatsu), 46:5-14, 62:7-15. Dr. Mazur's group publicly disclosed black silicon in 1998 when they reported the first observation of conical microstructures formed on the surface of silicon following irradiation with femtosecond laser pulses in an atmosphere of sulfur hexafluoride. *See* JX-0028C (Carey), 42:1-21; RX-0059C (Mazur-Hamamatsu), 63:7-18; 71:11-16. I also understand that, in 2004, Dr. Carey subsequently addressed the black silicon laser microstructuring process in his 2004 doctoral thesis, and also considered potential applications for black silicon, including solar cells, photodetectors, L-range photodiodes, and field emission devices. *See generally* JX-0028C (Carey), 40:20-44:17.

Q53 What did Drs. Mazur and Carey do with the black silicon process?

A53 My understanding is that by 2006, Dr. Carey expressed interest in working in industry and Dr. Mazur suggested a startup that might attempt to commercialize the use of black silicon in image sensors. *See* JX-0020C (Mazur), 17:11-18:20; JX-0028C (Carey), 57:11-21. Indeed, the corporate name "SiOnyx" is in direct reference to black silicon and used the tagline "the black silicon company" to convey its value proposition (i.e., black silicon) to the marketplace. JX-0028C (Carey), 22:7-23:3, 58:22-59:6. Dr. Carey indicated in his testimony that, as a practical matter, the company strategy, at least at the outset, was to commercialize black silicon photonic devices through a purported business merit of improving existing devices with a black silicon layer. *See* JX-0028C (Carey), 63:6-64:19. One of the benefits touted by SiOnyx was that its black silicon technology (which, as discussed earlier, had been disclosed to the public) could be easily incorporated into

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existing photodetectors. JX-0028C (Carey), 64:20-65:14. As such, in 2006, SiOnyx sought to add its black silicon laser microstructuring to otherwise known image sensor designs.

Q54 How did SiOnyx incorporate the publicly disclosed black silicon process into existing photodetectors?

A54 I understand that SiOnyx expressly contacted Hamamatsu in 2006 because Hamamatsu was highly respected for making image sensors and photodetectors, including detectors used by Dr. Carey. Carey Tr., 70:14-71:12. SiOnyx knew that Hamamatsu had decades of experience making photodiodes. JX-0028C (Carey), 72:2-4. Dr. Carey testified that SiOnyx sought to collaborate with Hamamatsu because Hamamatsu already made well-regarded image sensors, and SiOnyx could integrate its black silicon as merely an improvement feature to Hamamatsu's photodetectors. *See* JX-0028C (Carey), 71:13-16; 82:3-14.

Q55 What happened with the Hamamatsu collaboration?

A55 Dr. Carey stated in his testimony that SiOnyx's collaboration with Hamamatsu ended around 2008. JX-0028C (Carey), 87:2-6. To fill the void of image sensor expertise, I understand that SiOnyx hired a group of roughly ten experienced image sensor engineers from MagnaChip Semiconductor. JX-0028C (Carey), 86:22-88:2. According to Dr. Carey, the team that was hired had a long history of image sensor design and development. JX-0028C, 87:7-88:9.

Q56 Please turn to JX-0035C (Palsule). Do you recognize JX-0035C?

A56 JX-0035C is the deposition transcript of Chintamani Palsule, who I understand to be one of the engineers who joined SiOnyx from MagnaChip. He testified that the lead engineer of the group was Dr. Homayoon Haddad, formerly Vice President of Advanced Sensor & Pixel Development at MagnaChip. *See* JX-0035C (Palsule), 21:10-22:1. Dr. Palsule also said that joining SiOnyx allowed the group to continue the work they had done at Agilent and then at MagnaChip, but with the addition of integrating the black silicon process into existing image sensors. JX-0035C (Palsule), 26:14-22.

Q57 Please turn to JX-0027C (McKee). Do you recognize RX-0027C?

A57 Yes. JX-0027C is the deposition transcript of Jeff McKee, who I understand to be another of the engineers who joined SiOnyx from MagnaChip.

Q58 What did Mr. McKee have to say regarding Dr. Haddad's qualifications?

A58 Mr. McKee described Dr. Haddad as an engineer with extensive knowledgeable and experience in image processing. JX-0027C (McKee), 124:4-14

Q59 What is your understanding of Dr. Haddad's role at SiOnyx?

A59 According to Dr. Sickler's testimony, at SiOnyx, Dr. Haddad was involved in all aspects of image sensor design given his experience in the field. *See* JX-0017C (Sickler), 54:21-

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58:4. Additionally, Dr. Haddad is the primary inventor on a prior art International Publication (WO 2011/035188) that I expect to describe further in my analysis. Dr. Haddad's '188 publication discloses many of the fundamentals of image sensor pixels, such as isolation elements, surfaces comprising reflective materials, textured regions, and doping.

B. Light Trapping Patents Overview

1. Patent Background

Q60 Please turn to RX-0090 ('275 Provisional). Do you recognize RX-0090?

A60 Yes, RX-0090 is U.S. Provisional Patent Application No. 61/614,275. The '275 Provisional App. was filed on March 22, 2012. The '764 patent issued from Application No. 13/841,120, which is a non-provisional application claiming priority to the '275 Provisional App., on June 23, 2015. The '599 patent issued from Application No. 14/747,875, which is a continuation of the '120 Application, on February 27, 2018. The '359 patent issued from Application No. 15/216,244, which is a continuation of the '875 Application, on March 5, 2019. Application No. 16/290,740 is a continuation of the '244 Application. The '714 patent issued from Application No. 17/214,333, which is a continuation of the '740 Application, on August 8, 2023.

Q61 You referenced the Light Trapping Patents earlier, to what do they relate?

A61 The Light Trapping Patents relate to image sensor pixels and elements for trapping light within such pixels. '714 patent, 6:16-20.[1] The specification explains that reduced pixel size tends to increase electrical and optical crosstalk between adjacent pixels and decrease image signal-to-noise. '714 patent, 1:27-31. The patents purportedly disclose semiconductor devices with "enhanced light detection properties." '714 patent, 6:13-16.

Q62 What is your understanding of the disclosed semiconductor devices?

A62 In attempting to address challenges of reduced pixel size, the specification refers to "light trapping elements" that can "isolate neighboring pixels in an image sensor." '714 patent, 6:18-20. Such isolation elements can be configured "to optically and/or electrically isolate neighboring pixels from one another in addition to trapping light within the pixel." '714 patent, 6:20-22. The terms "trench isolation features" and "sidewalls" are also used in reference to isolation elements. '714 patent, 7:42-43. According to the specification, a light sensitive pixel may include "a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery." '714 patent, 1:43-48.

[1] As the Light Trapping Patents share a common written description, I refer to the '714 patent but understand that equivalent citations are present in all the Light Trapping Patents. Relatedly, my discussion here is directed to the Light Trapping Patents as a family.

Q63 Do the patents provide other details about the isolation elements?

A63 The specification broadly asserts that a "variety of reflective materials can be utilized in constructing the isolation features in order to provide optical isolation, light trapping, and/or electrical isolation." '714 patent, 7:64-8:1. Examples of such reflective materials include a Bragg reflector or a metal reflector. '714 patent, 8:1-3. A metal reflector may be made of materials such as "silver, aluminum, gold, platinum, reflective metal nitrides, reflective metal oxides, and the like." '714 patent, 8:7-9.

Q64 How might these materials be used?

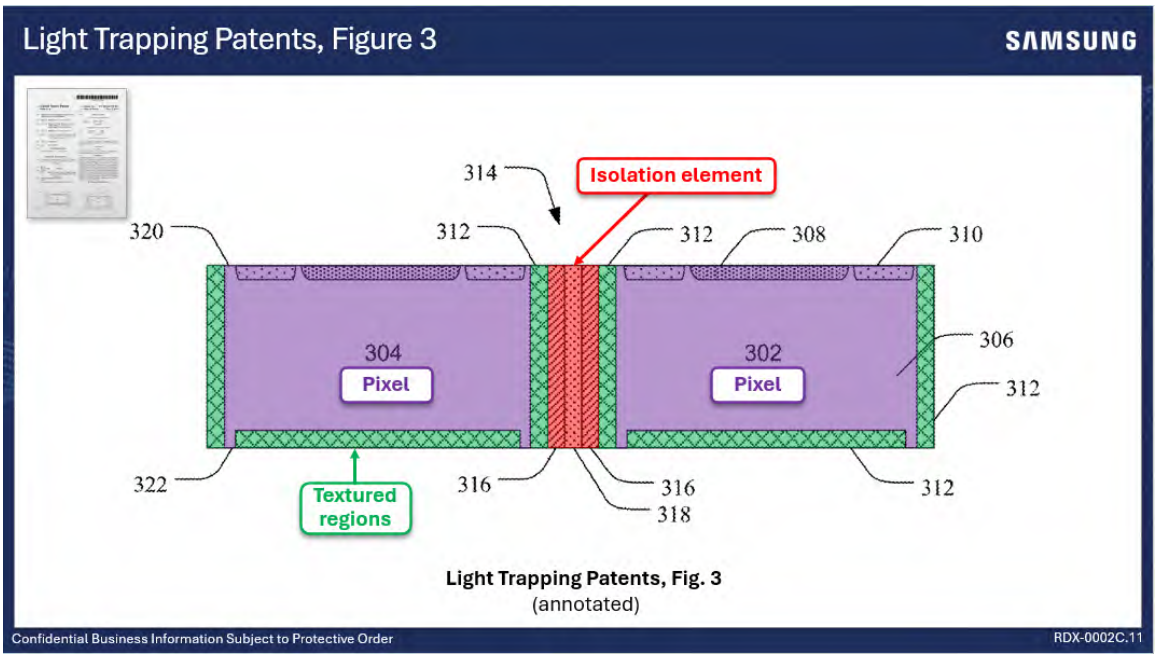
A64 The specification explains that the pixel may include a light trapping material on the backside surface or peripheral sidewall. '714 patent, 1:51-54 ("[A] backside light trapping material substantially covering the backside surface and a peripheral light trapping material substantially covering the peripheral sidewall."). Light that contacts the backside light trapping material or peripheral light trapping material is reflected toward the pixel. '714 patent, 1:54-57; 12:26-31 ("[L]ight entering the pixel that is not absorbed will interact with and be reflected internally."). Due to these internal reflections, light is "effectively maintained inside the pixel until it is absorbed." '714 patent, 12:31-32.

Q65 You referenced isolation elements; do the patents describe how they care constructed?

A65 Yes. The isolation element can be constructed with at least two layers of material having a lower refractive index as compared to the material of a third layer disposed between those two layers. '714 patent, 8:36-40. Such a construct acts as a Bragg reflector. '714 patent, 8:35-36. The specification states that a large index of refraction "mismatch" can result in "total reflection at the trench side walls." '714 patent, 9:26-28. The pixel design discussed in the specification can also include a "textured region." '714 patent, 6:45-47, 15:27-30 ("[A] textured region typically has a textured surface that increases the surface area and increases the probability of radiation absorption.").

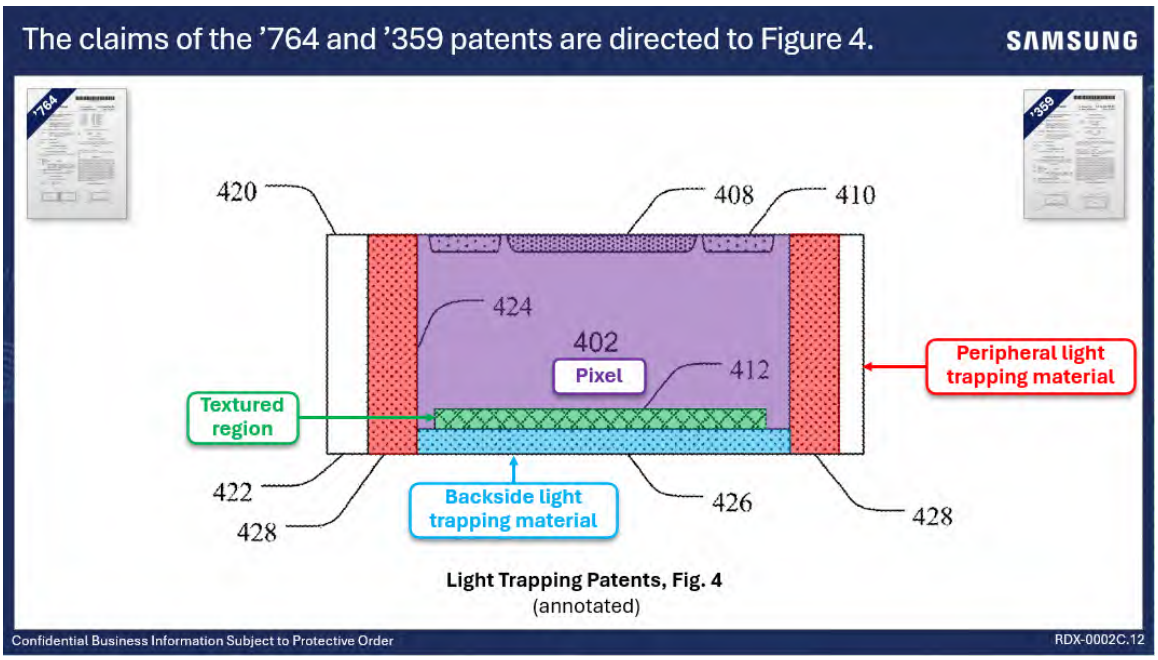
Q66 Does the specification provide an example of this arrangement?

A66 Yes. RDX-0002C.11 depicts Figure 3, an example of a disclosed light trapping pixel. Figure 3 is a cross-sectional view of multiple image sensor pixels in accordance with one embodiment discussed in the specification. '714 patent, 3:37-39.



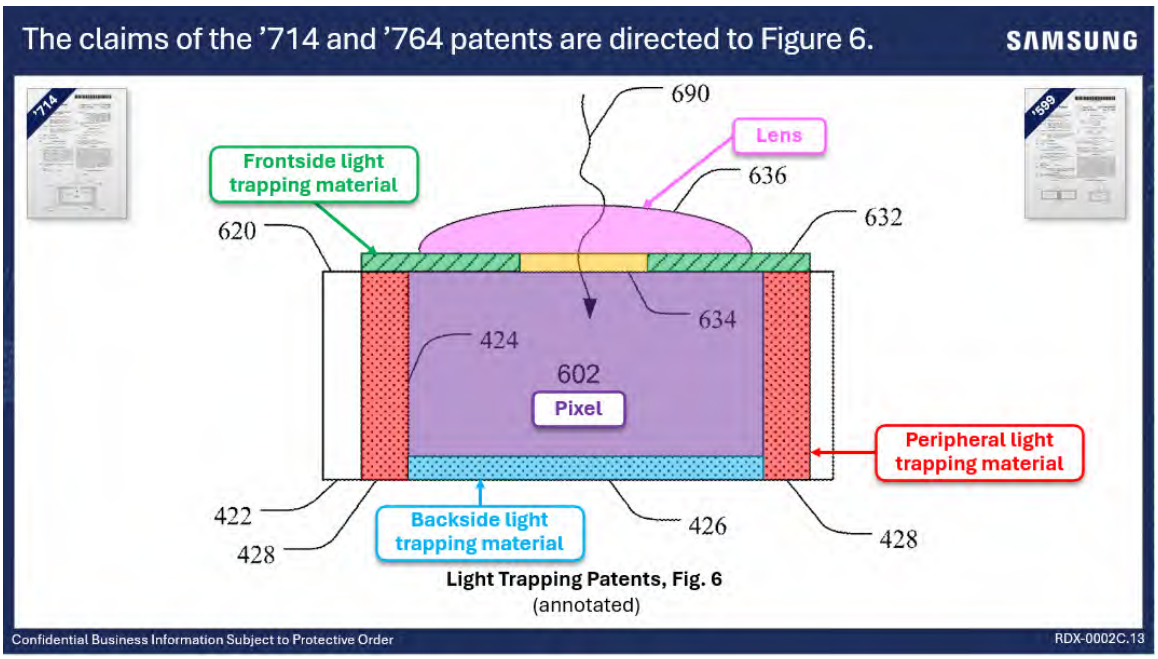
Q67 Does the specification provide another example of this arrangement?

A67 Yes. RDX-0002C.12 depicts Figure 4 from the specification. Figure 4 is a further cross-sectional view of a light trapping pixel discussed in the patent. '714 patent, 3:40-42. I understand that during prosecution of the '764 and '359 patents, the applicants stated that the claims of the '764 and '359 patents are directed towards the embodiment of Figure 4. JX-0014.417 ('764 FH) ("elect[ed] species 4, embodiment of FIG. 4"); JX-0006.1696 ('359 FH). Among other things, Figure 4 differs from Figure 3 above in that is depicts one pixel (rather than two) and in that it depicts "backside light trapping material 426." '714 patent, 11:22-24.



Q68 Does the specification provide any other examples of this arrangement?

A68 Yes. RDX-0002C.13 depicts Figure 6 from the specification. Figure 6 is a cross-sectional view of a light trapping pixel in accordance with another embodiment discussed in the specification. '714 patent, 3:46-48. I understand that during prosecution of the '714 and '599 patents, the applicants stated that the claims of the '714 and '599 patents are directed towards the embodiment of Figure 6. *See* JX-0013.95 ('714 FH) ("Applicant elects, without traverse, claims 1-20 represented by the species of FIG. 6."); JX-0010.92 ('599 FH) ("Applicants elect the species 6 corresponding to FIG. 6").



2. Level of Ordinary Skill in the Art

Q69 What is your understanding of the level of ordinary skill in the art for the Light Trapping Patents?

A69 I understand that the ALJ, as part of his Order Construing Claim Terms, found that POSITAs for the Light Trapping Patents "would have at least a bachelor's degree in electrical engineering, materials science, or physics (or an equivalent degree) and at least two years of experience in optoelectronics. The person should have knowledge of standard semiconductor manufacturing processes. A higher level of education may substitute for a lesser amount of experience, and vice versa." Order No. 36 at 19.

Q70 Do you meet this standard?

A70 My qualifications meet the foregoing definition of a POSITA, and would have met the qualifications as of March 22, 2012, the filing date of SiOnyx's '275 Provisional App. I have applied this definition in forming my opinions in this matter.

3. Claim Construction

Q71 Have the parties disputed any claim terms in the Light Trapping Patents?

A71 Yes. I understand that Samsung and SiOnyx have disputed the construction of several terms in the claims of the Light Trapping Patents, some of which are the subject of an Order from the ALJ, and some of which remain in dispute.

a. Claim Construction Order

Q72 You referenced the ALJ's Order Construing Claim Terms; did you review the claim constructions?

A72 I reviewed the ALJ's Order Construing Claim Terms and have applied those constructions in forming my opinions. For ease of reference, I have reproduced the ALJ's constructions with respect to the Light Trapping Patents in RDX-0002C.15-17.

Claim Terms Construed by the ALJ

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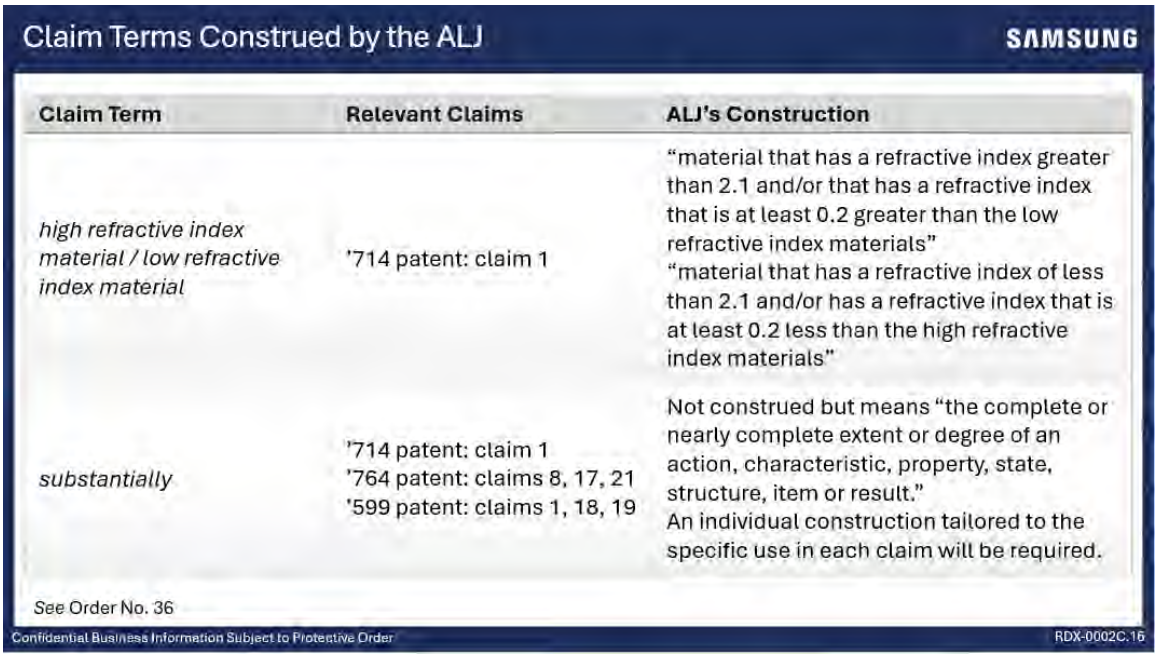
Claim Term	Relevant Claims	ALJ's Construction
sidewall	'714 patent: claim 1 '764 patent: claims 8, 17, 18, 21, 23 '599 patent: claims 1, 8, 18, 19	Plain and ordinary meaning. To the extent a construction is required: "trench wall"
a textured layer positioned to interact with light proximal to the backside surface	'764 patent: claim 21	Declined to construe at this time, will construe as part of the final Initial Determination.
light sensitive pixel / light sensitive image sensor pixels	'714 patent: claim 1 '764 patent: claims 8, 17, 21 '599 patent: claims 1. 19 '359 patent: claims 1, 18	Plain and ordinary meaning.

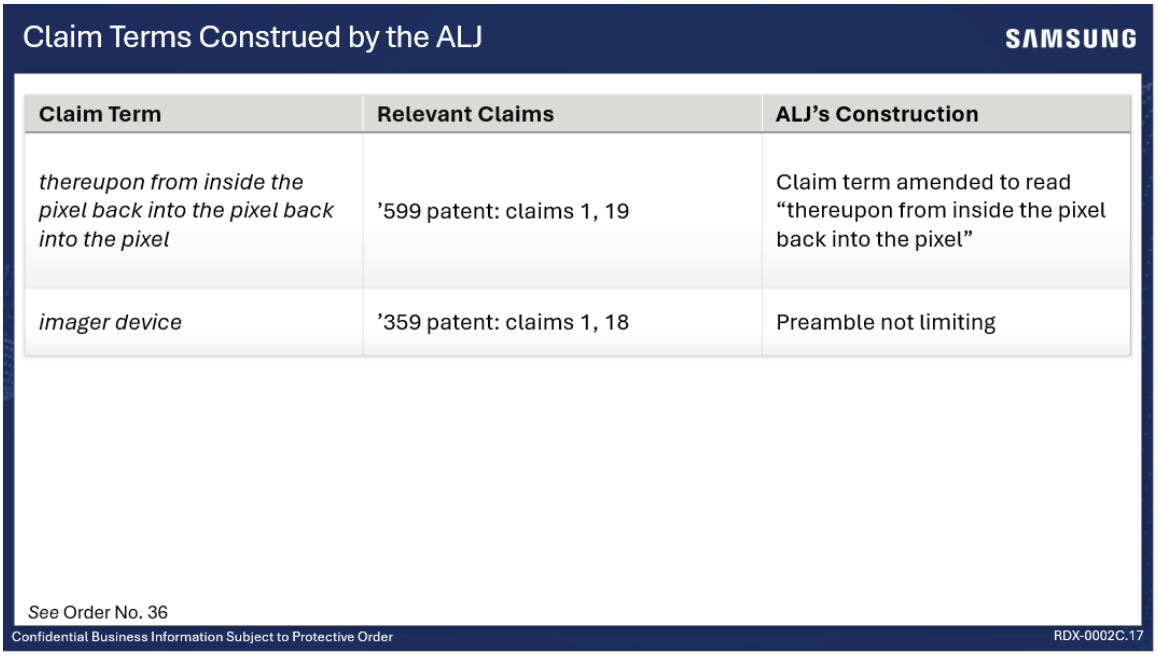
See Order No. 36

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b. Terms Remaining in Dispute

Q73 Are there any other claim terms in the Light Trapping Patents that are in dispute?

A73 I understand that the constructions of several other claim terms of the Light Trapping Patents remain disputed or otherwise unresolved. I have listed these terms in RDX-0002C.18-22, along with the constructions proposed by Samsung and SiOnyx earlier in the Investigation. RX-0894 (Samsung's Proposed Constructions); RX-0895 (SiOnyx's Proposed Constructions); RX-0223 (Claim Construction Emails); RX-0606C.1308-81 (SiOnyx's Validity Contentions).

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Claim Terms Remaining in Dispute

SAMSUNG

Claim Term	Samsung's Proposed Construction	SiOnyx's Proposed Construction
a high refractive index material sandwiched between two low refractive index materials ('714 patent: claim 1)	"a [high refractive index material] in contact with [low refractive index materials] on two opposing surfaces"	Plain and ordinary meaning: To the extent a construction is required: "a first material between two second materials, wherein the first material has a refractive index that is either higher than 2.1 or that is at least 0.2 higher than the two second materials, and wherein two second materials can be different from one another" *"a first material between two second materials wherein the first material has a refractive index of greater than 2.1 and/or that has a refractive index that is at least 0.2 greater than the low refractive index materials and wherein the two materials can be different from one another"*

See RX-0894 (Samsung's Proposed Constructions); RX-0895 (SiOnyx's Proposed Constructions); RX-0223 (Claim Construction Email Chain)

Claim Terms Remaining in Dispute

SAMSUNG

Claim Term	Samsung's Proposed Construction	SiOnyx's Proposed Construction
a first material sandwiched between two second materials ('764 patent: claim 8)	"a first material in contact with two materials on two opposing surfaces"	Plain and ordinary meaning: To the extent a construction is required: "a first material disposed between two second materials, wherein the two second materials can be different from one another" *"a first material between two second materials, wherein the two second materials can be different from one another"*
said third layer is disposed between said first and second layers ('359 patent: claims 1, 18)	"said third layer is in contact with said first and second layers on two opposing surfaces"	"a third layer between the first and second layers, wherein the first and second layers can be different materials from one another" *"a third layer between the first and second layers, wherein the first and second layers can be different materials from one another"*

See RX-0894 (Samsung's Proposed Constructions); RX-0895 (SiOnyx's Proposed Constructions); RX-0223 (Claim Construction Email Chain)

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Claim Terms Remaining in Dispute

SAMSUNG

Claim Term	Samsung's Proposed Construction	SiOnyx's Proposed Construction
textured layer ('764 patent: claim 21)	"a layer that includes features that diffuse electromagnetic radiation, redirect electromagnetic radiation, and/or absorb electromagnetic radiation, thus increasing the quantum efficiency of the device"	"a layer that includes features that diffuse, redirect, absorb, and/or increase the effective absorption length of the device" "*textured layer*"
textured region ('599 patent: claim 21)	"a region that includes features that diffuse electromagnetic radiation, redirect electromagnetic radiation, and/or absorb electromagnetic radiation, thus increasing the quantum efficiency of the device"	"a region that includes features that diffuse, redirect, absorb, and/or increase the effective absorption length of the device" "*a region that includes features that increase the path length of incident light*"
reflective layer ('599 patent: claims 1, 19)	"a layer that reflects more light back into the pixel than it transmits"	Plain and ordinary meaning: To the extent a construction is required: "a layer that reflects"

See RX-0894 (Samsung's Proposed Constructions); RX-0895 (SiOnyx's Proposed Constructions); RX-0223 (Claim Construction Email Chain)

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RDX-0002C.20

Claim Terms Remaining in Dispute

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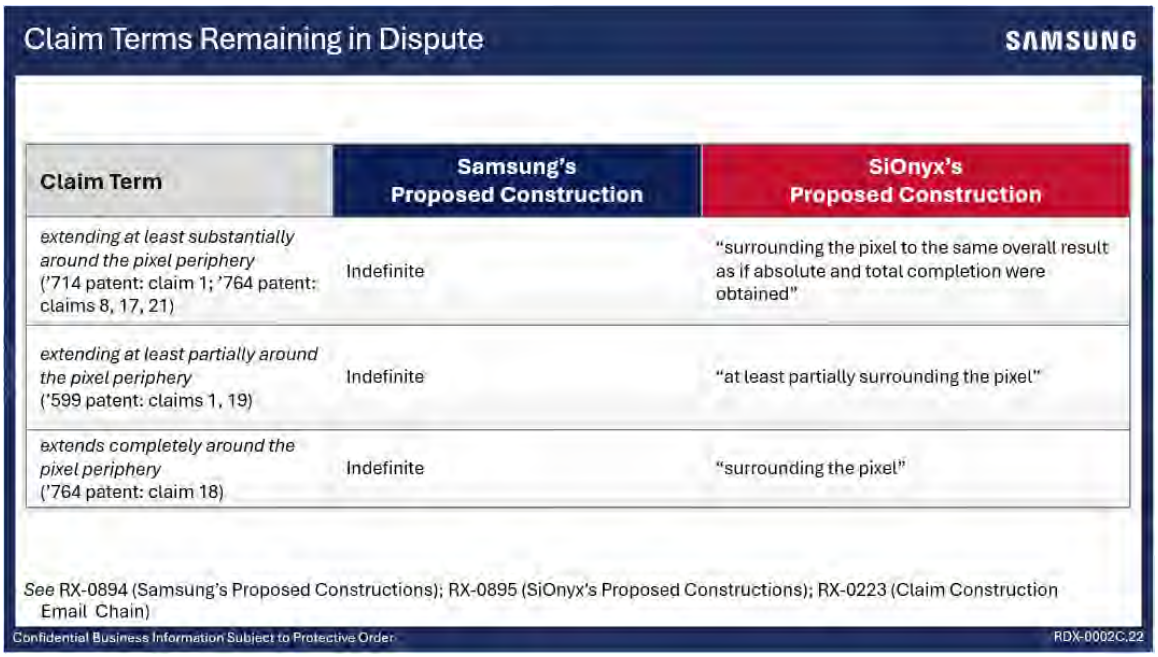
Claim Term	Samsung's Proposed Construction	SiOnyx's Proposed Construction
light trapping material ('714 patent: claims 1, 12, 13, 17, 18; '764 patent: claims 8, 16, 17, 20, 21; '599 patent: claims 1, 11, 19, 33)	"a material that reflects more light back into the pixel than it transmits"	Plain and ordinary meaning. To the extent a construction is required: "material or collection of materials that direct(s) light back into the pixel"
a peripheral sidewall disposed into at least a portion of the pixel ('714 patent: claim 1; '764 patent: claims 8, 17)	Indefinite	Plain and ordinary meaning. To the extent a construction is required: "peripheral trench wall that extends at least partially into the pixel"
sloped surface at the pixel device interface ('714 patent: claim 18; '764 patent: claim 17)	Indefinite	Plain and ordinary meaning. To the extent a construction is required: "sloped trench wall or sloped backside surface"

See RX-0894 (Samsung's Proposed Constructions); RX-0895 (SiOnyx's Proposed Constructions); RX-0223 (Claim Construction Email Chain)

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Q74 Why are some proposed constructions in italics in RDX-0002C.18-22?

A74 I have noted in italics instances in which SiOnyx appears to have proposed a construction in its December 20, 2024 Validity Contentions that differs from the construction SiOnyx proposed during claim construction.

Q75 How did you consider these disputed claim terms in forming your opinions?

A75 For these terms, I have applied the plain and ordinary meaning in forming my opinions. For purposes of my opinions as they relate to terms that remain in dispute, I have considered the parties' proposed constructions where both parties' proposed constructions were available and consistent with the plain and ordinary meaning. Where the parties' proposed constructions may have impacted my analysis, I will address each as is relevant to the analyses presented.

4. Priority Date

Q76 What is your understanding of the priority date of the Light Trapping Patents?

A76 I understand the Light Trapping Patents each claim priority to Provisional Application No. 61/614,275 ("'275 Provisional"), filed on March 22, 2012. I disagree that the '275 Provisional provides adequate written description support for all the Asserted Claims. However, for purposes of this Investigation, I will use the '275 Provisional's March 22, 2012 filing date as the priority date, as all the prior art references I rely upon predate March 22, 2012—something Dr. Mansoorian agrees with. *See* RX-0911C (Mansoorian Rpt.), ¶974.

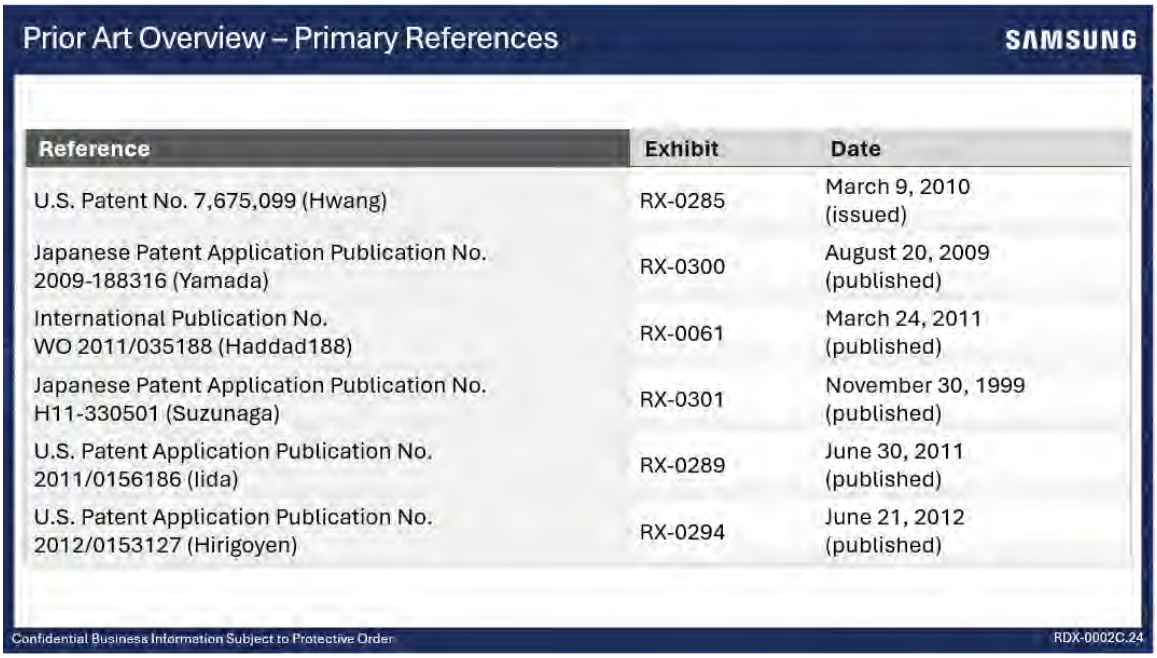
Q77 Has SiOnyx attempted to establish a priority date earlier than '275 Provisional filing date?

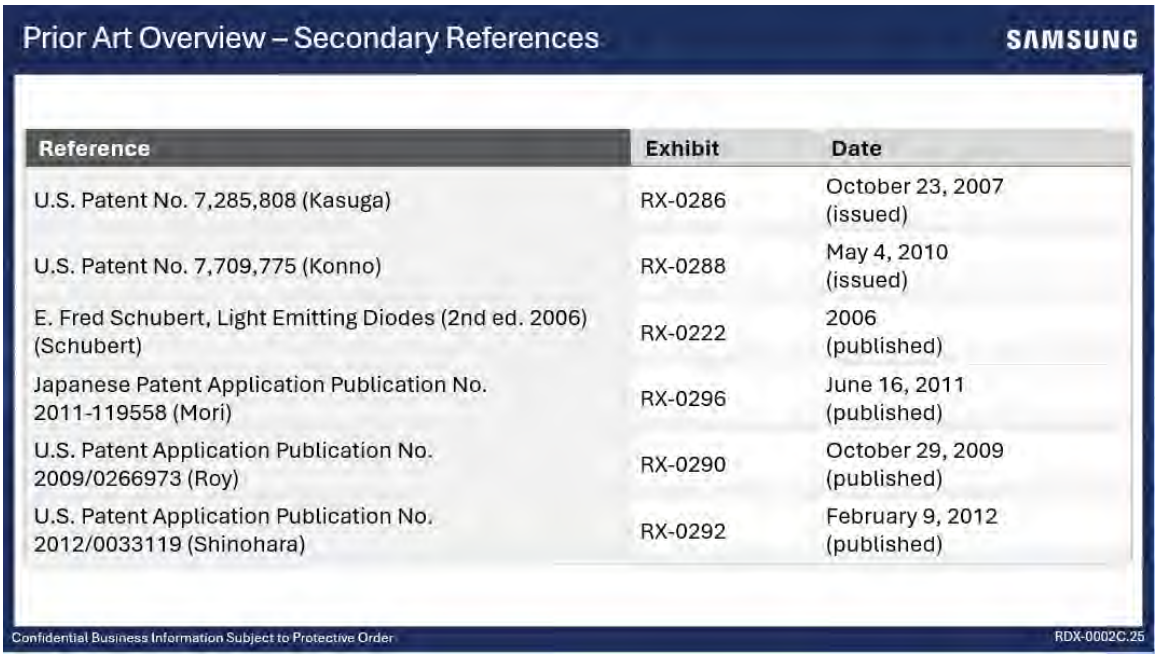
A77 No. While SiOnyx contended that the appropriate priority date is "at least as early as March 22, 2012," RX-0606C (Validity Contentions), I have not seen any assertion or analysis by SiOnyx, or its experts, that the Light Trapping Patents are entitled to an earlier priority date.

C. Prior Art Overview

Q78 Let's turn to the prior art you have relied upon. Can you please summarize the references used in your anticipation and obviousness opinions?

A78 My anticipation and obviousness opinions are based upon six primary references and six secondary references. As RDX-0002C.24-25 illustrates, all the references predate the '275 Provisional's March 22, 2012 filing date.





Additionally, I have relied upon other references to demonstrate what was known to POSITAs.

1. Primary References

a. Hwang

Q79 Please turn to RX-0899 (Hwang). Do you recognize RX-0899?

A79 Yes. RX-0899 is U.S. Patent No. 7,675,099 ("Hwang"), which is assigned to Samsung Electronics Co., Ltd. and issued on March 9, 2010. I have relied upon Hwang in forming my opinions regarding the invalidity of the Light Trapping Patents.

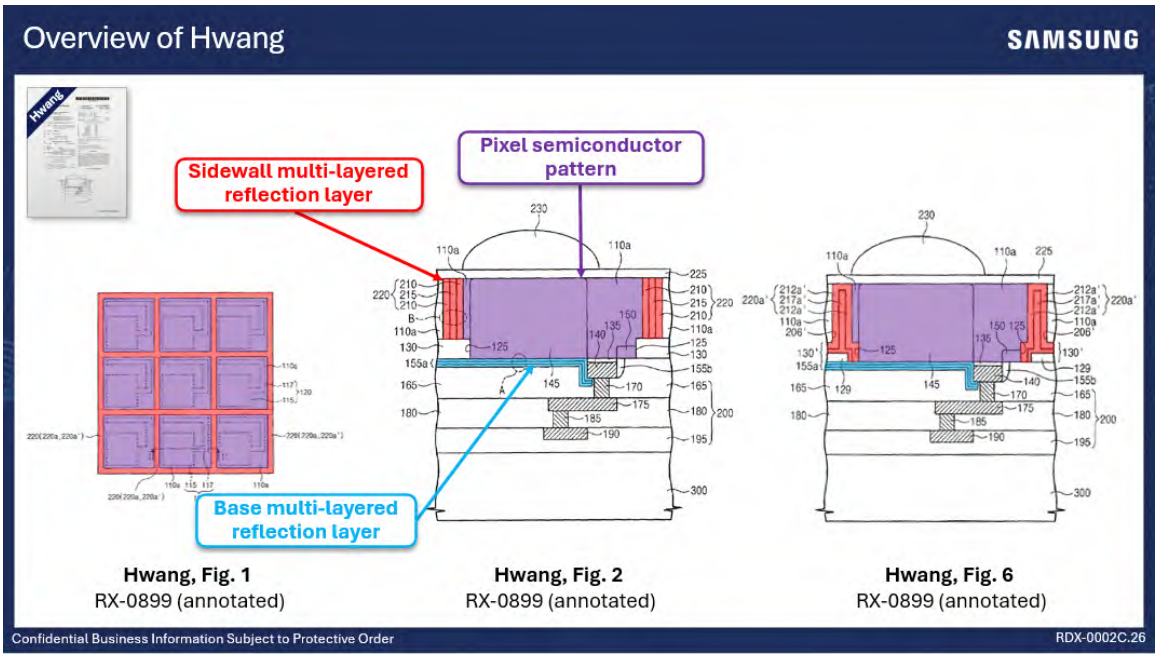
Q80 Can you briefly describe Hwang?

A80 Hwang is directed to "an image sensor with an increased spectral sensitivity," "capable of minimizing interference between neighboring pixels," and increasing detection sensitivity, by using base and sidewall multi-layered reflection layers to trap light within the pixel by enclosing it. Hwang, 1:31-67; *see also* Hwang, 8:61-9:14, 10:19-40, 15:38-48.

RDX-0002C.26 illustrates Hwang's Figure 1, a plan view of Hwang's image sensor, as well as Figures 2 and 6, which are cross-sectional views.[2]

[2] Figures 2 and 6 use differently arranged sidewall multi-layered reflection layers but are otherwise identical. Hwang, 11:57-60. Accordingly, POSITAs would recognize that teachings regarding Figure 2 (including layer 220 comprising layers 210 and 215) are pertinent to corresponding elements in Figure 6 (including layer 220*a*' comprising layers 212*a*' and 217*a*').

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To better trap light within the pixel, Hwang's base and sidewall multi-layered reflection layers comprise alternating material layers with different refractive indices, e.g., silicon and SiO_2. Hwang, 9:25-34, 10:2-5, 12:4-7.

b. Yamada

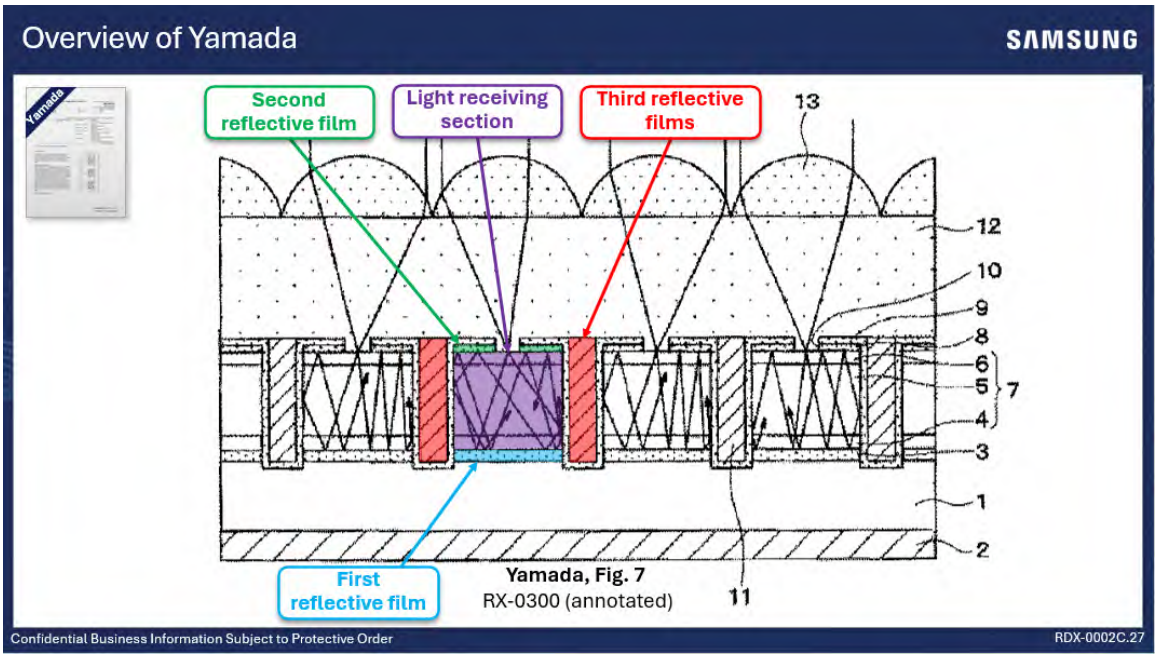
Q81 Please turn to RX-0300 (Yamada). Do you recognize RX-0300?

A81 Yes. RX-0300 is Japanese Patent Application Publication No. 2009-188316 ("Yamada"), which published on August 20, 2009. I have relied upon Yamada in forming my opinions regarding the invalidity of the '714, '764, and '599 patents.

Q82 Can you briefly describe Yamada?

A82 Yamada is directed to an "light receiving element," that uses "reflective films" to confine light within light receiving sections (e.g., PIN photodiodes)—by covering the light receiving section's backside, periphery, and frontside—which "improves the sensitivity" and prevents "optical crosstalk … between neighboring PIN photodiodes." Yamada, [0036]-[0038], as RDX-0002C.27 illustrates.[3]

[3] Figure 7 (Yamada's fifth embodiment) "share[s] the third reflecting film 11 between neighboring light receiving sections in contrast to the first embodiment," but otherwise is "the same as … the first embodiment." Yamada, [0049]-[0050].



To better trap light within the pixel, Yamada's first reflective film comprises a "semiconductor multilayer film [that] is composed of alternating layers of semiconductor films with a low refractive index and a high refractive index," Yamada, [0021], while Yamada's third reflective films are composed of "a metal" "such as [aluminum]." Yamada, [0012], [0026].

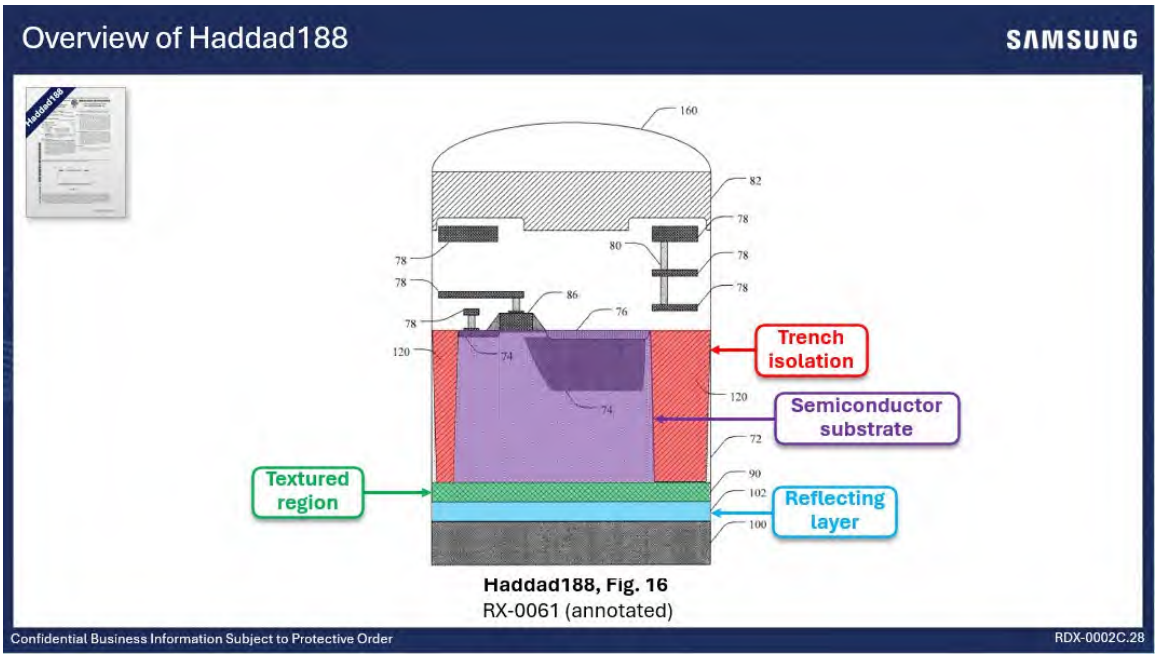
c. Haddad188

Q83 Please turn to RX-0061 (Haddad188). Do you recognize RX-0061?

A83 Yes. RX-0061 is International Publication No. WO 2011/035188 ("Haddad188"), applied for by SiOnyx and published on March 24, 2011. I have relied upon Haddad188 in forming my opinions regarding the invalidity of the Light Trapping Patents.

Q84 Can you briefly describe Haddad188?

A84 Haddad188 is directed to imaging devices with light-sensitive pixels using pixel separation structures. As RDX-0002C.28 illustrates Haddad188 discloses, among other things, "reflecting layer 102" and "trench isolation 120" that are capable of reflecting incident electromagnetic radiation to increase the effective absorption length of the device. *See* Haddad188, 24:7-9, 25:5-9. Haddad188 further discloses a "textured region 90" provided to "diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device." Haddad188, 14:29-31.



As RDX-0002C.28 illustrates, Haddad188 depicts its trench isolation 120 having a taper such that the top is wider than the bottom. Haddad188 also discloses, with respect to substantially similar embodiments, that its backside textured region can have a "nonparallel surface" to "effectively focus electromagnetic radiation into the semiconductor substrate from multiple sides." Haddad188, 24:1-15, Fig. 13.

Haddad188 also discloses, in its description of its Figure 16 embodiment, "aperture 164 formed in a metal or other reflective material layer 166" which "can increase the effectiveness of the optical cavity," Haddad188, 25:9-11, by reflecting light back into the pixel.[4]

d. Suzunaga

Q85 Please turn to RX-0301 (Suzunaga). Do you recognize RX-0301?

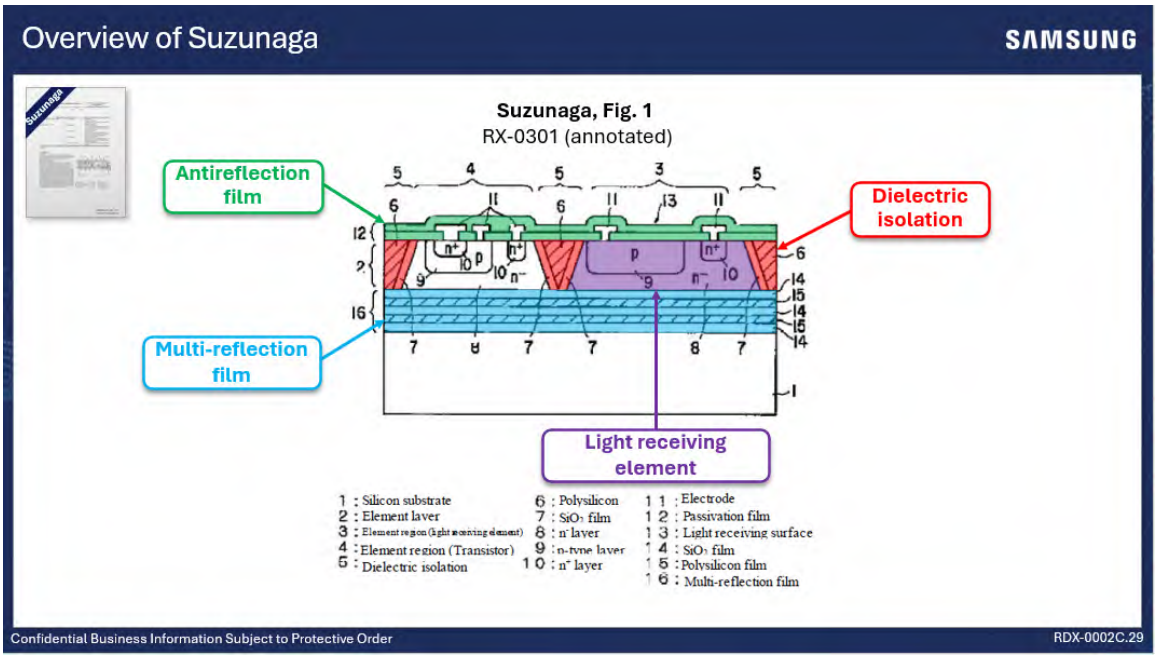
A85 Yes. RX-0301 is Japanese Patent Application Publication No. H11-330501 ("Suzunaga"), which published on November 30, 1999. I have relied upon Suzunaga in forming my opinions regarding the invalidity of the '714, '764, and '599 patents.

Q86 Can you briefly describe Suzunaga?

A86 Suzunaga is directed to "a light trapping device," i.e., a "semiconductor light receiving element … integrated using a dielectric isolation method and exhibits high light receiving

[4] Haddad188's aperture 164 and reflective material layer 166 are not depicted in Figure 16, however, Haddad188 describes those elements as part of Figure 16, Haddad188, 25:4-11, and incorporates by reference a provisional application containing a figure substantially similar to Figure 16 with those elements depicted. Haddad188, 1:4-8.

efficiency." Suzunaga, Abstract. To achieve high light receiving efficiency, Suzunaga includes "dielectric isolation region 5 … formed by embedding polysilicon 6 in a v-groove with a SiO_2 film 7 or the like interposed therebetween" Suzunaga, [0008], as well as "multi-reflection film 16" formed on the backside surface, as RDX-0002C.29 illustrates. Suzunaga also discloses a "passivation film 12" which "can also serve as an antireflection film," Suzunaga, [0010], to further trap light within Suzunaga's pixel.



Suzunaga's dielectric isolation region 5 and multi-reflection film 16—both formed of alternating layers of polysilicon and SiO_2—trap light by reflecting light back into Suzunaga's pixel. *See* Suzunaga, [0064] (dielectric isolation region 5 can be "a multi-reflection film"), [0028] ("almost 100% of the incident light … can be reflected by the multi-reflection film 16").

e. Iida

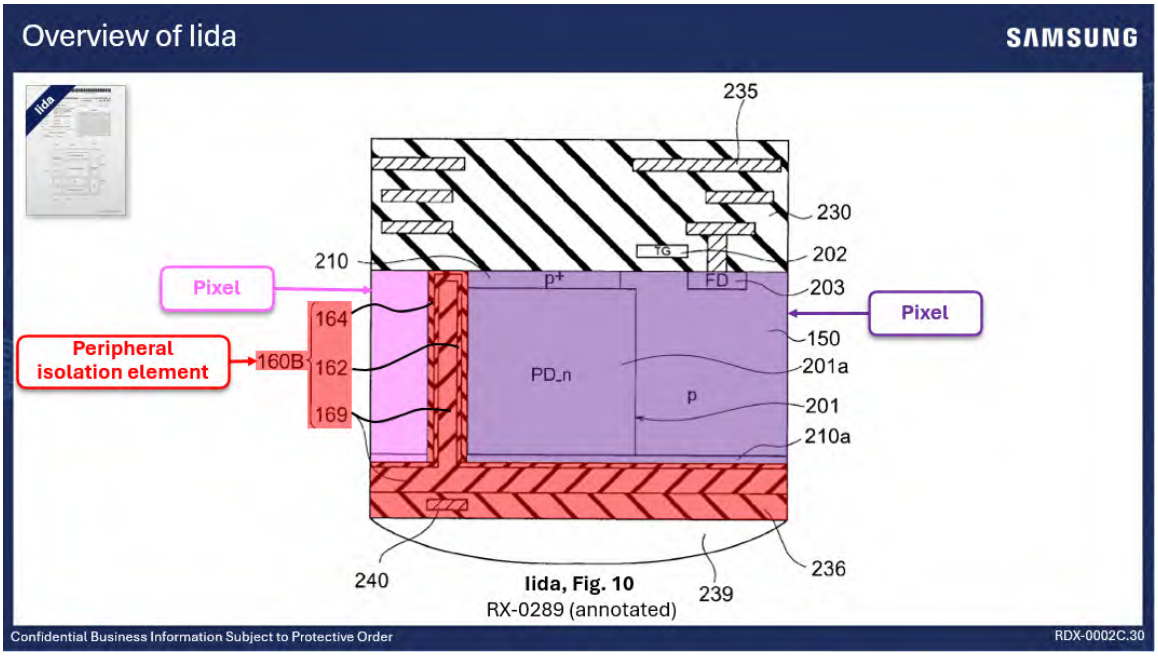
Q87 Please turn to RX-0289 (Iida). Do you recognize RX-0289?

A87 Yes. RX-0289 is U.S. Patent Application Publication No. 2011/0156186 ("Iida"), which published on June 30, 2011. I have relied upon Iida in forming my opinions regarding the invalidity of the '359 patent.

Q88 Can you briefly describe Iida?

A88 Iida is directed to light sensitive pixels in imaging devices. Iida, Abstract. Specifically, Iida addresses problems with smaller pixel sizes, including a reduction in the signal-to-noise ratio and the occurrence of electrical crosstalk between pixels. Iida, [0004]-[0005], [0010]-[0011]. Iida teaches reduction in optical crosstalk using trench separation structures "in which a material to reflect incident light is buried." Iida, [0013].

RDX-0002C.30 illustrates an exemplary embodiment, which is a cross-sectional view of an imaging device. Iida, [0035]. This embodiment includes trench-type pixel separation structure 160B, comprising silicon oxide layer 164, negative fixed charge film 162 made of hafnium oxide, and low refractive index film 169. Iida, [0099].



f. Hirigoyen

Q89 Please turn to RX-0294 (Hirigoyen). Do you recognize RX-0294?

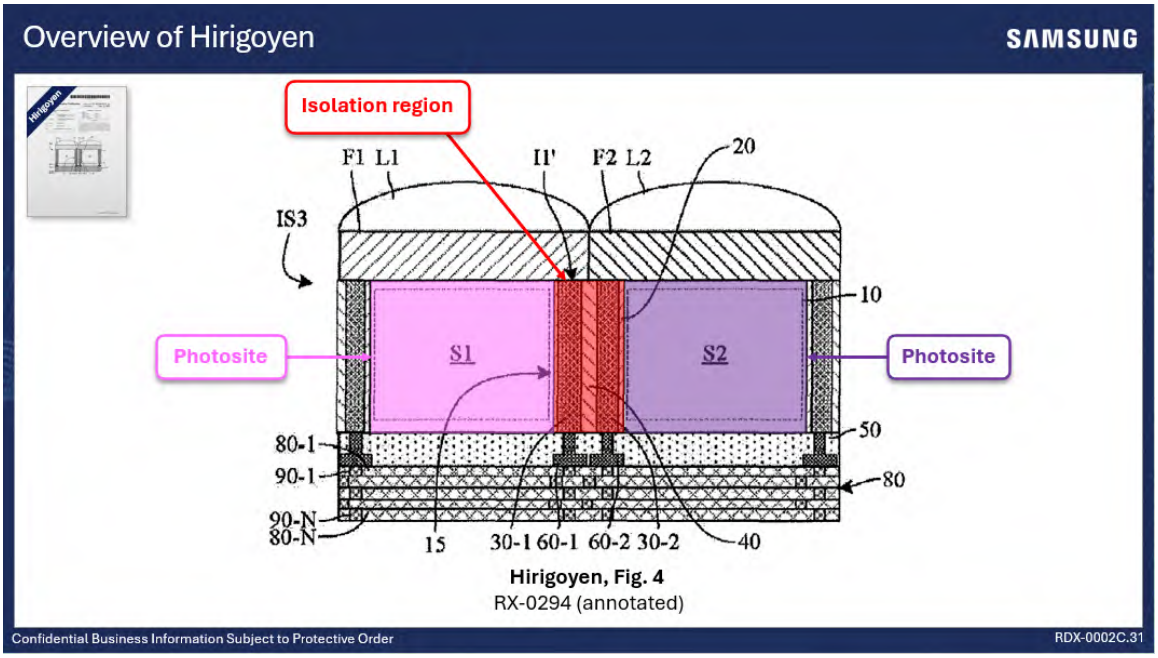
A89 Yes. RX-0294 is U.S. Patent Application Publication No. 2012/0153127 ("Hirigoyen"), which published on June 21, 2012. I have relied upon Hirigoyen in forming my opinions regarding the invalidity of the '359 patent.

Q90 Can you briefly describe Hirigoyen?

A90 Hirigoyen is directed to light-sensitive pixels (referred to as "photosites") in imaging devices that use "isolation regions" to separate adjacent pixels. Hirigoyen, Abstract. Specifically, Hirigoyen is directed to certain problems affecting the performance of such devices, such as optical and electrical crosstalk between pixels and dark current. Hirigoyen, [0005]-[0007]. Hirigoyen provides pixels and isolation regions designed to reduce these issues. Hirigoyen, [0011]-[0029], [0052], [0059]; *see* Hirigoyen, [0011] (disclosing "an image sensor including a semiconductor substrate, at least two photosites in the substrate, and an isolation region between the photosites").

RDX-0002C.31 illustrates an exemplary embodiment containing adjacent photosites (pixels) S1 and S2 in semiconductor substrate 10, as well as isolation region I1' comprising: (i) insulating liner 20 made of a dielectric material; (ii) conductive material 30-1 and 30-1 made of, e.g., polysilicon; and (iii) optical isolator 40 made of, e.g., SiO_2, all of which are

formed in trench 15. Hirigoyen, [0044]-[0048], [0057]. Also depicted are microlenses L1 and L2 and color filters F1 and F2, which transmit incident light.



2. Secondary References

a. Kasuga

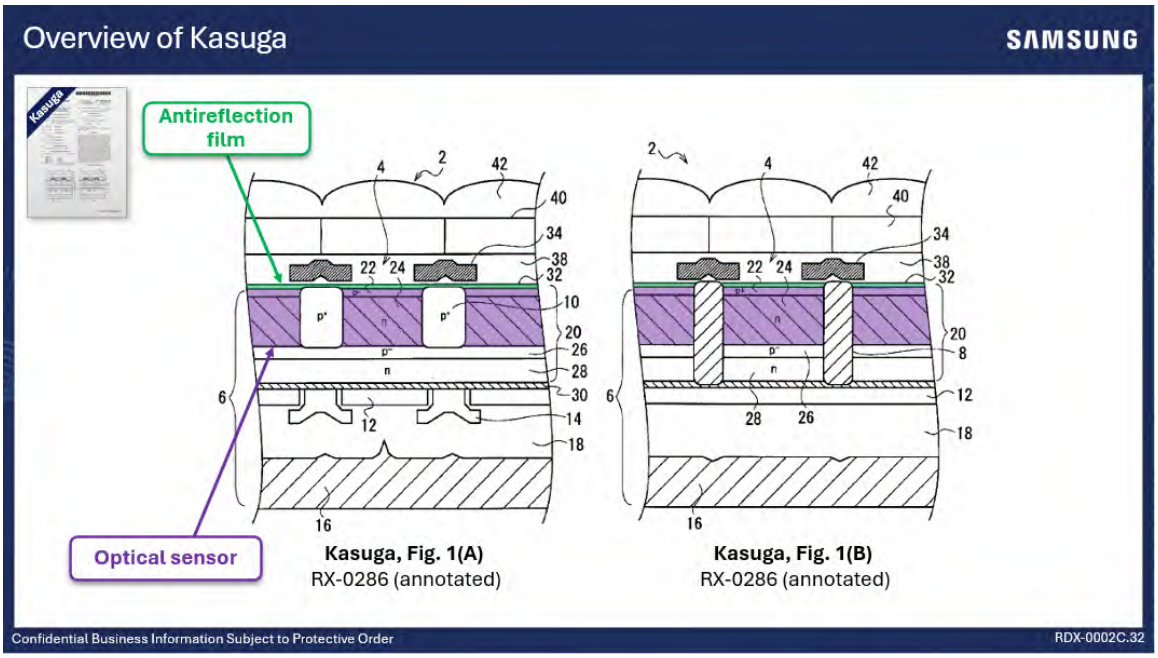
Q91 Please turn to RX-0286 (Kasuga). Do you recognize RX-0286?

A91 Yes. RX-0286 is U.S. Patent No. 7,285,808 (Kasuga), which issued on October 23, 2007. I have relied upon Kasuga in forming my opinions regarding the invalidity of the '714 patent.

Q92 Can you briefly describe Kasuga?

A92 Kasuga is directed to "a solid-state imaging device," Kasuga, 1:11-12, using reflective surfaces to increase the amount of incident light absorbed by the pixel. *See* Kasuga, 4:57-5:07, 5:38-43. As RDX-0002C.32 illustrates, Kasuga includes an "antireflection film 32 [that] is formed on the surfaces of the optical sensors 4 to prevent the reflection of light entering the optical sensors." Kasuga, 4:4-7. Kasuga teaches that antireflection film 32 creates internal reflections within the sensor—i.e., trapping light by reflecting light from within the sensor back into the sensor—which further improves the sensor's sensitivity. Kasuga, 5:23-31.[5]

[5] In Figure 1, the arrow for optical sensor 4 is pointing to 22 (p+ regions) and 24 (n-type regions) instead of a physical point on the sensor. *See* Kasuga, 3:45-48.



b. Konno

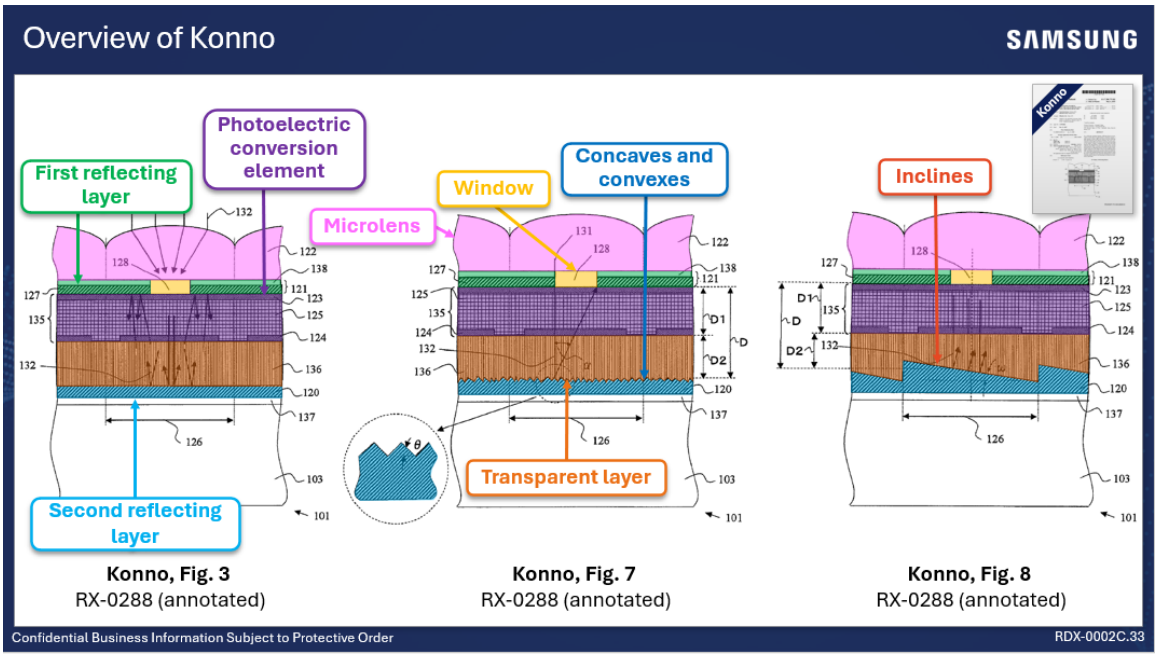
Q93 Please turn to RX-0288 (Konno). Do you recognize RX-0288?

A93 Yes. RX-0288 is U.S. Patent No. 7,709,775 ("Konno"), which issued on May 4, 2010. I have relied upon Konno in forming my opinions regarding the invalidity of the '714, '764, and '599 patents.

Q94 Can you briefly describe Konno?

A94 Konno is directed to a "solid-state imaging element" using reflective surfaces to increase the amount of incident light absorbed by the pixel to increase image quality. *See* Konno, Abstract, 2:49-55. As RDX-0002C.33 illustrates, Konno's figures 3, 7, and 8 include first and second reflecting layers 121 and 120 that "sandwich the … photoelectric conversion element 135," Konno, 8:22-25, thus "confining photons which entered into the solid-state imaging element [] between the both," Konno, 8:31-33, and improving sensitivity by allowing for "most of the photons [to] be absorbed with the photoelectric conversion films 125," Konno, 10:8-13. Konno explains that "second reflection layer 120," "can be formed by forming a thin film of a metal." Konno, 8:31-38. Konno also discloses a "microlens 122" that "concentrates photons which entered into the solid-state imaging element 110, and leads them to the light entrance window 128." Konno, 9:4-9.

Konno's Figure 7 is similar to Figure 3, but includes a transparent layer 136 which is textured by forming "concaves and convexes on [its] surface." Konno, 1:38-42. Likewise, Konno's Figure 8 is similar to Figure 3, but includes a "reflecting surface of the second reflecting layer 120 [that] inclines." Konno, 15:35-40.



Q95 Are you aware of Dr. Mansoorian's argument that POSITAs would not consider Konno when modifying other prior art references?

A95 Yes. Dr. Mansoorian opines that it would not have been obvious to combine Konno with other prior art references (e.g., Hwang, Yamada, and Suzunaga), because he contends that "Konno … is optimized for use in a 'personal authentication system.'" RX-0911C, ¶181; *see also* RX-0911C, ¶¶40, 182-83, 402, 595, 676. I disagree.

Q96 Why do you disagree with Dr. Mansoorian's opinion?

A96 First. Konno is not limited to personal authentication systems, and is instead directed to solid-state imaging elements more generally that *can* be used in personal authentication systems:

> The present invention relates to a photoelectric conversion element formed with a thin film of photoelectric absorption material, such as polysilicon film or amorphous silicon film, a solid-state imaging element or detector such as an image sensor, solar cell and X-ray flat panel sensor, and a system such as a liquid crystal display; biometric personal authentication system, photovoltaic power generation system, X-ray imaging system, and digital camera using the same.

Konno, 1:15-22; *see also* Konno, Abstract.[6] Second, neither Hwang, Yamada, Suzunaga, nor the '714, '764, and '599 patents are limited to a particular application of their light trapping devices. POSITAs would understand that Konno has numerous applications (including to but not limited to fingerprint identification), which, as Konno describes,

[6] All emphasis added unless otherwise noted.

involve the use of a light sensitive pixel and corresponding light trapping materials to convert light into electrical signals. *See* Konno, Abstract, 1:15-22.

Indeed, Dr. Mansoorian himself admits that Konno is an image sensor. *See* RX-0911C, ¶676 ("Konno discloses a monochrome image sensor for personal authentication devices.").

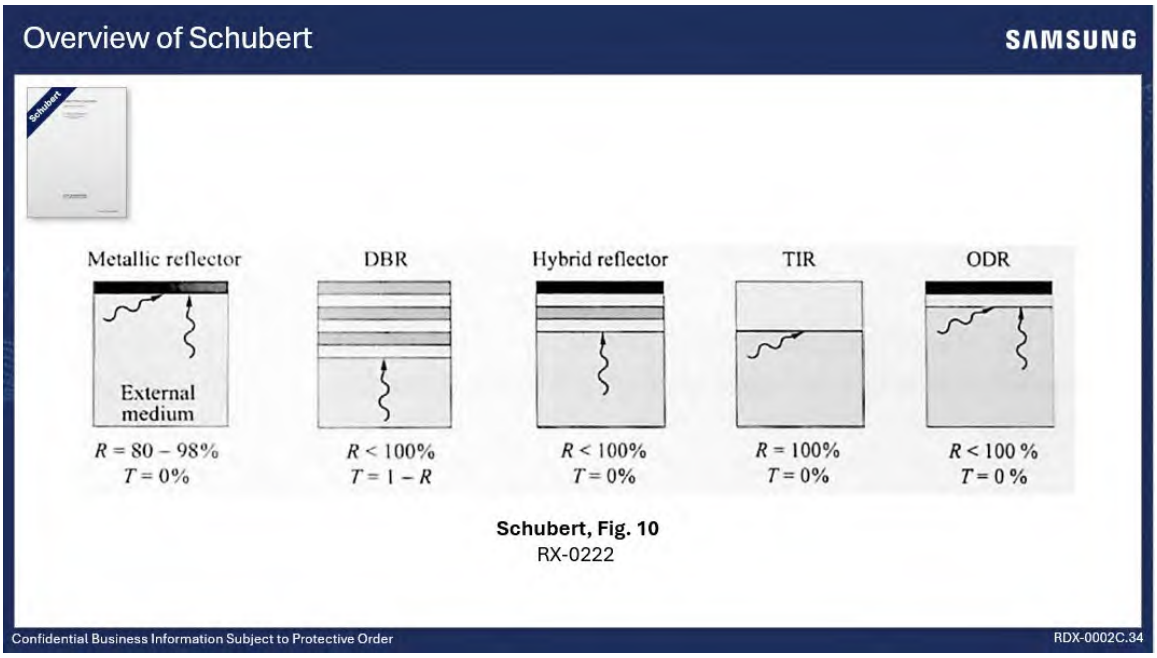
c. Schubert

Q97 Please turn to RX-0222 (Schubert). Do you recognize RX-0222?

A97 Yes. RX-0222 ("Schubert") is a chapter titled "Reflectors," from a textbook titled "Light Emitting Diodes," which was published in 2006. I have relied upon Schubert in forming my opinions regarding the invalidity of the '714, '764, and '599 patents.

Q98 Can you briefly describe Schubert?

A98 Schubert discloses the use of reflectors in optoelectronic devices. Specifically, Schubert includes a chapter titled "Reflectors" that discusses potential reflectors such as distributed Bragg reflectors ("DBR"), known to POSITAs. For example, as RDX-0002C.34 illustrates, Schubert discusses the "[d]ifferent types of reflectors" to use in optoelectronic devices, i.e., "a metallic reflector, distributed Bragg reflector (DBR), hybrid reflector, total internal reflector (TIR), and a triple-layer omni-directional reflector (ODR)." Schubert, 163.



Q99 Are you aware of Dr. Mansoorian's argument that POSITAs would not consider Schubert when modifying other prior art references?

A99 Yes. Dr. Mansoorian opines that it would not have been obvious to combine Schubert with other prior art references (e.g., Haddad188), because "Schubert is an excerpt from a

textbook on light emitting diodes (LEDs)," RX-0911C, ¶244, specifically that "Schubert's discussion of reflectors is within the context of Light Emitting Diodes, or LEDs, where reflectors function to concentrate photons generated within the LEDs for emission as a beam of light." *E.g.*, RX-0911C, ¶118. I disagree.

Q100 Why do you disagree with Dr. Mansoorian's opinion?

A100 As explained, Schubert includes a chapter titled "Reflectors" that discusses potential reflectors, such as DBRs, known to POSITAs, as well as the characteristics of an ideal reflector. POSITAs would understand the reflectors Schubert discusses are pertinent to image sensors, which include similar reflectors, such as Si/SiO_2 DBRs. *E.g.*, Hwang, Yamada, Haddad188, Suzunaga.

Moreover, POSITAs would understand that there are similarities between the structure and function of pixels in image sensors and pixels in an LED. For example, both are based on the use of a p-n junction. Indeed, the ALJ has found that the proper level of ordinary skill in the art "would have at least a bachelor's degree in electrical engineering, materials science, or physics (or an equivalent degree) and at least two years of experience in optoelectronics." Order No. 36 at 19. As SiOnyx noted, Schubert is "of interest to … graduate students in electrical engineering, applied physics, and material science." RX-0606C.1158.

d. Mori

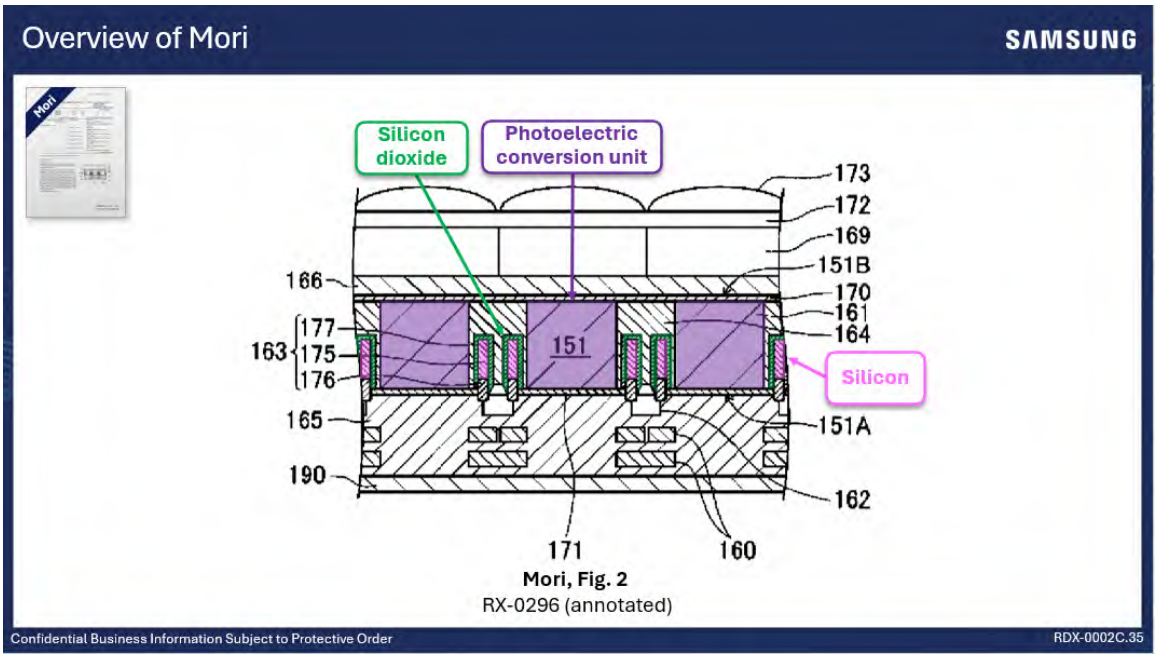
Q101 Please turn to RX-0296 (Mori). Do you recognize RX-0296?

A101 Yes. RX-0296 is Japanese Patent Application Publication No. 2011-119558 ("Mori"). I have relied upon Mori in forming my opinions regarding the invalidity of the '714, '764, and '599 patents.

Q102 Can you briefly describe Mori?

A102 Mori is directed to a "solid-state imaging device" having pixels separated by a multi-layered "partition part" 163 comprising silicon and SiO_2 layers. Mori, [0012]-[0013]. As RDX-0002C.35 illustrates, Mori's Figure 2 depicts three "[p]hotoelectric conversion units 161," (i.e., pixels), Mori, [0021]. Multi-layered partition part 163 separates the pixels and serves to reduce "color mixing [or 'crosstalk'] due to obliquely incident light." Mori, [0023], [0027]. Partition part 163 "has a silicon layer 175 formed on the light incident surface 151B side" and "a side SiO2 film 177 formed on its bottom and side surfaces." Mori, [0028], [0030].

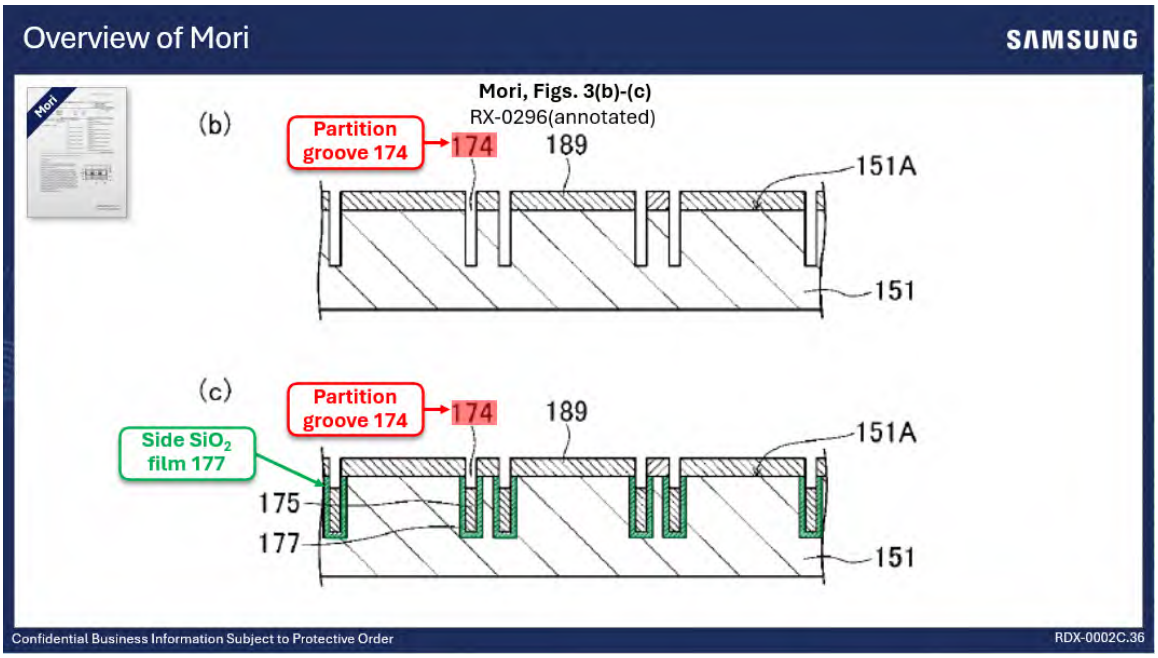
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Mori notes that existing imager devices that used light-reflective materials (such as tungsten) embedded within the semiconductor substrate to separate adjacent pixels experienced increased dark current. Mori, [0005]. Specifically, "the silicon layer formed on the embedded member contains many crystal defects. As a result, the charge generated when dark increases, and the sensitivity of the solid-state imaging device decreases." Mori, [0007]. Dark current is the unwanted flow of electric charge when no light is incident on the photodiode.

Mori teaches that using a multi-layer silicon/silicon dioxide partition solves a problem. Mori provides for a partition part having a silicon layer (e.g., layer 175) "made of amorphous silicon or polycrystalline silicon," Mori, [0011], and a "side silicon oxide film [e.g., SiO2 film 177] formed between the silicon layer and the semiconductor substrate embedded in a semiconductor substrate," Mori, [0013]. "With this configuration, crystal defects on the side surface of the groove for forming the partition part can be reduced, and the charges generated when dark can be reduced in order to achieve high sensitivity." Mori, [0013].

Mori also teaches doping the silicon dioxide film layer to further mitigate dark current stemming from crystal defects. Specifically, "[i]n order to prevent charges generated when dark due to crystal defects in the partition groove 174 from flowing into the photoelectric conversion unit 161, p-type impurities are preferably injected into the side walls of partition groove 174 after forming the side SiO2 film 177." Mori, [0036]. As RDX-0002C.36 illustrates, once deposited side SiO_2 film 177 completely covers partition groove 174's sidewalls, such that POSITAs would understand in order to inject p-type impurities into groove 174's sidewalls would require injecting p-type impurities into SiO_2 film 177.



e. Roy

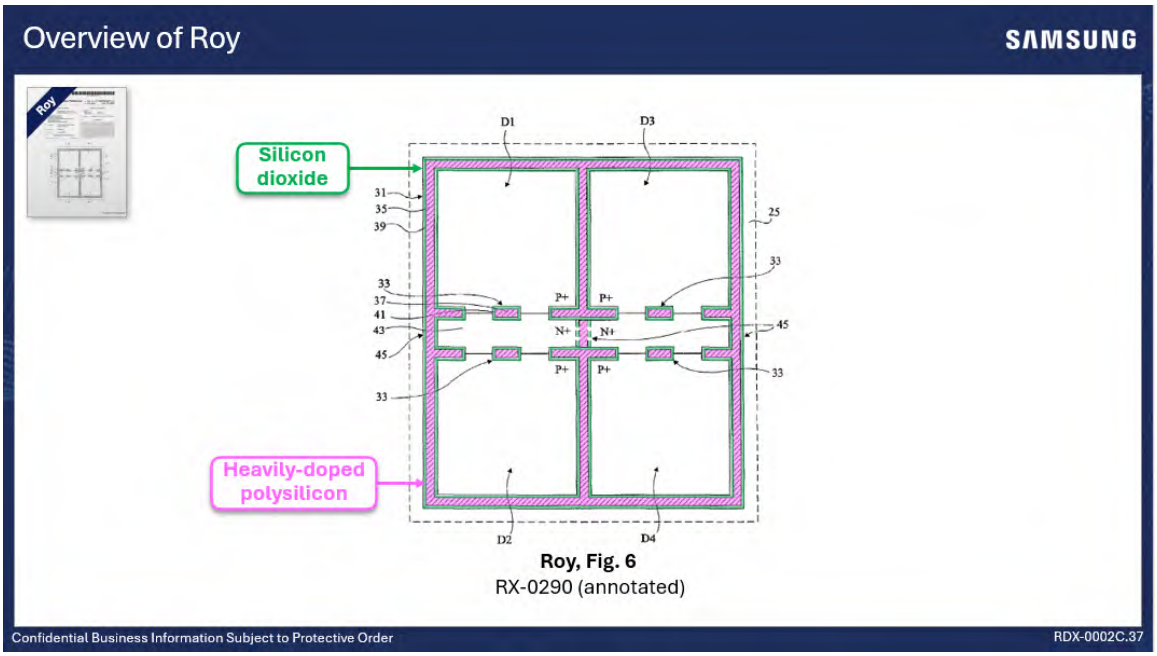
Q103 Please turn to RX-0290 (Roy). Do you recognize RX-0290?

A103 Yes. RX-0290 is U.S. Patent Application Publication No. 2009/0266973 ("Roy"), which was published on October 29, 2009. I have relied upon Roy in forming my opinions regarding the invalidity of the '599 patent.

Q104 Can you briefly describe Roy?

A104 Roy discloses "[a]n image sensor formed in a semiconductor stack of a lower region of a first conductivity type and of an upper region of a second conductivity type, including: a photodiode formed of a first portion of the stack." Roy, Abstract. Roy further discloses a pixel separation structure surrounding a photodiode. Roy, [0050] ("photodiode [] delimited by an enclosure comprising a trench.").

As RDX-0002C.37 illustrates, Roy discloses a pixel separation structure that delimits the photodiode and comprises trench 31/45 and column 33. Roy, [0050]. Roy discloses that pixel separation structure comprises conductive material layer 35 (heavily-doped polysilicon) and dielectric material layer 39 (SiO_2), Roy, [0050].



Roy teaches that it is beneficial when using a Si/SiO_2 film to use "heavily-doped polysilicon" as the silicon layer, Roy, [0050], and that "[t]he upper surfaces of the conductive materials of trench 31/45 is connected to a metallization (not shown) which enables putting this material in contact with a bias signal (V_p)," Roy, [0056]. Roy teaches that this doping and biasing "enables eliminating dark currents which are usually formed at the interfaces with insulating areas." Roy, [0071]. Roy teaches that its image sensor therefore achieves "reduced dimensions … with a low crosstalk, with a low dark current, and enabling efficient transfer of the electrons." Roy, [0045].

f. Shinohara

Q105 Please turn to RX-0292 (Shinohara). Do you recognize RX-0292?

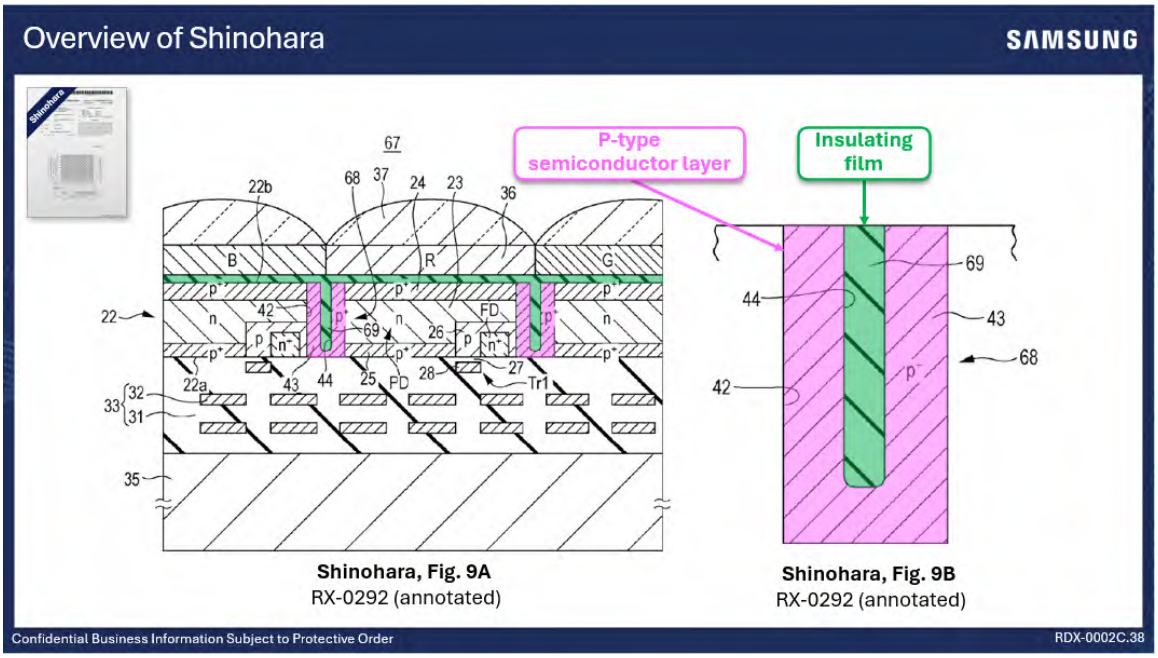
A105 Yes. RX-0292 is U.S. Patent Application Publication No. 2012/0033119 ("Shinohara"), which was published on February 9, 2012. I have relied upon Shinohara in forming my opinions regarding the invalidity of the '599 and '359 patents.

Q106 Can you briefly describe Shinohara?

A106 Shinohara discloses a backside illuminated imaging device arranged in a two-dimensional matrix including "an element isolation region isolating the pixels … which includes a semiconductor layer provided in a trench by an epitaxial growth." Shinohara, Abstract, [0006]. Shinohara also addresses how "leakage of photoelectrically converted charge into an adjacent pixel can be prevented." Shinohara, [0021].

As RDX-0002C.38 illustrates, Shinohara discloses an "insulating film 69 formed over the entire surface containing the photodiode PD of the surface 22 a as well as in the void 44." Shinohara, [0090]. Shinohara discloses that an insulating film having a negative fixed charge enhances the passivation characteristics of the element isolation region. Shinohara,

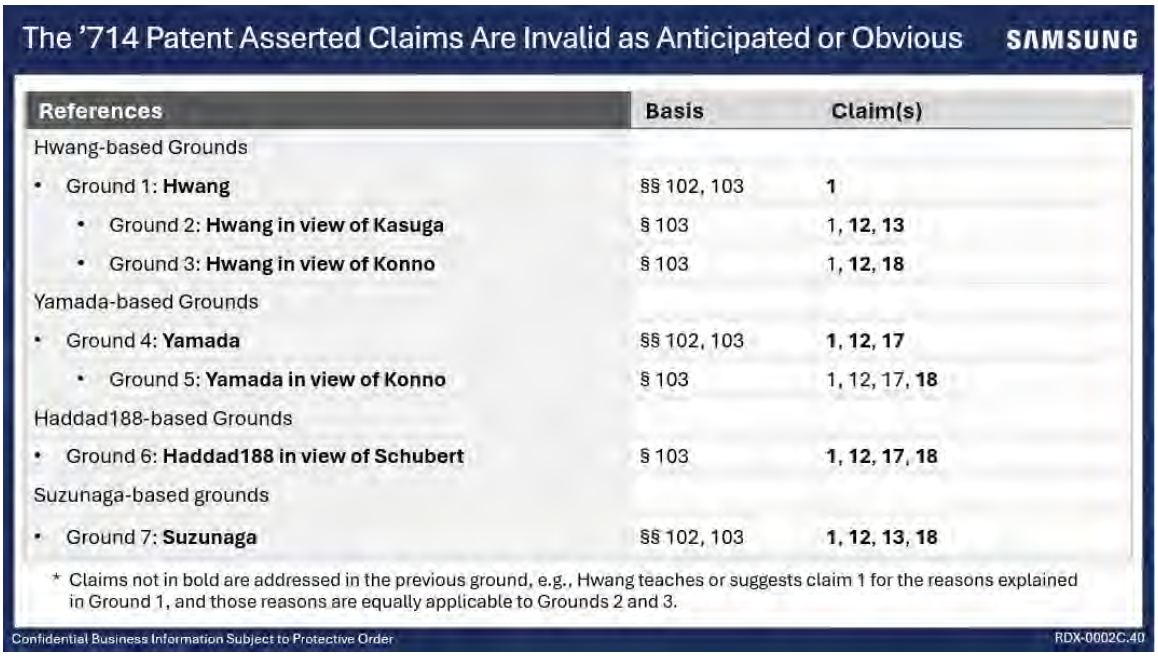
[0095]. Shinohara proposes using various materials as insulating film 69: "a film of hafnium dioxide (HfO_2), dialuminum trioxide (Al_2O_3), ditantalum pentaoxide (Ta_2O_5), dilanthanum trioxide (La_2O_3), or diyttrium trioxide (Y_2O_3)." Shinohara, [0091].



V. '714 Patent Invalidity Based on Anticipation and Obviousness

Q107 Let's start with the '714 patent. Can you summarize your opinions with respect to anticipation and obviousness of the '714 patent?

A107 Yes. As RDX-0002C.40 illustrates, in my opinion the '714 patent Asserted Claims are invalid based on four primary references: Hwang, Yamada, Haddad188, and Suzunaga.



A. Hwang-based Grounds

Q108 Let's start with your Hwang-based opinions. Can you please summarize your anticipation and obviousness opinions about the '714 patent based on Hwang?

A108 My Hwang-based opinions are divided into three grounds. Ground 1 is that Hwang anticipates, or at least renders obvious, claim 1. Ground 2 is that Hwang and Kasuga render obvious claims 1 and 12-13. Ground 3 is that Hwang and Konno render obvious claims 1, 12, and 18.

1. Ground 1: Hwang Anticipates, or at Least Renders Obvious, Claim 1

a. Claim 1

1. Limitation 1[a]

Q109 Let's start with your Ground 1 opinions that Hwang anticipates, or at least renders obvious, claim 1.

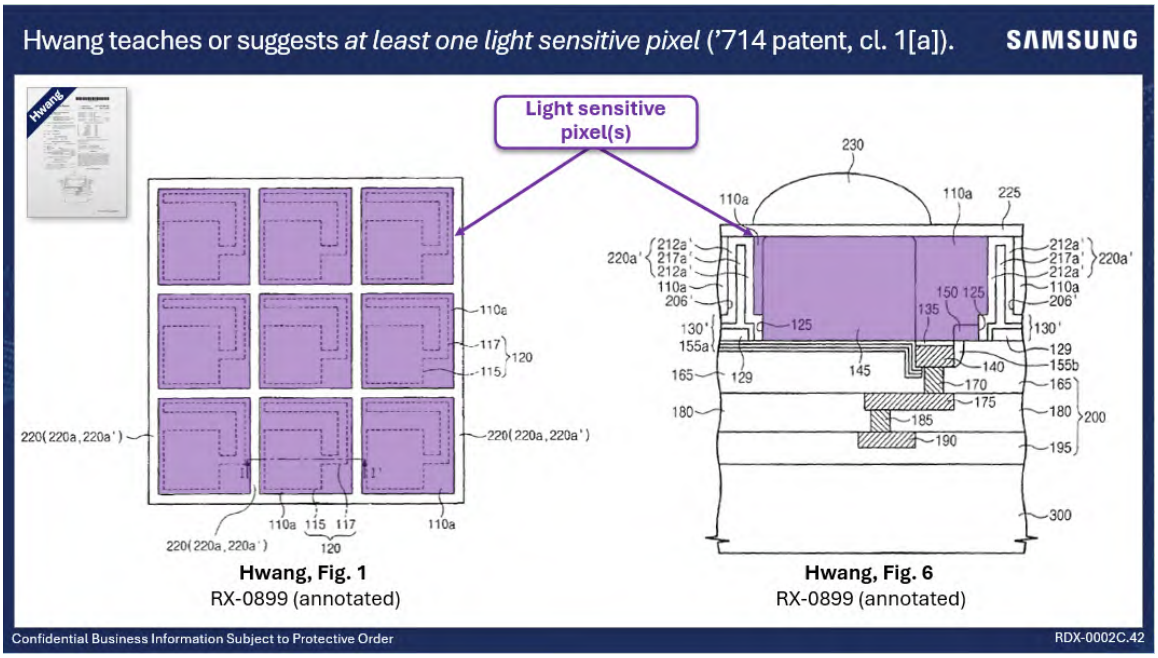
Claim 1's first limitation, 1[a], is relatively long, so let's take it in parts. The first element is *at least one light sensitive pixel*. Does Hwang satisfy this element?

A109 Yes. Hwang teaches or suggests *at least one light sensitive pixel*. Dr. Mansoorian has not disputed this.

I understand that the ALJ construed *light sensitive pixel* to have its plain and ordinary meaning. Order No. 36 at 27. Hwang includes a *light sensitive pixel* under its plain and ordinary meaning, which I consider to be portions of a device that convert light into electrical signals.

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Hwang discloses that its image sensor includes "a plurality of pixel semiconductor patterns 110*a*" "arranged two-dimensionally in rows and columns," Hwang, 5:52-59, as RDX-0002C.42 illustrates. Each pixel includes a photodiode, which "is a representative type of light receiver," "[w]hen external light is incident on a depletion region in the photodiode, electron-hole pairs are generated, and the external light is converted to electrical signals." Hwang, 1:23-29. Specifically, Hwang teaches that "[e]ach pixel semiconductor pattern 110*a* has a photodiode 145 disposed therein." Hwang, 5:57-58.



Q110 Would POSITAs consider Hwang's element 145 to itself act as a photodiode?

A110 No. Although Hwang calls element 145 a "photodiode," POSITAs would have understood that the photodiode encompasses more than just element 145 and would further encompass the surrounding pixel semiconductor patterns 110*a*. As Hwang explains, the photodiode comprises a junction created between differently doped semiconductor regions, of which element 145 is just one. *See* Hwang, 5:52-6:6 ("photodiodes 145 form a PN junction with the pixel semiconductor pattern 110*a*"); *see also* Haddad188, 8:15-19 ("photosensitive pixel can include a semiconductor substrate having multiple doped regions forming at least one junction"); JX-0027C (McKee), 97:9-18 (explaining that, when discussing Haddad188, Fig. 1, the photodiode is formed from the two doped regions and a silicon collection layer).

Q111 Are there any other reasons why POSITAs would consider the photodiode to be more than what Hwang labels as element 145?

A111 Yes. As explained, photodiodes comprise a junction created by differently doped semiconductor regions, i.e., a PN junction. *See* Hwang, 5:52-6:6. That is, making a diode requires two regions. Hwang discloses that what it labels as "photodiode 145" is doped "with a second conductive dopant," i.e., comprises only one doped region. Hwang, 5:60-

62. Thus, POSITAs would understand that what Hwang labels as "photodiode 145," could not function as a diode alone, as it comprises only one dopant type—and diodes require more than one dopant type—and is therefore only half of a diode. Instead, POSITAs would understand that the photodiode is the entirety of pixel semiconductor pattern 110*a*—which includes, alongside floating doped region 150, Hwang's element 145—as Hwang explains that "pixel semiconductor patterns 110*a* are doped with a first conductive dopant [(e.g., a p-type dopant)]" and that "photodiodes 145 are regions doped with a second conductive dopant [(e.g., a n-type dopant)]." Hwang, 6:58-62. Accordingly, POSITAs would understand that what Hwang labels as "photodiode 145" and "pixel semiconductor pattern 110*a*" are two parts of the diode which converts light into electrical signals.

Q112 Are you aware of Dr. Mansoorian's argument that Hwang's *pixel* is allegedly not pixel semiconductor pattern 110*a*?

A112 Yes. Dr. Mansoorian argues that Hwang's *pixel* is not Hwang's pixel semiconductor pattern 110*a*. RX-0911C, ¶¶135-142. Instead, Dr. Mansoorian appears to present two theories as to what Hwang's *pixel* is—one in his report and one during his deposition. I disagree and note these are theories presented in SiOnyx's contentions under Respondents' proposed construction of *pixel*. RX-0606C.18, 1104.

Q113 Why do you disagree with the theory Dr. Mansoorian presents in his report?

A113 In his report, Dr. Mansoorian appears to opine that Hwang's pixel is limited to element 145, as he argues that the *peripheral sidewall* is not *disposed into at least a portion of the pixel*, RX-0911C, ¶139 ("Hwang's pixel places the sidewall outside of the pixel as evidenced, for example, by the physical spacing between the active region of the pixel and the periphery of the 'pixel semiconductor pattern 110*a*.'"). That is, Dr. Mansoorian appears to argue that Hwang's *pixel* is limited to what Dr. Mansoorian opines is "the active region of the pixel," i.e., Hwang's element 145. Dr. Mansoorian likewise describes Hwang's pixel semiconductor pattern 110*a* as a "dead zone," as light that enters it "will likely be absorbed by [it] … and not be detected by the photodetector." RX-0911C, ¶141. I disagree.

As explained, what Hwang calls "photodiode 145," comprises only one doped region doped only with one dopant type, and thus is unable to form the PN junction necessary to convert light into electrical signals. Instead, Hwang's PN junction comprises both Hwang's element 145 and pixel semiconductor pattern 110*a*.

Q114 Why do you disagree with the theory Dr. Mansoorian presented in his deposition?

A114 During his deposition, Dr. Mansoorian opined that Hwang's *pixel* purportedly includes Hwang's element 145, lens 230, and the portions of Hwang's device—including alleged "dead zone" pixel semiconductor pattern 110*a*—that are directly underneath lens 230. *See* RX-0535C (Mansoorian), 92:18-97:17; RX-0285 (Mansoorian Dep. Ex. 8). I disagree.

First, Dr. Mansoorian's opinion as to what is Hwang's *pixel* is inconsistent with his admitted understanding of the plain and ordinary meaning of the term *pixel*, which, according to him, comprises the elements in an image sensor that convert light into an electrical signal. RX-0535C, 92:1-4. POSITAs would understand that a lens does not

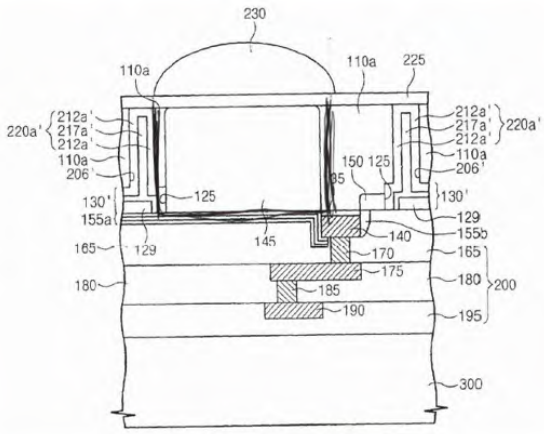
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convert light into electrical signal, as a lens merely focuses incident light instead of converting it.

Second, defining Hwang's *pixel* by the lens's external boundaries is nonsensical when considering Hwang's disclosure—particularly if Hwang is assumed to be drawn to scale, which Dr. Mansoorian incorrectly does elsewhere. *E.g.*, RX-0911C, ¶141 ("large dead zone in the pixel semiconductor pattern"). Reproduced in RDX-0002C.43 is RX-0285 (Mansoorian Depo Ex. 8) from Dr. Mansoorian's deposition, where he annotated Figure 6 of Hwang to depict what he viewed as the boundaries of Hwang's *pixel*. As RDX-0002C.43 illustrates, Dr. Mansoorian included portions of Hwang's second sidewall multi-layered reflection layer 217*a*' (a dielectric that does not convert light into electrical signals), and excluded portions of pixel semiconductor pattern 110*a* (which, as explained, does convert light into electrical signals). Dr. Mansoorian's definition further results in only part of Hwang's gate electrode 140 being in contact with the alleged *pixel*, while the majority is in contact with the alleged "dead zone." POSITAs would understand that Hwang's gate electrode is used to transfer the electrical signals created by the *pixel*, and thus it should be fully in contact with Hwang's *pixel*.

Dr. Mansoorian's opinion as to what Hwang's *pixel* is includes components that do not convert light into electrical signals, and excludes components that do.

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Mansoorian Depo Ex. 8

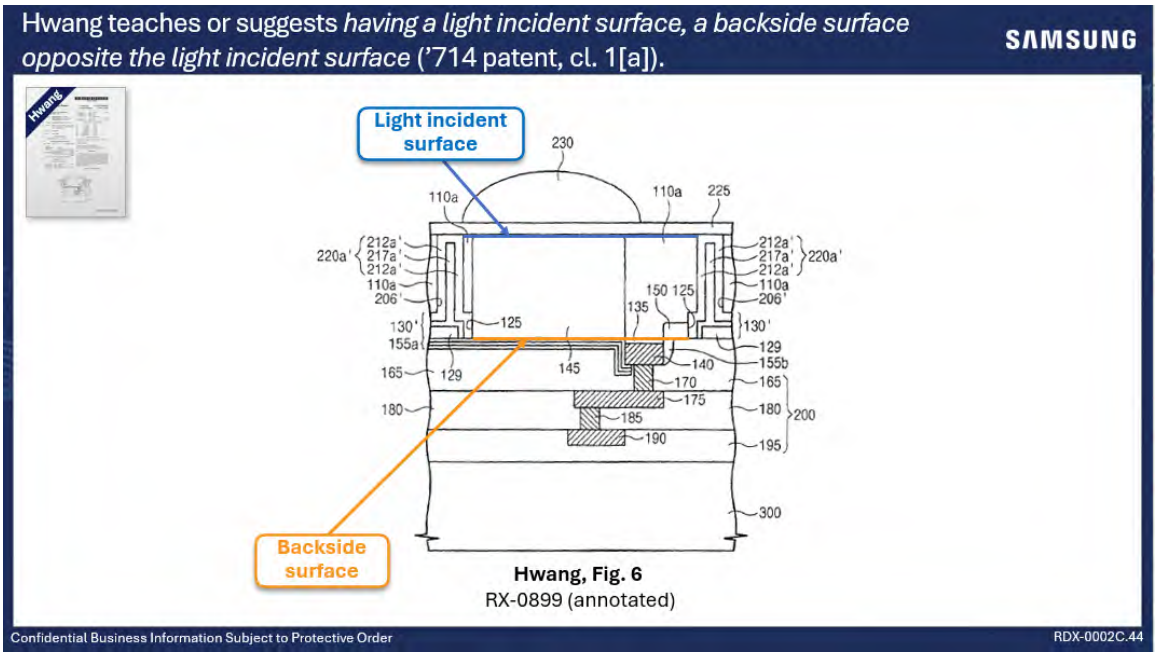
RX-0289 (showing annotations added to Hwang, Fig. 6 by Dr. Mansoorian to define Hwang's pixel)

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RDX-0002C.43

Q115 Limitation 1[a]'s second element is *having a light incident surface, a backside surface opposite the light incident surface*. Does Hwang satisfy this element?

A115 Yes. As RDX-0002C.44 illustrates, each pixel in Hwang's image sensor *ha[s] a light incident surface* [and] *a backside surface opposite the light incident surface*. Dr. Mansoorian has not disputed this.



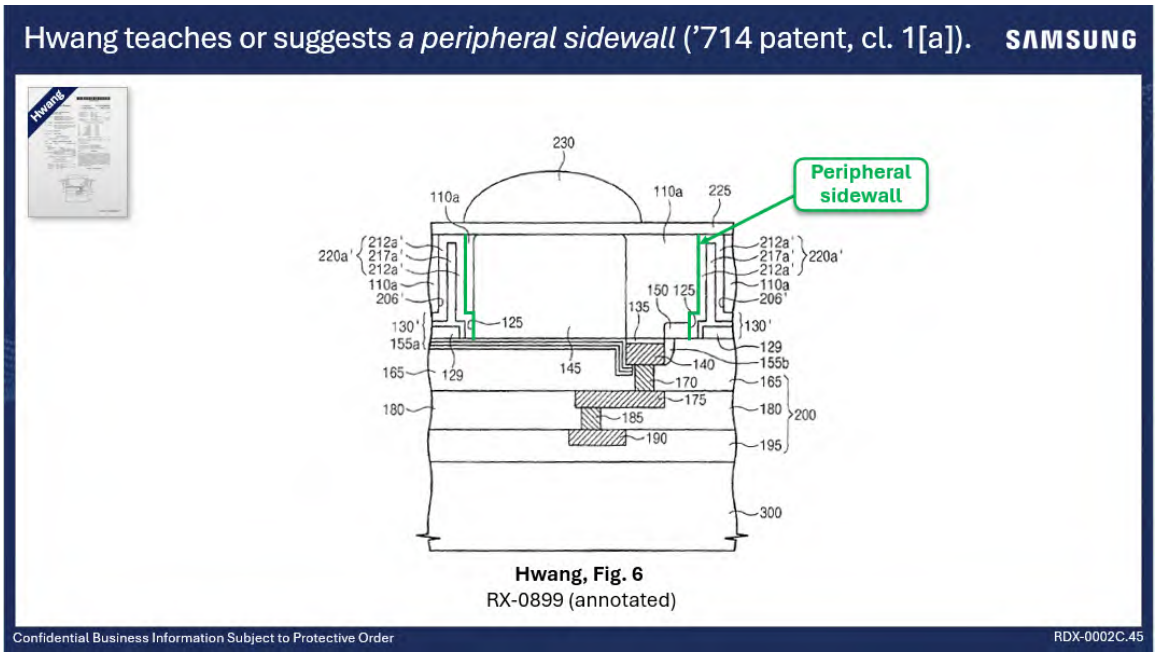
Each pixel "ha[s] first and second surfaces in parallel," with "the first surface" being "more proximate to the substrate 300 than is the second surface." Hwang, 6:37-40. Hwang's "second surface" is a *light incident surface*, as "[e]xternal light … is incident on the second surface," Hwang, 8:17-22, and Hwang's "first surface" is a *backside surface opposite the light incident surface*. *See* Hwang, 6:38-40, 6:63-65.

Q116 Limitation 1[a]'s third part is *a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery*. Have you formed an opinion regarding this element?

A116 Yes. In view of Dr. Foty's interpretation and application of this term wherein it is allegedly satisfied because the *peripheral sidewall* defines the pixel's bounds, and to the extent it is not indefinite (as I will explain), Hwang teaches or suggests this limitation.

Q117 Does Hwang include *a peripheral sidewall*?

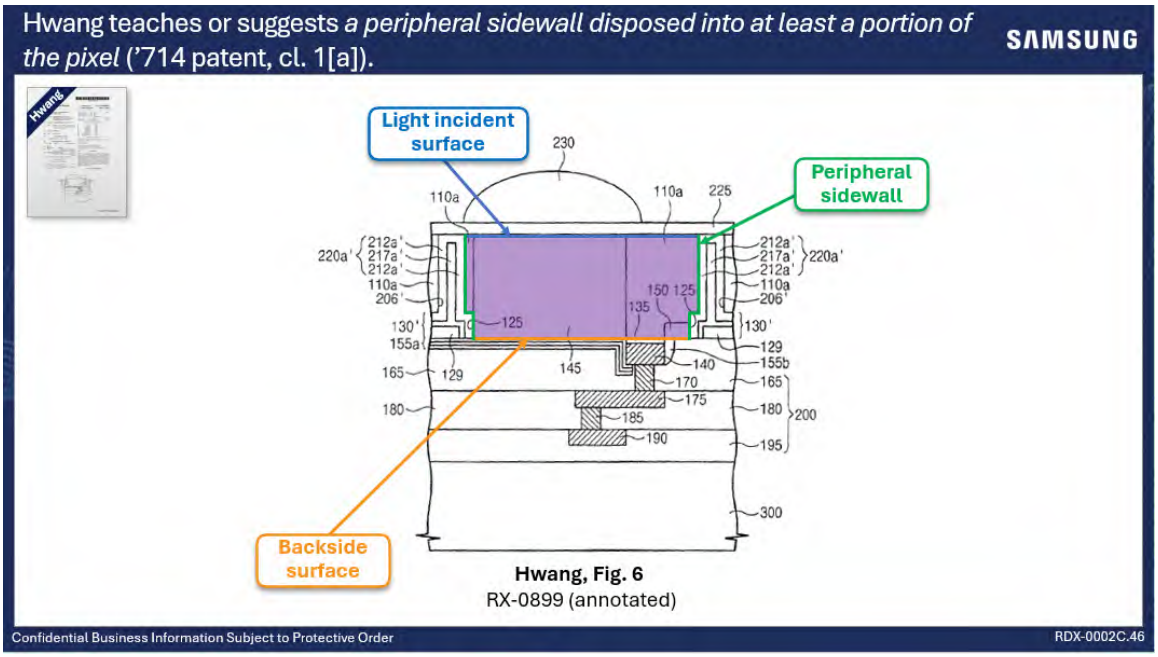
A117 Yes. I understand that the ALJ construed *sidewall* to mean trench wall. Order No. 36 at 20. As RDX-0002C.45 illustrates, each pixel has *a peripheral sidewall* (trench wall).



Hwang's "sidewall multi-layered reflection layer 220*a*' is disposed within a groove 206' formed between pixel semiconductor patterns 110*a*," Hwang, 11:64-66, such that it "is provided between the side walls of the pixel semiconductor pattern 110*a*." Hwang, 6:7-9. Accordingly, each pixel (110*a*) has *a peripheral sidewall* where it contacts sidewall multi-layered reflection layer 220*a*'.

Q118 Is Hwang's *peripheral sidewall disposed into at least a portion of the pixel*?

A118 In view of Dr. Foty's interpretation and application of this term and to the extent it is not indefinite, yes. As RDX-0002C.46 illustrates, the *peripheral sidewall* runs from Hwang's "second surface" (*light incident surface*) to its "first surface" (*backside surface*)—just like the '714 patent's peripheral sidewall 424.



Q119 Are you aware of Dr. Mansoorian's argument that Hwang's *peripheral sidewall* is not *disposed into at least a portion of the pixel*?

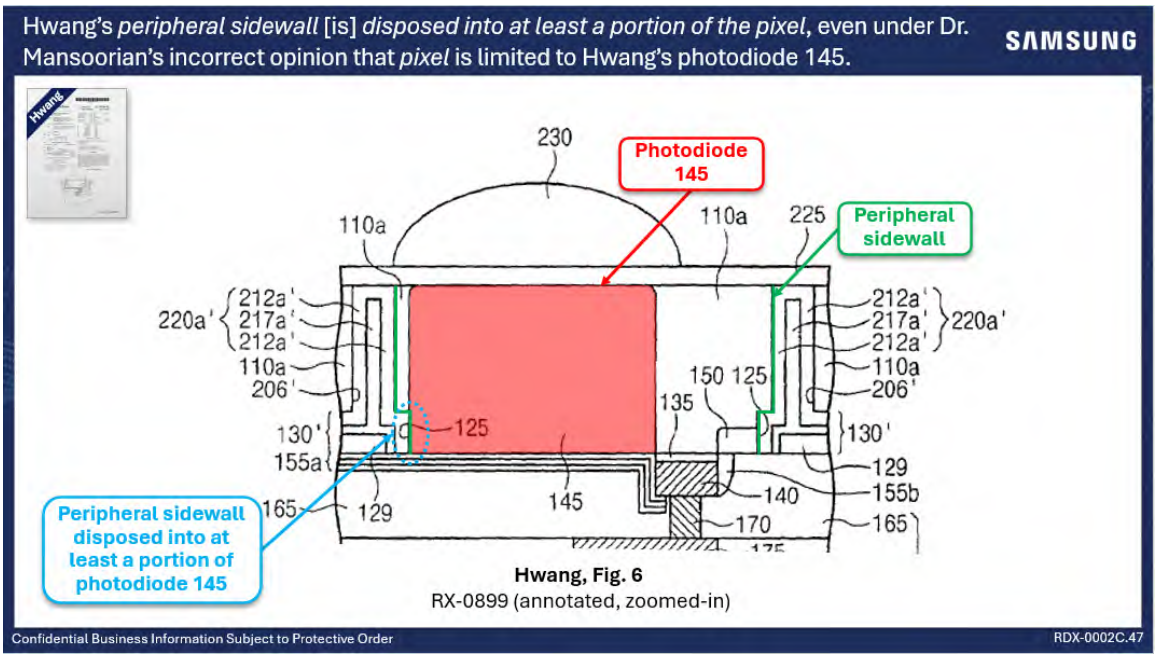
A119 Yes. Dr. Mansoorian opines that Hwang does not meet this limitation because "Hwang's pixel places the sidewall outside of the pixel." RX-0911C, ¶139; *see also* RX-0911C, ¶¶135-142. I disagree and note these are theories presented in SiOnyx's contentions under Respondents' proposed construction of *pixel*. RX-0606C.18, 1104.

Q120 Why do you disagree with Dr. Mansoorian's opinion?

A120 As explained, I believe that Dr. Mansoorian's *pixel* definition is both incorrect and inconsistent with positions he and SiOnyx's other expert, Dr. Foty, have taken. Regardless, even if Dr. Mansoorian's definition of *pixel* for Hwang were correct, Hwang would still teach or suggest a *peripheral sidewall disposed into at least a portion of the pixel*.

Q121 How does Hwang teach or suggest *a peripheral sidewall disposed into at least a portion of the pixel* under Dr. Mansoorian's definition of *pixel*?

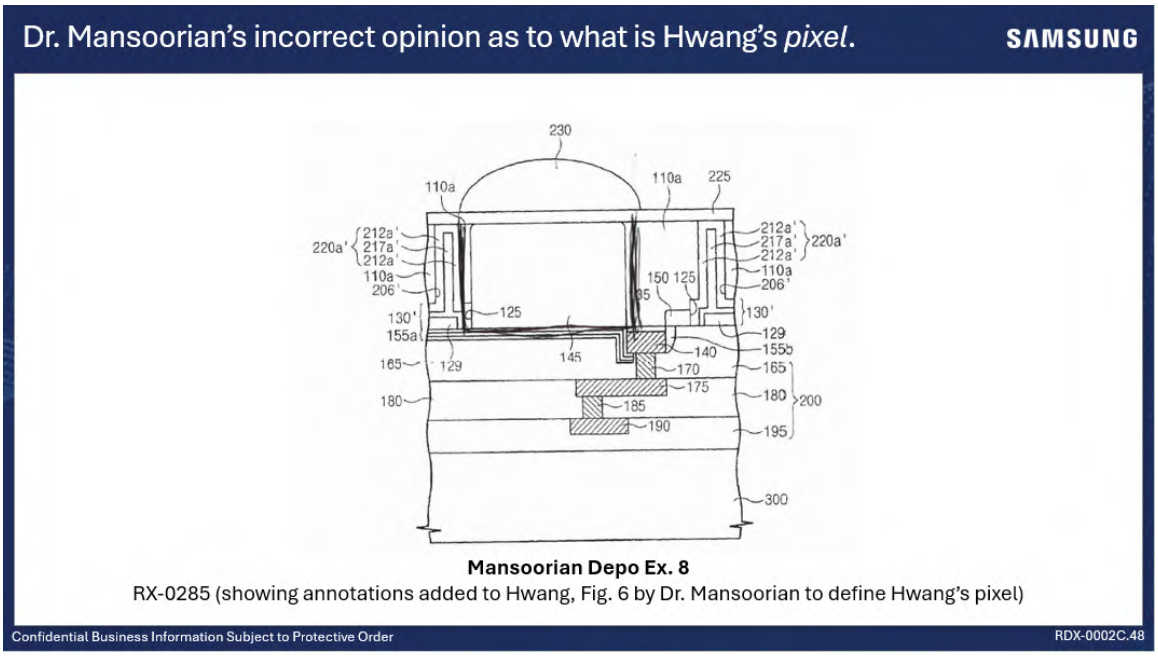
A121 For two reasons. First, Dr. Mansoorian's analysis as to why Hwang purportedly does not disclose *a peripheral sidewall disposed into at least a portion of the pixel* considers only Hwang, Figures 1-2. *See* RX-0911C, ¶¶140-141 (annotating Figure 2); *see also* RX-0911C, ¶139-142. However, my analysis for the '714, '764, and '599 patents focused on Hwang's alternative embodiment, shown in Figure 6. As RDX-0002C.47 illustrates, Figure 6, unlike Figure 2, depicts the *peripheral sidewall* (interface between multi-layered reflection layer 220*a*' and pixel semiconductor pattern 110*a*) disposed into Hwang's element 145, as it is "along the peripheral border of the pixel," RX-0905C (Foty Opening Report), ¶374, which Dr. Mansoorian appears to suggest is Hwang's *pixel*.



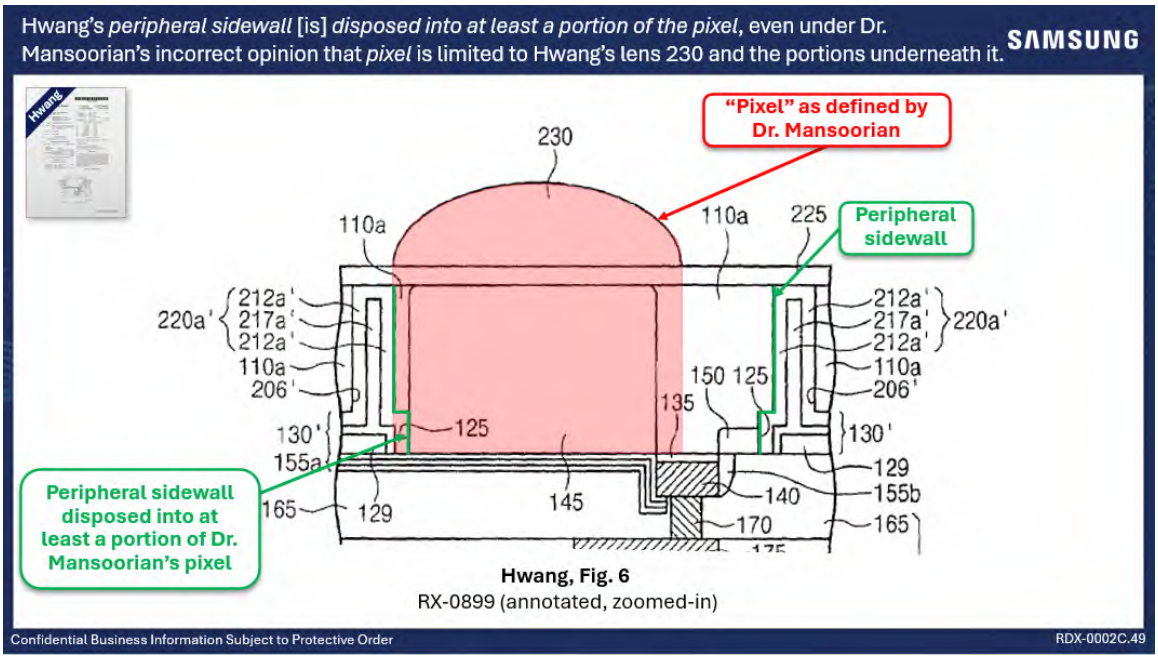
Accordingly, even if Hwang's pixel were limited to element 145, its *peripheral sidewall* would still be *disposed into at least a portion of the pixel*, as part of the peripheral sidewall is disposed into element 145.

Q122 You mentioned two reasons why Hwang teaches or suggests *a peripheral sidewall disposed into at least a portion of the pixel* under Dr. Mansoorian's definition of *pixel*. What is the second reason?

A122 Second, Dr. Mansoorian somewhat clarified his definition of pixel during his deposition, at least for Hwang, such that it includes Hwang's element 145, lens 230, and the portions of Hwang's device—including alleged "dead zone" pixel semiconductor pattern 110*a*—that are underneath lens 230. *See* RX-0535C (Mansoorian), 92:18-97:17; RX-0285 (Mansoorian Dep. Ex. 8). RDX-0002C.48 reproduces RX-0285 (Mansoorian Depo Ex. 8) where Dr. Mansoorian drew on Hwang, Figure 6 what he viewed as the boundaries of Hwang's *pixel* according to these parameters.



I have prepared RDX-0002C.49 to better illustrate what Dr. Mansoorian has now identified as Hwang's *pixel*. As RDX-0002C.49 illustrates, Hwang discloses a *peripheral sidewall* that is *disposed into at least a portion of the pixel*. Specifically, as shown, the *peripheral sidewall* (shown in green)— as well as part of Hwang's sidewall multi-layered reflection layer 220*a*'—is within what Dr. Mansoorian has identified as Hwang's *pixel* (shown in red).

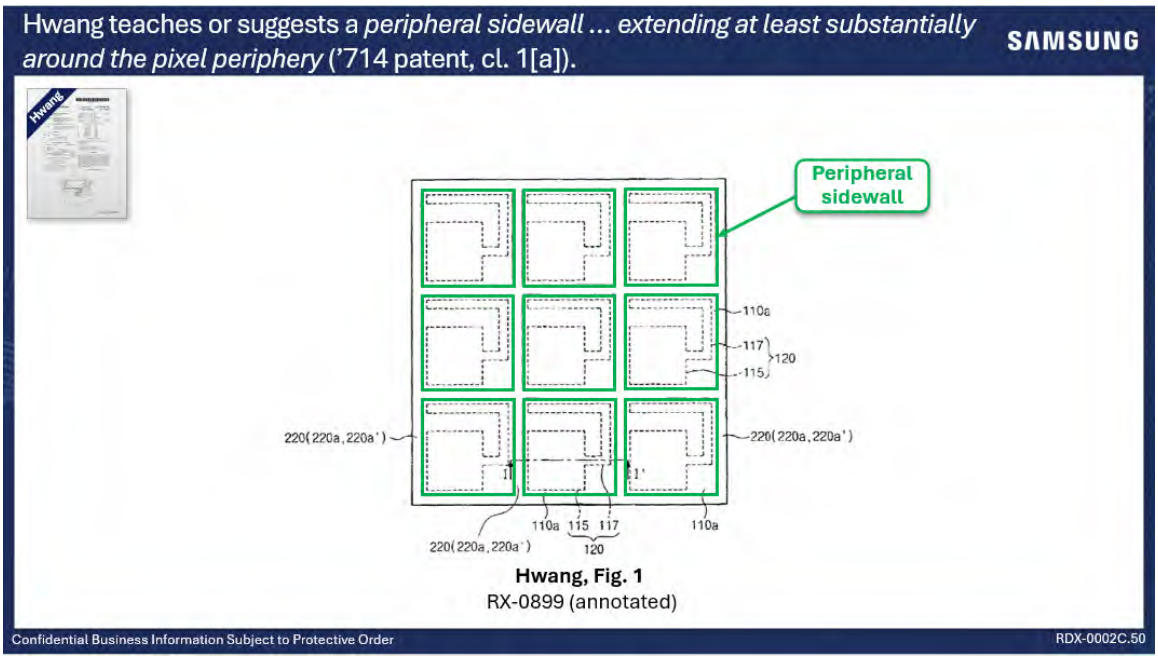


Accordingly, even under Dr. Mansoorian's incorrect definition of Hwang's *pixel*, Hwang discloses a *peripheral sidewall disposed into at least a portion of the pixel.*

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Q123 Does Hwang's *peripheral sidewall extend[] at least substantially around the pixel periphery*?

A123 In view of Dr. Foty's interpretation and application of this term and to the extent it is not indefinite, yes. I understand that the ALJ explained that "each instance of 'substantially' will need to have an individual construction tailored to the specific use," Order No. 36 at 34. As RDX-0002C.50 illustrates, "sidewall multi-layered reflection layer 220 [220*a*' in Figure 6] encloses the side walls of the pixel semiconductor pattern 110*a*." Hwang, 6:15-17. Thus, Hwang's *peripheral sidewall* extends completely around the pixel periphery, and therefore *extend[s] at least substantially around the pixel periphery*.



2. Limitation 1[b]

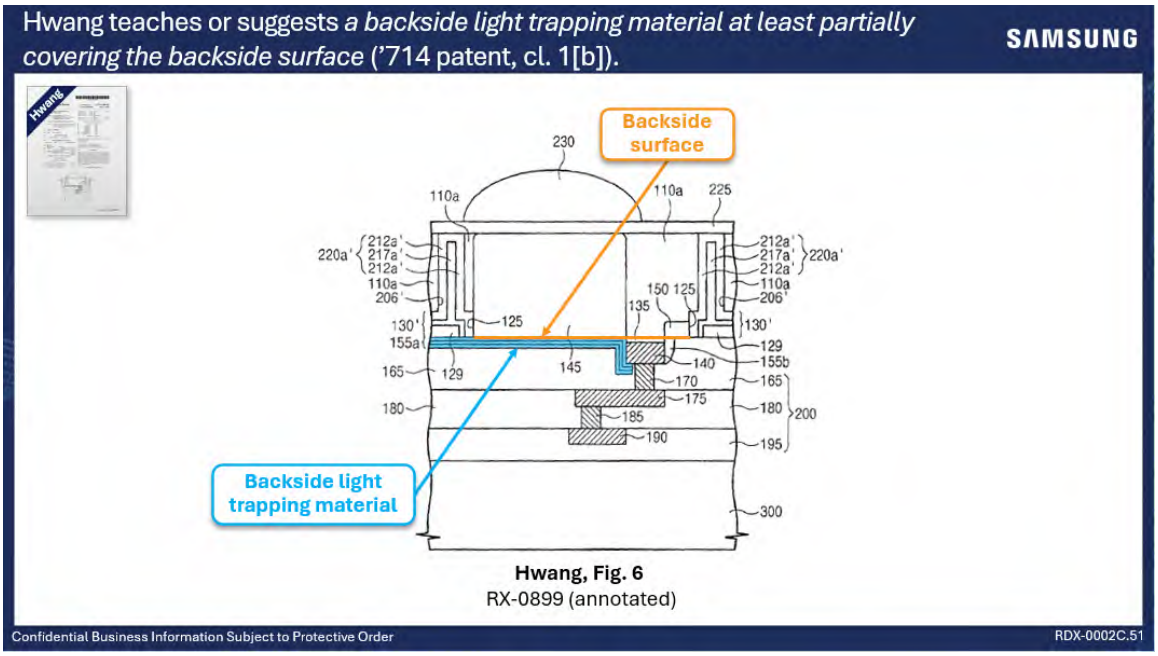
Q124 Limitation 1[b] is *a backside light trapping material at least partially covering the backside surface*. Does Hwang satisfy this limitation?

A124 Yes. Hwang teaches or suggests *a backside light trapping material at least partially covering the backside surface*. Dr. Mansoorian has not disputed this.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *light trapping material*. Hwang includes a *backside light trapping material* under either construction.

Q125 How does Hwang satisfy this limitation?

A125 As RDX-0002C.51 illustrates, Hwang's "base multi-layered reflection layer 155*a* is interposed between the photodiode 145 and the interlayer insulating layer 220," Hwang, 7:45-47, such that it "contacts the first surface [*backside surface*]," Hwang, 8:32-33. Accordingly, it *at least partially covers the backside surface*.



Base multi-layered reflection layer 155*a* constitutes a *light trapping material*. Hwang explains that "external light incident on … photodiode 145 is reflected by … base multi-layered reflection layer 155*a*," Hwang, 9:6:10, such that light reflected by base multi-layered reflection layer 155*a* "is incident again on the photodiode," therefore "increas[ing] the light sensitivity of the image sensor." Hwang, 9:6-14. Hwang teaches that such reflection occurs "at a high rate," 8:64-67, which is expected. As I will explain for limitation 1[e], base multi-layered reflection layer 155*a* is a Si/SiO_2 DBR. POSITAs would understand that such reflectors reflect more light than they transmit. For example, Schubert describes them as "yield[ing] high reflectivity" and, while using four pairs, 100% reflectivity at approximately 1-1.4µm. Schubert, 172, Fig. 10.8. Moreover, Suzunaga teaches that use of Si/SiO_2 DBRs in image sensors cause "almost 100% of incident light" to " be reflected." Suzunaga, [0027]-[0028].

Q126 How does base-multi-layered reflection layer 155*a* constitute a *light trapping material* under the parties' proposed constructions?

A126 Base multi-layered reflection layer 155*a* constitutes a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

3. Limitation 1[c]

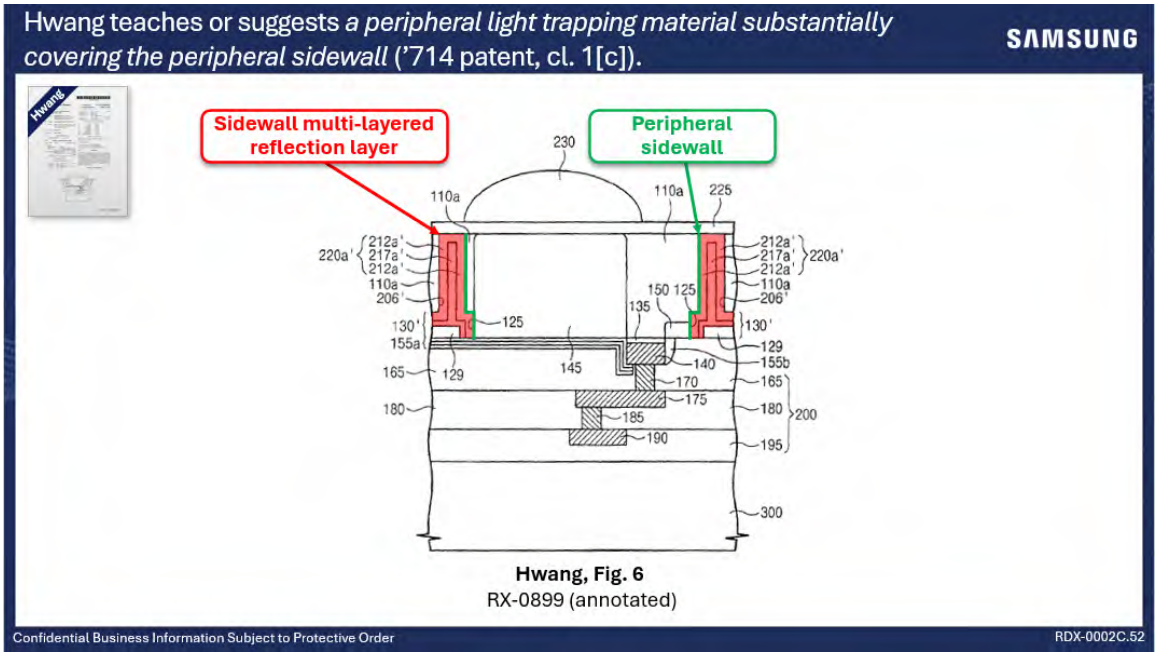
Q127 Limitation 1[c] is *a peripheral light trapping material substantially covering the peripheral sidewall*. Does Hwang satisfy this limitation?

A127 Yes. Hwang teaches or suggests *a backside light trapping material at least partially covering the backside surface*.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *light trapping material*. Hwang includes a *peripheral light trapping material* under either construction.

Q128 How does Hwang satisfy this limitation?

A128 As RDX-0002C.52 illustrates, Hwang's "sidewall multi-layered reflection layer 220*a*' is disposed within a groove 206' formed between pixel semiconductor patterns 110*a*," Hwang, 11:64-66, such that it "is disposed between the side walls of the pixel semiconductor pattern 110*a*," Hwang, 9:41-43.



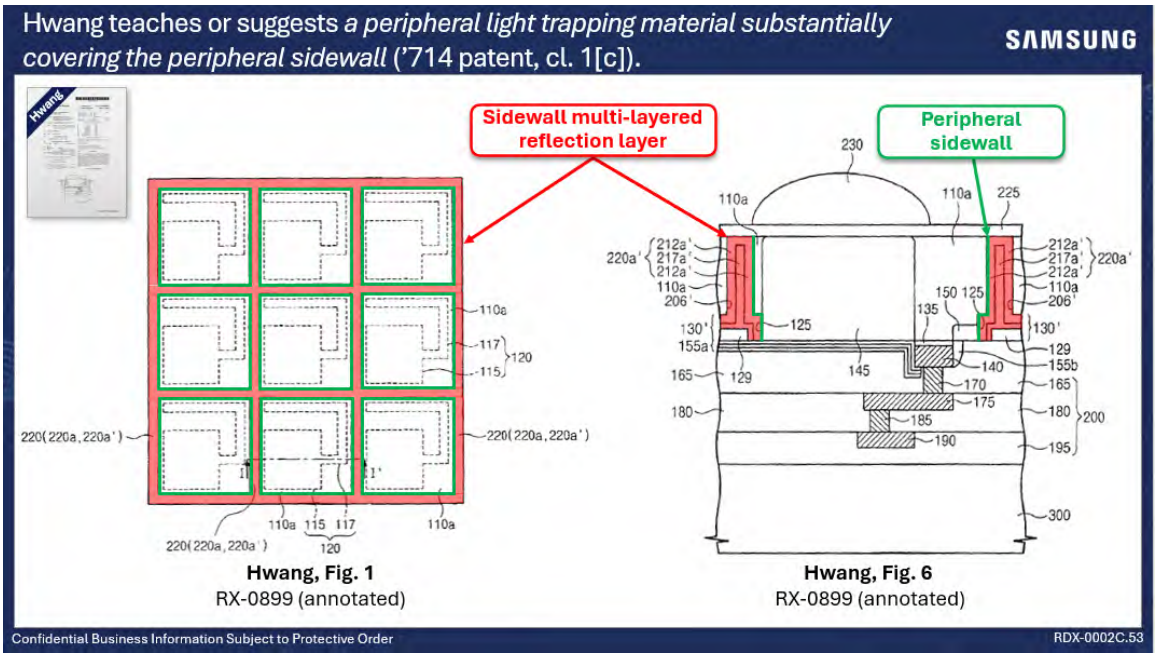
Sidewall multi-layered reflection layer 220*a*' constitutes a *light trapping material*, as light is "reflected from … sidewall multi-layered reflection layer 220 [220*a*' in Figure 6]" and thus is "incident again on the photodiode 145." Hwang, 10:28-35. Moreover, it "minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels." Hwang, 10:23-27. As I will explain for limitation 1[e], sidewall multi-layered reflection layer 220*a*' is a Si/SiO_2 DBR. As explained for limitation 1[b], POSITAs would understand such reflectors to reflect more light than they transmit.

Q129 How does sidewall multi-layered reflection layer 220*a*' constitute a *light trapping material* under the parties' proposed constructions?

A129 Sidewall multi-layered reflection layer 220*a*' constitutes a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

Q130 Does sidewall multi-layered reflection layer 220*a*' *substantially cover[] the peripheral sidewall*?

A130 Yes. As RDX-0002C.53 illustrates, "sidewall multi-layered reflection layer 220 [220*a*' in Figure 6] encloses the side walls of the pixel semiconductor pattern 110*a*," Hwang, 6:15-17 and "contact[s] the side walls of the pixel semiconductor pattern 110*a*," Hwang, 9:43-45. Thus, Hwang's *peripheral light trapping material* completely *cover[s] the peripheral sidewall*, and therefore, *substantially cover[s] it*.



4. Limitation 1[d]

Q131 Limitation 1[d] is *wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel*. Does Hwang satisfy this limitation?

A131 Yes. As explained for limitations 1[b]-[c], Hwang teaches or suggests that *light contacting* both *the backside light trapping material* [and] *the peripheral light trapping material is reflected back toward the pixel*. Hwang explains that "external light incident on … photodiode 145 is reflected by … base multi-layered reflection layer 155*a* [(*backside light trapping material*)]," and thus is "incident again on the photodiode 145." Hwang, 9:6-14. Dr. Mansoorian does not dispute this. Likewise, light is "reflected by … sidewall multi-layered reflection layer 220 [220*a*' in Figure 6 (*peripheral light trapping material*)]" and thus is "incident again on the photodiode 145." Hwang, 10:28-35.

5. Limitation 1[e]

Q132 Limitation 1[e] is *wherein at least one of the backside light trapping material or the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials*. Does Hwang satisfy this limitation?

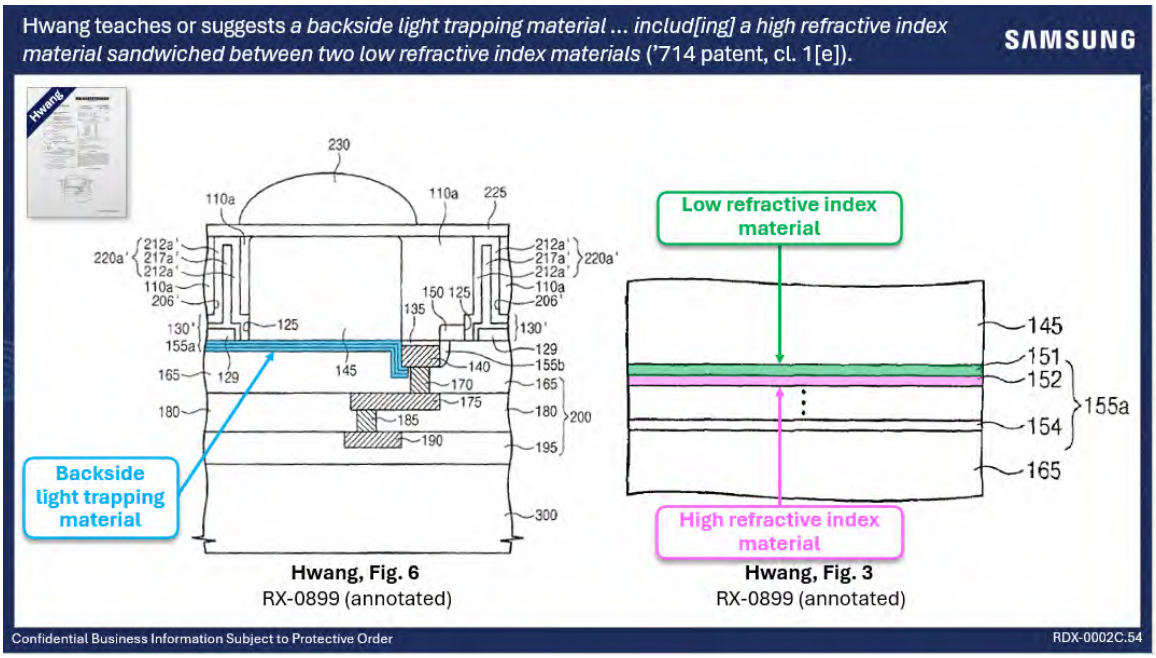
A132 Yes. Hwang teaches or suggests both a *backside light trapping material* and a *peripheral light trapping material* that *includes a high refractive index material sandwiched between two low refractive index materials*. Dr. Mansoorian has not disputed this.

As explained in the Claim Construction Order, I understand that the ALJ has construed *high refractive index material* and *low refractive index material*, Order No. 36 at 31. Hwang's *high* and *low refractive index materials* satisfy this construction.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for limitation 1[e] as a whole. Hwang satisfies limitation 1[e] under either construction.

Q133 How does Hwang's *backside light trapping material* satisfy this limitation?

A133 As RDX-0002C.54 illustrates, "base multi-layered reflection layer 155*a* [(*backside light trapping material*)] can include a first base multi-layered reflection layer 151 and a second base multi-layered reflection layer 152." Hwang, 8:40-52.[7]



[7] Figure 3 "is an enlarged view of section A in FIG. 2 for describing … base multi-layered reflection layer." Hwang, 4:64.

Hwang teaches that "first and second base multi-layered reflection layers 151 and 152 [are] respectively formed of silicon oxide (with a refractive index of approximately 1.46) and silicon (with a refractive index of approximately 4)." Hwang, 9:25-30. *See also* Hwang, 9:30-34 (describing light wavelength and multi-layered reflection layers 151 and 152's thickness).

Q134 What would POSITAs have understood Hwang's reference to silicon oxide to mean?

A134 POSITAs would know that "silicon oxide" generally includes both "silicon dioxide" (SiO_2) and "silicon monoxide" (SiO) but would also understand Hwang's reference to "silicon oxide" for its layers 210 to be a reference to silicon dioxide. While refractive indices vary based on different factors, POSITAs would know that silicon dioxide generally has a lower refractive index than silicon monoxide and would recognize that Hwang's disclosure that its "silicon oxide" layer has a refractive index of "approximately 1.46," Hwang, 9:28-29, means that layer is much more likely to be silicon dioxide than silicon monoxide. *See* RX-0312.852 (Sze) (disclosing a refractive index of "1.46" for its SiO_2); RX-0303.2-60 (Beadle) (disclosing a refractive index of ~1.4-1.5 in 400-700nm wavelength range for its SiO_2); RX-0299 (Hass), Abstract (disclosing a refractive index of 1.95-2.15 in 400-700nm wavelength for its silicon monoxide); RX-0298.17, Fig. 2 (Lopez) (disclosing a refractive index of ~1.8-1.9 in 1-5μm wavelength range for its silicon monoxide).

Consistent with this, the '714 patent also uses the generic term "silicon oxide" to refer to silicon dioxide. *See* '714 patent, 9:12-18 ("Bragg reflector can be made as in FIG 2…. In one specific aspect, for example, the Bragg reflector can be constructed of a layer of polysilicon sandwiched between two layers of silicon dioxide."), 10:20-22 ("Returning to FIG. 2, layers [of] silicon oxide and polysilicon….").

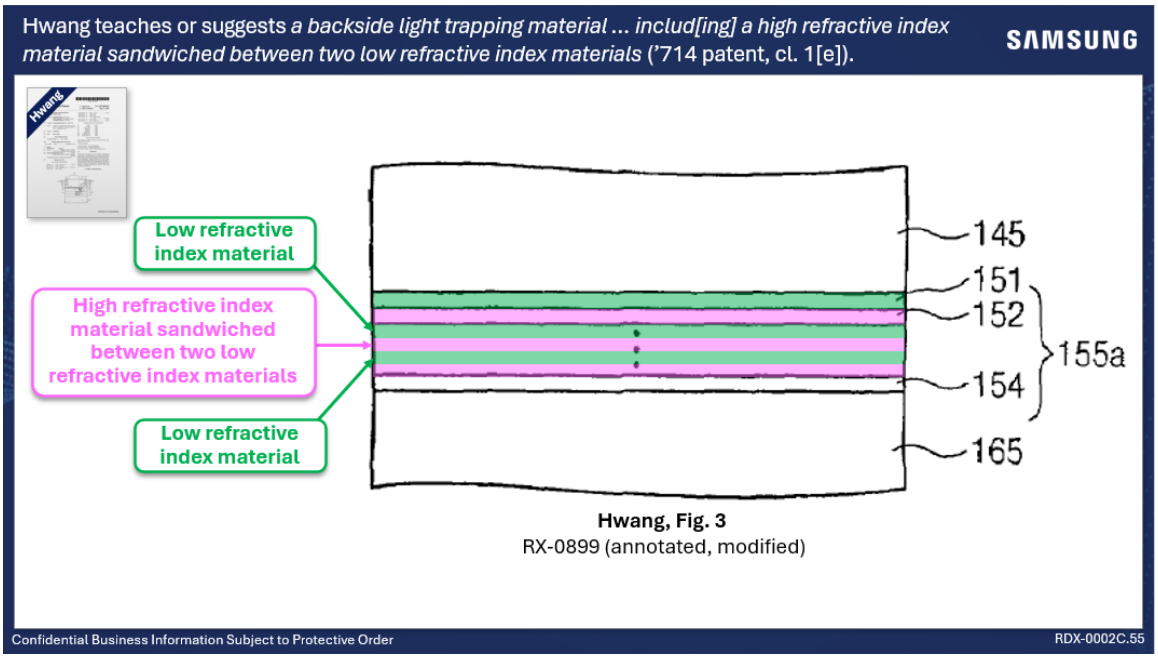
Q135 Do first and second base multi-layered reflection layers satisfy the ALJ's constructions?

A135 Yes. Second base multi-layered reflection layer 152—formed of a silicon, which Hwang discloses as having a refractive index of approximately 4—constitutes a *high refractive index material*, as Hwang discloses that its silicon has a refractive index of greater than 2.1 (i.e., ~4) and a refractive index that is at least 0.2 greater than the *low refractive index material* (i.e., SiO_2 which Hwang discloses having a refractive index of approximately 1.46). Likewise, first base multi-layered reflection layer 151—formed of a silicon oxide, which Hwang discloses having a refractive index of approximately 1.46—constitutes a *low refractive index material*, as Hwang discloses it having a refractive index of less than 2.1 (i.e., ~1.46) and a refractive index that is at least 0.2 less than the *high refractive index material* (i.e., silicon, which Hwang discloses as having a refractive index of approximately 4).

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Q136 Does Hwang teach or suggest second base multi-layered reflection layer 152 being sandwiched between two first base multi-layered reflection layers 151?

A136 Yes. As RDX-0002C.55 illustrates, Hwang teaches that "first and second base multi-layered reflection layers 151 and 152 [can be] alternatively stacked three times." Hwang, 9:25-26. *See also* Hwang, 8:54-56.



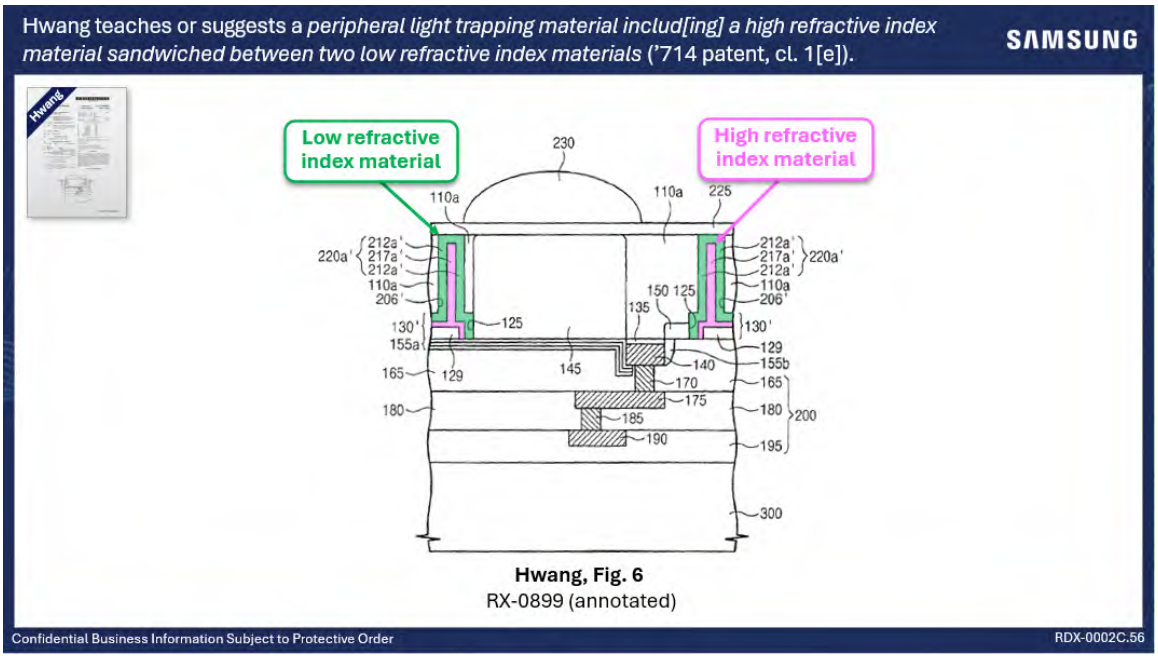
Accordingly, Hwang's *backside light trapping material includes a high refractive index material* (second base multi-layered reflection layer 152) *sandwiched between two low refractive index materials* (first base multi-layered reflection layer 151).

Q137 How does base multi-layered reflection layer 155*a* satisfy the parties' proposed constructions?

A137 Hwang's structure meets this limitation, including under either party's construction, as the *high refractive index material* is in contact with (and in between) the *low refractive index materials* on two opposing sides.

Q138 How does Hwang's *peripheral light trapping material* satisfy this limitation?

A138 As RDX-0002C.56 illustrates, Hwang teaches that "sidewall multi-layered reflection layer 220*a*' [(*peripheral light trapping material*)] includes a first sidewall reflection layer 212*a*' and a second sidewall reflection layer 217*a*'," wherein "second sidewall reflection layer 217*a*' is disposed below the first sidewall reflection layer 212*a*'." Hwang, 11:64-12:12.

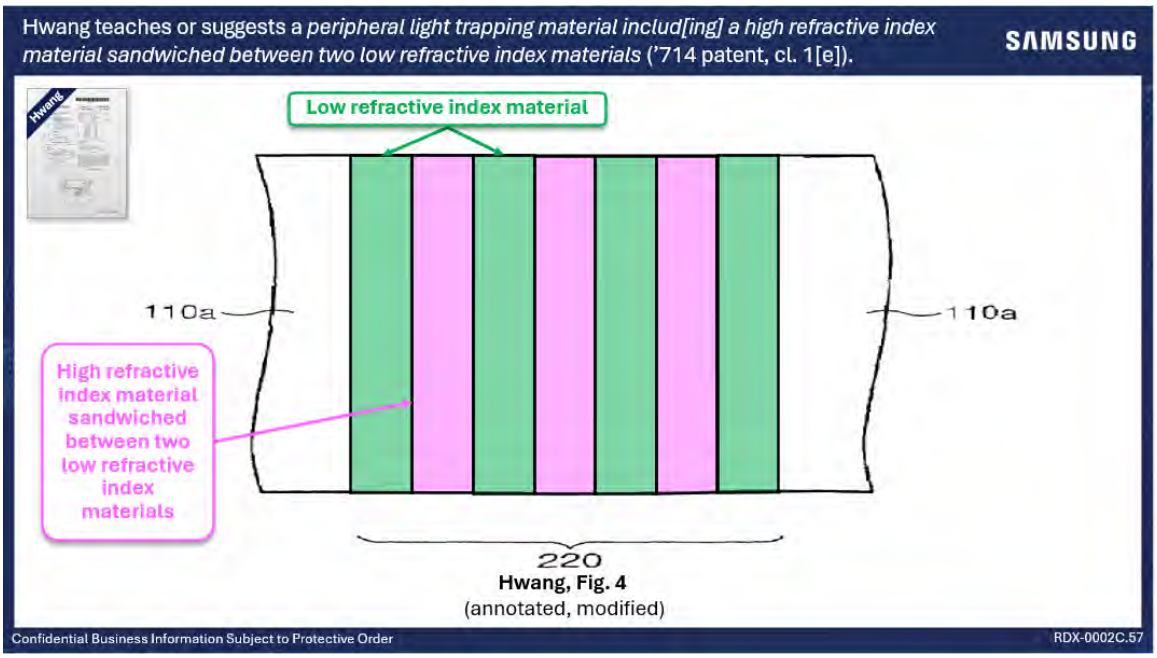


Hwang teaches that "first sidewall reflection layer 210 [212*a*' in Figure 6] can be a silicon oxide layer" and "second sidewall reflection layer 215 [217*a*' in Figure 6] can be a silicon layer." Hwang, 10:2-5; *see also* Hwang, 9:28-30, 12:4-7 For the same reasons explained for Hwang's *backside light trapping material*, first and second sidewall reflection layers 212*a*' and 217*a*' constitute *low* and *high refractive index materials*, respectively and satisfy the ALJ's constructions of those terms.

Q139 Does Hwang disclose second sidewall reflection layer 217*a*' being sandwiched between two first sidewall reflection layers 212*a*'?

A139 Yes. As RDX-0002C.57 illustrates, Hwang teaches that "first and second sidewall reflection layers 212*a*' and 217*a*' can be alternatively disposed at least once," i.e., they can be alternately stacked a plurality of times, Hwang, 12:24-25.[8]

[8] Figure 4 "is an enlarged view of B in FIG 2 for describing … sidewall multi-layered reflection layer." Hwang, 5:1-4. As explained, Figures 2 and 4's layers 220 and 215 correspond to Figure 6's layers 212*a*' and 217*a*', respectively.



By stacking sidewall reflection layers 212*a*' and 217*a*' a plurality of times, Hwang teaches or suggests a *high refractive index material* (217*a*') *sandwiched between two low refractive index materials* (212*a*'). As RDX-0002C.57 illustrates, the left *low refractive index material* is a separate layer than the second-left *low refractive index material*. Moreover, even without stacking sidewall reflection layers 212*a*' and 217*a*' a plurality of times, Hwang's image sensor is the same structure Dr. Foty accuses of infringement. RX-0905C, ¶840-843. To the extent this limitation can be read to cover the Accused Products, Hwang teaches or suggests it.

Q140 How does sidewall multi-layered reflection layer 220*a*' satisfy the parties' proposed constructions?

A140 Hwang's structure meets this limitation, including under either party's construction, including under either party's construction, as the *high refractive index material* (217*a*') is in contact with the *low refractive index material* (212*a*') on two opposing sides.

2. Ground 2: Hwang and Kasuga Render Obvious Claims 1 and 12-13

Q141 Let's turn to your Ground 2 opinions. Can you please summarize your Ground 2 opinions?

A141 In my opinion Hwang and Kasuga render obvious claims 1 and 12-13. As explained for Ground 1, Hwang anticipates, or at least renders obvious, claim 1. Those opinions are equally applicable to my Ground 2 opinions regarding Hwang and Kasuga, which further render obvious claims 12 and 13.

a. Claim 12

Q142 Let's turn to claim 12, which is *[t]he device of claim 1, further comprising a frontside light trapping material at least partially covering the light incident surface.* Have you formed an opinion regarding this claim?

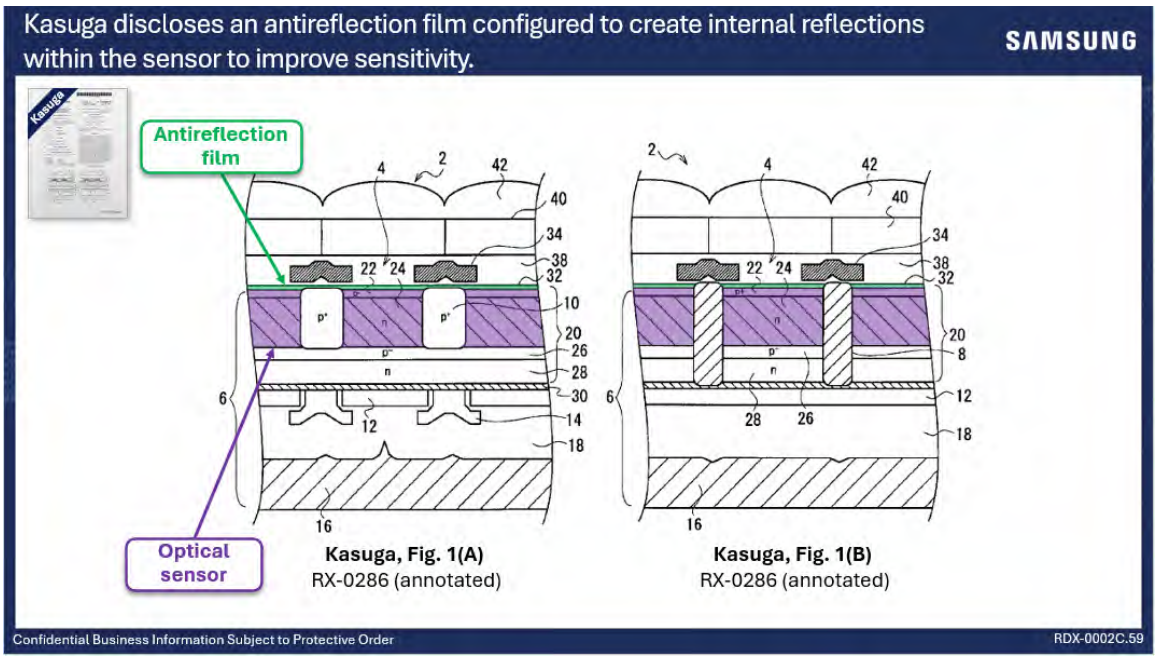
A142 Yes. Hwang and Kasuga render obvious a *frontside light trapping material at least partially covering the light incident surface*.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *light trapping material*. Hwang and Kasuga render obvious a *frontside light trapping material* under either construction.

Q143 How do Hwang and Kasuga satisfy this limitation?

A143 Yes. As explained for limitation 1[b], I understand that the parties proposed constructions for *light trapping material*. Hwang and Kasuga render obvious a *frontside light trapping material* under either party's construction.

As RDX-0002C.59 illustrates, Kasuga's "antireflection film 32 is formed on the surfaces of the optical sensors 4 to prevent the reflection of light entering the optical sensors 4, so that the amount of light entering the optical sensors 4 increases." Kasuga, 4:4-7.



Kasuga teaches that its antireflection film creates internal reflections within the sensor that improve sensitivity. For example, Kasuga teaches that, by using an antireflection film, "[e]ven if the returning light passes through the optical sensors 4 again, it is reflected by … the antireflection film 32, and is converted into electric charge by the optical sensors 4." Kasuga, 5:18-22. This allows for "multiple reflection of light [to] occur," resulting in

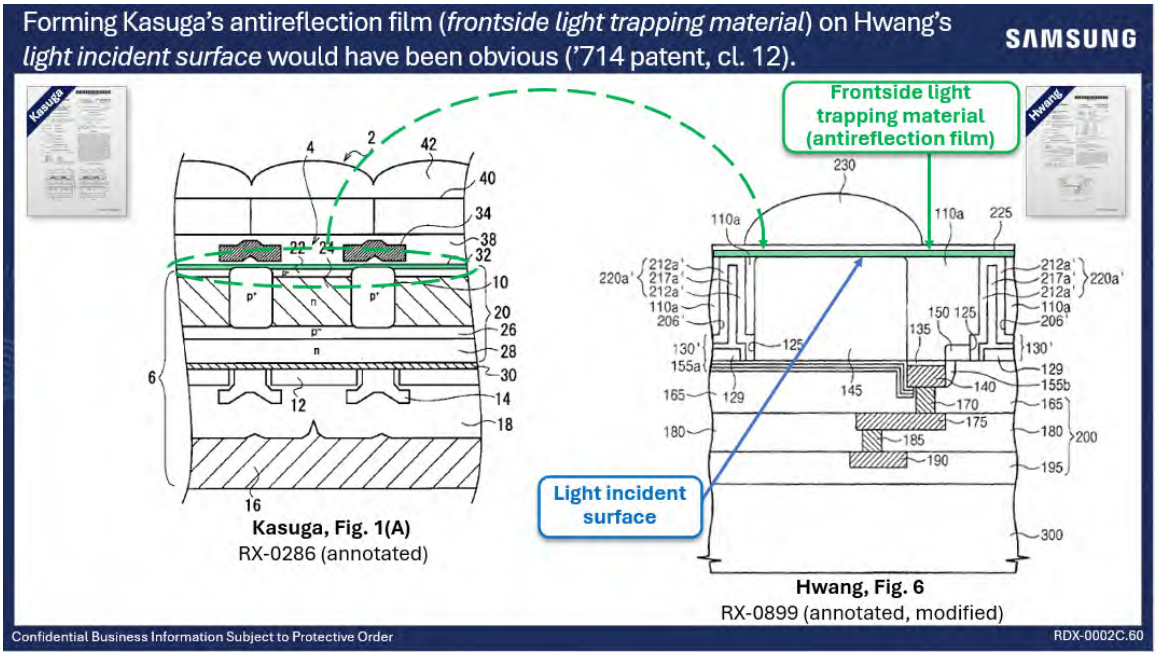
"the photoelectric conversion of incident light [being] extremely efficient." Kasuga, 5:22-31. Additionally, Kasuga teaches that:

> [W]hen the material and thickness of the antireflection film 32 are suitably selected such that light reflected by the top surface of the antireflection film 32 and light reflected by the bottom surface of the antireflection film 32 interfere with each other so as to intensify each other, the intensity of the reflected light [attempting to leave the pixel] further increases and the sensitivity [of the imaging device] can be further increased.

Kasuga, 5:40-43.

Q144 Would it be obvious to use Kasuga's antireflection film in Hwang's device?

A144 Yes. POSITAs would have been motivated to form Kasuga's antireflection film on Hwang's pixel's *light incident surface*, as RDX-0002C.60 illustrates.



This modification results in Hwang having a *frontside light trapping material* (antireflection film) *at least partially covering the light incident surface* (Hwang's "second surface"), including under either party's construction of *light trapping material*.

Q145 Why would POSITAs be motivated to make this combination?

A145 Adding Kasuga's antireflection film to Hwang's second surface results in "multiple reflection[s] of light [to] occur[] between the antireflection film.," which increases efficiency of the device. Hwang's base multi-layered reflection layer 155*a*, and Hwang's sidewall multi-layered reflection layer 220*a*'. Kasuga, 5:17-22. As Kasuga explains, "[e]ven if the returning light passes through the optical sensors," it will be "reflected by the … antireflection film" back into the optical sensors and "converted into electric charge

by the optical sensors." Kasuga, 5:17-22. Kasuga teaches that this causes "the total distance which light travels in the optical sensors [(Hwang's semiconductor pattern 110*a*) to] increase[], and the photoelectric conversion of incident light [to be] extremely efficient." Kasuga, 5:25-28.

Q146 Why would POSITAs reasonably have expected success in making this modification?

A146 Particularly given the similarities between Hwang and Kasuga. POSITAs would have recognized that Kasuga's antireflection film 32 could be readily implemented in Hwang. For example, in the manufacturing steps shown in Hwang, Figures 13/14 and 16/17, "color filter 225 is disposed on the second surface of the pixel semiconductor pattern 110*a*." Hwang, 8:17-18. POSITAs would have recognized that Kasuga's antireflection film could be placed between Hwang's color filter 225 and pixel semiconductor pattern 110*a*, similar to how, in Kasuga, "antireflection film 32 is formed on the surfaces of the optical sensors 4," beneath the "color filter 40." Kasuga, 4:4-14. *See also* Kasuga, Fig. 1.

Q147 How does antireflection film 32 constitute a *light trapping material* under the parties' proposed constructions?

A147 Antireflection film 32 constitutes a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

Q148 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination as it increases complexity?

A148 Yes. Dr. Mansoorian opines, without explanation, that POSITAs would not add Kasuga's antireflection film 32 to Hwang as doing so would add process steps which would increase defects and decrease yield. I disagree. As explained, adding Kasuga's antireflection film to Hwang would improve Hwang's sensitivity, which would balance against such speculated concerns.

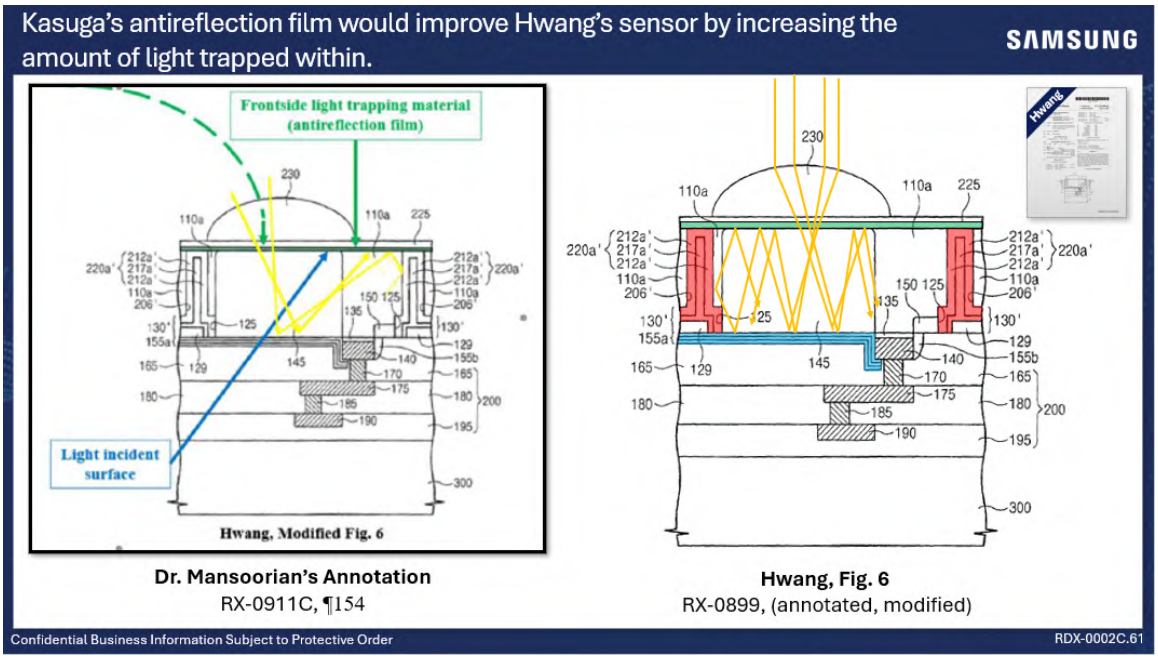
Q149 Are you aware of Dr. Mansoorian's argument that Kasuga's antireflection film would not work in Hwang because of the "large dead zones"?

A149 Yes. While Dr. Mansoorian acknowledges that Kasuga's "antireflection film is used to cause light to reflect into the pixel," he opines it would "not work in Hwang because of the large dead zones," RX-0911C, ¶154. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.1226-27.

First, as explained for '714 patent (Ground 1), limitation 1[a], Hwang does not have "dead zones," and even if it did, Hwang is not drawn to scale—something Dr. Mansoorian acknowledged, RX-0535C (Mansoorian), 160:14-17. Second, even if the "dead zones" were "large" as Dr. Mansoorian speculates, Kasuga's antireflection film would still reflect light into Hwang's pixel without entering the "dead zones." RDX-0002C.61 illustrates this point. On the left is Dr. Mansoorian's illustration, which appears to assume that light can only reflect into the right-side of Hwang's pixel. On the right, I note that light actually take numerous pathways, many of which avoid the "dead zone" entirely and are reflected off

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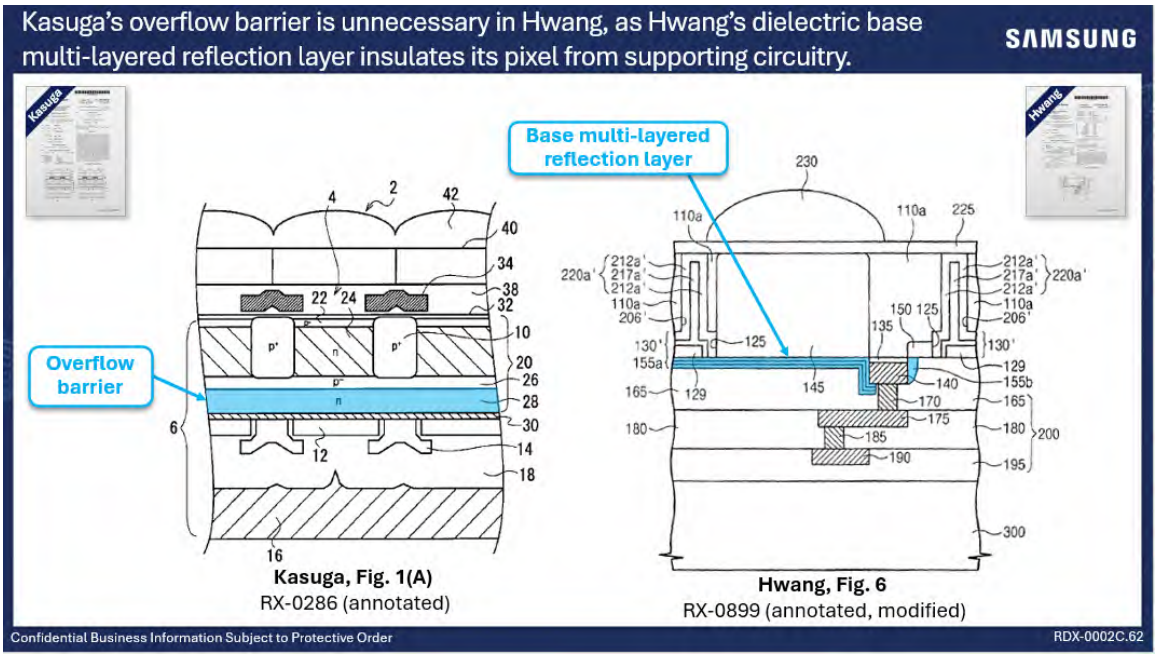
Kasuga's antireflection film. Finally, Dr. Mansoorian acknowledged that some light entering the "dead zone" would be reflected back into Hwang's pixel. *See* RX-0535C (Mansoorian), 139:17-141:13.



Q150 Are you aware of Dr. Mansoorian's argument Kasuga requires an "overflow barrier"?

A150 Yes. Dr. Mansoorian opines that POSITAs would not use Kasuga's antireflection film in Hwang because Kasuga "require[s] the use of an 'overflow barrier'" which "appears to be necessary for reflected light to be converted into an electric charge." RX-0911C, ¶155 (citing Kasuga, 9:15-22). I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.1226-1227.

Kasuga—in the same passage Dr. Mansoorian relies upon—explains that "the overflow barrier, [] does not contribute to photoelectric conversion." Moreover, as RDX-0002C.62 illustrates, Kasuga's overflow barrier 28 is located under the optical sensors to isolate them from Kasuga's circuitry. Such an overflow barrier is unnecessary in Hwang, which uses a dielectric multi-layered reflection layer 155*a* on its backside surface.



Q151 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination because Kasuga is related to CCDs and Hwang is related to CMOS devices?

A151 Yes. Dr. Mansoorian opines that POSTIAs would not have reasonably expected success in combining Kasuga and Hwang because "Kasuga is related to CCDs and Hwang is related to CMOS devices." RX-0911C, ¶157. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.1226-1227.

CCDs and CMOS devices are both used to convert light into electrical signals. In both types of devices, POSITAs would be motivated to use an antireflective film—like Kasuga's antireflection film 32—to get light into the device as well as trap light within. POSITAs understand that the antireflective film would function the same in both types of devices, and thus reasonably expect success in using such a film in Hwang despite the fact Kasuga is a CCD.

Q152 Are you aware of Dr. Mansoorian's argument that POSITAs would not consider Kasuga due to its various embodiments?

A152 Yes. Dr. Mansoorian opines that "Kasuga further appears to [claim] at least three different embodiments, each of which solves one problem and, even according to Kasuga, creates another." RX-0911C, ¶158. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.1226-1227.

First, I have only relied upon Kasuga's teachings regarding antireflection film 32, which is not present in Kasuga's other two embodiments. Second, the problems of "afterimage" present in Kasuga's first embodiment that Dr. Mansoorian points to are due to the use of polysilicon as the pixel material, which Kasuga explains would not occur when forming the pixel out of single crystal silicon. *See* Kasuga, 5:8-12. POSITAs would recognize that

Hwang teaches or suggests forming its pixel out of single crystal silicon given how Hwang is manufactured. *See* Hwang, Figs. 8-22.

b. Claim 13

Q153 Let's turn to claim 13, which is *[t]he device of claim 12, wherein the frontside light trapping material is an antireflective layer coating*. Have you formed an opinion regarding this claim?

A153 Yes. As explained for claim 12, implementing Kasuga's antireflection film 32 onto Hwang's pixel's "second surface" (*light incident surface*) would have been obvious. This added antireflection film constitutes *an antireflective layer coating*, as it serves to "prevent the reflection of light entering the optical sensors 4 so that the amount of light entering the optical sensors 4 increases." Kasuga, 4:4-7.

3. Ground 3: Hwang and Konno Render Obvious Claims 1, 12, and 18

Q154 Let's turn to your Ground 3 opinions. Can you please summarize your Ground 3 opinions?

A154 In my opinion Hwang and Konno render obvious claims 1, 12, and 18. As explained for Ground 1, Hwang anticipates, or at least renders obvious, claim 1. Those opinions are equally applicable to my Ground 3 opinions regarding Hwang and Konno, which further render obvious claims 12 and 18.

a. Claim 12

Q155 Let's turn to claim 12, which is *[t]he device of claim 1, further comprising a frontside light trapping material at least partially covering the light incident surface*. Have you formed an opinion regarding this claim?

A155 Yes. Hwang and Konno render obvious a *frontside light trapping material at least partially covering the light incident surface*.

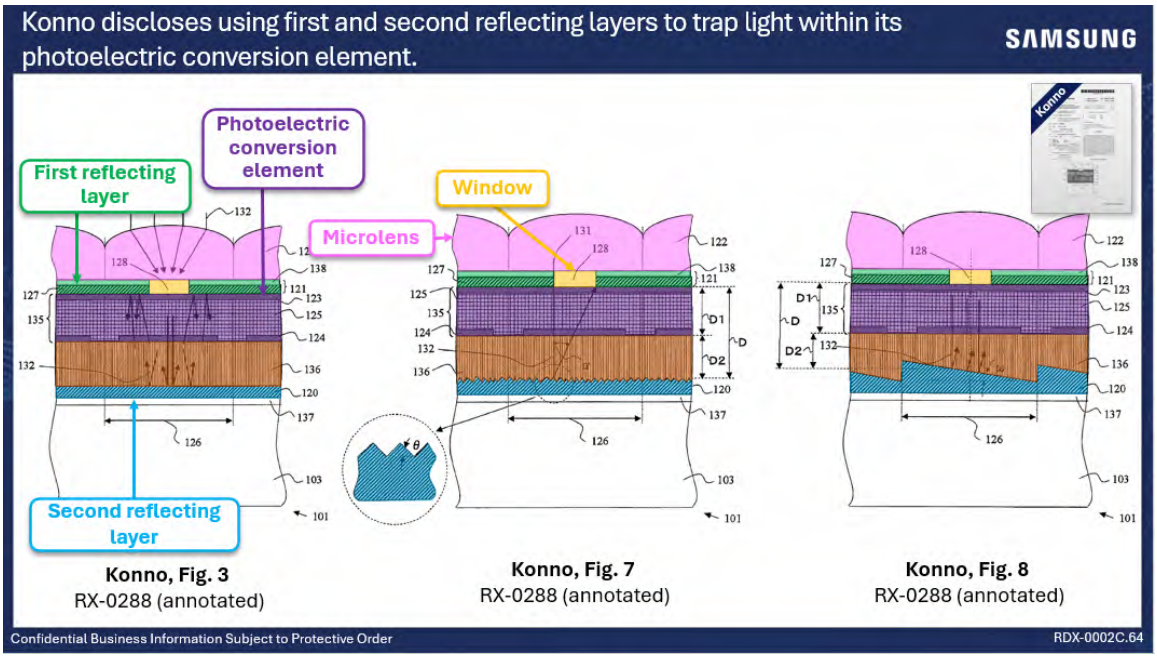
A155 As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *light trapping material*. Hwang and Konno render obvious a *frontside light trapping material*, including under either construction.

Q156 How do Hwang and Konno render this claim obvious?

A156 As explained for '714 patent (Ground 1), claim 1, Hwang teaches or suggests claim 1. Hwang in view of Konno further render obvious *a frontside light trapping material at least partially covering the light incident surface*. Specifically, it would be obvious to implement Konno's second reflecting layer 121 (*frontside light trapping material*) in Hwang.

As RDX-0002C.64 illustrates, Konno discloses a "solid-state imaging element 110 [that] has a structure where a reflecting layer (second reflecting layer) 120, a transparent layer 136, a photoelectric conversion element 135, a reflecting layer (first reflecting layer) 121

and microlens 122 are formed on a substrate 103," to improve detection sensitivity. Konno, 8:18-22. *See also* Konno, 8:22-25 ("second reflecting layer 120 and first reflecting layer 121 sandwich … photoelectric conversion element 135"). Konno teaches that "light entrance window 128 through which the incident photons 132 transmit is formed in the first reflecting layer 121." Konno, 8:56-58.



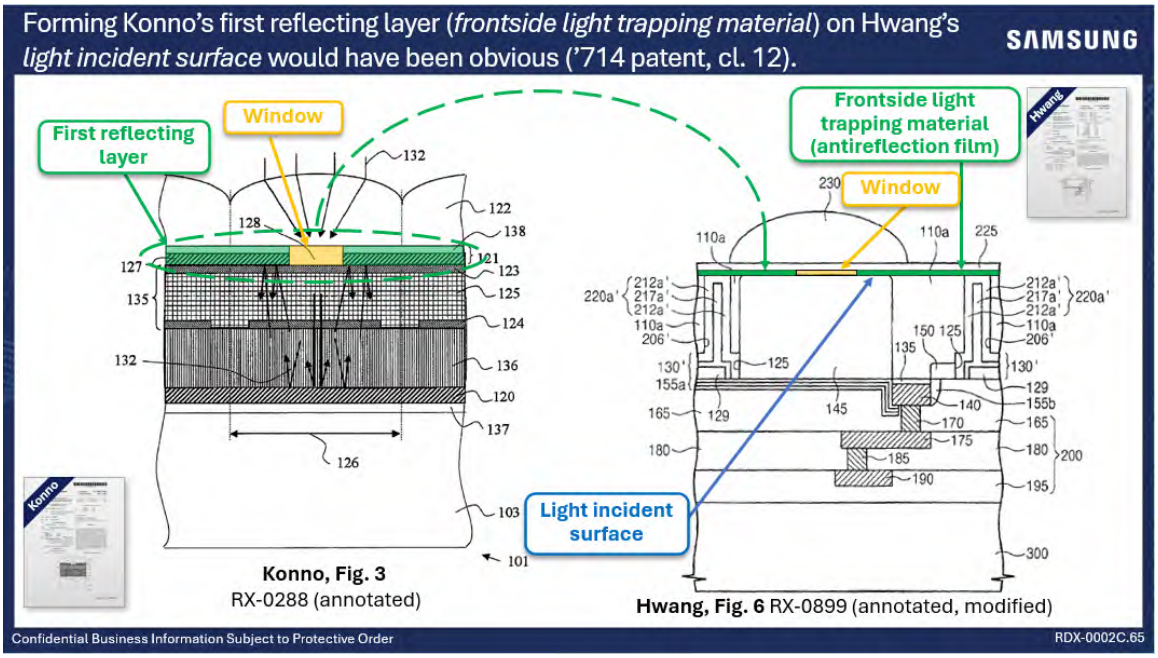
Q157 Does Konno describe the purpose of reflecting layer 121?

A157 Yes. Konno teaches that the reflecting layers reflect light back into the pixel. Specifically, Konno teaches that "photons which entered from the light entrance window 128 can be effectively confined between the first and second reflection layers 121 and 120 to … improve the detection sensitivity." Konno, 11:65-12:3. Konno also teaches that "part of the photons which passed through the photoelectric conversion film 125 reach the reflecting surface 127 of the first reflecting layer [121], are reflected again, and reach the photoelectric conversion film 125." Konno, 10:4-8.

Konno further teaches that "[t]he second reflecting layer 120 and the first reflecting layer 121 have a function of confining photons which entered into the solid-state imaging element 110 between the both." Konno, 8:31-33. Because "photons which entered into the solid-state imaging element 110 are reciprocated between the second reflecting layer 120 and the first reflecting layer 121, [the] amount of reciprocating photons … can be increased." Konno, 10:14-18. As Konno teaches, "photons which entered from the light entrance window 128 can be effectively confined between the first and second reflection layers 121 and 120 to increase the amount of photons participating in photoelectric conversion by the photoelectric conversion element 135 and thereby improve the detection sensitivity." Konno, 11:65-12:3.

Q158 Why would POSITAs use Konno's reflecting layer 121 in Hwang?

A158 As RDX-0002C.65 illustrates, implementing Konno's first reflecting layer 121, and corresponding light entrance window 128, in Hwang reduces the loss of light leaving Hwang's pixel after being reflected from its base multi-layered reflection layer 155*a* and sidewall multi-layered reflection layer 220*a*', thereby improving Hwang's detection sensitivity, would have been obvious.



As RDX-0002C.65 illustrates, this modification results in Hwang having a *frontside light trapping material* (first reflective layer 121) *at least partially covering the light incident surface* (Hwang's "second surface" at the top of pixel semiconductor pattern 110*a*).

This structure would satisfy the claim, including under either party's proposed construction.

Q159 How would Konno's reflecting layer 121, as added to Hwang, be a *light trapping material*?

A159 Konno teaches that first reflecting layer 121 "can be formed by forming a thin film of a metal such as aluminum or silver," or "[a]lternatively … may be [formed of] layers of a resin mixed with a white pigment." Konno, 8:35-43. Konno's first reflecting layer 121 constitutes a *light trapping material* that reflects light back into the pixel, as a solid metal film, as disclosed in Konno, reflects more light than it transmits. *See* Schubert, Table 10.2 (listing reflectivity of metal-air and metal-semiconductor reflectors at 0.5µm and 1.0µm, all of which have 50% or greater reflectivity).

Q160 How does reflecting layer 121 constitute a *light trapping material* under the parties' proposed constructions?

A160 Reflecting layer 121 constitutes a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

Q161 Why would POSITAs have been motivated to make this modification?

A161 POSITAs would have been motivated to make this modification, as adding Konno's first reflective layer 121, and corresponding window 128, to Hwang would allow for light to be reflected from the first reflective layer 121 back into Hwang's pixel, thus increasing its efficiency. Konno teaches that using its first reflecting layer 121 allows for "[t]he second reflecting layer 120 and the first reflecting layer 121 [to] have a function of confining photons which entered into the solid-state imaging element [] between the both." Konno, 8:31-33.

Q162 Would POSITAs have had a reasonable expectation of success in making this modification?

A162 Yes. POSITAs would have had a reasonable expectation of success in making this modification. For example, Hwang's base multi-layered reflection layer 155*a* and sidewall multi-layered reflection layer 220*a*' would serve to reflect light back to Konno's first reflective layer 121, which would then reflect light back into Hwang's pixel, thus increasing its efficiency. Additionally, like Konno, Hwang already includes a "micro lens 230," which "[e]xternal light passes through" before being "incident on the second surface," i.e., the light incident surface. Hwang, 8:20-22. When adding Konno's first reflecting layer 121 and light entrance window 128 to Hwang, it would have been obvious to POSITAs to configure Hwang's lens such that it concentrates the light through the window, as Konno teaches, in order to ensure that light enters the pixel.

Moreover, POSITAs would have recognized that Konno's first reflective layer 121, and corresponding light entrance window 128, could be readily implemented in Hwang. For example, in the manufacturing steps illustrated for Hwang's substantially similar embodiments in Figures 13/14 and 16/17, Hwang teaches that "color filter 225 is disposed on the second surface of the pixel semiconductor patter 110*a*." Hwang, 8:17-18. POSITAs would have recognized that Konno's first reflective layer 12, and corresponding light entrance window 128, could be placed between Hwang's color filter 225 and its pixel semiconductor pattern 110*a*, similar to how in Konno the first reflective layer 121 and light entrance window 128 are formed above the photoelectric conversion element 135. *See generally*, Konno, 8:18-30, Figs. 3-4.

Q163 Are you aware of Dr. Mansoorian' argument that POSITAs would not make this combination because it would require modifying Hwang's microlens?

A163 Yes. Dr. Mansoorian opines that "a POSITA would [not] have been able to perform this modification with a reasonable expectation of success" because "[m]odifying a microlens 'to concentrate[] the light through a small aperture is not a straightforward or simple

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engineering task." RX-0911C, ¶177. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.1229-1230.

While Dr. Mansoorian says "lens modification requires knowledge of optical engineering and often requires significant computer modeling to be successful," and is "more difficult due to the scale" of Hwang and Konno, such tasks are well within POSITAs' skill, who would "have would have at least a bachelor's degree in electrical engineering, materials science, or physics (or an equivalent degree) and at least two years of experience in optoelectronics." Order No. 36 at 19.

Indeed, the Light Trapping Patents do not provide for dimensions or configurations for the microlens; accordingly, it is unclear how POSITAs would be able to make and use the Light Trapping Patents' alleged invention under Dr. Mansoorian's theory.

Q164 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination as it would create dark current?

A164 Yes. Dr. Mansoorian opines for the first time in his report that POSITAs "would not have been motivated to modify the device of Hwang to include the reflective films of Konno … because the metal reflective films would create significant dark current when placed directly on Hwang's semiconductor pattern 110*a*." RX-0911C, ¶¶178-180. While I agree that placing a metal reflector directly on Hwang's pixel would create dark current, I disagree that this fact would mean POSITAs would not be motivated to make this combination. POSITAs would be well aware of the fact that such a modification would create dark current, as Dr. Mansoorian asserts, and would have likewise understood that such dark current could be easily overcome by placing a dielectric layer between the two, such as a thin layer of SiO_2.

I did not believe that explanation of such an obvious step, i.e., insulating the pixel from a metal layer, was necessary to explain in my opening report, particularly because SiOnyx did not make in its contentions the argument that Dr. Mansoorian is now advancing. Instead, SiOnyx merely argued that POSITAs would not make this combination as "Konno's second reflecting layer [(i.e., backside reflector] includes various surface features that can introduce dark current into the device." RX-0606C.387 (SiOnyx's Validity Contentions). As I pointed out in my report, SiOnyx's criticism was directed to the wrong layer, as this combination involves Konno's first reflective layer, i.e., its frontside reflector.

Q165 Are you aware of Dr. Mansoorian's argument that POSITAs would not be motivated to modify Hwang based on Konno because Konno is non-analogous art?

A165 Yes. Dr. Mansoorian opines that POSITAs would not combine Hwang and Konno because "Hwang discloses a device for use in generating picture-quality images, i.e., a camera," and "Konno, on the other hand, is optimized for use in a 'personal authentication system.'" RX-0911C, ¶181. I disagree. As I explained in the Overview of Konno, Konno is not limited to personal authentication systems, but is instead directed to solid-state imaging

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elements, including an "image sensor … and digital camera," just like Hwang. Konno, 1:15-22.

b. Claim 18

Q166 Let's turn to claim 18, which is *[t]he device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface*. Have you formed an opinion regarding this claim?

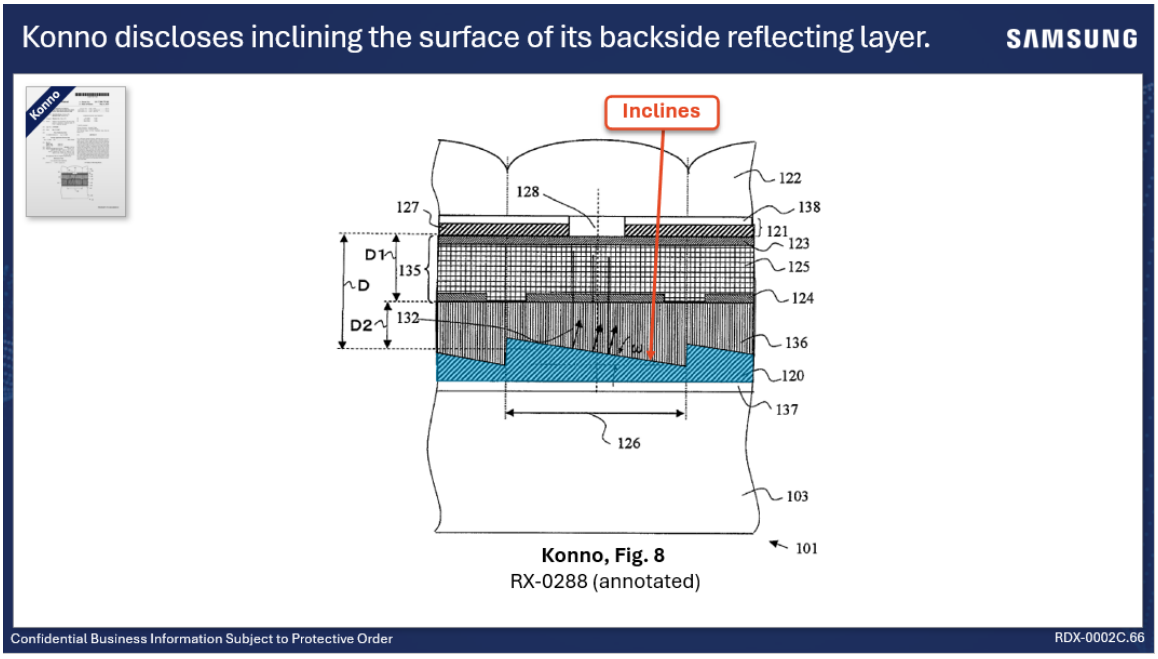
A166 As explained regarding the Terms Remaining in Dispute, I understand that Samsung proposed the term *sloped surface at the pixel device interface* is indefinite, and that SiOnyx proposed it has its plain and ordinary meaning, and to the extent a construction is required, it means sloped trench wall or sloped backside surface.

It is unclear what is meant by *a sloped surface at the pixel device interface*, in particular, what is meant by a *pixel device interface*. There is no discussion in the specification of a *pixel device interface*, and the term lacks antecedent basis, such that the specification fails to inform POSITAs, with reasonable certainty, of the claim's scope.

To the extent the limitation is not indefinite, Hwang and Konno render obvious a *backside light trapping material* that *has a sloped surface at the pixel device interface*.

Q167 Assuming the claim is not indefinite, do Hwang and Konno satisfy this limitation?

A167 As RDX-0002C.66 illustrates, Konno's Figure 8 embodiment includes a second reflecting layer 120 constituting a *backside light trapping material* that has *a sloped surface*. In particular, Konno teaches that "second reflecting layer 120," can have "incline[s]." Konno, 15:36-38.



Konno teaches that such inclined surfaces can be used to redirect light to other reflectors on the pixel's surface and thereby increase sensitivity. *See* Konno, 15:38-40 ("Incident photons are reflected by this reflecting surface to the first reflecting layer 121 on one side of the light entrance window 128."), 15:46-50 ("the inclination of the reflecting surface is designed so that most of the photons which entered at the light entrance window 128 except for those absorbed by the photoelectric conversion film 125 should reach the first reflecting layer 121").

Q168 Why would POSITAs use a sloped surface in Hwang?

A168 POSITAs would have been motivated to form Hwang's base multi-layered reflection layer 155*a* with a *sloped surface*, as POSITAs would have understood that such an inclined surface could be used to redirect light to Hwang's sidewall multi-layered reflection layer 220*a*', or to an added frontside light trapping material as discussed for '714 patent (Ground 3), claim 12, so as to increase Hwang's efficiency. Forming Hwang's base multi-layered reflection layer 155*a* with a *sloped surface* would have been nothing more than the use of a known technique to improve similar devices in the same way to yield predictable results (i.e., redirection of light at the backside surface). POSITAs would have reasonably expected success in making this modification. For example, such a sloped surface could be implemented after the manufacturing steps shown in Hwang's Figure 22 or between the manufacturing steps shown in Hwang's Figures 8/9 for a substantially similar embodiment.

Q169 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination as it would decrease the size of Hwang's pixel?

A169 Yes. Dr. Mansoorian opines that POSITAs would not make this combination as "it would require reducing the size of the active, light sensing depletion region within the photodiode," which would "reduce light absorption efficiency and light sensitivity of the device." RX-0911C, ¶205. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.153-154.

First, POSITAs could understand that Hwang's base multi-layered reflection layer 155*a* could be formed with a sloped surface without decreasing the size of Hwang's pixel. Dr. Mansoorian assumes base multi-layered reflection layer 155*a* must slope upwards into Hwang's pixel, however, POSITAs would recognize that it could also slope downwards into Hwang's interlayer insulating layer 165 (while also possibly adjusting Hwang's sidewall multilayered reflection layer 220*a*' to prevent crosstalk) which would increase the size of Hwang's pixel.

Second, even assuming base multi-layered reflection layered 155*a* must slope upwards into Hwang's pixel as Dr. Mansoorian opines, POSITAs would still be motivated to make this combination. As explained, sloping base multi-layered reflection layer 155*a* results in light being redirected to Hwang's sidewall multi-layered reflection layer 220*a*', or to an added frontside light trapping material as discussed for '714 patent (Ground 3), claim 12, so as to increase Hwang's efficiency. Specifically, it would trap additional light within Hwang's pixel by redirecting light that would ordinarily escape through Hwang's light incident surface to its sidewall reflectors, causing multiple reflections which increase the pathlength

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of light traveling within Hwang's pixel and allowing for the pixel to be made smaller while retaining sensitivity.

B. Yamada-based Grounds

Q170 Let's turn to your Yamada-based opinions. Can you please summarize your anticipation and obviousness opinions about the '714 patent based on Yamada?

A170 My Yamada-based opinions are divided into two grounds. Ground 4 is that Yamada anticipates, or at least renders obvious, claims 1, 12, and 17. Ground 5 is that Yamada and Konno render obvious claims 1, 12, and 17-18.

1. Ground 4: Yamada Anticipates, or at Least Renders Obvious, Claims 1, 12, and 17

a. Claim 1

1. Limitation 1[a]

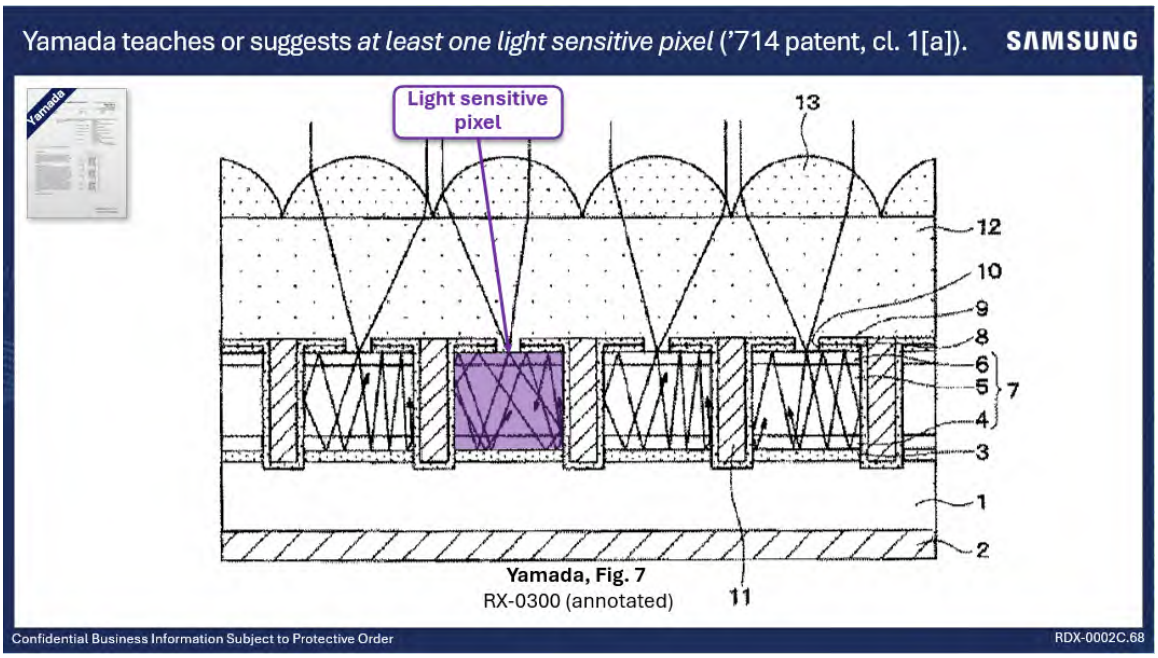
Q171 Let's start with your Ground 4 opinions that Yamada anticipates, or at least renders obvious, claims 1, 12, and 17.

Claim 1's first limitation, 1[a], is relatively long, so let's take it in parts. The first element is *at least one light sensitive pixel*. Have you formed an opinion regarding this element?

A171 Yes. Yamada teaches or suggests this element.

I understand that the ALJ construed *light sensitive pixel* to have its plain and ordinary meaning. Order No. 36 at 27. Yamada includes a *light sensitive pixel* under its plain and ordinary meaning, which I consider to be the portions of a device that convert light into electrical signals. As RDX-0002C.68 illustrates, Yamada includes "a light receiving element [that is] provided with a plurality of light receiving sections (7)." Yamada, [0009]. Yamada teaches that "light receiving section[s] (7) can be composed of a PIN photodiode," Yamada, [0016], and that "light energy is converted into electrical energy inside the PIN photodiode and a photocurrent caused by an electron-hole pair is generated to detect the light incident on the PIN photodiode 7," Yamada, [0035].

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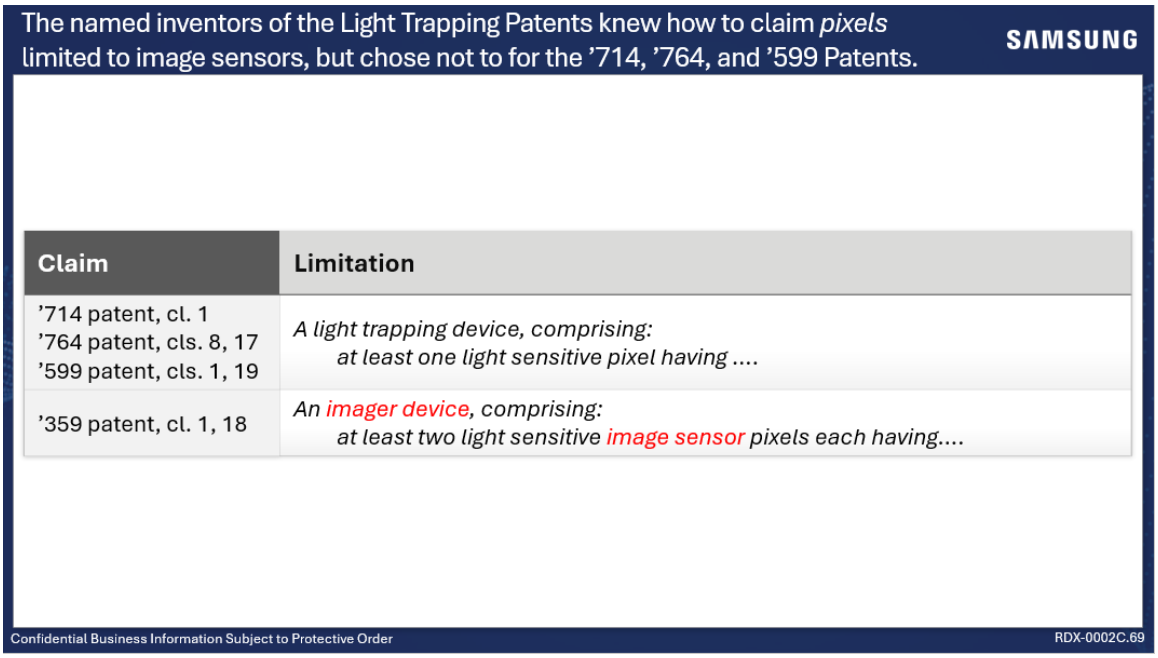
Q172 Are you aware of Dr. Mansoorian's argument that Yamada does not disclose *at least one light sensitive pixel*?

A172 Yes. I understand that, while Dr. Mansoorian admits Yamada "is used to capture light," he opines that it does not disclose *at least one light sensitive pixel* because "Yamada is not referring to a structure used in imaging devices," RX-0911C, ¶210; *see also* RX-0911C, ¶¶209-228. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.1147-1148.

First, the '714, '764, and '599 patents, which I use Yamada as a reference for, are not limited to image sensors. Second, even if they were limited, Yamada's light receiving section constitutes a light sensitive pixel that can be used in image sensors.

Q173 Why are the '714, '764, and '599 patents not limited to image sensors?

A173 First, the Light Trapping Patents are directed to light trapping devices and contemplate uses beyond just image sensors. *See* '714 patent, 1:42-46, 6:23-25 ("present disclosure is applicable to other optoelectronic devices such as solar cells, and that all such should be included in the present scope"). Second, as RDX-0002C.69 illustrates, the '714, '764, and '599 patents, unlike the '359 patent, only claim *light trapping devices comprising at least one light sensitive pixel*, as opposed to *[a]n imager device comprising: at least two adjacent light sensitive image sensor pixels*. *Compare* '714 patent, cl. 1, '764 patent, cls. 8, 17, 21, '599 patent, cls. 1, 19 *with* '359 patent, cls. 1, 18.



In my opinion, the fact that the patentee knew how to claim *light sensitive pixels* that were limited to image sensors, as evidenced by the related '359 patent, further shows that the applicants did not intend for the '714, '764, and '599 patents' *light sensitive pixels* to be limited to image sensors.

Q174 Why does Yamada's pixel constitute a light sensitive pixel capable of being used in an image sensor?

A174 Dr. Mansoorian opines at length, with limited cited support, that Yamada's PIN diode is not a *light sensitive pixel* used in an image sensor because image sensor pixels allegedly are normally pinned diodes, and that there is a substantial difference between PIN diodes and pinned diodes. I disagree. Despite his lengthy argument, Dr. Mansoorian does not actually assert that PIN diodes cannot be used in image sensors, and POSITAs would understand that image sensors can comprise a number of different dopant structures, including PIN diodes.

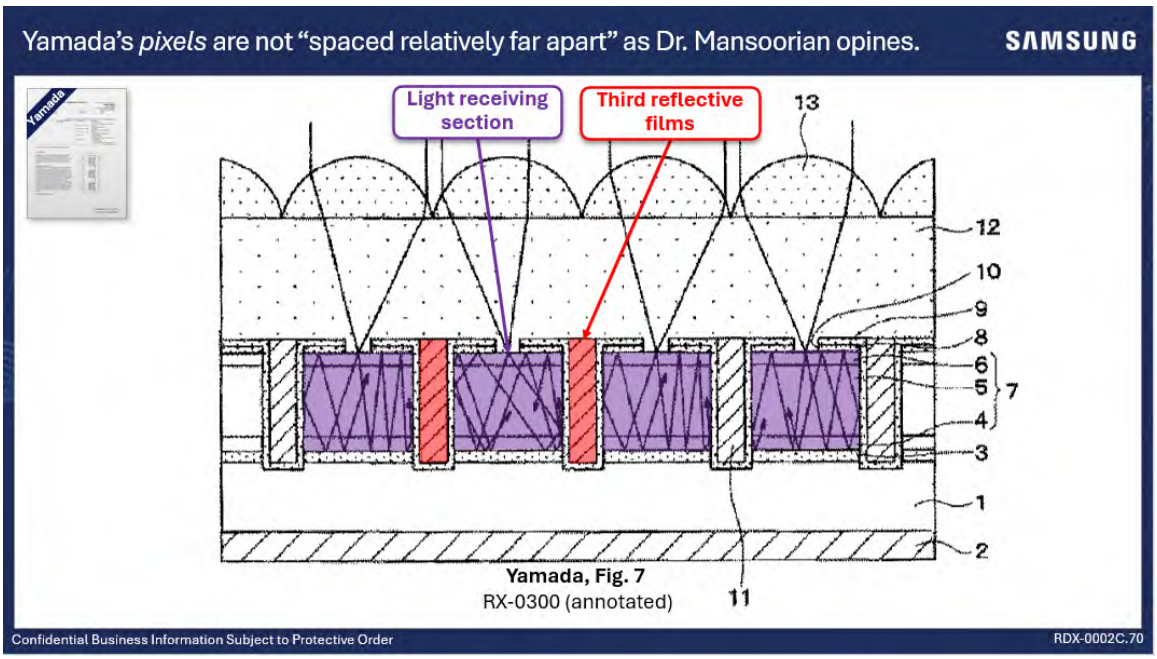
Indeed, POSITAs would understand that PIN diodes are capable of capturing images and being used in image sensors. Indeed, POSITAs would understand that CMOS active pixel image sensors (APS) were developed before pinned photodiodes and that it was not until several years after the introduction of APS devices that pinned photodiodes achieved widespread adoption. Accordingly, POSITAs would understand that image sensors are not limited to pinned photodiodes, and they could be formed using PIN diodes. Indeed, the specification envisions the use of PIN diodes. *E.g.*, 17:9-28.

Q175 Are you aware of Dr. Mansoorian's argument that Yamada does not disclose an image sensor because Yamada's pixels are spaced relatively far apart?

A175 Yes. Dr. Mansoorian opines that "[u]nlike the device of the '714 patent, which requires the pixels to be packed as closely as possible to increase device resolution, the PIN photodiodes

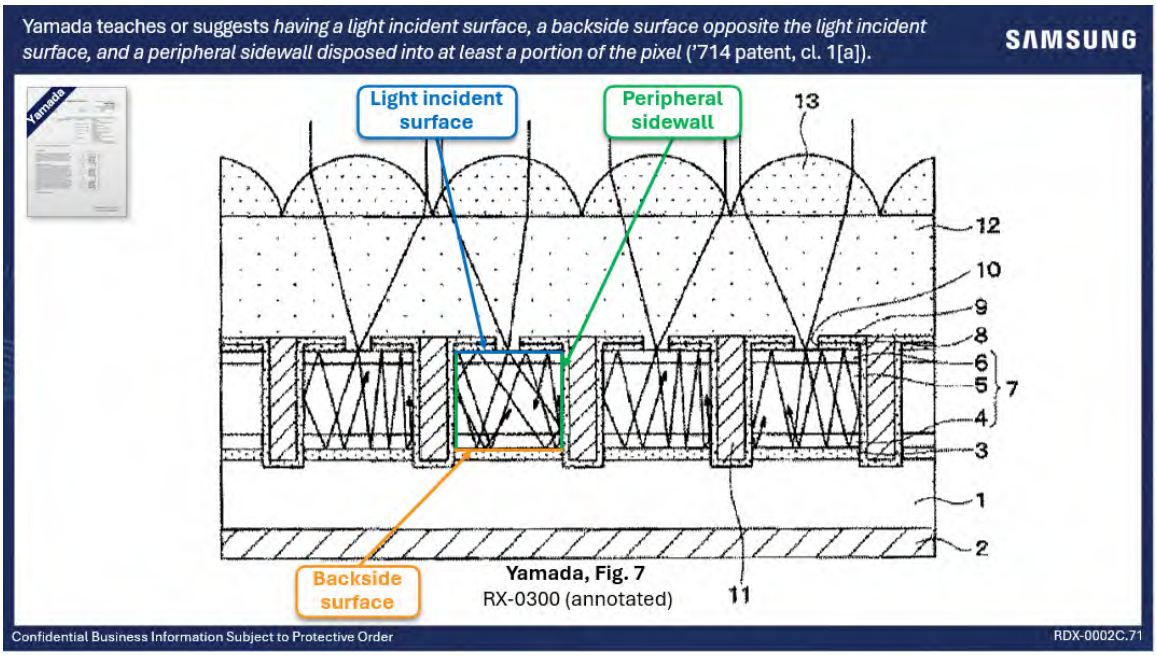
in Yamada are spaced relatively far apart." RX-0911C, ¶225. I note this theory was not presented in SiOnyx's contention1s, and I disagree. RX-0606C.1147-1148.

First, the Light Trapping Patents do not require pixels to be packed as closely as possible, indeed, the '714, '764, and '599 patents' claims are written to cover devices containing only one pixel. *E.g.*, '714 patent, cl. 1 ("at least one light sensitive pixel"). Second, Dr. Mansoorian's assertion that Yamada's pixels "are spaced relatively far apart," RX-0911C, ¶225, is speculation; nothing in Yamada indicates that it is drawn to scale and Yamada does not provide dimensions. Even if it was drawn to scale, Dr. Mansoorian appears to have based his opinions on Yamada Fig. 1, RX-0911C, ¶213, which has spaces between its pixels. However, my opinions are based on Yamada Figure 7. As RDX-0002C.70 illustrates, Figure 7 is configured such that the only thing separating neighboring pixels is third reflective film 11 and first insulating film 9, i.e., having pixels placed as closely as possible.



Q176 Limitation 1[a]'s second element is *having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel*. Have you formed an opinion regarding this element?

A176 Yes. I understand that the ALJ has construed *sidewall* to mean "trench wall," Order No. 36 at 20. As RDX-0002C.71 illustrates, each light receiving section 7 has a *light incident surface, a backside surface opposite the light incident surface*, and, to the extent the limitation is not indefinite, *a peripheral sidewall disposed into at least a portion of the pixel*, including at least under SiOnyx's proposed constructions of these terms.



Yamada teaches that each "light receiving element is provided with a first reflective film (3) arranged at a bottom surface of the light receiving section (7), a second reflective film (8) arranged opposing the first reflective film (3) at a front surface of the light receiving section (7) … [and] third reflective films (11) arranged at side surfaces of the light receiving section (7)." Yamada, [0009].

Q177 What is Yamada's *light incident surface*?

A177 As RDX-0002C.71 illustrates, the "front surface" is a *light incident surface*, as "light [that] is incident from the front surface … is converted into electrical energy" such that "detection is made of the light." Yamada, [0004].

Q178 What is Yamada's *backside surface*?

A178 The "bottom surface" opposes the front surface and therefore is a *backside surface opposite the light incident surface*, as RDX-0002C.71 illustrates.

Q179 What is Yamada's *peripheral sidewall*?

A179 Yamada's "side surfaces" are *peripheral sidewalls disposed into at least a portion of the pixel*, as they are on the sides of the light receiving element and are trench walls where the light receiving section 7 contacts the first insulating film 9 and third reflective film 11. As RDX-0002C.71 illustrates, Yamada's side surfaces run from the light receiving section 7's *light incident surface* to its *backside surface*—just like the '714 patent's peripheral sidewall 424.

Q180 Limitation 1[a]'s next part is *extending at least substantially around the pixel periphery*. Have you formed an opinion regarding this limitation?

A180 Yes. To the extent the limitation is not indefinite, Yamada satisfies it. I understand that the ALJ explained that "each instance of 'substantially' will need to have an individual construction tailored to the specific use," Order No. 36 at 34. Yamada teaches that "[e]ach of the embodiments is configured such that the entire side surfaces of the PIN photodiode 7 is covered by the third reflective films 11." Yamada, [0056]. Yamada further teaches that "the PIN photodiode 7 is surrounded by the … third reflective film 11, so when light is incident on the PIN photodiode 7, that light is reflected by … the third reflective films 11 so as to be confined within the PIN photodiode 7." Yamada, [0036].

2. Limitation 1[b]

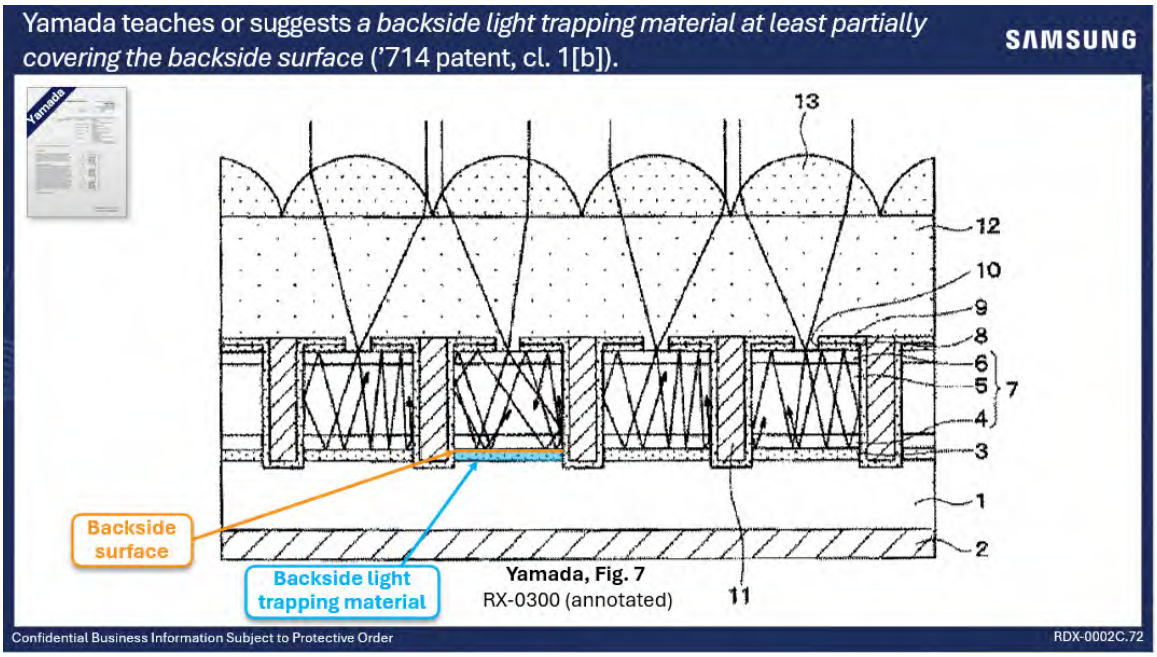
Q181 Limitation 1[b] is *a backside light trapping material at least partially covering the backside surface*. Does Yamada satisfy this limitation?

A181 Yes. Yamada teaches or suggests *a backside light trapping material at least partially covering the backside surface*. Dr. Mansoorian has not disputed this.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *light trapping material*. Yamada includes a *backside light trapping material*, including under either construction.

Q182 How does Yamada satisfy this limitation?

A182 As RDX-0002C.72 illustrates, Yamada's "first reflective film (3) [is] arranged at a bottom surface [*backside surface*] of the light receiving element (7)." Yamada, [0009]. Accordingly, it *at least partially covers the backside surface*.



First reflective film 3 constitutes a *light trapping material*. Yamada explains that "light … is reflected by the first reflective film (3) … so as to be confined within the light receiving section (7)," Yamada, [0010], and that [t]he first reflective film 3" has "a high reflectance of at least 99 percent," Yamada, [0022].

Q183 How does reflective film 3 constitute a *light trapping material* under the parties' proposed constructions?

A183 Reflective film 3 constitutes a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

3. Limitation 1[c]

Q184 Limitation 1[c] is *a peripheral light trapping material substantially covering the peripheral sidewall*. Does Yamada satisfy this limitation?

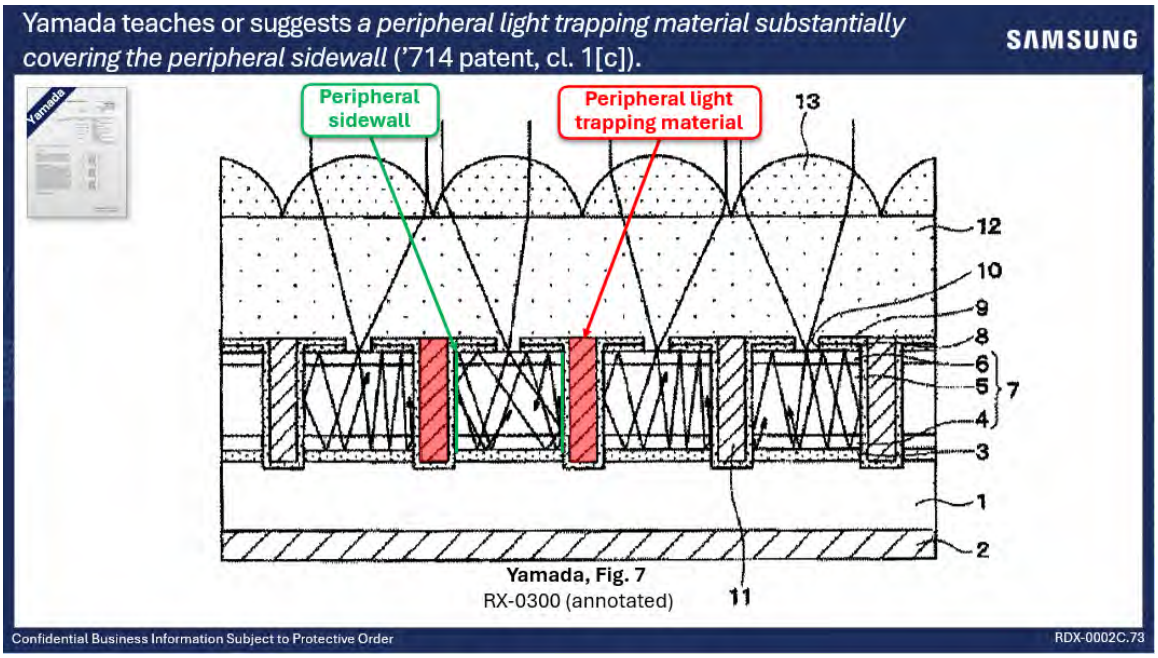
A184 Yes. Yamada teaches or suggests *a backside light trapping material at least partially covering the backside surface*. Dr. Mansoorian has not disputed this.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *light trapping material*. Yamada includes a *peripheral light trapping material*, including under either construction.

Q185 How does Yamada satisfy this limitation?

A185 As RDX-0002C.73 illustrates, Yamada's "third reflective films (11) [are] arranged at side surfaces of the light receiving section (7)," Yamada, [0009], and that "the side surfaces of the light receiving section (7) are covered by the third reflective films (11)," Yamada, [0010]. Accordingly, they *substantially cover[] the peripheral sidewall*.

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Third reflective films (11) constitute a *light trapping material*. Yamada explains that "light that enters the light receiving section (7) is reflected by … the third reflective films (11) so as to be confined within the light receiving section 7," Yamada, [0010], and that "since the sides of the PIN photodiode 7 are covered with the third reflective films 11, no incident light escapes from the sides of the PIN photodiode 7 and no optical crosstalk occurs between neighboring PIN photodiodes 7," Yamada, [0038].

Q186 How does reflective films 11 constitute a *light trapping material* under the parties' proposed constructions?

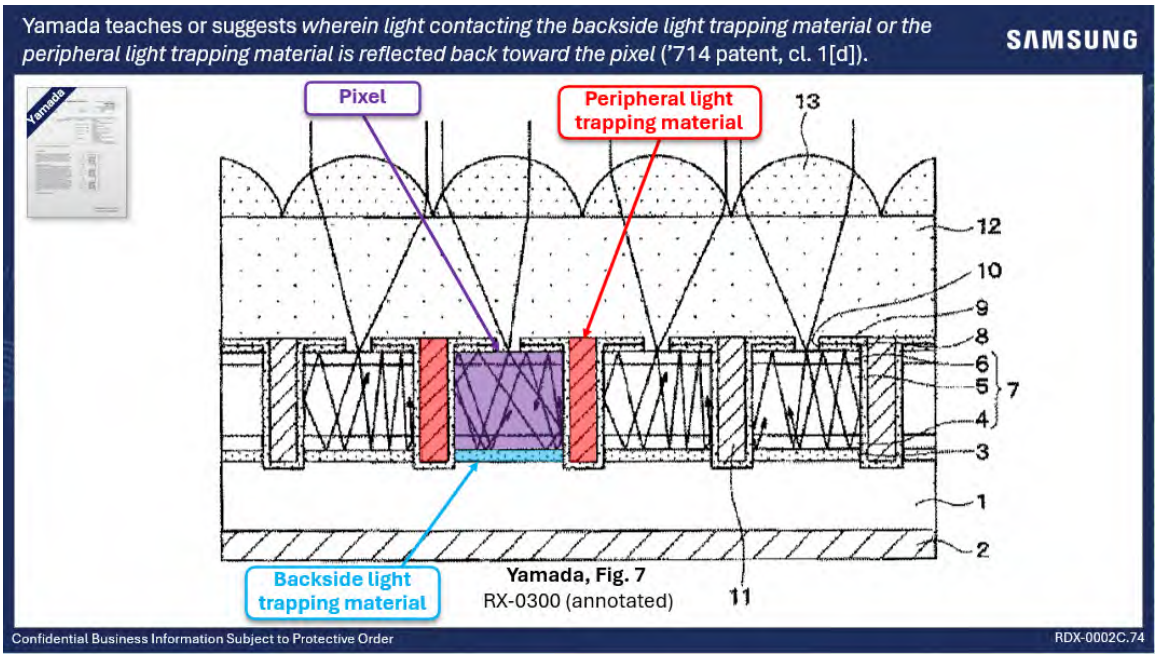
A186 Reflective films 11 constitutes a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

4. Limitation 1[d]

Q187 Limitation 1[d] is *wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel*. Does Yamada satisfy this limitation?

A187 Yes. As explained for limitations 1[b]-[c], Yamada teaches or suggests that *light contacting* both *the backside light trapping material* [and] *the peripheral light trapping material is reflected back toward the pixel*. Dr. Mansoorian has not disputed this.

As RDX-0002C.74 illustrates, Yamada teaches that "light that enters the light receiving section (7) is reflected by the first reflective films (3) … and the third reflective films (11) so as to be confined within the light receiving section 7." Yamada, [0010].



5. Limitation 1[e]

Q188 Limitation 1[e] is *wherein at least one of the backside light trapping material or the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials*. Have you formed an opinion regarding this limitation?

A188 Yes. Yamada teaches or suggests a *backside light trapping material* that *includes a high refractive index material sandwiched between two low refractive index materials*.

As explained in the Claim Construction Order, I understand that the ALJ has construed *high refractive index material* and *low refractive index material*, Order No. 36 at 31. Yamada's *high* and *low refractive index materials* satisfy this construction.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for limitation 1[e] as a whole. Yamada satisfies limitation 1[e], including under either construction.

Q189 How does Yamada's *backside light trapping material* satisfy this limitation?

A189 Yamada teaches that "first reflective film 3 [(*backside light trapping material*)] is composed of a semiconductor multilayer film," for example, "an $Al_xGa_{1-x}P$ semiconductor multilayer film." Yamada, [0021]. Yamada further teaches that "[t]he composition ratio X of $Al_xGa_{1-x}P$ is changed, as appropriate," such that "the semiconductor multilayer film is composed of alternating layers of semiconductor films with a low refractive index and a high refractive index." Yamada, [0021]. POSITAs would understand that choosing a ratio of X=1 results in aluminum phosphide (a low refractive index material, as contemplated by Yamada, with a refractive index of "2.75±0.1 at 0.5eV, to 3.10±0.1 at 2.8eV," RX-0297 (Adachi).153, or "about 2.8," at 530nm, RX-0293 (Liao), 5:11-12), and that choosing a

ratio of X=0 results in gallium phosphide (a high refractive index material, as contemplated by Yamada, with a refractive index of approximately 3.5 at 500nm, Schubert, Table 10.1).

Q190 Are you aware of Dr. Mansoorian's argument that POSITAs would not select values of X=0 and X=1?

A190 Yes. Dr. Mansoorian opines POSITAs would not understand Yamada's disclosed formula, $Al_xGa_{1-x}P$ to allow for values of X=0 and X=1, and that instead POSITAs "would have understood that 0<X<1, X is between, but not equal to 0 and 1," RX-0911C, ¶235; *see also* RX-0911C, ¶¶233-240. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.1147-1148.

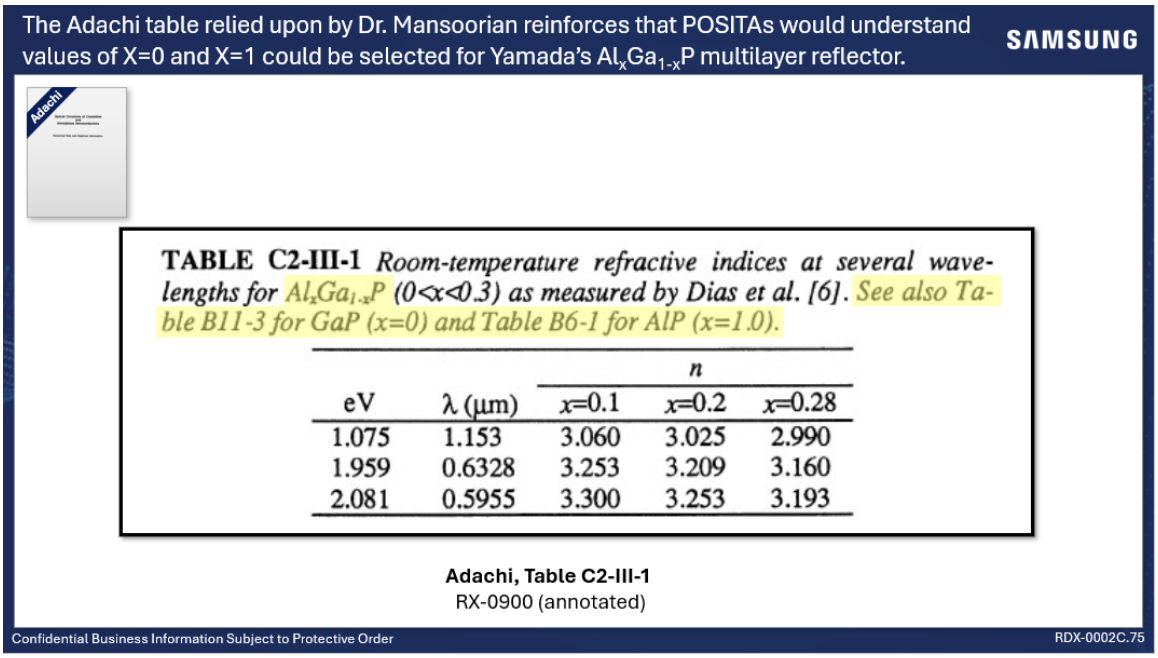
Q191 Why do you disagree?

A191 Nowhere does Yamada suggest that values of X=0 and X=1 cannot be chosen for the formulas it provides. Indeed, as Dr. Mansoorian notes, Yamada describes that the PIN photodiode 7 can be composed of "Si_xGe_{1-x}," Yamada, [0023], and gives "Si," i.e., selecting a value of X=1, as an example, Yamada, [0021]. That Yamada chose to give an example for its PIN photodiode, but no examples for its $Al_xGa_{1-x}P$ reflector, including no examples of 0<X<1, does not mean that Yamada teaches away from selecting values of X=0 and X=1.

Moreover, if anything, POSITAs would understand Yamada expressly teaches that such values should be chosen. Yamada teaches that "[t]he composition ratio X of $Al_xGa_{1-x}P$ is changed" such that "the semiconductor multilayer film is composed by alternating layers of semiconductor films with a low refractive index and a high refractive index," Yamada, [0021], and that it is "configured so that the light to be detected is reflected with a high reflectance of at least 99 percent," Yamada, [0022]. POSITAs would understand that DBRs, as Yamada describes, should have a "high index contrast,"—i.e., a large difference in refractive indices between the high and low refractive index material—to yield "high reflectivity." *E.g.*, Schubert, 172. POSITAs would understand aluminum phosphide (n≈2.75-3.10) and gallium phosphide (n≈3.5) results in the highest contrast of Yamada's low and high refractive index materials permissible in Yamada's $Al_xGa_{1-x}P$ reflector, and would further Yamada's goal of the reflector having "a high reflectance of at least 99 percent." Yamada, [0022].

Dr. Mansoorian's reliance on RX-0900 (Adachi, Full) to suggest that POSITAs would not select values of X=0 and X=1 further supports this point. As RDX-0002C.75 illustrates, the Adachi table Dr. Mansoorian relies upon also contemplates values of X=0 and X=1 for an $Al_xGa_{1-x}P$ reflector.

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Q192 Do aluminum phosphide and gallium phosphide satisfy the ALJ's constructions?

A192 Yes. The gallium phosphide layers in Yamada's first reflective film 3—which have a refractive index of approximately 3.5—constitute a *high refractive index material*, as they have a refractive index of greater than 2.1 (i.e., ~3.5) and a refractive index that is at least 0.2 greater than the *low refractive index material* (i.e., aluminum phosphide, which has a refractive index of ~2.75 or ~2.8). Likewise, the aluminum phosphide layers in Yamada's first reflective film 3—which have a refractive index of ~2.75 or ~2.8—constitute a *low refractive index material*, as they have a refractive index of at least 0.2 less than the *high refractive index material* (i.e., gallium phosphide, which has a refractive index of ~3.5). That is, the difference between gallium phosphide and aluminum phosphide's refractive indices is approximately 3.5–2.75=0.75 or 3.5–2.8=0.7.

Dr. Foty has relied upon bulk refractive index values in his infringement and technical DI opinions. *E.g.*, RX-0905C, ¶¶435-452. Accordingly, Yamada teaches or suggests this limitation under Dr. Foty's interpretation and application of this limitation. Moreover, it would have been obvious to manufacture the device such that the aluminum phosphide and gallium phosphide layers have refractive indices that are at least 0.2 different from each other given the values described.

Q193 What does Yamada teach or suggest about the layering of gallium phosphide aluminum phosphide?

A193 It would have been obvious to POSITAs that Yamada's disclosure of "alternating layers" of low and high refractive index materials in its first reflective film 3 is describing, or at a minimum suggesting, DBR—i.e., a structure formed by alternating materials with different refractive indices—which would consist of multiple pairs of low and high refractive index material. *See* Schubert, 171 ("A DBR is a multi-layer reflector consisting of typically 5–

50 pairs of two materials with different refractive indices."). Such DBRs would have at least one *high refractive index material* (gallium phosphide) *sandwiched between two low refractive index materials* (aluminum phosphide).

Q194 How does Yamada's $Al_xGa_{1-x}P$ reflector satisfy the parties' proposed constructions?

A194 Yamada's $Al_xGa_{1-x}P$ reflector satisfies the parties' proposed constructions, as the *high refractive index material* (gallium phosphide) is in contact with the *low refractive index material* (aluminum phosphide) on two opposing sides.

Q195 Are you aware of Dr. Mansoorian's argument that Yamada may not disclose a layer of gallium phosphide sandwiched between layers of aluminum phosphide?

A195 Yes. Dr. Mansoorian opines that, because Yamada "does not specify the number of layers nor … the arrangement," it is "unclear in Yamada the composition of the multilayer film" such that it may only have two or three layers not satisfying the claimed structure. I disagree. Dr. Mansoorian provides no support for his speculation why POSITAs would select such configurations. As explained, Yamada's disclosure of a "semiconductor multilayer film [] composed of alternating layers of … low refractive index and a high refractive index" materials, Yamada, [0021], is describing, or at least strongly suggesting, a DBR. It is obvious that Yamada's reflector would have at least four layers—and thus at least one *high refractive index material sandwiched between two low refractive index materials*—particularly given Yamada's teaching that the first reflective film 3 should have "a high reflectance of at least 99 percent." Yamada, [0022].

b. Claim 12

Q196 Let's turn to claim 12, which is *[t]he device of claim 1, further comprising a frontside light trapping material at least partially covering the light incident surface.* Does Yamada satisfy this claim?

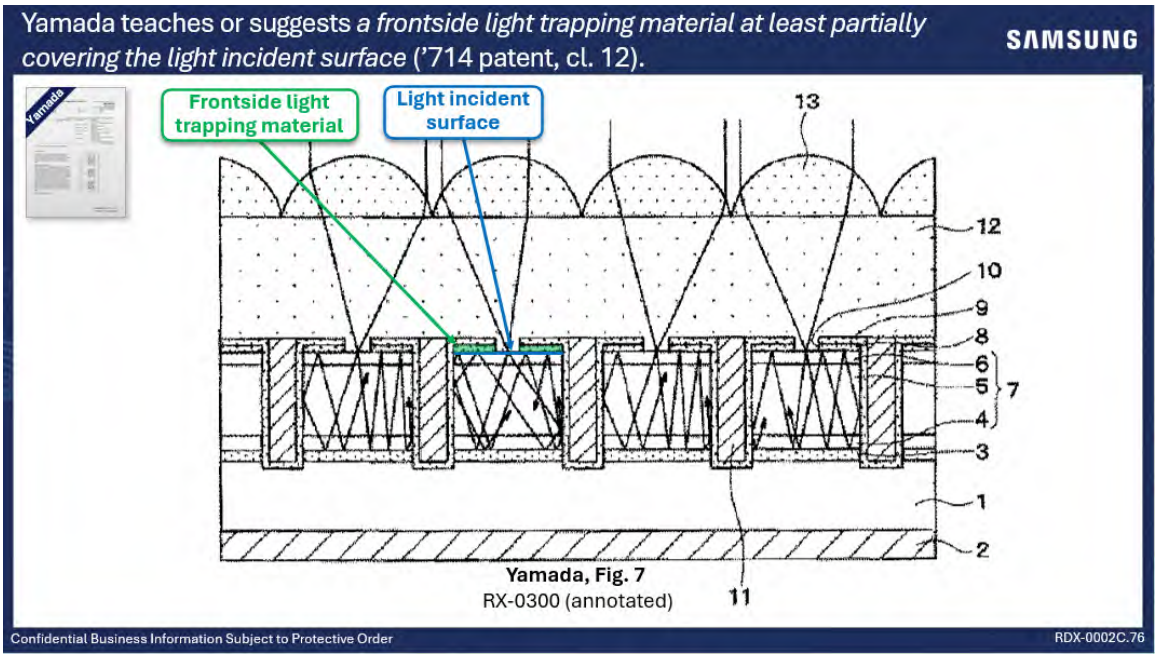
A196 Yes. Yamada teaches or suggests a *frontside light trapping material at least partially covering the light incident surface*. Dr. Mansoorian has not disputed this.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *light trapping material*. Yamada teaches or suggests a *frontside light trapping material*, including under either construction.

Q197 How does Yamada satisfy this limitation?

A197 As RDX-0002C.76 illustrates, Yamada includes a "second reflective film (8) [(*frontside light trapping material*)] arranged opposing the first reflective film (3) at a front surface of the light receiving section (7)." Yamada, [0009].

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Second reflective film 8 constitutes a *light trapping material*. Yamada explains that "light that enters the light receiving section (7) is reflected by … the second reflective film (8) … so as to be confined within the light receiving section (7)," Yamada, [0010], and that "second reflective film 8 … is configured so that the light to be detected is reflected with a high reflectance of at least 99 percent." Yamada, [0024].

Q198 How does second reflective film 8 constitute a *light trapping material* under the parties' proposed constructions?

A198 Second reflective film 8 constitutes a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

c. Claim 17

Q199 Let's turn to claim 17, which is *[t]he device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer*. Does Yamada satisfy this claim?

A199 Yes. Yamada teaches or suggests this limitation. Dr. Mansoorian has not disputed this.

As discussed for '714 patent (Ground 4), limitation 1[c], Yamada includes a *peripheral light trapping material*, i.e., "third reflective film (11)." Yamada explains that "third reflective film (11) can be composed of a metal" "such as Al." Yamada, [0012], [0026].

2. Ground 5: Yamada and Konno Render Obvious Claims 1, 12, and 17-18

Q200 Let's turn to your Ground 5 opinions. Can you please summarize your Ground 5 opinions?

A200 In my opinion Yamada and Konno render obvious claims 1, 12, and 17-18. As explained for Ground 4, Yamada anticipates, or at least renders obvious, claims 1, 12 and 17. Those opinions are equally applicable to my Ground 5 opinions regarding Yamada and Konno, which further render obvious claim 18.

a. Claim 18

Q201 Let's turn to claim 18, which is *[t]he device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface*. Have you formed an opinion regarding this claim?

A201 As explained regarding the Terms Remaining in Dispute, I understand that Samsung proposed the term *sloped surface at the pixel device interface* is indefinite, and that SiOnyx proposed it has its plain and ordinary meaning, and to the extent a construction is required, it means sloped trench wall or sloped backside surface.

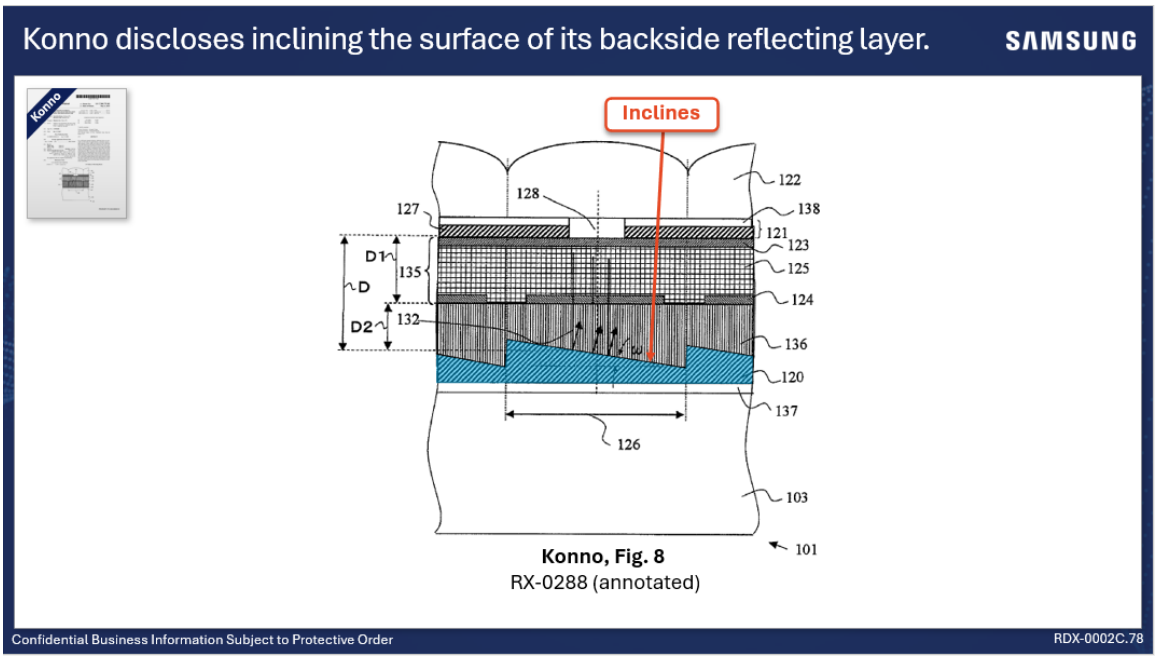
It is unclear what is meant by *a sloped surface at the pixel device interface*, in particular, what is meant by a *pixel device interface*. There is no discussion in the specification of a *pixel device interface*, and the term lacks antecedent basis, such that the specification fails to inform POSITAs, with reasonable certainty, of the claim's scope.

To the extent the limitation is not indefinite, Yamada and Konno render obvious a *backside light trapping material* that *has a sloped surface at the pixel device interface*.

Q202 Assuming the claim is not indefinite, do Yamada and Konno satisfy this claim?

A202 Yes. As RDX-0002C.78 illustrates, Konno's Figure 8 embodiment includes a second reflecting layer 120 constituting a *backside light trapping material* that has *a sloped surface*. In particular, Konno teaches that "second reflecting layer 120," can have "incline[s]." Konno, 15:36-38.

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Konno teaches that such inclined surfaces can be used to redirect light to other reflectors on the pixel's surface and thereby increase sensitivity. *See* Konno, 15:38-40 ("Incident photons are reflected by this reflecting surface to the first reflecting layer 121 on one side of the light entrance window 128."), 15:46-50 ("the inclination of the reflecting surface is designed so that most of the photons which entered at the light entrance window 128 except for those absorbed by the photoelectric conversion film 125 should reach the first reflecting layer 121").

Q203 Why would POSITAs use a sloped surface in Yamada?

A203 Using a *backside light trapping material* with an inclined surface in Yamada to improve Yamada's efficiency in a similar manner would have been obvious. That is, POSITAs would have been motivated to form Yamada's first reflective film 3 with a sloped surface. This modification would result in Yamada having a *backside light trapping material* (first reflective film 3) that has *a sloped surface.*

Q204 Why would POSITAs have been motivated to use a sloped surface in Yamada?

A204 POSITAs would have understood that such an inclined surface could be used to redirect light to Yamada's third reflective films (11) or second reflective film (8) to increase Yamada's efficiency.

Q205 Would POSITAs reasonably have expected success in making this modification?

A205 Yes. POSITAs reasonably would have expected success in making this modification. For example, such an inclined surface could be implemented in Yamada during the manufacturing steps shown for a substantially similar embodiment of Yamada shown in Figure 2(a).

Q206 Are you aware that Dr. Mansoorian opines that POSITAs would not be motivated to make this combination because POSITAs would not see a need to improve Yamada?

A206 Yes. Dr. Mansoorian opines that Yamada already "trap[s] the vast majority of the incident light" such that POSITAs "would not see a need to improve Yamada's design," RX-0911C, ¶¶260-261. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.165-167.

Unmodified, Yamada's first reflective film 3 (backside reflector) has flat surface, such that light which hits it perpendicularly (or nearly perpendicularly) will reflect off it perpendicularly (or nearly perpendicularly) back through Yamada's aperture (through-hole 10) instead of being reflected off Yamada's second reflective films 8 or third reflective films 11. Sloping Yamada's first reflective film 3 alleviates this issue and would result in a greater percentage of light impinging upon Yamada's first reflective film 3 to also hit Yamada's second reflective films 8 or third reflective films 11, as Konno teaches. Konno, 15:46-50 ("the inclination of the reflecting surface is designed so that most of the photons which entered at the light entrance window 128 except for those absorbed by the photoelectric conversion film 125 should reach the first reflecting layer 121").

Q207 Are you aware that Dr. Mansoorian opines that POSITAs would not be motivated to make this combination because adding a sloped surface would necessitate changes to Yamada's microlens?

A207 Yes. Dr. Mansoorian opines that "Yamada's microlens is configured to focus light so that it does not reflect light back through the aperture," and "is configured to function with a flat backside reflective surface," such that sloping Yamada's backside surface would require changes to the microlens. RX-0911C, ¶¶262-263. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.165-67.

Q208 Why do you disagree?

A208 First, POSITAs would understand that sloping Yamada's backside surface does not necessitate changes to Yamada's lens, as Yamada's lens is designed to direct light through its aperture (through-hole 10). *See* Yamada, [0009] (microlens is "configured so as to gather light at the exposed portion of the front surface of the light receiving section (7)," such that light "is made to enter the light receiving section (7) from the exposed portion of the front surface of the light receiving section [(Yamada's through-hole 10)]").Nowhere does Yamada disclose, nor suggest, that its microlens is designed to focus light so that it does not reflect back through the aperture or configured to function with a flat backside surface. Instead, it is configured to direct light through its aperture (through-hole 10).

Second, even if such a modification to Yamada's lens was necessary, modifying it would be well within POSITAs' skill, who would "have would have at least a bachelor's degree in electrical engineering, materials science, or physics (or an equivalent degree) and at least two years of experience in optoelectronics." Order No. 36 at 19. Indeed, the Light Trapping Patents do not provide for dimensions or configurations for the microlens; accordingly, it

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is unclear how POSITAs would be able to make and use the Light Trapping Patents' alleged invention if they could not modify a microlens.

Q209 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination as it would decrease the size of Yamada's pixel?

A209 Yes. Dr. Mansoorian opines that POSITAs would not make this combination as "implementing a sloped surface would decrease the volume of Yamada's PIN photodiode, minimizing its light absorptive capability." RX-0911C, ¶263. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.165-67.

First, POSITAs could understand that Yamada's first reflective film 3 could be formed with a sloped surface without decreasing the size of Yamada's pixel. Dr. Mansoorian assumes first reflective film 3 must slope upwards into Yamada's pixel, however, POSITAs would recognize that it could also slope downwards into Yamada's semiconductor substrate 1 (while also possibly adjusting Yamada's third reflective films 11 to prevent crosstalk) which would increase the size of Yamada's pixel.

Second, even assuming first reflective film 3 must slope upwards into Yamada's pixel as Dr. Mansoorian opines, POSITAs would still be motivated to make this combination. As explained, sloping first reflective film 3 results in light being redirected to Yamada's third reflective films (11) or second reflective film (8) so as to increase Yamada's efficiency. Specifically, it would trap additional light within Yamada's pixel by redirecting light that would ordinarily escape through Yamada's aperture to its reflective films, causing multiple reflections which increase the pathlength of light traveling within Yamada's pixel and allowing for the pixel to be made smaller while retaining sensitivity.

C. Haddad188-based Grounds

Q210 Let's turn to your Haddad188-based opinions. Can you please summarize your anticipation and obviousness opinions about the '714 patent based on Haddad188?

A210 My Haddad188-based opinions are based on a single ground, Ground 6, which is that Haddad188 and Schubert render obvious claims 1, 12, and 17-18.

1. Ground 6: Haddad188 and Schubert Render Obvious Claims 1, 12, and 17-18

a. Claim 1

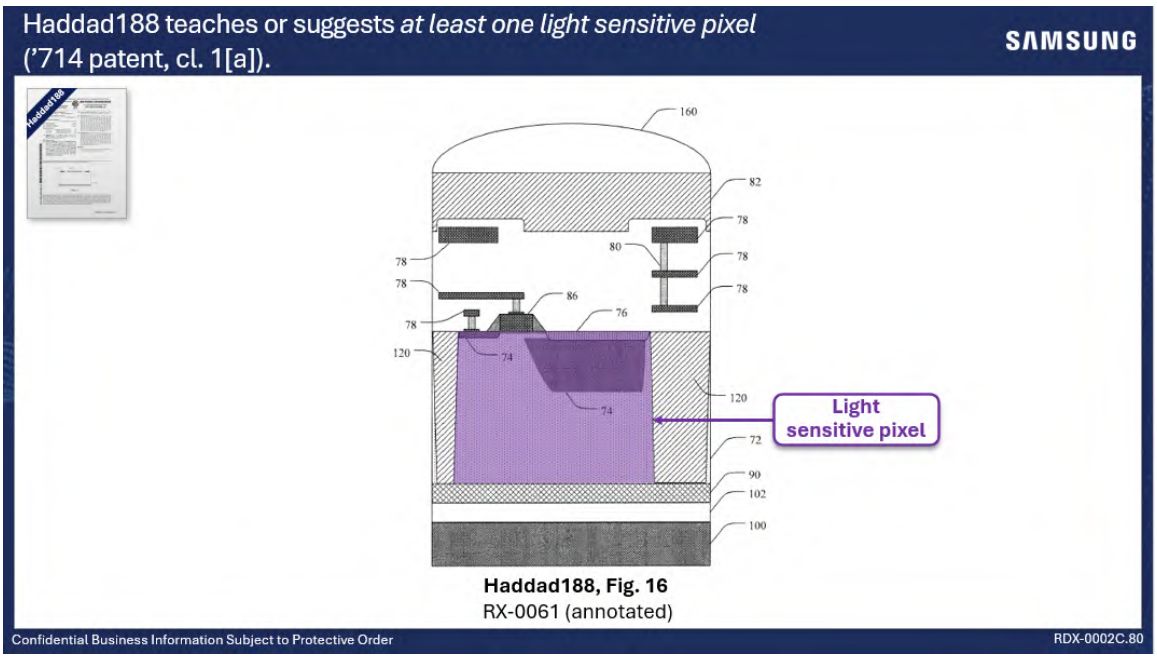
1. Limitation 1[a]

Q211 Let's start with claim 1. Claim 1's first limitation, 1[a], is relatively long, so let's take it in parts. The first element is *at least one light sensitive pixel*. Have you formed an opinion regarding this element?

A211 Yes. Haddad188 teaches or suggests *at least one light sensitive pixel*. Dr. Mansoorian has not disputed this.

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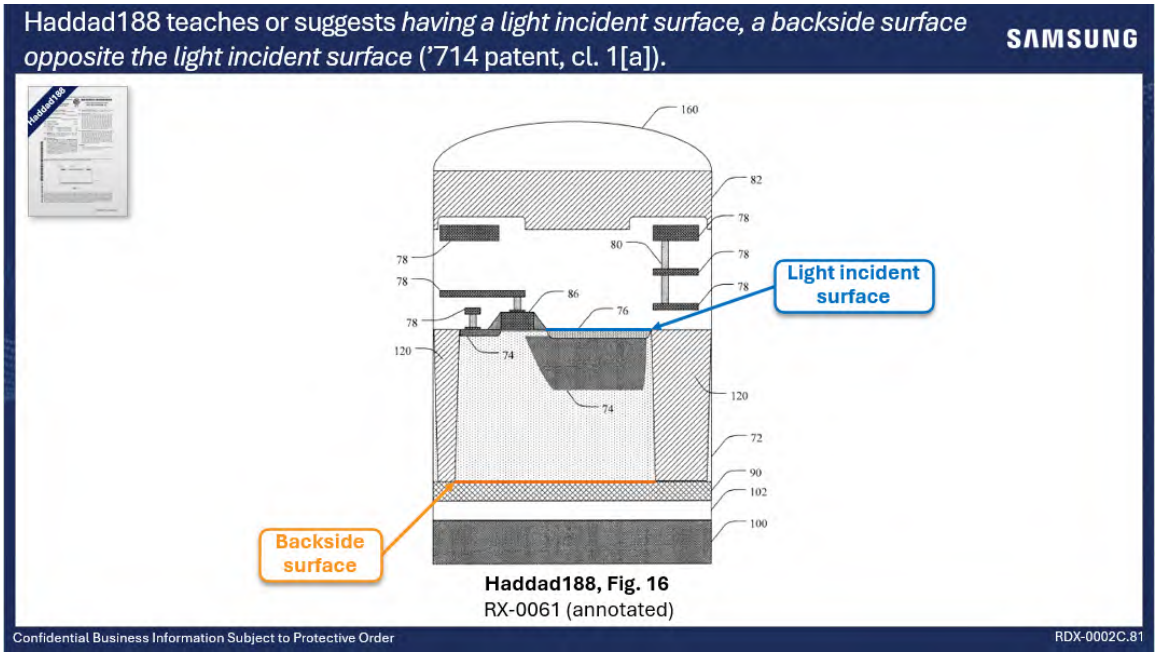
I understand that the ALJ construed *light sensitive pixel* to have its plain and ordinary meaning. Order No. 36 at 27. Haddad188 includes a *light sensitive pixel* under its plain and ordinary meaning, which I consider to be portions of a device that convert light into electrical signals. As RDX-0002C.80 illustrates, Haddad188 discloses "a schematic view of a photosensitive pixel device." Haddad188, 4:21-22. Haddad188 teaches that photosensitive imagers, like the one RDX-0002C.80 illustrates, "include photodiodes or pixels that are capable of absorbing electromagnetic radiation within a given wavelength range." Haddad188, 8:23-24. Haddad188 further teaches that "photosensitive imager[s] can include multiple photosensitive pixels." Haddad188, 8:19-20. Haddad188's photosensitive pixel device includes a semiconductor substrate 72, including doped regions 74 and highly doped regions 76, such that "highly doped region 76 can be formed on or near the doped region to create a pinned diode," i.e., a photodiode. Haddad188, 22:13-14. *See also* Haddad188, 8:5-22



Accordingly, as RDX-0002C.80 illustrates, Haddad188 discloses a *light sensitive pixel* which includes the semiconductor substrate 72, doped regions 74, and highly doped regions 76. *See* Haddad188, 8:15-19 ("photosensitive pixel can include a semiconductor substrate having multiple doped regions forming at least one junction"); *see also* JX-0027C (McKee), 97:12-18 (explaining that, when discussing Haddad188, Fig. 1, the photodiode is formed from two doped regions and a silicon collection layer). Each photosensitive pixel includes a photodiode capable of detecting light.

Q212 Limitation 1[a]'s second element is *having a light incident surface, a backside surface opposite the light incident surface*. Have you formed an opinion regarding this element?

A212 Yes. As RDX-0002C.81 illustrates, each pixel in Haddad188 has a *light incident surface* and a *backside surface opposite the light incident surface*. Dr. Mansoorian has not disputed this.



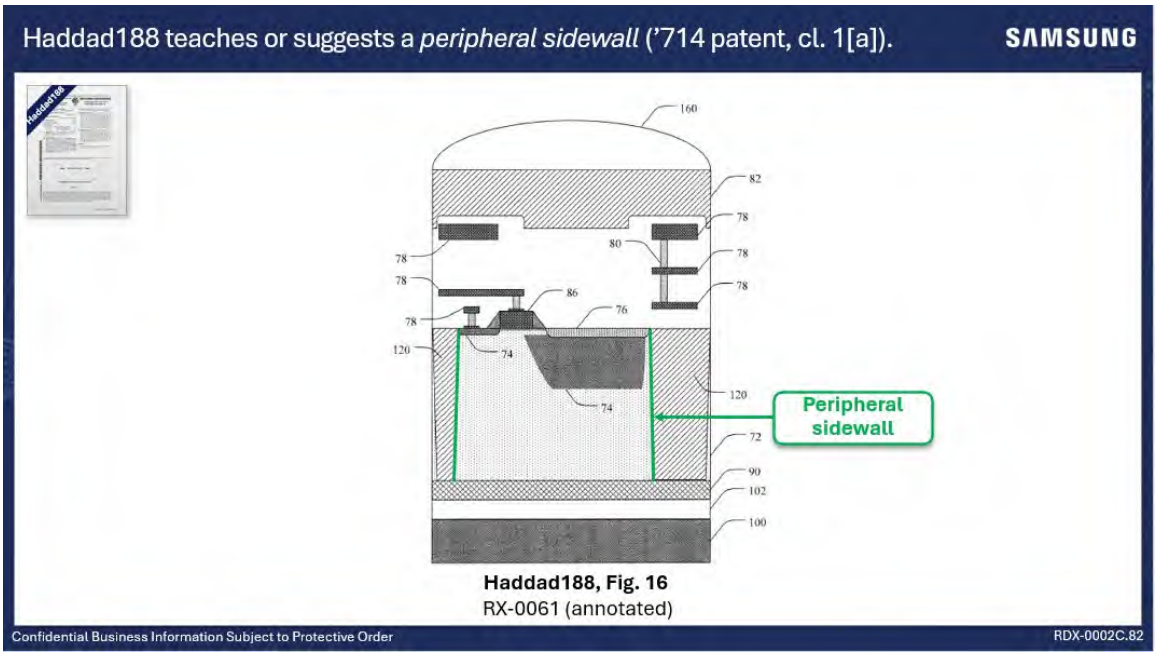
Haddad188 teaches that light passes through lens 160, through aperture 164 (not depicted in Figure 16), and through the top surface of the semiconductor substrate (i.e., the *light incident surface*). *See* Haddad188, 25:4-11. Haddad188 further teaches that textured region 90 and reflecting layer 102 are coupled to the bottom surface (i.e., the *backside surface*) of semiconductor substrate 72. *See* Haddad188, 25:6-9; *see also* Haddad188, 20:22-23 ("reflective layer can be located on the semiconductor substrate opposite the incoming electromagnetic radiation"). As RDX-0002C.81 illustrates, semiconductor substrate 72's top surface is a *light incident surface* and its bottom surface is *a backside surface opposite the light incident surface*.

Q213 Limitation 1[a]'s third part is *a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery*. Have you formed an opinion regarding this element?

A213 Yes. In view of Dr. Foty's interpretation and application of this term wherein it is allegedly satisfied because the *peripheral sidewall* defines the pixel's bounds, and to the extent it is not indefinite (as I will explain), Haddad188 teaches or suggests this limitation.

Q214 Does Haddad188 include a *peripheral sidewall*?

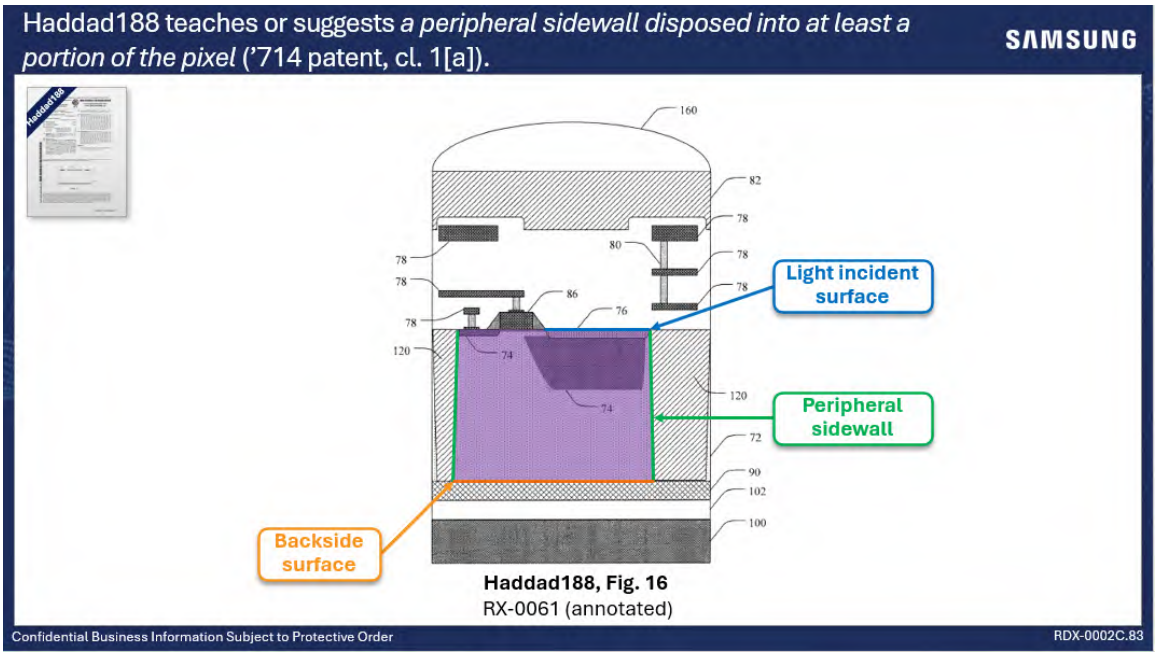
A214 Yes. I understand that the ALJ construed *sidewall* to mean trench wall. Order No. 36 at 20. As RDX-0002C.82 illustrates, each pixel includes a *peripheral sidewall* (trench wall) where the semiconductor substrate 72 meets trench isolation 120 (i.e., the side trench wall of trench isolation 120).



Haddad188's description of Figure 16 is silent as to trench isolation 120's function. However, Haddad188 explains elsewhere that the "trench isolation layer can be configured to reflect electromagnetic radiation, in some cases until it is absorbed, thereby increasing the effective absorption length of the device." Haddad188, 24:5-9; *see also* Haddad188, 22:25-29. Haddad188 further explains that "[t]rench isolation elements can maintain pixel to pixel uniformity by reducing optical and electrical crosstalk." Haddad188, 22:23-24.

Q215 Is Haddad188's *peripheral sidewall disposed into at least a portion of the pixel*?

A215 In view of Dr. Foty's interpretation and application of this term and to the extent it is not indefinite, yes. As RDX-0002C.83 illustrates, the *peripheral sidewall* runs from Haddad188's *light incident surface* to its *backside surface*—just like the '714 patent's peripheral sidewall 424.



Q216 Does Haddad188's *peripheral sidewall extend[] at least substantially around the pixel periphery*?

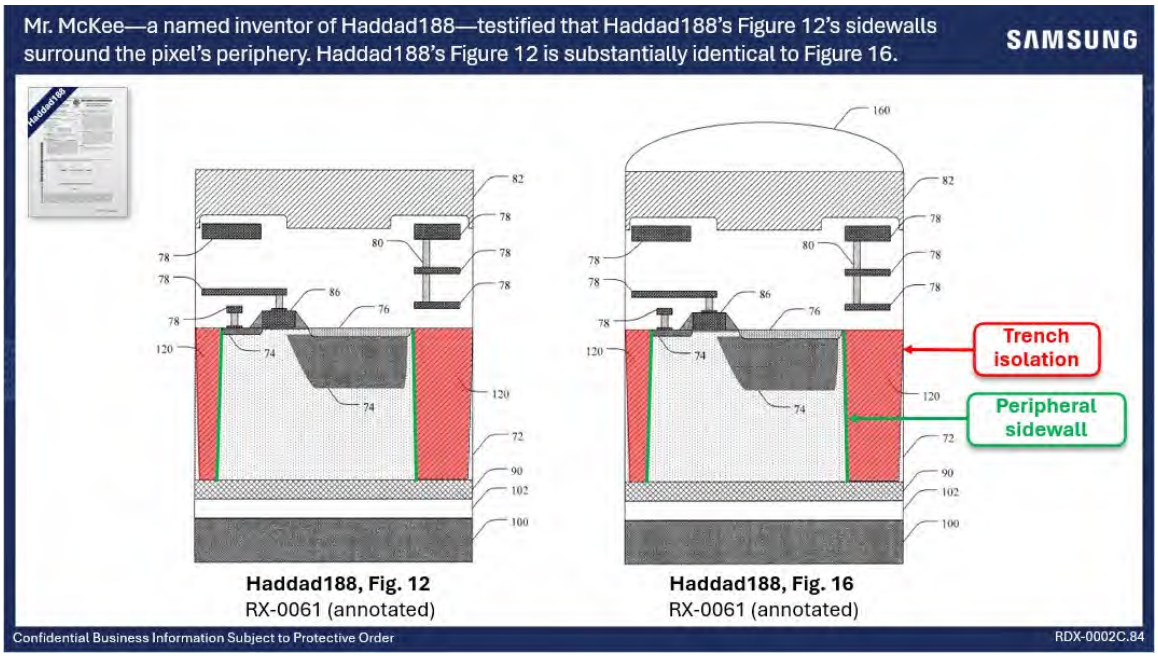
A216 In view of Dr. Foty's interpretation and application of this term and to the extent it is not indefinite, yes. I understand that the ALJ explained that "each instance of 'substantially' will need to have an individual construction tailored to the specific use," Order No. 36 at 34. Haddad188's peripheral sidewall *extend[s] at least substantially around the pixel periphery*. This is consistent with the role of trench isolation 120, for example, in reducing optical and electrical crosstalk. POSITAs would understand that the further the trench isolation 120 extends around the periphery, the more that light and charge will be prevented from moving between pixels, and the less of a chance that crosstalk will occur.

Q217 Does Haddad188 include a plan view of its image sensor?

A217 No. Like the Light Trapping Patents, Haddad188 does not include a plan view showing the extent to which trench isolation 120 surrounds the pixel; however, Haddad188 explains that trench isolation 120 is used to "maintain pixel uniformity by reducing optical and electrical crosstalk," i.e., to ensure that light and charge cannot move from one pixel to another. Haddad188, 22:23-24. POSITAs would have understood that increased coverage results in decreased optical and electrical crosstalk. Moreover, Haddad188 explains that its invention can include "a semiconducting photosensitive imager [that] can be a three or four transistor active pixel sensor (3T APS or 4T APS)." Haddad188, 8:27-28. POSITAs would understand that such APS (active pixel sensor) devices are associated with row and column addressing which is only used in two-dimensional pixel arrays. In such arrays, it would be advisable for trench isolation to extend *at least substantially*, if not completely, around the pixel periphery to optically and electrically isolate the pixels from one another. Therefore, it would have been at least obvious to POSITAs to make the trench isolation extend *at least*

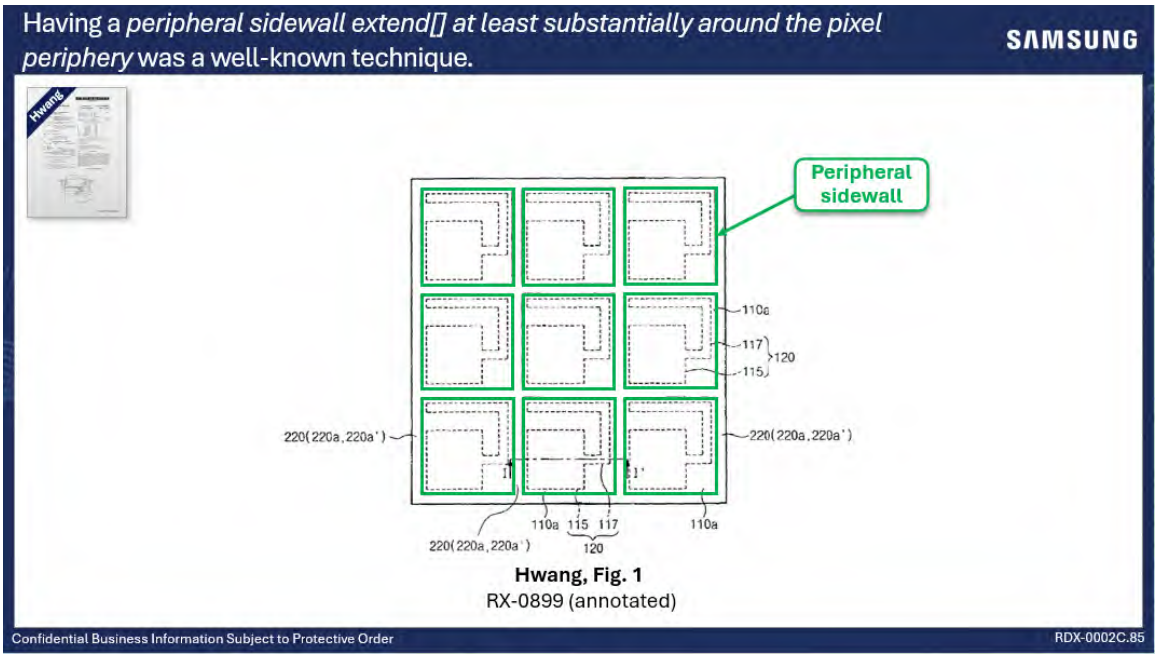
substantially, if not completely, around the pixel periphery to "maintain pixel to pixel uniformity by reducing optical and electrical crosstalk." Haddad188, 22:23-24.

Indeed, Mr. McKee—a named inventor of Haddad188—admitted that Haddad188's trench isolation as depicted in Figure 12—which, as RDX-0002C.84 illustrates, has substantially similar deep trench isolation to Figure 16, even sharing the same identifier 120—would surround the pixel's periphery by going all the way around it to isolate the pixel. JX-0027C (McKee), 110:7-115:22.



Q218 Are there any other reasons why you think Haddad188 teaches or suggests a *peripheral sidewall extending at least substantially around the pixel periphery*?

A218 Yes. Having peripheral sidewalls extend completely—which encompasses *at least substantially—around the pixel periphery* was a well-known technique used in similar devices. For example, as previously discussed, Hwang discloses an image sensor with a *peripheral sidewall extending* completely (i.e., *at least substantially*) *around the pixel periphery*, as RDX-0002C.85 illustrates. *See also* Hwang, 6:15-17 ("sidewall multi-layered reflection layer 220 encloses the side walls of the pixel semiconductor patterns 110*a*").

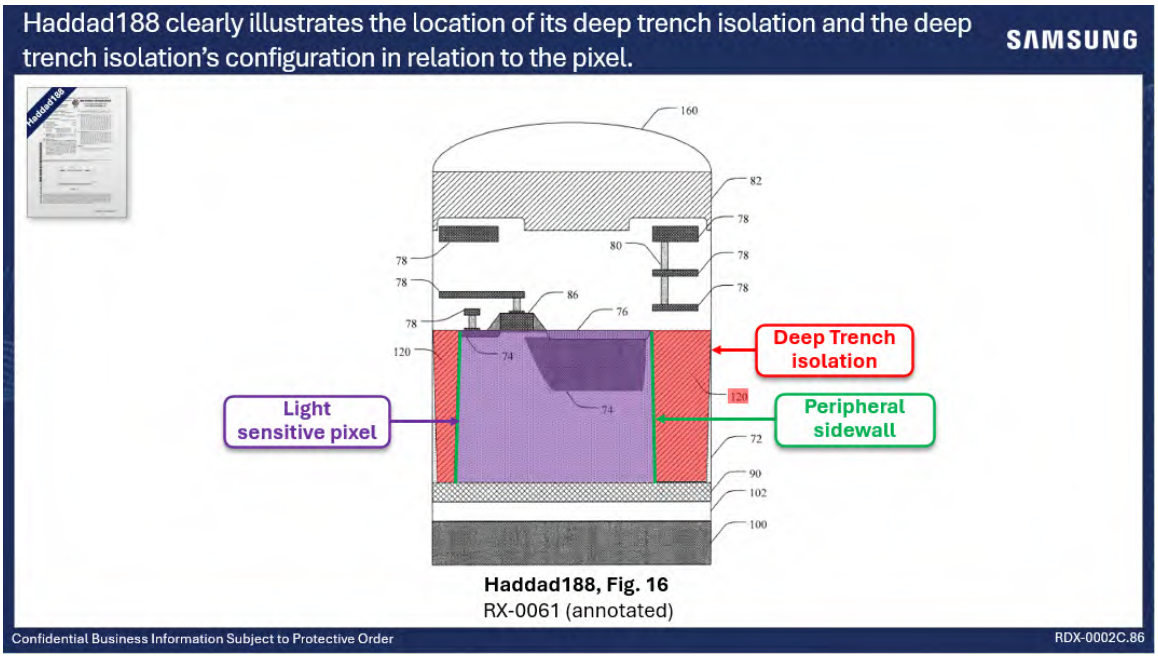


Likewise, as previously discussed, Yamada similarly discloses that each of its embodiments are "configured such that the entire side surfaces of the PIN photodiode 7 is covered by the third reflective films 11." Yamada, [0056]. Consistent with Haddad188's teachings, Yamada discloses that "the PIN photodiode 7 is surrounded by … third reflective film 11, so when light is incident on the PIN photodiode 7, that light is reflected by … third reflective films 11 so as to be confined within PIN photodiode 7." Yamada, [0036]. *See also* Roy, Fig. 3; RX-0896 (Roy283), 5:53-54 ("each photosite is completely surrounded by trenches").

Q219 Are you aware of Dr. Mansoorian's argument that Haddad188 does not disclose a *peripheral sidewall … extending at least substantially around the pixel periphery*?

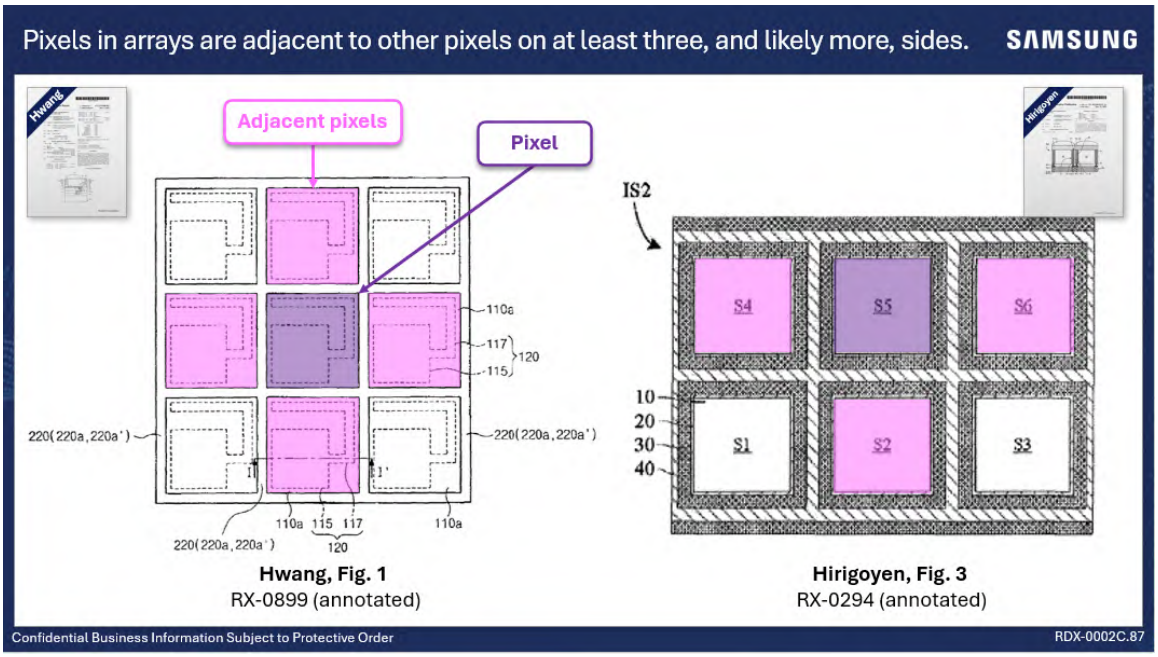
A219 Yes. However, Dr. Mansoorian only makes this argument for '764 patent, limitations 8[a], 17[a], and 21[a], not '714 patent limitation 1[a]. As I will explain, these limitations are identical, so I will address Dr. Mansoorian's argument here for convenience.

Dr. Mansoorian's assertion that this limitation is not satisfied because "[n]owhere does Haddad188 provide information as to the location of any deep trench isolation structure let alone their configuration in relation to the pixel," RX-0911C, ¶421, is incorrect. As explained, Haddad188 identifies its deep trench isolation as element 120, *see* Haddad188, 24:2-3, and as RDX-0002C.86 illustrates, such deep trench isolation 120 is clearly identified in relation to Haddad188's pixel.



Q220 Does Dr. Mansoorian make any other arguments why Haddad188 does not disclose this limitation?

A220 Dr. Mansoorian also opines that POSTIAs "would not have readily understood that merely increasing the coverage of the sidewall results in decreased optical and electrical crosstalk, as increasing the surface area of the DTI structures can instead lead to increased parasitic capacitance between pixels." RX-0911C, ¶421. I disagree. First, crosstalk is a separate issue from parasitic capacitance, and, as Dr. Mansoorian agrees, there are other steps that can be taken to address parasitic capacitance. RX-0911C, ¶421. However, to reduce crosstalk in a pixel array—which Dr. Mansoorian admits Haddad188 is describing—POSITAs would understand the DTI layers extend at least *substantially around the pixel periphery*. This is because in such arrays, at least one pixel is adjacent to other pixels on at least three, and likely more, sides, as RDX-0002C.87 illustrates. As Haddad188's cross-sectional Figure 16 illustrates, Haddad188 already discloses trench isolation 120 surrounding two sides (left and right) of the pixel. Accordingly, it would be obvious to POSITAs that, since Haddad188 already uses DTI, it should extend at least *substantially around the pixel periphery* (i.e., on the sides not shown in the cross section) in order to isolate the pixel from other, adjacent pixels, and that doing so would outweigh any additional risks of further defects.



2. Limitation 1[b]

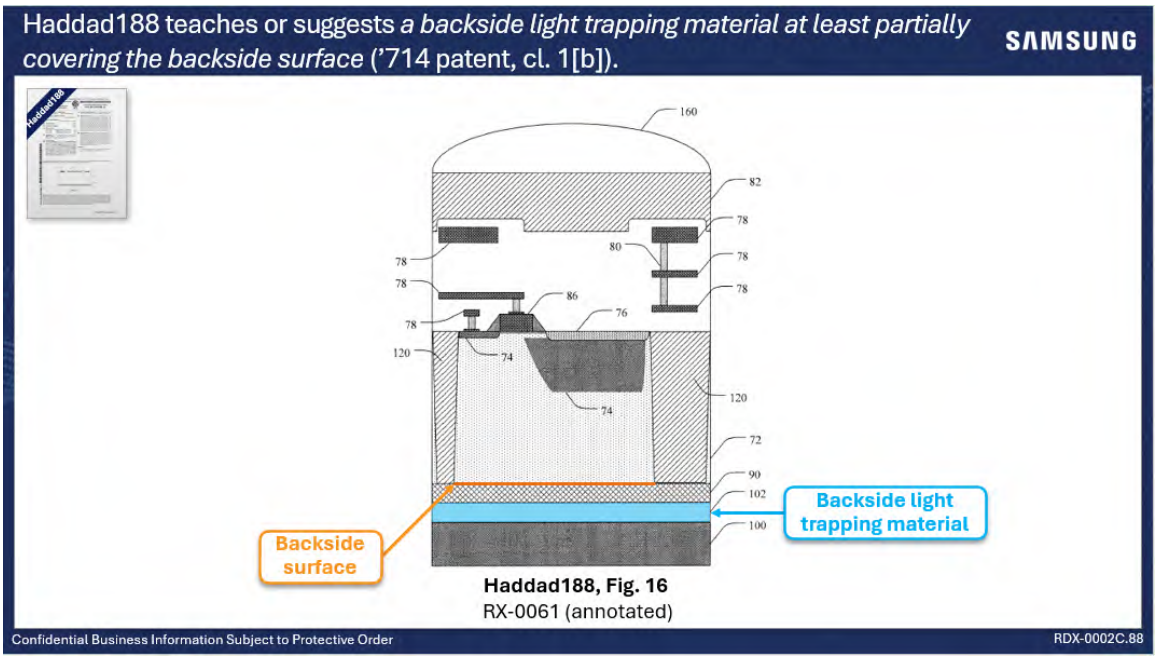
Q221 Limitation 1[b] is *a backside light trapping material at least partially covering the backside surface*. Does Haddad188 satisfy this limitation?

A221 Yes. Haddad188 teaches or suggests *a backside light trapping material at least partially covering the backside surface*. Dr. Mansoorian has not disputed this.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *light trapping material*. Haddad188 includes a *backside light trapping material*, including under either construction.

Q222 How does Haddad188 satisfy this limitation?

A222 As RDX-0002C.88 illustrates, Haddad188 includes a "reflecting layer 102" which is "coupled to the semiconductor substrate 72 opposite the lens." Haddad188, 25:6-7.



Reflecting layer 102 constitutes a *light trapping material*. Haddad188 teaches that the "textured region 90 … and reflecting layer 102 … provide diffusive scattering and reflection of incident electromagnetic radiation that passes through the semiconductor substrate," Haddad188, 25:6-9, and that the purpose of reflecting layer 102 is reflecting "electromagnetic radiation passing through [*sic*] the semiconductor substrate and the textured region … back into the semiconductor substrate." Haddad188, 20:20-23. Haddad188 further teaches that "the reflective layer material can be any reflective material" "such as silver, aluminum, and the like." Haddad188, 23:25-26. A solid metal layer, as Haddad188 discloses, reflects more light than it transmits and the region is arranged so that light is reflected back into the semiconductor substrate. *See, e.g.*, Schubert, Table 10.2.

Q223 How does reflecting layer 102 constitute a *light trapping material* under the parties' proposed constructions?

A223 Reflecting layer 102 constitutes a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

3. Limitation 1[c]

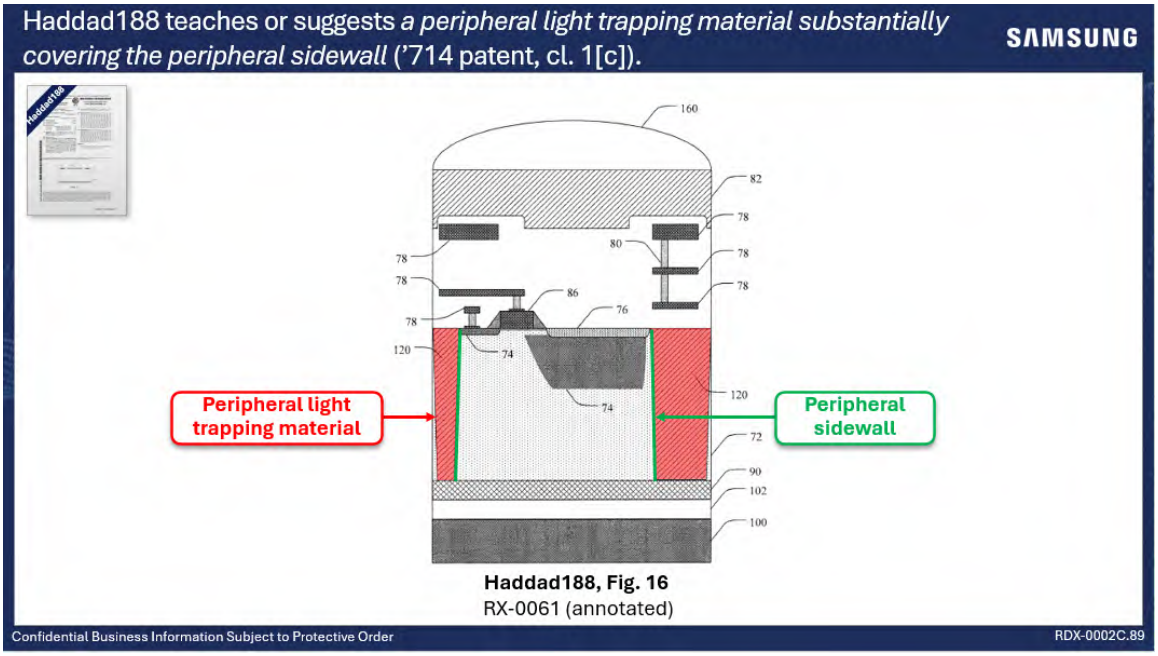
Q224 Limitation 1[c] is *a peripheral light trapping material substantially covering the peripheral sidewall*. Does Haddad188 satisfy this limitation?

A224 Yes. Haddad188 teaches or suggests *a backside light trapping material at least partially covering the backside surface*. Dr. Mansoorian has not disputed this.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *light trapping material*. Haddad188 includes a *peripheral light trapping material*, including under either construction.

Q225 How does Haddad188 satisfy this limitation?

A225 As RDX-0002C.89 illustrates, Haddad188's FSI imager includes "trench isolation 120."



Trench isolation 120 constitutes a *light trapping material*. Haddad188 explains that it "can be configured to reflect incident electromagnetic radiation" back into the pixel. Haddad188, 24:7-8. Haddad188 explains that "[t]rench isolation can include various materials, including, without limitation, dielectric materials, reflective materials, conductive materials, light diffusing features, and the like." Haddad188, 22:25-27. Haddad188 further explains that "[t]hese trench isolation regions can be configured to reflect incident light until it is absorbed, thereby increas[ing] the effective absorption length of the device." Haddad188, 22:27-30; *see also* Haddad188, 24:1-9.

Q226 How does trench isolation 120 constitute a *light trapping material* under the parties' proposed constructions?

A226 Trench isolation 120 constitutes a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

Q227 Does Haddad188's trench isolation 120 *substantially cover[] the peripheral sidewall*?

A227 Yes. As RDX-0002C.89 illustrates, Haddad188's *peripheral light trapping material* (trench isolation 120) completely *cover[s] the peripheral sidewall*, and therefore, *substantially cover[s]* it.

4. Limitation 1[d]

Q228 Limitation 1[d] is *wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel*. Does Haddad188 satisfy this limitation?

A228 Yes. Haddad188 teaches or suggests that *light contacting* both *the backside light trapping material* and *the peripheral light trapping material is reflected back towards the pixel*. Dr. Mansoorian has not disputed this.

Haddad188 teaches that the purpose of reflecting layer 102 (*backside light trapping material*) is to reflect "electromagnetic radiation passing through [*sic*] the semiconductor substrate … back into the semiconductor substrate." Haddad188, 20:20-23. Likewise, Haddad188 teaches that "trench isolation regions [(*peripheral light trapping material*)] can be configured to reflect incident light until it is absorbed, thereby increas[ing] the effective absorption length of the device." Haddad188, 22:27-30.

5. Limitation 1[e]

Q229 Limitation 1[e] is *wherein at least one of the backside light trapping material or the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials*. Have you formed an opinion regarding this limitation?

A229 Yes. Haddad188 and Schubert render obvious a *peripheral light trapping material* that *includes a high refractive index material sandwiched between two low refractive index materials*.

As explained in the Claim Construction Order, I understand that the ALJ has construed *high refractive index material* and *low refractive index material*, Order No. 36 at 31. Haddad188, as modified by Schubert, has *high* and *low refractive index materials* that satisfy this construction.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for limitation 1[e] as a whole. Haddad188 and Schubert satisfy limitation 1[e] , including under either construction.

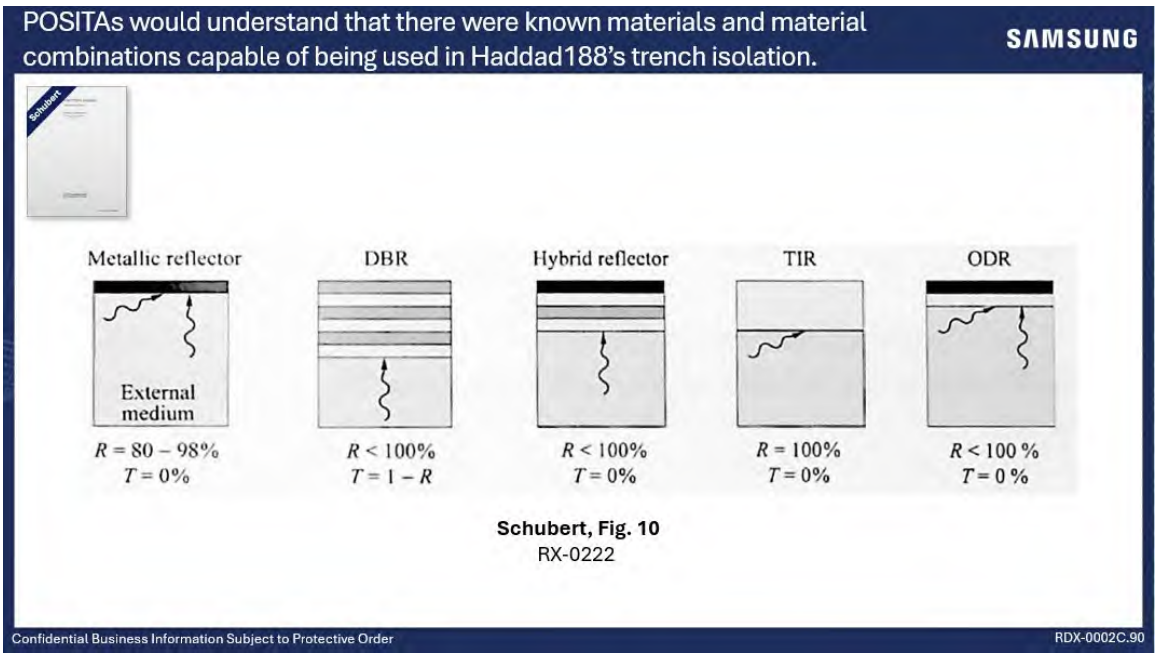
Q230 What is Haddad188's *peripheral light trapping material* formed of?

A230 Haddad188 is broad in its disclosure of what trench isolation 120 (*peripheral light trapping material*) can be made from: "trench isolation can include dielectric materials, reflective materials, conductive materials, and combinations thereof, including textured regions and other light diffusing features." Haddad188, 24:5-7. For example, Haddad188 explains that "[t]hese trench isolation regions can be configured to reflect incident light until it is absorbed, thereby increas[ing] the effective absorption length of the device." Haddad188, 22:27-30.

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Q231 What materials would POSITAs consider using in Haddad188's trench isolation?

A231 POSITAs would understand that there were known materials and material combinations capable of being used in such a trench isolation, each having its own benefits and considerations. For example, Mr. McKee—a named inventor of Haddad188—described different materials, such as dielectrics or metals that can be used as materials to optically isolate a pixel. JX-0027C, 82:13-83:8. As another example, Schubert discusses the "[d]ifferent types of reflectors" to use in optoelectronic devices, i.e., "a metallic reflector, distributed Bragg reflector (DBR), hybrid reflector, total internal reflector (TIR), and a triple-layer omni-directional reflector (ODR)," Schubert, 163, as RDX-0002C.90 illustrates.



As a common example of a DBR, Schubert teaches alternating layers of silicon (which Schubert discloses as having a refractive index of 3.51) and SiO_2 (which Schubert discloses as having a refractive index of 1.46). Schubert, 177.

Q232 Would a Si/SiO_2 DBR satisfy the ALJ's constructions?

A232 Yes. Si/SiO_2 DBRs comprise a *high refractive index material* (silicon) *sandwiched between two low refractive index materials* (SiO_2). Silicon constitutes a *high refractive index material*, as Schubert discloses silicon having a refractive index greater than 2.1 (i.e., 3.51) and a refractive index that is at least 0.2 greater than the *low refractive index material* (i.e., SiO_2, which has a refractive index of 1.46). Likewise, SiO_2 constitutes a *low refractive index material*, as Schubert discloses SiO_2 having a refractive index of less than 2.1 (i.e., 1.46) and a refractive index that is at least 0.2 less than the *high refractive index material* (i.e., silicon, which has a refractive index of 3.51).

Dr. Foty has relied upon bulk refractive index values in his infringement and technical DI opinions. *E.g.*, RX-0905C, ¶¶435-452. Accordingly, Haddad188, as modified by Schubert,

renders obvious this limitation under Dr. Foty's interpretation and application of this limitation. Moreover, it would have been obvious to manufacture the device such that the silicon and SiO_2 layers have refractive indices that are at least 0.2 different from each other given the values described. In particular, Schubert discloses the refractive indices of silicon and SiO_2 as used in a DBR.

Q233 Would a Si/SiO_2 DBR have a *high refractive index material sandwiched between two low refractive index materials*?

A233 Yes. Si/SiO_2 DBRs would have a *high refractive index material* (silicon) *sandwiched between two low refractive index materials* (SiO_2), including under either party's proposed construction. DBRs are "multi-layer reflector[s] consisting of typically 5–50 pairs of two materials with different refractive indices," Schubert, 171, which would result in at least one silicon layer (*high refractive index material*) being *sandwiched between two* SiO_2 layers (*low refractive index material*).

Q234 How does the Si/SiO_2 DBR satisfy the parties' proposed constructions?

A234 The Si/SiO_2 DBR would have at least one silicon layer (*high refractive index material*) being in contact with (and in between) SiO_2 layers (*low refractive index material*) on two opposing sides.

Q235 Why would POSITAs use a Si/SiO_2 DBR in Haddad188?

A235 Using a Si/SiO_2 DBR, as Schubert teaches, in Haddad188's trench isolation 120 (*peripheral light trapping material*), such that Haddad188 includes a *high refractive index material* (silicon), *sandwiched between two low refractive index materials* (SiO_2). Indeed, Schubert teaches that Si/SiO_2 is a known DBR that "yield[s] high reflectivity." Schubert, 172. Moreover, POSITAs would understand that isolation elements (i.e., trench isolation 120) comprised of a metal thinly insulated from the photodiode exhibit increased dark current. Mori, [0008]. ("Furthermore, metal is embedded in the silicon material…. [t]his also increases crystal defects in the silicon layer and increases charges generated when dark, resulting in a decrease in sensitivity."); *see also* Mori, [0007]. POSITAs would have realized that a known solution to reduce dark current was to replace such metal isolation elements with Si/SiO_2 partitions. For example, Mori explains that:

> [I]n the partition part 163 in the solid-state imaging device of the present embodiment, a silicon layer 175 is embedded in a partition groove….
>
> The partition part 163 also has a side SiO_2 film 177 formed on the bottom and side surfaces of the partition groove. Thereby, crystal defects occurring on the side surfaces of the separation trenches can be reduced, and a decrease in sensitivity caused by charges generated when dark can be suppressed.

Mori, [0029]-[0030].

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Q236 Would POSITAs have reasonably expected success in making this combination?

A236 Yes. POSITAs would have reasonably expected success in using a Si/SiO_2 DBR as Haddad188's trench isolation 120 such that it includes at least one layer of silicon sandwiched between layers of SiO_2. As explained for limitation 1[b], trench isolation 120 is used to reflect light back into the pixel. Schubert teaches that Si/SiO_2 DBRs "yield high reflectivity," Schubert, 172, and "high contrast materials Si ($\bar{n} \approx 3.5\ at\ \lambda = 1\ \mu m$) and SiO_2 ($\bar{n} \approx 1.46$) are natural candidates for [omnidirectional reflectors]," Schubert, 181; *see also* Schubert Fig. 10.8 (illustrating that a Si/SiO_2 reflector with four pairs having a 100% reflectance at approximately 1-14μm), 170 ("DBR's reflectivity can be increased by increasing the number of reflector pairs"). In fact, Si/SiO_2 reflectors were used as light trapping materials in similar known image sensors before the Light Trapping Patent's priority date. *See, e.g.*, Hwang, 9:25-30, 10:2-5; Mori, [0029]-[0030]; Suzunaga, [0035].

Accordingly, using a Si/SiO_2 DBR would have been nothing more than a simple substitution of a Si/SiO_2 DBR for Haddad188's trench isolation 120 to obtain predictable results (e.g., high reflectivity, reduced dark current, and omnidirectional characteristics). As Schubert teaches, Si/SiO_2 DBRs "yield high reflectivity," Schubert, 172, including up to 100% reflectance, Schubert, 170. Haddad188, as modified by Schubert, would have a *peripheral light trapping material*.

Q237 How does the Si/SiO_2 reflector used in Haddad188 in view of Schubert constitute a *light trapping material* under the parties' proposed constructions?

A237 The Si/SiO_2 reflector would constitute a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

Q238 Are you aware of Dr. Mansoorian's argument that Haddad188 does not need improvement?

A238 Yes. Dr. Mansoorian opines that POSITAs reading Haddad188's disclosure "would not see a need to improve Haddad188's design, as it already says that it reflects incident radiation and increases absorption length." RX-0911C, ¶270. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.196-198.

As discussed, and as Dr. Mansoorian notes, "Haddad188 only discloses [a] nonlimiting list of potential trench-filling materials." RX-0911C, ¶273. Thus, while Haddad188 teaches its trench isolation reflects incident radiation and increases absorption length, POSITAs would need to look to other sources—such as Schubert—to select the proper material(s) to use for Haddad188's trench isolation in order to use Haddad188's device.

Q239 Are you aware of Dr. Mansoorian's argument that POSITAs would not be motivated to modify Haddad188 based on Schubert because Schubert is non-analogous art?

A239 Yes. Dr. Mansoorian opines that POSITAs would not combine Haddad188 and Schubert because Schubert is an excerpt from a textbook on LEDs. RX-0911C, ¶272. I disagree. As I explained in the Overview of Schubert, Schubert's discussion of reflectors is pertinent to

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image sensors, given both the similarities between LEDs and image sensors and that reflectors in both are designed to reflect incident photons.

Q240 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination because Haddad188 only contemplates using a single material?

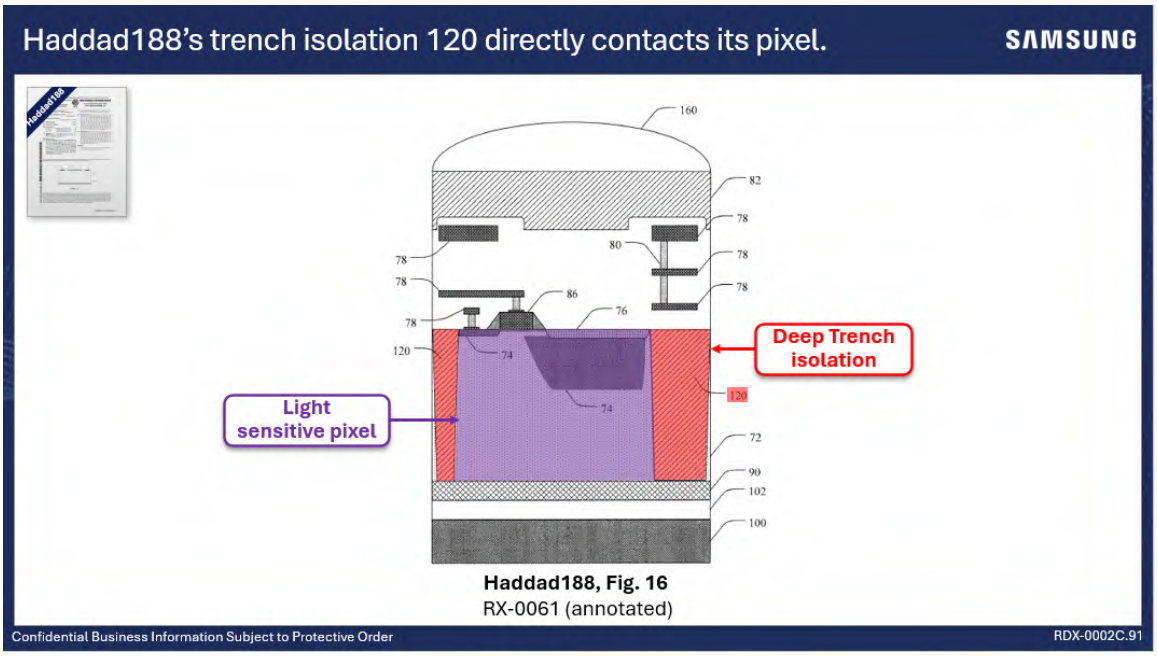
A240 Yes. Dr. Mansoorian opines that "Haddad188 only discloses a nonlimiting list of potential trench-filling materials from which one candidate material can be selected" and that "changing the trench fill material from the single material contemplated in Haddad188 to Schubert's DBR reflector" would be difficult. RX-0911C, ¶273; *see also* RX-0911C, ¶278. I disagree. First, nothing in Haddad188 suggests that its disclosure is limited to using a single material; indeed, Haddad188 contemplates "combinations thereof" of various materials, i.e., using multiple materials:

> Various types of trench isolation are contemplated and any such isolation is considered to be within the present scope…. Trench isolation can include dielectric materials, reflective materials, conductive materials, and combinations thereof….

Haddad188, 24:1-6; *see also* Haddad188, 24:4:27-32 ("disclosure is not limited to particular structures, process steps, or materials disclosed herein"). Second, Haddad188's contemplation of "[t]he trench isolation can include various materials, including, without limitation, dielectric materials, reflective materials, conductive materials, light diffusing features, and the like," Haddad188:22-25-27, encompasses the Si/SiO_2 layer added in this combination.

Moreover, Haddad188 contemplates filling the trench with a "conductive material," e.g., a metal. *See* Haddad188, 22:25-27. As RDX-0002C.91 illustrates, Haddad188's deep trench isolation 120 directly contacts its pixel. POSITAs would understand that such a metal-filled trench would require an insulating layer between it and the pixel—i.e., require that Haddad188's trench be filled with at least one other material in addition to the metal to prevent the metal from being in direct contact with the pixel and potentially creating a short circuit.

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Q241 Are you aware of Dr. Mansoorian's argument that Haddad188's trench isolation may not be in contact with the pixel?

A241 Yes. Dr. Mansoorian speculates that "[n]othing in Haddad188 states that the trench isolation should be in contact with the pixel," and that "there is no indication that [] Figure [16] is intended to be drawn to scale or that it is intended to illustrate how a pixel would be designed with a conductive material in the trench." RX-0911C, ¶278. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.196-198.

While Figure 16 is not drawn to scale, it does clearly show Haddad188's deep trench isolation 120 abutting its pixel, as RDX-0002C.91 illustrates.

Q242 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination because Schubert allegedly only discloses planar DBRs with 5-50 pairs of layers?

A242 Yes. Dr. Mansoorian opines that Schubert "merely discloses the general definition of a DBR reflector ('a multi-layer reflector consisting of typically 5-50 pairs of two materials with different refractive indices')." RX-0911C, ¶273. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.196-198.

POSITAs would recognize that, while Schubert said DBRs "consist[] of typically 5-50 pairs," Schubert, 171, DBRs can be suitable reflectors using fewer pairs—particularly if using a high-contrast DBR like a Si/SiO_2 reflector. For example, Schubert teaches that 100% reflectance at approximately 1-1.4µm can be achieved while only using four pairs of Si/SiO_2. Schubert, Fig. 10.8. Additionally, as explained for '714 patent (Ground 1), claim 1, Hwang teaches that its Si/SiO_2 sidewall multi-layered reflection layer 220 reflects incident light back into Hwang's pixel, and that it can be made with as few as three layers (i.e., 1.5 pairs). *E.g.*, Hwang, 9:28-30, 10:2-5, 10:28-35, 12:4-7.

Q243 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination because Schubert allegedly only disclosures planar DBRs?

A243 Yes. Dr. Mansoorian opines that Schubert "only considers implementation of a 'DBR reflector' within the planar context where layers of materials are stacked from the bottom (substrate side) to the top (epitaxial side)." RX-0911C, ¶273. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.196-198.

First, POSITAs would understand that Schubert's disclosure of DBRs stacked from the substrate side to the top epitaxial side refers to DBRs made of crystalline materials that are grown using epitaxy, which is irrelevant to Si/SiO_2 DBRs—or any DBR using a non-crystalline (e.g., SiO_2 or glass) material for one of its layers. POSITAs would thus understand that this disclosure does not preclude Si/SiO_2 reflectors from being placed in vertical trenches, as evidenced by other references using such reflectors in their trench isolation elements. *E.g.*, Hwang, Mori, Roy, Suzunaga.

Second, as explained, POSITAs would understand that Si/SiO_2 reflectors are omnidirectional reflectors, capable of reflecting light at a wider range of angles. *See* Schubert, 181 ("high contrast materials Si ($\bar{n} \approx 3.5\ at\ \lambda = 1\ \mu m$) and SiO_2 ($\bar{n} \approx 1.46$) are natural candidates for [omnidirectional reflectors]").

Q244 Are you aware of Dr. Mansoorian's argument POSITAs would not make this combination because forming a Si/SiO_2 reflector in Haddad188 would be too difficult?

A244 Yes. Dr. Mansoorian opines that "filling a trench with a single material is much different than [] filling a trench with multiple layers, let alone 5-50 pairs of layers," and that "precisely filling the trench with one material with minimal defects is a challenge, and altering the process to include multiple layers of materials would exacerbate the difficulties of fabrication." RX-0911C, ¶273. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.196-198.

First, as explained, a POSITA would understand that fewer than 5-50 layers could be used to achieve sufficient optical isolation. Second, filling deep trench isolation structures with multiple materials and layers was well within a POSITAs knowledge at least by the Light Trapping Patent's priority date, as evidenced by the numerous prior art references I have discussed. For example, Suzunaga—published over ten years before the Light Trapping Patents—discloses that its dielectric isolation 5 can consist of alternating layers of silicon and SiO_2. Suzunaga, [0064]. Likewise, Hwang teaches that its sidewall multi-layered reflection layer 220*a*' can contain multiple pairs of its silicon layer 212 and SiO_2 layer 217. Iida, Hirigoyen, Shinohara, and Mori similarly disclose multi-layer and multi-material deep trench isolation reflectors.

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Q245 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination because the resulting trench isolation would be too thick?

A245 Yes. First, Dr. Mansoorian opines that Schubert's DBR would need to be "at a minimum 625nm across" to reflect blue light and "at a minimum 975nm across" to reflect red light, that this "is a huge issue for image sensors that routinely fit millions of pixels into a small space." RX-0911C, ¶274. Second, he opines that the '714 patent "expressly describes the importance of size in image sensor design," and "a trench that is nearly one micron across is simply impractical." RX-0911C, ¶274. I disagree and note neither of these theories were presented in SiOnyx's contentions. RX-0606C.196-198.

Q246 Why do you disagree?

A246 First, using quarter-wavelength thicknesses is only necessary for total reflection, and POSITAs would understand that adequate optical isolation could be achieved using thinner layers. While Dr. Mansoorian asserts that "[t]here is no explanation in Schubert for how to select the appropriate thickness for an image sensor, nor any discussion of how to assess the oblique angle of incidence that would be appropriate for an image sensor," RX-0911C, ¶275, such calculations are well within POSITAs' knowledge. Moreover, the '714 patent contemplates deep trench isolation structures far thicker than the 975nm wide trench that Dr. Mansoorian asserts is "impractical." *E.g.*, '714 patent, 7:52-56.

Q247 Are you aware of Dr. Mansoorian's argument that POSITAs would not know how to implement Schubert's teachings into an image sensor?

A247 Yes. Dr. Mansoorian opines that this combination would not have been obvious, because I did not "consider whether POSITA[s] would use the larger trench necessary for red light for all pixels including the blue pixels, or whether the POSITA would consider that there would need to be a different trench structure for each color of pixel." RX-0911C, ¶276. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.196-198.

First, as explained, even the 975nm trenches Dr. Mansoorian alleges are necessary to reflect light are far narrower than those contemplated by the '714 patent. Second, optimizing trench thicknesses for particular uses—e.g., sacrificing some red-light reflectivity in exchange for more tightly packed pixels or optimizing the thickness for each color—are design choices well within a POSITAs' skills; skills that are necessary to implement the '714 patent which, apart from providing large potential ranges, does not inform how to select trench widths optimized for certain colors.

Q248 Are you aware of Dr. Mansoorian's argument that using a Si/SiO_2 reflector in Haddad188 would require a DH?

A248 Yes. Dr. Mansoorian opines that, "the need for a 'DH' on top of the DBR taught by Schubert will further increase the thickness of the DBR and the trench needed, exacerbating the problems discussed above." RX-0911C, ¶276. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.196-198.

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First, POSITAs would understand that "DH" as used in Schubert refers to a "double heterostructure" which is a semiconductor structure that Schubert provides as an example to convert electrical signals into light. *See* Schubert, Fig. 10.7. POSITAs would understand that such a DH is unnecessary in Haddad188, as Haddad188's pixel converts light into electrical signals, and does not need a structure to convert electrical signals into light.

Second, POSITAs would understand that a Si/SiO_2 reflector would not need to be lattice matched to the pixel like Schubert describes the DBR being lattice matched to the DH. Schubert states that lattice matching is necessary "since a DH is usually grown on top of the DBR." Schubert, 172. POSITAs would understand that Haddad188's pixel is not grown on top of its deep trench isolation, and that lattice matching would be irrelevant in such an instance. Indeed, the references I have relied upon have not considered such lattice matching necessary when using Si/SiO_2 reflectors. *See generally*, Suzunaga; Hwang.

Q249 Are you aware of Dr. Mansoorian's assertion that POSITAs would not make this combination as it allegedly would not provide adequate optical isolation?

A249 Yes. Dr. Mansoorian opines that "a DBR is much less effective than 'an ideal (metallic) reflector," as allegedly Schubert's Figure 10.9 "shows a DBR allows penetration of radiation through several layers of the DBR, while the metallic reflector stops incident radiation." RX-0911C, ¶277. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.196-198.

Q250 Why do you disagree with Dr. Mansoorian's opinion?

A250 First, as Dr. Mansoorian notes, Schubert's Figure 10.9 analyzes an ideal metallic reflector, i.e., a reflector with 100% reflectance. *See* Schubert, 165 ("An ideal metal has a very high conductivity, i.e. $\sigma \rightarrow \infty$ and therefore $\bar{k} \rightarrow \infty$."). However, POSITAs would realize that Haddad188's reflector would not be an ideal metallic reflector, but rather a real reflector, and that "[r]eal metals have high conductivity (but not an infinitely high conductivity) and the reflectivity of any real metal is therefore less than unity." Schubert, 165; *see also* Schubert Table 10.2 (showing less than 100% reflectivity for metal reflectors). Indeed, Dr. Mansoorian has argued against using metal reflectors elsewhere, opining that they have far less than 100% reflectivity. RX-0911C, ¶449. To the contrary, POSITAs would understand that Si/SiO_2 reflectors can be configured to achieve 100% reflectivity. *E.g.*, Suzunaga, [0028] (by "optimizing the thickness of the SiO_2 film 14 and the polysilicon film 15 for the wavelength of the incident light … almost 100% of the incident light passing through the element layer 2 can be reflected by the multi-reflection film 16").

Second, even if a Si/SiO_2 reflector would provide worse optical isolation than a metallic reflector—as Dr. Mansoorian incorrectly, and inconsistently, asserts—POSITAs would still be motivated to make this combination, as a Si/SiO_2 reflector would also reduce dark current, something Dr. Mansoorian repeatedly stresses throughout his report, and that SiOnyx employees and the prior art have verified. JX-0017C (Sickler), 42:1-10; McKee, 93:2-13; *See generally* RX-0911C, Shinohara, Iida, Konno, Mori, Roy. As explained, a thinly insulated metallic reflector is likely to cause dark current, as Mori teaches, thus

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motivating POSITAs to consider non-metallic reflectors, e.g., a Si/SiO_2 reflector as Schubert teaches.

b. Claim 12

Q251 Let's turn to claim 12, which is *[t]he device of claim 1, further comprising a frontside light trapping material at least partially covering the light incident surface*. Does Haddad188 satisfy this claim?

A251 Yes. Haddad188 teaches or suggests a *frontside light trapping material at least partially covering the light incident surface*.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *light trapping material*. Haddad188 teaches or suggests a *frontside light trapping material*, including under either construction.

Q252 How does Haddad188 satisfy this limitation?

A252 Haddad188 includes "a metal or other reflective material layer 166," Haddad188, 25:9-10, having an aperture to allow entry of light into the pixel. *See* Haddad188, 25:9-11 ("aperture 164 formed in a metal or other reflective material layer 166" "lens focuses electromagnetic radiation through the aperture").

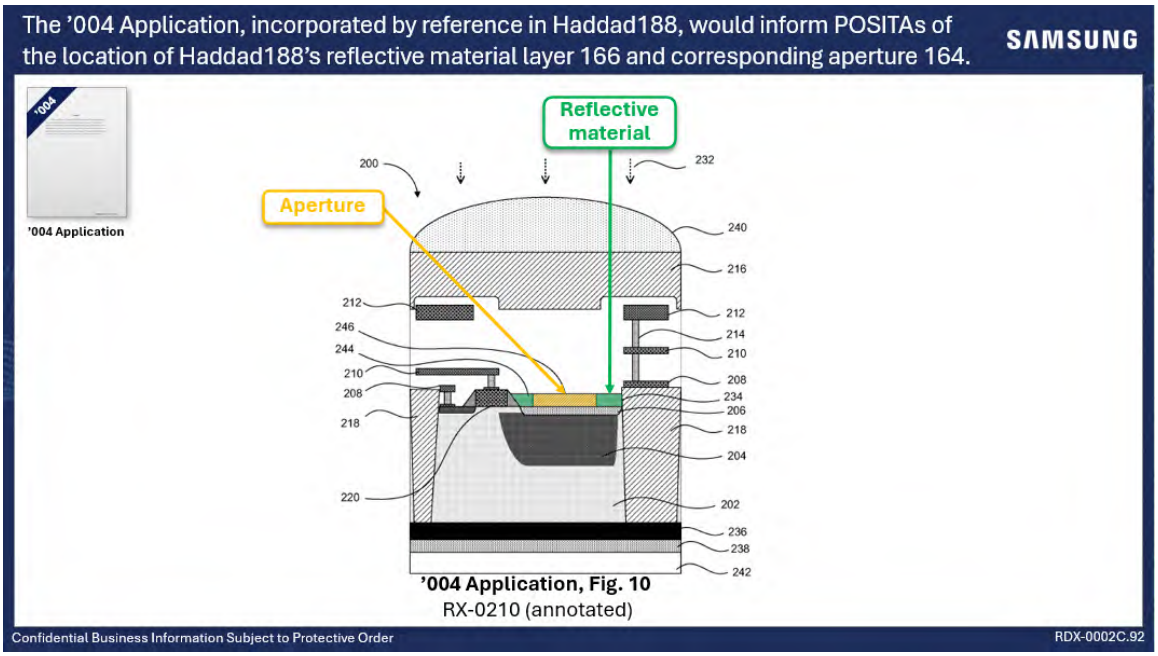
Q253 Does Haddad188 depict reflective material layer 166?

A253 Not in its figures. Although reflective material layer 166 is discussed in the specification's text, Haddad188's figures do not depict it. However, Haddad188 "incorporate[s] herein by reference" "U.S. Provisional Patent Application Serial No. 61/311,004" ("'004 Application), Haddad188, 1:4-8, which depicts the reflective material layer in its figures.

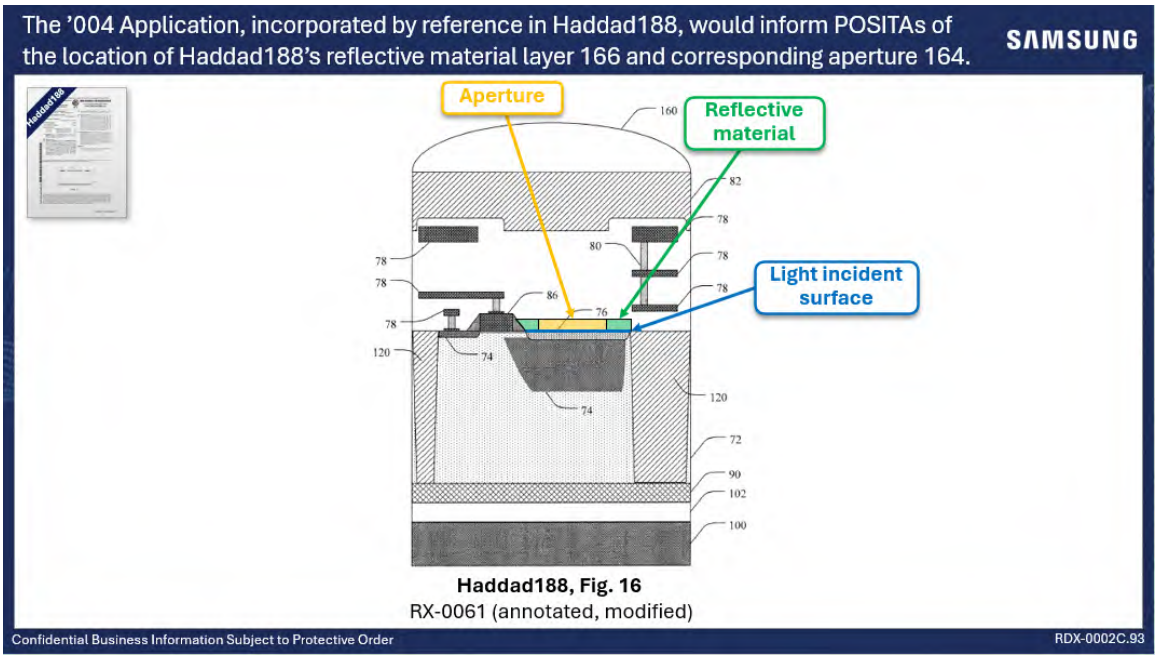
Q254 Please turn to RX-0210 ('004 Application). Do you recognize this document?

A254 Yes. RX-0210 is the '004 Application. As RDX-0002C.92 illustrates, the '004 Application depicts a reflective material 244, with corresponding aperture 246, disposed on semiconductor substrate 202's light incident side above highly doped region 206. '004 Application, 9.

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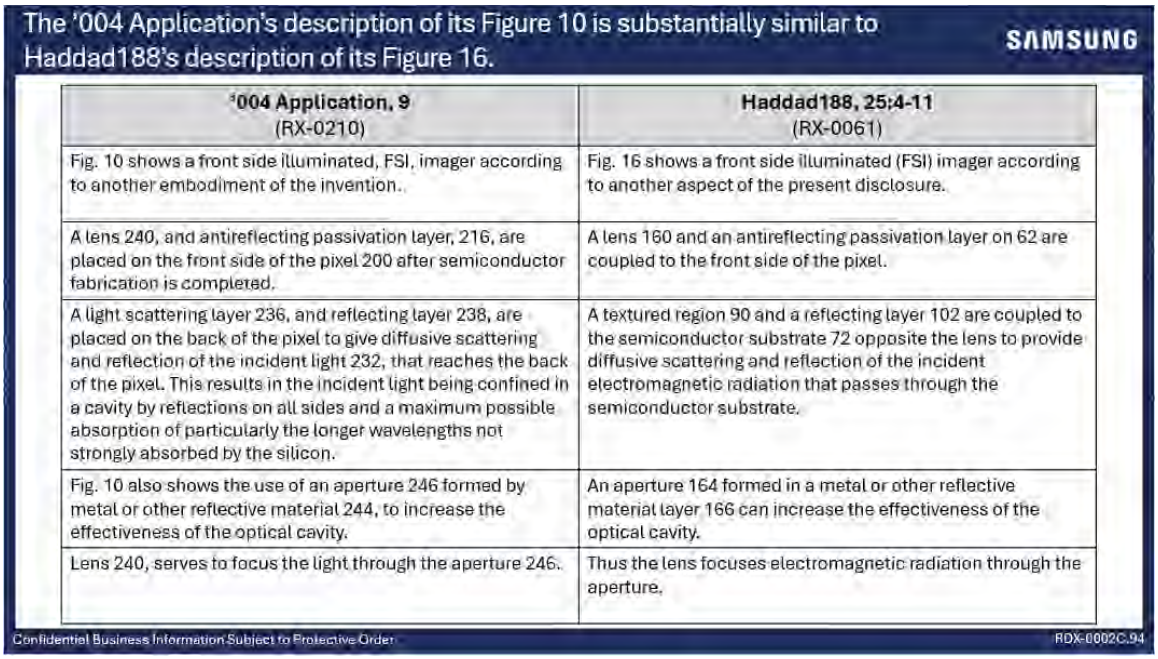
POSITAs would understand that Haddad188's reflective material layer 166, and corresponding aperture 164, would be similarly located in Haddad188's Figure 16, as RDX-0002C.93 illustrates. Placing these layers in a comparable position allows Haddad188's "lens [to] focus[] electromagnetic radiation through the aperture," and into the doped regions, Haddad188, 25:10-11, and would be consistent with Haddad188's specification. This placement would further "increase the effectiveness of the optical cavity," Haddad188, 25:10-11, as reflective material layer 166 would reflect incident light from inside the pixel back into the pixel.



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Q255 Is there any other support for your opinion?

A255 Yes. As RDX-0002C.92-93 illustrate, '004 Application, Figure 10 and Haddad188, Figure. 16 are nearly identical. Moreover, as RDX-0002C.94 illustrates, the '004 Application's description of Figure 10 is substantially similar to Haddad188's description of Figure 16. *Compare* '004 Application, 9 *with* Haddad188, 25:4-11.



Q256 Does reflective material layer 166 satisfy this limitation?

A256 Yes. Reflective material layer 166 constitutes a *light trapping material*. Haddad188 discloses that it "can increase the effectiveness of the optical cavity," Haddad188, 25:10-11, which POSITAs would understand to mean reflecting light from inside the pixel back into the pixel. POSITAs would have understood that it is located on the *light incident surface* based on the '004 Application's disclosures.

Q257 How does reflective material layer 166 constitute a *light trapping material* under the parties' proposed constructions?

A257 Reflective material layer 166 constitutes a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

Q258 Are you aware of Dr. Mansoorian's argument that Haddad188 does not disclose this limitation?

A258 Yes. Dr. Mansoorian opines that Haddad188 allegedly does not disclose this limitation because Haddad188 does not disclose reflective material layer 166's location or its light trapping characteristics. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.1169.

Q259 Why do you disagree with Dr. Mansoorian's opinion that Haddad188 does not disclose reflective material layer 166's location?

A259 Dr. Mansoorian speculates that, since reflective material layer 166 is not drawn in Figure 16, its location "could have changed" "[i]n between the filing of the provisional application and the filing of Haddad188." RX-0911C, ¶283. I disagree. I have been informed that when a document is "incorporated by reference" into a host document, such as a patent, the referenced document becomes effectively part of the host document as if it were explicitly contained therein. Haddad188 incorporates the '004 Application by reference without limitation. Haddad188, 1:4-8. Dr. Mansoorian points to no support in Haddad188, or its application history, suggesting that the '004 Application's teachings are irrelevant to Haddad188, nor why POSITAs could not consider them. As explained, Haddad188 teaches that a reflective material layer 166 is used in its Figure 16 embodiment but does not specify where, such that POSTIAs would be motivated to look to the rest of Haddad188's disclosures—including the '004 Application incorporated by reference—to determine where it should be located.

I further disagree with Dr. Mansoorian's opinion that POSITAs would not place reflective material layer 166 where the '004 Application teaches it should go. Dr. Mansoorian's argument that it should be placed elsewhere due to Haddad188's circuitry is contrary to Haddad188's own teachings. Moreover, while he opines that POSITAs would not consider putting reflective material layer 166 on Haddad188's pixel, he does not opine where else it should be located.

Q260 Why do you disagree with Dr. Mansoorian's opinion that reflective material layer 166 is not light trapping?

A260 Dr. Mansoorian opines that reflective material layer 166 does not constitute a *light trapping material* under either party's proposed construction, because it would not be obvious to configure reflective material layer 166 to reflect light back into the pixel.

However, as explained, Haddad188's disclosure that reflective material layer "can increase the effectiveness of the optical cavity," Haddad188, 25:10-11, teaches, or at least strongly suggests, that it is reflective such that it can reflect light back into the pixel. I disagree with Dr. Mansoorian's opinion that the aperture increases optical cavity effectiveness by focusing incident light. Apertures do not focus incident light, rather, a "lens focuses light electromagnetic radiation through the aperture." Haddad188, 9:11. Moreover, POSITAs reading Haddad188 would understand that its reference to "increas[ing] the effectiveness of the optical cavity" means increasing the effective absorption length by creating internal reflections within the pixel—i.e., trapping light by reflecting it from inside the pixel back into the pixel—rather than reducing crosstalk, as Dr. Mansoorian speculates. *E.g.*, Haddad188, 15:16-18 ("Such internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor substrate. This increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.").

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Finally, even if reflective material layer 166's primary purpose was to "direct light into the pixel" as Dr. Mansoorian opines, RX-0911C, ¶284, it is undisputed that reflective material layer is reflective. As explained, placing it on the *light incident surface* would have been obvious, and it would act as a *light trapping material* because incident light hitting it from below would be reflected back into the pixel.

c. Claim 17

Q261 Let's turn to claim 17, which is *[t]he device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer*. Have you formed an opinion regarding this claim?

A261 Yes. Haddad188 and Schubert render obvious claim 17. Haddad188 teaches or suggests a *backside light trapping material* that *is a metal layer*. Dr. Mansoorian has not disputed this.

As discussed for '714 patent (Ground 6), limitation 1[b], Haddad188's FSI imager includes a *backside light trapping material* (reflecting layer 102). Haddad188 explains that reflecting layer 102 "can be any reflective material that can be incorporated into such a device," "includ[ing] … silver, aluminum, and the like," Haddad188, 23:15-26, i.e., a *metal layer*.

d. Claim 18

Q262 Let's turn to claim 18, which is *[t]he device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface*. Have you formed an opinion regarding this claim?

A262 As explained regarding the Terms Remaining in Dispute, I understand that Samsung proposed the term *sloped surface at the pixel device interface* is indefinite, and that SiOnyx proposed it has its plain and ordinary meaning, and to the extent a construction is required, it means sloped trench wall or sloped backside surface.

It is unclear what is meant by *a sloped surface at the pixel device interface*, in particular, what is meant by a *pixel device interface*. There is no discussion in the specification of a *pixel device interface*, and the term lacks antecedent basis, such that the specification fails to inform POSITAs, with reasonable certainty, of the claim's scope.

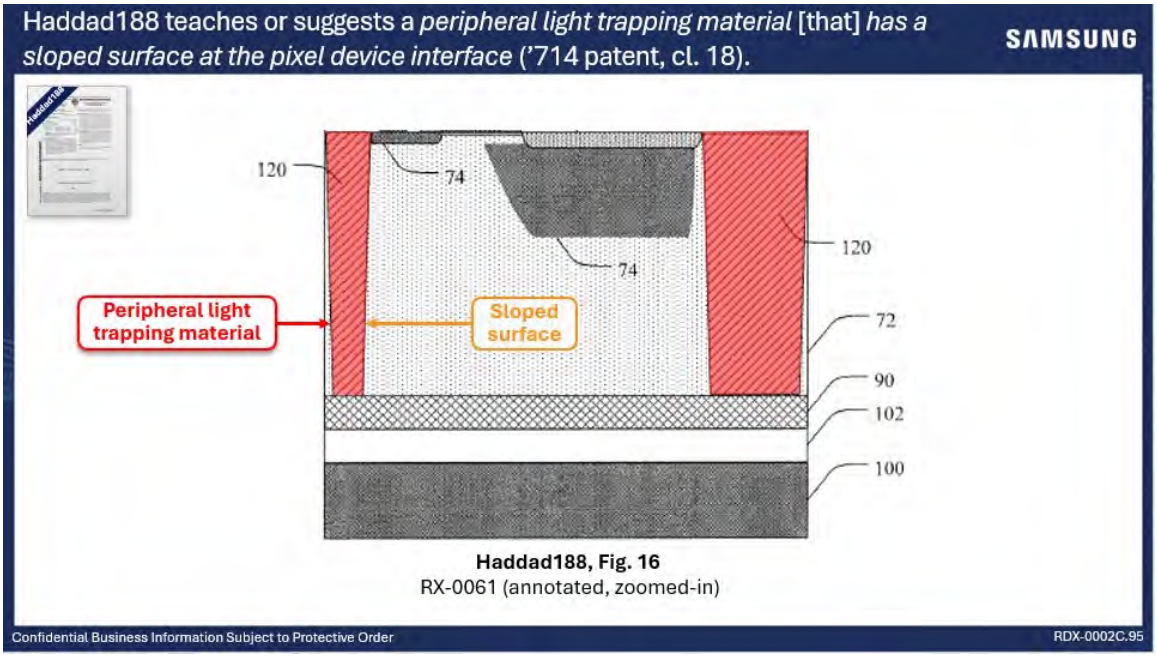
To the extent the limitation is not indefinite, Haddad188 includes booth a *backside light trapping material* and a *peripheral light trapping material* that *has a sloped surface at the pixel device interface*. Dr. Mansoorian has not disputed that Haddad188 includes a *backside light trapping material* that *has a sloped surface at the pixel device interface*.

Q263 How does Haddad188's *peripheral light trapping material* satisfy this claim?

A263 As explained for limitations 1[c] and 1[e], Haddad188 includes a *peripheral light trapping material* (trench isolation 102 which, as modified by Schubert, is formed out of alternating layers of SiO_2 and Si). As RDX-0002C.95 illustrates, trench isolation 102 *has a sloped*

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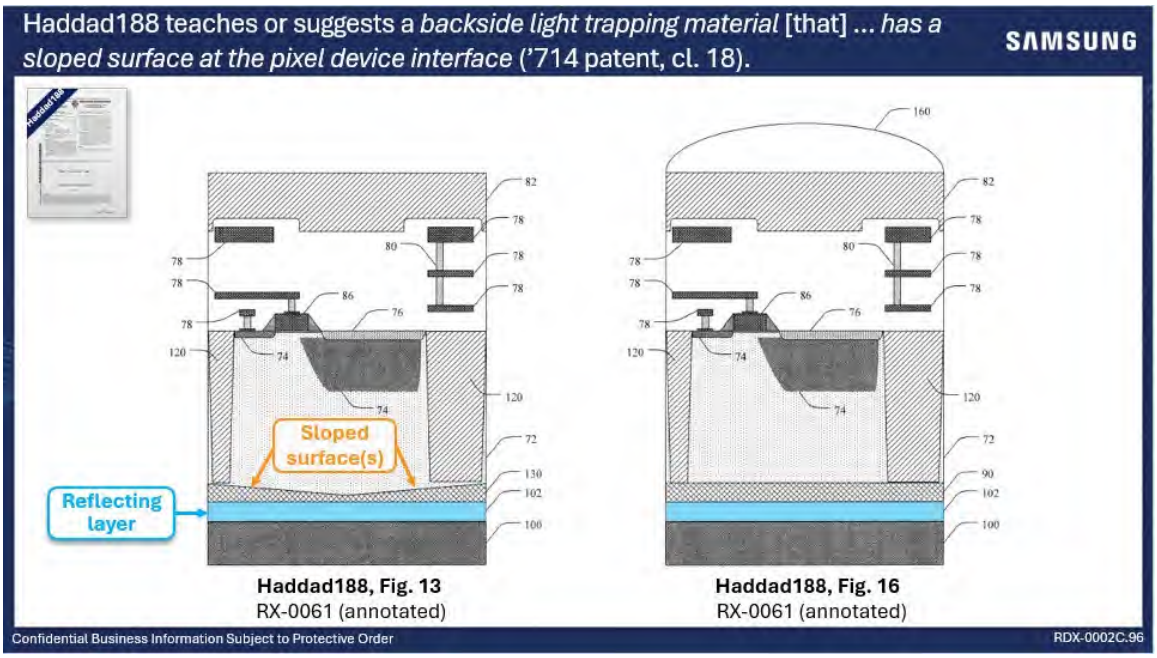
surface, as it has a taper such that the top is wider than the bottom, the same structure Dr. Foty accuses of infringement. RX-0905C, ¶¶488-493.



POSITAs would understand that the sloped surface could be maintained even when using the Si/SiO_2 layers taught by Schubert. For example, as I will later explain, and as RDX-0002C.95 illustrates, Suzunaga discloses a "dielectric isolation region 5 … formed by embedding polysilicon 6 in a V-groove with a SiO_2 film 7 or the like interposed therebetween." Suzunaga, [0008].

Q264 How does Haddad188's *backside light trapping material* satisfy this claim?

A264 As RDX-0002C.96 illustrates, Haddad188 teaches, for Figure 13, that "textured region 130 can have a nonparallel [(*sloped*)] surface with respect to the semiconductor substrate 72," which "can effectively focus electromagnetic radiation into the semiconductor substrate from multiple sides." Haddad188, 24:1-15. As RDX-0002C.96 illustrates, Figures 13 and 16 are substantially similar, such that POSITAs would understand Haddad188's Figure 13 teachings are applicable to Figure 16.



As explained for limitation 1[b], reflective layer 102 constitutes a *backside light trapping material*. However, a *backside light trapping material* could also comprise reflective layer 102 and textured region 130, such that it has *a sloped surface*, as RDX-0002C.96 illustrates. Moreover, POSITAs would understand a nonparallel (*sloped*) surface could be implemented in reflective layer 102, which would further Haddad188's goal of "effectively focus[ing] electromagnetic radiation into the semiconductor substrate from multiple sides." Haddad188, 24:1-15.

D. Suzunaga-based Grounds

Q265 Let's turn to your Suzunaga-based opinions. Can you please summarize your anticipation and obviousness opinions about the '714 patent based on Suzunaga?

A265 My Suzunaga-based opinions are based on a single ground, Ground 7, which is that Suzunaga anticipates, or at least renders obvious, claims 1, 12-13, and 18.

1. Ground 7: Suzunaga Anticipates, or at Least Renders Obvious, Claims 1, 12-13 and 18

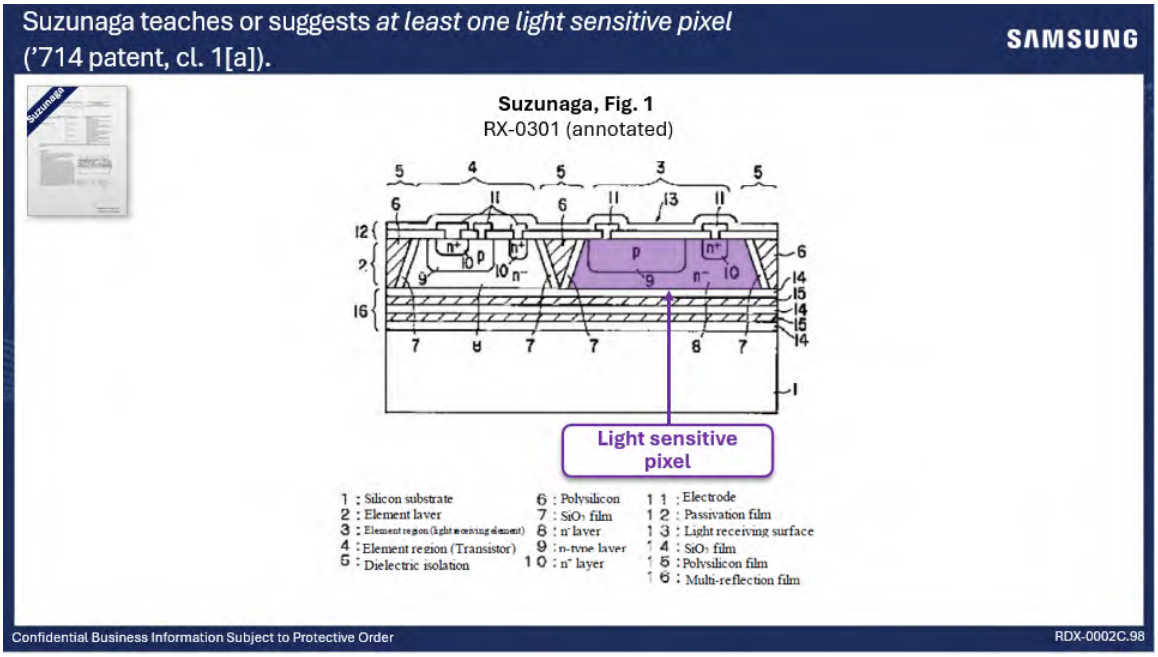
a. Claim 1

1. Limitation 1[a]

Q266 Let's start with claim 1. Claim 1's first limitation, 1[a], is relatively long, so let's take it in parts. The first element is *at least one light sensitive pixel*. Does Suzunaga satisfy this element?

A266 Yes. I understand that the ALJ construed *light sensitive pixel* to have its plain and ordinary meaning. Order No. 36 at 27. Suzunaga includes a *light sensitive pixel* under its plain and

ordinary meaning, which I consider to be portions of a device that convert light into electrical signals. As RDX-0002C.98 illustrates, Suzunaga discloses "[s]emiconductor light receiving elements that are mutually dielectrically isolated," Suzunaga, Abstract, that are "formed by using n^- layer 8 of the element layer 2, a p-type layer 9, and an n^+ layer 10 for making an n-side contact," Suzunaga, [0009]. Suzunaga explains that this "$p\text{-}n^-\text{-}n^+$ structure including elements 9, 8 and 10 constitutes a pin type light receiving element," where the "n^+ layer 10 is used as an emitter diffusion layer, a collector contact layer and a p-type layer 9 are used as a base region, and an n-type layer 8 is used as a collector region in the element region 4 forming the transistor." Suzunaga, [0009].



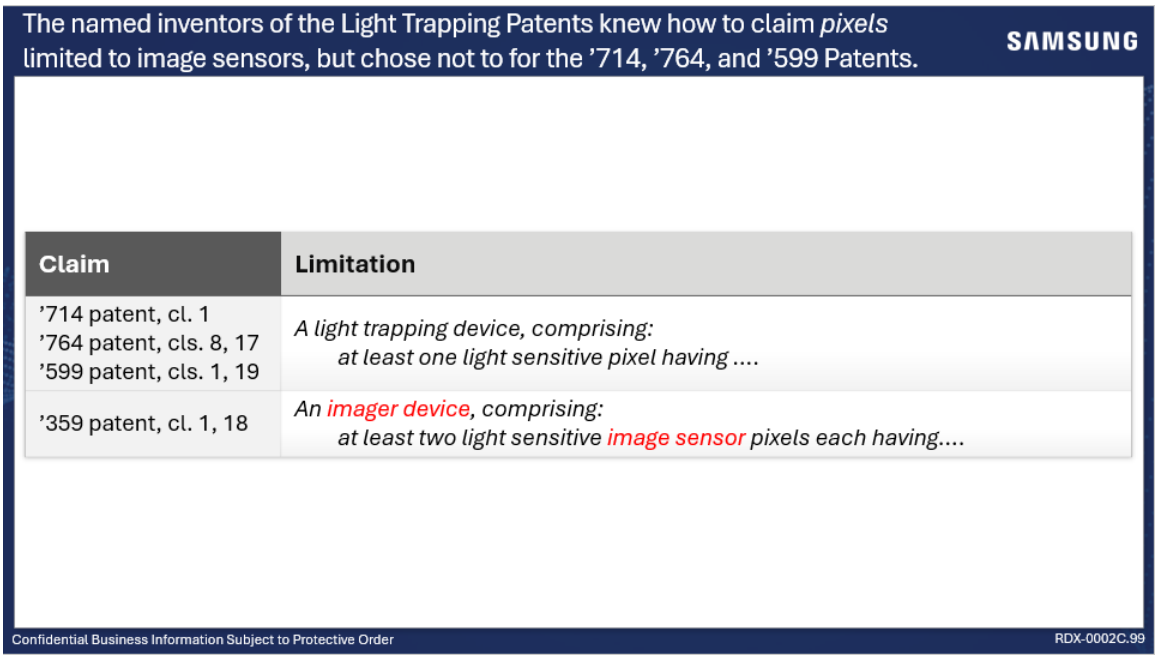
Q267 Are you aware of Dr. Mansoorian's argument that Suzunaga does not disclose *at least one light sensitive pixel*?

A267 Yes. I understand that, while Dr. Mansoorian admits Suzunaga "is used to capture light," he opines that it does not disclose *at least one light sensitive pixel* because "Suzunaga is not referring to a structure used in imaging devices." RX-0911C, ¶294; *see also* RX-0911C, ¶¶293-308. I disagree. First, the '714, '764, and '599 patents, for which I use Suzunaga as a reference, are not limited to image sensors. Second, even if they were limited, Suzunaga's light receiving element constitutes a light sensitive pixel that can be used in an image sensor.

Q268 Why are the '714, '764, and '599 patents not limited to image sensors?

A268 First, the Light Trapping Patents are directed to light trapping devices and contemplate uses beyond just image sensors. *See* '714 patent, 1:42-46, 6:23-25 ("present disclosure is applicable to other optoelectronic devices such as solar cells, and that all such should be included in the present scope"). Second, as RDX-0002C.99 illustrates, the '714, '764, and '599 patents, unlike the '359 patent, only claim *light trapping devices comprising at least*

one light sensitive pixel, as opposed to *[a]n imager device comprising: at least two adjacent light sensitive image sensor pixels*. *Compare* '714 patent, cl. 1, '764 patent, cls. 8, 17, 21, '599 patent, cls. 1, 19 *with* '359 patent, cls. 1, 18.



In my opinion, that the patentee knew how to claim *light sensitive pixels* that were limited to image sensors, as evidence by the related '359 patent, further shows that the applicants did not intend for the '714, '764, and '599 patents' *light sensitive pixels* to be limited to image sensors.

Q269 Why does Suzunaga's pixel constitute a light sensitive pixel capable of being used in an image sensor?

A269 Dr. Mansoorian opines at length, with limited cited support, that Suzunaga's PIN diode is not a *light sensitive pixel* used in an image sensor because image sensor pixels allegedly are normally pinned diodes, and that there is a substantial difference between PIN diodes and pinned diodes. I disagree. Despite his lengthy argument, Dr. Mansoorian does not actually assert that PIN diodes cannot be used in image sensors, and POSITAs would understand that image sensors can comprise a number of different dopant structures, including PIN diodes.

Indeed, POSITAs would understand that PIN diodes are capable of capturing images and being used in image sensors. Indeed, POSITAs would understand that CMOS active pixel image sensors (APS) were developed before pinned photodiodes and that it was not until several years after the introduction of APS devices that pinned photodiodes achieved widespread adoption. Accordingly, POSITAs would understand that image sensors are not limited to pinned photodiodes, and they could be formed using PIN diodes. Indeed, the specification envisions the use of PIN diodes. *E.g.*, 17:9-28.

Q270 Are you aware of Dr. Mansoorian's argument that Suzunaga does not disclose an image sensor because Suzunaga allegedly is not concerned with electrical or optical crosstalk?

A270 Yes. Dr. Mansoorian argues that Suzunaga "is not concerned with either electrical or optical crosstalk" and "is not separating one light receiving element from another" as alleged support for his opinion Suzunaga does not disclose an image sensor. RX-0911C. ¶305. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.96-97.

Q271 Why do you disagree?

A271 While Figure 1 only depicts one light receiving element 3 (*pixel*) separated from a transistor 4, POSITAs would understand that Suzunaga is still concerned with both electrical and optical crosstalk.

First, Suzunaga is not limited to what is depicted in Figure 1, but rather describes an array of light receiving elements, as Dr. Mansoorian admits. RX-0911C, ¶315 ("Suzunaga … teaches an array of PIN photodiodes"). POSITAs would understand that in such arrays Suzunaga's light receiving element would be adjacent to other light receiving elements, such that electrical and optical crosstalk are important. Indeed, as I will explain, Suzunaga discloses a "dielectric isolation method where a dielectric film is embedded in a trench or V-groove, in order to electrically isolate element regions into islands," Suzunaga, [0008], and that the "dielectric isolation region 5 [can be] a multi-reflection film," such that it "can be used as part of the reflection surface when scattered light is incident from the incident surface 13." Suzunaga, [0064]. That is, Suzunaga discloses using dielectric isolation 5 to electrically and optically isolate its light receiving element, i.e., prevent electrical and optical crosstalk.

Second, even if Suzunaga's array did not result in light receiving elements 5 being adjacent to one another, POSITAs would nonetheless understand that electrical and optical crosstalk is still important to isolate the light receiving elements 5 from the transistor 4. Indeed, as Figure 1 illustrates, Suzunaga discloses a dielectric isolation region 5 being formed between the two.

Q272 Are you aware of Dr. Mansoorian's argument that Suzunaga is too large to be an image sensor?

A272 Yes. Dr. Mansoorian opines that Suzunaga's light receiving element must be "at least 20μm deep," and that "[a]s shown in Figure 6, the element region 3 and element region 4 are longer than they are deep, meaning they would be at least 20μm across as well," and that "[t]his is too large for an image sensor," RX-0911C, ¶306 (quoting Suzunaga, [0012]). I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.96-97.

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Q273 Why do you disagree?

A273 First, Suzunaga explains that part of its invention—i.e., using multi-reflection film 16 to reflect light back into the pixel—overcomes shortcomings in the prior art and allows for thinner light receiving elements. Suzunaga, [0017] ("object of the present invention is to provide a light receiving element that exhibits sufficiently high light emitting efficiency in the infrared region, even when the thickness of the element layer is in a range of 10μm to 20μm.").

Second, Dr. Mansoorian's assertion that Suzunaga's "element region 3 and element region 4 are longer than they are deep," RX-0911C, ¶306 is speculation; nothing in Suzunaga indicates that it is drawn to scale and Suzunaga does not provide dimensions as to the device's length.

Third, Dr. Mansoorian's assertion that Suzunaga is "simply too large for an image sensor," RX-0911C, ¶306, is unsupported speculation. Moreover, the Light Trapping Patents do not claim *pixels* of certain sizes, and the specification actually contemplates pixels and features far larger than the dimensions Dr. Mansoorian attributes to Suzunaga. *E.g.*,

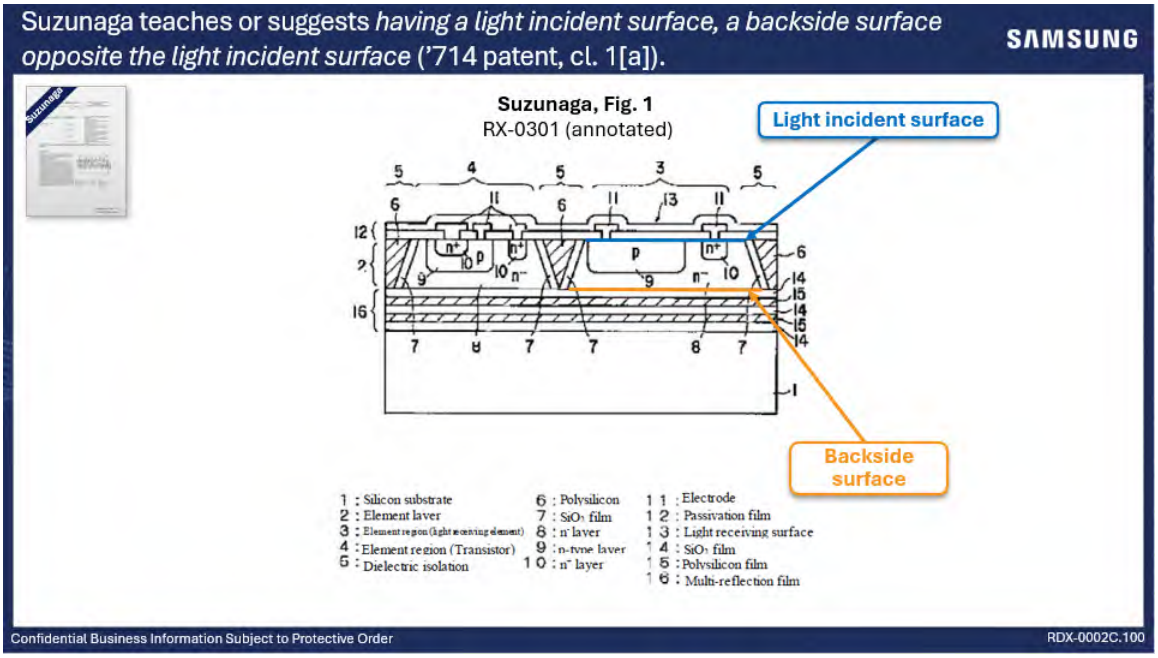
> The depth of the trench isolation feature can be in the range of from about 100 nm to about 50 μm depending on the design of the device. The width can be in the range of from about 100 nm to about 10 μm.
>
> ….
>
> In one aspect, for example, the textured region has a thickness of from about 500 nm to about 100 μm.
>
> ….
>
> Such a textured film layer can have an average thickness of from about 1 nm to 20 μm.
>
> ….
>
> In one aspect, for example, a semiconductor layer has a thickness of from about 500 nm to about 50 μm. In another aspect, the semiconductor material has a thickness of less than or equal to about 500 μm…. In a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 750 μm. In yet a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 100 μm.

'714 patent, 7:52-56, 13:54-63, 14:20-24, 16:45-54.

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Q274 Limitation 1[a]'s second element is *having a light incident surface, a backside surface opposite the light incident surface*. Does Suzunaga satisfy this element?

A274 Yes. As RDX-0002C.100 illustrates, each pixel in Suzunaga has a *light incident surface* and a *backside surface opposite the light incident surface*.



Suzunaga teaches that multi-reflection film 16 is coupled to the pixel's bottom surface. *See Suzunaga*, [0018] ("multi-reflection film in which a film having a first refractive index and a film having a second refractive index are alternately stacked at an interface with the semiconductor substrate."). As RDX-0002C.100 illustrates, Suzunaga's pixel's top surface is a *light incident surface*, and the bottom surface of semiconductor substrate 72 is a *backside surface opposite the light incident surface*.

Q275 Does Suzunaga's labeling of a "[l]ight receiving surface" 13 on top of its passivation film 12 affect your opinion as to what the *light incident surface* is?

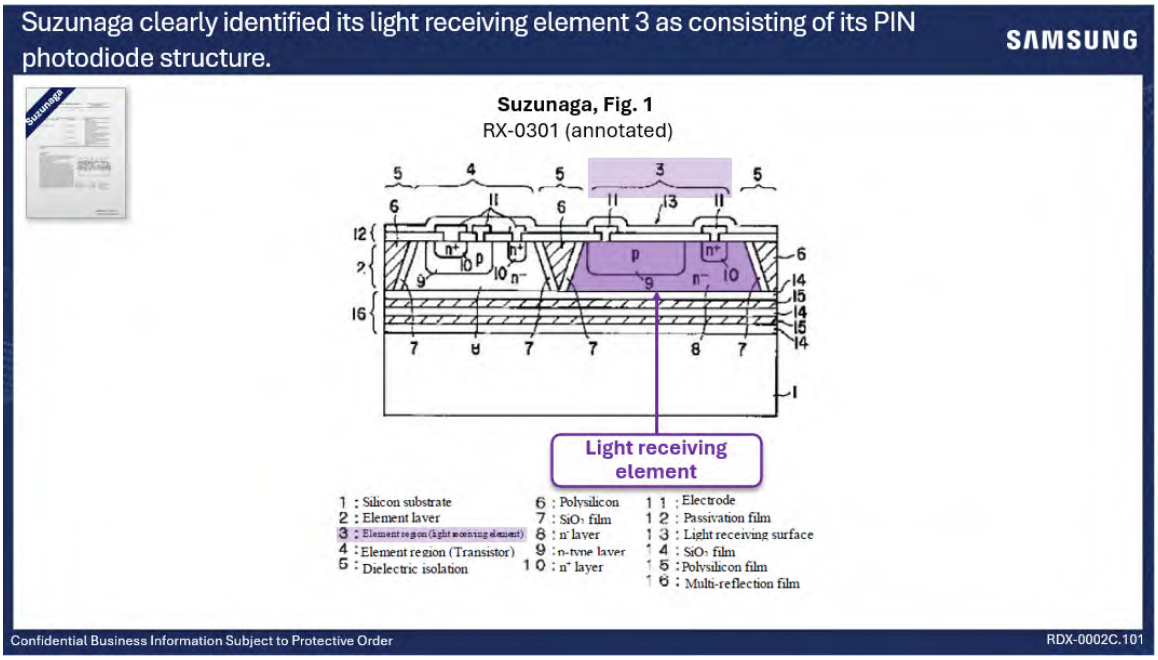
A275 No. While Suzunaga labels a "[l]ight receiving surface 13" of its light receiving element, POSITAs would understand that the *light incident surface* as claimed in the Light Trapping Patents is the light incident surface *of the pixel* (here, the topside). POSITAs would not consider the light receiving surface 13 to be the light incident surface *of the pixel*. In particular, the light receiving surface 13 is formed outside of the *pixel*, above the electrodes 11 and passivation film 12. POSITAs would not consider the electrodes or passivation film to be part of the pixel, there is no reference to such structures being part of the *pixel* in the Light Trapping Patents, and neither structure assists in converting light into an electrical signal.

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Q276 Are you aware of Dr. Mansoorian's argument that Suzunaga's light receiving element is broader than just the PIN photodiode structure?

A276 Yes. Dr. Mansoorian opines that identification of Suzunaga's *pixel* "improperly restricts the light receiving element, as identified by structure 3 in Fig. 1," and that "[t]he light receiving element is clearly broader than just the PIN photodiode structure." RX-0911C, ¶310. I disagree.

As RDX-0002C.101 illustrates, what I have identified as Suzunaga's *pixel* is Suzunaga's light receiving element 3. Dr. Mansoorian appears to suggest that Suzunaga's light receiving element should encompass everything below the highlighted bracket 3—i.e., the portions of Suzunaga's silicon substrate 1, multi-layer reflection film 16, doped layers 8-10, electrode 11 and passivation film 12 underneath the bracket. POSITAs would understand, however, that Suzunaga's light receiving does not encompass silicon substrate 1, multi-reflection film 16, electrode 11 or passivation film 12. For example, Suzunaga explains there is a "dielectric isolation region 5 between the element regions 3 and 4." Suzunaga, [0008]. The passivation film 12 goes across the entire portion of Suzunaga's structure, such that dielectric isolation region 5 could not separate light receiving element 3 from element region 4 if passivation film 12 was part of the light receiving element 3.

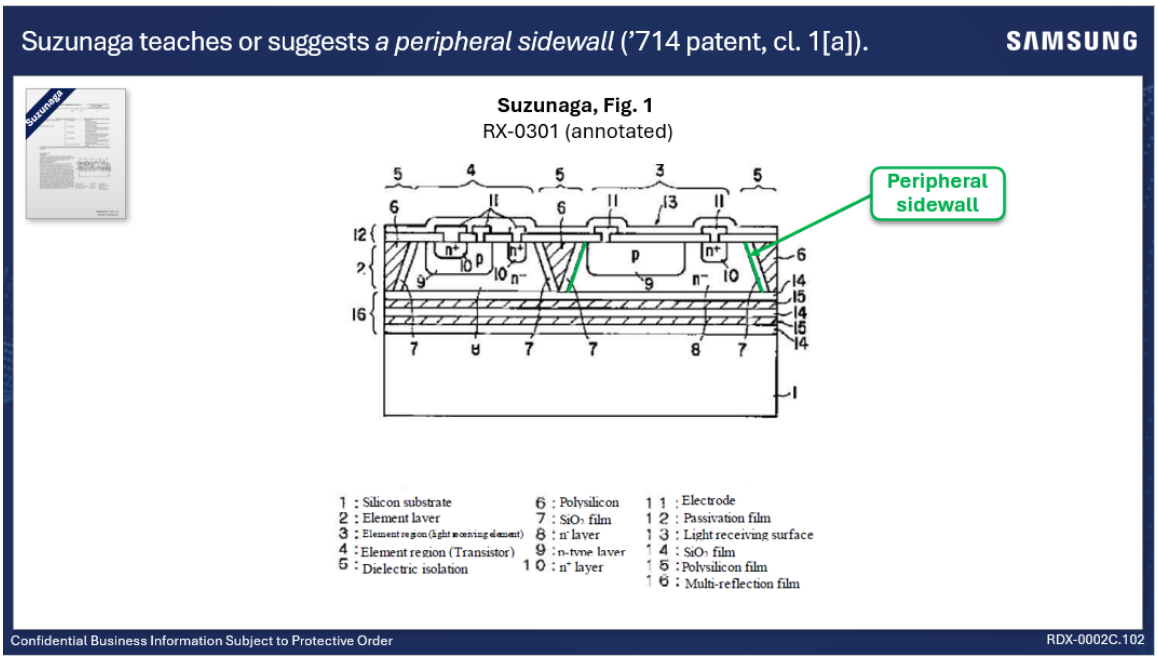


Q277 Limitation 1[a]'s third part is *a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery*. Have you formed an opinion regarding this element?

A277 Yes. In view of Dr. Foty's interpretation and application of this term wherein it is allegedly satisfied because the *peripheral sidewall* defines the pixel's bounds, and to the extent it is not indefinite (as I will explain), Suzunaga teaches or suggests this limitation.

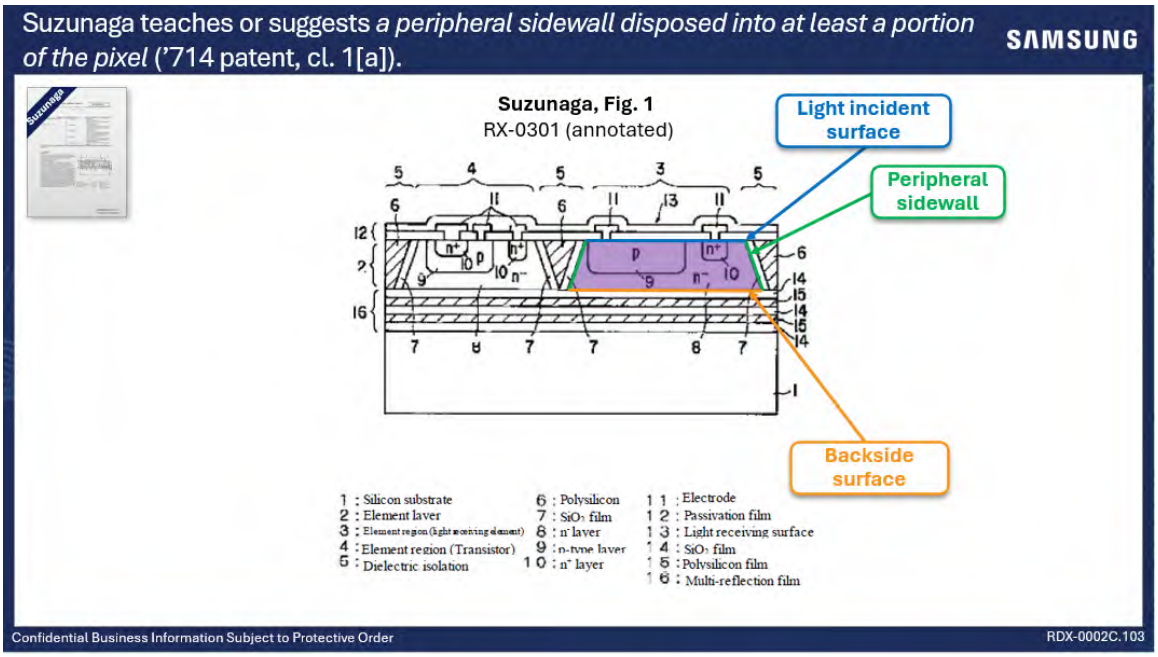
Q278 Does Suzunaga include a *peripheral sidewall*?

A278 Yes. I understand that the ALJ construed *sidewall* to mean trench wall. Order No. 36 at 20. Suzunaga discloses that a "dielectric region 5 between the element regions 3 and 4 is formed by embedding polysilicon in a V-groove with a SiO_2 film 7 or the like interposed therebetween as a dielectric body." Suzunaga, [0008]. As RDX-0002C.102 illustrates, each pixel (light receiving element) includes a *peripheral sidewall* (trench wall) where the pixel contacts the dielectric region 5. *See also* Suzunaga, [0008] ("dielectric isolation does not necessarily have to use a V-groove, but a method of forming a trench or the like and filling the trench with a dielectric material such as SiO_2 may also be used").



Q279 Is Suzunaga's *peripheral sidewall disposed into at least a portion of the pixel*?

A279 In view of Dr. Foty's interpretation and application of this term and to the extent it is not indefinite, yes. Suzunaga explains that "dielectric isolation region between the element regions 3 and 4 is formed by embedding polysilicon 6 in a V-groove with a SiO_2 film 7." Suzunaga, [0008]. As RDX-0002C.103 illustrates, Suzunaga's *peripheral sidewall* runs from the pixel's *light incident surface* to its *backside surface*—just like the '714 patent's peripheral sidewall 424.



Q280 Does Suzunaga's *peripheral sidewall extend[] at least substantially around the pixel periphery*?

A280 In view of Dr. Foty's interpretation and application of this term and to the extent it is not indefinite, yes. I understand that the ALJ explained that "each instance of 'substantially' will need to have an individual construction tailored to the specific use," Order No. 36 at 34. Suzunaga's peripheral sidewall *extend[s] at least substantially around the pixel periphery*.

Q281 Does Suzunaga include a plan view of its device?

A281 No. Like the Light Trapping Patents, Suzunaga does not include a plan view showing the extent to which dielectric isolation 5 surrounds the pixel; however, Suzunaga explains that "a dielectric isolation method, in which an element region on a silicon substrate is surrounded by an insulating film such as SiO_2, must be used in order to isolate elements in an optical integrated circuit." Suzunaga, [0004]. POSITAs would understand that to "surround" the element region, the *peripheral sidewall* must *extend[] at least substantially around* it.

Q282 To the extent Suzunaga does not disclose a peripheral sidewall *extending at least substantially around the pixel periphery*, would modifying it such that it does be obvious?

A282 Yes. To the extent Suzunaga does not explicitly disclose the peripheral sidewall *extending at least substantially around the pixel periphery*, modifying Suzunaga such that it does would have been obvious. Such modification is consistent with dielectric isolation 5's role, i.e., separating the element regions and reflecting light back into the pixel. *See* Suzunaga, [0019] ("element layer includes a plurality of element regions mutually separated by a dielectric film"), [0064] ("SiO_2 film 7 in the element isolation region 5 [can be] also a

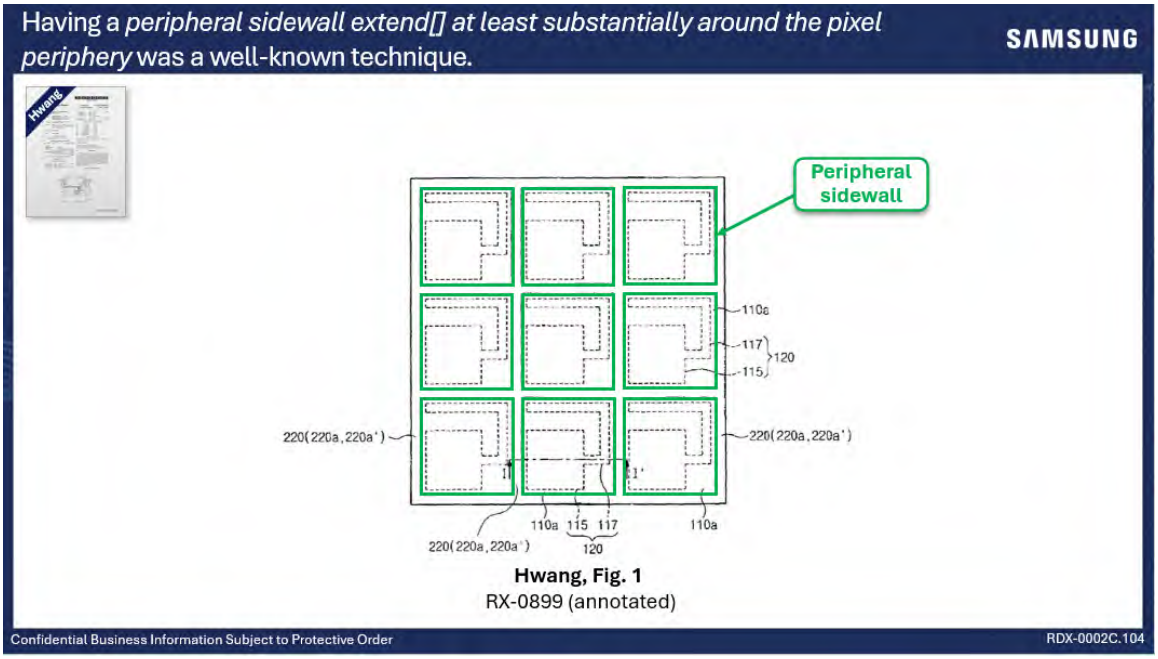
multi-reflection film," such that it "can be used as part of the reflection surface when scattered light is incident from the incident surface 13"). POSITAs would understand that the more dielectric isolation 5 extends around the periphery, the more that light and current will be prevented from moving between pixels, and the less of a chance crosstalk will occur:

> Generally, p-n junction isolation … is often used as an isolation method for integrated circuits. However, in the case of an optical integrated circuit, if light is incident on the p-n junction for isolating elements, the reverse-biased p-n junction exhibits photoconductivity, and therefore cannot fulfill the role of isolating elements. Therefore, a dielectric isolation method, in which an element region on a silicon substrate is surrounded by an insulating film such as SiO_2, must be used in order to isolate elements in an optical integrated circuit.

Suzunaga, [0004].

Q283 Are there any other reasons why you think Suzunaga teaches or suggests a *peripheral sidewall extending at least substantially around the pixel periphery*?

A283 Yes. Having peripheral sidewalls extend completely—which encompasses *at least substantially—around the pixel periphery* was a well-known technique used in similar devices. For example, as previously discussed, Hwang discloses an image sensor with a *peripheral sidewall extending* completely (i.e., *at least substantially*) *around the pixel periphery*, as RDX-0002C.104 illustrates. *See also* Hwang, 6:15-17 ("sidewall multi-layered reflection layer 220 encloses the side walls of the pixel semiconductor patterns 110*a*").



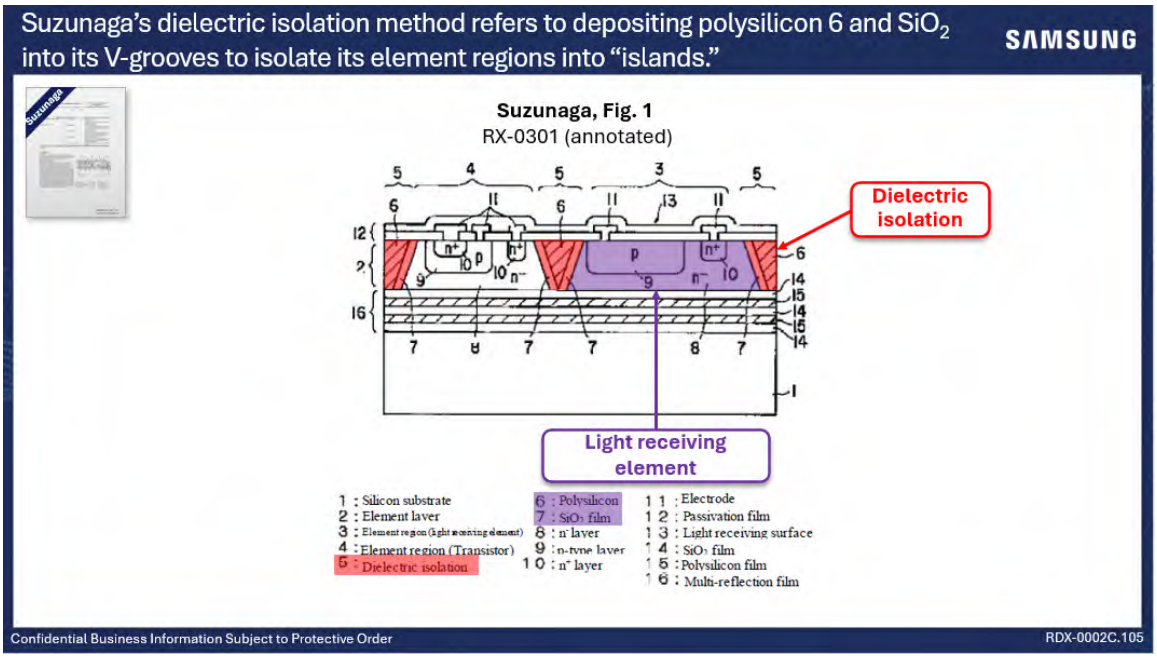
Likewise, as previously discussed, Yamada similarly discloses that each of its embodiments are "configured such that the entire side surfaces of the PIN photodiode 7 is covered by the third reflective films 11." Yamada, [0056]. Consistent with Suzunaga's teachings, Yamada discloses that "the PIN photodiode 7 is surrounded by … third reflective film 11, so when light is incident on the PIN photodiode 7, that light is reflected by … third reflective films 11 so as to be confined within PIN photodiode 7." Yamada, [0036]. *See also* Roy, Fig. 3; RX-0896 (Roy283), 5:53-54 ("each photosite is completely surrounded by trenches").

Q284 Are you aware of Dr. Mansoorian's argument that Suzunaga does not disclose a *peripheral sidewall … extending at least substantially around the pixel periphery*?

A284 Yes. While Dr. Mansoorian acknowledges that Suzunaga teaches "a dielectric isolation method, in which an element region on a silicon substrate is surrounded by an insulating film such as SiO_2," he nonetheless opines that "Suzunaga does not disclose the use of a sidewall, trench, or V-groove to surround the pixel, but instead an insulating film." RX-0911C, ¶314. Dr. Mansoorian then opines that "[t]he use of a trench or V-groove for isolation purposes is discussed throughout the specification, yet the patentee chose to describe 'dielectric isolation method' surrounded only by an insulating film, such as SiO_2." RX-0911C, ¶314. I disagree and note neither theory was presented in SiOnyx's contentions. RX-0606C.96-97.

Suzunaga's disclosure is clear that its dielectric isolation method—including polysilicon 6 and SiO_2 film 7—is what is deposited in the "trench" or "V-groove." For example, Suzunaga teaches that "a dielectric isolation method, in which an element region … is surrounded by an insulating film" means that the Suzunaga's trench surrounds the pixel (light receiving element), as RDX-0002C.105 illustrates. *See* Suzunaga, [0005] ("dielectric isolation method where a dielectric film is embedded in a trench or V-groove, in order to electrically isolate element regions into islands"), [0008] ("dielectric isolation region 5 … is formed by embedding polysilicon 6 in a V-groove with a SiO_2 film 7"); [0016] ("element regions are mutually separated by a dielectric isolation method in which a dielectric body is embedded in a V-groove or trench"); [0019] ("element layer includes a plurality of element regions mutually separated by a dielectric film"); [0042] ("conventional dielectric isolation process using a V-groove or trench or the like can be used"); [0071] ("element regions in which these elements are formed must be mutually isolated using a dielectric isolation method in which a dielectric body is embedded in a V-groove, trench, or the like").

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Q285 Are you aware of Dr. Mansoorian's argument that having a trench extend substantially around Suzunaga's periphery would not have been obvious?

A285 Yes. Dr. Mansoorian opines that "using the trench or V-groove … to extend at least substantially around the pixel periphery" in Suzunaga would not have been obvious because "Suzunaga is not an image sensor, nor can it be because it teaches an array of PIN photodiodes," and that "the V-groove structure already occupies a large portion of the element region." RX-0911C, ¶315. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.96-97.

First, as explained, Suzunaga explicitly discloses that its dielectric isolation region 5 extends *at least substantially around the pixel periphery*, such that no modification is needed. Assuming that were not the case, however, I still disagree with Dr. Mansoorian's opinion. First, as Dr. Mansoorian notes, Suzunaga "teaches an array of PIN photodiodes," such that POSITAs would understand Suzunaga's dielectric isolation region 5 should extend around the periphery (i.e., on all four sides) to isolate the pixels. Indeed, as explained, Suzunaga teaches such a structure. *E.g.*, Suzunaga, [0005] ("dielectric isolation method where a dielectric film is embedded in a trench or V-groove, in order to electrically isolate element regions into islands"). Second, Suzunaga does not specify it is drawn to scale, nor does it provide dimensions of its dielectric isolation region 5, such that I disagree with Dr. Mansoorian's speculation that "the V-groove structure already occupies a large portion of the element region." RX-0911C, ¶315.

2. Limitation 1[b]

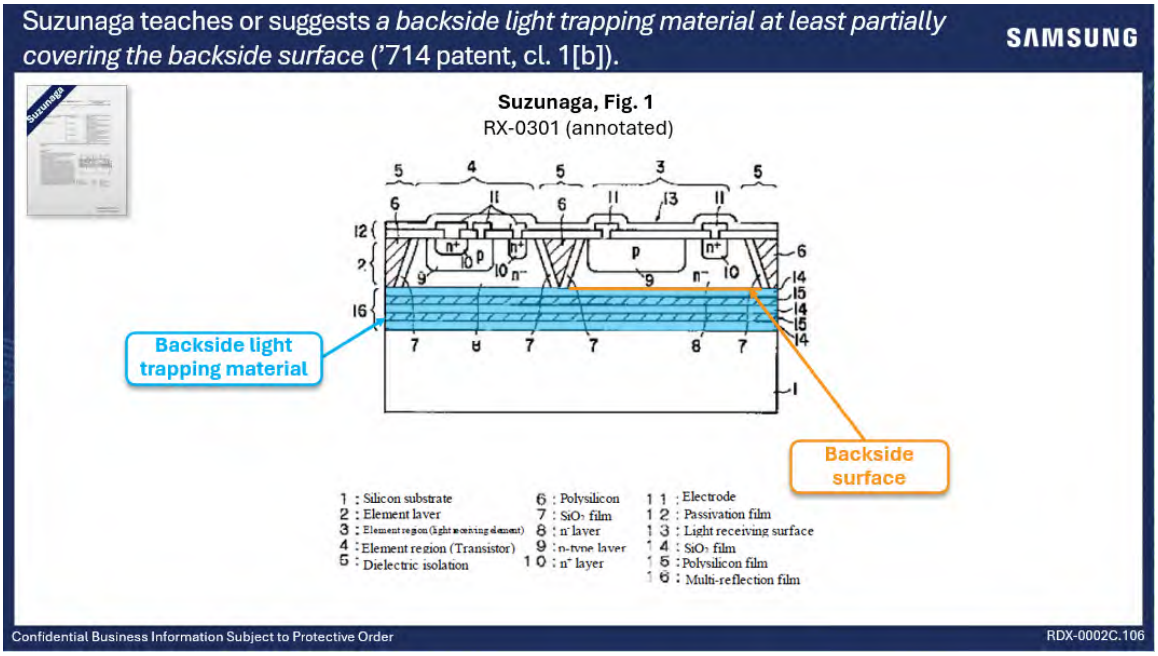
Q286 Limitation 1[b] is *a backside light trapping material at least partially covering the backside surface*. Does Suzunaga satisfy this limitation?

A286 Yes. Suzunaga teaches or suggests *a backside light trapping material at least partially covering the backside surface*.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *light trapping material*. Suzunaga includes a *backside light trapping material*, including under either construction.

Q287 How does Suzunaga satisfy this limitation?

A287 As RDX-0002C.106 illustrates, Suzunaga's "multi-reflection film 16 [is] between the element layer 2 forming the light receiving element and the silicon substrate 1." Suzunaga, [0028]. Accordingly, it *at least partially covers the backside surface*.



Multi-reflection film 16 constitutes a *light trapping material*. Suzunaga teaches that "multi-reflection film … reflects the transmitted light transmitted through the semiconductor light receiving element formed on the element layer, and impinges the reflected light again on the semiconductor light receiving element," Suzunaga, [0019], and that "almost 100% of the incident light passing through the element layer 2 can be reflected by the multi-reflection film 16," back into Suzunaga's pixel. Suzunaga, [0028].

Q288 How does multi-reflection film 16 constitute a *light trapping material* under the parties' proposed constructions?

A288 Multi-reflection film 16 constitutes a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

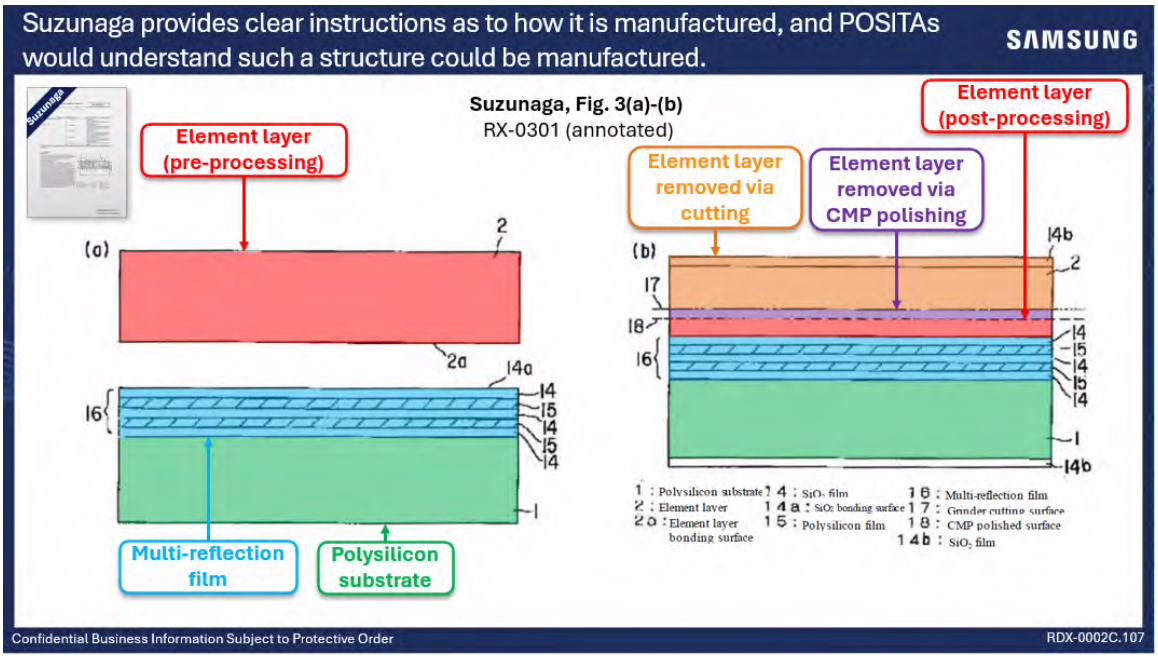
Q289 Are you aware of Dr. Mansoorian's argument that Suzunaga does not meet this limitation because Suzunaga's multi-reflection film 16 purportedly could not be manufactured?

A289 Yes. Dr. Mansoorian opines, without support, that "multi-reflection films 16 could not be manufactured as described" because "[f]or the reflection elements to function, the thickness of the element region cannot be more than 2 to 10 μm thick, i.e., the typical thickness of a backside illuminated image sensor," "Suzunaga does not describe how a piece of crystalline semiconductor that thin could be handled," and "it is not possible to handle silicon wafers that thin," RX-0911C, ¶319. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.96-97.

Contrary to Dr. Mansoorian's assertions, Suzunaga does describe how it is manufactured. As RDX-0002C.107 illustrates, first "[a]s depicted in FIG. 3(a) a SiO_2 film 14 formed by thermal oxidation and a polysilicon film 15 formed by CVD … are alternatively deposited on a silicon substrate 1." Suzunaga, [0043]. Next, "[a]s depicted in FIG. 3B the silicon substrate 1 and a silicon wafer that will become the element layer 2 are bonded together in a clean environment of class 10 or less," and then "are heat-treated in an oxidizing atmosphere at a temperature of 800°C to 1100°C for one hour." Suzunaga, [0074]-[0048]. Suzunaga next explains that "[t]he bonded state depicted in FIG. 3(b) obtained in this manner is extremely strong, so that the unnecessary thickness of the silicon wafer that will become the element layer 2 can be easily removed using a grinder down to the cutting surface 17." Suzunaga, [0050]. Next, Suzunaga explains that "CMP (Chemical-Mechanical Polishing) is further performed to remove material down to CMP polished surface 18." Suzunaga, [0051]. Suzunaga then goes on to explain the post-bonding manufacturing steps that take place to form features (e.g., dielectric isolation, pixels) in the element layer 2. *See* Suzunaga, [0051]-[0052].

Accordingly, Suzunaga is not teaching that thinner-than-normal wafers are being bonded as Dr. Mansoorian asserts. Instead, it is bonding two "wafer[s] purchased with normal specifications as a silicon wafer for mass production," Suzunaga, [0045], before removing the "unnecessary thickness," Suzunaga, [0050].

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3. Limitation 1[c]

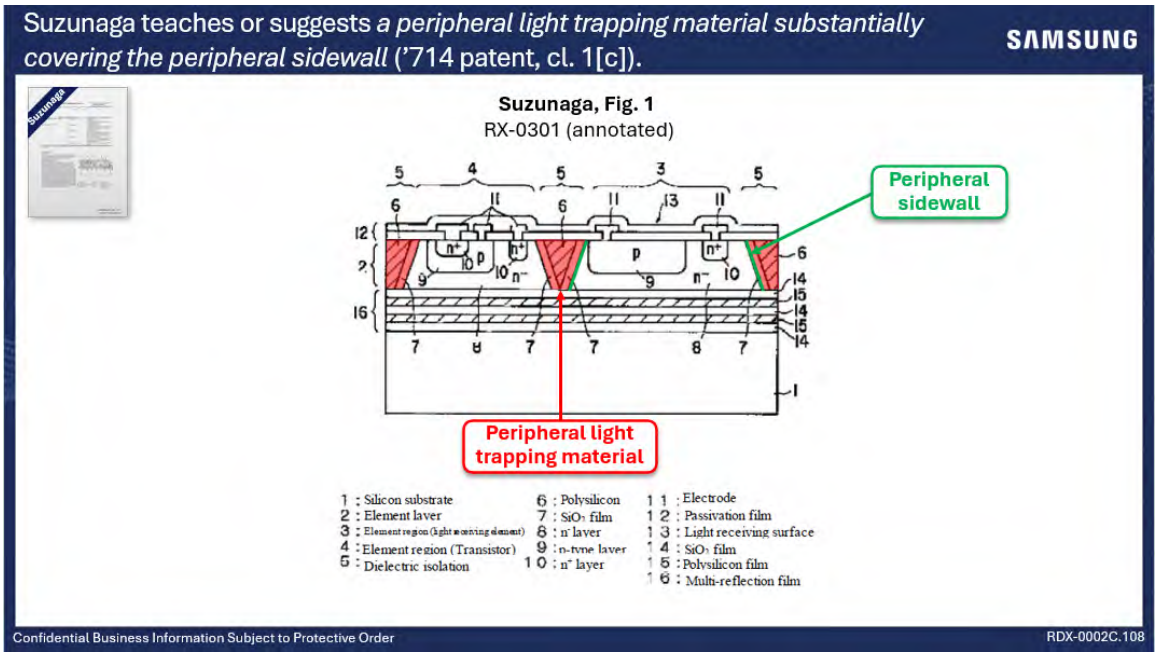
Q290 Limitation 1[c] is *a peripheral light trapping material substantially covering the peripheral sidewall*. Does Suzunaga satisfy this limitation?

A290 Yes. Suzunaga teaches or suggests *a backside light trapping material at least partially covering the backside surface*.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *light trapping material*. Suzunaga includes a *peripheral light trapping material*, including under either construction.

Q291 How does Suzunaga satisfy this limitation?

A291 As RDX-0002C.108 illustrates, Suzunaga's "dielectric isolation region 5 between the element regions 3 and 4 is formed by embedding polysilicon 6 in a V-groove with a SiO_2 film 7 or the like interposed therebetween as a dielectric body." Suzunaga, [0008]. Accordingly, it *substantially cover[s] the peripheral sidewall*.



Dielectric isolation region 5 constitutes a *light trapping material*. Suzunaga explains that "the SiO_2 film 7 in the element isolation region 5 [can be] also a multi-reflection film," such that it "can be used as part of the reflection surface when scattered light is incident from the incident surface 13." Suzunaga, [0064]. That is, Suzunaga's dielectric isolation region 5 can be configured such that is has a multi-reflection film to reflect light back into the pixel. As explained for limitation 1[b], Suzunaga teaches "almost 100% of the incident light passing through the element layer 2 can be reflected" by such multi-reflection films. Suzunaga, [0028].

Q292 How does dielectric isolation region 5 constitute a *light trapping material* under the parties' proposed constructions?

A292 Dielectric isolation region 5 constitutes a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

4. Limitation 1[d]

Q293 Limitation 1[d] is *wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel*. Does Suzunaga satisfy this limitation?

A293 Yes. As explained for limitations 1[b]-[c], Suzunaga teaches or suggests that *light contacting* both *the backside light trapping material* [and] *the peripheral light trapping material is reflected back towards the pixel*. Suzunaga teaches that "multi-reflection film [(*backside light trapping material*)] … reflects the transmitted light transmitted through the semiconductor light receiving element formed on the element layer, and impinges the reflected light again on the semiconductor element." Suzunaga, [0019]. Likewise, "the element isolation region 5 [(*peripheral light trapping material*)] [can be] a multi-reflection

film," such that it "can be used as part of the reflection surface when scattered light is incident from the light incident surface 13." Suzunaga, [0064].

5. Limitation 1[e]

Q294 Limitation 1[e] is *wherein at least one of the backside light trapping material or the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials*. Does Suzunaga satisfy this limitation?

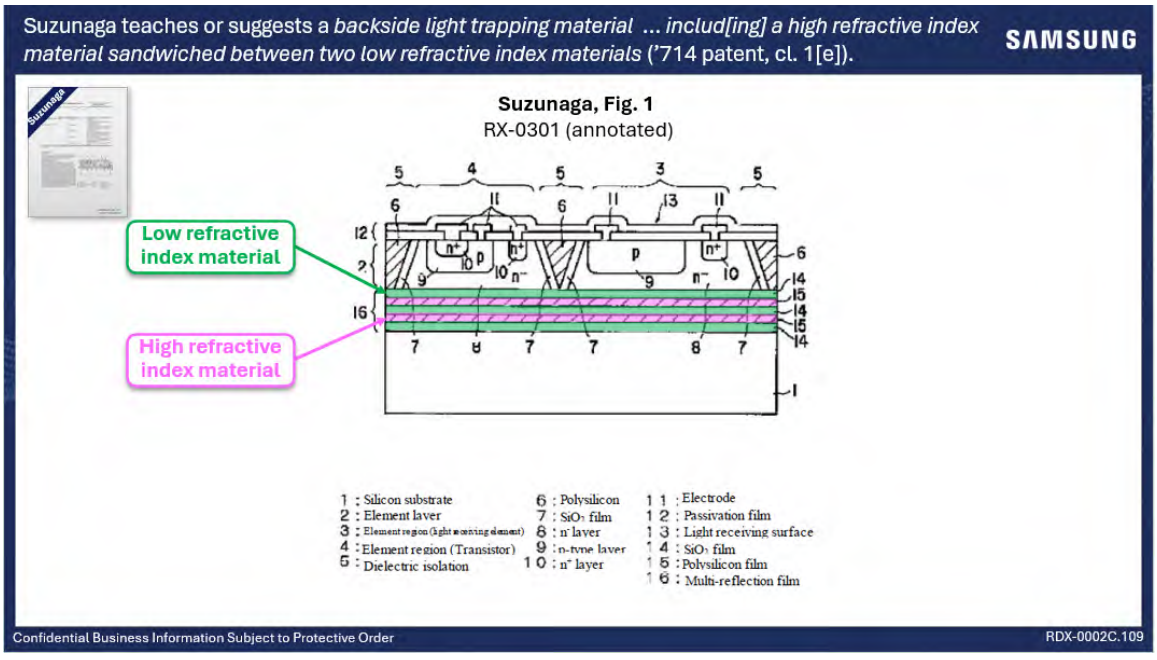
A294 Yes. Suzunaga teaches or suggests both a *backside light trapping material* and a *peripheral light trapping material* that *includes a high refractive index material sandwiched between two low refractive index materials*.

As explained in the Claim Construction Order, I understand that the ALJ has construed *high refractive index material* and *low refractive index material*, Order No. 36 at 31. Suzunaga's *high* and *low refractive index materials* satisfy this construction.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for limitation 1[e] as a whole. Suzunaga satisfies limitation 1[e] , including under either construction.

Q295 How does Suzunaga's *backside light trapping material* satisfy this limitation?

A295 As RDX-0002C.109 illustrates, Suzunaga's multi-reflection film 16 (*backside light trapping material*) consists of "SiO_2 films 14 and polysilicon films 15 [that] are alternately laminated." Suzunaga, [0027]; *see also* Suzunaga, [0021].



Suzunaga teaches that polysilicon has a refractive index of 3.5, and SiO_2 has a refractive index of 1.43~1.46. Suzunaga, Table 1.

Q296 Do Suzunaga's SiO_2 films 14 and polysilicon films 15 satisfy the ALJ's constructions?

A296 Yes. Polysilicon films 15 constitute a *high refractive index material*, as Suzunaga discloses that its polysilicon has a refractive index of greater than 2.1 (i.e., 3.5) and a refractive index that is at least 0.2 greater than the *low refractive index material* (i.e., SiO_2, which Suzunaga discloses having a refractive index of 1.43~1.46). Likewise, SiO_2 films 14 constitute a *low refractive index material*, as Suzunaga discloses that its SiO_2 has a refractive index of less than 2.1 (i.e., 1.43~1.46) and a refractive index that is at least 0.2 less than the *high refractive index material* (i.e., polysilicon, which Suzunaga discloses as having a refractive index of 3.5).

Q297 Does Suzunaga teach or suggest polysilicon films 15 being sandwiched between SiO_2 films 14?

A297 Yes. As RDX-0002C.109 illustrates, Suzunaga's multireflection film 16 includes at least one *high refractive index material* (polysilicon 15) *sandwiched between two low refractive index materials* (SiO_2 14).

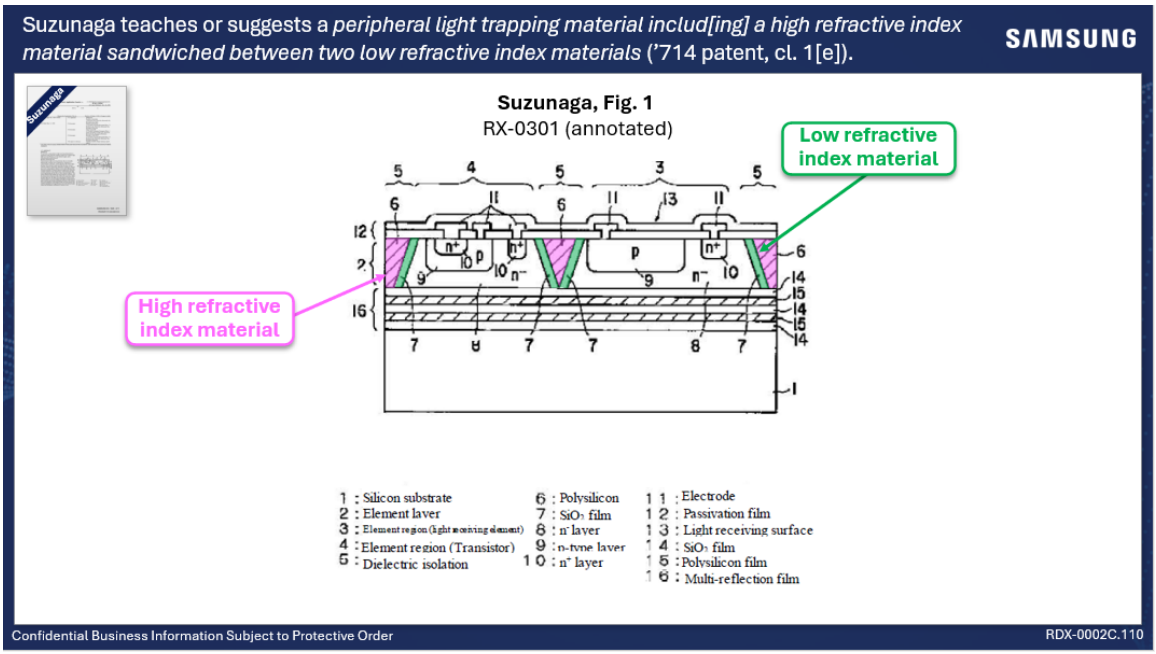
Q298 How do Suzunaga's disclosures satisfy the parties' proposed constructions for the disputed terms in these limitations?

A298 Suzunaga's multi-reflection film 16 would have a *high refractive index material* (polysilicon 15) in contact with (and in between) the *low refractive index materials* (SiO_2 14) on two opposing sides.

Q299 How does Suzunaga's *peripheral light trapping material* satisfy this limitation?

A299 As RDX-0002C.110 illustrates, Suzunaga teaches that its "dielectric isolation region 5 [(*peripheral light trapping material*)] … is formed by embedding polysilicon 6 in a V-groove with SiO_2 film 7 or the like interposed therebetween as a dielectric body." Suzunaga, [0008].

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Q300 Do Suzunaga's polysilicon 6 and SiO_2 film 7 satisfy the ALJ's constructions?

A300 Yes. Suzunaga teaches that polysilicon has a refractive index of 3.5, and SiO_2 has a refractive index of 1.43~1.46. Suzunaga, Table 1. Polysilicon 7 and SiO_2 film 7 constitute *high* and *low refractive index materials*, respectively. For the same reasons explained for Suzunaga's *backside light trapping material*, Suzunaga's polysilicon 7 and SiO_2 film satisfy the ALJ's constructions of *high* and *low refractive index materials*.

Q301 Does Suzunaga's *peripheral light trapping material* include a *high refractive index material sandwiched between two low refractive index materials*?

A301 Yes. Suzunaga teaches that "SiO_2 film 7 in the element isolation region 5 [can be] also a multi-reflection film," such that it "can be used as part of the reflection surface when scattered light is incident from the incident surface 13." Suzunaga, [0064]. That is, dielectric isolation 5 can be configured such that it is a multi-reflection film consisting of alternating layers of polysilicon and SiO_2, similar to multi-reflection film 16.

Accordingly, Suzunaga's *peripheral light trapping material* (dielectric isolation 5) includes a *high refractive index material* (polysilicon 6) *sandwiched between two low refractive index materials* (SiO_2 film 7).

Q302 How do Suzunaga's disclosures satisfy the parties' proposed constructions for the disputed terms in these limitations?

A302 Suzunaga's dielectric isolation 5 would have a *high refractive index material* (polysilicon 6) in contact with (and in between) the *low refractive index materials* (SiO_2 film 7) on two opposing sides.

b. Claim 12

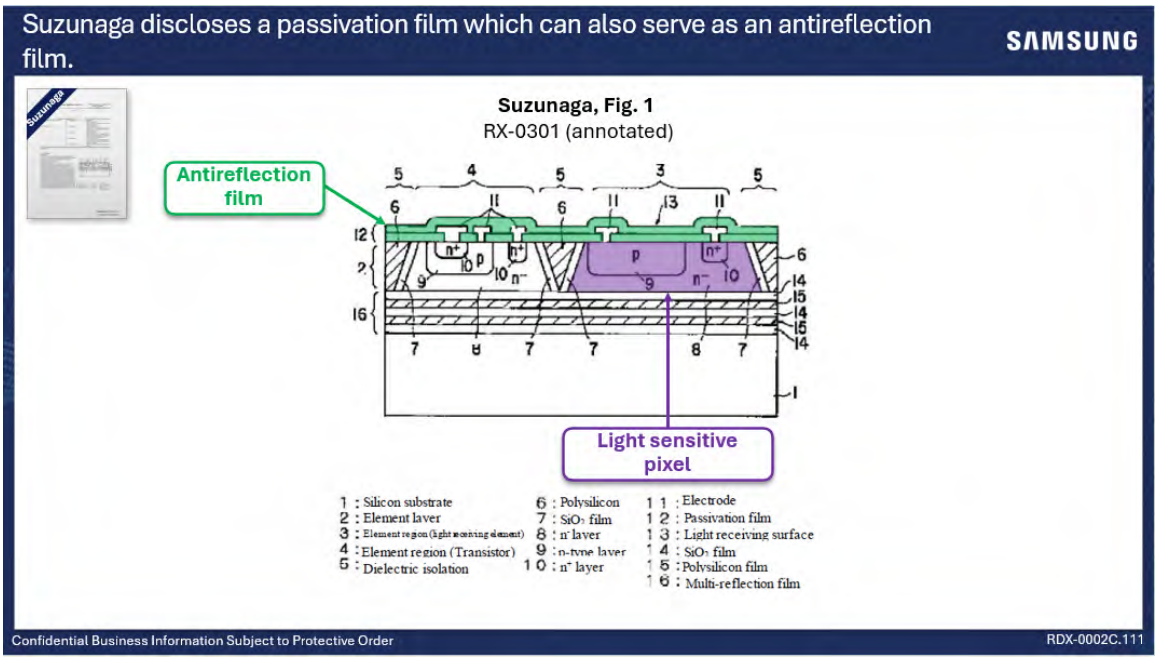
Q303 Let's turn to claim 12, which is *[t]he device of claim 1, further comprising a frontside light trapping material at least partially covering the light incident surface.* Does Suzunaga satisfy this claim?

A303 Yes. Suzunaga teaches or suggests a *frontside light trapping material at least partially covering the light incident surface*.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *light trapping material*. Suzunaga teaches or suggests a *frontside light trapping material*, including under either construction.

Q304 How does Suzunaga satisfy this limitation?

A304 As RDX-0002C.111 illustrates, Suzunaga includes "a passivation film [12] which covers the electrodes [11] and the wiring connecting the electrodes" that "can also serve as an antireflection film on the light receiving surface 13." Suzunaga, [0010].



Q305 Is Suzunaga's antireflection film a *light trapping material*?

A305 Suzunaga does not state whether the antireflection film reflects light back into the pixel. However, POSITAs would have understood that antireflection films can be configured to be reflective, and configuring Suzunaga's antireflection film to reflect light back into the pixel (i.e., act as a *light trapping material*) to increase Suzunaga's efficiency would have been obvious. As an example, Suzunaga explains that its "multi-reflection film" (*backside light trapping material*) is used to "reflect[] incident light onto the light receiving element formed in the element region so as to be incident on the light receiving element again,

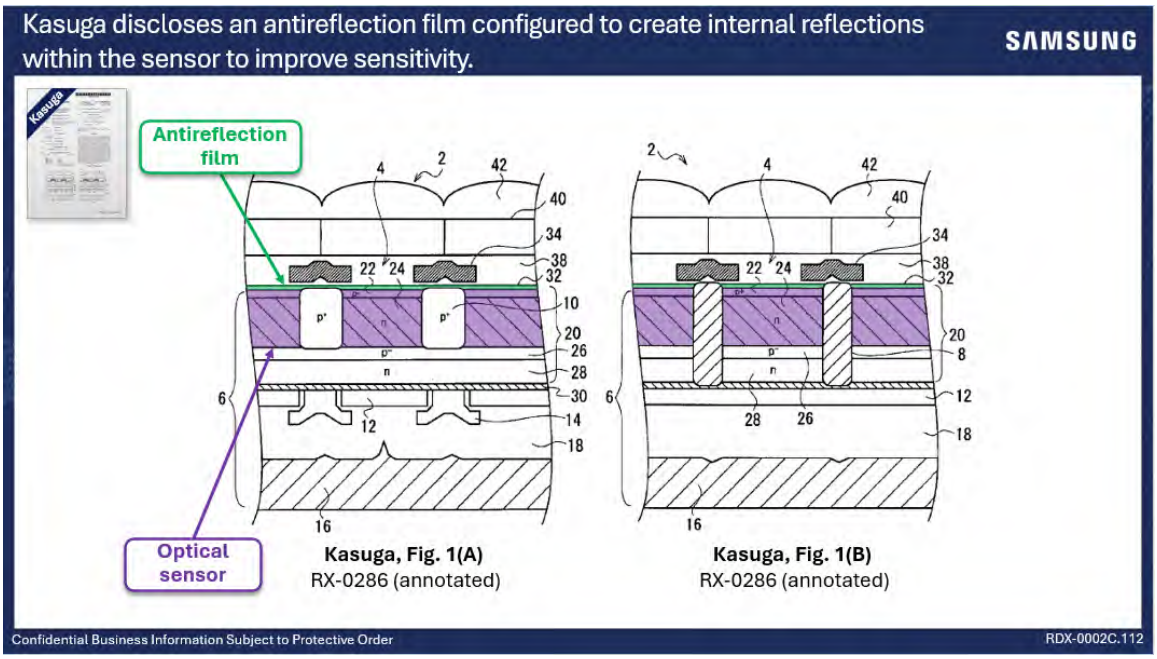
thereby … obtaining a semiconductor light receiving element that exhibits high light receiving efficiency." Suzunaga, Abstract.

Q306 How does Suzunaga's antireflection film constitute a *light trapping material* under the parties' proposed constructions?

A306 Suzunaga's antireflection film constitutes a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

Q307 Were antireflective films used to reflect light back into the pixel of other devices?

A307 Yes. Using antireflection films to reflect light back into the pixel was a well-known technique used in similar devices. For example, as discussed, Kasuga includes an "antireflection film 32 [that] is formed on the surfaces of the optical sensors 4 to prevent the reflection of light entering the optical sensors," Kasuga, 4:4-7, as RDX-0002C.112 illustrates.



Kasuga teaches that its antireflection film creates internal reflections within the sensor that improve sensitivity. For example, Kasuga teaches that, by using an antireflection film, "[e]ven if the returning light passes through the optical sensors 4 again, it is reflected by … the antireflection film 32, and is converted into electric charge by the optical sensors 4." Kasuga, 5:18-22. This allows for "multiple reflection of light [to] occur," resulting in "the photoelectric conversion of incident light [being] extremely efficient." Kasuga, 5:22-31. Additionally, Kasuga teaches that:

> [W]hen the material and thickness of the antireflection film 32 are suitably selected such that light reflected by the top surface of the antireflection film 32 and light reflected by the bottom surface of the antireflection film 32

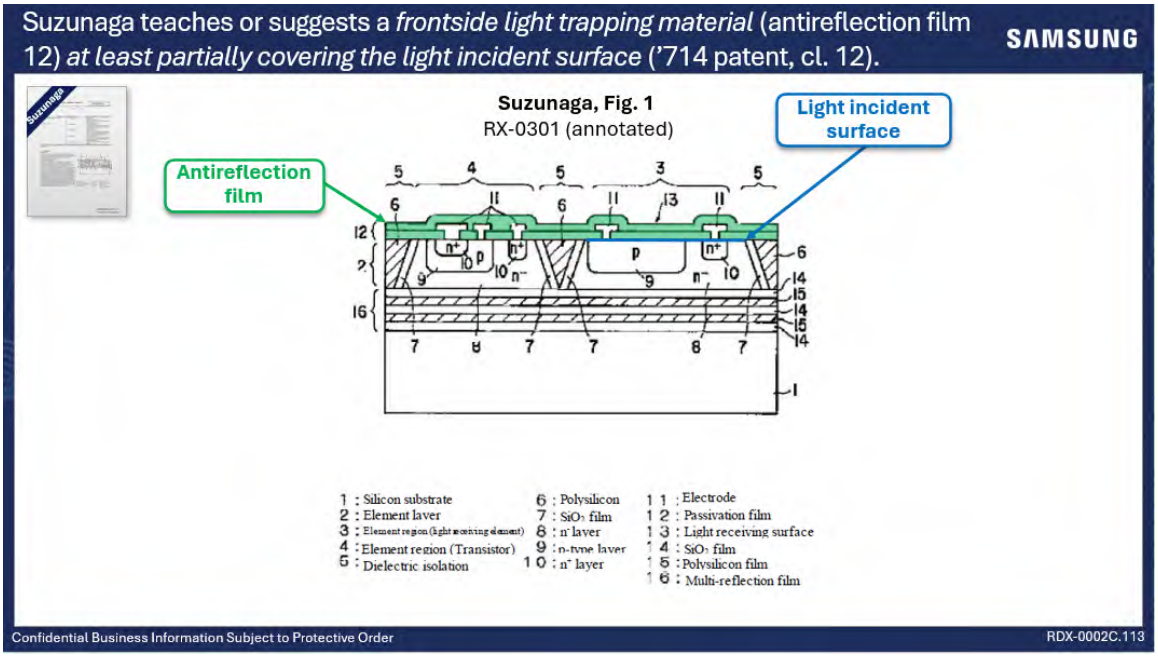
> interfere with each other so as to intensify each other, the intensity of the reflected light [attempting to leave the pixel] further increases and the sensitivity [of the imaging device] can be further increased.

Kasuga, 5:40-43.

Accordingly, it would have been at least obvious based on Suzunaga's teachings to select a material and thickness of its antireflection film 12 such that it reflects light back into the pixel, i.e., constitutes a *light trapping material*, including under either party's proposed construction.

Q308 Does Suzunaga's antireflection film *at least partially cover[] the light incident surface*?

A308 Yes. As RDX-0002C.113 illustrates, Suzunaga's antireflection film 12 (*frontside light trapping material*) *at least partially cover[s] the light incident surface* (Suzunaga's p-n^- n^+ structure located in the element layer 2).



Q309 Are you aware of Dr. Mansoorian's argument that Suzunaga cannot be manufactured with an antireflection film?

A309 Yes. Dr. Mansoorian opines that POSITAs "would know … Suzunaga could not be manufactured to include an anti-reflection film," as Suzunaga is a front side illuminated sensor containing frontside circuitry and POSITAs "would understand that antireflection films are not effective in front side illumination sensors." RX-0911C, ¶322. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.1176-1177.

First, POSITAs would understand that Suzunaga can be manufactured to include an antireflection film, as it is expressly taught by Suzunaga. *See* Suzunaga, Fig. 1 (depicting a passivation film 12), [0010] ("passivation film … can also serve as an antireflection

film"). Dr. Mansoorian appears to opine that—because the frontside circuitry would purportedly be at least 1000nm thick (an assertion for which he cites no evidence in support)—that POSITAs could not engineer an antireflection film into the circuitry. However, Suzunaga depicts its antireflection film on top of its circuitry (as opposed to within it), thus alleviating Dr. Mansoorian's concern.

Second, Dr. Mansoorian's assertion that antireflection films are incompatible in FSI devices is contradicted by SiOnyx's own patent applications. *See* Haddad188, 25:4-6 ("Fig. 16 shows a front side illuminated (FSI) imager…. A lens 160 and an antireflecting passivation layer on [*sic*] 62 are coupled to the front side of the pixel."). Accordingly, POSITAs would understand that an antireflection film could be used in Suzunaga, as evidenced by Suzunaga and SiOnyx's own teachings.

Q310 Are you aware of Dr. Mansoorian's argument that Suzunaga's antireflection film is not a *light trapping material*?

A310 Yes. Dr. Mansoorian opines that "the primary purpose of the passivation film … is to insulate any electric charges," and that "[t]he fact it may be used as an antireflective film is of secondary consideration," to argue that POSITAs would not be motivated to make it *light trapping*. RX-0911C, ¶322. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.1176-1177.

Even to the extent antireflection is a secondary objective, it is still expressly considered by Suzunaga, and as I explained, making it antireflective—and configuring it to trap light within Suzunaga's pixel—would increase Suzunaga's sensitivity.

Q311 Are you aware of Dr. Mansoorian's argument that POSITAs would not use Suzunaga's multi-reflection film 16 on the light incident side?

A311 Yes. Dr. Mansoorian appears to have misunderstood my analysis by thinking that I opined a POSITA would place Suzunaga's multi-reflection film 16 on the light incident side. *See* RX-0911C, ¶324. To the contrary, in paragraph 611 of my expert report, I was opining that, because Suzunaga uses a multi-reflection film 16 to reflect light back into the pixel, it would be obvious that some light could therefore impinge upon the bottom surface of Suzunaga's antireflection film such that it could then be reflected back into Suzunaga's pixel (therefore trapping light within the pixel).

c. Claim 13

Q312 Let's turn to claim 13, which is *[t]he device of claim 12, wherein the frontside light trapping material is an antireflective layer coating*. Does Suzunaga satisfy this claim?

A312 Yes. As discussed for '714 patent (Ground 7), claim 12, Suzunaga's *frontside light trapping material*, i.e., "passivation film 12" "can also serve as an antireflection film." Suzunaga, [0010].

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d. Claim 18

Q313 Let's turn to claim 18, which is *[t]he device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface*. Does Suzunaga satisfy this claim?

A313 As explained regarding the Terms Remaining in Dispute, I understand that Samsung proposed the term *sloped surface at the pixel device interface* is indefinite, and that SiOnyx proposed it has its plain and ordinary meaning, and to the extent a construction is required, it means sloped trench wall or sloped backside surface.

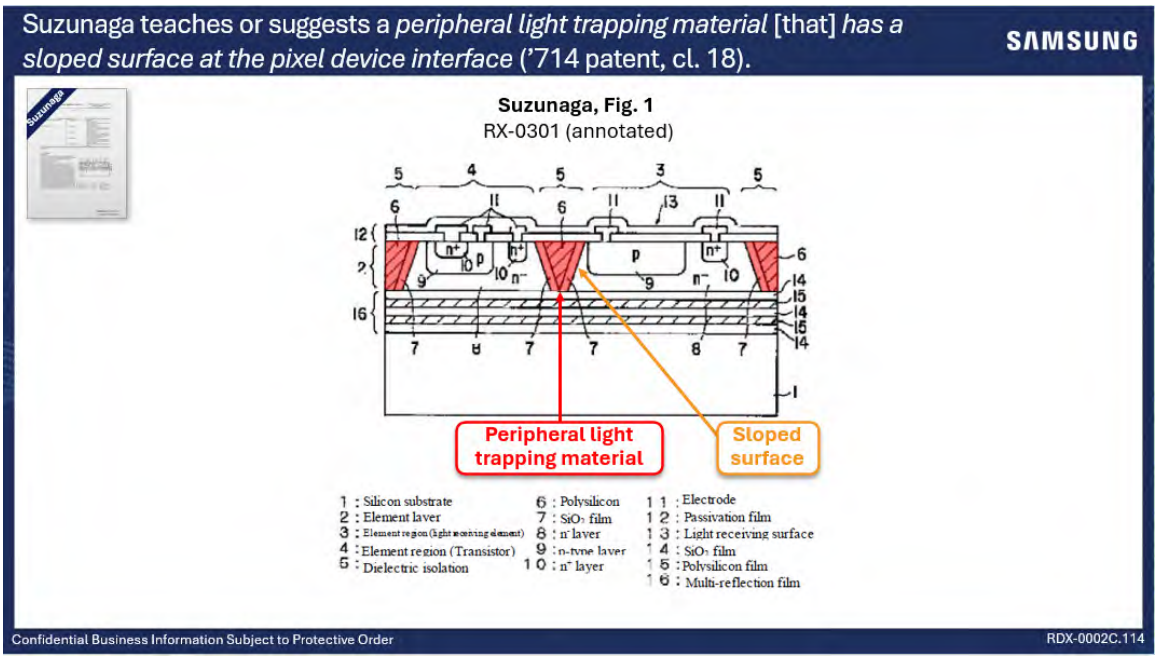
It is unclear what is meant by *a sloped surface at the pixel device interface*, in particular, what is meant by a *pixel device interface*. There is no discussion in the specification of a *pixel device interface*, and the term lacks antecedent basis, such that the specification fails to inform POSITAs, with reasonable certainty, of the claim's scope.

To the extent the limitation is not indefinite, Suzunaga includes a *peripheral light trapping material* that *has a sloped surface at the pixel device interface*.

Q314 Assuming the limitation is not indefinite, how does Suzunaga satisfy this limitation?

A314 As RDX-0002C.115 illustrates, "dielectric isolation region 5 [(*peripheral light trapping material*)] … is formed by embedding polysilicon 6 in a V-groove." Suzunaga, [0008]. *See also* Suzunaga, [0042], [0071].

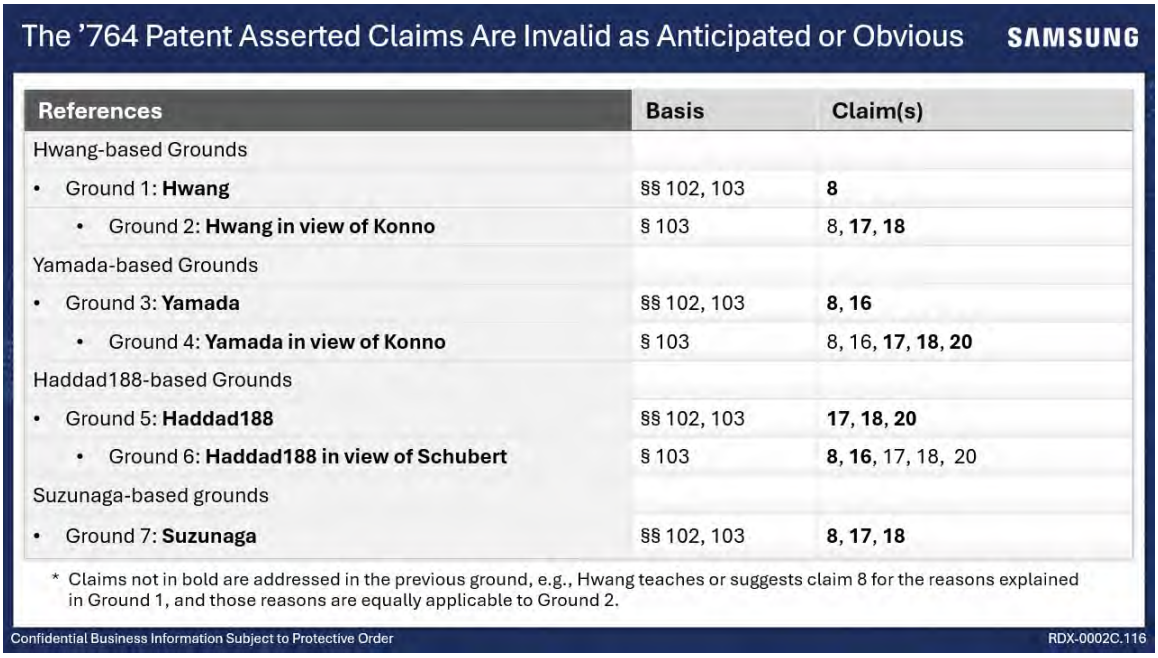
Suzunaga's V-groove accordingly a *sloped surface*.



VI. '764 Patent Invalidity Based on Anticipation and Obviousness

Q315 Let's turn to the '764 patent. Can you summarize your opinions with respect to anticipation and obviousness of the '764 patent?

A315 Yes. As RDX-0002C.116 illustrates, in my opinion the '764 patent Asserted Claims are invalid based on four primary references: Hwang, Yamada, Haddad188, and Suzunaga.



A. Hwang-based Grounds

Q316 Let's start with your Hwang-based opinions. Can you please summarize your anticipation and obviousness opinions about the '764 patent based on Hwang?

A316 My Hwang-based opinions are divided into two grounds. Ground 1 is that Hwang anticipates, or at least renders obvious, claim 8. Ground 2 is that Hwang and Konno render obvious claims 8, 17, and 18.

1. Ground 1: Hwang Anticipates, or at Least Renders Obvious, Claim 8

a. Claim 8

1. Limitation 8[a]

Q317 Let's start with your Ground 1 opinions that Hwang anticipates, or at least renders obvious, claim 8.

Are you aware of Dr. Mansoorian's assertion that you rely on the combination of Hwang, Konno, and Mori for claim 8?

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A317 Yes. Dr. Mansoorian asserts that I do "not render an opinion that any reference anticipates claim 8," and that I "rely on the combination of Hwang, Konno, and Mori." RX-0911C, ¶357. I disagree. As shown in my expert report and as I will explain, my opinion is that Hwang anticipates, or at least renders obvious, claim 8 and do not rely on Konno or Mori.

Q318 Claim 8's first limitation, 8[a], is at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery. Does Hwang satisfy this limitation?

A318 Yes. As RDX-0002C.118 illustrates, '764 patent, limitation 8[a] is identical to '714 patent, limitation 1[a]. Hwang teaches or suggests '764 patent, limitation 8[a] for the reasons discussed for '714 patent (Ground 1), limitation 1[a].

2. Limitation 8[b]

Q319 Limitation 8[b] is *a backside light trapping material substantially covering the backside surface*. Does Hwang satisfy this limitation?

A319 Yes. As RDX-0002C.119 illustrates, with differences shown in red, '764 patent, limitation 8[b] is identical to '714 patent, limitation 1[b], except that '764 patent, limitation 8[b] requires that the backside light trapping material *substantially* covers the backside surface, as opposed to '714 patent, limitation 1[b]'s requirement that it only *at least partially* covers the backside surface.

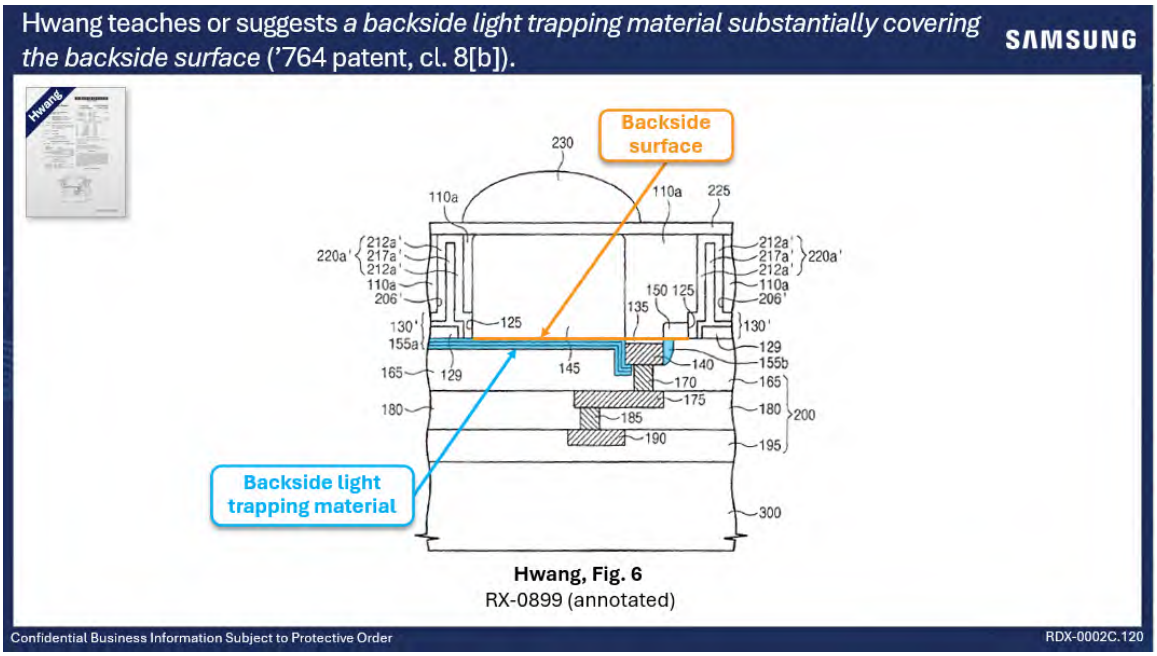
As discussed for '714 patent (Ground 1), limitation 1[b], Hwang teaches or suggests *a backside light trapping material at least partially covering the backside surface*. Hwang further teaches or suggests *a backside light trapping material substantially covering the backside surface*. Dr. Mansoorian has not disputed this.

Q320 Why does Hwang's *backside light trapping material substantially cover[] the backside surface*?

A320 Hwang's *backside light trapping material* (base multi-layered reflection layer 155*a* and spacer 155*b*) completely or nearly completely covers the backside surface. Hwang explains that base multi-layered reflection layer 155*a* is included in Hwang's image sensor so that "light that is incident on the photodiode is reflected by the base multi-layered reflection layer and re-enters the photodiode" such that "the sensitivity of the image sensor is improved." Hwang, 15:38-41.

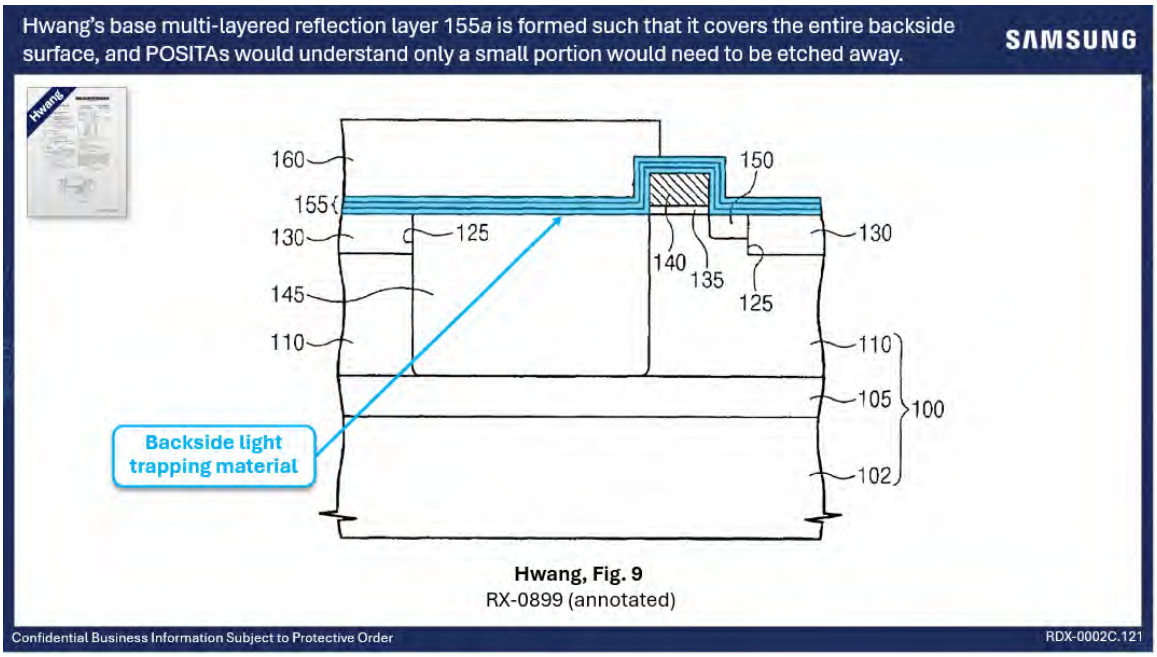
Consistent with that function, as RDX-0002C.120 illustrates, base multi-layered reflection layer 155*a* substantially covers the backside surface. Additionally, Hwang teaches that gate spacer 155*b* "can include the same material as the base multi-layered reflection layer 155*a*," Hwang, 7:35-55, and that base multi-layered reflection layer 155*a* can be "extended to cover a portion of the second surface of the gate electrode 140," Hwang, 7:45-51. In such instances, base multi-layered reflection layer 155*a* (shown in blue) (*backside light trapping material*) nearly completely covers the backside surface (particularly when viewed in three dimensions).

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Q321 Are there any other reasons why you believe Hwang satisfies this limitation?

A321 Yes. POSITAs would be motivated to maximize the amount of area covered by base multi-layered reflection layer 155*a* to maximize the amount of light reflected back into the pixel. *See* Hwang, 15:38-41. As RDX-0002C.121 illustrates, base multi-layered reflection layer 155*a* is formed during manufacturing such that it entirely covers the backside surface, including both photodiode 145 and pixel semiconductor pattern 110*a*. POSITAs would understand that while it may be necessary to etch away a small portion of base multi-layered reflection layer 155*a* around the gate electrode 140 to form the transistor connecting the pixel to the supporting circuitry (as RDX-0002C.120 illustrates), the remainder of the backside surface would be left covered. *See* Hwang, 4:56-58 ("drawings are not necessarily to scale, emphasis instead being placed upon illustrating aspects of the invention").



3. Limitation 8[c]

Q322 Limitation 8[c] is *a peripheral light trapping material substantially covering the peripheral sidewall*. Does Hwang satisfy this limitation?

A322 Yes. As RDX-0002C.122 illustrates, '764 patent, limitation 8[c] is identical to '714 patent, limitation 1[c]. Hwang teaches or suggests '764 patent, limitation 8[c] for the reasons discussed for '714 patent (Ground 1), limitation 1[c].

4. Limitations 8[d]-[e]

Q323 Limitations 8[d]-[e] are *wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials*, (8[d]), and *wherein the difference in refractive index between the first material and the two second materials is at least 0.2* (8[e]). Does Hwang satisfy these limitations?

A323 Yes. Hwang teaches or suggests this limitation. Dr. Mansoorian has not disputed this.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *a first material sandwiched between two second materials*. Hwang satisfies this limitation under either construction.

Q324 How does Hwang satisfy this limitation?

A324 As discussed for '714 patent, (Ground 1), limitation 1[e], both Hwang's *backside* and *peripheral light trapping material* (155*a* and 220*a*') *include a first material* (layers 152 and 217*a*') having "a refractive index of approximately 4," *sandwiched between two second*

materials (layers 151 and 212*a*') having "a refractive index of approximately 1.46," Hwang, 9:25-30, with a difference of approximately 2.54 (*at least 0.2*). *See* Hwang, 8:40-52, 10:2-5.

Q325 How do Hwang's disclosures satisfy the parties' proposed constructions for the disputed terms in these limitations?

A325 As discussed for '714 patent (Ground 1), limitation 1[e], Hwang's structure meets these limitations, including under either party's construction, as the *first material* is in contact with (and in between) the *two second materials* on two opposing sides.

5. Limitation 8[f]

Q326 Limitation 8[f] is *wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel*. Does Hwang satisfy this limitation?

A326 Yes. As RDX-0002C.123 illustrates, '764 patent, limitation 8[f] is identical to '714 patent, limitation 1[d]. Hwang teaches or suggests '764 patent, limitation 8[f] for the reasons discussed for '714 patent (Ground 1), limitation 1[d].

2. Ground 2: Hwang and Konno Renders Obvious Claims 8, 17-18, 21, and 23

Q327 Let's turn to your Ground 2 opinions. Can you please summarize your Ground 2 opinions?

A327 In my opinion, Hwang and Konno render obvious claims 8, and 17-18. As explained for Ground 1, Hwang anticipates, or at least renders obvious, claim 8. Those opinions are equally applicable to my Ground 2 opinions regarding Hwang and Konno, which further render obvious claims 17-18.

a. Claim 17

Q328 Let's turn to claim 17. Have you formed an opinion regarding claim 17?

A328 Yes. Hwang and Konno render obvious claim 17. As RDX-0002C.125 illustrates, limitations 17[a]-[c] and 17[e] are identical to limitations 8[a]-[c] and 8[f]. Hwang teaches or suggests these limitations for the reasons discussed for '764 patent (Ground 1), claim 8. The only limitation not identical to claim 8 is limitation 17[d].

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1. Limitation 17[d]

Q329 Limitation 17[d] is *wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface*. Have you formed an opinion regarding limitation 17[d]?

A329 Yes. As RDX-0002C.126 illustrates, '764 patent, claim 17[d] is identical to '714 patent, claim 18's additional limitations. Hwang in view of Konno render obvious '764 patent, claim 17[d] for the reasons discussed for '714 patent (Ground 3), claim 18.

b. Claims 18

Q330 Let's turn to claim 18 which is *[t]he device of claim 17, wherein the peripheral sidewall extends completely around the pixel periphery*. Have you formed an opinion regarding this claim?

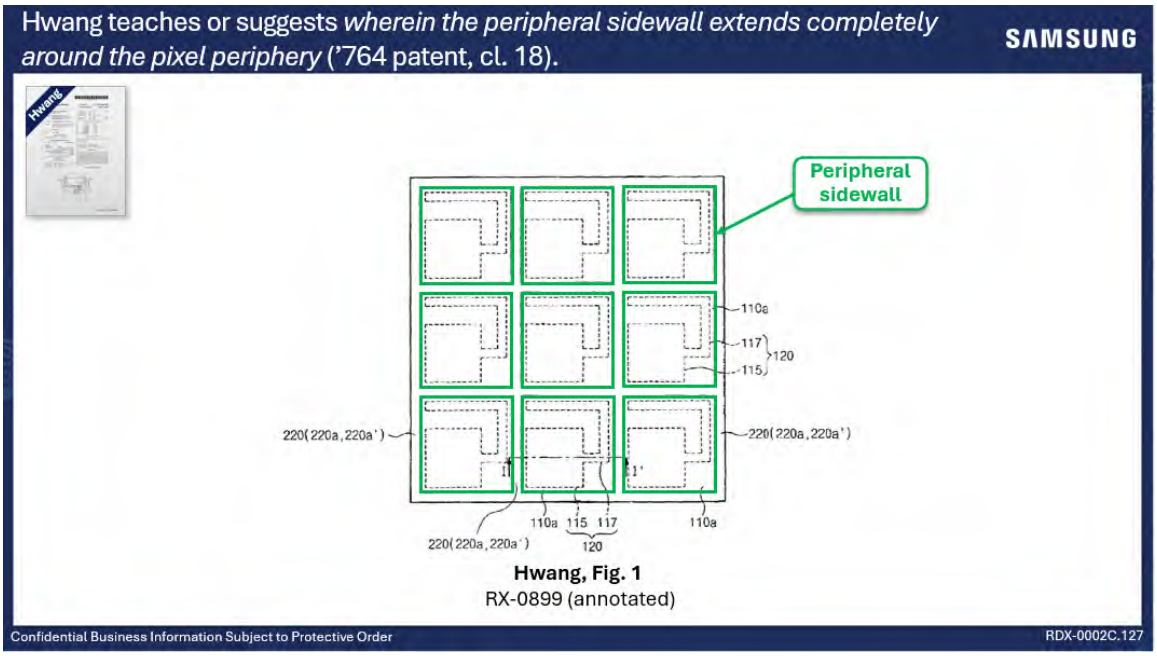
A330 As explained regarding the Terms Remaining in Dispute, I understand that Samsung proposed the limitation *extends completely around the pixel periphery* is indefinite, and that SiOnyx proposed it means surrounding the pixel.

It is unclear how the peripheral sidewall can be simultaneously both disposed into and around the pixel. However, in view of Dr. Foty's interpretation and application of this limitation in his infringement and technical DI opinions where this limitation is allegedly satisfied because the peripheral sidewall defines the bounds of the pixel, and to the extent this term is not indefinite, Hwang and Konno render it obvious. Dr. Mansoorian has not disputed this.

Q331 How do Hwang and Konno render claim 18 obvious?

As discussed for '714 patent, (Ground 1), limitation 1[a], Hwang teaches that "sidewall multi-layered reflection layer 220 [220*a*' in Figure 6] encloses the side walls of pixel semiconductor patterns 110*a*." Hwang, 6:15-17. This is expected, as POSITAs would understand that the *peripheral sidewall* should extend completely around the pixel to increase isolation. Accordingly, as RDX-0002C.127 illustrates, the *peripheral sidewall*—i.e., where pixel semiconductor pattern 110*a* contacts sidewall reflection layer 220 (220*a*' in Figure 6)—extends *completely around the pixel periphery*.

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B. Yamada-based Grounds

Q332 Let's turn to your Yamada-based opinions. Can you please summarize your anticipation and obviousness opinions about the '764 patent based on Yamada?

A332 My Yamada-based opinions are divided into two grounds. Ground 3 is that Yamada anticipates, or at least renders obvious, claims 8 and 16. Ground 4 is that Yamada and Konno render obvious claims 8, 16-18, and 20.

1. Ground 3: Yamada Anticipates, or at Least Renders Obvious, Claims 8 and 16

a. Claim 8

1. Limitation 8[a]

Q333 Let's start with your Ground 3 opinions that Yamada, anticipates, or at least renders obvious, claims 8 and 16.

Claim 8's first limitation, 8[a], is *at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery*. Does Yamada satisfy this limitation?

A333 Yes. As RDX-0002C.129 illustrates, '764 patent, limitation 8[a] is identical to '714 patent, limitation 1[a]. Yamada teaches or suggests '764 patent, limitation 8[a] for the reasons discussed for '714 patent (Ground 4), limitation 1[a].

2. Limitation 8[b]

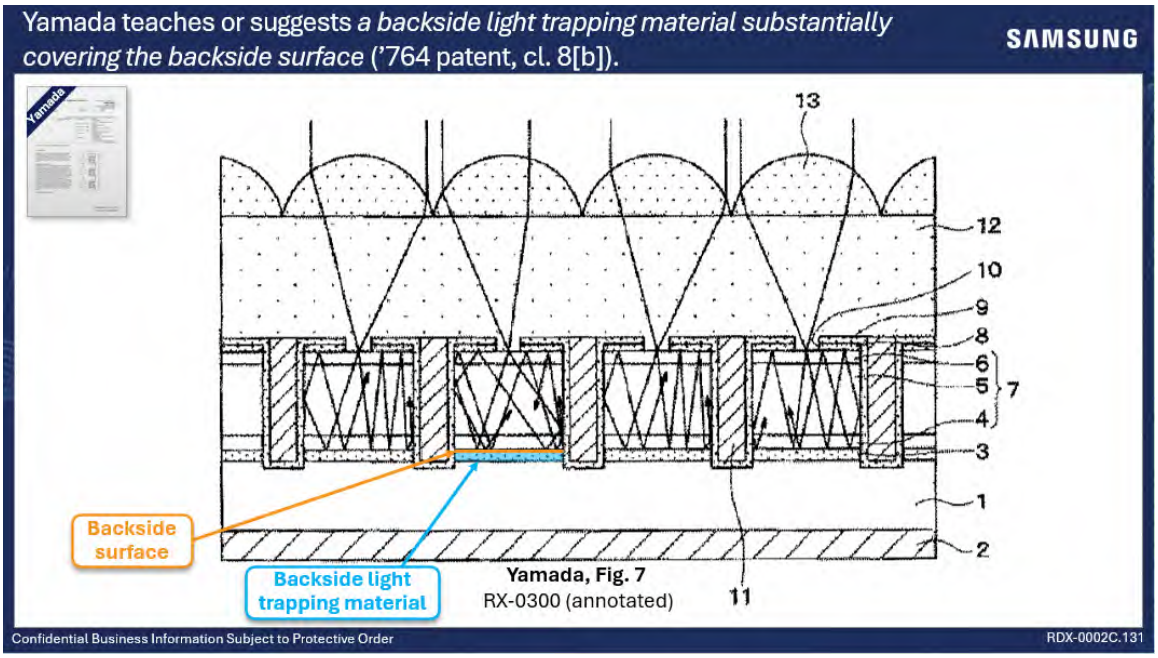
Q334 Limitation 8[b] is *a backside light trapping material substantially covering the backside surface*. Does Yamada satisfy this limitation?

A334 Yes. As RDX-0002C.130 illustrates, with differences shown in red, '764 patent, limitation 8[b] is identical to '714 patent, limitation 1[b], except that '764 patent, limitation 8[b] requires that the backside light trapping material *substantially* covers the backside surface, as opposed to '714 patent, limitation 1[b]'s requirement that it only *at least partially* covers the backside surface.

As discussed for '714 patent (Ground 4), limitation 1[b], Yamada teaches or suggests *a backside light trapping material* <u>*at least partially*</u> *covering the backside surface*. Yamada further teaches or suggests *a backside light trapping material* <u>*substantially*</u> *covering the backside surface*. Dr. Mansoorian has not disputed this.

Q335 How does Yamada's *backside light trapping material* <u>*substantially*</u> *cover[] the backside surface*?

A335 As RDX-0002C.131 illustrates, Yamada's *backside light trapping material* (first reflective film 3) covers the entire backside surface, and therefore *substantially cover[s]* it as well. POSITAs would expect that first reflective film 3 covers the backside surface in both directions, consistent with its role in reflecting light back into the light receiving element 7. *See* Yamada, [0022], [0009] (disclosing a "first reflective film (3)," that is "arranged at a bottom surface [*backside surface*] of the light receiving section (7)").



3. Limitation 8[c]

Q336 Limitation 8[c] is *a peripheral light trapping material substantially covering the peripheral sidewall*. Does Yamada satisfy this limitation?

A336 Yes. As RDX-0002C.132 illustrates, '764 patent, limitation 8[c] is identical to '714 patent, limitation 1[c]. Yamada teaches or suggests '764 patent, limitation 8[c] for the reasons discussed for '714 patent (Ground 4), limitation 1[c].

4. Limitation 8[d]-[e]

Q337 Limitations 8[d]-[e] are *wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials*, (8[d]), and *wherein the difference in refractive index between the first material and the two second materials is at least 0.2* (8[e]). Does Yamada satisfy these limitations?

A337 Yes, under Dr. Foty's interpretation and application of these limitations in his infringement and technical DI opinions where he has relied upon bulk refractive index values.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *a first material sandwiched between two second materials*. Yamada satisfies this limitation under either construction.

Q338 How does Yamada satisfy this limitation?

A338 As discussed for '714 patent (Ground 4), limitation 1[e], Yamada's *backside light trapping material* (first reflective film 3) *includes a first material* formed of gallium phosphide (with a refractive index of approximately 3.5) *sandwiched between two second materials* formed of aluminum phosphide (with a refractive index of approximately 2.75), with a difference of approximately 0.75 (*at least 0.2*).

Q339 How do Yamada's disclosures satisfy the parties' proposed constructions for the disputed terms in these limitations?

A339 As discussed for '714 patent (Ground 4), limitation 1[e], Yamada's structure meets these limitations, including under either party's construction, as the *first material* is in contact with (and in between) the *two second materials* on two opposing sides.

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5. Limitation 8[f]

Q340 Limitation 8[f] is *wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel*. Does Yamada satisfy this limitation?

A340 Yes. As RDX-0002C.133 illustrates, '764 patent, limitation 8[f] is identical to '714 patent, limitation 1[d]. Yamada teaches or suggests '764 patent, limitation 8[f] for the reasons discussed for '714 patent (Ground 4), limitation 1[d].

b. Claim 16

Q341 Let's turn to claim 16, which is *[t]he device of claim 8, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer*. Does Yamada satisfy this claim?

A341 Yes. As RDX-0002C.134 illustrates, '764 patent, claim 16's additional limitations are identical to '714 patent, claim 17's additional limitations. Yamada teaches or suggests '764 patent, claim 16's additional limitations for the reasons discussed for '714 patent (Ground 4), claim 17.

2. Ground 4: Yamada and Konno Render Obvious Claims 8, 16-18, and 20

Q342 Let's turn to your Ground 4 opinions. Can you please summarize your Ground 4 opinions?

A342 In my opinion Yamada and Konno render obvious claims 8, 16-18, and 20. As explained for Ground 3, Yamada anticipates, or at least renders obvious, claims 8 and 16. Those opinions are equally applicable to my Ground 4 opinions regarding Yamada and Konno, which further render obvious claims 17-18 and 20.

a. Claim 17

Q343 Let's turn to claim 17. Have you formed an opinion regarding claim 17?

A343 Yes. Yamada and Konno render obvious claim 17. As RDX-0002C.136 illustrates, limitations 17[a]-[c] and 17[e] are identical to limitations 8[a]-[c] and 8[f]. Yamada teaches or suggests these limitations for the reasons discussed for '764 patent (Ground 3), claim 8. The only limitation not identical to claim 8 is limitation 17[d].

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1. Limitation 17[d]

Q344 Limitation 17[d] is *wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface*. Have you formed an opinion regarding limitation 17[d]?

A344 Yes. As RDX-0002C.137 illustrates, '764 patent, claim 17[d] is identical to '714 patent, claim 18's additional limitations. Yamada and Konno render obvious '764 patent, claim 17[d] for the reasons discussed for '714 patent (Ground 5), claim 18.

b. Claim 18

Q345 Let's turn to claim 18, which is *[t]he device of claim 17, wherein the peripheral sidewall extends completely around the pixel periphery*. Have you formed an opinion regarding this claims?

A345 As explained regarding the Terms Remaining in Dispute, I understand that Samsung proposed the limitation *extends completely around the pixel periphery* is indefinite, and that SiOnyx proposed it means surrounding the pixel.

It is unclear how the peripheral sidewall can be simultaneously both disposed into and around the pixel. However, in view of Dr. Foty's interpretation and application of this limitation in his infringement and technical DI opinions where this limitation is allegedly satisfied because the peripheral sidewall defines the bounds of the pixel, and to the extent this term is not indefinite, Yamada and Konno render it obvious. Dr. Mansoorian has not disputed this.

Q346 How do Yamada and Konno render claim 18 obvious?

A346 As discussed for '714 patent (Ground 4), limitation 1[a], Yamada teaches that "[e]ach of the embodiments is configured such that the entire side surfaces of the PIN photodiode 7 is covered by the third reflective films 11," Yamada, [0056], and that "PIN photodiode 7 is surrounded by the … third reflective films 11, so when light is incident to the PIN photodiode 7, that light is reflected by … third reflective films 11 so as to be confined within PIN photodiode 7," Yamada, [0036]. This is expected, as POSITAs would understand that the *peripheral sidewall* should extend completely around the pixel to increase isolation.

c. Claim 20

Q347 Let's turn to claim 20, which is *[t]he device of claim 17, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer*. Does Yamada satisfy this claim?

A347 Yes. As RDX-0002C.138 illustrates, '764 patent claim 16's additional limitations are identical to '764 patent, claim 20's additional limitations as well as '714 patent, claim 17's additional limitations. Yamada teaches or suggests claim 20 for the reasons discussed for '764 patent (Ground 3), claim 16 and '714 patent (Ground 4), claim 17. Specifically,

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Yamada includes a *peripheral light trapping material*, i.e., "third reflective film (11)." Yamada explains that "third reflective film (11) can be composed of a metal" "such as Al." Yamada, [0012], [0026].

C. Haddad188-based Grounds

Q348 Let's turn to your Haddad188-based opinions. Can you please summarize your anticipation and obviousness opinions about the '764 patent based on Haddad188?

A348 My Haddad188-based opinions are divided into two grounds. Ground 5 is that Haddad188 anticipates, or at least renders obvious, claims 17-18, and 20. Ground 6 is that Haddad188 and Schubert render obvious claims 8, 16-18, and 20.

1. Ground 5: Haddad188 Anticipates, or at Least Renders Obvious, Claims 17-18, and 20

a. Claim 17

1. Limitation 17[a]

Q349 Let's start with your Ground 5 opinions that Haddad188 anticipates, or at least renders obvious, claims 17-18, and 20.

Claim 17's first limitation, 17[a], is at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery. Does Haddad188 satisfy this limitation?

A349 Yes. As RDX-0002C.140 illustrates, '764 patent, claim 17[a] is identical to '714 patent, limitation 1[a]. Haddad188 teaches or suggests '764 patent, claim 17[a] for the reasons discussed for '714 patent (Ground 6), limitation 1[a].

2. Limitation 17[b]

Q350 Limitation 17[b] is *a backside light trapping material substantially covering the backside surface*. Does Haddad188 satisfy this limitation?

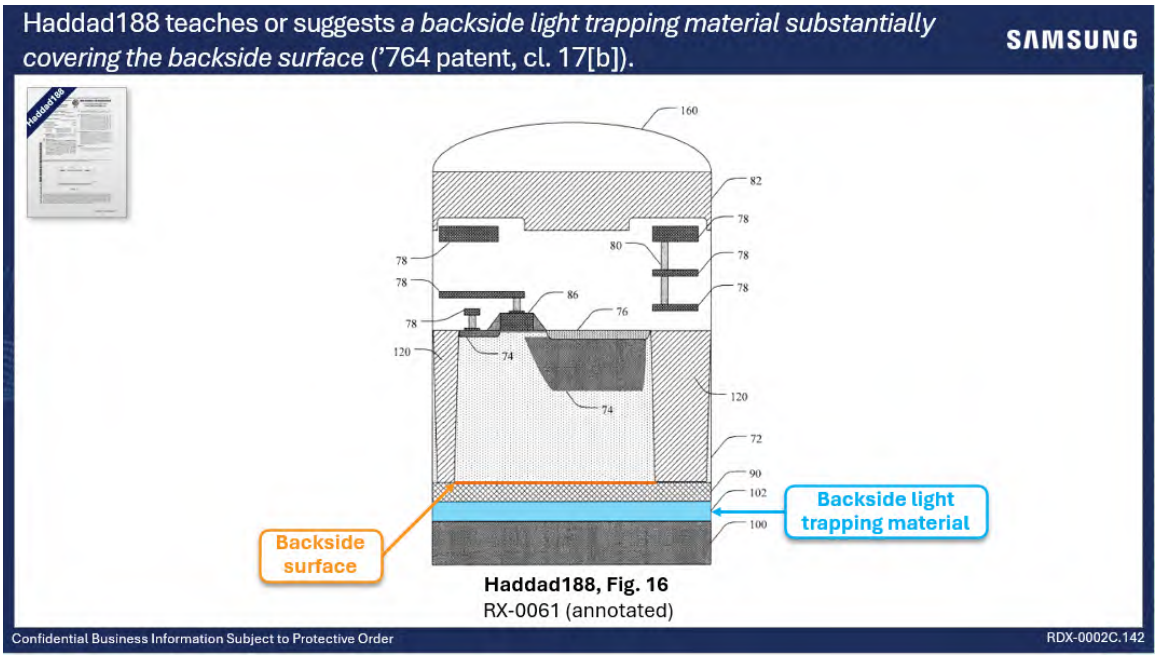
A350 Yes. As RDX-0002C.141 illustrates, with differences shown in red, '764 patent, claim 17[b] is identical to '714 patent, limitation 1[b], except that '764 patent claim 17[b] requires that the backside light trapping material *substantially* covers the backside surface, as opposed to '714 patent, limitation 1[b]'s requirement that it only *at least partially* covers the backside surface.

As discussed for '714 patent (Ground 6), limitation 1[b], Haddad188 teaches or suggests *a backside light trapping material at least partially covering the backside surface*. Haddad188 further teaches or suggests *a backside light trapping material substantially covering the backside surface*. Dr. Mansoorian has not disputed this.

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Q351 How does Haddad188's *backside light trapping material substantially cover[] the backside surface*?

A351 As RDX-0002C.142 illustrates, Haddad188's *backside light trapping material* (reflecting layer 102) covers the entire backside surface, and therefore *substantially cover[s]* it as well. POSITAs would expect that reflecting layer 102 covers the backside surface in both directions, consistent with its role in reflecting incident electromagnetic radiation that passes through the semiconductor substrate. *See* Haddad188, 25:6-9, 23:19-22.



3. Limitation 17[c]

Q352 Limitation 17[c] is *a peripheral light trapping material substantially covering the peripheral sidewall*. Does Haddad188 satisfy this limitation?

A352 Yes. As RDX-0002C.143 illustrates, '764 patent, claim 17[c] is identical to '714 patent, limitation 1[c]. Haddad188 teaches or suggests '764 patent, claim 17[c] for the reasons discussed for '714 patent (Ground 6), limitation 1[c].

4. Limitation 17[d]

Q353 Limitation 17[d] is *wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface*. Does Haddad188 satisfy this limitation?

A353 Yes. As RDX-0002C.144 illustrates, '764 patent, claim 17[d] is identical to '714 patent, claim 18's additional limitations. Haddad188 teaches or suggests '764 patent, claim 17[d] for the reasons discussed for '714 patent (Ground 6), claim 18.

5. Limitation 17[e]

Q354 Limitation 17[e] is *wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel*. Does Haddad188 satisfy this limitation?

A354 Yes. As RDX-0002C.145 illustrates, '764 patent, claim 17[e] is identical to '714 patent, limitation 1[d]. Haddad188 teaches or suggests '764 patent, claim 17[e] for the reasons discussed for '714 patent (Ground 6), limitation 1[d].

b. Claim 18

Q355 Let's turn to claim 18, which is *[t]he device of claim 1, wherein the peripheral sidewall extends completely around the pixel periphery*. Have you formed an opinion regarding this claims?

A355 As explained regarding the Terms Remaining in Dispute, I understand that Samsung proposed the limitation *extends completely around the pixel periphery* is indefinite, and that SiOnyx proposed it means surrounding the pixel.

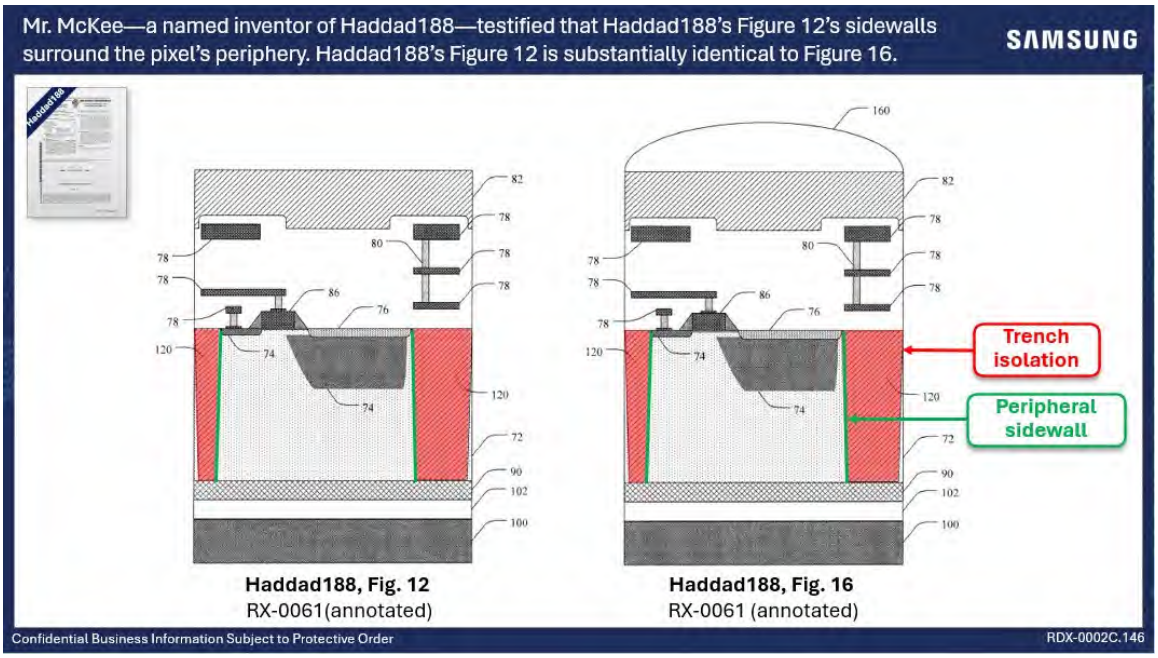
It is unclear how the peripheral sidewall can be simultaneously both disposed into and around the pixel. However, in view of Dr. Foty's interpretation and application of these limitations in his infringement and technical DI opinions where this limitation is allegedly satisfied because the peripheral sidewall defines the bounds of the pixel, and to the extent this term is not indefinite, Haddad188 teaches or suggests this claim.

Q356 How does Haddad188 teach or suggest these claims?

A356 As discussed for '714 patent (Ground 6), limitation 1[a], Haddad188, like the Light Trapping Patents, does not include a plan view showing the extent to which trench isolation 120 surrounds the pixel. However, Haddad188 explains that trench isolation 120 is used to "maintain pixel to pixel uniformity by reducing optical and electrical crosstalk," i.e., to ensure that light and charge cannot move from one pixel to the next. Haddad188, 22:23-24. POSITAs would have understood that increased coverage results in decreased optical and electrical crosstalk. Moreover, Haddad188 explains that its invention can include "a semiconducting photosensitive imager [that] can be a three or four transistor active pixel sensor (3T APS or 4T APS)." Haddad188, 8:27-28. POSITAs would have understood that such APS devices are associated with row and column addressing which is only used in a two-dimensional pixel array. In such arrays, having the trench isolation extend *completely* around the pixel periphery to optically and electrically isolate the pixels from one another would have been obvious, as Haddad188 explains.

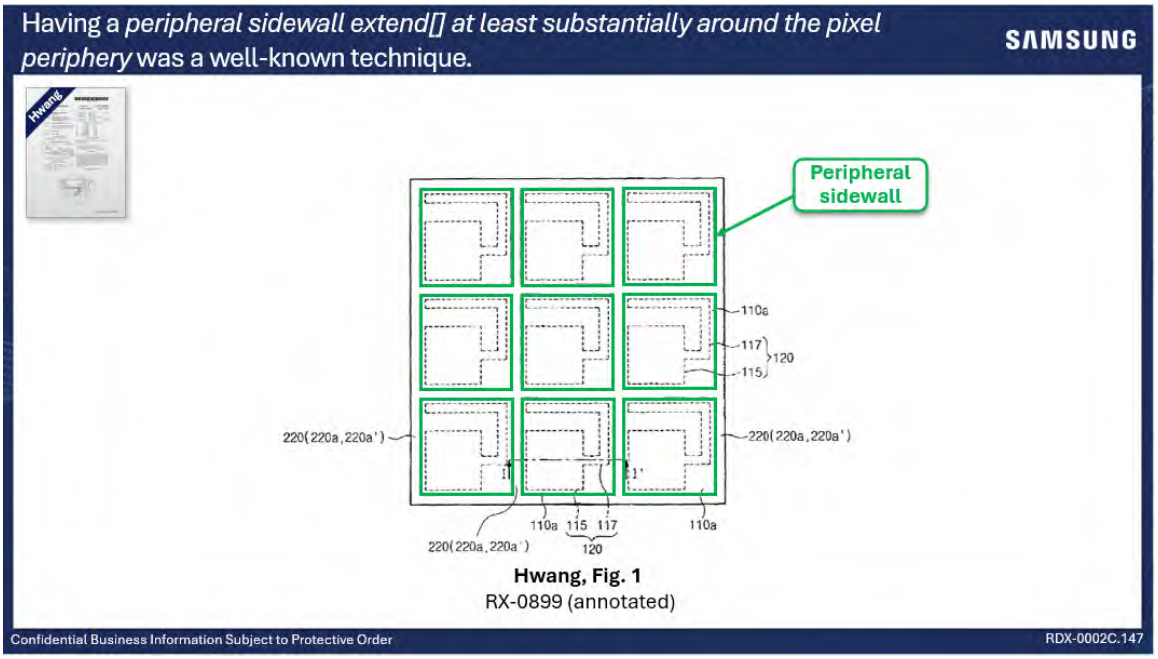
Indeed, Mr. McKee—a named inventor of Haddad188—admitted that Haddad188's trench isolation as depicted in Figure 12—which, as RDX-0002C.146 illustrates, has substantially similar deep trench isolation to Figure 16, even sharing the same identifier 120—would surround the pixel's periphery by going all the way around it in order to isolate the pixel. JX-0027C (McKee), 110:7-115:22.

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Q357 Are there any other reasons why you think Haddad188 teaches or suggests a *peripheral sidewall* that *extends completely around the pixel periphery*?

A357 Yes. Having peripheral sidewalls extend completely—which encompasses *at least substantially—around the pixel periphery* was a well-known technique used in similar devices. For example, as previously discussed, Hwang discloses an image sensor with a *peripheral sidewall extending completely around the pixel periphery*, as RDX-0002C.147 illustrates. *See also* Hwang, 6:15-17 ("sidewall multi-layered reflection layer 220 encloses the side walls of the pixel semiconductor patterns 110*a*").



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Likewise, as previously discussed, Yamada similarly discloses that each of its embodiments are "configured such that the entire side surfaces of the PIN photodiode 7 is covered by the third reflective films 11." Yamada, [0056]. Consistent with Haddad188's teachings, Yamada discloses that "the PIN photodiode 7 is surrounded by … third reflective films 11, so when light is incident to the PIN photodiode 7, that light is reflected by … third reflective films 11 so as to be confined within the PIN photodiode 7." Yamada, [0036]. *See also* Roy, Fig. 3; RX-0896 (Roy283), 5:53-54 ("each photosite is completely surrounded by trenches").

c. Claim 20

Q358 Let's turn to claim 20, which is *[t]he device of claim 17, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer*. Does Haddad188 satisfy this claim?

A358 Yes. As RDX-0002C.148 illustrates, '764 patent, claim 20's additional limitations are identical to '714 patent, claim 17's additional limitations. Haddad188 teaches or suggests '764 patent, claim 20's additional limitations for the reasons discussed for '714 patent (Ground 6), claim 17. Specifically, Haddad188's reflecting layer 102 (*backside light trapping material*) "can be any reflective material that can be incorporated into such a device," "includ[ing] … silver, aluminum, and the like," Haddad188, 23:15-26, i.e., a *metal layer*.

2. Ground 6: Haddad188 and Schubert Render Obvious Claims 8, 16-18, and 20

Q359 Let's turn to your Ground 6 opinions. Can you please summarize your Ground 6 opinions?

A359 In my opinion Haddad188 and Schubert render obvious claims 8, 16-18, and 20. As explained for Ground 5, Haddad188 anticipates, or at least renders obvious, claims 17-18, and 20. Those opinions are equally applicable to my Ground 6 opinions regarding Haddad188 and Schubert, which further render obvious claims 8 and 16.

a. Claim 8

Q360 Let's turn to claim 8. Have you formed an opinion regarding claim 8?

A360 Yes. Haddad188 and Schubert render obvious claim 8. As RDX-0002C.150 illustrates, limitations 8[a]-[c], and 8[f] are identical to limitations 17[a]-[c] and 17[e]. Haddad188 teaches or suggests these limitations for the reasons discussed for '764 patent (Ground 5), claim 17. The only limitations not identical to claim 17 is limitations 8[d]-[e].

1. Limitations 8[d]-[e]

Q361 Limitations 8[d]-[e] are *wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared*

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***to the two second materials*, (8[d]), and *wherein the difference in refractive index between the first material and the two second materials is at least 0.2* (8[e]). Have you formed an opinion regarding these limitations?**

A361 Yes. Dr. Foty has relied upon bulk refractive index values in his infringement and technical DI opinions. *E.g.*, RX-0905C, ¶¶435-452. Under such an interpretation and application Haddad188 in view of Schubert renders these limitations obvious.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *a first material sandwiched between two second materials*. Haddad in view of Schubert renders these limitations obvious under either construction.

Q362 How does Haddad188 in view of Schubert render these limitations obvious?

A362 Haddad188, as modified by Schubert, renders obvious this limitation under Dr. Foty's interpretation and application of this limitation. As discussed for '714 patent (Ground 6), limitation 1[e], it would have been obvious to modify Haddad188 in view of Schubert to use alternating layers of silicon and SiO_2 as the *peripheral light trapping material* in Haddad188. Accordingly, Haddad188, as modified by Schubert, has a *peripheral light trapping material* that *includes a first material* (i.e., silicon, which Schubert discloses as having a refractive index of 3.51) *sandwiched between two second materials* (i.e., SiO_2, which Schubert discloses as having a refractive index of 1.46), *wherein the first material has a higher refractive index* (i.e., 3.51) *as compared to the two second materials* (i.e., 1.46), *and wherein the difference in refractive index between the first material and the two second materials is at least 0.2* (i.e., a difference of 3.51–1.46=2.05). In any event, it would have been obvious to manufacture the device such that the silicon and SiO_2 layers have refractive indices that are at least 0.2 different from each other given the values described.

Q363 How does Haddad188's disclosures, as modified by Schubert, satisfy the parties' proposed constructions for the disputed terms in these limitations?

A363 As discussed for '714 patent (Ground 6), limitation 1[e], Haddad188's structure, as modified by Schubert, meets these limitations, including under either party's construction, as the *first material* is in contact with (and in between) the *two second materials* on two opposing sides.

b. Claim 16

Q364 Let's turn to claim 16, which is *[t]he device of claim 8, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer*. Does Haddad188 satisfy this claim?

A364 Yes. As RDX-0002C.151 illustrates, '764, claim 20's additional limitations are identical to '764 claim 16's additional limitations, as well as '714 patent, claim 17's additional limitations. Haddad188 teaches or suggests claim 20 for the reasons discussed for '764 patent (Ground 5), claim 16 as well as '714 patent (Ground 6), claim 17. Specifically, Haddad188's reflecting layer 102 (*backside light trapping material*) "can be any reflective

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material that can be incorporated into such a device," "includ[ing] … silver, aluminum, and the like," Haddad188, 23:15-26, i.e., a *metal layer*.

D. Suzunaga-based Grounds

Q365 Let's turn to your Suzunaga-based opinions. Can you please summarize your anticipation and obviousness opinions about the '764 patent based on Suzunaga?

A365 My Suzunaga-based opinions are based on a single ground, Ground 7, which is that Suzunaga anticipates, or at least renders obvious, claims 8 and 17-18.

1. Ground 7: Suzunaga Anticipates, or at Least Renders Obvious, Claims 8, and 17-18

a. Claim 8

1. Limitation 8[a]

Q366 Let's start with claim 8. Claim 8's first limitation, 8[a], is *at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery*. Does Suzunaga satisfy this limitation?

A366 Yes. As RDX-0002C.153 illustrates, '764 patent, limitation 8[a] is identical to '714 patent, limitation 1[a]. Suzunaga teaches or suggests '764 patent, limitation 8[a] for the reasons discussed for '714 patent (Ground 7), limitation 1[a].

2. Limitation 8[b]

Q367 Limitation 8[b] is *a backside light trapping material substantially covering the backside surface*. Does Suzunaga satisfy this limitation?

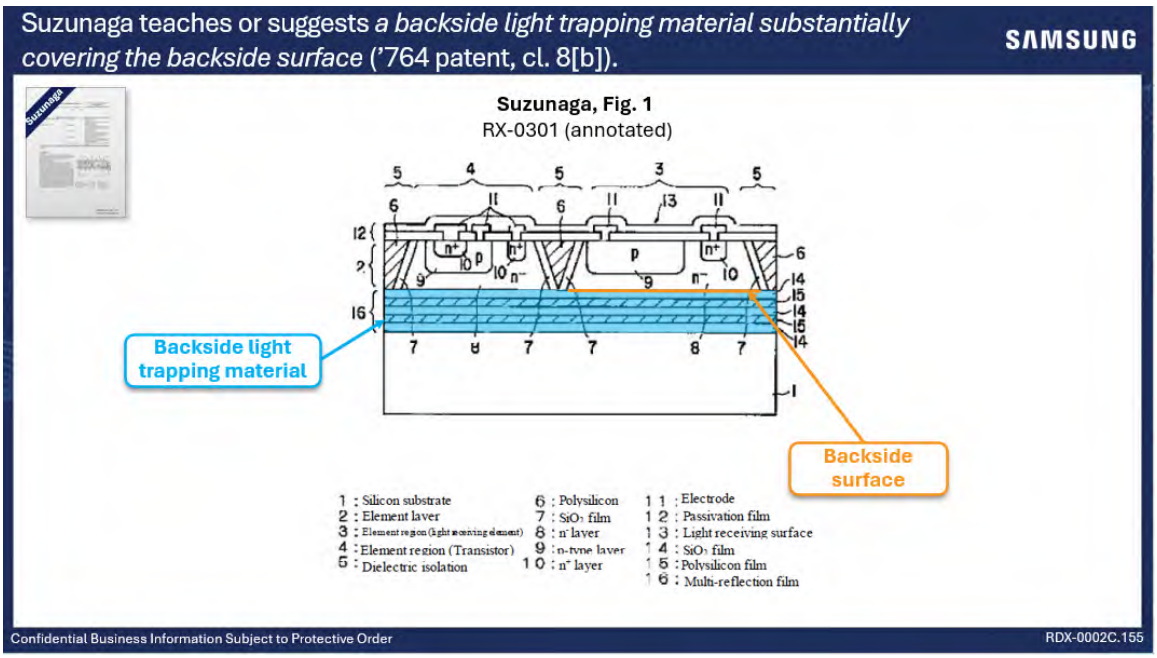
A367 Yes. As RDX-0002C.154 illustrates, with differences shown in red, '764 patent, limitation 8[b] is identical to '714 patent, limitation 1[b], except that '764 patent limitation 8[b] requires that the backside light trapping material *substantially* covers the backside surface, as opposed to '714 patent, limitation 1[b]'s requirement that it only *at least partially* covers the backside surface.

As discussed for '714 patent (Ground 7), limitation 1[b], Suzunaga teaches or suggests *a backside light trapping material <u>at least partially</u> covering the backside surface*. Suzunaga further teaches or suggests *a backside light trapping material <u>substantially</u> covering the backside surface*.

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Q368 How does Suzunaga's *backside light trapping material substantially cover[] the backside surface*?

A368 As RDX-0002C.155 illustrates, Suzunaga's *backside light trapping material* (multi-reflection film 16) covers the entire backside surface, and therefore *substantially cover[s]* it as well. POSITAs would expect that multi-reflection film 16 covers the backside surface in both directions, consistent with its role in "reflect[ing] the transmitted light transmitted through the semiconductor light receiving element formed on the element layer." Suzunaga, [0019]. *See also* Suzunaga, [0028] ("almost 100% of the incident light passing through the element layer 2 can be reflected by the multi-reflection film 16," back into the pixel).



3. Limitation 8[c]

Q369 Limitation 8[c] is *a peripheral light trapping material substantially covering the peripheral sidewall*. Does Suzunaga satisfy this limitation?

A369 Yes. As RDX-0002C.156 illustrates, '764 patent, limitation 8[c] is identical to '714 patent, limitation 1[c]. Suzunaga teaches or suggests '764 patent, limitation 8[c] for the reasons discussed for '714 patent (Ground 7), limitation 1[c].

4. Limitation 8[d]-[e]

Q370 Limitations 8[d]-[e] are *wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials*, (8[d]), and *wherein the difference in refractive index*

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between the first material and the two second materials is at least 0.2 **(8[e]). Does Suzunaga satisfy these limitations?**

A370 Yes. Suzunaga teaches or suggests this limitation.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *a first material sandwiched between two second materials*. Suzunaga satisfies this limitation under either construction.

Q371 How does Suzunaga satisfy this limitation?

A371 As discussed for '714 patent (Ground 7), limitation 1[e], both Suzunaga's *backside* and *peripheral light trapping material* (5 and 16) *and include a first material* (layers 15 and 6) are formed of polysilicon with a refractive index of 3.5, *sandwiched between two second materials* (layers 14 and 7) which are formed of silicon dioxide with a refractive index of 1.43~1.46, *see, e.g.*, Suzunaga, [0008], [0027], Fig. 1, Table 1, with a difference of approximately 2.07~2.04 (*at least 0.2*).

Q372 How does Suzunaga's disclosures satisfy the parties' proposed constructions for the disputed terms in these limitations?

A372 As discussed for '714 patent (Ground 1), limitation 1[e], Suzunaga's structure meets these limitations, including under either party's construction, as the *first material* is in contact with (and in between) the *two second materials* on two opposing sides.

5. Limitation 8[f]

Q373 Limitation 8[f] is *wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel*. Does Suzunaga satisfy this limitation?

A373 Yes. As RDX-0002C.157 illustrates, '764 patent, limitation 8[f] is identical to '714 patent, limitation 1[d]. Suzunaga teaches or suggests '764 patent, limitation 8[f] for the reasons discussed for '714 patent (Ground 7), limitation 1[d].

b. Claim 17

Q374 Let's turn to claim 17. Have you formed an opinion regarding claim 17?

A374 Yes. Suzunaga teaches or suggests claim 17. As RDX-0002C.158 illustrates, limitations 17[a]-[c] and 17[e] are identical to limitations 8[a]-[c] and 8[f]. Suzunaga teaches or suggests these limitations for the reasons discussed for '764 patent (Ground 7), claim 8. The only limitation not identical to claim 8 is limitation 17[d].

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1. Limitation 17[d]

Q375 Limitation 17[d] is *wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface*. Does Suzunaga satisfy this limitation?

A375 Yes. As RDX-0002C.159 illustrates, '764 patent, claim 17[d] is identical to '714 patent, claim 18's additional limitations. Suzunaga teaches or suggests '764 patent, claim 17[d] for the reasons discussed for '714 patent (Ground 7), claim 18.

c. Claim 18

Q376 Let's turn to claim 18, which is *[t]he device of claim 17 wherein the peripheral sidewall extends completely around the pixel periphery*. Have you formed an opinion regarding this claim?

A376 As explained regarding the Terms Remaining in Dispute, I understand that Samsung proposed the limitation *extends completely around the pixel periphery* is indefinite, and that SiOnyx proposed it means surrounding the pixel.

It is unclear how the peripheral sidewall can be simultaneously both disposed into and around the pixel. However, in view of Dr. Foty's interpretation and application of this limitation in his infringement and technical DI opinions where this limitation is allegedly satisfied because the peripheral sidewall defines the bounds of the pixel, and to the extent this term is not indefinite, Suzunaga teaches or suggests it.

Q377 How does Suzunaga teach or suggest claim 18?

A377 As discussed for '714 patent (Ground 7), limitation 1[a], Suzunaga, like the Light Trapping Patents, does not include a plan view showing the extent to which the dielectric isolation 5 surrounds the pixel. However, Suzunaga explains that the dielectric isolation 5 must "surround[]" the pixel to operate:

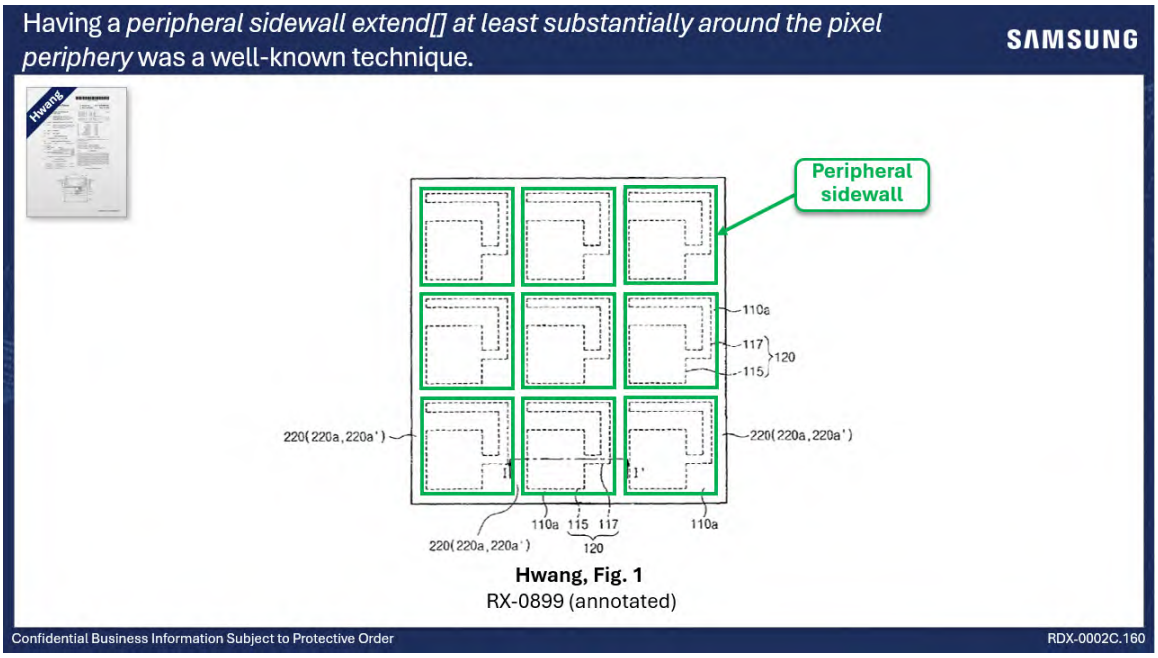
> Generally, p-n junction isolation, which is easy to form, is often used as an element isolation method for integrated circuits. However, in the case of an optical integrated circuit, if light is incident on the p-n junction for isolating elements, the reverse-biased p-n junction exhibits photoconductivity, and therefore cannot fulfill the role of isolating elements.
>
> Therefore, a dielectric isolation method, in which an element region on a silicon substrate is surrounded by an insulating film such as SiO_2, must be used in order to isolate elements in an optical integrated circuit.

Suzunaga, [0004]. This is expected, as POSITAs would understand that the *peripheral sidewall* should extend completely around the pixel to increase isolation. Therefore, it would have been at least obvious to POSITAs to make the trench isolation extend *completely* around the pixel periphery to "isolate" pixels in the optically integrated circuit.

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Q378 Are there any other reasons why you think Suzunaga teaches or suggests a *peripheral sidewall* that *extends completely around the pixel periphery*?

A378 Yes. Having peripheral sidewalls extend completely—which encompasses *at least substantially—around the pixel periphery* was a well-known technique used in similar devices. For example, as previously discussed, Hwang discloses an image sensor with a *peripheral sidewall extending* completely (i.e., *at least substantially*) *around the pixel periphery*, as RDX-0002C.160 illustrates. *See also* Hwang, 6:15-17 ("sidewall multi-layered reflection layer 220 encloses the side walls of the pixel semiconductor patterns 110*a*").

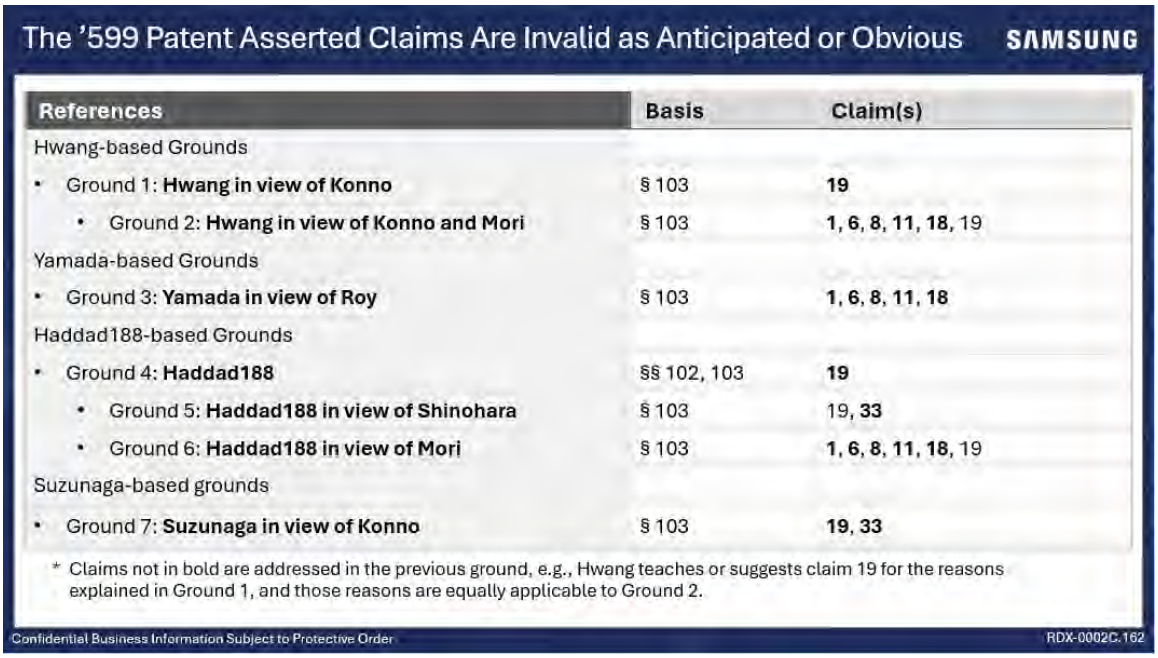


Likewise, as previously discussed, Yamada similarly discloses that each of its embodiments are "configured such that the entire side surfaces of the PIN photodiode 7 is covered by the third reflective films 11." Yamada, [0056]. Consistent with Suzunaga's teachings, Yamada discloses that "the PIN photodiode 7 is surrounded by … third reflective films 11, so when light is incident on the PIN photodiode 7, that light is reflected by … third reflective films 11 so as to be confined within PIN photodiode 7." Yamada, [0036]. *See also* Roy, Fig. 3; RX-0896 (Roy283), 5:53-54 ("each photosite is completely surrounded by trenches").

VII. '599 Patent Invalidity Based on Anticipation and Obviousness

Q379 Let's turn to the '599 patent. Can you summarize your opinions with respect to anticipation and obviousness of the '599 patent?

A379 Yes. As RDX-0002C.162 illustrates, in my opinion the '599 patent Asserted Claims are invalid based on four primary references: Hwang, Yamada, Haddad188, and Suzunaga.



A. Hwang-based Grounds

Q380 Let's start with your Hwang-based opinions. Can you please summarize your anticipation and obviousness opinions about the '599 patent based on Hwang?

A380 My Hwang-based opinions are divided into two grounds. Ground 1 is that Hwang and Konno render obvious claim 19. Ground 2 is that Hwang, Konno, and Mori render obvious claims 1, 6, 8, 11, and 18-19.

1. Ground 1: Hwang and Konno Render Obvious Claim 19

a. Claim 19

1. Limitation 19[a]

Q381 Let's start with your Ground 1 opinions that Hwang and Konno render obvious claim 19.

Claim 19's first limitation, 19[a], is *at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending at least partially around the pixel periphery*. Does Hwang satisfy this limitation?

A381 Yes. As RDX-0002C.164 illustrates, with differences shown in red, '599 patent, limitation 19[a] is identical to '714 patent, limitation 1[a], except that '599 patent, limitation 19[a] requires that the peripheral sidewall extend *at least partially* around the pixel periphery, whereas '714 patent, limitation 1[a] requires that the peripheral sidewall be *disposed into at least a portion of the pixel*, and extend *at least substantially* (as opposed to only *partially*) around the pixel periphery.

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As discussed for '714 patent (Ground 1), limitation 1[a], Hwang teaches or suggests a peripheral sidewall that extends *at least substantially around the pixel periphery*. Accordingly, Hwang teaches or suggests the more broad requirement that the peripheral sidewall extends only *at least partially around the pixel periphery* for the same reasons.

2. Limitations 19[b], [d]

Q382 Let's take limitations 19[b] and 19[d] together. 19[b] is *a backside light trapping material at least partially covering the backside surface*. 19[d] is *a textured region positioned to interact with light incident thereon to increase quantum efficiency of the device*. Have you formed an opinion regarding these limitations?

A382 Yes. Hwang and Konno render these limitations obvious.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *light trapping material* and *textured region*. Hwang and Konno render obvious a *backside light trapping material* and a *textured region*, including under either construction.

Q383 Let's start with 19[b], *a backside light trapping material at least partially covering the backside surface*. How do Hwang and Konno render this limitation obvious?

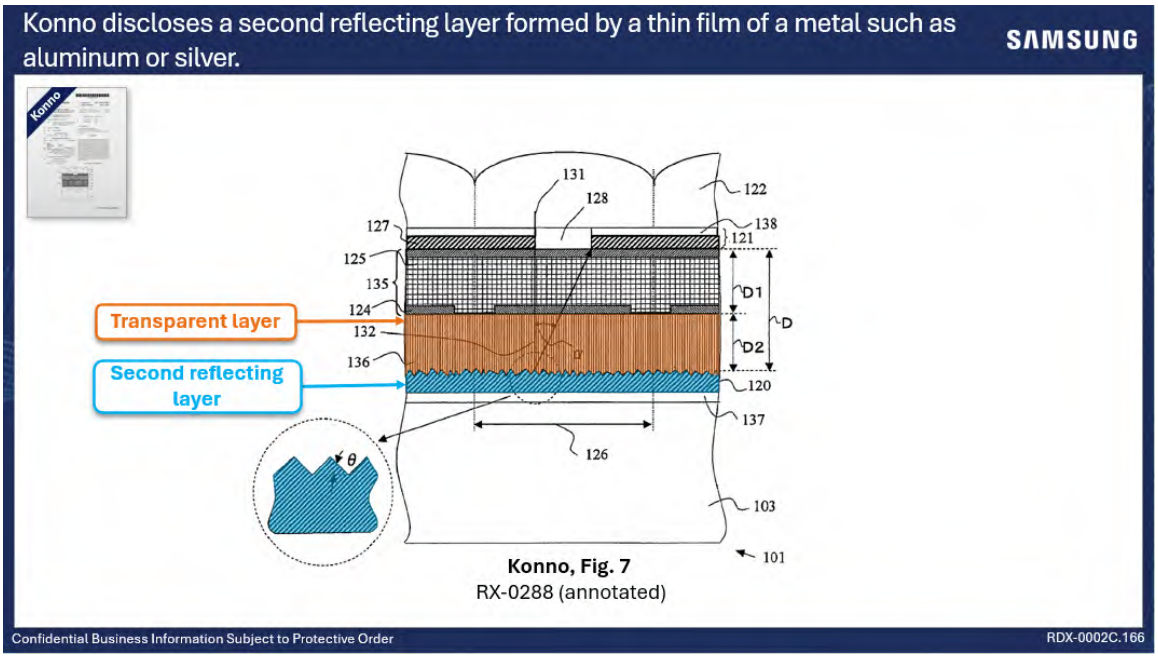
A383 As RDX-0002C.165 illustrates, '599 patent, limitation 19[b] is identical to '714 patent, limitation 1[b]. Hwang teaches or suggests '599 patent, limitation 19[b] for the reasons discussed for '714 patent (Ground 1), limitation 1[b]. Specifically, Hwang's base multi-layered reflection layer 155*a* constitutes *a backside light trapping material at least partially covering the backside surface*.

Additionally, POSITAs would be motivated to replace Hwang's base multi-layered reflection layer 155*a* with Konno's transparent layer 136 and second reflecting layer 120 to similarly cover Hwang's *backside surface*. Konno's transparent layer 136 and second reflecting layer 120, as used in Hwang, constitute a *backside light trapping material at least partially covering the backside surface* and *a textured region positioned to interact with light incident thereon to increase quantum efficiency of the device*.

Q384 Does Konno disclose *a backside light trapping material*?

A384 Yes. Konno's second reflecting layer 120 constitutes *a backside light trapping material*. As RDX-0002C.166 illustrates, Konno includes a second reflecting layer 120 "formed by forming a thin film of a metal such as aluminum or silver." Konno, 8:31-38. Such metal reflectors constitute a *light trapping material* that reflect light back into the pixel, as a solid metal film, as Konno discloses, reflects more light than it transmits, and is positioned to reflect light back into the pixel. *See* Schubert, Table 10.2 (listing reflectivity of metal-air and metal-semiconductor reflectors at 0.5μm and 1.0μm, all of which have 50% or greater reflectivity); Yamada, [0038] ("since the sides of the PIN photodiode 7 are covered with the third reflective films 11, no incident light escapes from the sides of the PIN photodiode 7 and no optical crosstalk occurs between neighboring PIN photodiodes 7"), [0012] ("[t]hird reflective films (11) composed of a metal [such as aluminum]").

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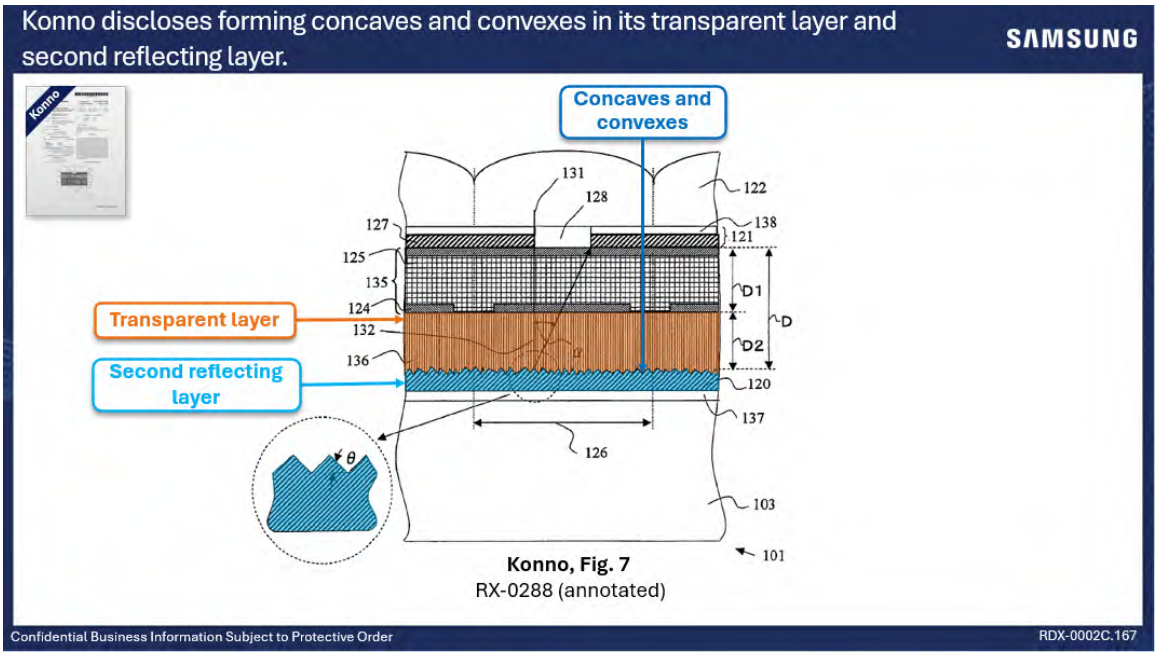


Q385 How does second reflecting layer 120 constitute a *light trapping material* under the parties' proposed constructions?

A385 Second reflecting layer 120 constitutes a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

Q386 Does Konno disclose *a textured region*?

A386 Yes. Konno's transparent layer 136 is textured by "forming concaves and convexes on [its] surface." Konno, 14:38-42. RDX-0002C.167 illustrates the textured features of transparent layer 136 alongside the complementary texturing of second reflecting layer 120.



Konno's transparent layer 136 constitutes a *textured region*. For example, the '599 patent states that "textured region 312 can have surface features configured to reflect and disperse light," '599 patent, 11:2-3, and that texturing may be created "across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch or a laser process to define a specific structure or pattern." '599 patent, 14:47-52.

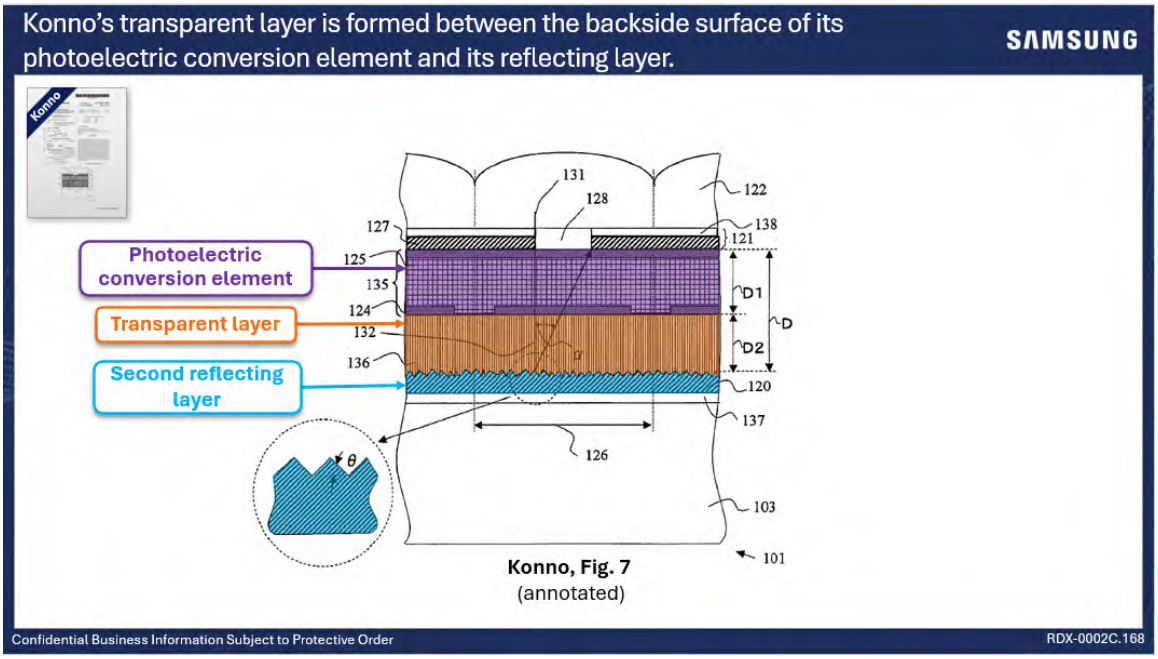
Like the '599 patent, Konno discloses that the concaves and convexes are formed "on the surface of the transparent layer 136 before producing the reflecting layer 120, and then depositing a metal thereon to produce the reflecting layer 120." Konno, 14:38-42. As in the '599 patent, Konno teaches that "[t]he concaves and convexes of the transparent layer 136 can be formed by a known technique such as sputtering and microlithography." Konno, 14:42-45. Konno further discloses that "by providing a transparent layer … convexes or concaves or a structure effective for reflecting or scattering photons can be realized in the reflecting layer adjacent to the transparent layer." Konno, 3:58-62. Konno teaches that transparent layer 136 "transmits photons" and "can provide concaves and convexes which realizes a large reflection angle." Konno, 4:54-58, 15:2-6. Konno also teaches that the textured region "makes it possible to reflect photons which entered from the light entrance window 128 to the first reflecting layer 121, and therefore the amount of photons to be detected again by the photoelectric conversion film can be increased." Konno, 13:66-14:3.

Q387 How does transparent layer 136 constitute a *textured region* under the parties' proposed constructions?

A387 Transparent layer 136 constitutes a *textured region* under the parties' proposed constructions, as it reflects or scatters photons, i.e., diffuses or redirects electromagnetic radiation, thus increasing the quantum efficiency of the device and the effective absorption length for the reasons just explained.

Q388 Is transparent layer 136 *positioned to interact with light incident thereon to increase quantum efficiency of the device?*

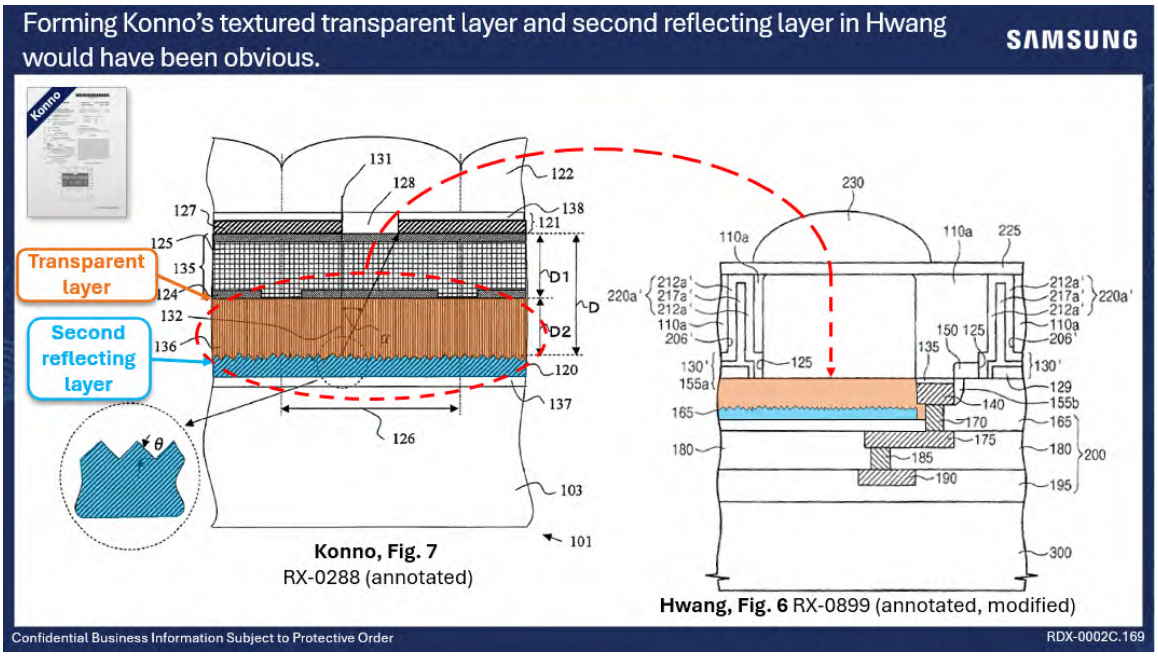
A388 Yes. Konno's transparent layer 136 is *positioned to interact with light incident thereon to increase quantum efficiency of the device*. As RDX-0002C.168 illustrates, Konno's transparent layer 136 is formed between the backside surface of its photoelectric conversion element 135 and its reflecting layer 120. *See also* Konno, 2:56-57 (describing "a structure where the first reflecting layer and the second reflecting layer sandwich the photoelectric conversion means together with the transparent layer").



Konno further teaches that transparent layer 136 "transmits photons" and "can provide concaves and convexes which realizes a large reflection angle." Konno, 4:54-58, 15:2-6. Konno also teaches that its texturing "makes it possible to reflect photons which entered from the light entrances window 128 to the first reflecting layer 121, and therefore the amount of photons to be detected again by the photoelectric conversion film 125 can be increased." Konno, 13:66-14:3. POSITAs would have understood that, by reflecting photons within the device to increase the amount of detected photons, Konno's textured region *increase[s]* the *quantum efficiency of the device*. *See* JX-0017C (Sickler), 108:4-109:19 (explaining that increasing the pathlength light travels within the pixel increases the pixel's quantum efficiency, as it provides more opportunities for the light to be absorbed).

Q389 Would implementing Konno's transparent layer 136 and second reflecting layer 120 in Hwang have been obvious?

A389 Yes. As RDX-0002C.169 illustrates, POSITAs would have been motivated to replace Hwang's base multi-layered reflection layer 155*a* with Konno's transparent layer 136 and second reflecting layer 120 to similarly cover Hwang's backside surface.



Q390 Why would POSITAs be motivated to make this combination?

A390 As discussed, Konno teaches that texturing transparent layer 136 "makes it possible to reflect photons which entered from the light entrance window 128 to the first reflecting layer 121, and therefore the amount of photons to be detected again by the photoelectric conversion film 125 can be increased." Konno, 13:66-14:3. Likewise, Hwang similarly discloses a benefit of configuring its device such that light reflects off the backside reflecting material also reflects off peripheral reflecting material in order to increase the light's path and maximize the pixel's absorption efficiency. *See* Hwang, 10:28-35 ("[l]ight that is reflected from the first and second boundary surfaces," i.e., light that reflects off base multi-layered reflection layer 155*a*, "is also reflected by the third boundary surface and also the fourth boundary surface within the sidewall multi-layered reflection layer 220 [(220*a*' in Figure 6)]" and that, as a result, "the absorption efficiency of external light is increased"); *see also* Hwang, 8:61-9:14. POSITAs would therefore have been motivated to implement Konno's textured surfaces in Hwang to achieve this shared goal.

Q391 Are there any other reasons why POSITAs would have been motivated to make this modification?

A391 Yes. Konno further teaches that:

> [W]hen the reflecting layers 120 and 121 consist of metals, it is also possible to electrically connect at least one of these to ground or electrode potential of a read-out circuit, a control circuit, a power supply or the like.
>
> By using such a [metal] structure, error signals and noises generated in output signals of the photo-detector 101 by external noises which flow in from the outside and flow into the photo-detector 101 and detected in the

photoelectric conversion element 135, wiring or the like can be thereby reduced.

Konno, 12:29-38. Accordingly, POSITAs would have been motivated to alter Hwang to incorporate Konno's transparent layer 136 and second reflecting layer 120 to reduce error signals and noises generated in output signals as Konno teaches—which Hwang's multilayer dielectric reflector would not have provided—as well as achieve this mutually-recognized benefit of increasing the amount of light reflected back into the pixel.

Q392 Would POSITAs have reasonably expected success in making this modification?

A392 Yes. POSITAs would have reasonably expected success in replacing Hwang's base multi-layered reflection layer 155*a* with Konno's textured transparent layer 136 and second reflecting layer 120. For example, Konno's textured transparent layer 136 and second reflecting layer 120 could be implemented in Hwang between the manufacturing steps occurring immediately after what is shown in Figure 22, or in between the manufacturing steps shown in Hwang's substantially similar embodiment depicted in Figures 8/9.

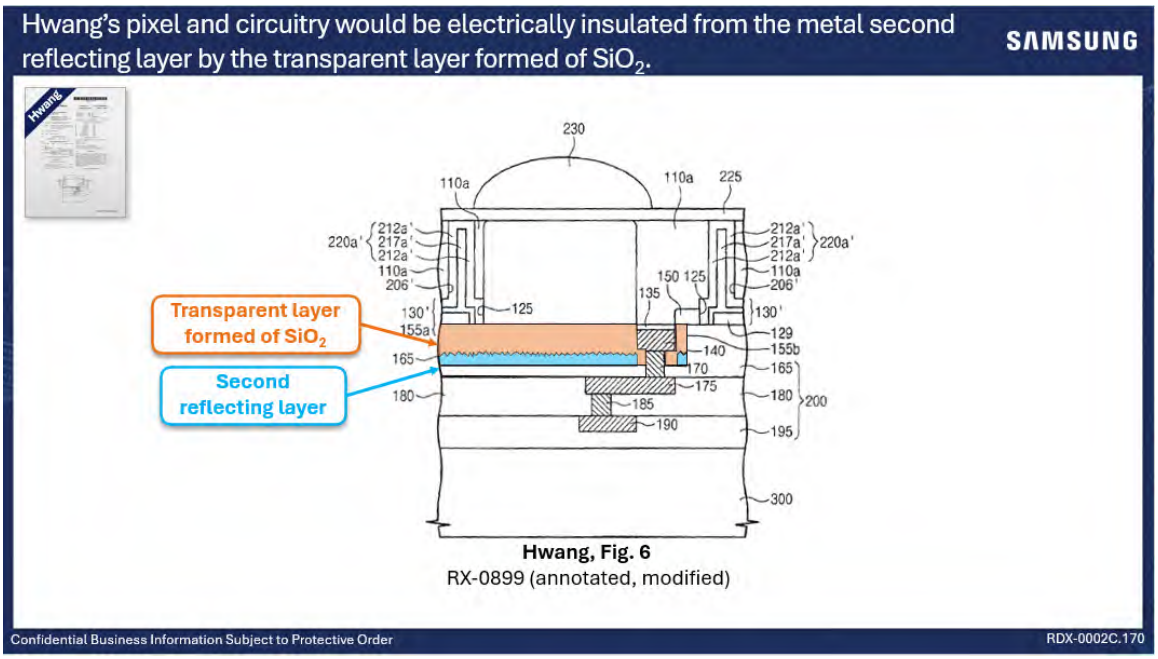
Additionally, Konno's transparent layer 136 is "formed from a material which transmits photons, for example, glass." Konno, 9:35-41. Hwang already uses layers of SiO_2—i.e., glass—on its backside surface. *See* Hwang, 8:40-52 ("base multi-layered reflection layer 155*a* can include a first base multi-layered reflection layer 151"), 9:25-30 ("first base multi-layered reflection layer[] 151" is "formed of silicon [di]oxide"). POSITAs would have understood that texturing Hwang's SiO_2 layer using Konno's methods requires nothing more than the use of a known technique to obtain predictable results.

Q393 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this modification, as it would create an electrical connection between the device circuitry and reflector layer?

A393 Yes. While not advanced by Dr. Mansoorian for this combination, Dr. Mansoorian opined elsewhere that "[r]eplacing base multi-layered reflection layer 155[*a*] with a metal reflector as disclosed in Konno would [] create an electrical connection between the device circuitry and the reflector layer." RX-0911C, ¶191. I disagree.

As explained, as part of this combination Konno's transparent layer 136 "formed from … glass," Konno 9:35-41, i.e., SiO_2 would be placed between the metal backside reflector and Hwang's pixel and device circuitry, as RDX-0002C.170 illustrates. POSITAs would recognize that SiO_2 is a dielectric material commonly used to isolate electrical elements in devices like Hwang and Konno, and would reasonably expect success that it would serve as an electrical insulator in such a modification. *E.g.*, Hwang, 12:30-31 ("insulating material, such as oxide material"). Indeed, Dr. Mansoorian admits that "insulation may be a secondary effect" of adding the SiO_2 "transparent layer 136." RX-0911C, ¶¶192-193. Even if "it is not designed for insulation," as Dr. Mansoorian asserts, POSITAs would still understand a layer of SiO_2 would act as an insulator.

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Q394 Are you aware of SiOnyx's argument that POSITAs would not make this modification, as texturing would cause dark current?

A394 Yes. While not advanced by Dr. Mansoorian, SiOnyx contended that POSTIAs would make this combination, as "incorporating a textured surface would increase the amount of dark current, which increases noise and reduces the performance of the pixels." RX-0606C.156 (SiOnyx Validity Contentions). I disagree. In this combination, the texturing (concaves and convexes) has no impact on the surface of Hwang's pixel, so POSITAs would not expect there to be increased dark current. Indeed, Konno teaches that, by texturing transparent layer 136 as opposed to the pixel itself, dark current can be prevented. Konno, 15:6-22. Furthermore, POSITAs would recognize that any dark current potentially stemming from such texturing could be readily reduced. *See* JX-0017C (Sickler), 43:19-44:2.

Q395 Are you aware of Dr. Mansoorian's argument that POSITAs would not be motivated to modify Hwang based on Konno because Konno is non-analogous art?

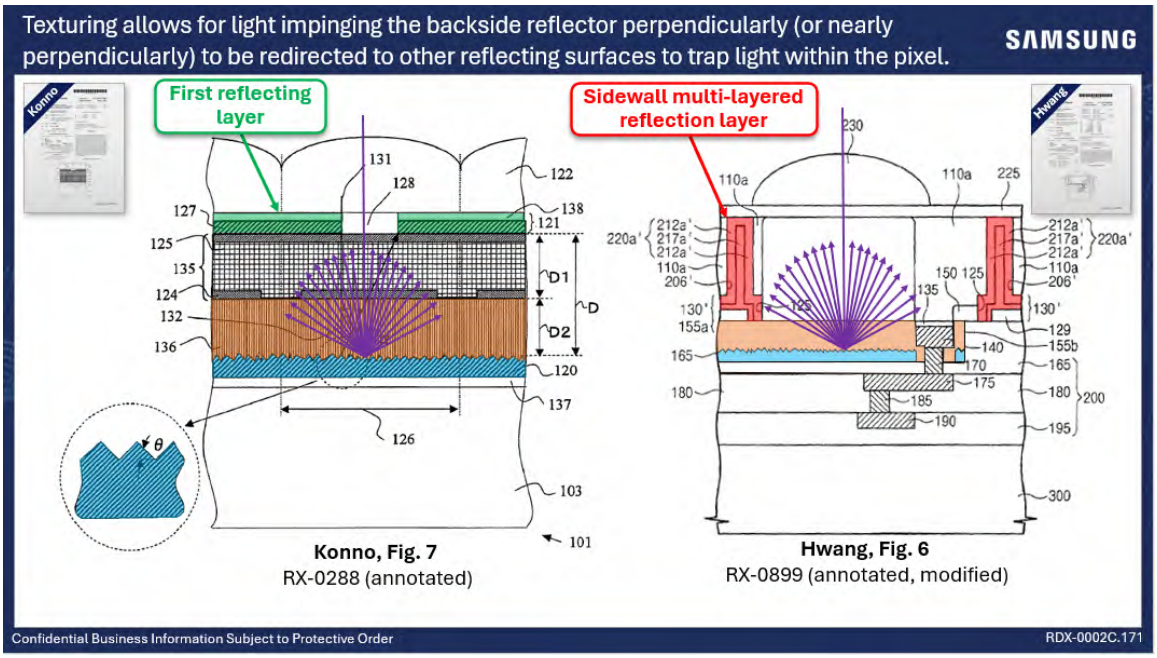
A395 Yes. While not advanced for this combination, Dr. Mansoorian opines elsewhere that POSITAs would not combine Hwang and Konno because "Hwang discloses a device for use in generating picture-quality images, i.e., a camera," and "Konno, on the other hand, is optimized for use in a 'personal authentication system.'" RX-0911C, ¶181. I disagree. As I explained in the Overview of Konno, Konno is not limited to personal authentication systems, but is instead directed to solid-state imaging elements, including an "image sensor … and digital camera," just like Hwang. Konno, 1:15-22.

Q396 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination without also adding Konno's first reflecting layer 121 and window 128?

A396 Yes. Dr. Mansoorian opines that POSITAs "would have understood the 'transparent layer 136' and the 'first reflecting layer 121' with 'window 128' to be inextricably linked," such that POSITAs would not incorporate Konno's teaching of a textured region without also adding Konno's frontside reflectors. RX-0911C, ¶373. I disagree and note this theory was not presented in SiOnyx's contentions. RX-0606C.155-156.

Q397 Why do you disagree?

A397 POSITAs would understand that the benefits Konno describes due to texturing, namely, reflecting light "with a large amount of horizontal components," i.e., "with a large reflection angle," thus making "it possible to reflect photons which entered from the light entrance window 128 to the first reflecting layer 121," to increase absorption. Konno, 13:63-14:3. That is, Konno teaches that texturing allows for light impinging the backside reflector perpendicularly (or nearly perpendicularly) can be redirected to other reflecting surfaces to trap it within the pixel. Such texturing would likewise be effective in Hwang, as it would cause light impinging Hwang's backside reflector perpendicularly (or nearly perpendicularly) to be scattered to Hwang's sidewall multi-layered reflection layer 220*a*' to trap light within Hwang's pixel, as RDX-0002C.171 illustrates.



Q398 Are there any other reasons why you disagree with Dr. Mansoorian's argument?

A398 Yes. As discussed, POSITAs would likewise understand that the thickness of transparent layer 136 and the depth of sidewall multi-layered reflection layer 220*a*' could be adjusted to increase Hwang's overall sensitivity, e.g., having sidewall multi-layered reflection layer 220*a*' extend to Hwang's backside reflector to prevent crosstalk. Additionally, transparent

layer 136 only needs to be slightly thicker than the depth of the concaves and convexes. *See* Konno, 15:6-16.

Finally, even if Konno's first reflecting layer 121 and window 128 were required for this combination, as Dr. Mansoorian incorrectly asserts, POSITAs would still be motivated to make this combination. As explained for '714 patent (Ground 3), claim 12, incorporating Konno's first reflecting layer 121 and window 128 in Hwang's device would have been obvious.

Q399 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination as it would increase crosstalk between Hwang's pixels?

A399 Yes. Dr. Mansoorian opines that the including Konno's transparent layer 136 in Hwang would create crosstalk, as he argues that any added transparent layer must "be at least as thick as the photodiode 145 of Hwang." RX-0911C, ¶¶374-381. I disagree and not this theory was not presented in SiOnyx's contentions. RX-0606C.155-156.

As explained, POSITAs would understand that transparent layer 136 only needs to be slightly thicker than the depth of the concaves and convexes, which POSITAs would understand could be quite small. *See* Konno, 15:6-16. While Konno discusses using a thicker transparent layer to minimize the angle of light which can escape through its window 128, POSITAs would recognize that transparent layer 136's thickness is a design choice and that in certain instances a thinner transparent layer 136 is preferable if they were trying to minimize the device's size as opposed to maximizing the amount of light absorbed. This is particularly true when transparent layer 136 is textured, as texturing will reflect light "with a large amount of horizontal components," i.e., "with a large reflection angle," Konno, 13:63-14:3, such that the amount of light being reflected at the angle which would cause to escape through the pixel's light incident surface (e.g., through the aperture) would decrease.

3. Limitation 19[c]

Q400 Limitation 19[c] is *a peripheral light trapping material substantially covering the peripheral sidewall*. Does Hwang satisfy this limitation?

A400 Yes. As RDX-0002C.172 illustrates, '599 patent, limitation 19[c] is identical to '714 patent, limitation 1[c]. Hwang teaches or suggests '599 patent, limitation 19[c] for the reasons discussed for '714 patent (Ground 1), limitation 1[c].

4. Limitation 19[e]

Q401 Limitation 19[e] is *a reflective layer coupled to the light incident side and having an aperture to allow entry of light into the pixel*. Have you formed an opinion regarding this limitation?

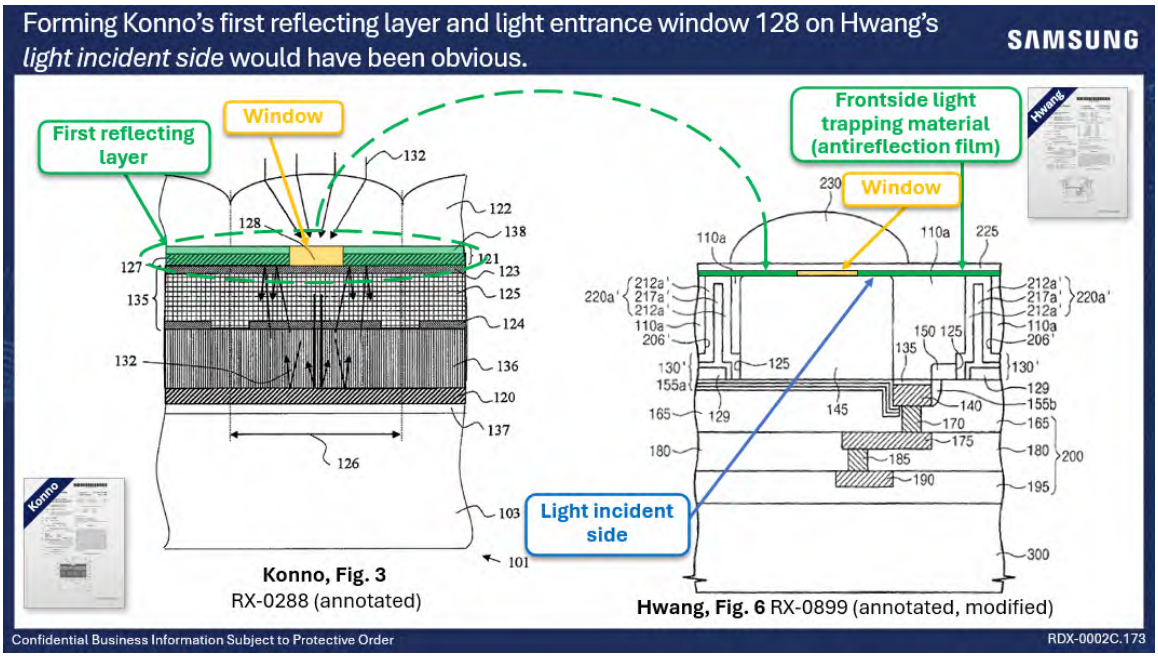
A401 Yes. Hwang and Konno render obvious *a reflective layer coupled to the light incident side and having an aperture to allow entry of light into the pixel*.

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As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *reflective layer*. Hwang, as modified by Konno, includes a *reflective layer coupled to the light incident side* under either construction.

Q402 How do Hwang and Konno render this limitation obvious?

A402 As explained for '714 patent (Ground 3), claim 12, it would have been obvious to implement Konno's reflecting layer 121, and corresponding light entrance window 128, in Hwang, as RDX-0002C.173 illustrates.



Q403 Would this combination satisfy limitation 19[f]?

A403 Yes. As RDX-0002C.173 illustrates, this modification results in Hwang having a *reflective layer* (first reflective layer 121) *coupled to the light incident side* (Hwang's "second surface" at the top of pixel semiconductor pattern 110*a*) *and having an aperture* (window 128) *to allow entry of light into the pixel*. Konno, 8:35-43. A solid metal film, as Konno teaches, reflects more light than it transmits. *See* Schubert, Table 10.2 (listing reflectivity of metal-air and metal-semiconductor reflectors at 0.5µm and 1.0µm, all of which have 50% or greater reflectivity).

Q404 How does reflective layer 121 constitute a *reflective layer* under the parties' proposed constructions?

A404 Reflecting layer 121 constitutes a *reflective layer* under either party's proposed construction, as it is a layer that reflects and will reflect more light back into the pixel than it transmits for the reasons just explained.

5. Limitation 19[f]

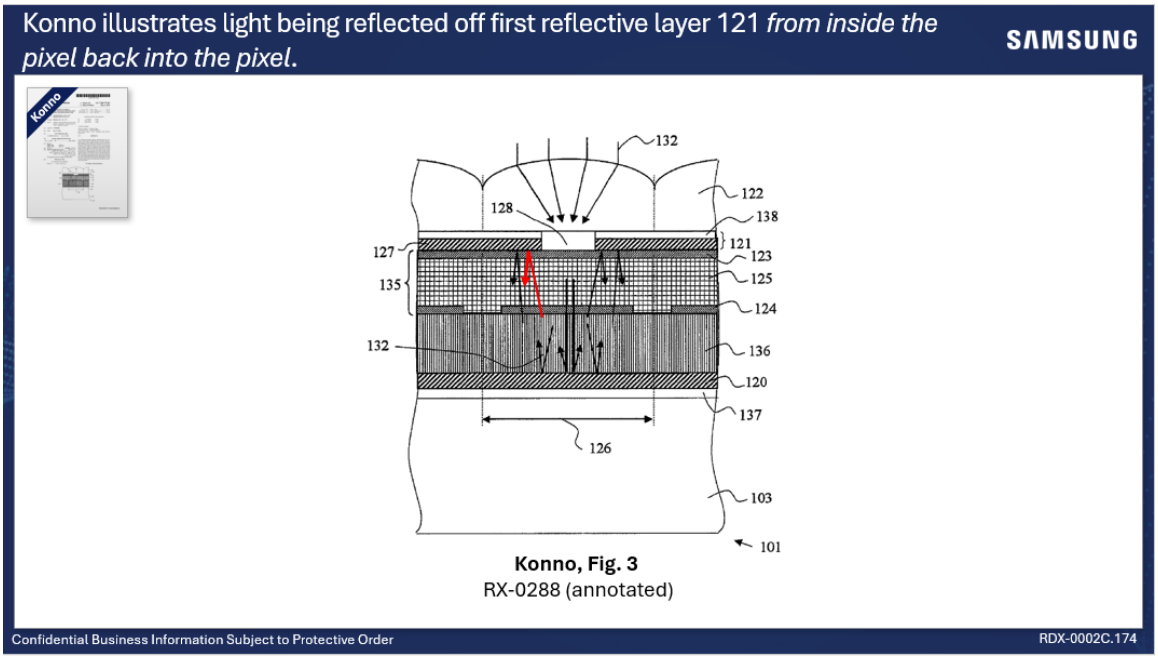
Q405 Limitation 19[f] is *wherein the reflective layer is operable to reflect at least a portion of light impinging thereupon from inside the pixel back into the pixel back into the pixel.* Have you formed an opinion regarding this limitation?

A405 Yes. Hwang and Konno render this limitation obvious. I understand that the ALJ amended *thereupon from inside the pixel back into the pixel back into the pixel* such that it now reads "thereupon from inside the pixel back into the pixel." Order No. 36 at 40.

Q406 How does Hwang, as modified by Konno, satisfy limitation 19[f]?

A406 As discussed for '599 (Ground 1), limitation 19[e], using Konno's first reflective layer 121 (*reflective layer coupled to the light incident side*) in Hwang would have been obvious. In such a structure, first reflective layer 121 constitutes a reflective layer that *is operable to reflect at least a portion of light impinging thereupon from inside the pixel back into the pixel*. As discussed for '714 patent (Ground 1), limitation 1[c] and '599 patent (Ground 1), claims 19[b], [d], Hwang, as modified by Konno, also includes a backside reflective layer (second reflecting layer 120) and a sidewall reflective layer (multi-layered reflecting layer 220*a*'), and the purpose of these backside and peripheral reflecting layers is to reflect light back into Hwang's pixel.

POSITAs would understand that Hwang—containing reflective peripheral, backside, and (as modified by Konno) frontside surfaces—is operable to reflect at least a portion of light off first reflective layer 121, i.e., to reflect light *from inside the pixel back into the pixel*. Indeed, as RDX-0002C.174 illustrates, Konno illustrates a light ray being reflected off first reflective layer 121 *from inside the pixel back into the pixel*.



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See also Yamada, Fig. 7 (illustrating a light ray being reflected by first reflective film 3, second reflective film 8, and third reflective film 11).

2. Ground 2: Hwang, Konno, and Mori Render Obvious Claims 1, 6, 8, 11, and 18-19

Q407 Let's turn to your Ground 2 opinions. Can you please summarize your Ground 2 opinions?

A407 In my opinion Hwang, Konno, and Mori render obvious claims 1, 6, 8, 11, 18, and 19. As explained for Ground 1, Hwang and Konno render obvious claim 19. Those opinions are equally applicable to my Ground 2 opinions regarding Hwang, Konno, and Mori, which further render obvious claims 1, 6, 8, 11, and 18.

a. Claim 1

Q408 Let's turn to claim 1. Have you formed an opinion regarding claim 1?

A408 Yes. Hwang, Konno, and Mori render obvious claim 1. As RDX-0002C.176 illustrates, limitations 1[a]-[b] and 1[d]-[e] are identical to limitations 19[a]-[b] and 19[e]-[f]. Hwang and Konno render obvious these limitations for the reasons discussed for '599 patent (Ground 1), claim 19. The only limitation not identical to claim 19 is limitation 1[c], however, I also have a separate opinion for limitation 1[b] for this Ground as well.

1. Limitation 1[b]

Q409 Let's start with limitation 1[b], which is *a backside light trapping material at least partially covering the backside surface*. What is your opinion regarding this limitation?

A409 Hwang teaches or suggests this limitation. As RDX-0002C.177 illustrates, '599 patent, limitation 1[b] is identical to '714 patent, limitation 1[b]. Hwang teaches or suggests '599 patent, limitation 1[b] for the reasons discussed for '714 patent (Ground 1), limitation 1[b].

Additionally, this limitation would have been obvious based on Hwang and Konno, for the reasons discussed for '599 patent (Ground 1), claims 19[b] and [d].

2. Limitation 1[c]

Q410 Limitation 1[c] is *a peripheral light trapping material substantially covering the peripheral sidewall, wherein said peripheral light trapping material is doped with a dopant to create a surface field*. Have you formed an opinion regarding this limitation?

A410 Yes. As part of his infringement opinions, Dr. Foty has opined that this limitation is met so long as at least part of the *peripheral light trapping material is doped*. RX-0905C, ¶¶1089-1095. This limitation is satisfied by Hwang and Mori under such an interpretation.

As RDX-0002C.178 illustrates, with differences shown in red, '599 patent, limitation 1[c] is identical to '714 patent, limitation 1[c], except that '599 patent, limitation 1[c]

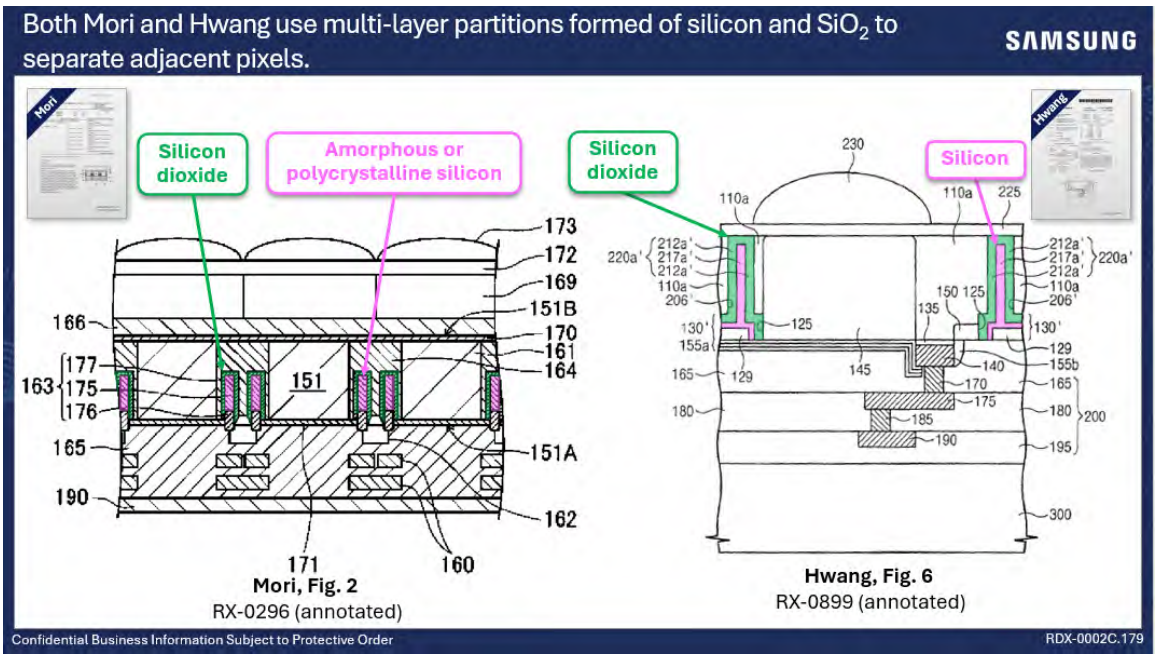
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additionally requires that the *peripheral light trapping material is doped with a dopant to create a surface field*.

As discussed for '714 patent (Ground 1), limitation 1[c], Hwang teaches or suggests *a peripheral light trapping material substantially covering the peripheral sidewall*. Hwang and Mori further render obvious a *peripheral light trapping material* that *is doped with a dopant to create a surface field*.

Q411 How does Hwang and Mori render obvious a *peripheral light trapping material* that is *doped with a dopant to create a surface field*?

A411 As explained for '714 patent, limitation 1[e], and as RDX-0002C.179 illustrates, Hwang's "sidewall multi-layered reflection layer 220*a*' [(*peripheral light trapping material*)] includes a first sidewall reflection layer 212*a*' and a second sidewall reflection layer 217*a*'." Hwang, 11:64-12:12. Hwang discloses that "first sidewall layer 210 [212*a*' in Figure 6] can be a silicon oxide layer," and that "second sidewall reflection layer 215 [217*a*' in Figure 6] can be a silicon layer." Hwang, 10:2-5. As RDX-0002C.179 also illustrates, Mori likewise discloses a multi-layer partition disposed between adjacent pixels of an image sensor and comprising a layer of silicon (silicon layer 175) surrounded between layers of SiO_2 (side SiO_2 film 177). *See* Mori, [0011], [0013], [0028], [0030].



See also Mori, Fig. 6 (illustrating the partition part 163 spanning along the entire side of photoelectric conversion unit 161), [0043]. Moreover, both Hwang and Mori use the Si/SiO_2 partition to mitigate against interference between pixels. *Cf.* Hwang, 15:46-48 ("interference between pixels can be minimized by the sidewall multi-layered reflection layer") *with* Mori, [0027] (Si/SiO_2 partition serves to reduce "color mixing [or 'crosstalk'] due to obliquely incident light").

Q412 Does Mori dope part of its Si/SiO_2 partition?

A412 Yes. Mori teaches that it is beneficial when using such a Si/SiO_2 partition to dope the SiO_2 layer (Mori's SiO_2 layer 177) with impurities, as explained in the overview of Mori. *See* Mori, [0036]. As Mori teaches, this doping is advantageous in mitigating dark current stemming from crystal defects, i.e., to "prevent charges generated when dark due to crystal defects in the partition groove 174 from flowing into the photoelectric conversion unit 161." Mori, [0036]. *See also* JX-0027C (McKee), 93:2-13 (explaining that you "typically try to use a dopant" to prevent dark current); JX-0017C (Sickler), 42:1-10 (explaining that doping is often used to minimize dark current).

Q413 Has the term *doped with a dopant to create a surface field* been construed?

A413 No, and I also understand that the parties have not proposed constructions for this term. Accordingly, I understand I should apply the term's plain meaning.

Q414 Does the '599 patent explain how doping the peripheral light trapping material creates a surface field?

A414 No. The '599 patent does not explain how doping the peripheral light trapping material creates a surface field. Instead, the '599 patent only states that:

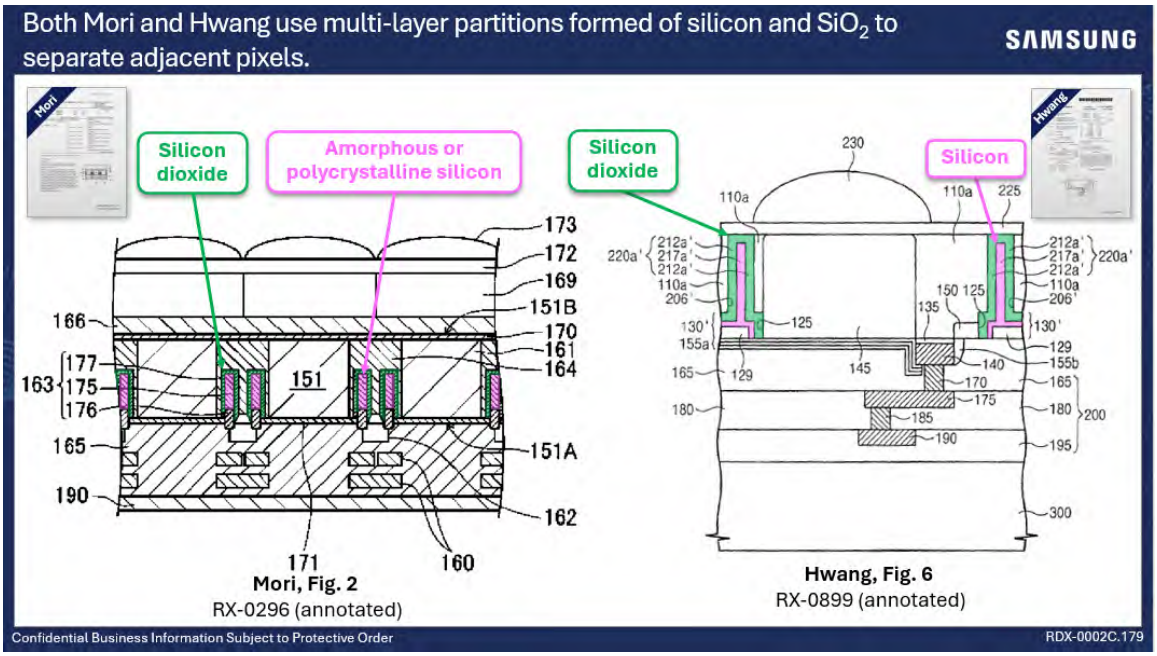
> [I]t can also be beneficial to dope the sidewalls to create a surface field that will improve electrical isolation between the pixels. In one aspect, it can also be beneficial to dope the low refractive index material of the Bragg-type reflectors to increase such electrical isolation.

'599 patent, 10:14-18. The '599 patent states that merely doping—e.g., the manner Mori describes—serves to increase electrical isolation between pixels via a surface field. Accordingly, Mori's doped SiO_2 film located along the side of its pixel (photoelectric conversion unit 161) constitutes a peripheral light trapping material that *is doped with a dopant to create a surface field* as contemplated by the '599 patent's limited disclosure.

Q415 Would POSITAs be motivated to similarly dope Hwang based on Mori's teachings?

A415 Yes. POSITAs would have been motivated to similarly dope Hwang's SiO_2 layers 212*a*' based on Mori's teachings, such that Hwang's *peripheral light trapping material* (sidewall multi-layered reflection layer 220*a*' containing SiO_2 layer 210*a*') *is doped with a dopant to create a surface field* in the same fashion as Mori's SiO_2 film. As RDX-0002C.179 illustrates, Hwang's SiO_2 layer 212*a*' adjoins the side of Hwang's pixel (pixel semiconductor pattern 110*a*), just like how Mori's side SiO_2 film 177 adjoins Mori's pixel.

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POSITAs would have recognized that doping Hwang's SiO_2 layer 212*a*' with impurities would similarly mitigate against dark current stemming from crystal defects in Hwang's sensor, which would improve Hwang's sensitivity. *See* JX-0017C (Sickler), 41:7-8 (explaining that dark current is harmful should be minimized).

Q416 Would POSITAs have reasonably expected success in making this modification?

A416 Yes. POSITAs would have reasonably expected success in making this modification, as Hwang has the same arrangement of a Si/SiO_2 partition disposed at the sidewall between the pixels as Mori. POSITAs would have recognized that doping described in Mori could have been readily implemented in Hwang in the manufacturing steps shown in Hwang's Figures 20/21 after applying layer 212*a*' in grooves 206'.

Q417 Are you aware of Dr. Mansoorian's argument that it is unclear what Mori is teaching?

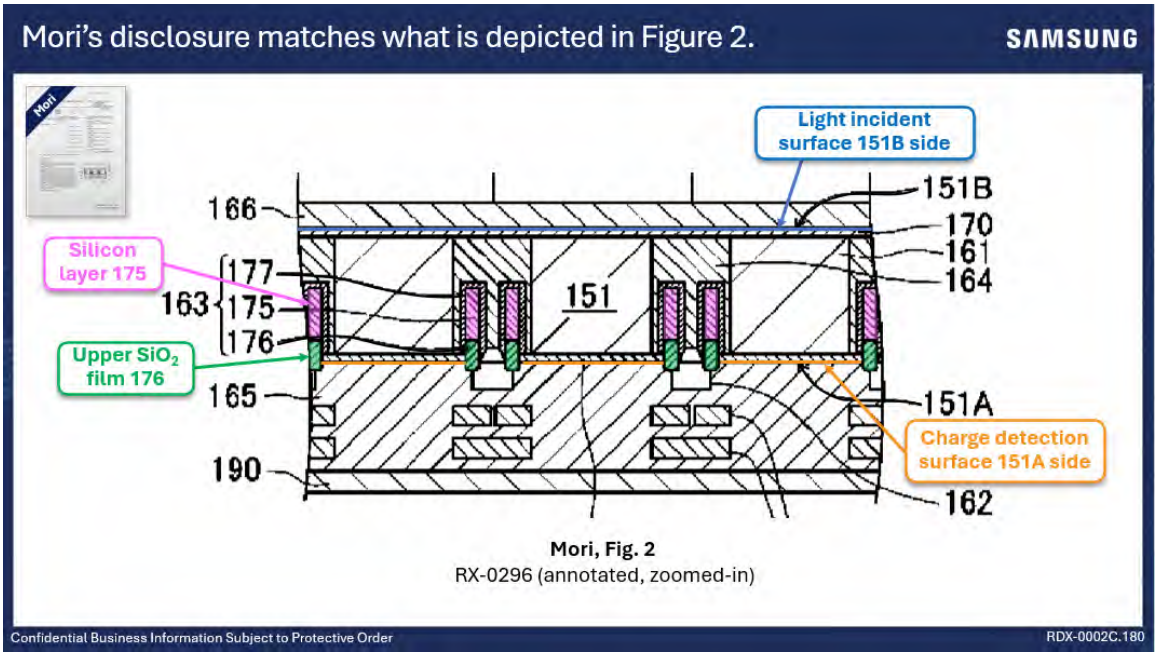
A417 Yes. Dr. Mansoorian opines that "it is unclear what Mori is teaching," and that it is "confusing." RX-0911C, ¶510. I disagree and note this is not a theory presented in SiOnyx's contentions. RX-0606C.281.

To attempt to show Mori is confusing, Dr. Mansoorian quotes the following passage:

> Furthermore, in the present embodiment, the partition part 163 as a silicon layer 175 formed on the light incident surface 151B side, and an upper SiO_2 film 176 formed on the charge detection surface 151A side.

RX-0911C (Mansoorian), ¶510 (quoting Mori, [0028]). According to Dr. Mansoorian, this passage "makes no sense in view of what is shown in FIG. 2," as Figure 2 purportedly shows "silicon layer 175 is not formed on the light incident surface side 151B." RX-0911C, ¶510. However, as RDX-0002C.180 illustrates, Mori's statement is accurate, as the silicon

layer 175 is formed on the light incident surface 151B side of the groove 174, while the upper SiO_2 film 176 is formed on the charge detection surface 151A side of groove 174.



Q418 Are you aware of Dr. Mansoorian's argument that Mori's disclosure is unclear due to its description of SiO_2 film 176?

A418 Yes. Dr. Mansoorian opines that Mori, [0029] is unclear because "it is not clear how the protrusion of film 176 has an impact on where the concentration of n-type impurities in the photoelectric conversion unit is maximum." RX-0911C, ¶511. I disagree and note this is not a theory presented in SiOnyx's contentions. RX-0606C.281.

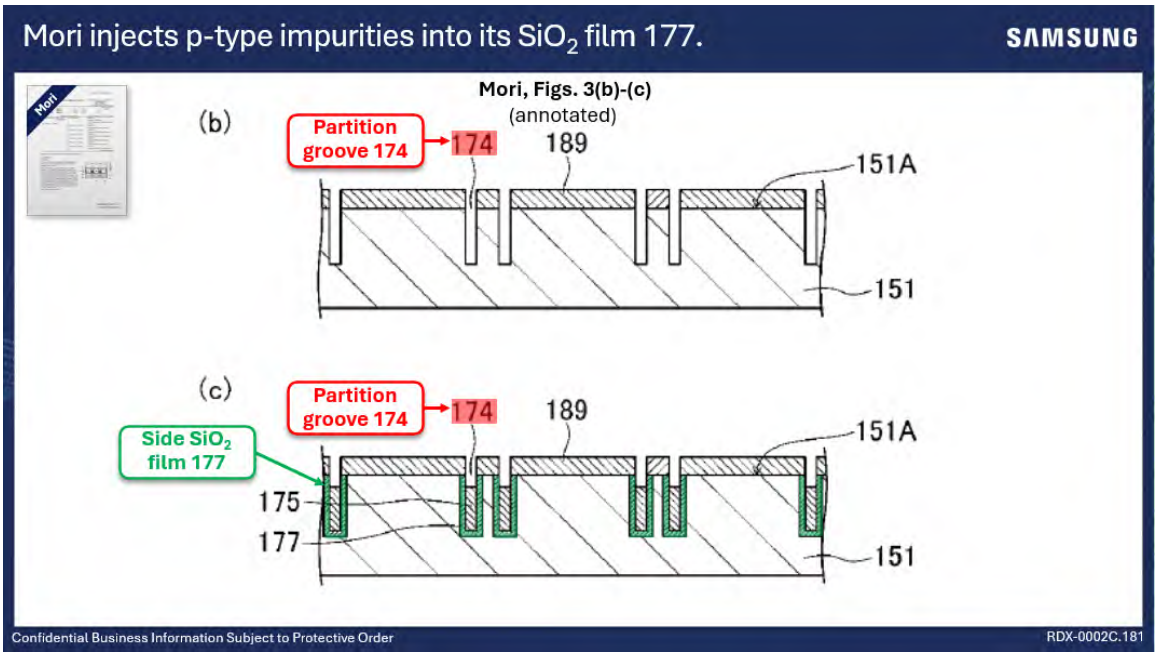
Dr. Mansoorian appears to have misunderstood it. Mori is not stating that SiO_2 film 176's depth impacts the distribution of n-type dopants in the pixel; rather, Mori is teaching that SiO_2 film 176's depth is extended below the pixel to ensure that "intrusion of long wavelength light into adjacent pixels can be reduced." Mori, [0029].

Q419 Are you aware of Dr. Mansoorian's argument that Mori does not dope the side SiO_2 film 177?

A419 Yes. According to Dr. Mansoorian, "Mori states that it is the partition groove 174 that is doped, not the SiO_2 film." RX-0911C, ¶512 (quoting Mori, [0036]). I disagree and note this is not a theory presented in SiOnyx's contentions. RX-0606C.281. Reviewing the paragraph quoted by Dr. Mansoorian shows Mori is doping SiO_2 film 177:

> In order to prevent charges generated when dark due to crystal defects on the partition groove 174 from flowing into the photoelectric conversion unit 161, p-type impurities are preferably injected into the side walls of the partition groove 174 after forming the side SiO_2 film 177.

Mori, [0036]. That is, Mori injects p-type impurities into partition groove 174's sidewall after lining the sidewall with SiO_2 film 177. As RDX-0002C.181 illustrates, once deposited side SiO_2 film 177 completely covers partition groove 174's sidewalls, such that POSITAs would understand that to inject p-type impurities into groove 174's sidewalls would require injecting p-type impurities into SiO_2 film 177.[9]



Accordingly, because Mori teaches that "p-type impurities are injected … after forming the side SiO_2 film 177," POSITAs would understand that p-type impurities must be injected into side SiO_2 film 177.

Q420 Are you aware of Dr. Mansoorian's argument that all the p-type impurities would pass through SiO_2 film 177?

A420 Yes. Apparently conceding that Mori injects p-type impurities into side SiO_2 film 177 to dope partition groove 174's sidewalls, Dr. Mansoorian next opines that "[a]t the lowest injection energy of 5keV, the p-type impurities would penetrate about 20-30nm through SiO_2, meaning all the way through Mori's SiO_2 film and into the side walls of the partition groove." RX-0911C, ¶513. I disagree and note this is not a theory presented in SiOnyx's contentions. RX-0606C.281.

Mori explains p-type impurities are injected using ion implementation, that the SiO_2 film 177 has "a thickness of 5 nm to 20 nm," and that the p-type impurity is injected with "an

[9] While Mori's Figure 3 does not depict an image after side SiO_2 film 177 is deposited but before silicon layer 175 is deposited, POSITAs would expect that p-type impurities are injected into partition groove 174's sidewalls before silicon 175 is deposited, as it would be difficult to inject p-type impurities through silicon 175—which fills partition groove 174—and into partition groove 174's sidewalls.

injection energy of 5 to 30 keV." Mori, [0036]. In ion implantation of silicon-based systems, the most commonly used p-type dopant is boron. The implant range—i.e., the distance into the target material at which most implanted dopants stop—of boron in silicon or SiO_2 is similar, and boron implanted at normal (perpendicular) incidence has a range of approximately 20nm at 5keV. Accordingly, POSITAs would understand that approximately half of the boron would remain in Mori's SiO_2 film 177—while the other half would be implanted into the underlying silicon—when selecting a SiO_2 thickness of 20nm and an injection energy of 5keV. Moreover, for an angled implant (i.e., an implant at a shallower anger than normal (perpendicular) incidence), as would likely be required in Mori, the penetration's depth becomes shallower resulting in more boron remaining in the SiO_2 film 177.

Q421 Are you aware of Dr. Mansoorian's assertion that POSITAs would not make this combination, as Hwang allegedly mitigates dark current using physical separation?

A421 Yes. Dr. Mansoorian opines that "dark current in the device of Hwang is mitigated by physically separating the 'groove 206' from the light sensitive, active portion of 'pixel semiconductor 110*a*,'" such that doping "would be unnecessary and redundant." RX-0911C, ¶¶515-516. I disagree and note this is not a theory presented in SiOnyx's contentions. RX-0606C.393.

As an initial matter, as explained for '714 patent (Ground 1), limitation 1[a], I disagree with Dr. Mansoorian's definition of pixel for Hwang. In my opinion, Hwang's pixel would contact groove 206. Regardless, even assuming Dr. Mansoorian is correct regarding Hwang's pixel, I disagree that POSITAs would find doping to be "unnecessary and redundant" as Dr. Mansoorian asserts. POSITAs would understand that the separation between groove 206 and what Dr. Mansoorian alleges is the "active portion" of Hwang's pixel, photodiode 145, provided by the alleged "dead zone" of pixel semiconductor pattern 110*a* is not large enough to mitigate dark current, and any dark current caused by defects in groove 206 would likely travel to photodiode 145. Despite Dr. Mansoorian's speculation that Hwang possesses a "large dead zone," RX-0911C, ¶141 (Hwang is not drawn to scale nor gives dimensions), POSITAs would understand that it is not large enough to prevent current travelling within, and, indeed, would be motivated to minimize its size if it was indeed, a "dead zone." Moreover, POSITAs would recognize that doping Hwang's sidewall multi-layered reflection layer would reduce dark current, such that the size of "dead zone" could be reduced, allowing for more tightly packed pixels and a more sensitive image sensor.

Q422 Are you aware of Dr. Mansoorian's argument that Mori teaches away from doping Hwang because Mori teaches doping metals?

A422 Yes. Dr. Mansoorian opines that "Mori teaches that doping to mitigate dark current is necessary in devices using metal as an isolation material disposed in a trench," and accordingly "teaches away from the need to dope the peripheral light trapping material in the device of Hwang." RX-0911C, ¶517 (citing Mori, [0008]). I disagree and note this is not a theory presented in SiOnyx's contentions. RX-0606C.281.

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Contrary to Dr. Mansoorian's assertions, Mori does not teach that doping is necessary to mitigate dark current in devices using metal partitions. Rather, Mori identified a problem in the prior art, namely, that because "metal is embedded in the silicon material," it "increases crystal defects in the silicon layer and increases charges generated when dark." Mori, [0008]. Mori proposes a two-step solution to overcome this problem. First, Mori replaces the metal partition with "a partition part made of a silicon layer," Mori, [0010], and "a side silicon oxide film formed between the silicon layer and the semiconductor substrate," Mori, [0013], for "charge[s] generated when dark [to] be reduced, and the sensitivity of the solid-state imagining device [to] be improved," Mori, [0012]. Next, Mori explains that "[i]n order to [further] prevent charges generated when dark … p-type impurities are preferably injected into the side walls of the partition groove 174 after forming the side SiO_2 film 177." Mori, [0036]. As explained, Mori injects p-type impurities (dopes) after forming the side SiO_2 film, such that the impurities are injected into the SiO_2 film (part of the peripheral light trapping material). Mori does not teach doping metals, nor would POSITAs understand doping to refer to introducing impurities into metals.

b. Claim 6

Q423 Let's turn to claim 6, which is *[t]he device of claim 1, wherein the dopant is boron or antimony*. Have you formed an opinion regarding this claim?

A423 Yes. Hwang and Mori render this claim obvious. As explained for '599 patent, limitation 1[c], it would have been obvious in view of Mori to inject p-type impurities into and through the peripheral light trapping material (i.e., SiO_2) and into the silicon layer—i.e., Mori teaches using a p-type dopant in the silicon layer.

Using *boron* as the dopant would have been further obvious, as boron is one of the most commonly used p-type dopants for silicon-based systems. *See* RX-0219.27-28 (Wolf) (explaining that Column-IV materials (e.g., silicon) are commonly doped with Column-III-dopants (e.g., boron)). POSITAs would have understood that using boron as the p-type dopant for silicon-based systems is a known technique that would have yield predictable results, particularly in light of boron's similar use as a p-type dopant in other similar light trapping devices. *See* RX-0291 (Chen), [0011] ("substrate 35 is a silicon substrate doped with a P-type dopant such as boron, in which case the substrate 35 is a P-type substrate"). Moreover, this claim would have also been obvious because POSITAs would have had a limited number of types of p-type dopants from which to choose.

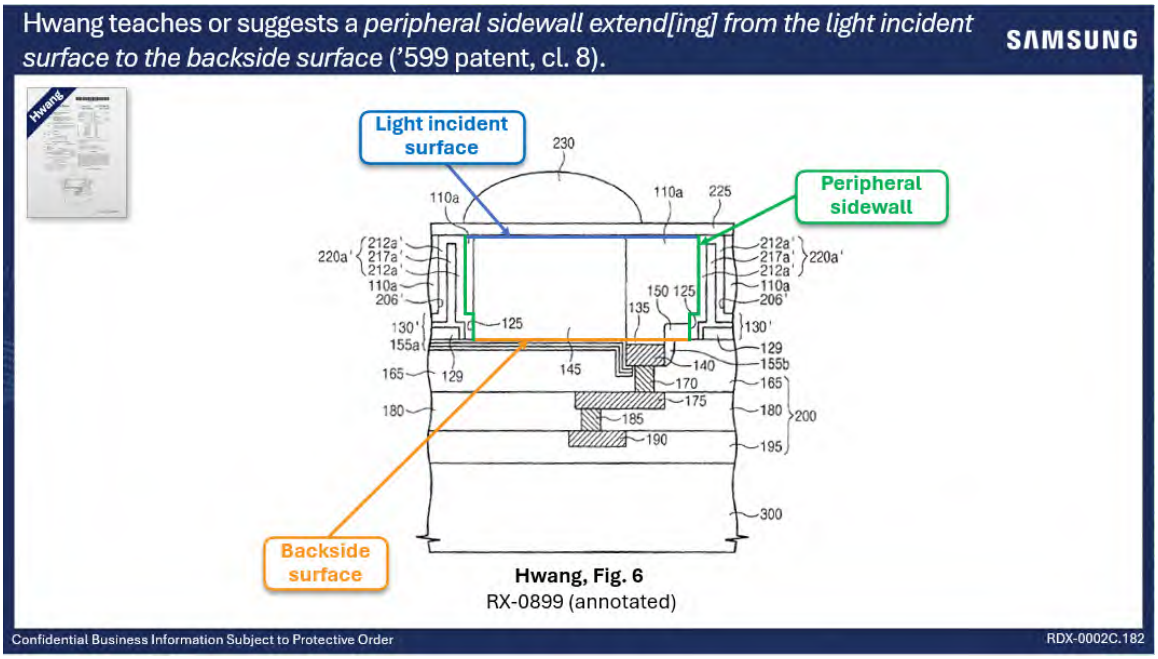
c. Claim 8

Q424 Let's turn to claim 8, which is *[t]he device of claim 1, wherein the peripheral sidewall extends from the light incident surface to the backside surface*. Have you formed an opinion regarding this claim?

A424 Yes. Hwang, Konno, and Mori render this claim obvious. As discussed for '599 patent (Ground 1), limitation 19[a], Hwang teaches that the *peripheral sidewall* (trench wall where pixel semiconductor pattern 110*a* contacts sidewall multi-layered reflection layer

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220*a*') *extends from the light incident surface to the backside surface*, as RDX-0002C.182 illustrates.



d. Claim 11

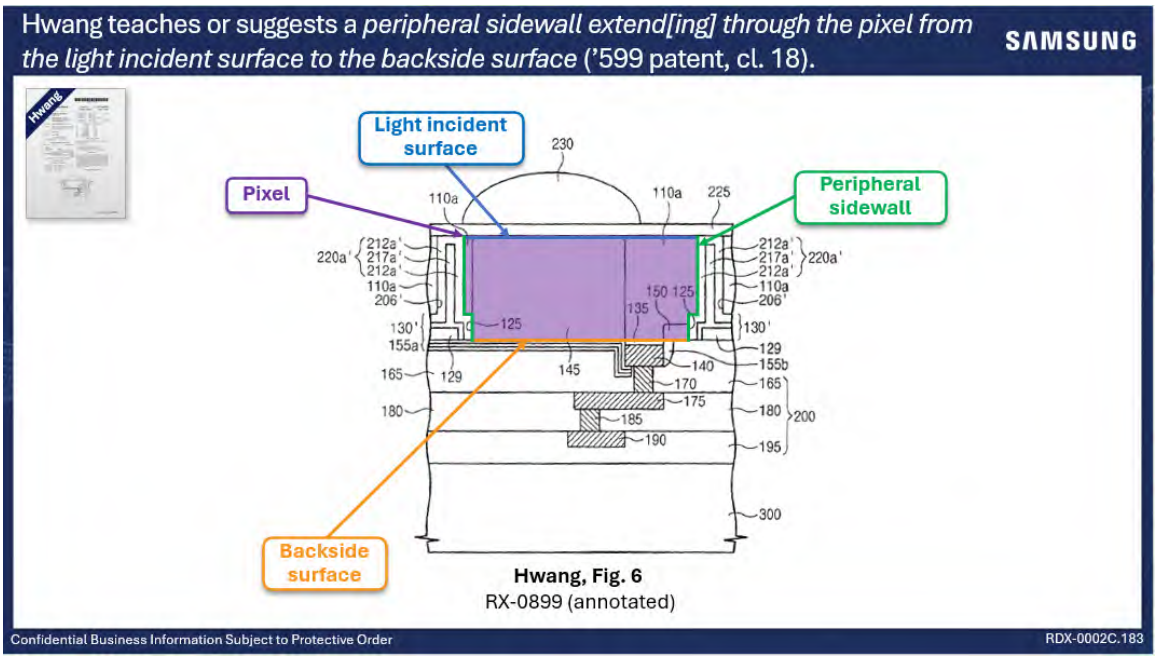
Q425 Let's turn to claim 11, which is *[t]he device of claim 11, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer*. Have you formed an opinion regarding this claim?

A425 Yes. Hwang, Konno, and Mori render this claim obvious. As explained for '599 patent (Ground 1), limitations 19[b] and [d], modifying Hwang based on Konno to use Konno's second reflecting layer 120 in place of Hwang's base multi-layered reflection layer 155*a* (*backside light trapping material*) would have been obvious. Konno discloses that its second reflecting layer 120 *is a metal layer*. *See* Konno, 8:31-38 ("second reflecting layer 120 … can be formed by forming a thin film of a metal such as aluminum and silver"), 13:57-59 (teaching that the second reflecting layer 120 is identical in the first and second embodiments besides its "shape").

e. Claim 18

Q426 Let's turn to claim 18, which is *[t]he device of claim 1, wherein the peripheral sidewall extends through the pixel substantially from the light incident surface to the backside surface*. Have you formed an opinion regarding this claim?

A426 Yes. Hwang, Konno, and Mori render this claim obvious. As discussed for '714 patent (Ground 1), limitation 1[a], Hwang teaches that the *peripheral sidewall* (trench wall where pixel semiconductor pattern 110*a* contacts sidewall multi-layered reflection layer 220*a*') *extends through the pixel substantially from the light incident surface to the backside surface*, as RDX-0002C.183 illustrates.



B. Yamada-based Grounds

Q427 Let's turn to your Yamada-based opinions. Can you please summarize your anticipation and obviousness opinions for the '599 patent based on Yamada?

A427 My Yamada-based opinions are based on a single ground, Ground 3, which is that Yamada and Roy render obvious claims 1, 6, 8, 11, and 18.

1. Ground 3: Yamada and Roy Render Obvious Claims 1, 6, 8, 11, and 18

a. Claim 1

1. Limitation 1[a]

Q428 Let's start with claim 1. Claim 1's first limitation, 1[a], is *at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending at least partially around the pixel periphery*. Does Yamada satisfy this limitation?

A428 Yes. As RDX-0002C.185 illustrates, with differences shown in red, '599 patent, limitation 19[a] is identical to '714 patent, limitation 1[a], except that '599 patent, limitation 19[a] requires that the peripheral sidewall extend *at least partially* around the pixel periphery, whereas '714 patent, limitation 1[a] requires that the peripheral sidewall be *disposed into at least a portion of the pixel*, and extend *at least substantially* (as opposed to only *partially*) around the pixel periphery.

As discussed for '714 patent (Ground 4), limitation 1[a], Yamada teaches or suggests a peripheral sidewall that extends *at least substantially around the pixel periphery*.

Accordingly, Yamada teaches or suggests the more broad requirement that the peripheral sidewall extends only *at least partially around the pixel periphery* for the same reasons.

2. Limitation 1[b]

Q429 Limitation 1[b] is *a backside light trapping material at least partially covering the backside surface*. Does Yamada satisfy this limitation?

A429 Yes. As RDX-0002C.186 illustrates, '599 patent, limitation 19[b] is identical to '714 patent, limitation 1[b]. Yamada teaches or suggests '599 patent, limitation 19[b] for the reasons discussed for '714 patent (Ground 4), limitation 1[b].

3. Limitation 1[c]

Q430 Limitation 1[c] is *a peripheral light trapping material substantially covering the peripheral sidewall, wherein said peripheral light trapping material is doped with a dopant to create a surface field*. Have you formed an opinion regarding this limitation?

A430 Yes. As part of his infringement opinions, Dr. Foty has opined that the Accused Products satisfy this limitation, and that this limitation is satisfied so long as at least part of the peripheral light trapping material is doped. RX-0905C, ¶¶1089-1095. To the extent that this limitation can be read to cover the accused Products and that this limitation is satisfied so long as at least part of the peripheral light trapping material is doped, Yamada and Roy render it obvious.

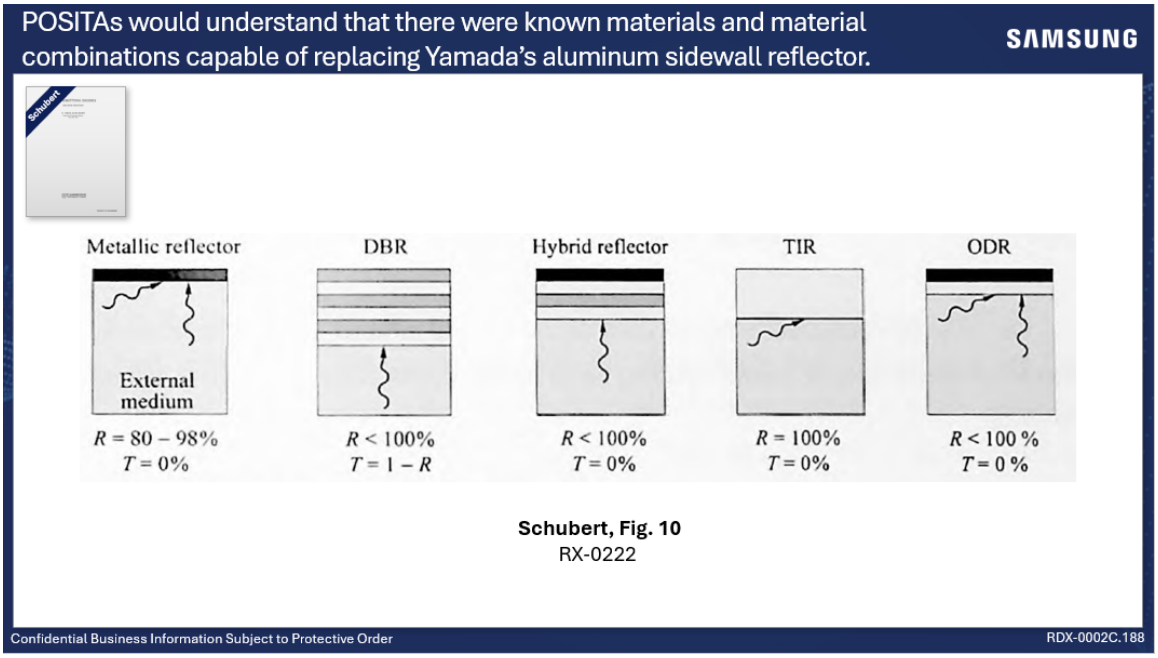
As RDX-0002C.187 illustrates, with differences shown in red, '599 patent, limitation 1[c] is identical to '714 patent, limitation 1[c], except that '599 patent, limitation 1[c] additionally requires that the *peripheral light trapping material is doped with a dopant to create a surface field*.

As discussed for '714 patent (Ground 4), limitation 1[c], Yamada teaches or suggests *a peripheral light trapping material substantially covering the peripheral sidewall*. Yamada and Roy further render obvious a *peripheral light trapping material* that *is doped with a dopant to create a surface field*.

Q431 How does Yamada and Roy render obvious a *peripheral light trapping material* that is *doped with a dopant to create a surface field*?

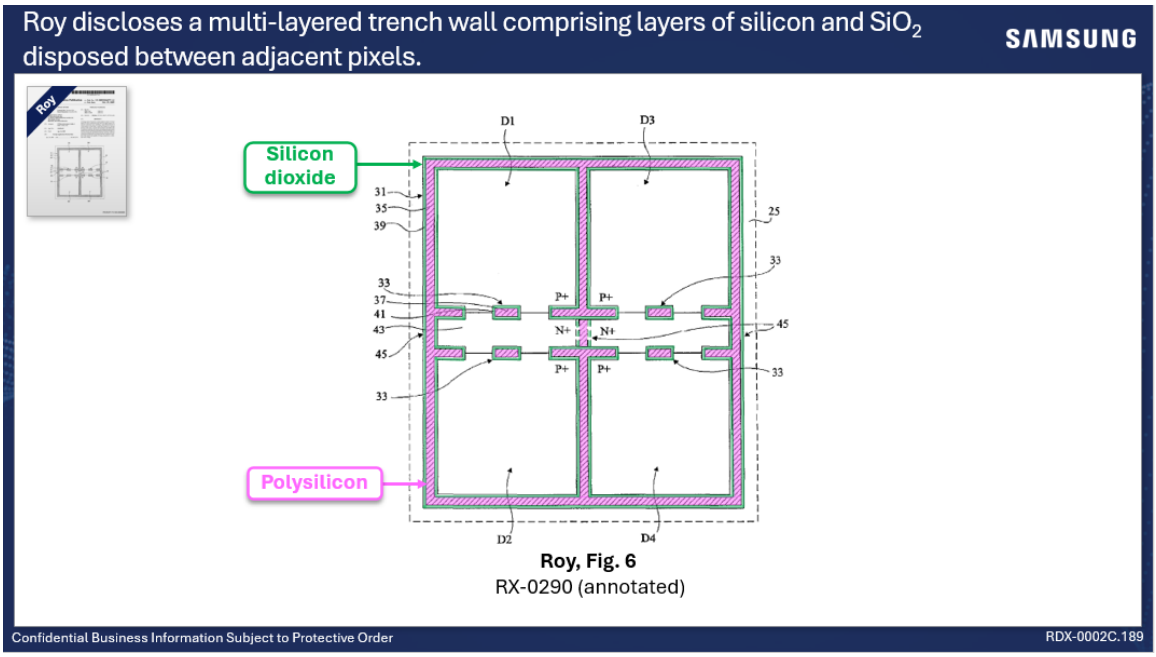
A431 As explained for '714 patent (Ground 4), limitation 1[c], Yamada discloses a *peripheral light trapping material* comprising third reflective film 11 that "can be made of a metal" such as aluminum. Yamada, [0012]. However, POSITAs would have recognized that there were other known materials and material combinations that could be used in such peripheral light trapping materials, each having its own benefits and considerations. *See* JX-0027C (McKee), 82:13-83:8 (describing different materials, such as dielectrics or metals that can be used as materials to optically isolate a pixel). For example, as RDX-0002C.188 illustrates, Schubert discusses the "[d]ifferent types of reflectors" to use in optoelectronic devices, i.e., "a metallic reflector, distributed Bragg reflector (DBR), hybrid

metal-DBR reflector based on total internal reflector (TIR), and [a triple-layer] omni-directional reflector (ODR)," Schubert, 163.



Q432 Does Roy disclose an alternative to Yamada's aluminum sidewall reflectors?

A432 Yes. As RDX-0002C.189 illustrates, Roy discloses a multi-layered trench wall disposed between adjacent pixels of an image sensor comprising layers of polysilicon (conductive layers 35, 37) and SiO_2 (dielectric layers 39, 41).



As explained regarding the overview of Roy, Roy teaches that it is beneficial when using a Si/SiO_2 film to use "heavily-doped polysilicon" as the silicon layer, Roy, [0050], and that "[t]he upper surfaces of the conductive materials of trench 31/45 is connected to a metallization (not shown) which enables putting this material in contact with a bias signal (V_p)," Roy, [0056].

Q433 Why does Roy dope and bias its polysilicon?

A433 Roy teaches that this doping and biasing "enables eliminating dark currents which are usually formed at the interface with insulation areas." Roy, [0071]. Specifically, Roy explains that:

> [T]he biasing of trench 31 to a reference voltage, and also of column 33 during the accumulation phase, which forms an accumulation of holes at the photodiode periphery, enables eliminating dark currents which are usually formed at the interface with insulation areas. The structure according to an embodiment thus enables significantly decreasing parasitic physical phenomena which usually occur in conventional devices.

Roy, [0071].

Q434 Would it be obvious to POSITAs to implement Roy's teachings in Yamada?

A434 Yes. It would have been obvious to use Si/SiO_2 films where the silicon layer comprises heavily doped polysilicon that is biased to obtain the benefits Roy describes, i.e., "eliminating dark currents" and "significantly decreasing parasitic physical phenomena." Roy, [0071]. Moreover, POSITAs would have reasonably expected success in doing so with predictable results. In fact, it was well-known that layers of silicon and SiO_2 could be used as reflectors. *See* Schubert, 163, 173 (explaining that Si/SiO_2 DBRs "yield high reflectivity"), 177 (explaining that Si and SiO_2 are "natural candidates" for "omnidirectional reflectors").

Q435 Are there any other reasons why POSITAs would be motivated to make this combination?

A435 Yes. POSITAs would understand that isolation elements comprising metal thinly insulated from the pixel exhibit increased dark current, *See* Mori, [0007]-[0008], and that a known solution to reduce dark current was to replace such thinly insulated metal isolation elements, like Yamada's aluminum third reflective films 11, with a Si/SiO_2 reflector. *See* Mori, [0029]-[0030].

Q436 Would this modification satisfy limitation 1[c]?

A436 Yes. Yamada, as modified by Roy and containing multiples layers of silicon and SiO_2, would include a *peripheral light trapping material*. As explained for'714 patent (Ground 4), limitation 1[c], this peripheral light trapping material would also *substantially cover[] the peripheral sidewall*.

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Q437 How would the Si/SiO_2 reflector constitute a *light trapping material* under the parties' proposed constructions?

A437 The Si/SiO_2 reflector would constitute a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

Q438 Has the term *doped with a dopant to create a surface field* been construed?

A438 No, and I also understand that the parties have not proposed constructions for this term. Accordingly, I understand I should apply the term's plain meaning.

Q439 Does the '599 patent explain how doping the peripheral light trapping material creates a surface field?

A439 No. The '599 patent does not explain how doping the peripheral light trapping material creates a surface field. Instead, the '599 patent only states that:

> [I]t can also be beneficial to dope the sidewalls to create a surface field that will improve electrical isolation between the pixels. In one aspect, it can also be beneficial to dope the low refractive index material of the Bragg-type reflectors to increase such electrical isolation.

'599 patent, 10:14-18. The '599 patent states that merely doping serves to increase electrical isolation between pixels via a surface field. The '599 patent does not disclose, nor claim, doping *and then the application of a bias voltage to create a surface field*, as is done in Roy. *Compare*, '599 patent, limitation 1[c], 10:18-18 *with* Roy, [0071]. However, I understand that the structure Roy discloses is the same structure Dr. Foty accuses of infringement. RX-0905C, ¶¶1089-1095. Accordingly, Roy teaches a *peripheral light trapping material* [that] *is doped with a dopant to create a surface field* to the extent this limitation could be read to cover the Accused Products.

Q440 Would POSITAs be motivated to dope Yamada, as modified by Roy?

A440 Yes. POSITAs would have recognized that the doping Roy describes could have been readily implemented in Yamada. For example, Roy's doping could have been readily implemented in Yamada prior to the second deposition of Yamada's second insulating film 12, as shown in Figure 3(e).[10]

[10] Yamada's Figure 7—corresponding to Yamada's fifth embodiment, *see* Yamada, [0049]-[0050]—"share[s] the third reflecting film 11 between neighboring light receiving sections," but the "[o]ther details are the same as in the first embodiment and are not described," with respect to its fifth embodiment. Yamada, [0049]. Accordingly, disclosures made regarding Figure 3, which shows the manufacturing process for Yamada's first embodiment, *see* Yamada. [0028], are pertinent to Figure 7.

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Q441 Could the polysilicon, as added to Yamada in view of Roy, be connected to a metallization as Roy teaches?

A441 Yes. POSITAs would recognize that Yamada could be configured such that the polysilicon replacing Yamada's third reflective films 11 is connected with a metallization to enable it to be in contact with a bias signal. *See* Yamada, Fig. 4, [0041] ("explaining that in Figure 4 "the first insulating film 9 arranged between the third reflective film 11 and the semiconductor substrate 1 is removed," such that "third reflective film 11 can be used as an electrode").

Q442 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination as Yamada allegedly does not need improvement?

A442 Yes. Dr. Mansoorian opines that POSITAs "would not have looked to Roy for inspiration to modify Yamada because Yamada discloses a complete design and does not indicate that it needs improvement," as it "already teaches a series of reflective films covering the PIN photodiode." RX-0911C, ¶576. I disagree.

While Dr. Mansoorian is correct that Yamada discloses a device designed to optically isolate pixels by trapping light within, Yamada does not address how to electrically isolate pixels or prevent dark current. POSITAs would accordingly look to improve Yamada, as electrical isolation and dark current mitigation are considerations for optoelectronic devices, something Dr. Mansoorian repeatedly stresses throughout his report, and that SiOnyx employees and the prior art have verified. *E.g.*, RX-0911C (Mansoorian), ¶171, ¶178 ("many of the prior art references relied upon by Dr. Neikirk highlight the importance of minimizing dark current") (citing Shinohara, Iida, Konno), ¶180, ¶196, ¶484 (arguing against modifications made to Suzunaga as they would "increase he generation of dark current"), ¶487; JX-0017C (Sickler), 42:1-10; McKee, 93:2-13; *see generally* RX-0911C, Shinohara, Iida, Konno, Mori, Roy.

As explained, Yamada's thinly insulated metal partition is likely to cause dark current, as Mori teaches, thus motivating POSITAs to look to other sources, e.g., Roy, in order to mitigate such dark current.

Q443 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination because Schubert is directed to reflectors that allegedly would not be used in this combination?

A443 Yes. Dr. Mansoorian opines POSITAs would not make this combination by referencing his Haddad188 and Schubert argument for '714 patent, claim 1, that "Schubert teaches the use of DBRs for omni-directional reflectors in LEDs," that "Schubert teaches that 'a multi-layer reflector consisting of typically 5-50 pairs of two materials with different refractive indices,' and teaches that the reflectivity of the DBR increases with the number of materials used." RX-0911C, ¶579. I disagree and note these theories were not presented in SiOnyx's contentions. RX-0606C.452-454.

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Q444 Why do you disagree?

A444 As discussed at length for '714 patent (Ground 6), limitation 1[e] regarding Haddad188 in view of Schubert, I disagree with Dr. Mansoorian's opinions that Schubert is non-analogous art merely because it is a textbook concerning LEDs. Rather, Schubert's discussion of reflectors is pertinent to image sensors, given both the similarities between LEDs and image sensors and that reflectors in both are designed to reflect incident photons.

I further disagree with Dr. Mansoorian's opinion that POSITAs would not consider Schubert's teachings because it "teaches the use of DBRs for omni-directional reflectors." RX-0579C, ¶579. To the contrary, POSITAs would recognize that it would be desirable to use reflectors with omnidirectional characteristics as the peripheral isolation material. Indeed, Si/SiO_2 reflectors—a "natural candidate for such [omnidirectional reflectors]," Schubert, 181—are commonly used as the peripheral isolation material in similar devices. *E.g.*, Hwang, 9:28-30, 10:2-5, 10:28-35, 12:4-7; Suzunaga, [0008], [0064]; Mori, [0012]-[0013], [0023], [0027].

Moreover, POSITAs would recognize that, while Schubert said DBRs "consist[] of typically 5-50 pairs," Schubert, 171, DBRs can be suitable reflectors using fewer pairs—particularly if using a high-contrast DBR like a Si/SiO_2 reflector. For example, Schubert teaches that 100% reflectance at approximately 1-1.4μm can be achieved while only using four pairs of Si/SiO_2. Schubert, Fig. 10.8. Additionally, as explained for '714 patent (Ground 1), claim 1, Hwang teaches that its Si/SiO_2 sidewall multi-layered reflection layer 220 reflects incident light back into Hwang's pixel, and that it can be made with as few as three layers (i.e., 1.5 pairs). *E.g.*, Hwang, 9:28-30, 10:2-5, 10:28-35, 12:4-7.

Q445 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination as Roy's structure would not provide sufficient optical isolation?

A445 Yes. Dr. Mansoorian opines that POSITAs would not make this combination because "Roy's disclosure of a single pair of materials [is not] a DBR," "there are no teachings in Roy to suggest optical isolation is even desirable," and "because Roy's Si/SiO_2 structure has only one pair of materials, the teachings of Schubert would suggest to a POSITA that Roy's structure is significantly less effective of a reflector than Yamada's existing metal reflector." RX-0911C, ¶¶579-580. I disagree.

As explained, POSITAs would be motivated to incorporate Roy's teachings because Roy addresses electrical isolation—something Yamada does not address but POSITAs would recognize would be desirable to incorporate. While Roy does not address optical isolation, Yamada does, and POSITAs would thus be motivated to incorporate Roy's teachings while maintaining Yamada's optical isolation. As explained, POSITAs would recognize that Roy's Si/SiO_2 structure could be modified—e.g., by adding layers or increasing layer thickness, as Schubert teaches—to optimize optical isolation, and would have reasonably expected success in doing so, given that similar devices use Si/SiO_2 peripheral structures to optically isolate pixels. *E.g.*, Hwang, 9:41-43. 10:2-5, 11:64-12:12; Suzunaga, [0064].

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POSITAs would be motivated to make this modification to provide Yamada with a significant increase in electrical isolation even if this change resulted in a decrease in optical isolation.

Q446 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination as it would allegedly increase manufacturing complexity?

A446 Yes. Dr. Mansoorian opines that POSITAs "would have understood that replacing a single metal film with two films (Si/SiO_2) would increase the complexity and decrease the yield when manufacturing Yamada's device." RX-0911C, ¶580. I disagree. First, filling deep trench isolation structures with multiple materials and layers was well within a POSITAs knowledge at least by the Light Trapping Patent's priority date, as evidenced by the numerous prior art references I have discussed. For example, Suzunaga—published over ten years before the Light Trapping Patents—discloses that its dielectric isolation 5 can consist of alternating layers of silicon and SiO_2. Suzunaga, [0064]. Likewise, Hwang teaches that its sidewall multi-layered reflection layer 220*a*' can contain multiple pairs of its silicon layer 212 and SiO_2 layer 217. Iida, Hirigoyen, Shinohara, and Mori similarly disclose multi-layer and multi-material deep trench isolation reflectors. Second, even if replacing Yamada's metal reflector with Si/SiO_2 was more complex, POSITAs would still be motivated to do so due to the benefits of Si/SiO_2 I have described (e.g., reduced dark current).

Q447 Are you aware of SiOnyx's argument that Roy's dielectric material 39 is too thin to be optically isolating?

A447 Yes. While not advanced by Dr. Mansoorian, SiOnyx contended that Roy's thin dielectric material 39 is too thin to be part of any optical structure. RX-0606C.453 (SiOnyx Validity Contentions). I disagree. Si/SiO_2 reflectors were commonly used as peripheral light trapping materials in similar sensors. *See* Hwang, 9:25-30, 10:2-5, Suzunaga, [0035]. As explained, POSITAs would understand that such a partitions the reflectivity of Si/SiO_2 reflectors could be increased by increasing the number of alternating layers and/or increasing layer thickness. *See* Schubert, 170; Suzunaga, [0028], [0032]. Moreover, Roy's dielectric material 39 is almost twice as thick as the layers that SiOnyx's other expert, Dr. Foty, has accused of infringing as being part of peripheral light trapping materials. *See* RX-0905C, ¶435-55; RX-0128 (Teardown Report).

4. Limitation 1[d]

Q448 Limitation 1[d] is *a reflective layer coupled to the light incident side and having an aperture to allow entry of light into the pixel*. Does Yamada satisfy this limitation?

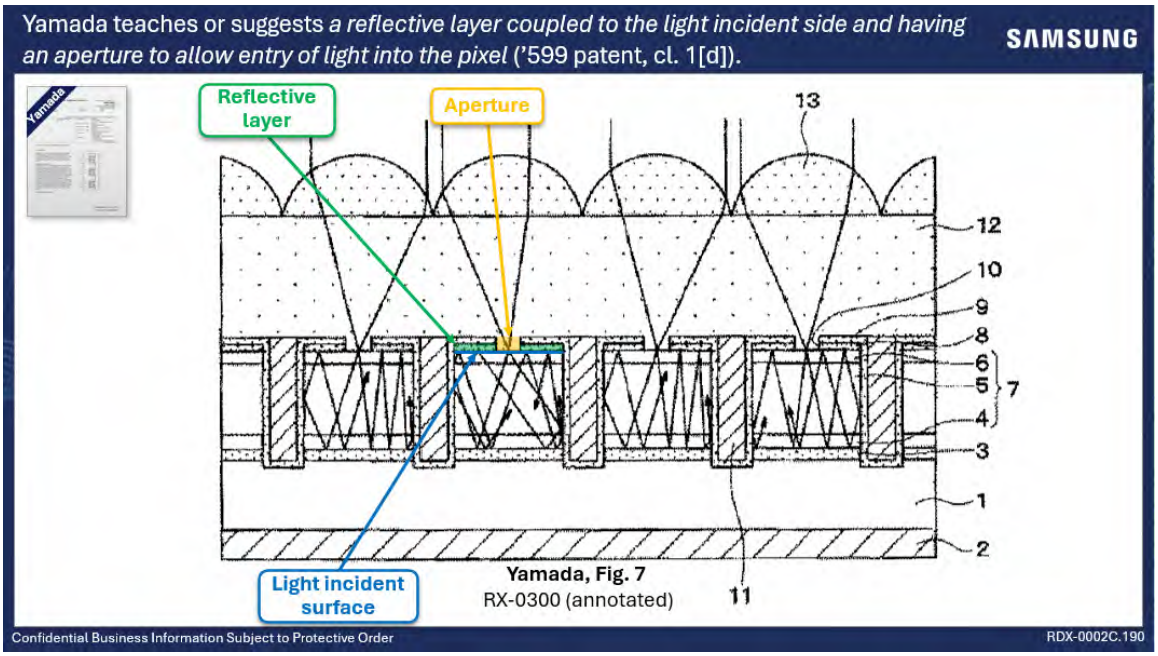
A448 Yes. Yamada teaches or suggests *a reflective layer coupled to the light incident side and having an aperture to allow entry of light into the pixel*.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *reflective layer*. Yamada teaches or suggests a *reflective layer coupled to the light incident side* under either construction.

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Q449 How does Yamada satisfy this limitation?

A449 As RDX-0002C.190 illustrates, Yamada includes a "second reflective film (8) [(*reflective layer*) that is] arranged opposing the first reflective film (3) at a front surface of the light receiving section (7) [(*light incident side*)] and is formed with a through-hole 10 [(*aperture*)]." Yamada, [0009].



Q450 Is Yamada's second reflective film 8 a *reflective layer*?

A450 Yes. Yamada teaches that "light that enters the light receiving section (7) is reflected by … second reflective film (8) … so as to be confined within the light receiving section 7." Yamada, [0010]. In particular, Yamada teaches that "second reflective film 8 … is configured so that the light to be detected is reflected [back into the light receiving section 7] with a high reflectance of at least 99 percent." Yamada, [0024].

Q451 How does second reflective film 8 constitute a *reflective layer* under the parties' proposed constructions?

A451 Second reflective film 8 constitutes a *reflective layer* under either party's proposed construction, as it is a layer that reflects and will reflect more light back into the pixel than it transmits for the reasons just explained.

Q452 Is Yamada's through-hole 10 *an aperture to allow entry of light into the pixel*?

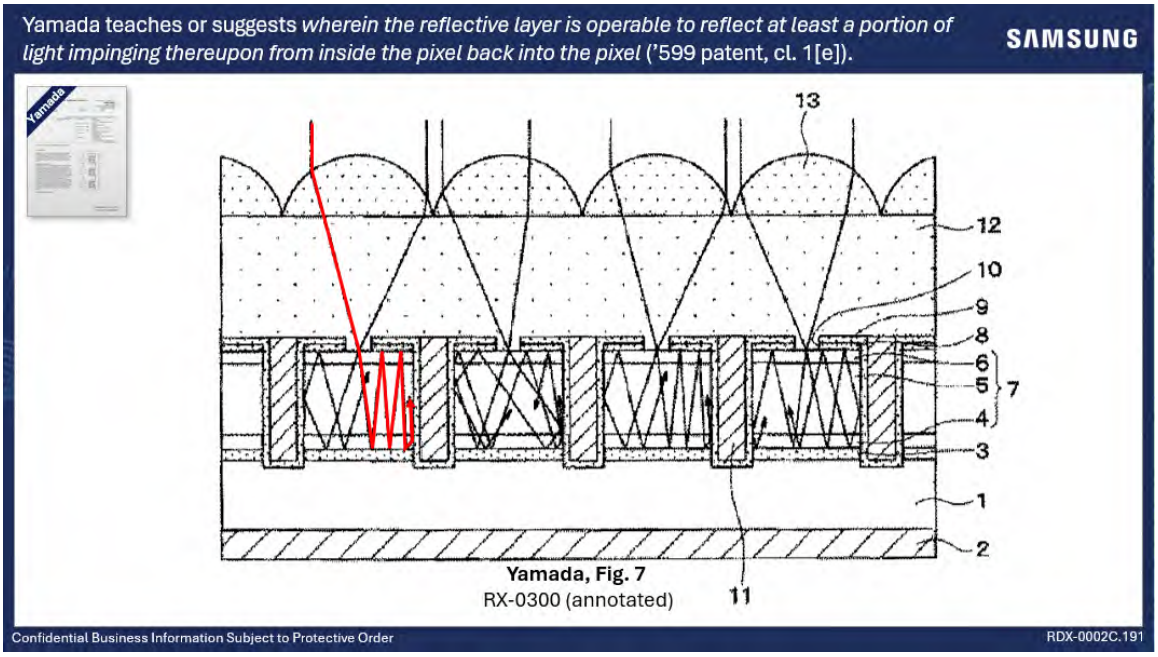
A452 Yes. Yamada discloses that its *aperture* is used *to allow entry of light into the pixel*. In particular, Yamada discloses that the "through-hole 10 [(*aperture*)] expose[s] a portion of the front surface of the light receiving section (7) [(*pixel*)]" to light. Yamada, [0009].

5. Limitation 1[e]

Q453 Limitation 1[e] is *wherein the reflective layer is operable to reflect at least a portion of light impinging thereupon from inside the pixel back into the pixel back into the pixel.* Does Yamada satisfy this limitation?

A453 Yes. I understand that the ALJ has amended the term *thereupon from inside the pixel back into the pixel back into the pixel*s such that it is now *thereupon from inside the pixel back into the pixel*. Order No. 36 at 40.

Yamada's *reflective layer* (second reflective film 8) coupled to the light incident side i*s operable to reflect at least a portion of light impinging thereupon from inside the pixel back into the pixel*. As RDX-0002C.191 illustrates, Yamada depicts a light ray being reflected by reflective film 8 (*reflective layer*) back into the pixel.



b. Claim 6

Q454 Let's turn to claim 6, which is *[t]he device of claim 1, wherein the dopant is boron or antimony*. Have you formed an opinion regarding this claim?

A454 Yamada and Roy render this claim obvious. As explained for '599 patent (Ground 3), limitation 1[c], it would have been obvious in view of Roy use heavily doped polysilicon in Yamada's peripheral light trapping material. It would have further been obvious that Roy dopes the polysilicon layer with a p-type dopant. For example, Roy teaches that a -1V bias signal is applied to semiconductor conductive materials 35 and 37. *See* Roy, [0059]-[0060], [0050] ("conductive material 35, 37 may be heavily doped polysilicon"). Roy further teaches that "[s]uch a biasing of conductive materials 35 and 37 provides an accumulation of holes (t_+) along the walls of trench 31/45 and of column 33," and that "[t]his sets area 29 to a reference voltage." Roy, [0060]. As illustrated in Roy's labeled

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figures, the semiconductor in which the holes (t_+) exist is n-type. *See* Roy, Figs. 2-6. POSITAs would have understood that the negative bias Roy teaches is as expected for a p-channel MOSFET and that Roy's structure is analogous thereto. It is common for silicon pMOSFET to have a polysilicon gate (i.e., conductive materials 35 and 37 in Roy) and that for such a pMOSFET the gate is normally doped p+, as this helps reduce threshold voltage shifts, reduces leakage current, and enhances device reliability. Accordingly, it is obvious that Roy is doping the polysilicon layer with a p-type dopant.

It would have further been obvious to use *boron* as the p-type dopant, as boron is one of the most commonly used p-type dopants for silicon-based systems. *See* RX-0219.27-28 (Wolf) (explaining that Column-IV materials (e.g., Si) are commonly doped with Column-III-dopants (e.g., boron)). POSITAs would have understood that using boron as the dopant for silicon-based systems is a known technique that would have yielded predictable results, particularly in light of boron's similar use as a p-type dopant in other similar light trapping devices. *See* RX-0291 (Chen), [0011] ("substrate 35 is a silicon substrate doped with a P-type dopant such as boron, in which case the substrate 35 is a P-type substrate"). Moreover, this claim would have also been obvious because POSITAs would have had a limited number of types of p-type dopants from which to choose.

Q455 Are you aware of Dr. Mansoorian's argument that POSITAs would not understand Roy to be using a p-type dopant?

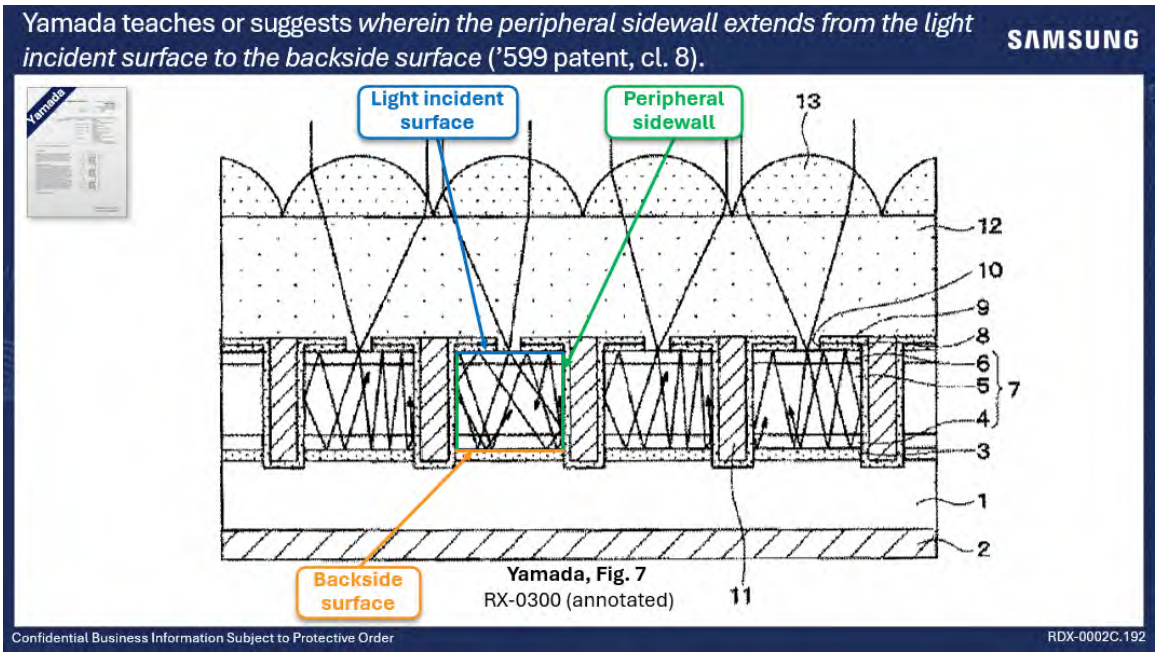
A455 Yes. While Dr. Mansoorian does not make this argument for this combination, Dr. Mansoorian opines elsewhere that Roy does not disclose a p-type dopant because "[o]pposite charges attract" "[s]o[] the accumulation of holes (t_+) does not indicate a p^+ a negative charge in the conductive materials." RX-0911C, ¶534. I disagree. Dr. Mansoorian here is misstating what produces the accumulation of holes in the adjacent silicon sidewall. It is the bias applied to the polysilicon—which, as I explained, POSITAs would understand to act like a MOSFET gate, and would be boron-doped—that forms the hole layer at the silicon sidewall.

c. Claim 8

Q456 Let's turn to claim 8, which is *[t]he device of claim 1, wherein the peripheral sidewall extends from the light incident surface to the backside surface.* Have you formed an opinion regarding this claim?

A456 Yes. Yamada and Roy render this claim obvious. As RDX-0002C.192 illustrates, Yamada's *peripheral sidewall* (trench wall where light receiving section (7) contacts the first insulating film 9 and third reflective film 11) *extends* fully *from the light incident surface to the backside surface*, which allows for the light to be "confined within the PIN photodiode 7." Yamada, [0036]; *see also* Yamada, [0056] ("Each of the embodiments is configured such that the entire side surfaces of the PIN photodiode 7 is covered by the third reflective film 11").

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d. Claim 11

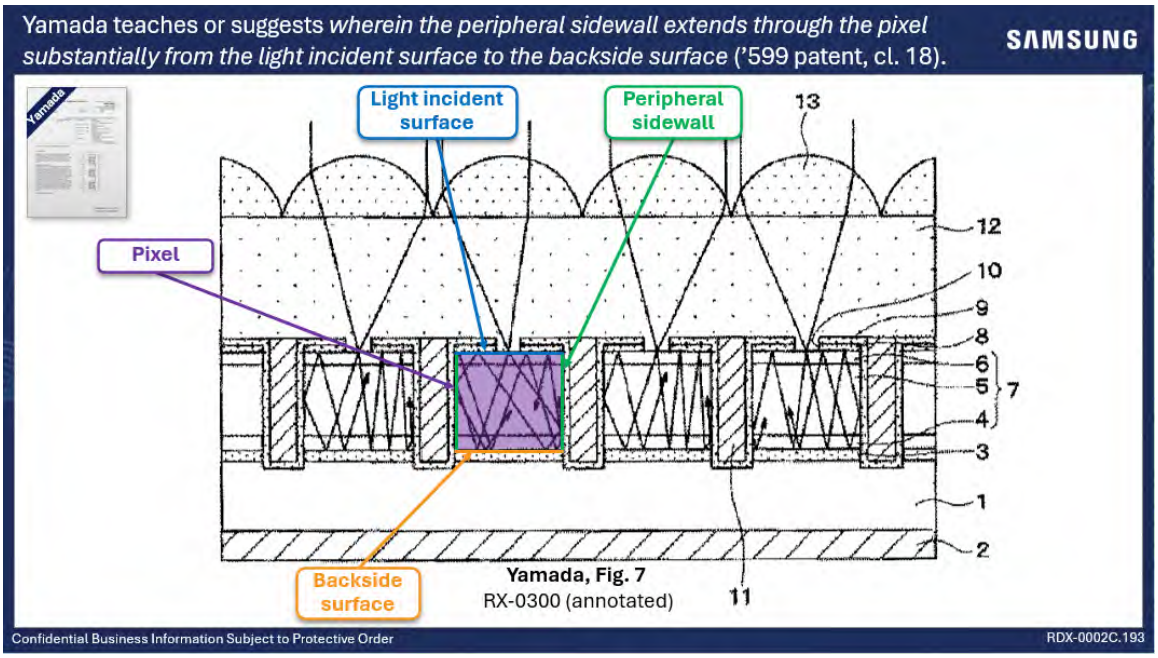
Q457 Let's turn to claim 11, which is *[t]he device of claim 11, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer*. Have you formed an opinion regarding this claim?

A457 Yes. Yamada and Roy render this claim obvious. Yamada explains that its light receiving element may be "configured such that the first reflecting film 3 [(*backside light trapping material*)] is made of a metal such as Al," as illustrated in Figure 6. Yamada, [0048]. POSITAs would have understood that this teaching is equally applicable to Yamada's Figure 7 embodiment. For example, Yamada explains that such a metal film can allow for "the same effect" as Yamada's baseline "first embodiment," which uses the same first reflecting film 3 as Figure 7. Yamada, [0048]; *see also* Yamada, [0048]-[0049] (Yamada's first, fourth, and fifth embodiments are substantially similar).

e. Claim 18

Q458 Let's turn to claim 18, which is *[t]he device of claim 1, wherein the peripheral sidewall extends through the pixel substantially from the light incident surface to the backside surface*. Have you formed an opinion regarding this claim?

A458 Yes. This Yamada and Roy render this claim obvious. As RDX-0002C.193 illustrates, Yamada's *peripheral sidewall* (trench wall where light receiving section (7) contacts the first insulating film 9 and third reflective film 11) *extends through the pixel substantially from the light incident surface to the backside surface*, which allows for the light to be "confined within the PIN photodiode 7." Yamada, [0036]; *see also* Yamada, [0056] ("Each of the embodiments is configured such that the entire side surfaces of the PIN photodiode 7 is covered by the third reflective film 11").



C. Haddad188-based Grounds

Q459 Let's turn to your Haddad188-based opinions. Can you please summarize your anticipation and obviousness opinions about the '599 patent based on Haddad188?

A459 My Haddad188-based opinions are divided into three grounds. Ground 4 is that Haddad188 anticipates, or at least renders obvious, claim 19. Ground 5 is that Haddad188 and Shinohara render obvious claims 19 and 33. Ground 6 is that Haddad188 and Mori render obvious claims 1, 6, 8, 11, 18, and 19.

1. Ground 4: Haddad188 Anticipates, or at Least Renders Obvious, Claim 19

a. Claim 19

1. Limitation 19[a]

Q460 Let's start with your Ground 4 opinions that Haddad188 anticipates, or at least renders obvious, claim 19.

Claim 19's first limitation, 19[a], is *at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending at least partially around the pixel periphery*. Does Haddad188 satisfy this limitation?

A460 Yes. As RDX-0002C.195 illustrates, with differences shown in red, '599 patent, limitation 19[a] is identical to '714 patent, limitation 1[a], except that '599 patent, limitation 19[a] requires that the peripheral sidewall extend *at least partially* around the pixel periphery, whereas '714 patent, limitation 1[a] requires that the peripheral sidewall be *disposed into*

at least a portion of the pixel, and extend *at least substantially* (as opposed to only *partially*) around the pixel periphery.

As discussed for '714 patent (Ground 6), limitation 1[a], Haddad188 teaches or suggests a peripheral sidewall that extends *at least substantially around the pixel periphery*. Accordingly, Haddad188 teaches or suggests the more broad requirement that the peripheral sidewall extends only *at least partially around the pixel periphery* for the same reasons.

2. Limitation 19[b]

Q461 Limitation 19[b] is *a backside light trapping material at least partially covering the backside surface*. Does Haddad188 satisfy this limitation?

A461 Yes. As RDX-0002C.196 illustrates, '599 patent, limitation 19[b] is identical to '714 patent, limitation 1[b]. Haddad188 teaches or suggests '599 patent, limitation 19[b] for the reasons discussed for '714 patent (Ground 6), limitation 1[b].

3. Limitation 19[c]

Q462 Limitation 19[c] is *a peripheral light trapping material substantially covering the peripheral sidewall*. Does Haddad188 satisfy this limitation?

A462 Yes. As RDX-0002C.197 illustrates, '599 patent, limitation 19[c] is identical to '714 patent, limitation 1[c]. Haddad188 teaches or suggests '599 patent, limitation 19[c] for the reasons discussed for '714 patent (Ground 6), limitation 1[c].

4. Limitation 19[d]

Q463 Limitation 19[d] is *a textured region positioned to interact with light incident thereon to increase quantum efficiency of the device*. Does Haddad188 satisfy this limitation?

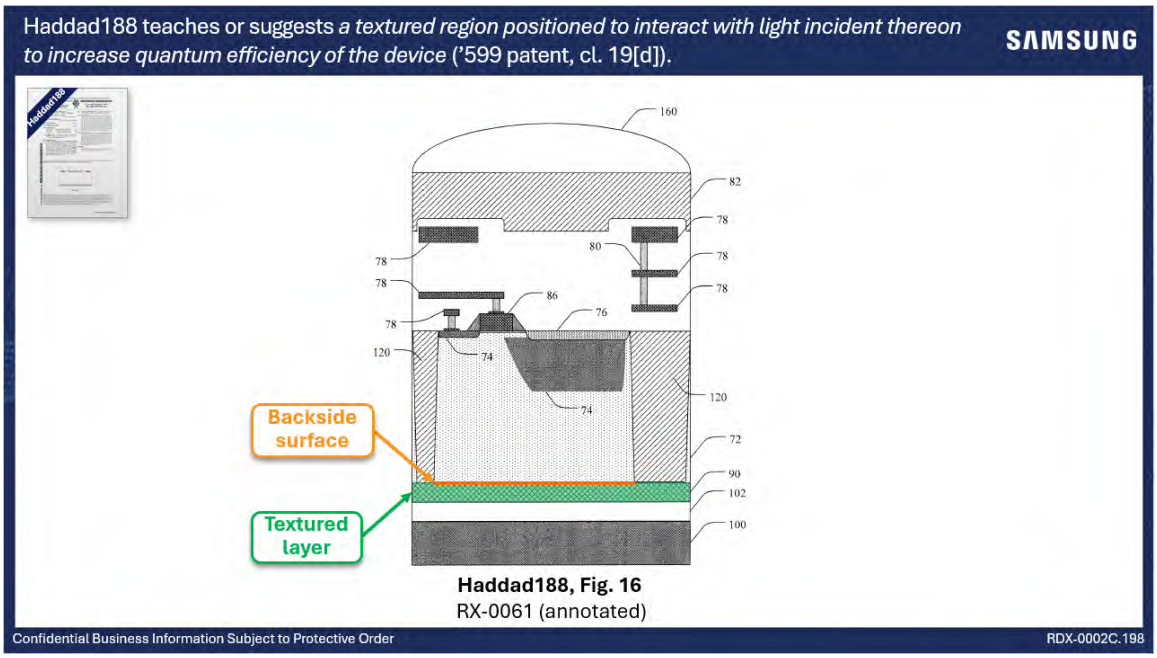
A463 Yes. Haddad188 teaches or suggests *a textured region positioned to interact with light incident thereon to increase quantum efficiency of the device*.

A463 As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *textured region*. Haddad188 teaches or suggests a *textured region*, including under either construction.

Q464 How does Haddad188 teach or suggest this limitation?

A464 As RDX-0002C.198 illustrates, Haddad includes a "textured region 90 and a reflecting layer 102 [that] are coupled to the semiconductor substrate 72 opposite the lens to provide diffusive scattering and reflection of the incident electromagnetic radiation." Haddad188, 25:6-9.

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As Haddad188 teaches elsewhere, "the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device." Haddad188, 14:29-31; *see also* Haddad188, 15:14-19 ("Textured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device…. This increase in absorption length increases the quantum efficiency of the device.").

Accordingly, Haddad188's textured region 90 constitutes a *textured region positioned to interact with light incident thereon to increase quantum efficiency of the device*, as it reflects, diffuses, redirects, or absorbs electromagnetic radiation, thus increasing the quantum efficiency of the device.

Q465 How does textured region 90 constitute a *textured region* under the parties' proposed construction?

A465 Textured region 90 constitutes a *textured region* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

5. Limitation 19[e]

Q466 Limitation 19[e] is *a reflective layer coupled to the light incident side and having an aperture to allow entry of light into the pixel*. Does Haddad188 satisfy this limitation?

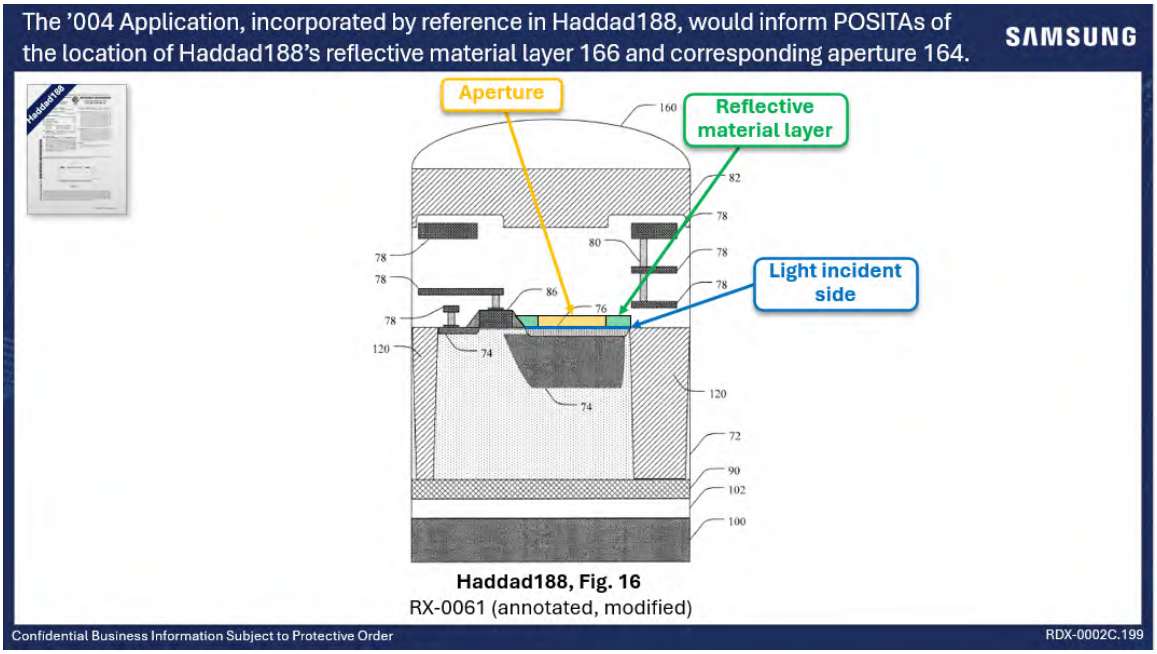
A466 Yes. Haddad188 teaches or suggests *a reflective layer coupled to the light incident side and having an aperture to allow entry of light into the pixel*.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *reflective layer*. Haddad188 teaches or suggests a *reflective layer coupled to the light incident side* under either construction.

Q467 How does Haddad188 satisfy this limitation?

A467 As explained for '714 patent (Ground 6), claim 12 Haddad188 discloses "a metal or other reflective material 166," Haddad188, 25:9-10, having an aperture to allow entry of light into the pixel. See Haddad188, 25:9-11 ("aperture 164 formed in a metal or other reflective material layer 166" "lens focuses electromagnetic radiation through the aperture"). While Haddad188 does not depict reflective material layer 166 in its figures, it is discussed in the specification's text, and Haddad188 "incorporate[s] herein by reference" the '004 Application, Haddad188, 1:4-8, which depicts the reflective material layer in its figures.

As explained for '714 patent (Ground 6), claim 12—due to similarities between the '004 Application's figures and text and Haddad188's—POSITAs would understand that Haddad188's reflective material layer 166, and corresponding aperture 164, would be similarly located in Haddad188's Figure 16, as RDX-0002C.199 illustrates.



Q468 Does reflective material layer 166 satisfy this limitation?

A468 Yes. As RDX-0002C.199 illustrates, Hadddad188 discloses a *reflective layer* (reflective material layer 166) *coupled to the light incident side* (top surface of semiconductor substrate 72), *and having an aperture* (aperture 164) *to allow entry of light into the pixel*.

Reflective material layer 166 constitutes a *reflective layer*, as Haddad188 discloses that it "can increase the effectiveness of the optical cavity," Haddad188, 25:10-11, which POSITAs would understand to mean reflecting light from inside the pixel back into the pixel.

Moreover, POSITAs would understand that a reflective layer, as described by Haddad188 would reflect light back into the pixel due to its placement covering part of the pixel's light incident side, as RDX-0002C.199 illustrates.

Q469 How does reflective material layer 166 constitute a *reflective layer* under the parties' proposed constructions?

A469 Reflecting material layer 166 constitutes a *reflective layer* under either party's proposed construction, as it is a layer that reflects and will reflect more light back into the pixel than it transmits for the reasons just explained.

6. Limitation 19[f]

Q470 Limitation 19[f] is *wherein the reflective layer is operable to reflect at least a portion of light impinging thereupon from inside the pixel back into the pixel back into the pixel.* Does Haddad188 satisfy this limitation?

A470 Yes. I understand that the ALJ has amended the term *thereupon from inside the pixel back into the pixel back into the pixel*s such that it is now *thereupon from inside the pixel back into the pixel*. Order No. 36 at 40.

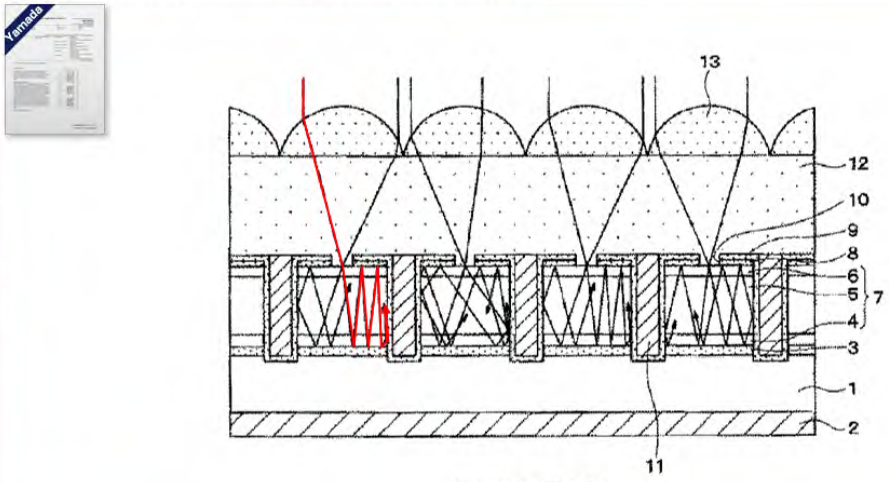
Haddad188's *reflective layer* (reflective material layer 166) *is operable to reflect at least a portion of light impinging thereupon from inside the pixel back into the pixel*. As discussed for '599 patent (Ground 4), limitations 19[b]-[c], and [e], Haddad188 includes both a backside reflecting layer 102, a frontside reflective material layer 166, and a peripheral reflecting layer (trench isolation 120). As Haddad188 teaches, the purpose of its reflective layers is "to maintain the electromagnetic radiation in the semiconductor substrate," by "reflect[ing] incident light until it is absorbed." *See* Haddad188, 2:29-31, 20:19-25, 22:22-29.

POSITAs would have understood that Haddad188, containing reflective peripheral, backside, and frontside surfaces is operable to reflect at least a portion of light off reflective material layer 166, i.e., to reflect light *from inside the pixel back into the pixel*. For example, as RDX-0002C.200 illustrates, Yamada depicts a light ray being reflected by the first reflective film 3, the second reflective film 8, and the third reflective film 11.

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Yamada depicts a light ray being reflected by the first reflective film 3, the second reflective film 8, and the third reflective film 11.

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Yamada, Fig. 7
RX-0300 (annotated)

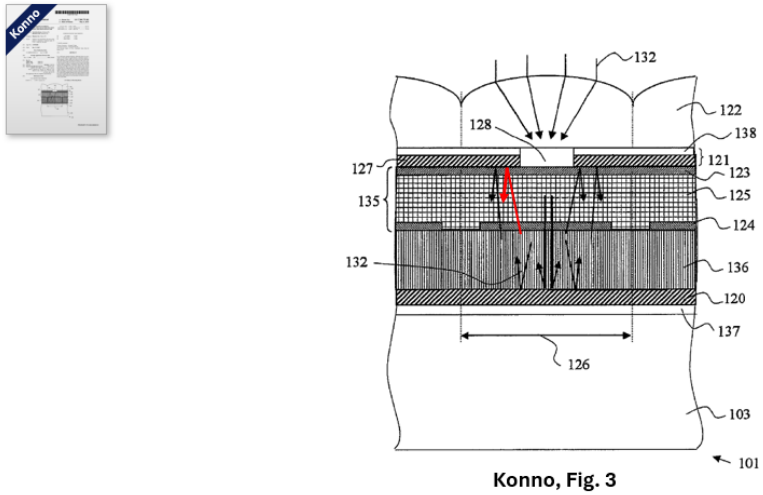
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RDX-0002C.200

Likewise, as RDX-0002C.201 illustrates, Konno depicts a light ray being reflected off the first reflective layer 121 *from inside the pixel back into the pixel*.

Konno illustrates light being reflected off first reflective layer 121 *from inside the pixel back into the pixel*.

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Konno, Fig. 3
RX-0288 (annotated)

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RDX-0002C.201

2. Ground 5: Haddad188 and Shinohara Render Obvious Claims 19 and 33

Q471 Let's turn to your Ground 5 opinions. Can you please summarize your Ground 5 opinions?

A471 In my opinion Haddad188 and Shinohara render obvious claims 19 and 33. As explained for Ground 4, Haddad188 anticipates, or at least renders obvious, claim 19. Those opinions are equally applicable to my Ground 5 opinions regarding Haddad188 and Shinohara, which further render obvious claim 33.

a. Claim 33

Q472 Let's turn to claim 33, which is *[t]he device of claim 19, wherein the peripheral light trapping material comprises any of aluminum oxide and hafnium oxide*. Have you formed an opinion regarding this claim?

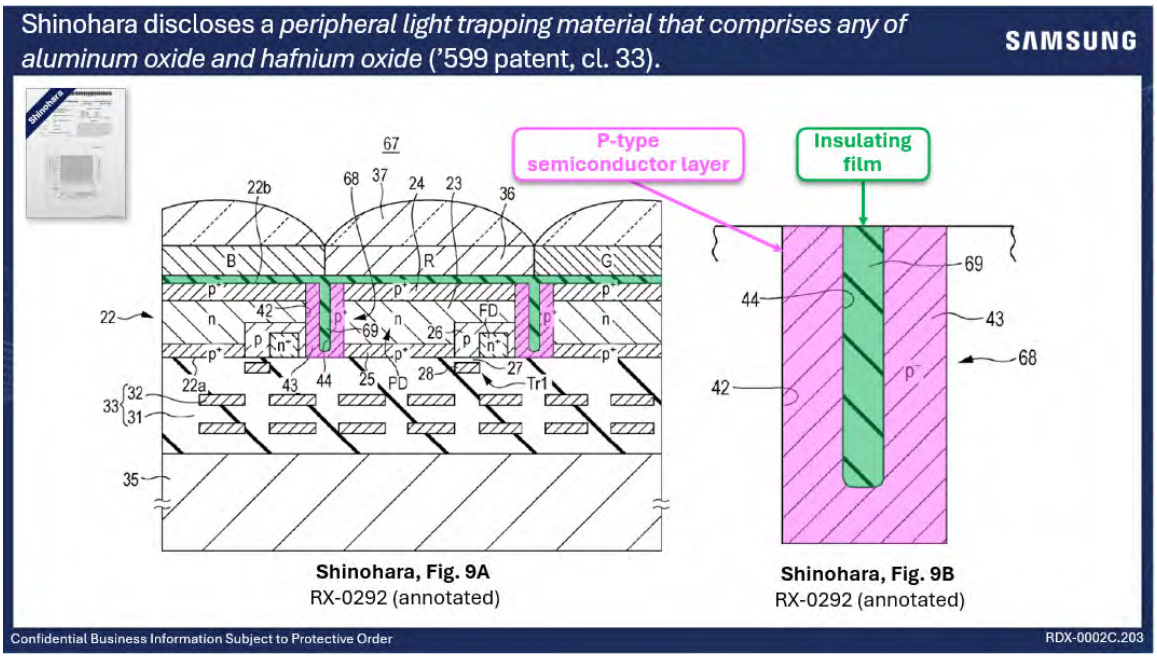
A472 Yes. Haddad188 teaches or suggests this limitation. Dr. Mansoorian has not disputed this.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *light trapping material*. Haddad188 and Shinohara render claim 33 obvious, including under either party's proposed construction.

Q473 How would Haddad18 and Shinohara render claim 33 obvious?

A473 As RDX-0002C.203 illustrates, Shinohara discloses a *peripheral light trapping material that comprises any of aluminum oxide and hafnium oxide*. Specifically, Shinohara discloses "an element region 68 for isolating pixels," Shinohara, [0091], which is formed with "insulating film 69" formed within "void 44" in "p-type semiconductor layer 43." Shinohara, [0043].

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Q474 What material is insulating film 69 formed of?

A474 Shinohara teaches that it is beneficial to form "insulating film 69" out of a material having a negative fixed charge. Specifically, Shinohara teaches that "[w]hen the insulating film having a negative fixed charge is used as the insulating film 69, the hole pinning state by the p-type semiconductor layer 43 of the element isolation region 68 can be enhanced." Shinohara, [0095]. Shinohara further explains that "the generation of … dark current can be further suppressed." Shinohara, [0095].

Shinohara describes examples of negative fixed charge materials, including "hafnium dioxide (HfO_2)" or "dialuminum trioxide (Al_2O_3)." Shinohara, [0091]. POSITAs would recognize that the claimed *hafnium oxide* encompasses Shinohara's "hafnium dioxide," as *hafnium oxide* is commonly used to refer to hafnium dioxide. *See* RX-0579C.17-18 (SiOnyx Infringement Contentions, Appx. 2) (using hafnium oxide and hafnium dioxide interchangeably). Likewise, POSITAs would understand that the claimed *aluminum oxide* encompasses Shinohara's dialuminum trioxide. For example, the '599 patent uses the terms "aluminum oxide" and "Al_2O_3" interchangeably. *See* '599 patent, 9:53-59.

Q475 Why would POSITAs use Shinohara's isolation region in Haddad188?

A475 POSITAs would have been motivated to use Shinohara's isolation region 68—which Shinohara teaches can be either *hafnium oxide* or *aluminum oxide*—in place of Haddad188's trench isolation 120 to reduce dark current. POSITAs would have reasonably expected success in making this modification. For example, Haddad188 explains that "trench isolation [120] can include various materials, including, without limitation, dielectric materials, reflective materials, conductive materials, light diffusing features, and the like." Haddad188, 22:25-29; *see also* Haddad188, 25:21-22 (acknowledging the use of passivation layers to help reduce dark current). Additionally, Shinohara's isolation region

68 serves the same purpose as Haddad188's trench isolation 120, e.g., Shinohara explains that "inclined incident light is reflected at the interface between the silicon and the insulating film [of the isolation region 68] and does not leak outside from the pixel, and hence no color mixture occurs." Shinohara, [0094]. Moreover, *aluminum oxide* was used as a reflective material in similar reflectors. *See* Suzunaga, [0067] ("film having a high refractive index is not necessarily limited to a semiconductor material, but may be for example, any one of … Al_2O_3 … and the like as depicted in Table 1").

Q476 Would this modification satisfy '599 patent, claim 19's requirement of a *peripheral light trapping material*?

A476 Yes. This modification still satisfy claim '599 patent, 19[c]'s requirement of a *peripheral light trapping material*, including under either party's proposed construction. Shinohara teaches that:

> When the insulating film having a negative fixed charge is used, one type of film or a laminate containing a plurality of types of films may be used. For example, a laminate containing two types of films [e.g., a distributed Bragg reflector] may be used as the insulating film having a negative fixed charge.

Shinohara, [0091]. That is, Shinohara teaches that "inclined incident light is reflected at the interface between the silicon and the insulating film and does not leak outside from the pixel, and hence no color mixture occurs." Shinohara, [0094].

Q477 How does the reflector added to Haddad188 as part of this combination constitute a *light trapping material* under the parties' proposed constructions?

A477 The reflector added to Haddad188 as part of this combination constitutes a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

3. Ground 6: Haddad188 and Mori Render Obvious Claims 1, 6, 8, 11, and 18-19

Q478 Let's turn to your Ground 6 opinions. Can you please summarize your Ground 6 opinions?

A478 In my opinion Haddad188 and Mori render obvious claims 1, 6, 8, 11, and 18-19. As explained for Ground 4, Haddad188 anticipates, or at least renders obvious, claim 19. Those opinions are equally applicable to my Ground 6 opinions regarding Haddad188 and Mori, which further render obvious claims 1, 6, 8, 11, and 18.

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a. Claim 1

Q479 Let's turn to claim 1. Have you formed an opinion regarding claim 1?

A479 Yes. Haddad188 and Mori render obvious claim 1. As RDX-0002C.205 illustrates, limitations 1[a]-[b] and 1[d]-[e] are identical to limitations 19[a]-[b] and 19[e]-[f]. Haddad188 teaches or suggests these limitations for the reasons discussed for '599 patent (Ground 4), claim 19. The only limitation not identical to claim 19 is limitation 1[c].

1. Limitation 1[c]

Q480 Limitation 1[c] is *a peripheral light trapping material substantially covering the peripheral sidewall, wherein said peripheral light trapping material is doped with a dopant to create a surface field*. Have you formed an opinion regarding this limitation?

A480 Yes. As part of his infringement opinions, Dr. Foty has opined that this limitation is met so long as at least part of the *peripheral light trapping material is doped*. RX-0905C, ¶¶1089-1095. This limitation is satisfied by Haddad188 and Mori under such an interpretation.

As RDX-0002C.206 illustrates, with differences shown in red, '599 patent, limitation 1[c] is identical to '714 patent, limitation 1[c], except that '599 patent, limitation 1[c] additionally requires that the *peripheral light trapping material is doped with a dopant to create a surface field*.

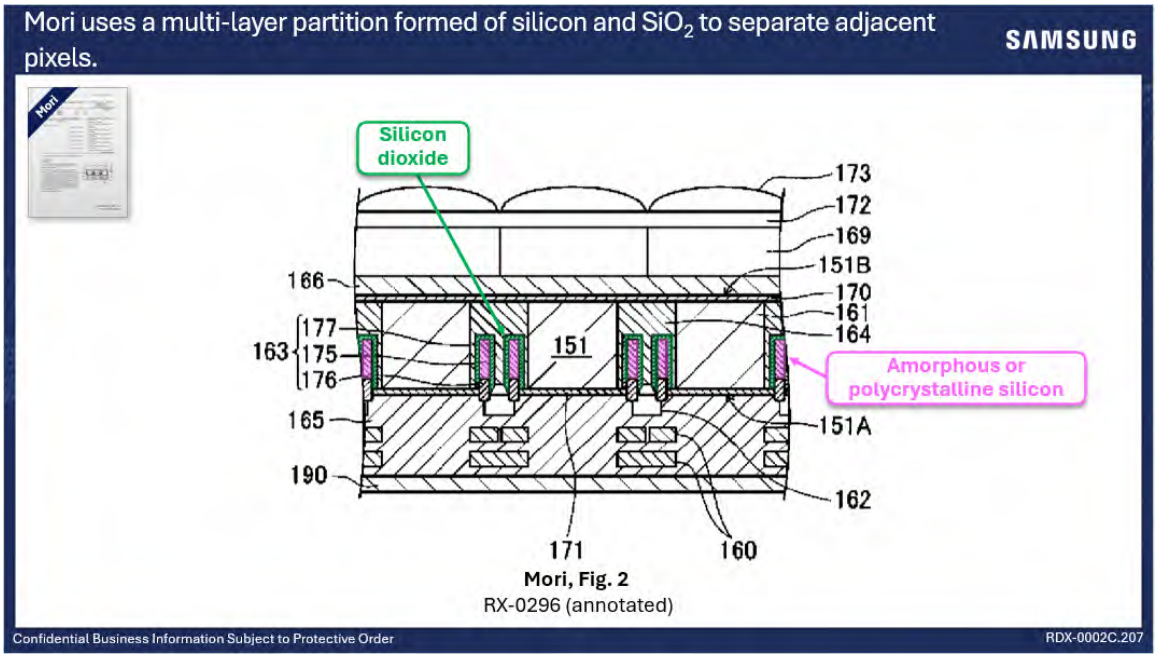
As discussed for '714 patent (Ground 6), limitation 1[c], Haddad188 teaches or suggests *a peripheral light trapping material substantially covering the peripheral sidewall*. Haddad188 and Mori further render obvious a *peripheral light trapping material* that *is doped with a dopant to create a surface field*.

Q481 How does Haddad188 and Mori render obvious a *peripheral light trapping material* that is *doped with a dopant to create a surface field*?

A481 As explained for '714 patent (Ground 6), limitation 1[e], Haddad188 is broad in its disclosure of what its trench isolation can be made of: "[t]rench isolation can include dielectric materials, reflective materials, conductive materials, and combinations thereof, including textured regions and other light diffusing features." Haddad188, 24:5-7. Haddad188 further teaches that "[t]hese trench isolation regions can be configured to reflect incident light until it is absorbed, thereby increas[ing] the effective absorption length of the device." Haddad188, 22:27-30.

As RDX-0002C.207 illustrates, Mori discloses a "partition part 163" separating its pixels and, like Haddad188, serving to reduce "color mixing [or 'crosstalk'] due to obliquely incident light." Mori, [0027]. Mori teaches that its partition part 163 has a silicon layer 175 "made of amorphous silicon or polycrystalline silicon," Mori, [0011], and a "silicon oxide film [177] formed between the silicon layer and the semiconductor substrate," Mori, [0013]. Mori explains that "[w]ith this configuration, crystal defects on the side surface of

the groove for forming the partition part can be reduced, and the charges generated when dark can be reduced in order to achieve high sensitivity." Mori, [0013], [0029]-[0030].



See also Mori, Fig. 6 (illustrating partition part 163 spanning along the entire side surface of photoelectric conversion unit 161), [0043].

Q482 Why would POSITAs use a Si/SiO_2 partition, like Mori describes, in Haddad188?

A482 Using a Si/SiO_2 isolation element, like Mori discloses, in Haddad188 to obtain the benefits Mori describes—i.e., reduced dark current and high sensitivity—would have been obvious. Moreover, POSITAs would have reasonably expected success in doing so with predictable results.

Q483 Why would POSITAs have reasonably expected success in making this combination?

A483 It was well-known that layers of silicon and SiO_2 could be used as reflectors. *See* Schubert, 163, 173 (explaining that Si/SiO_2 DBRs "yield high reflectivity"), 177 (explaining that Si and SiO_2 are "natural candidates" for omnidirectional reflectors). Indeed, Si/SiO_2 reflectors were commonly used as peripheral light trapping materials in similar sensors. *See* Hwang, 9:25-30, 10:2-5; Suzunaga, [0035] ("process of laminating a SiO_2 film and a polysilicon film has a proven track record in the manufacture of semiconductor integrated circuits, and a major advantage of this process is thought to be that there are no processing problems"). POSITAs would further understand that an isolation element's reflectivity could be increased by increasing the number of alternating layers of silicon and SiO_2 alternated in the isolation element and/or increasing the layer's thickness. *See* Schubert, 170 ("DBR's reflectivity can be increased by increasing the number of reflector pairs"); Suzunaga, [0028] (by "optimizing the thickness of the SiO_2 film 14 and the polysilicon film 15 for the wavelength of the incident light … almost 100% of the incident light passing through the element layer 2 can be reflected by the multi-reflection film 16"), [0032] ("reflectance of

90% or more can be obtained by optimizing the thickness of the layers, including a total of five layers including three SiO_2 layers and two polysilicon layers").

Accordingly, using a Si/SiO_2 DBR would have been nothing more than a simple substitution of a metal layer to obtain predictable results (e.g., high reflectivity, reduced dark current, and omnidirectional characteristics). As Schubert teaches, such Si/SiO_2 DBRs "yield high reflectivity," Schubert, 172, including up to 100% reflectance, Schubert, 170. *See also* Suzunaga, [0028].

Q484 Would this modification satisfy '599 patent, claim 1's requirement of a *peripheral light trapping material*?

A484 Yes. Haddad188, as modified by Mori, would include a *peripheral light trapping material*, including under either party's proposed construction, for the reasons just explained. Additionally, as explained for '714 patent (Ground 6), limitation 1[c], the peripheral light trapping material would also *substantially cover[] the peripheral sidewall*.

Q485 How does Haddad188 as modified by Mori include a *light trapping material* under the parties' proposed constructions?

A485 Haddad188 as modified by Mori includes a *light trapping material* under the parties' proposed constructions, as it directs light back into the pixel and reflects more light back into the pixel than it transmits for the reasons just explained.

Q486 Limitation 1[c]'s second element is *wherein said peripheral light trapping material is doped with a dopant to create a surface field*. Have you formed an opinion regarding this element?

A486 Yes. Doping the peripheral light trapping material with a dopant to create a surface field would have been obvious. Mori teaches that it is beneficial when using such a Si/SiO_2 partition to dope the SiO_2 layer (Mori's SiO_2 layer 177) with impurities, as explained in the overview of Mori. *See* Mori, [0036]. As Mori teaches, this doping is advantageous in mitigating dark current stemming from crystal defects, i.e., to "prevent charges generated when dark due to crystal defects on the partition groove 174 from flowing into the photoelectric conversion unit 161." Mori, [0036]. *See also* JX-0027C (McKee), 93:2-13 (explaining that doping is often used to reduce dark current); JX-0017C (Sickler), 42:1-10 (explaining that doping is often used to reduce dark current).

Q487 Has the term *doped with a dopant to create a surface field* been construed?

A487 No, and I also understand that the parties have not proposed constructions for this term. Accordingly, I understand I should apply the term's plain meaning.

Q488 Does the '599 patent explain how doping the peripheral light trapping material creates a surface field?

A488 No. The '599 patent does not explain how doping the peripheral light trapping material creates a surface field. Instead, the '599 patent only states that:

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> [I]t can also be beneficial to dope the sidewalls to create a surface field that will improve electrical isolation between the pixels. In one aspect, it can also be beneficial to dope the low refractive index material of the Bragg-type reflectors to increase such electrical isolation.

'599 patent, 10:14-18. The '599 patent states that merely doping—e.g., the manner Mori describes—serves to increase electrical isolation between pixels via a surface field. Accordingly, Mori's doped SiO_2 film located along the side of its pixel (photoelectric conversion unit 161) constitutes a peripheral light trapping material that *is doped with a dopant to create a surface field* as contemplated by the '599 patent's limited disclosure.

Q489 Would POSITAs be motivated to similarly dope Haddad188 based on Mori's teachings?

A489 Yes. POSITAs would have been motivated to similarly dope the SiO_2 layer of the Si/SiO_2 reflector that replaces Haddad188's trench isolation 120. POSITAs would recognize that doping the SiO2 layer with impurities would similarly mitigate against dark current stemming from crystal defects in Haddad188's pixel, which would improve Haddad188. *See* JX-0017C (Sickler), 41:7-8 (explaining that dark current is harmful should be minimized).

Q490 Are you aware of Dr. Mansoorian's argument that Mori does not dope the side SiO_2 film 177?

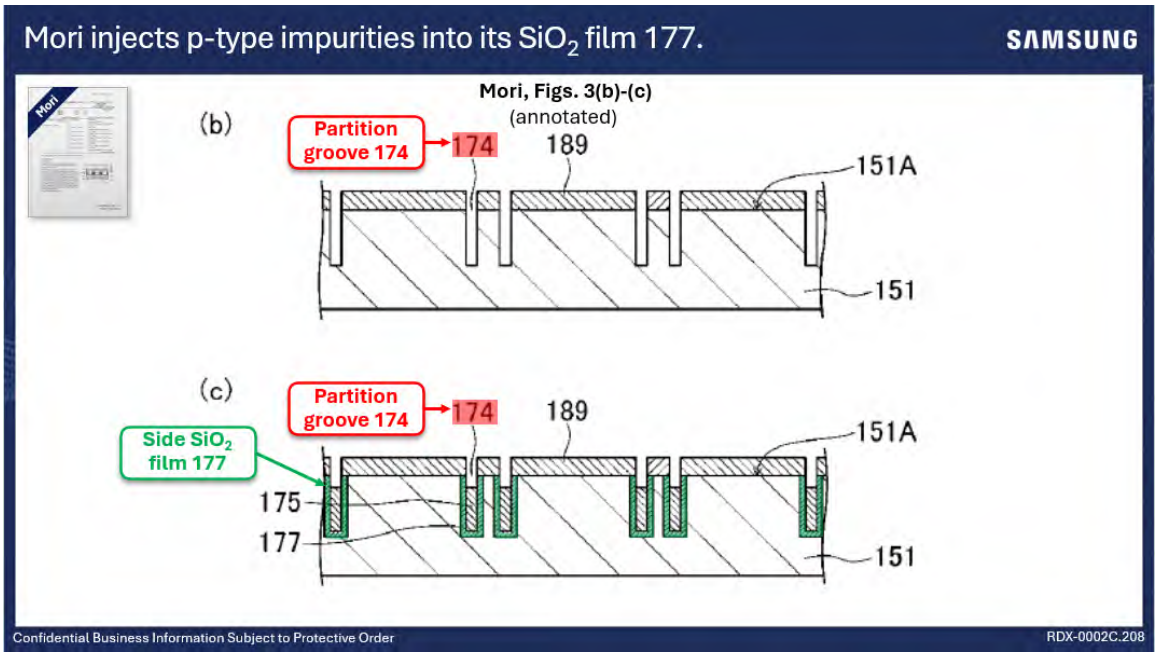
A490 Yes. Dr. Mansoorian opines that "Mori does not teach a 'doped SiO_2 film located along the side of its pixel.'" RX-0911C, ¶604 (quoting Mori, [0036]). I disagree and note this is not a theory presented in SiOnyx's contentions. RX-0606C.281. Reviewing the paragraph quoted by Dr. Mansoorian shows Mori is doping SiO_2 film 177:

> In order to prevent charges generated when dark due to crystal defects on the partition groove 174 from flowing into the photoelectric conversion unit 161, p-type impurities are injected into the side walls of the partition groove 174 <u>after forming the side SiO_2 film 177</u>.

Mori, [0036]. That is, Mori injects p-type impurities into partition groove 174's sidewall <u>after</u> lining the sidewall with SiO_2 film 177. As RDX-0002C.208 illustrates, once deposited side SiO_2 film 177 completely covers partition groove 174's sidewalls, such that POSITAs would understand that to inject p-type impurities into groove 174's sidewalls would require injecting p-type impurities into SiO_2 film 177.[11]

[11] While Mori's Figure 3 does not depict an image after side SiO_2 film 177 is deposited but before silicon layer 175 is deposited, POSITAs would expect that p-type impurities are injected into partition groove 174's sidewalls before silicon 175 is deposited, as it would be difficult to inject p-type impurities through silicon 175—which fills partition groove 174—and into partition groove 174's sidewalls.

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Accordingly, because Mori teaches that "p-type impurities are injected … after forming the side SiO_2 film 177," POSITAs would understand that p-type impurities must be injected into side SiO_2 film 177.

Q491 Are you aware of Dr. Mansoorian's argument that all of the p-type impurities would pass through SiO_2 film 177?

A491 Yes. While he does not argue it for this combination, apparently conceding that Mori injects p-type impurities into side SiO_2 film 177 in order to dope partition groove 174's sidewalls, Dr. Mansoorian opines elsewhere that "[a]t the lowest injection energy of 5keV, the p-type impurities would penetrate about 20-30nm through SiO_2, meaning all the way through Mori's SiO_2 film and into the side walls of the partition groove." RX-0911C, ¶513. I disagree and note this is not a theory presented in SiOnyx's contentions. RX-0606C.281.

Mori explains p-type impurities are injected using ion implementation, that the SiO_2 film 177 has "a thickness of 5 nm to 20 nm," and that the p-type impurity is injected with "an injection energy of 5 to 30 keV." Mori, [0036]. In ion implantation of silicon-based systems, the most commonly used p-type dopant is boron. The implant range—i.e., the distance into the target material at which most implanted dopants stop—of boron in silicon or SiO_2 is similar, and boron implanted at normal (perpendicular) incidence has a range of approximately 20nm at 5keV. Accordingly, POSITAs would understand that approximately half of the boron would remain in Mori's SiO_2 film 177—while the other half would be implanted into the underlying silicon—when selecting a SiO_2 thickness of 20nm and an injection energy of 5keV. Moreover, for an angled implant (i.e., an implant at a shallower anger than normal (perpendicular) incidence), as would likely be required in Mori, the penetration's depth becomes shallower resulting in more boron remaining in the SiO_2 film 177.

Q492 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination as Haddad188 allegedly does not need improvement?

A492 Yes. Dr. Mansoorian opines, without explanation, that "a POSITA would not have been motivated to combine the teachings of Mori to the device of Haddad188 because doing so would be unnecessary and redundant," and that "[d]oping the peripheral isolation element of Haddad188 would merely add complexity without adding any meaningful benefit." RX-0911C, ¶605. I disagree and note this is not a theory presented in SiOnyx's contentions. RX-0606C.368-369. As discussed earlier, POSITAs would recognize that Mori's teachings could be incorporated into Haddad188 to minimize dark current.

b. Claim 6

Q493 Let's turn to claim 6, which is *[t]he device of claim 1, wherein the dopant is boron or antimony*. Have you formed an opinion regarding this claim?

A493 Yes. Haddad188 and Mori render this claim obvious. As explained for '599 patent, limitation 1[c], it would have been obvious in view of Mori to inject p-type impurities into and through the peripheral light trapping material (i.e., SiO_2) and into the silicon layer—i.e., Mori teaches using a p-type dopant in the silicon layer.

Using *boron* as the dopant would have been further obvious, as boron is one of the most commonly used p-type dopants for silicon-based systems. *See* RX-0219.27-28 (Wolf) (explaining that Column-IV materials (e.g., silicon) are commonly doped with Column-III-dopants (e.g., boron)). POSITAs would have understood that using boron as the p-type dopant for silicon-based systems is a known technique that would have yield predictable results, particularly in light of boron's similar use as a p-type dopant in other similar light trapping devices. *See* RX-0291(Chen), [0011] ("substrate 35 is a silicon substrate doped with a P-type dopant such as boron, in which case the substrate 35 is a P-type substrate"). Moreover, this claim would have also been obvious because POSITAs would have had a limited number of types of p-type dopants from which to choose.

Q494 Are there any other reasons why using *boron* as the dopant would have been obvious?

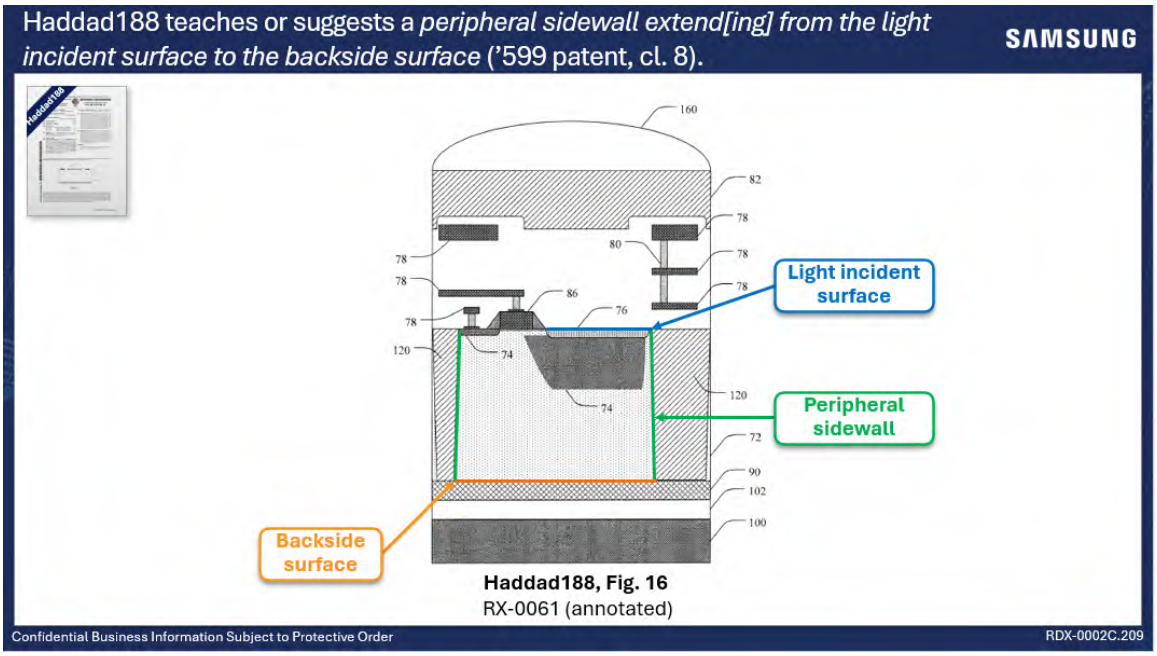
A494 Yes. Haddad188 itself discloses using boron as a dopant. Haddad188, 18:5-7 ("non-limiting examples of dopant materials can include S, F, B, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof").

c. Claim 8

Q495 Let's turn to claim 8, which is *[t]he device of claim 1, wherein the peripheral sidewall extends from the light incident surface to the backside surface*. Have you formed an opinion regarding this claim?

A495 Yes. Haddad188 and Mori render this claim obvious. As RDX-0002C.209 illustrates, Haddad188's *peripheral sidewall* (trench wall where semiconductor substrate 72 meets trench isolation 120) *extends from the light incident surface to the backside surface*.

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d. Claim 11

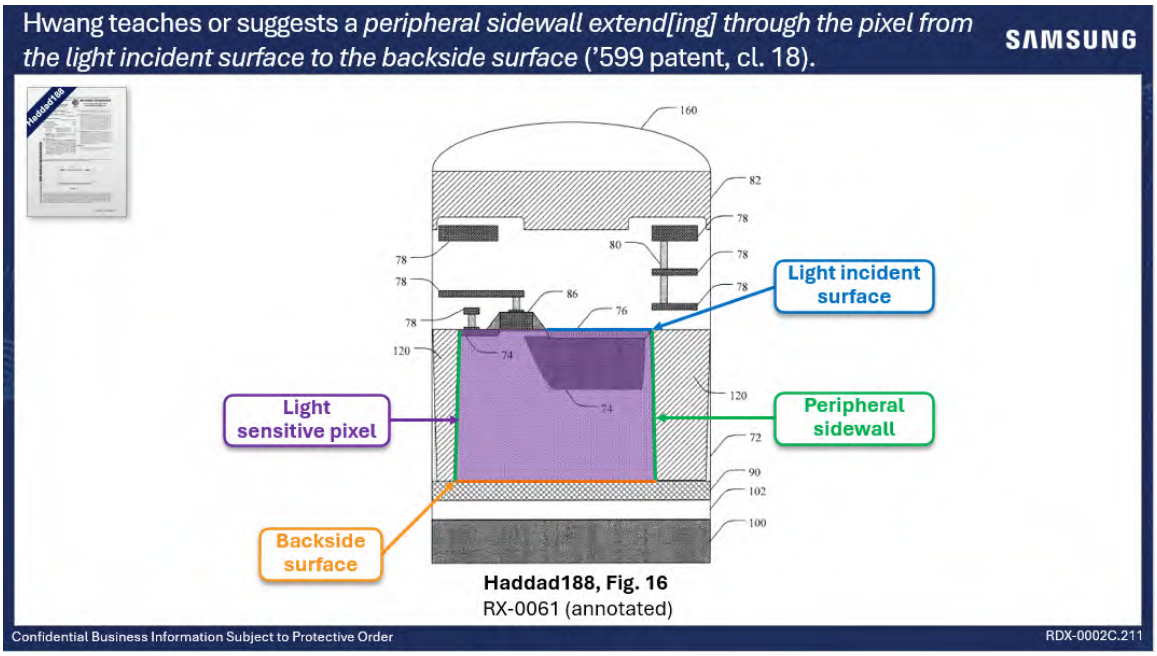
Q496 Let's turn to claim 11, which is *[t]he device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer*. Have you formed an opinion regarding this claim?

A496 Yes. As RDX-0002C.210 illustrates, '599 patent, claim 11's additional limitations are identical to '714 patent, claim 17's additional limitations. Haddad188 teaches or suggests '599 patent, claim 11's additional limitations for the reasons discussed for '714 patent (Ground 6), claim 17. Specifically, Haddad188's reflecting layer 102 (*backside light trapping material*) "can be any reflective material that can be incorporated into such a device," "includ[ing] … silver, aluminum, and the like," Haddad188, 23:15-26, i.e., a *metal layer*.

e. Claim 18

Q497 Let's turn to claim 18, which is *[t]he device of claim 1, wherein the peripheral sidewall extends through the pixel substantially from the light incident surface to the backside surface*. Have you formed an opinion regarding this claim?

A497 Yes. Haddad188 and Roy render this claim obvious. As RDX-0002C.211 illustrates, Haddad188's *peripheral sidewall* (trench wall where semiconductor substrate 72 meets trench isolation 120) *extends through the pixel substantially from the light incident surface to the backside surface*.



D. Suzunaga-based Grounds

Q498 Let's turn to your Suzunaga-based opinions. Can you please summarize your anticipation and obviousness opinions for the '599 patent based on Suzunaga?

A498 My Suzunaga-based opinions are based on a single ground, Ground 7, which is that Suzunaga and Konno render obvious claims 19 and 33.

1. Ground 7: Suzunaga and Konno Render Obvious Claims 19 and 33

a. Claim 19

1. Limitation 19[a]

Q499 Claim 19's first limitation, 19[a], is *at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending at least partially around the pixel periphery*. Does Suzunaga satisfy this limitation?

A499 Yes. As RDX-0002C.213 illustrates, with differences shown in red, '599 patent, limitation 19[a] is identical to '714 patent, limitation 1[a], except that '599 patent, limitation 19[a] requires that the peripheral sidewall extend *at least partially* around the pixel periphery, whereas '714 patent, limitation 1[a] requires that the peripheral sidewall be *disposed into at least a portion of the pixel*, and extend *at least substantially* (as opposed to only *partially*) around the pixel periphery.

As discussed for '714 patent (Ground 7), limitation 1[a], Suzunaga teaches or suggests a peripheral sidewall that extends *at least substantially around the pixel periphery*.

Accordingly, Suzunaga teaches or suggests the more broad requirement that the peripheral sidewall extends only *at least partially around the pixel periphery* for the same reasons.

2. Limitations 19[b], [d]

Q500 Let's take limitations 19[b] and 19[d] together. 19[b] is *a backside light trapping material at least partially covering the backside surface*. 19[d] is *a textured region positioned to interact with light incident thereon to increase quantum efficiency of the device*. Have you formed an opinion regarding these limitations?

A500 Yes. Suzunaga and Konno render these limitations obvious.

As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *light trapping material* and *textured region*. Suzunaga and Konno render obvious a *backside light trapping material* and a *textured region*, including under either construction.

Q501 Let's start with 19[b], *a backside light trapping material at least partially covering the backside surface*. How do Suzunaga and Konno render this limitation obvious?

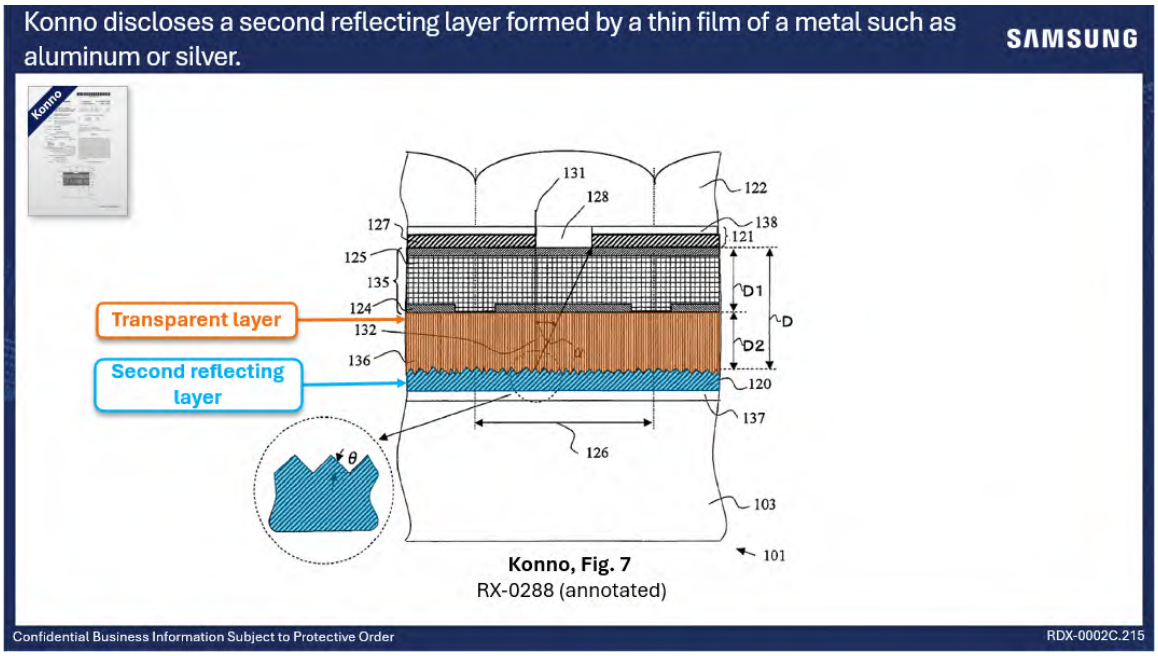
A501 As RDX-0002C.214 illustrates, '599 patent, limitation 19[b] is identical to '714 patent, limitation 1[b]. Suzunaga teaches or suggests '599 patent, limitation 19[b] for the reasons discussed for '714 patent (Ground 1), limitation 1[b]. Specifically, Suzunaga's multi-reflection film 16 constitutes *a backside light trapping material at least partially covering the backside surface*.

Additionally, POSITAs would be motivated to replace Suzunaga's multi-reflection film16 with Konno's transparent layer 136 and second reflecting layer 120 to similarly cover Suzunaga's *backside surface*. Konno's transparent layer 136 and second reflecting layer 120, as used in Suzunaga, constitute a *backside light trapping material at least partially covering the backside surface* and *a textured region positioned to interact with light incident thereon to increase quantum efficiency of the device*.

Q502 Does Konno disclose *a backside light trapping material*?

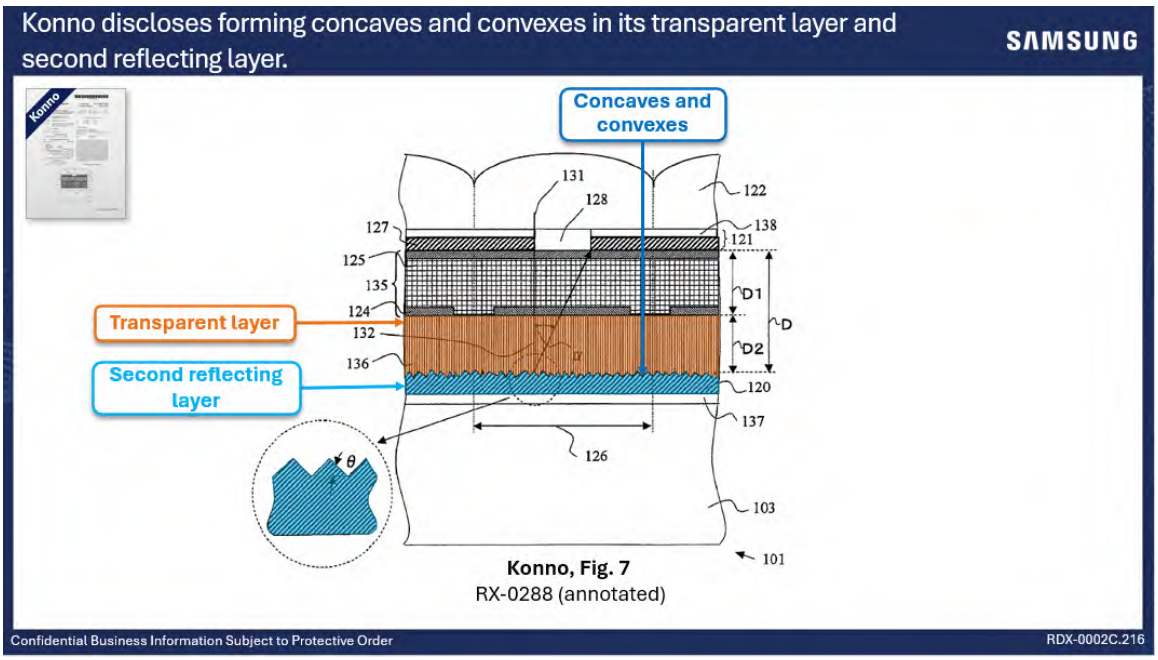
A502 Yes. Konno's second reflecting layer 120 constitutes *a backside light trapping material*. As RDX-0002C.215 illustrates, Konno includes a second reflecting layer 120 "formed by forming a thin film of a metal such as aluminum or silver." Konno, 8:31-38. Such metal reflectors constitute a *light trapping material* that reflect light back into the pixel, as a solid metal film, as Konno discloses, reflects more light than it transmits, and is positioned to reflect light back into the pixel. *See* Schubert, Table 10.2 (listing reflectivity of metal-air and metal-semiconductor reflectors at 0.5μm and 1.0μm, all of which have 50% or greater reflectivity); Yamada, [0038] ("since the sides of the PIN photodiode 7 are covered with the third reflective films 11, no incident light escapes from the sides of the PIN photodiode 7 and no optical crosstalk occurs between neighboring PIN photodiodes 7"), [0012] ("third reflective film (11) can be composed of a metal [such as aluminum]").

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Q503 Does Konno disclose *a textured region*?

A503 Yes. Konno's transparent layer 136 is textured by "forming concaves and convexes on [its] surface." Konno, 14:38-42. RDX-0002C.216 illustrates the textured features of transparent layer 136 alongside the complementary texturing of second reflecting layer 120.



Konno's transparent layer 136 constitutes a *textured region*. For example, the '599 patent states that "textured region 312 can have surface features configured to reflect and disperse light," '599 patent, 11:2-3, and that texturing may be created "across only a portion of a

surface by using a selective etching technique, such as a mask, photolithography, and an etch or a laser process to define a specific structure or pattern." '599 patent, 14:47-52.

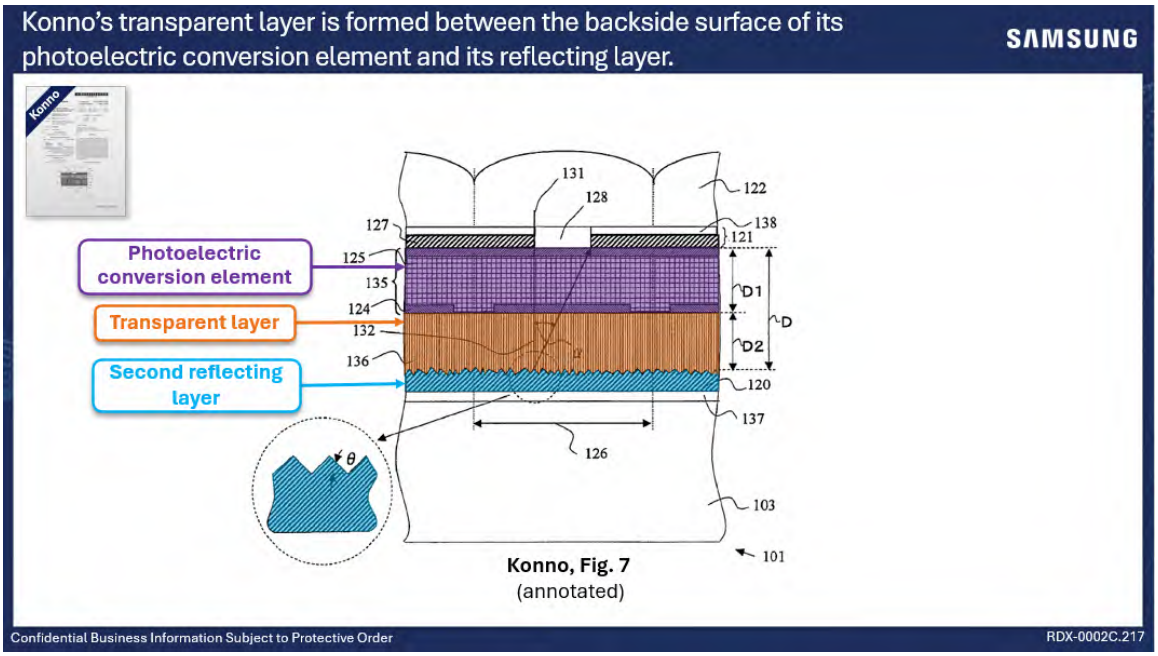
Like the '599 patent, Konno discloses that the concaves and convexes are formed "on the surface of the transparent layer 136 before producing the reflecting layer 120, and then depositing a metal thereon to produce the reflecting layer 120." Konno, 14:38-42. As in the '599 patent, Konno teaches that "[t]he concaves and convexes of the transparent layer 136 can be formed by a known technique such as sputtering and microlithography." Konno, 14:42-45. Konno further discloses that "by providing a transparent layer … convexes or concaves or a structure effective for reflecting or scattering photons can be realized in the reflecting layer adjacent to the transparent layer." Konno, 3:58-62. Konno teaches that transparent layer 136 "transmits photons" and "can provide concaves and convexes which realizes a large reflection angle." Konno, 4:54-58, 15:2-6. Konno also teaches that the textured region "makes it possible to reflect photons which entered from the light entrance window 128 to the first reflecting layer 121, and therefore the amount of photons to be detected again by the photoelectric conversion film 125 can be increased." Konno, 13:66-14:3.

Q504 How does transparent layer 136 constitute a *textured region* under the parties' proposed constructions?

A504 Transparent layer 136 constitutes a *textured region* under the parties' proposed constructions, as it reflects or scatters photons, i.e., diffuses or redirects electromagnetic radiation, thus increasing the quantum efficiency of the device and the effective absorption length for the reasons just explained.

Q505 Is transparent layer 136 *positioned to interact with light incident thereon to increase quantum efficiency of the device?*

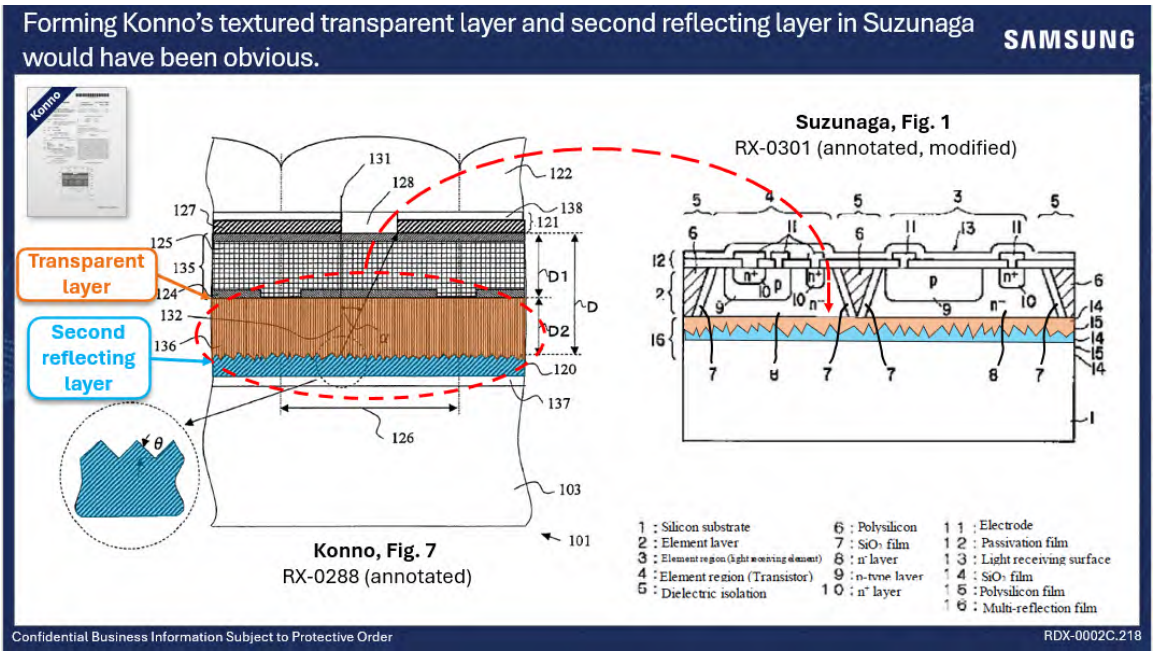
A505 Yes. Konno's transparent layer 136 is *positioned to interact with light incident thereon to increase quantum efficiency of the device*. As RDX-0002C.217 illustrates, Konno's transparent layer 136 is formed between the backside surface of its photoelectric conversion element 135 and its reflecting layer 120. *See also* Konno, 2:56-63 (describing "a structure where the first reflecting layer and the second reflecting layer sandwich the photoelectric conversion means together with the transparent layer").



Konno further teaches that transparent layer 136 "transmits photons" and "can provide concaves and convexes which realizes a large reflection angle." Konno, 4:54-58, 15:2-6. Konno also teaches that its texturing "makes it possible to reflect photons which entered from the light entrances window 128 to the first reflecting layer 121, and therefore the amount of photons to be detected again by the photoelectric conversion film can be increased." Konno, 13:66-14:3. POSITAs would have understood that, by reflecting photons within the device to increase the amount of detected photons, Konno's textured region *increase[s]* the *quantum efficiency of the device*. *See* JX-0017C (Sickler), 108:4-109:19 (explaining that increasing the pathlength light travels within the pixel increases the pixel's quantum efficiency, as it provides more opportunities for the light to be absorbed).

Q506 Would implementing Konno's transparent layer 136 and second reflecting layer 120 in Suzunaga have been obvious?

A506 Yes. As RDX-0002C.218 illustrates, POSITAs would have been motivated to replace Suzunaga's multi-reflection film 16 with Konno's transparent layer 136 and second reflecting layer 120 to similarly cover Suzunaga's backside surface.



Q507 Why would POSITAs be motivated to make this combination?

A507 As discussed, Konno teaches that texturing transparent layer 136 "makes it possible to reflect photons which entered from the light entrance window 128 to the first reflecting layer 121, and therefore the amount of photons to be detected again by the photoelectric conversion film can be increased." Konno, 13:66-14:3. Likewise Suzunaga similarly discloses a benefit of configuring its device such that light reflects off the backside reflecting material also reflects off the peripheral reflecting material in order to increase the light's path and maximize the pixel's absorption efficiency. *See* Suzunaga, [0019] ("multi-reflection film … reflects the transmitted light transmitted through the semiconductor light receiving element formed on the element layer, and impinges the reflected light again on the semiconductor light receiving element"), [0064] ("SiO_2 film 7 in the element region [can be] also a multi-reflection film," such that it "can be used as part of the reflection surface when scattered light is incident from the incident surface 13"). POSITAs would therefore have been motivated to implement Konno's textured surfaces in Suzunaga to achieve this shared goal.

Q508 Are there any other reasons why POSITAs would have been motivated to make this modification?

A508 Yes. Konno further teaches that:

> [W]hen the reflecting layers 120 and 121 consist of metals, it is also possible to electrically connect at least one of these to ground or electrode potential of a read-out circuit, a control circuit, a power supply or the like.
>
> By using such a [metal] structure, error signals and noises generated in output signals of the photo detector 101 by external noises which flow in from the outside and flow into the photo-detector 101 and detected in the

> photoelectric conversion element 135, wiring or the like can be thereby reduced.

Konno, 12:29-38. Accordingly, POSITAs would have been motivated to alter Suzunaga to incorporate Konno's transparent layer 136 and second reflecting layer 120 to reduce error signals and noises generated in output signals as Konno teaches—which Suzunaga's multilayer dielectric reflector would not have provided—as well as achieve this mutually-recognized benefit of increasing the amount of light reflected back into the pixel.

Q509 Would POSITAs have reasonably expected success in making this modification?

A509 Yes. POSITAs would have reasonably expected success in replacing Suzunaga's multi-reflection film 16. For example, Konno's transparent layer 136 is "formed from a material which transmits photons, for example, glass." Konno, 9:35-41. Suzunaga teaches that its multi-reflection film can comprise a layer of SiO_2—i.e., glass—on its backside surface. POSITAs would have understood that texturing one of Suzunaga's SiO_2 layers using Konno's methods requires nothing more than the use of a known technique to obtain predictable results. *See also* Suzunaga, [0035] ("process of laminating a SiO_2 film and a polysilicon film has a proven track record in the manufacture of semiconductor integrated circuits, and a major advantage of this process is thought to be that there are no processing problems").

Q510 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination due to increased dark current?

A510 Yes. Dr. Mansoorian opines, without explanation, that "substituting Konno's metal reflector for Suzunaga's multi-reflection film 16 would significantly increase the generation of dark current." RX-0911C, ¶484. I disagree. As explained, the added metal reflector would be separated from Suzunaga's pixel by a SiO_2 transparent layer, and Konno teaches that such a configuration prevents dark current. *See* Konno, 15:6-22 .

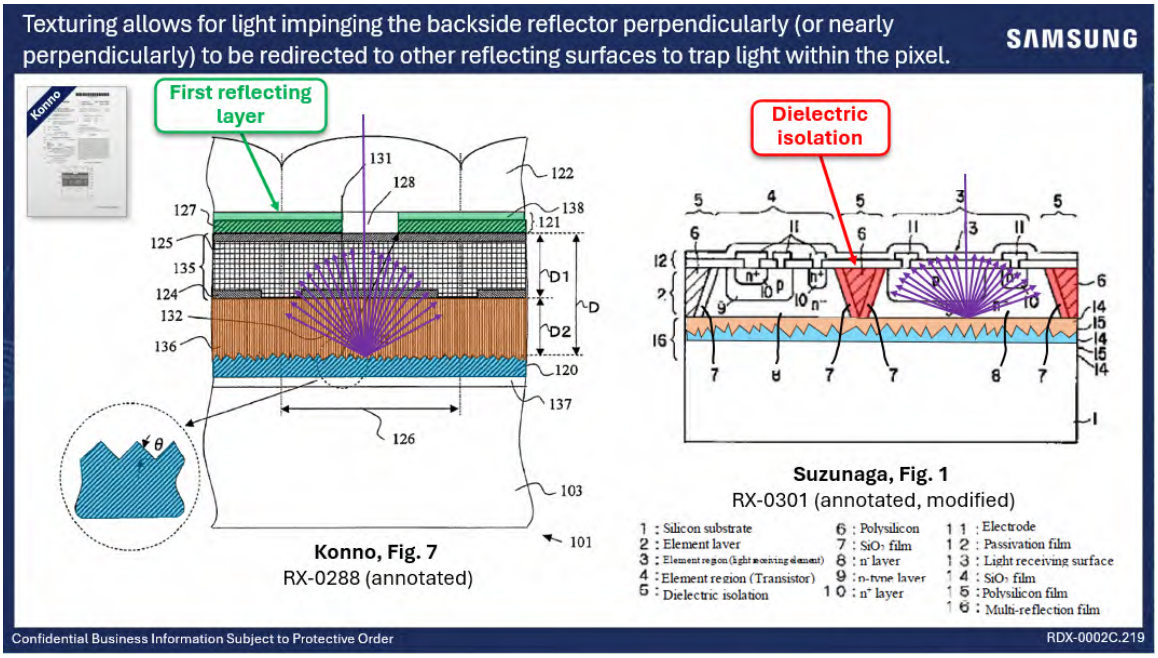
Q511 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination without also adding Konno's first reflecting layer 121 and window 128?

A511 Yes. Dr. Mansoorian opines that POSITAs "would have understood the 'transparent layer 136' and the 'first reflecting layer 121' with 'window 128' to be inextricably linked," such that POSITAs would not incorporate Konno's teaching of a textured region without also adding Konno's frontside reflectors. RX-0911C, ¶485. I disagree and note this is not a theory presented in SiOnyx's contentions. RX-0606C.438-439.

POSITAs would understand that the benefits Konno describes due to texturing, namely, reflecting light "with a large amount of horizontal components," i.e., "with a large reflection angle," thus making "it possible to reflect photons which entered the light entrance window 128 to the first reflecting layer 121," to increase absorption. Konno, 13:63-14:3. That is, Konno teaches that texturing allows for light impinging the backside reflector perpendicularly (or nearly perpendicularly) can be redirected to other reflecting surfaces to trap it within the pixel. Such texturing would likewise be effective in Suzunaga, as it would cause light impinging Suzunaga's backside reflector perpendicularly (or nearly

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perpendicularly) to be scattered to Suzunaga's dielectric isolation 5 to trap light within Suzunaga's pixel, as RDX-0002C.219 illustrates.



Q512 Are there any other reasons why you disagree with Dr. Mansoorian's argument?

A512 Yes. As discussed, POSITAs would likewise understand that the thickness of transparent layer 136 and the depth of dielectric isolation 5 could be adjusted to increase Suzunaga's overall sensitivity, e.g., having dielectric isolation 5 extend to Suzunaga's backside reflector to prevent crosstalk. Additionally, transparent layer 136 only needs to be slightly thicker than the depth of the concaves and convexes. *See* Konno, 15:6-16.

Finally, even if Konno's first reflecting layer 121 and window 128 were required for this combination, as Dr. Mansoorian incorrectly asserts, POSITAs would still be motivated to make this combination. As I will explain for '599 patent (Ground 7) claim 19[e], incorporating Konno's first reflecting layer 121 and window 128 in Suzunaga's device would have been obvious. In particular, Dr. Mansoorian's speculated concerns regarding dark current would be nullified by the fact that Suzunaga's passivation film 12 would separate Konno's first reflecting layer 121 and window 128 from Suzunaga's pixel.

Q513 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination because it would not improve Suzunaga's efficiency?

A513 Yes. Dr. Mansoorian opines that this limitation is not met because "Dr. Neikirk fails to provide any support for the notion that the textured transparent layer 136 leads to improved efficiency over Suzunaga's multi-reflection film 16," and that "[t]o the detriment of his own opinion, Dr. Neikirk refers to a portion of Schubert that states 'the metal-semiconductor reflectors … have 50% or greater reflectivity,' whereas Suzunaga teaches a multi-reflection layer 16 that reflects 'almost 100% of the incident light.'" RX-0911C,

¶488. I disagree and note this is not a theory presented in SiOnyx's contentions. RX-0606C.437-438.

Q514 Why do you disagree?

A514 First, as explained, POSITAs would understand that using Konno's textured transparent layer 136 and second reflecting layer would increase the amount of light detected by Suzunaga—and thus improve Suzunaga's efficiency—by reflecting perpendicular (or nearly perpendicular) light that would ordinarily escape Suzunaga's pixel to Suzunaga's dielectric isolation 5 (or an added frontside reflector, as I will explain) to trap it within Suzunaga's pixel.

Second, Dr. Mansoorian's reliance on Schubert's statement that "the metal-semiconductor reflectors … have 50% or greater reflectivity," RX-0911C, ¶488 (citing Schubert, Table 10.2), is misplaced. As Dr. Mansoorian notes, these reflectivity values are for metal-semiconductor reflectors, i.e., a metal abutting a semiconductor. In Suzunaga as modified by Konno, however, the reflector would be a metal-dielectric reflector, as Konno's metal second reflecting layer 120 would be separated from Suzunaga's pixel by SiO_2 transparent layer 136. Moreover, Konno's second reflecting layer 120 is formed "of a metal such as aluminum and silver." Konno, 8:35-38. All the reflectivity values listed in Schubert Table 10.2 for silver exceed 96.9% and for aluminum exceed 80.05%. Schubert, Table 10.2

Q515 Are you aware of Dr. Mansoorian's argument that POSITAs would not be motivated to make this combination due to manufacturing difficulties?

A515 Yes. Dr. Mansoorian opines this limitation is not met because "Dr. Neikirk fails to show how a POSITA would understand the transparent layer 136 and the second reflecting layer 120 to bond the silicon substrate 1 and the element layer 2 of Suzunaga." RX-0911C, ¶489. I disagree.

As explained, Konno's transparent layer 136 is "formed from … for example, glass," e.g., SiO_2, Konno, 9:35-41, and Suzunaga's multi-reflection film can comprise a layer of SiO_2—i.e., glass—on its backside surface. *E.g.*, Suzunaga, Fig. 1. That is, POSITAs would understand that transparent layer 136 could be bonded to the element layer 2 in the same fashion, as both transparent layer 136 and the top layer of Suzunaga's multi-reflection film 16 are formed of SiO_2.

Q516 Are you aware of Dr. Mansoorian's argument that POSITAs would not understand that transparent layer 136's thickness could be adjusted?

A516 Yes. Dr. Mansoorian opines that POSITAs "would have understood Konno to teach away from having an adjustable thickness." RX-0911C, ¶490. I disagree. As explained, POSITAs would understand that transparent layer 136 only needs to be slightly thicker than the depth of the concaves and convexes, which POSITAs would understand could be quite small. *See* Konno, 15:6-16.

While Konno discusses using a thicker transparent layer in order to minimize the angle of light which can escape through its window 128, POSITAs would recognize that transparent

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layer 136's thickness is a design choice and that in certain instances a thinner transparent layer 136 is preferable if they were trying to minimize the device's size as opposed to maximizing the amount of light absorbed. This is particularly true when transparent layer 136 is textured, as texturing will reflect light "with a large amount of horizontal components," i.e., "with a large reflection angle," Konno, 13:63-14:3, such that the amount of light being reflected at the angle which would cause to escape through the pixel's light incident surface (e.g., through the aperture) would decrease.

Q517 Are you aware of Dr. Mansoorian's argument that POSITAs would understand Konno to suggest that transparent layer 136' cannot be thin?

A517 Yes. Dr. Mansoorian opines that at 15:6-16 "Konno suggests an embodiment in which the concaves and convexes are larger than the photoelectric conversion element." RX-0911C, ¶491. I disagree. POSITAs would understand that 15:6-16 suggests that transparent layer 136 allows for concaves and convexes of "various sizes [to] be realized." That is, transparent layer 136 provides a space for the concaves and convexes to be formed, and, as explained, POSITAs would understand transparent layer 136 only needs to be slightly thicker than the depth of the concaves and convexes.

Q518 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination because Konno's reflecting layer 120, as used in Suzunaga, could not be connected to a metallization?

A518 Yes. Dr. Mansoorian opines that Konno's reflecting layer 120 could not be a metallization because "[t]here is no conceivable way the reflecting layers 120 and 121 could connect to the electrodes 13 without interfering with the light receiving element." RX-0911C, ¶¶450-451. I disagree. POSITAs would understand that reflecting layer 120 could be connected to metallization not depicted in Suzunaga's figure 1.

Q519 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination because it would be too large for an image sensor?

A519 Yes. Dr. Mansoorian opines that Suzunaga and Konno do not render this limitation obvious because the resulting device "would be too large and undesirable for an image sensor." RX-0991C, ¶458. I disagree. First, as explained for '714 patent (Ground 7), claim 1, the Light Trapping Patents are not limited to image sensors; Dr. Mansoorian is incorrect in his assumptions regarding Suzunaga's dimensions; and, even if his assumptions were correct, Suzunaga's dimensions are well within the dimensions contemplated by the Light Trapping Patents. Second, as explained, Konno's transparent layer 136 does not need to be at least as thick as Suzunaga's pixel.

Q520 Are you aware of Dr. Mansoorian's argument that POSITAs would not be motivated to modify Suzunaga based on Konno because Konno is non-analogous art?

A520 Yes. While not advanced for this combination, Dr. Mansoorian opines elsewhere that POSITAs would not combine Suzunaga and Konno because "Suzunaga discloses a device comprising a single or an array of PIN photodiodes capable for use in fiber-optic detection," while "Konno... discloses monochrome image sensor used for personal

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authentication devices." RX-0911C, ¶403. I disagree. As I explained in the Overview of Konno, Konno is not limited to personal authentication systems, but is instead directed to solid-state imaging elements, including an "image sensor … and digital camera," just like Hwang. Konno, 1:15-22. And as explained for '714 patent (Ground 7), claim 1, POSITAs would not consider PIN photodiodes and pinned photodiodes to be entirely different technology.

3. Limitation 19[c]

Q521 Limitation 19[c] is *a peripheral light trapping material substantially covering the peripheral sidewall*. Does Suzunaga satisfy this limitation?

A521 Yes. As RDX-0002C.220 illustrates, '599 patent, limitation 19[c] is identical to '714 patent, limitation 1[c]. Suzunaga teaches or suggests '599 patent, limitation 19[c] for the reasons discussed for '714 patent (Ground 7), limitation 1[c].

4. Limitation 19[e]

Q522 Limitation 19[e] is a reflective layer coupled to the light incident side and having an aperture to allow entry of light into the pixel. Have you formed an opinion regarding this limitation?

A522 Yes. This Suzunaga and Konno render obvious *a reflective layer coupled to the light incident side and having an aperture to allow entry of light into the pixel*.

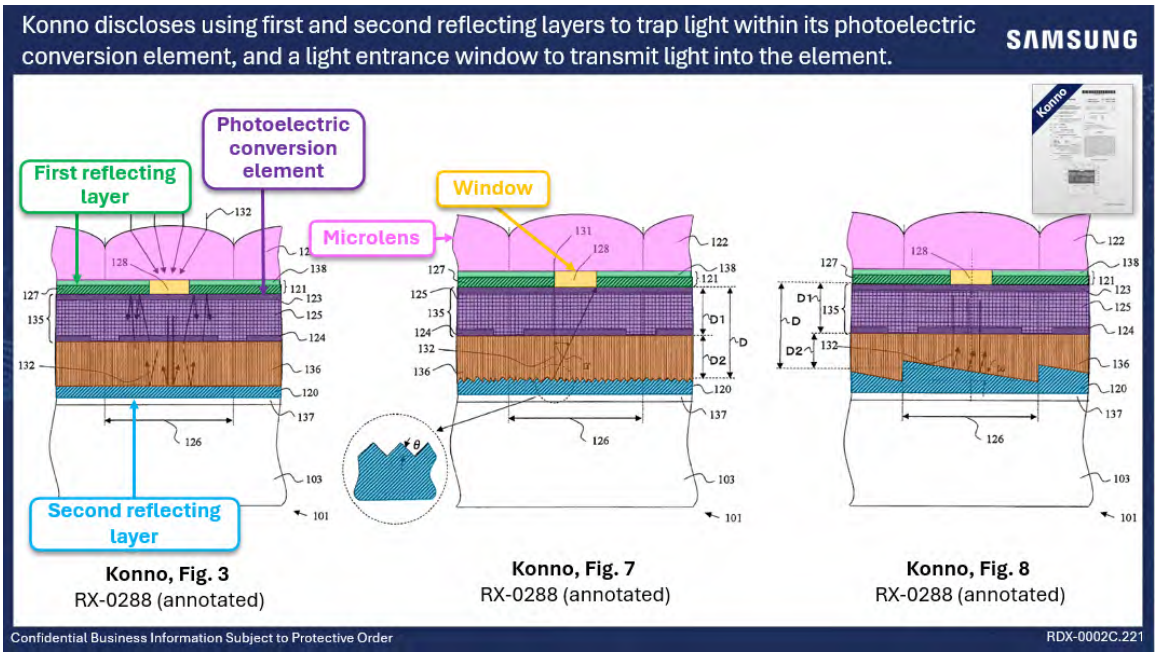
As explained regarding the Terms Remaining in Dispute, I understand that the parties proposed constructions for *reflective layer*. Yamada, as modified by Konno, includes a *reflective layer coupled to the light incident side* under either construction.

Q523 How do Suzunaga and Konno render this claim obvious?

A523 As I will explain, it would be obvious to implement Konno's second reflecting layer 121 (*reflective layer coupled to the light incident side and having an aperture to allow entry of light into the pixel*) in Suzunaga.

As RDX-0002C.221 illustrates, Konno discloses a "solid-state imaging element 110 [that] has a structure where a reflecting layer (second reflecting layer) 120, a transparent layer 136, a photoelectric conversion element 135, a reflecting layer (first reflecting layer) 121 and microlens 122 are formed on a substrate 103," to improve detection sensitivity. Konno, 8:18-22. *See also* Konno, 8:22-25 ("second reflecting layer 120 and first reflecting layer 121 sandwich … photoelectric conversion element 135"). Konno teaches that "light entrance window 128 through which the incident photons 132 transmit is formed in the first reflecting layer 121." Konno, 8:56-58.

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Q524 Does Konno describe the purpose of reflecting layer 121?

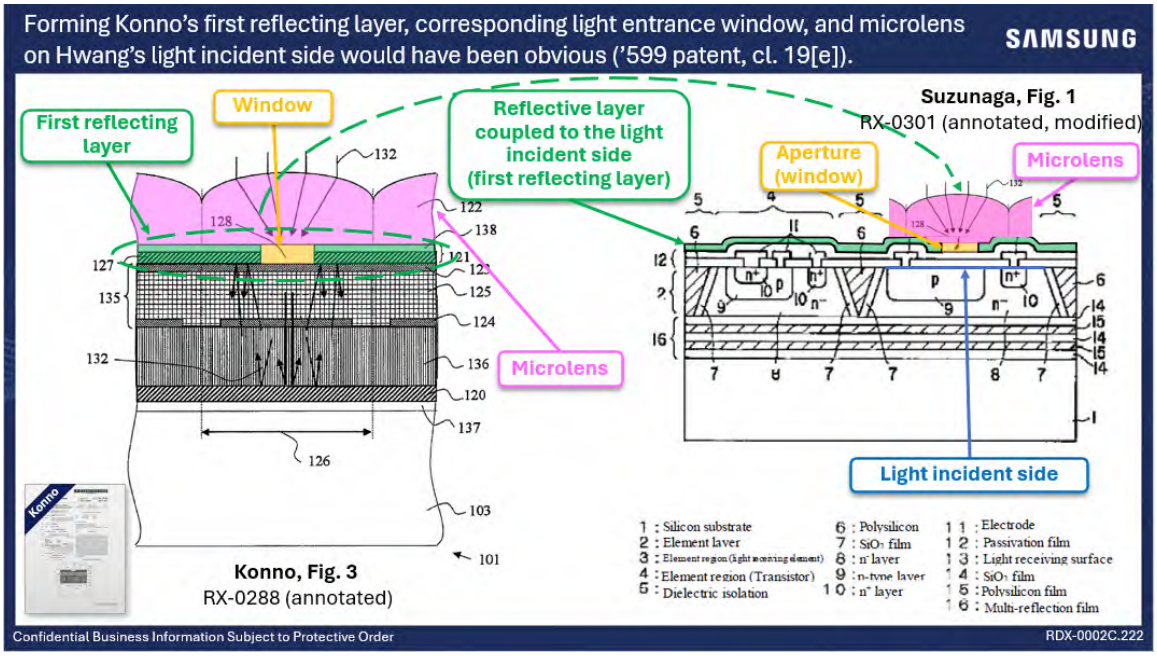
A524 Yes. Konno teaches that the reflecting layers reflect light back into the pixel. Specifically, Konno teaches that "photons which entered from the light entrance window 128 can be effectively confined between the first and second reflection layers 121 and 120 to … improve the detection sensitivity." Konno, 11:65-12:3. Konno also teaches that "part of the photons which passed through the photoelectric conversion film 125 reach the reflecting surface 127 of the first reflecting layer [121], are reflected again, and reach the photoelectric conversion film 125." Konno, 10:4-8.

Konno further teaches that "[t]he second reflecting layer 120 and the first reflecting layer 121 have a function of confining photons which entered into the solid-state imaging element 110 between the both." Konno, 8:31-33. Because "photons which entered into the solid-state imaging element 110 are reciprocated between the second reflecting layer 120 and the first reflecting layer 121, [the] amount of reciprocating photons … can be increased." Konno, 10:14-18. As Konno teaches, "photons which entered from the light entrance window 128 can be effectively confined between the first and second reflection layers 121 and 120 to increase the amount of photons participating in photoelectric conversion by the photoelectric conversion element 135 and thereby improve the detection sensitivity." Konno, 11:65-12:3.

Q525 Why would POSITAs use Konno's reflecting layer 121 in Suzunaga?

A525 As RDX-0002C.222 illustrates, implementing Konno's first reflecting layer 121, corresponding light entrance window 128, and microlens 122 in Suzunaga reduces the loss of light leaving Suzunaga's pixel after being reflected from its dielectric isolation 5 and multi-reflection film 16, and to thereby further improve Suzunaga's detection sensitivity. As RDX-0002C.222 also illustrates, POSITAs would also be motivated to add Konno's microlens 122, which Konno teaches "concentrates photons which entered into the solid-

state imaging element 110, and leads them to the light entrance window 128." Konno, 9:4-9.



As RDX-0002C.222 illustrates, this modification results in Suzunaga having a *frontside light trapping material* (first reflective layer 121) *at least partially covering the light incident surface* (top surface of Suzunaga's pixel).

This structure would satisfy the claim, including under either party's proposed construction.

Q526 How would Konno's reflecting layer 121, as added to Suzunaga, be a *reflective material*?

A526 Konno teaches that first reflecting layer 121 "can be formed by forming a thin film of a metal such as aluminum and silver," or "[a]lternatively … may be [formed of] layers of a resin mixed with a white pigment." Konno, 8:35-43. Konno's first reflecting layer 121 constitutes a *light trapping material* that reflects light back into the pixel, as a solid metal film, as disclosed in Konno, reflects more light than it transmits. *See* Schubert, Table 10.2 (listing reflectivity of metal-air and metal-semiconductor reflectors at 0.5µm and 1.0µm, all of which have 50% or greater reflectivity).

Q527 How does reflecting layer 121 constitute a *reflective layer* under the parties' proposed constructions?

A527 Reflecting layer 121 constitutes a *reflective layer* under either party's proposed construction, as it is a layer that reflects and will reflect more light back into the pixel than it transmits for the reasons just explained.

Q528 Would POSITAs have been motivated to make this modification?

A528 Yes. POSITAs would have been motivated to make this modification, as adding Konno's first reflective layer 121, corresponding window 128, and microlens 122 to Suzunaga would allow for light to be reflected from the first reflecting layer back into Suzunaga's pixel, thus increasing its efficiency. Specifically, Konno teaches that using its first reflective layer 121 allows for "[t]he second reflecting layer 120 and the first reflecting layer 121 [to] have a function of confining photons which entered into the solid-state imaging element [] between the both…." Konno, 8:31-33. POSITAs would have had a reasonable expectation of success in making this modification because, for example, Suzunaga multi-reflection film 16 and dielectric isolation 5 would serve to reflect light back to Konno's first reflective layer 121, which would then reflect light back into Suzunaga's pixel, thus increasing its efficiency.

Q529 Would POSITAs have had a reasonable expectation of success in making this modification?

A529 Yes. POSITAs would have reasonably expected success in making this modification, as POSITAs would have recognized that adding Konno's first reflective layer 121, corresponding light entrance window 128, and microlens 122 could be readily implemented in Suzunaga according to commonly known manufacturing methods.

5. Limitation 19[f]

Q530 Limitation 19[f] is *wherein the reflective layer is operable to reflect at least a portion of light impinging thereupon from inside the pixel back into the pixel back into the pixel.* Have you formed an opinion regarding this limitation?

A530 Yes. Suzunaga and Konno render this limitation obvious. I understand that the ALJ amended *thereupon from inside the pixel back into the pixel back into the pixel* such that it now reads "thereupon from inside the pixel back into the pixel." Order No. 36 at 40.

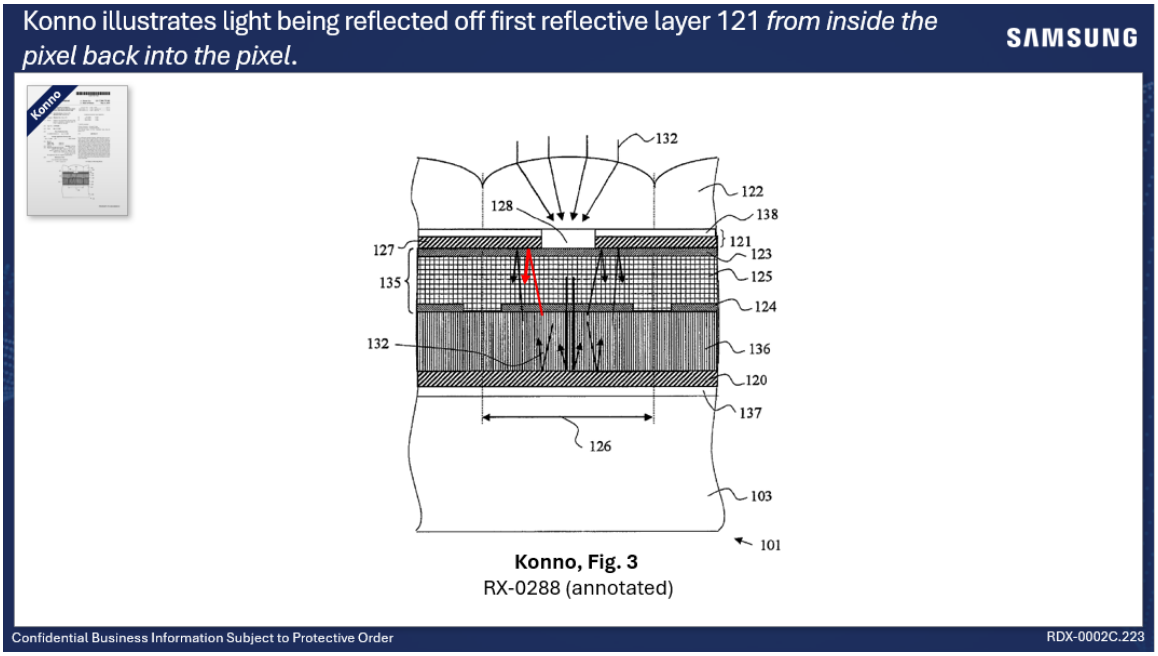
Q531 How does Suzunaga, as modified by Konno, satisfy limitation 19[f]?

A531 As discussed for '599 patent (Ground 7), limitation 19[e], using Konno's first reflective layer 121 (*reflective layer coupled to the light incident side*) in Suzunaga would have been obvious. such a structure, first reflective layer 121 constitutes a reflective layer that *is operable to reflect at least a portion of light impinging thereupon from inside the pixel back into the pixel*. As discussed for '714 patent (Ground 7), limitation 1[c] and '599 patent (Ground 7), limitations 19[b]-[c], Suzunaga, as modified by Konno, also includes a backside reflective layer (multi-reflection film 16) and a sidewall reflective layer (dielectric isolation 5), and the purpose of these backside and peripheral reflecting layers is to reflect light back into Suzunaga's pixel.

POSITAs would understand that Suzunaga—containing reflective peripheral, backside, and (as modified by Konno) frontside surfaces—is operable to reflect at least a portion of light off first reflective layer 121, i.e., to reflect light *from inside the pixel back into the*

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pixel. Indeed, as RDX-0002C.223 illustrates, Konno illustrates a light ray being reflected off first reflective layer 121 *from inside the pixel back into the pixel*.



See also Yamada, Fig. 7 (illustrating a light ray being reflected by first reflective film 3, second reflective film 8, and third reflective film 11).

b. Claim 33

Q532 Let's turn to claim 33, which is *[t]he device of claim 19, wherein the peripheral light trapping material comprises any of aluminum oxide and hafnium oxide*. Have you formed an opinion regarding this claim?

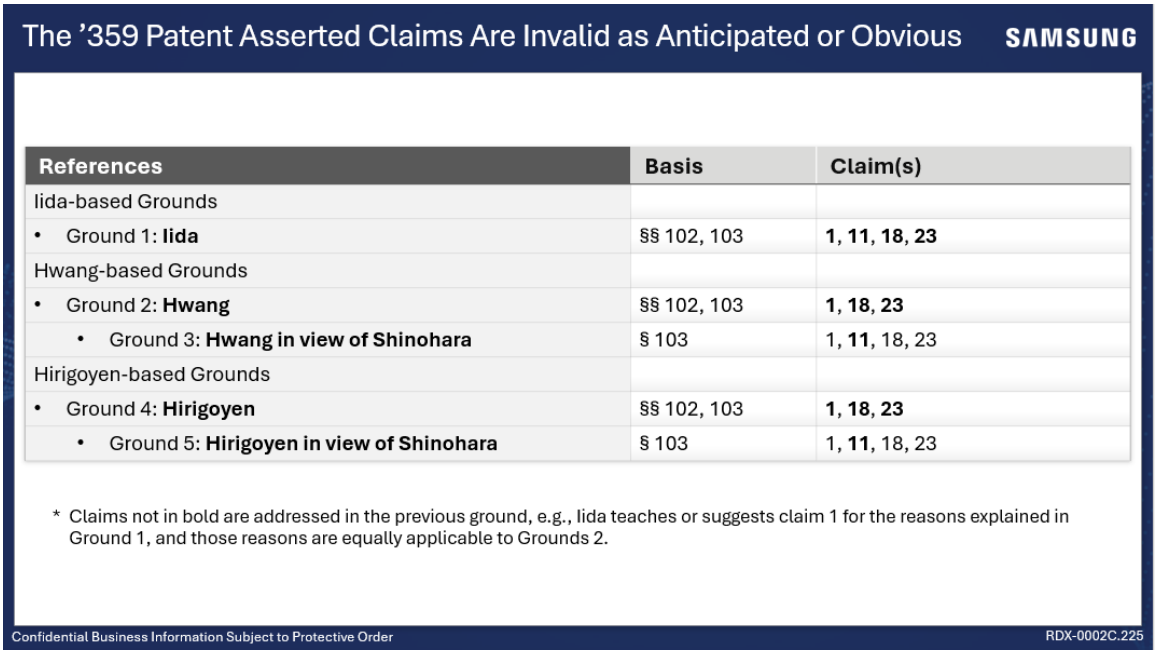
A532 Yes. As explained for '714 patent, limitation 1[c], Suzunaga includes a *peripheral light trapping material*, i.e., a "dielectric isolation region 5 … formed by embedding polysilicon 6 in a V-groove with a SiO_2 film 7 or the like interposed therebetween as a dielectric body," Suzunaga, [0008], that can also be "a multi-reflection film," Suzunaga, [0064]. That is, Suzunaga teaches that its *peripheral light trapping material* (dielectric isolation region 5) can be a "multi-reflection film in which a film having a first refractive index and a film having a second refractive index are alternately laminated." Suzunaga, [0020]. Suzunaga further teaches that "the films having the first and second refractive indexes are each made of one of the following materials … Al_2O_3," Suzunaga, [0022]; *see also* Suzunaga, [0021] ("film having the first refractive index is made of a dielectric material" "dielectric body is made of one of … Al_2O_3"), [0067] ("the thin film having a high refractive index … may be … Al_2O_3.").

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VIII. ’359 Patent Invalidity Based on Anticipation and Obviousness

Q533 Let’s turn to the ’359 patent. Can you summarize your opinions with respect to anticipation and obviousness of the ’359 patent?

A533 Yes. As RDX-0002C.225 illustrates, in my opinion, the ’359 patent Asserted Claims are invalid based on three primary references: Iida, Hwang, and Hirigoyen.



A. Iida-based Grounds

Q534 Let’s start with your Iida-based opinions. Can you please summarize your anticipation and obviousness opinions for the ’359 patent based on Iida?

A534 My Iida-based opinions are based on a single ground, Ground 1, which is that Iida anticipates, or at least renders obvious, claims 1, 11, 18, and 23.

1. Ground 1: Iida Anticipates, or at Least Renders Obvious, Claims 1, 11, 18, and 23

a. Claim 1

1. Limitation 1[a]

Q535 Let’s start with claim 1. Claim 1’s first limitation, 1[a], is relatively long, so let’s take it in parts. The first element is *at least two adjacent light sensitive image sensor pixels*. Does Iida satisfy this element?

A535 Yes. Iida teaches or suggests *at least two adjacent light sensitive image sensor pixels*. Dr. Mansoorian has not disputed this.

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I understand that the ALJ construed *light sensitive image sensor pixel* to have its plain and ordinary meaning. Order No. 36 at 27. Iida discloses an image sensor including *at least two adjacent light sensitive image sensor pixels* under that phrase's plain and ordinary meaning, which I consider to be portions of a device that convert light into electrical signals. Iida states that, according to its fourth embodiment, "the effect to reduce optical crosstalk caused by obliquely incident light entering adjacent pixels is improved." Iida, [0101]. Iida further states that, "[i]n the solid-state imaging device of the third embodiment, each trench-type pixel separation structure 160 is provided between adjacent pixels in a silicon substrate 150 in which photodiodes 201 are formed," Iida, [0081], and that the third embodiment (shown in Figure 9) "is the same" as the fourth embodiment (shown in Figure 10) "except that" in the fourth embodiment "the trench-type pixel separation structure 160 is replaced with a trench-type pixel separation structure 160B," Iida, [0098].

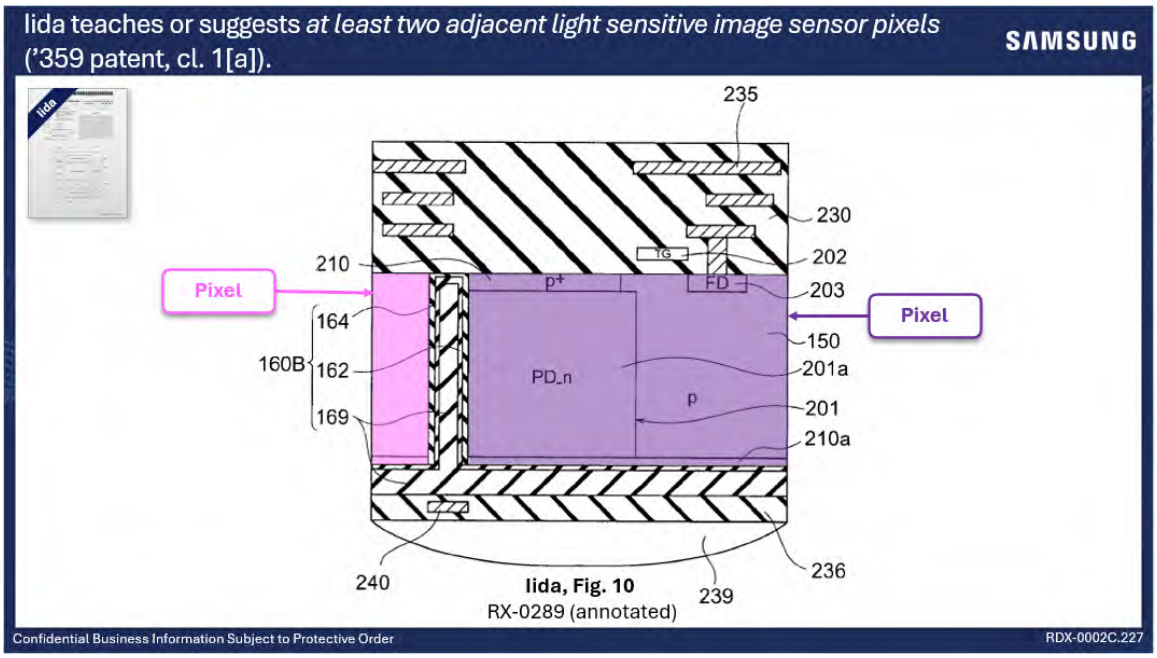
Q536 On w hich embodiment of Iida are you basing your analysis?

A536 Unless otherwise noted, my analyses for the '359 patent pertain to Iida's fourth embodiment, depicted in Figure 10. While I will occasionally reference disclosures pertaining to Iida's third embodiment, they are equally applicable to Iida's fourth embodiment.

Q537 Can you please describe the pixels in Iida's fourth embodiment?

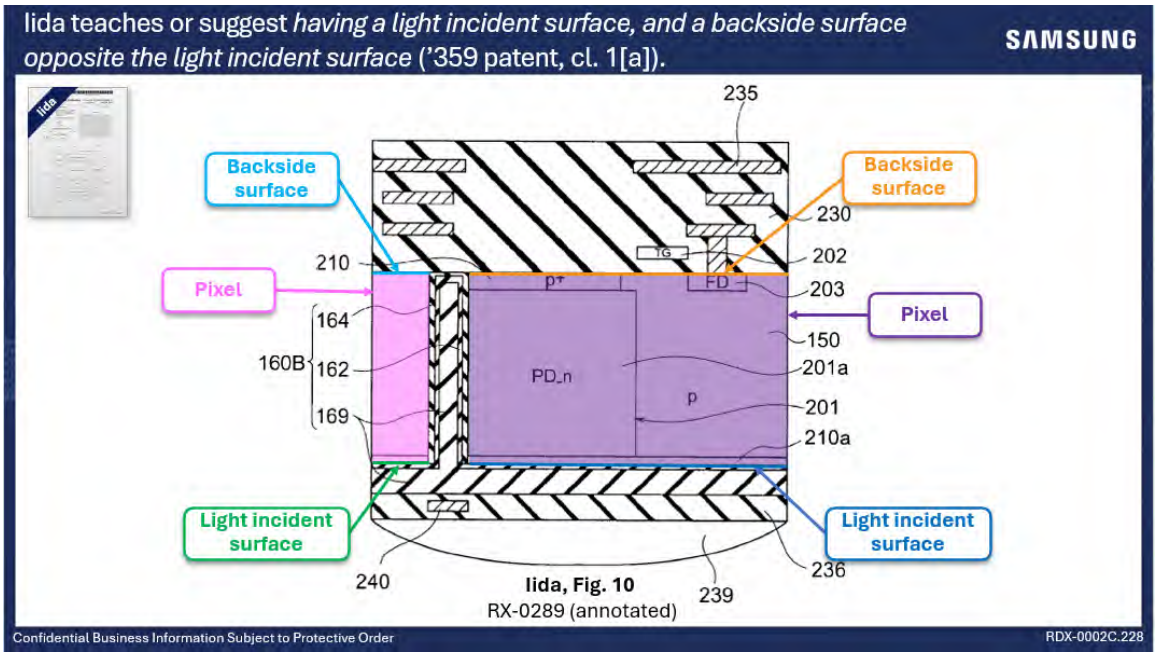
A537 Yes. RDX-0002C.227 depicts a representative pixel from Iida's fourth embodiment, along with an adjacent pixel. POSITAs would understand that each pixel includes n-type semiconductor region 201 ("PD_n" region) and the surrounding semiconductor regions, including p-type semiconductor substrate 150 and doped regions 210, 210a, and 203, with photodiode 201 comprising the junction created between differently doped semiconductor regions. *See* Iida, [0049] ("An n-type impurity region (hereinafter also referred to as a PD_n-region) 201a forming the photodiode 201 is formed in a p-type silicon substrate 150. Signal electrons generated through photoelectric conversions in the photodiode 201 having a pn junction formed with the PD_n-region 201a and the p-type semiconductor substrate 150 are stored in the PD_n-region 201a.").

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Q538 Limitation 1[a]'s second element is *having a light incident surface, and a backside surface opposite the light incident surface*. Does Iida satisfy this element?

A538 Yes. As RDX-0002C.228 illustrates, each pixel in Iida has *a light incident surface and a backside surface opposite the light incident surface*. The interface between the pixel and the horizontal portion of fixed charge film 162 is *a light incident surface*. *See* Iida, [0080] ("Incident light enters a front-illuminated solid-state imaging device from the front face side. On the other hand, the solid-state imaging device of the third embodiment is of a back-illuminated type."). Likewise, the interface between the pixel and insulating film 230 is *a backside surface opposite the light incident surface*. *See* Iida, [0044] ("interlayer insulating film 230 is provided on the front face of the silicon substrate 150").

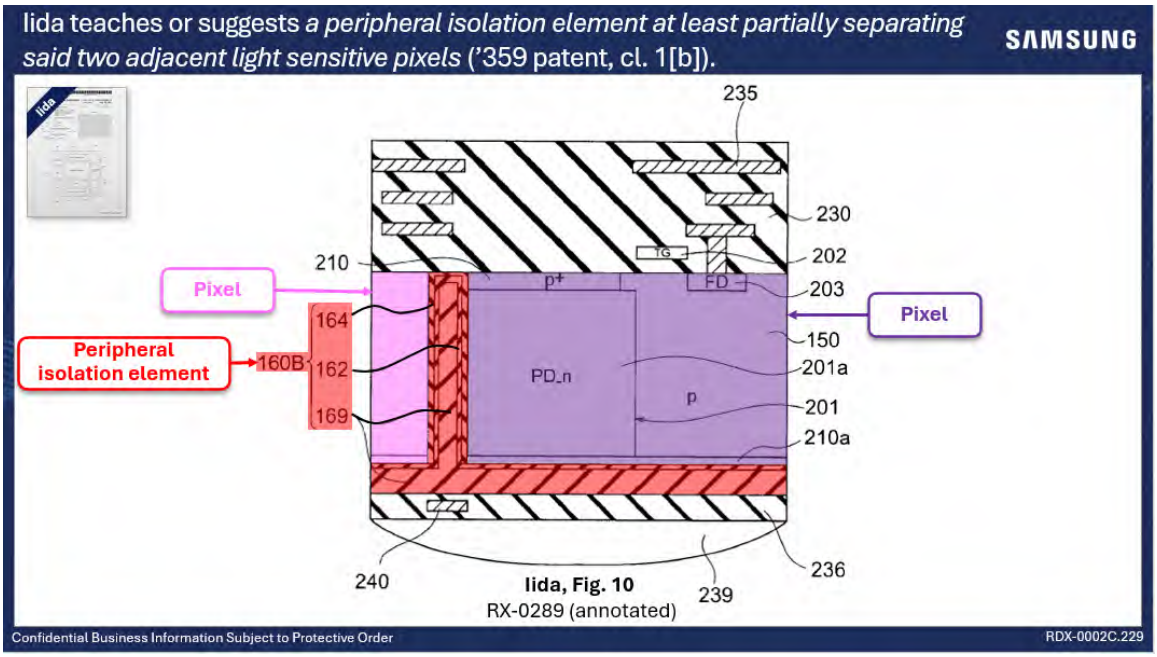


POSITAs would understand that each of the pixels in Iida's fourth embodiment have the same structure as shown in Figure 10. *See* Iida, [0044] (disclosing that the embodiments "provide a solid-state imaging device including … a plurality of pixels provided in the semiconductor substrate"), [0045] (disclosing that the embodiments "will be described more specifically with reference to the drawings").

2. Limitation 1[b]

Q539 Limitation 1[b] is *a peripheral isolation element at least partially separating said two adjacent light sensitive pixels*. Does Iida satisfy this limitation?

A539 Yes. Iida includes an *isolation element*: "a trench-type pixel separation structure 160B." Iida, [0098]. As RDX-0002C.229 illustrates, Iida's pixel separation structure 160B (i) is *peripheral* because it extends along the pixel's periphery; and (ii) *at least partially separates said two adjacent light sensitive pixels* because it isolates the pixel from an adjacent pixel.



Q540 Are you aware of Dr. Mansoorian's argument that Iida does not disclose or render obvious *a peripheral isolation element* because trench-type pixel separation structure 160B allegedly is not disposed along the pixel periphery?

A540 Yes. Dr. Mansoorian opines that, in Iida's Figure 10, "the edge of the pixel, indicated, for example, by microlens 239, extends past trench-type pixel separation structure 160B, clearly showing it does not extend along the pixel periphery." RX-0911C, ¶¶689-690, 693. In other words, Dr. Mansoorian opines that the area shown in the annotated figure in pink is part of the same pixel as the area shown in purple, rather than part of a different pixel adjacent to the purple pixel. I disagree and note this is not a theory presented in SiOnyx's contentions. RX-0606C.467-468.

Q541 Why do you disagree?

A541 POSITAs would understand that structure 160B, which Iida specifically defines and consistently describes as a "pixel separation structure," Iida, [0098], is located at the edges of, and constitutes the boundary between, the two adjacent pixels it separates, as clearly shown in Figure 10. Iida expressly and repeatedly discloses that its "pixel separation structure" 160 serves to separate, and therefore is placed "between," adjacent pixels. *See* Iida, [0081] ("[E]ach trench-type pixel separation structure 160 is provided between adjacent pixels in a silicon substrate 150."); Iida, [0098] ("The solid-state imaging device of the fourth embodiment is the same as the solid-state imaging device of the third embodiment illustrated in FIG. 9, except that the trench-type pixel separation structure 160 is replaced with a trench-type pixel separation structure 160B."); Iida, [0050] ("A trench-type pixel separation structure 160 is provided as a pixel separation structure for element separation from adjacent pixels."); Iida, Abstract ("a plurality of pixels … and a pixel separation structure provided between adjacent ones of the pixels"); Iida, [0044] ("a plurality of pixels … and a pixel separation structure provided between adjacent ones of

the pixels"); Iida, p. 11, claims 1 and 7 (claiming "a pixel separation structure provided between adjacent ones of the pixels in the semiconductor substrate"). Further confirming this, Iida discloses that its light shield 240, located in pixel separation structure 160B between the pink and purple pixels as shown in the annotated figure, serves the purpose of "preventing light from entering between pixels." Iida, [0086] ("the light shield 240 for preventing light from entering between pixels"). If, as Dr. Mansoorian contends, the pixel shown in Figure 10 of Iida extended from the left edge to the right edge of microlens 239, light shield 240 would prevent light from entering the pixel, frustrating the purpose of the microlens itself and Iida's goal of improving light absorption. Moreover, if the pink and purple regions depicted were part of the same pixel, structure 160B would interfere with the operation of the photodiode as it would isolate the "PD_n" region from 201a from adjacent p-type semiconductor substrate 150.

I disagree with Dr. Mansoorian's unsupported assumption that microlenses are always or necessarily "disposed centered on each pixel with their edges aligning with the periphery." RX-0911C, ¶690. POSITAs would know that microlenses can be purposefully offset—specifically, gradually shifted from the center of pixels toward the side of pixels when proceeding from the center to the periphery of the image sensor device—to obtain better sensitivity to off-axis ray paths. Indeed, the concept of "microlens shift" was well-known to POSITAs and reflected in the prior art, including Iida. Multiple embodiments of Iida—not just the fourth embodiment shown in Figure 10—show microlenses not centered on and aligned with the edges of each pixel. *See* Iida, Figs. 3, 9, 10. Other prior art references similarly disclose microlenses not centered on and aligned with the edges of each pixel. *See, e.g.*, Hwang, Figs. 2, 5, 6.

3. Limitation 1[c]

Q542 Limitation 1[c] is *each of said pixels having at least one doped region disposed on at least one of the light incident surface and the backside surface*. Does Iida satisfy this limitation?

A542 Yes. Each pixel in Iida *ha[s] at least one doped region disposed on at least one of the light incident surface and the backside surface*. Dr. Mansoorian has not disputed this. Iida discloses that "p+ type impurity diffused region 210 for preventing dark current … is provided in a region on the front face side of the silicon substrate 150 between the PD_n-region 201a and the interlayer insulating film 230." Iida, [0082]. Iida further discloses that "p+-type impurity diffused region 210a for preventing dark current … is provided in a region on the back face side of the silicon substrate 150 between the PD_n-region 201a and the fixed charge film 162." Iida, [0082].

Q543 Are regions 210 and 210a doped regions?

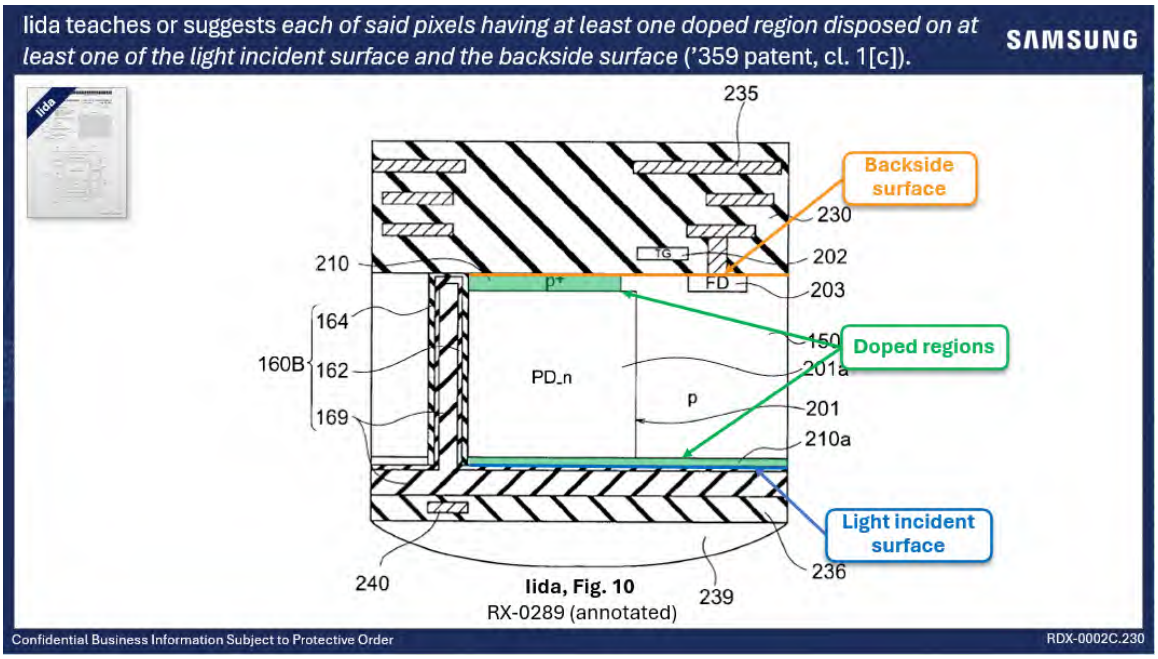
A543 Yes. POSITAs would understand that regions 210 and 210a are *doped regions*. The '359 patent similarly discloses forming p+-type regions as regions doped by introduction of impurities. *See* '359 patent, 17:9-30:

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> [L]ayers can vary in majority carrier polarity (i.e., donor or acceptor impurities). The donor or acceptor impurities are typically determined by the type of dopant/impurities introduced into the device…. In some aspects, such semiconductor materials can include … a p-type layer…. [I]n some aspects, … p(+) … type semiconductor layers can be used. The … positive signs are indicators of the relative magnitude of the doping of the semiconductor material.

Q544 Are regions 210 and 210a *disposed on* the *light incident* and *backside* surfaces of Iida's pixels, respectively?

A544 Yes. As RDX-0002C.230 illustrates, doped region 210 *is disposed on the light incident surface* and doped region 210a is *disposed on the backside surface*. As discussed for limitation 1[a], the interface between the pixel and the horizontal portion of fixed charge film 162 is the pixel's *light incident surface* and the interface between the pixel and insulating film 230 is the pixel's *backside surface*. As RDX-0002C.230 illustrates, region 210 is disposed at the interface between the pixel and the horizontal portion of fixed charge film 162 and region 210a is disposed at the interface between the pixel and insulating film 230.



4. Limitation 1[d]

Q545 Limitation 1[d] is *wherein the peripheral isolation element comprises at least two materials having different indices of refraction*. Does Iida satisfy this limitation?

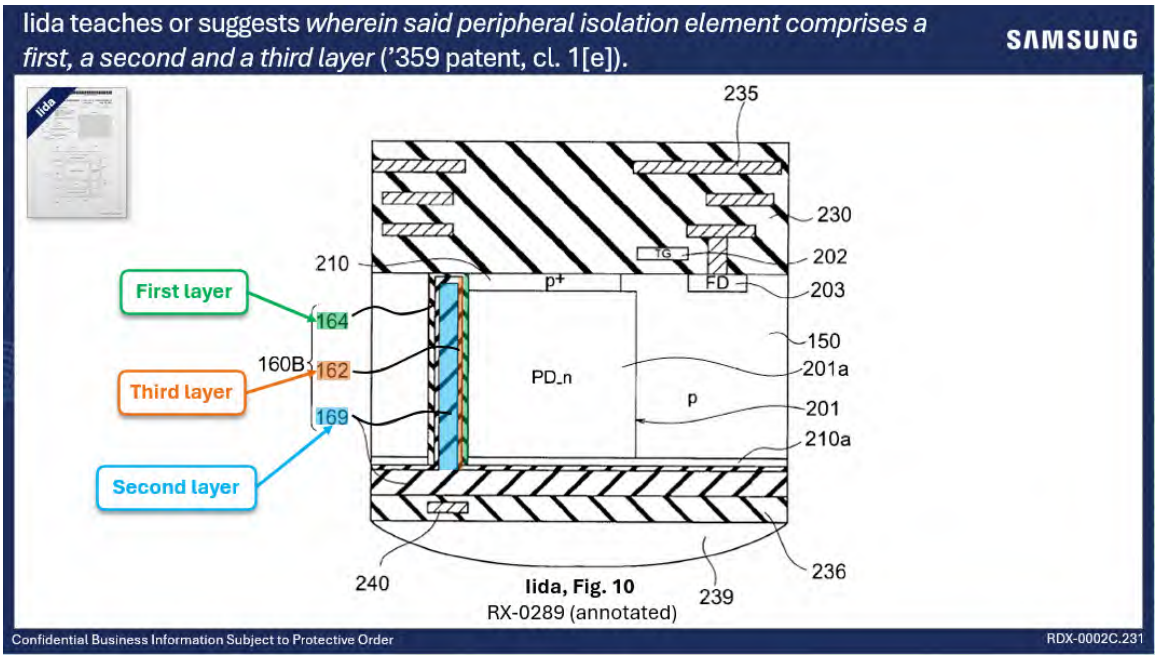
A545 Yes. Iida's pixel separation structure 160B *comprises at least two materials having different indices of refraction*. Dr. Mansoorian has not disputed this. Iida discloses that pixel separation structure 160B comprises, among other things, "silicon oxide layer 164" and "fixed charge film 162 made of hafnium oxide." Iida, [0099]. Iida discloses that its

silicon oxide has a refractive index of 1.4, Iida, [0052], and that its hafnium oxide has a refractive index of 2.0, Iida, [0100].

5. Limitation 1[e]

Q546 Limitation 1[e] is *wherein said peripheral isolation element comprises a first, a second and a third layer*. Does Iida satisfy this limitation?

A546 Yes. As RDX-0002C.231 illustrates, Iida's pixel separation structure 160B *comprises a first, a second and a third layer*: (1) "silicon oxide layer 164" (*first layer*); (2) "film 169 made of a low refractive index material" (*second layer*); and (3) "fixed charge film 162 made of hafnium oxide" (*third layer*).



6. Limitation 1[f]

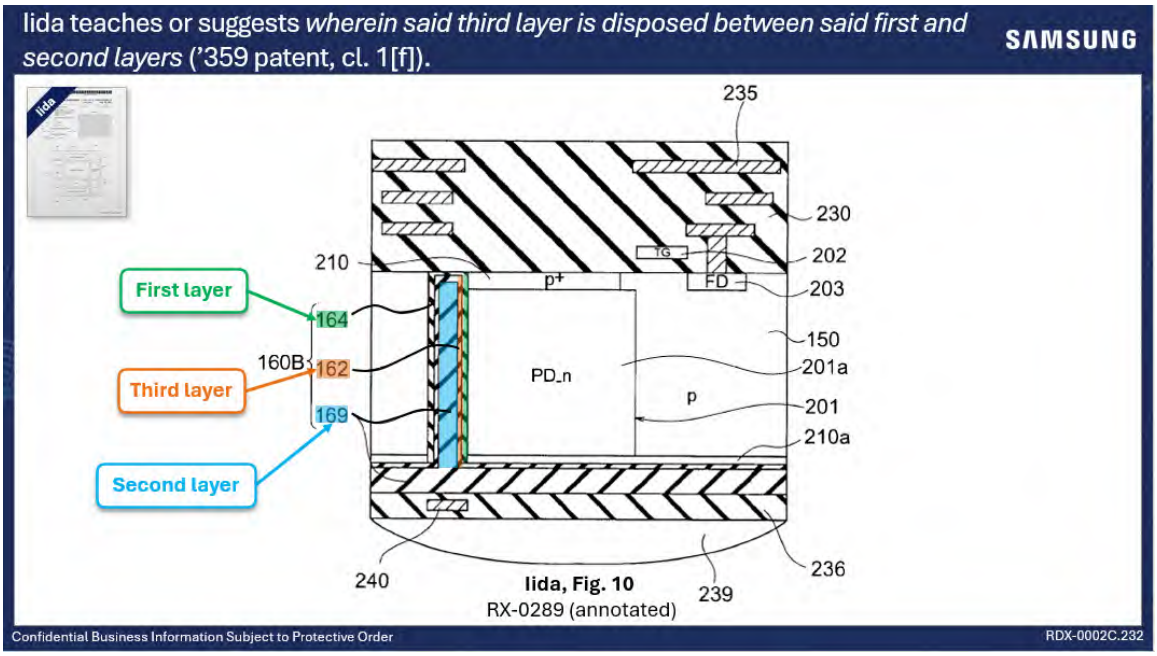
Q547 Limitation 1[f] is *wherein said third layer is disposed between said first and second layers*. Does Iida satisfy this limitation?

A547 Yes. Iida teaches or suggests *wherein said third layer is disposed between said first and second layers*. Dr. Mansoorian has not disputed this.

As explained in the Terms Remaining in Dispute, I understand that the parties proposed constructions for limitation 1[f] as a whole. Iida satisfies limitation 1[f] under either construction.

Q548 How does Iida satisfy this limitation?

A548 RDX-0002C.232 illustrates, the *third layer* of pixel separation structure 160B (fixed charge film 162) *is disposed between the first layer* (layer 164) *and the second layer* (film 169).



7. Limitation 1[g]

Q549 Limitation 1[g] is *wherein each of said first and second layer exhibits an index of refraction less than an index of refraction of said third layer*. Does Iida satisfy this limitation?

A549 Yes. Each of the *first layer* and *second layer* of Iida's pixel separation structure 160B *exhibits an index of refraction less than an index of refraction of said third layer*. Dr. Mansoorian has not disputed this. Iida discloses that its silicon oxide layer 164 (*first layer*) has a refractive index of 1.4; that the refractive index of its low refractive index film 169 (*second layer*) "should preferably be … lower … than the refractive index of hafnium oxide," Iida, [0100]; and that its hafnium oxide film 162 (*third layer*) has a refractive index of 2.0, Iida, [0100]. Accordingly, Iida teaches that its silicon oxide layer 164 (*first layer*) and low refractive index film 169 (*second layer*) have indices of refraction less than the refractive index of its hafnium oxide layer 162 (*third layer*).

b. Claim 11

Q550 Let's turn to claim 11, which is *[t]he device of claim 1, wherein the peripheral isolation element comprises any of aluminum oxide and hafnium oxide*. Does Iida satisfy this claim?

A550 Yes. Iida's *peripheral isolation element* (pixel separation structure 160B) *comprises hafnium oxide*. *See* Iida, [0099] ("pixel separation structure 160B has … [a] fixed charge film 162 made of hafnium oxide"). Dr. Mansoorian has not disputed this.

c. Claim 18

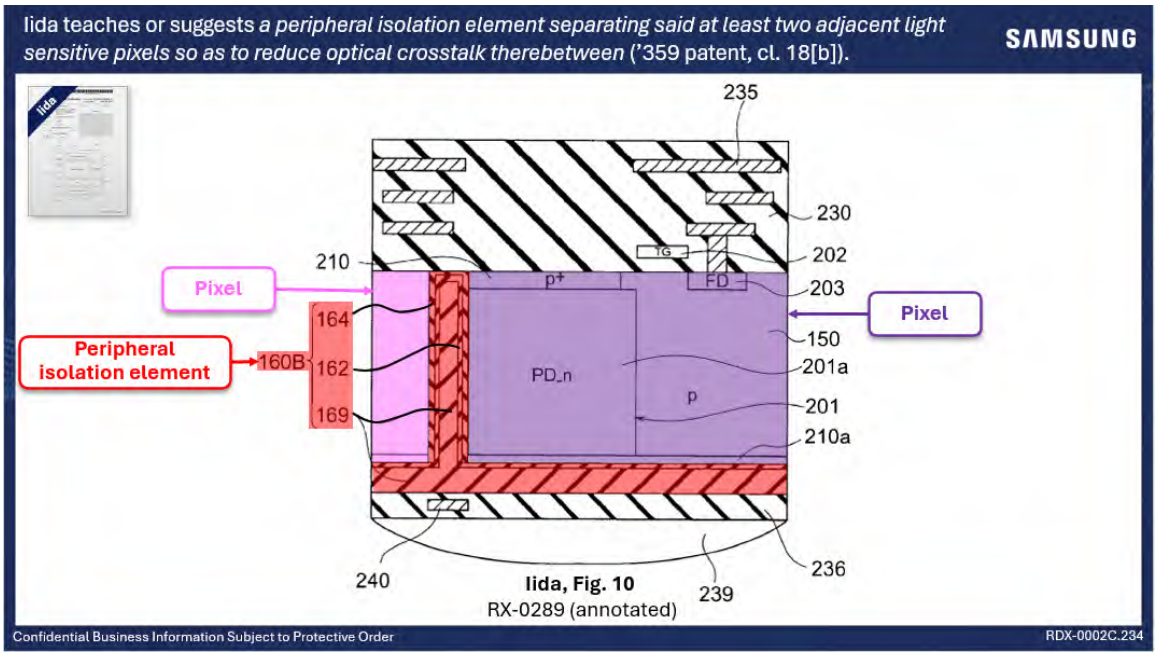
Q551 Let's turn to claim 18. Have you formed an opinion regarding claim 18?

A551 Yes. Iida teaches or suggests claim 18. As RDX-0002C.233 illustrates, limitations 18[a] and 18[c]-[g] are identical to limitations 1[a] and 1[c]-[g]. Iida teaches or suggests these limitations for the reasons discussed for the corresponding limitations of '359 patent (Ground 1), claim 1. The only limitation not identical to a limitation of claim 1 is limitation 18[b].

1. Limitation 18[b]

Q552 Limitation 18[b] is *a peripheral isolation element separating said at least two adjacent light sensitive pixels so as to reduce optical crosstalk therebetween*. Does Iida satisfy this limitation?

A552 Yes. As discussed for '359 patent (Ground 1), limitation 1[b], Iida discloses a *peripheral isolation element* (pixel separation structure 160B). As RDX-0002C.234 illustrates, pixel separation structure 160B *separates said at least two adjacent light sensitive pixels* as it "is provided between adjacent pixels in a silicon substrate 150 in which photodiodes 201 … are formed." Iida, [0081]. Iida further discloses that pixel separation structure 160B *reduces optical crosstalk* between said adjacent pixels. *See* Iida, [0102] ("Optical crosstalk is reduced by each pixel separation structure as described above."), [0101]-[0108] (detailing how pixel separation structure 160B reduces optical crosstalk between adjacent pixels).



Q553 Are you aware of Dr. Mansoorian's argument that Iida does not disclose or render obvious *a peripheral isolation element*?

A553 Yes. Dr. Mansoorian opines that Iida does not disclose or render obvious this limitation for the same reasons he provides with respect to limitation 1[b]. RX-0911C, ¶697. I disagree and note this is not a theory presented in SiOnyx's contentions. RX-0606C.471.

Q554 Why do you disagree?

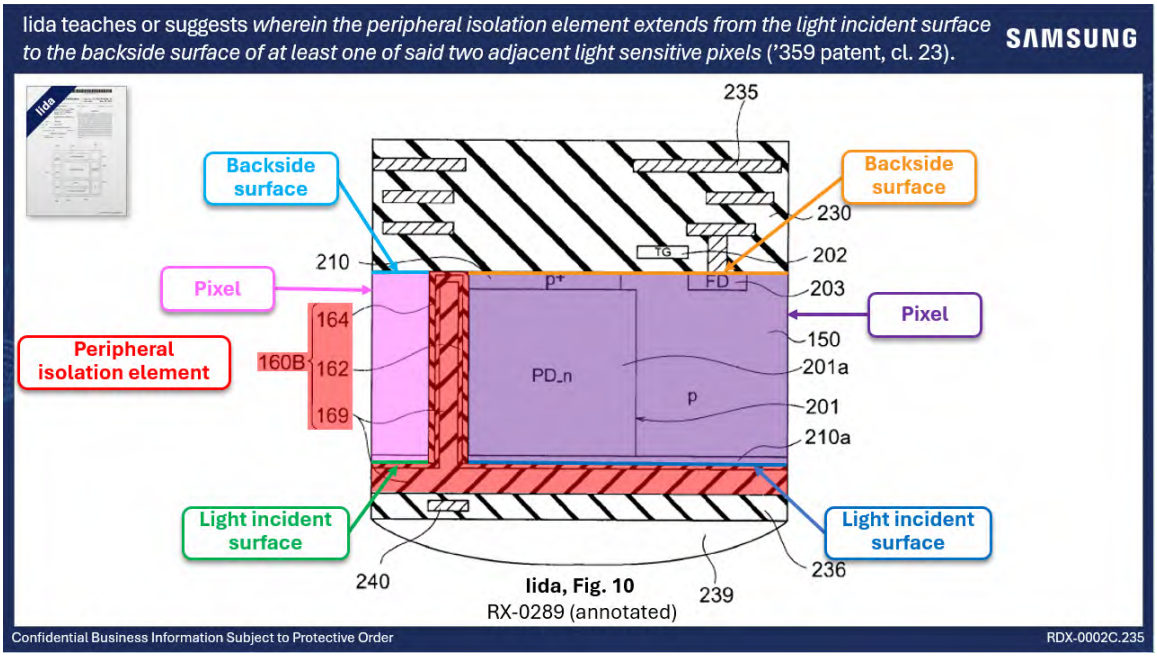
A554 I disagree for the same reasons I provided with respect to limitation 1[b].

d. Claim 23

Q555 Let's turn to claim 23, which is *[t]he device of claim 18, wherein the peripheral isolation element extends from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels*. Does Iida satisfy this limitation?

A555 Yes. Iida teaches or suggests this limitation. Dr. Mansoorian has not disputed this.

Iida discloses that its pixel separation structure 160B "has a trench that penetrates through the silicon substrate 150 from the back side to the front face side." Iida, [0081]. As discussed for '359 patent (Ground 1), limitation 1[a], the interface between the pixel and the horizontal portion of negative fixed charge film 162 is the pixel's *light incident surface*, and the interface between the pixel and the interlayer insulating film 230 is the pixel's *backside surface*. As RDX-0002C.235 illustrates, pixel separation structure 160B *extends* from the pixel's *light incident surface* (162-210a interface) to the pixel's *backside surface* (230-150 interface).



B. Hwang-based Grounds

Q556 Let's turn to your Hwang-based opinions. Can you please summarize your anticipation and obviousness opinions for the '359 patent based on Hwang?

A556 My Hwang-based opinions are divided into two grounds. Ground 2 is that Hwang anticipates, or at least renders obvious, claims 1, 18, and 23. Ground 3 is that Hwang and Shinohara render obvious claims 1, 11, 18, and 23.

1. Ground 2: Hwang Anticipates, or at Least Renders Obvious, Claims 1, 18, and 23

a. Claim 1

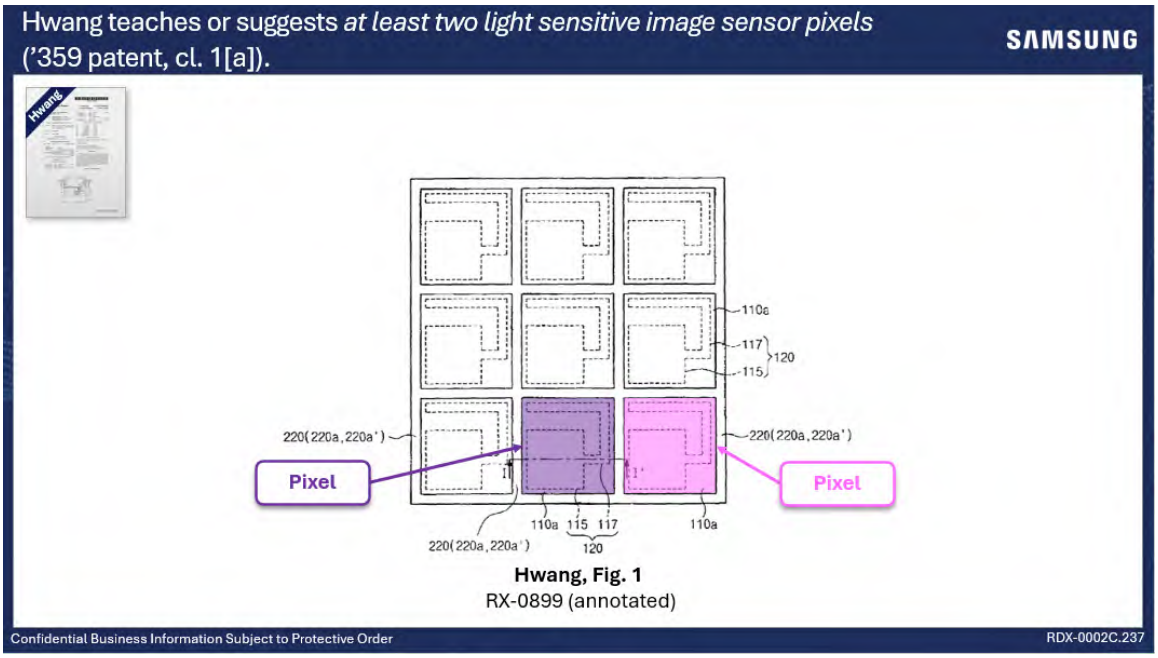
1. Limitation 1[a]

Q557 Let's start with your Ground 2 opinions that Hwang anticipates, or at least renders obvious, claims 1, 18, and 23. Claim 1's first limitation, 1[a], is relatively long, so let's take it in parts. The first element is *at least two adjacent light sensitive image sensor pixels*. Does Hwang satisfy this element?

A557 Yes. Hwang teaches or suggests *at least two adjacent light sensitive image sensor pixels*. Dr. Mansoorian has not disputed this.

I understand that the ALJ construed *light sensitive image sensor pixel* to have its plain and ordinary meaning. Order No. 36 at 27. Hwang discloses an image sensor comprising *at least two adjacent light sensitive image sensor pixels* under that phrase's plain and ordinary meaning, which I consider to be portions of a device that convert light into electrical signals. Hwang discloses an image sensor comprising "a plurality of pixel semiconductor patterns 110*a* … arranged two-dimensionally in rows and columns." Hwang, 5:52-59. As RDX-0002C.237 illustrates, Hwang's Figure 1 shows two adjacent pixels, which I have annotated in pink and purple.

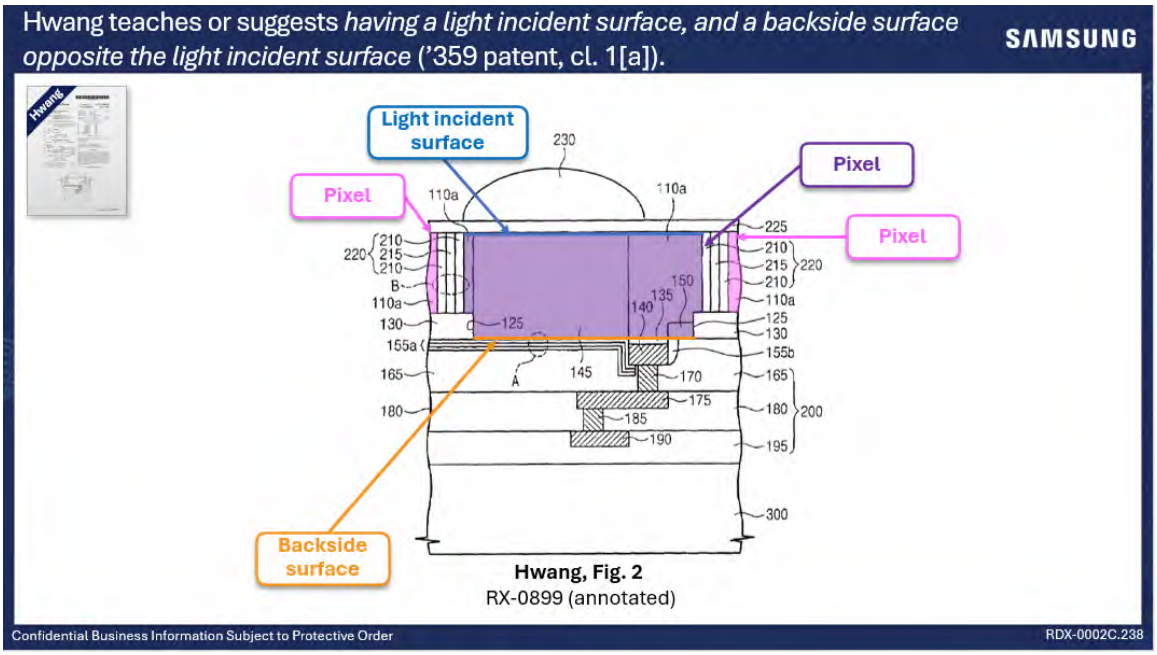
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Each pixel includes a photodiode. Hwang, 5:57-58 ("Each pixel semiconductor pattern 110*a* has a photodiode 145 disposed therein."). "A photodiode is a representative type of light receiver. When external light is incident on a depletion region in the photodiode, electron-hole pairs are generated, and the external light is converted to electrical signals." Hwang, 1:23-29. Although Hwang calls element 145 a "photodiode," POSITAs would understand that the photodiode encompasses more than just element 145 and would further encompass the surrounding pixel semiconductor patterns 110*a*. As Hwang explains, the photodiode comprises a junction created between differently doped semiconductor regions. *See* Hwang, 5:52-6:6 ("photodiodes 145 form a PN junction with the pixel semiconductor pattern 110*a*"); *see also* Haddad188, 8:15-19 ("[a] photosensitive pixel can include a semiconductor substrate having multiple doped regions forming at least one junction"). Accordingly, each of Hwang's pixels is a *light sensitive image sensor pixel*.

Q558 Limitation 1[a]'s second element is *having a light incident surface, and a backside surface opposite the light incident surface*. Does Hwang satisfy this element?

A558 Yes. As RDX-0002C.238 illustrates, each pixel in Hwang has *a light incident surface, and a backside surface opposite the light incident surface*.



Pixel semiconductor pattern 110*a*'s "second surface" is *a light incident surface*. *See* Hwang, 8:17-22 ("A color filter 225 is disposed on the second surface of the pixel semiconductor pattern 110*a*, and a micro lens 230 that covers the photodiode 145 is disposed on the color filter 225. External light passes through the micro lens 230 and the color filter 225, and is incident on the second surface of the photodiode 145.").

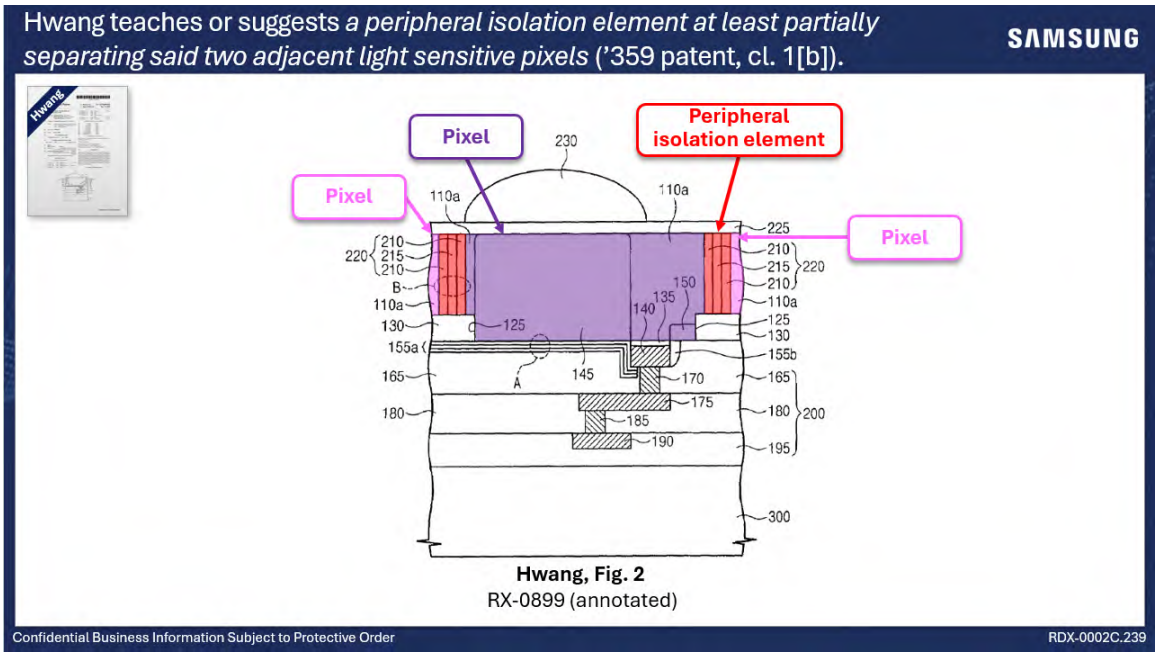
Pixel semiconductor pattern 110*a*'s "first surface" is *a backside surface opposite the light incident surface*. The first surface is opposite the second surface. *See* Hwang, 6:37-40 ("The pixel semiconductor patterns 110*a* have first and second surfaces in parallel, i.e., that face one another…. [T]he first surface … is more proximate to the substrate 300 than is the second surface."), 6:63-65 ("first surface of the photodiode 145 is coplanar with the first surface of the pixel substrate pattern 110*a*"), 7:40-42 ("first surface of the floating doped region 150 shares the same surface with the first surface of the pixel semiconductor pattern 110*a*").

2. Limitation 1[b]

Q559 Limitation 1[b] is *a peripheral isolation element at least partially separating said two adjacent light sensitive pixels*. Does Hwang satisfy this limitation?

A559 Yes. Hwang includes an *isolation element*: "sidewall multi-layered reflection layer 220." Hwang, 6:7. As RDX-0002C.239 illustrates, Hwang's sidewall multi-layered reflection layer 220 is *peripheral* because it "is provided between the side walls of the pixel semiconductor patterns 110*a*." Hwang, 6:7-9. Layer 220 *at least partially separates the adjacent light sensitive pixels*, as it "is interposed between a pair of neighboring pixel semiconductor patterns 110*a*" to "minimize[]" "the occurrence of interference between neighboring pixels." Hwang, 10:10-18. *See* Hwang, 6:19-23 ("layer 220 can be disposed along the boundaries of all of the pixel semiconductor patterns 110*a*, and all of the pixel semiconductor patterns 110*a* can thus be separated by the sidewall multi-layered reflection

layer 220"), 10:23-26 ("sidewall multi-layered reflection layer 220 minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels"). Dr. Mansoorian agrees that layer 220 physically separates the adjacent pixels. *See* RX-0911C, ¶713 (acknowledging that Hwang's disclosures "show that the 'multi-layered reflection layer' is *physically* located between adjacent pixels").



Q560 Are you aware of Dr. Mansoorian's argument that Hwang does not disclose or render obvious this limitation because layer 220 allegedly "fails to provide meaningful isolation"?

A560 Yes. Dr. Mansoorian opines that this limitation is not met because Hwang's multi-layered reflection layer 220 "does not provide meaningful optical or electrical isolation." RX-0911C, ¶¶712-716. I disagree and note this is not a theory presented in SiOnyx's contentions. RX-0606C.482.

Q561 Why do you disagree?

A561 Limitation 1[b] only requires that the peripheral isolation element "at least partially separate[] the adjacent light sensitive pixels"; it does not require that the element provide "optical isolation" or "electrical isolation." Instead, separate claims of the '359 patent that depend on claim 1 require that the peripheral isolation element provide optical isolation or electrical isolation. *See, e.g.*, '359 patent, claims 39 ("wherein said peripheral isolation element optically isolates …."), 40 ("wherein said peripheral isolation element electrically isolates…."), 68 ("wherein the peripheral isolation element is further configured to optically isolate…."), 69 ("wherein the peripheral isolation element is further configured to electrically isolate….").

Q562 Are there any other reasons why you disagree with Dr. Mansoorian?

A562 Yes. Even if limitation 1[b] required that the peripheral isolation element provide "optical isolation" and/or "electrical isolation," POSITAs would recognize that Hwang's multi-layered reflection layer 220 provides both of those forms of isolation. First, Hwang expressly discloses that layer 220 provides optical isolation between adjacent pixels. *See, e.g.*, Hwang, 10:10-18 (disclosing that layer 220 is interposed between adjacent pixels so that "the occurrence of interference between neighboring pixels can be minimized"); 10:19-27 (disclosing that layer 220 "minimizes incidence of the light (reflected by the base multi-layered reflection layer 155a at the first and second boundary surfaces) on the photodiode 145 within another pixel semiconductor pattern 110a. In other words, … layer 220 minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels. Therefore, interference of the image sensor can be minimized, and image distortion can be minimized."); 10:28-40 (describing how layer 220 reflects light incident on it such that the incidence of light reflected from certain surfaces of one pixel "on neighoring pixels can be minimized"); 15:42-48 (describing how the sidewall multi-layered reflection layer "encloses the sidewalls of the pixel semiconductor patterns forming the photodiode" and "minimize[s]" incidence of light "on neighboring pixels").

I understand that Dr. Mansoorian opines that layer 220 "does not effectively optically isolate adjacent pixels" because "most, if not all" of the light exiting the "light sensitive portions" of a pixel toward an adjacent pixel is likely to be absorbed by "inactive, P-doped portions[] of the pixel semiconductor pattern" before the light reaches layer 220. RX-0911C, ¶¶715-716. I disagree. POSITAs would readily understand, consistent with Hwang's clear disclosures already identified, that at least some if not all light incident on the light sensitive portion of one of Hwang's pixels would reach layer 220 and cross over into the light sensitive portion of an adjacent pixel if not reflected by layer 220. Dr. Mansoorian appears to concede this, as he opines only that "most" (not "all") light would not reach layer 220 and has acknowledged that some light would reach antireflection layers at the pixel boundary and be reflected back. *See* RX-0535C (Mansoorian), 139:17-141:13. I also note that Dr. Mansoorian's argument that light exiting one pixel's active portion and traveling toward an adjacent pixel "must first pass through a … large, inactive, P-doped portion" (or a similar inactive portion of the adjacent pixel before reaching the adjacent pixel's active region) incorrectly assumes that Hwang's figures are drawn to scale. Dr. Mansoorian has since acknowledged that those figures are not drawn to scale. *See* RX-0535C (Mansoorian), 160:14-17. Regardless, for the same reasons I explained regarding limitation 1[a] of the '714 patent, light takes numerous pathways, and POSITAs would readily recognize that many of those pathways would avoid what Dr. Mansoorian alternatively refers to as "dead zones" and "inactive, P-doped portions" and be reflected by layer 220 back into the pixel. *See* RX-0535C (Mansoorian), 89:6-90:14.

Second, Hwang discloses that layer 220 provides electrical isolation between adjacent pixels. POSITAs would know that pixel separation structures such as Hwang's sidewall multi-layered reflection layer electrically isolate adjacent light sensitive image sensor pixels—i.e., prevent electrical crosstalk between such pixels. *See, e.g.*, Hirigoyen, [0006] ("Electrical crosstalk occurs when an electron is generated in one photosite and migrates to another photosite. Isolation regions are therefore commonly provided between

photosites to prevent … electrical crosstalk."); [0064] (because "adjacent pixels are physically isolated from each other … the leakage of charge in the photodiode PD into an adjacent pixel can be substantially prevented"). The fact that, as shown in Figure 2, layer 220 sits atop a "device isolation pattern 130" whose purpose is electrical insulation below layer 220 further confirms that layer 220 as well provides electrical isolation. *See* Hwang, 11:61-62 ("As shown, the sidewall multi-layered reflection layer 220 can contact the device isolation pattern 130."); Hwang, 12:29-31 ("[T]he device isolation pattern 130' can further include a device isolation insulating material, such as oxide material").

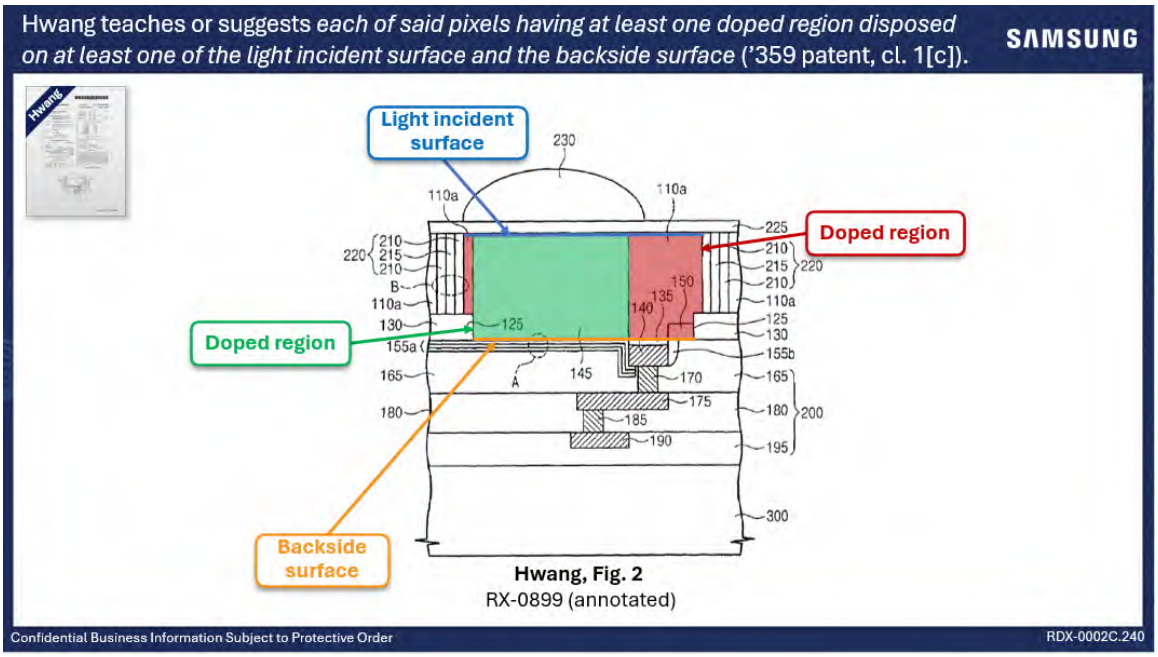
Moreover, as discussed below regarding claim 23, it would have been obvious to POSITAs to modify the embodiment of Hwang's imager device shown in Figure 2 so that layer 220 would extend from the light incident surface to the backside surface of the pixel. As discussed, POSITAs would have been motivated to do so, among other reasons, to further minimize the electrical crosstalk that results from charges migrating under a sidewall from one pixel into an adjacent pixel. POSITAs would therefore understand that layer 220 in Hwang's modified embodiment would *electrically isolate the adjacent pixels*.

3. Limitation 1[c]

Q563 Limitation 1[c] is *each of said pixels having at least one doped region disposed on at least one of the light incident surface and the backside surface*. Does Hwang satisfy this limitation?

A563 Yes. Each pixel in Hwang *ha[s] at least one doped region disposed on at least one of the light incident surface and the backside surface*. Dr. Mansoorian has not disputed this. Hwang discloses that "pixel semiconductor patterns 110*a* are doped with a first conductive dopant" and that "photodiodes 145 are regions doped with a second conductive dopant." Hwang, 5:58-60.

Doped regions 110*a* and 145 are both *disposed on at least one of the light incident surface and the backside surface*. As RDX-0002C.240 illustrates, doped regions 110*a* and 145 are disposed on Hwang's "first" and "second" surface. As explained for '359 patent (Ground 2), limitation 1[a], Hwang's "second surface" is a *light incident surface* and Hwang's "first surface" is a *backside surface*.



4. Limitation 1[d]

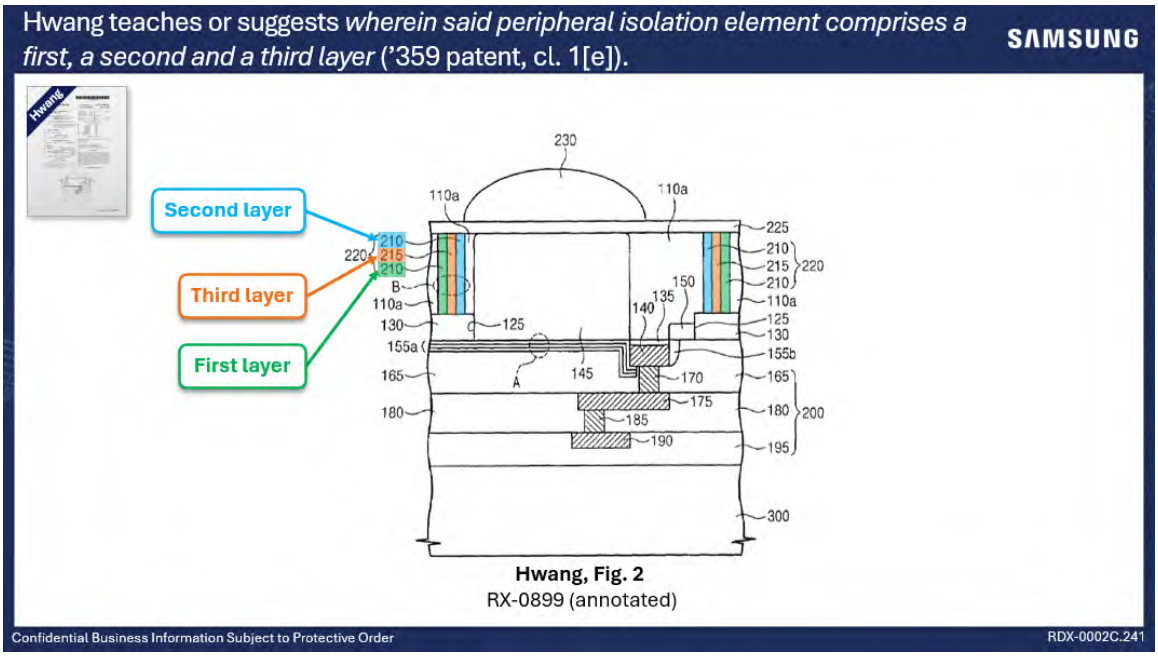
Q564 Limitation 1[d] is *wherein the peripheral isolation element comprises at least two materials having different indices of refraction*. Does Hwang satisfy this limitation?

A564 Yes. Hwang's sidewall multi-layered reflection layer 220 *comprises at least two materials having different indices of refraction*. Dr. Mansoorian has not disputed this. Hwang discloses that layer 220 includes "a first sidewall reflection layer 210 and a second sidewall reflection layer 215," Hwang, 9:58-60; that "layer 210 can be a silicon oxide layer" and that "layer 215 can be a silicon layer," Hwang, 10:2-5; that its silicon oxide "has a refractive index of approximately 1.46," Hwang, 9:28-29; that its silicon has "a refractive index of approximately 4," Hwang, 9:29-30; and that "[t]he refractive index of the first sidewall reflection layer 210 is different from the refractive index[] of … the second sidewall reflection layer 215," Hwang, 9:60-63.

5. Limitation 1[e]

Q565 Limitation 1[e] is *wherein said peripheral isolation element comprises a first, a second and a third layer*. Does Hwang satisfy this limitation?

A565 Yes. As RDX-0002C.241 illustrates, Hwang's sidewall multi-layered reflection layer 220 *comprises a first, a second and a third layer*: "second sidewall reflection layer 215" (*third layer*) "interposed between two first sidewall reflection layers 210 (*first* and *second* layers). Dr. Mansoorian has not disputed this.



6. Limitation 1[f]

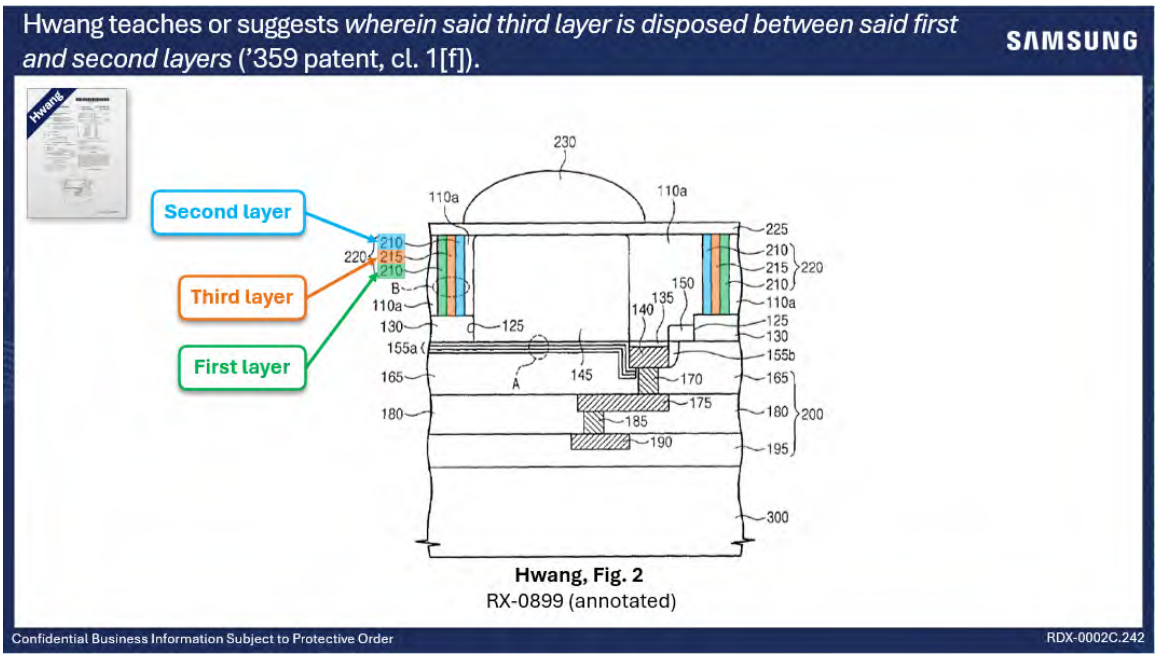
Q566 Limitation 1[f] is *wherein said third layer is disposed between said first and second layers*. Does Hwang satisfy this limitation?

A566 Yes. Hwang teaches or suggests *wherein said third layer is disposed between said first and second layers*. Dr. Mansoorian has not disputed this.

As explained in the Terms Remaining in Dispute, I understand that the parties proposed constructions for limitation 1[f] as a whole. Hwang satisfies limitation 1[f] under either construction.

Q567 How does Hwang satisfy this limitation?

A567 As RDX-0002C.242 illustrates, the *third layer* of sidewall multi-layered reflection layer 220 (layer 215) *is disposed between the first layer* (layer 210 on its left) *and the second layer* (layer 210 on its right). *See also* Hwang, 10:17-17, 10:48-20 ("second sidewall reflection layer 215 interposed between two first sidewall reflection layers 210").



7. Limitation 1[g]

Q568 Limitation 1[g] is *wherein each of said first and second layer exhibits an index of refraction less than an index of refraction of said third layer*. Does Hwang satisfy this limitation?

A568 Yes. Each of the *first layer* and *second layer* of Hwang's sidewall multi-layered reflection layer 220 *exhibits an index of refraction less than an index of refraction of said third layer*. Hwang discloses that the refractive index of the first sidewall reflection layer 210 (*first* and *second layers*) "can be lower than the refractive index[] of" the second sidewall reflection layer 215 (*third layer*). Hwang, 9:63-66. Dr. Mansoorian has not disputed this.

b. Claim 18

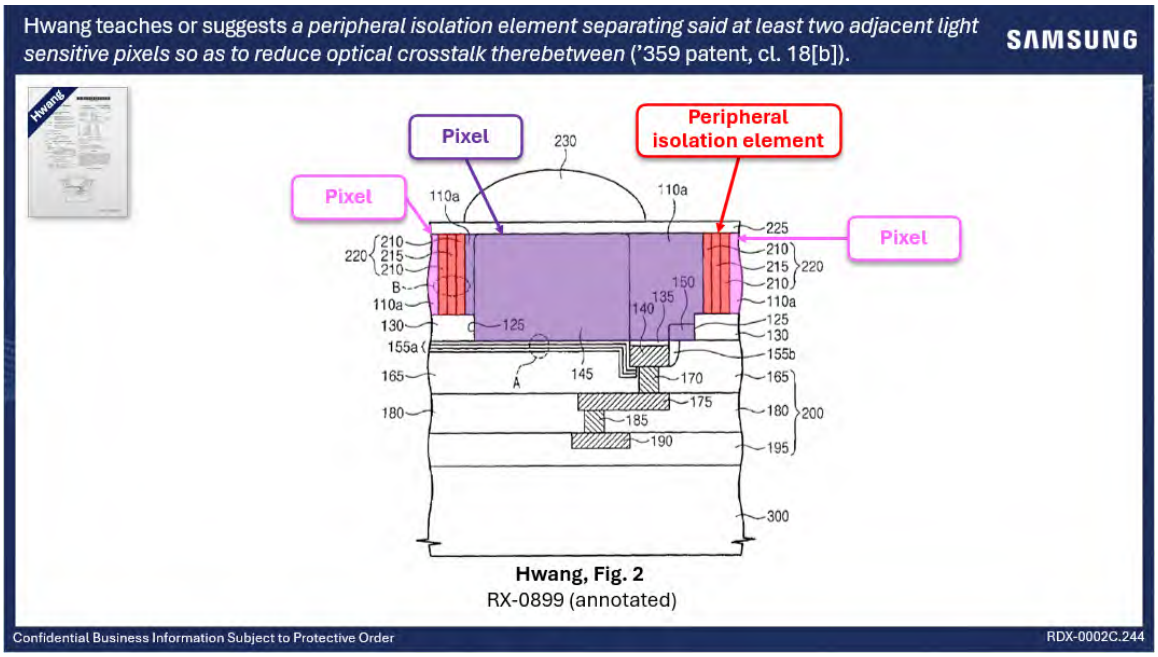
Q569 Let's turn to claim 18. Have you formed an opinion regarding claim 18?

A569 Yes. Hwang teaches or suggests claim 18. As RDX-0002C.243 illustrates, limitations 18[a] and 18[c]-[g] are identical to limitations 1[a] and 1[c]-[g]. Hwang teaches or suggests these limitations for the reasons discussed for the corresponding limitations of '359 patent (Ground 2), claim 1. The only limitation not identical to a limitation of claim 1 is limitation 18[b].

1. Limitation 18[b]

Q570 Limitation 18[b] is *a peripheral isolation element separating said at least two adjacent light sensitive pixels so as to reduce optical crosstalk therebetween*. Does Iida satisfy this limitation?

A570 Yes. As discussed for '359 patent (Ground 2), limitation 1[b], Hwang discloses a *peripheral isolation element* (sidewall multi-layered reflection layer 220). As RDX-0002C.244 illustrates, layer 220 *separates said at least two adjacent light sensitive pixels* because it "is interposed between a pair of neighboring pixel semiconductor patterns 110*a*." Hwang, 10:10-18. *See also* Hwang, 6:19-23 ("layer 220 can be disposed along the boundaries of all of the pixel semiconductor patterns 110*a*, and all of the pixel semiconductor patterns 110*a* can thus be separated by the sidewall multi-layered reflection layer 220"). Dr. Mansoorian agrees that layer 220 physically separates the adjacent pixels. *See* RX-0911C, ¶713 (acknowledging that Hwang's disclosures "show that the 'multi-layered reflection layer' is *physically* located between adjacent pixels").



Q571 Does sidewall multi-layered reflection layer 220 *reduce optical crosstalk* between adjacent pixels?

A571 Yes. Hwang discloses that layer 220 *reduces optical crosstalk* between said pixels. *See* Hwang, 10:10-18 (layer 220 interposed between adjacent pixels so that "the occurrence of interference between neighboring pixels can be minimized"); 10:19-27 (layer 220 "minimizes incidence of the light (reflected by the base multi-layered reflection layer 155*a* at the first and second boundary surfaces) on the photodiode 145 within another pixel semiconductor pattern 110*a*. In other words, … layer 220 minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels. Therefore, interference of the image sensor can be minimized, and image distortion can be minimized."), 10:28-40 (describing how layer 220 reflects light incident on it such that the

incidence of light reflected from certain surfaces of one pixel "on neighboring pixels can be minimized"), 15:42-48 (describing how layer 220 "encloses the sidewalls of pixel semiconductor patterns forming the photodiode" and "minimize[s]" incidence of light "on neighboring pixels").

Q572 Are you aware of Dr. Mansoorian's argument that Hwang does not disclose or render obvious *a peripheral isolation element separating said at least two adjacent light sensitive pixels so as to reduce optical crosstalk therebetween*?

A572 Yes. Dr. Mansoorian notes that this limitation is "effectively the same limitation present in claim 1(b)" and opines that Hwang does not disclose or render obvious the limitation for the same reasons he provides with respect to limitation 1[b]. RX-0911C, ¶726. I disagree and note this is not a theory presented in SiOnyx's contentions. RX-0606C.486.

Q573 Why do you disagree?

A573 I disagree for the same reasons I provided with respect to limitation 1[b].

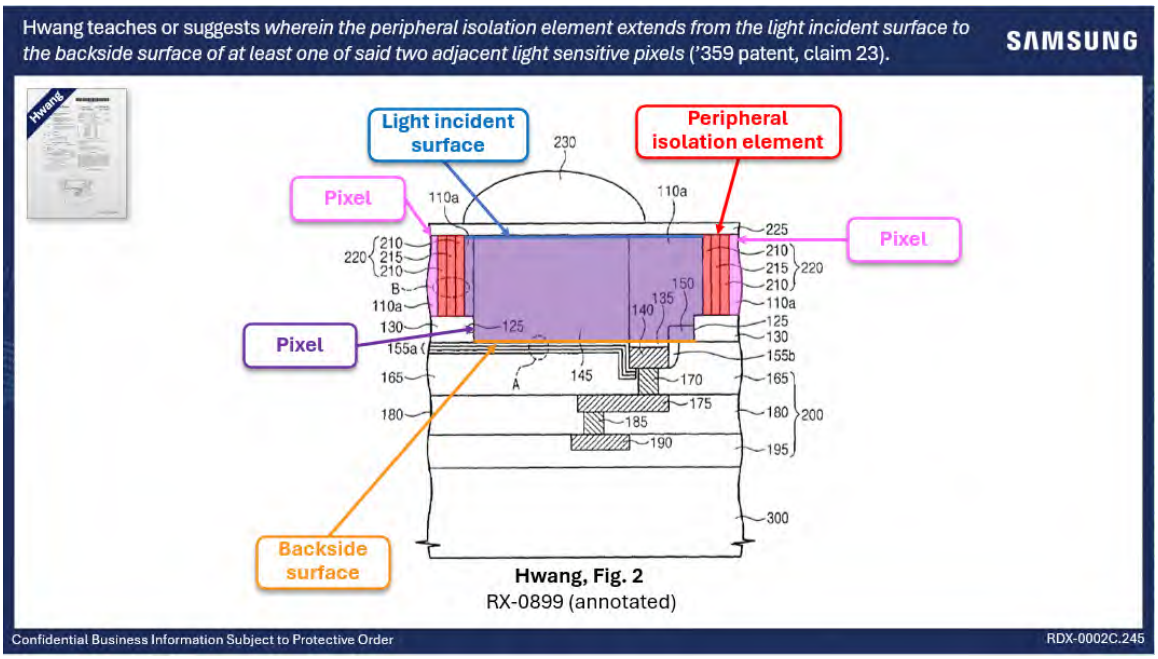
c. Claim 23

Q574 Let's turn to claim 23, which is *[t]he device of claim 18, wherein the peripheral isolation element extends from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels*. Have you formed an opinion regarding this limitation?

A574 Yes. Hwang teaches or suggests this limitation. Dr. Mansoorian has not disputed this.

As RDX-0002C.245 illustrates, Hwang's sidewall multi-layered reflection layer 220 extends from Hwang's "first surface" to isolation pattern 130, which extends to Hwang's "second surface." *See also* Hwang, 10:61-62 (layer 220 "can contact the device isolation pattern 130"). As discussed for '359 patent (Ground 2), limitation 1[a], Hwang's "second" and "first surfaces" are the *light incident* and *backside surfaces*, respectively.

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Q575 Does sidewall multi-layered reflection layer 220 satisfy this limitation?

A575 The FDTI structures that Dr. Foty opines infringe this limitation have DTI pixel separation structures that are similarly situated above an STI structure. *See* RX-0905C, ¶¶950-956, 974-979; JX-0036C, 89:12-90:14 (discussing "BDDP poly-depo scheme"); RX-0490C.29; RX-0485C.10, 22 (showing "high-level depiction"). In view of Dr. Foty's interpretation and application of this limitation in his infringement opinions, layer 220 *extends substantially* from the *light incident surface to the backside surface of each pixel*.

Q576 Do you have any other opinions as to why Hwang satisfies this claim?

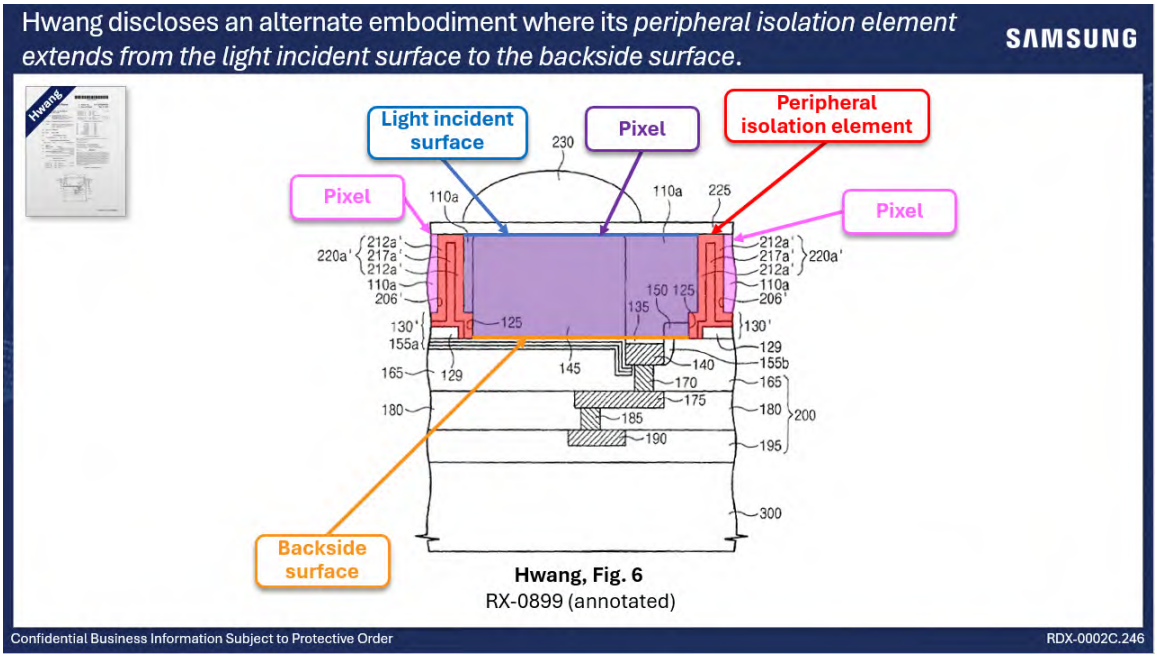
A576 Yes. It is also my opinion that modifying layer 220 so that it extends *completely* from the *light incident surface to the backside surface* would have been obvious. Hwang discloses that layers 210 of layer 220 are formed by etching grooves 205 in semiconductor layer 110 then filling grooves 205 with a material such as SiO_2:

> Referring to Fig. 13, the exposed second surface of the semiconductor layer 110 can selectively be etched to form a plurality of grooves 205…. Referring to Fig. 14, the grooves 205 are filled with a predetermined material…. The sidewall multi-layered reflection layer 220 includes a material layer 210 filling the grooves 205 and the residual portion 215 of the semiconductor layer 110 disposed between the grooves 205. The material layer 210 filling the grooves 205 corresponds to the first sidewall reflection layer 210 described with reference to Figs. 1 through 4, and the residual portion 215 corresponds to the second sidewall reflection layer 215 described with reference to Figs. 1 through 4.").

Hwang, 12:42-61. Accordingly, etching the grooves 205 so that they extend completely from the *light incident surface* (Hwang's "second surface") *to the backside surface* (Hwang's "first surface") would have been obvious.

Q577 Are there any other reasons why modifying Hwang in this manner would have been obvious?

A577 Yes. As RDX-0002C.246 illustrates, Hwang discloses in its Figure 6 an alternate embodiment where sidewall multi-layered reflection layer 220*a*' is "extended into trench 125" and thus extends from the *light incident surface* (Hwang's "second surface") all the way to the *backside surface* (Hwang's "first surface"). Hwang, 12:25-26 ("first and second sidewall reflection layers 212*a*' and 217*a*' can be extended into trench 125"); *see also* Hwang, 11:66-12:2 ("sidewall multi-layered reflection layer 220*a*' includes a first sidewall reflection layer 212*a*' and a second sidewall reflection layer 217*a*' having different refractive indexes.").



Q578 Would POSITAs have been motivated to make this modification?

A578 Yes. POSITAs would have been motivated by Hwang's alternate embodiment to modify Hwang's sidewall multi-layered reflection layer 220 to *extend from the light incident surface to the backside surface*. POSITAs would understand that such a modification would increase the device's "absorption efficiency" and decrease "interference between neighboring pixels." Hwang, 10:28-40. POSITAs would have known that a gap in the sidewall reflection layer between the *light incident surface* and the *backside surface* would allow some charges to migrate under the sidewall reflection layer into an adjacent pixel, resulting in unwanted electrical crosstalk. *See* Roy, [0039] ("Usually, trench 11 has a depth ranging between 0.3 and 0.7 µm. Thereby, this trench limits the crosstalk without however completely canceling it since electron/hole pairs may be photogenerated down to a depth

from 3 to 10 μm…. Electrons can thus pass under trench 11 from the N area of a photodiode to the N area of a neighboring photodiode.").

Q579 Would POSITAs have reasonably expected success in making this modification?

A579 Yes. Extending layer 220 was a known technique—disclosed by Hwang itself in connection with an alternate embodiment—to improve a similar device in the same way Hwang contemplated for its alternate embodiment. Furthermore, POSITAs would have understood that extending a single trench for layer 220—instead of creating separate trenches 205 and 125 as taught for Figure 2's embodiment—would simplify the manufacturing process by reducing the number of manufacturing steps. *See* Iida, [0097] (teaching forming peripheral isolation element structures "at the same time" to "simplify the manufacturing procedures and lower the production costs"); Roy, [0079] (teaching that forming peripheral isolation element by filling "trench(es) … with identical materials" provides "advantage of … manufacturing simplicity").

2. Ground 3: Hwang and Shinohara Render Obvious Claims 1, 11, 18, 23, and 24

Q580 Let's turn to your Ground 3 opinions. Can you please summarize your Ground 3 opinions?

A580 In my opinion Hwang and Shinohara render obvious claims 1, 11, 18, and 23. As explained for Ground 2, Hwang anticipates, or at least renders obvious, claims 1, 18, and 23. Those opinions are equally applicable to my Ground 3 opinions regarding Hwang and Shinohara, which further render obvious claim 11.

a. Claim 11

Q581 Let's turn to claim 11, which is *[t]he device of claim 1, wherein the peripheral isolation element comprises any of aluminum oxide and hafnium oxide*. Have you formed an opinion regarding this limitation?

A581 Yes. Hwang and Shinohara render claim 11 obvious. Shinohara discloses using Al_2O_3 as an insulating layer in a pixel separation structure. *See* Shinohara, [0091] ("[A]s the insulating film 69, an insulating film having a negative fixed charge may also be used. As the insulating film having a negative fixed charge, for example, there may be used a film of … dialuminum trioxide (Al_2O_3).").

It would have been obvious to POSITAs to use Shinohara in selecting materials for Hwang's sidewall multi-layered reflection layer 220 (*peripheral isolation element*), for the first sidewall reflection layer 210 (*first* and *second* layers). Specifically, POSITAs would have been motivated to use Al_2O_3 as a pixel separation structure material, as Shinohara teaches, in Hwang's layer 210 and would have reasonably expected success in doing so.

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Q582 Why would POSITA look to Shinohara to modify Hwang?

A582 Hwang and Shinohara are both directed to the same field of endeavor: imager devices comprising light-sensitive pixels. *See* Hwang, Abstract, 1:14-18; Shinohara, [0051]. Both references similarly seek to minimize crosstalk by inserting trench-type separation structures between adjacent pixels. *See* Hwang, 1:31-2:61, 10:6-60; Shinohara, [0011]-[0013], [0017] ("forming a trench … in a semiconductor substrate … filling a semiconductor layer in the trench by an epitaxial growth to form an element isolation region"), [0021], [0090].

As discussed for '359 patent (Ground 2), limitation 1[e], Hwang discloses a pixel separation structure comprising at least two materials having different refractive indices: first sidewall reflection layer 210 (comprising silicon oxide "with a refractive index of approximately 1.46") with a refractive index lower than the refractive indices of pixel semiconductor pattern 110*a* and second sidewall reflection layer 215 (both comprising silicon "with a refractive index of approximately 4"). *See* Hwang, 9:28-31, 9:63-10:4. POSITAs would understand that the interface between Si and SiO_2 existing in Hwang's pixel separation structure generates dark current and causes the signal-to-noise ratio to deteriorate. *See* Iida, [0007]. Surface recombination contributes to dark current, which reduces image quality. *See* Iida, [0007]; Hirigoyen, [0006] ("performance of an image sensor depends on many factors, such as … dark current (the amount of current generated even when the photosites are not receiving incident light rays)"). Accordingly, POSITAs seeking to implement Hwang would be motivated to look for guidance to identify potentially more suitable materials for the first sidewall reflection layer 210 in Hwang's sidewall multi-layered reflection layer (*peripheral isolation element*), to further improve Hwang's absorption and sensitivity. *See* JX-0027C (McKee), 82:13-83:8 (describing different materials, such as dielectrics or metals that can be used as materials to optically isolate a pixel).

Q583 Why would POSITAs consider Shinohara for this purpose?

A583 POSITAs would look to Shinohara for this purpose because, as discussed, Hwang and Shinohara are both directed to the design of pixel separation structures in imager devices and because Shinohara teaches suitable materials for pixel separation structure layers. *See* Shinohara, [0091].

POSITAs would be particularly motivated to look to Shinohara because Shinohara teaches that its trench separation structure materials help reduce optical and electrical crosstalk. *See* Shinohara, [0008] (stressing that "it is important to suppress the occurrence of color mixture caused by leakage of charge (such as electron) photoelectrically converted in the vicinity of the rear surface side into an adjacent pixel"), [0094] ("since the filled insulated film 69 has a refractive index different from that of the p-type semiconductor layer 43, even if inclined incident light is incident thereon, the light is not photoelectrically converted in an adjacent pixel after passing through the element isolation region 68"). Shinohara further explains that its teachings are directed, in part, to overcome shortcomings in the prior art where the formation of trench-type pixel separation structures results in white spots and dark current. *See* Shinohara, [0011] ("element isolation region which

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physically isolates pixels is formed by a trench [method] in a rear surface of a substrate so as to suppress leakage of charge into an adjacent pixel"). As an additional benefit, Shinohara teaches that its disclosures enable a more efficient manufacturing process. *See, e.g.*, Shinohara, [0088]-[0089], [0093], [0096]. Thus, several important performance objectives such as achieving high levels of absorption and efficiency would motivate POSITAs to look to Shinohara in selecting the material for the insulating film in Hwang's pixel separation structure to minimize electrical and optical crosstalk and dark current. *See* JX-0017C (Sickler), 41:7-8 (explaining that dark current is harmful should be minimized).

Q584 Why would POSITAs be motivated to use Shinohara's Al_2O_3 for the outermost sidewall reflection layers of Hwang?

A584 POSITAs would have known that Al_2O_3, as taught by Shinohara as an insulating material for pixel separation structures, exhibits low surface recombination velocity—lower than that of the SiO_2 used in Hwang's first sidewall reflection layer 210—and achieves high-quality chemical passivation. *See* RX-0311.1-3 (Saint-Cast); RX-0309.104 (Hoex). POSITAs would understand that, to get Al_2O_3's benefit of surface recombination properties as a negative fixed charge material, the Al_2O_3 should be in contact with the semiconductor (silicon) substrate—i.e., be used as the material for Hwang's first sidewall reflection layer 210. Additionally, Al_2O_3 can exhibit a refractive index of approximately 1.7, which is lower than the refractive index of "approximately 4" that Hwang discloses for its pixel semiconductor pattern 110*a* and second sidewall reflection layer 215, both of which are comprised of silicon. *See* Suzunaga, [0070] (disclosing a refractive index of 1.7 for its Al_2O_3); RX-0304.B-68 (CRC Handbook) (disclosing a refractive index of 1.76 for Al_2O_3); Hwang, 9:28-31, 9:60-10:5.

Accordingly, POSITAs would have been motivated to use an Al_2O_3 pixel separation structure layer, as Shinohara teaches, in place of Hwang's first sidewall reflection layer 210 to achieve better passivation and reduce surface recombination velocity along the sidewalls of Hwang's pixels.

Q585 Would POSITAs have reasonably expected success in making this combination?

A585 Yes. POSITAs would have reasonably expected success in making this combination. As discussed, Hwang and Shinohara both are directed to imager devices comprising light-sensitive pixels and specifically to the use of trench separation structures between adjacent pixels to reduce crosstalk. Given the similarities in structure and function of Hwang and Shinohara, POSITAs would have viewed building Hwang's pixel separation structure with Al_2O_3, as Shinohara teaches, as a simple design choice and the application of a known technique to improve a similar device in the way Shinohara teaches, to yield predictable results.

Q586 Are there any other reasons why POSITAs have reasonably expected success in making this combination?

A586 Yes. Further reinforcing POSITAs expectation of success, including Al_2O_3, as Shinohara teaches, would have involved routine manufacturing steps that Hwang and Shinohara

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already taught. *See* Hwang, 12:42-61; Shinohara, [0091] ("As a method for forming the insulating film having a negative fixed charge, for example, an atomic layer deposition (ALD) method or a metal-organic chemical vapor deposition (MOCVD) method may be used. When the insulating film having a negative fixed charge is used, one type of film or a laminate containing a plurality of types of films may be used."). Forming a layer of Al_2O_3 by deposition was well known to POSITAs since at least the 1990s. *E.g.*, Suzunaga, [0067] ("film having a high refractive index … may be for example, any one of … Al_2O_3"); RX-0477 (Lan); RX-0482 (Wang). The fabrication process would involve standard modules, standard techniques, and standard processes that would have been well within the scope of POSITAs' abilities. The technique for forming layers of materials such as silicon materials and dielectrics, including oxides, were well known to POSITAs. Fabrication processing techniques such as photolithography, etching deposition, and metallization, were well known, as were material properties such as refractive index, etch rate, and crystal quality.

Q587 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination because they would consider the combination unnecessary?

A587 Yes. Dr. Mansoorian opines that POSITAs would not use Shinohara's Al_2O_3 for the outermost sidewall reflection layers of Hwang because "Hwang's architecture – particularly the large meaningless fill factor – already mitigates the generation and effects of dark current in Hwang's device," citing his analysis of '714 patent, limitation 1[a]. RX-0911C, ¶¶ 720-21, 723-24. I disagree. As I explained for '714 patent (Ground 1), limitation 1[a] and '359 patent (Ground 2), limitation 1[b], Dr. Mansoorian's arguments about "large" dead zones or inactive p-doped areas incorrectly assume that Hwang's figures are drawn to scale. Dr. Mansoorian has since acknowledged that those figures are not drawn to scale. *See* RX-0535C (Mansoorian), 160:14-17. Moreover, even assuming for the sake of argument that Hwang's figures were drawn to scale, POSITAs would recognize that on one side of each of Hwang's pixels, the multilayered sidewall reflection layer 220 is located very close to the pixel's active region. *See, e.g.*, Hwang, Fig. 2 (element 145 positioned very close to layer 220 on its left-hand side). Therefore, POSITAs would understand that it would be important to mitigate the dark current generated in the vicinity of Hwang's pixel separation structure. As explained, POSITAs would understand that the interface between Si and SiO_2 existing in Hwang's pixel separation structure generates dark current and causes the signal-to-noise ratio to deteriorate. I understand that Dr. Mansoorian agrees. *See* RX-0535C (Mansoorian), 216:3-7.

Q588 Would it be obvious to use hafnium oxide in Hwang?

A588 Yes. Shinohara also discloses using "a film of hafnium oxide (HfO_2)" as an alternative to Al_2O_3 as a negative fixed charge material for its insulating film 69, Shinohara, [0091]. Accordingly, for the same reasons discussed regarding Al_2O_3, building Hwang with a pixel separation structure comprising a first sidewall reflection layer 210 made of hafnium oxide would have been obvious.

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C. Hirigoyen-based Grounds

Q589 Let's turn to your Hirigoyen-based opinions. Can you please summarize your anticipation and obviousness opinions for the '359 patent based on Hirigoyen?

A589 My Hirigoyen-based opinions are divided into two grounds. Ground 4 is that Hirigoyen anticipates, or at least renders obvious, claims 1, 18, and 23. Ground 5 is that Hirigoyen and Shinohara render obvious claims 1, 11, 18, and 23.

1. Ground 4: Hirigoyen Anticipates, or at Least Renders Obvious, Claims 1, 18, and 23

a. Claim 1

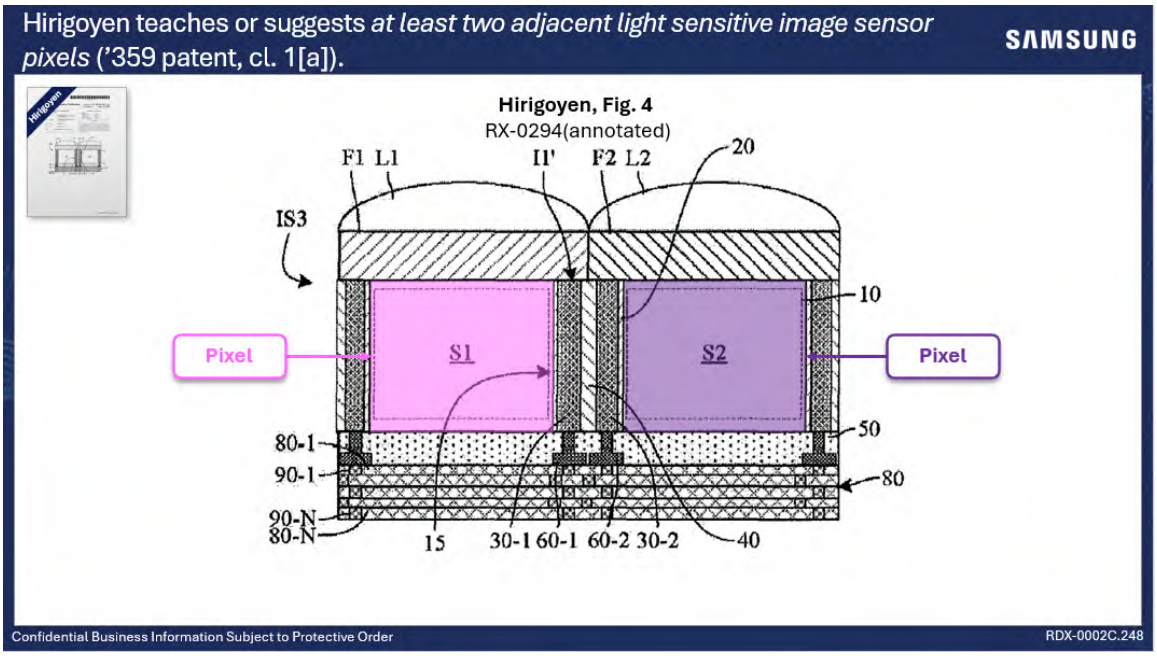
1. Limitation 1[a]

Q590 Let's start with your Ground 4 opinions that Hirigoyen anticipates, or at least renders obvious, claims 1, 18, and 23. Claim 1's first limitation, 1[a], is relatively long, so let's take it in parts. The first element is *at least two adjacent light sensitive image sensor pixels*. Does Hirigoyen satisfy this element?

A590 Yes. Hirigoyen teaches or suggests *at least two adjacent light sensitive image sensor pixels*. Dr. Mansoorian has not disputed this.

I understand that the ALJ construed *light sensitive image sensor pixel* to have its plain and ordinary meaning. Order No. 36 at 27. Hirigoyen discloses an imager device including *at least two adjacent light sensitive image sensor pixels* under that phrase's plain and ordinary meaning, which I consider to be portions of a device that convert light into electrical signals. As RDX-0002C.248 illustrates, Hirigoyen discloses an image sensor including "at least two photosites separated by an isolation region." Hirigoyen, [0002]; *see also* Hirigoyen, [0004] ("photosites are generally arranged in a matrix"), Fig. 3 (depicting a matrix), [0033]-[0034]. As RDX-0002C.248 illustrates, photosites S1 and S2 are formed in the semiconductor substrate 10. *See* Hirigoyen, [0017] ("forming at least two photosites in a semiconductor substrate").

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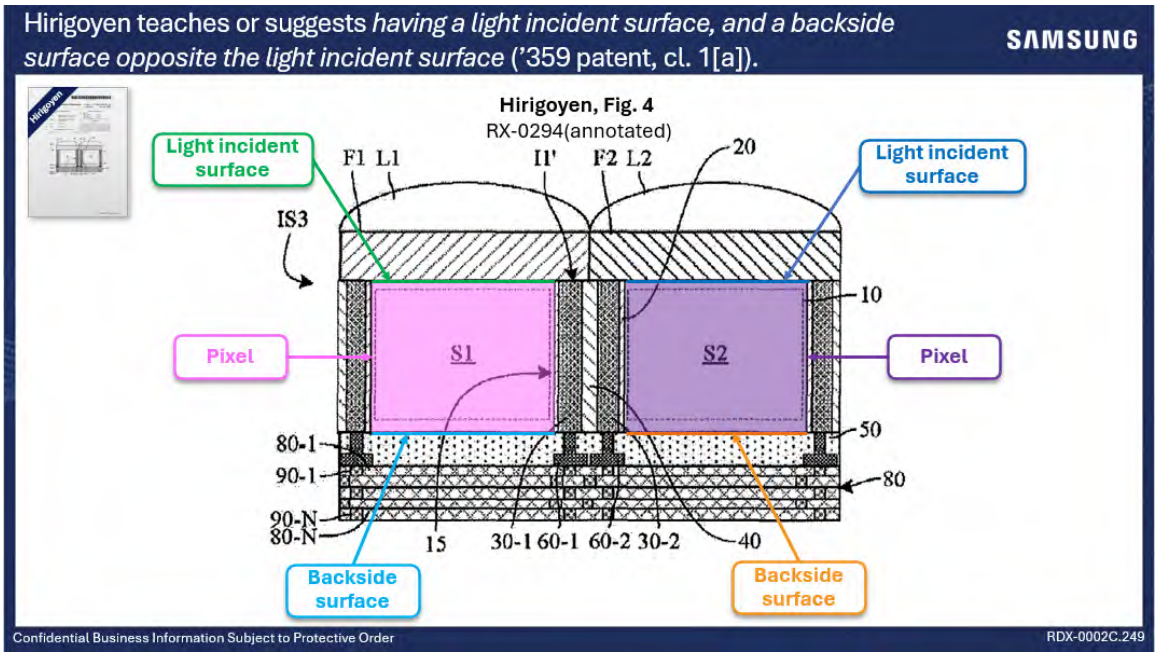


Q591 Are Hirigoyen's photosites *light sensitive image sensor pixels*?

A591 Yes. POSITAs would understand that each photosite, which may include a "photodiode," corresponds to an *image sensor pixel*. Hirigoyen, [0004] ("[O]ne or more photosites correspond[] to a pixel of a captured image. The photosites … may include for example photodiodes."). The photosites are thus *light sensitive pixels*. *See* Hirigoyen, [0005] ("A photon of an incident light ray penetrates into the material of the photosite, and … an electron-hole pair is generated. The number of electrons per photosite may be read as an electronic signal used to supply light information for the image."). Hirigoyen explains that microlenses as well as color filters are disposed above the pixels. *See, e.g.*, Hirigoyen, [0004] ("In general, above the photosites are distributed a mosaic of microlenses to converge incident light rays on the photosites and a mosaic of color filters to filter the light."), [0051], [0057]. Below the pixels lies a "pre-metal dielectric" layer. *See* Hirigoyen, [0049] ("pre-metal dielectric ('PMD') layer 50 is then deposited on the top surface of the image sensor").

Q592 Limitation 1[a]'s second element is *having a light incident surface, and a backside surface opposite the light incident surface*. Does Hirigoyen satisfy this element?

A592 Yes. As RDX-0002C.249 illustrates, each pixel in Hirigoyen has *a light incident surface and a backside surface opposite the light incident surface*.



The interface between photosite S1 and color filter F1 is a *light incident surface* for photosite S1 and the interface between S2 and color filter F2 is a *light incident surface* for photosite S2. *See* Hirigoyen, [0057] ("color filters F1, F2, F3, and microlenses L1, L2, L3 are arranged on the backside of the substrate 10, which is then turned around to face the incident light"), [0051] ("Color filters F1, F2 are formed over the photosites, and then microlenses L1, L2 are formed above the color filters.").

Likewise, the interface between each photosite and the "pre-metal dielectric layer 50" is a *backside surface opposite the light incident surface* of that photosite. *See* Hirigoyen [0049] ("pre-metal dielectric ('PMD') layer 50 is then deposited on the top surface of the image sensor IS2").

Q593 Which embodiment of Hirigoyen are you basing your analysis on?

A593 Unless otherwise noted, my analyses for the '359 patent pertain to Hirigoyen's second embodiment, depicted in Figure 4. While I will occasionally reference disclosures pertaining to Hirigoyen's "IS2" embodiment, depicted in Figure 3, they are equally applicable to Hirigoyen's second embodiment ("IS3"). *See* Hirigoyen, [0038] ("Reference throughout this specification to 'one embodiment,' or 'an embodiment' means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment.").

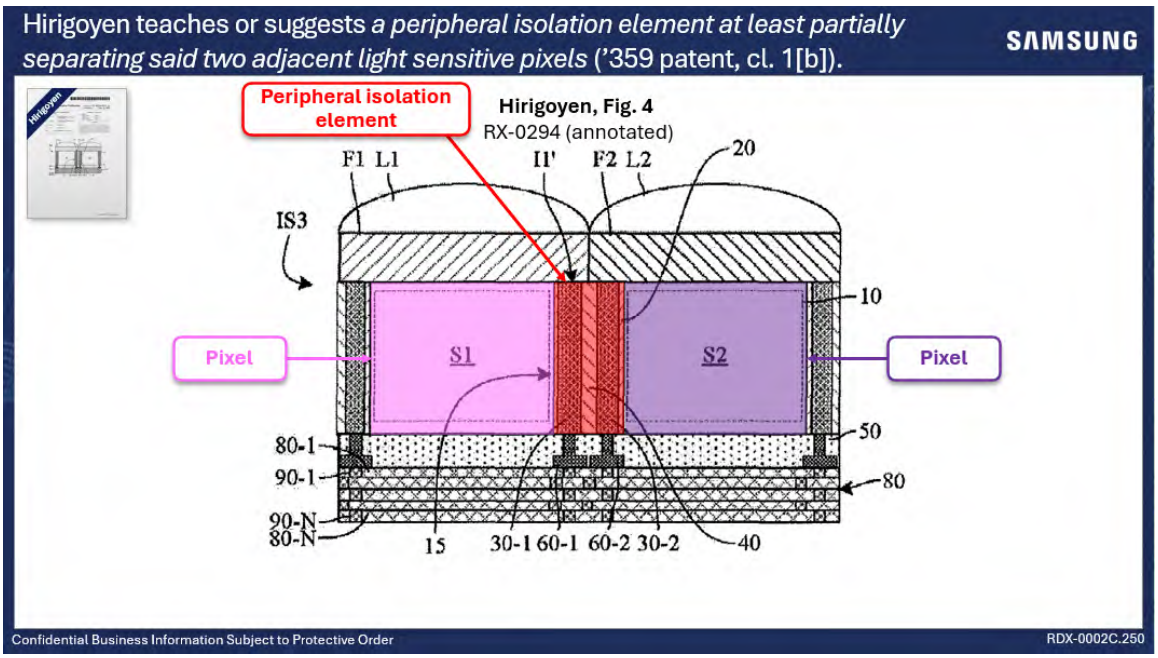
2. Limitation 1[b]

Q594 Limitation 1[b] is *a peripheral isolation element at least partially separating said two adjacent light sensitive pixels*. Does Hirigoyen satisfy this limitation?

A594 Yes. Hirigoyen teaches or suggests this limitation. Dr. Mansoorian has not disputed this. Hirigoyen includes an *isolation element*, i.e., "isolation region I1'":

> Isolation region I1' extends between sites S1, S2 and comprises the first deep trench 15 having its bottom and sidewalls covered by the thin liner 20 and filled with the conductive material 30. The isolation region I1' further comprises the second trench 35 in the conductive material 30, filled with the optically isolating material 40.

Hirigoyen, [0051]. As RDX-0002C.250 illustrates, Hirigoyen's isolation region I1' is *peripheral*, as it extends along the periphery of the photosites. As RDX-0002C.250 also illustrates, isolation region I1' also *at least partially separates said two adjacent light sensitive pixels*, as it separates adjacent photosites. *See* Hirigoyen, [0002] ("present disclosure relates to an image sensor including at least two photosites separated by an isolation region"), [0055] ("[E]ach photosite is completely surrounded by the isolation regions. In particular, any two photosites are separated by the liner 20, the conductive material 30, the optical isolator 40, the conductive material 30, and the liner 20.").



3. Limitation 1[c]

Q595 Limitation 1[c] is *each of said pixels having at least one doped region disposed on at least one of the light incident surface and the backside surface*. Does Hirigoyen satisfy this limitation?

A595 Yes. Each pixel in Hirigoyen *ha[s] at least one doped region disposed on at least one of the light incident surface and the backside surface*. Dr. Mansoorian has not disputed this. Hirigoyen discloses that photosites (*pixels*) S1 and S2 are formed in semiconductor substrate 10 and include "photodiodes." Hirigoyen, [0004] ("photosites … may include ...photodiodes"); *see* Hirigoyen, [0017] ("forming at least two photosites in a semiconductor substrate"), [0008] ("substrate 10 including two photosites S1, S2"), [0042] ("substrate 10 comprises photosites S1, S2").

POSITAs would understand that photodiodes consist of a p-n junction of *doped* semiconductor *regions* doped with p-type and n-type dopants. *See* Hwang, 5:59-65 ("The pixel semiconductor patterns … are doped with a first conductive dopant. The photodiodes … are regions doped with a second conductive dopant. That is, a photodiode … is a region doped with the second conductive dopant within a predetermined region of a pixel semiconductor pattern…. The first conductive dopant can be a P-type dopant, and the second conductive dopant may be an N-type dopant. Conversely, the first conductive dopant can be an N-type dopant, and the second conductive dopant can be a P-type dopant."); Iida, [0049] (describing photodiode as a p-n junction between an n-type impurity region and a p-type silicon substrate); Roy, [0038] (describing photodiode as junction of doped p-type semiconductor substrate and doped n-type region); Haddad188, 9:18-20 (describing photodiode as "semiconductor substrate … having multiple doped regions … forming at least one junction"). Consistent with this understanding, Hirigoyen expressly discloses that its photosites' substrate 10 includes doped semiconductors. Hirigoyen, [0063] ("term 'substrate' should be understood as including … doped and undoped semiconductors").

Q596 Are Hirigoyen's doped regions *disposed on at least one of the light incident surface and the backside surface*?

A596 Yes. As discussed for '359 patent (Ground 4), limitation 1[a], semiconductor substrate 10 provides the pixel's light incident and backside surfaces: the interface between photosite S1 and color filter F1 is a *light incident surface* for photosite S1 and the interface between photosite S2 and color filter F2 is a light incident surface for photosite S2. POSITAs would know that the p-type and n-type doped regions that form photodiodes would commonly have surfaces at the *light incident* and/or *backside surfaces* of the semiconductor substrate in which they reside. *See* Iida, Figs. 5-15; Hwang, Figs. 2, 5-6; Haddad188, Figs. 2-6. Accordingly, POSITAs would expect, and find it obvious, that *at least one* of the p-type and n-type *doped regions* that make up Hirigoyen's photodiode in substrate 10 would have at least one side forming the pixel's *light incident surface* or *backside surface* and thus be *disposed on at least one of the light incident surface and the backside surface*.

Hirigoyen also teaches diffusing dopants into semiconductor substrate 10. *See* Hirigoyen, [0061] ("if a doped conductive material 30, such as a doped polysilicon, is deposited or formed in the trench, an annealing step may then be performed to 'outdiffuse' the dopants into the substrate area near the sidewalls in order to passivate the interfacial traps"). POSITAs would understand that this diffusion of dopants from areas of the isolation region near the photosites' *light incident surface* and *backside surface* would also result in doped regions *disposed on the light incident surface and the backside surface of the photosites*, in the vicinity of the isolation region.

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4. Limitation 1[d]

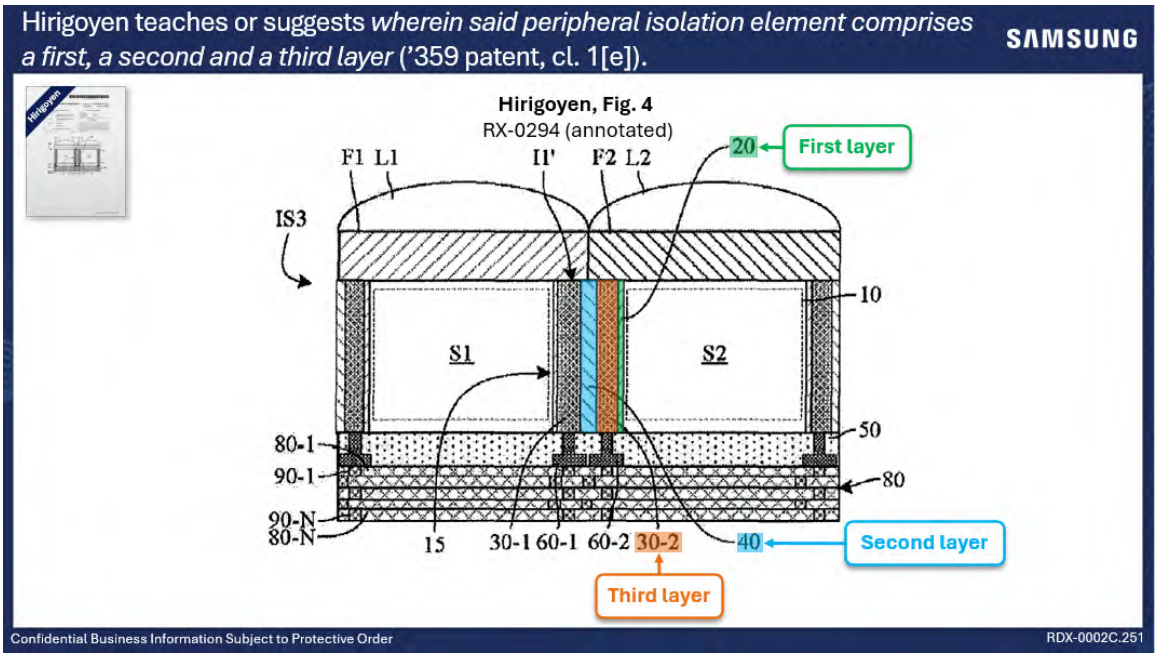
Q597 Limitation 1[d] is *wherein the peripheral isolation element comprises at least two materials having different indices of refraction*. Does Hirigoyen satisfy this limitation?

A597 Yes. Hirigoyen's isolation region I1' *comprises at least two materials having different indices of refraction*. Dr. Mansoorian has not disputed this. Hirigoyen discloses that isolation region I1' comprises five layers: "the liner 20, the conductive material 30, the optical isolator 40, the conductive material 30, and the liner 20." Hirigoyen, [0055]; *see also* Hirigoyen, [0057] ("The trench 15 extends entirely through the substrate 10 and the liner 20 extends on both sidewalls of the trench. The optical isolator 40 extends entirely through the trench 15, and the conductive material 30 in the trench is separated into two regions 30-1 and 30-2."). Hirigoyen discloses that optical isolator 40 and conductive material 30 are made of different materials having different refractive indices. *See* Hirigoyen, [0045] ("conductive material 30 has as second refractive index, which may be, for example, 3.5 for polysilicon"), [0047] ("optical isolator 40 has a third index of refraction, which may be, for example, 1.5 for silicon dioxide").

5. Limitation 1[e]

Q598 Limitation 1[e] is *wherein said peripheral isolation element comprises a first, a second and a third layer*. Does Hirigoyen satisfy this limitation?

A598 Yes. As RDX-0002C.251 illustrates, Hirigoyen's isolation region Il' *comprises a first, a second and a third layer*: (1) a liner 20 (*first layer*); (2) optical isolator (*second layer*); and (3) conductive material 30-2 (*third layer*). Dr. Mansoorian has not disputed this.



6. Limitation 1[f]

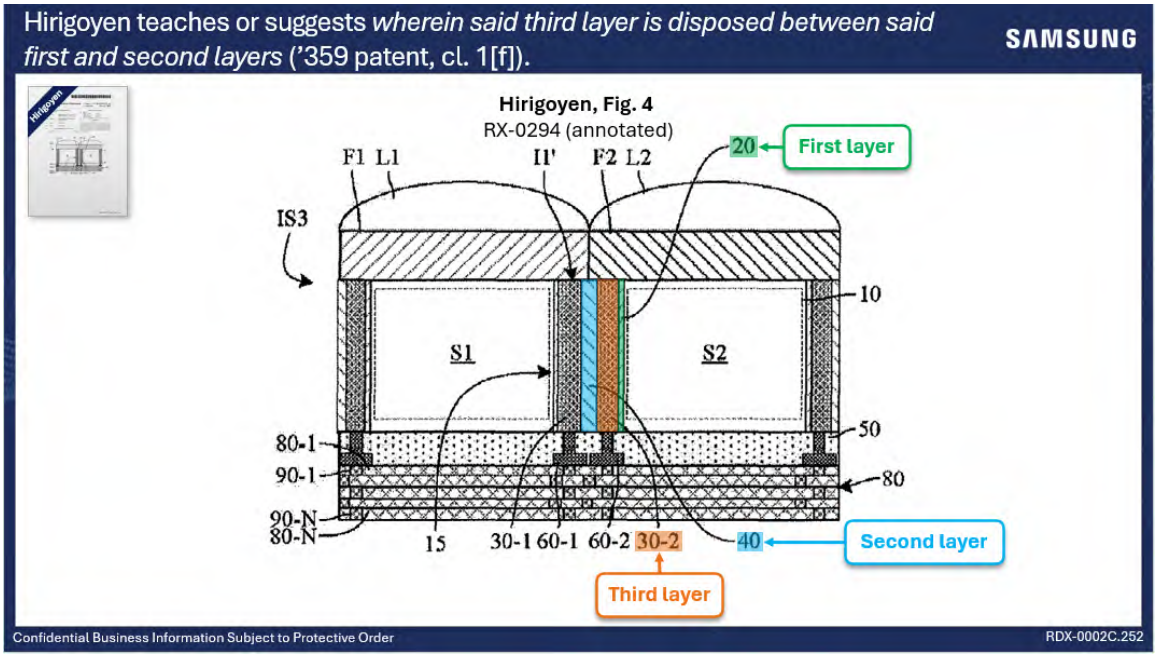
Q599 Limitation 1[f] is *wherein said third layer is disposed between said first and second layers*. Does Hirigoyen satisfy this limitation?

A599 Yes. Hirigoyen teaches or suggests *wherein said third layer is disposed between said first and second layers*. Dr. Mansoorian has not disputed this.

As explained in the Terms Remaining in Dispute, I understand that the parties proposed constructions for limitation 1[f] as a whole. Hirigoyen satisfies limitation 1[f] under either construction.

Q600 How does Hirigoyen satisfy this limitation?

A600 As RDX-0002C.252 illustrates, the *third layer* of isolation region I1' (conductive material 30-2) *is disposed between the first layer* (liner 20) *and the second layer* (optical isolator 40).



7. Limitation 1[g]

Q601 Limitation 1[g] is *wherein each of said first and second layer exhibits an index of refraction less than an index of refraction of said third layer*. Does Hirigoyen satisfy this limitation?

A601 Yes. Each of the *first layer* and *second layer* of Hirigoyen's isolation region I1' *exhibits an index of refraction less than an index of refraction of the third layer*. Hirigoyen discloses a refractive index of 3.5 for its conductive material 30-2 made of polysilicon. *See* Hirigoyen, [0045] ("conductive material 30 has a second refractive index, which may be, for example, 3.5 for polysilicon"). Hirigoyen discloses a refractive index of 1.5 for its

optical isolator 40 made of silicon dioxide. *See* Hirigoyen, [0047] ("optical isolator 40 has a third index of refraction, which may be, for example, 1.5 for silicon dioxide"). Hirigoyen discloses that the liner 20 may be made of silicon dioxide like optical isolator 40. *See* Hirigoyen, [0044] ("liner 20 may be a dielectric material, silicon dioxide SiO_2"). Accordingly, liner 20 (*first layer*) and optical isolator 40 (*second layer*) have an index of refraction (1.5) less than an index of refraction (3.5) of conductive material 30-2 (*third layer*).

Q602 Are you aware of Dr. Mansoorian's argument that Hirigoyen does not disclose or render obvious this limitation because your identification of the claimed layers in Hirigoyen would allegedly frustrate Hirigoyen's teachings?

A602 Yes. I understand that Dr. Mansoorian contends that my identification of Hirigoyen's "liner 20" as the claimed first layer, "conductive material 30-2" as the claimed third layer, and "optical isolator 40" as the claimed second layer, "frustrates the preferred design of Hirigoyen of having the layers with refractive indices lined up such that the first index is greater than the second, and the second index is greater than the third" because Hirigoyen's "first index is less than the second index." RX-0911C, ¶¶ 737, 741. I disagree. Dr. Mansoorian conflates the limitation's numbered layers with Hirigoyen's numbering of refractive indices. Hirigoyen's "first index" is the refractive index of substrate 10 (not liner 20, i.e., the claimed first layer); Hirigoyen's "second index" is the refractive index of conductive material 30-2, i.e., the claimed third layer (not the claimed second layer); and Hirigoyen's "third index" is the refractive index of optical isolator 40 (i.e., the claimed second layer, not the claimed third layer). *See* Hirigoyen, [0053] ("[T]he substrate 10 has a first refractive index such as 4, the conductive material 30 has a second refractive index such as 3.5, and the optical isolator 40 has a third refractive index such as 1.5. These indices may be chosen so that the first index is greater than the second, and the second index is greater than the third."). My identification of liner 20, conductive material 30-2, and optical isolator 40 as the claimed "first," "second," and "third" layers, respectively, is consistent with Hirigoyen's "first index" (4, for its substrate) being greater than its "second index" (3.5, for its conductive material) and its "second index" being greater than its "third index" (1.5, for its optical isolator).

Q603 Are you aware of Dr. Mansoorian's argument that Hirigoyen does not disclose or render obvious this limitation for additional reasons?

A603 Yes. I understand that Dr. Mansoorian contends that Hirigoyen does not disclose or render obvious this limitation because Hirigoyen allegedly discloses that liner 20 "may be a variety of materials" and allegedly does not specifically disclose an index of refraction for liner 20. RX-0911C, ¶¶ 733-736, 739-740. I disagree. As I noted, Hirigoyen specifically discloses "silicon dioxide" as one of six material options for liner 20. Hirigoyen, [0044] ("The liner 20 may be a dielectric material, silicon dioxide SiO2, nitric oxide NO, silicon oxide SiO, a high density plasma (HDP) oxide, a spin on dielectric (SOD) or other suitable material."). In view of SiOnyx's apparent interpretation and application of the term "refractive index" in its infringement and domestic industry technical prong contentions, where SiOnyx appears to have relied upon bulk refractive index values, POSITAs would know that Hirigoyen's liner 20, when made of silicon dioxide as Hirigoyen expressly

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discloses, would have a refractive index of 1.5, given that Hirigoyen expressly discloses, in describing optical isolator 40, that "silicon dioxide" has a refractive index of "1.5."

I also understand that Dr. Mansoorian contends that "Hirigoyen teaches away from considering liner 20 as an optically relevant layer, stating: 'liner 20 is generally too thin to influence the optical properties of the isolation regions.'" RX-0911C, ¶ 736. I disagree. Limitation 1[g] does not require the claimed "first layer" to be "considered optically relevant." Moreover, in Dr. Foty and SiOnyx's own apparent interpretation and application of this limitation in its infringement and domestic industry technical prong contentions, this limitation is satisfied by peripheral isolation element layers that are approximately or less than 10nm wide. *See, e.g.*, RX-0905C, ¶¶540-561; RX-0579C.35-37; RX-0128.32; *see* Hirigoyen, [0044] ("The liner 20 may have a thickness of approximately 10 nm.").

b. Claim 18

Q604 Let's turn to claim 18. Have you formed an opinion regarding claim 18?

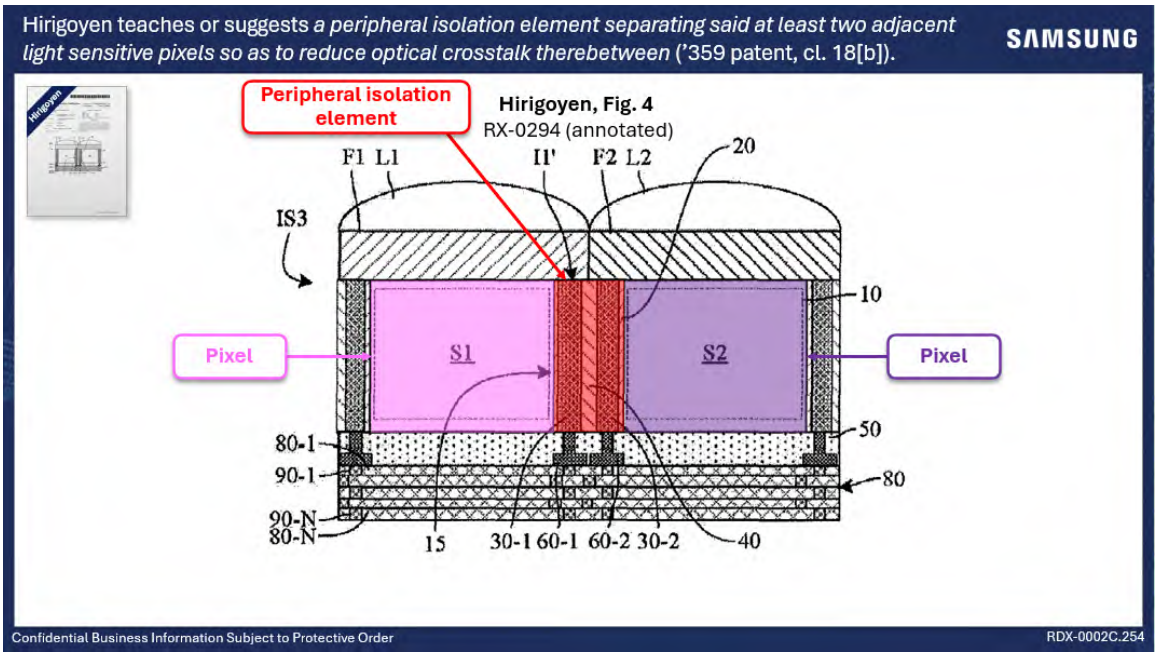
A604 Yes. Hirigoyen teaches or suggests claim 18. As RDX-0002C.253 illustrates, limitations 18[a] and 18[c]-[g] are identical to limitations 1[a] and 1[c]-[g]. Hirigoyen teaches or suggests these limitations for the reasons discussed for the corresponding limitations of '359 patent (Ground 4), claim 1. The only limitation not identical to a limitation of claim 1 is limitation 18[b].

1. Limitation 18[b]

Q605 Limitation 18[b] is *a peripheral isolation element separating said at least two adjacent light sensitive pixels so as to reduce optical crosstalk therebetween*. Does Hirigoyen satisfy this limitation?

A605 Yes. Hirigoyen teaches or suggests this limitation. Dr. Mansoorian has not disputed this.

As discussed for '359 patent (Ground 4), limitation 1[b], Hirigoyen discloses a *peripheral isolation element* (isolation region I1'). As RDX-0002C.254 illustrates, isolation region I1' *separates said at least two adjacent light sensitive pixels*. *See* Hirigoyen, [0002] ("present disclosure relates to an image sensor including at least two photosites separated by an isolation region"), [0055] ("any two photosites are separated by the liner 20, the conductive material 30, the optical isolator 40, the conductive material 30, and the liner 20").



Q606 Does isolation region I1' *reduce optical crosstalk* between said pixels?

A606 Yes. Hirigoyen teaches that isolation region I1' separates two adjacent pixels *so as to reduce optical crosstalk therebetween*. *See* Hirigoyen, [0052] ("Isolation region I1' reduces optical crosstalk thanks to an optical waveguide formed by the differences in refractive indices between the substrate 10, the conductive material 30, and the optical isolator 40."), [0006] ("Optical crosstalk between photosites occurs when the photons of an incident light ray are absorbed by a photosite other than the one that should absorb them…. Isolation regions are therefore commonly provided between photosites to prevent optical and/or electrical crosstalk."), [0007] ("The isolation region may be in the form of a deep trench isolation…. The deep trench may further be filled with an optically isolating material such as oxide to create an 'optical waveguide' reducing optical crosstalk….").

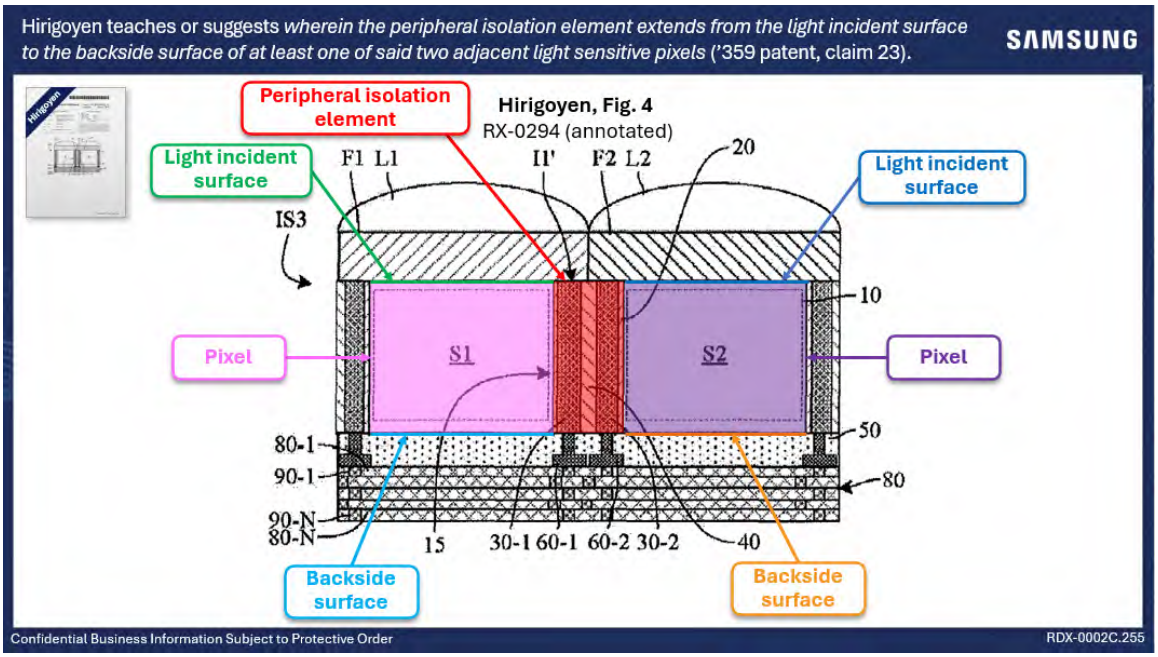
c. Claim 23

Q607 Let's turn to claim 23, which is *[t]he device of claim 18, wherein the peripheral isolation element extends from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels*. Does Hirigoyen satisfy this limitation?

A607 Yes. Hirigoyen teaches or suggests this limitation. Dr. Mansoorian has not disputed this.

As RDX-0002C.255 illustrates, Hirigoyen's isolation region I1' *extends* completely *from the light incident surface* (F1/10 and F2/10 interfaces of photosites S1 and S2, respectively) *to the backside surface* (10/50 interfaces) *of at least one of said two adjacent light sensitive pixels* (photosites S1 and S2). *See* Hirigoyen, [0051] ("Isolation region I1' extends between sites S1, S2"), [0057] ("The trench 15 extends entirely through the substrate 10 and the liner 20 extends on both sidewalls of the trench.... The optical isolator extends entirely through trench 15."), [0059] ("isolation regions may therefore extend entirely through the substrate"), [0007] ("The isolation region may be in the form of a deep trench isolation

('DTI') with a depth as great as possible…. In this manner, generated electrons cannot pass under or through the isolation region from one photosite to another, reducing electrical crosstalk."), [0025], [0027].



2. Ground 5: Hirigoyen and Shinohara Render Obvious Claims 1, 11, 18 and 23

Q608 Let's turn to your Ground 5 opinions. Can you please summarize your Ground 5 opinions?

A608 In my opinion Hirigoyen and Shinohara render obvious claims 1, 11, 18, and 23. As explained for Ground 4, Hirigoyen anticipates, or at least renders obvious, claims 1, 18, and 23. Those opinions are equally applicable to my Ground 5 opinions regarding Hirigoyen and Shinohara, which further render obvious claim 11.

a. Claim 11

Q609 Let's turn to claim 11, which is *[t]he device of claim 1, wherein the peripheral isolation element comprises any of aluminum oxide and hafnium oxide*. Have you formed an opinion regarding this limitation?

A609 Yes. Hirigoyen and Shinohara render this claim obvious. Shinohara discloses using Al_2O_3 as an insulating layer in a pixel separation structure. *See* Shinohara, [0091] ("[A]s the insulating film 69, an insulating film having a negative fixed charge may also be used. As the insulating film having a negative fixed charge, for example, there may be used a film of … dialuminum trioxide (Al_2O_3).").

It would have been obvious to POSITAs to use Shinohara in selecting materials for Hirigoyen's isolation region (*peripheral isolation element*) and to use Al_2O_3, as taught by

Shinohara, for Hirigoyen's first insulating liner 20 (*first layer*). Specifically, POSITAs would have been motivated to use Al_2O_3 as a pixel separation structure material for Hirigoyen's liner 20 and would have reasonably expected success in doing so.

Q610 Why would using Shinohara's Al_2O_3 in Hirigoyen have been obvious?

A610 Hirigoyen and Shinohara are both directed to the same field of endeavor: imager devices comprising light-sensitive pixels. *See* Hirigoyen, [0002]; Shinohara, [0051]. Both references similarly seek to minimize crosstalk by inserting trench-type separation structures between adjacent pixels. *See* Hirigoyen, [0006], [0011]; Shinohara, [0011]-[0013], [0017] ("forming a trench … in a semiconductor substrate … filling a semiconductor layer in the trench by an epitaxial growth to form an element isolation region"), [0021], [0090].

As discussed for '359 patent (Ground 4), limitation 1[e], Hirigoyen discloses a pixel isolation region I1' comprising thin electrically insulating liner 20, electrically conductive material 30, and optically isolating material 40. *See* Hirigoyen, [0044]-[0048]. Hirigoyen discloses that its liner 20 "may be a dielectric material, silicon dioxide SiO_2, nitric oxide NO, silicon oxide SiO, a high density plasma (HDP) oxide, a spin on dielectric (SOD) or other suitable material." Hirigoyen, [0044]. POSITAs would have known that, should silicon dioxide be selected for liner 20, the interface between Si and SiO_2 in Hirigoyen's isolation region would generate dark current and cause the signal-to-noise ratio to deteriorate. *See* Iida, [0007]. Surface recombination contributes to dark current, which reduces image quality. *See* Iida, [0007]; Hirigoyen, [0006] ("performance of an image sensor depends on many factors, such as … dark current (the amount of current generated even when the photosites are not receiving incident light rays)"). Accordingly, POSITAs seeking to implement Hirigoyen would be motivated to look for guidance to identify potentially more suitable materials for liner 20 in Hirigoyen's isolation region I1' (*peripheral isolation element*) to further improve Hirigoyen's absorption and sensitivity. *See* JX-0027C (McKee), 82:13-83:8 (describing different materials, such as dielectrics or metals that can be used as materials to optically isolate a pixel).

Q611 Why would POSITAs consider Shinohara for this purpose?

A611 POSITAs would look to Shinohara for this purpose because, as discussed, Hirigoyen and Shinohara are both directed to the design of pixel separation structures in imager devices and because Shinohara teaches suitable materials for pixel separation structure layers.

POSITAs would be particularly motivated to look to Shinohara because Shinohara teaches that its trench separation structure materials help reduce optical and electrical crosstalk. *See* Shinohara, [0008] (stressing that "it is important to suppress the occurrence of color mixture caused by leakage of charge (such as electron) photoelectrically converted in the vicinity of the rear surface side into an adjacent pixel"), [0094] ("since the filled insulated film 69 has a refractive index different from that of the p-type semiconductor layer 43, even if inclined incident light is incident thereon, the light is not photoelectrically converted in an adjacent pixel after passing through the element isolation region 68"). Shinohara further explains that its teachings are directed, in part, to overcome shortcomings

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in the prior art where the formation of trench-type pixel separation structures results in white spots and dark current. *See* Shinohara, [0011] ("element isolation region which physically isolates pixels is formed by a trench method in a rear surface of a substrate so as to suppress leakage of charge into an adjacent pixel"). As an additional benefit, Shinohara teaches that its disclosures enable a more efficient manufacturing process. *See, e.g.*, Shinohara, [0088]-[0089], [0093], [0096]. Thus, several important performance objectives such as achieving high levels of absorption and efficiency would motivate POSITAs to look to Shinohara in selecting the material for Hirigoyen's insulating liner 20 to minimize electrical and optical crosstalk and dark current. *See* JX-0017C (Sickler), 41:7-8 (explaining that dark current is harmful should be minimized).

Q612 Why would POSITAs be motivated to use Al_2O_3 in Hirigoyen?

A612 Like Hirigoyen, Shinohara teaches that silicon oxide can be used as an electrically insulating film. *See* Shinohara, [0091] ("an insulating film, such as a silicon oxide film … may be used"); Hirigoyen, [0044] ("liner 20 may be … silicon oxide"). However, Shinohara teaches that using "an insulating film having a negative fixed charge" provides an additional benefit: enhanced passivation. *See* Shinohara, [0094] ("When the insulating film having a negative fixed charge is used as the insulating film 69, the hole pinning state by the p-type semiconductor layer 43 of the element isolation region 68 can be enhanced…. Accordingly, the generation of white spots and dark current can be further suppressed.").

POSITAs would have known that Al_2O_3, taught by Shinohara as an insulating material for pixel separation structures, exhibits low surface recombination velocity—lower than that of the SiO_2 used in Hirigoyen's liner 20—and achieves high-quality chemical passivation. *See* RX-0311.1-3 (Saint-Cast); RX-0309.104 (Hoex). POSITAs would understand that, to get Al_2O_3's benefit of surface recombination properties as a negative fixed charge material, the Al_2O_3 should be in contact with the semiconductor (silicon) substrate—i.e., be used as the material for Hirigoyen's insulating liner 20. Additionally, Al_2O_3 can exhibit a refractive index of approximately 1.7, which is lower than the refractive index of "approximately 4" that Hirigoyen discloses for its silicon substrate 10. *See* Suzunaga, [0070] (disclosing a refractive index of 1.7 for its Al_2O_3); RX-0304.B-68 (CRC Handbook) (disclosing a refractive index of 1.76 for Al_2O_3); Hirigoyen, [0042], [0053].

Moreover, using a thin film of Al_2O_3, as an alternative to silicon dioxide, in combination with a light-blocking layer, was known to POSITAs. *See* RX-0897 (Masuda), 18:12-53 (disclosing use of an "underlying film 42" made of, for example, "Al_2O_3 (aluminum oxide)" instead of "silicon dioxide," "in … combination" with a "light blocking layer 41," to reduce crosstalk between adjacent pixels in an imager device. Accordingly, POSITAs would have been motivated to use Al_2O_3 pixel separation structure layer, as Shinohara teaches, in place of Hirigoyen's insulating liner 20 to achieve better passivation and reduce surface recombination velocity along the sidewalls of Hirigoyen's photosites.

Q613 Would POSITAs have reasonably expected success in making this combination?

A613 Yes. POSITAs would have reasonably expected success in making this combination. As discussed, Hirigoyen and Shinohara both are directed to imager devices comprising light-

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sensitive pixels and specifically to the use of trench separation structures between adjacent pixels to reduce crosstalk. Given the similarities in structure and function of Hirigoyen and Shinohara, POSITAs would have viewed building Hirigoyen's insulating liner 20 with Al_2O_3, as Shinohara teaches, as a simple design choice and the application of a known technique to improve a similar device in the way Shinohara teaches, to yield predictable results.

Q614 Are there any other reasons why POSITAs have reasonably expected success in making this combination?

A614 Yes. Further reinforcing POSITAs expectation of success, including Al_2O_3, as Shinohara teaches, would have involved routine manufacturing steps that Hirigoyen and Shinohara already taught. *See* Hirigoyen, [0044] ("The liner 20 may be formed using a conformal process, so that its thickness is substantially uniform. The liner 20 … may be thermally grown or deposited."); Shinohara, [0091] ("As a method for forming the insulating film having a negative fixed charge, for example, an atomic layer deposition (ALD) method or a metal-organic chemical vapor deposition (MOCVD) method may be used. When the insulating film having a negative fixed charge is used, one type of film or a laminate containing a plurality of types of films may be used.").

Q615 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination because they would consider the combination unnecessary because Hirigoyen teaches another method for suppressing dark current?

A615 Yes. Dr. Mansoorian opines that POSITAs would not use Shinohara's Al_2O_3 for Hirigoyen's liner 20 because Hirigoyen already teaches suppressing dark current by biasing the conductive materials 30-1 and 30-2 and adjusting the amount of biasing. RX-0911C, ¶¶ 747-50. I disagree. While Hirigoyen does teach a biasing method to reduce dark current, a POSITA would view use of Al_2O_3 as the pixel separation structure's outer layer as taught by Shinohara as a complementary method for reducing dark current and would have been motivated to combine these methods to reduce dark current as much as possible. *See* JX-0017C (Sickler), 41:7-8 ("dark current is a bad thing, you want to keep it to a minimum.").

Q616 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination because it "would introduce design complications"?

A616 Yes. Dr. Mansoorian does not explain what he means by "design complications" and "electrical design complications." RX-0911C, ¶ 748, 752. Regardless, I disagree. As explained, in my opinion, POSITAs would have viewed building Hirigoyen's insulating liner 20 with Al_2O_3, as Shinohara teaches, as a simple design choice and the application of a known technique to improve a similar device in the way Shinohara teaches, to yield predictable results.

Q617 Are you aware of Dr. Mansoorian's argument that POSITAs would not make this combination because it would frustrate Hirigoyen's teachings?

A617 Yes. Dr. Mansoorian opines that using Shinohara's Al_2O_3 for Hirigoyen's liner 20 "would frustrate Hirigoyen's preferred arrangement of the layers with refractive indices lined up

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such that the first index is greater than the second, and the second index is greater than the third" because it "would introduce a material with a low refractive index between the substrate (refractive index 4) and the conductive material (refractive index 3.5) of Hirigoyen." RX-0911C, ¶ 751-52. I disagree. As explained for '359 patent (Ground 4), limitation 1[g], Dr. Mansoorian's argument that my identification of liner 20—whether made of silicon dioxide with a refractive index of 1.5 or Al_2O_3 with a refractive index of 1.7—as the claimed "first layer" frustrates' Hirigoyen's design conflates the '359 patent claim limitation's numbered layers with Hirigoyen's numbering of refractive indices.

IX. Secondary Considerations

Q618 As part of your obviousness analysis, did you consider whether any secondary considerations of nonobvious exist?

A618 Yes. I understand that it is SiOnyx's burden as patent owner to come forward with evidence of secondary considerations. I have analyzed the evidence that SiOnyx and Dr. Mansoorian have provided in this Investigation regarding the Light Trapping Patents. In my opinion, the presented evidence is unpersuasive of any alleged secondary considerations or of any nexus between any alleged secondary consideration and the claimed inventions.

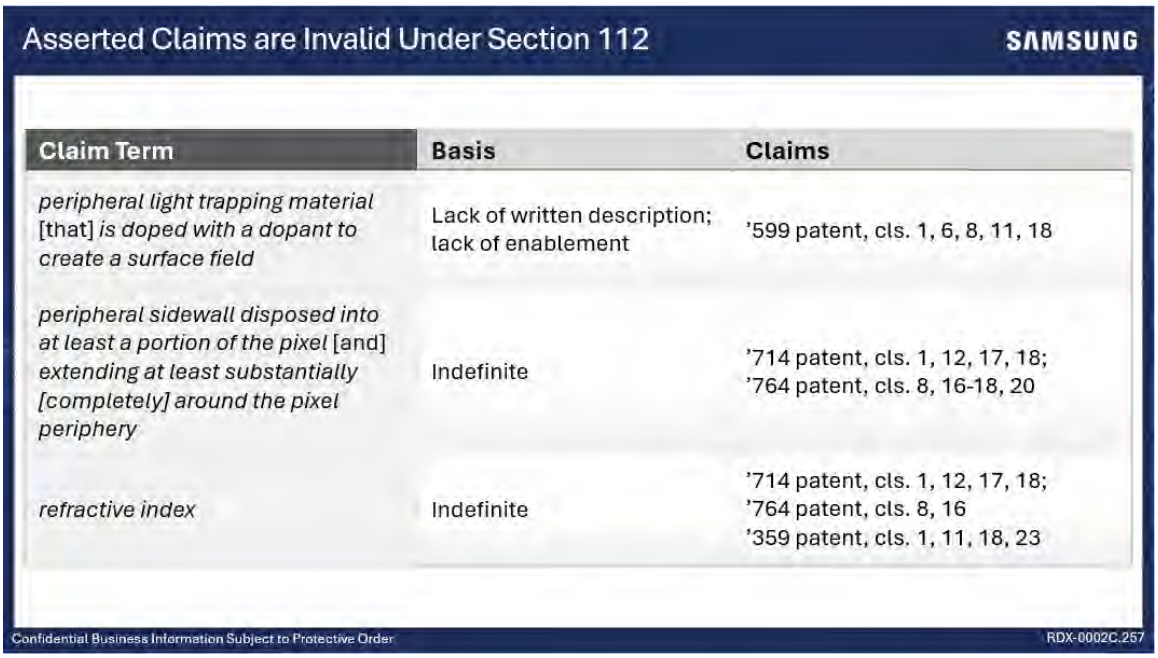
I understand that the ALJ has informed the parties that Samsung's experts should opine as to secondary considerations as part of their rebuttal testimony. Accordingly, I will analyze provide my detailed analysis regarding purported secondary considerations as part of my rebuttal testimony.

X. Invalidity Based on Lack of Written Description, Lack of Enablement, and Indefiniteness

Q619 Have you formed any opinions as to whether any of the Asserted Claims of the Light Trapping Patents are invalid for failing to satisfy the requirements of Section 112?

A619 Yes. As RDX-0002C.257 illustrates, in my opinion, several Asserted Claims of the Light Trapping Patents are invalid for failing to satisfy the requirements of Section 112.

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Q620 Can you please summarize your invalidity opinions based on Section 112?

A620 In my opinion, '599 patent, claims 1, 6, 8, 11, and 18 are invalid for lack of written description and enablement due to, in part, claim 1's requirement of a *peripheral light trapping material* that *is doped with a dopant to create a surface field*.

Additionally, in my opinion, '714 patent, claims 1, 12, 17, 18; and '764 patent, claims 8, 16-18, 20-21, and 23 are invalid because the term *peripheral sidewall disposed into at least a portion of the pixel* and *extending at least substantially [completely] around the pixel periphery* is indefinite, at least based on Drs. Foty and Mansoorian's interpretation of them.

Finally, in my opinion, '714 patent, claims 1, 12, 17, 18; '764 patent, claims 8, 16; and '359 patent, claims 1, 11, 18, 23-24 are invalid because the terms *refractive index* and *index of refraction* are invalid as indefinite based on Dr. Foty's interpretation of them.

A. Written Description and Enablement

1. Doping

Q621 Let's turn to your opinion that '599 patent, claims 1, 6, 8, 11, and 18 are invalid due lack of written description and enablement. Can you please explain why this is your opinion?

A621 '599 patent, claim 1, requires, in relevant part, a *peripheral light trapping material* [that] *is doped with a dopant to create a surface field*. However, the '599 patent does not explain how to dope the peripheral light trapping material to create the claimed *surface field*. The '599 patent merely states, in relevant part, that:

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> [I]t can also be beneficial to dope the sidewalls to create a surface field that will improve electrical isolation between the pixels. In one aspect, it can also be beneficial to dope the low refractive index material of the Bragg-type reflectors to increase such electrical isolation.

'599 patent, 10:14-18. This paragraph, as well as the remainder of the specification, would not convey to POSITAs that the inventors possessed the claimed subject matter at the time of the patent, nor how to make and use the claimed invention without undue experimentation. This is particularly true given that the claims allow—and in certain instances specifically set forth—a number of different materials for the peripheral light trapping material that POSITAs would not understand to be capable of: (i) being doped, and/or (ii) being doped in a manner that would result in a surface field.

Q622 What materials does the '599 patent allow, and/or set forth, for the peripheral light trapping material that POSITAs would not understand as being capable of being doped and/or being doped in a manner that would result in a surface field?

A622 '599 patent, claim 4—which depends from claim 1—requires that the *peripheral light trapping material includes a material selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof*. POSITAs would understand that doping generally refers to introducing impurities into solids, not *gas[ses]* or *partial vacuums*. The '599 patent's named inventors confirmed this understanding in their depositions. Specifically, Dr. Pralle testified that doping is understood to mean adding impurities into crystalline, or solid, materials—not gasses or partial vacuums—in order to impart an electrical charge. JX-0038C (Pralle), 271:14-15. Likewise, Dr. Sickler testified that doping would not ordinarily be considered to cover imparting impurities into gasses or partial vacuums. JX-0017C (Sickler), 189:10-16, 190:5-12.

Q623 Assuming that doping a gas or partial vacuum were possible, would such doping *create a surface field*?

A623 No. Even if doping a gas or partial vacuum was possible, POSITAs would not understand how to dope a gas or partial vacuum *to create a surface field*, as the claims require. Indeed, the '599 patent's named inventors were unaware how this could be accomplished. Specifically, neither Dr. Pralle nor Dr. Sickler knew how you could dope a gas or a partial vacuum *to create a surface field*. JX-0038C (Pralle), 271:16-21; JX-0017C (Sickler), 190:5-12.

Q624 Does the '599 patent contain adequate disclosure to reasonably convey to POSITAs that the named inventors possessed the full scope of the claimed invention?

A624 No. Consistent with the named inventors' own lack of understanding as to whether a *gas* or *partial vacuum* could be doped, as well as how or whether doping such materials could *create a surface field*, the '599 patent's specification does not contain an adequate disclosure to reasonably convey to POSITAs that the named inventors possessed the full claimed scope of the subject matter at the time the application was filed.

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That is, the '599 patent's specification would not convey to POSITAs that the named inventors had possession of a *peripheral light trapping material* comprising *a gas* or *at least a partial vacuum* that could be *doped with a dopant to create a surface field*.

Q625 Does the '599 patent enable POSITAs to make and use the claimed invention without undue experimentation?

A625 No. Similarly, the '599 patent's specification does not enable POSITAs to make and use the claimed invention without undue experimentation. That is, the '599 patent's specification would not inform POSITAs how to form a *peripheral light trapping material* comprising *a gas* or *at least a partial vacuum* that is *doped with a dopant to create a surface field* without undue experimentation.

B. Indefiniteness

1. Peripheral Sidewall

Q626 Let's turn to your opinion that '714 patent, claims 1, 12, 17, 18; and '764 patent, claims 8, 16-18, and 20 are invalid due to indefiniteness. Can you please explain why this is your opinion?

A626 During claim construction, the parties disputed the proper construction of the terms *light sensitive pixel* and *light sensitive image sensor pixels*. I understand that the ALJ declined to construe these terms or address the scope of *pixel* at that stage. *See* Order No. 36 at 26.

SiOnyx—including its experts Drs. Foty and Mansoorian—have not taken a clear, consistent, position as to what they believe constitutes the claimed *pixel*. Absent a clear indication of the bounds of the *pixel*, POSITAs cannot determine with reasonable certainty, whether a peripheral sidewall is *disposed into at least a portion of the pixel*, nor whether it *extend[s] at least substantially [completely] around the pixel periphery*.

Q627 Are these claims structural claims or method claims?

A627 I understand that these claims are structural, i.e., they describe the structure of a device, as opposed to the methods of manufacturing such a device. Accordingly, I understand that in order to satisfy this claim, there must be a structure having *a peripheral sidewall* which is simultaneously both *disposed into at least a portion of the pixel* and *extending at least substantially, [completely] around the pixel periphery*. That is, I understand the *peripheral sidewall*—which I understand the ALJ construed to mean "trench wall," *see* Order No. 36 at 20—must be both simultaneously disposed into the pixel and extending around it.

Q628 Can a *peripheral sidewall* be both simultaneously disposed into and extending around a pixel?

A628 It is unclear how a *peripheral sidewall*, i.e., a trench wall, could be both simultaneously disposed into and extending around a pixel. Nor do I believe POSITAs would be able to reasonably appraise these terms' meanings with reasonable certainty, when read simultaneously, in light of the specification and the prosecution history.

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Q629 Are you aware of Dr. Mansoorian's argument that the Light Trapping Patents' Figures depict a peripheral sidewall disposed into the pixel?

A629 Yes. Dr. Mansoorian opines that Light Trapping Patents' Figures—Figures 1 and 4 in particular—purportedly illustrate a *peripheral sidewall* disposed into the pixel. RX-0911C, ¶¶333-334. However, these figures do not show a *peripheral sidewall* disposed into the pixel, let alone simultaneously disposed into and extending around the pixel; at most, they appear to demarcate the pixel's outer bounds.[12] For example, at least Figures 1-3 illustrate *peripheral sidewalls* (i.e., trench walls) demarcating the boundary between the pixel and a trench, said trench separating two adjacent pixels. *E.g.*, '714 patent, 7:2-4 ("FIG. 1 illustrates a simplified drawing of an imager having a first pixel 102 and a second pixel 104, that are formed monolithically on a common semiconductor substrate 106 and are isolated from one another by an isolation element 114."), 8:26-28 ("As is shown in FIG. 2, for example, an imager having at least two pixels or photodiodes (202 and 204) and at least one isolation element 214. The pixels are formed monolithically on a common semiconductor substrate 206."), 10:63-65 ("a photosensitive imager having at least two pixels (302 and 304) and at least one trench isolation region 314 is shown in FIG. 3").

Q630 Are you aware of Dr. Mansoorian's argument that the Light Trapping Patents' specification describes a sidewall being simultaneously disposed into and extending around a pixel?

A630 Yes. Dr. Mansoorian points to various passages in an attempt to explain how a peripheral sidewall can be both simultaneously disposed into and extend around a pixel. For example, Dr. Mansoorian argues that "[t]he specification further explains that the isolation element extend into the semiconductor material and that the process for forming the isolation element involves etching the semiconductor material in which the pixels are formed." RX-0911C, ¶339. I disagree.

As explained, the claims are structural, i.e., describing the structure of a device, as opposed to methods of manufacturing such a device. Accordingly, while a trench may be formed by etching into a semiconductor layer, as Dr. Mansoorian opines, such that it may be disposed into that semiconductor layer, these passages do not inform a POSITA how the peripheral sidewall can be disposed into the finished pixel itself; let alone how it could also simultaneously extend around it.

Nor do I believe that the passages Dr. Mansoorian cites as allegedly "explain[ing] that the peripheral sidewall extends at least substantially around the pixel periphery for optical and electrical isolation of the pixel device," RX-0911C, ¶336, in fact explain how a *peripheral sidewall* can be both simultaneously disposed into and extend around a pixel. Instead, these passages merely describe a process of etching a trench around the *pixel*. '714 patent, 2:64-67, 12:41-42, 13:6-9. While '714 patent, 11:15-22 states that "a peripheral sidewall 424 [is] disposed into at least a portion of the pixel 402 and extending at least substantially around the pixel periphery," Figure 4 does not depict the sidewall 424 being simultaneously

[12] As discussed, to the extent the figures of the patent illustrate a peripheral sidewall that is both *disposed in* and *extending around the pixel periphery*, the prior art discloses such a structure.

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disposed into and extending around the pixel 402; rather the peripheral sidewall is once again shown as a boundary to the pixel.

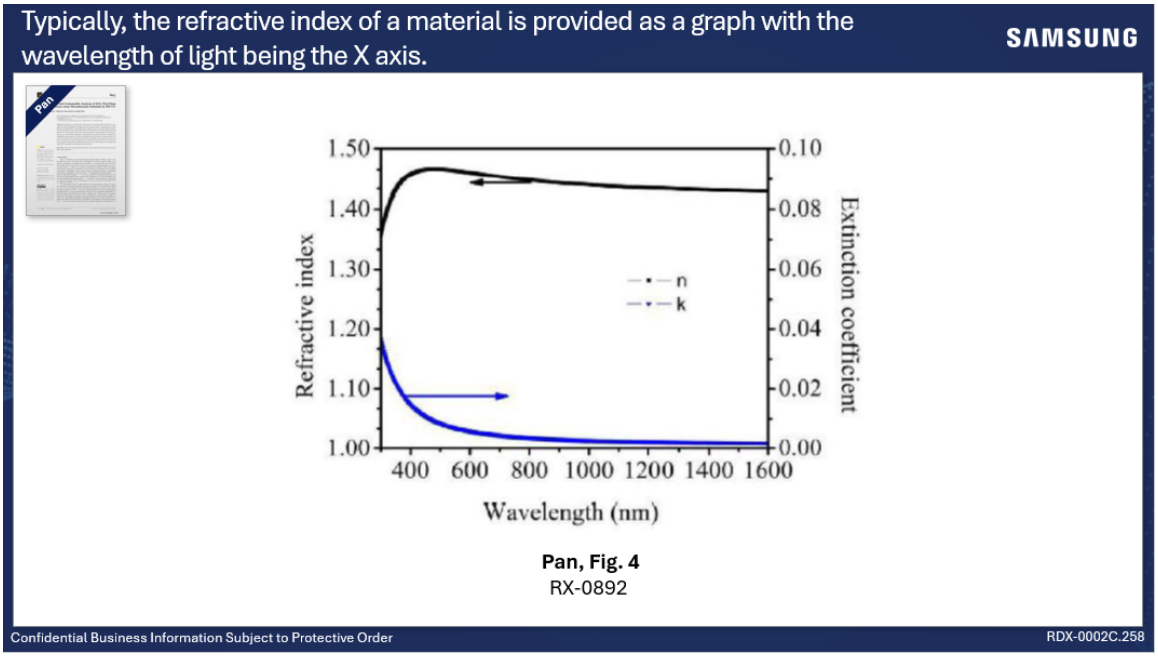
2. Refractive Index

Q631 Let's turn to your opinion that '714 patent, claims 1, 12, 17, 18; '764 patent, claims 8, 16; and '359 patent, claims 1, 11, 18, 23 are invalid due to indefiniteness. Can you please explain why this is your opinion?

A631 In my opinion, Dr. Foty's approach to proving infringement renders the claims indefinite because his analysis is not based on measuring the actual refractive index of the accused materials. Rather, he analyzes infringement based on published literature for materials that have a similar composition regardless of other factors that would affect the refractive index of the accused material.

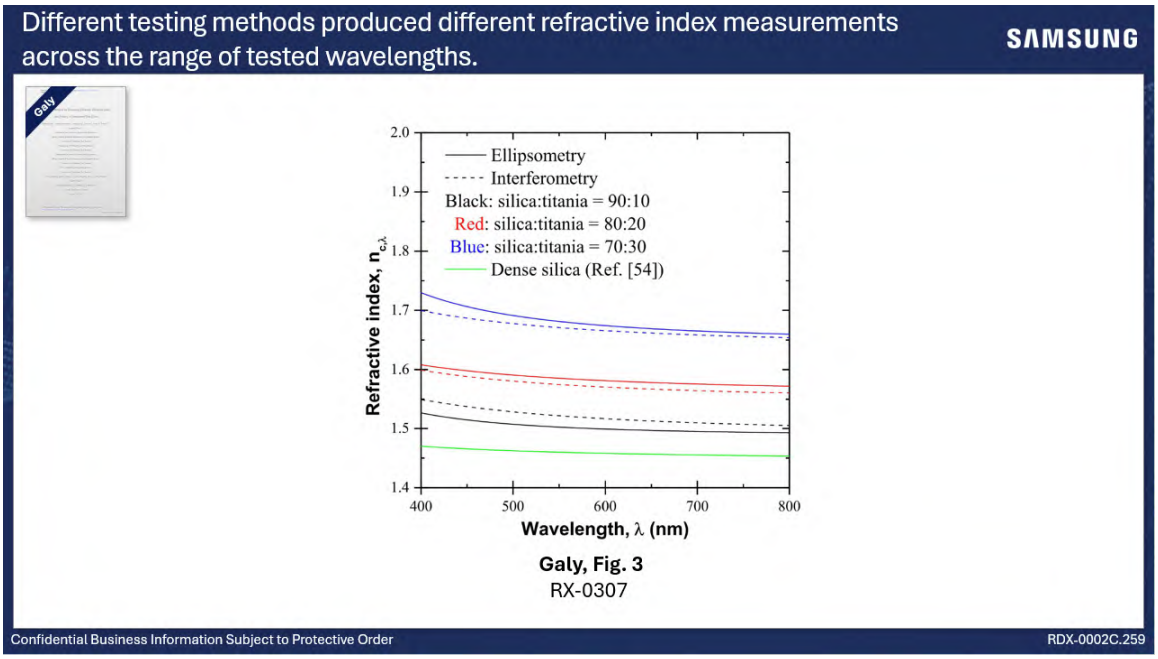
Q632 What is the refractive index?

A632 The refractive index is a well-known measure indicating how much the path of light is reflected when entering a material. The refractive index of a material is not a single number. Rather, the complex refractive index of a material, which includes the refractive index *n* and extinction coefficient *k*, is measured at different wavelengths of light. Typically, the refractive index of a material is provided as a graph with the wavelength of light being the X axis. For example, Dr. Foty cites to RX-0892 (Pan), *see* RX-0905C (Foty), ¶86 that includes a graph showing both the refractive index and extinction coefficient at different wavelengths, as RDX-0002C.258 illustrates.



Q633 How is a material's refractive index measured?

A633 Measuring the refractive index of materials, including thin film materials, has been an active area of research for many decades. As a result, numerous methods have been developed to determine a material's refractive index. For example, RX-0307 (Galy) compared the use of interferometry and ellipsometry to measure the effective refractive index. *See* RX-0307. RDX-0002C.259 illustrates the results of these techniques on three different compositions of silica-titania films. As it is readily apparent from Galy's Figure 3, the two testing methods produced different results across the range of tested wavelengths.



Q634 Besides how it is measured, are there other factors that may influence a material's refractive index?

A634 Yes. As another example, RX-0305 (Salwan) compared additional methods for determining the refractive index of thin films. *See* RX-0305.0001-7. Salwan explains that the refractive index of thin films varies on different parameters including: "deposition techniques, substrate temperature, annealing temperature, degree of oxidation, mixing ratio, density, doping, hydrogen content, films thickness, non-stoichiometry inhomogeneity, and anisotropy of the deposited films" and "other external effects such as temperature, pressure, electric field, light intensity, exciton modulation, radiation, fatigue, etching and aging effects." RX-0305.0006.

In my opinion, these variations illustrate why relying on the composition of a material, alone, is insufficient to determine the material's refractive index. Rather, the refractive index must be measured.

Q635 Are there any other reasons why you believe the refractive index must be measured?

A635 Yes. The papers relied upon by Dr. Foty in forming his infringement and technical DI opinions reinforce my conclusion that the refractive index of an accused product must be measured. For example, RX-0915 (Rammula) compares the refractive index of thin films deposited at different temperatures and pressures. *See* RX-0915, Fig. 11. Similarly, RX-0477 (Lan) compares the effects of deposition rates and anneal temperatures on the refractive index of Al_2O_3 films. *See* RX-0477, Figs. 1-2 (with and without chamber heating); *see also* RX-0482 (Wang), Figs. 3, 5. These papers illustrate examples of how the refractive index changes even in carefully controlled situations in which the differences in how the thin films were created have been carefully narrowed to a single variable, such as anneal temperature. Thus, in my opinion, the accused materials must be tested to determine their refractive index.

Q636 Do the Light Trapping Patents instruct POSITAs how to measure refractive indices?

A636 No. The specification does not provide instructions for how a material's refractive index should be measured. As discussed, different measurement techniques are likely to result in different values for the refractive index of the same material.

Additionally, the specification cites the refractive index as a single number, e.g., it states that "Hafnium Oxide … has a refractive index of about 1.9," '764 patent, 10:25-27, but does not specify a particular wavelength of light as reference. Choosing a different wavelength can also lead to different results for the same materials. *See* RX-0892 (Pan), Fig. 4; RX-0307 (Galy), Fig. 3. I was unable to locate any explicit instructions in the specification for how to determine the refractive index of a material, and the limited examples did not include sufficient detail to determine what method and wavelength should be used.

Q637 Does Dr. Foty rely on measurements of the materials in the Accused Products' refractive indices in support of his opinions that the Accused Products infringe?

A637 No. Dr. Foty does not rely on actual measurements of the Accused Products. Rather, Dr. Foty cites to values in different publications for layers that are purported to have similar compositions. *See generally* RX-0905C. By using this approach and relying on these references, Dr. Foty concluded that "hafnium oxide … [has] a refractive index generally above 2." RX-0905C, ¶441. This is a different value from the value in the patent's specification (1.9). '714 patent, 10:48-49 ("Hafnium oxide, which has a refractive index of about 1.9").

Q638 How does Dr. Foty's approach affect your opinion as to whether these claims are valid?

A638 In my opinion, Dr. Foty's approach to analyzing the claims renders the claim's scope indefinite. This is because whether a particular material in an Accused Product meets claim limitations related to its refractive index varies depending on arbitrary selection of published literature, including literature published after the patent's filing date—such as RX-0482 (Wang) published in 2015—and its arbitrary choice of wavelengths to highlight.

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For example, Dr. Foty states that RX-0482 (Wang) illustrates a "refractive index being about 1.65 in the middle of the range of wavelengths" and "with the refractive index begins to increase as the wavelength decreases." RX-0905C, ¶315. But even if the cited graph's indication of arbitrary units is ignored, the values for refractive index exceed 1.8 for certain wavelengths. RX-0482.3. The reason Dr. Foty chose to ignore the values at these wavelengths is unclear, but I am unable to locate any guidance in the specification that would lead to that result. Thus, Dr. Foty's approach to determining the refractive index appears to rely on arbitrary decisions made as to which publications to select and which wavelengths from the provided data to include in his calculation.

Q639 Are there other reasons why you believe Dr. Foty's approach renders these claims invalid?

A639 Yes. Additionally, Dr. Foty's reliance on an ever-evolving body of literature means that the same material's refractive index may change based on newly published works. Thus, an accused material may not meet the claim's limitation at the time it is manufactured but might suddenly be within the claim's scope based on a newly published study of refractive index. This is apparent from Dr. Foty now arguing that hafnium oxide has a higher refractive index than the value provided in the specification.

Accordingly, in my opinion, these claims are indefinite, at least as applied for infringement, because they fail to inform, with reasonable certainty, POSITAs about the scope of the invention.

[redacted]

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Dated: March 19, 2025



Dean P. Neikirk, Ph.D.

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APPENDIX OF EXHIBITS REFERENCED IN DEAN NEIKIRK WITNESS STATEMENT

Exhibit No.	Description
JX-0006	Certified File History - U.S. Patent No. 10,224,359
JX-0008	Certified File History - U.S. Patent No. 11,721,714
JX-0009	Certified File History - U.S. Patent No. 9,064,764
JX-0010	Certified File History - U.S. Patent No. 9,905,599
JX-0011	Certified U.S. Patent No. 10,244,359
JX-0013	Certified U.S. Patent No. 11,721,714
JX-0014	Certified U.S. Patent No. 9,064,764
JX-0015	Certified U.S. Patent No. 9,905,599
JX-0017C	2024.12.19 Transcript of Jason Sickler, Ph.D.
JX-0020C	2025.01.03 Transcript of Eric Mazur, Ph.D.
JX-0027C	2025.01.09 Transcript of Jeffrey Alan McKee
JX-0028C	2025.01.10 Transcript of James Carey, Ph.D.
JX-0035C	2025.01.15 Transcript of Chintamani Palsule, Ph.D., Corporate Designee & Individually
JX-0036C	2025.01.15 Transcript of Junseok Yang, Corporate Designee & Individually
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