

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Samsung Electronics Co., Ltd.,
Petitioner,

v.

SiOnyx, LLC,
Patent Owner.

Case No. IPR2025-00164
Patent No. 9,064,764

**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,064,764
UNDER 35 U.S.C. §§ 311–319 AND 37 C.F.R. § 42.100 *et seq.***

Table of Contents

I.	Introduction.....	1
II.	Standing, Mandatory Notices, and Fee Authorization	1
III.	Summary of Challenge	2
IV.	Overview of The '764 Patent.....	4
V.	Level of Ordinary Skill.....	5
VI.	Claim Construction.....	5
VII.	Application of Prior Art to the Challenged Claims.....	6
A.	Ground 1: Claims 8–15 Are Anticipated, Or At A Minimum, Obvious Based on Hwang.....	6
1.	Overview of Hwang.....	6
2.	Claim 8.....	7
a)	8[pre]: “A light trapping device, comprising”	7
b)	8[a]: “at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery”	8
c)	8[b]: “a backside light trapping material substantially covering the backside surface”.....	12
d)	8[c]: “a peripheral light trapping material substantially covering the peripheral sidewall”.....	15
e)	8[d]: “wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials”.....	17

f)	8[e]: “wherein the difference in refractive index between the first material and the two second materials is at least 0.2,”	21
g)	8[f]: “wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel”	21
3.	Claim 9: “The device of claim 8, wherein the two second materials have a refractive index of less than about 2.1.”	22
4.	Claim 10: “The device of claim 9, wherein at least one of the two second materials includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.”	22
5.	Claim 11: “The device of claim 9, wherein the at least one of the two second materials includes a member selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.”	23
6.	Claim 12: “The device of claim 8, wherein the first material includes a material having a refractive index of greater than or equal to about 2.1.”	23
7.	Claim 13: “The device of claim 12, wherein the first material includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and combinations thereof.”	23
8.	Claim 14: “The device of claim 8, wherein the peripheral sidewall extends completely around the pixel periphery.”	24
9.	Claim 15: “The device of claim 8, wherein the peripheral sidewall extends from the light incident surface to the backside surface.”	25
B.	Ground 2: Claims 16–25 Are Obvious Based on Hwang and Konno.	26
1.	Overview of Konno.....	26

2.	Claim 17	29
a)	Limitations 17[pre]–[c], [e]	29
b)	17[d]: “wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface”	29
3.	Claim 21	32
a)	Limitations 21[pre]–[c], [e]	32
b)	21[d]: “a textured layer positioned to interact with light proximal to the backside surface”	32
4.	Claims 16, 20, 25: “The device of claim [8, 17, 21], wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”	36
5.	Claims 18, 23	39
6.	Claims 19, 24	39
7.	Claim 22: “The device of claim 21, wherein the textured layer is located between the backside surface and the backside light trapping material.”	40
C.	Ground 3: Claims 1–5, 7 Are Obvious Based on Hwang and Mori.	41
1.	Overview of Mori.....	41
2.	Claim 1	44
a)	Limitations 1[pre]–[c], [f].....	44
b)	1[d]: “wherein at least one of the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials”	44

c)	1[e]: “wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field”	45
3.	Claim 2: “The device of claim 1, wherein the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.”	49
4.	Claim 3: “The device of claim 1, wherein the dopant is boron or antimony.”	49
5.	Claims 4, 5	50
6.	Claim 7: “An array of light trapping pixel devices of claim 1.”	50
D.	Ground 4: Claim 6 Are Obvious Based on Hwang, Mori, and Konno	51
1.	Claim 6: “The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”	51
E.	Ground 5: Claims 8, 12, 14–16 Are Obvious Based on Yamada	52
1.	Overview of Yamada	52
2.	Claim 8	53
a)	8[pre]: “A light trapping device, comprising”	53
b)	8[a]: “at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery”	54
c)	8[b]: “a backside light trapping material substantially covering the backside surface”	58

d)	8[c]: “a peripheral light trapping material substantially covering the peripheral sidewall”	59
e)	8[d]: “wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials”	61
f)	8[e]: “wherein the difference in refractive index between the first material and the two second materials is at least 0.2”	62
g)	8[f]: “wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel”	62
3.	Claim 12: “The device of claim 8, wherein the first material includes a material having a refractive index of greater than or equal to about 2.1.”	63
4.	Claim 14: “The device of claim 8, wherein the peripheral sidewall extends completely around the pixel periphery.”	63
5.	Claim 15: “The device of claim 8, wherein the peripheral sidewall extends from the light incident surface to the backside surface.”	64
6.	Claim 16: “The device of claim 8, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”	65
F.	Ground 6: Claims 8–11, 13 Are Obvious Based on Yamada and Schubert.....	65
1.	Overview of Schubert	65
2.	Claim 8.....	65
a)	Limitations 8[pre]–[c], [f].....	65

b)	8[d]: “wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials”	66
c)	8[e]: “wherein the difference in refractive index between the first material and the two second materials is at least 0.2”	69
3.	Claim 9: “The device of claim 8, wherein the two second materials have a refractive index of less than about 2.1.”	69
4.	Claim 10: “The device of claim 9, wherein at least one of the two second materials includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.”	69
5.	Claim 11: “The device of claim 9, wherein the at least one of the two second materials includes a member selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.”	70
6.	Claim 13: “The device of claim 12, wherein the first material includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and combinations thereof.”	70
G.	Ground 7: Claims 1–7 Are Obvious Based on Yamada, Schubert, and Mori.	71
1.	Claim 1	71
a)	Limitations 1[pre]–[c], [f]	71
b)	1[d]: “wherein at least one of the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials”	71

c)	1[e]: “wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field,”	72
2.	Claim 2: “The device of claim 1, wherein the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.”	74
3.	Claim 3: “The device of claim 1, wherein the dopant is boron or antimony.”	75
4.	Claims 4–5	75
5.	Claim 6: “The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”	76
6.	Claim 7: “An array of light trapping pixel devices of claim 1.”	76
H.	Ground 8: Claims 17–25 Are Obvious Based on Yamada and Konno.	77
1.	Claim 17	77
a)	Limitations 17[pre]–[c], [e]	77
b)	17[d]: “wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface”	77
2.	Claim 21	79
a)	Limitations 21[pre]–[c],[e]	79
b)	21[d]: “a textured layer positioned to interact with light proximal to the backside surface”	79
3.	Claim 22: “The device of claim 21, wherein the textured layer is located between the backside surface and the backside light trapping material.”	83

Petition for *Inter Partes* Review of U.S. Pat. No. 9,064,764

4.	Claims 18, 23	84
5.	Claims 19, 24	84
6.	Claims 20, 25	84
VIII.	Discretionary Denial Is Inappropriate	85
IX.	Conclusion	85

List of Exhibits

Exhibit	Description
1001	U.S. Patent No. 9,064,764 (“the ’764 patent”)
1002	File History for U.S. Patent No. 9,064,764
1003	Declaration of Dr. Michael Lebby
1004	Curriculum Vitae of Dr. Michael Lebby
1005	U.S. Patent No. 7,675,099 (Hwang)
1006	Japanese Patent Application Publication No. 2011-119558 (Mori)
1007	Certified English Translation of Japanese Patent Application Publication No. 2011-119558 (Mori)
1008	[not used]
1009	[not used]
1010	U.S. Patent No. 7,709,775 (Konno)
1011	Japanese Patent Application Publication No. 2009-188316 (Yamada)
1012	Certified English Translation of Japanese Patent Application Publication No. 2009-188316 (Yamada)
1013	E. Fred Schubert, LIGHT-EMITTING DIODES (2nd ed. 2006) (Excerpt)
1014	Samsung’s Proposed Constructions, Inv. No. 337-TA-1403 (Aug. 27, 2024)
1015	SiOnyx’s Proposed Constructions, Inv. No. 337-TA-1403 (Aug. 27, 2024)
1016	Email from N. Subhedar re: Claim Construction M&C Follow-Up (Sept. 8, 2024)
1017	Joint Proposed Claim Construction Chart, Inv. No. 337-TA-1403 (Nov. 1, 2024)
1018	Stanley Wolf, MICROCHIP MANUFACTURING (2003) (Excerpts)
1019	U.S. Patent Application Publication No. 2012/0025199 (Chen)
1020	U.S. Patent No. 8,288,836
1021	Sadao Adachi, Optical Constants of Crystalline and Amorphous Semiconductors, Numerical Data and Graphical Information (1st Ed. 1999) (Excerpt)
1022	U.S. Patent No. 4, 644,553
1023	George Hass & Calvin D. Salzberg, <i>Optical Properties of Silicon Monoxide in the Wavelength Region from 0.24 to 14.0 Microns</i> , Vol. 44 No. 3, JOURNAL OF THE OPTICAL SOCIETY OF AM., 181 (1954)

Petition for *Inter Partes* Review of U.S. Pat. No. 9,064,764

Exhibit	Description
1024	F. Lopez & E. Bernab��, <i>Refractive Index of Vacuum-Evaporated SiO Thin Films: Dependence on Substrate Temperature</i> , ELECTRONICS & OPTICS, 13 (1990)

I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner”) petitions for *inter partes* review seeking cancellation of claims 1–25 (the “Challenged Claims”) of U.S. Patent No. 9,064,764 (Ex-1001, “the ’764 patent”).

II. STANDING, MANDATORY NOTICES, AND FEE AUTHORIZATION

Grounds for Standing: Pursuant to 37 C.F.R. §42.104(a), Petitioner certifies that the ’764 patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the ’764 patent on the grounds identified in this petition.

Real Parties-in-interest: The real parties-in-interest are Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.

Related Matters: Petitioner identifies the following related matters.

- *Sensors with Pixels and Products Containing the Same*, Inv. No. 337-TA-1403 (ITC) (the “Related Case”)
- *SiOnyx, LLC v. Samsung Electronics, Co., Ltd.*, 2:24-cv-00291 (E.D. Tex.)

Counsel Information: Petitioner designates the following counsel:

Lead Counsel	Back-Up Counsel
David A. Garr (Reg. No. 74,932) dgarr@cov.com Covington & Burling LLP One CityCenter, 850 Tenth Street NW Washington, DC 20001	Scott C. Weidenfeller (Reg. No. 54,531) sweidenfeller@cov.com Covington & Burling LLP One City Center, 850 Tenth Street NW Washington, DC 20001

T: (202) 662-6000; F: (202) 662-6291	T: (202) 662-5923; F: (202) 778-5923
	Alice J. Ahn (Reg. No. 79,829) aahn@cov.com Covington & Burling LLP Salesforce Tower 415 Mission Street, Ste. 5400 San Francisco, CA 94105-2533 T: (415) 591-7091; F: (415) 955-6591

Service Information: Service information is provided in the designation of counsel above. Petitioner consents to service of all documents via electronic mail at the email addresses above and at Samsung-SiOnyx-IPR-Cov@cov.com.

Fee Authorization: The Office is authorized to charge all fees due in connection with this proceeding to Deposit Account No. 60-3160.

III. SUMMARY OF CHALLENGE

This petition presents the following claim challenges:

- ***Ground 1:*** Claims 8–15 are anticipated, or at a minimum obvious, obvious based on Hwang
 - ***Ground 2:*** Claims 16–25 are obvious based on Hwang and Konno
 - ***Ground 3:*** Claims 1–5, 7 are obvious based on Hwang and Mori
 - ***Ground 4:*** Claim 6 are obvious based on Hwang, Mori, and Konno
- ***Ground 5:*** Claims 8, 12, 14–16 are obvious based on Yamada

- **Ground 6:** Claims 8–11, 13 are obvious based on Yamada and Schubert
 - **Ground 7:** Claims 1–7 are obvious based on Yamada, Schubert, and Mori
- **Ground 8:** Claims 17–25 are obvious based on Yamada and Konno

The '764 patent was filed on March 15, 2023 and claims priority through a chain of applications to a provisional application filed on March 22, 2012. Each asserted reference is available as prior art under 35 U.S.C. §102, as shown below:

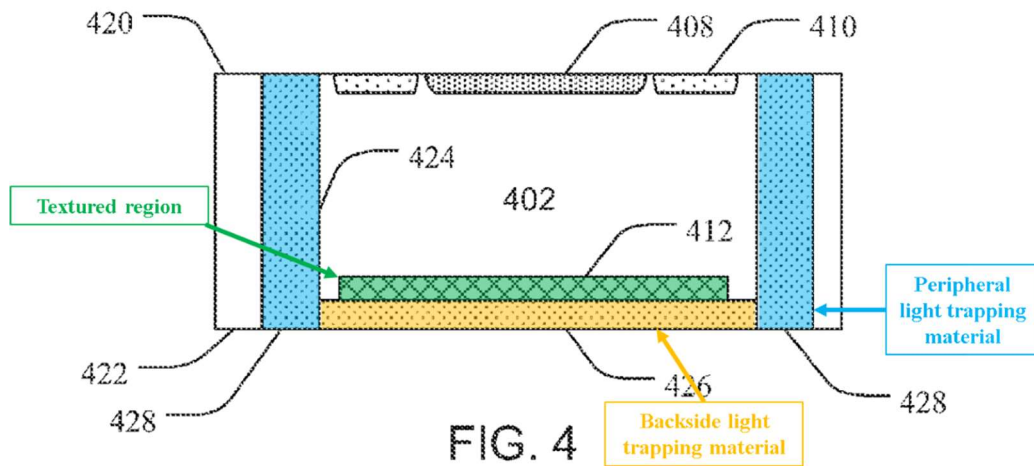
Exhibit	Reference	Date(s)	Availability as Prior Art
1005	U.S. Patent No. 7,675,099 (Hwang)	March 9, 2010 (issued)	§§102(a)–(b), (e)
1010	U.S. Patent No. 7,709,775 (Konno)	May 4, 2010 (issued)	§§102(a)–(b), (e)
1006 (certified translation Ex-1007)	Japanese Patent Application Publication No. 2011-119558 (Mori)	June 16, 2011 (published)	§§102(a)
1011 (certified translation Ex-1012)	Japanese Patent Application Publication No. 2009-188316 (Yamada)	August 20, 2009 (published)	§§102(a)–(b)
1013 (excerpted Chapter 10)	E. Fred Schubert, Light-Emitting Diodes (2nd ed. 2006)	2006 (published)	§§102(a)–(b)

None of these references were cited during prosecution or considered by the Examiner. The supporting declaration of Dr. Michael Lebby (Ex-1003) was also not

before the Examiner. Accordingly, the prior art and arguments in this Petition are not the same, or substantially the same, as those previously presented to the Office under 35 U.S.C. §325(d).

IV. OVERVIEW OF THE '764 PATENT

The '764 patent relates to elements for trapping light within image sensor pixels, and purportedly provides for “enhanced light detection properties.” '764 patent, 5:64–67. During prosecution, the patent examiner issued a restriction and election requirement. Ex-1002 at 385–92. In response, the applicant “elect[ed] Species 4, embodiment of FIG. 4,” shown below. *Id.* at 417.



'764 Patent, Fig. 4 (annotated). As shown in the Figure, this embodiment includes a “backside light trapping material,” a “peripheral light trapping material,” and “an optional textured region 412.” *E.g.*, '764 patent, 10:56–11:9. “[L]ight contacting the backside light trapping material 426 or the peripheral light trapping material 428 is reflected back towards the pixel 402.” *Id.*, 11:3–5. The textured layer “can act as a

diffusive scattering site for the incident” light. *Id.*, 7:66–8:4.

V. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art (“POSITA”) as of March 2012 would have had a Bachelor’s degree in engineering, physics, or a related or equivalent field, and two or more years of experience researching, developing, designing, and/or evaluating image sensors using photonics. Ex-1003, ¶51. A person with less or different education but more relevant practical experience, or vice versa, may also meet this standard. *Id.*

VI. CLAIM CONSTRUCTION

For purposes of this petition, Petitioner does not believe that any specialized claim constructions are necessary. However, in the Related Case the parties have proposed constructions for certain terms, which are addressed as relevant below. *See* Exs. 1014–17.¹

¹ Petitioner notes that it raised in the Related Case contentions that certain claim terms are indefinite. For purposes of this proceeding, Petitioner adopts Patent Owner’s position that such terms are not indefinite.

VII. APPLICATION OF PRIOR ART TO THE CHALLENGED CLAIMS

A. Ground 1: Claims 8–15 Are Anticipated, Or At A Minimum, Obvious Based on Hwang

1. Overview of Hwang

Hwang is directed to “an image sensor with an increased spectral sensitivity,” “capable of minimizing interference between neighboring pixels” by using base and sidewall multi-layered reflection layers as illustrated below. Hwang, 1:52–67.

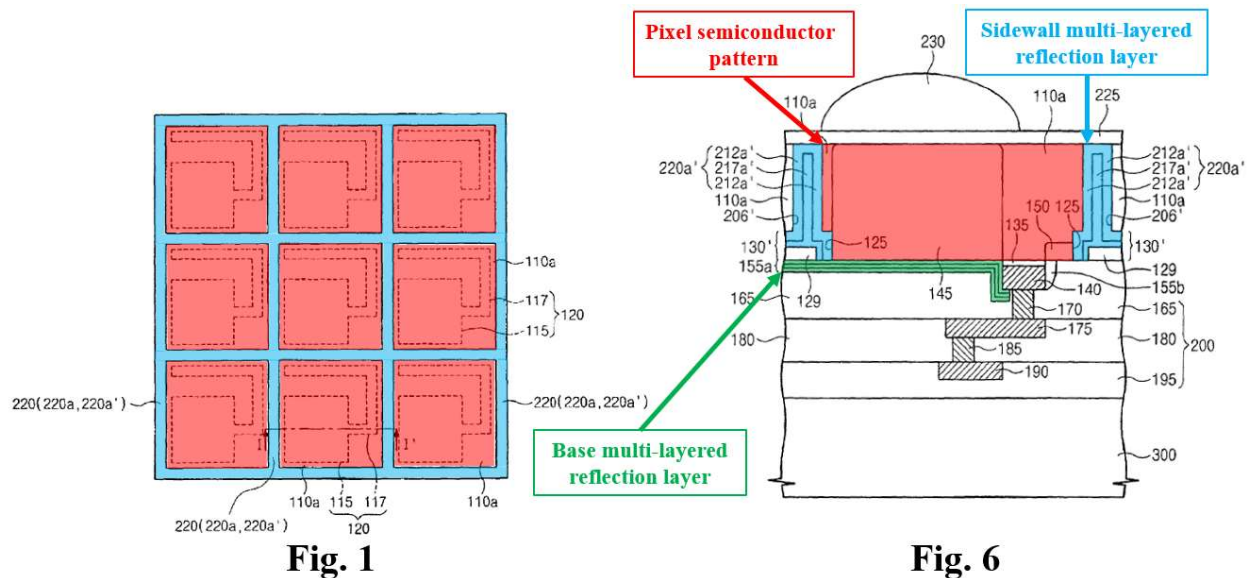


Fig. 1

Fig. 6

Id., Figs. 1, 6 (annotated) 4:59–63; Ex-1003, ¶¶55–59.² Like the '764 patent, Hwang

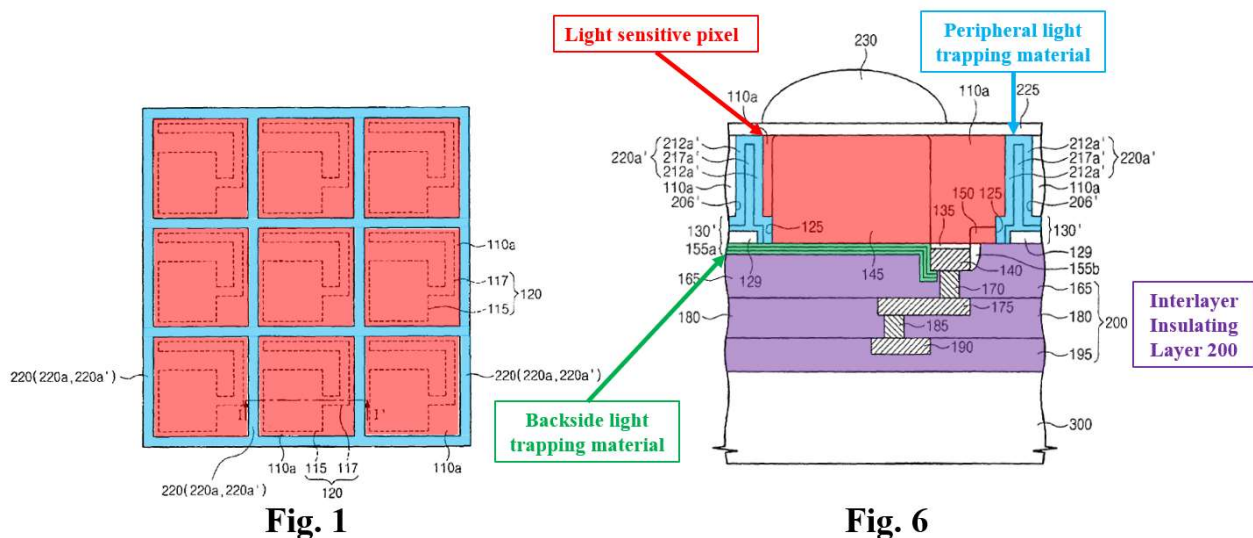
² Figures 2 and 6 use differently arranged sidewall multi-layered reflection layers but are otherwise the same. *See* Hwang, 11:57–60; Ex-1003, ¶57. Therefore, POSITAs would appreciate that Hwang’s disclosures for elements in Figure 2 (including layer 220 comprising layers 210 and 215) are pertinent to corresponding elements in Figure 6 (including layer 220a’ comprising layers 212a’ and 217a’).

concerns improving image quality by increasing the percent of incident light the photodiode absorbs. *E.g., id.*, 1:31–36.

2. Claim 8

a) 8 ``` [pre]: “A light trapping device, comprising” ```

To the extent the preamble is limiting, Hwang teaches or suggests it. Ex-1003, ¶¶60–63. As illustrated below, Hwang discloses an “image sensor that converts incident light to electrical signals,” Hwang, 1:14–18, using base and sidewall multi-layered reflection layers (155a and 220a', respectively) for *trapping light* by reflecting light back into the pixel. Ex-1003, ¶¶61–63. *E.g.*, Hwang, 6:7–9, 7:45–74, 9:10–11; 10:28–35; 11:57–12:31; 15:36–48.³



Id., Fig. 1, 6 (annotated), 4:59–63; Ex-1003, ¶¶61–63.

³ All emphasis added except where otherwise noted.

- b) 8[a]: “at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery”

Hwang’s image sensor comprises *at least one light sensitive pixel*. Ex-1003, ¶¶64–65. As depicted below, it includes “a plurality of pixel semiconductor patterns 110a,” Hwang 5:52–59 (each containing a “photodiode 145 disposed therein,” *id.*) to convert light to electrical signals, *id.*, 1:23–29.⁴

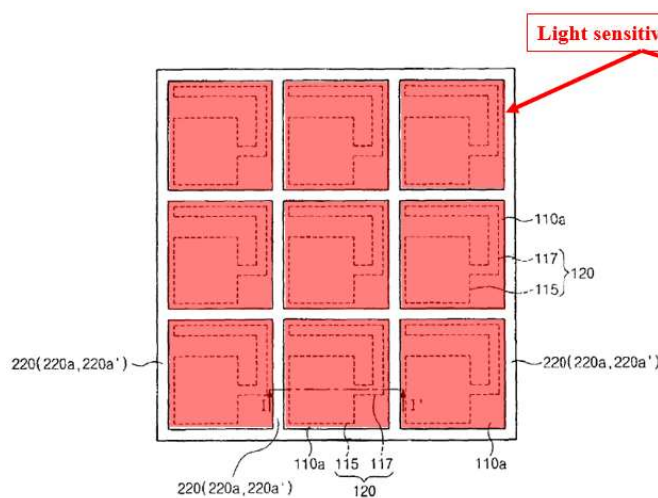


Fig. 1

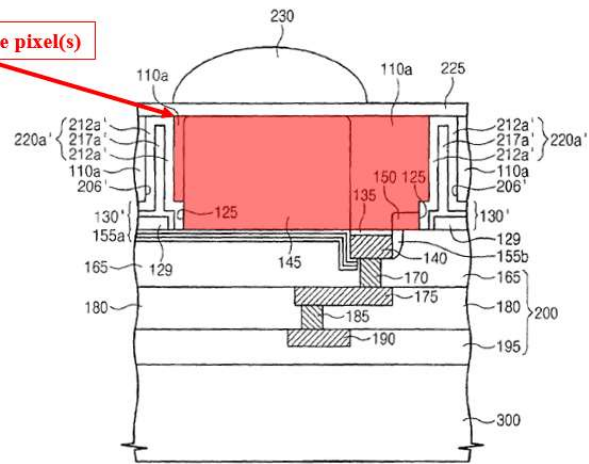


Fig. 6

⁴ While Hwang calls element 145 a “photodiode,” POSITAs would understand that term (i.e., the structure that converts light into an electrical signal) encompasses more than just element 145, and would further include the surrounding pixel semiconductor patterns 110a. Ex-1003, ¶65. See Hwang, 5:52–6:6 (“photodiodes 145 form a PN junction with the pixel semiconductor pattern 110a”).

Id., Fig. 1, 6 (annotated); Ex-1003, ¶65.

Each pixel (110a) further has a *light incident surface* and a *backside surface* opposite the *light incident surface*, as illustrated below.

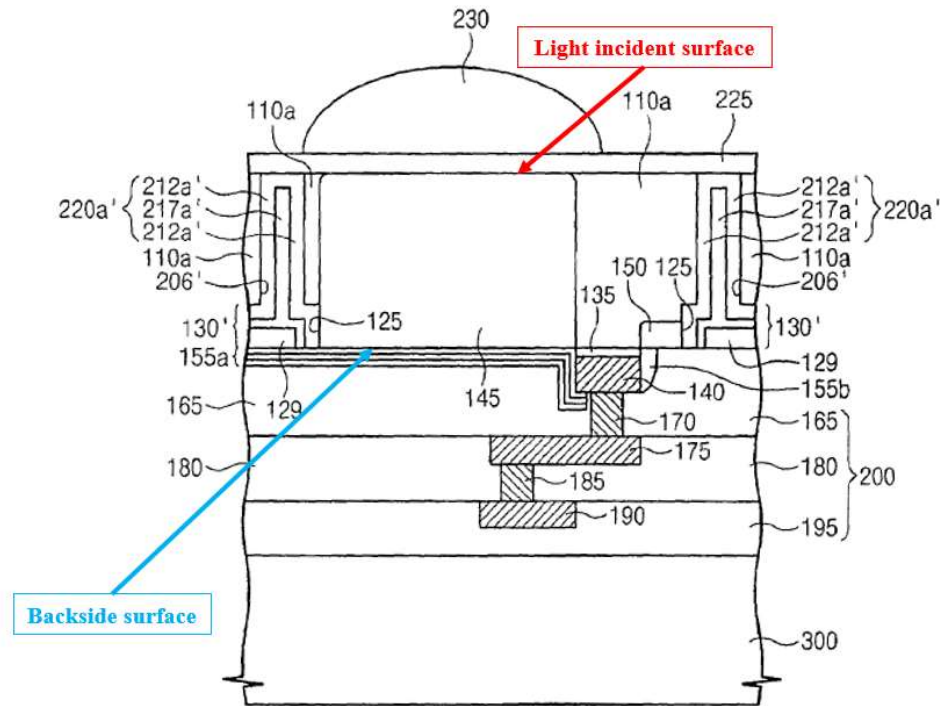


Fig. 6

Hwang, Fig. 6 (annotated); Ex-1003, ¶66. “The pixel semiconductor patterns 110a have first and second surfaces in parallel, i.e., that face one another,” where “the first surface ... is more proximate to the substrate 300 than is the second surface.” Hwang, 6:37–40. Hwang’s “second surface” constitutes a *light incident surface*, see Hwang, 8:17–22 (“[e]xternal light ... is incident on the second surface of the photodiode 145.”), and its “first surface” constitutes a *backside surface opposite the light incident surface*. Ex-1003, ¶¶67–69.

Each pixel further has *a peripheral sidewall disposed into at least a portion of the pixel*, as illustrated below.

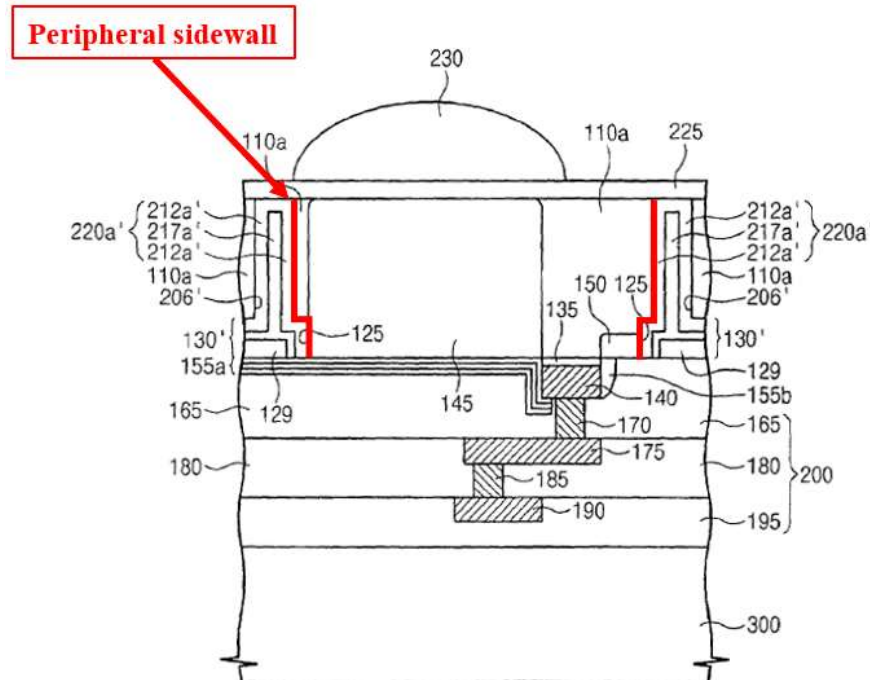


Fig. 6

Hwang, Fig. 6 (annotated); Ex-1003, ¶70.

Hwang’s “sidewall multi-layered reflection layer 220a’ is disposed within a groove 206’ formed between pixel semiconductor patterns 110a’.” Hwang, 11:64–66; *see also id.*, 6:7–9 (“sidewall multi-layered reflection layer 220 [220a’ in Figure 6] is provided between the side walls of the pixel semiconductor pattern 110a”). Thus, pixel (110a) includes a *peripheral sidewall* where it contacts the sidewall reflection layer 220a’. Ex-1003, ¶71.

This peripheral sidewall is *disposed into at least a portion of the pixel*. As shown below, it runs from the pixel’s “second surface” (*light incident surface*) to its

“first surface” (*backside surface*)—just like peripheral sidewall 424 in the ’764 patent. *See* ’764 patent, Fig. 4, 10:58–64 (illustrating “peripheral sidewall 424 disposed into at least a portion of the pixel 402”).

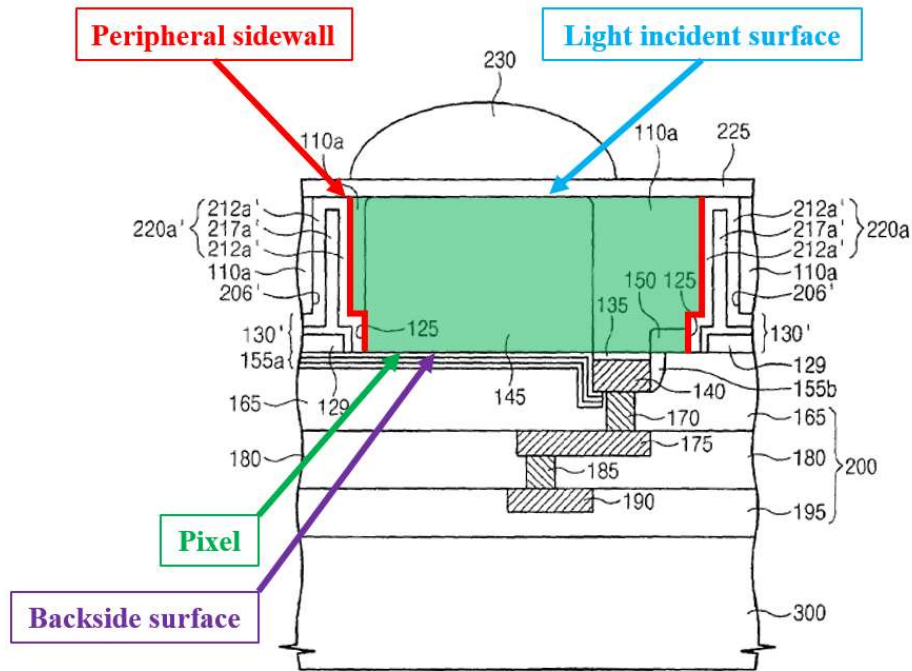


Fig. 6

Hwang, Fig. 6 (annotated); Ex-1003, ¶72.

The peripheral sidewall further *extend[s]* at least substantially around the pixel periphery. Ex-1003, ¶73. As illustrated below, “sidewall multi-layered reflection layer 220 [220a’ in Figure 6] encloses the side walls of the pixel semiconductor patterns 110a.” Hwang, 6:15–17.

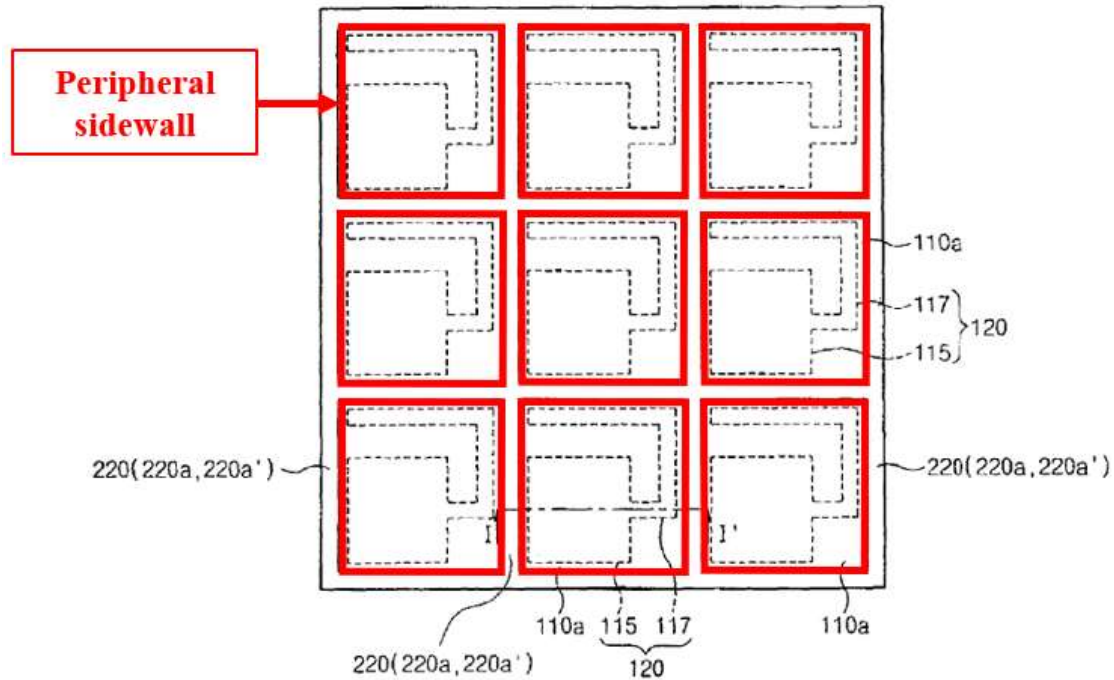
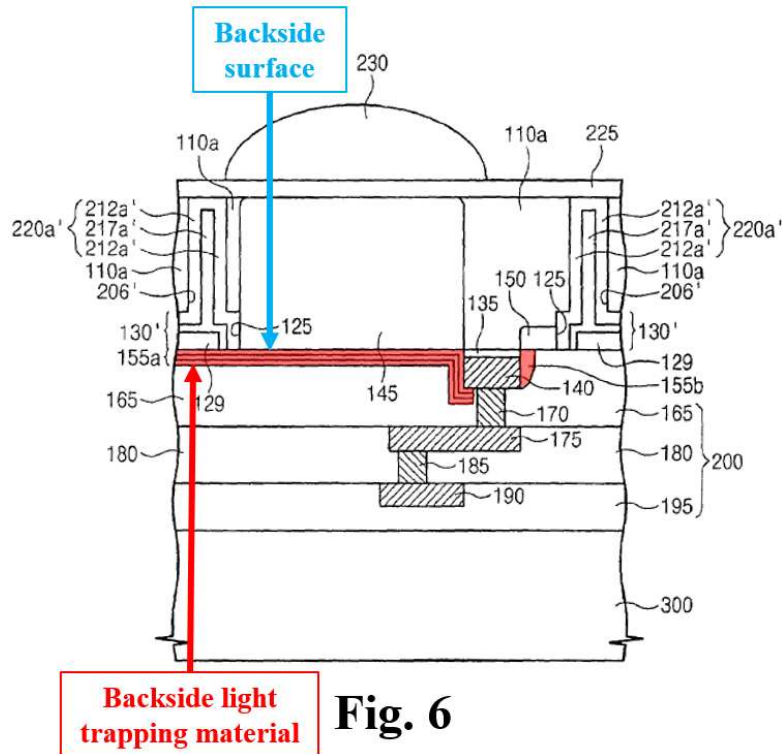


Fig. 1

Id., Fig. 1 (annotated); Ex-1003, ¶73. See Hwang, 11:61.

c) 8[b]: “a backside light trapping material substantially covering the backside surface”

Hwang’s image sensor includes a *backside light trapping material substantially covering the backside surface* of the pixel. Ex-1003, ¶¶75–79. As illustrated below, Hwang’s “base multi-layered reflection layer 155a is interposed between the photodiode 145 and the interlayer insulating layer 200,” Hwang, 7:45–47, and “contacts the first surface [*backside surface*],” *id.*, 8:32–33. Hwang’s “gate spacer 155b can include the same material as the base multi-layered reflection layer 155a.” *Id.*, 7:53–55.



Hwang Fig. 6 (annotated); Ex-1003, ¶76.

This material traps light, as “external light incident on ... photodiode 145 is reflected by ... base multi-layered reflection layer 155a,” and is therefore “incident again on the photodiode.” Hwang, 9:6–14; Ex-1003, ¶77.

Hwang teaches that the light trapping material *substantially covers* the backside surface. Ex-1003, ¶78. Although Hwang’s Figure 6 depicts base multi-layered reflection layer 155a covering the backside surface of photodiode 145, Hwang also teaches “[a] layer of the base multi-layered reflection layer contacting the pixel semiconductor pattern,” i.e. 110a. Hwang, 4:33–36. In Figure 9, Hwang depicts multi-layered reflection layer 155a completely covering the backside surface, including both photodiode 145 and pixel semiconductor pattern 110a.

155b “can include the same material as the base multi-layered reflection layer 155a,” Hwang, 7:53–55, so as to minimize the area not covered by the base multi-layered reflection layer. Ex-1003, ¶78.

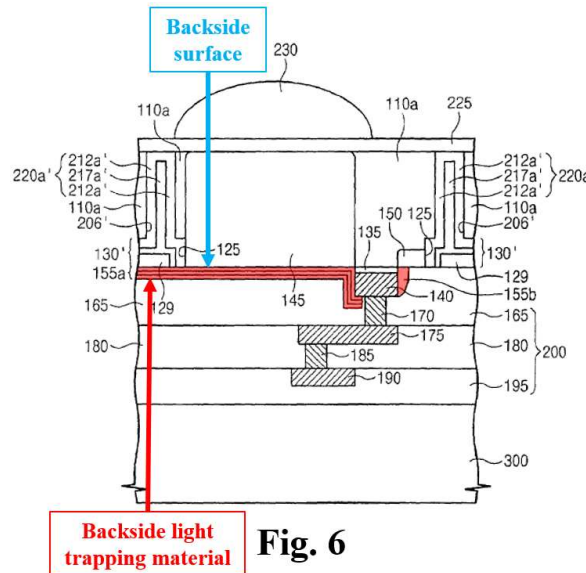


Fig. 6

Hwang, Fig. 6 (annotated).

d) 8[c]: “a peripheral light trapping material substantially covering the peripheral sidewall”

Hwang’s image sensor includes a *peripheral light trapping material substantially covering the peripheral sidewall*. Ex-1003, ¶¶80–84. As illustrated below, Hwang’s “sidewall multi-layered reflection layer 220a’ is disposed within a groove 206’ formed between pixel semiconductor patterns 110a.” Hwang, 11:64–66. *See* Hwang 9:41–43 (“sidewall multi-layered reflection layer 220 [220a’ in Figure 6] is disposed between the side walls of the pixel semiconductor pattern 110a.”).

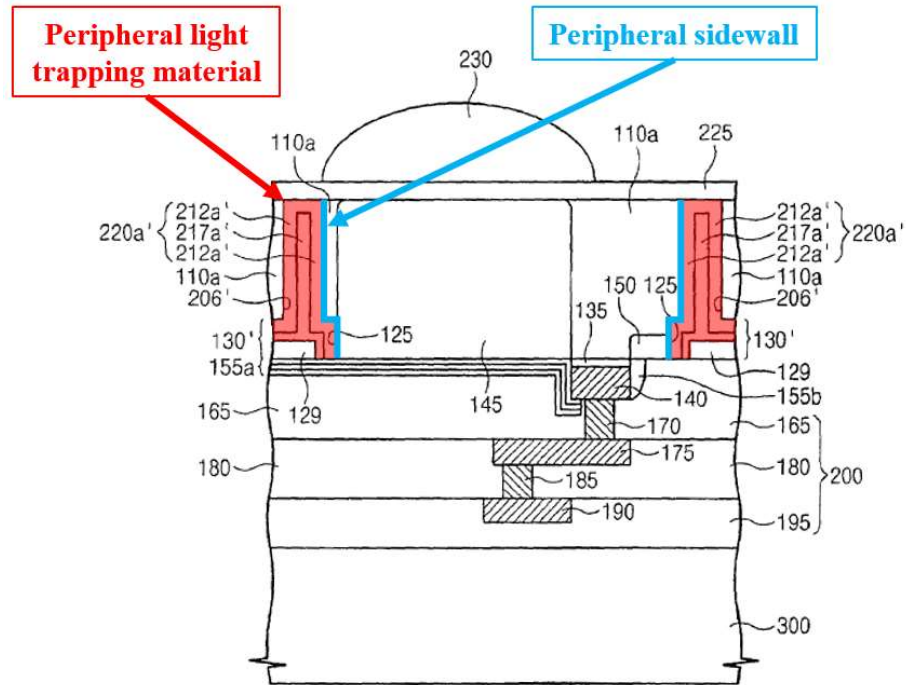


Fig. 6

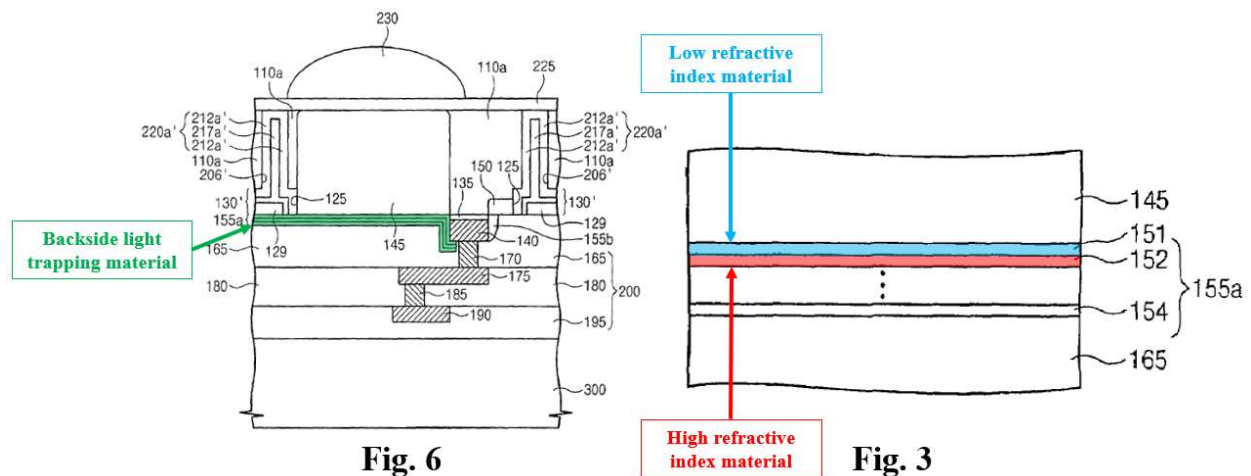
Id., Fig. 6 (annotated); Ex-1003, ¶81. “The sidewall multi-layered reflection layer 220 [220a’ in Figure 6] encloses the side walls of the pixel semiconductor pattern 110a,” and can also “contact the sidewalls of the pixel semiconductor patterns 110a.” *Id.*, 6:15–17, 9:43–45. *See* Ex-1003, ¶83.

This layer traps light, as light is “reflected from ... the sidewall multilayered reflection layer 220 [220a’ in Figure 6],” and is therefore “incident again on the photodiode 145, so that the absorption efficiency of external light is increased.” Hwang, 10:28–35. Additionally, “sidewall multi-layered reflection layer 220 [220a’ in Figure 6] minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels.” *Id.*, 10:23–27; Ex-1003, ¶82.

- e) 8[d]: “wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials”

Hwang teaches or suggests this limitation.⁵ Ex-1003, ¶¶85–95.

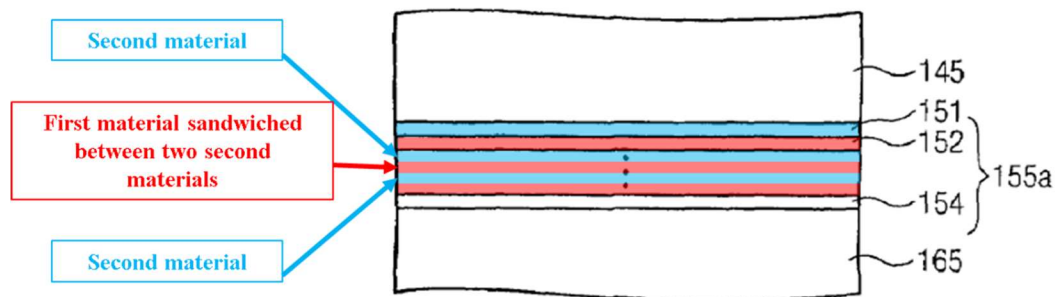
First, Hwang’s backside light trapping material includes a first material sandwiched between two second materials. Ex-1003, ¶¶86–90. As illustrated below, Hwang’s “base multi-layered reflection layer 155a can include a first base multi-layered reflection layer 151 and a second base multi-layered reflection layer 152.” Hwang, 8:40–52.



⁵ In the Related Proceeding, Patent Owner proposed a construction that “the two second materials can be different from one another” (i.e., they need not be different materials). Ex-1015 at 2. Petitioner adopts Patent Owner’s position for purposes of this proceeding.

Id., Figs. 6, 3 (annotated); Ex-1003, ¶¶87–89.⁶ “[T]he first and second base multi-layered reflection layers 151 and 152 [are] respectively formed of silicon oxide (with a refractive index of approximately 1.46) and silicon (with a refractive index of approximately 4).” Hwang, 9:25–30.⁷

Additionally, these “first and second base multi-layered reflection layers 151 and 152 [can be] alternately stacked a plurality of times.” Hwang, 8:54–56; *see also id.*, 9:25–26. Accordingly, as illustrated below, Hwang’s *backside light trapping material* includes a first material (second base layer 152) sandwiched between two second materials (first base layers 151).



Modified Fig. 3

⁶ Figure 3 is an enlarged view of base multi-layered reflection layer 155a in Figure 2. Hwang, 4:64.

⁷ POSITAs would understand Hwang’s “silicon oxide” to mean specifically “silicon dioxide” (SiO₂), as Hwang discloses it has “a refractive index of approximately 1.46.” Hwang, 9:28–29. Ex-1003, ¶88; Schubert at 181 (“SiO₂ ($\bar{n} \approx 1.46$)”).

Hwang, Fig. 3 (annotated, modified); Ex-1003, ¶¶90. Additionally, *the first material has a higher refractive index (approximately 4) as compared to the two second materials (approximately 1.46). See Hwang, 9:25–30 (disclosing refractive indices).*

Second, Hwang’s peripheral light trapping material includes a first material sandwiched between two second materials. Ex-1003, ¶¶91–95. As illustrated below, Hwang’s “sidewall multi-layered reflection layer 220a’” includes a first sidewall reflection layer 212a’ and a second sidewall reflection layer 217a’,” wherein “[t]he second sidewall reflection layer 217a’ is disposed below the first sidewall reflection layer 212a.’” Hwang, 11:64–12:23.

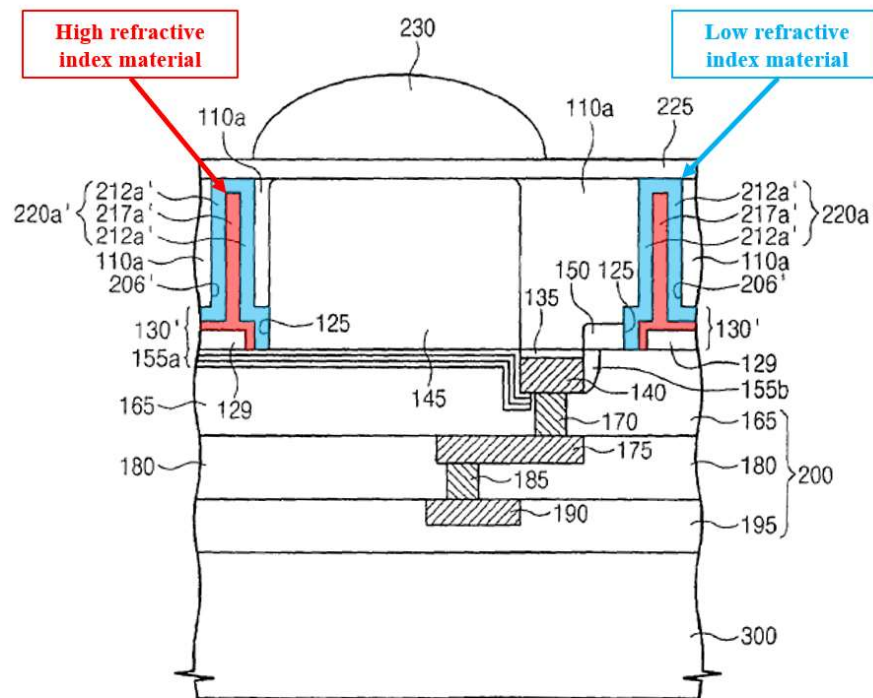
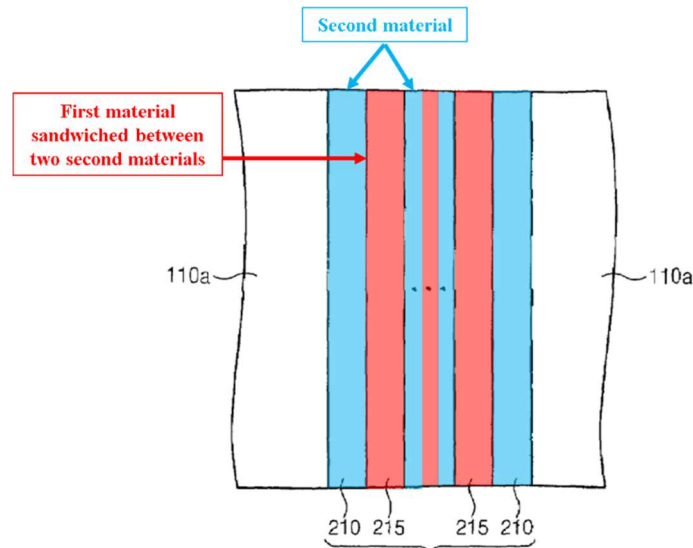


Fig. 6

Hwang, Fig. 6 (annotated); Ex-1003, ¶¶92–93. “[T]he first sidewall reflection layer 212a’” has “a lower refractive index than ... the second sidewall reflection layer

217a’.” Hwang, 12:4–7. For example, “first sidewall reflection layer 210 [212a’ in Figure 6] can be a silicon oxide layer” and “second sidewall reflection layer 215 [217a’ in Figure 6] can be a silicon layer.” Hwang, 10:2–5.

Hwang explains that “[t]he first and second sidewall reflection layers 212a’ and 217a’ can be alternatively disposed at least once,” i.e., they can be alternatively stacked a plurality of times. Hwang, 12:24–25. Ex-1003, ¶¶94. As illustrated below, Hwang accordingly teaches use of a *peripheral light trapping material* including a *first material* (second sidewall reflection layer 217a’), *sandwiched between two second materials* (first sidewall reflection layer 212a’).



Modified Fig. 4

Hwang, Fig. 4 (annotated, modified); Ex-1003, ¶94.⁸ Additionally, *the first material has a higher refractive index (approximately 4) as compared to the two second materials (approximately 1.46). See* Hwang, 9:25–30 (disclosing refractive indices).

f) 8[e]: “wherein the difference in refractive index between the first material and the two second materials is at least 0.2,”

Hwang teaches or suggests this limitation. Ex-1003, ¶96. Both Hwang’s backside and peripheral light trapping material (155*a* and 220*a*’) include a *first material* (layers 152 and 217*a*’) having a “a refractive index of approximately 4,” Hwang, 9:25–30, *sandwiched between two second materials* (layers 151 and 212*a*’) having “a refractive index of approximately 1.46,” *id.*, 9:25–30—with a difference of approximately 2.54 (i.e., *at least 0.2*). *Supra*, §VII.A.2.e (claim 8[d]). *See* Hwang, 8:40–52, 10:2–5.

g) 8[f]: “wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel”

Hwang discloses *that light contacting both the backside light trapping material [and] the peripheral light trapping material is reflected back towards the pixel*. Ex-1003, ¶¶97–100. That is, “external light incident on ... photodiode 145 is

⁸ Figure 4 is an enlarged view of the sidewall reflection layer 220 in Figure 2. Hwang, 9:37–40.

reflected by ... base multi-layered reflection layer 155a” (*backside light trapping material*) and is therefore “incident again on the photodiode 145.” Hwang, 9:6–14. Similarly, light is “reflected by ... the sidewall multi-layered reflection layer 220 [220a’ in Figure 6]” (*peripheral light trapping material*) and is therefore “incident again on the photodiode 145....” *Id.*, 10:28–35.

3. Claim 9: “The device of claim 8, wherein the two second materials have a refractive index of less than about 2.1.”

Hwang teaches or suggests this limitation. Ex-1003, ¶101. Hwang’s *two second materials* (151 and 212a’—used in the backside and peripheral light trapping materials, respectively—have “a refractive index of approximately 1.46.” Hwang, 9:25–30. *Supra*, §VII.A.2.e (claim 8[d]). *See* Hwang, 8:40–52, 10:2–5.

4. Claim 10: “The device of claim 9, wherein at least one of the two second materials includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.”

Hwang teaches or suggests this limitation. Ex-1003, ¶102. Hwang’s *two second materials* 151 and 212a’—used in the backside and peripheral light trapping materials, respectively—are “formed of silicon oxide.” Hwang, 9:25–30. *Supra*, §VII.A.2.e (claim 8[d]). *See* Hwang, 8:40–52, 10:2–5.

5. **Claim 11: “The device of claim 9, wherein the at least one of the two second materials includes a member selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶103. Hwang’s *two second materials* 151 and 212a’—used in the backside and peripheral light trapping materials, respectively—are “formed of silicon [di]oxide.” Hwang, 9:25–30. *Supra*, §VII.A.2.e (claim 8[d]). *See* Hwang, 8:40–52, 10:2–5.

6. **Claim 12: “The device of claim 8, wherein the first material includes a material having a refractive index of greater than or equal to about 2.1.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶104. Hwang’s *first materials* 152 and 217a’—used in the backside and peripheral light trapping materials, respectively—have “a refractive index of approximately 4.” Hwang, 9:25–30. *Supra*, §VII.A.2.e (claim 8[d]). *See* Hwang, 8:40–52, 10:2–5.

7. **Claim 13: “The device of claim 12, wherein the first material includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and combinations thereof.”**

Hwang teaches or suggests this limitation. Ex-1003, ¶¶105–108. Hwang’s *first materials* 152 and 217a’—used in the backside and peripheral light trapping materials, respectively—are “formed of ... silicon.” Hwang, 9:25–30. *Supra*, §VII.A.2.e (claim 8[d]). *See* Hwang, 10:2–5.

This silicon is one of the claimed silicon types. Ex-1003, ¶¶105–108. First, POSITAs would understand that references to “silicon,” without modification, typically pertain to *single crystal silicon*. Ex-1003, ¶¶107.

Second, to the extent that Hwang’s disclosure of “silicon” may be ambiguous, this limitation is still obvious, because POSITAs would have had a limited number of types of silicon from which to choose, and in fact the group of materials specified in this claim encompasses all forms of silicon. Ex-1018 at 114 (“Silicon-films can be either amorphous, polycrystalline, or single-crystal...”); *see also id.* at 145; Ex-1003, ¶¶108.

8. Claim 14: “The device of claim 8, wherein the peripheral sidewall extends completely around the pixel periphery.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶109–110. Hwang’s “sidewall multi-layered reflection layer 220 [220a’ in Figure 6] encloses the side walls of the pixel semiconductor patterns 110a.” Hwang, 6:15–17. *Supra* §VII.A.2.b (claim 8[a]). Accordingly, as illustrated below, the *peripheral sidewall* where pixel 110a contacts sidewall reflection layer 220 [220a’ in Figure 6] *extends completely around the pixel periphery*.

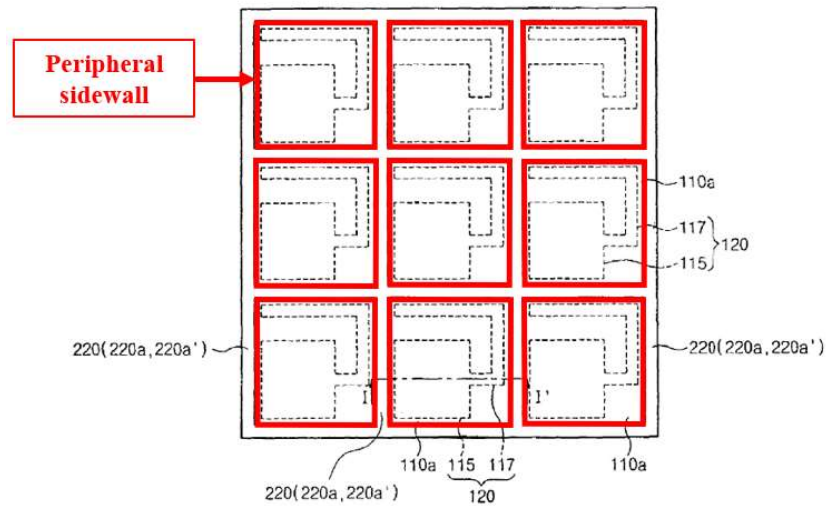


Fig. 1

Hwang, Fig. 1 (annotated); Ex-1003, ¶110.

9. **Claim 15:** “The device of claim 8, wherein the peripheral sidewall extends from the light incident surface to the backside surface.”

As illustrated below, the *peripheral sidewall* where pixel semiconductor pattern 110a contacts sidewall multi-layered reflection layer 220a' constitutes a peripheral sidewall that extends fully *from the light incident surface to the backside surface*.

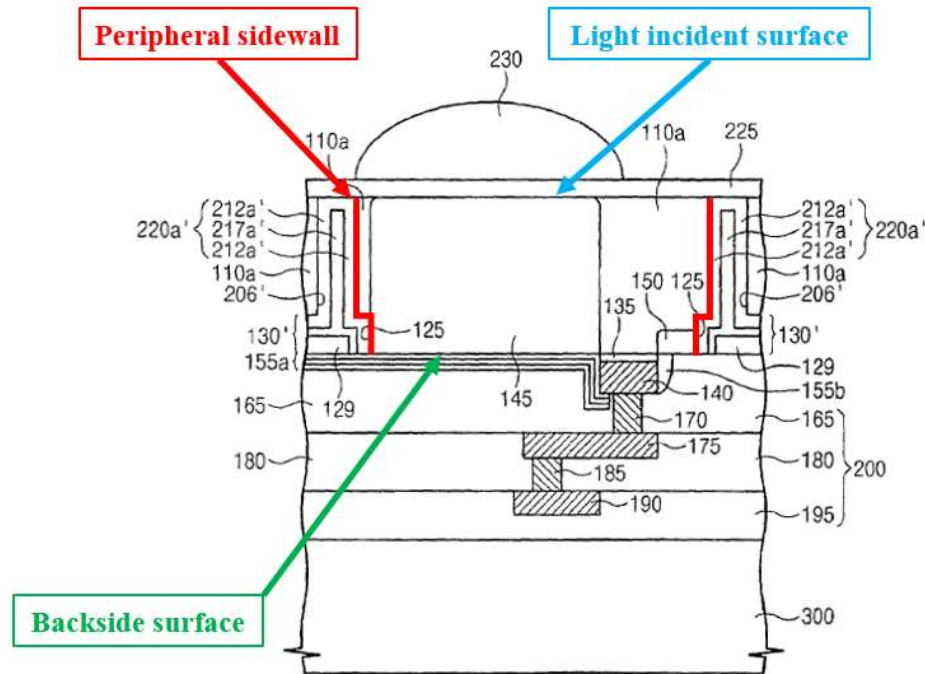


Fig. 6

Hwang, Fig. 6 (annotated); Ex-1003, ¶111; *supra*, §VII.A.2.b (claim 8[a]).

B. Ground 2: Claims 16–25 Are Obvious Based on Hwang and Konno.

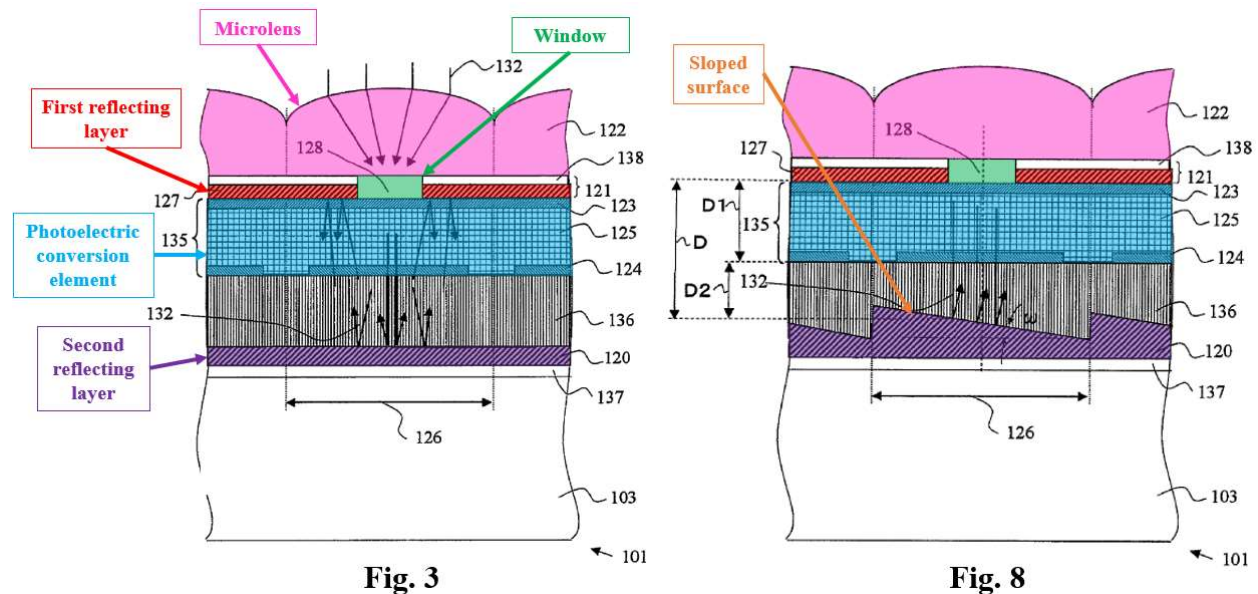
1. Overview of Konno

Konno is directed to a “solid-state imaging element”—i.e., an image sensor. Konno, Abstract. Like the ’764 patent, Konno concerns increasing image quality by using reflective surfaces to increase the amount of incident light absorbed by the photodiode. *See generally* Konno, 2:49–55.

As illustrated in Figure 3 below, Konno’s sensor includes first and second reflecting layers 121 and 120 that “sandwich the ... photoelectric conversion element 135,” *id.*, 8:22–25, thus “confining photons which entered into the solid-state imaging element [] between the both,” *id.*, 8:31–33, and improving sensitivity

by allowing for “most of the photons [to] be absorbed with the photoelectric conversion film 125,” *id.*, 10:8–13. Konno explains that “second reflection layer 120,” “can be formed by forming a thin film of a metal such as aluminum and silver.” *Id.*, 8:31–38.

Konno’s Figure 8 further includes a “reflecting surface of the second reflecting layer 120 [that] inclines”—i.e., a sloped surface. Konno, 15:35–40.



Konno, Figs. 3, 8 (annotated); Ex-1003, ¶¶112–113.

Konno’s sensor also includes “a transparent layer or layers disposed between the first electrode and first reflecting layer and/or between the second electrode and the second reflecting layer.” Konno, 3:16–19. Konno explains that “by providing a transparent layer in the solid-state imaging element of the present invention, convexes or concaves or a structure effective for reflecting or scattering photons can

be realized in the reflecting layer adjacent to the transparent layer.” *Id.*, 3:58–62. For example, Figure 7 below depicts an embodiment in which the transparent layer 136 is textured in order to scatter the incoming light.

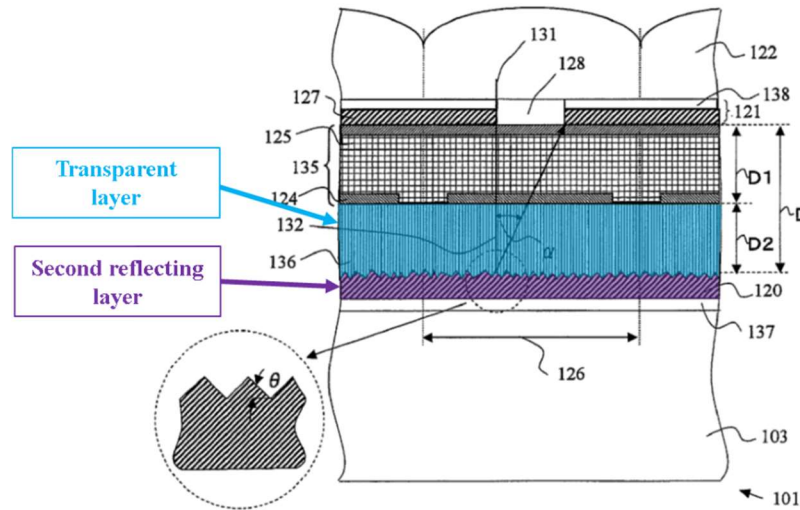


Fig.7

Konno, Fig. 7 (annotated); Ex-1003, ¶114.

Konno explains that the shape of the transparent and reflecting layers “makes it possible to reflect photons . . . and therefore the amount of photons to be detected again by the photoelectric conversion film 125 can be increased.” Konno, 13:66–14:3. Konno discloses that this structure “can be manufactured by, for example, forming concaves and convexes on the surface of the transparent layer 136 ... and then depositing a metal thereon to produce the reflecting layer 120.” *Id.*, 14:38–45.

2. Claim 17

a) Limitations 17[pre]–[c], [e]⁹

Limitations 17[pre]–[c] and 17[e] are identical to limitations 8[pre]–[c] and 8[f]. Hwang teaches or suggests these limitations for the reasons discussed in Sections VII.A.2.

b) 17[d]: “wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface”

This limitation is obvious based on Hwang in view of Konno. Ex-1003, ¶¶124–128.

In Konno’s Figure 8 embodiment, the solid-state imaging element includes a second reflecting layer 120 constituting a *backside light trapping material* that *has a sloped surface*. Ex-1003, ¶125. That is, Konno teaches that its “second reflecting layer 120” can have “incline[s],” as illustrated below. Konno, 15:36–38.

⁹ A listing of the challenged claims, including the labels for each limitation, is provided in the Claims Appendix at the end of this document.

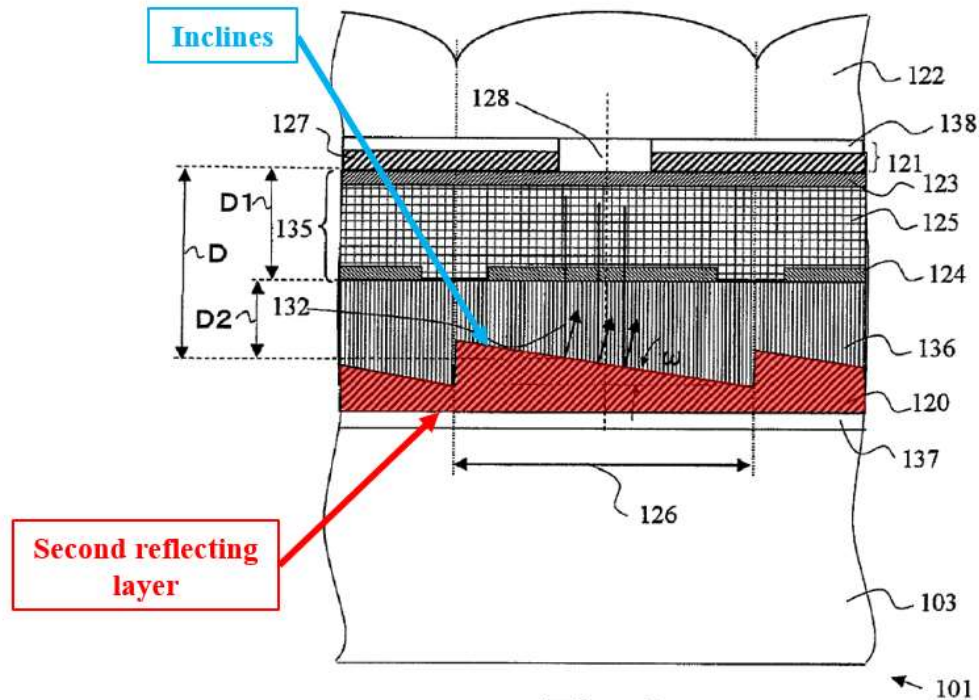


Fig. 8

Konno, Fig. 8 (annotated); Ex-1003, ¶125. Konno explains that “inclination of the reflecting surface is designed so that most of photons which entered at the end of the light entrance window 128 ... reach to the first reflecting layer 121” to increase sensitivity. Konno, 15:38–50.

Therefore, it would have been obvious to use Konno’s inclined surface in Hwang’s image sensor—i.e., forming Hwang’s base multi-layered reflection layer 155a with an inclined surface—to improve efficiency in a similar manner. Ex-1003, ¶¶126–127.

This modification would result in Hwang’s image sensor having a *backside light trapping material* (i.e., Hwang’s base multi-layered reflection layer 155a) *that has a sloped surface at the pixel device interface*. Ex-1003, ¶127.

POSITAs would have been motivated to make this modification, as such an inclined surface would redirect light to Hwang's sidewall multi-layer reflection layer 220a' to increase efficiency. Ex-1003, ¶128. Hwang discloses that "[l]ight that is reflected from the first and second boundary surfaces," i.e. light that reflects off of the base multi-layered reflection layer, "is also reflected by the third boundary surface and also the fourth boundary surface within the sidewall multi-layered reflection layer 220" and that, as a result, "the absorption efficiency of external light is increased." Hwang, 10:28–35; *see also* Hwang, 8:61–9:14. Thus, both Hwang and Konno teach that it is desirable to configure the image sensor so that light that reflects off of the backside light reflecting material also reflects off of the peripheral light reflecting material in order to increase the path of the light and maximize the absorption efficiency of the pixel. POSITAs would therefore be motivated to implement Konno's sloped surfaces in Hwang's image sensor in order to achieve this mutually recognized goal.

POSITAs would reasonably have expected success in implementing Konno's sloped surface, as, e.g., it could be implemented after the manufacturing step shown in Hwang's Figure 22 or between the manufacturing steps shown in Hwang's Figures 8/9 for a substantially similar embodiment. Ex-1003, ¶128.

3. Claim 21

a) Limitations 21[pre]–[c], [e]

Limitations 21[pre]–[c] and 21[e] are identical to limitations 8[pre]–[c] and 8[f]. Hwang teaches or suggests these limitations for the reasons discussed in Sections VII.A.2.

b) 21[d]: “a textured layer positioned to interact with light proximal to the backside surface”

This limitation is obvious based on Hwang in view of Konno. Ex-1003, ¶¶137–145.

In Konno’s Figure 7 embodiment, the transparent layer is textured by “forming concaves and convexes on the surface of the transparent layer 136.” Konno, 14:38–40. The textured surface “can be formed by a known technique such as sputtering and microlithography.” *Id.*, 14:43–45. Konno’s second reflective layer may then formed on the transparent layer by “depositing a metal” thereby forming concaves and convexes in the reflective layer. *Id.*, 14:38–43.

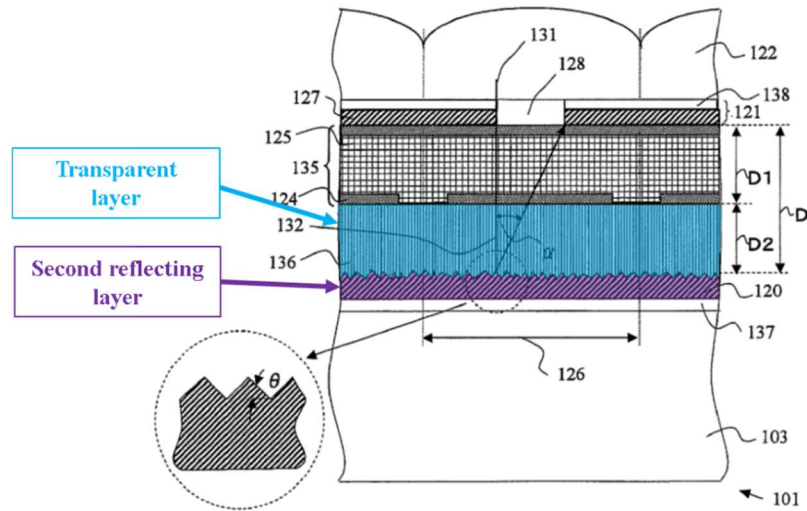


Fig. 7

Konno, Fig. 7 (annotated); Ex-1003, ¶138

Konno's transparent layer is *a textured layer positioned to interact with light proximal to the backside surface*. As shown in Figure 7, the transparent layer is formed on the backside surface of photoelectric conversion element 135. The texturing of the transparent layer, and the resulting shape of the second reflecting layer are constructed so that “[w]hen it reflects the incident photons 132, it can thereby reflect them with a large amount of horizontal components.” Konno, 13:63–66. In this way, “the amount of photons to be detected again by the photoelectric conversion film 125 can be increased,” thereby increasing the sensitivity of the device. *Id.*, 13:66–14:3; Ex-1003, ¶¶139–140. In particular, “[t]he photons not absorbed by the photoelectric conversion film 125 transmit the pixel electrode 124 and the transparent layer 136 and reach the second reflecting layer.” Konno, 9:64–67. By transmitting the photons not absorbed by the photoelectric conversion film,

the transparent layer is *positioned to interact with light proximal to the backside surface*.

It would have been obvious to use Konno's textured transparent layer in Hwang's image sensor to improve efficiency in a similar manner. Ex-1003, ¶141.

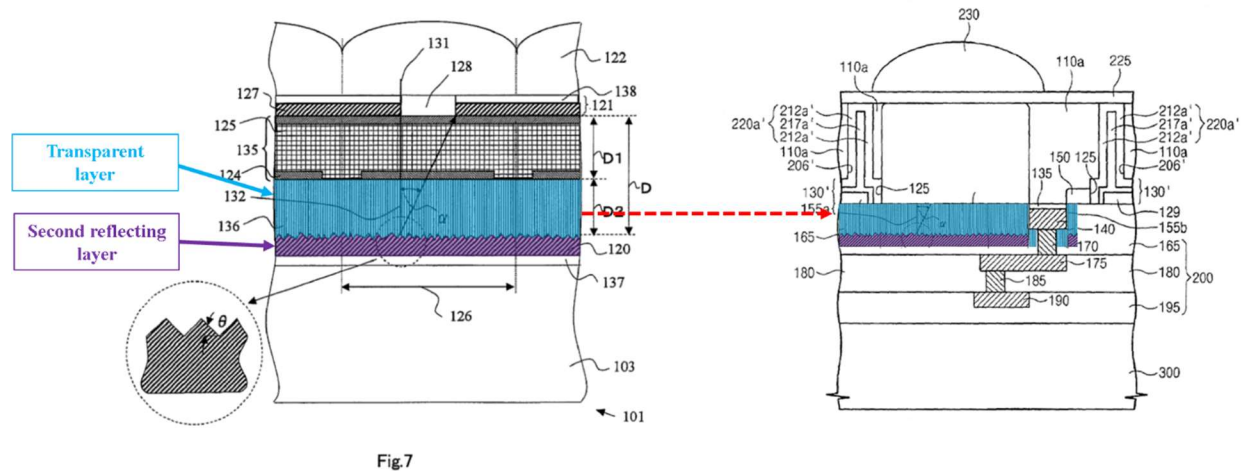


Fig.7

Konno, Fig. 7 (annotated); Hwang, Fig. 6 (annotated, modified; Ex-1003, ¶141. As shown above, this modification results in Hwang's image sensor having a *textured layer* (the transparent layer) *positioned to interact with light proximal to the backside surface*.

Additionally, this modification would still meet the requirement of a *backside light trapping material substantially covering the backside surface* as specified in limitation 21[b] (and 8[b]). That is, the modification would include a “second reflecting layer 120” as taught in Konno, which “can be formed by forming a thin film of a metal such as aluminum and silver by deposition or the like.” Konno, 8:31–

38. See Ex-1003, ¶141. This layer further would *substantially cover[] the backside surface* as illustrated above. See Ex-1003, ¶141.

POSITAs would have been motivated to make this modification, as such a textured layer would redirect light to Hwang's sidewall multi-layer reflection layer 220a' to increase efficiency. Ex-1003, ¶¶142–143. Hwang discloses that “[l]ight that is reflected from the first and second boundary surfaces,” i.e. light that reflects off of the base multi-layered reflection layer, “is also reflected by the third boundary surface and also the fourth boundary surface within the sidewall multi-layered reflection layer 220” and that, as a result, “the absorption efficiency of external light is increased.” Hwang, 10:28–35; *see also* Hwang, 8:61–9:14. Thus, both Hwang and Konno teach that it is desirable to configure the image sensor so that light that reflects off of the backside light reflecting material also reflects off of the peripheral light reflecting material in order to increase the path of the light and maximize the absorption efficiency of the pixel. POSITAs would therefore be motivated to implement Konno's sloped surfaces in Hwang's image sensor in order to achieve this mutually recognized goal.

POSITAs would reasonably have expected success in implementing Konno's textured layer. Konno teaches that the transparent layer “is formed from a material which transmits photons, for example glass and plastics such as acrylic resins.” Konno, 9:35–41. Hwang teaches that base multi-layered reflection layer 155a

comprises a layer of silicon dioxide (i.e. glass). POSITAs would understand that texturing Hwang's silicon dioxide layer using the methods described in Konno requires nothing more than the use of known techniques that would have yielded predictable results. Ex-1003, ¶¶144–145. The textured layer could be implemented after the manufacturing step shown in Hwang's Figure 22 or between the manufacturing steps shown in Hwang's figures 8/9 for a substantially similar embodiment. Ex-1003, ¶¶144–145.

4. Claims 16, 20, 25: “The device of claim [8, 17, 21], wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”

These limitations are obvious based on Hwang in view of Konno. Ex-1003, ¶¶115–119. 132, 150.

Hwang discloses a backside light trapping material comprising base multi-layered reflection layer 155*a*. *Supra*, §VII.A.2.c (claim 8[b]). However, POSITAs would have recognized that there were other known materials and material combinations to use in such backside light trapping materials, each of which having its own benefits and considerations. Ex-1003, ¶115. For example, Schubert, discusses “[d]ifferent types of reflectors” to use in optoelectronic devices, i.e., “a metallic reflector, distributed Bragg reflector (DBR), hybrid reflector, total internal reflector (TIR), and a triple-layer omni-directional reflector (ODR).” Schubert at 163.

As illustrated below, Konno's solid-state imaging element includes a second reflecting layer 120 constituting *a backside light trapping material that is a metal layer*. Ex-1003, ¶¶116–117. Konno explains that this layer 120, has “reflection parts consist[ing] of light reflective surfaces such as mirror surfaces ... formed ... of a metal such as aluminum and silver.” Konno, 8:31–38.

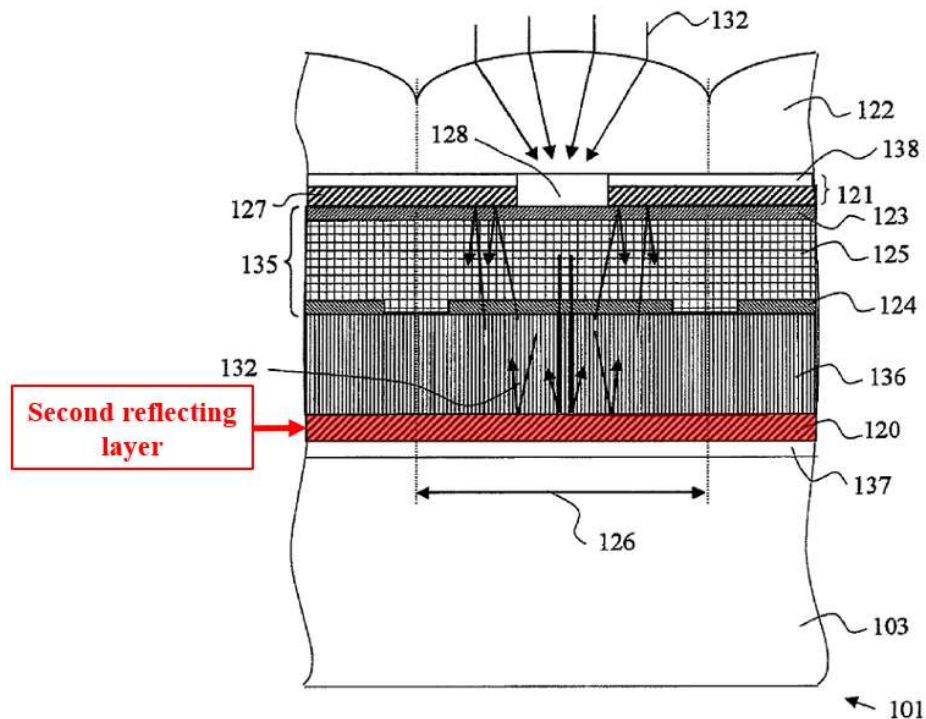


Fig. 3

Id., Fig. 3 (annotated); Ex-1003, ¶¶116–117.

As relevant to claim 20, which depends on claim 17 and therefore requires a “sloped surface,” Konno teaches that, in the embodiment of Figure 8, reflecting layer 120 differs only as to its shape and is therefore also a metal layer. Konno, 15:33–36; Ex-1003, ¶¶132.

As relevant to claim 25, which depends on claim 21 and therefore requires a “textured layer,” Konno teaches that, in the embodiment of Figure 7, reflecting layer 120 is again a metal layer. Konno, 14:38–45; Ex-1003, ¶¶150.

Konno explains that “when the reflecting layers 120 and 121 consist of metals, it is also possible to electrically connect at least one of these to ground or electrode potential of a read-out circuit, a control circuit, a power supply or the like.” Konno, 12:29–31. “By using such a [metal] structure, error signals and noises generated in output signals of the photodetector 101 by external noises ... can be thereby reduced.” Konno, 12:33–38.

Therefore, it would have been obvious to use Konno’s metal backside reflective layer in Hwang’s image sensor—i.e., substituting Konno’s metal reflector for Hwang’s base multi-layered reflection layer 155*a*. This modification would result in Hwang’s image sensor having a *backside light trapping material that is a metal layer*.¹⁰ Ex-1003, ¶¶117–118.

¹⁰ Even with this substitution, Hwang’s *peripheral light trapping material* would still include a *first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials*, which is sufficient for limitation 8[d]. *Supra*, §VII.A.2.e.

POSITAs would be motivated to use Konno's metal backside reflective layer in Hwang's image sensor to achieve these benefits, e.g., reducing error signals and noises generated by external noises. Ex-1003, ¶118.

POSITAs would reasonably have expected success in making such a modification, i.e., substituting Hwang's non-metallic reflector with Konno's metal reflector. For example, Konno's second reflecting layer 120 could be incorporated (alongside an intermediate insulating layer, such as transparent layer 136) between the manufacturing steps shown in Hwang's Figures 8 and 9. Ex-1003, ¶118. POSITAs would understand that the design of these layers could be tailored based on the use of a mask (e.g., Hwang's mask 160), followed by a subsequent etch. Ex-1003, ¶118.

5. Claims 18, 23

The additional limitations of claims 18 and 23 are identical to that of claim 14. Hwang teaches or suggests these limitations for the reasons discussed in Ground 1. *Supra*, §VII.A.8.

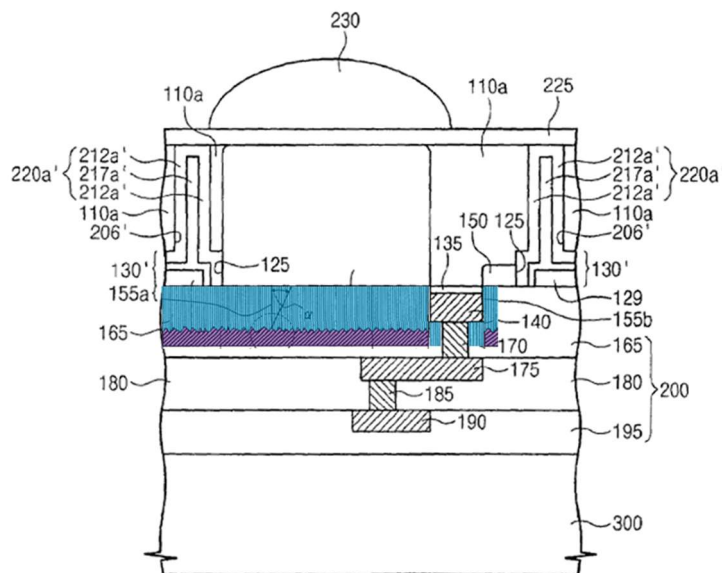
6. Claims 19, 24

The additional limitations of claims 19 and 24 are identical to that of claim 15. Hwang teaches or suggests these limitations for the reasons discussed in Ground 1. *Supra*, §VII.A.9.

7. Claim 22: “The device of claim 21, wherein the textured layer is located between the backside surface and the backside light trapping material.”

This claim is obvious based on Hwang in view of Konno. Ex-1003, ¶147.

As discussed with respect to limitation 21[d], above, it would have been obvious to modify Hwang to incorporate Konno’s textured region, as illustrated in the figure below.

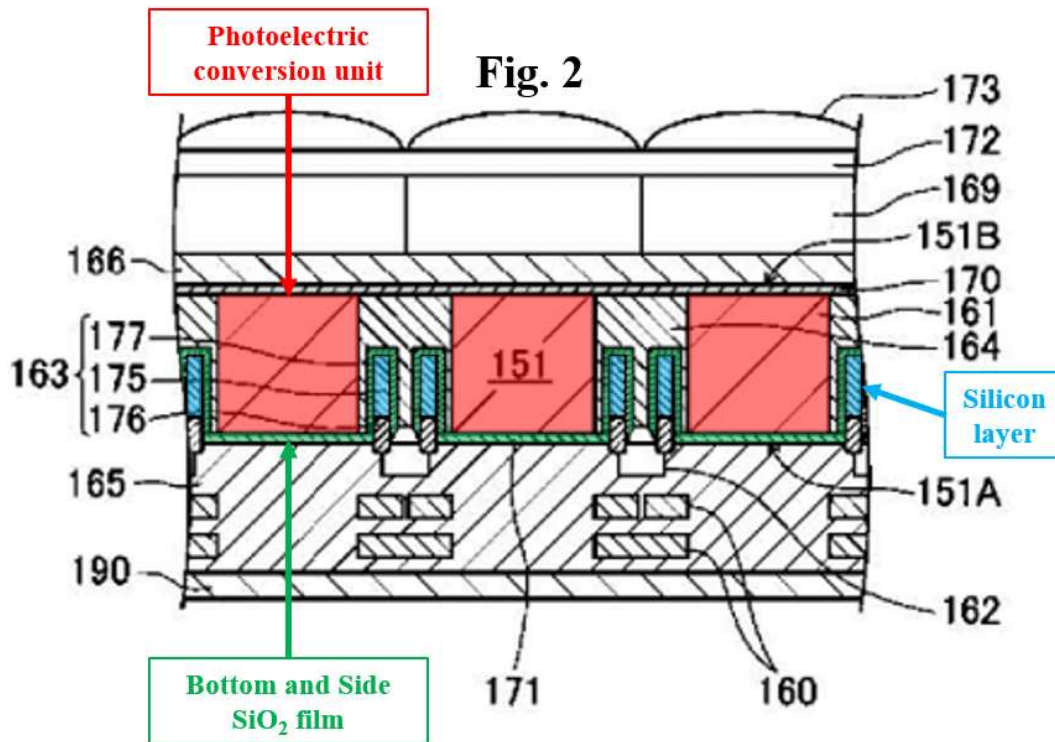


Hwang, Fig. 6 (annotated, modified; Ex-1003, ¶147. As shown, the textured layer (in blue) is located between the backside surface of the pixel and backside light trapping material (in purple).

C. Ground 3: Claims 1–5, 7 Are Obvious Based on Hwang and Mori.

1. Overview of Mori

Mori is directed to a “solid-state imaging device,” i.e., an image sensor, having pixels separated by a “partition part” comprising silicon and silicon oxide layers. Mori, [0012]–[0013]. An exemplary embodiment is depicted below.



Mori, Fig. 2 (annotated); Ex-1003, ¶151–153. Figure 2 depicts three “[p]hotoelectric conversion units 161,” (i.e., pixels), Mori, [0021], and a multi-layered “partition part 163,” *id.*, [0023], (having a “silicon layer 175,” *id.*, [0028] and a “side SiO₂ film 177,” *id.*, [0030]) to reduce “color mixing [or ‘crosstalk’] due to obliquely incident light,” *id.*, [0027].

Mori teaches that this multi-layer Si/SiO₂ partition solves a problem in conventional imaging devices which use partitions “made of a light-reflective material such as tungsten.” Mori, [0005]. As Mori explains:

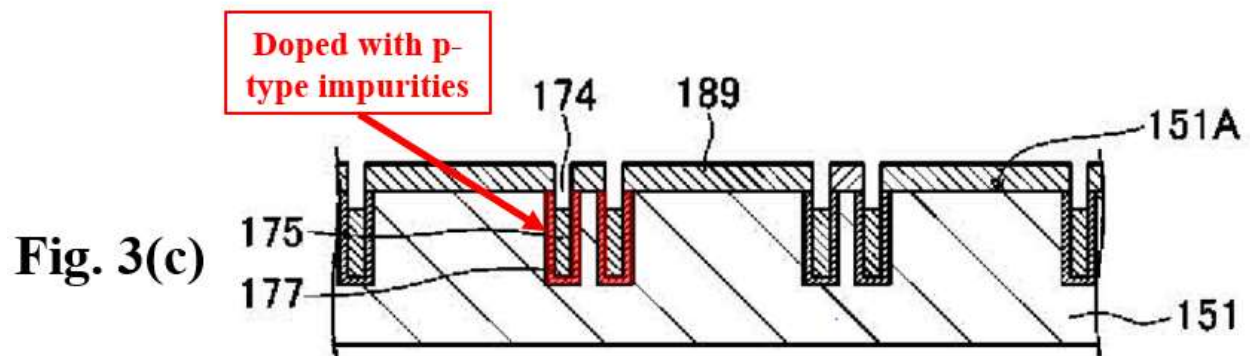
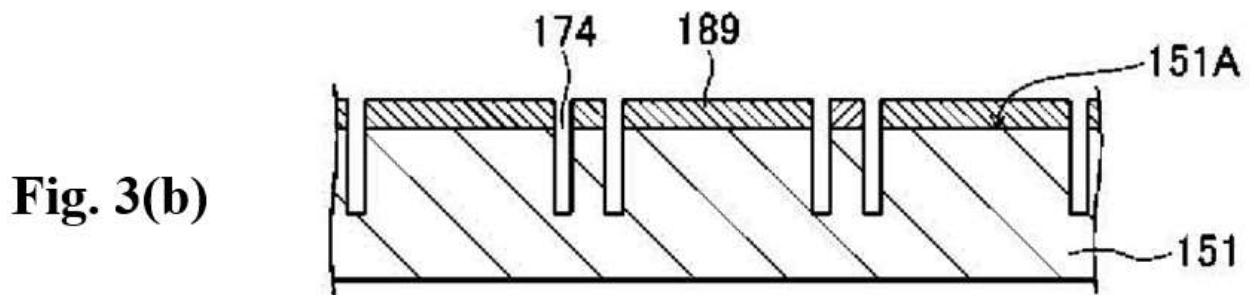
A single crystal epitaxial layer cannot easily be formed on the embedded member because metal and silicon have different lattice constants. ***Therefore, the silicon layer formed on the embedded member contains many crystal defects.*** As a result, the charge generated when dark increases, and the sensitivity of the solid-state imaging device decreases.

Mori, [0007]. That is, the crystal defects can cause what is known in the art as “dark current”—i.e., a “very small current when an electric charge (electron) [is] generated” when no light is incident on the photodiode (when the pixel should be “off”). Ex-1020, 1:25–28. Ex-1003, ¶154.

Mori therefore uses a Si/SiO₂ partition part, to reduce “crystal defects on the side surface of the groove for forming the partition part” and “charges generated when dark ... to achieve high sensitivity.” Mori, [0013].

Mori also discloses doping the SiO₂ film layer to further mitigate dark current stemming from crystal defects. Ex-1003, ¶¶155–156. As illustrated below, first, the side SiO₂ film 177 is “formed on the side surface of [a] partition groove 174.” Mori, [0036]. Next, “[i]n order to prevent charges generated when dark due to crystal defects in the partition groove 174 from flowing into the photoelectric conversion

unit 161, p-type impurities are preferably injected into the side walls of partition groove 174 after forming the side SiO₂ film 177.” Mori, [0036]. That is, the SiO₂ film 177 on the side walls is doped with p-type impurities, resulting in an excess of positively charged carriers (or “holes”). Ex-1003, ¶156. “Subsequently, a silicon layer 175 is formed in the partition groove 174,” to complete formation of the Si/SiO₂ partition. Mori, [0036].



Mori, Figs. 3(b)-(c) (annotated); Ex-1003, ¶¶156.

2. Claim 1

a) Limitations 1[pre]–[c], [f]

Limitations 1[pre]–[c] and 1[f] are identical to limitations 8[pre]–[c] and 8[f].

Hwang teaches or suggests these limitations for the reasons discussed in Ground 1.

Supra, §VII.C.1.

b) 1[d]: “wherein at least one of the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials”

Although the language of limitation 1[d] differs slightly from that of limitation 8[d], those differences do not alter the analysis. The same disclosures in Hwang that teach or suggest limitation 8[d] also teach or suggest limitation 1[d]. Ex-1003, ¶¶161–166. Claim 8 recites “a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials.” The “high refractive index material” of claim 1 thus corresponds to the “first material” of claim 8. The “two low refractive index materials” of claim 1 correspond to the “two second materials” of claim 8.

With respect to Hwang’s *backside light trapping material*, the second base multi-layered reflection layer 152 (formed of silicon with a refractive index of approximately 4) is both the *first material* of claim 8 and the *high refractive index material* of claim 1. The first base multi-layered reflection layer 151 (formed of silicon dioxide with a refractive index of approximately 1.46) is both the *second*

material of claim 8 and the *low refractive index material* of claim 1.¹¹ Ex-1003, ¶¶163–164.

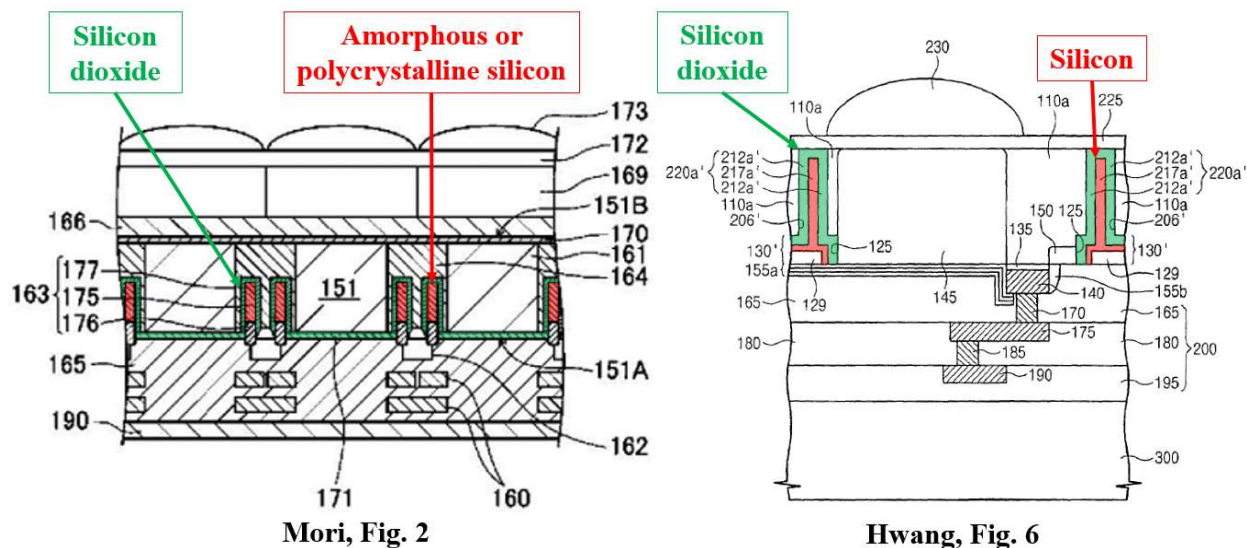
With respect to Hwang’s *peripheral light trapping material*, the second sidewall reflection layer 217a’ (formed of silicon with a refractive index of approximately 4) is both the *first material* of claim 8 and the *high refractive index material* of claim 1. The first sidewall reflection layer 212a’ (formed of silicon dioxide with a refractive index of approximately 1.46) is both the *second material* of claim 8 and the *low refractive index material* of claim 1. Ex-1003, ¶¶165–166

- c) **1[e]: “wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field”**

This limitation is obvious based on Hwang in view of Mori. Ex-1003, ¶¶167–174.

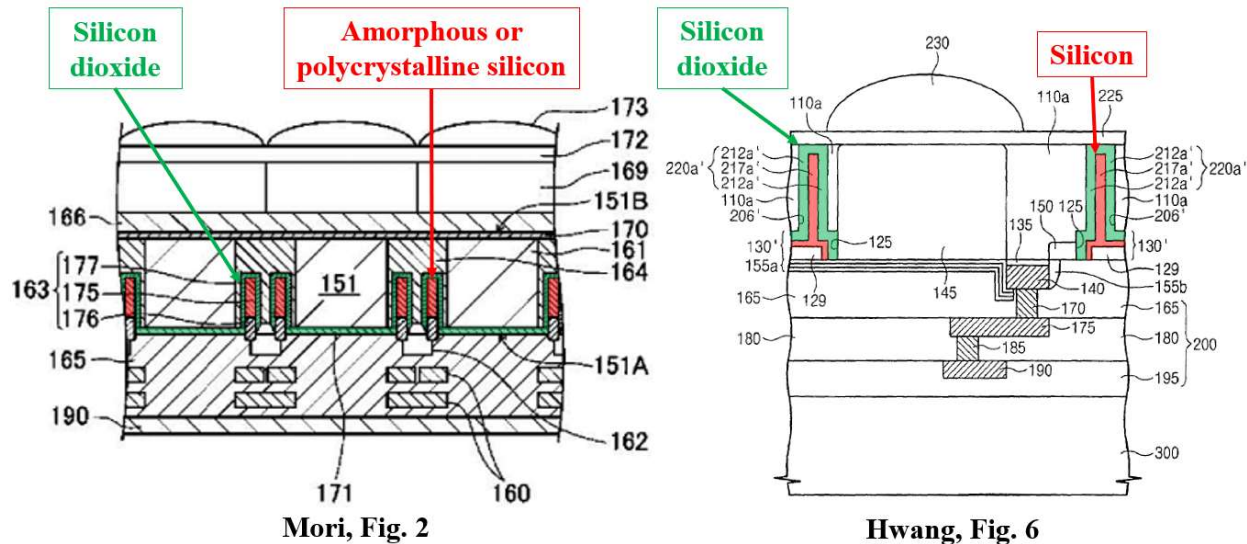
¹¹ In the Related Proceeding, Petitioner proposed to construe *low refractive index material(s)* to mean “material(s) that have a refractive index less than 2.1,” while Patent Owner proposed that it also may encompass “[m]aterial that has ... a refractive index that is at least 0.2 less than the high refractive index material.” Ex-1017 at 3 (cleaned up). Hwang’s first base multi-layered reflection layer 151 is a *low refractive index material* under either construction.

Both Mori and Hwang disclose image sensors including multi-layer Si/SiO₂ films to mitigate against interference between pixels. As illustrated below, both references utilize similar Si/SiO₂ films disposed at the pixel sidewalls Hwang's image sensor includes a peripheral multi-layer reflection layer (layer 220a') disposed along the pixel sidewall and comprising a silicon layer (layer 217a') sandwiched between silicon dioxide layers (layer 212a'). *Supra*, §VII.A.2.e (claim 8[d]). Mori similarly discloses a multi-layer partition (layer 163) disposed between adjacent pixels and comprising a silicon layer (layer 175) sandwiched between silicon dioxide layers (layer 177).



Mori, Fig. 2 (annotated); Hwang, Fig. 6 (annotated); Ex-1003, ¶168. *See also* Mori, Fig. 6 (depicting partition part 163 spanning along the entire side of photoelectric conversion unit 161). And in both references, the Si/SiO₂ film mitigates interference between pixels. *Cf.* Hwang, 15:46—48 (“interference between pixels can be

minimized by the sidewall multi-layered reflection layer”) with Mori, ¶[0027] (Si/SiO₂ partition serves to reduce “color mixing [or ‘crosstalk’] due to obliquely incident light”).



Mori, Fig. 2 (annotated); Hwang, Fig. 6 (annotated); Ex-1003, ¶168.

Mori teaches that “[i]n order to prevent charges generated when dark due to crystal defects ... p-type impurities are preferably injected into the side walls of partition groove 174 after forming the side SiO₂ film 177.” Mori, ¶[0036]. *Supra*, §VII.C.1 (Mori Overview).

Accordingly, Mori teaches that its side SiO₂ film *is doped with a dopant to create a surface field* as set forth in this limitation. Ex-1003, ¶170. The ’764 patent does not explain how doping the low refractive index material operates to create a surface field. Ex-1003, ¶170–71. Rather, its only disclosure relating to such doping is that:

[I]t can also be beneficial to dope the sidewalls to create a surface field that will improve electrical isolation between the pixels. In one aspect, it can also be beneficial to dope the low refractive index material of the Bragg-type reflectors to increase such electrical isolation.

'764 patent, 9:60–65. That is, the '764 patent teaches that doping in such a manner as in Mori serves to increase electrical isolation between the pixels via a surface field. Ex-1003, ¶170. Thus, Mori's doped SiO₂ film 177 along the side of its pixel (photoelectric conversion unit 161) would constitute a *low refractive index material doped with a dopant to create a surface field* to the extent that is contemplated by the limited disclosure of the '764 patent. Ex-1003, ¶170–71.

Based on Mori's teaching, it would have been obvious to similarly dope Hwang's silicon oxide layers 212a'—such that this *low refractive index material* (Hwang's silicon oxide layers) *is doped with a dopant to create a surface field* in the same manner as Mori's SiO₂ film. Ex-1003, ¶172. Hwang's silicon oxide layer 212a' adjoins the side of Hwang's pixel (pixel semiconductor pattern 110a), just like Mori's side SiO₂ film 177 adjoins Mori's pixel. Ex-1003, ¶172. Accordingly, POSITAs would have recognized that doping Hwang's silicon oxide layer 212a' with p-type impurities would similarly mitigate dark current stemming from crystal defects in Hwang's sensor. Ex-1003, ¶172.

POSITAs would reasonably expect success in making this modification, given that Hwang and Mori have the same arrangement of a silicon/silicon oxide film

disposed at the sidewall between pixels. Ex-1003, ¶173. Moreover, this doping could be readily implemented in Hwang’s sensor, e.g., in the manufacturing steps shown in Hwang’s figures 20/21 after applying layer 212a’ in grooves 206’. Ex-1003, ¶173.

3. Claim 2: “The device of claim 1, wherein the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶176–177. Limitation 1[d] requires that *at least one of the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials*. But as explained for Limitation 1[d] above in Section VII.C.2.b, Hwang’s *backside light trapping material* and *peripheral light trapping material* both have this structure. Thus, this limitation of claim 2 is satisfied for the reasons explained in that section above.

4. Claim 3: “The device of claim 1, wherein the dopant is boron or antimony.”

This limitation is obvious based on Hwang in view of Mori. Ex-1003, ¶¶178–180.

It would have been obvious in view of Mori to dope the Hwang’s silicon oxide layer (the *low refractive index material*) with p-type impurities—i.e., a p-type dopant. *Supra*, §VII.C.2.c (claim 1[e]). Ex-1003, ¶¶167–174, 179. It further would be obvious to use boron as the p-type dopant, as boron is one of the most commonly

used p-type dopants for Si-based systems. Ex-1003, ¶179. *E.g.*, Ex-1018 at 27–28 (explaining silicon is commonly doped with Column-III-dopants (e.g., boron)). POSITAs would recognize that using boron as a p-type dopant for silicon-based systems is a known technique that would have yielded predictable results, particularly in light of boron’s similar use as a p-type dopant in other similar light trapping devices. Ex-1003, ¶179. *E.g.*, Ex-1019, ¶[0011] (“silicon substrate doped with a P-type dopant such as boron”). Additionally, using boron would have been obvious to try, as POSITAs would have had a limited number of types of p-type dopants from which to choose. Ex-1003, ¶179.

5. Claims 4, 5

The additional limitations of claims 4 and 5 are identical to the additional limitations of claim 14 and 15. Hwang teaches or suggests these limitations for the reasons discussed in Ground 1. *Supra*, §§VII.A.8–9.

6. Claim 7: “An array of light trapping pixel devices of claim 1.”

Hwang teaches or suggests this limitation. Ex-1003, ¶¶183–184.

Hwang teaches “a plurality of pixel semiconductor patterns 110a,” that are “arranged two-dimensionally in rows and columns,” Hwang 5:52–59, as shown in Figure 1, below. Hwang’s two-dimensional arrangement of pixels is *an array of light trapping pixel devices*, each of which meet the requirements of claim 1 for the reasons discussed for claim 1 above.

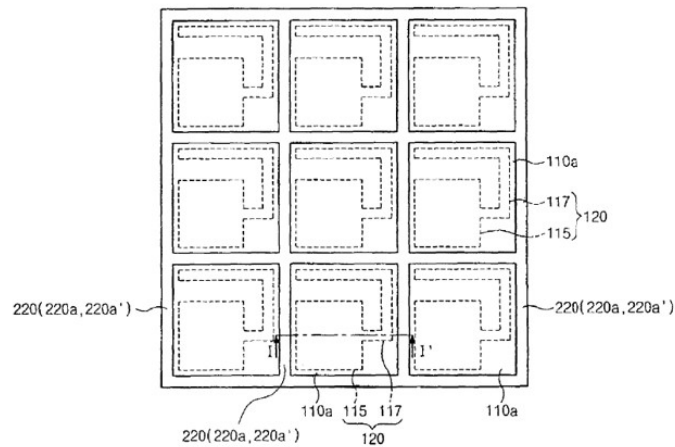


Fig. 1

Hwang, Fig. 1. Ex-1003, ¶184.

D. Ground 4: Claim 6 Are Obvious Based on Hwang, Mori, and Konno

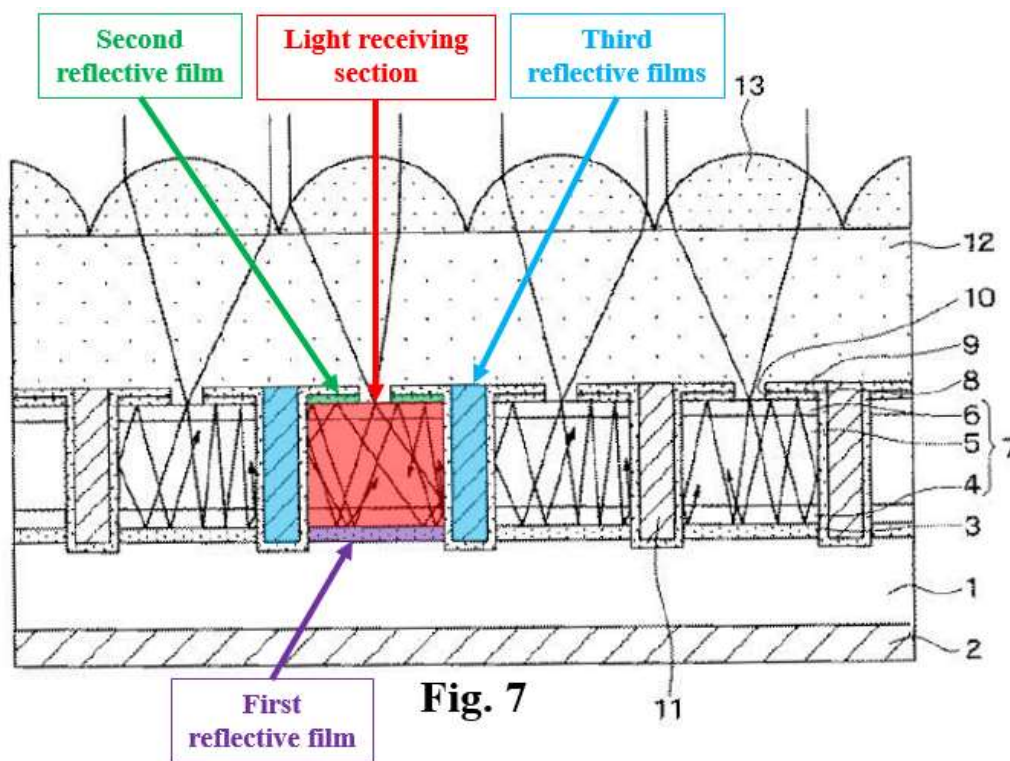
- 1. Claim 6: “The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”**

This claim is obvious based on Hwang in view of Mori and Konno. The additional limitation of claim 6 is identical to that of claim 16. As discussed in Section VII.B.4, POSITAs would be motivated to use Konno’s metal backside reflective layer in Hwang’s image sensor to achieve the benefits, for example, reducing error signals and noises generated by external noises and would have had a reasonable expectation of success in substituting Hwang’s non-metallic reflector with Konno’s metal reflector. Ex-1003, ¶185.

E. Ground 5: Claims 8, 12, 14–16 Are Obvious Based on Yamada

1. Overview of Yamada

Yamada is directed to an image sensor, i.e., a “light receiving element,” that uses “reflective films” to confine light within a light receiving section (e.g., PIN photodiodes), which “improves the sensitivity” and prevents “optical crosstalk ... between neighboring PIN photodiodes.” Yamada, ¶¶[0036]–[0038]. An exemplary embodiment is depicted below.



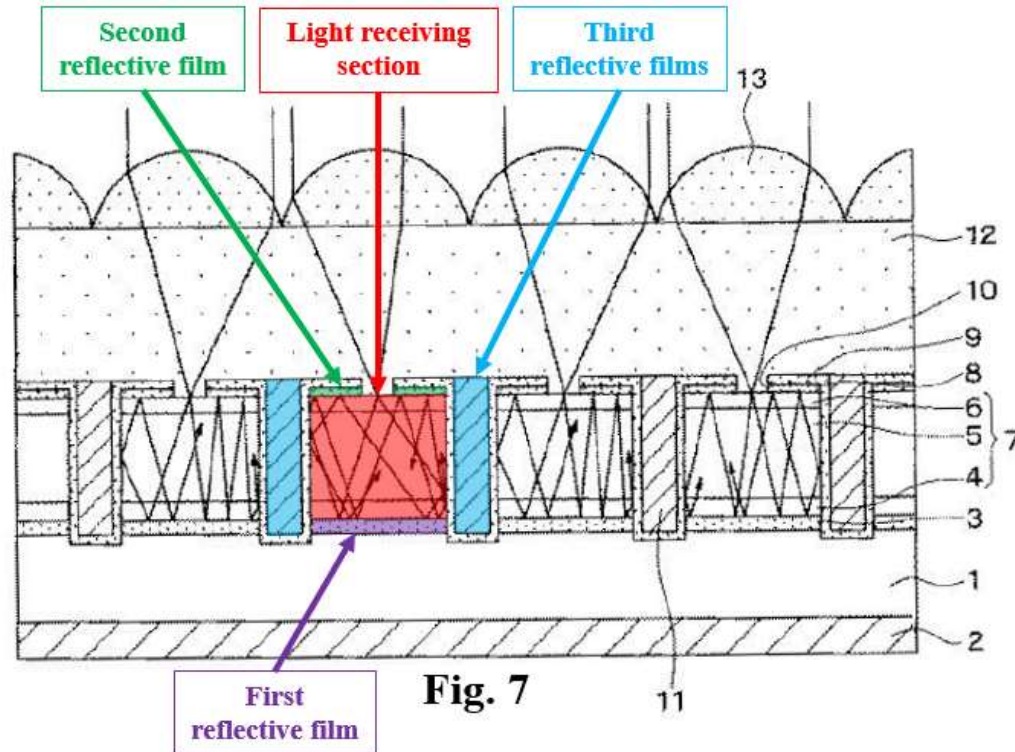
Id., Fig. 7 (annotated); Ex-1003, ¶¶186–190.¹²

2. Claim 8

a) 8[pre]: “A light trapping device, comprising”

To the extent the preamble is limiting, Yamada teaches or suggests it. Ex-1003, ¶¶191–194. As illustrated below, Yamada discloses a “light receiving element provided with a plurality of light receiving sections (7),” Yamada, ¶[0009], “composed of a PIN photodiode[s],” *id.*, ¶[0004], which convert “light energy ... into electrical energy,” *id.*, ¶[0035].

¹² Figure 7 (Yamada’s fifth embodiment) “share[s] the third reflecting film 11 between neighboring light receiving sections in contrast to the first embodiment,” but otherwise is “the same as ... the first embodiment.” Yamada, ¶¶[0049]–[0050]. Ex-1003, ¶188.

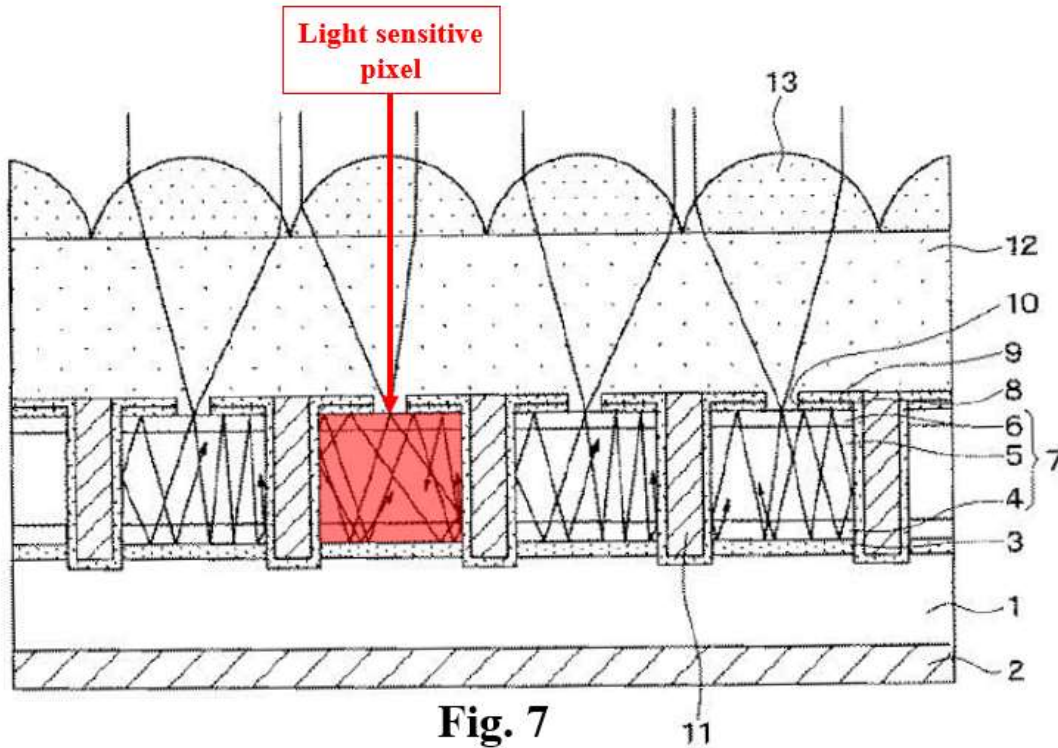


Id., Fig. 7 (annotated); Ex-1003, ¶192.

This device includes a “first reflective film (3)” “second reflective film (8)” and “third reflective films (11)” surrounding each the light receiving section such that light “[is] confined within the light receiving section 7,” Yamada, ¶[0010]—i.e., for *trapping light* by reflecting light back into the pixel. Ex-1003, ¶193.

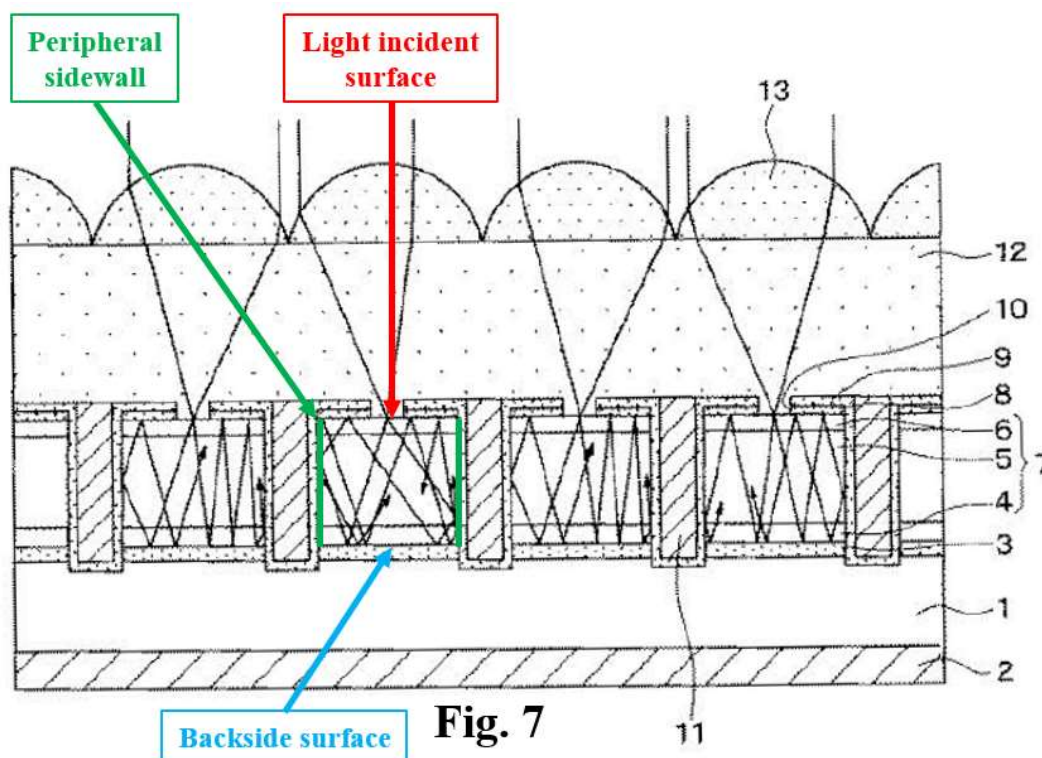
- b) 8[a]: “at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery”

Yamada’s light receiving element comprises *at least one light sensitive pixel*, as it is “provided with a plurality of light receiving sections (7),” as depicted below. Yamada, ¶[0009].



Id., Fig. 7 (annotated); Ex-1003, ¶¶195–201. “The light receiving section (7) can be composed of a PIN photodiode,” Yamada, ¶[0016], which converts “light energy ... into electrical energy,” *id.*, ¶[0035].

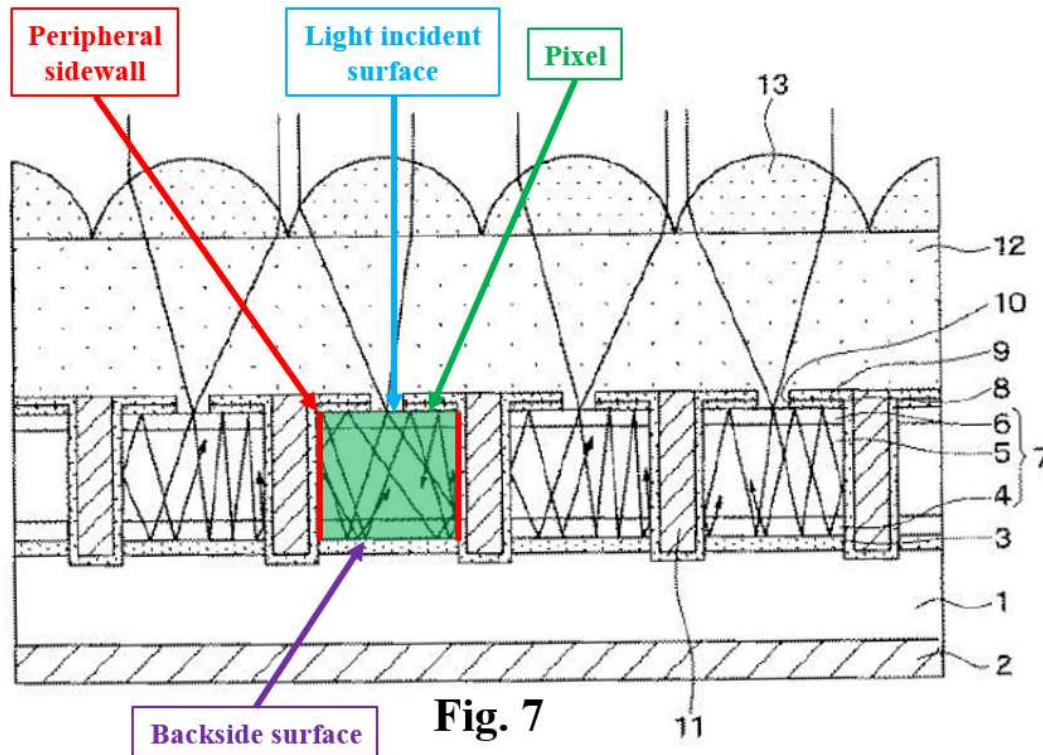
Each pixel (7) has a *light incident surface*, a *backside surface opposite the light incident surface*, and a *peripheral sidewall*, as illustrated below.



Id., Fig. 7 (annotated); Ex-1003, ¶197. As Yamada explains, each pixel has (i) “a first reflective film (3) arranged at a bottom surface”; (ii) “a second reflective film (8) arranged opposing the first reflective film (3) at a front surface”; and (iii) “third reflective films (11) arranged at side surfaces.” Yamada, ¶[0009].

The “front surface” constitutes a *light incident surface*, as “light [that] is incident from the front surface ... is converted into electrical energy” *Id.*, ¶[0004]; Ex-1003, ¶198. The “bottom surface” is “opposing the ... front surface” and thus constitutes a *backside surface opposite the light incident surface*. Ex-1003, ¶198. The “side surfaces” constitute *peripheral sidewalls*, as they are on the sides of the light receiving element. Ex-1003, ¶198.

These peripheral sidewalls are *disposed into at least a portion of the pixel*. As shown below, they run from the pixel's light incident surface to the backside surface—just like peripheral sidewalls 424 of the '764 patent. See '764 patent, Fig. 4, 10:58–64.

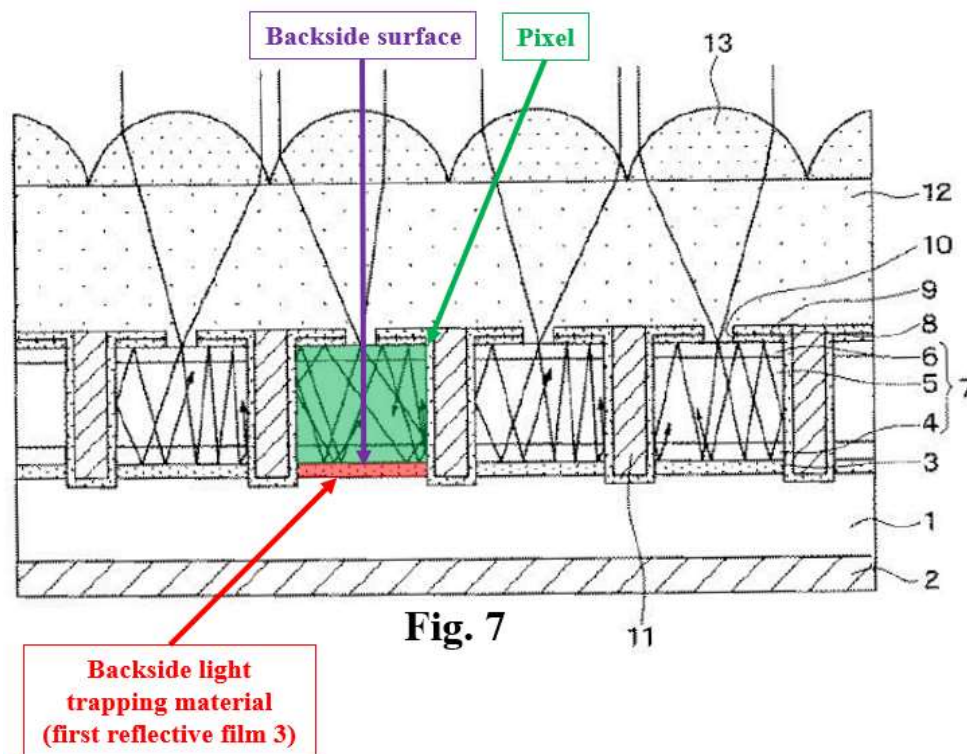


Yamada, Fig. 7 (annotated); Ex-1003, ¶199.

The peripheral sidewalls further *extend at least substantially around the pixel periphery*. Ex-1003, ¶200. Yamada discloses that “the entire side surfaces of the PIN photodiode 7 is covered by the third reflective films 11,” Yamada, ¶[0056], such that “the PIN photodiode 7 is surrounded by the ... third reflective film 11.” *Id.*, ¶[0036].

c) **8[b]: “a backside light trapping material substantially covering the backside surface”**

Yamada’s light receiving element includes a *backside light trapping material substantially covering the backside surface* of the pixel. Ex-1003, ¶¶202–206. As illustrated below, Yamada’s “first reflective film (3) [is] arranged at a bottom surface [*backside surface*] of the light receiving section (7),” Yamada, ¶[0009].



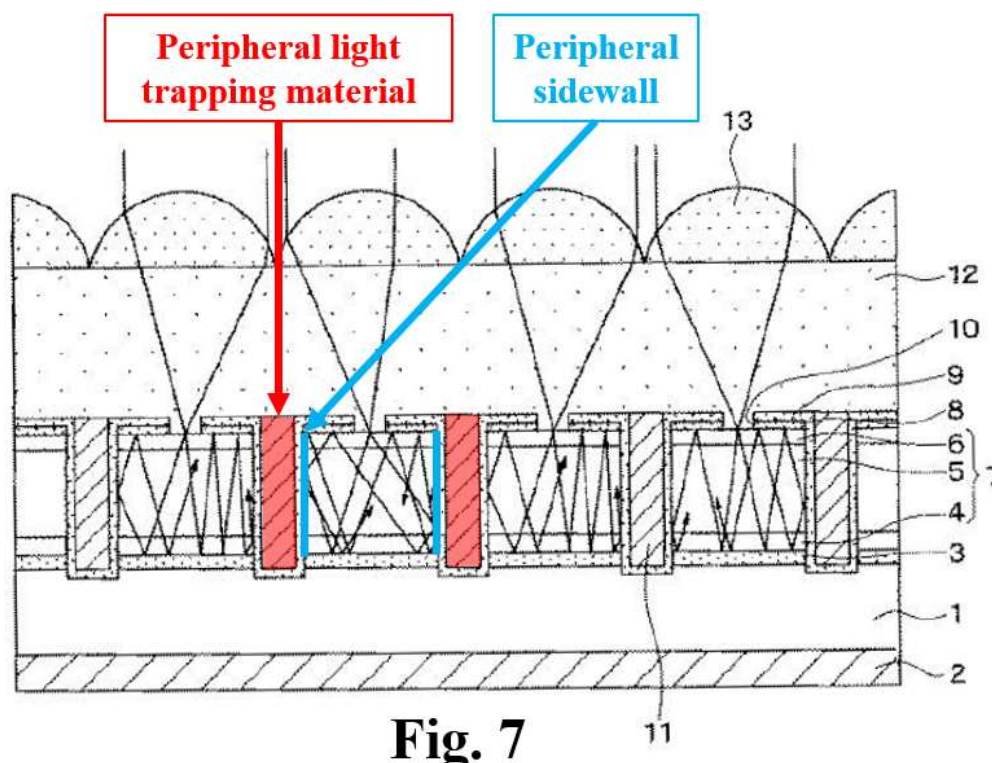
Id., Fig. 7 (annotated); Ex-1003, ¶203.

This layer traps light, as “light that enters the light receiving section (7) is reflected by the first reflective film (3) ... so as to be confined within the light receiving section (7).” Yamada, ¶[0010]; *see also id.*, ¶[0022] (“first reflective film 3” has “a high reflectance of at least 99 percent”); Ex-1003, ¶204.

Figure 7 above shows that Yamada's first reflective film *substantially covers*—if not completely covers—*the backside surface*. Yamada further discloses that “the PIN photodiode 7 is surrounded by the first reflective film 3, the second reflective film 8, and the third reflective films “ so that any light incident on the PIN photodiode is “confined within the PIN photodiode.” Yamada thus teaches that the first reflective film *substantially covers the backside surface* in order to confine the light and prevent it from leaking out of the photodiode. Ex-1003, ¶205.

d) 8[c]: “a peripheral light trapping material substantially covering the peripheral sidewall”

Yamada's light receiving element includes *a peripheral light trapping material substantially covering the peripheral sidewall*. Ex-1003, ¶¶207–211. As illustrated below, Yamada's “third reflective films (11) [are] arranged at side surfaces of the light receiving section (7).” Yamada, ¶[0009].



Id., Fig. 7 (annotated); Ex-1003, ¶208. Yamada discloses that the third reflective films 11 *substantially cover[] the peripheral sidewall*: “[S]ince the sides of PIN photodiode 7 are covered with the third reflective films 11, no incident light escapes from the sides of the PIN photodiode 7 and no optical crosstalk occurs between neighboring PIN photodiodes 7.” *Id.*, ¶[0038]; Ex-1003, ¶210.¹³

¹³ To the extent this element could arguably be interpreted to require that the peripheral light trapping material directly contact the peripheral sidewall, Yamada still satisfies it, as Yamada’s third reflective film 11 and first insulating film 9 would collectively constitute *a peripheral light trapping material* directly contacting and covering the *peripheral sidewall*. Ex-1003, ¶210.

This layer traps light, as “light that enters the light receiving section (7) is reflected by ... the third reflective films (11) so as to be confined within the light receiving section 7....” Yamada, ¶[0010]; Ex-1003, ¶209.

- e) **8[d]: “wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials”**

Yamada teaches or suggests this limitation. Ex-1003, ¶¶212–217.

Yamada’s *backside light trapping material* (first reflective film 3) *includes a first material sandwiched between two second materials*. Ex-1003, ¶213–215.

Yamada’s “first reflective film 3 is composed of,” e.g., “an $\text{Al}_x\text{Ga}_{1-x}\text{P}$ semiconductor multilayer film” where “[t]he composition ratio of X of $\text{Al}_x\text{Ga}_{1-x}\text{P}$ is changed” such that “the semiconductor multilayer film is composed by alternating layers of semiconductor films with a low refractive index and a high refractive index.”

Yamada, ¶[0021]. For example, choosing a ratio of 0 results in a *first material* of GaP (gallium phosphide, having a refractive index of 3.5 at 500nm. Schubert, Table 10.1). Ex-1003, ¶214–215. Choosing a ratio of 1 results in a *second material* of AlP (aluminum phosphide, having a refractive index of “ 2.75 ± 0.1 at 2.8eV,” Ex-1021, 153 or “about 2.8,” at 530nm, Ex-1022, 5:11–12). Ex-1003, ¶214–215.

POSITAs would recognize that Yamada’s alternating layers of low and high refractive index materials constitute (or at a minimum, strongly suggest) a

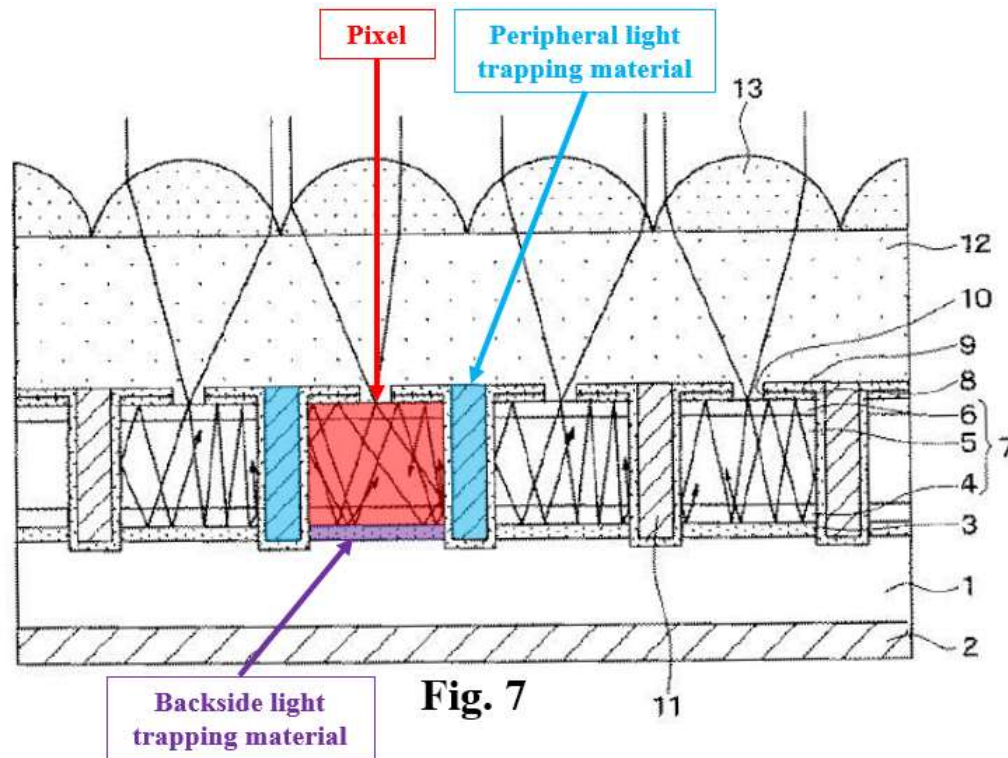
distributed Bragg reflector (“DBR”), i.e., a “multi-layer reflector consisting of typically 5–50 pairs of two materials with different refractive indices.” Schubert, 171. Ex-1003, ¶216. Such a reflector would have at least one layer of the *first material* (gallium phosphide) *sandwiched between two second materials* (aluminum phosphide). Ex-1003, ¶216. Additionally, *the first material has a higher refractive index* (about 3.5) *as compared to the two second materials* (above 2.8).

f) 8[e]: “wherein the difference in refractive index between the first material and the two second materials is at least 0.2”

Yamada teaches or suggests this limitation. Ex-1003, ¶218. As discussed in the previous section, the refractive index of the first material (gallium phosphide) is about 3.5. The refractive index of the second material (aluminum phosphide) is about 2.8. The difference is at least 0.2. *Id.*

g) 8[f]: “wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel”

Yamada discloses that *light contacting both the backside light trapping material [and] the peripheral light trapping material is reflected back towards the pixel*. Ex-1003, ¶¶219–221. That is, as illustrated by the arrows depicted below, “light that enters the light receiving section (7) is reflected by the first light reflective film (3) ... and the third reflective films (11) so as to be confined within the light receiving section 7.” Yamada, ¶[0010].



Id., Fig. 7 (annotated); Ex-1003, ¶220.

3. **Claim 12:** “The device of claim 8, wherein the first material includes a material having a refractive index of greater than or equal to about 2.1.”

Yamada teaches or suggests this limitation. Ex-1003, ¶222. Yamada’s *first material* in its first reflective film 3 (the *backside light trapping material*) may be formed of gallium phosphide, which has a refractive index of approximately 3.5. *Supra*, §VII.E.2.e (claim 8[d]).

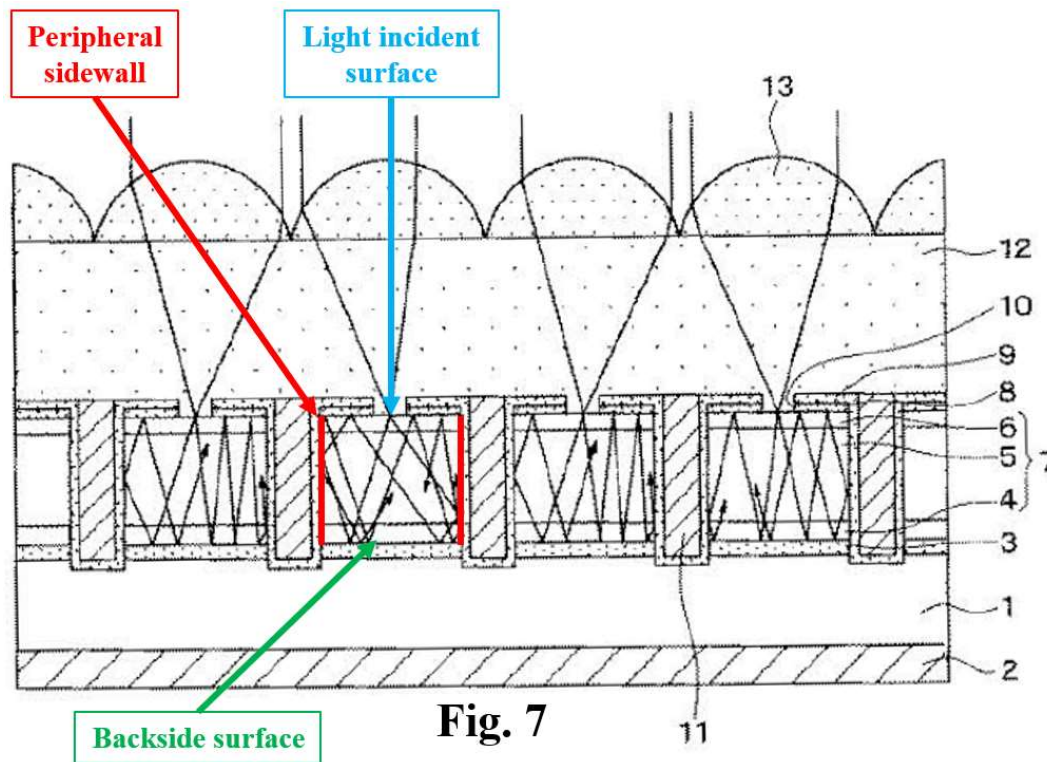
4. **Claim 14:** “The device of claim 8, wherein the peripheral sidewall extends completely around the pixel periphery.”

Yamada teaches or suggests this limitation. Ex-1003, ¶223. Yamada discloses that “the entire side surfaces of the PIN photodiode 7 is covered by the third

reflective films 11,” Yamada, ¶[0056], and that “the PIN photodiode 7 is surrounded by the ... third reflective film 11, so when light is incident to the PIN photodiode 7, that light is ... confined within the PIN photodiode 7,” *id.*, ¶[0036]. *Supra*, §§VII.E.2.b,d (claims 8[a,c]).

5. Claim 15: “The device of claim 8, wherein the peripheral sidewall extends from the light incident surface to the backside surface.”

Yamada teaches or suggests this limitation. Ex-1003, ¶224. As depicted below, Yamada’s peripheral sidewall extends fully *from the light incident surface to the backside surface*, allowing for light to be “to be confined within the PIN photodiode 7.” Yamada, ¶[0036]. *Supra*, §§VII.E.2.b,d (claims 8[a,c]).



Yamada, Fig. 7 (annotated); Ex-1003, ¶224. *See also* Yamada, ¶[0056].

6. Claim 16: “The device of claim 8, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”

Yamada’s third reflective films 11 constitute a *peripheral light trapping material* (*supra*, §VII.E.2.d (claim 8[c])) that *is a metal layer*. Ex-1003, ¶¶225. Yamada discloses that “[t]he third reflective film (11) can be composed of a metal. . . .” Yamada, ¶[0012]; *see also id.*, ¶[0026] (“[t]hird reflective films 11 composed of a metal such as Al”).

F. Ground 6: Claims 8–11, 13 Are Obvious Based on Yamada and Schubert

1. Overview of Schubert

Schubert discusses the use of reflectors in optoelectronic devices. Specifically, Schubert is a textbook chapter titled “Reflectors,” and discusses potential reflectors, including distributed Bragg reflectors, as well as the characteristics of an ideal reflector. Schubert at 163. Ex-1003, ¶¶226–227.

2. Claim 8

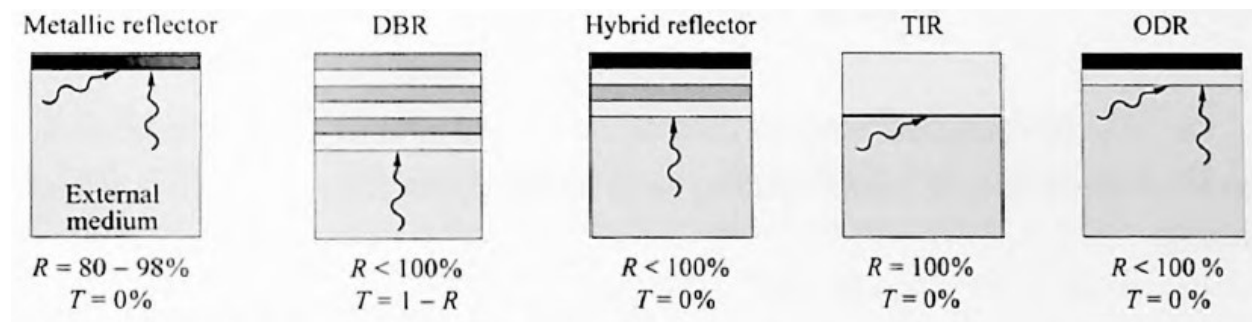
a) Limitations 8[pre]–[c], [f]

As discussed in Ground 5, Yamada teaches or suggests these limitations. *See* Section VII.E.2.

- b) 8[d]: “wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials”

Yamada alone teaches or suggests this limitation. *See* Section VII.E.2.e. Additionally, this limitation is obvious based on Yamada in view of Schubert. Ex-1003, ¶¶232–238.

As explained in Ground 6 above, Yamada discloses a peripheral light trapping material comprising third reflective film 11 that “can be composed of a metal.” Yamada, ¶[0012]. However, POSITAs would have recognized that there were other known materials and material combinations to use in such peripheral light trapping materials, each of which having its own benefits and considerations. Ex-1003, ¶233. For example, Schubert discusses the “[d]ifferent types of reflectors” to use in optoelectronic devices, i.e., “a metallic reflector, distributed Bragg reflector (DBR), hybrid reflector, total internal reflector (TIR), and a triple-layer omni-directional reflector (ODR).” Schubert at 163.



Schubert, Fig. 10.1; Ex-1003, ¶233. As a common example of a DBR, Schubert

further discloses alternating layers of silicon dioxide (having a refractive index of 1.46) and silicon (having a refractive index of 3.51). Schubert at 177. Such a Si/SiO₂ DBR comprises a *first material* (silicon layer) *sandwiched between two second materials* (silicon dioxide layers), as a DBR is a “multi-layer reflector consisting of typically 5–50 pairs of two materials with different refractive indices,” Schubert at 171; Ex-1003, ¶234.

Accordingly, it would have been obvious to use an Si/SiO₂ DBR (as taught in Schubert) in place of Yamada’s peripheral third reflective films 11 and first insulator 9, such that Yamada’s light receiving element includes a *peripheral light trapping material* (the Si/SiO₂ DBR) that *includes a first material* (silicon) *sandwiched between two second materials* (silicon dioxide). Ex-1003, ¶235. Moreover, in this DBR, *the first material* (silicon) *has a higher refractive index as compared to the two second materials* (silicon dioxide). *Id.*

Schubert teaches that Si/SiO₂ is a known DBR option that “yield[s] high reflectivity,” Schubert at 172. POSITAs would further understand that isolation elements comprising a metal thinly insulated from the photodiode may lead to increased dark current due to crystal defects. Ex-1003, ¶235. *Supra*, §VII.C.1 (Mori Overview); Mori ¶[0008] (“Furthermore, metal is embedded in the silicon material, ... [t]his also increases crystal defects in the silicon layer and increases charges generated when dark, resulting in a decrease in sensitivity.”); *see also id.*, ¶[0007].

A known solution to this problem was replacing such metal isolation elements (like Yamada's) with Si/SiO₂ partitions. Ex-1003, ¶235. *E.g.*, Mori, ¶¶[0029]–[0030] (“[I]n the partition part 163” “a silicon layer 175 is embedded in the partition groove” and a “partition part 163 also has a side SiO₂ film 177 formed on the ... side surfaces.... Thereby crystal defects occurring on the side surfaces of the separation trenches can be reduced....”).

POSITAs would have reasonably expected success in making such a combination. Ex-1003, ¶¶236–238. Yamada's third reflective films are used to reflect light back into the photodiode. *Supra*, §VII.E.2.c (claim 8[b]). Schubert teaches that Si/SiO₂ DBRs “yield high reflectivity,” Schubert at 172, and “high-contrast materials Si ($\bar{n} \approx 3.5$ at $\lambda = 1 \mu\text{m}$) and SiO₂ ($\bar{n} \approx 1.46$) are natural candidates for [omni-directional reflectors],” *id.* at 181. *See also id.*, Fig. 10.8 (showing a Si/SiO₂ reflector with four pairs having a 100% reflectance at approximately 1-1.4 μm), 170 (“DBR's reflectivity can be increased by increasing the number of reflector pairs....”). Indeed, Si/SiO₂ reflectors were used as light trapping materials in similar known image sensors. Ex-1003, ¶236. *E.g.*, Hwang, 9:25–30 (using silicon and silicon dioxide as alternating layers in its backside reflection layer); Mori, ¶¶[0029]–[0030].

Accordingly, using a Si/SiO₂ DBR would have been nothing more than a simple substitution of a Si/SiO₂ DBR for a metal layer to obtain predictable results

(e.g., high reflectivity, reduced dark current, and omnidirectional characteristics).

Ex-1003, ¶237.

- c) **8[e]: “wherein the difference in refractive index between the first material and the two second materials is at least 0.2”**

This limitation is obvious based on Yamada in view of Schubert. Ex-1003, ¶239. When using an Si/SiO₂ DBR in place of Yamada’s peripheral light trapping material, *the difference in refractive index between the first material* (silicon, $\bar{n} \approx 3.5$ at $\lambda = 1 \mu\text{m}$) *and the two second materials* (silicon dioxide, $\bar{n} \approx 1.46$) *is at least 0.2. Id.*

3. **Claim 9: “The device of claim 8, wherein the two second materials have a refractive index of less than about 2.1.”**

This claim is obvious based on Yamada in view of Schubert. Ex-1003, ¶241. When using an Si/SiO₂ DBR in place of Yamada’s peripheral light trapping material, *the two second materials* (silicon dioxide, $\bar{n} \approx 1.46$) *have a refractive index of less than about 2.1. Id.*

4. **Claim 10: “The device of claim 9, wherein at least one of the two second materials includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.”**

This claim is obvious based on Yamada in view of Schubert. Ex-1003, ¶242. When using an Si/SiO₂ DBR in place of Yamada’s peripheral light trapping material,

at least one of the two second materials includes an oxide, namely silicon dioxide.

Id.

5. **Claim 11: “The device of claim 9, wherein the at least one of the two second materials includes a member selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.”**

This claim is obvious based on Yamada in view of Schubert. Ex-1003, ¶243.

When using an Si/SiO₂ DBR in place of Yamada’s peripheral light trapping material,

at least one of the two second materials includes silicon dioxide. Id.

6. **Claim 13: “The device of claim 12, wherein the first material includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and combinations thereof.”**

This claim is obvious based on Yamada in view of Schubert. Ex-1003, ¶¶244–247. When using an Si/SiO₂ DBR in place of Yamada’s peripheral light trapping material, *the first material includes silicon*. POSITAs would understand silicon (as taught in Schubert) to be one of the claimed silicon types. *Id.* First, POSITAs would understand that references to “silicon,” without modification, typically pertain to *single crystal silicon*. Ex-1003, ¶246.

Second, to the extent that Schubert’s disclosure of “silicon” may be ambiguous, this claim still would have been obvious, because POSITAs would have had a limited number of types of silicon from which to choose, and in fact the group of silicon materials specified in this claim encompasses all forms of silicon. Ex-1018,

114 (“Silicon-films can be either amorphous, polycrystalline, or single-crystal...”); *see also id.* at 145; Ex-1003, ¶247.

G. Ground 7: Claims 1–7 Are Obvious Based on Yamada, Schubert, and Mori.

1. Claim 1

a) Limitations 1[pre]–[c], [f]

Limitations 1[pre]–[c] and 1[f] are identical to limitations 8[pre]–[c] and 8[f].

As discussed in Grounds 5 and 6, Yamada teaches or suggests these limitations.

Supra, §§VII.E.2, VII.F.2.

b) 1[d]: “wherein at least one of the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials”

Although the language of limitation 1[d] differs slightly from that of limitation 8[d], those differences do not alter the analysis. This limitation would have been obvious based on Yamada in view of Schubert for the reasons discussed in Section VII.F.2.b. As discussed above, it would have been obvious to use an Si/SiO₂ DBR (as taught in Schubert) in place of Yamada’s peripheral light trapping material. Ex-1003, ¶253. In such a configuration, *the peripheral light trapping material include a silicon layer sandwiched between two silicon dioxide layers. Id.* The silicon is *a high refractive index material* having a refractive index of approximately 3.5. *Id.*

The silicon dioxide is *a low refractive index material*, having a refractive index of approximately 1.46. *Id.*

- c) 1[e]: “wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field,”

This limitation is obvious based on Yamada in view of Schubert in further view of Mori. Ex-1003, ¶¶254–261.

Both Mori and Yamada (as modified by Schubert) use image sensors including multi-layer Si/SiO₂ partitions to mitigate against interference between pixels. Ex-1003, ¶255.

Mori teaches that “[i]n order to prevent charges generated when dark due to crystal defects ... p-type impurities are preferably injected into the side walls of partition groove 174 after forming the side SiO₂ film 177.” Mori, ¶[0036]. *Supra*, §VII.C.1 (Mori Overview).

Accordingly, Mori teaches that a *low refractive index material* (Mori’s SiO₂ film) *is doped with a dopant to create a surface field* as set forth in this limitation. Ex-1003, ¶¶256–257. The ’764 patent does not explain how doping the low refractive index material operates to create a surface field. Ex, 1003, ¶257. Rather, its only disclosure relating to such doping is that:

[I]t can also be beneficial to dope the sidewalls to create a surface field that will improve electrical isolation between the pixels. In one aspect,

it can also be beneficial to dope the low refractive index material of the Bragg-type reflectors to increase such electrical isolation.

'764 patent, 9:60–65. That is, the '764 patent teaches that doping in such a manner as in Mori serves to increase electrical isolation between the pixels via a surface field. Ex-1003, ¶257. Thus, Mori's doped SiO₂ film 177 along the side of its pixel (photoelectric conversion unit 161) would constitute *a low refractive index material doped with a dopant to create a surface field* to the extent that is contemplated by the limited disclosures of the '764 patent. Ex-1003, ¶257.

Based on Mori's teaching, it would have been obvious to similarly dope Yamada's (as modified by Schubert) silicon dioxide layer (*low refractive index material*)—such that it *is doped with a dopant to create a surface field* in the same manner as Mori's SiO₂ film. Ex-1003, ¶259. Yamada's (as modified by Schubert) silicon dioxide layer adjoins the side of Yamada's pixel (PIN photodiode 7), just like Mori's side SiO₂ film 177 adjoins Mori's pixel. Ex-1003, ¶259. Accordingly, POSITAs would have recognized that doping Yamada's (as modified by Schubert) silicon dioxide layer with p-type impurities would similarly mitigate dark current stemming from crystal defects in Yamada's sensor. Ex-1003, ¶259.

POSITAs would reasonably have expected success in making this modification, given that Yamada (as modified by Schubert) and Mori have similar arrangement of a silicon/silicon dioxide film disposed at the sidewall between pixels.

Ex-1003, ¶260. Moreover, this doping could have been readily implemented in Yamada's sensor, e.g., after applying the first SiO₂ layer. Ex-1003, ¶260.

2. Claim 2: “The device of claim 1, wherein the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.”

This claim is obvious based on Yamada in view of Schubert and Mori. Ex-1003, ¶¶263–264. As discussed with respect to limitation 1[d], when using an Si/SiO₂ DBR in place of Yamada's peripheral light trapping material, *the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials. Supra*, §§VII.F.2.b, VII.G.1.b.

Furthermore, as discussed in Section VII.E.2.e, Yamada's backside light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials. Yamada's first material, gallium phosphide, is a *high refractive index material*, having a refractive index of 3.5 at 500nm. Schubert, Table 10.1; Ex-1003, ¶264. Yamada's second material, aluminum phosphide, is a *low refractive index material*, having a refractive index of “2.75±.1 at 2.8eV,” Ex-1021 at 153, or “about 2.8,” at 530nm, Ex-1022, 5:11–12. Ex-1003, ¶264.

3. Claim 3: “The device of claim 1, wherein the dopant is boron or antimony.”

This claim is obvious based on Yamada in view of Schubert and Mori. Ex-1003, ¶¶265–267.

As discussed for limitation 1[e], doping the silicon dioxide layer used in Yamada (as modified by Schubert) with p-type impurities—i.e., a p-type dopant—would have been obvious in view of Mori. Ex-1003, ¶¶254–261, 266. Using boron as the p-type dopant would be obvious, as boron is one of the most commonly used p-type dopants for Si-based systems. Ex-1003, ¶266. *E.g.*, Ex-1017 (explaining silicon is commonly doped with Column-III-dopants (e.g., boron)). POSITAs would have recognized that using boron as a p-type dopant for silicon-based systems is a known technique that would have yielded predictable results, particularly in light of boron’s similar use as a p-type dopant in other similar light trapping devices. Ex-1003, ¶266. *E.g.*, Ex-1019, ¶[0011] (“silicon substrate doped with a P-type dopant such as boron”). Additionally, using boron would have been obvious to try, as POSITAs would have had a limited number of types of p-type dopants from which to choose. Ex-1003, ¶266.

4. Claims 4–5

These claim are obvious based on Yamada in view of Schubert and in further view of Mori. Ex-1003, ¶¶268–269. The additional limitations of claims 4–5 are

identical those of claims 14–15. Yamada teaches or suggests these limitations for the reasons discussed in Sections VII.E.4–5.

5. Claim 6: “The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”

This claim is obvious based on Yamada in view of Schubert and Mori. Ex-1003, ¶270. As discussed in Section VII.E.2.c, Yamada’s “first reflective film (3)” is the backside light trapping material. Yamada, ¶[0009]. Ex-1003, ¶270. In some embodiments, Yamada’s first reflective film comprises “an $\text{Al}_x\text{Ga}_{1-x}\text{P}$ semiconductor multilayer film.” Yamada, ¶[0021]. However, Yamada also discloses an embodiment in which “the first reflecting film 3 is made of a metal such as Al.” *Id.* ¶[0048]; *see also id.* ¶[0047] (“Other details are the same as in the third embodiment....”).

6. Claim 7: “An array of light trapping pixel devices of claim 1.”

This claim is obvious based on Yamada in view of Schubert and Mori. Ex-1003, ¶271. Yamada discloses that it was “conventionally known” to form a light receiving element having a plurality of light receiving sections “and to arrange these light receiving sections in a two-dimensional array. Yamada, ¶[0002]. Yamada further discloses that “[t]he light receiving sections (7) can be arranged in a matrix.” *Id.* ¶[0018]. Yamada therefore teaches or suggests *an array of light trapping pixel devices of claim 1*.

H. Ground 8: Claims 17–25 Are Obvious Based on Yamada and Konno.

1. Claim 17

a) Limitations 17[pre]–[c], [e]

Limitations 17[pre]–[c] and 17[e] are identical to limitations 8[pre]–[c] and 8[f]. Yamada teaches or suggests these limitations for the reasons discussed in Section VII.E.2.

b) 17[d]: “wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface”

This limitation is obvious based on Yamada in view of Konno. Ex-1003, ¶¶277–281.

In Konno’s Figure 8 embodiment, the solid-state imaging element includes a second reflecting layer 120 constituting a *backside light trapping material* that *has a sloped surface*. Ex-1003, ¶278–279. That is, Konno teaches that its “second reflecting layer 120,” can have “inclines,” as illustrated below. Konno, 15:36–38.

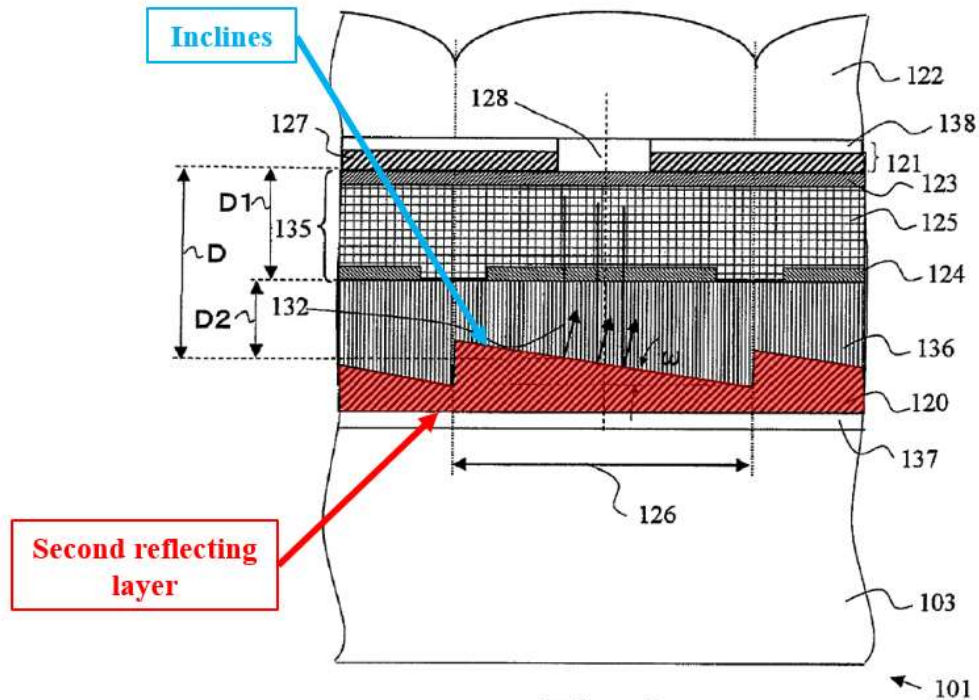


Fig. 8

Id., Fig. 8 (annotated); Ex-1003, ¶278. Konno explains that “inclination of the reflecting surface is designed so that most of photons which entered at the end of the light entrance window 128 ... reach to the first reflecting layer 121” to increase sensitivity. Konno, 15:38–50.

Therefore, it would have been obvious to use Konno's inclined surface in Yamada's light receiving element—i.e., forming Yamada's first reflective film 3 with a sloped surface—to improve efficiency in a similar manner. Ex-1003, ¶280.

This modification results in Yamada's light receiving element having a *backside light trapping material* (i.e., Yamada's first reflective film 3) *that has a sloped surface at the pixel device interface*. Ex-1003, ¶280.

POSITAs would have been motivated to make this modification, as such an inclined surface would redirect light to Yamada's third reflective films (11) and/or second reflective film (8) to increase efficiency. Ex-1003, ¶281.

POSITAs would reasonably have expected success in implementing Konno's sloped surface, as, e.g., it could be implemented during the manufacturing steps shown in Yamada's Figure 2(a). Ex-1003, ¶281.

2. Claim 21

a) Limitations 21[pre]–[c],[e]

Limitations 21[pre]–[c] and 21[e] are identical to limitations 8[pre]–[c] and 8[f]. Yamada teaches or suggests these limitations for the reasons discussed in Sections VII.E.2.

b) 21[d]: “a textured layer positioned to interact with light proximal to the backside surface”

This limitation is obvious based on Yamada in view of Konno. Ex-1003, ¶¶290–299.

Konno includes transparent layer 136 between photoelectric conversion element 135 and second reflecting layer 120. In Konno's Figure 7 embodiment, the transparent layer is textured by “forming concaves and convexes on the surface of the transparent layer 136.” Konno, 14:38–40. The textured surface “can be formed by a known technique such as sputtering and microlithography.” *Id.*, 14:43–45. Konno's second reflective layer may then formed on the transparent layer by

“depositing a metal” thereby forming concaves and convexes in the reflective layer.

Id., 14:38–43.

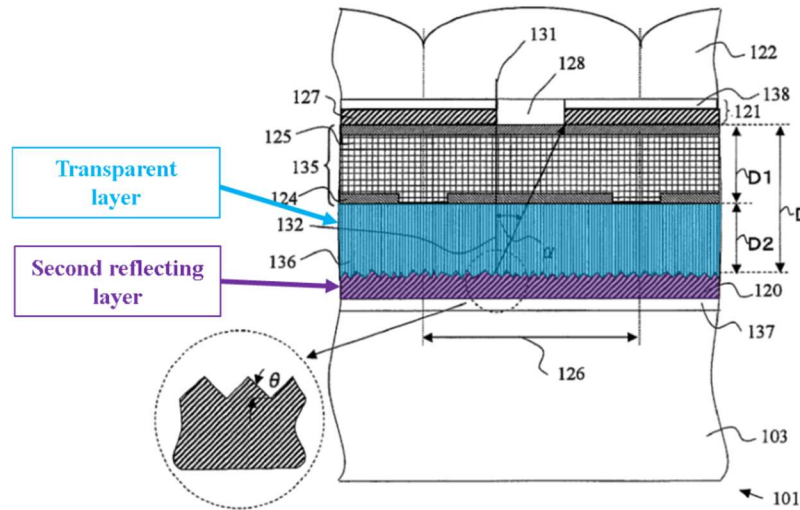


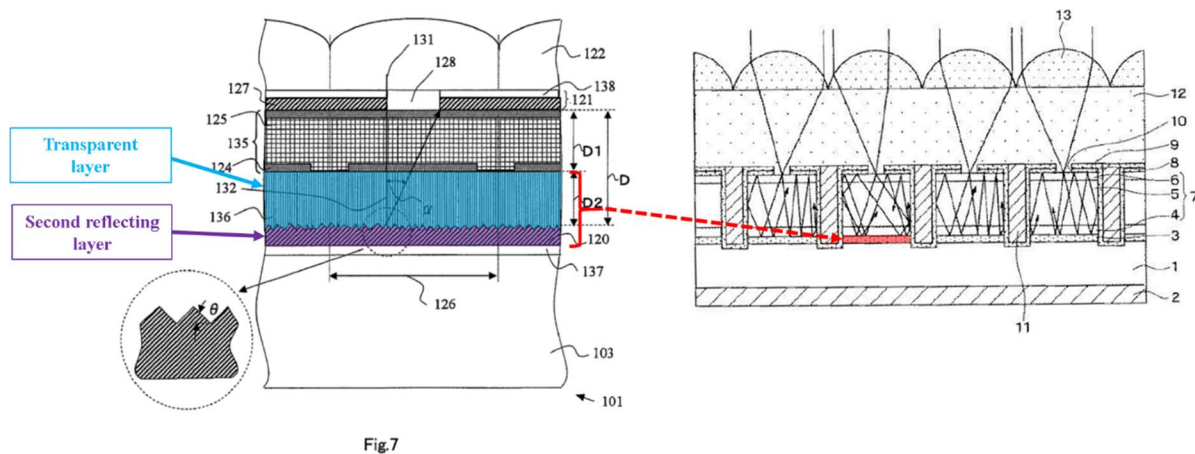
Fig.7

Konno, Fig. 7 (annotated); Ex-1003, ¶291.

Konno’s transparent layer is *a textured layer positioned to interact with light proximal to the backside surface*. As shown in Figure 6, the transparent layer is formed on the backside surface of photoelectric conversion element 135. The texturing of the transparent layer, and the resulting shape of the second reflecting layer are so that “[w]hen it reflects the incident photons 132, it can thereby reflect them with a large amount of horizontal components.” Konno, 13:63–66. In this way, “the amount of photons to be detected again by the photoelectric conversion film 125 can be increased,” thereby increasing the sensitivity of the device. *Id.*, 13:66–14:3; Ex-1003, ¶¶292–293. In particular, “[t]he photons not absorbed by the photoelectric conversion film 125 transmit the pixel electrode 124 and the

transparent layer 136 and reach the second reflecting layer.” Konno, 9:64–67. By transmitting the photons not absorbed by the photoelectric conversion film, the transparent layer is *positioned to interact with light proximal to the backside surface*. Ex-1003, ¶293.

It would have been obvious to use Konno’s textured transparent layer in Yamada’s light receiving element to improve efficiency in a similar manner. Ex-1003, ¶294.



Konno, Fig. 3 (annotated); Yamada Fig. 6 (annotated); Ex-1003, ¶294. As shown above, this modification results in Yamada’s device having a *textured layer* (the transparent layer) *positioned to interact with light proximal to the backside surface*.

Both Yamada and Konno teach using a metal layer as the backside light trapping material. See Yamada, ¶[0048] (“As shown in FIG. 6, the light receiving element of the present embodiment is configured such that the first reflecting film 3 is made of a metal such as Al.”); Konno, 8:31–38 (second reflecting layer 120 “can

be formed by forming a thin film of a metal such as aluminum and silver by deposition or the like”). It would have been obvious to include Konno’s textured transparent layer in order to texture Yamada’s first reflective film. Ex-1003, ¶¶295–297

POSITAs would have been motivated to make this modification. Konno teaches that the transparent layer makes it “possible to increase amount of photons reciprocating in a space between the second reflecting layer 120 and the first reflecting layer 121 including the photoelectric conversion element 135,” thereby increasing the sensitivity of the device. Konno, 9:42–51. This configuration causes photons reflecting off the backside light trapping material to reflect “with a large reflection angle,” *id.*, 13:63–66, which would redirect light towards Yamada third reflective film. As Konno explains, the “amount of photons reciprocating without being detected decreases exponentially to the number of times of reflection. *Id.*, 18:53–55. Therefore, by directing the photons towards the third reflective film, the textured transparent layer would further increase the efficiency and the sensitivity of Yamada’s device. Ex-1003, ¶¶296–297.

POSITAs would reasonably have expected success in making this modification. Ex-1003, ¶¶298–299. Yamada already discloses forming the first reflecting film 3 from “a metal such as Al[uminum].” Yamada, ¶[0048]. POSITAs would have understood that texturing the metal layer using the techniques disclose

in Konno, such as microlithography, *see* Konno, 14:42–45, was nothing more than the application of a known technique that would have yielded predictable results. Ex-1003, ¶¶298. POSITAs would also have expected to succeed in forming a transparent layer. According to Konno, the transparent layer can be made from glass, i.e., silicon dioxide. Konno, 9:35–41. Forming layers of silicon dioxide in such light receiving elements was a well-known technique with predictable results. Ex-1003, ¶¶299. Additionally, a POSITA would have been motivated to include a layer of silicon dioxide on top of the textured first reflecting film as a planarization layer on which to form Yamada’s light receiving section 7. Ex-1003, ¶¶299.

3. Claim 22: “The device of claim 21, wherein the textured layer is located between the backside surface and the backside light trapping material.”

This claim is obvious based on Yamada in view of Konno. Ex-1003, ¶¶301.

As discussed with respect to limitation 21[d], above, it would have been obvious to modify Yamada to incorporate Konno’s textured region, as illustrated in the figure below.

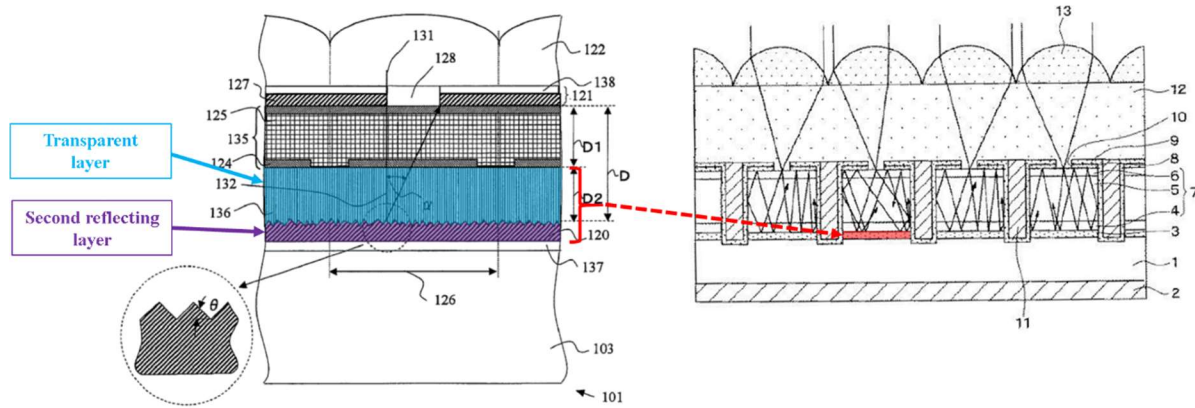


Fig.7

Konno, Fig. 3 (annotated); Yamada Fig. 6 (annotated); Ex-1003, ¶301. As shown, the textured layer (in blue) is located between the backside surface of the pixel and the backside light trapping material (in purple).

4. Claims 18, 23

The additional limitations of claims 18 and 23 are identical to that of claim 14. Yamada teaches or suggests these limitations for the reasons discussed in Section VII.E.4.

5. Claims 19, 24

The additional limitations of claims 19 and 24 are identical to that of claim 15. Yamada teaches or suggests these limitations for the reasons discussed in Section VII.E.5.

6. Claims 20, 25

The additional limitations of claims 20 and 25 are identical to that of claim 16. Yamada teaches or suggests these limitations for the reasons discussed in Section VII.E.6.

VIII. DISCRETIONARY DENIAL IS INAPPROPRIATE

The Board should not exercise its discretion to deny institution under 35 U.S.C. §314(a). No other petitions have been filed against the '764 patent, thus the *General Plastic* factors for serial petitions do not weigh against institution. The existence of a parallel ITC proceeding should not be a factor for consideration in determining whether the Board may exercise its discretion to deny institution. Vidal, K., Memorandum—Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, USPTO (June 21, 2022) at 6–7, https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf. The parallel district court case has been stayed. Discretionary denial is further inappropriate because this petition presents compelling evidence of unpatentability. Accordingly, the *Fintiv* factors should not be applied to deny institution of this proceeding.

IX. CONCLUSION

Petitioner respectfully requests *inter partes* review and cancellation of the Challenged Claims of the '764 patent.

Date: November 29, 2024

Respectfully submitted,

By: /Dave A. Garr /

Dave A. Garr

Registration No.: 74,932

COVINGTON & BURLING LLP

Petition for *Inter Partes* Review of U.S. Pat. No. 9,064,764

One CityCenter, 850 Tenth Street, NW
Washington, DC 20001

Scott C. Weidenfeller
Reg No.: 54,531
sweidenfeller@cov.com
COVINGTON & BURLING LLP
One CityCenter, 850 Tenth Street, NW
Washington, DC 20001

Alice J. Ahn
Reg. No.: 79,829
COVINGTON & BURLING LLP
Salesforce Tower
415 Mission Street, Ste 5400
San Francisco, CA 94105-2533

CLAIMS APPENDIX

1[pre]. A light trapping device, comprising:

1[a] at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

1[b] a backside light trapping material substantially covering the backside surface; and

1[c] a peripheral light trapping material substantially covering the peripheral sidewall,

1[d] wherein at least one of the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials,

1[e] wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field, and

1[f] wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

2. The device of claim 1, wherein the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.

3. The device of claim 1, wherein the dopant is boron or antimony.

4. The device of claim 1, wherein the peripheral sidewall extends completely around the pixel periphery.

5. The device of claim 1, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

6. The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

7. An array of light trapping pixel devices of claim 1.

8[pre]. A light trapping device, comprising:

8[a] at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

8[b] a backside light trapping material substantially covering the backside surface; and

8[c] a peripheral light trapping material substantially covering the peripheral sidewall,

8[d] wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials, and

8[e] wherein the difference in refractive index between the first material and the two second materials is at least 0.2, and

8[f] wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

9. The device of claim 8, wherein the two second materials have a refractive index of less than about 2.1.

10. The device of claim 9, wherein at least one of the two second materials includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.

11. The device of claim 9, wherein the at least one of the two second materials includes a member selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.

12. The device of claim 8, wherein the first material includes a material having a refractive index of greater than or equal to about 2.1.

13. The device of claim 12, wherein the first material includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and combinations thereof.

14. The device of claim 8, wherein the peripheral sidewall extends completely around the pixel periphery.

15. The device of claim 8, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

16. The device of claim 8, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

17[pre]. A light trapping device, comprising:

17[a] at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

17[b] a backside light trapping material substantially covering the backside surface; and

17[c] a peripheral light trapping material substantially covering the peripheral sidewall,

17[d] wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface, and

17[e] wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

18. The device of claim 17, wherein the peripheral sidewall extends completely around the pixel periphery.

19. The device of claim 17, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

20. The device of claim 17, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

21[pre]. A light trapping device, comprising:

21[a] at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

21[b] a backside light trapping material substantially covering the backside surface; a peripheral light trapping material substantially covering the peripheral sidewall; and

21[c] a peripheral light trapping material substantially covering the peripheral sidewall,

21[d] a textured layer positioned to interact with light proximal to the backside surface,

21[e] wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

22. The device of claim 21, wherein the textured layer is located between the backside surface and the backside light trapping material.

23. The device of claim 21, wherein the peripheral sidewall extends completely around the pixel periphery.

24. The device of claim 21, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

25. The device of claim 21, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

CERTIFICATION OF WORD COUNT

I certify that the foregoing complies with the type-volume limitation of 37 C.F.R. § 42.24 and contains 13,334 words based on the word count indicated by the word-processing system used to prepare the paper, and excluding those portions exempted by § 42.24(a).

Date: November 29, 2024

/Dave A. Garr/

Dave A. Garr (Reg. No. 74,932)

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6 and 42.105, I hereby certify that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,064,764 under U.S.C. §§ 311–319 and 37 C.F.R. § 42.100 *et seq.*, together with its supporting exhibits, and Power of Attorney was served by Federal Express for Saturday delivery, a means at least as fast and reliable as Priority Mail Express®, on the following correspondence address of record for patent owner:

Troutman Pepper Hamilton Sanders LLP
70 Linden Oaks
Suite 210
Rochester, NY 14625
Customer # 11951

A courtesy copy was also sent patent owner's litigation counsel:

Troutman Pepper Hamilton Sanders LLP
19th Floor, High Street Tower
125 High Street
Boston, MA 02110-2736
SiOnyxITC@troutman.com

Date: November 29, 2024

/Dave A. Garr/

Dave A. Garr (Reg. No. 74,932)