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January 16, 2024

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APPLICATION NUMBER: *14/747,875*
FILING DATE: *June 23, 2015*
PATENT NUMBER: *9905599*
ISSUE DATE: *February 27, 2018*

Certified by

Performing the Functions and Duties of the
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP.CON
	Application Number	
Title of Invention	Pixel Isolation Elements, Devices and Associated Methods	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Martin	U.	Pralle	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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Prefix	Given Name	Middle Name	Family Name	Suffix
	Jason		Sickler	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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Postal Code	02474	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	20551		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	Pixel Isolation Elements, Devices and Associated Methods		
Attorney Docket Number	3035-052.NP.CON	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	4	Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

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Customer Number	20551

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	13/841120	2013-03-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
13/841120	Claims benefit of provisional	61/614275	2012-03-22

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Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) [i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

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Application Number	Country [i]	Filing Date (YYYY-MM-DD)	Access Code [i] (if applicable)

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(•) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. [X]

Organization Name	SiOnyx, Inc.

Mailing Address Information:

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Country [i]	US	Postal Code	01915
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

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Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

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If the Assignee or Non-Applicant Assignee is an Organization check here. [X]

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Title of Invention	Pixel Isolation Elements, Devices and Associated Methods	

Organization Name	SiOnyx, Inc.

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Address 2			
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Country i	US	Postal Code	01915
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

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NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/Todd B. Alder/			Date (YYYY-MM-DD)	2015-06-23
First Name	Todd B.	Last Name	Alder	Registration Number	54598

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS

PRIORITY DATA

This application is a continuation of U.S. Patent Application Serial No. 13/841,120, filed March 15, 2013, which claims the benefit of U.S. Provisional Patent Application Serial No. 61/614,275, filed on March 22, 2012, each of which are incorporated herein by reference.

BACKGROUND

Image sensors are typically formed on various forms of semiconductor materials such as, for example, silicon. Imagers can be incorporated into a variety of devices, including digital cameras, camcorders, computers, cell phones, etc. Due to the ever decreasing size (foot print) of these devices, image sensors have correspondingly seen a decrease in size. Backside illuminated (BSI) image sensors have increased in importance due to the small size of these imagers as compared to front side illuminated (FSI) image sensors. However, pixel size reduction can lead to a significant sacrifice in image quality. As pixel sizes continue to decrease, image signal to noise tends to decrease while electrical and optical cross-talk between adjacent sensor pixels tends to increase. Traditional attempts to reduce the impact of these effects have included adding microlenses above each image sensor in front side pixel sensors to focus the light on the active detector regions, thereby increasing efficiency and reducing cross-talk. Backside illuminated pixel sensors can present different design considerations. For example, significant cross-talk can be generated due to reflection off the often planar back surface of the device.

SUMMARY

The present disclosure provides for light trapping pixels, devices incorporating such pixels, photovoltaic solar cells, and other optoelectronic devices, including various associated methods. In one aspect, for example, a light trapping device can include at least one light sensitive pixel having a light incident surface, a backside surface opposite

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the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery. The pixel can also include a backside light trapping material substantially covering the backside surface and a peripheral light trapping material substantially covering the peripheral sidewall. The light contacting the backside light trapping material or the peripheral light trapping material is thus reflected back toward the pixel. In another aspect, the present disclosure additionally provides an array of light trapping pixels.

A variety of light trapping materials can be utilized and are contemplated, and any such material capable of being used to trap light in a pixel is considered to be within the present scope. In one aspect, at least one of the backside light trapping material and the peripheral light trapping material can include a high refractive index material sandwiched between two low refractive index materials. In another aspect, the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials. It is contemplated that the two low refractive index materials have a refractive index of less than about 2.1. Non-limiting examples of low refractive index material can include nitrides, oxynitrides, gasses, at least a partial vacuum, and the like, including appropriate combinations thereof. Other non-limiting examples of low refractive index materials can include silicon oxide, silicon nitride, silicon dioxide, and the like. Furthermore, in another aspect a light trapping material can include a higher refractive index material sandwiched between two materials having a refractive index that is at least 0.2 lower as compared to the higher refractive index material. In this case, the materials are not limited by the definition of low vs. high refractive index outlined above, but are rather defined by the relative difference in refractive index.

Furthermore, it is contemplated that high refractive index materials have a refractive index of greater than or equal to about 2.1. Non-limiting examples of high refractive index material can include polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and the like, including appropriate combinations thereof.

In one aspect, the peripheral sidewall can extend completely around the pixel periphery. In another aspect, the peripheral sidewall can extend from the light incident surface towards the backside surface.

In some aspects it is also contemplated that the light incident surface can include a frontside light trapping material at least partially covering the surface thereof. In one aspect, the frontside light trapping material can be an antireflective layer coating. In another aspect, the frontside light trapping material can be a reflective layer having an aperture to allow entry of light into the pixel, wherein the reflective layer is operable to reflect light impinging thereupon from inside the pixel back into the pixel. In some aspects it can be beneficial to include a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.

In another aspect the present disclosure additionally provides a substantially light trapping pixel device including a light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending from the light incident surface to the backside surface and extending around the pixel periphery. The pixel additionally includes a backside light trapping material substantially covering the backside surface, and a peripheral light trapping material substantially covering the peripheral sidewall. Furthermore, an internally reflective frontside light trapping material can cover at least a portion of the light incident surface that is operable to allow entrance of light into the pixel and is operable to reflect light impinging thereupon from inside the pixel back into the pixel, and the light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

In yet another aspect, the present disclosure provides a method of making a light trapping device, including forming at least one pixel by forming a backside light trapping material on a semiconductor layer, the backside light trapping material including a high refractive index material sandwiched between two low refractive index materials, and forming a pixel device layer on the semiconductor layer opposite the light trapping material. The method can additionally include etching a trench circumscribing the pixel device layer and filling the trench with a light trapping material. In some aspects, the trench can be etched to a depth that contacts at least the first low refractive index

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material. In some aspects, an incident light trapping material can be applied to the pixel device layer. It is also noted that the light trapping material can be located anywhere in the backside region of the device, and that the current scope is not limited to the location of materials or the manufacturing method described above.

In another aspect, filling the trench with the light trapping material can further include depositing a low refractive index material into the trench to fill a portion of the trench from the trench walls inward, ceasing deposition of the low refractive index material to leave an internal space within the trench, and depositing a high refractive index material into the trench to fill the internal space.

In another aspect, the method can include forming a textured region on at least a portion of the semiconductor layer between the semiconductor layer and the first low refractive index prior to depositing the first low refractive index material onto the semiconductor layer. Non-limiting examples of techniques for forming the textured region include plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, the like, including appropriate combinations thereof. In one specific aspect, forming the textured region includes laser texturing.

BRIEF DESCRIPTION OF THE DRAWINGS

For a further understanding of the nature and advantage of the present disclosure, reference is being made to the following detailed description of embodiments and in connection with the accompanying drawings, in which:

FIG. 1 is a cross-sectional view of multiple image sensor pixels in accordance with an embodiment of the present disclosure;

FIG. 2 is a cross-sectional view of multiple image sensor pixels in accordance with another embodiment of the present disclosure;

FIG. 3 is a cross-sectional view of multiple image sensor pixels in accordance with another embodiment of the present disclosure;

FIG. 4 is a cross-sectional view of a light trapping pixel in accordance with another embodiment of the present disclosure;

FIG. 5 is a cross-sectional view of a light trapping pixel in accordance with another embodiment of the present disclosure;

FIG. 6 is a cross-sectional view of a light trapping pixel in accordance with another embodiment of the present disclosure; and

FIG. 7 is a depiction of a method of making a light trapping pixel in accordance with yet another aspect of the present disclosure.

DETAILED DESCRIPTION

Before the present disclosure is described herein, it is to be understood that this disclosure is not limited to the particular structures, process steps, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting.

Definitions

The following terminology will be used in accordance with the definitions set forth below.

It should be noted that, as used in this specification and the appended claims, the singular forms "a," and, "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a dopant" includes one or more of such dopants and reference to "the layer" includes reference to one or more of such layers.

As used herein, the terms "light" and "electromagnetic radiation" can be used interchangeably and can refer to electromagnetic radiation in the ultraviolet, visible, near infrared and infrared spectra. The terms can further more broadly include electromagnetic radiation such as radio waves, microwaves, x-rays, and gamma rays. Thus, the term "light" is not limited to electromagnetic radiation in the visible spectrum. Many examples of light described herein refer specifically to electromagnetic radiation in the visible and infrared (and/or near infrared) spectra. For purposes of this disclosure, visible range wavelengths are considered to be from approximately 350 nm to 800 nm and non-visible wavelengths are considered to be longer than about 800 nm or shorter than about 350 nm. Furthermore, the infrared spectrum is considered to include a near

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infrared portion of the spectrum including wavelengths of approximately 800 to 1100 nm, a short wave infrared portion of the spectrum including wavelengths of approximately 1100 nm to 3 micrometers, and a mid-to-long wavelength infrared (or thermal infrared) portion of the spectrum including wavelengths greater than about 3 micrometers up to about 30 micrometers. These are generally and collectively referred to herein as "infrared" portions of the electromagnetic spectrum unless otherwise noted.

As used herein, "quantum efficiency" (QE) is typically referring to "external quantum efficiency" (EQE) which is defined as the ratio of electrons collected per photons incident on an optoelectronic device. "Internal quantum efficiency" is defined as the ratio of electrons collected per photons absorbed by an optoelectronic device..

As used herein, the terms "3D" and "three dimensional" can be used interchangeably, and refer to obtaining distance information using electromagnetic radiation.

As used herein, the terms "disordered surface" and "textured surface" can be used interchangeably, and refer to a surface having a topology with nano- to micron-sized surface variations. Such a surface topology can be formed by the irradiation of a laser pulse or laser pulses, chemical etching, wet or dry etching including masked or maskless etching, lithographic patterning, interference of multiple simultaneous laser pulses, reactive ion etching, plasma etching or any other technique that can be used to form such a topology. While the characteristics of such a surface can be variable depending on the materials and techniques employed, in one aspect such a surface can be several hundred nanometers thick and made up of nanocrystallites (e.g. from about 10 to about 50 nanometers), nanopores, and the like. In another aspect, such a surface can include micron-sized structures (e.g. about 1 μm to about 60 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 500 μm. A variety of criteria can be utilized to measure the size of such structures. For example, for cone-like structures the above ranges are intended to be measured from the peak of a structure to the valley formed between that structure and an adjacent neighboring structure. For structures such as nanopores, the above ranges are intended to be approximate diameters. Additionally, the surface structures can be spaced at various average distances from one another. In one aspect, neighboring structures can be spaced

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at a distance of from about 50nm to about 50 μm. In another aspect, neighboring structures can be spaced at a distance of from about 50nm to about 2 μm. Such spacing is intended to be from a center point of one structure to the center point of a neighboring structure.

As used herein, the term "fluence" refers to the amount of energy from a single pulse of laser radiation that passes through a unit area. In other words, "fluence" can be described as the energy density of one laser pulse.

As used herein, the term "target region" refers to an area of a semiconductor material that is intended to be doped or surface modified. The target region of a semiconductor material can vary as the surface modifying process progresses. For example, after a first target region is doped or surface modified, a second target region may be selected on the same semiconductor material.

As used herein, the term "absorptance" refers to the fraction of incident electromagnetic radiation absorbed by a material or device.

As used herein, the term "monolithic" refers to an electronic device in which electronic components are formed on the same substrate. For example, two monolithic pixel elements are pixel elements that are formed on the same semiconductor substrate.

As used herein, the term "substantially" refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is "substantially" enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use of "substantially" is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is "substantially free of" particles would either completely lack particles, or so nearly completely lack particles that the effect would be the same as if it completely lacked particles. In other words, a composition that is "substantially free of" an ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

As used herein, the term "about" is used to provide flexibility to a numerical range endpoint by providing that a given value may be "a little above" or "a little below" the endpoint.

As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of "about 1 to about 5" should be interpreted to include not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

The Disclosure

The present disclosure provides semiconductor devices and associated methods that can exhibit various enhanced properties, such as, for example, enhanced light detection properties. More specifically, in one aspect the disclosure relates to image sensor pixels and elements for trapping light within such pixels. In other aspects, various light trapping elements can additionally isolate neighboring pixels in an image sensor. Isolation elements can be configured to optically and/or electrically isolate neighboring

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pixels from one another in addition to trapping light with in the pixel. It is additionally contemplated that the present disclosure is applicable to other optoelectronic devices such as solar cells, and that all such should be included in the present scope.

In various aspects, image sensors can be front side or backside illuminated, 3D sensors, or any other device or system that incorporate a unique isolation element configured to reduce cross-talk between pixel elements. For example, in one aspect an image sensor can be capable of detecting visible and infrared light, whereas an isolation element associated with such an imager can be designed and configured to reduce and in some cases eliminate electrical and/or optical cross-talk between neighboring pixels from straying visible and infrared light. In some cases, isolation elements can be doped with a dopant that enables the repelling of electrical carriers from the isolation elements or in other words from the side walls of the device. In other cases, isolation elements can include light trapping or reflective materials to optically isolate neighboring pixels. It is additionally contemplated that isolation elements can include both a dopant and a light trapping or reflective material to both electrically and optically isolate the pixels. Moreover, isolation elements can also include surface features formed thereon or associated therewith. Additionally, in some cases a pixel can include a textured region to enhance the detection of infrared light among other things.

In one aspect, a variety of optoelectronic devices are provided such as, without limitation, photosensitive diodes, pixels, and imagers capable of detecting visible and infrared light while exhibiting reduced optical and electrical cross-talk between neighboring pixels or diodes. It is also contemplated that the present scope include methods associated with such devices, including methods of making and using. The present devices can additionally exhibit enhanced absorption and quantum efficiencies. Such devices can also include a plurality of photodiodes or pixels. In some cases, the present devices can achieve a quantum efficiency of 10% for wavelengths at 1064nm and having a thickness of less than 10 microns. In another embodiment, the present device can achieve a quantum efficiency of about 20% for wavelengths at 940nm and a thickness of less than 10 microns.

In one aspect, a device can include at least a semiconductor substrate having a first side for receiving incident light and a second side opposite the first side. Either or

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both the first or second sides can include at least one doped region. Furthermore, the image sensor can include at least one isolation element or feature for at least partially separating and isolating neighboring pixels. FIG. 1 illustrates a simplified drawing of an imager having a first pixel 102 and a second pixel 104, that are formed monolithically on a common semiconductor substrate 106 and are isolated from one another by an isolation element 114. Doped regions 108 and 110 can be disposed on either the first side 120 or second side 122 of the semiconductor substrate, or in some cases on opposite sides of the device. In the present figure, the device is configured such that the first side is capable of receiving incident light. A textured region 112 having surface features is shown on the second side 122 of the semiconductor substrate 106. This architecture having the texture region 112 on the back side 122 can enable enhanced detection and absorption of electromagnetic radiation having wavelengths in the range of about 600 nm to about 1200 nm. It should be noted that this architecture can be used in either a FSI or BSI image sensor architecture. Furthermore, the textured region can be located on the first side 120, the second side 122, or both the first and second sides.

In a typical FSI imager, incident light enters the semiconductor device by first passing by transistors and metal circuitry. The light, however, scatters off of the transistors and circuitry prior to entering the light sensing portion of the imager, thus causing optical loss and noise. A lens can be disposed on the topside of a FSI pixel to direct and focus the incident light to the light sensing active region of the device, thus partially avoiding the circuitry. BSI imagers, one the other hand, are configured to have the light sensing portion of the device opposite the circuitry. Incident light enters the device via the light sensing portion and is at least partially absorbed by the device prior to reaching the circuitry. BSI designs allow for smaller pixel architecture and a high fill factor for the imager. As mentioned, the devices according to aspects of the present disclosure can be adapted for either configuration. It should also be understood that devices according to aspects of the present disclosure can be incorporated into complimentary metal-oxide-semiconductor (CMOS) imager architectures or charge-coupled device (CCD) imager architectures, as well as other optoelectronic devices.

Regarding isolation elements, also referred to herein as trench isolation features or sidewalls, various processes can be employed to form the isolation elements. It is

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contemplated that the isolation features can extend from either the first surface or the second surface into the semiconductor material and depending on the depth of the trench can be considered either deep trench isolation or shallow trench isolation. The dimensions of the trench can vary, depending on the application. For example, trenches can have parallel walls, or they can have sloping walls, bottle neck architecture, or any other useful configuration. The depth of the trench isolation feature can be in the range of from about 100 nm to about 50 μm depending on the design of the device. The width can be in the range of from about 100 nm to about 10 μm. For simplicity, the figures in this disclosure show deep trench isolation but it should be understood that shallow trench isolation architectures can be utilized, and that deep trench isolation need not completely extend from one side to the other. The processes contemplated for forming trenches or other isolation features can include, reactive ion etch, isotropic plasma etch, wet chemical etch, laser irradiation, or any other known etch technique.

A variety of reflective materials can be utilized in constructing the isolation features in order to provide optical isolation, light trapping, and/or electrical isolation, and any such material capable of incorporation into a photosensitive device is considered to be within the present scope. Non-limiting examples of such materials include a Bragg reflector, a metal reflector, a metal reflector over a dielectric material, a transparent conductive oxide such as zinc oxide, indium oxide, or tin oxide, and the like, including combinations thereof. Non-limiting examples of metal reflector materials can include silver, aluminum, gold, platinum, reflective metal nitrides, reflective metal oxides, and the like, including combinations thereof. In one specific aspect, the dielectric layer can include an oxide layer and the reflecting region can include a metal layer. The surface of the metal layer on an oxide acts as a mirror-like reflector for the incident electromagnetic radiation. In addition, in some aspects trench isolation features can be doped to further affect the properties of the material with respect to electrical isolation.

In one specific aspect, a reflective region can include a transparent conductive oxide, an oxide, and a metal layer. The transparent oxide can be textured and a metal reflector deposited thereupon. The textured surface of the metal on a roughened transparent conductive oxide can act as a diffusive scattering site for the incident electromagnetic radiation.

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In some cases, materials having disparate properties can be utilized in the trench isolation features in order to derive a useful combined interaction. As is shown in FIG. 2, for example, an imager having at least two pixels or photodiodes (202 and 204) and at least one isolation element 214. The pixels are shown formed monolithically on a common semiconductor substrate 206. Doped regions 208 and 210 can be disposed on either the first side 220 or second side 222 of the semiconductor substrate. A textured region 212 having surface features is created on the second side 222 of the semiconductor substrate 206.

In some aspects, the isolation element 214 can be designed to function as a Bragg reflector. In such cases, the isolation element 214 includes at least two layers 216 comprised of material having a lower refractive index (n) as compared to the material of the third layer 218 disposed or sandwiched therebetween. In other words, the isolation element includes a high refractive index material sandwiched between two low refractive index materials, and such a configuration forms a Bragg reflector. Additionally, in some aspects the low reflective index materials can be chosen to have a lower refractive index as compared to the semiconductor substrate 206.

Furthermore, in another aspect an isolation element or light trapping material can include a higher refractive index material sandwiched between two materials having a refractive index that is at least 0.2 lower as compared to the higher refractive index material. In this case, the materials are not limited by the definition of low vs. high refractive index outlined below, but are rather defined by the relative difference in refractive index. For example, in one aspect a light trapping material can include silicon dioxide/silicon nitride/silicon dioxide, each material of which would be considered to be a low refractive index material. There is, however, a greater than 0.2 difference in the refractive indexes between silicon dioxide and silicon nitride, and thus such an isolation element would be included within the present scope. It is also noted that the light trapping material can have greater than three layers. As one non-limiting example, a material can have silicon dioxide/silicon nitride/polysilicon/silicon nitride/silicon dioxide.

As has been described, in some aspects a Bragg reflector can be utilized as an isolation element to trap electromagnetic radiation within the pixel. A Bragg reflector is a structure formed from multiple layers of alternating materials with varying refractive

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indexes, or by a periodic variation of some characteristic (e.g. height) of a dielectric waveguide, resulting in periodic variation in the effective refractive index in the guide. Each layer boundary causes a partial reflection of an optical wave. For waves whose wavelength is close to four times the optical thickness of the layers, the many reflections combine with constructive interference, and the layers act as a high-quality reflector. Thus the coherent super-positioning of reflected and transmitted light from multiple interfaces in the structure interfere so as to provide the desired reflective, transmissive, and absorptive behavior. In one aspect, a Bragg reflector can be made as in FIG. 2, whereby a high refractive index material sandwiched between two low refractive index materials. In one specific aspect, for example, the Bragg reflector can be constructed of a layer of polysilicon sandwiched between two layers of silicon dioxide. Because of the high refractive index difference between silicon and silicon dioxide, and the thickness of these layers, this structure can be fairly low loss even in regions where bulk silicon absorbs appreciably. Additionally, because of the large refractive index difference, the optical thickness of the entire layer set can be thinner, resulting in a broader-band behavior and fewer fabrications steps.

In terms of optical isolation from pixel to pixel, the large index of refraction mismatch can result in total reflection at the trench side walls. To prevent excessive dark current in the pixels, a passivation layer may be disposed on the side walls of the trench to prevent the generation of carriers and leakage current. Silicon nitride deposited over a thin grown oxide layer is also commonly used, in this case the oxide may be a low temperature grown plasma oxide.

It can be shown through calculations that a low recombination velocity of silicon oxide and silicon nitride is the result of moderately high positive oxide charge ($5x10^{11}$ to $1x10^{12}$ cm^{-2}) and relatively low midgap interface state density ($1x10^{10}$ to $4x10^{10}$ cm^{-2} eV^{-1}). The addition of silicon oxide or nitride can reduce surface recombination and surface generation. Reducing the surface recombination can increase quantum efficiency of photon collection and surface generation can cause excessive dark current in the imagers thereby reducing the quality of the image.

Since the positive oxide charge of silicon nitride or silicon oxynitride is relatively low on silicon on insulator imagers a p-type layer can be adjacent the silicon oxide,

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silicon oxynitride and/or silicon nitride layers as an alternative embodiment. In this case the p-type layer will accumulate the surface or the backside of the p-type silicon layer and p-type sidewalls.

Other possible passivation techniques include a hot steam anneal of hydrogenated silicon nitride or the use of amorphous silicon.

Aluminum oxide can also be deposited in the trench to form an isolating barrier. Aluminum oxide can have low stress, a negative fixed charge and higher index of refraction than silicon oxide or low stress silicon oxynitride nitride. Low surface recombination velocities, as low as 10 cm/s can be obtained through various deposition processes of Al_2O_3 layers on the silicon substrate. Low surface recombination can be achieved by field induced surface passivation due to a high density of negative charges stored at the interface. PECVD aluminum oxide is described here for the backside passivation of the backside and backside trenches in backside illuminated image sensors.

The index of refraction of the aluminum oxide can be increased slightly as required by the addition of other metallic elements to make ternary insulators like Aluminum Oxynitride (AlON), Hafnium Aluminum Oxide (HfAlO), Zirconium Aluminum Oxide (ZrAlO), Lanthanum Aluminum Oxide (LaAlO), Titanium Aluminum Oxide (TiAlO) or quaternary dielectrics like Hafnium Aluminum Oxynitride (HfAlON), Tantalum Aluminum Oxynitride (TaAlON), Lanthanum Aluminum Oxynitride (LaAlON).

Low temperature PECVD deposition processes are contemplated for the backside passivation of the backside and backside trenches in backside illuminated image sensors. As previously mentioned the large index of refraction mismatch between silicon and the insulators in the trenches results in reflection of the incident light and provides optical isolation. The trenches also provide electrical isolation. Additionally, it can also be beneficial to dope the sidewalls to create a surface field that will improve electrical isolation between the pixels. In one aspect, it can also be beneficial to dope the low refractive index material of the Bragg-type reflectors to increase such electrical isolation.

Returning to FIG. 2, layers the silicon oxide and polysilicon can optically and electrically isolate the adjacent pixels, as well as function to trap light within the pixel. While any thicknesses capable of forming such a reflector are considered to be within the

present scope, layer 216 can have a thickness in the range of from about 50 nm to about 500 nm. Layer 118 can have a thickness in the range of from about 5 nm to about 100 nm. Thus, the difference in refractive indexes and thickness can determine the intensity of the internal reflection of electromagnetic radiation. Notably, other materials such as metals, as well as other material not listed herein can be used to increase internal reflection of the light.

It is noted that, for the purposes of the present disclosure, in one aspect a low refractive index material can have a refractive index of less than about 2.1. In the case of the sandwiched materials, the two low refractive index materials can be the same or different materials having a refractive index of less than about 2.1. Non-limiting examples of low refractive index materials can include oxides, nitrides, oxynitrides, gasses, at least a partial vacuums, and the like, including appropriate combinations thereof. Non-limiting specific examples of such materials can include silicon oxide, silicon nitride, silicon oxynitride, and the like, including combinations thereof. Additionally, a high K dielectric material can also make a suitable low reflective index material due to their low refractive index properties and good dielectric properties, and as such, are considered to be within the present scope. One example is Hafnium oxide, which has a refractive index of about 1.9. Other examples of high K dielectrics include hafnium silicate, zirconium silicate, zirconium dioxide, and the like.

Additionally, in another aspect a high refractive index material can include a material having a refractive index of greater than or equal to about 2.1. Thus, in the case of the sandwiched materials, the high refractive index material disposed between the low refractive index materials has a refractive index of about 2.1 or greater. Non-limiting examples of high refractive index materials can include polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and the like, including appropriate combinations thereof.

In still another aspect of the present disclosure, a photosensitive imager having at least two pixels (302 and 304) and at least one trench isolation region 314 is shown in FIG. 3. The pixels can include a semiconductor substrate 306, having a first and second surface, 320 and 322 respectively; at least two doped regions 308 and 310, and a textured region 312 formed at least on the opposite side of the light incident surface (i.e. the

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second side 322). The textured region 312 can have surface features configured to reflect and disperse light. Further, the sidewalls can include a texture region 312 to increase the internal reflections of light. Regarding the isolation element 314 in FIG. 3, the isolation element can include several layers of materials that can passivate the sidewalls and each have a different index of refraction, as was described in FIG. 2. Further, a textured region 312 can be formed on the side walls of the isolation element(s) 314.

The present disclosure additionally provides pixels and imager devices, including imager arrays, which trap light therewithin. In one aspect as is shown in FIG. 4, for example, a light trapping pixel device can include a light sensitive pixel or device 402 having a light incident surface 420, a backside surface 422 opposite the light incident surface 420, and a peripheral sidewall 424 disposed into at least a portion of the pixel 402 and extending at least substantially around the pixel periphery. It is noted that the pixel sidewall is also known as a trench. The pixel can also include a backside light trapping material 426 substantially covering, partially covering, or completely covering the backside surface 422. A peripheral light trapping material 428 can be substantially covering, partially covering, or completely covering the peripheral sidewall 424. As such, light contacting the backside light trapping material 426 or the peripheral light trapping material 428 is reflected back toward the pixel 402. Also shown in FIG. 4 are at least two doped regions 408 and 410 and an optional textured region 412. It is noted that, in addition to a single pixel as shown, pixel arrays are also contemplated and are to be included in the present scope.

The light trapping materials of FIG. 4 can be as described above, either single or multiple layer structures. In one aspect, for example, at least one of the backside light trapping material 426 and the peripheral light trapping material 428 includes a high refractive index material sandwiched between two low refractive index materials. In another aspect, the backside light trapping material 426 and the peripheral light trapping material 428 includes a high refractive index material sandwiched between two low refractive index materials. It is noted that these light trapping materials are shown in FIG. 4 as a single layer for clarity, and that multiple layers are contemplated. Furthermore, the peripheral sidewall can extend for a portion, a substantial portion, or completely around the pixel periphery. Additionally, as has been described herein, the

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peripheral sidewall can extend partially into the pixel, substantially through the pixel, or completely through the pixel to the backside surface. Thus, both deep and shallow trenches are contemplated.

In another aspect, as is shown in FIG. 5, a pixel 502 can include a frontside light trapping material 530 that at least partially covers, substantially covers, or completely covers the light incident surface 520. The frontside light trapping material 530 can be multiple layer of materials have a variety of properties and uses, including passivation, antireflection, light trapping, and the like, including combinations thereof. Note that numerical indicators in FIG. 5 from previous figures are intended to reflect the previous descriptions for those elements, and as such, reference is made to FIG. 4.

In another aspect, as is shown in FIG. 6, a pixel 602 can include a frontside light trapping material 632 associated with the light incident surface 620 that is an internal reflective layer having an aperture 634 to allow entry of light 690 into the pixel 602. The frontside light trapping material 632 is thus operable to reflect light impinging thereupon from inside the pixel 602 back into the pixel. Additionally, in some aspects a lens 636 can be functionally coupled to the aperture 634 to focus incident light 690 through the aperture 634 and into the pixel 602. The effective surface area of the aperture compared to the frontside surface area of the pixel can vary depending on the design of the device and the presence, absence, or particular properties of a lens. In one aspect, however, the aperture can be large enough to accept and trap incoming light to a degree that increases the efficiency of the pixel. In one specific aspect, the aperture has an effective surface area of less than about 90% of the incident light surface total surface area. It is noted that various elements such as the doped regions and the optional textured layer are not shown in FIG. 6 for clarity. Furthermore, numerical indicators in FIG. 6 from previous figures are intended to reflect the previous descriptions for those elements, and as such, reference is made to FIG. 4.

The frontside light trapping material can be made of a variety of materials including metals as have been described herein with respect to other light trapping materials. As such, any material that can be applied to the light incident surface and that is internally reflective toward the inside of the pixel is considered to be within the present scope. Thus, the aforementioned pixel is reflective on 6 internal sides, and as such, light

entering the pixel that is not absorbed will interact with and be reflected internally be either the backside, peripheral sidewall, or frontside light trapping materials. Light is thus effectively maintained inside the pixel until it is absorbed.

In another aspect of the present disclosure, a method of making a light trapping pixel device is provided. Such a method can include, as is shown in FIG. 7, 702 forming a pixel by: 704 forming a backside light trapping material on a semiconductor layer, the backside light trapping material including a high refractive index material sandwiched between two low refractive index materials, and 706 forming a pixel device layer on the semiconductor layer opposite the light trapping material. The method can additionally include 708 etching a trench circumscribing the pixel device layer and 710 filling the trench with a light trapping material. Further details regarding the wafer bonding and wafer-bonded structures described can be found in copending US Application Serial No. 13/069,135, filed on March 22, 2011, which is incorporated herein by reference.

The formation of the backside light trapping material can be accomplished by a variety of techniques, all of which are considered to be within the present scope. In one aspect, for example, depositing a first low refractive index material onto the semiconductor layer, bonding the first low refractive index material to a high refractive index material having a second low refractive index material coupled thereto such that the high refractive index material is sandwiched in between the first and second low refractive index materials. In some cases the second low refractive index material can be coupled to a carrier wafer. In another aspect, the first low refractive index can be deposited onto the semiconductor layer followed by deposition of the high refractive index material and then the second low refractive index material. In another aspect, the layered structure can be formed on a carrier wafer, and the outermost low refractive index material can then be bonded to the semiconductor layer. The carrier wafer can then be optionally removed. In yet another aspect, the first refractive index material can be deposited onto the semiconductor layer, the second refractive index material can be deposited onto a carrier wafer, and the high refractive index material can be deposited onto either the first or second refractive index material, followed by bonding of the structure together.

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As has been described, the trench can be a shallow trench or a deep trench. In one aspect, however, etching the trench circumscribing the pixel device layer can further include etching the trench to a depth that contacts at least the first low refractive index material. Furthermore, the method can also include applying an incident light trapping material to the pixel device layer.

In some aspects the various trenches can be filled with a material, or they can be gas filled or have a partial vacuum applied thereto. For those aspects whereby the trenches will be filled in with a non-gas material, a variety of deposition techniques are contemplated and all are considered to be within the present scope. In one aspect, however, the trench can be filled with a high refractive index material and a low refractive index material in a sandwich structure as has been described. In one exemplary technique, the filling of the trench with such light trapping material can include depositing a low refractive index material into the trench to fill a portion of the trench from the trench walls inward, ceasing deposition of the low refractive index material to leave an internal space within the trench, and depositing a high refractive index material into the trench to fill the internal space. As such, the sandwiched layer of low-high-low refractive index materials is thus created in the trench.

In another aspect, the method can also include forming a textured region on at least a portion of the semiconductor layer between the semiconductor layer and the first low refractive index prior to depositing the first low refractive index material onto the semiconductor layer. Non-limiting examples of texture formation techniques can include plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof. In one specific aspect, the textured region includes laser texturing.

A device design having a textured region located on, for example, the back surface of a photodetector, provides significant performance benefits. The textured region can have surface features that can lead to higher recombination of photocarriers for short wavelengths (e.g. in the blue green part of the spectrum) due to the very shallow penetration of those wavelengths into the detecting volume of the device. By physically locating the textured on the back surface of the device, a pristine surface is provided for the collection of short wavelengths on the top surface (i.e. the light incident surface), and

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the longer wavelengths that penetrate deep into or through the detecting region of the semiconductor material are collected by or with the help of the textured region opposite the light incident surface.

The textured region can be of various thicknesses, depending on the desired use of the material. In one aspect, for example, the textured region has a thickness of from about 500 nm to about 100 μm. In another aspect, the textured region has a thickness of from about 500 nm to about 15 μm. In yet another aspect, the textured region has a thickness of from about 500 nm to about 2 μm. In a further aspect, the textured region has a thickness of from about 500 nm to about 1 μm. In another aspect, the textured region has a thickness of from about 200 nm to about 2 μm.

The textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and/or to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device. The textured region can include surface features to further increase the effective absorption length of the device. Non-limiting examples of shapes and configurations of surface features include cones, pillars, pyramids, micolenses, quantum dots, inverted features, gratings, protrusions, sphere-like structures, and the like, including combinations thereof. Additionally, surface features can be micron-sized, nano-sized, or a combination thereof. For example, cones, pyramids, protrusions, and the like can have an average height within this range. In one aspect, the average height would be from the base of the feature to the distal tip of the feature. In another aspect, the average height would be from the surface plane upon which the feature was created to the distal tips of the feature. In one specific aspect, a feature (e.g. a cone) can have a height of from about 50 nm to about 2 μm. As another example, quantum dots, microlenses, and the like can have an average diameter within the micron-sized and/or nano-sized range.

In addition to or instead of surface features, the textured region can include a textured film layer. In one aspect, for example, the textured region can include a substantially conformal textured film layer. Such a textured film layer can have an average thickness of from about 1 nm to about 20 μm. In those aspects where the textured region includes surface features, the conformal textured film layer can have a varying thickness relative to the location on the surface features upon which is deposited.

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In the case of cones, for example, the conformal textured film layer can become thinner toward the tips of the cones. Such a conformal film layer can include various materials, including, without limitation, SiO_2, Si_3N_4, amorphous silicon, polysilicon, a metal or metals, and the like, including combinations thereof. The conformal textured film layer can also be one or more layers of the same or different materials, and can be formed during the creation of surface features or in a separate process.

Textured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared). Such internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor layer. This increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.

The texturing process can texture the entire substrate to be processed or only a portion of the substrate. In one aspect, for example, a substrate such as the semiconductor layer can be textured and patterned by an appropriate technique over an entire surface to form the texture region. In another aspect, a substrate such as the semiconductor layer can be textured and patterned across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch or a laser process to define a specific structure or pattern.

In addition to surface features, the textured region can have a surface morphology that is designed to focus or otherwise direct electromagnetic radiation. For example, in one aspect the textured region has a surface morphology operable to direct electromagnetic radiation into the semiconductor layer. Non-limiting examples of various surface morphologies include sloping, pyramidal, inverted pyramidal, spherical, square, rectangular, parabolic, asymmetric, symmetric, and the like, including combinations thereof.

The textured region, including surface features as well as surface morphologies, can be formed by various techniques, including plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, selective epitaxial growth, and the like.

One effective method of producing a textured region is through laser processing. Such laser processing allows discrete target areas of a substrate to be textured, as well as entire surfaces. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope. Laser treatment or processing can allow, among other things, enhanced absorption properties and thus increased electromagnetic radiation focusing and detection.

In one aspect, for example, a target region of the substrate to be textured can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Patents 7,057,256, 7,354,792 and 7,442,629, which are incorporated herein by reference in their entireties. Briefly, a surface of a substrate material is irradiated with laser radiation to form a textured or surface modified region. Such laser processing can occur with or without a dopant material. In those aspects whereby a dopant is used, the laser can passed through a dopant carrier and onto the substrate surface. In this way, dopant from the dopant carrier is introduced into the target region of the substrate material. Such a region incorporated into a substrate material can have various benefits in accordance with aspects of the present disclosure. For example, the textured region typically has a textured surface that increases the surface area and increases the probability of radiation absorption. In one aspect, such a textured region is a substantially textured surface including micron-sized and/or nano-sized surface features that have been generated by the laser texturing. In another aspect, irradiating the surface of a substrate material includes exposing the laser radiation to a dopant such that irradiation incorporates the dopant into the substrate. Various dopant materials are known in the art, and are discussed in more detail herein.

Thus the surface of the substrate at the target region is thus chemically and/or structurally altered by the laser treatment, which may, in some aspects, result in the formation of surface features appearing as structures or patterned areas on the surface and, if a dopant is used, the incorporation of such dopants into the substrate material. In some aspects, the features or structures can be on the order of 50 nm to 20 μm in size and can assist in the absorption of electromagnetic radiation. In other words, the textured surface can increase the probability of incident radiation being absorbed.

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A variety of semiconductor materials are contemplated for use with the pixel devices and methods according to aspects of the present disclosure. Such materials can be utilized as the semiconductor layer and/or the semiconductor substrate, as well as for the secondary semiconductor layer and the epitaxially grown semiconductor layer. Non-limiting examples of such semiconductor materials can include group IV materials, compounds and alloys comprised of materials from groups II and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can include silicon carbide (SiC) and silicon germanium (SiGe). In one specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum gallium arsenide, and combinations thereof.

Exemplary combinations of group II-VI materials can include cadmium selenide (CdSe), cadmium sulfide (CdS), cadmium telluride (CdTe), zinc oxide (ZnO), zinc selenide (ZnSe), zinc sulfide (ZnS), zinc telluride (ZnTe), cadmium zinc telluride (CdZnTe, CZT), mercury cadmium telluride (HgCdTe), mercury zinc telluride (HgZnTe), mercury zinc selenide (HgZnSe), and combinations thereof.

Exemplary combinations of group III-V materials can include aluminum antimonide (AlSb), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum phosphide (AlP), boron nitride (BN), boron phosphide (BP), boron arsenide (BAs), gallium antimonide (GaSb), gallium arsenide (GaAs), gallium nitride (GaN), gallium phosphide (GaP), indium antimonide (InSb), indium arsenide (InAs), indium nitride (InN), indium phosphide (InP), aluminum gallium arsenide (AlGaAs, $Al_xGa_{1-x}As$), indium gallium arsenide (InGaAs, $In_xGa_{1-x}As$), indium gallium phosphide (InGaP), aluminum indium arsenide (AlInAs), aluminum indium antimonide (AlInSb), gallium arsenide nitride (GaAsN), gallium arsenide phosphide (GaAsP), aluminum gallium nitride (AlGaN), aluminum gallium phosphide (AlGaP), indium gallium nitride (InGaN),

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indium arsenide antimonide (InAsSb), indium gallium antimonide (InGaSb), aluminum gallium indium phosphide (AlGaInP), aluminum gallium arsenide phosphide (AlGaAsP), indium gallium arsenide phosphide (InGaAsP), aluminum indium arsenide phosphide (AlInAsP), aluminum gallium arsenide nitride (AlGaAsN), indium gallium arsenide nitride (InGaAsN), indium aluminum arsenide nitride (InAlAsN), gallium arsenide antimonide nitride (GaAsSbN), gallium indium nitride arsenide antimonide (GaInNAsSb), gallium indium arsenide antimonide phosphide (GaInAsSbP), and combinations thereof.

The semiconductor material can be of any thickness that allows the desired property or functionality of the semiconductor device, and thus any such thickness of semiconductor material is considered to be within the present scope. The textured region can increase the efficiency of the device such that, in some aspects, the semiconductor material can be thinner than has previously been possible. Decreasing the thickness reduces the amount of semiconductor material used to make such a device. In one aspect, for example, a semiconductor material such as the semiconductor layer has a thickness of from about 500 nm to about 50 μm. In another aspect, the semiconductor material has a thickness of less than or equal to about 500 μm. In yet another aspect, the semiconductor material has a thickness of from about 1 μm to about 10 μm. In a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 750 μm. In yet a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 100 μm.

Additionally, various configurations of semiconductor materials are contemplated, and any such material configuration that can be incorporated into a semiconductor device is considered to be within the present scope. In one aspect, for example, the semiconductor material can include monocrystalline materials. In another aspect, the semiconductor material can include multicrystalline materials. In yet another aspect, the semiconductor material can include microcrystalline materials. It is also contemplated that the semiconductor material can include amorphous materials.

As has been described, the semiconductor substrate can be of any size, shape, and material capable of supporting the semiconductor layer and associated components during manufacture and/or use. The semiconductor substrate can be made from various

materials, including the semiconductor materials described above, as well as non-semiconductor materials. Non-limiting examples of such materials can include metals, polymeric materials, ceramics, glass, and the like. In some aspects, the semiconductor substrate and the semiconductor layer have the same or substantially the same thermal expansion properties.

Furthermore, the semiconductor material according to aspects of the present disclosure can comprise multiple layers. In some aspects, layers can vary in majority carrier polarity (i.e. donor or acceptor impurities). The donor or acceptor impurities are typically determined by the type of dopant/impurities introduced into the device either through a growth process, deposition process, epitaxial process, implant process, lasing process or other known process to those skilled in the art. In some aspects such semiconductor materials can include an n-type layer, an intrinsic (i-type) layer, and a p-type layer, thus forming a p-i-n semiconductor material stack that creates a junction and/or depletion region. A semiconductor material devoid of an i-type layer is also contemplated in accordance with the present disclosure. In other aspects the semiconductor material may include multiple junctions. Additionally, in some aspects, variations of n(--), n(-), n(+), n(++), p(--), p(-), p(+), or p(++) type semiconductor layers can be used. The minus and positive signs are indicators of the relative magnitude of the doping of the semiconductor material.

A variety of dopant materials are contemplated for both the formation of doped regions in the semiconductor layer and for doping of the textured region, and any dopant that can be used in such processes to modify a material is considered to be within the present scope. It should be noted that the particular dopant utilized can vary depending on the material being doped, as well as the intended use of the resulting material.

A dopant can be either a charge donating or a charge accepting dopant species. More specifically, an electron donating or a hole donating species can cause a region to become more positive or negative in polarity as compared to the substrate upon which the rests. In one aspect, for example, the doped region can be p-doped. In another aspect the doped region can be n-doped.

In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof. It should be noted that the

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scope of dopant materials should include, not only the dopant materials themselves, but also materials in forms that deliver such dopants (i.e. dopant carriers). For example, S dopant materials includes not only S, but also any material capable being used to dope S into the target region, such as, for example, H_2S, SF_6, SO_2, and the like, including combinations thereof. In one specific aspect, the dopant can be S. Sulfur can be present at an ion dosage level of from about 5×10^{14} to about 3×10^{20} ions/cm^2. Non-limiting examples of fluorine-containing compounds can include ClF_3, PF_5, F_2 SF_6, BF_3, GeF_4, WF_6, SiF_4, HF, CF_4, CHF_3, CH_2F_2, CH_3F, C_2F_6, C_2HF_5, C_3F_8, C_4F_8, NF_3, and the like, including combinations thereof. Non-limiting examples of boron-containing compounds can include $B(CH_3)_3$, BF_3, BCl_3, BN, $C_2B_{10}H_{12}$, borosilica, B_2H_6, and the like, including combinations thereof. Non-limiting examples of phosphorous-containing compounds can include PF_5, PH_3, $POCl_3$, P_2O_5, and the like, including combinations thereof. Non-limiting examples of chlorine-containing compounds can include Cl_2, SiH_2Cl_2, HCl, $SiCl_4$, and the like, including combinations thereof. Dopants can also include arsenic-containing compounds such as AsH_3 and the like, as well as antimony-containing compounds. Additionally, dopant materials can include mixtures or combinations across dopant groups, i.e. a sulfur-containing compound mixed with a chlorine-containing compound. In one aspect, the dopant material can have a density that is greater than air. In one specific aspect, the dopant material can include Se, H_2S, SF_6, or mixtures thereof. In yet another specific aspect, the dopant can be SF_6 and can have a predetermined concentration range of about 5.0×10^{-8} mol/cm^3 to about 5.0×10^{-4} mol/cm^3. As one non-limiting example, SF_6 gas is a good carrier for the incorporation of sulfur into a substrate via a laser process without significant adverse effects on the material. Additionally, it is noted that dopants can also be liquid solutions of n-type or p-type dopant materials dissolved in a solution such as water, alcohol, or an acid or basic solution. Dopants can also be solid materials applied as a powder or as a suspension dried onto the wafer.

In another aspect, the band structure optimization can be realized by forming a heterojunction along a modified semiconductor interface. For example, a layer of amorphous silicon can be deposited on the textured region interface, thus forming a heterojunction that bends the minority carrier band towards the desired energy direction.

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CLAIMS

What is claimed is:

1. A light trapping device, comprising:

at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

a backside light trapping material substantially covering the backside surface; and

a peripheral light trapping material substantially covering the peripheral sidewall;

wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

2. The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.

3. The device of claim 1, wherein the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.

4. The device of claim 3, wherein the two low refractive index materials have a refractive index of less than about 2.1.

5. The device of claim 4, wherein at least one of the two low refractive index material includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.

6. The device of claim 4, wherein the at least one of the two low refractive index materials includes a member selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.

7. The device of claim 3, wherein the high refractive index material includes a material having a refractive index of greater than or equal to about 2.1.

8. The device of claim 7, wherein the high refractive index material includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and combinations thereof.

9. The device of claim 2, wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field.

10. The device of claim 9, wherein the dopant is boron or antimony.

11. The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials, and wherein the difference in refractive index between the first material and the two second materials is at least 0.2.

12. The device of claim 1, wherein the peripheral sidewall extends completely around the pixel periphery.

13. The device of claim 1, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

14. The device of claim 1, further comprising a frontside light trapping material at least partially covering the light incident surface.

15. The device of claim 14, wherein the frontside light trapping material is an antireflective layer coating.

16. The device of claim 14, wherein the frontside light trapping material is a reflective layer having an aperture to allow entry of light into the pixel, wherein the reflective layer is operable to reflect light impinging thereupon from inside the pixel back into the pixel.

17. The device of claim 16, further comprising a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.

18. The device of claim 16, wherein the aperture has an effective surface area of _____ % of the incident light surface total surface area.

19. The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

20. The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface.

21. The device of claim 1, further comprising a textured layer positioned to interact with light proximal to the backside surface.

22. The device of claim 21, wherein the textured layer is located between the backside surface and the backside light trapping material.

23. An array of light trapping pixel devices of claim 1.

24. A substantially light trapping device, comprising:

at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending from the light incident surface to the backside surface and extending around the pixel periphery;

a backside light trapping material substantially covering the backside surface;

a peripheral light trapping material substantially covering the peripheral sidewall; and

an internally reflective frontside light trapping material covering at least a portion of the light incident surface operable allow entrance of light into the pixel and operable to reflect light impinging thereupon from inside the pixel back into the pixel, and wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

25. The device of claim 24, wherein the internally reflective frontside light trapping material includes an aperture to allow entry of light into the pixel.

26. The device of claim 25, further comprising a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.

27. A method of making a light trapping device, comprising:

forming a pixel by:

forming a backside light trapping material on a semiconductor layer, the backside light trapping material including a high refractive index material sandwiched between two low refractive index materials; and

forming a pixel device layer on the semiconductor layer opposite the light trapping material;

etching a trench circumscribing the pixel device layer; and

filling the trench with a peripheral light trapping material.

28. The method of claim 27, wherein etching the trench circumscribing the pixel device layer can further include etching the trench to a depth that contacts at least the backside light trapping material.

29. The method of claim 27, further comprising applying an incident light trapping material to the pixel device layer.

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30. The method of claim 27, wherein filling the trench with the peripheral light trapping material further includes:

depositing a low refractive index material into the trench to fill a portion of the trench from the trench walls inward;

ceasing deposition of the low refractive index material to leave an internal space within the trench; and

depositing a high refractive index material into the trench to fill the internal space.

31. The method of claim 27, further comprising forming a textured region on at least a portion of the semiconductor layer between the semiconductor layer and the backside light trapping material.

32. The method of claim 31, wherein forming the textured region includes a technique selected from the group consisting of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.

33. The method of claim 32, wherein forming the textured region includes laser texturing.

ABSTRACT OF THE DISCLOSURE

Light trapping pixels, devices incorporating such pixels, and various associated methods are provided. In one aspect, for example, a light trapping pixel device can include a light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery. The pixel can also include a backside light trapping material substantially covering the backside surface and a peripheral light trapping material substantially covering the peripheral sidewall. The light contacting the backside light trapping material or the peripheral light trapping material is thus reflected back toward the pixel.

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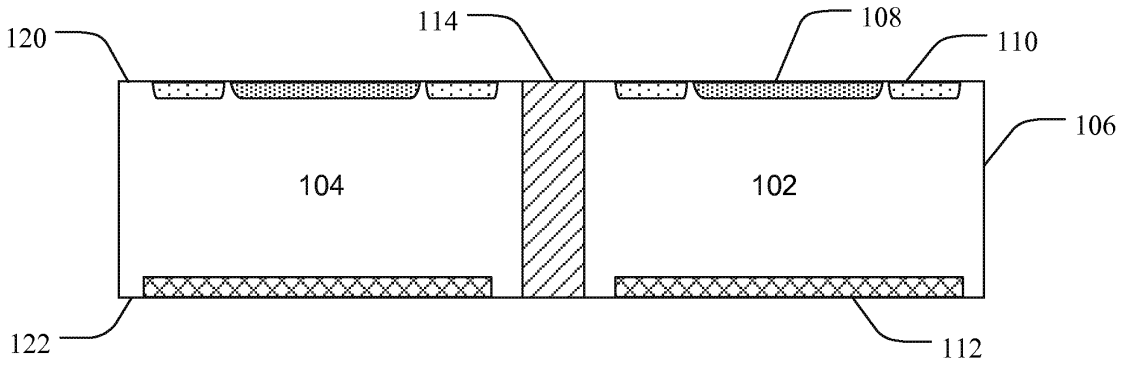

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FIG. 1

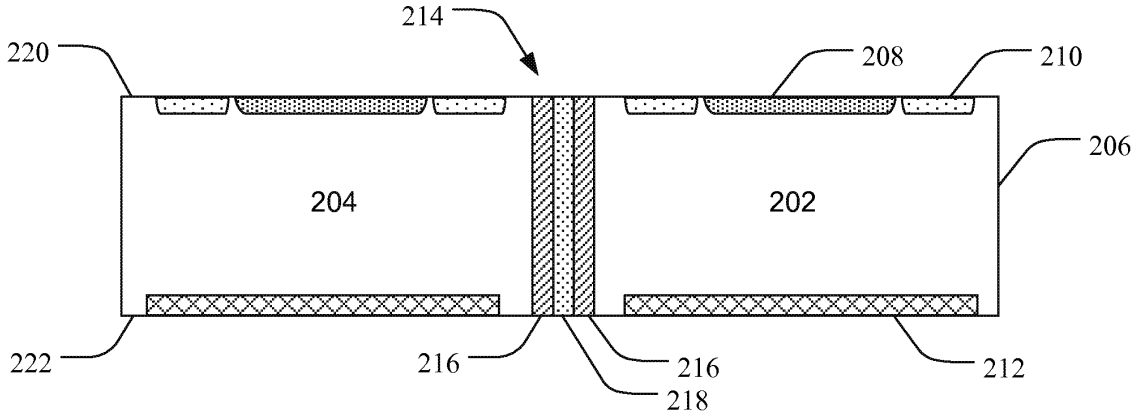

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FIG. 2

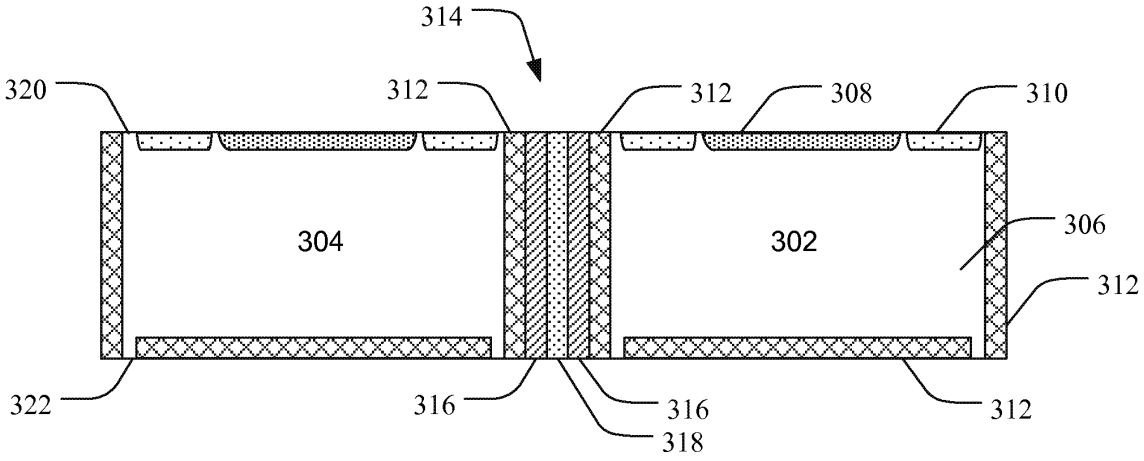


FIG. 3

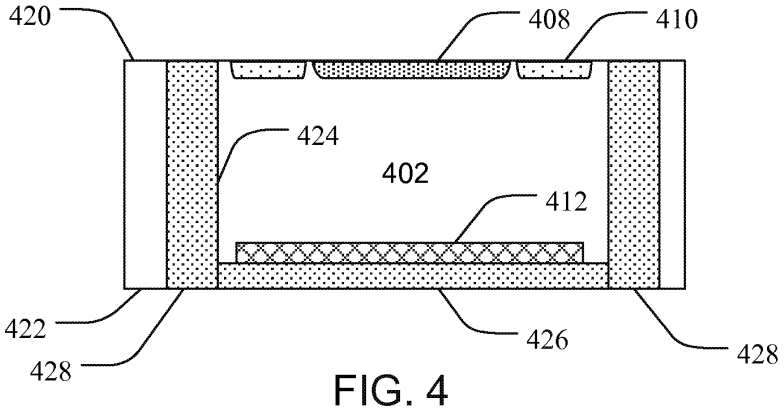


FIG. 4

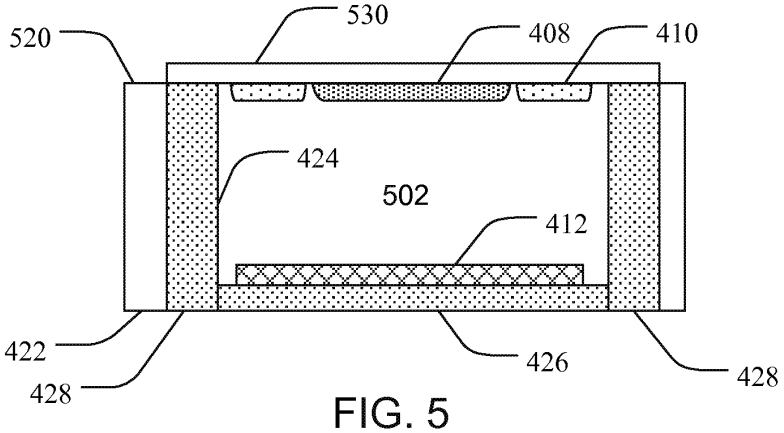


FIG. 5

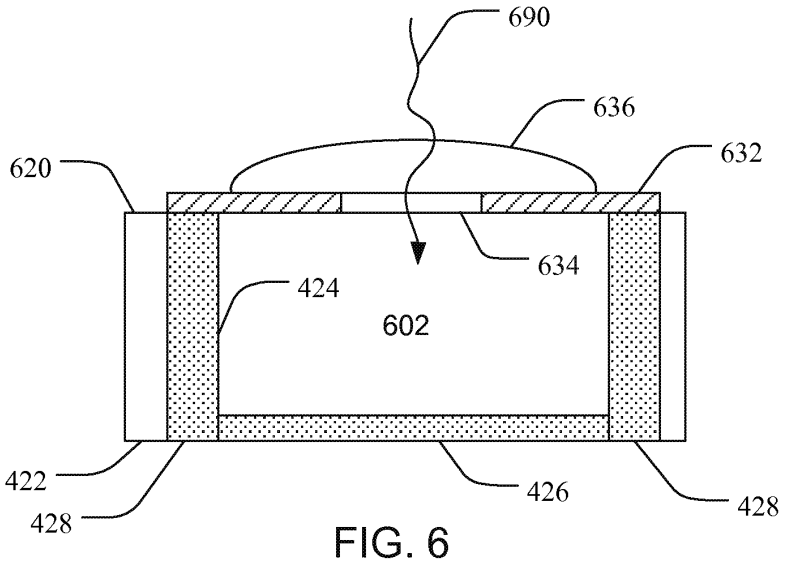


FIG. 6

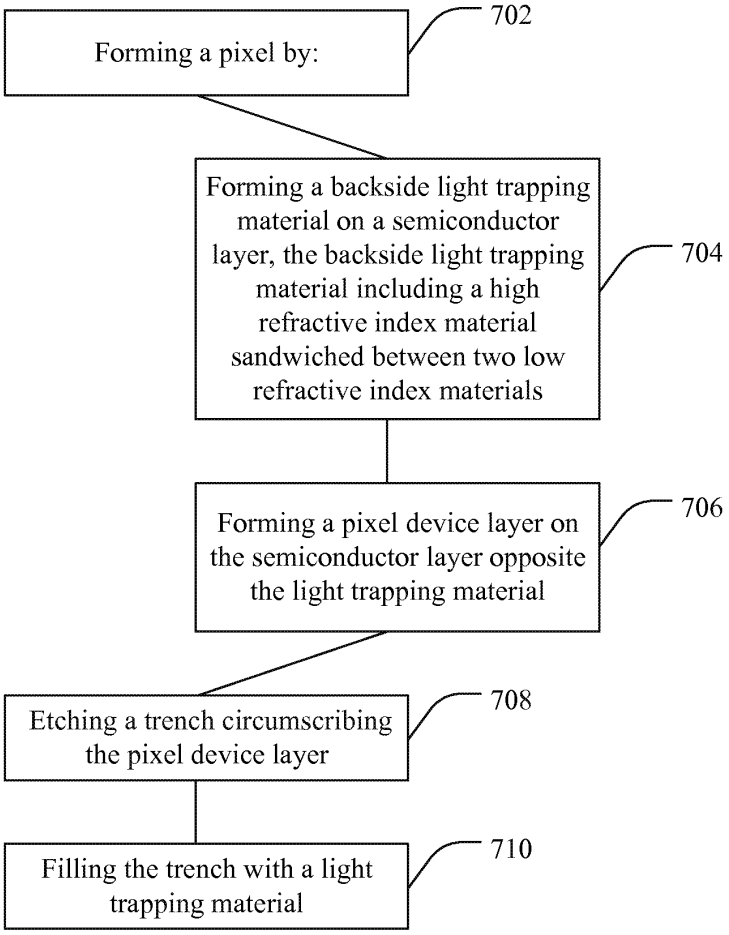

Forming a pixel by:
702
Forming a backside light trapping material on a semiconductor layer, the backside light trapping material including a high refractive index material sandwiched between two low refractive index materials
704
Forming a pixel device layer on the semiconductor layer opposite the light trapping material
706
Etching a trench circumscribing the pixel device layer
708
Filling the trench with a light trapping material
710

FIG. 7

Docket Number: 3035-052.NP

Substitute Form PTO/AIA/01

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	Pixel Isolation Elements, Devices and Associated Methods

As the below named inventor, I hereby declare that:

This declaration Is directed to:

☐ The attached application or,

☑ United States application or PCT international application number 13/841,120 filed on 3/15/2013.

The above-identified application was made or authorized to be made by me.

I have reviewed and understand the contents of the above-identified application, including the claims. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

LEGAL NAME OF INVENTOR

Inventor: Martin U. Pralle Date (Optional): 4/3/14

Signature:

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

Docket Number: **3035-052.NP** Substitute Form PTO/AIA/01

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I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

LEGAL NAME OF INVENTOR

Inventor: Jeffrey McKee Date (Optional): 4-7-14

Signature: _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

Docket Number: 3035-052.NP

Substitute Form PTO/AIA/01

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LEGAL NAME OF INVENTOR

Inventor: Jason Sickler Date (Optional): 4/3/2014

Signature:

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

Electronic Acknowledgement Receipt

EFS ID:	22718168
Application Number:	14747875
International Application Number:	
Confirmation Number:	1722
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	20551
Filer:	Todd Brent Alder/Nicole Solomon
Filer Authorized By:	Todd Brent Alder
Attorney Docket Number:	3035-052.NP.CON
Receipt Date:	23-JUN-2015
Filing Date:	
Time Stamp:	17:59:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	3035-052_NP_CON_ADS.pdf	1265255 4696d2e70b8f0e22de389a3385fe855bb76c37fc	no	7

Warnings:	
Information:	

2		3035-052_NP_CON_Application.PDF	170874 a003a27b8aed66f2b326cd5e7e07caba1969476c	yes	32

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Specification	1	26
Claims	27	31
Abstract	32	32

Warnings:					
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3	Drawings-only black and white line drawings	3035-052_NP_CON_Drawings.pdf	70273 c0ac70f369d3cad25a87aa1778fb99861fc4cd27	no	4
Warnings:					
Information:					
4	Oath or Declaration filed	3035-052_NP_CON-Declarations.pdf	626449 d63c72dabdb5a12ec99281fc844b468ae2d7c09b	no	3
Warnings:					
Information:					
		Total Files Size (in bytes):	2132851		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/747,875	06/23/2015	2852	0.00	3035-052.NP.CON	33	3

CONFIRMATION NO. 1722

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

FILING RECEIPT

OC000000078105579

Date Mailed: 07/07/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Martin U. Pralle, Wayland, MA;
Jeffrey McKee, Tualatin, OR;
Jason Sickler, Arlington, MA;

Applicant(s)

SiOnyx, Inc., Beverly, MA;

Assignment For Published Patent Application

SiOnyx, Inc., Beverly, MA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 13/841,120 03/15/2013 PAT 9064764
which claims benefit of 61/614,275 03/22/2012

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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If Required, Foreign Filing License Granted: 07/06/2015
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/747,875**

SAMSUNG EX. 1002 - 50/4148

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****
Title

Pixel Isolation Elements, Devices and Associated Methods

Preliminary Class

396

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

SAMSUNG EX. 1002 - 51/4148

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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SAMSUNG EX. 1002 - 52/4148

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/747,875

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	33 minus 20 =	* 13	x 40 =	520	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*	x 210 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	1250		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/747,875	06/23/2015	Martin U. Pralle	3035-052.NP.CON

CONFIRMATION NO. 1722

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

FORMALITIES LETTER

OC000000076105580

Date Mailed: 07/07/2015

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Additional claim fees of $ **520** as a small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. Small entity discount is in effect. If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **70** basic filing fee.
- $ **70** surcharge.
- $ **300** search fee.
- $ **360** examination fee.
- $ **520** for **13** total claims over 20.

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- $(**0**) previous unapplied payment amount.
- $ **1320** TOTAL FEE BALANCE DUE.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

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For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/mhteklu/

SAMSUNG EX. 1002 - 55/4148

To: patentdocket@tnw.com,rich@tnw.com,annette.fields@tnw.com
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 20551

Jul 07, 2015 05:27:47 AM

Dear PAIR Customer:

THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 20551 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

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Application	Document	Mailroom Date	Attorney Docket No.
14747875	APP.FILE.REC	07/07/2015	3035-052.NP.CON
	NTC.MISS.PRT	07/07/2015	3035-052.NP.CON

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Thank you for prompt attention to this notice,

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PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ART UNIT:	2852
EXAMINER:	n/a
FIRST NAMED INVENTOR:	Martin U. Pralle
SERIAL NO.:	14/747,875
FILED:	06/23/2015
CONF. NO.:	1722
FOR:	Pixel Isolation Elements, Devices and Associated Methods
DOCKET NO.:	3035-052.NP.CON

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8

DATE OF DEPOSIT: September 8, 2015

I hereby certify that this paper or fee (along with any paper or fee referred to as being attached or enclosed) is being submitted on the date indicated above via:

- ☒ EFS Web
- ☐ facsimile to _____
- ☐ the United States Postal Service with sufficient postage as first class mail addressed to: Mail Stop _____, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

/Nicole Solomon/
Nicole Solomon

THORPE NORTH & WESTERN, LLP
Customer No. 20,551
P.O. Box 1219
Sandy, Utah 84091-1219

PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant offers the following Preliminary Amendment to accompany application serial number 14/747,875, and requests consideration thereof.

SAMSUNG EX. 1002 - 57/4148

AMENDMENT TO THE CLAIMS

Please amend the claims as follows:

1. (currently amended) A light trapping device, comprising:

at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

a backside light trapping material substantially covering the backside surface; and

a peripheral light trapping material substantially covering the peripheral sidewall,~~;~~

wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

2. (original) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.

3. (original) The device of claim 1, wherein the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.

4. (original) The device of claim 3, wherein the two low refractive index materials have a refractive index of less than about 2.1.

5. (original) The device of claim 4, wherein at least one of the two low refractive index material includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.

6. (original) The device of claim 4, wherein the at least one of the two low refractive index materials includes a member selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.

SAMSUNG EX. 1002 - 58/4148

7. (original) The device of claim 3, wherein the high refractive index material includes a material having a refractive index of greater than or equal to about 2.1.

8. (original) The device of claim 7, wherein the high refractive index material includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and combinations thereof.

9. (original) The device of claim 2, wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field.

10. (original) The device of claim 9, wherein the dopant is boron or antimony.

11. (original) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials, and wherein the difference in refractive index between the first material and the two second materials is at least 0.2.

12. (original) The device of claim 1, wherein the peripheral sidewall extends completely around the pixel periphery.

13. (original) The device of claim 1, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

14. (original) The device of claim 1, further comprising a frontside light trapping material at least partially covering the light incident surface.

15. (original) The device of claim 14, wherein the frontside light trapping material is an antireflective layer coating.

16. (original) The device of claim 14, wherein the frontside light trapping material is a reflective layer having an aperture to allow entry of light into the pixel, wherein the reflective

layer is operable to reflect light impinging thereupon from inside the pixel back into the pixel.

17. (original) The device of claim 16, further comprising a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.

18. (canceled)

19. (original) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

20. (original) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface.

21 - 33. (canceled)

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SAMSUNG EX. 1002 - 60/4148

REMARKS

Applicant expresses appreciation to Examiner for consideration of the subject patent application. This Preliminary Amendment accompanies application serial number - 14/747,875. Claims 1-33 were originally presented. Claim 1 has been amended to correct a typographical error. Claims 18 and 21-33 have been canceled. Accordingly, Applicants submit that no new matter has been added.

SAMSUNG EX. 1002 - 61/4148

CONCLUSION

If any impediment to examination is found after consideration of the above-recited remarks that could be removed during a telephone interview, Examiner is invited to telephone the undersigned attorney at (801) 566-6633 so that such issues may be resolved as expeditiously as possible.

The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 20-0100.

DATED this 8th day of September, 2015.

Respectfully submitted,

THORPE, NORTH & WESTERN, LLP

/Todd B. Alder/

Todd B. Alder
Reg. No. 54,598
8180 South 700 East, Suite 350
Sandy, UT 84070
Telephone: (801) 566-6633
Facsimile: (801) 566-0750

Electronic Patent Application Fee Transmittal

Application Number:	14747875
Filing Date:	23-Jun-2015
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Filer:	Todd Brent Alder/Nicole Solomon
Attorney Docket Number:	3035-052.NP.CON

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	70	70
Utility Search Fee	2111	1	300	300
Utility Examination Fee	2311	1	360	360
Pages:				
Claims:				
Miscellaneous-Filing:				
Late Filing Fee for Oath or Declaration	2051	1	70	70
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**800**

Electronic Acknowledgement Receipt	
EFS ID:	23432810
Application Number:	14747875
International Application Number:	
Confirmation Number:	1722
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	20551
Filer:	Todd Brent Alder/Nicole Solomon
Filer Authorized By:	Todd Brent Alder
Attorney Docket Number:	3035-052.NP.CON
Receipt Date:	08-SEP-2015
Filing Date:	23-JUN-2015
Time Stamp:	18:49:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$800
RAM confirmation Number	7026
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		3035-052_NP_CON_Prel_Amend.pdf	66774 082ffd77b10a483d22958ef23cede575d191c3d5	yes	6

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Preliminary Amendment	1	1
Claims	2	4
Applicant Arguments/Remarks Made in an Amendment	5	6

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	36960 d73cc24c9310b1724e0af8b6a8302e336597248e	no	2

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Total Files Size (in bytes):	103734

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/747,875	06/23/2015	2852	800	3035-052.NP.CON	19	1

CONFIRMATION NO. 1722

UPDATED FILING RECEIPT

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

OC000000077485336

Date Mailed: 09/18/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Martin U. Pralle, Wayland, MA;
Jeffrey McKee, Tualatin, OR;
Jason Sickler, Arlington, MA;

Applicant(s)

SiOnyx, Inc., Beverly, MA;

Assignment For Published Patent Application

SiOnyx, Inc., Beverly, MA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 13/841,120 03/15/2013 PAT 9064764
which claims benefit of 61/614,275 03/22/2012

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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If Required, Foreign Filing License Granted: 07/06/2015
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/747,875**

SAMSUNG EX. 1002 - 67/4148

Projected Publication Date: 12/24/2015

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****
Title

Pixel Isolation Elements, Devices and Associated Methods

Preliminary Class

396

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

SAMSUNG EX. 1002 - 68/4148

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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SAMSUNG EX. 1002 - 69/4148

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/747,875

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	19 minus 20 =	*	x 40 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*	x 210 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	730		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

To: patentdocket@tnw.com,rich@tnw.com,annette.fields@tnw.com
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 20551

Sep 18, 2015 05:46:47 AM

Dear PAIR Customer:

THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 20551 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

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Application	Document	Mailroom Date	Attorney Docket No.
14747875	APP.FILE.REC	09/18/2015	3035-052.NP.CON

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

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Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

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PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

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UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/747,875	06/23/2015	Martin U. Pralle	3035-052.NP.CON

CONFIRMATION NO. 1722

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

PUBLICATION NOTICE

OC000000079564988

Title: Pixel Isolation Elements, Devices and Associated Methods

Publication No.US-2015-0372040-A1
Publication Date:12/24/2015

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

SAMSUNG EX. 1002 - 72/4148

To: patentdocket@tnw.com,rich@tnw.com,annette.fields@tnw.com
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 20551

Jan 09, 2016 06:45:20 AM

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P.O. Box 1219
SANDY, UT 84091-1219
UNITED STATES

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Application	Document	Mailroom Date	Attorney Docket No.
14747875	NTC.PUB	12/28/2015	3035-052.NP.CON

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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☒ Practitioners associated with Customer Number: 136549

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☑ The address associated with Customer Number: 136549

OR

☐	Firm or Individual Name			
	Address			
	City		State	Zip
	Country			
	Telephone		Email	

Assignee Name and Address: SiOnyx, LLC
100 Cummings Center, Suit 243F
Beverly, MA 01915

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	12/18/15
Name	Stephen Saylor	Telephone	508.521.4305
Title	CEO, SiOnyx LLC		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	24612573
Application Number:	14747875
International Application Number:	
Confirmation Number:	1722
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	20551
Filer:	Andrew W. Schultz
Filer Authorized By:	
Attorney Docket Number:	3035-052.NP.CON
Receipt Date:	13-JAN-2016
Filing Date:	23-JUN-2015
Time Stamp:	15:45:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Assignee showing of ownership per 37 CFR 3.73	StatementUnder37CFR373.pdf	120223 7d5c1dcbbf08f578ffc18cf6677b721768ba14a1	no	3

Warnings:	
Information:	

SIONYX1403000014.0077

2	Power of Attorney	SiOnyxGeneralPOA.pdf	135238 e9afbd7bc0956680044b1515c2efca6b59ea1bc3	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	255461

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/96 (08-12)
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: SiOnyx, LLC

Application No./Patent No.: 14/747,875 Filed/Issue Date: June 23, 2015

Titled: PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS

SiOnyx, LLC, a Limited Liability Company

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Inventors To: SiOnyx, Inc.

   The document was recorded in the United States Patent and Trademark Office at Reel 037347, Frame 0032, or for which a copy thereof is attached.

2. From: SiOnyx, Inc. To: SiOnyx, LLC

   The document was recorded in the United States Patent and Trademark Office at Reel 037449, Frame 0884, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Andrew W. Schultz/	January 13, 2016
Signature	Date
Andrew W. Schultz	66,869
Printed or Typed Name	Title or Registration Number

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/747,875	06/23/2015	Martin U. Pralle	3035-052.NP.CON

CONFIRMATION NO. 1722

POA ACCEPTANCE LETTER



136549
Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

Date Mailed: 01/29/2016

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/13/2016.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/dtdinh/

To: docketingbn@pepperlaw.com,davisdr@pepperlaw.com,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 136549

Jan 29, 2016 05:22:41 AM

Dear PAIR Customer:

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 136549 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

Disclaimer:
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Application	Document	Mailroom Date	Attorney Docket No.
14747875	N570	01/29/2016	3035-052.NP.CON

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/747,875	06/23/2015	Martin U. Pralle	143705.05211	1722

136549 7590 04/21/2016

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
04/21/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketingbn@pepperlaw.com
davisdr@pepperlaw.com

Office Action Summary	Application No. 14/747,875	Applicant(s) PRALLE ET AL.	
	Examiner LONG PHAM	Art Unit 2814	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-17,19 and 20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) *1-17 and 19-20* are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Election/Restrictions

This application contains claims directed to the following patentably distinct species: embodiment or species 1 of fig. 1, embodiment or species 2 of fig. 2, embodiment or species 3 of fig. 3, embodiment or species 4 of fig. 4, embodiment or species 5 of fig. 5, embodiment or species 6 of fig. 6, embodiment or species 7 of fig. 7. The species are independent or distinct because **the patentability or unpatentability of one species does not necessarily imply the patentability or unpatentability of another species**. In addition, these species are not obvious variants of each other based on the current record.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species, or a single grouping of patentably indistinct species, for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no independent claim appears to be generic to other independent claims.

There is a search and/or examination burden for the patentably distinct species as set forth above because at least the following reason(s)

apply: **The searches of the patentably distinct species are not co-extensive**.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected species or grouping of patentably indistinct species**, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species or grouping of patentably indistinct species.

Should applicant traverse on the ground that the species, or groupings of patentably indistinct species from which election is required, are not patentably distinct, applicant should submit evidence or identify such

evidence now of record showing them to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.A telephone call was made to -- on -- to request an oral election to the above restriction requirement, but did not result in an election being made.

The examiner has required restriction between product or apparatus claims and process claims. Where applicant elects claims directed to the product/apparatus, and all product/apparatus claims are subsequently found allowable, withdrawn process claims that include all the limitations of the allowable product/apparatus claims should be considered for rejoinder. All claims directed to a nonelected process invention must include all the limitations of an allowable product/apparatus claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product/apparatus claims and the rejoined process claims will be withdrawn,

and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product/apparatus are found allowable, an otherwise proper restriction requirement between product/apparatus claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product/apparatus claim will not be rejoined. See MPEP § 821.04. Additionally, in order for rejoinder to occur, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product/apparatus claims. **Failure to do so may result in no rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LONG PHAM whose telephone number is (571)272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The

fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

/LONG PHAM/
Primary Examiner, Art Unit 2814

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14747875	PRALLE ET AL.
	Examiner	Art Unit
	LONG PHAM	2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	04/17/2016								
	1	÷								
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	19	÷								
	20	÷								

To: docketingbn@pepperlaw.com,davisdr@pepperlaw.com,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 136549

Apr 21, 2016 05:32:19 AM

Dear PAIR Customer:

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736
UNITED STATES

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Application	Document	Mailroom Date	Attorney Docket No.
14747875	CTRS	04/21/2016	143705.05211

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Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Martin U. Pralle Application No.: 14/747,875 Filed: June 23, 2015 For: PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS	Confirmation No.: 1722 Art Unit: 2814 Examiner: Long Pham

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Certificate of Mailing

I hereby certify that this correspondence is being electronically filed via EFS-Web to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

June 22, 2016 (Dated) Electronic Signature: Reza Mollaaghababa

RESPONSE TO RESTRICTION REQUIREMENT

Dear Sir:

In response to the Election/Restrictions Requirement issued in the above-referenced patent application, Applicants elect the species 6 corresponding to FIG. 6 of Applicants' specification.

Amendments to the Claims begin on page 2.

Remarks begin on page 5.

SAMSUNG EX. 1002 - 92/4148

LISTING OF CLAIMS

1. (Currently Amended) A light trapping device, comprising:

at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall ~~disposed into at least a portion of the pixel and~~ extending at least ~~substantially~~ partially around the pixel periphery;

a backside light trapping material at least partially covering the backside surface; and

a peripheral light trapping material substantially covering the peripheral sidewall,

a reflective layer coupled to the light incident side and having an aperture to allow entry of light into the pixel;

wherein the reflective layer is operable to reflect at least a portion of light impinging thereupon from inside the pixel back into the pixel back into ~~toward~~ the pixel.

2. (Currently Amended) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material reflects light incident thereon back into the pixel ~~includes a high refractive index material sandwiched between two low refractive index materials~~.

3. (Canceled)

4. (Currently Amended) The device of claim 1 ~~3~~, wherein said peripheral light trapping material has ~~the two low refractive index materials have~~ a refractive index of less than about 2.1.

5. (Currently Amended) The device of claim 1[4], wherein ~~at least one of the two low refractive index~~ said peripheral light trapping material includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.

6. (Currently Amended) The device of claim 5 [4],wherein said peripheral light trapping material is selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide,

SAMSUNG EX. 1002 - 93/4148

and combinations thereof.

7. (Canceled)

8. (Canceled)

9. (Currently Amended) The device of claim 1 ~~2~~, wherein said peripheral light trapping material ~~at least on the two low refractive index materials~~ is doped with a dopant to create a surface field.

10. (Original) The device of claim 9, wherein the dopant is boron or antimony.

11. (Canceled)

12. (Original) The device of claim 1, wherein the peripheral sidewall extends completely around the pixel periphery.

13. (Original) The device of claim 1, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

14. (Currently Amended) The device of claim 1, wherein said aperture has an effective surface area of less than about 90% of total area of the incident light surface ~~further comprising a frontside light trapping material at least partially covering the light incident surface~~.

15. (Canceled)

16. (Canceled)

17. (Original) The device of claim 16, further comprising a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.

18. (Canceled)

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SAMSUNG EX. 1002 - 94/4148

19. (Original) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

20. (Canceled)
21 – 33 (Canceled)

34. (New) The device of claim 1, further comprising a textured region positioned to interact with light incident thereon to increase quantum efficiency of the device.

35. (New) The device of claim 34, wherein said textured region comprises a textured film layer.

36. (New) The device of claim 35, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.

37. (New) The device of claim 1, wherein the peripheral light trapping material comprises any of aluminum oxide and hafnium oxide.

38. (New) The device of claim 1, wherein the backside light trapping material substantially covers the backside surface.

39. (New) The device of claim 1, wherein the backside light trapping material completely covers the backside surface.

40. (New) The device of claim 1, wherein said peripheral sidewall extends through the pixel substantially from the light incident surface to the backside surface.

SIONYX1403000014.0096

SAMSUNG EX. 1002 - 95/4148

REMARKS

As noted above, Applicants elect species 6 corresponding to FIG. 6 of the specification. Applicants believe that claims 1, 2, 4, 5, 6, 9, 10, 12 – 14, 17, 19, and newly-added claims 34-40 encompass the elected species. Applicants note in this regard that the description of FIG. 6 indicates that "numerical indicators in FIG. 6 from previous figures are intended to reflect the previous descriptions for those elements, and as such, reference is made to FIG. 4."

Claims 3, 7, 8, 11, 15 and 16 are canceled without prejudice (claims 18, 21-33 were previously canceled). Claims 4, 5, 6, 9 and 10 are withdrawn. Claim 1 is generic to the withdrawn claims. Accordingly, upon allowance of claim 1, the rejoinder of the withdrawn claims is requested.

Further, Applicants amend claims 1, 2, 4, 5, 6, 9, and 14, and add new claims 34-40. Support for the amendments and the new claims can be found, e.g., at col. 9, line 34, col. 10, line 26, and lines 56-67, col. 11, lines 38-60, and col. 13, line 66 to col. 14, line 2 of U.S. Patent No. 9,064,764 from which the present application claims priority as a continuation application.

The Examiner is invited to call the undersigned if there are any questions.

The Director is hereby authorized to charge any fees that may be associated with this filing and/or credit any overpayments to our Deposit Account No. 50-0436, under Docket No. 143705.05211.

Dated: June 22, 2016

Respectfully submitted,
Electronic Signature: /Reza Mollaaghababa/
Reza Mollaaghababa, Reg. No. 43,810
Attorney for Applicants
Pepper Hamilton LLP
125 High Street
19th Floor, High Street Tower
Boston, MA 02210
Tel: (617) 204-5168
Fax: (617) 204-5150

SAMSUNG EX. 1002 - 96/4148

Electronic Patent Application Fee Transmittal

Application Number:	14747875
Filing Date:	23-Jun-2015
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Filer:	Reza Mollaaghababa/Jillian Stockel
Attorney Docket Number:	143705.05211

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 1 month with $0 paid	1251	1	200	200
Miscellaneous:				
		Total in USD ($)		**200**

SAMSUNG EX. 1002 - 98/4148

Electronic Acknowledgement Receipt	
EFS ID:	26141927
Application Number:	14747875
International Application Number:	
Confirmation Number:	1722
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	136549
Filer:	Reza Mollaaghababa/Jillian Stockel
Filer Authorized By:	Reza Mollaaghababa
Attorney Docket Number:	143705.05211
Receipt Date:	22-JUN-2016
Filing Date:	23-JUN-2015
Time Stamp:	15:02:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$200
RAM confirmation Number	062316INTEFSW15042401
Deposit Account	1014
Authorized User	Jillian Stockel
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

SIONYX1403000014.0100

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		ResponseRestReq.pdf	107403 07589502511a226fa484d4e6bff3f217daa93088	yes	5

Multipart Description/PDF files in .zip description

Document Description	Start	End
Response to Election / Restriction Filed	1	1
Claims	2	4
Applicant Arguments/Remarks Made in an Amendment	5	5

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30490 87f66bdbd8ec947f32f18294f5708c981ce75938	no	2

Warnings:

Information:

Total Files Size (in bytes):	137893

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/747,875	Filing Date 06/23/2015	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	06/22/2016	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	X $40 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $210 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

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Substitute for Form 1449/PTO				Complete if Known	
				Application No.:	14/747,875
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date:	June 23, 2015
				First Named Inventor:	Martin U. Pralle
				Group Art Unit:	2814
(use as many sheets as necessary)				Examiner Name:	Long Pham
Sheet	1	of	20	Attorney Docket No.:	143705.05211

U. S. PATENT DOCUMENTS						
Examiner's Initials	**Cite No.**	**U.S. Patent Document** Number Kind Code (if known)	**Name of Patentee or Applicant of Cited Document**	**Date of Publication of Cited Document MM-DD-YYYY**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	
	A1	3487223	St. John	12/30/1969		
	A2	3922571	Smith	11/25/1975		
	A3	3973994	Redfield	8/10/1976		
	A4	3994012	Warner, Jr.	11/23/1976		
	A5	4017887	Davies et al.	4/12/1977		
	A6	4149174	Shannon	4/10/1979		
	A7	4176365	Kroger	11/27/1979		
	A8	4201450	Trapani	5/6/1980		
	A9	4242149	King et al.	12/30/1980		
	A10	4253882	Dalal	3/3/1981		
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	A20	4593313	Nagasaki	6/3/1986		
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	A22	4630082	Sakai	12/16/1986		
	A23	4648936	Ashby et al.	3/10/1987		
	A24	4663188	Kane	5/5/1987		
	A25	4672206	Suzuki	6/9/1987		
	A26	4673770	Mandelkorn	6/16/1987		
	A27	4679068	Lillquist et al.	7/7/1987		
	A28	4751571	Lillquist	6/14/1988		
	A29	4775425	Guha et al.	10/4/1988		
	A30	4777490	Sharma et al.	10/11/1988		
	A31	4829013	Yamazaki	5/9/1989		
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	A34	4894526	Bethea et al.	1/16/1990		
	A35	4910568	Taki, et al.	3/20/1990		
	A36	4910588	Kinoshita, et al.	3/20/1990		
	A37	4964134	Westbrook et al.	10/16/1990		
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				First Named Inventor:	Martin U. Pralle
				Group Art Unit:	2814
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	A38	4965784	Land et al.	10/23/1990		
	A39	4968372	Maass	11/6/1990		
	A40	4999308	Nishiura et al.	3/12/1991		
	A41	5021100	Ishihara et al.	6/4/1991		
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	A50	5223043	Olson et al.	6/29/1993		
	A51	5234790	Lang, et al.	8/10/1993		
	A52	5244817	Hawkins et al.	9/14/1993		
	A53	5296045	Banerjee et al.	3/22/1994		
	A54	5309275	Nishimura et al.	5/3/1994		
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				Group Art Unit:	2814
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	A82	5731213	Ono	3/24/1998		
	A83	5751005	Wyles et al.	5/12/1998		
	A84	5758644	Diab et el.	6/2/1998		
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	A113	6290713	Russell	9/18/2001		
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	A115	6313901	Cacharelis	11/6/2001		
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	A118	6372591	Mineji et al.	4/16/2002		
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	A122	6429036	Nixon, et al.	8/6/2002		
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	A124	6465860	Shigenaka, et al.	10/15/2002		
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				First Named Inventor:	Martin U. Pralle
				Group Art Unit:	2814
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	A126	6483116	Kozlowski et al.	11/19/2002		
	A127	6483929	Marakami et al.	11/19/2002		
	A128	6486522	Bishay et al.	11/26/2002		
	A129	6493567	Krivitski et al.	12/10/2002		
	A130	6498336	Tian et al.	12/24/2002		
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	A156	6867806	Lee et al.	3/15/2005		
	A157	6900839	Kozlowski et al.	5/31/2005		
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	A160	6923625	Sparks	8/2/2005		
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	A164	7041525	Clevenger et al.	5/9/2006		
	A165	7057256	Carey, III et al.	6/6/2006		
	A166	7075079	Wood	7/11/2006		
	A167	7091411	Falk et al.	8/15/2006		
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				Group Art Unit:	2814
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	A170	7132724	Merrill	11/7/2006		
	A171	7202102	Yao	4/10/2007		
	A172	7211501	Liu et al	5/1/2007		
	A173	7235812	Chu, et al.	6/26/2007		
	A174	7247527	Shimomura et al.	7/24/2007		
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	A205	7605397	Kindem et al.	10/20/2009		
	A206	7615808	Pain, et al.	11/10/2009		
	A207	7618839	Rhodes	11/17/2009		
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	A210	7648851	Fu, et al.	1/19/2010		
	A211	7649156	Lee	1/19/2010		
	A212	7705879	Kerr et al.	4/27/2010		
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	A214	7741666	Nozaki, et al.	6/22/2010		
	A215	7745901	McCaffrey et al	6/29/2010		
	A216	7763913	Fan et al	7/27/2010		
	A217	7772028	Adkisson et al	8/10/2010		
	A218	7781856	Mazur et al.	8/24/2010		
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	A238	8088219	Knerer et al.	1/3/2012		
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	A244	8288702	Veeder	10/16/2012		
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	A246	8564087	Yamamura et al.	10/22/2013		
	A247	8603902	Mazer et al.	12/10/2013		
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	A249	8680591	Haddad et al.	3/25/2014		
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	A251	8884226	Miyazaki, et al.	11/11/2014		
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	A253	8994135	Yamamura et al.	6/31/2015		
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	A256	20010017344	Aebi	8/30/2001		
	A257	20010022768	Takahashi	9/20/2001		

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	A258	20010044175	Barret et al.	11/22/2001		
	A259	20020020893	Lhorte	2/21/2002		
	A260	20020024618	Imai	2/28/2002		
	A261	20020056845	Iguchi et al.	5/16/2002		
	A262	20020060322	Tanabe et al.	5/23/2002		
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				Application No.:	14/747,875
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date:	June 23, 2015
				First Named Inventor:	Martin U. Pralle
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	C138	Zhang et al, "Ultra-Shallow P+-Junction Formation in Silicon by Excimer Laser Doping: a Heat and Mass Transfer Perspective," Int. J. Heat Mass Transfer, 1996, 3835-3844, vol. 39, No. 18, Elsevier Science Ltd., Great Britain.	
	C139	Zhu et al., "Evolution of Silicon Surface Microstructures by Picosecond and Femtosecond Laser Irradiations," Applied Surface Science, 2005, 102-108, Elsevie, Amsterdam, NL.Ultra-Shallow P+-Junction Formation in Silicon by Excimer Laser Doping: a Heat and Mass Transfer Perspective," Int. J. Heat Mass Transfer, 1996, 3835-3844, vol. 39, No. 18, Elsevier Science Ltd., Great Britain.	

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

SAMSUNG EX. 1002 - 121/4148

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(54) LASER GROOVED SOLAR CELLS

(71) UNISEARCH LIMITED
(21) 36664/84 565214 (22) 23.12.83
(23) 13.12.84 (24) 23.12.83
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(51)[3] H01L 31/18 H01L 31/06

(72) STUART ROSS WENHAM AND MARTIN ANDREW GREEN

(74) R1

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US 4046594
US 4137123
EP 14759

(57) Claim

1. A method of manufacturing solar cells, said method comprising the steps of scribing a pattern of grooves or holes in a surface of semiconductor substrate with a laser scriber and subsequently forming a rectifying junction on said surface, said junction extending into said holes or grooves.

3. The method of claims 1 or 2 wherein after said scribing step and before forming the rectifying junction, an etching step is performed, said etching step comprising etching said grooves or holes with a chemical etchant, the etching step being used to control the shape of the grooves or holes in the final cell.

4. The method of claim 3 wherein the chemical etchant is selected to etch the base region of the grooves or holes more slowly than the top region to convert the grooves into V-shaped troughs and to convert the holes to shapes approximating inverted pyramids, and said junction extending into said troughs or inverted pyramids.

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565214

COMMONWEALTH OF AUSTRALIA

Patents Act 1952

APPLICATION FOR A STANDARD PATENT

~~I~~/WE, UNISEARCH LIMITED a company limited by guarantee and incorporated under the laws of the State of New South Wales, Australia, of 221-227 Anzac Parade, Kensington, New South Wales, Australia,

hereby apply for the grant of a Standard Patent for an invention entitled

"The Laser Grooved Solar Cell"

which is described in the accompanying provisional ~~complete~~ specification.

~~This application is made under the provision of Part XVI of the Patents Act 1952 and is a request for a patent or similar protection in~~

~~in~~ ~~xxx~~

~~APPLICATION ACCEPTED AND AMENDMENTS~~ ~~xxx~~ ~~xNax~~

ALLOWED 27-7-87 ~~xNax~~

~~My~~/Our address for service is: F.B. RICE & CO.,
28A Montague Street,
Balmain, NSW 2041

Dated this 23rd day of December, 1983.

UNISEARCH LIMITED

LODGED AT SUB-OFFICE
23 DEC 1983
Sydney

By: Patent Attorney

To : The Commissioner of Patents
COMMONWEALTH OF AUSTRALIA

F.B. RICE & CO.,
Patent Attorneys,
Sydney

POST STAMP
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~~Complete~~ and ~~Provisional~~ SPECIFICATION No. 36664/84

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SAMSUNG EX. 1002 - 123/4148

Commonwealth of Australia
The Patents Act 1952
DECLARATION IN SUPPORT

In support of the (~~Convention~~) Application made by: UNISEARCH LIMITED

for a patent for an invention entitled: The Laser Grooved Solar Cell,

I (~~We~~) RICHARD PETER CARTMER
of and care of the applicant company do solemnly and sincerely declare as follows:

~~a) I am the applicant in respect of this application.~~
~~or~~
b) I am (~~We are~~) authorised by the applicant(~~s~~) for the patent to make this declaration on its behalf.

Delete the following if not a Convention Application.

~~The basic application(s) as defined by section 141 of the Act was (were) made in~~

~~in~~ ~~on~~

~~in~~ ~~on~~

~~in~~ ~~on~~

~~by~~

~~The basic application(s) referred to in this paragraph is (are) the first application(s) made in a Convention country in respect of the invention the subject of the application.~~

~~a) I am the actual inventor.~~
~~or~~
b) STUART ROSS WENHAM of 17 Fortescue Street, Bexley North, N.S.W., 2207 and
MARTIN ANDREW GREEN, of 10 Blandford Avenue, Waverley, N.S.W., 2024
~~is~~ (are) the actual inventor(s) of the invention and the facts upon which Unisearch Limited is (~~are~~) entitled to make the application are as follows:

The applicant is the assignee of the invention from the said actual inventors.

Declared at KENSINGTON this 4th day of DECEMBER 19 94

Signed [signature] Status SENIOR OFFICER (LEGAL)

Declarant's Name RICHARD PETER CARTMER

F. B. RICE & CO PATENT ATTORNEYS
This form is suitable for any type of Patent Application. No legalisation required.

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COMMONWEALTH OF AUSTRALIA

565214

Patent Act 1952

COMPLETE SPECIFICATION

(ORIGINAL)

Class Int. Class

Application Number : PG 3004
Lodged : 23 December 1983

Complete Specification Lodged :
Accepted :
Published :

Priority :

Related Art : 36664/84.

Name of Applicant : UNISEARCH LIMITED

Address of Applicant : 221-227 Anzac Parade,
Kensington N.S.W. 2033

Actual Inventors : Stuart Ross Wenham;
Martin Andrew Green

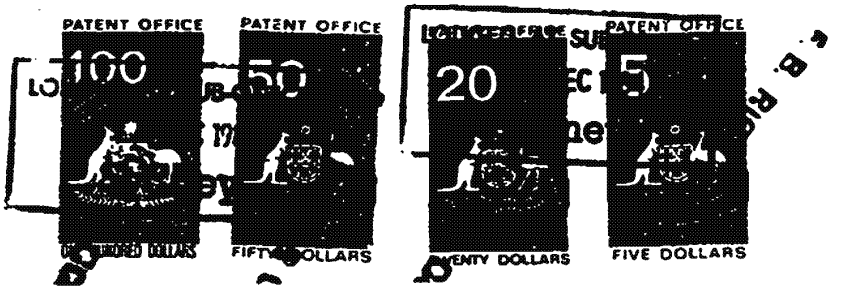
Address for Service : P.B. RICE & CO.,
Patent Attorneys,
28A Montague Street,
BALMAIN. 2041.

LODGED AT SUB-OFFICE
Sydney

Complete Specification for the invention entitled:

The Laser Grooved Solar Cell

The following statement is a full description of this invention including the best method of performing it known to us:-



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The present invention relates to improvements in the fabrication of solar cells whereby the structure of the cell facilitates collection of photon generated minority carriers from deep within the wafer substrate.

Long wavelength light striking a photocell will penetrate much further into the cell than shorter wavelength light, on average, before being absorbed and therefore minority carriers generated by photons of long wavelength energy must travel much further before being collected by the rectifying junction of the cell. As a result, the chances of a minority carrier resulting from a long wavelength photon, being collected before recombination occurs are greatly reduced over those of a minority carrier resulting from a shorter wavelength photon. This effect is even more pronounced in solar cells used in space, due to the radiation damage which is caused to a solar cell in this environment, and which results in a reduction in minority carrier life times.

In an attempt to overcome the effects of reduced minority carrier life time in the space environment, prior art solar cells have been produced wherein a plurality of grooves were chemically etched into the surface of the substrate prior to the formulation of the rectifying junction of the cell, such that the junction provided within the grooves penetrates deep into the bulk of the substrate to aid in the collection of minority carriers formed in the bulk regions.

However, while the formation of grooves in the substrate provides an improvement in short circuit current densities, complications associated with the chemical etching step make this solution too expensive to be of practical use, particularly in the case of mass produced cells for terrestrial use.

A laser scriber has previously been used to separate cells formed on a common wafer, by scribing a groove between

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a pair of adjacent cells and then breaking the wafer along the scribe line in a similar manner to that used when cutting glass or ceramic tiles. Lasers have also been used to isolate doped regions of a substrate by cutting or drilling an opening between the two adjacent regions to be isolated, however, it has not previously been considered feasible to use lasers in the processing of the active regions of semiconductor devices, due to the damage to the crystal structure caused by the laser.

A first aspect of the present invention relies upon the unexpected result that grooves scribed in the surface of a substrate by way of a laser scriber do not cause a significant deleterious effect upon the solar cell subsequently formed on the substrate, due to crystal damage caused by the laser, but to the contrary the crystal damage provides getterring sites to which impurities in the substrate migrate during subsequent high temperature processing, thereby enhancing the performance of the solar cell by increasing the life time of minority carriers in the bulk of the substrate.

It has also been found that grooving of the surface of the cell enhances the anti-reflective properties of the cell, as light falling within the grooved area, if it is not initially absorbed by the cell, will be reflected onto another surface of the groove, thereby increasing the possibility of absorption. In order to escape from the grooved area, a photon will need to be reflected several times within the groove, and therefore the probability of escape is low.

The provision of grooves in the substrate also increases greatly the area of the cell junction and additionally provides the possibility of having differing sheet resistivities in the top layer of the cell, with a high resistivity in the region between the grooves to enhance the photovoltaic effect and a lower resistivity within the

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grooves to decrease the series resistance of the cell and to allow the wider spacing of the contact fingers used to conduct current from the top layer.

According to a first aspect, the present invention consists in a method of manufacturing solar cells, said method comprising the steps of scribing a pattern of holes or grooves in a surface of a semiconductor substrate with a laser scriber and subsequently forming a rectifying junction on said surface, said junction extending into said holes or grooves.

Preferably embodiments of the invention achieve a plurality of parallel grooves or a regular pattern of holes by scribing the surface of the substrate using a laser scriber adapted to simultaneously scribe a repeating pattern of grooves or holes.

In a preferred embodiment of the invention, a chemical etching step is employed between the step of laser scribing and the step of forming the rectifying junction, such that precise control of the shape of holes and grooves is achieved.

Some embodiments of the invention will also make use of holes bored through the substrate during the laser etching step to allow contact to be made with the surface layer of the cell from the rear of the substrate.

Embodiments of the invention may also employ grooving of the rear surface of the substrate to form thin strong cell structures which have high efficiency and are radiation resistant.

In further embodiments of the present invention a solar cell is produced having a substrate, one surface of which has a plurality of grooves or hollows formed therein, and a rectifying junction formed on said surface and extending into said grooves, a top layer of said junction having a sheet resistivity which is greater in the region between the grooves than in the region within the grooves.

In yet further embodiments of the present invention

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~~consists in~~ is produced having a solar cell ~~comprising~~ a substrate, opposite surfaces of which each have a plurality of grooves or hollows formed therein, a rectifying junction being formed on one of said surfaces and extending into the grooves or hollows of that surface.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings wherein:

Figure 1 schematically illustrates a sectional view of a solar cell manufactured in accordance with a first embodiment of the present invention;

Figure 2 schematically illustrates the solar cell of Figure 1 when viewed from the top;

Figure 3 schematically illustrates a sectional view of a solar cell manufactured in accordance with a second embodiment of the present invention;

Fig. 4 schematically illustrates a sectional view of a fully etched substrate according to an embodiment of the invention;

Fig. 5 schematically illustrates (a) a plan view of a laser scribing pattern; (b) a plan view of a fully etched substrate and (c) a perspective view of a fully etched substrate for a fourth embodiment of the invention;

Fig. 6 schematically illustrates (a) a plan view of a laser scribing pattern; (b) a plan view of a fully etched substrate and (c) a perspective view of a fully etched substrate for a fifth embodiment of the present invention;

Figs. 7, 8 and 9 schematically illustrate (a) a plan view of a laser scribing pattern and (b) a perspective view of a fully etched substrate for sixth, seventh and eighth embodiments respectively, of the present invention; and

Fig. 10 schematically illustrates an improved method of connecting electrodes to the embodiment of Fig. 8.

Referring to Figure 1, a substrate 10 is provided with a back contact 11 and a rectifying junction 12 on opposite

surfaces, the junction being formed between the substrate 10, which may be of either p-type or n-type semiconductor material, but in this embodiment is p-type material, and a top layer 13 extending over the top surface of the substrate and which is formed of a semiconductor material of opposite impurity type to the substrate 10. Grooves 14 scribed in the top surface of the substrate by a laser scriber, prior to formation of the junction 12, greatly increase the junction area and at the same time facilitate the collection of minority carriers 15 generated deep within the bulk of the substrate, by placing sections of the junction in closer proximity to the region in which these carriers are generated.

Grooves 14 in the cell surface also improve the anti-reflection properties of the cell by acting as light traps. Light 16a striking the surfaces of the cell between the grooves, and which is not absorbed by the cell, will be reflected by the surface and wasted, however, light 16b striking a surface of one of the grooves 14, and which is not absorbed, will generally be reflected onto another surface of the groove, depending upon the angle of incidence of the light and the shape of the grooves. For light 16b falling normal to the top surface of the cell, the number of reflections within the groove 14 will be large, thereby reducing the percentage of light which is reflected out of the grooves.

A further improvement in the anti-reflective properties of the cell may be achieved by filling the grooves with a transparent material such as silicon oxide, and the slope of the groove walls can be optimized after scribing by an unmasked etch of the entire substrate surface.

As well as the improvement in current density due to the physical positioning of the junction within the groove and the increased area of the junction, a further improvement can be attributed to the production of getterring sites during the laser scribing of the surface of the substrate, thereby

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allowing an increased degree of getterring during subsequent high temperature processing.

Getterring is the process by which impurities are attracted to certain areas of the substrate during high temperature processing, and typical getterring sites are regions of stress causd by diffusion processes and areas of crystal structure damage as caused by laser scribing. The laser scribing process, being a particularly robust process, creates a significant amount of damage to the crystal structure and accordingly a large number of getterring sites will be produced by this process.

The reduction in the number of impurities in the bulk of the substrate, as a result of getterring, has the effect of increasing the minority carrier life time and accordingly increasing the probability of a minority carrier being collected at the rectifying junction 12 before recombination occurs.

The series resistance of the grooved solar cell can also be decreased by selecting a lower sheet resistivity for the portion of the top layer 13 formed in the grooves 14 than for that used in the portion of the top layer between the grooves. In a non-grooved solar cell, manufactured for terrestrial use, the metal contact grid applied to the top layer is often applied by screen printing in order to keep cost to a minimum, however, screen printing imposes restrictions upon the minimum dimensions achievable, these being a minimum contact width of typically 150μm and a mimimum spacing of at least 3mm. With these contact dimensions, it is necessary to provide a top layer sheet resistivity in the order of 25 Ω/□ to 50 Ω/□ to minimize lateral resistance, however, such low values of sheet resistivity degrade the photovoltaic properties of the cell. This problem is less pronounced in cells produced for use in space, as in these cells a more sophisticated method of contact formation is used which allows the use of thinner

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contacts having a closer spacing, such that higher sheet resistivities can be used without degrading the series resistance of the cell. However, the method of contact formation used in space cells adds considerably to their manufacturing costs.

In the case of grooved cells made according to the present invention, sheet resistivities in the order of 25Ω/□ to 50 Ω /□ can be provided for that portion of the top layer 13 within the grooves 14, while sheet resistivities in the order of 100-200 Ω /□ can be achieved in the top layer portions between the grooves. Typically the groove would be in the order of 50μm wide and the space between the grooves would be 100μm, the metal contact fingers 17 (see Fig. 2) running in the direction normal to the grooves and having the dimensions previously stated for screen printed contacts.

A lower sheet resistivity can be achieved in the grooved regions in numerous ways, some examples of which are:

(a) Diffuse the entire surface, oxidise and/or deposit nitride, form laser grooves through the oxide and/or nitride and first diffusion, chemically clean the grooves, complete a second heavy diffusion. This second diffusion will be localized to the grooved areas due to the blocking action of oxide and/or nitride.

(b) Oxidise wafer . as a thinner oxide than in (a) above results, form laser grooves through the oxide, chemically clean the grooves, and diffuse heavily. Oxide will partly block the diffusion in non-grooved areas resulting in a lighter diffusion in these areas.

(c) Dilute commercially available 'spin on' dopant source and apply to grooved surface. The source will coat non-grooved areas to a thickness determined by source viscosity and spin speed, but can completely fill grooves. This will result in a larger volume of source per unit surface area in grooved as opposed to non-grooved areas. Consequently more dopants will enter the surface in grooved

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areas in subsequent high temperature treatments than non-grooved areas.

(d) Diffuse entire grooved wafer surface heavily. Use dilute chemical etch to etch back diffused areas. The etch will have less opportunity for replenishment in grooved areas and will quickly become depleted and ineffective in these regions. Hence, diffused material will be selectively removed from non-grooved areas. A similar technique which makes use of plasma etching is also possible.

(e) Use a laser to locally heat the silicon in grooved regions subsequent to the application of a diffusion source.

The low sheet resistivity of the top layer in the grooved regions will have a detrimental effect on the response of the cell to short wavelength (blue) light due to the increased top layer thickness and therefore the sheet resistivity chosen will be a compromise between a value which gives low series resistance and a value which does not seriously degrade the response to blue light. It will be recognised, however, that while low sheet resistivity will degrade the response to blue light, the beneficial effects of

low series resistance and improved current density due to increased junction area and the provision of a portion of the junction deep within the bulk of the substrate, will more than make up for this degradation. Further, the low sheet resistivity in the grooves will not seriously affect the response of the cell to long wavelength (red) light.

The use of a low sheet resistivity top layer in the grooved regions of space cells will also allow the contact fingers in these cells to be spaced more widely, thereby, allowing the use of less costly formation process and accordingly reducing the manufacturing costs of the cell.

Referring now to Figure 3 the metal contact fingers 17 in Figure 2 may be replaced by Conductor-Insulator-Silicon (CIS) contacts wherein the top layer 13 is a lightly doped region, the rectifying effect of the junction 12 being reinforced by the MIS contact comprising a thin layer of insulation 18 over the top layer and a metal, or a highly doped polycrystalline, contact finger 19 formed over the insulation layer 18. The fingers 19 will be arranged in a similar configuration to the metal fingers 17 shown in Figure 2, however, the insulation layer may either be formed over the entire surface of the cell, by using a transparent insulation layer such as a silicon oxide, or alternatively the insulation layer may be only formed in the region of the conductor finger 19.

Referring to Fig. 4 of the drawings, reflection properties of the laser groove cell can be optimised by arranging the grooving so that the sloping groove walls intersect with one another, thereby substantially eliminating the flat intergroove regions illustrated in Figs. 1, 2 and 3. With the structure of Fig. 4, the only ungrooved regions required are flat paths 21 (refer to Fig. 5) provided for the top contact metallisation.

As illustrated in Fig. 4, very precise control can be obtained of such structures in single crystal material by

using chemical etches with anisotropic properties, combined with laser grooving. For example, dilute caustic soda solutions etch silicon very slowly in the [111] crystal direction but etch very rapidly in other directions. Therefore, if the surface 22 of a wafer has [100] orientation and is grooved by a laser to form grooves 23 and then subsequently etched in dilute caustic soda solutions, the silicon is very quickly etched away until the [111] crystal planes are exposed to form the grooved surface 24 of Fig. 4. Once the [111] crystal planes, coinciding with the faces of the surface 24, are exposed, the rate of etching slows markedly, allowing precise control of the final etched surface shape, thereby allowing the resulting surface geometry of the device to be precisely defined by the depth and spacing of the original grooves 23.

Regardless of the method used to control the slope of the groove walls, interesting and useful structures can be obtained by the use of intermittent grooving of the cell surface and several such structures will now be described with reference to Figs. 5, 6, 7, 8 and 9.

Referring to Fig. 5, a "slat" structure is illustrated wherein the laser grooving 23 is intermittently broken by gaps 25 in order to provide strengthening ribs or struts 26 in the final etched substrate of Fig. 5(c). In addition, a larger gap 27 in the laser grooving pattern results in the flat path 21 in the final etched substrate which provides a location for top contact metallisation in the completed cell.

Turning to Fig. 6, the laser grooves 23 of Fig. 5 are replaced by holes 33 which are bored by the laser scriber in the square pattern illustrated in Fig. 6a, such that after etching, an inverted pyramid structure as illustrated in Fig. 6b and Fig. 6c is produced with the top surface 34 of the inverted pyramid structure again corresponding to the [111] crystal planes of the substrate.

Combined grooving of the front and rear surfaces of the

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wafer and subsequent etching gives rise to a further class of cells which have been termed "crinkle cut" cells. Referring to Fig. 7, if a grooving pattern 43, similar to the pattern 23 of Fig. 5a is provided in a top surface of the wafer and a second grooving pattern 53, again similar to the pattern 23 of Fig. 5a, is provided in the bottom surface of the wafer and the wafer is subsequently etched, a structure of the form illustrated in Fig. 7b will be produced, wherein parallel grooves run along both sides of the wafer, the grooves in one side corresponding with the peaks in the other side of the wafer to provide a [illegible]gated structure having strengthening struts or ribs 46 and [illegible] (ribs 56 not shown) and the surfaces 44 and 54 each corresponding to [111] crystal planes of the substrate.

Figs. 8 and 9 illustrate additional "crinkle cut" structures, the structure of Fig. 8 comprising inverted pyramids similar to those of Fig. 6 on each side of the wafer, with the pyramids on one side of the wafer being offset from those on the other side, while the structure of Fig. 9 has inverted pryamids on the top surface and a crossed groove structure on the bottom surface to provide an etched wafer structure having a substantially constant thickness as is the case with the structure of Fig. 7. The structures of Fig. 7 and Fig. 9 allow very thin strong cells having good reflection properties to be fabricated and these structures will assist in the production of very high efficiency cells with good radiation resistance. The structure of Fig. 8 on the other hand will produce cells having good reflection properties with moderate thickness but great strength.

The laser grooving technique can also be used to produce structures which have holes extending right through the cell from one side to the other. The structures illustrated in Figs. 6, 8 and 9 are particularly suited to this technique. The advantage of a structure which employs holes passing completely through the cell is that it is then possible to

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have both contacts to the cell made on the rear surface of the cell, thereby avoiding the losses associated with top contact shading. For example, a section of a structure similar to that of Fig. 6 is illustrated in Fig. 10, wherein the grooving is much greater than that previously illustrated such that the apex 35 of inverted pyramids extends to the back surface of the wafer. With this structure, once the top layer 13 has been formed, metallised top contacts 36 can be provided from the back of the cell at each apex point. This technique allows an improvement in overall cell efficiency by removing the problem of top contract shading which would otherwise occur, while at the same time allowing connections to the top contacts to be of greater current carrying capacity, as the trade off between current carrying capacity and degree of shading is no longer necessary.

The laser used to produce any of the previous laser groove structures can be programmed very simply to punch holes through the cell in any prescribed location so that a variety of such punch through structures are possible with this approach and clearly the punch through technique can be used with any of the structures previously described.

A preferred method of manufacturing laser groove cells requires starting with a silcon wafer of desired surface orientation (for example [100])and then grooving one or both sides of the cell in the desired pattern using a laser. The wafer is then etched in an appropriate chemical solution to define the shape of the walls of the groove. Thereafter, cell processing proceeds as it would with prior art devices. The top junction is formed by the diffusion of an appropriate dopant and, if desired, a back surface field region is formed at the rear of the cell. Top and rear contact metallization can then be formed by any chosen sequence, e.g. vacuum deposition, screen printing or electroplating, as can the antireflection coating.

It will be recognised by persons skilled in the art that

numerous variations and modifications may be made to the invention as described above without departing from the spirit or scope of the invention as broadly described.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:-

1. A method of manufacturing solar cells, said method comprising the steps of scribing a pattern of grooves or holes in a surface of semiconductor substrate with a laser scriber and subsequently forming a rectifying junction on said surface, said junction extending into said holes or grooves.

2. The method of claim 1 wherein said laser scriber is adapted to simultaneously scribe a plurality of grooves or holes in said substrate.

3. The method of claims 1 or 2 wherein after said scribing step and before forming the rectifying junction, an etching step is performed, said etching step comprising etching said grooves or holes with a chemical etchant, the etching step being used to control the shape of the grooves or holes in the final cell.

4. The method of claim 3 wherein the chemical etchant is selected to etch the base region of the grooves or holes more slowly than the top region to convert the grooves into V-shaped troughs and to convert the holes to shapes approximating inverted pyramids, and said junction extending into said troughs or inverted pyramids.

5. The method of claims 1, 2, 3 or 4 wherein the laser scriber is used to bore holes through the substrate during the laser scribing step and the junction extends through said holes to cover a portion of the rear surface thereof such that contact can be made with the top layer of the cell from the rear of the substrate.

6. The method of any one of the preceding claims, wherein grooving of the rear surface of the substrate is employed to reduce the thickness of the cell structure, grooves in the rear surface being located between grooves in the top surface of the substrate.

7. A solar cell manufactured using the method as claimed in any one of the preceding claims wherein said rectifying

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junction has a top layer with a sheet resistivity which is greater in the region between the grooves than in the region within the grooves.

8. A solar cell as claimed in claim 7, wherein the sheet resistivity of the top layer within the grooves is in the order of 25-50 Ω/□ while sheet resistivity of the top layer between the grooves is in the order of 100-200 Ω/□ .

9. A solar cell as claimed in any one of claims 7 or 8 wherein holes are provided through the substrate, the top layer of the rectifying junction extending into the through holes and metalized top contacts being provided on the back of the substrate at each of said holes to make an electrical connection with the top layer of the junction.

10. A solar cell, made in accordance with the method of claim 1.

11. A method of manufacturing a solar cell as claimed in claim 1, substantially as hereinbefore described.

12. A solar cell substantially as hereinbefore described with reference to the accompanying drawings.

DATED this 7th day of July 1987

UNISEARCH LIMITED
Patent Attorneys for the
Applicant:

F.B. RICE & CO.

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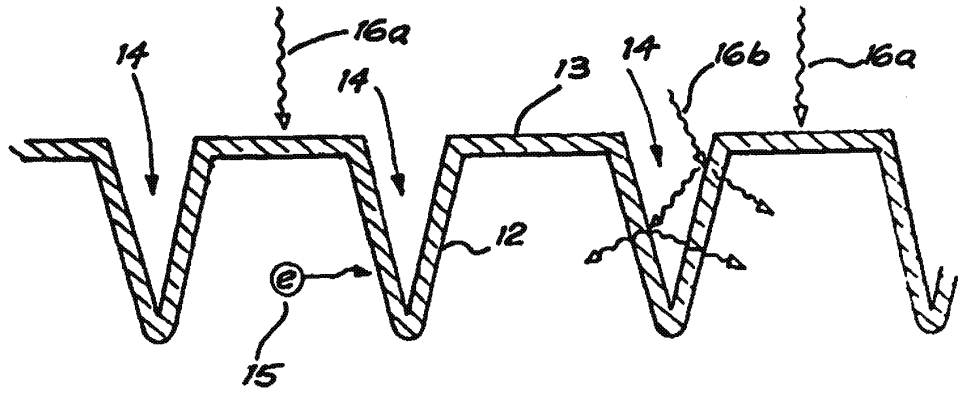




FIG.1

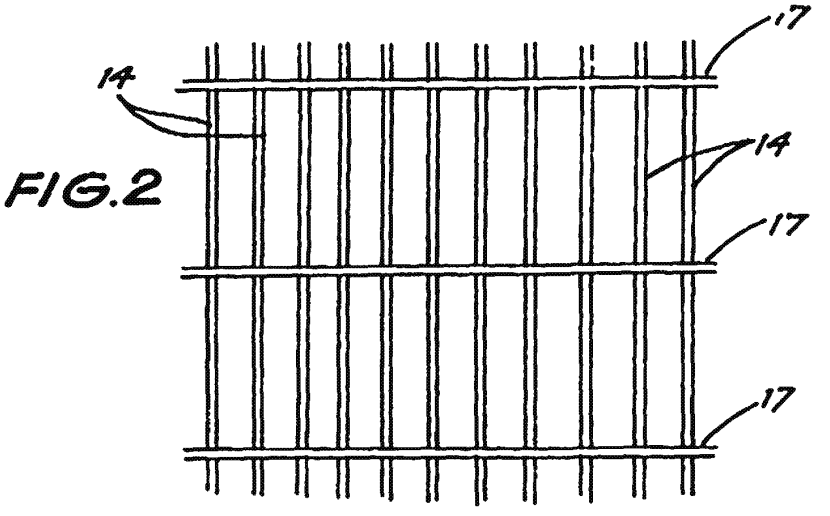


FIG.2

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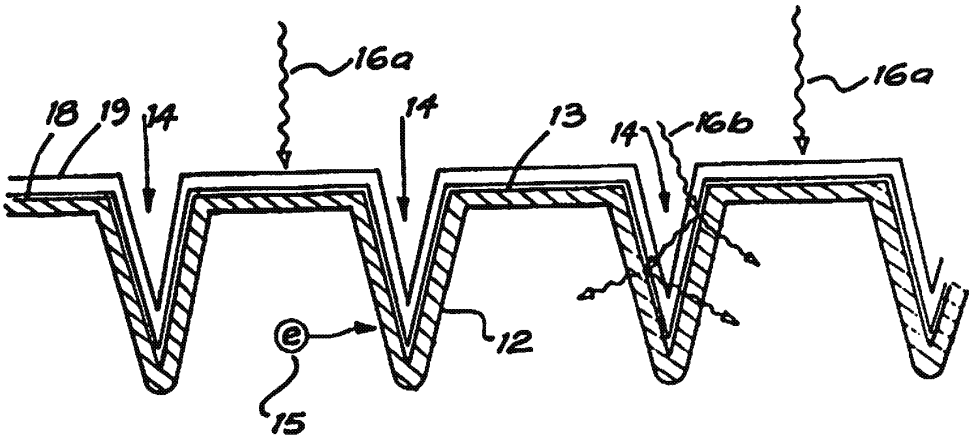


FIG. 3

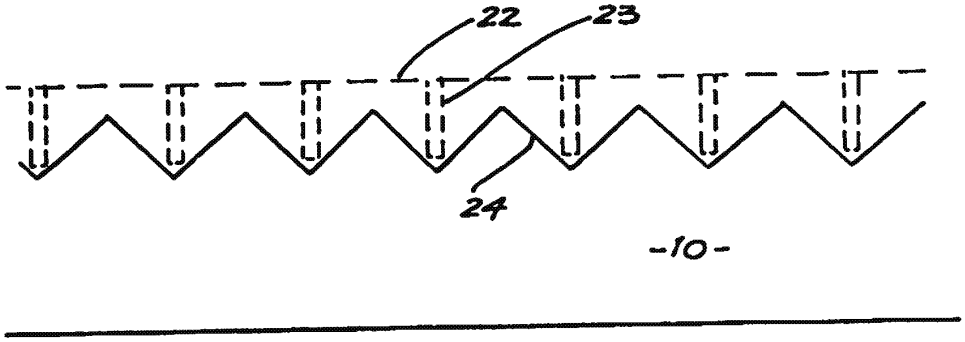


FIG. 4

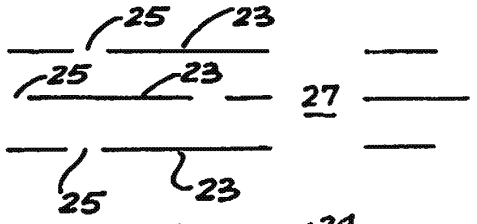


FIG. 5a

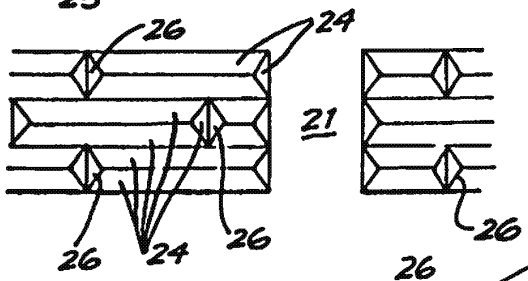


FIG. 5b

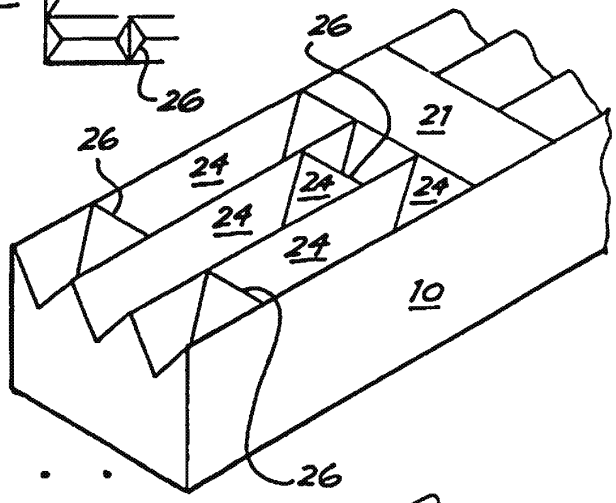


FIG. 5c



FIG. 6a

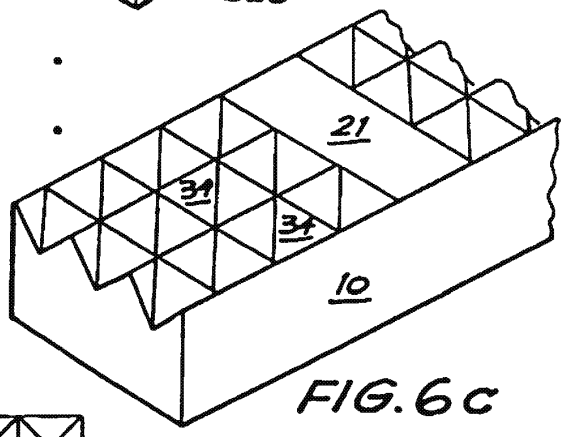


FIG. 6c

FIG. 6b

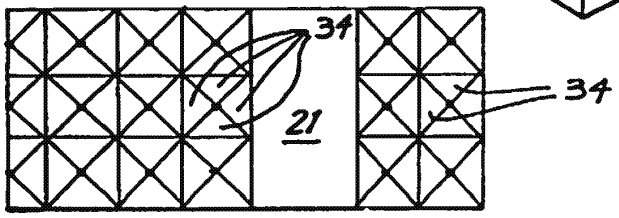


FIG. 7a

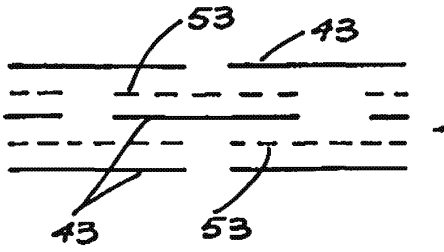
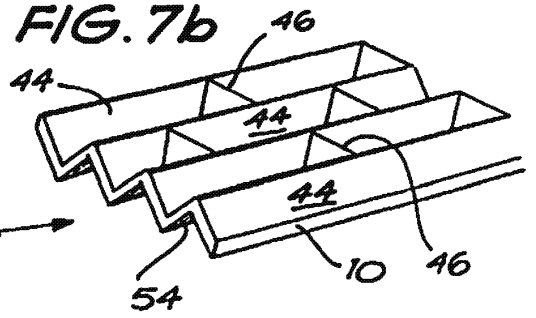


FIG. 7b



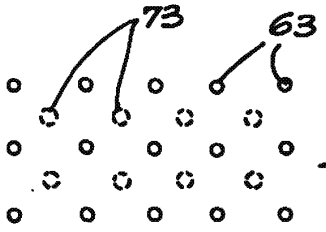


FIG. 8a

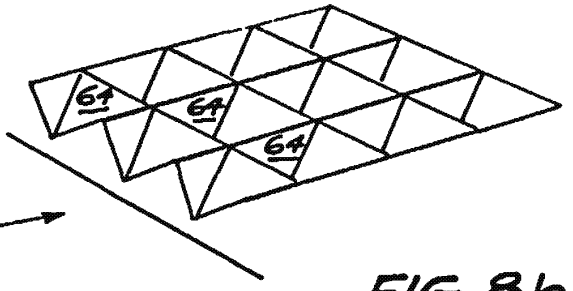
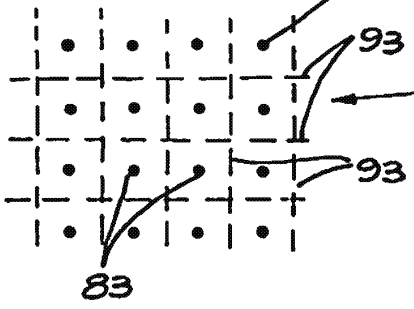


FIG. 8b

FIG. 9a



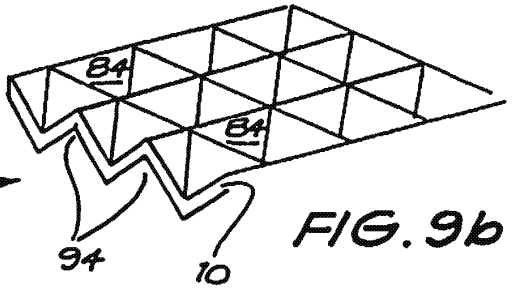
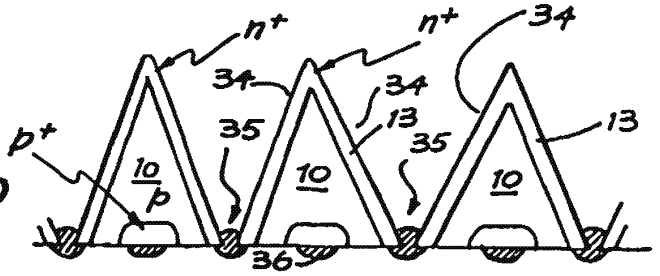


FIG. 9b

FIG. 10



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FIG. 7a

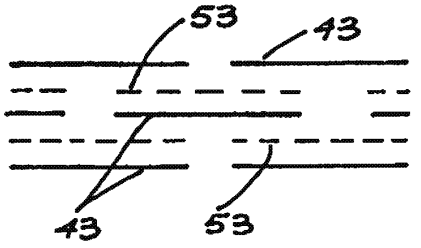
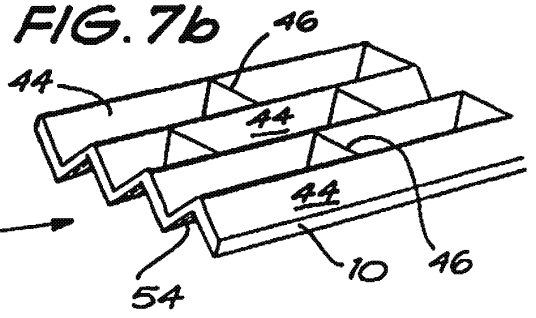


FIG. 7b



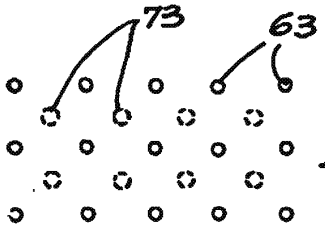


FIG. 8a

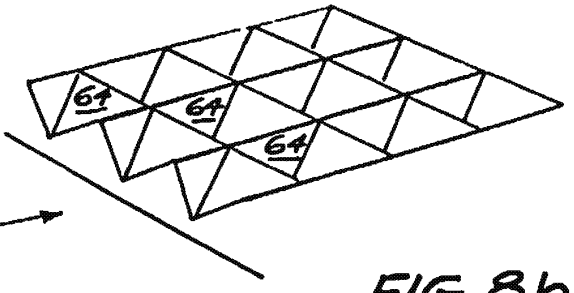
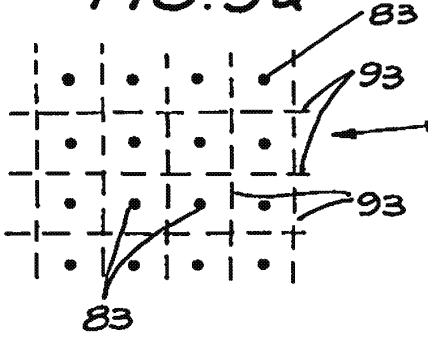


FIG. 8b

FIG. 9a



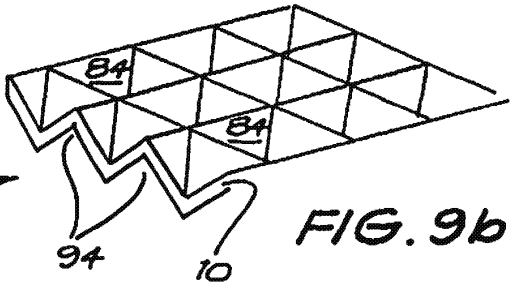
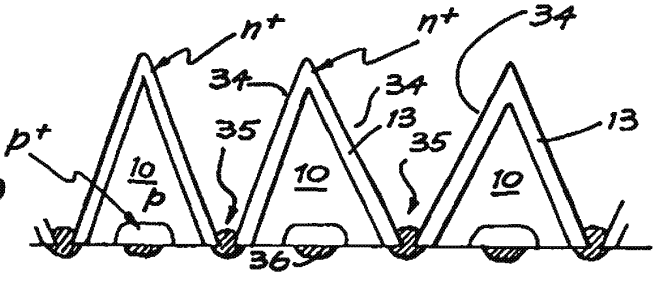


FIG. 9b

FIG. 10



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(54) **Electronic switch comprising a photosensitive semiconductor.**

(57) An electronic switch comprises a photosensitive semiconductor (1,11,12) and a light source (14,24) which, when actuated, illuminates the semiconductor and causes the latter to become conductive, the photosensitive semiconductor being a sintered mixture comprising, by weight, 58 - 72% of cadmium, 14.8 - 21% of selenium, 7 - 15% of tellurium, 7 - 12% of sulphur, 0.1 - 1% of chlorine, and 0.005 - 0.1% of copper.

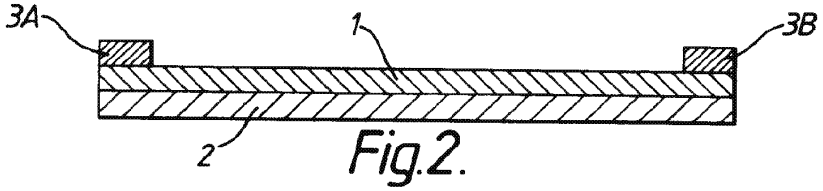


Fig.2.

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The present invention relates to an electronic switch comprising a photosensitive semiconductor and a light source which, when actuated, illuminates the semiconductor and causes the latter to become conductive.

Photosensitive semiconductors are well known and need not be described in detail. The main characteristic of such semiconductors is their ability to pass from an electrically non-conductive and high resistance state to an electrically conductive and low resistance state when they are illuminated with light.

Materials presently used as or in industrial photosensitive semiconductors are for example : silicon, carbon, germanium, gallium arsenide, silicon carbide, cadmium selenide, cadmium sulphide, indium phosphide, and potassium phosphide. These prior art photosensitive semiconductors can be used in various electronic devices, for example, in electronic switches, and are generally doped with 'impurities' such as, for example : cobalt, copper, chromium, gold, iron, oxygen, silver, and zinc.

Electronic switches comprising a photosensitive semiconductor are described, for example, in the following U.S. Patents: 4,301,362; 4,347,437; 4,438,331; 4,490,709; 4,577,114 and 4,695,733. Various configurations of switches are described in these patents. They all comprise a light source and a photosensitive semiconductor provided with two spaced electrodes. The semiconductors are made of various materials and the light source is generally a laser.

When, for a given semiconductor, a certain bias voltage is applied across the electrodes of a photosensitive switch, the semiconductor will not permit the electrical current to pass between the electrodes and the switch will be in its "off" position, but when the light source projects light energy on to the area of the semiconductor located between the electrodes the semiconductor becomes electrically conductive and the switch will be in its "on' position. The main advantage of switches of this type is that they can switch an electrical current on or off very rapidly.

A disadvantage of known photosensitive switches and, in particular, of the switches disclosed in the above six U.S. patents is that they are only capable of switching electrical supplies which have voltages of a few kV, for example up to 3-5 kV, and thus cannot be used in electrical devices where a higher voltage is required.

It is therefore a first object of the invention to provide an electronic switch activated by light that is capable of withstanding/switching high voltage, low amperage electrical currents, that is electrical supplies having a voltage of at least 30 kV and having an amperage of less than 0.2 A. It is a further object of the invention to provide a very compact and a very economical high voltage, low amperage photosensitive switch and it is also an object of the invention to provide a photosensitive switch capable of operating with a high pulse repetition rate.

We have now found that certain doped cadmium sulpho-selenide-telluride semiconductor compositions have a desirable combination of properties such that when used as the semiconductor in a photosensitive switch, the latter is capable of switching high voltage, low amperage electrical supplies and can be constructed compactly and cheaply and can be operated at a high pulse repetition rate.

According to the present invention, there is provided an electronic switch comprising a photosensitive semiconductor and a light source which, when actuated, illuminates the semiconductor and causes the latter to become conductive, in which the photosensitive semiconductor is a sintered mixture comprising, by weight, 58 to 72% of cadmium, 14.8 to 21% of selenium, 7 to 15% of tellurium, 7 to 12% of sulphur, 0.1 to 1% of chlorine, and 0.005 to 0.1% of copper.

The semiconductor is preferably in the form of an adherent layer on an electrically insulating substrate. The semiconductor is provided with spaced electrodes to which, in use, the circuit which the switch is to control is connected. The electrodes may be two adherent, spaced electrode layers on the sintered semiconductor layer or the substrate may be provided with two adherent, spaced electrode layers and the adherent sintered semiconductor layer may be applied over the electrode layers and the substrate between them; in the latter case the electrode layers are below the semiconductor layer.

The electrode layers may be formed of any suitable electrically conductive material, preferred materials being, for example, silver, gold, indium and aluminium and resins, for example epoxy resins, loaded with any one or more of these metals.

According to another aspect of the present invention, there is provided a method of making an electronic switch according to the invention, which comprises forming a paste of a finely divided powder mixture comprising, by weight, 32 to 47% of cadmium selenide, 32 to 49% of cadmium sulphide, 7 to 15% of tellurium, 4.7 to 13% cadmium chloride, and 0.01 to 0.1% of copper chloride, a binder and a volatile liquid, forming a coating of the paste on an electrically insulating substrate and drying the coating, sintering the dried coating at a temperature of from 510°C to 800°C to form an adherent layer of photosensitive semiconductor on the substrate, providing adherent spaced electrode layers either on or below the semiconductor layer, and assembling the coated substrate with a light source.

The formation of the sintered semiconductor layer may be carried out in accordance with conventional sintering techniques which will be well known to those skilled in the art.

In order to obtain the desired photosensitivity and electrical properties in the sintered semiconductor, the

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finely divided powder materials must be of the highest purity, for example of 99,999% or more, and the size of the powder particles is preferably less than 3 μm.

Suitable binders and volatile liquids for forming the paste will be known to those skilled in the art. It is generally preferred to use ethyl cellulose as the binder, but other suitable binders include, for example, linseed oil and cellulose acetate. Preferred volatile liquids are organic liquids; suitable organic liquids include, for example, turpineol, acetone and ethanol, of which the first is generally preferred. The binder is preferably present as a 10% by weight solution in the volatile liquid. The proportion of binder/volatile liquid solution in the paste will, of course, depend on the desired viscosity of the paste which will, in turn, depend on the method of coating the substrate with the paste which is used. For many purposes, a paste containing about 15% by weight of the binder/volatile liquid solution is suitable.

Suitable methods of forming a layer of the paste on the substrate include, for example, screen printing, spraying, spinning and sedimentation. Screen printing is a very precise method that produces a layer having a smooth, even surface and a thickness of 10 to 50 μm depending on the mesh of the screen; this method is generally preferred.

Suitable electrically insulating substrate materials are, for example, alumina ceramics, fused silica and "Pyrex" glass (Trade Mark).

The coated substrate is then dried to remove the volatile liquid, preferably by heating in an oven at a temperature of about 100°C for about 10 minutes.

The dried coating is then sintered in a substantially inert atmosphere at a temperature of from 510°C to 800°C. For this purpose the coated substrate is preferably placed in a container through which a stream of nitrogen (or other inert gas) containing a small proportion of oxygen, preferably added as air, can be passed and the container is placed in a suitable oven or furnace, preferably an electrical furnace. The proportion of air in the inert gas/air mixture is suitably 1 to 3% by volume. The inert gas/air mixture is passed through the container at a relatively slow rate, for example 2 to 6 litres per hour.

The furnace is gradually heated to the sintering temperature, for example over a period of 30 minutes, and is held at the sintering temperature for 10 to 60 minutes, preferably 10 to 20 minutes. The sintering temperature does not appear to be critical; if the temperature is much less than 510°C, the layer fails to sinter and if it is more than 800°C, the layer decomposes. Best results are obtained at sintering temperatures of from 520°C to 700°C.

The sintered layers thus obtained are firm, adherent and chemically stable. A reduction of thickness takes place during the sintering operation and the final thicknesses are generally in the range of 5 to 25 μm, depending on the initial thickness of the layer. There is also always a loss of weight during sintering and the final chemical composition of the semiconductor may vary somewhat as a function of the sintering temperature and as a function of the sintering time.

In a modification of this process, the copper content of the semiconductor is not provided by the inclusion of copper chloride in the initial powder mixture, but is provided by evaporating a thin layer of copper metal on to the surface of the semiconductor layer after the latter has been applied to the substrate and dried and before it is fired (the copper chloride being omitted, in this case, from the initial powder mixture). During the firing stage, the thin layer of copper diffuses into the semiconductor layer so as to incorporate therein a very precise and uniform copper content. The thickness of the evaporated copper layer should be monitored during deposition by suitable apparatus, such as an Edwards evaporated film thickness monitor which is accurate to a resolution of 0.1 nm.

It is preferred to form evaporated copper layers having a thickness of from 0.5 nm to 2.0 nm which give rise to final copper contents of from 0.007% to 0.028%. It has been found that by using this method, the photosensitivity and speed of response of the semiconductor layer can be carefully and consistently controlled by varying the thickness of the evaporated copper layer by as little as 0.2 nm.

The sintered semiconductor layer is then provided with two spaced electrodes which can be made, for example, of silver, gold, indium, or aluminium or of an epoxy resin loaded with one of these metals. Suitable methods of forming the electrodes on the semiconductor include, for example, (a) evaporating the electrode metal on to the surface of the semiconductor, (b) screen printing the loaded epoxy resin on to the surface, and (c) pressing a foil of the metal on to the surface of the semiconductor.

Of these three methods, methods (a) and (b) are generally preferred. In both methods, the area between the electrodes is masked before applying the electrode material on to the surface of the semiconductor. Method (a) is usually followed by a short heat treatment which, when silver or aluminium is used, consists, for example, of heating the electrode layer in nitrogen at 300°C for 20 minutes. Method (b) requires that the epoxy resin is heated in air, for example, at 150°C for 35 minutes, in order to harden the layer.

Another method for providing the semiconductor with two spaced electrodes consists of forming the electrodes as layers on the electrically insulating substrate, for example, by any of the methods described above,

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while masking the area between the electrodes and then forming the semiconductor layer over the electrodes and the area of substrate between them.

This procedure, that is the provision of the electrode layers below the semiconductor layer, is preferred to the provision of the electrode layers over the semiconductor layer since the former procedure greatly increases the effective area of the electrodes (since the part of the semiconductor layer lying above the electrode layers can be illuminated and rendered conductive) which, in turn, significantly decreases the electric resistance of the electrodes to high surge currents.

In this procedure, the preferred electrode material is gold. A preferred method of forming gold electrode layers consists of silk screen printing a conventional fritless gold thick film conductor paste onto the surface and then firing the coated substrate at 900°C. Such fritless gold pastes typically comprise 99% pure finely powdered gold which when fired, fuse onto the surface of the substrate to form a robust conductive gold layer which is preferably approximately 5 μm in thickness.

An alternative, and less preferred, method of forming gold electrode layers is by evaporation.

We have found that the ability of electronic switches according to the invention to withstand electric field strengths in excess of 10kV/cm over a prolonged period is in most cases improved by providing a so-called "stress relieving" layer between the electrically insulating substrate and the semiconductor layer. Stress relieving coatings are used in electrical insulation technology to deal with the problems caused by uneven electrical fields across the surface of high voltage electrical insulators; they essentially comprise a material which exhibits non-linear resistance in that it permits a disproportionate increase in current with an increase in electrical potential. Suitable materials of this kind include, for example, finely divided zinc oxide and silicon carbide. The electrical characteristics of coatings containing these materials are largely determined by the size and density of the particles, rather than the electrical properties of each particle. Generally the materials show very little electrical conductivity up to a certain threshold value where conduction rapidly increases with a rise in electrical potential.

The procedure for forming a stress relieving layer on the substrate depends on whether the non-linear resistive material can be sintered to form a coherent and adherent layer at acceptable temperatures, that is up to, say, 1100°C. Zinc oxide can be sintered at temperatures of 1000-1100°C, but silicon carbide can not. Materials of the latter kind, such as silicon carbide, are mixed with a suitable electrically insulating vitreous glaze, such as a vitreous borosilicate glaze which can be sintered at a temperature of about 900°C.

A preferred zinc oxide-based stress relieving layer comprises, by weight:

zinc oxide	96.4%
manganese oxide	1.1%
bismuth oxide	1.0%
antimony oxide	1.0%
cobalt oxide	0.5%

Powders of these oxides are mixed and ground in a microliser, and the resulting powder mixture is mixed with turpineol or other suitable liquid medium to form a paste for screen printing as described above for the semiconductor layer. The paste is printed, dried and fired at a temperature of 1000°-1100°C in air to obtain a layer having a thickness of 8 to 10 μm.

For the other type of non-resistive material, such as silicon carbide, which cannot be sintered on its own, a range of electrically insulating vitreous glazes is commercially available and any of these glazes can be used provided they are compatible with the non-linear resistive material. The mixture of glaze and non-linear resistive material suitably comprises from 25 to 75% by weight of the latter; it has been found that the threshold value of the electrical characteristic can be changed by varying the relative proportions of these components.

In general, it is preferred to use a stress relieving layer which does not contain a glaze. With glaze-containing stress relieving layers, it is found that when the semiconductor layer is fired there is a tendency for components of the stress relieving layer to diffuse into the semiconductor layer and this has the effect of reducing the photosensitivity of the latter and in some cases of making the photosensitivity unstable. Products having zinc oxide-based stress relieving layers as described above are more photosensitive and much less subject to instability than are products comprising glaze-containing stress relieving layers.

The electronic switch according to the invention may take a number of forms. For reasons of compactness it is preferred that the semiconductor layer and the substrate should have the form of a hollow cylinder. It is further preferred that in this arrangement the semiconductor layer should be on the inside of the hollow cylinder and the light source should be located on the longitudinal axis of the cylinder.

A variety of light sources may be used. It is preferred to use one or more light emitting diodes (LEDs) or a glow discharge lamp or tube giving light having a wavelength of 500 to 900 nm. Suitable LEDs include high efficiency red LEDs with a peak emission of about 660 nm visible red light and a viewing angle of 90° or 140°, and infra-red LEDs which emit a peak emission of 830 nm and have a viewing angle of more than 30°.

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Suitable discharge lamps are, for example neon discharge lamps and tubes.

For the better understanding of the invention, preferred embodiments of semiconductor/substrate and of switch assemblies will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a plan view of a semiconductor/ substrate embodiment,

Figure 2 is a section on line II-II of Figure 1,

Figure 3 is a section similar to that of Figure 2 of a second semiconductor/substrate embodiment,

Figure 4 is a section similar to that of Figure 2 of a third semiconductor/substrate embodiment,

Figure 5 is a section similar to that of Figure 2 of a fourth semiconductor/substrate embodiment,

Figure 6 is a cross-section of a first embodiment of a cylindrical electronic switch assembly,

Figure 7 is a sectional elevation on line VII-VII of Figure 6,

Figure 8 is a cross-section of a second embodiment of a cylindrical electronic switch assembly, and

Figure 9 is a sectional elevation on line IX-IX of Figure 8.

Referring to Figures 1 and 2, a semiconductor/substrate assembly comprises a sintered photosensitive semiconductor layer 1 coated on a flat electrically insulating substrate 2 and spaced electrically conducting electrodes 3A and 3B. The semiconductor layer 1 has the Cd/Se/Te/S/Cl/Cu composition referred to above.

The semiconductor/substrate assembly shown in Figure 3 is similar to that shown in Figures 1 and 2, but additionally comprises an electrical stress relieving layer 4 as described above.

The semiconductor/substrate assembly shown in Figure 4 is generally similar to that shown in Figure 3, but the electrically conducting electrodes 3A and 3B are positioned directly on the substrate 2 and are overlaid by the semiconductor layer 1 and the stress relieving layer 4.

In this arrangement, the electrodes are preferably formed of gold as described above. In a specific embodiment of this arrangement, the stress relieving layer 4 overlaps each electrode 3A, 3B by approximately 2 mm and the semiconductor layer overlaps each electrode by 2 to 3 mm.

The semiconductor/substrate assembly shown in Figure 5 is again generally similar to that shown in Figure 3, the whole of the substrate 2 being covered by the stress relieving layer 4. The electrodes 3A and 3B are formed on the stress relieving layer 4 and the semiconductor layer 1 overlaps the electrodes 3A and 3B. In this arrangement, the electrodes are preferably formed of gold as described above.

As previously indicated, the advantage of the arrangements shown in Figures 4 and 5 over the arrangements shown in Figures 1, 2 and 3 is that the former (Figures 4 and 5) allows the portions of the semiconductor layer which overlie the electrodes 3A, 3B to be illuminated and thus rendered conductive. The contact area between the semiconductor layer and the electrode layers is, therefore, greatly increased.

Of the two arrangements shown in Figures 4 and 5, that of Figure 4 is preferred. The arrangement of Figure 5 is, however, necessary if the stress relieving layer 4 needs to be fired at a temperature in excess of the sintering temperature used for forming the electrode layers 3A, 3B.

The electronic switch shown in Figures 6 and 7 comprises an adherent sintered photosensitive semiconductor layer 11 and an insulating substrate 12 in the form of a hollow cylinder, and two annular electrodes 13A and 13B at each end of the cylinder. The switch further comprises a light source 14 which is a discharge tube giving light having a wavelength of 500 to 900 nanometers; the light source 14 is arranged along the axis of the cylinder 11/12. The semiconductor layer 11 has the Cd/Se/Te/S/Cl/Cu composition referred to above.

The electronic switch shown in Figures 8 and 9 comprises hollow cylindrical semiconductor layer 21 and insulating substrate 22 similar to the semiconductor layer 11 and the substrate 12 of the previous embodiment, but in this embodiment the electrodes take the form of two elongated strip electrodes, 23A and 23B, arranged along diametrically opposed generators of the cylinder 21. The switch assembly further comprises six light emitting diodes 24 arranged along the axis of the cylinder 21/22. The semiconductor layer 21 has the Cd/Se/Te/S/Cl/Cu composition referred to above.

The operation of the electronic switches shown in Figures 6 and 7 and Figures 8 and 9 is as follows. A bias voltage is applied across the electrodes (13A-13B, 23A-23B); no significant current flows as long as the light source (14,24) is not illuminated and as soon as it is illuminated the current passes.

Electronic switches as illustrated can be made very compact. The properties of the semiconductors described are such that the switches can safely handle voltage pulses of up to 30 kV and DC voltages of up to 30 Kv with a spacing between the electrodes of as little as 10 or 20 mm.

In order that the invention may be more fully understood, the following example, in which all percentages are by weight unless otherwise stated, is given by way of illustration only.

Example 1

A powder mixture of the following composition :

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cadmium selenide	33.3%
cadmium sulphide	47.7%
tellurium	10%
cadmium chloride	8.92%
copper (cupric)	chloride 0.08%

was formed and then dry ground in a mechanical grinder, such as a microliser, to obtain a homogeneous mixture in which all particles were less than 3 um in size.

A 10% solution of ethyl cellulose in turpineol was mixed with the powder mixture, the amount of the solution being 15% of the combined weights of the solution and the powder mixture. Mixing was continued until a smooth paste was obtained.

The paste was applied to the surface of a high density 96% alumina ceramic substrate of the kind used for the production of thick film circuits, by silk screen printing. The substrate had the dimensions 5cm x 3.5cm x 0.05 cm and the paste was printed to cover a rectangular area of 4cm x 2.5cm. A 305 mesh screen material was used which gave a layer of paste approximately 15 um in thickness.

The coated substrate was placed in an oven and heated to 100°C for 10 minutes to evaporate the turpineol.

The coated substrate was then placed in a Pyrex glass container having a top cover of the same material. Gas could be introduced into one end of the container through a Pyrex glass tube and could be vented from the opposite end through a gap between the container and its top cover. This assembly was placed in an electrically heated furnace.

Prior to heating, pure nitrogen was first passed through the container at a flow rate of 4.5 litres per hour for a period of 20 minutes to purge out the bulk of the air that was initially present. The furnace was then heated to 520°C over a period of 50 minutes while continuing to pass pure nitrogen. Once a temperature of 520°C has been attained, a small proportion of air, that is 3% by volume, was added to the nitrogen and flow of this mixture was continued at 4.5 litres per hour. The temperature of 520°C was maintained for 10 minutes and at the end of this period,

the furnace was turned off and allowed to cool over a period of 60 to 90 minutes. The flow of the nitrogen/air mixture is continued until the furnace had cooled to below 150°C. Thereafter air could be blown through the furnace to accelerate cooling.

The sintered layer obtained was firm, adherent and chemically stable. There was an approximately 40% reduction in the thickness of the layer. Electron microscope studies of the surface of the sintered material showed that the latter consisted primarily of large grains of about 9 um fused together at the grain boundaries.

Indium was then evaporated onto the marginal portions of the long sides of the substrate to form electrodes. For this purpose a metal mask was positioned to cover all of the sintered composition apart from a 1.5 mm wide marginal zone along each long edge. Indium was then evaporated using a conventional metal evaporation apparatus to coat the masked substrate. The mask was then carefully removed; the thickness of the indium coating was 0.5 um. The coated substrate was placed in an oven and heated to 160°C for 15 minutes to cause fusion of the indium to the surface of the sintered composition.

The final product accordingly had a band of the sintered composition about 17mm wide (between the long sides of the substrate) and an indium electrode strip about 4 mm wide on either side of the sintered composition and extending to the long edges of the substrate.

To form the switch, six light emitting diodes (LEDs) of the visible light type were mounted on a piece of printed circuit board measuring 5cm x 3.5cm in two rows of three running across the width of the board. Each row was positioned with its centre at 1.8cm from each end and the LEDs were arranged to be equally spaced along the length of the row. Each row of three LEDs was connected electrically in series and the two rows were connected in parallel to form a common drive connection. The array of LEDs was mounted over the surface of the semiconductor on the substrate with a spacing of 3mm from the surface to the tip of each LED. The assembly of the LEDs board and the coated substrate were mounted in a rigid plastics frame that electrically insulated the coated substrate from the LEDs. Electrical connections were made to the indium electrodes on each edge of the substrate. The whole assembly was then immersed in transformer oil to prevent electrical flashover from occurring across the surface of the semiconductor layer.

The LEDs used were high efficiency red diodes with a peak emission of 660 nm visible red light and a viewing angle of 140°. Their light output for a current of 20 ma was 200 mcd (0.2 candela); for pulsed current operation, the light output for 100 ma pulses was typically 1 candela at 25°C.

The electrical properties of the switch were as follows:

Dark Conditions:

The following properties were recorded with the switch immersed in transformer oil at a temperature of 25°C

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and in total darkness.

For a DC voltage of 30 kV applied across the semiconductor contacts, a current of less than 30uA was recorded; this corresponds to a switch dark resistance of more than 1000 mega ohms.

Electrical breakdown of the semiconductor occurred at a DC voltage of 35-40 kV from tests carried out on several samples.

Illuminated Conditions:

The following properties were recorded with the switch immersed in transformer oil at a temperature of 25°C and the following illumination conditions.

Diode Forward Current,

current pulses of 3 ms duration and magnitudes greater than 0.15, at pulse repetition frequency 50 per second.

Time response Test

A 500 volt DC bias was applied across the semiconductor layer contacts and the above forward current conditions applied to the diodes causing pulses of current to be generated in the 500 volt bias circuit. The characteristics of these pulses were as follows:

peak current recorded;	1.5 mA
time from minimum current to maximum current where zero time marks the beginning of the illumination pulse	0.75ms
time for the current to fall to 1% of the peak value following termination of the diode current pulse	5.7 ms
estimated minimum resistance	270,000 ohms

Claims

1. An electronic switch comprising a photosensitive semiconductor and a light source which, when actuated, illuminates the semiconductor and causes the latter to become conductive, in which the photosensitive semiconductor is a sintered mixture comprising, by weight, 58 to 72% of cadmium, 14.8 to 21% of selenium, 7 to 15% of tellurium, 7 to 12% of sulphur, 0.1 to 1% of chlorine, and 0.005 to 0.1% of copper.

2. A switch according to claim 1, in which the semiconductor is in the form of an adherent layer on an electrically insulating substrate.

3. A switch according to claim 2, which comprises two adherent, spaced electrode layers on the sintered semiconductor layer.

4. A switch according to claim 1, which comprises an electrically insulating substrate, two adherent, spaced electrode layers on the substrate, and an adherent layer of the sintered semiconductor composition overlying the electrode layers and the substrate between them.

5. A switch according to claim 3 or 4, in which the electrode layers are formed of silver, gold, indium or aluminium or an epoxy resin loaded with silver, indium or aluminium.

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6. A switch according to any of claims 2 to 5, in which a stress relieving layer is provided between the electrically insulating substrate and the sintered semiconductor layer, the stress relieving layer being adherent to the substrate and comprising a finely divided non-linear resistive material.

7. A switch according to claim 6, in which the stress relieving layer consists essentially of a sintered layer of zinc oxide.

8. A switch according to claim 6, in which the stress relieving layer consists essentially of a sintered mixture of silicon carbide and an electrically insulating vitreous glaze.

9. A switch according to any of claims 2 to 8, in which the semiconductor layer and the substrate and the stress relieving layer, if present, have the form of a hollow cylinder.

10. A switch according to claim 9, in which the light source is located on the longitudinal axis of the cylinder.

11. A switch according to any of claims 1 to 10, in which the light source is one or more light emitting diodes.

12. A switch according to any of claims 1 to 10, in which that the light source is a glow discharge lamp or tube giving light having a wavelength of 500 to 900 nanometers.

13. A method of making an electronic switch according to claim 1, which comprises forming a paste of a finely divided powder mixture comprising, by weight, 32 to 47% of cadmium selenide, 32 to 49% of cadmium sulphide, 7 to 15% of tellurium, 4.7 to 13% of cadmium chloride, and 0.01 to 0.1% of copper chloride, a binder and a volatile liquid, forming a coating of the paste on an electrically insulating substrate and drying the coating, sintering the dried coating at a temperature of from 510°C to 800°C to form an adherent layer of photosensitive semiconductor on the substrate, providing adherent spaced electrode layers either on or below the semiconductor layer, and assembling the coated substrate with a light source.

14. A method of making an electronic switch according to claim 1, which comprises forming a paste of a finely divided powder mixture comprising, by weight, 32 to 47% of cadmium selenide, 32 to 49% of cadmium sulphide, 7 to 15% of tellurium, and 4.7 to 13% of cadmium chloride, a binder and a volatile liquid, forming a coating of the paste on an electrically insulating substrate, drying the coating, evaporating a layer of copper metal on the surface of the dried coating, the thickness of the copper layer being such as to provide the desired final copper content when the copper is diffused through the semiconductor layer, sintering the copper coated coating at a temperature of from 510°C to 800°C to form an adherent layer of photosensitive semiconductor on the substrate and to diffuse the copper through said layer, providing adherent spaced electrode layers either on or below the semiconductor layer, and assembling the coated substrate with a light source.

15. A method according to claim 13 or 14, in which the substrate is coated with an electrical stress relieving layer comprising a material which exhibits non-linear resistance and the photosensitive semiconductor layer is formed on the stress relieving layer.

16. A method according to claim 16, in which the stress relieving layer is formed by sintering a powder layer consisting essentially of zinc oxide.

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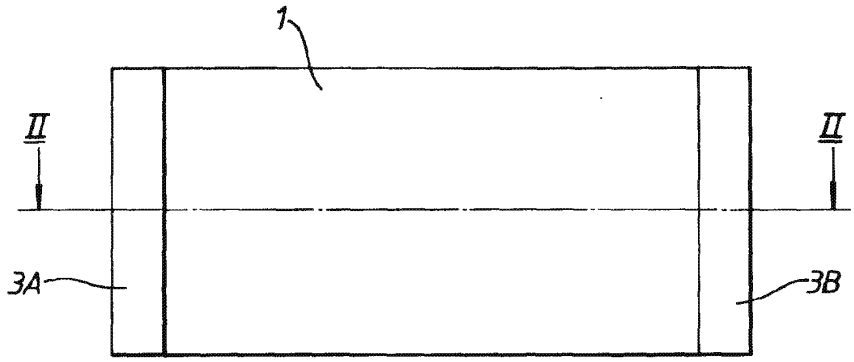


Fig.1.

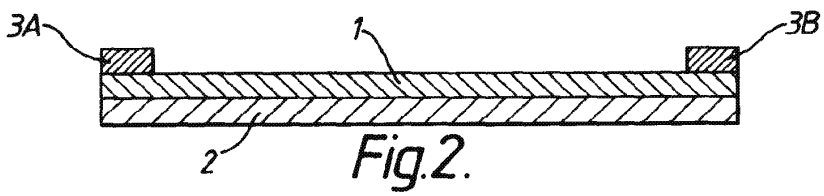


Fig.2.

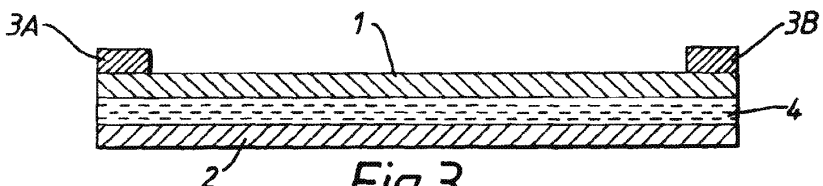


Fig.3.

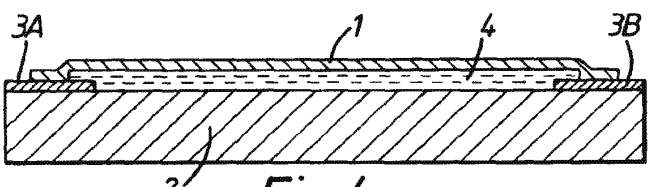


Fig.4.

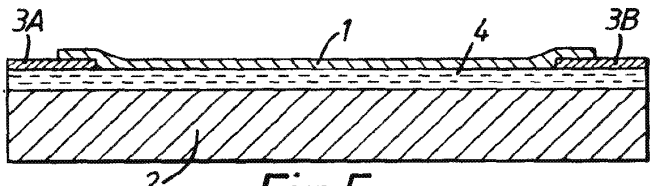


Fig.5.

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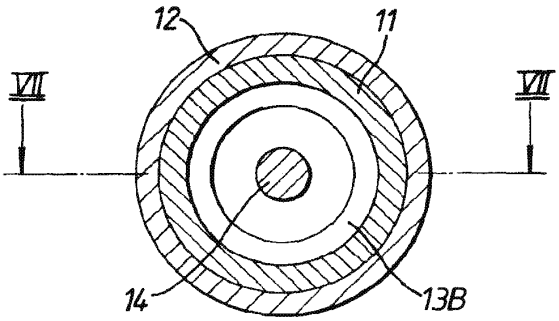


Fig. 6.

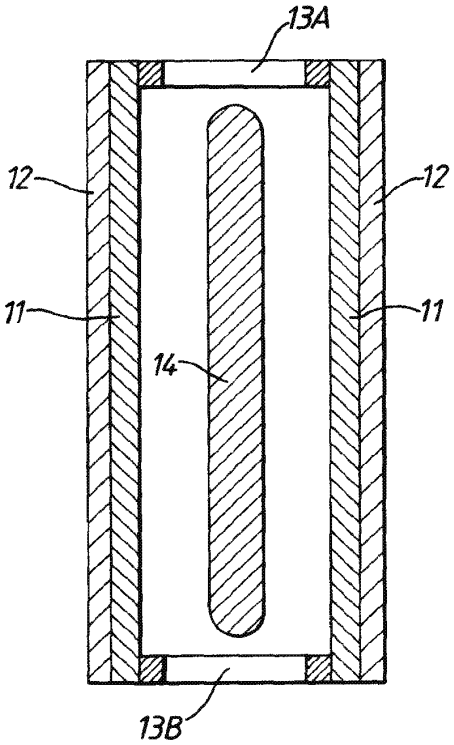


Fig. 7.

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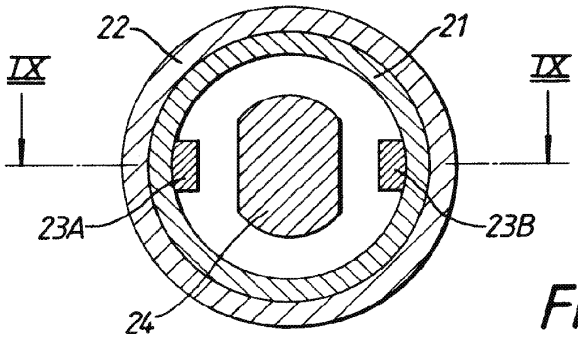


Fig. 8.

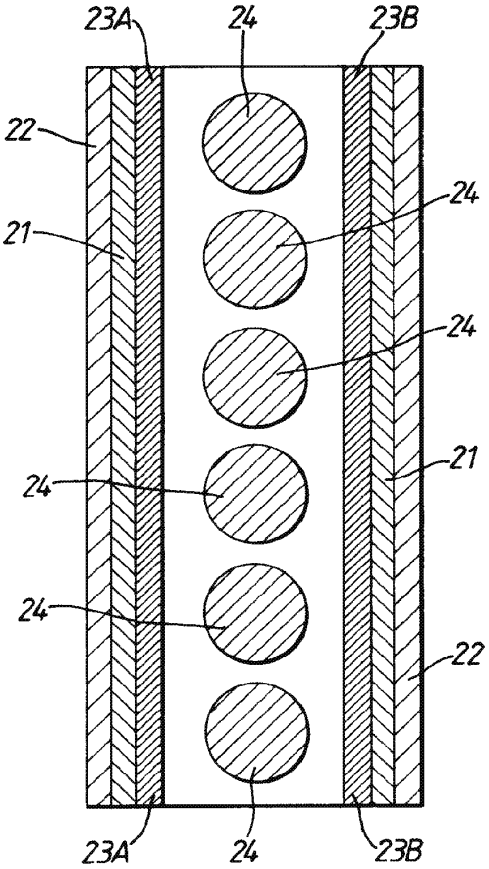


Fig. 9.

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(54) **Infrared sensor and method for production thereof.**

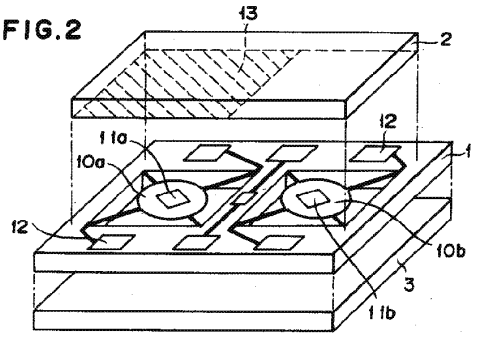
(57) The disclosed infrared sensor comprises substrate provided with a bridging part and a sensing part made of an infrared temperature-sensitive film formed in the bridging part. A first lid member covers the sensing part and bridging part and a second lid member covers the reverse surface of the substrate and tightly seals a cavity formed between the substrate and the bridging part.

The invention preferably comprises an electrode pad electrically connected to the infra red temperature sensitive film and formed of a laminate film including an etchant-resistant electrically conductive film.

The invention provides an infrared sensor with a small stable bridging structure which allows easy formation of a contact hole on an electrode pad witout causing a breakage of the bridging part.

A method for the production of an infrared sensor is also disclosed.

FIG.2



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BACKGROUND OF THE INVENTION

Field of the Invention:

This invention relates to an infrared sensor for the non-contact measurement of the temperature of a given object and a method for the production thereof. More particularly, it relates to an infrared sensor provided on an infrared temperature-sensing film with an electrode and a method for the production thereof. Description of the Prior Art:

Recently, various techniques have been developed for the production of infrared sensors usable ideally for non-contact thermometers, for example, by effective use of the technique of microfine fabrication of semiconductors. The infrared sensors come in various types such as, for example, those of the thermobolometer type and the thermopile type. The infrared sensors of the thermobolometer type are superior to those of other types in allowing easy dimensional reduction because of the fact that their sensitive film which is made of a substance fulfilling the function of a thermistor, is capable of measuring an increase in temperature caused by the incidence of infrared radiation by measuring a change in the magnitude of electrical resistance and consequently determining the amount of the infrared radiation.

In the infrared sensor of the thermobolometer type, if the infrared temperature-sensitive film of the sensor has a small heat capacity, the amount of heat transmitted outwardly from the film decreases, the temperature rises remarkably and the response of the sensor to a minute amount of infrared radiation gains in sensitivity in proportion. The conventional infrared sensor of the thermobolometer type, therefore, has been constructed so that an extremely small bridging part is formed on a supporting substrate made of a semiconducting material and an infrared sensitive film is formed on the bridging part by the microfine fabrication technique. To be specific, the bridging structure keeps a temperature-sensing part of the sensor afloat from the supporting substrate for the purpose of improving the response sensitivity of the sensor.

The infrared sensor requires various contrivances for the sake of measurement because it is intended to handle a very minute amount of infrared radiation emitted from a given object. For example, one infrared sensor is provided with two entirely identical infrared temperature-sensitive films having bridging structures; one of the films is exposed to the incidence of infrared radiation and the other shielded from the infrared radiation. By constantly comparing the output of the infrared temperature-sensitive film exposed to the infrared radiation and the output of the infrared temperature-sensitive film shielded from the infrared radiation, the infrared sensor is enabled to exclude the electrical noise and thermal disturbance and detect the net amount of infrared radiation.

The infrared sensor of this type is furnished with various contrivances so as to ensure an efficient incidence of infrared radiation on the exposed infrared sensitive film. From the practical point of view, however, the infrared sensor requires the minute bridging structure formed therein to be protected mechanically and physically. Heretofore, for the protection of the bridging structure, the practice of keeping the infrared sensor device in such a container as a can has been commonly used.

The conventional infrared sensor has the sensor element thereof kept in a container as described above. When the sensor accommodated in the container as described above is used as a non-contact thermometer, it poses problems in relation to thermal conductivity, restriction in size, and cost of production. Thus, there is a need for a packaging method which allows the sensor element to be protected as required by a simple procedure at a low cost.

In the infrared sensor of this kind, for the purpose of ensuring selective incidence of the infrared radiation on one of the pair of infrared temperature-sensitive films, the sensor element is required to have on the front side thereof, a lid as means for effecting the selective incidence of infrared radiation. In the meantime, the sensor element generally has on the reverse side thereof an opening of desired shape and size formed during the fabrication of the bridging structure so as to allow anisotropic etching such as, with an aqueous hydrazine solution. This opening is likewise preferably sealed with a lid to diminish the otherwise inevitable effect of reflection and absorption of infrared radiation through the opening.

To cope with the situation, the following measure has been conceived. Some hundreds of sensor elements are simultaneously incised in one silicon wafer and the sensor elements still held on the wafer are tested for electrical properties as with a probe to discriminat between conforming and non-conforming articles. Thereafter, the sensor elements are severally cut off the wafer with a dicing saw. Each of the separated sensor elements is then washed, with a lid joined to the front side (the side for admitting the incident infrared radiation) thereof and another lid joined to the rear side thereof.

This method, however has the following problems. For example, at the step of cutting the silicon wafer with the dicing saw, the practice of feeding cooling water to the dicing saw for the purpose of removing the heat generated between the chip and the rotary blade, lubricating the dicing saw, and

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ensuring chip ejection is prevalent. This cooling water causes breakage of the bridging structure. In this case, the breakage of the bridging structure can be precluded by precoating the chip with electron wax. Since the chip must be subsequently cleaned of this wax as by washing, the impact of this washing brings about breakage of the bridging structure.

In the conventional infrared sensor, the possible loss of the energy of the infrared radiation impinging on the infrared temperature-sensitive film is avoided by having this infrared temperature-sensitive film formed on the minute bridging structure as described above. Since the energy of the infrared radiation impinging on the infrared temperature-sensitive film is lost through the air which envelopes the infrared temperature-sensitive film, the problem arises that an infrared sensor which excels in practical utility and possesses high sensitivity cannot be obtained simply by imparting a bridging structure to the infrared temperature-sensitive film.

Two methods are available for the formation of the bridging structure. One of them comprises the steps of forming an excavated part in a sensor substrate, temporarily refilling the excavated part thereby forming a sacrificial layer, forming on this sacrificial layer a pattern for the bridging structure, forming an infrared temperature-sensitive film on the pattern, and then removing the sacrificial layer while leaving the formed bridging part behind. The other method comprises the steps of forming on one surface of a sensor substrate a pattern for a bridging part and an infrared temperature-sensitive film and performing an anisotropic etching on the other surface of the sensor substrate thereby forming a cavity below the bridging pattern and completing the bridging structure. The latter method is easier procedurally than the former method.

Incidentally, in the latter method, hydrazine or an aqueous potassium hydroxide solution is used to effect the anisotropic etching. Since this etchant is strongly alkaline, it dissolves not only the silicon as the material for the sensor substrate but also materials other than silicon such as, for example, aluminum which is generally used as the material for electrodes and conductors. Thus, the manufacture of the bridging structure needs to resort to the following method, for example.

This method comprises the steps of forming an insulating film intended to form a bridging part on a silicon substrate destined to form a sensor substrate, superposing an infrared temperature-sensitive film on the insulating film, forming thereon a wiring layer and an electrode pad both of aluminum, coating the entire surface with a protective film (insulating film), then carrying out the anisotropic etching selectively on the rear surface of the silicon substrate thereby forming a bridging part, subsequently boring a contact hole in the protective film on the upper surface of the silicon substrate to a depth reaching the electrode pad, and electrically connecting the electrode pad and a flexible printed substrate (FPC) by soldering through the medium of the contact hole.

An object of this invention, therefore, is to provide an infrared sensor which is furnished with a stable bridging structure and is small and inexpensive and a method for the production thereof.

Another object of this invention is to provide a method for the production of an infrared sensor which allows easy formation of a contact hole on an electrode pad without involving breakage of a bridging part.

A further object of this invention is to provide an infrared sensor such that during the process of etching for the formation of electrodes, the phenomenon of side etching if allowed to occur will produce no gap between electrodes and an insulating film or no dispersion in the magnitude of electrical resistance of an infrared temperature-sensitive film.

Yet another object of this invention is to provide an infrared sensor of high sensitivity which enables the amount of energy lost through the periphery of the infrared temperature-sensitive film to be minimized.

SUMMARY OF THE INVENTION

The objects mentioned above are accomplished by an infrared sensor which comprises a substrate provided with a bridging part, a sensing part made of an infrared temperature-sensitive film formed in the bridging part, a first lid member covering the sensing part and the bridging part, and a second lid member covering the reverse surface of the substrate and tightly sealing a cavity formed between the substrate and the bridging part.

This invention contemplates the infrared sensor mentioned above in a construction such that it further comprises an electrode pad electrically connected to the infrared temperature-sensitive film and formed of a laminate film including an etchant-resistant electrically conductive film. This invention also contemplates the infrared sensor mentioned above in a construction such that it further comprises an infrared temperature-sensitive film formed through the medium of a first insulating film on the substrate, a second insulating film formed on the infrared temperature-sensitive film and provided therein with a contact hole deep enough to reach the infrared temperature-sensitive film, and an electrode formed on the second insulating film, electrically connected to the infrared temperature-sen-

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sitive film through the medium of the contact hole, and furnished on the second insulating film with a part having a width greater than the width of the part inside the contact hole.

The objects described above are accomplished by a method for the production of an infrared sensor which comprises a step of forming on a semiconductor wafer a plurality of sensor elements provided on a bridging part with an infrared temperature-sensitive film, a step of tightly sealing the sensor elements severally with lid members, and a step of cutting the semiconductor wafer to separate the tightly sealed sensor elements asunder.

The objects described above are also accomplished by a method for the production of an infrared sensor which comprises a step of forming a first insulating film intended to form a bridging part on one of the main surfaces of a sensor substrate made of a semiconducting material and a second insulating film containing an opening for etching on the other main surface of the sensor substrate, a step of forming an infrared temperature-sensitive film on the first insulating film, a step of forming on the first insulating film an electrode pad provided in the uppermost layer thereof with an etchant-resistant electrically conductive film in such a manner as to be electrically connected to the infrared temperature-sensitive film, a step of forming a third insulating film on the sensor substrate including the electrode pad and selectively forming in the third insulating film a contact hole deep enough to reach the electrode pad, and a step of anisotropically etching the sensor substrate through the opening mentioned above after the formation of the contact hole thereby forming a bridging part.

The objects described above are further accomplished by a method for the production of an infrared sensor which comprises a step of forming a first insulating film on the obverse surface of a sensor substrate and then forming an infrared temperature-sensitive film on the insulating film, a step of forming a second insulating layer in such a manner as to cover the infrared temperature-sensitive film, a step of forming a first etchant-resistant film containing a prescribed contact hole pattern on the second insulating film and etching the second insulating film while using the first etchant-resistant film as a mask thereby forming in the second insulating film a contact hole deep enough to reach the infrared temperature-sensitive film, a step of superposing an electrically conducting layer on the second insulating film having the contact hole formed therein, and a step of forming on the electrically conductive layer a second etchant-resistant film containing an electrode pattern having a greater width than the contact hole pattern of the first etchant-resistant film and etching the electrically conductive layer with the second etchant-resistant film as a mask thereby forming an electrode.

The objects described above are further accomplished by an infrared sensor which comprises a sensor substrate containing a cavity and having an infrared temperature-sensitive film disposed in the cavity and vacuum sealing means covering the cavity in the sensor substrate and sealing the infrared temperature-sensitive film so as to keep the periphery thereof in a vacuum state.

In the infrared sensor of this invention, since the sensing part is constructed by forming the infrared temperature-sensitive film on the bridging part and, at the same time, tightly sealing the sensing part, the bridging part and the infrared temperature-sensitive film inside the sensor proper can be protected infallibly and a small infrared sensor can be produced inexpensively.

Further since the infrared sensor of this invention is provided with a sensor substrate made of a semiconducting material and furnished with a bridging part, an infrared temperature-sensitive film formed on the bridging part of the sensor substrate, and an electrode pad electrically connected to the infrared temperature-sensitive film and formed of a laminate film including an etchant-resistant electrically conductive film, the electrode pad can be anisotropically etched with a strong alkali liquid after the formation of a contact hole therein and, as a result, the bridging part can be stably obtained.

In the infrared sensor of this invention, since the part of the electrode on the infrared temperature-sensitive film which rises above the second insulating film is given a width larger than the width of the part of the electrode which lies within the contact hold, no gap is formed between the electrode and the second insulating film and no dispersion in the magnitude of electrical resistance of the infrared temperature-sensitive film is allowed.

In the method of this invention for the production of the infrared sensor, since the lid members are disposed so as to seal tightly the bridging parts and the infrared temperature-sensitive film in the sensor elements before the sensor elements are separated asunder, possible leakage of cooling water into the sensor elements during the process of separation can be avoided. This method, therefore, is effective in preventing the bridging parts in the sensor elements from breakage, notably improving the yield of production, and enhancing the ease of handling of the produced sensor elements.

By the method of this invention for the production of an infrared sensor, an electrode pad provided in the uppermost layer thereof with an etchant-resistant electrically conductive film is formed and a contact hole is bored therein before the anisotropic etching with a strong alkali liquid is

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carried out. Since the etchant-resistant electrically conductive film is already formed in the uppermost layer of the electrode pad when the anisotropic etching commences, this method is effective in precluding the possibility of the electrode pad being dissolved with the etchant and the bridging part being broken consequently and improving the yield of production.

The method of this invention for the production of an infrared sensor comprises a step of forming a first insulating film on the obverse surface of a sensor substrate and then forming an infrared temperature-sensitive film on the insulating film, a step of forming a second insulating film in such a manner as to cover the infrared temperature-sensitive film, a step of forming on the second insulating film a first etchant-resistant film containing a prescribed contact hole pattern and etching the second insulating film while using the first etchant-resistant film as a mask thereby boring a contact hole in the second insulating film to a depth sufficient to reach the infrared temperature-sensitive film, a step of superposing an electrically conductive layer on the second insulating film having the contact hole bored therein, and a step of forming on the electrically conductive layer a second etchant-resistant film containing an electrode pattern having a larger width than that of the contact hole pattern of the first etchant-resistant film and etching the electrically conductive layer with the second etchant-resistant film as a mask thereby forming an electrode. Even when the phenomenon of side etching is allowed to occur in the electrically conductive layer during the process of etching the electrically conductive layer with the second etchant-resistant film as a mask, it is prevented from producing a gap between the electrode and the second insulating layer, and thereby damaging the infrared temperature-sensitive film, or causing dispersion in the magnitude of electrical resistance.

Since the infrared sensor of this invention seals the infrared temperature-sensitive film so tightly as to keep the periphery thereof in a vacuum state as described above, it is capable of minimizing the amount of infrared radiation energy lost through the infrared temperature-resistant film and is effective in notably enhancing the sensitivity of the sensor.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a perspective view of an infrared sensor as one embodiment of this invention.

Fig. 2 is a perspective view illustrating the infrared sensor of Fig. 1 in a disassembled state.

Figs. 3A - 3J are longitudinal cross sections representing a series of steps followed in the production of the infrared sensor shown in Fig. 1.

Fig. 4 is a longitudinal cross section illustrating an infrared sensor as another embodiment of this invention.

Figs. 5A to 5I are longitudinal cross sections representing a series of steps followed in the production of the infrared sensor shown in Fig. 4.

Fig. 6 is a longitudinal cross section illustrating an infrared sensor as yet another embodiment of this invention.

Fig. 7 is a plan view illustrating an infrared sensor as still another embodiment of this invention.

Fig. 8 is a cross section taken through Fig. 7 along line VIII-VIII.

Figs. 9A to 9E are cross sections representing a series of steps followed in the production of the infrared sensor shown in Fig. 7.

Fig. 10 is a longitudinal cross section illustrating an infrared sensor as a further embodiment of this invention.

Fig. 11 is a diagram schematically illustrating the construction of a system used in the first example experiment conducted on this invention.

Fig. 12 is a graph showing the results of the test performed in the system of Fig. 11 and in vacuum.

Fig. 13 is a graph showing the relationship between the degree of vacuum and the magnitude of temperature increase in comparison with the test results obtained in the open air.

Fig. 14 is a cross section illustrating the construction of a package used for the second example of experiment conducted on this invention.

Fig. 15 is a graph showing the results of the second example of experiment.

DESCRIPTION

As the supporting substrate for the sensor proper, substrates of such semiconductors as silicon and germanium are used. Preferably, silicon substrates which can be obtained easily and inexpensively are used. The infrared temperature-sensitive film is formed of a film of amorphous germanium (a-Ge), polycrystalline geranium, amorphous silicon (a-Si), or polycrystalline silicon, for example. For the formation of this infrared temperature-sensitive film, such techniques as spattering, ion beam sputtering, and CVD (chemical vapor deposition) are available.

The bridging part can be formed of silicon oxide film (SiO_x), silicon nitride film (SiNy), or silicon oxynitride film (SiO_xN_y), for example. Preferably, it is formed of silicon oxynitride film. The silicon oxynitride film combines the properties of both silicon oxide film and silicon nitride film and, therefore, enjoys ideal stress balance and allows formation of a stable bridging structure. For the

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formation of the bridging part, a method which comprises forming an excavated part in the supporting substrate, temporarily refilling the excavated part thereby forming a sacrificial layer, forming a pattern of the bridging part on the sacrificial layer and, at the same time, forming an infrared temperature-sensitive film on the bridging part pattern, and then removing the sacrificial layer and giving rise to the bridging part is available. Another method which comprises forming a pattern for the bridging part and an infrared temperature-sensitive film on one of the surfaces of the supporting substrate, etching the other surface of the supporting substrate thereby forming a cavity under the bridging part pattern thereby giving rise to the bridging part, and further forming a lid member on the other surface in such a manner as to cover the cavity is also available. The latter method is easier to carry out from the procedural point of view than the former method.

As the material for the lid member, various semiconductor substances such as silicon and various metallic substances are usable. A silicon substrate is preferably used because of its low price and stable quality. When the lid member is made of the silicon substrate and it is used in a thermometer for the measurement of a body temperature, the transmittance of this lid member to infrared radiation of a wavelength of about 10 μm emanating from the human body is about 50%. When the infrared sensor is constructed by installing two identical infrared temperature-sensitive films in the sensor proper, exposing one of the infrared temperature-sensitive films to infrared radiation, and shielding the other infrared temperature-sensitive film from the infrared radiation, the side of the sensor proper which is covered with the lid member must be furnished with an infrared-intercepting film which is formed of aluminum (Al), for example.

The method of this invention for the production of an infrared sensor comprises a step of forming on a semiconductor wafer a plurality of sensor elements provided on a bridging part thereof with an infrared temperature-sensitive film, a step of tightly sealing the sensor elements individually with lid members, and a step of separating the tightly sealed sensor elements asunder.

By this method of production, since the sensor elements are tightly sealed individually with the lid members prior to the step of separating them as under (dicing step) and in the subsequently assumed state of being cut off by dicing, invasion by cooling water can be prevented and the bridging parts thereof are protected against breakage. When the produced infrared sensor is exposed to the impact of handling or it is incorporated into the probe, the possibility of the bridging part being broken by the shock is avoided because it is protected with the lid member.

Though adhesive agent or solder is usable for the union of the lid member with the sensor proper, this union may be obtained by the method of anode bonding. This method allows elimination of the effects of air convection and improves the sensor properties because it is capable of tightly sealing the sensor proper so as to keep the interior thereof in a vacuum state.

Further, in the infrared sensor according to this invention, the contact hole is formed on the electrode pad and the electrode pad is exposed because the electrode pad is formed so as to include therein an etchant-resistant electrically conductive film.

By the method of this invention, the possibility of the electrode pad being dissolved with the etching liquid is nil because the etchant-resistant electrically conductive film has been already formed in the uppermost layer of the electrode pad when the anisotropic etching is carried out with such a strong alkali liquid as hydrazine after the formation of the contact hole in the third insulating film on the electrode pad. Since the formation of the contact hole is not required to follow the formation of the bridging part, the bridging part is not broken and the yield of production is improved.

The electrode pad is generally formed of an aluminum (Al) film. For the etchant-resistant film of the uppermost layer, a copper (Cu) film or a gold (Au) film is used. When the etchant-resistant film is formed of a copper film, it is preferably overlaid with a nickel (Ni) film for prevention from oxidation.

In the infrared sensor produced in accordance with this invention, the upper peripheral part of the contact hole formed on the second insulating film is so shaped as to be covered with the part of the electrode which is given an increased width. In the structure of this kind, even when the phenomenon of side etching is allowed to occur during the fabrication of the electrode by etching, it only narrows the part of increased width and avoids inserting a gap between the electrode and the second insulating film, corroding the infrared temperature-sensitive film, or causing dispersion in the magnitude of electrical resistance.

The method of this invention for the production of an infrared sensor comprises a step of forming a first insulating film on the surface of a sensor substrate and then superposing an infrared temperature-sensitive film on the insulating film, a step of forming a second insulating film in such a manner as to cover the infrared temperature-sensitive film, a step of forming a first etchant-resistant film containing a prescribed contact hole pattern on the second insulating film and etching the second insulating film while using the first etchant-resistant

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film as a mask thereby producing in the second insulating film a contact hole deep enough to reach the infrared temperature-sensitive film, a step of superposing an electrically conductive layer on the second insulating film having the contact hole formed therein, and a step of forming on the electrically conductive layer a second etchant-resistant film containing an electrode pattern having a greater width than the contact hold pattern of the first etchant-resistant film and etching the electrically conductive layer with the second etchant-resistant film as a mask thereby forming an electrode.

By this method, the electrode pattern of the second etchant-resistant film has a greater width than the contact hole pattern of the first etchant-resistant film when the electrically conductive layer is etched with the second etchant-resistant film as a mask. Even when the phenomenon of side etching is allowed to occur in the electrically conductive layer, the method prevents the insertion of a gap between the electrode and the second insulating film, corroding of the infrared temperature-sensitive film, or causing dispersion in the magnitude of electrical resistance.

Now, the present invention will be described specifically below with reference to embodiments illustrated in the annexed drawings.

Fig. 2 is a perspective view illustrating an infrared sensor as one embodiment of this invention, in a state ready for assembly. Fig. 1 illustrates this infrared sensor in an assembled state.

The infrared sensor of this embodiment is constructed by joining a front lid 2 to the obverse surface of a sensor proper 1 and a rear lid 3 to the reverse surface thereof. The sensor proper 1 is provided with a pair of bridging parts 10a, 10b perfectly identical in construction. On the central parts of these bridging parts 10a, 10b, infrared temperature-sensitive films 11a, 11b are respectively formed. A plurality of electrode pads 12 are disposed around the bridging parts 10a, 10b and these electrode pards 12 are electrically connected to the infrared temperature-sensitive films 11. The front lid 2 is formed of a silicon substrate of a size slightly smaller than the sensor proper 1. On the reverse surface of the front lid 2 in one half of the lid opposite to the infrared temperature-sensitive film 11a on the lefthand side in the bearings of the diagram, an infrared-intercepting film 13 made of an aluminum film is formed. The rear lid 3 is likewise formed of a silicon substrate in a size equal to the size of the sensor proper 1.

In this infrared sensor, the infrared radiation impinging on the obverse surface of the infrared sensor penetrates the front lid 2 and selectively reaches the infrared temperature-sensitive film 11b. The infrared sensor can detect the true amount of infrared radiation by measuring through the medium of the electrode pads 12 the differential output of the infrared temperature-sensitive film 11b exposed to the infrared radiation and the infrared temperature-sensitive film 11a shielded from the infrared radiation. The infrared radiation tending to enter the infrared sensor from the reverse surface side thereof is intercepted by the rear lid 3.

In the infrared sensor of the present embodiment, the front lid 2 and the rear lid 3 both made of silicon are respectively joined to the obverse and reverse surfaces of the sensor proper 1 so as to protect the bridging parts 10a, 10b and the infrared temperature-sensitive films 11a, 11b disposed inside the sensor proper 1. This infrared sensor, therefore, is allowed a notable decrease in size and consequently a reduction in the cost of production as compared with the conventional infrared sensor enclosed with a container such as a can.

Figs. 3A to 3J illustrate a series of steps followed in the production of the infrared sensor described above.

First, a silicon substrate (silicon wafer) 31 having a crystal face orientation (100) as shown in Fig. 3A was prepared. Then, on the obverse surface of this silicon substrate 31, a silicon oxynitride film 32 of a thickness of 1 μm was formed as shown in Fig. 3B by the plasma CVD (chemical vapor deposition) method. Subsequently, on the silicon oxynitride film 32, a multiplicity of infrared temperature-sensitive films 33 were formed as spaced at a fixed interval as shown in Fig. 3C. To be specific, by means of sputtering with germanium (Ge) as a target, an germanium (a-Ge) film was formed on the silicon oxynitride film 32. By a subsequent annealing treatment at 500 °C, impartation of an increasingly polycrystalline structure to this amorphous germanium was promoted. Then, the germanium film which had acquired the polycrystalline structure was patterned by reactive ion etching.

The silicon substrate 31 was heated to 150 °C. Then, by the technique of vacuum deposition, a chromium (Cr) film 34a of a thickness of 0.05 μm, a copper (Cu) film 34b of a thickness of 1.0 μm, and a nickel (Ni) film 34c of a thickness of 1 μm were sequentially superposed to form a laminate composite film 34 on the obverse surface and reverse surface of the hot silicon substrate 31 as shown in Fig. 3D. In the laminate film, the chromium layer 34a was intended as an adhesive layer with the foundation, the copper layer 34b as an electrically conductive layer, and the nickel layer 34c as an antioxidant film for the copper layer 34b. Then, the laminate composite film 34 on the obverse surface alone was patterned to obtain selective survival of the laminate composite film 34 around each of the infrared temperature-sensitive films 33.

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Then on the obverse surface of the silicon substrate 31, an electrode wiring layer and electrode pads were formed, though not illustrated in the diagram, and the silicon oxynitride film 32 was patterned after the fashion of bridges. Subsequently, with the aid of the openings which are consequently formed in the silicon oxynitride film 32, the silicon substrate 31 was etched selectively to give rise to cavities 35 and bridging parts 33a as shown in Fig. 3E. This etching was carried out anisotropically by the use of an aqueous hydrazine solution. Optionally, this anisotropic etching may be performed by the use of an aqueous potassium hydroxide solution.

A rear lid 36 was joined by the technique of soldering to the reverse surface of the silicon substrate 31 as shown in Figs. 3F and 3G. This rear lid 36 was formed in the same size as the silicon substrate 31. Similarly to the silicon substrate 31, the rear lid 36 was provided in advance with a laminate composite film 37 composed of a chromium film 37a, a copper film 37b, and a nickel film 37c and obtained by the technique of vacuum deposition.

After the rear lid 36 had been joined as described above, the plurality of sensor elements were individually tested with a probe to select conforming articles. To the surfaces of the sensor elements selected as conforming articles, such front lids 38 as shown in Fig. 3H were joined with flip chip bonder so as to cover the bridging parts 33a and the infrared temperature-sensitive films 33. The front lids 38, similarly to the rear lid 36, were each provided in advance with a laminate composite film 38 composed of a chromium film 38a, a copper film 38b, and a nickel film 38c and obtained by the technique of vacuum deposition. After the front lids 38 had been joined to all the sensor elements, the sensor elements were separated asunder by cutting with a dicing saw as shown in Fig. 3I, to obtain sensor elements having the opposite surfaces thereof protected with front lids 38 and rear lids 36 as shown in Fig. 3J.

In the present embodiment, since the front lids 38 and the rear lids 36 were made to cover the obverse and reverse surfaces of the sensor proper by the method described above, the bridging parts 32a formed in the sensor proper sustained virtually no injury from the impact of the cooling water to be used for the purpose of preventing evolution of heat during the process of dicing. Thus, the yield of the production in this case was 98%, a notably high level as compared with the level of 50% obtained in the production in which chips were separated asunder and then lids were joined to the separate chips. The separate chips produced in the present embodiment allowed decisively improved convenience of handling.

In the present embodiment, the bridging parts 32a and the infrared temperature-sensitive films 33 formed internally were protected by joining the front lids 38 and the rear lid 36 to the opposite surfaces of the silicon substrate 31. In the case of the method which relies on a sacrificial layer for the formation of bridging parts, it is sufficient to use only front lids 38 because the reverse surface side of the silicon substrate 31 is closed. The embodiment described above represents a case of preparatorily dividing the front lids 38 from one another, covering the sensor elements individually with the separate front lids 38, and thereafter separating the sensor elements asunder by cutting with a dicing saw. Optionally, the production of these separate sensor elements may be accomplished by joining the silicon substrate 31 with one rear lid 36 and one front lid 38 each in the form of a wafer and subsequently separating the individual sensor elements by cutting the silicon substrate 31 in conjunction with the corresponding portions of the rear lid 36 and front lid 38. The embodiment cited above has been described as using an infrared sensor of the type admitting the incident infrared radiation from the obverse surface side of the sensor proper 1. It is naturally permissible to use an infrared sensor of the type admitting the incident infrared radiation from the reverse surface side of the sensor proper 1.

In an infrared sensor 110 which is obtained in the present embodiment, a cavity 121 is formed in a silicon substrate 111 as a sensor substrate. On the upper side of this cavity 121, a silicon oxynitride (SiO_xN_y) film 112 provided with a bridging part 112a measuring 20 μm in width, 2 mm in length, and 3 μm in thickness is formed. An infrared temperature-sensitive film 114 is disposed on the upper surface in the central part of the bridging part 112a. This infrared temperature-sensitive film 114 is formed of amorphous germanium (a-Ge), for example. To the infrared temperature-sensitive film 114, one terminal part of an electrode wiring layer 115 formed of an aluminum (Al) film, for example, is electrically connected. In the peripheral part on the silicon substrate 111, electrode pads 130a, 130b are superposed on the electrode wiring layer 115.

The electrode pads 130a, 130b are each formed of a laminate film composed of a chromium (Cr) film 116 and a copper (Cu) film 117. The obverse surface of the silicon substrate 111 is covered with a silicon oxynitride film 118 as a protective film. In this silicon oxynitride film 118, contact holes are bored as opposed respectively to the electrode pads 130a, 130b. Inside these contact holes 119, a nickel (Ni) film 122 is superposed on the copper film 117 for the purpose of preventing the copper film 117 from oxidation. To the

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nickel film 122, a flexible printed substrate (not shown) is electrically connected as by soldering. On the lower surface of the silicon substrate 111, a silicon oxynitride film 113 intended for the formation of bridging parts is formed.

In this infrared sensor 110, the incident infrared radiation is injected into the infrared temperature-sensitive film 114. The magnitude of electricalal resistance of the infrared temperature-sensitive film 114 is varied in accordance with the amount of the infrared radiation (temperature). Since the magnitude of the electric current flowing to the electrode wiring layer 115 is varied and the magnitude of the voltage between the electrode pads 130a, 130b is consequently varied in accordance with the variation in the magnitude of this electrical resistance, the temperature of the object under test can be determined by detecting the variation in the magnitude of electric current or that of voltage in a signal processing circuit through the medium of a flexible printed substrate (not shown).

Figs. 5A to 5F illustrate a series of steps to be followed in the production of the infrared sensor 110 mentioned above.

First, a silicon substrate 111 having a crystal face orientation (100) as shown in Fig. 5A was prepared. On the opposite surfaces of this silicon substrate 111, silicon oxynitride films 112, 113 having a thickness of 1 μm as shown in Fib. 5B were formed as first and second insulating films by the technique of plasma CVD. To be specific, the silicon substrate 111 was heated to 450 °C and the hot silicon substrate was swept with reactant gases, i.e. monosilane (SiH_4) fed at a flow rate of 15 SCCM, nitrogen (N_2) 203 SCCM, and nitrous oxide (N_2O) 32 SCCM, under the film-forming conditions of 0.45 Torr of pressure and 400 W of high frequency output to effect vapor-phase deposition of silicon oxynitride on the opposite surfaces of the silicon substrate 111 for 20 minutes.

Then, the silicon oxynitride film 112 superposed on the surface of the silicon substrate 111 was patterned to give shape to the bridging part 112a. This patterning was effected by reactive ion etching (RIE) and continued until the underlying silicon substrate 111 was exposed. For this etching, methane trifluoride (CHF_3) and oxygen (O_2) were used as etching gases and they were fed at respective flow volumes of 47.5 SCCM and 2.5 SCCM. The etching conditions employed herein were 0.075 Torr of pressure, 150 W of high frequency output, and 3 hours of time.

Subsequently, on the upper surface in the central part of the silicon oxynitride film 112, an infrared temperature-sensitive film 114 as shown in Fig. 5C was formed. To be more specific, by means of sputtering with germanium (Ge) as a target, an amorphous germanium (a-Ge) film was superposed on the silicon oxynitride film 112. This sputtering was carried out under continued flow of argon (Ar) gas at a flow volume of 4 SCCM under the conditions of 3×10^{-3} Torr of film-forming pressure, 160 W of high frequency output, and 10 minutes of time. Then, by means of an annealing treatment at 400 °C, impartation of an increasingly polycrystalline structure to the amorphous germanium was promoted. The amorphous germanium film which had undergone the impartation of a polycrystalline structure was patterned by reactive ion etching. The silicon substrate 111 was then heated to 150 °C. On the obverse surface of the hot silicon substrate, an aluminum film of a thickness of 0.5 μm was superposed as by the technique of vacuum deposition. This aluminum film was patterned to give rise to an electrode wiring layer 115 as shown in Fig. 5D.

Then, electrode pads 130a, 130b were formed in the edge parts of the silicon substrate 111 as shown in Fig. 5E. To be more specific, on the electrode wiring layer 115, a chromium (Cr) film 116 of a thickness of 0.05 μm and a copper (Cu) film 117 of a thickness of 1.5 μm as an etchant-resistant film were formed sequentially by the technique of vacuum deposition. On the surface of the silicon substrate 111, a silicon oxynitride film 118 of a thickness of 1 μm was formed as a third insulating film as shown in Fig. 5F.

Then, in the silicon oxynitride film 118, the contact holes 119 were formed so as to correspond to the electrode pads 130a, 130b as shown in Fig. 5G. Subsequently, an opening part 120 was formed in the silicon oxynitride film 113 on the reverse surface by selectively etching this film 113.

Then, via this opening part 120, the silicon substrate 111 was selectively etched from the reverse surface side to form the cavity 121 as shown in Fig. 5H. This etching was carried out anisotropically by the use of an aqueous hydrazine solution as an etching liquid at a temperature of 110 °C for one and a half hours to a depth reaching the silicon oxynitride film 112 on the obverse surface of the silicon substrate 111. Optionally, this etching may, instead, be performed by the use of an aqueous potassium hydroxide solution.

Then, in the contact holes 119 of the electrode pads 130a, 130b, the nickel films 122 for preventing the copper films 117 from oxidation were formed by the technique of electroless plating as shown in Fig. 5I. This plating was effected by immersion in a plating liquid (product of Okuno Seiyaku Kogyo K.K. and marketed under trademark designation of "Top Chemicalloy B-1") at 65 °C for five minutes until the nickel films 122 grew to a thickness of 1 μm.

By the method of the present embodiment, since the copper films 117 possessing an etchant-

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resistant property have been already formed in the uppermost layers of the electrode pads 130a, 130b when the contact holes 119 are formed in the silicon oxynitride film 118 as the third insulating film and then the film 118 is subjected to anisotropic etching with a strong alkali liquid such as hydrazine, the possibility that the electrode pads 130a, 130b will be dissolved by the etching liquid is nil. Further, since the bridging parts 112a have not yet been formed when the contact holes 119 are formed on the upper surface of the silicon substrate 111, the bridging parts 112a are precluded from the otherwise inevitable breakage and the yield of production is notably improved.

The embodiment described thus far represents a case of forming the nickel films 122 for the prevention of the copper films 117 from oxidation subsequently to the step of anisotropic etching (Fig. 5I). Optionally, the formation of the nickel film 122 may be carried out before the step of anisotropic etching and after the formation of the contact holes 119.

Further, the embodiment cited above contemplates forming the electrode pads 130a, 130b each with a two-layer laminate film composed of a chromium film 116 and a copper film 117. This laminate film, when necessary, may be constructed in a three-layer structure having a gold (Au) film 123 additionally superposed on the copper film 117. This laminate has no use any longer for the nickel film 122 which is essentially used in the embodiment described above.

In the infrared sensor which is obtained as described above, the cavity 121 is tightly sealed as shown in Fig. 1 by joining thereto a front lid and a rear lid (neither shown herein).

Fig. 7 is a plan view illustrating the construction of an infrared sensor 210 as yet another embodiment of this invention. Fig. 8 is a cross section taken through Fig. 7 along line VIII-VIII.

This infrared sensor 210 has a silicon oxynitride film 212 of a thickness of 1 μm formed as a first insulating film on the upper surface of a silicon substrate 211 as a sensor substrate. On this silicon oxynitride film 212, an infrared temperature-sensitive film 213 made of polycrystalline germanium is superposed. This infrared temperature-sensitive film 213 is covered with a silicon oxynitride film 214 as a second insulating film. In the silicon oxynitride film 214, contact holes 224a, 224b shaped like mutually opposed combs are formed.

On the silicon oxynitride film 214, electrodes 225a, 225b extending through the thickness of the contact holes 224a, 224b and reaching the infrared temperature-sensitive film 213 are formed. The electrodes 225a, 225b are made of an electrically conductive layer such as, for example, aluminum film. In a plan view, they are shaped like mutually opposed combs in conformity to the contact holes 224a, 224b. The electrodes 225a, 225b are connected to a wiring electrode (not shown) respectively through the medium of wiring layers 218a, 218b which are made of an aluminum film. The parts of the electrodes 225a, 225b rising above the silicon oxynitride film 214 have a width greater by a size, t, (5 μm, for example) than the width (10 μm, for example) of the parts thereof extending through the concrete holes 224a, 224b. Thus, the electrodes 225a, 225b form parts of increased width 217 above the silicon oxynitride film 214 and, as a result, have a T-shaped cross section.

In this infrared sensor 211, the magnitude of electric resistance of the infrared temperature-sensitive film 213 is proportionately varied with the amount (heat quantity) of the incident infrared radiation. Thus, the amount of the radiation (temperature) can be detected by measuring with a signal processing circuit (not shown) the magnitude of electrical current flowing to the electrodes 225a, 225b and the wiring layers 218a, 218b or the magnitude of voltage generated between the wiring electrodes (not shown) in accordance with the variation in the magnitude of electric resistance.

In the infrared sensor 210 of the present embodiment, the parts (parts of increased width 217) of the electrodes 225a, 225b rising above the silicon oxynitride film 214 have a width greater than the width of the parts thereof extending inside the contact holes 224a, 224b and the edge parts of the upper surfaces of the contact holes 224a, 224b, therefore, are covered with the parts of increased width 217 of the electrodes 225a, 225b. In this infrared sensor 210, the parts of increased width 217 are etched and reduced in width even when the phenomenon of side etching is allowed to occur during the etching of the electrodes 225a, 225b. No dispersion occurs in the magnitude of electric resistance, therefore, because no gap is inserted between the electrodes 225a, 225b and the silicon oxynitride film 214 or no etching is eallowed to occur on the infrared temperature-sensitive film 213.

Figs. 9A to 9E illustrate a series of steps followed in the production of electrode parts in the infrared sensor 210.

First, the silicon oxynitride film 212 was formed by the technique of plasma CVD on the silicon substrate 211 as shown in Fig. 9A. Then, by means of sputtering, the infrared temperature-sensitive film 213 made of an amorphous germanium (a-Ge) film was formed in a thickness of 1 μm on the silicon oxynitride film 212. This sputtering was carried out by feeding argon (Ar) gas at a flow volume of 4 SCCM under the conditions of 3×10^{-3} Torr of film-forming pressure, 160 W of high frequency output, and about 10 minutes of time. Then, by an

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annealing treatment performed at a temperature of 100 °C, impartation of an increasing polycrystalline structure to the amorphous germanium was promoted. Subsequently, by reactive ion etching (RIE), the germanium film which had acquired a grown polycrystalline structure was patterned. This reactive ion etching was carried out by feeding Freon (CF_4) gas at a flow volume of 40 SCCM under the conditions of 0.2 Torr of pressure, 150 W of high frequency output, and about 10 minutes of time.

Then, by the technique of plasma CVD, the silicon oxynitride film 214 was formed so as to cover the infrared temperature-sensitive film 213 on the silicon oxynitride film 212 as shown in Fig. 9B. Then, on this silicon oxynitride film 214, a photoresist film 226 containing a contact hole pattern (t1 in width) was formed. The silicon oxynitride film 214 was etched with the photoresist film 226 as a mask, to give rise to the contact holes 224a, 224b as shown in Fig. 9C.

Then, by performing vacuum deposition of aluminum at a temperature of 150 °C for about 8 minutes, an aluminum film 215 of a thickness of 1.5 μm was formed on the infrared temperature-sensitive film 213 as shown in Fig. 9D. Subsequently, on the aluminum film 215, a photoresist film 227 of a thickness of 1 μm containing an electrode pattern was superposed. Here, the width t2 of the electrode pattern in the photoresist 227 was greater by 2t than the width t1 of the contact holes 224a, 224b.

Thereafter, the aluminum film 215 was selectively etched wet with the photoresist film 227 as a mask to give rise to the electrodes 225a, 225b as shown in Fig. 9E. The wet etching was carried out at 40 °C for about 5 minutes by the use of an etching liquid composed of phosphoric acid (H_3PO_4), nitric acid (HNO_3), acetic acid (CH_3COOH), and water (H_2O) at a mixing ratio of 18 : 1 : 2 : 1. The infrared sensor 210 constructed as illustrated in Fig. 8 was obtained as a consequence of the process described above.

By this method, the electrode pattern in the photoresist film 227 has a greater width than the contact hole pattern of the photoresist 226 (Fig. 9B). Even when the phenomenon of side etching is allowed to occur in the aluminum film 215 during the etching of the aluminum film 215 at the step of Fig. 9E, only the parts of the electrodes 225a, 225b rising above the silicon oxynitride film 214 are etched and reduced in width. Thus, no gap occurs between the electrodes 225a, 225b and the silicon oxynitride film 214 or no etching is allowed to occur on the infrared temperature-sensitive film 213.

The infrared sensor of this invention is furnished with a cavity. In this cavity, it is provided with a sensor substrate having an infrared temperature-sensitive film superposed thereon and vacuum sealing means for covering the cavity and sealing the periphery of the infrared temperature-sensitive film in a vacuum state.

In this infrared sensor, since the infrared temperature-sensitive film is tightly sealed to keep the periphery thereof in a vacuum state, the amount infrared radiation energy lost through the infrared temperature-sensitive film is minimized and, as a result, the temperature rise of the infrared temperature-sensitive film is increased and the sensitivity of the sensor is remarkably enhanced.

The term "vacuum" as used in this specification shall be construed as designating a state in which the pressure is not higher than 1.0 Torr. Where the degree of vacuum is 10^{-3} Torr or less, the effect of this vacuum is substantially equal to that which is obtained when the pressure is 10^{-3} Torr.

More specifically, the infrared sensor of this invention is preferably so constructed as to have the sensor substrate thereof provided therein with a pair of cavities, the cavities provided individually with infrared temperature-sensitive films identical in structure, one of the infrared temperature-sensitive films adapted to admit infrared radiation selectively, and the other infrared temperature-sensitive film shielded from the infrared radiation. This infrared sensor, by detecting the difference between the output of the infrared temperature-sensitive film admitting the infrared radiation and that of the infrared temperature-sensitive film not admitting the infrared radiation, is able to determine the net amount of infrared radiation while precluding electrical noise and thermal disturbance. When the two cavities in this construction are made to communicate with each other, they can be maintained at one and the same degree of vacuum and the detection of infrared radiation can be attained with enhanced accuracy. The pair of cavities may be formed in one and the same sensor substrate. Otherwise, they may be formed separately in different sensor substrates on the condition that they are adapted to have sufficient thermal contact to maintain the same temperature.

For the sensor substrate, such semiconducting substrates of silicon, germanium, etc. are usable. Preferably, a silicon substrate is used because it can be obtained easily and less expensively.

Generally, the infrared temperature-sensitive films come in the bolometer type, the thermopile type, the collector type, etc. The infrared temperature-sensitive film of the bolometer type among other types proves to be particularly preferable in the sense that it allows miniaturization of the sensor because the resistance of the sensor element varies with the variation in the temperature

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of the sensor caused by infrared radiation and, therefore, the amount of infrared radiation (temperature) can be directly detected from the magnitude of resistance. The infrared temperature-sensitive film in this case is formed of a film of amorphous germanium (a-Ge), amorphous silicon (a-Si), polycrystalline germanium, polycrystalline silicon, etc. For the formation of this infrared temperature-sensitive film, the techniques of sputtering, ion beam sputtering, CVD (chemical vapor deposition), etc. are available. For supporting the infrared temperature-sensitive film, such structures as a bridge of the type supported at the opposite ends thereof, a cantilever, and a diaphragm are usable. The structure of the bridge mentioned above among other structures proves to be particularly desirable for the purpose of decreasing the heat capacity and, at the same time, ensuring structural stability.

As the material for the bridging structure, a silicon oxide (SiO_x) film, a silicon nitride (SiN_y) film, a silicon oxynitride (SiO_xN_y) film, etc. are usable. The silicon oxynitride film among other materials cited above proves to be particularly preferable. The silicon oxynitride film combines the properties of both silicon oxide film and silicon nitride film and, therefore, enjoys an ideal stress balance and permits stable formation of the bridge structure. This bridging part can be produced by one superposing silicon oxynitride films on each of the opposite surfaces of a silicon substrate, with one of the surfaces patterned in advance after the fashion of a bridge and the other surface after the fashion of a window of desired size, and anisotropically etching the silicon oxynitride films with an aqueous hydrazine solution or potassium hydroxide (KOH), for example.

Specifically, the means for vacuum sealing comprises lids (front lid and rear lid) which are joined to the opposite surfaces of the sensor substrate. The sealing of the sensor substrate sufficient to keep the interior thereof in a vacuum state is attained by joining one of the lids to one surface of the sensor substrate and then joining the other lid to the other surface of the sensor substrate held in an atmosphere of vacuum. For the lids, silicon substrates may be used. In this case, for the purpose of enabling one of the pair of infrared temperature-sensitive films to selectively admit infrared radiation, the silicon substrate which forms the lid for passing the infrared radiation is preferably provided on the opposite surfaces thereof with an infrared-reflecting film such as an aluminum film and to be provided partially in each of the infrared-reflecting films with a window (opening part).

As means for joining the lids to the sensor substrate, the technique of solder welding and the technique of anode bonding are available. The anode bonding is a technique for joining glass (such as, for example, Pyrex glass) to silicon. It is said that the silicon substrate and glass are joined across their interface due to the covalent bond of silicon and oxygen atoms which exist at the interface. When this anode bonding technique is adopted, it is carried out under a vacuum to enable the periphery of the temperature-sensitive film of the infrared sensor to be kept in a vacuum state. To ensure this vacuum sealing, a glass layer must be interposed between the front lid of silicon and the sensor substrate of silicon and between the rear lid of silicon and the sensor substrate of silicon. For this purpose, it is necessary to have a thin glass film formed by the technique of sputtering, for example, on either of the front lid and the sensor substrate and either of the rear lid and the sensor substrate.

Now, the method for joining the lids to the sensor substrate by the anode bonding will be described more specifically below. First, a wafer cut in the shape of a rear lid (rear-lid wafer) is placed on a cathode and a wafer cut in the shape of a sensor proper (sensor-proper wafer) is placed on the rear-lid wafer. On the surface of the rear lid intended for contact, a low melting glass film is formed in advance by sputtering. On the sensor-proper wafer, a needle-shaped electrode is erected. A DC voltage in the range of 30 to 100 V is applied between this needle-shaped electrode and the cathode. The advance of the anode bonding is followed by monitoring the magnitude of the electrical current. Generally, the magnitude of electrical current decreases monotonously and ceases to decrease at the level of the leakage current (generally on the order of 1 mA, depending on the area of a sample). At the end of the anode bonding, the joined part is tested for leakage with a helium leak detector. Then, by following the same procedure, a wafer cut in the shape of a front lid (front-lid wafer) is joined to the first two wafers already joined. The work which follows the union of the lids to the sensor substrate is carried out inside a vacuum chamber for the purpose of sealing the sensor proper in a vacuum state. Since the opposition of the front lid to the joined wafers in an atmosphere of vacuum cannot be performed as effectively as in the open air, it must be carried out with the aid of an infrared scope as kept under constant observation through a vacuum quality inspection window (made of quartz). During the evacuation of the entrapped air for creation of a vacuum, they are separated with a sufficient space to provide ample conductance for the removal of the entrapped air from the tightly sealed space. They are not brought into contact and joined until the fall in vacuum to a level below 10^{-5} Torr has been confirmed. When the front lid and the rear lid are made of glass, they

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can be joined directly to the sensor substrate without requiring interposition of a thin glass film. When the silicon substrate and the lids of silicon are used as described above and they are both formed of single crystal, they serve ideally to maintain the cavity in a vacuum state because they have an extremely small gas content due to the quality of the single crystal and they are sparingly pervious to an external gas.

Now, this invention will be described more specifically below with reference to working examples.

Fig. 10 is a diagram illustrating the construction of an infrared sensor 310 as one embodiment of this invention. The infrared sensor 310 of this embodiment uses a silicon substrate (single crystal silicon) 311 as a sensor substrate. In the silicon substrate 311, two cavities 314a, 314b are formed. These cavities 314a, 314b each open in the upper and lower surfaces of the silicon substrate 311. On the lower surface of the silicon substrate 311, a silicon oxynitride (SiO_xN_y) film 312 containing two bridging parts 312a, 312b is formed. Infrared temperature-sensitive films 313a, 313b are formed on the lower surfaces in the central parts respectively of the bridging parts 312a, 312b. These infrared temperature-sensitive films 313a, 313b are formed of amorphous germanium (a-Ge), for example. To the infrared temperature-sensitive films 313a, 313b, single-terminal parts of electrode wiring layers formed of aluminum (Al) film are electrically connected though not shown in the diagram. The other terminal parts of the electrode wiring layers are connected to electrode pads 315a, 315b which are formed in the edge parts on the lower surface of the silicon substrate 311.

On the upper surface of the silicon substrate 311, a silicon oxynitride film 316 is formed. A front lid 317 is joined to the upper surface of this silicon oxynitride film 316. The front lid 317 is formed of a silicon substrate 318. On the obverse and reverse surfaces of this silicon substrate 318, infrared reflection preventing films 319a, 319b are respectively formed. On the obverse surfaces of these infrared reflection preventing films 319a, 319b, infrared-intercepting films 320a, 320b made of aluminum (Al) are formed. In these infrared-intercepting films 320a, 320b at the positions thereof opposed to the infrared temperature-sensitive film 313a falling on the righthand side in the bearings, an opening part 321 for guiding the infrared radiation is formed. The front lid 317 is joined to the silicon oxynitride film 316 by the technique of high melting solder welding, for example.

To the lower surface of the silicon substrate 311, a rear lid 322 is joined. This rear lid 322 is formed of silicon like the front lid 317. In the upper surface of the rear lid 322, excavated parts 323a, 323b are formed as opposed to the cavities 314a, 314b of the silicon substrate 311. These excavated parts 323a, 323b are made to communicate with each other via a communicating part 324. The rear lid 322 is joined to the silicon oxynitride film 312 in a vacuum atmosphere by the technique of high melting solder welding or the technique of anode bonding. As a result, the infrared temperature-sensitive films 313a, 313b in the cavities 314a, 314b of the silicon substrate 311 and in the excavated parts 323a, 323b of the rear lid 322 are sealed under one and the same degree of vacuum.

On the wall surfaces of the cavities 314a, 314b and the excavated parts 323a, 323b, an infrared-reflecting film 325 made of nickel (Ni), for example, is formed so as to prevent the infrared radiation which has entered the infrared temperature-sensitive film 313a from further entering the other infrared temperature-sensitive film 313b. To the electrode pads 315a, 315b in the edge parts of the rear lid 222, FPC (flexible printed circuit) substrates are electrically connected. The infrared sensor 310 is wholly supported by a base 327 which is made of copper (Cu). A depression 328 is formed in the central part of the base 327. To this depression 328, the rear lid 322 is joined by the technique of low melting solder welding.

In this infrared sensor, the infrared radiation introduced from above in the bearings of the diagram is passed through the opening part 321 of the front lid 317 and the cavity 314a and then injected selectively into the infrared temperature-sensitive film 313a. The other infrared temperature-sensitive film 313b is shielded from the infrared radiation by the infrared-intercepting films 320a, 320b. The differential output between the infrared temperature-sensitive film 313a admitting the infrared radiation and the infrared temperature-sensitive film 313b expelling the infrared radiation is detected through the medium of the FPC substrate 326. Since the periphery of the infrared temperature-sensitive film 313a inside the cavity 314a and the excavated part 323a is maintained in a vacuum state, the energy of the incident infrared radiation is not lost through the air and the very small amount of infrared radiation emanating from a sample can be absorbed efficiently and the sensitivity of the sensor is enhanced. The infrared temperature-sensitive film 313b inside the other cavity 314b and the excavated part 323b is also maintained under the same degree of vacuum. Due to the differential output between the two infrared temperature-sensitive films 313a, 313b, the true amount of infrared radiation can be detected.

(First experimental example)

Fig. 11 schematically illustrates the construction of an experimental system used for confirming

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the effect of an infrared sensor embodying this invention. In this system, a semiconductor laser having an output wavelength of 673 nm was used as a light source 331. The light emanating from this semiconductor laser was condensed with a lens 332 on one infrared temperature-sensitive film 313a of the infrared sensor 310. Thus, the differential output which occurred between this infrared temperature-sensitive film 313a and the other infrared temperature-sensitive film 313b was obtained. The output from the semiconductor laser was made to occur in the form of a pulse so as to allow evaluation of the sensitivity of response of the infrared temperature-sensitive film 313a.

Line A in Fig. 12 shows the results (relation between the time T and the value dT of rise of temperature) of a comparative experiment carried out on the infrared sensor 310 set in the open air. In this case, the differential output corresponding to the output of the semiconductor laser could not be clearly detected. Line B in Fig. 12 shows the results of an experiment carried out under the same conditions as described above, excepting the infrared sensor 310 was set under a vacuum (3.2×10^{-3} Torr). The differential output could be clearly detected, indicating that the sensitivity of response was improved in this case. Fig. 13 shows the results of the same experiment carried out under the same conditions, except that the degree of vacuum P was varied to produce data usable for comparison with those obtained in the open air. In the data shown in the diagram, those enclosed with parentheses are the values given for the purpose of comparison with those obtained in the open air. The effect began to show clearly (1.5 times) when the degree of vacuum was 1.0 Torr and reached about 20 times when the degree of vacuum was about 10^{-3} Torr. When the degree of vacuum was lower than the level just mentioned, the sensitivity of response was substantially equal to that obtained at 10^{-3} Torr.

(Second experimental example)

Fig. 14 is a diagram illustrating an infrared sensor used in the second experimental example. An infrared sensor 310 of this experiment was sealed in a can package 340 and kept in a vacuum state. It was joined to the upper surface of a stem 341 by die bonding with a heat-resistant epoxy resin. An infrared-intercepting plate 342 was disposed on a lead terminal 343 of the can package 340. A cap 344 was joined by soldering to the upper surface of the stem 341. An upper opening part 345 of this cap 344 was covered with a reflection-proof film 346 made of silicon. The reflection-proof film 346 was fastened to the cap 344 with low melting glass 347. Getter members 348 for adsorbing the internal gas were attached fast to the inner ceiling surface of the cap 344 and to the infrared-intercepting plate 342. The getter members 348 were made of an aqueous solution of powder mixture of zirconium (Zr) and carbon (C) (a product of Giken Kagakusha K.K. having an activating temperature of 225 °C).

The vacuum sealing of the can package 340 was effected by placing the stem 341 and the cap 344 in a vacuum container, evacuating the entrapped air from the vacuum container to a vacuum (3×10^{-6} Torr), heating the stem 341 and the cap 344 with their respective heaters to 230 °C, continuing the removal of internal gas for three hours, and thereafter slowly joining the stem 341 and the cap 344. The solder used in this case was a product having a melting point of 221 °C and containing flux. The solder in a molten state was placed in advance on the stem 341 and the cap 344 in the open air. Afterwards, the flux floating on the solder surface was removed with trichloroethylene.

Fig. 15 shows the results of the determination of infrared radiation with the infrared sensor using the can package 340 of Fig. 14. The data clearly indicate that the sensitivity of the present sensor was about 14 times as high as that obtained with the conventional sensor containing normal air.

Claims

1. An infrared sensor comprising a substrate provided with a bridging part, a detecting part composed of an infrared temperature-sensitive film formed in said bridging part, a first lid covering said detecting part and said bridging part, and a second lid covering the reverse surface of said substrate and tightly closing a cavity formed between said substrate and said bridging part.

2. An infrared sensor according to claim 1, wherein said substrate is made of a semiconducting material.

3. An infrared sensor according to claim 1, wherein said bridging part is formed of a film made of at least one member selected from the group consisting of silicon oxides, silicon nitrides, and silicon oxynitrides.

4. An infrared sensor according to claim 1, wherein said infrared temperature-sensitive film is made of at least one member selected from the group consisting of amorphous germanium, amorphous silicon, polycrystalline silicon, and polycrystalline germanium.

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5. An infrared sensor according to claim 1, wherein said lids are made of a semiconducting material.

6. An infrared sensor according to claim 5, wherein two bridging parts and two infrared detecting parts are used and each odd one of said paired components is provided with an infrared-intercepting film.

7. An infrared sensor according to claim 1, which further comprises an electrode pad electrically connected to said infrared temperature-sensitive film and formed of a laminate film including an etchant-resistant electrically conductive film.

8. An infrared sensor according to claim 7, wherein said electrode pad is made of a laminate film consisting of aluminum and said etchant-resistant film is made of copper or gold.

9. An infrared sensor according to claim 1, which further comprises an infrared temperature-sensitive film formed on said substrate through the medium of a first insulating film, a second insulating film formed on said infrared temperature-sensitive film and provided with a contact hole so deep as to reach said infrared temperature-sensitive film, and an electrode formed on said second insulating film, electrically connected to said infrared temperature-sensitive film via said contact hole, and provided above said second insulating film with a part of increased width greater than the width of the part thereof extending inside said contact hole.

10. A method for the production of an infrared sensor, comprising a step of forming on a semiconductor wafer a plurality of sensor elements provided on a bridging part with an infrared temperature-sensitive film, a step of sealing said sensor elements each with a lid member capable of tightly sealing said sensor element, and a step of separating the tightly sealed sensor elements asunder by cutting.

11. A method according to claim 10, wherein said semiconductor wafer is a silicon wafer.

12. A method according to claim 10, which comprises forming a film of a bridge-forming material on one surface of a semiconductor wafer, forming an infrared temperature-sensitive film on the obverse surface of said film of bridge-forming material, forming a laminate composite film on one surface of said semiconductor wafer and a laminate composite film on the other surface of said semiconductor wafer around the periphery of said infrared temperature-sensitive film, partially etching said semiconductor wafer thereby forming a cavity therein, joining a second lid to the cavity side semiconductor wafer, joining a first lid to the upper surface of said laminate composite film on said infrared temperature-sensitive film side and tightly sealing said laminate composite film, and separating the portions of said semiconductor wafer corresponding to said infrared temperature-sensitive films asunder by cutting.

13. A method according to claim 12, wherein said laminate composite film comprises a chromium layer, a copper layer, and a nickel layer.

14. A method for the production of an infrared sensor, comprising a step of forming a first insulating film intended for formation of a bridging part on one of the main surfaces of a sensor substrate made of a semiconducting material and forming a second insulating film containing an opening for etching on the other main surface of said sensor substrate, a step of forming an infrared temperature-sensitive film on said first insulating film, a step of forming on said first insulating film an electrode pad provided in the uppermost layer thereof with an etchant-resistant electrically conductive film in such a manner as to be connected electrically to said infrared temperature-sensitive film, a step of forming a third insulating film on said sensor substrate containing said electrode pad and selectively forming a contact hole in said third insulating film in a depth reaching said electrode pad, and a step of anisotropically etching said sensor substrate via said opening of the contact hole thereby forming a bridging part.

15. A method according to claim 14, wherein said semiconducting material is silicon.

16. A method according to claim 14, wherein said first, second, and third insulating films are made of at least one member selected from the group consisting of silicon oxynitrides, silicon oxides, and silicon nitrides.

17. A method according to claim 14, wherein said infrared temperature-sensitive film is made of at least one member selected from the group consisting of amorphous germanium, amorphous silicon, polycrystalline silicon, and polycrystalline germanium.

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18. A method for the production of an infrared sensor, comprising a step of forming a first insulating film on the obverse surface of a sensor substrate and then forming an infrared temperature-sensitive film on said insulating film, a step of forming a second insulating film in such a manner as to cover said infrared temperature-sensitive film, a step of forming on said second insulating film a first etchant-resistant film containing a prescribed contact hole pattern and etching said second insulating film with said first etchant-resistant film as a mask thereby forming in said second insulating film a contact hole so deep as to reach said infrared temperature-sensitive film, a step of superposing an electrically conductive layer on said second insulating film having said contact hole formed therein, and a step of forming on said electrically conductive layer a second etchant-resistant film containing an electrode pattern of a width greater than the width of said contact hole pattern in said first etchant-resistant film and etching said electrically conductive film with said second etchant-resistant film as a mask thereby forming an electrode.

19. A method according to claim 18, wherein said first and second insulating films are made of at least one member selected from the group consisting of silicon oxynitrides, silicon oxides, and silicon nitrides.

20. A method according to claim 18, wherein said infrared temperature-sensitive film is made of at least one member selected from the group consisting of amorphous germanium, amorphous silicon, and polycrystalline silicon.

21. An infrared sensor comprising a sensor substrate possessed of a cavity and provided in said cavity with an infrared temperature-sensitive film and vacuum sealing means covering said cavity in said sensor substrate and sealing said sensor substrate by the periphery of said infrared temperature-sensitive film so as to keep a vacuum state.

22. An infrared sensor according to claim 21, wherein said sensor substrate is made of a semiconducting material.

23. An infrared sensor according to claim 22, wherein said semiconducting material is single crystal silicon.

24. An infrared sensor according to claim 21, wherein said vacuum sealing means comprises a front lid covering the upper opening part of said sensor substrate and a rear lid covering said infrared temperature-sensitive film disposed in the lower opening part while allowing intervention of an empty space therebetween.

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FIG.1

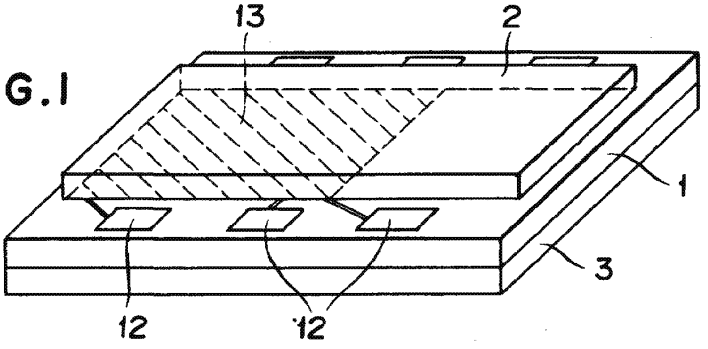


FIG.2

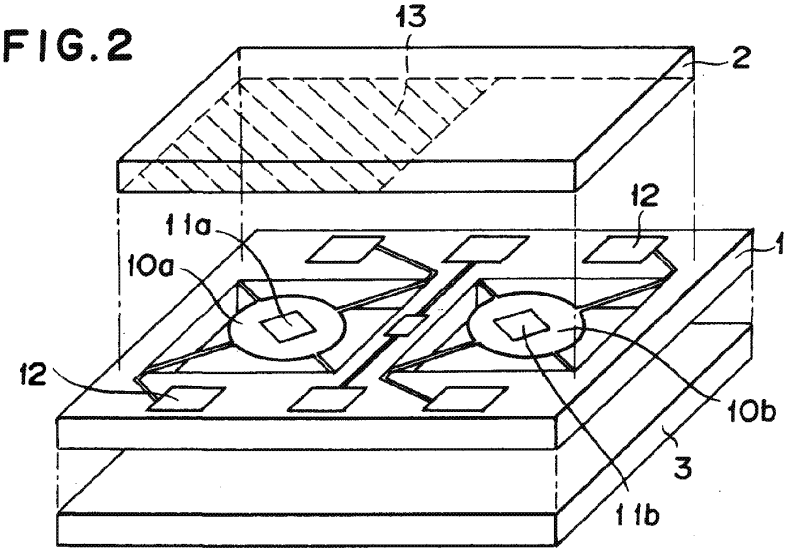


FIG.3A

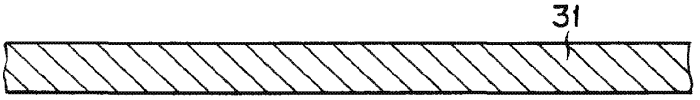


FIG.3B

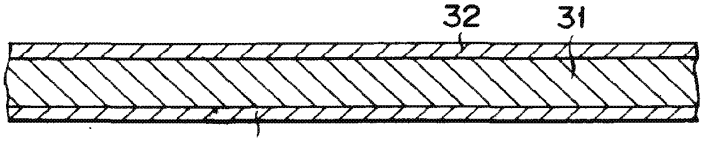
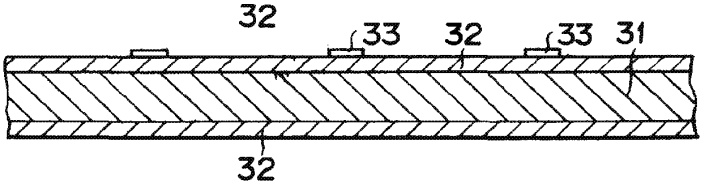


FIG.3C



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FIG.3D

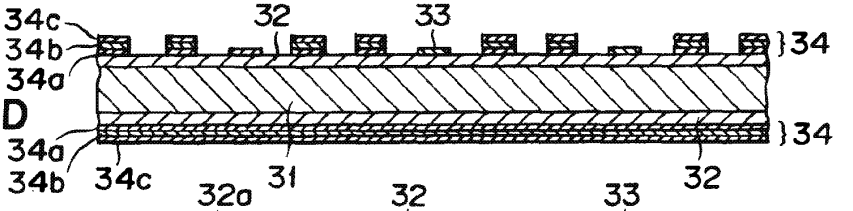


FIG.3E

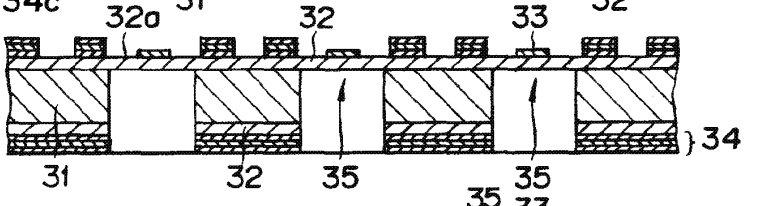


FIG.3F

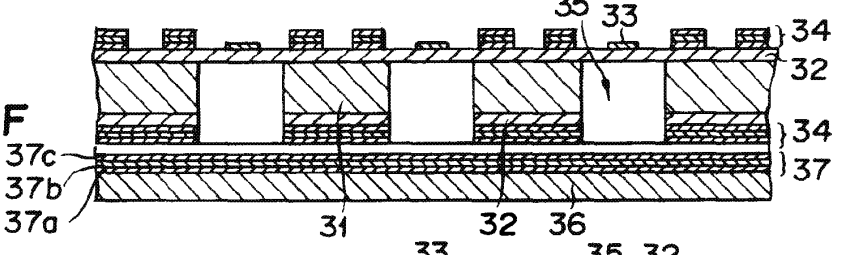


FIG.3G

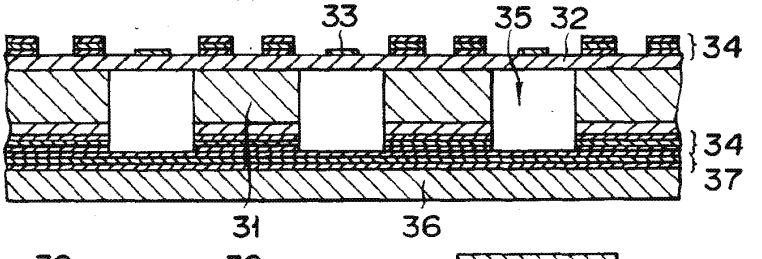


FIG.3H

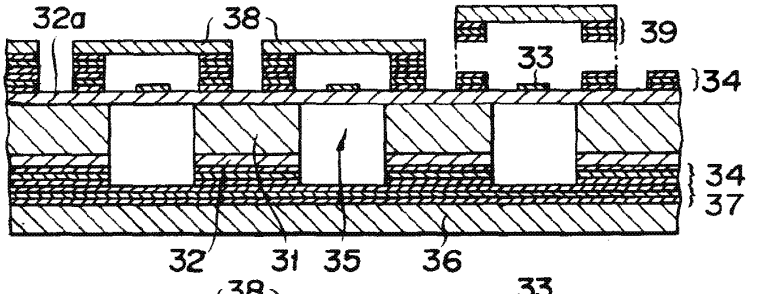
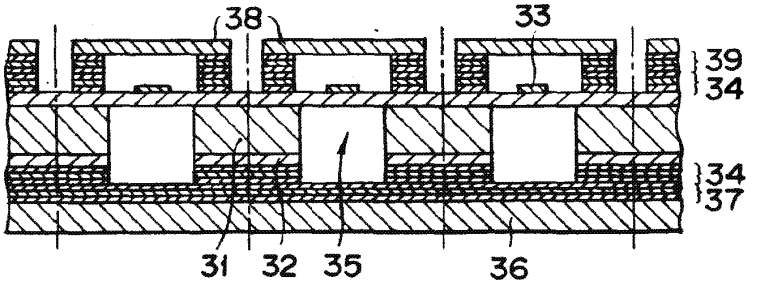


FIG.3I



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FIG.3J

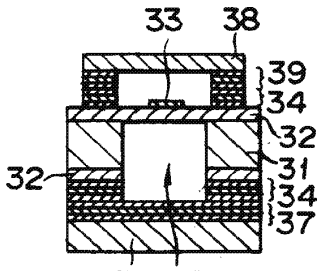


FIG.4

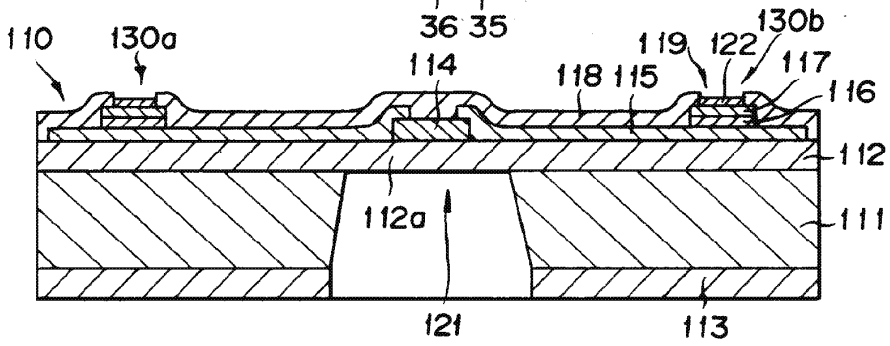


FIG.5A

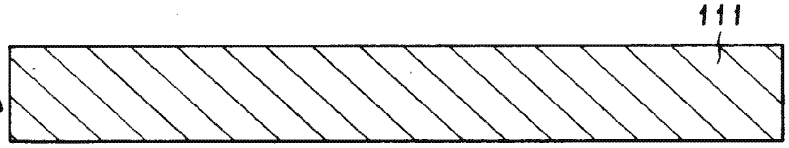


FIG.5B

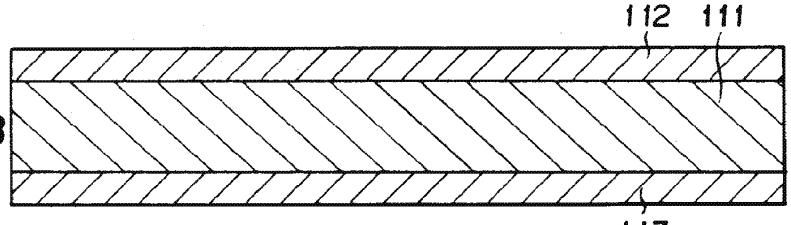
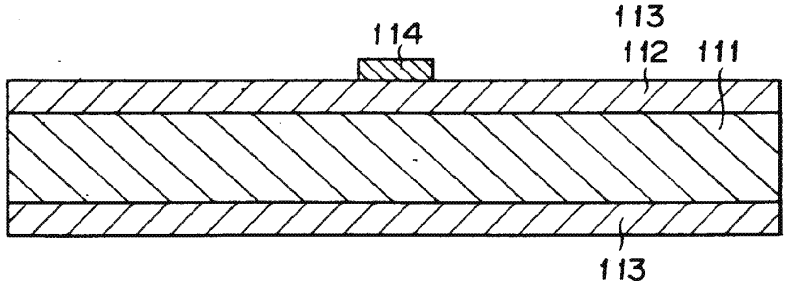


FIG.5C



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FIG.5D

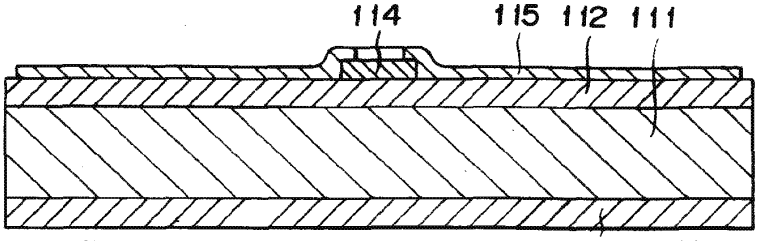


FIG.5E

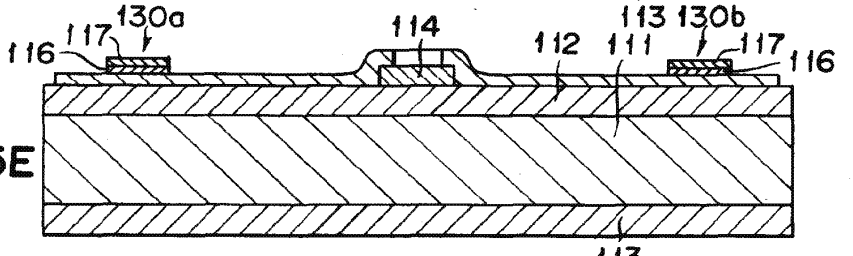


FIG.5F

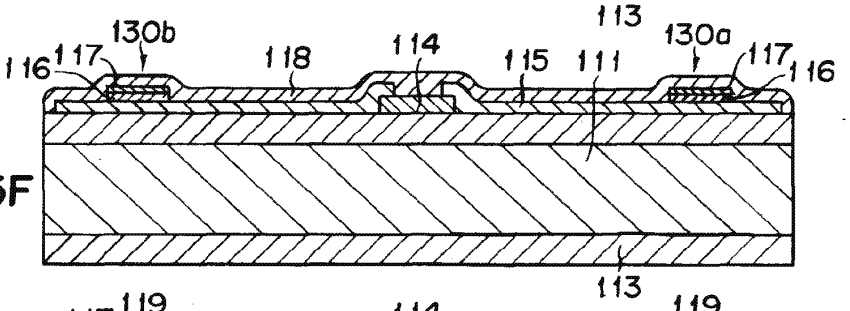


FIG.5G

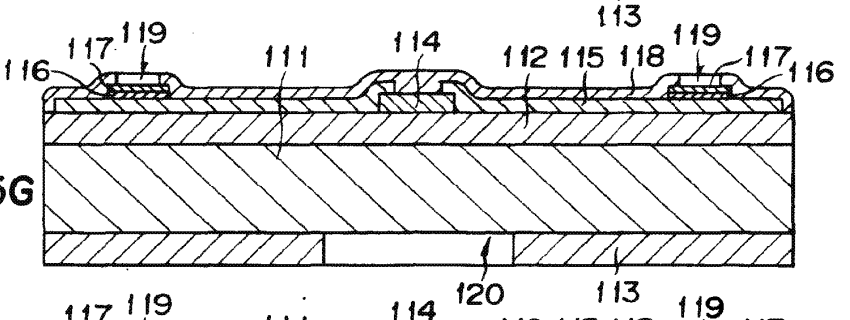
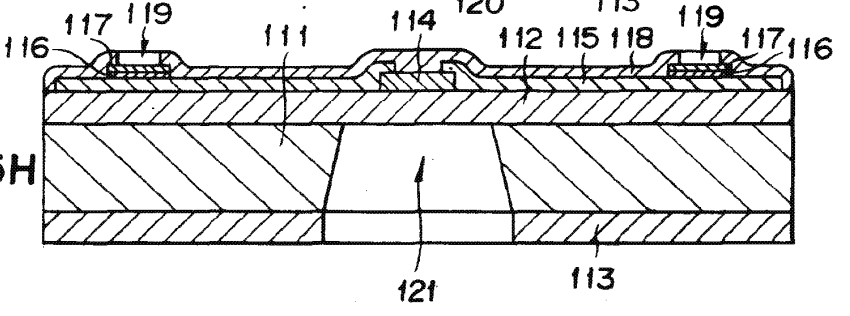


FIG.5H



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FIG.5I

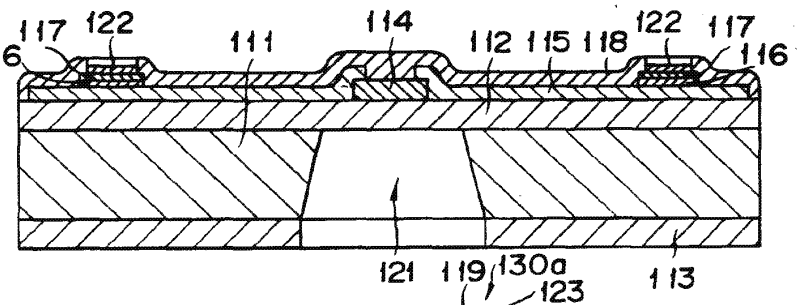


FIG.6

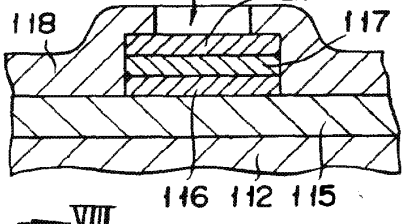


FIG.7

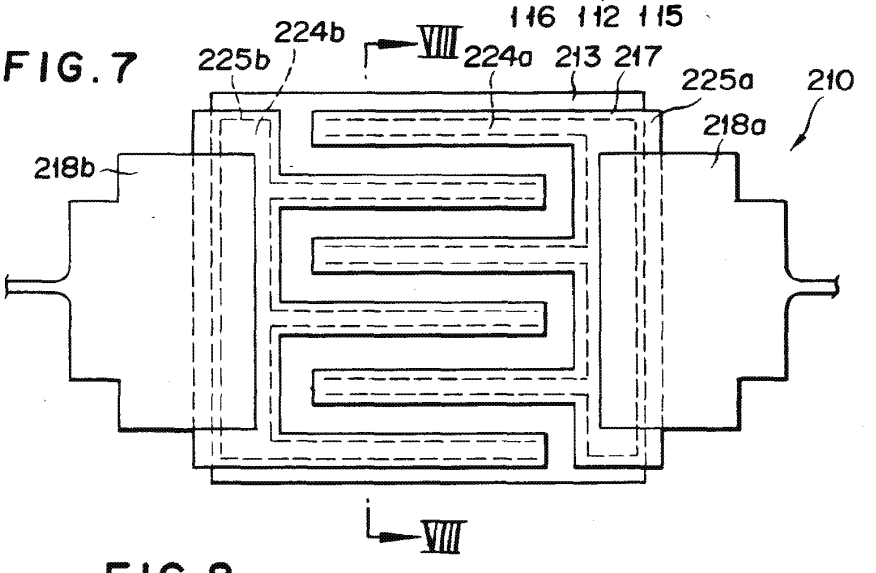
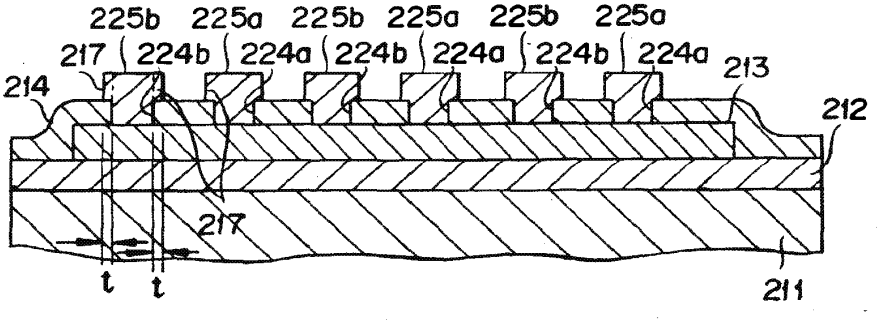


FIG.8



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FIG. 9A

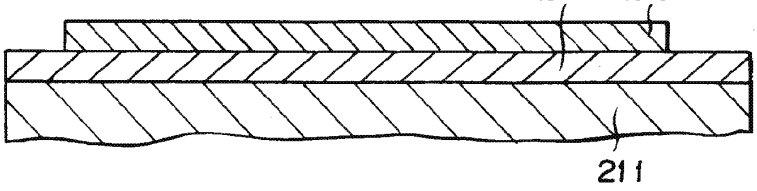


FIG. 9B

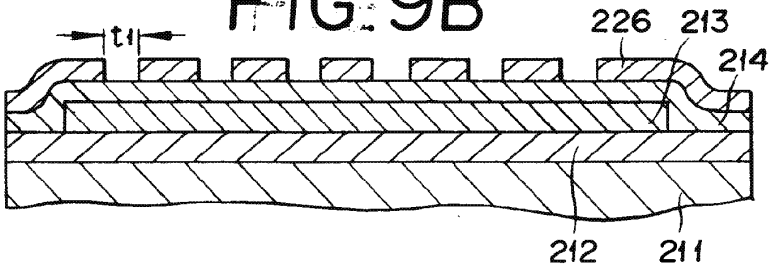


FIG. 9C

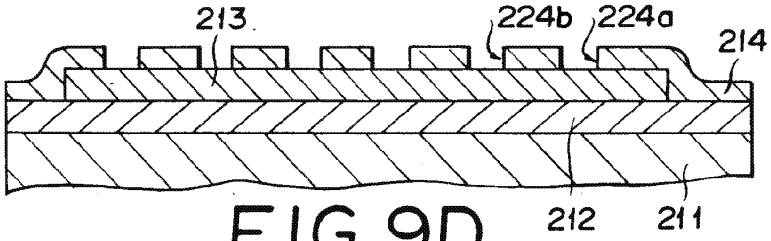


FIG. 9D

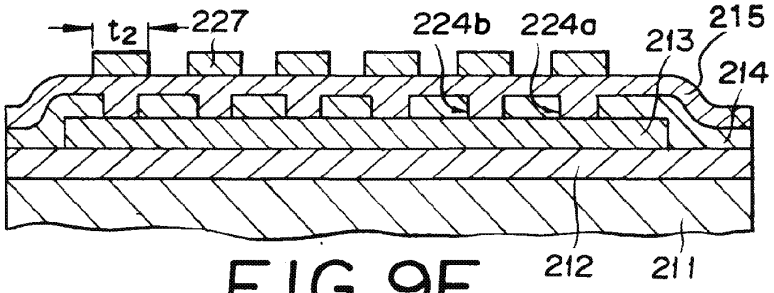
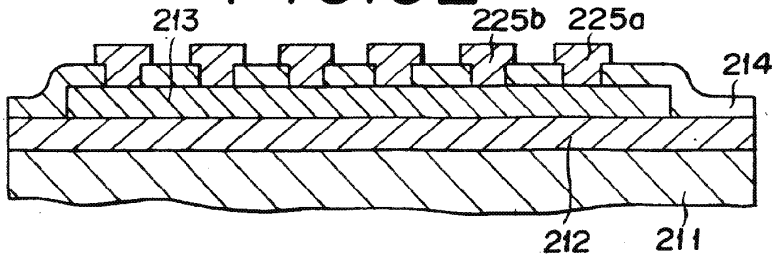


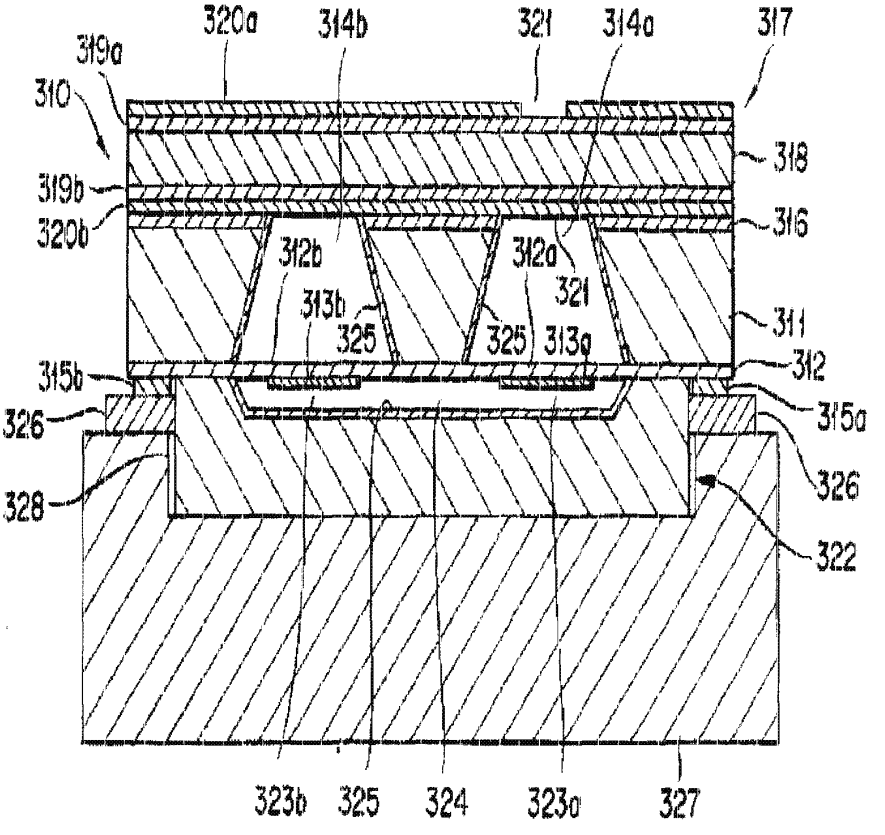
FIG. 9E



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FIG. 10



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FIG. 11

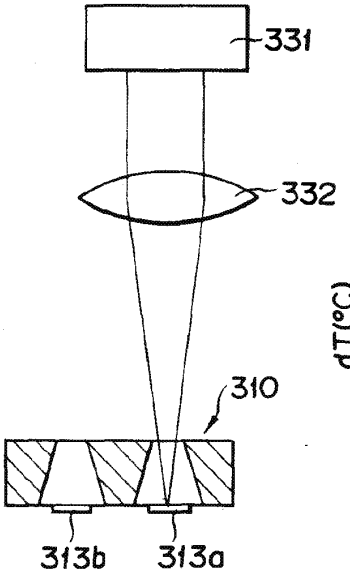


FIG. 13

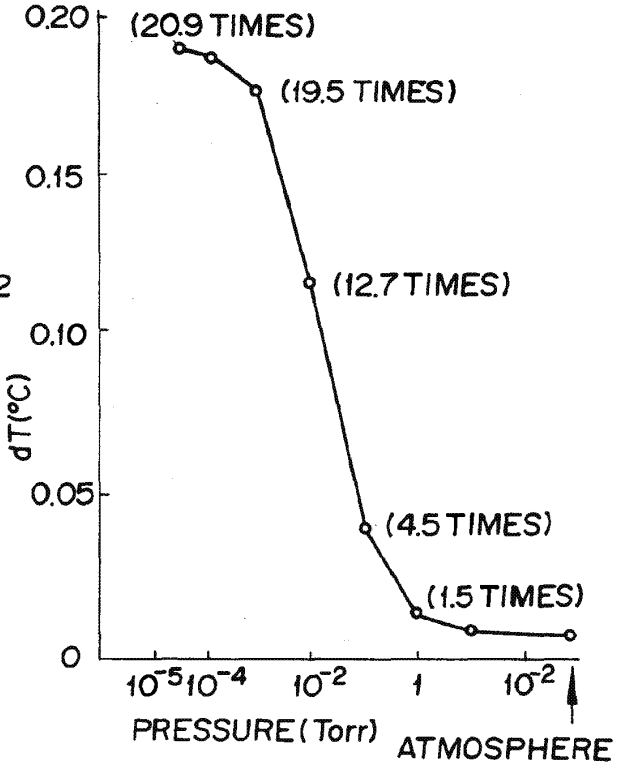
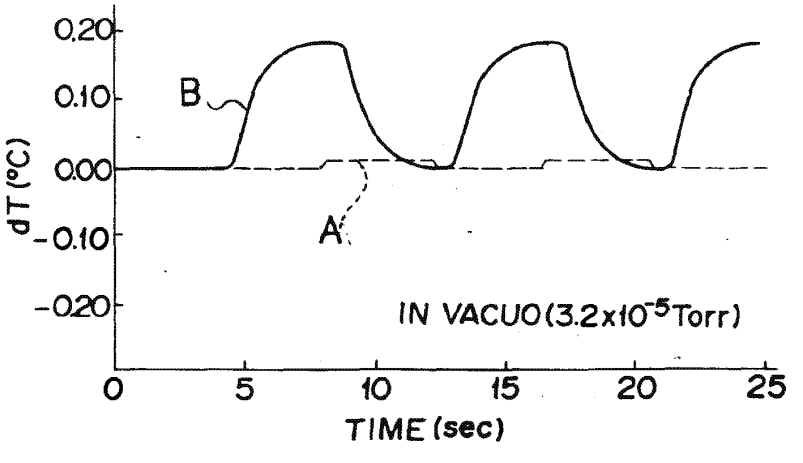


FIG. 12



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FIG. 14

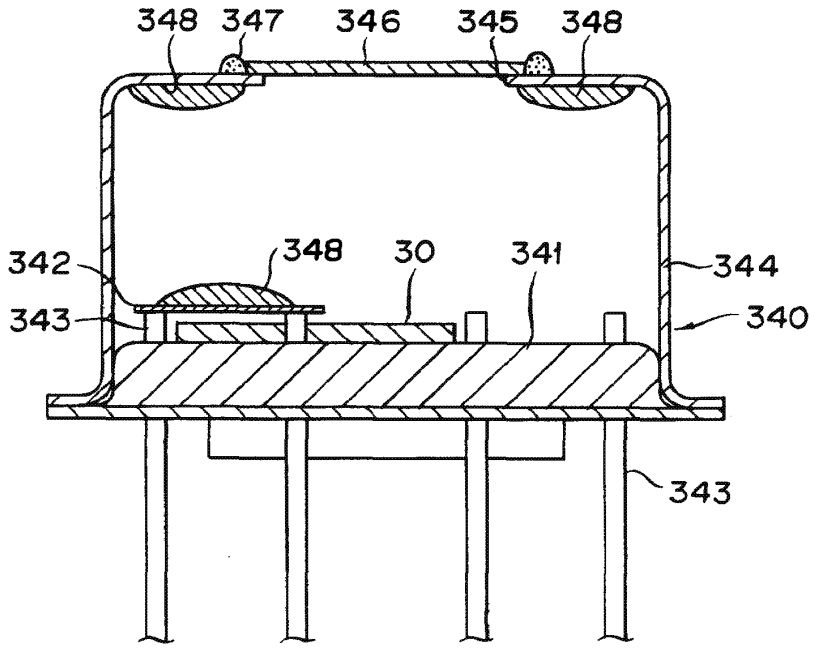
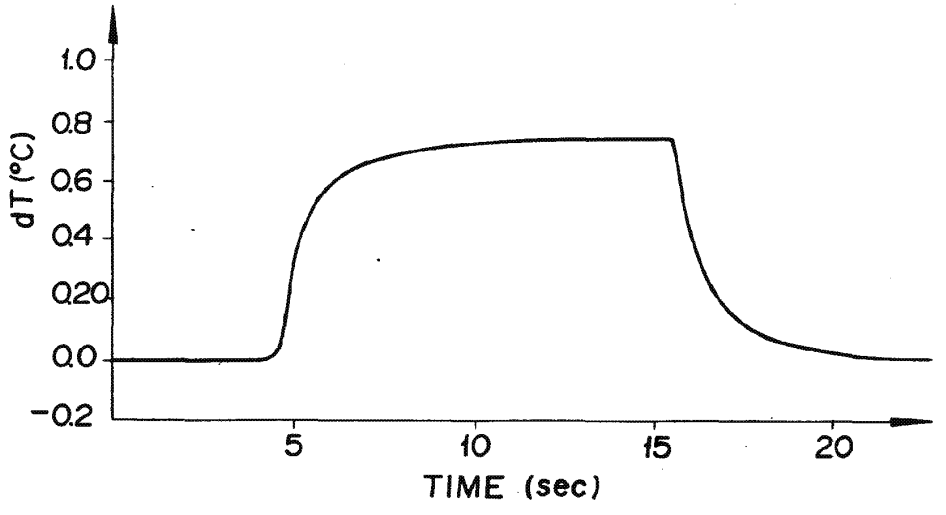


FIG. 15



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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 10 6318

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 453 372 (TERUMO KABUSHIKI KAISHA) * the whole document *	1-4,6,7, 10-12, 14-23	G01J5/20 H01L31/09
P,A	EP-A-0 523 716 (TERUMO KABUSHIKI KAISHA) * the whole document *	1-4,6,7, 10-12, 14-20, 22,23	
A	PATENT ABSTRACTS OF JAPAN vol. 014, no. 504 (P-1127)5 November 1990 & JP-A-22 10 230 (MITSUTERU KIMURA) 21 August 1990 * abstract *	1,2,10, 11,14, 18,21	
A	PATENT ABSTRACTS OF JAPAN vol. 015, no. 351 (E-1108)5 September 1991 & JP-A-31 36 379 (SATOU AKINOBU) 11 June 1991 * abstract *	1,2,10, 11,14, 18,21	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
A	DE-A-3 536 133 (ROBERT BOSCH GMBH) * the whole document *	1,10	G01J H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	16 JULY 1993	SCHEU M.

CATEGORY OF CITED DOCUMENTS

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(54) AN IMAGING DEVICE AND AN IMAGING METHOD

(57) An optical lens 1 makes three components of visible light and near infrared light in different wavelength regions severally form images at different locations according to their wavelengths. An imaging element 2 has a plurality of pixels, which include pixels having a visible light detection section 6 and pixels having a near infrared light detection section 8. The visible light detection section 6 has three detectors 3, 4, and 5 which detect three components of visible light which form images at locations of different depths in the same pixel according to their wavelengths. The near infrared light detection section 8 has a near infrared light detector 7 which detects near infrared light which forms an image at a location of a depth different from the depths at which the three components of visible light form images. Clear color images with good color reproducibility are obtained by the visible light detection section 6, and at the same time clear luminance information or monochrome images are obtained by the near infrared light detection section 8.

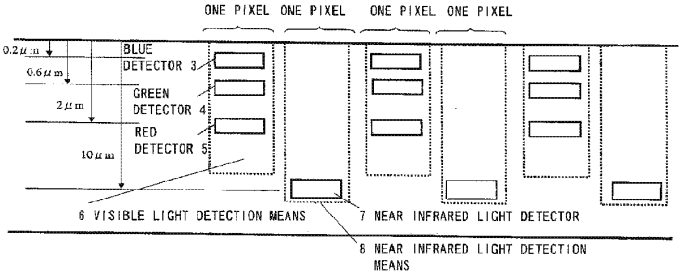


FIG. 3

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Description

Technical Field

[0001] The present invention relates to an imaging device and imaging method for detecting and receiving three components of visible light and near infrared light in different wavelength regions and for imaging pictures of both visible light and near infrared light.

Background Art

[0002] Conventional visible light and near infrared light imaging devices have a configuration in which each of pixels can detect one of three colors of different wavelengths in visible light and near infrared light and such pixels are arranged in a mixed manner in the same imaging element, for example a CCD or CMOS imaging element (e.g. see Figure 2 of Japanese Patent Laid-Open Application No . 2002-142228). For example, as shown in Figure 10, Mg (magenta) color detectors 81, Ye (yellow) color detectors 82, Cy (cyan) color detectors 83, and near infrared light detectors 84 are arranged on an imaging element like amosaic so that the combination repeats lengthwise and crosswise.

[0003] Here, one detector corresponds to just one pixel.

[0004] Incidentally, a bare pixel has a property of detecting visible light and near infrared light of 400 nm to 1000 nm. And an Mg color detector 81 is composed of a pixel covered with a bandpass filter for the region of the Mg color. The Ye color detectors 82 and Cy color detectors 83 are also composed of pixels covered with bandpass filters which derive the regions of their respective wavelengths. Bare pixels are arranged as the near infrared light detectors 84. Properly speaking, the visible light region requires to be cut off. But it need not be cut off because obtaining luminance information will suffice. The above configuration allows imaging pictures of both visible light and near infrared light.

[0005] In one of previously-suggested visible light imaging devices, three photodiodes are formed on a silicon substrate at different depths from the surface. This conventional device uses absorbance differences in silicon among three kinds of light of different wavelengths in the visible light region, e.g. blue, green, and red, to detect the three kinds of light of different wavelengths (e.g. see Figures 5 and 6 of Published Japanese Translation of PCT International Application (*Tokuhyo*) No. 2002-513145). In this visible light imaging device, three photodiodes of different depths can be arranged in one pixel. This prior art can therefore enable higher color resolution and prevent degradation of image quality caused by false color, in comparison with an art in which one pixel detects one color.

[0006] Figure 11 shows the structure of a pixel formed on an imaging element. An n-type doped region 92 of an n-type semiconductor is formed on a p-type semiconductor substrate 91. Similarly,a p-type doped region 93 is formed thereon. Moreover, an n-type doped region 94 is formed thereon. In this way, a three-layer semiconductor structure (triple-well structure) is made on the substrate. Since each pn interface region can function as a photosensor, three photosensors can be made up in total.

[0007] Now, as described in Figure 5 of Published Japanese Translation of PCT International Application (*Tokuhyo*) No. 2002-513145 as reference data, blue light is absorbed at a depth of 0.2μm in a silicon layer. Green is absorbed at 0.6μm, and red is not absorbed until it reaches a depth of 2μm. Accordingly, depths of interfaces, which work as photosensors for each light, are set to 0.2pm, 0.6μm, and 2μm respectively. Three colors (three wavelength bands) of light can thus be taken out almost spectrally. Then, an electric current generated by blue light is detected by a current detector 95. Similarly, green light is detected by a current detector 96, and red light is detected by a current detector 97. In this way, colors can be extracted numerically. Of course, it is actually impossible to separate light completely. But a degree of mixing of each color is known (or can be measured) in advance, so corrections can be made. The above-mentioned three-layer semiconductor doping structure allows one pixel to take out three colors of visible light and can realize a visible light imaging device with significantly improved color resolution.

[0008] However, in conventional visible light and near infrared light imaging devices such as the one described in the above-mentioned Japanese Patent Laid-Open Application No. 2002-142228, individual pixels can only detect one color (limited wavelength region). Other colors and luminance information need to be complemented with information from adjacent pixels. Because of this, color resolution and luminance resolution decrease, and false color, which is not the original color, appears.

[0009] In addition, an optical system comprising optical lenses commonly provides an image of a subject on the surface of an imaging element. Since focuses fundamentally differ depending on wavelengths, chromatic aberration occurs in imaged pictures (when one color comes into focus, the others go out of focus). So, as shown in Figure 12, for example, an optical system having a property of an achromatic lens is commonly provided so that an imaging element is within the depth of focus (color shift is negligible within the range) with regard to magenta, yellow, and cyan in the visible light region, and the optical system therefore focuses.

[0010] However, there is a limit to achromatism. It is difficult to make a perfect achromatic optical system for a very wide range of wavelengths from the visible light region to the near infrared light region (from 400nm to 1000nm). Even

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if it could be made, such optical system would be very expensive, so that it is difficult to use in current common industries (it is impossible to match all the focus points of visible light and near infrared light to each other). For this reason, when visible light and infrared light are detected on the same photosensitive surface, and if focused pictures are obtained in the visible light region, only out-of-focus pictures can be obtained in the near infrared light region. In other words, if an imaging element whose configuration is as described above were designed on paper, the optical system would be difficult to realize and it is highly likely that such an element could not be put in practical use.

[0011] Moreover, conventional visible light imaging devices such as described in Published Japanese Translation of PCT International Application (*Tokuhyo*) No. 2002-513145 are confined to three-layer semiconductor doping structure and are configured to detect visible light. For that reason, when three primary colors of visible light are to be detected, near infrared light cannot be detected. Suppose that the depth of a photodiode is readjusted such that visible light of two kinds of wavelength regions and near infrared light, a total of three kinds of light, can be detected. However, as described above, it is impossible to make a perfect achromatic optical system for a very wide range of wavelengths from the visible light region to the near infrared light region (from 400nm to 1000nm). So if visible light images are to be sharpened, near infrared light images go out of focus. After all, modification of an imaging element alone is insufficient for imaging clearly from visible light to near infrared light.

Disclosure of Invention

[0012] The present invention solves the conventional problems mentioned above. A purpose of the invention is to provide an excellent visible light and near infrared light imaging device and method which can obtain clear color images with good color reproducibility by a visible light detection means and can at the same time obtain clear luminance information or monochrome images by a near infrared light detection means.

[0013] The imaging device related to the invention comprises: an optical system means in which three components of visible light and near infrared light in different wavelength regions severally (or respectively) form images at different locations according to their wavelengths; and an imaging element which has a plurality of pixels; wherein said plurality of pixels include pixels having a visible light detection means and pixels having a near infrared light detection means, said visible light detection means detecting said three components of visible light which form images at locations of different depths in the same pixel according to their wavelengths, said near infrared light detection means detecting near infrared light which forms an image in a pixel at a location of a depth different from the depths at which said three components of visible light form images.

[0014] In the invention, the visible light detection means has three detectors which are provided at locations of different depths according to wavelength dependence of light absorption depth and detect visible light in three different wavelength regions of blue, green, and red, and the near infrared light detection means has a detector which is provided at a location of a depth different from the depths of the three detectors and detects near infrared light.

[0015] With such a configuration, clear color images with good color reproducibility can be obtained by a visible light detection means and at the same time clear luminance information or monochrome images can be obtained by a near infrared light detection means. As a result, for example, color images with good color reproducibility and high color resolution can be provided in the daytime; sharp monochrome images can be obtained even in a dark place, e.g. nighttime, by shining some light; and, moreover, composites of those images can equivalently increase the dynamic range. An excellent imaging device can thus be provided.

[0016] In the invention, the imaging element has a configuration in which pixels having the visible light detection means and pixels having the near infrared light detection means are alternately arranged in rows and columns.

[0017] With this configuration, a filter which can prevent the influence of near infrared light can be further added to the visible light detection means, so that color images with very good color reproducibility can be obtained.

[0018] In the invention, the imaging element has a configuration in which pixels having the visible light detection means and pixels having the near infrared light detection means are uniformly arranged such that the number ratio of the pixels is one to three.

[0019] In the invention, the imaging element has a configuration in which pixels having the visible light detection means and pixels having the near infrared light detection means are uniformly arranged such that the area ratio of the pixels is one to three.

[0020] In this way, two kinds of pixels are arranged such that the number ratio or area ratio is one to three, so that luminance resolution, rather than color resolution, can be improved and clear luminance information of a range up to the near infrared light region can be obtained.

[0021] An imaging device of another aspect of the invention comprises: an optical system means in which three components of visible light and near infrared light in different wavelength regions severally form images at different locations according to their wavelengths; and an imaging element which has a plurality of pixels; wherein the plurality of pixels have a detection means which detects the three components of visible light and the near infrared light which severally form images at locations of different depths in the same pixel according to their wavelengths.

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[0022] In the invention, the plurality of pixels comprise a detection means which detects three components of visible light of blue, green, and red and near infrared light by means of four detectors which are provided at locations of different depths according to wavelength dependence of light absorption depth.

[0023] In terms of color reproducibility and detection loss, such a configuration is inferior to a configuration in which different pixels detect visible light and near infrared light separately. However, there is an advantage that resolutions of both color images and near infrared images can similarly be improved.

[0024] In the invention, the optical system means has a configuration in which a focal length monotonously increases according to wavelengths of light from short-wavelength visible light to near infrared light so that visible light in three different wavelength regions of blue, green, and red and near infrared light form images at different locations.

[0025] With this configuration, clear pictures can be imaged in both visible light and near infrared light without being out of focus.

[0026] Moreover, an imaging method related to the invention comprises: making three components of visible light and near infrared light in different wavelength regions severally form images at different locations according to their wavelengths; detecting the three components of visible light and the near infrared light using the fact that wavelength dependence of light absorption depth varies; and imaging pictures of both the three components of visible light and the near infrared light.

[0027] With this configuration, clear color images with good color reproducibility can be obtained, and at the same time clear luminance information or monochrome images can be obtained. As a result, for example, color images with high color reproducibility and color resolution can be provided in the daytime; sharp monochrome images can be obtained even in a dark place, e.g. nighttime; and, moreover, composites of those images can equivalently increase the dynamic range. An excellent imaging method can thus be provided.

[0028] As described above, clear color images with good color reproducibility can be obtained and clear luminance information or monochrome images can be obtained according to the invention.

Brief Description of Drawings

[0029]

Figure 1 illustrates a visible light and near infrared light imaging device and method related to the invention, and shows the essence of an optical system of the invention.
Figure 2 shows the relation between the focal length of the optical system related to the invention and wavelengths.
Figure 3 shows a configuration of an imaging element related to a first embodiment of the invention.
Figure 4 shows a configuration of an imaging element related to the first embodiment of the invention.
Figure 5 is an equivalent circuit schematic of an imaging element related to the first embodiment of the invention.
Figure 6 shows an example of a mixed arrangement of visible light detection sections and near infrared light detection sections on an imaging element related to the first embodiment of the invention.
Figure 7 shows an example of a mixed arrangement of visible light detection sections and near infrared light detection sections on an imaging element related to the first embodiment of the invention.
Figure 8 shows a configuration of an imaging element related to a second embodiment of the invention.
Figure 9 is an equivalent circuit schematic of an imaging element related to the second embodiment of the invention.
Figure 10 shows an example of an imaging element of a conventional visible light and near infrared light imaging device.
Figure 11 shows an example of an imaging element of a conventional visible light imaging device.
Figure 12 illustrates an achromatic optical system used in a conventional visible light imaging device.

Best Mode of Embodying the Invention

[0030] Each embodiment of the invention will now be described with reference to the drawings.

<First Embodiment>

[0031] As shown in Figure 1, a visible light and near infrared light imaging device related to the invention has an optical lens 1. The optical lens 1 is an optical system whose focal length is variable according to wavelengths, and makes three components of visible light and near infrared light in different wavelength regions form images at different locations according to their wavelengths. The optical lens 1 condenses light from an external subject and forms an image on an imaging element 2. In the lower part of Figure 1, light pencils from the optical lens 1 are shown separately by different wavelengths.

[0032] The optical lens 1 forms images at different locations according to wavelengths as described above. This is

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shown more specifically in Figure 2. For example, if blue of 470nm is a focal-point reference A, the focal length of green of 520nm is 0.4μm longer than the reference A. Similarly, the focal length of red of 700nm is 2μm longer than the reference A, and the focal length of near infrared of 1000nm is 10μm longer than the reference A. As shown in Figure 2, the focal length of the optical lens 1 increases according to wavelengths, from that of short-wavelength light in visible light to near infrared light, and therefore three components of visible light and near infrared light form images at different locations.

[0033] On the other hand, the imaging element 2 composes a light receiving section together with the optical lens 1 qua an optical system. Figure 3 schematically shows the configuration of the imaging element 2. As shown in Figure 3, visible light detection sections 6 and near infrared light detection sections 8 are arranged in the imaging element 2. The visible light detection section 6 comprises three detectors of different depths, and it detects with these three detectors three components of visible light in different wavelength regions which are condensed by the optical lens 1 and form images, using the fact that wavelength dependence of light absorption depth varies. The near infrared light detection section 8 has a detector which detects near infrared light.

[0034] The visible light detection section 6 is composed of a blue detector 3, a green detector 4, and a red detector 5. These detectors 3 to 5 are photodiodes located at different depths from the surface. Three primary colors are obtained separately, so that any color is reproducible. Unlike the conventional Japanese Patent Laid-Open Application No. 2002-142228, one pixel can obtain output of three colors in visible light. As described in explanations of conventional arts, it is actually impossible to separate light into three colors completely. But a degree of mixing of each color is known (or can be measured) in advance, so corrections can be made.

[0035] The infrared light detection section 8 is composed of a near infrared light detector 7, which is a photodiode. In order to detect near infrared light mainly, the near infrared light detector 7 is located around the depth of the highest detectability. As described in Published Japanese Translation of PCT International Application (*Tokuhyo*) No. 2002-513145 as reference data, near infrared light is absorbed at a depth deeper than red light in a silicon layer. So, the near infrared light detector 7 is located, for example, at the depth of 10μm. Luminance information can be obtained from the visible light detector 6 by combining three colors with one another. If output from the near infrared light detector 7 is to be in proportion to overall light intensity, output from the near infrared light detector 7 may be used as luminance information.

[0036] Figure 4 shows the configuration of the imaging element 2 related to the first embodiment. As shown in Figure 4, the configuration of the visible light detection section 6 on the left of the figure is almost similar to the conventional example. An n-type doped region 10 of an n-type semiconductor is formed on a p-type semiconductor substrate 9. Similarly, a p-type doped region 11 is formed thereon. Moreover, an n-type doped region 12 is formed thereon. In this way, a three-layer semiconductor structure (triple-well structure) is made on the substrate. Three current detectors 14, 15, and 16 detect output of B, G, and R of visible light. But if the three colors are somewhat influenced by near infrared light, colors reproduced later may be different from real colors. In order to avoid this, a near infrared light cut filter 13 is placed in front of the light entrance to the current detectors. The influence of light in the near infrared region is thus eliminated.

[0037] On the other hand, in the near infrared light detection section 8 on the right of Figure 4, an n-type doped region 17 of an n-type semiconductor is formed additionally on the p-type semiconductor substrate 9. With the pn junction reversely biased (the n side is at higher potential than the p side), the current detector 18 detects a current when near infrared light comes in. In Figure 4, the pn junction surface, that is, the near infrared light detector 7 in Figure 3, is provided at the depth of 10μm. In this way, the near infrared light detector 7 is located where detectability for near infrared light is the highest. However, near infrared light has a very wide wavelength range from 770nm to 1000nm. Accordingly, the above-mentioned value may vary depending on the purpose of detection, i.e. which wavelength region is to be mainly detected.

[0038] Now, by means of the optical lens 1 described in Figures 1 and 2, light in desired wavelength regions focuses on each detection area of the four current detectors 14, 15, 16, and 18. In other words, light of desired color comes into focus on a detection area of each detector. In order to realize this, the optical lens 1 is deliberately provided with aberration.

[0039] In Figure 4, visible light entering the near infrared light detection section 8 on the right would cause defocusing. Most visible light is absorbed until it reaches around the photodiode detection area, i.e. the pn interface, but some visible light that comes through without being absorbed may become a factor of defocusing. So, as shown in Figure 4, a visible light cut filter 27 may be added in front of the light entrance.

[0040] Figure 5 shows an equivalent circuit schematic. As shown in Figure 5, each photodiode is reversely biased, and currents corresponding to incoming light are detected. In the interests of simplicity, power supply and grounds are common in the equivalent circuit schematic of Figure 5. However, the invention is not limited to this.

[0041] Figures 6 and 7 show examples of actual arrangements of visible light detection sections 6 and near infrared light detection sections 8.

[0042] In Figures 6 and 7, visible light detection sections 6 and near infrared light detection sections 8 are arranged in a mixed manner. In Figure 6, a visible light detector 30 composes the visible light detection section 6 and a near

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infrared light detector 31 composes the near infrared light detection section 8. In Figure 6, the visible light detectors 30 and the near infrared light detectors 31 are alternately arranged in rows and columns in a mixed manner, and the ratio of the number or area of both pixels is one to one. As for visible light information in the area of the near infrared light detection section 8, an average for adjacent visible light detection sections 6 may be taken. Generally, resolution of color information may be lower than luminance resolution assuming that the use is humans' seeing images. However, this arrangement has higher resolution in both luminance and color than, for example, the conventional Japanese Patent Laid-Open Application No. 2002-142228.

[0043] Output from the near infrared light detection section 8 is useful as luminance information for detecting near infrared light in a relatively wide wavelength region. Sunlight especially contains a lot of near infrared light components. There are some cases where luminance information is obtained with a rather better S/N ratio from near infrared light than from the three RGB colors. Therefore, luminance information is obtained from adjacent near infrared light detection section 8. Alternatively, information from the near infrared light detection section 8 is used to correct output from the visible light detection section 6.

[0044] For example, luminance can usually be obtained by the following equation 1 when RGB is known.

$$Y = 0.299 \times R + 0.587 \times G + 0.114 \times B \quad \ldots (1)$$

[0045] In the equation 1, luminance is a linear sum of RGB.

[0046] In contrast to this, luminance may be obtained by the following equation 2 when average luminance information I is derived from a plurality of adjacent near infrared light detection sections 8.

$$Y = c1 \times R + c2 \times G + c3 \times B + c4 \times I \quad \ldots (2)$$

(where c1 + c2 + c3 + c4 = 1)

[0047] Figure 7 shows a configuration in which luminance information from near infrared light is actively used. With the configuration in Figure 7, the S/N ratio and resolution of luminance information can be improved. Again in Figure 7, the visible light detector 30 composes the visible light detection section 6 and the near infrared light detector 31 composes the near infrared light detection section 8. Besides that, the visible light detectors 30 and the near infrared light detectors 31 are alternately arranged in rows and columns in a mixed manner. However, the ratio of the number or area of visible light detection sections 6 to that of near infrared light detection sections 8 is one to three in Figure 7. More specifically, a set of one pixel of the visible light detection section 6 (visible light detector 30) and three pixels of the near infrared light detection sections (near infrared light detectors 31) is arranged in a square, and the sets are arranged in rows and columns. In this way, they are uniformly arranged in the ratio of one to three. Here, if luminance is obtained from a linear sum of three components of visible light, local fluctuations in RGB may cause luminance to fluctuate, which becomes noise. However, with the configuration in Figure 7, luminance resolution, rather than color resolution, can be improved. As a result, clear luminance information can be obtained for the range up to near infrared light.

<Second Embodiment>

[0048] Next, Figure 8 shows a configuration of an imaging element related to a second embodiment, and Figure 9 is an equivalent circuit schematic of an imaging element related to the second embodiment. In the imaging element shown in Figure 8, a visible light detection section and near infrared light detection section are placed in one pixel. The figure shows one pixel, which comprises a detection section to separate and detect three components of visible light and near infrared light in different wavelength regions, four components in total. In other words, four current detectors 23, 24, 25, and 26 arranged in one pixel detect B, G, and R of visible light and near infrared light.

[0049] As shown in Figure 8, an n-type doped region 19 of an n-type semiconductor is formed on a p-type semiconductor substrate 9.

[0050] Similarly, a p-type doped region 20 is formed thereon. Moreover, an n-type doped region 21 is formed thereon. Furthermore, a p-type doped region 22 is formed thereon. In this way, a four-layer semiconductor structure (quadruple-well structure) is made on the substrate. Since each pn interface region functions as a photosensor, four photosensors can be made up in total. The depth of each interface, i.e. detection area, is determined and controlled as previously described. Light in four wavelength regions of blue, green, red, and near infrared light can thus be detected. Actually, it is difficult to separate four colors of light completely, and a mixture occurs. But a degree of mixing of each color is known (or can be measured) in advance, so corrections can be made.

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[0051] Figure 9 is an equivalent circuit schematic of Figure 8. Four photodiodes are reversely biased, and currents corresponding to incoming light are detected. In the interests of simplicity, power supply and grounds are common. However, the invention is not limited to this.

[0052] In the above-described second embodiment, the mixing of visible light into near infrared light is unavoidable. As a result, color reproducibility may be slightly worse in the second embodiment than in the first embodiment even if corrections are made. However, there is an advantage that resolution of both color and luminance is better because one pixel simultaneously processes four colors. Incidentally, visible light is separated into three wavelength regions in the embodiment, but it may be separated into four or more wavelength regions. In this case, good color images with higher color reproduction and resolution can be obtained.

[0053] While there has been described what are at present considered to be preferred embodiments of the invention, it will be understood that various modifications may be made thereto, and it is intended that appended claims cover all such modifications as fall within the true spirit and scope of the invention.

Industrial Applicability

[0054] As described above, good color images and near infrared light images can be obtained according to the invention, and the invention is useful as an imaging device and method or the like.

Claims

1. An imaging device comprising:

   an optical system means in which three components of visible light and near infrared light in different wavelength regions severally form images at different locations according to their wavelengths; and
   an imaging element which has a plurality of pixels;

   wherein said plurality of pixels include pixels having a visible light detection means and pixels having a near infrared light detection means, said visible light detection means detecting said three components of visible light which form images at locations of different depths in the same pixel according to their wavelengths, said near infrared light detection means detecting near infrared light which forms an image in a pixel at a location of a depth different from the depths at which said three components of visible light form images.

2. The imaging device according to claim 1, wherein said visible light detection means has three detectors which are provided at locations of different depths according to wavelength dependence of light absorption depth and detect visible light in three different wavelength regions of blue, green, and red, and said near infrared light detection means has a detector which is provided at a location of a depth different from the depths of said three detectors and detects near infrared light.

3. The imaging device according to claim 1, wherein said imaging element has a configuration in which pixels having said visible light detection means and pixels having said near infrared light detection means are alternately arranged in rows and columns.

4. The imaging device according to claim 1, wherein said imaging element has a configuration in which pixels having said visible light detection means and pixels having said near infrared light detection means are uniformly arranged such that the number ratio of the pixels is one to three.

5. The imaging device according to claim 1, wherein said imaging element has a configuration in which pixels having said visible light detection means and pixels having said near infrared light detection means are uniformly arranged such that the area ratio of the pixels is one to three.

6. An imaging device comprising:

   an optical system means in which three components of visible light and near infrared light in different wavelength regions severally form images at different locations according to their wavelengths; and
   an imaging element which has a plurality of pixels;
   wherein said plurality of pixels detect said three components of visible light and said near infrared light which severally form images at locations of different depths in the same pixel according to their wavelengths.

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7. The imaging device according to claim 6, wherein said plurality of pixels detect three components of visible light of blue, green, and red and near infrared light by means of four detectors which are provided at locations of different depths according to wavelength dependence of light absorption depth.

8. The imaging device according to claim 1, wherein said optical system means provides a focal length which monotonously increases according to wavelengths of light from short-wavelength visible light to near infrared light so that visible light in three different wavelength regions of blue, green, and red and near infrared light form images at different locations.

9. The imaging device according to claim 7, wherein said optical system means provides a focal length which monotonously increases according to wavelengths of light from short-wavelength visible light to near infrared light so that visible light in three different wavelength regions of blue, green, and red and near infrared light form images at different locations.

10. An imaging method comprising:

making three components of visible light and near infrared light in different wavelength regions severally form images at different locations according to their wavelengths;
detecting said three components of visible light and said near infrared light using the fact that wavelength dependence of light absorption depth varies; and
imaging pictures of both said three components of visible light and said near infrared light.

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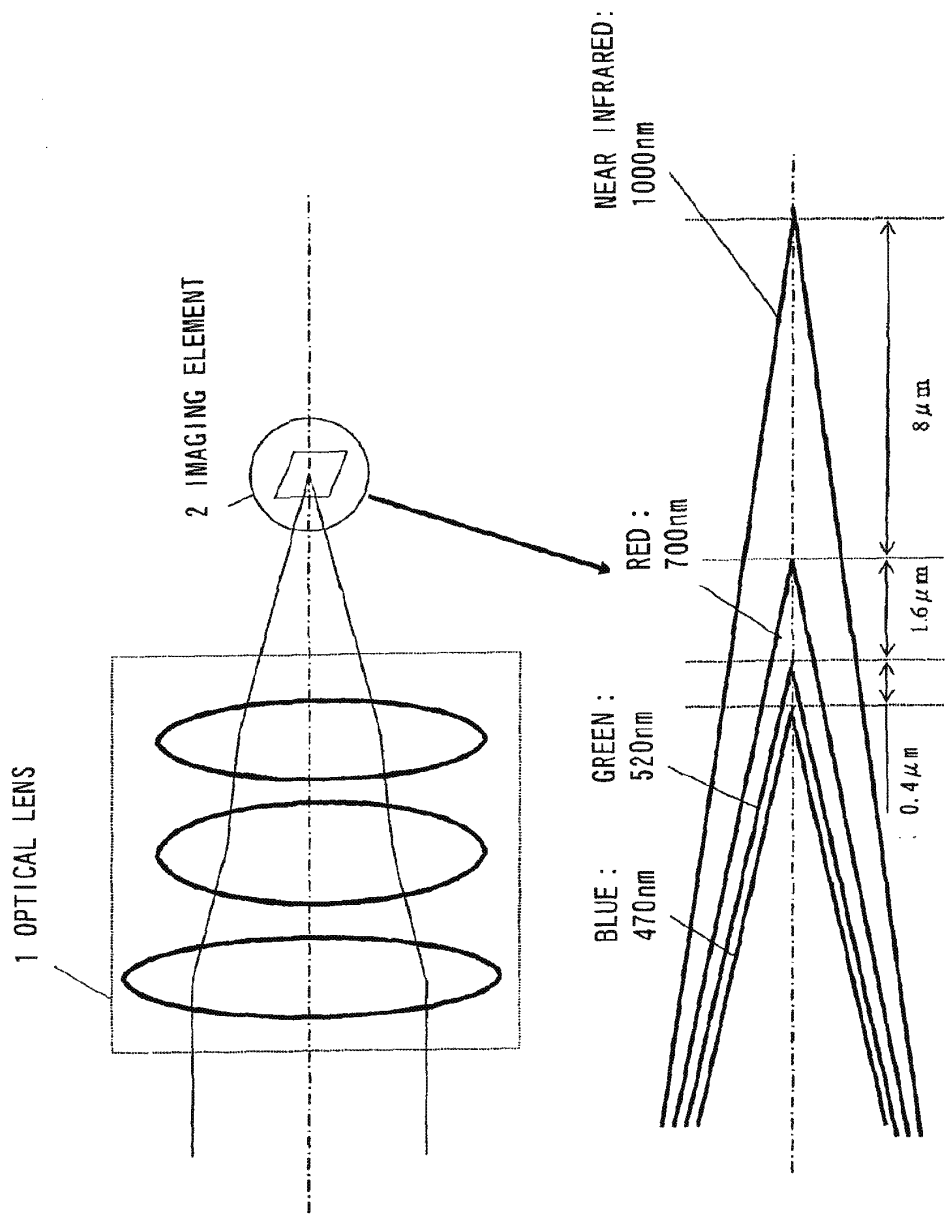


FIG. 1

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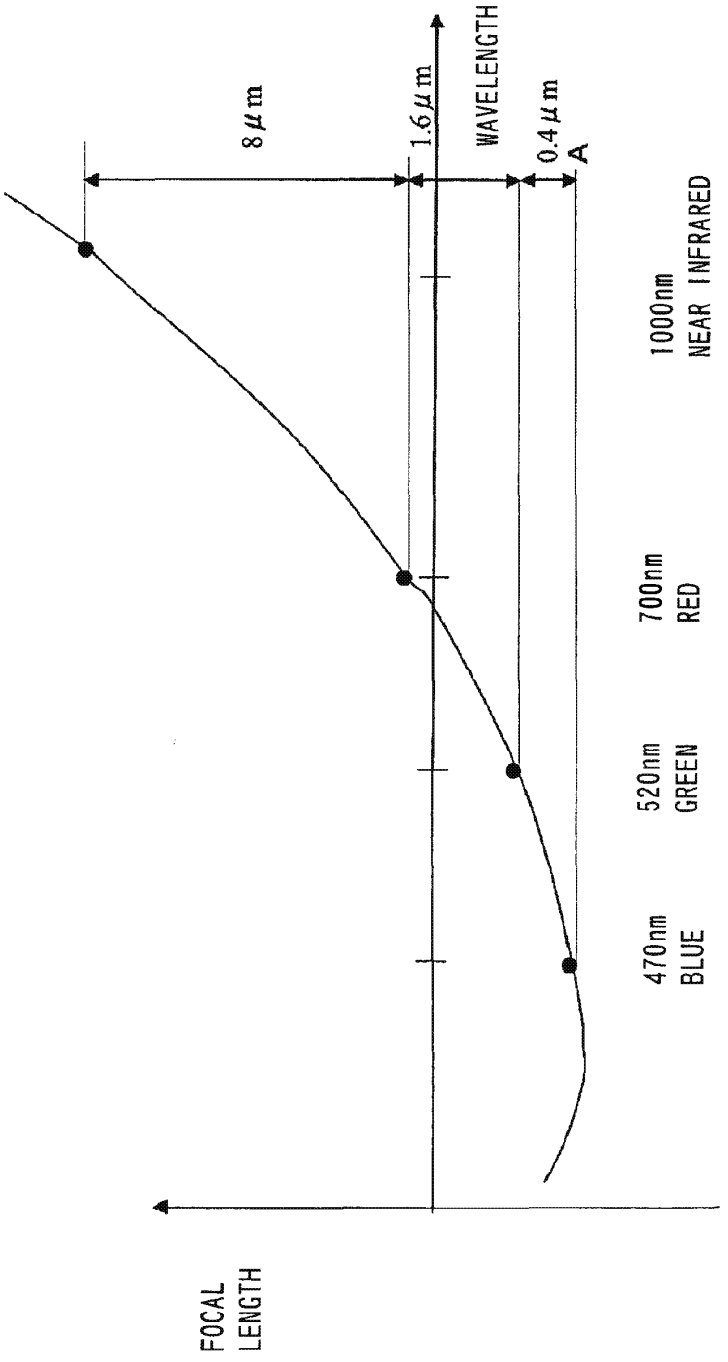


FIG. 2

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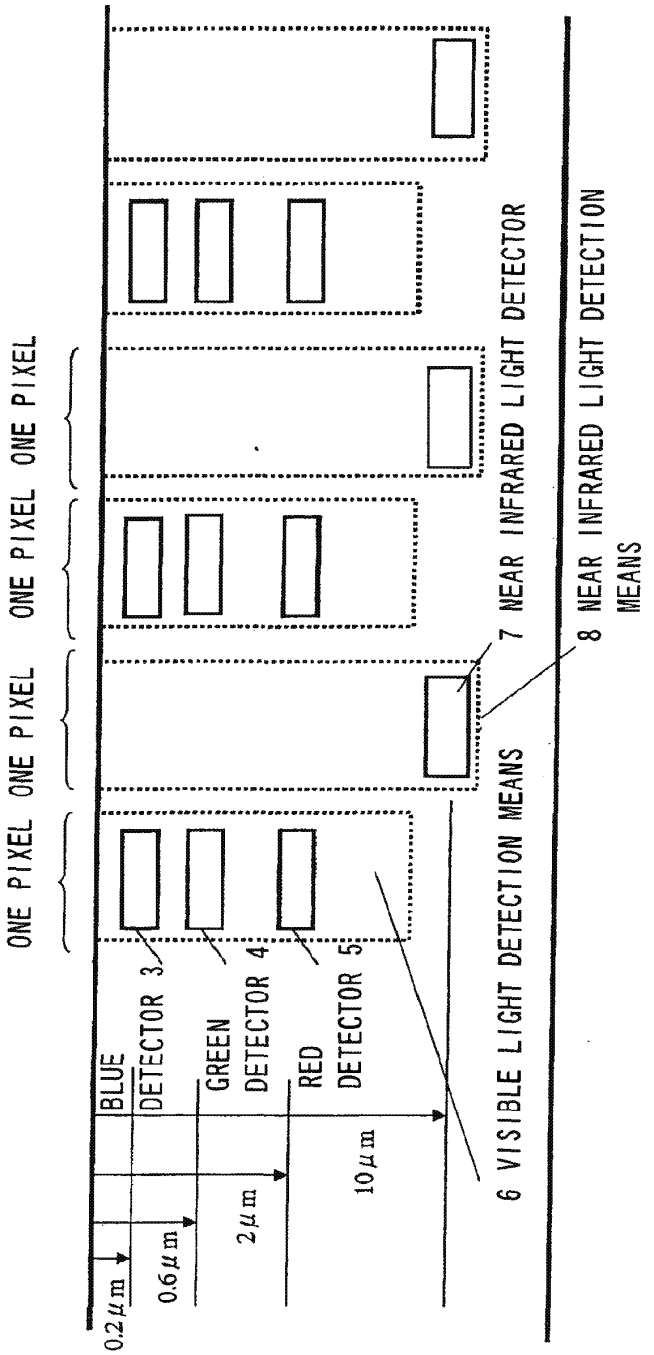


FIG. 3

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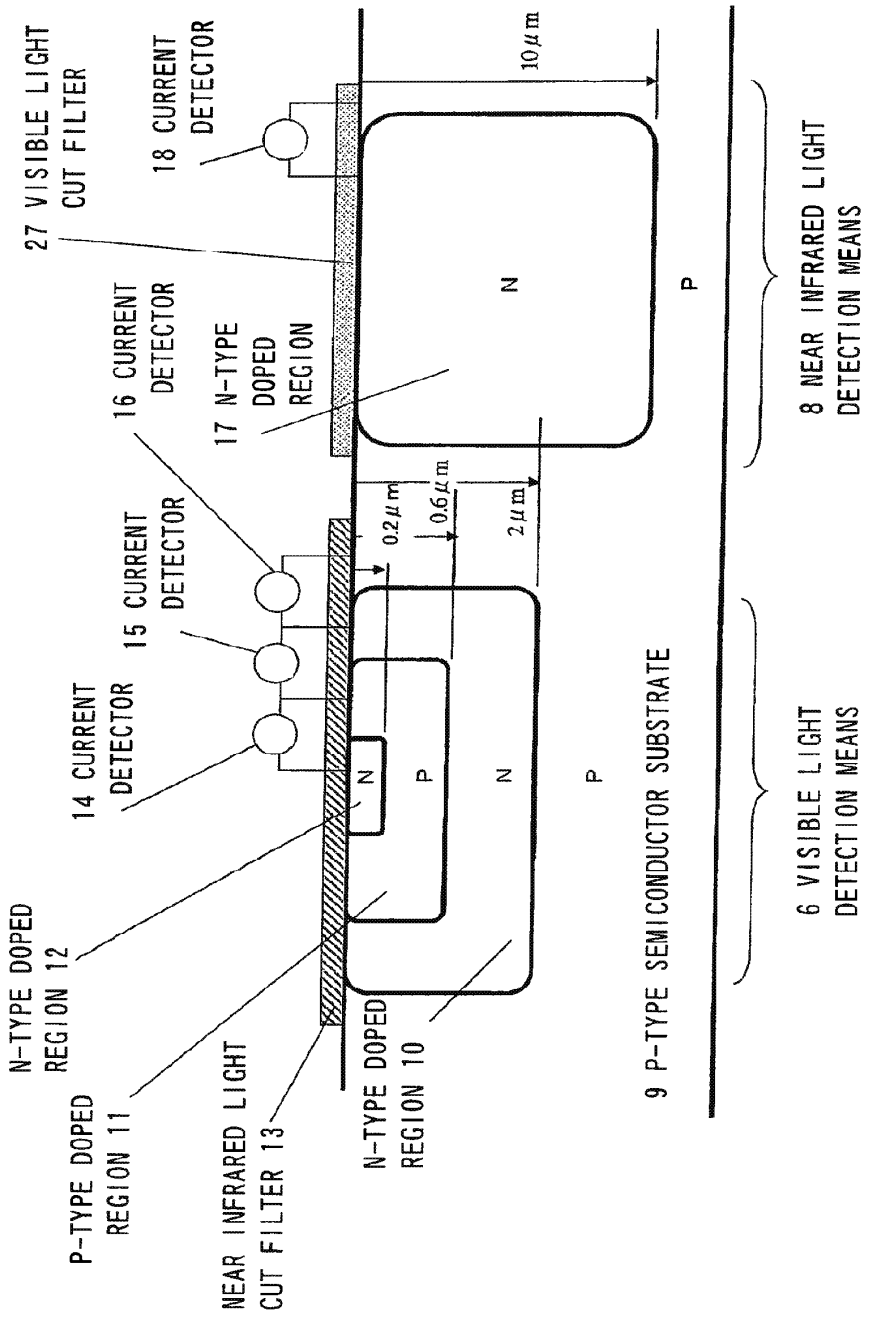


FIG. 4

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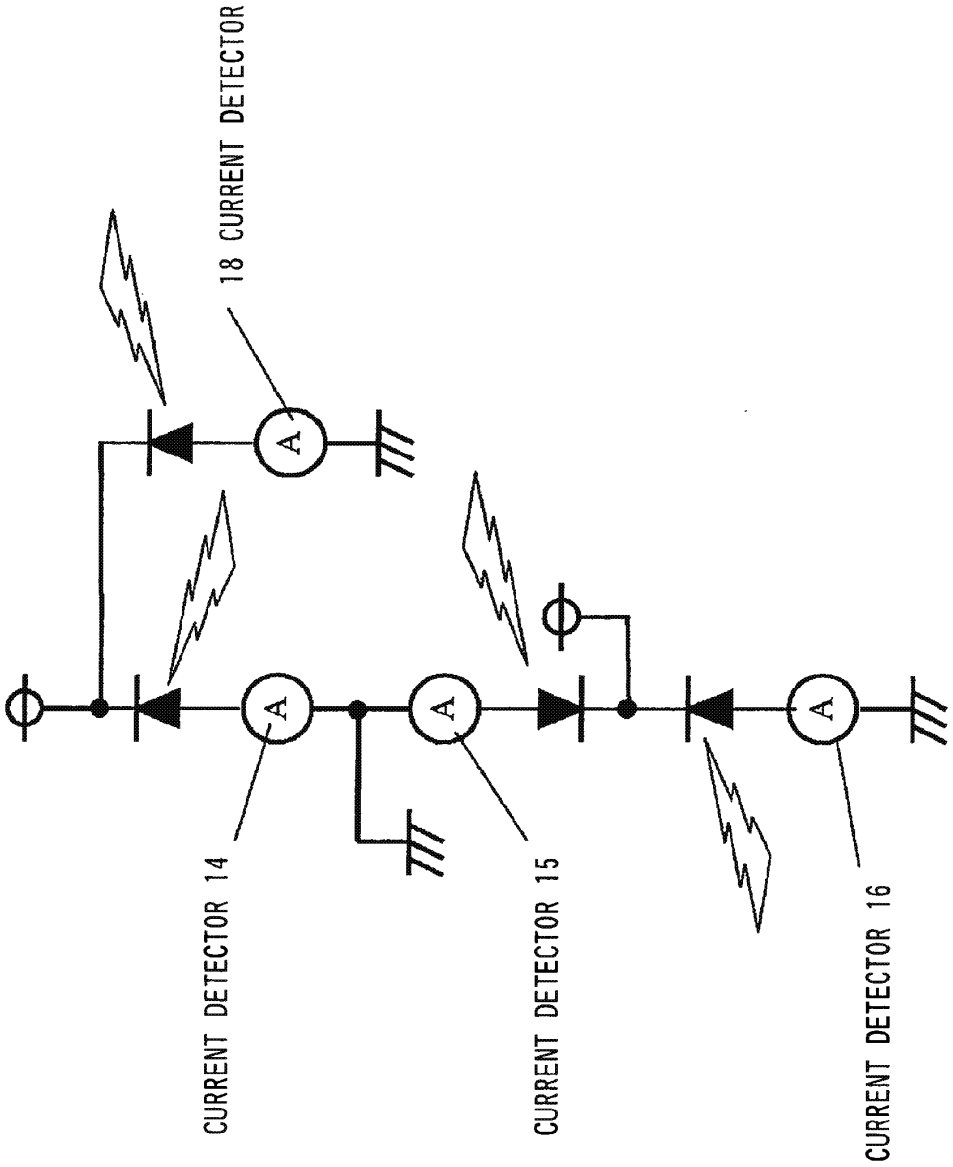


FIG. 5

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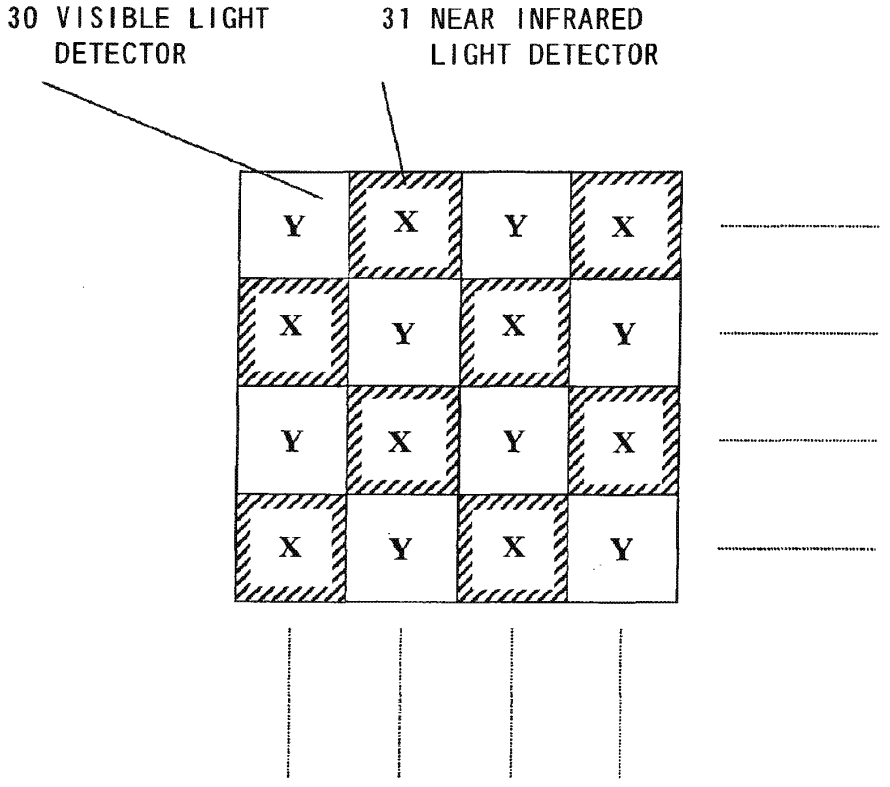


FIG. 6

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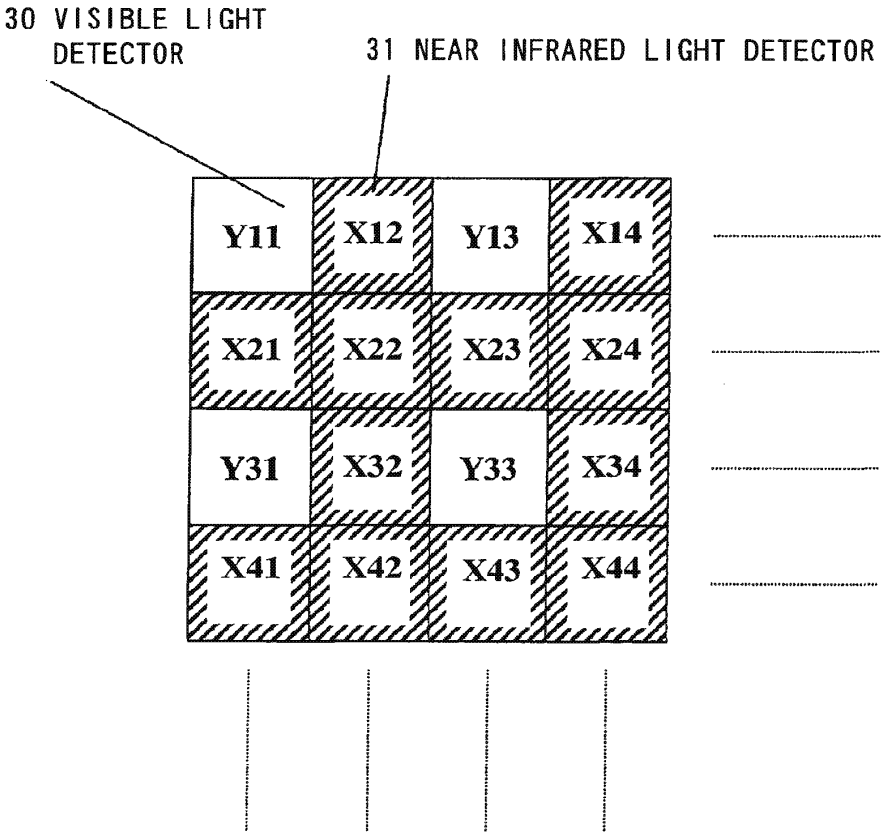


FIG. 7

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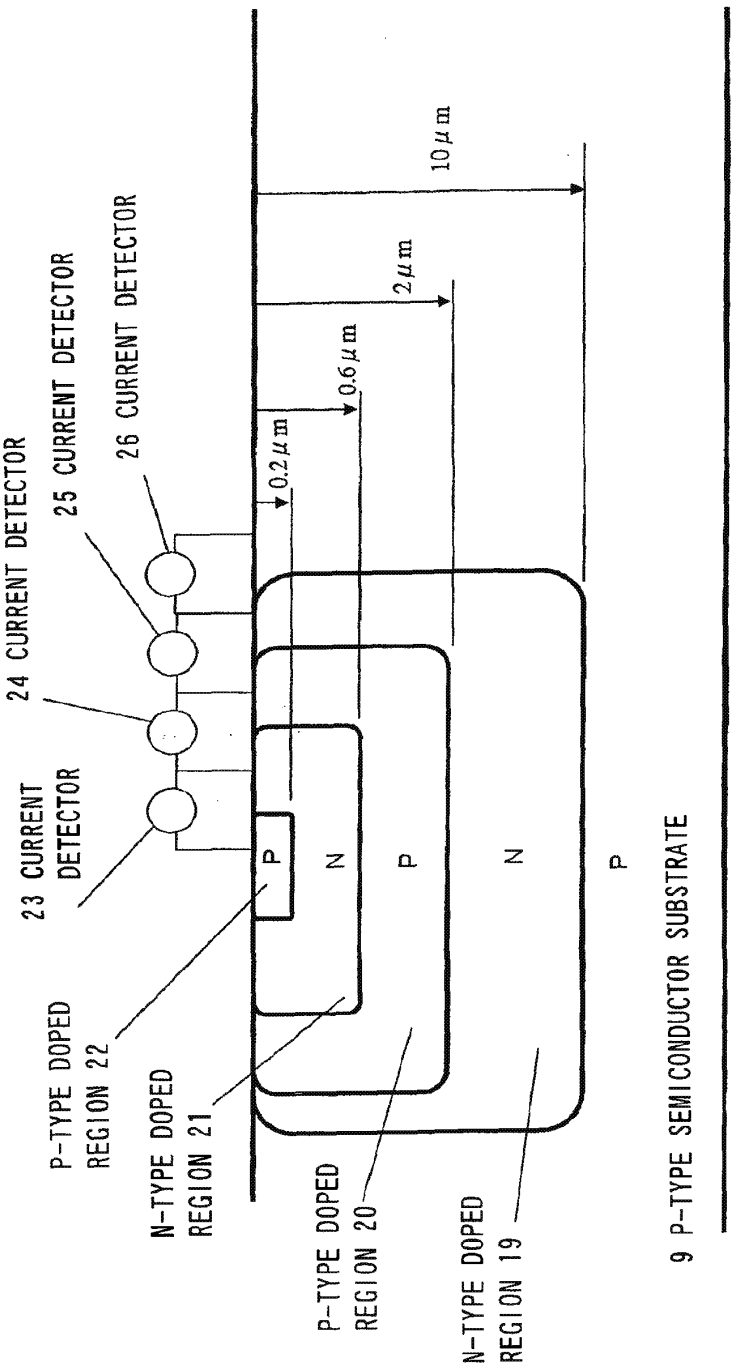


FIG. 8

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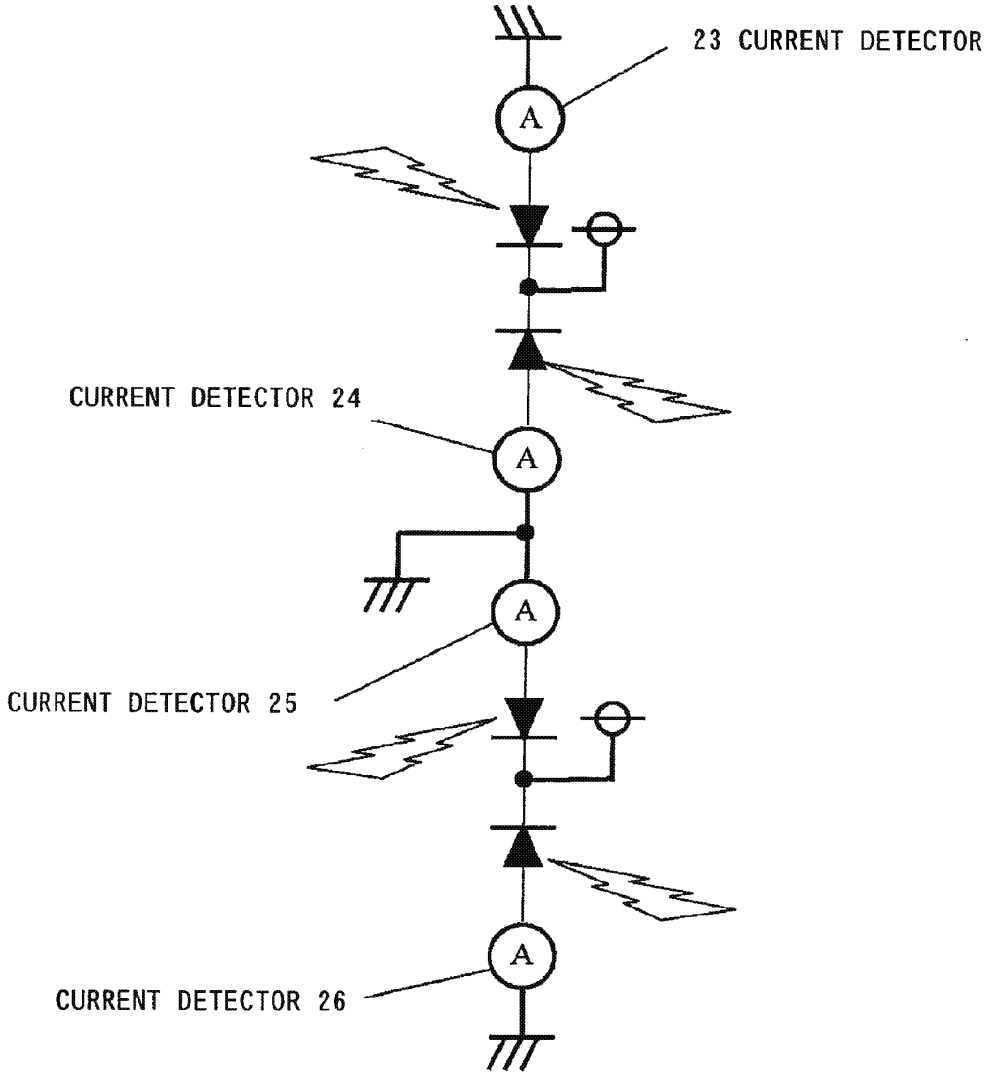


FIG. 9

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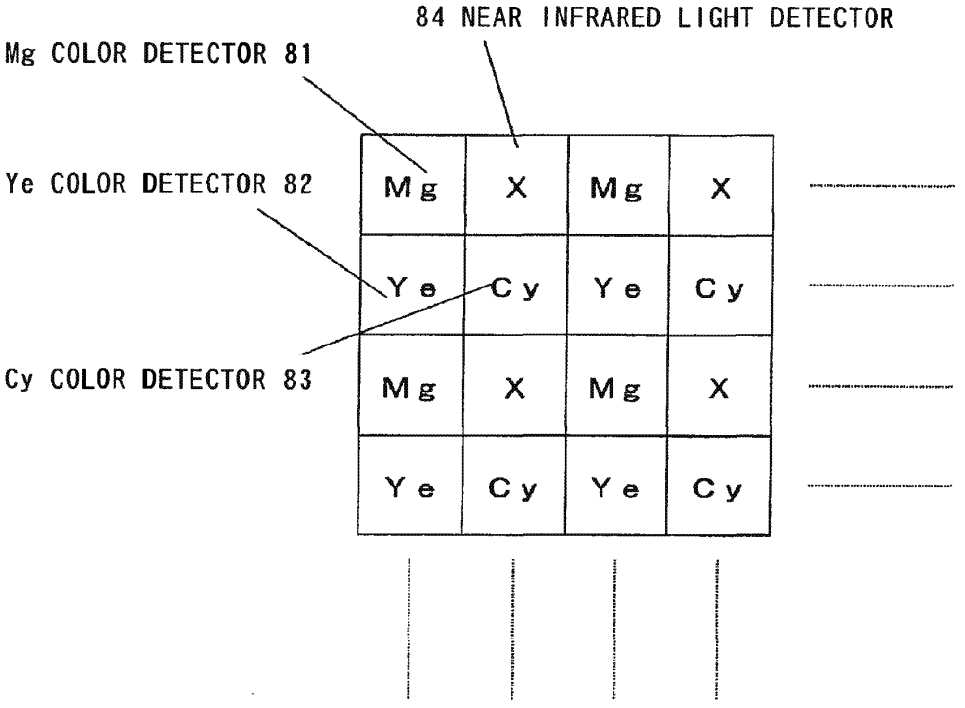


FIG. 10

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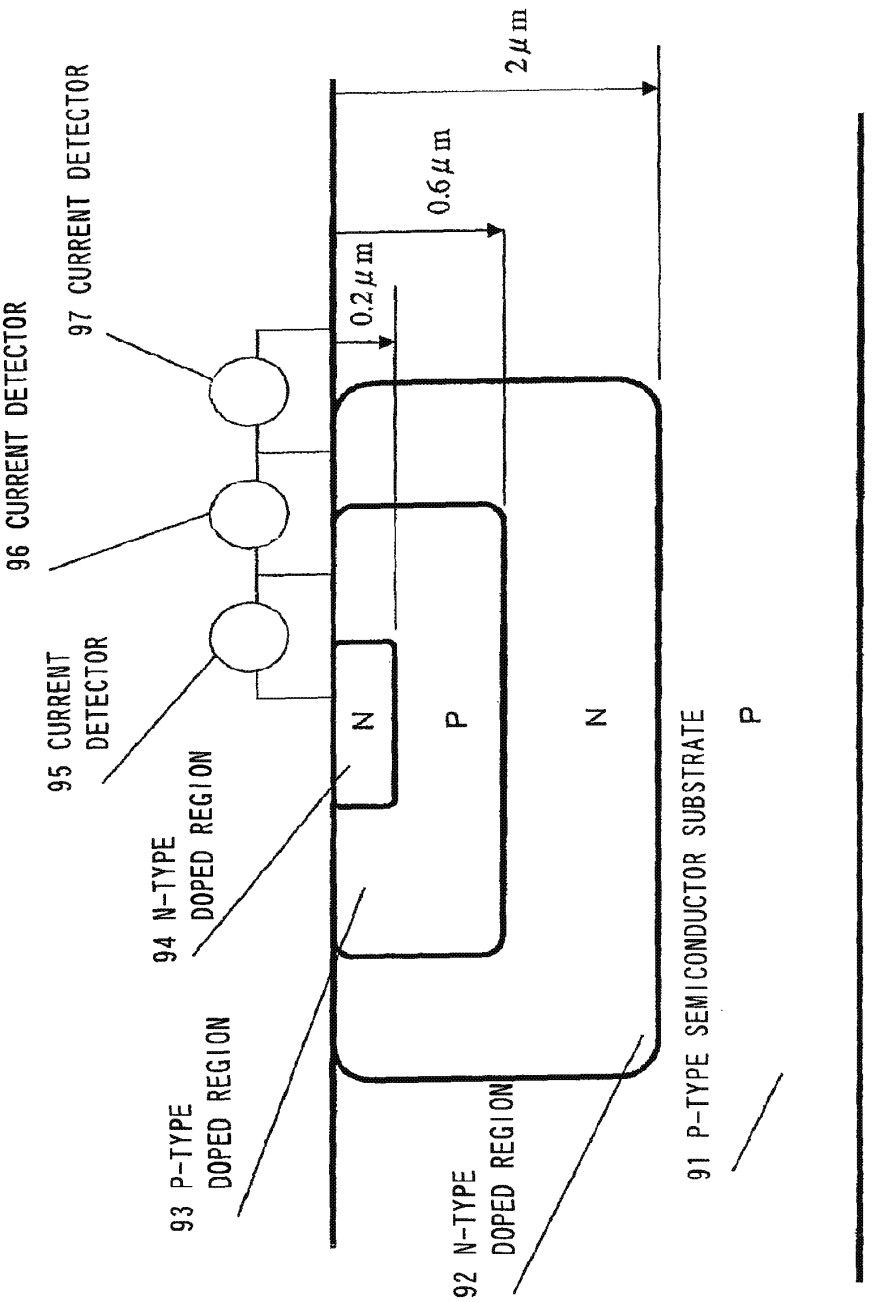


FIG. 11

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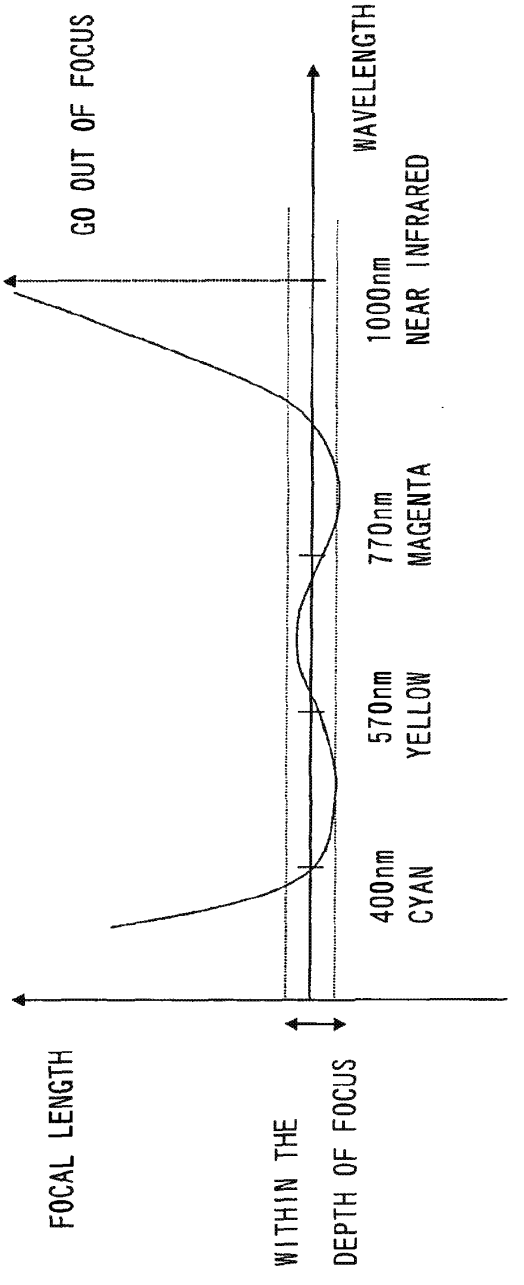


FIG. 12

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2004/005799

A. CLASSIFICATION OF SUBJECT MATTER
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H01L27/146, H01L31/10, H04N5/335

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2004
Kokai Jitsuyo Shinan Koho 1971-2004 Toroku Jitsuyo Shinan Koho 1994-2004

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 7-74340 A (Toshiba Corp.), 17 March, 1995 (17.03.95), Full text; all drawings (Family: none)	1-10
A	JP 55-52277 A (Recognition Equipment Inc.), 16 April, 1980 (16.04.80), Full text; all drawings & US 4238760 A & NL 7907416 A & GB 2034971 A & FR 2438344 A1 & DE 2940343 A1	1-10
A	JP 2003-304548 A (Canon Inc.), 24 October, 2003 (24.10.03), Full text; all drawings & US 2003/193011 A1	1-10

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
05 July, 2004 (05.07.04)	20 July, 2004 (20.07.04)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (January 2004)

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2004/005799

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 6-205162 A (Canon Inc.), 22 July, 1994 (22.07.94), Full text; all drawings & CA 2112734 A & DE 69329990 D & EP 605259 A2 & US 5724152 A	1-10

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(54) Photovoltaic device which includes all-back-contact configuration; and related fabrication processes

(57) A semiconductor structure is described, which includes a semiconductor substrate (10) of one conductivity type, having a front surface (12) and a back surface (14). A first amorphous semiconductor layer (16) is applied on the front surface (12); and second (22) and third (32) amorphous semiconductor layers are disposed on portions of the back surface (14) of the substrate (10). The second and third layers are each compositionally graded through their depth, from substantially intrinsic at the interface with the substrate (10), to substantially conductive at their opposite surfaces. In some instances, the first semiconductor layer (16) is also compositionally graded, while in other instances, it is intrinsic in character. The semiconductor structures can function as solar cells; and modules which include a number of such cells represent another embodiment of the invention. Methods for making a photovoltaic device are also described..

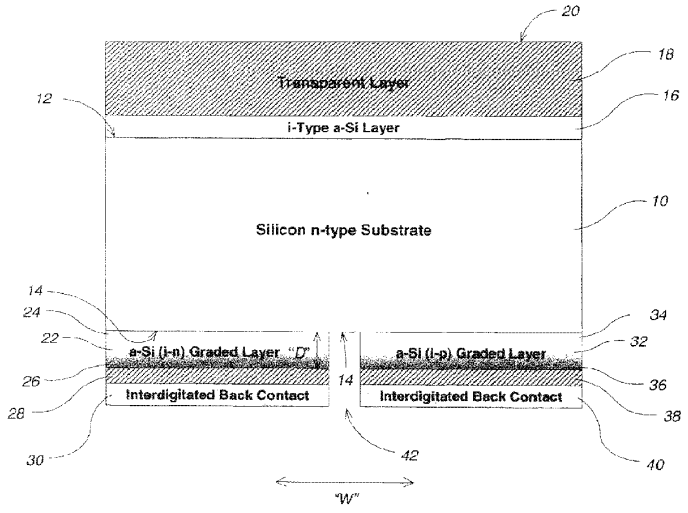


FIG. 1

EP 1 873 840 A1

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Description

BACKGROUND OF THE INVENTION

[0001] This invention relates generally to high efficiency solar cells. More specifically, the invention relates to solar cells based on semiconductor devices which include a heterojunction.

[0002] There is no doubt that solar energy offers the potential for providing virtually unlimited energy for use by man, if the solar energy can be made available in a useful form. Perhaps the greatest effort so far as been in using the sun's energy to obtain electricity, which can then be utilized through any existing electrical network - on the household, community, or industrial level. A primary approach to generating this electricity from solar radiation has involved direct generation by way of photovoltaic converters. These types of devices rely on the presence of a heterojunction, and are well-known in the art. (As used in this context, a heterojunction is a semiconductor junction which is composed of layers of dissimilar semiconductor material. These materials usually have non-equal band gaps. As one example, a heterojunction can be formed by contact between a layer or region of one conductivity type with a layer or region of opposite conductivity, e.g., a "p-n" junction). In addition to solar cells, other devices which utilize the heterojunction include thin film transistors and bipolar transistors.

[0003] In general, photovoltaic devices convert radiation, such as solar, incandescent, or fluorescent radiation, into electrical energy. Sunlight is the typical source of radiation for most devices. The conversion to electrical energy is achieved by the well-known photovoltaic effect. According to this phenomenon, radiation striking a photovoltaic device is absorbed by an active region of the device, generating pairs of electrons and holes, which are sometimes collectively referred to as photo-generated charge carriers.

[0004] The electrons and holes diffuse, and are collected by the electric field built into the device.

[0005] In view of the potential for solar cells to serve as such a reliable form of clean, renewable energy, great efforts have been made to increase their performance. One primary measurement for such performance is the photoelectric conversion efficiency of the device. Conversion efficiency is usually measured as the amount of electrical current generated by the device, as a proportion of the light energy which contacts its active surface. As documented in the literature, extremely small increases in photoelectric conversion efficiency, e.g., 1% or less, represent very significant advances in photovoltaic technology.

[0006] The performance of photovoltaic devices depends in large part on the composition and microstructure of each semiconductor layer. For example, defect sites which result from structural imperfections or impurity atoms may reside on the surface or within the bulk of monocrystalline semiconductor layers. Moreover, polycrystalline semiconductor materials may contain randomly-oriented grains, with grain boundaries which induce a large number of bulk and surface defect sites.

[0007] The presence of various defects of this type can be the source of deleterious effects in the photovoltaic device. For example, many of the charge carriers recombine at the defect sites near the heterojunction, instead of continuing on their intended pathway to one or more collection electrodes. Thus, they become lost as current carriers. Recombination of the charge carriers is one of the chief reasons for decreased photoelectric conversion efficiency.

[0008] The negative effects of surface defects can be minimized to some degree by passivation techniques. For example, a layer of intrinsic (i.e., undoped) amorphous semiconductor material can be formed on the surface of the substrate. The presence of this intrinsic layer decreases the recombination of charge carriers at the substrate surface, and thereby improves the performance of the photovoltaic device.

[0009] The use of this type of intrinsic layer is generally described in U.S. Patent 5,213,628 (Noguchi et al). Noguchi describes a photovoltaic device which includes a monocrystalline or polycrystalline semiconductor layer of a selected conductivity type. A substantially intrinsic layer of 250 Angstroms or less is formed over the substrate. A substantially amorphous layer is formed over the intrinsic layer, having a conductivity opposite that of the substrate, and completing a "semiconductor sandwich structure." The photovoltaic device is completed by the addition of a light-transparent electrode over the amorphous layer, and a back electrode attached to the underside of the substrate.

[0010] The photovoltaic devices described in the Noguchi patent appear to considerably minimize the problem of charge carrier recombination in some situations. For example, the presence of the intrinsic layer at selected thicknesses is said to increase the photoelectric conversion efficiency of the device. Moreover, the concept of passivating the surfaces of semiconductor substrates in this manner has been described in a number of references since the issuance of Noguchi et al. Examples include U.S. Patent 5,648,675 (Terada et al); and U.S. Patent Publications 2002/0069911 A1 (Nakamura et al): 2003/0168660 A1 (Terakawa et al); and 2005/0062041 A1 (Terakawa et al).

[0011] While the references mentioned above address the recombination problem to some degree, there are some considerable drawbacks remaining. For example, the presence of the intrinsic layer, while beneficial, results in the formation of yet another interface, i.e., between the intrinsic layer and the overlying amorphous layer. This new interface is yet another site for impurities and spurious contaminants to become trapped and to accumulate, and possibly cause additional recombination of the charge carriers. As an example, interruptions between the deposition steps during fabrication of a multilayer structure can provide unwelcome opportunities for

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the entry of the contaminants. Moreover, abrupt band bending at the interface, due to a change in conductivity, and/or variations in band gap, can lead to a high density of interface states, which is another possible source of recombination.

[0012] Furthermore, while the elimination of charge carrier recombination certainly increases photoelectric conversion efficiency, there are other factors which can still decrease the performance of conventional solar cells. As an example, solar cells in the past have often been produced with many of the electrical connections on the front-side of the cell, i.e., the surface receiving incident light. Thus, the front surface of the cell usually included front-side metal grid lines or current collection ribbons, along with associated devices and hardware, such as bus bars and tabs.

[0013] The presence of these features on the front-side of a solar cell can be disadvantageous for a number of reasons. For example, the grid lines and tabs detract from the uniformity and overall appearance of the solar cell. Aesthetic features for the solar cells often represent critical quality parameters, e.g., in residential home design. Moreover, the operational performance of the solar cell can be adversely affected by the presence of these front-side features, since they "shade" portions of the incident light which would otherwise be absorbed by the cell.

[0014] The various problems associated with front surface features in solar cells have been addressed with some success. For example silicon photovoltaic devices with all of the electrical connections on the back side of the cell have been developed. As described in U.S. Patent 5,053,083 (Sinton), the "back side"-type of cell can exhibit increased efficiency - primarily because of the lack of front-side features which block the desired light energy. Moreover, the absence of these features can facilitate other treatments and operations on the front-side of the cell, e.g., texturing applications, as described below.

[0015] Nevertheless, the drive to increase photoelectric efficiency continues to be relentless, since efficiency directly affects the economic viability of photovoltaic devices. Thus, improved photovoltaic devices would be very welcome in the art. The devices should minimize the problem of charge-carrier recombination at various interface regions between semiconductor layers. Moreover, the devices should exhibit electrical properties which ensure good photovoltaic performance, e.g., photoelectric conversion efficiency. Furthermore, the devices should be capable of being made efficiently and economically.

[0016] The fabrication of the devices should eliminate process steps which would allow the entry of excessive levels of impurities and other defects. Another important requirement for many of these devices is their visual features. Specifically, the solar cell structure should be aesthetically pleasing and stylish when used in certain applications, e.g., architectural designs for homes and other structures.

BRIEF DESCRIPTION OF THE INVENTION

[0017] One embodiment of this invention is directed to a semiconductor structure, comprising:

(a) a semiconductor substrate of one conductivity type, having a front surface and a back surface;

(b) a first amorphous semiconductor layer disposed on the front surface of the semiconductor substrate;

(c) a second amorphous semiconductor layer disposed on a portion of the back surface of the semiconductor substrate, wherein the second amorphous semiconductor layer is compositionally graded through its depth, from substantially intrinsic at the interface with the substrate, to substantially conductive at the opposite side, said second amorphous semiconductor layer having a selected conductivity type obtained by the incorporation of selected dopant atoms; and

(d) a third amorphous semiconductor layer disposed on another portion of the back surface of the semiconductor substrate, and spaced from the second amorphous semiconductor layer, wherein the third amorphous semiconductor layer is compositionally graded through its depth, from substantially intrinsic at the interface with the substrate, to substantially conductive at the opposite side, said third amorphous semiconductor layer having a conductivity type different from that of the second amorphous layer, and obtained by the incorporation of selected dopant atoms.

[0018] Another embodiment of the invention is directed to a solar module, comprising one or more solar cell devices, wherein at least one of the solar cell devices comprises the semiconductor structure described herein.

[0019] A method for making a photovoltaic device constitutes another embodiment of this invention. The method comprises the steps of:

(I) forming a first amorphous semiconductor layer over a front surface of a semiconductor substrate;

(II) forming a second amorphous semiconductor layer on a portion of a back surface of the semiconductor substrate, by continuously depositing semiconductor material and a dopant over the back surface portion, while altering the concentration of the dopant, so that the second amorphous semiconductor layer becomes compositionally-graded through its depth, from substantially intrinsic at the interface with the back surface of the substrate, to substantially conductive at the opposite side;

(III) forming a third amorphous semiconductor layer

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on another portion of the back surface of the semiconductor substrate, by continuously depositing semiconductor material and a dopant over the back surface portion, while altering the concentration of the dopant, so that the third amorphous semiconductor layer becomes compositionally-graded through its depth, from substantially intrinsic at the interface with the back surface of the substrate, to substantially conductive at the opposite side.

[0020] Various features, aspects, and advantages of this invention will become more apparent from the following detailed description, taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] FIG. 1 is a schematic cross-section which depicts the structure of a photovoltaic device according to one embodiment of the present invention.

[0022] FIG. 2 is a schematic cross-section which depicts the structure of a photovoltaic device according to another embodiment of the present invention.

[0023] FIG 3 is a schematic cross-section which depicts the structure of a photovoltaic device according to still another embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0024] The silicon substrate of this invention can be in a variety of forms. As depicted in FIG. 1, substrate 10 can be monocrystalline or polycrystalline. Furthermore, the substrate material can be n-type or p-type, depending in part on the electrical requirements for the photovoltaic device. Substrate 10 includes a front surface 12, and a back surface 14. The substrate usually has a thickness of about 50 microns to about 600 microns. (It should be understood that all of the figures provided herein are not necessarily drawn to scale, and are instead drawn for easier understanding of the text).

[0025] A variety of conventional treatment steps are usually carried out on the substrate, prior to deposition of the other semiconductor layers. For example, the substrate can be cleaned and placed in a vacuum chamber (e.g., a plasma reaction chamber, as described below). The chamber can then be heated to temperatures sufficient to remove any moisture on or within the substrate. Usually, a temperature in the range of about 120-240 °C is sufficient. Sometimes, hydrogen gas is then introduced into the chamber, and the substrate is exposed to a plasma discharge, for additional surface-cleaning. However, many variations on cleaning and pretreatment steps are possible. Usually, these steps are carried out in the chamber used for additional fabrication of the device.

[0026] The various semiconductor layers formed over the substrate are usually (though not always) applied by plasma deposition. Many different types of plasma deposition are possible. Non-limiting examples include chemical vapor deposition (CVD); vacuum plasma spray (VPS); low pressure plasma spray (LPPS), plasma-enhanced chemical-vapor deposition (PECVD), radio-frequency plasma-enhanced chemical-vapor deposition (RFPECVD); expanding thermal-plasma chemical-vapor deposition (ETPCVD); electron-cyclotron-resonance plasma-enhanced chemical-vapor deposition (ECRPECVD), inductively coupled plasma-enhanced chemical-vapor deposition (ICPECVD), and air plasma spray (APS). Sputtering techniques can also be used, e.g., reactive sputtering. Moreover, combinations of any of these techniques might also be employed. Those skilled in the art are familiar with the general operating details for all of these deposition techniques. In some preferred embodiments, the various semiconductor layers are formed by a PECVD process.

[0027] In one embodiment of this invention depicted in FIG. 1, an intrinsic amorphous silicon layer 16 is formed on the front surface 12 of substrate 10. As mentioned previously, intrinsic layer 16 is un-doped (i.e., having a dopant concentration of substantially zero). The layer can be formed in a number of ways. As a non-limiting example, silicon substrate 10 could be placed in a plasma reaction chamber (e.g., CVD or PECVD). After evacuating the chamber, the substrate could be heated to an appropriate temperature, e.g., about 120°C to about 240°C. A silicon-containing gas, such as silane, is pumped into the chamber as a plasma is generated, e.g., by glow discharge. The plasma causes decomposition of the gaseous precursor, resulting in formation of the amorphous layer of silicon.

[0028] The thickness of intrinsic layer 16 will depend on various factors, including the optical and electrical characteristics of the layer. The thickness of the layer is influenced most heavily by the extent to which the recombination of charge carriers at the substrate interface has to minimized. Usually, the thickness of layer 16 is less than or equal to about 250 Angstroms. In some specific embodiments, layer 16 has a thickness in the range of about 30 Angstroms to about 180 Angstroms. The most appropriate thickness in a given situation can be determined without undue effort, e.g., by taking measurements related to the photoelectric conversion efficiency of photovoltaic devices which incorporate the semiconductor.

[0029] According to this embodiment, a transparent film or layer 18 is disposed on intrinsic amorphous silicon layer 16, on the light-receiving side of the photovoltaic device.

[0030] Film 18 provides anti-reflective (AR) characteristics for the device. The transparent film can comprise a variety of materials, such as metal oxides. Non-limiting examples include silicon nitride (SiN), zinc oxide (ZnO), doped ZnO, and indium tin oxide (ITO). Film 18 can be formed by various conventional techniques, such as sputtering or evaporation. Its thickness will depend on various factors, including desired AR characteristics. Usually, transparent film 18 (which has a top surface 20)

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will have a thickness in the range of about 200 Angstroms to about 1000 Angstroms.

[0031] A second amorphous semiconductor layer 22 is disposed on a portion of the back surface 14 of substrate 10. While substrate 10 is the primary power generating layer of the photovoltaic device, semiconductor layer 22 constitutes a component of one of the electrodes of the device. As those skilled in the art understand, the electrodes are typically designed to carry the power (electrical current) through the device and out to an external circuit. Semiconductor layer 22 can be either n-type or p-type, depending upon the electrical configuration of the photovoltaic device.

[0032] According to a primary embodiment of the present invention, second amorphous layer 22 is compositionally graded, in terms of dopant concentration. In general, the dopant concentration is substantially zero at the interface with the substrate, i.e., region 24 in FIG. 1. On the opposite side of layer 22, i.e., region 26, the dopant concentration is at a maximum, in terms of semiconductor conductivity objectives. The concept of compositional grading for these types of layers is also generally described in a pending application assigned to the assignee of the present invention: U.S. Patent Application S.N. 11/263,159, filed on October 31, 2005, for J. Johnson and V. Manivannan. The contents of that patent application are incorporated herein by reference.

[0033] The term "compositionally-graded" is meant to describe a change (i.e., a "gradation") in dopant concentration as a function of the depth ("D") of semiconductor layer 22. In some embodiments, the gradation is substantially continuous, but this does not always have to be the case. For example, the rate-of-change in concentration may itself vary through the depth, increasing slightly in some regions, and decreasing slightly in others. (However, the overall gradation is always characterized as a decrease in dopant concentration in the direction toward substrate 10). Moreover, in some instances, the dopant concentration may remain constant for some portion of the depth, although that portion would probably be very small. Any and all of these variations in gradations are meant to be encompassed by the term "graded". The specific dopant concentration profile for a given semiconductor layer will depend on various factors, e.g., the type of dopant and the electrical requirements for the semiconductor device; as well as its microstructure and thickness.

[0034] As mentioned above, the dopant concentration for layer 22 is substantially zero at the interface with the substrate, regardless of the particular dopant profile. Thus, an intrinsic region 24 functions to prevent recombination of the charge-carriers at the interface with substrate surface 14. At the opposite, lower surface of amorphous layer 22, region 26 is substantially conductive. The specific dopant concentration in that region will depend on the particular requirements for the semiconductor device. As a non-limiting example in the case of a polycrystalline or single crystalline silicon substrate, region 26 will often have a concentration of dopant in the range of about 1×10^{16} cm^{-3} to about 1×10^{21} cm^{-3}.

[0035] The thickness of graded amorphous layer 22 will also depend on various factors, such as the type of dopant employed; the conductivity-type of the substrate; the grading profile; and the dopant concentration in region 26. As in the case of layer 16, the thickness of layer 22 is usually less than or equal to about 250 Angstroms. In some specific embodiments, graded layer 22 has a thickness in the range of about 30 Angstroms to about 180 Angstroms. As described previously for layer 16, the most appropriate thickness in a given situation can readily be determined by taking measurements related to the photoelectric conversion efficiency of the device. Measurement of other properties (such as open circuit voltage (V_{oc}), short circuit current (I_{sc}), and fill factor (FF)) can also be helpful in determining the most appropriate thickness for layer 22.

[0036] In some preferred embodiments (though not all), an electrode layer 28 is formed on the backside of amorphous semiconductor layer 22 (FIG. 1). Usually, electrode layer 28 functions as a diffusion barrier layer, preventing metal atoms from diffusing from a conductive layer (described below) into semiconductor layer 22. Electrode layer 28 is typically formed from a conductive material such as indium tin oxide, ZnO, doped ZnO, and the like. It can be formed from any of the typical deposition techniques used to deposit conductive layers. Layer 28 usually has a thickness in the range of about 50 Angstroms to about 500 Angstroms, although this range may vary considerably.

[0037] With continued reference to FIG. 1, a metal contact 30 is disposed over amorphous semiconductor layer 22. Metal contact 30 would be applied directly on layer 22, in the absence of intervening electrode layer 28. When layer 28 is present, metal layer 30 would be applied thereover. Metal contact 30 functions as a conducting electrode, conveying the electric current generated by the photovoltaic device to a desired location. The metal contact can be formed of a variety of conductive materials, such as silver (Ag), aluminum (Al), copper (Cu), molybdenum (Mo), tungsten (W), titanium (Ti), palladium (Pd), and various combinations thereof. Although metal contact 30 is illustrated as a layer of material in FIG. 1, its shape and size can vary considerably, as further described below. The metal contact can be formed by various techniques, e.g., plasma deposition, screen printing; vacuum evaporation (sometimes using a mask); pneumatic dispensing; or direct-write techniques such as ink jet printing.

[0038] A third amorphous semiconductor layer 32 is disposed on another portion of the back surface 14 of substrate 10. As in the case of layer 22, semiconductor layer 32 constitutes another component of one of the electrodes of the photovoltaic device. Layer 32 can be of the n-type or p-type. However, in most of the semiconductor configurations of this type, layer 32 has a conductivity (n or p) different from that of semiconductor layer

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22. (In FIG. 1, layer 22 is arbitrarily depicted as n-type, while layer 32 is depicted as p-type).

[0039] As in the case of amorphous semiconductor layer 22, layer 32 is compositionally graded, in terms of dopant concentration. Thus, the dopant concentration is substantially zero at the interface with the substrate, i.e., region 34 in FIG. 1. This intrinsic region prevents recombination of the charge-carriers, as described previously. On the opposite side of layer 32, i.e., region 36, the dopant concentration is at a maximum, in terms of semiconductor conductivity objectives. As in the case of layers 22 and 16, the thickness of layer 32 is usually less than or equal to about 250 Angstroms. In some specific embodiments, the layer has a thickness in the range of about 30 Angstroms to about 180 Angstroms.

[0040] As in the case of region 26, region 36 will usually have a concentration of dopant in the range of about 1 x 10^{16} cm^{-3} to about 1 x 10^{21} cm^{-3}. However, the specific concentration need not be identical to that of region 26, and will depend in part on the overall configuration of the device. Moreover, the overall gradation pattern for semiconductor layer 32 may be similar or substantially identical to that of semiconductor layer 22. However, in some embodiments, the gradation profiles can differ from each other - again depending on factors such as layer composition and thickness, dopant-type, semiconductor requirements, and the like. Moreover, it should be emphasized that the exact depth of "regions" 24, 26, 34, and 36 can vary, depending on factors discussed herein, such as semiconductor layer thickness and dopant profile. The same is true for the analogous regions depicted in the other figures.

[0041] In FIG. 1, the individual widths of semiconductor layers 22 and 32 are depicted as being equal to each other. (In the figure, the width dimension is designated with an arrow and the letter "W"). However, it is not necessary that the widths be equal. In some preferred embodiments, the width of the i-p-graded amorphous layer (here, An optional electrode layer 38 can be applied over the backside of amorphous semiconductor layer 32. Layer 38 performs in a manner similar to layer 28, e.g., functioning as a diffusion barrier layer between the underlying amorphous semiconductor layer and the metal contact described below. Electrode layer 38 is also typically formed from a conductive material. It can have the same thickness as layer 28, but in some embodiments, the thickness can differ as well.

[0042] A metal contact 40 is disposed over amorphous semiconductor layer 32, as depicted in FIG. 1. As in the case of metal contact 30, contact 40 would be applied directly on layer 32, or on top of optional layer 38. Metal contact 40 functions as another conducting electrode, conveying the electric current generated by the photovoltaic device to a desired location. The metal contact can be formed from the conductive materials described above, and is usually made from the same material as contact 30. Moreover, the size and shape of contact 40 can vary significantly, as can the manner in which it is formed. In other words, these parameters and details do not have to be the same as for contact 30, as they depend in large part on the overall construction of the photoelectric device.

[0043] As also shown in FIG. 1, second amorphous semiconductor layer 22 is spaced from third amorphous semiconductor layer 32 by an isolation trench 42. Typically, the primary function of trench 42 is to electrically and structurally isolate the two semiconductor layers, and/or to isolate contact layer 30 from contact layer 40. The precise shape of the trench can also vary. The trench can be formed by a number of conventional techniques - either during or after the fabrication of the various semiconductor and metal layers. As an example, the trench could be formed by drilling processes such as laser drilling, or by mechanical scribing techniques. In some instances, the trench is filled or partially filled with an electrically-insulating material, e.g., a polymeric resin (not shown here). The insulating material may serve to protect the underside of substrate 10 during various fabrication steps used to form the device, such as etching, milling, or scribing steps.

[0044] Contact layers 30 and 40 constitute a portion of an electrical system for interconnecting the various semiconductor elements. Any conventional electrical design may be used for such a system. As emphasized herein, preferred embodiments call for all of the electrical contacts to be incorporated into locations which ensure that the front surface of the device, i.e., top surface 20, is substantially free of any features which would obstruct incoming light. Typically, then, the various electrical interconnections are located in the general vicinity of substrate back surface 14, forming an "all-back-contact" configuration.

[0045] As one illustration, the contacts may be interdigitated. For example (and when viewed from a planar perspective for the device), the contacts may be arranged in a comb-shape, as described in U.S. Publication 2005/0062041 A1, which is incorporated herein by reference. Interdigitated arrangements are also described in various other references, e.g., U.S. Patent 5,053,083 (Sinton); 4,200,472 (Chappell et al); and Publication 2004/0200520 A1 (Mulligan et al), which are also incorporated herein by reference. Those skilled in the art will be able to readily determine the most appropriate metallization and electrical scheme for a particular device, without undue effort.

[0046] The compositional-grading of semiconductor layers 22 and 32 can be carried out by various techniques. The deposition of each layer is typically undertaken in separate steps. Usually, grading is accomplished by adjusting the dopant levels during plasma deposition. In a typical embodiment, a silicon precursor gas such as silane (SiH_4) is introduced into the vacuum chamber in which the substrate is situated. A diluting gas such as hydrogen may also be introduced with the silicon precursor gas. Flow rates for the precursor gas can vary considerably, but are typically in the range of about 10

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sccm to about 300 sccm. During the initial stages of deposition, no dopant precursors are present. Therefore, regions 24 and 34 are substantially intrinsic ("undoped"), as mentioned above, thus serving to passivate the surface of substrate 10.

[0047] As the deposition process continues for each of layers 22 and 32, a dopant precursor is added to the plasma mixture. Choice of a precursor will of course depend on the selected dopant, e.g., n-type dopants such as phosphorus (P), arsenic (As), and antimony (Sb); or p-type dopants such as boron (B). Several non-limiting examples of dopant compounds can be provided: diborane gas (B_2H_6) for the p-type dopant, or phosphine (PH_3) for the n-type dopant. The dopant gases may be in pure form, or they may be diluted with a carrier gas, such as argon, hydrogen, or helium.

[0048] During the formation of each layer 22 and 32, the addition of the dopant gas is carefully controlled, to provide the desired doping profile. Those skilled in the art are familiar with gas metering equipment, e.g., mass flow controllers, which can be used to carry out this task. The feed rate for the dopant gas will be selected to substantially match the gradation scheme described above. Thus, in very general terms, the feed rate of the dopant gas will gradually increase during the deposition process. However, many specific changes in feed rate can be programmed into the deposition scheme. Maximum flow rates at the conclusion of this step of the process result in the formation of substantially-conductive regions 26 and 36, as mentioned previously. Each of regions 26 and 36 forms a heterojunction with the substrate.

[0049] In the embodiment of FIG. 1, an intrinsic amorphous silicon layer was formed on the front surface of the substrate. However, in other embodiments, a compositionally-graded amorphous semiconductor layer is formed in place of the intrinsic layer. One illustration of this alternative embodiment is depicted in FIG. 2. (In this figure, many of the elements similar or identical to those of FIG. 1 are not labeled, or are provided with the same element numerals). Thus, as shown in FIG. 2, a first amorphous semiconductor layer 50 is disposed on the front surface 12 of substrate 10. The first amorphous semiconductor layer is compositionally graded through its depth. Thus, the layer is substantially intrinsic at the interface with the substrate (i.e., region 52), and substantially conductive at the opposite side (region 54).

[0050] Layer 50 can be compositionally graded according to the same techniques described previously, for the graded layers of FIG. 1. Moreover, the graded profile for layer 50 may be similar to that of the other graded layers, though it can have a different profile as well. Usually, the conductive region of the layer (i.e., region 54) will have a concentration of dopant atoms in the general range described previously, i.e., about 1×10^{16} cm^{-3} to about $1x10^{21}$ cm^{-3}. The type of dopant used for graded layer 50 will depend in part on the conductivity-type of the substrate. Typically, the layer forms a heterojunction with the substrate.

[0051] As in the case of the other doped regions, the specific dopant concentration profile for layer 50 will depend on various factors, e.g., the type of dopant and the electrical requirements for the semiconductor device; as well as its microstructure and thickness. The presence of compositionally graded layer 50 can be very advantageous as an additional site for preventing recombination of charge carriers. In this manner, the intended path of the charge carriers toward the collection electrodes of the device is enhanced, thereby resulting in greater photoelectric conversion. Layer 50 can be referred to as a front surface field (FSF).

[0052] As in the embodiment of FIG. 1, a transparent film or layer 56 is disposed on top of amorphous semiconductor layer 50 in FIG. 2, providing anti-reflective characteristics for the device. Moreover, the device also includes second and third amorphous semiconductor layers 22, 32, formed on the back surface 14 of the substrate. In preferred embodiments, each of these layers is compositionally graded, as described previously.

[0053] With continued reference to FIG. 2, metal contact layers 30 and 40 are formed over layers 22 and 32, respectively. In this particular illustration, there are no electrode layers between the metal contact layers and underlying amorphous layers 22 and 32 (i.e., analogous to layers 28 and 38 in FIG. 1). However, it should be understood that the electrode layers could also be utilized in this embodiment as well, e.g., to perform as a diffusion barrier.

[0054] In some preferred embodiments of the present invention, at least one of the planar surfaces of the semiconductor device is textured. Texturing of the various surfaces of the device can reduce undesirable light reflection. Moreover, texturing can utilize incoming light much more effectively, by elongating an optical path length in one of the semiconductor layers ("optical light trapping"). Usually, at least the front-side (i.e., the surface closest to incident light) is textured.

[0055] Texturing can be carried out by a variety of techniques. One instructive source of information is an article by David King et al, "Experimental Optimization of an Anisotropic Etching Process for Random Texturization of Silicon Solar Cells", IEEE Conference Proceedings (1991), pages 303-308. This article is incorporated herein by reference. Very often, texturing can be carried out by etching techniques, using mild alkaline solutions with low concentrations (e.g., less than about 5% by volume) of basic compounds like potassium hydroxide or sodium hydroxide. The alkaline solutions can contain other components as well, e.g., hydroxy compounds such as isopropyl alcohol. Many other types of alkaline solutions may also be employed.

[0056] Fig 3 is a non-limiting illustration of a semiconductor device for some of these preferred embodiments. (In this figure, many of the elements similar or identical to those of FIG. 1 are not labeled, or are provided with the same element numerals). In some preferred embodiments, the front surface 12 of the substrate is textured,

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as shown in FIG. 3. Moreover, back surface 14 can be textured.

[0057] The type of texturing can vary considerably, depending on a number of factors discussed previously. As one example, textured features can be in the form of microscopic pyramids 60, as shown in FIG. 3. It should be emphasized that FIG. 3 happens to show all planar surfaces as being textured, although there is no requirement or preference for that to be the case. As those skilled in the art understand, the textured profile for many of the surfaces can effectively result from the profile of the underlying surfaces. For example, if substrate surfaces 12 and 14 are textured, layers deposited over those surfaces (and layers thereafter) will often adapt the conformal features of the substrate surfaces. For example, this is shown in FIG. 3 for semiconductor layers 16, 22, 32; transparent layer 18; and metallic contact layers 30, 40. (The optional electrode layers, e.g., layers 28 and 38 in FIG. 1, can also be textured, when present).

[0058] Various other details regarding the texturing of semiconductor layers for photovoltaic devices are known in the art. As one example, U.S. Patent 6,670,542 (Sakata et al) describes steps in forming textured surfaces for single crystalline layers used in photovoltaic conversion devices. The Sakata et al patent is also incorporated herein by reference. Moreover, Sakata et al describes procedures which are helpful in ensuring that i-type amorphous layers (like those described herein) are formed on textured surfaces with the desired degree of layer-uniformity.

[0059] The discussion above relates to semiconductor structures which are often used as solar cell devices. One or more of these devices can be incorporated into the form of a solar module. For example, a number of the solar cells can be electrically connected to each other, in series or in parallel, to form the module. (Those of ordinary skill in the art are familiar with details regarding the electrical connections, etc). Such a module is capable of much greater energy output than the individual solar cell devices.

[0060] Non-limiting examples of solar modules are described in various references, e.g., U.S. Patent 6,667,434 (Morizane et al), which is incorporated herein by reference. The modules can be formed by various techniques. For example, a number of solar cell devices can be sandwiched between glass layers, or between a glass layer and a transparent resin sheet, e.g., those made from EVA (ethylene vinyl acetate). Thus, according to some embodiments of this invention, solar modules contain at least one solar cell device which itself comprises a compositionally-graded amorphous layer adjacent a semiconductor substrate, as described previously. The use of the graded layers can improve device properties like photoelectric conversion efficiency, etc., and thereby improve the overall performance of the solar module.

[0061] The Morizane et al reference also describes various other features for some of the solar modules. For example, the patent describes "two-side incidence"-type solar modules in which light can contact both front and rear surfaces of the module. Moreover, the patent describes solar modules which must be extremely moistureproof (e.g., those used outdoors). In these types of modules, sealing resins can be used to seal the side of each solar cell element. Furthermore, the modules may include various resinous layers which prevent the undesirable diffusion of sodium from nearby glass layers. All of these types of solar modules may incorporate devices which comprise the compositionally-graded amorphous layer (or layers) described herein.

[0062] Those skilled in the art are generally familiar with many other details regarding the primary components of the solar modules, e.g., the various substrate materials, backing materials, and module frames. Other details and considerations are also well-known, e.g., wire connections in and out of the module (for example, those leading to an electrical inverter); as well as various module encapsulation techniques.

EXAMPLES

[0063] A general example is provided below. It should be viewed as merely illustrative, and should not be construed to be any sort of limitation on the scope of the claimed invention.

[0064] The fabrication of photovoltaic devices according to some embodiments of the present invention can be undertaken as follows: Monocrystalline or polycrystalline semiconductor substrates (or silicon wafers) of one conductivity type can first be etched by conventional techniques. For example, a texturing solution containing selected proportions of ultra-pure deionized water, potassium hydroxide (KOH, 45% concentration), and isopropyl alcohol can first be prepared in a quartz vessel. The temperature of the texturing solution is usually maintained at about 65°C - 80°C. The substrate can then be immersed in the agitated solution for a period of time determined to be suitable to achieve the desired degree of etching (typically about 5-60 minutes). Following the texturing step, the substrate is removed and rinsed with deionized water.

[0065] In some instances, the substrate is subjected to various pre-treatment steps, prior to texturing. For example, the substrate (e.g., a wafer) can be immersed in a buffer-oxide-etch (BOE) solution for 60 seconds, followed by a surface damage-removal etch. The latter step can be carried out in a 1 : 1 solution of KOH : H_2O solution for 30 minutes at 85°C, and can result in the desired thinning of the substrate by about 30 microns. The wafer can then be stored in isopropyl alcohol for at least 10 minutes, to prevent surface oxidation.

[0066] With reference to the exemplary embodiment of FIG. 3, the substrate 10 can then be placed in a plasma reaction chamber (for example: a plasma enhanced chemical vapor deposition system), in preparation for the formation of the features on the front side of the device. A vacuum pump is used to remove atmospheric gases

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from the chamber, and the substrate is then pre-heated to about 120 to about 240°C. An optional hydrogen plasma surface preparation step is performed on the front surface of the substrate. Hydrogen (H_2) is introduced into the chamber at a flow rate of about 50 to about 500 seem (standard cubic centimeters per minute). A throttle valve is used to maintain a constant processing pressure in the range of about 200 mTorr to about 800 mTorr. Alternating frequency input power with a power density in the range of about 6 mW/cm^2 to about 50 mW/cm^2 range is used to ignite and maintain the plasma. Applied input power can be from about 100 kHz to about 2.45 GHz. Hydrogen plasma surface preparation time is about 1 to about 60 seconds.

[0067] At the end of the hydrogen plasma preparation step (if such a step is employed), silane (SiH_4) is introduced into the process chamber at a flow rate of about 10 seem to about 300 seem. This will initiate the deposition of the intrinsic amorphous silicon layer 16. (In this embodiment, there are no dopant precursors included in the plasma, so that the composition of the amorphous layer is intrinsic (undoped), thus serving to passivate the surface of the semiconductor substrate). Deposition continues until the intrinsic layer achieves the desired, average thickness. As described above, the layer usually conforms to the surface profile of the underlying substrate, and would thus also have a textured surface.

[0068] After formation of intrinsic layer 16, transparent anti-reflective layer or coating 18 can be formed within a suitable process chamber. As mentioned previously, a number of techniques can be used to form such a layer, such as sputtering, CVD, evaporation, and the like. Deposition continues until layer 18 has a desired thickness. As in the case of layer 16, layer 18 will usually conform closely to the underlying surface, thus resulting in a textured uppermost surface 20.

[0069] Substrate 10 can then be repositioned in the vacuum chamber, in preparation for the formation of all of the backside features. There are a number of details regarding formation of each of the backside amorphous layers, as well as the overlying metal contacts, and intervening, optional electrode layers. There is no need to elaborate on the many steps involved in the formation of these layers, since they are very conventional to the semiconductor industry. As those skilled in the art understand, the formation of the various layers on the backside involves a serious of deposition and photolithographic steps, e.g., masking, curing (exposure), photoresist lift-off, etching, and the like.

[0070] A brief review will be undertaken in regard to formation of graded layers 22 and 32. (The steps in their formation can be substantially equivalent, although different dopant atoms are used to provide the different conductivity types). As described for the front side of the device, a hydrogen plasma preparation step may first be undertaken on the backside, in which silane is introduced into the process chamber at a flow rate of about 10 seem to about 300 seem. This will result in the formation of intrinsic amorphous regions 24 and 34 (depending on which layer is being formed first). In each instance, the absence of dopant precursors functions to passivate the back surface 14 of the substrate.

[0071] As the deposition process for each of layers 22 and 32 progresses, the desired dopant precursor is subsequently added to the plasma mixture. Examples of dopant precursors are: B_2H_6, $B(CH_3)_3$, and PH_3. These may be in pure form or diluted with a carrier gas such as argon, hydrogen or helium. The flow rate of the precursor is increased over the course of the compositionally-graded layer deposition. This forms a gradient in the doping concentration through the single layer. At the conclusion of the graded layer deposition process, concentrations of dopant precursor in the plasma are such that substantially doped amorphous semiconductor properties are achieved, i.e., in regions 26 and 36.

[0072] Electrode layers 28 and 38 (if present) can then be formed over the respective, graded layers, according to one or more of the techniques described previously, such as sputtering. Contacts 30 and 40 can also be formed in the conventional manner, e.g., by screen-printing. isolation trench 42 can also be formed in known fashion, e.g., by laser-drilling or mechanical scribing. Those skilled in the art will be familiar with other conventional fabrication steps for the device as well. Moreover, the patents and other references set forth above provide further details regarding the manufacture of modules which contain multiple devices of this type.

[0073] Although the present invention has been described and illustrated in detail, it should be clearly understood that the description discloses examples of different embodiments of the invention, and is not intended to be limited to the examples or illustrations provided. Accordingly, various modifications, adaptations, and alternatives may occur to one skilled in the art without departing from the scope of the claimed inventive concept. All of the patents, patent applications, articles, and texts which are mentioned above are incorporated herein by reference.

Claims

1. A semiconductor structure, comprising:

   (a) a semiconductor substrate (10) of one conductivity type, having a front surface (12) and a back surface (14);

   (b) a first amorphous semiconductor layer (16) disposed on the front surface (12) of the semiconductor substrate (10);

   (c) a second amorphous semiconductor layer (22) disposed on a portion of the back surface (14) of the semiconductor substrate (10), wherein the second amorphous semiconductor layer (22) is compositionally graded through its depth, from substantially intrinsic at the interface with

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the substrate (10), to substantially conductive at the opposite side, said second amorphous semiconductor layer (22) having a selected conductivity type obtained by the incorporation of selected dopant atoms; and
(d) a third amorphous semiconductor layer (32) disposed on another portion of the back surface (14) of the semiconductor substrate (10), and spaced from the second amorphous semiconductor layer (22), wherein the third amorphous semiconductor layer (32) is compositionally graded through its depth, from substantially intrinsic at the interface with the substrate (10), to substantially conductive at the opposite side, said third amorphous semiconductor layer(32) having a conductivity type different from that of the second amorphous layer (22), and obtained by the incorporation of selected dopant atoms.

2. The semiconductor structure of claim 1, wherein for both the second amorphous semiconductor layer (22) and the third amorphous semiconductor layer (32), the concentration of dopant atoms at the interface with the substrate (10) is substantially zero; and the concentration of dopant atoms at the opposite side is in the range of about 1×10^{16} cm to about 1×10^{21} cm^{-3}.

3. The semiconductor structure of claim 1 or claim 2, wherein at least one electrical contact (30) is disposed over the second amorphous semiconductor layer (22), and at least one electrical contact (40) is disposed over the third amorphous semiconductor layer (32).

4. The semiconductor structure of claim 3, wherein an electrode layer (28) is disposed between the second amorphous semiconductor layer (22) and its overlying electrical contact (30); and an electrode layer (38) is disposed between the third amorphous semiconductor layer (32) and its overlying electrical contact (40).

5. The semiconductor structure of any preceding claim, wherein the second amorphous semiconductor layer (22) is spaced from the third amorphous semiconductor layer (32) by an isolation trench (42).

6. The semiconductor structure of any preceding claim, wherein a transparent layer (18) is disposed on the first amorphous semiconductor layer (16).

7. The semiconductor structure of claim 6, wherein the transparent layer (18) comprises an anti-reflective structure.

8. The semiconductor structure of claim 6, wherein the transparent layer (18) is formed of a material comprising silicon nitride.

9. The semiconductor structure of any preceding claim, wherein the substrate (10) is monocrystalline or polycrystalline; and is n-type or p-type.

10. The semiconductor structure of any preceding claim, wherein the first amorphous semiconductor layer (16) is intrinsic.

11. The semiconductor structure of any one of claims 1 to 9, wherein the first amorphous semiconductor layer (16) is compositionally graded through its depth, from substantially intrinsic at the interface with the substrate (10), to substantially conductive at the opposite side.

12. The semiconductor structure of any preceding claim, wherein the front surface (12) of the substrate (10) is textured.

13. The semiconductor structure of claim 3, wherein at least one electrical contact (30) disposed on the second amorphous semiconductor layer (22) is interdigitated with at least one electrical contact (40) disposed on the third amorphous semiconductor layer (32).

14. A solar cell, comprising a semiconductor structure having an all-back-contact configuration, wherein at least one amorphous semiconductor layer of the structure comprises a compositionally-graded dopant atom profile.

15. A method for making a photovoltaic device, comprising the steps of:

(I) forming a first amorphous semiconductor layer (16) over a front surface (12) of a semiconductor substrate (10);
(II) forming a second amorphous semiconductor layer (22) on a portion of a back surface (14) of the semiconductor substrate (10), by depositing semiconductor material and a dopant over the back surface portion, while altering the concentration of the dopant, so that the second amorphous semiconductor layer (22) becomes compositionally-graded through its depth, from substantially intrinsic at the interface with the back surface (14) of the substrate, to substantially conductive at the opposite side; and
(III) forming a third amorphous semiconductor layer (32) on another portion of the back surface (14) of the semiconductor substrate (10), by depositing semiconductor material and a dopant over the back surface portion, while altering the concentration of the dopant, so that the third amorphous semiconductor layer (32) becomes

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compositionally-graded through its depth, from substantially intrinsic at the interface with the back surface (14) of the substrate (10), to substantially conductive at the opposite side.

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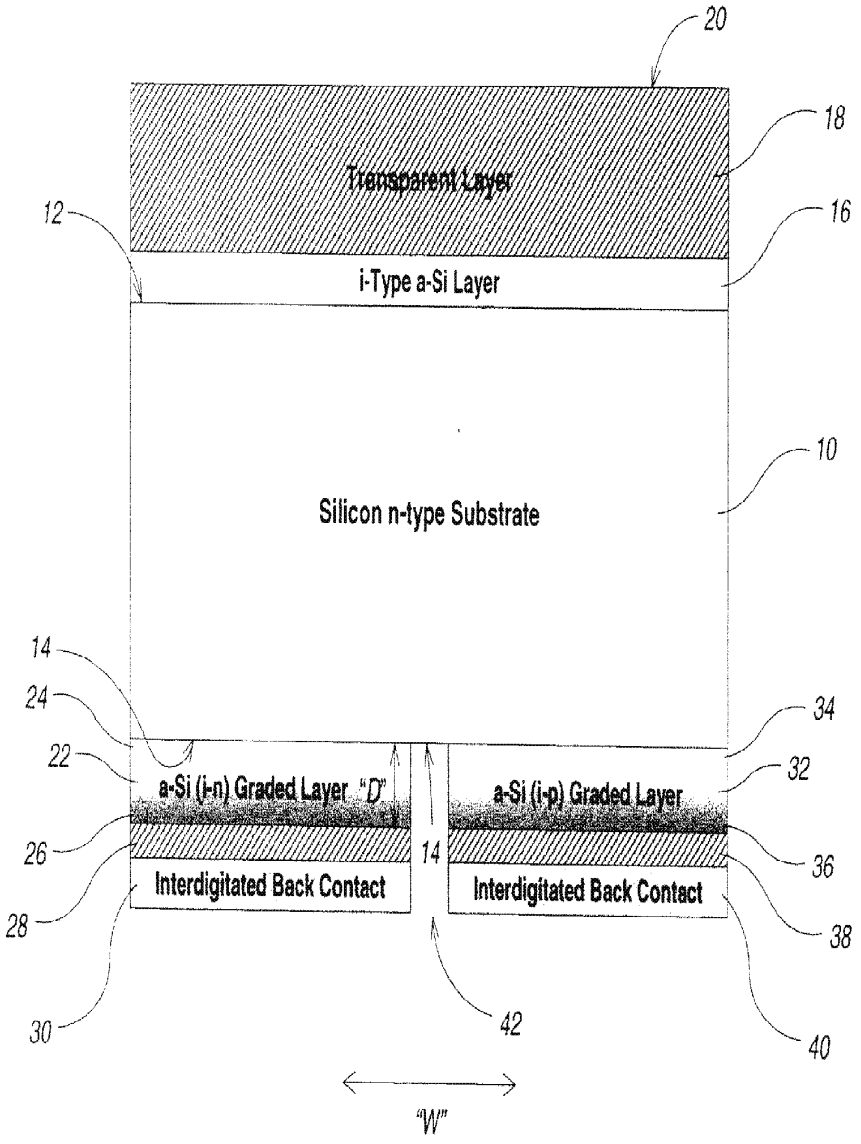

20
18
Transparent Layer
12
16
i-Type a-Si Layer
10
Silicon n-type Substrate
14
24
22
a-Si (i-n) Graded Layer "D"
34
32
a-Si (i-p) Graded Layer
26
14
36
Interdigitated Back Contact
Interdigitated Back Contact
28
38
30
42
40
"W"

FIG. 1

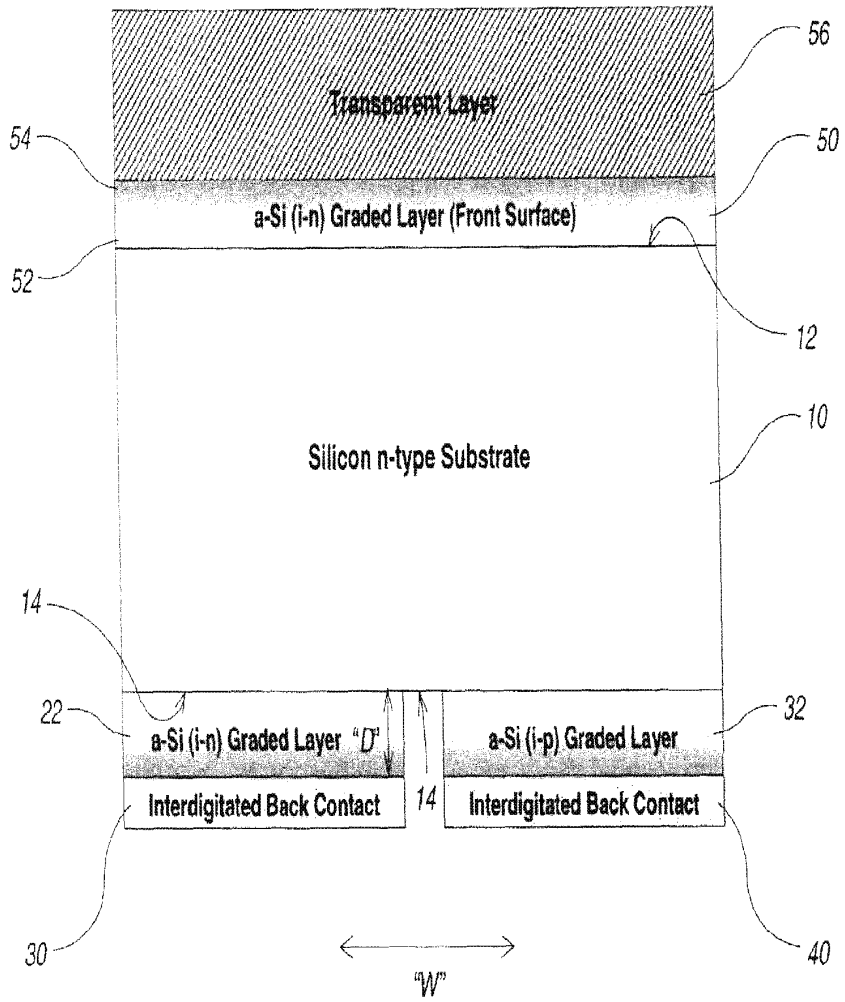


FIG. 2

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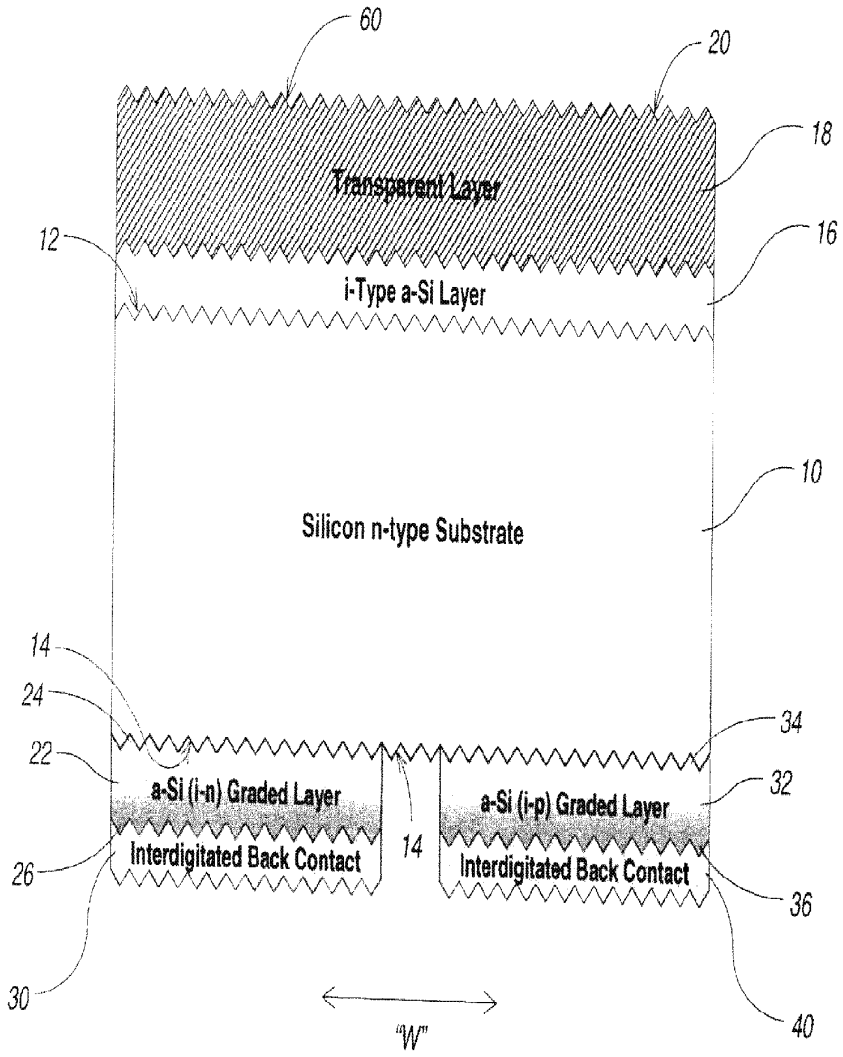

60
20
18
Transparent Layer
12
16
i-Type a-Si Layer
10
Silicon n-type Substrate
14
24
22
34
a-Si (i-n) Graded Layer
a-Si (i-p) Graded Layer
32
14
26
Interdigitated Back Contact
Interdigitated Back Contact
36
30
"W"
40

FIG. 3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 07 11 0609

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	9 October 2007	Heising, Stephan

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X : particularly relevant if taken alone
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A : technological background
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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 07 11 0609

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
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CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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D : document cited in the application
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AL BA MK RS

(30) Priority: **18.12.2007 JP 2007326175**

(71) Applicant: **Sony Corporation**
Tokyo 108-0075 (JP)

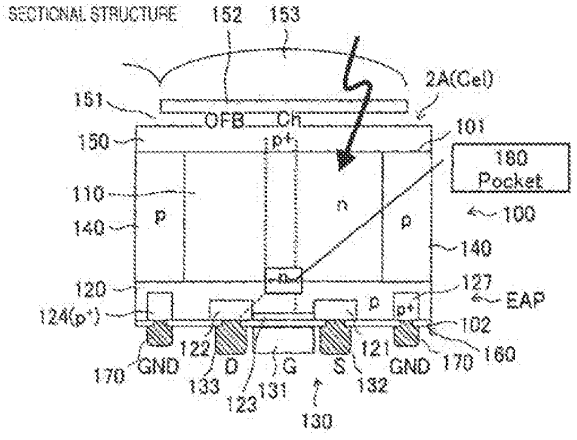
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(54) Solid-state imaging device and camera

(57) A solid-state imaging device includes pixel cells that are formed on a substrate having a first substrate surface side, on which light is irradiated, and a second substrate surface side, on which elements are formed, and separated by an adjacent cell group and an element separation layer for each of the pixel cells or with plural pixel cells as a unit. Each of the pixel cells has a first conductive well formed on the first substrate surface side and a second conductive well formed on the second substrate surface side. The first conductive well receives light from the first substrate surface side and has a photoelectric conversion function and a charge accumulation function for the received light. A transistor that detects accumulated charges in the first conductive well and has a threshold modulation function is formed in the second conductive well.

FIG. 2B



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Description

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] The present invention contains subject matter related to Japanese Patent Application JP 2007-326175 filed in the Japanese Patent Office on December 18, 2007, the entire contents of which being incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates to a solid-state imaging device and a camera having a photoelectric conversion element.

2. Description of the Related Art

[0003] It is known that, in solid-state imaging devices such as a CCD image sensor and a CMOS image sensor, a crystal defect in a photodiode as a photoelectric conversion element of a light sensing section and a deep level defect in an interface between the light sensing section and an insulating film thereon cause dark current.

[0004] As a method of suppressing the occurrence of the dark currents due to the interface state density, an embedded photodiode structure is effective. The embedded photodiode is configured by, for example, forming an n-type semiconductor region and forming a shallow p-type semiconductor region (a hole accumulation region) with high impurity density for the suppression of the dark currents near the surface of the n-type semiconductor region, i.e., an interface between the n-type semiconductor region and an insulating film.

[0005] As a method of manufacturing the embedded photodiode, it is a general practice to ion-implant B or BF_2 serving as p-type impurities and annealing the same and form a p-type semiconductor region near the interface between the n-type semiconductor region forming the photodiode and the insulating film.

[0006] In the CMOS image sensor, each of pixels includes a photodiode and various kinds of transistors such as readout, reset, and amplification transistors. A signal photoelectrically converted by the photodiode is processed by these transistors. A wiring layer including multilayer metal wiring is formed above each of the pixels. A color filter that specifies the wavelength of light made incident on the photodiode and an on-chip lens that condenses light on the photodiode are formed on the wiring layer.

[0007] As such a CMOS image sensor, device structures having various characteristics are proposed.

[0008] Specifically, there is proposed various devices such as a charge modulation device (CMD, see Japanese Patent No. 1938092, JP-A-6-120473, and JP-A-60-140752) that adopts a CCD-like characteristic in a photoelectric conversion element structure, a bulk charge modulation device (BCMD, see JP-A-64-14959), a floating well amplifier (FWA, see Japanese Patent No. 2692218 and Japanese Patent No. 3752773) in which a channel is formed on the surface thereof according to a charge amount of photo-holes accumulated to a maximum point, a source to drain current changes according to the charge amount on the surface, and, as a result, readout corresponding to a signal charge is possible, and a Vth modulation image sensor (VMIS, see JP-A-2-304973, JP-A-2005-244434, Japanese Patent No. 2935492, and JP-A-2005-85969) in which a light sensing section and a signal detecting section are divided and arranged adjacent to each other.

[0009] There is also proposed a solid-state imaging device in which a light sensing element having all functions of performing photoelectric conversion using incident light, accumulating signal charges obtained by the photoelectric conversion, and outputting signal voltage according to a charge amount of the accumulated signal charges has a potential distribution for facilitating the signal charges to be accumulated in the same place in terms of a plane and facilitating a surface channel current to flow (see JP-A-2003-31785).

[0010] These CMOS image sensors are basically front-illuminated solid-state imaging devices that irradiate light from a front side of a device.

[0011] On the other hand, there is proposed a back (rear)-illuminated solid-state imaging device that has a rear side of a silicon substrate, on which a photodiode and various transistors are formed, ground to be thinned and makes light incident from the rear side of the substrate to perform photoelectric conversion (see JP-A-10-65136).

SUMMARY OF the INVENTION

[0012] In the front-illuminated CMD, BCMD, FWA, VMIS, and the like, since the substrate is used as an overflow, back (rear) illumination is difficult and reset voltage is high.

[0013] In the front-illuminated CMD, BCMD, FWA, VMIS, and the like, since a light sensing section is arranged beside a pickup transistor, there is a disadvantage that an aperture ratio falls.

[0014] In an existing photo-gate structure, since light is received through a thin-film gate, there is a disadvantage that blue sensitivity falls.

[0015] When a photo-gate type MOS transistor is formed on an n^- layer in the front-illuminated type as in the BCMD, carrier generation by light irradiation is performed near the surface of a semiconductor. Therefore, there is a disadvantage that carriers are captured by a trap present in an interface between the semiconductor and an insulating film, accumulated carriers are not immediately discharged even if reset voltage is applied, and a device characteristic is affected.

[0016] When a light sensing photodiode region and a

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signal detection transistor are arranged to be adjacent to each other in the front-illuminated type as in the VMIS, accumulation and modulation operation for charges generated by light reception are not dynamic actions and are performed separate in terms of time. This is disadvantageous for high-speed signal processing.

[0017] Similarly, when the light sensing photodiode region and the signal detection transistor are arranged to be adjacent to each other in the front-illuminated type, contrivance such as provision of a light shielding film above a signal detecting section is necessary. Therefore, there is a disadvantage that an element manufacturing process is complicated.

[0018] In the front-illuminated BCMD image sensor, since an entire channel region below a photo-gate electrode is a charge accumulation layer, a current-voltage characteristic (ID-VDD) is not a saturation characteristic but is a triode characteristic. Therefore, there is a disadvantage that, when the image sensor is used in a source follower type, the image sensor is hard to use.

[0019] Further, in the front-illuminated CMOS image sensor, there is a disadvantage that light is blocked by wiring above pixels, sensitivity of each of the pixels falls, and, when the light reflected by the wiring is made incident on adjacent pixels, color mixture and the like are caused.

[0020] In the solid-state imaging device disclosed in JP-A-2003-31785, a two-layer gate structure is used in order to realize one transistor with a single well. Therefore, there is a disadvantage that, for example, special work is necessary for an element separation area and an element manufacturing process is complicated.

[0021] Since this solid-state imaging device is also the front-illuminated type, the solid-state imaging device also has the problems such as the fall in the blue sensitivity and the color mixture of the front-illuminated type.

[0022] In the case of the back-illuminated solid-state imaging device disclosed in JP-A-10-65138, hole accumulation regions are formed on a front side and a rear side of the substrate. However, there is a limit in formation of a shallow and dense p-type semiconductor region by ion implantation. Therefore, when it is attempted to further increase the impurity density of the p-type semiconductor region for suppression of dark currents, the p-type semiconductor region is deepened. When the p-type semiconductor region is deepened, since pn junction of the photodiode is separated from a transfer gate, it is likely that a readout ability by the transfer gate falls.

[0023] Therefore, it is desirable to provide a solid-state imaging device and a camera that can efficiently and quickly perform a series of operations such as generation and accumulation of photo-carriers, readout of charges, and transmission (reset) of remaining charges, prevent the influence of a trap on carriers in a silicon interface due to light, and realize improvement of sensitivity and pixel size shrinking without deteriorating sensitivity of light with respect to blue.

[0024] According to an embodiment of the present invention, there is provided a solid-state imaging device including pixel cells that are formed on a substrate having a first substrate surface side, on which light is irradiated, and a second substrate surface side, on which elements are formed, and separated by an adjacent cell group and an element separation layer for each of the pixel cells or with plural pixel cells as a unit. Each of the pixel cells has a first conductive well formed on the first substrate surface side and a second conductive well formed on the second substrate surface side. The first conductive well receives light from the first substrate surface side and has a photoelectric conversion function and a charge accumulation function for the received light. A transistor that detects accumulated charges in the first conductive well and has a threshold modulation function is formed in the second conductive well.

[0025] Preferably, the accumulated charges and signal charges are identical carriers.

[0026] Preferably, the transistor has a function of a readout transistor, a function of a reset transistor, and a function of a selection transistor.

[0027] Preferably, the transistor has a source and a drain and a gate electrode formed on a channel formation region between the source and the drain, and pixel signal reset is an operation for discarding charges in the drain.

[0028] Preferably, the pixel cell has a gamma characteristic that a modulation degree increases when illuminance is low.

[0029] Preferably, the pixel cell has the structure in which a capacity increases during a large signal output and has a function of realizing a high dynamic range according to the gamma characteristic.

[0030] Preferably, a second conductive separation layer is formed at least on a side of the first conductive well of the first conductive well and the second conductive well.

[0031] Preferably, a first conductive source region and a first conductive drain region are formed in the second conductive well or the second conducive separation layer, and a gate electrode is formed on a channel formation region in the second conductive well between the source region and the drain on the second substrate surface side of the substrate.

[0032] Preferably, a plurality of the pixel cells are arranged in an array form and share, with adjacent pixel cells, a part or a plurality of contacts of the drain, the source, the wells, or the gate.

[0033] Preferably, the contacts of the drain, the source, the wells, and the gate are arranged in four directions of a pixel array of the gate.

[0034] Preferably, a plurality of the pixel cells are arranged in an array form, a gate electrode of the pixel cells are formed in common to the pixel cells in a stripe shape in one direction of the pixel array, and a well contact is formed on the source region side or the drain region side.

[0035] Preferably, a well contact region is formed in the second conductive separation layer.

[0036] Preferably, the well contact region is formed in

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the second conductive separation layer on the first substrate surface side.

[0037] Preferably, when the well contact is formed on the drain side, the well contact is formed in a pinch shape with drain width reduced.

[0038] Preferably, in the arrangement of the pixel cells in the array form, the drain contacts are divided into two or more groups in a column and share a column circuit of a signal readout processing system.

[0039] Preferably, drain line wiring is backed by a conductor in order to reduce resistance.

[0040] Preferably, the solid-state imaging device has, in the gate electrode of the transistor on the second substrate surface side or a further front section of the gate electrode, a reflector that reflects light transmitted through the substrate and makes the light incident on the second conductive well and the first conductive well of the substrate.

[0041] Preferably, the thickness of the substrate is set to thickness with which near infrared light can be utilized as the reflected light of the reflector.

[0042] Preferably, the thickness of the substrate is set to thickness with which red (R) light can be utilized as the reflected light of the reflector.

[0043] Preferably, electrode wiring is formed by a transparent film having high visible light transmittance.

[0044] Preferably, the reflector is used as a predetermined wiring layer as well.

[0045] Preferably, charges are injected from the drain to the pixels immediately before pixel reset and then the pixels are reset.

[0046] Preferably, the solid-state imaging device includes an inverse γ correction circuit that performs inverse gamma correction using a transistor having a back gate terminal of the structure same as that of the transistor of the pixel cells.

[0047] Preferably, the solid-state imaging device includes a signal processing system for reading out a signal from the pixel cells, and the signal processing system includes a comparator and utilizes a reset level of a preceding line as a reference level of the comparator.

[0048] Preferably, the signal processing system has a function of performing analog sampling during D phase readout and performing digital sampling during P phase readout.

[0049] Preferably, the pixel cells are arranged in an array form to obtain one output signal with plural pixels.

[0050] Preferably, the pixel cells are arranged in an array form and separated by the element separation layer in a unit of plural pixels to obtain one output signal.

[0051] Preferably, the solid-state imaging device includes a signal processing system that performs, during signal readout from the pixels, destructive readout for continuing photoelectric conversion without resetting the pixels.

[0052] According to another embodiment of the present invention, there is provided a camera including a solid-state imaging device that receives light from a first substrate surface side of a substrate, an optical system that guides incident light to the first substrate surface side of the solid-state imaging device, and a signal processing circuit that processes an output signal of the solid-state imaging device. The solid-state imaging device includes pixel cells that are formed on the substrate having the first substrate surface side, on which light is irradiated, and a second substrate surface side, on which elements are formed, and separated by an adjacent cell group and an element separation layer for each of the pixel cells or with plural pixel cells as a unit. Each of the pixel cells has a first conductive well formed on the first substrate surface side and a second conductive well formed on the second substrate surface side. The first conductive well receives light from the first substrate surface side and has a photoelectric conversion function and a charge accumulation function for the received light. A transistor that detects accumulated charges in the first conductive well and has a threshold modulation function is formed in the second conductive well.

[0053] According to the embodiments of the present invention, light is irradiated on the pixels of the cell structure from the substrate rear surface (first substrate surface) side, photoelectric conversion of the received light is performed in the first conductive well, and charges of the light is accumulated.

[0054] The charge accumulation is detected and threshold modulation of the transistor formed in the second conductive well is performed to extract a signal.

[0055] In this way, the pixel cells have the double-well structure in the back-illuminated type. The accumulated charges and channel currents (signal charges) are identical carriers.

[0056] According to the embodiments of the present invention, it is possible to efficiently and quickly perform a series of operations such as generation and accumulation of photo-carriers, readout of charges, and transmission (reset) of remaining charges.

[0057] Further, it is possible to prevent the influence of a trap on carriers in a silicon interface due to light and realize improvement of sensitivity and pixel size shrinking without deteriorating sensitivity of light to blue.

BRIEF DESCRIPTION OF THE DRAWINGS

[0058]

Fig. 1 is a block diagram of a schematic configuration of a solid-state imaging device according to an embodiment of the present invention;

Figs. 2A and 2B are diagrams of a basic structure of a pixel section of the solid-state imaging device according to the embodiment;

Fig. 3 is a diagram of an equivalent circuit of a pixel cell according to the embodiment;

Fig. 4 is a diagram for explaining what kind of relation the wavelength of incident light has with an arrangement of transistors in the case of a front-illuminated

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BMCD;

Fig. 5 is a diagram of an overview of an energy band state formed by a transparent electrode, a gate silicon oxide film, and silicon monocrystal in the case of a front-illuminated type;

Fig. 6 is a diagram of a change in potential with respect to electrons in a semiconductor substrate in a direction perpendicular to a semiconductor substrate surface in each region according to a change in a potential state of the device shown in Figs. 2A and 2B;

Fig. 7 is a diagram of an example of a potential distribution in an a-a' line shown in Figs. 2A and 2B;

Fig. 8 is a schematic diagram of a configuration of a signal readout processing system according to the embodiment;

Fig. 9 is a diagram of an example of a layout of pixel cells in the pixel section according to the embodiment;

Figs. 10A and 10B are simplified sectional views taken along an a-a' line and a b-b' line shown in Fig. 9;

Fig. 11 is a diagram of the structure in which the pixel cells are arranged to be rotated 45 degrees from those shown in Fig. 9;

Fig. 12 is a diagram of an example of a layout in which a gate is used in common in an X direction (horizontal direction) stripe;

Fig. 13 is a diagram of an example of a layout in which a drain side is pinched;

Fig. 14 is a diagram of another example of the layout of the pixel cells in the pixel section according to the embodiment;

Figs. 15A and 15B are simplified sectional views taken along an a-a' line and a b-b' line shown in Fig. 14;

Figs. 16A and 16B are diagrams of an example in which a reflector is provided in pixel cells having different thicknesses;

Figs. 17A and 17B are diagrams of an example of a pixel cell array of a contact sharing pixel section;

Fig. 18 is a diagram of an equivalent circuit in which a layout shown in Fig. 17A is adopted and a signal processing system and a pixel section that share a column circuit are simplified;

Figs. 19A and 19B are diagrams of signal output orders in a square array shown in Figs. 17A and 17B;

Figs. 20A and 20B are diagrams of a zigzag array formed by rotating the square array shown in Figs. 17A and 17B by 45 degrees;

Fig. 21 is a diagram of an equivalent circuit in which a layout shown in Fig. 20A is adopted and a signal processing system and a pixel section that share a column circuit are simplified;

Figs. 22A and 22B are diagrams of another zigzag array formed by rotating the square array shown in Figs. 17A and 17B by 45 degrees;

Fig. 23 is a diagram of an equivalent circuit in which a layout shown in Fig. 22A is adopted and a signal processing system and a pixel section that share a column circuit are simplified;

Figs. 24A and 24B are diagrams of signal output orders in the zigzag array shown in Figs. 20A and 20B;

Figs. 25A and 25B are diagrams of signal output orders in the zigzag array shown in Figs. 22A and 22B;

Figs. 26A and 26B are diagrams for explaining an example of formation of the reflector at the time when the square array is adopted;

Fig. 27 is a diagram of a first example of the reflector and a wiring sharing layout;

Fig. 28 is a diagram of a second example of the reflector and the wiring sharing layout;

Fig. 29 is a diagram of a third example of the reflector and the wiring sharing layout;

Figs. 30A and 30B are diagrams for explaining a basic concept of pre-line reset;

Figs. 31A and 31B are conceptual diagrams of a signal processing system corresponding to a hard reset function according to the embodiment;

Fig. 32 is an equivalent circuit diagram for explaining a basic concept of a signal processing system including an inverse γ correction circuit;

Figs. 33A to 33C are diagrams of a level diagram of a pre-line reset system, two-column sharing, and 2x2 pixel timing;

Fig. 34 is a plan view of a configuration example in which plural pixels are arranged in an array form and one output signal is obtained by the plural pixels;

Fig. 35 is a plan view of a configuration example in which plural pixels are arranged in an array form and element separation is performed in a unit of plural pixels to obtain one output signal;

Figs. 36A and 36B are sectional views of configuration examples in which plural pixels are arranged in a pixel form and element separation is performed in a unit of plural pixels to obtain one output signal;

Fig. 37 is a plan view of another configuration example in which plural pixels are arranged in an array form and element separation is performed in a unit of plural pixels to obtain one output signal;

Figs. 38A and 38B are simplified sectional views taken along an a-a' line and a b-b' line shown in Fig. 37;

Fig. 39 is a diagram of an example of a wide dynamic range (Wide D-Range) sequence by nondestructive readout;

Fig. 40 is a diagram of an example of a low-speed live view sequence by nondestructive readout; and

Fig. 41 is a diagram of an example of a configuration of a camera system to which the solid-state imaging device according to the embodiment is applied.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0059] Embodiments of the present invention will be hereinafter explained with reference to the accompanying drawings.

[0060] Fig. 1 is a block diagram of a schematic configuration of a solid-state imaging device according to an

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embodiment of the present invention.

[0061] A solid-state imaging device 1 includes, as shown in Fig. 1, a pixel section 2 as a sensing section, a row direction (Y-direction) control circuit 3, a column direction (X direction) control circuit 4, and a timing control circuit 5.

[0062] In the pixel section 2, as described in detail later, plural pixel cells 2A are arranged in, for example, a matrix shape.

[0063] The pixel cells 2A of the pixel section 2 according to this embodiment is configured as a rear (back)-illuminated image sensor of a threshold modulation (CMD) system having the double-well structure.

[0064] The pixel section 2 according to this embodiment adopts the double-well structure. In the pixel section 2, accumulated charges and channel currents are identical carriers. The pixel section 2 has a one-transistor architecture (structure) in which one transistor has functions of a readout transistor, a reset transistor, and a selection transistor.

[0065] In a pixel array of the pixel section 2, the pixel cells 2A arranged in an identical row are connected to common row lines H0, H1, and the like and the pixel cells 2A arranged in an identical column are connected to common column lines V0, V1, and the like.

[0066] In the solid-state imaging device 1, a timing control circuit 5 that generates an internal clock, a row direction (Y direction) control circuit 3 that controls a row address and row scanning, and a column direction (X direction) control circuit 4 that controls a column address and column scanning are arranged as control circuits for sequentially reading out signals of the pixel section 2.

[0067] The row direction (Y direction) control circuit 3 receives a timing control pulse of the timing control circuit 5 and drives predetermined row lines H0, H1, and the like.

[0068] The row direction (X direction) control circuit 4 receives timing control pulse of the timing control circuit 5, receives signals read out to predetermined column lines V0, V1, and the like, and performs predetermined processing (CDS (Correlated Double Sampling) processing), analog to digital conversion processing, and the like.

[0069] A configuration and functions concerning signal readout processing from the pixel cells 2A in the column direction control circuit 4 are described in detail later.

[0070] A specific device structure of the pixel section of the solid-state imaging device according to this embodiment is explained below.

[0071] Figs. 2A and 2B are diagrams of a basic structure of the pixel section of the solid-state imaging device according to this embodiment. Fig. 2A is a plan view and Fig. 2B is a simplified sectional view taken along an a-a' line shown in Fig. 2A.

[0072] As shown in Fig. 2B, the solid-state imaging device 1 is formed as a rear (back)-illuminated device in which light is made incident from a first substrate surface 101 side (a rear side) of a substrate (a silicon substrate) 100 and an element area portion EAP, in which a MOS transistor is formed, is formed on a second substrate surface 102 side (a front side).

[0073] The substrate 100 is formed by thin-filming a silicon wafer such that light can be made incident from the rear side. The thickness of the substrate 100 is 2 μm to 6 μm for visible light and 6 μm to 10 μm for near infrared light depending on a type of the solid-state imaging device 1.

[0074] In this way, the substrate 100 has the first substrate surface 101 side on which light is irradiated and the second substrate surface 102 side on which elements are formed. The plural cells Cel (2A) separated by adjacent cells and an element separation layer are formed on the substrate 100.

[0075] In this embodiment, on the substrate 100, the plural pixel cells Cel (2A) separated by an adjacent cell group and the element separation layer for each of pixels cells or with plural pixel cells as a unit are formed.

[0076] Each of the pixel cells Cel includes a first conductive (in this embodiment, n-type) well (hereinafter referred to as first well) 110 formed on the first substrate surface 101 side and a second conductive (p-type) well (hereinafter referred to as second well) 120 formed further on the second substrate surface 102 side than the first well 110.

[0077] The n-type first well 110 functions as a light sensing section that receives light from the first substrate surface 101 side and has a photoelectric conversion function and a charge accumulation function for the received light.

[0078] A MOS transistor that detects accumulated charges in the light sensing section of the first well 110 and has a threshold modulation function is formed in the second well 120.

[0079] A p-type element separation layer (conductive layer) 140 of a second conducive type opposite to a first conductive type (in this embodiment, n-type) is formed to surround sidewalls of the first well 110. A p^+ layer 150 is formed on the first substrate surface 101, which is a light incident surface of the substrate 100.

[0080] An insulating film and a protective film 151 formed of, for example, silicon oxide are formed on a light incident surface side of the p^+ layer 150. A color filter 152 that transmits only light in a desired waveform region is formed on the protective film 151. A microlens 153 that condenses incident light on the light sensing section of the first well 110 is formed on the color filter 152.

[0081] In the p-type second well 120, a source region 121 and a drain region 122 formed by an n^+ layer are formed in the center thereof at a predetermined space apart from each other. A channel forming region 123 is formed between the source region 121 and the drain region 122.

[0082] Well (substrate) contact regions 124 to 127 formed of a p^+ layer are formed in an area (an end side area) of the second well 120 not overlapping the first well 110.

[0083] An insulating film 160 of silicon oxide or the like

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is selectively formed by a predetermined process on the surface of the second substrate surface 102 of the substrate 100 on which the source region 121, the drain region 122, and the well contact regions 124 to 127 are formed.

[0084] A gate electrode 131 of the transistor 130 is formed, via the insulating film 160, on the channel forming region 123 between the source region 121 and the drain region 122 on the second substrate surface 102 side of the substrate 100.

[0085] A source electrode 132 of the transistor 130 connected to the source region 121 is formed by opening a part of the insulating film 160 on the source region 121.

[0086] Similarly, a drain electrode 133 of the transistor 130 connected to the drain region 122 is formed by opening a part of the insulating film 160 on the drain region 122.

[0087] A well contact electrode 170 connected to the well contact regions 124 to 127 is formed by opening a part of the insulating film 160 on the well contact regions 124 to 127. A level of the well contact region 170 is set to, for example, the ground potential GND (0V) or -1.2 V.

[0088] In the configuration described above, the transistor 130 including an insulated-gate field effect transistor (referred to as MOS transistor) is formed by the source region 121, the drain region 122, and the channel forming region 123 formed in the second well 120 on the second substrate surface 102 side and the gate electrode 131, the source electrode 132, and the drain electrode 133 formed on the surface side of the second substrate surface 102.

[0089] In Fig. 2B, reference sign S denotes a source of the transistor 130, D denotes a drain of the transistor 130, and G denotes a gate of the transistor 130.

[0090] In this way, each of the pixel cells Cel (2A) according to this embodiment is formed as the rear (back)-illuminated image sensor of the threshold modulation (CMD) system having the double-well structure.

[0091] Fig. 3 is a diagram of an equivalent circuit of the pixel cell according to this embodiment.

[0092] The pixel cell 2A (Cel) includes, as shown in Fig. 3, a photoelectric conversion and charge accumulation element section 111 formed in the first well 110 and one transistor 130 formed by the second well 120 and an electrode on the second substrate surface 102 side.

[0093] As described above, the pixel cell Cel according to this embodiment is the back-illuminated type and has the double-well structure. In the pixel cell Cel, accumulated charges and channel currents are identical carriers. Further, the pixel cell Cel has a one-transistor architecture (structure) in which one transistor has functions of a readout transistor, a reset transistor, and a selection transistor.

[0094] In other words, in this embodiment, the pixel cell Cel is the back-illuminated type and adopts the double-well structure and does not adopt a single-well modulation system. A reason for this is explained below.

[0095] When the single-well modulation system is adopted, pocket implantation for linearity improvement is necessary. This makes it difficult to obtain saturated charges Qs during pixel size shrinking in order to reduce an accumulation region.

[0096] Even if the single-well structure has a high modulation degree and high conversion efficiency, the single-well structure is susceptible to a defect. In the single-well structure, pixel fluctuation in linearity (non-linearity like as cat's paw) tends to frequently occur and, when the pixel fluctuation occurs, it is difficult to correct the pixel fluctuation.

[0097] Since pinning comes off during readout, the single-well structure is incompatible with column digital CDS. In analog CDS, an increase in a capacity hinders pixel size shrinking.

[0098] Even if the single-well structure is combined with the back-illumination, since a reset transistor is necessary and a pixel cell has two transistors, this is disadvantageous for pixel size shrinking.

[0099] On the other hand, in this embodiment, the pixel cell Cel is the back-illuminated type and has the double-well structure, accumulated charges and channel currents are identical carriers, and pixel separation can be performed by an independent carrier. Therefore, the transistor structure does not need to be a ring. The transistor can be configured by so-called unidirectional structure of drain (D)/gate (G) /source (S) same as the structure of the normal transistor.

[0100] In this embodiment, the structure for discharging signal carriers to the drain of the transistor 130 is adopted. This realizes a complete one-transistor and lateral reset structure in which one transistor is used as a readout (pickup) transistor, a rest transistor, and a selection transistor.

[0101] In other words, since the pixel cell structure according to this embodiment only has to be the single-layer gate structure rather than the double-layer gate structure, special work is unnecessary for the element separation area.

[0102] A drain, a source, and a gate can be shared between adjacent pixels. Therefore, it is possible to remarkably improve layout efficiency and perform pixel size shrinking.

[0103] Since lateral reset by the drain of the transistor is adopted, it is possible to share a column and shrink a column circuit by using lateral wiring for the drain and using separate wiring in shared pixel units.

[0104] Since a space is formed on the gate of the transistor, a reflector structure, which makes use of metal of wiring or the like, can be provided in the space. As a result, it is possible to reflect light transmitted through a silicon (Si) substrate, photoelectrically convert the light in Si again, and improve, for example, near infrared sensitivity.

[0105] In the existing structure, dark currents generated in the interface are recombined with holes by turning off the gate during a light emission period and pinning the surface of the silicon (Si) substrate. Therefore, com-

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ponents not completely recombined cause dark current unevenness and a white dot defect.

[0106] On the other hand, in the structure according to this embodiment, since the double-well structure is adopted, there is an advantage that it is possible to discharge dark current electrons generated on the Si surface from the channel to the drain and completely shut out dark currents and white dots caused in the interface.

[0107] As a result, even if the gate is turned on during column readout, dark currents and white dots do not pose a problem. Therefore, it is possible to perform nondestructive readout of signals.

[0108] An array structure for realizing pixel size shrinking, a configuration including a reflector, a configuration and functions of a signal readout processing system, and nondestructive readout processing for signals are described in detail later.

[0109] Operations in the pixel cell having the configuration described above are explained below.

[0110] Light is made incident in the pixel cell from the first substrate surface (rear surface) 101 on the rear side. Electron and hole pairs are generated mainly by a photoelectric effect in the n-type first well 110 in the pixel cell. The generated holes are discharged to the outside through the p-type element separation layer 140 forming a wall surface of the cell.

[0111] Only the electrons are accumulated in the n-type first well 110 and accumulated in a potential well formed near a gate region semiconductor surface between the source and the drain of the transistor 130 serving as the MOS transistor. A signal of the accumulated charges is amplified and detected through the transistor 130, the accumulated charges are discharged as appropriate, and control of color mixture and a saturate charge amount is performed.

[0112] The thickness of a semiconductor layer of a sensor of the solid-state imaging device 1 is about 2 μm to 10 μm, which is the thickness enough for displaying quantum efficiency of photoelectric conversion in a wavelength range of light.

[0113] On the other hand, in the case of the front-illuminated type, usually, the thickness of the semiconductor substrate needs to be kept at the thickness (up to several hundreds μm) that makes an element less easily cracked. Therefore, a leak current between a source and a drain through a substrate of the element may be unable to be neglected and may pose a problem.

[0114] On the other hand, in this embodiment, since the thickness of the element is sufficiently small, it is possible to reduce the leak current through the substrate and prevent the problem.

[0115] The configuration and the functions of the solid-state imaging device 1 according to this embodiment are explained above.

[0116] The solid-state imaging device 1 is examined more in detail below.

[0117] Fig. 4 is a diagram for explaining what kind of relation the wavelength of incident light has with an arrangement of transistors in the case of a front-illuminated BMCD.

[0118] In a front-illuminated BMCD 10 shown in Fig. 4, an insulating film 11, transparent electrodes 12, light shielding electrodes 13, and the like are formed on a substrate front surface side. Reference numeral 14 denotes lateral drains, 15 denotes a gate insulating film, and 16 denotes a silicon substrate.

[0119] In the case of the front illumination shown in Fig. 4, light penetrates from a side on which transistors are set. Since the lateral drain regions 14 are covered with the light shielding electrodes 13, the light penetrates into the silicon substrate 16 from an opening other than the lateral drain regions 14 while being transmitted through the insulating film 11, the transparent electrodes 12, the gate insulating film 15, and the like. Red light and near infrared light having large wavelength penetrate relatively deep from the surface of silicon. However, blue light and near ultraviolet light are photoelectrically converted in a place not so deep inside. When light having small wavelength passes through an insulating multilayer film on the surface, the light tends to lose energy because of scattering, absorption, reflection on an interface surface, or the like.

[0120] On the other hand, in the case of the rear illumination according to the embodiment shown in Fig. 2B, light penetrates into the substrate (the silicon substrate) 100 from the side where the transistor 130 is not arranged. Most of light having large wavelength reaches near the transistor 130 but only a part of light having small wavelength reaches near the transistor 130.

[0121] Various proposals are made concerning how a diffusion layer of a source and a drain and a well layer should be formed in order to maximize quantum efficiency including the wavelength of incident light.

[0122] However, there is little argument concerning the possibility that light passing through a silicon oxide film (an insulating film) affects a transistor characteristic. In this embodiment, a mechanism concerning this point is clarified to some extent, although qualitatively.

[0123] Fig. 5 is a diagram of an overview of an energy band state formed by a transparent electrode, a gate silicon oxide film, and silicon monocrystal in the case of the front-illuminated type.

[0124] A characteristic of a gate oxide film may be considerably different depending on a manufacturing method or processing. When the manufacturing method of the processing is not well-controlled, a trap that captures electrons and holes remains in the silicon oxide film. In the figure, a trap that captures electrons is present in a position of 2.0 eV under a conduction band of the silicon oxide film.

[0125] In the case of a silicon thermal oxide film, a band gap is about 8.0 eV. When an ITO is used as a transparent electrode, a work function is about 4.3 eV to 4.7 eV. Therefore, a Fermi level of the transparent electrode is located a little below the center of an energy gap of the silicon thermal oxide film.

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[0126] When attention is paid to a blue light component in incident light, for example, wavelength λ of 450 nm, this is equivalent to E=2.75eV from the Einstein photoelectric law E=hν. As shown in the figure, this energy is substantially equal to a position of an energy level of an electron trap in the oxide film measured from the Fermi level of the transparent electrode.

[0127] At this point, if relatively large negative voltage is applied to the transparent gate electrode compared with voltage applied to the silicon substrate, electrons ejected from the metal surface (the transparent electrode) by the photoelectric effect are excited in the oxide film and captured by the trap.

[0128] The electrons captured by the trap are ejected again by an electric field, flow into the conduction band of the silicon monocrystal according to hopping conduction, bring the gate electrode and the silicon into a weak conduction state, and cause fluctuation in the transistor characteristic and a signal amount.

[0129] In the rear illumination according to this embodiment, light having large energy and small wavelength consumes most of energy thereof for photo-carrier generation in the silicon substrate until the light reaches the transistor region. Therefore, the rear illumination does not have the disadvantage of the front illumination.

[0130] Fig. 6 is a diagram of a change in potential with respect to electrons in a semiconductor substrate in a direction perpendicular to a semiconductor substrate surface in each of regions according to a potential state change of the device shown in Figs. 2A and 2B.

[0131] In all states, voltage VGND of the well contact electrode 170 is set to 0 V.

(i) Gate readout

[0132] When the gate voltage VG of the transistor 130 is set to 1.0 V and the drain voltage VD thereof is set to 1.8 V, the source voltage VS thereof is about 1. 6 V to 1.4 V. Accumulated charges (electrons) decrease and a channel electron current flowing from the source to the drain is modulated and decreases according to the decrease in the accumulated charges. If this current change is measured, an amount of change of charges of the accumulated electrons is obtained.

(ii) Gate accumulation (non-readout state)

[0133] When the gate voltage VG of the transistor 130 is set to 0 V and the drain voltage VD thereof is set to 1.8 V, the source voltage VS thereof is equal to or lower than 1.2 V. Electrons are accumulated in the potential well formed near the semiconductor surface in the gate region between the source and the drain of the transistor 130.

(iii) Gate accumulation (non-reset state, hard reset)

[0134] When the gate voltage VG of the transistor 130 is set to 0 V to -1.0 V and the drain voltage VD thereof is set to 1.8 V, the source voltage VS thereof has high impedance Hi-Z or LD. The accumulated electrons overflow. In other words, the pixel cell Cel is saturated. At this point, a signal is held.

(iv) Reset

[0135] When the gate voltage VG of the transistor 130 is set to 0 V to -1.0 V and the drain voltage VD thereof is set to be equal to or higher than 3.0 V, for example, set to 3.7 V, the source voltage VS thereof has high impedance Hi-Z or LD. The electrons present in the accumulation well are discharged to the outside through the drain electrode.

[0136] As described above, in this embodiment, as pixel signal reset, the drain voltage VD is modulated and, in some case, both the drain voltage VD and the gate voltage VG are modulated (in the example shown in Fig. 6, a potential difference between the drain and the gate is increased) to discharge signal charges (electrons) accumulated in the drain electrode.

[0137] In this embodiment, a so-called gamma (γ) characteristic is given to the pixel cell to increase a degree of modulation and conversion efficiency when illuminance is low.

[0138] In this embodiment, the γ characteristic is applied to a high dynamic range (DR).

[0139] The γ characteristic of the pixel cell is explained below.

[0140] Fig. 7 is a diagram of an example of a potential distribution in an a-a' line shown in Fig. 2A.

[0141] As one of characteristics of a double well, as shown in Fig. 7, a sensor accumulation region has a broad potential shape. Therefore, a capacity of the double well changes according to a signal amount and has nonlinearity (the γ characteristic).

[0142] However, in the case of the γ characteristic that a gain increases during a small signal output in response to nonlinearity of the single-well structure and lack of a signal during the small signal output, since inverse γ correction is possible and a gain during low illuminance is minus, noise is compressed simultaneously with the signal. This makes it possible to reduce noise.

[0143] In this way, in this embodiment, the γ characteristic is positively utilized and, as shown in Fig. 2B, a rather deep n-type gamma pocket 180 for accumulating small signals is provided.

[0144] In the gamma pocket 180, signal carries and signal currents concentrate on one point and a degree of modulation of the small signals is improved.

[0145] It is possible to perform inverse gamma correction in a DSP at a later stage, which performs signal processing, and realize total noise compression.

[0146] As shown in Fig. 7, the pixel cell Cel has the structure in which a capacity thereof increases during a large signal output and realizes the high dynamic range (DR) according to the γ characteristic.

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[0147] Fig. 8 is a schematic diagram of a configuration of the signal readout processing system according to this embodiment.

[0148] The column (X) direction control circuit 4 includes a CDS circuit 41. An accumulated signal of the pixel cell Cel in an ON state is transferred to the CDS circuit 41 through a signal transmission line SL and a switch SW. Reference sign IS denotes a current source for forming a source follower.

[0149] The configuration and the functions of the pixel cell according to this embodiment are explained above.

[0150] An array of the pixel cells of the pixel section 2, a configuration including a reflector, and the like are explained below.

[0151] Fig. 9 is a diagram of an example of a layout of pixel cells in the pixel section according to this embodiment. Fig. 10A is a simplified sectional view taken along an a-a' line shown in Fig. 9. Fig. 10B is a simplified sectional view taken along a b-b' line shown in Fig. 9.

[0152] In this example, the pixel cells Cel are arranged in a matrix shape. A Bayer array is adopted.

[0153] A p-type element separation layer (conductive layer) 140A is formed on sidewalls of the first well 110 and the second well 120. A source region 141 and a drain region 142 including the n^+ layer forming the transistor 130 are formed in the p-type element separation layer 140A. A well contact region 143 is formed on the source region 141 side or the drain region 142 side. In this example, the well contact region 143 is formed on the source region 141 side.

[0154] A gate contact electrode 190 is formed in a position opposed to the p-type element separation layer 140A.

[0155] A reflector 200 is formed on a front side (a side where light is not irradiated) of the gate electrode 131 of the pixel cell Cel excluding the element separation layer 140A.

[0156] In this way, the pixel cells are arranged to share, with adjacent pixel cells, a part or a plurality of contacts of the drain, the source, the wells, or the gate. This makes it possible to improve the layout efficiency.

[0157] In other words, since the pixel cell Cel can be configured by one transistor, the contacts of the drain, the source, the gate, and the well are arranged in the four directions on the pixel separation layers and the gate occupies the entire pixel. Therefore, random noise of the transistor is remarkably reduced.

[0158] In the layout example shown in Fig. 9, a drain contact DCNT and a source contact SCNT are shared by pixel cells adjacent to each other in a Y direction (a vertical direction or a row direction) of X and Y directions shown in the figure. A gate contact GCNT and a well contact WCNT are shared by pixel cells adjacent to each other in the X direction (a horizontal direction or a column direction).

[0159] In this way, the drain contact DCNT, the source contact SCNT, the gate contact GCNT, and the well (substrate) contact WCNT can be arranged in the four direction of the gate. Therefore, as shown in Fig. 11, the layout can be used in a so-called zigzag array as well.

[0160] In an example shown in Fig. 11, the arrangement shown in Fig. 9 is rotated by 45 degrees.

[0161] Fig. 12 is a diagram of an example of a layout in which a gate is shared in an X direction (horizontal direction) stripe.

[0162] As shown in the figure, in the layout, the gate is shared in the horizontal stripe and the well (substrate) contact WCNT is set on the source side or the drain side. This makes it possible to easily form the reflector 200.

[0163] In this case, the well (substrate) contact WCNT may be arranged in every other column in the X (horizontal) direction.

[0164] It may be determined according to withstanding pressure or a layout whether the well (substrate) contact WCNT should be set on the drain side or the source side.

[0165] When the well (substrate) contact WCNT is set on the source side, since a potential difference is reduced, there is an advantage that pixel size shrinking can be easily performed.

[0166] Fig. 13 is a diagram of an example of a layout in which the drain side is pinched.

[0167] When the well (substrate) contact WCNT is set on the drain side, drain width is reduced, i.e., pinched to secure withstanding pressure.

[0168] Consequently, since a cannel on the source side is widened, the source side is deepened and a portion in which signals are accumulated and a portion to which modulation tends to be applied coincide with each other, and a high modulation characteristic is obtained.

[0169] Fig. 14 is a diagram of another example of the layout of the pixel cells in the pixel section according to this embodiment. Fig. 15A is a simplified sectional view taken along an a-a' line shown in Fig. 14. Fig. 15B is a simplified sectional view taken along a b-b' line shown in Fig. 14.

[0170] The layout shown in Fig. 14 is the same as that of the example shown in Fig. 9. However, in this example, the well (substrate) contact WCNT is formed on the first substrate surface 101 (rear surface) side rather than the second substrate surface 102 side. The gate electrode 131 is formed over the entire pixel cell including the p-type element separation layer 140A on the second substrate surface 102 side.

[0171] In this case, a not-shown light shielding film for color mixture prevention can also be used as not-shown wiring.

[0172] By adopting such a configuration, wiring of the reflector 200 is symmetrically formed. This is advantageous in terms of withstanding pressure.

[0173] The reflector 200 is explained more in detail.

[0174] In the pixel cell Cel according to this embodiment that is the back-illuminated type and adopts the double-well structure, a space is formed on the gate electrode 131 of the transistor 130. Therefore, a reflector structure, which makes use of metal of wiring or the like, can be provided in the space.

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[0175] Light transmitted through the silicon substrate 100 is reflected by the reflector 200 and photoelectrically converted in the first well 110 of the silicon substrate 100 again. This makes it possible to improve, for example, near infrared sensitivity.

[0176] In this case, as shown in Fig. 16A, the substrate is relatively thick (about 6 μm to 10 μm) and can be applied to, for example, a night vision monitor camera by making use of reflection of near infrared light by the reflector 200.

[0177] Moreover, as shown in Fig. 16B, if the thickness of the substrate 100 is positively reduced to reflect G light to R light, it is possible to further halve a pixel size because only about a half substrate thickness is necessary. This makes it possible to prevent color mixture.

[0178] Usually, a silicon substrate needs to have the thickness of 2 μm to 3 μm is necessary for visible light and has to receive light with an angle of incidence up to about 25 degrees. About 1:2 in an aspect ratio is a limit. Therefore, it is said that about 1 μm to 1.5 μm is a limit of the pixel size.

[0179] However, as in this embodiment, if the reflector 200 is used, the silicon substrate has to have only a half thickness 1 μm to 1.5 μm. Therefore, as the pixel size, a sub-micron pixel is possible.

[0180] In this case, it is desirable to use an ITO film having high visible light transmittance for an electrode.

[0181] In this embodiment, the reflector 200 is wiring of metal (Al, etc.). This configuration example is described later.

[0182] Although not specifically explained, a reflector may be formed of a nonconductive insulating film or the like.

[0183] A configuration in which downsizing can be realized by sharing a column circuit is explained below.

[0184] In this case, in the matrix array of the pixel cells in the pixel section 2, drain contacts are divided into two or more groups in a column to share a column circuit in the column direction (X direction) control circuit 4 and realize downsizing.

[0185] Figs. 17A and 17B are diagrams of an example of a pixel cell array of a contact sharing pixel section. Fig. 17A is a diagram of an example of a layout of pixel cells. Fig. 17B is a diagram of a pattern layout corresponding to Fig. 17A.

[0186] Fig. 18 is a diagram of an equivalent circuit in which the layout shown in Fig. 17A is adopted and signal processing system and pixel sections that share a column circuit are simplified.

[0187] In the following explanation, it is assumed that a signal Sel is supplied to a selected gate of a transistor.

[0188] In this example, two vertical lines share a drain.

[0189] In the example shown in Fig. 17A, selected and shown sixteen cells Cel are arranged in a matrix shape.

[0190] Basically, the Bayer array is adopted. A pixel cell Cel11 of G (green, Gr) is arranged in the first row, first column, a pixel cell Cel12 of B (blue) is arranged in the first row, second column, a pixel cell Cel21 of R (red) is arranged in the second row, first column, and a pixel cell Cel22 of G (Gb) is arranged in the second row, second column.

[0191] Similarly, a pixel cell Cel13 of G (Gr) is arranged in the first row, third column, a pixel cell Cel14 of B is arranged in the first row, fourth column, a pixel cell Cel23 of R is arranged in the second row, third column, and a pixel cell Cel24 of G (Gb) is arranged in the second row, second column.

[0192] A pixel cell Cel31 of G is arranged in the third row, first column, a pixel cell Cel32 of B is arranged in the third row, second column, a pixel cell Cel41 of R is arranged in the fourth row, first column, and a pixel cell Cel42 of G (Gb) is arranged in the fourth row, second column.

[0193] Similarly, a pixel cell Cel33 of G (Gr) is arranged in the third row, third column, a pixel cell Cel34 of B is arranged in the third row, fourth column, a pixel cell Cel43 of R is arranged in the fourth row, third column, and a pixel cell Cel44 of G (Gb) is arranged in the fourth row, fourth column.

[0194] In each of the columns of the pixel cell array, pixel cells in an odd number row and an even number row adjacent to each other share a drain contact.

[0195] In the example shown in Fig. 17A, the pixel cells Cel11 and Cel21 share the drain contact DCNT and the pixel cells Cel31 and Cel41 share the drain contact DCNT.

[0196] Similarly, the pixel cells Cel12 and Cel22 share the drain contact DCNT and the pixel cells Cel32 and Cel42 share the drain contact DCNT.

[0197] The pixel cells Cel13 and Cel23 share the drain contact DCNT and the pixel cells Cel33 and Cel43 share the drain contact DCNT.

[0198] The pixel cells Cel14 and Cel24 share the drain contact DCNT and the pixel cells Cel34 and Cel44 share the drain contact DCNT.

[0199] In the example shown in Fig. 17A, a group GRP1 is formed by the pixel cells Cel11 to Cel14 in the first row and the pixel cells Cel21 to Cel24 in the second row that share the drain contact DCNT.

[0200] Similarly, a group GRP2 is formed by the pixel cells Cel31 to Cel34 in the third row and the pixel cells Cel41 to Cel44 in the fourth row that share the drain contact DCNT.

[0201] In each of the columns between groups adjacent to each other, pixel cells adjacent to each other share the source contact SCNT.

[0202] In the example shown in Fig. 17A, the pixel cell Cel21 of the group GRP1 and the pixel cell CEL31 of the group GRP2 share the source contact SCNT.

[0203] The pixel cell Cel22 of the group GRP1 and the pixel cell Cel32 of the group GRP2 share the source contact SCNT.

[0204] The pixel cell Cel23 of the group GRP1 and the pixel cell Cel33 of the group GRP2 share the source contact SCNT.

[0205] The pixel cell Cel24 of the group GRP1 and the

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pixel cell Cel34 of the group GRP2 share the source contact SCNT.

[0206] In Fig. 17B, reference signs LGND1 to LGND5 and the like denote ground lines connected to the well contact WCNT, LSGN1 to LSGN4 and the like denote signal lines connected to the source contact SCNT, LGT1 to LGT3 and the like denote gate lines connected to the gate contact, and LDRN1 to LDRN 4 and the like denote drain lines connected to the drain contact.

[0207] The ground line LGND and the signal line LSGN are wired for each of the columns in the Y direction (the row direction).

[0208] The gate line LGT and the drain line LDRN are wired for each of the rows in the X direction (the column direction).

[0209] The ground line LGND, the signal line LSGN, the gate line LGT, and the drain line LDRN are formed by a laminated structure of the wiring.

[0210] For example, the ground line LGND is formed by first metal wiring (1MT) in a bottom layer.

[0211] The signal line LSGN is formed by second metal wiring (2MT) in a layer second from the bottom.

[0212] The gate line LGT and the drain line LDRN are formed by third metal wiring (3MT) of a top layer via an insulating film provided between the lines while maintaining insulating properties.

[0213] In this embodiment, the drain line LDRN formed by the third metal wiring is backed by, for example, Al wiring Lal to reduce resistance as measures against IR drop.

[0214] In this embodiment, as shown in Figs. 17A and 17B and Fig. 18, in each of the groups GRP1 to GRP3, in pixel cells that share the drain contact, the gate contact GCNT and the well (substrate) contact WCNT are formed to face opposite directions in the X direction (the column direction).

[0215] In an odd number column and an even number column, the gate contact GCNT and the well (substrate) contact WCNT are formed to face opposite directions as well.

[0216] Specifically, in the group GRP1, the gate contact GCNT of the pixel cell Cel11 in the first column is formed on the left side in the figure in the X direction and the well contact WCNT is formed on the right side in the figure in the X direction.

[0217] On the pixel cell Cel21 in the first column, the gate contact GCNT is formed on the right side in the figure in the X direction and the well contact WCNT is formed on the left side in the figure in the X direction.

[0218] The gate of the transistor 130 of the pixel cell Cel11 is connected to the gate line LGT1 via the gate contact GCNT. The well contact WCNT is connected to the ground line LGND2 wired in the second column.

[0219] The gate of the transistor 130 of the pixel cell Cel21 is connected to the gate line LGT1 via the gate contact GCNT. The well contact WCNT is connected to the ground line LGND1 wired in the first column.

[0220] On the pixel cell Cel12 in the second column, the gate contact GCNT is formed on the right side in the figure in the X direction. The well contact WCNT is formed on the left side in the figure in the X direction.

[0221] The gate contact GCNT of the pixel cell Cel22 in the second column is formed on the left side in the figure in the X direction. The well contact WCNT is formed on the right side in the figure in the X direction.

[0222] The gate of the transistor 130 of the pixel cell Cel12 is connected to the gate line LGT1 via the gate contact GCNT. The well contact WCNT is connected to the ground line LGND2 wired in the second column.

[0223] The gate of the transistor 130 of the pixel cell Cel22 is connected to the gate line LGT1 via the gate contact GCNT. The well contact WCNT is connected to the ground line LGND3 wired in the third column.

[0224] The gate contact GCNT of the pixel cell Cel13 in the third column is formed on the left side in the figure in the X direction and the well contact WCNT is formed on the right side in the figure in the X direction.

[0225] The gate contact GCNT of the pixel cell Cel23 in the first column is formed on the right side in the figure in the X direction and the well contact WCNT is formed on the left side in the figure in the X direction.

[0226] The gate of the transistor 130 of the pixel cell Cel13 is connected to the gate line LGT1 via the gate contact GCNT. The well contact WCNT is connected to the ground line LGND4 wired in the fourth column.

[0227] The gate of the transistor 130 of the pixel cell Cel23 is connected to the gate line LGT1 via the gate contact GCNT. The well contact WCNT is connected to the ground line LGND3 wired in the third column.

[0228] The gate contact GCNT of the pixel cell Cel14 in the fourth column is formed on the right side in the figure in the X direction and the well contact WCNT is formed on the left side in the figure in the X direction.

[0229] The gate contact GCNT of the pixel cell Cel24 in the second column is formed on the left side in the figure in the X direction and the well contact WCNT is formed on the right side in the figure in the X direction.

[0230] The gate of the transistor 130 of the pixel cell Cel14 is connected to the gate line LGT1 via the gate contact GCNT. The well contact WCNT is connected to the ground line LGND4 wired in the fourth column.

[0231] The gate of the transistor 130 of the pixel cell Cel24 is connected to the gate line LGT1 via the gate contact GCNT. The well contact WCNT is connected to the ground line LGND5 (not shown) wired in the fifth column.

[0232] The groups GRP2 and GRP3 are basically formed in the same pattern. Therefore, detailed explanation of the groups GRP2 and GRP3 is omitted.

[0233] As shown in Fig. 18, for top readout and bottom readout, the signal lines LSGN1 to LSGN4 and the like are respectively divided into two signal lines LSGN1-T and LSGN1-B, LSGN2-T and LSGN2-B, LSGN3-T and LSGN3-B, and LSGN4-T and LSGN4-B and the like.

[0234] An odd number group select switch (a top switch) OGSW1 and an even number group select switch

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(a bottom switch) EGSW1 are provided and a top switch OGSW2 and a bottom switch EGSW2 are provided in a unit of two columns.

[0235] The signal lines LSGN1-T and LSGN2-T are connected to two switching terminals of the top switch OGSW1. The signal lines LSGN1-B and LSGN2-B are connected to two switching terminals of the bottom switch EGSW1. The signal lines LSGN1-T and LSGN2-T are connected to the source contact SCNT of the odd number groups GRP1, GRP3 and the like. The signal lines LSGN1-B and LSGN2-B are connected to the source contact SCNT of the even number groups GRP2, GRP4 and the like.

[0236] Similarly, the signal lines LSGN3-T and LSGN4-T are connected to two switching terminals of the top switch OGSW2. The signal lines LSGN3-B and LSGN3-B are connected to two switching terminals of the bottom switch EGSW2. The signal lines LSGN3-T and LSGN4-T are connected to the source contact SCNT of the odd number groups GRP1, GRP3 and the like. The signal lines LSGN3-B and LSGN4-B are connected to the source contact SCNT of the even number groups GRP2, GRP4 and the like.

[0237] Fixed terminals of the top switches OGSW1, OGSW2 and the like are connected to a first signal transfer line LSTM1. Fixed terminals of the bottom switches EGSW1 and EGSW2 are connected to a second signal transfer line LSTM2.

[0238] A current source I401 is connected to the first signal transfer line LSTM1. A connection point of the current source I401 and the first signal transfer line LSTM1 is connected to a comparator 401 of a column circuit 400 via a capacitor C401.

[0239] An inverting input (-) of the comparator 401 is connected to the capacitor C401. Reference potential is given to a non-inverting input (+) thereof.

[0240] A reset switch 402 is connected between the inverting input (-) and an output of the comparator 401. The switch 402 is formed by, for example, a MOS transistor.

[0241] A current source I411 is connected to the second signal transfer line LSTM2. A connection point of the current source I411 and the second signal transfer line LSTM2 is connected to a comparator 411 of a column circuit 410 via a capacitor 411.

[0242] An inverting input (-) of the comparator 411 is connected to the capacitor C411. Reference potential is given to a non-inverting input (+) thereof.

[0243] A reset switch 412 is connected between the inverting input (-) and an output of the comparator 411. The switch 412 is formed by, for example, a MOS transistor.

[0244] In such a configuration, it is possible to perform reset separately for an odd number and an even number and sample signals in order of a D phase Do of the odd number, a P phase Po of the odd number, a D phase De of the even number, and a P phase Pe of the even number. It is possible to perform arbitrary adding processing of signals from same color pixels with digital addition both vertically and horizontally (counter addition vertically).

[0245] Figs. 19A and 19B are diagrams of signal output orders in the square array shown in Figs. 17A and 17B. Fig. 19A is a diagram of a signal output order for outputting signals when horizontal columns are not shared. Fig. 19B is a diagram of a signal output order for outputting signals when horizontal columns are shared.

[0246] In Figs. 19A and 19B, to arrange pixel cells in the signal output orders, an arrangement of the pixel cells is vertically reversed from that shown in the layout diagram.

[0247] In this example, rows and columns are represented as V rows and H columns and numbers are affixed to the respective rows and columns. Numbers corresponding to RGB of pixel cells and a matrix array are given to output signals. For example, a signal in the first row, first column is represented as R11 and a signal in the first row, second column is represented as G12.

[0248] In the case of an example shown in Fig. 19A, signals are outputted in order according to a pixel cell array both on a bottom side and a top side.

[0249] In the case of an example shown in Fig. 19B, signals are outputted in a time division manner.

[0250] For example, first, signals of pixel cells G12, G14, and the like are read out on the bottom side and signals of pixel cells B22 and B24 are readout on the top side and, second, signals of pixel cells R11, R13, and the like are read out on the bottom side and signals of pixel cells G21 and G23 are read out on the top side.

[0251] In this way, it is possible to perform signal readout for each of same colors and perform arbitrary adding processing of signals from same color pixels.

[0252] As explained above, in the example shown in Figs. 17A and 17B and Fig. 18, Gb and Gr are alternately read out for every two lines and read out dividedly in an odd number column and an even number column.

[0253] In this example, since a drain is shared by two lines, parallel processing according to an upper and lower column array (double speed) is necessary. Moreover, since signals of Gr/Gb lines are outputted from above and below alternately for every two lines, digital addition or 2/4 thinning-out is performed vertically.

[0254] It is possible to share two or more horizontal columns according to separation of a horizontal reset drain (e.g., into an odd number column and an even number column) (1/n deceleration).

[0255] Further, it is possible to perform column shrinking.

[0256] Moreover, it is possible to perform, in color coding synchronization, arbitrary adding processing of signals from same color pixels by digital addition in an identical column signal.

[0257] Furthermore, since the horizontal wiring of the drain line LDRN is backed by Al for a reduction in resistance, it is possible to prevent a fall in signal voltage transmitted to the drain line.

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[0258] Figs. 20A and 20B are diagrams of a zigzag array formed by rotating the square array shown in Figs. 17A and 17B by 45 degrees. Fig. 20A is a diagram of an example of a layout of pixel cells. Fig. 20B is a diagram of a pattern layout corresponding to Fig. 20A.

[0259] Fig. 21 is a diagram of an equivalent circuit in which the layout shown in Fig. 20A is adopted and a signal processing system and a pixel section that share a column circuit are simplified.

[0260] The zigzag array can be realized by simply rotating an electrode and the structure below the electrode by 45 degrees and contriving wiring for the zigzag array.

[0261] In this case, a basic operation is the same as that in the case of the square array shown in Figs. 17A and 17B and Fig. 18. It is possible to perform reset separately for an odd number and an even number and sample signals in order of a D phase Do of the odd number, a P phase Po of the odd number, a D phase De of the even number, and a P phase Pe of the even number. It is possible to perform arbitrary adding processing of signals from same color pixels with digital addition both vertically and horizontally (counter addition vertically).

[0262] Figs. 22A and 22B are diagrams of another zigzag array formed by rotating the square array shown in Figs. 17A and 17B. Fig. 22A is a diagram of an example of a layout of pixel cells. Fig. 22B is a diagram of a pattern layout corresponding to Fig. 22A.

[0263] Fig. 23 is a diagram of an equivalent circuit in which the layout shown in Fig. 22A is adopted and a signal processing system and a pixel section that share a column circuit are simplified.

[0264] In an example shown in Figs. 20A and 20B and Fig. 21, a form of signal readout is the same as that in the case of Figs. 17A and 17B and Fig. 18. However, in an example shown in Figs. 22A and 22B and Fig. 23, a column at the bottom and a column at the top are alternately arranged.

[0265] In this case, a basic operation is the same as that in the case of the square array shown in Figs. 17A and 17B and Fig. 18. It is possible to perform reset separately for an odd number and an even number and sample signals in order of a D phase Do of the odd number, a P phase Po of the odd number, a D phase De of the even number, and a P phase Pe of the even number. It is possible to perform arbitrary adding processing of signals from same color pixels with digital addition both vertically and horizontally (counter addition vertically).

[0266] Figs. 24A and 24B are diagrams of signal output orders in the zigzag array shown in Figs. 20A and 20B. Fig. 24A is a diagram of a signal output order for outputting signals when horizontal columns are not shared. Fig. 24B is a diagram of a signal output order for outputting signals when horizontal columns are shared.

[0267] In this example, rows and columns are represented as V rows and H columns and numbers are affixed to the respective rows and columns. Numbers corresponding to RGB of pixel cells and a matrix array are given to output signals.

[0268] In the case of an example shown in Fig. 24A, signals are outputted in order according to a pixel cell array both on a bottom side and a top side.

[0269] In the case of an example shown in Fig. 24B, signals are outputted in a time division manner.

[0270] For example, first, signals of pixel cells R11, R13, and the like are read out on the bottom side and signals of pixel cells G22 and G24 are readout on the top side and, second, signals of pixel cells B12, B14, and the like are read out on the bottom side and signals of pixel cells G23 and G25 are read out on the top side.

[0271] In this way, it is possible to perform signal readout for each of same colors and perform arbitrary adding processing of signals from same color pixels.

[0272] Figs. 25A and 25B are diagrams of signal output orders in the zigzag array shown in Figs. 22A and 22B. Fig. 25A is a diagram of a signal output order for outputting signals when horizontal columns are not shared. Fig. 25B is a diagram of a signal output order for outputting signals when horizontal columns are shared.

[0273] In this example, rows and columns are represented as V rows and H columns and numbers are affixed to the respective rows and columns. Numbers corresponding to RGB of pixel cells and a matrix array are given to output signals.

[0274] In the case of an example shown in Fig. 25A, signals are outputted in order according to a pixel cell array both on a bottom side and a top side.

[0275] In the case of an example shown in Fig. 25B, signals are outputted in a time division manner.

[0276] For example, first, signals of pixel cells R11, R13, R15, and the like are read out on the bottom side and signals of pixel cells G21, G23, and G25 are readout on the top side and, second, signals of pixel cells G22, G24, G26, and the like are read out on the bottom side and signals of pixel cells B12, B14, and B16 are read out on the top side.

[0277] In this way, it is possible to perform signal readout for each of same colors and perform arbitrary adding processing of signals from same color pixels.

[0278] The specific examples of the pixel cell array are explained above.

[0279] An example of formation of a reflector at the time when the square array shown in Figs. 17A and 17B is adopted is explained below.

[0280] In the pixel cell array according to this embodiment, the drain contact DCNT, the source contact SCNT, the gate contact GCNT, and the well (substrate) contact WCNT can be arranged in the four direction of the gate. Therefore, as shown in Fig. 26A, an entire light sensing region is a gate region.

[0281] Therefore, as shown in Fig. 26B, the reflector 200 can be basically formed to be superimposed on the entire gate region.

[0282] On the other hand, when the square array shown in Figs. 17A and 17B is adopted, the reflector can be formed by using any wiring of a laminated structure.

[0283] First to third examples are explained below.

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[0284] Fig. 27 is a diagram of a first example of the reflector and a wiring sharing layout.

[0285] Fig. 28 is a diagram of a second example of the reflector and the wiring sharing layout.

[0286] Fig. 29 is a diagram of a third example of the reflector and the wiring sharing layout.

[0287] In the first example shown in Fig. 27, unlike the example shown in Figs. 17A and 17B, the gate line LGT is first metal wiring, the drain line LDRN is second metal wiring, and the signal line LSGN and the ground line LGND are third metal wiring.

[0288] In this case, the first metal wiring of the gate line LGT is used as the reflector 200. The reflector 200 is selectively formed in association with the gate region.

[0289] In the second example shown in Fig. 28, as in the example shown in Figs. 17A and 17B, the ground line LGND is first metal wiring, the signal line LSGN is second metal wiring, and the gate line LGT and the drain line LDRN are third metal wiring.

[0290] In this case, the first metal wiring of the ground line LGND is used as the reflector 200.

[0291] In the third example shown in Fig. 29, as in the example shown in Fig. 27, the gate line LGT is first metal wiring, the drain line LDRN is second metal wiring, and the signal line LSGN and the ground line LGND are third metal wiring.

[0292] In this case, the first metal wiring of the gate line LGT is used as the reflector 200. The reflector 200 is formed in a stripe shape.

[0293] The examples of the pixel cell structure, the array, and the formation of the reflector are explained above.

[0294] A characteristic configuration and functions of the signal processing system including the column circuit side are explained below.

[0295] First, in this embodiment, the solid-state imaging device 1 has a pre-line reset function for improving large light amount resistance using a reset level of a preceding line as a reference level of the comparator 401 (411) of the column circuit 400 (410).

[0296] Figs. 30A and 30B are diagrams for explaining a basic concept of pre-line reset. Fig. 30A is a diagram of an equivalent circuit. Fig. 30B is a timing chart.

[0297] In this case, before an operation for comparison with a ramp waveform VRAMP in the comparator 401 (411) (before D-phase readout), the switch (SW) 402 (412) of the column circuit 400 (410) is turned on and an input and an output of the comparator are connected to perform circuit reset.

[0298] Consequently, large light amount resistance is improved by using a reset level of a preceding line as a reference level of the comparator 401 (411) of the column circuit 400 (410).

[0299] This embodiment adopts a function of reducing a residual image by performing a reset operation after injecting charges from the drain to the pixels immediately before pixel reset to saturate the pixel cells (hard resetting the pixel cells).

[0300] Figs. 31A and 31B are schematic diagrams of a signal processing system corresponding to a hard reset function according to this embodiment. Fig. 31A is a diagram of an equivalent circuit. Fig. 31B is a timing chart.

[0301] In this case, a transistor Q401, a drain of which is connected to power supply potential and a source of which is connected to the capacitor C401 (C411), a capacitor C402 connected between a connection point of the transistor Q401 and a ground line via a switch SW402, a current source I402 connected to the source of the transistor Q401 via a switch W403, and a current source I403 connected to a gate of the transistor Q401 are provided between the switch SW 401 and the capacitor C401 (C411) arranged between the signal transfer line and the column line 400 (410). The gate of the transistor Q401 is connected to a switch SW401.

[0302] In the hard reset, when the gate voltage VG of the transistor 130 is set to 0 V to -1.0 V and the drain voltage VD thereof is set to 1.8 V, the source voltage VS thereof is high impedance Hi-Z or LD. The accumulated electrons overflow (OF). In other words, the pixel cell Cel is saturated. At this point, a signal is held.

[0303] In the following reset operation, when the gate voltage VG of the transistor 130 is set to 0 V to -1.0 V and the drain voltage VD thereof is set to be equal to or higher than 3.0 V, for example, set to 3.7 V, the source voltage VS thereof is high impedance Hi-Z or LD. The electrons present in the accumulation well are discharged to the outside through the drain electrode.

[0304] In this case, to prevent leak on a signal side that consumes sampling time, for example, analog sampling is performed only on the signal side and the CDS is digitally performed. As a result, a significant improvement effect is obtained by adding one capacitor.

[0305] For example, it is possible to improve large light amount resistance with a small size by combining analog sampling for a D phase and digital sampling for a P phase.

[0306] A circuit configuration corresponding to the analog SHD and the digital CDS can be applied to pixel cells of a so-called floating diffusion (FD) configuration as well.

[0307] In this embodiment, a γ characteristic is positively given to the pixel cells. In association with the γ characteristic, an inverse γcorrection circuit is configured by using a transistor having a back gate terminal of the same structure as the transistor 130 of the pixel cells.

[0308] Fig. 32 is an equivalent circuit diagram for explaining a basic concept of a signal processing system including the inverse γ correction circuit.

[0309] The inverse γ correction circuit 420 includes a transistor 421 having a back gate terminal, transistors 422 and 423 configuring a current mirror, a switch SW421, a capacitor C421, and current sources I421, I422, and I423.

[0310] A source of the transistor 421 and the current source I421 are connected. A connection point of the source of the transistor 421 and the current source I421 is connected to the switch SW401. A drain of the tran-

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sistor 421 is connected to a source of the transistor 422. A gate and a drain of the transistor 422 are connected. A connection point of the gate and the drain is connected to the current source I422, a gate of the transistor 423, and the switch SW421.

[0311] A drain of the transistor 423 is connected to power supply potential. A source of the transistor 423 is connected to a current source I423. Connection points of the source of the transistor 423 and the current source I423 are connected to the substrate of the transistor 421 and the capacitor 401. The capacitor C421 is connected to the switch SW421.

[0312] Since a timing chart of the signal processing system is the same as that shown in Fig. 32B, the timing chart is not shown in the figure.

[0313] The γ characteristic is reduced by the inverse γ correction circuit 420, i.e., non-linearity of the γ characteristic is changed to linearity to perform analog to digital conversion.

[0314] The signal processing system according to this embodiment has the characteristics described above.

[0315] In general column digital CDS or ADC, CDS or ADC is slowly performed in one H (horizontal) period. A signal memorized in an FD is assumed.

[0316] However, in the threshold modulation system, a signal change is caused by received light even during CDS or ADC. Therefore, when a high-speed electronic shutter is used with a large light amount, it is likely that a signal error and floating black occur.

[0317] In general, such a problem is prevented by high-speed analog CDS. In this system, it is conceivable to correct a black level taking into account shutter speed and a signal amount. Electronic shutter speed in a practical range is not considered to specifically cause a problem.

[0318] To prevent leak on a signal side that consumes sampling time, as described above, for example, analog sampling is performed only on the signal side. As a result, a significant improvement effect is obtained by adding one capacitor.

[0319] The pre-line reset system that makes use of a reset level of a preceding line can cope with reset of the column digital CDS.

[0320] Figs. 33A to 33C are diagrams of a level diagram of the pre-line reset system, two-column sharing, and 2x2 pixel timing. Fig. 33A is a diagram of an example of working voltage. Fig. 33B is a diagram of an example of a still image sequence in two column sharing. Fig. 33C is a diagram of an example of a 2x2 pixel addition sequence.

[0321] In this embodiment, for example, as shown in Fig. 34, pixel cells (transistors) are arranged in an array shape to obtain one output signal with plural pixels. This makes it possible to attain a high-Qs and low-noise dynamic range.

[0322] A method of obtaining one output signal may be performed in a solid-state imaging element or in a signal processing IC outside the element. When the method is performed in the signal processing IC outside the element, there is an advantage that, for example, a defective pixel can be corrected.

[0323] In this embodiment, for example, as shown in a plan view of Fig. 35 and a simplified sectional view of Fig. 36A, on condition that one output is finally obtained, element separation is performed in a unit of plural pixels to prepare for mixing of signals in plural pixels arranged in an array shape. Consequently, the sensor accumulation region is further expanded and a high dynamic range (D-Range) can be attained.

[0324] In this embodiment, for example, as shown in a simplified sectional view of Fig. 36B, if color filter coding is not the same color in plural pixels arranged in an array shape but, for example, primary colors B (Blue) and R (Red), a complementary color magenta is obtained. Therefore, complementary color signal processing used in a cam coder and the like can be used. As a result, color reproducibility is the same as that of the primary colors and improvement of mass productivity through sharing of color filter materials can be attained.

[0325] In this embodiment, for example, as shown in Fig. 37 and Figs. 38A and 38B, in a pixel that shares a part or a plurality of contacts of a drain, a source, a substrate (a well), or a gate with an adjacent pixel cell, when element separation is performed in a unit of plural pixels, since an element separation p-well under a reset drain can be eliminated, there is an effect that reset voltage can be reduced.

[0326] In the solid-state imaging device 1 according to this embodiment, it is possible to perform nondestructive readout without worsening of dark currents by continuing photoelectric conversion without resetting pixels in signal readout from pixels.

[0327] It is possible to realize, according to the nondestructive readout, for example, a high-S/N wide dynamic range (Wide D-Range) and live view during low-speed exposure and valve exposure.

[0328] It is also possible to realize, according to the nondestructive readout, various forms, for example, it is possible to perform still image low-speed exposure and asynchronous and synchronous simultaneous operations of a moving image, use for both AE and AF is possible, and it is possible to perform real-time AE/AF at random in an entire area through high-speed partial scan.

[0329] Fig. 39 is a diagram of an example of a wide dynamic range (Wide D-Range) sequence according to the nondestructive readout.

[0330] In Fig. 39, the vertical direction indicates a signal level and the horizontal direction indicates exposure time.

<Step ST1>

[0331] The signal level is reset and black scan is performed. A threshold Vh variation image is captured.

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<Step ST2>

[0332] At time t1, first intermediate scan (SCAN #1) is performed. A high-luminance image is captured and a Vth difference is obtained.

<Step ST3>

[0333] At time t2, second intermediate scan (SCAN #2) is performed. A medium-luminance image is captured and a Vth difference is obtained.

<Step ST4>

[0334] At time t3, final scan is performed to reset the signal level. A low-luminance image is captured (CDS).

[0335] Although not shown in the figure, as step ST5, a wide dynamic range is realized by image combination of the high-luminance image, the medium-luminance image, and the low-luminance image. (The respective images are multiplied by time ratios and combined by level to obtain a high-DR image.)

[0336] Fig. 40 is a diagram of an example of a low-speed live view sequence according to the nondestructive readout.

[0337] In Fig. 40, the vertical direction indicates a signal level and the horizontal direction indicates exposure time.

<Step ST11>

[0338] The signal level is reset and black scan is performed. A threshold Vh variation image is captured.

<Step ST12>

[0339] First intermediate scan (SCAN #1) is performed. #1 image is captured and a #0Vth difference is obtained and, for example, displayed for monitoring.

<Step ST13>

[0340] Second intermediate scan (SCAN #2) is performed. #2 image is captured and #1 Vth difference is obtained and, for example, displayed for monitoring.

<Step ST14>

[0341] Final scan is performed. #n image is captured and #n Vth difference is obtained and, for example, displayed for monitoring.

<Step ST15>

[0342] Capturing scan is performed to reset the signal level. Final image capturing CDS and recording in a memory are performed.

<Step ST16>

[0343] In the case of an asynchronous type, the image capture in step ST15 (a still image) is displayed in terms of 1/30s.

[0344] In this way, it is possible to realize, according to the nondestructive readout, for example, a high-S/N wide dynamic range (Wide D-Range) and live view during low-speed exposure and valve exposure.

[0345] As explained above, according to this embodiment, the substrate 100 includes the first substrate surface 101 side on which light is irradiated and the second substrate surface 102 side on which elements are formed. The plural pixel cells Cel (2A) separated by the adjacent cell group and the element separation layer are formed. Each of the pixel cells Cel includes the first conductive (in this embodiment, n-type) well (the first well) 110 formed on the first substrate surface 101 side and the second conductive (p-type) well (the second well) 120 formed further on the second substrate surface 102 side than the first well 110. The n-type first well 110 functions as a light sensing section that receives light from the first substrate surface 101 side and has the photoelectric conversion function and the charge accumulation function for the received light. The MOS transistor 130 that detects accumulated charges in the light sensing section of the first well 110 and has the threshold modulation function is formed in the second well 120. The p-type element separation layer (conductive layer) 140 of the second conductive type opposite to the first conductive type (in this embodiment, n-type) is formed on the sidewalls of the first well 110 and the second well 120 to surround the sidewalls. Therefore, effects described below can be obtained.

[0346] A pixel can be formed by one transistor of the drain (D)/gate (G)/source (S) structure. An increase in the number of steps can be minimized because the pixel structure is compatible with a logic process.

[0347] Layout efficiency is high and a micro-pixel can be realized because the contacts of the drain, the source, the gate, and the well can be shared.

[0348] Since a gate area is large, transistor noise is extremely small.

[0349] Since the entire pixel is an accumulation region, a saturation signal amount is large and a high dynamic range (DR) can be realized.

[0350] Since dark currents generated from the interface are discharged to the drain, a dark current image defect in the interface does not occur.

[0351] It is possible to perform nondestructive readout in which dark currents do not worsen regardless of ON or OFF of the gate.

[0352] The entire light sensing section is the gate. When the reflector is mounted, near infrared high sensitivity and an ultra-fine pixel can be realized.

[0353] Noise can be reduced by the inverse γ correction function.

[0354] The solid-state imaging device having the char-

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acteristics described above can be applied as imaging devices of a digital camera and a video camera.

[0355] Fig. 41 is a diagram of an example of a configuration of a camera system to which the solid-state imaging device according to this embodiment is applied.

[0356] This camera system 500 includes, as shown in Fig. 41, an imaging device 510 to which the solid-state imaging device 1 according to this embodiment can be applied, an optical system that guides incident light to a pixel region of the imaging device 510 (focuses a subject image), for example, a lens 520 that focuses incident light (image light) on an imaging surface, a driving circuit (DRV) 530 that drives the imaging device 510, and a signal processing circuit (PRC) 540 that processes an output signal of the imaging device 510.

[0357] The driving circuit 503 includes a timing generator (not shown) that generates various timing signals including a start pulse and a clock pulse for driving circuits in the imaging device 510. The driving circuit 530 drives the imaging device 510 with a predetermined timing signal.

[0358] The signal processing circuit 540 applies signal processing such as CDS (Correlated Double Sampling) to an output signal of the imaging device 510.

[0359] An image signal processed by the signal processing circuit 540 is recorded in a recording medium such as a memory. The image signal recorded in the recording medium is hard-copied by a printer or the like. The image signal processed by the signal processing circuit 540 is displayed as a moving image on a monitor including a liquid crystal display.

[0360] As described above, in imaging apparatuses and electronic apparatuses such as a digital camera, a monitoring camera, a camera mounted on a cellular phone, a single lens reflex camera, and a scanner, it is possible to realize a highly accurate camera by mounting the solid-state imaging device 1 as the imaging device 510.

[0361] The present invention is not limited by the explanation of the embodiment.

[0362] For example, the numerical values and the materials described in the embodiment are only examples. The present invention is not limited to the numerical values and the materials.

[0363] Besides, various alterations are possible without departing from the spirit of the present invention.

[0364] It should be understood by those skilled in the art that various modifications, combinations, sub-combinations, and alterations may occur depending on design requirements and other factors insofar as they are within the scope of the appended claims or the equivalents thereof.

Claims

1. A solid-state imaging device comprising pixel cells that are formed on a substrate having a first substrate surface side, on which light is irradiated, and a second substrate surface side, on which elements are formed, and separated by an adjacent cell group and an element separation layer for each of the pixel cells or with plural pixel cells as a unit, wherein
each of the pixel cells includes:

a first conductive well formed on the first substrate surface side; and
a second conductive well formed on the second substrate surface side,
the first conductive well receives light from the first substrate surface side and has a photoelectric conversion function and a charge accumulation function for the received light, and
a transistor that detects accumulated charges in the first conductive well and has a threshold modulation function is formed in the second conductive well.

2. A solid-state imaging device according to claim 1, wherein the accumulated charges and signal charges are identical carriers.

3. A solid-state imaging device according to claim 1 or 2, wherein the transistor has a function of a readout transistor, a function of a reset transistor, and a function of a selection transistor.

4. A solid-state imaging device according to claims 1 to 3, wherein the pixel cell has a gamma characteristic that a modulation degree increases when illuminance is low.

5. A solid-state imaging device according to claim 4, wherein the pixel cell has the structure in which a capacity increases during a large signal output and has a function of realizing a high dynamic range according to the gamma characteristic.

6. A solid-state imaging device according to claims 1 to 5, wherein a second conductive separation layer is formed at least on a side of the first conductive well of the first conductive well and the second conductive well.

7. A solid-state imaging device according to claim 6, wherein
a first conductive source region and a first conductive drain region are formed in the second conductive well or the second conductive separation layer, and
a gate electrode is formed on a channel formation region in the second conductive well between the source region and the drain on the second substrate surface side of the substrate.

8. A solid-state imaging device according to claim 7, wherein a plurality of the pixel cells are arranged in

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an array form and share, with adjacent pixel cells, a part or a plurality of contacts of the drain, the source, the wells, or the gate.

9. A solid-state imaging device according to claim 7, wherein
a plurality of the pixel cells are arranged in an array form,
a gate electrode of the pixel cells are formed in common to the pixel cells in a stripe shape in one direction of the pixel array, and
a well contact is formed on the source region side or the drain region side.

10. A solid-state imaging device according to claim 9, wherein a well contact region is formed in the second conductive separation layer.

11. A solid-state imaging device according to claim 10, wherein the well contact region is formed in the second conductive separation layer on the first substrate surface side.

12. A solid-state imaging device according to claims 9 to 11, wherein, when the well contact is formed on the drain side, the well contact is formed in a pinch shape with drain width reduced.

13. A solid-state imaging device according to claims 1 to 12, wherein, in the arrangement of the pixel cells in the array form, the drain contacts are divided into two or more groups in a column and share a column circuit of a signal readout processing system.

14. A solid-state imaging device according to claim 3, wherein the solid-state imaging device has, in the gate electrode of the transistor on the second substrate surface side or a further front section of the gate electrode, a reflector that reflects light transmitted through the substrate and makes the light incident on the second conductive well and the first conductive well of the substrate.

15. A camera comprising:

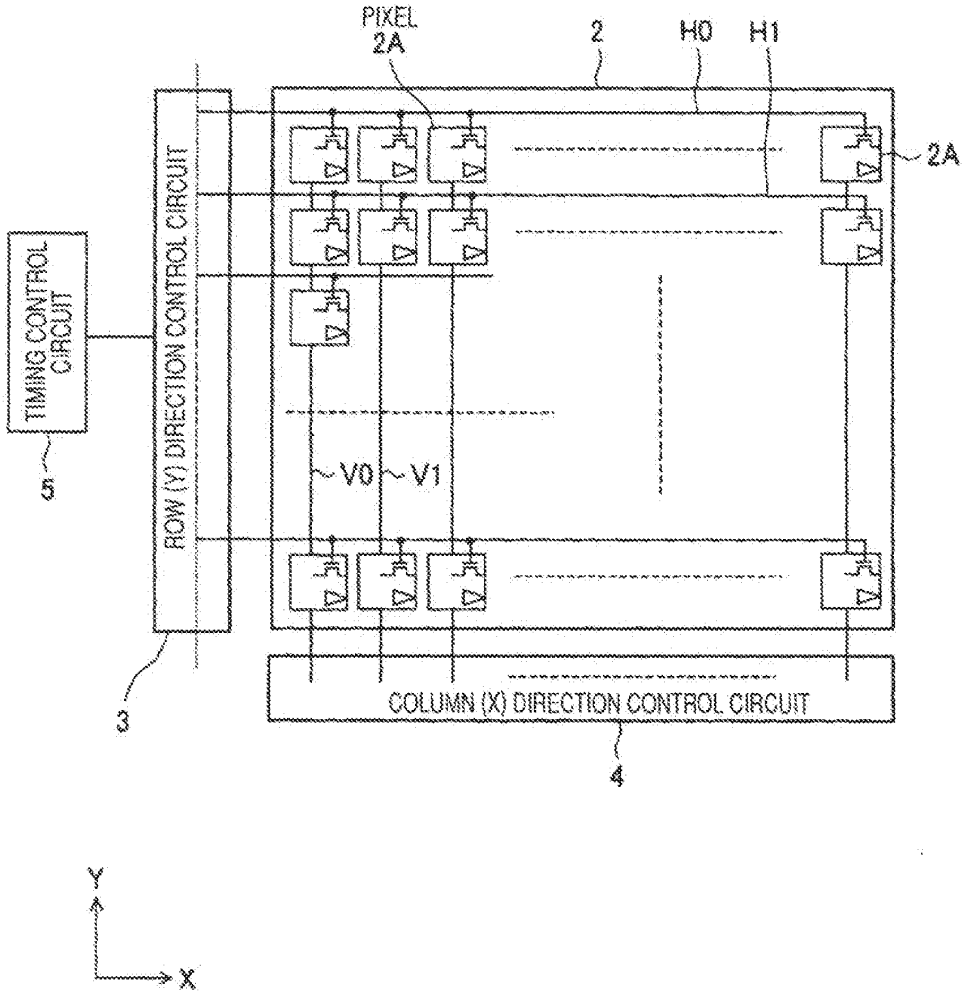
a solid-state imaging device that receives light from a first substrate surface side of a substrate;
an optical system that guides incident light to the first substrate surface side of the solid-state imaging device; and
a signal processing circuit that processes an output signal of the solid-state imaging device,
wherein
the solid-state imaging device includes pixel cells that are formed on the substrate having the first substrate surface side, on which light is irradiated, and a second substrate surface side, on which elements are formed, and separated by an adjacent cell group and an element separation layer for each of the pixel cells or with plural pixel cells as a unit,
each of the pixel cells includes:

a first conductive well formed on the first substrate surface side; and
a second conductive well formed on the second substrate surface side,
the first conductive well receives light from the first substrate surface side and has a photoelectric conversion function and a charge accumulation function for the received light, and
a transistor that detects accumulated charges in the first conductive well and has a threshold modulation function is formed in the second conductive well.

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FIG. 1



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FIG. 2A

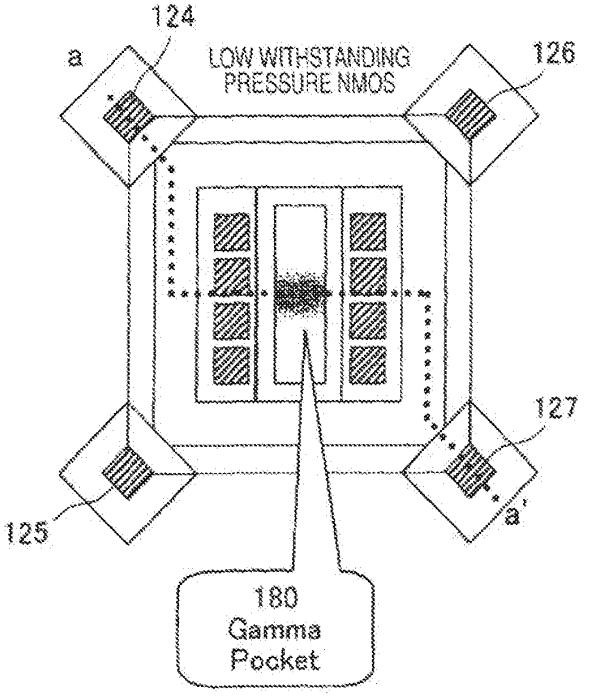
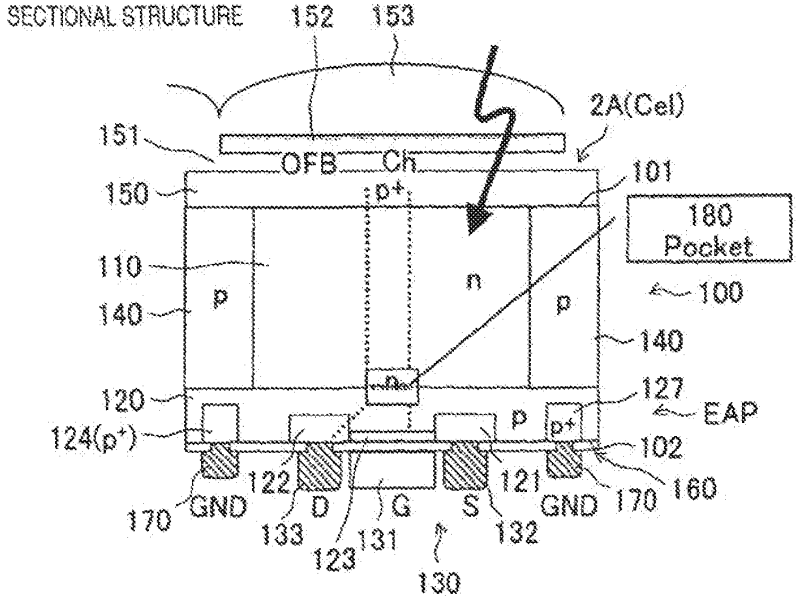


FIG. 2B



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FIG. 3

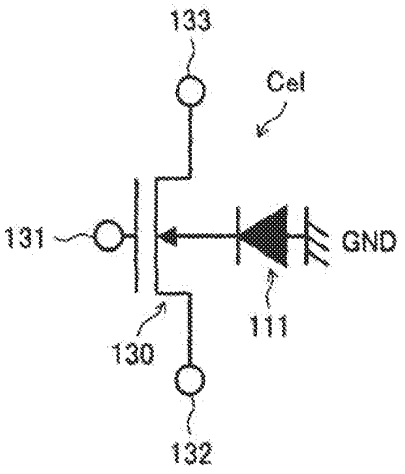
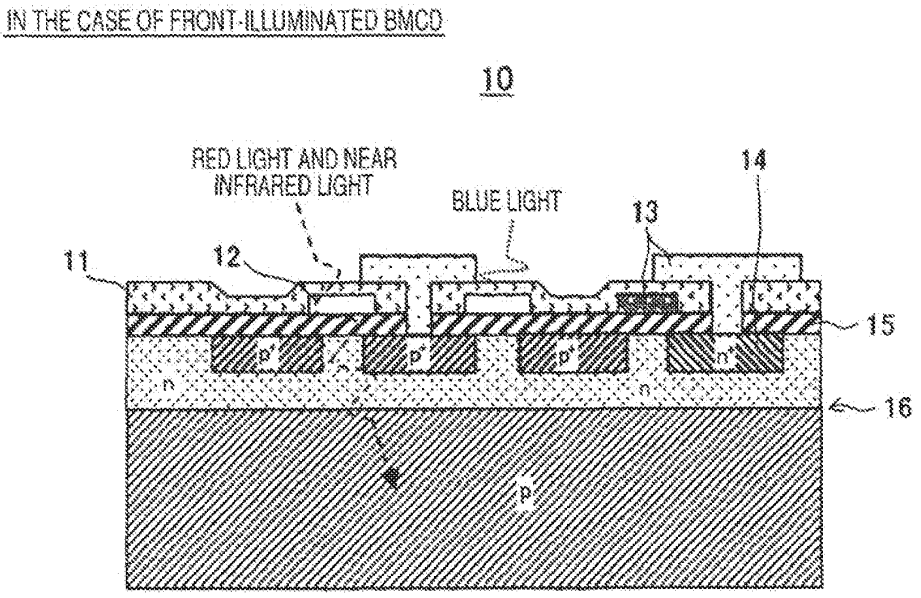


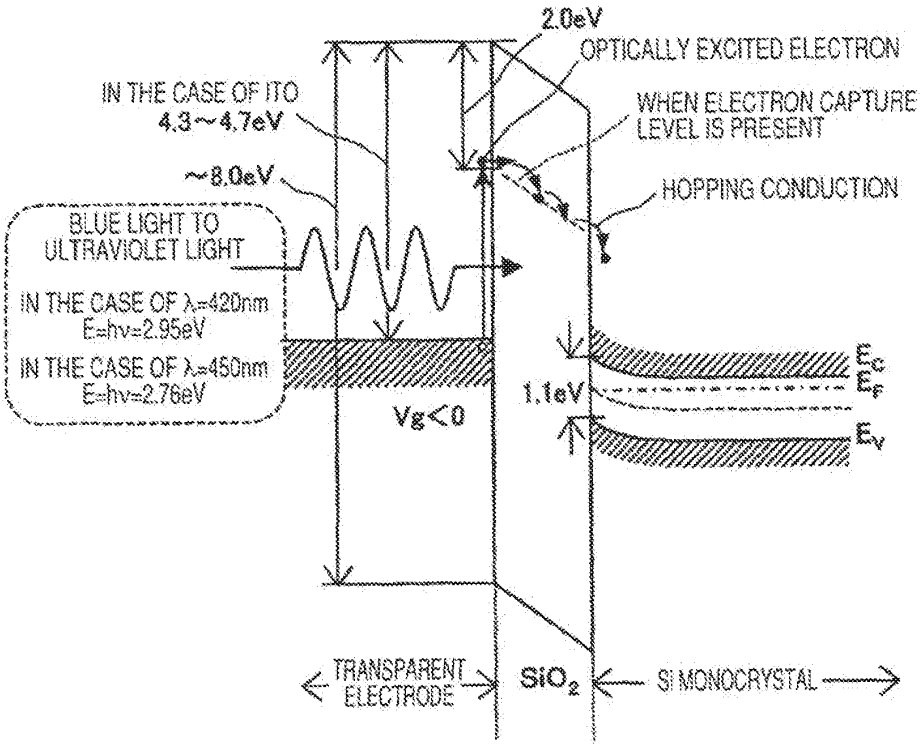
FIG. 4



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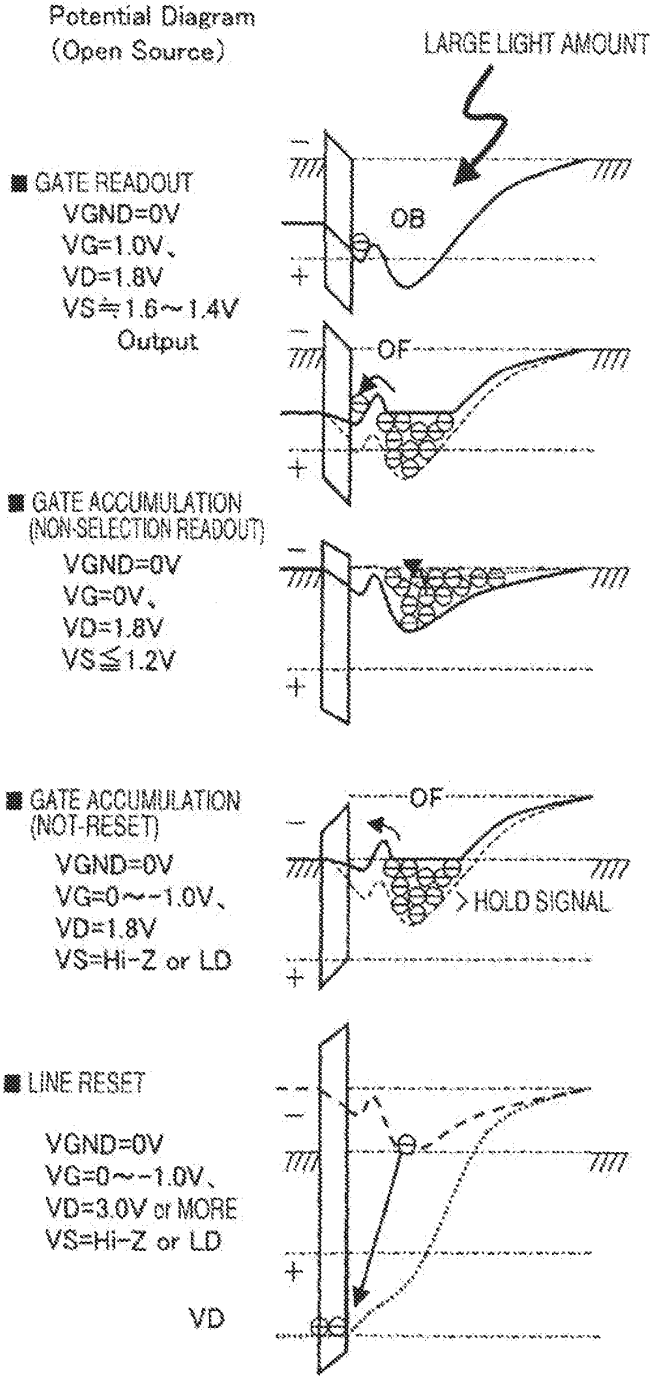
FIG. 5



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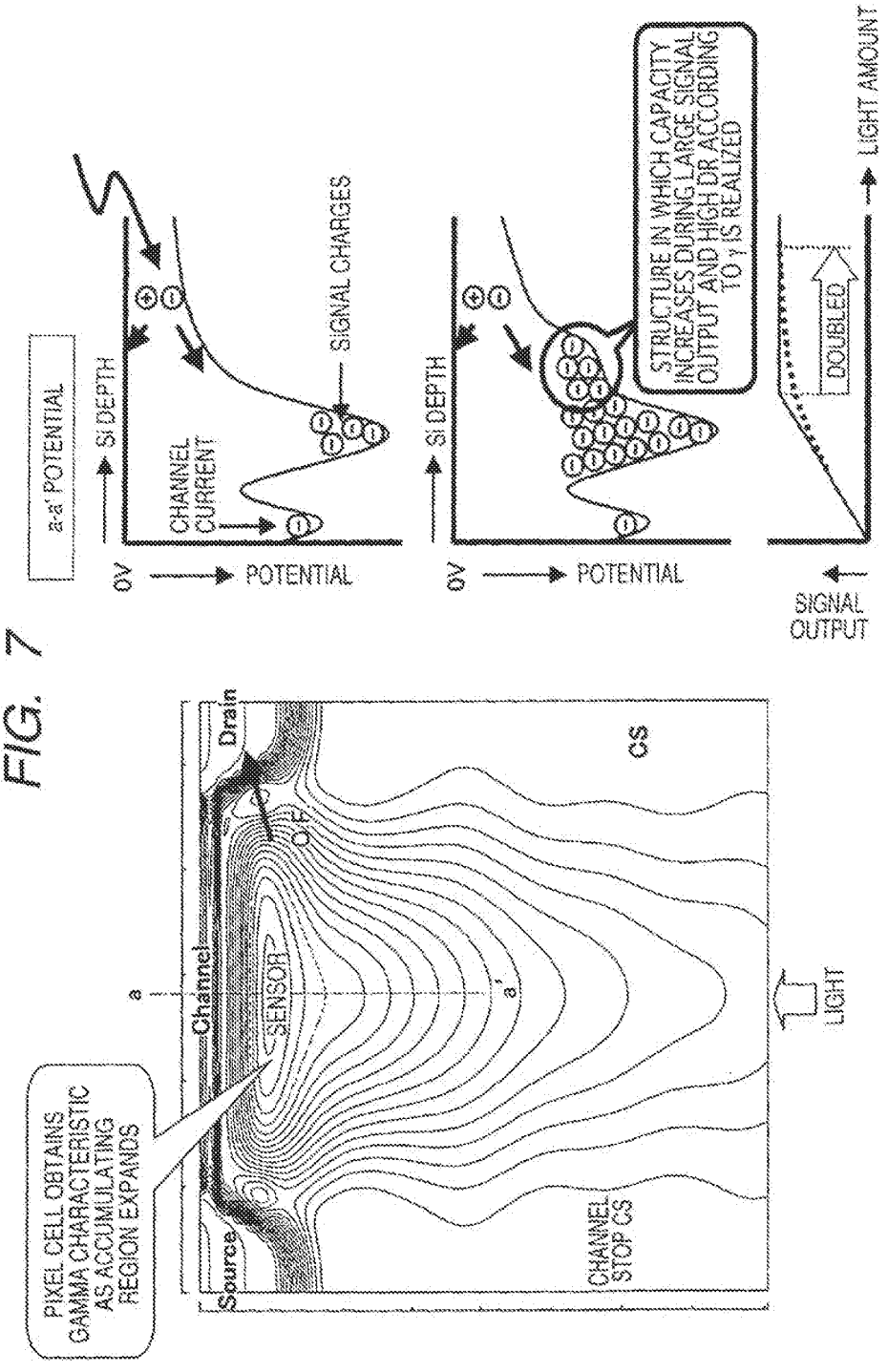
FIG. 6



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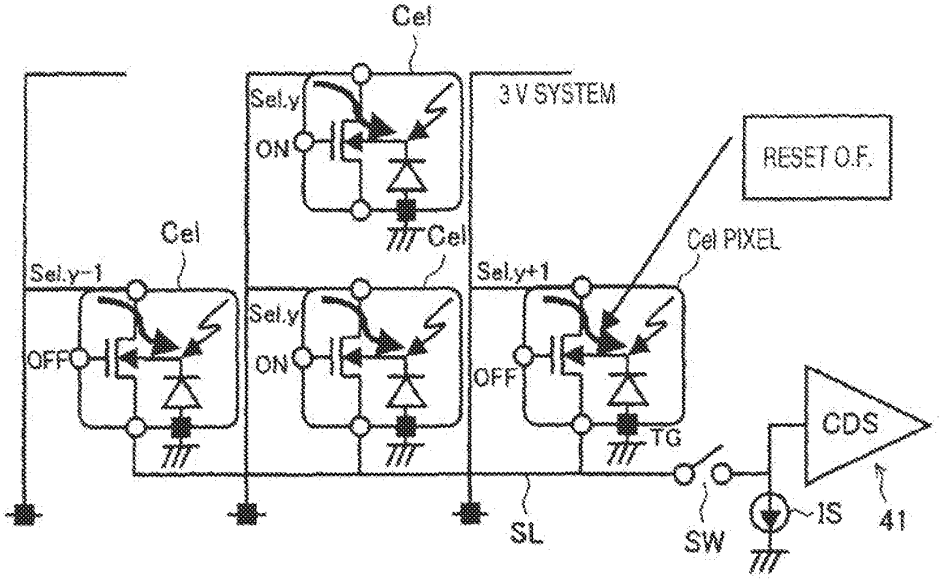
FIG. 7



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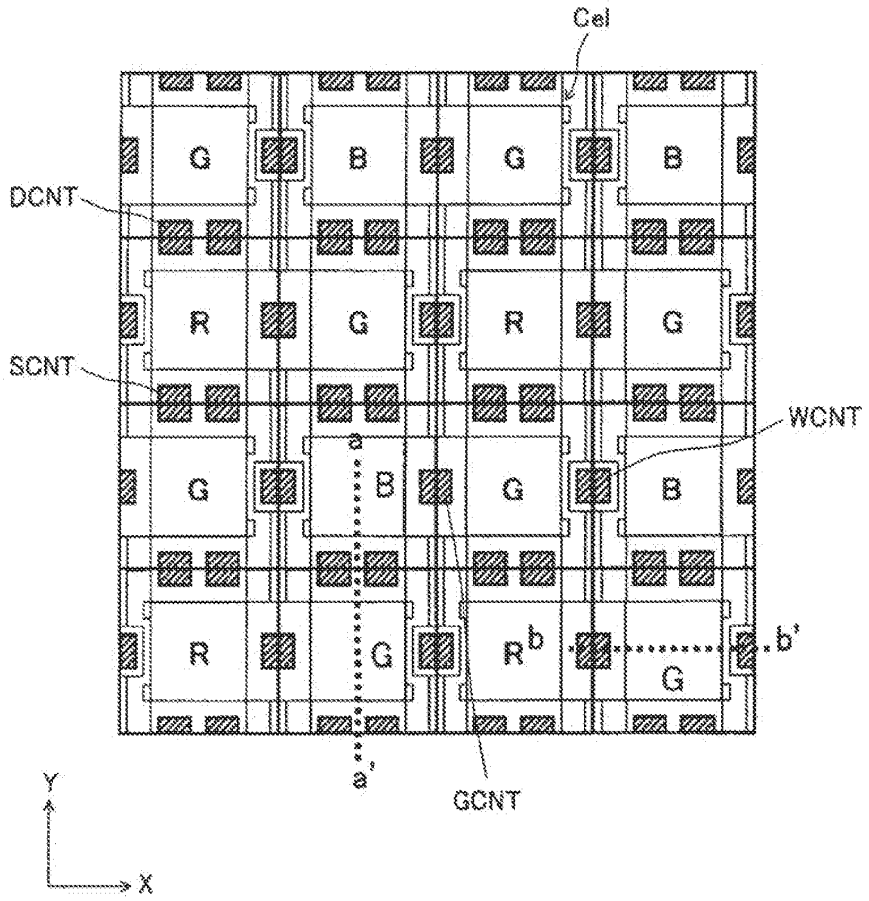
FIG. 8



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FIG. 9



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FIG. 10A

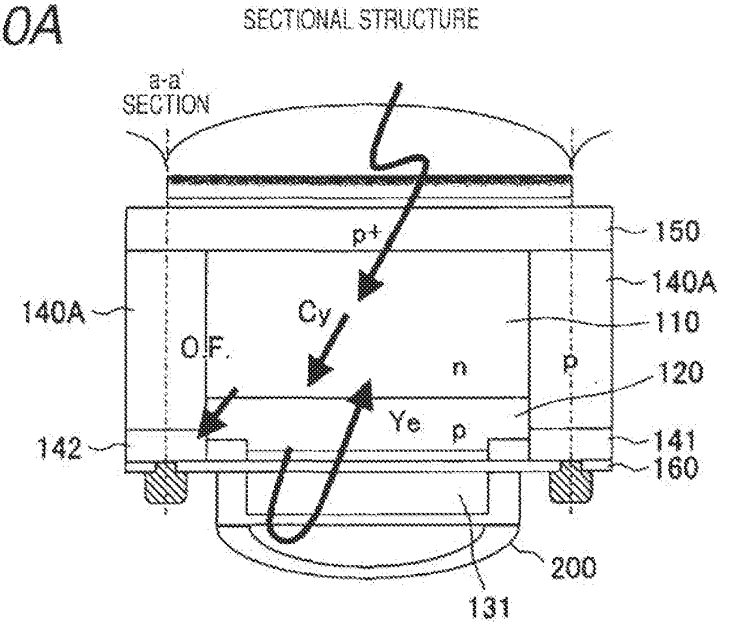
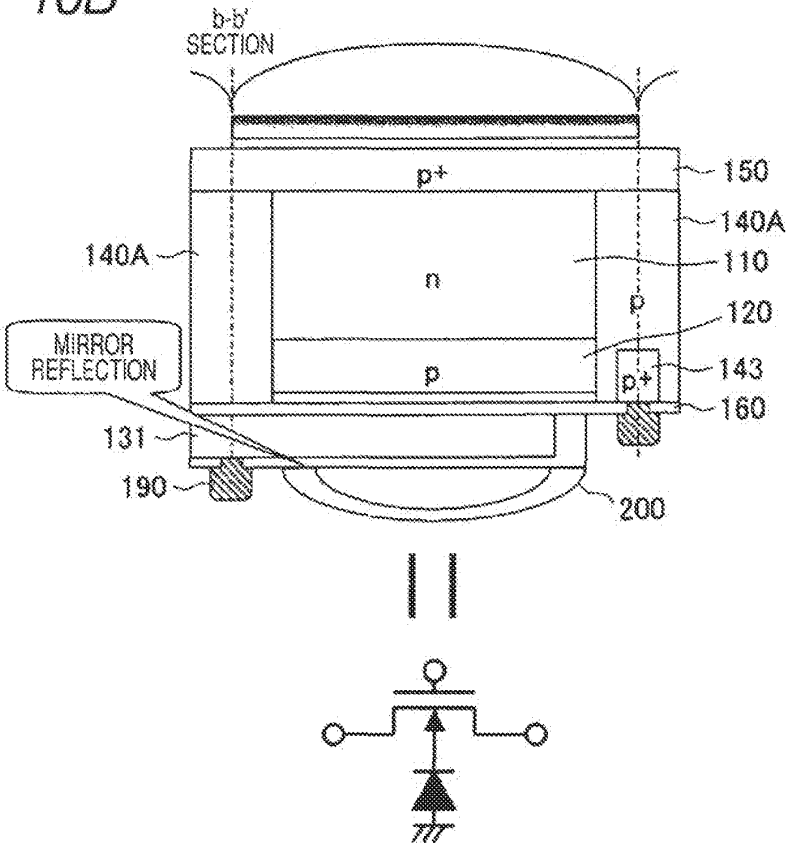


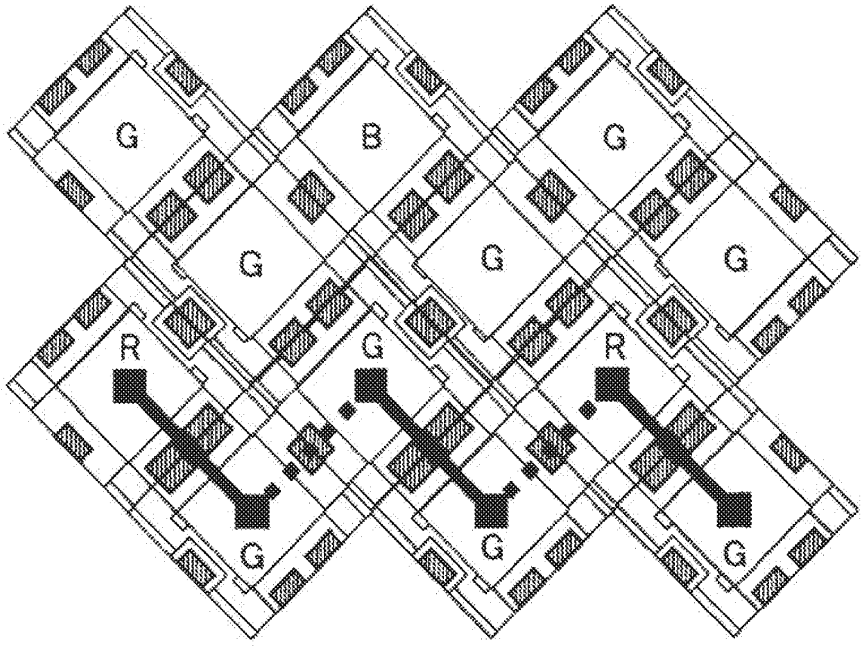
FIG. 10B



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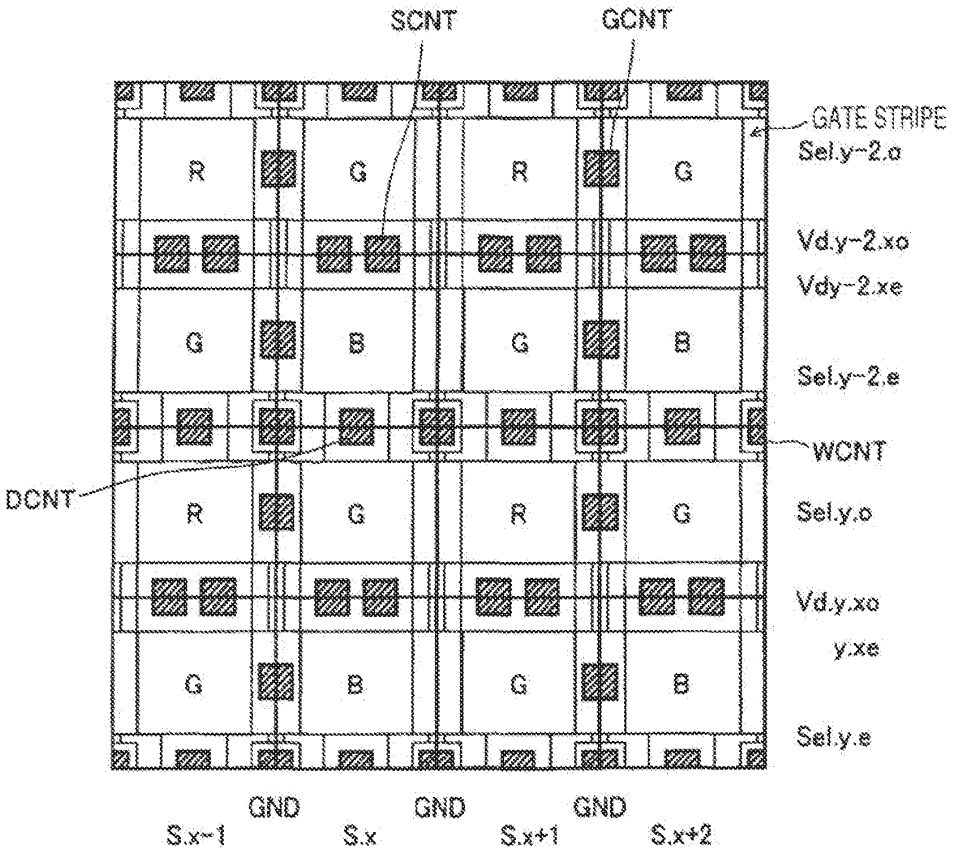
FIG. 11



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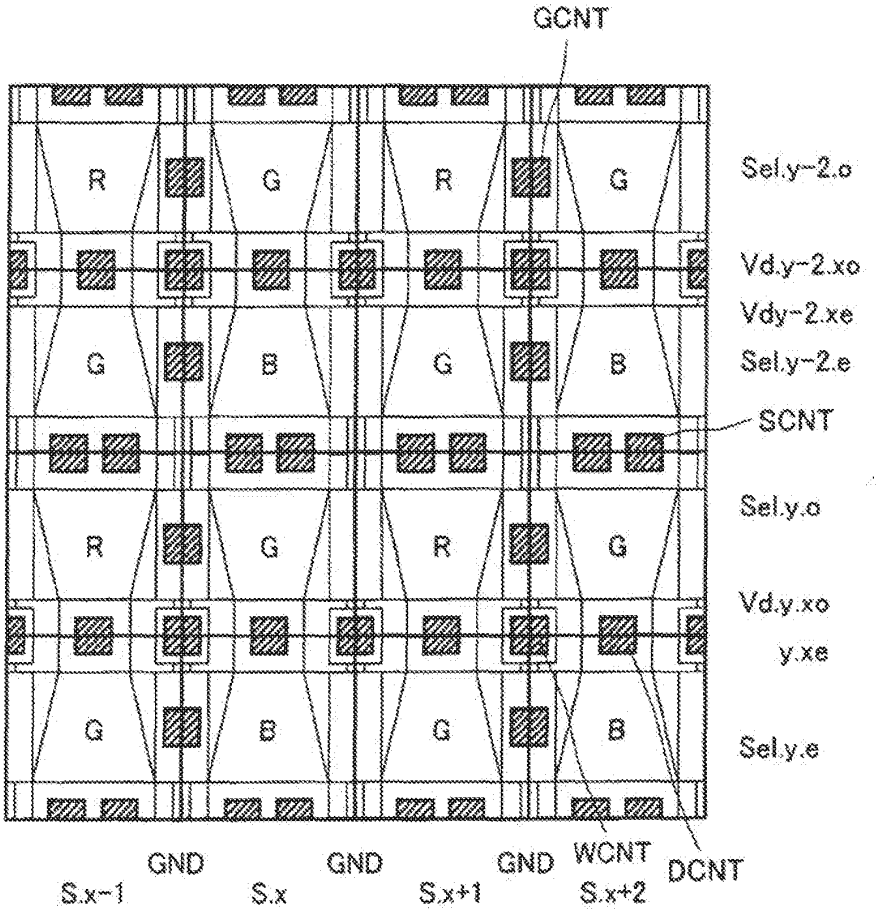
FIG. 12



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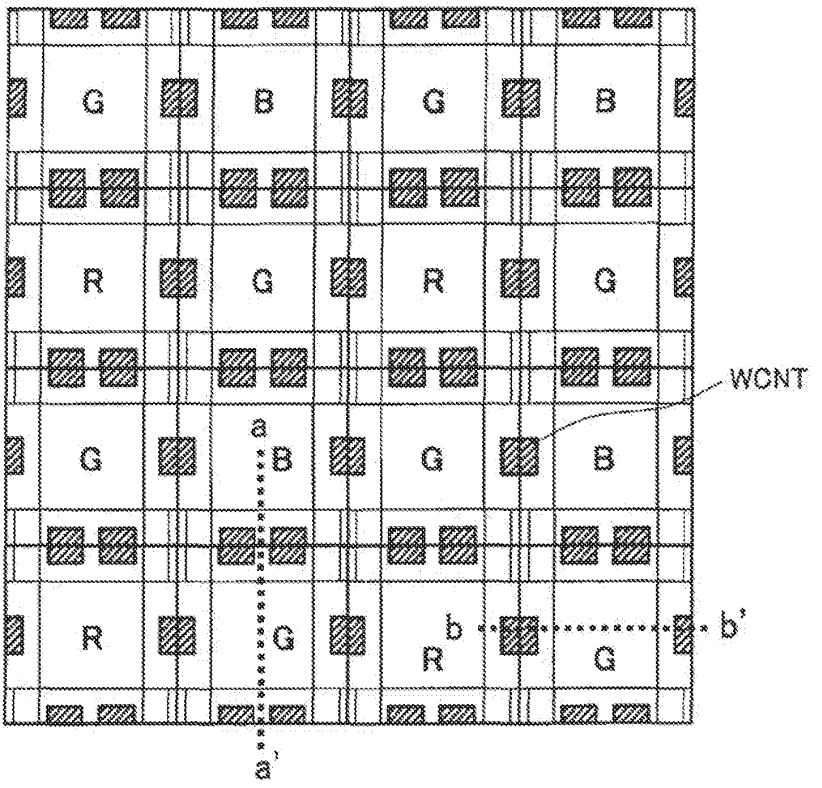
FIG. 13



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FIG. 14



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FIG. 15A

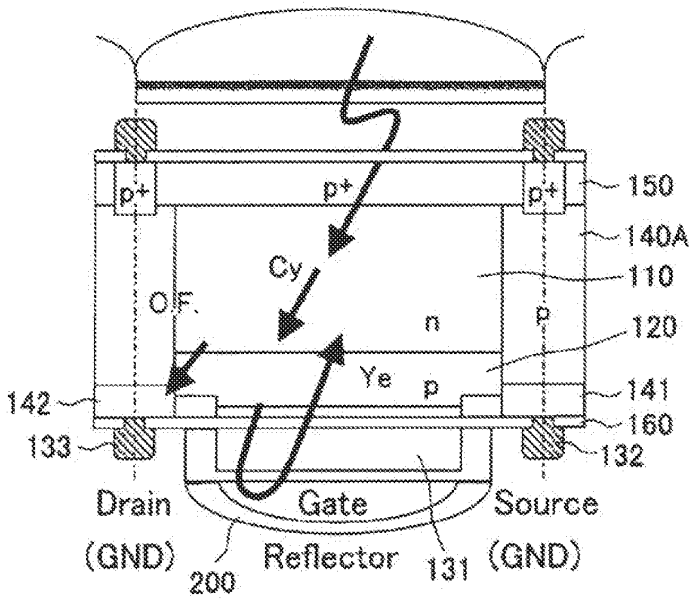
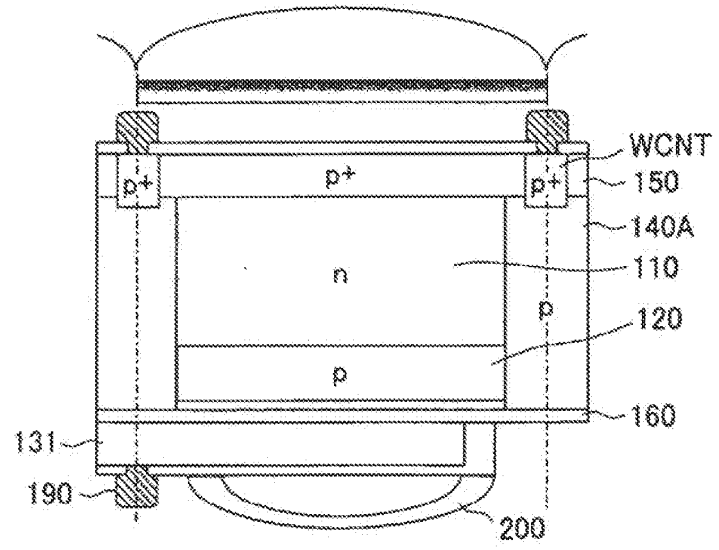


FIG. 15B



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FIG. 16B

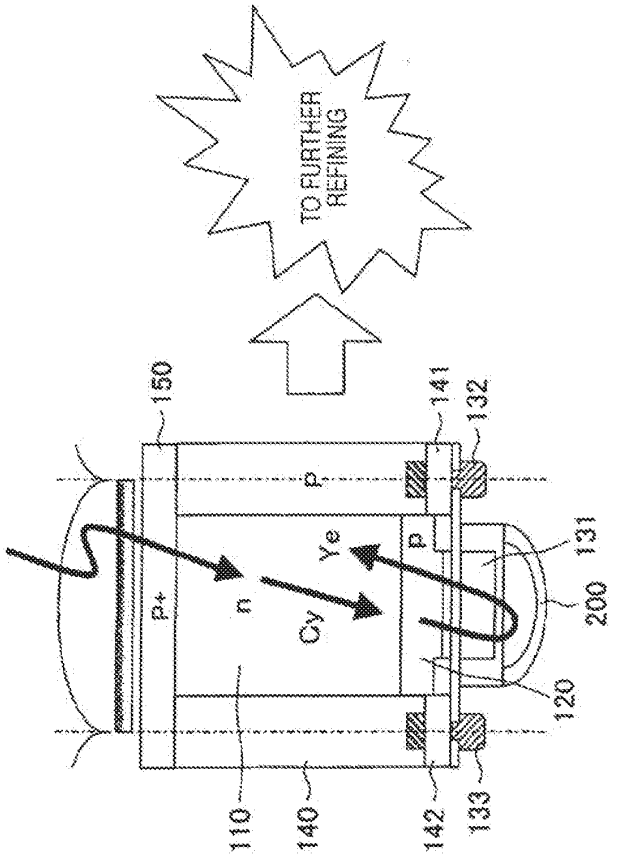
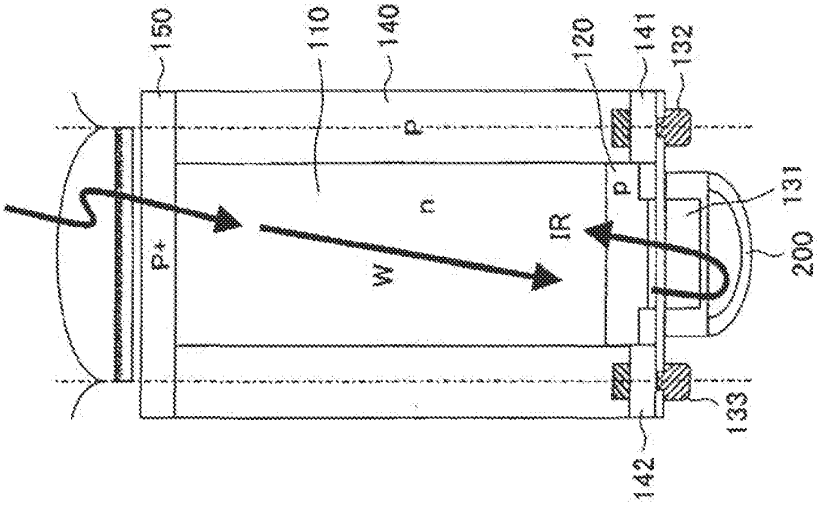


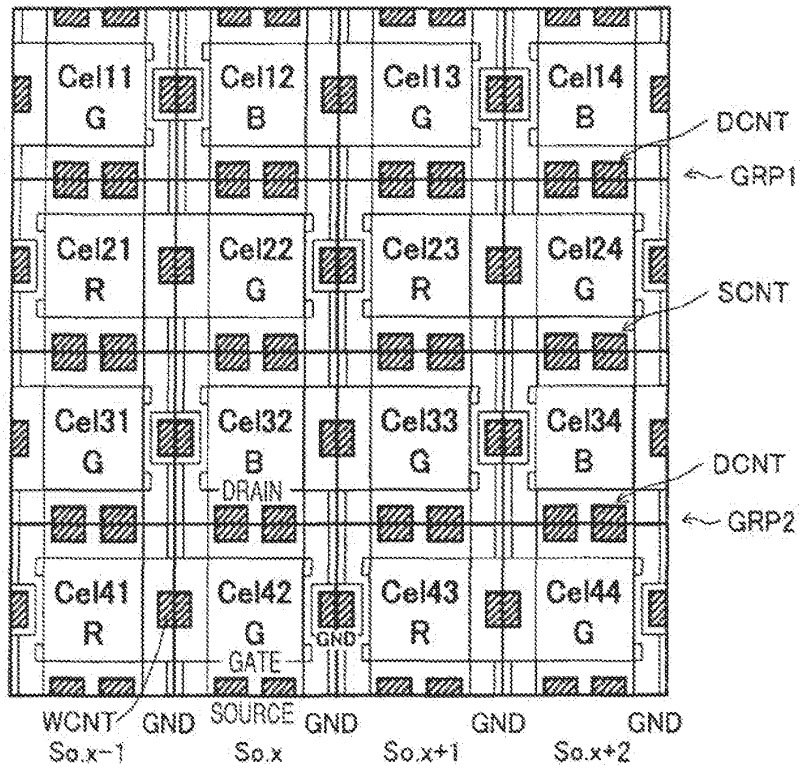
FIG. 16A



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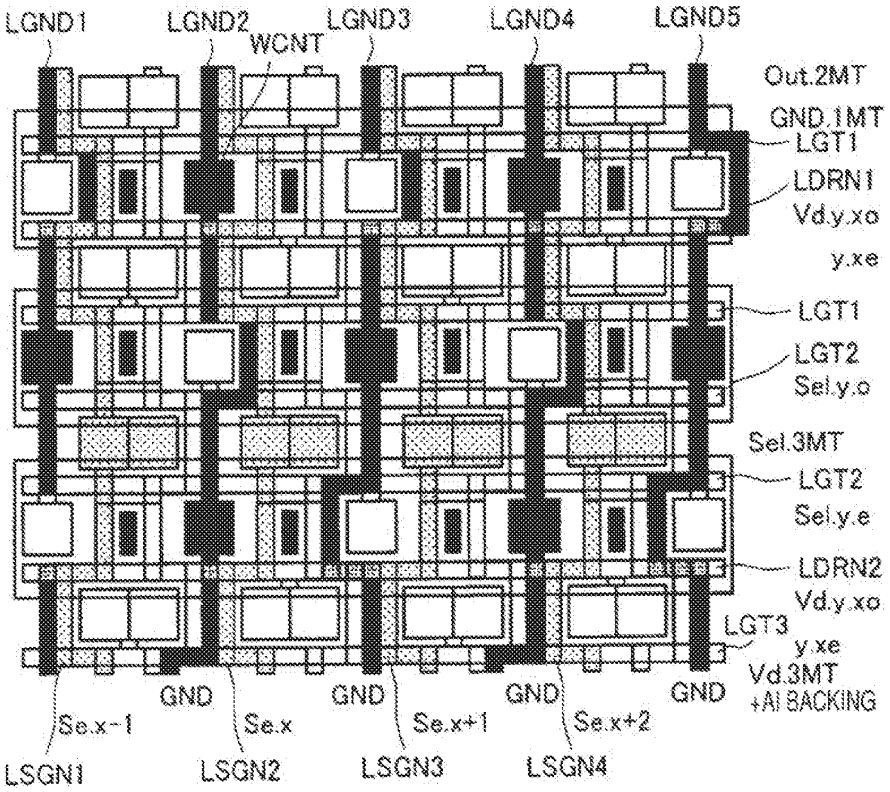
FIG. 17A



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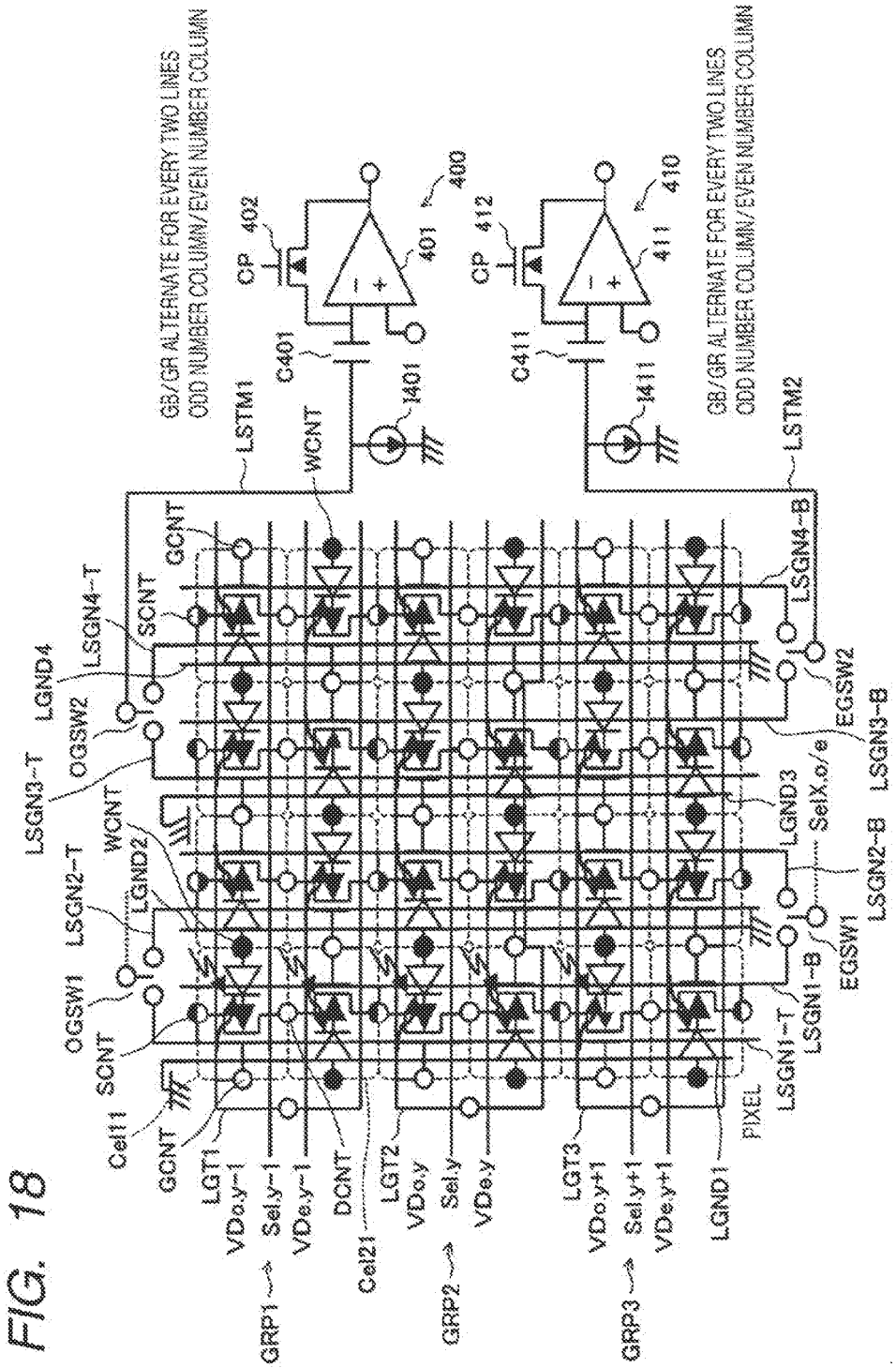
FIG. 17B



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FIG. 18



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FIG. 19A

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FIG. 19B

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FIG. 20A

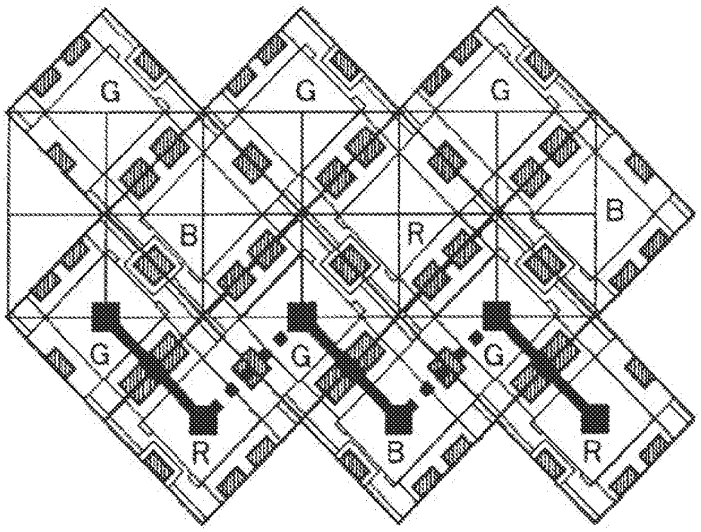
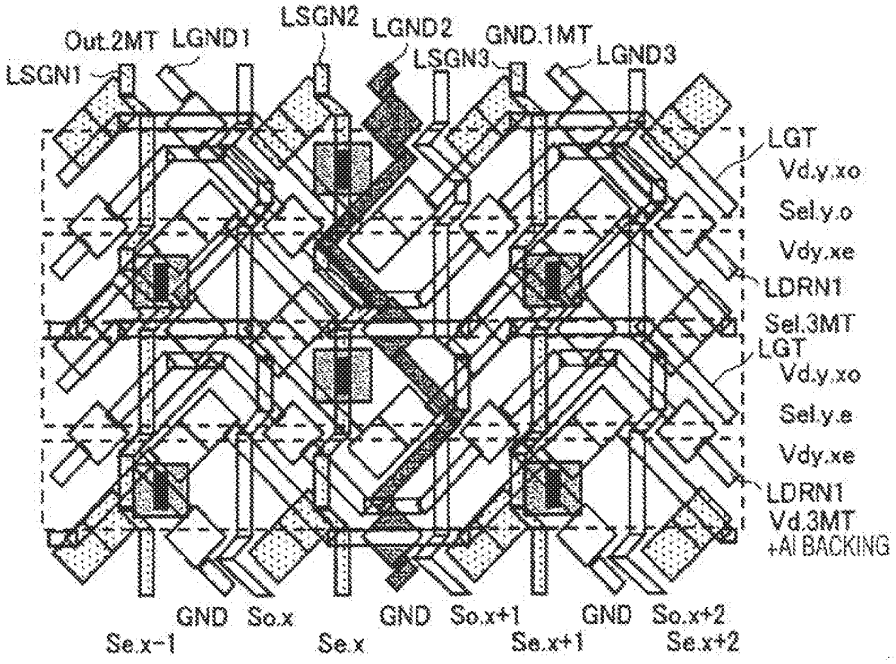


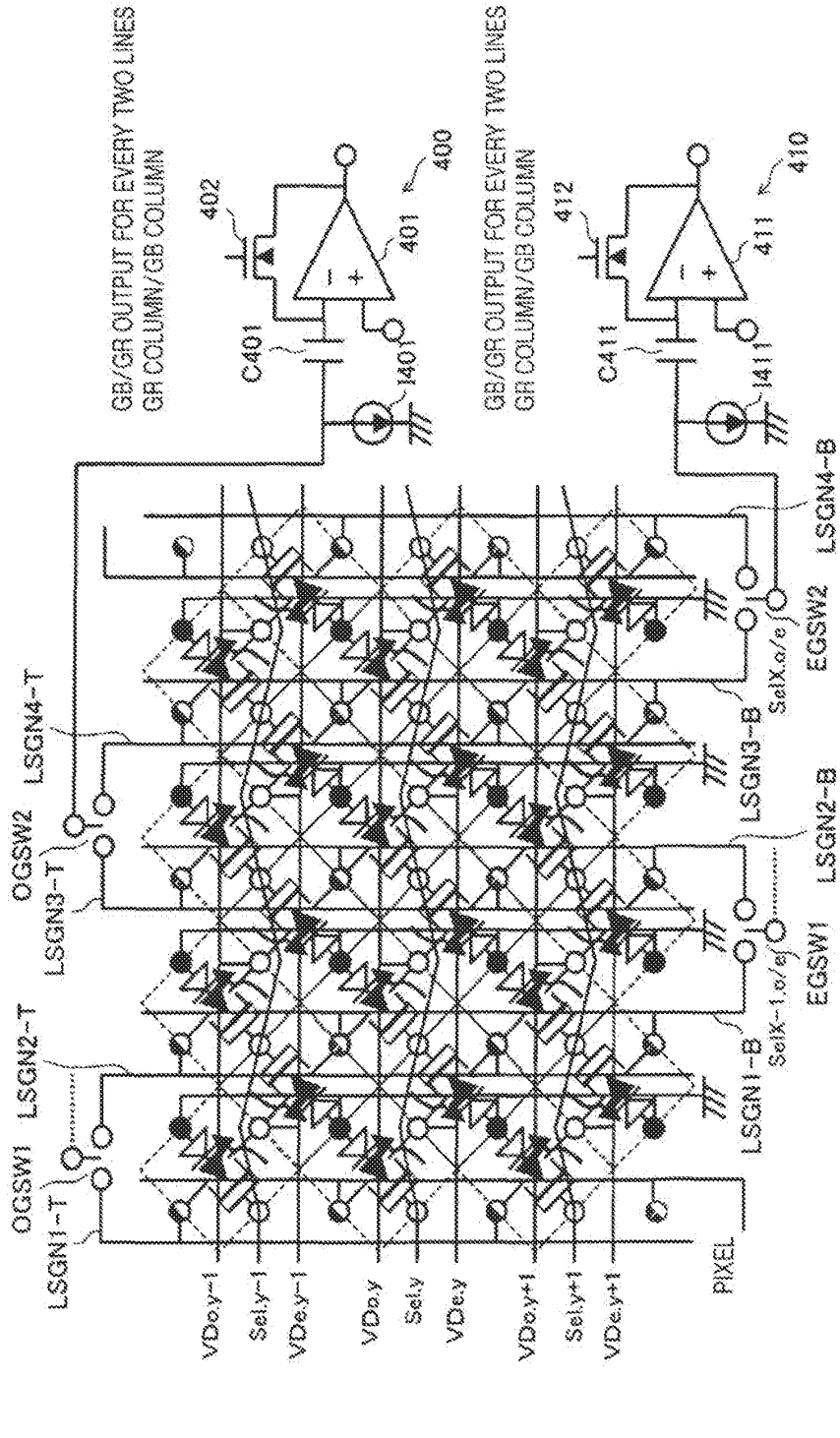
FIG. 20B



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FIG. 21



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FIG. 22A

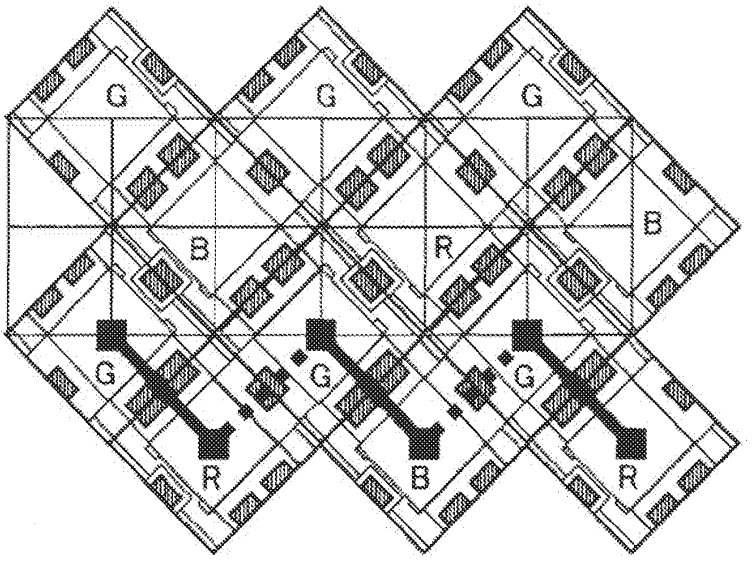
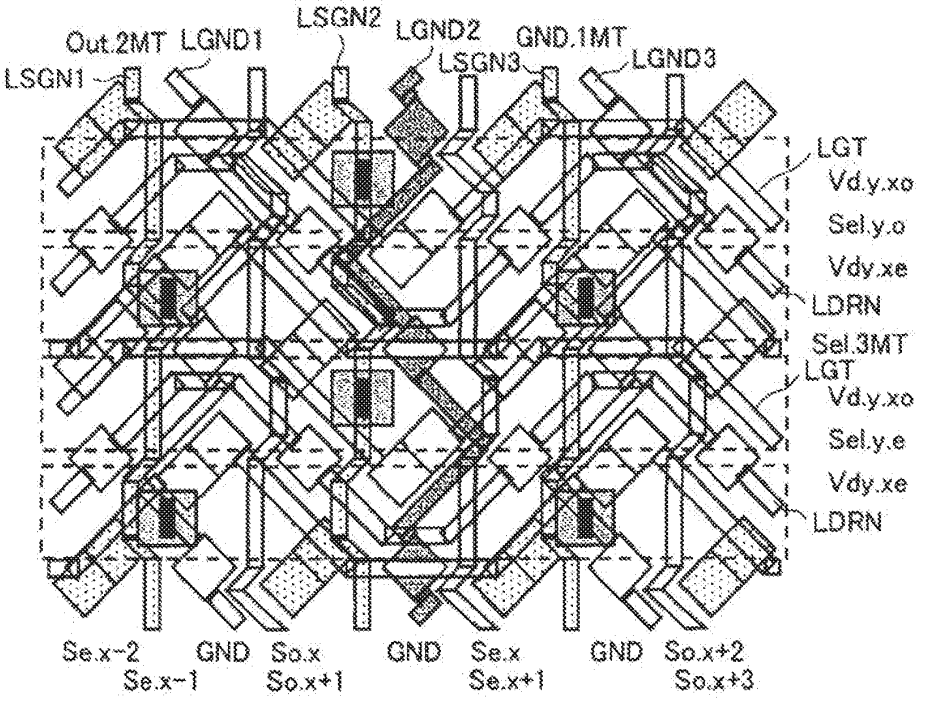


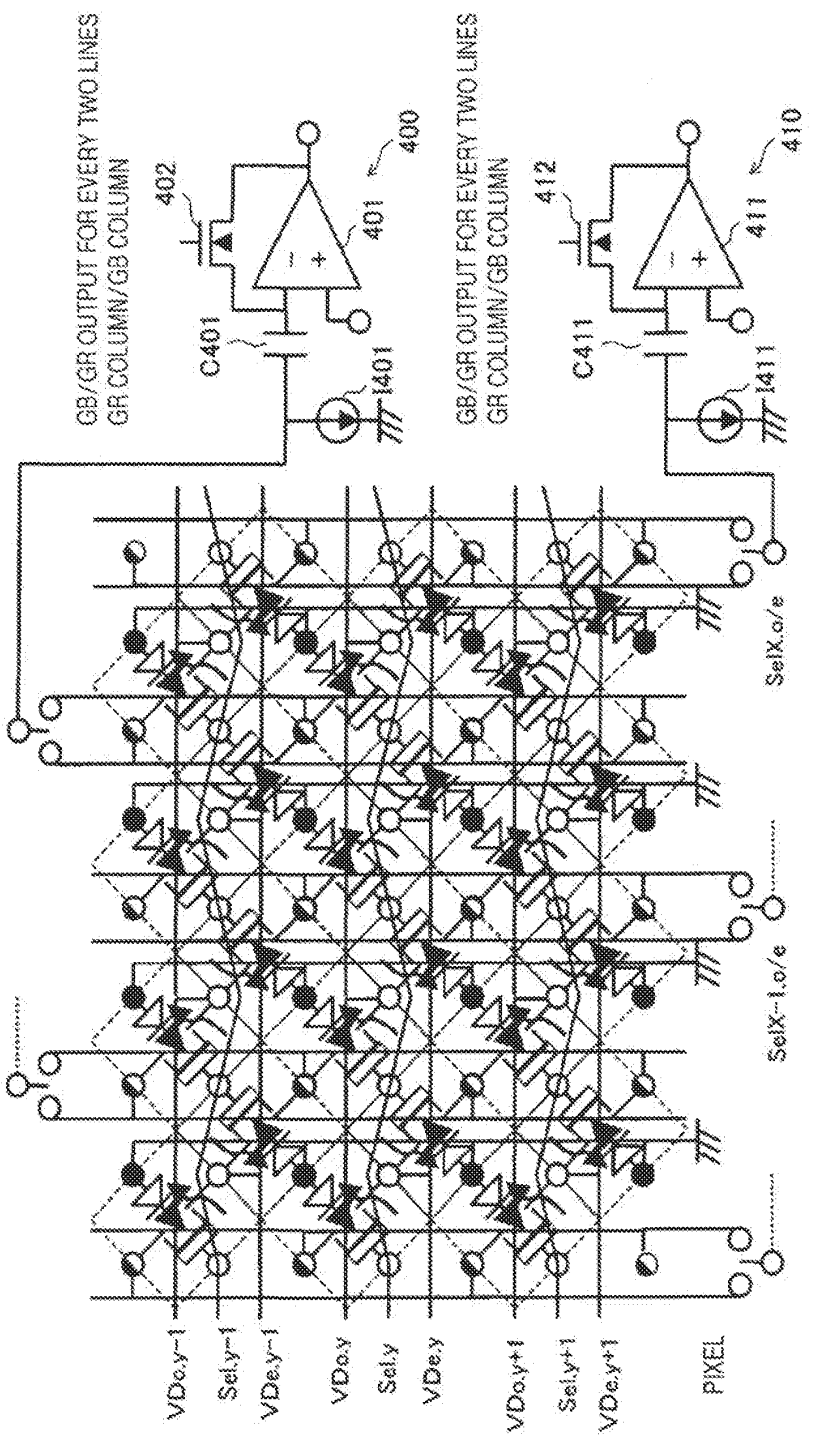
FIG. 22B



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FIG. 23



SIONYX1403000025.0108

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FIG. 24A

SIGNAL WIRING #1

SIONYX1403000025.0109

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FIG. 24B

SIGNAL WIRING #1

SIONYX1403000025.0110

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FIG. 25A

SIGNAL WIRING #2

SIONYX1403000025.0111

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FIG. 25B

SIGNAL WIRING #2

SIONYX1403000025.0112

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FIG. 26A

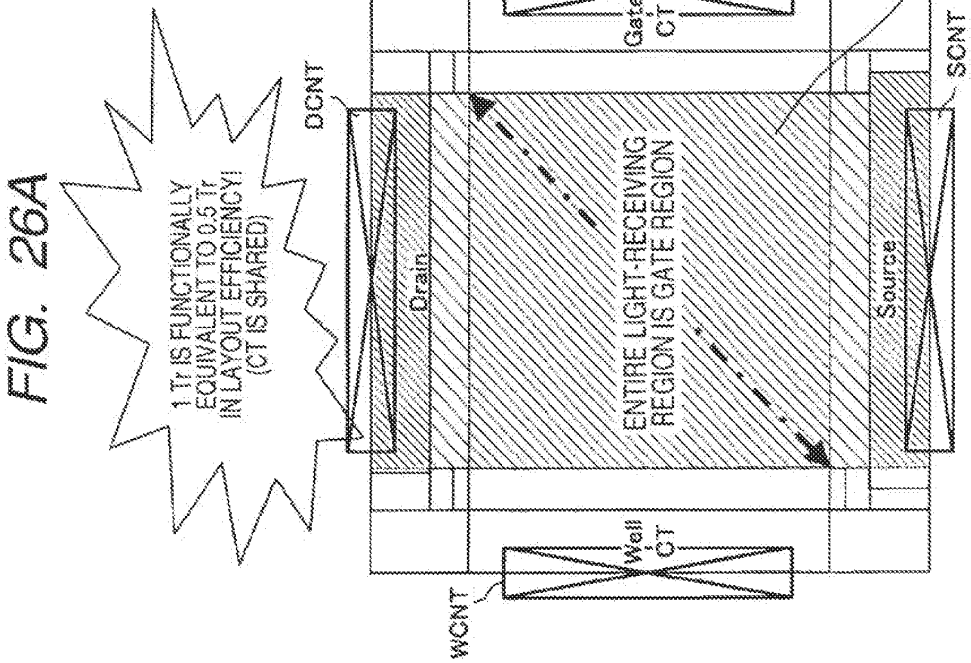
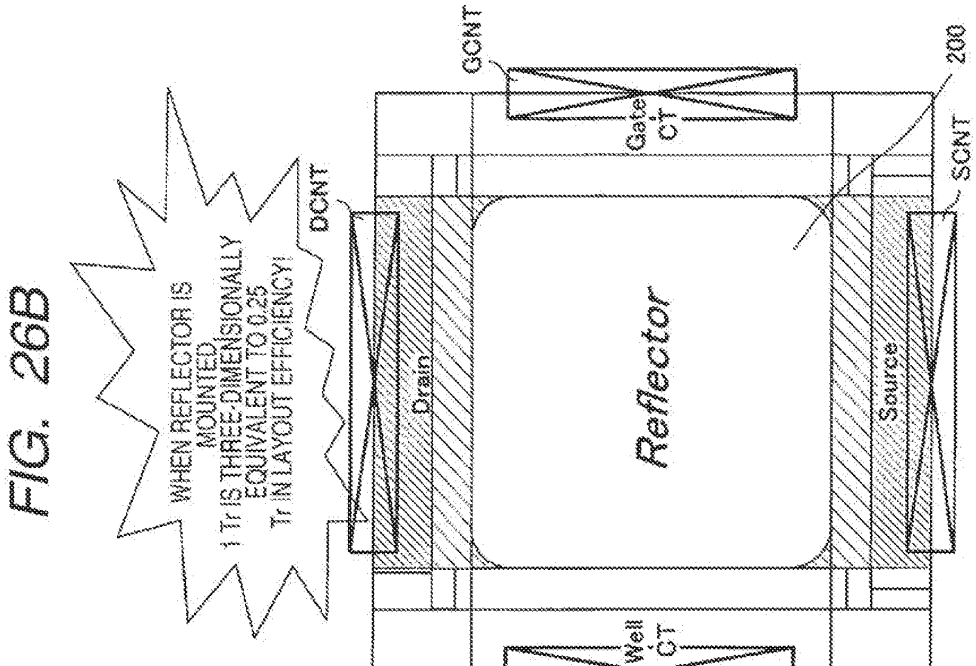


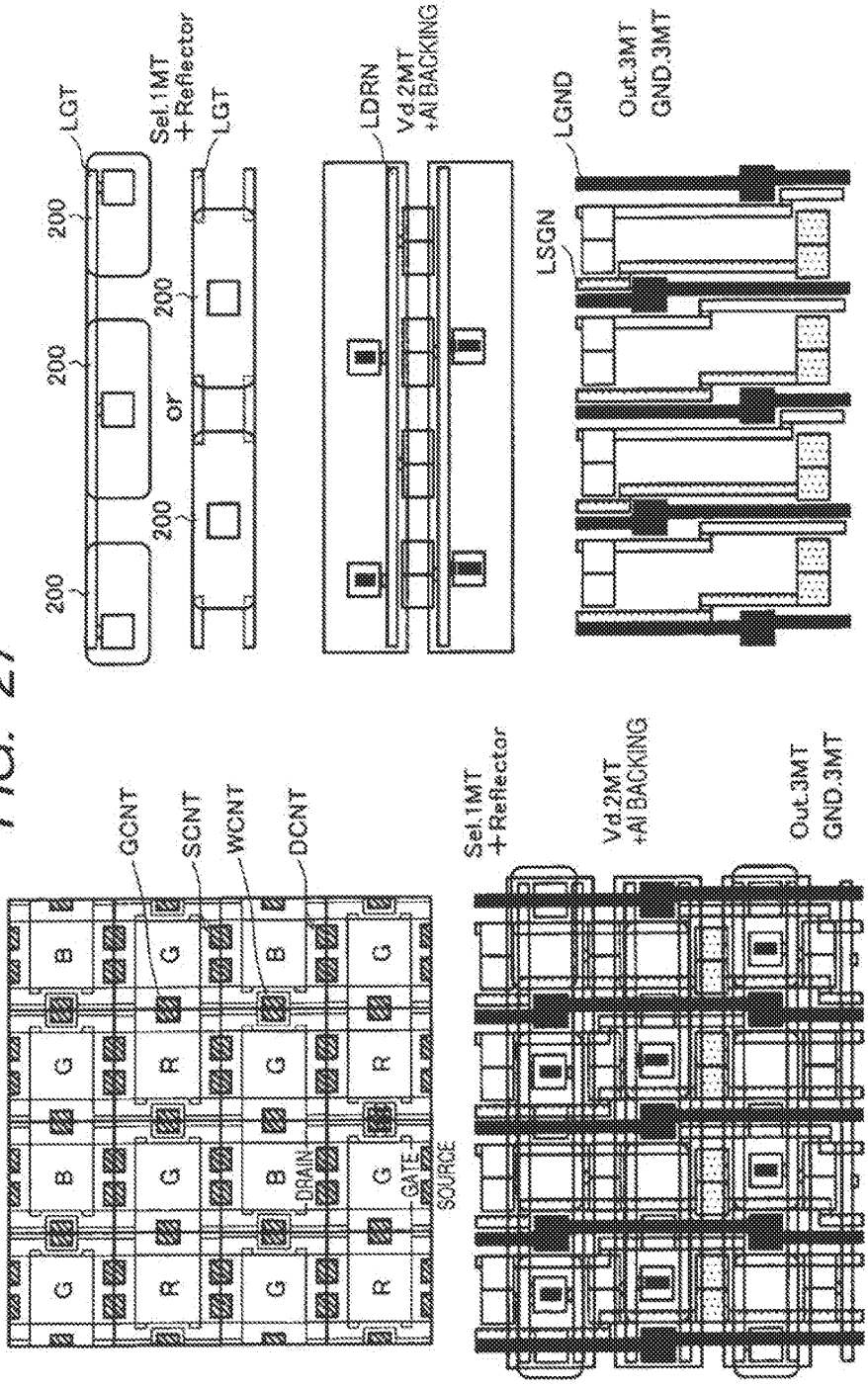
FIG. 26B



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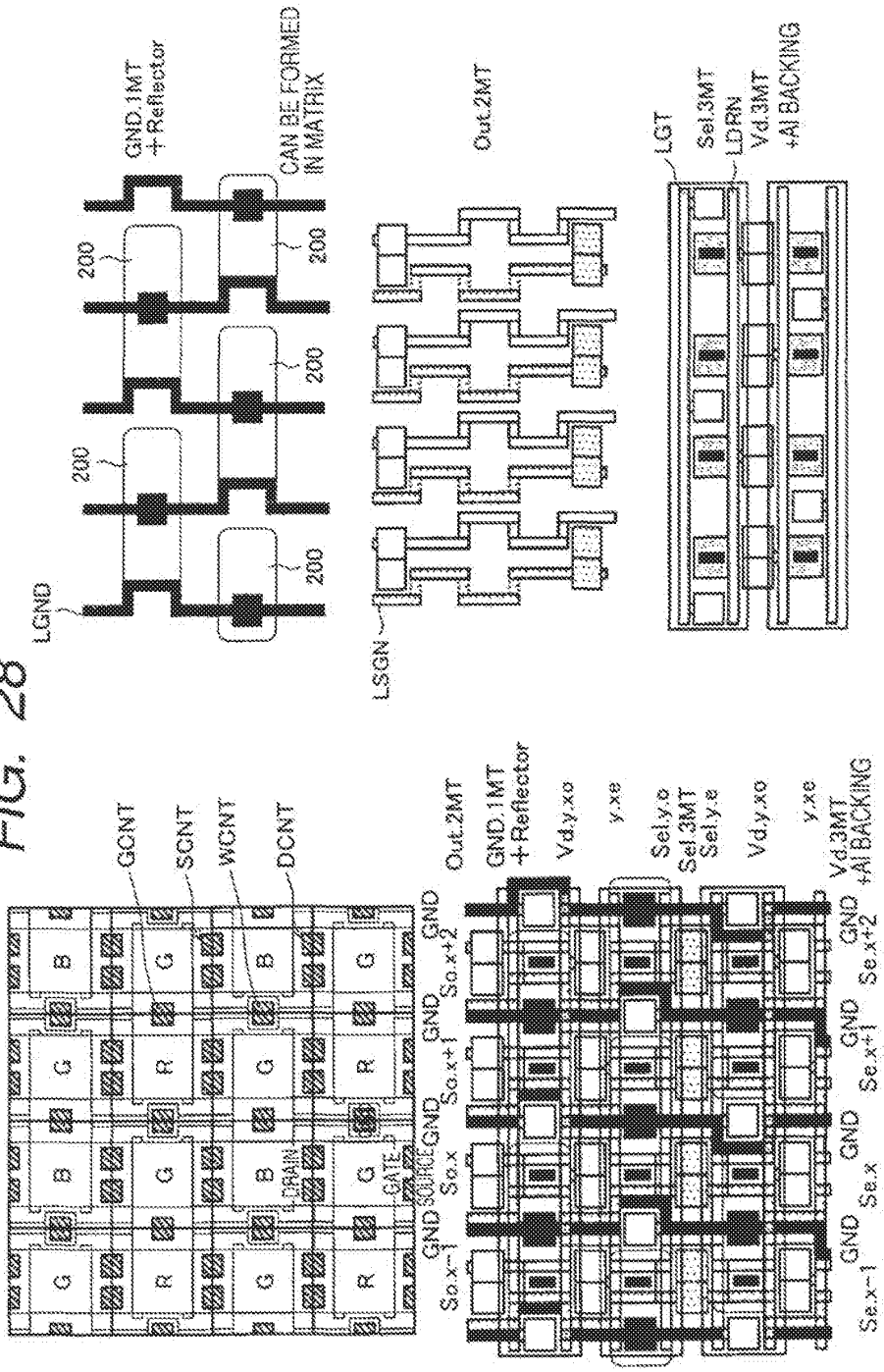
FIG. 27



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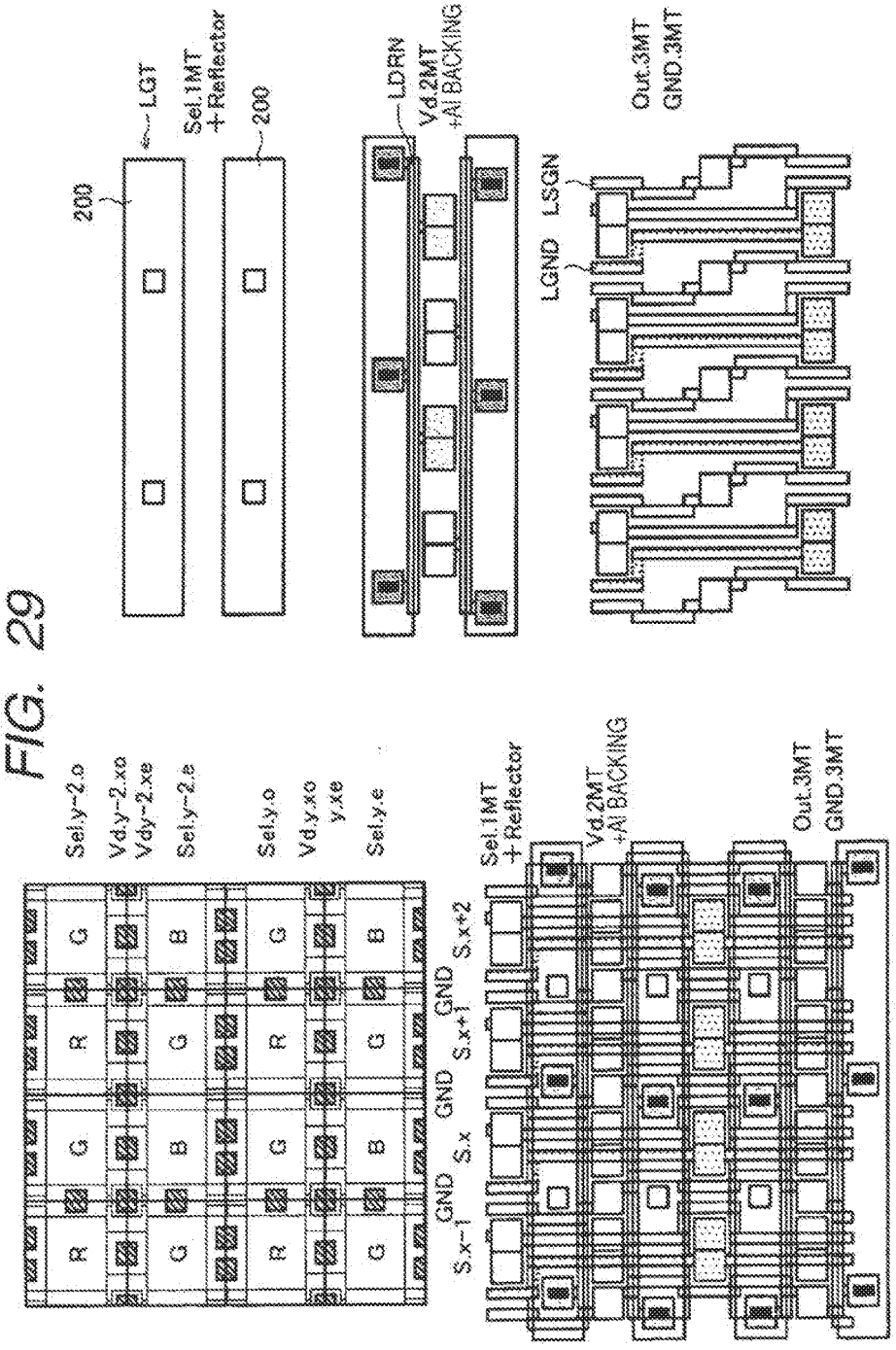
FIG. 28



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FIG. 29



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FIG. 30A

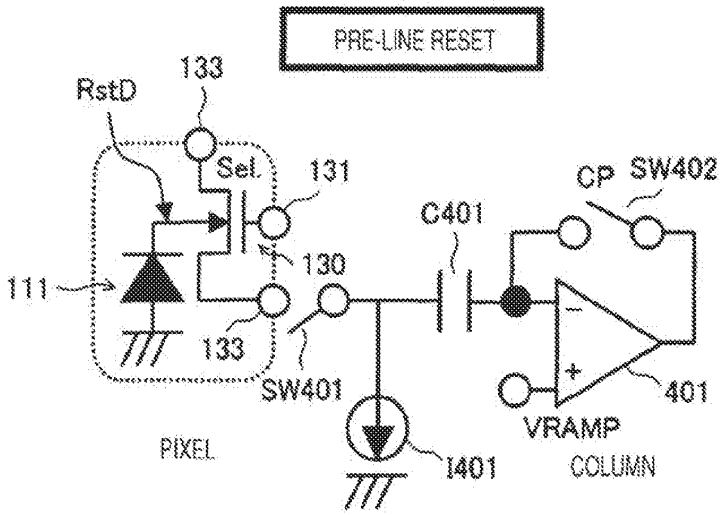
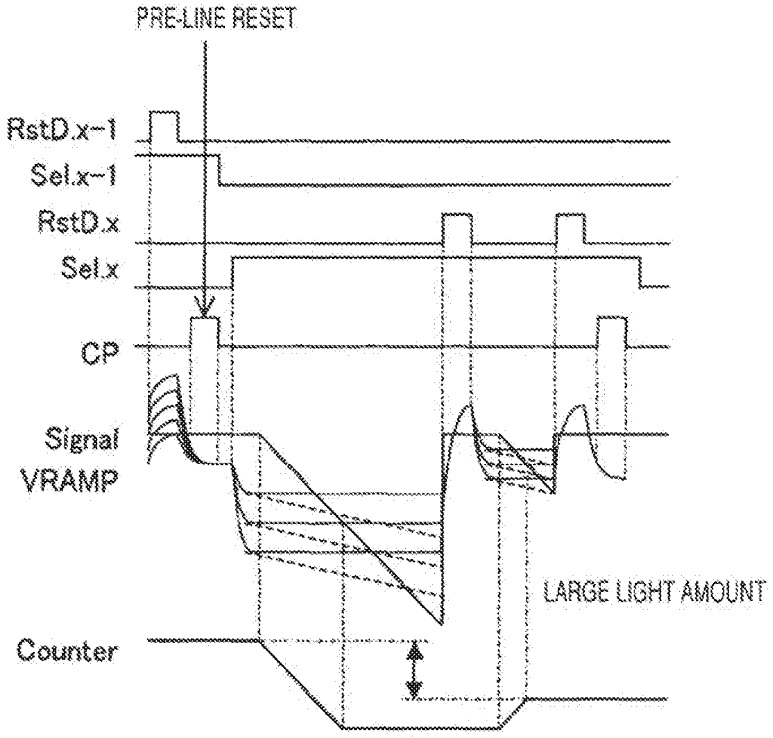


FIG. 30B



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FIG. 31A

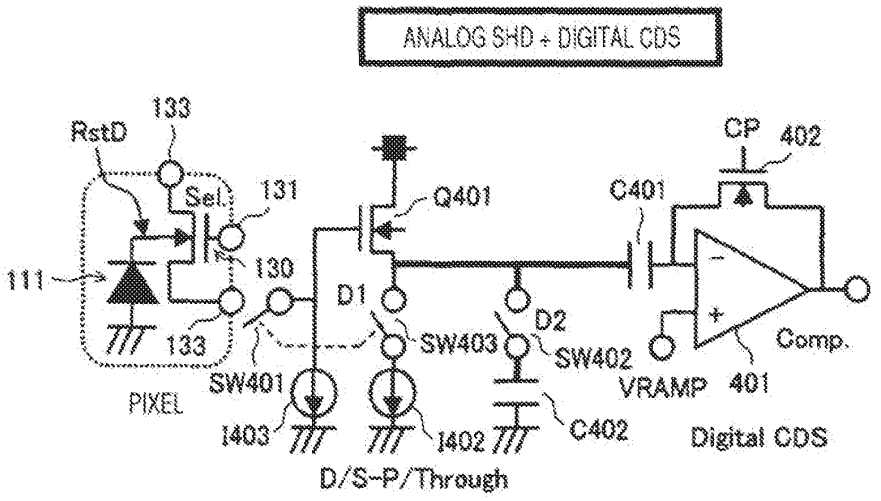
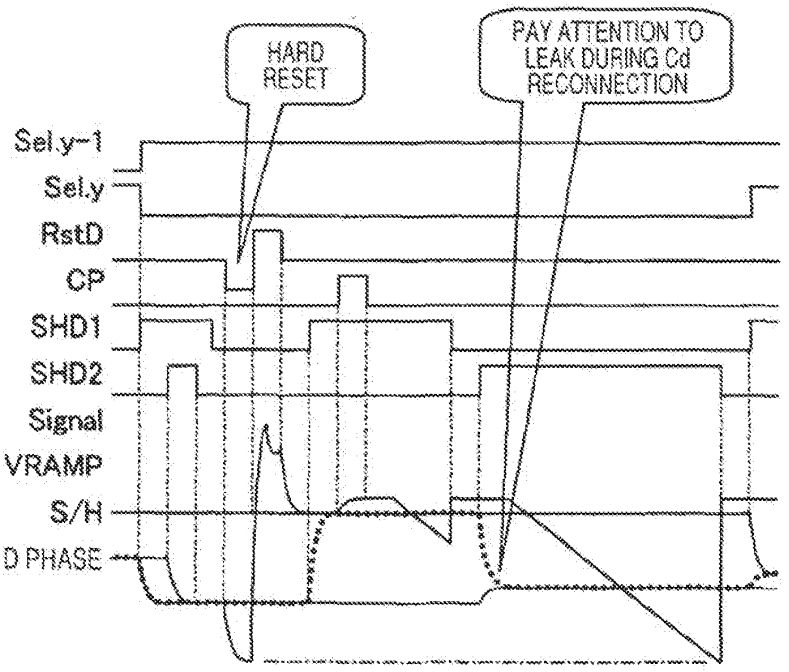


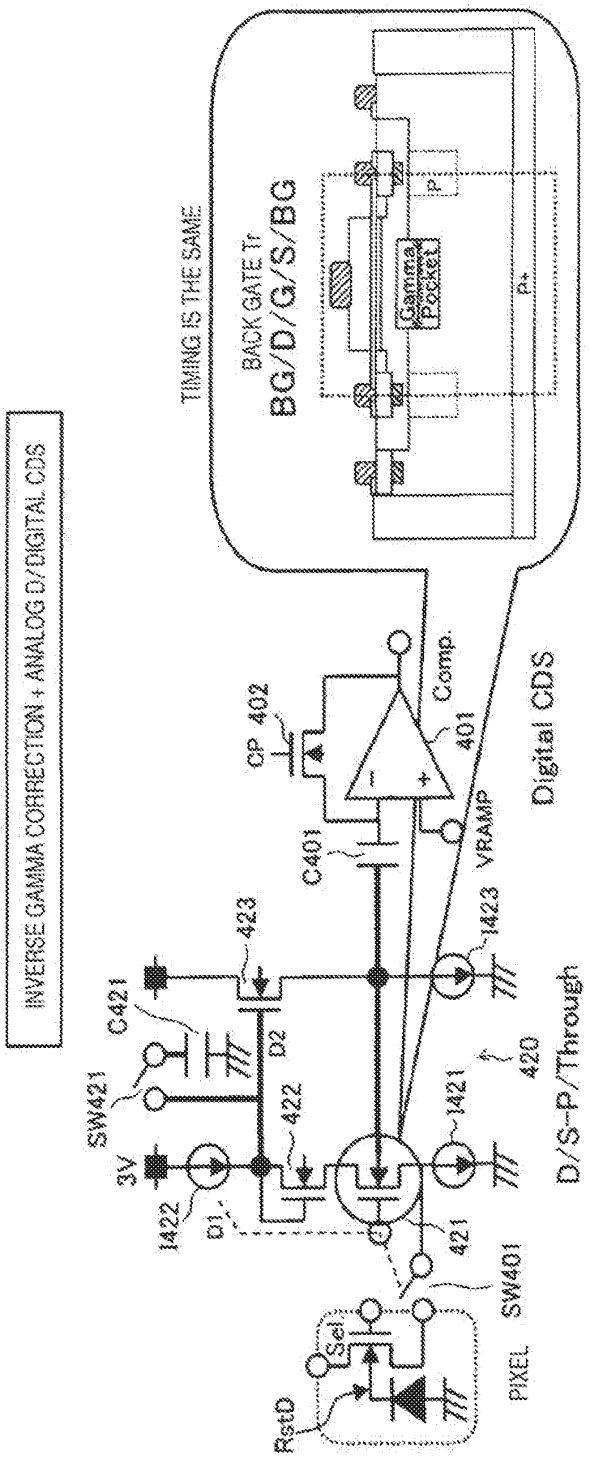
FIG. 31B



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FIG. 32



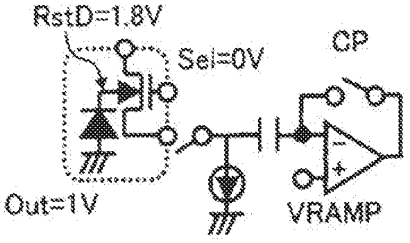
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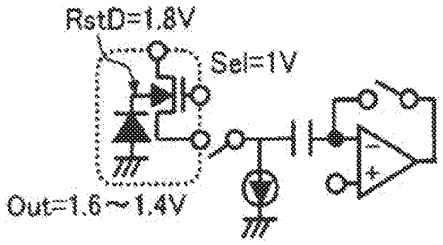
FIG. 33A

WORKING VOLTAGE

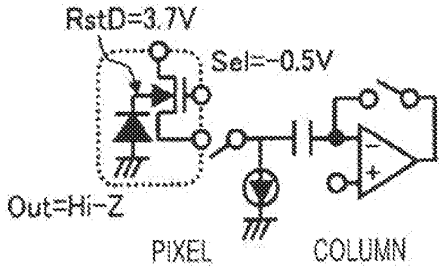
1. ACCUMULATION PIXEL (NON-SELECT PIXEL)



2. DATA READOUT



2. RESET



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DRIVING TIMING

FIG. 33B

■ STILL IMAGE SEQUENCE IN TWO-COLUMN SHARING

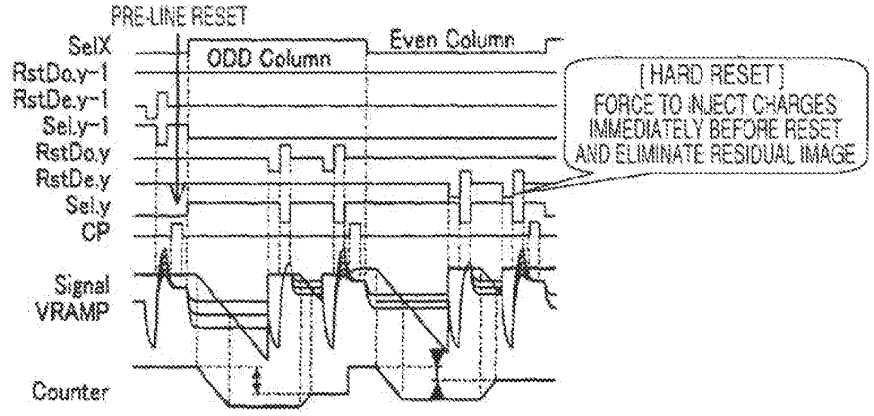
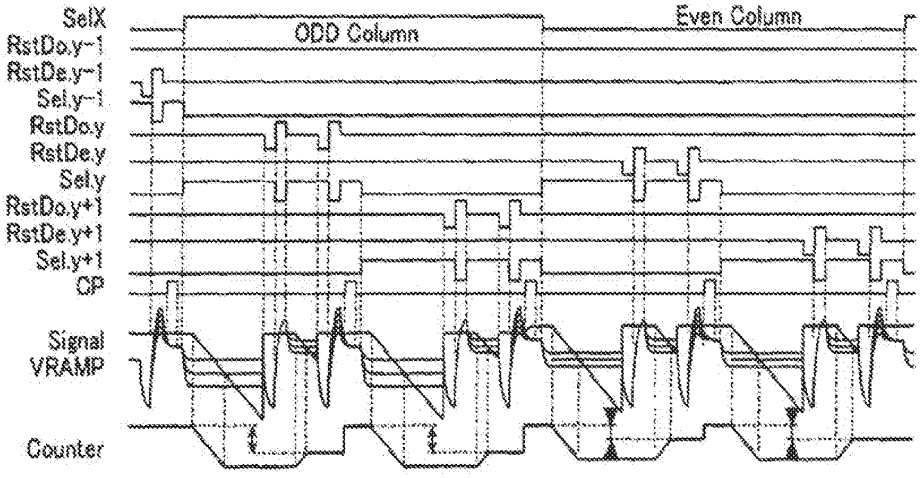


FIG. 33C

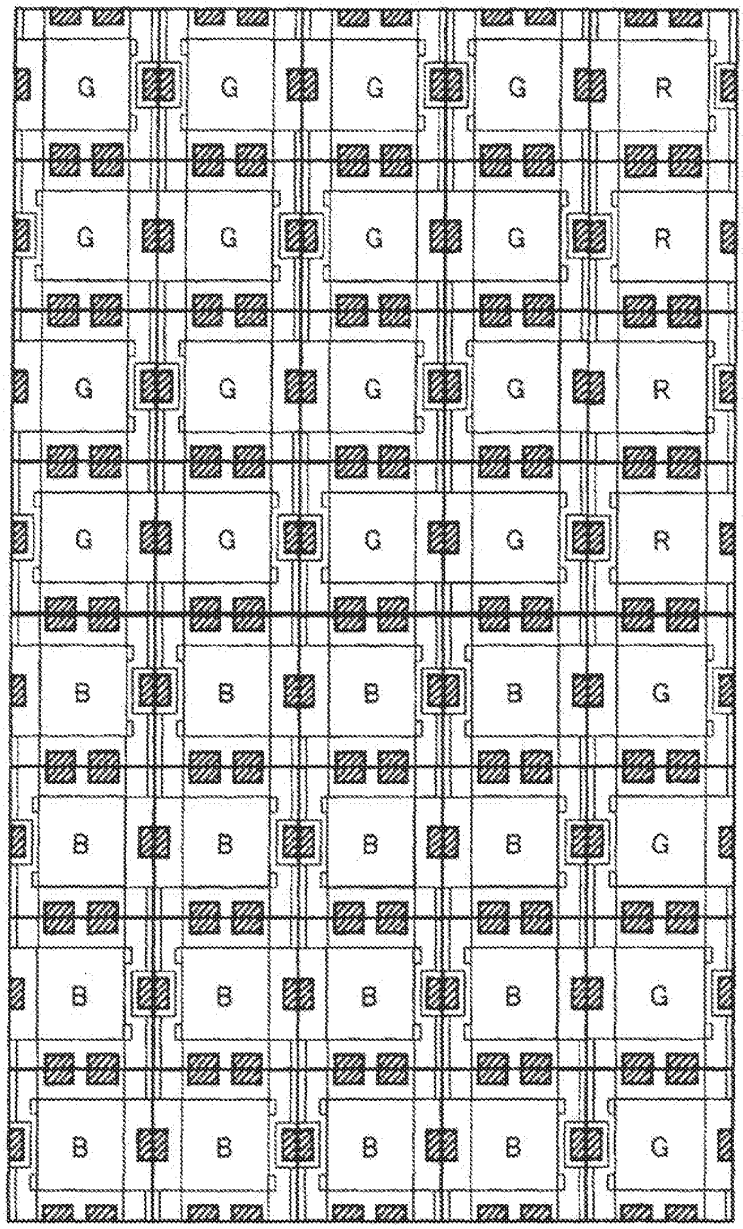
■ EXAMPLE OF 2 x 2 PIXEL ADDITION SEQUENCE



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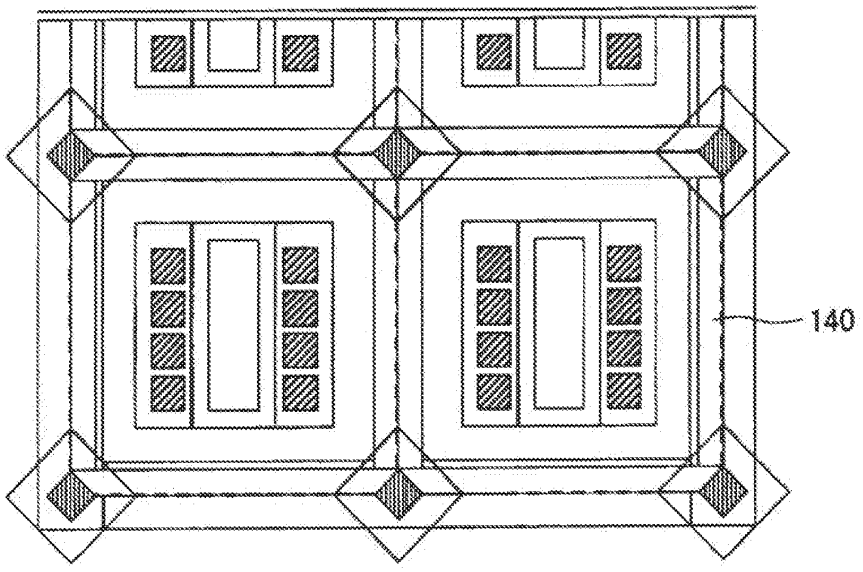
FIG. 34



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FIG. 35



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FIG. 36A

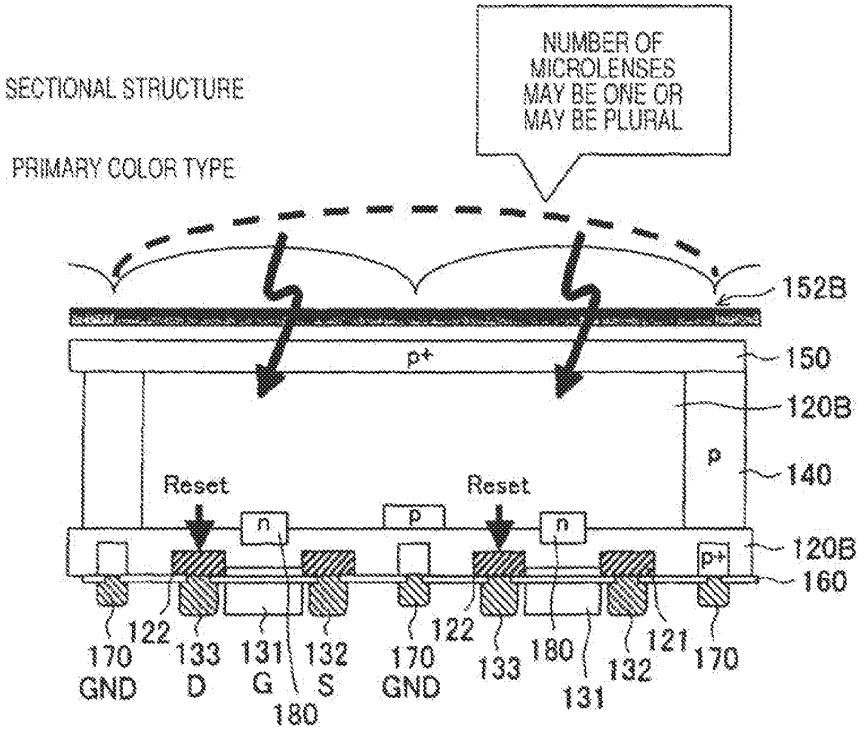
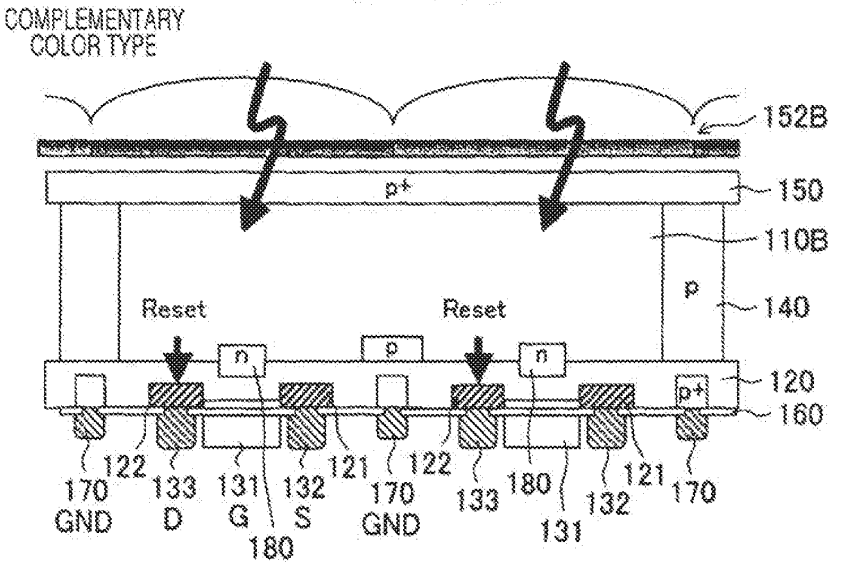


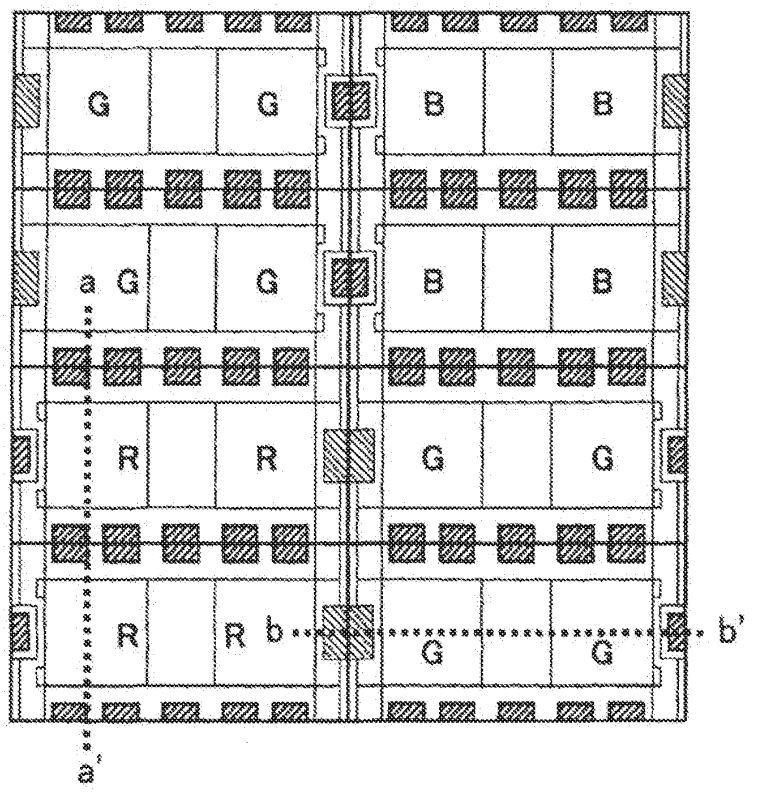
FIG. 36B



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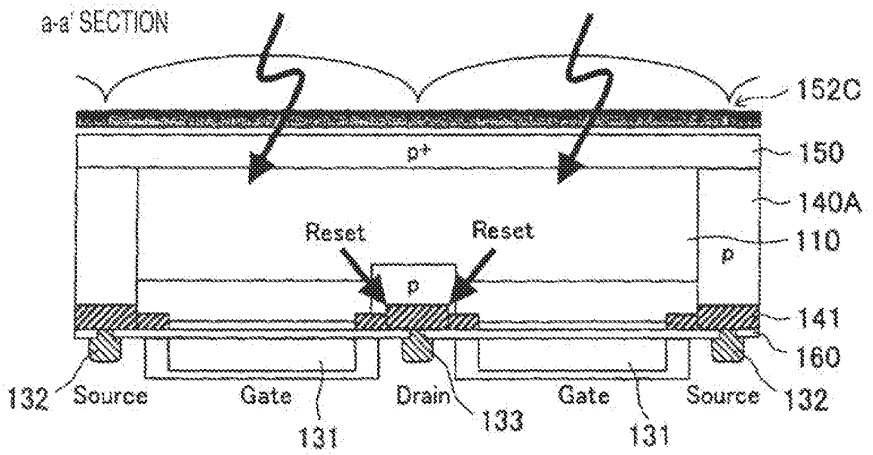
FIG. 37



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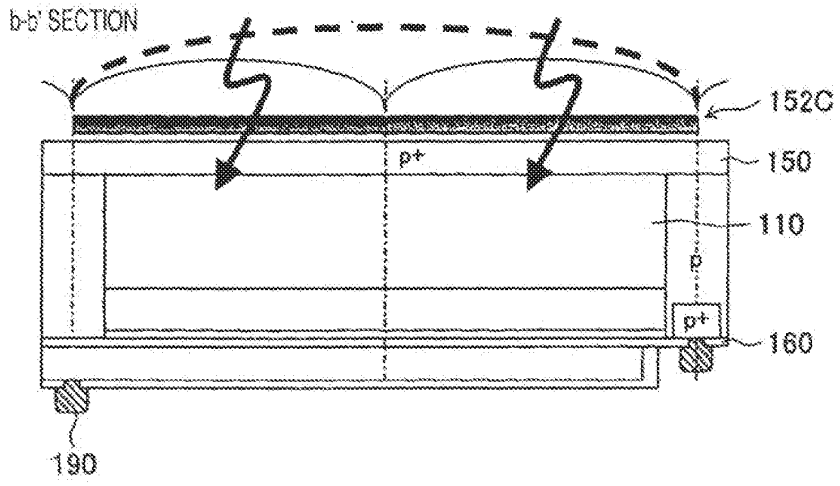
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FIG. 38A



COLOR FILTER ARRAY IN
COMPLEMENTARY COLOR TYPE

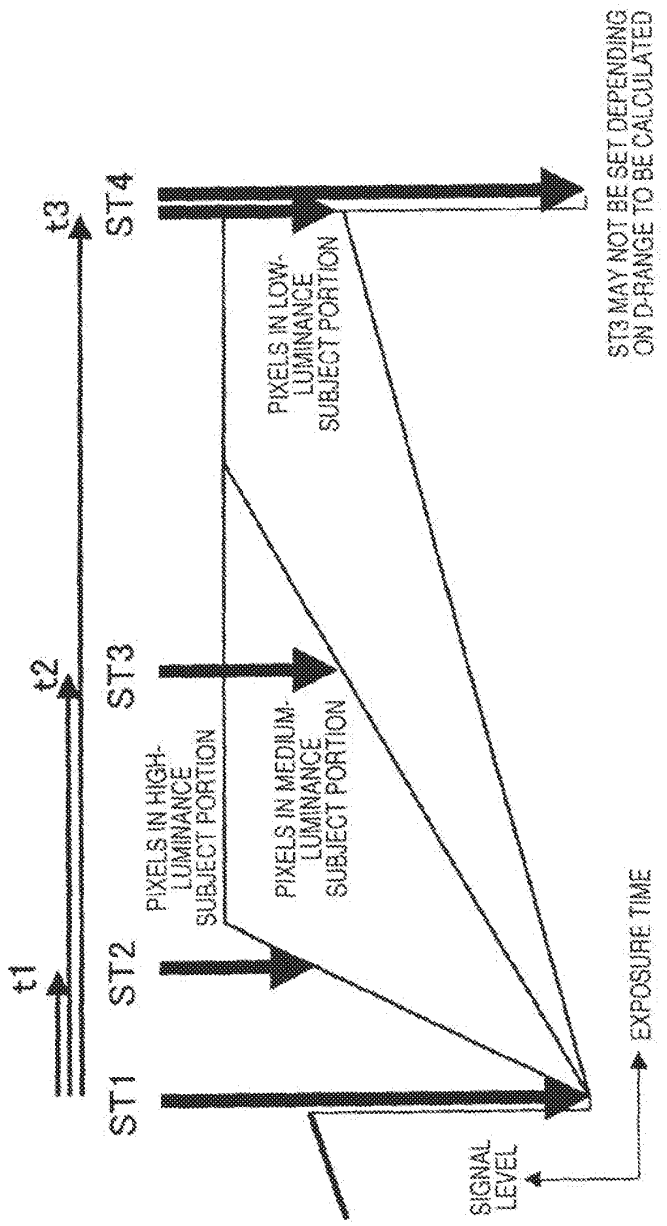
FIG. 38B



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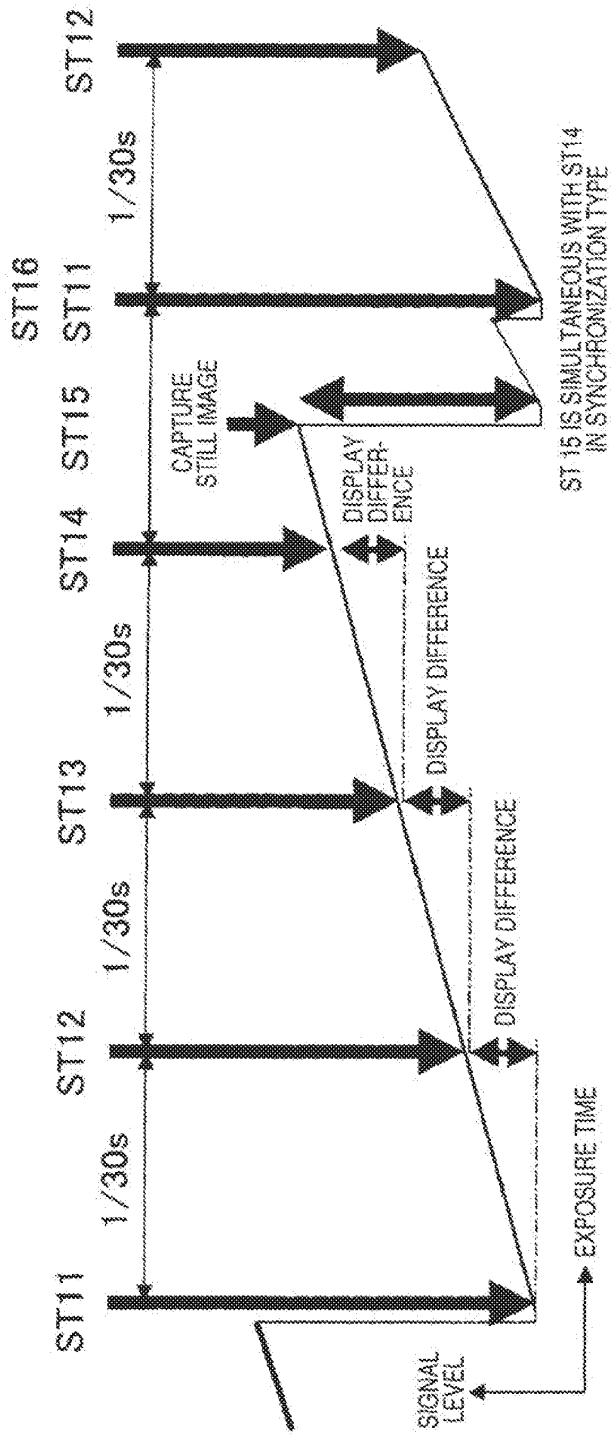
FIG. 39



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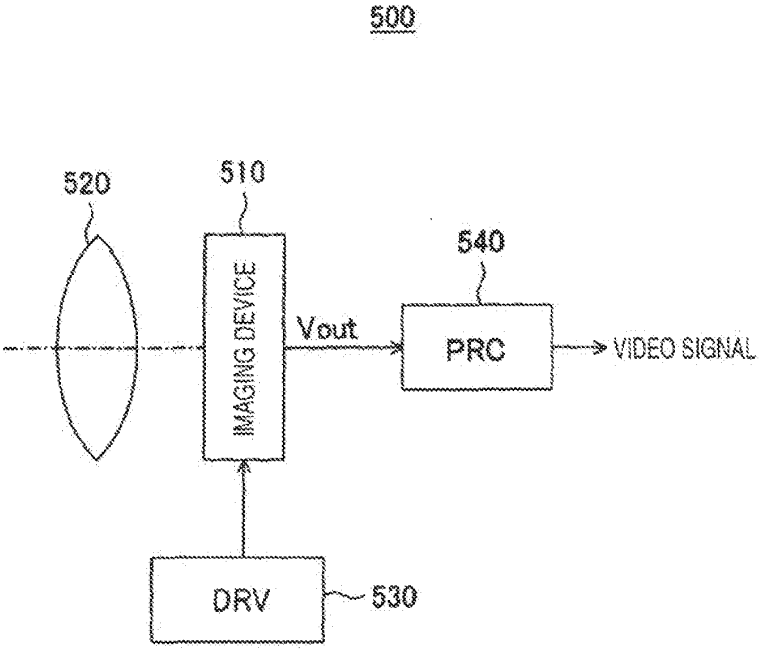
FIG. 40



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FIG. 41



SIONYX1403000036.0003

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REFERENCES CITED IN THE DESCRIPTION

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- JP 1938092 A **[0008]**
- JP 6120473 A **[0008]**
- JP 60140752 A **[0008]**
- JP 6414959 A **[0008]**
- JP 2692218 B **[0008]**
- JP 3752773 B **[0008]**
- JP 2304973 A **[0008]**
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- JP 2005085999 A **[0008]**
- JP 2003031765 A **[0009] [0020]**
- JP 10065138 A **[0011] [0022]**

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Espacenet

Bibliographic data: FR2827707 (A1) — 2003-01-24

Bolometric detector production comprises use of sacrificial auxiliary layer to connect reading circuit to bolometric substrate of polycrystalline silicon to detect infrared radiation

Inventor(s): LARRE ANNICK ± (LARRE ANNICK)

Applicant(s): FR DE DETECTEURS INFRAROUGES S [FR] ± (SOCIETE FRANCAISE DE DETECTEURS INFRAROUGES - SOFRADIR)

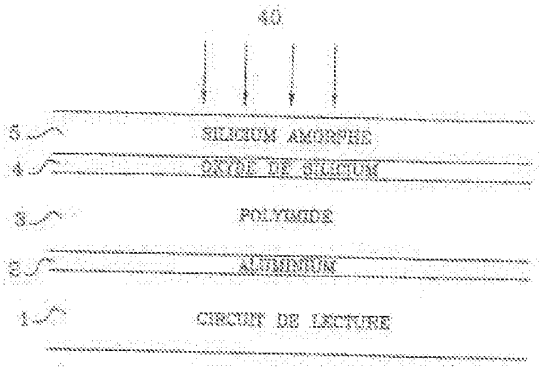
Classification: - international: ***G01J5/20; H01L27/146; H01L31/18;*** (IPC1-7): G01J5/20; H01L27/146; H04N5/33
- cooperative: **G01J5/02**; **G01J5/023**; **G01J5/024**; **G01J5/20**; **H01L27/14649**; **H01L27/14683**; **H01L31/1872**; G01J5/046; Y02E10/50; Y02P70/521

Application number: FR20010009715 20010720

Priority number (s): FR20010009715 20010720

Also published as: FR2827707 (B1)

Abstract of FR2827707 (A1)



The production of a bolometric detector comprises, from a reading circuit produced on a silicon substrate (1): (a) forming a first auxiliary sacrificial layer (3) on the silicon substrate, destined to be removed after the realization of the detector in order to thermally decouple the reading circuit of the detection module; and (b) forming on this sacrificial layer a layer of bolometric material of amorphous silicon (5) and electrodes to carry the necessary electric signals for the operation of the bolometer and to send the signal resulting from the detection of infrared radiation by the bolometer to the reading circuit. The layer of bolometric material is subjected to a laser radiation to transform it

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into a polycrystalline silicon. An Independent claim is also included for a bolometric detector using polycrystalline silicon as the bolometric material.

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(22) Date de dépôt : 20.07.01.

(30) Priorité :

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(56) Liste des documents cités dans le rapport de recherche préliminaire : *Se reporter à la fin du présent fascicule*

(60) Références à d'autres documents nationaux apparentés :

(71) Demandeur(s) : *STE FRANCAISE DE DETECTEURS INFRAROUGES - SOFRADIR Société à responsabilité limitée* — FR.

(72) Inventeur(s) : LARRE ANNICK.

(73) Titulaire(s) :

(74) Mandataire(s) : CABINET LAURENT ET CHARRAS.

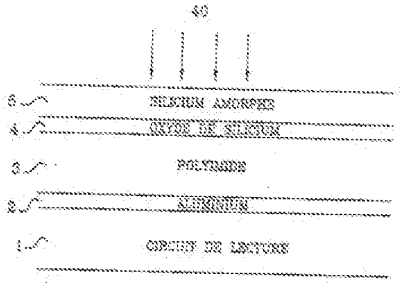
(54) PROCEDE DE REALISATION D'UN DETECTEUR BOLOMETRIQUE ET DETECTEUR REALISE SELON CE PROCEDE.

(57) Ce procédé pour la fabrication d'un détecteur bolométrique, consiste, à partir d'un circuit de lecture, notamment réalisé sur un substrat silicium (1):

- tout d'abord, à former une première couche auxiliaire sacrificielle (3) sur ledit substrat silicium, destinée à être ôtée par tout moyen connu après réalisation du détecteur afin de découpler thermiquement le circuit de lecture (1) du module de détection;

- puis à former sur cette couche auxiliaire sacrificielle (3), entre autres une couche de matériau bolométrique en silicium amorphe (5), mais également des électrodes (6), destinées à envoyer des signaux électriques nécessaires au fonctionnement du bolomètres et à acheminer le signal résultant de la détection du rayonnement infra rouge par ledit bolomètre au niveau du circuit de lecture.

On soumet la couche (5) de matériau bolométrique, constituée de silicium amorphe, à un rayonnement laser, destiné à le transformer en silicium polycristallin.



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PROCEDE DE REALISATION D'UN DETECTEUR BOLOMETRIQUE ET DETECTEUR BOLOMETRIQUE REALISE SELON CE PROCEDE.

L'invention concerne un procédé pour la réalisation de détecteurs bolométriques. Elle vise également le détecteur bolomètre obtenu selon ce procédé. L'invention trouve tout naturellement son application dans le domaine de l'imagerie infrarouge, et en particulier, dans l'assemblage matriciel d'une pluralité de détecteurs élémentaires (également dénommés « pixels » ou « photosites »).

De nombreux types de détecteurs de rayonnement infrarouge sont aujourd'hui disponibles. Parmi ces différents types de détecteurs, certains d'entre eux sont susceptibles de fonctionner à température ambiante, c'est à dire sans la nécessité d'un refroidissement, contrairement aux dispositifs du type détecteurs quantiques, qui convertissent directement l'énergie du rayonnement capté en porteurs électriques libres.

Ce type de détecteur non refroidi met en œuvre la variation d'une propriété de l'un des matériaux qui les constituent en fonction de la température. Dans le cadre des détecteurs bolométriques, cette propriété est la résistivité du matériau.

De manière connue, un tel détecteur non refroidi associe pour chaque photosite :

- des moyens d'absorption du rayonnement infrarouge pour la conversion de ce dernier en chaleur ;
- des moyens d'isolation thermique du détecteur, permettant à celui-ci de s'échauffer ;
- des moyens de thermométrie qui, dans le cadre d'un détecteur bolométrique utilise un élément résistif variable avec la température, et ;
- des moyens de lecture des signaux électriques issus des moyens de thermométrie, lesdits moyens de lecture intégrant une composante de prise de contact et de transport du signal du matériau bolométrique vers une composante d'exploitation du signal, en général de nature microélectronique.

Dans le cadre de l'imagerie infrarouge, les détecteurs mis en œuvre sont généralement réalisés sous forme de matrices de détecteurs élémentaires, rapportés sur un substrat, le plus souvent constitué de silicium.

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Les performances d'un tel détecteur bolométrique non refroidi dépendent de différents facteurs, parmi lesquels figure bien évidemment, le matériau bolométrique mis en œuvre.

Avantageusement, ce matériau bolométrique est constitué de silicium amorphe (voir par exemple US-A-5 021 663 ou US-A-5 367 167), mais peut être également constitué de silicium/germanium, voire d'oxyde de Vanadium (V_2O_5).

La mise en œuvre de silicium amorphe est en outre décrite dans le document FR-A-2 752 299. Dans ce document, le détecteur bolométrique est composé d'électrodes assurant simultanément les fonctions d'électrodes, et d'absorbeur de rayonnement photonique, lesdites électrodes étant interdigitées sur la même couche de matériau sensible constitutif du matériau bolométrique. Dans une version particulière décrite dans ce document, les électrodes sont insérées entre deux couches de matériau bolométrique.

On connaît également, par le document FR-A-2 796 148, un autre type d'empilement technologique pour détecteur bolométrique, dans lequel les électrodes assurent également la double fonction d'électrodes et d'absorbeur du rayonnement photonique, mais dans lequel, le matériau sensible constitutif du bolomètre, également constitué de silicium amorphe, est partiellement isolé électriquement des électrodes.

Quel que soit le montage mis en œuvre, le détecteur en résultant présente encore un niveau élevé de bruit à basse fréquence. Par ailleurs, le silicium amorphe présente également l'inconvénient d'être métastable, c'est à dire que ses caractéristiques sont susceptibles d'évoluer de manière importante sous l'influence des différentes étapes technologiques, se traduisant en quelque sorte par des recuits, mettant en œuvre des excursions thermiques (cuisson des résines, gravures, dépôts).

Par voie de conséquence, le détecteur bolométrique en résultant présente des variations importantes des signaux en réponse à la détection du rayonnement infrarouge en fonction des différentes conditions thermiques dans lesquelles il est susceptible de s'être trouvé.

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A titre surabondant, la mise en œuvre de silicium amorphe sur un circuit de lecture et d'exploitation dont la fabrication est achevée, impose un dépôt dudit matériau à basse température (inférieure à 450 °C), ce qui conditionne un niveau de dopage, notamment en hydrogène ou en bore, relativement peu élevé, et qu'il est impossible d'augmenter de façon significative.

Or, on a pu montrer qu'un niveau de dopage plus important permettait d'accroître la variabilité de la résistivité du matériau bolométrique en fonction de la température, et partant, la réponse du détecteur bolométrique au rayonnement infrarouge qu'il est destiné à détecter.

En outre, l'accroissement du dopage augmente la résistance thermique du matériau silicium amorphe, et par voie de conséquence, celle des bras-support de la microstructure flottante, ce qui s'avère favorable à l'isolation thermique de ladite structure, et partant, à la réduction des bruits des signaux en réponse.

L'objet de l'invention est d'améliorer les caractéristiques du matériau bolométrique sensible au rayonnement infrarouge, notamment en s'affranchissant des contraintes et des limites thermiques imposées à l'ensemble du circuit de lecture/élément détecteur.

Ce procédé, pour la fabrication d'un détecteur bolométrique, consiste, à partir d'un circuit de lecture, notamment réalisé sur un substrat silicium :

- tout d'abord, à former une première couche auxiliaire sacrificielle sur ledit substrat silicium, destinée à être ôtée par tout moyen connu après réalisation du détecteur afin alors de découpler thermiquement le circuit de lecture du module de détection ;
- puis à former sur cette couche auxiliaire sacrificielle, entre autres une couche de matériau bolométrique en silicium amorphe, mais également des électrodes destinées à envoyer les signaux électriques (impulsions, stimuli ou courant de polarisation) nécessaires au fonctionnement du bolomètre, et à acheminer le signal résultant de la détection du rayonnement infra rouge par le bolomètre au niveau du circuit de lecture.

Il se caractérise en ce que l'on soumet la couche de matériau bolométrique, constituée de silicium amorphe, à un rayonnement laser propre à le transformer en silicium polycristallin.

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Ce faisant, on confère tout d'abord au détecteur ainsi réalisé une plus grande stabilité vis à vis des diverses sollicitations, principalement thermiques, en comparaison avec les détecteurs à base de silicium amorphe.

Ensuite, on optimise de manière déterminante la sensibilité du détecteur, puisque d'une part, le silicium polycristallin présente une variabilité de la résistivité plus importante sous l'effet de la chaleur, et par voie de conséquence du rayonnement infra rouge incident, et d'autre part, son niveau de dopage peut être accentué, diminuant de fait le bruit basse fréquence que l'on rencontre avec le silicium amorphe. Le dopage favorise également l'augmentation de la résistance thermique dudit bolomètre, et donc la sensibilité de sa réponse aux signaux infra rouges incidents.

Avantageusement, le laser mis en œuvre est un laser à excimère, agissant par impulsions. On dispose ainsi d'une gamme de puissance ou de densité d'énergie tout à fait adapté au matériau bolométrique mis en œuvre.

Selon une autre caractéristique avantageuse de l'invention, le matériau bolométrique est séparé de la couche auxiliaire sacrificielle par une couche diélectrique, constituée d'un oxyde de silicium, et notamment de SiO_x (proche de SiO_2) ou de nitrure de silicium.

Par ailleurs, et avantageusement, le substrat en silicium recevant le circuit de lecture est revêtu d'une couche d'un matériau réfléchissant le rayonnement infrarouge, et typiquement constitué d'aluminium.

L'invention concerne également le détecteur bolométrique issu de ce procédé.

Ce détecteur bolométrique, associé à un circuit de lecture notamment par la technologie dite « microponts », comprend au moins une couche de matériau bolométrique associée à au moins deux électrodes, ledit matériau bolométrique étant thermiquement isolé dudit circuit de lecture. Il se caractérise en ce que le matériau bolométrique est constitué par un silicium polycristallin.

Avantageusement, le matériau bolométrique repose sur une couche d'un matériau diélectrique, notamment constitué d'oxyde de silicium (silice) ou de nitrure de silicium.

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La manière dont l'invention peut être réalisée et les avantages qui en découlent ressortiront mieux des exemples de réalisation qui suivent donnés à titre indicatif et non limitatif, à l'appui des figures annexées.

La figure 1 est une représentation schématique en section illustrant la mise en œuvre du procédé conforme à l'invention.
La figure 2 est une représentation schématique en perspective simplifiée d'une forme de réalisation dudit détecteur bolométrique conforme à l'invention.
La figure 3 est une vue analogue à la figure 2 d'une autre forme de réalisation de l'invention.

On a représenté sur la figure 1, et sur les figures 2 et 3, sous la référence (1) un substrat, notamment en silicium, comprenant des dispositifs électroniques (non représentés), tels que par exemple réalisés selon la technologie CMOS. Ces dispositifs sont destinés à, d'une part, envoyer en direction du matériau bolométrique proprement dit les signaux nécessaires au fonctionnement du détecteur, et d'autre part, à recevoir et pouvoir interpréter les signaux en réponse issus dudit matériau bolométrique, ensuite notamment d'une irradiation de celui-ci par un rayonnement infrarouge.

Selon une caractéristique avantageuse, ce substrat en silicium est recouvert d'une couche de matériau réfléchissant dans la gamme de longueurs d'ondes de l'infrarouge, et typiquement constitué par une couche d'aluminium (2). Le dépôt d'une telle couche s'effectue de manière connue par pulvérisation cathodique.

Le complexe ainsi réalisé reçoit une couche auxiliaire sacrificielle (3), avantageusement réalisée en polyimide, et destinée à être supprimée, après réalisation définitive du détecteur bolométrique, par tout moyen connu, et notamment par plasma oxygène. La suppression de cette couche va ainsi définir une cavité destinée à isoler thermiquement le bolomètre du circuit de lecture.

Cette couche auxiliaire sacrificielle (3) est revêtue avantageusement d'une couche d'un matériau diélectrique (4), typiquement réalisé en silice SiO_2, voire par du nitrure de silicium. De la sorte, le bolomètre (5), décrit ci-après plus en détail, est supporté mécaniquement par un matériau isolant électrique sans effet sur ses propriétés, et en particulier sur sa résistance électrique.

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Enfin, on revêt l'ensemble d'une couche de silicium amorphe, constitutive du bolomètre (5) proprement dit, selon une des techniques classiques et bien connues de l'homme du métier, telle la décomposition thermique (CVD), ou la décomposition plasma (PECVD), ou encore la décomposition cathodique.

Quelle que soit la technologie retenue, à savoir structure sandwich à électrodes parallèles (figure 2), ou électrodes coplanaires (figure 3), des électrodes (6) sont positionnées en temps utile, et tel que cela a été abondamment décrit dans les documents de l'art antérieur précités.

Par exemple, et ainsi que cela a été décrit dans les deux documents précités, on peut tout d'abord déposer le matériau bolométrique (Silicium amorphe) avant le matériau constitutif des électrodes. Le traitement dudit silicium amorphe conformément à l'invention intervient alors avant la fabrication desdites électrodes. Mais on peut également réaliser la technologie propre aux électrodes sur la couche sacrificielle ou sur la couche de matériau isolant, et exécuter ensuite le dépôt de silicium amorphe et son traitement conforme à l'invention.

Dans l'exemple décrit, on a représenté un seul bolomètre au sein du détecteur. De fait, ce bolomètre est connecté au substrat silicium (1) à la fois électriquement et mécaniquement par le biais desdites électrodes (6).

De fait, et ainsi qu'évoqué précédemment, lors de l'achèvement du détecteur bolométrique conforme à l'invention, la couche auxiliaire sacrificielle est supprimée, de sorte que le bolomètre est maintenu thermiquement isolé du substrat silicium (1) par la cavité ainsi générée, avantageusement occupée par un gaz lourd, tel que le xénon, ou encore vide de gaz, en plaçant le détecteur alors obtenu dans une enceinte sous vide.

Cette structure est dénommée dans la technologie en question par structure à microponts.

L'invention s'applique également aux structures où les fonctions électrodes et absorbeurs sont dissociées, et leurs matériaux séparés par un diélectrique, telles que cela a été décrit en relation avec les brevets américains précités.

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Selon une caractéristique fondamentale de l'invention, le matériau bolométrique ainsi réalisé est soumis à un rayonnement laser, et notamment au moyen d'un laser à excimère, afin d'aboutir à la transformation du silicium amorphe constitutif du bolomètre (5) proprement dit en silicium polycristallin. La soumission du silicium amorphe à ce rayonnement laser induit un recuit du silicium amorphe et plus précisément, aboutit à la fusion du silicium amorphe et à sa recristallisation pour aboutir à du silicium polycrystallin.

L'interaction du laser avec le silicium amorphe a pour effet principal d'élever instantanément la température du matériau irradié et d'induire, si l'énergie laser est suffisante, la fusion de celui-ci, sans pour autant affecter significativement les couches sous-jacentes, et en particulier la couche auxiliaire sacrificielle. Le circuit de lecture est a fortiori épargné par cette opération.

La durée de l'élévation de température de la fusion est de l'ordre de grandeur de la durée de l'impulsion laser. Elle peut typiquement atteindre quelques dizaines de nanosecondes, en fonction de l'énergie laser pour des impulsions classiques de 10 à 20 nanosecondes des lasers à excimère.

La fusion de la surface commence vers la fin de l'impulsion laser, le retard diminuant avec l'énergie des impulsions laser mises en oeuvre. Le front de fusion pénètre à l'intérieur du matériau jusqu'à atteindre une valeur maximum qui définit la profondeur fondue avant de revenir vers la surface. La profondeur fondue ainsi que la durée de fusion augmente bien évidemment avec l'énergie laser.

Le choix d'un laser à excimère du type XeCl ou KrF, voire encore d'un laser YAG triplé, donc fonctionnant tous dans le domaine de l'UV, est dicté par la puissance souhaitée au niveau de l'impulsion. On choisit typiquement une densité d'énergie comprise entre 200 et 400 mJ/cm².

Avantageusement, on sélectionne l'énergie laser afin que l'intégralité du film de silicium amorphe soit refondue et recristallisée.

On a pu montrer que pour une énergie laser supérieure à 360 mJ/cm², une épaisseur de 50 nm de silicium amorphe était complètement recristallisée en silicium polycristallin de bonne qualité.

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L'énergie laser est aisément ajustable par l'homme du métier afin de fondre la totalité de l'épaisseur du matériau amorphe en un seul voire en plusieurs tirs ou impulsions laser en fonction de l'équipement utilisé. De même, en fonction d'un tel équipement, le spot laser est scanné ou déplacé (pas à pas) jusqu'à induire la transformation de la totalité de la couche de silicium amorphe de la pluralité de photosites bolométriques considérée.

Par la transformation du matériau bolométrique d'une nature amorphe à une nature cristalline, on aboutit à un matériau parfaitement stable, notamment thermiquement, en tout cas aux conditions de fonctionnement du détecteur bolométrique, et insensible aux opérations technologiques impliquant des excursions thermiques non intentionnelles (durcissement des résines, par exemple, dépôt, gravures…). En d'autres termes, le détecteur bolométrique résultant est insensible à l'environnement thermique qu'il peut rencontrer sous ses conditions normales de fabrication et d'utilisation.

Par ailleurs, il devient possible d'accroître le niveau de dopage, en raison, en particulier, d'une meilleure incorporation, et ceci de manière parfaitement uniforme sur toute l'épaisseur du matériau, du fait du passage en phase liquide et de l'état cristallin du silicium une fois solidifié.

Ainsi que déjà précisé, du dopage dépend la résistance thermique du matériau bolométrique, et partant son isolation du circuit sous-jacent. En outre, le bruit basse fréquence tend à diminuer lorsque le dopage augmente. De la sorte, la mise en œuvre de silicium polycristallin permet de jouer sur ces deux paramètres, dans l'objectif d'améliorer les propriétés de détection et la sensibilité de tels détecteurs.

En outre, la mise en œuvre du procédé conforme à l'invention permet de conserver l'intégrité du circuit de lecture sous-jacent, ainsi que de la couche auxiliaire sacrificielle en polyimide. Cette couche sacrificielle est éliminée en phase ultime de réalisation du détecteur. La mise en œuvre du polyimide s'avère tout particulièrement avantageuse, compte tenu notamment de son enlèvement aisé et respectueux du reste de la structure, en raison de la sélectivité du plasma oxygène.

On conçoit dès lors tout l'intérêt du procédé conforme à l'invention, ainsi que du détecteur en résultant en termes de qualité et de sensibilité de détection infrarouge à température ambiante, mais également en termes de facilité de réalisation et des coûts réduits en résultant.

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REVENDICATIONS

1. Procédé pour la fabrication d'un détecteur bolométrique, consistant, à partir d'un circuit de lecture, notamment réalisé sur un substrat silicium (1) :
   - tout d'abord, à former une première couche auxiliaire sacrificielle (3) sur ledit substrat silicium, destinée à être ôtée par tout moyen connu après réalisation du détecteur afin de découpler thermiquement le circuit de lecture (1) du module de détection ;
   - puis à former sur cette couche auxiliaire sacrificielle (3), entre autres une couche de matériau bolométrique en silicium amorphe (5), mais également des électrodes (6), destinées à envoyer des signaux électriques nécessaires au fonctionnement du bolomètres et à acheminer le signal résultant de la détection du rayonnement infra rouge par ledit bolomètre au niveau du circuit de lecture,

   caractérisé en ce que l'on soumet la couche (5) de matériau bolométrique, constituée de silicium amorphe, à un rayonnement laser, destiné à le transformer en silicium polycristallin.

2. Procédé pour la fabrication d'un détecteur bolométrique selon la revendication 1, ***caractérisé*** en ce que le laser est un laser à excimère ou un YAG triplé.

3. Procédé pour la fabrication d'un détecteur bolométrique selon l'une des revendications 1 et 2, ***caractérisé*** en ce que la densité d'énergie du laser est comprise entre 200 et 400 mJ/cm^2.

4. Procédé pour la fabrication d'un détecteur bolométrique selon l'une des revendications 1 à 3, ***caractérisé*** en ce que préalablement à l'irradiation du silicium amorphe, constitutif du matériau bolométrique, on revêt la couche auxiliaire sacrificielle d'une couche d'un matériau diélectrique (4), notamment constituée d'un oxyde de silicium ou d'un nitrure de silicium.

5. Procédé pour la fabrication d'un détecteur bolométrique selon l'une des revendications 1 à 4, ***caractérisé*** en ce que préalablement à l'irradiation du silicium amorphe, constitutif du matériau bolométrique, on revêt le substrat silicium constitutif du circuit de lecture d'une couche d'un matériau réfléchissant le rayonnement infrarouge, et notamment par de l'aluminium.

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6. Détecteur bolométrique, associé à un circuit de lecture (1) notamment par la technologie dite « microponts », comprenant au moins une couche de matériau bolométrique (5) associée à au moins deux électrodes (6) assurant le contact électrique et mécanique dudit bolomètre avec le substrat (1) constitutif du circuit de lecture, ledit matériau bolométrique étant thermiquement isolé dudit circuit de lecture, *caractérisé* en ce que le matériau bolométrique est constitué par un silicium polycristallin.

7. Détecteur bolométrique selon la revendication 6, *caractérisé* en ce que le matériau bolométrique (5) repose sur une couche d'un matériau diélectrique, notamment constitué d'oxyde de silicium ou de nitrure de silicium.

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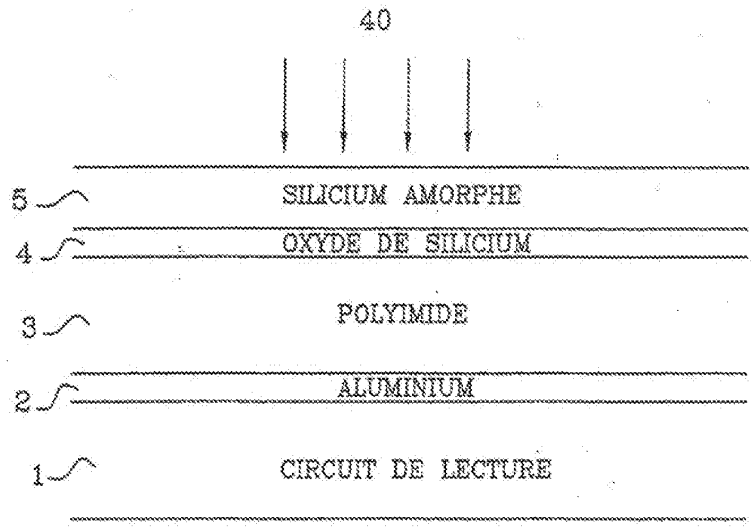


Fig. 1

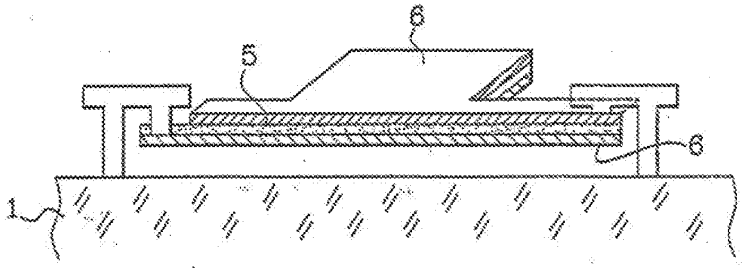


Fig. 2

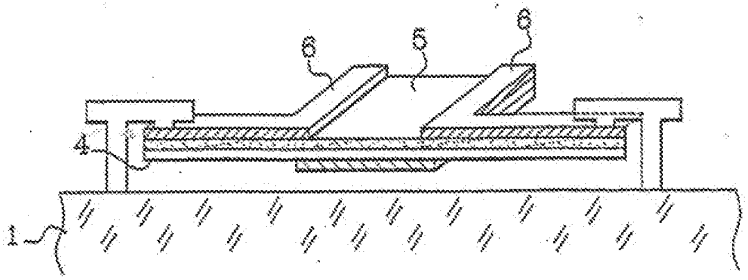


Fig. 3

SIONYX1403000036.0018

RÉPUBLIQUE FRANÇAISE

INPI
INSTITUT NATIONAL DE LA PROPRIETE INDUSTRIELLE

2827707

RAPPORT DE RECHERCHE PRÉLIMINAIRE

établi sur la base des dernières revendications déposées avant le commencement de la recherche

N° d'enregistrement national
FA 609582
FR 0109715

DOCUMENTS CONSIDÉRÉS COMME PERTINENTS		Revendication(s) concernée(s)	Classement attribué à l'invention par l'INPI
Catégorie	Citation du document avec indication, en cas de besoin, des parties pertinentes		
Y	US 5 260 225 A (LIU MICHAEL S ET AL) 9 novembre 1993 (1993-11-09)	1-3	H01L27/146 G01J5/20
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A		4,7	
Y	US 4 309 225 A (FAN JOHN C C ET AL) 5 janvier 1982 (1982-01-05) * colonne 4, ligne 26 - colonne 6, ligne 51; figures 7,8 *	1-3	
X	EP 0 867 702 A (IMEC INTER UNI MICRO ELECTR) 30 septembre 1998 (1998-09-30)	6	
A	* page 6, ligne 52 - page 7, ligne 41 *	1-5,7	
A,D	US 5 367 167 A (KEENAN WILLIAM F) 22 novembre 1994 (1994-11-22) * colonne 4, ligne 32 - colonne 5, ligne 24 * * colonne 6, ligne 50-64 *	1,5-7	
A	US 5 912 464 A (VILAIN MICHEL ET AL) 15 juin 1999 (1999-06-15) * le document en entier *	1-7	DOMAINES TECHNIQUES RECHERCHÉS (Int.Cl.7) G01J H01L
A	US 4 059 461 A (FAN JOHN C C ET AL) 22 novembre 1977 (1977-11-22) * le document en entier *		

Date d'achèvement de la recherche	Examinateur
14 mai 2002	Boero, M

CATÉGORIE DES DOCUMENTS CITÉS

X : particulièrement pertinent à lui seul
Y : particulièrement pertinent en combinaison avec un autre document de la même catégorie
A : arrière-plan technologique
O : divulgation non-écrite
P : document intercalaire

T : théorie ou principe à la base de l'invention
E : document de brevet bénéficiant d'une date antérieure à la date de dépôt et qui n'a été publié qu'à cette date de dépôt ou qu'à une date postérieure.
D : cité dans la demande
L : cité pour d'autres raisons

& : membre de la même famille, document correspondant

2

EPO FORM 1503 03.99 (P04C14)

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ANNEXE AU RAPPORT DE RECHERCHE PRÉLIMINAIRE RELATIF A LA DEMANDE DE BREVET FRANÇAIS NO. FR 0109715 FA 609582

La présente annexe indique les membres de la famille de brevets relatifs aux documents brevets cités dans le rapport de recherche préliminaire visé ci-dessus.
Les dits membres sont contenus au fichier informatique de l'Office européen des brevets à la date du 14-05-2002
Les renseignements fournis sont donnés à titre indicatif et n'engagent pas la responsabilité de l'Office européen des brevets, ni de l'Administration française

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EPO FORM P0499

Pour tout renseignement concernant cette annexe : voir Journal Officiel de l'Office européen des brevets, No.12/82

SAMSUNG EX. 1002 - 304/4148

(12) UK Patent Application (19) GB (11) 2 030 766 A

(21) Application No **7930141**
(22) Date of filing
30 Aug 1979
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30 Aug 1979
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(31) **78/35406**
(32) **2 Sep 1978**
(33) **United Kingdom (GB)**
(43) Application published
10 Apr 1980
(51) **INT CL³ H01L 21/268**
31/06
(52) Domestic classification
H1K 1EA 1EB 2R3X
2S20 2S6 3F 3R1 9C2
9C3 9L 9R1 LCX
(56) Documents cited
GB 1477670
GB 1258657
GB 1176889
(58) Field of search
H1K
(71) Applicant
The Plessey Company Limited
Vicarage Lane
Ilford
Essex
(72) Inventors
Ricardo Simon Sussmann
Allen William Mabbitt
(74) Agents
C Goodman

(54) **Laser treatment of semiconductor material**

(57) A layer or layers of amorphous material deposited on a non-crystalline amorphous substrate are subjected to treatment by exposure to a laser beam. The treatment may either recrystallise or anneal the amorphous material depending on the laser power and improves its suitability for such devices as solar cells by improving the life times and diffusion lengths within the material as compared to the untreated material.

The use of P type SiC or polycrystalline silicon on superposed i and n type amorphous silicon layers to improve the transmissivity of the outer layers of solar cells, and the use of varying composition SiC layers for visible light emission devices are also disclosed.

GB 2 030 766 A

The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

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SAMSUNG EX. 1002 - 305/4148

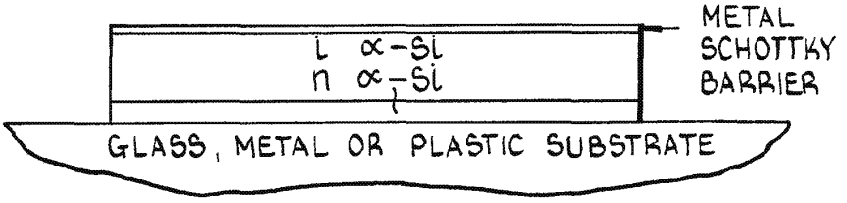


FIG. 1.

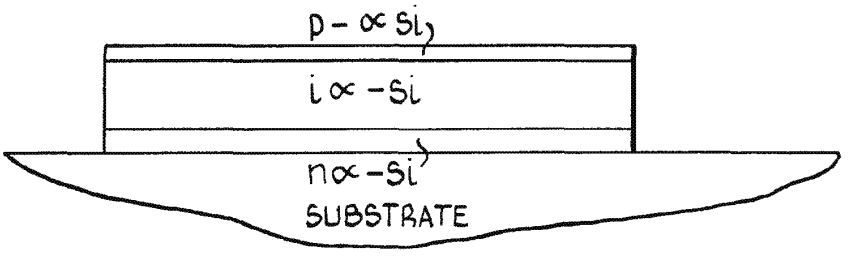


FIG. 2.

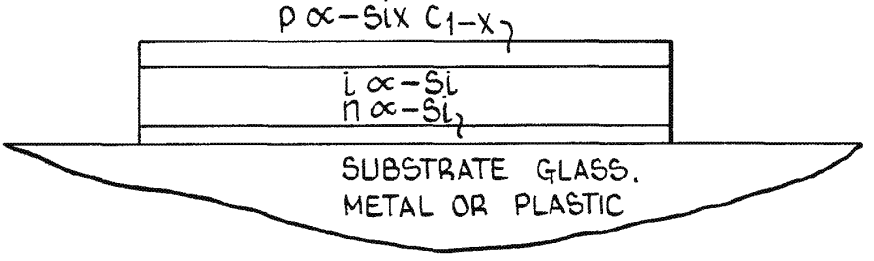


FIG. 3.

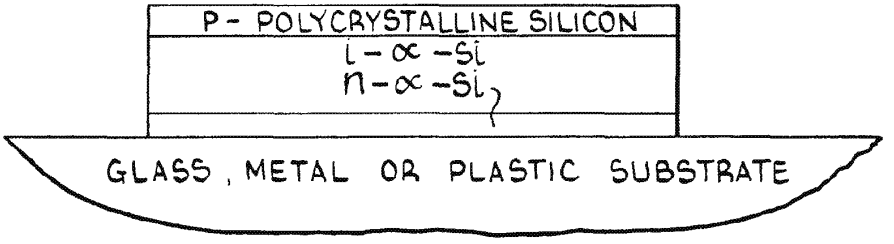


FIG. 4.

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SPECIFICATION

Improvements in or relating to solar cells and other devices.

The present invention relates to method of treatment of amorphous material layers to make them more suitable for the production of solar cells and other similar devices and to the solar cells and or other devices produced using the treated materials.

The possible use of thin film amorphous materials for solar cells, (or other devices such as p–n junctions, Schottky diodes, zener diodes) integrated into large area systems such as displays is extremely attractive due to the relatively low cost in terms of materials and energy. A disadvantage however, is that device performance has previously been severely limited by the short life times and diffusion lengths typical of amorphous materials. For example, the present state of the art A.M.I. efficiencies for polycrystalline silicon solar cells is about 10% which is a factor of 2 higher than the best cell produced with amorophous material.

It is an object of the present invention to produce a treated layer of amorphous material which is substantially superior to that known at present and thus to be able to combine the advantages in terms of the low cost and large area capability of amorphous thin film with the superior device performance of the polycrystalline material.

According to the present invention there is provided a method of treating one or more layers of amorphous material deposited on a non-crystalline substrate, to improve the suitability of the material for use in solar cells or similar devices as hereinbefore defined, by subjecting the layer of amorphous material to exposure by a laser.

The present invention also provides an amorphous silicon solar cell comprising an upper layer of p type Si_xC_{1-x} an intermediate layer of i_x–Si and a lower layer of n Si on a suitable substrate.

The invention also provides an amorphous silicon solar cell comprising an upper layer of p type polycrystalline silicon an intermediate layer of i –Si and a lower layer of n Si on a suitable substrate.

In a preferred embodiment the amorphous material is silicon.

Embodiments of the present invention will now be described, by way of example with reference to the accompanying drawings, in which:

Figure 1 shows a conventional schottky barrier cell,

Figure 2 shows a conventional P–i–n barrier cell,

Figure 3 shows a first solar cell heterostructure according to the present invention and,

Figure 4 shows a second solar cell structure according to the present invention.

An amorphous silicon layer or multi-layer amorphous structure of 6,000Å was grown on an amorphous non-crystalline substrate e.g. glass, metallised glass or stainless steel by known methods, for example the glow discharge decomposition of SiH_4 or by sputtering. The amorphous layer or layers are then subjected to exposure by a suitable laser. The effect of the exposure to the laser is either to crystallise a controlled thickness of the amorphous structure when a high power is used to anneal the amorphous layer when a lower power is used.

The recrystallised layer possesses optical and electronic properties which make it more suitable as part of a solar cell, p–n junction or other devices.

In the case of the annealed, non-recystallised layer the properties will tend to reduce the density of the defect states in the gap.

Referring now to the drawings current practise when using amorphous-silicon (α– Si) for solar cells is to use p–i–n or Schottky barrier – i – n structures, as shown in Figs. 1 and 2. These approaches limit the attainable solar conversion efficiency, for any quality *i*–Si, because of the p layer or metal Schottky barrier prevents a large proportion of the incident light from reaching the depleted *i* region. If these surface layers could be replaced by a relatively optically transparent material, which still forms an electrically active junction, then the device efficiency would be improved.

This invention replaces the pα –Si or metal Schottky barrier with an amorphous layer of 'p' type Si_xC_{1-x} in which 0×1 as shown in Fig. 3. Amorphous $S1_xC_{1-x}$ forms a continuous series of solid solutions with a bandgap that increases as x decreases, thus a larger fraction of the incident light reaches the junction depletion than with conventional structures. This application therfore provides a heterojunction α–SiC/Si structure.

Further uses of this concept includes

$Si_xC_{1-x}/Si_yC_{1-y}/Si_xC_{1-x}$/glass/metal

or plastic substrate structures for visible light emission which would have applications for flat panel displays.

Referring now to Fig. 4 a second preferred solar cell according to the present invention is shown. Current amorphous silicon solar cells are limited in efficiency because of absorption or reflection of light by the top pα–Si or metal Schottky barrier layer. The solar cell shown in Fig. 4 reduces the wastage of input photons by forming a p–n junction between p-type polycrystalline silicon and the conventional i–nα–Si layers as shown in Figs. 1 and 2. The cell is therefore more efficient than previously known solar cells.

In the above shown solar cells suitable front

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and rear contact metallisations are applied to realise a working structure.

CLAIMS

1. A method of treating one or more layers of amorphous material deposited on a non-crystalline substrate, to improve the suitability of the material for use in solar cells or similar devices as hereinbefore defined by subjecting the layer of amorphous material to exposure by a laser.

2. A method of treating one or more layers of amorphous material as claimed in claim 1 in which the amorphous material is silicon, or hydrogenated amorphous silicon or silicon carbide or gallium arsenide or gallium phosphide.

3. A method of treating one or more layers of amorphous material as claimed in claim 2 in which the amorphous silicon or hydrogenated amorphous silicon is deposited on the amorphous substrate using the glow discharge decomposition of SiH_4.

4. A method of treating one or more layers of amorphous material as claimed in any one of the preceding claims in which the exposure is at a low enough level so that the material is not recrystallised but is annealed so as to reduce the number of defect states in the gap with a consequent improvement in lifetime and diffusion lengths.

5. A method of treating one or more layers of amorphous material as claimed in any one of the preceding claims in which the exposure is at a level high enough to recrystallise at least one layer of the amorphous material.

6. A method of treating one or more layers of amorphous material substantially as described.

7. An amorphous silicon solar cell comprising an upper layer of p type Si_xC_{1-x}, and intermediate layer of iα–Si and a lower layer of nαSi mounted on a suitable substrate.

8. An amorphous silicon solar cell comprising an upper layer of p type polycrystalline silicon an intermediate layer of iα–Si and a lower layer of nαSi mounted on a suitable substrate.

9. An amorphous silicon solar cell substantially as described with reference to Fig. 3 or 4 of the accompanying drawings.

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Espacenet

Bibliographic data: JPH04318970 (A) — 1992-11-10

MANUFACTURE OF PHOTOSENSOR

Inventor(s): ENDO YUTARO ± (ENDO YUTARO)

Applicant(s): MITSUBISHI ELECTRIC CORP ± (MITSUBISHI ELECTRIC CORP)

Classification: **- international:** ***H01L27/14; H01L31/00;*** (IPC1-7): H01L27/14; H01L31/00

- cooperative:

Application number: JP19910085162 19910417

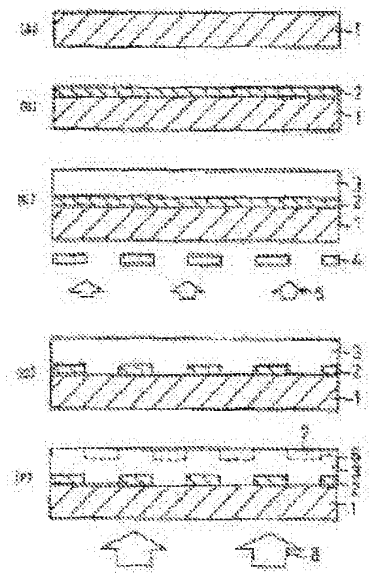
Priority number(s): JP19910085162 19910417

Abstract of JPH04318970 (A)

PURPOSE:To easily manufacture a photosensor having a crosstalk preventive light absorption layer at a lower part between pixels without using complicate photoengraving, etching on the way of a growth. CONSTITUTION:After an HgTe layer 2, a p-type CdHgTe layer 3 are sequentially grown on a CdTe substrate 1, only the layer 2 disposed at a lower part of a region formed of pixels is irradiated with a YAG laser 5 from a lower surface side of the substrate 1 to be absorbed to generate heat, the region is assimilated with the layer 3, and an n-type CdHgTe layer 7 to become a pixel is formed on the assimilated layer 3.

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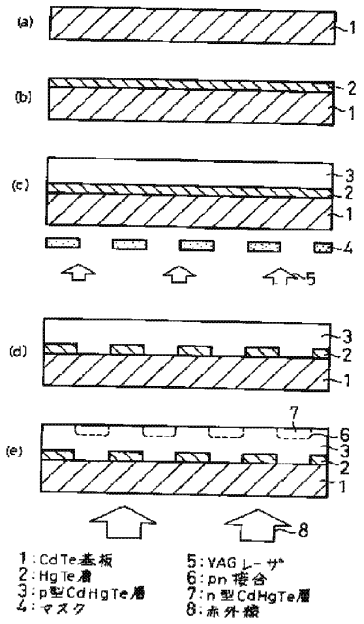
(74)代理人　弁理士　高田　守　(外１名)

(54)【発明の名称】　光検知装置の製造方法

(57)【要約】

【目的】　成長途中において，複雑な写真製版，エッチングを用いることなく，画素間の下部にクロストーク防止用の光吸収層を備えた光検知装置の製造を容易にする。

【構成】　ＣｄＴｅ基板１上にＨｇＴｅ層２，ｐ型ＣｄＨｇＴｅ層３を順次成長させた後，ＣｄＴｅ基板１の下面側から画素が構成される領域の下部に位置するＨｇＴｅ層２のみにＹＡＧレーザ５を照射して吸収，発熱させ，この領域をｐ型ＣｄＨｇＴｅ層３に同化させ，この同化されたｐ型ＣｄＨｇＴｅ層３上に画素となるｎ型ＣｄＨｇＴｅ層７を形成することを特徴としている。



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【特許請求の範囲】

【請求項１】基板上に光吸収層を成長させる工程と、この光吸収層上に複数の画素が構成される光電変換層を成長させる工程と、前記基板の下面側から前記画素が構成される領域の下部に位置する光吸収層のみにレーザ光を照射して前記光吸収層に吸収，発熱させ、この領域の光吸収層を前記光電変換層に同化させる工程と、前記光電変換層内にｐｎ接合を形成して前記画素を形成する工程とを含むことを特徴とする光検知装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、アレイ状の受光部を持つ背面入射型の光検知装置の製造方法に関し、特にその各画素のクロストーク防止に関するものである。

【０００２】

【従来の技術】図３（ａ）～（ｅ）は従来の光検知装置の製造方法を示す側断面図であり、図において、１はＣｄＴｃ基板、２は赤外線吸収層としてのＨｇＴｃ層、３は光電変換層としてのｐ型ＣｄＨｇＴｅ層、６はｐｎ接合、７は画素を構成するｎ型ＣｄＨｇＴｅ層、８は赤外線である。

【０００３】次に、動作について説明する。まず、アレイ状の受光部を持つ背面入射型の光検知装置の問題点の１つであるクロストークについて図４を用いて説明する。図４は、図３（ｃ）の光検知装置からＨｇＴｃ層２を取り除いた場合を示す図であり、７ａ，７ｂはｎ型ＣｄＨｇＴｅ層、９はキャリアである。まず、ＣｄＴｅ基板１側から入射した赤外線８は、ｐ型ＣｄＨｇＴｅ層３で吸収され、キャリア９を発生する。このキャリア９がｎ型ＣｄＨｇＴｅ層７ａ，７ｂ付近のｐｎ接合６に到達すると光電流となり、光を検知できる。しかし、図のように隣接した画素間に入射した光によって発生したキャリア９の拡散長は、画素を高密度に構成すればするほど、画素ピッチに比べて長くなり、ｎ型ＣｄＨｇＴｅ層７ａ，７ｂのいずれの画素にも到達可能となり、クロストークが生じる。このため、図３（ｅ）に示すように、画素間に光が入射しないように赤外線吸収層としてのＨｇＴｅ層２を設けて画素間でキャリア９が生じないように構成している。ここで、赤外線吸収層としてＨｇＴｅ層２が用いられる理由は、零ギャップ半導体であり、赤外線の吸収効率が良いからである。

【０００４】次に、ＨｇＴｅ層２を設けた光検知装置の製造方法について図３に従って説明する。まず、図３（ａ）に示すＣｄＴｅ基板１上に赤外線吸収層となるＨｇＴｅ層２を図３（ｂ）に示すように、エピタキシャルイ成長させる。次いで、画素となるｎ型ＣｄＨｇＴｅ層７を選択的に作るマスクと、これを反転したマスクを用いて写真製版を行い、エッチング技術を用いて図３（ｃ）に示す形状のＨｇＴｅ層２を形成する。次いで、図３（ｄ）に示すように、ｐ型ＣｄＨｇＴｅ層３をエピタキシャル成長させた後、Ｈｇ拡散あるいはイオン注入技術のいずれかを用いてＨｇＴｅ層２と重ならない部分に図３（ｅ）に示すようにｎ型ＣｄＨｇＴｅ層７を形成する。

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【０００５】

【発明が解決しようとする課題】上記のような従来の光検知装置の製造方法では、赤外線吸収層となるＨｇＴｅ層２，ｐ型ＣｄＨｇＴｅ層３を形成するために２度のエピタキシャル成長を行わなければならないうえ、ｐ型ＣｄＨｇＴｅ層３を形成する２度目のエピタキシャル成長では、ＨｇＴｅ層２を写真製版，エッチング技術を用いて赤外線吸収層となるパターンに形成した後、この段差のできたＨｇＴｅ層２上にエピタキシャル成長させなければならず、プロセスが複雑であるという問題点があった。

【０００６】本発明は、上記のような問題点を解消するためになされたもので、赤外線吸収層を形成するための写真製版，エッチング技術を省略できるうえ、段差上へのエピタキシャル成長工程を用いることもなく、クロストークを防止するための赤外線吸収層を設けた光検知装置を得ることが可能な光検知装置の製造方法を得ることを目的とする。

【０００７】

【課題を解決するための手段】本発明に係る光検知装置の製造方法は、基板上に光吸収層を成長させる工程と、この光吸収層上に複数の画素が構成される光電変換層を成長させる工程と、基板の下面側から画素が構成される領域の下部に位置する光吸収層のみにレーザ光を照射して光吸収層に吸収，発熱させ、この領域の光吸収層を光電変換層に同化させる工程と、光電変換層内にｐｎ接合を形成して画素を形成する工程とを含むものである。

【０００８】

【作用】本発明においては、基板上に光吸収層，光電変換層が順次成長された後、基板の下面側からのレーザ光の照射によって画素が構成される領域下の光吸収層のみが加熱されて光電変換層と同化され、この同化された領域上に画素が構成される。

【０００９】

【実施例】以下、本発明の一実施例を図について説明する。図１（ａ）～（ｅ）は本発明の光検知装置の製造方法の一実施例を示す側断面図であり、図２は、図１（ｅ）においてｐ型ＣｄＨｇＴｅ層３を一部除去した状態の図である。これらの図において、図３と同一符号は同一のものを示し、４はマスク、５はＹＡＧレーザである。

【００１０】次に、本発明による光検知装置の製造方法について説明する。まず、図１（ａ）に示すＣｄＴｅ基板１上に１．５μｍ程度の赤外線吸収層（光吸収層）としてのＨｇＴｅ層２を、図１（ｂ）に示すように、エピタキシャル成長させ、次いで、このＨｇＴｅ層２上に光

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電変換層としてのｐ型ＣｄＨｇＴｅ部３を図１（ｃ）に示すように、エピタキシャル成長させる。次に、ＣｄＴｅ基板１側からｎ型ＣｄＨｇＴｅ層７形成のための写真製版に用いるマスクを反転したパターンのメタルマスクをマスクとして、画素となるｎ型ＣｄＨｇＴｅ層７を形成する領域の下部に位置するＨｇＴｅ層２のみにＣｄＴｅ基板１に吸収されにくいＹＡＧレーザ５を照射し、照射されたＨｇＴｅ層２付近の温度が４００℃程度になるように吸収，発熱させる。これにより、ＨｇＴｅ層２とＣｄＴｅ基板１とが相互拡散され、図１（ｄ）に示すように、ＨｇＴｅ層２はｐ型ＣｄＨｇＴｅ層３に同化される。この場合、ＨｇＴｅは零ギャップ半導体であるため、光を吸収しやすくなっている。ＹＡＧレーザ５の照射方法もマスク４を用いず所定のパターンで走査してもよい。すなわち、クロストーク防止層となる赤外線吸収層が画素以外の領域に形成されたことになり、この後、従来技術と同様にＨｇ拡散，不純物拡散あるいはイオン注入技術等を用いて、図１（ｃ）に示すように、ｎ型ＣｄＨｇＴｅ層７を形成すれば画素部が完成する。

【００１１】なお、上記実施例では基板１にＣｄＴｅを、赤外線吸収層２にＨｇＴｅを、画素部を有する第１導電型の半導体層にＣｄＨｇＴｅを用いたが、基板材料にはＣｄｙ Ｚｎ1-ｙ Ｔｅ（０．０５≦ｙ＜１）ＧａＡｓ等、赤外線吸収層はＣｄＨｇＴｅ等、第１の導電型の半導体層よりもＣｄ量が少ないものもしくは同じものなら何でも良い。また、半導体層としては、ＺｎＨｇＴｅ，ＰｂＳｎＴｅ等のほか、ＣｄＴｅとＨｇＴｅの超格子層を用いても良い。

【００１２】また、上記実施例では、赤外線を検知する場合について述べたが、本発明は可視光，赤外線，紫外線，放射線の検出器にも利用できることはいうまでもない。また、赤外線吸収層２にＨｇＴｅを用いた場合、ＹＡＧレーザ５の替わりに０．８６μｍより長い波長光なら何を用いても同様の効果を有し、ＣｄＨｇＴｅ（第１の導電型の半導体層よりもＣｄ量が少ないもの）を用いた場合は、０．８６μｍより大きく検出光（１０μｍ程度）より小さな波長領域のものであれば何を用いても同様の効果を有する。

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【００１３】

【発明の効果】以上説明したように、本発明は基板上に光吸収層を成長させる工程と、この光吸収層上に複数の画素が構成される光電変換層を成長させる工程と、基板の下面側から画素が構成される領域の下部に位置する光吸収層のみにレーザ光を照射して光吸収層に吸収，発熱させ、この領域の光吸収層を光電変換層に同化させる工程と、光電変換層内にｐｎ接合を形成して画素を形成する工程とを含むので、画素間の下部に選択的に光吸収層を形成する際に従来のような写真製版，エッチング技術を途中の工程で用いながら２回に分けて結晶成長を行う必要がなくなり、簡単な工程で歩留りよく光検知を得ることができるという効果がある。

【図面の簡単な説明】

【図１】本発明の光検知装置の製造方法の一実施例を示す側断面図である。

【図２】図１で製造された光検知装置の一部を取り除いた状態の斜視図である。

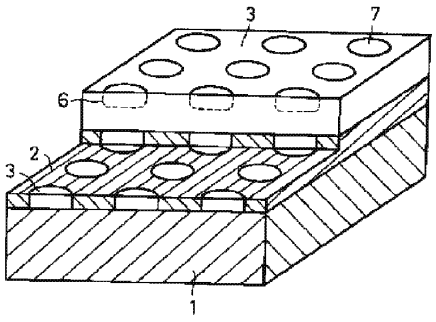
【図３】従来の光検知装置の製造方法を示す側断面図である。

【図４】従来の光検知装置のクロストークについて説明するための側断面図である。

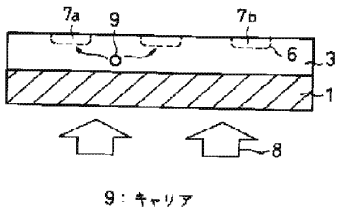
【符号の説明】

１　ＣｄＴｅ基板
２　ＨｇＴｅ層
３　ｐ型ＣｄＨｇＴｅ層
４　マスク
５　ＹＡＧレーザ
６　ｐｎ接合
７　ｎ型ＣｄＨｇＴｅ層
８　赤外線
９　キャリア

【図２】



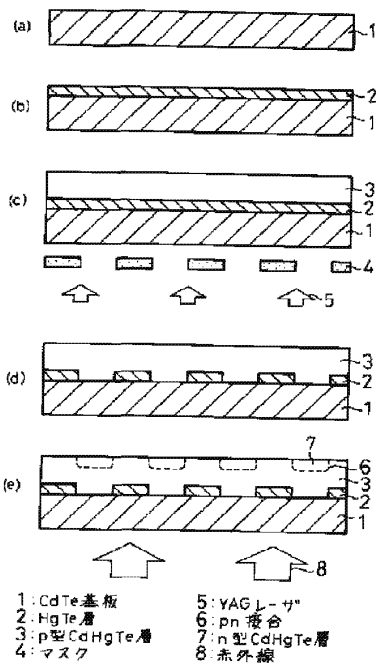
【図４】



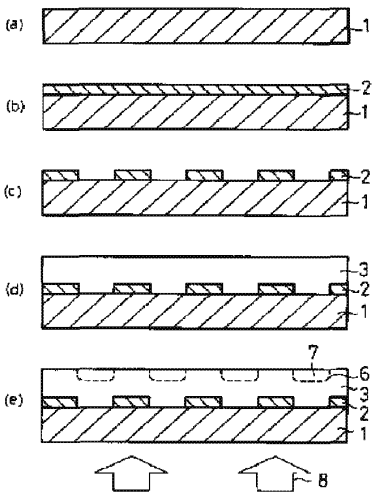
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【図１】



【図３】



【手続補正書】
【提出日】平成４年３月４日
【手続補正１】
【補正対象書類名】明細書
【補正対象項目名】００１１
【補正方法】変更
【補正内容】
【００１１】なお、上記実施例では基板１にＣｄＴｅを、赤外線吸収層２にＨｇＴｅを、画素部を有する第１導電型の半導体層にＣｄＨｇＴｅを用いたが、基板材料にはＣｄ，$Zn_{1-y}Te$（０．０５≦ｙ＜１），ＧａＡｓ等、赤外線吸収層はＣｄＨｇＴｅ等、第１の導電型の半導体層よりもＣｄ量が少ないものもしくは同じものなら何でも良い。また、半導体層としては、ＺｎＨｇＴｅ，ＰｂＳｎＴｅ等のほか、ＣｄＴｅとＨｇＴｅの超格子層を用いても良い。

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Espacenet

Bibliographic data: JPS57173966 (A) — 1982-10-26

SOLID STATE IMAGE PICKUP DEVICE

Inventor(s): KAWAJIRI KAZUHIRO; MIZOBUCHI YUUZOU; SAITOU MITSUO ± (KAWAJIRI KAZUHIRO, ; MIZOBUCHI YUUZOU, ; SAITOU MITSUO, ; MIZOBUCHI JUZO, ; SAITO MITSUO)

Applicant(s): FUJI PHOTO FILM CO LTD ± (FUJI SHASHIN FILM KK, ; FUJI PHOTO FILM CO LTD)

Classification: - international:***H01L27/146; H04N5/335; H04N5/369; H04N5/372; H04N5/374;*** (IPC1-7): H01L27/14; H04N5/30
- cooperative: **H01L27/14665**

Application number: JP19810059612 19810420

Priority number (s): JP19810059612 19810420

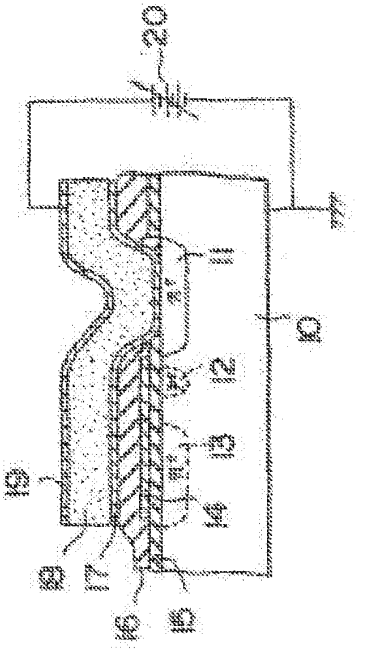
Also published as: JPH023552 (B2)

Abstract of JPS57173966 (A)

PURPOSE:To manufacture an inexpensive, high efficiency optical image pickup device by a method wherein a photodetector layer and electrodes are formed of amorphous Si in a solid state image pickup device with a photodetector on a semiconductor substrate provided with a scanning circuit. CONSTITUTION:An n<+> type region 11 is provided for the formation of a diode and, at the same time, a scanning circuit forming p<+> type region 12 (CCD) or an n<+> type region 13 (BBD) are formed on a p type semiconductor substrate 10. A gate electrode 14 is built on the substrate 10 across an insulator film 15 and an insulator layer 16 is laid on the electrode 14. Next, on the substrate 10, a diode electrode 17, and a photodetecting layer 18 and a transparent electrode 19 forming a photoconductive layer or photodiode or phototransistor are provided on the substrate 10.; The electrode 17, photodetector 18, and transparent electrode 19 are composed of amorphous Si and formed in an uninterrupted process.

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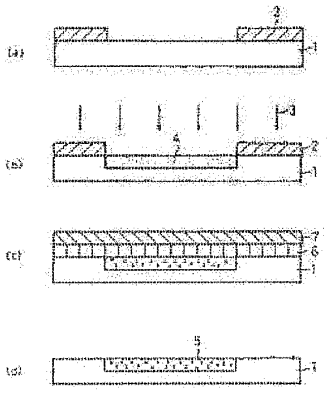
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MANUFACTURE OF SEMICONDUCTOR DEVICE

Publication number: JP63116421 (A)
Publication date: 1988-05-20
Inventor(s): OSAWA MASARU +
Applicant(s): MITSUBISHI ELECTRIC CORP +
Classification:
- international: ***H01L21/265; H01L21/324;*** **H01L21/02**; (IPC1-7): H01L21/265; H01L21/324
- European:
Application number: JP19860263160 19861105
Priority number(s): JP19860263160 19861105

Abstract of **JP 63116421 (A)**

PURPOSE:To prevent As from oozing from a GaAs substrate thereby to obtain a semiconductor device having good characteristics by depositing an amorphous As layer on an ion implanted surface as is after implanting, continuously depositing an insulating layer on the surface of the amorphous As layer, and then annealing it. CONSTITUTION:An active layer forming photoresist pattern 2 is formed by photocomposing technique on a GaAs substrate 1. Si<+29> ions 3 are implanted to form an ion implanted region 4. It is dipped in acetone to remove the pattern 2, and an a-As layer 6 and an insulating layer 7 are continuously deposited by a CVD method on the ion 3 implanted surface. It is heat treated at 800 deg.C for 40 min in a reducing atmosphere to obtain a highly activated active layer 5. It is dipped in a fluoric acid to remove the insulating layer, and dipped in a hydrochloric acid to remove the layer 6 to thereby expose the surface of the substrate 1. Thus, it can prevent As from oozing from the substrate 1 to obtain a semiconductor device having good characteristics.



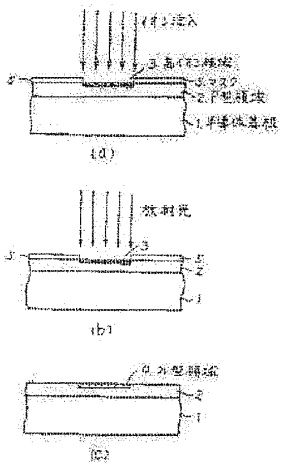
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MANUFACTURE OF SEMICONDUCTOR DEVICE

Publication number: JP2152226 (A)
Publication date: 1990-06-12
Inventor(s): SUGITA YOSHIHIRO +
Applicant(s): FUJITSU LTD +
Classification:
- international: ***H01L21/22; H01L21/26; H01L21/265; H01L21/316;*** **H01L21/02;** (IPC1-7): H01L21/22; H01L21/26; H01L21/265; H01L21/316
- European:
Application number: JP19880306346 19881202
Priority number(s): JP19880306346 19881202

Abstract of **JP 2152226 (A)**

PURPOSE:To heat the extreme surface of an element formation region and to activate this region by a method wherein the element formation region of a semiconductor is irradiated with a non-coherent radiated beam having a continuous spectrum of a soft X-ray region from an extreme vacuum ultraviolet- ray region. CONSTITUTION:A mask 5 is formed on a p-type region 2 formed on a semiconductor substrate 1; n-type impurity ions, e.g. phosphorus ions (P<+>), are implanted very shallowly, e.g. down to a depth of about 50nm, from the upper part; a high-ion region 3 is formed. The high-ion region 3 is irradiated with a synchrotron radiation having a continuous spectrum of a soft X-ray region from an extreme vacuum ultraviolet-ray region. The high-ion region 3 is heated and activated; an n-type region 4 is formed; the mask 5 is removed.



Data supplied from the ***espacenet*** database — Worldwide

⑲日本国特許庁(JP)　⑪特許出願公開

⑫公開特許公報(A)　平2−152226

⑤Int.Cl.⁵	識別記号	庁内整理番号	㊸公開　平成2年(1990)6月12日
H 01 L 21/26	L	7738−5F	
21/22	E	7738−5F	
21/265			
21/316	S	6810−5F	
		7522−5F　H 01 L 21/265	B

審査請求　未請求　請求項の数 1　(全4頁)

㊹発明の名称　半導体装置の製造方法

㉑特　願　昭63−306346
㉒出　願　昭63(1988)12月2日

㉒発明者　杉田　義博　神奈川県川崎市中原区上小田中1015番地　富士通株式会社内
㉑出願人　富士通株式会社　神奈川県川崎市中原区上小田中1015番地
㉔代理人　弁理士　井桁　貞一

明　細　書

1．発明の名称

半導体装置の製造方法

2．特許請求の範囲

極真空紫外光領域から軟X線領域の連続スペクトルを持つ非干渉性の放射光を半導体の素子形成領域に照射することにより，該素子形成領域の極表面を加熱して活性化する工程を含むことを特徴とする半導体装置の製造方法。

3．発明の詳細な説明

〔概要〕

半導体装置の製造方法に係り，特に半導体装置の素子形成領域の表面加熱方法に関し，

半導体装置の素子形成領域の表面に極めて薄い活性領域を形成することを目的とし，

極真空紫外光領域から軟X線領域の連続スペクトルを持つ非干渉性の放射光を半導体の素子形成領域に照射することにより，該素子形成領域の極表面を加熱して活性化する工程を含む半導体装置の製造方法により構成する。

〔産業上の利用分野〕

本発明は半導体装置の製造方法に係り，特に半導体装置の素子形成領域の表面加熱方法に関する。

半導体デバイスの微細化に伴い，浅い接合の形成技術や薄膜の活性化技術の開発が必要とされ，盛んに研究が行われている。

〔従来の技術〕

従来，紫外光を用いた半導体の極表面加熱法が試みられており，放電ランプによるラピッドサーマルアニール（Rapid Thermal Anneal）法や，それより短波長で出力密度の高いエキシマレーザを用いた方法が研究されている。

半導体の極表面加熱には，200 乃至300nm という短波長光を利用できるエキシマレーザは，ランプ光源よりも有望であるが，一方，光照射損傷によるデバイスの歩留り低下，信頼性低下を引き起

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こすおそれがある。

第5図（a），（b）は従来例としてレーザ光を用いる加熱の工程例を示し，1は半導体基板，2はp型領域，4はn型領域，5はマスク，6はドーピング原料を表す。以下，これらの図を参照しながら説明する。

第5図（a）参照

半導体基板1上に形成されたp型領域2上にマスク5を形成してその開口部にドーピング原料6を付着させる。ドーピング原料6はn型不純物を含むものであって，例えばフォスフィン（PH_3）である。

開口部の上からエキシマレーザによるレーザ光を照射してp型領域2の表面を加熱する。

第5図（b）参照

ドーピング原料6はp型領域2の中に拡散して極く薄いn型領域4が形成される。その後マスク5を除去する。

ところで，レーザ光を物質に照射した場合，光照射損傷のおそれがあり，その光照射損傷には熱的なものの他にレーザ光の単色性，可干渉性に起因するアバランシェ破壊がある。

第6図はレーザ光照射の場合の電界振幅を示す。

真空から物質に入射したレーザ光には界面を節とする定在波が立ち，表面から1／4波長入ったところで電界振幅は最大となる。したがって，その深さで電界集中が起こりアバランシェ破壊を生じ易くなる。

さらに，物質中にレーザ光特有の波長を吸収する吸収センタが含まれているとき，そこが熱発生源となって不均一な熱歪みが発生するといった問題もある。

〔発明が解決しようとする課題〕

従って，レーザ光による加熱の場合は表面を均一に加熱出来ないという問題，デバイスに局部的な損傷を与えるといった問題がある。

本発明は，上記の欠点を克服して，デバイスに損傷を与えることなく極めて薄い表面を均一に加熱し，極めて薄い活性領域を形成する方法を提供することを目的とする。

〔課題を解決するための手段〕

上記課題は，極真空紫外光領域から軟X線領域の連続スペクトルを持つ非干渉性の放射光を半導体の素子形成領域に照射することにより，該素子形成領域の極表面を加熱して活性化する工程を含む半導体装置の製造方法によって解決される。

〔作用〕

高速荷電粒子の制動放射光であるシンクロトロン放射光は，紫外線領域からX線領域までの連続光光源として知られ，結晶の分析評価に用いられている。その波長域はエキシマレーザでは達成できない数十nm域の極真空紫外光から1nm程度の軟X線を含む。

本発明では，かかる放射光を利用する。波長が短ければ物質への進入深さが浅くなり，極表面の加熱に有利となる。

さらに，シンクロトロン放射光を光源とした場合，利用できる光は広い範囲の連続光となり，しかも非干渉性であるので，レーザ光に見られる前記の欠点を避けることができる。

第4図に放射光照射の場合の電界振幅を示す。この場合は真空から物質への界面で干渉による定在波は発生せず，進入深さとともに電界振幅は漸減する。したがって，レーザ光を用いる場合のような1／4波長深さでのアバランシェ破壊といった現象は生じない。

したがって，シンクロトロン放射光のような放射光を用いれば半導体の素子形成領域を均一にしかもデバイスに損傷を与えることなく極表面だけ加熱して，そこを活性化することができる。

〔実施例〕

以下，本発明の実施例について説明する。

第1図（a）乃至（c）は実施例Iで，極く薄い接合を作成する工程の例であり，1は半導体基板，2はp型領域，3は高イオン領域，4はn型領域，5はマスクを表す。

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第1図（a）参照

半導体基板1上に形成されたp型領域2上にマスク5を形成し，上部からn型の不純物イオン，例えば燐イオン（P^+）を極く浅く例えば50nm程度の深さまで打ち込んで，高イオン領域3を形成する。

第1図（b）参照

極真空紫外線光領域から軟X線領域の連続スペクトルを有するシンクロトロン放射光を高イオン領域3に照射する。

第1図（c）参照

高イオン領域3は加熱され，活性加されてn型領域4を形成する。

マスク5を除去する。

第2図（a），（b）は実施例Ⅱで，極く薄い接合を作成する別の工程例であり，1は半導体基板，2はp型領域，4はn型領域，5はマスク，6はドーピング原料を表す。

第2図（a）参照

半導体基板1上に形成されたp型領域2上にマスク5を形成し，その開口部にn型の不純物を含むドーピング原料6として，例えばフォスフィン（PH_3）を吸着させる。あるいはドーピング原料雰囲気中に半導体基板1を配置する。

上部から極真空紫外線光領域から軟X線領域の連続スペクトルを有するシンクロトロン放射光を照射する。

第2図（b）参照

p型領域2の表面付近は加熱されて，ドーピング原料6の不純物イオンがp型領域2中に拡散して，極く浅いn型領域4が形成される。マスク5を除去する。

この実施例は，イオン注入過程がなく，また，光照射損傷もないため極めて結晶性の高いドーピング領域のn型領域4が形成される。

第3図（a），（b）は実施例Ⅲで，半導体基板上にドーパントを含む絶縁膜を作成する例であり，1はSi基板，6はドーピング原料，7はSiO_2膜，71はドーパントを含むSiO_2膜を表す。

第3図（a）参照

半導体基板1として，例えばSi基板を用い，表面に熱酸化により厚さ約50nmのSiO_2膜7を形成する。

不純物固着トラップとして働く原子，例えば塩素（Cl）原子を含むドーピング原料6をSiO_2膜7上に吸着させる。あるいはドーピング原料雰囲気中にSi基板1を配置する。

上部から極真空紫外線光領域から軟X線領域の連続スペクトルを有するシンクロトロン放射光を照射する。

第3図（b）参照

SiO_2膜7は加熱されて塩素（Cl）原子を取込み，ドーパントを含むSiO_2膜71が形成される。

ドーパントを含むSiO_2膜71中の塩素（Cl）原子はSi基板1とドーパントを含むSiO_2膜71の界面に存在する重金属イオンを吸い寄せて固着する。

したがって，このように活性化された絶縁膜を用いればSi基板1の界面特性を改善することができる。

なお，極真空紫外線光領域以下の波長の放射光を用いることにより，従来のエキシマレーザ光では達成できない極めて浅い表面層を加熱することができるが，軟X線領域よりも短い波長では逆に侵入深さが大きくなって目的が達成されない。

〔発明の効果〕

以上説明した様に，本発明によれば，半導体装置の素子形成領域の極表面を均一にしかもデバイスに損傷を与えることなく加熱することができ，極く浅い接合や不純物トラップ機能を有する極く薄い絶縁膜等の活性領域を形成することができ，半導体デバイスの微細化，高速化に寄与するところが大きい。

4．図面の簡単な説明

第1図は実施例Ⅰ，

第2図は実施例Ⅱ，

第3図は実施例Ⅲ，

第4図は放射光照射の場合の電界振幅，

第5図は従来例，

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第6図はレーザ光照射の場合の電界振幅である。図において，

1は半導体基板であってSi基板，

2はp型領域，

3は高イオン領域，

4はn型領域，

5はマスク，

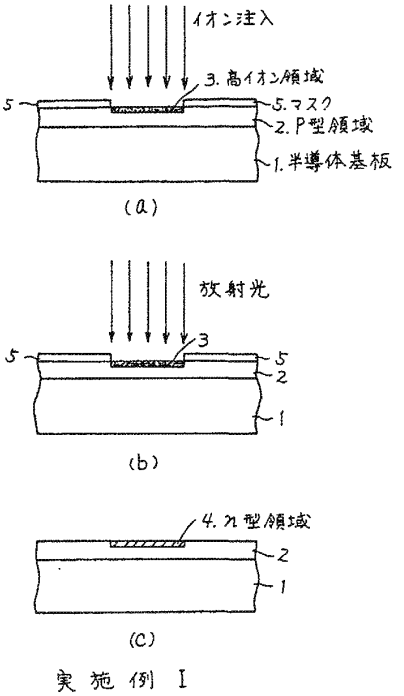
6はドーピング原料，

7は絶縁膜であってSiO_2膜，

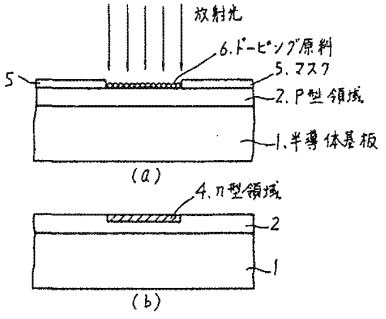
71はドーパントを含むSiO_2膜

を表す。

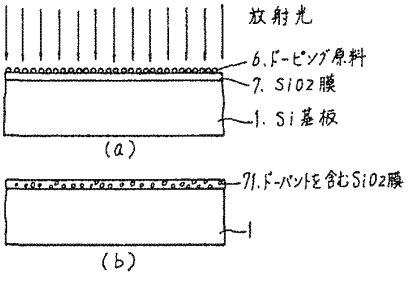
代理人　弁理士　井桁貞一



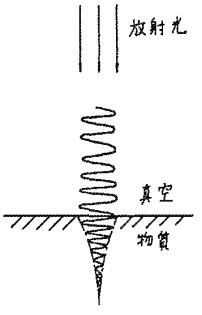
実施例 I
第1図



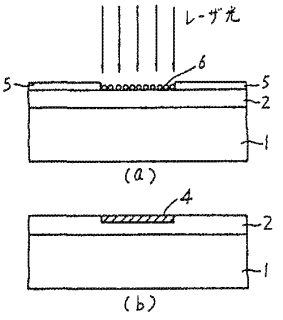
実施例 II
第2図



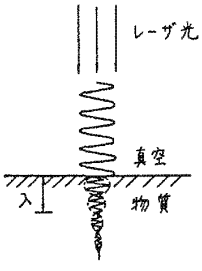
実施例 III
第3図



放射光照射の場合の電界振幅
第4図



従来例
第5図



レーザ光照射の場合の電界振幅
第6図

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Espacenet

Bibliographic data: JPH02237026 (A) — 1990-09-19

MANUFACTURE OF SEMICONDUCTOR DEVICE

Inventor(s): SUMI HIROBUMI; NOGUCHI TAKASHI ± (SUMI HIROBUMI, ; NOGUCHI TAKASHI)

Applicant(s): SONY CORP ± (SONY CORP, ; SONII KK)

Classification: - international: ***H01L21/28; H01L21/3205; H01L21/336; H01L23/52; H01L29/78;*** (IPC1-7): H01L21/28; H01L21/3205; H01L21/336; H01L29/784
- cooperative: H01L2924/0002 more

Application number: JP19890057571 19890309

Priority number (s): JP19890057571 19890309

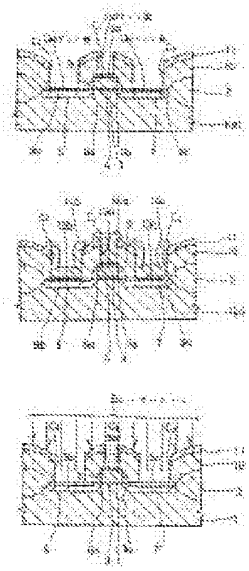
Also published as: JP2864518 (B2)

Abstract of JPH02237026 (A)

PURPOSE:To reduce junction leakage current, contact resistance and sheet resistance by a method wherein a high melting point metallic silicide film is irradiated with specific laser beams in an atmosphere containing N to form a high melting point nitride film. CONSTITUTION:The surface of an interlayer insulating film 10 excluding the parts of contact holes C1 to C3 is covered with a reflection film 11 and then the whole surface is irradiated with laser beams B in an atmosphere containing N so that only TiSi2 films 9a to 9c inside these contact holes C1 to C3 may be locally heated at high temperature. Accordingly, TiN films 13a to 13c can be formed in self-alignment with these contact holes C1 to C3 on the TiSi2 films 9a to 9c.; In this case, the parts not irradiated with the laser beams B are not heated at high temperature so that the surface of the TiSi2 films 9a to 9c on the parts not nitrified may not be subjected to the deterioration in morphology even if any hillock is formed on the surface. Through these procedures, contact resistance, sheet resistance and leakage current can be kept small.

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⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　平2−237026

⑤1Int.Cl.⁵	識別記号	庁内整理番号	⑬公開　平成2年(1990)9月19日
H 01 L 21/28	301 T	7738−5F	
	R	7738−5F	
21/3205			
21/336			
29/784			
		8422−5F	H 01 L 29/78　301 P
		6810−5F	21/88　Q

審査請求　未請求　請求項の数 1　（全7頁）

⑤4発明の名称　半導体装置の製造方法

⑳特　願　平1−57571
㉒出　願　平1(1989)3月9日

⑦2発明者　角　博文　東京都品川区北品川6丁目7番35号　ソニー株式会社内
⑦2発明者　野口　隆　東京都品川区北品川6丁目7番35号　ソニー株式会社内
⑦1出願人　ソニー株式会社　東京都品川区北品川6丁目7番35号
⑦4代理人　弁理士　志賀　富士弥　外1名

明　細　書

1．発明の名称

半導体装置の製造方法

2．特許請求の範囲

（1）高融点金属シリサイド膜と、該高融点金属シリサイド膜上に形成された高融点金属窒化物膜とを有する半導体装置の製造方法において、

N（窒素）を含む雰囲気中で前記高融点金属シリサイド膜に、エネルギー密度1400～2200mJ／cm²のレーザビームを選択的に照射することにより前記高融点金属窒化物膜を形成するようにしたことを特徴とする半導体装置の製造方法。

3．発明の詳細な説明

［産業上の利用分野］

本発明は、半導体装置の製造方法に関し、更に詳しくは、配線のコンタクト部に高融点金属シリサイド膜と高融点金属窒化物膜との二層構造の膜を有する半導体装置の製造方法に係るものである。

［発明の概要］

本発明は、高融点金属シリサイド膜と、該高融点金属シリサイド膜上に形成された高融点金属窒化物膜とを有する半導体装置の製造方法において、

N（窒素）を含む雰囲気中で前記高融点金属シリサイド膜に、エネルギー密度1400～2200mJ／cm²のレーザビームを選択的に照射することにより前記高融点金属窒化物膜を形成するようにしたことにより、

接合リーク電流，コンタクト抵抗及びシート抵抗を低くするようにしたのもである。

［従来の技術］

半導体装置においては、半導体基板中に形成された拡散層に、層間絶縁膜に形成されたコンタクトホールを通じてアルミニウム（Al）の配線がコンタクトしている。従来、この拡散層のシート抵抗の低減及びAl配線とこの拡散層との反応防止を図るために、例えばチタンシリサイド（$TiSi_2$）膜とその上に形成された窒化チタン（T

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ｉＮ）膜との二層構造の膜を介してＡｌ配線を拡散層にコンタクトさせる技術が知られている。

特開昭６２－１６９４１２号公報には、このＴｉＳｉ$_x$膜上にＴｉＮ膜を形成する方法として、拡散層上にＴｉＳｉ$_x$膜を形成した後に、窒素（Ｎ）を含む雰囲気中において９００℃以上の高温でアニールを行ってこのＴｉＳｉ$_x$膜の表面を窒化することによりＴｉＮ膜を形成する方法が開示されている。

［発明が解決しようとする課題］

しかしながら、上述の特開昭６２－１６９４１２号公報に開示された方法は、半導体基板全体が９００℃以上の高温に加熱されることに起因して、窒化されない部分におけるＴｉＳｉ$_x$膜の表面のモフォロジー（morphology）が劣化し、その結果、電気的特性の劣化が生じてしまうという問題点があった。また、特に、近年素子の微細化に伴ってソース・ドレイン領域の深さ寸法（x_j）が浅くなっているため、このように半導体基板全体が高温に加熱されることにより、拡散層中の不純物の再拡散が生じて拡散層が広がってしまうという問題もあった。

本発明は、このような従来の問題点に着目して創案されたものであって、高融点金属シリサイド膜のモフォロジーの劣化や不純物の再拡散を生じることなく高融点金属窒化物膜を高融点金属シリサイド膜上に形成可能とすると共に、接合リーク電流，コンタクト抵抗及びシート抵抗を低減化させることを可能にする半導体装置の製造方法を得んとするものである。

［課題を解決するための手段］

そこで、本発明は、高融点金属シリサイド膜と、該高融点金属シリサイド膜上に形成された高融点金属窒化物膜とを有する半導体装置の製造方法において、Ｎ（窒素）を含む雰囲気中で前記高融点金属シリサイド膜に、エネルギー密度１４００～２２００ｍＪ／ｃｍ^{2}のレーザビームを選択的に照射することにより前記高融点金属窒化物膜を形成するようにしたことを、その解決手段としている。

［作用］

Ｎを含む雰囲気中で、レーザビームを選択的に照射することにより、高融点金属シリサイド膜の窒化を行うべき部分のみが局所的に高温に加熱されてこの部分に高融点金属窒化物膜が形成されるが、その他の部分は高温に加熱されない。このため、この窒化が行われない部分における高融点金属シリサイド膜の表面のモフォロジーの劣化や不純物の再拡散が生じるのを防止することが可能となる。また、レーザビームのエネルギー密度を１４００～２２００ｍＪ／ｃｍ^{2}とすることにより、コンタクト抵抗，シート抵抗及びリーク電流を低く保つことが可能となる。

［実施例］

以下、本発明に係る半導体装置の製造方法の詳細を図面に示す実施例に基づいて説明する。この実施例は、本発明をＭＯＳトランジスクの製造に適用した実施例である。

第１図Ａ～第１図Ｈは、本実施例の製造方法の工程を示す断面図である。

本実施例においては、第１図Ａに示すように、例えばｐ型のシリコン基板である半導体基板１の表面に例えばＳｉＯ$_2$膜のようなフィールド絶縁膜２を選択的に形成して素子間分離を行った後、このフィールド絶縁膜２で囲まれた活性領域の表面に例えば熱酸化により例えばＳｉＯ$_2$膜のようなゲート絶縁膜３を形成する。次に、このゲート絶縁膜３上に例えば不純物をドープした多結晶Ｓｉ膜を形成した後、これらの多結晶Ｓｉ膜及びゲート絶縁膜３をエッチングにより所定形状にパターンニングする。これによって、ゲート電極４が形成される。この後、このゲート電極４をマスクとして半導体基板１中に例えばリン（Ｐ）のようなｎ型不純物を低濃度にイオン注入する。次に、例えばＣＶＤにより全面に例えばＳｉＯ$_2$膜を形成した後、例えば反応性イオンエッチング（ＲＩ

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Ｅ）によりこのＳｉＯ₂膜を基板表面と垂直方向に異方性エッチングしてＳｉＯ₂から成る側壁（サイドウォールスペーサ）５を形成する。次に、この側壁５をマスクとして半導体基板１中に例えばヒ素（Ａｓ）のようなｎ型不純物を比較的高濃度にイオン注入する。これによって、例えばｎ⁺型のソース領域６及びドレイン領域７がゲート電極４に対して自己整合的に形成される。これらのゲート電極４、ソース領域６及びドレイン領域７により、ｎチャンネルＭＯＳＦＥＴが構成される。これらのソース領域６及びドレイン領域７は、側壁５の下方の部分に例えばｎ⁻型の低不純物濃度部６ａ，７ａを有しており、従ってこのｎチャンネルＭＯＳＦＥＴはこの低不純物濃度部７ａによりドレイン領域７の近傍の電界を緩和した、いわゆるＬＤＤ（Lightly Doped Drain）構造を有する。なお、このｎチャンネルＭＯＳＦＥＴは必ずしもＬＤＤ構造を有する必要はない。この後、アニールを行うことにより、イオン注入された不純物の電気的活性化を行う。

次に第１図Ｂに示すように、例えばスパッタや蒸着により全面チタン（Ｔｉ）膜８を形成する。

次に、例えば８００℃程度の温度でアニールを行うことにより、Ｔｉ膜８とこのＴｉ膜８が直接接しているゲート電極４、ソース領域６及びドレイン領域７とを反応させる。これによって、これらのゲート電極４、ソース領域６及びドレイン領域７の表面がシリサイド化される。この後、未反応のＴｉ膜８をエッチング除去する。このようにして、第１図Ｃに示すように、ゲート電極４、ソース領域６及びドレイン領域７の表面にそれぞれＴｉＳｉ₂膜９ａ～９ｃが形成される。これらのＴｉＳｉ₂膜９ａ～９ｃの膜厚は例えば１０００Å程度である。これらのＴｉＳｉ₂膜９ａ～９ｃにより、ゲート電極４、ソース領域６及びドレイン領域７のシート抵抗の低減を図ることができる。なお、上述のアニールは例えば赤外線（ＩＲ）アニールにより行うことも可能である。

次に第１図Ｄに示すように、例えばＣＶＤにより全面に例えばリンシリケートガラス（ＰＳＧ）膜のような層間絶縁膜１０を形成し、さらにこの層間絶縁膜１０の上に例えばスパッタや蒸膜により例えばＡｌ膜のような後述のレーザビームＢに対する反射膜１１を形成した後、リソグラフィーによりこの反射膜１１の上に所定形状のレジストパターン１２を形成する。

次に、このレジストパターン１２をマスクとして反射膜１１及び層間絶縁膜１０の所定部分を例えばＲＩＥによりエッチングして、第１図Ｅに示すようにコンタクトホールＣ₁～Ｃ₃を形成する。この後、レジストパターン１２を除去する。

次に第１図Ｆに示すように、Ｎを含む雰囲気、例えばＮ₂ガスやアンモニア（ＮＨ₃）ガス中（７００ｍ Ｔｏｒｒ）で全面にレーザビームＢを照射する。このレーザビームＢとしては、例えばＸｅＣｌエキシマーレーザのようなエキシマーレーザによるパルスレーザビーム（波長３０８ｎｍ）を用いることができる。この場合、レーザビームＢの照射エネルギー密度は１４００～２２００ｍＪ／ｃｍ²に設定する。そして、反射膜１１に入射したレーザビームＢは反射されるため、結果的に反射膜１１で覆われていないコンタクトホールＣ₁～Ｃ₃内部のＴｉＳｉ₂膜９ａ～９ｃにのみレーザビームＢが照射される。このレーザビームＢの照射によってコンタクトホールＣ₁～Ｃ₃内部のＴｉＳｉ₂膜９ａ～９ｃのみが局所的に高温に加熱され、この部分がレーザビームＢの照射により分解された雰囲気ガス中のＮによって所定深さまで窒化される。これによって、ＴｉＮ膜１３ａ～１３ｃがコンタクトホールＣ₁～Ｃ₃に対して自己整合的に形成される。これらのＴｉＮ膜１３ａ～１３ｃによって、後述の配線１４ａ～１４ｃとゲート電極４、ソース領域６及びドレイン領域７との反応を防止することができる。なお、この反応を効果的に防止するためには、これらのＴｉＮ膜１３ａ～１３ｃの厚さは例えば５００Å程度以上であるのが好ましい。

次に、例えばスパッタや蒸着により全面に例えばＡｌ膜を形成した後、このＡｌ膜をエッチングにより所定形状にパターンニングして第１図Ｈに

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示すように配線１４ａ～１４ｃを形成し、これによって目的とするＭＯＳＬＳＩを完成させる。

以上のように、この実施例によれば、コンタクトホールＣ₁～Ｃ₃の部分を除いた層間絶縁膜１０の表面を反射膜１１で覆い、この状態でＮを含む雰囲気中においてレーザビームＢを照射することによりこれらのコンタクトホールＣ₁～Ｃ₃の内部におけるＴｉＳｉ₂膜９ａ～９ｃのみを局所的に高温に加熱しているので、これらのコンタクトホールＣ₁～Ｃ₃の内部におけるＴｉＳｉ₂膜９ａ～９ｃの上にこれらのコンタクトホールＣ₁～Ｃ₃に対して自己整合的にＴｉＮ膜１３ａ～１３ｃを形成することができる。この場合、レーザビームＢが照射されない部分は高温に加熱されないので、窒化が行われない部分におけるＴｉＳｉ₂膜９ａ～９ｃの表面にヒロック（hillock）が形成されたりしてモフォロジーの劣化が生じることがなく、従って電気的特性の劣化は生じない。さらにまた、ソース領域６及びドレイン領域７中の不純物の再拡散が生じることのないので、これらのソース領域６及びドレイン領域７が広がることもない。

なお、第２図及び第３図は、上記実施例における方法により６００～７００Åの厚さのＴｉＳｉ₂膜に照射するエキシマレーザのエネルギー密度を変化させた場合のコンタクト抵抗及びシート抵抗を測定した結果を示すグラフである。なお、両図において示す矢印はエキシマレーザを照射しない場合の値を示している。また、第４図は、ｐ型ＭＯＳトランジスタにおけるリーク電流を、上記実施例によるエキシマレーザのエネルギー密度を変えて測定した結果を示すグラフである。なお、同図中矢印は、エキシマレーザを照射しない場合の値を示している。

これらグラフが示すように、コンタクト抵抗，シート抵抗及びリーク電流に対して、レーザ照射条件が大きく影響を及ぼすことが判る。例えばエキシマレーザのエネルギー密度が３０００ｍＪ以上になると抵抗値が非常に高くなると共に、８００ｍＪではリークレベルが、エキシマレーザを照射しない場合と同程度となる（～１０００ｎＡ）。また、１４００ｍＪ～２２００ｍＪにおいて、コンタクト抵抗，シート抵抗及びリーク電流が低く保たれていることが判る。

次に、第５図は、本発明に係る他の実施例を示している。

本実施例においては、上記した実施例の第１図Ｅに示す工程の後に、ＴｉＳｉ₂9ａ，９ｂ，９ｃ表面上にＳｉ⁺を例えば、出力２０ＫｅＶ，ドーズ量２１．５×１０¹⁵／ｃｍ²の条件でイオン注入を行ないＴｉＳｉ₂の表面をアモルファス層(図中×印で示す）を形成する。

次に、上記した実施例の第１図Ｆに相当する工程を行ないＴｉＳｉ₂表面の前記アモルファス層をＴｉＮ膜に変化させる。なお、本工程においては、エキシマレーザの照射は、パルスショット処理を行なってもよい。また、注入するイオンはＳｉ⁺の他、Ｔｉ⁺やＮ⁺等を用いてもよい。

本実施例においては、形成されたアモルファス層の融点が低いため、エネルギー効率を向上することが可能となる。また、ＴｉＳｉ₂表面にイオン注入するのではなく、Ｓｉ基板上にイオン注入を行なってもよい。本実施例は、特に径寸法の小さいコンタクトホール（０．３５μ以下のプロセス）に適用した場合に効果的である。さらに、アモルファス層の融点が低くなるため、レーザビームの大面積化及びレーザ装置の小型化を可能にする利点がある。

以上、本発明の実施例につき具体的に説明したが、本発明は、上述の実施例に限定されるものではなく、本発明の技術的思想に基づく各種の変形が可能である。

例えば、上記両実施例においては、高融点金属としてＴｉを用いたが、タングステン（Ｗ），モリブデン（Ｍｏ）等を適用しても同様である。

また、上記実施例においては、最終構造に反射膜１１を残しているが、この反射膜１１は例えば配線１４～１４ｃを形成する前に例えばリン酸によりエッチング除去することも可能である。また、この反射膜１１としては、例えばＴｉ膜のようなバリアメタル膜を用いることも可能である。さら

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に、この反射膜１１の代わりにレーザビームＢに対して吸収性のある他の金属膜を用いても、コンタクトホールＣ₁～Ｃ₃の内部におけるＴｉＳｉ₂膜９ａ～９ｃにのみレーザビームＢを選択的に照射することが可能である。

また、上述の実施例においては、本発明をＭＯＳトランジスタに適用した場合について説明したが、本発明は、例えばバイポーラＬＳＩやバイポーラＣＭＯＳＬＳＩのようなＭＯＳＬＳＩ以外の半導体集積回路装置の製造に適用することも可能である。

［発明の効果］

以上述べたように、本発明によれば、窒素を含む雰囲気中で高融点金属シリサイド膜にレーザビームを選択的に照射することにより高融点金属窒化物膜を形成するようにしているので、レーザビームが照射されない部分は高温に加熱されず、従って、高融点金属シリサイド膜の表面のモフォロジーの劣化や不純物の再拡散が生じるのを防止することができる。

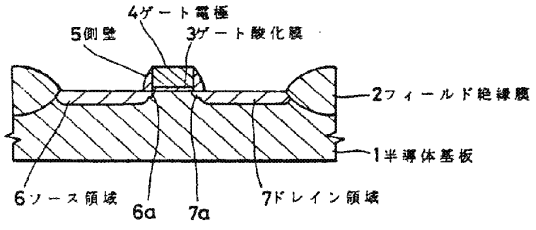
また、本発明によれば、コンタクト抵抗，シート抵抗及びリーク電流を低く保てる効果がある。

４．図面の簡単な説明

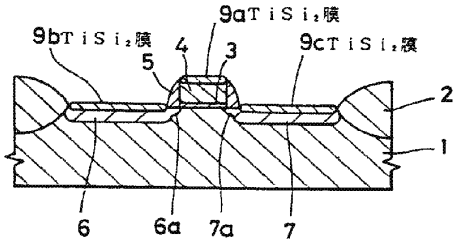
第１図Ａ～第１図Ⅱは本発明の実施例によるＭＯＳトランジスタの製造方法を工程順に示す断面図、第２図はエキシマレーザのエネルギー密度とコンタクト抵抗との関係を示すグラフ、第３図はエキシマレーザのエネルギー密度とシート抵抗との関係を示すグラフ、第４図はエキシマレーザのエネルギー密度とリーク電流の関係を示すグラフ、第５図は本発明の他の実施例を示す断面図である。

１…半導体基板、２…フィールド絶縁膜、４…ゲート電極、６…ソース領域、７…ドレイン領域、８…Ｔｉ膜、９ａ～９ｃ…ＴｉＳｉ₂膜、１１…反射膜、１３ａ～１３ｃ…ＴｉＮ膜、１４～１４ｃ…配線、Ｃ₁～Ｃ₃…コンタクトホール。

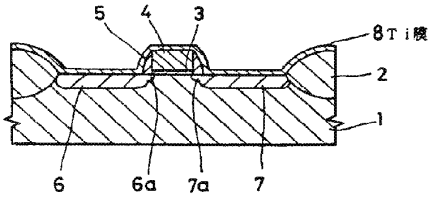
代理人　志賀富士弥　外１名



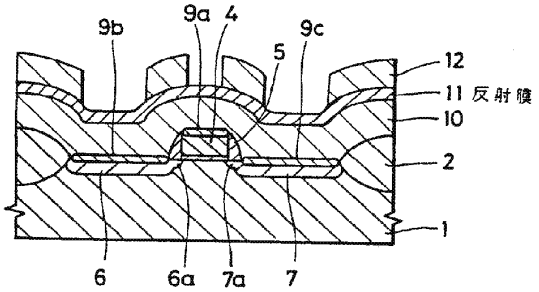
実施例
第１図Ａ



実施例
第１図Ｃ



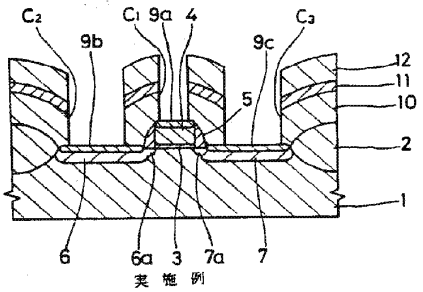
実施例
第１図Ｂ



実施例
第１図Ｄ

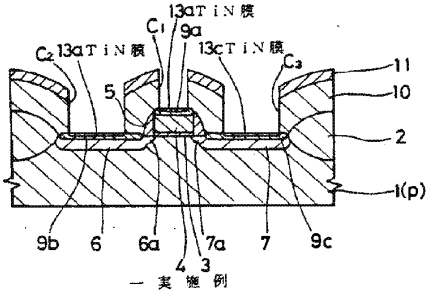
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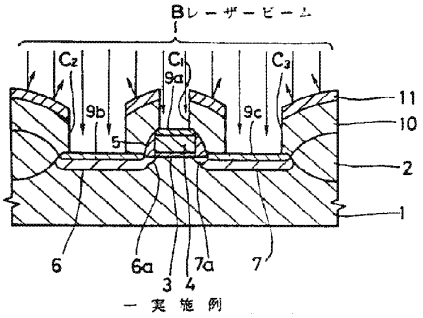
一 実 施 例

第 1 図E



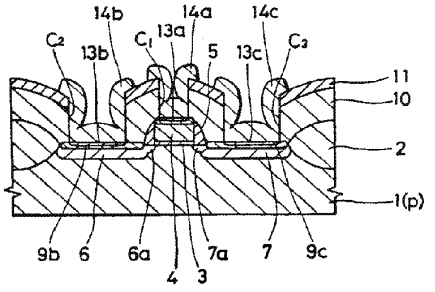
一 実 施 例

第 1 図G



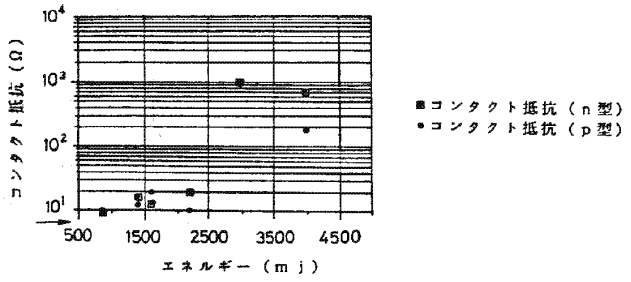
一 実 施 例

第 1 図F



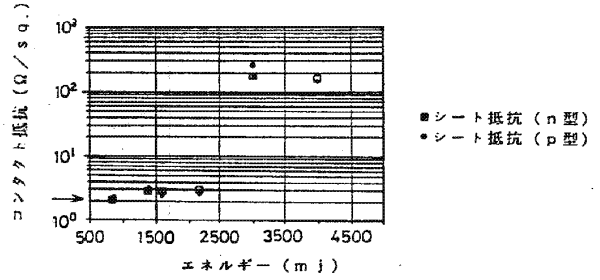
一 実 施 例

第 1 図H



エキシマレーザのエネルギー密度とコンタクト抵抗を示すグラフ

第 2 図

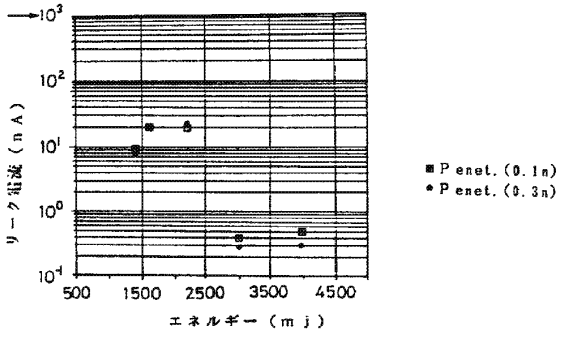


エキシマレーザのエネルギー密度とシート抵抗を示すグラフ

第 3 図

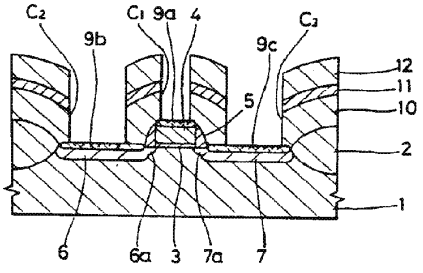
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エキシマレーザのエネルギー密度とリーク電流を示すグラフ

第 4 図



他の実施例

第 5 図

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Espacenet

Bibliographic data: JPH03183037 (A) — 1991-08-09

OPTICAL MEMORY MEDIUM

Inventor(s): YANAGISAWA MASAHIRO ± (YANAGISAWA MASAHIRO)

Applicant(s): NEC CORP ± (NEC CORP, ; NIPPON DENKI KK)

Classification: **- international:** ***G11B7/24;*** (IPC1-7): G11B7/24
- cooperative:

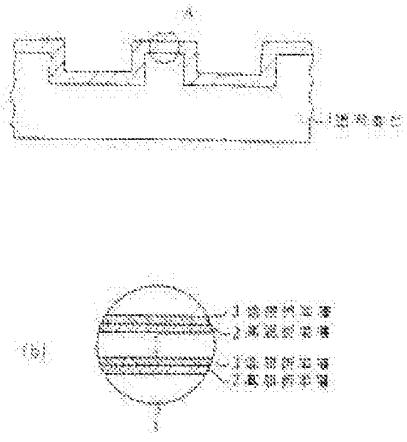
Application number: JP19890318799 19891211

Priority number(s): JP19890318799 19891211

Also published as: JP2647982 (B2)

Abstract of JPH03183037 (A)

PURPOSE:To improve reliability by forming combined layers of high-refractive index layers of adequate film thicknesses on a transparent substrate, thereby obtaining a high reflectivity.
CONSTITUTION:The combinations of the high-refractive index layers 2 consisting of silicon, germanium, etc., and the low-refractive index layers 3 consisting of silicon oxide, magnesium fluoride, etc., are formed in >=1 layers on the transparent substrate 1. The reflecting layers consisting of the respective layers generate multiple interferences in this way. The phases coincide and the reflectivity can be increased up to about 100% when the film thicknesses of the respective layers are selected at adequate values. There is, therefore, no need for forming the reflecting films consisting of Al, Au, etc., directly on the transparent substrate and the optical



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recording medium having the high reliability is obtd.

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⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　平3－183037

⑤1Int.Cl.⁵	識別記号	庁内整理番号	㊸公開　平成3年(1991)8月9日
G 11 B 7/24	B	8120－5D	

審査請求　未請求　請求項の数 2　（全6頁）

㊹発明の名称　光記憶体

㉑特　願　平1－318799
㉒出　願　平1(1989)12月11日

㉒発明者　柳沢　雅広　東京都港区芝5丁目33番1号　日本電気株式会社内
㉑出願人　日本電気株式会社　東京都港区芝5丁目7番1号
㉔代理人　弁理士　舘野　千恵子

明　細　書

1．発明の名称

光記憶体

2．特許請求の範囲

(1) 透明基板と、該透明基板の記録ピット形成面上に被覆される高屈折率層および低屈折率層の順よりなる組み合わせ層または低屈折率層および高屈折率層の順よりなる組み合わせ層を少なくとも1層以上を備えてなることを特徴とする光記憶体。

(2) 透明基板と、該透明基板の記録ピット形成面上に被覆される高屈折率層および低屈折率層の順よりなる組み合わせ層を少なくとも1層以上と、該組み合わせ層上に被覆される反射層とを備えてなることを特徴とする光記憶体。

3．発明の詳細な説明

［産業上の利用分野］

本発明は音響機器または情報機器などに用いられる光記憶体に関する。

［従来の技術］

従来、光記憶体の一つであるコンパクトディスク（以下、CDと略す。）の反射膜の材料としては、アルミニウムや金が使用されている。しかし、近年、CDにコンピュータデータを記録したCD－ROMが普及し、従来にも増して、高温・高湿下での保存性の高いものが望まれている。

［発明が解決しようとする課題］

従来の金あるいはアルミニウムの反射膜を使用した光記憶体は、かかる過酷な環境下において、蒸着された反射膜がアルミニウムの場合は腐食、また金の場合は下地体から剥離し、信号読み取りの指標とされるエラーレートが増加し、上記したようなニーズに適応できないという問題があった。またアルミニウムや金以外の反射膜材料は、反射率が不足するため使用できない状態にあった。

本発明は、以上述べたような従来の課題を解決するためになされたもので、耐候性、特に優れた耐食性と付着性を有し、かつ高反射率の反射膜を具備する光記憶体を提供することにある。

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［課題を解決するための手段］

本発明は、透明基板と、該透明基板の記録ピット形成面上に被覆される高屈折率層および低屈折率層の順よりなる組み合わせ層または低屈折率層および高屈折率層の順よりなる組み合わせ層を少なくとも１層以上を備えてなることを特徴とする光記憶体、および透明基板と、該透明基板の記録ピット形成面上に被覆される高屈折率層および低屈折率層の順よりなる組み合わせ層を少なくとも１層以上と、該組み合わせ層上に被覆される反射層とを備えてなることを特徴とする光記憶体である。

本発明で用いられる高屈折率層は主としてシリコン，ゲルマニウム，ほう素，硫化亜鉛，酸化チタン，酸化ジルコニウム，酸化インジウム，酸化アンチモン，硫化アンチモン，テルル，テルル化カドミウム，テルル化鉛などを使用することができる。

また本発明で用いられる低屈折率層は酸化珪素，ふっ化マグネシウム，酸化アルミニウム，ふっ化セリウム，酸化マグネシウム，ふっ化カルシウム，ふっ化ナトリウム，ふっ化リチウム，カーボン（非晶質またはダイアモンド）などを使用することができる。

本発明で用いられる反射層はクロム，モリブデン，タングステン，バナジウム，ニオブ，タンタル，チタン，ジルコニウム，ハフニウム，マンガン，レニウム，ルテニウム，鉄，オスミウム，コバルト，ロジウム，イリジウム，ニッケル，パラジウム，白金，亜鉛，カドミウム，錫，鉛，タリウム，アンチモン，ビスマス，インジウム，ガリウムなどの金属またはそれらの合金または窒化チタン，窒化ジルコニウム，窒化ハフニウムなどの金属窒化物を使用することができる。また、金または銀の単体を反射層として用いることは付着性の面で、さらに銅，アルミニウムの場合は腐食性の点で望ましくないため、これらの金属を用いる場合には、前記反射層として使われる金属との合金として使用することが望ましい。

本発明で用いられる透明基板は、アクリル樹脂，ポリカーボネート樹脂，ポリオレフィン樹脂，エポキシ樹脂，フッ素樹脂，ガラス，ゾルゲルガラスなどを用いることができる。

本発明の光記憶体は、射出成形あるいはスタンパからの密着転写などにより記録ピットを形成した透明基板の上に、高屈折率層および低屈折率層を交互にスパッタ法、イオンプレーティング法、クラスターイオンビーム法、プラズマＣＶＤ法あるいは蒸着法等により被覆し、さらに必要に応じて反射層を上記と同様に組み合わせ層上に被覆して形成する。

透明基板は、例えば、ガラス基板の上に珪酸重合物をスピン塗布し、スタンパを密着させてピットを転写させ、ピット付きの透明基板を形成する。またスタンパの型の中に樹脂を射出し、型から取り出してピット付きの透明基板を形成してもよい。

このように作製した本発明の光記憶体は、高反射率と高耐候性（高付着および高耐食性）を併せ持ち、従来の金またはアルミニウム反射膜を直接透明基板に被覆したものよりはるかに優れた長期のデータ保存に関する信頼性を有する。

［作用］

本発明の光記憶体は、透明基板上に高屈折率層と低屈折率層よりなる組み合わせ層を形成する。この組み合わせ層によって、各層からの反射光が多重干渉を起こし、この時、各層の膜厚を適切な値に選択すると位相が一致し、反射率を 100%近くにまで高めることができる。従って、従来のように透明基板上に直接Ａℓ やＡｕ等よりなる反射膜を形成しなくともよく、信頼性の高い光記憶体が提供される。

高屈折率層と低屈折率層の組み合わせ層のみでも反射率を 100%近くにすることができるが、多層の組み合わせが必要となる。そこで低屈折率層と高屈折率層の組み合わせ層上に反射層を設けると、少ない組み合わせ層数で高反射率を得ることができる。また高屈折率層と低屈折率層の屈折率の差が大きいほど該２層の膜厚を薄くすることができ、ピットの形状（深さ，巾，長さ）を損ねる

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ことが少ない。

［実施例］

以下に、図面を参照して本発明の実施例を詳細に説明する。

第１図は本発明の光記憶体の一実施例を示したもので、第１図(a)はその部分断面図、第１図(b)は(a)におけるＡ部の拡大断面図である。ここで、透明基板１、高屈折率層２、低屈折率層３がそれぞれ第１表のⅠおよびⅡに示す材質，構成および膜厚で被覆された２個の試料を作製した。

第２図は本発明の光記憶体１の他の一実施例を示したもので、第２図(a)はその部分断面図、第２図(b)は(a)におけるＢ部の拡大断面図である。ここで、透明基板１、低屈折率層３、高屈折率層２がそれぞれ第１表のⅢおよびⅣに示す材質，構成および膜厚で被覆された２個の試料を作製した。

第３図は本発明の光記憶体１の他の一実施例を示す部分断面図である。ここで、透明基板１、高屈折率層２、低屈折率層３、反射層４がそれぞれ第１表のⅤ，Ⅵ，Ⅶに示す材質，構成および膜厚で被覆された３個の試料を作製した。

得られた各試料の反射率を併せて第１表に示す。

（以下余白）

第　１　表

試料	透明基板	高屈折率層			低屈折率層			層数	反射層	反射率
		材質	膜厚(nm)	屈折率	材質	膜厚(nm)	屈折率		(膜厚nm)	(%)
Ⅰ	ポリカーボネート	Si	40	3.5	SiO_2	60	1.5	10	なし	90
Ⅱ	ゾルゲルガラス	TiO_2	60	2.7	MgF_2	60	1.4	10	なし	70
Ⅲ	ポリオレフィン	PbTe	30	5.5	LiF	40	1.4	9	なし	96
Ⅳ	ゾルゲルガラス	Ge	40	4.0	CaF_2	50	1.2	7	なし	85
Ⅴ	ポリカーボネート	Si	40	3.5	SiO_2	60	1.5	1	Cr (200)	80
Ⅵ	ポリオレフィン	Ge	40	4.0	MgF_2	60	1.4	1	Ta (200)	75
Ⅶ	ゾルゲルガラス	Si	40	3.5	CaF_2	50	1.2	1	TiN (300)	70

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次に、これらの試料とポリカーボネート樹脂からなる透明基板の上にアルミニウムおよび金を反射膜として形成した比較試料について、温度 70 ℃、相対湿度 95 %の耐候性試験を6ヶ月間行い、信号の良否の指標となるエラー数を測定した。6ヶ月の耐候性試験後、本発明の試料のエラー数は全く劣化がみられなかったが、アルミニウム反射膜を用いた比較試料は腐食により、また金反射膜を用いた比較試料は剥離によりエラーの測定が不能になるほど劣化した。

［発明の効果］

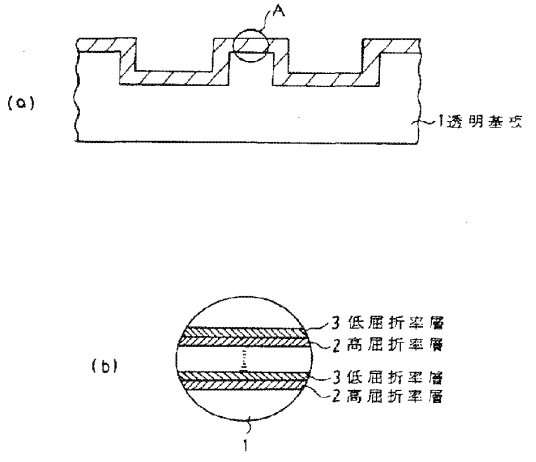
以上、詳細に述べたように、本発明の光記憶体は透明基板との密着性に優れ、かつ耐食性および高反射率を有しており、アルミニウムや金の反射膜を使用した光記憶体に比べてはるかに信頼性を向上させることができる。

4．図面の簡単な説明

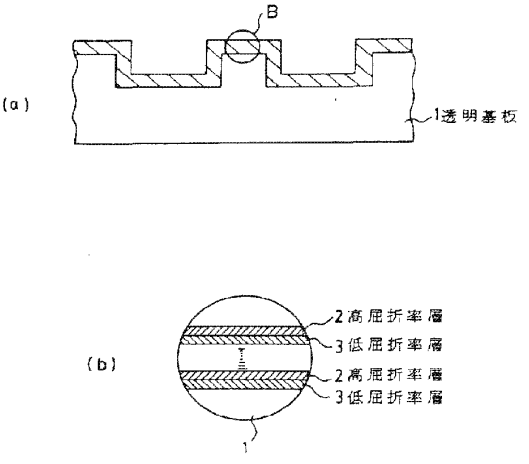
第1図から第3図はそれぞれ本発明の光記憶体の一実施例の部分断面図である。

1…透明基板
2…高屈折率層
3…低屈折率層
4…反射層

特許出願人　日本電気株式会社
代理人　弁理士　舘野千恵子



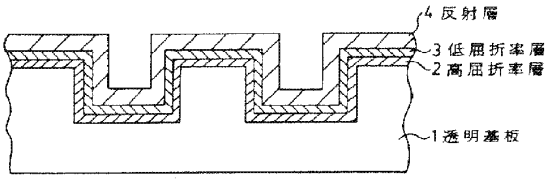
第1図



第2図

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第3図

手続補正書（自発）

平成3年3月5日

特許庁長官 殿

1．事件の表示

特願平1－318799号

2．発明の名称

光記憶体

3．補正をする者

事件との関係 ・ 特許出願人

住 所 東京都港区芝五丁目7番1号

名 称 (423) 日本電気株式会社

代表者 関 本 忠 弘

4．代 理 人 〒158

住 所 東京都世田谷区玉川4丁目12番16号

チロル玉川 202号 ☎03(3707)1639

氏 名 (9052) 弁理士 舘 野 千恵子

特許庁
3.3.6

5．補正の対象

明細書の「発明の詳細な説明」の欄と
明細書の「図面の簡単な説明」の欄、
および図面

6．補正の内容

(1) 明細書第3頁 19 行目～ 20 行目に「酸化珪素，ふっ化マグネシウム」とあるのを「酸化珪素，酸化ジルコニウムを含む酸化珪素，ふっ化マグネシウム」と補正する。

(2) 明細書第8頁3行目のあとに以下の文を挿入する。

「第4図は本発明を再生専用光記憶体に適用した一実施例の部分断面図である。ここで1はゾルゲル法により記録ピットを設けた強化ガラス基板、高屈折率層2、低屈折率層3、反射層4がそれぞれ第1表のⅦに示す材料、構成および膜厚で被覆した1個の試料を作製した。反射層4の上には試料を操作する際に反射層等に傷が発生することを防止する意味でシリコン系の樹脂膜5が 10 μm被覆されている。また、強化ガラスの基板面側にはガラスの腐食を防止するための保護膜6として 10 %の酸化ジルコニウムを含む酸化珪素を 100nm被覆した。」

(3) 明細書第9頁第1表を以下のように補正する。

（以下余白）

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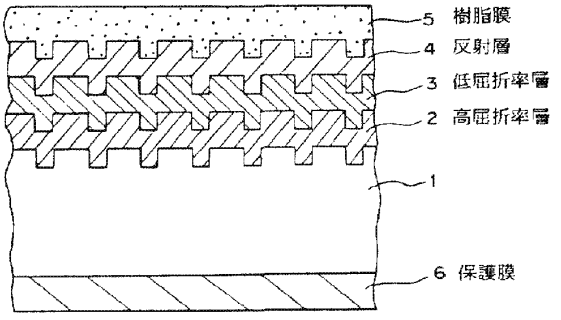
第　1　表

試料	透明基板	高屈折率層			低屈折率層			層数	反射層	反射率
		材質	膜厚	屈折率	材質	膜厚	屈折率		(膜厚nm)	(%)
Ⅰ	ポリカーボネート	Si	40 nm	3.5	SiO_2	60 nm	1.5	10	なし	90
Ⅱ	ゾルゲルガラス	TiO_2	60	2.7	MgF_2	60	1.4	10	なし	70
Ⅲ	ポリオレフィン	PbTe	30	5.5	LiF	40	1.4	9	なし	96
Ⅳ	ゾルゲルガラス	Ge	40	4.0	CaF_2	50	1.2	7	なし	85
Ⅴ	ポリカーボネート	Si	40	3.5	SiO_2	60	1.5	1	Cr (200)	80
Ⅵ	ポリオレフィン	Ge	40	4.0	MgF_2	60	1.4	1	Ta (200)	75
Ⅶ	ゾルゲルガラス	Si	40	3.5	CaF_2	50	1.2	1	TiN (300)	70
Ⅷ	ゾルゲルガラス	Si	60	3.5	SiO_2 − 10%ZrO_2	40	1.5	1	Cr (100)	82

(4) 明細書第 10 頁 18 行目に「第1図から第3図」とあるのを「第1図から第4図」と補正する。

(5) 明細書第11頁1行目～3行目に「2…高屈折率層　3…低屈折率層　4…反射層」とあるのを「2…高屈折率層　3…低屈折率層　4…反射層　5…樹脂膜　6…保護膜」と補正する。

(6) 本願添付図面の第3図の次に別紙図面の第4図を追加する。



第4図

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Espacenet

Bibliographic data: JPH06275641 (A) — 1994-09-30

METHOD OF FORMING THIN FILM TRANSISTOR

Inventor(s): CHIYOU KOUYUU ± (CHIYOU KOUYUU)

Applicant(s): SEMICONDUCTOR ENERGY LAB ± (SEMICONDUCTOR ENERGY LAB CO LTD)

Classification: **- international:** ***H01L21/28; H01L21/336; H01L29/78; H01L29/786;*** (IPC1-7): H01L21/336; H01L29/784
- cooperative:

Application number: JP19930086752 19930322

Priority number (s): JP19930086752 19930322

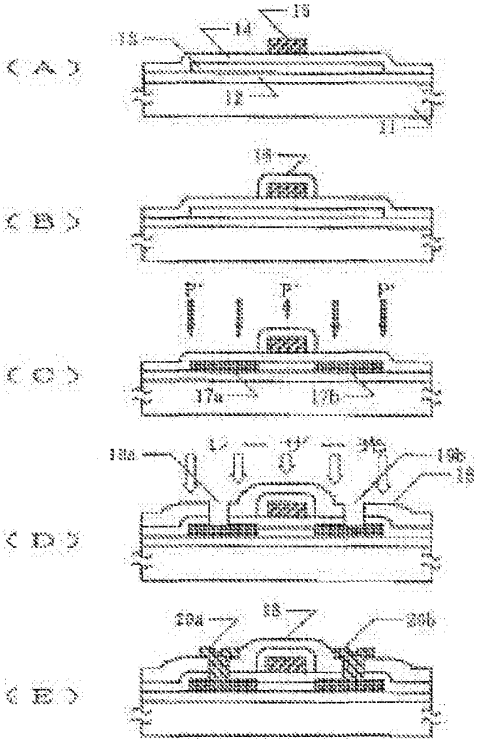
Also published as: JP3315191 (B2)

Abstract of JPH06275641 (A)

PURPOSE:To form contact without an silicon oxide coating film of nonstoichiometry ratio, and reduce the contact resistance of an impurity region, by performing laser annealing after an interlayer insulating film and contact holes are previously formed. CONSTITUTION:A gate insulating film 14 is formed so as to cover a thin film type semiconductor region 13, and a gate electrode 15 is formed so as to traverse the semiconductor region 13. An anodic oxidation material layer 16 is grown on the surface of the gate electrode 15. After that, the gate electrode 15 and an anodic oxidation material layer 16 around the gate electrode are used as masks, and doping impurities are introduced in a self-alignment manner, through a gate insulating film 18. An interlayer insulating film 18 and contact holes 19a, 19b are formed, and the doping impurities are activated by laser beam irradiation.; Electrode wirings 20a, 20b of a source region and a drain region are formed. Thereby a high resistance film which is to be formed by the combination of the semiconductor film and the gate insulating film at the time of laser beam annealing is not formed, so that contact resistance can be reduced.

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(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号

特開平6－275641

(43)公開日　平成６年(1994)９月30日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０１Ｌ　21/336				
29/784				
		9056－4M	Ｈ０１Ｌ　29/ 78	３１１　Ｐ

審査請求　未請求　請求項の数２　ＦＤ　（全　４　頁）

(21)出願番号　特願平5－86752

(22)出願日　平成５年(1993)３月22日

(71)出願人　000153878
株式会社半導体エネルギー研究所
神奈川県厚木市長谷398番地

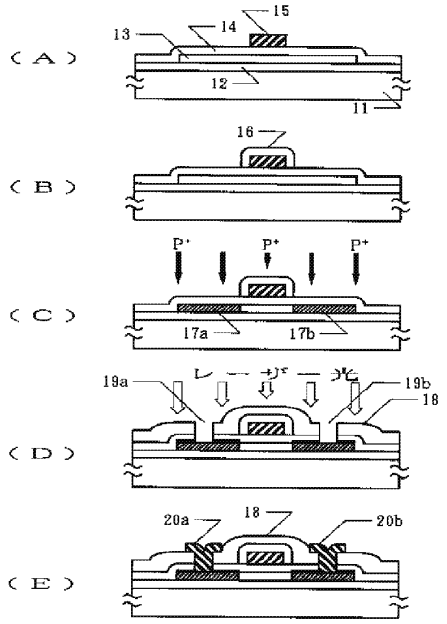
(72)発明者　張　宏勇
神奈川県厚木市長谷398番地　株式会社半導体エネルギー研究所内

(54)【発明の名称】　薄膜トランジスタの作製方法

(57)【要約】

【目的】　レーザーアニールによってドーピング不純物の活性化をおこなうＴＦＴの製造方法において、不純物領域のコンタクト抵抗を低減せしめる方法を提供する。

【構成】　薄膜状半導体領域を覆って、ゲイト絶縁膜を設け、また、該半導体領域を横断してゲイト電極を設ける。その後、このゲイト電極をマスクとして、ゲイト絶縁膜を通して、自己整合的にドーピング不純物を導入する。その後、層間絶縁物を形成し、コンタクトホールを設け、レーザーもしくはそれと同等な強光を照射することによってドーピング不純物の活性化をおこなう。しかるのちにソース、ドレインの電極を形成する。かくすることにより、レーザーアニールの際に半導体膜とゲイト絶縁膜が化合して生じる高抵抗膜ができないので、コンタクト抵抗を減じることができる。



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【特許請求の範囲】
【請求項１】　基板上に島状非単結晶半導体領域を形成する第１の工程と、
前記非単結晶半導体領域を覆って絶縁被膜と、前記絶縁被膜上に、ゲイト電極を形成する第２の工程と、
前記ゲイト電極をマスクとして不純物をドーピングする第３の工程と、
前記ゲイト電極を覆って層間絶縁物を堆積する第４の工程と、
前記層間絶縁物を通して、前記半導体領域の不純物のドーピングされた領域にコンタクトホールを形成する第５の工程と、
前記層間絶縁物およびコンタクトホールを通してレーザーもしくはそれと同等な強光を照射することによって、前記半導体領域にドーピングされた不純物を活性化する第６の工程とを有することを特徴とする薄膜トランジスタの作製方法。
【請求項２】　請求項１において、第２の工程と第３の工程の間に前記ゲイト電極を陽極酸化する工程、を有することを特徴とする薄膜トランジスタの作製方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、非単結晶半導体薄膜を有する薄膜トランジスタ（ＴＦＴ）の作製方法に関するものである。本発明によって作製される薄膜トランジスタは、ガラス等の絶縁基板上、単結晶シリコン等の半導体基板上、いずれにも形成される。
【０００２】
【従来の技術】最近、絶縁基板上に、薄膜状の活性層（活性領域ともいう）を有する絶縁ゲイト型の半導体装置の研究がなされている。特に、薄膜状の絶縁ゲイトトランジスタ、いわゆる薄膜トランジスタ（ＴＦＴ）が熱心に研究されている。これらは、利用する半導体の材料・結晶状態によって、アモルファスシリコンＴＦＴや結晶性シリコンＴＦＴというように区別されている。
【０００３】結晶半導体は、アモルファス半導体よりも電界移動度が大きく、したがって、高速動作が可能である。また、結晶性シリコンでは、ＮＭＯＳのＴＦＴだけでなく、ＰＭＯＳのＴＦＴも同様に得られるのでＣＭＯＳ回路を形成することが可能である。このため、特に最近では結晶シリコンを使用したＴＦＴが盛んに研究されている。
【０００４】結晶シリコンは通常、６００℃以上の温度で長時間のアニールによって得られ、また、イオン注入、イオンドーピング等の方法によって不純物のドーピングされた結晶シリコンにおいて、ドーピング不純物の活性化をおこなうにも同様な温度での熱処理が必要とされてきた。しかしながら、このような高温での熱処理は基板やＴＦＴの構成材料の選択の余地を狭めることとなるのでより低温での処理が求められている。
【０００５】
【発明が解決しようとする課題】結晶化・活性化の低温化の手段として、レーザーもしくはそれと同等な強力な光をシリコン膜に照射することによってシリコンの結晶化、活性化をおこなうことが提案されている。このような方法を光源の名称によってレーザーアニール、もしくはランプアニールと称する。以下では、これらの方法を全てレーザーアニールと総称することとする。
【０００６】レーザーアニールを用いたシリコン膜のドーピング不純物の活性化プロセスを有するＴＦＴの作製工程の例を図２に示す。まず、基板２１上に下地絶縁膜２２を堆積し、その上に結晶シリコン領域２３を形成する。シリコン膜の結晶化には熱アニール、レーザーアニールいずれもが使用される。そして、このシリコン領域を覆って、ゲイト絶縁膜２４が堆積される。さらに、ゲイト電極２５がその上に形成される。（図２（Ａ））
【０００７】そして、ゲイト電極の表面を陽極酸化法によって酸化する。これは不純物領域（ソース、ドレイン）とゲイト電極がオフセット状態となることによって、より良い特性を得るためである。もちろん、このような陽極酸化物２６を形成することは必ずしも必要なわけではない。（図２（Ｂ））
【０００８】その後、イオン注入法、イオンドーピング法等の手段によって、ゲイト絶縁膜２４を通して、シリコン領域２３に不純物が導入される。このときには不純物の導入はゲイト絶縁膜を通すことが歩留りを上げるうえで必要である。こうして、ソース、ドレイン２７ａ、２７ｂが形成される。先に述べた通り、不純物領域とゲイト電極は重なりあうことがなく、わずかに陽極酸化物２７の幅だけ離れた状態（オフセット状態）となっている。（図２（Ｃ））
【０００９】そして、レーザーもしくはそれと同等な強光によって、ドーピングされた不純物の活性化をおこなう。このときには、レーザーエネルギーによってドーピング不純物（燐やホウ素）、シリコン、酸化珪素が化合して、厚さ３０～５００Åの非化学量論比の酸化珪素系の被膜２８がシリコン領域とゲイト絶縁膜２４の境界に形成される。（図２（Ｄ））
【００１０】最後に、コンタクトホールを形成して、ソース、ドレインに金属電極３０ａ、３０ｂを形成するのであるが、この際に、先に形成された非化学量論比の酸化珪素系の被膜２８は、酸化剤を含まないフッ化水素酸系のエッチャントでは十分に除去できない。一方、ドライエッチングでは、酸化珪素とシリコンのエッチング比がそれほど大きくないので、特にシリコン領域が薄い場合には、コンタクトホールがシリコン領域を貫通してしまうことがあった。（図２（Ｅ））
【００１１】このような非化学量論比の酸化珪素系の被膜２８は抵抗が高く、ＴＦＴのコンタクト不良の原因であった。本発明はこのような非化学量論比の酸化珪素系

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の被膜のないコンタクトを作製する方法を提供することを目的とする。

【００１２】

【課題を解決するための手段】本発明は、レーザーアニールをおこなう前に、層間絶縁物とコンタクトホールを予め形成し、しかるのちにレーザーアニールをおこなうことを特徴とする。そのため、コンタクトホールの領域では反応すべき酸化珪素が存在しないので、上記のような非化学量論比の酸化珪素系の被膜は形成されない。その後、このコンタクトホールに金属電極を形成することによって確実なコンタクトが形成される。以下に実施例を用いて、より詳細に本発明を説明する。

【００１３】

【実施例】図１に本実施例の作製工程の断面図を示す。まず、基板（コーニング７０５９）１１上にスパッタリング法によって厚さ２０００Åの酸化珪素の下地膜３２を形成した。さらに、プラズマＣＶＤ法によって、厚さ５００～１５００Å、例えば１５００Åの真性（Ｉ型）のアモルファスシリコン膜を、さらにその上にスパッタリング法によって厚さ２００Åの酸化珪素膜を堆積した。そして、このアモルファスシリコン膜を窒素雰囲気中、６００℃、４８時間アニールして結晶化させた。

【００１４】この工程はレーザーアニールによっておこなってもよい。レーザーとしては各種エキシマーレーザーが使用できる。レーザーのエネルギー密度は、２００～５００ｍＪ／ｃｍ^2、例えば３５０ｍＪ／ｃｍ^{2}とし、１か所につき２～１０ショット照射し、レーザー照射時には基板を１００～４５０℃に加熱すればよい。

【００１５】結晶化工程後、シリコン膜をパターニングして、島状シリコン領域１３を形成し、さらに、スパッタリング法によって厚さ１０００Åの酸化珪素膜１４をゲイト絶縁膜として堆積した。スパッタリングには、ターゲットとして酸化珪素を用い、スパッタリング時の基板温度は２００～４００℃、例えば２５０℃、スパッタリング雰囲気は酸素とアルゴンで、アルゴン／酸素＝０～０．５、例えば０．１以下とした。

【００１６】引き続いて、スパッタリング法によって、シリコンを０．５～３％、例えば２％含むアルミニウム膜を厚さ１０００～１００００Å、例えば５０００Å堆積した。なお、この酸化珪素とアルミニウム膜の成膜工程は連続的におこなうことが望ましい。そして、アルミニウム膜をパターニングして、ゲイト電極１５を形成した。アルミニウムの代わりにシリコン、チタン、タンタル、モリブテン、タングステン等の他の金属・半導体材料、あるいはそれらの珪化物でもよい。また、単層の膜ではなく、異種の被膜を重ねた多層の膜でもよい。（図１（Ａ））

【００１７】続いて、酒石酸のエチレングリコール溶液（１～５％、アンモニアによって中性にする）に基板を浸漬して、ゲイト電極に電流を通じ、ゲイト電極の表面に陽極酸化物（酸化アルミニウム）層１６を成長させた。陽極酸化物の厚さは１０００～５０００Å、特に２０００～３０００Åが好ましかった。ここでは２５００Åとした。（図１（Ｂ））

【００１８】そして、イオンドーピング法によって、シリコン領域にゲイト電極とその周囲の陽極酸化物をマスクとして不純物（燐）を注入した。ドーピングガスとして、フォスフィン（PH_3）を用い、加速電圧を６０～９０ｋＶ、例えば８０ｋＶとした。ドーズ量は1×10^{15}～8×10^{15}ｃｍ$^{-2}$、例えば、2×10^{15}ｃｍ$^{-2}$とした。この結果、Ｎ型の不純物領域１７ａ、１７ｂが形成された。（図１（Ｃ））

【００１９】続いて、厚さ６０００Åの酸化珪素膜１８を層間絶縁物としてプラズマＣＶＤ法によって形成し、これにコンタクトホール１９ａ、１９ｂを形成した。その後、レーザー光を照射し、レーザーアニールをおこなった。レーザーとしてはＫｒＦエキシマーレーザー（波長２４８ｎｍ、パルス幅２０ｎｓｅｃ）を用いたが、その他のレーザー、例えば、ＸｅＦエキシマーレーザー（波長３５３ｎｍ）、ＸｅＣｌエキシマーレーザー（波長３０８ｎｍ）、ＡｒＦエキシマーレーザー（波長１９３ｎｍ）等を用いてもよい。ただし、レーザー光が層間絶縁物１８を十分に透過することが必要とされる。レーザーのエネルギー密度は、２００～５００ｍＪ／ｃｍ^2、例えば２５０ｍＪ／ｃｍ^{2}とし、１か所につき２～１０ショット、例えば２ショット照射した。レーザー照射時に、基板を１００～４５０℃、例えば２５０℃に加熱した。こうして、不純物の活性化をおこなった。（図１（Ｄ））

【００２０】最後に、金属材料、例えば、窒化チタンとアルミニウムの多層膜によってＴＦＴのソース領域、ドレイン領域の電極・配線２０ａ、２０ｂを形成した。金属材料のデポジションの前に基板を薄いフッ化水素酸で洗浄することによって、コンタクト部分に生じたシリコンの自然酸化膜を除去すると、より完全なコンタクトが形成された。最後に、１気圧の水素雰囲気で３５０℃、３０分のアニールをおこなった。以上の工程によって薄膜トランジスタが完成した。（図１（Ｅ））

【００２１】

【発明の効果】本発明によって、ソース、ドレインのコンタクトの良好なＴＦＴを得ることができた。これによって、ＴＦＴの作製歩留りは格段に向上し、また、特性ばらつきも著しく減らすことができた。このように本発明は工業上有益な発明である。

【図面の簡単な説明】

【図１】　実施例のＴＦＴの作製工程断面図を示す。

【図２】　従来のＴＦＴの作製工程断面図を示す。

【符号の説明】

１１・・・基板

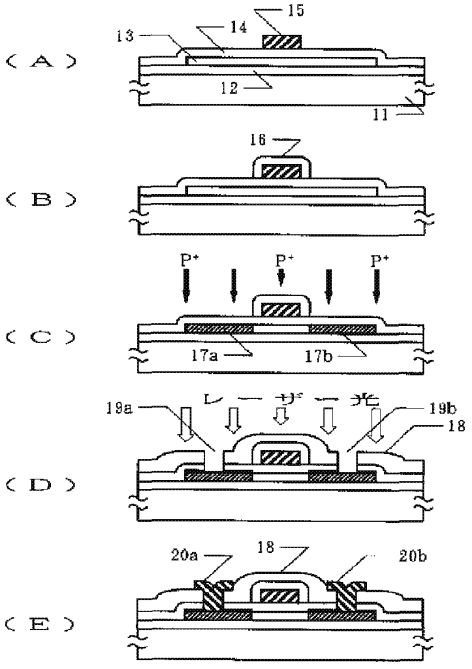
１２・・・下地絶縁膜（酸化珪素）

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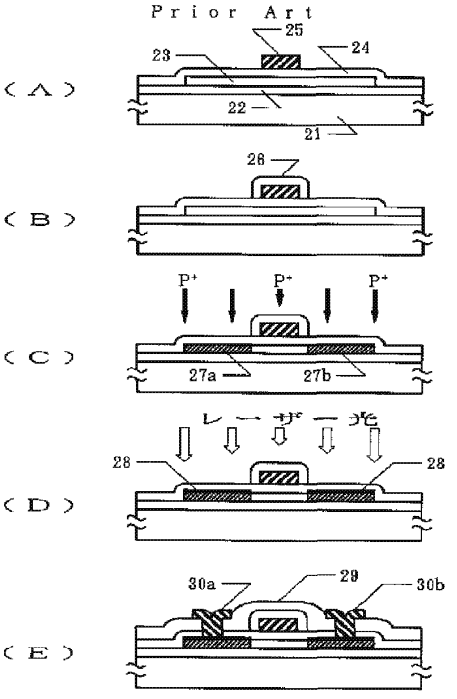
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１３・・・島状シリコン領域
１４・・・ゲイト絶縁膜（酸化珪素）
１５・・・ゲイト電極（アルミニウム）
１６・・・陽極酸化物（酸化アルミニウム）
１７・・・不純物領域（ソース、ドレイン）
１８・・・層間絶縁物（酸化珪素）
１９・・・コンタトホール
２０・・・金属電極・配線（窒化チタン／アルミニウム）

【図１】



【図２】



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PATENT ABSTRACTS OF JAPAN

(11)Publication number : 57-071188
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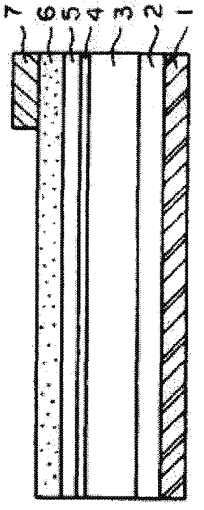
(51)Int.Cl. H01L 31/04

(21)Application number : 55-147846
(22)Date of filing : 21.10.1980

(71)Applicant : MITSUBISHI ELECTRIC CORP
(72)Inventor : HIGAKI YUKIO
YUKIMOTO YOSHINORI

(54) AMORPHOUS SOLAR CELL

(57)Abstract:
PURPOSE: T obtain P-i-N type cell, of small electric resistance, by constituting most of poly-crystal and a part of amorphous layer in a P type layer, as for a solar cell which consists of a P type semiconductor layer and an i type amorphous semiconductor layer, accumulated subsequently on a substrate, and an N type amorphous semiconductor layer.
CONSTITUTION: An N type layer 2 and an i type layer 3, composed of amorphous layer, and a P type layer 4 are accumulated on a metal substrate 1 of stainless steel or the like. A P type polycrystalline layer 5 is accumulated thereon. A transparent electrode 6 of In-Sn composite is accumulated thereon. An Al metal electrode 7 is attached to an end thereon. In this constitution, the layers 2-4 are formed subsequently by glow discharge or the like. THe layer 5 is formed temporarily as a P type amosphous layer, and mostly converted into poly-crystal, while partly remaining as unification with the P type amorphous layer 4, by applying a laser beam. This allows poly-crystallization so as to decrease the electric resistace as well as reduce absorption coefficient, thereby to make it possible to increase the thickness correspondingly and further lowes the resistance.



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⑲ 日本国特許庁 (JP)　　⑪ 特許出願公開

⑫ 公開特許公報 (A)　　昭57—71188

⑤Int. Cl.³	識別記号	庁内整理番号	⑬公開 昭和57年(1982)5月1日
H 01 L 31/04		7021—5F	

発明の数 1
審査請求 未請求

(全 3 頁)

⑤④アモルファス太陽電池

⑳特　願 昭55—147846
㉒出　願 昭55(1980)10月21日

⑦発 明 者 檜垣幸夫
伊丹市瑞原4丁目1番地三菱電機株式会社エル・エス・アイ研究所内

⑦発 明 者 行本善則
伊丹市瑞原4丁目1番地三菱電機株式会社エル・エス・アイ研究所内

⑦出 願 人 三菱電機株式会社
東京都千代田区丸の内2丁目2番3号

⑦代 理 人 弁理士 葛野信一　外1名

明　細　書

1. 発明の名称

アモルファス太陽電池

2. 特許請求の範囲

(1) 基板上に順次積層されたp型半導体層，i型アモルファス半導体層，n型アモルファス半導体層を有するアモルファス太陽電池において、前記p型半導体層は大部分がp型多結晶層半導体層によつて形成されかつ一部がp型アモルファス半導体層によつて形成されていることを特徴とするアモルファス太陽電池。

(2) p型多結晶半導体層は、p型アモルファス半導体層にレーザ光を照射することによつて形成されていることを特徴とする特許請求の範囲第1項記載のアモルファス太陽電池。

3. 発明の詳細な説明

この発明はアモルファス半導体を用いたpin型構造を有する太陽電池に関するものである。

この種の太陽電池においては一般に、光エネルギを受けて電子と正孔のキャリアを発生する部分は主としてi型半導体部に集中しており、p型およびn型層はキャリアの発生には殆んど寄与しない。従つて、光が照射される側にあるp型層については、特に、光の無駄な吸収を防ぐためにできる限り薄く形成する必要がある。

しかしながら、このようにp型アモルファス半導体層を薄くすると、他方で電気抵抗が増大するという問題が生じて来る。

この発明は、このような従来技術における問題を解決するためになされたもので、その目的は、電気抵抗の小さいpin型のアモルファス太陽電池を提供することにある。

このような目的を達成するために、この発明によるアモルファス太陽電池は、p型アモルファス半導体層の大部分を多結晶半導体層によつて置換したものである。以下、実施例によつて、この発明によるアモルファス太陽電池を詳細に説明する。

第1図は、この発明によるアモルファス太陽電池の一実施例を示す断面図である。同図において、ステンレス鋼等の金属基板(1)の上にn型アモルファス

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層(2)，i型アモルファス層(3)，p型アモルファス層(4)，p型多結晶層(5)が積層され、その上に、例えばインジウムとすずの混合物を蒸着することによつて透明電極(6)が形成されている。この透明電極(6)の上に更に、アルミニウム等によつて金属電極(7)が形成されている。該n型アモルファス層(2)，i型アモルファス層(3)，p型アモルファス層(4)は、例えばグロー放電法によつて順次形成される。またp型多結晶層(5)は、一旦p型アモルファス層を形成してこれにレーザ光を照射し、一部をp型アモルファス層(4)として残して大部分を多結晶層に変換することによつて形成される。

このように一旦形成したp型アモルファス層の大部分を多結晶化することにより、電気抵抗を低減することができる。また、多結晶化によつて光の吸収係数が小さくなるために、アモルファス層のみの場合に比べて厚くすることができ、電気抵抗が更に低減される。またこの場合には、はじめから薄いp型アモルファス層を形成しなければならない従来のものに比べ、膜厚の成長条件を緩和することができる利点がある。また、多結晶化する部分の厚さは、照射されるレーザ光の出力を調整することによつて高精度で制御することができる。

第2図は、この発明によるアモルファス太陽電池の他の実施例を示す断面図であり、第1図と同一部分は同一記号を用いてその詳細説明を省略する。同図において、ガラス基板(8)の上に、透明電極(6)が形成され、その上に、ボロンを大量にドーピングしたp型多結晶層(5)が形成されている。このp型多結晶層(5)を形成するには、先ず例えば化学的気相成長法によつてノンドーピングの多結晶層を形成した後にボロンをドーピングしてもよいし、予めドーピングしたガスを用いて化学的気相成長を行なつてもよい。また、グロー放電法により、ガス中にドーピングしながら高温で形成してもよいし、低温でアモルファス状態のものを形成した後に、レーザ光を照射して多結晶化する方法によつてもよい。このp型多結晶層(5)の上に、周辺の一部を残してp型アモルファス層(4)，i型アモルファス層(3)，n型アモルファス層(2)が順次積層されている。これらのアモルファス層は、該周辺の一部を金属マスクで蔽つた状態で、例えばグロー放電法によつて形成することができる。該n型アモルファス層(2)および露出したp型多結晶層(5)の表面上に、金属電極(7a)，(7b)が設けられている。この金属電極は、所定のパターンを有する金属マスクを用い、アルミニウム等の金属を蒸着することによつて形成される。

この場合も、p型半導体層のうちアモルファス層は極く薄く形成し、大部分を多結晶層によつて構成したことにより、電気抵抗を低減することができる。

以上説明したように、この発明によるアモルファス太陽電池によれば、光が照射される側のp型半導体層を、アモルファス層と該アモルファス層よりも小さい比抵抗を有する多結晶層とによつて形成したことにより、アモルファス層のみを用いた場合に比べて電気抵抗を低減することができる。また、該多結晶層はアモルファス層に比べて光の吸収係数が小さいため、キャリア発生部としてのi型半導体部に到達する前にp型半導体層において無駄に吸収される光を減少させることができる。従つて、p型半導体層で吸収される光を一定とした場合には、従来のものに比べて厚く形成することができ、電気抵抗を更に減少させることが可能になると共に、製造が容易になる等の種々優れた効果を有する。

4. 図面の簡単な説明

第1図はこの発明によるアモルファス太陽電池の一実施例を示す断面図、第2図はこの発明によるアモルファス太陽電池の他の実施例を示す断面図である。

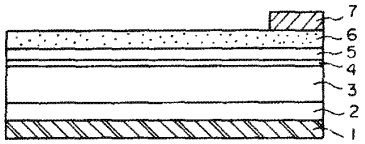
(1)・・・・金属基板、(2・・・・n型アモルファス層、(3)・・・・i型アモルファス層、(4)・・・・p型アモルファス層、(5)・・・・p型多結晶層、(8)・・・・ガラス基板。

代理人　高　野　信　一（外1名）

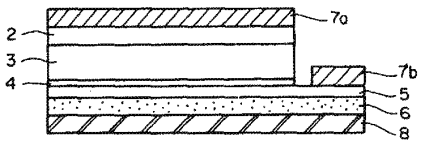
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第1図



第2図



手 続 補 正 書 （自発）

昭和[illegible]年[illegible]月16日

特許庁長官殿

1. 事件の表示　　特願昭 55－147846号 ✓

2. 発明の名称

アモルファス太陽電池

3. 補正をする者

事件との関係　特許出願人
住 所　東京都千代田区丸の内二丁目2番3号
名 称(601)　三菱電機株式会社
代表者　進 藤 貞 和
片 山 仁八郎

4. 代 理 人
住 所　東京都千代田区丸の内二丁目2番3号
三菱電機株式会社内
氏 名(6699)　弁理士 葛 野 信 一

(1)

5. 補正の対象

明細書の発明の詳細な説明の欄

6. 補正の内容

(1) 明細書第3頁第3行の「インジウムとすず」を「酸化インジウムと酸化すず」と補正する。

以 上

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Espacenet

Bibliographic data: JP2000164914 (A) — 2000-06-16

PHOTOSENSITIVE SEMICONDUCTOR ELEMENT, PHOTOSENSITIVE SEMICONDUCTOR DEVICE, PHOTOSENSITIVE CIRCUIT, AND FRAME CONTROL METHOD USING PHOTOSENSITIVE SEMICONDUCTOR ELEMENT OR PHOTOSENSITIVE SEMICONDUCTOR DEVICE

Inventor(s): PAUCHARD ALEXANDRE; POPOVIC RADIVOJE; RACZ ROBERT ± (PAUCHARD ALEXANDRE, ; POPOVIC RADIVOJE, ; RACZ ROBERT)

Applicant(s): ELECTROWATT TECHNOL INNOV AG ± (ELECTROWATT TECHNOL INNOV AG)

Classification: **- international:** ***F23N5/08; H01L31/0352; H01L31/10; H01L31/11;*** (IPC1-7): H01L31/10
- cooperative: **F23N5/082; H01L31/0352; H01L31/11**

Application number: JP19990256472 19990910

Priority number (s): EP19980117134 19980910

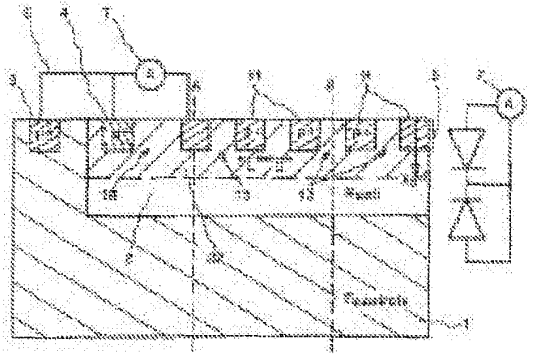
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Abstract of JP2000164914 (A)

PROBLEM TO BE SOLVED: To provide a small and durable photosensitive semiconductor element or photosensitive semiconductor device with high selectivity, effectiveness, and detection capability. SOLUTION: The photosensitive semiconductor element comprises a substrate 1, an intermediate layer 2, and an external layer 5 while the intermediate layer 2 at least partially embedded in the substrate 1 and the external layer 5 in the intermediate layer 2. The intermediate layer 2 and external layer 5 form a photosensitive region 22, generating a light-dependent signal such as optical current. The external layer 5 is divided into regions 11 which, spaced apart from each other, are isolated by a region 13 of the intermediate layer 2. The spaced region 11 of the external layer is used, for example, as an anode of a photosensitive semiconductor element, connected to a detection circuit. Thanks to the region 11, re-coupling of a charge carrier reduces, preventing formation of an inactive layer. Thus, the optical current generated by incident light increases.

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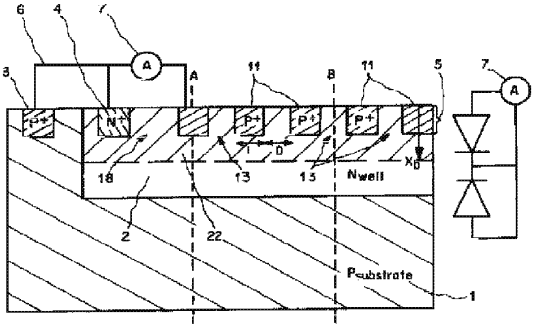
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最終頁に続く

(54)【発明の名称】　感光性半導体素子、感光性半導体装置、感光性回路、並びにこの感光性半導体素子ないしは感光性半導体装置を使用して火炎を制御する方法

(57)【要約】
【課題】　小さくて丈夫で、さらに非常に高い選択性、有効性並びに極めて高い検出能力を有する感光性半導体素子ないしは感光性半導体装置を提供する。
【解決手段】　感光性半導体素子は、基板１、中間層２および外部層５からなり、少なくとも部分的に中間層２が基板１の内部に、また外部層５が中間層２の内部に埋め込まれる。中間層２と外部層５は、感光性領域２２を形成し、光電流のような光依存性の信号を発生させる。外部層５は、中間層２の領域１３によって分離された互いに離間した領域１１に分割されている。外部層の離間した領域１１は、たとえば感光性の半導体素子の陽極として用いられ、検出回路に接続される。離間した領域１１によって、電荷担体の再結合が減少し不活性層の形成が防止される。それにより入射光により発生される光電流を増大させることができる。

Fig.4



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【特許請求の範囲】

【請求項１】　基板（１）、中間層（２）および外部層（５）からなり、少なくとも部分的に中間層（２）が基板（１）の内部に、また外部層（５）が中間層（２）の内部に埋め込まれており、中間層（２）と外部層（５）により感光性領域（２２）が形成され光依存性の信号（Ｒ）が生成される感光性半導体素子において、
外部層（５）が、中間層（２）の中間領域（１３）によって分離された互いに離間した領域（１１）からなることを特徴とする感光性半導体素子。

【請求項２】　基板（１）はアクセプタがドープされたシリコンから、中間層（２）ないしは中間領域（１３）はドナーがドープされたシリコンから、そして離間した領域（１１）はアクセプタが高濃度でドープされたシリコンからなり、離間した領域（１１）が感光性半導体素子の陽極（３０）として用いられることを特徴とする請求項１に記載の半導体素子。

【請求項３】　離間した領域（１１）、中間領域（１３）並びに中間層（２）の一部を包囲する感光性領域（２２）が、入射光の所定の波長領域を検出するために、入射光のほぼ１波長（W_t）の大きさの深さ（X_b）を有することを特徴とする請求項１または２に記載の半導体素子。

【請求項４】　感光性領域（２２）が、紫外線を検出するために、約０．０１から０．５μm、好ましくは０．１から０．４μm程度の深さ（X_b）を有することを特徴とする請求項１から３のいずれか１項に記載の半導体素子。

【請求項５】　中間領域（１３）が、感光性領域（２２）の深さ（X_b）の約２倍の幅（Ｄ）を有することを特徴とする請求項１から４のいずれか１項に記載の半導体素子。

【請求項６】　中間層（２）の一部はドナーが高濃度にドープされて感光性半導体素子の陰極（４）として用いられ、陰極（４）、陽極（３０）並びに場合によっては基板（１）が、同様に基板（１）上に配置された電子読み出し装置（７、１９）に接続されることを特徴とする請求項１から５のいずれか１項に記載の半導体素子。

【請求項７】　１つまたは複数の基板（１）と、少なくとも２つの中間層（２、2*）と、少なくとも２つの外部層（５、5*）からなり、少なくとも部分的に中間層（２、2*）が基板（１）の内部に、また外部層（５、5*）が対応する中間層（２、2*）の内部に埋め込まれており、基板（１）、中間層（２、2*）並びに外部層（５、5*）により少なくとも２つの感光性領域（２２、２２*）が形成され、光依存性の信号（２０ａ、２０ｂ）が生成される感光性半導体装置において、
第１の外部層（５）が、対応する中間層（２）の中間領域（１３）によって分離された互いに離間した領域（１１）からなり、
対応する中間層（２）を有する第１の外部層（５）により深さ（X_b）を有する第１の感光性領域（２２）が形成され、
第２の外部層（5*）は対応する中間層（2*）と短絡されていて、第２の中間層（2*）の一部と基板（１）からなる第２の感光性領域（２２*）が深さ（X_b）の下方に形成されることを特徴とする感光性半導体装置。

【請求項８】　第１の感光性領域（２２）を用いて入射光の予め定められた波長領域が検出され、また第２の感光性領域（２２*）を用いて入射光の他の波長領域が検出されることを特徴とする請求項７に記載の半導体装置。

【請求項９】　第１の感光性領域（２２）を用いて入射光の予め定められた波長領域が検出され、また第２の感光性領域（２２*）を用いて隣接する波長領域が検出され、対応する層（２、2*、５、5*）が電子読み出し装置（７、１９）と接続されて、第１の感光性領域（２２）によって検出された隣接する波長領域成分がほぼ抑圧されることを特徴とする請求項７または８に記載の半導体装置。

【請求項１０】　第１の感光性領域（２２）により第１の信号（２０ａ）が、また第２の感光性領域（２２*）により第２の信号（２０ｂ）が生成され、光が入射したとき第２の信号（２０ｂ）が所定の波長（W_{tIR}）から第１の信号（２０ａ）とほぼ等しい大きさになるように、第２の感光性領域（２２*）が構成されていることを特徴とする請求項７から９のいずれか１項に記載の半導体装置。

【請求項１１】　第１の感光性領域（２２）を用いて主に紫外線が検出され、また第２の感光性領域（２２*）を用いて主に赤外線が検出され、第１の感光性領域（２２）により第１の光電流（I_{phUV}）が、また第２の感光性領域（２２*）を用いて第２の光電流（I_{phIR}）が生成され、光が入射したとき第２の光電流（I_{phIR}）が約４００から５００ｎmの波長から第１の光電流（I_{phUV}）とほぼ等しい大きさになるように、第２の感光性領域（２２*）が構成されていることを特徴とする請求項７から１０のいずれか１項に記載の半導体装置。

【請求項１２】　請求項１から６のいずれか１項に記載の半導体素子または請求項７から１１のいずれか１項に記載の半導体装置を有する感光性回路において、
半導体素子または感光性半導体装置および／または電子読み出し装置（７、１９）のすべての層が、基板（１）上にＣＭＯＳ技術で一緒に製造されることを特徴とする感光性回路。

【請求項１３】　請求項１から６のいずれか１項に記載の半導体素子または請求項７から１１のいずれか１項に記載の感光性半導体装置あるいは請求項１２に記載の回路を用いて、空気と燃料の混合気の燃焼により発生する、特に暖房装置のバーナーの火炎を制御する方法にお

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いて、
火炎によって発生される光の所定の波長領域が検出されて、この波長領域の有無および／または強度に基づき空気と燃料の混合気が調節されることを特徴とする火炎を制御する方法。
【請求項１４】　火炎の有無が検出されることを特徴とする請求項１３に記載の方法。
【請求項１５】　それぞれ異なる波長領域を選択する複数の感光性半導体装置が並べて配置され、これらの半導体装置が互いに接続され、周波数分布に基づいて火炎の燃焼および／または強度が調節されることを特徴とする請求項１３または１４に記載の方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、請求項１のおいて書きに記載の感光性半導体素子、請求項７のおいて書きに記載の感光性半導体装置、請求項１２に記載の感光性回路、並びにこの感光性半導体素子ないしは感光性半導体装置を使用して火炎を制御する請求項１３に記載の方法に関するものである。
【０００２】
【従来の技術】この種の感光性半導体素子は、フォトダイオードまたはフォトトランジスタとしても知られており、所定にドーピングされた半導体素子のいわゆるｐｎ接合として既に存在し、たとえばスツェ（Ｓ．Ｍ．Ｓｚｅ）の「セミコンダクタデバイスの物理学（Ｐｈｙｓｉｃｓ　ｏｆ　Ｓｅｍｉｃｏｎｄｕｃｔｏｒ－Ｄｅｖｉｃｅｓ）」第2版、１９８１年、Ｊｏｈｎ　Ｗｉｌｅｙ　＆　Ｓｏｎｓ、Ｉｎｃ．出版社、第Ｖ部、第１３章「光電検出器（Ｐｈｏｔｏｄｅｔｅｃｔｏｒｓ）」に記載されている。この光電検出器ないしは感光性半導体素子は、光、すなわち可視光または不可視光、たとえば紫外線または赤外線の検出に用いられる。この種の感光性半導体素子の品質を記述する３つの重要なパラメータは、感度、すなわちスペクトル感度（所定波長における感度）、応答時間、すなわち光の入射からセンサ信号の検出までの時間、並びに量子効率である。
【０００３】また、この種の感光性半導体素子はすでに知られており、たとえばジョーンズ（Ａ．Ｒ．Ｊｏｎｅｓ）の「火炎欠陥検出と最新のボイラー（Ｆｌａｍｅ　ｆａｉｌｕｒｅ　ｄｅｔｅｃｔｉｏｎ　ａｎｄ　ｍｏｄｅｒｎ　ｂｏｉｌｅｒｓ）」、Ｊ．Ｐｈｙｓ．Ｅ．：Ｓｃｉ．Ｉｎｓｔｒｕｍ．２１（１９８８）、９２１－９２８には、極めて高い感度を有していて本質的に選択性のある、いわゆる紫外線に感度を有するガス放電管が記載されている。しかしこの種のタイプの光電検出器は、極めて高価であって、壊れやすく、大きな外形寸法を有し、かつ極めて高いエネルギー供給を必要とする。
【０００４】さらに、所定の選択性を得るために、フィルタを外付けしたまたはフィルタを内蔵した従来型のシリコンフォトダイオードが知られている。このフォトダイオードは、極めて小型で、ほとんど壊れない。ＵＶ領域（紫外線領域）において高い選択性を得るために、すなわち可視光と可視領域に隣接する赤外線をフィルタで除去するために、干渉フィルタが使用されている。それにもかかわらず、この種のＵＶフォトダイオードは、極めて高価である。というのは、干渉フィルタがコストを高いものにし、それによって大量生産に使用するための回路全体を魅力のないものにしているからである。しかし一方では、低い値段帯の干渉フィルタも存在するが、その干渉フィルタは可視光と可視領域に接する赤外線に対するフィルタ特性がよくないので、選択性は多くの使用例で十分ではない。
【０００５】市販されている高選択性のＵＶフォトダイオードが、たとえばポポヴィック他（Ｒ．Ｓ．Ｐｏｐｏｖｉｃ　ｅｔ　ａｌ．）の「シリコン紫外線検出器（Ａ　ｓｉｌｉｃｏｎ　ｕｌｔｒａｖｉｏｌｅｔ　ｄｅｔｅｃｔｏｒ）」、Ｓｅｎｓｏｒｓ　ａｎｄ　Ａｃｔｕａｔｏｒｓ、Ａ２１－Ａ２３、１９９０、５５３－５５８に記載され、かつＥＰ０２９６３７１から知られている。その場合、このＵＶフォトダイオードは、高い選択性を得るために、対応する半導体層をドーピングするとき極めて煩雑で手間のかかる最適化プロセスを受ける。それによってこのフォトダイオードは極めて高価であり、大量生産での使用には、まったく適していない。
【０００６】光を検出するこれら公知の半導体素子、すなわちたとえばフォトダイオードは、シリコン(ケイ素)からなる基板を有し、その中に中間層と外部層が少なくとも部分的に埋め込まれている。この中間層と外部層は、異なるドーピングにより異なる特性にされ、すなわちたとえばアクセプタあるいはドナーがドープされて、それにより光電流に必要なｐｎ接合が形成されている。中間層と外部層は感光性領域を形成し、光依存性の信号、すなわちたとえば光電流を発生させる。感光性領域では、光子が入射すると、いわゆる電荷担体（キャリヤ）、すなわち半導体の伝導帯ないし価電子帯に存在する電子と正孔が形成される。この電荷担体の移送によって、場合によってはさらに電荷担体を発生させることによって（なだれ効果）、光電流が発生し、その光電流はこの層の表面に設けた対応する接点によって測定することができる。それぞれ対応する半導体層の構造とドーピングによって、電荷担体の生成、移送並びに速度を調節することができる。しかし多くの場合、この種の素子を製造するために必要な質的な要請は、それ自体矛盾している。
【０００７】従って従来の感光性半導体素子は、高い選択性をもつが、その場合は非常に大型で極めて高価であり、あるいは小型で安価ではあるが、その場合は選択性がわずかであるか有効性に欠けている。従って、重要な電子回路に信頼性をもって使用することはできない。た

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とえば「フェイル−セイフ」特性を保証すべき監視回路用に所定の感光性半導体素子が設けられる。この場合も、これまでは、安価であると同時に簡単に製造することができる利用可能な解決策はまだ見出されていない。

【０００８】たとえば、個人家屋または工業的な建物の暖房装置のバーナーにおける火炎の監視に使用するため、火災警報システムのため、あるいは建物監視システムのための従来の感光性半導体素子は、十分に高い選択性と十分な量的な効果を有する場合には、相応の単価では、現在では入手することはできない。

【０００９】

【発明が解決しようとする課題】従って本発明の課題は、従来技術の欠点を解決し、小さくて丈夫で、さらに非常に高い選択性、有効性並びに極めて高い検出能力を有し、標準技術ないしは標準プロセスによって安価に製造することができる、上述した種類の感光性半導体素子ないしは感光性の半導体装置を提供することである。

【００１０】

【課題を解決するための手段】本発明によれば、この課題は、基板（１）、中間層（２）および外部層（５）からなり、少なくとも部分的に中間層（２）が基板（１）の内部に、また外部層（５）が中間層（２）の内部に埋め込まれており、中間層（２）と外部層（５）により感光性領域（２２）が形成され光依存性の信号（Ｒ）が生成される感光性半導体素子において、外部層（５）が、中間層（２）の中間領域（１３）によって分離された互いに離間した領域（１１）からなることを特徴とする感光性半導体素子によって解決される（請求項１）。

【００１１】また、この課題は、１つまたは複数の基板（１）と、少なくとも２つの中間層（２、2*）と、少なくとも２つの外部層（５、5*）からなり、少なくとも部分的に中間層（２、2*）が基板（１）の内部に、また外部層（５、5*）が対応する中間層（２、2*）の内部に埋め込まれており、基板（１）、中間層（２、2*）並びに外部層（５、5*）により少なくとも２つの感光性領域（２２、２２*）が形成され、光依存性の信号（２０ａ、２０ｂ）が生成される感光性半導体装置において、第１の外部層（５）が、対応する中間層（２）の中間領域（１３）によって分離された互いに離間した領域（１１）からなり、対応する中間層（２）を有する第１の外部層（５）により深さ（X_b）を有する第１の感光性領域（２２）が形成され、第２の外部層（5*）は対応する中間層（2*）と短絡されていて、第２の中間層（2*）の一部と基板（１）からなる第２の感光性領域（２２*）が深さ（X_b）の下方に形成されることを特徴とする感光性半導体装置によって解決される（請求項７）。

【００１２】さらに、請求項１２には、感光性回路が、そして請求項１３には請求項１と７の特徴に基づくこの感光性半導体素子ないしは感光性半導体装置を使用した、火炎を制御する方法が記載されている。本発明の他の形態は、対応する従属請求項から得られる。

【００１３】本発明による感光性半導体素子は、基板、中間層並びに外部層からなり、少なくとも部分的に中間層が基板の内部に、また外部層が中間層の内部に埋め込まれている。中間層と外部層により、感光性領域が形成され、たとえば光電流のような、光依存性の信号が発生される。外部層は、たとえばアクセプタが高濃度にドープされた（P^+ドーピング）シリコンからなり、中間層の中間領域によって分離された互いに離間した領域に分割される。その場合、中間層は、たとえばドナーがドープされた（Ｎドーピング）シリコンからなり、一方基板はアクセプタがドープされた（Ｐドーピング）シリコンから形成されて、中間層と外部層は感光性半導体素子の表面に支持される。

【００１４】外部層の離間した領域は、たとえば感光性半導体素子の陽極（アノード）として用いられ、その半導体素子はフォトダイオードとして用いられ、対応した電子検出装置（電子読み出し装置）に接続される。中間層はさらに、ドナーが高濃度にドープされた（N^+ドーピング）領域を有し、その領域がたとえば感光性半導体素子の陰極（カソード）として用いられ、その領域は必要に応じて、アクセプタが高濃度にドープされた（P^+ドーピング）基板領域と短絡される。

【００１５】本発明による半導体素子の極めて高い選択性は、外部層を互いに離間した領域に分割することによって得られる。その場合、外部層は、中間層（N_{well}）内に埋め込まれているので、感光性領域を外部層の表面から測って所定の深さまでに制限する電位障壁が形成される。従来の半導体素子においては、外部層の表面におけるドーピング濃度（たとえばホウ素によるP^+ドーピング）は、大きな光電流を得るためには、特に高濃度のドーピングが望まれるのにもかかわらず、ドーピング効果とドーピング原子の再分布（「ｒｅｄｉｓｔｒｉｂｕｔｉｏｎ」）によって減少する。互いに離間した領域は、外部層が中間層へ埋め込まれていく過程で形成される外部層の表面の「不活性な」層の形成を防止する（図３を参照）。この不活性な領域は、光子により発生された電荷担体、すなわち電子と正孔が再結合することから発生し、それによってこれらの電荷担体はもはや光電流を発生させることができず、従って発生した光電流は、望ましいことではないが下降してしまう。

【００１６】本発明の感光性半導体素子においては、電子と正孔が再結合されるのではなく、分離してそれぞれの陽極ないし陰極へ流れ、そこで電子読み出し装置によって検出されることが特に重要である。外部層の外表面では電子と正孔の発生はそれ自体最大となるが、入射光により発生する電子と正孔のこの外表面での再結合により、発生した光電流は顕著に減少する。この再結合は、上述したように、ドーピングされた外部層の外表面領

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域、すなわち上述した不活性領域において、ドープされたホウ素原子の濃度が減少することによって発生し、これには種々の物理的な原因が考えられる。たとえば外表面ではドーピング効果が非常に強くなり、ホウ素原子が再分布されるので、この外表面でホウ素濃度を高くしなければならないのに、ドープされたホウ素原子の濃度が低くなってしまう。

【００１７】外部層の離間した領域を設けることによって、不活性層の発生が顕著に防止される。離間した領域間のドナーがドープされているシリコン原子の伝導帯の下限と価電子帯の上限間のエネルギー帯の構造に変化がもたらされるので（図５を参照）、それによって発生する離間した領域間の電位に支持されて、この領域に存在する少数キャリア（正孔）が下方へ押しやられ、電子と正孔の再結合は行われないか、あってもごくわずかになる。それによって外部層の表面では、入射光に対する所望の高い応答性が得られる。というのは、入射する光子によって発生される電子と正孔は、ほぼ完全に陽極ないし陰極へ流れ、その前に再結合されることはないからである。それによって、フォトダイオードが設計された所定波長領域の光電流がほぼ完全に得られるようになる。

【００１８】この幾何学的な構成によって、入射光に対する選択性が極めて高くなるだけでなく、極めて安価でかつ標準技術により製造可能な素子が得られ、大量生産できる素子であるという要請並びに素子の品質に関しても適した素子が得られる。

【００１９】その場合、すべての層は、標準構成として一体のセンサとして構成でき、公知のＣＭＯＳ技術により一緒に同じ一つの基板内へ拡散させることができる。全体の感光性半導体素子を、好ましくは同様に同じ一つの基板上にＣＭＯＳ技術で実現される電子検出装置と接続して一体化された構造にすることによって、極めて安価な価格で製造できるようになる。それによって様々な利用のために、１つのプロセスで一緒に、場合によっては電子検出装置と共に、同じ一つのチップ上に構成することのできる極めて安価で小型かつ頑丈な感光性半導体が製造できる。

【００２０】個々の層をどのようにドーピングするかに従って、ないしは感光性領域の厚みに応じて、光の種々の波長領域を検出でき、その場合、感光性半導体素子の表面の対応する領域を離間させることによって常に所望の選択性が得られる。離間した領域、中間領域並びに中間層の一部を包囲する感光性領域は、入射光のほぼ１波長（W_t）の長さの深さ（X_b）を有し、それにより入射光の所定波長領域が検出される。

【００２１】たとえば、紫外線を検出するための感光性領域は、約０．０１から０．８μｍ、特に０．１から０．４μｍで、好ましくは０．５μｍの深さを有する。その場合、中間領域は、好ましくは感光性領域の深さの約２倍の大きさの幅を有する。というのは、それによって互いに離間した領域をできるだけ小さくすることができるとともに、中間領域は大きくなり過ぎず、漏れ電流、すなわち正孔がその下にある基板へ拡散することが防止されるからである。

【００２２】本発明はさらに、１つまたは複数の基板と、少なくとも２つの中間層と、少なくとも２つの外部層とからなる感光性半導体装置を開示する。その場合、少なくとも部分的に中間層は基板の内部に、また外部層は対応する中間層の内部に埋め込まれている。基板、中間層および外部層は、少なくとも２つの感光性領域を形成し光依存性の信号を発生させる。第１の外部層は、対応する中間層の中間領域によって分離された互いに離間した領域からなる。この領域の機能は、上述した機能と同一であり、第１の外部層の表面に不活性層が形成されるのを防止することである。第１の外部層は、対応する中間層と共に、上述したのと同様にｐｎ接合の電位障壁によって限定される所定深さの第１の感光性領域を形成する。第２の外部層は、対応する中間層と短絡されているので、第２の中間層の一部と基板とからなる第２の感光性領域が、ほぼ上記所定の深さに対応する第２の外部層からの深さの下方に形成される。

【００２３】第１の感光性領域を用いて、入射光の予め定められた波長領域（周波数領域）が検出され、また第２の感光性領域を用いて入射光の他の波長領域、好ましくは入射光の予め定められた波長領域に隣接する波長領域が検出される。その場合、半導体素子の対応する層は、電子読み出し装置と接続され、第１の感光性領域によって検出された隣接する波長領域成分がほぼ抑圧される。これは、第２の感光性領域によって検出された入射光信号の大きさが、２つが重なる領域において第１の感光性領域により生成された信号にほぼ相当する場合に可能になる。第２の感光性領域は、光が入射したときこの領域で生成される第２の信号が、所定の波長（W_{tIR}）から、第１の感光性領域で生成される第１の信号とほぼ等しい大きさになるように、構成されている。

【００２４】第１の感光性領域は、たとえば特に紫外線を検出するように、また第２の感光性領域は特に赤外線を検出するように構成されている。第１の感光性領域は第１の光電流を発生させ、第２の感光性領域は第２の光電流を発生させ、その場合、第２の感光性領域は、光が入射したとき第２の光電流が約４００から５００ｎｍの波長から第１の光電流とほぼ等しい大きさになるように、構成されている。

【００２５】この「第１の」感光性半導体素子と並んで配置された「第２の」感光性半導体素子は、たとえば赤外線を検出する機能を有し、その場合、両半導体素子は互いに接続され、紫外線（ＵＶ）センサの光電流から赤外線（ＩＲ）センサの光電流が減算されるので、紫外線選択性が増大する。その場合、対応する感光性領域の層厚に従い、発生する光電流を調節し、ＵＶ光電流とＩＲ

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光電流が重なる領域では同じになるようにすることができるので、両電流を減算したとき、UV領域外ではほぼゼロに等しい出力信号が発生する。

【００２６】両感光性半導体素子、すなわち対応する各層は、この場合も１つの同じ基板上で実現され、その場合同様にCMOS技術を使用することができる。UVフォトダイオードを対応したIRフォトダイオードと組み合わせることによって、高価な干渉フィルタまたはカラーフィルタを使用する必要がなくなる。それによって全体として、入射光の種々のスペクトル領域を検出するための極めて安価でしかも選択性の高いフォトダイオードないしは感光性半導体素子が得られる。

【００２７】この感光性半導体素子によって、小型で安価であり、周波数ないし波長選択性があり、高速で頑丈で、しかも信頼性の有る効果的な感光性回路が実現できる。その場合、半導体素子または感光性半導体装置および／または電子読み出し装置のすべての層は、CMOS技術で基板上に一緒に形成することができる。それによってフィルタ、接続装置などが省略できる。

【００２８】本発明による半導体素子は、特に空気と燃料の混合気の燃焼によって発生する暖房装置のバーナーの火炎を制御する方法に使用される。この火炎は、空気と燃料の混合の調節に従って異なる強度と異なる燃焼値で燃焼し、その場合、それぞれ異なるスペクトル領域の光が放出される。本発明による極めて周波数選択性のある半導体素子によって、火炎により発生する光の所定スペクトル領域ないしは所定波長領域が検出され、この波長領域の有無および／または強度に基づいて空気と燃料の混合気が調節される。その場合、それぞれ異なる波長領域を選択する感光性半導体装置を複数配置し、これらを互いに接続して、周波数分布に基づいて火炎の燃焼および／または強度を制御するようにすることができる。この「周波数検出器」の「マトリクス」は、本発明によって付加的なフィルタや他の構成素子を設けることなく共通のチップ上に実現することができる。これにより可視光用のCCDカメラの原理に基づく一種の「カメラ」が得られ、その場合、マトリクスのすべての素子が同時に電子検出装置に電流を送るのではなく、そのとき放出された周波数に応答する素子のみが電流を送ることになる。

【００２９】

【発明の実施の形態】本発明の幾つかの好ましい実施形態を、図面を用いて詳細に説明する。

【００３０】図１には、基板１、中間層２および外部層５を有する従来構造の感光性半導体素子が図示されている。中間層２は基板１の内部に、また外部層５は中間層２の内部に部分的に埋め込まれており、中間層２と外部層５は感光性領域２２（ハッチングで示す）を形成し、光依存性の信号を生成する。感光性領域２２は、電位障壁により下方へ向かって深さX_bまでに制限ないし限定されている。アクセプタが高濃度にドープされた（P^+ドーピング）外部層５と、ドナーが高濃度にドープされた（N^+ドーピング）領域４間には、電位が発生する中間領域１８が存在する。外部層５とドナーがドープされた（Nドーピング）中間層（N_{well}）の一部が一緒になって感光性領域２２を形成する。

【００３１】図１の右側には、感光性半導体素子の接続が図示されており、同図で外部層５が陽極（アノード）３０を示し、アクセプタがドープされた（Pドーピング）基板１の内部にあるアクセプタが高濃度にドープされた（P^+ドーピング）領域３は導線６を介して陰極（カソード）４と短絡されている。電流計７が、感光性領域２２によって発生される電流を検出する。図１に示す半導体素子は、特にUV（紫外線）選択性のフォトダイオードであって、UV光を検出できるように構成されている。

【００３２】図２は、図１に示す線Aに沿った半導体素子のドーピング濃度の図表である。図表の垂直軸は、ドーピング原子Dcの濃度を粒子／cm^3で示している。横軸は、外部層５の表面からその下に位置する基板１の方向の深さTをμmで示している。中間層２は、アクセプタがドープされた基板１内で燐（リン）原子（ドナー）を用いてドープされており、外部層５は中間層２内でホウ素原子（アクセプタ）を用いて高濃度にドープされている。図表から明らかなように、ホウ素原子の濃度８は約５００nmの深さX_bまで連続的に減少し、一方、燐原子の濃度９は中間層２と基板１間の接合部（深さX_bの約２倍）までほぼ一定である。

【００３３】従って図２のドーピング構成は、代表的な０．５μm標準C－MOSプロセスに相当する。ドーピング濃度、すなわちホウ素原子の濃度８は、深さX_Dにおいて最大となり、この深さX_Dから表面までは減少していることが理解できる。大きな光電流を得るにはここで特に高濃度のドーピングが望まれるにもかかわらず、ドーピング効果とドーピング原子の「再分布」により望ましくない効果が、不可避的に発生する。それによって外部層５の外端領域には、シリコン表面、すなわちまさに入射光（たとえば紫外線）の最も多くの光子が吸収される場所に、「不活性層」ないし「不感層」１２が形成される。

【００３４】図３は、図１の線Aに沿った図２に示すドーピング濃度を有する半導体素子の材料の外側エネルギー帯を概略的に示す。下方の価電子帯１０bと上方の伝導帯１０a並びに表面から下方の基板１方向に測定したエネルギーレベルが図示されている。深さX_bに感光性領域２２を限定してしまう電位障壁が存在していることがわかる。しかし、外部層５の表面１２では深さX_Dまでは両バンド１０aと１０bのエネルギーレベルが下降することも認められる。この効果は、上述した「不感層」１２によってもたらされる。光子によって生成され

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る外部層５、従って外表面の少数キャリア１４（電子）は、上述した効果によりホウ素濃度８が減少することによって、「不感層」１２内で再結合する。それによってこれらの電子（そしてそれに対応する正孔、すなわち多数キャリア）は光電流に寄与せず、入射光に対する半導体素子の感度は小さくなり、従ってその選択性は悪くなる。

【００３５】図４は、本発明による感光性半導体素子を示している。本発明による感光性半導体素子は、基板１、中間層２および外部層５からなり、少なくとも部分的に中間層２が基板１の内部に、また外部層５が中間層２の内部に埋め込まれている。中間層２と外部層５は、感光性領域２２を形成し、たとえば光電流のような光依存性の信号を生成する。アクセプタが高濃度にドープされたシリコンからなる外部層５は、互いに離間した領域１１に分割されており、これらの領域１１は中間層２の中間領域１３によって分離されている。中間層２はドナーがドープされたシリコンからなり、基板１はアクセプタがドープされたシリコンから形成され、感光性半導体素子の表面に中間層２と外部層５が支持されている。

【００３６】外部層５の離間した領域１１は、図１について説明したのと同様に、感光性半導体素子の陽極３０として用いられる。接続も、図１と同一である。

【００３７】本発明による感光性半導体素子の極めて高い選択性は、外部層５が互いに離間した領域１１に分離されていることによって得られる。幅Ｌを有し、かつ距離Ｄで互いに分離された離間した領域１１により、外部層５の表面の不活性層、すなわち「不感」層の形成が防止される。

【００３８】図５に概略的に示すように、図４の線Ｂに沿った半導体素子の外部エネルギー帯の構造は変化する。外部層５の離間した領域１１間、すなわち中間領域１３内のドナーがドープされたシリコン原子の伝導帯１０ａ*の下限と価電子帯１０ｂ*の上限間のエネルギー帯は、外部層５の表面と深さX_b間で、深さX_bから表面方向に見て下方へ湾曲したカーブとなっているので、それによって離間した領域１１間に発生する電位により支援されて、この領域に存在する少数キャリア１４*（正孔）が深さX_bの方向に、すなわち表面から離れ基板１の方向へ押しやられる。「不感層」１２は、離間した領域１１間に発生する電位によって最小限に減少される。すなわち外部層の上端縁においては、電子と正孔の再結合は発生せず、ないしは発生してもわずかでしかない。

【００３９】図２から明らかなように、中間層２、すなわち外部層５の中間領域１３内の燐原子の濃度９は、外部層５の端縁へ向かって増大している。これは、シリコン／二酸化シリコン接合における偏析（Ｓｅｇｒｅｇａｔｉｏｎ）に基づいている。この増大により、図５に示すエネルギー帯において、外部層５の表面近傍の両バンド１０ａ*と１０ｂ*に軽微なエネルギー降下がもたらされるので、正孔１４*が深い方へ押しやられ、望ましくない再結合が防止される。「不感領域」は減少してＬ／（Ｌ＋Ｄ）倍になる。その場合、互いに離間した領域１１の幅Ｌは、技術的に実現可能な限り狭く設計することができるが、この領域１１間の距離Ｄには最適な値が存在し、それは深さX_bの約２倍の大きさである。距離Ｄをもっと狭くすると、「不感層」１２が増大し、距離Ｄをもっと大きくすると、正孔はさらに下方へ押しやられるので、正孔が基板１内へ拡散し、それによって同様に光感度が減少する。

【００４０】これにより外部層の表面には、入射光に対して所望の高い応答性が得られる。というのは、入射する光子により生成される電子と正孔はほぼ完全に陽極ないし陰極へ流出し、それに先だって再結合されてしまうことがないからである。それによってフォトダイオード用に設計された所定の波長領域の光電流をほぼ完全に利用できるようになる。

【００４１】図６は、従来の半導体素子に比較して、本発明による半導体素子の応答性を表す図表である。本発明による中間領域１３を用いない場合(ストライプなし)入射光の波長Ｗ（ｎｍ）に対する応答性、すなわち感光性領域２２によって発生される半導体素子の信号Ｒ（カーブ１５で示す）と、本発明による中間領域１３を用いた場合(ストライプあり)の半導体素子の応答性ないしその信号（カーブ１７で示す）と、両カーブ１５および１７の互いに対する比ｒ（カーブ１６で示す）が図示されている。本発明による半導体素子のカーブ１７の信号Ｒが、所定の波長W_tまでは従来の半導体素子の信号Ｒよりも強いことが理解できる。約３００ｎｍの波長において、比ｒが最大となり約r_{max}＝１．６５の値を有する。その場合に幅Ｌは、約０．６μｍの値を有し、距離Ｄは約１．０μｍである。

【００４２】本発明による半導体素子は、さらに他の利点を有する。０Ｖを中心とする領域の電圧と電流比に相当する分路抵抗R_{sh}は、接合領域ないし空乏層面の大きさに間接的に比例し、距離Ｄが大きくなるにつれて増大する。この抵抗はフォトダイオードに発生するオフセット電圧に間接的に比例するので、抵抗が大きくなるほど、オフセット電圧は小さくなる。この抵抗は、本発明による「ストライプ層」５において、すなわち離間した領域１１によってより大きくなることにより、このオフセット電圧が減少する。これは特に、このオフセット電圧が問題となりかねない、高温度において重要である。さらに、離間した領域１１を設けることによって、フォトダイオードのキャパシタンスが減少される。このキャパシタンスは信号電圧との相互作用により応答時間を遅延させてしまう。これも接合領域ないし空乏層面が減少することに起因する。

【００４３】図７は、接続が異なる感光性半導体素子を示している。配置は、図１の配置に対応するが、Ｐ型基

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板１内のアクセプタが高濃度にドープされた領域３ではなく、外部層５*が導線６を介して陰極４*と短絡されているところが相違する。それによって中間層２*と基板１間に深さX_bから感光性領域２２*が形成される。電流計７は、感光性領域２２*によって生成される電流を検出する。図７に示す半導体素子は、特に赤外線選択性のあるフォトダイオードであって、異なる接続によって、入射光の波長が長いことにより約５００ｎｍの深さより深い位置にある層内に生成される電荷担体を検出する。

【００４４】図８は、図４と図７に示す半導体素子を備えた本発明による感光性半導体装置を示している。感光性半導体装置は、基板１、２つの中間層２、２*および２つの外部層５、５*からなり、その場合、中間層２、２*は基板１の内部に、また外部層５、５*は対応する中間層２、２*の内部に部分的に埋め込まれている。基板１、中間層２、２*および外部層５、５*が、少なくとも２つの感光性領域２２、２２*を形成し、光依存性の信号２０ａ、２０ｂ（図９を参照）を生成する。第１の外部層５は、互いに離間した領域１１からなり、対応する中間層２と共に深さがX_bの第１の感光性領域２２を形成する。中間層２*を有する第２の外部層５*は、図７に示すように短絡されているので、深さX_bの下方に第２の中間層２*の一部と基板１とからなる第２の感光性領域２２*が形成される。

【００４５】基板は電位V_{ss}にあり、中間層２は電位V_{dd}にある。第１の外部層５、第２の外部層５*並びに第２の中間層２*は、出力増幅器（演算増幅器）７によって形成される仮想電位V_{dd}にある。従って出力増幅器７の入力領域では、電位V_{dd}を中心とする分極が可能になるので、最少の光電流でも測定することができる。しかし、V_{dd}の代わりに、正の基準電圧を出力増幅器の分極に利用することも可能である。

【００４６】図９に示すように、第１の感光性領域２２により第１の信号（２０ａ）が、また第２の感光性領域２２*により第２の信号２０ｂが発生される。その場合、第２の感光性領域２２*は、光が入射したとき第２の信号２０ｂが所定の波長W_{tIR}から第１の信号２０ａとほぼ同じ大きさになるように、構成されている。

【００４７】特に、第１の感光性領域２２は紫外線を検出するのに適しており、一方第２の感光性領域２２*は赤外線を検出するのに適している。これは、第１の感光性領域２２により第１の光電流（光電電流）I_{phUV}が発生され、また第２の感光性領域２２*によって第２の光電流I_{phIR}が発生されることにより、また、光が入射したとき第２の光電流I_{phIR}が約４００から５００ｎｍの波長から、第１の光電流I_{phUV}とほぼ同じ大きさになるように第２の感光性領域２２*が構成されていることによる。演算増幅器７は、両信号２０ａと２０ｂを減算することによって得られる図１０に示す合成信号２１を検出する。その場合、この信号は波長W_{tUV}において最も強くなり、第２の半導体素子が検出する波長W_{tIR}の方向には顕著に減少する。従って選択性が向上し、個々の波長領域をシャープに検出するための「一体型の」フィルタが得られる。

【００４８】

【発明の効果】以上説明したように、本発明の半導体素子ないし半導体装置は、外部層が互いに離間した領域に分割され、ストライプ層になっているので、周波数選択性が極めて高くなり、また小型で丈夫であって、しかも高い検出能力を有するとともに、標準的なプロセスで安価に製造できる、という効果が得られる。

【図面の簡単な説明】

【図１】従来構造の感光性半導体素子の構成を示す構成図である。

【図２】図１のＡに沿った半導体素子のドーピング濃度を示す線図である。

【図３】図１の線Ａに沿った半導体の外部エネルギー帯を概略的に図示する線図である。

【図４】本発明による感光性半導体素子の構成を示す構成図である。

【図５】図４に示す線Ｂに沿った半導体素子の外部エネルギー帯を概略的に示す線図である。

【図６】本発明による半導体素子の応答性を従来の半導体素子に比較して示す線図である。

【図７】赤外線検出用の感光性半導体素子の構成を示す構成図である。

【図８】図４と図７に示す半導体素子を有する感光性半導体装置の構成を示す構成図である。

【図９】図８に示す感光性半導体装置の光電流を示す線図である。

【図１０】図９に示す両信号を組み合わせたときに得られる信号を示す線図である。

【符号の説明】

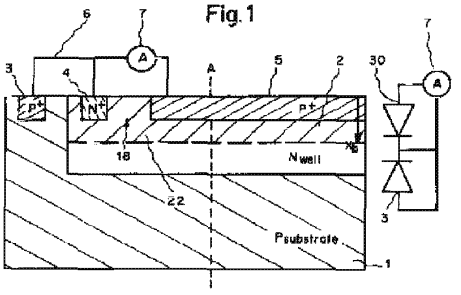
１　基板
２　中間層
５　外部層
１１　離間した領域
１３　中間領域
２２　感光性領域

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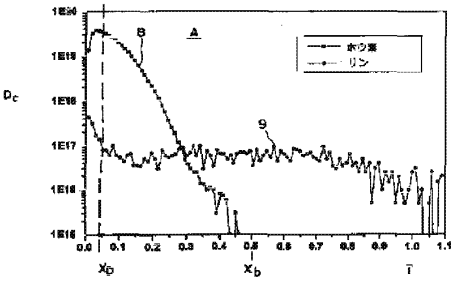
【図1】

Fig.1



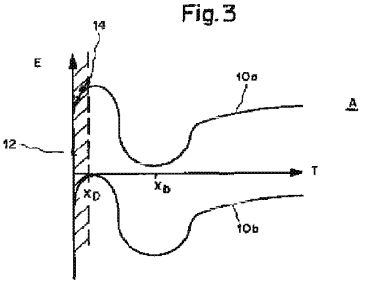
【図2】

Fig.2



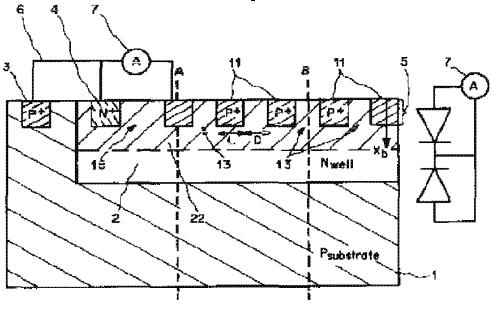
【図3】

Fig.3



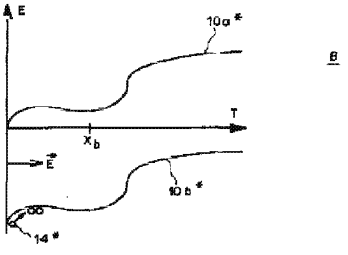
【図4】

Fig.4



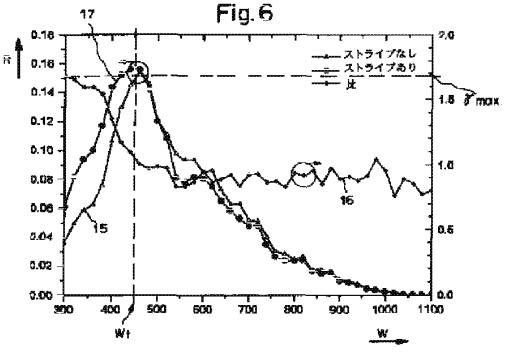
【図5】

Fig.5



【図6】

Fig.6

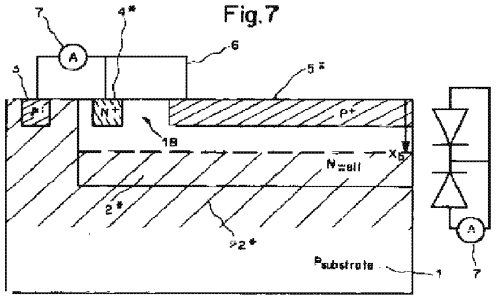


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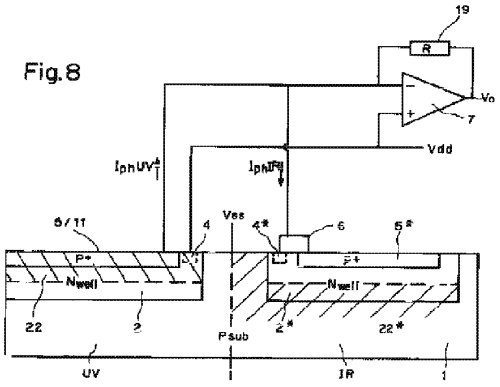
【図7】

Fig.7



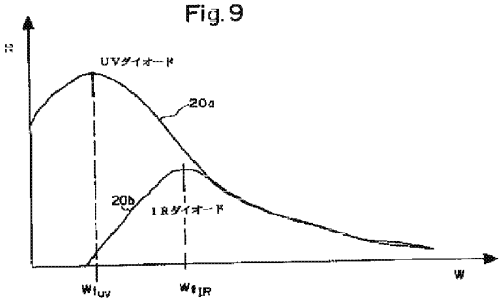
【図8】

Fig.8



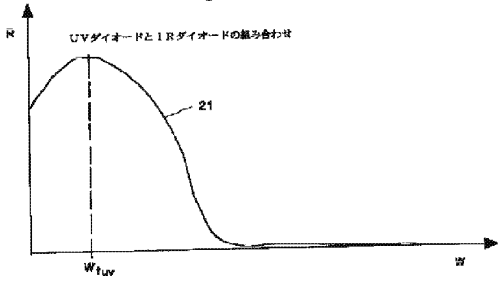
【図9】

Fig.9



【図10】

Fig.10



フロントページの続き

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Espacenet

Bibliographic data: JP2002043594 (A) — 2002-02-08

OPTICAL TRANSMISSION TYPE THIN FILM SOLAR CELL MODULE

Inventor(s): OUCHIDA TAKASHI ± (OUCHIDA TAKASHI)

Applicant(s): SHARP KK ± (SHARP CORP)

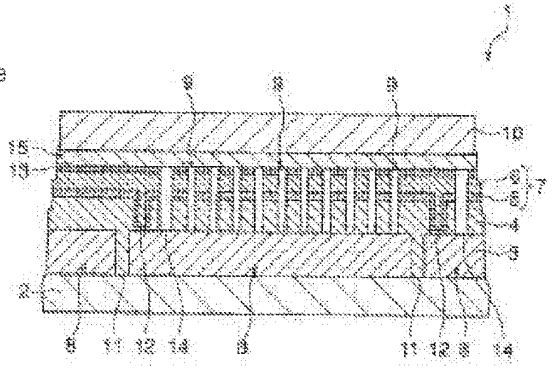
Classification: **- international:** ***H01L31/04;*** (IPC1-7): H01L31/04
- cooperative: Y02E10/50

Application number: JP20000221029 20000721

Priority number(s): JP20000221029 20000721

Abstract of JP2002043594 (A)

PROBLEM TO BE SOLVED: To provide an optical transmission type thin film solar cell module capable of obtaining a high output by reducing a photodegradation. SOLUTION: The optical transmission type thin film solar cell module comprises a solar cell formed by sequentially laminating a transparent surface electrode layer, a photoelectric conversion layer and a back electrode layer on an optical transmission substrate, a transparent portion for transmitting from the surface electrode layer through the conversion layer and the back electrode layer, and a transparent sealing material covering the back electrode layer so that the sealing material has a light absorptivity of 40% or more in a near infrared wavelength region of 500 to 2,000 nm and thus a deterioration of the photoelectric conversion efficiency is prevented.



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特開2002－43594
（P2002－43594A）
(43)公開日　平成14年２月８日(2002.2.8)

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Ｈ０１Ｌ　31/04		Ｈ０１Ｌ　31/04	Ｂ　５Ｆ０５１

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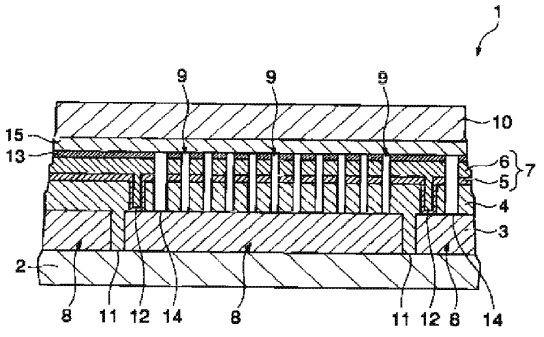
(22)出願日　平成12年７月21日(2000.7.21)

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Ｆターム(参考)　5F051 AA05 BA17 CB25 CB27 DA04 EA01 FA02 GA03 JA02 JA04 JA05

(54)【発明の名称】　光透過型薄膜太陽電池モジュール

(57)【要約】
【課題】　光劣化が低減されて高い出力が得られる光透過型薄膜太陽電池モジュールを提供すること。
【解決手段】　光透過型薄膜太陽電池モジュールは、透光性基板上に透明な表面電極層、光電変換層及び裏面電極層を順に積層して太陽電池セルを形成し、表面電極層から光電変換層を通って裏面電極層を透過する透光部を設け、裏面電極層を透光性の封止材で覆い、封止材が１５００～２０００ｎｍの近赤外波長領域で４０％以上の光吸収率を有し、それによって光電変換効率の劣化を防止する。



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【特許請求の範囲】

【請求項１】　透光性基板上に透明な表面電極層、光電変換層及び裏面電極層を順に積層して太陽電池セルを形成し、表面電極層から光電変換層を通って裏面電極層を透過する透光部を設け、裏面電極層を透光性の封止材で覆い、封止材が１５００～２０００ｎｍの近赤外波長領域で４０％以上の光吸収率を有することを特徴とする光透過型薄膜太陽電池モジュール。

【請求項２】　封止材が、４００～８００ｎｍの可視光領域で７０％以上の光透過率を有する青板ガラスであることを特徴とする請求項１に記載の光透過型薄膜太陽電池モジュール。

【請求項３】　封止材は、酸化亜鉛膜、または酸化亜鉛膜と銀膜との積層膜が表面に形成されたガラス板であって４００～８００ｎｍの可視光領域で７０％以上の透過率を有することを特徴とする請求項１に記載の光透過型薄膜太陽電池モジュール。

【請求項４】　透光性基板上に透明な表面電極層、光電変換層及び裏面電極層を順に積層して太陽電池セルを形成し、表面電極層から光電変換層を通って裏面電極層を透過する透光部を設け、裏面電極層を透光性の封止材で覆い、封止材が気体を体積比で１％～５０％含んだガラスであることを特徴とする光透過型薄膜太陽電池モジュール。

【請求項５】　透光性基板上に透明な表面電極層、光電変換層及び裏面電極層を順に積層して太陽電池セルを形成し、表面電極層から光電変換層を通って裏面電極層を透過する透光部を設け、裏面電極層を透光性の封止材で覆い、さらに、透光性基板上または封止材上を透光性の断熱部材で覆うことを特徴とする光透過型薄膜太陽電池モジュール。

【請求項６】　断熱部材が、シート状のシリカエアロゲルであることを特徴とする請求項５に記載の光透過型薄膜太陽電池モジュール。

【請求項７】　透光性基板が、１５００～２０００ｎｍの近赤外波長領域で４０％以上の光吸収率を有することを特徴とする請求項１～６のいずれか１つに記載の光透過型薄膜太陽電池モジュール。

【請求項８】　透光性基板が、４００～８００ｎｍの波長領域で７０％以上の透過率を有する、透明導電膜付き青板ガラス基板であることを特徴とする請求項７に記載の光透過型薄膜太陽電池モジュール。

【請求項９】　光透過型薄膜太陽電池モジュールの周縁部を囲うフレームをさらに備え、このフレームの透光性基板側の熱放射率は封止材側の熱放射率よりも高いことを特徴とする請求項１～６のいずれか１つに記載の光透過型薄膜太陽電池モジュール。

【請求項１０】　フレームは、その透光性基板側が黒色または暗色で封止材側が銀色または白色であることを特徴とする請求項９に記載の光透過型薄膜太陽電池モジュール。

【請求項１１】　フレームは、その透光性基板側が黒色または暗色で封止材側に断熱部材を有することを特徴とする請求項９に記載の光透過型薄膜太陽電池モジュール。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】この発明は、光透過型薄膜太陽電池モジュールに関し、詳しくは、発電機能に加えて入射光の一部を裏面側へ透過させる採光機能も有する光透過型薄膜太陽電池モジュールに関する。

【０００２】

【従来の技術及び発明が解決しようとする課題】薄膜太陽電池モジュールは結晶ウエハーを用いる太陽電池モジュールよりも半導体材料の使用量が少なくて済み、ガラスや金属等の安価な基板上に低温プロセスで形成できるため、低価格化が期待されている。薄膜太陽電池モジュールの中でも非晶質シリコン系太陽電池モジュールは、材料であるシリコンが非常に豊富に存在する点や、ＣｄやＳｅを使用する化合物系太陽電池モジュールに比べて材料が無害で環境への影響がない点で優れているのでさかんに開発がすすめられている。またその中で、発電機能に加えて入射光の一部を裏面側へ透過させる採光機能も有する光透過型薄膜太陽電池モジュールの開発もすすめられている。

【０００３】一般に、非晶質シリコン系太陽電池モジュールの構造は大きく分けて２種類ある。１つはガラス等の透光性絶縁基板上にSnO_2、ＩＴＯ、ＺｎＯ等の透明導電膜が形成され、その上に非晶質半導体のｐ層、ｉ層、ｎ層が順に積層されて光電変換層が形成され、さらにその上にＩＴＯ、ＺｎＯ等の透明導電膜と、Ａｇ、Ａｌ等の金属膜が順に積層されて裏面電極が形成される構造である。もう１つは、金属基板上にＩＴＯ、ＺｎＯ等の透明導電膜が形成され、その上に非晶質シリコン系半導体のｎ層、ｉ層、ｐ層が順に積層されて光電変換層が形成され、さらにその上にSnO_2、ＩＴＯ、ＺｎＯ等の透明導電膜が形成される構造である。

【０００４】これらのうち、ガラス等の透光性絶縁基板を用いる非晶質シリコン系太陽電池モジュールにおいて、入射光の一部を透過させる透光部を形成するためには一般的に２つの方法が用いられている。１つは、光電変換層上に部分的に裏面電極を形成し、この裏面電極をマスクとして裏面電極から露出した光電変換層をエッチング除去するウェットプロセスである。もう１つは、レーザースクライブ法により光電変換層及び裏面電極を部分的に同時除去するドライプロセスである。

【０００５】このようにいずれかのプロセスで透光部が形成された後、裏面電極側はエチレンビニルアセテート（以下、この明細書において「ＥＶＡ」という）やポリビニルブチラール（以下、この明細書において「ＰＶ

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Ｂ」という）等の接着剤で板ガラスが貼り付けられて封止される。裏面電極側を封止する部材としては、板ガラス以外にも透明ＰＥＴシートやテドラー等の透明なバックシートなどがある。このようにして作製された光透過型薄膜太陽電池モジュールは、その周縁部にアルミニウムやステンレス等のフレームが取り付けられて屋外で設置使用される。

【０００６】一般に、光透過型薄膜太陽電池モジュール（以下、この明細書において単に「光透過型モジュール」ともいう）は発電領域の約１～５０％程度を透光部とするので、非透過型薄膜太陽電池モジュール（以下、この明細書において単に「非透過型モジュール」ともいう）よりも単位面積当たりの発電効率が低くなる。従って、ある所定の発電量をまかなうためには非透過型モジュールよりもモジュール枚数を増やして設置面積を大きくとらなければならない。以上のような事情により、光透過型モジュールの発電効率は特に高いことが望まれる。なお、この明細書においてモジュールとは、基板上に形成された複数の太陽電池セルが互いに電気的に接続されたものを示している。

【０００７】また一方で、一般的な非晶質シリコン系太陽電池モジュールにはステブラー・ロンスキー効果と呼ばれる光照射による変換効率の初期劣化現象（以下、この明細書において「光劣化」という）がある。光劣化は、屋外の太陽光で発電する太陽電池モジュールの光電変換層に非晶質シリコン系半導体を用いる場合の課題となっている。

【０００８】このような非晶質シリコン系太陽電池モジュールの光劣化を完全になくす方法は未だ発見されていない。しかし、単位セルを２層、３層と積層したタンデム、トリプル構造の積層型太陽電池モジュールにおいて、その非晶質シリコン系半導体層の膜厚を薄くすることにより光劣化を低減する方法が知られている。また、光劣化によって低下した変換効率は、非晶質シリコン系太陽電池モジュールを高温にすることによって回復することが知られている。回復効果は約４０℃程度の温度でも見られるが、温度の高いほうが効果が大きく、例えば約７０℃以上の高温にすると大幅に特性が回復することが知られている。

【０００９】一方、非晶質シリコン系太陽電池モジュールの出力の温度依存性は、結晶系シリコン太陽電池モジュールに比べると非常に少なく、約１℃の温度上昇による出力低下は約０．１～０．２％である。このため、非晶質シリコン系太陽電池モジュールを高温に保ちながら使用すると、温度上昇による出力低下よりも光劣化が回復することによる変換効率の向上の方が効果として大きい。

【００１０】すなわち、非晶質シリコン系太陽電池モジュールを高温に保って光劣化を回復させながら使用すると光劣化が低減されて高い出力を得ることができる。このような非晶質シリコン系太陽電池モジュールの温度特性を生かして光劣化を低減する具体的な方法として、非晶質シリコン系太陽電池モジュールの裏面側に断熱部材を設け、太陽光による熱が裏面側から放熱されるのを抑制する方法が一般に知られている（例えば、特開平４－７１２７６号公報参照）。

【００１１】しかしながら、このような従来技術には以下の課題があった。すなわち、非晶質シリコン系太陽電池モジュール（以下、この明細書において単に「太陽電池モジュール」ともいう）の裏面に断熱部材を設けることにより、太陽電池モジュールの最高到達温度は夏期の日中で約７０℃程度まで上昇したが、他の季節では太陽電池モジュールの温度が約７０℃を越えることはなかった。

【００１２】また、上記のような断熱部材を有する太陽電池モジュールにおいて、太陽電池モジュールの強度を高めるためにその周縁部にフレームを設けると、太陽電池モジュールからフレームへの熱の伝導が大きくなってしまうことが知られている。つまり、太陽電池モジュールの特に周辺部の熱がフレームに伝導し、フレームから大気中へ放熱されてしまうのである。このため、フレームの近傍となる太陽電池モジュール周辺部の温度は、太陽電池モジュール中央部の温度よりも約２０度程度低くなることが多かった。

【００１３】このような太陽電池モジュール周辺部の温度低下に対する対策として従来の太陽電池モジュールとフレームとの間に断熱部材を設ける方法を用いたところ、太陽電池モジュール周辺部の温度低下は抑制された。しかし、この方法では、太陽電池モジュールとフレームとの間に断熱部材を挟み込むことにより太陽電池モジュールの取付強度が低下し、太陽電池モジュールの機械的強度が低下するという問題があった。

【００１４】また、太陽電池モジュールの周辺部では光電変換層に水分が侵入しないように封止を行う必要がある。しかし、太陽電池モジュールとフレームとの間に挟み込む断熱部材の耐候性能が十分でない場合、断熱部材の劣化等で封止性能が大きく低下して光電変換層に水分が侵入して侵食されてしまい、太陽電池モジュールの出力が低下するという問題もあった。

【００１５】特に、熱伝導の少ない発泡樹脂等を断熱部材として使用した場合に取付強度の低下や封止性能の低下が大きかった。なお、太陽電池モジュール裏面や太陽電池モジュールとフレームとの間に断熱部材を設ける上述の従来技術は、いずれも光透過型モジュールを前提としていないので、当然ながら断熱部材も透明でないものを使用するのが一般的であった。

【００１６】この発明は以上のような事情を考慮してなされたものであり、光劣化が抑制されて高い出力が得られる光透過型薄膜太陽電池モジュールを提供するものである。

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【００１７】
【課題を解決するための手段】この発明は、透光性基板上に透明な表面電極層、光電変換層及び裏面電極層を順に積層して太陽電池セルを形成し、表面電極層から光電変換層を通って裏面電極層を透過する透光部を設け、裏面電極層を透光性の封止材で覆い、封止材が約１５００～２０００ｎｍの近赤外波長領域で約４０％以上の光吸収率を有し、それによって光電変換効率の劣化を防止することを特徴とする光透過型薄膜太陽電池モジュールを提供するものである。
【００１８】またこの発明は、透光性基板上に透明な表面電極層、光電変換層及び裏面電極層を順に積層して太陽電池セルを形成し、表面電極層から光電変換層を通って裏面電極層を透過する透光部を設け、裏面電極層を透光性の封止材で覆い、封止材が気体を体積比で約１％～５０％含んだガラスであり、それによって光電変換効率の劣化を防止することを特徴とする光透過型薄膜太陽電池モジュールを提供するものでもある。
【００１９】またこの発明は、透光性基板上に透明な表面電極層、光電変換層及び裏面電極層を順に積層して太陽電池セルを形成し、表面電極層から光電変換層を通って裏面電極層を透過する透光部を設け、裏面電極層を透光性の封止材で覆い、さらに、透光性基板上または封止材上を透光性の断熱部材で覆い、それによって光電変換効率の劣化を防止することを特徴とする光透過型薄膜太陽電池モジュールを提供するものでもある。
【００２０】
【発明の実施の形態】この発明による光透過型薄膜太陽電池モジュールは、その一つの形態として、透光部より裏面にぬける太陽光のうち約１５００～２０００ｎｍの波長を有する近赤外波長領域を選択的に吸収できる透光性の封止材を用いる。これにより、採光機能を低下させることなく光透過型薄膜太陽電池モジュールの温度を上昇させてアニール効果を促進し、光劣化を低減できる。
【００２１】このような目的を達成できる封止材としては、例えば、約４００～８００ｎｍの可視光領域で約７０％以上の光透過率を有する青板ガラスなどを挙げることができる。
【００２２】また、封止材としては、酸化亜鉛膜、または酸化亜鉛膜と銀膜との積層膜が表面に形成されたガラス板であって約４００～８００ｎｍの可視光領域で約７０％以上の透過率を有するものを用いることもできる。このようなガラス板は熱線吸収ガラスとして機能するので、この発明の光透過型薄膜太陽電池モジュールに用いる封止材として好適である。また、酸化亜鉛と銀は太陽電池素子の裏面電極層として用いている材料であるため、新たに設備投資をすること無く簡易に作製できるので好都合である。
【００２３】またこの発明による光透過型薄膜太陽電池モジュールは、その一つの形態として、気体を体積比で約１～５０％含んだガラスを透光性の封止材として用いる。つまり、ガラスが例えば空気などの気体を含むと熱伝導率が低くなるので断熱効果を期待できるようになる。従って、光透過型薄膜太陽電池モジュールに吸収された熱が裏面側からすぐに放熱されるのを防止して光透過型薄膜太陽電池モジュールを高温に維持し、アニール効果を促進して光劣化を低減できる。もちろん、採光機能が低下することもない。
【００２４】なお、気体を体積比で約１～５０％含んだガラスとしたのは、気体の体積比が約１％以下では断熱効果が少なく、体積比が約５０％以上では封止材として強度が弱くなるからである。
【００２５】またこの発明による光透過型薄膜太陽電池モジュールは、その一つの形態として透光性基板上または封止材上を透光性の断熱部材で覆う。
【００２６】つまり、光透過型モジュールに断熱部材が密着した構造とすることにより、光透過型モジュールに吸収された熱がすぐに放熱されるのを防止して光透過型モジュールを高温に維持し、アニール効果を促進して光劣化を低減できる。また、断熱部材は透光性のものを用いるので採光機能を低下させることもない。
【００２７】断熱部材としては、熱伝導率が小さく可視光線透過率が高いものほど望ましく、例えば、透明樹脂に属するメタクリル樹脂、ポリカーボネート樹脂、ポリスチレン樹脂、メタロセン触媒で重合されたポリオレフィン類、ポリエステル樹脂、透明フッ素樹脂、ポリイミド樹脂などを用いることができ、なかでも、熱伝導率が約０．０２ｋｃａｌ／ｍｈ℃で、可視光線透過率が約９０％以上の性質をもつシリカエアロゲルを用いれば断熱効果と採光機能を最大限に発揮できる。なお、断熱部材は高温になるため、耐熱性、光照射状態での耐候性に優れることが望ましく、更には焼却時にダイオキシン等の公害物質を発生しないことが望ましい。
【００２８】断熱部材を透光性基板上または封止材上に設ける際には接着剤を使用するが、具体的な接着剤としては例えば、透明シリコン樹脂からなるものやＥＶＡからなるものなどを挙げることができる。
【００２９】また、この発明の光透過型薄膜太陽電池モジュールは、透光性基板が約１５００～２０００ｎｍの近赤外波長領域で平均約４０％以上の光吸収率を有するものを用いることができる。このような透光性基板としては、例えば、約４００～８００ｎｍの非晶質シリコン系半導体感度波長領域で平均約７０％以上の透過率を有する、透明導電膜付き青板ガラス基板などを挙げることができる。
【００３０】また、この発明の光透過型薄膜太陽電池モジュールは、その周縁部を囲うフレームをさらに備えてもよい。この場合、フレームの透光性基板側の熱放射率は封止材側の熱放射率よりも高いことが好ましい。というのは、このようなフレームを用いるとフレームの透光

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性基板側、つまりフレームの受光面では太陽光の吸収が増大し、一方、フレームの封止材側、つまり非受光面では熱の放射が低減してフレームの温度が上昇するからである。

【００３１】これにより、光透過型モジュール周辺部からフレームへ伝導する熱は減少するかまたは無くなり光透過型モジュール周辺部の温度が上昇するので、アニール効果がより一層促進されて光劣化が低減する。また、フレームからの熱放射の低減によりフレーム自体が高温となるので、従来のようにモジュールとフレームとの間に断熱部材を設ける必要が無くなり、光透過型モジュールとフレームとを強固に固定できるようになる。

【００３２】このようなフレームとしては、例えば、その透光性基板側が黒色または暗色で封止材側が銀色または白色のフレームを挙げることができる。つまり、フレームの透光性基板側を黒色または非晶質シリコン系半導体層と同系の暗色とすればフレームの受光面における太陽光の吸収が増大し、一方、フレームの封止材側を白色または銀色とすればフレームの非受光面における熱の放射が低減される。これにより、フレームの温度が上昇する。

【００３３】また、透光性基板側が黒色または暗色で封止材側に断熱部材が設けられてもよい。つまり、フレームの封止材側を白色または銀色とするかわりに断熱部材を用いることもできる。なお、このようなフレームを非透過型モジュールに使用しても同様の効果を発揮することは明らかである。

【００３４】

【実施例】以下に図面に示す実施例に基づいてこの発明を詳述する。なお、この実施例によってこの発明が限定されるものではない。

【００３５】実施例１

この発明の実施例１に係る光透過型薄膜太陽電池モジュールについて図１～図３に基づいて説明する。図１はこの発明の実施例１に係る光透過型薄膜太陽電池モジュールの部分拡大断面図である。光透過型薄膜太陽電池モジュール１は、ガラス基板２上に透明な表面電極層３、光電変換層４、透明導電膜５と金属膜６とから構成される裏面電極層７を順に積層して太陽電池セル８を形成し、表面電極層３から光電変換層４を通って裏面電極層７を透過する透光部９を設け、裏面電極層７を透光性の封止材１０で覆い、封止材１０が約１５００～２０００ｎｍの近赤外波長領域で約４０％以上の光吸収率を有し、それによって光電変換効率の劣化を防止することを特徴としている。

【００３６】以下に光透過型太陽電池モジュール１の作製方法を示す。SnO_2からなる透明な表面電極層３が成膜されたガラス基板２にＹＡＧ基本波レーザーを用いて表面電極層３のパターニングを行った。

【００３７】詳しくは、レーザー光をガラス基板２側から入射させることにより、表面電極層３を短冊状に分離して表面電極層分離ライン１１を形成した。この後、ガラス基板２を純水で洗浄して光電変換層４をプラズマＣＶＤ装置により形成した。光電変換層はｐ層、ｉ層、ｎ層のアモルファスシリコンからなり、各層の膜厚の合計は約１００～６００ｎｍ程度である。

【００３８】次にＹＡＧ　ＳＨＧレーザーにより光電変換層４のパターニングを行った。詳しくは、レーザー光をガラス基板２側から入射させることにより、光電変換層４を短冊状に分離して光電変換層分離ライン１２を形成した。

【００３９】この後、透明導電膜５と金属膜６からなる裏面電極層７をスパッタリング装置により形成した。詳しくは、透明導電膜５としてＺｎＯを膜厚約１００ｎｍで成膜した後、金属膜６としてＡｇを膜厚約５００ｎｍで成膜した。

【００４０】次に、顔料により任意の色に着色された着色レジスト膜１３を裏面電極層７上に膜厚約１～１０μｍでスプレー方式で塗布し、乾燥炉で乾燥させた。次に、ＹＡＧ　ＳＨＧレーザーにより裏面電極層７のパターニングを行った。詳しくは、レーザ光をガラス基板側から入射させることにより、裏面電極層７を短冊状に分離して裏面電極層分離ライン１４を形成した。

【００４１】その後、ＹＡＧ　ＳＨＧレーザーにより発電領域内に透光部９を形成するためのパターニングを行った。詳しくは、透光部９を不連続のライン形状とするためにマスクを用いてレーザー光をガラス面から入射させることにより、透光部９を形成した。この時に透光部９の本数や長さを変えることにより透光率を自由に設定できるが、実施例１では全発電領域の約１０％を透光部とした。透光部９の形成後、酸系及び硫化鉄系のエッチング液により、裏面電極層７の残りかすを除去した。

【００４２】その後、裏面電極層７上にＥＶＡのシート状接着剤１５を用いて、ラミネート及びキュア工程を経てガラス基板２と同サイズの青板ガラスを封止材１０として貼り付け、ガラス基板２との合わせガラス構造とした。青板ガラスは厚さ約４ｍｍのものを用いた。この青板ガラスは可視光線透過率が高く、また、近赤外線領域で約４０％以上の光吸収率を有する低コスト材料である。

【００４３】端子（図示せず）は＋極と－極を封止材１０に設けた穴（図示せず）からそれぞれ取り、封止材１０に接着した端子ボックス（図示せず）を経由して電力を取り出せるようにした。

【００４４】その後、図２及び図３に示すように、光透過型薄膜太陽電池モジュール１の周囲にブチルゴム（図示せず）を介してアルミニウム製のフレーム１６を取り付けて完成させた。なお、図２はフレーム１６が取り付けられた光透過型薄膜太陽電池モジュール１の平面図であり、図３は図２の簡略的なＡ－Ａ断面図である。図２

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および図３共に光透過型薄膜太陽電池モジュール１の細部構造、ブチルゴム、端子及び端子ボックスは省略してある。

【００４５】比較例

次に、この発明による光透過型薄膜太陽電池モジュールとの比較のために作製した非透過型薄膜太陽電池モジュールについて図９に基づいて簡単に説明する。図９に示すように、比較例として作製した非透過型薄膜太陽電池モジュール２０１は、実施例１のように透光部９を設けず、また、封止材１０の代わりにシート状のガラス繊維からなる断熱部材２１０をＥＶＡからなる接着剤１５で貼り付けたものである。断熱部材２１０はガラス基板２と同じ寸法を有し、その厚さは約２ｍｍである。その他の構成は実施例１と同じである。以上のような非透過型薄膜太陽電池モジュール２０１を、実施例１で用いたのと同じフレーム１６にブチルゴムを介して取り付け、比較例とした。

【００４６】実施例１に係る光透過型薄膜太陽電池１と比較例に係る非透過型薄膜太陽電池２０１とを屋外に設置し、その温度と光電変換効率の変化を調べた。比較例では、モジュールの温度が夏期において最高でもモジュール中央部で気温より約４０度の温度上昇、フレーム近傍のモジュール周辺部で約２５度の温度上昇に止まった。実施例１のモジュールでは気温に対してモジュール全面平均で約３０～４５度の温度上昇となり、夏期において約６０～７５℃となった。この結果、比較例では年平均で約２４％の光劣化が生じていたが、実施例１では光劣化が年平均で約２２％となり、改善効果が確認された。

【００４７】実施例２

この発明の実施例２に係る光透過型薄膜太陽電池モジュールについて図４に基づいて説明する。図４は実施例２に係る光透過型薄膜太陽電池モジュールの部分拡大断面図である。

【００４８】図４に示すように、実施例２に係る光透過型薄膜太陽電池モジュール２１は、封止材３０としてガラス板３０ａに酸化亜鉛膜３０ｂを膜厚約１μｍで成膜したものを使用した。それ以外の構成および各部材の形成方法は実施例１に係る光透過型薄膜太陽電池モジュール１と同じなので、それらの説明は省略する。

【００４９】実施例２に係る光透過型薄膜太陽電池２１と比較例に係る非透過型薄膜太陽電池２０１とを屋外に設置し、その温度と光電変換効率の変化を調べた。比較例では、モジュールの温度が夏期において最高でもモジュール中央部で気温より約４０度の温度上昇、フレーム近傍のモジュール周辺部で約２５度の温度上昇に止まった。実施例２のモジュールでは気温に対してモジュール全面平均で約３５～５０度の温度上昇となり、夏期において約６５～８０℃となった。この結果、比較例では年平均で約２４％の光劣化が生じていたが、実施例２では光劣化が年平均で約２１％となり、改善効果が確認された。

【００５０】なお、実施例２では封止材３０としてガラス板３０ａに酸化亜鉛膜３０ｂを膜厚約１μｍで成膜したものを用いたが、熱線吸収膜として最適化された酸化亜鉛膜と銀膜との積層膜を用いるとさらに良い。

【００５１】実施例３

この発明の実施例３に係る光透過型薄膜太陽電池モジュールについて図５に基づいて説明する。図５は実施例３に係る光透過型薄膜太陽電池モジュールの部分拡大断面図である。図５に示すように、実施例３に係る光透過型薄膜太陽電池モジュール４１は、封止材５０として空気を体積比で約１０％含んだガラス板を用いた。それ以外の構成および各部材の形成方法は実施例１に係る光透過型薄膜太陽電池モジュール１と同じなので、それらの説明は省略する。

【００５２】実施例３に係る光透過型薄膜太陽電池４１と比較例に係る非透過型薄膜太陽電池２０１とを屋外に設置し、その温度と光電変換効率の変化を調べた。比較例では、モジュールの温度が夏期において最高でもモジュール中央部で気温より約４０度の温度上昇、フレーム近傍のモジュール周辺部で約２５度の温度上昇に止まった。実施例３のモジュールでは気温に対してモジュール全面平均で約３５～５０度の温度上昇となり、夏期において約６５～８０℃となった。この結果、比較例では年平均で約２４％の光劣化が生じていたが、実施例３では光劣化が年平均で約２１％となり、改善効果が確認された。

【００５３】実施例４

この発明の実施例４に係る光透過型薄膜太陽電池モジュールについて図６に基づいて説明する。図６は実施例４に係る光透過型薄膜太陽電池モジュールの断面を簡略的に説明する断面図であり、実施例１の図３に相当する図である。なお、実施例１～３と同じ名称および構成の部材は同じ符号を用いて説明する。

【００５４】図６に示すように、実施例４に係る光透過型薄膜太陽電池モジュール６１は、実施例１に係る光透過型薄膜太陽電池モジュール１（図１、図３参照）の封止材１０上に透明な断熱部材１６を透明なシリコーン樹脂からなる接着剤を用いて貼り付けたものである。

【００５５】断熱部材１６は、熱伝導率が約０．０２ｋｃａｌ／ｍｈ℃で、可視光線透過率が約９０％のシリカエアロゲルからなるもので、その厚さは約１０ｍｍである。また、断熱部材の接着方法は、上記透明シリコーン樹脂を用いた接着に限らず、ＥＶＡを接着剤としたラミネート法、もしくはモジュールに直接塗布して硬化させる方法でも良い。それ以外の構成および各部材の形成方法は実施例１に係る光透過型薄膜太陽電池モジュール１と同じなので、それらの説明は省略する。

【００５６】実施例４に係る光透過型薄膜太陽電池６１

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と比較例に係る非透過型薄膜太陽電池２０１とを屋外に設置し、その温度と光電変換効率の変化を調べた。比較例では、モジュールの温度が夏期において最高でもモジュール中央部で気温より約４０度の温度上昇、フレーム近傍のモジュール周辺部で約２５度の温度上昇に止まった。実施例４のモジュールでは気温に対してモジュール全面平均で約４２～５５度の温度上昇となり、夏期において約７２～８５℃となった。この結果、比較例では年平均で約２４％の光劣化が生じていたが、実施例４では光劣化が年平均で約２０％となり、改善効果が確認された。

【００５７】実施例５

この発明の実施例５に係る光透過型薄膜太陽電池モジュールについて図７に基づいて説明する。図６は実施例４に係る光透過型薄膜太陽電池モジュールの断面を簡略的に説明する断面図であり、実施例１の図３に相当する図である。なお、実施例１～４と同じ名称及び構成の部材は同じ符号を用いて説明する。

【００５８】図７に示すように、実施例５に係る光透過型薄膜太陽電池モジュール８１は、実施例１に係る光透過型薄膜太陽電池モジュール１（図１、図３参照）のガラス基板２と表面電極層３を、熱ＣＶＤ法によって酸化錫透明導電膜が蒸着された青板ガラス８２としたものである。そして、上述の実施例４と同様に封止材１０上に透明な断熱部材１６を透明なシリコーン樹脂からなる接着剤を用いて貼り付けたものである。それ以外の構成および各部材の形成方法は実施例１に係る光透過型薄膜太陽電池モジュールと同じなので、それらの説明は省略する。

【００５９】実施例５に係る光透過型薄膜太陽電池８１と比較例に係る非透過型薄膜太陽電池２０１とを屋外に設置し、その温度と光電変換効率の変化を調べた。比較例では、モジュールの温度が夏期において最高でもモジュール中央部で気温より約４０度の温度上昇、フレーム近傍のモジュール周辺部で約２５度の温度上昇に止まった。実施例５のモジュールでは気温に対してモジュール全面平均で約５０～６０度の温度上昇となり、夏期において約８０～９０℃となった。この結果、比較例では年平均で約２４％の光劣化が生じていたが、実施例５では光劣化が年平均で約１８％となり、大きな改善効果が確認された。

【００６０】実施例６

この発明の実施例６に係る光透過型薄膜太陽電池モジュールについて図８に基づいて説明する。図８は実施例６に係る光透過型薄膜太陽電池モジュールの断面を簡略的に説明する断面図であり、実施例１の図３に相当する図である。なお、実施例１～５と同じ名称及び構成の部材は同じ符号を用いて説明する。

【００６１】図８に示すように、実施例６に係る光透過型薄膜太陽電池モジュール１０１は、実施例１に係る光透過型薄膜太陽電池モジュール１（図３参照）のフレーム１５を、太陽光が直接照射される面（受光面）が黒色でそれ以外の部分（非受光面）が銀色のフレーム１１５としたものである。図８において、フレーム１１５の黒色とされた部分は、ガラス基板２と平行となる表面１１５ａと、表面１１５ａからほぼ垂直に折れ曲がった側面１１５ｂである。そして、上述の実施例４と同様に封止材１０上に透明な断熱部材１６が透明なシリコーン樹脂からなる接着剤を用いて貼り付けられている。

【００６２】実施例６に係る光透過型薄膜太陽電池１０１と比較例に係る非透過型薄膜太陽電池２０１とを屋外に設置し、その温度と光電変換効率の変化を調べた。比較例では、モジュールの温度が夏期において最高でもモジュール中央部で気温より約４０度の温度上昇、フレーム近傍のモジュール周辺部で約２５度の温度上昇に止まった。実施例６のモジュールでは気温に対してモジュール全面平均で約４５～５５度の温度上昇となり、夏期において約７５～８５℃となった。この結果、比較例では年平均で約２４％の光劣化が生じていたが、実施例６では光劣化が年平均で約１９％となり、大きな改善効果が確認された。

【００６３】実施例のまとめとして、比較例と実施例１～６の気温からの上昇温度と光劣化率をそれぞれ表１に示す。なお表１中の気温からの上昇温度は、比較例ではモジュール中央部で測定した温度であり、実施例１～６ではモジュール全面の平均温度である。

【００６４】

【表１】

	従来	実施例１	実施例２	実施例３	実施例４	実施例５	実施例６
気温からの上昇温度（deg）	25～40	30～45	35～50	30～50	42～55	50～60	45～55
光劣化率（%）	24	22	21	21	20	18	19

【００６５】

【発明の効果】この発明によれば、光透過型薄膜太陽電池モジュールの透光性の封止材が約１５００～２０００ｎｍの近赤外波長領域で約４０％以上の光吸収率を有するので、光透過型薄膜太陽電池モジュールの光劣化を低減して高い出力を得ることができる。

【図面の簡単な説明】

【図１】この発明の実施例１に係る光透過型薄膜太陽電池モジュールの部分拡大断面図である。

【図２】この発明の実施例１に係る光透過型薄膜太陽電池モジュールにフレームを取り付けた状態を示す平面図である。

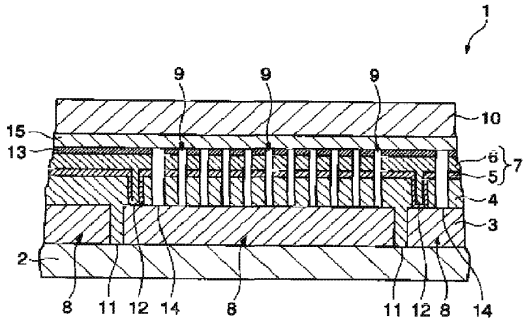
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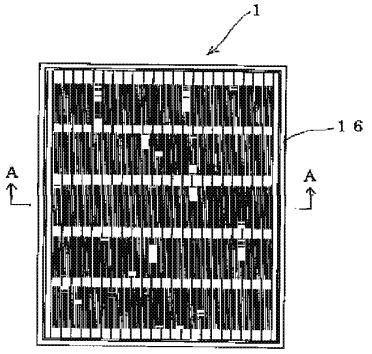
【図３】図２のＡ－Ａ断面を簡略的に示した断面図である。
【図４】この発明の実施例２に係る光透過型薄膜太陽電池モジュールの部分拡大断面図である。
【図５】この発明の実施例３に係る光透過型薄膜太陽電池モジュールの部分拡大断面図である。
【図６】この発明の実施例４に係る光透過型薄膜太陽電池モジュールの断面を簡略的に示した断面図である。
【図７】この発明の実施例５に係る光透過型薄膜太陽電池モジュールの断面を簡略的に示した断面図である。
【図８】この発明の実施例６に係る光透過型薄膜太陽電池モジュールの断面を簡略的に示した断面図である。
【図９】比較例として作製した非透過型薄膜太陽電池モジュールの部分拡大断面図である。
【符号の説明】

１・・・光透過型薄膜太陽電池モジュール
２・・・ガラス基板
３・・・表面電極層
４・・・光電変換層
５・・・透明導電膜
６・・・金属膜
７・・・裏面電極層
８・・・太陽電池セル
９・・・透光部
１０・・・封止材
１１・・・表面電極層分離ライン
１２・・・光電変換層分離ライン
１３・・・着色レジスト膜
１４・・・裏面電極層分離ライン
１５・・・接着剤

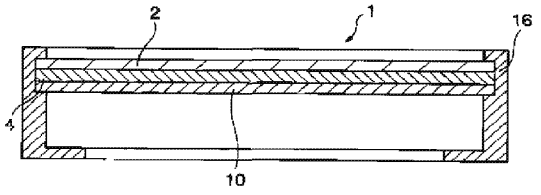
【図１】



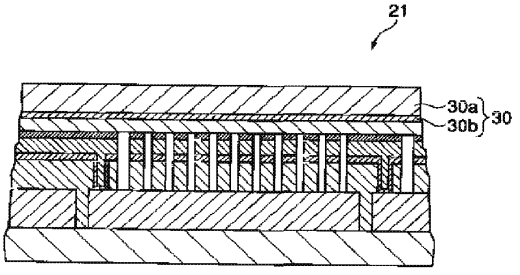
【図２】



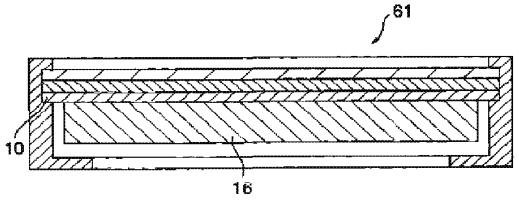
【図３】



【図４】

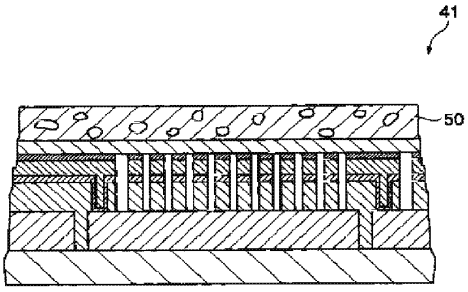


【図６】

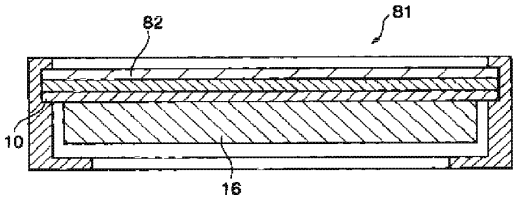


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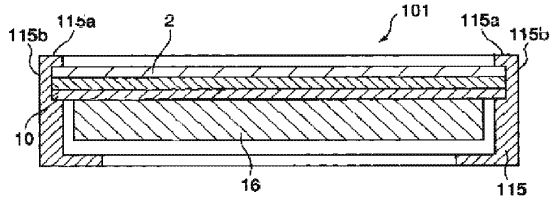
【図５】



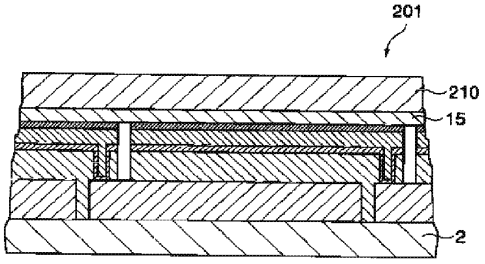
【図７】



【図８】



【図９】



Espacenet

Bibliographic data: JP2002134640 (A) — 2002-05-10

THIN PHOTOSENSITIVE SEMICONDUCTOR DEVICE

Inventor(s): BAI JINCHUAN + (BAI JINCHUAN)

Applicant(s): UNITED TEST CT INC + (UNITED TEST CENTER INC)

Classification: - international: ***H01L23/02; H01L23/04; H01L23/12; H01L23/28; H01L31/02; H01L31/0203; H01L31/024;***
(IPC1-7): H01L23/02; H01L23/04; H01L23/12; H01L23/28; H01L31/02
- cooperative: **H01L31/0203**; **H01L31/024**; H01L2224/45144; H01L2224/48091; H01L2224/48227; H01L2224/73265 more

Application number: JP20010027456 20010202

Priority number (s): TW20000121163 20001011

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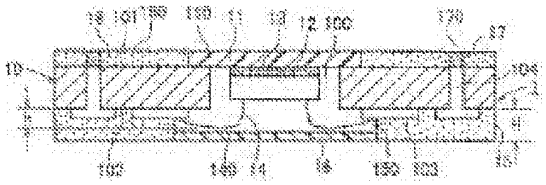
Abstract of JP2002134640 (A)

PROBLEM TO BE SOLVED: To provide a thin photosensitive semiconductor device that can satisfy requirements of making thinner, by effectively reducing the height of a semiconductor device. SOLUTION: This device comprises a first surface 101, a second surface 102 of the opposite side of the first surface 101, a substrate 10 having a connecting electrode 103 at the second surface 102, a contact hole 104 that penetrates the substrate 10 and connects to the connecting electrode 103 electrically, a large diameter cavity 100 for storing a semiconductor element 12, a cover sheet 11 by which the large diameter cavity 100 is covered and to which the semiconductor element 12 is adhered, a first resin covering layer 15 that is formed on the second surface 102 to cover the connecting electrode 103, a seal member for isolating the semiconductor element 12 and a first conductive member,; which connect to a first resin covering layer 15 in succession, in an air tightness state from an external, and a second resin covering layer 18 formed on the first surface 101 of the substrate 10.

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FIG. 1



SIONYX1403000036.0089

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特開2002－134640
（P2002－134640A）
(43)公開日　平成14年５月10日(2002.5.10)

(51)Int.Cl.[7]	識別記号	ＦＩ		テーマコード(参考)
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23/02		23/02	Ｆ	５Ｆ０８８
23/12	５０１	23/12	５０１Ｔ	
23/28		23/28	Ｋ	
31/02		31/02	Ｂ	

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(32)優先日　平成12年10月11日(2000.10.11)
(33)優先権主張国　台湾（ＴＷ）

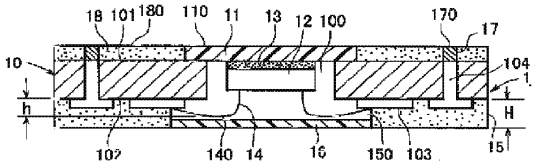
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Ｆターム(参考)　4M109 AA04 BA04 DB16
5F088 BA15 BB03 JA03 JA07 JA10

(54)【発明の名称】　薄型感光式半導体装置

(57)【要約】
【課題】半導体装置の高さを効果的に低減して、薄型化の要求を満足することが可能な薄型感光式半導体装置を提供する。
【解決手段】第１の表面１０１と、第１の表面１０１反対側の面である第２の表面１０２と、第２の表面１０２に接続電極１０３を有する基板１０と、基板１０を貫通して接続電極１０３と電気的に接続される接続孔１０４と、半導体素子１２を収納する大径孔１００と、前記大径孔１００を被すと共に前記半導体素子１２が接着されるカバーシート１１と、前記の第２の表面１０２上に形成して前記接続電極１０３を被覆する第１の樹脂被覆層１５と、前記第１の樹脂被覆層１５に連接して前記半導体素子１２及び第１の導電部材を外部から気密的に隔離するシール部材と、前記基板１０の第１の表面１０１上に形成する第２の樹脂被覆層１８とを含む。

FIG. 1



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【特許請求の範囲】
【請求項１】第１の表面と、前記第１の表面の反対側の面に複数の接続電極を形成した第２の表面とを有する基板に、前記基板を貫通し、且つ前記第２の表面上の複数の接続電極に電気的に接続された複数の接続孔と、前記基板を貫通して形成された大径孔を有し、前記基板の第１の表面側にて、前記基板の大径孔を外側から被すカバーシートと、前記基板の大径孔内に収納されて前記カバーシートに接着された半導体素子と、前記半導体素子と前記接続電極を電気的に接続する複数の第１導電部材と、前記基板の第２の表面上に形成されて前記接続電極を被覆する第１の樹脂被覆層と、前記第１の樹脂被覆層に連続して前記半導体素子及び第１の導電部材を外部から気密的に隔離するシール部材と、前記基板の第１の表面上に配設されて前記接続孔に電気的に接続される第２の導電部材、及び前記基板の第１の表面上に形成される第２の樹脂被覆層を含み、前記カバーシート及び第２導電部材は前記第２の樹脂被覆層より露出されると共に、カバーシートの露出面及び第２導電部材の露出部を前記第２樹脂被覆層の外部表面と同一平面に形成したことを特徴とする薄型感光式半導体装置。
【請求項２】前記カバーシートが樹脂材で作成されたことを特徴とする請求項１に記載の薄型感光式半導体装置。
【請求項３】前記カバーシートが伝熱性の良い金属で作成されたことを特徴とする請求項１に記載の薄型感光式半導体装置。
【請求項４】前記シール部材が透明シート体であって、前記基板の大径孔に対応して、前記第１樹脂被覆層に形成される開孔部をシールすることを特徴とする請求項１に記載の薄型感光式半導体装置。
【請求項５】前記シール部材が透明シート体であって、前記シール部材を前記第１樹脂被覆層全面に接着して、前記第１樹脂被覆層及び前記基板の大径孔に対応して前記第１樹脂被覆層に形成される開孔部をカバーすることを特徴とする請求項１に記載の薄型感光式半導体装置。
【請求項６】前記シール部材が透明樹脂で形成された充填樹脂であって、シール部材を前記基板大径孔内の充填に用い、前記半導体素子及び第１導電部材を完全に被覆することを特徴とする請求項１に記載の薄型感光式半導体装置。
【請求項７】前記第１導電部材が金線であることを特徴とする請求項１に記載の薄型感光式半導体装置。
【請求項８】前記第２導電部材が半田ボール（solder ball）であることを特徴とする請求項１に記載の薄型感光式半導体装置。
【請求項９】前記第２導電部材が接続バンプ（connecting bump）であることを特徴とする請求項１に記載の薄型感光式半導体装置。
【請求項１０】前記バンプは、導電性金属で作成されたことを特徴とする請求項９に記載の薄型感光式半導体装置。
【請求項１１】前記第１樹脂被覆層の厚さを、前記第１導電部材が基板の第２の表面の高さより大きくして、前記第１導電部材が前記第１樹脂被覆層から露出しないようにしたことを特徴とする請求項１に記載の薄型感光式半導体装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、感光型半導体パッケージに関し、特に、外部光線を入射可能にして、封止された半導体素子が外部光線を受光しうるようにした感光型半導体パッケージに関する。
【０００２】
【従来の技術】一般の半導体装置は、その半導体素子（チップとも云う）を外部の空気または湿気による化学変化を防止すると共に、外力の衝撃によって前記半導体素子が破損することを避けるため、通常は前記の半導体素子を不透光モールド樹脂内に封止して保護する。しかし、半導体素子が撮像素子のような画像検出（image sensing）型または紫外線消去可能な（ultraviolet erasable）ＥＰ-ＲＯＭ等である半導体装置は、前記半導体素子が外部からの光線を受光できるようにしなければならない。従って、感光式半導体装置の構造は、外部光線が装置内部に入射して、装置内部の感光型素子が入射光線を検知することが出来るように設計される。
【０００３】従来の感光式半導体装置は業者の必要と設計とによって多種類の形式に構成される。図４に示す半導体装置もその一つである。図４に示す半導体装置３は、基板３０の上面に半導体素子（以下単に素子と略称する）３２をダイボンドすると共に、金線３４を用いて基板３０上の接続電極３１とワイヤボンディングして電気的接続を形成し、素子３２を該基板３０上に固着した状態でケース体３６内に収納する。次いで、透明蓋体３８をケース体３６上に固着して、前記素子３２と、金線３４とを外部から気密に隔離する。但し、外部光線が、前記透明蓋体３８を通ってケース体３６内の前記素子３２を照射可能に構成される。図４において、３７は接続電極３１を半田ボール３９と電気的に接続する接触孔（ビアとも云う）である。
【０００４】上記の従来の構成は、半導体装置３全体の高さが半田ボール３９と、基板３０と、素子３２と金線３４が素子３２の高さを越えた部分と、金線３４と透明蓋体３８との間の距離、及び透明蓋体３８等の高さ（厚さ）等を含むので、薄型化が難しく、製品薄型化の需要を満足することが出来ない。なお、前記基板３０は、その上面に素子３２とケース体３６を固着し、底面部に半田ボール３９を植設するため、温度サイクル及び信頼性試験等の大幅な温度変化があると、材質の熱膨張係数の差異によって、基板３０に熱応力が発生して反り（warp

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age）を発生し、そのため、基板３０と素子３２との間の接着部分に剥離（delamination）が発生する他、複数の半田ボール３９の平面度を失い、前記半田ボール３９がプリント基板等の外部装置との電気的接続のリフロー（reflow）作業において、複数の半田ボール３９が外部装置上の接続点に均一に溶接しえなくなって、品質及び信頼性に著しく影響する。

【０００５】

【発明が解決しようとする課題】この発明の目的は、半導体装置の高さを効果的に低減して、薄型化の要求を満足することが可能な薄型感光式半導体装置を提供することである。

【０００６】本発明の別の目的は、半導体装置の機械強度を増強することによって、基板の反りの発生を有効に防止しうる薄型感光式半導体装置を提供することである。

【０００７】本発明の他の目的は、放熱性が良好な薄型感光式半導体装置を提供することである。

【０００８】本発明のさらに別の目的は、外部装置との電気的接続性が向上された薄型感光式半導体装置を提供することである。

【０００９】本発明のさらに別の目的は、基板厚さの薄型化において製造性に影響せず、且つ、基板コストの低減に寄与しうる薄型感光式半導体装置を提供することである。

【００１０】

【課題を解決するための手段】本発明の薄型感光式半導体装置は、第１の表面と、前記第１の表面の反対側の面に複数の接続電極を形成した第２の表面とを有する基板に、前記基板を貫通し、且つ前記第２の表面上の複数の接続電極に電気的に接続された複数の接続孔と、前記基板を貫通して形成された大径孔を有し、前記基板の第１の表面側にて、前記基板の大径孔を外側から被すカバーシートと、前記基板の大径孔内に収納されて前記カバーシートに接着された半導体素子と、前記半導体素子と前記接続電極を電気的に接続する複数の第１導電部材と、前記基板の第２の表面上に形成されて前記接続電極を被覆する第１の樹脂被覆層と、前記第１の樹脂被覆層に連続して前記半導体素子及び第１の導電部材を外部から気密的に隔離するシール部材と、前記基板の第１の表面上に配設されて前記接続孔に電気的に接続される第２の導電部材、及び前記基板の第１の表面上に形成される第２の樹脂被覆層を含み、前記カバーシート及び第２導電部材は前記第２の樹脂被覆層より露出されると共に、カバーシートの露出面及び第２導電部材の露出部を前記第２樹脂被覆層の外部表面と同一平面に形成したことを特徴とする。

【００１１】また、前記カバーシートが樹脂材で作成されたことを特徴とする。

【００１２】また、前記カバーシートが伝熱性の良い金属で作成されたことを特徴とする。

【００１３】また、前記シール部材が透明シート体であって、前記基板の大径孔に対して、前記第１樹脂被覆層に形成される開孔部をシールすることを特徴とする。

【００１４】また、前記シール部材が透明シート体であって、前記シール部材を前記第１樹脂被覆層全面に接着して、前記第１樹脂被覆層及び前記基板の大径孔に対応して前記第１樹脂被覆層に形成される開孔部をカバーすることを特徴とする。

【００１５】また、前記シール部材が透明樹脂で形成された充填樹脂であって、シール部材を前記基板大径孔内の充填に用い、前記半導体素子及び第１導電部材を完全に被覆することを特徴とする。

【００１６】また、前記第１導電部材が金線であることを特徴とする。

【００１７】また、前記第２導電部材が半田ボール（solder ball）であることを特徴とする。

【００１８】また、前記第２導電部材が接続バンプ（connecting bump）であることを特徴とする。

【００１９】また、前記バンプは、導電性金属で作成されたことを特徴とする。

【００２０】また、前記第１樹脂被覆層の厚さを、前記第１導電部材が基板の第２の表面の高さより大きくして、前記第１導電部材が前記第１樹脂被覆層から露出しないようにしたことを特徴とする。

【００２１】前記カバーシートは、シリカゲル（silica gel）、エポキシ樹脂（epoxy）、ポリイミド（polyimide）または類似材料から成るシート状部材、或いは、放熱性の良い金属銅、アルミニウム、銅合金、アルミ合金等で構成し、更に放熱性を良くするため、伝熱性粘着剤を使用して前記素子をカバーシートに接着する。

【００２２】前記シール部材は、ガラス、プラスチックまたは金属材料等で透明なシート体を形成し、前記基板の大径孔に対応して第１樹脂被覆層上に形成される開孔部を蓋して前記大径孔内の素子及び第１の導電素子の外部との気密隔離を行う。また、前記シール部材を前記基板の大径孔及び第１樹脂被覆層の開孔部に充填する透明樹脂体を形成する。前記の樹脂材は透明である故、前記透明樹脂体に被覆された素子は、効果的に外部からの入射光を検知することが出来る。

【００２３】第１導電部材に金線を用い、第２導電部材は、周知の植球技術により基板の第１の表面上の接続孔端部に半田ボール（solder ball）を形成して、半田ボールと導通孔を電気接続する。なお、銅、錫、その合金またはその他の導電性金属を用いて接続バンプ（Connecting bump）を従来の印刷技術で基板第１の表面上の接続孔端部位置に形成することも可能である。第２導電部材を基板の第１の表面上に形成した後、前記第２導電部材及び前記カバーシートを露出させるように、第２樹脂被覆層を前記基板の第１の表面上に形成する。第２樹脂

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被覆層は、第２導電部材とカバーシートを全面的に被覆した後に、研磨して第２導電部材とカバーシートを露出させても良い。前記第２樹脂被覆層、或いは第２樹脂被覆層と第２導電部材、または第２樹脂体と第２導電部材及びカバーシートの表面をさらに研磨して全体を薄くする。従って、効果的にシール後の完製品全体の高さを低減させ、前記第２樹脂被覆層と前記第２導電部材の露出端部及びカバーシートの露出表面を同一面に形成する。

【００２４】

【発明の実施の形態】実施例１

図１は、本発明に係る実施例１の薄型感光式半導体装置１の断面図である。図１に示すように、本発明の実施例１の半導体装置１は、中央部分に大径孔１００を形成した基板１０を用い、前記基板１０は第１の表面１０１と、前記第１の表面１０１の反対側の第２の表面１０２とを有し、前記第２の表面１０２上に導電性材料がある複数の接続電極１０３を形成し、この接続電極１０３に接続され、前記基板１０を貫通して形成される接続孔１０４を有する。前記接続電極１０３及び接続孔１０４は、従来の半導体装置３のそれと同一であるので、説明を省略する。前記基板１０の第１の表面１０１に完全を被すように、カバーシート１１を接着する。基板１０の大径孔１００に臨むカバーシート１１の表面に半導体素子１２を銀蝋等接着剤１３で接着して、基板１０の大径孔１００内に収納する。

【００２５】以上に説明したように、前記カバーシート１１は、ポリイミド等の樹脂材料で構成するシート、或いは銅等の伝熱性金属で作成された放熱シートで構成される。前記カバーシート１１を放熱性の良い材料で形成すると、半導体素子１２に発生する熱は直接前記カバーシート１１に伝導されて外部へ放出されるので、半導体装置１の放熱効率を向上させる。

【００２６】前記半導体素子１２をカバーシート１１の適当な位置に固着した後、複数の金線１４を用いて、前記半導体素子１２を基板１０に、ＴＡＢ（tab automated bond）技術等の周知の方法で接続する。

【００２７】金線１４の接続作業が完了すると、基板１０の第２の表面１０２の大径孔１００の部分と接続電極１０３に金線１４が接続された箇所を含む部分を開孔部１５０として、この開孔部１５０以外の領域を樹脂材料で被覆して第１の樹脂被覆層１５を形成する。この第１の樹脂被覆層１５は印刷方法などの方法で、その厚さHを、金線１４の円弧頂点１４０、即ち金線１４であるワイヤループの高さｈを十分に超越し（図１においてＨ＞ｈ）、かつ後述する透明シート１６の厚さを含む程度に設定する。

【００２８】上述のように第１の樹脂被覆層１５の厚さＨを抑制することによって、半導体装置１全体の厚さを、図４に示す従来のＢＧＡ型半導体装置の全体の厚さより小さくすることができる。

【００２９】前記第１の樹脂被覆層１５を形成した後、前記開孔部１５０に透明シート１６を嵌着して大径孔１００を含む開孔部１５０を気密に封止する。こうした構成により、外部からの光は透明シート１６を通って半導体装置１内へ入射し、半導体素子１２によってそれを検知することができるようになる。

【００３０】また、前記基板１０の第１の表面１０１上に周知の印刷方法で複数の接続バンプ１７を前記接続孔１０４の第１の表面１０１の端部に形成し、それぞれの接続バンプ１７を前記接続孔１０４に電気的に接続し、この接続バンプ１７を介して前記半導体素子１２を外部装置（図示しない）に電気的に接続しうるようにする。

【００３１】接続バンプ１７を前記基板１０の第１の表面１０１上に布設した後、基板１０の第１の表面１０１をエポキシ樹脂等の封止材にて被覆して第２の樹脂被覆層１８を形成する。この時、第２の樹脂被覆層１８の硬化後に前記接続バンプ１７の表面部１７０及びカバーシート１１の外表面１１０が前記第２の樹脂被覆層１８の外部に露出するようにするか、または、前記接続バンプ１７及びカバーシート１１を完全に被覆した後に、周知の研磨方式で前記第２の樹脂被覆層１８を、前記接続バンプ１７の表面部１７０及びカバーシート１１の外表面１１０が露出する迄薄く研磨し、前記第２の樹脂被覆層１８の頂点１８０、接続バンプ１７の表面部１７０及びカバーシート１１の外表面１１０を同一平面上に整合させる。さらに、半導体装置１の全体の高さを低減させたい場合は、前記接続バンプ１７及びカバーシート１１を前記第２の樹脂被覆層１８から露出させた後、基板１０の方向に向けて前記第２の樹脂被覆層１８と、接続バンプ１７及びカバーシート１１を適切な厚さまでに研磨することができる。前記第２の樹脂被覆層１８の頂点１８０と、接続バンプ１７の表面部１７０及びカバーシート１１の外表面１１０が同一平面になるようにしたので、前記半導体装置１の接続バンプ１７の表面部１７０と外部装置、例えば、プリント基板上の接続パッド（図示しない）を表面接続技術（surface mounting technology, SMT）等の方式で電気的に接続させる時に、それぞれの接続バンプ１７を均一に外部装置上の接続点に接続させることが出来る。故に従来ＢＧＡ型半導体装置に発生する半田ボール３９端部の不均一平面による接続不良は発生しない。従って、本発明による半導体装置１はより良い加工性を有する。

【００３２】また、基板１０の第１の表面１０１及び第２の表面１０２上に第１の樹脂被覆層１５と第２の樹脂被覆層１８を形成するので、装置本体の構造上において機械強度を増強する他、温度循環及び実際操作中の高温環境においても、第１の樹脂被覆層１５と第２の樹脂被覆層１８が基板１０に対して発生する熱応力を効果的に吸収して装置本体の反り（warpage）の発生を防止し、半導体素子１２とカバーシート１１間に剥離が発生する

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ことを回避する。よって、製品の歩留及び信頼性向上になる。

【００３３】さらに、前記半導体素子１２を基板１０の大径孔１００内に収納し、且つ、第１の樹脂被覆層１５及び第２の樹脂被覆層１８の厚さは、従来の半導体装置３における素子３２の厚さと半田ボール３９の高さよりも小さいので、本発明の半導体装置１における全体の高さは、従来の素子３２を基板３０上面に粘設し、半田ボール３９を基板３０底面に植設したＢＧＡ型半導体装置の全体の高さに比べて低くなる。従って薄型化の要求に対応することができる。

【００３４】また、前記基板１０の第１の表面１０１及び第２の表面１０２上にそれぞれ第２の樹脂被覆層１８及び第１の樹脂被覆層１５を形成することによって、装置本体の機械強度が増加する。従って、基板１０の厚さを小さくしても装置全体の機械強度は十分に確保できる。

【００３５】なお、上述の実施例１では透明シート１６を開孔部１５０に嵌着させたが、図２に示すように第１の樹脂被覆層１５の表面全体に被着して開孔部１５０をその他の領域と共に封止してもよい。

【００３６】実施例２

図３は、本発明の実施例２の薄型感光式半導体装置２におけるさらに別の実施形態の断面図である。この実施例２の半導体装置２の構造は、前記実施例１とほぼ同一である。しかし、実施例２の半導体装置２に使用される素子２２及び金線２４を外部から気密隔離する部材に充填樹脂体２６が用いられる。充填樹脂体２６として、透明樹脂体を基板２０の大径孔２００と第１の樹脂被覆層２５の開孔部２５０に充填して硬化させる。形成後の充填樹脂体２６によって、前記素子２２及び金線２４を外部から気密隔離すると共に、前記基板２０の第１の表面２０１上に周知の方法で、ＳｎまたはＳｎ・Ｐｂ合金の半田ボール２７を形成し、半田ボール２７と前記基板２０の接続２０４とを電気的に接続させ、前記基板２０の第１の表面２０１上に、封止シート２１及び半田ボール２７とを被覆する第２の樹脂被覆層２８を形成した後、研磨にて前記第２の樹脂被覆層２８及び半田ボール２７の厚さを封止シート２１等の高さ迄に薄型化し、前記第２の樹脂被覆層２８の頂点２８０と半田ボール２７の表面２７０及び封止シート２１の外表面２１０を同一表面になるように研磨して、平坦な表面を形成する。

【００３７】

【発明の効果】以上に説明したように、本発明の薄型感光式半導体装置は、全体の厚さが薄くなり、且つ、外部装置との電気的接続性が良くなる効果がある。

【図面の簡単な説明】

【図１】本発明の実施例１の薄型感光式半導体装置の断面図である。

【図２】本発明の実施例１の薄型感光式半導体装置における別の実施形態の断面図である。

【図３】本発明の実施例２の薄型感光式半導体装置におけるさらに別の実施形態の断面図である。

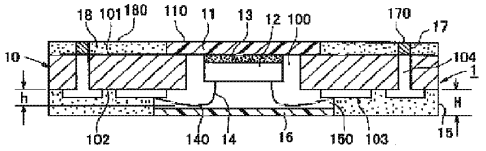
【図４】従来の感光式半導体装置の断面図である。

【符号の説明】

１　半導体装置	３　半導体装置
１０　基板	１１　カバーシート
１２　半導体素子	
１４　金線	１５　第１の樹脂体
１７　接続バンプ	１８　第２の樹脂体
３０　基板	３２　素子
３４　金線	３６　ケース体
３８　透明蓋体	３９　半田ボール
１００　大径孔	１０１　第１の表面
１０２　第２の表面	１０３　接続電極
１０４　接続孔	
１４０　円弧頂点	１５０　開孔部
１７０　表面部	１８０　頂点
ｈ　高さ	Ｈ　厚さ

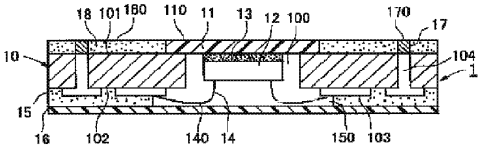
【図１】

FIG. 1



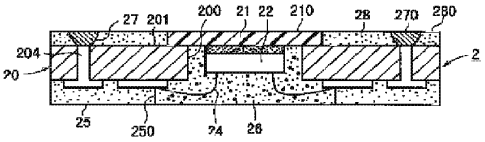
【図２】

FIG. 2



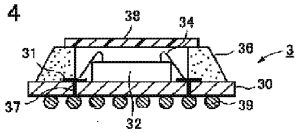
【図3】

FIG. 3



【図4】

FIG. 4



Electronic Acknowledgement Receipt

EFS ID:	26312553
Application Number:	14747875
International Application Number:	
Confirmation Number:	1722
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	136549
Filer:	Andrew W. Schultz/Jillian Stockel
Filer Authorized By:	Andrew W. Schultz
Attorney Docket Number:	143705.05211
Receipt Date:	11-JUL-2016
Filing Date:	23-JUN-2015
Time Stamp:	15:49:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	IDSTransmittal.pdf	102190 c46a80244ef83384d8eb5fbb709f09c178ba0906	no	2
Warnings:					

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	Sub1449.pdf	809140 780579f8c62ac02f64d6a247ffc3336199de2d7d	no	20
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4	Foreign Reference	EP0473439A2.pdf	651670 59d8287bba0a6aa7574dd7d25ecc7d64dc431ff2	no	11
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5	Foreign Reference	EP0566156A1.pdf	2045450 329d7a3636b72d25be4bf4c1a66527669814e2508	no	26
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6	Foreign Reference	EP1630871A1.pdf	814623 16238f4837f929d06eb51ad48b66b6b80394b4ef	no	22
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7	Foreign Reference	EP1794804A2.pdf	19989 8dfcaf3a44ecfd44e361d16bc5aca4a4c7e783b6	no	1
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8	Foreign Reference	EP1873840A1.pdf	1226159 542aa022ea6f8b82f189c83a6e1c102982d079c1	no	18
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9	Foreign Reference	EP2073270.pdf	11423386 3aadd5471a9a017201e2f0df98685ae7626599db	no	65
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18	Foreign Reference	JPH06275641.pdf	296929 d60269e8faca202867f9294c16eb025e3799e501	no	6
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New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No.: 143705.05211
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Martin U. Pralle	Confirmation No.: 1722
Application No.: 14/747,875	Art Unit: 2814
Filed: June 23, 2015	Examiner: Long Pham
For: PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS	

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July 11, 2016 (Dated)
Electronic Signature: /Andrew W. Schultz/
Andrew Schultz, Reg. No. 66,869

INFORMATION DISCLOSURE STATEMENT (IDS)

Dear Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached Substitute for Form 1449/PTO. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed before the mailing date of a first Office Action on the merits as far as is known to the undersigned (37 CFR 1.97(b)(3)).

In accordance with 37 CFR 1.98(a)(2)(ii), Applicant has not submitted copies of U.S. patents and U.S. patent applications. Applicant submits herewith copies of foreign patents and non-patent literature in accordance with 37 CFR 1.98(a)(2).

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In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in § 1.56 (b).

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 50-0436, under Order No. 143705.05211.

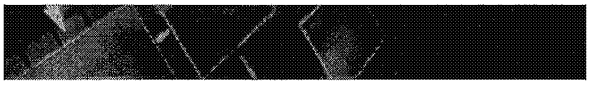
Dated: July 11, 2016

Respectfully submitted,
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Near-infrared spectroscopy as an index of brain and tissue oxygenation

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Author Affiliations

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Abstract

Continuous real-time monitoring of the adequacy of cerebral perfusion can provide important therapeutic information in a variety of clinical settings. The current clinical availability of several non-invasive near-infrared spectroscopy (NIRS)-based cerebral oximetry devices represents a potentially important development for the detection of cerebral ischaemia. In addition, a number of preliminary studies have reported on the application of cerebral oximetry sensors to other tissue beds including splanchnic, renal, and spinal cord. This review provides a synopsis of the mode of operation, current limitations and confounders, clinical applications, and potential future uses of such NIRS devices.

Key words brain, ischaemia brain, oxygen consumption measurement techniques, oximeters monitoring, oxygen oxygen, saturation

Reflectance near-infrared spectroscopy

Jobsis[34] first reported in 1977 that the relatively high degree of transparency of myocardial and brain tissue in the near-infrared (NIR) range enabled real-time non-invasive detection of tissue oxygen saturation using transillumination spectroscopy. By 1985, Ferrari and colleagues[19] reported some of the first human cerebral oximetry studies using near-infrared spectroscopy (NIRS). After United States Food and Drug Administration (FDA) approval, in May 1993, the first commercial cerebral oximetry device, INVOS 3100®, was marketed (Somanetics Corporation, Troy, MI, USA). Subsequently, after FDA approval, CAS Medical Systems (Branford, CN, USA) and Nonin Medical Inc. (Minneapolis, MN, USA) also began marketing NIRS cerebral oximetry devices.

NIR light can be used to measure regional cerebral tissue oxygen saturation (rSO_2). This technique uses principles of optical spectrophotometry that make use of the fact that biological material, including the skull, is relatively transparent in the NIR range. However, because of the poor signal-to-noise ratio as a result of the low intensity of transmitted light, most commercially available devices use reflectance-mode NIRS in which receiving optodes are placed ipsilateral to the transmitter and exploit the fact that photons transmitted through a sphere will traverse an elliptical path in which the mean depth of penetration is proportional to the transmitter and receiver optode separation. Fundamental challenges posed in utilizing transcranial reflectance NIRS to measure cerebral tissue oxygen saturation include the potential requirement for knowledge of the photon pathlength, the presence of non-haeme chromophores, and variable light absorption by overlying extracerebral tissue.

Tissue oxygen saturation

Measurement of tissue oxygen saturation and tissue haemoglobin content is determined by the difference in intensity between a transmitted and received light delivered at specific wavelengths as described by the Beer–Lambert law (see below). A decrement in transmitted light intensity is equivalent to the quantity of the substance and the amount of light absorbed by a unit quantity of that substance, defined as the extinction coefficient (ε), a factor that varies with the substance and the incident-light wavelength. The depth of penetration is proportional to the mean pathlength of photons through tissue.

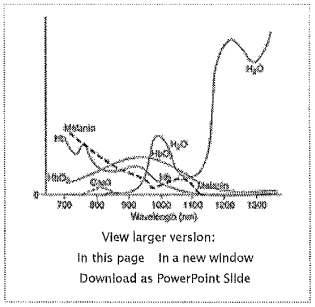
Transmission of light at a given wavelength through tissue depends on a combination of reflectance, scattering, and absorptive effects. Reflectance is a

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function of the angle of the light beam and the regularity of the tissue surface. This decreases with increasing wavelength, thus favouring transmission of NIR *vs* visible light. Scattering is a function of tissue composition and number of tissue interfaces while absorption is determined by the molecular properties of substances within the light path. Above 1300 nm, water (H_2O) absorbs all photons over a pathlength of a few millimetres with a secondary peak between 950 and 1050 nm, whereas below 700 nm, increasing light scattering and more intense absorption bands of haemoglobin prevent effective transmission. In the 700–1300 nm range, NIR light penetrates biological tissue several centimetres.[48]

Within the NIR range, the primary light-absorbing molecules in tissue are metal complex chromophores: haemoglobin, bilirubin, and cytochrome. The absorption spectra of deoxyhaemoglobin (Hb) ranges from 650 to 1000 nm, oxyhaemoglobin (HbO_2) shows a broad peak between 700 and 1150, and cytochrome oxidase aa3 (Caa3) has a broad peak at 820–840 nm (Fig. 1).[34] The wavelengths of NIR light used in commercial devices are selected to be sensitive to these biologically important chromophores and generally utilize wavelengths between 700 and 850 nm where the absorption spectra of Hb and HbO_2 are maximally separated and there is minimal overlap with H_2O. The *isobestic* point (wavelength at which oxy- and deoxyhaemoglobin species have the same molar absorptivity) for Hb/HbO_2 is 810 nm. As discussed below, the isobestic absorption spectra can be utilized to measure total tissue haemoglobin concentration.



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Fig 1
Absorption spectra for oxygenated haemoglobin (HbO_2), deoxygenated haemoglobin (Hb), Caa3, melanin, and water (H_2O) over wavelengths in NIR range. Note the relatively low peak for Caa3. Commercial cerebral NIRS devices currently utilize wavelengths in the 700–850 nm range to maximize separation between Hb and HbO_2. The presence of melanin as found in human hair can significantly attenuate Hb, HbO_2, and Caa3 signals.

As outlined previously, the absorption of NIR light in tissue is determined by the Beer–Lambert law relating pathlength of NIR light to the concentration and absorption spectra of tissue chromophores and is conventionally written as:

$$\Delta A = L \times \mu$$

where ΔA is the amount of light attenuation, L the differential photon pathlength through tissue, and μ the absorption coefficient of chromophore X and can be expressed as [X]×ε, where [X] is the tissue concentration of chromophore X and ε the extinction coefficient of chromophore X, thus $[X]=\Delta A/L\times\varepsilon$, which, in theory, allows measurement of tissue oxygen saturation (SO_2).

Multiwavelength NIRS and absolute vs relative oxygen saturation

Since ΔA is measured directly and ε has been determined for various tissue chromophores, absolute chromophore concentration [X] is thus inversely proportional to the optical pathlength. However, photon pathlength cannot be measured directly due to reflection and refraction in the various tissue layers involved. Unless pathlength can be determined, only relative change in chromophore concentration can be assessed. Modelling and computer simulation can be used to estimate photon tissue pathlength. By using successive approximation, an analysis algorithm can be calibrated to provide a measure of absolute change of chromophore concentration, as utilized by some commercial devices.

In order to measure absolute tissue chromophore concentrations, a different approach is used based on radiative transport theory and using multiple NIRS wavelengths and frequency-domain NIRS (fdNIRS) or time-domain NIRS (tdNIRS)

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analyses to determine tissue absorption coefficients (μ). Theoretically, approaches such as fdNIRS or tdNIRS avoid the need for actual photon pathlength determination.[42 46] Fundamental to such techniques is that tissue absorption coefficients can be measured directly using multiwavelength NIRS. Since

$$\mu = [X] \times \varepsilon$$

tissue chromophore concentration can thus be measured absolutely, there is no requirement for determination of optical pathlength.[40] This approach has been shown to yield reasonable fidelity using an *in vitro* model of human skull and brain, but haemoglobin concentration <6 g dl^{-1} yields errors of ~15% and increasing skull thickness produces errors as high as 32%.[40] Accordingly, some correction for extracerebral tissue must still be made even with such 'absolute' measurements.

NIRS limitations and confounds

Extracerebral tissue

Transcutaneous NIRS is reflective of a heterogeneous tissue field containing arteries, veins, and capillary networks and also other non-vascular tissue. For NIRS of cerebral tissue, photons must penetrate several tissue layers including scalp, skull, and dura, which can contain various concentrations of blood and tissue-derived chromophores. Both computer simulation and experimental tissue models of transcranial NIR light transmission have demonstrated an elliptical photon distribution centred around the transmitter whose mean depth is proportional to the separation of the optodes by a factor of ~1/3.[21] Increasing transmitter/receptor distance increases depth of penetration and minimizes the effect of extracerebral tissue,[21] but power must be limited to prevent direct thermal tissue damage. Since signal intensity is inversely proportional to the square of the pathlength, 5 cm separation appears to be the functional maximal optode spacing.[58] This provides a mean depth of NIR light penetration ~1.7 cm giving increased weighting to cerebral *vs* extracerebral tissue.[58] As there is still significant attenuation from extracerebral tissue even with optimized transmitter/receiver separation, additional techniques must be utilized.

Spatial resolution

Since mean depth of photon penetration approximates 1/3 the transmitter/receiver separation, by utilizing two differentially spaced receiving optodes—one spaced more closely and the other spaced farther from the transmitter—a degree of spatial resolution can be achieved. Accordingly, the closer receiver (e.g. 3 cm separation) detects primarily superficial tissue, whereas the farther optode (e.g. 4 cm separation) reflects deeper tissue. Incorporation of a subtraction algorithm enables calculation of the difference between the two signals and thus a measure of deeper, cortical tissue saturation. Thus differential spacing of receiving optodes can provide spatial resolution to distinguish signals from cerebral *vs* extracerebral tissue. In certain models, this has been interpreted as demonstrating transcutaneous photon penetration to the level of the cerebral ventricles.[58] It has been estimated that ~85% of cerebral regional oxygen saturation (rSO_2) is derived from cortical tissue with the remaining 15% derived from overlying extracerebral tissue.

Cerebral arterial/venous blood partitioning

Cerebral NIRS devices measure mean tissue oxygen saturation and, as such, reflect haemoglobin saturation in venous, capillary, and arterial blood comprising the sampling volume. For cerebral cortex, average tissue haemoglobin is distributed in a proportion of ~70% venous and 30% arterial,[47] based on correlations between position emission tomography (PET) and NIRS.[58] However, clinical studies have demonstrated that there can be considerable biological variation in individual cerebral arterial/venous (A/V) ratios between patients, further underscoring that the use of a fixed ratio can produce significant divergence from actual *in vivo* tissue oxygen saturation, thus confounding even 'absolute' measures of cerebral oxygenation, for example, fdNIRS or tdNIRS.[80] A further confound can be introduced if there is significant variation in haemoglobin concentration as a consequence of haemodilution which may give rise to changes in cerebral rSO_2 without attendant alterations in jugular venous oxygen saturation.[87] Whether this represents subclinical regional ischaemia, changes in photon pathlength, alterations in cerebral A/V partitioning, or other factors remain unclear.[60 87]

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In clinical practice, the use of cerebral NIRS as a trend monitor with interventions designed to preserve cerebral saturation values close to their individual baseline values has produced a significantly lower incidence of adverse clinical events in patients undergoing coronary artery bypass (CAB) surgery.[51] A trend monitoring approach thus minimizes confounds introduced by biological variation in individual cerebral A/V ratios and outer layer tissue composition. These can produce an 'offset' in measured saturation values and result in inaccurate therapy if based on the assumption that a device is measuring 'absolute' *in vivo* cerebral oxygenation.

Extracerebral tissue

It is important to recognize that confounders such as extracerebral or subdural haematoma can change the proportion of cerebral to extracerebral haemoglobin and thus offset tissue oxygen saturation values by a variable amount. Using computed tomographic assessment of skull thickness (t-skull), cerebrospinal fluid area (a-CSF), and haemoglobin concentration, NIRO-100® (Hamamatsu Photonics KH, Hamamatsu City, Japan) was compared with INVOS 4100® (Somanetics Corporation) in a recent study of 103 cardiac surgical and neurosurgical patients.[88] This study demonstrated that INVOS rSO_2 values were potentially influenced by haemoglobin concentration, t-skull, and a-CSF. There was a potential confound in this evaluation as there was no assessment of superficial tissue attenuation of NIR light, for which INVOS uses a subtraction algorithm as compensation.[88] One implication of this is reflected in the potential for artifact and signal attenuation when extracerebral tissue is thickened or oedematous. Since haemoglobin represents the primary chromophore at these wavelengths, extracranial or subdural haemorrhage can artifactually influence measured cerebral saturation values. Based in part on PET studies, most clinical NIRS devices assume venous/arterial distribution in cortical tissue of ~70/30%.[32] Consequently, changes in rSO_2 largely reflect alterations in cerebral venous saturation and may also vary between patients.

Significant changes in extracerebral tissue saturation as induced by a scalp tourniquet have been shown to confound the ability to measure changes in cerebral rSO_2.[22] However, in a non-tourniquet clinical study of oxygenation of blood drawn from both the facial vein and the jugular venous bulb, there was no correlation between cerebral rSO_2 and facial vein oxygenation, but there was a significant correlation between regional cerebral oxygenation and jugular venous bulb oxygenation.[24] The authors concluded that extracranial tissue oxygenation had a negligible influence on the values recorded using NIRS but noted that individual changes in jugular venous bulb oxygenation may be poorly reflected.[24]

Non-haeme tissue chromophores

Because melanin pigmentation, as found in hair,[62] can significantly attenuate light transmission and impede NIRS measurements, optimal placement of transmitting and receiving optodes is high on the frontal eminences, ~2–3 cm above the orbital ridge to avoid frontal sinuses. Melanin in skin is confined to the epidermal layer at a depth of 50–100 μm and as such does not appear to produce significant attenuation of NIRS signal. However, conjugated bilirubin has an absorption peak at 730 nm, and is deposited throughout all tissue layers such that concern has been raised about the ability of NIRS to assess cerebral oxygenation in the presence of jaundice. In a study of 48 patients undergoing orthotopic liver transplantation, total plasma bilirubin was related to rSO_2 as determined from NIRS. During reperfusion of the grafted liver, rSO_2 increased by an average of 7%, and plasma bilirubin concentration did not influence the increase. Although bilirubin dampens the cerebral NIRS, even at high bilirubin values changes in cerebral perfusion can be discerned.[44] This further supports the approach of establishing a baseline value in each patient individually and observing for perturbations from that baseline rather than relying primarily upon a specific threshold value.

Non-metabolizing tissue

Tissue oxygen saturation in non-metabolizing tissue can be high or low, and can be near normal in dead or non-metabolizing brain because of sequestered cerebral venous blood in capillaries and venous capacitance vessels.[17] Schwarz and colleagues[71] examined rSO_2 in 18 adult human cadavers and found values in one-third of the subjects that exceeded the lowest values that they had previously recorded in normal subjects raising concern regarding the validity of

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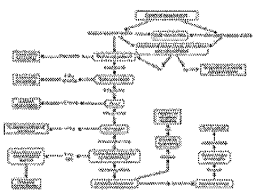
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the rSO_2 measurement. However, Maeda and colleagues[45] examined cerebral venous oxygen saturation during 214 autopsies and found the values to range from 0.3% to 95.1% apparently as a consequence of total haemoglobin content, cause of death, and cadaver storage conditions. Accordingly, rSO_2 or other measures of cerebral oxygen saturation can appear discordantly high, which rather than indicative of error may reflect the pathophysiology of non-metabolizing yet non-perfused tissue.[71] In clinical practice, it is thus the detection of 'context-sensitive change' in cerebral NIRS (e.g. during cooling or rewarming) that is of fundamental importance rather than an 'absolute' value.

Clinical applications

A number of the limitations as discussed above have raised questions regarding the clinical utility of cerebral oximetry monitoring.[60 89] However, a number of clinical studies and case reports have demonstrated that despite such limitations, the ability of cerebral oximetry monitoring to detect otherwise clinically silent episodes of cerebral ischaemia in a variety of clinical settings renders it an important safeguard for cerebral function. In a recent study in patients with subarachnoid haemorrhage, episodes of angiographic cerebral vasospasm were strongly associated with reduction in trend ipsilateral NIRS signal.[5] Furthermore, the degree of spasm (especially more than 75% vessel diameter reduction) was associated with a greater reduction in same-side NIRS signal demonstrating real-time detection of intracerebral ischaemia.

The proper management of brain oxygenation is one of the principal endpoints of all anaesthesia procedures, but the brain remains one of the least monitored organs during clinical anaesthesiology. There are some medical procedures where iatrogenic brain ischaemia is present, including carotid endarterectomy (CEA) in patients with high-grade carotid artery stenosis, temporary clipping in brain aneurysm surgery, hypothermic circulatory arrest for aortic arch procedures, and others in which the pathology itself generates brain ischaemia, such as traumatic brain injury and stroke. One of the most common limitations seen in studies assessing the impact of cerebral oximetry monitoring has been the absence of a defined protocol based on physiologically derived interventions to treat decreases in rSO_2. In order to provide a pathophysiological rationale for interventions and to facilitate clinical strategies designed to improve cerebral rSO_2, an intervention algorithm has been devised (Fig. 2),[16] and has proven effective in improving outcomes in at least two separate randomized prospective clinical trials.[10 51]



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Fig 2
Proposed algorithm in the use of brain oximetry. CT, computed tomography; ICHT, intra-cranial hypertension; MAP, mean arterial pressure; MRI, magnetic resonance imaging. Reprinted from Denault and colleagues,[16] with permission from SAGE Publications Inc.

Cardiac surgery

Coronary artery bypass surgery

There have been a number of case-control and retrospective studies of cerebral oximetry in cardiac surgical procedures that have shown improvements in outcome associated with cerebral oximetry monitoring and correlations between cerebral desaturation and adverse outcomes.[18] However, to date there have been relatively few randomized, prospective clinical trials. In a study utilizing cerebral oximetry in 265 patients undergoing primary CAB surgery and randomized to active monitoring and a series of interventions designed to improve rSO_2 or to a control group in which blinded monitoring was used, a significant association was found between prolonged cerebral desaturation and early cognitive decline, and also a three-fold increased risk of prolonged hospital stay.[72] However, cerebral desaturation rates were similar between the groups and ascribed to poor

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compliance with the treatment protocol, resulting in no difference in the incidence of cognitive dysfunction between the groups. In a prospective, randomized blinded study in 200 patients undergoing coronary artery grafting, active treatment of declining cerebral rSO_2 values prevented prolonged cerebral desaturations and was associated with a shorter intensive care unit length of stay and a significantly reduced incidence of major organ morbidity or mortality.[51 52] The intervention protocol undertaken to return rSO_2 to baseline resulted in a rapid improvement in rSO_2 in 84% of cases and did not add undue risk to the patient, including no increase in allogeneic blood transfusions.[16 51] There were also numerically fewer clinical strokes in the monitored patients consistent with previous studies. For example, a significant reduction in perioperative stroke rate, from 2.0% to 0.97%, was observed in patients in whom INVOS rSO_2 cerebral oximetry was used to optimize and maintain intraoperative cerebral oxygenation in comparison with an untreated comparator group operated upon in the preceding 18 month interval.[23]

Deep hypothermic circulatory arrest

Moderate (25–30°C) and deep (<25°C) hypothermia remain a mainstay for cerebral and systemic protection during complex aortic arch repair, since surgical access can require interruption of systemic perfusion for relatively protracted periods. As there is relatively little ability to monitor cerebral function during such times since EEG becomes progressively attenuated below 25°C, cerebral NIRS has been advocated as a means of monitoring and detecting onset of cerebral ischaemia during deep hypothermic circulatory arrest.[38 39] In a study of 46 consecutive patients in whom selective anterograde cerebral perfusion (SACP) was established by perfusion of the right subclavian artery (with or without left carotid artery perfusion) or by separate concomitant perfusion of the innominate and the left carotid arteries, bilateral regional cerebral tissue oxygen saturation index was monitored by INVOS 4100 NIRS.[59] Six patients died in hospital, and six patients (13%) experienced a perioperative stroke in all of whom rSO_2 values were significantly lower during SACP and in whom rSO_2 tended to be lower in the affected hemisphere. During selective antegrade cerebral perfusion, regional cerebral tissue oxygen saturation decreasing to between 76% and 86% of baseline had a sensitivity of up to 83% and a specificity of up to 94% in identifying individuals with stroke. It was concluded that monitoring of regional cerebral tissue oxygen saturation using NIRS during SACP allows detection of clinically important cerebral desaturations and can help predict perioperative neurological sequelae.[59]

There have also been a number of case reports of aortic arch surgery in which cerebral oximetry has been shown to detect cerebral hypoperfusion from a variety of factors including ascending aortic dissection with occlusion of carotid lumen,[33] intraoperative thrombosis of a common carotid graft,[69] kinking or obstruction of perfusion cannula during SACP,[67] or due to diminished Blalock–Taussig shunt flow after paediatric cardiac surgery.[65]

Carotid endarterectomy

During CEA, temporary cross-clamping of the internal carotid artery (ICA) is an integral part of the surgery and can produce brain ischaemia in patients with poor collateral flow. The perioperative stroke rate after CEA can be as high as 5%,[2 66] a situation that renders intraoperative brain monitoring of special interest.[53] Monitoring devices such as transcranial Doppler (TCD), EEG, and somatosensory evoked potentials (SSEP) have been used successfully for a number of years but have logistic limitations and disadvantages.[3 12 15 83] In up to 20% of patients, TCD cannot be performed due to relative absence of transcranial window, while SSEP and EEG measurements are influenced by anaesthetic agents and electrocautery, and involve a high level of technical complexity. In at least one large clinical study of 314 patients undergoing awake CEA, EEG identified cerebral ischaemia in only 59% of patients needing shunt placement, with a false-positive rate of 1.0% and a false-negative rate of 41%, concluding that both stump pressure (SP) and EEG as a guide to shunt placement have poor sensitivity.[27] Although measurement of SP after common carotid clamping is also used as a method to assess adequacy of collateral flow through the Circle of Willis, it is not widely used in the clinical setting as it is affected by numerous factors including arterial pressure, Pa_{co_2}, and type of anaesthetic agent,[31 50] and has the significant disadvantage of being a one-time

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discontinuous measurement, thus rendering it incapable of detecting ischaemia developing later during performance of the arterectomy.

Various studies have shown that cerebral oximetry monitoring can be a valuable tool for detection of cerebral ischaemia during CEA.[8 9 30 50 77 85 86] In comparison with other modalities, non-invasive NIRS devices are easy and simple to use and provide continuous measurement of frontal cortex oxygen saturation. A major thrust of most studies utilizing intraoperative NIRS during CEA has been defining the sensitivity and specificity of changes in cerebral rSO_2 as correlated with either clinical signs of cerebral ischaemia or other neuromonitoring modalities. Among the earliest of these was a study from 1998 in which there was a positive correlation between TCD and NIRS comparing the percentage change in middle cerebral artery flow velocity *vs* change in rSO_2.[37] In 99 patients undergoing awake CEA with cervical plexus anaesthesia, regression analysis was used to evaluate the specificity and sensitivity of various rSO_2 cut-off points to detect neurologically defined intraoperative brain ischaemia.[68] A sensitivity of 80% with a specificity of 82% was found using a cut-off point of 20% relative decrease in rSO_2, with a false-positive and false-negative rate of 67% and 2.6%, respectively. Similar results were found in another study in which brain ischaemia with possible neurological compromise could result when cerebral rSO_2 was <54–56% during carotid cross-clamping. A reduction in rSO_2 of 16–18% during CEA was a predictor of neurological compromise.[30 68]

A large cohort of NIRS data from 594 CEA performed under general anaesthesia was studied to determine the sensitivity, specificity, and predictive values of various rSO_2 cut-off points to predict the need for shunting or resulting in neurological complications.[49] The previously described 20% reduction by Samra and colleagues[68] was found to have a low sensitivity of 30% but a very high specificity (98%), with positive and negative predictive values of 37% and 98%, respectively. Accordingly, a cut-off point utilizing a 12% decrease in rSO_2 was identified as optimal, having a sensitivity of 75% and a specificity of 77% with a positive predictive value of 37% and a negative value of 98%.[49] Subsequently, in 50 patients having CEA under cervical plexus block, an independent neurologist evaluated clinical and EEG signs of ischaemia during continuous NIRS monitoring.[64] Ten per cent of patients experienced clinical and EEG brain ischaemia requiring shunt placement and in these patients, the reduction in NIRS averaged 17% whereas the NIRS reduction in those with no clinical or EEG ischaemia was 8%, a difference consistent with the 12% threshold as determined by Mille and colleagues.[49] Concern has been raised that in comparison with TCD, decreases in rSO_2 >13% during CEA, while sensitive, are less specific, have a false-positive rate of 17%, and can lead to unnecessary shunt placement.[25] However, in this study,[25] TCD was technically inadequate in four of 59 patients, underscoring the compromise between sensitivity, specificity, and reliability of these various monitoring modalities for intraoperative detection of cerebral ischaemia.

Overall, these studies indicate that utilizing a decrease in cerebral rSO_2 of >12% is a reliable, sensitive, and relatively specific threshold for brain ischaemia secondary to ICA clamping and necessitates shunt placement or other pharmacological or physiological intervention. A caveat is necessary, however, based on a recent report.[20] In this series, multi-modality neuromonitoring of 323 CEA procedures under general anaesthesia showed significant discrepancies in 24 patients (7.4%), of whom 16 showed no significant EEG/SSEP changes but profound changes occurred in rSO_2 and no shunt was placed, whereas in seven patients, there was no change in rSO_2 but a profound change in EEG/SSEP and shunts were placed. These authors reported that the sensitivity of rSO_2 compared with EEG/SSEP was 68%, and the specificity was 94% yielding a positive-predictive value of 47% and a negative-predictive value of 98%,[20] essentially similar to data from Mille and colleagues.[49]

Post-CEA hyperperfusion syndrome

Postoperative neurological complication after CEA can be related to rebound increases in cerebral blood flow (CBF) after surgical repair of carotid stenosis. Impaired autoregulation as a consequence of chronic brain ischaemia with a rapid restoration of regional perfusion can generate a hyperperfusion syndrome characterized by headache, brain oedema, seizures, and in severe cases intracerebral haemorrhage.[57] A significant correlation between rSO_2 values immediately after declamping and changes in CBF was found with a sensitivity and specificity for detecting patients at risk of developing hyperperfusion

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syndrome of 100% and 86.4%, respectively, using a cut-off value of 5%.[56 57] With this 5% cut-off point, cerebral oximetry demonstrated a positive predictive value of 50% and a negative predictive value of 100%.

The use of NIRS has also been explored in head injury patients; however, the results have been equivocal. A poor correlation with ICP and jugular oximetry indicates a low sensitivity of cerebral oximetry after acute brain injury.[7] However, good sensitivity of the cerebral oximetry for detection of intracranial haematomas correlating with computed tomography or MRI has been reported.[35] The use of cerebral oximetry in traumatic head injury remains an area of interest.[26]

Paediatrics

In complex settings such as paediatric cardiac surgery, paediatric neurosurgery, and paediatric and neonatal intensive care, NIRS is being increasingly used to monitor and detect episodes of cerebral ischaemia both intraoperatively when combined with bispectral index monitoring,[29] and after operation where decreased cerebral rSO_2 within 48 h of surgery has been associated with adverse outcomes after the Norwood procedures.[61] Premature and low birth weight infants are at significant risk for apnoea due to brain immaturity, intraventricular/intraparenchymal haemorrhage (IVH), and periventricular leukomalacia, the common pathophysiological pathway for all involving cerebral ischaemia.

Cerebral oximetry has been used to evaluate variations in the cerebral circulation in 11 preterm infants presenting with 145 apnoeic episodes.[84] Standard monitoring including Sp_{O_2}, heart rate, ventilatory frequency, and arterial pressure was compared against the change in NIRS-derived cerebral blood volume and cerebral oxygenation during apnoeic episodes. A significant change in cerebral circulation was found during the apnoeic episode, such that when the Sp_{O_2} dropped below 85%, total cerebral haemoglobin increased and rSO_2 decreased.

In neonatal birth asphyxia, mild brain cooling has been utilized in an attempt to minimize subsequent cerebral hyperaemia and IVH. In a recent study, cerebral oximetry and EEG were used to document changes in cerebral perfusion during mild systemic cooling.[1] Cerebral NIRS identified a reduction in cerebral blood volume (CBV) during hypothermia that recovered during the rewarming period, whereas brain oxygenation remained stable. As brain cooling is thought to reduce delayed hyperaemia and to help maintain neuronal metabolism after cerebral insults, cerebral oximetry monitoring may be useful during hypothermia treatments in order to monitor changes in CBV and brain oxygenation as possible indicators of the efficacy of such treatment.

In many settings, mixed venous oxygen saturation (Sv_{O_2}) is used to monitor the adequacy of cardiac output and as a surrogate for cerebral oxygenation during paediatric cardiovascular surgery and neonatal and paediatric intensive care.[75 81] Tortoriello and colleagues[75] validated the use of NIRS in estimating Sv_{O_2} in 20 paediatric cardiac surgery patients and demonstrated a positive correlation between rSO_2 and Sv_{O_2}.[75] In a larger study of 155 critically ill neonates and infants, cerebral tissue oxygenation index (cTOI—defined as the ratio of oxygenated to total haemoglobin) correlated with arterial oxygen saturation, arteriovenous oxygen extraction, and central venous oxygen saturation.[81] A significant correlation between cerebral rSO_2 and superior vena cava oxygen saturation during inhalation of either room air or oxygen 100% was reported in 29 postoperative paediatric heart transplant patients undergoing myocardial biopsy;[6] rSO_2 was also the best predictor of pulmonary artery saturations. Intraoperative cerebral rSO_2 studied in comparison with Sv_{O_2} in 20 paediatric cardiac surgical patients <10 kg body weight showed that cerebral rSO_2 was more sensitive for cerebral desaturation and is thus an early and sensitive monitor of adequacy of brain perfusion because Sv_{O_2} primarily represents lower torso oxygenation status.[63] For paediatric patients in whom haemodynamic monitoring is necessarily limited, monitoring the adequacy of systemic perfusion using cerebral oximetry appears to be an appropriate surrogate.

Tissue perfusion

There is increasing interest in the utilization of cerebral oximetry sensors to monitor adequacy of tissue perfusion when placed on somatic sites in both adult

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and paediatric patients.[4,41,70,76,78] In settings including volume rescuscitation in traumatic shock,[13,73,79] dehydrated paediatric patients,[28] and as an estimate of splanchnic perfusion after paediatric cardiac surgery,[36] somatic NIRS has been found to correlate with other indices of tissue perfusion. Lower extremity rSO_2 was used to confirm the development of compartment syndrome after surgical cutdown for vascular access,[74] whereas others have used NIRS to assess the effect of various anaesthetic agents on skeletal microcirculation.[14]

NIRS has been reported as a monitor for non-cerebral tissue oxygenation with the objective of comparing liver tissue oxygenation (TOI[liver]) with Sv_{O_2} and intestinal perfusion measured by gastric mucosa pH (pHi) in 20 paediatric patients undergoing craniofacial surgery with expected major blood loss.[82] Although only a moderate positive correlation was demonstrated between TOI [liver] and Sv_{O_2} and gastric pHi, intra-individual TOI[liver] values, however, demonstrated close correlation with Sv_{O_2} values but a varying correlation with gastric pHi values. These investigators concluded that while TOI[liver] provided a better trend monitor of central venous oxygen saturation than pHi, overall, because of its limited sensitivity and specificity to indicate deterioration of Sv_{O_2}, TOI[liver] was not felt to provide additional practical information for clinical management in this setting.[82]

More recently, correlations between renal rSO_2, abdominal (splanchnic) rSO_2, and gastric tonometry, central mixed venous saturation, and blood lactate were examined in 20 postoperative neonates with congenital heart disease within 48 h of surgery.[36] There was a strong correlation between abdominal rSO_2 and pHi and also between abdominal rSO_2 and Sv_{O_2} and a significant negative correlation between the abdominal rSO_2 and serum lactate. The investigators concluded that abdominal site rSO_2, measured in infants with either single or biventricular physiology, exhibits a strong correlation with gastric pHi and also with serum lactate and Sv_{O_2} and that rSO_2 measurements over the anterior abdominal wall correlate more strongly than flank rSO_2 with regard to systemic indices of oxygenation and perfusion. Abdominal NIRS monitoring thus appears to be a valid modality providing real-time, continuous, and non-invasive measurement of splanchnic rSO_2 in infants after cardiac surgery for congenital heart disease.[36]

The relationship between cerebral and somatic rSO_2 measured in cerebral, splanchnic, renal, and muscle has been compared with blood lactate levels measured in 23 children after repair of congenital heart disease.[11] Cerebral rSO_2 had the strongest inverse correlation with lactate level followed by splanchnic, renal, and muscle rSO_2, and an averaged cerebral and renal rSO_2 $\leq$65% predicted a lactate level $\geq$3.0 mmol litre^{-1} with a sensitivity of 95% and a specificity of 83%. Overall, it was felt that averaged cerebral and renal rSO_2 <65% as measured by NIRS predicts increased lactate in acyanotic children after congenital heart surgery and may facilitate the identification of global hypoperfusion caused by low cardiac output syndrome in this population.[11]

Somatic NIRS is also being investigated as an indicator of need for transfusion in trauma patients thought to be at high risk for haemorrhagic shock.[73] A minimum somatic rSO_2 <70% correlated with the need for blood transfusion with a sensitivity of 88% and a specificity of 78%, whereas the need for blood transfusion within 24 h of arrival was not predicted by hypotension, tachycardia, arterial lactate, base deficit, or haemoglobin. The authors concluded that somatic rSO_2 may represent an important screening tool for identifying trauma patients who require blood transfusion.[73]

Other

Since cerebral dysautoregulation can occur in head injury and in a variety of other conditions, the potential for cerebral NIRS to provide a reliable bedside non-invasive assessment of cerebral autoregulation is being actively investigated in a variety of clinical settings and may provide a further refinement in the assessment of risk of cerebral ischaemia.[55] Cerebral oximetry sensors have also been demonstrated to detect progressive spinal cord ischaemia after sequential intercostal artery ligation in a large animal swine study.[43] A recent preliminary clinical report has correlated changes in spinal cord perfusion during lumbar CSF drainage with changes in rSO_2 from cerebral oximetry sensors located over the lumbar spine area in a patient undergoing thoracic endovascular thoracoabdominal stenting.[54] Overall, these studies suggest an increasing role for cerebral and somatic oxygen saturation monitoring that, despite limitations,

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provides the only indication of compromised brain and tissue perfusion in a number of clinical settings. Against the ease of use and continuous nature of such NIRS monitoring must be considered the relative sensitivity and specificity of such devices *vs* other monitoring modalities.

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Enhancing Near-IR Avalanche Photodiodes Performance by Femtosecond Laser Microstructuring

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Abstract A processing technique using femtosecond laser pulses to microstructure the surface of a silicon avalanche photodiode (APD) has been used to enhance its near-infrared response. Experiments were performed to optimize the APD performance by varying the parameters of the structuring as well as the post-structuring processes. Following thermal annealing, we have been able to fabricate APD arrays with quantum efficiencies as high as 58% at 1064 nm without degradation to its noise or gain performance. Experimental results provide no evidence to suggest that the enhancement is a result of changes to the silicon band structure.

OCIS codes: (040.1240) array detectors; (040.5170) photodiodes;(040.3060) infrared detectors

1. Introduction

There is a wide range of interest for improving the responsivity of silicon in the near-infrared (near-IR) region of the electromagnetic spectrum. This is driven by the prevailing use of silicon throughout the semiconductor industries. However, while the use of silicon detectors is also popular for optoelectronic applications, their use in the telecommunications industry is limited because the bandgap of ordinary bulk silicon is ~ 1.12 eV.[1] This reduces the absorption and thus the photoresponse of silicon-based photodiodes at wavelengths beyond 1100 nm. In addition, the responsivity of these detectors to wavelengths near the silicon bandgap often fails to meet the industry's needs. The maturity of high power lasers near this bandgap makes them attractive for the development of rugged, long-range applications including free-space optical communications and LADAR. Detectors with higher responsivity in this range would help meet eye-safety requirements, allow a more compact package by reducing the laser power requirements and provide the enhanced sensitivity needed for many ranging or communication applications.[2-5]

To achieve enhanced near-IR response, fabrication of thick silicon photodiodes, including avalanche photodiodes (APDs) with internal gain can compensate for the longer penetration depth of the radiation.[6] However, as the volume of bulk material increases the detector noise also increases, limiting the advantage of a thicker detector. Reflective surfaces on the backside of the detector have also been fabricated with varying degrees of success but with increased processing challenges.[7] Optical anti-reflection coatings can also improve the overall response, but the best commercial detectors using one or more of these techniques still does not achieve

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quantum efficiencies above 40% at the common laser wavelength of 1064 nm. While other semiconductor materials, including indium gallium arsenide and germanium are used for near-IR detection, their higher noise characteristics, poor integration with existing silicon-based electronics and higher material cost have sustained the desire for improved responsivity in silicon.[8,9]

The last several years have seen the development of a surface structuring technique to enhance the absorption of radiation both below and above the bandgap of silicon.[10-13] Through the use of femtosecond or nanosecond lasers to form microstructures along the exposed silicon surface, absorption of silicon has been as high as 90% at wavelengths ranging from 250 to 2500 nm.[14] Further demonstrations of the absorption properties of bulk silicon and the effect of the laser microstructuring parameters have been reported in the literature.[15-18] Developmental work includes using the laser microstructuring to form a photodiode junction in an *n-type* silicon wafer, providing sensitivity to wavelengths up to 1600 nm.[19]

In this article we report on the laser microstructuring of a silicon-based APDs and APD arrays. Using a series of post-structuring fabrications steps including annealing, we have demonstrated responsivities 2 to 3 times greater than the unstructured APDs at near-IR wavelengths without degradation to the other performance characteristics.

2. Experimental Methods

We fabricate our APDs from *n-type* neutron transmutation doped silicon wafers (30 Ω·cm, 100-crystal orientation). Grooves are cut in the wafer with a diamond saw to define and isolate the individual pixel elements. This is followed by very deep diffusion in a high temperature diffusion furnace. Grinding and chemical etching steps are then used to create a p-n junction 40 to 60 μm below the device surface.[20,21]

The microstructuring was performed following the fabrication of the APD device structure. This process removed silicon from the surface of the wafer, creating numerous defect sites and changing the thickness of the APD surface layers. In order to achieve high APD gain, a reverse bias is applied, expanding the width of the depletion region towards the silicon anode surface. As the depletion region width reaches towards the detector anode surface boundary, charges from defect states near the surface have a greater probability of being collected. RMD's APDs have been carefully fabricated to achieve the highest gain without significantly increasing the leakage current until breakdown is reached.[22] We therefore attempted to minimize the volume of silicon removed to maintain the optimal thickness of each APD layer and limit any increase in the leakage current from surface change collection. Both APD arrays and single element APDs, with an active area of ~ 2 mm x 2 mm were used throughout these studies.

The laser microstructuring was done in vacuum using a Ti-sapphire laser at a wavelength of 800 nm, a pulse width of 100 fs and a repetition rate of 1 kHz. The irradiating beam was directed normal to the anode side of the APD wafer, which was translated to allow structuring of a surface area larger than the focal spot size of ~ 150 μm. The translation speed was adjusted so that any one region on the surface was exposed to a range of 10 to 400 laser pulses. To further evaluate the microstructuring process parameters, we also varied the laser fluence from 3 to 8 kJ/m^2. Formation of microstructures took place in atmospheres of SF_6, H_2S, N_2 and air at a

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