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S45	2	S36 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:25

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		H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.)				
S46	1	("20140138785").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:26
S47	3930	(257/432).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:54
S48	218	(257/228).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:54
S50	1	("9373732").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/07/13 15:10
S51	1	("9373732").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/07/15 10:13

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S49	1	(257/432).CCLS.		OR	OFF	2015/01/05 11:54

7/ 15/ 2016 1:44:41 PM
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SAMSUNG EX. 1002 - 3415/4148

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("20150372040").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/04/14 10:04
L2	20	("5101260" | "5600130" | "5626687" | "5635089" | "6082858" | "6204506" | "6907135" | "20030214595" | "20030228883" | "20050093100" | "20060086956" | "20060128087" | "20070189583" | "20070237504" | "20080158398" | "20080192133" | "20080284884" | "20090308457" | "20100200658" | "20110292380").PN.	US-PGPUB; USPAT	OR	ON	2017/04/14 10:18
L3	7750	H01L27/1463.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/14 10:19
L5	14058	H01L27/14627.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/14 10:19
L6	3241	H01L27/14629.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/14 10:20
L7	10559	H01L27/14685.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/14 10:20
L8	10261	H01L27/14625.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/14 10:20
L9	3375	H01L27/1462.CPC.	US-PGPUB; USPAT; USOCR;	OR	ON	2017/04/14 10:20

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			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L10	1616	H01L27/14607.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/14 10:20
L11	5668	H01L27/14645.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/14 10:20
L12	9763	H01L27/14689.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/14 10:20
S2	84	US-3035052-$.DID. OR US-20030029495-$.DID. OR US-20040222187-$.DID. OR US-20050127401-$.DID. OR US-20050227390-$.DID. OR US-20060011955-$.DID. OR US-20060079062-$.DID. OR US-20060118781-$.DID. OR US-20060180885-$.DID. OR US-20060231914-$.DID. OR US-20070145505-$.DID. OR US-20080026550-$.DID. OR US-20080036022-$.DID. OR US-20080044943-$.DID. OR US-20080076240-$.DID. OR US-20080099804-$.DID. OR US-20080178932-$.DID. OR US-20080258604-$.DID. OR US-20090065051-$.DID. OR US-20090142879-$.DID. OR US-20090160983-$.DID. OR US-20090194671-$.DID. OR US-20090200586-$.DID. OR US-20090213883-$.DID. OR US-3487223-$.DID. OR US-4277793-$.DID. OR US-4419533-$.DID. OR US-4493942-$.DID. OR US-4514582-$.DID. OR US-4536608-$.DID. OR US-4663188-$.DID. OR US-4829013-$.DID. OR US-5080725-$.DID. OR US-5081049-$.DID. OR US-5100478-$.DID. OR US-5114876-$.DID. OR US-5164324-$.DID. OR US-5322988-$.DID. OR US-5346850-$.DID. OR US-5597621-$.DID. OR US-5714404-$.DID. OR US-5731213-$.DID. OR US-5792280-$.DID. OR US-6147297-$.DID. OR US-6498336-$.DID. OR US-6580053-$.DID. OR US-6583936-$.DID. OR US-6667528-$.DID.	US-PGPUB; USPAT; USOCR; JPO; IBM_TDB	OR	ON	2014/06/25 14:14

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SAMSUNG EX. 1002 - 3417/4148

		OR US-6759262-$.DID. OR US-6800541-$.DID. OR US-7057256-$.DID. OR US-7091411-$.DID. OR US-7109517-$.DID. OR US-7247527-$.DID. OR US-7314832-$.DID. OR US-7354792-$.DID. OR US-7390689-$.DID. OR US-7442629-$.DID. OR US-7456452-$.DID. OR US-7482532-$.DID. OR US-7498650-$.DID. OR US-7504325-$.DID. OR US-7504702-$.DID. OR US-7511750-$.DID. OR US-7745901-$.DID. OR US-7781856-$.DID. OR US-7816220-$.DID. OR US-7847253-$.DID. OR US-7884439-$.DID. OR US-7884446-$.DID. OR US-8030726-$.DID. OR US-8058615-$.DID. OR US-8207051-$.DID. OR US-8476681-$.DID. OR US-3666484-$.DID. OR US-2030766-$.DID. OR JP-07173484-$.DID. OR JP-071734840721-$.DID. OR JP-2008187003-$.DID. OR JP-2011091128-$.DID. OR JP-2152226-$.DID. OR JP-63116421-$.DID. OR JP-9298308-$.DID. OR KR-20010061058-$.DID. OR KR-20100118864-$.DID. OR WO-2006086014-$.DID. OR WO-2009100023-$.DID. OR WO-2011035188-$.DID. OR WO-2011119618-$.DID.				
S3	7768	(light adj2 (trapping or trapped))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 14:16
S4	11	S2 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 14:16
S5	2251	(reflector or Bragg) and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:40
S6	14	(reflector or Bragg) and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:41
S7	888	(reflector or Bragg) near3 backside	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:55

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S8	51623	(reflector or Bragg) near3 (side or sidewall or edge or wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:55
S9	112640	pixel near5 (side or sidewall or edge or wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:56
S10	143	S7 same S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:56
S11	2	S9 same4 S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:56
S12	3	S9 and S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:57
S13	1	S12 not S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:57
S14	179	S7 same4 S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:58
S15	145	S14 and (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:59
S16	129	S14 same10 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2014/06/25 15:59

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SAMSUNG EX. 1002 - 3419/4148

			DERWENT; IBM_TDB			
S17	128	S14 same8 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:59
S18	1204	(reflector or Bragg) near5 backside	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S19	71202	(reflector or Bragg) near5 (side or sidewall or edge or wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S20	280	S18 same4 S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S21	195	S20 same4 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S22	7	S18 same2 S9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:10
S23	7	S22 same4 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:10
S24	217	S18 same S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:13
S25	0	(light adj2 sensitive adj2 pixel) same4 S24	US-PGPUB; USPAT; USOCR;	OR	ON	2014/06/25 16:14

SIONYX1403000034.0031

SAMSUNG EX. 1002 - 3420/4148

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S26	0	(light adj2 sensitive adj2 pixel) and S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:14
S27	14	pixel same4 S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:14
S28	7	S27 and index	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:18
S29	26925	(high adj2 index) near3 (layer or film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:48
S30	27823	(low adj2 index) near3 (layer or film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:48
S31	12802	S29 near10 S30	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:48
S32	1170	(reflector or Bragg) same S31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:49
S33	611	(reflector or Bragg) near10 S31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:49
S34	4200	S30 near5 ("between")	US-PGPUB;	OR	ON	2014/06/26

SIONYX1403000034.0032

SAMSUNG EX. 1002 - 3421/4148

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			12:49
S35	1972	S34 near10 S29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:50
S36	81	(reflector or Bragg) near10 S35	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:50
S37	188	S29 near5 (polysilicon or polycrystalline or poly or (amorphous adj2 silicon) or germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:53
S38	2500	S30 near5 (oxide or nitride or oxynitride or oxynitrides)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:53
S39	14	S37 near20 S38	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:53
S40	0	(reflector or Bragg) same S39	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:54
S41	0	S39 near20 ("between")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:54
S42	51	backside near6 (textured near2 (layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2014/06/26 13:12

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			IBM_TDB			
S43	10	S42 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:25
S44	5	S39 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:25
S45	2	S36 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:25

SIONYX1403000034.0034

SAMSUNG EX. 1002 - 3423/4148

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S46	1	("20140138785").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:26
S47	3930	(257/432).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:54
S48	218	(257/228).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:54
S50	1	("9373732").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/07/13 15:10
S51	1	("9373732").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/07/15 10:13
S52	395	reflective near3 (aluminum adj oxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/15 13:07

4/14/2017 10:21:32 AM
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SAMSUNG EX. 1002 - 3424/4148

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14747875	PRALLE ET AL.
	Examiner	Art Unit
	LONG PHAM	2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	04/17/2016	07/15/2016	04/14/2017						
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	2	÷	✓	=						
	3	÷	-							
	4	÷	✓	=						
	5	÷	✓	=						
	6	÷	✓	=						
	7	÷	-							
	8	÷	-							
	9	÷	O	-						
	10	÷	O	=						
	11	÷	-							
	12	÷	✓	=						
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	15	÷	-							
	16	÷	-							
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	19	÷	✓	=						
	20	÷	-							
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	36		O	=						
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	49			=						
	50			=						

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14747875	PRALLE ET AL.
	Examiner	Art Unit
	LONG PHAM	2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	04/17/2016	07/15/2016	04/14/2017						
	51			=						
	52			=						
	53			=						
	54			=						
	55			=						
	56			=						
	57			=						
	58			=						

To: docketingbn@pepperlaw.com,davisdr@pepperlaw.com,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 136549

Apr 27, 2017 03:31:11 AM

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The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

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Application	Document	Mailroom Date	Attorney Docket No.
14747875	NOA	04/27/2017	143705.05211
	1449	04/27/2017	143705.05211

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

PRINTER RUSH
(PTO ASSISTANCE)

Application: 14747875	Examiner: Pham	GAU: 2814
From: Nran Hem	Location: IDC	Creation Date: 05/10/2017

Week Date: 4/24/2017

DOC CODE	DOC DATE	MISCELLANEOUS
[ ] 1449		[ ] Continuing Data
[ ] IDS		[ ] Foreign Priority
[X] CLM	01/23/2017	[ ] Document Legibility
[X] IIFW/FWCLM	04/27/2017	[ ] Fees
[ ] SRFW		[ ] Petition (TC)
[ ] DRW		[ ] Other
[ ] OATH		
[ ] 312		
[ ] SPEC		

[RUSH] Message:

1. Claim 10 depends on itself.

2. Original claim 18 has been canceled per (CLM 01/23/2017), but is shown on claim index as renumbered claim 11 and listed on PTOL-37.

Thank you

[XRUSH] Response:

Initials: _____

Examiner: PUBS contact - James Leija, (703) 756-1197
NOTE: This form will be included as part of the official USPTO record with the response document coded as XRUSH.
REV: AUG 16

SIONYX1403000034.0039

SAMSUNG EX. 1002 - 3428/4148

PRINTER RUSH
(PTO ASSISTANCE)

Application: 14747875	Examiner: Pham	GAU: 2814
From: Nran Hem	Location: IDC	Creation Date: 05/10/2017

Week Date: 4/24/2017

DOC CODE	DOC DATE	MISCELLANEOUS
[ ] 1449		[ ] Continuing Data
[ ] IDS		[ ] Foreign Priority
[X] CLM	01/23/2017	[ ] Document Legibility
[X] IIFW/FWCLM	04/27/2017	[ ] Fees
[ ] SRFW		[ ] Petition (TC)
[ ] DRW		[ ] Other
[ ] OATH		
[ ] 312		
[ ] SPEC		

[RUSH] Message:

1. Claim 10 depends on itself.

2. Original claim 18 has been canceled per (CLM 01/23/2017), but is shown on claim index as renumbered claim 11 and listed on PTOL-37.

Thank you

[XRUSH] Response:

/L.P/ (05/15/2017)

Initials: _____

Examiner: PUBS contact - James Leija, (703) 756-1197
NOTE: This form will be included as part of the official USPTO record with the response document coded as XRUSH.
REV: AUG 16

SIONYX1403000034.0040

SAMSUNG EX. 1002 - 3429/4148

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14747875	PRALLE ET AL.
	Examiner	**Art Unit**
	LONG PHAM	2814

CPC						
Symbol					**Type**	**Version**
H01L		27	/	1463	F	2013-01-01
H01L		27	/	14627	I	2013-01-01
H01L		27	/	14629	I	2013-01-01
H01L		27	/	14685	I	2013-01-01
H01L		27	/	14625	I	2013-01-01
H01L		27	/	1462	I	2013-01-01
H01L		27	/	14607	I	2013-01-01
H01L		27	/	14645	I	2013-01-01
H01L		27	/	14689	I	2013-01-01
			/			
			/			
			/			
			/			
			/			
			/			

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	36	
/LONG PHAM/ Primary Examiner.Art Unit 2814	05/15/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3,6

SAMSUNG EX. 1002 - 3430/4148

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14747875	PRALLE ET AL.
	Examiner	Art Unit
	LONG PHAM	2814

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
		H	0	1	L	27 / 146 (2006.01.01)						
CROSS REFERENCE(S)												
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											

NONE (Assistant Examiner) (Date)	Total Claims Allowed: 36	
/LONG PHAM/ Primary Examiner.Art Unit 2814 05/15/2017 (Primary Examiner) (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3,6

SAMSUNG EX. 1002 - 3431/4148

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14747875	PRALLE ET AL.
	Examiner	**Art Unit**
	LONG PHAM	2814

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	39	33	55										
2	2	18	40	34	56										
3	4	19	41	35	57										
4	5	20	42	36	58										
5	6	21	43												
6	10	22	44												
7	12	23	45												
8	13	24	46												
9	14	25	47												
10	17	26	48												
11	19	27	49												
12	34	28	50												
13	35	29	51												
14	36	30	52												
15	37	31	53												
16	38	32	54												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	36	
/LONG PHAM/ Primary Examiner.Art Unit 2814	05/15/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3,6

SAMSUNG EX. 1002 - 3432/4148

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14747875	PRALLE ET AL.
	Examiner	Art Unit
	LONG PHAM	2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	04/17/2016	07/15/2016	04/14/2017						
	1	÷	✓	=						
	2	÷	✓	=						
	3	÷	-							
	4	÷	✓	=						
	5	÷	✓	=						
	6	÷	✓	=						
	7	÷	-							
	8	÷	-							
	9	÷	O	-						
	10	÷	O	=						
	11	÷	-							
	12	÷	✓	=						
	13	÷	✓	=						
	14	÷	✓	=						
	15	÷	-							
	16	÷	-							
	17	÷	✓	=						
	19	÷	✓	=						
	20	÷	-							
	34		O	=						
	35		O	=						
	36		O	=						
	37		✓	=						
	38		✓	=						
	39		✓	=						
	40		✓	=						
	41			=						
	42			=						
	43			=						
	44			=						
	45			=						
	46			=						
	47			=						
	48			=						
	49			=						
	50			=						

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14747875	PRALLE ET AL.
	Examiner	**Art Unit**
	LONG PHAM	2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	04/17/2016	07/15/2016	04/14/2017						
	51			=						
	52			=						
	53			=						
	54			=						
	55			=						
	56			=						
	57			=						
	58			=						

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/747,875	06/23/2015	Martin U. Pralle	143705.05211	1722

136549 7590 05/24/2017

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
05/24/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketingbn@pepperlaw.com
davisdr@pepperlaw.com

Corrected Notice of Allowability	**Application No.** 14/747,875	**Applicant(s)** PRALLE ET AL.	
	Examiner LONG PHAM	**Art Unit** 2814	**AIA (First Inventor to File) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-2, 4-6, 10, 12-14, 17, 19, and 34-58*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/LONG PHAM/
Primary Examiner, Art Unit 2814

The present application is being examined under the pre-AIA first to invent provisions.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In claim 10, line 1, after "of claim", delete "10", and inser6 –1--.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LONG PHAM whose telephone number is (571)272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The

fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

/LONG PHAM/
Primary Examiner, Art Unit 2814

SAMSUNG EX. 1002 - 3438/4148

To: docketingbn@pepperlaw.com,davisdr@pepperlaw.com,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 136549

May 24, 2017 03:35:01 AM

Dear PAIR Customer:

Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 136549 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

Disclaimer:
The list of documents shown below is provided as a courtesy and is not part of the official file wrapper. The content of the images shown in PAIR is the official record.

Application	Document	Mailroom Date	Attorney Docket No.
14747875	NOA	05/24/2017	143705.05211

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

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Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-14)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	14747875	Filing Date	2015-06-23	Docket Number (if applicable)	143705.05211	Art Unit	2814
First Named Inventor	Martin U. Pralle			Examiner Name	Long Pham		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, to any international application that does not comply with the requirements of 35 U.S.C. 371, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV.

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 500436

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

Applicant Signature

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-14)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Andrew W. Schultz/	Date (YYYY-MM-DD)	2017-07-26
Name	Andrew W. Schultz	Registration Number	66869

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Docket No.: 143705.05211

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Martin U. Pralle Application No.: 14/747,875 Filed: June 23, 2015 For: PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS	Confirmation No.: 1722 Art Unit: 2814 Examiner: Long Pham

VIA EFS-WEB
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Certificate of Mailing
I hereby certify that this correspondence is being electronically filed via EFS-Web to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

July 26, 2017 (Dated)
Electronic Signature: /Andrew W. Schultz/
Andrew Schultz, Reg. No. 66,869

INFORMATION DISCLOSURE STATEMENT (IDS) TRANSMITTAL LETTER

Dear Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SUB/1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed concurrent with the filing of a request for continued examination (37 CFR 1.97(b)(4)). A certification statement pursuant to 37 C.F.R. 1.97(e) is not submitted herewith.

In accordance with 37 CFR 1.98(a)(2)(ii), Applicant has not submitted copies of U.S. patents and U.S. patent applications. Applicant submits herewith copies of foreign patents and non-patent literature in accordance with 37 CFR 1.98(a)(2) and (d).

SAMSUNG EX. 1002 - 3443/4148

In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in § 1.56 (b).

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 50-0436, under Order No. 143705.05211.

Respectfully submitted,

Dated: July 26, 2017

Andrew W. Schultz, Reg. No. 66,869
Attorney for Applicants
Pepper Hamilton LLP
125 High Street
19th Floor, High Street Tower
Boston, MA 02210
Tel: (617) 204-5716
Fax: (617) 204-5150

#44877463 v1

SIONYX1403000034.0055

SAMSUNG EX. 1002 - 3444/4148

Substitute for Form 1449/PTO				Complete if Known	
				Application No.:	14747875
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date:	June 23, 2015
				First Named Inventor:	Martin U. Pralle
				Group Art Unit:	2814
(use as many sheets as necessary)				Examiner Name:	Long Pham
Sheet	1	of	2	Attorney Docket No.:	143705.05211

U. S. PATENT DOCUMENTS						
Examiner's Initials	**Cite No.**	**U.S. Patent Document** Number Kind Code (if known)	**Name of Patentee or Applicant of Cited Document**	**Date of Publication of Cited Document MM-DD-YYYY**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	
	A1	4886958	Merryman	12/12/1989		
	A2	5351446	Langsdorf	10/4/1994		
	A3	5641969	Cooke et al.	6/24/1997		
	A4	5727096	Ghirardi et al	3/10/1998		
	A5	6327022	Nishi	12/4/2001		
	A6	6331885	Nishi	12/18/2001		
	A7	6340281	Haraguchi	1/22/2002		
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	B1	CN101404307	Univ. Zhongshan	4/8/2009				

Examiner Signature		Date Considered	

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SAMSUNG EX. 1002 - 3445/4148

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application No.:	14747875
				Filing Date:	June 23, 2015
				First Named Inventor:	Martin U. Pralle
				Group Art Unit:	2814
(use as many sheets as necessary)				Examiner Name:	Long Pham
Sheet	2	of	2	Attorney Docket No.:	143705.05211

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	B18	WO 2014110484	Digimarc Corp.	7/17/2014				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
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Examiner Signature		Date Considered	

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Electronic Patent Application Fee Transmittal

Application Number:	14747875
Filing Date:	23-Jun-2015
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Filer:	Andrew W. Schultz/Jillian Stockel
Attorney Docket Number:	143705.05211

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
RCE- 1st Request	2801	1	600	600
		Total in USD ($)		**600**

Electronic Acknowledgement Receipt	
EFS ID:	29900513
Application Number:	14747875
International Application Number:	
Confirmation Number:	1722
Title of Invention:	Pixel Isolation Elements, Devices and Associated Methods
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	136549
Filer:	Andrew W. Schultz/Jillian Stockel
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Attorney Docket Number:	143705.05211
Receipt Date:	26-JUL-2017
Filing Date:	23-JUN-2015
Time Stamp:	17:41:24
Application Type:	Utility under 35 USC 111(a)

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Payment was successfully received in RAM	$600
RAM confirmation Number	072717INTEFSW17430600
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Foreign Reference	DE19838439.pdf	1680083 1bbd6553cd61e869de070de2645cd4308d79229f	no	9
Warnings:					
Information:					
2	Foreign Reference	EP2509107A1.pdf	1361527 7ce82ba536ff3d53d041387548 9e5475a614a1d7	no	39
Warnings:					
Information:					
3	Foreign Reference	JP2003258285A.pdf	2303631 8d3d6eb46904c0fa2755f292e2e52cb050a9f4c5	no	7
Warnings:					
Information:					
4	Foreign Reference	JPH07235658.pdf	1194297 5cd86a0973bcb28f8d14310778669d37079e8b32	no	20
Warnings:					
Information:					
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Warnings:					
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Warnings:					
Information:					
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Espacenet

Bibliographic data: DE19838439 (C1) — 2000-04-27

Vertically integrated thin film photodiode, for photodetector used e.g. in optical data storage and transmission, is produced by thinning and reflective coating of a photodiode substrate bonded to a temporary substrate

Inventor(s): BUCHNER REINHOLD [DE]; SAX MELANIE [DE] ± (BUCHNER, REINHOLD, ; SAX, MELANIE)

Applicant(s): FRAUNHOFER GES FORSCHUNG [DE] ± (FRAUNHOFER-GESELLSCHAFT ZUR FOERDERUNG DER ANGEWANDTEN FORSCHUNG E.V)

Classification: - **international:** ***H01L31/0216; H01L31/0232; H01L31/0236;*** (IPC1-7): H01L31/0232; H01L31/0236; H01L31/102
- **cooperative:** **H01L31/02161**; **H01L31/0232**; **H01L31/0236**; Y02E10/50

Application number: DE1998138439 19980824

Priority number (s): DE1998138439 19980824

Abstract of DE19838439 (C1)

Thin film photodiode production comprises thinning and reflective coating of a photodiode substrate (1) bonded to a temporary substrate prior to bonding to a third substrate. A thin film photodiode is produced by bonding the photodiode side of a first substrate (1) to a second substrate, thinning the first substrate to a few microns thickness, applying a reflective layer or layer sequence onto the first substrate, bonding the reflective side of the first substrate onto a third substrate and removing the second substrate.

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(56) Für die Beurteilung der Patentfähigkeit in Betracht gezogene Druckschriften:

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US 55 63 084 A

(54) Dünnfilmphotodiode und Verfahren zur Herstellung

(57) Die Erfindung betrifft Dünnfilmphotodioden und ein Verfahren zur Herstellung.
Bei dem Verfahren wird ein erstes Substrat, das auf einer ersten Seite eine Photodiode aufweist, bereitgestellt. Das erste Substrat wird mit einem zweiten Substrat verbunden, wobei die erste Seite zum zweiten Substrat gerichtet ist. Das erste Substrat wird dann von einer zweiten, der ersten gegenüberliegenden Seite, bis auf eine Dicke von wenigen Mikrometern gedünnt. Anschließend wird eine die zu detektierende Strahlung reflektierende Schicht oder Schichtfolge auf die zweite Seite des ersten Substrates aufgebracht. Schließlich werden das erste Substrat auf ein drittes Substrat aufgebracht und das zweite Substrat entfernt.
Durch die erfindungsgemäße reflektierende Schicht an der Unterseite der Photodiode wird die Strahlung umgelenkt und durchdringt erneut die optisch aktive Schicht der Photodiode, so daß der Wirkungsgrad von Dünnfilmphotodioden stark erhöht wird.

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Beschreibung

Die Erfindung betrifft ein Verfahren zur Herstellung einer Dünnfilmphotodiode mit hohem Wirkungsgrad.

Es gibt derzeit viele technische Systeme, bei denen optische Signale erfaßt und zur Weiterverarbeitung in elektrische Signale umgewandelt werden müssen. Beispiele hierfür sind die Anwendungsfelder (magneto-)optische Datenspeicherung, wie bei CD-, DVD- oder MO-Laufwerken, die optische Datenübertragung über Glasfasernetzwerke, sowie die Bereiche Bildverarbeitung, Mustererkennung und optische Spektroskopie. Zur Detektion der elektromagnetischen Strahlung werden bei diesen Systemen in der Regel Halbleiter-Photodioden als Photodetektoren verwendet, die je nach Anforderung als Einzeldiode, Diodenzeile oder Diodenarray angeordnet werden. Im Bereich der Bildverarbeitung kommen hierbei insbesondere zeilenweise oder flächig angeordnete Detektoren zum Einsatz.

Als Grundmaterial zur Herstellung von Photodioden wird ein Halbleitersubstrat, beispielsweise aus Silizium, Germanium, III-V- oder IV-VI-Verbindungen, verwendet. Beispiele für III-V-Halbleiter sind GaAs, GaP, InP, InAs, InSb, GaInAs oder InGaAsP, für IV-VI-Halbleiter PbSe, PbTe.

Die einfallende elektromagnetische Strahlung wird im Halbleitersubstrat absorbiert und erzeugt Ladungsträger, die schließlich einen Photostrom hervorrufen. Die Größe des Stromflusses hängt von der Beleuchtungsstärke der zu erfassenden Strahlung ab. Der detektierbare Wellenlängenbereich wird durch das verwendete Halbleiter-Grundmaterial bestimmt. Dieser liegt im Fall von Silizium bei ca. 200 nm bis 1100 nm, während er bei Germanium ca. 200 nm bis 1700 nm umfaßt.

Zwischen den beiden Elektroden der Photodiode wird eine Raumladungszone erzeugt, in deren elektrischem Feld die Trennung der generierten Ladungsträger erfolgt. Um einen hohen Wirkungsgrad der Photodiode zu erhalten, muß gewährleistet werden, daß ein möglichst großer Teil der Strahlung in die Diode eingekoppelt und weitgehend innerhalb der Raumladungszone absorbiert wird. Außerhalb der Raumladungszone erzeugte Ladungsträger rekombinieren überwiegend und tragen nicht zum Photostrom bei. Die Rekombinationsrate wird durch Störungen des Kristallgitters und Defekte, die auch durch Verunreinigungen hervorgerufen werden können, erhöht und ist insbesondere im Bereich der Oberfläche sehr hoch.

Die Strahlungseinkopplung in die Photodiode wird durch die Brechungsindizes des Halbleitermaterials, der Deckschicht über der Photodiode und der Umgebung bestimmt. Bei monochromatischer Strahlung treten außerdem Interferenzeffekte durch Reflexionen an Grenzflächen auf, die die Transmission beeinflussen. Durch geeignete Wahl der Deckschichten über der Photodiode können eine optische Vergütung realisiert und die Strahlungseinkopplung für eine Wellenlänge oder einen Wellenlängenbereich optimiert werden.

Die Intensität der einfallenden Strahlung nimmt gemäß dem Absorptionsgesetz exponentiell mit zunehmender Eindringtiefe ab. Die Absorption und damit die Eindringtiefe werden durch den Absorptionskoeffizienten bestimmt, der hauptsächlich vom Halbleitermaterial und dessen Dotierung, sowie von der Wellenlänge der Strahlung abhängt. Die Absorption steigt in der Regel mit sinkender Wellenlänge und zunehmender Dotierung an. Ebenso bewirken Kristallstörungen, wie sie in polykristallinem oder amorphem Material in starkem Maß vorliegen, ein Ansteigen der Strahlungsabsorption.

Die Weite der Raumladungszone hängt bei gegebener elektrischer Spannung im Wesentlichen von der Dotierung des Halbleiters ab und nimmt mit sinkendem Dotierungsniveau zu. Häufig werden daher sog. pin-Photodioden verwendet, die eine intrinsische Halbleiterschicht enthalten, die sehr niedrig dotiert ist. Damit können Raumladungszonen mit einer Ausdehnung von mehreren Mikrometern erzeugt werden.

Lag in der Vergangenheit der Schwerpunkt der Entwicklung bei der Fertigung von Einzelphotodioden, so macht die zunehmende Nachfrage nach Gesamtsystemlösungen die Herstellung von integrierten Systemen erforderlich, bei denen Detektoren mit der dazugehörenden Auswerteelektronik, die Verstärkungs-, Logik- oder Speicherelemente enthalten kann, integriert werden.

Neben der monolithischen Integration, bei der Detektoren und Elektronik nebeneinander auf einem Substrat erzeugt werden, gewinnt mittlerweile die vertikale Integration (siehe z. B. Y. Akasaka, Proc IEEE 74 (1986) 1703) bzw. die Herstellung von Dünnfilmelementen für Anwendungen, die mit dem Begriff "Smart Label" umschrieben werden, eine immer größere Bedeutung. Hierbei spielen auch die Kosten eine Rolle, da die monolithische Integration zum einen die Entwicklung von speziellen Fertigungsprozessen erfordert und insgesamt höhere Fertigungskosten verursacht. Zum anderen sind Photodioden im Vergleich zur Auswerteelektronik verhältnismäßig einfache Elemente, die in der Regel eine große Fläche beanspruchen. Bei der Integration fallen damit für die Photodioden wesentlich höhere Flächenkosten an, als bei der Fertigung im Rahmen eines einfachen Photodiodenprozesses. Für die genannten Anwendungsgebiete ist es erforderlich, Photodioden in dünnen Halbleiterfilmen mit Dicken von wenigen Mikrometern herzustellen.

Eine Problematik bei der vertikalen Integration ist die Herstellung von elektrischen Verbindungen zwischen den einzelnen Ebenen. Es sind jedoch Verfahren zur Herstellung von dreidimensionalen Schaltungsanordnungen bekannt, mit denen nach dem Aufbringen der Ebene elektrische Verbindungen hergestellt werden können (siehe z. B. US-A-5563084). Voraussetzung dafür ist jedoch in der Regel, daß die einzelnen Ebenen möglichst dünn sind, typischerweise wenige Mikrometer. Die Dicke wird dabei überwiegend durch die Verdrahtungsebenen (Mehrlagenmetallisierung) bestimmt, das Siliziumsubstrat wird in der Regel bis auf Restdicken von bis zu 0,5 µm gedünnt.

Andererseits beträgt die Eindringtiefe der Strahlung in Silizium bei einer Wellenlänge von 800 nm ca. 10 µm, während sie bei einer Wellenlänge von 500 nm, was einer Strahlung im blaugrünen Spektralbereich entspricht, nur noch ca. 1 µm groß ist. Dies bedeutet, daß in Dünnfilmphotodioden, besonders bei längerwelliger Strahlung, nur noch ein geringer Teil der einfallenden Strahlung absorbiert und in elektrische Signale umgesetzt wird.

Der Erfindung liegt daher die Aufgabe zugrunde, ein Verfahren zur Herstellung von Dünnfilmphotodioden anzugeben, die gerade bei längerwelliger Strahlung noch einen hohen Wirkungsgrad aufweisen.

Die Aufgabe wird mit dem Verfahren nach Anspruch 1 gelöst. Vorteilhafte Ausgestaltungen des Verfahrens sind Gegenstand der Unteransprüche.

Bei dem erfindungsgemäßen Verfahren werden zunächst ein oder mehrere Photodioden auf bekannte Weise vorzugsweise in einem Standard-Halbleitersubstrat hergestellt, wobei in der Regel ein reiner Photodiodenprozeß verwendet wird. Anschließend wird ein Trägersubstrat mit der Vorderseite des Halbleitersubstrats verbunden, die die Photodioden aufweist. Hierbei ist keine Justage erforderlich. Es genügt vielmehr eine grobe Ausrichtung der beiden Substrate. Nun wird das Halbleitersubstrat von der Rückseite her auf die geforderte Restdicke des Halbleiterbereiches von einigen Mikrometern gedünnt. Anschließend wird die Rückseite mit ei-

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ner oder mehreren Schichten versehen, die die zu detektierende Strahlung reflektieren, vorzugsweise mit einem Reflexionsgrad von mindestens 50%. Diese Schichten können Metalle (z. B. Al, Cu, Mo, Ta, Ti, W), Metallverbindungen (z. B. AlSi, AlSiCu, $MoSi_2$, $TaSi_2$, $TiSi_2$, PtSi, WSi_2) oder dielektrische Schichten wie Oxid oder Nitrid sein, die eine Totalreflexion der zu detektierenden Strahlung an der Grenzfläche zwischen dem Halbleiterbereich und diesen Schichten bewirken.

Vorzugsweise wird vor dem Aufbringen der reflektierenden Schichten die Oberfläche des Halbleiter-Substrates aufgerauht oder angeätzt (z. B. mit KOH), um eine diffuse Reflexion oder eine Änderung des Reflexionswinkels an dieser Fläche zu erzielen.

Wird die Photodiode so ausgelegt, daß sich die Raumladungszone über die gesamte Schichtdicke erstreckt, so tragen die in der gesamten Schichtdicke (optisch aktive Schicht) generierten Ladungsträger zum Photostrom bei. Infolge der Absorption nimmt die Strahlungsintensität exponentiell mit zunehmender Tiefe ab. Bei einer geringen Absorption würde jedoch ein Großteil der Strahlung die optisch aktive Schicht der Photodiode durchdringen und nicht zum Photostrom beitragen. Durch die erfindungsgemäße reflektierende Schicht an der Unterseite der Photodiode wird die Strahlung umgelenkt, durchdringt erneut die optisch aktive Schicht der Photodiode und erzeugt wiederum Ladungsträger. Bei senkrechtem Einfall des Lichtes wird damit mindestens eine Verdopplung der optisch wirksamen Tiefe erreicht. Durch die oben genannte Behandlung bzw. Strukturierung der Rückseite wird zusätzlich eine Richtungsänderung der Strahlung erreicht, so daß sich die Weglänge nochmals vergrößert. Darüber hinaus tritt auch an der Oberfläche der Photodiode beim Übergang vom optisch dichteren Halbleitermaterial in die Deckschichten, die in der Regel aus Oxid, Nitrid oder organischen Schichten, wie Polyimid, bestehen, eine Totalreflexion auf, so daß insgesamt der Wirkungsgrad von Dünnfilmphotodioden stark erhöht wird. Die erfindungsgemäße Rückseitenverspiegelung muß zur Erhöhung des Wirkungsgrades natürlich nicht unbedingt strukturiert werden.

Nach dem Aufbringen der reflektierenden Schicht bzw. Schichten wird die Photodiode auf ein weiteres Substrat aufgebracht. Nach dem Entfernen des Trägersubstrates werden schließlich die elektrischen Verbindungen hergestellt.

Die Rückseitenverspiegelung gewährleistet außerdem, daß die einfallende Strahlung nicht in darunterliegende Schichten einer vertikalen Integrierten Schaltung eindringt und die Eigenschaften der Schaltung beeinflußt. Eindringende Strahlung würde Ladungsträger erzeugen, die innerhalb einer Schaltung elektrische Ströme hervorrufen, die z. B. als unerwünschte Leckströme die Funktion des Bausteins stören können.

In einer vorteilhaften Ausführungsform wird die Rückseitenverspiegelung mit elektrisch leitenden Schichten realisiert und dient dadurch gleichzeitig als elektromagnetische Abschirmung, so daß ein Übersprechen zwischen den Ebenen verhindert wird.

Durch das erfindungsgemäße Verfahren können Dünnfilm-Photodetektoren geringer Dicke mit hohem Quantenwirkungsgrad hergestellt werden, die sich gut für eine vertikale Integration eignen.

Im folgenden wird die Erfindung anhand der Figuren und eines Ausführungsbeispiels näher erläutert. Hierbei zeigen

Fig. 1 ein Ausgangssubstrat mit einer auf übliche Weise hergestellten Photodiode;

Fig. 2 das gedünnte Ausgangssubstrat mit dem verbundenen Trägersubstrat auf der Vorderseite;

Fig. 3 das Trägersubstrat mit dem gedünnten Ausgangssubstrat nach Herstellung der Rückseitenverspiegelung;

Fig. 3a das Trägersubstrat mit dem gedünnten Ausgangssubstrat mit einer Rückseitenstreuschicht nach Herstellung der Rückseitenverspiegelung;

Fig. 3b das Trägersubstrat mit dem gedünnten Ausgangssubstrat mit lateralen Reflektoren nach Herstellung der Rückseitenverspiegelung; und

Fig. 4 ein Bauelementsubstrat mit vertikal integrierten Dünnfilm-Photodioden gemäß der vorliegenden Erfindung.

Das folgende Ausführungsbeispiel beschreibt die Herstellung einer Dünnfilm-Photodiode.

In einem Ausgangssubstrat **1**, beispielsweise aus monokristallinem Silizium, wird eine Photodiode **8** gemäß einem Standardverfahren der Halbleitertechnologie hergestellt. Solche Standardverfahren sind z. B. aus D. Widmann et al., Technologie hochintegrierter Schaltungen, Springer-Verlag, Berlin 1996, bekannt.

Die Diode besteht aus einem pn-Übergang von der hochdotierten Elektrode **3** zum Substrat **1**. Die Elektrode **3** ist dabei von entgegengesetzter Polarität wie das Substrat, d. h. bei einem n-leitenden Substrat p-dotiert. Das dotierte Gebiet **3** wird durch Ionenimplantation oder Diffusion erzeugt, wobei anschließend eine Temperung zum Eintreiben und/oder Aktivieren der Dotierstoffe folgen kann. Die Isolationsschicht **2**, die in der Regel aus Oxid besteht, kann dabei als Maskierung dienen. Alternativ ist selbstverständlich auch die Verwendung von Photolack zur Maskierung möglich.

Vor der Realisierung der elektrischen Anschlüsse wird eine Isolationsschicht **4** aufgebracht oder erzeugt, die aus undotiertem oder dotiertem Oxid, wie FSG, PSG, BSG oder BPSG, aus Nitrid oder einem Schichtsystem der genannten Materialien bestehen kann. Neben der Isolation gewährleistet diese Schicht auch einen Schutz der Photodiode. Anschließend wird die Metallisierung **5** hergestellt und eine Passivierungsschicht **6**, die beispielsweise aus Oxid und Nitrid besteht, abgeschieden. Das Ergebnis ist in **Fig.** 1 dargestellt.

Als Verdrahtung kann auch eine Mehrlagenmetallisierung zum Einsatz kommen. Die Deckschichten über der Photodiode können zur Optimierung der Strahlungseinkopplung in die Photodiode auch teilweise oder vollständig entfernt, bzw. modifiziert werden.

Für eine vertikale Integration muß das Substrat **1** auf eine Restdicke von wenigen Mikrometern, vorzugsweise auf ≤ 5 µm, gedünnt werden. Dazu wird ein Trägersubstrat **10**, das eventuell mit einer Abdeckschicht **11**, aus beispielsweise Oxid, versehen ist, auf das erste Substrat **1** aufgebracht, wie in **Fig.** 2 gezeigt. Als Trägersubstrat sind neben mono- oder polykristallinen Siliziumsubstraten auch andere Materialien verwendbar, die zu Halbleiterprozessen kompatibel sind, wie z. B. Quarz- oder Glassubstrate. Um eine gute Verbindung zu erreichen, wird dabei vorzugsweise die Oberfläche des Substrates **1** vorher planarisiert.

Die Planarisierung kann mit verschiedenen Verfahren durchgeführt werden. Dabei wird zuerst eine Isolationsschicht **7**, wie z. B. Spin-on-Glas oder ein CVD-Oxid aufgebracht. Die maximal mögliche Temperatur wird durch das zulässige Temperaturbudget, in der Regel durch die bei der Metallisierung verwendeten Materialien vorgegeben und liegt typischerweise im Bereich von 400°C. Anschließend wird die Oberfläche eingeebnet, was durch Rückätzen, mechanisches und/oder chemomechanisches Schleifen erfolgt. Nun wird auf die Oberfläche des Substrates **1** oder des Trägersubstrates **10** ganzflächig eine Haftschicht **12** aus einem organischen Material, wie Polyimid oder Photolack, aufgebracht. Diese Haftschicht **12** mit einer Dicke von typischerweise 1–2 µm bewirkt außerdem eine Planarisierung der Oberfläche. Auf die Haftschicht **12** wird schließlich das Trä-

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gersubstrat **10** aufgeklebt. Das Trägersubstrat **10** wird als Handlingsubstrat für die weiteren Prozeßschritte verwendet und schützt die Oberfläche des Substrates **1** bei der weiteren Bearbeitung.

Danach wird das Substrat **1**, das die Photodioden enthält, durch Ätzen und/oder Schleifen von der Rückseite her gedünnt, bis die Dicke des Substrates **1** nur noch wenige Mikrometer beträgt.

Dieser Dünnungsprozeß kann dadurch vereinfacht werden, daß als Ausgangsmaterial für das Substrat **1** SOI-Material verwendet wird, welches eine vergrabene Oxidschicht enthält. Dies hat den Vorteil, daß der Dünnungsprozeß so ausgelegt werden kann, daß diese vergrabene Oxidschicht als Ätzstopp dient. Aufgrund der großen Selektivität der Ätzprozesse wird damit eine hohe Homogenität der Dicke des gedünnten Substrates **1** erreicht. Die Enddicke des Substrates **1** wird dabei durch die Dicke der Substratschicht oberhalb des vergrabenen Oxides, das danach entfernt werden kann, bestimmt.

Eine weitere Alternative stellt die Verwendung einer hochdotierten Schicht als Ätzbarriere dar. In diesem Fall wäre die vergrabene Oxidschicht beim SOI-Material im Substrat **1** durch ein hochdotiertes Gebiet ersetzt. Durch den Einsatz von Ätzverfahren, deren Ätzraten stark dotierungsabhängig sind, wird schließlich erreicht, daß die Dünnung des Substrates **1** selbständig an dieser hochdotierten Schicht stoppt.

Nun wird die Rückseite des Substrates **1** gemäß **Fig. 3** mit einer Schicht oder einem Schichtsystem **13** versehen, das die zu detektierende Strahlung reflektiert. Diese Schichten können dabei Metalle (z. B. Al, Cu, Mo, Ta, Ti, W), Metallverbindungen (z. B. AlSi, AlSiCa, $MoSi_2$, $TaSi_2$, $TiSi_2$, PtSi, WSi_2) oder dielektrische Schichten wie Oxid oder Nitrid sein, die eine Totalreflexion der zu detektierenden Strahlung an der Grenzfläche zwischen den Schichten und dem Substrat bewirken. Durch elektrisch leitende Schichten kann außerdem ein Rückseitenkontakt zur Verfügung gestellt werden.

Vorzugsweise wird vor dem Aufbringen der reflektierenden Schichten die Oberfläche des Halbleiter-Substrates aufgerauht oder angeätzt, um eine diffuse Reflexion oder eine Änderung des Reflexionswinkels zu erzielen. Dieses Aufrauhen kann mechanisch und/oder chemisch erfolgen. Bei einer chemischen Behandlung kommen dabei Defektätzen oder Ätzen, deren Ätzrate von der Kristallorientierung abhängt, wie die KOH-Ätze, zur Anwendung. Alternativ oder zusätzlich können auch mit Hilfe einer Rückseitenlithographie, die hierzu keine Justierung erfordert, in Verbindung mit auf die Kristallorientierung sensitiven Ätzverfahren Schrägen bzw. Gräben **14** erzeugt werden. Durch diese Schrägen **14** werden mit der Rückseitenverspiegelung **13** die Richtung des reflektierten Lichtes geändert und damit Vielfachreflexionen im Substrat **1** hervorgerufen (vgl. **Fig. 3a**). Durch diese Maßnahme werden die optisch wirksame Substratdicke vervielfacht und der Wirkungsgrad der Photodiode stark erhöht. Für den Fall, daß die Schrägen **14** den später folgenden Verbindungsprozeß der vertikalen Integration stören, kann die Rückseite nach dem Erzeugen der Rückseitenverspiegelung **13** mit einem der bereits erwähnten Verfahren planarisiert werden.

Durch die Reflexionen kann jedoch auch eine Störung von benachbarten Elementen verursacht werden. Um dies zu verhindern, können zusätzlich Reflektoren **15** im Substrat **1** erzeugt werden, die das gedünnte Substrat **1** vorzugsweise durchdringen und damit einige Mikrometer tief sind (vgl. **Fig. 3b**). Die Reflektoren **15** können aus dielektrischen Schichten wie Oxid oder Nitrid bestehen. Weiterhin sind Schichtsysteme aus den genannten dielektrischen Schichten, polykristallinem Halbleitermaterial, Metallen oder Metallverbindungen möglich. Bei elektrisch leitfähigen Schichten ist dabei in der Regel eine seitliche Isolation zum Substrat **1** erforderlich, die durch dielektrische Schichten sichergestellt wird.

Ein Bauelementsubstrat **20**, welches elektronische Bauelemente **21** enthalten kann, wird als Grundsubstrat für die vertikale Integration verwendet. Nach Planarisierung der Oberfläche des Substrates **20** mit einem der bereits erwähnten Verfahren wird eine Haftschicht **22** aus z. B. Polyimid oder Photolack auf das Substrat **20** oder auf die Rückseite des Substrates **1** aufgebracht. Anschließend wird das Substrat **1**, welches die Photodioden enthält, justiert mit dem Bauelementsubstrat verbunden. Danach werden das Trägersubstrat **10**, die Abdeckschicht **11** und die Haftschicht **12** entfernt. Das resultierende System ist in **Fig. 4** dargestellt.

Das Trägersubstrat **10** und die Abdeckschicht **11** können durch Abätzen oder Abschleifen, die Haftschicht **12** mit einem Sauerstoffplasma oder einem Lösungsmittel abgetragen werden. Die Abdeckschicht **11** kann dabei als Stoppschicht für das Entfernen des Trägersubstrates **10** dienen.

Die Schichten **4**, **6** und **7** stellen gleichzeitig die Deckschichten über der Photodiode dar. Im Zuge einer Optimierung der Strahlungseinkopplung in die Photodiode kann bei Bedarf eine Modifikation dieser Schichten über den Photodioden durchgeführt werden. Dies kann durch ein lokales Dünnen, Entfernen und/oder Abschneiden erfolgen.

Die elektrische Verbindung zwischen den Photodioden und den Bauelementen **21** kann beim Aufbringen des Substrates **1** oder nach Entfernung des Trägersubstrates **10** mit einem bekannten Verfahren hergestellt werden.

Patentansprüche

1. Verfahren zur Herstellung von Dünnfilmphotodioden, mit folgenden Schritten:
   - Bereitstellen eines ersten Substrates (**1**) mit einer Photodiode auf einer ersten Seite;
   - Verbinden des ersten Substrates mit einem zweiten Substrat (**10**), wobei die erste Seite zum zweiten Substrat gerichtet ist;
   - Dünnen des ersten Substrates von einer zweiten, der ersten gegenüberliegenden Seite bis auf eine Dicke von wenigen Mikrometern;
   - Aufbringen einer die zu detektierende Strahlung reflektierende Schicht oder Schichtfolge (**13**) auf die zweite Seite des ersten Substrates;
   - Aufbringen des ersten Substrates auf ein drittes Substrat (**20**), wobei die reflektierende Schicht oder Schichtfolge zum dritten Substrat gerichtet ist; und
   - Entfernen des zweiten Substrates.
2. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß als erstes Substrat (**1**) ein Substrat aus Halbleitermaterial bereitgestellt wird, in dem die Photodiode aus unterschiedlich dotierten Bereichen gebildet ist.
3. Verfahren nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die reflektierende Schicht oder Schichtfolge (**13**) auf der dem ersten Substrat (**1**) zugewandten Seite strukturiert wird.
4. Verfahren nach Anspruch 3, dadurch gekennzeichnet, daß die Strukturierung durch Aufrauhen oder Anätzen der zweiten Seite des ersten Substrates (**1**) vor dem Aufbringen der reflektierenden Schicht oder Schichtfolge (**13**) erfolgt.
5. Verfahren nach Anspruch 3, dadurch gekennzeichnet, daß die Strukturierung durch Ätzen von Gräben (**14**) auf der zweiten Seite des ersten Substrates (**1**) vor

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dem Aufbringen der reflektierenden Schicht oder Schichtfolge (13) erfolgt.

6. Verfahren nach einem der Ansprüche 1 bis 5, dadurch gekennzeichnet, daß für die reflektierende Schicht oder Schichtfolge (13) elektrisch leitendes Material verwendet wird.

7. Verfahren nach einem der Ansprüche 1 bis 6, dadurch gekennzeichnet, daß das Dünnen des ersten Substrates (1) bis auf eine Dicke von maximal 5 Mikrometer erfolgt.

8. Verfahren nach einem der Ansprüche 1 bis 7, dadurch gekennzeichnet, daß als drittes Substrat (20) ein Substrat mit elektronischen Bauelementen (21) und/oder Metallisierungsebenen eingesetzt wird.

9. Verfahren nach einem der Ansprüche 1 bis 8, dadurch gekennzeichnet, daß auf dem ersten Substrat (1) mehrere Photodioden gebildet sind, wobei zwischen den Photodioden Gräben erzeugt und mit einem Material (15) zur Reflexion der zu detektierenden Strahlung gefüllt werden.

Hierzu 2 Seite(n) Zeichnungen

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- Leerseite -

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Veröffentlichungstag: 27. April 2000

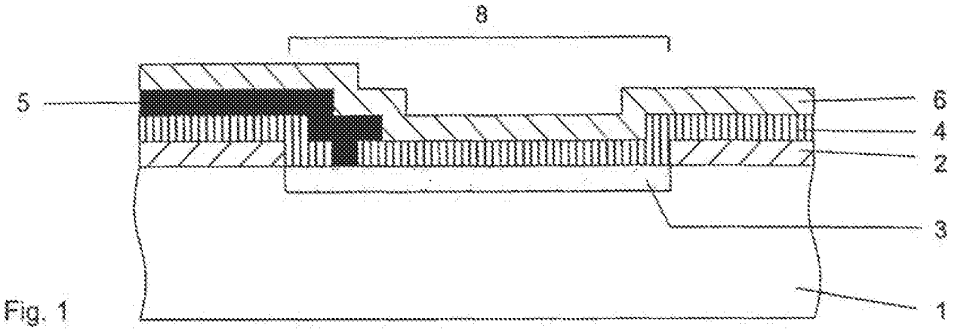

Fig. 1

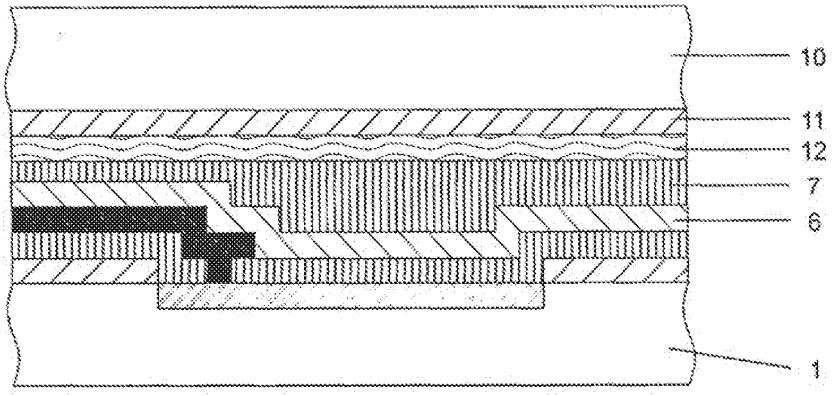

Fig. 2

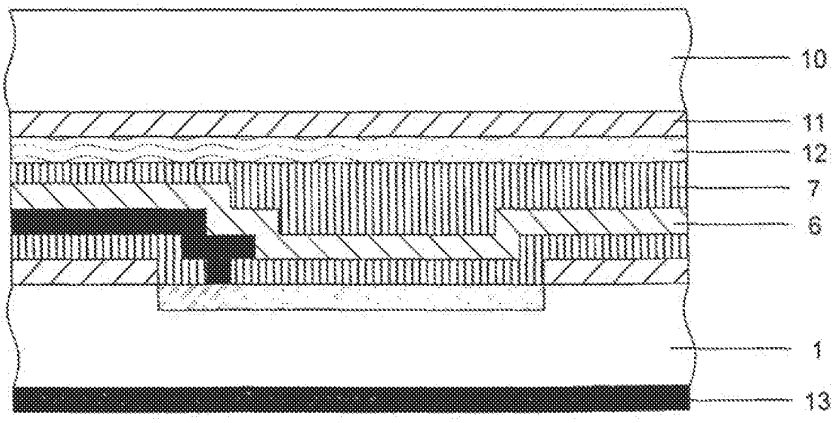

Fig. 3

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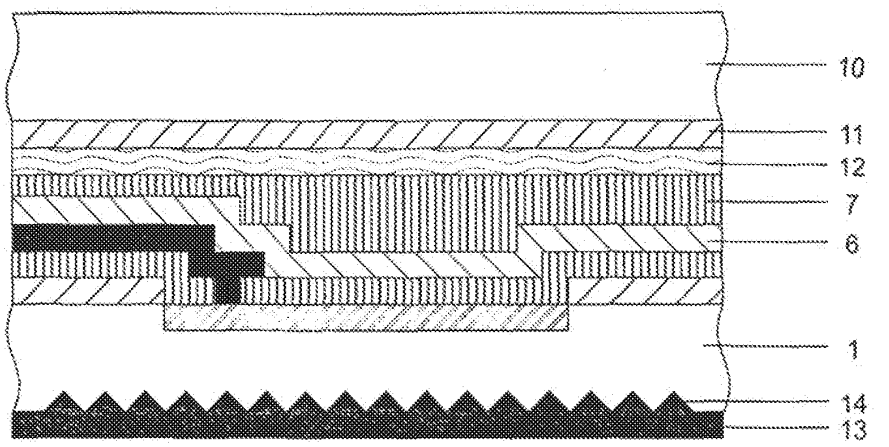

Fig. 3a

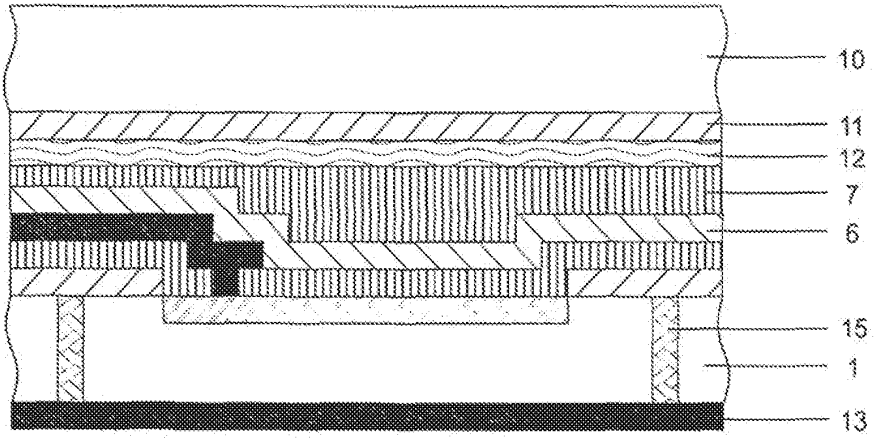

Fig. 3b

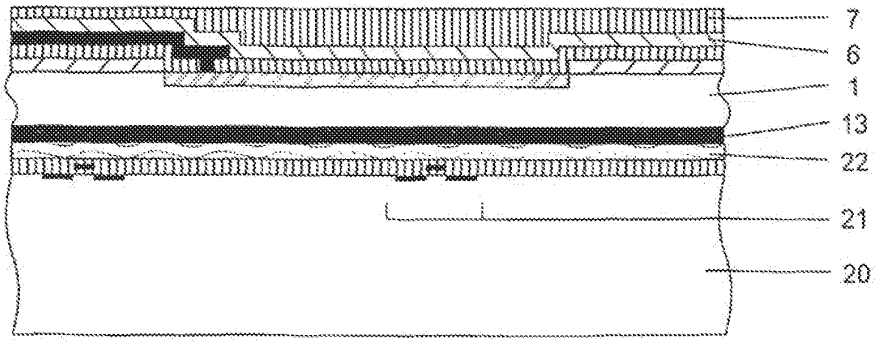

Fig. 4

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(54) **MULTISPECTRAL PHOTOSENSITIVE DEVICE**

(57) A multi-spectrum photosensitive device comprises two, three, or four composite sensing pixels arranged in layers up and down in a base layer of P-type or N-type silicon by means of single-sided processing or double-sided processing, each composite sensing pixels can sense respectively spectrum orthogonal or complementary to each other in visible light or visible and infrared light. The basic sensing pixels on different layers of the composite sensing pixels can be designed to sense different colors or spectrums, so that a multi-spectrum photosensitive chip can be achieved by repeatedly arranging the macro units consisting of more than one composite sensing pixel. The present disclosure also includes a new multi-layer sensing pixel, and examples of which used in a single-sided double-layer, or a double-sided double-layer, or a double-sided three-layer, or a double-sided four-layer, or a single-sided mixed double-layer, or a double-sided mixed with double-layer or a multi-layer multi-spectrum sensing device. A multi-spectrum photosensitive device according to the present disclosure has the advantage of better color sensing performance, integration of color sensing and infrared sensing, and a simple processing technique.

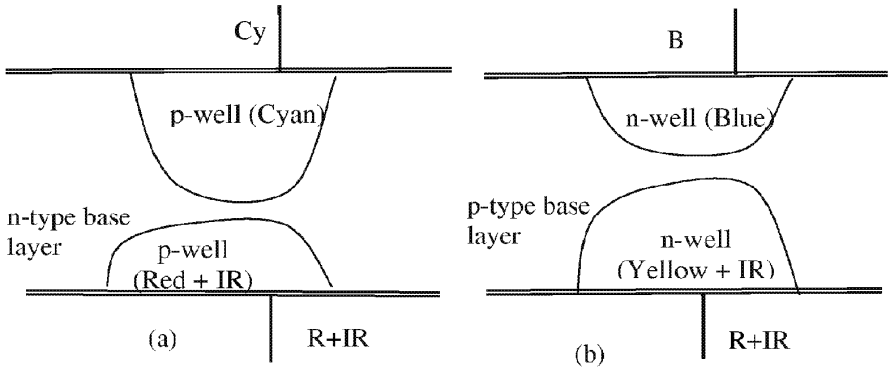

Fig 4

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Description

TECHNICAL FIELD

[0001] The present disclosure relates to a multi-spectrum photosensitive device, in particular, to physical implementation and manufacture thereof. More particularly, the present invention relates to a sensing device for panchromatic images which is achievable by CCD or CMOS semiconductor for simultaneously sensing several spectra (such as visible light and infrared). Herein, the panchromatic spectrum (or color) comprises the entire spectra of interest. For normal sensing devices (e.g., those for visible light), the panchromatic refers to the entire spectra of visible light that contains red, green, blue and white. For sensing devices used for a combination of infrared and visible light, the panchromatic refers to spectra of the visible light and infrared. The present disclosure applies to multi-spectrum sensing device for sensing infrared, monochrome and color images.

BACKGROUND ART

[0002] The present disclosure is a continuation of earlier applications titled "Multi-spectrum Photosensitive Device and Manufacturing Methods Thereof" (PCT/CN2007/071262) and "Multi-spectrum Photosensitive Device and Manufacturing Method Thereof" (Chinese Application No. 200810217270.2) owned by the present inventor, and aims to provide more specific and preferred semiconductor physical implementations.

[0003] The previous sensing devices focus on sensing either color visible light or infrared light, few of them sense both of color visible light and infrared light. Although there are other inventions or applications, such as using indium antimony semiconductor technology ("Silicon infrared focal plane arrays", M. Kimata, in Handbook of Infrared Detection Technologies, edited by M. Henini and M. Razeghi, pp.352-392, Elsevier Science Ltd., 2002), to simultaneously realize photosensitivity of visible light and infrared light, they do not sense color of light. The existing method of simultaneously obtaining the color and infrared light is to physically superpose a color sensing device with an infrared sensing device (such as "Backside-hybrid Photo detector for trans-chip detection of NIR light", by T. Tokudaetal., in IEEE Workshop on Charge-coupled Devices & Advanced Image Sensors, Elmau, Germany, May 2003, and "A CMOS image sensor with eye-safe detection function using backside carrier injection", T. Tokudaetal., J. Inst. Image Information & Television Eng., 60(3):366-372, March 2006).

[0004] There are three main reasons for failure of the existing sensing device in integrating the color sensing device with infrared sensing device. The first reason is that the existing color sensing device needs to use color filter film (including red / green / blue, or cyan /yellow / magenta / green) to get the color. However, these filter films also have a strong filtering characteristic on the infrared light. In addition, in order to make color vivid, an infrared filter is added to the lens specifically to reduce the possible fogging phenomenon caused by infrared light on color image. Foveon Company's X3 three-layer sensing technology achieves the selection of color according to the depth. Though this method does not use the filter film, the manufacture of the three-layer sensing technology has been very difficult and industrialization is not very successful. If an infrared layer is further added below the three layers, it will be more complicated and there is almost no practical value. The second reason is that silicon that is widely used in semiconductors absorbs the infrared with wavelength only below 1100 nm. Therefore, many infrared sensing devices utilize other semiconductor materials, such as germanium, silicon-germanium mixed crystals, HgCdTe, InSb and the like. These materials are not suitable for sensing visible light. The third reason is due to lack of practicable technology for manufacturing double-layer or multi-layer sensing device.

[0005] Therefore, some problems, such as how to achieve better photosensitivity and integrate the color sensing device with infrared sensing device, needs to be further invented and improved.

SUMMARY

TECHNICAL PROBLEM

[0006] Based on the above description, the present disclosure provides a multi-spectrum sensing device, which not only achieves color photosensitivity better, but also provides an implementation for integrating a color sensing device with an infrared sensing device.

TECHNICAL SOLUTION

[0007] The technical solution according to the present invention includes:

[0008] A multi-spectrum photosensitive device, comprising a base layer, wherein a plurality of composite sensing pixel macro units is repeatedly arranged in accordance with a preset pattern on the base layer, the composite sensing pixel macro unit comprises at least one composite sensing pixel comprising at least two basic sensing pixels, the basic sensing pixels are arranged in layers along a direction of light irradiation, each layer having one basic sensing pixel, and the basic sensing pixels are distributed at the top side, or bottom side, or top side and bottom side of the base layer in a manner of each side with at most two layers.

[0009] In an example of the multi-spectrum photosensitive device, the composite sensing pixel includes two basic sensing pixels, which are arranged in two layers at the top side or bottom side of the base layer to form a single-side double-layer composite sensing pixel, or are disposed respectively at the top side and bottom side of the base layer to form a double-sided double-layer com-

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posite sensing pixel.

[0010] In the multi-spectrum photosensitive device, the composite sensing pixel in the base layer may be a single-sided double-layer composite sensing pixel, so that the multi-spectrum sensing device constitutes a single-sided double-layer sensing device.

[0011] The single-sided double-layer composite sensing pixel may be formed by a composite N-P-N junction which is formed by doping P-type impurity on a base layer of N-type silicon to make a P-doped layer, then doping N-type impurity on P-doped layer.

[0012] The single-sided double-layer composite sensing pixel could be formed by a composite P-N-P junction, which is formed by doping N-type impurity on a base layer of P-type silicon to make an N-doped layer, then doping P-type impurity on the N-doped layer.

[0013] In the multi-spectrum photosensitive device, the composite sensing pixel in the base layer may be a double-sided double-layer composite sensing pixel, so that the multi-spectrum sensing device constitutes a double-sided double-layer sensing device.

[0014] The double-sided double-layer composite sensing pixel may be formed by a composite P-N-P junction which is formed by doping P-type impurity on both top side and bottom side of a base layer of N-type silicon.

[0015] The double-sided double-layer composite sensing pixel may be formed by a composite N-P-N junction which is obtained by doping N-type impurity on both top side and bottom side of a base layer of P-type silicon.

[0016] In an example of the multi-spectrum photosensitive device, the composite sensing pixel includes three or four basic sensing pixels, two of which are disposed in two layers at top side or bottom side of the base layer, and the remain basic sensing pixel(s) are disposed in one or two layers at bottom side or top side of the base layer, so as to form a double-sided multi-layer composite sensing pixel.

[0017] In the multi-spectrum photosensitive device, a composite sensing pixel in the base layer may be a double-sided multi-layer composite sensing pixel, so that the multi-spectrum sensing device constitutes a double-sided multi-layer sensing device.

[0018] The double-sided multi-layer composite sensing pixel may be formed by a composite junction of P-N-P, or N-P-N-P, or P-N-P-N, or N-P-N-P-N, wherein the composite junction is made by doping P-type impurity on both top side and bottom side of a base layer of N-type silicon to make a P-doped layer, and then doping N-type impurity on the P-doped layer.

[0019] The double-sided multi-layer composite sensing pixel may be formed by a composite junction of N-P-N, N-P-N-P, P-N-P-N or P-N-P-N-P, wherein the composite junction is made by doping N-type impurity on both top side and bottom side of a base layer of P-type silicon to make an N-doped layer, and then doping P-type impurity on the N-doped layer.

[0020] In the multi-spectrum photosensitive device, the basic sensing pixels in the composite sensing pixel respectively senses one of two spectrum bands of visible light or visible and infrared light orthogonal to each other, the combination of spectra sensed by all the composite sensing pixels in the composite sensing pixels macro units contains spectral information indispensable for color reconstruction within the color space of RGB or CMYK.

[0021] In the multi-spectrum photosensitive device, the spectrum sensed by the basic sensing pixels of the composite sensing pixels closest to the light source includes blank color, blue, green, cyan, white, and white plus infrared.

[0022] In the multi-spectrum photosensitive device, the spectrum sensed by basic sensing pixels of the composite sensing pixels farthest away from the light source includes blank color, green, red, yellow, white, red plus infrared, yellow plus infrared, and white plus infrared.

[0023] In the multi-spectrum photosensitive device, the bottom surface of the basic sensing pixel sensing infrared light in the bottom layer of the composite sensing pixel units is grown with silicon germanium crystal layer or germanium crystal layer for absorbing infrared light better.

[0024] In the multi-spectrum photosensitive device, the bottom of the basic sensing pixels for sensing infrared light is coated with a mirror reflection film.

[0025] In the multi-spectrum photosensitive device, the composite sensing pixel is sampled in an active manner to form an active pixel.

[0026] In the multi-spectrum photosensitive device, the composite sensing pixel is sampled in a passive manner to form a passive pixel.

[0027] In the multi-spectrum photosensitive device, the basic sensing pixel in the composite sensing pixels is a photo diode or a photo gate.

[0028] In the multi-spectrum photosensitive device, sensing mode of the multi-spectrum sensing device comprises front side sensing, back side sensing, or double-direction sensing mode, the double-direction sensing mode includes direction-selected-by-time-sharing mode, direction-selected-by-area-division mode, or direction-selected-by-pixel mode.

[0029] In the multi-spectrum photosensitive device, the preset pattern includes repeated ordering, rectangular pattern, or honeycomb pattern adopted by the composite pixels.

BENEFICIAL EFFECT

[0030] The beneficial technical effects of the present disclosure are designed to:

[0031] 1. A better color sensing performance is provided and a color sensing device is integrated with an infrared sensing device. In the present disclosure, at least two sensing pixel layers are provided in a direction of the light source irradiation in the form of composite sensing pixel containing at least two basic sensing pixels, the basic sensing pixels senses each spectral band of the

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spectrum at various layers, so that it is implemented that at least two spectral bands can be sensed at the same pixel position of one surface of the base layer but at different depths, so as to provide a better flexibility and a more pixel disposition on pattern arrangement of composite sensing pixel macro unit of the surface thereon, so that the sensibility, resolution and dynamic scope of the sensing device are greatly enhanced. On the other hand, when two sensing pixel layers are disposed as one sensing visible light and the other sensing infrared light, the integration of visible light device and infrared light device is realizable easily to sense color light and infrared light simultaneously.

[0032] 2. The processing technique implementing products is simple. By adopting existing CCD or CMOS sensing chip processing techniques and equipment, the present disclosure could easily manufacture a single-sided double-layer multi-spectrum sensing device, double-sided double-layer multi-spectrum sensing device and double-sided multi-spectrum sensing device for front side sensing, back side sensing or double-direction sensing. For the Foveon company's three-layer sensing device mentioned above, in order to carry out color sensing, it is necessary to dispose three layers at the same position to respectively sense three RGB colors so as to carry out color reconstruction. However, such method is difficult in processing three layers, and obviously makes wiring between transistors difficult, since connectors for different layers need to be separated from each other. Based on that, it is almost impossible for adding one more layer to the three RGB layers to perform infrared sensing. While the present disclosure carries out color reconstruction with pixel arranged in a pattern on the surface, so that it is unnecessary to dispose three layers in the direction of depth to implement color reconstruction, hence better color sensing performance is realized in the manner of dispose only two layers of basic sensing pixels on the same one surface. Since only two sensing pixel layers at most are disposed on the same surface, the difficulty of three-dimensional processing techniques is distinctly decreased, and wiring is relatively easy. Especially when a double-sided double-layer method is utilized, i.e. two basic sensing pixels in the composite sensing pixels are respectively disposed on two opposite sides, not only the single side double-layer method has better color sensing performance, but also each side processing is simplified as planar processing, that is, one sensing pixel layer is plane-processed on one side, then the base layer is turned over and the other sensing pixel layer is again plane-processed, so that the processing technique of double-sided double-layer sensing device is similar to that of current single-sided single-layer sensing device.

[0033] 3. Because the sensing device of the present disclosure carries out color reconstruction by combining depth spectrum filter and plane pattern arrangement, on one hand, it is unnecessary to adopt a color film, which greatly enhances production yield. On the other hand, redundant color information may be obtained so that many bad spots and dead spots could be compensated by background processing and the use of redundant color information. Accordingly, the fault occurrence ratio of the sensing device is decreased overall.

[0034] A plurality of the double-layer and multi-layer multi-spectrum sensing device suitable for sensing visible and infrared light according to embodiments of the present disclosure will be discussed, which are exemplary only for demonstrating the present disclosure, and are not intended to limit the protection scope of the present disclosure.

[0035] For those skilled in the art, the above and other purposes as well as advantages of the present disclosure will be apparent from the detailed description and illustration of preferred embodiments with reference to the drawings as shown below.

[0036] For the sake of simplicity, the following descriptions of drawings are mainly based on photo diode. However, almost all the examples may also use photo gate instead.

DESCRIPTIONS OF THE DRAWINGS

[0037] Figure 1 is a schematic diagram of traditional single-layer photo diode.

[0038] Figure 2 is a schematic diagram of a three-layer composite photo diode invented by Foveon Company, in which the diode at top layer senses blue, the diode at middle layer senses green, and the diode at bottom layer senses red. This manner makes full use of the relationship between light penetration depth and wavelength. From this figure we can imagine the difficulties of such kind of sensing device on pixel reading, for example, for the pixels of three distinct colors, the reading circuit will occupy a large space and the wiring will be difficult.

[0039] Figures 3 (a) and Figures 3 (b) are schematic diagrams of double-layer multi-spectrum sensing devices according to the present disclosure respectively. Figure 3(a) is suitable for illustrating a single-sided double-layer sensing device, and Figure 3(b) is suitable for illustrating a double-sided double-layer sensing device. The depths of T_1, T_2, T_3, and T_4 are determined in accordance with the relationship curve between incident depth and wavelength of light in the base material (silicon) (Gerald C. Holst and Terrance S. Lomheim, "CMOS/CCD Sensors and Camera Systems", JCD Publishing, pp. 125-125, ISBN 9780819467300, 2007). For example, if the photo diode at top layer is intended to sense blue (or cyan), T_1 should be chosen as about 1.5um (or about 4.5um); and if the bottom layer is intended to obtain red, T_2 and T_4 should be at least 8um, and T_3 should be at least 4.5um. If the photo diode at bottom layer is intended to obtain blue yellow, T_2 and T_4 should be at least 8um, and T_3 should be at least 1.5um. The photo diode at top layer and the bottom layer form a composite diode pair (composite sensing pixels). When the light is irradiated from the top, the photo diode at top layer is closer to the light source. When the light is irradiated from the bottom,

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the photo diode at bottom layer is closer to the light source.

[0040] Figure 4 (a) and Figure 4 (b) show a composite photo diode pair (composite sensing pixels) for sensing both the visible light and the infrared light simultaneously. In order to receive infrared light, the thickness of silicon substrate (T2 and T4 in Figure 3) can be thicker.

[0041] Figure 5 (a) and Figure 5 (b) are the situation of the composite photo diode pair in a single-layer sensing device being irradiated from the back side, in which the photo diode in Figure 5 (a) only senses visible light, and the photo diode in Figure 5 (b) senses both visible light and infrared light. In order to make the two composite photo diodes have a basically same thickness, germanium or silicon germanium crystal (SiGe), which can absorb infrared light better, can be grown at the back of the photo diode sensing the infrared light.

[0042] Figure 6 (a) and Figure 6 (b) are the situation of composite photo diode pair in a double-sided double-layer sensing device being irradiated from the front side, in which the photo diode in Figure 6 (a) only senses visible light, and the photo diode in Figure 6 (b) senses both visible light and infrared light. Similarly, in order to make the two composite photo diodes have a basically same thickness, germanium or silicon germanium crystal (SiGe), which can absorb infrared light better, can be grown at the back of the photo diode sensing the infrared light.

[0043] Figure 7 shows the situation of a composite photo diode in Figure 3 (a) with reading means. Due to the difficulty of wiring and sharing reading circuit, the single-sided double-layer sensing device is more suitably implemented with passive pixel (without FD and amplifying circuit).

[0044] Figure 8 shows the situation of composite photo diode in Figure 3 (b) with reading means. In contrast, when disposing reading circuit, the double-sided double-layer sensing device is easier and more flexible than the single-layer sensing device. Therefore, the double-sided double-layer sensing device can be achieved by either passive pixel, or active pixel. Furthermore, if it is achieved by active pixel, each pixel can be read with using only an average of 1.5 gates (utilizing 3T reading circuit), or 1.75 gates (utilizing 4T reading circuit).

[0045] Figure 9 shows a currently good reading circuit for a 4T active sensing pixel shared by 4-point, wherein one pixel utilizes 1.75 gates on average. We use it to explain that the double-layer or multi-layer sensing device according to the present disclosure could utilize the current standard reading and sampling circuit.

[0046] Figure 10 shows an example of a double-sided three-layer sensing device obtained by simply and directly applying a single-sided double-layer sensing device to bidirectional sensing, wherein the front side in Figure 10 (a) has one layer and the back side therein has two layers, while the front side in Figure 10 (b) has two layers and the back side therein has one layer. Such a sensing device with also three layers is easier and has more variations than Foveon Company's X3 three-layer sensing device. Take note to the difference between Figure 10 and Figure 2. The sensing pixels sensing three colors in Figure 2 are crowded on one side, while in Figure 10, there are only two pixels on one side and another pixel on the other side.

[0047] Figure 11 shows a double-sided four-layer sensing device generated by combining a single-sided double-layer sensing device and double-sided sensing mode. By using such a sensing device, four colors of blue, green, red and infrared may be sensed by one pixel. Although there are more colors and more layers, the manufacturing of the sensing device is much easier than that of Foveon Company's X3 three-layer sensing device.

[0048] Figure 12 shows examples of a double-sided multi-layer sensing device with mixing three layers and four layers.

[0049] Figure 13 shows examples of a double-sided multi-layer sensing device with mixing two layers and four layers.

[0050] Figure 14 shows examples of a double-sided multi-layer sensing device with mixing two layers and three layers.

[0051] Figure 15 and Figure 16 show examples of single-sided or double-sided double-layer sensing device with mixing two layers and one layer.

[0052] We see a degenerative case of a multi-layer composite sensing pixel in Figures 12-16: if one of the N-layer composite sensing pixels is a blank pixel, N-layer composite sensing pixels are degenerated to (N-1)-layer composite sensing pixels. Some double-layer sensing pixels degenerated to a single layer are shown in Figures 15 and 16. If two of the N-layer composite sensing pixels are blank pixels, N-layer composite sensing pixels are degenerated to (N-2)-layer composite sensing pixels, and so forth.

[0053] When the number of layers in the composite pixel is inconsistent, some of the layers may be treated as containing blank pixels (sensing blank color). Therefore, a mixed multi-layer sensing device is a specific case of a multi-layer sensing device, i.e. some of the composite pixels contain blank pixels.

[0054] These examples sufficiently demonstrate the capacity of a single-side double-layer sensing device and a double-sided double-layer or multi-layer sensing device. A series of new colorful sensing device with high performance is generated by combining the technologies of the two devices. It is specifically noted that, in a sensing device with more than three layers, the spectrum sensed by a photo diode positioned in each layer must be orthogonal to each other (that is, there is no common or overlapped portion, theoretically).

[0055] Figure 17 (a) and Figure 17 (b) shows a top view of a double-sided double-layer sensing device with rectangular pattern and honeycomb pattern, wherein FD is a reading capacitor shared by the upper layer and the lower layer. Of course, if needed, the upper layer and the lower layer could utilize a reading capacitor, respectively,

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even if using a group of reading capacitors, respectively.

[0056] Figure 18 (a) shows a top view of a double-sided double-layer multi-spectrum (sensing color plus infrared) sensing device with rectangular pattern, wherein FD is a reading capacitor shared by the upper layer and the lower layer. Figure 18 (b) shows a top view of a double-sided double-layer multi-spectrum (sensing color plus infrared) sensing device with rectangular pattern, wherein FD is a reading capacitor sharing the upper layer and the lower layer. Such kind of macro-pixel unit consisted of two composite pixels could also utilize active sensing pixels with 4-point sharing reading circuit as shown in Figure 9. Different from the single-side single-layer sensing device, the device in Figure 18 (a) adopts four sensing diodes sharing a reading circuit disposed on two sides.

[0057] Figure 19 shows a cross sectional view of 8-point or 4-point sharing reading circuit of a double-sided double-layer multi-spectrum (color plus infrared) sensing device (omitting 3T or 4T reading circuit). Here is an extreme case of FD which connects the upper layer and the lower layer. For a double-sided double-layer multi-spectrum (color plus infrared) sensing device, even if a 4-point sharing reading circuit also has two choices: one is that the 4 points are on the same surface, the other is that the 4 points are on different surfaces. In this diagram, we use another method to improve the absorbing efficiency of infrared light, i.e., mirror reflection materials (such as aluminum, silver or other reflection materials well matched with germanium or silicon) are coated at the back of the germanium layer and the silicon-germanium layer.

[0058] Figure 20 shows a cross section view of an 8-point or 4-point sharing reading circuit of the double-sided double-layer multi-spectrum (color plus infrared) sensing device (omitting 3T or 4T reading circuit). Here is a simpler case of FD not connecting upper layer and lower layer. When FD is not connecting the upper layer and lower layer, the top side or the bottom side of the double-sided double-layer multi-spectrum sensing device is the same as that of the single-sided single-layer sensing device.

[0059] Figure 21 shows a simple situation of producing the double-sided double-layer sensing device. When the base layer is opaque, the upper layer and lower layer can be achieved by a simple method of repeating the processing of the single-sided single-layer sensing device twice. The devices on both sides of the device can also be completely independent. This is a most simple method to achieve a double-direction sensing device.

[0060] Figure 22 (a) and Figure 22 (b) show a situation of a single-sided double-layer sensing devices being used for front side sensing and back side sensing, respectively. It is noted that, in the double-layer photo diode pairs, the photo diode closer to the light source will obtain color with shorter wavelength.

[0061] Figure 23 (a) and Figure 23 (b) show a situation of a double-sided double-layer sensing devices being used for front side sensing and back side sensing, respectively. It is noted that, when the direction of light source is changed, the color sensed by the double-layer photo diode pairs will changed, too. Generally, for two-way symmetrical double-sided double-layer sensing devices (referring to Chinese Application No. 200810217270.2, titled "Multi-spectrum sensing device and manufacturing method thereof"), when the direction of light source changes is changed, cyan and yellow will be exchanged, and blue and red will be exchanged, while green remains the same.

[0062] Figure 24 (a) and Figure 24 (b) show a situation of the front side and back side of a double-sided double-layer sensing device, in which macro pixel comprises three composite photo diodes (composite sensing pixels). When the macro pixel comprises three pixels, the three pixels are usually arranged in honeycomb pattern.

[0063] Figure 25, Figure 26, and Figure 27 are other possible implementations of a double-sided double-layer sensing device. These figures fully show the features of flexibility and diversity of a double-sided double-layer device. After a reasonable change, the discussions with respect to composite diodes in figures 3-16 are also applicable to the situation of figures 22-27. The small numbers of figures are just used to illustrate the principle, rather than limiting the essence and scope of the present disclosure.

[0064] Figure 28 is a principle schematic diagram of a photo gate. In the above illustration, if photo diode used as a basic sensing pixel is replaced by a photo gate, many completely similar implementations and conclusions can be obtained.

DETAILED DESCRIPTION

[0065] In order to facilitate describing the disclosure and explaining differences between the invention and existing technology, the following definition of the terms are provided: double-layer sensing device, multi-layer sensing device, double-sided sensing device, double-direction sensing device. The double-layer sensing device means that sensing pixels thereof are physically divided into two layers, each of which contains sensing pixels for sensing specific spectrum. The multi-layer sensing device refers to a sensing device with more than two layers, such as Foveon Company's X3 sensing device. The double-sided sensing device refers to a sensing device with two sensing surfaces, each of which can sense light from at least one direction. The bidirectional sensing device means that the sensing device can sense light from two directions (which usually form an angle of 180 degrees), i.e., both the front side and the back side of the sensing device can sense light.

[0066] A sensing device can simultaneously have one, two, or all of the following three characteristics: double-layer or multi-layer, double-sided, and double-direction. This disclosure mainly relates to a single-sided double-layer sensing device (as shown in Figure 22(a) and Figure 22(b)), a double-sided double-layer sensing device

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(as shown in Figure 23(a) and Figure 23(b)), and a double-sided multi-layer sensing device (as shown in Figures 10-14). Irrespective of a single-sided double-layer sensing device or a double-sided double-layer sensing device or a multi-layer sensing device, all of them can be used in front side sensing (as shown in Figure 22(a)), back side sensing (as shown in Figure 22(b)), or double-direction sensing (as shown in Figure 21 or Figure 23). However, designs of the sensing devices are different under different irradiation.

[0067] A multi-spectrum photosensitive device according to an embodiment of the present disclosure comprises a base layer, wherein a plural of composite sensing pixel macro units is repeatedly arranged in accordance with a preset pattern on the base layer, the composite sensing pixel macro unit comprises at least one composite sensing pixel consisting of at least two basic sensing pixels, the basic sensing pixels are arranged in layers along a direction of light irradiation, each layer having one basic sensing pixel, and the basic sensing pixels are distributed at the top side, or bottom side, or top side and bottom side of the base layer in a manner of single side with at most two layers. It is noted that, herein the terms "top side" and "bottom side" are just used to express the relative position of two sides of the base layers, rather than limiting the absolute physical location of the surfaces of the base layer. In the following description, to convey a similar definition, the positions with respect to the position of light source are also used to describe the terms "the obverse" (the front side) and "the reverse" (the back side) of the base layer.

[0068] Herein three terms are given: composite sensing pixel macro unit, composite sensing pixel, and basic sensing pixel. The basic sensing pixel is a sensing pixel on a layer and can not be divided. The composite sensing pixel is a combination of at least two basic sensing pixels. The basic sensing pixels in the composite sensing pixel are arranged in layers along a direction of light irradiation, and each layer is provided with one basic sensing pixel (the layer herein is called a sensing-pixel layer). As described in the aforementioned description of drawings, the basic sensing pixel can be a photo diode or a photo gate. When the basic sensing pixel is a photo diode, the composite sensing pixel is in a form of a composite sensing diode pair. Of course, it is noted that, each sensing-pixel layer in a composite sensing pixel is arranged along a direction of light irradiation (which is usually the normal direction of the sensing surface of the base layer), rather than limiting to just be arranged on a side of the base layer. Between the two opposite sides of the base layer irradiated by a light source, if taking the side closer to the light source as front side of the base layer and taking the side far away from the light source as back side of the base layer, each sensing-pixel layer in a composite sensing pixel can be arranged on front side of the base layer, or on back side of the base layer, or on both front side and back side of the base layer, but there are at most two layers of sensing pixels on each side. The relationship between the arrangement and quantity of the sensing-pixel layers can be summarized that, for a direction of a light source, the arrangement of the sensing-pixel layer may be [2,0], [0,2] (i.e., single-sided double-layer), or [1,1] (i.e., double-sided double-layer), or [1,2],[2,1] (i.e., double-sided multi-layer), wherein the first number in an array is the number of sensing-pixel layers arranged on front side of the base layer in the composite sensing pixel, and the second number is the number of the sensing-pixel layer arranged on back side of the base layer in the composite sensing pixel. The composite sensing pixel macro unit, also known as a macro-pixel, is a collection of the minimum number of composite sensing pixels, from which color reconstruction can be performed. A composite sensing pixel macro unit is repeatedly arranged in accordance with a preset pattern (such as square or honeycomb pattern, or repeated ordering), so that the color can be reconstructed throughout the image plane. For the double-layer multi-spectrum sensing device, the composite sensing pixel macro unit usually comprises at least two composite pixels. However, for a two-sided multi-layer multi-spectrum sensing device, the composite sensing pixel macro unit may be one composite pixel.

[0069] Since a composite pixel may be in various types, and a plurality of composite sensing pixels arranged on the base layer may be of different types, the sensing device according to the present disclosure may have a variety of flexible forms. For a composite sensing pixel, according to the number and distribution of the basic sensing pixel therein, the composite sensing pixel may be a single-sided double-layer composite sensing pixel, a double-sided double-layer composite sensing pixel, and a double-sided multi-layer composite sensing pixel. As mentioned above, in a single-sided double-layer composite sensing pixel or a double-sided double-layer composite sensing pixel, there are two basic sensing pixels, but the distribution therein are different. The basic sensing pixels in a single-sided double-layer composite sensing pixel are arranged in layers on one side of the base layer, while the basic sensing pixels of a double-sided double-layer composite sensing pixel are arranged on two sides of the base layer. For a double-sided multi-layer composite sensing pixel, there are three or four basic sensing pixels. Since at most two sensing-pixel layers are arranged on one side of the base layer, the basic sensing pixels therein must be arranged on two sides of the base layer, at least one side is provided with two basic sensing pixels arranged in layers. It is noted that, in a special case, the composite sensing pixel may comprise a blank pixel, in other words, the pixel is used for sensing blank color. In that case, if a basic sensing pixel in a single-sided double-layer composite sensing pixel is a blank pixel, the single-sided double-layer composite sensing pixel is equivalent to a single-sided single-layer composite sensing pixel from the perspective of sensing effectiveness.

[0070] Due to the various types, the arrangement of

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pixels in a composite sensing pixel is quite flexible. For example, if a single-sided double-layer composite sensing pixel is arranged at a certain position on the base layer, a double-sided double-layer composite sensing pixel may be arranged at a position adjacent to the said certain position, and the double-sided multi-layer composite sensing pixels may be arranged at another position adjacent to the said certain position. In short, different types of composite sensing pixels can be arranged at different positions on the base layer. In particular, according to this feature, when all the composite sensing pixels on the base layer in a sensing device are of the identical type, the sensing device is defined according to the type of the composite sensing pixels. For example, when all the composite sensing pixels of the base layer are the single-sided double-layer composite sensing pixels, the corresponding sensing device is regarded as a single-sided double-layer sensing device, and the sensing devices adopting the other two afore-mentioned composite sensing pixels are regarded as a double-sided double-layer sensing device or a double-sided multi-layer sensing device, respectively. It is noted that, as mentioned above, the composite sensing pixel may contain a blank pixel, thus the composite sensing pixel at a position of the base layer may be degenerated. For example, in a single-sided double-layer sensing device, if a composite sensing pixel comprises one blank pixel, the single-sided double-layer sensing pixel is actually degenerated as a single-sided single-layer sensing pixel, so that from the viewpoint of the details, a composite sensing pixel of a single-sided double-layer sensing device is not entirely a single-sided double-layer sensing pixel, but in a whole, this sensing device is still classified as a single-sided double-layer sensing device. Particularly, this sensing device can also be referred to as a mixed single-sided double-layer sensing device. Correspondingly, there exist also a mixed double-sided double-layer sensing device and a mixed double-sided multi-layer sensing device.

[0071] The basic sensing pixels of a composite sensing pixel are generally arranged to sense different spectral bands of visible light or visible and infrared light. For example, one of two spectral bands of visible light or visible and infrared light orthogonal to each other can be sensed respectively by two basic sensing pixel of the composite sensing pixel. Different spectral bands may be sensed respectively by the basic sensing pixels of the composite sensing pixel and composite sensing pixels of the composite sensing pixel macro unit, thus the combination of all spectra sensed by all composite sensing pixels of a composite sensing pixel macro unit contains the spectrum indispensable for color reconstruction within the color space of RGB or CMYK.

[0072] The spectra sensed by the basic sensing pixels closest to the light source in a composite sensing pixel includes blank color, blue, green, cyan, white, and white plus infrared. The spectra sensed by the basic sensing pixels farthest away from the light source in the composite sensing pixels includes blank color, green, red, yellow, white, red plus infrared, yellow plus infrared, and white plus infrared.

[0073] Hereto the arrangement of the sensing pixel according to the present disclosure has been described. Hereinafter, the processing implementation of a multi-spectrum sensing device according to the present disclosure will be described.

According to different materials of the base layer, an approach for achieving a single-sided double-layer multi-spectrum sensing device comprises:

[0074] Providing a base layer of N-type silicon crystal (see Figure 5 (a)), i.e. N-Substrate, at a location of a pixel on a side of the N-type base layer, P-type impurity is doped into the base layer at a certain depth from the surface of the location into the interior of the base layer according to the requirement of color depth, so as to form a P-doped layer. The P-doped layer is a sensing layer of a composite sensing pixel, that is, it forms a basic sensing pixel of the composite sensing pixel. Then, an N-type impurity is doped into the P-doped layer at another depth, which forms an N-doped layer within the P-doped layer, that is, it forms another basic sensing pixel in the composite sensing pixel. In the case, this single-sided double-layer composite sensing pixel is formed by a composite P-N-P junction.

[0075] Another approach is to provide a base layer of P-type silicon crystal (see Figure 5 (b)), i.e., P-substrate, at a location of a pixel on a side of the P-type base layer, N-type impurity is doped into the base layer at a certain depth from the surface of the location into the interior of the base layer according to the requirement of color depth, so as to form a N-doped layer. The N-doped layer is a sensing layer of a composite sensing pixel, that is, it forms a basic sensing pixel of the composite sensing pixel. Then, a P-type impurity is doped into the N-doped layer at another depth, which forms a P-doped layer within the N-doped layer, that is, it forms another basic sensing pixel in the composite sensing pixel. In this case, this single-sided double-layer composite sensing pixel is formed by a composite N-P-N junction.

[0076] The production of a composite sensing pixel is described above. For the production of other composite sensing pixels on the sensing side of the base layer, the processing thereof is the same. But the depths doped by impurities are different at different locations of pixels according to the wavelength of color spectrum desired to be sensed by the corresponding pixel.

[0077] An implementation of a double-sided double-layer multi-spectrum sensing device comprises:

[0078] providing a base layer of N-type silicon crystal (see Figure 4 (a)), i.e., N-substrate, classifying the pixels on the front side of the base layer according to the desired color, and doping P impurity with a certain depth according to the requirement of color depth for each type of pixel. Similarly, the pixels on the back side will also be classified according to the desired color, and P impurity with a certain depth is doped according to the require-

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ment of color depth for each type of pixel. The depth of the P impurity doped is determined according to the wavelength of spectrum desired to be sensed.

[0079] Another more advantageous approach is to provide a P-type base layer of silicon crystal (see Figure 4 (b)), i.e., P-substrate, classify the pixels on the front side according to the desired color, and dope N impurity with a certain depth according to the requirement of color depth for each type of pixel. Similarly, the pixels on the back side will also be classified according to the desired color, and N impurity with a certain depth is doped according to the requirement of color depth for each type of pixel. The depth of the N impurity doped is determined according to the wavelength of spectrum desired to be sensed. Since the mobility of N-type is better than that of P-type, the double-sided double-layer composite sensing pixel formed by this N-P-N composite junction is superior to the double-sided double-layer composite sensing pixel formed by the afore-described P-N-P composite junction.

[0080] An implementation of a double-sided multi-layer multi-spectrum sensing device comprises:

[0081] providing a base layer of N-type or P-type silicon crystal (Figure 9-14), making the front side of the base layer as one or two sensing pixel layers in the manner of single-sided double-layer or single-sided, and making the back side as one or two sensing pixel layers in the manner of single-sided double-layer or single-sided. According to the differences between the arrangement of the front side and the back side, a composite junction of a double-sided multi-layer composite sensing pixel comprising N-P-N, P-N-P, N-P-N-P, P-N-P-N, N-P-N-P-N, P-N-P-N-P and the like is formed.

[0082] After obtaining the composite sensing pixel, if it is needed to read the optical signal, a reading circuit and other control circuits are needed. The arrangement of the reading circuit and other control circuits is designed in accordance with passive pixel or active pixel. If it is designed with active pixel, in addition to the photo diode in Figure 3 (a), there will be a reading circuit shown in Figure 7, and many standard timing and control circuits (not shown in figures).

[0083] For the sensing pixel layer used to sense infrared light, germanium or silicon germanium crystal layer may grow on the bottom side of the corresponding position of the sensing pixel layer, that is the bottom side of the sensing pixel layer used to sensing the infrared light, in order to improve the absorption efficiency of the infrared spectrum. In addition, after growing the germanium or silicon germanium crystal layer, a mirror reflection film formed by aluminum, silver or other materials is plated on the bottom of the basic sensing pixel, in order to reflect the unabsorbed infrared photons, which are re-absorbed by infrared sensing pixel layer. The reflected intensity is determined according to the thickness and the absorption rate of the infrared sensing pixel layer, so as to avoid unnecessary interference with other pixels.

[0084] If the multi-spectrum sensing device is used for double-direction sensing, and the direction-selected-by-pixel pattern and the direction-selected-by-area-division pattern described in the patent application titled "Multi-spectrum sensing devices and manufacturing methods thereof" (China Application No. 200810217270.2, i.e., PCT/CN2010/073441) are used, a shading film is coated on some types of pixels or pixel areas of the front side, and on the other types of pixels or pixel areas of the back side.

[0085] In the above-mentioned implementation, we can completely use photo gate to replace photo diode, resulting in obtaining a single-sided double-layer sensing device, a double-sided double-layer sensing device, and a double-sided multi-layer sensing device, which are based on the photo gate.

[0086] Since the single-sided double-layer sensing device, the double-sided double-layer sensing device, and the double-sided multi-layer sensing device according to the present disclosure provide redundant color information, for the application to which the cost and size are critical (such as mobile phone), some composite pixels may contain blank pixel, resulting in a mixed single-sided double-layer sensing device, a mixed double-sided double-layer sensing device, and a mixed double-sided multi-layer sensing device.

[0087] The present disclosure can be produced by both CCD technology and CMOS technology. Since the production of the disclosure may be ultra-high sensitivity, the basic pixel can be read by means of passive pixel, or by means of active pixel. These features make the present disclosure integrated fully with the existing mature semiconductor chip production technology, therefore, the methods or production according to the present disclosure can be widely used. The disclosure dramatically improves the performance and functionality of sensing chip, at the same time, due to the increased product yields, the cost can be reduced or at least not increased.

[0088] By means of arranging optimally the basic sensing pixel in the composite sensing pixel on two depths, and forming various types of the sensing devices, such as single-sided double-layer, double-sided double-layer, and double-sided multi-layer, the present disclosure greatly extends the types of sensing chips, and physically realizes overlap and integration of the infrared sensing and the color sensing on a single chip for the first time.

[0089] In accordance with production methods provided by the present disclosure and natural and minor modifications thereof (such as, adding a filter film), a double-layer or multi-layer composite sensing pixel, which can sense spectrum orthogonal to each other within the space of visible light or visible plus infrared light, such as (blank color, white), (blue, yellow), (blue, green), (green, red), (blue, red), (blue, red + infrared), (blue, yellow + IR), (blank color, white + IR), (white + IR), (blue / green / red / green / yellow / white, infrared) and the like, can be achieved in the form of single-sided double-layer, double-sided double-layer, or double-sided multi-layer.

[0090] By using the aforementioned sensing methods

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such as double-sided, double-direction, double-layer and multi-layer methods, according to the present disclosure, a single sensing device can be used in a double-direction system, for greatly reducing system cost, lowering the size, reducing system complexity, and making it possible for some applications to receive multi-spectrum or multi-direction (or multi-spectrum signals from two directions) in the same system. For example, a capsule-style camera currently used for checking the patient's gastrointestinal system has a camera mounted on just one side thereof. In order to obtain the image of a certain location in the gastrointestinal system, multiple uses may be required, which cause great pain to the patient and the big expenses. For this purpose, it is desired to improve the capture range of a single shot. And if it is necessary to mount a camera on the other side of the capsule-style camera, by using the existing technology, two systems must be mounted in a very small space, which is quite difficult. However, by using the present invention, it just needs to add a lens on the other side, and still only one sensing chip is utilized, leading to smaller space demand and lower economic cost than those of two sets of sensing systems. In addition, the present disclosure can be used to monitor both front and back direction in a monitoring camera. For many 3G mobile phones with both front camera and back camera, the front camera and back camera can be replaced by a bidirectional camera according to the present disclosure, and switching between front sense and back scene can be achieved by electronic or mechanical switches. For some surveillance system of top class hotels, if it is required to monitor scenes at both ends of the corridor, by using the present disclosure, it just needs one monitoring system to complete the necessary monitoring rather than two monitoring systems for monitoring in both directions.

[0091] According to the integration method provided by the present disclosure, color and infrared can be sensed simultaneously in the same device (using CMOS or CCD semiconductor), and color image and infrared image are overlaid in the same space position. This new type of sensing device greatly extends the dynamic range of sensing device, so as to meet the high performance of automotive, security and other fields. Moreover, it will also be used for a small-size color sensing device such as the camera of mobile phones, to significantly improve image quality.

[0092] Although the present disclosure is disclosed through the above-mentioned preferred embodiments, such disclosure should not be considered limitations to the disclosure. For those skilled in the image sensing devices (such as semiconductor image sensor chips), from the disclosure, it is possible to anticipate many variations and extensions of the present disclosure, without departing from the spirit and concept of the invention.

Claims

1. A multi-spectrum photosensitive device, comprising a base layer, wherein a plurality of composite sensing pixel macro units is repeatedly arranged in accordance with a preset pattern on the base layer, the composite sensing pixel macro unit comprises at least one composite sensing pixel comprising at least two basic sensing pixels, the basic sensing pixels in a same composite sensing pixel are arranged in layers along a direction of light irradiation, each layer having one basic sensing pixel, and the basic sensing pixels are distributed at the top side, or bottom side, or top side and bottom side of the base layer, and each side comprises at most two layers.

2. The multi-spectrum photosensitive device according to claim 1, wherein the composite sensing pixel includes two basic sensing pixels which are arranged in two layers at the top side or bottom side of the base layer to form a single-sided double-layer composite sensing pixel, or are disposed respectively at the top side and bottom side of the base layer to form a double-sided double-layer composite sensing pixel.

3. The multi-spectrum photosensitive device according to claim 2, wherein the composite sensing pixel in the base layer is a single-sided double-layer composite sensing pixel, so that the multi-spectrum sensing device constitutes a single-sided double-layer sensing device.

4. The multi-spectrum photosensitive device according to claim 2 or 3, wherein the single-sided double-layer composite sensing pixel is formed by a composite N-P-N junction which is formed by doping P-type impurity on a base layer of an N-type silicon to make a P-doped layer, then doping N-type impurity on P-doped layer.

5. The multi-spectrum photosensitive device according to claim 2 or 3, wherein the single-sided double-layer composite sensing pixel is formed by a composite P-N-P junction which is formed by doping N-type impurity on a base layer of P-type silicon to make an N-doped layer, then doping P-type impurity on the N-doped layer.

6. The multi-spectrum photosensitive device according to claim 2, wherein the composite sensing pixel in the base layer is a double-sided double-layer composite sensing pixel, so that the multi-spectrum sensing device constitutes a double-sided double-layer sensing device.

7. The multi-spectrum photosensitive device according to claim 2 or 6, wherein the double-sided double-

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layer composite sensing pixel is formed by a composite P-N-P junction which is formed by doping P-type impurity on both top side and bottom side of a base layer of N-type silicon.

8. The multi-spectrum photosensitive device according to claim 2 or 6, wherein the double-sided double-layer composite sensing pixel is formed by a composite N-P-N junction which is obtained by doping N-type impurity on both top side and bottom side of a base layer of P-type silicon.

9. The multi-spectrum photosensitive device according to claim 1, wherein the composite sensing pixel includes three or four basic sensing pixels, two of which are disposed in two layers at top side or bottom side of the base layer, and the remain basic sensing pixel(s) are disposed in one or two layers at bottom side or top side of the base layer, so as to form a double-sided multi-layer composite sensing pixel.

10. The multi-spectrum photosensitive device according to claim 9, wherein the composite sensing pixel in the base layer is a double-sided multi-layer composite sensing pixel, so that the multi-spectrum sensing device constitutes a double-sided multi-layer sensing device.

11. The multi-spectrum photosensitive device according to claim 9 or 10, wherein the double-sided multi-layer composite sensing pixel is formed by a composite junction of P-N-P, or N-P-N-P, or P-N-P-N, or N-P-N-P-N, wherein the composite junction is made by doping P-type impurity on both top side and bottom side of a base layer of N-type silicon to make a P-doped layer, then doping N-type impurity on the P-doped layer.

12. The multi-spectrum photosensitive device according to claim 9 or 10, wherein the double-sided multi-layer composite sensing pixel is formed by a composite junction of N-P-N, or N-P-N-P, or P-N-P-N, or P-N-P-N-P, wherein the composite junction is made by doping N-type impurity on both top side and bottom side of a base layer of P-type silicon to make an N-doped layer, then doping P-type impurity on the N-doped layer.

13. The multi-spectrum photosensitive device according to claim 1, wherein the spectral bands sensed by the basic sensing pixels in a same composite sensing pixels respectively are orthogonal to each other, the spectral bands contains spectra of visible light or visible and infrared light, the combination of spectra sensed by all the composite sensing pixels in the composite sensing pixels macro units contains spectral information indispensable for color reconstruction within the color space of RGB or CMYK.

14. The multi-spectrum photosensitive device according to any one of claims 1-13, wherein the spectrum sensed by the basic sensing pixels of the composite sensing pixels closest to the light source includes blank color, blue, green, cyan, white, and white plus infrared.

15. The multi-spectrum photosensitive device according to any one of claims 1-14, wherein the spectrum sensed by the basic sensing pixels of the composite sensing pixels farthest away from the light source includes blank color, green, red, yellow, white, red plus infrared, yellow plus infrared, and white plus infrared.

16. The multi-spectrum photosensitive device according to any one of claims 1-15, wherein the bottom surface of the basic sensing pixel sensing infrared light in the bottom layer of the composite sensing pixel units grows with silicon germanium crystal layer or germanium crystal layer for absorbing infrared light better.

17. The multi-spectrum photosensitive device according to any one of claims 1-16, wherein the bottom of the basic sensing pixels for sensing infrared light is coated with a mirror reflection film.

18. The multi-spectrum photosensitive device according to any one of claims 1-17, wherein the composite sensing pixel is sampled in an active manner to form an active pixel.

19. The multi-spectrum photosensitive device according to any one of claims 1-17, wherein the composite sensing pixel is sampled in a passive manner to form a passive pixel.

20. The multi-spectrum photosensitive device according to any one of claims 1-19, wherein the basic sensing pixel in the composite sensing pixels is a photo diode or a photo gate.

21. The multi-spectrum photosensitive device according to any one of claims 1-20, wherein the sensing mode of the multi-spectrum sensing device comprises front side sensing, back side sensing, or double-direction sensing mode, wherein the double-direction sensing mode includes direction-selected-by-time-sharing mode, direction-selected-by-area-division mode, or direction-selected-by-pixel mode.

22. The multi-spectrum photosensitive device according to any one of claims 1-21, wherein the preset pattern includes repeated ordering, rectangular pattern, or honeycomb pattern adopted by the composite pixels.

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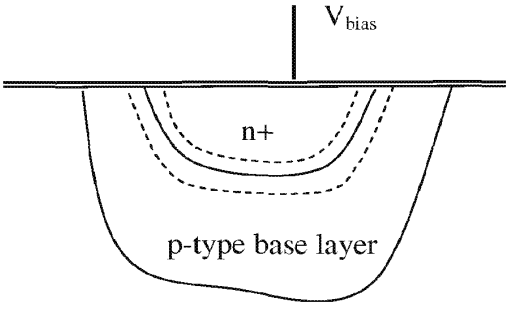

Fig 1

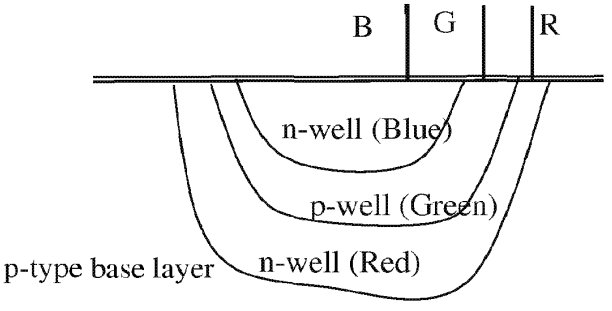

Fig 2

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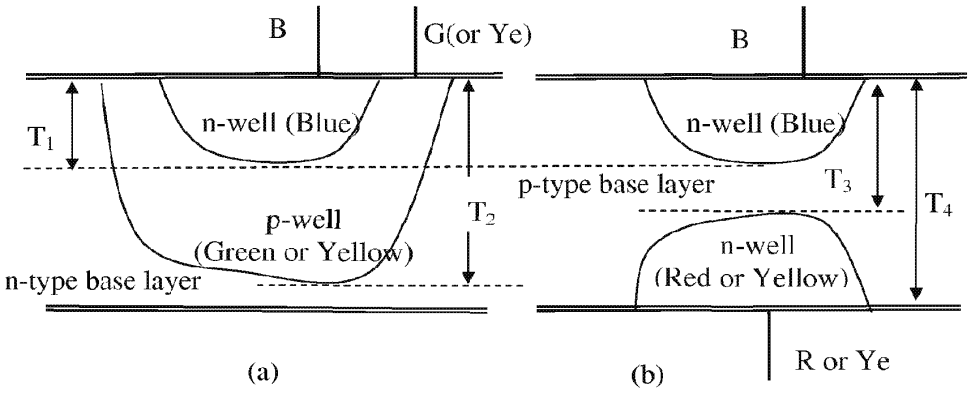

Fig 3

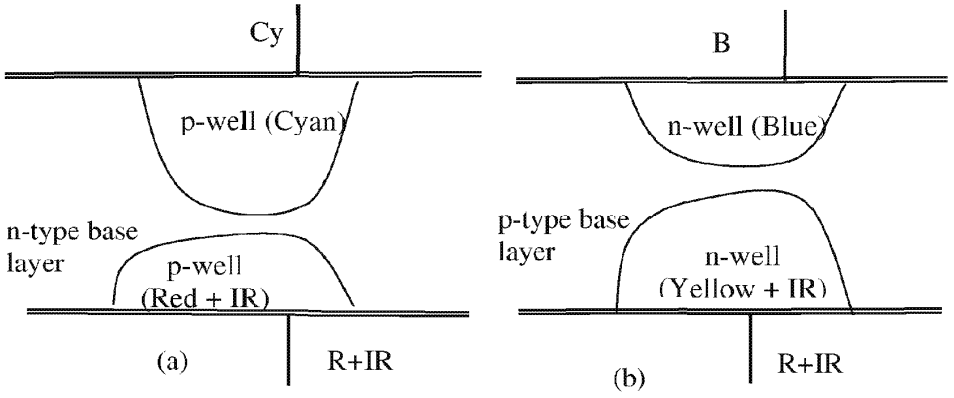

Fig 4

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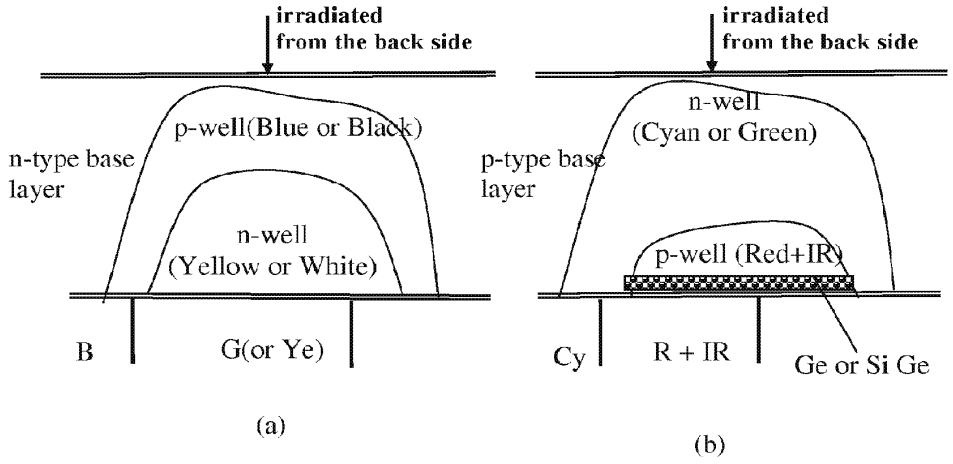

Fig 5

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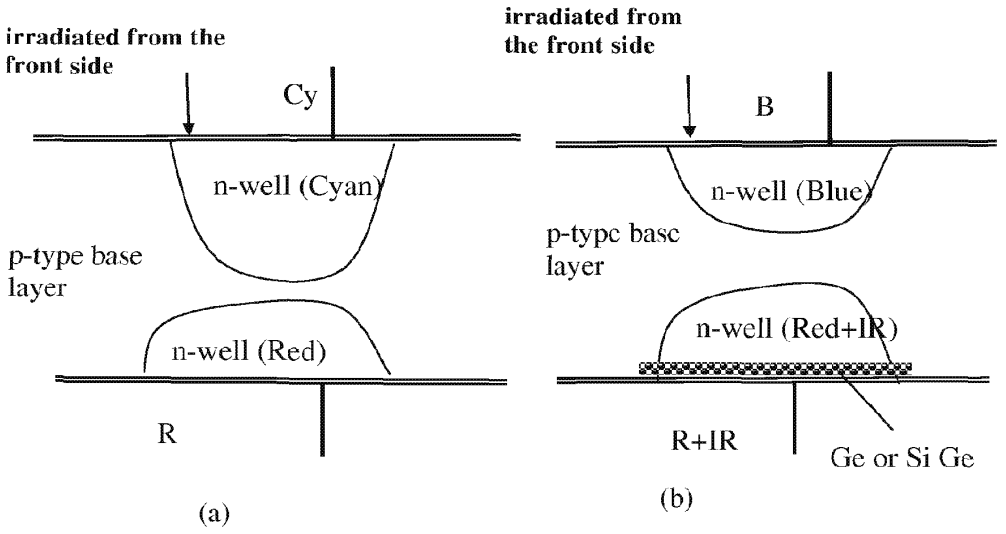

Fig 6

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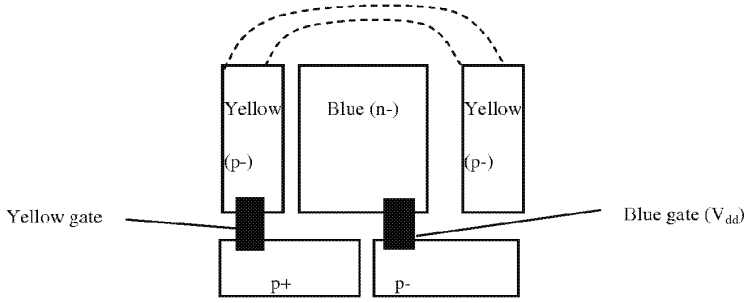

Fig 7

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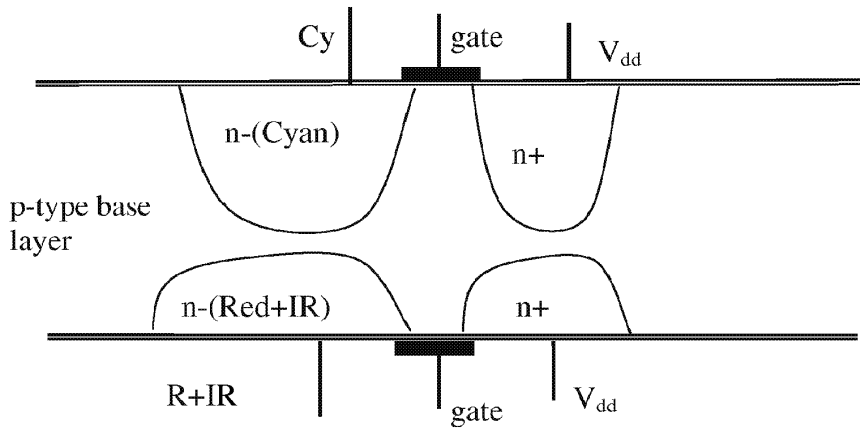

Fig 8

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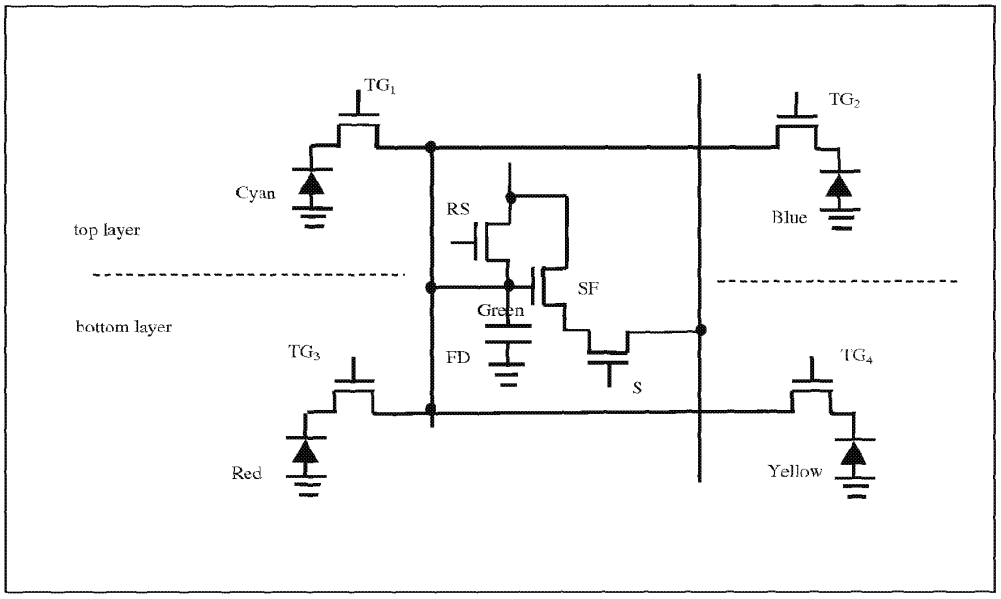

Fig 9

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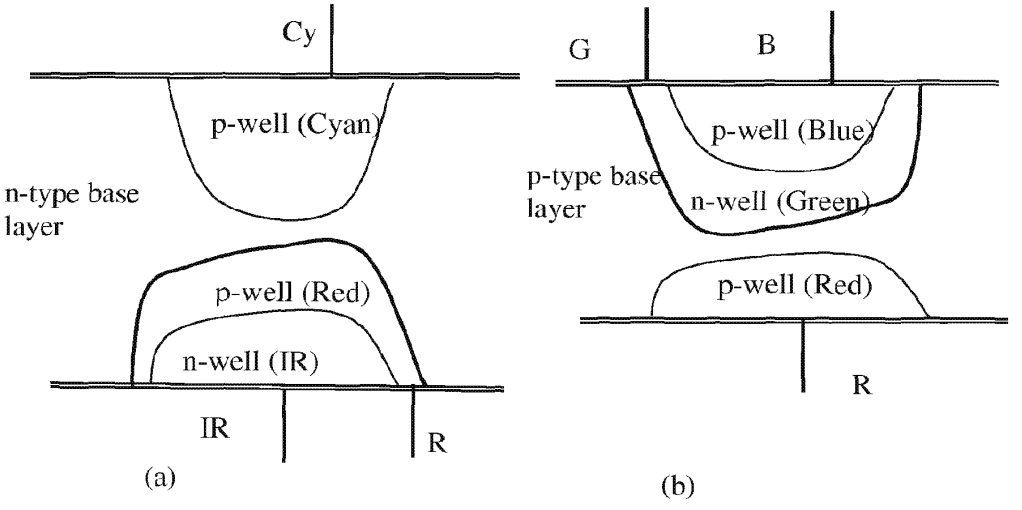

Fig 10

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SAMSUNG EX. 1002 - 3482/4148

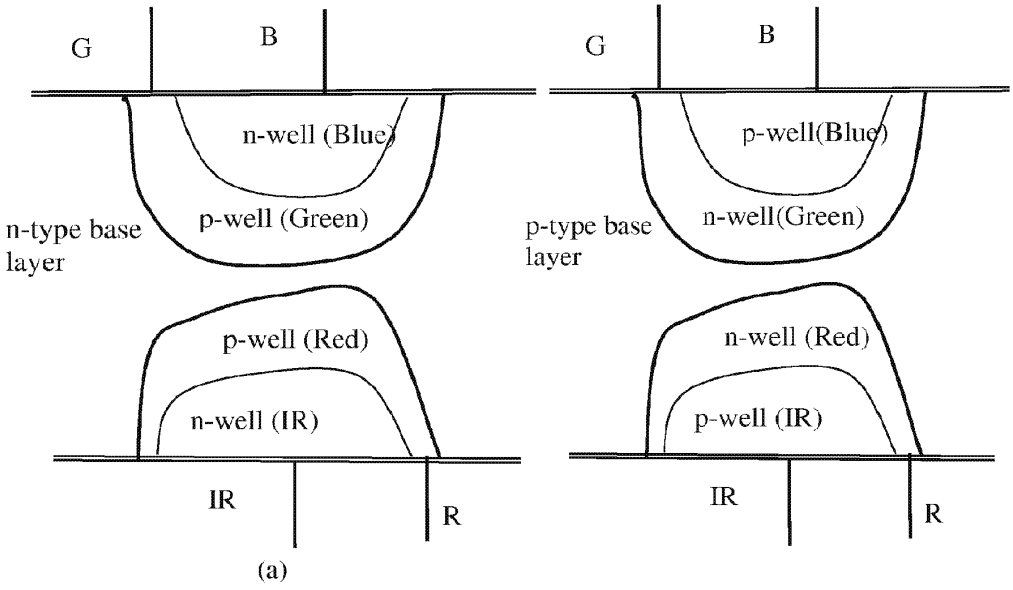

Fig 11

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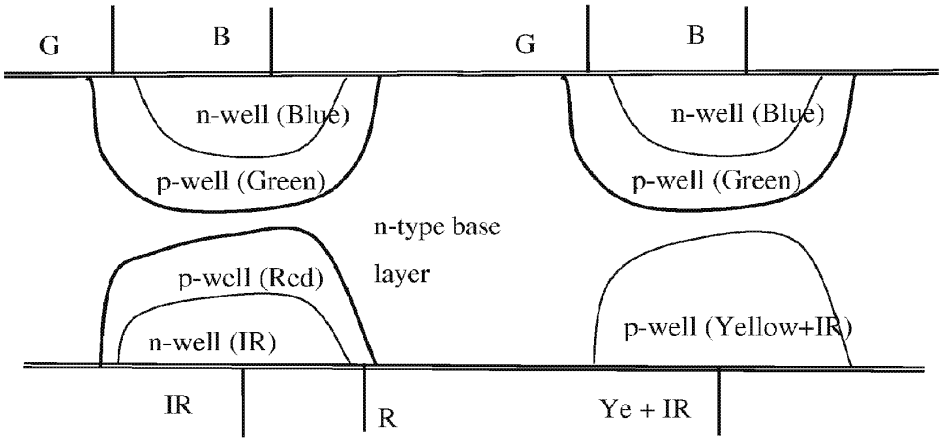

Fig 12

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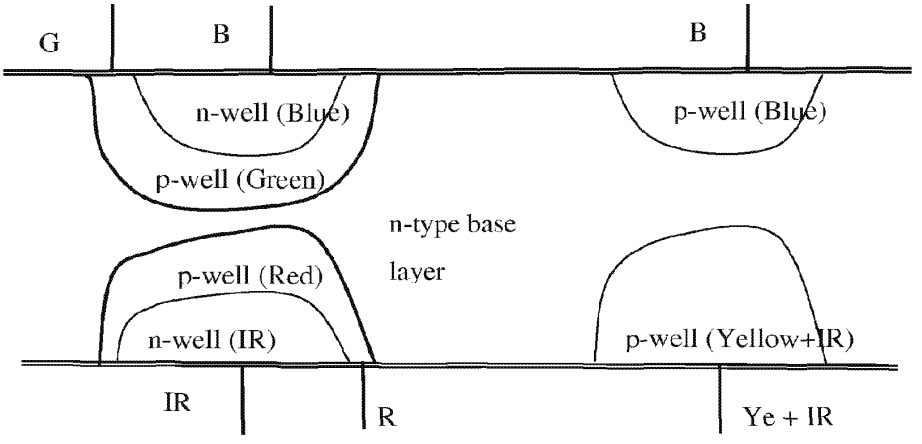

Fig 13

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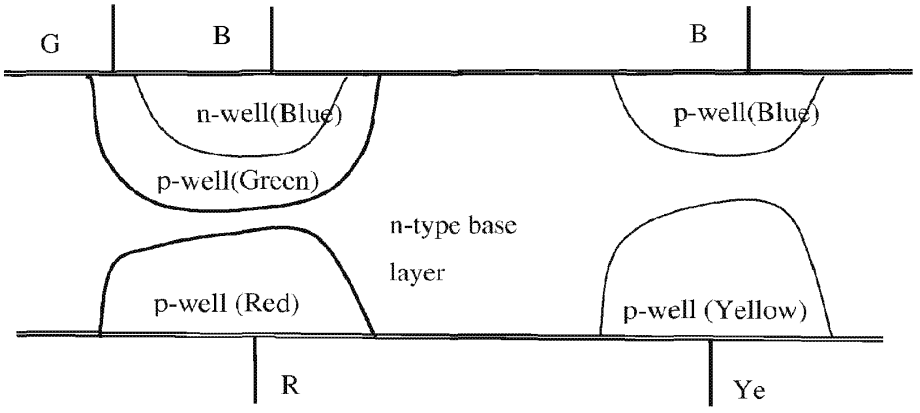

Fig 14

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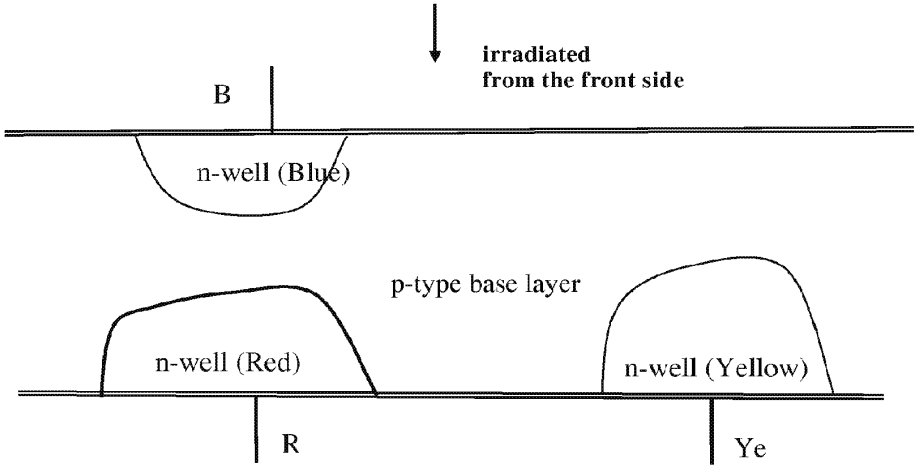

Fig 15

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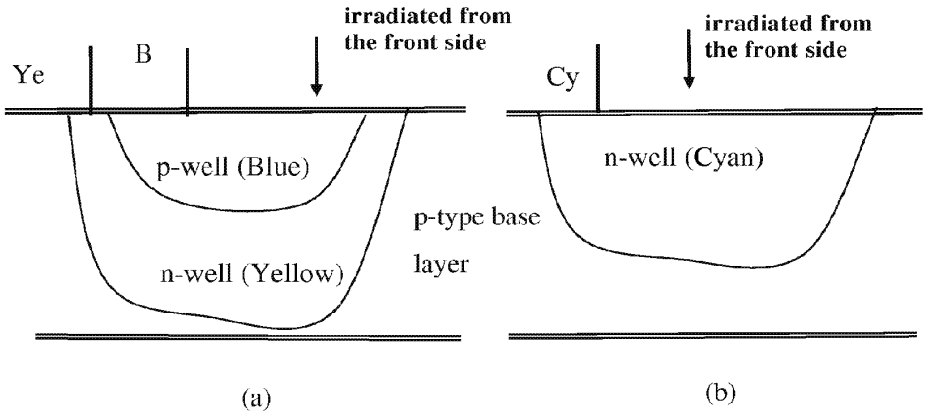

Fig 16

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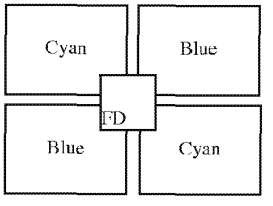

Fig17(a)

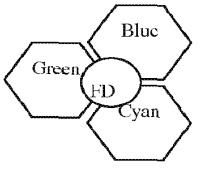

Fig17(b)

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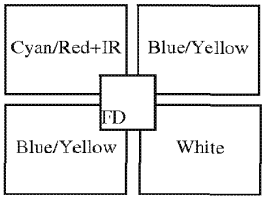

Fig 18(a)

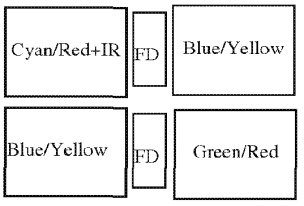

Fig18(b)

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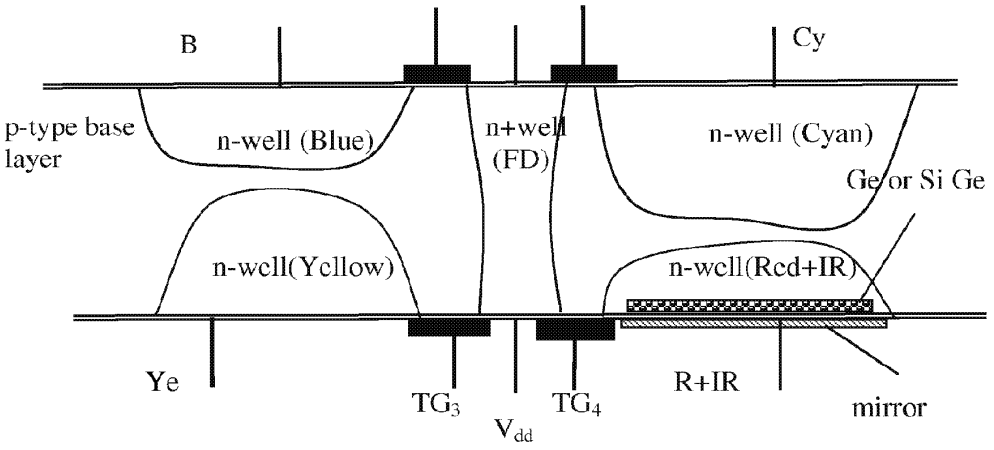

Fig 19

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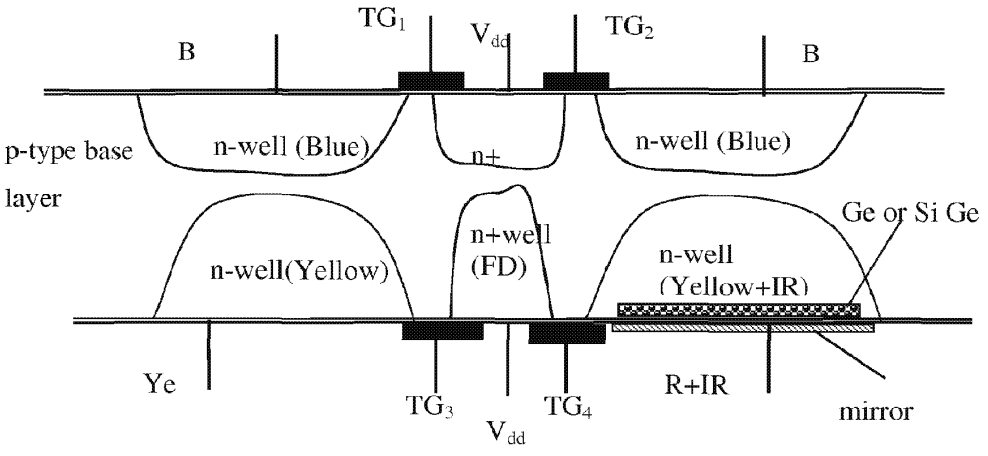

Fig 20

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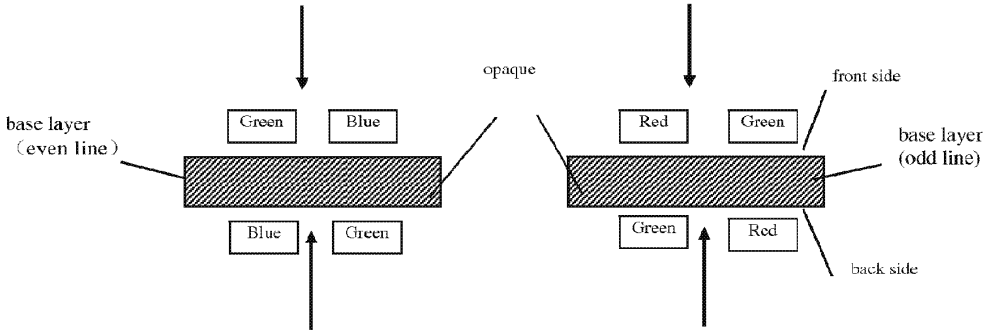

Fig 21

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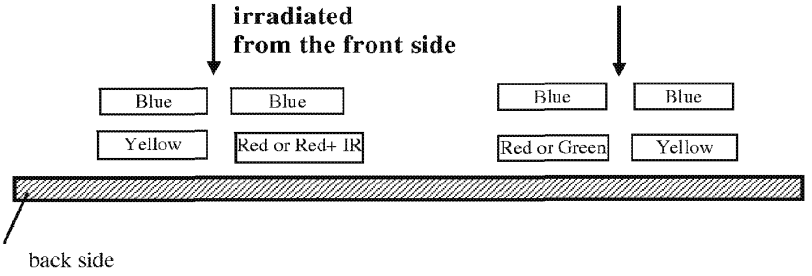

Fig 22(a)

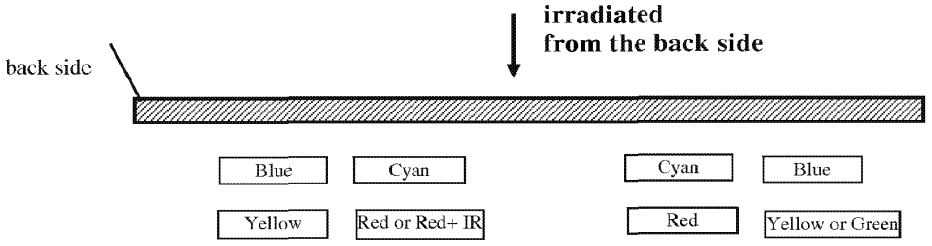

Fig 22(b)

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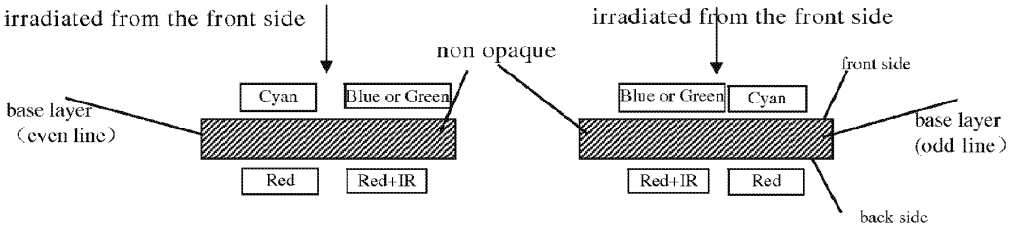

Fig23 (a)

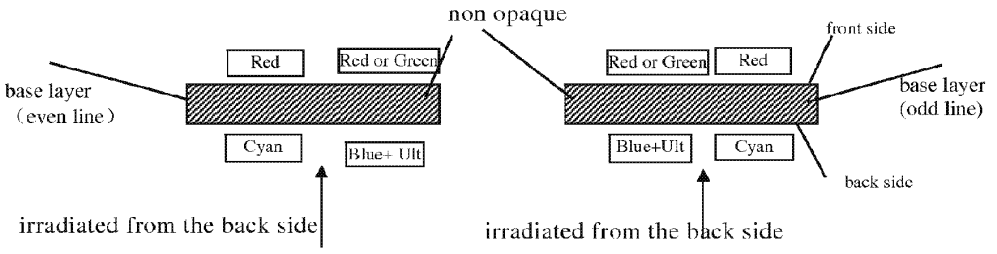

Fig23 (b)

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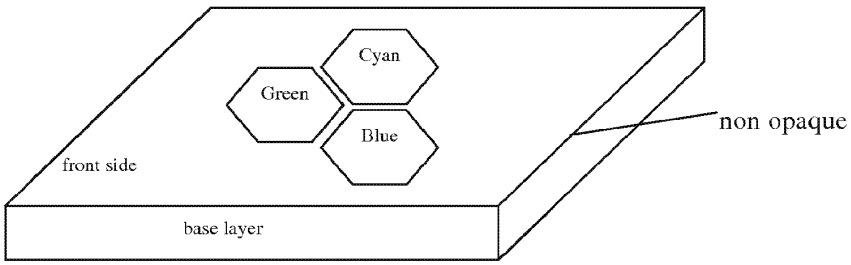

Fig24（a）

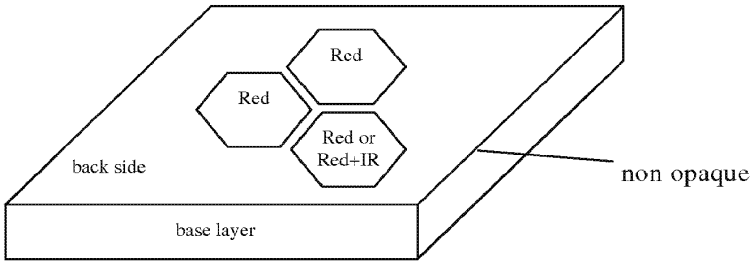

Fig24（b）

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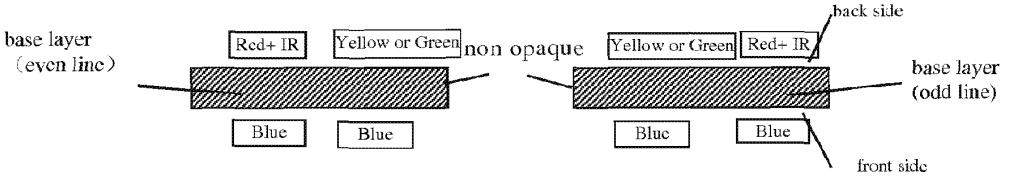

Fig 25

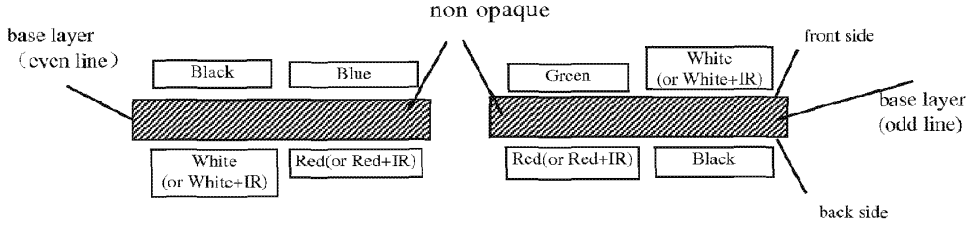

Fig 26

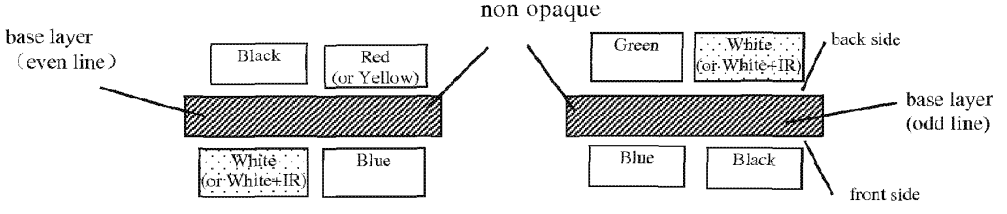

Fig 27

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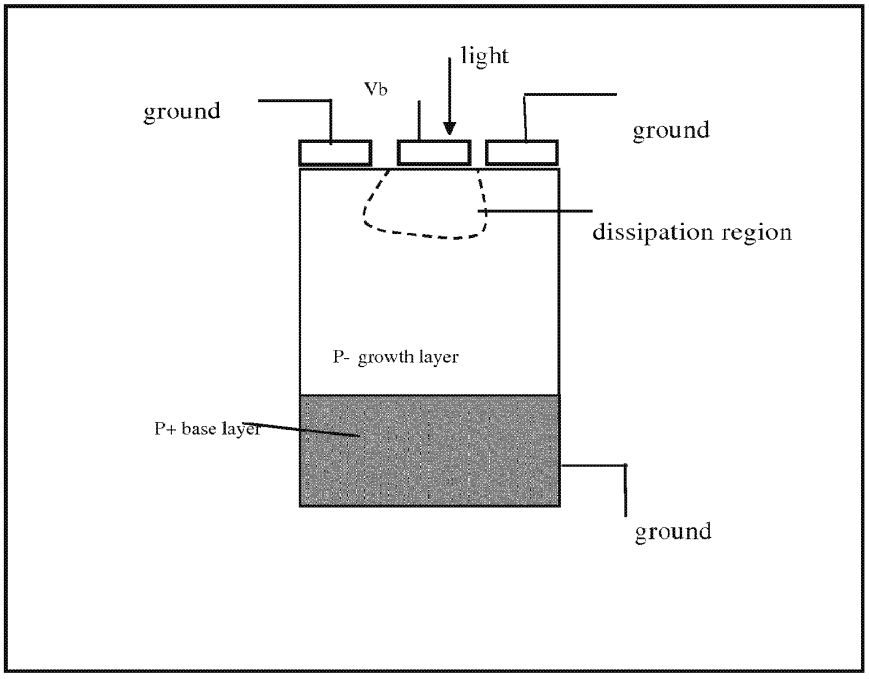

Fig 28

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2010/073440

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/146 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L 27/-, H01L 21/-, H01L 29/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI,WPI, EPODOC: composite pixel photosensi+ muli-colo?r multispec+ back backside rear photodiode photo-diode stack+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US2010/0109060A1 (OMNIVISION TECHNOLOGIES INC.) 06 May 2010 (06.05.2010) page 2, par. 16 to page 3, par. 29, figures 1-3	1-3, 9-10, 18-22
E	CN101807590A (BOLY MEDIA COMMUNICATIONS (SHENZHEN) CO., LTD.) 18 Aug. 2010 (18.08.2010) claims 1-22	1-22
A	CN101640213A (DONGBUHAITEK CO., LTD.) 03 Feb. 2010 (03.02.2010) The whole document	1-22
A	CN101345248A (BOLY MEDIA COMMUNICATIONS (SHENZHEN) CO., LTD.) 14 Jan. 2009 (14.01.2009) the whole document	1-22

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 Feb. 2011 (21.02.2011)	**24 Mar. 2011 (24.03.2011)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer YANG Yong Telephone No. (86-10)62411777

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2010/073440

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN101577287A (SAMSUNG ELECTRONICS CO., LTD.) 11 Nov. 2009 (11.11.2009) the whole document	1-22
A	US2007/0218578A1 (SHARP LABORATORIES OF AMERICA, INC.) 20 Sep. 2007 (20.09.2007) the whole document	1-22
A	Dietmar Knipp et al. Vertically Integrated Amorphous Silicon Color Sensor Arrays, IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 53, No. 7, Jul. 2006, pages 1551-1557	1-22

Form PCT/ISA /210 (continuation of second sheet) (July 2009)

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2010/073440

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
US2010/0109060A1	06.05.2010	NONE	
CN101807590A	18.08.2010	NONE	
CN101640213A	03.02.2010	US2010026863A1	04.02.2010
		KR20100012639A	08.02.2010
CN101345248A	14.01.2009	WO2009006776A1	15.01.2009
		EP2172973A1	07.04.2010
		US2010141771A1	10.06.2010
		KR20100057599A	31.05.2010
		CA2705315A1	15.01.2009
		INMUMNP201000137E	16.07.2010
		JP2010532869T	14.10.2010
		CN101345248B	14.07.2010
CN101577287A	11.11.2009	EP2117047A1	11.11.2009
		US2009278048A1	12.11.2009
		JP2009272620A	19.11.2009
		KR20090117437A	12.11.2009
US2007/0218578A1	20.09.2007	US7419844B2	02.09.2008

Form PCT/ISA /210 (patent family annex) (July 2009)

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REFERENCES CITED IN THE DESCRIPTION

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- CN 200810217270 **[0002] [0061] [0084]**
- CN 2010073441 W **[0084]**

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- **GERALD C. HOLST ; TERRANCE S. LOMHEIM.** CMOS/CCD Sensors and Camera Systems. JCD Publishing, 2007, 125-125 **[0039]**

SIONYX1403000034.0113

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Espacenet

Bibliographic data: JP2003258285 (A) — 2003-09-12

MANUFACTURING METHOD OF RUGGED SURFACE STRUCTURE AND SOLAR BATTERY

Inventor(s): YO MINKYO ± (YO MINKYO)

Applicant(s): SHARP KK ± (SHARP CORP)

Classification: **- international:*H01L21/308; H01L31/04;*** (IPC1-7): H01L21/308; H01L31/04
- cooperative: Y02E10/546

Application number: JP20020051513 20020227 Global Dossier

Priority number (s): JP20020051513 20020227

Abstract of JP2003258285 (A)

PROBLEM TO BE SOLVED: To provide a manufacturing method of a silicon substrate by which a rugged surface structure of high quality can be attained at low cost. ;SOLUTION: This manufacturing method of the surface rugged structure comprises a process for forming grooves by irradiating the surface of a silicon substrate with a laser beam, and a process for forming the ruggedness on the silicon substrate by selectively etching the grooves by chemical etching. ;COPYRIGHT: (C)2003,JPO

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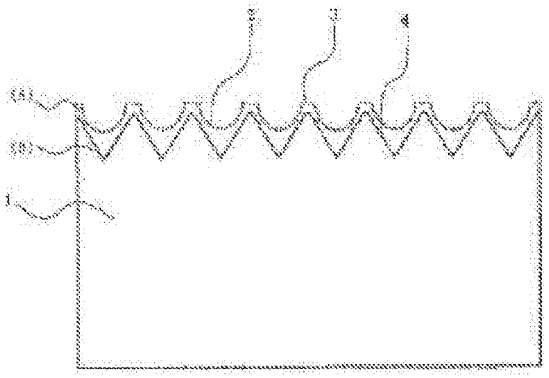

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(19)日本国特許庁（ＪＰ）　(12) 公開特許公報（Ａ）　(11)特許出願公開番号
特開2003－258285
（P2003－258285A）
(43)公開日　平成15年９月12日(2003.9.12)

(51)Int.Cl.⁷	識別記号	ＦＩ		ﾃｰﾏｺｰﾄﾞ(参考)
Ｈ０１Ｌ　31/04		Ｈ０１Ｌ　21/308	Ｄ	５Ｆ０４３
21/308		31/04	Ｈ	５Ｆ０５１

審査請求　未請求　請求項の数５　ＯＬ　（全５頁）

(21)出願番号　特願2002－51513(P2002－51513)

(22)出願日　平成14年２月27日(2002.2.27)

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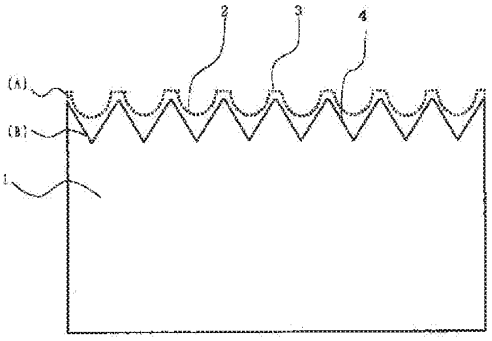
(74)代理人　100065248
弁理士　野河　信太郎

Ｆターム(参考)　5F043 AA10 BB03 FF04 GG10
5F051 AA03 BA11 CB21 CB27 CB30
DA03 FA10 GA04 GA14 GA15
GA20 HA03 HA07

(54)【発明の名称】　表面凹凸構造の作製方法及び太陽電池

(57)【要約】
【課題】　低コストで高品質の表面凹凸構造を備えたシリコン基板の製造方法を提供することを課題とする。
【解決手段】　シリコン基板の表面にレーザー光を照射することで溝を形成する工程と、化学エッチングにより溝を選択的にエッチングすることでシリコン基板の表面に凹凸を形成する工程を含むことを特徴とする表面凹凸構造の作製方法により上記課題を解決する。



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【特許請求の範囲】
【請求項１】　シリコン基板の表面にレーザー光を照射することで溝を形成する工程と、化学エッチングにより溝を選択的にエッチングすることでシリコン基板の表面に凹凸を形成する工程を含むことを特徴とする表面凹凸構造の作製方法。
【請求項２】　化学エッチングが、フッ酸：硝酸＝３～１０：１（モル比）の混酸中で行なわれる請求項１に記載の作製方法。
【請求項３】　化学エッチングが、フッ酸及び硝酸と、酢酸、硫酸及びリン酸から選択されるいずれかの酸との混酸中で行なわれる請求項１又は２に記載の作製方法。
【請求項４】　化学エッチングが、撹拌下、０～２５℃の範囲で行なわれる請求項１～３のいずれか１つに記載の作製方法。
【請求項５】　請求項１～４のいずれか１つに記載の方法を用いて作製された表面凹凸構造を有するシリコン基板を備えた太陽電池。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、表面凹凸構造の作製方法及び太陽電池に関する。更に詳しくは、本発明は、光閉じ込め用の表面凹凸構造の作製方法及びその方法により作製された表面凹凸構造を含む太陽電池に関する。
【０００２】
【従来の技術】単結晶シリコン太陽電池の一般的な製造方法は、次のような工程からなる。まず、光入射面となるシリコン基板表面に表面反射を低減するための凹凸構造を形成する。次に、熱拡散によるＰＮ接合を形成し、反射防止膜を形成し、表面及び裏面の電極を形成する。
【０００３】上記表面凹凸構造は、単結晶シリコン基板をＮａＯＨ、ＫＯＨ、Na_2CO_3等アルカリ水溶液に浸して、８０～９０℃の温度でエッチングを行うことで形成される。アルカリ水溶液は面方位に対して、エッチング速度が違うため、シリコン面方位（１００）の基板を用いた場合には低い反射率のピラミッド型の表面凹凸構造が得られる。
【０００４】しかしながら、近年低コスト化の必要性から、多結晶シリコン基板が単結晶に代わり用いられるようになってきている。多結晶基板では、種々の面方位の結晶粒から構成されるので、面方位（１００）に近い結晶粒の表面以外は、低い反射率の表面凹凸を得ることは困難である。従って、全体の表面反射率として低減の余地がある。
【０００５】このため、各種の表面凹凸構造の形成技術が開発されている。その中で、ダイサー等を用いる機械加工、レーザー加工（例えば、特開平６－１３６３２号公報参照）、フォトリソグラフィによる化学エッチングでの加工、プラズマとガス反応併用のエッチング加工（ＲＩＥ）等の低い反射率の凹凸構造の作製方法の検討が行われている。
【０００６】また、特開平１０－３０３４４３号公報に記載されているように、エッチング速度の調整剤となるリン酸あるいはカルボン酸を、添加した硝酸とフッ酸の混酸に混合する又は界面活性剤を添加した硝酸とフッ酸の混酸を用いた方法も検討されている。この方法では、微小な球面状の凹部から構成されるテクスチャ表面が得られる。
【０００７】
【発明が解決しようとする課題】機械加工による溝形成方法は、ダイサーの刃がシリコン基板と直接に接触するため、刃の消耗が大きい、また、特開平６－１３６３２号公報に記載されているようなレーザー加工による溝形成方法はＶ型溝の形成には、数回のスキャンニングが必要とされ、１枚の基板加工時間はかなり長くなる。フォトリソグラフィ方法ではレジスト膜の形成、露光、現像等複数工程が必要であり、低コスト化は困難である。また、ＲＩＥ方法では、腐食性のガスを使い、真空プロセス装置を使用するため、低コスト化、実用化の観点から困難である。更に、前述の特開平１０－３０３４４３号公報に記載されているようにフッ酸と硝酸を含む混酸を用いた等方性エッチング方法では、鋭角の凹凸構造を形成するのは難しく、反射率低減が十分ではない。
【０００８】
【課題を解決するための手段】かくして本発明によれば、シリコン基板の表面にレーザー光を照射することで溝を形成する工程と、化学エッチングにより溝を選択的にエッチングすることでシリコン基板の表面に凹凸を形成する工程を含むことを特徴とする表面凹凸構造の作製方法が提供される。
【０００９】更に、本発明によれば、上記の方法を用いて作製された表面凹凸構造を有するシリコン基板を備えた太陽電池が提供される。
【００１０】
【発明の実施の形態】まず、本発明では、シリコン基板の表面にレーザー光を照射することで溝を形成する。
【００１１】使用することができるシリコン基板としては、単結晶、多結晶及びアモルファスのシリコン基板が挙げられる。この内、表面凹凸構造の形成が比較的困難な多結晶シリコン基板を使用することが好ましい。また、シリコン基板は、Ｐ又はＮの導電型を有していてもよい。
【００１２】溝の形状は、後の化学エッチングにより所望の凹凸を形成することができさえすれば特に限定されない。例えば、平面形状がストライプ状、ドット状等の形状が挙げられ、断面形状が方形、Ｖ字型、Ｕ字型等の形状が挙げられる。また、溝の幅は１０～１００μｍ、深さは１０～１００μｍであることが好ましい。
【００１３】特に、溝は、一定のピッチで形成されたス

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トライプ状であることが好ましい。ピッチは、10～100μmであることが好ましい。また、シリコン基板表面には、未照射面が残っていることが、加工速度という観点から好ましい。

【0014】レーザー光を生じるレーザー発振器は、シリコン基板の表面に溝を形成することができさえすれば特に限定されず、公知の発振器を使用することができる。例えば、エキシマレーザー、CO_2レーザー、YAGレーザー等の光照射でシリコン基板表面部分を融解できるレーザー発振器が挙げられる。

【0015】レーザー光の照射条件は、所望の形状の溝を形成しうるように適宜調整される。例えば、4×10^{6}～1×10^{9}W／cm^{2}のエネルギー密度になるように、波長、周波数、照射形状等の条件が調整される。なお、レーザー光の照射面積は、シリコン基板の表面積の1／3以下であることが、未照射面を残すという観点から好ましい。

【0016】次に、化学エッチングにより溝を選択的にエッチングすることでシリコン基板の表面に凹凸を形成する。化学エッチングにより形成される凹凸の形状は、レーザー光の照射による溝の形状に依存する。すなわち、レーザー光が照射された部分は、レーザー光で溶解した部分とその下部に結晶欠陥があるため、化学エッチングのエッチング速度は、上記部分以外に比べて相対的に速くなる。つまり、選択エッチングが生じる。この選択エッチングを利用して、レーザー光が照射された部分が優先的にエッチングされ、平坦部の面積が相対的に狭くなっていき、溝の形状に依存した凹凸が形成される。

【0017】化学エッチングは、ドライエッチング又はウェットエッチングのいずれでもよいが、ウェットエッチングであることが好ましい。このエッチングに使用できるエッチャントとしては、例えば、フッ酸と硝酸の混酸が挙げられる。混酸中のフッ酸：硝酸は、3～10：1（モル比）割合であることが好ましい。この割合の混酸を使用すれば、酸化剤である硝酸の濃度が相当低いので、シリコン基板に酸化物層が形成されるより、シリコン基板表面に多数存在する結晶欠陥部分からエッチングを始めることができる。この混酸には、エッチング速度を制御するため、酢酸、硫酸及びリン酸から選択されるいずれかの酸が更に含まれていてもよい。

【0018】混酸中には、プロピオン酸、酪酸、ピバル酸、カプロン酸、酒石酸、コハク酸、アジピン酸、プロパントリカルボン酸等を更に添加してもよい。

【0019】化学エッチングは、0～25℃の範囲で行なうことが好ましい。この範囲内では、上記欠陥部分の反応比率を大きくでき、このことにより溝内の側面のエッチング速度を抑えることができる。更に、エッチング液を撹拌することで、溝底部へのエッチング液の供給を促進することができる。それにより、より鋭角（例えば、シリコン基板表面に対する溝側面の角度が45°以上）な凹形状（例えば、V字型）の凹凸構造が形成できる。

【0020】ここで、凹凸構造の凹部の深さは30～120μm、幅は30～120μmであることが好ましい。深さは、30～80μm、幅は30～80μmであることがより好ましい。

【0021】上記表面凹凸構造を備えたシリコン基板は、太陽電池の基板として好適に使用される。

【0022】太陽電池の製造方法は、例えば、シリコン基板の表面凹凸構造側に、導電性不純物を拡散することでPN接合を形成する。この半導体層は、シリコン基板がPの場合はN、Nの場合はPの導電型を有している。半導体層は、例えば、単結晶、多結晶、アモルファスのシリコン層が使用できる。次いで、シリコン基板の裏面に裏面電極、半導体層上の表面収集電極を形成することで太陽電池を製造することができる。

【0023】なお、表面収集電極と半導体層の間に、反射防止膜を形成してもよい。

【0024】上記構成の太陽電池では、シリコン基板が表面凹凸構造を有していることで、太陽電池の反射率を著しく低減でき、その構造のない太陽電池より、光電変換効率を向上させることができる。

【0025】

【実施例】以下、本発明を実施例により更に詳細に説明するが、本発明は以下の実施例には限定されない。

【0026】図1は本発明によるレーザー表面加工とウェットエッチング方法の併用で表面凹凸構造を形成した多結晶シリコン基板の概略断面図である。図2は、実施例の多結晶太陽電池の概略断面図である。

【0027】本実施例では、光照射でシリコン基板表面を融解できるレーザー発振器として、YAGレーザーを用いた。

【0028】以下には、本発明の方法を用いた多結晶基板の表面凹凸構造の形成及び太陽電池の作製について説明する。

【0029】まず、レーザー光による溝の形成について説明する。

【0030】基板は、厚さ約350μm、抵抗率1Ω・cm程度のP型多結晶シリコン基板を用いた。最初に、酸による等方性エッチングを行い、表面の研削ダメージ層を除く。

【0031】高速移動できる電動ステージに該多結晶シリコン基板を載せ、レーザー光を照射すると、照射した面のシリコンが溶融、蒸発する。レーザー光は、波長1．06μm、周波数5kHzのパルス光を用いた。レーザー光は、図4に示すように光強度分布があるものを使用し、これを光学レンズで集光し、四角形のスリットを通した。レーザー光照射形状は50×50μm^{2}の正方形であり、照射面におけるエネルギー密度を8×10^{5}W／cm^{2}とした。このレーザー光の1回照射で、浅い

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U形の穴を形成する。すなわち、シリコン基板を載せた電動ステージをX軸方向へ高速に移動すると、線形の浅いU型溝が形成される。また、Y軸方法へ一定ピッチ移動し、X軸方向へ高速移動すると、もう一つのU型溝が形成される。このように繰り返すと、図1中、レーザー光照射後の表面形状である（A）に示すように、X軸とY軸におけるシリコン基板1表面に一定ピッチのU型溝2が全面的に形成される。U型溝のピッチは75μm、幅は約50μm、深さは約20μmである。図1中、3は平坦部である。

【0032】次に、ウェットエッチングを行う。この実施例における処理方法では、まず、フッ酸：硝酸：リン酸＝5：1：12（モル比）の混酸からなるエッチャントを調製する。エッチャントの温度はエッチング槽外の恒温槽により5℃程度に制御しておく。また、スクラーを用いて磁石回転によるエッチャントを撹拌する。レーザー光で表面加工した基板をテフロン（登録商標）製のキャリアに載せて、エッチング液と接触させることでエッチングを行う。シリコンエッチング速度は約3μm／minである。このウェットエッチングではレーザー光に照射された部分とその下にある浅い部分が除去されるとともに、レーザー光で照射していない部分の平坦部が少なくなる。図1のウェットエッチング後の表面形状である（B）に示すように深いV型溝4からなる表面凹凸構造が形成される。このV型溝4の幅は約72μm、深さは約35μm、シリコン基板1表面に対するV型溝4側面の角度は°である。この表面凹凸構造による反射率スペクトルを図3に示す（図中a）。なお、図3には、エッチング処理を行なわない場合（図中b）と、レーザー光照射及びエッチング処理の両方を行なわない場合（図中c）の反射率スペクトルも合わせて示している。

【0033】この表面凹凸構造を形成した後に、RCA方法で洗浄し、燐拡散によりPN接合を形成し、厚さ約0.3μm、不純物濃度1.2×$10^{20}$$cm^{-3}$のN型シリコン層5を形成する。続いて光入射面とする表面側の拡散層だけを樹脂マスクで保護し、裏面とする反対側面のN型拡散層を化学エッチングにより除去する。

【0034】次に、N型シリコン層5の上にTiO_2反射防止膜6を形成した後、裏面にA1ペーストと表面に銀ペーストを印刷し、それぞれ、ベルト焼成炉で乾燥、焼成して（温度700℃）、表面収集電極7及び裏面電極8を形成する。また、半田用Sn溶融液にディップして、両電極を厚くする。最終に電極リード線を付けて、表面凹凸構造を有する多結晶シリコン基板を含む太陽電池が形成される。この太陽電池の概略断面図を図2に示す。

【0035】表面凹凸構造を形成することにより、太陽電池表面の反射率を著しく低減でき、光電流密度が向上した。その結果、太陽電池の変換効率向上に一層寄与できた。多結晶シリコン太陽電池の光電変換効率は、従来アルカリ法で形成した表面凹凸構造の太陽電池の変換効率の14%程度から17%程度まで顕著に向上させることができるという効果があった。この実施例で得られた太陽電池の特性を従来例と共に表1に示す。

【0036】

【表1】

	Jsc(mA/cm²)	Voc(mV)	F. F.	効率（%）
従来例	33.3	605	0.741	14.9
実施例	36.2	613	0.764	17.0

【0037】なお、表中、Jsc（mA／cm²）、Voc（mV）、F. F. 及び効率は以下の方法により測定した。

【0038】測定ステージの温度を25℃、AM1・5の太陽光シュミレーターの照射強度100mW／cm²、太陽電池の面積を100mm²として測定した。

【0039】

【発明の効果】本発明によれば、多結晶太陽電池の表面凹凸形成において、レーザー光照射と化学エッチングの併用により、低コストで高品質の表面凹凸構造を備えたシリコン基板を得ることができる。更に、この表面凹凸構造を備えたシリコン基板を太陽電池に用いることで、より光電変換効率を向上させることができる。

【図面の簡単な説明】

【図1】本発明によるレーザー光照射と化学エッチングの併用で表面凹凸構造を形成した多結晶シリコン基板の概略断面図である。

【図2】実施例の太陽電池の概略断面図である。

【図3】実施例の表面凹凸構造による反射率スペクトルである。

【図4】実施例で使用するレーザー光の光強度分布を示すグラフである。

【符号の説明】

1 シリコン基板
2 U型溝
3 平坦部
4 V型溝
5 N型シリコン層
6 反射防止膜
7 表面収集電極
8 裏面電極
A レーザー光照射後の表面形状
B ウェットエッチング後の表面形状

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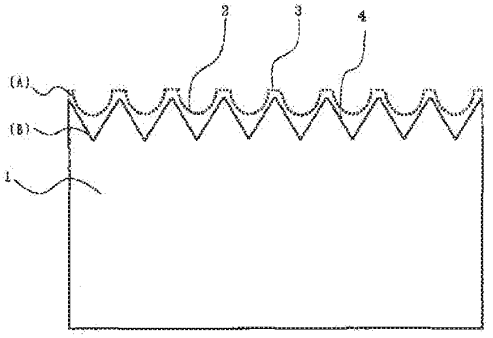
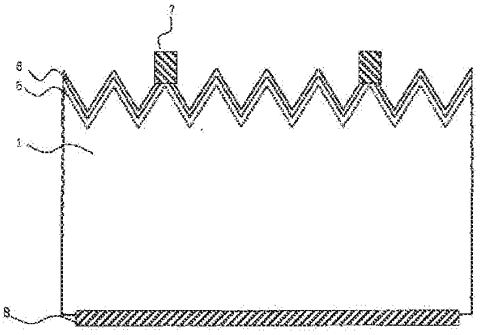
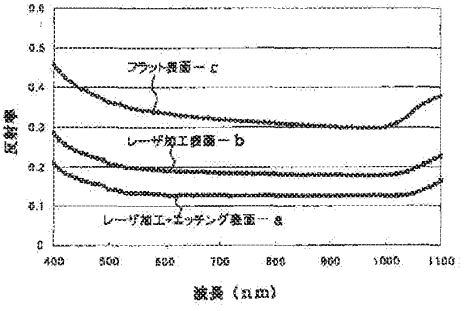
【図1】


2
3
4
(A)
(B)
1

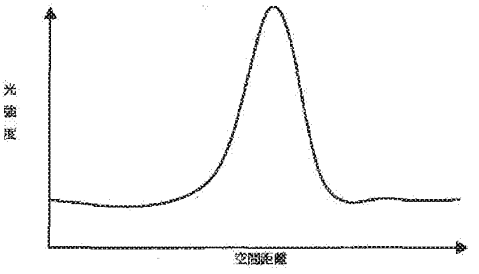
【図2】


7
6
5
1
8

【図3】


0.6
0.5
0.4
0.3
0.2
0.1
0
反射率
フラット表面－ c
レーザ加工表面－ b
レーザ加工＋エッチング表面－ a
400
500
600
700
800
900
1000
1100
波長（nm）

【図4】


光強度
空間距離

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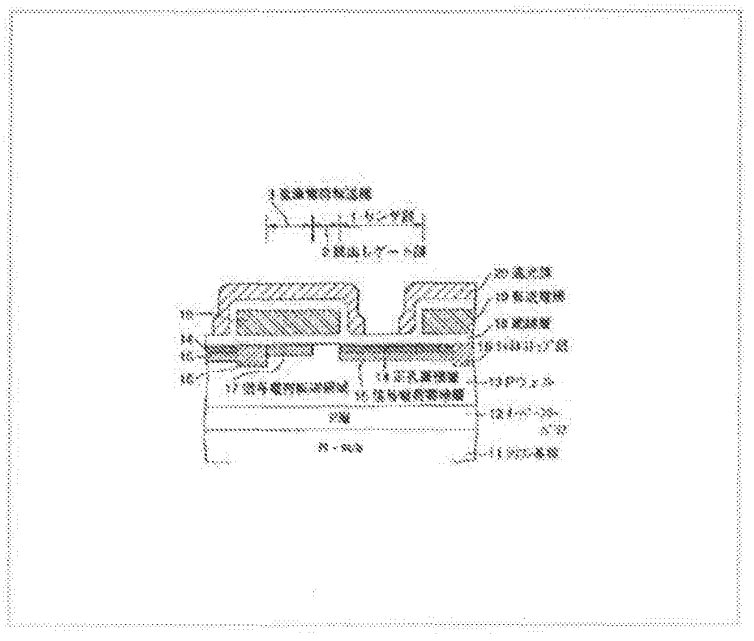
(71)Applicant	SONY CORP
(72)Inventor	ABE HIDEJI

(54)SOLID-STATE IMAGE SENSOR AND FORMATION OF SENSOR STRUCTURE THEREOF

(57)Abstract

PURPOSE: To provide the structure of a solid-state image sensor, wherein the multiple reflections between the surface of a substrate and the lower edge of a light screening film or a transfer electrode in a charge transfer part is eliminated and smear can be decreased.

CONSTITUTION: In a CCD area sensor having a plurality of sensor parts 1 and vertical charge transfer parts 3 for transferring the signal charges read out of the sensor parts, the sensor structure is formed so that each incident surface of the sensor part 1 is formed in an irregular shape, and the light, which is obliquely cast into the sensor part 1, is not reflected into the protruding part forming the irregular shape and is not cast in a signal-charge transfer region 17.



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CLAIMS

[Claim(s)]
[Claim 1]A solid state imaging device which is provided with the following and characterized by a thing of each incident plane of two or more aforementioned sensor parts for which a peripheral edge part is making uneven form at least.
Two or more sensor parts which carry out photoelectric conversion of the incident light, and accumulate the signal charge and which were arranged by at least one row.
A charge transfer section which transmits a signal charge read from two or more aforementioned sensor parts.

[Claim 2]The solid state imaging device according to claim 1, wherein each whole incident plane surface of two or more aforementioned sensor parts is making uneven form.
[Claim 3]The solid state imaging device according to claim 1 or 2, wherein a pitch and height of a protruding part of said uneven form are set up 1 of wavelength of incident light / 10 to 10 times.
[Claim 4]Two or more sensor parts which carry out photoelectric conversion of the incident light, and accumulate the signal charge and which were arranged by at least one row.
A charge transfer section which transmits a signal charge read from two or more aforementioned sensor parts.
In a formation method of sensor structure in a solid state imaging device provided with the above,
A formation method of sensor structure which forms hemispherical grain polysilicon on it and is characterized by etching the aforementioned silicon oxide film from a gap between said hemispherical grain polysilicon while forming a silicon oxide film on a sensor surface.

[Claim 5]A formation method of the sensor structure according to claim 4 characterized by forming a trench in a sensor surface of the etching portion after etching the aforementioned silicon oxide film.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]The present invention relates to a solid state imaging device, and relates to structure of the sensor part especially in a solid state imaging device, and a formation method for the same.
[0002]
[Description of the Prior Art]As an example of a solid state imaging device, it is CCD (ChargeCoupled Device) of an interline transmission mode, for example. The schematic structure of an area sensor is shown in Fig.6. In the figure, level and two or more sensor parts 1 which two-dimensional array is perpendicularly carried out, carry out photoelectric conversion of the incident light, and accumulate the signal charge, The imaging part 4 is constituted by the vertical charge transfer section 3 which transmits perpendicularly the signal charge which was arranged for every vertical file of these sensor parts 1, and read at a part of vertical blanking period, and was read via the gate section 2.
[0003]In this imaging part 4, the sensor part 1 consists of photo-diodes, and the vertical charge transfer section 3 is constituted by CCD. The signal charge read from the sensor part 1 to the vertical charge transfer section 3 is transmitted to the horizontal transfer part 5 in order of partial [every] which is equivalent to one scanning line at a part of horizontal blanking period. The signal charge for this one scanning line is sequentially transmitted horizontally by the level charge transfer section 5.
[0004]The transmitted signal charge is detected, and it converts to a signal level, for example, the charge detector 6 which consists of FDA (Floating Diffusion Amplifier) is arranged at the output side of the level charge transfer section 5. The essential part of the section (A-A' arrowed cross-section of Fig.6) structure of the sensor part 1 and the vertical charge transfer section 3 is shown in Fig.7.
[0005]
[Problem to be solved by the invention]At the vertical charge transfer section 3 in the above-mentioned CCD area sensor, as shown in Fig.7, the structure which intercepts the incidence of an extraneous light to the signal-charge transfer region 73 is taken by forming the light-shielding film 72 which becomes the portion except the sensor part 1, i.e., the outside of the transfer electrode 71, from aluminum etc.
[0006]However, since the surface of the sensor part 1 is formed as a flat surface in the conventional sensor structure so that clearly from Fig.7, When light enters into the sensor part 1 aslant, the lower end surface 72a of the light-shielding film 72 has an incident component among the lights reflected in the sensor surface, This reflected light component repeated the multiple echo between the substrate surface, the lower end surface 72a of the light-shielding film 72, or the transfer electrode 71, it jumped into the signal-charge transfer region 73 eventually, the photoelectron was generated, and there was a problem of making a smear

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component increase.
[0007]In light of the above-mentioned problems, the present invention comes out.
the object loses a multiple echo between a substrate surface, a lower end surface of a light-shielding film, or a transfer electrode which can be boiled and set, and there is in providing sensor structure of a solid state imaging device which enabled reduction of a smear, and a formation method for the same.

[0008]
[Means for solving problem]Two or more sensor parts which the solid state imaging device according to claim 1 carries out photoelectric conversion of the incident light, and accumulate the signal charge and which were arranged by at least one row, The charge transfer section which transmits the signal charge read from two or more of these sensor parts is provided, and it has the composition of each incident plane of two or more sensor parts that the peripheral edge part made uneven form at least.
[0009]The solid state imaging device according to claim 2 has the composition that each whole incident plane surface of two or more sensor parts made uneven form, in the solid state imaging device according to claim 1. The solid state imaging device according to claim 3 has the composition that uneven-shaped the pitch and height of the protruding part were set up 1 of the wavelength of incident light / 10 to 10 times, in the solid state imaging device according to claim 1 or 2.
[0010]The formation method of the sensor structure according to claim 4 forms hemispherical grain polysilicon on it, and etches the silicon oxide film under it from the gap between this hemispherical grain polysilicon while it forms a silicon oxide film on a sensor surface. In the formation method of the sensor structure according to claim 4, the formation method of the sensor structure according to claim 5 forms a trench in the sensor surface of the etching portion, after etching a silicon oxide film.
[0011]
[Function]In the solid state imaging device according to claim 1, when light enters into a sensor part aslant, the incident light is reflecting on the side surface of the protruding part which forms the uneven form of an incident plane peripheral edge part, and it does not enter to the charge transfer section side. Therefore, the substrate surface in a charge transfer section, the lower end surface of a light-shielding film, or the multiple echo between transfer electrodes does not happen, and does not enter into the transfer region of a charge transfer section. On the side surface of a yet another protruding part, by repeating a reflection, eventually, the light reflected on the side surface of the protruding part transmits, and photoelectric conversion is carried out to the substrate side. As a result, the sensitivity of a sensor part improves.
[0012]In the solid state imaging device according to claim 2, when the light which entered into the sensor part from the upper part transmits the uneven surface of an incident plane, the part reflects it. This reflected light is repeating a reflection on the side surface of a protruding part, and it transmits it to the substrate side eventually. That is, although a reflection of a certain amount of light in an incident plane is not avoided, the reflected light is also eventually incorporated into a sensor part. As a result, the sensitivity of a sensor part improves. In the solid state imaging device according to claim 3, the above-mentioned operation is effectively exerted by setting up uneven-shaped the pitch and height of a protruding part 1 of the wavelength of incident light / 10 to 10 times.
[0013]In the formation method of the sensor structure according to claim 4, a silicon oxide film is formed on a sensor surface, and hemispherical grain polysilicon is formed on it.
Hemispherical grain polysilicon is formed as a thing of fine particle diameter. A silicon oxide film

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is etched from the gap between this hemispherical grain polysilicon. A sensor surface is locally exposed and a minute protruding part is formed by this etching. In the formation method of the sensor structure according to claim 5, a trench is formed in the sensor surface exposed by etching, and the height of a protruding part is set up by this.

[0014]

[Working example]Hereinafter, the working example of the present invention is described in detail based on Drawings. Fig.1 is a section structure figure of the sensor part in the CCD area sensor concerning the present invention, and a vertical charge transfer section, and shows the A-A' arrowed cross-section of Fig.6. In Fig.1, the P well 13 is laminated via the overflow barrier 12 which consists of P layer on the N type silicon substrate 11.

[0015]HAD (Holl Accumulation Diode) which consists of the electron hole accumulation layer 14 which consists of P^+ layer where the sensor part 1 was formed in the surface side of the P well 13, and the signal-charge accumulation layer 15 which consists of N layer under it It is taking structure and is aiming at improvement in sensitivity, and reduction of dark current. This electron hole accumulation layer 14 and the signal-charge accumulation layer 15 are adjoined, and the channel stop part 16 is formed. The vertical charge transfer section 3 is constituted by the signal-charge transfer region 17 formed in the surface side of the substrate 11, and the transfer electrode 19 consisting of the polysilicon formed via the insulating layer 18 which consists of silicon oxide films (SiO_2) on the substrate surface.

[0016]Between the sensor part 1 and the vertical charge transfer section 3, photoelectric conversion is carried out by the sensor part 1, and the read-out gate section 2 for reading the signal charge accumulated in the signal-charge accumulation layer 15 to the vertical charge transfer section 3 is provided. As a gate electrode of this read-out gate section 2, the transfer electrode 19 is made to serve a double purpose by this example. And it reads except for the sensor part 1, and it provides so that the light-shielding film 20 which consists of aluminum etc. via the insulating layer 18 may cover the outside of the transfer electrode 19 on the gate section 2, the vertical charge transfer section 3, and the channel stop part 16.

[0017]In the above-mentioned sensor structure, even if there are few incident planes of the sensor part 1, a peripheral edge part, preferably the whole incident plane surface are making uneven form. The enlarged section of an example of this uneven form is shown in Fig.2. In the figure, each protruding part 21 which forms uneven form is set up so that conical shape may be made and the pitch p and height h may be 1 of the wavelength of incident light / about 10 to 10 times. As an example, when the wavelength of incident light is 400 nm - 700 nm, moreover, the pitch p of the protruding part 21 and height h are set as about [of pixel size / less than 1/10] at 0.04 micrometer - about 7 micrometers.

[0018]Even if light enters into the sensor part 1 aslant as are mentioned above, and when [of the incident plane of the sensor part 1] the peripheral edge part is making uneven form at least shows to Fig.3, it reflects on the slope (side surface) of the protruding part 21 of conical shape. Then, the reflected light will be reflected towards the lower part [not the upper part of the sensor part 1 but] side. Therefore, since the reflected light in the surface of the sensor part 1 does not repeat a multiple echo between the substrate surface, the lower end surface of the light-shielding film 20, or the transfer electrode 19 in the vertical charge transfer section 3 and an incident thing therefore does not have the reflected light to the vertical charge transfer section 3 side, a smear can be reduced substantially.

[0019]And since it will transmit to the substrate side eventually and photoelectric conversion also of the reflected light component will be carried out by repeating a reflection between the slopes of other protruding parts several times, the reflected light in the slope of the protruding part 21 of conical shape can improve the sensitivity of the sensor part 1. By the way, when the surface of the sensor part 1 is flat, a part of light which entered is transmitted to the substrate

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side, and it serves as a signal charge after photoelectric conversion, is accumulated, and serves as an effective signal. However, since the refractive index of silicon is larger than the transparent membrane (a color filter is included) generally formed on the sensor part 1, the actual condition is being reflected several 10% on the surface of the sensor part 1, and having lost light.

[0020]However, as shown in Fig.3, while transmitting the slope of the protruding part 21 of conical shape, the part will reflect, but the light which entered into the sensor part 1 from the upper part in this example by having made not only the peripheral edge part of the incident plane of the sensor part 1 but the whole incident plane surface into uneven form. It transmits to the substrate side eventually because the reflected light repeats a reflection on the slope concerned several times. Since photoelectric conversion will be performed by this also about the reflected light component which had been lost conventionally, the sensitivity of the sensor part 1 can be improved.

[0021]By forming sufficiently the vertical angle of the conical shape of the protruding part 21 in an acute angle, it becomes possible to suppress an upward reflection of incident light very low, and can improve the sensitivity of the sensor part 1 more. The problem of the flare, such as a cell ghost, is also solvable by the ability of an upward reflection of the sensor part 1 to be reduced. A cell ghost means here the phenomenon which a minute pixel cell is expanded and projects, when the light reflected by the sensor part 1 causes multiple interference by the optical system of the lens etc. which were mounted on the CCD area sensor.

[0022]These operations and effects are effectively exerted by moreover setting the pitch p of the protruding part 21 of conical shape, and height h as about [of pixel size / less than 1/10] at 1 of the wavelength of incident light / about 10 to 10 times, as mentioned previously. incidentally, if the pitch p of the protruding part 21 of conical shape and height h are too small, a reflective effect will be lost to incident light, and if too conversely large, the adverse effect of an and also [sensor form gives compared with the size of an element] will become big.

[0023]Although the protruding part 21 which forms the uneven form of a sensor surface was made into the thing of conical shape in this example, It may be not the thing limited to this form but protruding part of shape of **** abbreviated hemisphere shown, for example in Fig.4 21', and in short, if a sensor surface is not a flat surface but unevenness, the desired end can be attained.

[0024]Next, based on process drawing of Fig.5 (a) - (d), it describes about the formation method of the sensor structure mentioned above. First, in the (a) process 1, on the sensor part 1, it is thinner than the transfer electrode 18 top, for example, grows up a silicon oxide film (5 nm - about 30 nm) (SiO_2). Next, HSG (Hemispherical Grained: hemispherical grain) polysilicon (Poly-Si) is grown up into the whole surface with the fine particle diameter of about 0.1 micrometer.

[0025]If formation of this HSG polysilicon is faced, karyogenesis is carried out at low temperature by performing core attachment using Si_2H_6 gas. And polysilicon is formed at low temperature focusing on this. The grain density and the particle diameter of HSG are decided by Si_2H_6 gas mass flow and substrate temperature. Si_2H_6 partial pressure under core attachment is set to 10^{-5} - 10^{-4}Torr, for example. As a formation method of HSG polysilicon, the thing of disclosure is known [1147 pages - 1151 pages / of the 11 No. (1992) with an academic journal "applied physics" of volume / 61st], for example.

[0026](b) the process 2 -- the silicon oxide film of the gap between HSG polysilicon to the bottom -- a hydrogen fluoride (HF) system -- expose a sensor surface locally by etching with a solution. (c) Form a minute trench in a sensor surface by RIE etching of silicon in the process 3. At this time, unnecessary polysilicon is removed simultaneously. (d) In the process 4, heat-treat the surface for interface-state-density stabilization, carry out NSG/PSG deposition, and

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form the light-shielding film 19 by a henceforth usual CCD process.

[0027]As mentioned above, when forming the uneven form of a sensor surface, a thin silicon oxide film (SiO_2) is grown up on the sensor part 1, HSG polysilicon can be formed on it and uneven form can be easily formed also in the sensor surface where pixel size is small by etching a lower silicon oxide film from the gap between HSG polysilicon, and exposing a sensor surface locally.

[0028]This is not indispensable requirements although it presupposed that a minute trench is formed in the sensor surface exposed locally in the process 3. However, a trench is formed and there is an advantage which can set up the height of a protruding part arbitrarily by adjusting the depth. As a formation method of the uneven form of a sensor surface, it is not restricted to the above-mentioned formation method, and, otherwise, many things are considered. For example, when pixel size is large, it is also possible to form uneven form using lithography and etching.

[0029]The present invention is not limited to application to a CCD area sensor, and a sensor part can apply it to the solid state imaging device at large which has charge transfer sections, such as a CCD line (linear) sensor by which only single-tier powder was arranged.

[0030]

[Effect of the Invention]As described above, according to the invention according to claim 1, by [of each incident plane of a sensor part] having made the peripheral edge part into uneven form at least, Since the light which entered aslant reflects in a sensor part on the side surface of the protruding part which forms uneven form and does not enter into it to a charge transfer section, a smear can be reduced substantially. Since the light reflected on the side surface of the protruding part transmits and photoelectric conversion is eventually carried out by repeating a reflection on the side surface of a yet another protruding part to the substrate side, it is also being able to improve the sensitivity of a sensor part.

[0031]According to the invention according to claim 2, by having made not only the peripheral edge part of each incident plane of a sensor part but the whole surface into uneven form, Since this reflected light transmits and photoelectric conversion is eventually carried out by repeating a reflection on the side surface of a protruding part to the substrate side even if that part reflects, when the light which entered into the sensor part from that upper part transmits the uneven surface of an incident plane, the sensitivity of a sensor part can be improved. According to the invention according to claim 3, the above-mentioned operation and effect can be exerted to the utmost by setting up uneven-shaped the pitch and height of a protruding part 1 of the wavelength of incident light / 10 to 10 times.

[0032]While forming a silicon oxide film on a sensor surface according to the invention according to claim 4, Since a sensor surface is locally exposed and a minute protruding part is formed by forming hemispherical grain polysilicon on it and having etched the silicon oxide film from the gap between this hemispherical grain polysilicon, A sensor part with small pixel size can also form the sensor surface in uneven form easily.

[0033]By having formed the trench in the sensor surface exposed by etching, after etching a silicon oxide film according to the invention according to claim 5, Since the height of a protruding part can be arbitrarily set up by adjusting the depth of the trench, the height of a protruding part can be set up the optimal to the wavelength of incident light.

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a section structure figure showing one working example of the present invention.
[Drawing 2]It is an expanded sectional view of a sensor surface.
[Drawing 3]It is the figure showing behavior of incident light.
[Drawing 4]It is a cross sectional view showing the modification of the form of a protruding part.
[Drawing 5]It is process drawing of the formation method of the sensor structure by the present invention.
[Drawing 6]It is a schematic configuration diagram of a CCD area sensor.
[Drawing 7]It is a cross sectional view of an essential part showing a conventional case.
[Explanations of letters or numerals]
1 Sensor part
3 Vertical charge transfer section
5 Level charge transfer section
11 N type silicon substrate
12 Overflow barrier
14 Electron hole accumulation layer
15 Signal-charge accumulation layer
17 Signal-charge transfer region
19 Transfer electrode
20 Light-shielding film
21 Protruding part

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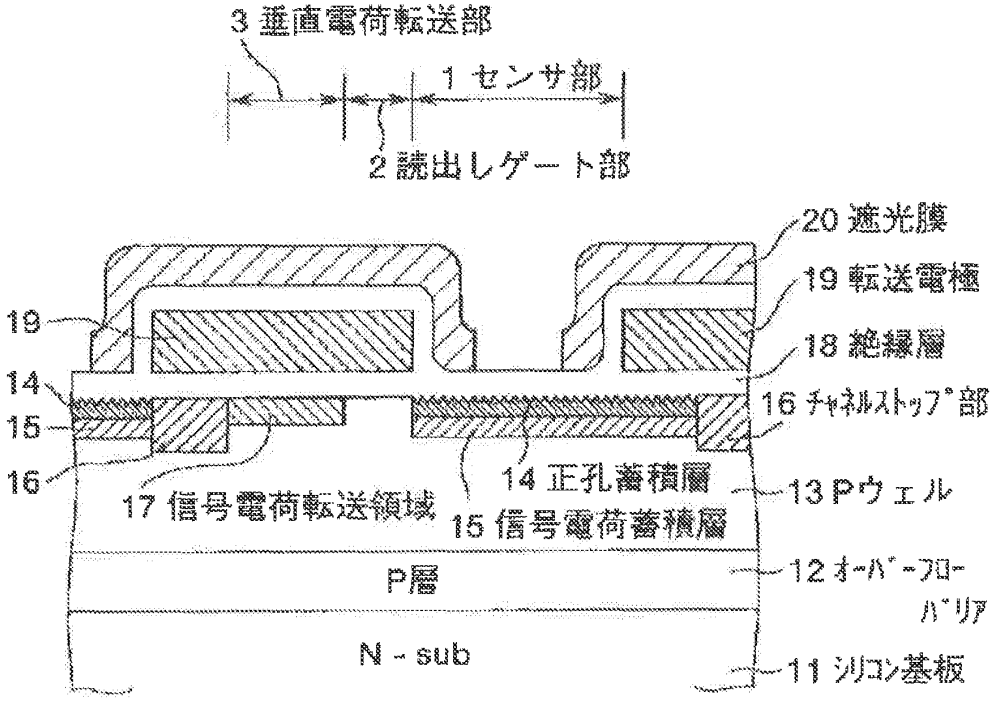
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]



本発明に係る断面構造図

[Drawing 2]

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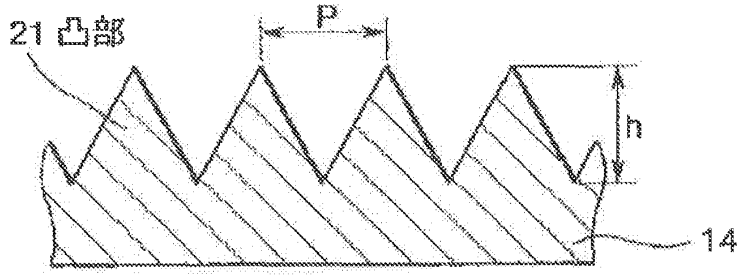
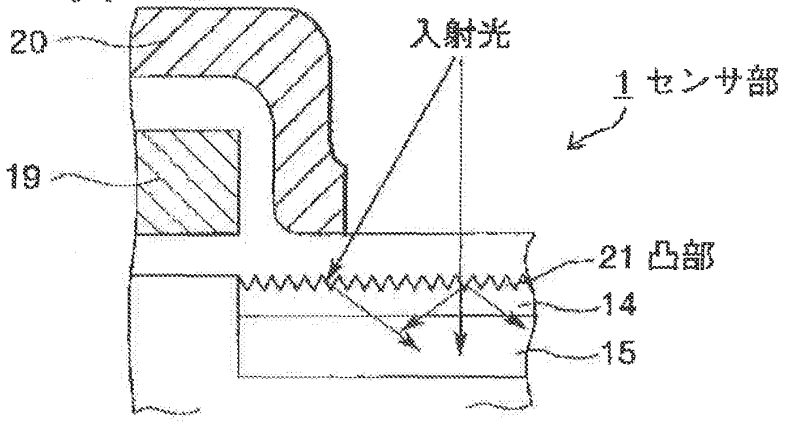


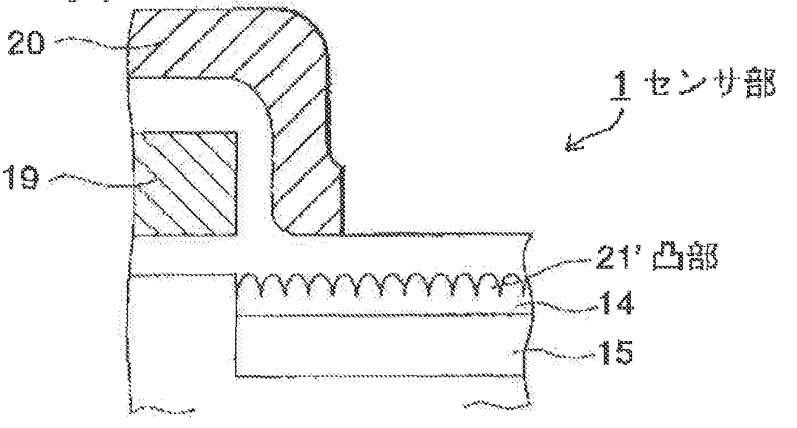
要部の拡大断面図

[Drawing 3]



入射光の振舞いを示す図

[Drawing 4]



変形例を示す断面図

[Drawing 5]

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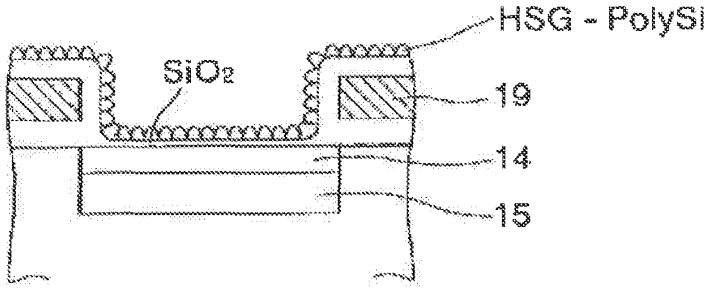
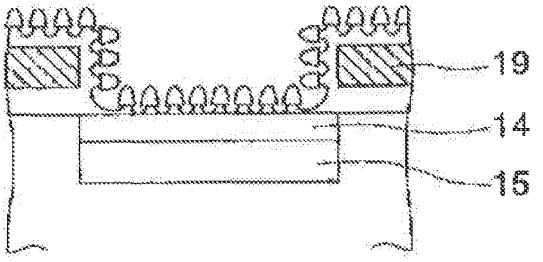
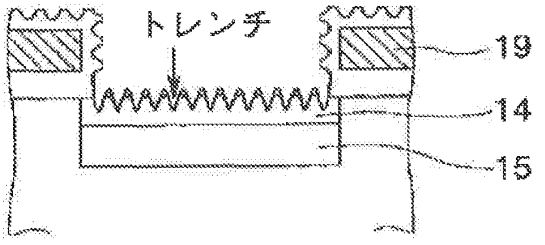


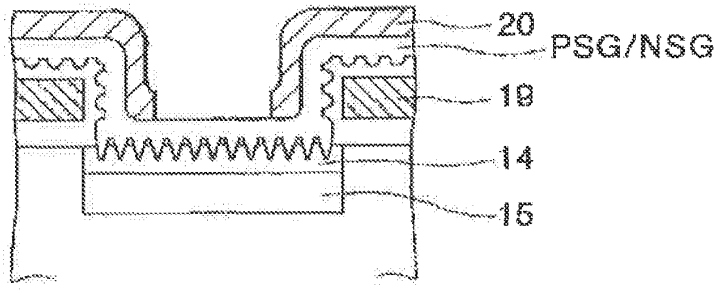
(a) 工程1



(b) 工程2



(c) 工程3



(d) 工程4

本発明に係る工程図

[Drawing 6]

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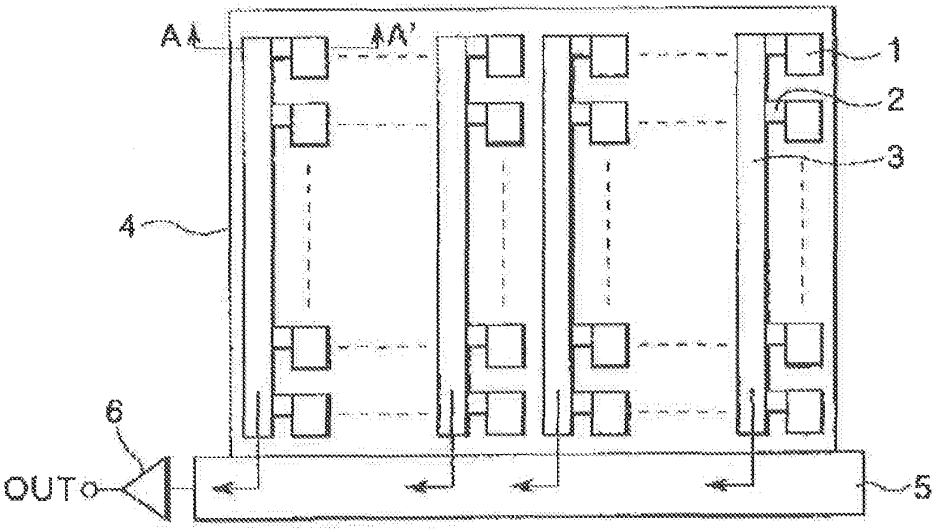
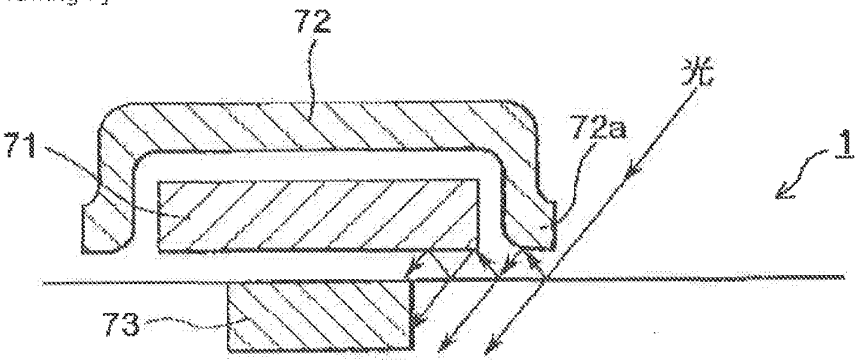


CCDエリアセンサの概略構成図

[Drawing 7]



従来例の要部断面図

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(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開平7－235658
(43)公開日　平成７年(1995)９月５日

(51)Int.Cl.[6]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０１Ｌ　27/148				
Ｈ０４Ｎ　5/335	Ｕ			
		7376－4Ｍ	Ｈ０１Ｌ　27/14	Ｂ

審査請求　未請求　請求項の数５　ＦＤ　（全　６　頁）

(21)出願番号　特願平6－49859

(22)出願日　平成６年(1994)２月22日

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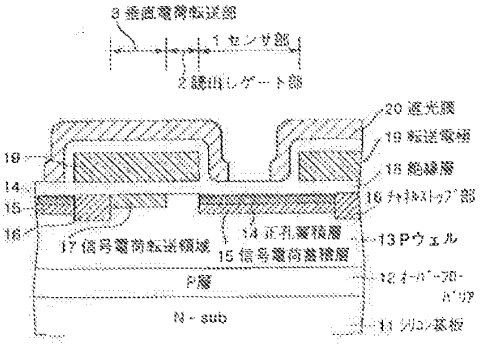
(54)【発明の名称】　固体撮像装置及びそのセンサ構造の形成方法

(57)【要約】
【目的】　電荷転送部における基板表面と遮光膜の下端面又は転送電極との間での多重反射をなくし、スミアの低減を可能とした固体撮像装置のセンサ構造を提供する。
【構成】　縦数個のセンサ部１とこのセンサ部から読み出された信号電荷を転送する垂直電荷転送部３とを具備するＣＣＤエリアセンサにおいて、センサ部１の各々の入射面を凸凹形状に形成し、センサ部１に斜めに入射した光が凸凹形状を形成する凸部で反射して信号電荷転送領域１７に入り込まないようにしたセンサ構造とする。



本発明に係る断面構造図

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【特許請求の範囲】
【請求項１】　入射光を光電変換してその信号電荷を蓄積する少なくとも１列分配列された複数個のセンサ部と、
前記複数個のセンサ部から読み出された信号電荷を転送する電荷転送部とを具備し、
前記複数個のセンサ部の各々の入射面の少なくとも周縁部が凸凹形状をなしていることを特徴とする固体撮像装置。
【請求項２】　前記複数個のセンサ部の各々の入射面全面が凸凹形状をなしていることを特徴とする請求項１記載の固体撮像装置。
【請求項３】　前記凸凹形状の凸部のピッチ及び高さは、入射光の波長の１／１０～１０倍に設定されていることを特徴とする請求項１又は２記載の固体撮像装置。
【請求項４】　入射光を光電変換してその信号電荷を蓄積する少なくとも１列分配列された複数個のセンサ部と、前記複数個のセンサ部から読み出された信号電荷を転送する電荷転送部とを具備した固体撮像装置におけるセンサ構造の形成方法であって、
センサ表面上にシリコン酸化膜を形成するとともに、その上に半球状グレインポリシリコンを形成し、
前記半球状グレインポリシリコンの隙間から前記シリコン酸化膜をエッチングすることを特徴とするセンサ構造の形成方法。
【請求項５】　前記シリコン酸化膜をエッチングした後、そのエッチング部分のセンサ表面にトレンチを形成することを特徴とする請求項４記載のセンサ構造の形成方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、固体撮像装置に関し、特に固体撮像装置におけるセンサ部の構造及びその形成方法に関する。
【０００２】
【従来の技術】固体撮像装置の一例として、例えばインターライン転送方式のＣＣＤ(Charge Coupled Device)エリアセンサの概略構成を図６に示す。同図において、水平及び垂直方向にて２次元配列されて入射光を光電変換し、その信号電荷を蓄積する複数個のセンサ部１と、これらセンサ部１の垂直列毎に配されかつ垂直ブランキング期間の一部にて読出しゲート部２を介して読み出された信号電荷を垂直方向に転送する垂直電荷転送部３とによって撮像部４が構成されている。
【０００３】この撮像部４において、センサ部１は例えばフォトダイオードからなり、垂直電荷転送部３はＣＣＤによって構成されている。センサ部１から垂直電荷転送部３に読み出された信号電荷は、水平ブランキング期間の一部にて１走査線に相当する部分ずつ順に水平転送部５へ転送される。この１走査線分の信号電荷は、水平電荷転送部５によって順次水平方向に転送される。
【０００４】水平電荷転送部５の出力側には、転送されてきた信号電荷を検出して信号電圧に変換する例えばＦＤＡ(Floating Diffusion Amplifier)からなる電荷検出部６が配されている。図７に、センサ部１及び垂直電荷転送部３の断面（図６のＡ－Ａ′矢視断面）構造の要部を示す。
【０００５】
【発明が解決しようとする課題】上記ＣＣＤエリアセンサにおける垂直電荷転送部３では、図７に示すように、センサ部１を除く部分、即ち転送電極７１の外側にアルミニウム等からなる遮光膜７２を形成することで、信号電荷転送領域７３への外部光の入射を遮断する構造を採っている。
【０００６】しかしながら、従来のセンサ構造では、図７から明らかなように、センサ部１の表面が平坦面として形成されているので、センサ部１に光が斜めに入射した場合、センサ表面で反射した光のうち遮光膜７２の下端面７２ａに入射する成分があり、この反射光成分が基板表面と遮光膜７２の下端面７２ａ又は転送電極７１との間で多重反射を繰り返し、最終的に信号電荷転送領域７３に飛び込んで光電子を発生し、スミア成分を増加させるという問題があった。
【０００７】本発明は、上記課題に鑑みてなされたものであり、その目的とするところは、電荷転送部における基板表面と遮光膜の下端面又は転送電極との間での多重反射をなくし、スミアの低減を可能とした固体撮像装置のセンサ構造及びその形成方法を提供することにある。
【０００８】
【課題を解決するための手段】請求項１記載の固体撮像装置は、入射光を光電変換してその信号電荷を蓄積する少なくとも１列分配列された複数個のセンサ部と、この複数個のセンサ部から読み出された信号電荷を転送する電荷転送部とを具備し、複数個のセンサ部の各々の入射面の少なくとも周縁部が凸凹形状をなした構成となっている。
【０００９】請求項２記載の固体撮像装置は、請求項１記載の固体撮像装置において、複数個のセンサ部の各々の入射面全面が凸凹形状をなした構成となっている。請求項３記載の固体撮像装置は、請求項１又は２記載の固体撮像装置において、凸凹形状の凸部のピッチ及び高さが、入射光の波長の１／１０～１０倍に設定された構成となっている。
【００１０】請求項４記載のセンサ構造の形成方法は、センサ表面上にシリコン酸化膜を形成するとともに、その上に半球状グレインポリシリコンを形成し、この半球状グレインポリシリコンの隙間からその下のシリコン酸化膜をエッチングする。請求項５記載のセンサ構造の形成方法は、請求項４記載のセンサ構造の形成方法において、シリコン酸化膜をエッチングした後、そのエッチン

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グ部分のセンサ表面にトレンチを形成する。

【００１１】

【作用】請求項１記載の固体撮像装置において、センサ部に光が斜めに入射したとき、その入射光は入射面周縁部の凸凹形状を形成する凸部の側面で反射することとて、電荷転送部側へは入り込まない。したがって、電荷転送部における基板表面と遮光膜の下端面又は転送電極との間での多重反射は起こらず、よって電荷転送部の転送領域に入射しない。また、凸部の側面で反射した光がさらに他の凸部の側面で反射を繰り返すことで、最終的に基板側へ透過し、光電変換される。その結果、センサ部の感度が向上する。

【００１２】請求項２記載の固体撮像装置において、センサ部にその上方より入射した光は入射面の凸凹面を透過する際に、その一部が反射する。この反射した光は、凸部の側面で反射を繰り返すことで、最終的に基板側へ透過する。すなわち、入射面でのある程度の光の反射は避けられないが、その反射光も最終的にセンサ部へ取り込まれる。その結果、センサ部の感度が向上する。請求項３記載の固体撮像装置では、凸凹形状の凸部のピッチ及び高さを入射光の波長の１／１０～１０倍に設定することで、上記作用が有効に発揮される。

【００１３】請求項４記載のセンサ構造の形成方法において、センサ表面上にシリコン酸化膜を形成し、その上に半球状グレインポリシリコンを形成する。半球状グレインポリシリコンは微小粒径のものとして形成される。この半球状グレインポリシリコンの隙間からシリコン酸化膜をエッチングする。このエッチングにより、センサ表面が局所的に露出し、微小な凸部が形成される。請求項５記載のセンサ構造の形成方法において、エッチングによって露出したセンサ表面にトレンチを形成し、これによって凸部の高さを設定する。

【００１４】

【実施例】以下、本発明の実施例を図面に基づいて詳細に説明する。図１は、本発明に係るＣＣＤエリアセンサにおけるセンサ部及び垂直電荷転送部の断面構造図であり、図６のＡ－Ａ′矢視断面を示す。図１において、Ｎ型シリコン基板１１上にはＰ型からなるオーバーフローバリア１２を介してＰウェル１３が積層されている。

【００１５】センサ部１は、Ｐウェル１３の表面側に形成されたＰ＋層からなる正孔蓄積層１４と、その下のＮ層からなる信号電荷蓄積層１５とからなるＨＡＤ(Hole Accumulation Diode)構造を採ることで、暗電流の向上と暗電流の低減を図っている。この正孔蓄積層１４及び信号電荷蓄積層１５に隣接してチャネルストップ部１６が形成されている。垂直電荷転送部３は、基板１１の表面側に形成された信号電荷転送領域１７と、基板表面上にシリコン酸化膜(SiO)よりなる絶縁層１８を介して形成されたポリシリコンよりなる転送電極１９とによって構成されている。

【００１６】また、センサ部１と垂直電荷転送部３の間には、センサ部１で光電変換され、信号電荷蓄積層１５に蓄積された信号電荷を垂直電荷転送部３へ読み出すための読出しゲート部２が設けられている。この読出しゲート部２のゲート電極として、本例では転送電極１９が兼用されている。そして、センサ部１を除いて読出しゲート部２、垂直電荷転送部３及びチャネルストップ部１６上には、絶縁層１８を介してアルミニウム等からなる遮光膜２０が転送電極１９の外側を覆うように設けられている。

【００１７】上記のセンサ構造において、センサ部１の入射面の少なくとも周縁部、好ましくは入射面全面が凸凹形状をなしている。この凸凹形状の一例の拡大断面を図２に示す。同図において、凸凹形状を形成する個々の凸部２１は円錐形状をなし、そのピッチｐ及び高さｈが入射光の波長の１／１０～１０倍程度になるように設定されている。一例として、入射光の波長を４００ｎｍ～７００ｎｍとしたとき、凸部２１のピッチｐ及び高さｈは、０．０４μｍ～７μｍ程度で、しかも画素サイズの１／１０程度以内に設定される。

【００１８】上述したように、センサ部１の入射面の少なくとも周縁部が凸凹形状をなしていることにより、図３に示すように、センサ部１に光が斜めに入射しても、円錐状の凸部２１の斜面（側面）で反射する。すると、その反射光はセンサ部１の上方側ではなく、その下方側に向けて反射することになる。したがって、センサ部１の表面での反射光が、垂直電荷転送部３における基板表面と遮光膜２０の下端面又は転送電極１９との間で多重反射を繰り返すことはなく、よってその反射光が垂直電荷転送部３側へ入射することはないので、スミアを大幅に低減できる。

【００１９】しかも、円錐状の凸部２１の斜面での反射光は、他の凸部の斜面との間で反射を何回か繰り返すことによって最終的に基板側へ透過し、反射光成分も光電変換されることになるため、センサ部１の感度を向上できる。ところで、センサ部１の表面が平坦な場合、入射した光の一部は基板側へ透過し、光電変換後信号電荷となって蓄積され、有効な信号となる。しかし、シリコンは屈折率が一般にセンサ部１上に形成される透明膜（カラーフィルタを含む）よりも大きいため、センサ部１の表面で数１０％は反射されてしまい、光を損失しているのが現状である。

【００２０】ところが、本実施例においては、センサ部１の入射面の周縁部のみならず、入射面全面を凸凹形状としたことにより、センサ部１に上方より入射した光は、図３に示すように、円錐状の凸部２１の斜面を透過するとともにその一部が反射することになるが、その反射光が当該斜面での反射を何回か繰り返すことで最終的に基板側へ透過する。これにより、従来損失となっていた反射光成分についても光電変換が行われることになる

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ため、センサ部１の感度を向上できる。

【００２１】なお、凸部２１の円錐状の頂角を十分に鋭角に形成することで、入射光の上方への反射を極めて低く抑えることが可能となり、センサ部１の感度をより向上できることになる。また、センサ部１の上方への反射を低減できることで、セルゴーストなどのフレアの問題も解消できる。ここに、セルゴーストとは、センサ部１で反射した光が、ＣＣＤエリアセンサ上にマウントされたレンズ等の光学系で多重干渉を起こすことにより、微小な画素セルが拡大されて映し出される現象を言う。

【００２２】これらの作用・効果は、円錐状の凸部２１のピッチｐ及び高さｈを、先述した如く入射光の波長の１／１０～１０倍程度に、しかも画素サイズの１／１０程度以内に設定することで有効に発揮される。ちなみに、円錐状の凸部２１のピッチｐ及び高さｈが小さすぎると、入射光に対して反射の効果はなくなり、逆に大きすぎると、素子のサイズに比べてセンサ形状が与える他への悪影響が大きなものとなる。

【００２３】なお、本実施例では、センサ表面の凸凹形状を形成する凸部２１を円錐状のものとしたが、この形状に限定されるものではなく、例えば図４に示す如き略半球状の凸部２１′であっても良く、要は、センサ表面が平坦面でなく、凸凹であれば、所期の目的を達成することができる。

【００２４】次に、上述したセンサ構造の形成方法について、図５（ａ）～（ｄ）の工程図に基づいて説明する。先ず、（ａ）工程１では、センサ部１上に転送電極１８上よりも薄い、例えば５ｎｍ～３０ｎｍ程度のシリコン酸化膜（ＳｉＯ₂）を成長させる。次に、ＨＳＧ（Hemispherical Grained：半球状グレイン）ポリシリコン（Poly-Si）を全面に０．１μｍ程度の微小粒径で成長させる。

【００２５】このＨＳＧポリシリコンの形成に際しては、ＳｉＨ₄ガスを用いて核付けを行うことによって低温で核発生させる。そして、これを中心に低温でポリシリコンの形成を行う。ＨＳＧの粒密度及び粒径は、ＳｉＨ₄ガス流量及び基板温度によって決まる。また、核付け中のＳｉＨ₄分圧は、例えば10^{-3}～10^{-4}Ｔｏｒｒとする。ＨＳＧポリシリコンの形成方法としては、例えば学会誌「応用物理」第６１巻第１１号（１９９２）１１４７頁～１１５１頁に開示のものが知られている。

【００２６】（ｂ）工程２では、ＨＳＧポリシリコンの隙間から、下のシリコン酸化膜をフッ化水素（ＨＦ）系溶液でエッチングすることで、センサ表面を局所的に露出させる。（ｃ）工程３では、シリコンのＲＩＥエッチングにより、センサ表面に微小トレンチを形成する。このとき、不要なポリシリコンは同時に除去される。（ｄ）工程４では、界面準位安定化のため表面を熱処理し、ＮＳＧ／ＰＳＧ積層し、以降通常のＣＣＤプロセスによって遮光膜１９を形成する。

【００２７】上述したように、センサ表面の凸凹形状を

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形成するに際し、センサ部１上に薄いシリコン酸化膜（ＳｉＯ₂）を成長させ、その上にＨＳＧポリシリコンを形成し、ＨＳＧポリシリコンの隙間から下のシリコン酸化膜をエッチングしてセンサ表面を局所的に露出させることで、画素サイズが小さいセンサ表面にも容易に凸凹形状を形成することができる。

【００２８】なお、工程３では、局所的に露出したセンサ表面に微小トレンチを形成するとしたが、これは必須の要件ではない。ただし、トレンチを形成し、その深さを調整することで凸部の高さを任意に設定できる利点がある。また、センサ表面の凸凹形状の形成方法としては、上記の形成方法に限られるものではなく、他にも種々考えられる。例えば、画素サイズが大きいときは、リソグラフィーとエッチングを使用して凸凹形状を形成することも可能である。

【００２９】また、本発明は、ＣＣＤエリアセンサへの適用に限定されるものではなく、センサ部が一列分だけ配列されたＣＣＤライン（リニア）センサ等、電荷転送部を有する固体撮像装置全般に適用し得るものである。

【００３０】

【発明の効果】以上説明したように、請求項１記載の発明によれば、センサ部の各々の入射面の少なくとも周縁部を凸凹形状としたことにより、センサ部に斜めに入射した光が凸凹形状を形成する凸部の側面で反射し、電荷転送部へは入り込まないため、スミアを大幅に低減できることになる。また、凸部の側面で反射した光がさらに他の凸部の側面で反射を繰り返すことで、最終的に基板側へ透過し、光電変換されるため、センサ部の感度を向上できることにもなる。

【００３１】請求項２記載の発明によれば、センサ部の各々の入射面の周縁部のみならず、全面を凸凹形状にしたことにより、センサ部にその上方より入射した光が入射面の凸凹面を透過する際にその一部が反射しても、この反射した光が凸部の側面で反射を繰り返すことで、最終的に基板側へ透過し、光電変換されるため、センサ部の感度を向上できることになる。なお、請求項３記載の発明によれば、凸凹形状の凸部のピッチ及び高さを入射光の波長の１／１０～１０倍に設定することにより、上記の作用・効果を最大限に発揮できることになる。

【００３２】請求項４記載の発明によれば、センサ表面上にシリコン酸化膜を形成するとともに、その上に半球状グレインポリシリコンを形成し、この半球状グレインポリシリコンの隙間からシリコン酸化膜をエッチングするようにしたことにより、センサ表面が局所的に露出し、微小な凸部が形成されるので、画素サイズの小さなセンサ部でも容易にそのセンサ表面を凸凹形状に形成することができる。

【００３３】請求項５記載の発明によれば、シリコン酸化膜をエッチングした後、エッチングによって露出したセンサ表面にトレンチを形成するようにしたことによ

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り、そのトレンチの深さを調整することによって凸部の高さを任意に設定することができるので、入射光の波長に対して凸部の高さを最適に設定できることになる。

【図面の簡単な説明】

【図１】本発明の一実施例を示す断面構造図である。

【図２】センサ表面の拡大断面図である。

【図３】入射光の振舞いを示す図である。

【図４】凸部の形状の変形例を示す断面図である。

【図５】本発明によるセンサ構造の形成方法の工程図である。

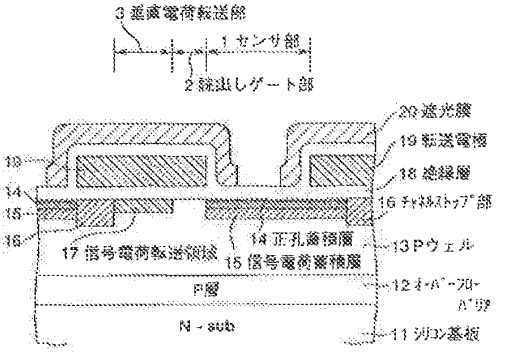
【図６】ＣＣＤエリアセンサの概略構成図である。

【図７】従来例を示す要部の断面図である。

＊【符号の説明】

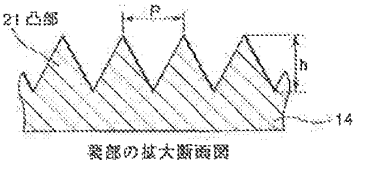
１　センサ部
３　垂直電荷転送部
５　水平電荷転送部
１１　Ｎ型シリコン基板
１２　オーバーフローバリア
１４　正孔蓄積層
１５　信号電荷蓄積層
１７　信号電荷転送領域
１９　転送電極
２０　遮光膜
２１　凸部

【図１】



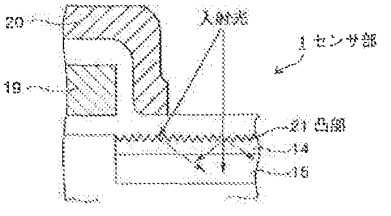
本発明に係る断面構造図

【図２】



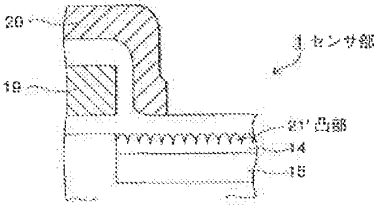
要部の拡大断面図

【図３】



入射光の振舞いを示す図

【図４】



変形例を示す断面図

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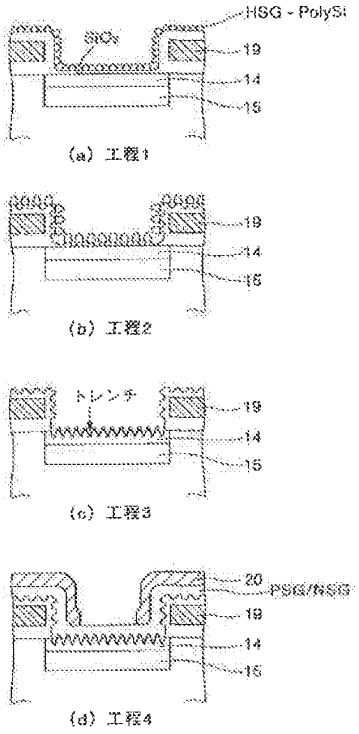
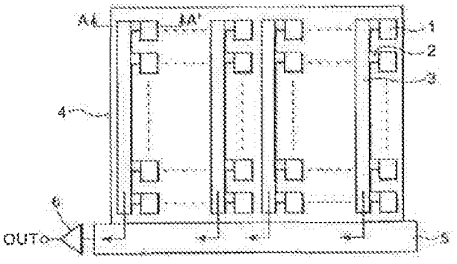
【図5】



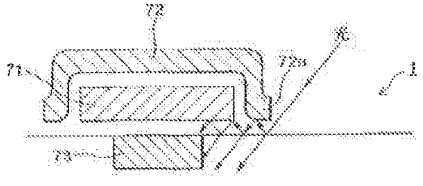
本発明に係る工程図

【図6】



CCDエリアセンサの概略構成図

【図7】



従来例の要部断面図

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(71)Applicant	TOSHIBA CORP
(72)Inventor	OHASHI KENICHI

(54)SOLID-STATE IMAGE PICKUP DEVICE

(57)Abstract

PROBLEM TO BE SOLVED: To provide a solid-state image pickup device, having a small loss in the quantity of incident light and superior sensitivity characteristics, by reducing the reflection of the light at a substrate surface and on a film interface, where the refractive index differs at the inside and on the surface.

SOLUTION: A fine projection 7, having an aspect ratio of at least 1, is provided on the insulating film of the lower layer of an interface having the different refractive index in the passivation film 6 of the solid-state image pickup device, formed on a semiconductor substrate 1 and multilayer insulating films 3, 6 formed on the surface of the silicon semiconductor substrate 1, where a photodiode 2 is formed or the surface of the semiconductor substrate at a period of the wavelength of the incident light or shorter. Although the formation is made in the passivation film in Figure, an antireflection structure can be provided on the surface of the photodiode 2 and on the surface of the insulating film 3. By the formation of the fine projections, the reflection of light, occurring on the surface of the semiconductor substrate or the film interface where the refractive index in the inside differs, can be reduced drastically, thus obtaining a solid-state image pickup device, having small loss in the quantity of incident light and the superior sensitivity characteristics.

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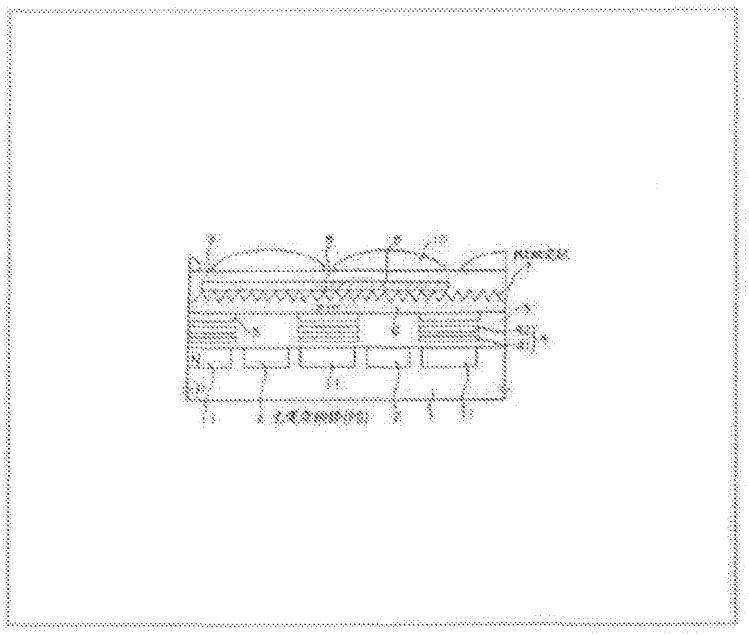

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CLAIMS

[Claim(s)]
[Claim 1]
A semiconductor substrate,
A photoelectric conversion part formed in the aforementioned semiconductor substrate,
A charge transfer section which transmits an electric charge generated from the aforementioned photoelectric conversion part,
It is formed on the aforementioned semiconductor substrate and a passivation film which covers the aforementioned photoelectric conversion part and the aforementioned charge transfer section is provided,
A solid state imaging device, wherein the aforementioned passivation film has the antireflection structure to which array forming of the fine projection was carried out on the surface.
[Claim 2]
The solid state imaging device according to claim 1, wherein array forming of the fine projection which constitutes the aforementioned antireflection structure is carried out by cycle of 0.05-1 micrometer, and one or more aspect ratios.
[Claim 3]
The solid state imaging device according to claim 1, wherein a fine projection which constitutes the aforementioned antireflection structure is arranged at random within the scope of a cycle of 0.05-1 micrometer, and one or more aspect ratios and an aspect ratio changes at random.
[Claim 4]
The solid state imaging device according to claim 1 or 2, wherein an array cycle of a fine projection which constitutes the aforementioned antireflection structure is smaller than wavelength of incident light which enters into the aforementioned photoelectric conversion part and generates an electric charge.
[Claim 5]
A semiconductor substrate,
A photoelectric conversion part formed in the aforementioned semiconductor substrate,
A charge transfer section which transmits an electric charge generated from the aforementioned photoelectric conversion part is provided,
A solid state imaging device, wherein the aforementioned photoelectric conversion part has the antireflection structure to which array forming of the fine projection was carried out on the surface.
[Claim 6]
The solid state imaging device according to claim 5, wherein an array cycle of a fine projection which constitutes the aforementioned antireflection structure is smaller than wavelength of incident light which enters into the aforementioned photoelectric conversion part and generates an electric charge.
[Claim 7]

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A semiconductor substrate,
A photoelectric conversion part formed in the aforementioned semiconductor substrate,
A charge transfer section which transmits an electric charge generated from the aforementioned photoelectric conversion part is provided,
A solid state imaging device, wherein an insulator layer on that lower layer side has the antireflection structure by which array forming of the fine projection was carried out to that surface in an interface of an insulator layer which consists of a refractive index which a multilayer insulator layer which consists of a transparent material is formed in the upper layer of the aforementioned photoelectric conversion part, and is different among this multilayer insulator layer.

[Claim 8]

The solid state imaging device according to claim 7, wherein an array cycle of a fine projection which constitutes the aforementioned antireflection structure is smaller than wavelength of incident light which enters into the aforementioned photoelectric conversion part and generates an electric charge.

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]
The present invention relates to a solid state imaging device, and relates to the solid state imaging device which was excellent in the sensitivity characteristic provided with the antireflection layer which has a new structure especially.
[0002]
[Description of the Prior Art]
In solid state imaging devices, such as a charge coupled device (CCD:Charged Coupled Device) and a CMOS (Complementary Metal Oxide Semiconductor) sensor, Usually, insulation films, such as SiO_2 and SiN, are formed in the surface as a passivation film. When light entered into the solid state imaging device, the light reflex in the interface happened for the refractive index difference of air (n= 1) and SiN (n-2.0 (abbreviation 2.0)), and the reflected light did not reach the photo-diode formed in the bottom of it, but, as a result, there were problems -- sufficient sensitivity is not obtained -- to incident light quantity.
[0003]
The CCD area image sensor shown in Fig.9 in the conventional solid state imaging device is made into an example, and is described. A CCD area image sensor is used for a digital camera or video, for example. This area image sensor is formed in the p type semiconductor substrate 101, for example. A plurality of n type impurity diffusion regions are formed in the surface area of the semiconductor substrate 101. One kind of them constitutes the photo-diode 102, and is arranged by matrix form to the predetermined region of the semiconductor substrate 101. The photo-diode 102 is called pixel and constitutes the photoelectric conversion part. Since the photo-diode 102 is arranged by matrix form, it consists of a plurality of sequences, and each sequence is called pixel row. Between each pixel row, other n type impurity diffusion regions which constitute CCD register 111 are formed. On CCD register 111, the electrode 104 laminated via the insulator layer is formed. The first electrode 141 that becomes right above CCD register 111 from polysilicon etc. is formed, and the second electrode 142 consisting of polysilicon etc. is formed on it. The electrode 104 and CCD register 111 constitute the vertical charge transfer register. The electric charge converted by the first electrode 141 with the photo-diode 102 (photoelectric conversion part), It is shifted to CCD register 111, and the inside of a vertical charge transfer register is sent by the second electrode 142, and it is sent to a horizontal charge transfer register (not shown), and is outputted to outside from this horizontal charge transfer register.
[0004]
The SiO_2 insulator layer 103 accumulates with a CVD method etc. on the semiconductor substrate 101 so that the photo-diode 102, and level and a vertical charge transfer register may be covered. On this insulator layer 103, the light-shielding film 105 which consists of

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aluminum etc. so that the photo-diode 102 may not be covered is selectively formed so that it may be level and a vertical charge transfer register may be covered. Next, the passivation film 106 consisting of a silicon nitride film (SiN) etc. is formed on the semiconductor substrate 101 so that the light-shielding film 105 and the insulator layer 103 may be covered. The color filter 108 of red (R) green (G) blue (B) is formed via the color filter flattening film 112 which consists of organic resin on this passivation film 106. On the passivation film 106, the color filter flattening film 112 which consists of organic resin is formed. The color filter 108 is fixed with the insulator layer 109 consisting of organic resin, and the micro lens 110 is formed on the insulator layer 109. And the color filter 108 and the micro lens 110 are formed so that it may be arranged on the photo-diode 102.

[0005]

[Problem to be solved by the invention]

In such a conventional solid state imaging device, in order to improve conversion efficiency, to be converted in a photoelectric conversion part is required, without an incident light reflecting. As the method of the antireflection for reflecting few as much as possible, coating of the antireflection film using a monolayer or a multilayer interference film is known. Although these have the antireflection characteristic excellent in the specific wavelength band, they are difficult for forming the antireflection film outstanding in the visible light whole region. These methods are sensitive to the film thickness of each film, and in order to maintain the stable antireflection characteristic, it has many problems, like manufacturing management is difficult and there is. The present invention is made by such a situation, makes very small a reflection of the light which occurs by the membrane interface from which the refractive index of a substrate surface and an inside differs, and its loss of incident light quantity is small, and it provides the solid state imaging device excellent in the sensitivity characteristic.

[0006]

[Means for solving problem]

The present invention is a passivation film of the solid state imaging device formed on the semiconductor substrate. It is characterized by forming an one or more-aspect ratio minute projection in the lower layer insulator layer of an interface in which refractive indices differ among the multilayer insulator layers formed on the silicon surface in which the photo-diode was formed, or the silicon surface with the cycle below the wavelength of incident light, such as visible light and infrared rays. Since a reflection of the light which occurs by formation of a fine projection by the membrane interface from which the refractive index of a passivation film, a semiconductor substrate surface, or an inside differs can be made very small, the solid state imaging device with which the loss of incident light quantity was small excellent in the sensitivity characteristic is obtained. Silicon oxide films (SiO_2), such as a silicon nitride film (SiN) or PSG, etc. are used for the passivation film used for the present invention.

The photoelectric conversion part by which the solid state imaging device of the present invention was formed in the semiconductor substrate and the aforementioned semiconductor substrate, It is formed the charge transfer section which transmits the electric charge generated from the aforementioned photoelectric conversion part, and on the aforementioned semiconductor substrate, The passivation film which covers the aforementioned photoelectric conversion part and the aforementioned charge transfer section is provided, and the aforementioned passivation film is characterized by having the antireflection structure to which array forming of the fine projection was carried out. The array forming of the fine projection which constitutes the aforementioned antireflection structure may be made to be carried out by the cycle of 0.05-1 micrometer, and one or more aspect ratios. The fine projection which constitutes the aforementioned antireflection structure is arranged at random within the scope of the cycle of 0.05-1 micrometer, and one or more aspect ratios, and it may be made for an

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aspect ratio to change at random. The array cycle of the fine projection which constitutes the aforementioned antireflection structure is smaller than the wavelength of the incident light which enters into the aforementioned photoelectric conversion part and generates an electric charge, is also made, and is good.

[0007]

The solid state imaging device of the present invention possesses a semiconductor substrate, the photoelectric conversion part formed in the aforementioned semiconductor substrate, and the charge transfer section which transmits the electric charge generated from the aforementioned photoelectric conversion part, and the aforementioned photoelectric conversion part is characterized by having the antireflection structure to which array forming of the fine projection was carried out on the surface. The array cycle of the fine projection which constitutes the aforementioned antireflection structure may be made smaller than the wavelength of the incident light which enters into the aforementioned photoelectric conversion part and generates an electric charge.

The photoelectric conversion part by which the solid state imaging device of the present invention was formed in the semiconductor substrate and the aforementioned semiconductor substrate, In the interface of the insulator layer which consists of a refractive index which the charge transfer section which transmits the electric charge generated from the aforementioned photoelectric conversion part is provided, and the multilayer insulator layer which consists of a transparent material is formed in the upper layer of the aforementioned photoelectric conversion part, and is different among this multilayer insulator layer, The insulator layer on the lower layer side is characterized by having the antireflection structure to which array forming of the fine projection was carried out on the surface. The array cycle of the fine projection which constitutes the aforementioned antireflection structure may be made smaller than the wavelength of the incident light which enters into the aforementioned photoelectric conversion part and generates an electric charge. When there is unevenness (fine projection) below the wavelength of incident light, in order that light may regard it as the layer which has an inclination where a refractive index is smooth and changes from the bottom part of a projection to a tip (Graded Index), there is no rapid refractive index change in an interface, and it is effective in the loss in the case of a penetration almost being lost.

[0008]

[Mode for carrying out the invention]

Hereinafter, an embodiment of the invention is described with reference to Drawings.

First, a first working example is described with reference to Fig.1 thru/or Fig.4.

The plan view of the semiconductor substrate in which Fig.1 describes the cross sectional view of a solid state imaging device, Fig.2 describes the manufacturing process cross sectional view of the solid state imaging device of Fig.1, and Fig.3 describes the photo-diode (photoelectric conversion part) and electrode of a solid state imaging device of Fig.1, and Fig.4 are the plan views of the semiconductor substrate which describes the color filter of the solid state imaging device of Fig.1. The cross sectional view of the portion which is along the A-A' line of Fig.3 is shown in Fig.1. The CCD area image sensor shown in Fig.1 in this working example is made into an example, and is described.

[0009]

A CCD area image sensor is used for a digital camera or video, for example. This area image sensor is formed in the p type semiconductor substrate 1, for example. A plurality of n type impurity diffusion regions are formed in the surface area of the semiconductor substrate 1. The part constitutes a plurality of photo-diodes (PD) 2, and is arranged by matrix form to the predetermined region of the semiconductor substrate 1. The photo-diode 2 is called a photoelectric conversion pixel and what is called pixel, and constitutes the photoelectric

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conversion part. Since the photo-diode 2 is arranged by matrix form, it consists of a plurality of sequences, and each sequence is called pixel row. Between each pixel row, other different n type impurity diffusion regions from the photo-diode which constitutes CCD register 11 are formed. On CCD register 11, the electrode 4 laminated via the insulator layer 3 which consists of SiO_2 etc. is formed. The first electrode 41 that becomes right above CCD register 11 from polysilicon etc. among the laminated electrodes 4 is formed, and the second electrode 42 which consists of polysilicon etc. via the insulator layer 3 is formed on it. The electrode 4 and CCD register 11 constitute the vertical charge transfer register. The end is made to overlap the two electrodes 41 and 42, and they are formed. The electric charge converted with the photo-diode 2 (photoelectric conversion part), It is shifted to CCD register 11 by the first electrode 41, and the inside of a vertical charge transfer register is transmitted by the 1st and the second electrodes 41 and 42, and it is sent to a horizontal charge transfer register (not shown), and is further outputted to outside from this horizontal charge transfer register.

[0010]

The insulator layer 3 accumulates with a CVD method etc. on the semiconductor substrate 1 so that the photo-diode 2, and level and a vertical charge transfer register may be covered. On this insulator layer 3, the light-shielding film 5 which consists of aluminum etc. so that the photo-diode 2 may not be covered is selectively formed so that it may be level and a vertical charge transfer register may be covered. Next, the passivation film 6 consisting of a silicon nitride film (SiN) etc. is formed on the semiconductor substrate 1 so that the light-shielding film 5 and the insulator layer 3 may be covered. Other materials, such as a silicon oxide film, can be used for this passivation film. The color filter 8 of red (R) green (G) blue (B) is formed on this passivation film 6. The color filter 8 is fixed with the insulator layer 9 consisting of organic resin, and the micro lens 10 is formed on the insulator layer 9. The color filter 8 and the micro lens 10 are arranged so that the photo-diode 2 may be covered.

In this working example, the antireflection structure which is the characteristics of the present invention is formed in a passivation film. As shown in the figure, the fine projection 7 is formed in the surface of the passivation film 6 as an antireflection structure. As for the passivation film 6, the fine projection 7 is formed in thickness d of the inner surface of thickness D. Therefore, the portion of lower thickness h mainly has a function as a passivation film.

[0011]

If the fine projection which constitutes an antireflection structure is formed so that it may become smaller than the wavelength of an incident light at a photo-diode (photoelectric conversion part), an efficient antireflection operation will be obtained. Therefore, in this working example, from the inside of the cycle of 0.05-1 micrometer, and one or more aspect ratios, a fine projection chooses a predetermined value and array forming is carried out. However, by the present invention, a fine projection can be arranged at random within the scope of the cycle of 0.05-1 micrometer, and one or more aspect ratios, and it can also be constituted so that an aspect ratio may be changed at random.

Next, the arrangement on the semiconductor substrate of the CCD area image sensor shown in Fig.1 with reference to Fig.3 is described. The electrode 4 formed on the sequence of the photo-diode (PD) 2 and the CCD register is alternately located in a line with the sensor part of the semiconductor substrate 1. The electric charge converted with the photo-diode 2 (photoelectric conversion part) as mentioned above is shifted to a CCD register, the inside of a vertical charge transfer register is transmitted to it by the electrode 4, it is sent to the horizontal charge transfer register 12, and is outputted to outside from this horizontal charge transfer register 12. The peripheral circuit part which drives an I/O terminal and an electrode is formed in the region in which the sensor part of the semiconductor substrate 1 is not formed.

[0012]

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Next, the color filter attached to the sensor part of Fig.3 with reference to Fig.4 is described. The color filter 8 is formed on a passivation film so that the photo-diode 2 top and its neighborhood may be covered. The color of a filter is arranged so that it may differ every photo-diode 2. As shown in the figure, the color filter 8 of red (R) green (G) blue (B) is formed on the four photo-diodes 2, respectively. Considering the four color filters 8 shown in the figure as one color pattern, this color pattern covers a substrate top and the color filter 8 is formed on the surface of a CCD area image sensor. The color filter 8 is fixed with the insulator layer consisting of organic resin, and a micro lens is formed on this insulator layer. A micro lens is formed so that it may be arranged right above the photo-diode 2.

[0013]

Next, the manufacturing process of the CCD area image sensor shown in Fig.1 with reference to Fig.2 is described. First, the impurity diffusion region which constitutes the photo-diode 2 and CCD area image sensor 11 in the semiconductor substrate 1 which consists of silicon is formed, The electrode 4 covered with the insulator layer 3 which consists of SiO_2 etc. is formed on the semiconductor substrate 1, and the light-shielding film 5 of aluminum is formed via the insulator layer 3 on the electrode 4. The photo-diode 2 which carries out photoelectric conversion of the light which entered into the semiconductor substrate 1 is provided by matrix form, and a light-shielding film is formed in the electrode 4 for making an electric charge transmit in the form which adjoins a transverse direction and the portion corresponding to this. And the silicon nitride film (SiN) which constitutes the passivation film 6 is made to deposit about 400 nm in thickness on the insulator layer 3 (Fig.2 (a)).

[0014]

Next, 200 nm of film thickness applied EB (electron beam) resist to the semiconductor substrate 1, and one side performed EB drawing and development for this, and formed the resist pattern 14 of island shape so that space with an adjacent pattern might be set to 100 nm at 100 nm (Fig.2 (b)). Next, use the resist pattern of island shape as a mask, and by RIE (Reactive Ion Etching), It etches until a resist is lost by CF_4/Ar=20/80sccm, pressure 10Torr, and the power 200W (). That is, SiN/resist carries out low selection-ratio etching, and it forms the pattern of the fine projection 7 of the cycle of 200 nm, and the aspect ratio 1.5 in a silicon nitride film (SiN). Thus, the antireflection structure which consists of the fine projection 7 is obtained on the surface of the semiconductor substrate 1 (Fig.2 (c)).

The insulator layer 9 and the micro lens 10 which consists of the color filter 8 and organic resin are formed on the pattern of the fine projection 7, and a CCD area image sensor is completed (refer to Fig.1).

[0015]

By forming a fine projection pattern on the passivation film of a semiconductor substrate surface, the interface reflection with a color filter was reduced and the sensitivity characteristic improved 8% conventionally as compared with the CCD area image sensor of structure.

the insulator layer (organic resin --) which is formed on the passivation film (refractive index n= 1.9-2.0) and the surface of the CCD area image sensor formed on the semiconductor substrate, and fixes a color filter In n= 1.5, although refractive indices differ, a reflection of the light which occurs by a passivation film can be made very small by having formed an one or more-aspect ratio fine projection in the lower layer insulator layer (passivation film) of the interface with the cycle below the wavelength of incident light. Therefore, the CCD area image sensor with which the loss of incident light quantity was small excellent in the sensitivity characteristic is obtained. Thus, in the whole region of a light range (400 nm - 700 nm), the surface reflectance of the passivation film was able to be reduced to 2% or less by forming a fine projection in a passivation film. Since a reflection of the incident light which happens by the interface from which a refractive index differs can be reduced according to this method,

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without using methods, such as formation of a multilayer interference film, the CCD area image sensor excellent in the sensitivity characteristic is obtained without changing the existing film constitution largely.

[0016]

Next, a second working example is described with reference to Fig.5 and Fig.6.

Fig.5 and Fig.6 are the cross sectional views of a solid state imaging device. A CCD area image sensor is made into an example, and this working example is described. This area image sensor is formed in the p type semiconductor substrate 21, for example. A plurality of n type impurity diffusion regions are formed in the surface area of the semiconductor substrate 21. The part constitutes a plurality of photo-diodes (PD) 22, and is arranged by matrix form to the predetermined region of the semiconductor substrate 21. The photo-diode 22 is called a photoelectric conversion pixel and what is called pixel, and constitutes the photoelectric conversion part. Since the photo-diode 22 is arranged by matrix form, it consists of a plurality of sequences, and each sequence is called pixel row. Between each pixel row, a different n type impurity diffusion region from the photo-diode which constitutes CCD register 31 is formed. On CCD register 31, the electrode 24 laminated via the insulator layer 23 which consists of SiO_2etc. is formed. The first electrode 241 that becomes right above CCD register 31 from polysilicon etc. among the laminated electrodes 24 is formed, and the second electrode 242 which consists of polysilicon etc. via the insulator layer 23 is formed on it. The electrode 24 and CCD register 31 constitute the vertical charge transfer register. Photo-diode 22 (photoelectric conversion part)

The electric charge come out of and converted is shifted to CCD register 31 by the first electrode 241, the inside of a vertical charge transfer register is transmitted to it by the second electrode 242, it is sent to a horizontal charge transfer register (not shown), and is further outputted to outside from a horizontal charge transfer register.

[0017]

The above-mentioned insulator layer 23 accumulates with a CVD method etc. on the semiconductor substrate 21 so that the photo-diode 22, and level and a vertical charge transfer register may be covered. On this insulator layer 23, the light-shielding film 25 which consists of aluminum etc. so that the photo-diode 2 may not be covered is selectively formed so that it may be level and a vertical charge transfer register may be covered. Next, the passivation film 26 consisting of a silicon nitride film (SiN) etc. is formed on the semiconductor substrate 21 so that the light-shielding film 25 and the insulator layer 23 may be covered. The color filter 28 of red (R) green (G) blue (B) is formed on this passivation film 26. The color filter 28 is fixed with the insulator layer 29 consisting of organic resin, and the micro lens 30 is formed on the insulator layer 29. The color filter 28 and the micro lens 30 are arranged so that the photo-diode 22 may be covered.

[0018]

The way (micro-lens 30-color filter 28-passivation film 26-insulator layer 23-photo-diode 22) along which the light from the outside passes, When the passivation film 26 is a silicon nitride film (SiN), an opportunity for incident light to reflect increases more than other films largely (n= 1.9-2.0), and the refractive index n has become one of the causes which degrades a sensitivity characteristic. Therefore, the passivation film of this portion was removed and it was possible to form the portion (opening) which does not have a film in a passivation film. However, if an opening is formed in this way, the color filter by which formation arrangement is carried out will not be stably installed on it. Then, the ground in which a color filter was placed formed the color filter flattening film on the passivation film evenly conventionally. In this working example, it has such a structure. Organic resin whose refractive index n is about 1.5 is used for the flattening film.

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Therefore, in this working example, the opening 261 is provided into the portion of the light path which is on the passivation film 26 which used the silicon nitride film on the photo-diode 22. And the light-shielding film 25 also covers the side surface of a light path, and makes shielding effects high so that the insulator layer 23 which covers the laminated electrode 24 may be wrapped. The insulator layers 33, such as a silicon oxide film, are formed in the portion in contact with the photo-diode 22 which is the lower part of a light path by the CVD method etc., and the color filter flattening film 34 consisting of organic resin etc. is formed on this insulator layer 33 and the passivation film 26.

[0019]

In this working example, the antireflection structure which is the characteristics of the present invention is formed in the surface portion of the insulator layer 33 which consists of a silicon oxide film. As shown in the figure, the fine projection 27 is formed in the surface of the insulator layer 33 provided by the light path as an antireflection structure. If the array cycle of the fine projection 27 which constitutes an antireflection structure is made smaller to the photo-diode 22 than the wavelength of an incident light, an efficient antireflection operation will be obtained. Therefore, in this working example, from the inside of the cycle of 0.05-1 micrometer, and one or more aspect ratios, a fine projection chooses a predetermined value and array forming is carried out. However, a fine projection can be arranged at random within the scope of the cycle of 0.05-1 micrometer, and one or more aspect ratios, and it can also be constituted so that an aspect ratio may be changed at random.

The color filter flattening film (refractive-index n= abbreviation 1.5) of the CCD area image sensor formed on the semiconductor substrate, The insulator layer (n= 1.45) which consists of the silicon oxide film which touches this differs that the difference is small in the refractive index, Although it is in the environment where a reflection occurs, a reflection of the light which occurs with an insulator layer can be made very small by having formed an one or more-aspect ratio fine projection in the lower layer insulator layer of the interface with the predetermined cycle below the wavelength of incident light. Therefore, the CCD area image sensor with which the loss of incident light quantity was small excellent in the sensitivity characteristic is obtained. Thus, in the whole region of a light range (400 nm - 700 nm), the surface reflectance of the passivation film was able to be reduced to 2% or less by forming a fine projection in a passivation film. Since a reflection of the incident light which happens by the interface from which a refractive index differs can be reduced according to this method, without using methods, such as formation of a multilayer interference film, the CCD area image sensor excellent in the sensitivity characteristic is obtained without changing the existing film constitution largely.

[0020]

In order to form an opening in a passivation film, after making a passivation film deposit, two kinds of methods, the case where etch this selectively and opening formation is carried out, and when carrying out the mask of the predetermined portion to an opening configuration from the beginning and depositing a passivation film, can be used.

As for the solid state imaging device shown in Fig.5, the opening is formed in the passivation film. However, in this working example, it can also be used as it is without forming an opening in a passivation film. Fig.6 is an example using a passivation film without an opening. In this example, the process of forming an opening in a passivation film can be skipped.

[0021]

Next, the 3rd working example is described with reference to Fig.7.

Fig.7 is a cross sectional view of a solid state imaging device. A CCD area image sensor is made into an example, and this working example is described. This area image sensor is formed in the p type semiconductor substrate 41, for example. A plurality of n type impurity

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diffusion regions are formed in the surface area of the semiconductor substrate 41. The part constitutes a plurality of photo-diodes (PD) 42, and is arranged by matrix form to the predetermined region of the semiconductor substrate 41. The photo-diode (pixel) 42 constitutes the photoelectric conversion part. Since the photo-diode 42 is arranged by matrix form, it consists of a plurality of sequences, and each sequence is called pixel row. Between each pixel row, a different n type impurity diffusion region from the photo-diode which constitutes CCD register 51 is formed. On CCD register 51, the electrode 44 laminated via the insulator layer 43 which consists of SiO_2 etc. is formed. The first electrode 441 that becomes right above CCD register 51 from polysilicon etc. among the laminated electrodes 44 is formed, and the second electrode 442 which consists of polysilicon etc. via the insulator layer 43 is formed on it. The electrode 44 and CCD register 51 constitute the vertical charge transfer register. The electric charge converted with the photo-diode 42 (photoelectric conversion part), It is shifted to CCD register 51 by the first electrode 441, and the inside of a vertical charge transfer register is transmitted by the second electrode 442, and it is sent to a horizontal charge transfer register (not shown), and is further outputted to outside from a horizontal charge transfer register.

[0022]

The above-mentioned insulator layer 43 accumulates with a CVD method etc. on the semiconductor substrate 41 so that the photo-diode 42, and level and a vertical charge transfer register may be covered. On this insulator layer 43, the light-shielding film 45 which consists of aluminum etc. so that the photo-diode 42 may not be covered is selectively formed so that it may be level and a vertical charge transfer register may be covered. Next, the passivation film 46 consisting of a silicon nitride film (SiN) etc. is formed on the semiconductor substrate 41 so that the light-shielding film 45 and the insulator layer 43 may be covered. They are red (R) green (G) and blue on this passivation film 46. The color filter 48 of (B) is formed. The color filter 48 is fixed with the insulator layer 49 consisting of organic resin, and the micro lens 50 is formed on the insulator layer 49. The color filter 48 and the micro lens 50 are arranged so that the photo-diode 42 may be covered.

[0023]

The way along which the light from the outside passes like a second working example, Since the refractive index n is one of the causes which an opportunity for incident light to reflect increases [**] more than other films largely (n= 1.9-2.0), and degrades a sensitivity characteristic when a passivation film is a silicon nitride film (SiN), In this working example, the passivation film of this portion is removed and the portion (opening 461) which does not have a film in the passivation film 46 is formed. And the ground in which a color filter is placed forms the color filter flattening film 54 on the passivation film 46 evenly. Organic resin whose refractive index n is about 1.5 is used for the flattening film 54. The light-shielding film 45 also covers the side surface of a light path, and makes shielding effects high so that the insulator layer 43 which covers the electrode 44 may be wrapped. The insulator layers 53, such as a silicon oxide film, are formed in the portion in contact with the photo-diode 42 which is the lower part of a light path by the CVD method etc., and the above-mentioned color filter flattening film 54 is formed on this insulator layer 53 and the passivation film 46.

In this working example, the antireflection structure which is the characteristics of the present invention is formed in the surface portion of the semiconductor substrate 41 which consists of silicon. As shown in the figure, the fine projection 47 is formed in the surface of the photo-diode 42 exposed to a light path as an antireflection structure. If the array cycle of the fine projection 47 which constitutes an antireflection structure is made smaller to the photo-diode 42 than the wavelength of an incident light, an efficient antireflection operation will be obtained. Therefore, in this working example, from the inside of the cycle of 0.05-1

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micrometer, and one or more aspect ratios, a fine projection chooses a predetermined value and array forming is carried out. However, a fine projection can be arranged at random within the scope of the cycle of 0.05-1 micrometer, and one or more aspect ratios, and it can also be constituted so that an aspect ratio may be changed at random.

[0024]

The insulator layer (n= 1.45) 53 and the semiconductor substrate (n> 3) 41 which consists of a silicon oxide film which touch the color filter flattening film formed on the semiconductor substrate differ in the refractive index largely, Although it is in the environment where a reflection occurs, a reflection of the light which occurs with a semiconductor substrate can be made very small by having formed the one or more-aspect ratio fine projection 47 in the photo-diode 42 of the lower layer semiconductor substrate 41 of the interface with the predetermined cycle below the wavelength of incident light. Therefore, the CCD area image sensor with which the loss of incident light quantity was small excellent in the sensitivity characteristic is obtained. Thus, in the whole region of a light range (400 nm - 700 nm), the surface reflectance of the passivation film was able to be reduced to 2% or less by forming a fine projection in a passivation film. Since a reflection of the incident light which happens by the interface from which a refractive index differs can be reduced according to this method, without using methods, such as formation of a multilayer interference film, the CCD area image sensor excellent in the sensitivity characteristic is obtained without changing the existing film constitution largely.

The method of forming an opening in a passivation film is as having described in the second working example.

Although the antireflection structure which reduces a reflection of the incident light which happens by the interface from which a refractive index differs is formed in one place in a second working example and the 3rd working example, respectively, in the interface from which a refractive index differs in the present invention, the place where environment is bad is able to apply to all with plurality. For example, an antireflection structure can be provided to two places so that a second working example and the 3rd working example may be doubled.

[0025]

Next, the 4th working example is described with reference to Fig.8.

Fig.8 is a cross sectional view of a solid state imaging device. In this working example, a CCD linear image sensor is described as a solid state imaging device. The photo-diode (pixel) of a photoelectric conversion part has arranged the linear image sensor to one dimension. To the semiconductor substrate 61, provide linearly the photo-diode 62 used as a photoelectric conversion part, and to it by the same method as a first working example, The electrode 64 consisting of the polysilicon etc. which comprised the first electrode 641 and the second electrode 642 was formed, and the aluminum light-shielding film 65 was formed via the insulator layer 63 which consists of a silicon oxide film. CCD register (n type impurity diffusion region) 68 which constitutes a charge transfer register with the electrode 64 is formed in the surface area of the semiconductor substrate 61 under the electrode 64. The silicon oxide film (PSG) of the phosphorus dope was formed in the passivation film 66 used as the topmost film at 400 nm in thickness.

The electric charge converted with the photo-diode 62 (photoelectric conversion part) is shifted to CCD register 68 by the first electrode 641, and the inside of a charge transfer register is transmitted to it by the second electrode 642, and it is outputted to outside from here.

[0026]

The pattern of the fine projection 67 was formed in the PSG passivation film 66 on the photo-diode 62 by RIE by EB drawing like the first working example. Here, the color filter did not form in the upper part of the fine projection 67, but it considered it as monochrome purpose.

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The interface reflection with surface PSG and air could be inhibited, and the sensitivity characteristic improved 4% conventionally as compared with the CCD linear image sensor of structure.

Although the air (n= abbreviation 1) in contact with the passivation film (refractive index n= 1.9-2.0) and the surface of the CCD area image sensor formed on the semiconductor substrate differs in a refractive index, By having formed an one or more-aspect ratio fine projection in the lower layer insulator layer (passivation film) of the interface with the cycle below the wavelength of incident light, a reflection of the light which occurs by a passivation film can be made very small. Therefore, the CCD linear image sensor with which the loss of incident light quantity was small excellent in the sensitivity characteristic is obtained. Thus, in the whole region of a light range (400 nm - 700 nm), the surface reflectance of a passivation film can be reduced to 2% or less by forming a fine projection in a passivation film. Since a reflection of the incident light which happens by the interface from which a refractive index differs can be reduced according to this method, without using methods, such as formation of a multilayer interference film, the CCD linear image sensor excellent in the sensitivity characteristic is obtained without changing the existing film constitution largely.

[0027]

[Effect of the Invention]

As mentioned above, according to the present invention, a reflection of the incident light which happens by the interface from which a refractive index differs can be reduced without using methods, such as formation of a multilayer interference film, and the solid state imaging device excellent in the sensitivity characteristic can be provided, without changing the existing film constitution largely.

[Brief Description of the Drawings]

[Drawing 1]The cross sectional view of the solid state imaging device concerning the first working example of the present invention.

[Drawing 2]The manufacturing process cross sectional view of the solid state imaging device of Fig.1.

[Drawing 3]The plan view of the semiconductor substrate which describes the photo-diode (photoelectric conversion part) and electrode of a solid state imaging device of Fig.1.

[Drawing 4]The plan view of the semiconductor substrate which describes the color filter of the solid state imaging device of Fig.1.

[Drawing 5]The cross sectional view of the solid state imaging device concerning the second working example of the present invention.

[Drawing 6]The cross sectional view of the solid state imaging device concerning the second working example of the present invention.

[Drawing 7]The cross sectional view of the solid state imaging device concerning the 3rd working example of the present invention.

[Drawing 8]The cross sectional view of the solid state imaging device concerning the 4th working example of the present invention.

[Drawing 9]The cross sectional view of the CCD area image sensor which is the conventional solid state imaging device.

[Explanations of letters or numerals]

1, 21, 41, 61, 101 ... Semiconductor substrate

2, 22, 42, 62, 102 ... Photo-diode (photoelectric conversion part)

3, 23, 33, 43, 53, 63, 103 ... Insulator layer

4, 24, 44, 64, 104 ... Electrode

5, 25, 45, 65, 105 ... Light-shielding film

6, 26, 46, 66, 106 ... Passivation film

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7, 27, 47, 67 ... Fine projection (antireflection structure)
8, 28, 48, 108 ... Color filter
9, 29, 49, 109 ... Insulator layer consisting of organic resin
10, 30, 50, 110 ... Micro lens
11, 31, 51, 68, 111 ... CCD register
12 ... Level charge transfer REJISHITA
13 ... Peripheral circuit 14 ... Resist pattern
34, 54, 112 ... Color filter flattening film
41, 141, 241, 441, 641 ... First electrode
42, 142, 242, 442, 642 ... Second electrode
261, 461 ... Opening

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DRAWINGS

*** NOTICES ***

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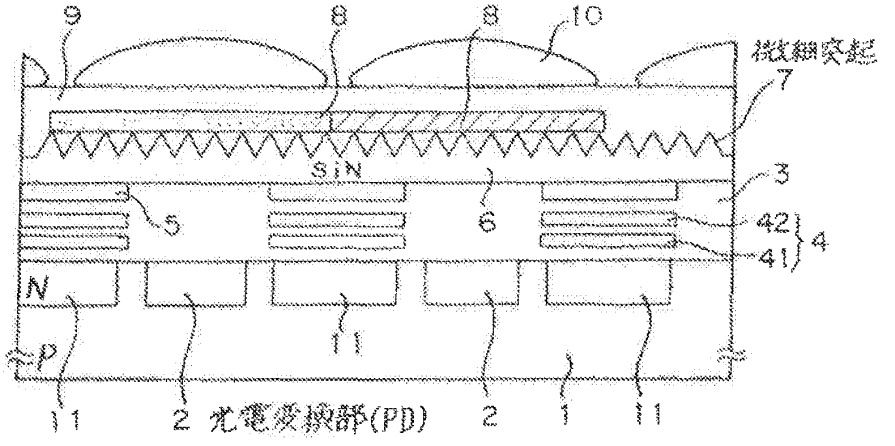
1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]



[Drawing 2]

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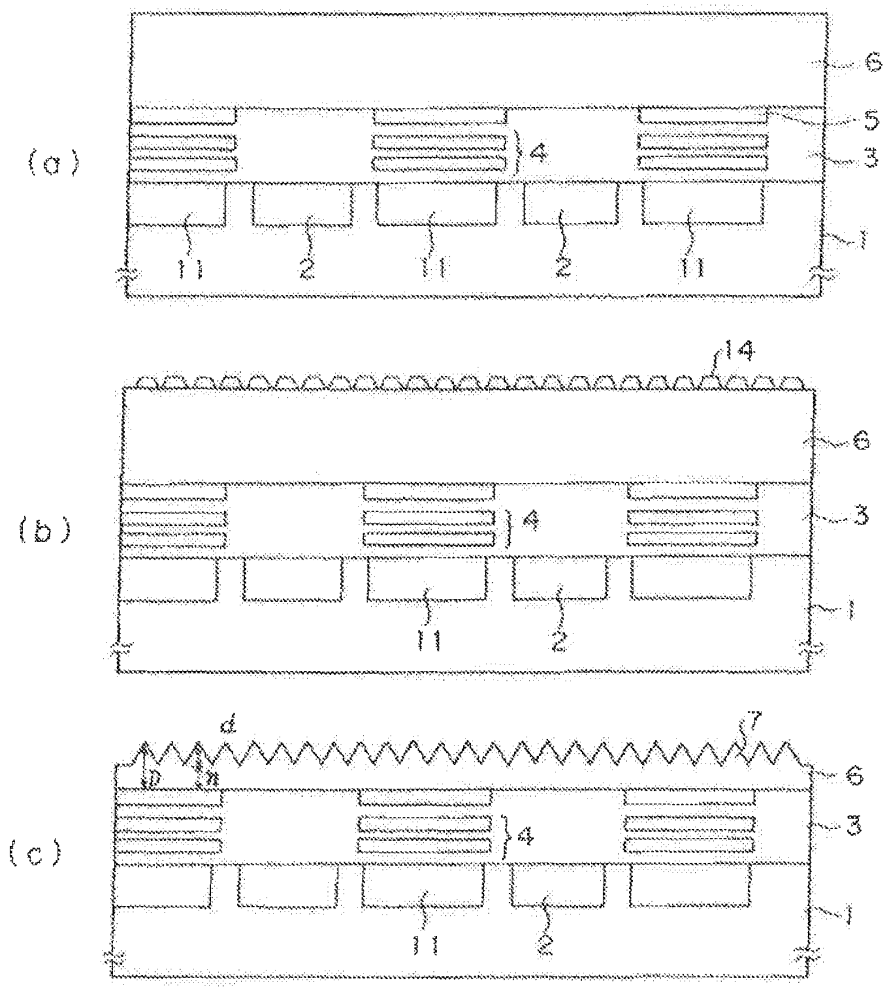

[Drawing 3]

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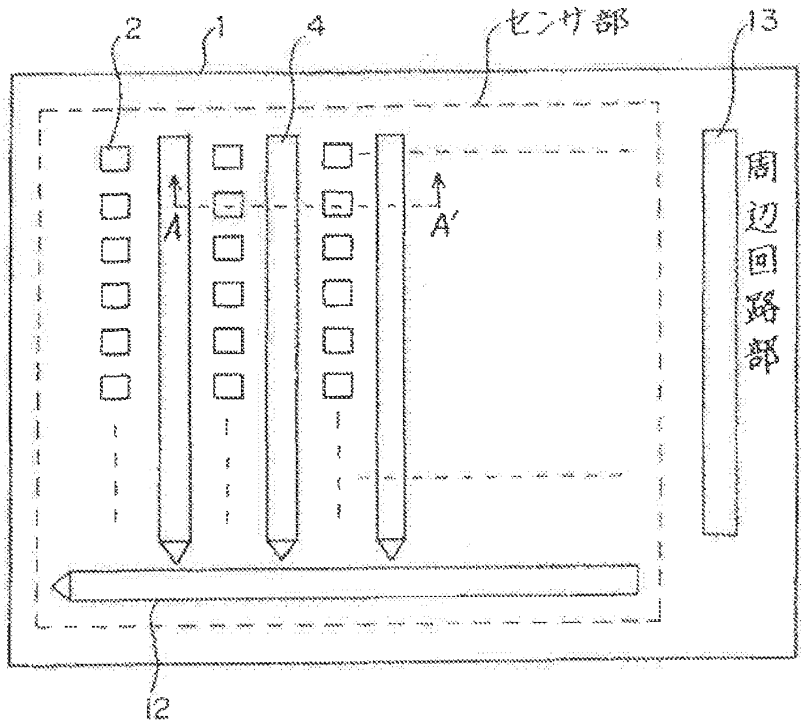
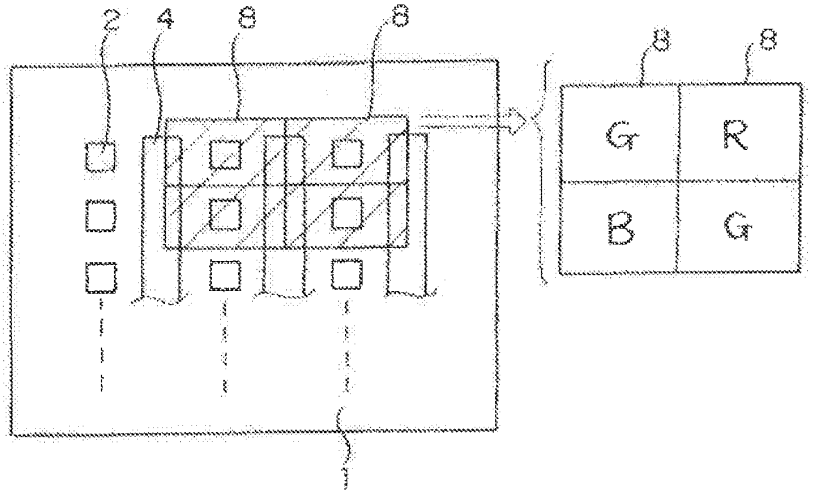


[Drawing 4]



[Drawing 5]

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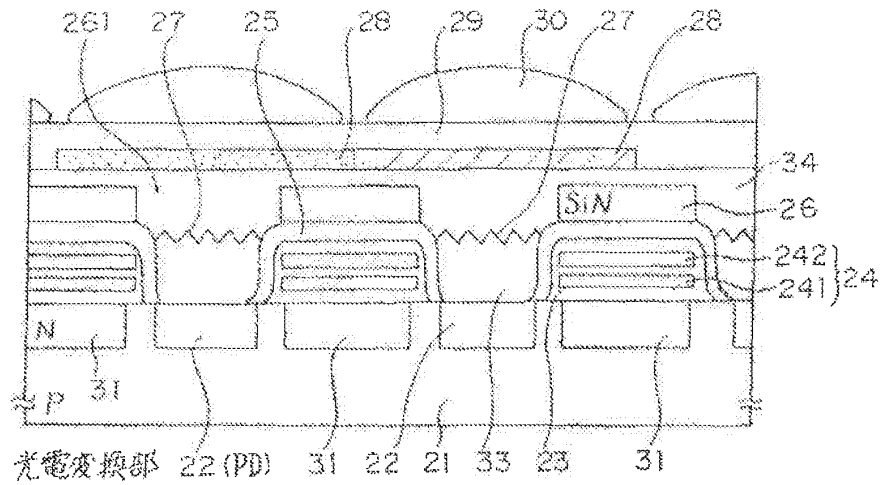
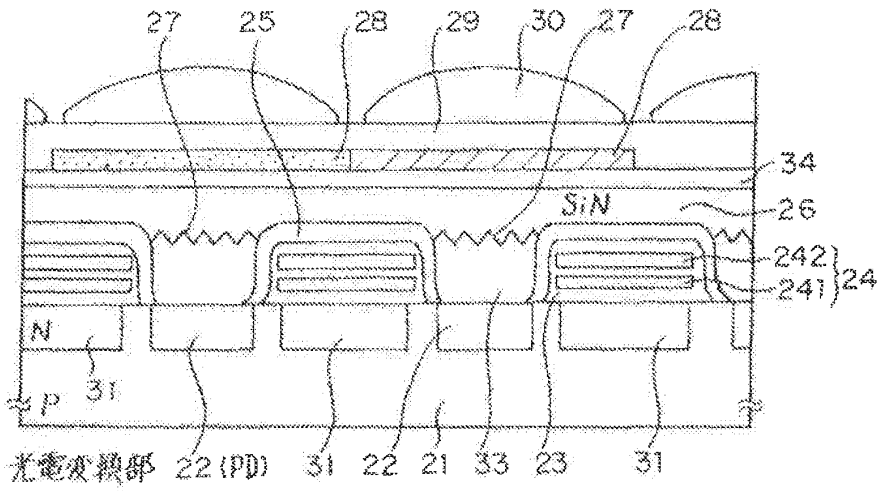


[Drawing 6]



[Drawing 7]

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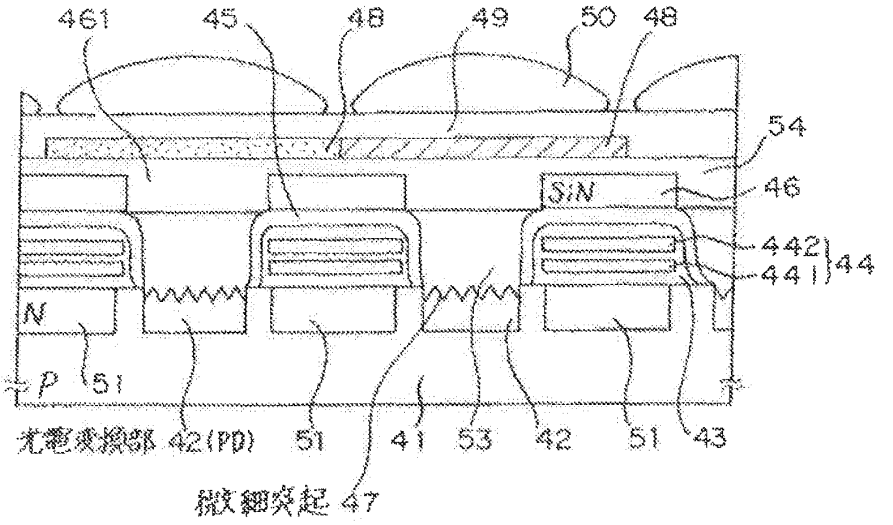

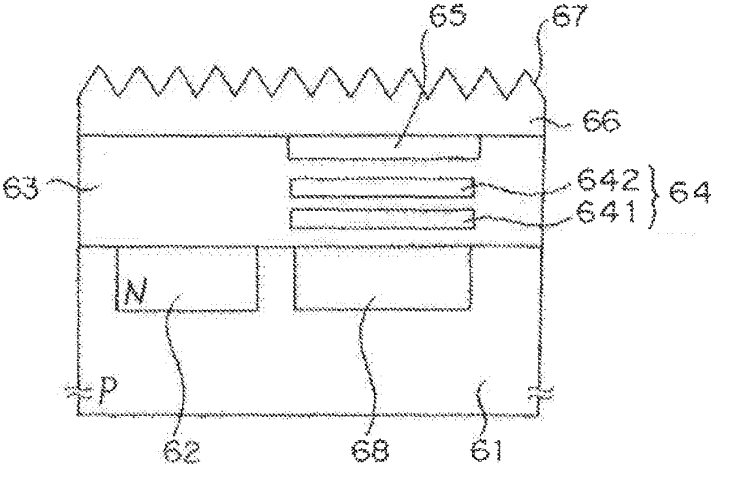

[Drawing 8]

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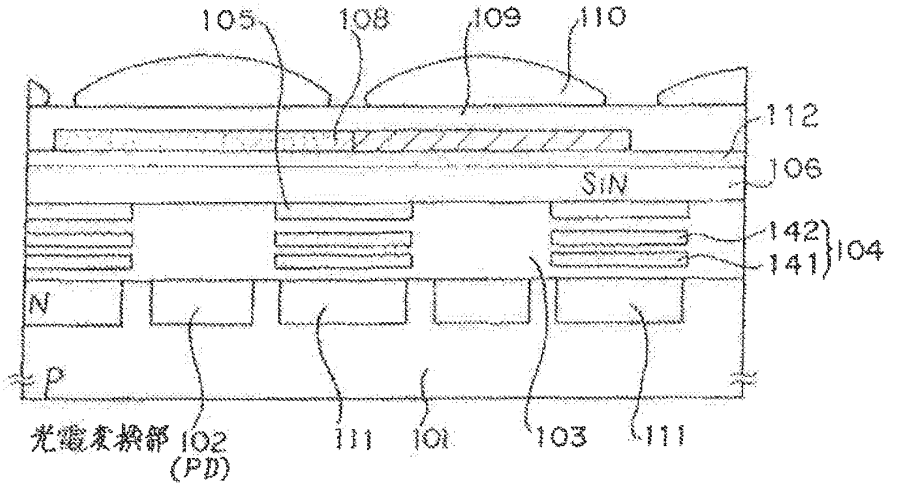
[Drawing 9]



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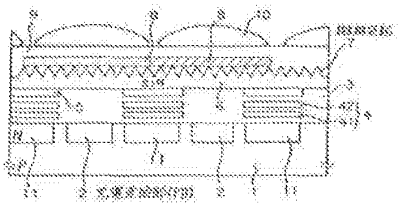
5C024 CY47 EX01 GX01

(54)【発明の名称】固体撮像装置

(57)【要約】
【課題】基板表面及び内部の屈折率が異なる境界面で起きる光の反射を極く小さくして入射光量の損失が小さく感度特性に優れた固体撮像装置を提供する。
【解決手段】半導体基板１上に形成された固体撮像装置のパッシベーション膜６、フォトダイオード２が形成されたシリコン半導体基板１の表面もしくは半導体基板表面上に形成された多層の絶縁膜３、６のうち屈折率が異なる界面の下層の絶縁膜に入射光の波長以下の周期で、アスペクト比１以上の微細突起７を設ける。図ではパッシベーション膜に形成するが、フォトダイオード２の表面、絶縁膜３の表面に反射防止構造体を設けることができる。微細突起の形成により、パッシベーション膜、半導体基板表面もしくは内部の屈折率が異なる境界面で起きる光の反射を極めて小さくできるため入射光量の損失が小さく感度特性に優れた固体撮像装置が得られる。
【選択図】　図１



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【特許請求の範囲】
【請求項１】
半導体基板と、
前記半導体基板に形成された光電変換部と、
前記光電変換部から生成された電荷を転送する電荷転送部と、
前記半導体基板上に形成され、前記光電変換部及び前記電荷転送部を被覆するパッシベーション膜とを具備し、
前記パッシベーション膜は、その表面に微細突起が配列形成された反射防止構造体を有することを特徴とする固体撮像装置。
【請求項２】
前記反射防止構造体を構成する微細突起は、０．０５～１μｍの周期、１以上のアスペクト比で配列形成されていることを特徴とする請求項１に記載の固体撮像装置。
【請求項３】
前記反射防止構造体を構成する微細突起は、０．０５～１μｍの周期及び１以上のアスペクト比の範囲内でランダムに配列され、ランダムにアスペクト比が変化することを特徴とする請求項１に記載の固体撮像装置。
【請求項４】
前記反射防止構造体を構成する微細突起の配列周期は、前記光電変換部に入射して電荷を生成する入射光の波長より小さいことを特徴とする請求項１又は請求項２に記載の固体撮像装置。
【請求項５】
半導体基板と、
前記半導体基板に形成された光電変換部と、
前記光電変換部から生成された電荷を転送する電荷転送部とを具備し、
前記光電変換部は、その表面に微細突起が配列形成された反射防止構造体を有することを特徴とする固体撮像装置。
【請求項６】
前記反射防止構造体を構成する微細突起の配列周期は、前記光電変換部に入射して電荷を生成する入射光の波長より小さいことを特徴とする請求項５に記載の固体撮像装置。
【請求項７】
半導体基板と、
前記半導体基板に形成された光電変換部と、
前記光電変換部から生成された電荷を転送する電荷転送部とを具備し、
前記光電変換部の上層には透明な材質からなる多層の絶縁膜が形成され、この多層の絶縁膜のうち、異なる屈折率からなる絶縁膜の界面において、その下層側の絶縁膜は、その表面に微細突起が配列形成された反射防止構造体を有することを特徴とする固体撮像装置。
【請求項８】
前記反射防止構造体を構成する微細突起の配列周期は、前記光電変換部に入射して電荷を生成する入射光の波長より小さいことを特徴とする請求項７に記載の固体撮像装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】
本発明は、固体撮像装置に関し、とくに新規な構造を有する反射防止層を備えた感度特性の優れた固体撮像装置に関するものである。
【０００２】
【従来の技術】
電荷結合素子（ＣＣＤ：Ｃｈａｒｇｅｄ　Ｃｏｕｐｌｅｄ　Ｄｅｖｉｃｅ）やＣＭＯＳ（Ｃｏｍｐｌｅｍｅｎｔａｒｙ　Ｍｅｔａｌ　Ｏｘｉｄｅ　Ｓｅｍｉｃｏｎｄｕｃｔｏｒ）センサー等の固体撮像装置では、通常パッシベーション膜として表面にSiO_2やＳｉＮ等の絶縁薄膜が形成されている。光が固体撮像装置に入射すると、空気（ｎ＝１）と

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ＳｉＮ（ｎ～２．０（略２．０））の屈折率差のために界面での光反射が起こり、反射した光はその下に形成されたフォトダイオードに到達せず、その結果入射光量に対して、十分な感度が得られない等の問題があった。

【０００３】

従来の固体撮像装置を図９に示されたＣＣＤエリアイメージセンサを例にして説明する。ＣＣＤエリアイメージセンサは、例えば、デジタルカメラやビデオに用いられる。このエリアイメージセンサは、例えば、ｐ型半導体基板１０１に形成される。半導体基板１０１の表面領域には、複数のｎ型不純物拡散領域が形成されている。その内の１種類はフォトダイオード１０２を構成し、半導体基板１０１の所定の領域にマトリックス状に配列されている。フォトダイオード１０２は、画素といい、光電変換部を構成している。フォトダイオード１０２は、マトリックス状に配列されているので、複数の列からなり、各列を画素列という。各画素列間にはＣＣＤレジスタ１１１を構成する他のｎ型不純物拡散領域が形成されている。ＣＣＤレジスタ１１１の上には、絶縁膜を介して積層された電極１０４が形成されている。ＣＣＤレジスタ１１１の直上にはポリシリコン等からなる第１の電極１４１が形成され、その上にポリシリコンなどからなる第２の電極１４２が形成されている。電極１０４及びＣＣＤレジスタ１１１は、垂直電荷転送レジスタを構成している。第１の電極１４１によりフォトダイオード１０２（光電変換部）で変換された電荷は、ＣＣＤレジスタ１１１へシフトされ、第２の電極１４２により垂直電荷転送レジスタ内を送られて水平電荷転送レジスタ（図示しない）に送られ、この水平電荷転送レジスタから外部へ出力される。

【０００４】

フォトダイオード１０２、水平及び垂直電荷転送レジスタが被覆されるように半導体基板１０１上にＣＶＤ法などによりＳｉＯ$_2$　絶縁膜１０３が堆積される。この絶縁膜１０３上に、水平及び垂直電荷転送レジスタを被覆するように、そして、フォトダイオード１０２を被覆しないように、アルミニウムなどからなる遮光膜１０５を選択的に形成する。次に、遮光膜１０５及び絶縁膜１０３を被覆するように半導体基板１０１上にシリコン窒化膜（ＳｉＮ）などからなるパッシベーション膜１０６を形成する。このパッシベーション膜１０６上に有機樹脂からなるカラーフィルタ平坦化膜１１２を介して赤（Ｒ）、緑（Ｇ）、青（Ｂ）のカラーフィルタ１０８を形成する。パッシベーション膜１０６の上には有機樹脂からなるカラーフィルタ平坦化膜１１２が形成されている。カラーフィルタ１０８は、有機樹脂よりなる絶縁膜１０９で固定され、絶縁膜１０９上には、マイクロレンズ１１０が形成されている。そして、カラーフィルタ１０８及びマイクロレンズ１１０は、フォトダイオード１０２の上に配置されるように形成されている。

【０００５】

【発明が解決しようとする課題】

このような従来の固体撮像装置において、変換効率を高めるためには、入射する光が反射することなく光電変換部において変換されることが必要である。可能な限り反射を少なくするための反射防止の方法としては、単層もしくは多層干渉膜を利用した反射防止膜のコーティングが知られている。これらは、特定の波長域で優れた反射防止特性を有しているが、可視光全域において優れた反射防止膜を形成することは困難である。また、これらの方法は、各膜の膜厚に敏感であり、安定した反射防止特性を維持するためには製造上の管理が困難であるなどの多くの問題を抱えている。

本発明は、このような事情によりなされたものであり、基板表面及び内部の屈折率が異なる膜界面で起きる光の反射を極めて小さくして入射光量の損失が小さく、感度特性に優れた固体撮像装置を提供する。

【０００６】

【課題を解決するための手段】

本発明は、半導体基板上に形成された固体撮像装置のパッシベーション膜、フォトダイオードが形成されたシリコン表面もしくはシリコン表面上に形成された多層の絶縁膜のうち屈折率が異なる界面の下層の絶縁膜に可視光や赤外線などの入射光の波長以下の周期でア

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スペクト比１以上の微細な突起を形成したことを特徴としている。微細突起の形成により、パッシベーション膜、半導体基板表面もしくは内部の屈折率が異なる境界面で起きる光の反射を極めて小さくできるため入射光量の損失が小さく感度特性に優れた固体撮像装置が得られる。本発明に用いるパッシベーション膜にはシリコン窒化膜（ＳｉＮ）あるいはＰＳＧなどのシリコン酸化膜（ＳｉＯ。　）などが用いられる。

本発明の固体撮像装置は、半導体基板と、前記半導体基板に形成された光電変換部と、前記光電変換部から生成された電荷を転送する電荷転送部と、前記半導体基板上に形成され、前記光電変換部及び前記電荷転送部を被覆するパッシベーション膜とを具備し、前記パッシベーション膜は、微細突起が配列形成された反射防止構造体を有することを特徴としている。前記反射防止構造体を構成する微細突起は、０．０５～１μｍの周期、１以上のアスペクト比で配列形成されているようにしても良い。前記反射防止構造体を構成する微細突起は、０．０５～１μｍの周期及び１以上のアスペクト比の範囲内でランダムに配列し、ランダムにアスペクト比が変化するようにしても良い。前記反射防止構造体を構成する微細突起の配列周期は、前記光電変換部に入射して電荷を生成する入射光の波長より小さいようにしても良い。

【０００７】

また、本発明の固体撮像装置は、半導体基板と、前記半導体基板に形成された光電変換部と、前記光電変換部から生成された電荷を転送する電荷転送部とを具備し、前記光電変換部は、その表面に微細突起が配列形成された反射防止構造体を有することを特徴としている。前記反射防止構造体を構成する微細突起の配列周期は、前記光電変換部に入射して電荷を生成する入射光の波長より小さくしても良い。

また、本発明の固体撮像装置は、半導体基板と、前記半導体基板に形成された光電変換部と、前記光電変換部から生成された電荷を転送する電荷転送部とを具備し、前記光電変換部の上層には透明な材質からなる多層の絶縁膜が形成され、この多層の絶縁膜のうち、異なる屈折率からなる絶縁膜の界面において、その下層側の絶縁膜は、表面に微細突起が配列形成された反射防止構造体を有することを特徴としている。前記反射防止構造体を構成する微細突起の配列周期は、前記光電変換部に入射して電荷を生成する入射光の波長より小さくしても良い。入射光の波長以下の凹凸（微細突起）がある場合、光は、突起の底部から先端まで屈折率が滑らかな傾斜を持って変わる（Ｇｒａｄｅｄ　Ｉｎｄｅｘ）膜と見なすため、界面での急激な屈折率変化がなく、透過の際の損失が殆どなくなるという効果がある。

【０００８】

【発明の実施の形態】

以下、図面を参照して発明の実施の形態を説明する。

まず、図１乃至図４を参照して第１の実施例を説明する。

図１は、固体撮像装置の断面図、図２は、図１の固体撮像装置の製造工程断面図、図３は、図１の固体撮像装置のフォトダイオード（光電変換部）及び電極を説明する半導体基板の平面図、図４は、図１の固体撮像装置のカラーフィルタを説明する半導体基板の平面図である。図３のＡ－Ａ′線に沿う部分の断面図が図１に示されている。この実施例を図１に示されたＣＣＤエリアイメージセンサを一例にして説明する。

【０００９】

ＣＣＤエリアイメージセンサは、例えば、デジタルカメラやビデオに用いられる。このエリアイメージセンサは、例えば、ｐ型半導体基板１に形成される。半導体基板１の表面領域には、複数のｎ型不純物拡散領域が形成されている。その一部は複数のフォトダイオード（Ｐｄ）２を構成し、半導体基板１の所定の領域にマトリックス状に配列されている。フォトダイオード２は、光電変換画素、いわゆる画素といい、光電変換部を構成している。フォトダイオード２は、マトリックス状に配列されているので、複数の列からなり、各列を画素列という。各画素列間にはＣＣＤレジスタ１１を構成するフォトダイオードとは異なる他のｎ型不純物拡散領域が形成されている。ＣＣＤレジスタ１１の上には、ＳｉＯ。　などからなる絶縁膜３を介して転送された電極４が形成されている。転送された電極

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４の内、ＣＣＤレジスタ１１の直上にはポリシリコンなどからなる第１の電極４１が形成され、その上に絶縁膜３を介してポリシリコンなどからなる第２の電極４２が形成されている。電極４及びＣＣＤレジスタ１１は、垂直電荷転送レジスタを構成している。２つの電極４１、４２は、その端部をオーバーラップさせて形成される。フォトダイオード２（光電変換部）で変換された電荷は、第１の電極４１によりＣＣＤレジスタ１１へシフトされ、第１及び第２の電極４１、４２により垂直電荷転送レジスタ内を転送されて水平電荷転送レジスタ（図示しない）に送られ、さらに、この水平電荷転送レジスタから外部へ出力される。

【００１０】

フォトダイオード２、水平及び垂直電荷転送レジスタが被覆されるように半導体基板１上にＣＶＤ法などにより絶縁膜３が堆積される。この絶縁膜３上に、水平及び垂直電荷転送レジスタを被覆するように、そして、フォトダイオード２を被覆しないように、アルミニウムなどからなる遮光膜５を選択的に形成する。次に、遮光膜５及び絶縁膜３を被覆するように半導体基板１上にシリコン窒化膜（ＳｉＮ）などからなるパッシベーション膜６を形成する。このパッシベーション膜にはシリコン酸化膜などの他の材料を用いることができる。このパッシベーション膜６上に赤（Ｒ）、緑（Ｇ）、青（Ｂ）のカラーフィルタ８が形成されている。カラーフィルタ８は、有機樹脂よりなる絶縁膜９で固定され、絶縁膜９上には、マイクロレンズ１０が形成される。カラーフィルタ８及びマイクロレンズ１０は、フォトダイオード２を覆うように配設されている。

この実施例では、本発明の特徴である反射防止構造体は、パッシベーション膜に形成される。図に示すように、パッシベーション膜６の表面には反射防止構造体として微細突起７が形成されている。パッシベーション膜６は、厚さＤの内表面の厚さｄに微細突起７が形成されている。したがって、下側の厚さｈの部分がパッシベーション膜としての機能を主として持っている。

【００１１】

反射防止構造体を構成する微細突起は、フォトダイオード（光電変換部）に入射する光の波長より小さくなるように形成すると効率良い反射防止作用が得られる。したがって、この実施例では、微細突起は０．０５～１μｍの周期及び１以上のアスペクト比の内から所定の値を選択して配列形成される。しかし、本発明では、微細突起は、０．０５～１μｍの周期及び１以上のアスペクト比の範囲内でランダムに配列し、ランダムにアスペクト比を変化するように構成することもできる。

次に、図３を参照して図１に示すＣＣＤエリアイメージセンサの半導体基板上の配置を説明する。半導体基板１のセンサ部にはフォトダイオード（ＰＤ）２の列とＣＣＤレジスタ上に形成された電極４が交互にならんでいる。前述のようにフォトダイオード２（光電変換部）で変換された電荷は、ＣＣＤレジスタへシフトされ、電極４により垂直電荷転送レジスタ内を転送されて水平電荷転送レジスタ１２に送られ、この水平電荷転送レジスタ１２から外部へ出力される。半導体基板１のセンサ部が形成されていない領域には入出力端子部や電極を駆動する周辺回路部が形成されている。

【００１２】

次に、図４を参照して図３のセンサ部に取り付けられるカラーフィルタを説明する。カラーフィルタ８は、フォトダイオード２の上及びその近傍を被覆するようにパッシベーション膜上に形成される。フィルタのカラーは、フォトダイオード２毎に異なるように配置する。図に示すように、４つのフォトダイオード２上にそれぞれ赤（Ｒ）、緑（Ｇ）、青（Ｂ）のカラーフィルタ８を形成する。図に示された４つのカラーフィルタ８を１つのカラーパターンとして、このカラーパターンが基板上を覆ってＣＣＤエリアイメージセンサの表面にカラーフィルタ８が形成される。カラーフィルタ８は、有機樹脂よりなる絶縁膜で固定され、この絶縁膜上にマイクロレンズが形成される。マイクロレンズは、フォトダイオード２の真上に配置されるように形成される。

【００１３】

次に、図２を参照して図１に示されたＣＣＤエリアイメージセンサの製造工程を説明する

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。まず、シリコンからなる半導体基板１にフォトダイオード２、ＣＣＤエリアイメージセンサ１１を構成する不純物拡散領域を形成し、半導体基板１上にＳｉＯ$_2$　などからなる絶縁膜３で被覆された電極４を形成し、電極４の上に絶縁膜３を介してアルミニウムの遮光膜５を形成する。半導体基板１に入射した光を光電変換するフォトダイオード２は、マトリクス状に設けられ、そして横方向に隣接する形で電荷を転送させるための電極４及びこれに対応する部分に遮光膜が形成される。そして、絶縁膜３の上にはパッシベーション膜６を構成するシリコン窒化膜（ＳｉＮ）を厚さ４００ｎｍ程度堆積させる（図２（ａ））。

【００１４】

次に、半導体基板１にＥＢ（電子ビーム）レジストを膜厚２００ｎｍ塗布し、１辺が１００ｎｍで隣接パターンとのスペースが１００ｎｍとなるようにこれをＥＢ描画、現像を行って島状のレジストパターン１４を形成した（図２（ｂ））。次に、島状のレジストパターンをマスクとして、ＲＩＥ（Ｒｅａｃｔｉｖｅ　Ｉｏｎ　Ｅｔｃｈｉｎｇ）により、CF_4　／Ａｒ＝２０／８０ｓｃｃｍ、圧力１０Ｔｏｒｒ、パワー２００Ｗでレジストがなくなるまでエッチング（すなわち、ＳｉＮ／レジストの低選択比エッチング）し、シリコン窒化膜（ＳｉＮ）に周期２００ｎｍ、アスペクト比１．５の微細突起７のパターンを形成する。このようにして、半導体基板１の表面に微細突起７からなる反射防止構造体が得られる（図２（ｃ））。

さらに、微細突起７のパターン上にカラーフィルタ８、有機樹脂からなる絶縁膜９及びマイクロレンズ１０を形成してＣＣＤエリアイメージセンサが完成する（図１参照）。

【００１５】

半導体基板表面のパッシベーション膜上に、微細突起パターンを形成することによりカラーフィルタとの界面反射が軽減され、従来構造のＣＣＤエリアイメージセンサと比較して感度特性が８％向上した。

半導体基板上に形成されたＣＣＤエリアイメージセンサのパッシベーション膜（屈折率ｎ＝１．９～２．０）とその表面上に形成されカラーフィルタを固定する絶縁膜（有機樹脂、ｎ＝１．５）とは屈折率が異なるものの、その界面の下層の絶縁膜（パッシベーション膜）に入射光の波長以下の周期でアスペクト比１以上の微細突起を形成したことにより、パッシベーション膜で起きる光の反射を極めて小さくできる。したがって、入射光量の損失が小さく感度特性に優れたＣＣＤエリアイメージセンサが得られる。このように、パッシベーション膜に微細突起を形成することにより、４００ｎｍ～７００ｎｍの可視光領域の全域において、パッシベーション膜の表面反射率を２％以下にまで低減することができた。この方法によれば、多層干渉膜の形成等の方法を使わずに、屈折率の異なる界面で起こる入射光の反射を低減できるので、既存の膜構成を大きく変えることなく感度特性に優れたＣＣＤエリアイメージセンサが得られる。

【００１６】

次に、図５及び図６を参照して第２の実施例を説明する。

図５及び図６は、固体撮像装置の断面図である。この実施例をＣＣＤエリアイメージセンサを一例にして説明する。このエリアイメージセンサは、例えば、ｐ型半導体基板２１に形成される。半導体基板２１の表面領域には、複数のｎ型不純物拡散領域が形成されている。その一部は複数のフォトダイオード（ＰＤ）２２を構成し、半導体基板２１の所定の領域にマトリックス状に配列されている。フォトダイオード２２は、光電変換画素、いわゆる画素といい、光電変換部を構成している。フォトダイオード２２は、マトリックス状に配列されているので、複数の列からなり、各列を画素列という。各画素列間にはＣＣＤレジスタ３１を構成するフォトダイオードとは異なるｎ型不純物拡散領域が形成されている。ＣＣＤレジスタ３１の上には、ＳｉＯ$_2$　などからなる絶縁膜２３を介して積層された電極２４が形成されている。配列された電極２４の内、ＣＣＤレジスタ３１の直上にはポリシリコンなどからなる第１の電極２４１が形成され、その上に絶縁膜２３を介してポリシリコンなどからなる第２の電極２４２が形成されている。電極２４及びＣＣＤレジスタ３１は、垂直電荷転送レジスタを構成している。フォトダイオード２２（光電変換部）

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で変換された電荷は、第１の電極２４１によりＣＣＤレジスタ３１へシフトされ、第２の電極２４２により垂直電荷転送レジスタ内を転送されて水平電荷転送レジスタ（図示しない）に送られ、さらに水平電荷転送レジスタから外部へ出力される。

【００１７】

フォトダイオード２２、水平及び垂直電荷転送レジスタが被覆されるように半導体基板２１上にＣＶＤ法などにより前述の絶縁膜２３が堆積される。この絶縁膜２３上に、水平及び垂直電荷転送レジスタを被覆するように、そして、フォトダイオード２を被覆しないように、アルミニウムなどからなる遮光膜２５が選択的に形成されている。次に、遮光膜２５及び絶縁膜２３を被覆するように半導体基板２１上にシリコン窒化膜（ＳｉＮ）などからなるパッシベーション膜２６が形成されている。このパッシベーション膜２６上に赤（Ｒ）、緑（Ｇ）、青（Ｂ）のカラーフィルタ２８が形成されている。カラーフィルタ２８は、有機樹脂よりなる絶縁膜２９で固定され、絶縁膜２９上には、マイクロレンズ３０が形成されている。カラーフィルタ２８及びマイクロレンズ３０は、フォトダイオード２２を覆うように配置されている。

【００１８】

外部からの光が通る路（マイクロレンズ３０－カラーフィルタ２８－パッシベーション膜２６－絶縁膜２３－フォトダイオード２２）は、パッシベーション膜２６がシリコン窒化膜（ＳｉＮ）の場合、屈折率ｎが他の膜より大きく（ｎ＝１．９～２．０）、入射光が反射する機会が多くなり、感度特性を劣化させる原因の１つとなっている。そのために、この部分のパッシベーション膜を除去し、パッシベーション膜に膜のない部分（開口部）を形成することが考えられた。しかし、このように開口部を形成すると、その上に形成配置されているカラーフィルタが安定して設置されない。そこで、従来は、カラーフィルタが置かれる下地が平坦であるように、パッシベーション膜の上にカラーフィルタ平坦化膜を形成していた。この実施例ではこのような構造になっている。平坦化膜は、屈折率ｎが１．５程度の有機樹脂を用いている。

したがって、この実施例では、シリコン窒化膜を用いたパッシベーション膜２６には、フォトダイオード２２上にある光の通路の部分に開口部２６１を設けている。そして、遮光膜２５は、積層された電極２４を被覆する絶縁膜２３を包むように、光の通路の側面をも被覆して遮光効果を高くしている。さらに、光の通路の下部であるフォトダイオード２２と接触する部分にはシリコン酸化膜などの絶縁膜３３がＣＶＤ法などにより形成されており、この絶縁膜３３及びパッシベーション膜２６の上に有機樹脂などからなるカラーフィルタ平坦化膜３４が形成されている。

【００１９】

この実施例では、本発明の特徴である反射防止構造体は、シリコン酸化膜からなる絶縁膜３３の表面部分に形成される。図に示すように、光の通路に設けられた絶縁膜３３の表面には反射防止構造体として微細突起２７が形成されている。反射防止構造体を構成する微細突起２７の配列周期は、フォトダイオード２２に入射する光の波長より小さくすると効率良い反射防止作用が得られる。したがって、この実施例では、微細突起は、０．０５～１μｍの周期及び１以上のアスペクト比の内から所定の値を選択して配列形成される。しかし、微細突起は、０．０５～１μｍの周期及び１以上のアスペクト比の範囲内でランダムに配列し、ランダムにアスペクト比を変化するように構成することもできる。

半導体基板上に形成されたＣＣＤエリアイメージセンサのカラーフィルタ平坦化膜（屈折率ｎ＝約１．５）と、これと接するシリコン酸化膜からなる絶縁膜（ｎ＝１．４５）とは屈折率がその差は小さくとも異なっており、反射が起きる環境にあるものの、その界面の下層の絶縁膜に入射光の波長以下の所定の周期でアスペクト比１以上の微細突起を形成したことにより、絶縁膜で起きる光の反射を極めて小さくできる。したがって、入射光量の損失が小さく感度特性に優れたＣＣＤエリアイメージセンサが得られる。このように、パッシベーション膜に微細突起を形成することにより、４００ｎｍ～７００ｎｍの可視光領域の全域において、パッシベーション膜の表面反射率を２％以下にまで低減することができた。この方法によれば、多層干渉膜の形成等の方法を使わずに、屈折率の異なる界面で

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起こる入射光の反射を低減できるので、既存の膜構成を大きく変えることなく感度特性に優れたＣＣＤエリアイメージセンサが得られる。

【００２０】

なお、パッシベーション膜に開口部を形成するには、パッシベーション膜を堆積させてから、これを選択的にエッチングして開口形成をする場合と、最初から所定の部分を開口部形状にマスクしてパッシベーション膜を堆積する場合の２通りの方法を用いることができる。

図５に示す固体撮像装置は、パッシベーション膜に開口部が形成されている。しかし、この実施例では、パッシベーション膜に開口部を形成しないでそのまま使用することもできる。図６は、開口部のないパッシベーション膜を用いた例である。この例ではパッシベーション膜に開口部を形成する工程が省略できる。

【００２１】

次に、図７を参照して第３の実施例を説明する。

図７は、固体撮像装置の断面図である。この実施例をＣＣＤエリアイメージセンサを一例にして説明する。このエリアイメージセンサは、例えば、ｐ型半導体基板４１に形成される。半導体基板４１の表面領域には、複数のｎ型不純物拡散領域が形成されている。その一部は、複数のフォトダイオード（ＰＤ）４２を構成し、半導体基板４１の所定の領域にマトリックス状に配列されている。フォトダイオード（画素）４２は、光電変換部を構成している。フォトダイオード４２は、マトリックス状に配列されているので、複数の列からなり、各列を画素列という。各画素列間にはＣＣＤレジスタ５１を構成するフォトダイオードとは異なるｎ型不純物拡散領域が形成されている。ＣＣＤレジスタ５１の上には、SiO_2 などからなる絶縁膜４３を介して積層された電極４４が形成されている。積層された電極４４の内、ＣＣＤレジスタ５１の直上にはポリシリコンなどからなる第１の電極４４１が形成され、その上に絶縁膜４３を介してポリシリコンなどからなる第２の電極４４２が形成されている。電極４４及びＣＣＤレジスタ５１は、垂直電荷転送レジスタを構成している。フォトダイオード４２（光電変換部）で変換された電荷は、第１の電極４４１によりＣＣＤレジスタ５１へシフトされ、第２の電極４４２により垂直電荷転送レジスタ内を転送されて水平電荷転送レジスタ（図示しない）に送られ、さらに水平電荷転送レジスタから外部へ出力される。

【００２２】

フォトダイオード４２、水平及び垂直電荷転送レジスタが被覆されるように半導体基板４１上にＣＶＤ法などにより前述の絶縁膜４３が堆積される。この絶縁膜４３上に、水平及び垂直電荷転送レジスタを被覆するように、そして、フォトダイオード４２を被覆しないように、アルミニウムなどからなる遮光膜４５が選択的に形成されている。次に、遮光膜４５及び絶縁膜４３を被覆するように半導体基板４１上にシリコン窒化膜（ＳｉＮ）などからなるパッシベーション膜４６が形成されている。このパッシベーション膜４６上に赤（Ｒ）、緑（Ｇ）、青（Ｂ）のカラーフィルタ４８が形成されている。カラーフィルタ４８は、有機樹脂よりなる絶縁膜４９で固定され、絶縁膜４９上には、マイクロレンズ５０が形成されている。カラーフィルタ４８及びマイクロレンズ５０は、フォトダイオード４２を覆うように配置されている。

【００２３】

第２の実施例と同様に外部からの光が通る路は、パッシベーション膜がシリコン窒化膜（ＳｉＮ）の場合、屈折率ｎが他の膜より大きく（ｎ＝１．９～２．０）、入射光が反射する機会が多くなり、感度特性を劣化させる原因の１つとなっているために、この実施例ではこの部分のパッシベーション膜を除去し、パッシベーション膜４６に膜のない部分（開口部４６１）を形成する。そして、カラーフィルタが置かれる下地が平坦であるように、パッシベーション膜４６の上にカラーフィルタ平坦化膜５４を形成する。平坦化膜５４は、屈折率ｎが１．５程度の有機樹脂を用いている。遮光膜４５は、電極４４を被覆する絶縁膜４３を包むように、光の通路の側面をも被覆して遮光効果を高くしている。さらに、光の通路の下部であるフォトダイオード４２と接触する部分にはシリコン酸化膜などの絶

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縁膜５３がＣＶＤ法などにより形成されており、この絶縁膜５３及びパッシベーション膜４６上に前述のカラーフィルタ平坦化膜５４が形成されている。
この実施例では、本発明の特徴である反射防止構造体は、シリコンからなる半導体基板４１の表面部分に形成される。図に示すように、光の通路に露出するフォトダイオード４２の表面に反射防止構造体として微細突起４７が形成されている。反射防止構造体を構成する微細突起４７の配列周期は、フォトダイオード４２に入射する光の波長より小さくすると効率良い反射防止作用が得られる。したがって、この実施例では、微細突起は０．０５～１μｍの周期及び１以上のアスペクト比の内から所定の値を選択して配列形成される。しかし、微細突起は、０．０５～１μｍの周期及び１以上のアスペクト比の範囲内でランダムに配列し、ランダムにアスペクト比を変化するように構成することもできる。

【００２４】
半導体基板上に形成されたカラーフィルタ平坦化膜と接するシリコン酸化膜からなる絶縁膜（ｎ＝１．４５）５３と半導体基板（ｎ＞３）４１とは屈折率が大きく異なっており、反射が起きる環境にあるものの、その界面の下層の半導体基板４１のフォトダイオード４２に入射光の波長以下の所定の周期でアスペクト比１以上の微細突起４７を形成したことにより、半導体基板で起きる光の反射を極めて小さくできる。したがって、入射光量の損失が小さく感度特性に優れたＣＣＤエリアイメージセンサが得られる。このように、パッシベーション膜に微細突起を形成することにより、４００ｎｍ～７００ｎｍの可視光領域の全域において、パッシベーション膜の表面反射率を２％以下にまで低減することができた。この方法によれば、多層干渉膜の形成等の方法を使わずに、屈折率の異なる界面で起こる入射光の反射を低減できるので、既存の膜構成を大きく変えることなく感度特性に優れたＣＣＤエリアイメージセンサが得られる。
なお、パッシベーション膜に開口部を形成する方法は、第２の実施例で説明した通りである。
第２の実施例及び第３の実施例では、屈折率の異なる界面で起こる入射光の反射を低減する反射防止構造体をそれぞれ１か所に形成しているが、本発明では屈折率の異なる界面において、環境が悪い場所が複数あれば全てに適用することが可能である。例えば、第２の実施例と第３の実施例を合わせるように２か所に反射防止構造体を設けることができる。

【００２５】
次に、図８を参照して第４の実施例を説明する。
図８は、固体撮像装置の断面図である。この実施例では固体撮像装置としてＣＣＤリニアイメージセンサを説明する。リニアイメージセンサは、光電変換部のフォトダイオード（画素）が１次元に配列している。半導体基板６１に、光電変換部となるフォトダイオード６２をリニアに設け、第１の実施例と同様の方法で、第１の電極６４１、第２の電極６４２から構成されたポリシリコンなどからなる電極６４を形成し、アルミニウム遮光膜６５をシリコン酸化膜からなる絶縁膜６３を介して形成した。電極６４の下の半導体基板６１の表面領域には電極６４と共に電荷転送レジスタを構成するＣＣＤレジスタ（ｎ型不純物拡散領域）６８が形成されている。最上部の膜となるパッシベーション膜６６には、リンドープのシリコン酸化膜（ＰＳＧ）を厚さ４００ｎｍに形成した。
フォトダイオード６２（光電変換部）で変換された電荷は、第１の電極６４１によりＣＣＤレジスタ６８へシフトされ、第２の電極６４２により電荷転送レジスタ内を転送され、ここから外部へ出力される。

【００２６】
第１の実施例と同様に、ＥＢ描画によりフォトダイオード６２上のＰＳＧパッシベーション膜６６にＲＩＥにより微細突起６７のパターンを形成した。ここでは、微細突起６７の上部にカラーフィルタは形成せず、白黒用途とした。表面のＰＳＧと空気との界面反射が抑制でき、従来構造のＣＣＤリニアイメージセンサと比較して感度特性が４％向上した。
半導体基板上に形成されたＣＣＤエリアイメージセンサのパッシベーション膜（屈折率ｎ＝１．９～２．０）とその表面に接触している空気（ｎ＝略１）とは屈折率が異なるものの、その界面の下層の絶縁膜（パッシベーション膜）に入射光の波長以下の周期でアスペ

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クト比１以上の微細突起を形成したことにより、パッシベーション膜で起きる光の反射を極めて小さくできる。したがって、入射光量の損失が小さく感度特性に優れたＣＣＤリニアイメージセンサが得られる。このように、パッシベーション膜に微細突起を形成することにより、４００ｎｍ～７００ｎｍの可視光領域の全域において、パッシベーション膜の表面反射率を２％以下にまで低減することができる。この方法によれば、多層干渉膜の形成等の方法を使わずに、屈折率の異なる界面で起こる入射光の反射を低減できるので、既存の膜構成を大きく変えることなく感度特性に優れたＣＣＤリニアイメージセンサが得られる。

【００２７】

【発明の効果】

以上、本発明によれば、多層干渉膜の形成等の方法を使わずに、屈折率の異なる界面で起こる入射光の反射を低減でき、既存の膜構成を大きく変えることなく感度特性に優れた固体撮像装置を提供できる。

【図面の簡単な説明】

【図１】本発明の第１の実施例に係る固体撮像装置の断面図。

【図２】図１の固体撮像装置の製造工程断面図。

【図３】図１の固体撮像装置のフォトダイオード（光電変換部）及び電極を説明する半導体基板の平面図。

【図４】図１の固体撮像装置のカラーフィルタを説明する半導体基板の平面図。

【図５】本発明の第２の実施例に係る固体撮像装置の断面図。

【図６】本発明の第２の実施例に係る固体撮像装置の断面図。

【図７】本発明の第３の実施例に係る固体撮像装置の断面図。

【図８】本発明の第４の実施例に係る固体撮像装置の断面図。

【図９】従来の固体撮像装置であるＣＣＤエリアイメージセンサの断面図。

【符号の説明】

１、２１、４１、６１、１０１・・・半導体基板
２、２２、４２、６２、１０２・・・フォトダイオード（光電変換部）
３、２３、３３、４３、５３、６３、１０３・・・絶縁膜
４、２４、４４、６４、１０４・・・電極
５、２５、４５、６５、１０５・・・遮光膜
６、２６、４６、６６、１０６・・・パッシベーション膜
７、２７、４７、６７・・・微細突起（反射防止構造体）
８、２８、４８、１０８・・・カラーフィルタ
９、２９、４９、１０９・・・有機樹脂よりなる絶縁膜
１０、３０、５０、１１０・・・マイクロレンズ
１１、３１、５１、６８、１１１・・・ＣＣＤレジスタ
１２・・・水平電荷転送レジスタ
１３・・・周辺回路　１４・・・レジストパターン
３４、５４、１１２・・・カラーフィルタ平坦化膜
４１、１４１、２４１、４４１、６４１・・・第１の電極
４２、１４２、２４２、４４２、６４２・・・第２の電極
２６１、４６１・・・開口部

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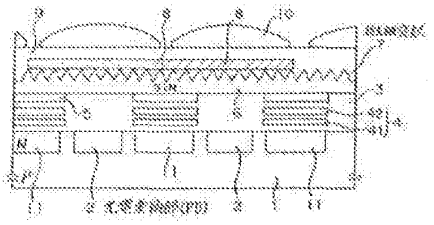
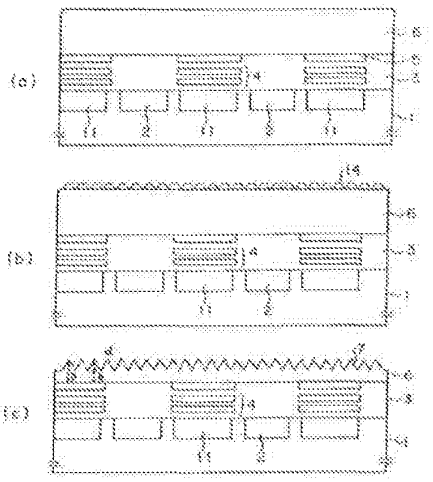
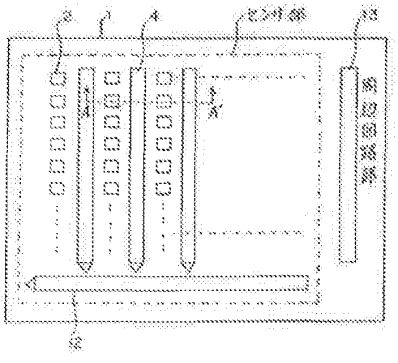
【図１】



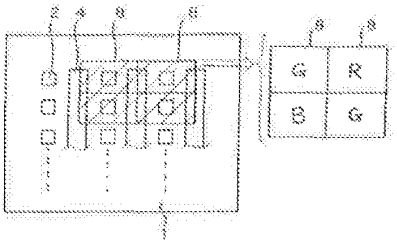
【図２】



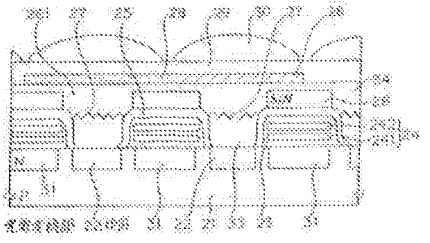
【図３】



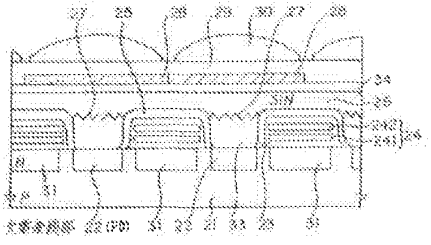
【図４】



【図５】



【図６】



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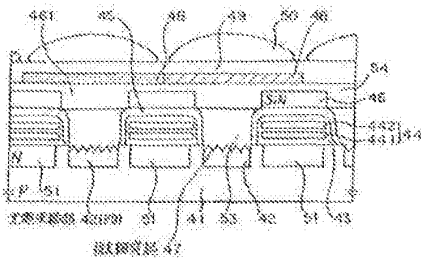
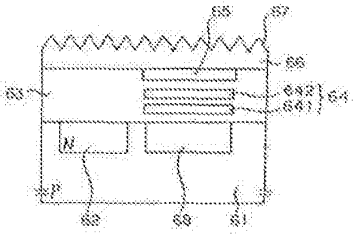
【図７】



【図８】



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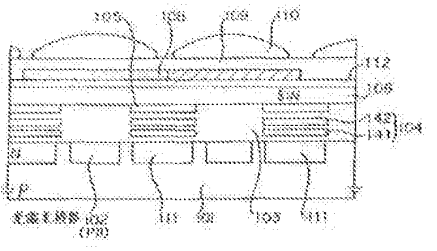

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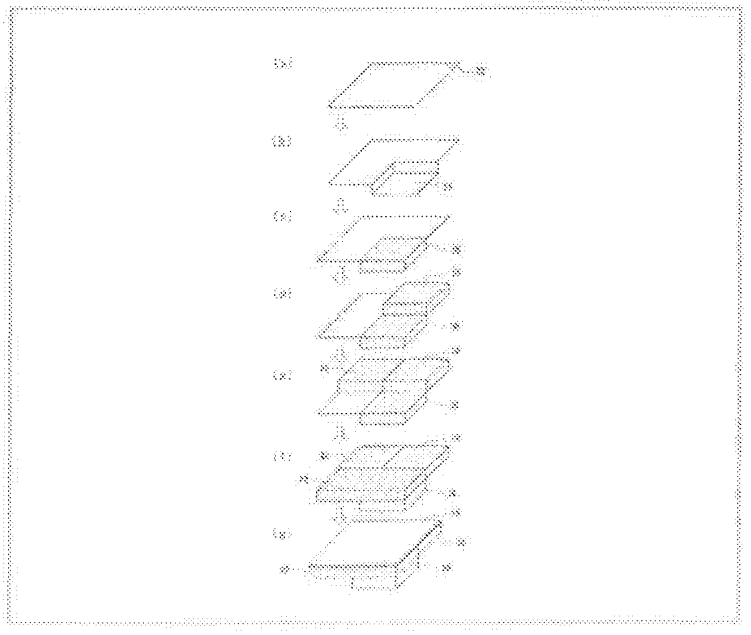
(72)Inventor	MATSUYAMA HISASHI

(54)SOLID-STATE IMAGE SENSING DEVICE AND ITS MANUFACTURING METHOD

(57)Abstract

PROBLEM TO BE SOLVED: To solve the problem of generation of irregularities in the surface of an image sensor due to a thick IR transmitting filter laminated in an IR picture element in a solid-state image sensing element wherein R, G, B picture elements detecting RGB color factors and IR picture element detecting infrared light factor are disposed.

SOLUTION: After a transfer electrode and a wiring are formed on a semiconductor substrate 30, a flattened film 32 is formed. A recess 34 is formed by etching the flattened film 32 in a position corresponding to an IR picture element. A B filter 36 is buried in the recess 34 on the IR picture element, and an R filter 42 is further laminated. R, G, B filters are laminated on the R, G, B picture elements using the unetched flattened film 32 as a foundation. The height of the surface of a filter array formed in the RGB picture element and IR picture element becomes even by making the recess part 34 deep by one layer of a color filter.



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CLAIMS

[Claim(s)]
[Claim 1]
Two or more kinds of visible light component photo detectors laminated on a light receiving surface via a foundation layer with a respectively transparent colored filter which transmits each other different color, In a solid state imaging device with which an infrared light component photo detector in which an infrared light transmission filter which transmits an infrared light component selectively was laminated on a light receiving surface via the aforementioned foundation layer was arranged,
The aforementioned foundation layer is formed on a light receiving surface of the aforementioned infrared light component photo detector more thinly than a light receiving surface top of the aforementioned visible light component photo detector,
The aforementioned infrared light transmission filter laminates two or more kinds of colored filters which transmit infrared light among the aforementioned colored filters on the aforementioned foundation layer, and it is constituted,
A solid state imaging device by which it is characterized.
[Claim 2]
In the solid state imaging device according to claim 1,
It has a red transmission filter which transmits a component according to red as the aforementioned colored filter, and a blue transmission filter which transmits a component to which it responded blue,
The aforementioned infrared light transmission filter laminates the aforementioned red transmission filter and said blue transmission filter, and it is constituted,
A solid state imaging device by which it is characterized.
[Claim 3]
In how to manufacture a solid state imaging device with which two or more kinds of visible light component photo detectors in which a colored filter which transmits each other different color was laminated on a light receiving surface, respectively, and an infrared light component photo detector in which an infrared light transmission filter in which an infrared light component is transmitted selectively was laminated on a light receiving surface were arranged,
A process of forming a transparent foundation layer in common on the aforementioned light receiving surface of each aforementioned visible light component photo detector and the aforementioned infrared light component photo detector,
An infrared light transmission filter formation process which forms the aforementioned infrared light transmission filter,
It ****,
The aforementioned infrared light transmission filter formation process,
An etching step which etches the aforementioned foundation layer and forms a concave part of the aforementioned foundation layer on the aforementioned light receiving surface of the

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aforementioned infrared light component photo detector,
A lower filter formation process laminated on the aforementioned concave part by using as a lower filter at least one kind of colored filter which transmits infrared light among the aforementioned colored filters,
An upper filter formation process laminated on the lower filter concerned by using as an upper filter a colored filter of a kind which transmits infrared light among the aforementioned colored filters, and is different from the aforementioned lower filter,
A ****(ing) manufacturing method.
[Claim 4]
In how to manufacture a solid state imaging device with which two or more kinds of visible light component photo detectors in which a colored filter which transmits each other different color was laminated on a light receiving surface, respectively, and an infrared light component photo detector in which an infrared light transmission filter in which an infrared light component is transmitted selectively was laminated on a light receiving surface were arranged,
A process of forming a transparent foundation layer in common on the aforementioned light receiving surface of each aforementioned visible light component photo detector and the aforementioned infrared light component photo detector,
An infrared light transmission filter formation process which forms the aforementioned infrared light transmission filter,
It ****,
The aforementioned infrared light transmission filter formation process,
A recessed-parts-forming process of forming a concave part of the aforementioned foundation layer on the aforementioned light receiving surface of the aforementioned infrared light component photo detector,
A lower filter formation process laminated on the aforementioned concave part by using as a lower filter at least one kind of colored filter which transmits infrared light among the aforementioned colored filters,
An upper filter formation process laminated on the lower filter concerned by using as an upper filter a colored filter of a kind which transmits infrared light among the aforementioned colored filters, and is different from the aforementioned lower filter,
A ****(ing) manufacturing method.
[Claim 5]
In the manufacturing method according to claim 3 or 4,
A manufacturing method of a solid state imaging device forming either of the blue transmission filters which transmit a red transmission filter which transmits a component according to red, and a component to which it responded blue as the aforementioned lower filter, and forming the other as said upper filter.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[Field of the Invention]

[0001]

The present invention relates to a solid state imaging device and a manufacturing method for the same, and relates to the ontip color filter in the solid state imaging device containing the photo detector which has sensitivity in an infrared region especially.

[Background of the Invention]

[0002]

Solid state image pickup devices (solid state imaging device), such as a CCD (Charge Coupled Device) image sensor mounted on a video camera or a digital camera, have the light-receiving part (photo detector) by which the two-dimensional array was carried out, carry out photoelectric conversion of the incident light by this light-receiving part, and generate an electric picture signal. the light range whose wavelength of the light-receiving part itself is about 380-780 nm -- in addition, it has sensitivity to the near infrared region of long wavelength further generally. Therefore, in order to acquire a color picture, two or more kinds of color filters from which it differs, the color, i.e., the transmitted wave length region, of the transmitted light, are arranged on a light receiving surface. After a color filter forms a transparent flattening film on a light receiving surface, it is laminated on this flattening film. On a color filter, still more nearly special flattening film and protective film are laminated.

[0003]

There are a filter set of the primary color system whose transmitted lights are red (R) green (G) and blue (B), and a filter set of the complementary color system which are cyanogen (Cy), magenta (Mg), and yellow (Ye) in a color filter. Although these color filters color an organic material, and are constituted and the visible light of a color corresponding, respectively is transmitted, infrared light is also transmitted on the material. For example, Fig.5 is a graph which shows the wavelength characteristic of transmissivity of RGB each filter.

The figure also shows the spectral sensitivity characteristic of a light-receiving part collectively.

[0004]

Since a light-receiving part has sensitivity also in infrared light, if an infrared light component enters, the signal charge by the component concerned will be generated and it cannot do a right color expression. Therefore, the infrared cut filter is conventionally arranged separately between the lens of a camera, and a solid state image pickup device.

[0005]

Visible light also attenuates this infrared cut filter about 10 to 20% at the same time it cuts infrared light. Therefore, incident visible luminous intensity decreased to the light-receiving part, the S/N ratio of the output signal was deteriorated according to it, and there was a problem of causing degradation of image quality.

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[0006]
As dealing with this problem, while losing an infrared cut filter, the light-receiving part which detects only the infrared light component in incident light fundamentally is provided, and how to perform signal processing reproducing a right color can be considered based on the information about the infrared light component obtained from the light-receiving part concerned.
[0007]
The light-receiving part which detects only an infrared light component is realizable by laminating two or more kinds of color filters which transmit the visible light of each other different color on the light receiving surface. That is, a color filter laminated each other prevents a penetration of visible light by absorbing a visible light component which transmitted a certain color filter by other color filters.
On the other hand, as a result of each color filter's transmitting an infrared light component, infrared light is transmitted selectively.

[Patent document 1] Japanese Patent Application No. 2003-425708
[Description of the Invention]
[Problem to be solved by the invention]
[0008]
Fig.6 is a typical cross sectional view of the conventional filter array of an imaging part. When making mosaic shape carry out mixture arrangement of the light-receiving part 60 which detects each color component of visible light, and the light-receiving part 62 which detects an infrared light component, to the light-receiving part 60 corresponding to a visible light component, One layer of color filters 66 which transmit the color component are laminated on the flattening film 64, on the other hand the color filters 66 and 68 of two or more layers are laminated on the flattening film 64 by the light-receiving part 62 corresponding to an infrared light component. Therefore, the difference arose in the thickness of the filter laminated on the flattening film 64 by the light-receiving part 62 which detects an infrared light component, and other light-receiving parts 60 which detect a visible light component, and when forming a structure on these filters, there was a problem that trouble might be caused. For example, when film thickness of the flattening film 70 formed on a filter was made thin, reservation of surface smoothness became difficult, and when it was going to secure surface smoothness on the contrary, there was a problem that film thickness became thick.
[0009]
The present invention is made in order to solve the above-mentioned problem.
The purpose is to provide a solid state image pickup device which improves the surface smoothness of the surface of a solid state image pickup device after color filter formation, and makes easy prevention from deterioration of resolution by optical refraction in a flattening film on a color filter, and formation of a microlens array which may be further laminated on a color filter.

[Means for solving problem]
[0010]
Two or more kinds of visible light component photo detectors in which the colored filter which transmits the color from which the solid state imaging device concerning the present invention differs each other was laminated on the light receiving surface via the respectively transparent foundation layer, In that by which the infrared light component photo detector in which the infrared light transmission filter which transmits an infrared light component selectively was laminated on the light receiving surface via the aforementioned foundation layer was arranged,

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The aforementioned foundation layer is formed on the light receiving surface of the aforementioned infrared light component photo detector more thinly than the light receiving surface top of the aforementioned visible light component photo detector, and the aforementioned infrared light transmission filter laminates two or more kinds of colored filters which transmit infrared light among the aforementioned colored filters, and comprises on the aforementioned foundation layer in them.

[0011]

The suitable modes of the present invention is a red transmission filter which transmits the component according to red as the aforementioned colored filter. And it has a blue transmission filter which transmits the component to which it responded blue, and the aforementioned infrared light transmission filter is a solid state imaging device which laminates the aforementioned red transmission filter and the above-mentioned blue transmission filter, and is constituted.

[0012]

Two or more kinds of visible light component photo detectors in which the colored filter which transmits the color from which the manufacturing method of the solid state imaging device concerning the present invention differs each other was laminated on the light receiving surface, respectively, In the method of manufacturing the solid state imaging device with which the infrared light component photo detector in which the infrared light transmission filter which transmits an infrared light component selectively was laminated on the light receiving surface was arranged, The process of forming a transparent foundation layer in common on the aforementioned light receiving surface of each aforementioned visible light component photo detector and the aforementioned infrared light component photo detector, The infrared light transmission filter formation process which forms the aforementioned infrared light transmission filter, The etching step which it ****, and the aforementioned infrared light transmission filter formation process etches the aforementioned foundation layer, and forms the concave part of the aforementioned foundation layer on the aforementioned light receiving surface of the aforementioned infrared light component photo detector, The lower filter formation process laminated on the aforementioned concave part by using as a lower filter at least one kind of colored filter which transmits infrared light among the aforementioned colored filters, It has an upper filter formation process laminated on the lower filter concerned by using as an upper filter the colored filter of a kind which transmits infrared light among the aforementioned colored filters, and is different from the aforementioned lower filter.

[0013]

Other manufacturing methods of the solid state imaging device concerning the present invention, Two or more kinds of visible light component photo detectors in which the colored filter which transmits each other different color was laminated on the light receiving surface, respectively, In the method of manufacturing the solid state imaging device with which the infrared light component photo detector in which the infrared light transmission filter which transmits an infrared light component selectively was laminated on the light receiving surface was arranged, The process of forming a transparent foundation layer in common on the aforementioned light receiving surface of each aforementioned visible light component photo detector and the aforementioned infrared light component photo detector, The infrared light transmission filter formation process which forms the aforementioned infrared light transmission filter, The recessed-parts-forming process at which it **** and the aforementioned infrared light transmission filter formation process forms the concave part of the aforementioned foundation layer on the aforementioned light receiving surface of the aforementioned infrared light component photo detector, The lower filter formation process laminated on the aforementioned concave part by using as a lower filter at least one kind of

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colored filter which transmits infrared light among the aforementioned colored filters, It has an upper filter formation process laminated on the lower filter concerned by using as an upper filter the colored filter of a kind which transmits infrared light among the aforementioned colored filters, and is different from the aforementioned lower filter.

[0014]

The suitable modes of the present invention is a manufacturing method which forms either of the blue transmission filters which transmit the red transmission filter which transmits the component according to red, and the component to which it responded blue as the aforementioned lower filter, and forms the other as above-mentioned upper filter.

[Effect of the Invention]

[0015]

According to the present invention, on an infrared light component photo detector, the foundation layer of a colored filter becomes depressed and is formed from a visible light component photo detector top. The infrared light transmission filter formed by laminating a plurality of colored filters becomes thick compared with the colored filter on a visible light component photo detector. However, since the infrared light transmission filter concerned is formed in the dent (concave part) of a foundation layer, flattening of the surface of an infrared light transmission filter and the colored filter on a visible light component photo detector is attained.

[Best Mode of Carrying Out the Invention]

[0016]

Hereinafter, based on Drawings, it describes about an embodiment of the invention (henceforth an embodiment).

[0017]

Fig.1 is a typical plan view showing the composition of the CCD series concerning this embodiment. This CCD series is a frame transmission type thing, and is constituted including the imaging part 2, the accumulating part 4, the horizontal transfer part 6, and the outputting part 8 which are formed on a semiconductor substrate.

[0018]

The imaging part 2 consists of a plurality of CCD shift registers (vertical shift register 10) extended to a line direction (vertical direction), and these vertical shift registers 10 are arranged by the line writing direction (horizontal). Each bit of the vertical shift register 10 which constitutes the imaging part 2 functions as a light-receiving part which constitutes a pixel, respectively.

[0019]

A color filter is arranged corresponding to each light-receiving part, and the light component in which a light-receiving part has sensitivity becomes settled according to the penetration characteristic of the color filter. Here, 2x2-pixel arrangement constitutes the unit of the arrangement of a light-receiving part. For example, the light-receiving parts 12, 14, 16, and 18 constitute this unit.

[0020]

The light-receiving parts 12, 14, and 16 have G filter, R filter, and B filter arranged, respectively. Each of these filters have the penetration characteristic shown in Fig.5. The light-receiving part 12 generates the signal charge according to G component and IR component to the incident light containing an infrared light component (IR component). Similarly, the light-receiving part 14 generates the signal charge according to R component and IR component, and the light-receiving part 16 generates the signal charge according to B component and IR component.

[0021]

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The light-receiving part 18 has an IR filter (infrared light transmission filter) which transmits an infrared light component selectively arranged, and generates the signal charge according to IR component in incident light. This IR filter can laminate and constitute R filter and B filter. Because, in order that B component which transmits B filter among visible light may not transmit R filter and R component which transmits R filter on the other hand may not transmit B filter, it is letting both filters pass, It is because a visible light component is removed fundamentally and IR component which transmits both filters remains in the transmitted light chiefly.

[0022]

The 2x2-pixel composition concerned is repeatedly arranged by the imaging part 2 to vertical direction and each horizontal direction.

[0023]

The accumulating part 4 as well as the imaging part 2 consists of a plurality of vertical shift registers 20. Each vertical shift register 20 is provided corresponding to the vertical shift register 10 of the imaging part 2, respectively, and the input terminal is connected to the outgoing end of the vertical shift register 10. The vertical shift register 20 holds the signal charge in which vertical transfer was carried out at high speed by frame transfer operation from the imaging part 2, and carries out vertical transfer of every one line of the signal charge to the horizontal transfer part 6.

[0024]

The horizontal transfer part 6 comprises CCD shift registers, and the outgoing end of the vertical shift register 20 is connected to each of that bit. After the horizontal transfer part 6 receives the signal charges for one line outputted in parallel from a plurality of vertical shift registers 20, it turns these signal charges to the outputting part 8, and carries out horizontal transfer.

[0025]

The outputting part 8 converts the signal charge outputted from the horizontal transfer part 6 to a voltage signal, and outputs it as a picture signal.

[0026]

Each vertical shift register 10 is the impurity diffused layer formed in the semiconductor substrate, and it becomes a charge transfer passage and it is constituted including a plurality of vertical transfer electrodes which were extended and formed at the line writing direction the channel regions which function also as a light-receiving part, and on the semiconductor substrate, and were arranged in the line direction.

[0027]

On a semiconductor substrate, the wiring layer formed with an Al film is laminated further, for example. The clock wiring etc. which are extended along the channel stop top which patterns this and separates between adjoining channel regions are formed. Here, clock wiring applies a transfer clock to a vertical transfer electrode. After laminating the flattening film which consists of a transparent material on this wiring layer, above-mentioned R, G, B filter, and the filter array which consists of an IR filter are further formed on it.

[0028]

Fig.2 is a typical perspective view showing the manufacturing method of the filter array of an imaging part. Fig.3 and Fig.4 are the typical cross sectional views showing the manufacturing method of the filter array of an imaging part. These figures take out and show the above-mentioned light-receiving parts 12-18. Fig.3 shows signs that the direction of the light-receiving parts 12 and 14 was seen, from the vertical section which passes along the light-receiving parts 16 and 18, and Fig.4 shows signs that the direction of the light-receiving parts 12 and 16 was seen from the vertical section which passes along the light-receiving parts 14

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and 18. As mentioned above, after a transfer electrode and a wiring layer are formed on the semiconductor substrate 30, the flattening film 32 is formed (Fig.2 (a), Fig.3 (a), Fig.4 (a)). The transfer electrode and the wiring layer are omitted in Fig.2 - Fig.4.

[0029]

The flattening film 32 is etched in the portion on the light receiving surface of the light-receiving part 18, after being formed so that the surface may once become flat as shown in Fig.2 (a), Fig.3 (a), and Fig.4 (a). Thereby, the concave part 34 is formed on the light receiving surface of the light-receiving part 18 at the flattening film 32 (Fig.2 (b), Fig.3 (b), Fig.4 (b)). For example using photolithography technique, this etching is performed, after forming the mask layer to etching in portions other than light-receiving part 18 among flattening membrane surfaces. Etching quantity, i.e., the depth of a concave part, is set up according to the thickness of B filter laminated on this concave part 34 at the following process.

[0030]

The B filter 36 is laminated on the concave part 34 on the light-receiving part 18 (Fig.2 (c), Fig.3 (c), Fig.4 (c)). This B filter 36 is formed using the photopolymer colored blue, for example. For example, after being applied by methods, such as a spin coat, all over a semiconductor substrate, the photopolymer concerned is exposed using a photo mask and is further developed. A photopolymer is patterned by this exposure and developing process so that it may remain only in the portion of the concave part 34, and the B filter 36 is formed. The depth of the concave part 34 and the film thickness of the B filter 36 are defined so that the B filter 36 may be embedded in the concave part 34, for example, the top surface may serve as height comparable as the surface of the surrounding flattening film 32 of the concave part 34.

[0031]

Subsequently, the B filter 38 is laminated on the light-receiving part 16 by the same method as the B filter 36 (Fig.2 (d), Fig.3 (d), Fig.4 (d)). The G filter 40 is too laminated on the light-receiving part 12 by the same method as the B filter 36 (Fig.2 (e), Fig.3 (e), Fig.4 (e)). Since these B filters 38 and the G filter 40 are formed on the flattening film 32 contiguous to the concave part 34 which was not etched, the top surface becomes higher than the B filter 36.

[0032]

The R filter 42 is laminated on the light-receiving part 14 and the light-receiving part 18. The R filter 42 is laminated on the flattening film 32 in the position of the light-receiving part 14. On the other hand, in the position of the light-receiving part 18, it laminates on the B filter 36. Here, since the height of the top surface of the B filter 36 and the surface of the flattening film 32 of the position of the light-receiving part 14 has gathered fundamentally as mentioned above, the R filter 42 can be integrally formed evenly on the light-receiving parts 14 and 18, for example (Fig.2 (f), Fig.3 (f), Fig.4 (f)).

[0033]

A color filter is laminated on each light-receiving part by the above process. Although a two-layer color filter called the B filter 36 and the R filter 42 is laminated on the light-receiving part 18 which detects IR component and an IR filter is formed in it, The filter of the two-layer eye formed on the light-receiving part 18 is prevented from projecting from the filter of a surrounding light-receiving part by having provided the concave part 34 to the flattening film 32 of the ground, and having embedded the color filter of one layer in the concave part 34. That is, the surface smoothness of the surface of the filter array formed on each light-receiving part 12-18 improves. The flattening film 44 is laminated on this surface (Fig.2 (g), Fig.3 (g), Fig.4 (g)). Since boom hoisting of the surface of the filter array used as the ground of the flattening film 44 is inhibited as mentioned above, the flattening film 44 can realize flattening of the imaging part 2 surface by comparatively thin film thickness.

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[0034]
Although frame transmission type CCD series was shown here, an interline transmission type etc. can apply the present invention also to other things of a type and C-MOS image sensors.
[0035]
When the set of the color filter of a complementary color system is used, three, Cy filter, Mg filter, and Ye filter, can be laminated, and an IR filter can be constituted. In this case, the concave part 34 is formed in the depth for color filter two-layer. Thereby, the height of the surface of the color filter of the 3rd layer of the top layer which constitutes an IR filter, and the color filter of the light-receiving part for surrounding visible light can be arranged.
[Brief Description of the Drawings]
[0036]
[Drawing 1]It is a typical plan view showing the composition of the CCD series concerning an embodiment.
[Drawing 2]It is a typical perspective view showing each process of the manufacturing method of the filter array of an imaging part.
[Drawing 3]It is a typical cross sectional view showing each process of the manufacturing method of the filter array of an imaging part.
[Drawing 4]It is a typical cross sectional view showing each process of the manufacturing method of the filter array of an imaging part.
[Drawing 5]It is a graph which shows the wavelength characteristic of the transmissivity of RGB each filter, and the spectral sensitivity characteristic of a light-receiving part.
[Drawing 6]It is a typical cross sectional view of the conventional filter array of an imaging part.
[Explanations of letters or numerals]
[0037]
2 An imaging part and 4 [A horizontal transfer part and 8 / A light-receiving part and 30 / A flattening film and 34 / A concave part, 36, 38 B filter, 40 G filter, 42 R filter.] An outputting part, 10, 20 vertical shift registers, and 12-18 A semiconductor substrate, and 32 and 44 An accumulating part and 6

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DRAWINGS

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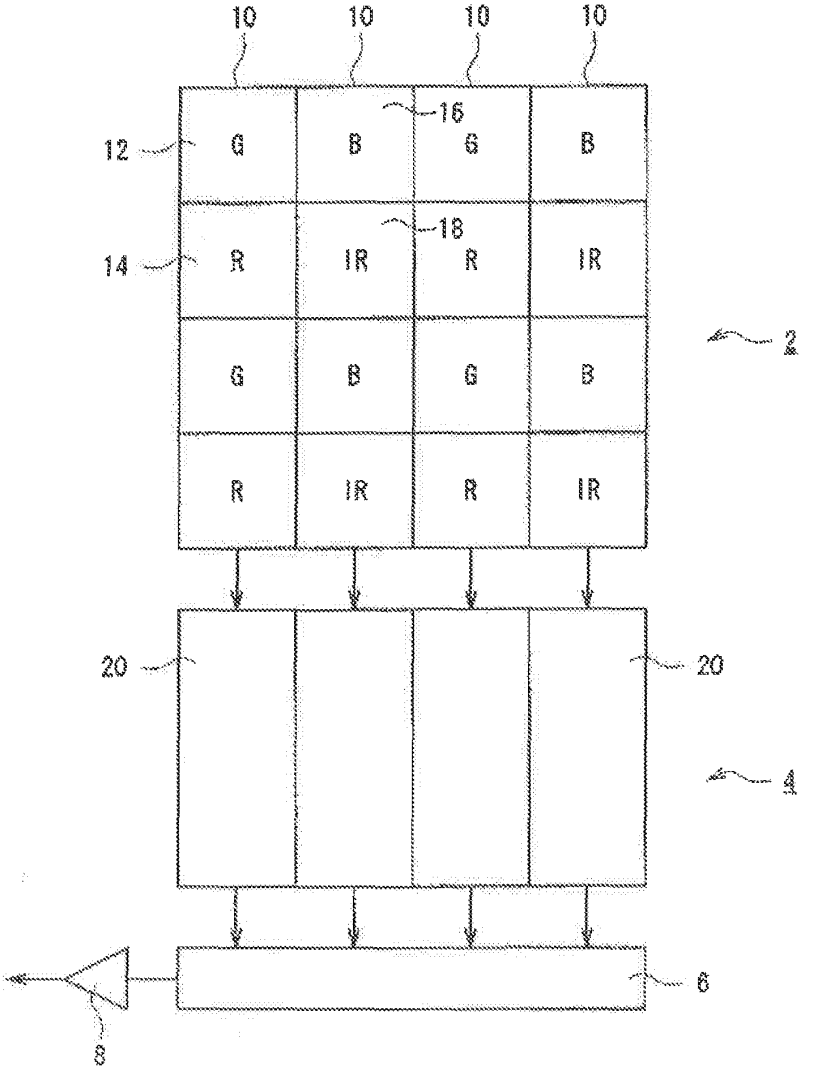
DRAWINGS

[Drawing 1]



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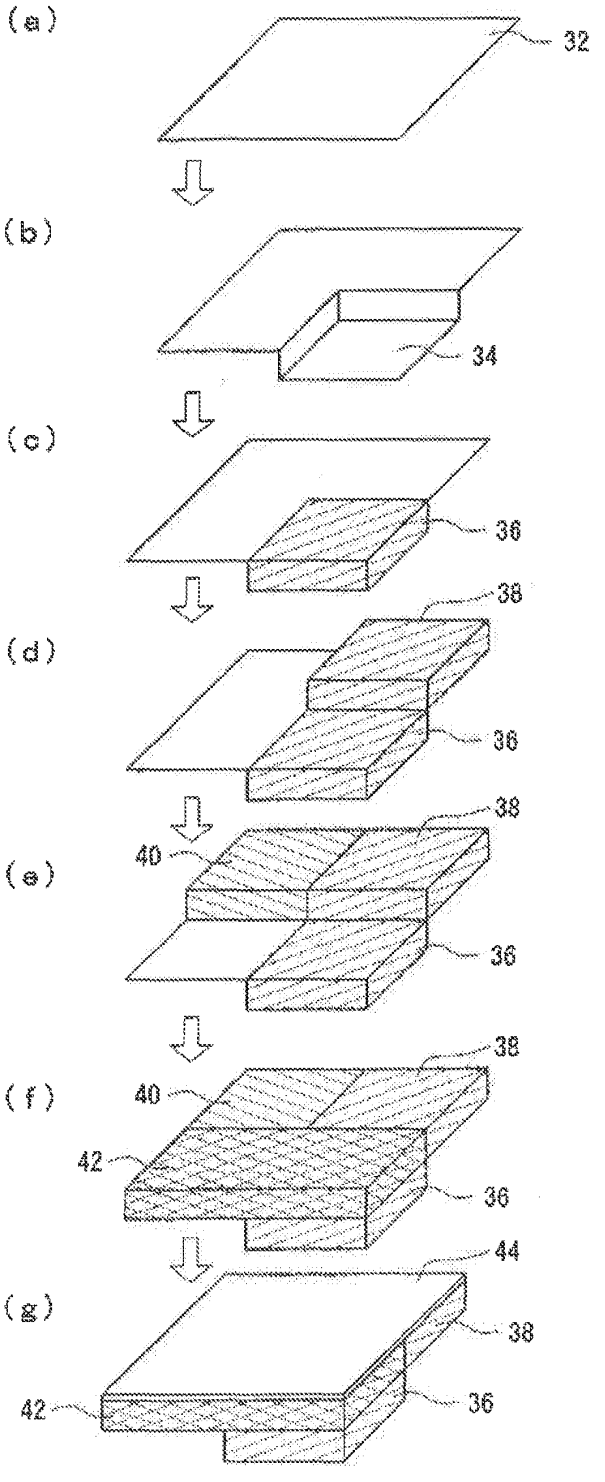
[Drawing 2]



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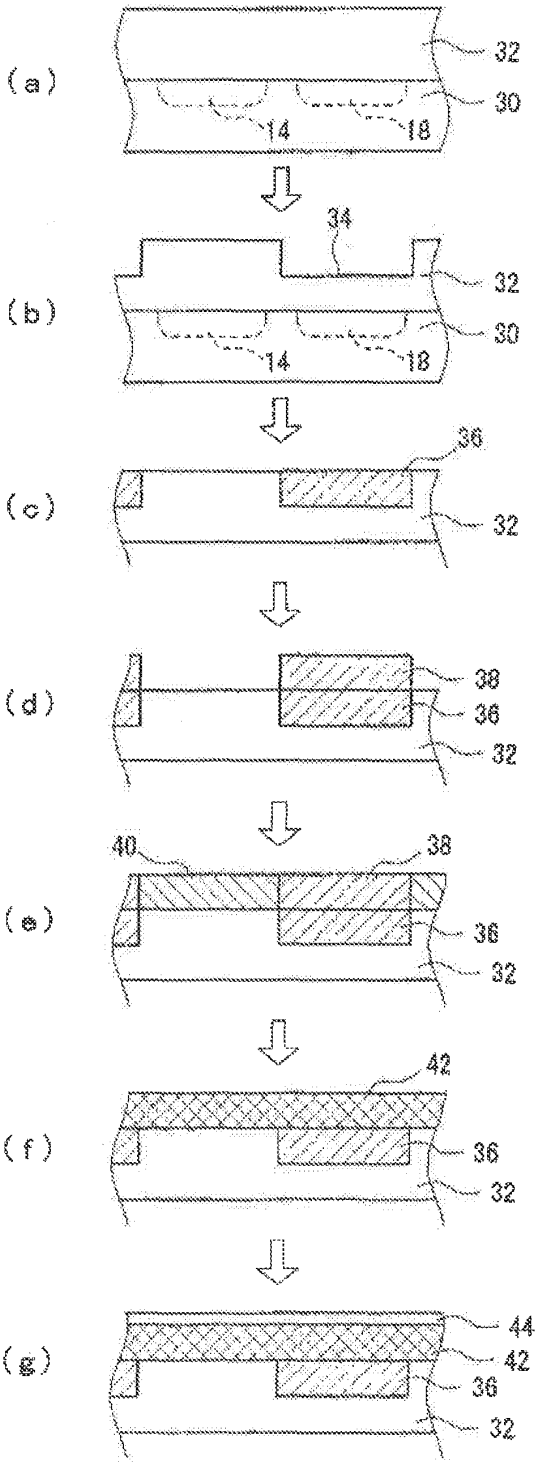

[Drawing 3]

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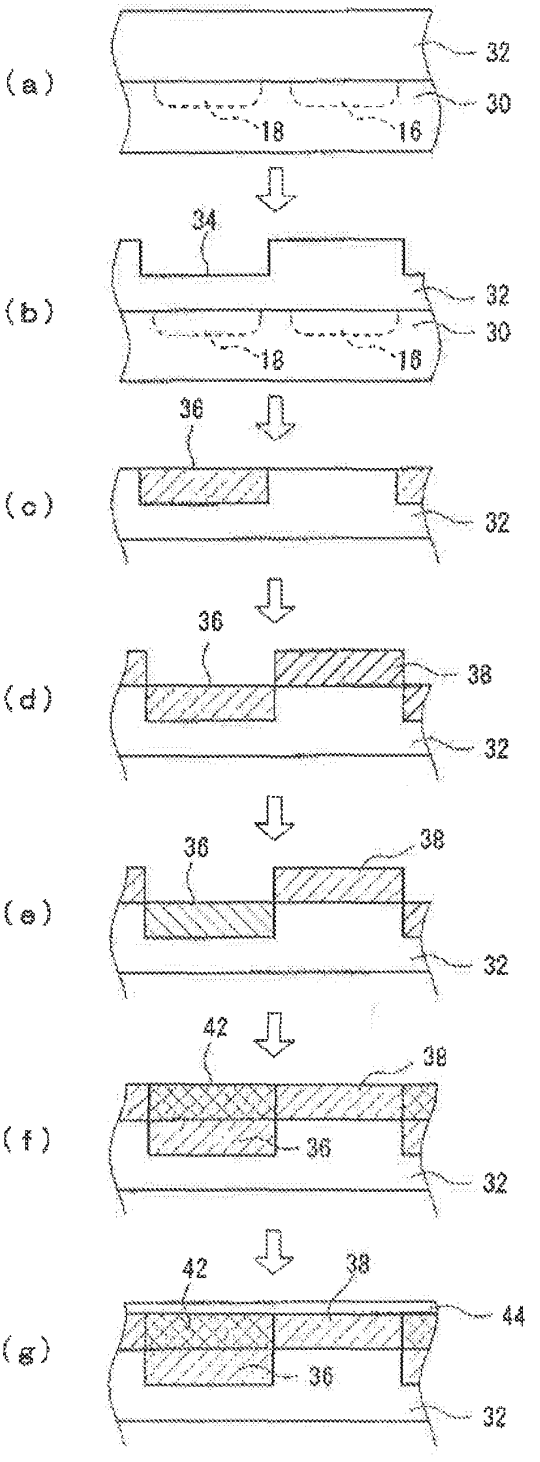

[Drawing 4]

[Drawing 5]

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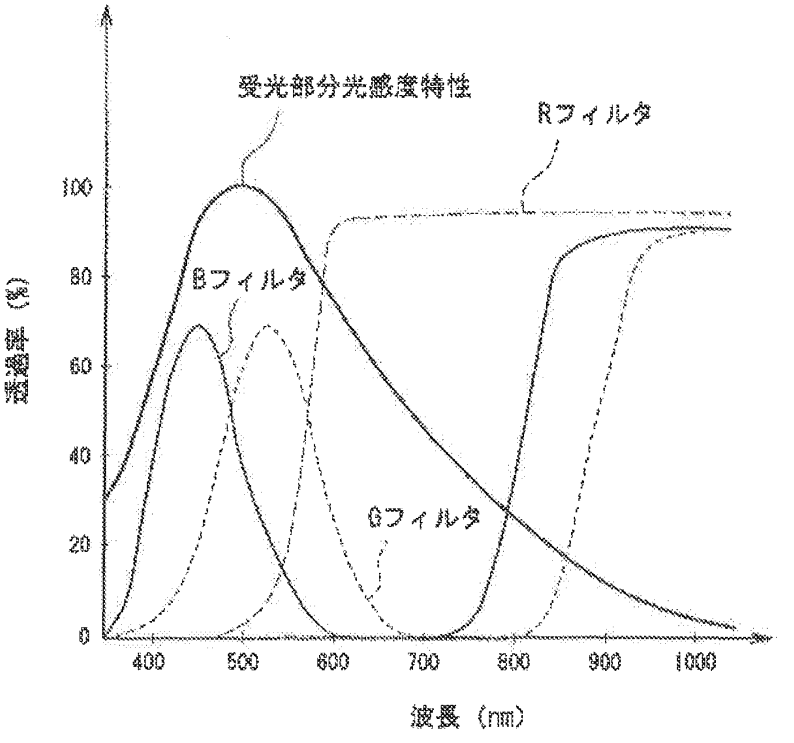

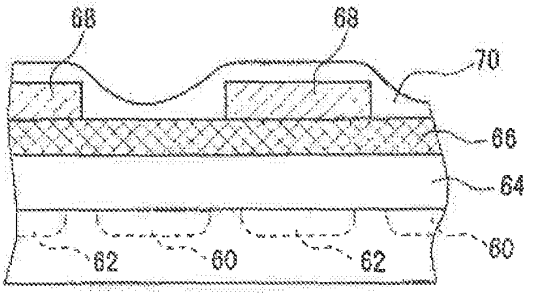

[Drawing 6]

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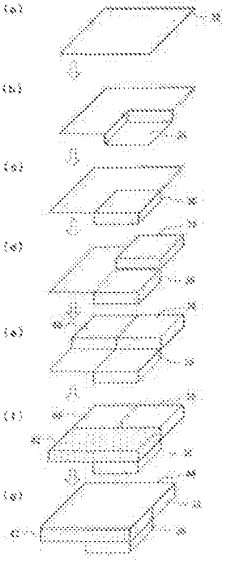
(54)【発明の名称】固体撮像装置及びその製造方法

(57)【要約】
【課題】　ＲＧＢ色成分を検知するＲ，Ｇ，Ｂ各画素と赤外光成分を検知するＩＲ画素とが配列された固体撮像素子において、ＩＲ画素に積層されるＩＲ透過フィルタが厚い分，撮像部表面に凹凸が生じる。
【解決手段】　半導体基板３０上には、転送電極や配線を形成した後，平坦化膜３２が形成される。ＩＲ画素に対応する位置の平坦化膜３２をエッチングして、凹部３４を形成する。ＩＲ画素の上には、この凹部３４にＢフィルタ３６を埋め込み、さらにＲフィルタ４２を積層する。Ｒ，Ｇ，Ｂ画素の上には、エッチングされていない平坦化膜３２を下地として、それぞれＲ，Ｇ，Ｂフィルタを積層する。凹部３４の深さをカラーフィルタ１層分に応じたものとすることで、ＲＧＢ画素及びＩＲ画素に形成されたフィルタアレイの表面の高さが揃う。
【選択図】　図２



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【特許請求の範囲】
【請求項１】
互いに異なる色を透過する色フィルタがそれぞれ透明の下地層を介して受光面上に積層された複数種類の可視光成分受光素子と、赤外光成分を選択的に透過する赤外光透過フィルタが前記下地層を介して受光面上に積層された赤外光成分受光素子とが配列された固体撮像装置において、
前記下地層は、前記赤外光成分受光素子の受光面上にて、前記可視光成分受光素子の受光面上より浅く形成され、
前記赤外光透過フィルタは、前記色フィルタのうち赤外光を透過する複数種類の色フィルタを前記下地層上にて積層して構成されること、
を特徴とする固体撮像装置。
【請求項２】
請求項１に記載の固体撮像装置において、
前記色フィルタとして、赤色に応じた成分を透過する赤色透過フィルタ、及び青色に応じた成分を透過する青色透過フィルタを有し、
前記赤外光透過フィルタは、前記赤色透過フィルタ及び前記青色透過フィルタを積層して構成されること、
を特徴とする固体撮像装置。
【請求項３】
互いに異なる色を透過する色フィルタがそれぞれ受光面上に積層された複数種類の可視光成分受光素子と、赤外光成分を選択的に透過する赤外光透過フィルタが受光面上に積層された赤外光成分受光素子とが配列された固体撮像装置を製造する方法において、
前記各可視光成分受光素子及び前記赤外光成分受光素子の前記受光面上に共通に、透明の下地層を形成する工程と、
前記赤外光透過フィルタを形成する赤外光透過フィルタ形成工程と、
を有し、
前記赤外光透過フィルタ形成工程は、
前記下地層をエッチングして前記赤外光成分受光素子の前記受光面上に前記下地層の凹部を形成するエッチング工程と、
前記色フィルタのうち赤外光を透過する少なくとも１種類の色フィルタを下部フィルタとして前記凹部に積層する下部フィルタ形成工程と、
前記色フィルタのうち赤外光を透過し、かつ前記下部フィルタとは異なる種類の色フィルタを上部フィルタとして当該下部フィルタ上に積層する上部フィルタ形成工程と、
を有することを特徴とする製造方法。
【請求項４】
互いに異なる色を透過する色フィルタがそれぞれ受光面上に積層された複数種類の可視光成分受光素子と、赤外光成分を選択的に透過する赤外光透過フィルタが受光面上に積層された赤外光成分受光素子とが配列された固体撮像装置を製造する方法において、
前記各可視光成分受光素子及び前記赤外光成分受光素子の前記受光面上に共通に、透明の下地層を形成する工程と、
前記赤外光透過フィルタを形成する赤外光透過フィルタ形成工程と、
を有し、
前記赤外光透過フィルタ形成工程は、
前記赤外光成分受光素子の前記受光面上に前記下地層の凹部を形成する凹部形成工程と、
前記色フィルタのうち赤外光を透過する少なくとも１種類の色フィルタを下部フィルタとして前記凹部に積層する下部フィルタ形成工程と、
前記色フィルタのうち赤外光を透過し、かつ前記下部フィルタとは異なる種類の色フィルタを上部フィルタとして当該下部フィルタ上に積層する上部フィルタ形成工程と、
を有することを特徴とする製造方法。

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【請求項５】
請求項３又は請求項４に記載の製造方法において、
赤色に応じた成分を透過する赤色透過フィルタ及び青色に応じた成分を透過する青色透過フィルタのいずれか一方を前記下部フィルタとして形成し、他方を前記上部フィルタとして形成することを特徴とする固体撮像装置の製造方法。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明は、固体撮像装置及びその製造方法に関し、特に、赤外領域に感度を有する受光素子を含んだ固体撮像装置におけるオンチップカラーフィルタに関する。
【背景技術】
【０００２】
ビデオカメラやデジタルカメラに搭載されるＣＣＤ（Charge Coupled Device）イメージセンサ等の固体撮像素子（固体撮像装置）は二次元配列された受光部（受光素子）を有し、この受光部で入射光を光電変換して電気的な画像信号を生成する。受光部自体は、波長が３８０～７８０ｎｍ程度の可視光領域全般に加え、さらに長波長の近赤外領域まで感度を有する。そのため、カラー画像を取得するために、透過光の色、つまり透過波長領域が異なる複数種類のカラーフィルタを受光面上に配置する。カラーフィルタは、受光面上に透明な平坦化膜を形成した後、この平坦化膜の上に積層される。また、カラーフィルタの上にはさらに別途の平坦化膜や保護膜が積層される。
【０００３】
カラーフィルタには、透過光が赤（Ｒ）、緑（Ｇ）及び青（Ｂ）である原色系のフィルタセットや、シアン（Ｃｙ）、マゼンタ（Ｍｇ）及びイエロー（Ｙｅ）である補色系のフィルタセットがある。これらカラーフィルタは例えば、有機材料を着色して構成され、それぞれ対応する色の可視光を透過するが、その材質上、赤外光も透過する。例えば、図５は、ＲＧＢ各フィルタの透過率の波長特性を示すグラフであり、同図は受光部の分光感度特性も併せて示している。
【０００４】
受光部は赤外光にも感度を有するため、赤外光成分が入射すると当該成分による信号電荷が発生し、正しい色表現ができない。そのため、従来は、カメラのレンズと固体撮像素子との間に、別途、赤外カットフィルタを配置している。
【０００５】
この赤外カットフィルタは、赤外光をカットすると同時に、可視光も１０～２０％程度、減衰させる。そのため、受光部に入射する可視光の強度が減少し、それに応じて出力信号のＳ／Ｎ比が低下し、画質の劣化を招くという問題があった。
【０００６】
この問題への対処として、赤外カットフィルタを無くす一方で、基本的に入射光中の赤外光成分のみを検出する受光部を設け、当該受光部から得られる赤外光成分に関する情報に基づき、正しい色を再現する信号処理を行う方法が考えられる。
【０００７】
赤外光成分のみを検出する受光部は、その受光面上に互いに異なる色の可視光を透過する複数種類のカラーフィルタを積層することにより実現できる。すなわち、互いに積層されたカラーフィルタは、あるカラーフィルタを透過した可視光成分を他のカラーフィルタで吸収することにより可視光の透過を阻止する一方、各カラーフィルタが赤外光成分を透過する結果、赤外光を選択的に透過する。
【特許文献１】特願２００３－４２５７０８号
【発明の開示】
【発明が解決しようとする課題】
【０００８】
図６は、撮像部の従来のフィルタアレイの模式的な断面図である。可視光の各色成分を

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検出する受光部６０と赤外光成分を検出する受光部６２とをモザイク状に混在配置させる場合，可視光成分に対応する受光部６０には、平坦化膜６４の上にその色成分を透過するカラーフィルタ６６が１回だけ積層され、これに対して、赤外光成分に対応する受光部６２には、平坦化膜６４の上に複数層のカラーフィルタ６６，６８が積層される。そのため、赤外光成分を検出する受光部６２と可視光成分を検出する他の受光部６０とで平坦化膜６４の上に積層されるフィルタの厚みに差異が生じ、それらフィルタ上に構造物を形成する際に支障を来し得るという問題があった。例えば、フィルタ上に形成される平坦化膜７０の膜厚を薄くすると平坦性の確保が難しくなり、反対に平坦性を確保しようとすると膜厚が厚くなるという問題があった。

【０００９】

本発明は上記問題を解決するためになされたものであり、カラーフィルタ形成後の固体撮像素子の表面の平坦性を向上し、カラーフィルタ上の平坦化膜での光の屈折による解像度の低下防止や、さらにカラーフィルタ上に積層され得るマイクロレンズアレイの形成を容易とする固体撮像素子を提供することを目的とする。

【課題を解決するための手段】

【００１０】

本発明に係る固体撮像装置は、互いに異なる色を透過する色フィルタがそれぞれ透明の下地層を介して受光面上に積層された複数種類の可視光成分受光素子と、赤外光成分を選択的に透過する赤外光透過フィルタが前記下地層を介して受光面上に積層された赤外光成分受光素子とが配列されたものにおいて、前記下地層が，前記赤外光成分受光素子の受光面上にて、前記可視光成分受光素子の受光面上より薄く形成され、前記赤外光透過フィルタが、前記色フィルタのうち赤外光を透過する複数種類の色フィルタを前記下地層上にて積層して構成される。

【００１１】

本発明の好適な態様は、前記色フィルタとして、赤色に応じた成分を透過する赤色透過フィルタ、及び青色に応じた成分を透過する青色透過フィルタを有し、前記赤外光透過フィルタが，前記赤色透過フィルタ及び前記青色透過フィルタを積層して構成される固体撮像装置である。

【００１２】

本発明に係る固体撮像装置の製造方法は、互いに異なる色を透過する色フィルタがそれぞれ受光面上に積層された複数種類の可視光成分受光素子と、赤外光成分を選択的に透過する赤外光透過フィルタが受光面上に積層された赤外光成分受光素子とが配列された固体撮像装置を製造する方法において、前記各可視光成分受光素子及び前記赤外光成分受光素子の前記受光面上に共通に、透明の下地層を形成する工程と，前記赤外光透過フィルタを形成する赤外光透過フィルタ形成工程と、を有し、前記赤外光透過フィルタ形成工程が、前記下地層をエッチングして前記赤外光成分受光素子の前記受光面上に前記下地層の凹部を形成するエッチング工程と、前記色フィルタのうち赤外光を透過する少なくとも１種類の色フィルタを下部フィルタとして前記凹部に積層する下部フィルタ形成工程と，前記色フィルタのうち赤外光を透過し、かつ前記下部フィルタとは異なる種類の色フィルタを上部フィルタとして当該下部フィルタ上に積層する上部フィルタ形成工程と，を有するものである。

【００１３】

本発明に係る固体撮像装置の他の製造方法は、互いに異なる色を透過する色フィルタがそれぞれ受光面上に積層された複数種類の可視光成分受光素子と、赤外光成分を選択的に透過する赤外光透過フィルタが受光面上に積層された赤外光成分受光素子とが配列された固体撮像装置を製造する方法において、前記各可視光成分受光素子及び前記赤外光成分受光素子の前記受光面上に共通に、透明の下地層を形成する工程と、前記赤外光透過フィルタを形成する赤外光透過フィルタ形成工程と、を有し、前記赤外光透過フィルタ形成工程が，前記赤外光成分受光素子の前記受光面上に前記下地層の凹部を形成する凹部形成工程と、前記色フィルタのうち赤外光を透過する少なくとも１種類の色フィルタを下部フィル

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タとして前記凹部に積層する下部フィルタ形成工程と、前記色フィルタのうち赤外光を透過し、かつ前記下部フィルタとは異なる種類の色フィルタを上部フィルタとして当該下部フィルタ上に積層する上部フィルタ形成工程と、を有するものである。

【００１４】

本発明の好適な態様は、赤色に応じた成分を透過する赤色透過フィルタ及び青色に応じた成分を透過する青色透過フィルタのいずれか一方を前記下部フィルタとして形成し、他方を前記上部フィルタとして形成する製造方法である。

【発明の効果】

【００１５】

本発明によれば、色フィルタの下地層が可視光成分受光素子上より赤外光成分受光素子上にて窪んで形成される。複数の色フィルタを積層して形成される赤外光透過フィルタは可視光成分受光素子上の色フィルタに比べて厚くなる。しかし、当該赤外光透過フィルタは下地層の窪み（凹部）に形成されるので、赤外光透過フィルタと可視光成分受光素子上の色フィルタとの表面の平坦化が図られる。

【発明を実施するための最良の形態】

【００１６】

以下、本発明の実施の形態（以下実施形態という）について、図面に基づいて説明する。

【００１７】

図１は、本実施形態に係るＣＣＤイメージセンサの構成を示す模式的な平面図である。このＣＣＤイメージセンサはフレーム転送型のものであり、半導体基板上に形成される撮像部２、蓄積部４、水平転送部６、及び出力部８を含んで構成される。

【００１８】

撮像部２は、列方向（垂直方向）に延びる複数のＣＣＤシフトレジスタ（垂直シフトレジスタ１０）からなり、これら垂直シフトレジスタ１０は行方向（水平方向）に配列される。撮像部２を構成する垂直シフトレジスタ１０の各ビットは、それぞれ画素を構成する受光部として機能する。

【００１９】

各受光部に対応してカラーフィルタが配置され、そのカラーフィルタの透過特性に応じて、受光部が感度を有する光成分が定まる。ここでは、２×２画素の配列が受光部の配列の単位を構成する。例えば、受光部１２、１４、１６、１８がこの単位を構成する。

【００２０】

受光部１２、１４、１６はそれぞれＧフィルタ、Ｒフィルタ、Ｂフィルタを配置される。これら各フィルタは例えば、図５に示す透過特性を有する。赤外光成分（ＩＲ成分）を含む入射光に対して、受光部１２はＧ成分及びＩＲ成分に応じた信号電荷を発生する。また、同様に、受光部１４はＲ成分及びＩＲ成分に応じた信号電荷を発生し、受光部１６はＢ成分及びＩＲ成分に応じた信号電荷を発生する。

【００２１】

受光部１８は、赤外光成分を選択的に透過するＩＲフィルタ（赤外光透過フィルタ）を配置され、入射光中のＩＲ成分に応じた信号電荷を発生する。このＩＲフィルタは、ＲフィルタとＢフィルタとを積層して構成することができる。なぜならば、可視光のうちＢフィルタを透過するＢ成分はＲフィルタを透過せず、一方、Ｒフィルタを透過するＲ成分はＢフィルタを透過しないため、両フィルタを通すことで、基本的に可視光成分が除去され、もっぱら透過光には両フィルタを透過するＩＲ成分が残るからである。

【００２２】

撮像部２には、当該２×２画素の構成が垂直方向、水平方向それぞれに繰り返して配列される。

【００２３】

蓄積部４も撮像部２と同様に複数の垂直シフトレジスタ２０からなる。各垂直シフトレジスタ２０は、それぞれ撮像部２の垂直シフトレジスタ１０に対応して設けられ、その入

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力端が垂直シフトレジスタ１０の出力端に接続される。垂直シフトレジスタ２０は撮像部２からフレーム転送動作により高速に垂直転送された信号電荷を保持し、その信号電荷を１行ずつ水平転送部６へ垂直転送する。

【００２４】

水平転送部６は、ＣＣＤシフトレジスタで構成され、その各ビットに垂直シフトレジスタ２０の出力端が接続される。水平転送部６は、複数の垂直シフトレジスタ２０から並列に出力される１行分の信号電荷を受け取った後、それら信号電荷を出力部８へ向けて水平転送する。

【００２５】

出力部８は、水平転送部６から出力される信号電荷を電圧信号に変換し、画像信号として出力する。

【００２６】

各垂直シフトレジスタ１０は、半導体基板に形成された不純物拡散層であって電荷転送路となると共に、受光部としても機能するチャネル領域と、半導体基板上に行方向に延在して形成され、かつ列方向に配列された複数の垂直転送電極とを含んで構成される。

【００２７】

半導体基板上には、さらに、例えば、Ａｌ膜で形成される配線層が積層される。これをパターニングして、隣接するチャネル領域間を分離するチャネルストップ上に沿って延びるクロック配線等が形成される。ここで、クロック配線は垂直転送電極に転送クロックを印加する。この配線層の上に透明な材質からなる平坦化膜を積層した後、さらにその上に上述のＲ，Ｇ，Ｂフィルタ、及びＩＲフィルタからなるフィルタアレイが形成される。

【００２８】

図２は、撮像部のフィルタアレイの製造方法を示す模式的な斜視図である。また図３及び図４は、撮像部のフィルタアレイの製造方法を示す模式的な断面図である。これら図は、上述の受光部１２～１９を取り出して示したものである。図３は、受光部１６，１８を通る垂直断面から受光部１２，１４の方向を見た様子を示しており、図４は、受光部１４，１８を通る垂直断面から受光部１２，１６の方向を見た様子を示している。上述のように、半導体基板３０の上に転送電極や配線層が形成された後、平坦化膜３２が形成される（図２（ａ）、図３（ａ）、図４（ａ））。なお、図２～図４では転送電極や配線層は省略されている。

【００２９】

平坦化膜３２は、図２（ａ）、図３（ａ）、図４（ａ）に示すように一旦、その表面が平坦となるように形成された後、受光部１８の受光面上の部分をエッチングされる。これにより、平坦化膜３２には受光部１８の受光面上に凹部３４が形成される（図２（ｂ）、図３（ｂ）、図４（ｂ））。このエッチングは、例えば、フォトリソグラフィ技術を用いて、平坦化膜表面のうち受光部１８以外の部分にエッチングに対するマスク層を形成した上で行われる。また、エッチング量、つまり凹部の深さは、次の工程でこの凹部３４に積層されるＢフィルタの厚さに応じて設定される。

【００３０】

受光部１８上の凹部３４には、Ｂフィルタ３６が積層される（図２（ｃ）、図３（ｃ）、図４（ｃ））。このＢフィルタ３６は、例えば、青色に着色された感光性樹脂を用いて形成される。例えば、当該感光性樹脂は、半導体基板全面にスピンコート等の方法で塗布された後、フォトマスクを用いて露光され、さらに現像される。この露光・現像工程により、感光性樹脂は、凹部３４の部分だけに残るようにパターニングされ、Ｂフィルタ３６が形成される。Ｂフィルタ３６は、凹部３４に埋め込まれ、例えば、その上面が凹部３４の周りの平坦化膜３２の表面と同程度の高さとなるように、凹部３４の深さとＢフィルタ３６の膜厚とが定められる。

【００３１】

次いで、Ｂフィルタ３６と同様の方法により、受光部１６上にＢフィルタ３８が積層される（図２（ｄ）、図３（ｄ）、図４（ｄ））。また、やはりＢフィルタ３６と同様の方

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法により、受光部１２上にＧフィルタ４０が積層される（図２（ｅ）、図３（ｅ）、図４（ｅ））。これらＢフィルタ３８及びＧフィルタ４０は、凹部３４に隣接するエッチングされなかった平坦化膜３２上に形成されるので、その上面はＢフィルタ３６より高くなる。

【００３２】

また、受光部１４と受光部１８の上にＲフィルタ４２が積層される。Ｒフィルタ４２は、受光部１４の位置では平坦化膜３２に積層される。一方、受光部１８の位置ではＢフィルタ３６に積層される。ここで、上述のようにＢフィルタ３６の上面と受光部１４の位置の平坦化膜３２の表面との高さは基本的に揃っているので、例えば、Ｒフィルタ４２は、受光部１４，１８の上に一体的に平坦に形成することができる（図２（ｆ）、図３（ｆ）、図４（ｆ））。

【００３３】

以上の工程により、各受光部の上にカラーフィルタが積層される。ＩＲ成分を検出する受光部１８には、Ｂフィルタ３６及びＲフィルタ４２という２層のカラーフィルタを積層してＩＲフィルタが形成されるが、その下地の平坦化膜３２に凹部３４を設けて、１層のカラーフィルタをその凹部３４に埋め込んだことにより、受光部１８の上に形成された２層目のフィルタが周りの受光部のフィルタより突出することが防止される。すなわち、各受光部１２～１８の上に形成されたフィルタアレイの表面の平坦性が向上する。この表面に、平坦化膜４４が積層される（図２（ｇ）、図３（ｇ）、図４（ｇ））。平坦化膜４４の下地となるフィルタアレイの表面の起伏が上述のように抑制されているので、平坦化膜４４は比較的薄い膜厚で撮像部２表面の平坦化を実現することができる。

【００３４】

なお、ここではフレーム転送型ＣＣＤイメージセンサを示したが、インターライン転送型等、他のタイプのものや、Ｃ－ＭＯＳイメージセンサにも本発明を適用することができる。

【００３５】

また、補色系のカラーフィルタのセットを用いた場合には、ＩＲフィルタをＣｙフィルタ、Ｍｇフィルタ及びＹｅフィルタの３つを積層して構成することができる。この場合には、凹部３４はカラーフィルタ２層分の深さに形成する。これにより、ＩＲフィルタを構成する最上層の３層目のカラーフィルタと、周りの可視光用の受光部のカラーフィルタとの表面の高さを揃えることができる。

【図面の簡単な説明】

【００３６】

【図１】実施形態に係るＣＣＤイメージセンサの構成を示す模式的な平面図である。

【図２】撮像部のフィルタアレイの製造方法の各工程を示す模式的な斜視図である。

【図３】撮像部のフィルタアレイの製造方法の各工程を示す模式的な断面図である。

【図４】撮像部のフィルタアレイの製造方法の各工程を示す模式的な断面図である。

【図５】ＲＧＢ各フィルタの透過率の波長特性及び受光部の分光感度特性を示すグラフである。

【図６】撮像部の従来のフィルタアレイの模式的な断面図である。

【符号の説明】

【００３７】

２　撮像部、４　蓄積部、６　水平転送部、８　出力部、１０，２０　垂直シフトレジスタ、１２～１８　受光部、３０　半導体基板、３２，４４　平坦化膜、３４　凹部、３６，３８　Ｂフィルタ、４０　Ｇフィルタ、４２　Ｒフィルタ。

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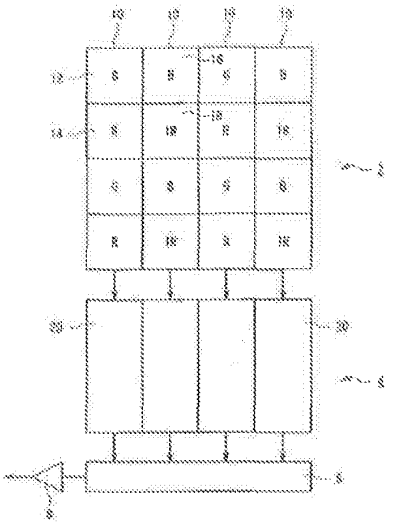
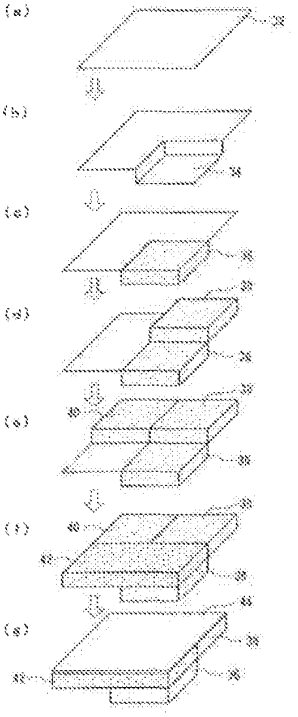
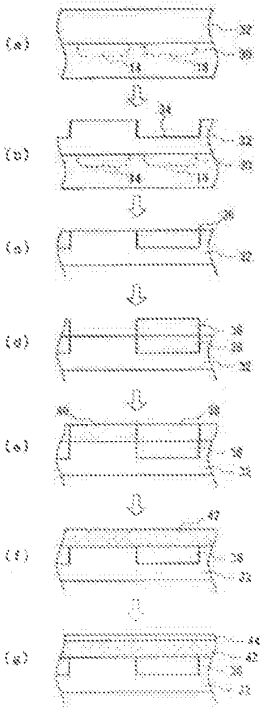
【図１】



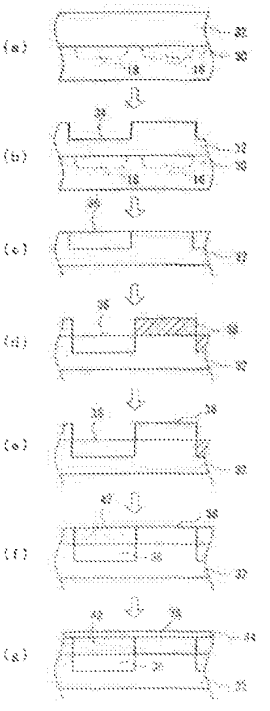
【図２】



【図３】



【図４】



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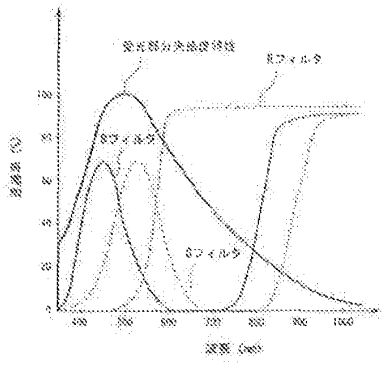
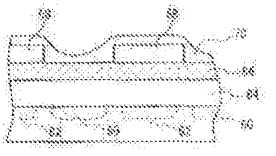
【図５】



【図６】



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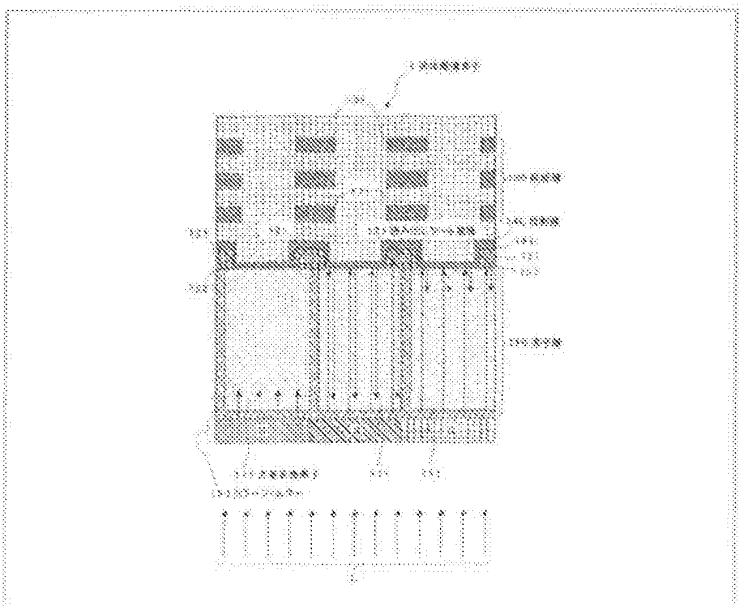
(21)Application number	2005-076498
(22)Date of filing	17.03.2005
(71)Applicant	SONY CORP
(72)Inventor	NATORI TAICHI

(54)SOLID-STATE IMAGE SENSING DEVICE, ITS MANUFACTURING METHOD AND IMAGING DEVICE

(57)Abstract

PROBLEM TO BE SOLVED: To improve sensitivity and to prevent an adjacent pixel from being mixed with colors by providing a reflection film which covers a read-out gate electrode.
SOLUTION: A plurality of unit pixels are arranged including an active device which changes and outputs signal electric charge by which photoelectric conversion is carried out to an electric signal by a photoelectric conversion element 111. A solid-state image sensing device 1 is provided with a wiring layer 130 which serves as wiring 131 to an active device, on the other side of an element layer 110 where a photoelectric conversion element 111 is formed so as to make an incidence light L penetrate a color filter 150 formed at the other side of the element layer 110 and make it enter into the photoelectric conversion element 111. It has a reflection film 140 formed so that the whole pixel surface including a read-out gate electrode 121 which reads signal electric charge where the photoelectric conversion of the active devices is carried out to the wiring layer 130 side of the element layer 110 via an insulating film 141 may be covered.



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CLAIMS

[Claim(s)]
[Claim 1]
A plurality of unit pixels containing an active device which converts a signal charge by which photoelectric conversion was carried out to an electrical signal, and outputs it by an optoelectric transducer were arranged,
It has a wiring layer which wires the surface side of one of these to the aforementioned active device to an element layer in which the aforementioned optoelectric transducer is formed,
In a solid state image pickup device which makes a light filter which formed incident light in the surface side of another side of the aforementioned element layer transmit and in which it enters the aforementioned optoelectric transducer,
A reflecting film formed so that the whole pixel surface containing a reading gate electrode which reads a signal charge in which photoelectric conversion of [of the aforementioned active devices] was carried out to the aforementioned wiring layer side of the aforementioned element layer via an insulator layer might be covered
A solid state image pickup device characterized by preparation ******.
[Claim 2]
While an opening is formed in a position which opposes to an optoelectric transducer into which red light which transmits the aforementioned light filter of the aforementioned reflecting film enters,
A reflecting layer is formed in the aforementioned wiring layer side of the aforementioned opening.
The solid state image pickup device according to claim 1 characterized by things.
[Claim 3]
Between wiring of the aforementioned wiring layer, the aforementioned reflecting layer keeps the aforementioned wiring and an interval, and is formed.
The solid state image pickup device according to claim 2 characterized by things.
[Claim 4]
The aforementioned reflecting layer is formed via an insulator layer between the aforementioned element layer and the aforementioned wiring layer.
The solid state image pickup device according to claim 2 characterized by things.
[Claim 5]
A plurality of unit pixels containing an active device which converts a signal charge by which photoelectric conversion was carried out to an electrical signal, and outputs it by an optoelectric transducer were arranged,
It has a wiring layer which wires the surface side of one of these to the aforementioned active device to an element layer in which the aforementioned optoelectric transducer is formed,
In a manufacturing method of a solid state image pickup device which makes a light filter which formed incident light in the surface side of another side of the aforementioned element

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layer transmit and in which it enters the aforementioned optoelectric transducer,
A process of forming a reading electrode which reads a signal charge to a semiconductor layer in which the aforementioned element layer is formed,
A process of forming the aforementioned optoelectric transducer in the aforementioned semiconductor layer,
A process of forming a reflecting film so that the whole pixel surface which contains the aforementioned reading electrode in a side in which the aforementioned wiring layer of the aforementioned semiconductor layer is formed via an insulator layer may be covered
A manufacturing method of a solid state image pickup device characterized by preparation ******.

[Claim 6]
A process of forming an opening in a position which opposes to an optoelectric transducer into which red light which transmits the aforementioned light filter of the aforementioned reflecting film enters,
A process of forming a reflecting layer in the aforementioned wiring layer side of the aforementioned opening via an insulator layer
A manufacturing method of the solid state image pickup device according to claim 5 characterized by preparation ******.

[Claim 7]
Between wiring of the aforementioned wiring layer, the aforementioned reflecting layer keeps the aforementioned wiring and an interval, and is formed.
A manufacturing method of the solid state image pickup device according to claim 6 characterized by things.

[Claim 8]
The aforementioned reflecting layer is formed via an insulator layer between the aforementioned element layer and the aforementioned wiring layer.
A manufacturing method of the solid state image pickup device according to claim 6 characterized by things.

[Claim 9]
In an image photographing apparatus which used a solid state image pickup device for an image sensor,
The aforementioned solid state image pickup device,
A plurality of unit pixels containing an active device which converts a signal charge by which photoelectric conversion was carried out to an electrical signal, and outputs it by an optoelectric transducer were arranged,
It has a wiring layer which wires the surface side of one of these to the aforementioned active device to an element layer in which the aforementioned optoelectric transducer is formed,
It is a solid state image pickup device which makes a light filter which formed incident light in the surface side of another side of the aforementioned element layer transmit and in which it enters the aforementioned optoelectric transducer,
It consists of a thing provided with a reflecting film formed so that the whole pixel surface containing a reading gate electrode which reads a signal charge in which photoelectric conversion of [of the aforementioned active devices] was carried out to the aforementioned wiring layer side of the aforementioned element layer via an insulator layer might be covered.
An image photographing apparatus characterized by things.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[Field of the Invention]
[0001]
While improving the efficiency which carries out photoelectric conversion of the light which entered, the present invention, With the side into which light enters, preventing the mixed colors by the reflected light reflected with the wiring provided to the opposite side relates to the image photographing apparatus using an easy solid state image pickup device, the manufacturing method of the solid state image pickup device, and its solid state image pickup device.
[Background of the Invention]
[0002]
A photo-diode is formed in the back surface side opposite to the surface in which an electrode, wiring, etc. are formed as a structure of a new image sensor, and the back surface exposure type image sensor which irradiates light and performs photoelectric conversion from a back surface is proposed. This structure can form a photo-diode all over a picture element region, and can make 100% the effective area product of a theory top light receiving surface.
[0003]
In order to protect the mixed colors in the upper layer from the light receiving surface of the optoelectric transducer 710 like the conventional image sensor as shown in Fig.18 when using a back surface exposure type image sensor as a single version color sensor, The micro lens 730 on chip is formed in the upper layer of the light filter 720 (for example, see Patent Document 1.). It can form near the light receiving surface of the optoelectric transducer 710, and this micro lens 730 on chip turns into a lens with a short focal distance, when there is neither an electrode nor a wiring layer. For this reason, the variation in the condensing state over change of the F value of the lens of apparatus and eye relief on which an image sensor is mounted can decrease, and can provide the stable image quality. In the back surface exposure type CMOS image sensor, the thickness of the optoelectric-transducer (for example, photo-diode) layer is usually 5 micrometers - about 7 micrometers.
[0004]
The ratio that light is absorbed in the region whose absorption index alpha of the silicon (Si) in a light range, depth by which the light which entered into silicon (Si) is absorbed 90%, and depth are 7 micrometers is shown in Table 1.
[0005]
[Table 1]

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波長λ [nm]	吸収係数α [cm^{-1}]	入射光が９０％吸収される深さ [μm]	７μmの領域での光吸収率
４００	１．２２Ｅ＋０５	０．１９	１
４５０	４．６３Ｅ＋０４	０．５０	１
５００	１．８５Ｅ＋０４	１．２５	１
５５０	６．３０Ｅ＋０３	３．６５	０．９９
６００	５．００Ｅ＋０３	４．６１	０．９７
６５０	３．２７Ｅ＋０３	７．０４	０．９０
７００	２．００Ｅ＋０３	１１．５１	０．７５

[0006]
Although the light which entered into silicon (Si) is absorbed about 100% on the wavelength of 400 nm - 550 nm, the 7-micrometer-deep photoelectric conversion region (photo-diode) shows that the component transmitted without being absorbed increases with the light of the long wave length beyond it, so that clearly from Table 1. That is, the component which transmits the optoelectric transducer 710R to the long wavelength side can exist, and the light L10 which entered into the optoelectric transducer 710 of the back surface exposure type CMOS image sensor can carry out photoelectric conversion of all the lights that entered into the optoelectric transducer 710, and cannot make it contribute to sensitivity, as shown in Fig.19.
[0007]
What is called mixed colors that the light L11 which transmitted the photoelectric conversion region 710R reaches the wiring layer 740, and the light L12 reflected with the wiring 741 enters into the optoelectric transducers 710G and 710B which are adjacent pixels, and generate photoelectric conversion occur, and it affects image quality.
[0008]
[Patent document 1] Japanese Published Patent Application No. 2003-31785 (JP2003-31785A)
[Description of the Invention]
[Problem to be solved by the invention]
[0009]
The problem which it is going to solve is a point which the component which transmits a photoelectric conversion region to the long wavelength side can exist, and the light which entered into the photoelectric conversion region of the back surface exposure type CMOS image sensor can make able to carry out photoelectric conversion of all the lights that entered into the photoelectric conversion region, and cannot be made to contribute to sensitivity. It is the point which what is called mixed colors occur and has on image quality of the light which transmitted these photoelectric conversion regions reaching a wiring layer, entering into the photoelectric conversion region whose light reflected with the wiring is an adjacent pixel, and generating photoelectric conversion.
[0010]
The present invention improves the efficiency which carries out photoelectric conversion of the light which entered into the photo-diode that the above-mentioned problem should be solved, and makes it problem further to prevent the mixed colors by reflection with the wiring on the surface side.
[Means for solving problem]
[0011]
The solid state image pickup device of the present invention is that by which a plurality of unit pixels containing the active device which converts the signal charge by which photoelectric

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conversion was carried out to an electrical signal, and outputs it by an optoelectric transducer were arranged, It has a wiring layer which wires the surface side of one of these to the aforementioned active device to the element layer in which the aforementioned optoelectric transducer is formed, In the solid state image pickup device which makes the light filter which formed incident light in the surface side of another side of the aforementioned element layer transmit and in which it enters the aforementioned optoelectric transducer, It had the reflecting film formed so that the whole pixel surface containing the reading gate electrode which reads the signal charge in which photoelectric conversion of [of the aforementioned active devices] was carried out to the aforementioned wiring layer side of the aforementioned element layer via the insulator layer might be covered.

[0012]

The present invention the manufacturing method of the solid state image pickup device of the present invention, It is that by which a plurality of unit pixels containing an active device which converts a signal charge by which photoelectric conversion was carried out to an electrical signal, and outputs it by an optoelectric transducer were arranged, It has a wiring layer which wires the surface side of one of these to the aforementioned active device to an element layer in which the aforementioned optoelectric transducer is formed, A manufacturing method of a solid state image pickup device which makes a light filter which formed incident light in the surface side of another side of the aforementioned element layer transmit and in which it enters the aforementioned optoelectric transducer is characterized by comprising:

A process of forming a reading electrode which reads a signal charge to a semiconductor layer in which the aforementioned element layer is formed.

A process of forming the aforementioned optoelectric transducer in the aforementioned semiconductor layer.

A process of forming a reflecting film so that the whole pixel surface which contains the aforementioned reading electrode in a side in which the aforementioned wiring layer of the aforementioned semiconductor layer is formed via an insulator layer may be covered.

[0013]

In the image photographing apparatus used for the image sensor, the image photographing apparatus of the present invention a solid state image pickup device the aforementioned solid state image pickup device, It is that by which a plurality of unit pixels containing the active device which converts the signal charge by which photoelectric conversion was carried out to an electrical signal, and outputs it by an optoelectric transducer were arranged, It has a wiring layer which wires the surface side of one of these to the aforementioned active device to the element layer in which the aforementioned optoelectric transducer is formed, Are a solid state image pickup device which makes the light filter which formed incident light in the surface side of another side of the aforementioned element layer transmit and in which it enters the aforementioned optoelectric transducer, and via an insulator layer to the aforementioned wiring layer side of the aforementioned element layer, It consists of a thing provided with the reflecting film formed so that the whole pixel surface containing the reading gate electrode which reads the signal charge in which photoelectric conversion of [of the aforementioned active devices] was carried out might be covered.

[Effect of the Invention]

[0014]

Since it had the reflecting film formed so that the whole pixel surface containing the reading gate electrode which reads the signal charge in which photoelectric conversion of [of the active devices] was carried out to the wiring layer side of an element layer via the insulator layer might be covered, the solid state image pickup device of the present invention is. Since

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the light (for example, red light) of the long wavelength transmitted in part without being completely absorbed by an optoelectric transducer can be returned to the optoelectric transducer which carries out photoelectric conversion of the light of long wavelength with a reflecting film, there is an advantage that the photoelectric conversion of the light which entered into the optoelectric transducer can be carried out efficiently. Since a reflecting film prevents the reflection by wiring of a wiring layer, it stops entering into the pixel which a reflected light adjoins, and there is an advantage that mixed colors can be prevented.

[0015]

Since it has the process of forming a reflecting film so that the whole pixel surface which contains a reading electrode in the side in which the wiring layer of a semiconductor layer is formed via an insulator layer may be covered, the manufacturing method of the solid state image pickup device of the present invention is. Since the light (for example, red light) of the long wavelength transmitted in part without being completely absorbed by an optoelectric transducer can be returned to the optoelectric transducer which carries out photoelectric conversion of the light of long wavelength with a reflecting film, there is an advantage of coming to be able to carry out the photoelectric conversion of the light which entered into the optoelectric transducer efficiently. Since a reflecting film prevents the reflection by wiring of a wiring layer, it stops entering into the pixel which a reflected light adjoins, and there is an advantage that mixed colors can be prevented.

[0016]

Since the solid state image pickup device of the present invention is mounted on the image sensor, and the image photographing apparatus of the present invention can carry out photoelectric conversion of the incident light efficiently and can prevent the mixed colors to the adjoining pixel, there is an advantage that improvement in sensitivity and improvement in image quality can be aimed at.

[Best Mode of Carrying Out the Invention]

[0017]

An example (the 1st example) of the embodiment concerning the solid state image pickup device of the present invention is described with the schematic structure cross sectional view of Fig.1.

[0018]

As shown in Fig.1, the solid state image pickup device 1 of the present invention, The optoelectric transducer (for example, photo-diode) 111 is formed in the element layer 110 which comprises a semiconductor layer, A plurality of unit pixels containing the active device (not shown) which converts the signal charge by which photoelectric conversion was carried out to an electrical signal, and outputs it by this optoelectric transducer 111 are arranged, It has the wiring layer 130 which wires the surface side of one of these to the above-mentioned active device to the element layer 110 in which the above-mentioned optoelectric transducer 111 is formed. The above-mentioned optoelectric transducer 111 is formed, for example by the 5 micrometers - 15 micrometers-thick silicon layer. The light filter 150 is formed in the surface side of another side of the element layer 110 in the incident light L. The reading gate electrode 121 which constitutes the read transistor which reads the signal charge in which photoelectric conversion of [of the above-mentioned active devices] was carried out is formed in the wiring layer 130 side of the above-mentioned element layer 110 via the insulator layer 122. This reading gate electrode 121 is formed, for example with polycrystalline silicon. For this reason, the reading gate electrode 121 has a light transmitting property.

[0019]

The reflecting film 140 is formed so that the whole pixel surface containing the above-mentioned reading gate electrode 121 may be covered via the insulator layer 141.

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[0020]
The above-mentioned reflecting film 140 is formed with aluminum, an aluminum oxide, etc., for example. In particular, the aluminum film can obtain the surface reflectance of about 90% or more to visible light. Therefore, it is preferable to adopt an aluminum film as the above-mentioned reflecting film 140. Although described behind, if it takes into consideration that the wavelength of light to reflect is green light and red light, it is also possible to use the silver which has 95% or more by the film in which the reflectance of green light and red light was formed by high vacuum vacuum deposition.
[0021]
Here, it describes by Fig.2 about the required film thickness at the time of using an aluminum film as the reflecting film 140. Fig.2 shows transmissivity to a left-vertical axis by making each film thickness of aluminum (Al) in a light range into a parameter, and shows reflectance to a right longitudinal axis, and the wavelength of incident light is shown on a horizontal axis.
[0022]
It will become mixed colors, if transmit the optoelectric transducer 111 and the aluminum film of the reflecting film 140 is transmitted further, it reflects with the upper wiring 131, the reflecting film 140 is transmitted from the surface side to the next pixel and it enters into the optoelectric transducer 111, as shown in Fig.2. Since the reflectance of aluminum (Al) is about 90% in a light range when light which the amount of mixed colors transmitted the optoelectric transducer 111, and arrived at the aluminum surface is made into 100%, It is 0.9% even when the transmissivity of 0.009% and an aluminum film is 10% in the case where the transmissivity of 0.00009% and an aluminum film is 1% in the case where the transmissivity of an aluminum film is 0.1%. If it takes into consideration that incident luminous intensity is about 10% to the optoelectric transducer 111 by the red (R) pixel when arriving at an aluminum surface, if transmissivity is stopped to about 1%, it is sufficient. Therefore, when an aluminum film is used for the reflecting film 140, there should just be 30 nm or more of the film thickness.
[0023]
The incident light L, as for, the above-mentioned solid state image pickup device 1 carries out light reception transmits the above-mentioned light filter 150, and goes into the optoelectric transducer 111. For example, when the above-mentioned light filter 150 is formed by 3 colors (for example, three primary colors of light) of blue (B) green (G) and red (R). The incident light L which transmits the light filter 150 and, as for, the above-mentioned optoelectric transducer 111 carries out light reception. Since the thickness of the above-mentioned optoelectric transducer 111 is formed in 7 micrometers - 15 micrometers, since wavelength of blue glow is short, it is absorbed about 100% by the incidence close-attendants side of the optoelectric transducer 111, and since photoelectric conversion is carried out, it cannot turn into the transmitted light which reaches the reflecting film 140. Although most is absorbed within the optoelectric transducer 111 as for green light, the part serves as a transmitted component. However, since it is reflected by the reflecting film 140 and is again returned to the optoelectric transducer 111, almost will be absorbed in the optoelectric transducer 111. On the other hand, in a part, red light transmits the optoelectric transducer 111. Therefore, the light volume of the red light by which photoelectric conversion is carried out by the optoelectric transducer 111 had become less than other colors. However, since the above-mentioned reflecting film 140 is provided, it is reflected by the reflecting film 140 and the red light which transmitted the optoelectric transducer 111 enters into the optoelectric transducer 111 again. For this reason, the amount of photoelectric conversion of red light becomes substantially equivalent to the amount of photoelectric conversion of other colors, and it can prevent deterioration of sensitivity.
[0024]

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The light which transmitted the optoelectric transducer 111 of each pixel since the above-mentioned reflecting film 140 was formed right above each pixel especially green light - red light, It is reflected by the reflecting film 140, and since the reflected light enters into the optoelectric transducer 111 transmitted as it is, there is almost no reflection to an adjacent pixel. For this reason, mixed colors are inhibited and good image quality can be obtained.

[0025]

Since the above-mentioned reflecting film 140 is formed so that the reading gate electrode 121 which consists of polycrystalline silicon may be covered, it is made to reflect with the reflecting film 140, and the light which transmitted the reading gate electrode 121 can also return it to the optoelectric transducer 111. Therefore, in the optoelectric transducer 111, it becomes possible to carry out photoelectric conversion of the incident light efficiently.

[0026]

Next, a detailed example of the CMOS sensor which can apply the solid state image pickup device of the above-mentioned composition is described with the schematic structure cross sectional view of Fig.3.

[0027]

As for back surface light reception type CMOS sensor 101, the picture element part and the peripheral circuit part are formed in the element layer 110 which consists of a silicon layer. It is formed in a thickness of 5 micrometers - 15 micrometers in the region which usually carries out light reception of the visible light to the above-mentioned element layer 110 using what ground the N^- type silicon substrate in desired thickness by chemical mechanical polishing. When carrying out light reception of the infrared light, and carrying out light reception of the ultraviolet radiation to a thickness of 15 micrometers - 50 micrometers, it is desirable to be formed in a thickness of 3 micrometers - 7 micrometers.

[0028]

The photosensor which consists of the N^- type layer used as the photoelectric conversion region 111 is formed in the picture element part of the above-mentioned element layer 110. This N^- type layer uses the above-mentioned N^- type silicon substrate. The N^+ layer 112 is formed in the upper part of the above-mentioned photoelectric conversion region 111, and the charge storage layer 113 which consists of P^+ layer for considering it as an embedding photo-diode is further formed in the upper part.

[0029]

The well area 115 of P type is formed in the picture element part of the above-mentioned photoelectric conversion region 111 so that the side periphery of the above-mentioned photoelectric conversion region 111 - the charge storage layer 113 may be surrounded. A part of this P type well area 115 is formed so that the element layer 110 may be penetrated, and that portion serves as the isolation region 116 between pixels. Furthermore, the P^+ layer 117 linked to the well area 115 (isolation region 116 between pixels) of the above-mentioned P type is formed in the lower part side of the above-mentioned element layer 110. This P^+ layer 117 side is a side into which light enters. And in order to secure a light-receiving region widely, the above-mentioned photoelectric conversion region 111 is formed so that the occupation area on the layout on the above-mentioned P^+ layer 117 side may become wide.

[0030]

It reads to the one side of the above-mentioned N^+ layer 112 and the charge storage layer 113, and the region 123 is formed in the P^- layer. On the above-mentioned reading region 123, it reads via the insulator layer 122, and the gate electrode 121 is formed. Furthermore, in the charge storage layer 113 of the above-mentioned reading gate electrode 121, it reads to an opposite side, the region 123 is adjoined, and the floating diffusion layer 125 which consists of N^+ layer is formed. Thus, the read transistor 120 is constituted.

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[0031]
The transistors 160 other than the above-mentioned read transistor 120 are formed in the well area 115 of the above-mentioned P type. As this transistor 160, there are a reset transistor, an amplification transistor, a vertical selection transistor, etc., for example, and it comprises an NMOS transistor.

[0032]
The reflecting film 140 is formed so that the whole pixel surface containing the above-mentioned reading gate electrode 121 may be covered via the insulator layer 141. This reflecting film 140 is formed with aluminum, an aluminum oxide, etc., for example. In particular, the aluminum film can obtain the surface reflectance of about 90% or more to visible light. Therefore, it is preferable to adopt an aluminum film as the above-mentioned reflecting film 140. Although described behind, if it takes into consideration that the wavelength of light to reflect is green light and red light, the surface reflectance of green light and red light is possible also for using the silver which has 95% or more.

[0033]
In the surface of one side of the above-mentioned element layer 110 (in Drawings, it is called the surface of an upper side, and the following surface), The insulator layer 132 which covers the above-mentioned read transistor 120, the transistor 160, etc. is formed, the wiring layer 130 which consists of the wiring 131 formed in two or more layers is formed into the insulator layer, and the support substrate 170 is provided further.

[0034]
The light-shielding film 182 is formed on the surface of the other side of the above-mentioned element layer 110 (in Drawings, it is called the surface on the lower part side, and a following back surface) via the transparent insulating film 181. This light-shielding film 182 is to prevent incident light from irradiating in addition to a picture element region, and the opening 183 is formed in the position which opposes to the region in which the optoelectric transducer 111 is formed so that light may enter into the optoelectric transducer 111. Furthermore, the light filter 150 is formed via the transparent insulating film 184. It consists of 3 colors of (B) and this light filter 150 is provided on trichromatic red (R) green (G) of light, and the blue optoelectric transducer 111 which carries out light reception of the predetermined color, respectively, for example. The light filter 150 is not limited to the three primary colors, but it can also provide [is] an emerald green light filter, an orange light filter, etc. like trichromatic neutral colors besides the three primary colors, for example. Furthermore, the micro lens 155 is formed on each light filter 150.

[0035]
Next, an example (the 2nd example) of the embodiment concerning the solid state image pickup device of the present invention is described with the schematic structure cross sectional view of Fig.4.

[0036]
As shown in Fig.4, the solid state image pickup device 2 of the present invention, The optoelectric transducer (for example, photo-diode) 111 is formed in the element layer 110 which comprises a semiconductor layer, A plurality of unit pixels containing the active device (not shown) which converts the signal charge by which photoelectric conversion was carried out to an electrical signal, and outputs it by this optoelectric transducer 111 are arranged, It has the wiring layer 130 which wires the surface side of one of these to the above-mentioned active device to the element layer 110 in which the above-mentioned optoelectric transducer 111 is formed. The above-mentioned optoelectric transducer 111 is formed, for example by the 5 micrometers - 15 micrometers-thick silicon layer. The light filter 150 is formed in the surface side of another side of the element layer 110 in the incident light L. The reading gate electrode

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121 which constitutes the read transistor 120 which reads the signal charge in which photoelectric conversion of [of the above-mentioned active devices] was carried out is formed in the wiring layer 130 side of the above-mentioned element layer 110 via the insulator layer 122. This reading gate electrode 121 is formed, for example with polycrystalline silicon. For this reason, the reading gate electrode 121 has a light transmitting property.

[0037]

The reflecting film 140 is formed in the whole surface of a pixel containing the above-mentioned reading gate electrode 121 so that it may cover via the insulator layer 141. However, the opening 142 is formed in the above-mentioned reflecting film 140 of the position which opposes to the optoelectric transducer 111 into which the red light which transmits the light filter 150 enters although the reflecting film 140 is formed in the whole surface of the green (Green) pixel and the blue (Blue) pixel. The reflecting layer 143 is formed in the above-mentioned wiring layer 130 side of the above-mentioned opening 142. This reflecting layer 143 is formed so that it may oppose to the opening 142 and the opening 142 top may be covered. [the interval which can secure the wiring 131 and insulation, for example, the interval which is about 0.2 micrometer,], when the wiring 131 is formed in the position which opposes to the opening 142, it is formed. Therefore, between the wiring 131 of the above-mentioned wiring layer 130, the above-mentioned reflecting layer 143 keeps the above-mentioned wiring 131 and an interval, and is formed.

[0038]

An aluminum (Al) film and an aluminum oxide film can be used for the above-mentioned reflecting film 140 and the reflecting layer 143. The aluminum film can obtain the surface reflectance of about 90% or more to visible light especially. Therefore, it is preferable to adopt an aluminum film as the above-mentioned reflecting film 140 and the reflecting layer 143. On the other hand, as for the above-mentioned wiring 131 made to reflect red light and the reflecting layer 143, since the copper film can obtain the surface reflectance of about 96% or more to red light, forming with copper is also preferable.

[0039]

Thus, it is only that the composition of the above-mentioned reflecting film 140 of a red (Red) picture element part differs in the solid state image pickup device 2, and other composition is the same as that of the aforementioned solid state image pickup device 1.

[0040]

The incident light L, as for, the above-mentioned solid state image pickup device 2 carries out light reception transmits the above-mentioned light filter 150, and goes into the optoelectric transducer 111. For example, when the above-mentioned light filter 150 is formed by 3 colors (for example, three primary colors of light) of blue (B) green (G) and red (R). The incident light l. which transmits the light filter 150 and, as for, the above-mentioned optoelectric transducer 111 carries out light reception. Since the thickness of the above-mentioned optoelectric transducer 111 is formed in 7 micrometers - 15 micrometers, since the blue glow LB which transmitted the blue filter has short wavelength, it is absorbed about 100% by the incidence close-attendants side of the optoelectric transducer 111, and since photoelectric conversion is carried out, it cannot turn into the transmitted light which reaches the reflecting film 140. Although most is absorbed within the optoelectric transducer 111 as for the green light LG which transmitted the green filter, the part serves as a transmitted component. However, since it is reflected by the reflecting film 140 and is again returned to the optoelectric transducer 111, almost will be absorbed in the optoelectric transducer 111. On the other hand, in a part, red light LR which transmitted the red filter transmits the optoelectric transducer 111. Therefore, the light volume of red light LR by which photoelectric conversion is carried out by the optoelectric transducer 111 had become less than other colors. However, since the above-

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mentioned reflecting layer 143 is provided, it is reflected by the reflecting layer 143 and red light LR which transmitted the optoelectric transducer 111 enters into the optoelectric transducer 111 again. For this reason, the amount of photoelectric conversion of red light LR becomes substantially equivalent to the amount of photoelectric conversion of other colors, and it can prevent deterioration of sensitivity.

[0041]

The component of an incident light is light with long wavelength to which most transmits the optoelectric transducer 111 to a red (Red) pixel. On the other hand, the wavelength of an incident light is 30% or less of only light intensity in 600 nm with a peak of 500 nm - 550 nm, and a green (Green) pixel has few components which transmit the optoelectric transducer 111. As the blue (Blue) pixel was described previously, there is no component of the light which transmits the 7-micrometer optoelectric transducer 111. That is, the degree of incidence which the light reflected with the reflecting film 140 enters into the optoelectric transducer 111 which is an adjacent pixel, and starts mixed colors, The component of the light which entered into the red (Red) pixel overwhelmingly may be kept from entering into the photo-diode which is a pixel of green (Green) and blue (Blue) largely. [reflected light / in the reflecting film 140 of the light which entered into the red (Red) pixel] Even if the light which entered into the reflective surface of the reflecting layer 143 aslant reflects in an adjacent pixel at an incident angle [like], in the above-mentioned solid state image pickup device 2 the reflected light, Since it is reflected with the reflecting film 140 formed on green (Green) and a blue (Blue) pixel and escapes to the wiring layer 130 side, The mixed colors of the light of a component with long wavelength which has transmitted the red (Red) pixel in a green (Green) and blue (Blue) pixel can be prevented, and good image quality can be obtained.

[0042]

That it may be what reflects a red light, by a case, the above-mentioned reflecting layer 143 has the advantage that it can form at the same process as the wiring 131, when the wiring 131 of the wiring layer 130 is formed with the metal used for the wiring material of the usual semiconductor device, such as aluminum and copper. Since it becomes unnecessary to newly provide by this the process of producing the reflecting layer 143, the reflecting layer 143 can be formed without covering a process load.

[0043]

Next, an example (the 3rd example) of the embodiment concerning the solid state image pickup device of the present invention is described with the schematic structure cross sectional view of Fig.5.

[0044]

As shown in Fig.5, the solid state image pickup device 3 of the present invention, The optoelectric transducer (for example, photo-diode) 111 is formed in the element layer 110 which comprises a semiconductor layer, A plurality of unit pixels containing the active device (not shown) which converts the signal charge by which photoelectric conversion was carried out to an electrical signal, and outputs it by this optoelectric transducer 111 are arranged, It has the wiring layer 130 which wires the surface side of one of these to the above-mentioned active device to the element layer 110 in which the above-mentioned optoelectric transducer 111 is formed. The above-mentioned optoelectric transducer 111 is formed, for example by the 5 micrometers - 15 micrometers-thick silicon layer. The light filter 150 is formed in the surface side of another side of the element layer 110 in the incident light L. The reading gate electrode 121 which constitutes the read transistor 120 which reads the signal charge in which photoelectric conversion of [of the above-mentioned active devices] was carried out is formed in the wiring layer 130 side of the above-mentioned element layer 110 via the insulator layer 122. This reading gate electrode 121 is formed, for example with polycrystalline silicon. For

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this reason, the reading gate electrode 121 has a light transmitting property.

[0045]

The reflecting film 140 is formed in the whole surface of a pixel containing the above-mentioned reading gate electrode 121 so that it may cover via the insulator layer 141. However, the opening 142 is formed in the above-mentioned reflecting film 140 of the position which opposes to the optoelectric transducer 111 into which the red light which transmits the light filter 150 enters although the reflecting film 140 is formed in the whole surface of the green (Green) pixel and the blue (Blue) pixel. The reflecting layer 143 is formed in the above-mentioned wiring layer 130 side of the above-mentioned opening 142. This reflecting layer 143 is formed so that it may oppose to the opening 142 and the opening 142 top may be covered. The above-mentioned reflecting layer 143 is formed via the insulator layer 144 between the above-mentioned element layer 110 and the above-mentioned wiring layer 130.

[0046]

An aluminum (Al) film and an aluminum oxide film can be used for the above-mentioned reflecting film 140 and the reflecting layer 143. The aluminum film can obtain the surface reflectance of about 90% or more to visible light especially. Therefore, it is preferable to adopt an aluminum film as the above-mentioned reflecting film 140 and the reflecting layer 143. On the other hand, as for the above-mentioned wiring 131 made to reflect red light and the reflecting layer 143, since the copper film can obtain the surface reflectance of about 96% or more to red light, forming with copper is also preferable.

[0047]

Thus, it is only that the composition of the above-mentioned reflecting film 140 of a red (Red) picture element part differs in the solid state image pickup device 3, and other composition is the same as that of the aforementioned solid state image pickup device 1.

[0048]

The incident light L, as for, the above-mentioned solid state image pickup device 3 carries out light reception transmits the above-mentioned light filter 150, and goes into the optoelectric transducer 111. For example, when the above-mentioned light filter 150 is formed by 3 colors (for example, three primary colors of light) of blue (B) green (G) and red (R). The incident light L which transmits the light filter 150 and, as for, the above-mentioned optoelectric transducer 111 carries out light reception. Since the thickness of the above-mentioned optoelectric transducer 111 is formed in 5 micrometers - 15 micrometers, since the blue glow LB which transmitted the blue filter has short wavelength, it is absorbed about 100% by the incidence close-attendants side of the optoelectric transducer 111, and since photoelectric conversion is carried out, it cannot turn into the transmitted light which reaches the reflecting film 140. Although most is absorbed within the optoelectric transducer 111 as for the green light LG which transmitted the green filter, the part serves as a transmitted component. However, since it is reflected by the reflecting film 140 and is again returned to the optoelectric transducer 111, almost will be absorbed in the optoelectric transducer 111. On the other hand, in a part, red light LR transmits the optoelectric transducer 111. Therefore, the light volume of red light LR by which photoelectric conversion is carried out by the optoelectric transducer 111 had become less than other colors. However, since the above-mentioned reflecting layer 143 is provided, it is reflected by the reflecting layer 143 and red light LR which transmitted the optoelectric transducer 111 enters into the optoelectric transducer 111 again. For this reason, the amount of photoelectric conversion of red light LR becomes substantially equivalent to the amount of photoelectric conversion of other colors, and it can prevent deterioration of sensitivity.

[0049]

Even if the light which entered into the reflective surface of the reflecting layer 143 aslant

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reflects in an adjacent pixel at an incident angle [like], in the above-mentioned solid state image pickup device 3 the reflected light, Since it is reflected with the reflecting film 140 formed on green (Green) and a blue (Blue) pixel and escapes to the wiring layer 130 side, The mixed colors of the light of a component with long wavelength which has transmitted the red (Red) pixel in a green (Green) and blue (Blue) pixel can be prevented, and good image quality can be obtained.

[0050]

Next, an example (the 1st example) of the embodiment concerning the manufacturing method of the solid state image pickup device of the present invention is described with Fig.6 - the manufacturing process cross sectional view of Fig.10.

[0051]

A substrate is prepared although a graphic display is not carried out. This substrate consisted of the 1st conductivity-type (N type) silicon substrate, and what has the sheet resistance of 10 ohm-cm - 50 ohm-cm degree was used for it. Next, a P^- type silicon layer is formed as the P^- type semiconductor layer 211 on the above-mentioned substrate with an epitaxial grown method, for example.

[0052]

Next, the channel stopping area which consists of P^+ type region is formed in the predetermined position of the semiconductor layer 211 above-mentioned surface. This channel stopping area can be formed by an ion implantation. Next, the above-mentioned channel stopping area is adjoined in the predetermined position of the semiconductor layer 211 above-mentioned surface, and the well area which consists of P type region is formed in the region in which a vertical charge transfer section is formed. The predetermined position of the semiconductor layer 211 above-mentioned surface is adjoined in the above-mentioned channel stopping area, and N type region of a vertical charge transfer section is formed in the above-mentioned well area upper layer.

[0053]

Next, as shown in Fig.6 (1), on the region used as the vertical charge transfer section top on the above-mentioned semiconductor layer 211, and a read section, it reads via the insulator layer 122 and forms the gate electrode (a transfer electrode is also included) 121. This reading gate electrode 121 may be formed so that it may overlap on a channel stopping area. The above-mentioned electrode formation forms a polysilicon film as an electrode formation film, for example, after forming the insulator layer 122 in the semiconductor layer 211 surface. Then, a polysilicon film is read with the etching technology using the usual resist mask, and it can pattern after the gate electrode 121 and can form.

[0054]

Next, as shown in Fig.6 (2), the read section in which the above-mentioned reading gate electrode 121 of the semiconductor layer 211 above-mentioned surface was formed is adjoined, and N type region of the optoelectric transducer 111 is formed. N type region of this optoelectric transducer 111 can be formed by an ion implantation. Subsequently, the hole storage layer which consists of P^+ type region is formed in N type region surface of the above-mentioned optoelectric transducer 111. This hole storage layer can be formed by an ion implantation.

[0055]

Next, after forming the insulator layer 141 so that the above-mentioned reading gate electrode 121 may be covered on the whole surface as shown in Fig.7 (3), the reflecting film 140 is formed in the whole surface. By a CVD method, the above-mentioned insulator layer 141 deposits silicon oxide on a thickness of several 10 nm, and is formed, for example. The above-mentioned reflecting film 140 deposits aluminum, an aluminum oxide, etc. by CVD method,

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sputtering process, etc., for example, and is formed. Then, after forming the resist mask which covers a picture element region with the usual resist application technology, a lithography technology, etc., the reflecting film 140 of regions other than a mask is removed. Then, the above-mentioned resist mask is removed.

[0056]

As for the above-mentioned reflecting film 140, it is preferable to form with the aluminum film which can obtain the surface reflectance of about 90% or more to visible light especially. As described by the aforementioned Fig.2, when an aluminum film is used for the reflecting film 140, 30 nm or more of the film thickness should just exist. If it takes into consideration that the wavelength of light to reflect is green light and red light, the surface reflectance of green light and red light is possible also for using the silver which has 95% or more.

[0057]

Next, although a graphic display is not carried out, after forming the element of the peripheral circuit area of a solid state image pickup device by the usual CMOS-LSI process, as shown in Fig.8 (4), by the formation technology of the usual multilevel interconnection, the wiring 131 of two or more layers is formed on the element layer 110, and the wiring layer 130 is accomplished. A support substrate may be formed in the wiring layer 130 side although a graphic display is not carried out.

[0058]

Next, the substrate (not shown) side is removed and flattened by polish, and as shown in Fig.9 (5), a back surface is ground to about 111 optoelectric transducer. It leaves 3.5 micrometers - about 7 micrometers of semiconductor layers 211 to the optoelectric-transducer 111 side, for example.

[0059]

Finally, as shown in Fig.10 (6), the light filter 150 is formed in the back surface side, and a graphic display is not carried out further, but the solid state image pickup device 1 described by the aforementioned Fig.1 etc. is completed by forming a lens on chip etc. by the same method as the usual surface type image sensor.

[0060]

Since it has the process of forming the reflecting film 140 so that the whole pixel surface which reads to the side in which the wiring layer 130 of the semiconductor layer 211 is formed via the insulator layer 141, and contains the gate electrode 121 may be covered, the manufacturing method of the above-mentioned solid state image pickup device is. Since the light (for example, red light) of the long wavelength transmitted in part without being completely absorbed by the optoelectric transducer 111 can be returned to the optoelectric transducer 111 which carries out photoelectric conversion of the light of long wavelength with the reflecting film 140, There is an advantage of coming to be able to carry out the photoelectric conversion of the light which entered into the optoelectric transducer 111 efficiently. Since the reflecting film 140 prevents the reflection by the wiring 131 of the wiring layer 130, it stops entering into the pixel which a reflected light adjoins, and there is an advantage that mixed colors can be prevented.

[0061]

Next, an example (the 2nd example) of the embodiment concerning the manufacturing method of the solid state image pickup device of the present invention is described with Fig.11 - the manufacturing process cross sectional view of Fig.15.

[0062]

A substrate is prepared although a graphic display is not carried out. This substrate consisted of the 1st conductivity-type (N type) silicon substrate, and what has the sheet resistance of 10 ohm-cm - 50 ohm-cm degree was used for it. Next, a P $^{-}$ type silicon layer is formed as the P $^{-}$

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type semiconductor layer 211 on the above-mentioned substrate with an epitaxial grown method, for example.

[0063]

Next, the channel stopping area which consists of P^+ type region is formed in the predetermined position of the semiconductor layer 211 above-mentioned surface. This channel stopping area can be formed by an ion implantation. Next, the above-mentioned channel stopping area is adjoined in the predetermined position of the semiconductor layer 211 above-mentioned surface, and the well area which consists of P type region is formed in the region in which a vertical charge transfer section is formed. The predetermined position of the semiconductor layer 211 above-mentioned surface is adjoined in the above-mentioned channel stopping area, and N type region of a vertical charge transfer section is formed in the above-mentioned well area upper layer.

[0064]

Next, as shown in Fig.11 (1), on the region used as the vertical charge transfer section top on the above-mentioned semiconductor layer 211, and a read section, it reads via the insulator layer 122 and forms the gate electrode (a transfer electrode is also included) 121. This reading gate electrode 121 may be formed so that it may overlap on a channel stopping area. The above-mentioned electrode formation forms a polysilicon film as an electrode formation film, for example, after forming the insulator layer 122 in the semiconductor layer 211 surface. Then, a polysilicon film is read with the etching technology using the usual resist mask, and it can pattern after the gate electrode 121 and can form.

[0065]

Next, as shown in Fig.11 (2), the read section in which the above-mentioned reading gate electrode 121 of the semiconductor layer 211 above-mentioned surface was formed is adjoined, and N type region of the optoelectric transducer 111 is formed. N type region of this optoelectric transducer 111 can be formed by an ion implantation. Subsequently, the hole storage layer which consists of P^+ type region is formed in N type region surface of the above-mentioned optoelectric transducer 111. This hole storage layer can be formed by an ion implantation.

[0066]

Next, after forming the insulator layer 141 so that the above-mentioned reading gate electrode 121 may be covered on the whole surface as shown in Fig.12 (3), the reflecting film 140 is formed in the whole surface. By a CVD method, the above-mentioned insulator layer 141 deposits silicon oxide on a thickness of several 10 nm, and is formed, for example. The above-mentioned reflecting film 140 deposits aluminum, an aluminum oxide, etc. by CVD method, sputtering process, etc., for example, and is formed.

[0067]

As for the above-mentioned reflecting film 140, it is preferable to form with the aluminum film which can obtain the surface reflectance of about 90% or more to visible light especially. As described by the aforementioned Fig.2, when an aluminum film is used for the reflecting film 140, 30 nm or more of the film thickness should just exist. If it takes into consideration that the wavelength of light to reflect is green light and red light, the surface reflectance of green light and red light is possible also for using the silver which has 95% or more.

[0068]

Then, as shown in Fig.12 (4), after forming the resist mask which covers with the usual resist application technology, a lithography technology, etc. the blue picture element region where wavelength is short, and a green picture element region, the reflecting film 140 of regions other than a mask is removed. Therefore, the reflecting film 140 of a red picture element region is removed, and while the opening 142 is formed, although the graphic display is not

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carried out, the reflecting film 140 of a peripheral circuit area is also removed. Then, the above-mentioned resist mask is removed.

[0069]

Next, although a graphic display is not carried out, after forming the element of the peripheral circuit area of a solid state image pickup device by the usual CMOS-LSI process, as shown in Fig.13 (5), by the formation technology of the usual multilevel interconnection, the wiring 131 of two or more layers is formed on the element layer 110, and the wiring layer 130 is accomplished. When forming the wiring 131 of the bottom of the heap, for example in that case, the reflecting layer 143 is formed on the above-mentioned red picture element region. This reflecting layer 143 is formed so that it may oppose to the opening 142 and the opening 142 top may be covered. When the wiring 131 is formed in the position which opposes to the opening 142, the wiring 131 and insulation can be secured and it is formed [the interval, for example, the interval which are 0.4 micrometer - about 0.2 micrometer, that red light does not leak between the wiring 131 and the light shielding layers 143]. Therefore, between the wiring 131 of the above-mentioned wiring layer 130, the above-mentioned reflecting layer 143 keeps the above-mentioned wiring 131 and an interval, and is formed.

[0070]

An aluminum (Al) film and an aluminum oxide film can be used for the above-mentioned reflecting film 140 and the reflecting layer 143. The aluminum film can obtain the surface reflectance of about 90% or more to visible light especially. Therefore, it is preferable to adopt an aluminum film as the above-mentioned reflecting film 140 and the reflecting layer 143. On the other hand, as for the above-mentioned wiring 131 made to reflect red light and the reflecting layer 143, since the copper film can obtain the surface reflectance of about 96% or more to red light, forming with copper is also preferable. Thus, if the above-mentioned reflecting layer 143 will be formed with copper if the wiring 131 is formed with copper, and formed with aluminum, it will become possible by forming with aluminum to form in the same process as the wiring 131. A support substrate may be formed in the wiring layer 130 side although a graphic display is not carried out.

[0071]

Next, the substrate (not shown) side is removed and flattened by polish, and as shown in Fig.14 (6), a back surface is ground to about 111 optoelectric transducer. It leaves 3.5 micrometers - about 7 micrometers of semiconductor layers 211 to the optoelectric-transducer 111 side, for example.

[0072]

Finally, as shown in Fig.15 (7), the light filter 150 is formed in the back surface side, and a graphic display is not carried out further, but the solid state image pickup device 2 described by the aforementioned Fig.1 etc. is completed by forming a lens on chip etc. by the same method as the usual surface type image sensor.

[0073]

In the manufacturing method of the above-mentioned solid state image pickup device 2, since wavelength of blue glow is short, it is absorbed about 100% by the incidence close-attendants side of the optoelectric transducer 111, and since photoelectric conversion is carried out, it cannot turn into the transmitted light which reaches the reflecting film 140. Although most is absorbed within the optoelectric transducer 111 as for green light, the part serves as a transmitted component. However, since it is reflected by the reflecting film 140 and is again returned to the optoelectric transducer 111, almost will be absorbed in the optoelectric transducer 111. On the other hand, in a part, red light transmits the optoelectric transducer 111. Therefore, although the light volume of the red light by which photoelectric conversion is carried out by the optoelectric transducer 111 becomes less than other colors, since the above-

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mentioned reflecting layer 143 is provided, it is reflected by the reflecting layer 143 and the red light which transmitted the optoelectric transducer 111 enters into the optoelectric transducer 111 again. For this reason, the amount of photoelectric conversion of red light becomes substantially equivalent to the amount of photoelectric conversion of other colors, and it can prevent deterioration of sensitivity.

[0074]

Even if the light which entered into the reflective surface of the reflecting layer 143 aslant reflects in an adjacent pixel at an incident angle [like], the reflected light, Since it is reflected with the reflecting film 140 formed on green (Green) and a blue (Blue) pixel and escapes to the wiring layer 130 side, The mixed colors of the light of a component with long wavelength which has transmitted the red (Red) pixel in a green (Green) and blue (Blue) pixel can be prevented, and good image quality can be obtained.

[0075]

That it may be what reflects a red light, by a case, the above-mentioned reflecting layer 143 has the advantage that it can form at the same process as the wiring 131, when the wiring 131 of the wiring layer 130 is formed with the metal used for the wiring material of the usual semiconductor device, such as aluminum and copper. Since it becomes unnecessary to newly provide by this the process of producing the reflecting layer 143, the reflecting layer 143 can be formed without covering a process load.

[0076]

Although the case where the reflecting layer 143 was provided between the wiring 131 was described in the above-mentioned manufacturing method, the wiring 131 of the above-mentioned reflecting layer 143 is possible also for forming by a different layer as the 3rd example of an embodiment. In this case, it becomes composition like the aforementioned Fig.5. That is, the same with having described by the aforementioned Fig.12, the reflecting film 140 is formed in the whole surface of a pixel containing the above-mentioned reading gate electrode 121 so that it may cover via the insulator layer 141. However, the whole surface of a green (Green) pixel and a blue (Blue) pixel forms the reflecting film 140, and forms the opening 142 in the above-mentioned reflecting film 140 of the position which opposes to the optoelectric transducer 111 into which red light enters.

[0077]

Next, as shown in Fig.16, the insulator layer 144 which reads to the element layer 110 side and covers the gate electrode 121, the reflecting film 140, etc. is formed. Then, after forming the reflecting layer 143 on the insulator layer 144, patterning which leaves the reflecting layer 143 so that it may oppose to the opening 142 and the opening 142 top may be covered with the formation technology of the usual etching mask and etching technology (for example, anisotropic dry etching) is performed. For example, the reflecting layer 143 may be the same as the aperture shape of the optoelectric transducer 111 except the reading gate electrode 121 of the red (Red) pixel, etc. Then, an etching mask is removed.

[0078]

An aluminum (Al) film and an aluminum oxide film can be used for the above-mentioned reflecting film 140 and the reflecting layer 143. The aluminum film can obtain the surface reflectance of about 90% or more to visible light especially. Therefore, it is preferable to adopt an aluminum film as the above-mentioned reflecting film 140 and the reflecting layer 143. On the other hand, as for the above-mentioned reflecting layer 143 in which red light is reflected, since the copper film can obtain the surface reflectance of about 96% or more to red light, forming with copper is also preferable.

[0079]

After that, by the formation technology of the usual multilevel interconnection, the wiring 131

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of two or more layers is formed on the element layer 110, and the wiring layer 130 is accomplished.

[0080]

Next, the substrate (not shown) side is removed and flattened by polish, and a back surface is ground to about 111 optoelectric transducer. It leaves 3.5 micrometers - about 7 micrometers of semiconductor layers 211 to the optoelectric-transducer 111 side, for example.

[0081]

Although the light filter 150 is formed in the back surface side and a graphic display finally is not carried out further, the solid state image pickup device 3 described by the aforementioned Fig.5 is completed by forming a lens on chip etc. by the same method as the usual surface type image sensor.

[0082]

In the manufacturing method of the above-mentioned solid state image pickup device 3, since wavelength of blue glow is short, it is absorbed about 100% by the incidence close-attendants side of the optoelectric transducer 111, and since photoelectric conversion is carried out, it cannot turn into the transmitted light which reaches the reflecting film 140. Although most is absorbed within the optoelectric transducer 111 as for green light, the part serves as a transmitted component. However, since it is reflected by the reflecting film 140 and is again returned to the optoelectric transducer 111, almost will be absorbed in the optoelectric transducer 111. On the other hand, in a part, red light transmits the optoelectric transducer 111. Therefore, although the light volume of the red light by which photoelectric conversion is carried out by the optoelectric transducer 111 becomes less than other colors, since the above-mentioned reflecting layer 143 is provided, it is reflected by the reflecting layer 143 and the red light which transmitted the optoelectric transducer 111 enters into the optoelectric transducer 111 again. For this reason, the amount of photoelectric conversion of red light becomes substantially equivalent to the amount of photoelectric conversion of other colors, and it can prevent deterioration of sensitivity.

[0083]

Even if the light which entered into the reflective surface of the reflecting layer 143 aslant reflects in an adjacent pixel at an incident angle [like], the reflected light, Since it is reflected with the reflecting film 140 formed on green (Green) and a blue (Blue) pixel and escapes to the wiring layer 130 side, The mixed colors of the light of a component with long wavelength which has transmitted the red (Red) pixel in a green (Green) and blue (Blue) pixel can be prevented, and good image quality can be obtained.

[0084]

Next, one working example concerning the image photographing apparatus of the present invention is described with the block diagram of Fig.17.

[0085]

As shown in Fig.17, the image photographing apparatus 500 is provided with the solid state image pickup device 510. The condensing side of this solid state image pickup device 510 is equipped with the image formation optical system 520 which makes an image image, and the drive circuit 530 which drives it is connected to the solid state image pickup device 510. And the digital disposal circuit 540 which processes in an image the signal by which photoelectric conversion was carried out with the solid state image pickup device 510 is connected. The picture signal processed by the above-mentioned digital disposal circuit 540 is memorized by the image storage section 550. In such an image photographing apparatus 500, either of the solid state image pickup devices 1, 2, and 3 described by the 1st example of the aforementioned embodiment, the 2nd example, and the 3rd example can be used for the above-mentioned solid state image pickup device 510.

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[0086]
There is an advantage that the image excellent in color reproducibility can be acquired since the solid state image pickup device 1, the solid state image pickup device 2, or the solid state image pickup device 3 of the present invention is used for the image sensor and the image photographing apparatus 500 of the present invention does not have mixed colors, and an image [high sensitivity moreover] can be acquired.
[0087]
The image photographing apparatus 500 of the present invention is not limited to the above-mentioned composition, and if it is an image photographing apparatus using a solid state image pickup device, it is applicable to the thing of any composition.
[Brief Description of the Drawings]
[0088]
[Drawing 1]It is a schematic structure cross sectional view showing the example of 1 embodiment concerning the solid state image pickup device of the present invention (the 1st example).
[Drawing 2]It is a related figure of the transmissivity and reflectance which made film thickness of the reflecting film the parameter, and the wavelength of incident light.
[Drawing 3]It is a schematic structure cross sectional view showing the example of 1 embodiment concerning the CMOS sensor with which the solid state image pickup device of the present invention is applied.
[Drawing 4]It is a schematic structure cross sectional view showing the example of 1 embodiment concerning the solid state image pickup device of the present invention (the 2nd example).
[Drawing 5]It is a schematic structure cross sectional view showing the example of 1 embodiment concerning the solid state image pickup device of the present invention (the 3rd example).
[Drawing 6]It is a manufacturing process cross sectional view showing the example of 1 embodiment concerning the manufacturing method of the solid state image pickup device of the present invention (the 1st example).
[Drawing 7]It is a manufacturing process cross sectional view showing the example of 1 embodiment concerning the manufacturing method of the solid state image pickup device of the present invention (the 1st example).
[Drawing 8]It is a manufacturing process cross sectional view showing the example of 1 embodiment concerning the manufacturing method of the solid state image pickup device of the present invention (the 1st example).
[Drawing 9]It is a manufacturing process cross sectional view showing the example of 1 embodiment concerning the manufacturing method of the solid state image pickup device of the present invention (the 1st example).
[Drawing 10]It is a manufacturing process cross sectional view showing the example of 1 embodiment concerning the manufacturing method of the solid state image pickup device of the present invention (the 1st example).
[Drawing 11]It is a manufacturing process cross sectional view showing the example of 1 embodiment concerning the manufacturing method of the solid state image pickup device of the present invention (the 2nd example).
[Drawing 12]It is a manufacturing process cross sectional view showing the example of 1 embodiment concerning the manufacturing method of the solid state image pickup device of the present invention (the 2nd example).
[Drawing 13]It is a manufacturing process cross sectional view showing the example of 1 embodiment concerning the manufacturing method of the solid state image pickup device of

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the present invention (the 2nd example).

[Drawing 14]It is a manufacturing process cross sectional view showing the example of 1 embodiment concerning the manufacturing method of the solid state image pickup device of the present invention (the 2nd example).

[Drawing 15]It is a manufacturing process cross sectional view showing the example of 1 embodiment concerning the manufacturing method of the solid state image pickup device of the present invention (the 2nd example).

[Drawing 16]It is a manufacturing process cross sectional view showing the example of 1 embodiment concerning the manufacturing method of the solid state image pickup device of the present invention (the 3rd example).

[Drawing 17]It is a block diagram showing the example of 1 embodiment concerning an image photographing apparatus.

[Drawing 18]It is a schematic structure perspective view showing an example concerning the conventional solid state image pickup device.

[Drawing 19]It is a schematic structure cross sectional view showing the problem concerning the conventional solid state image pickup device.

[Explanations of letters or numerals]

[0089]

1 -- solid state image pickup device, 110 -- element layer, 111 -- optoelectric transducer, 121 -- reading gate electrode, 130 -- wiring layer, 131 -- wiring, 140 -- reflecting film, 141 -- insulator layer

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DRAWINGS

*** NOTICES ***

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1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DRAWINGS

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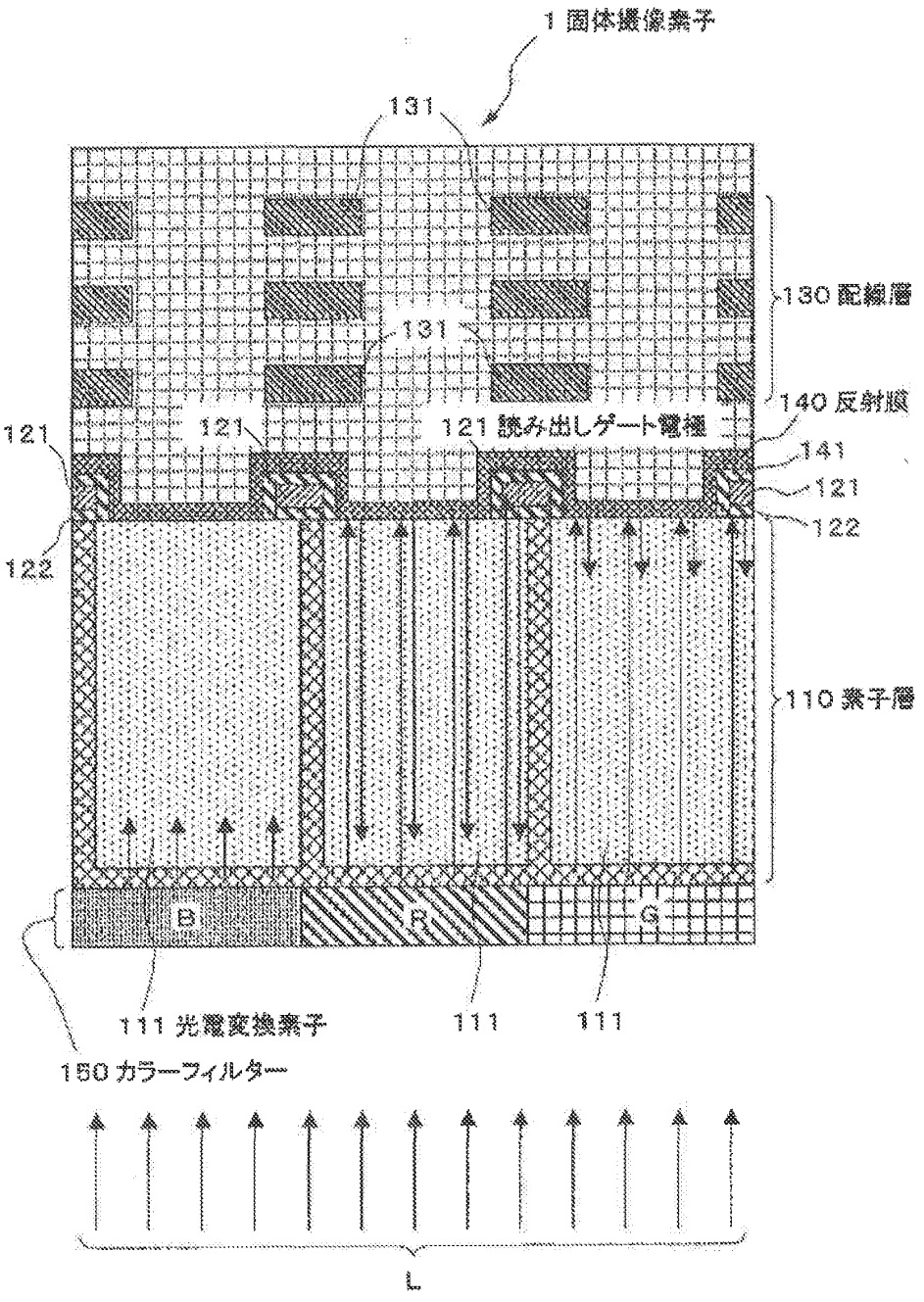
[Drawing 1]



[Drawing 2]

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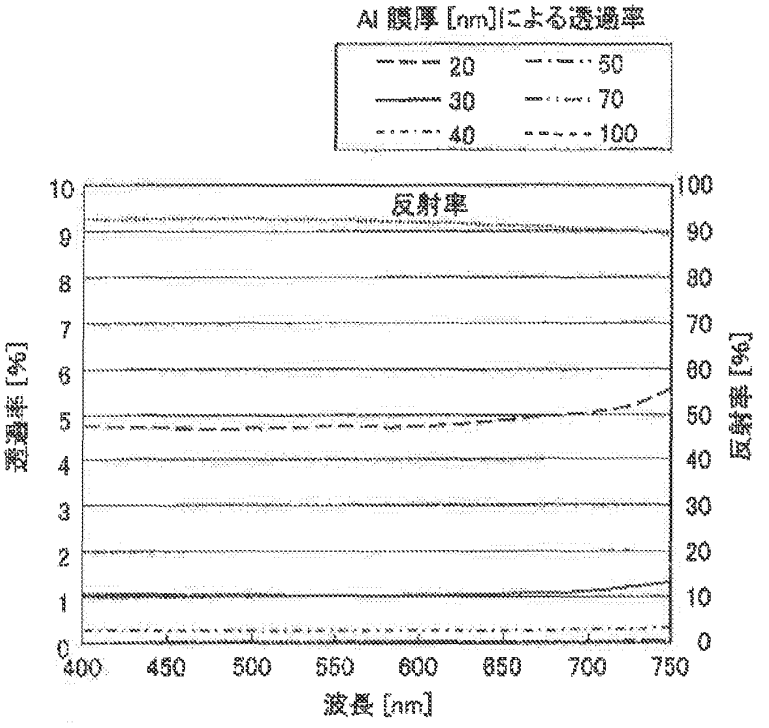

[Drawing 3]

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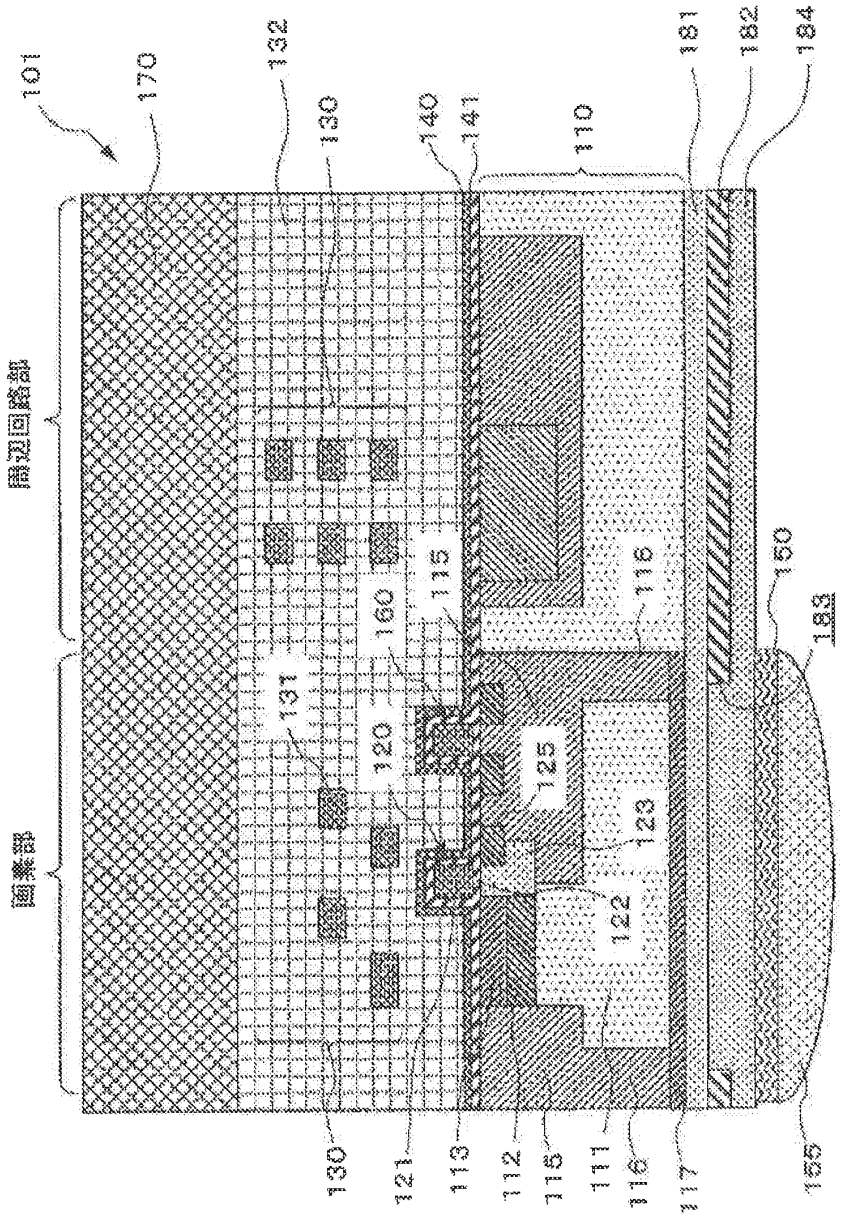

[Drawing 4]

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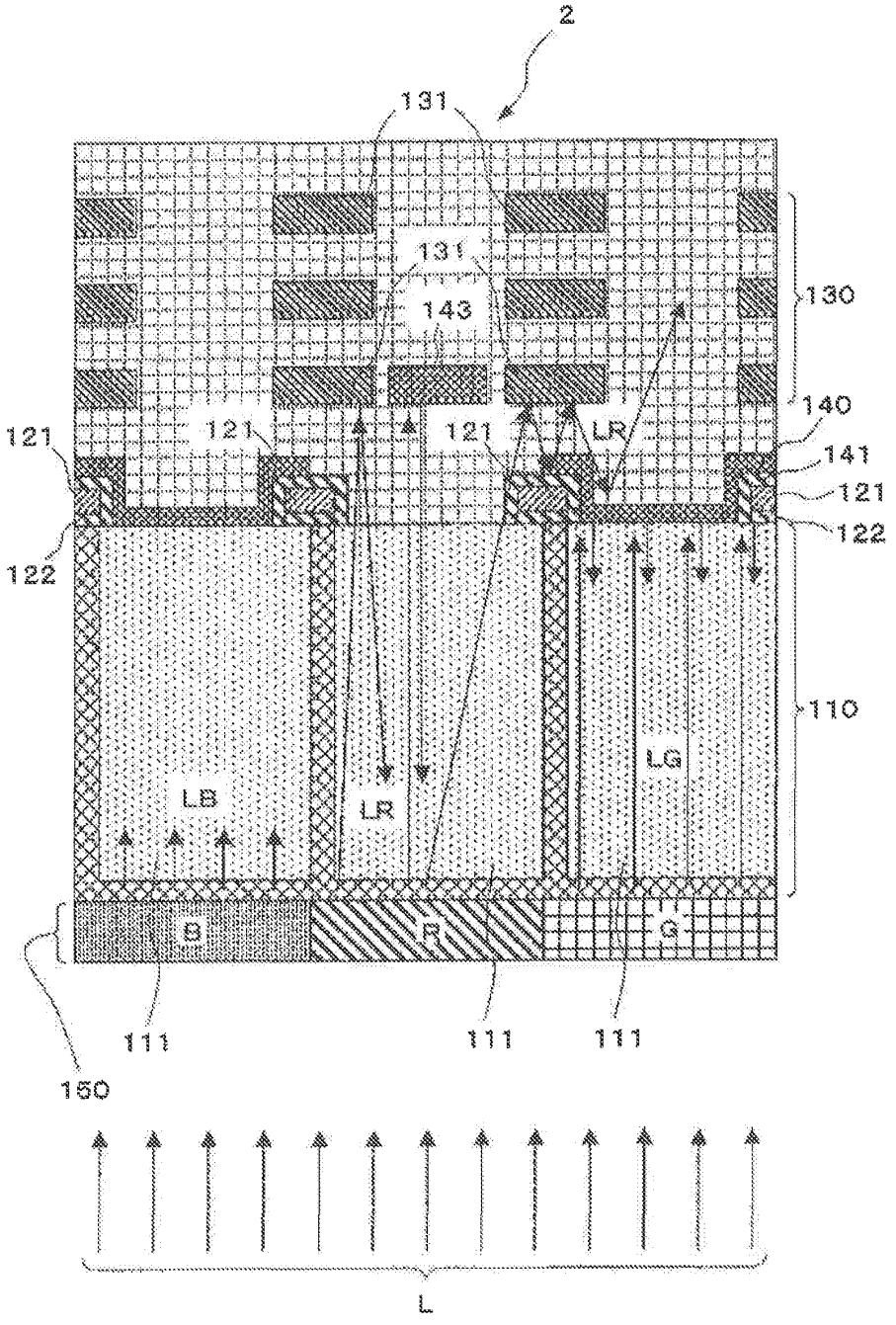

[Drawing 5]

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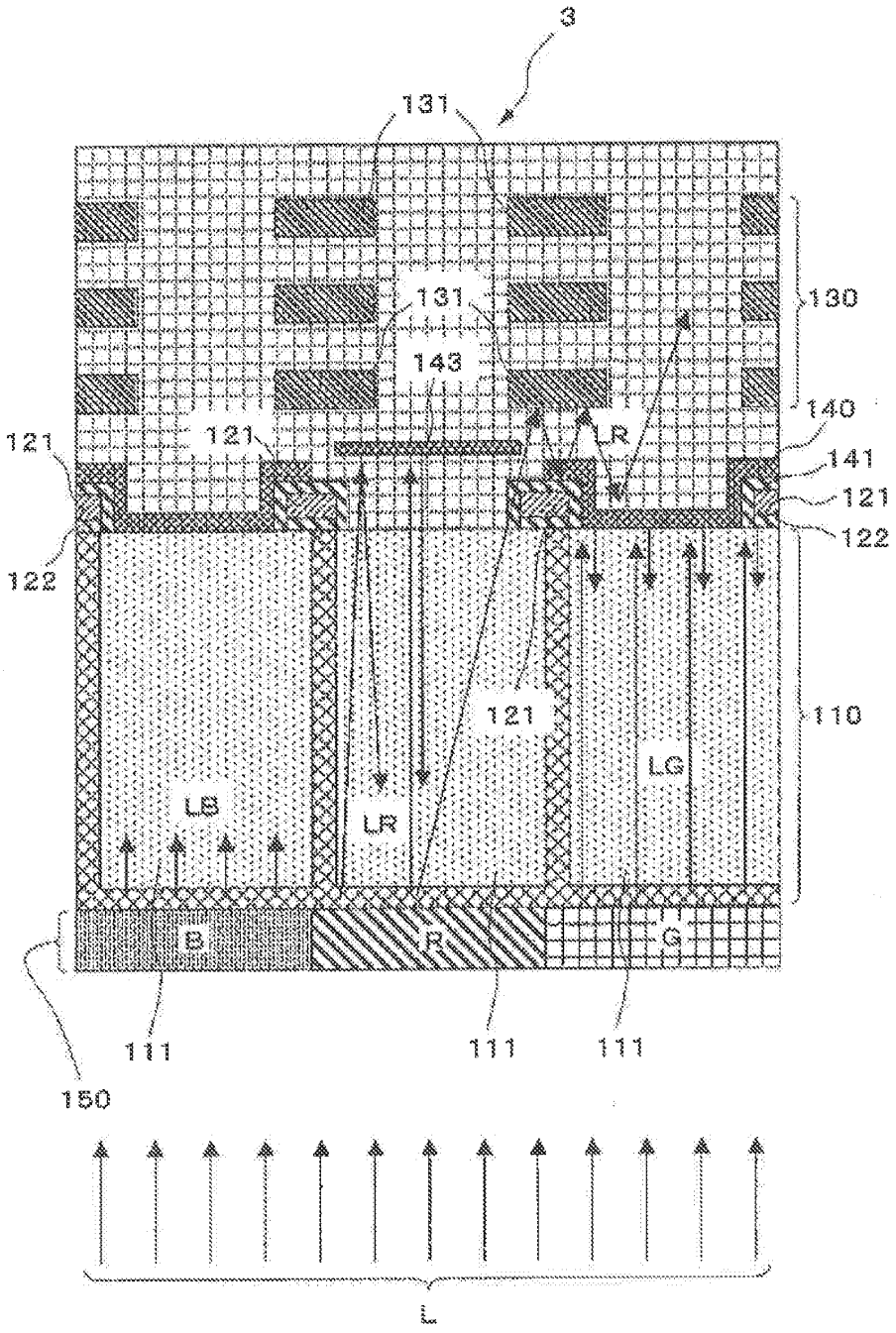

[Drawing 6]

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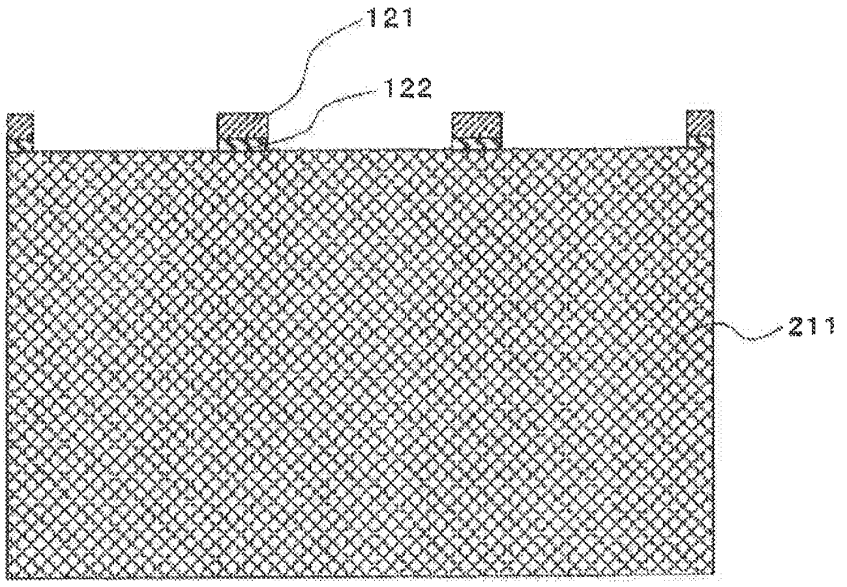

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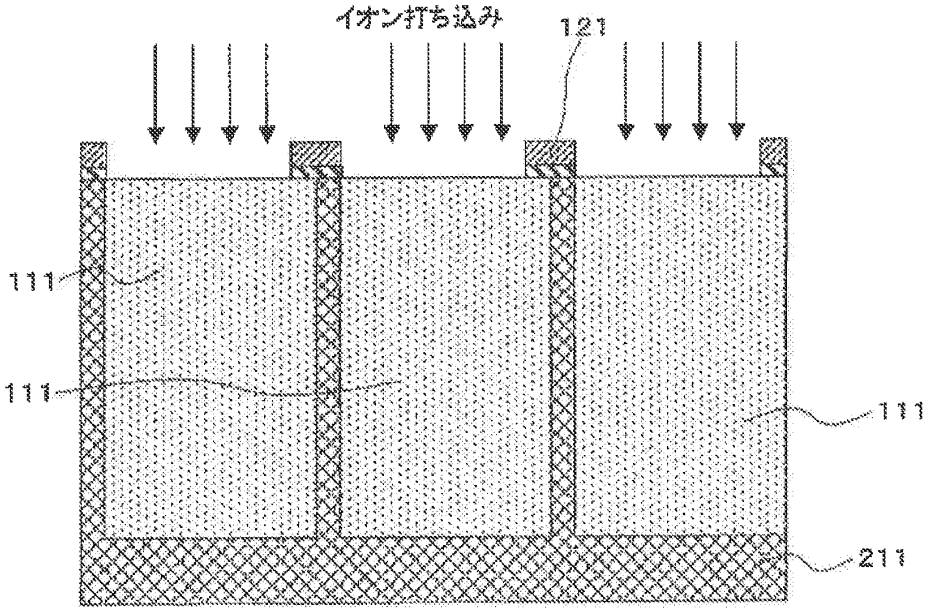

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[Drawing 7]

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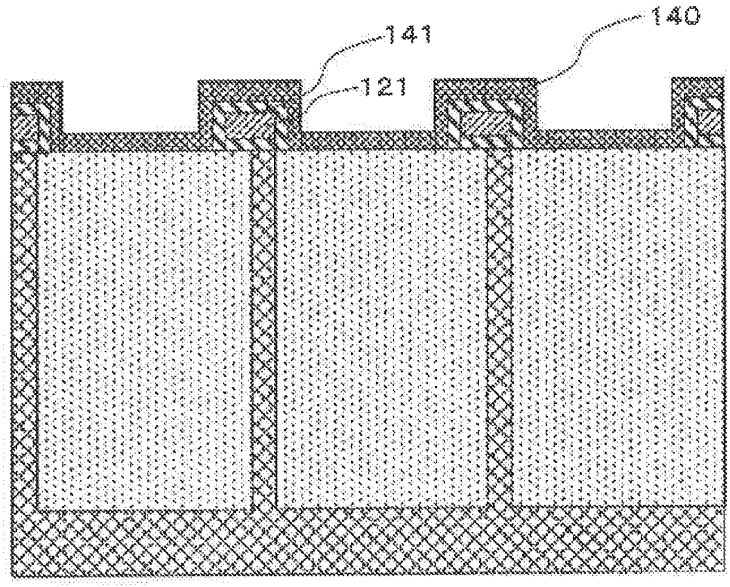

(3)

[Drawing 8]

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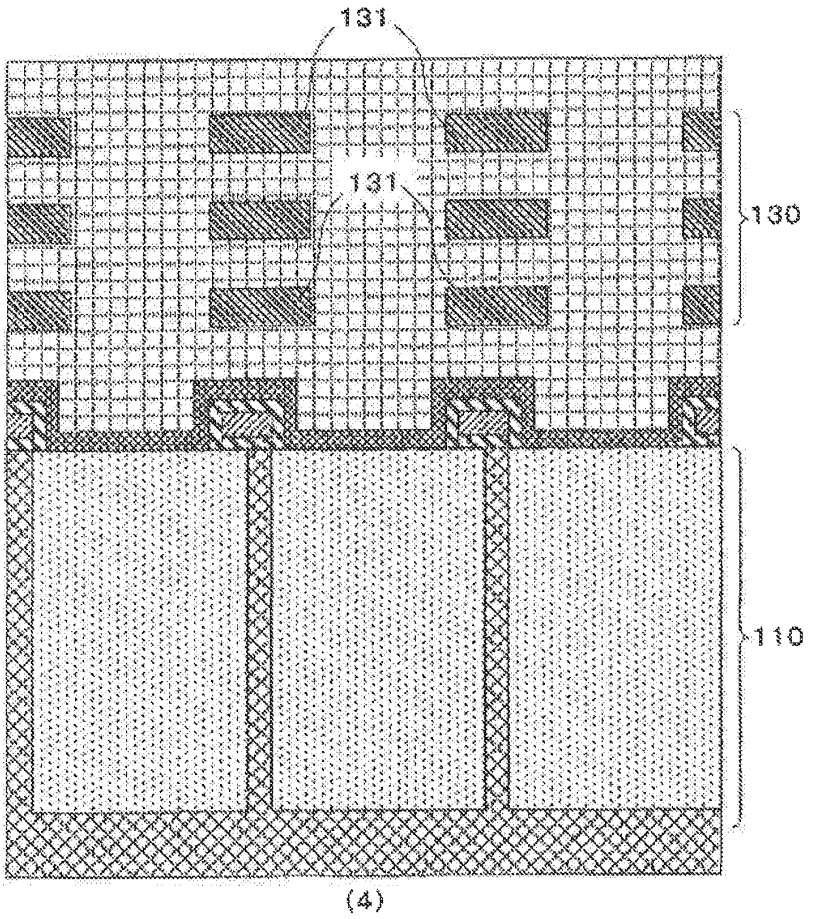

(4)

[Drawing 9]

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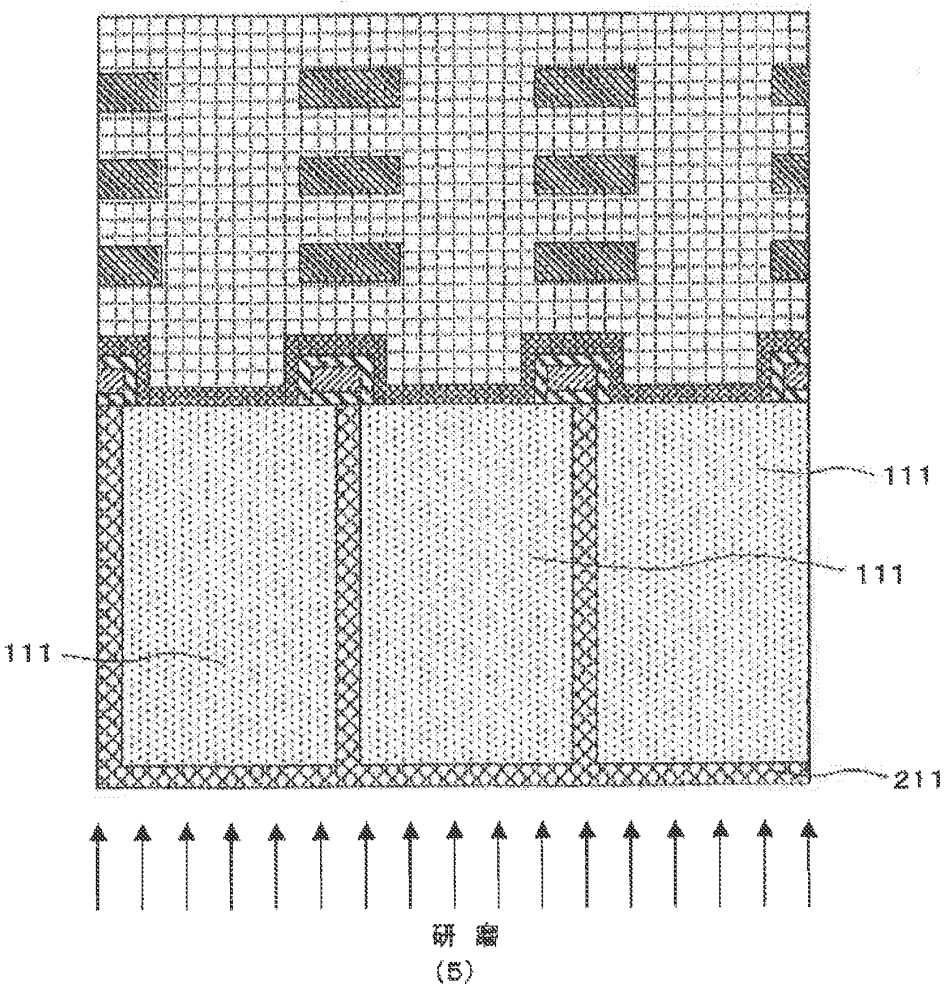

[Drawing 10]

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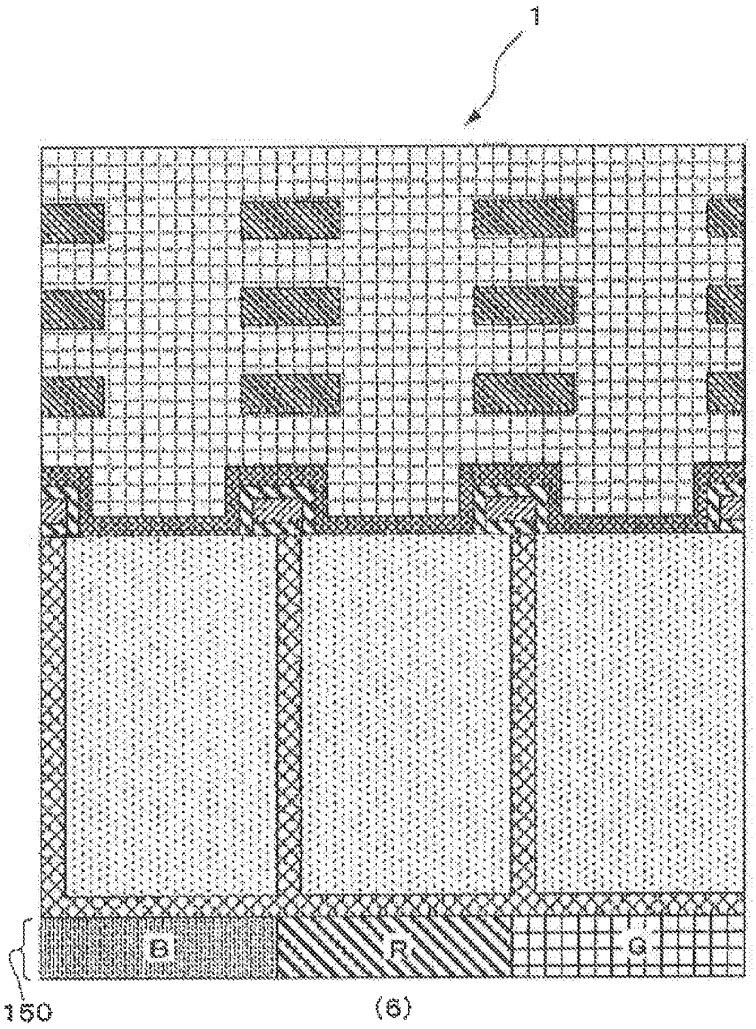

[Drawing 11]

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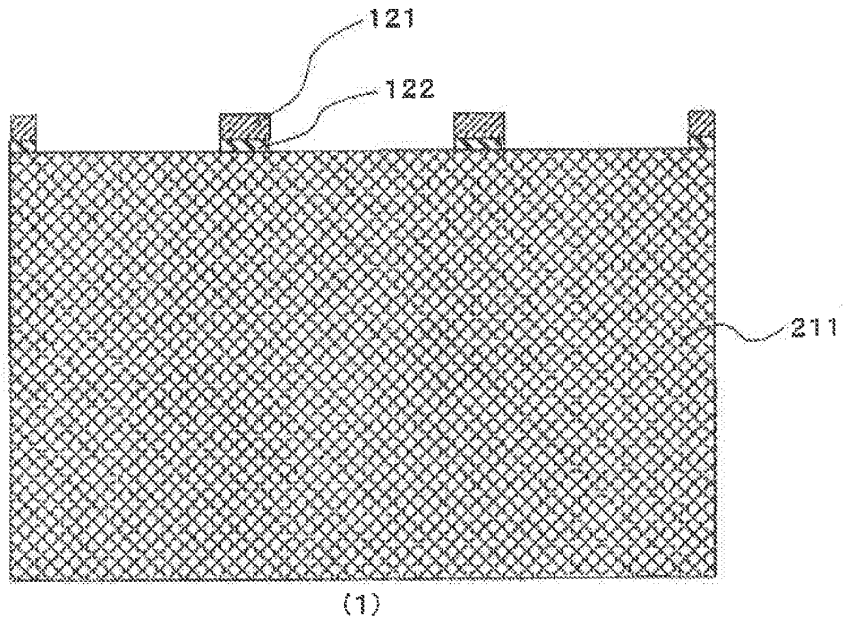

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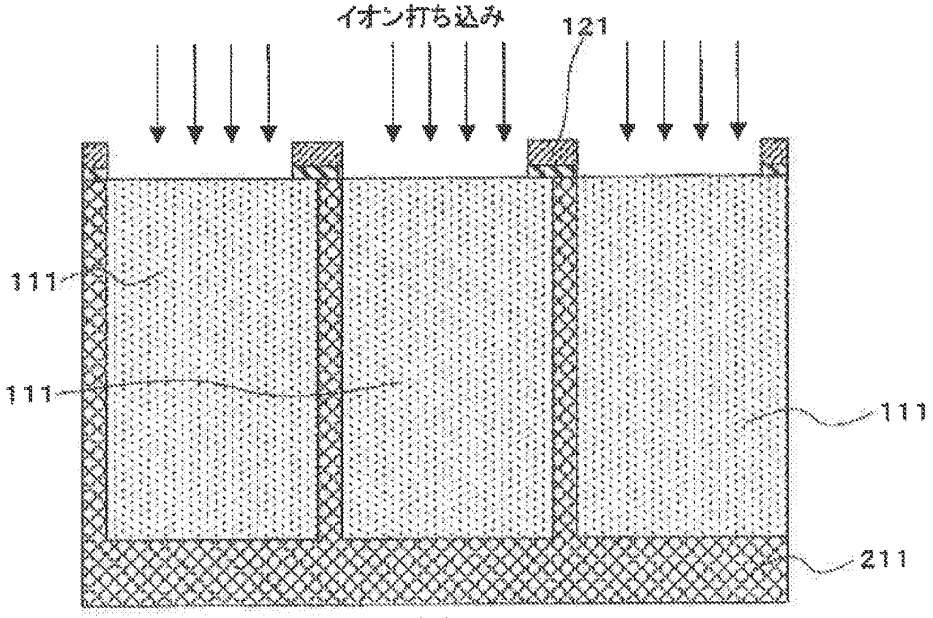

(2)

[Drawing 12]

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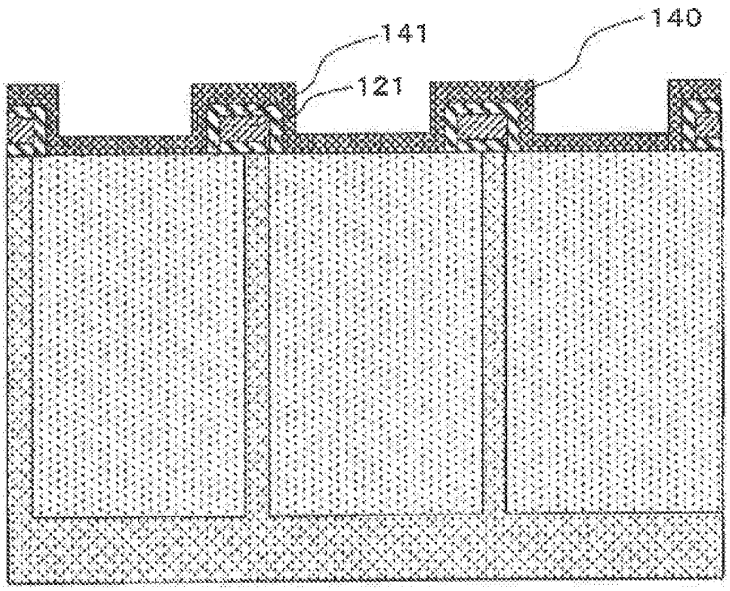

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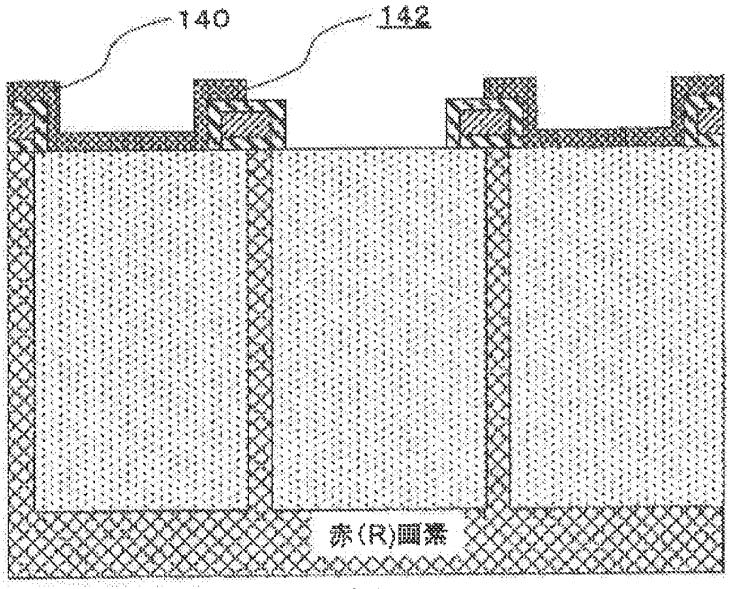

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[Drawing 13]

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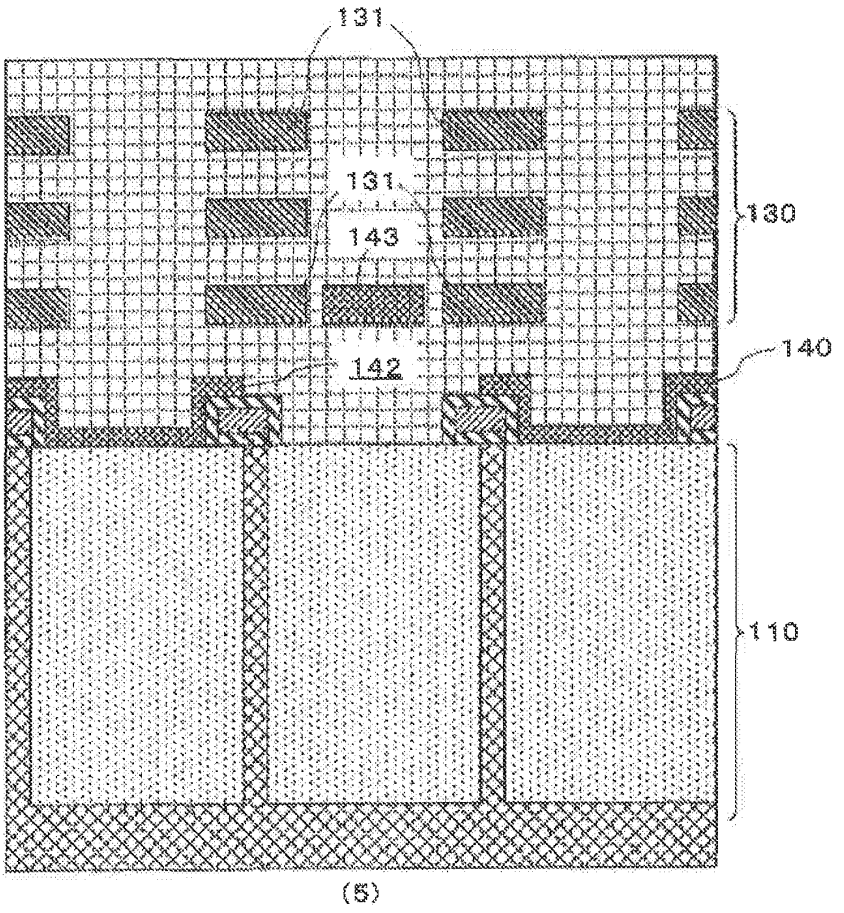

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[Drawing 14]

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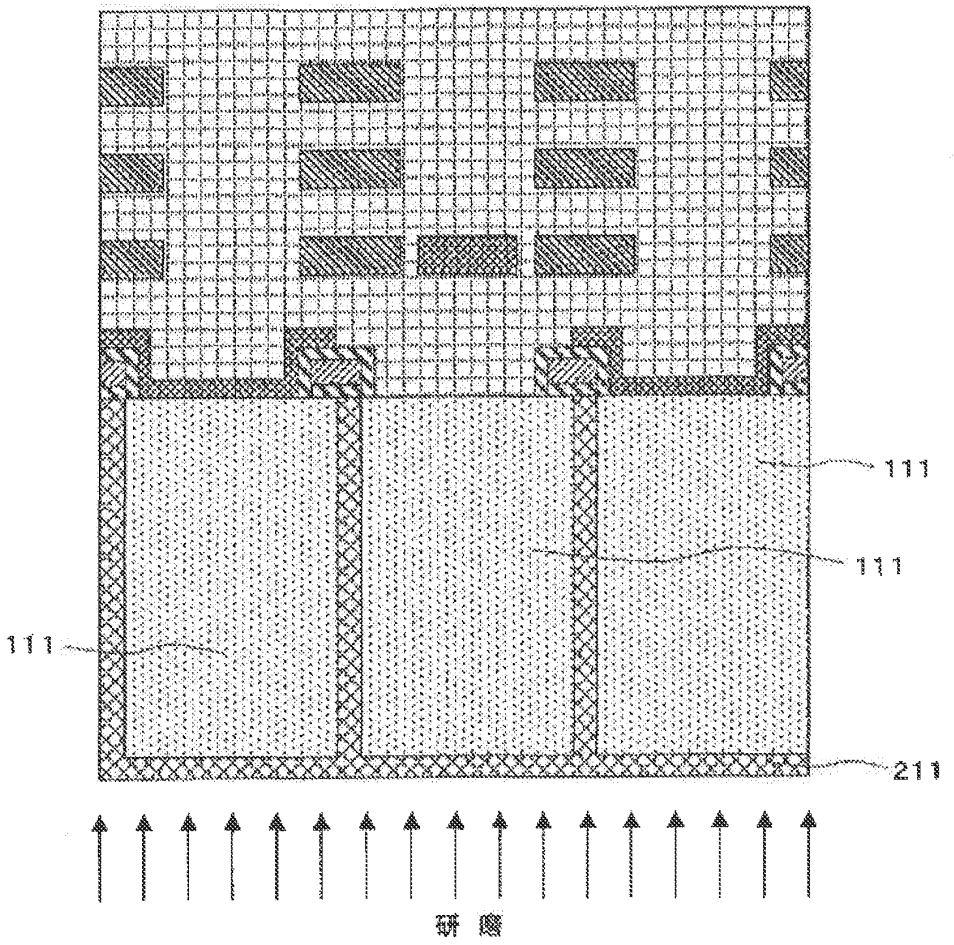

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[Drawing 15]

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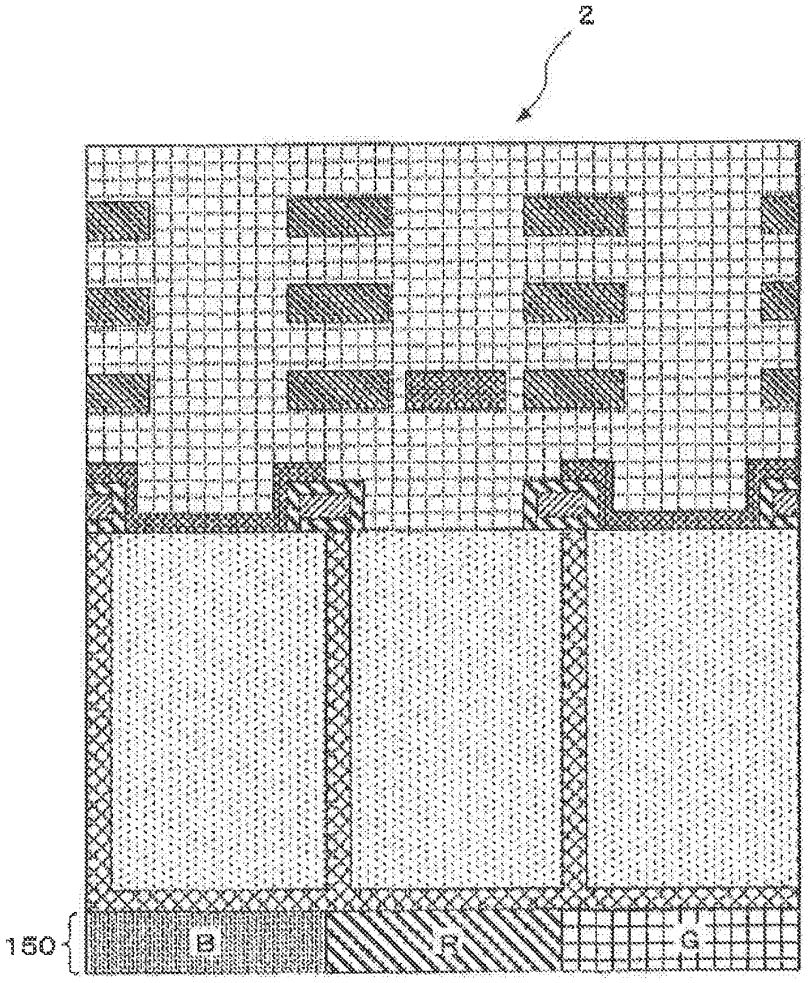

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[Drawing 16]

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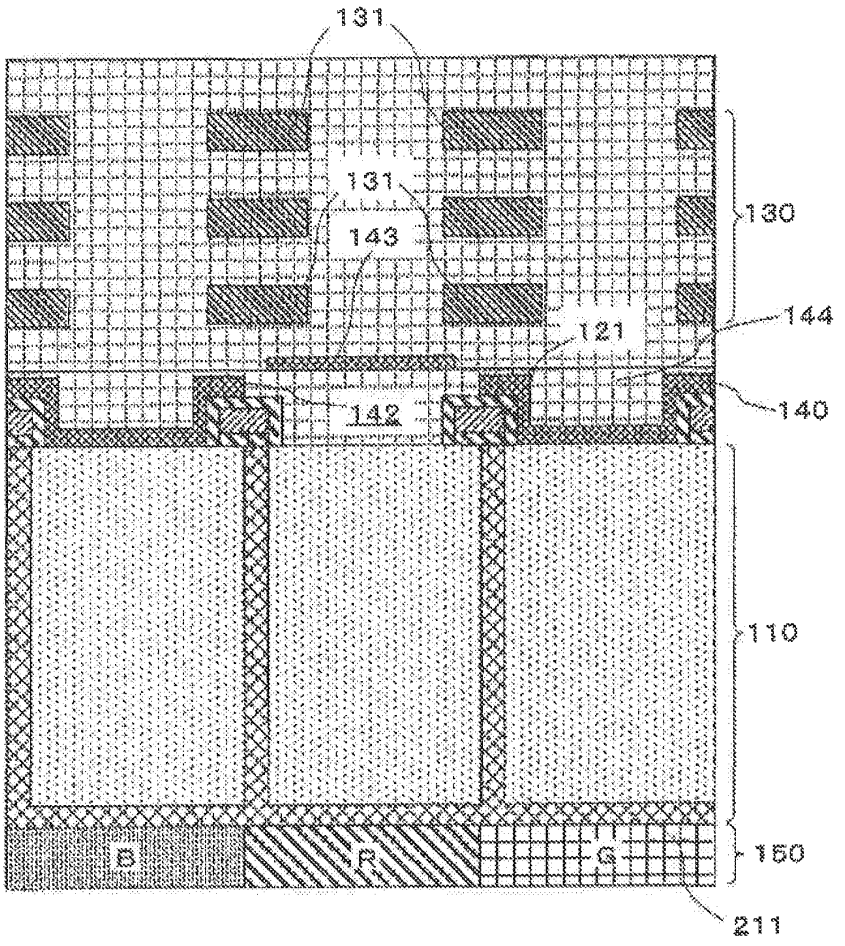

[Drawing 17]

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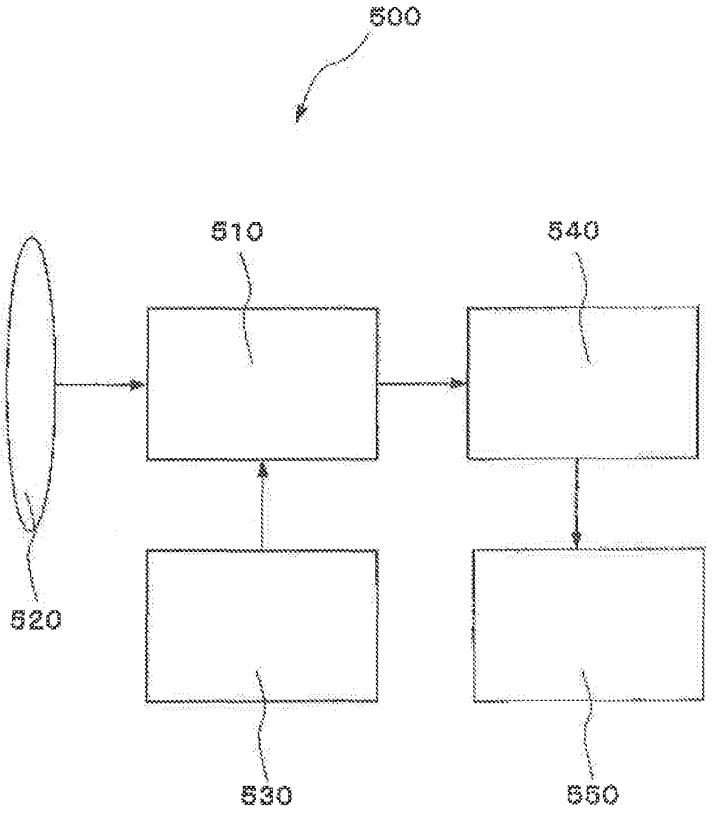

[Drawing 18]

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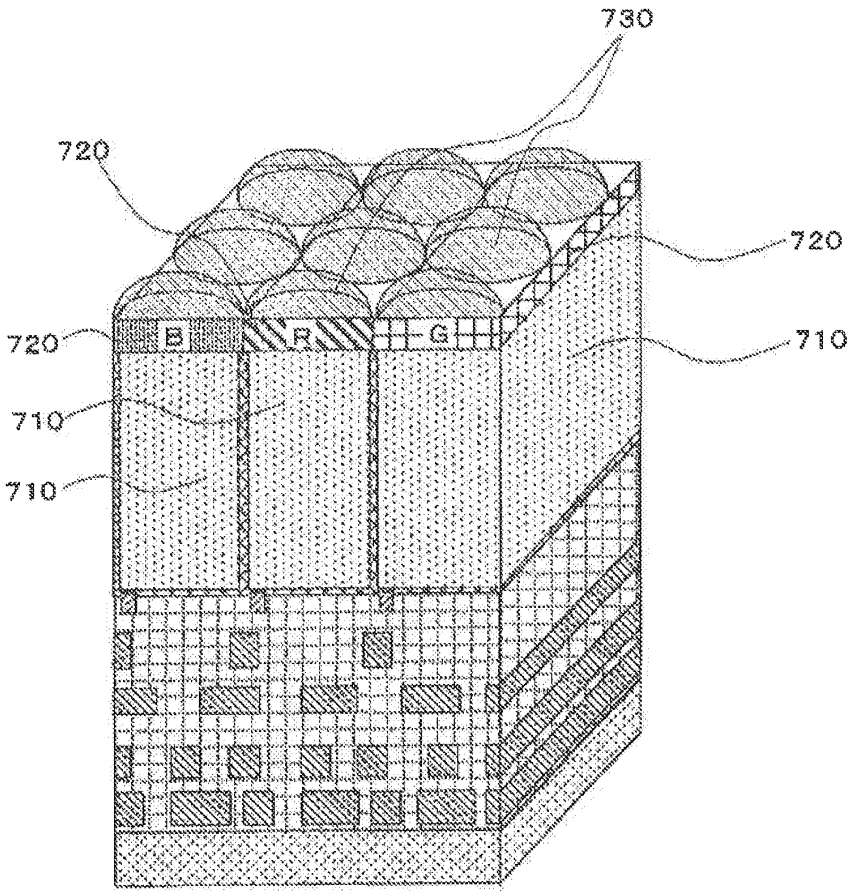

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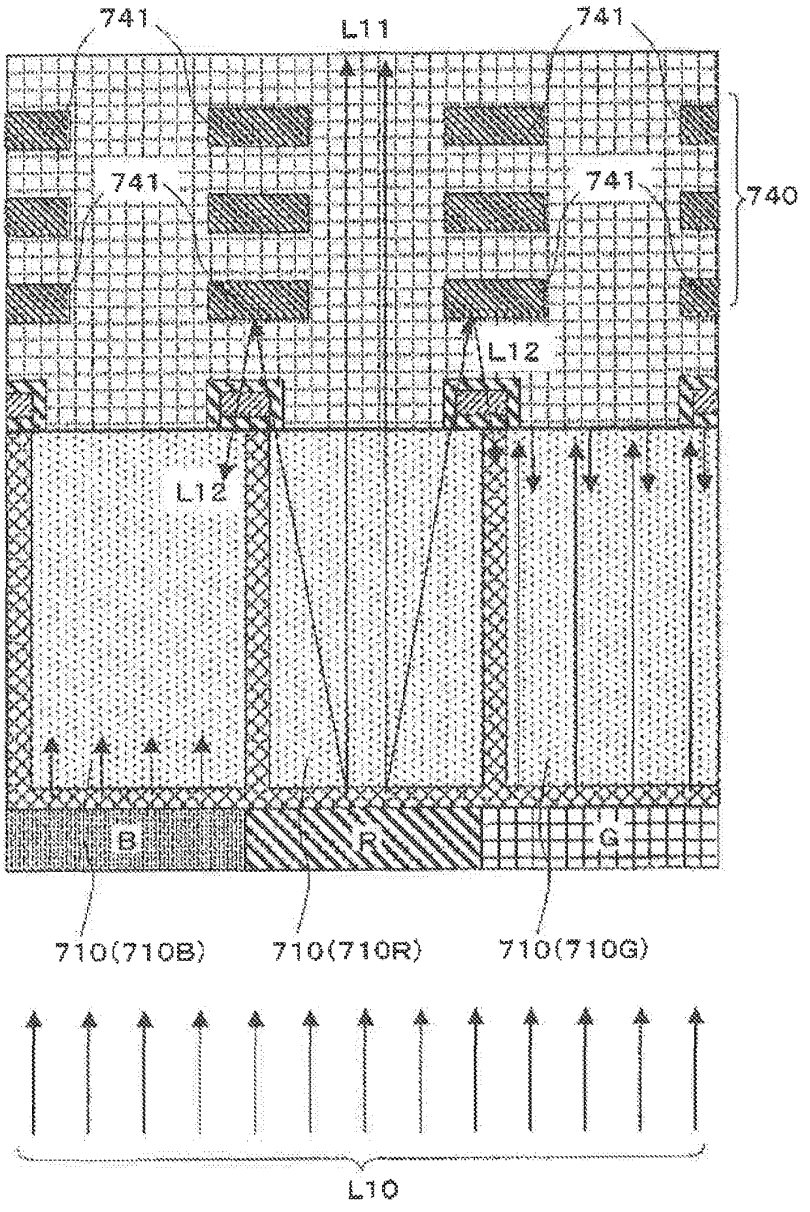
[Drawing 19]



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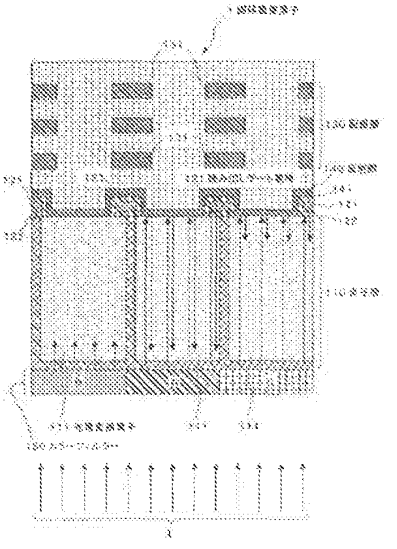
(54)【発明の名称】固体撮像素子および固体撮像素子の製造方法および画像撮影装置

(57)【要約】
【課題】読み出しゲート電極を被覆する反射膜を設けることで、隣接画素への混色を防止し、感度の向上を可能とする。
【解決手段】光電変換素子１１１で光電変換された信号電荷を電気信号に変換して出力する能動素子を含む複数の単位画素が配列されたもので、光電変換素子１１１が形成される素子層１１０に対してその一方の面側に、能動素子に対して配線１３１をなす配線層１３０を備え、入射光Ｌを素子層１１０の他方の面側に形成したカラーフィルター１５０を透過させて光電変換素子１１１に入射させる固体撮像素子１において、素子層１１０の配線層１３０側に、絶縁膜１４１を介して、能動素子のうちの光電変換された信号電荷を読み出す読み出しゲート電極１２１を含む画素全面を被覆するように形成した反射膜１４０を備えたものである。
【選択図】図１



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【特許請求の範囲】
【請求項１】
光電変換素子で光電変換された信号電荷を電気信号に変換して出力する能動素子を含む複数の単位画素が配列されたもので、
前記光電変換素子が形成される素子層に対してその一方の面側に、前記能動素子に対して配線をなす配線層を備え、
入射光を前記素子層の他方の面側に形成したカラーフィルターを透過させて前記光電変換素子に入射させる固体撮像素子において、
前記素子層の前記配線層側に、絶縁膜を介して、前記能動素子のうちの光電変換された信号電荷を読み出す読み出しゲート電極を含む画素全面を被覆するように形成した反射膜
を備えたことを特徴とする固体撮像素子。
【請求項２】
前記反射膜の前記カラーフィルターを透過する赤色光が入射される光電変換素子に対向する位置に開口部が形成されるとともに、
前記開口部の前記配線層側に反射膜が形成されている
ことを特徴とする請求項１記載の固体撮像素子。
【請求項３】
前記反射層は前記配線層の配線間に前記配線と間隔を置いて形成されている
ことを特徴とする請求項２記載の固体撮像素子。
【請求項４】
前記反射層は前記素子層と前記配線層との間に絶縁膜を介して形成されている
ことを特徴とする請求項２記載の固体撮像素子。
【請求項５】
光電変換素子で光電変換された信号電荷を電気信号に変換して出力する能動素子を含む複数の単位画素が配列されたもので、
前記光電変換素子が形成される素子層に対してその一方の面側に、前記能動素子に対して配線をなす配線層を備え、
入射光を前記素子層の他方の面側に形成したカラーフィルターを透過させて前記光電変換素子に入射させる固体撮像素子の製造方法において、
前記素子層が形成される半導体層に信号電荷を読み出す読み出し電極を形成する工程と
前記半導体層に前記光電変換素子を形成する工程と、
前記半導体層の前記配線層が形成される側に、絶縁膜を介して前記読み出し電極を含む画素全面を被覆するように反射膜を形成する工程と
を備えたことを特徴とする固体撮像素子の製造方法。
【請求項６】
前記反射膜の前記カラーフィルターを透過する赤色光が入射される光電変換素子に対向する位置に開口部を形成する工程と、
前記開口部の前記配線層側に絶縁膜を介して反射膜を形成する工程と
を備えたことを特徴とする請求項５記載の固体撮像素子の製造方法。
【請求項７】
前記反射層は前記配線層の配線間に前記配線と間隔を置いて形成される
ことを特徴とする請求項６記載の固体撮像素子の製造方法。
【請求項８】
前記反射層は前記素子層と前記配線層との間に絶縁膜を介して形成される
ことを特徴とする請求項６記載の固体撮像素子の製造方法。
【請求項９】
固体撮像素子を撮像素子に用いた画像撮影装置において、
前記固体撮像素子は、
光電変換素子で光電変換された信号電荷を電気信号に変換して出力する能動素子を含む

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複数の単位画素が配列されたもので、
前記光電変換素子が形成される素子層に対してその一方の面側に、前記能動素子に対して配線をなす配線層を備え、
入射光を前記素子層の他方の面側に形成したカラーフィルターを透過させて前記光電変換素子に入射させる固体撮像素子であって、
前記素子層の前記配線層側に、絶縁膜を介して、前記能動素子のうちの光電変換された信号電荷を読み出す読み出しゲート電極を含む画素全面を被覆するように形成した反射膜を備えたものからなる
ことを特徴とする画像撮影装置。

【発明の詳細な説明】
【技術分野】
【０００１】
本発明は、入射した光を光電変換する効率を高めるとともに、光が入射される側とは反対側に設けた配線で反射される反射光による混色を防止することが容易な固体撮像素子およびその固体撮像素子の製造方法およびその固体撮像素子を用いた画像撮影装置に関するものである。
【背景技術】
【０００２】
新しいイメージセンサの構造として、電極や配線などが形成されている面と反対の裏面側にフォトダイオードを形成し、裏面より光を照射して光電変換を行う裏面照射型イメージセンサが提案されている。この構造は、画素領域全面にフォトダイオードを形成することができ、理論上受光面の開口面積を１００％にすることができる。
【０００３】
また、裏面照射型イメージセンサを単板カラーセンサとして用いる場合、図１８に示すように、従来のイメージセンサと同様に光電変換素子７１０の受光面よりも上層での混色を防ぐために、カラーフィルター７２０の上層にオンチップマイクロレンズ７３０が形成されている（例えば、特許文献１参照。）。このオンチップマイクロレンズ７３０は、電極や配線層がないことにより光電変換素子７１０の受光面の近くに形成することができ、焦点距離の短いレンズとなる。このため、イメージセンサが搭載される機器のレンズのＦ値および射出瞳距離の変動に対する集光状態のバラツキは減少し、安定した画質を提供することができる。裏面照射型ＣＭＯＳイメージセンサでは、通常、光電変換素子（例えばフォトダイオード）層の厚みは５μｍ～７μｍ程度となっている。
【０００４】
表１に、可視光領域におけるシリコン（Ｓｉ）の吸収係数αと、シリコン（Ｓｉ）中に入射した光が９０％吸収される深さ、深さが７μｍの領域内で光が吸収される割合を示す。
【０００５】

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【表１】

波長λ［ｎｍ］	吸収係数α［ｃｍ$^{-1}$］	入射光が９０％吸収される深さ［μｍ］	７μｍの領域での光吸収率
４００	１．２２Ｅ＋０５	０．１９	１
４５０	４．６３Ｅ＋０４	０．５０	１
５００	１．８５Ｅ＋０４	１．２５	１
５５０	６．３０Ｅ＋０３	３．６５	０．９９
６００	５．００Ｅ＋０３	４．６１	０．９７
６５０	３．２７Ｅ＋０３	７．０４	０．９０
７００	２．００Ｅ＋０３	１１．５１	０．７５

【０００６】
表１から明らかなように、深さが７μｍの光電変換領域（フォトダイオード）では、シリコン（Ｓｉ）中に入射した光は４００ｎｍ～５５０ｎｍの波長ではほぼ１００％吸収されるか、それ以上の長い波長の光では吸収されずに透過する成分が増えることを示している。すなわち、図１９に示すように、裏面照射型ＣＭＯＳイメージセンサの光電変換素子７１０に入射した光Ｌ１０は、長波長側において光電変換素子７１０Ｒを透過する成分が存在し、光電変換素子７１０に入射した光をすべて光電変換させ、感度に寄与させることができない。
【０００７】
また、光電変換領域７１０Ｒを透過した光Ｌ１１が配線層７４０に到達し、その配線７４１によって反射した光Ｌ１２が隣接画素の光電変換素子７１０Ｇ、７１０Ｂに入射して光電変換を発生する、いわゆる混色が発生し、画質に影響を及ぼす。
【０００８】
【特許文献１】特開２００３－３１７８５号公報
【発明の開示】
【発明が解決しようとする課題】
【０００９】
解決しようとする問題点は、裏面照射型ＣＭＯＳイメージセンサの光電変換領域に入射した光は、長波長側において光電変換領域を透過する成分が存在し、光電変換領域に入射した光をすべて光電変換させ、感度に寄与させることができない点である。また、これら光電変換領域を透過した光が配線層に到達し、その配線によって反射した光が隣接画素の光電変換領域に入射して光電変換を発生する、いわゆる混色が発生し、画質に影響を及ぼす点である。
【００１０】
本発明は、上記問題点を解決すべく、フォトダイオードに入射した光を光電変換する効率を高め、さらに、表面側の配線での反射による混色を防止することを課題としている。
【課題を解決するための手段】
【００１１】
本発明の固体撮像素子は、光電変換素子で光電変換された信号電荷を電気信号に変換して出力する能動素子を含む複数の単位画素が配列されたもので、前記光電変換素子が形成される素子層に対してその一方の面側に、前記能動素子に対して配線をなす配線層を備え、入射光を前記素子層の他方の面側に形成したカラーフィルターを透過させて前記光電変換素子に入射させる固体撮像素子において、前記素子層の前記配線層側に、絶縁膜を介して、前記能動素子のうちの光電変換された信号電荷を読み出す読み出しゲート電極を含む画素全面を被覆するように形成した反射膜を備えたことを特徴とする。
【００１２】
本発明の固体撮像素子の製造方法は、光電変換素子で光電変換された信号電荷を電気信

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号に変換して出力する能動素子を含む複数の単位画素が配列されたもので、前記光電変換素子が形成される素子層に対してその一方の面側に、前記能動素子に対して配線をなす配線層を備え、入射光を前記素子層の他方の面側に形成したカラーフィルターを透過させて前記光電変換素子に入射させる固体撮像素子の製造方法において、前記素子層が形成される半導体層に信号電荷を読み出す読み出し電極を形成する工程と、前記半導体層に前記光電変換素子を形成する工程と、前記半導体層の前記配線層が形成される側に、絶縁膜を介して前記読み出し電極を含む画素全面を被覆するように反射膜を形成する工程とを備えたことを特徴とする。

【００１３】

本発明の画像撮影装置は、固体撮像素子を撮像素子に用いた画像撮影装置において、前記固体撮像素子は、光電変換素子で光電変換された信号電荷を電気信号に変換して出力する能動素子を含む複数の単位画素が配列されたもので、前記光電変換素子が形成される素子層に対してその一方の面側に、前記能動素子に対して配線をなす配線層を備え、入射光を前記素子層の他方の面側に形成したカラーフィルターを透過させて前記光電変換素子に入射させる固体撮像素子であって、前記素子層の前記配線層側に、絶縁膜を介して、前記能動素子のうちの光電変換された信号電荷を読み出す読み出しゲート電極を含む画素全面を被覆するように形成した反射膜を備えたものからなることを特徴とする。

【発明の効果】

【００１４】

本発明の固体撮像素子は、素子層の配線層側に、絶縁膜を介して、能動素子のうちの光電変換された信号電荷を読み出す読み出しゲート電極を含む画素全面を被覆するように形成した反射膜を備えたため、光電変換素子で完全に吸収されずに一部透過された長波長の光（例えば赤色光）を反射膜によって長波長の光を光電変換する光電変換素子に戻すことができるので、光電変換素子に入射した光を効率的に光電変換できるという利点がある。また、反射膜が配線層の配線による反射を防止するので、反射光が隣接する画素へ入射されなくなり、混色を防止することができるという利点がある。

【００１５】

本発明の固体撮像素子の製造方法は、半導体層の配線層が形成される側に、絶縁膜を介して読み出し電極を含む画素全面を被覆するように反射膜を形成する工程を備えているため、光電変換素子で完全に吸収されずに一部透過された長波長の光（例えば赤色光）を反射膜によって長波長の光を光電変換する光電変換素子に戻すようにすることができるので、光電変換素子に入射した光を効率的に光電変換できるようになるという利点がある。また、反射膜が配線層の配線による反射を防止するので、反射光が隣接する画素へ入射されなくなり、混色を防止することができるという利点がある。

【００１６】

本発明の画像撮影装置は、撮像素子に本発明の固体撮像素子を搭載しているため、入射光を効率的に光電変換でき、隣接する画素への混色を防止することができるので、感度の向上、画質の向上が図れるという利点がある。

【発明を実施するための最良の形態】

【００１７】

本発明の固体撮像素子に係る実施の形態の一例（第１例）を、図１の概略構成断面図によって説明する。

【００１８】

図１に示すように、本発明の固体撮像素子１は、半導体材で構成される素子層１１０に光電変換素子（例えばフォトダイオード）１１１が形成され、この光電変換素子１１１で光電変換された信号電荷を電気信号に変換して出力する能動素子（図示せず）を含む複数の単位画素が配列されたものであり、上記光電変換素子１１１が形成される素子層１１０に対してその一方の面側に、上記能動素子に対して配線をなす配線層１３０を備えている。上記光電変換素子１１１は、例えば５μｍ～１５μｍの厚さのシリコン層で形成されている。また、入射光Ｌを素子層１１０の他方の面側にはカラーフィルター１５０が形成さ

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れている。また、上記素子層１１０の配線層１３０側には、上記能動素子のうちの光電変換された信号電荷を読み出す読み出しトランジスタを構成する読み出しゲート電極１２１が絶縁膜１２２を介して形成されている。この読み出しゲート電極１２１は、例えば多結晶シリコンで形成されている。このため、読み出しゲート電極１２１は光透過性を有する。

【００１９】

上記読み出しゲート電極１２１を含む画素全面を、絶縁膜１４１を介して被覆するように反射膜１４０が形成されている。

【００２０】

上記反射膜１４０は、例えば、アルミニウム、酸化アルミニウム等で形成される。特に、アルミニウム膜は、可視光線に対しておよそ９０％以上の表面反射率を得ることができる。したがって、上記反射膜１４０にアルミニウム膜を採用することが好ましい。また、後に説明するか、反射させる光の波長が緑色光、赤色光であることを考慮すると、緑色光、赤色光の反射率が高真空蒸着法により形成された膜では９５％以上を有する銀を用いることも可能である。

【００２１】

ここで、反射膜１４０としてアルミニウム膜を用いた場合の必要膜厚について、図２によって説明する。図２は、可視光領域におけるアルミニウム（Ａｌ）の各膜厚をパラメータとして、左縦軸に透過率を示し、右縦軸に反射率を示し、横軸に入射光の波長を示す。

【００２２】

図２に示すように、光電変換素子１１１を透過し、さらに反射膜１４０のアルミニウム膜を透過し、上層の配線１３１で反射して隣の画素に表面側から反射膜１４０を透過して光電変換素子１１１に入射すると混色になる。その混色量は、光電変換素子１１１を透過してアルミニウム面に到達した光を１００％とすると、アルミニウム（Ａｌ）の反射率は可視光領域でほぼ９０％であるので、アルミニウム膜の透過率が０．１％の場合で０．０００９％、アルミニウム膜の透過率が１％の場合で０．００９％、アルミニウム膜の透過率が１０％の場合でも０．９％である。アルミニウム面に到達する時点で光電変換素子１１１に入射する光の強度は赤（Ｒ）の画素で約１０％になっていることを考慮すると透過率は１％程度に抑えられていれば十分である。従って、反射膜１４０にアルミニウム膜を用いた場合には、その膜厚は３０ｎｍ以上あればよいことになる。

【００２３】

上記固体撮像素子１が受光する入射光Ｌは、上記カラーフィルター１５０を透過して光電変換素子１１１に入る。例えば、上記カラーフィルター１５０が青（Ｂ）、緑（Ｇ）、赤（Ｒ）の３色（例えば光の３原色）で形成されている場合には、カラーフィルター１５０を透過して上記光電変換素子１１１が受光する入射光Ｌは、上記光電変換素子１１１の厚さが７μｍ～１５μｍに形成されていることから、青色光は波長が短いため光電変換素子１１１の入射側近傍でほぼ１００％吸収されて光電変換されるため、反射膜１４０に達するような透過光とはなり得ない。緑色光は光電変換素子１１１内で大部分が吸収されるが、一部は透過成分となっている。しかしながら、反射膜１４０によって反射され、再び光電変換素子１１１に戻されるので、光電変換素子１１１においてほとんど吸収されることになる。一方、赤色光は光電変換素子１１１を一部は透過する。そのため、光電変換素子１１１で光電変換される赤色光の光量が他の色よりも少なくなっていた。しかしながら、上記反射膜１４０が設けられていることから、光電変換素子１１１を透過した赤色光は反射膜１４０によって反射され、再び光電変換素子１１１に入射される。このため、赤色光の光電変換量が他の色の光電変換量とほぼ同等となり、感度の低下を防止することができる。

【００２４】

また、上記反射膜１４０は、各画素の直上に形成されていることから、各画素の光電変換素子１１１を透過した光、特に、緑色光～赤色光は、反射膜１４０によって反射され、その反射光はそのまま透過してきた光電変換素子１１１に入射されるため、隣接画素への

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反射はほとんどない。このため、混色が抑制され、良好な画質を得ることができる。

【００２５】

また、上記反射膜１４０は、多結晶シリコンからなる読み出しゲート電極１２１を被覆するように形成されていることから、読み出しゲート電極１２１を透過した光も反射膜１４０によって反射させて光電変換素子１１１に戻すことができる。したがって、光電変換素子１１１では入射光を効率よく光電変換することが可能になる。

【００２６】

次に、上記構成の固体撮像素子を適用できるＣＭＯＳセンサの詳細の一例を、図３の概略構成断面図によって説明する。

【００２７】

裏面受光型のＣＭＯＳセンサ１０１は、シリコン層からなる素子層１１０に、画素部と周辺回路部が形成されている。上記素子層１１０にはＮ⁻型シリコン基板を例えば化学的機械研磨により所望の厚さに研磨したものを用い、通常、可視光線を受光する領域では、５μｍ～１５μｍの厚さに形成されている。また、赤外光を受光する場合には、１５μｍ～５０μｍの厚さに、紫外光を受光する場合には３μｍ～７μｍの厚さに形成されることが望ましい。

【００２８】

上記素子層１１０の画素部には光電変換領域１１１となるＮ⁻型層からなるフォトセンサが形成されている。このＮ⁻型層は上記Ｎ⁻型シリコン基板を用いている。上記光電変換領域１１１の上部にはＮ⁺層１１２が形成され、さらに上部には埋め込みフォトダイオードとするためのＰ⁺層からなる電荷蓄積層１１３が形成されている。

【００２９】

また上記光電変換領域１１１の画素部には、上記光電変換領域１１１～電荷蓄積層１１３の側周を囲むように、Ｐ型のウエル領域１１５が形成されている。このＰ型ウエル領域１１５の一部は、素子層１１０を貫通するように形成され、その部分が画素間分離領域１１６となっている。さらに上記素子層１１０の下部側には上記Ｐ型のウエル領域１１５（画素間分離領域１１６）に接続するＰ⁺層１１７が形成されている。このＰ⁺層１１７側が、光が入射される側になっている。そして、上記光電変換領域１１１は、受光領域を広く確保するため、上記Ｐ⁺層１１７側のレイアウト上の占有面積が広くなるように形成されている。

【００３０】

上記Ｎ⁺層１１２および電荷蓄積層１１３の一方側には読み出し領域１２３がＰ⁻層で形成されている。上記読み出し領域１２３上には絶縁膜１２２を介して読み出しゲート電極１２１が形成されている。さらに上記読み出しゲート電極１２１の電荷蓄積層１１３とは反対側には読み出し領域１２３に隣接してＮ⁺層からなるフローティングディフュージョン層１２５が形成されている。このように、読み出しトランジスタ１２０が構成されている。

【００３１】

また、上記Ｐ型のウエル領域１１５には、上記読み出しトランジスタ１２０以外のトランジスタ１６０が形成されている。このトランジスタ１６０としては、例えばリセットトランジスタ、増幅トランジスタ、垂直選択トランジスタ等があり、ＮＭＯＳトランジスタで構成されている。

【００３２】

上記読み出しゲート電極１２１を含む画素全面を、絶縁膜１４１を介して被覆するように反射膜１４０が形成されている。この反射膜１４０は、例えば、アルミニウム、酸化アルミニウム等で形成される。特に、アルミニウム膜は、可視光線に対しておよそ９０％以上の表面反射率を得ることができる。したがって、上記反射膜１４０にアルミニウム膜を採用することが好ましい。また、後に説明するが、反射させる光の波長が緑色光、赤色光であることを考慮すると、緑色光、赤色光の表面反射率が９５％以上を有する銀を用いることも可能である。

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【００３３】
上記素子層１１０の一方側の面（図面では上部側の面、以下表面という）には、上記読み出しトランジスタ１２０、トランジスタ１６０等を覆う絶縁膜１３２が形成され、その絶縁膜中には、複数層に形成された配線１３１からなる配線層１３０が形成され、さらに支持基板１７０が設けられている。
【００３４】
また、上記素子層１１０の他方側の面（図面では下部側の面、以下裏面という）には、透明絶縁膜１８１を介して遮光膜１８２が形成されている。この遮光膜１８２は、画素領域以外に入射光が照射されるのを防止するためのもので、光電変換素子１１１が形成される領域に対向する位置には、光電変換素子１１１に光が入射されるように開口部１８３が形成されている。さらに透明絶縁膜１８４を介してカラーフィルター１５０が形成されている。このカラーフィルター１５０は、例えば光の３原色の赤（Ｒ）、緑（Ｇ）、青（Ｂ）の３色からなり、それぞれ、所定の色を受光する光電変換素子１１１上に設けられている。なお、カラーフィルター１５０は３原色に限定されず、３原色の他に、例えば３原色の中間色のような、例えばエメラルドグリーンのカラーフィルター、橙色のカラーフィルター等を設けることもできる。さらに各カラーフィルター１５０上にマイクロレンズ１５５が形成されている。
【００３５】
次に、本発明の固体撮像素子に係る実施の形態の一例（第２例）を、図４の概略構成断面図によって説明する。
【００３６】
図４に示すように、本発明の固体撮像素子２は、半導体層で構成される素子層１１０に光電変換素子（例えばフォトダイオード）１１１が形成され、この光電変換素子１１１で光電変換された信号電荷を電気信号に変換して出力する能動素子（図示せず）を含む複数の単位画素が配列されたものであり、上記光電変換素子１１１が形成される素子層１１０に対してその一方の面側に、上記能動素子に対して配線をなす配線層１３０を備えている。上記光電変換素子１１１は、例えば５μｍ～１５μｍの厚さのシリコン層で形成されている。また、入射光Ｌを素子層１１０の他方の面側にはカラーフィルター１５０が形成されている。また、上記素子層１１０の配線層１３０側には、上記能動素子のうちの光電変換された信号電荷を読み出す読み出しトランジスタ１２０を構成する読み出しゲート電極１２１が絶縁膜１２２を介して形成されている。この読み出しゲート電極１２１は、例えば多結晶シリコンで形成されている。このため、読み出しゲート電極１２１は光透過性を有する。
【００３７】
上記読み出しゲート電極１２１を含む、画素の全面には絶縁膜１４１を介して被覆するように反射膜１４０が形成されている。ただし、緑（Ｇｒｅｅｎ）画素および青（Ｂｌｕｅ）画素の全面は反射膜１４０が形成されているが、カラーフィルター１５０を透過する赤色光が入射される光電変換素子１１１に対向する位置の上記反射膜１４０には開口部１４２が形成されている。さらに、上記開口部１４２の上記配線層１３０側に反射層１４３が形成されている。この反射層１４３は、開口部１４２に対向して開口部１４２上を覆うように形成される。なお、開口部１４２に対向する位置に配線１３１が形成されている場合には、その配線１３１と絶縁性が確保できる間隔、例えば０．２μｍ程度の間隔を置いて形成される。したがって、上記反射層１４３は上記配線層１３０の配線１３１間に上記配線１３１と間隔を置いて形成されている。
【００３８】
上記反射膜１４０、反射層１４３には、アルミニウム（Ａｌ）膜、酸化アルミニウム膜を用いることができる。特にアルミニウム膜は、可視光線に対しておよそ９０％以上の表面反射率を得ることができる。したがって、上記反射膜１４０、反射層１４３にアルミニウム膜を採用することが好ましい。一方、銅膜は、赤色光に対しておよそ９６％以上の表面反射率を得ることができるので、赤色光を反射させる上記配線１３１、反射層１４３は

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銅で形成することも好ましい。

【００３９】

このように、固体撮像素子２では、赤（Ｒｅｄ）画素部の上記反射膜１４０の構成が異なるのみで、その他の構成は前記固体撮像素子１と同様である。

【００４０】

上記固体撮像素子２が受光する入射光Ｌは、上記カラーフィルター１５０を透過して光電変換素子１１１に入る。例えば、上記カラーフィルター１５０が青（Ｂ）、緑（Ｇ）、赤（Ｒ）の３色（例えば光の３原色）で形成されている場合には、カラーフィルター１５０を透過して上記光電変換素子１１１が受光する入射光Ｌは、上記光電変換素子１１１の厚さが７μｍ～１６μｍに形成されていることから、青色フィルタを透過した青色光ＬＢは波長が短いため光電変換素子１１１の入射側近傍でほぼ１００％吸収されて光電変換されるため、反射膜１４０に達するような透過光とはなり得ない。緑色フィルタを透過した緑色光ＬＧは光電変換素子１１１内で大部分が吸収されるが、一部は透過成分となっている。しかしながら、反射膜１４０によって反射され、再び光電変換素子１１１に戻されるので、光電変換素子１１１においてほとんど吸収されることになる。一方、赤色フィルタを透過した赤色光ＬＲは光電変換素子１１１を一部は透過する。そのため、光電変換素子１１１で光電変換される赤色光ＬＲの光量が他の色よりも少なくなっていた。しかしながら、上記反射層１４３が設けられていることから、光電変換素子１１１を透過した赤色光ＬＲは反射膜１４３によって反射され、再び光電変換素子１１１に入射される。このため、赤色光ＬＲの光電変換量が他の色の光電変換量とほぼ同等となり、感度の低下を防止することができる。

【００４１】

また、赤（Ｒｅｄ）画素に入射する光の成分は、ほとんどが光電変換素子１１１を透過する波長の長い光である。一方、緑（Ｇｒｅｅｎ）画素に入射する光は波長が５００ｎｍ～５５０ｎｍをピークとして、６００ｎｍでは３０％以下の光強度でしかなく、光電変換素子１１１を透過する成分は少ない。青（Ｂｌｕｅ）画素は、先に説明したように、７μｍの光電変換素子１１１を透過する光の成分はない。つまり、反射膜１４０で反射した光が隣接画素の光電変換素子１１１に入射して混色を起こす影響度は、圧倒的に赤（Ｒｅｄ）画素に入射した光の成分が大きく、赤（Ｒｅｄ）画素に入射した光の反射膜１４０での反射光が緑（Ｇｒｅｅｎ）、青（Ｂｌｕｅ）の画素のフォトダイオードに入射しないようにすれば良い。上記固体撮像素子２では、反射層１４３の反射面に斜めに入射した光が隣接画素に入射するような角度で反射したとしても、その反射光は、緑（Ｇｒｅｅｎ）、青（Ｂｌｕｅ）画素上に形成された反射膜１４０で反射され配線層１３０側へと抜けていくので、緑（Ｇｒｅｅｎ）、青（Ｂｌｕｅ）の画素における赤（Ｒｅｄ）画素を透過してきた波長の長い成分の光の混色を防止することができ、良好な画質を得ることができる。

【００４２】

また、上記反射層１４３は、赤色の光を反射するものであれば良い場合で、配線層１３０の配線１３１が通常の半導体装置の配線材料に用いられるアルミニウム、銅等の金属で形成される場合には、配線１３１と同一工程で形成することができるという利点がある。これにより、反射層１４３を作製する工程を新たに設ける必要がなくなるので、プロセス負荷をかけることなく反射層１４３を形成することができる。

【００４３】

次に、本発明の固体撮像素子に係る実施の形態の一例（第３例）を、図５の概略構成断面図によって説明する。

【００４４】

図５に示すように、本発明の固体撮像素子３は、半導体層で構成される素子層１１０に光電変換素子（例えばフォトダイオード）１１１が形成され、この光電変換素子１１１で光電変換された信号電荷を電気信号に変換して出力する能動素子（図示せず）を含む複数の単位画素が配列されたものであり、上記光電変換素子１１１が形成される素子層１１０に対してその一方の面側に、上記能動素子に対して配線をなす配線層１３０を備えている

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。上記光電変換素子１１１は、例えば５μｍ～１５μｍの厚さのシリコン層で形成されている。また、入射光Ｌを素子層１１０の他方の面側にはカラーフィルター１５０が形成されている。また、上記素子層１１０の配線層１３０側には、上記能動素子のうちの光電変換された信号電荷を読み出す読み出しトランジスタ１２０を構成する読み出しゲート電極１２１が絶縁膜１２２を介して形成されている。この読み出しゲート電極１２１は、例えば多結晶シリコンで形成されている。このため、読み出しゲート電極１２１は光透過性を有する。

【００４５】

上記読み出しゲート電極１２１を含む、画素の全面には絶縁膜１４１を介して被覆するように反射膜１４０が形成されている。ただし、緑（Ｇｒｅｅｎ）画素および青（Ｂｌｕｅ）画素の全面は反射膜１４０が形成されているが、カラーフィルター１５０を透過する赤色光が入射される光電変換素子１１１に対向する位置の上記反射膜１４０には開口部１４２が形成されている。さらに、上記開口部１４２の上記配線層１３０側に反射層１４３が形成されている。この反射層１４３は、開口部１４２に対向して開口部１４２上を覆うように形成される。上記反射層１４３は上記素子層１１０と上記配線層１３０との間に絶縁膜１４４を介して形成されている。

【００４６】

上記反射膜１４０、反射層１４３には、アルミニウム（Ａｌ）膜、酸化アルミニウム膜を用いることができる。特にアルミニウム膜は、可視光線に対しておよそ９０％以上の表面反射率を得ることができる。したがって、上記反射膜１４０、反射層１４３にアルミニウム膜を採用することが好ましい。一方、銅膜は、赤色光に対しておよそ９６％以上の表面反射率を得ることができるので、赤色光を反射させる上記配線１３１、反射層１４３は銅で形成することも好ましい。

【００４７】

このように、固体撮像素子３では、赤（Ｒｅｄ）画素部の上記反射膜１４０の構成が異なるのみで、その他の構成は前記固体撮像素子１と同様である。

【００４８】

上記固体撮像素子３が受光する入射光Ｌは、上記カラーフィルター１５０を透過して光電変換素子１１１に入る。例えば、上記カラーフィルター１５０が青（Ｂ）、緑（Ｇ）、赤（Ｒ）の３色（例えば光の３原色）で形成されている場合には、カラーフィルター１５０を透過して上記光電変換素子１１１が受光する入射光Ｌは、上記光電変換素子１１１の厚さが５μｍ～１５μｍに形成されていることから、青色フィルタを透過した青色光ＬＢは波長が短いため光電変換素子１１１の入射側近傍でほぼ１００％吸収されて光電変換されるため、反射膜１４０に達するような透過光とはなり得ない。緑色フィルタを透過した緑色光ＬＧは光電変換素子１１１内で大部分が吸収されるか、一部は透過成分となっている。しかしながら、反射膜１４０によって反射され、再び光電変換素子１１１に戻されるので、光電変換素子１１１においてほとんど吸収されることになる。一方、赤色光ＬＲは光電変換素子１１１を一部は透過する。そのため、光電変換素子１１１で光電変換される赤色光ＬＲの光量が他の色よりも少なくなっていた。しかしながら、上記反射層１４３が設けられていることから、光電変換素子１１１を透過した赤色光ＬＲは反射層１４３によって反射され、再び光電変換素子１１１に入射される。このため、赤色光ＬＲの光電変換量が他の色の光電変換量とほぼ同等となり、感度の低下を防止することができる。

【００４９】

また、上記固体撮像素子３では、反射層１４３の反射面に斜めに入射した光が隣接画素に入射するような角度で反射したとしても、その反射光は、緑（Ｇｒｅｅｎ）、青（Ｂｌｕｅ）画素上に形成された反射膜１４０で反射され配線層１３０側へと抜けていくので、緑（Ｇｒｅｅｎ）、青（Ｂｌｕｅ）の画素における赤（Ｒｅｄ）画素を透過してきた波長の長い成分の光の混色を防止することができ、良好な画質を得ることができる。

【００５０】

次に、本発明の固体撮像素子の製造方法に係る実施の形態の一例（第１例）を、図６～

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図１０の製造工程断面図によって説明する。

【００５１】

図示はしないが、基板を用意する。この基板は、第１導電型（Ｎ型）シリコン基板からなり、１００Ω・ｃｍ～５００Ω・ｃｍ程度のシート抵抗を有するものを用いた。次に、例えばエピタキシャル成長法によって、上記基板上にＰ⁻型の半導体層２１１として、例えばＰ⁻型のシリコン層を形成する。

【００５２】

次に、上記半導体層２１１表層の所定位置にＰ⁺型領域からなるチャネルストップ領域を形成する。このチャネルストップ領域はイオン注入により形成することができる。次に、上記半導体層２１１表層の所定位置に上記チャネルストップ領域に隣接して、垂直電荷転送部が形成される領域にＰ型領域からなるウエル領域を形成する。上記半導体層２１１表層の所定位置に上記チャネルストップ領域に隣接して、上記ウエル領域上層に垂直電荷転送部のＮ型領域を形成する。

【００５３】

次に、図６（１）に示すように、上記半導体層２１１上の垂直電荷転送部上および読み出し部となる領域上に、絶縁膜１２２を介して読み出しゲート電極（転送電極も含む）１２１を形成する。この読み出しゲート電極１２１は、チャネルストップ領域上にオーバラップするように形成されてよい。上記電極形成は、例えば、半導体層２１１表面に絶縁膜１２２を形成した後、電極形成膜としてポリシリコン膜を成膜する。その後、通常のレジストマスクを用いたエッチング技術によりポリシリコン膜を読み出しゲート電極１２１にパターニングして形成することができる。

【００５４】

次に、図６（２）に示すように、上記半導体層２１１表層の上記読み出しゲート電極１２１が形成された読み出し部に隣接して、光電変換素子１１１のＮ型領域を形成する。この光電変換素子１１１のＮ型領域はイオン注入により形成することができる。次いで、上記光電変換素子１１１のＮ型領域表層にＰ⁺型領域からなるホール蓄積層を形成する。このホール蓄積層はイオン注入により形成することができる。

【００５５】

次に、図７（３）に示すように、全面に上記読み出しゲート電極１２１を被覆するように絶縁膜１４１を形成した後、全面に反射膜１４０を形成する。上記絶縁膜１４１は、例えば、ＣＶＤ法によって、酸化シリコンを数１０ｎｍの厚さに堆積して形成される。また上記反射膜１４０は、アルミニウム、酸化アルミニウム等を、例えば、ＣＶＤ法、スパッタリング法などによって堆積して成膜される。その後、通常のレジスト塗布技術、リソグラフィー技術等によって画素領域を被覆するレジストマスクを形成した後、マスク以外の領域の反射膜１４０を除去する。その後、上記レジストマスクを除去する。

【００５６】

上記反射膜１４０は、特に、可視光線に対しておよそ９０％以上の表面反射率を得ることができるアルミニウム膜で形成することが好ましい。また、前記図２によって説明したように、反射膜１４０にアルミニウム膜を用いた場合には、その膜厚は３０ｎｍ以上あればよい。また、反射させる光の波長が緑色光、赤色光であることを考慮すると、緑色光、赤色光の表面反射率が９５％以上を有する膜を用いることも可能である。

【００５７】

次に、図示はしないが、通常のＣＭＯＳ・ＬＳＩプロセスにより固体撮像素子の周辺回路領域の素子を形成した後、図８（４）に示すように、通常の多層配線の形成技術により、素子層１１０上に複数層の配線１３１を形成し、配線層１３０を成す。さらに、図示はしないが、配線層１３０側に支持基板を形成してもよい。

【００５８】

次に、基板（図示せず）側を研磨により除去、平坦化し、図９（５）に示すように、裏面を光電変換素子１１１近傍まで研磨する。光電変換素子１１１側には、半導体層２１１を例えば３．５μｍ～７μｍ程度残す。

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【００５９】
最後に、図１０（６）に示すように、裏面側にカラーフィルター１５０を形成し、さらに図示はしないがオンチップレンズなどを通常の表面型イメージセンサと同様の方法により形成することにより、前記図１等により説明した固体撮像素子１が完成する。
【００６０】
上記固体撮像素子の製造方法は、半導体層２１１の配線層１３０が形成される側に、絶縁膜１４１を介して読み出しゲート電極１２１を含む画素全面を被覆するように反射膜１４０を形成する工程を備えているため、光電変換素子１１１で完全に吸収されずに一部透過された長波長の光（例えば赤色光）を反射膜１４０によって長波長の光を光電変換する光電変換素子１１１に戻すようにすることができるので、光電変換素子１１１に入射した光を効率的に光電変換できるようになるという利点がある。また、反射膜１４０が配線層１３０の配線１３１による反射を防止するので、反射光が隣接する画素へ入射されなくなり、混色を防止することができるという利点がある。
【００６１】
次に、本発明の固体撮像素子の製造方法に係る実施の形態の一例（第２例）を、図１１～図１５の製造工程断面図によって説明する。
【００６２】
図示はしないが、基板を用意する。この基板は、第１導電型（Ｎ型）シリコン基板からなり、１０Ω・ｃｍ～５０Ω・ｃｍ程度のシート抵抗を有するものを用いた。次に、例えばエピタキシャル成長法によって、上記基板上にＰ－型の半導体層２１１として、例えばＰ－型のシリコン層を形成する。
【００６３】
次に、上記半導体層２１１表層の所定位置にＰ＋型領域からなるチャネルストップ領域を形成する。このチャネルストップ領域はイオン注入により形成することができる。次に、上記半導体層２１１表層の所定位置に上記チャネルストップ領域に隣接して、垂直電荷転送部が形成される領域にＰ型領域からなるウエル領域を形成する。上記半導体層２１１表層の所定位置に上記チャネルストップ領域に隣接して、上記ウエル領域上層に垂直電荷転送部のＮ型領域を形成する。
【００６４】
次に、図１１（１）に示すように、上記半導体層２１１上の垂直電荷転送部上および読み出し部となる領域上に、絶縁膜１２２を介して読み出しゲート電極（転送電極も含む）１２１を形成する。この読み出しゲート電極１２１は、チャネルストップ領域上にオーバラップするように形成されてよい。上記電極形成は、例えば、半導体層２１１表面に絶縁膜１２２を形成した後、電極形成膜としてポリシリコン膜を成膜する。その後、通常のレジストマスクを用いたエッチング技術によりポリシリコン膜を読み出しゲート電極１２１にパターニングして形成することができる。
【００６５】
次に、図１１（２）に示すように、上記半導体層２１１表層の上記読み出しゲート電極１２１が形成された読み出し部に隣接して、光電変換素子１１１のＮ型領域を形成する。この光電変換素子１１１のＮ型領域はイオン注入により形成することができる。次いで、上記光電変換素子１１１のＮ型領域表層にＰ＋型領域からなるホール蓄積層を形成する。このホール蓄積層はイオン注入により形成することができる。
【００６６】
次に、図１２（３）に示すように、全面に上記読み出しゲート電極１２１を被覆するように絶縁膜１４１を形成した後、全面に反射膜１４０を形成する。上記絶縁膜１４１は、例えば、ＣＶＤ法によって、酸化シリコンを約１０ｎｍの厚さに堆積して形成される。また上記反射膜１４０は、アルミニウム、酸化アルミニウム等を、例えば、ＣＶＤ法、スパッタリング法などによって堆積して成膜される。
【００６７】
上記反射膜１４０は、特に、可視光線に対しておよそ９０％以上の表面反射率を得るこ

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とができるアルミニウム膜で形成することが好ましい。また、前記図２によって説明したように、反射膜１４０にアルミニウム膜を用いた場合には、その膜厚は３０ｎｍ以上あればよい。また、反射させる光の波長が緑色光、赤色光であることを考慮すると、緑色光、赤色光の表面反射率が９５％以上を有する銀を用いることも可能である。

【００６８】

その後、図１２（４）に示すように、通常のレジスト塗布技術、リソグラフィー技術等によって波長の短い青色の画素領域および緑色の画素領域を被覆するレジストマスクを形成した後、マスク以外の領域の反射膜１４０を除去する。したがって、赤色の画素領域の反射膜１４０は除去され、開口部１４２が形成されるとともに、図示はしていないが周辺回路領域の反射膜１４０も除去される。その後、上記レジストマスクを除去する。

【００６９】

次に、図示はしないが、通常のＣＭＯＳ・ＬＳＩプロセスにより固体撮像素子の周辺回路領域の素子を形成した後、図１３（５）に示すように、通常の多層配線の形成技術により、素子層１１０上に複数層の配線１３１を形成し、配線層１３０を成す。その際、例えば最下層の配線１３１を形成する際に、上記赤色の画素領域上に、反射層１４３を形成する。この反射層１４３は、開口部１４２に対向して開口部１４２上を覆うように形成される。なお、開口部１４２に対向する位置に配線１３１が形成されている場合には、その配線１３１と絶縁性が確保でき、配線１３１と遮光層１４３との間を赤色光が漏れないような間隔、例えば０．４μｍ～０．２μｍ程度の間隔を設いて形成される。したがって、上記反射層１４３は上記配線層１３０の配線１３１間に上記配線１３１と間隔を置いて形成される。

【００７０】

上記反射膜１４０、反射層１４３には、アルミニウム（Ａｌ）膜、酸化アルミニウム膜を用いることができる。特にアルミニウム膜は、可視光線に対しておよそ９０％以上の表面反射率を得ることができる。したがって、上記反射膜１４０、反射層１４３にアルミニウム膜を採用することが好ましい。一方、銅膜は、赤色光に対しておよそ９６％以上の表面反射率を得ることができるので、赤色光を反射させる上記配線１３１、反射層１４３は銅で形成することも好ましい。このように、上記反射層１４３は、配線１３１が銅で形成されるならば銅で形成し、アルミニウムで形成されるならばアルミニウムで形成することにより、配線１３１と同一プロセスで形成することが可能になる。さらに、図示はしないが、配線層１３０側に支持基板を形成してもよい。

【００７１】

次に、基板（図示せず）側を研磨により除去、平坦化し、図１４（６）に示すように、裏面を光電変換素子１１１近傍まで研磨する。光電変換素子１１１側には、半導体層２１１を例えば３．５μｍ～７μｍ程度残す。

【００７２】

最後に、図１５（７）に示すように、裏面側にカラーフィルター１５０を形成し、さらに図示はしないかオンチップレンズなどを通常の表面型イメージセンサと同様の方法により形成することにより、前記図１等により説明した固体撮像素子２が完成する。

【００７３】

上記固体撮像素子２の製造方法では、青色光は波長が短いため光電変換素子１１１の入射側近傍でほぼ１００％吸収されて光電変換されるため、反射膜１４０に達するような透過光とはなり得ない。緑色光は光電変換素子１１１内で大部分が吸収されるが、一部は透過成分となっている。しかしながら、反射膜１４０によって反射され、再び光電変換素子１１１に戻されるので、光電変換素子１１１においてほとんど吸収されることになる。一方、赤色光は光電変換素子１１１を一部は透過する。そのため、光電変換素子１１１で光電変換される赤色光の光量が他の色よりも少なくなるが、上記反射層１４３が設けられていることから、光電変換素子１１１を透過した赤色光は反射層１４３によって反射され、再び光電変換素子１１１に入射される。このため、赤色光の光電変換量が他の色の光電変換量とほぼ同等となり、感度の低下を防止することができる。

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【００７４】
また、反射層１４３の反射面に斜めに入射した光が隣接画素に入射するような角度で反射したとしても、その反射光は、緑（Ｇｒｅｅｎ）、青（Ｂｌｕｅ）画素上に形成された反射膜１４０で反射され配線層１３０側へと抜けていくので、緑（Ｇｒｅｅｎ）、青（Ｂｌｕｅ）の画素における赤（Ｒｅｄ）画素を透過してきた波長の長い成分の光の混色を防止することができ、良好な画質を得ることができる。
【００７５】
また、上記反射層１４３は、赤色の光を反射するものであれば良い場合で、配線層１３０の配線１３１が通常の半導体装置の配線材料に用いられるアルミニウム、銅等の金属で形成される場合には、配線１３１と同一工程で形成することができるという利点がある。これにより、反射層１４３を作製する工程を新たに設ける必要がなくなるので、プロセス負荷をかけることなく反射層１４３を形成することができる。
【００７６】
上記製造方法では、反射層１４３を配線１３１側に設けた場合を説明したが、実施の形態の第３例として、上記反射層１４３は配線１３１とは別層で形成することも可能である。この場合、前記図５のような構成となる。すなわち、前記図１２によって説明したのと同様に、上記読み出しゲート電極１２１を含む、画素の全面には絶縁膜１４１を介して被覆するように反射膜１４０を形成する。ただし、緑（Ｇｒｅｅｎ）画素および青（Ｂｌｕｅ）画素の全面は反射膜１４０を形成し、赤色光が入射される光電変換素子１１１に対向する位置の上記反射膜１４０には開口部１４２を形成する。
【００７７】
次に、図１６に示すように、素子層１１０側に読み出しゲート電極１２１、反射膜１４０等を覆う絶縁膜１４４を形成する。その後、絶縁膜１４４上に反射層１４３を成膜した後、通常のエッチングマスクの形成技術、エッチング技術（例えば異方性ドライエッチング）により、開口部１４２に対向して開口部１４２上を覆うように反射層１４３を残すパターニングを行う。例えば反射層１４３は、赤（Ｒｅｄ）画素の読み出しゲート電極１２１などを除いた光電変換素子１１１の開口形状と同じでよい。その後、エッチングマスクを除去する。
【００７８】
上記反射膜１４０、反射層１４３には、アルミニウム（Ａｌ）膜、酸化アルミニウム膜を用いることができる。特にアルミニウム膜は、可視光線に対しておよそ９０％以上の表面反射率を得ることができる。したがって、上記反射膜１４０、反射層１４３にアルミニウム膜を採用することが好ましい。一方、銅膜は、赤色光に対しておよそ９６％以上の表面反射率を得ることができるので、赤色光を反射させる上記反射層１４３は銅で形成することも好ましい。
【００７９】
その後は、通常の多層配線の形成技術により、素子層１１０上に複数層の配線１３１を形成し、配線層１３０を成す。
【００８０】
次に、基板（図示せず）側を研磨により除去、平坦化し、裏面を光電変換素子１１１近傍まで研磨する。光電変換素子１１１側には、半導体層２１１を例えば３．５μｍ～７μｍ程度残す。
【００８１】
最後に、最前側にカラーフィルター１５０を形成し、さらに図示はしないがオンチップレンズなどを通常の表面型イメージセンサと同様の方法により形成することにより、前記図５により説明した固体撮像素子３が完成する。
【００８２】
上記固体撮像素子３の製造方法では、青色光は波長が短いため光電変換素子１１１の入射側近傍でほぼ１００％吸収されて光電変換されるため、反射膜１４０に達するような透過光とはなり得ない。緑色光は光電変換素子１１１内で大部分が吸収されるか、一部は透

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過成分となっている。しかしながら、反射膜１４０によって反射され、再び光電変換素子１１１に戻されるので、光電変換素子１１１においてほとんど吸収されることになる。一方、赤色光は光電変換素子１１１を一部は透過する。そのため、光電変換素子１１１で光電変換される赤色光の光量が他の色よりも少なくなるが、上記反射層１４３が設けられていることから、光電変換素子１１１を透過した赤色光は反射層１４３によって反射され、再び光電変換素子１１１に入射される。このため、赤色光の光電変換量が他の色の光電変換量とほぼ同等となり、感度の低下を防止することができる。

【００８３】

また、反射層１４３の反射面に斜めに入射した光が隣接画素に入射するような角度で反射したとしても、その反射光は、緑（Ｇｒｅｅｎ）、青（Ｂｌｕｅ）画素上に形成された反射膜１４０で反射され配線層１３０側へと抜けていくので、緑（Ｇｒｅｅｎ）、青（Ｂｌｕｅ）の画素における赤（Ｒｅｄ）画素を透過してきた波長の長い成分の光の混色を防止することができ、良好な画質を得ることができる。

【００８４】

次に、本発明の画像撮影装置に係る一実施例を、図１７のブロック図によって説明する。

【００８５】

図１７に示すように、画像撮影装置５００は、固体撮像素子５１０を備えている。この固体撮像素子５１０の集光側には像を結像させる結像光学系５２０が備えられ、また、固体撮像素子５１０には、それを駆動する駆動回路５３０が接続されている。そして固体撮像素子５１０で光電変換された信号を画像に処理する信号処理回路５４０が接続されている。上記信号処理回路５４０によって処理された画像信号は画像記憶部５５０によって記憶される。このような画像撮影装置５００において、上記固体撮像素子５１０には、前記実施の形態の第１例、第２例、第３例で説明した固体撮像素子１、２、３のうちのいずれかを用いることができる。

【００８６】

本発明の画像撮影装置５００は、本発明の固体撮像素子１もしくは固体撮像素子２もしくは固体撮像素子３を撮像素子に用いているため、疑色がないので色再現性に優れた画像を得ることができ、しかも高感度な画像を得ることができるという利点がある。

【００８７】

なお、本発明の画像撮影装置５００は、上記構成に限定されることはなく、固体撮像素子を用いる画像撮影装置であれば如何なる構成のものにも適用することができる。

【図面の簡単な説明】

【００８８】

【図１】本発明の固体撮像素子に係る一実施の形態例（第１例）を示した概略構成断面図である。

【図２】反射膜の膜厚をパラメータとした透過率、反射率と入射光の波長との関係図である。

【図３】本発明の固体撮像素子が適用されるＣＭＯＳセンサに係る一実施の形態例を示した概略構成断面図である。

【図４】本発明の固体撮像素子に係る一実施の形態例（第２例）を示した概略構成断面図である。

【図５】本発明の固体撮像素子に係る一実施の形態例（第３例）を示した概略構成断面図である。

【図６】本発明の固体撮像素子の製造方法に係る一実施の形態例（第１例）を示した製造工程断面図である。

【図７】本発明の固体撮像素子の製造方法に係る一実施の形態例（第１例）を示した製造工程断面図である。

【図８】本発明の固体撮像素子の製造方法に係る一実施の形態例（第１例）を示した製造工程断面図である。

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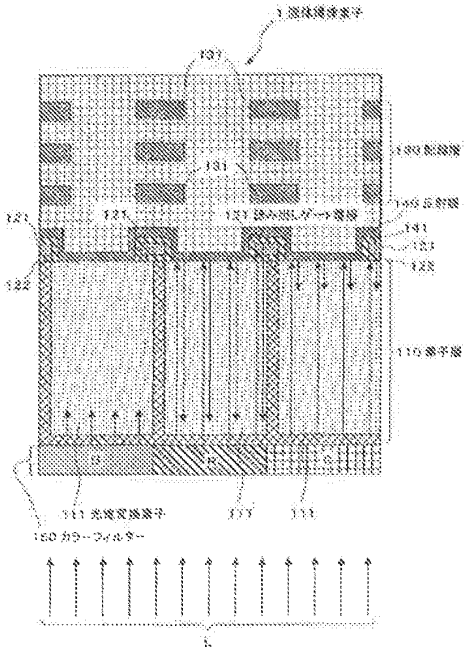
【図９】本発明の固体撮像素子の製造方法に係る一実施の形態例（第１例）を示した製造工程断面図である。
【図１０】本発明の固体撮像素子の製造方法に係る一実施の形態例（第１例）を示した製造工程断面図である。
【図１１】本発明の固体撮像素子の製造方法に係る一実施の形態例（第２例）を示した製造工程断面図である。
【図１２】本発明の固体撮像素子の製造方法に係る一実施の形態例（第２例）を示した製造工程断面図である。
【図１３】本発明の固体撮像素子の製造方法に係る一実施の形態例（第２例）を示した製造工程断面図である。
【図１４】本発明の固体撮像素子の製造方法に係る一実施の形態例（第２例）を示した製造工程断面図である。
【図１５】本発明の固体撮像素子の製造方法に係る一実施の形態例（第２例）を示した製造工程断面図である。
【図１６】本発明の固体撮像素子の製造方法に係る一実施の形態例（第３例）を示した製造工程断面図である。
【図１７】画像撮影装置に係る一実施の形態例を示したブロック図である。
【図１８】従来の固体撮像素子に係る一例を示した概略構成斜視図である。
【図１９】従来の固体撮像素子に係る問題点を示した概略構成断面図である。
【符号の説明】
【００６９】
１…固体撮像素子、１１０…素子層、１１１…光電変換素子、１２１…読み出しゲート電極、１３０…配線層、１３１…配線、１４０…反射膜、１４１…絶縁膜

【図１】



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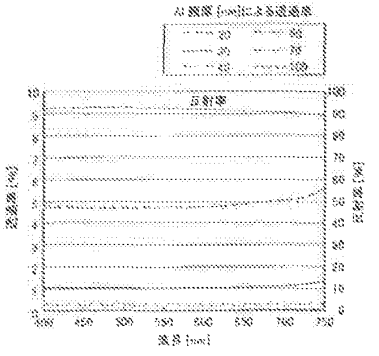

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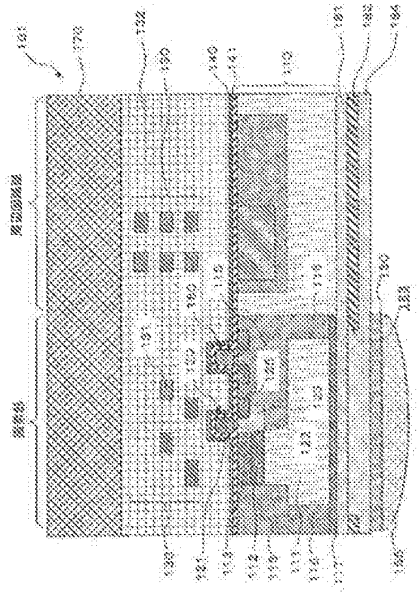
【図３】



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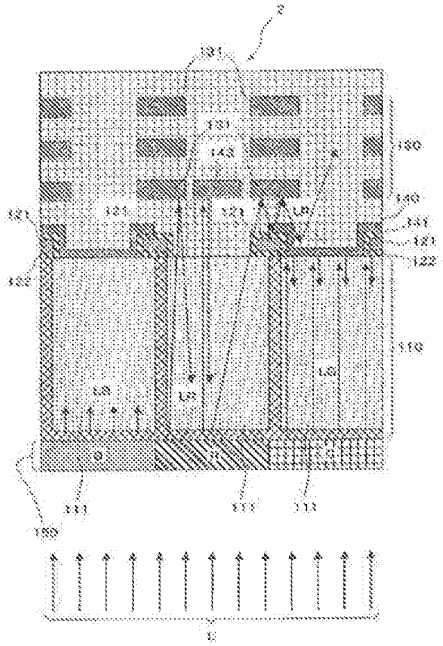

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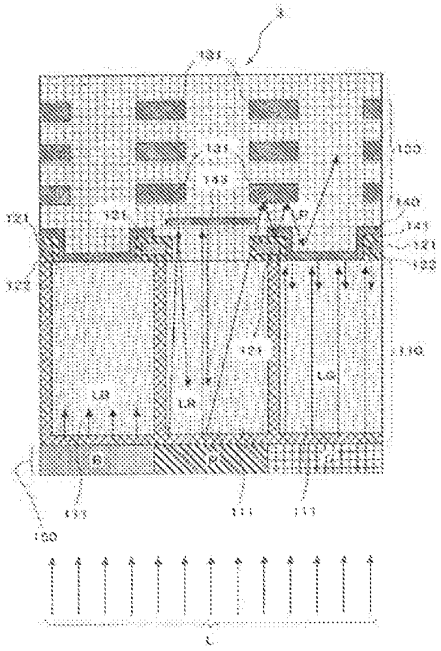

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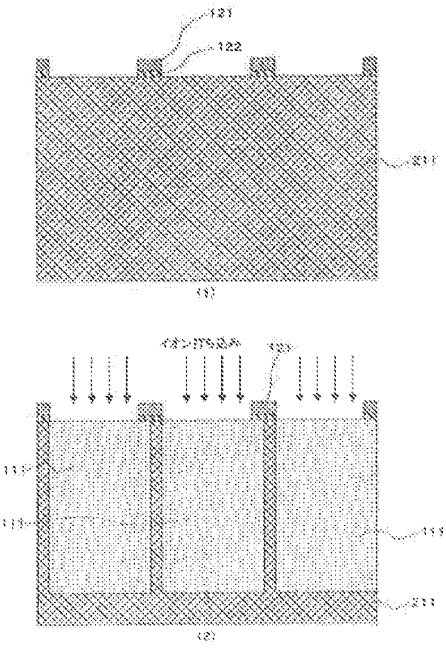

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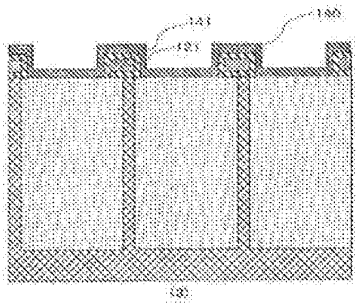

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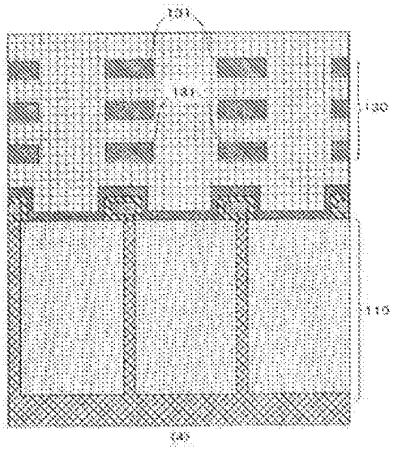

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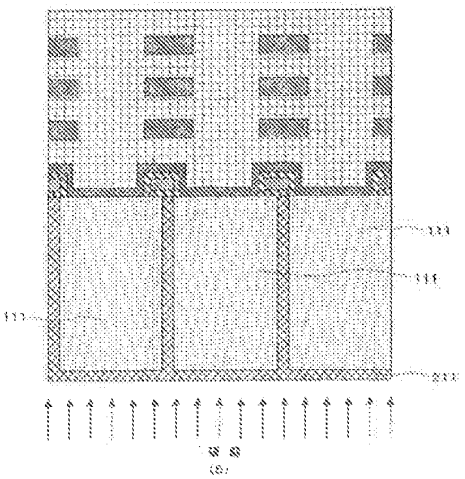
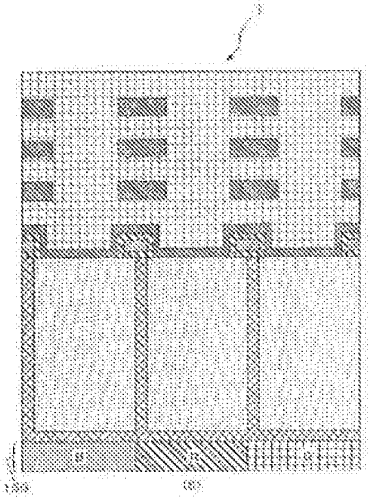
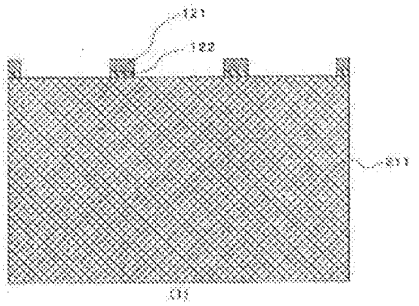


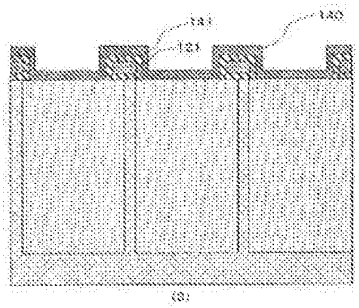
【図１０】

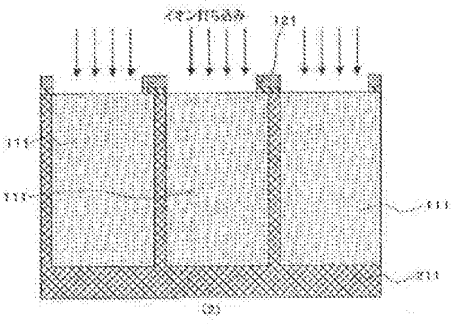


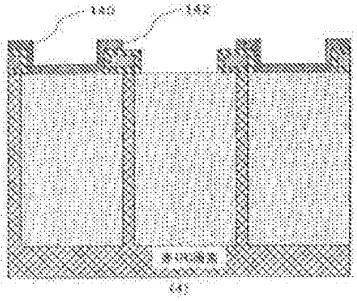
【図１１】



【図１２】







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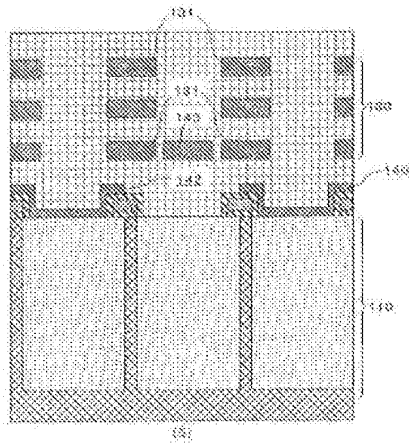

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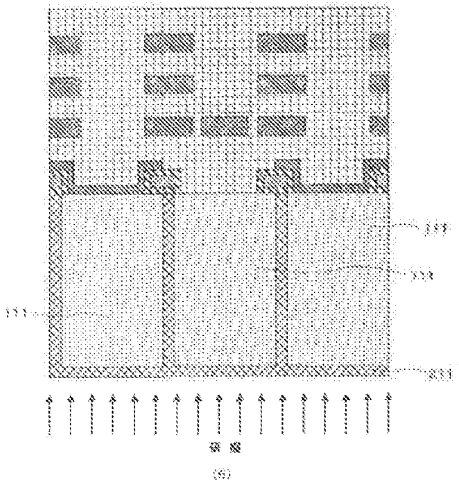

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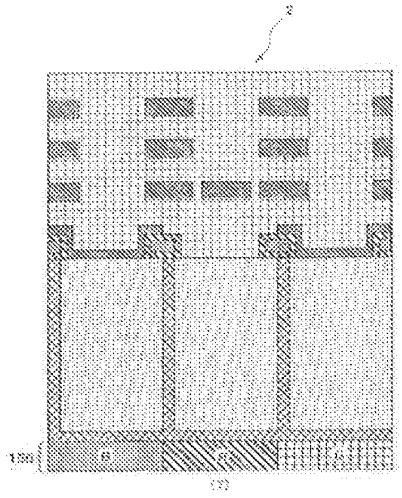
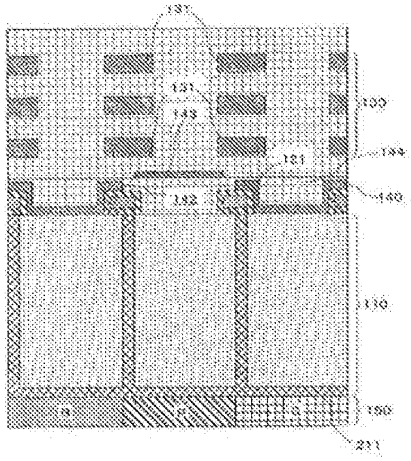
【図１５】



【図１６】



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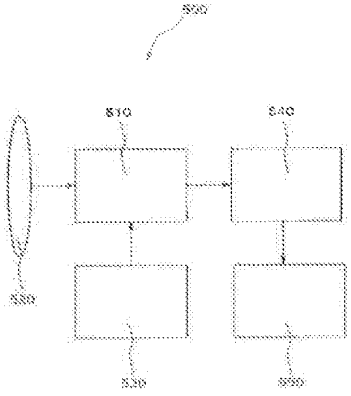

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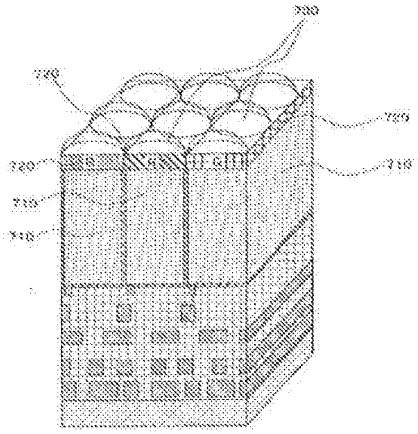
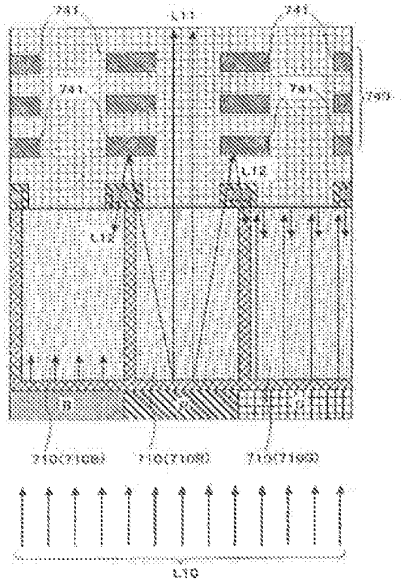


【図１９】



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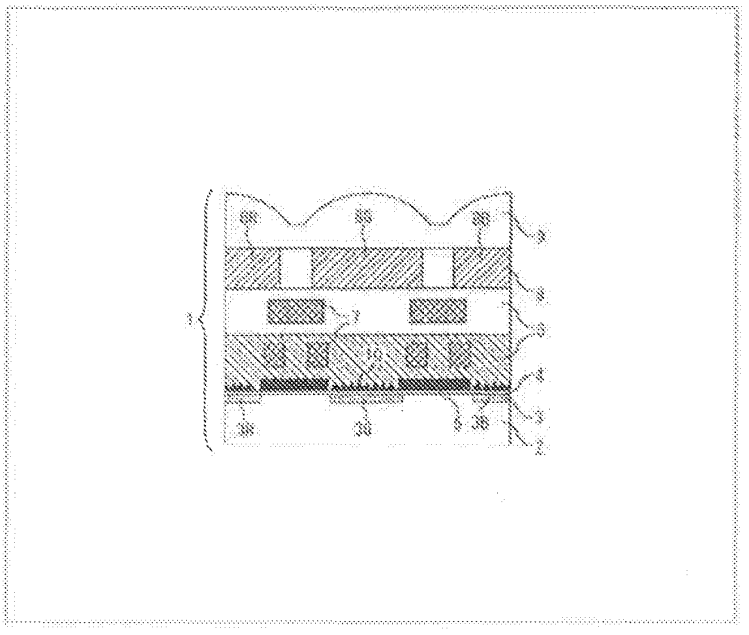
(21)Application number	2004-338726
(22)Date of filing	24.11.2004
(71)Applicant	CANON INC
(72)Inventor	OKUNO TAKEHARU

(54)SOLID STATE IMAGE SENSOR, AND OPTICAL APPLIANCE HAVING THE SAME

(57)Abstract

PROBLEM TO BE SOLVED: To obtain a highly sensitive solid state image sensor wherein the reflection of a light is so reduced in the interface between its photoelectric converting portion and its insulating film as to suppress the generation of such a noise light as flare and ghost. SOLUTION: The solid state image sensor is the one wherein photoelectric converting elements for generating charges in response to the intensity of an incident light on a silicon substrate are formed. Each fine irregular structure is formed on the incident-light side of each photoelectric converting element via an insulating film comprising a silicon oxide film.



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[Claim(s)]
[Claim 1]
It is a solid state image pickup device in which a photoelectric conversion part which generates an electric charge according to luminous intensity which entered into a substrate was formed, A solid state image pickup device having a rugged structure object via a thin film in the light incidence side of the optoelectric transducer.
[Claim 2]
The solid state image pickup device according to claim 1 with which the aforementioned thin film is characterized by thickness being 10A or more and 500A or less.
[Claim 3]
The solid state image pickup device according to claim 1 or 2, wherein the aforementioned thin film is a silicon oxide film.
[Claim 4]
A solid state image pickup device of a description in any 1 item of Claim 1, wherein the aforementioned photoelectric conversion part is formed with silicon to 3.
[Claim 5]
A solid state image pickup device of a description in any 1 item of Claim 1 which the aforementioned rugged structure object arranges a plurality of uneven parts in two dimensions, is constituted, and is characterized by the uneven part being form which the volume share increases from the light incidence side gradually toward the aforementioned photoelectric conversion part side to 4.
[Claim 6]
A solid state image pickup device of a description in any 1 item of Claim 1 which the aforementioned rugged structure object arranges a plurality of uneven parts in two dimensions, is constituted, and is characterized by the uneven part being approximately quadrangular pyramid form, approximately conical shape, substantially trapezoidal quadrangular pyramid form, or substantially trapezoidal conical shape to 5.
[Claim 7]
A solid state image pickup device of a description to any one of the Claims 1-6, wherein height of the rugged structure object is 100A or more and 5000A or less.
[Claim 8]
A solid state image pickup device of a description in any 1 item of Claim 1, wherein the aforementioned rugged structure object is made from single crystal silicon, polycrystalline silicon, or an amorphous silicon to 7.
[Claim 9]
It has the aforementioned rugged structure object and a color filter of a plurality of kinds in the a plurality of photoelectric conversion part [which were formed in the aforementioned substrate], and light incidence side of each photoelectric conversion part,

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A solid state image pickup device of a description in any 1 item of Claim 1, wherein height or/and a pitch of the uneven part differ from each other according to a kind of color filter to 8.

[Claim 10]

A solid state image pickup device of an any 1 item description of nine from Claim 1

A ****(ing) optical instrument.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[Field of the Invention]
[0001]
The present invention is suitable to optical instruments with the solid state image pickup device of the high sensitivity which was related with solid state image pickup devices, such as CMOS and CCD, and inhibited especially deterioration of the sensitivity of a light-receiving part, such as a digital camera, a video camera, and an electronic "still" camera.
[Background of the Invention]
[0002]
The solid state image pickup device represented by CMOS and CCD in recent years, In order for multi pixel-ization to proceed in order to acquire a high brilliance image, and to mount on what is called mobile terminals, such as a mobile phone and PDA, the miniaturization was called for, the area of per stroke matter became very small by this, and there was a tendency for sensitivity to be deteriorated.
[0003]
With the optoelectric transducer (photoelectric conversion part) formed with silicon when its attention was paid to the internal structure of a solid state image pickup device and the insulator layer formed on it, Since the rates of optical refraction differed largely, there was a tendency for the light beyond about 20% or it of incident light to be reflected as a whole from each interface, and for sensitivity to be deteriorated.
[0004]
The light again reflected by another part and the component is the cause which noise light, such as the flare and a ghost, generates by the incident thing at the photoelectric conversion part.
[0005]
An antireflection means is provided to the front side (light incidence side) of a photoelectric conversion part (light-receiving part), and the solid state image pickup device which lessened deterioration of light-receiving sensitivity is known (a Patent document 1, 2).
[Patent document 1] Japanese Published Patent Application No. 2000-12822 (JP2000-12822A)
[Patent document 2] Japanese Published Patent Application No. 2003-249639 (JP2003-249639A)
[Description of the Invention]
[Problem to be solved by the invention]
[0006]
A Patent document 1 is forming the antireflection film which changes from a silicon nitride film about 60 nm thick via the gate oxide film (insulator layer) which comprises 100-200-nm-thick SiO_2 on a light-receiving part (photoelectric conversion part), The MOS type solid state imaging device of the structure which inhibits a reflection of the light in a photoelectric conversion part

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(light-receiving part) is proposed.

[0007]

The MOS type solid state imaging device of a Patent document 1 in view of the refractive index for which an antireflection film is asked a silicon nitride film (refractive index 2.04 [about] in the wavelength of 550 nm), It is difficult to prevent completely a reflection of the interface of silicon (complex-index-of-refraction 4.08-0.04i in the wavelength of 550 nm), and a silicon oxide film (refractive index 1.46 in the wavelength of 550 nm).

[0008]

Even if the high antireflection effect is acquired to one specific wavelength corresponding to the thickness of the silicon nitride film in this composition, the antireflection effect is deteriorated to different wavelength and the reflected light which was not able to be inhibited serves as a generation cause of the flare or a ghost after all.

[0009]

A Patent document 2 is providing the uneven shape in which a refractive index carries out a monotone change to the interface of a photo-diode (photoelectric conversion part) and the insulator layer which consists of a silicon oxide film continuously, and preventing a reflection of light, While solving or eliminating the problem of deterioration of the sensitivity of the appearance resulting from a reflection, the solid state imaging device which solves or eliminated the problem of deterioration of the imaging performance resulting from a smear is proposed.

[0010]

When uneven shape is formed in the photo-diode surface by etching etc. as the solid state imaging device of the Patent document 2 is described there, generating of a noise may increase remarkably by generating of the plasma damage at the time of etching, or the lattice defect of silicon, entering of metallic contamination, etc.

[0011]

Even if it is able to etch by the method of a plasma damage, contamination, etc. twisting, according to a subsequent thermal process, a lattice defect arises in the stress by the difference of a coefficient of thermal expansion from a silicon oxide film, etc., it becomes a generation cause of a noise, and improvement in the degree of real textures is difficult.

[0012]

There are few reflected lights and the present invention aims at offer of the optical instrument which has high sensitivity solid state image pickup device and it which inhibited noise light, such as the flare and a ghost, while it improves the transmission quantity of the light to a photoelectric conversion part.

[Means for solving problem]

[0013]

the solid state image pickup device of the present invention is a solid state image pickup device in which the photoelectric conversion part which generates an electric charge according to the luminous intensity which entered into the substrate was formed -- it is characterized by having a rugged structure object via the thin film at the light incidence side of the optoelectric transducer.

[Effect of the Invention]

[0014]

According to the present invention, while improving the transmission quantity of the light to a photoelectric conversion part, there are few reflected lights and the optical instrument which has high sensitivity solid state image pickup device and it which inhibited noise light, such as the flare and a ghost, is obtained.

[Best Mode of Carrying Out the Invention]

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[0015]

[Work example 1]

[0016]

Fig.1 is an essential part cross sectional view of the solid state image pickup device of the working example 1 of the present invention.

[0017]

In Fig.1, the solid state image pickup device 1 is the photoelectric conversion part 3 (3R, 3G, 3B) of plurality [silicon substrate / 2]. It has the color filter 8 which has the gate oxide film (thin film) 4, the gate electrode 5, the interlayer insulation film 6, the metallic wiring 7, the red filter 8R, the green filter 8G, and the blue filter 8G which comprise the silicon oxide film as an insulator layer, and the micro lens 9. the photoelectric conversion part (photo-diode) 3 -- the upper (light incidence side) -- **** -- the fine rugged structure object 10 which has arranged a plurality of fine unevenness parts 10a which consist of single crystal silicon for antireflections in two dimensions is formed via the gate oxide film (thin film) 4 with a thickness of 50 A (5 nm) which consists of silicon oxide films.

[0018]

The solid state image pickup device 1 of the working example 1 is providing the fine rugged structure object 10 which uses silicon as main materials via the insulator layer 4 at the light incidence side of the photoelectric conversion part of the solid state image pickup device 1.

[0019]

It is an element which inhibits interface reflected light quantity by the fine rugged structure object 10 being called SWS (Sub Wave length Structure), and forming minute shape in visible light and the pitch below equivalent. The fine rugged structure object is manufactured using a semiconductor manufacturing process (lithography).

[0020]

Fig.2 is the perspective view which expanded an about ten fine rugged structure object [consisting of the single crystal silicon of Fig.1] portion. In the working example 1, the fine unevenness part 10a of the fine rugged structure object 10 is made into the form where it covered with a plurality of quadrangular pyramids periodically, and it is height h from the bottom surface of the square weight 10a of the fine rugged structure object 10 to a vertex.

100A <= h<=5000A

It is carrying out.

[0021]

In working example 1, height h set 1400 A (140 nm) and one side p of the bottom surface of the one quadrangular pyramid 10a to 0.2 micrometer.

[0022]

The transmissivity, the reflectance, and the absorptivity of the light which entered into the solid state imaging device 1 which has the structure shown in Fig.1 are shown in Fig.3. The value shown here is the transmissivity of the beam of light which results in the photoelectric conversion part 3 through the fine rugged structure object 10 and the gate oxide film 4 out of the interlayer insulation film 6. Reflectance and an absorptivity are expressed and the penetration by the interface of the color filter 8, the interface of the interlayer insulation film 6 and the color filter 8, and the micro lens 9 and the interface of air and the micro lens 9, a reflection, absorption, etc. are not taken into consideration.

[0023]

Fig.4 is an essential part cross sectional view of the solid state image pickup device 1a which is not providing the working example 1 and such a fine rugged structure object 10 for comparison.

[0024]

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Fig.5 is the transmissivity, the reflectance, and the absorptivity of the light which entered into the photoelectric conversion part 3 which consists of silicon through the gate oxide film 4 which consists of the interlayer insulation film 6 and silicon oxide film in the solid state image pickup device 1a in Fig.4.

[0025]

From comparison of Fig.3 and Fig.5, the solid state image pickup device 1 by the working example 1 has the following characteristics compared with the solid state image pickup device 1a of Fig.4.

[0026]

(A1) It crosses throughout a visible range with a wavelength of 400 nm - 700 nm, and transmissivity is improving largely.

[0027]

(A2) It crosses throughout a visible range with a wavelength of 400 nm - 700 nm, and reflectance is dramatically low.

[0028]

Therefore, the solid state image pickup device 1 of the working example 1 can attain improvement in the sensitivity of a solid state image pickup device by the increase in transmission quantity from a point of (A1), and photographing of a clear and high-definition image with little generating of noise light, such as the flare, a ghost, etc. by the reflected light from a point of (A2), is easy for it.

[0029]

In the solid state image pickup device of the working example 1, since single crystal silicon was used as the fine rugged structure object 10, some absorption of light has happened by the structure, but. In the conventional solid state image pickup device, the light which was not transmitted reflects and such lights do not pose a problem at all compared with becoming a cause of noise light, such as the flare and a ghost.

[0030]

In the solid state image pickup device by a Patent document 1, since the light which what can expect the improvement in the transmissivity of the light to a photoelectric conversion part did not transmit since the antireflection film by a dielectric was formed on an insulating layer turns into a reflected light, noise light, such as the flare and a ghost, may generate it.

[0031]

By the way, although single crystal silicon was used as the fine rugged structure object 10 in working example 1, as long as it does not limit to this and uses silicon as main materials, polycrystalline silicon, an amorphous silicon, etc. may be sufficient.

[0032]

Since what was formed simultaneously with the gate electrode 5 can be diverted especially when polycrystalline silicon is used, it is preferable also from a manufacturing viewpoint. Since the imaginary component of a complex index of refraction enlarges polycrystalline silicon and an amorphous silicon as compared with single crystal silicon and it becomes what has a slightly high rate of the absorption of light, polycrystalline silicon or single crystal silicon with crystallinity high preferable as much as possible is preferable. In addition, other high refractive index materials, such as germanium (germanium), may be used.

[0033]

Although the structured division 10a of the fine rugged structure object 10 was made into quadrangular pyramid form and the height from a bottom surface to a vertex was 1400 A in the working example 1, there may be dispersion in a certain amount of height.

[0034]

The transmissivity, the reflectance, and the absorptivity at the time of changing to the case

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where square weight-shaped height changes to 1100 A, and 1700 A are shown in Fig.6 and Fig.7, respectively.

[0035]

As shown in Fig.6 and Fig.7, the fine structure part 10a of the fine rugged structure object 10 has that transmissivity, reflectance, and an absorptivity change [little] largely, even if height varies.

[0036]

Although similarly the fine structure part 10a of the fine rugged structure object 10 was made into the abbreviated 4 pyramid form containing quadrangular pyramid form in working example 1, it may be an abbreviated cone containing not the thing to limit to this but the approximately multiple weight which the angle of the structure is slightly round or contains polygonal pyramids other than a quadrangular pyramid, or a cone -- a drill -- it does not matter even if the vertex of form serves as substantially trapezoidal weight form containing even trapezoid ******.

[0037]

Although the fine structure part 10a of the fine rugged structure object 10 was made into quadrangular pyramid form and one side p of the bottom surface was furthermore 0.2 micrometer in working example 1, It is not necessary to be not the thing to limit to this but the less than degree which incident light does not diffract, i.e., 0.4 micrometer, and to be a periodic structure which quadrangular pyramid form has arranged tidily.

[0038]

The part (pixel) 3B which carries out photoelectric conversion of the blue zone (wavelength -450nm) of the incident light which passes the color filter 8, Height, form and a pitch of the topography part 10a of the fine rugged structure object 10, etc. may be changed into every part (pixel) 3G which carries out photoelectric conversion of the green zone (wavelength -550nm), and part (pixel) which carries out photoelectric conversion of red zone (wavelength -650nm) 3R.

[Work example 2]

[0039]

Fig.8 is an essential part cross sectional view of the solid state image pickup device of the working example 2 of the present invention.

[0040]

The working example 2 only differs in the composition of the fine rugged structure object 10 compared with the working example 1, and is the same. [of other composition]

[0041]

In Fig.8, the solid state image pickup device 1 has the photoelectric conversion part (photo-diode) 3, the gate oxide film 4, the gate electrode 5, the interlayer insulation film 6, the metallic wiring 7, the color filter 8, and the micro lens 9 in the silicon substrate 2.

[0042]

the photoelectric conversion part (photo-diode) 3 -- the upper (light incidence side) --- **** -- the fine rugged structure object 10 consisting of the single crystal silicon for antireflections is formed via the gate oxide film 4 with a thickness of 50 A which consists of silicon oxide films.

[0043]

Fig.9 is the perspective view which expanded an about ten fine rugged structure object [consisting of the single crystal silicon of Fig.8] portion.

[0044]

The fine rugged structure object 10 is made into the form where a plurality of rectangular parallelepipeds 10a were arranged at a certain interval, in the working example 2. All the form where height h of the rectangular parallelepiped 10a set the interval p of 600 A and

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arrangement to 0.1 micrometer, and it saw the rectangular parallelepiped 10a from the top is squares, and the width w of one side. The fine unevenness part 10B in the part (pixel) 3B which carries out photoelectric conversion of the blue zone (wavelength -450nm) of incident light is 63 nm. In the fine unevenness part 10R in the part (pixel) 3R which carries out photoelectric conversion of 71 nm and the red zone (wavelength -650nm) in the fine unevenness part 10G of the part (pixel) 3a which carries out photoelectric conversion of the green zone (wavelength -550nm), it may be 78 nm.

[0045]

Namely, when setting the space share F of the fine unevenness parts 10B, 10G, and 10R ($=w^2/p^2$) to F10B, F10G, and F10R

F10B<F10G<F10R

He is trying to become.

[0046]

The structure shown in Fig.10 at Fig.8 to the pixel 3B for the blue zones of the solid state image pickup device 1 which it has The transmissivity of an incident light, The transmissivity, the reflectance, and the absorptivity of an incident light are shown in Fig.11 at the pixel 3G for green zones, and the transmissivity, the reflectance, and the absorptivity of incident light are shown for reflectance and an absorptivity in Fig.12 at the pixel 3R for red zones, respectively.

[0047]

The value shown here is the transmissivity of the beam of light which results in the photoelectric conversion part 3 through the fine rugged structure object 10 and the gate oxide film 4 out of the interlayer insulation film 6. Reflectance and an absorptivity are expressed and the penetration by the interface of the color filter 8, the interface of the interlayer insulation film 6 and the color filter 8, and the micro lens 9 and the interface of air and the micro lens 9, a reflection, absorption, etc. are not taken into consideration.

[0048]

The transmissivity of the light in the photoelectric conversion part which consists of a gate oxide film which consists of a silicon oxide film in the solid state image pickup device which is not providing the fine rugged structure object 10 like Fig.4 mentioned above for comparison, and silicon which entered, As compared with the Fig.5 in which reflectance and an absorptivity were shown, about the pixel of a blue zone, from comparison of Fig.10 and Fig.5, While transmissivity is all improving largely from comparison of Fig.12 and Fig.5 compared with the solid state image pickup device of the former [direction / of the solid state image pickup device by the working example 2] in the pixel of comparison of Fig.11 and Fig.5 to a red zone about the pixel of a green zone, it turns out that reflectance is dramatically low.

[0049]

Therefore, the solid state image pickup device of the working example 2 can photo the clear and high-definition image which attained improvement in sensitivity, and reduction of the flare or a ghost simultaneously.

[0050]

In the solid state image pickup device of the working example 2, since single crystal silicon was used as a fine rugged structure object, some absorption of light has happened by the structure, but. In the conventional solid state image pickup device, the light which was not transmitted reflects and such lights do not pose a problem at all compared with becoming a cause of noise light, such as the flare and a ghost.

[0051]

By the way, although single crystal silicon was used as a fine rugged structure object in working example 2, as long as it does not limit to this and uses silicon as main materials, polycrystalline silicon, an amorphous silicon, etc. may be sufficient.

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[0052]
Since what was formed simultaneously with the gate electrode 5 can be diverted especially when polycrystalline silicon is used, it is preferable also from a manufacturing viewpoint.
[0053]
Since the imaginary component of a complex index of refraction enlarges polycrystalline silicon and an amorphous silicon as compared with single crystal silicon and it becomes what has a slightly high rate of the absorption of light, polycrystalline silicon or single crystal silicon with crystallinity high preferable as much as possible is preferable. In addition, other high refractive index materials, such as germanium (germanium), may be used.
[0054]
In the working example 2, although the structured division 10a of the fine rugged structure object 10 was made into the shape of a square pilaster, it does not limit to this, and the angle of the structure may be slightly round or you may have form of multiple pillars other than a quadratic prism, a pillar, and an elliptic cylinder.
[0055]
Although the fine rugged structure object was used as the quadratic prism and the interval p of arrangement was furthermore 0.1 micrometer in working example 2, it may be the less than degree which is not limited to this and incident light does not diffract, i.e., 0.4 micrometer.
[0056]
moreover -- the working example 2 -- the object for blue zones, the object for green zones, and the object for red zones -- although the height of the fine rugged structure object was the same 600 A by all the pixel and only a width of one side was changed, it may not limit to this and may change height for every pixel.
[0057]
As described above, according to each working example of the present invention, a reflection of the light in the interface of the photoelectric conversion part and interlayer insulation film in a solid state image pickup device can be reduced, while inhibiting generating of noise light, such as the flare and a ghost, the transmissivity of light can also improve, and it can realize a high sensitivity solid state image pickup device.
[0058]
Next, the working example of the camera (optical instrument) using the solid state image pickup device of the present invention as an imaging means is described using Fig.13.
[0059]
It is the photographing optical system which 20 was constituted by the camera body and 21 comprised with the zoom lens in Fig.13. 22 -- a photographing optical system -- 21 -- an object image -- light reception -- carrying out -- CCD -- CMOS -- etc. -- the present invention -- starting -- a solid state image pickup device -- 23 -- a solid state image pickup device -- 22 -- light reception -- having carried out -- an object image -- recording -- a recording device -- 24 -- being not shown -- a display device -- displaying -- having had -- an object image -- observing -- a sake -- a finder -- it is .
[0060]
The above-mentioned display device is constituted by the liquid crystal panel etc., and the object image formed on the solid state image pickup device 22 is displayed.
[0061]
Thus, by applying the solid state image pickup device of the present invention to optical instruments, such as a camera, the optical instrument which has small and high optical performance is realized.
[Brief Description of the Drawings]
[0062]

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[Drawing 1]The essential part cross sectional view of the working example 1 of the present invention

[Drawing 2]The fine rugged structure extension-of-field perspective view concerning the working example 1 of the present invention

[Drawing 3]The explanatory view of the transmissivity, the reflectance, and the absorptivity of the light in the photoelectric conversion part and interlayer insulation film interface in a solid state image pickup device of the working example 1 of the present invention

[Drawing 4]The essential part cross sectional view of the conventional solid state image pickup device

[Drawing 5]The explanatory view of the transmissivity, the reflectance, and the absorptivity of the light in the conventional photoelectric conversion part and interlayer insulation film interface in a solid state image pickup device

[Drawing 6]The explanatory view of the transmissivity, the reflectance, and the absorptivity of the light in a photoelectric conversion part and an interlayer insulation film interface when the height of the fine rugged structure object concerning the working example 1 of the present invention becomes 1100 A

[Drawing 7]The explanatory view of the transmissivity, the reflectance, and the absorptivity of the light in a photoelectric conversion part and an interlayer insulation film interface when the height of the fine rugged structure object concerning the working example 1 of the present invention becomes 1700 A

[Drawing 8]The essential part cross sectional view of the working example 2 of the present invention

[Drawing 9]The fine rugged structure extension-of-field perspective view concerning the working example 2 of the present invention

[Drawing 10]The explanatory view of the transmissivity, the reflectance, and the absorptivity of the light in the photoelectric conversion part and interlayer insulation film interface of the pixel for blue zones in the solid state image pickup device of the working example 2 of the present invention

[Drawing 11]The explanatory view of the transmissivity, the reflectance, and the absorptivity of the light in the photoelectric conversion part and interlayer insulation film interface of the pixel for green zones in the solid state image pickup device of the working example 2 of the present invention

[Drawing 12]The explanatory view of the transmissivity, the reflectance, and the absorptivity of the light in the photoelectric conversion part and interlayer insulation film interface of the pixel for red zones in the solid state image pickup device of the working example 2 of the present invention

[Drawing 13]The essential part schematic view of the optical instrument of the present invention

[Explanations of letters or numerals]

[0063]

1 Solid state image pickup device
2 Silicon substrate
3 Optoelectric transducer (photo-diode)
4 Gate oxide film
5 Gate electrode
6 Interlayer insulation film
7 Metallic wiring
8 Color filter
9 Micro lens

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10 Antireflection structure
20 Camera body
21 Photographing optical system
22 Solid state image pickup device
23 Recording device
24 Finder (not shown)

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DRAWINGS

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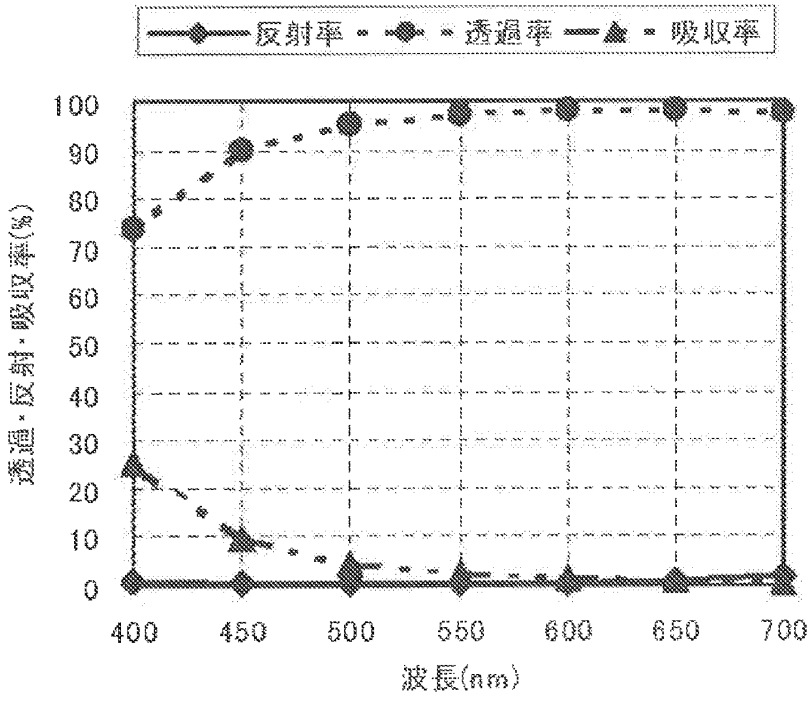
DRAWINGS

[Drawing 3]



[Drawing 5]

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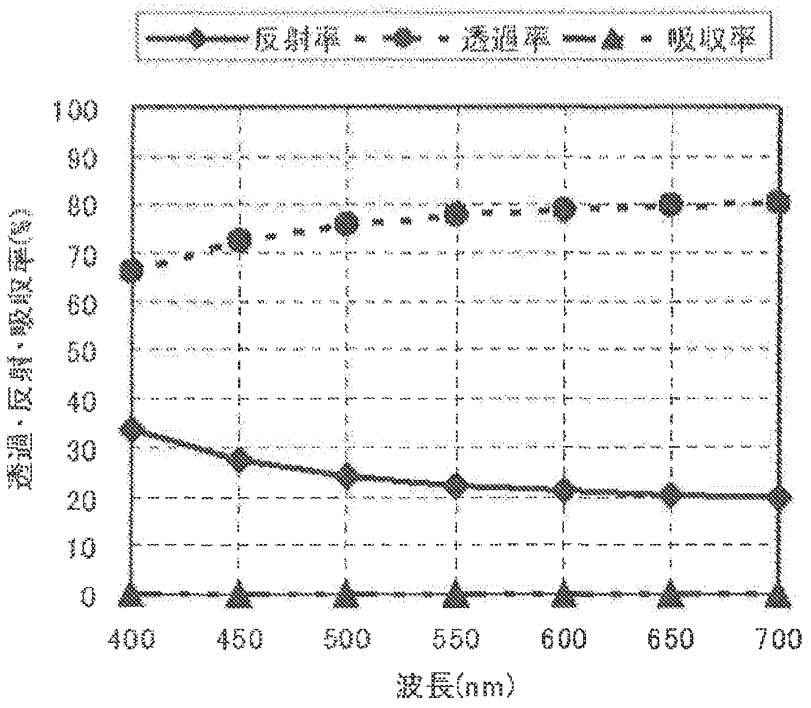
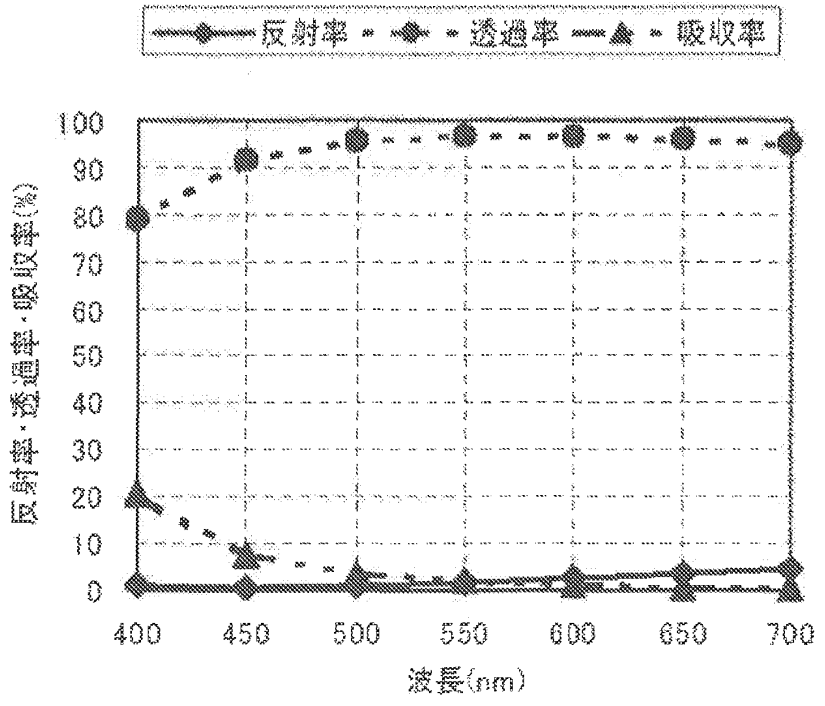


[Drawing 6]



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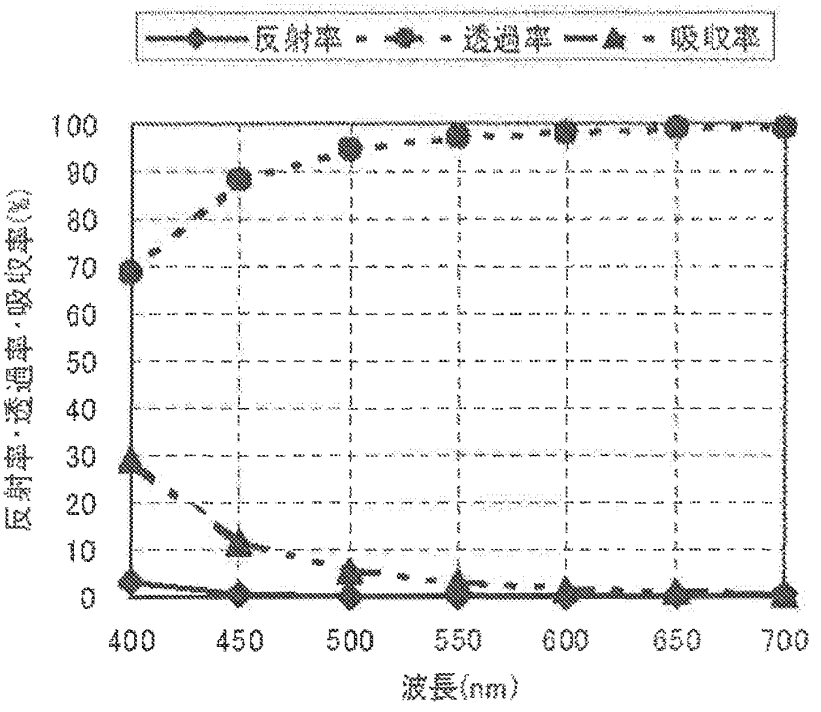
[Drawing 7]



[Drawing 10]

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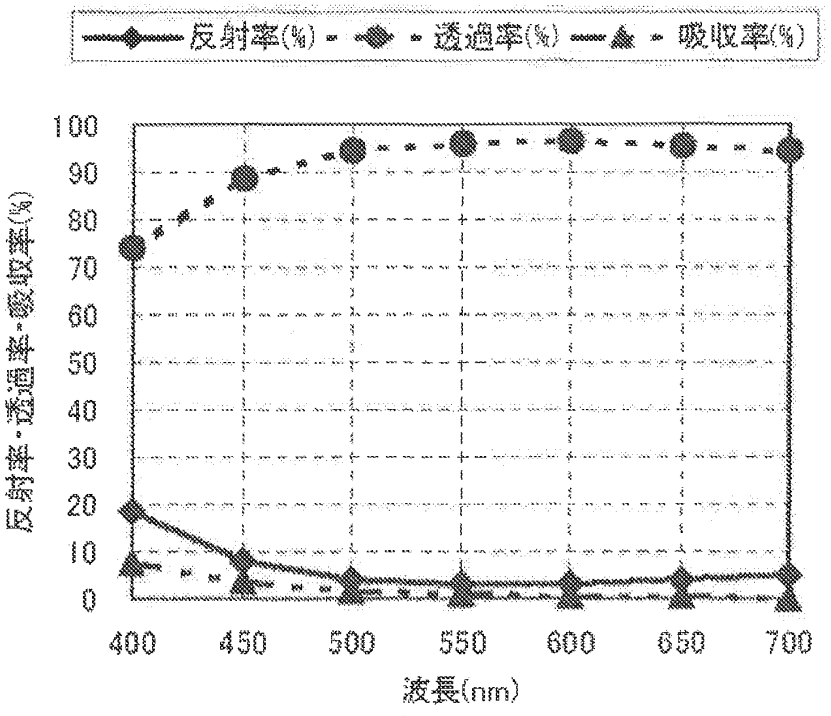
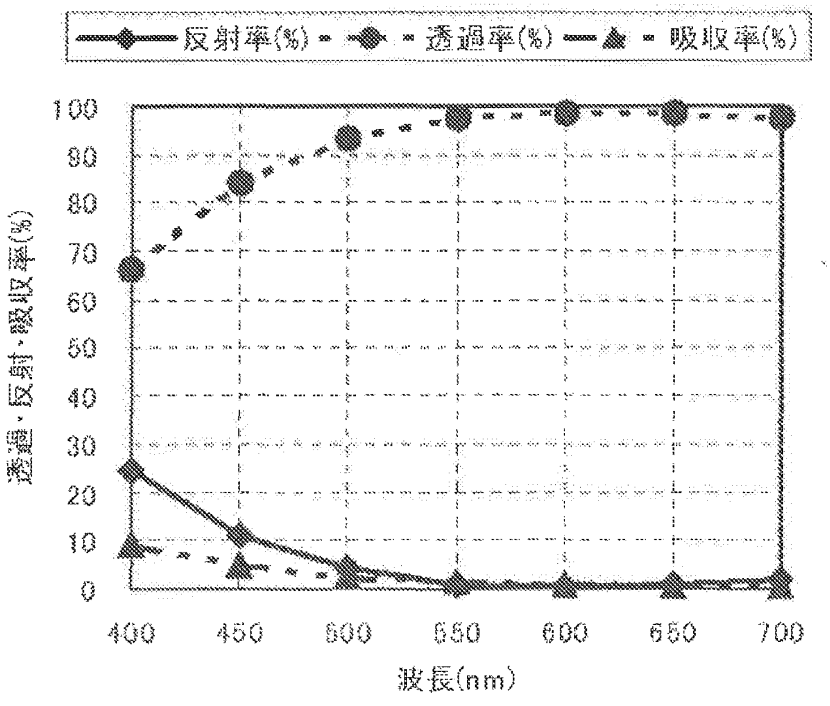


[Drawing 11]



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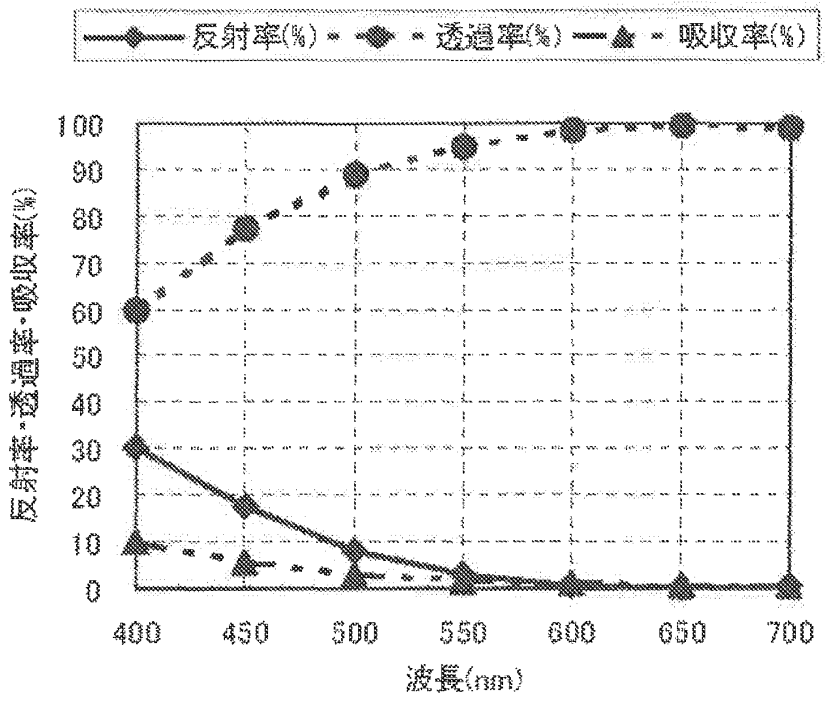
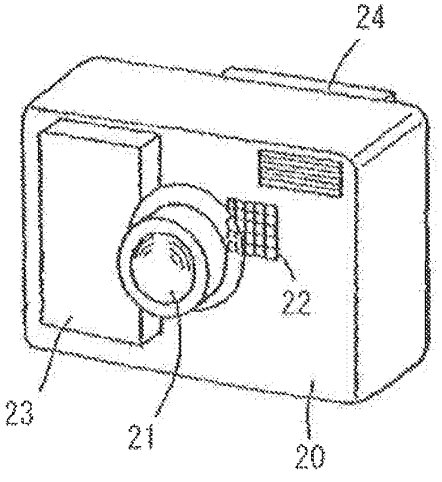
[Drawing 12]





[Drawing 13]

[Drawing 1]

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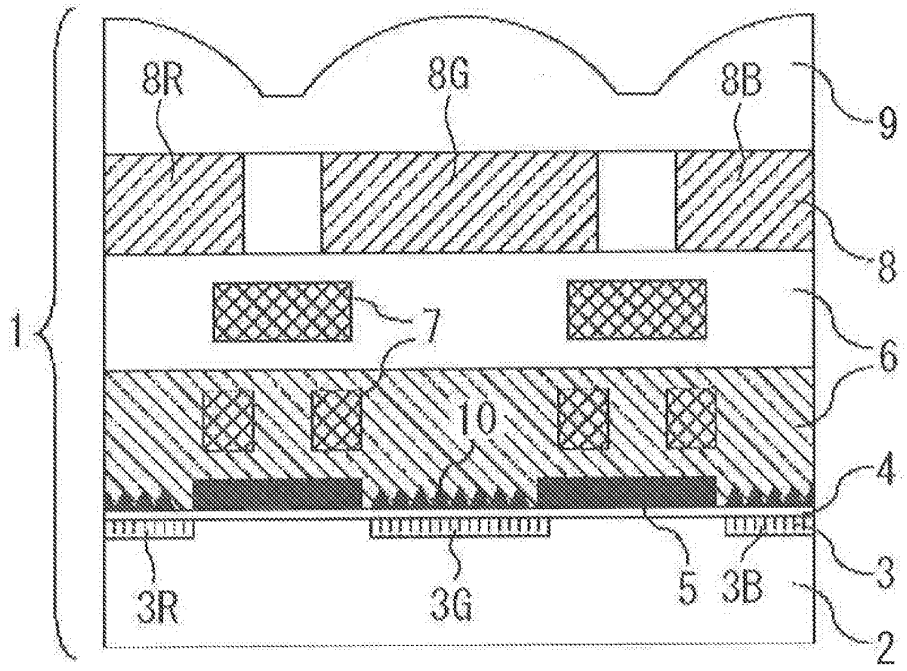
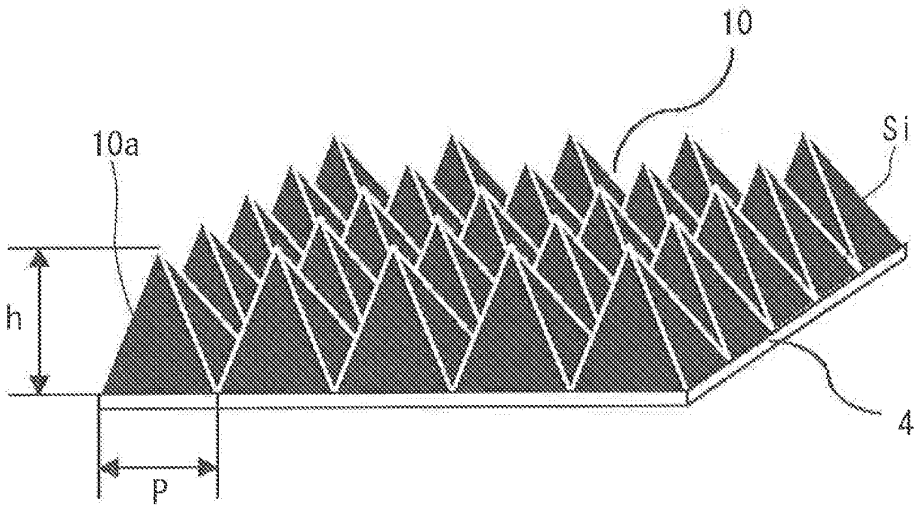


[Drawing 2]



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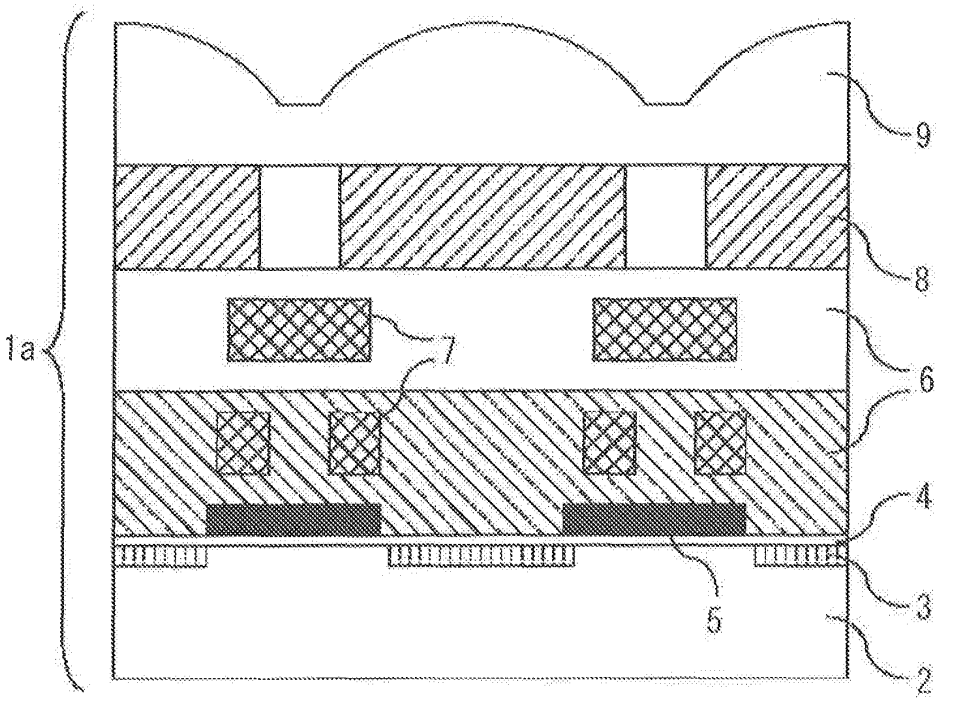

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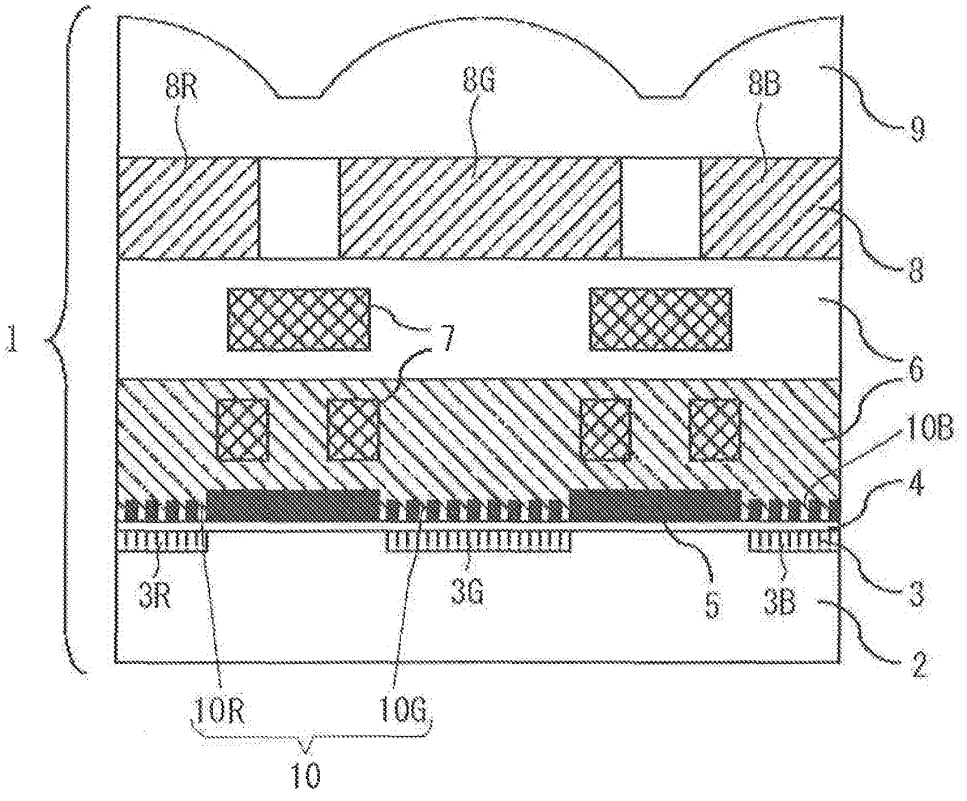

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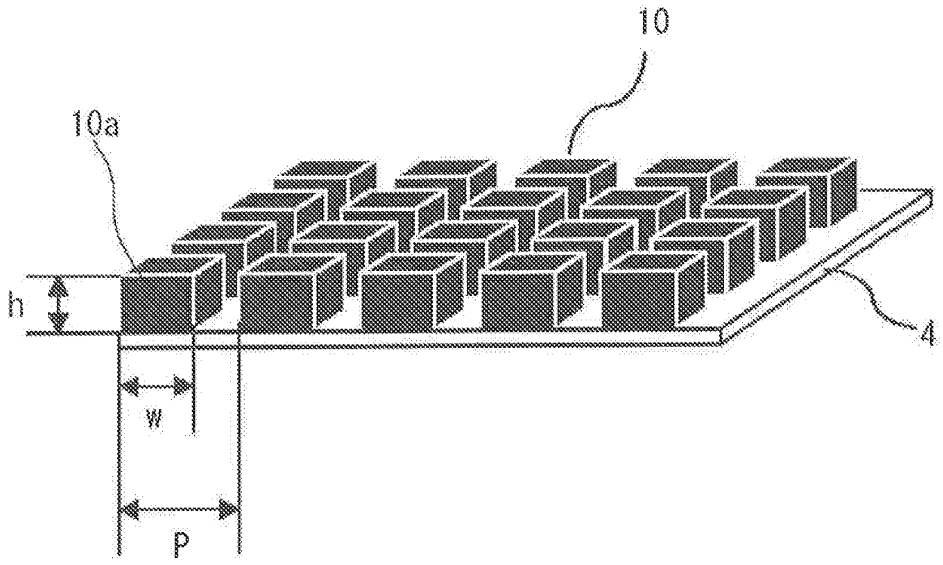

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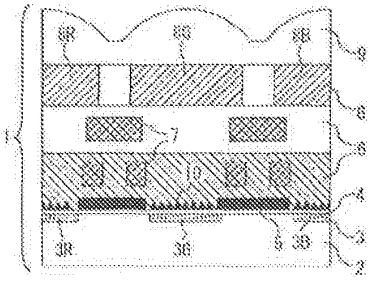
(54)【発明の名称】固体撮像素子及びそれを有する光学機器

(57)【要約】
【課題】　光電変換部と絶縁膜との界面での光の反射を低減し、フレアやゴーストなどのノイズ光の発生を抑制するとともに、高感度な固体撮像素子を得ること。
【解決手段】　シリコンからなる基板に、入射した光の強度に応じて電荷を発生させる光電変換素子を形成した固体撮像素子であって、
　該光電変換素子の光入射側にシリコン酸化膜からなる絶縁膜を介して、微細凹凸構造体が形成されていること。
【選択図】　図1



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【特許請求の範囲】
【請求項１】
基板に入射した光の強度に応じて電荷を発生させる光電変換部を形成した固体撮像素子であって、
該光電変換素子の光入射側に薄膜を介して、凹凸構造体を有することを特徴とする固体撮像素子。
【請求項２】
前記薄膜は、厚さが１０Å以上５００Å以下であることを特徴とする請求項１に記載の固体撮像素子。
【請求項３】
前記薄膜はシリコン酸化膜であることを特徴とする請求項１又は２に記載の固体撮像素子。
【請求項４】
前記光電変換部はシリコンで形成されていることを特徴とする請求項１から３のいずれか１項に記載の固体撮像素子。
【請求項５】
前記凹凸構造体は、複数の凹凸部を２次元的に配置して構成されており、該凹凸部は、光入射側から前記光電変換部側に向かって徐々に体積占有率が増加する形状であることを特徴とする請求項１から４のいずれか１項に記載の固体撮像素子。
【請求項６】
前記凹凸構造体は、複数の凹凸部を２次元的に配置して構成されており、該凹凸部は略四角錐形状、又は略円錐形状、又は略台形四角錐形状又は略台形円錐形状であることを特徴とする請求項１から５のいずれか１項に記載の固体撮像素子。
【請求項７】
該凹凸構造体の高さは、１００Å以上５０００Å以下であることを特徴とする請求項１～６のいずれか１項に記載の固体撮像素子。
【請求項８】
前記凹凸構造体は、単結晶シリコン又は多結晶シリコン又はアモルファスシリコンを材料とすることを特徴とする請求項１から７のいずれか１項に記載の固体撮像素子。
【請求項９】
前記基板に形成された複数の光電変換部と、各光電変換部の光入射側に前記凹凸構造体と複数の種類のカラーフィルタとを有し、
該凹凸部の高さ又は／及びピッチは、カラーフィルタの種類に応じて異なることを特徴とする請求項１から８のいずれか１項に記載の固体撮像素子。
【請求項１０】
請求項１から９のいずれか１項記載の固体撮像素子と
を有することを特徴とする光学機器。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明はＣＭＯＳやＣＣＤ等の固体撮像素子に関し、特に受光部の感度の低下を抑制した高感度の固体撮像素子を有したデンタルカメラ、ビデオカメラ、電子スチルカメラ等の光学機器に好適なものである。
【背景技術】
【０００２】
近年、ＣＭＯＳやＣＣＤに代表される固体撮像素子は、高精彩な画像を得るために多画素化が進み、かつ、携帯電話やＰＤＡなどのいわゆるモバイル端末に搭載するために小型化が求められ、これによって一画素あたりの面積が非常に小さくなり、感度が低下する傾向があった。
【０００３】

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また、固体撮像素子の内部構造に着目すると、シリコンで形成された光電変換素子（光電変換部）とその上に形成された絶縁膜とでは、光の屈折率が大きく異なることから、各境界面から全体として入射光の２０％近くないしはそれ以上の光を反射してしまい感度が低下する傾向があった。

【０００４】

又、別の部位、部材で再度反射してきた光が光電変換部に入射することにより、フレアやゴーストなどのノイズ光が発生する原因となっている。

【０００５】

光電変換部（受光部）の前側（光入射側）に反射防止手段を設けて、受光感度の低下を少なくした固体撮像素子が知られている（特許文献１，２）。

【特許文献１】特開２０００－１２８２２号公報

【特許文献２】特開２００３－２４９６３９号公報

【発明の開示】

【発明が解決しようとする課題】

【０００６】

特許文献１は、受光部（光電変換部）の上に厚さ１００～２００ｎｍのSiO_2により成るゲート酸化膜（絶縁膜）を介して厚さ６０ｎｍ程度のシリコン窒化膜より成る反射防止膜を形成することで、光電変換部（受光部）での光の反射を抑制する構造のＭＯＳ型固体撮像装置を提案している。

【０００７】

特許文献１のＭＯＳ型固体撮像装置は、反射防止膜に求められる屈折率の観点から、シリコン窒化膜（波長５５０ｎｍにおける屈折率約２．０４）は、シリコン（波長５５０ｎｍにおける複素屈折率４．０８－０．０４ｉ）とシリコン酸化膜（波長５５０ｎｍにおける屈折率１．４６）の界面の反射を完全に防止することが難しい。

【０００８】

また、この構成はシリコン窒化膜の厚さに対応した１つの特定の波長に対して高い反射防止効果が得られても、異なる波長に対しては反射防止効果が低下してしまい、結局、抑制しきれなかった反射光はフレアやゴーストの発生原因となる。

【０００９】

特許文献２はフォトダイオード（光電変換部）とシリコン酸化膜からなる絶縁膜の界面に屈折率が連続的に単調変化する凹凸形状を設け光の反射を防止することで、反射に起因した見掛けの感度の低下の問題を改善または解消するとともに、スミアに起因した撮像性能の低下の問題を改善または解消した固体撮像装置を提案している。

【００１０】

特許文献２の固体撮像装置は、そこに記載されているように、フォトダイオード表面にエッチングなどにより凹凸形状を形成した場合、エッチング時のプラズマダメージやシリコンの格子欠陥の発生、金属汚染の侵入などによりノイズの発生が著しく増大してくることがある。

【００１１】

また、プラズマダメージや汚染などのない方法でエッチングすることができたとしても、その後の熱プロセスにより、シリコン酸化膜との熱膨張係数の違いなどによる応力で格子欠陥が生じてノイズの発生原因となり、実質感度の向上が難しい。

【００１２】

本発明は、光電変換部への光の透過量を向上するとともに、反射光が少なく、フレアやゴーストなどのノイズ光を抑制した、高感度な固体撮像素子及びそれを有する光学機器の提供を目的とする。

【課題を解決するための手段】

【００１３】

本発明の固体撮像素子は、基板に入射した光の強度に応じて電荷を発生させる光電変換部を形成した固体撮像素子であって、

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該光電変換素子の光入射側に薄膜を介して、凹凸構造体を有することを特徴としている。

【発明の効果】

【００１４】

本発明によれば、光電変換部への光の透過量を向上するとともに、反射光が少なく、フレアやゴーストなどのノイズ光を抑制した、高感度な固体撮像素子及びそれを有する光学機器が得られる。

【発明を実施するための最良の形態】

【００１５】

【実施例１】

【００１６】

図１は、本発明の実施例１の固体撮像素子の要部断面図である。

【００１７】

図１において、固体撮像素子１は、シリコン基板２に複数の光電変換部３（３Ｒ，３Ｇ，３Ｂ）、絶縁膜としてのシリコン酸化膜より成るゲート酸化膜（薄膜）４、ゲート電極５、層間絶縁膜６、金属配線７、赤色フィルタ８Ｒ、緑色フィルタ８Ｇ、青色フィルタ８Ｂを有するカラーフィルタ８、マイクロレンズ９を有している。光電変換部（フォトダイオード）３の上（光入射側）には、シリコン酸化膜よりなる厚さ５０Å（５ｎｍ）のゲート酸化膜（薄膜）４を介して、反射防止用の単結晶シリコンよりなる複数の微細凹凸部１０ａを２次元的に配置した微細凹凸構造体１０が形成されている。

【００１８】

実施例１の固体撮像素子１は、固体撮像素子１の光電変換部の光入射側に絶縁膜４を介して、シリコンを主要な材料とする微細凹凸構造体１０を設けている。

【００１９】

微細凹凸構造体１０はＳＷＳ（Sub Wave length Structure）と呼ばれ、可視光と同等以下のピッチで微細形状を形成することで界面反射光量を抑制する素子である。微細凹凸構造体は、半導体製造プロセス（リングラフィー）を利用して製造している。

【００２０】

図２は、図１の単結晶シリコンよりなる微細凹凸構造体１０近傍の部分を拡大した斜視図である。実施例１では、微細凹凸構造体１０の微細凹凸部１０ａを複数の四角錐を周期的に敷きつめた形状としており、微細凹凸構造体１０の四角錐１０ａの底面から頂点までの高さｈは

$$１００Å \leqq h \leqq ５０００Å$$

としている。

【００２１】

実施例１では高さｈは、１４００Å（１４０ｎｍ）、１つの四角錐１０ａの底面の一辺ｐを０．２μｍとした。

【００２２】

図３に、図１に示す構造を有する固体撮像装置１に入射した光の透過率、反射率及び吸収率を示す。なお、ここで示した値は、層間絶縁膜６中から微細凹凸構造体１０、ゲート酸化膜４を経て光電変換部３に至る光線の透過率、反射率、吸収率を表したものであって、カラーフィルタ８と層間絶縁膜６の界面、カラーフィルタ８とマイクロレンズ９の界面、空気とマイクロレンズ９の界面での透過、反射、吸収などは考慮していない。

【００２３】

図４は、実施例１と比較のための、このような微細凹凸構造体１０を設けていない固体撮像素子１ａの要部断面図である。

【００２４】

図５は図４において、固体撮像素子１ａでの層間絶縁膜６とシリコン酸化膜よりなるゲート酸化膜４を経てシリコンよりなる光電変換部３に入射した光の透過率、反射率および吸収率である。

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【００２５】
図３と図５の比較から、実施例１による固体撮像素子１は、図４の固体撮像素子１ａに比べて以下のような特徴を有する。
【００２６】
（Ａ１）波長４００ｎｍ～７００ｎｍの可視域全域にわたって、透過率が大きく向上している。
【００２７】
（Ａ２）波長４００ｎｍ～７００ｎｍの可視域全域にわたって、反射率が非常に低い。
【００２８】
従って実施例１の固体撮像素子１は、（Ａ１）の点から、透過量の増加により固体撮像素子の感度の向上が達成でき、（Ａ２）の点から、反射光によるフレアやゴーストなどノイズ光の発生が少ないクリアで高品位な画像の撮影が容易である。
【００２９】
また、実施例１の固体撮像素子では、微細凹凸構造体１０として単結晶シリコンを用いたために、同構造体により若干の光の吸収が起こっているが、これらの光は従来の固体撮像素子では透過しなかった光が反射してしまい、フレアやゴーストなどのノイズ光の原因になるのに比べ、何ら問題となるものではない。
【００３０】
さらに、特許文献１による固体撮像素子では、絶縁層上に誘電体による反射防止膜を形成しているために、光電変換部への光の透過率の向上は期待できるものの透過しなかった光は反射光となるため、フレアやゴーストなどのノイズ光が発生する場合がある。
【００３１】
ところで、実施例１では微細凹凸構造体１０として、単結晶シリコンを用いたが、これに限定するものではなく、シリコンを主要な材料とするものであれば多結晶シリコン、アモルファスシリコンなどでも構わない。
【００３２】
特に、多結晶シリコンを用いた場合は、ゲート電極５と同時に形成したものを流用可能なので、製造上の観点からも好ましい。単結晶シリコンと比較して、多結晶シリコン、アモルファスシリコンは複素屈折率の虚数成分が大きくなるため、光の吸収率が若干高いものとなってしまうので、好ましくはできるだけ結晶性の高い多結晶シリコンないしは単結晶シリコンが好ましい。この他Ｇｅ（ゲルマニウム）等他の高屈折率材料を用いても良い。
【００３３】
また、実施例１では、微細凹凸構造体１０の構造部１０ａを四角錐形状とし、底面から頂点までの高さを１４００Åとしたが、ある程度の高さのばらつきがあっても良い。
【００３４】
図６,図７に四角錐形状の高さが１１００Åに変化した場合と１７００Åに変化した場合の透過率、反射率及び吸収率をそれぞれ示す。
【００３５】
図６、図７に示したように、微細凹凸構造体１０の微細構造部１０ａは、高さがばらついても透過率、反射率および吸収率が大きく変化することは少ない。
【００３６】
同様にして、実施例１では、微細凹凸構造体１０の微細構造部１０ａを四角錐形状を含む略４角錐形状としたが、これに限定するものではなく、若干構造体の角が丸まっていたり、四角錐以外の多角錐を含む略多角錐あるいは円錐を含む略円錐になっていてもよく、また錐形状の頂点が平らな台形錐形状を含む略台形錐形状となっていても構わない。
【００３７】
さらに実施例１では、微細凹凸構造体１０の微細構造部１０ａを四角錐形状とし、その底面の一辺ｐを０．２μｍとしたが、これに限定するものではなく、入射光が回折しない程度、すなわち０．４μｍ以下であればよく、また、四角錐形状が恒久と配列しているよ

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うな周期的な構造である必要もない。

【００３８】

また、カラーフィルタ８を通過する入射光の青帯域（波長～４５０ｎｍ）を光電変換する部位（画素）３Ｂ、緑帯域（波長～５５０ｎｍ）を光電変換する部位（画素）３Ｇ、赤帯域（波長～６５０ｎｍ）を光電変換する部位（画素）３Ｒごとに、微細凹凸構造体１０の微細構成部１０ａの高さや形状そしてピッチ等を変えても良い。

【実施例２】

【００３９】

図８は、本発明の実施例２の固体撮像素子の要部断面図である。

【００４０】

実施例２は実施例１に比べて微細凹凸構造体１０の構成が異なっているだけであり、その他の構成は同じである。

【００４１】

図８において、固体撮像素子１は、シリコン基板２に光電変換部（フォトダイオード）３、ゲート酸化膜４、ゲート電極５、層間絶縁膜６、金属配線７、カラーフィルタ８、マイクロレンズ９を有している。

【００４２】

光電変換部（フォトダイオード）３の上（光入射側）には、シリコン酸化膜よりなる厚さ５０Åのゲート酸化膜４を介して、反射防止用の単結晶シリコンよりなる微細凹凸構造体１０が形成されている。

【００４３】

図９は、図８の単結晶シリコンよりなる微細凹凸構造体１０近傍の部分を拡大した斜視図である。

【００４４】

実施例２では、微細凹凸構造体１０を複数の直方体１０ａをある間隔で配列した形状としている。直方体１０ａの高さｈは６００Å、配列の間隔ｐは０．１μｍとし、直方体１０ａを上から見た形状はすべて正方形であり、一辺の幅ｗは、入射光の青帯域（波長～４５０ｎｍ）を光電変換する部位（画素）３Ｂでの微細凹凸部１０Ｂは６３ｎｍ、緑帯域（波長～５５０ｎｍ）を光電変換する部位（画素）３ａの微細凹凸部１０Ｇでは７１ｎｍ、赤帯域（波長～６５０ｎｍ）を光電変換する部位（画素）３Ｒでの微細凹凸部１０Ｒでは７８ｎｍとしている。

【００４５】

即ち、微細凹凸部１０Ｂ，１０Ｇ，１０Ｒの空間占有率Ｆ（$=w^2/p^2$）をＦ１０Ｂ，Ｆ１０Ｇ，Ｆ１０Ｒとするとき

Ｆ１０Ｂ＜Ｆ１０Ｇ＜Ｆ１０Ｒ

となるようにしている。

【００４６】

図１０に図８に示す構造を有する固体撮像素子１の青帯域用の画素３Ｂに入射する光の透過率、反射率及び吸収率を、図１１に緑帯域用の画素３Ｇに入射する光の透過率、反射率及び吸収率を、図１２に赤帯域用の画素３Ｒに入射する光りの透過率、反射率及び吸収率をそれぞれ示す。

【００４７】

なお、ここで示した値は、層間絶縁膜６中から微細凹凸構造体１０、ゲート酸化膜４を経て光電変換部３にいたる光線の透過率、反射率、吸収率を表したものであって、カラーフィルタ８と層間絶縁膜６の界面、カラーフィルタ８とマイクロレンズ９の界面、空気とマイクロレンズ９の界面での透過、反射、吸収などは考慮していない。

【００４８】

比較のために、前述した図４のような微細凹凸構造体１０を設けていない固体撮像素子でのシリコン酸化膜よりなるゲート酸化膜とシリコンよりなる光電変換部での入射した光の透過率、反射率および吸収率を示した図５と比較すると、青帯域の画素については図１

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０と図５の比較から、緑帯域の画素については図１１と図５の比較から、赤帯域の画素においては図１２と図５の比較から、いずれも実施例２による固体撮像素子の方が従来の固体撮像素子に比べ、透過率が大きく向上しているとともに、反射率が非常に低いことが分かる。

【００４９】

従って、実施例２の固体撮像素子は、感度の向上とフレアやゴーストの低減を同時に達成した、クリアで高品位な画像が撮影可能である。

【００５０】

また、実施例２の固体撮像素子では、微細凹凸構造体として単結晶シリコンを用いたために、同構造体により若干の光の吸収が起こっているが、これらの光は従来の固体撮像素子では透過しなかった光が反射してしまい、フレアやゴーストなどのノイズ光の原因になるのに比べ、何ら問題となるものではない。

【００５１】

ところで、実施例２では微細凹凸構造体として、単結晶シリコンを用いたが、これに限定するものではなく、シリコンを主要な材料とするものであれば多結晶シリコン、アモルファスシリコンなどでも構わない。

【００５２】

特に、多結晶シリコンを用いた場合は、ゲート電極５と同時に形成したものを流用可能なので、製造上の観点からも好ましい。

【００５３】

単結晶シリコンと比較して、多結晶シリコン、アモルファスシリコンは複素屈折率の虚数成分が大きくなるため、光の吸収率が若干高いものとなってしまうので、好ましくはできるだけ結晶性の高い多結晶シリコンないしは単結晶シリコンが好ましい。この他Ｇｅ（ゲルマニウム）等他の高屈折率材料を用いても良い。

【００５４】

また、実施例２では、微細凹凸構造体１０の構造部１０ａを四角柱形状としたが、これに限定するものではなく、若干構造体の角が丸まっていたり、四角柱以外の多角柱や円柱、楕円柱の形状になっていても構わない。

【００５５】

さらに実施例２では、微細凹凸構造体を四角柱とし、配列の間隔ｐを０．１μｍとしたが、これに限定するものではなく、入射光が回折しない程度、すなわち０．４μｍ以下であればよい。

【００５６】

また、実施例２では、青帯域用、緑帯域用、赤帯域用全ての画素で微細凹凸構造体の高さを同じ６００Åとし、一辺の幅だけを変化させたが、これに限定するものではなく、画素ごとに高さを変化させても良い。

【００５７】

以上説明したように、本発明の各実施例によれば、固体撮像素子における光電変換部と層間絶縁膜との界面での光の反射を低減し、フレアやゴーストなどのノイズ光の発生を抑制するとともに光の透過率も向上し、高感度な固体撮像素子を実現することができる。

【００５８】

次に本発明の固体撮像素子を撮像手段として用いたカメラ（光学機器）の実施例を図１３を用いて説明する。

【００５９】

図１３において、２０はカメラ本体、２１はズームレンズによって構成された撮影光学系、２２は撮影光学系２１によって被写体像を受光するＣＣＤやＣＭＯＳ等の本発明に係る固体撮像素子、２３は固体撮像素子２２が受光した被写体像を記録する記録手段、２４は不図示の表示素子に表示された被写体像を観察するためのファインダーである。

【００６０】

上記表示素子は液晶パネル等によって構成され、固体撮像素子２２上に形成された被写

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体像が表示される。

【００６１】

このように本発明の固体撮像素子をカメラ等の光学機器に適用することにより、小型で高い光学性能を有する光学機器を実現している。

【図面の簡単な説明】

【００６２】

【図１】本発明の実施例１の要部断面図

【図２】本発明の実施例１に係る微細凹凸構造体の拡大斜視図

【図３】本発明の実施例１の固体撮像素子における光電変換部と層間絶縁膜界面での光の透過率・反射率・吸収率の説明図

【図４】従来の固体撮像素子の要部断面図

【図５】従来の固体撮像素子における光電変換部と層間絶縁膜界面での光の透過率・反射率・吸収率の説明図

【図６】本発明の実施例１に係る微細凹凸構造体の高さが１１００Åとなった場合の光電変換部と層間絶縁膜界面での光の透過率・反射率・吸収率の説明図

【図７】本発明の実施例１に係る微細凹凸構造体の高さが１７００Åとなった場合の光電変換部と層間絶縁膜界面での光の透過率・反射率・吸収率の説明図

【図８】本発明の実施例２の要部断面図

【図９】本発明の実施例２に係る微細凹凸構造体の拡大斜視図

【図１０】本発明の実施例２の固体撮像素子における青帯域用画素の光電変換部と層間絶縁膜界面での光の透過率・反射率・吸収率の説明図

【図１１】本発明の実施例２の固体撮像素子における緑帯域用画素の光電変換部と層間絶縁膜界面での光の透過率・反射率・吸収率の説明図

【図１２】本発明の実施例２の固体撮像素子における赤帯域用画素の光電変換部と層間絶縁膜界面での光の透過率・反射率・吸収率の説明図

【図１３】本発明の光学機器の要部概略図

【符号の説明】

【００６３】

１　固体撮像素子
２　シリコン基板
３　光電変換素子（フォトダイオード）
４　ゲート酸化膜
５　ゲート電極
６　層間絶縁膜
７　金属配線
８　カラーフィルタ
９　マイクロレンズ
１０　反射防止構造体
２０　カメラ本体
２１　撮影光学系
２２　固体撮像素子
２３　記録手段
２４　ファインダー（不図示）

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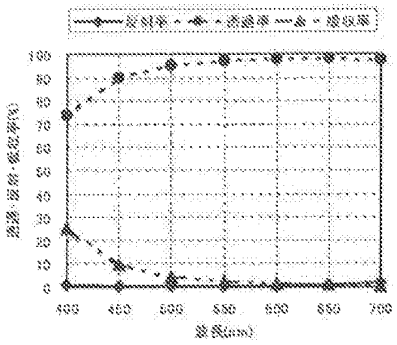
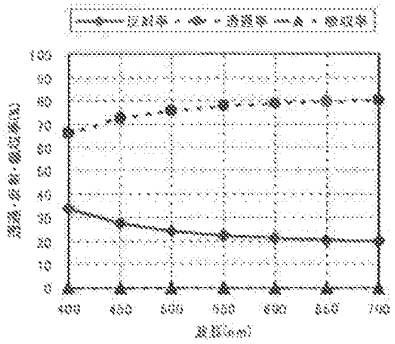
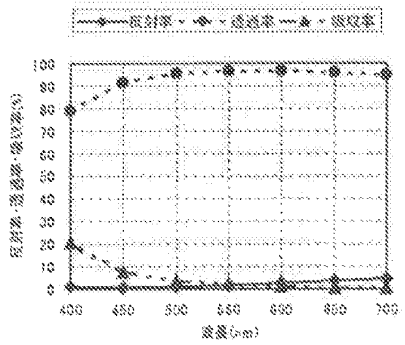
【図３】



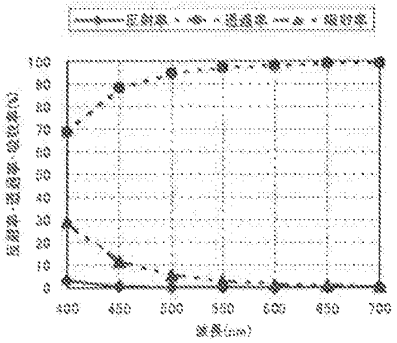
【図５】



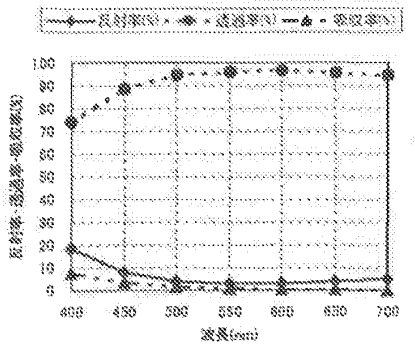
【図６】



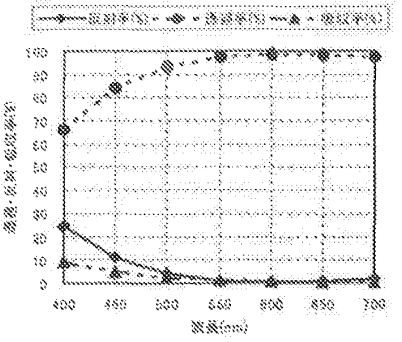
【図７】



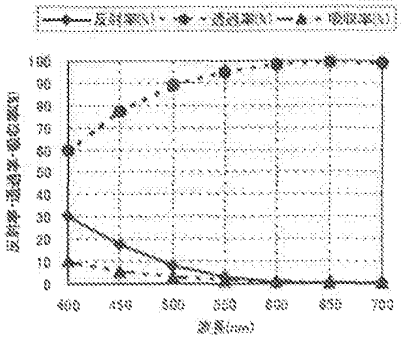
【図１０】



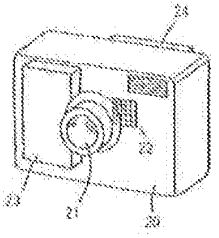
【図１１】



【図１２】



【図１３】



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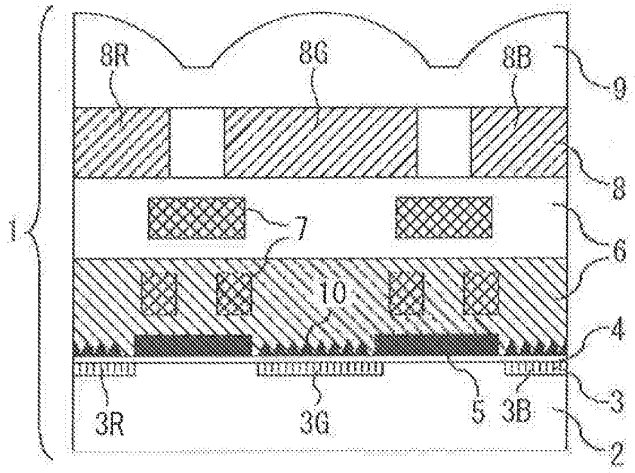
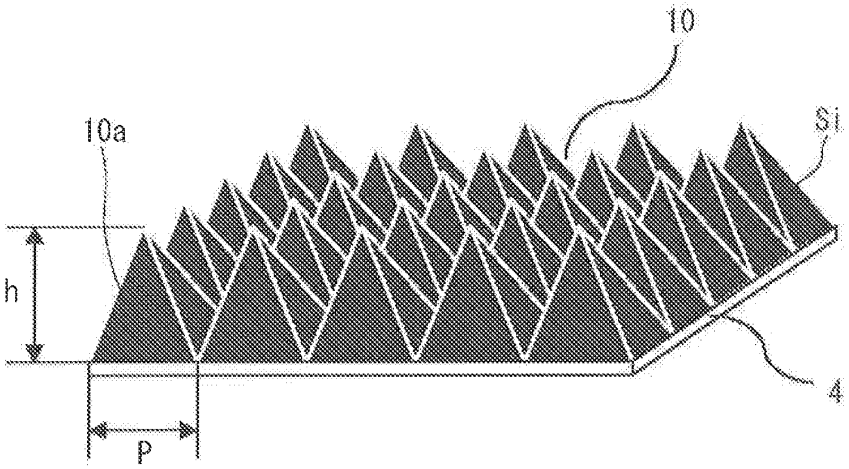
【図１】



【図２】



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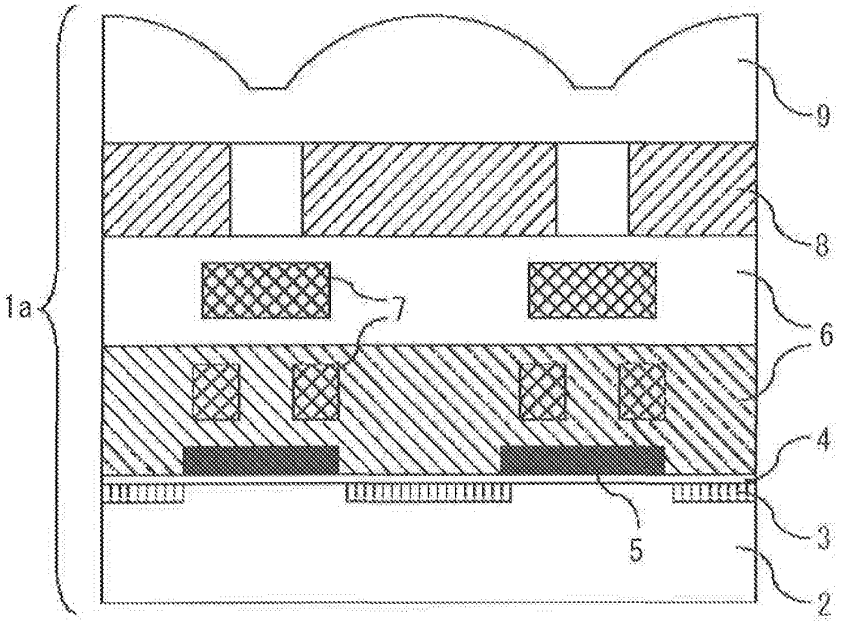
【図４】



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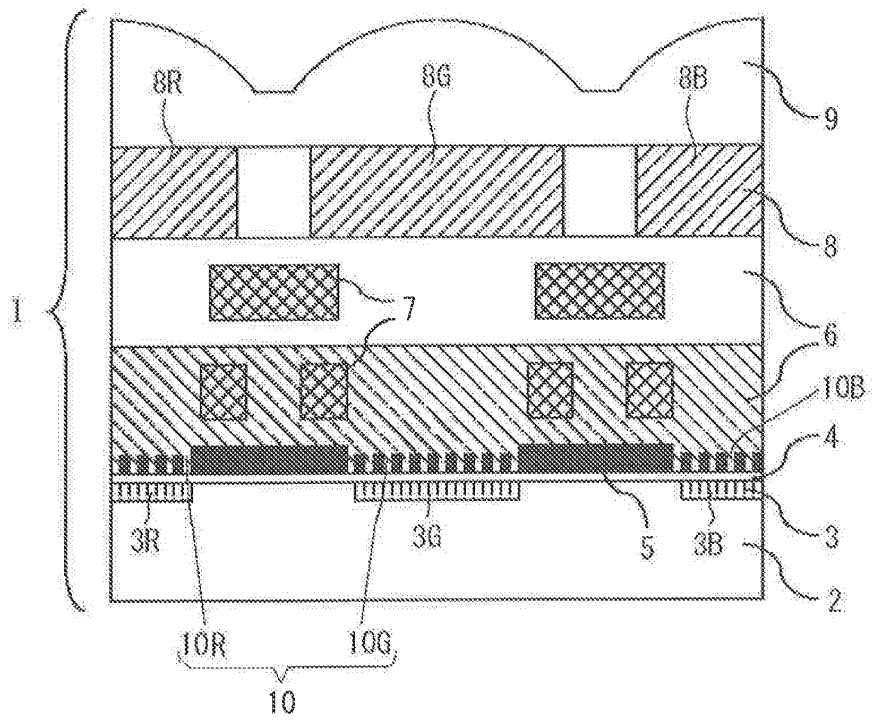
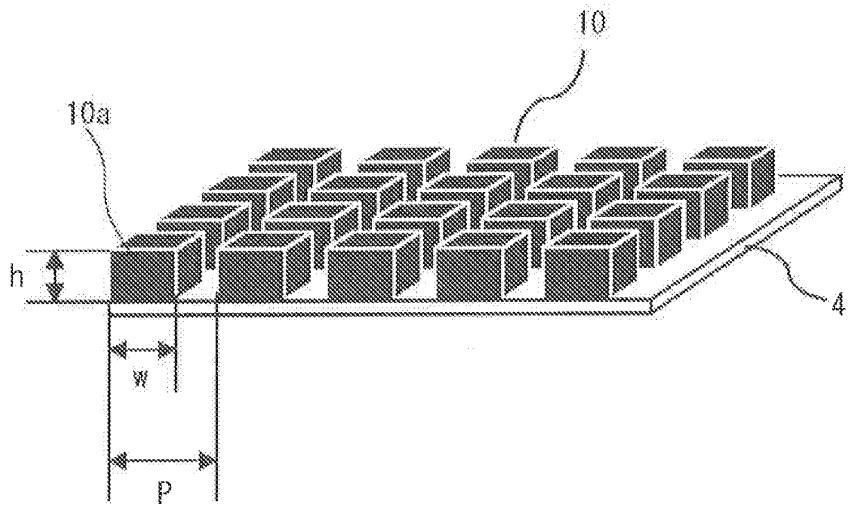
【図８】



【図９】



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(54)IMAGING APPARATUS

(57)Abstract

PROBLEM TO BE SOLVED: To provide an inexpensive imaging apparatus where crosstalk is suppressed and the number of components and mandays are reduced.

SOLUTION: Respective microlenses 21 in a microlens array 20 form subject images in a plurality of pixels 11 of an imaging device 10. A first color filter array 31 is arranged on a subject side compared with the imaging device 10, and a second color filter array 32 is arranged between the first color filter array 31 and the imaging device 10. The first and second color filter arrays 31 and 32 are provided with at least 2 kinds of color filters of the same arrangement. The color filters provided in the first and second color filter arrays 31 and 32 and the microlenses 10 correspond to each other by one to one.

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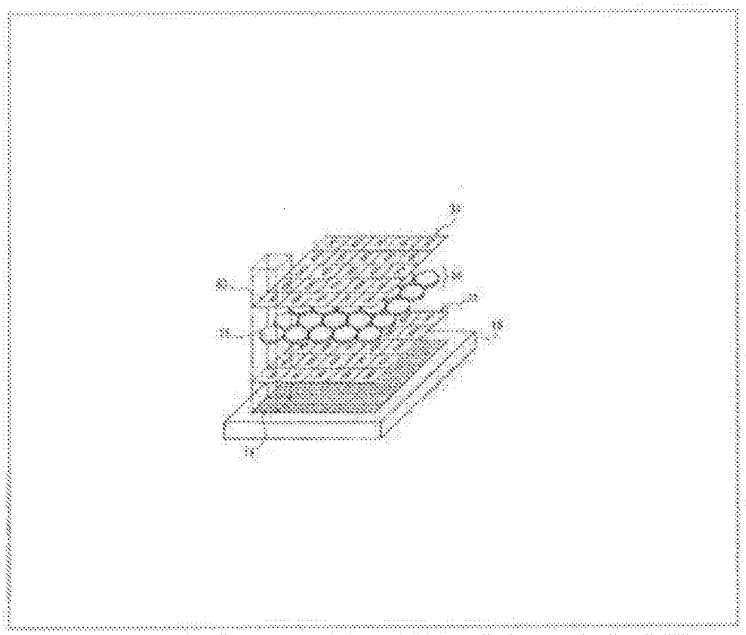

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CLAIMS

[Claim(s)]
[Claim 1]
A solid state image pickup device provided with a many pixel which has a photoelectric conversion function arranged in the 1st plane, It is an imaging device which images an object image to a plurality of aforementioned pixels to which have microlens array provided with a plurality of microlenses arranged in the 2nd plane, a plurality of aforementioned pixels are equivalent to to the one aforementioned microlens, and each aforementioned microlens corresponds,
The 1st color filter array provided with at least 2 or more type of color filters arranged in the 3rd plane on the object side to said 1st plane, It has the 2nd color filter array provided with at least 2 or more type of color filters arranged in the 4th plane that is placed between said 3rd plane and said 1st plane by the same arrangement as a color filter of said 1st color filter array,
An imaging device, wherein each of aforementioned color filters of said 1st color filter array, aforementioned microlenses, and the aforementioned color filters of said 2nd color filter array and the aforementioned microlenses corresponds to the couple 1.
[Claim 2]
The imaging device comprising according to claim 1:
A color filter in which said 1st color filter array and said 2nd color filter array transmit red light.
A color filter which transmits green light.
A color filter which transmits blue glow.

[Claim 3]
The imaging device according to claim 1 with which 2 or more aforementioned type of color filters are arranged in the shape of a checker in said 1st color filter array and said 2nd color filter array so that a color filter of the same kind may not be adjacent to mutually.
[Claim 4]
The imaging device according to claim 1 with which said 3rd plane is placed at the object side to said 2nd plane.
[Claim 5]
The imaging device according to claim 1 which said 3rd plane was placed between said 2nd plane and said 4th plane, and said 3rd plane and said 4th plane have separated.
[Claim 6]
The imaging device according to claim 1 which said 2nd color filter array approaches an incident plane of a solid state image pickup device, or is arranged on the aforementioned incident plane.
[Claim 7]
The imaging device according to claim 1 containing a color filter which transmits a color filter in which said 1st color filter array and said 2nd color filter array transmit infrared light, and/or

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ultraviolet radiation.

[Claim 8]

The imaging device according to claim 1 further provided with an extracting circuit which extracts selectively only a signal from the aforementioned pixel corresponding to the aforementioned color filter of the same kind among signals from the many aforementioned pixel of the aforementioned solid state image pickup device.

[Claim 9]

The imaging device according to claim 1 whose aforementioned solid state image pickup device is CCD.

[Claim 10]

The imaging device according to claim 1 whose aforementioned solid state image pickup device is CMOS.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[Field of the Invention]

[0001]

The present invention relates to an imaging device. It is related with the imaging device which has arranged the microlens array which arranged a plurality of microlenses in the plane on the object side of the solid state image pickup device which has a many pixel especially.

[Background of the Invention]

[0002]

In the commercial scene of a digital still camera which market size is enlarging, the needs for the small size and the thin camera which were more excellent in portability are growing in recent years. The miniaturization is proceeding circuit components, such as LSI which bears signal processing, by high efficiency by micronization of the wiring pattern, etc. Small size and a mass thing can also obtain an archive medium now at a low price. However, it cannot say that the miniaturization of the imaging system which comprises a lens and solid state image pickup devices, such as CCD and CMOS, is still sufficient, but also in order to realize the camera which was more excellent in portability, development of a small imaging system is demanded.

[0003]

The imaging device using the lens array optical system which arranged a plurality of microlenses on the plane as composition for realizing the miniaturization of an imaging system is known. Since it became long to optical axis direction, volume increased, and since the lens diameter was large, the optical system which arranged a plurality of lenses in on the conventional optic axis had the problem that aberration enlarged. On the other hand, it can do thinly in optical axis direction, and since each diameter of a microlens is small, the lens array optical system can suppress aberration comparatively small.

[0004]

The imaging device using such a lens array is disclosed in the Patent document 1. The microlens array 111 by which a plurality of microlenses 111a were arranged in the same plane sequentially from the object side as this imaging device was shown in Fig.6, It has the barrier layer 112 which consists of the septum 112a of the shape of a lattice frame for separating so that the lightwave signal from each microlens 111a may not interfere each other, and the photo detector array 113 by which the many optoelectric transducer 113a is arranged in the same plane. The one microlens 111a, one space corresponding to this separated by the septum 112a, and a plurality of optoelectric transducers 113a constitute the one image formation unit 115. In each image formation unit 115, the microlens 111a images an object image on a plurality of corresponding optoelectric transducers 113a. Thereby, a taken image is obtained every image formation unit 115. The resolution of this taken image is dependent on the number of the optoelectric transducers 113a which constitute the one image formation unit 115 (pixel number). When the relative locations of each microlens 111a to an object differ, the

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image formation positions of the object image formed on a plurality of optoelectric transducers 113a differ every image formation unit 115. As a result, the taken images obtained differ every image formation unit 115. One image can be acquired by carrying out signal processing of several of these mutually different taken images.

[0005]

Since there are few pixel numbers which constitute each image formation unit 115 with this imaging device. Although the image quality of the taken image obtained from each image formation unit 115 is low, the image of the same image quality as the case where a photograph is taken by a many optoelectric transducer can be acquired by carrying out signal processing using the taken image shifted little by little obtained in a plurality of image formation units 115, respectively, and reconstructing an image.

[0006]

the optoelectric transducer 113a of the next image formation unit 115 in which the light from the microlens 111a does not correspond with this microlens 111a in the imaging device of Fig.6 -- being incident (this phenomenon is called a "cross talk") --- A high-definition image is not reconstructible, or the stray light occurs, and image quality deteriorates, or it produces optical loss. Therefore, in order to prevent a cross talk, the barrier layer 112 is used. in the Patent document 1, the same effect as this is replaced with the barrier layer 112, and is described as being obtained, even if it arranges the deviation filter array which has arranged the deviation transmission filter, respectively to the 111st page of microlens array, and the 113rd page of a photo detector array so that a deflection direction may intersect perpendicularly every image formation unit 115.

[Patent document 1] Japanese Published Patent Application No. 2001-61109 (JP2001-61109A)

[Description of the Invention]

[Problem to be solved by the invention]

[0007]

However, in order to form the septum 112a corresponding to each image formation unit 115, the barrier layer 112 used for the imaging device of the above-mentioned Fig.6 carries out micro processing of the stainless steel etc., it assembles with high precision, and shines, and is created. Therefore, a process is complicated and serves as a high cost. While managing a relative location strictly, it is necessary to assemble the barrier layer 112, the microlens array 111, and the photo detector array 113 which were obtained, and assembly operation becomes complicated.

[0008]

Since the deviation filter array used instead of the barrier layer 112 is created using a diffraction grating or a refraction type optical element, the number of parts and the number of assemblers increase it.

[0009]

An object of the present invention is to provide the inexpensive imaging device which solved the problem which the conventional above-mentioned imaging device has, and could inhibit the cross talk and with which the number of parts and a man-hour were reduced.

[Means for solving problem]

[0010]

An imaging device of the present invention is provided with the following.

A solid state image pickup device provided with a many pixel which has a photoelectric conversion function arranged in the 1st plane.

Microlens array provided with a plurality of microlenses arranged in the 2nd plane.

An object image is imaged to a plurality of aforementioned pixels to which a plurality of aforementioned pixels are equivalent to to the one aforementioned microlens, and each

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aforementioned microlens corresponds.

[0011]

The 1st color filter array that the imaging device of the present invention equips with at least 2 or more type of color filters arranged in the 3rd plane on the object side to the 1st above-mentioned plane further, It has the 2nd color filter array provided with at least 2 or more type of color filters arranged in the 4th plane that is placed between the 3rd above-mentioned plane and the 1st above-mentioned plane by the same arrangement as the color filter of the 1st above-mentioned color filter array, Each of aforementioned color filters of the 1st above-mentioned color filter array, aforementioned microlenses, and the aforementioned color filters of the 2nd above-mentioned color filter array and the aforementioned microlenses corresponds to the couple 1.

[Effect of the Invention]

[0012]

According to the present invention, generating of a cross talk can be inhibited, without using the indispensable barrier layer and a polarizing filter array in the conventional imaging device, since it has the 1st color filter array and the 2nd color filter array which have the same color filter arrangement.

[0013]

Since a cross talk can be inhibited, a high-definition image can be photoed that image quality deterioration can be lessened, by the ability to suppress generating of the stray light, etc.

[0014]

Since assembly operation can be simplified since the barrier layer and the polarizing filter array are unnecessary, and the number of parts can be reduced, an inexpensive imaging device can be provided. Since part precision and assembling precision can be improved, a high quality imaging device can be provided.

[Best Mode of Carrying Out the Invention]

[0015]

As for the 1st above-mentioned color filter array and the 2nd above-mentioned color filter array, in the above-mentioned imaging device of the present invention, it is preferable that the color filter which transmits red light, the color filter which transmits green light, and the color filter which transmits blue glow are included. Thereby, color photography can be performed.

[0016]

In the 1st above-mentioned color filter array and the 2nd above-mentioned color filter array, it is preferable that 2 or more aforementioned type of color filters are arranged in the shape of a checker so that a color filter of the same kind may not be adjacent to mutually. Thereby, a cross talk can be reduced.

[0017]

As for the 3rd above-mentioned plane, it is preferable that it is placed at the object side to the 2nd above-mentioned plane. Since the interval between the 1st color filter array and the 2nd color filter array can be secured comparatively largely by this, making thickness of the whole imaging device thin, the reduction effect of a cross talk improves.

[0018]

Or as for the 3rd above-mentioned plane, it is preferable that were placed between the 2nd above-mentioned plane and the 4th above-mentioned plane, and the 3rd above-mentioned plane and the 4th above-mentioned plane have separated. This composition can also reduce a cross talk by securing the interval between the 1st color filter array and the 2nd color filter array.

[0019]

As for the 2nd above-mentioned color filter array, it is preferable to approach the incident plane

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of a solid state image pickup device, or to be arranged on the aforementioned incident plane. Thereby, the cross talk between the 2nd color filter array and a solid state image pickup device can be reduced.

[0020]

The 1st above-mentioned color filter array and the 2nd above-mentioned color filter array may contain the color filter which transmits the color filter which transmits infrared light, and/or ultraviolet radiation. Thereby, photographing by infrared rays and/or ultraviolet rays is attained.

[0021]

It may further have the extracting circuit which extracts selectively only the signal from the aforementioned pixel corresponding to the aforementioned color filter of the same kind among the signals from the many aforementioned pixel of the aforementioned solid state image pickup device. This becomes possible to choose and photo only the light of a desired specific wavelength range.

[0022]

The aforementioned solid state image pickup device may be CCD. Or it may be CMOS.

[0023]

Hereinafter, about an embodiment of the invention, while referring to Drawings, it describes.

[0024]

(Embodiment 1)

Fig.1 is a perspective view showing the schematic structure of the imaging device of the embodiment 1 of the present invention. Fig.2 is a fragmentary sectional view in a surface including the optic axis of a microlens of the imaging device of the embodiment 1 of the present invention. Fig.3 (A) is the figure showing the outline of processing of the signal from a solid state image pickup device in the imaging device of the embodiment 1 of the present invention. Fig.3 (B) is a perspective view showing the light-receiving part which constitutes one image formation unit in the imaging device of the embodiment 1 of the present invention.

[0025]

It is the microlens array provided with a plurality of microlenses 21 arranged in the every direction in the 2nd plane that was parallel to the 1st plane as for a solid state image pickup device (for example, CCD and CMOS) provided with the many pixel 11 by which 10 was arranged by the every direction in the 1st plane in Fig.3, and 20, and was separated from Fig.1.

[0026]

31 is parallel to the 1st plane, and it is the 1st color filter array provided with a plurality of color filters arranged by the every direction in the 3rd plane on the object side rather than the 1st plane. 32 is parallel to the 1st plane, and it is the 2nd color filter array provided with a plurality of color filters arranged in the every direction in the 4th plane that is placed between the 3rd plane and the 1st plane. In this embodiment, the 1st and 2nd color filter arrays 31 and 32, It has the color filter R which transmits red light selectively, the color filter G which transmits green light selectively, and the color filter B which transmits blue glow selectively, and is arranged in the shape of a checker in each region where these were classified in the shape of a lattice frame. The 1st color filter array 31 and the 2nd color filter array 32 are the same about arrangement of the color filter R, G, and B.

[0027]

The red who constitutes the 1st color filter array 31 to the one microlens 21, the color filter of any 1 color of green and the blue, The red who constitutes the 2nd color filter array 32, the color filter of any 1 color of green and the blue, and a plurality of pixels 11 correspond, and the one image formation unit 40 is constituted by these. The color of the color filter of the 1st color

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filter array 31 and the color of the color filter of the 2nd color filter array 32 which constitute the same image formation unit 40 correspond.

[0028]

Only which colored light of red-green blue is chosen by the 1st color filter array 31, and the light flux from an object transmits this, and enters into a plurality of microlenses 21. Each microlens 21 forms an object image on a plurality of corresponding pixels 11. Which colored light of the red-green blue which emitted the microlens 21 enters into the 2nd color filter array 32, before becoming the pixel 11. Each color filter of the 2nd color filter array 32 makes only the colored light same among incident light as the color of an own color filter transmit.

[0029]

The imaging device of this embodiment can prevent a cross talk by the above-mentioned composition. This is described using Fig.2.

[0030]

For example, the beam of light R1 from an object enters into the red color filter R of the 1st color filter array 31, and only the light of a red wavelength range passes this and it enters into the red color filter R of the 2nd color filter array 32 after passing the microlens 21. Since this incident light is the light of a red wavelength range, it can pass this color filter R and forms a red object image on the pixel 11.

[0031]

On the other hand, by a bigger incidence angle than the beam of light R1, to an imaging device the beam of light R2 from an incident object, It enters into the red color filter R of the 1st color filter array 31, and only the light of a red wavelength range passes this and enters into the green color filter G which constitutes the image formation unit of the next door of the 2nd color filter array 32 after passing the microlens 21. The green color filter G does not pass the incident light of this red wavelength range. Therefore, the light of any wavelength ranges which constitute the beam of light R2 does not become the pixel 11.

[0032]

Thus, as for the imaging device of the present invention, each image formation unit 40 equips optical axis direction with two layers of color filters of the same color. In the 1st and 2nd color filter arrays 31 and 32, it is arranged so that the color filter R, G, and B from which a color differs may constitute a checker. That is, the color filter R, G, and B is arranged so that the color of any one color filter may differ from the color of four color filters which are adjacent to to an every direction on both sides of four sides of this color filter. As a result, the beam of light exceeding the boundary between the image formation units 40 which are adjacent to between until it is incident to the 2nd color filter array 32 in an every direction cannot pass the 2nd color filter array 32 after passing the 1st color filter array 31 like the above-mentioned beam of light R2. Therefore, generating of a cross talk can be prevented. Thereby, image quality deterioration can be lessened and generating of the stray light can be suppressed. As a result, a high-definition image can be photoed.

[0033]

It is made to be the same as that of the color filter array currently used widely in the color filter used for CCD or a liquid crystal display element, For example, the 1st color filter array 31 may be formed on the microlens array 20, the 2nd color filter array 32 can be formed on the solid state image pickup device 10, respectively, and manufacture can be markedly simplified compared with the conventional septum and deviation filter array of an imaging device which were mentioned above, and the number of parts can also be reduced. Since the accuracy of the 1st and 2nd color filter arrays 31 and 32 self and the accuracy to the microlens array 20 and the solid state image pickup device 10 can also improve compared with the former, quality is improved and stabilized.

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[0034]
Although the 1st color filter array 31 is arranged rather than the microlens array 20 at the object side and the 2nd color filter array 32 is arranged between the microlens array 20 and the solid state image pickup device 10 in the above-mentioned embodiment, Arrangement of the 1st and 2nd color filter arrays 31 and 32 will not be limited to this, if generating of a cross talk can be inhibited. For example, the 1st color filter array 31 and the 2nd color filter array 32 may be arranged between the microlens array 20 and the solid state image pickup device 10. In this case, as for the 1st color filter array 31 and the 2nd color filter array 32, it is preferable to make optical axis direction separate only a predetermined distance. Since the beam of light with a big incidence angle will cross the boundary between the image formation units 40 which are adjacent to if both are close, it becomes meaningless substantially to have used the color filter arrays 31 and 32 of two sheets.
[0035]
However, irrespective of the arrangement order of the 1st color filter array 31, the 2nd color filter array 32, and the microlens array 20, As for the 2nd color filter array 32 arranged rather than the 1st color filter array 31 at solid state image pickup device 10 slippage, it is preferable to approach the incident plane of the solid state image pickup device 10, or to be arranged on the incident plane of the solid state image pickup device 10. After the beam of light which passed the 2nd color filter array 32 crosses the boundary between the image formation units 40 which are adjacent to by this, it can reduce entering into the solid state image pickup device 10. That is, generating of the cross talk between the 2nd color filter array 32 and the solid state image pickup device 10 can be reduced.
[0036]
Next, the method of acquiring an image from the light flux which entered into each light-receiving part 11 of the solid state image pickup device 10 is described using Fig.3 (A) and Fig.3 (B).
[0037]
As shown in Fig.3 (A), the microlens 21 of the microlens array 20 images the image 91 of the object 90 on the solid state image pickup device 10 every image formation unit 40. Each light-receiving part (pixel) 11 of the solid state image pickup device 10 carries out photoelectric conversion of the light flux which entered. Here, the horizontal axis of the solid state image pickup device 10 is made into a x axis, a vertical axis is made into the y-axis, and if the signal from the light-receiving part 11 in a position (x, y) is set to I (x, y), the signal I about all the light-receiving parts 11 contained in the solid state image pickup device 10 (x, y) will be read (Step 101).
[0038]
Next, the signal I from each of this light-receiving part 11 (x, y) is divided every image formation unit 40. Namely, the i-th row in the image formation unit 40 in which the light-receiving part 11 is arranged at an m sequence xn line as shown in Fig.3 (B), If the position of the light-receiving part 11 in the position of the k-th line is made into $_{(m,n)}$ (i, k) and the signal from this light-receiving part 11 is made into I(i, k) $_{(m,n)}$, each above-mentioned signal I (x, y) will be treated as signal I(i, k) $_{(m,n)}$ in the image formation unit 40. As a result, the image which consists of the pixel of an m sequence xn line is reconstructed every image formation unit 40 (Step 103).
[0039]
Then, between the different image formation units 40, signal I(i, k) $_{(m,n)}$ is processed and the image of one sheet is reconstructed (Step 105). As this signal processing, the method described in the above-mentioned Patent document 1 can be used, and that detailed explanation is omitted. Since the forming positions of the object image 91 in the image

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formation unit 40 differ every image formation unit 40, signal I(i, k) $_{(m,n)}$ from the light-receiving part 11 with same position (i, k) differs every image formation unit 40. Therefore, the image of the high resolution which exceeded the number of the light-receiving parts 11 contained in the one image formation unit 40 (mxn individual) you to be Haruka is acquired.

[0040]

(Embodiment 2)

Fig.4 is a front view showing arrangement of the color filter of the 1st and 2nd color filter array 71 and 72 mounted on the imaging device concerning the embodiment 2 of the present invention. Fig.5 is a block diagram showing the flow of processing of the signal from a solid state image pickup device in the imaging device concerning the embodiment 2 of the present invention.

The imaging device of this embodiment is replaced with the 1st and 2nd color filter array 31 and 32 provided with 3 type of color filters R, G, and B shown by embodiment 1, and the 1st and 2nd color filter array 71 and 72 shown in Fig.4 is used. This 1st and 2nd color filter array 71 and 72, Like the 1st and 2nd color filter array 31 and 32 shown by embodiment 1, In addition to the color filter B which transmits selectively the color filter G which transmits selectively the color filter R which transmits red light selectively, and green light, and blue glow, it has color filter IR which transmits infrared light selectively. 4 type of these color filters R, G, and B and IR are arranged in the shape of a checker in each region classified in the shape of a lattice frame corresponding to the image formation unit 40. The color of the color filter which is adjacent to is not the same like embodiment 1. Thereby, the beam of light exceeding the boundary between the image formation units 40 which are adjacent to between until it is incident to the 2nd color filter array 72 cannot pass the 2nd color filter array 72 after passing the 1st color filter array 71 the same with having described by embodiment 1. Therefore, generating of a cross talk can be prevented.

[0041]

In this embodiment 2, the output signal from such an imaging device is processed as follows by the video chain 50 shown in Fig.5. That is, each light-receiving part 11 of the solid state image pickup device 10 carries out photoelectric conversion of the lightwave signal of the object 90, and outputs it. The extracting circuit 51 in the video chain 50 extracts selectively the signal from the light-receiving part 11 with which the color of a color filter is included in the same image formation unit 40 among the signals from the solid state image pickup device 10. The adder circuit 52 performs processing described by Fig.3 (A) and Fig.3 (B) to the monochromatic signal extracted in the extracting circuit 51, and reconstructs the image of monochromatic high resolution.

[0042]

For example, if the extracting circuit 51 extracts the signal from the image formation unit 40 corresponding to red and the green and blue color filter R, G, and B of 3 colors among the signals from the solid state image pickup device 10, the adder circuit 52 will reconstruct red and the green and blue image of 3 colors. If this image of 3 colors is synthesized, a color picture can be displayed on the display device 60.

[0043]

If the extracting circuit 51 extracts only the signal from the image formation unit 40 corresponding to color filter IR of infrared light among the signals from the solid state image pickup device 10, the adder circuit 52 will reconstruct the image of infrared light. Therefore, an infrared taken image can be displayed on the display device 60.

[0044]

Thus, since the 1st and 2nd color filter array 71 and 72 is provided [according to this embodiment] with color filter IR in addition to the color filter R, G, and B, Infrared

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photographing in the darkness which cannot be recognized visually in naked eyes, such as night, can also be performed as well as the ability to perform color photography like embodiment 1.

[0045]

Of course, it is able for the extracting circuit 51 to extract only the signal from the image formation unit 40 corresponding to 1 color or any 2 [red and] of 3 green and blue colors, and to acquire the image of a desired color.

[0046]

Although the 1st and 2nd color filter array 71 and 72 was provided with color filter IR which transmits infrared light selectively in this embodiment 2, it may have the color filter which replaces with color filter IR or transmits ultraviolet radiation selectively in addition to this. It may have the color filter which makes only the light of specific wavelength ranges other than infrared light or ultraviolet radiation transmit.

[Industrial applicability]

[0047]

Although there is no restriction in particular, since the field of the invention of the imaging device of the present invention can obtain high resolution images though it has small size and a thin shape, it can be used for various personal digital assistants, such as a digital still camera, a mobile phone, a notebook sized personal computer, and PDA, etc., for example.

[Brief Description of the Drawings]

[0048]

[Drawing 1]Fig.1 is an exploded perspective view showing the schematic structure of the imaging device of the embodiment 1 of the present invention.

[Drawing 2]Fig.2 is a cross sectional view in a surface including the optic axis of a microlens of the imaging device of the embodiment 1 of the present invention.

[Drawing 3]Fig.3 (A) is the figure showing the outline of processing of the signal from a solid state image pickup device in the imaging device of the embodiment 1 of the present invention. Fig.3 (B) is an imaging device of the embodiment 1 of the present invention.

It is a perspective view showing the light-receiving part which sets and constitutes one image formation unit.

[Drawing 4]Fig.4 is a front view showing the color filter array in the imaging device of the embodiment 2 of the present invention.

[Drawing 5]Fig.5 is a block diagram showing the outline of processing of the signal from a solid state image pickup device in the imaging device of the embodiment 2 of the present invention.

[Drawing 6]Fig.6 is an exploded perspective view showing the schematic structure of the conventional imaging device.

[Explanations of letters or numerals]

[0049]

10 Solid state image pickup device
11 Pixel
20 Microlens array
21 Microlens
31 and 71 The 1st color filter array
32 and 72 The 2nd color filter array
40 Image formation unit
50 Video chain
51 Extracting circuit
52 Adder circuit

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60 Display device
90 Object

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DRAWINGS

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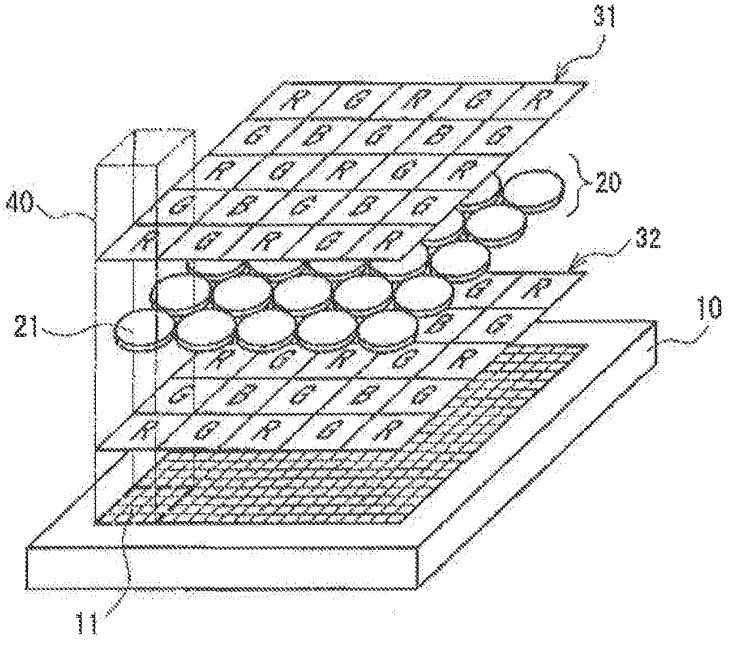
DRAWINGS

[Drawing 1]



[Drawing 2]

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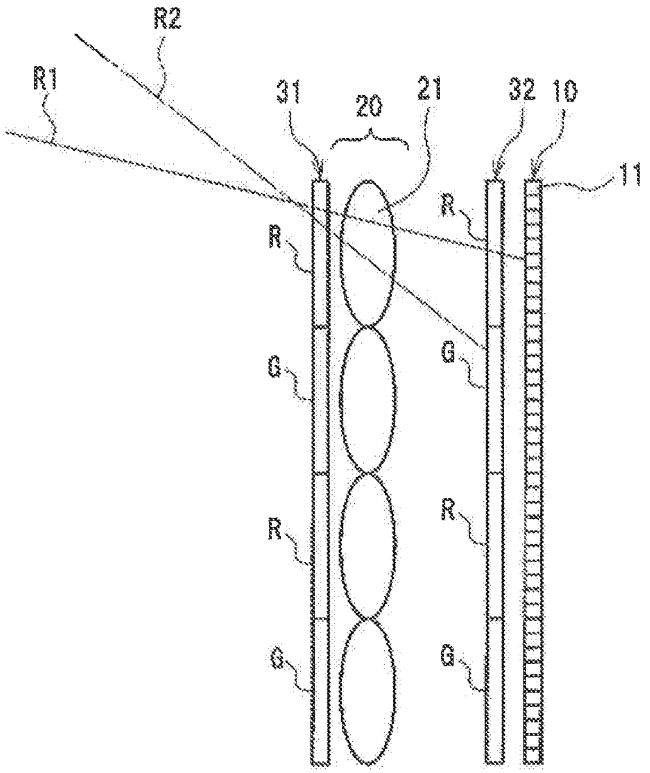

[Drawing 3]

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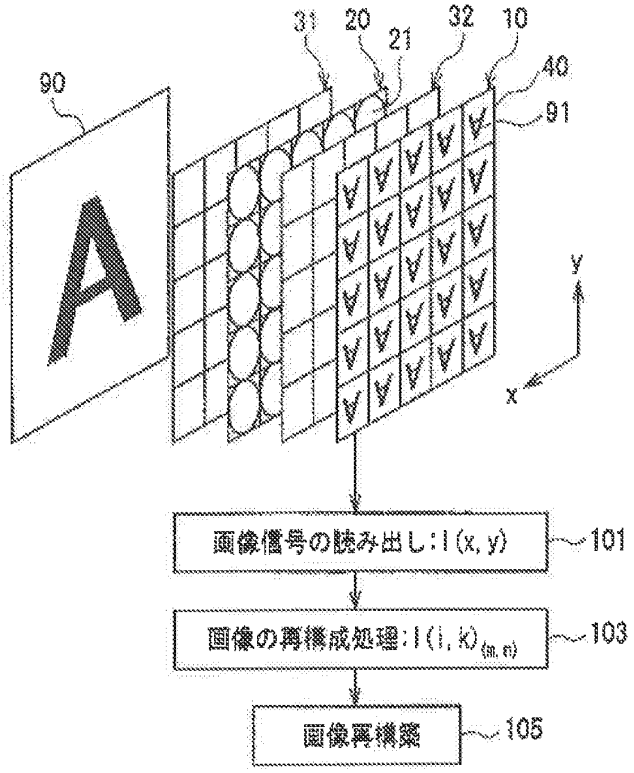

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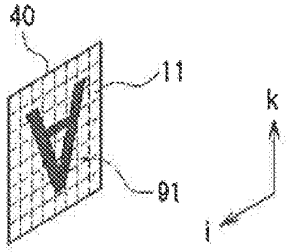

[Drawing 4]

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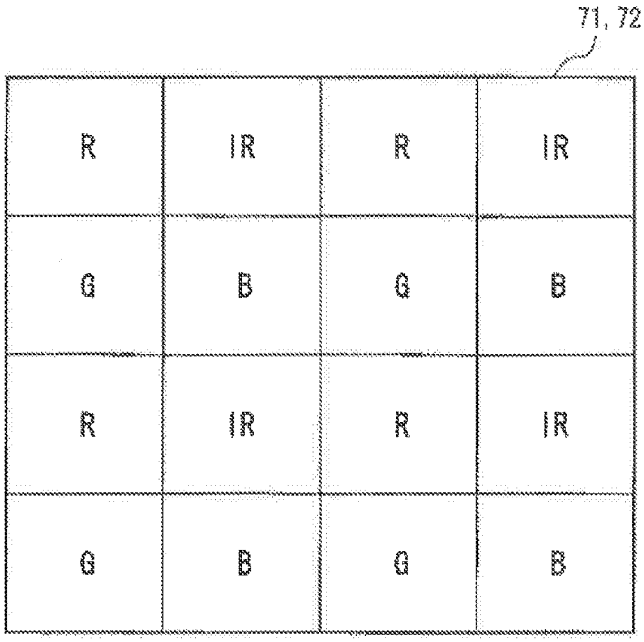

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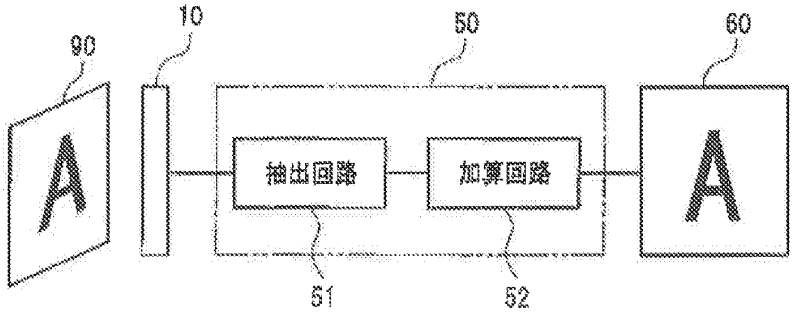

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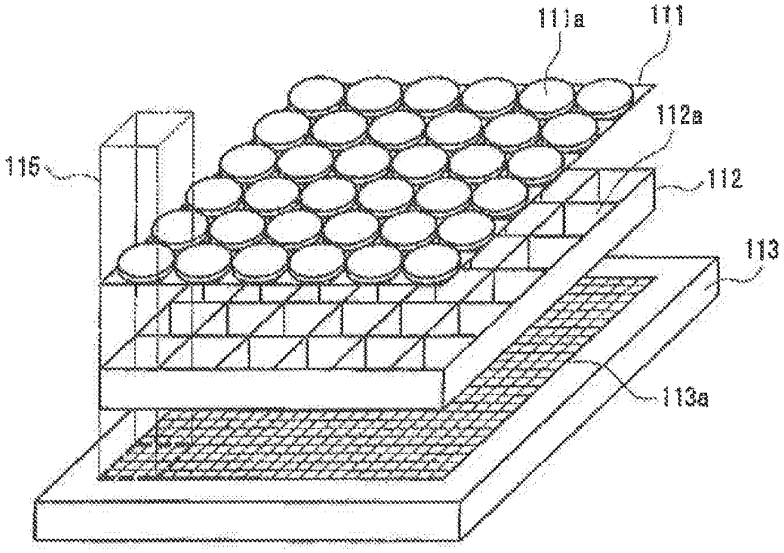
[Drawing 6]



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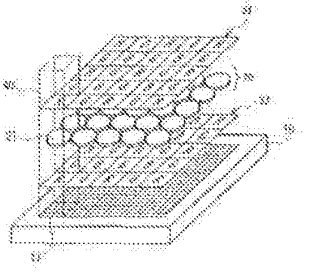
(54)【発明の名称】撮像装置

(57)【要約】
【課題】　クロストークが抑制でき、且つ部品点数や工数が低減された安価な撮像装置を提供する。
【解決手段】　微小レンズアレイ２０の各微小レンズ２１は固体撮像素子１０の複数の画素１１に被写体像を結像する。固体撮像素子１０よりも被写体側に第１カラーフィルタアレイ３１が、第１カラーフィルタアレイ３１と固体撮像素子１０との間に第２カラーフィルタアレイ３２が配置される。第１，第２カラーフィルタアレイ３１，３２は同じ配置の少なくとも２種以上のカラーフィルタを備える。第１，第２カラーフィルタアレイ３１，３２のカラーフィルタと微小レンズ１０とは一対一に対応する。
【選択図】　図１



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【特許請求の範囲】
【請求項１】
第１平面内に配置された光電変換機能を有する多数の画素を備える固体撮像素子と、第２平面内に配置された複数の微小レンズを備える微小レンズアレイとを有し、１つの前記微小レンズに対して複数の前記画素が対応し、それぞれの前記微小レンズが対応する複数の前記画素に被写体像を結像する撮像装置であって、
更に、前記第１平面に対して被写体側の第３平面内に配置された少なくとも２種以上のカラーフィルタを備える第１カラーフィルタアレイと、前記第１カラーフィルタアレイのカラーフィルタと同じ配置で前記第３平面と前記第１平面との間に位置する第４平面内に配置された少なくとも２種以上のカラーフィルタを備える第２カラーフィルタアレイとを有し、
前記第１カラーフィルタアレイの前記カラーフィルタと前記微小レンズ、及び前記第２カラーフィルタアレイの前記カラーフィルタと前記微小レンズとは、いずれも一対一に対応していることを特徴とする撮像装置。
【請求項２】
前記第１カラーフィルタアレイ及び前記第２カラーフィルタアレイは、赤色光を透過するカラーフィルタと、緑色光を透過するカラーフィルタと、青色光を透過するカラーフィルタとを含む請求項１に記載の撮像装置。
【請求項３】
前記第１カラーフィルタアレイ及び前記第２カラーフィルタアレイにおいて、同種のカラーフィルタが相互に隣り合わないように、前記２種以上のカラーフィルタが市松模様状に配置されている請求項１に記載の撮像装置。
【請求項４】
前記第３平面は、前記第２平面に対して被写体側に位置する請求項１に記載の撮像装置。
【請求項５】
前記第３平面は、前記第２平面と前記第４平面との間に位置し、前記第３平面と前記第４平面とが離間している請求項１に記載の撮像装置。
【請求項６】
前記第２カラーフィルタアレイは、固体撮像素子の入射面に近接して、又は前記入射面上に配置されている請求項１に記載の撮像装置。
【請求項７】
前記第１カラーフィルタアレイ及び前記第２カラーフィルタアレイは、赤外光を透過するカラーフィルタ及び／又は紫外光を透過するカラーフィルタを含む請求項１に記載の撮像装置。
【請求項８】
前記固体撮像素子の多数の前記画素からの信号のうち、同種の前記カラーフィルタに対応する前記画素からの信号のみを選択的に抽出する抽出回路を更に備える請求項１に記載の撮像装置。
【請求項９】
前記固体撮像素子がＣＣＤである請求項１に記載の撮像装置。
【請求項１０】
前記固体撮像素子がＣＭＯＳである請求項１に記載の撮像装置。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明は撮像装置に関する。特に、多数の画素を有する固体撮像素子の被写体側の平面内に複数の微小レンズを配列した微小レンズアレイを配置した撮像装置に関する。
【背景技術】
【０００２】

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近年市場規模が大きくなりつつあるデジタルスチルカメラの市場においては、より携帯性に優れた小型・薄型のカメラに対するニーズが高まってきている。信号処理を担うＬＳＩ等の回路部品は、配線パターンの微細化などにより高機能で小型化が進んでいる。また、記録メディアも小型・大容量のものが廉価にて入手できるようになってきている。しかしながら、レンズとＣＣＤやＣＭＯＳなどの固体撮像素子とで構成される撮像系の小型化は未だ十分とは言えず、より携帯性に優れたカメラを実現するためにも小型の撮像系の開発が要望されている。

【０００３】

撮像系の小型化を実現するための構成として、平面上に複数の微小レンズを配列したレンズアレイ光学系を用いた撮像装置が知られている。従来の光軸上に複数のレンズを並べた光学系は、光軸方向に長くなるため体積が増大し、またレンズ径が大きいため収差が大きくなるという問題を有していた。これに対して、レンズアレイ光学系は、光軸方向に薄くでき、かつ個々の微小レンズ径が小さいため収差を比較的小さく抑えることが可能である。

【０００４】

このようなレンズアレイを用いた撮像装置が特許文献１に開示されている。この撮像装置は、図６に示すように、被写体側から順に、複数の微小レンズ１１１ａが同一平面内に配列された微小レンズアレイ１１１と、各微小レンズ１１１ａからの光信号が互いに混信しないように分離するための格子枠状の隔壁１１２ａからなる隔壁層１１２と、多数の光電変換素子１１３ａが同一平面内に配置された受光素子アレイ１１３とを備える。１つの微小レンズ１１１ａと、これに対応する、隔壁１１２ａによって分離された１つの空間と、複数の光電変換素子１１３ａとが、１つの結像ユニット１１５を構成する。個々の結像ユニット１１５において、微小レンズ１１１ａが、対応する複数の光電変換素子１１３ａ上に被写体像を結像する。これにより、結像ユニット１１５ごとに撮影画像が得られる。この撮影画像の解像度は１つの結像ユニット１１５を構成する光電変換素子１１３ａの数（画素数）に依存する。被写体に対する個々の微小レンズ１１１ａの相対的位置が異なることにより、複数の光電変換素子１１３ａ上に形成される被写体像の結像位置が結像ユニット１１５ごとに異なる。その結果、得られる撮影画像は結像ユニット１１５ごとに異なる。この互いに異なる複数の撮影画像を信号処理することにより、一つの画像を得ることができる。

【０００５】

この撮像装置では、個々の結像ユニット１１５を構成する画素数は少ないため、個々の結像ユニット１１５から得られる撮影画像の画質は低いが、複数の結像ユニット１１５においてそれぞれ得られる少しずつずれた撮影画像を用いて信号処理して画像を再構築することにより、多数の光電変換素子で撮影した場合と同等の画質の映像を得ることができる。

【０００６】

図６の撮像装置では、微小レンズ１１１ａからの光がこの微小レンズ１１１ａと対応しない隣の結像ユニット１１５の光電変換素子１１３ａに入射する（この現象を「クロストーク」と呼ぶ）と、高画質の画像を再構築できなかったり、迷光が発生して画質が劣化したり、光損失を生じたりする。従って、クロストークを防止するために、隔壁層１１２が用いられている。特許文献１では、これと同様の効果は、隔壁層１１２に代えて、結像ユニット１１５ごとに偏向方向が直交するように偏向透過フィルタを配置した偏向フィルタアレイを微小レンズアレイ１１１面及び受光素子アレイ１１３面にそれぞれ配置しても得られると記載されている。

【特許文献１】特開２００１－６１１００号公報

【発明の開示】

【発明が解決しようとする課題】

【０００７】

しかしながら、上記の図６の撮像装置に使用される隔壁層１１２は、各結像ユニット１

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１５に対応する隔壁１１２ａを形成するために、ステンレス鋼などを微細加工して高精度に組み立てられて作成される。従って、工程が煩雑で、コスト高となる。また、得られた隔壁層１１２と微小レンズアレイ１１１及び受光素子アレイ１１３とを相対的位置を緻密に管理しながら組み立てる必要があり、組立作業が煩雑となる。

【０００８】

また、隔壁層１１２の代わりに使用される偏向フィルタアレイは、回折格子や屈折型光学素子を用いて作成されるため、部品点数や組み立て工数が増加する。

【０００９】

本発明は、従来の上記の撮像装置が有する問題を解決し、クロストークが抑制でき、且つ部品点数や工数が低減された安価な撮像装置を提供することを目的とする。

【課題を解決するための手段】

【００１０】

本発明の撮像装置は、第１平面内に配置された光電変換機能を有する多数の画素を備える固体撮像素子と、第２平面内に配置された複数の微小レンズを備える微小レンズアレイとを有する。１つの前記微小レンズに対して複数の前記画素が対応し、それぞれの前記微小レンズが対応する複数の前記画素に被写体像を結像する。

【００１１】

本発明の撮像装置は、更に、前記第１平面に対して被写体側の第３平面内に配置された少なくとも２種以上のカラーフィルタを備える第１カラーフィルタアレイと、前記第１カラーフィルタアレイのカラーフィルタと同じ配置で前記第３平面と前記第１平面との間に位置する第４平面内に配置された少なくとも２種以上のカラーフィルタを備える第２カラーフィルタアレイとを有し、前記第１カラーフィルタアレイの前記カラーフィルタと前記微小レンズ、及び前記第２カラーフィルタアレイの前記カラーフィルタと前記微小レンズとは、いずれも一対一に対応している。

【発明の効果】

【００１２】

本発明によれば、同じカラーフィルタ配置を有する第１カラーフィルタアレイと第２カラーフィルタアレイとを備えるので、従来の撮像装置において必須であった隔壁層や偏光フィルタアレイを用いることなく、クロストークの発生を抑制できる。

【００１３】

クロストークを抑制できるので、画質劣化を少なくできること、また、迷光の発生を抑えることができることなどにより、高画質画像を撮影できる。

【００１４】

また、隔壁層や偏光フィルタアレイが不要であるので、組立作業を簡素化でき、また部品点数を削減できるので、安価な撮像装置を提供できる。更に、部品精度や組立精度を向上できるので、高品質の撮像装置を提供できる。

【発明を実施するための最良の形態】

【００１５】

本発明の上記撮像装置において、前記第１カラーフィルタアレイ及び前記第２カラーフィルタアレイは、赤色光を透過するカラーフィルタと、緑色光を透過するカラーフィルタと、青色光を透過するカラーフィルタとを含むことが好ましい。これにより、カラー撮影を行うことができる。

【００１６】

また、前記第１カラーフィルクアレイ及び前記第２カラーフィルクアレイにおいて、同種のカラーフィルタが相互に隣り合わないように、前記２種以上のカラーフィルタが市松模様状に配置されていることが好ましい。これにより、クロストークを低減できる。

【００１７】

また、前記第３平面は、前記第２平面に対して被写体側に位置することが好ましい。これにより、撮像装置の全体の厚みを薄くしながら、第１カラーフィルクアレイと第２カラーフィルタアレイとの間の間隔を比較的大きく確保できるので、クロストークの低減効果

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が向上する。

【００１８】

あるいは、前記第３平面は、前記第２平面と前記第４平面との間に位置し、前記第３平面と前記第４平面とが離間していることが好ましい。この構成でも、第１カラーフィルタアレイと第２カラーフィルタアレイとの間の間隔を確保することによりクロストークを低減することができる。

【００１９】

また、前記第２カラーフィルタアレイは、固体撮像素子の入射面に近接して、又は前記入射面上に配置されていることが好ましい。これにより、第２カラーフィルタアレイと固体撮像素子との間でのクロストークを低減できる。

【００２０】

また、前記第１カラーフィルタアレイ及び前記第２カラーフィルタアレイは、赤外光を透過するカラーフィルタ及び／又は紫外光を透過するカラーフィルタを含んでいても良い。これにより、赤外線及び／又は紫外線による撮影が可能となる。

【００２１】

また、前記固体撮像素子の多数の前記画素からの信号のうち、同種の前記カラーフィルタに対応する前記画素からの信号のみを選択的に抽出する抽出回路を更に備えていても良い。これにより、所望する特定の波長帯の光のみを選択して撮影することが可能となる。

【００２２】

前記固体撮像素子は、ＣＣＤであっても良い。あるいは、ＣＭＯＳであっても良い。

【００２３】

以下、本発明の実施の形態について、図面を参照しながら説明する。

【００２４】

（実施の形態１）

図１は、本発明の実施の形態１の撮像装置の概略構成を示した斜視図である。図２は、本発明の実施の形態１の撮像装置の、微小レンズの光軸を含む面での部分断面図である。図３（Ａ）は、本発明の実施の形態１の撮像装置において、固体撮像素子からの信号の処理の概略を示した図である。図３（Ｂ）は、本発明の実施の形態１の撮像装置において、１つの結像ユニットを構成する受光部を示した斜視図である。

【００２５】

図１から図３において、１０は第１平面内に縦横方向に配列された多数の画素１１を備える固体撮像素子（例えば、ＣＣＤやＣＭＯＳ）、２０は、第１平面と平行で且つ離間した第２平面内に縦横方向に配列された複数の微小レンズ２１を備える微小レンズアレイである。

【００２６】

３１は、第１平面と平行で、且つ第１平面よりも被写体側の第３平面内に縦横方向に配列された複数のカラーフィルタを備える第１カラーフィルタアレイである。３２は、第１平面と平行で、且つ第３平面と第１平面との間に位置する第４平面内に縦横方向に配列された複数のカラーフィルタを備える第２カラーフィルタアレイである。本実施の形態では、第１及び第２カラーフィルタアレイ３１，３２は、赤色光を選択的に透過するカラーフィルタＲと、緑色光を選択的に透過するカラーフィルタＧと、青色光を選択的に透過するカラーフィルタＢとを備え、これらが格子枠状に区分された各領域内に市松模様状に配置されている。第１カラーフィルタアレイ３１と第２カラーフィルタアレイ３２とは、カラーフィルタＲ，Ｇ，Ｂの配置に関して同一である。

【００２７】

１つの微小レンズ２１に対して、第１カラーフィルタアレイ３１を構成する赤・緑・青のうちの何れか一色のカラーフィルタ、第２カラーフィルタアレイ３２を構成する赤・緑・青のうちの何れか一色のカラーフィルタ、及び複数の画素１１が対応し、これらによって１つの結像ユニット４０が構成される。同じ結像ユニット４０を構成する第１カラーフィルタアレイ３１のカラーフィルタの色と第２カラーフィルタアレイ３２のカラーフィル

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タの色とは一致する。

【００２８】

被写体からの光束は、第１カラーフィルタアレイ３１にて赤緑青の何れかの色光のみが選択されてこれを透過し、複数の微小レンズ２１に入射する。各微小レンズ２１は、対応する複数の画素１１上に被写体像を形成する。微小レンズ２１を出射した赤緑青の何れかの色光は、画素１１に達する前に、第２カラーフィルタアレイ３２に入射する。第２カラーフィルタアレイ３２の各カラーフィルタは、入射光のうち、自身のカラーフィルタの色と同じ色光のみを透過させる。

【００２９】

本実施の形態の撮像装置は、上記の構成によりクロストークを防止できる。これを図２を用いて説明する。

【００３０】

例えば、被写体からの光線Ｒ１は、第１カラーフィルタアレイ３１の赤色のカラーフィルタＲに入射して、赤色の波長帯の光のみがこれを通過し、微小レンズ２１を通過後、第２カラーフィルタアレイ３２の赤色のカラーフィルタＲに入射する。この入射光は赤色の波長帯の光であるから、このカラーフィルタＲを通過することができ、画素１１上に赤色の被写体像を形成する。

【００３１】

一方、光線Ｒ１よりも大きな入射角で撮像装置に入射する被写体からの光線Ｒ２は、第１カラーフィルタアレイ３１の赤色のカラーフィルタＲに入射して、赤色の波長帯の光のみがこれを通過し、微小レンズ２１を通過後、第２カラーフィルタアレイ３２の隣の結像ユニットを構成する緑色のカラーフィルタＧに入射する。緑色のカラーフィルタＧはこの赤色の波長帯の入射光を通過させない。従って、光線Ｒ２を構成する如何なる波長帯の光も画素１１に達しない。

【００３２】

このように、本発明の撮像装置は、各結像ユニット４０が同一色のカラーフィルタを光軸方向に２層備えている。更に、第１及び第２カラーフィルタアレイ３１，３２では色の異なるカラーフィルタＲ，Ｇ，Ｂが市松模様を構成するように配置されている。即ち、任意の１つのカラーフィルタの色と、このカラーフィルタの４つの辺を挟んで縦横方向に隣り合う４つのカラーフィルタの色とが異なるように、カラーフィルタＲ，Ｇ，Ｂが配置されている。この結果、上記光線Ｒ２のように、第１カラーフィルタアレイ３１を通過後、第２カラーフィルタアレイ３２に入射するまでの間に縦横方向に隣り合う結像ユニット４０間の境界を越える光線は第２カラーフィルタアレイ３２を通過することができない。従って、クロストークの発生を防止することができる。これにより、画質劣化を少なくでき、また、迷光の発生を抑えることができる。この結果、高画質画像を撮影することができる。

【００３３】

更に、ＣＣＤや液晶表示素子に使用されるカラーフィルタにおいて汎用されているカラーフィルタアレイと同様にして、例えば第１カラーフィルタアレイ３１を微小レンズアレイ２０上に、第２カラーフィルタアレイ３２を固体撮像素子１０上に、それぞれ形成すれば良く、上述した従来の撮像装置の隔壁や偏向フィルタアレイに比べて製造を格段に簡単化でき、また、部品点数も削減できる。更に、第１及び第２カラーフィルタアレイ３１，３２自身の精度や微小レンズアレイ２０及び固体撮像素子１０に対する精度も従来に比べて向上できるので、品質が向上し且つ安定する。

【００３４】

上記の実施の形態では、第１カラーフィルタアレイ３１は微小レンズアレイ２０よりも被写体側に、第２カラーフィルタアレイ３２は微小レンズアレイ２０と固体撮像素子１０との間に配置されているが、第１及び第２カラーフィルタアレイ３１，３２の配置は、クロストークの発生が抑制できればこれに限定されない。例えば、第１カラーフィルタアレイ３１及び第２カラーフィルタアレイ３２を微小レンズアレイ２０と固体撮像素子１０と

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の間に配置しても良い。この場合、第１カラーフィルタアレイ３１と第２カラーフィルタアレイ３２とは光軸方向に所定の距離だけ離間させることが好ましい。両者が近接していると、入射角が大きな光線は隣り合う結像ユニット４０間の境界を越えてしまうので、２枚のカラーフィルタアレイ３１、３２を用いたことが実質的に無意味となる。

【００３５】

但し、第１カラーフィルタアレイ３１、第２カラーフィルタアレイ３２、及び微小レンズアレイ２０の配置順序にかかわらず、第１カラーフィルタアレイ３１よりも固体撮像素子１０寄りに配置される第２カラーフィルタアレイ３２は、固体撮像素子１０の入射面に近接して、又は固体撮像素子１０の入射面上に配置されていることが好ましい。これにより、第２カラーフィルタアレイ３２を通過した光線が、隣り合う結像ユニット４０間の境界を越えた後、固体撮像素子１０に入射するのを低減することができる。即ち、第２カラーフィルタアレイ３２と固体撮像素子１０との間でのクロストークの発生を低減できる。

【００３６】

次に、固体撮像素子１０の各受光部１１に入射した光束から画像を得る方法を図３（Ａ）及び図３（Ｂ）を用いて説明する。

【００３７】

図３（Ａ）に示すように、結像ユニット４０ごとに、微小レンズアレイ２０の微小レンズ２１は、被写体９０の像９１を固体撮像素子１０上に結像する。固体撮像素子１０の各受光部（画素）１１は入射した光束を光電変換する。ここで、固体撮像素子１０の水平軸をｘ軸、垂直軸をｙ軸とし、位置（ｘ，ｙ）にある受光部１１からの信号をＩ（ｘ，ｙ）とすると、固体撮像素子１０に含まれる全ての受光部１１についての信号Ｉ（ｘ，ｙ）が読み出される（ステップ１０１）。

【００３８】

次に、この各受光部１１からの信号Ｉ（ｘ，ｙ）を結像ユニット４０ごとに分割する。即ち、図３（Ｂ）に示すように、受光部１１がｍ列×ｎ行に配置された結像ユニット４０内の第ｉ列、第ｋ行の位置にある受光部１１の位置を$(i, k)_{(s,t)}$とし、この受光部１１からの信号を$I(i, k)_{(s,t)}$とすると、上記各信号Ｉ（ｘ，ｙ）を結像ユニット４０内における信号$I(i, k)_{(s,t)}$として取り扱う。この結果、結像ユニット４０ごとにｍ列×ｎ行の画素からなる画像が再構成される（ステップ１０３）。

【００３９】

その後、異なる結像ユニット４０間において、信号$I(i, k)_{(s,t)}$を処理して１枚の画像を再構築する（ステップ１０５）。この信号処理としては、上記特許文献１に記載された方法を用いることができ、その詳細説明を省略する。結像ユニット４０内における被写体像９１の形成位置が結像ユニット４０ごとに異なるために、位置（ｉ，ｋ）が同じ受光部１１からの信号$I(i, k)_{(s,t)}$は結像ユニット４０ごとに異なる。従って、１つの結像ユニット４０に含まれる受光部１１の数（ｍ×ｎ個）を遙かに超えた高解像度の画像が得られる。

【００４０】

（実施の形態２）

図４は、本発明の実施の形態２に係る撮像装置に搭載される第１，第２カラーフィルタアレイ７１，７２のカラーフィルタの配置を示した正面図である。図５は、本発明の実施の形態２に係る撮像装置において固体撮像素子からの信号の処理の流れを示したブロック図である

本実施の形態の撮像装置は、実施の形態１で示した３種のカラーフィルタＲ，Ｇ，Ｂを備える第１，第２カラーフィルタアレイ３１，３２に代えて、図４に示す第１，第２カラーフィルタアレイ７１，７２が使用される。この第１，第２カラーフィルタアレイ７１，７２は、実施の形態１で示した第１，第２カラーフィルタアレイ３１，３２と同様に、赤色光を選択的に透過するカラーフィルタＲ，緑色光を選択的に透過するカラーフィルタＧ、及び青色光を選択的に透過するカラーフィルタＢに加えて、更に赤外光を選択的に透過するカラーフィルタＩＲを備える。この４種のカラーフィルタＲ，Ｇ，Ｂ，ＩＲが，結像

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ユニット４０に対応して格子枠状に区分された各領域内に市松模様状に配置されている。実施の形態１と同様に、隣り合うカラーフィルタの色は同一ではない。これにより、実施の形態１で説明したのと同様に、第１カラーフィルタアレイ７１を通過後、第２カラーフィルタアレイ７２に入射するまでの間に隣り合う結像ユニット４０間の境界を越える光線は第２カラーフィルタアレイ７２を通過することができない。従って、クロストークの発生を防止することができる。

【００４１】

更に、本実施の形態２では、このような撮像装置からの出力信号は図５に示す映像回路５０により以下のように処理される。即ち、固体撮像素子１０の各受光部１１は被写体９０の光信号を光電変換し、出力する。映像回路５０内の抽出回路５１は、固体撮像素子１０からの信号のうち、カラーフィルタの色が同一である結像ユニット４０に含まれる受光部１１からの信号を選択的に抽出する。加算回路５２は、抽出回路５１で抽出された単色の信号に対して図３（Ａ）及び図３（Ｂ）で説明した処理を行い単色の高解像度の画像を再構築する。

【００４２】

例えば、抽出回路５１が、固体撮像素子１０からの信号のうち、赤、緑、青の３色のカラーフィルタＲ，Ｇ，Ｂに対応する結像ユニット４０からの信号を抽出すると、加算回路５２は、赤、緑、青の３色の画像を再構築する。この３色の画像を合成すれば、表示装置６０にカラー画像を表示することができる。

【００４３】

また、抽出回路５１が、固体撮像素子１０からの信号のうち、赤外光のカラーフィルタＩＲに対応する結像ユニット４０からの信号のみを抽出すると、加算回路５２は、赤外光の画像を再構築する。従って、表示装置６０に赤外線撮影画像を表示することができる。

【００４４】

このように、本実施の形態によれば、第１，第２カラーフィルタアレイ７１，７２がカラーフィルタＲ，Ｇ，Ｂに加えてカラーフィルタＩＲを備えているために、実施の形態１と同様にカラー撮影を行うことができるのはもちろん、夜間などの肉眼では視認できない暗闇での赤外線撮影も行うことができる。

【００４５】

もちろん、抽出回路５１が、赤、緑、青の３色のうちの任意の１色又は２色に対応する結像ユニット４０からの信号のみを抽出して、所望する色の画像を得ることも可能である。

【００４６】

本実施の形態２では、第１，第２カラーフィルタアレイ７１，７２が赤外光を選択的に透過するカラーフィルタＩＲを備えていたが、カラーフィルタＩＲに代えて、又はこれに加えて紫外光を選択的に透過するカラーフィルタを備えていても良い。また、赤外光や紫外光以外の特定の波長帯の光のみを透過させるカラーフィルタを備えていても良い。

【産業上の利用可能性】

【００４７】

本発明の撮像装置の利用分野は特に制限はないが、小型・薄型でありながら高解像度画像を得ることができるので、例えばデジタルスチルカメラ、携帯電話、ノート型パソコン、ＰＤＡなどの各種携帯型情報端末などに利用することができる。

【図面の簡単な説明】

【００４８】

【図１】図１は、本発明の実施の形態１の撮像装置の概略構成を示した分解斜視図である。

【図２】図２は、本発明の実施の形態１の撮像装置の、微小レンズの光軸を含む面での断面図である。

【図３】図３（Ａ）は、本発明の実施の形態１の撮像装置において、固体撮像素子からの信号の処理の概略を示した図である。図３（Ｂ）は、本発明の実施の形態１の撮像装置に

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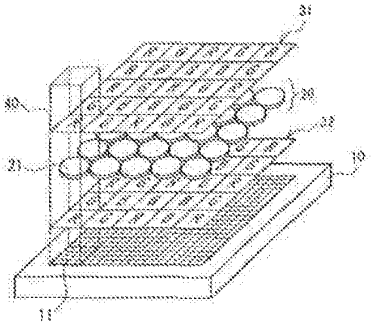
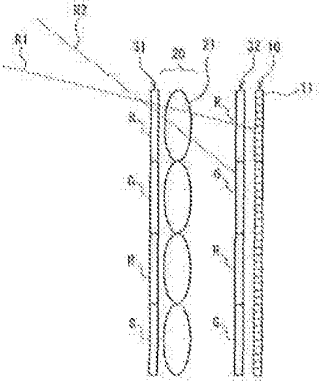
おいて、１つの結像ユニットを構成する受光部を示した斜視図である。
【図４】図４は、本発明の実施の形態２の撮像装置におけるカラーフィルタアレイを示した正面図である。
【図５】図５は、本発明の実施の形態２の撮像装置において固体撮像素子からの信号の処理の概略を示したブロック図である。
【図６】図６は、従来の撮像装置の概略構成を示した分解斜視図である。
【符号の説明】
【００４９】
１０　固体撮像素子
１１　画素
２０　微小レンズアレイ
２１　微小レンズ
３１，７１　第１カラーフィルタアレイ
３２，７２　第２カラーフィルタアレイ
４０　結像ユニット
５０　映像回路
５１　抽出回路
５２　加算回路
６０　表示装置
９０　被写体

【図１】



【図２】



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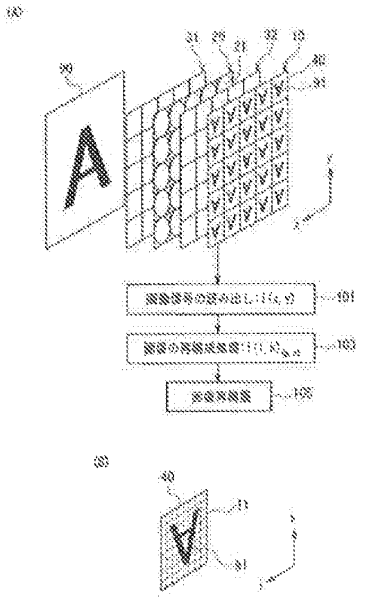
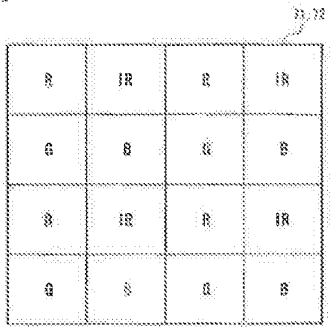
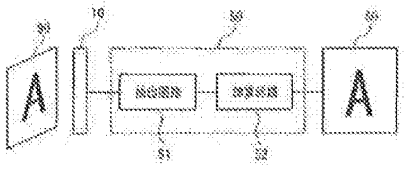
【図３】



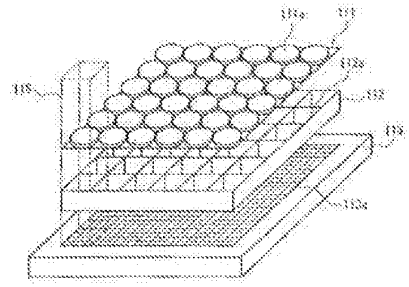
【図４】



【図５】



【図６】



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METHOD FOR MANUFACTURING PHOTOELECTRIC CONVERSION DEVICE

Inventor(s): ARAI YASUYUKI ± (ARAI YASUYUKI)

Applicant(s): SEMICONDUCTOR ENERGY LAB ± (SEMICONDUCTOR ENERGY LAB CO LTD)

Classification: - international:***H01L31/04***
- cooperative: **H01L31/02168**; **H01L31/0236**; **H01L31/0725**; **H01L31/1864**; H01L31/022425; H01L31/028; H01L31/036; H01L31/03682; H01L31/1804; Y02E10/50; Y02P70/521

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Abstract of JP2009152569 (A)

PROBLEM TO BE SOLVED: To provide a method for manufacturing a photoelectric conversion device typified by a solar cell, having an excellent photoelectric conversion characteristic by effectively utilizing a silicon semiconductor material. ;SOLUTION: The surface of a single crystal semiconductor layer bonded to a supporting substrate is irradiated with a pulsed laser beam to make the surface rough. The single crystal semiconductor layer bonded to the supporting substrate is irradiated with the pulsed laser beam in an atmosphere containing an inert gas such as nitrogen and oxygen so that the surface thereof is made rough. With roughness on the surface of the single crystal semiconductor layer, light reflection is suppressed, so that an effect for trapping incident light can be displayed. Accordingly, even when the thickness of the single crystal semiconductor layer is equal to or greater than 0.1 to 10 [mu]m, the optical path length of incident light is substantially increased and the amount of light absorption can be increased. ;COPYRIGHT: (C)2009,JPO&INPIT

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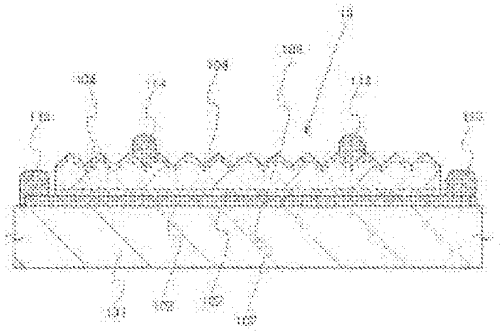

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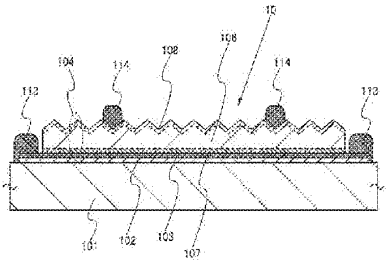
(54)【発明の名称】光電変換装置の製造方法

(57)【要約】
【課題】シリコン半導体材料を有効に利用して光電変換特性に優れた、太陽電池に代表される光電変換装置の製造方法を提供する。
【解決手段】支持基板に接合させた単結晶半導体層の表面にパルスレーザビームを照射して、該単結晶半導体層の表面を凹凸化させることを要旨とする。支持基板に接合した単結晶半導体層に、窒素等の不活性気体と酸素を含む雰囲気中でパルスレーザビームを照射して単結晶半導体層の表面を凹凸化する。結晶半導体層の表面に凹凸構造があることにより光の反射が抑えられ、入射した光を閉じ込める効果を奏する。それにより、単結晶半導体層の厚さが、０．１μｍ～１０μｍ以下であっても入射光の光路長が実質的に増大し、光の吸収量を増やすことができる。
【選択図】図２



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【特許請求の範囲】
【請求項1】
一面に一導電型の第１不純物半導体層、前記第１不純物半導体層に接する電極、及び質量が水素分子よりも重い水素のクラスターイオンを７０％以上含むイオンビームを一面から注入することによって形成される損傷層を有する単結晶半導体基板と、絶縁表面を有する支持基板と、を接合層を介して接着し、
熱処理を行うことにより、前記損傷層を劈開させ、前記単結晶半導体基板から単結晶半導体層を分離し、前記支持基板上に前記単結晶半導体層を残存させたまま前記単結晶半導体基板を除去し、
不活性気体及び酸素を含む雰囲気中で、前記単結晶半導体層の劈開面にパルスレーザビームを照射して、前記単結晶半導体層の表面を凹凸化し、
前記単結晶半導体層の劈開面側に、前記一導電型とは逆の導電型の第２不純物半導体層を形成すること
を特徴とする光電変換装置の製造方法。
【請求項2】
請求項１において、
前記第２不純物半導体層の上に、前記一導電型の第３不純物半導体層、非単結晶半導体層、及び前記一導電型とは逆の導電型の第４不純物半導体層を堆積すること
を特徴とする光電変換装置の製造方法。
【請求項3】
請求項１又は２において、
前記不活性気体及び酸素を含む雰囲気における酸素濃度は、０．１体積％乃至２５体積％であること
を特徴とする光電変換装置の製造方法。
【請求項4】
請求項１乃至３のいずれか一項において、前記パルスレーザビームの照射時に照射領域の前記単結晶半導体層が、２５０℃から６００℃の温度に加熱されていること
を特徴とする光電変換装置の製造方法。
【請求項5】
請求項１乃至４のいずれか一項において、前記クラスターイオンが、H_3^+であること
を特徴とする光電変換装置の製造方法。
【請求項6】
請求項１乃至５のいずれか一項において、前記損傷層は、前記単結晶半導体基板の表面から１０μｍ未満の深さに形成されること
を特徴とする光電変換装置の製造方法。

【発明の詳細な説明】
【技術分野】
【0001】
単結晶又は多結晶半導体を用いた光電変換装置の製造方法に関する。
【背景技術】
【0002】
太陽電池の全世界生産量は、２００５年において１，７５９ＭＷが報告されており、対前年度比で１４７％の増加である。この太陽電池の生産量の大部分は、単結晶シリコン太陽電池又は多結晶シリコン太陽電池で占められている。
【0003】
シリコン半導体は、太陽電池産業だけでなく、メモリやマイクロプロセッサーなどの半導体産業でも広く使われる資源である。そのため、太陽電池の生産量が年々増加するにつれ、シリコンの原料である多結晶シリコンの供給不足と、それによるシリコンウエハの価格の高騰が産業界の問題となっている。
【0004】

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ところで、シリコンを材料とする結晶系太陽電池は、太陽光を吸収するために１０μｍ程度の厚さがあれば十分であるが、実際のシリコンウエハは２００μｍから３００μｍ程度の厚さを有している。つまり、結晶系太陽電池では光電変換に必要な厚さよりも１０倍以上厚く形成されていることになり、シリコンウエハを有効利用しているとは言い難い状況にある。極端に言えば、シリコンウエハの殆どは太陽電池の形状を維持するための構造体として機能しているにすぎない。

【0005】

上記のように、十分厚いシリコンウエハを使いながらも、結晶系太陽電池では入射光を有効利用するために光閉じこめ用の表面凹凸構造が設けられている。表面凹凸構造は、ＮａＯＨ、ＫＯＨなどアルカリ溶液のエッチング速度がシリコンの結晶面方位によって違う性質を利用して形成している。しかし、アルカリ溶液のエッチングでは理想的な表面凹凸構造を形成するのは難しいことから、レーザ加工技術と化学エッチングを組み合わせた方法が開示されている（例えば、特許文献１参照）。

【特許文献1】特開２００３－２５８２８５号公報

【発明の開示】

【発明が解決しようとする課題】

【0006】

上記のように、太陽電池の生産量は、原材料である多結晶シリコンの生産量に律速されている。すなわち、生産能力に余裕があっても、原材料が足りなくなって、供給が需要に追いつかないといった問題が顕在化している。或いは、シリコンウエハの調達コストが増大して、太陽電池の生産工場の収益を悪化させることが問題となっている。

【0007】

このような状況に鑑み、シリコン半導体材料を有効に利用して光電変換特性に優れた、太陽電池に代表される光電変換装置の製造方法を提供することを目的の一とする。

【課題を解決するための手段】

【0008】

本発明は光電変換装置に係り、支持基板に接合させた単結晶半導体層の表面にパルスレーザビームを照射して、該単結晶半導体層の表面を凹凸化させることを要旨とする。

【0009】

この光電変換装置の製造方法には、次に示す処理が含まれている。一面に一導電型の第１不純物半導体層、該第１不純物半導体層に接する電極、及び質量が水素分子よりも重い水素のクラスターイオンを７０％以上含むイオンビームを一面から注入することによって形成される損傷層を有する単結晶半導体基板と、絶縁表面を有する支持基板と、を接合層を介して接着する。熱処理を行い、損傷層を劈開させ、単結晶半導体基板から単結晶半導体層を分離し、支持基板上に単結晶半導体層を残存させる。単結晶半導体層の劈開面に、不活性気体と酸素を含む雰囲気中でパルスレーザビームを照射して単結晶半導体層の表面を凹凸化する。単結晶半導体層の劈開面側に、一導電型とは逆の導電型の第２不純物半導体層を形成する。

【0010】

その後、第２不純物半導体層の上に、一導電型の第３不純物半導体層、非単結晶半導体層及び一導電型とは逆の導電型の第４不純物半導体層を堆積する場合も含む。

【発明の効果】

【0011】

本発明によれば、支持基板上に接合した単結晶半導体層に、酸素を含む雰囲気中でレーザビームを照射することにより、該単結晶半導体層の表面を凹凸化することができる。それにより、単結晶半導体層の表面反射率を低減することができる。この単結晶半導体層を光電変換層とすることで、光閉じ込め効果が発揮され、変換効率を向上させることができる。

【発明を実施するための最良の形態】

【0012】

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本発明の実施の形態について、図面を用いて以下に説明する。但し、本発明は以下の説明に限定されず、本発明の趣旨及びその範囲から逸脱することなくその形態及び詳細をさまざまに変更し得ることは当業者であれば容易に理解される。従って、本発明は以下に示す実施の形態の記載内容に限定して解釈されるものではない。以下に説明する本発明の構成において、同じものを指す符号は異なる図面間で共通して用いる。

【0013】

（実施形態１）

単結晶半導体基板から薄い単結晶半導体層を分離して、絶縁表面を有する基板若しくは絶縁性の支持基板に該単結晶半導体層を転置して光電変換装置を製造する方法について図面を参照して説明する。

【0014】

図１は本形態に係る光電変換装置１０の平面図を示す。この光電変換装置１０は、支持基板１０１上に固着された単結晶半導体層１０６に光が入射することで光電効果を発現する。単結晶半導体層１０６には、内蔵電界を形成するための不純物半導体層が形成されている。単結晶半導体層１０６としては、代表的には単結晶シリコンが適用される。また、単結晶半導体層１０６に代えて多結晶半導体層を適用することができる。この場合、多結晶シリコンが適用される。

【0015】

図１では、単結晶半導体層１０６の表面側に、網状の第２補助電極１１４が設けられ、裏面側に第１電極（平面図では表示されない）が設けられている。第１補助電極１１３は裏面に設けられる第１電極と接続する電極である。本形態の光電変換装置１０は、絶縁表面を有する支持基板１０１に単結晶半導体層１０６が接着される構成なので、正極とそれに対する負極の電極は、支持基板１０１の同じ面に配設されている。

【0016】

図１のＡ－Ｂ切断線に対応する光電変換装置１０の断面構造を図２に示す。図２は、支持基板１０１に単結晶半導体層１０６が接合された光電変換装置を示す。支持基板１０１は絶縁表面を有する基板若しくは絶縁基板であり、例えば、アルミノシリケートガラス、アルミノホウケイ酸ガラス、バリウムホウケイ酸ガラスのような電子工業用に使われる各種ガラス基板が適用される。

【0017】

支持基板１０１と単結晶半導体層１０６の間には絶縁層１０２が設けられている。絶縁層１０２と単結晶半導体層１０６の間には第１電極１０３が設けられている。絶縁層１０２は支持基板１０１と接合しており、さらに第１電極１０３と密着していることにより、単結晶半導体層１０６が支持基板１０１上に固定される。絶縁層１０２は、支持基板１０１と接合するために、平滑面を有し親水性表面を有している絶縁膜で形成される。

【0018】

単結晶半導体層１０６は、代表的には単結晶シリコンが適用される。また、単結晶半導体層に代えて多結晶半導体層（代表的には多結晶シリコン）を適用することもできる。一導電型の第１不純物半導体層１０７と、一導電型とは逆の導電型の第２不純物半導体層１０８は、所定の元素を単結晶半導体層１０６に添加することにより形成される。第１不純物半導体層１０７をｐ型とする場合、第２不純物半導体層１０８はｎ型であり、その逆の選択も可能である。ｐ型不純物元素としては硼素などの元素周期表第１３族の元素が適用され、ｎ型不純物元素としてはリン、砒素など元素周期表第１５族の元素が適用される。不純物元素の添加は、イオン注入若しくはイオンドーピングで行うことができる。本明細書では、イオン注入とはイオン化したガスを質量分離して半導体に注入する方式を指し、イオンドーピングとはイオン化したガスを質量分離せず半導体に注入する方式をいう。

【0019】

単結晶半導体層１０６に第１不純物半導体層１０７と第２不純物半導体層１０８を形成することにより内蔵電界が形成され、光照射により起電力を発生させることができる。すなわち、単結晶半導体層１０６に第１不純物半導体層１０７と第２不純物半導体層１０８で

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ユニットセル（以下、第１ユニットセル１０４ともいう）を形成していることになる。なお、単結晶半導体層１０６にｐ型若しくはｎ型の単結晶半導体が適用される場合、第１不純物半導体層１０７は省略することが可能である。

【0020】

単結晶半導体層１０６は単結晶半導体基板を薄片化して形成される。例えば、単結晶半導体基板として単結晶シリコンウエハを用い、所定の深さに水素イオンを高濃度に注入し、その後、熱処理を行って表層の単結晶シリコン層を分離する水素イオン注入分離法で単結晶半導体層１０６を形成する。また、ポーラスシリコン上に単結晶半導体をエピタキシャル成長させた後、ポーラスシリコン層をウオータージェットで劈開して分離する方法を適用しても良い。単結晶半導体基板として、代表的には単結晶シリコンウエハが適用される。単結晶半導体層１０６の厚さは０．１μｍ以上、１０μｍ以下、好ましくは１μｍ以上５μｍ以下とする。単結晶半導体層１０６として単結晶シリコン半導体を適用する場合には、エネルギーギャップが１．１２ｅＶであり、間接遷移型の半導体であることから、太陽光を吸収するためにはこのような厚さが要求される。

【0021】

単結晶半導体層１０６の表面は凹凸構造を有している。この凹凸構造は、最大高低差（Ｐ－Ｖ）で３００ｎｍ～５００ｎｍの値を有している。なお、ここでいう山谷の最大高低差とは、山頂と谷底の高さの差を示す。また、ここでいう山頂と谷底とはＪＩＳ　Ｂ０６０１で定義されている「山頂」「谷底」を三次元に拡張したものであり、山頂とは指定面の山において最も標高の高いところ、谷底とは指定面の谷において最も標高の低いところと表現される。この単結晶半導体層１０６の表面における凹凸構造は、酸素を含む雰囲気中でパルスレーザビームを照射することにより調整されている。

【0022】

第１電極１０３は、単結晶半導体層１０６の周辺端部領域で第１補助電極１１３と接触し、第２補助電極１１４は第２不純物半導体層１０８と接触している。この構成により、単結晶半導体層１０６の凹凸構造を有する面から光が入射することにより、第１電極１０３（第１補助電極１１３）と第２補助電極１１４の間に起電力が発生する。このとき、単結晶半導体層１０６の表面に凹凸構造があることにより光の反射が押さえられ、単結晶半導体層１０６に入射した光を閉じ込める効果を奏する。それにより、単結晶半導体層１０６の厚さが、０．１μｍ以上、１０μｍ以下、好ましくは１μｍ以上５μｍ以下であっても入射光の光路長が実質的に増大し、光の吸収量を増やすことができる。すなわち、単結晶半導体層１０６に形成された凹凸構造は、光電変換装置１０の変換効率を向上させる作用を奏する。

【0023】

図３はタンデム型光電変換装置２０を示す。図２で示す第１ユニットセル１０４上に第２ユニットセル１０５を積層したものである。第２ユニットセル１０５は、非単結晶半導体層１０９を用いて作製される。非単結晶半導体層１０９は、代表的には非晶質半導体である非晶質シリコンが適用される。また、非晶質シリコンに代えて非晶質シリコンゲルマニウムを適用してもよいし、非単結晶半導体層１０９に微結晶半導体層（代表的には微結晶シリコン）を適用することも可能である。一導電型の第３不純物半導体層１１０と、一導電型とは逆の導電型の第４不純物半導体層１１１は所定の不純物元素を含んで形成された非晶質半導体層又は微結晶半導体層で作製される。代表的には、所定の不純物元素を含んだ非晶質シリコン又は微結晶シリコンであり、その他、所定の不純物元素を含んだ非晶質シリコンカーバイトが適用される。第３不純物半導体層１１０をｐ型とする場合、第４不純物半導体層１１１はｎ型であり、その逆の選択も可能である。

【0024】

非単結晶半導体層１０９は、半導体材料ガスを含む反応性ガスを電磁エネルギーにより分解して形成する。半導体材料ガスとしては、シラン若しくはジシランに代表されるシリコンの水素化物であり、その他シリコンのフッ化物又はシリコンの塩化物によるガスを用いる。このような半導体材料ガス、又は半導体材料ガスに水素、不活性ガスを混合して反応

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性ガスとして用いる。非単結晶半導体層１０９は、この反応性ガスを用い、電磁エネルギーとして、１０ＭＨｚから２００ＭＨｚの高周波電力を印加して薄膜の形成を行うプラズマＣＶＤ法により形成する。電磁エネルギーとしては、高周波電力に代えて１ＧＨｚから５ＧＨｚ、代表的には２．４５ＧＨｚのマイクロ波電力を印加しても良い。第３不純物半導体層１１０及び第４不純物半導体層１１１も同様にプラズマＣＶＤ法で形成されるものであり、前記した反応性ガスに、ｐ型化する場合には不純物としてジボランを、ｎ型化する場合には不純物としてフォスフィンを添加して成膜を行う。非単結晶半導体層１０９として、代表的には非晶質シリコン層が適用される。非単結晶半導体層１０９の厚さは５０ｎｍ以上、３００ｎｍ以下、好ましくは１００ｎｍ以上、２００ｎｍ以下とする。非単結晶半導体層１０９として非晶質シリコン半導体を適用する場合には、エネルギーギャップが１．７５ｅＶであり、この厚さにすることで、６００ｎｍよりも短い波長領域の光を吸収して光電変換することができる。

【0025】

第２ユニットセル１０５の非単結晶半導体層１０９において、微結晶半導体層（代表的には微結晶シリコン層）を適用することもできる。微結晶半導体層を形成するために用いられる代表的な半導体材料ガスは、シラン（SiH_4）であり、その他にもジシラン（Si_2H_6）が適用される。また、シラン（SiH_4）にジクロロシラン（SiH_2Cl_2）、トリクロロシラン（$SiHCl_3$）、テトラクロロシラン（$SiCl_4$）、テトラフルオロシラン（SiF_4）などを適宜混合して用いても良い。この半導体材料ガスを水素若しくはフッ素、水素若しくはフッ素とヘリウム、アルゴン、クリプトン、ネオンから選ばれた一種または複数種の希ガス元素で希釈して用いることで微結晶半導体層をプラズマＣＶＤ法で作製する。希釈率は１０倍～３０００倍の範囲で半導体材料ガスを希釈することが好ましい。成膜は、概略０．１Ｐａ～１３３Ｐａの減圧下で生成されるグロー放電プラズマで成膜が行われる。プラズマを形成するための電力は１０ＭＨｚから２００ＭＨｚの高周波電力又は、高周波電力に代えて１ＧＨｚから５ＧＨｚ、代表的には２．４５ＧＨｚのマイクロ波電力が印加される。また、半導体材料ガス中に、メタン（CH_4）、エタン（C_2H_6）などの炭化物気体、ゲルマン（GeH_4）、四フッ化ゲルマニウム（GeF_4）などのゲルマニウム化気体を混入させて、エネルギーバンド幅を１．５～２．４ｅＶ、若しくは０．９～１．１ｅＶに調節しても良い。微結晶半導体層は格子歪みを有し、該格子歪みにより光学特性が、単結晶シリコンの間接遷移型から直接遷移型に変化する。少なくとも１０％の格子歪みにより、光学特性が直接遷移型に変化するが、局部的な歪みが存在することにより、直接遷移と間接遷移の混在した光学特性を呈する。微結晶シリコン層では、エネルギーギャップが概略１．４５ｅＶであり、単結晶シリコンよりもエネルギーギャップが広がるので、６００ｎｍよりも短い波長領域の光を吸収して光電変換することができる。

【0026】

本形態の光電変換装置は、第２電極１１２側から光を入射する構成である。第２電極１１２は、酸化インジウムスズ、酸化スズ、酸化亜鉛などの透明導電材料を用いて形成する。第１電極１０３は、チタン、モリブデン、タングステン、タンタル、クロム、ニッケルから選択された金属材料で形成する。また、第１電極１０３は、チタン、モリブデン、タングステン、タンタルの窒化物層を有し、該窒化物層が第１不純物半導体層１０７と接触する構成とする。半導体層と金属層の間に金属窒化物を介在させることにより、密着性を向上させることができる。

【0027】

第２ユニットセル１０５は、単結晶半導体層１０６の凹凸表面上に形成されることにより、その凹凸構造の影響を受けて、第２電極１１２の表面も凹凸化される。第２電極１１２の表面が凹凸化されていることにより、入射光の反射が低減する。すなわち、光入射側から下層に位置する単結晶半導体層１０６の凹凸構造と互いに作用しあって、第１ユニットセル１０４と第２ユニットセル１０５に光閉じ込め効果を発現させることができる。この効果により、タンデム型光電変換装置２０の変換効率を向上させることができる。

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【0028】
図４は、エネルギーギャップ１．１２ｅＶの単結晶半導体層１０６を有する第１ユニットセル１０４と、エネルギーギャップ１．７５ｅＶの非単結晶半導体層１０９を有する第２ユニットセル１０５を用いた場合のエネルギーバンド図を示す。光入射側にエネルギーギャップの広い非単結晶半導体層１０９を有する第２ユニットセル１０５が位置しており、その後方にエネルギーギャップの狭い単結晶半導体層１０６を有する第１ユニットセル１０４が配置している。なお、第１不純物半導体層１０７と第３不純物半導体層１１０はｐ型半導体、第２不純物半導体層１０８と第４不純物半導体層１１１はｎ型半導体の場合を示している。
【0029】
図４のバンドモデル図で示すように光を吸収して励起された電子はｎ型半導体側に流れ、ホールはｐ型半導体側に流れる。その結果、第１ユニットセル１０４と第２ユニットセル１０５の接続部では、第１ユニットセル１０４側の電子及び第２ユニットセル側のホールがトラップされる形になる。この場合、第２不純物半導体層１０８と第３不純物半導体層１１０の接合界面に再結合中心が形成されるようにして、この接合界面で再結合電流が流れるようにする。第２不純物半導体層１０８は単結晶半導体であり、その上に第３不純物半導体層１１０として、非晶質半導体層又は微結晶半導体層をプラズマＣＶＤ法などで堆積することにより、接合界面で再結合電流が流れるような接合を形成することができる。
【0030】
図３のタンデム型の光電変換装置によれば、単結晶半導体層１０６で形成される第１ユニットセル１０４をボトムセルとして用いることで、８００ｎｍ以上の長波長光の吸収をして光電変換することが可能となり、光電変換効率の向上に寄与する。この場合、単結晶半導体層１０６が１０μｍ以下と薄層化されていることにより、光生成キャリアの再結合による損失を低減することができる。この場合において、光入射側から下層に位置する単結晶半導体層１０６の凹凸構造と互いに作用しあって、第１ユニットセル１０４と第２ユニットセル１０５に光閉じ込め効果を発現させることができる。この効果により、タンデム型光電変換装置２０の変換効率を向上させることができる。
【0031】
（実施形態２）
次に、実施の形態１において示す図１のＡ―Ｂ切断線に対応する断面構造として、図２の場合を前提として光電変換装置１０の製造方法について説明する。
【0032】
図５（Ａ）に示す半導体基板１１５は円形の単結晶半導体基板より略四辺形に切り出されたものである。半導体基板１１５は、代表的には単結晶シリコンであって、表面が鏡面研磨されたものが好ましい。保護膜１１６は酸化シリコン又は窒化シリコンで形成することが好ましく化学気相成長法により形成する。
【0033】
半導体基板１１５の一面に一導電型の第１不純物半導体層１０７を形成する。例えば、一導電型の不純物として硼素を添加して、第１不純物半導体層１０７をｐ型に形成する。第１不純物半導体層１０７は、本形態の光電変換装置において、光入射側と反対側の面に配置され、裏面電界（ＢＳＦ：Ｂａｃｋ　Ｓｕｒｆａｃｅ　Ｆｉｅｌｄ）を形成する。硼素の添加は、ジボラン（B_2H_6）、三フッ化硼素（BF_3）をソースガスとして、生成されたイオンを質量分離しないで電界で加速して、生成されるイオン流を基板に照射するイオンドーピング装置を用いて行う。
【0034】
図５（Ｂ）は、保護膜１１６を除去して、第１不純物半導体層１０７上に第１電極１０３を形成している。第１電極１０３は耐熱性金属で形成することが好ましい。耐熱性金属としては、チタン、モリブデン、タングステン、クロムなどの金属材料が適用される。これらの金属材料の窒化物を第１不純物半導体層１０７に接して形成し、さらに該金属層を積層して第１電極１０３を二層構造としても良い。金属窒化物を形成することで、第１電極

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１０３の密着性を向上させることができる。第１電極１０３は真空蒸着法又はスパッタリング法で形成する。

【0035】

図５（Ｃ）は、第１電極１０３が形成された面から、水素イオンを含むイオンビームを半導体基板１１５に照射して、損傷層１１７を形成する段階を示している。水素イオンは、好ましくはH_3^+に代表されるようなクラスターイオンを打ち込んで、表面から一定の深さの領域に損傷層１１７を形成する。損傷層１１７の深さは、イオンの加速エネルギーによって制御される。損傷層１１７の深さにより半導体基板１１５から分離される単結晶半導体層の厚さが決まるので、クラスターイオンを加速する電界強度はそのことを考慮して決められる。損傷層１１７は半導体基板１１５の表面から１０μｍ未満の深さ、すなわち５０ｎｍ以上１００００ｎｍ未満、好ましくは１００ｎｍから５０００ｎｍの深さに損傷層を形成することが好ましい。第１電極１０３を通してクラスターイオンを半導体基板１１５に打ち込むことで、イオンの照射により表面が損傷を受けてしまうことを防止することができる。

【0036】

水素イオンであるH_3^+イオンに代表されるようなクラスターイオンの注入は、水素プラズマを生成し、該プラズマ中に生成されるイオンを質量分離せず、そのまま電界で加速することにより注入するイオンドーピング装置を用いて行うことができる。イオンドーピング装置を用いることにより、面積の大きい半導体基板１１５に対しても容易に行うことができる。

【0037】

図９は、イオンドーピング装置の構成を示す。イオン源２００では質量の異なる複数種のイオンが生成される。イオン源２００にはガス供給部２０４から水素等の所定のガスが供給される。イオン源２００に水素等が導入された後、イオン源２００のフィラメント２０１に電圧を印加してアーク放電を発生させる。これにより、水素がイオン化して、質量の異なる複数種のイオンが生成される。

【0038】

イオン源２００で生成されたイオンは、引出し電極系２０５によってイオンビームを形成する。イオンビームは載置台２０６に置かれた半導体基板１１５に照射される。イオンビームに含まれるイオン種の割合は載置台２０６の近傍に設けられた質量分析管２０７によって計量される。質量分析管２０７によって計数されたイオン密度は質量分析計２０８で信号変換され、その結果を電源制御部２０３にフィードバックさせるようにしても良い。電源制御部２０３はイオン密度の計数結果に従って、フィラメント電源２０２を制御することができる。

【0039】

ガス供給部２０４から供給された水素等のガスは、イオンドーピング装置のチャンバー内を流れる。イオン源２００に供給された水素は、式（１）の反応によりイオン化する。

$$H_2 + e^- \rightarrow H_2^+ + 2e^- - Q \quad (Q=15,39eV) \quad (1)$$

【0040】

イオンドーピング装置のチャンバー内の圧力は1×10^{-2}Ｐａから1×10^{-1}Ｐａであり、電離度があまり高くないことからH_2^+イオンより原料ガスであるH_2が多く存在している。従って、イオン源で生成されたH_2^+イオンは、引出し電極系２０５で引き出されるまでにH_2と反応し、式（２）の反応が起こる。

$$H_2^+ + H_2 \rightarrow H_3^+ + H + Q \quad (Q=1,49eV) \quad (2)$$

【0041】

H_3^+は、H^+及びH_2^+よりも安定な分子として存在するため、H_2と衝突する割合が高ければH_3^+が多量に生成されることになる。このことは、質量分析管２０７を用いて載置台２０６に照射されるイオンビームの質量分析結果を見れば明らかである。イオン種H^+、H_2^+、H_3^+の総量に対してH_3^+イオンの割合は７０％以上となっている。それにより、クラスターイオンであるH_3^+を多量に発生させたイオンビームを基板に照射

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することで、H^+、H_2^+を注入するよりも水素原子の注入効率が向上し、ドーズ量が少なくても水素を半導体基板１１５に高濃度に注入することができる。

【0042】

クラスターイオンとしてH_3^+の割合を高めておくことで、損傷層１１７には1×10^{20}ａｔｏｍｓ／ｃｍ^{3}以上の水素を含ませることが可能である。半導体基板１１５に形成される損傷層１１７は結晶構造が失われ微小な空孔が形成され、多孔質構造となっている。そのため、比較的低温（６００℃以下）の熱処理によって損傷層１１７に形成された微小な空洞の体積変化が起こり、損傷層１１７に沿って単結晶半導体層を分離することができる。

【0043】

図５（Ｄ）は、第１電極１０３上に絶縁層１０２を形成する段階を示す。絶縁層１０２は、酸化シリコン、酸化窒化シリコン、窒化酸化シリコン、窒化シリコンなどの絶縁膜で形成する。絶縁層１０２は平滑で親水性の表面を有するものであれば良い。絶縁層１０２の平滑性でいえば、平均面粗さＲａ値が１ｎｍ以下、好ましくは０．５ｎｍ以下であることが好ましい。なお、ここでいう平均面粗さとは、ＪＩＳ　Ｂ０６０１で定義されている中心線平均粗さを面に対して適用できるよう三次元に拡張したものである。

【0044】

平滑面を有し親水性表面を形成できる絶縁層としては、水素を含有する酸化シリコン、水素を含有する窒化シリコン、酸素と水素を含有する窒化シリコン、水素を含有する酸化窒化シリコン、水素を含有する窒化酸化シリコン等を適用することができる。

【0045】

なお、酸化窒化シリコン膜とは、その組成として、窒素よりも酸素の含有量が多いものであって、濃度範囲として酸素が５５～６５原子％、窒素が０．５～２０原子％、シリコンが２５～３５原子％、水素が０．１～１０原子％の範囲で含まれるものをいう。また、窒化酸化シリコン膜とは、その組成として、酸素よりも窒素の含有量が多いものであって、濃度範囲として酸素が１５～３０原子％、窒素が２０～５０原子％、シリコンが２５～３５原子％、水素が１５～２５原子％の範囲で含まれるものをいう。

【0046】

水素を含有する酸化シリコンとしては、例えば有機シランを用いた化学気相成長法により作製される酸化シリコンが好ましい。有機シランを用いて形成された絶縁層１０２として、酸化シリコン膜を用いることによって、支持基板と転置用半導体層との接合を強固にすることができるためである。有機シランとしては、テトラエトキシシラン（ＴＥＯＳ：化学式$Si(OC_2H_5)_4$）、テトラメチルシラン（ＴＭＳ：化学式$Si(CH_3)_4$）、テトラメチルシクロテトラシロキサン（ＴＭＣＴＳ）、オクタメチルシクロテトラシロキサン（ＯＭＣＴＳ）、ヘキサメチルジシラザン（ＨＭＤＳ）、トリエトキシシラン（$SiH(OC_2H_5)_3$）、トリスジメチルアミノシラン（$SiH(N(CH_3)_2)_3$）等のシリコン含有化合物を用いることができる。

【0047】

水素を含有する窒化シリコンは、シランガスとアンモニアガスを用いたプラズマＣＶＤ法により作製することができる。前記ガスに水素が加えられていても良い。酸素と水素を含有する窒化シリコンは、シランガスとアンモニアガスと亜酸化窒素ガスを用いたプラズマＣＶＤ法で作製することができる。いずれにしても、プラズマＣＶＤ法、減圧ＣＶＤ法、常圧ＣＶＤ法等の化学気相成長法により、シランガス等を原料ガスとして用いて作製される酸化シリコン、酸化窒化シリコン、窒化酸化シリコンであって水素が含まれるものであれば適用することができる。絶縁層１０２の成膜温度は、単結晶半導体基板に形成した損傷層１１７から水素が脱離しない温度として、３５０℃以下の成膜温度が推奨される。

【0048】

図６（Ａ）は支持基板１０１と半導体基板１１５とを接着する段階を示す。この接着は、平滑であり親水性表面を有する絶縁層１０２が支持基板１０１に密着することによりなされる。この接合は、水素結合やファン・デル・ワールス力が作用している。接合は、半導

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体基板１１５及び支持基板１０１の表面の水酸基や水分子が接着剤として働くことによって起きる。熱処理によって、水分子が拡散し、残留成分のシラノール基（Ｓｉ－ＯＨ）同士が水素結合で結合する。さらにこの接合部は、水素が抜けることでシロキサン結合（Ｓｉ－Ｏ－Ｓｉ）が形成されることで共有結合になり、半導体基板１１５と支持基板１０１の接合が強固なものとなる。なお、支持基板１０１の接着面にも、バリア層１１８として窒化シリコン膜、窒化酸化シリコン膜などを形成しておいても良い。バリア層１１８を形成することで、支持基板１０１からの不純物汚染を防止することができる。

【0049】

図６（Ｂ）は、加熱処理により損傷層１１７を劈開して半導体基板１１５を支持基板１０１から分離する段階を示す。加熱処理の温度は絶縁層１０２の成膜温度以上、支持基板１０１の耐熱温度以下で行うことが好ましい。例えば４００℃から６００℃の加熱処理を行うことにより、損傷層１１７に形成された微小な空洞の堆積変化が起こり、その領域に沿って劈開する。絶縁層１０２は支持基板１０１と接着しているので、支持基板１０１には単結晶半導体層１０６と第１電極１０３が残存する。このとき、単結晶半導体層１０６の厚さは、損傷層の深さにほぼ対応し、５０ｎｍ以上１００００ｎｍ未満、好ましくは１００ｎｍから５０００ｎｍの厚さに形成される。以上の工程により、支持基板１０１上に絶縁層１０２により固定された単結晶半導体層１０６を設けることができる。

【0050】

図７（Ａ）は、結晶欠陥の残留する単結晶半導体層１０６の修復と、表面に凹凸構造を形成するために、単結晶半導体層１０６の劈開面にレーザ処理をする段階を示している。レーザビームを単結晶半導体層１０６の劈開面に照射することで、単結晶半導体層１０６の少なくとも劈開面側は溶融し固相状態の下層部を種結晶として、その後の冷却過程で再単結晶化する。その過程で単結晶半導体層１０６の表面を凹凸化させることができる。

【0051】

このレーザ処理は酸素を含む雰囲気中で、パルスレーザビームを単結晶半導体層１０６の劈開面に照射することにより行われる。このレーザ処理のとき、少なくともレーザビームの照射領域は、２５０℃から６００℃の温度に加熱されていることが好ましい。照射領域を加熱しておくことで、レーザビームの照射による溶融時間を長くすることができ、表面の凹凸化と同時に結晶欠陥の修復を効果的に行うことができる。レーザビームは単結晶半導体層１０６の劈開面側を溶融させるものの、支持基板１０１は殆ど加熱されないので、ガラス基板のような耐熱性の低い支持基板を用いることが可能になる。また、第１電極１０３は耐熱性金属で形成されているので、上記温度で加熱されても単結晶半導体層１０６に悪影響を及ぼすことがない。当該耐熱性金属と第１不純物半導体層１０７の界面ではシリサイドが形成され、より電流が流れ易くなる。

【0052】

単結晶半導体層１０６の表面を凹凸化させるレーザ処理は、窒素又はアルゴンに代表される不活性気体に酸素が０．１体積％から２５体積％含まれる雰囲気中で行う。また、窒素又はアルゴンに代表される不活性気体に酸素若しくは酸化物気体が０．１体積％から５０体積％含まれる雰囲気中で行ってもよい。酸化物気体としては、二酸化炭素、亜酸化窒素などが適用可能である。その他、上記雰囲気に代えて、空気中、好ましくは乾燥空気中で行っても良い。

【0053】

パルスレーザビームは、光源（レーザ発振器）として、エキシマレーザ（ＸｅＣｌ（３０８ｎｍ）、ＫｒＦ（２４８ｎｍ）、ＡｒＦ（１９３ｎｍ））、ＹＡＧ、YVO_4レーザに代表される固体レーザ（第２高調波（５３２ｎｍ）、第３高調波（３５５ｎｍ）第４高調波（２６６ｎｍ））を用いる。例えば、波長３０８ｎｍのエキシマレーザビームを照射する場合には、発振周波数５～５０Ｈｚ、エネルギー密度１００～５００ｍＪ／ｃｍ^2、線状ビームのオーバーラップ割合を８０～９８％として、単結晶半導体層１０６を処理する。

【0054】

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また、パルスレーザビームの波長と照射回数を制御することにより、規則性のある凹凸構造を単結晶半導体層１０６の表面に形成することができる。例えば、波長３０８ｎｍのエキシマレーザビームを、３５０ｍＪ／ｃｍ^2～４５０ｍＪ／ｃｍ^{2}として、同じ領域に、パルス幅１０ｎｓｅｃ～３０ｎｓｅｃで繰り返し周波数が１０Ｈｚ～５０Ｈｚのパルスレーザビームを２０回～５０回照射することで、凸部が格子状に整列した凹凸構造を形成することができる。この凸部の整列間隔は照射するパルスレーザビームの波長を選択することによって制御することができる。例えば、波長３０８ｎｍのエキシマレーザを照射することで、凸部のピッチを概ね３０８ｎｍとすることができる。また、波長５２７ｎｍのＹＬＦレーザを用いると凸部のピッチは概ね５２７ｎｍとなり、Ｎｄ：ＹＡＧレーザの第２高調波（発振波長：５３２ｎｍ）を用いると凸部のピッチは概ね５３２ｎｍとすることができる。

【0055】

レーザ処理を行うためのレーザ処理装置の一例を図１０を参照して説明する。レーザ処理装置は、レーザ発振器２１０、レーザ光を細い線状ビームに集光伸張させる光学系２１１、レーザ照射領域の雰囲気を制御するガス噴射筒２１２、該ガス噴射筒２１２に雰囲気制御ガスを供給するガス供給部２１３、流量制御部２１４、ガス加熱部２１５、支持基板１０１を浮遊させ搬送する基板ステージ２２２、基板の両端を支持して搬送するガイドレール２２３、基板ステージ２２２に浮遊用にガスを供給するガス供給部２１６を備えている。

【0056】

レーザ発振器２１０は、その発振波長が、紫外光域乃至可視光域にあるものが選択される。レーザ発振器２１０は、パルス発振型のＡｒＦ、ＫｒＦ又はＸｅＣｌエキシマレーザ、或いはＮｄ：ＹＡＧレーザ、ＹＬＦレーザなどの固体レーザで、繰り返し周波数１ＭＨｚ以下、パルス幅１０ｎ秒以上５００ｎ秒以下のものが好ましい。例えば、繰り返し周波数１０Ｈｚ～３００Ｈｚ、パルス幅１０～３０ｎｓｅｃ、波長３０８ｎｍのＸｅＣｌエキシマレーザを用いる。

【0057】

光学系２１１はレーザ光を集光及び伸張して、被照射面に断面形状が線状となるレーザビームを形成する。線状ビームを形成する光学系２１１は、シリンドリカルレンズアレイ２１７、シリンドリカルレンズ２１８、ミラー２１９、ダブレットシリンドリカルレンズ２２０により構成される。レンズの大きさにもよるが、長手方向は１００ｍｍ～７００ｍｍ、短手方向は１００μｍ～５００μｍ程度の線状レーザ光を照射することが可能である。

【0058】

線状に集光されたレーザビームはガス噴射筒２１２の光導入窓２２１を通して支持基板１０１に照射される。ガス噴射筒２１２は支持基板１０１と近接して配置されている。ガス噴射筒２１２にはガス供給部２１３から窒素等の不活性ガスと酸素を含むガスが供給されている。当該ガスはガス噴射筒２１２の支持基板１０１に面した開口部から噴出する。ガス噴射筒２１２の開口部は、光導入窓２２１から入射したレーザビームが支持基板１０１に照射されるように、線状レーザビームの光軸に合わせて配置されている。ガス噴射筒２１２の開口部から噴射する酸化性気体により、レーザビームの照射領域の雰囲気制御を行う。

【0059】

ガス噴射筒２１２に供給する窒素等の不活性ガスと酸素を含むガスは、ガス加熱部２１５を２５０℃から７００℃に制御することにより、支持基板１０１のレーザビームの照射面の温度を１００℃から６００℃に制御でき、上記のようにレーザビームの照射による溶融時間を制御することができる。

【0060】

基板ステージ２２２には、ガス供給部２１６から空気又は窒素が流量制御部２１４を通して供給される。ガス供給部２１６から供給される気体は、基板ステージ２２２の上面から、支持基板１０１の下面を吹き付けるように噴出させて、該支持基板１０１を浮遊させる

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。支持基板１０１は両端がガイドレール２２３上を動くスライダ２２４に載せられて搬送されるが、基板ステージ２２２側からガスが吹き付けられることにより、湾曲せずに浮遊した状態で搬送することができる。本形態のレーザ処理装置では、支持基板１０１の上面にガス噴射筒２１２から窒素ガスが噴出するので、その裏側からもガスを吹き付けることにより、支持基板１０１の撓みを防ぐことができる。このような基板ステージ２２２の構成は、一辺が５００ｍｍを超え、厚さが１ｍｍ以下の支持基板を処理する場合に有効である。例えば、６００ｍｍ×７２０ｍｍ乃至７３０ｍｍ×９２０ｍｍで厚さが０．７ｍｍ以下の支持基板を処理することができる。

【0061】

基板ステージ２２２は、レーザ照射部近傍と、それ以外の領域に区画されていても良い。基板ステージ２２２のレーザ照射部近傍では、ガス加熱部２１５により加熱された窒素ガスを吹き付けるようにしても良い。それにより、支持基板１０１を加熱することができる。

【0062】

なお、図１０で示すレーザ処理装置は一例であり、レーザビーム照射時の雰囲気を窒素等の不活性ガスと酸素を含む雰囲気に制御できるものであれば他の構成を適用することもできる。例えば、レーザビームを導入可能な窓を備えた密閉可能な処理室に支持基板を保持し、該処理室に窒素等の不活性ガスと酸素を含むガスを導入して雰囲気制御しても良い。

【0063】

図７（Ｂ）は、単結晶半導体層１０６に第１不純物半導体層１０７とは逆の導電型の不純物元素を添加して、第２不純物半導体層１０８を形成する。例えば、リン又は砒素を添加して第２不純物半導体層１０８をｎ型に形成する。この場合、先の工程でレーザ処理により表面の結晶欠陥が修復されているので、第２不純物半導体層１０８の不純物濃度を精密に制御することができる。すなわち、レーザビームを照射して、単結晶半導体層の表面を処理し、その後、不純物領域を形成することにより、不純物濃度を高濃度化することができ、浅い接合を形成することができる。それにより、光生成キャリアの収集効率の高い光電変換装置を得ることができる。

【0064】

図７（Ｃ）は、単結晶半導体層１０６の端部をエッチングして第１電極１０３を露出させる段階を示している。エッチングは単結晶半導体層１０６にマスクを形成し、三フッ化窒素（NF_3）、六フッ化硫黄（SF_6）などのガスを用いてドライエッチングを行う。

【0065】

図８（Ａ）は、第１電極１０３に接する第１補助電極１１３と、第２不純物半導体層１０８上の第２補助電極１１４を形成する段階を示している。第１補助電極１１３は図７（Ｃ）でエッチングにより露出した第１電極１０３に接触するように形成する。第２補助電極１１４は、図１の平面図で示すように櫛型又は格子状の電極である。第１補助電極１１３及び第２補助電極１１４は、アルミニウム、銀、鉛錫（半田）などで形成すれば良い。例えば、銀ペーストを用いてスクリーン印刷法で形成する。

【0066】

その後、図８（Ｂ）で示すように、パッシベーション膜を兼ねた反射防止膜１１９を形成する。反射防止膜１１９は、窒化シリコン膜で形成することが好ましく、窒化シリコンと窒化酸化シリコンの積層膜で形成しても良い。

【0067】

このようにして図１で示す光電変換装置１０を製造することができる。本工程によれば、異種材料間の接合技術と、レーザ処理技術を用いることにより、７００℃以下（好適には５００℃以下）のプロセス温度で１０μｍ以下の単結晶半導体層を有する光電変換装置を製造することができる。すなわち、耐熱温度が７００℃以上の大面積ガラス基板に、単結晶半導体層を設けた光電変換装置を製造することができる。単結晶半導体層は単結晶半導体基板の表層を分離することにより得られるが、当該単結晶半導体基板は繰り返し利用することができるので資源を有効に利用することができる。なお、同様の工程により第２ユ

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ニットセルを作製することで、図３に示すタンデム型光電変換装置を製造することができる。

【0068】

（実施形態３）

本形態は、実施形態２と異なる製造工程を図１１に示す。図１１において、（Ａ）保護膜１１６を形成して第１不純物半導体層１０７を半導体基板１１５の一面に形成した後、（Ｂ）保護膜１１６をそのまま残して損傷層１１７を形成する。その後、（Ｃ）保護膜１１６を除去して第１電極１０３を形成する。本形態の工程によれば保護膜１１６を有効に利用することができる。すなわち、保護膜１１６を損傷層１１７形成後に除去することで、半導体基板１１５の表面の接合表面を平坦なものとすることができる。保護膜１１６は５０ｎｍから２００ｎｍの厚さで設けることが好ましい。また、第１不純物半導体層１０７を通して水素のクラスターイオンが打ち込まれる損傷層１１７を形成することにより、第１不純物半導体層１０７の水素化を兼ねることができる。

【0069】

（実施形態４）

本形態は、実施形態２と異なる製造工程を図１２に示す。図１２において、（Ａ）半導体基板１１５の一面に第１電極１０３を形成し、（Ｂ）第１電極１０３を通して一導電型の不純物元素を添加して第１不純物半導体層１０７を形成する。そして、（Ｃ）第１電極１０３を通して水素のクラスターイオンを打ち込み損傷層１１７を形成する。本工程では、第１電極１０３の形成後にイオンドーピングを行うことにより、第１電極１０３をイオンドーピングにおける損傷防止層として利用することができる。それによりイオンドーピングのために保護膜を形成する工程を省略することができる。

【0070】

（実施形態５）

本形態は、実施形態２と異なる製造工程を図１３に示す。図１３において、（Ａ）半導体基板１１５の一面に第１電極１０３を形成し、（Ｂ）第１電極１０３を通して水素のクラスターイオンを打ち込み損傷層１１７を形成する。そして、（Ｃ）第１電極１０３を通して一導電型の不純物元素を添加して第１不純物半導体層１０７を形成する。本工程では、第１電極１０３を最初に形成することにより、第１電極１０３をイオンドーピングにおける損傷防止層として利用することができる。本形態では、イオンドーピングのために保護膜を形成する工程を省略することができる。

【0071】

（実施形態６）

本形態は、実施形態２と異なる製造工程を図１４に示す。図１４において、（Ａ）保護膜１１６を形成して水素のクラスターイオンを半導体基板１１５の一面に打ち込んで損傷層１１７を形成し、（Ｂ）保護膜１１６をそのまま残して第１不純物半導体層１０７を形成する。そして、（Ｃ）保護膜１１６を除去して第１電極１０３を形成する。本工程は保護膜１１６をイオンドーピング時の損傷防止膜として、さらに第１不純物半導体層１０７を形成するときのドーピング深さを調節する膜として有効に利用している。また、損傷層１１７を形成した後に、第１不純物半導体層１０７を形成することにより、該第１不純物半導体層１０７の不純物濃度を高濃度化することができ、浅い接合を形成することができる、それにより、裏面電界（ＢＳＦ：Ｂａｃｋ　Ｓｕｒｆａｃｅ　Ｆｉｅｌｄ）効果を発現させ、光生成キャリアの収集効率を高めることができる。

【0072】

（実施形態７）

本形態は、実施形態２と異なる製造工程を図１５に示す。図１５において、（Ａ）保護膜１１６を形成して水素のクラスターイオンを打ち込み損傷層１１７を形成し、（Ｂ）保護膜１１６を除去して第１電極１０３を形成する。そして、（Ｃ）第１電極１０３を通して一導電型の不純物元素を添加して第１不純物半導体層１０７を形成する。第１電極１０３を通して第１不純物半導体層１０７を形成することにより、第１不純物半導体層１０７の

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厚さを制御することが容易となる。

【0073】

（実施形態８）

本形態は、実施形態２と異なる製造工程を図１６に示す。支持基板１０１上に単結晶半導体層１０６を接着し（図６（Ｂ））、図１６（Ａ）で示すように結晶欠陥の残留する単結晶半導体層１０６の修復と、表面に凹凸構造を形成するレーザ処理を行う。そして図１６（Ｂ）で示すように、単結晶半導体層１０６に第１不純物半導体層１０７とは逆の導電型の不純物元素を添加して第２不純物半導体層１０８を形成する。その後、図１６（Ｃ）に示すように第２不純物半導体層１０８上に反射防止膜１１９を形成する。

【0074】

その後、図１７（Ａ）で示すように、単結晶半導体層１０６の端部をエッチングして第１電極１０３を露出させ、図１７（Ｂ）で示すように第１補助電極１１３及び第２補助電極１１４を形成する。第２補助電極１１４は反射防止膜１１９上に形成し、その後、絶縁破壊電圧を瞬間的に印加することにより第２不純物半導体層１０８と導通をとることができ、補助電極として機能させることができる。

【0075】

本形態によれば、単結晶半導体層１０６に第２不純物半導体層１０８を形成した後にパッシベーション膜としても機能する反射防止膜１１９を形成することで、表面再結合速度を低くすることができ、光電変換装置の変換効率を高めることができる。

【0076】

本形態は、実施形態２～７と自由に組み合わせることができる。

【0077】

（実施形態９）

本形態は、実施形態２と異なる製造工程を図１８に示す。支持基板１０１上に単結晶半導体層１０６を接着した後（図６（Ｂ））、図１８（Ａ）において示すように、結晶欠陥の残留する単結晶半導体層１０６の修復と、表面に凹凸構造を形成するレーザ処理を行う。その後、図１８（Ｂ）で示すように反射防止膜１１９を形成し、図１８（Ｃ）で示すように第２不純物半導体層１０８を形成する。本形態によれば、第２不純物半導体層１０８の形成前にレーザ処理を行うので、レーザビームの照射による溶融領域を単結晶半導体層１０６の内部まで広げることができ、再単結晶化による欠陥修復の効果をより高めることができる。

【0078】

その後、図7（Ｃ）のように単結晶半導体層１０６の周辺部をエッチングして第１電極１０３を露出させ、第１補助電極１１３及び第２補助電極１１４を形成すれば良い。第２補助電極１１４は反射防止膜１１９上に形成されるが、絶縁破壊電圧を瞬間的に印加してバーンインコンタクトを形成することにより電極として機能させることができる。

【0079】

本形態は、実施形態２～７と自由に組み合わせることができる。

【0080】

（実施形態１０）

本形態は、実施形態２と異なる製造工程を図１９に示す。支持基板１０１上の単結晶半導体層１０６にレーザ処理を行い、再単結晶化と表面に凹凸構造を形成する。そして図１９（Ａ）で示すように、単結晶半導体層１０６を覆うように絶縁層１２０を形成する。そして、図１９（Ｂ）で示すように、絶縁層１２０に開口部を形成して単結晶半導体層１０６を露出させ、その開口部に第２不純物半導体層１０８を形成する。その後、図１９（Ｃ）で示すように、絶縁層１２０と単結晶半導体層１０６を貫通し第１電極１０３に達する開口部を形成し、第１補助電極１１３及び第２補助電極１１４を形成する。さらに反射防止膜１１９を形成する。本形態のように、単結晶半導体層１０６の内側に開口部を形成して第１電極１０３と導通する第１補助電極１１３を形成することにより、光電変換装置の小型化を図ることができる。

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【0081】
本形態は、実施形態２～７と自由に組み合わせることができる。
【0082】
（実施形態１１）
実施形態１～１０により製造される光電変換装置を用いた太陽光発電モジュールの一例を図２０（Ａ）に示す。この太陽光発電モジュール３０は、支持基板１０１に設けられた単結晶半導体層１０６により光電変換装置１０が構成されている。単結晶半導体層１０６には光電変換機能を発現させる第１不純物半導体層、第２不純物半導体層などが形成されている。
【0083】
第１補助電極１１３は単結晶半導体層１０６の裏面側に形成されている第１電極と接続する電極であり、第２補助電極１１４は櫛形又は格子状の電極である。第１補助電極１１３と第２補助電極１１４は支持基板１０１の一面に形成され、支持基板１０１の端部領域でコネクタ用の第１裏面電極１２１と第２裏面電極１２２とそれぞれ接続する。図２０（Ｂ）は、Ｃ－Ｄ切断線に対応する断面図であり、支持基板１０１の貫通口を通して第１補助電極１１３と第２補助電極１１４が第１裏面電極１２１と第２裏面電極１２２とそれぞれ接続している。
【0084】
このように、支持基板１０１に単結晶半導体層１０６を接合して光電変換装置１０を形成することにより、太陽光発電モジュールの薄型化を図ることができる。なお、本形態において、光電変換装置１０に代えて、図３で示すタンデム型光電変換装置２０を適用しても良い。
【0085】
（実施形態１２）
図２１は太陽光発電モジュール３０を用いた太陽光発電システムの一例を示す。一又は複数の太陽光発電モジュール３０の出力電力は、充電制御回路１２３により蓄電池１２４を充電する。蓄電池１２４の充電量が多い場合には、負荷１２５に直接出力される場合もある。
【0086】
蓄電池１２４として電気二重層キャパシタを用いると、充電に化学反応を必要とせず、急速に充電することができる。また、化学反応を利用する鉛蓄電池などに比べ、寿命を約８倍、充放電効率を１．５倍に高めることができる。負荷１２５としては、蛍光灯、発光ダイオード、エレクトロルミネッセンスパネルなどの照明、小型の電子機器など、さまざまな用途に応用することができる。
【図面の簡単な説明】
【0087】
【図1】光電変換装置の構成を示す平面図。
【図2】光電変換装置の製造工程を説明する断面図。
【図3】タンデム型光電変換装置の製造工程を説明する断面図。
【図4】タンデム型光電変換装置の動作を説明するエネルギーバンド図。
【図5】光電変換装置の製造工程を説明する断面図。
【図6】光電変換装置の製造工程を説明する断面図。
【図7】光電変換装置の製造工程を説明する断面図。
【図8】光電変換装置の製造工程を説明する断面図。
【図9】イオンドーピング装置の構成を説明する図。
【図10】レーザ処理装置の構成を説明する図。
【図11】光電変換装置の製造工程を説明する断面図。
【図12】光電変換装置の製造工程を説明する断面図。
【図13】光電変換装置の製造工程を説明する断面図。
【図14】光電変換装置の製造工程を説明する断面図。

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【図15】光電変換装置の製造工程を説明する断面図。
【図16】光電変換装置の製造工程を説明する断面図。
【図17】光電変換装置の製造工程を説明する断面図。
【図18】光電変換装置の製造工程を説明する断面図。
【図19】光電変換装置の製造工程を説明する断面図。
【図20】（Ａ）太陽光発電モジュールの構成を説明する平面図。（Ｂ）切断線Ｃ－Ｄによる図２０（Ａ）の断面図。
【図21】太陽光発電システムの一例を説明する図。
【符号の説明】
【0088】
１０　光電変換装置
２０　タンデム型光電変換装置
３０　太陽光発電モジュール
１０１　支持基板
１０２　絶縁層
１０３　第１電極
１０４　第１ユニットセル
１０５　第２ユニットセル
１０６　単結晶半導体層
１０７　第１不純物半導体層
１０８　第２不純物半導体層
１０９　非単結晶半導体層
１１０　第３不純物半導体層
１１１　第４不純物半導体層
１１２　第２電極
１１３　第１補助電極
１１４　第２補助電極
１１５　半導体基板
１１６　保護膜
１１７　損傷層
１１８　バリア層
１１９　反射防止膜
１２０　絶縁層
１２１　第１裏面電極
１２２　第２裏面電極
１２３　充電制御回路
１２４　蓄電池
１２５　負荷
２００　イオン源
２０１　フィラメント
２０２　フィラメント電源
２０３　電源制御部
２０４　ガス供給部
２０５　引出し電極系
２０６　載置台
２０７　質量分析管
２０８　質量分析計
２１０　レーザ発振器
２１１　光学系
２１２　ガス噴射筒

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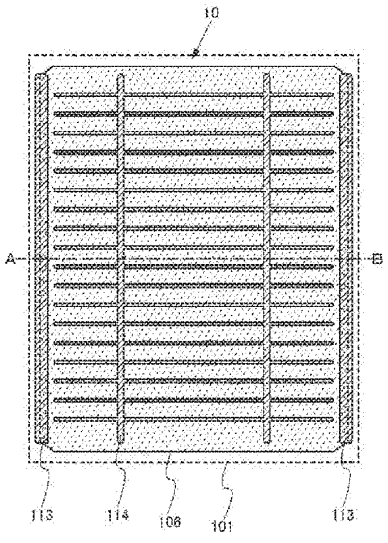
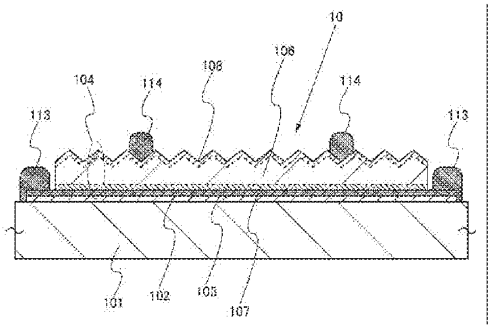
２１３　ガス供給部
２１４　流量制御部
２１５　ガス加熱部
２１６　ガス供給部
２１７　シリンドリカルレンズアレイ
２１８　シリンドリカルレンズ
２１９　ミラー
２２０　ダブレットシリンドリカルレンズ
２２１　光導入窓
２２２　基板ステージ
２２３　ガイドレール
２２４　スライダ

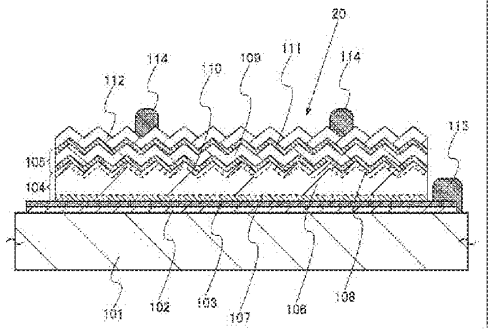
【図1】



【図2】



【図3】



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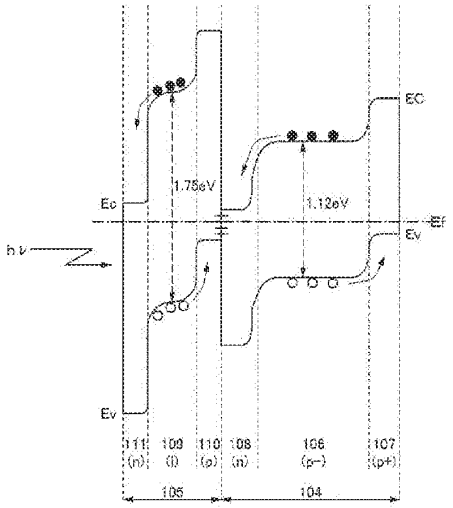
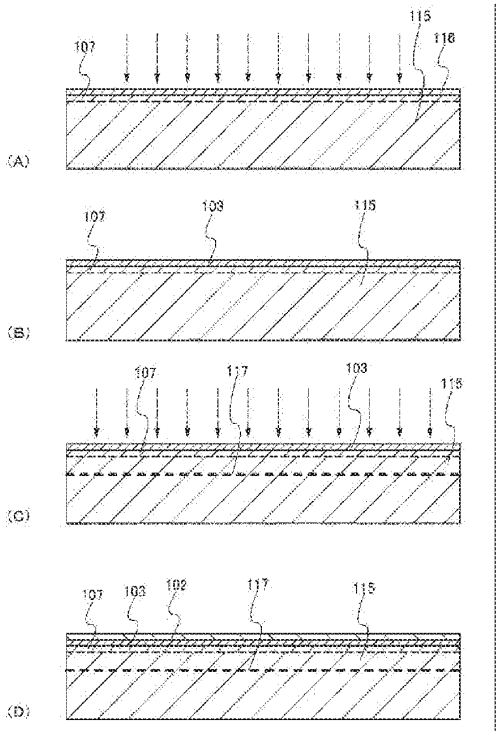
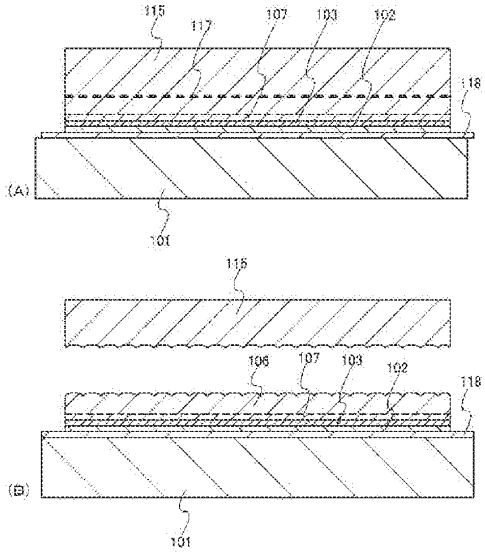
【図4】



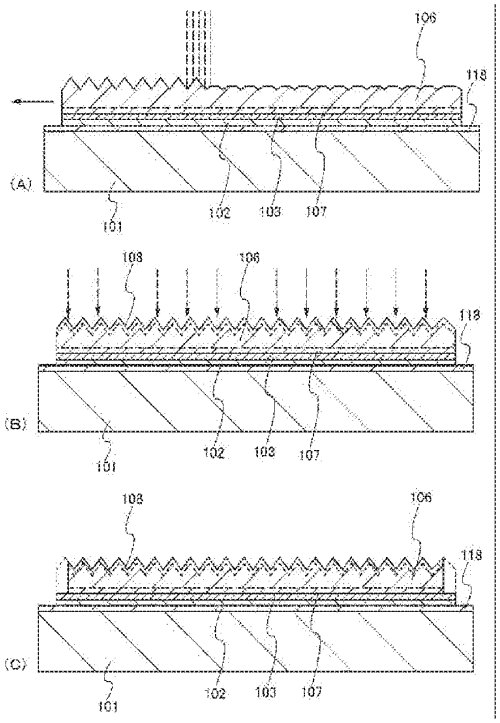
【図5】



【図6】



【図7】



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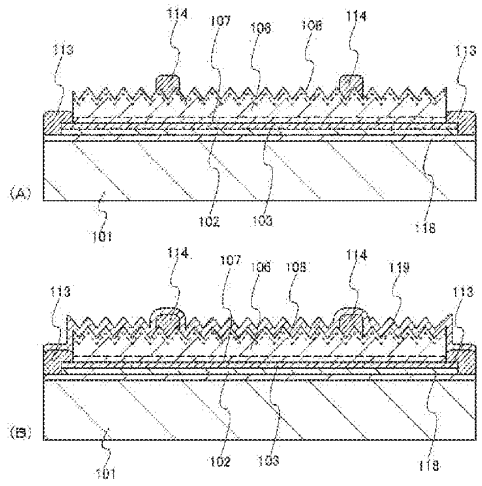
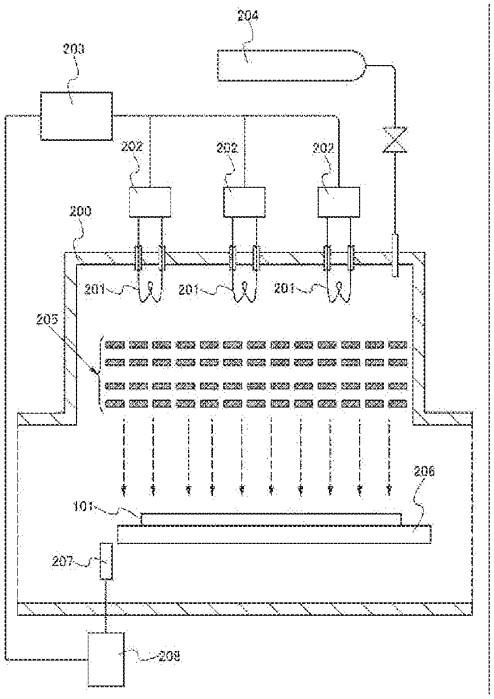
【図8】



【図9】



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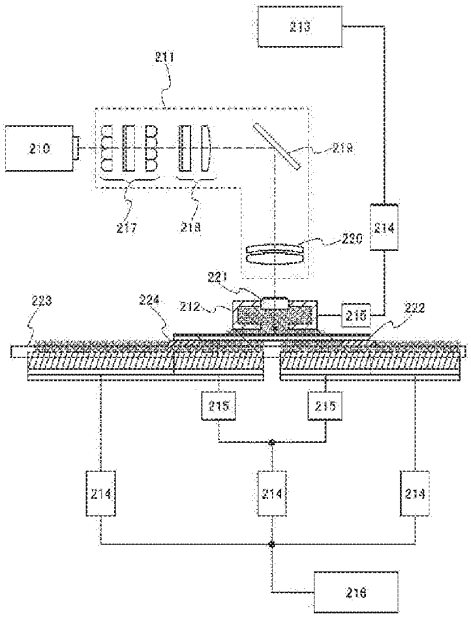
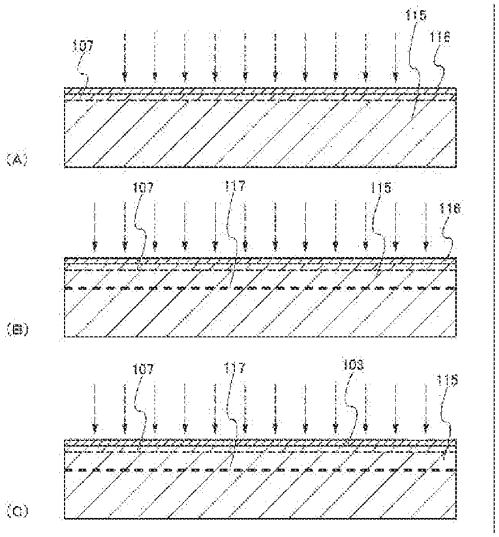


【図11】



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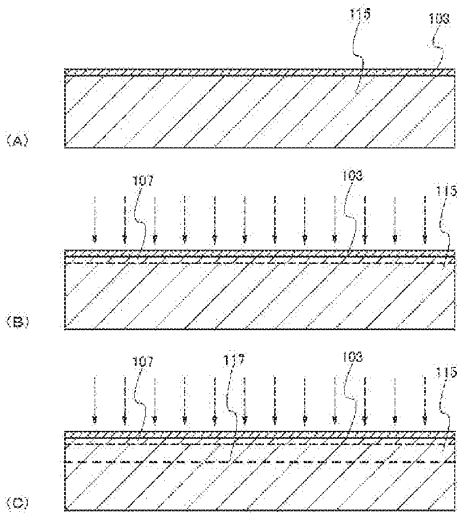
【図12】



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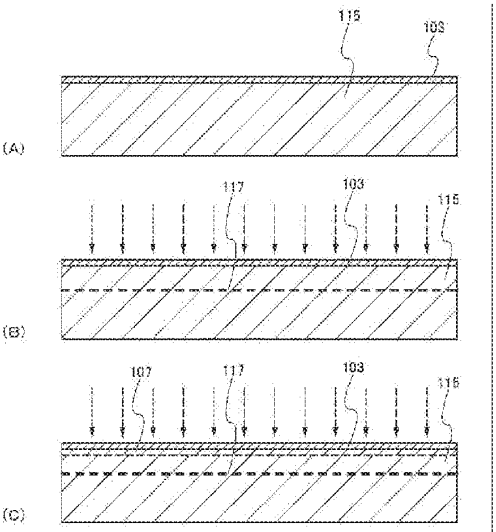

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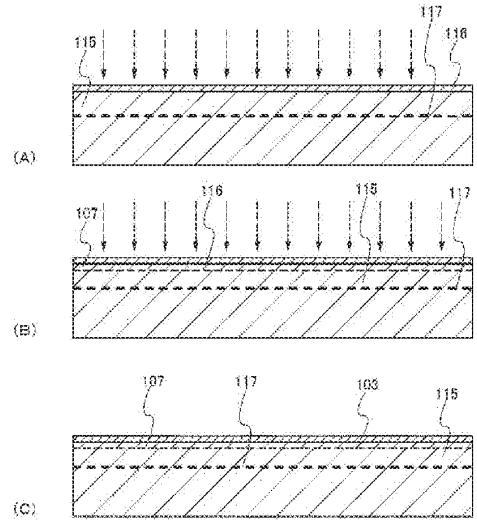

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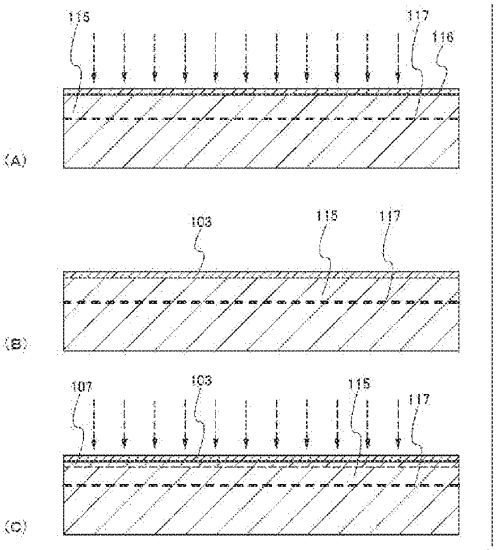

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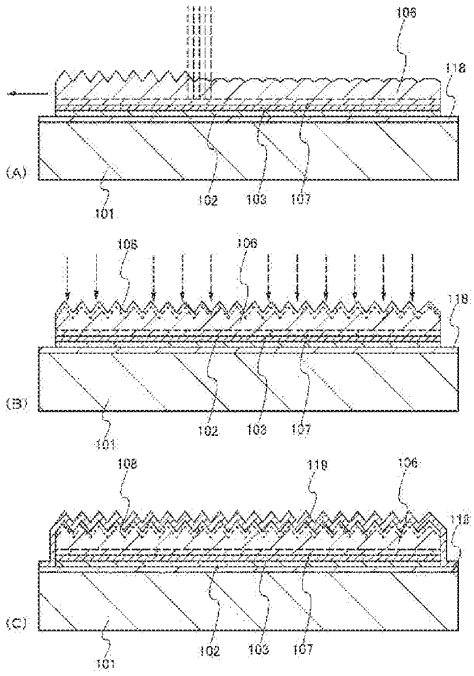

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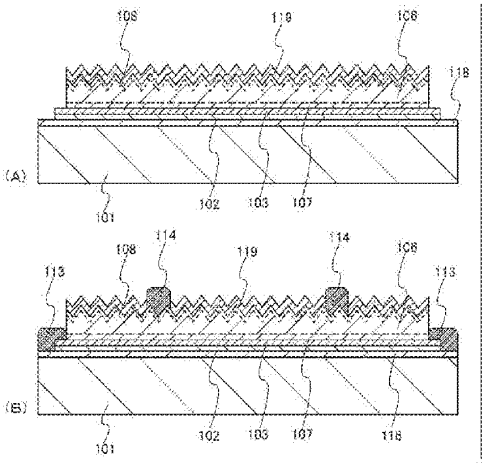

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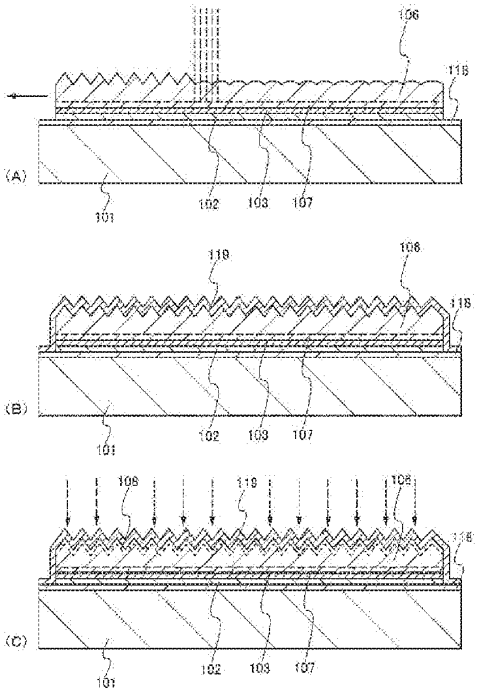

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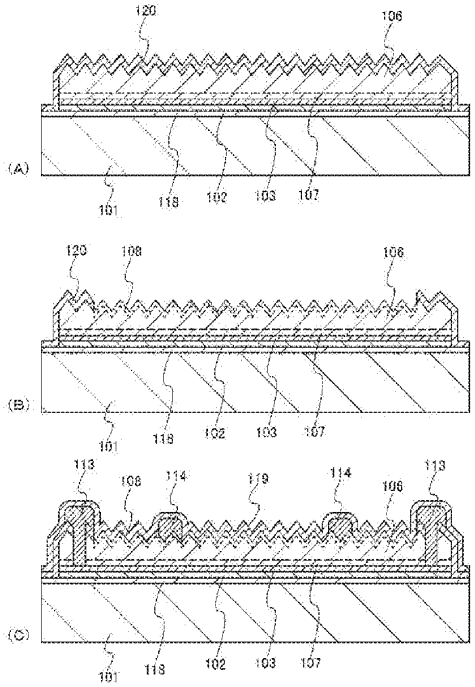

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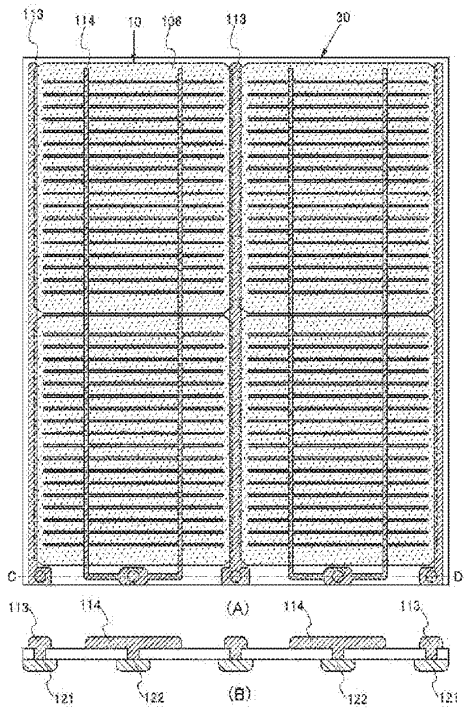
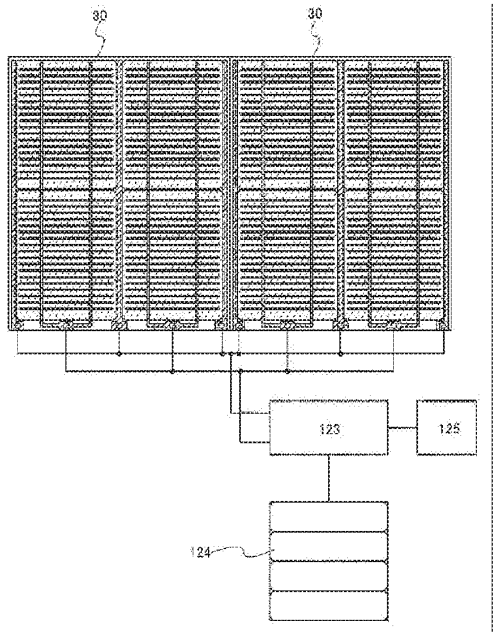
【図20】


113
114
10
108
113
30
C
D
(A)
113
114
114
113
121
122
(B)
122
121

【図21】


80
30
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125
124

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Agent.	PARK, Byung Chang
Inventor	CHOI, Chul Chae | KIM, Hye Won | YOON, Phil Won | KIM, Jin Sung
Applicant	LG Electronics Inc.
Rightholder	LG Electronics Inc.

발명의 명칭

나노 텍스쳐링 구조를 갖는 반도체 웨이퍼 기판을 포함하는벌크형 태양전지의 제조방법

Title of Invention

The bulk type method for manufacturing solar cell including the semiconductor wafer substrate having the nano texturing structure.

요약

본 발명에 따르면, 벌크형 태양전지에 포함되는 실리콘 웨이퍼 기판 상에 나노 텍스쳐링(texturing) 구조를 형성하는 방법에 있어서, 금속 나노 입자를 촉매로 하는 에칭법을 이용하여 상기 나노 텍스쳐링 구조를 형성함으로써 우수한 특성을 갖는 반사방지막을 손쉽게 얻을 수 있는 벌크형 태양전지의 제조방법이 제공된다. 본 발명에 따르면, 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서, 상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되, 상기 나노 텍스쳐링 구조 형성 단계는 금속을 촉매로 하는 에칭법에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법이 제공된다.

나노 텍스쳐링, 나노 금속, 촉매, 에칭, 태양전지

Abstract

According to the present invention, provided is the bulk type method for manufacturing solar cell which easily can obtain the reflection barrier layer which has the excellent characteristic by forming the nano texturing structure as to the method for forming the nano texturing structure on the silicon wafer substrate included in the bulk type solar cell using the etching method the metal nanoparticle to the catalyst. According to the present invention, provided is the bulk type method for manufacturing solar cell which includes the step of forming the nano texturing structure of having the pattern of the nano-size on the silicon wafer substrate surface as to the bulk type method for manufacturing solar cell including the silicon wafer substrate and in which the nano texturing structure formation step is performed with the etching method the metal to the catalyst.

The nano texturing, the nano metal, the catalyst, the etching, the solar cell

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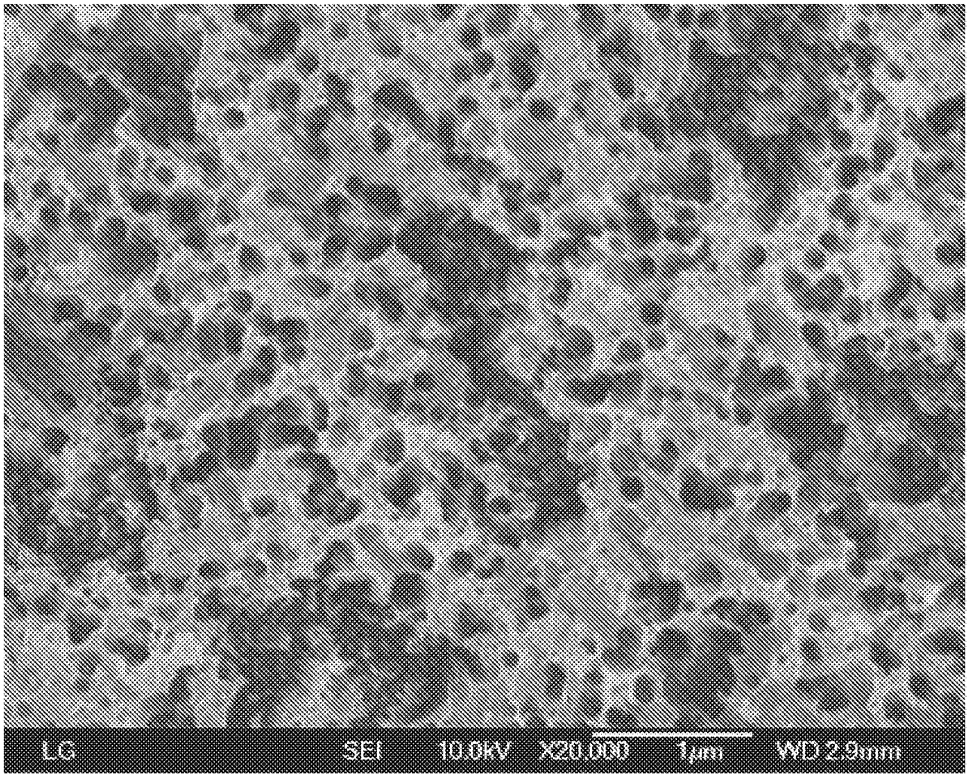
대표도면(Representative drawing)



청구의 범위

청구 **1**항:

실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서, 상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되, 상기 나노 텍스쳐링 구조 형성 단계는 금속을 촉매로 하는 에칭법에 의해 수행되고, 상기 나노 텍스쳐링 구조 형성 단계는, 나노 금속 입자들이 혼합되어 있는 용액을 상기 실리콘 웨이퍼 기판 상에 분산시키는 단계;열처리에 의하여 상기 용액을 건조시켜 상기 나노 금속입자들이 사이로 상기 실리콘 웨이퍼 기판이 노출되도록 상기 나노 금속 입자들을 남기는 단계; 에칭액을 사용하여 상기 나노 금속 입자들 사이에 노출된 상기 실리콘 웨이퍼 기판을 에칭하는 단계; 및상기 나노 금속 입자들을 제거하는 단계를 포함하는 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구 **2**항:

삭제

청구 **2**항:

Scope of Claims

Claim 1:

The bulk type method for manufacturing solar cell comprising the silicon wafer substrate, wherein the bulk type method for manufacturing solar cell is characterized by comprising the step: step: step: of etching the silicon wafer substrate exposed using the etchant between nano metal particles and the step of removing nano metal particles that nano metal particles leave nano metal particles the silicon wafer substrate is exposed by the interval it dries the solution with the thermal process that the nano texturing structure formation step disperses the solution in which nano metal particles are mixed on the silicon wafer substrate the nano texturing structure formation step is performed with the etching method the metal to the catalyst it includes the step of forming the nano texturing structure of having the pattern of the nano-size on the silicon wafer substrate surface.

Claim 2:

Deletion.

Claim 2:

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삭제

Deletion.

청구 3항:

Claim 3:

제1항에 있어서, 상기 나노 금속 입자들의 입경은 20nm 내지 200nm인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 1, the bulk type method for manufacturing solar cell in which the particle diameter of nano metal p articles is 20nm to 200nm.

청구 4항:

Claim 4:

제1항에 있어서, 상기 나노 금속 입자들은 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 중 적어도 하나인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 1, the bulk type method for manufacturing solar cell in which nano metal particles are at least one among the gold (Au), silver (Ag), copper (Cu), palladiu m (Pd), tin (Sn).

청구 5항:

Claim 5:

제1항에 있어서, 상기 에칭액은 플루오르화 수소(HF)와 과산화수소수(H2O2)의 혼합용액인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 1, the bulk type method for manufacturing solar cell in which the etchant is the mixture of the hyd rogen peroxide liquid (H(SB)2(/SB)O(SB)2(/SB)) and hy drogen fluoride (HF).

청구 6항:

Claim 6:

제5항에 있어서, 상기 플루오르화 수소(HF)와 과산화수소수(H2O2)의 혼합비는 10:1인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 5, the bulk type method for manufacturing solar cell in which the mixing ratio of the hydrogen pero xide liquid (H(SB)2(/SB)O(SB)2(/SB)) and hydrogen fluo ride (HF) is 10:1.

청구 7항:

Claim 7:

제1항에 있어서, 상기 용액에서 상기 나노 금속 입자들의 농도는 1000ppm 내지 100000ppm 인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 1, the bulk type method for manufacturing solar cell in which the concentration of nano metal part icles is 1000ppm to 100000ppm in the solution.

청구 8항:

Claim 8:

제1항에 있어서, 상기 나노 금속 입자들이 혼합되어 있는 용액을 분산시키는 단계는, 스프레이법(spraying), 스핀코팅법(spin coating), 디핑법(dipping) 중 어느 하나에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법.

As for claim 1, the bulk type method for manufacturing solar cell performed by any one of step, of dispersing t he solution in which nano metal particles are mixed is t he spraying, the spin coating method, and the dipping method.

청구 9항:

Claim 9:

제1항, 그리고 제3항 내지 제8항 중 어느 하나의 제조방법으로 제조된 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 포함하는 벌크형 태양전지.

The bulk type solar cell including the nano texturing structure of having the pattern of the nano-size on the silicon wafer substrate surface manufactured with one manufacturing method among the claims 1 and 3 throu gh 8.

기술분야

Technical Field

본 발명은 벌크형 태양전지의 제조방법에 관한 것이다. 보다 상세하게는 벌크형 태양전지에 포함되는 실리콘 웨이퍼 기판 상에 나노 텍스쳐링(texturing) 구조를 형성하는 방법에 있어서, 금속 나노 입자를 촉매로 하는 에칭법을 이용하여 상기 나노 텍스쳐링 구조를 형성함으로써 우수한 특성을 갖는 반사방지막을 손쉽게 얻을 수 있는 벌크형 태양전지의 제조방법에 관한 것이다.

The present invention relates to the bulk type method for manufacturing solar cell. More specifically, it is abou t the bulk type method for manufacturing solar cell whi ch easily can obtain the reflection barrier layer which h as the excellent characteristic by forming the nano tex turing structure as to the method for forming the nano texturing structure on the silicon wafer substrate inclu ded in the bulk type solar cell using the etching method the metal nanoparticle to the catalyst.

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배경기술

태양전지는 포토다이오드의 일종으로 태양광을 직접 전력으로 전환시키는 목적에 이용되고 있어, 대체 에너지원으로서 지상에서는 물론이고 우주개발을 위해서도 그 이용이 점차 확대되어가고 있어 전력용 전자소자로서 매우 중요하다. 그 구조도 p-n 접합형, 쇼트키 배리어형 및 이종(異種)반도체의 접합으로 이루어지는 것 등이 있으며, 소재로서는 실리콘#183#갈륨비소 등의 결정체, 기타 각종 반도체가 광범위하게 이용되고 있다. 특히 근래에 와서는 다결정(多結晶) 실리콘이나 비정질(非晶質) 실리콘을 이용한 태양전지의 개발과 실용화가 크게 각광을 받고 있다.

그러나 높은 광전변환효율과 품질특성 때문에 단결정의 실리콘 웨이퍼를 기반으로하는 벌크형 태양전지가 상용화되고 있는 실정이다.

일반적으로 실리콘 결정계(crystalline) 태양전지는 실리콘 웨이퍼를 출발 원료로 한다. 실리콘 웨이퍼는 고순도로 정제된 실리콘을 고온으로 가열하여 결정으로 성장된 잉곳을 만들고 이를 절단 및 연마를 통해 대형의 결정판 형태의 웨이퍼 기판을 만든다. 결정은 원자가 규칙적으로 배열된 물질을 의미한다.

종래의 태양전지를 제조하기 위한 웨이퍼의 처리 방법 중 가장 중요한 처리는 기판 표면의 텍스처링(texturing), 즉 조직화이다. 이러한 텍스처링의 목적은 빛을 받는 태양전지의 전면부에서의 반사율을 감소시키고, 태양전지 내에서 빛의 통과 길이를 길게 함으로써 태양전지 내부로 빛이 흡수되도록 하여 효율을 향상시키고자 하는 것이다. 한편, 기판 상에 광학 박막을 형성시켜 반사방지막으로서의 기능을 하게 할 수도 있다.

텍스처링된 종래의 태양전지용 웨이퍼 기판의 표면을 확대한 단면도는 도 1a에 도시하였다. 텍스처링한 후의 표면은 피라미드 구조를 가지므로 옆면에서 관찰할 때 정삼각형의 형상을 가진다.

종래 기술에 의하면, 경면 연마처리(Polishing)된 웨이퍼 표면은 입사되는 태양 빛의 30% 내지 50% 정도를 반사시키고, 표면을 피라미드 형태로 조직화(texturing)시키면 입사되는 태양광의 10% 내지 20% 정도를 반사하게 되어 반사율이 현저하게 줄어든다. 또한, 조직화시킨 표면에 반사방지막(anti-reflection, AR)을 증착시키면 반사율을 약 5% 내지 10%까지 감소시킬 수 있는 것으로 알려져 있다.

그러나, 상기 반사율은 태양광의 주요 흡수 파장대역인 500nm 내지 1000nm 에서관찰된 평균값으로서, 태양광 파장범위의 낮은 파장영역인 300nm 내지 400nm에서는 비교적 높은 반사도를 가지며, 반사방지막의 증착 이후라야만 비로소 상대적으

Background Art

The solar cell is used to the purpose of converting the sunlight into the direct electricity as a kind of the photo diode and it is in ground and the usage is gradually expanded as the alternation energy source for the space development and the purpose is important as the electric power electric component. It has to be made of the structure is the p-n heterogeneous, and the junction of the inhomogeneous semiconductor and schottky barrier type and crystal, the other all kinds of semiconductor including silicone · the GaAs etc. are extensively used as the material. Particularly, recently, development and put to practical use of the solar cell coming and uses the poly-crystal silicon or the amorphous silicon are in the spotlight.

But the high photoelectric conversion efficiency and the bulk type solar cell which therefore has the silicon wafer of the monocrystal as the base with quality characteristic are commercialized.

Generally, the silicon crystal (crystalline) solar cell the silicon wafer to the starting raw material. The silicone refined to the high purity is heated with the high temperature and the silicon wafer makes the ingot grown up to the Decision and this the wafer substrate of the definitive edition form of the large size is made through the cut and grinding. The material in which the atom as to the Decision, is regularly arranged is meant.

Most, the important processing is the texturing of the substrate surface, in other words, the organizing among the processing method of the wafer for manufacturing the conventional solar cell. The reflectivity at the front surface of the solar cell in which the object of such texturing receives light is decreased and Light is absorbed in the solar cell into the solar cell inside by drawing the passing length of light and to improve the efficiency. In the meantime, the optical thin film is formed on the substrate and it functions as the reflection barrier layer.

The cross-sectional view enlarging the surface of the wafer substrate for the textured conventional solar cell showed in the drawing 1a. When observing in side since the surface of the texturing has the pyramid structure it has the shape of the regular triangle.

According to the prior art, 30% of the sunlight in which the wafer surface which becomes with the mirror-polishing processing (Polishing) is incoming to about 50% is reflected and 10% of the sunlight which is incoming if it orders the surface through the pyramid shape with the organizing (texturing) to about 20% is reflected and reflectivity remarkably decreases. Moreover, it is known that reflectivity can be reduced to about 5% to 10% if the reflection barrier layer (anti-reflection, AR) is evaporated in the surface structured.

But reflectivity includes the relatively high reflectivity in 300nm which is 500nm which is the major absorption wavelength band of the sunlight to the average value which becomes with 1000nm west observation and is t

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로 더 낮은 반사도를 갖게 되는 문제점을 가지고 있다. 따라서, 모든 태양광의 파장영역에서 균일하게 낮은 반사율을 갖는 기판 표면을 형성하고자 하는 연구가 진행되었고, 그 결과 나노 구조를 갖는 나노 텍스쳐링 구조가 형성된 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지가 개발되었다.

he low wavelength area of the sunlight wavelength range. To 400nm, and the problem of having the reflectivity which is relatively lower as the deposition after of the reflection barrier layer at last. Therefore, in the wavelength area of all sunlights, the research to form the substrate surface having the low reflectivity proceeded and the bulk type solar cell including the silicon wafer substrate in which the nano texturing structure consequently of having the nanostructure was formed was developed.

이러한 나노 텍스쳐링 구조를 갖는 종래 태양전지용 실리콘 웨이퍼 기판의 표면을 확대한 이미지는 도 1과 같다. 도 1을 참조하면 조직화된 웨이퍼 기판 상에는 피라미드 형태의 나노 구조가 형성되어 있음을 알 수 있다.

The image enlarging the surface of the conventional solar battery use silicone wafer substrate having such nano texturing structure is same as those of fig. 1. Referring to Figure 1, it can know that the nanostructure of the pyramid shape is formed on the wafer substrate which becomes systemized.

이러한 나노 텍스쳐링 구조로 형성되는 반사방지막은 넓은 파장영역 및 넓은 입사각 범위에서 반사 방지막으로서의 기능을 수행한다. 종래에는 이러한 나노 텍스쳐링 구조를 형성하기 위해 진공 중에서 염소(Cl) 기체 또는 플루오르화 황(SF6)을 이용하여 반응성 이온 에칭(RIE; Reactive Ion Etching)을 수행하거나, 실리콘 웨이퍼 기판 표면에 금속을 매우 얇게 증착한 후 습식에칭을 수행하였다.

The function as the reflection barrier layer is performed in the wavelength area in which the reflection barrier layer formed into such nano texturing structure is broad and the wide incidence angular range. Conventionally, in order to form the nano texturing structure of being like that the reactive ion etch (RIE: Reactive Ion Etching) was performed among the vacuum using the chlorine (Cl) gas or the sulfonicfluoride (SF(SB)6(/SB)) or it was very thin the metal the wet etching was performed in the silicon wafer substrate surface after doing the deposition.

그러나, 상기 방법 중 반응성 이온 에칭법을 이용하는 방법은 복잡하고 값비싼 장비를 필요로 하는 진공 공정이 필수적이라는 문제가 있다. 한편, 습식 에칭을 이용하는 방법은 금속과 에칭액과의 촉매반응으로 실리콘을 에칭하여 나노 텍스쳐링 구조를 형성하는 방식으로 반응성 이온 에칭(RIE)을 이용하는 방식보다 공정상 간단하다는 장점이 있다. 그러나, 이 방법 또는 진공 장비를 사용하여야 하는 문제가 있다.

But it has the problem the vacuum process which need the expensive equipment in which the method for using the reactive ion etching method among the method is complicated and is essential. In the meantime, the wet etching is used. And a method has the advantage that is simple than the mode which uses with eutectic phase the metal, and the mode etching the silicone to the catalyst reaction with the etchant and forms the nano texturing structure the reactive ion etch (RIE). But there is a problem that it does using this method or the vacuum equipment.

따라서, 진공 장비 등을 사용하지 않기 위하여 실리콘에 전기도금 방식을 이용하여 금속을 얇게 도금한 후 이를 에칭하여 위와 같은 방법으로 나노 텍스쳐링 구조를 형성시키기도 한다.

Therefore, in order not to use the vacuum equipment etc., it thins this the metal is etched using the electro plating after doing plating and the nano texturing structure is formed into the method as in the above in the silicone.

한편, 실리콘 웨이퍼 기판 표면에 나노 텍스쳐링 구조를 형성시키는 또 다른 방법으로는 황 가스 분위기에서 실리콘 웨이퍼 기판 표면에 엑시머 레이저를 조사함으로써 나노 텍스쳐링 구조를 형성하는 방법이 있다.

In the meantime, in another method for forming the nano texturing structure in the silicon wafer substrate surface the sulfur gas atmosphere, it has the method for forming the nano texturing structure by irradiating the excimer laser in the silicon wafer substrate surface.

또한, 나노 텍스쳐링 구조가 아닌 복수 개의 홀로 이루어지는 다공성 구조를 실리콘 웨이퍼 기판에 형성시킴으로써 반사방지막을 형성하기도 한다. 그러나, 이 방법은 기판 표면에 다공성 구조를 형성시키기 위해 전기분해장치 등 복잡한 장치를 이용한 공정을 필요로 한다는 문제가 있다.

Moreover, by forming the porous structure of being alone made of being not nano texturing structure of multiple in the silicon wafer substrate the reflection barrier layer is formed. But this method has the problem that the process of using the apparatus complicated with the electrolysis device etc. in order to form the porous structure in the substrate surface, is required.

따라서, 간단한 공정만으로도 우수한 특성을 가지는 텍스쳐링 구조를 형성시킬 수 있는 기술에 대한 개발이 필요하다.

Therefore, the development about the technology forming the texturing structure of having the excellent

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characteristic into the simple process is.

발명의 내용

Summary of Invention

해결하고자 하는 과제

Problem to be solved

본 발명은 상술한 바와 같은 종래 기술의 문제점을 해결하기 위한 것으로, 진공공정 등의 필요없이 간소화된 공정만으로 실리콘 웨이퍼 기판 표면에 우수한 반사방지 특성을 갖는 나노 텍스쳐링 구조를 형성시킬 수 있는 벌크형 태양전지의 제조방법을 제공하는 데에 그 목적이 있다.

It has the purpose to provides the bulk type method for manufacturing solar cell forming the nano texturing structure of having the excellent anti-reflection property on the silicon wafer substrate surface into the process of becoming streamlined without the need including the vacuum process etc. the invention solves the problem of the prior art as described above.

과제해결 수단

Means to solve the problem

상술한 목적을 달성하기 위한 본 발명의 일 실시형태에 따르면, 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서, 상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되, 상기 나노 텍스쳐링 구조 형성 단계는 금속을 촉매로 하는 에칭법에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법이 제공된다.

The step of forming the nano texturing structure of having the pattern of the nano-size on the silicon wafer substrate surface is included as to the bulk type method for manufacturing solar cell including the silicon wafer substrate for achieving the above-described purpose. The bulk type method for manufacturing solar cell performed by the etching method in which the nano texturing structure formation step the metal to the catalyst is provided.

상기 나노 텍스쳐링 구조 형성 단계는, 나노 금속 입자가 혼합되어 있는 용액을 상기 실리콘 웨이퍼 기판 상에 분산시키는 단계, 에칭액을 사용하여 상기 나노 금속 입자가 분산된 실리콘 웨이퍼 기판을 에칭하는 단계, 및 상기 나노 금속 입자를 제거하는 단계를 포함할 수 있다.

The nano texturing structure formation step comprises the step of dispersing the solution, and the step of etching the silicon wafer substrate and the step of removing the nano metal particle. As to the step of, the nano metal particle is mixed on the silicon wafer substrate. As to the step of, the nano metal particle is dispersed using the etchant.

상기 나노 금속 입자의 입경은 20nm 내지 200nm로 하는 것이 바람직하다.

It is the be desirable that the particle diameter of the nano metal particle is done by 20nm to 200nm.

상기 나노 금속 입자는 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 중 적어도 하나로 하는 것이 바람직하다.

It is the be desirable that the nano metal particle is done by at least one among the gold (Au), silver (Ag), copper (Cu), palladium (Pd), tin (Sn).

상기 에칭액은 플루오르화 수소(HF)와 과산화수소수(H2O2)의 혼합용액인 것이 바람직하다.

The etchant is the be desirable the mixture of the hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/SB)) and hydrogen fluoride (HF).

상기 플루오르화 수소(HF)와 과산화수소수(H2O2)의 혼합비는 10:1로 하는 것이 바람직하다.

It is the be desirable that the mixing ratio of the hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/SB)) and hydrogen fluoride (HF) is done by 10:1.

상기 용액에서 상기 나노 금속 입자의 농도는 1000ppm 내지 100000ppm 으로 하는 것이 바람직하다.

In the solution, it is the be desirable that the concentration of the nano metal particle is done by 1000ppm to 100000ppm.

상기 나노 금속 입자가 혼합되어 있는 용액을 분산시키는 단계는, 스프레이법(spraying), 스핀코팅법(spin coating), 디핑법(dipping) 중 어느 하나에 의해 수행될 수 있다.

It can be performed by any one of step, of dispersing the solution in which the nano metal particle is mixed is the spraying, the spin coating method, and the dipping method.

상기 목적을 달성하기 위한 본 발명의 벌크형 태양전지는 상기의 제조방법으로 제조되고 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 포함할 수 있다.

The nano texturing structure of the bulk type solar cell of the invention for achieving the purpose being made of the manufacturing method described in the above and having the pattern of the nano-size on the silicon

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wafer substrate surface is include might.

발명의 효과

Effects of the Invention

본 발명에 따르면, 진공공정 등의 복잡한 공정의 필요없이 간소화된 공정만으로 실리콘 웨이퍼 기판 표면에 우수한 반사방지 특성을 갖는 나노 텍스쳐링 구조를 형성시킬 수 있다.

According to the invention, the nano texturing structure of having the anti-reflection property of being excellent on the silicon wafer substrate surface can be formed into the process of becoming streamlined without the need of the process of being complicated including the vacuum process etc.

상세설명

Detailed Description

이하, 첨부되는 도면을 참조하여 본 발명의 실시형태들을 상세하게 설명하도록 한다.

Hereinafter, specifically the attached embodiments of the invention is illustrated.

도 2는 본 발명의 일 실시형태에 따른 태양전지용 실리콘 웨이퍼 기판의 표면을 전자현미경으로 관찰한 이미지이다.

Figure 2 is an image observing the surface of the solar battery use silicone wafer substrate to the electron microscope according to one embodiment of the invention.

도 2를 참조하면, 본 발명의 실리콘 웨이퍼 기판의 표면은 나노 패턴으로 이루어지는 나노 텍스쳐링 구조를 갖는다.

Referring to Figure 2, the surface of the silicon wafer substrate of the invention has the nano texturing structure of being made of the nano pattern.

상기 나노 텍스쳐링 구조는 나노크기의 패턴으로 이루어져 있다. 즉, 실리콘 웨이퍼 기판 상부에 나노 크기의 패턴들이 조직화되어 있는 구조이다. 나노 텍스쳐링 구조에 의하면 반사방지막(anti-refletion; AR)을 사용하는 것과 다른 특징을 얻을 수 있다. 즉, 반사방지막을 사용하면 특정 파장 대역에서만 반사방지의 효과를 얻을 수 있는 반면 나노 텍스쳐링 구조에 의하면 넓은 파장영역에서 균일하게 반사방지의 효과를 얻을 수 있다.

The nano texturing structure comprises the pattern of the nano-size. That is, the structure where the patterns of the nano-size become systematic in the silicon wafer substrate upside. According to the nano texturing structure, the other characteristic can be obtained the reflection barrier layer (anti-refletion: AR) is used. That is, if the reflection barrier layer is used the effect of the anti-reflection can be obtained from the certain wavelength band on the other hands the effect of the anti-reflection can be uniformly obtained according to the nano texturing structure from the wide wavelength area.

나노 패턴의 크기는 태양전지의 반사방지막으로서의 기능을 최대한 달성할 수 있는 범위 내에서 선택될 수 있다. 즉, 패턴의 크기가 너무 크면 반사율이 저하될 수 있고, 반대로 패턴의 크기가 너무 작으면 반사가 방지되어 태양전지로 흡수되는 광량이 미미해지기 때문에, 그 크기를 적절하게 선택하여야 한다.

The size of the nano pattern can be selected in the range that to the utmost can achieve the function as the anti-reflection layer for a solar cell. That is, reflectivity can be degraded if the size of the pattern is so big and the light quantity which the reflection is prevented if the size of the pattern is so small on the contrary and is absorbed into the solar cell is sight. Therefore the size has to be appropriately selected.

이하, 본 발명의 태양전지용 실리콘 웨이퍼 기판의 나노 텍스쳐링 구조를 형성하는 방법에 대해 설명하기로 한다. 도 3a 내지 도 3f는 본 발명의 일 실시형태에 따른 나노 텍스쳐링 구조를 갖는 실리콘 웨이퍼 기판을 포함하는 태양전지를 제조하는 과정을 설명하는 공정도이다.

Hereinafter, it decides to explain the method for forming the nano texturing structure of the solar battery use silicone wafer substrate of the invention. Figures 3a through 3f are the process map for illustrating the process of manufacturing the solar cell including the silicon wafer substrate having the nano texturing structure according to one embodiment of the invention.

먼저, 도 3a에 도시되는 바와 같은 실리콘 웨이퍼 기판(110) 표면에 잔류하는 네이티브 옥사이드(native oxide; 120)를 제거한다. 실리콘 웨이퍼 기판(110)의 표면에는 실리콘 웨이퍼 기판(110)의 제조 과정에서 형성되거나, 대기 중의 노출 등에 따라 형성되는 네이티브 옥사이드(120)가 잔류하게 되는데 나노 텍스쳐링 구조를 형성하기 전에 이러한 이물질을 제거해

In advance, the native oxide (native oxide: 120) remaining in the silicon wafer substrate (110) surface as illustrated in Figure 3a is removed. In the surface of the silicon wafer substrate (110), it is formed at the manufacturing process of the silicon wafer substrate (110) or before the native oxide (120) formed according to

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주어야 한다. 실리콘 웨이퍼 기판(110)을 플루오르화 수소(HF) 혼합용액에 담금으로써 일어나는 화학 반응에 의해 상기와 같은 네이티브 옥사이드(120)가 제거될 수 있다.

the exposure among the atmosphere etc. remaining behind but forming the nano texturing structure such foreign substance is removed. The above-mentioned native oxide (120) can be the silicon wafer substrate (110) removed in the hydrogen fluoride (HF) mixture as the dipping with the chemical reaction occurring.

그 후, 도 3b에 도시되는 바와 같이, 네이티브 옥사이드(120)가 제거된 실리콘 웨이퍼 기판(110) 상에 나노 금속 입자(135)가 분산되어 있는 수용액(130)을 도포하고 건조시킨다. 후에 나노 금속 입자(135)가 형성되어 있지 않은 부분의 실리콘 웨이퍼 기판(110)이 에칭됨으로써 나노 텍스쳐링 구조가 형성된다. 상기 수용액(130)에는 나노 금속 입자(135)가 약 1000 ppm 내지 100000ppm 의 농도로 고르게 분산되어 있을 수 있다. 한편, 나노 금속 입자(135)의 입경은 형성하고자 하는 나노 텍스쳐링 구조의 패턴의 형태에 따라 적절하게 선택될 수 있다. 나노 금속 입자(135)의 입경이 너무 크면 나노 텍스쳐링 구조에 포함되는 패턴 간의 거리가 지나치게 멀어지게 되고, 입경이 너무 작으면 패턴이 너무 조밀하게 형성될 수 있으므로, 적절한 범위 내에서 선택될 수 있다. 일례로서 나노 금속 입자(135)의 입경을 20nm 내지 200nm 의 범위 내에서 선택할 수 있다. 한편, 나노 금속 입자의 구성 물질은 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 등으로 할 수 있다. 일례로서, 약 100nm의 입경을 갖는 은(Ag)을 나노 금속 입자(135)로 선택할 수 있다.

Thereafter, as shown in Figure 3b, the aqueous solution (130) in which the nano metal particle (135) is dispersed is coated with on the silicon wafer substrate (110) from which the native oxide (120) is removed and it dries. After, the nano texturing structure is formed since the silicon wafer substrate (110) of the part in which the nano metal particle (135) is not formed is etched. In the aqueous solution (130), the nano metal particle (135) is evenly dispersed into the concentration of about 1000ppm to 100000ppm. In the meantime, according to the form which the particle diameter of the nano metal particle (135) forms of the pattern of the nano texturing structure, it can be appropriately selected. If the particle diameter of the nano metal particle (135) is so large, the distance included in the nano texturing structure between the pattern becomes overly distant and the pattern can be so tightly formed if the grain size is so small. Therefore it can be selected in the proper range. As an example, the particle diameter of the nano metal particle (135) can be chosen in the range of 20nm to 200nm. In the meantime, the configuration element of the nano metal particle can be done by the gold (Au), the silver (Ag), the copper (Cu), the palladium (Pd), the tin (Sn) etc. As an example, the silver (Ag) having the particle diameter of about 100nm can be selected as the nano metal particle (135).

한편, 나노 금속 입자(135)가 혼합되어 있는 수용액(130)을 실리콘 웨이퍼 기판(110) 상에 도포하는 데에는 스프레이법(spraying), 스핀코팅법(spin coating), 디핑법(dipping) 등이 이용될 수 있다. 스프레이법은 수용액(130)을 실리콘 웨이퍼 기판(110) 상에 고르게 분사하는 방식이고, 스핀코팅법은 실리콘 웨이퍼 기판(110) 상에 수용액(130)을 떨어뜨린 후 이를 회전시켜 수용액(130)이 원심력에 의해 실리콘 웨이퍼 기판(110) 상에 코팅될 수 있도록 하는 방식이며, 디핑법은 실리콘 웨이퍼 기판(110)을 수용액(130)에 담가 코팅을 하는 방식이다. 이러한 방식으로 나노 금속 입자(135)가 분산되어 있는 수용액(130)이 실리콘 웨이퍼 기판(110) 상에 도포되면, 열처리 등을 통하여 이를 건조시켜 실리콘 웨이퍼 기판(110) 상에 나노 금속 입자(135)만이 남을 수 있도록 한다.

In the meantime, the spraying, the spin coating method, the dipping method etc. can be used to coat with the aqueous solution (130) in which the nano metal particle (135) is mixed on the silicon wafer substrate (110). It is the mode in which the spraying evenly sprays the aqueous solution (130) on the silicon wafer substrate (110) and it is the mode in which it rotates this after the spin coating method drops down the aqueous solution (130) on the silicon wafer substrate (110) and the aqueous solution (130) is coated with the centrifugal force on the silicon wafer substrate (110) and it is the mode in which the dipping method dips the silicon wafer substrate (110) in the aqueous solution (130) and coated. In this way, if the aqueous solution (130) in which the nano metal particle (135) is dispersed is coated on the silicon wafer substrate (110) this is dried through the thermal process etc. and it remains on the silicon wafer substrate (110) only the nano metal particle (135).

다음으로, 실리콘 웨이퍼 기판(110)을 에칭액에 담궈 에칭(etching)한다. 상기 에칭액으로는 플루오르화 수소(HF)와 과산화수소수(H2O2)가 혼합되어 있는 용액을 사용할 수 있다. 본래는 플루오르화 수소(HF)와 과산화수소수(H2O2)가 혼합

Next, the silicon wafer substrate (110) is dipped in the etchant and it does with the etching (etching). The solution in which the hydrogen fluoride (HF) and hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/SB)) are mixed can

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되어 있는 용액만으로는 실리콘 웨이퍼 기판(110)을 에칭시킬 수 없으나, 기판(110) 상에 분산되어 있는 나노 금속 입자(135)가 촉매로 작용하여 나노 금속 입자(135)를 사이의 공간에 노출되어 있는 실리콘 웨이퍼 기판(110)이 에칭될 수 있는 것이다. 플루오르화 수소(HF)와 과산화수소수(H2O2)의 혼합비는 10:1 정도로 하는 것이 바람직하다. 도 3c는 이러한 방법에 의해 에칭된 실리콘 웨이퍼 기판(110)의 단면 구조를 나타낸다. 나노 금속 입자(135)를 사이의 공간에 노출된 실리콘 웨이퍼 기판(110)이 에칭됨으로써 나노 패턴으로 형성되는 나노 텍스쳐링 구조가 형성되게 되는 것이다.

be used as the etchant. The inherent cannot etch the silicon wafer substrate (110) to the solution in which t he hydrogen fluoride (HF) and hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/SB)) are mixed. But the nano met al particle (135) dispersed on the substrate (110) acts on the catalyst and the exposed silicon wafer substrat e (110) can be etched on space between nano metal p article (135). It is the be desirable that the mixing ratio of the hydrogen peroxide liquid (H(SB)2(/SB)O(SB)2(/S B)) and hydrogen fluoride (HF) is done by about 10:1. Figure 3c shows the section structure of the silicon wa fer substrate (110) etched with such method. Since th e silicon wafer substrate (110) exposed to space betw een nano metal particle (135) is etched the nano textu ring structure of being formed with the nano pattern is formed.

에칭이 완료되면 순수(pure water)를 이용하여 실리콘 웨이퍼 기판(110)을 세척한 후에 금속 에칭을 수행하여 나노 금속 입자(135)를 제거한다. 도 3d는 에칭에 의해 나노 금속 입자(135)가 제거된 실리콘 웨이퍼 기판(110)의 모습을 나타낸다. 이렇게 함으로써 표면에 나노 텍스쳐링 구조가 형성된 실리콘 웨이퍼 기판(110)이 얻어질 수 있다.

When the etching is completed, after the silicon wafer substrate (110) is washed using the pure water the me tal etching is performed and the nano metal particle (1 35) is removed. Figure 3d shows the display of the silic on wafer substrate (110) in which the nano metal parti cle (135) is removed using the etching. By doing this, t he silicon wafer substrate (110) in which the nano text uring structure is formed in the surface can be obtaine d.

그 후, 도 3e에 도시되는 바와 같이, 상기 나노 텍스쳐링 구조가 형성된 제1전도성(예를 들면, p형)을 갖는 실리콘 웨이퍼 기판(110)에 제2전도성(예를 들면, n형)을 갖는 물질을 확산시켜 p-n 접합을 형성하고, 표면에 패시베이션 층(passivation; 150)을 형성한다. 패시베이션 층(150)은 실리콘 웨이퍼 기판(110)을 부동태화시켜 표면 결함을 최소화하기 위한 것이다. 패시베이션 층(150)은 실리콘 웨이퍼 기판(110)의 표면을 산화시킴으로써 형성될 수 있다. 즉, 상기 산화 반응에 의해 안정한 물질인 실리콘 산화물(SiOx)이 실리콘 웨이퍼 기판(110) 표면에 형성됨으로써 패시베이션 층(150)이 형성될 수 있다. 한편, 실리콘 질화물(SiNx) 등의 물질을 상기 실리콘 웨이퍼 기판(110) 표면에 증착함으로써 패시베이션 층(150)을 형성시킬 수도 있다.

Thereafter, as shown in Figure 3e, material having the second conductivity (for example, the n-type) are diffu sed over the silicon wafer substrate (110) having the fi rst conductivity (for example, the p-type) in which the nano texturing structure is formed and the p-n junction is formed and the passivation layer (passivation: 150) i s formed on the surface. The passivation layer (150) m akes something passive the silicon wafer substrate (11 0) and the surface defect is to be minimized. The passi vation layer (150) can be formed by oxidizing the surfa ce of the silicon wafer substrate (110). That is, since t he silicon oxide (SiO(SB)x(/SB)) which is material which are stable with the oxidation reaction is formed in the s ilicon wafer substrate (110) surface the passivation lay er (150) can be formed. In the meantime, the passivati on layer (150) can be formed by depositing the materia l including the silicon nitride (SiN(SB)x(/SB)) etc. on th e silicon wafer substrate (110) surface.

다음으로, 도 3f에 도시되는 바와 같이, 상기 패시베이션 층(150)이 형성된 실리콘 웨이퍼 기판(110) 상에 전극(170)을 형성시킴으로써 태양전지가 완성된다. 전극(170)은 통상의 인쇄법(printing) 등에 의해 형성될 수 있다.

Next, as shown in Figure 3f, by forming the electrode (170) on the silicon wafer substrate (110) in which the passivation layer (150) is formed the solar cell is compl eted. The electrode (170) is formed by the normal print ing method etc.

이러한 방법에 의하면, 진공공정 또는 전기분해공정 등을 사용하지 않고도 실리콘 웨이퍼 기판에 나노 텍스쳐링 구조를 형성할 수 있으며, 이에 따라 나노 텍스쳐링 구조 형성에 필요한 작업 공수를 간소화할 수 있고, 제조 원가가 절감될 수 있다.

According to such method, the nano texturing structure can be formed on the silicon wafer substrate even though the vacuum process or the electrolysis pr ocess etc. are not used and accordingly the necessary man-hour can be streamlined in the nano texturing text uring and the manufacturing cost can be cut down.

또한, 값비싼 장비 또는 복잡한 공정 없이도 나노 텍스쳐링 구조와 같은 우수한 특성의 반사방지막을 얻을 수 있다.

Moreover, expensive the reflection barrier layer of the excellent characteristic like the nano texturing structur e can be obtained without the complex process.

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면책안내

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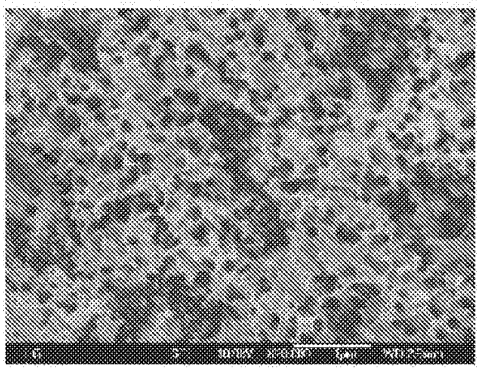
(54) 발명의 명칭 **나노 텍스쳐링 구조를 갖는 반도체 웨이퍼 기판을 포함하는벌크형 태양전지의 제조방법**

(57) 요 약

본 발명에 따르면, 벌크형 태양전지에 포함되는 실리콘 웨이퍼 기판 상에 나노 텍스쳐링(texturing) 구조를 형성하는 방법에 있어서, 금속 나노 입자를 촉매로 하는 에칭법을 이용하여 상기 나노 텍스쳐링 구조를 형성함으로써 우수한 특성을 갖는 반사방지막을 손쉽게 얻을 수 있는 벌크형 태양전지의 제조방법이 제공된다. 본 발명에 따르면, 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서, 상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되, 상기 나노 텍스쳐링 구조 형성 단계는 금속을 촉매로 하는 에칭법에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법이 제공된다.

대 표 도 - 도2



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특허청구의 범위

청구항 1

실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서,

상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되,

상기 나노 텍스쳐링 구조 형성 단계는 금속촉 촉매로 하는 에칭법에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 2

제1항에 있어서,

상기 나노 텍스쳐링 구조 형성 단계는,

나노 금속 입자가 혼합되어 있는 용액을 상기 실리콘 웨이퍼 기판 상에 분산시키는 단계;

에칭액을 사용하여 상기 나노 금속 입자가 분산된 실리콘 웨이퍼 기판을 에칭하는 단계; 및

상기 나노 금속 입자를 제거하는 단계를 포함하는 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 3

제2항에 있어서,

상기 나노 금속 입자의 입경은 20㎚ 내지 200㎚인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 4

제2항에 있어서,

상기 나노 금속 입자는 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 중 적어도 하나인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 5

제2항에 있어서,

상기 에칭액은 플루오르화 수소(HF)와 과산화수소수(H_2O_2)의 혼합용액인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 6

제5항에 있어서,

상기 플루오르화 수소(HF)와 과산화수소수(H_2O_2)의 혼합비는 10:1인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 7

제2항에 있어서,

상기 용액에서 상기 나노 금속 입자의 농도는 1000ppm 내지 100000ppm 인 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 8

제2항에 있어서,

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상기 나노 금속 입자가 혼합되어 있는 용액을 분산시키는 단계는, 스프레이법(spraying), 스핀코팅법(spin coating), 디핑법(dipping) 중 어느 하나에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법.

청구항 9

제1항 내지 제8항 중 어느 하나의 제조방법으로 제조된 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 포함하는 벌크형 태양전지.

명 세 서

발명의 상세한 설명

기 술 분 야

[0001] 본 발명은 벌크형 태양전지의 제조방법에 관한 것이다. 보다 상세하게는 벌크형 태양전지에 포함되는 실리콘 웨이퍼 기판 상에 나노 텍스쳐링(texturing) 구조를 형성하는 방법에 있어서, 금속 나노 입자를 촉매로 하는 에칭법을 이용하여 상기 나노 텍스쳐링 구조를 형성함으로써 우수한 특성을 갖는 반사방지막을 손쉽게 얻을 수 있는 벌크형 태양전지의 제조방법에 관한 것이다.

배 경 기 술

[0002] 태양전지는 포토다이오드의 일종으로 태양광을 직접 전력으로 전환시키는 목적에 이용되고 있어, 대체 에너지원으로서 지상에서는 물론이고 우주개발을 위해서도 그 이용이 점차 확대되어가고 있어 전력용 전자소자로서 매우 중요하다. 그 구조도 p-n 접합형, 쇼트키 배리어형 및 이종(異種)반도체의 접합으로 이루어지는 것 등이 있으며, 소재로서는 실리콘 갈륨비소 등의 결정체, 기타 각종 반도체가 광범위하게 이용되고 있다. 특히 근래에 와서는 다결정(多結晶) 실리콘이나 비정질(非晶質) 실리콘을 이용한 태양전지의 개발과 실용화가 크게 각광을 받고 있다.

[0003] 그러나 높은 광전변환효율과 품질특성 때문에 단결정의 실리콘 웨이퍼를 기반으로하는 벌크형 태양전지가 상용화되고 있는 실정이다.

[0004] 일반적으로 실리콘 결정계(crystalline) 태양전지는 실리콘 웨이퍼를 출발 원료로 한다. 실리콘 웨이퍼는 고순도로 정제된 실리콘을 고온으로 가열하여 결정으로 성장된 잉곳을 만들고 이를 절단 및 연마를 통해 대형의 결정판 형태의 웨이퍼 기판을 만든다. 결정은 원자가 규칙적으로 배열된 물질을 의미한다.

[0005] 종래의 태양전지를 제조하기 위한 웨이퍼의 처리 방법 중 가장 중요한 처리는 기판 표면의 텍스쳐링(texturing), 즉 조직화이다. 이러한 텍스쳐링의 목적은 빛을 받는 태양전지의 전면부에서의 반사율을 감소시키고, 태양전지 내에서 빛의 통과 길이를 길게 함으로써 태양전지 내부로 빛이 흡수되도록 하여 효율을 향상시키고자 하는 것이다. 한편, 기판 상에 광학 박막을 형성시켜 반사방지막으로서의 기능을 하게 할 수도 있다.

[0006] 텍스쳐링된 종래의 태양전지용 웨이퍼 기판의 표면을 확대한 단면도는 도 1a에 도시하였다. 텍스쳐링한 후의 표면은 피라미드 구조를 가지므로 옆면에서 관찰할 때 정삼각형의 형상을 가진다.

[0007] 종래 기술에 의하면, 경면 연마처리(Polishing)된 웨이퍼 표면은 입사되는 태양 빛의 30% 내지 50% 정도를 반사시키고, 표면을 피라미드 형태로 조직화(texturing)시키면 입사되는 태양광의 10% 내지 20% 정도를 반사하게 되어 반사율이 현저하게 줄어든다. 또한, 조직화시킨 표면에 반사방지막(anti-reflection, AR)을 증착시키면 반사율을 약 5% 내지 10%까지 감소시킬 수 있는 것으로 알려져 있다.

[0008] 그러나, 상기 반사율은 태양광의 주요 흡수 파장대역인 500㎚ 내지 1000㎚ 에서관찰된 평균값으로서, 태양광 파장범위의 낮은 파장영역인 300㎚ 내지 400㎚에서는 비교적 높은 반사도를 가지며, 반사방지막의 증착 이후라야만 비로소 상대적으로 더 낮은 반사도를 갖게 되는 문제점을 가지고 있다. 따라서, 모든 태양광의 파장영역에서 균일하게 낮은 반사율을 갖는 기판 표면을 형성하고자 하는 연구가 진행되었고, 그 결과 나노 구조를 갖는 나노 텍스쳐링 구조가 형성된 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지가 개발되었다.

[0009] 이러한 나노 텍스쳐링 구조를 갖는 종래 태양전지용 실리콘 웨이퍼 기판의 표면을 확대한 이미지는 도 1과 같다. 도 1을 참조하면 조직화된 웨이퍼 기판 상에는 피라미드 형태의 나노 구조가 형성되어 있음을 알 수

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있다.

[0010] 이러한 나노 텍스쳐링 구조로 형성되는 반사방지막은 넓은 파장영역 및 넓은 입사각 범위에서 반사 방지막으로서의 기능을 수행한다. 종래에는 이러한 나노 텍스쳐링 구조를 형성하기 위해 진공 중에서 염소(Cl) 기체 또는 플루오르화 황(SF_6)을 이용하여 반응성 이온 에칭(RIE: Reactive Ion Etching)을 수행하거나, 실리콘 웨이퍼 기판 표면에 금속을 매우 얇게 증착 한 후 습식에칭을 수행하였다.

[0011] 그러나, 상기 방법 중 반응성 이온 에칭법을 이용하는 방법은 복잡하고 값비싼 장비를 필요로 하는 진공 공정이 필수적이라는 문제가 있다. 한편, 습식 에칭을 이용하는 방법은 금속과 에칭액과의 촉매반응으로 실리콘을 에칭하여 나노 텍스쳐링 구조를 형성하는 방식으로 반응성 이온 에칭(RIE)을 이용하는 방식보다 공정상 간단하다는 장점이 있다. 그러나, 이 방법 또는 진공 장비를 사용하여야 하는 문제가 있다.

[0012] 따라서, 진공 장비 등을 사용하지 않기 위하여 실리콘에 전기 도금 방식을 이용하여 금속을 얇게 도금한 후 이를 에칭하여 위와 같은 방법으로 나노 텍스쳐링 구조를 형성시키기도 한다.

[0013] 한편, 실리콘 웨이퍼 기판 표면에 나노 텍스쳐링 구조를 형성시키는 또 다른 방법으로는 할 가스 분위기에서 실리콘 웨이퍼 기판 표면에 엑시머 레이저를 조사함으로써 나노 텍스쳐링 구조를 형성하는 방법이 있다.

[0014] 또한, 나노 텍스쳐링 구조가 아닌 복수 개의 홈로 이루어지는 다공성 구조를 실리콘 웨이퍼 기판에 형성시킴으로써 반사방지막을 형성하기도 한다. 그러나, 이 방법은 기판 표면에 다공성 구조를 형성시키기 위해 전기분해 장치 등 복잡한 장치를 이용한 공정을 필요로 한다는 문제가 있다.

[0015] 따라서, 간단한 공정만으로도 우수한 특성을 가지는 텍스쳐링 구조를 형성시킬 수 있는 기술에 대한 개발이 필요하다.

발명의 내용

해결 하고자하는 과제

[0016] 본 발명은 상술한 바와 같은 종래 기술의 문제점을 해결하기 위한 것으로, 진공공정 등의 필요없이 간소화된 공정만으로 실리콘 웨이퍼 기판 표면에 우수한 반사방지 특성을 갖는 나노 텍스쳐링 구조를 형성시킬 수 있는 벌크형 태양전지의 제조방법을 제공하는 데에 그 목적이 있다.

과제 해결수단

[0017] 상술한 목적을 달성하기 위한 본 발명의 일 실시형태에 따르면, 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조방법에 있어서, 상기 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 형성하는 단계를 포함하되, 상기 나노 텍스쳐링 구조 형성 단계는 금속을 촉매로 하는 에칭법에 의해 수행되는 것을 특징으로 하는 벌크형 태양전지의 제조방법이 제공된다.

[0018] 상기 나노 텍스쳐링 구조 형성 단계는, 나노 금속 입자가 혼합되어 있는 용액을 상기 실리콘 웨이퍼 기판 상에 분산시키는 단계, 에칭액을 사용하여 상기 나노 금속 입자가 분산된 실리콘 웨이퍼 기판을 에칭하는 단계, 및 상기 나노 금속 입자를 제거하는 단계를 포함할 수 있다.

[0019] 상기 나노 금속 입자의 입경은 20㎚ 내지 200㎚로 하는 것이 바람직하다.

[0020] 상기 나노 금속 입자는 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 중 적어도 하나로 하는 것이 바람직하다.

[0021] 상기 에칭액은 플루오르화 수소(HF)와 과산화수소수(H_2O_2)의 혼합용액인 것이 바람직하다.

[0022] 상기 플루오르화 수소(HF)와 과산화수소수(H_2O_2)의 혼합비는 10:1로 하는 것이 바람직하다.

[0023] 상기 용액에서 상기 나노 금속 입자의 농도는 1000ppm 내지 100000ppm 으로 하는 것이 바람직하다.

[0024] 상기 나노 금속 입자가 혼합되어 있는 용액을 분산시키는 단계는, 스프레이법(spraying), 스핀코팅법(spin

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coating), 디핑법(dipping) 중 어느 하나에 의해 수행될 수 있다.

[0025] 상기 목적을 달성하기 위한 본 발명의 벌크형 태양전지는 상기의 제조방법으로 제조되고 실리콘 웨이퍼 기판 표면에 나노크기의 패턴을 갖는 나노 텍스쳐링(texturing) 구조를 포함할 수 있다.

효 과

[0026] 본 발명에 따르면, 진공공정 등의 복잡한 공정의 필요없이 간소화된 공정만으로 실리콘 웨이퍼 기판 표면에 우수한 반사방지 특성을 갖는 나노 텍스쳐링 구조를 형성시킬 수 있다.

실시를 위한 구체적인 내용

[0027] 이하, 첨부되는 도면을 참조하여 본 발명의 실시형태들을 상세하게 설명하도록 한다.

[0028] 도 2는 본 발명의 일 실시형태에 따른 태양전지용 실리콘 웨이퍼 기판의 표면을 전자현미경으로 관찰한 이미지이다.

[0029] 도 2를 참조하면, 본 발명의 실리콘 웨이퍼 기판의 표면은 나노 패턴으로 이루어지는 나노 텍스쳐링 구조를 갖는다.

[0030] 상기 나노 텍스쳐링 구조는 나노크기의 패턴으로 이루어져 있다. 즉, 실리콘 웨이퍼 기판 상부에 나노 크기의 패턴들이 조직화되어 있는 구조이다. 나노 텍스쳐링 구조에 의하면 반사방지막(anti-reflection; AR)을 사용하는 것과 다른 특징을 얻을 수 있다. 즉, 반사방지막을 사용하면 특정 파장 대역에서만 반사방지의 효과를 얻을 수 있는 반면 나노 텍스쳐링 구조에 의하면 넓은 파장영역에서 균일하게 반사방지의 효과를 얻을 수 있다.

[0031] 나노 패턴의 크기는 태양전지의 반사방지막으로서의 기능을 최대한 발생할 수 있는 범위 내에서 선택될 수 있다. 즉, 패턴의 크기가 너무 크면 반사율이 저하될 수 있고, 반대로 패턴의 크기가 너무 작으면 반사가 발지되어 태양전지로 흡수되는 광량이 미미해지기 때문에, 그 크기를 적절하게 선택하여야 한다.

[0032] 이하, 본 발명의 태양전지용 실리콘 웨이퍼 기판의 나노 텍스쳐링 구조를 형성하는 방법에 대해 설명하기로 한다. 도 3a 내지 도 3f는 본 발명의 일 실시형태에 따른 나노 텍스쳐링 구조를 갖는 실리콘 웨이퍼 기판을 포함하는 태양전지를 제조하는 과정을 설명하는 공정도이다.

[0033] 먼저, 도 3a에 도시되는 바와 같은 실리콘 웨이퍼 기판(110) 표면에 잔류하는 네이티브 옥사이드(native oxide; 130)를 제거한다. 실리콘 웨이퍼 기판(110)의 표면에는 실리콘 웨이퍼 기판(110)의 제조 과정에서 형성되거나, 대기 중의 노출 등에 따라 형성되는 네이티브 옥사이드(130)가 잔류하게 되는데 나노 텍스쳐링 구조를 형성하기 전에 이러한 이물질을 제거해주어야 한다. 실리콘 웨이퍼 기판(110)을 플루오르화 수소(HF) 혼합용액에 담금으로써 일어나는 화학 반응에 의해 상기와 같은 네이티브 옥사이드(120)가 제거될 수 있다.

[0034] 그 후, 도 3b에 도시되는 바와 같이, 네이티브 옥사이드(120)가 제거된 실리콘 웨이퍼 기판(110) 상에 나노 금속 입자(135)가 분산되어 있는 수용액(130)을 도포하고 건조시킨다. 후에 나노 금속 입자(135)가 형성되어 있지 않은 부분의 실리콘 웨이퍼 기판(110)이 에칭됨으로써 나노 텍스쳐링 구조가 형성된다. 상기 수용액(130)에는 나노 금속 입자(135)가 약 1000ppm 내지 100000ppm 의 농도로 고르게 분산되어 있을 수 있다. 한편, 나노 금속 입자(135)의 입경은 형성하고자 하는 나노 텍스쳐링 구조의 패턴의 형태에 따라 적절하게 선택될 수 있다. 나노 금속 입자(135)의 입경이 너무 크면 나노 텍스쳐링 구조에 포함되는 패턴 간의 거리가 지나치게 멀어지게 되고, 입경이 너무 작으면 패턴이 너무 조밀하게 형성될 수 있으므로, 적절한 범위 내에서 선택될 수 있다. 일례로서 나노 금속 입자(135)의 입경을 20㎚ 내지 200㎚ 의 범위 내에서 선택할 수 있다. 한편, 나노 금속 입자의 구성 물질은 금(Au), 은(Ag), 구리(Cu), 팔라듐(Pd), 주석(Sn) 등으로 할 수 있다. 일례로서, 약 100㎚의 입경을 갖는 은(Ag)을 나노 금속 입자(135)로 선택할 수 있다.

[0035] 한편, 나노 금속 입자(135)가 혼합되어 있는 수용액(130)을 실리콘 웨이퍼 기판(110) 상에 도포하는 데에는 스프레이법(spraying), 스핀코팅법(spin coating), 디핑법(dipping) 등이 이용될 수 있다. 스프레이법은 수용액(130)을 실리콘 웨이퍼 기판(110) 상에 고르게 분사하는 방식이고, 스핀코팅법은 실리콘 웨이퍼 기판(110) 상에 수용액(130)을 떨어뜨린 후 이를 회전시켜 수용액(130)이 원심력에 의해 실리콘 웨이퍼 기판(110) 상에 코팅될 수 있도록 하는 방식이며, 디핑법은 실리콘 웨이퍼 기판(110)을 수용액(130)에 담가 코팅을 하는 방식이다. 이

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러한 방식으로 나노 금속 입자(135)가 분산되어 있는 수용액(130)이 실리콘 웨이퍼 기판(110) 상에 도포되면, 열처리 등을 통하여 이를 건조시켜 실리콘 웨이퍼 기판(110) 상에 나노 금속 입자(135)만이 남을 수 있도록 한다.

[0036] 다음으로, 실리콘 웨이퍼 기판(110)을 에칭액에 담궈 에칭(etching)한다. 상기 에칭액으로는 플루오르화 수소(HF)와 과산화수소수(H_2O_2)가 혼합되어 있는 용액을 사용할 수 있다. 본래는 플루오르화 수소(HF)와 과산화수소수(H_2O_2)가 혼합되어 있는 용액만으로는 실리콘 웨이퍼 기판(110)을 에칭시킬 수 없으나, 기판(110) 상에 분산되어 있는 나노 금속 입자(135)가 촉매로 작용하여 나노 금속 입자(135)들 사이의 공간에 노출되어 있는 실리콘 웨이퍼 기판(110)이 에칭될 수 있는 것이다. 플루오르화 수소(HF)와 과산화수소수(H_2O_2)의 혼합비는 10:1 정도로 하는 것이 바람직하다. 도 3c는 이러한 방법에 의해 에칭된 실리콘 웨이퍼 기판(110)의 단면 구조를 나타낸다. 나노 금속 입자(135)들 사이의 공간에 노출된 실리콘 웨이퍼 기판(110)이 에칭됨으로써 나노 패턴으로 형성되는 나노 텍스쳐링 구조가 형성되게 되는 것이다.

[0037] 에칭이 완료되면 순수(pure water)를 이용하여 실리콘 웨이퍼 기판(110)을 세척한 후에 금속 에칭을 수행하여 나노 금속 입자(135)를 제거한다. 도 3d는 에칭에 의해 나노 금속 입자(135)가 제거된 실리콘 웨이퍼 기판(110)의 모습을 나타낸다. 이렇게 함으로써 표면에 나노 텍스쳐링 구조가 형성된 실리콘 웨이퍼 기판(110)이 얻어질 수 있다.

[0038] 그 후, 도 3e에 도시되는 바와 같이, 상기 나노 텍스쳐링 구조가 형성된 제1전도성(예를 들면, p형)을 갖는 실리콘 웨이퍼 기판(110)에 제2전도성(예를 들면, n형)을 갖는 물질을 확산시켜 p-n 접합을 형성하고, 표면에 패시베이션 층(passivation; 150)을 형성한다. 패시베이션 층(150)은 실리콘 웨이퍼 기판(110)을 부동태화시켜 표면 결함을 최소화하기 위한 것이다. 패시베이션 층(150)은 실리콘 웨이퍼 기판(110)의 표면을 산화시킴으로써 형성될 수 있다. 즉, 상기 산화 반응에 의해 안정한 물질인 실리콘 산화물(SiO_2)이 실리콘 웨이퍼 기판(110) 표면에 형성됨으로써 패시베이션 층(150)이 형성될 수 있다. 한편, 실리콘 질화물(Si_3N_4) 등의 물질을 상기 실리콘 웨이퍼 기판(110) 표면에 증착함으로써 패시베이션 층(150)을 형성시킬 수도 있다.

[0039] 다음으로, 도 3f에 도시되는 바와 같이, 상기 패시베이션 층(150)이 형성된 실리콘 웨이퍼 기판(110) 상에 전극(170)을 형성시킴으로써 태양전지가 완성된다. 전극(170)은 통상의 인쇄법(printing) 등에 의해 형성될 수 있다.

[0040] 이러한 방법에 의하면, 진공공정 또는 전기분해공정 등을 사용하지 않고도 실리콘 웨이퍼 기판에 나노 텍스쳐링 구조를 형성할 수 있으며, 이에 따라 나노 텍스쳐링 구조 형성에 필요한 작업 공수를 간소화할 수 있고, 제조 원가가 절감될 수 있다.

[0041] 또한, 값비싼 장비 또는 복잡한 공정 없이도 나노 텍스쳐링 구조와 같은 우수한 특성의 반사방지막을 얻을 수 있다.

도면의 간단한 설명

[0042] 도 1은 종래 태양전지용 실리콘 웨이퍼 기판 표면에 형성된 나노 텍스쳐링 구조를 전자현미경으로 관찰한 이미지이다.

[0043] 도 2는 본 발명의 일 실시형태에 따른 태양전지용 실리콘 웨이퍼 기판의 표면을 전자현미경으로 관찰한 이미지이다.

[0044] 도 3a 내지 도 3f는 본 발명의 일 실시형태에 따른 태양전지용 실리콘 웨이퍼 기판을 포함하는 벌크형 태양전지의 제조과정을 설명하는 공정도이다.

[0045] <도면의 주요부분에 대한 부호의 설명>

[0046] 110: 기판 120: 네이티브 옥사이드

[0047] 130: 나노 금속 입자가 혼합된 수용액 135: 금속 나노 입자

[0048] 150: 패시베이션 층 170: 전극

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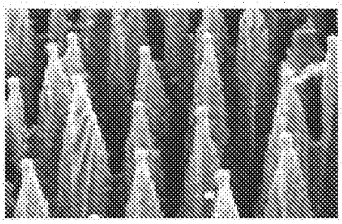
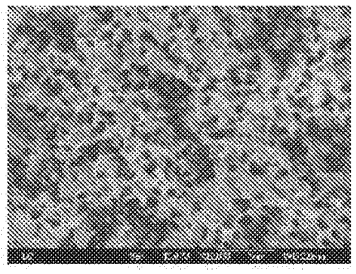
도면

도면1



도면2



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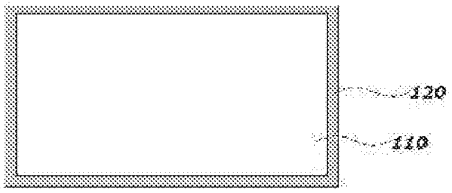

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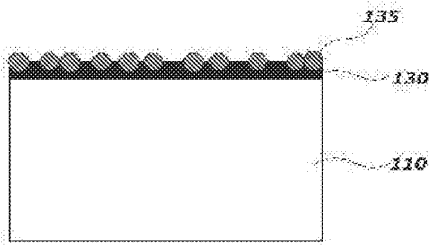
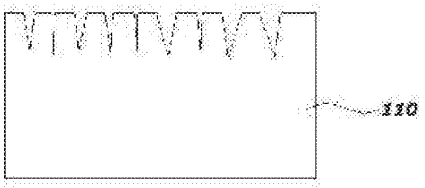
도면3b

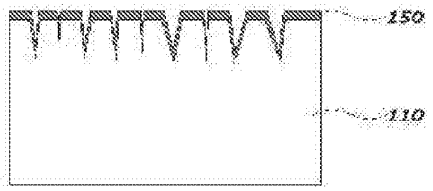


도면3c

도면3d



도면3e



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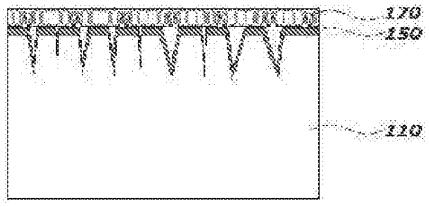
도면8



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(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

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[Fortsetzung auf der nächsten Seite]

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(54) **Title**: MULTISPECTRAL SENSOR

(54) **Bezeichnung**: MULTISPEKTRALER SENSOR

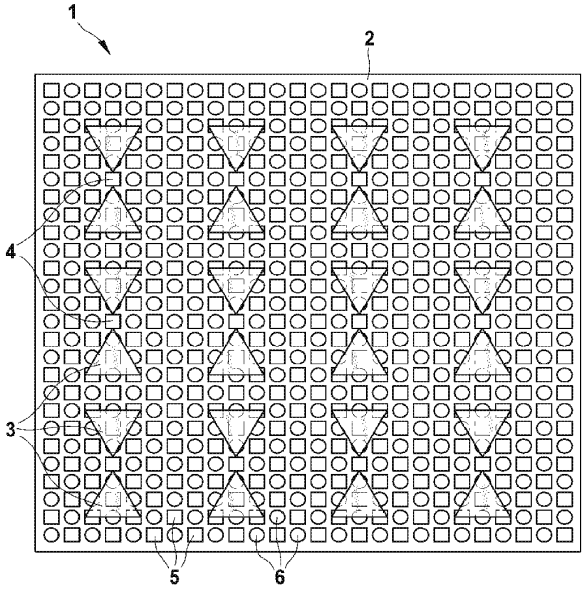

Fig. 1

(57) **Abstract**: The present invention relates to a multispectral sensor (1) comprising a complementary metal oxide semiconductor substrate (2) with a switching circuit, at least one antenna (3) - receiving means (4) combination device for detecting teraherz radiation, at least one other bolometer (5) for detecting mid-ranged infrared radiation and at least one diode (6) for detecting radiation in the visible to near infrared range, a multispectral imaging and/or spectroscopy system, method for detecting and/or examining life forms, objects and materials using such a system, as well as the use of such a sensor (1) and system.

(57) **Zusammenfassung**: Die vorliegende Erfindung betrifft einen multispektralen Sensor (1), der ein komplementäres Metall-Oxid-Halbleiter-Substrat (2) mit Schaltkreis, mindestens eine Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtung zur Detektion von Terahertzstrahlung, mindestens ein weiteres Bolometer (5) zur Detektion von mittlerer Infrarotstrahlung, und mindestens eine Diode (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs umfasst, ein multispektrales Bildgebungs- und/oder Spektroskopie-System, Verfahren zur Detektion und/oder Untersuchung von Lebewesen, Gegenständen und Materialien mit einem derartigen System sowie die Verwendung eines derartigen Sensors (1) und Systems.

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(84) Bestimmungsstaaten *(soweit nicht anders angegeben, für jede verfügbare regionale Schutzrechtsart)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), eurasisches (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), europäisches (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Veröffentlicht:

— *mit internationalem Recherchenbericht (Artikel 21 Absatz 3)*

— *vor Ablauf der für Änderungen der Ansprüche geltenden Frist; Veröffentlichung wird wiederholt, falls Änderungen eingehen (Regel 48 Absatz 2 Buchstabe h)*

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Titel

Multispektraler Sensor

Beschreibung

Die vorliegende Erfindung betrifft einen multispektralen Sensor zur Detektion von Terahertzstrahlung, Infrarotstrahlung und Strahlung des sichtbaren bis nahen Infrarot-Bereichs, ein multispektrales Bildgebungs- und/oder Spektroskopie-System, ein Verfahren zur Detektion und/oder Untersuchung von Lebewesen, Gegenständen und Materialien mit einem derartigen System sowie die Verwendung eines derartigen Sensors und Systems.

Stand der Technik

Das elektromagnetische Spektrum kann im Bereich des Terahertz-Frequenzbandes Informationen über die komplexe chemische Zusammensetzung von Stoffen, sowie über die dielektrischen Eigenschaften von Gegenständen geben. Für diese Anwendung werden derzeit recht komplexe Systeme verwendet, die beispielsweise gepulste Laserquellen enthalten. Ein wesentlicher Schwachpunkt der angebotenen Terahertz-Systeme besteht neben der Komplexität darin, dass eine Messung allein im Terahertz-Frequenzband wenig aussagekräftig ist und häufig durch parallele Messungen im sichtbaren oder infraroten Frequenzband ergänzt werden muss. Dies erfolgt herkömmlicherweise durch die parallele Verwendung mehrerer Detektoren oder Detektierungssysteme, die eine komplexe gegenseitige optische Ausrichtung erfordern, was hohe Kosten des Gesamtsystems zur Folge hat.

Offenbarung der Erfindung

Vorteile der Erfindung

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Der erfindungsgemäße multispektrale Sensor umfassend

- ein komplementäres Metall-Oxid-Halbleiter-Substrat mit Schaltkreis, und
- mindestens eine Antenne-Empfängermittel-Kombinationsvorrichtung zur Detektion von Terahertzstrahlung, und
- mindestens eine Vorrichtung zur Detektion von mittlerer Infrarotstrahlung, und
- mindestens eine Diode zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs

hat zum einen den Vorteil, dass alle Bauelemente des Sensors bei Raumtemperatur betrieben werden können. Daher bedarf ein erfindungsgemäßer Sensor **1** keiner Kühlung, insbesondere keiner kryoskopischen Kühlung. Zum anderen hat der erfindungsgemäße Sensor **1** den Vorteil, dass darauf verschiedenen Funktionen auf einem einzigen Bauteil vereint werden, wodurch vorteilhafterweise ein einziger Sensor zur Bewältigung komplexer Detektierungsanwendungen genügt. Darüber hinaus entfällt vorteilhafterweise das aufwendige Einstellen verschiedener Sensoren und es wird nur eine einzige breitbandige, vorzugsweise reflektive, Optik benötigt. Der erfindungsgemäße Sensor ermöglicht weiterhin vorteilhafterweise eine parallele, im Idealfall Echtzeit-Detektion von elektromagnetischer Strahlung im sichtbaren-nah-infraroten, mittel-infraroten und Terahertz-Bereich. Ferner können die erfindungsgemäßen Sensoren langfristig betrachtet zu niedrigen Produktionsstückkosten hergestellt werden, was auch eine Anwendung in Massenprodukten ermöglicht.

Zeichnungen

Weitere Vorteile und vorteilhafte Ausgestaltungen des erfindungsgemäßen Gegenstandes werden durch die Zeichnungen veranschaulicht und in der nachfolgenden Beschreibung erläutert. Dabei ist zu beachten, dass die Figuren nur beschreibenden Charakter haben und nicht dazu gedacht sind, die Erfindung in irgendeiner Form einzuschränken.

Fig. 1 zeigt eine Draufsicht auf eine Ausführungsform eines erfindungsgemäßen multispektralen Sensors.

Figur 1 zeigt, dass der erfindungsgemäße Sensor **1** ein komplementäres Metall-Oxid-Halbleiter-Substrat **2** mit einem nicht dargestellten Schaltkreis umfasst. Derartige Substrate werden üblicherweise auch als CMOS-Substrat („complementary metal oxide semiconductor") bezeichnet. Erfindungsgemäß sind auf dem CMOS-Substrat **2** mindestens eine Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zur Detektion von Terahertzstrahlung, mindestens eine Vorrichtung **5** zur Detektion von mittlerer Infrarotstrahlung und mindestens eine Diode **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs angeordnet.

Im Rahmen der vorliegenden Erfindung wird unter dem Begriff „Terahertzstrahlung" elektromagnetische Strahlung in einem Bereich von etwa ≥ 15 µm bis etwa ≤ 1000 µm, und unter dem Begriff „mittlerer Infrarotstrahlung" elektromagnetische Strahlung in einem Bereich von etwa ≥ 1 µm bis etwa < 15 µm, und unter dem Begriff „Strahlung des sichtbaren bis nahen Infrarot-Bereichs" elektromagnetische Strahlung in einem Bereich von etwa $\geq 0{,}380$ µm bis etwa < 1 µm, verstanden.

Das Detektierungsintervall des erfindungsgemäßen Sensors **1** kann im Terahertz-Bereich sowohl $> 0{,}3$ Terahertz bis ≤ 20 Terahertz als auch beispielsweise $\geq 0{,}3$ Terahertz oder $\geq 0{,}5$ Terahertz oder ≥ 1 Terahertz bis ≤ 3 Terahertz oder ≤ 5 Terahertz oder ≤ 10 Terahertz, sein. Entsprechend kann das Detektierungsintervall des erfindungsgemäßen Sensors **1** im Terahertz-Bereich sowohl ≥ 15 µm bis < 1000 µm als auch beispielsweise ≥ 30 µm oder ≥ 60 µm oder ≥ 100 µm bis ≤ 300 µm oder ≤ 600 µm oder < 1000 µm, sein.

Ebenso kann das Detektierungsintervall des erfindungsgemäßen Sensors **1** im mittleren Infrarot-Bereich sowohl > 20 Terahertz bis ≤ 300 Terahertz als auch $\geq 21{,}4$ Terahertz bis $\leq 37{,}5$ Terahertz oder ≥ 60 Terahertz oder ≤ 100 Terahertz, sein. Entsprechend kann das Detektierungsintervall des erfindungsgemäßen Sensors **1** im mittleren Infrarot-Bereich sowohl ≥ 1 µm bis etwa < 15 µm als auch beispielsweise ≥ 3 µm bis ≤ 5 µm oder ≥ 8 µm bis ≤ 14 µm, sein.

Analog kann das Detektierungsintervall des erfindungsgemäßen Sensors **1** im sichtbaren bis nah-infraroten Bereich > 300 Terahertz bis ≤ 790 Terahertz sein.

Im Rahmen der vorliegenden Erfindung muss eine Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zur Detektion von Terahertzstrahlung beziehungsweise eine Vorrichtung **5** zur Detektion von mittlerer Infrarotstrahlung beziehungsweise eine Diode **6** zur

Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs folglich nicht den kompletten jeweiligen Strahlungsbereich detektieren.

Im Rahmen einer bevorzugten Ausführungsform der vorliegenden Erfindung weist der erfindungsgemäße Sensor **1** mindestens zwei unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern auf.

Eine Unterteilung des Terahertz-Bereichs in mindestens zwei, insbesondere schmalbandige, Unterbänder, hat den Vorteil, dass sich schmalbandige Antennen **3** besser an das Empfangsmittel **4** anpassen, insbesondere koppeln, lassen, wodurch bei geeigneter Anordnung die Empfindlichkeit („Performance") des Gesamtsystems verbessert werden kann.

Der erfindungsgemäße Sensor **1** weist daher vorzugsweise mindestens zwei unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen auf, die derart ausgebildet sind, dass der Terahertz-Bereich in mindestens zwei, insbesondere schmalbandige, Unterbänder aufgeteilt wird, welche den Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zugeordnet sind.

Darüber hinaus kann der erfindungsgemäße Sensor **1** mindestens zwei unterschiedliche Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern aufweisen.

Ferner kann der erfindungsgemäße Sensor **1** auch mindestens zwei unterschiedliche Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern aufweisen.

Wie Figur 1 zeigt, weist ein erfindungsgemäßer Sensor **1** vorzugsweise eine Vielzahl, beispielsweise gleicher und/oder unterschiedlicher (nicht dargestellt), Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs auf.

Als Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtung haben sich im Rahmen der vorliegenden Erfindung Antenne-Bolometer-Kombinationsvorrichtungen und/oder Antenne-

Diode-Kombinationsvorrichtungen, insbesondere Antenne-Bolometer-, Antenne-Schottky-Diode- und/oder Antenne-MIM-Diode-Kombinationsvorrichtungen, als besonders vorteilhaft erwiesen, da derartige Kombinationsvorrichtungen keine Kühlung, insbesondere keine kryoskopische Kühlung benötigen. Dabei wird im Sinn der vorliegenden Erfindung unter einer MIM-Diode eine Metall-Isolator-Metall-Diode („metal insulator metal diode") verstanden. Die Variation dieser unterschiedlichen **3**-Empfängermittel-**4**-Kombinationsvorrichtungen bietet eine Möglichkeit unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

Im Rahmen der vorliegenden Erfindung weist eine Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtung mindestens eine an das Empfängermittel **4**, insbesondere kapazitiv, gekoppelte Antennen **3** auf. Die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtung kann jedoch auch mindestens zwei Antennen **3** aufweisen, welche an das Empfängermittel **4**, insbesondere kapazitiv, gekoppelt sind. Die Zahl der Antennen bietet eine weitere Möglichkeit unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

Beim Einsatz eines Bolometers als Empfängermittel **4** dient die Antenne **3** dazu Terahertzstrahlung zu absorbieren, welche in dem mit der Antenne **3**, insbesondere kapazitiv, gekoppelten Bolometer in Wärme umgewandelt wird, wobei eine resultierende Widerstandsänderung des Bolometers gemessen wird. Bei dem Bolometer kann es sich dabei um ein Mikrobolometer handeln. Das Bolometer **4** kann im Rahmen der vorliegenden Erfindung ein in etwa $\geq 25\ \mu m^2$ bis $\leq 4900\ \mu m^2$, insbesondere $\geq 625\ \mu m^2$ bis $\leq 2500\ \mu m^2$, großes schichtförmiges Substrat aufweisen, welches mittels zwei elektrisch leitenden Stützen beabstandet zu dem CMOS-Substrat **2** angeordnet ist. Dabei kann das schichtförmige Substrat sowohl polygon, insbesondere rechteckig und/oder viereckig, als auch im Wesentlichen unrund, insbesondere ellipsoid oder kreisförmig, ausgestaltet sein. Das schichtförmige Substrat kann dabei amorphes Silizium oder Vanadiumoxid umfassen. Das schichtförmige Substrat kann beispielsweise parallel zu dem CMOS-Substrat **2** angeordnet sein. Die Bolometerausgestaltung bietet eine weitere Möglichkeit unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

Beim Einsatz einer Diode **4**, insbesondere einer Schottky- oder MIM-Diode, als Empfängermittel **4** wird das von der Antenne **3** empfangene Terahertzsignal gleichgerichtet beziehungsweise bei einer heterodynen Empfangslösung mit einem weiteren Terahertzsignal in ein Zwischenfrequenzsignal gemischt. Die Diodenausgestaltung bietet eine weitere Möglichkeit unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

Im Rahmen der vorliegenden Erfindung können mehrere, insbesondere alle, Antennen **3**, wie in Figur 1 gezeigt, in einer Ebene angeordnet sein. Ebenso können im Rahmen der vorliegenden Erfindung mehrere, insbesondere alle, Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung beziehungsweise mehrere, insbesondere alle, Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs jeweils in einer Ebene angeordnet sein. Wie in Figur **1** gezeigt, können die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs dabei in einer gemeinsamen Ebene angeordnet sein.

Im Rahmen einer Ausführungsform der vorliegenden Erfindung ist mindestens eine Antenne **3** beziehungsweise sind die Antennen **3** der Antennenebene bezüglich mindestens einer Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und/oder mindestens einer Diode **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs, insbesondere bezüglich der Ebene der Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und/oder der Ebene der Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs, strahlungsseitig angeordnet.

Durch unterschiedliche Antennendesigns können Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen Absorptionseigenschaften hinsichtlich Frequenz und Polarisation im Terahertzband realisiert werden. Unterschiedliche Antennendesigns bieten eine weitere, insbesondere bevorzugte, Möglichkeit unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

Dabei kann eine Antenne **3** sowohl wie in Figur 1 gezeigt flächig als auch nicht-flächig ausgestaltet sein. Beispielsweise kann eine Antenne **3** im Rahmen der vorliegenden Erfindung

polygon, insbesondere dreieckig, rechteckig und/oder viereckig, im Wesentlichen unrund, insbesondere ellipsoid oder kreisförmig, oder spiralförmig ausgestaltet sein.

Im Rahmen einer Ausführungsform der vorliegenden Erfindung weist der erfindungsgemäße Sensor **1** mindestens zwei Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen mit unterschiedlichem Antennendesign auf. Beispielsweise können mehrere Antennendesigns, insbesondere selektiv, auf einem Sensor **1** kombiniert werden, welche mehrere, beispielsweise beabstandete, Frequenzbänder im Terahertz-Bereich zur Folge haben, welche auf spezielle zu detektierende Frequenzbereiche, beispielsweise für Sprengstoffe charakteristische Frequenzbereiche, abgestimmt sind und dadurch dem erfindungsgemäßen Sensor **1** vorteilhafterweise eine Spektroskopie- und/oder Frequenzselektions-Funktion verleihen.

Im Rahmen einer bevorzugten Ausführungsform der vorliegenden Erfindung weist der erfindungsgemäße Sensor **1** daher mindestens zwei unterschiedliche Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen auf, die, insbesondere durch unterschiedliche Antennendesigns, auf speziell/bevorzugt zu detektierende Frequenzbereiche im Terahertz-Bereich abgestimmt sind.

Im Rahmen einer bevorzugten Ausführungsform der vorliegenden Erfindung umfasst eine Antenne **3** eine, insbesondere dünne, Metallschicht und/oder Halbleiterschicht und/oder eine Schicht aus einem oder mehreren elektrisch leitenden Polymeren und/oder eine auf Kohlenstoffnanoröhren („carbon nanotubes“) basierende Schicht. Insbesondere kann eine Antenne **3** dabei aus einer, insbesondere dünnen, Metallschicht oder Halbleiterschicht oder Schicht aus einem oder mehreren elektrisch leitenden Polymeren oder auf Kohlenstoffnanoröhren („carbon nanotubes“) basierenden Schicht ausgebildet sein. Beispielsweise kann die Metallschicht aus Gold ausgebildet sein. Die Halbleiterschicht kann aus einem Halbleiter mit einer breiten Bandlücke („wide band gap semiconductor“), beispielsweise Indium-Zinn-Oxyd, Zinkoxid, Alluminiumnitrid, Galliumnitrid, und/oder Siliciumcarbid, insbesondere dotiertes Indium-Zinn-Oxyd, Zinkoxid, Alluminiumnitrid, Galliumnitrid, und/oder Siliciumcarbid, ausgebildet sein.

Im Rahmen einer besonders bevorzugten Ausführungsform der vorliegenden Erfindung ist die Metallschicht und/oder Halbleiterschicht durchlässig für Strahlung des sichtbaren bis nahen Infrarot-Bereichs und/oder des mittleren Infrarot-Bereichs. Dies hat den Vorteil, dass unterhalb der Antenne/n **3** einer Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtung eine oder mehrere Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und/oder eine oder

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mehrere Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs angeordnet sein können. Dabei dient der Begriff „unterhalb" nicht dazu die Ausrichtung bezüglich der Gravitationsrichtung, sondern bezüglich der erwarteten Strahlungsrichtung zu definieren, wobei „unterhalb einer Antenne" als auf der strahlungsabgewandten Seite einer Antenne **3** zu verstehen ist.

Im Rahmen der in Figur 1 gezeigten Ausführungsform sind unterhalb den Antennen **3** beziehungsweise zwischen den Antennen **3** und dem komplementären Metall-Oxid-Halbleiter-Substrat **2** zahlreiche Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs angeordnet. Dabei besteht zwischen den Antennen **3** und den Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung beziehungsweise den Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs keine galvanisch leitende Verbindung. Dabei bedeutet „keine galvanisch leitende Verbindung", dass keine „direkte" Leitung über eine, beispielsweise metallische, Leitung vorliegt, wobei eine kapazitive und/oder induktive „indirekte" Leitung nicht ausgeschlossen ist. Eine galvanisch leitende Verbindung zwischen den Antennen **3** und den Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung beziehungsweise den Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs kann beispielsweise dadurch vermieden werden, dass die Antennen **3** auf einem oder mehreren, nicht dargestellten, Träger/n, beispielsweise einer Trägerschicht, insbesondere aus einem oder mehreren nicht galvanisch leitenden Polymeren, aus einem galvanisch nicht-leitenden Material angeordnet sind.

Als Vorrichtung **5** zur Detektion von mittlerer Infrarotstrahlung können im Rahmen der vorliegenden Erfindung Bolometer und/oder MIM-Dioden eingesetzt werden. Der Einsatz von Bolometern und MIM-Dioden bietet daher eine Möglichkeit unterschiedliche Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen. Beim Einsatz von Bolometern **5** als Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung sind die Bolometer **5** vorzugsweise, wie in Figur 1 gezeigt, freistehend ausgebildet und angeordnet.

Als Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung eignet sich beispielsweise ein Bolometer, welches ein in etwa $\geq 25\ \mu m^2$ bis $\leq 4900\ \mu m^2$, insbesondere $\geq 625\ \mu m^2$ bis $\leq 2500\ \mu m^2$, großes schichtförmiges Substrat aufweist. Das schichtförmige Substrat kann dabei insbesondere mittels zwei galvanisch leitenden Stützen beabstandet zu dem CMOS-Substrat **2** angeordnet sein. Dabei kann das schichtförmige Substrat sowohl polygon, insbesondere

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rechteckig und/oder viereckig, als auch im Wesentlichen unrund, insbesondere ellipsoid oder kreisförmig, ausgestaltet sein. Das schichtförmige Substrat kann dabei amorphes Silizium oder Vanadiumoxid umfassen. Das schichtförmige Substrat ist vorzugsweise parallel zu dem CMOS-Substrat **2** angeordnet. Durch den Abstand zwischen dem schichtförmigen Substrat und dem CMOS-Substrat **2** kann dabei vorteilhafterweise der Wellenlängenbereich der zu detektierenden Strahlung eingestellt werden. Für eine optimale Detektion entspricht der Abstand vorzugsweise einem Viertel der Wellenlänge der zu detektierenden Strahlung. Eine Änderung des Abstands zwischen dem schichtförmigen Substrat und dem CMOS-Substrat **2** bietet daher eine weitere Möglichkeit unterschiedliche Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern zur Verfügung zu stellen.

Als Dioden eignen sich beispielsweise Dioden, insbesondere Fotodioden, die in CMOS-bildgebenden Detektoren verwendet werden.

Wie Figur 1 veranschaulicht kann der erfindungsgemäße Sensor **1**, insbesondere ein Teil des erfindungsgemäßen Sensors **1**, beispielsweise das CMOS-Substrat **2**, die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtung/en, die Vorrichtung/en **5** zur Detektion von mittlerer Infrarotstrahlung und die Diode/n **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs des Sensors **1**, vorteilhafterweise monolithisch ausgestaltet sein. Dabei bedeutet der Begriff „monolithisch", dass die Einheiten **2, 3, 4, 5, 6** des Sensors **1** eine, insbesondere untrennbare, Einheit bilden. Insbesondere kann es sich bei dem erfindungsgemäßen Sensor um einen monolithisch integrierten Chip handeln.

Der in Figur 1 nicht dargestellte Schaltkreis, die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs sind im Rahmen der vorliegenden Erfindung vorzugsweise derart ausgebildet und angeordnet, dass die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs, insbesondere unabhängig voneinander, beschaltet und/oder ausgelesen werden können. Zum Auswerten der ausgelesenen Messergebnisse weist der erfindungsgemäße Sensor **1** vorzugsweise eine Auswertelektronik auf. Darüber hinaus weist der Sensor vorzugsweise eine multispektrale Optik, beispielsweise eine reflektive Optik auf der Basis von Spiegeln, auf. Eine derartige multispektrale Optik ist zweckmäßigerweise bezüglich der auf dem CMOS-Substrat **2** angeordneten Bauelemente **3, 4, 5, 6** strahlungsseitig angeordnet.

Die Auswertelektronik und multispektrale Optik kann, muss jedoch nicht, in den monolithischen Teil des Sensors **1** integriert sein.

Figur 1 zeigt, dass die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs rasterförmig angeordnet sein können. Dementsprechend können die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs auch als „Pixel" bezeichnet werden. Im Rahmen einer Ausführungsform der vorliegenden Erfindung sind die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs als Pixel eines Rasters von mindestens 20 mal 20, beispielsweise von mindestens 50 mal 50, insbesondere von mindestens 100 mal 100, Pixeln auf dem Sensor **1** angeordnet. Die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs können dabei in einem symmetrischen Muster auf dem Sensor **1** angeordnet sein. Vorzugsweise sind die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen, die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs dabei, wie in Figur 1 gezeigt, gleichmäßig auf dem Sensor **1** verteilt angeordnet. Insbesondere können dabei die Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und die Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs alternierend angeordnet sein. Die Zahl an Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen kann im Rahmen der vorliegenden Erfindung geringer als die der Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und der Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs sein. Die Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen können dann beispielsweise, wie in Figur 1 gezeigt, in regelmäßigen Abständen anstelle von einer Vorrichtung **5** zur Detektion von mittlerer Infrarotstrahlung oder Diode **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs in der ansonsten alternierenden Anordnung von Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung und Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs angeordnet werden.

Das Verhältnis von Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zu Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung kann im Rahmen der vorliegenden Erfindung in einem Bereich von $\geq$ 1:100 bis $\leq$ 100:1, beispielsweise von $\geq$ 1:50

bis ≤ 50:1, insbesondere von ≥ 1:30 bis ≤ 30:1, und/oder das Verhältnis von Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zu Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs in einem Bereich von ≥ 1:100 bis ≤ 100:1, beispielsweise von ≥ 1:50 bis ≤ 50:1, insbesondere von ≥ 1:30 bis ≤ 30:1, und/oder das Verhältnis von Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung zu Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs in einem Bereich von ≥ 1:50 bis ≤ 50:1, beispielsweise von ≥ 1:10 bis ≤ 10:1, insbesondere von ≥ 1:3 bis ≤ 3:1, liegen. Beispielsweise kann das Verhältnis von Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zu Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung ≥ 1:5, beispielsweise ≥ 1:10, insbesondere ≥ 1:20 , und/oder das Verhältnis von Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zu Dioden **6** ≥ 1:5, beispielsweise ≥ 1:10, insbesondere von ≥ 1:20, und/oder das Verhältnis von Vorrichtungen **5** zur Detektion von mittlerer Infrarotstrahlung zu Dioden **6** zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs etwa 1:1, sein.

Ferner betrifft die vorliegende Erfindung ein multispektrales Bildgebungs- und/oder Spektroskopie-System, welches einen erfindungsgemäßen Sensor **1**, welcher als Detektor dient, und eine Terahertzstrahlungsquelle aufweist. Dabei können der Sensor **1** und die Terahertzstrahlungsquelle bezüglich des zu untersuchenden Objektes sowohl derart angeordnet sein, dass der Sensor **1** die nach dem Durchstrahlen des Objektes verbleibende Strahlung detektiert als auch dass der Sensor **1** die von dem Objekt reflektierte und/oder gestreute Strahlung detektiert. Folglich können die Terahertzstrahlungsquelle, der Sensor **1** und das Objekt sowohl entlang einer Achse angeordnet sein, wobei das Objekt zwischen der Terahertzstrahlungsquelle und dem Sensor angeordnet ist, als auch nicht entlang einer Achse zueinander angeordnet sein.

Das erfindungsgemäße System ermöglicht vorteilhafterweise eine Echtzeit-Spektroskopie im Terahertz-Bereich sowie eine bildgebende Detektierung im Terahertz-Bereich sowie im Infrarot- und sichtbaren und nah-infraroten Bereich.

Darüber hinaus betrifft die vorliegende Erfindung ein Verfahren zur Detektion und/oder Untersuchung von Lebewesen, insbesondere Menschen und Tieren, Gegenständen und Materialien, mit einem erfindungsgemäßen System. Insbesondere kann dieses Verfahren auf Frequenzbereichsspektroskopie basieren. Vorzugsweise strahlt die Terahertzquelle in dem erfindungsgemäßen Verfahren ein schmales Terahertzband, beispielsweise mit einer Breite von

etwa ≥ 20 Gigahertz bis etwa ≤ 200 Gigahertz, insbesondere von etwa ≥ 60 Gigahertz bis etwa ≤ 100 Gigahertz, aus, welches innerhalb eines breiten Frequenzbereichs, beispielsweise in einem Bereich von etwa ≥ 0,3 Terahertz bis etwa ≤ 20 Terahertz, beispielsweise von ≥ 0,3 Terahertz oder von ≥ 0,5 Terahertz oder von ≥ 1 Terahertz bis ≤ 3 Terahertz oder bis ≤ 5 Terahertz oder bis ≤ 10 Terahertz, verändert wird, wobei die transmittierte, reflektierte und/oder gestreute Strahlung durch den erfindungsgemäßen Sensor **1** detektiert, insbesondere gemessen wird. Das Messergebnis des erfindungsgemäßen Sensors **1** kann dabei durch ein Ausgabegerät, beispielsweise ein Display, einen Bildschirm oder einen Drucker, ausgegeben werden.

Weiterhin betrifft die vorliegende Erfindung die Verwendung eines erfindungsgemäßen Sensors **1**, eines erfindungsgemäßen Systems und/oder eines erfindungsgemäßen Verfahrens im Überwachungs/Sicherheitstechnik-, Transport-, Produktions-, Life-Science- und/oder Gesundheitsbereich. Insbesondere betrifft die vorliegende Erfindung die Verwendung eines erfindungsgemäßen Sensors **1**, eines erfindungsgemäßen Systems und/oder eines erfindungsgemäßen Verfahrens zur Detektion und/oder Untersuchung von Lebewesen, insbesondere Menschen und Tieren, Gegenständen und Materialien, insbesondere Sprengstoffen, beispielsweise bei Sicherheitskontrollen an Grenzen, in Transitgebäuden, wie Flughäfen und Bahnhöfen, in Transportmitteln, wie Bahnen, Bussen, Flugzeugen und/oder Schiffen, und/oder bei Großveranstaltungen, zur Einbruchssicherung von Gebäuden, Räumen und Fortbewegungsmitteln, zu medizinischen Zwecken und/oder zur zerstörungsfreien Überprüfung eines Werkstücks („non-destructive testing"), insbesondere von Werkstücken aus Kunststoff.

Ansprüche

1. Multispektraler Sensor (1), umfassend
   - ein komplementäres Metall-Oxid-Halbleiter-Substrat (2) mit Schaltkreis, und
   - mindestens eine Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtung zur Detektion von Terahertzstrahlung, und
   - mindestens eine Vorrichtung (5) zur Detektion von mittlerer Infrarotstrahlung, und
   - mindestens eine Diode (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs.

2. Sensor (1) nach Anspruch 1, dadurch gekennzeichnet, dass
   - die Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtung eine Antenne-Bolometer-Kombinationsvorrichtung oder eine Antenne-Diode-Kombinationsvorrichtung, insbesondere eine Antenne-Bolometer-, Antenne-Schottky-Diode- oder eine Antenne-Metall-Isolator-Metall-Diode-Kombinationsvorrichtung, und/oder
   - die Vorrichtung (5) zur Detektion von mittlerer Infrarotstrahlung ein Bolometer oder eine Metall-Isolator-Metal-Diode,

   ist.

3. Sensor (1) nach Anspruch 1 oder 2, dadurch gekennzeichnet, dass der Sensor (1)
   - mindestens zwei unterschiedliche Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern; und/oder
   - mindestens zwei unterschiedliche Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern, und/oder,

- mindestens zwei unterschiedliche Diode (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs mit unterschiedlichen zueinander beabstandeten oder aneinander angrenzenden oder überlappenden Detektionsfrequenzbändern,

aufweist.

4. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass der Sensor (1) mindestens zwei unterschiedliche Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen aufweist, die derart ausgebildet sind, dass der Terahertz-Bereich in mindestens zwei Unterbänder aufgeteilt wird, welche den Antenne-**3**-Empfängermittel-**4**-Kombinationsvorrichtungen zugeordnet sind.

5. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass der Sensor (1) mindestens zwei Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen mit unterschiedlichem Antennendesign aufweist.

6. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass der Sensor (1) mindestens zwei unterschiedliche Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen auf, die auf bevorzugt zu detektierende Frequenzbereiche im Terahertz-Bereiche abgestimmt sind.

7. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass der Sensor (1) eine Vielzahl von Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen, Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung und Dioden (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs aufweist, wobei die Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen, Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung und Dioden (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs rasterförmig angeordnet sind.

8. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen, Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung und Dioden (6) zur Detektion von Strahlung des

sichtbaren bis nahen Infrarot-Bereichs als Pixel eines Rasters von mindestens 20 mal 20, beispielsweise von mindestens 50 mal 50, insbesondere von mindestens 100 mal 100, Pixeln auf dem Sensor (1) angeordnet sind.

9. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen, Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung und Dioden (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs in einem symmetrischen Muster auf dem Sensor (1) angeordnet sind.

10. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die Antenne/n (3) eine Metallschicht und/oder eine Halbleiterschicht und/oder eine Schicht aus einem oder mehreren elektrisch leitenden Polymeren und/oder eine auf Kohlenstoffnanoröhren basierende Schicht umfassen, welche durchlässig für Strahlung des sichtbaren bis nahen Infrarot-Bereichs und/oder Infrarotstrahlung ist.

11. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass unterhalb der Antenne/n (3) einer Antenne-(3)-Empfängermittel-(4)-Kombinationsvorrichtungen eine oder mehrere Vorrichtungen (5) zur Detektion von mittlerer Infrarotstrahlung und/oder eine oder mehrere Dioden (6) zur Detektion von Strahlung des sichtbaren bis nahen Infrarot-Bereichs angeordnet sind.

12. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass die Antenne/n (3) auf einem oder mehreren Träger/n aus einem galvanisch nicht-leitenden Material angeordnet sind.

13. Sensor (1) nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, dass der Sensor (1) eine multispektrale Optik, insbesondere eine reflektive Optik, und/oder eine Auswertelektronik aufweist.

14. Multispektrales Bildgebungs- und/oder Spektroskopie-System, umfassend einen Sensor nach einem der vorhergehenden Ansprüche und eine Terahertzstrahlungsquelle.

15. Verfahren zur Detektion und/oder Untersuchung von Lebewesen, insbesondere Menschen und Tieren, Gegenständen und Materialien, mit einem System nach Anspruch 14, in dem die Terahertzquelle ein schmales Terahertzband ausstrahlt, welches innerhalb eines breiten Frequenzbereichs verändert wird, wobei die transmittierte, reflektierte und/oder gestreute Strahlung durch den erfindungsgemäßen Sensor (1) detektiert wird.

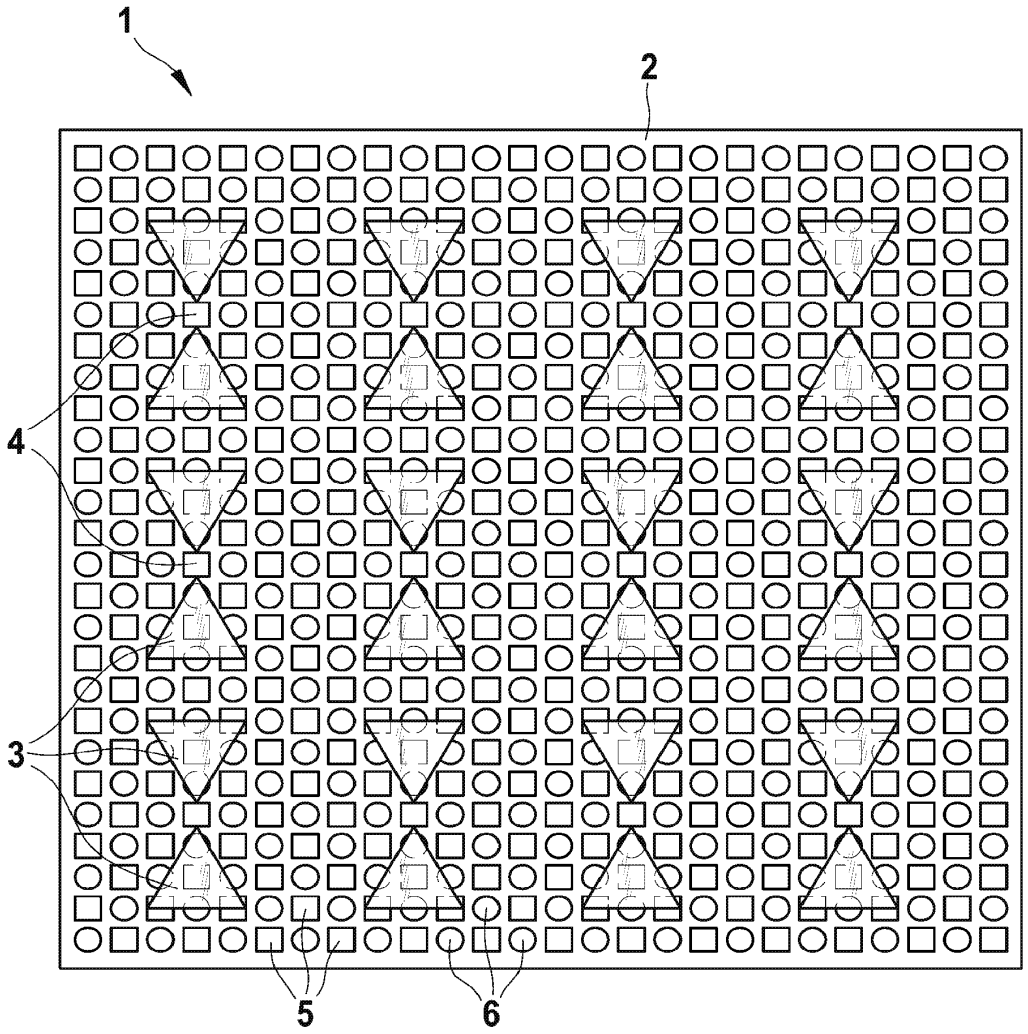

Fig. 1

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[Continued on next page]

(54) Title: A TEMPERATURE CONTROL DEVICE FOR OPTOELECTRONIC DEVICES

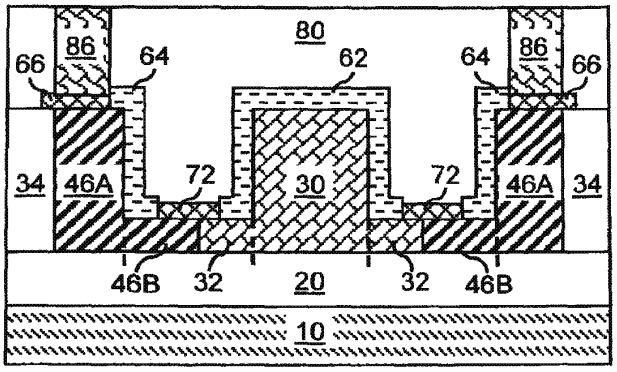

FIG. 9B

(57) Abstract: Current may be passed through an n-doped semiconductor region, a recessed metal semiconductor alloy portion, and a p-doped semiconductor region so that the diffusion of majority charge carriers in the doped semiconductor regions transfers heat from or into the semiconductor waveguide through Peltier-Seebeck effect. Further, a temperature control device may be configured to include a metal semiconductor alloy region located in proximity to an optoelectronic device, a first semiconductor region having a p-type doping, and a second semiconductor region having an n-type doping. The temperature of the optoelectronic device may thus be controlled to stabilize the performance of the optoelectronic device.

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A TEMPERATURE CONTROL DEVICE FOR OPTOELECTRONIC DEVICES

BACKGROUND

The present invention relates to a semiconductor structure, and particularly to a temperature control device for an optoelectronic device and a germanium photodetector for silicon waveguide, and methods of manufacturing the same, and methods of operating the same.

A semiconductor waveguide may be employed in microphotonic devices to enable high efficiency long range transmission of light over distances in the micrometer range or in the millimeter range. The semiconductor waveguide typically employs a single crystalline semiconductor material to minimize signal loss due to absorption of light. The semiconductor material in the semiconductor waveguide has a relative high refractive index. For example, silicon and germanium have a refractive index of about 3.45 and about 4.0, respectively. A dielectric material having a lower refractive constant surrounds the semiconductor waveguide so that a total reflection condition is satisfied at the interface between the semiconductor waveguide and the dielectric material for light impinging on the interface at a glancing angle. The semiconductor wave guide may thus be employed to transmit light having a wavelength greater than the wavelength corresponding to the band gap of the semiconductor material. Typically, infrared lights are employed in the semiconductor waveguide.

Many microphotonic devices manipulate the light in the semiconductor waveguide in some way. For example, the light in the semiconductor waveguide may be absorbed, reflected, or induced to change the phase. Many of the prior art methods that accomplish such optical manipulation employ exotic materials or special processing steps that are not typically employed in standard complementary metal-oxide-semiconductor (CMOS) processing steps, thereby increasing the manufacturing cost and processing complexity.

In view of the above, there exists a need to provide a structure that manipulates the light in a semiconductor waveguide with standard CMOS processing steps, and methods of manufacturing the same. Particularly, there exists a need to provide a structure that

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modulates the phase of the light in the semiconductor waveguide with standard CMOS processing steps, and methods of manufacturing the same.

Further, performance of many optoelectronic devices is temperature sensitive. For example, performance of a semiconductor laser device is significantly affected by temperature variation. In a semiconductor chip integrating conventional semiconductor devices and optoelectronic devices, the performance of optoelectronic devices may be affected significantly due to the heat generated by conventional semiconductor devices and transferred to the optoelectronic devices. Thus, it is necessary to stabilize the temperature of the optoelectronic devices to provide stable operation of the optoelectronic devices within the semiconductor chip.

While placing optoelectronic devices at a location far away from the conventional semiconductor devices the thermal effect on the performance of the optoelectronic devices, such a design lowers the areal density of the conventional semiconductor devices or the optoelectronic devices. Thus, an integrated semiconductor chip including conventional semiconductor devices and optoelectronic devices at high density without adverse impact on the performance of the optoelectronic devices due to the thermal effects on the optoelectronic devices is desired.

BRIEF SUMMARY

The present invention provides a semiconductor waveguide having an integrated thermoelectric temperature control device to enable phase shifting of the light in the semiconductor waveguide and an optoelectronic device having an integrated thermoelectric temperature control device to control the temperature of the optoelectronic device.

In one embodiment of the present invention, a semiconductor waveguide is formed integrally with non-recessed semiconductor regions that are adjoined to the semiconductor waveguide through a recessed semiconductor portion having a lesser thickness than the semiconductor waveguide. One of the non-recessed semiconductor portions and an adjoining region of the recessed semiconductor portion are doped with p-type dopants to form a p-doped

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semiconductor region, and another of the non-recessed semiconductor portions and an adjoining region of the recesses semiconductor portion are doped with n-type dopants to form an n-doped semiconductor region. After forming a dielectric spacer that covers sidewalls of the p-doped semiconductor region and the n-doped semiconductor region, the recessed semiconductor portion is metallized to form a recessed metal semiconductor alloy portion. Current is passed through the n-doped semiconductor region, the recessed metal semiconductor alloy portion, and the p-doped semiconductor region. The diffusion of majority charge carriers in the doped semiconductor regions transfers heat from or into the semiconductor waveguide through Peltier-Seebeck effect. The temperature change in the semiconductor waveguide alters refractive index of the semiconductor waveguide, which may be employed to modulate the phase of the light passing through the semiconductor waveguide.

According to an aspect of the present invention, a semiconductor structure is provided, which comprises: a semiconductor waveguide having a first thickness and located on a top surface of an insulator layer; a recessed semiconductor region of integral construction with the semiconductor waveguide, having a second thickness that is less than the first thickness, located on the insulator layer, and including a substantially undoped recessed semiconductor region; a p-doped semiconductor region laterally abutting the substantially undoped recessed semiconductor region; an n-doped semiconductor region laterally abutting the substantially undoped recessed semiconductor region and not abutting the p-doped semiconductor region; and a recessed metal semiconductor alloy portion abutting the recessed semiconductor region, the p-doped semiconductor region, and the n-doped semiconductor region.

According to another aspect of the present invention, a method of forming a semiconductor structure is provided, which comprises: forming shallow trench isolation structures laterally abutting a top semiconductor portion and vertically abutting a buried insulator layer in a top semiconductor layer of a semiconductor-on-insulator (SOI) substrate; forming a semiconductor waveguide by patterning the top semiconductor portion; forming a p-doped semiconductor region in the top semiconductor portion; forming an n-doped semiconductor region not abutting the p-doped semiconductor region in the top semiconductor region; and

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forming a recessed metal semiconductor alloy portion directly on a recessed region of the top semiconductor portion, wherein the recessed metal semiconductor alloy portion is formed directly on the p-doped semiconductor region and the n-doped semiconductor region.

According to yet another aspect of the present invention, a method of operating a semiconductor device is provided, which comprises: providing a semiconductor structure including: a semiconductor waveguide located on a top surface of an insulator layer; a p-doped semiconductor region thermally connected to the silicon waveguide; an n-doped semiconductor region thermally connected to the silicon waveguide and not abutting the p-doped semiconductor region; and a recessed metal semiconductor alloy portion abutting the p-doped semiconductor region and the n-doped semiconductor region; and passing current through the n-doped semiconductor region, the recessed metal semiconductor alloy portion, and the p-doped semiconductor region.

In another embodiment of the present invention, an optoelectronic device is formed on a semiconductor substrate in proximity to a temperature control device. A semiconductor waveguide that is optically coupled to the optoelectronic device may be formed to enable transmission of optical signal through the semiconductor waveguide. The temperature control device is configured to include a metal semiconductor alloy region located in proximity to the optoelectronic device, a first semiconductor region having a p-type doping, and a second semiconductor region having an n-type doping. The metal semiconductor alloy region is thermally coupled with the optoelectronic device. Electrical current may be caused to flow through the first semiconductor region, the metal semiconductor alloy region, and the second semiconductor region to allow cooling of the metal semiconductor alloy region and the optoelectronic device through heat transfer. Conversely, the current may be caused to flow in the opposite direction to allow heating of the metal semiconductor alloy region and the optoelectronic device through heat transfer. The temperature of the optoelectronic device may thus be controlled to stabilize the performance of the optoelectronic device.

According to an aspect of the present invention, a semiconductor structure including a temperature control device and an optoelectronic device is provided. The temperature control device includes: a first metal semiconductor alloy region located on a substrate; a p-

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doped semiconductor portion abutting the first metal semiconductor alloy region and located on the substrate; an n-doped semiconductor portion abutting the first metal semiconductor alloy region located on the substrate; wherein the temperature control device is configured to pass current from the p-doped semiconductor portion, through the first metal semiconductor alloy region, and to the n-doped semiconductor portion or from the n-doped semiconductor portion, through the first metal semiconductor alloy region, and to the p-doped semiconductor portion. The optoelectronic device includes a device that comprises a semiconductor material, configured to manipulate electromagnetic radiation, and is thermally coupled to the temperature control device.

According to another aspect of the present invention, a method of forming a semiconductor structure including a temperature control device and an optoelectronic device is provided. The method includes: patterning a top semiconductor layer of a semiconductor-on-insulator substrate to form a p-doped semiconductor portion and an n-doped semiconductor portion; forming a first metal semiconductor alloy region directly on the p-doped semiconductor portion and the n-doped semiconductor portion, wherein the p-doped semiconductor portion and an n-doped semiconductor portion and the first metal semiconductor alloy region constitute a portion of a temperature control device; forming a current conduction path configured to pass current from the p-doped semiconductor portion, through the first metal semiconductor alloy region, and to the n-doped semiconductor portion or from the n-doped semiconductor portion, through the first metal semiconductor alloy region, and to the p-doped semiconductor portion; and forming an optoelectronic device comprising a semiconductor material, configured to manipulate electromagnetic radiation, and is thermally coupled to the temperature control device.

According to yet another aspect of the present invention, a method of operating a semiconductor structure comprising a temperature control device and an optoelectronic device is provided. The method includes: providing a temperature control device including a first metal semiconductor alloy region located on a substrate, a p-doped semiconductor portion abutting the first metal semiconductor alloy region and located on the substrate, and an n-doped semiconductor portion abutting the first metal semiconductor alloy region located on the substrate; providing an optoelectronic device including a device that

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comprises a semiconductor material, configured to manipulate electromagnetic radiation, and is thermally coupled to the temperature control device; and passing electrical current from the p-doped semiconductor portion, through the first metal semiconductor alloy region, and to the n-doped semiconductor portion or from the n-doped semiconductor portion, through the first metal semiconductor alloy region, and to the p-doped semiconductor portion, wherein heat is transferred in the direction of flow of majority charge carriers in the p-doped semiconductor portion and the n-doped semiconductor portion.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Embodiments of the present invention will now be described, by way of example only, with reference to the accompanying drawings in which:

FIGS. 1A – 1C are various views of a first exemplary semiconductor structure corresponding to the step after formation of a shallow trench isolation structures 34;

FIGS. 2A – 2C are various views of the first exemplary semiconductor structure corresponding to the step after formation of a pair of recessed line trenches 31;

FIGS. 3A – 3C are various views of the first exemplary semiconductor structure corresponding to the step after removal of a first photoresist (37A, 37B, 37C);

FIGS. 4A – 4C are various views of the first exemplary semiconductor structure corresponding to the step after formation of p-doped semiconductor regions (46A, 46B);

FIGS. 5A – 5C are various views of the first exemplary semiconductor structure corresponding to the step after formation of n-doped semiconductor regions (48A, 48B);

FIGS. 6A – 6C are various views of the first exemplary semiconductor structure corresponding to the step after removal of a third photoresist 47;

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FIGS. 7A – 7C are various views of the first exemplary semiconductor structure corresponding to the step after formation of a dielectric material layer 60L;

FIGS. 8A – 8C are various views of the first exemplary semiconductor structure corresponding to the step after formation of a dielectric material portion 62 and dielectric spacers 64;

FIGS. 9A – 9C are various views of the first exemplary semiconductor structure corresponding to the step after formation of various metal semiconductor alloy portions, a middle-of-line (MOL) dielectric layer 80, and various conductive contact vias;

FIGS. 10, 11, and 12A, 12B, 13A, 13B, 14A, 14B, 15A, 15B, 16A, and 16B are various views of a second exemplary semiconductor structure corresponding to a second embodiment of the present invention. FIGS. 10 and 11 are vertical cross-sectional views. Each of FIG. 12A, 13A, 13A, 14A, 15A, and 16A is a vertical cross-sectional view along a vertical plane labeled Z – Z' in figures with the numeric label and the suffix "B." FIGS. 11B, 12B, 13B, and 14B are top-down views. FIG. 15B is a top-down view of selected elements to demonstrate lateral geometrical relationship between the selected elements;

FIG. 17 is a vertical cross-sectional view of a third exemplary semiconductor structure;

FIG. 18 is a vertical cross-sectional view of a fourth exemplary semiconductor structure;

FIG. 19 is a vertical cross-sectional view of a fifth exemplary semiconductor structure;

FIGS. 20 and 21 are sequential vertical cross-sectional views of a sixth exemplary semiconductor structure; and

FIG. 22 is a top-down view of selected elements to demonstrate lateral geometrical relationship between the selected elements of a seventh exemplary semiconductor structure according to a seventh embodiment of the present invention.

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For all of the figures herein, the following conventions apply. Figures with the same numeric label correspond to the same stage of manufacturing for an exemplary semiconductor structure. Within FIGS. 1A – 9C, figures with the suffix "A" are top-down views, and figures with the suffix "B" or "C" are horizontal cross-sectional views along the plane B – B' or the plane C – C', respectively, in the figure with the same numeric label and the suffix "A."

DETAILED DESCRIPTION

As stated above, the present invention relates to a temperature control device for an optoelectronic device and a germanium photodetector for silicon waveguide, and methods of manufacturing the same, and methods of operating the same, which are now described in detail with accompanying figures. Throughout the drawings, the same reference numerals or letters are used to designate like or equivalent elements. Detailed descriptions of known functions and constructions unnecessarily obscuring the subject matter of the present invention have been omitted for clarity. The drawings are not necessarily drawn to scale.

Referring to FIGS. 1A – 1F, an exemplary semiconductor structure according to the present invention comprises a semiconductor substrate, which is a semiconductor-on-insulator (SOI) substrate. The semiconductor substrate includes an insulator layer 20 and a top semiconductor layer located above the insulator layer 20. The semiconductor substrate may further include a handle substrate 10, which is attached to the bottom surface of the insulator layer 20. The handle substrate 10 may comprise a semiconductor material, an insulator material, a conductive material, or a combination thereof. The insulator layer 20 and the handle substrate 10, if present, provide structural support to the top semiconductor layer which may comprise a contiguous semiconductor material layer that covers the entirety of the insulator layer 20.

The contiguous semiconductor material layer comprises a semiconductor material. Exemplary semiconductor materials that may be employed for the contiguous semiconductor material layer include, but are not limited to, silicon, germanium, silicon-germanium alloy, silicon carbon alloy, silicon-germanium-carbon alloy, gallium arsenide, indium arsenide, indium phosphide, III-V compound semiconductor materials, II-VI compound

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semiconductor materials, organic semiconductor materials, and other compound semiconductor materials. Preferably, the entirety of the contiguous semiconductor material layer comprises a single crystalline semiconductor material having an epitaxial alignment among the semiconductor atoms. For example, the semiconductor material of the contiguous semiconductor material layer may comprise single crystalline silicon or single crystalline germanium. The thickness of the contiguous semiconductor material layer, which is herein referred to as a first thickness *t1*, may be from about 50 nm to about 1,000 nm, and typically from about 200 nm to about 500 nm, although lesser and greater thicknesses can also be employed.

Preferably, the contiguous semiconductor material layer comprises a substantially undoped semiconductor material so that the amount of impurities, including dopant atoms, in the contiguous semiconductor material layer is minimized. By minimizing the amount of impurities in the contiguous material layer, a semiconductor waveguide to be subsequently formed from a portion of the contiguous material layer provides low absorption rate of the signal. The atomic concentration of impurities, including dopants, in the contiguous semiconductor material layer is less than about $1.0 \times 10^{16}/cm^3$, and preferably less than about $1.0 \times 10^{15}/cm^3$, and more preferably less than about $1.0 \times 10^{14}/cm^3$. In case the contiguous semiconductor material layer comprises silicon, the resistivity of the material of the contiguous semiconductor material layer is greater than about 1 Ohm-cm, and preferably greater than about 10 Ohm-cm, and more preferably greater than about 100 Ohm-cm.

Trenches extending to the top surface of the insulator layer 20 are formed within the contiguous semiconductor material layer by a combination of lithographic means and an etch. Specifically, a photoresist (not shown) is applied over the top surface of the contiguous semiconductor material layer and lithographically patterned. The pattern in the photoresist is transferred into the contiguous semiconductor material layer by the etch, which is typically an anisotropic etch. After removal of the photoresist, the trenches are filled with a dielectric material such as a dielectric oxide, a dielectric nitride, a dielectric nitride, or a combination thereof. For example, silicon oxide and/or silicon nitride may be deposited into the trenches. The dielectric material above the top surface of the contiguous semiconductor material layer is removed, for example, by chemical mechanical planarization. The remaining portions of

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the dielectric material filling the trenches constitute shallow trench isolation (STI) structures 34. Pad dielectric layers (not shown) may be employed to facilitate the planarization process.

The remaining portion of the contiguous semiconductor material layer constitutes a top semiconductor portion, which includes a primary top semiconductor portion 30P, first laterally protruding top semiconductor portions 30A, and second laterally protruding top semiconductor portions 30B. The primary top semiconductor portion 30P, the first laterally protruding top semiconductor portions 30A, and the second laterally protruding top semiconductor portions 30B comprise the same semiconductor material, have the same thickness, i.e., the first thickness *t1*, and are epitaxially aligned among one another. The sidewalls of the top semiconductor portion (30P, 30A, 30B) are laterally abutted by the shallow trench isolation structures 34. The first laterally protruding top semiconductor portions 30A and the second laterally protruding top semiconductor portions 30B laterally protrude out of the sidewalls of the primary top semiconductor portion 30P into the shallow trench isolation structures 34. Thus, each of the first laterally protruding top semiconductor portions 30A and the second laterally protruding top semiconductor portions 30B may comprise multiple sidewalls that laterally abut the shallow trench isolation structures 34. The shallow trench isolation structures 34 and the top semiconductor portion (30P, 30A, 30B) have substantially the same thickness, i.e., the first thickness *t1*.

At least one pair of a first laterally protruding top semiconductor portions 30A and a second laterally protruding top semiconductor portions 30B may be formed on one side of the primary top semiconductor portion 30P, and at least another pair of a first laterally protruding top semiconductor portions 30A and a second laterally protruding top semiconductor portions 30B may be formed on an opposite side of the primary top semiconductor portion 30P. The width of the semiconductor portion *SPW* may be from about 400 nm to about 3,000 nm, and preferably from about 600 nm to about 1,500 nm, although lesser and greater widths can also be employed. The length of the semiconductor portion *SPL* is the length of a semiconductor waveguide that is intended to be manufactured, and may be from about 10 μm to about 3 cm, and typically from about 30 μm to about 1 cm, although lesser and greater lengths can also be employed. Further, configurations for a

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semiconductor waveguide having a curvature or a taper can also be employed, in which the shape of the top semiconductor portion (30P, 30A, 30B) are adjusted with a curvature, a taper, and/or other suitable geometric adjustments.

Referring to FIGS. 2A – 2C, a first photoresist is applied over the top surfaces of the top semiconductor portion (30P, 30A, 30B) and the shallow trench isolation structures 34 and lithographically patterned. The pattern in the first photoresist includes a pair of line troughs separated by a central photoresist portion 37A, which is a remaining portion of the first photoresist after lithographic patterning. The central photoresist portion 37A has a constant width, which is herein referred to as a waveguide width *ww*. The waveguide width *ww* may be from about 200 nm to about 1,500 nm, and preferably from about 300 nm to about 750 nm, although lesser and greater widths can also be employed. The remaining portions of the first photoresist include a first-side photoresist portion 37B and a second-side photoresist portion 37C, which are separated from the central photoresist portion 37A by the pair of line troughs. Each of the line troughs may have a substantially constant width, which is herein referred to as a line trough width *ltw*. The two line troughs may have the same line trough width *ltw*, or may have different line trough widths *ltw*. The sum of the two line trough widths *ltw* and the waveguide width *ww* may be less than, equal to, or greater than the width of the semiconductor portion *SPW*. While the present invention is described for the case in which the sum of the two line trough widths *ltw* and the waveguide width *ww* is less than the width of the semiconductor portion *SPW*, embodiments in which the sum of the two line trough widths *ltw* and the waveguide width *ww* is equal to, or greater than, the width of the semiconductor portion *SPW* are explicitly contemplated herein.

The pattern in the patterned portions of the first photoresist, i.e., the set of the central photoresist portion 37A, the first-side photoresist portion 37B, and the second-side photoresist portion 37C is transferred into the primary top semiconductor portion 30P, for example, by an anisotropic etch such as a reactive ion etch (RIE). The exposed portions of the primary top semiconductor portion 30P are vertically recessed by a recess depth *rd*, which is less than the first thickness *t1*. A pair of recessed line trenches 31 is formed directly underneath the two line troughs between the central photoresist portion 37A and each of the first-side and second-side photoresist portions (37B, 37C).

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The recessed portions of the primary top semiconductor portion 30P are herein referred to as recessed semiconductor regions 30R. The recessed semiconductor regions have a second thickness *t2*, which is equal to the difference between the first thickness *t1* and the recess depth *rd*. The second thickness *t2* may be from about 10 nm to about 200 nm, and typically from about 30 nm to about 100 nm, although lesser and greater thicknesses can also be employed. The remaining sub-portion of the primary top semiconductor portion 30P underneath the central photoresist portion 37A is herein referred to a semiconductor waveguide 30. The semiconductor waveguide 30 has the first thickness *t1* and the waveguide width *ww*. The semiconductor waveguide 30 may be employed to transmit light along the direction of the length of the semiconductor portion *SPL* (See FIG. 1A). The sub-portions of the top semiconductor portion 30P directly underneath the pair of line trenches 31 are the recessed semiconductor regions 30R, which are of integral construction with the semiconductor waveguide 30.

The first-side photoresist portion 37B and the second-side photoresist portion 37C cover the upper surfaces of the first laterally protruding top semiconductor portions 30A and the second laterally protruding top semiconductor portions 30B. Thus, the first-side photoresist portion 37B and the second-side photoresist portion 37C are not recessed by the anisotropic etch, and have the first thickness *t1*. Each of the first laterally protruding top semiconductor portions 30A and the second laterally protruding top semiconductor portions 30B is a sub-portion of the top semiconductor portion (30P, 30A, 30b) having the first thickness *t1*. Sidewalls of the first laterally protruding top semiconductor portions 30A and the second laterally protruding top semiconductor portions 30B are exposed to the pair of recessed line trenches 31.

The semiconductor waveguide 30, the recessed semiconductor regions 30R, the first-side photoresist portions 37B, and the second-side photoresist portions 37C are of integral and unitary construction, i.e., in a single contiguous structure without any interface therebetween. In case the entirety of the top semiconductor portion (30P, 30A, 30B) is single crystalline prior to the formation of the semiconductor waveguide 30, the semiconductor waveguide 30, the recessed semiconductor regions 30R, the first-side photoresist portions 37B, and the second-side photoresist portions 37C are single crystalline

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and epitaxially aligned among one another. In case the semiconductor substrate is an SOI substrate, the semiconductor waveguide 30, the semiconductor waveguide 30, the recessed semiconductor regions 30R, the first-side photoresist portion 37B, the second-side photoresist portion 37C, and the shallow trench isolation structures 34 are formed in a top semiconductor layer of the SOI substrate.

Referring to FIGS. 3A – 3C, the first photoresist is removed selective to the semiconductor material of the semiconductor waveguide 30, the recessed semiconductor regions 30R, the first-side photoresist portion 37B, the second-side photoresist portion 37C. Preferably, the removal of the first photoresist is selective to the dielectric material of the shallow trench isolation structures 34. While the present invention is described for the case in which edges of the recessed line trenches 31 is coincident with the sidewalls of the shallow trench isolation structures 34 that laterally abut the primary top semiconductor portion 30P (See FIG. 1A), embodiments in which the edges of the recessed line trenches 31 is offset from the sidewalls of the shallow trench isolation structures 34 inward or outward are explicitly contemplated herein.

Referring to FIGS. 4A – 4C, a second photoresist 45 is applied over the first exemplary semiconductor structure and lithographically patterned to form openings. The first laterally protruding top semiconductor portions 30A are exposed within the openings. Further, portions of the recessed semiconductor regions 30R that adjoin the first laterally protruding top semiconductor portions 30A are also exposed within the opening in the second photoresist 45. The second photoresist 45 covers the entirety of the semiconductor waveguide 30 and the second laterally protruding top semiconductor portions 30B. Further, the second photoresist 45 covers portions of the recessed semiconductor regions 30R that laterally abut the semiconductor waveguide 30.

P-type dopants are implanted into the first laterally protruding top semiconductor portions 30A and the exposed portions of the recessed semiconductor regions 30R. P-type dopants may be boron, gallium, indium, or a combination thereof. Preferably, the dose and the energy of the p-type dopants are selected to provide a heavy doping in the implanted regions. For example, the atomic concentration of p-type dopants in the implanted regions may be

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from about 1.0 x 10^{19}/cm^3 to about 1.0 x 10^{21}/cm^3, and typically from about 5.0 x 10^{19}/cm^3 to about 5.0 x 10^{20}/cm^3, although lesser and greater dopant concentrations can also be employed.

The first laterally protruding top semiconductor portions 30A as implanted with the p-type dopants are herein referred to as p-doped non-recessed semiconductor regions 46A, which has a third thickness *t3*. Typically, the third thickness *t3* is the same as the first thickness *t1*. The portions of the recessed semiconductor regions 30R that are implanted with the p-type dopants are herein referred to as p-doped recessed semiconductor regions 46B. A contiguous pair of a p-doped non-recessed semiconductor region 46A and a p-doped recessed semiconductor region 46B collectively constitutes a p-doped semiconductor region (46A, 46B). The portions of the recessed semiconductor regions 30R that are not implanted with the p-type dopants are herein referred to as substantially undoped recessed semiconductor regions 32, which has the same composition as the semiconductor waveguide 30, i.e., has a total concentration of impurities, including dopants, less than about 1.0 x 10^{16}/cm^3.

Within each p-doped semiconductor region (46A, 46B), a p-doped non-recessed semiconductor region 46A laterally abuts a p-doped recessed semiconductor region 46B. Further, each p-doped recessed semiconductor region 46B laterally abuts a substantially undoped recessed semiconductor region 32. The second photoresist 45 is subsequently removed.

Referring to FIGS. 5A – 5C, a third photoresist 47 is applied over the first exemplary semiconductor structure and lithographically patterned to form openings. The second laterally protruding top semiconductor portions 30B are exposed within the openings. Further, portions of the substantially undoped recessed semiconductor regions 32 that adjoin the second laterally protruding top semiconductor portions 30B are also exposed within the opening in the third photoresist 47. The third photoresist 47 covers the entirety of the semiconductor waveguide 30 and the p-doped semiconductor region (46A, 46B). Further, the third photoresist 47 covers portions of the substantially undoped recessed semiconductor regions 32 that laterally abut the semiconductor waveguide 30.

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N-type dopants are implanted into the second laterally protruding top semiconductor portions 30B and the exposed portions of the substantially undoped recessed semiconductor regions 32. N-type dopants may be phosphorus, arsenic, antimony, or a combination thereof. Preferably, the dose and the energy of the n-type dopants are selected to provide a heavy doping in the implanted regions. For example, the atomic concentration of n-type dopants in the implanted regions may be from about $1.0 \times 10^{19}/cm^3$ to about $1.0 \times 10^{21}/cm^3$, and typically from about $5.0 \times 10^{19}/cm^3$ to about $5.0 \times 10^{20}/cm^3$, although lesser and greater dopant concentrations can also be employed.

The second laterally protruding top semiconductor portions 30B as implanted with the n-type dopants are herein referred to as n-doped non-recessed semiconductor regions 48A, which has the third thickness *t3*. The portions of the substantially undoped recessed semiconductor regions 32 that are implanted with the n-type dopants are herein referred to as n-doped recessed semiconductor regions 48B. A contiguous pair of an n-doped non-recessed semiconductor region 48A and an n-doped recessed semiconductor region 48B collectively constitutes an n-doped semiconductor region (48A, 48B). The substantially undoped recessed semiconductor regions 32 is reduced as portions of the substantially undoped recessed semiconductor regions 32 are converted into the n-doped recessed semiconductor regions 48B.

Within each n-doped semiconductor region (48A, 48B), an n-doped non-recessed semiconductor region 48A laterally abuts an n-doped recessed semiconductor region 48B. Further, each n-doped recessed semiconductor region 48B laterally abuts a substantially undoped recessed semiconductor region 32. The third photoresist 47 is subsequently removed.

Referring to FIGS. 6A – 6C, the first exemplary semiconductor structure after removal of the third photoresist 47 is shown. The substantially undoped recessed semiconductor regions 32, the p-doped recessed semiconductor regions 46B, and the n-doped recessed semiconductor regions 48B collectively constitute the recessed semiconductor regions (32, 46B, 48B). The recessed semiconductor regions (32, 46B, 48B) underlie the pair of recessed line trenches 31. The p-doped non-recessed semiconductor regions 48A, the n-doped non-

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recessed semiconductor regions 48A, and the semiconductor waveguide 30 are not recessed. Each of the p-doped non-recessed semiconductor regions 48A and the n-doped non-recessed semiconductor regions 48A has a sidewall that is exposed to one of the recessed line trenches 31. The semiconductor waveguide 30 has two substantially parallel and substantially vertical sidewalls separated by the waveguide width *ww*. Each sidewall of the semiconductor waveguide 30 is exposed to one of the two recessed line trenches 31.

Referring to FIGS. 7A – 7C, a dielectric layer 60L is formed directly on the exposed surfaces of the first exemplary semiconductor structure including the top surface and the sidewall surfaces of the semiconductor waveguide 30, the top surfaces of the recessed semiconductor regions (32, 46B, 48B), the top surfaces and the sidewalls of the p-doped non-recessed semiconductor region 46A and the n-doped non-recessed semiconductor region 48A, and the top surfaces of the shallow trench isolation structures 34. The dielectric layer 60L comprises a dielectric material such as a dielectric oxide, a dielectric nitride, a dielectric oxynitride, or a combination thereof. For example, the dielectric layer 60L may comprise silicon nitride or silicon oxide. The dielectric material for the dielectric layer 60L has a lower refractive index than the semiconductor material of the semiconductor waveguide 30.

The dielectric layer 60L may be conformal or non-conformal. The thickness of the dielectric layer 60L, as measured on the top surface of the semiconductor waveguide 30, may be from about 4 nm to about 100 nm, and typically from about 10 nm to about 50 nm, although lesser and greater thicknesses can also be employed. The dielectric layer 60L may be formed by low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), rapid thermal chemical vapor deposition (RTCVD), atomic layer deposition (ALD), etc.

Referring to FIGS. 8A – 8C, the dielectric layer 60L is lithographically patterned into at least three portions. The lithographic patterning may be effected by applying a photoresist (not shown) to the top surface of the dielectric layer 60L and lithographically patterning the photoresist, followed by a pattern transfer into the dielectric layer by an etch. The etch may be an anisotropic etch or an isotropic etch.

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Remaining portions of the dielectric layer 60L after the lithographic patterning include a dielectric material portion 62 which covers the entirety of the top surface and sidewalls of the semiconductor waveguide 30. The remaining portions of the dielectric layer 60L further includes dielectric spacers 64, each of which is located directly on at least one of a sidewall of a p-doped non-recessed semiconductor region 46A and a sidewall of an n-doped non-recessed semiconductor region 48A. In one embodiment, a dielectric spacer 64 may be formed contiguously and directly on a sidewall of a p-doped non-recessed semiconductor region 46A, a sidewall of an n-doped non-recessed semiconductor region 48A, and a sidewall of one of the shallow trench isolation structures 34 that is located between the p-doped non-recessed semiconductor region 46A and the sidewall of an n-doped non-recessed semiconductor region 48A. Horizontal surfaces of the p-doped non-recessed semiconductor regions 46A, the n-doped non-recessed semiconductor regions 48A, the p-doped recessed semiconductor regions 46B, and the n-doped recessed semiconductor regions 48B are exposed. All sidewalls of the p-doped non-recessed semiconductor regions 46A and the n-doped non-recessed semiconductor regions 48A are covered by the dielectric spacers 64.

On each side of the semiconductor waveguide 30, a contiguous set of exposed semiconductor surfaces is formed, which includes a top surface of a p-doped recessed semiconductor regions 46B, a top surface of an n-doped recessed semiconductor regions 48B, and a top surface of a portion of a substantially undoped recessed semiconductor regions 32 located therebetween.

Referring to FIGS. 9A – 9C, various metal semiconductor alloy portions are formed on the exposed semiconductor surfaces of the first exemplary semiconductor structure. Specifically, recessed metal semiconductor alloy portions 72 are formed directly on the exposed surfaces of the recessed semiconductor regions (32, 46B, 48B). First metal semiconductor alloy portions 66 are formed directly on the top surfaces of the p-doped non-recessed semiconductor regions 46A. Second metal semiconductor alloy portions 68 are formed directly on the top surfaces of the n-doped non-recessed semiconductor regions 46B.

The various metal semiconductor alloy portions (72, 66, 68) may be formed by methods known in the art such as deposition of a blanket metal layer, anneal at an elevated

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temperature to induce formation of metal semiconductor alloy materials, and removal of unreacted portions of the blanket metal layer. In case the semiconductor material of the recessed semiconductor regions (32, 46B, 48B) and the doped non-recessed semiconductor regions (46A, 48A) comprise silicon, the various metal semiconductor alloy portions (72, 66, 68) comprise a metal silicide. In case the semiconductor material of the recessed semiconductor regions (32, 46B, 48B) and the doped non-recessed semiconductor regions (46A, 48A) comprise germanium, the various metal semiconductor alloy portions (72, 66, 68) comprise a metal germanide. The recessed metal semiconductor alloy portions 72, the first metal semiconductor alloy portions 66, and the second metal semiconductor alloy portions 68 comprise the same metal semiconductor alloy material.

A middle-of-line (MOL) dielectric material layer 80 is formed on the first exemplary semiconductor structure. The pair of line troughs 31 is filled with the MOL dielectric layer 80. The dielectric materials that may be used for the MOL dielectric layer 80 include, but are not limited to, a silicate glass, an organosilicate glass (OSG) material, a SiCOH-based low-k material formed by chemical vapor deposition, a spin-on glass (SOG), or a spin-on low-k dielectric material such as SiLK™, etc. The silicate glass includes an undoped silicate glass (USG), borosilicate glass (BSG), phosphosilicate glass (PSG), fluorosilicate glass (FSG), borophosphosilicate glass (BPSG), etc. The dielectric material may be a low dielectric constant (low-k) material having a dielectric constant less than 3.0. The dielectric material may non-porous or porous.

A conductive contact via is formed directly on each of the first metal semiconductor alloy portions 66 and the second metal semiconductor alloy portions 68. Specifically, a first conductive contact via 86 is formed directly on each of the first metal semiconductor alloy portion 66, and a second conductive contact via 88 is formed directly on each of the second metal semiconductor alloy portion 68. The first and second metal semiconductor alloy portions (66, 68) comprise a conductive material such as doped polysilicon, a doped silicon-containing semiconductor material, W, Cu, Al, TaN, TiN, Ta, Ti, or a combination thereof.

Heat may be transferred between the semiconductor waveguide 30 and the set of the first metal semiconductor alloy portions 66 and the second metal semiconductor alloy portions 68

by passing current. Specifically, a voltage bias may be applied across a resistively connected pair of a first conducive contact via 86 and a second conductive contact via 88.

In one embodiment, the second conductive contact via 88 is held at a positive voltage relative to the first conductive contact via 86. In this case, electrical current flows from the second conductive contact via 88, then through a second metal semiconductor alloy portion 68, then through an n-doped non-recessed semiconductor region 48A, then through an n-doped recessed semiconductor region 48B, then through a recessed metal semiconductor alloy portion 72, then through a p-doped recessed semiconductor region 46B, then through a p-doped non-recessed semiconductor region 46A, then through a first metal semiconductor alloy portion 66, and into the first conductive contact via 86. In metallic materials or metal semiconductor alloy portions in the current path, electrons move in the opposite direction of the current flow to conduct electricity.

In semiconductor material portions, majority charge carriers provide electrical conduction. Specifically, holes having positive charges travel in the p-doped recessed semiconductor region 46B and the p-doped non-recessed semiconductor region 46A along the direction from the recessed metal semiconductor alloy portion 72 toward the first metal semiconductor alloy portion 66. Electrons having negative charges travel in the n-doped recessed semiconductor region 48B and the n-doped non-recessed semiconductor region 48A along the direction from the recessed metal semiconductor alloy portion 72 toward the second metal semiconductor alloy portion 68. Thus, the majority charge carriers travel away from the recessed metal semiconductor alloy portion 72 in the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B).

The mechanism of Peltier-Seebeck effect is in operation in the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B). According to Peltier-Seebeck effect, heat transfer accompanies diffusion of charge carriers in a semiconductor material and vice versa. In this case, the majority charge carriers diffuse away from the interface with the recessed metal semiconductor alloy portion 72 toward the interface with the first or second metal semiconductor alloy portion (66 or 68) in each of the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B).

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Therefore, there is a net heat transfer from the recessed metal semiconductor alloy portion 72 to the first and second metal semiconductor alloy portions (66, 68). The heat that is transferred to the first and second metal semiconductor alloy portions (66, 68) may further be transferred to a heat sink through the first and second conductive contact vias (86, 88) and other metal interconnect structures (not shown) attached thereto.

Since the semiconductor waveguide 30, the recessed semiconductor regions (32, 46B, 48B), the p-doped semiconductor region (46A, 46B), and the n-doped semiconductor region (48A, 48B) are of integral construction without any interface therebetween, the entirety of the semiconductor waveguide 30, the recessed semiconductor regions (32, 46B, 48B), the p-doped semiconductor region (46A, 46B), and the n-doped semiconductor region (48A, 48B) is thermally connected among one another. Continual transfer of heat from the recessed metal semiconductor alloy portions 72, through the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B), and into the first and second metal semiconductor alloy portions (66, 68) cools the semiconductor waveguide 30.

Cooling of the semiconductor waveguide 30 affects the refractive index of the semiconductor material of the semiconductor waveguide. For example, single crystalline silicon has a wavelength-dependent refractive index, which is from about 3.42 to about 3. 56 between the wavelength range from about 1 micron to about 6 microns. The temperature dependency of the refractive index of silicon is about 1.6×10^{-4} per degree Celsius. Germanium has similar temperature dependency as silicon.

Temperature change in the semiconductor waveguide 30 may be advantageously employed to change the phase of light passing through the semiconductor waveguide. For example, light having a wavelength of about 3.42 micron in vacuum has a wavelength of about 1.00 micron in a semiconductor waveguide 30 that consists essentially of silicon. 1 degree change in the temperature of the semiconductor waveguide 30 induces a phase change of about $2\pi \times 1.6 \times 10^{-4}$ radian per 1 micron. The light changes phase by π radian after traveling about 3.125 mm. By employing a beam splitter connected to two semiconductor waveguides 30 and modulating the phase of the light in one of the semiconductor waveguides 30, constructive interference or destructive interference may be induced between

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the two beams as the phase of one beam is modulated through cooling. Thus, by modulating the refractive index of a semiconductor waveguide 30 through the temperature change in the semiconductor waveguide 30 caused by heat transfer out of the semiconductor waveguide 30, the phase of the light passing through the semiconductor waveguide 30 may be modulated.

In another embodiment, the second conductive contact via 88 is held at a negative voltage relative to the first conductive contact via 86. In this case, electrical current flows from the first conductive contact via 86, then through a first metal semiconductor alloy portion 66, then through a p-doped non-recessed semiconductor region 46A, then through a p-doped recessed semiconductor region 46B, then through a recessed metal semiconductor alloy portion 72, then through an n-doped recessed semiconductor region 48B, then through an n-doped non-recessed semiconductor region 48A, then through a second metal semiconductor alloy portion 68, and into the second conductive contact via 88. In other words, the electrical current flows in the opposite direction of the current flow in the previous embodiment.

In this case, holes in the p-doped semiconductor region (46A, 46B) along the direction from the first metal semiconductor alloy portion 66 to the recessed metal semiconductor alloy portion 72. Electrons travel in the n-doped semiconductor region (48A, 48B) along the direction from the second metal semiconductor alloy portion 68 toward the recessed metal semiconductor alloy portion 72. Thus, the majority charge carriers travel toward the recessed metal semiconductor alloy portion 72 in the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B).

The mechanism of Peltier-Seebeck effect is also in operation in the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B). However, the majority charge carriers diffuse away from the interface with the first or second metal semiconductor alloy portion (66 or 68) toward the interface with the recessed metal semiconductor alloy portion 72 in each of the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B). Therefore, there is a net heat transfer from

the first and second metal semiconductor alloy portions (66, 68) to the recessed metal semiconductor alloy portion 72.

Since the entirety of the semiconductor waveguide 30, the recessed semiconductor regions (32, 46B, 48B), the p-doped semiconductor region (46A, 46B), and the n-doped semiconductor region (48A, 48B) is thermally connected among one another, heat transferred into the recessed metal semiconductor alloy portion 72 is transferred into the semiconductor waveguide 30. Thus, the semiconductor waveguide is heated as the current flows through the p-doped semiconductor region (46A, 46B) and the n-doped semiconductor region (48A, 48B). The mechanism for the heat accumulation in the semiconductor waveguide 30 is not Joule heating, but a heat transfer through Peltier-Seebeck effect.

Heating of the semiconductor waveguide 30 affects the refractive index of the semiconductor material of the semiconductor waveguide in the same manner as the cooling of the semiconductor waveguide 30 except for the reversal of the polarity of the change in the refractive index. In a similar manner as in the previous embodiment, temperature change in the semiconductor waveguide 30 may be advantageously employed to change the phase of light passing through the semiconductor waveguide. By modulating the refractive index of a semiconductor waveguide 30 through the temperature change in the semiconductor waveguide 30 caused by heat transfer into the semiconductor waveguide 30, the phase of the light passing through the semiconductor waveguide 30 may be modulated.

Referring to FIG. 10, a second exemplary semiconductor structure according to a second embodiment of the present invention comprises a semiconductor substrate 108, which is a semiconductor-on-insulator (SOI) substrate. The SOI substrate includes a handle substrate 10, an insulator layer 20 abutting a top surface of the handle substrate 10, and a top semiconductor layer 129 located above the insulator layer 20. The insulator layer 20 and the handle substrate 10 provide structural support to the top semiconductor layer 129 which may comprise a contiguous semiconductor material layer that covers the entirety of the insulator layer 20. The top semiconductor layer 129 comprises a semiconductor material, which may be any of the material that may be employed for the contiguous semiconductor material layer of the first embodiment.

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Preferably, the top semiconductor layer 129 comprises a substantially undoped semiconductor material so that the amount of impurities, including dopant atoms, in the top semiconductor layer 129 is minimized. By minimizing the amount of impurities in the contiguous material layer, a semiconductor waveguide having a low absorption rate of the signal may be subsequently formed from a portion of the top semiconductor layer. The atomic concentration of impurities, including dopants, in the top semiconductor layer 129 is less than about $1.0 \times 10^{16}/cm^3$, and preferably less than about $1.0 \times 10^{15}/cm^3$, and more preferably less than about $1.0 \times 10^{14}/cm^3$. In case the top semiconductor layer 129 comprises silicon, the resistivity of the material of the top semiconductor layer 129 is greater than about 1 Ohm-cm, and preferably greater than about 10 Ohm-cm, and more preferably greater than about 100 Ohm-cm.

The buried insulator layer 20 comprises a dielectric material such as a dielectric oxide, a dielectric nitride, or a dielectric oxynitride. For example, the buried insulator layer 20 may comprise silicon oxide. The buried insulator layer 20 may comprise a dielectric material having a dielectric constant greater than 3.0.

The handle substrate 10 may comprise a semiconductor material, an insulator material, a conductive material, or a combination thereof. In case the handle substrate 10 comprises a semiconductor material, the material for the handle substrate 10 may comprise any of the semiconductor material that may be employed for the top semiconductor layer 129 as described above.

Referring to FIG. 11, a hard mask layer 125 may be deposited on a top surface of the top semiconductor layer 129 and lithographically patterned to mask a portion of the top semiconductor layer 129, while exposing other portions of the top semiconductor layer 129. The hard mask layer 125 comprises a dielectric material such as silicon oxide, silicon nitride, or silicon oxynitride. The exposed portions of the top semiconductor layer 129 are recessed. An epitaxial semiconductor layer 127 may be deposited on the recessed surface of the top semiconductor layer 129. The epitaxial semiconductor layer may comprise a different semiconductor material than the top semiconductor layer 129. The material of the epitaxial

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semiconductor layer 127 is single crystalline, and is epitaxially aligned to semiconductor material of the top semiconductor layer 127. For example, the top semiconductor layer 129 may comprise single crystalline silicon, and the epitaxial semiconductor layer 127 may comprise a silicon germanium alloy.

The hard mask layer 125 is subsequently removed. The top surface of the top semiconductor portions of the top semiconductor layer 129 may be planarized, for example, by chemical mechanical planarization.

Referring to FIGS. 12A and 12B, portions of the top semiconductor layer 129 are appropriately doped and patterned to form at least one p-doped semiconductor portion (131, 132) and at least one n-doped semiconductor portion (133, 134). Each of the at least one p-doped semiconductor region (131, 132) may comprise a lower p-doped semiconductor region 131 and an upper p-doped semiconductor region 132. Each of the at least one n-doped semiconductor region (133, 134) may comprise a lower n-doped semiconductor region 133 and an upper n-doped semiconductor region 134. In addition, a semiconductor waveguide 136 may be formed by a patterning another portion of the top semiconductor layer 129 without implanting additional dopant atoms. In this case, the semiconductor waveguide may comprise a substantially intrinsic semiconductor material having the same composition as the at least one p-doped semiconductor portion (131, 132) and the at least one n-doped semiconductor portion (133, 134) except for dopant species and dopant concentration. The substantially intrinsic semiconductor material may have a resistivity greater than 1 Ohm-cm as the material of the top semiconductor layer 129 described above. In one case, the semiconductor waveguide 136 may consist essentially of silicon, and the at least one lower p-doped semiconductor region 131 may consist essentially of p-doped silicon, and the at least one n-doped semiconductor region 133 may consist essentially of n-doped silicon.

The at least one upper p-doped semiconductor portion 132 may be formed by implanting p-type dopants into at least one portion of the epitaxial semiconductor layer 127 through at least one opening in a first implantation mask layer (not shown), which may be a first patterned photoresist layer. The at least one lower p-doped semiconductor portion 131 may

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be formed by implanting p-type dopants into at least one portion of the top semiconductor layer 129 through the at least one opening in the first implantation mask layer. The at least one upper n-doped semiconductor portion 134 may be formed by implanting n-type dopants into at least one portion of the epitaxial semiconductor layer 127 through at least one opening in a second implantation mask layer (not shown), which may be a second patterned photoresist layer. The at least one lower n-doped semiconductor portion 133 may be formed by implanting n-type dopants into at least one portion of the top semiconductor layer 129 through the at least one opening in the second implantation mask layer.

After implantation of the p-type dopants and the n-type dopants, the top semiconductor layer 129 is lithographically patterned. The remaining portions of the epitaxial semiconductor layer 127 and the top semiconductor layer 129 after lithographic patterning include the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and optionally, the semiconductor waveguide 136. Thus, the heights of the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and the semiconductor waveguide 136 are substantially the same at this step.

Each of the at least one p-doped semiconductor portion (131, 132) may laterally abut the at least one n-doped semiconductor portion (133, 134). Alternately, a substantially undoped semiconductor material portion (not shown) having the same composition as the semiconductor waveguide 136 may be formed between one of the at least one p-doped semiconductor portion (131, 132) and the at least one n-doped semiconductor portion (133, 134).

Referring to FIGS. 13A and 13B, metal semiconductor alloy regions are formed on the sub-portions of the at least one upper p-doped semiconductor portion 132 and the at least one upper n-doped semiconductor portion 134. Specifically, a first metal semiconductor alloy region 140 is formed on each laterally abutting pair of a first sub-portion of the at least one p-doped semiconductor portion (131, 132) and a first sub-portion of the at least one n-doped semiconductor portion (133, 134). Each first metal semiconductor alloy region 140 is contiguous.

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A second metal semiconductor alloy region 142 is formed on a second sub-portion of each of the at least one upper p-doped semiconductor portion 132. The second sub-portion of each of the at least one upper p-doped semiconductor portion 132 is located on an opposite end of the first sub-portion of that p-doped semiconductor portion 134. In each of the at least one p-doped semiconductor portion (131, 132), a middle sub-portion of the p-doped semiconductor portion (131, 132) that does not underlie a metal semiconductor alloy region separates, and laterally abuts, a first sub-portion of the p-doped semiconductor portion (131, 132) and a second sub-portion of the p-doped semiconductor portion (131, 132). Each of the at least one p-doped semiconductor portion (131, 132) includes a first sub-portion located directly underneath a portion of a first metal semiconductor alloy region 140, a second sub-portion located directly underneath a second metal semiconductor alloy region 142, and a middle sub-portion that laterally separates the first sub-portion and the second sub-portion of that p-doped semiconductor portion (131, 132).

A third metal semiconductor alloy region 144 is formed on a second sub-portion of each of the at least one upper n-doped semiconductor portion 134. The second sub-portion of each of the at least one upper n-doped semiconductor portion 134 is located on an opposite end of the first sub-portion of that n-doped semiconductor portion (133, 134). In each of the at least one n-doped semiconductor portion (133, 134), a middle sub-portion of the n-doped semiconductor portion (133, 134) that does not underlie a metal semiconductor alloy region separates, and laterally abuts, a first sub-portion of the n-doped semiconductor portion (133, 134) and a second sub-portion of the n-doped semiconductor portion (133, 134). Each of the at least one n-doped semiconductor portion (133, 134) includes a first sub-portion located directly underneath a portion of a first metal semiconductor alloy region 140, a second sub-portion located directly underneath a third metal semiconductor alloy region 144, and a middle sub-portion that laterally separates the first sub-portion and the second sub-portion of that p-doped semiconductor portion (131, 132).

The metal semiconductor alloy regions (140, 142, 144) may be formed by depositing an insulator layer (not shown), patterning openings in the insulator layer in areas in which the metal semiconductor alloy regions (140, 142, 144) are to be formed, depositing a metal

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layer, reacting the material of the metal layer with the underlying semiconductor material, and removing unreacted portions of the metal layer. The insulator layer may, or may not, be subsequently removed. The metal layer comprises a metal that reacts with the underlying semiconductor material of the at least one p-doped semiconductor portion (131, 132) and the at least one n-doped semiconductor portion (133, 134). Non-limiting examples of the metal that may be employed as the material of the metal layer include Co, Ta, Ti, W, Ni, Pt, Os, and Ir. In case the underlying semiconductor material comprises silicon, the metal semiconductor alloy regions (140, 142, 144) may comprise a metal silicide. The thickness of the metal semiconductor alloy regions (140, 142, 144) may be from 10 nm to 100 nm, although lesser and greater thicknesses can also be employed.

Referring to FIGS. 14A and 14B, a photoresist 147 is applied over the top surface of the second exemplary semiconductor structure. An opening is formed in the photoresist 147 by lithographic patterning. The at least one first metal semiconductor alloy region 140 is exposed within the opening in the photoresist 147. A portion of the semiconductor waveguide 136 may be exposed within the opening in the photoresist 147. Not necessarily but preferably, edges of the photoresist 147 may overlie the middle sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) and the middle sub-portion(s) of the at least one n-doped semiconductor portion (133, 134).

Portions of the top surface of the buried insulator layer 20 are exposed within the opening in the photoresist 147. The exposed portions of the buried insulator layer 20 are removed from underneath the opening in the photoresist 147 by an etch, which may be an isotropic etch or an anisotropic etch. The photoresist 147 protects covered portions of the buried insulator layer 20 from the etch. The etch is selective to the metal semiconductor alloy portions (140, 142, 144), the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and the semiconductor waveguide 136. A trench is formed within the buried insulator layer 20 underneath the opening in the photoresist 147. A top surface of the handle substrate 10 may be exposed underneath the trench in the buried insulator layer 20.

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The trench may undercut the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and a portion of the semiconductor waveguide 136. Preferably, the undercut of the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and a portion of the semiconductor waveguide 136 is controlled to prevent a complete dissociation from the top surface of the buried insulator layer 20 and to insure that each of the at least one p-doped semiconductor portion (131, 132), the at least one n-doped semiconductor portion (133, 134), and a portion of the semiconductor waveguide 136 remains attached to the buried insulator layer 20. Preferably, the edge of the trench in the buried insulator layer 20 is directly adjoined to the middle sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) and the middle sub-portion(s) of the at least one n-doped semiconductor portion (133, 134). Each of the first sub-portion of the at least one p-doped semiconductor portion (131, 132) and each of the first sub-portion of the at least one n-doped semiconductor portion (133, 134) may laterally protrude from the edges of the trench within the buried insulator layer 20, and overhang above the trench in the buried insulator layer 20. The remaining portions of the buried insulator layer 20 constitute at least one dielectric material portion that vertically abuts the bottom surfaces of the second sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) and the second sub-portion(s) of the at leas one n-doped semiconductor portion (133, 134).

Referring to FIGS. 15A and 15B, the trench in the buried insulator layer 20 is filled with a dielectric material. Preferably, the dielectric material filling the trench in the buried insulator layer 20 comprises a different material than the dielectric material of the buried insulator layer 20. Preferably, the dielectric material filling the trench comprises a low dielectric constant (low-k) material having a dielectric constant less than 3.0. In this case, the dielectric material filling the trench constitutes a low dielectric constant (low-k) dielectric material portion 150. The low-k dielectric material portion 150 laterally abuts the buried insulator layer 20 and vertically abuts the bottom surfaces of the first sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) and the first sub-portion(s) of the at leas one n-doped semiconductor portion (133, 134). The interface between the buried insulator layer 20 and the low-k dielectric material portion 150 may be located underneath

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the middle sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) and the middle sub-portion(s) of the at least one n-doped semiconductor portion (133, 134).

The dielectric material portion of the buried insulator layer 20 comprises a dielectric material having a second edge underlying the middle sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) located between one of the at least one first metal semiconductor region 140 and one of the at least one second metal semiconductor region 142 and having a third edge underlying a middle sub-portion(s) of the at least one n-doped semiconductor portion (133, 134) located between one of the at least one first metal semiconductor region 140 and the at least one third metal semiconductor region 144. Further, the low-k dielectric material portion 150 comprises a dielectric material having a second edge underlying the middle sub-portion(s) of the at least one p-doped semiconductor portion (131, 132) located between one of the at least one first metal semiconductor region 140 and one of the at least one second metal semiconductor region 142 and having a third edge underlying a middle sub-portion(s) of the at least one n-doped semiconductor portion (133, 134) located between one of the at least one first metal semiconductor region 140 and the at least one third metal semiconductor region 144.

Exemplary low-k dielectric materials that may be employed for the low-k dielectric material portion 150 include, but are not limited to, fluorinated or non-fluorinated organic polymer based low k materials such as Dow Chemical's SiLK™ dielectric, Honeywell's Flare™, polyimides, benzocyclobutene, polybenzoxazoles, aromatic thermoset polymers based on polyphenylene ethers, chemical vapor deposited polymers such as poly(p-xylylene), and organosilicate glasses (OSG's) that may be deposited by chemical vapor deposition. Organosilicate glasses contain a matrix of a hydrogenated oxidized silicon carbon material (SiCOH) comprising atoms of Si, C, O and H in a covalently bonded tri-dimensional network, and may be referred to as SiCOH dielectric materials. The low-k dielectric materials may be porous or non-porous. Typically, the low-k dielectric material of the low-k dielectric material portion 150 has less thermal conductivity than the dielectric material of the buried insulator layer 20. The low-k dielectric material portion 150 as deposited may cover the entirety of the second exemplary semiconductor structure. Preferably, the top surface of the low-k dielectric material portion 150 is planar, which may be effected by

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depositing a self-planarizing low-k dielectric material or by planarizing a non-self-planarizing low-k dielectric material layer by chemical mechanical planarization, a recess etch, or a combination thereof.

An optoelectronic device 160 is formed on the top surface of the low-k dielectric material portion 150. The optoelectronic device may be any device that manipulates an optical signal, i.e., electromagnetic radiation. The optical signal may be in the ultraviolet range, in the visible spectrum, in the infrared range, or in a microwave range. The optoelectronic device 160 may include a plurality of devices that manipulate at least one optical signal and may, or may not, be interconnected amongst one another. The optoelectronic device 160 may, or may not, be optically coupled to the semiconductor waveguide 136. In case the optoelectronic device 160 is optically coupled to the semiconductor waveguide 136, the optoelectronic device 160 may manipulate the optical signal that are fed into, or received from, the semiconductor waveguide 136. The optoelectronic device 160 may include at least one of a laser, optical amplifier, an optical sensor, a waveguide, a quantum well, or any other device that may manipulate an optical signal. The optoelectronic device 160 may comprise any semiconductor material that may be employed for the top semiconductor layer 129 as described above. Particularly, the optoelectronic device 160 may comprise a III-V compound semiconductor material such as GaAs, $In_xGa_{1-x}As$, $Al_xIn_yGa_{1-x-y}As$, InP, $In_xGa_{1-x}As_yP_{1-y}$, etc. The range of x, y, and 1-x-y are between 0 and 1. The optoelectronic device 160 may comprise a doped semiconductor material or an undoped semiconductor material.

Optionally, the region of the low-k dielectric material portion 150 that is not covered by the optoelectronic device 160 may be etched by an etch that is selective to the optoelectronic device, the second and third metal semiconductor alloy regions (142, 144), the at least one p-doped semiconductor portion (131, 132), and the at least one n-doped semiconductor portion (133, 134).

Referring to FIGS. 16A and 16B, an interconnect-level dielectric material layer 80 is formed over the optoelectronic device 160 and the exposed portions of the buried insulator layer 20, the at least one second metal semiconductor alloy region 142, the at least one third metal semiconductor alloy region 144, the at least one p-doped semiconductor portion (131, 132), and the at least one n-doped semiconductor portion (133, 134). FIG. 16A is a vertical cross-

sectional view along the vertical plane Z – Z' in FIG. 16B, and FIG. 16B is a top-down view of selected elements including the at least one p-doped semiconductor portion (131, 132), the at least one first metal semiconductor alloy region 140, the at least one second metal semiconductor alloy region 142, the at least one third metal semiconductor alloy region 144, and the semiconductor waveguide 136. The location of the optoelectronic device 160 is shown in a broken line. The interconnect-level dielectric material layer 80 comprises a dielectric material, which may comprise any of the dielectric material that may be employed for the buried insulator layer or the low-k dielectric material portion 150. Additionally or alternately, the interconnect-level dielectric material layer 80 may comprise a doped silicate glass such as phosphosilicate glass (PSG), borosilicate glass (BSG), borophosphosilicate glass (BPSG), fluorosilicate glass (FSG), etc. The interconnect-level dielectric material layer 80 may further include other dielectric materials as well.

A first set of via holes may be formed in the interconnect-level dielectric material layer 80 above the optoelectronic device 160 and filled with a compound semiconductor material to form at least one compound semiconductor via 85. Each of the at least one compound semiconductor via vertically abuts the optoelectronic device 160 and provides conduction of electrical current or transmission of light to or from the optoelectronic device 160.

A second set of via holes is formed in the interconnect-level dielectric material layer 80 above each of the at least one second metal semiconductor alloy region 142 and the at least one third metal semiconductor alloy region 144. At least one first metal contact via 90 abutting each of the at least one second metal semiconductor alloy region 142 and at least one second metal contact via 92 abutting each of the at least one third metal semiconductor alloy region 144 are formed within the second set of via holes by filling the second set of via holes with a conductive metal and removing excess metal from above the top surface of the interconnect-level dielectric material layer 80. The at least one first metal contact via 90 and the at least one second metal contact via 92 comprises a metallic material such as W, Ta, Ti, WN, TaN, TiN, Cu, and Al. Other metallic materials may also be employed instead of, or in addition to, the metallic material described above.

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Each adjoined set of a first metal contact via 90, a second metal semiconductor alloy region 142, a p-doped semiconductor portion (131, 132), a first metal semiconductor alloy region 140, an n-doped semiconductor portion (133, 134), a third metal semiconductor alloy region 144, and a second metal contact via 92 constitutes a temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92). Each temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) is configured to provide a path for conduction of electrical current.

The path for conduction of electrical current may be from a second metal contact via 92, then through a third metal semiconductor alloy region 144, then through an n-doped semiconductor portion (133, 134), then through a first metal semiconductor alloy region 140, then through a p-doped semiconductor portion (131, 132), then through a second metal semiconductor alloy region 142, and then to a first metal contact via 90. This direction of current flow is herein referred to as a forward current direction. Alternately, the path for conduction of electrical current may be from a first metal contact via 90, then through a second metal semiconductor alloy region 142, then through a p-doped semiconductor portion (131, 132), then through a first metal semiconductor alloy region 140, then through an n-doped semiconductor portion (133, 134), then through a third metal semiconductor alloy region 144, and then to a second metal contact via 92. This direction of current flow is herein referred to as a reverse current direction.

Each temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92) is thermally coupled to the optoelectronic device 160, which comprises a semiconductor material and is configured to manipulate electromagnetic radiation, i.e., an optical signal.

As electrical current flows through each of the at least one temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92), heat is transferred in the direction of the flow of the majority charge carrier. This is because the mechanism of Peltier-Seebeck effect is in operation in the at least one p-doped semiconductor portion (131, 132) and the at least one n-doped semiconductor portion (133, 134). According to Peltier-Seebeck effect, heat transfer accompanies diffusion of charge carriers in a semiconductor material and vice versa.

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If the electrical current flows in the forward current direction, the majority charge carriers diffuse away from the interface with one of the at least one first metal semiconductor alloy region 140 and toward the interface with one of the at least one second metal semiconductor alloy region 142 and the at least one third metal semiconductor alloy region 144 within the p-doped semiconductor portion (131, 132) and the n-doped semiconductor region 134 of each temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92). The majority charge carriers are holes in the at least one p-doped semiconductor portion (131, 132), and are electrons in the at least one n-doped semiconductor region 134. The heat is further transferred to the at least one first metal contact via 90 and the at least one second metal contact via 92. Because of the thermal coupling between the at least one first metal semiconductor alloy region 140 and the optoelectronic device 160, the heat is also transferred from the optoelectronic device 160 to the at least one first metal semiconductor alloy region 140 as the at least one first metal semiconductor alloy region 140 is cooled. Therefore, there is a net heat transfer from the optoelectronic device 160 to the at least one first metal contact via 90 and the at least one second metal contact via 92. The heat that is transferred to the at least one first metal contact via 90 and the at least one second metal contact via 92 may further be transferred to a heat sink (not shown) through metallic interconnect structures embedded in the interconnect-level dielectric material layer 80.

If the electrical current flows in the reverse current direction, the majority charge carriers diffuse toward the interface with one of the at least one first metal semiconductor alloy region 140 and away from the interface with one of the at least one second metal semiconductor alloy region 142 and the at least one third metal semiconductor alloy region 144 within the p-doped semiconductor portion (131, 132) and the n-doped semiconductor region 134 of each temperature control device (90, 142, 131, 132, 140, 133, 134, 144, 92). The transferred heat accumulates at the at least one second metal semiconductor alloy region 142 and the at least one third metal semiconductor alloy region 144. Because of the thermal coupling between the at least one first metal semiconductor alloy region 140 and the optoelectronic device 160, the heat is further transferred from the at least one first metal semiconductor alloy region 140 to the optoelectronic device 160 as the at least one first metal semiconductor alloy region 140 is heated by heat transfer. Therefore, there is a net heat transfer from the at least one first metal contact via 90 and the at least one second metal

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